DESIGN, CONTROL, AND IMPLEMENTATION OF A HIGH POWER DENSITY ACTIVE NEUTRAL POINT CLAMPED INVERTER FOR ELECTRIC VEHICLE APPLICATIONS

DESIGN, CONTROL, AND IMPLEMENTATION OF A HIGH POWER DENSITY ACTIVE NEUTRAL POINT CLAMPED INVERTER FOR ELECTRIC VEHICLE APPLICATIONS

BY

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A THESIS

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

AND THE SCHOOL OF GRADUATE STUDIES

OF MCMASTER UNIVERSITY

IN PARTIAL FULFILMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

Doctor of Philosophy (2022) McMaster University

(Electrical & Computer Engineering) Hamilton, Ontario, Canada

TITLE:	DESIGN, CONTROL, AND IMPLEMENTATION OF A HIGH POWER DENSITY ACTIVE NEUTRAL POINT CLAMPED INVERTER FOR ELECTRIC VEHICLE APPLICATIONS
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NUMBER OF PAGES:	xx, 189

To all the brave Iranian women and men who are fighting for Freedom.

To Iman and Mehdi, who will remain in my heart forever.

Abstract

Traction inverter, as a critical component in electrified transportation, has been the subject of many research studies in terms of topologies, modulation, and control schemes. Recently, some of the well-known electric vehicle manufacturers have utilized higher-voltage batteries to benefit from lower current, higher power density, and faster charging times. With the ongoing trend toward higher voltage DC-link in electric vehicles, some multilevel structures have been investigated as a feasible and efficient option for replacing the two-level inverters. Higher efficiency, higher power density, better waveform quality, and inherent fault-tolerance are the foremost advantages of multilevel inverters which make them an attractive solution for this application.

The first contribution of this thesis is to investigate and present a comprehensive review of the multilevel structures in traction applications. Various topologies, as well as modulation and control techniques are explored in this thesis. Based on the major criteria in EVs, a comparison has been made among the well-known and advanced structures and control techniques. Secondly, this thesis proposes an electro-thermal model based on first-order and second-order foster equivalent thermal networks for a designed three-level active neutral point clamped (ANPC) inverter, as well as a modified sinusoidal pulse-width modulation (SPWM) -based technique. This electro-thermal model and the modified SPWM technique enable temperature estimation

in the inverter and minimization of the maximum junction temperature and hence, increase the power density. Based on the experimental results derived from the implemented setup, a 12% increase in power density is achieved with the proposed technique. The other contribution is a reduced-complexity model-predictive controller (MPC) for the three-level ANPC inverter without weighting factors in which the number of calculations has dropped from 27 to 12 in each sampling period.

The improvements to the structure and control system of the inverter are supported by theoretical analysis, simulation results, and experimental tests. A three-level inverter is implemented for 800 V, 70 kW operation and tested. 750 V Silicon Carbide (SiC) switches are utilized in the inverter structure. Finally, future trends and suggestions for the following studies are stated in this thesis.

Acknowledgements

First and foremost, I wish to express my appreciation to my supervisors, Dr. Ali Emadi and Dr. Mehdi Narimani who offered me the valuable opportunity to work in a unique, professional, and successful environment at McMaster Automotive Resource Center (MARC). I sincerely appreciate your guidance, support, and inspiration.

I would like to thank my colleagues, Alex Wang, Jigar Mistry, and Fatemeh Abolqasemi, who contributed greatly in designing and implementing the three-level inverter which was used in this dissertation. Thank you very much for being so helpful, professional, and passionate throughout this project.

My thanks and appreciation to my supervisory committee members Dr. Berker Bilgin and Dr. Babak Nahid-Mobarakeh, for the most valuable contributions and feedback during my Ph.D. studies.

This thesis would not have been done without the sincere helps and advises from my colleagues and friends. Special thanks to Behzad, Sima, Sumedh, Jiaqi, Alex, Diego, Negar, Lucas, Maryam, Rasul, Theresa, Alan, Niloufar, Peter, Wesam, Phil, John, Teresa, Justin, Kevin, and many others who helped me through this path and did not hesitate to spend time and effort to contribute to my success.

I would also like to thank Dr. Farzad Tahami, my Master's supervisor at Sharif University of Technology, who introduced Power Electronics to me and allowed me

to gain hands-on experience in this field for the first time.

The most special thanks to my friends, colleagues, and roommates, Iman Aghabali and Mehdi Eshaghian, who were tragically killed in PS752 flight on January 8, 2020. They left me with a broken heart forever.

My truthful gratitude to my lovely family. You are the reason that I have always tried to be a better and more successful person. Thank you my lovely wife, shadi, my parents, Leyla and Ghasem, my parents-in-law, Azar and Reza, my brother, AmirHossein, my siblings-in-law, Hashem, Yalda, Arash, and Behnaz, and lovely Dena.

This research was undertaken, in part, thanks to funding from the Canada Research Chair in Transportation Electrification and Smart Mobility and the Natural Sciences and Engineering Research Council of Canada (NSERC).

To all the people who supported me in my life, Thank you.

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Chapter 1

Introduction

1.1 Background and Motivation

Electrified transportation has been considered as a promising solution to many issues caused by its gas-fueled counterpart. Greenhouse gas emissions of the transportation sector was 27% share of total emissions in the United States in 2020 [1]. The emission can be either reduced or eliminated by hybrid or pure-electric transportation [2]. Other than the reduction in gas emissions, transportation electrification leads to higher energy efficiency, better acceleration, and less required maintenance [2, 3]. Electric transportation, mostly passenger electric vehicles (EVs), can also contribute to the improvement of power system stability, reliability, and efficiency when they are equipped with bidirectional chargers [4, 5].

Despite the advantages mentioned above, there have always been several non-negligible challenges impeding the fast growth of transportation electrification. Most importantly, long charging time and low maximum driving range of battery-powered electric vehicles (BEVs), trucks, and buses before recharging are still the biggest

challenges for the manufacturers [6].

Recent advancements in li-ion batteries and battery management systems has led to improved range and recharging time of BEVs [7, 8]. Although the increased battery capacity is making the driving range of BEVs more satisfactory, the charging time is still far from being comparable with the refueling time of internal combustion engine vehicles (ICEVs).

A comparison has been made between passenger EVs and ICEVs in [9] in terms of the time required for an 845 km inter-city travel. It is demonstrated that to have comparable travel time between EVs and ICEVs based on current batteries capacities, there is a need for chargers with the power of more than 350 kW. Using extreme fast chargers (XFCs), with the output voltage of at least 800 VDC, is a possible solution for 350 kW chargers [10].

Enabling extreme fast charging is just one of the benefits of moving toward a higher-voltage DC link in electrified vehicles. Besides, employing higher-voltage batteries allows for a reduction in size and weight of the required cables for transferring a certain amount of power [11], or equivalently it helps to increase transferred power using a specified cable size in both BEVs and grid-connected vehicles. Moreover, traction motors operating at a higher voltage for a given power can reduce the motor current and thus achieve higher efficiency [12].

Due to the advantages mentioned above, recently, there has been a trend among manufacturers to move toward higher voltage DC-link in traction drives. Table 1.1 lists some of the commercial passenger EVs, and some of their relevant specifications [10, 13–21]. As can be seen from Table 1.1, Porsche manufactured its all-electric car in 2019, 4 years after unveiling a concept car named Mission E, and named it Porsche

Table 1.1: Specifications of Some EVs Available in the Market (First release year)

Vehicle Model	Year	Motor Rating (kW)	Battery Voltage (V)	Battery kWh	Range (km)
Nissan Leaf	2010	80	360	24	117
Tesla Model S	2012	310	375	60	335
Chevrolet Spark EV	2013	97	360	20	132
Tesla Model X P90DL	2015	397	375	90	375
Audi e-tron	2018	265	400	95	329
Porsche Taycan	2019	460	800	93.4	450
Lucid Air	2020	746	900	120	644
Aston Martin Rapide E	N/A	450	800	65	322

Taycan [22]. This car is capable of being charged with a maximum power of 270 kW at 800 V. With the use of higher voltage DC system inside the car and also in the charger, it takes just 22.5 minutes to recharge its 93 kWh battery from 5% to 80% [23].

Other than Porsche Taycan, Aston Martin Rapide E, and Fisker's EMotion are among the first vehicles which announced utilizing 800 V batteries to exploit its advantages [24, 25]. Lucid Air, manufactured by Lucid Motors will be the first car using over 900 V batteries for further reduction of weight and charging time [15]. Additionally, Hyundai has also announced that it joins IONITY, cooperating with BMW Group, Daimler AG, Ford Motor Company and Volkswagen Group with Porsche AG to enable utilizing 800 V systems in its EVs to use 350 kW charging system[26]. GM has also announced that it will use 800 V batteries with 350 kW chargers for its trucks [27].

Despite all the benefits mentioned, new challenges emerge by moving toward a higher voltage DC link. A higher voltage battery utilizes more cells connected in series. This will increase the cost and the complexity of the sensing and balancing circuits. Furthermore, the insulation requirements will increase which will lead to higher cost and volume of some of the equipment, like charging connectors [28].

When it comes to power electronics, reducing current results in lower conduction loss. However, higher voltage increases switching losses which usually reduce total efficiency if the same inverter technology is used [29]. Therefore, an important challenge is the inverter of the powertrain. A conventional six-switch 2-level inverter with 650 V switches cannot be used efficiently for high voltage DC link. As a result, either the semiconductors or the inverter topology must change. High-voltage semiconductors lead to an increase in the cost and switching losses of the components. Therefore, a possible solution is to use multilevel inverter topologies in electrified transportation to withstand high voltages.

Multilevel inverters are gaining attention in many medium to high-power, high-voltage applications due to their exceptional characteristics. Reduced voltage stress and loss of each individual semiconductor device, better power quality, and lower electromagnetic interference are among the foremost advantages of multilevel inverters. Various multilevel inverter topologies, different modulation schemes, and different control techniques make a wide variety in the selection of the best multilevel structure. The best choice is dependent on the application, load, and requirements [30].

Although employing multilevel inverters in traction drives has been the topic of several studies, they have not been used widely in transportation electrification yet.

While these structures are being used in high-power electric trains [31, 32], other applications like electric trucks, buses, and passenger EV manufacturers have preferred the conventional 2-level inverter due to the simplicity in design and implementation [33]. However, the trend toward utilizing higher voltage batteries makes these structures a more interesting choice to be used both in the off-board charger and in the motor drive.

Although the multilevel structures show some salient advantages, voltage balancing issue, increased number of semiconductors and capacitors, more complex control, and unequal loss distribution in the switches are the most important challenges in these structures [34, 35]. The unequal loss distribution in some multilevel structures leads to the presence of a single hot spot in each converter leg. This will cause a drop in the achievable power density of the drive system. As a result, addressing this unbalance in junction temperatures of switches in a multilevel EV inverter can be critical for power density improvement of the powertrain.

A variety of control and modulation schemes are suitable candidates for multilevel inverter structures. The field-oriented control (FOC) scheme with the well-known, reliable sinusoidal pulse width modulation (SPWM) which is popular due to its simplicity can be modified by adding some control variables in an attempt to address the mentioned issues, including the voltage balancing. The same approach can be taken in case of more complex modulators like space vector modulation (SVM), or advanced, but more complex control schemes such as model-predictive control (MPC).

The first focus of this thesis is to derive methods to improve the maximum power density by reducing the hotspot temperature in a three-level inverter designed for the EV application by modifying the control and modulation strategies based on

the inverter thermal model. Hence, after presenting a comprehensive review on the subject matter, an electro-thermal model is developed for the three-level active neutral point clamped (ANPC) inverter to estimate the junction temperature of the power devices. Then, the power density improvement is achieved using a modified SPWM technique to minimize the junction temperatures. The other goal of this thesis is to develop an MPC controller for the inverter. Due to the large computational burden of conventional MPC controller, it can not be used at high frequency multilevel drives effectively. Therefore, a simplified MPC technique with minimum computational burden is introduced. All proposed techniques are verified using both simulations and experimental results.

1.2 Contributions

There are multiple contributions made by the author in the area of multilevel inverter structures and their control techniques in EV application. These contributions are listed as below:

- Presenting a comprehensive review regarding the recent trends of DC-link voltage in EVs and the application of multilevel structures to address the raised issues, as well as a comparative study of the various topologies, their benefits, and drawbacks in this specific application
- Presenting a comparative review of the modulation and control techniques for multilevel inverters in traction drive applications
- Implementing a compact, high-frequency, 800 V, 70 kW, SiC-based three-level ANPC inverter for EV application

- Introducing two electro-thermal models for the three-level ANPC inverter
- Improving the inverter's power density by 12% by proposing a modified SPWM technique with temperature estimation to ensure junction temperature balancing among the switches in each converter leg
- Proposing an advanced MPC controller for three-level ANPC inverter, featuring reduced number of calculations (27 to 12) and eliminated weighting factors

1.3 Thesis Outline

This thesis aims to propose methods to improve the power density and control simplicity of a three-level SiC-based ANPC inverter, used for high voltage DC-link powertrain of EVs, using both FOC+SPWM and MPC control schemes.

The recent trend in increasing the DC-link voltage of multiple commercial passenger EVs is investigated in Chapter 2. A detailed survey of the advantages of moving to 800 V batteries is presented. These benefits include faster charging, lower conduction loss, smaller and lighter motors, and lower cable weights. On the other hand, either the inverter structure or the semiconductor devices inside the inverter must be changed in order to fit the new breakdown voltage requirements.

In Chapter 3, multilevel inverter topologies are investigated as a suitable option to address the higher input voltage, where the voltage stress on the inverter switches can be divided among multiple devices. There is a variety of multilevel topologies in the literature with different advantages and requirements. Considering the major criteria in EV powertrain, these structures are compared to each other which helps the best topology to be selected.

Moving towards multilevel structures is more than just changing the hardware. Many new concerns arise in these topologies in comparison to their conventional two-level counterparts. Capacitor voltage balancing, unequal power loss, and higher complexity requires a reliable control technique to be adapted. Therefore, Chapter 4 presents a comparative review of the most recent studies on the control and modulation techniques for multilevel inverters by taking into account the specific requirements of traction inverters.

Based on the studies on the available topologies and the specifications which are set for the experimental setup, a compact three-level ANPC is implemented for the purpose of this thesis. Chapter 5 explains the details on the specifications of the inverter, hardware design, and capabilities of the inverter including the utilized semiconductors, capacitors, sensors, protection measures, as well as software specifications including the processor selection, communication protocols, etc. The final cost of the single implemented inverter, as well as its comparison with the cost of a two-level inverter is presented.

In Chapter 6, first, the loss model of a power MOSFET investigated, focusing on the selected SiC MOSFET. Then, the inherent drawback of the NPC inverter in junction temperature balancing and its solution, which is the ANPC inverter, is investigated. Then, a loss model for three-level ANPC inverter is derived which considers all the loss values in the semiconductor devices. This loss model is then used with a temperature estimation algorithm in a second order foster network to predict the junction temperature of the switch in the next sampling period. This estimation is critical when it comes to developing the algorithm to balance the junction temperatures. A survey of the available methods for junction temperature measurement

is also presented. Moreover, at the end of this section, some experimental test results are presented which have been used to extract the thermal characteristics of the inverter.

In order to increase the power density of the inverter using control methods, the well-known SPWM modulation technique has been modified in Chapter 7 in order to consider the temperature balancing of the switches in each converter leg. After presenting a survey on the previous works in this area, the theory of the proposed technique is proved first. Simulation and experimental results are then shown to validate the idea. In addition to power density improvement, this method can be used as an additional protection level to ensure the switches remain in the permitted operating temperature at all load conditions.

In addition to the SPWM modulation, this thesis investigates MPC technique as a substitute control scheme. A finite control set MPC (FCS-MPC), with a cost function formed of multiple terms is utilized in Chapter 8. Other than the basic current control term in the cost function, voltage balancing and temperature balancing terms are also added to the cost function. Moreover, simplifying methods have been applied to reduce the number of voltage vectors that are evaluated at each step. The results of this chapter is also supported with simulation and experimental results.

Finally, the conclusion is presented in Chapter 9. In addition to a summary of results of the thesis, several suggestions have been made in this chapter for future works on this topic.

Chapter 2

Recent Trends Towards High-Voltage DC-Link Electric Vehicle (EV) Drive Systems

This chapter discusses the primary motivation of moving towards multilevel inverters in traction applications, especially EVs. While all current commercial EVs utilize two-level inverters, the higher voltage DC-link makes multilevel structures more practical. In this chapter first, the current market is investigated in terms of DC-link voltage and then, the benefits and drawbacks of moving towards higher voltages is investigated one by one. Finally, the multilevel inverters are proposed to solve some of the issues related to high-voltage batteries.

2.1 Traction Inverters on the Market

Although numerous studies have investigated multilevel structures in different traction applications, the market hasn't relied on these topologies yet, especially in low power applications.

Table. 2.1 shows the maximum DC voltage and the conventional structures in different traction applications. Due to the higher power and input voltage in electrified trains and tramways, three-level solutions are suggested in these applications. While SIEMENS and MEDCOM cover DC voltages of 750 V, 1500 V, and 3000 V with IGBT-based two-level inverters [36, 37], ABB provides Indian Railways, Deutsche Bahn, Swedish State Railways, and Swiss Federal Railways with 3-level IGBT-based traction inverters which resulted in lower stress on the motors, and high energy efficiency [31, 32].

Thyristors and GTOs, due to their high voltage and current ratings, were considered the predominant switching device in high-power traction inverters in the past. However, with the increase of switching frequency, and availability of high-power IGBT switches, GTO-based inverters are being replaced with IGBTs, resulting in smaller, lighter, and more efficient inverters [31, 32, 38].

Two-level voltage source inverters are used as the inverter structure for electric buses with 600 V batteries. Using SiC devices in MEDCOM inverters for electric buses has led to a 40% reduction in size, 30% loss reduction, and significant reduction in noise [39]. In the case of electric buses and heavy traction equipment, multiphase inverters are also an interesting option. For these applications, TM4 has developed multiphase inverters and motors [33].

Currently, all passenger EVs that use 400 V batteries utilize two-level inverters.

Table 2.1: Traction Inverters' Structure on the Market

Application	DC Voltage (V)	Structure	Switching Devices
Trains and Tramways	up to 3000	Two-level or Three-level	GTO, Thyristor, or IGBT
Buses, Trucks	up to 1500	Two-level	IGBT
Passenger EVs	up to 800	Two-level	IGBT, MOSFET

A comprehensive investigation of the inverter structures in well-known EV manufacturers' products is presented in [33]. Due to the low voltage and high currents, Nissan and Tesla are using three and six switches in parallel, respectively, in their two-level voltage source inverters (VSI) [33].

With the recent trend in increasing battery voltages in traction applications, new alternatives are being available. For low-power passenger EVs, TM4, Eaton, and Delphi have developed traction inverters for 800 V input voltage [40–42]. Higher input voltages will also make multilevel structures more attractive due to higher efficiency, especially in high switching frequency [33].

Regarding the switching devices, silicon IGBTs are the most common choice in low-power traction inverters due to well-established technology, availability in required power levels, and low price [33]. Recently, TM4 and Delphi have announced that they are using SiC switches in their designs. TM4 has announced 195 kW/L power density, which surpasses other traction inverters on the market. Other than power density, the quality of output voltage and current has improved due to the significantly increased switching frequency with SiC devices [40, 42].

2.2 Higher DC-Link Voltage: Benefits and Challenges

Most of today's commercial passenger EVs use 400 V batteries to supply the electrical loads inside the car. Electrified trucks, buses, and larger vehicles usually utilize 600 VDC to 800 VDC systems since they require higher power to operate [43]. High-power electric trains utilize 750 VDC to 3 kVDC to reduce the operating currents.

According to Table 1.1, several EV manufacturers have used 800 VDC link for their latest passenger products. Fisker Inc. has announced that its new 800V EV will benefit from lighter and thinner cables, lower weight, less heat generation, lower manufacturing cost, higher power throughput, faster charging, and more efficient motors [44]. This section deals with the motivations and challenges of moving toward a higher voltage system inside electrified passenger and large vehicles.

2.2.1 Cables

Copper is one of the key materials in the electric transportation industry since it is required inside vehicles, in charging stations, and in infrastructure. Inside an electric vehicle, bus, or train, copper is used in the cables, in the electric motor(s), and in the battery packs. A typical passenger EV utilizes about 80 kg copper [45], which is equal to approximately 4% of the total weight of a typical EV. For a typical battery-powered electric bus, the copper weight is about 370 kg [46]. However, it should be noted that these values may be subject to variations in different vehicles due to different characteristics of them.

An important factor in copper weight inside an EV is DC-link voltage. Porsche

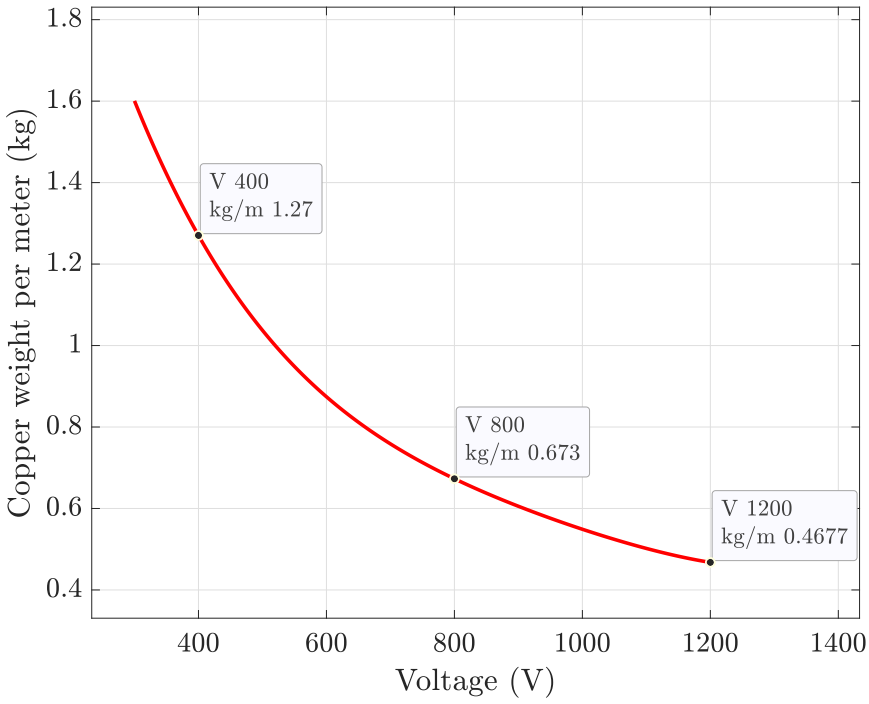


Figure 2.1: Copper weight per meter versus voltage in a 150kW system

says that it has reduced 30 kg from electrical harness due to doubling the battery voltage [47]. According to Fig. 2.1, utilizing 1.2kV instead of 400V in a 150kW system, can reduce the weight per meter of copper by 63% due to the current reduction from 375A to 125A. Moreover, due to the reduced cross-section of the wiring harness from $280mm^2$ to $70mm^2$, higher voltage cables usually show more flexibility for routing which facilitates packaging and manufacturing [43, 48].

Another concern is the weight of the cables which connect the charger to the EV. According to Occupational Safety and Health Administration (OSHA), the weight of the cable should be limited to a maximum of 22.7 kg for a single person to handle. As can be seen in Fig. 2.2, with the conventional 400 V system, or even with an 800V system, the cable's weight for an XFC exceeds the safety limit for 350 kW chargers.

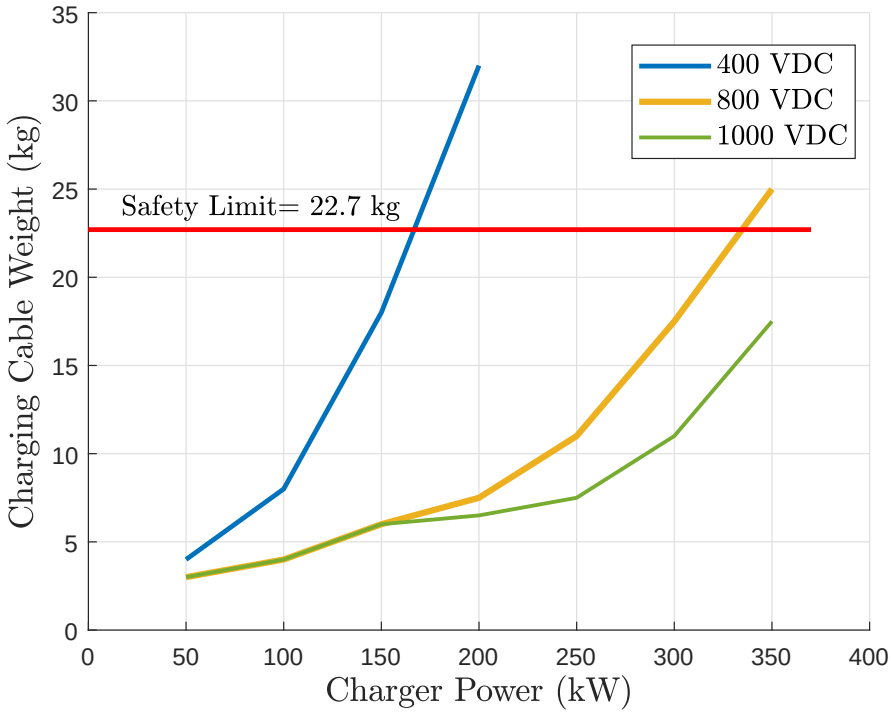


Figure 2.2: Charging cable weight versus charging power with three different DC-link voltages

Utilizing 1kVDC bus voltage ensures that the charging cable's weight remains within the standards [49].

Although the reduction in copper cross-section contributes to the reduction of total cable weight and size, it is not the only involving factor. Increasing system voltage inside an EV poses a need to have a higher level of insulation. According to ISO 6469-3, conventional EVs can be classified in voltage class 2. However, voltages higher than 600VAC or 900VDC are considered in voltage class 3 with a maximum voltage of 1000VAC or 1500VDC. A higher thickness is defined for class 3 cables which results in increasing cable's insulation diameter and cost. This will diminish the effective cable's weight and cost reduction due to increasing voltage [50].

2.2.2 Motors

Although most of the efforts for improving electrified transportation are focused on the batteries, other components like motors can be improved as well [51]. Due to the IDTechEx report, "Electric Motors for Electric Vehicles: Land, Water, Air 2019-2029", a new emphasis will be on the power to weight ratio in EVs [52]. By increasing the motor's rated voltage, its power density can be improved since higher-voltage motors are smaller, faster, and more efficient [53, 54].

2.2.3 Fast Charging

Off-board chargers, without the space and weight limitations of their onboard counterparts, have enabled fast charging of EVs. With the ongoing trend in increasing range and decreasing charging time of EVs, XFCs were introduced to enable even higher-power charging of EVs. The goal of XFCs is to recharge the EV battery from 0% to 80% in a comparable time to the refueling time of ICEVs [13]. The main characteristics of XFCs are 800-1000 V output voltage range and charging power of 350kW or more. Higher charging power mostly benefits long-distance travels and public transportation [9].

The standards of DC chargers have been revised in order to enable fast chargers. CHAdeMO and CCS standards have introduced new voltage/power classes for EV chargers. While CHAdeMO has defined 1kV, 400kW charging level, CCS has a maximum 920V, 350kW level [13]. As the latest update, CHAdeMO in collaboration with China Electricity Council (CEC) have exhibited a new version of an inlet for 900 kW charging power. The new standard will increase the maximum allowed

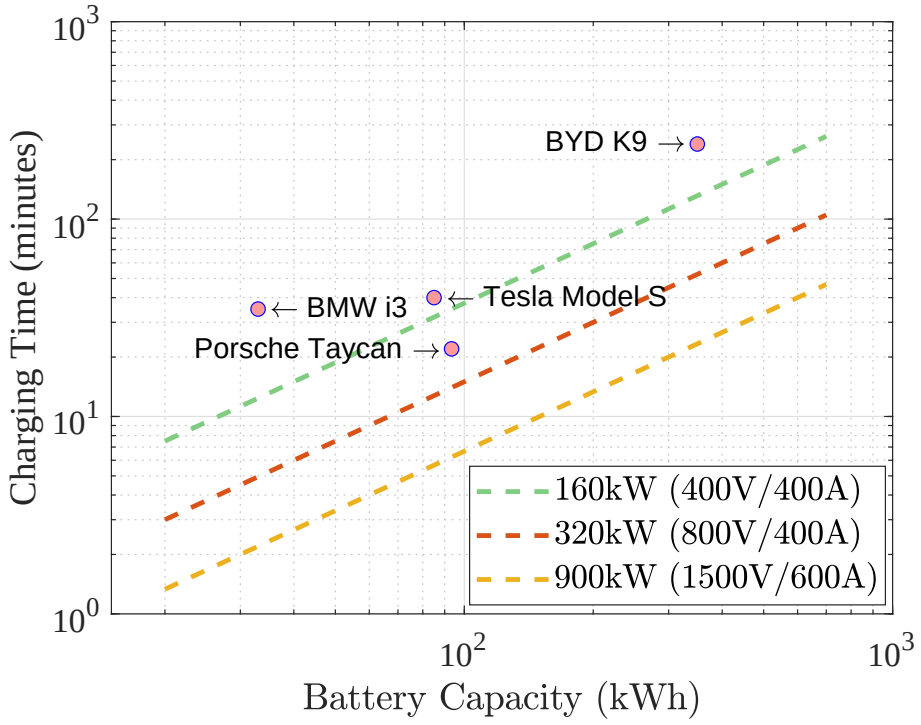


Figure 2.3: Charging times versus battery capacity with different charging powers

output DC voltage to 1500V, and output current to 600A [55–57]. This can be considered as a solution not only for passenger EVs, but also for other types of electrified transportation, like electric buses and trucks.

While the typical charging time of an EV using a 50kW charger is about 80 minutes, the shift to higher voltages can reduce it to about 15 minutes [58]. Fig. 2.3 depicts charging time in some commercial passenger EVs and buses and compares them with feasible charging times using high voltage XFCs. According to Fig. 2.3, an electric bus with a charging time of 4 hours using an 80kW charger, can be charged in 25 minutes using a 900kW charger, or in 70 minutes using a 320 kW charger. The charging time of Tesla model S will also reduce to half using an 800V charger. This can be considered as a huge step toward equal recharging/refueling time in EVs

and ICEVs. However, it should be noted that other than charger system, battery technology and cooling systems need to progress as well in order to enable high-power charging levels.

2.2.4 Batteries

Utilizing higher voltage batteries doesn't affect the total number of cells in a battery pack. However the configuration of series and parallel cells changes [43]; Therefore, there are some challenges that need to be addressed. High current in a battery pack can impact pack hardware, busbars, fuses, disconnect switches, and tabs which results in increasing battery pack cost and weight [59]. On the other hand, a higher-voltage battery pack has higher insulation requirements. Moreover, as the number of series cells increases, cell voltage balancing will be more complex [60]. Additionally, available battery thermal management systems (BMS) and cooling systems are not capable of controlling and limiting the battery temperature during an XFC charging period [61]. Consequently, additional cost would be predictable for the future battery management and cooling systems.

2.2.5 Filters

dv/dt Filtering

High-frequency transitions inside an inverter are unavoidable in order to control the traction motor. However, due to these fast transitions and the existence of parasitic inductances and capacitances, considerable EMI issues emerge in both conducted and transmitted emissions. Due to the typical size and frequency of the inverter, the noise is mainly emitted through the lines and cables. At the inverter output, voltage spikes

may reduce the motor lifetime by damaging the windings, insulation, bearing balls, or rollers [62, 63]. These issues are even more important in the modern inverters which use new IGBTs and MOSFETs with faster transitions. IEC and NEMA have suggested a maximum dv/dt of 500 $V/\mu s$ [64].

An increase in battery voltage leads to the increase of dv/dt value. Consequently, higher levels of filtering must be applied. As wide bandgap (WBG) devices are gaining more attention in power electronics, it should be noted that conversion to high-frequency WBG devices can aggravate the problems of insulation damage and high CM currents due to faster transitions [65]. While the reactor filters and dv/dt filters can be used to reduce the destroying effects of high dv/dt on the motors, high speed transitions in the inverter may also affect other electrical equipment, like batteries [66, 67].

Harmonic Filtering

Voltage harmonics in the output of an inverter give rise to current harmonics. Current harmonics result in torque ripple and higher power loss, especially in the cores. Accordingly, efforts must be made in order to limit the THD value in traction applications. For example, standards have limited the maximum THD in aerospace application to 3% [68]. As long as the motor voltage increase proportionately, increasing the DC-link voltage does not affect THD value due to the constant modulation index value [69]. dv/dt chokes are not useful for harmonic reduction since they are designed to filter high frequencies. Low frequency sine-wave filters are suitable for this purpose [63, 64].

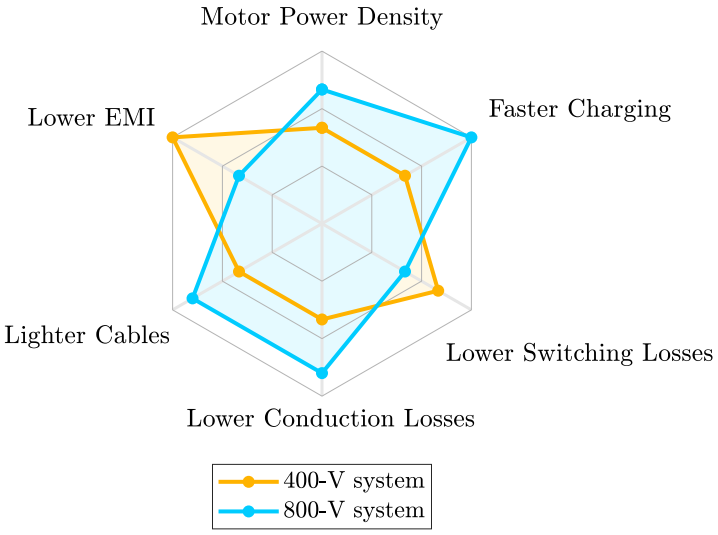


Figure 2.4: Pros and cons of increasing DC-link voltage in traction drives

2.2.6 Other

As mentioned in Chapter 1, higher voltage levels inside a traction drive affects the efficiency of power electronic converters, such as the inverter, due to changing conduction and switching losses. Higher voltage and lower current reduce conduction losses. On the other hand, switching losses increase as a result of increasing the DC input voltage. Moreover, moving to higher voltages affect the sensors, especially current and voltage sensors. Higher galvanic isolation is needed [70] which increases the cost of voltage sensors.

2.3 Summary

Fig. 2.4 summarizes the comparison of a 400 VDC traction drive versus its 800 VDC counterpart. Although high DC-link voltage offers several attractive advantages,

higher EMI, higher switching losses, and larger voltage stress on the switches are three non-negligible drawbacks. Multilevel inverters can compensate these two drawbacks by utilizing low-voltage switches and reducing dv/dt transitions. Consequently, the next chapter of this thesis deal with a review and comparison of multilevel topologies in traction application, their advantages and disadvantages.

Chapter 3

Multilevel Inverter Structures for EV Powertrain Applications

Facilitating higher voltage powertrain in EVs is the major motivation to examine and investigate multilevel inverters. This section presents a comprehensive literature review of both well-known and new multilevel structures and compares them based on the EV requirements.

3.1 Multilevel Inverter Topologies in Traction Drives

In the past decades, many conventional two-level voltage source inverters are replaced by their multilevel counterparts, mostly in medium to high-voltage applications in order to gain lower current and voltage THD, lower EMI, higher efficiency, and lower voltage stress on devices [71, 72]. Moreover, some multilevel topologies benefit from modularity and fault-tolerance [71] which makes them even more interesting in particular applications. On the other hand, the capacitor voltage balancing, suppressing

circulating currents, lack of integrated multilevel power modules on the market, and reduced reliability due to higher number of devices and capacitors are the challenges that need to be addressed when approaching multilevel converters [73, 74].

Utilization of multilevel inverters in traction drives was first proposed in 1988, where a three-level GTO-based neutral point clamped (NPC) was proposed as an efficient substitute for two-level inverters of locomotives' induction motors [75]. One decade later, this topology was implemented in a back-to-back structure and tested successfully by Siemens AG for the TRANSRAPID propulsion system in Emsland [76].

In 2005, a cascaded H-bridge (CHB) converter was proposed as a front-end rectifier for AC-fed traction drives which has a modular and scalable structure [77]. Flying capacitor (FC) multilevel converter is also proposed in the same application [78].

In 2016, a six-level NPC inverter, using selective harmonic elimination (SHE) technique was designed and implemented as a traction inverter for the railway with an input DC voltage of 1500V. It is shown that the efficiency has increased by at least 5% comparing to the conventional two-level converters in industry [79]. Another application of multilevel converters in railway traction drives is proposed by [80], where modular multilevel converters (MMC) is used to store the regenerative energy of the train inside low-voltage supercapacitor cells which resulted in a more efficient energy storage system comparing to two-level designs. In [81], an MMC-based railway power supply system is proposed. Improved power quality, increased modularity, and scalability make this configuration superior comparing to the conventional traction supply system.

Multilevel inverters have also been suggested as an option in ships, where high

power quality, high power density, and fault tolerance are mandatory [71]. Load commutated inverters and cycloconverters, which are the dominant solution in ship propulsion system due to high efficiency and low size, suffer from poor input current quality which will disturb the on-board ship power system [82]. Due to these power quality issues, the DC shipboard power system has become more attractive [71]. Medium-voltage DC-link inside the ship enables the utilization of multilevel inverters for the propulsion. In comparison to other solutions in ships, multilevel converters offer higher power quality, lower insulation stress, and lower over-voltage on motor terminals [83, 84].

In low-power, low-voltage electrified transportation, such as passenger EVs, multilevel inverters have been the topic of several studies as well. In 1998, cascaded multilevel inverter was suggested for the first time as a suitable choice for all-electric high power heavy-duty trucks and military combat vehicles, since they facilitate using higher voltage motors [85].

In [86, 87], MMC inverter is recommended for EV in order to eliminate the need for BMS. One battery cell is connected to each module of the inverter. Consequently, the voltage balancing of cells is ensured without using a BMS. However, in practice, either large number of modules or a step-up transformer is required in order for this topology to be used in commercial EVs.

An integrated bidirectional charger/inverter, based on a 10-level CHB inverter is presented in [88], where a maximum voltage and current THD of 1% is achieved due to the high number of levels. In [89] a dual PMSM motor is driven using a dual T-type NPC (TNPC) converter which resulted in over 90% reduction in DC-link capacitors. [90] presents a method for having low frequency output currents in an MMC inverter

which is suitable for variable frequency drive applications like traction application. A 23-level asymmetrical CHB (ACHB) using only one DC source is presented in [91], where a high-frequency transformer is used in order to provide isolated voltage sources.

In an effort to reduce the number of components in multilevel inverters, a new topology, called nested neutral point clamped (NNPC), was proposed in [92]. Fewer diodes and floating capacitors compared to NPC and FC topologies respectively, makes it an interesting option regarding the size and cost of the inverter. Three-level T-type inverter is also introduced which benefits from fewer components and lower conduction losses. However, it requires high-voltage switches and suffers from high switching loss [93].

A multi-source inverter topology based on three-level NPC and T-type inverters is proposed for hybrid and plug-in hybrid EVs. Unlike conventional multilevel structures, the two input voltage sources of the proposed multi-source inverter are independent. This configuration has resulted in a higher-efficient powertrain and a smaller DC/DC boost converter [94]. In [95], an NPC inverter with multi-battery input is proposed which is capable of balancing the state of charge (SOC) of the battery packs by controlling the flow of energy from the batteries to the load.

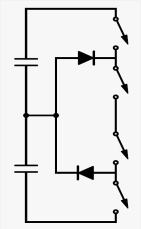
Different topologies of multilevel inverters for multiphase drives (MPD) have also been investigated in the literature [96]. However, these multilevel structures for MPDs are developed for industrial drives, not for electrified transportation [96].

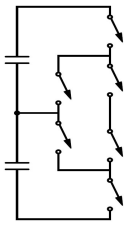
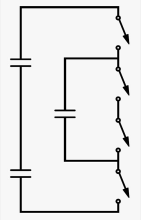
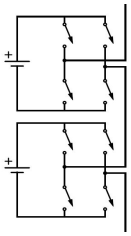
In spite of the studies that have been conducted in this area, all commercial EV drives are based on conventional two-level inverters [33]. However, due to the discussion in Chapter 2, there is a trend toward higher DC-link voltage in EVs which

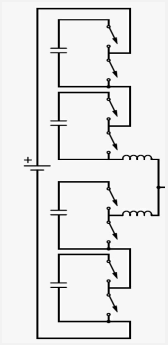
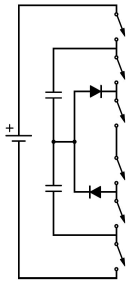
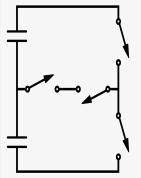
makes multilevel inverters more attractive for use in commercial products.

As mentioned before, there are various multilevel topologies with different characteristics that make them suitable for different applications. The selection of the best topology of multilevel converters totally depends on the application and its specific requirements [72]. Traction drive application, likewise any other application, has its own specific requirements. The following subsections deal with a review of the most important requirements of traction drives which affect the selection of the best topology. Based on these requirements, Table. 3.1 compares well-known topologies.

Table 3.1: Comparison of Famous Multilevel Topologies

Topology	Schematic	Advantages	Disadvantages
Neutral Point Clamped (NPC)		+ No floating capacitors + Simple design + No need to isolated DC sources + Low cost and compact in 3-level structure + Fault-tolerant	- Increased cost and reduced reliability as number of levels increase due to drammatical increase in number of diodes - Unequal loss in switches

Active Neutral Point Clamped (ANPC)		+ No floating capacitors in 3-level structure + Loss balancing capable + Simple design + No need to isolated DC sources + Low cost and compact in 3-level structure + Fault-tolerant	- Increased number of floating capacitors as levels increase - More complex control than NPC - Different voltage rating of power switches at higher levels
Flying Capacitor (FC)		+ efficient in higher level structures + No need to isolated DC sources + Fault-tolerant	- Numerous floating capacitors - Complex control - Large stored energy - High voltage ripples at low frequencies - Voluminous and heavy - Numerous of voltage sensors - Low reliability
Cascaded H-Bridge (CHB)		+ Reliable and fault-tolerant + Modular + No floating capacitors + Simple control	- Isolated DC sources are needed which is not provided in grid-connected traction applications - Increased number of power switches

Modular Multilevel Converter (MMC)		+ Reliable and fault-tolerant + Modular + Scalable + No need to isolated DC sources	- High number of floating capacitors - Complex control - Pre-charging circuits for the capacitors - High stored energy in capacitors - High voltage ripples at low frequencies - Voluminous and heavy - Requires lots of voltage sensors - Circulating Currents
Nested Neutral Point Clamped (NNPC)		+ No need to isolated DC sources + Fewer capacitors comparing to FC + Fewer diodes comparing to NPC	- All of the issues related to floating capacitors - Unequal voltage sharing on switches at levels higher than 4
T-type Multilevel Inverter		+ No floating capacitors + No diodes + Simple control + No need to isolated DC sources	- Requires high-voltage switching - Low efficiency due to high-voltage switches

Cost and Size

Since cost and size are the two important challenges for EVs, in 2017, the US Department of Energy (DoE) has updated its requirements of EV electrical components. For the inverter and the boost converter if applicable, the targets for cost and size are 2.7 $/kW and 100 kW/L respectively, which shows 18% and 87% change compared to the 2020 targets [97]. Consequently, the cost and size of different topologies have to be considered prior to selection.

The capacitors are the most voluminous parts in the traction inverter [33]. Moreover, low-frequency operation of traction drives increases voltage ripple in floating capacitors of the multilevel structure [90], necessitating higher capacities. As a result, the topologies with more floating capacitors are more voluminous than others [98]. From the cost point of view, since diodes and switches are usually more expensive than capacitors, topologies with a large number of switches and diodes are more expensive, especially in a large number of levels [69].

Issues Related to Floating Capacitors

Other than cost and weight, an increased number of floating capacitors is also discouraging since they increase the complexity of the control system. The voltage balancing of these capacitors requires plenty of isolated voltage sensors [99]. Additionally, each capacitor needs to be pre-charged in order to ensure equal voltage sharing on devices from the beginning [100]. Low reliability of the capacitors will also reduce the total reliability of the inverter.

Isolated DC Sources

Isolated DC sources are available in BEVs from the battery packs. However, changes must be made to the battery pack to split it into isolated sources. Consequently, CHB multilevel inverter is also a choice for BEVs [101]. However, additional measures are required to ensure the equal share of battery packs in feeding the motor. On the other hand, modularity and scalability, which are demanded in many industrial applications as well as traction drives [71], can be obtained using CHB or MMC inverters. In large automotive electric drives, CHB inverters can be a suitable choice because of the large number of battery cells [102].

Fault-Tolerance and Reliability

Another comparison criterion is fault-tolerance capability and reliability in different topologies. Since various failures may occur inside the propulsion system of an electrified vehicle, continuity of operation is of great importance [103]. Therefore, fault-tolerance is identified as one of the requirements of the propulsion system of EVs including motor drive in ISO 26262, mainly in limp-home mode [71].

Considering the increased number of capacitors and semiconductor devices in multilevel converters, the reliability of multilevel inverters seems to be low. However, intrinsic fault tolerance in some multilevel topologies increases the reliability of these inverters [74]. A comparison of reliability has been conducted in [104] between FC, NPC, and CHB structures. The large number of capacitors has resulted in the highest failure rate for FC structure, while CHB has the highest reliability between the three.

Based on the above criteria, a comparison of the most well-known classic and advanced multilevel inverter topologies in EV application can be found in Table 3.1.

3.2 Comparison of Multilevel Inverters vs. Two-Level Inverters for Traction Drives

This section deals with a comparison of Multilevel and two-level structures in terms of 7 major criteria in EV drives; Efficiency, cost, power density, power quality, reliability, fault tolerance, and cooling system.

3.2.1 Efficiency

The efficiency of a traction inverter not only affects the power consumption and battery discharge rate, but also impact the thermal design of the system. A more efficient inverter topology can be manufactured in a smaller footprint since the heatsink and cooler system size can be reduced. Consequently, an important criterion to compare different structures is efficiency.

A CHB multilevel inverter using low voltage Si MOSFETs is compared with two-level IGBT and SiC MOSFET based inverters [105]. For a realistic comparison, the authors have used the inverter structures in a verified EV model, with less than 2% error in estimating the energy consumption. Efficiency maps of the three options, which have been verified using ANSYS Simplorer, are used to model the inverter inside the EV model. The first difference of the three inverter structures appears in the low-speed range of the motor, where the minimum efficiency of the inverter has increased from 70% in IGBT-based two-level inverter to 92% in the MOSFET-based CHB inverter.

In higher speeds, multilevel inverter's efficiency still higher than two-level IGBT-based inverter by 2%-3%. The EV model has been simulated in different standard

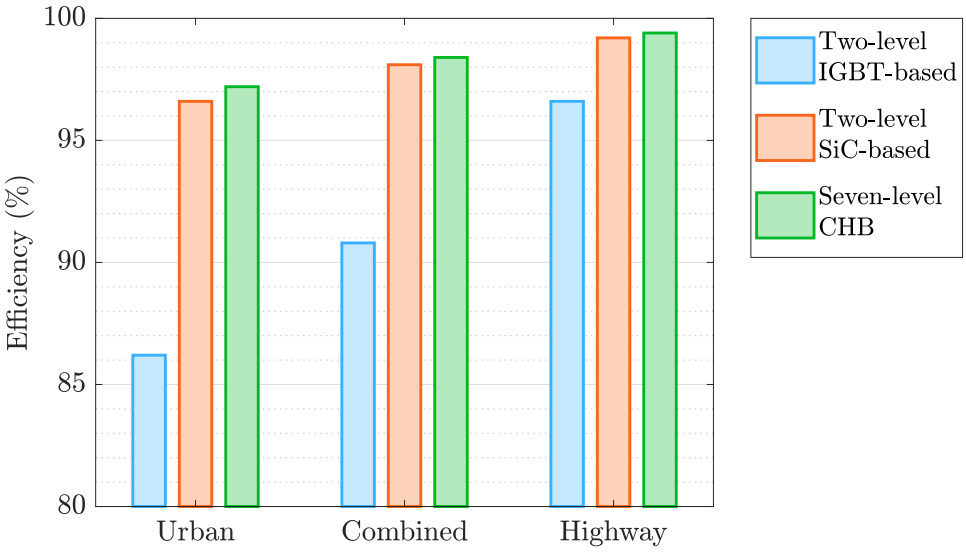


Figure 3.1: Comparison of efficiency between two-level and 7-level structures

driving cycles with different characteristics. In highway driving cycles, MOSFET-based multilevel structure has improved the efficiency by 2%-3%, since the speed is high in most of driving cycle points. On the other hand, for urban driving cycles, the efficiency has been improved by approximately 10% due to the lower speed of the vehicle and motor. It should be noted that the SiC two-level inverter has similar conduction loss with Si multilevel inverter, while the switching loss is slightly larger in the former [105]. The results of the mentioned study are shown in Fig. 3.1.

Moreover, due to lower output current THD with multilevel inverters, motor efficiency also benefits from this structure [106], leading to increased system efficiency. It is shown in [107] that 3.41kWh energy per 100km is saved in urban cycles by using CHB inverter instead of the conventional one. In the highway cycles, the amount of energy saving has been reduced to less than 1kWh per 100km.

In another research, MMC inverter for EVs is evaluated from the efficiency point of view [108]. In the proposed structure, each of the submodules is connected to a battery

cell. Consequently, the SOC of each cell can be controlled separately using proper control and modulation technique, eliminating the need for a BMS. The authors have developed a loss model for MMC, which is then verified using simulation and experimental results. In a comparison of MMC and two-level inverter with different drive cycles, the former has shown increased efficiency, especially in urban cycles.

In all of the aforementioned studies, the switching devices for the multilevel topology are MOSFETs. An important factor in the efficiency increase of low-speed operating points is the physical behavior of MOSFET [107]. However, with the increasing DC-link voltage in traction applications, multilevel IGBT-based inverters using IGBT modules is also an alternative to two-level inverters, especially in heavy-duty applications. By comparing same-technology IGBTs with different rated voltages, it can be resulted that a series connection of two low-voltage IGBTs in a multilevel inverter will have less power loss than a single high-voltage IGBT in a two-level structure. Although the conduction loss increase in the former structure, the sum of switching losses will decrease in a way that the total efficiency usually increases. Consequently, the higher the switching frequency is, the more superior the multilevel inverter is [35].

Although the above results are for EVs, it can be extended to heavy-duty electrified transportation as well. Multilevel MOSFET-based inverters can increase efficiency significantly in urban electric buses or trains since they operate at low speeds for a considerable portion of the time. On the other hand, efficiency increase in intercity transportation is less significant due to the constant, and close to nominal speed.

3.2.2 Power Quality

As mentioned before, the values of output voltage and current THD reduce considerably by using multilevel inverters. The amount of THD reduction depends on the operating point of the traction inverter which determines the modulation and frequency indexes. However, it can be seen that in a typical operating condition, output current and voltage THD reduce by a factor of 2-3 by using a three-level multilevel inverter [69].

Moreover, high dv/dt transitions in two-level inverters cause voltage spikes, arcing, leakage currents, and sparks which can cause the bearing balls or rollers to fail. The problem of high dv/dt is not limited to damaging the motor. The interference from long power cables inside the vehicle can be coupled to low-voltage circuits in the vehicle. Current trend toward higher-voltage DC-link will intensify this issue. Although using shielded cables can mitigate radiated EMI, it can't decrease the conducted emissions [63]. EMI filters and ferrite ring cores can be used in order to reduce the damaging effects of this high frequency interference in traction inverters [63, 109]. However, it is well-known that passive components increase the cost, volume, and weight of the traction system. Multilevel inverters can decrease dv/dt and reduce or eliminate common-mode (CM) voltages [110] on the motor side which results in reduced EMI, increased motor lifetime [111], and eliminating the need to use different types of filters. For example, a 5-level NPC inverter reduces the maximum dv/dt and CM voltage value by four times.

Table 3.2: Multilevel vs Two-level System Cost Comparison

Costs	Two-level Inverter	7-Level CHB Inverter
Switches	296.6	203.4
Gate Drivers	39	234
Capacitors	30.3	0
Heatsink	17.3	16.2
Controller	150	300
Battery	5760	5310
Contactor	74	180
Overhead Cost	133.3	188.6
Sum	6500.5	6433.3

3.2.3 Cost

Cost reduction, as an important objective of the future electrified transportation, plays an important role in selection of the inverter structure. Utilizing multilevel inverters affect the cost of traction drive. However, based on the side-effects of these converters, changes are not limited to the inverter. In what follows, cost alterations in the inverter and other devices are discussed.

Based on the introduced models in [112, 113], a cost comparison is made between a two-level IGBT-based traction inverter and a 7-level CHB inverter in [105]. Other than the inverter cost, the authors have considered the cost saving in the battery by using the multilevel structure. Since the multilevel inverter has found to be more efficient in the same research, the vehicle is capable of maintaining same driving range with a lower battery capacity. The results of the comparison is shown in Table. 3.2. It can be seen that although the inverter cost is higher in case of 7-level CHB structure, overal system cost has been slightly reduced by using multilevel inverter.

Table 3.3: Multilevel vs Two-level System Cost Comparison

Costs	Two-level Inverter	Three-Level NPC Inverter
Switches	204	216
Fast Diodes	0	72
Capacitors	90	90
Heatsink	400	400
Controller	150	300
Gate Drivers	60	120
Filter	842	640
Sensors	80	90
Sum	1726	1678

Another comparison has been made in [35] between a conventional two-level inverter with a three-level NPC inverter. The switching devices in both inverters are IGBTs. The authors have considered the price of IGBTs, fast diodes, voltage sensors, heat sink, gate drivers, control system, DC-link capacitors, and filters as can be seen in Table. 3.3. This comparison doesn't include battery price, therefore it can be valid for grid-connected electrified transportation. It can be seen that reduced filter cost has resulted in a 3%-5% lower system cost in case of three-level NPC inverter.

3.2.4 Fault-Tolerance

While the common solution for fault-tolerant two-level inverters is to add a fourth leg, multilevel inverters usually offer inherent fault-tolerance due to larger number of semiconductor devices and redundant switching states for voltage space vectors [114].

In multilevel inverters, the faulty cell or switch can be bypassed using a bidirectional switch in order for the operation to continue with a reconfigured modulation

without adding any auxiliary cell or switch to the inverter. A fault diagnosis technique, capable of detecting and locating the short-circuit and open-circuit faults is proposed for CHB inverter in [115]. The proposed method can detect the fault in six cycles using the output phase voltage data. Special modulation schemes for fault-tolerant FC [116], NPC [117–119], and MMC [120] topologies are also investigated in the literature.

Although multilevel inverters offer intrinsic fault-tolerance, the voltage rating of the devices should be selected in a way that the healthy cells or devices can tolerate the DC voltage after bypassing the faulty cell or device, at least with a derated operation.

3.2.5 Reliability

At first glance, it seems that a larger number of power devices, drivers, and capacitors in multilevel structures compared to two-level inverters leads to a large difference between the reliability of the two options. However, the intrinsic fault-tolerant capability of most of the multilevel inverters reduces the gap. Authors have investigated this issue in [74] for two, three, and five-level inverters. It is resulted that by including one fault-tolerant capability, the gap between *R(t)* function of three structures remains below 0.2 for 0-25000 hours of operation. Moreover, by including multiple fault-tolerant capability, the reliability of multilevel topologies surpasses two-level inverter. Moreover, since cabling, control electronics, and fan failures have a higher failure rate than semiconductors, the higher efficiency of multilevel inverters increase reliability by reducing the temperature inside the system [35].

3.2.6 Cooling System

Increased efficiency of multilevel inverters offers a simpler and lighter cooling system. Additionally, due to the power loss division among multiple switching devices, the cooling system benefits from a more uniform loss distribution comparing to the conventional inverters. However, two-level inverters can also achieve this advantage through using parallel switches to divide the power loss.

3.2.7 Power Density

The power density of the multilevel inverter structure depends on the selected topology. As mentioned in section 3.1, topologies with floating capacitors have lower power density comparing to the other multilevel inverters. However, other topologies show an increased inverter power density due to the smaller cooling system. An important note to mention here is that, a lack of suitable industrial multilevel power modules on the market and the essence of using discrete devices, especially in low power ratings leads to larger footprint in multilevel inverters. Therefore, with the current available power modules on the market, the power density increase in multilevel structures can be realized mainly in high-power electric transportation where half-bridge modeles can be used in the multilevel structure.

Other than the inverter power density, the power density of the system benefits even more. With the decrease of output voltage THD and EMI, the volume and the weight of the filters reduce. Smaller required battery capacity also contributes to the increasing power density of the system.

A comparison of all the mentioned criteria is shown in Fig. 3.2.

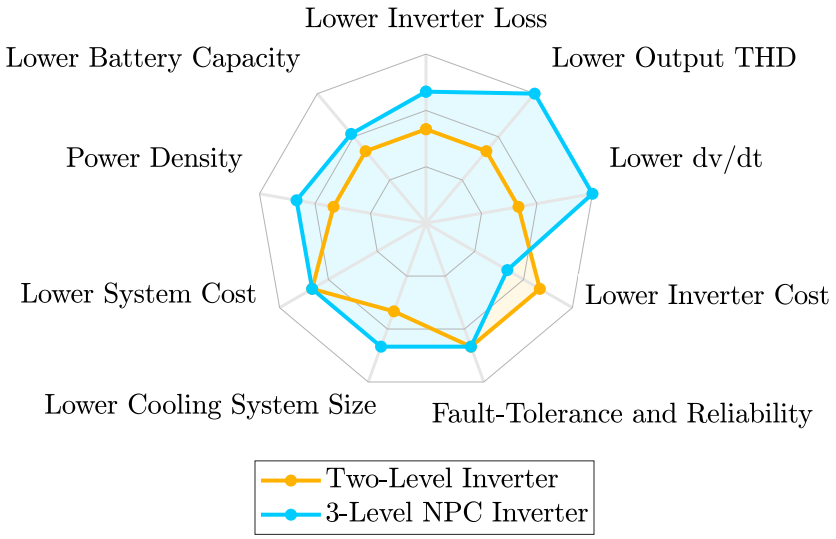


Figure 3.2: Comparison of different criteria in two-level and three-level NPC

3.3 Summary

Multilevel inverters operate at higher efficiency compared to their two-level counterparts, especially when the motor is operating at low speeds, like urban cycles for EVs. In a comparison of cost, multilevel inverters are usually more expensive than their two-level counterparts. However, considering the savings in the cost of battery, filters, and heatsink results in an almost equal price for the two structures. Lower $\frac{dv}{dt}$ reduces the EMI in the drive system. In terms of reliability, although the high number of components in multilevel inverters lowers the reliability, the intrinsic fault-tolerance of multilevel structures compensate the lower reliability.

A comparison of different multilevel topologies was conducted in this chapter. Requirements of traction application establish the criteria for selection between the various options. Topologies with a large number of floating capacitors, like FC and MMC, are discouraging since capacitors are bulky, unreliable, and add complexity

to the control circuit. On the other hand, NPC topology is not cost-efficient if the number of levels goes higher than 3. CHB topology can be used in battery electric vehicles, trucks, and buses in case of re-structuring the battery pack into smaller isolated packs.

Chapter 4

Control and Modulation of Multilevel Inverters in Traction Applications

As mentioned in Chapter 1, multilevel inverters face some challenges such as voltage balancing, control complexity, etc. Addressing these challenges require the best control and modulation techniques to be utilized. Hence, this chapter presents an overview of the modulation and control techniques for multilevel structures, while focusing on the application of EVs and traction drives.

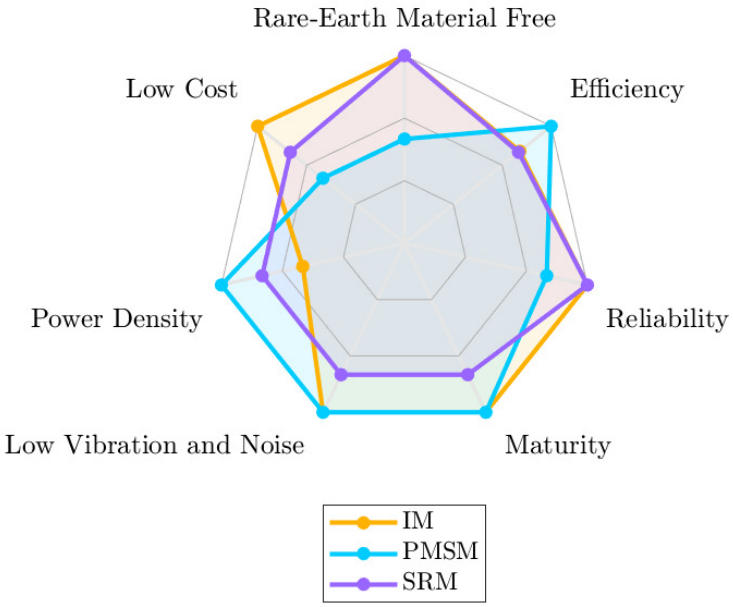


Figure 4.1: A Comparison of IM, PMSM, and SRM for EVs and HEVs

4.1 Control and Modulation Techniques in Motor Drives

Different types of machines including DC machines, interior permanent magnet synchronous machines (IPMSM), induction machines (IM), and switched reluctance machines (SRM) are being used in traction applications. Constant power speed range, power density, efficiency, and required permanent magnet materials are some of the main criteria in choosing the best machine for each application [121]. Due to the different dynamic equations of the current in each of the aforementioned machine types, control parameters and equations differ in each [72, 121, 122]. A comparison of three motor types in EVs is presented in Fig. 4.1.

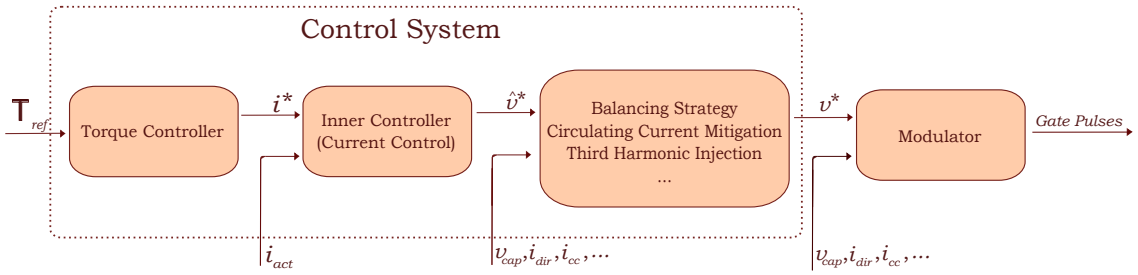


Figure 4.2: General structure of a multilevel drive control and modulation system

Despite various control and modulation techniques for different machines in traction applications, there are usually four general stages in the operational structure of a conventional cascade-controlled multilevel drive: Outer control loop, inner control loop, modulator, and a mid-stage which mostly deals with the capacitor voltage balancing issue [72].

The outer control loop, or the primary controller, controls the torque of the motor and feeds the current reference into the inner control loop. In a conventional drive application, the external control loop, which is also called speed controller, is normally a PI controller [123]. Advanced speed control strategies like adaptive PID controller for IPMSM [124] are proposed in order to improve the operation of the external control loop. However, due to their complexity, manufacturers have not shown interest in complex speed control methods [125].

As mentioned above, the objective of the secondary controller is to follow the output of the primary controller, which is usually current in the case of the traction inverter application. The dynamic equations of the output, which differ based on the motor type, need to be determined for designing the inner control loop [72, 126]. Various control schemes can be used in this stage. Scalar controllers for drives, like the V/f control scheme, only control the magnitude of variables and are the simplest

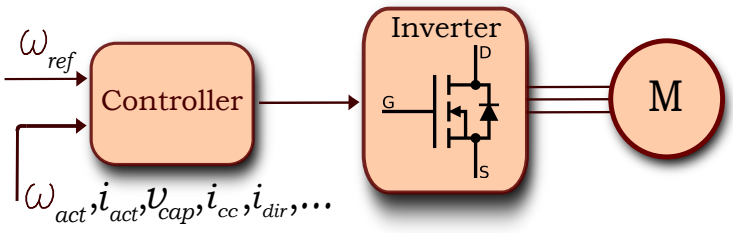


Figure 4.3: Control System with implicit modulator

control methods to be implemented [127]. Due to their poor dynamic response, scalar control methods are not suitable for traction drives. Therefore, field-oriented control (FOC), which is a vector control method and offers higher accuracy, better dynamic response, and ease of implementation in microprocessors [128] is a better fit for this application. FOC has been applied to multilevel-based drives in the literature [129, 130].

Before applying the reference voltage into the modulator, additional measures need to be taken into account. Although other stages are present in both two-level and multilevel inverters, the third stage plays a vital role in multilevel inverters. The injection of a third harmonic voltage into the reference voltage balances the DC-link capacitor in NPC structure [131], increases DC-link utilization, and reduces the common-mode voltage[132]. Moreover, this stage can perform in-phase capacitor charge balancing strategies applicable to MMC and CHB inverters [72].

The modulator stage provides gating signals for the multilevel inverter switches based on the output of the third stage. The generated output gate signals ensure proper control of the fundamental output voltage waveform which is essential for accurate control of the traction motor [133]. Similar to the selection of the topology and control method, choosing the best modulation scheme for multilevel inverters is a key step in each application [10]. Power loss, output THD, and complexity of

implementation are dependant on the selected modulation technique [72]. Generally, modulation techniques for multilevel converters can be classified into carrier-based modulation (SPWM), space vector pulse width modulation (SVPWM or SVM), and selective harmonic elimination (SHE) modulation techniques. Several papers have investigated and compared different modulation techniques for multilevel converters with the pros and cons of each of them [30, 134–137].

Additionally, there are other control methods, direct torque control (DTC) and model-predictive control (MPC), which offer an implicit modulator, shown in Fig. 4.3. A switching table is used in these methods instead of the modulator. Due to removing the modulator, these control schemes offer simpler implementation and better dynamic response [133, 138]. However, their complexity grows with increased number of levels [126]. In [139], a control strategy based on DTC is investigated for flying capacitor inverter in order to balance capacitor voltages and controlling the motor simultaneously. A good example of the superiority of MPC over conventional control schemes is the MMC inverter, where multiple control objectives need to be satisfied at the same time [140]. MPC is also offered in traction application with a field-weakening algorithm for induction motor of an EV [141].

Classification of the control and modulation techniques are presented in Figs. 4.4 and 4.5, respectively. Further investigation and comparison of these techniques, with focus on multilevel traction inverters is presented in Sections 4.3 and 4.4.

4.2 Selection Criteria

As mentioned, proper selection of control and modulation techniques for a multilevel drive is essential since each technique has different characteristics. An investigation of

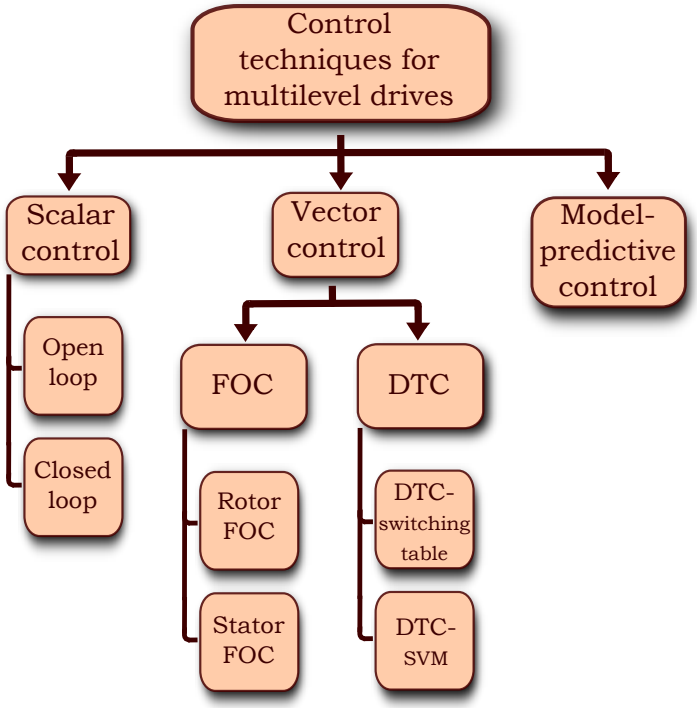


Figure 4.4: Classification of the most popular motor control techniques

the most important criteria for selection of the best control and modulation methods in traction applications is presented in this section. Fig. 4.6 shows the most important criteria in this application.

4.2.1 Dynamic Response

An essential characteristic of a suitable control system in traction applications is the fast dynamic response of the machine to torque demand [142, 143]. In a comparison of an electric machine with an internal combustion engine (ICE), the former should be several times faster than the latter in responding to torque demand changes. Fast response also ensures proper regulation slip-speed ratio [121]. In addition to the fast response to a step torque demand, meeting the maximum required torque ramp is

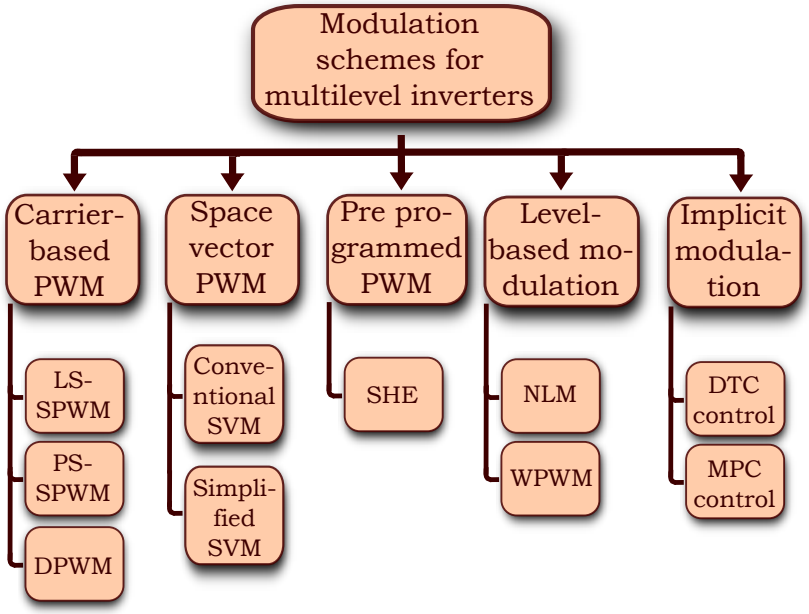


Figure 4.5: Classification of the most popular modulation schemes

essential when the motor is operating in the field-weakening region [144].

4.2.2 Voltage Balancing and Low-Frequency Operation

In traction applications, low-speed operation of the motor is pretty common. This mode of operation causes voltage unbalances in the capacitors of the multilevel inverter. These voltage fluctuations become more considerable as the frequency decreases [145]. Since this issue is more considerable in topologies with floating capacitors, special modulation and control techniques have been proposed for these inverters. Without a suitable voltage balancing strategy, the size of the capacitors in the multilevel structure increase. In the structures where the battery cells are connected separately to each sub-module, the state of charge (SOC) of battery cells need to be balanced with a proper controller [86, 146].

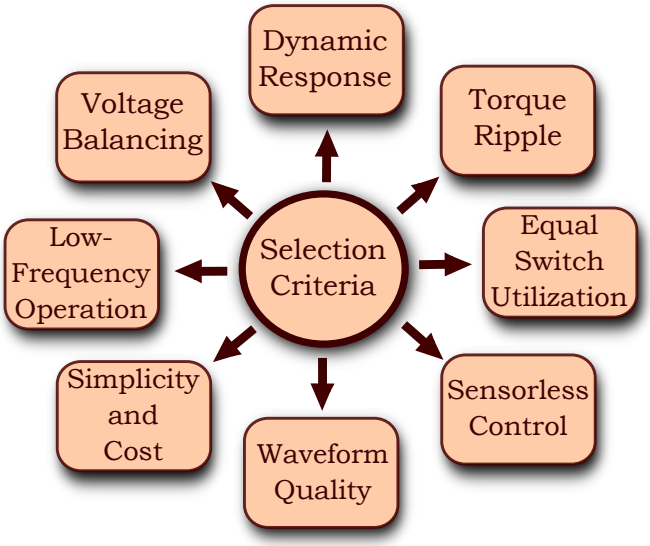


Figure 4.6: Selectrion criteria for control and modulation techniques

The voltage imbalance issue in capacitors or in the neutral point of a multilevel topology depends on the operating point. The worst-case happens in low power factor and high modulation index. This unbalance between voltages can produce load current imbalance, and more importantly, can damage the switches by exceeding the switch voltage limit [147]. It should be mentioned that balancing control techniques may inject common-mode voltages and increase the THD value. A comparison of some balancing algorithms is presented in [148].

4.2.3 Simplicity and Cost

Different control and modulation techniques vary from the complexity perspective. The simpler techniques are preferred due to their higher reliability and lower computational burden. However, with the advancements in digital signal processing, more complex techniques become viable. Regarding the cost, techniques with a smaller

number of required sensors are preferred [149]. Pre-charging the capacitors is another issue that may increase the complexity and cost of the control system in the topologies with a large number of floating capacitors [150].

4.2.4 Sensorless Control

Due to the need to increase reliability and reduce the cost of traction systems, there is a trend toward removing speed and position sensors in this industry [151]. Moreover, sensorless control techniques provide more compactness, higher noise immunity, and less required maintenance. These techniques are offered for different control methods. However, sensorless control methods are not capable of ensuring a robust dynamic performance at low and zero speeds without additional measures [121, 142]. Some multilevel topologies with specific control techniques can be used to improve the low-speed sensorless operation of the drive system [152]. Several studies have investigated sensorless control techniques in traction inverter and other drive applications [153–157].

4.2.5 Torque Ripple

High torque ripple in a traction motor results in a higher vibration, acoustic noise, and malfunction in the drive system. Although different types of motors exhibit different values of torque ripples, selection of the control and modulation scheme also affects the ripple value. Consequently, different modifications are proposed for control techniques to decrease the torque ripple value [158–160]. Using multilevel inverters also helps further reduction of the motor torque ripple with a constant switching frequency [161].

4.2.6 Power Quality and Equal Switch Utilization

Although multilevel inverters offer traction motor loss reduction compared to two-level converters due to lower THD and EMI [34, 162], the amount of reduction depends on the modulation scheme. Moreover, some of the modulation schemes need periodic switching pattern rotation in order to have equal power loss in the semiconductor devices [69]. This will in turn increase the complexity of the controller and modulator. Also, in some topologies, such as NPC, an inherent loss unbalance is present in each converter leg due to unequal conduction and switching losses. This issue can be resolved by moving towards the ANPC structure and employing a proper loss balancing scheme.

4.3 Control Techniques for Traction Multilevel Drives

A comparison of different control methods for multilevel inverters in traction drives is presented here. Scalar control and FOC in multilevel drives are similar to the two-level inverters since the control stage provides the input to the modulator stage [82].

Conversely, other control techniques, like DTC and MPC need to be adjusted to match the inverter topology since the modulator and control stages are combined together. For example, neutral point balancing needs to be addressed in designing a controller based on the DTC method for an NPC traction inverter. Consequently, this section mostly deals with the DTC control technique with the implicit modulator.

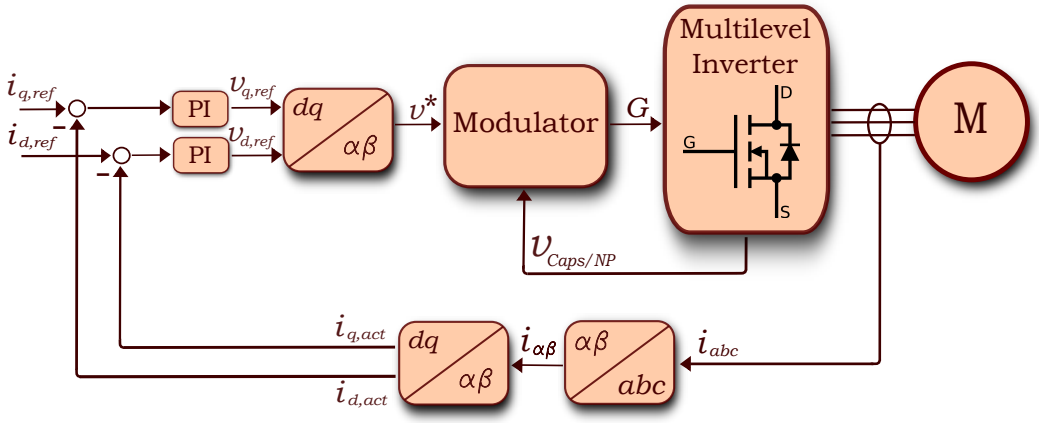


Figure 4.7: FOC Scheme Block Diagram

4.3.1 Scalar Control

Scalar control aims at controlling the magnitude of the control variables and is founded on the steady-state model of the machine. In other words, it doesn't consider the coupling effects in the motor [163]. Although scalar control is a cheap and simple method to implement, it has a poor performance, especially in applications with fast dynamic requirements [164], like traction applications.

The dynamic response of the scalar controller can be improved by adding two feedforward paths for the slip and stator voltage magnitude to the control scheme. Its performance improvement depends on the accuracy of these feedforward paths [144]. The scalar controller is not investigated further here for traction application.

4.3.2 Field-Oriented Control

Field-oriented control, which is a vector control method is a suitable option for traction drives due to its enhanced dynamic performance over the entire speed range. Motor's flux and torque are represented as functions of the stator currents which are

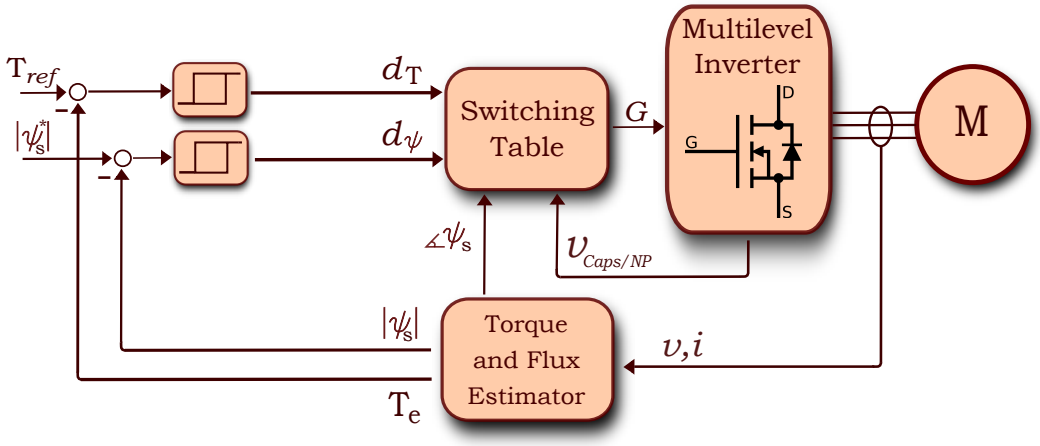


Figure 4.8: DTC Scheme Block Diagram

controlled directly [144]. This in turn results in a relatively fast dynamic response and low current and torque ripple in FOC-based drives [164, 165]. However, the presence of a modulator stage in the control diagram slows down the control process [149].

The schematic of a FOC-based multilevel PMSM drive is shown in Fig. 4.7. As mentioned before, there is no difference in FOC-based control of Multilevel and two-level drives except in the modulator stage.

4.3.3 Direct Torque Control

Direct torque control, which is a well-established motor control scheme, aims at controlling the flux and torque directly, not through the stator currents. Hysteresis controllers are used for tracking the torque and flux. Then, the optimum voltage vector and gating signals are selected using a switching table [163, 166]. The schematic of a DTC scheme for a traction motor is depicted in Fig. 4.8.

The main advantages of the DTC scheme are the very fast torque response, robust operation, and simple structure with low computation time [166]. The simplicity of

the DTC scheme stems from eliminating the need for current regulators, co-ordination transformations, and modulators. Moreover, the DTC method is considered intrinsically sensorless since it is capable of presenting good dynamic torque response without using a mechanical sensor on the shaft [165]. The mentioned advantages make it a potential option for traction drives. However, higher noise and more difficult control at very low speed, higher torque and current ripple, varying switching frequency, absence of current control, and large start-up current are the disadvantages of this method comparing to FOC [165, 167].

A multilevel DTC motor drive benefits from the enhancement of the low-speed performance and reduction of the torque ripple when compared to its two-level DTC counterpart. The reason for this performance improvement is the increased number of voltage vectors [161]. However, the common switching table which is employed for two-level inverter cannot be used for the multilevel drive since the issues of smooth vector switching and balancing the capacitor voltages or neutral point need to be addressed when applying DTC scheme to a multilevel drive [167].

A three-level medium voltage, high power inverter with DTC control scheme is manufactured for drive applications by ABB, where the manufacturer has announced that the application of this drive system is marine propulsion system [168].

In an attempt to use the advantages of both FOC and DTC, a combined control method for an NPC multilevel inverter is presented in [169]. The authors have claimed that this control method benefits from fast dynamic response and simplicity of the DTC scheme as well as low current and torque ripple of the FOC method. However, using a modulator stage and current regulators has increased the complexity of the system comparing to the conventional DTC.

In [167], two modified DTC methods are presented for a multilevel-fed induction motor drive in order to solve the smooth vector switching and neutral point balancing issues. In the first scheme, intermediate and small vectors are utilized in order to address the mentioned issues. However, this increases the complexity of the DTC scheme. In the second proposed modified DTC, discrete space vector modulation (DSVM) is extended to a three-level structure with low extra computations. A sequence for a set of synthesizing vectors is presented which decouples the vector selection for torque and flux control from the circuit requirements of the three-level structure. In the same study, a fuzzy logic controller and a flux observer were used to improve the performance of the sensorless drive. A pre-excitation method is also employed for the large start-up current issue. 6 RPM operation of the sensorless induction motor drive is achieved by the mentioned techniques.

A DTC scheme is proposed in [170] for a three-level traction drive, where the authors have used extremum seeking control (ESC) to determine the optimum flux with a model-free adaptive controller. A dynamic look-up table method is proposed in [171] which is capable of reducing torque ripple regardless of the motor speed. However, the flux ripple is increased slightly in low speeds. A DTC-based control scheme for a five-level FC drive is presented in [139]. The proposed control scheme maintains the floating capacitors' voltages in the required range while providing the required output voltage.

Although most of the studies on the multilevel DTC scheme in the literature are dealing with IM drives, [161] proposes a DTC scheme for three-level IPMSM drives which are getting more popular in traction applications. The proposed scheme is a duty cycle DTC (D-DTC) based method, aimed at minimizing torque ripple while

Table 4.1: A Comparison of Control Techniques for Multilevel Traction Drives

Control Technique	Advantages	Disadvantages
Scalar	+ Simple and cheap + No feedback required	- Poor dynamic response - Inaccurate control - High torque ripple - Torque is not controlled
FOC	+ Good dynamic response + Low torque and current ripple + Fixed Switching Frequency + Full torque at zero speed	- Feedback is required - Costly - Slower response comparing to DTC and MPC - Requires an external modulator - More complex compared to DTC
DTC	+ Very fast dynamic response + Intrinsically sensorless + Simple structure + Low computation time	- Variable switching frequency - Difficult control at low speed - Higher torque and current ripple comparing to FOC - Large start-up current

avoiding a significant increase in the switching frequency. The proper selection of the small voltage vectors according to the neutral point voltage has resulted in minimum neutral point voltage fluctuations. The proposed method also satisfies smooth voltage vector switching.

While most of the studies investigated this scheme for three-level drives, a generalized DTC scheme for multilevel inverters is proposed in [172] for any number of levels. By replacing the conventional torque hysteresis controller with a PI regulator and two carrier-fed comparators, the inverter can operate with a constant switching frequency.

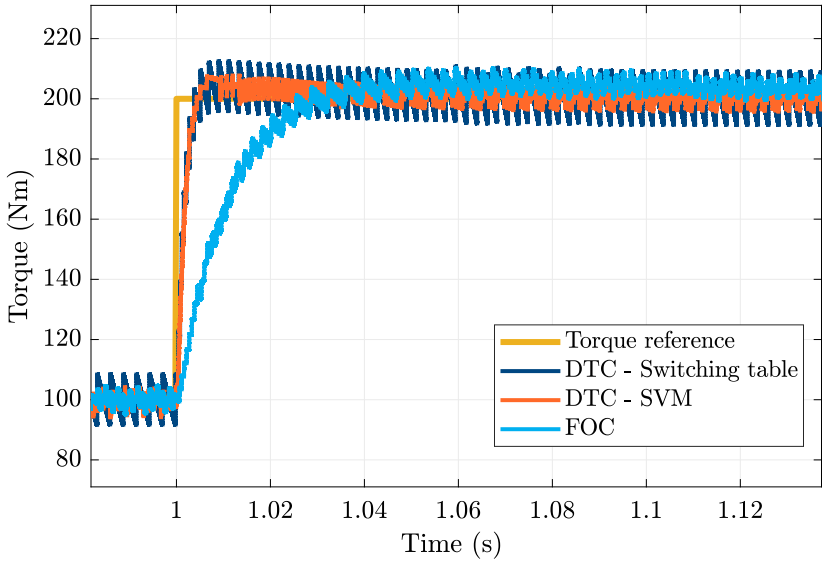


Figure 4.9: Comparison of response to a change in applied torque with DTC-Switching table, DTC-SVM, and FOC schemes

Torque ripple values have been reduced by more than 50% at different speeds by using the proposed method at the cost of about 25% increase in computational cost. In [173] a DTC scheme with imposed switching frequency algorithm is proposed for an 11-level cascaded drive in order to minimize switching frequency variations. A DTC-based induction motor for EV propulsion in a 7-level single source CHB inverter is proposed in [174]. The authors proposed a hybrid modulation scheme to be added to the control system. Capacitor voltage control is also achieved by adjustment of the active and reactive powers.

While simplicity is the interesting feature of DTC-based drives, the proposed methods, which improve the characteristics of the control system, lead to an increase in the complexity of it [165].

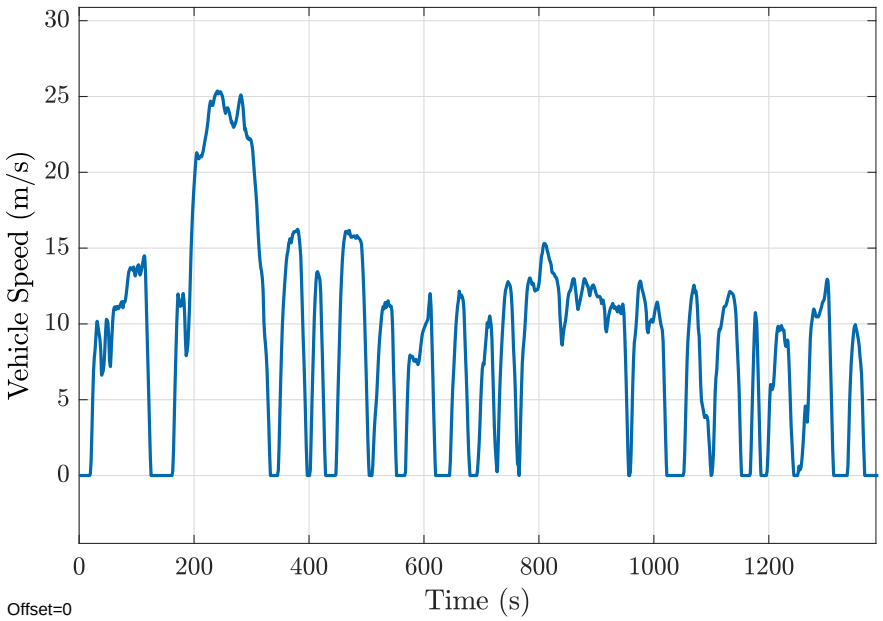


Figure 4.10: UDDS driving cycle

4.3.4 Comparison of Results

Following the mentioned characteristics for each of the methods, a comparison based on simulations is presented in this subsection. Fig. 4.9 exhibits the torque response to a change in the applied torque when the speed is constant. Although the DTC method has the fastest dynamic response compared to other methods, the torque ripple is shown to be higher in this technique. However, the torque ripple of the DTC method can be reduced at the cost of higher complexity by adding an SVM modulator instead of the hysteresis control. It needs to be mentioned that a very fast tracking response may affect the stability of the system regarding the DC-link which has to be considered in the design.

Comparing multilevel inverters to their two-level counterparts show that the amount of torque ripple reduces as the number of levels goes higher. Based on the results

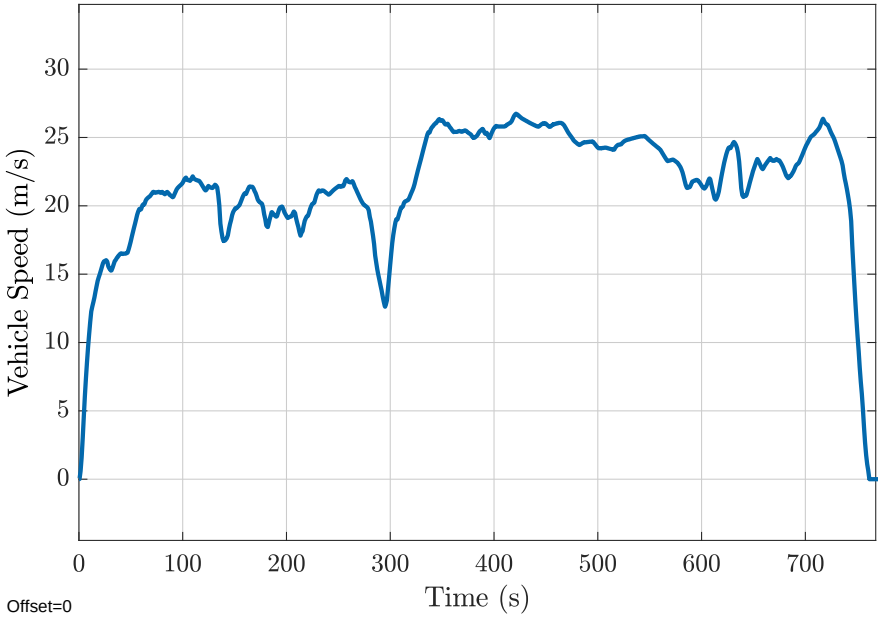


Figure 4.11: HWFET driving cycle

presented in [175], the amount of torque ripple has reduced to less than half in a four-level inverter compared to the conventional two-level structure.

Following speed reference in an electric vehicle can be a more accurate measure of the dynamic performance of a traction control system. In this study, two standard driving cycles are selected to measure the RMS error in following the speed reference using each of the control techniques. Urban dynamometer driving schedule (UDDS) and highway fuel economy driving schedule (HWFET) driving cycles are selected as urban and highway driving cycles respectively. Table 4.2 shows the RMS error percent in following the reference speed. Fig. 4.12 magnifies some parts of the UDDS driving cycle and response of each controller to the reference speed.

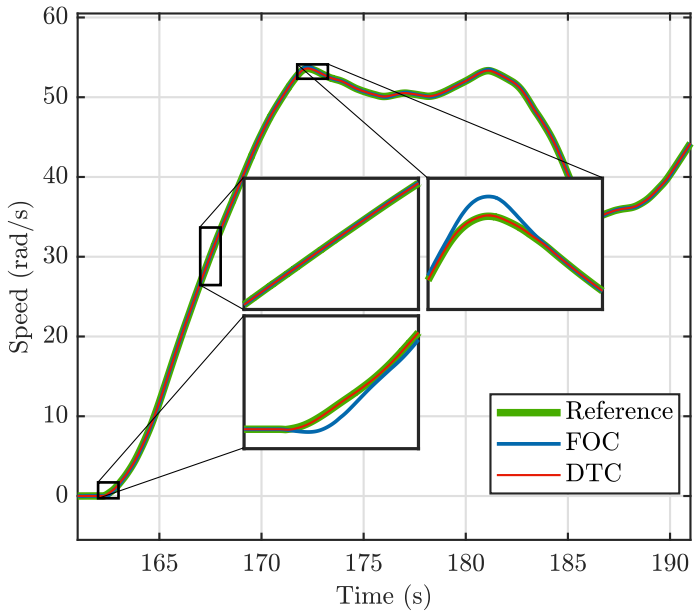


Figure 4.12: Following reference speed in UDDS driving cycle with different control methods

4.4 Modulation Schemes for Traction Multilevel Drives

Generally, modulation techniques for multilevel converters can be classified into carrier-based pulse-width modulation, space vector pulse-width modulation, pre-programmed pulse-width modulation, and level-based modulation. As mentioned before, conventional DTC and MPC methods do not require separate modulators.

Table 4.2: RMS Error in Following Speed Reference (% of Reference)

Control Method	UDDS	HWFET
Scalar	2.71 %	1.19 %
FOC	0.94 %	0.34 %
DTC	0.07 %	0.04 %

4.4.1 Sinusoidal Pulse Width Modulation (SPWM)

Sinusoidal pulse width modulation (SPWM), in both phase-shifted (PS-SPWM) and level-shifted (LS-SPWM) variations, is an extension of the well-known SPWM technique for the two-level inverter. Both techniques are considered simple modulation schemes. This is more considerable in higher number of levels, where other modulation techniques become more complex [69].

In a comparison of the PS-SPWM and LS-SPWM, the latter benefits from a lower total harmonic distortion (THD) in the same modulation index. However, due to unequal switch utilization, there might be a need to rotate the switching patterns in LS-SPWM. In a three-level inverter, voltage balancing and maximum DC-link utilization can be achieved by adding a third harmonic content to the carrier. However, in higher number of levels, voltage balancing cannot be achieved simply. The THD of SPWM is higher compared to more advanced modulation techniques. The response of the SPWM-based multilevel drive in low-speed operation as well as their dynamic response is poor [33, 69, 137, 176].

There have been studies to improve the characteristics of the SPWM technique. In order to overcome unequal switch utilization of LS-SPWM cascaded multilevel inverter, [177] has proposed a sorting strategy that ensures equal distribution of pulses

even in the fault condition of one or more cells. In [147], the issue of balancing the neutral point in NPC inverter is addressed for the entire power factor range by introducing a modulating voltage component which is in phase with the load currents. The issue of low-frequency oscillation in the neutral point of NPC drive is addressed in [178] by using two modulating signals for each inverter phase. A capacitor voltage balancing method based on SPWM for nested neutral point clamped (NNPC) inverter is proposed in [179], where the proper switching state is determined based on the required output voltage level and current direction. It should be mentioned that the proposed improvements for the SPWM scheme deteriorate its simplicity by adding additional stages in the modulator.

4.4.2 Space Vector Modulation (SVM)

With the widespread use of fast microprocessors, space vector modulation (SVM) or space vector pulse width modulation (SVPWM) has been more popular due to lower THD, lower *dv/dt*, higher flexibility, more redundant states, lower common-mode voltage, and higher efficiency in both inverter and motor. It is believed that SVM in the linear region, and six-step modulation (square-wave modulation) in the overmodulation region, are mostly utilized in two-level traction application [33, 144, 180].

SVM for multilevel drives suffers from high computation times. As the number of levels of an inverter increases, the number of switching states increases dramatically. Consequently, simplification of the SVM technique for multilevel inverters has been the subject of many studies [180–183]. In [180] the required memory for a multilevel inverter is reduced by storing the switching states of only the first vertex of the

modulation triangle. The switching states of other vertices are achieved by a mapping technique. This method has increased the speed of computations by eliminating the look-up tables.

In [34], a switching sequence is presented for balancing the DC-link capacitors' voltages of a three-level NPC inverter used in EVs. The proposed sequence reduces the number of transitions and switching loss while ensuring a low difference between the capacitors' voltages. A modified virtual SVM technique, which is designed for traction inverters, is proposed in [184] with the purpose of minimizing neutral point voltage fluctuations in transient conditions.

4.4.3 Discontinuous Pulse Width Modulation (DPWM)

Discontinuous pulse width modulation (DPWM) scheme which was first proposed for two-level inverters is capable of reducing switching losses considerably by eliminating switchings at the peak of the sinusoidal currents. However, applying this technique to multilevel inverters is challenging due to the issue of voltage balancing in multilevel inverters [185]. Moreover, the value of current and voltage THD is high in with this modulation technique. Fig. 4.13 compares power loss in continuous carrier-based PWM (CPWM) and DPWM schemes presented in [186]. The switching frequency in this study is 10 kHz.

In order to utilize the DPWM method in NPC structure, additional measures need to be taken to ensure low ripple on neutral point voltage. In [187], three switching patterns are proposed to be used based on the drive operating speed in order to ensure a low imbalance on the neutral point. In [188] two offset voltage with opposite influences are used and reduced neutral point voltage fluctuations effectively. This

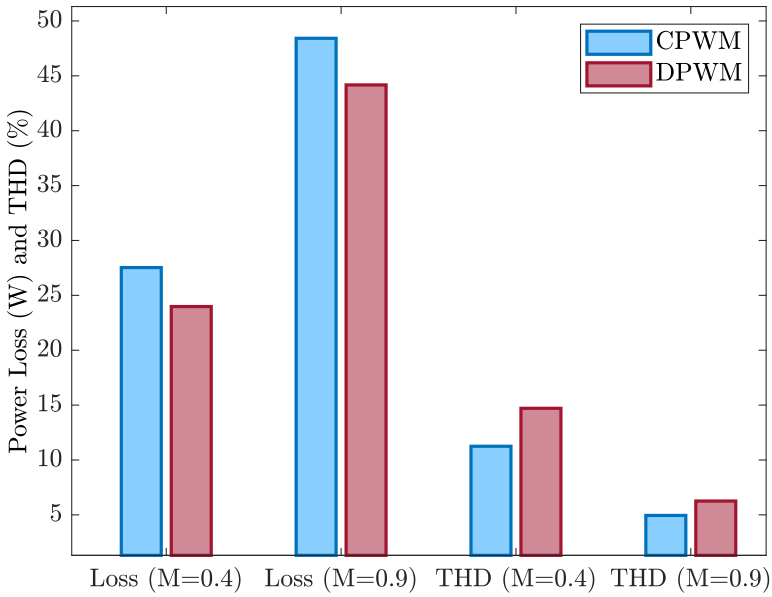


Figure 4.13: Comparison of CPWM and DPWM

method has increased inverter losses comparing to conventional DPWM. However, the loss value is still lower than other modulation schemes.

DPWM technique is also proposed for traction inverter applications [189–191]. A hybrid strategy is proposed in [191] with a variable to control the discontinuous interval in a three-level traction drive which is operating under different load and power factor conditions. The control of the discontinuous interval addresses the tradeoff between switching loss and neutral point voltage imbalance.

4.4.4 Selective Harmonic Elimination (SHE)

Selective harmonic elimination (SHE) modulation technique uses pre-determined angles of commutation in order to eliminate low-order selected harmonics. Although the SHE scheme lacks fast dynamic response, in high-power traction drives like electric trains, the SHE method is used at high-speed region of operation of the motors

[144, 192, 193]. This scheme benefits from low switching frequency, high efficiency, and small filter requirements [194]. SHE technique has been expanded to multilevel topologies [194]. In [79], an SHE technique is proposed for a traction inverter in railway transportation which is based on NPC multilevel inverter. It should be mentioned that voltage balancing in a multilevel inverter that uses SHE modulation is an issue due to the low switching frequency. Large capacitors are required which makes it uninteresting, especially for low-power battery-powered EV drive systems.

4.4.5 Nearest Level Modulation (NLM) and Windowed Pulse Width Modulation (WPWM)

The switching frequency in the nearest level modulation (NLM) technique is low, like the SHE scheme. However, this technique does not require the calculation of commutation angles which makes it simpler. The main drawback of this technique is low-quality output waveform in low number of levels [195]. Consequently, this modulation technique is not suitable for low-power traction drives. It is proposed for high-voltage MMC-based multilevel inverter for railway electrification in [81]. A large number of levels ensure acceptable waveform quality.

Some modifications and improvements have been applied to the NLM method. Improving the waveform quality, capacitor voltage control, and circulating current control in MMC inverters is achieved in [195, 196]. In [197] a modulation technique called windowed pulse width modulation (WPWM) is proposed for traction drives. The idea behind this scheme is to combine NLM and PWM in order to take advantage of low switching loss of NLM and good quality output waveform of PWM methods. In this scheme, PWM is applied at some specific intervals. These intervals

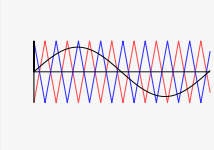
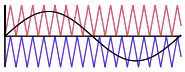
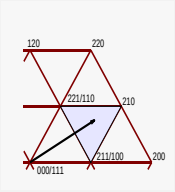
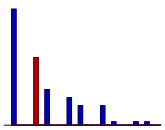
are determined dynamically based on the traction drive's operating condition.

4.5 Summary

An important factor in designing an inverter for EV application is selection of the best control scheme. Based on the literature review presented in this chapter, some major criteria must be taken into account like fast dynamic response, torque ripple, etc. Additionally, some requirements are specific to multilevel drives due to their different structure. Voltage balancing and power loss distribution are among the most essential criteria. Both DTC and FOC with proper modulator show an acceptable performance regarding the mentioned criteria in EV industry. Advanced control techniques, like MPC, are investigated in more details in Chapter 8.

Regarding the modulator selection, SPWM, SVM, and DPWM show interesting characteristics when modified for the selected multilevel topology. Techniques such as SHE and NLM are not utilized in low-power EV drives due to their limited switching frequency. Loss distribution techniques are investigated in more details in Chapter 7.

Table 4.3: A Comparison of Modulation Schemes for Multilevel Traction Drives

Modulation Technique	Scheme	Advantages	Disadvantages
PS-SPWM		+ Simple structure + No need to rotate switching patterns + three-level voltage balancing achieved by adding third order harmonic content	- Higher THD than other techniques - Not flexible for voltage balancing in high-level structures - Poor response in low-speed motor operation - Poor dynamic response
LS-SPWM		+ Simple structure + Better output waveform quality than PS-SPWM + three-level voltage balancing achieved by adding third harmonic content	- Higher THD than SVM - Not flexible for voltage balancing in high-level structures - Poor response in low-speed motor operation - Poor dynamic response
SVM		+ Redundant switching states + Effective voltage balancing strategy + Low output THD + Good dynamic response + Low dv/dt + High Efficiency	- Complex in high-level structures - slower dynamic response than MPC with implicit modulator
SHE	 $cos(5\theta_1) + cos(5\theta_2) = 0$	+ Suitable for high-power applications + Effective low-order harmonic elimination, resulting in smaller filters + Good steady-state response + Very low switching losses + High efficiency	- Slow dynamic response - Not suitable for low-power traction drives - Poor response in low-speed motor operation - Not flexible for voltage balancing

Chapter 5

Compact High-Power Three-Level Active Neutral Point Clamped (ANPC) Inverter for EV Applications

A three-level ANPC inverter is designed and implemented for EV applications. Achieving high power density in the final implemented inverter has been the design goal which impacted the selection of the structure, power MOSFEFTs, switching frequency, etc. A brief introduction of the specifications, structure, and implementation cost of the inverter is presented in this chapter.

Table 5.1: Inverter Specifications

Parameter	Value	Description
Continuous Power	70 kW	Continuous operation
Peak Power	100 kW	10 Seconds
Input Voltage	800V	700V - 850 V
Topology	3-L ANPC	Three-Level Active Neutral-Point Clamped
Input Coolant Temperature	60 C	Glycol(50%) Water(50%)
Communication Protocols	CAN, RS232	Available from output connector C2
Speed Sensor Compatibility	Resolver	Available from output connector C3
Auxilliary Supply	12V	Input connector C1
Dimensions	292*242*57	mm
Ingress Protection (IP) Rating	IP67	IP67
Peak power density	31 kW/L	With proposed method in Section 7

5.1 Inverter Specification and Structure

In order to satisfy the requirements of a city BEV with high-voltage 800V batteries, Table 5.1 has listed the set of specifications of the inverter.

5.1.1 Inverter Structure

The selected topology for implementing this inverter is Three-level Active Neutral-Point Clamped (3L-ANPC). The selection of this structure is made based on the

results of the survey in Chapter 3. FC-based structures are not the best solution due to first, the voltage unbalance at low output frequency operation and second, the increased number of capacitors which make the may reduce both power density and reliability. On the other hand, the MMC topology is suffering from both large number of capacitors and circulating current. Minimizing the circulating current requires adding some passive elements that reduce the power density. Also, the CHB structure suffers from large number of required devices and the need for isolated DC sources. Finally, ANPC was selected over NPC due to the higher flexibility in loss distribution since the clamping diodes are replaced with fully controlled switching devices.

Regarding the decision about the number of levels, the three-level structure is used due to the availability of automotive power switches on the market. Since the input voltage in this inverter is two times higher than most EV inverters, an 800V 3L-ANPC inverter can make use of the vast switch options (both IGBTs and SiC MOSFETs) suited for 400V two-level inverters. Structure of a three-phase 3L-ANPC inverter is shown in Fig. 5.1.

As shown in Fig. 5.1, each leg of the inverter has 6 active switching devices. The maximum voltage stress on each switch, ignoring the overshoots and spikes, is half of DC-link voltage. However, this only happens if the capacitor voltages are balanced with a reliable control technique.

5.1.2 Maximizing Power Density

As mentioned earlier, a major step in achieving high power density in an automotive inverter is increasing the operating DC voltage of the inverter which is usually equal

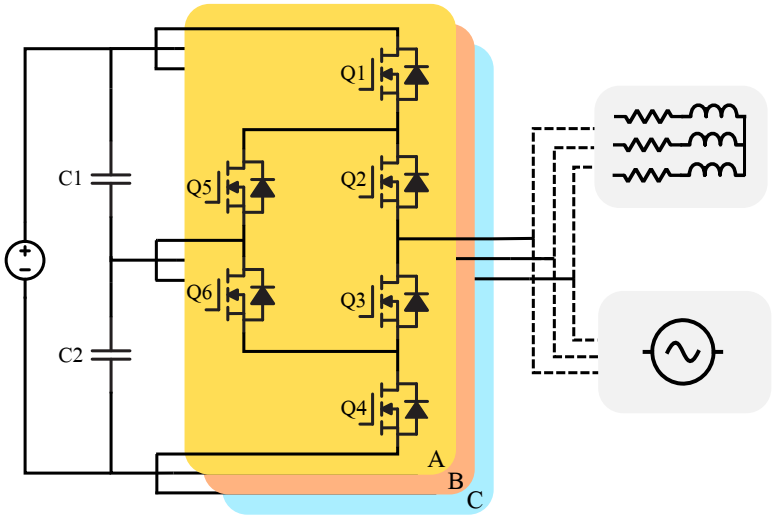


Figure 5.1: The schematic of a three-phase, three-level ANPC inverter

to the battery voltage. Therefore, moving from 400 V to 800 V input voltage in the proposed inverter structure enables a shift in the power density of the inverter mainly due to smaller current stress in the power circuit from the input to the output of the inverter.

A large portion of the automotive inverter's volume is dedicated to the DC-link capacitors. Two major factors which determines the volume of input capacitors in a motor drive are the maximum current passed through the capacitors and the allowable DC-link voltage ripple. By assuming that the current drawn from the battery is pure DC, the AC component of the input current of the three-phase bridges is equal to the current drawn from the capacitor banks. Hence, the RMS current of the capacitor can be written as (5.1):

$$I_{C,rms} = \sqrt{I_{rms,in}^2 - I_{dc,in}^2} \tag{5.1}$$

By increasing the DC-link voltage, the input RMS and DC currents of the inverter

reduce correspondingly. Hence, the capacitor RMS current in an 800 V inverter is reduced by half compared to a 400 V drive.

Additionally, the voltage ripple on each leg of the inverter is also determined by the capacitor value based on (5.2) and (5.3):

$$i_c = C \frac{dv_c}{dt} \tag{5.2}$$

$$C = \frac{i_c}{\Delta V \times f_{sw}} \tag{5.3}$$

Based on (5.3), increasing switching frequency can result in smaller capacitor requirement in the input. Additionally, higher switching frequency can reduce the size of any required filters in the powertrain outside the inverter module. In the implemented inverter, a maximum switching frequency of 50 kHz was selected based on the utilized switching devices in order to minimize the volume of the input capacitors.

5.1.3 Main Components

The main components used in implementing this inverter are listed in Table 5.2. All components are selected to be able to operate at the range of -40 $°C$ to +95 $°C$ ambient temperature inside the inverter enclosure. The MOSFETs, which are attached to the heatsink, are capable of operating at a maximum junction temperature of 175 $°C$.

5.2 Protection and Safety Measures

There are many reasons in a power electronic converter for a malfunction or fault occurance. These reasons vary from the defects in the design, to environmental

Table 5.2: Main Components of the Inverter

Component	Part number	Manufacturer	Description
MOSFET	UJ4C075018K4S	United SiC	750V-18mW SiC FET, Two MOSFETs in parallel per each switching device
Capacitors	MKP1848580704K2	Vishay	700V-8uF MKP capacitor, 18 capacitors are used to form two 72uF capacitor banks
Gate Driver	UCC21750	Texas Instruments	10-A, isolated, single channel IGBT/SiC MOSFET driver with fault protection
Microprocessor	TMS320F28379D	Texas Instruments	Dual core, 200 MHz, Floating-point, Two programmable CLA units
Current Sensor	HTFS 200-P	LEM	Up to 200A RMS AC/DC current measurement
Voltage Sensor	ISO224	Texas Instruments	Isolated amplifier

factors. Hence, it is vital for a converter to be able to detect these faults and switch off (or restart) the inverter. In the designed inverter, multiple protection measures are implemented to maximize safety:

- Ambient temperature measurement and tripping in case the ambient temperature is out of predefined range (-40 C to +90 C)
- Input DC overvoltage (>900) detection
- Input DC undervoltage lockout
- Heat-sink temperature measurement using thermocouples (at 8 points)

- Grounded enclosure
- Watchdog protection for microprocessor
- Analog and digital signal buffering from/to gate driver to/from control board
- MOSFET protection (for all MOSFETs) by gate driver
- 5V and 3.3V under/over voltage protection on the control board
- undervoltage lockout for all gate driver ICs

5.3 Designed PCBs and Enclosure

The implemented inverter with all the input and output connectors is shown in Fig. 5.2. A1 and A3 are the negative and positive input DC-link respectively. A2 in the optional input which is connected to the capacitors' middle point in case a multi-source input is to be used. B1, B2, and B3 outputs are the three-phase output connectors which connect to the load. C1 is an input terminal which connects the 12 V supply for the control and gate driver boards. C2 is a connector which is used for CAN and RS232 serial connections as well as the turn-on and turn-off commands to the inverter. C3 terminal is used for motor resolver connection. Finally, D1 and D2 are the coolant input and outputs, respectively. It worth mentioning that the three current sensors required for control loop are implanted in the enclosure, where the output cables connect to the power PCB.

The inverter has three main boards. The inverter's top view with an open lid can be seen in Fig. 5.3, where the control and gate driver boards which are placed on the top of the power board can be seen.

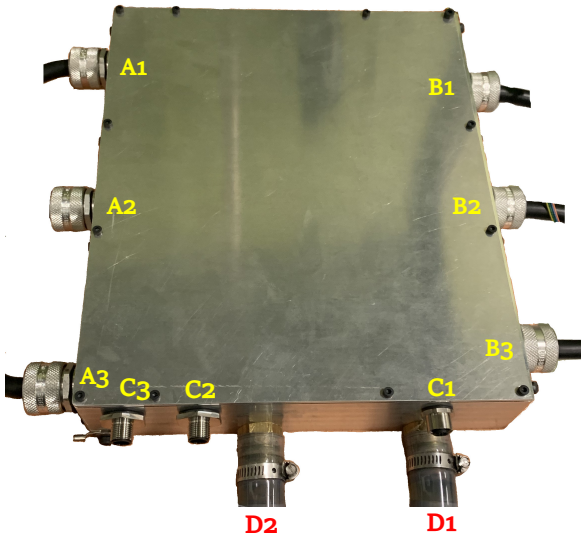


Figure 5.2: Top view of the inverter with I/O connectors and coolant input and output

An exploded view of the power PCB as well as the fin base, cooling block and the housing is depicted in Fig. 5.4. On the very bottom lies the power board. The DC-link capacitors and 36 MOSFETs (2 parallel MOSFETs per switching device) are soldered to this board from the bottom and attached to the heatsink. On the top of the power PCB, gate driver board is placed. Gate signals are sent to the power board using the bottom-entry connectors. Finally, the control board can be seen on the top of gate driver. It should be mentioned that the control and gate driver circuitry is split between two boards for higher modularity in the prototype design. They can be designed on the same board to decrease the volume further.

5.3.1 Power PCB

Due to increasing the voltage in this inverter, the max continuous output current for 70 kW operation remains smaller than 80 Arms which allows using high-current 6

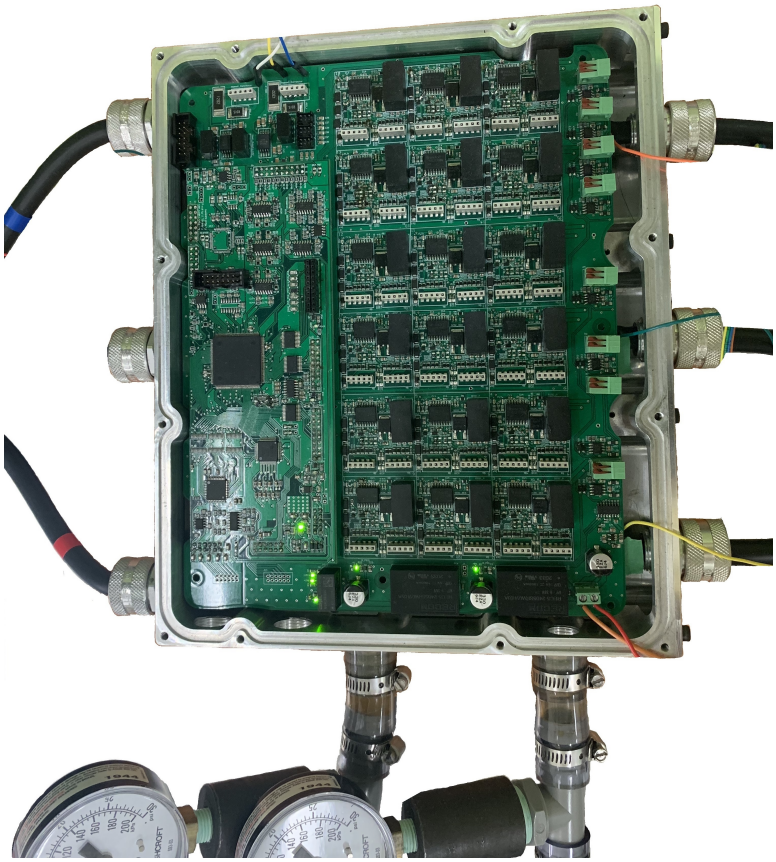


Figure 5.3: Top view of the inverter with open lid; Control and gate driver boards

oz PCB traces with adequate width in 6 layers to be used instead of busbars. One benefit of this will be smaller gap between the forward and return current paths which minimizes the stray inductance of the current path. Stray inductance of all possible current paths in each leg of this inverter is investigated and simulated in [198]. Also, thermal response of the PCB in continuous and peak power modes is extracted from ANSYS simulations in the mentioned article.

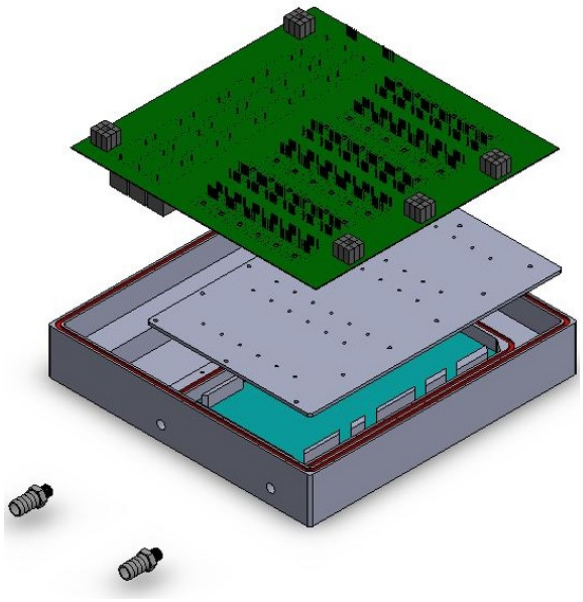
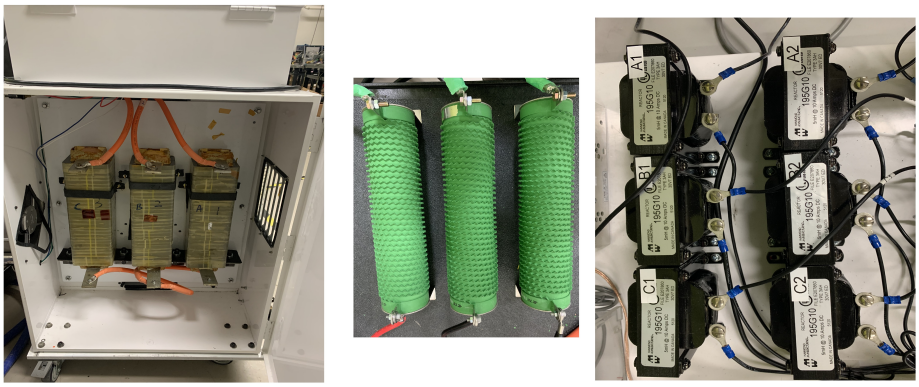


Figure 5.4: Exploded view of the enclosure, coolant block, fin base, and power PCB

5.3.2 Gate Driver and Control PCBs

The gate driver is a 4-layer, 1-oz PCB where 18 gate driver ICs are in charge of driving 36 MOSFETs. 18 DC/DC converters are providing the required isolated 15V/-5V for driving MOSFETs. The connectors for current and voltage sensors are also placed on the gate driver board. Moreover, thermocouple amplifier circuits are placed on the gate driver board with input terminals. These thermocouple amplifier circuits help measuring different temperatures on the heatsink during thermal characteristics extraction. The input supply to the gate driver board is a 12 V supply which goes to the required isolated DC/DC converters.



(a) (b) (c)

Figure 5.5: Output loads used in the experimental tests; a) 200 μH high-current inductors, b) resistive bank, and c) 5 mH inductors

5.4 Load

A three-phase high current inductive load with the initial inductance of 200 μH, shown in Fig. 5.5(a), will be used for high current inductive tests in this thesis. In pure inductive tests, due to the inductive nature of this load, the input DC source is only supplying the losses. However, when higher power factor is needed, high power resistive banks as shown in Fig. 5.5(b) are used in series with the inductive load. Other than the high-current inductors, some 5 mH inductors, shown in Fig.5.5(c) will be used in series and parallel for lower-current tests in section 8.

5.5 Cost

In this section, the cost of the main components in the implemented prototype inverter is compared to that of an inverter with similar output power requirements, but with a two-level structure and 400 V input DC-link voltage. Tables 5.3 and 5.4 list the

Table 5.3: Main Components of a 70 kW three-level ANPC Inverter with 800 V input voltage

Component	Part number	Count	Unit cost (CAD)	Total cost (CAD)
MOSFETs	UJ4C075018K4S	36	27	972
DC-link capacitors	MKP1848580704K2	18	8.5	153
Gate drivers	UCC21750	18	9	162
DC/DC converters	MGJ2D122005SC	18	12	216
Control card	Based on TMS320F28379D	1	250	250
Current sensors	HTFS 200-P	2	23.5	47
Voltage sensors	ISO224	2	25	50
Total component cost				1850

main components and compare the total cost. It should be mentioned that all the costs in this table are based on a single prototype, and not mass production.

It can be seen that the inverter cost of a three-level structure has increased by about 35% compared to its two-level counterpart. This was also shown in the section 3. However, when other costs inside an EV are taken into account, the total powertrain cost can be even reduced. The lower cost for cables, motors, and filtering requirements leads to the lower total powertrain cost in case of the three-level inverter compared to two-level structure.

Table 5.4: Main Components of a 70 kW two-level Inverter with 400 V input voltage

Component	Part number	Count	Unit cost (CAD)	Total cost (CAD)
MOSFETs	UJ4C075018K4S	24	27	648
DC-link capacitors	MKP1848580704K2	18	8.5	153
Gate drivers	UCC21750	12	9	108
DC/DC converters	MGJ3T12150505MC	6	25.5	153
Control card	Based on TMS320F28379D	1	250	250
Current sensors	HTFS 200-P	2	23.5	47
Voltage sensors	X	0	0	0
Total component cost				1359

5.6 Summary

A brief overview of the designed three-level ANPC inverter was presented in this chapter. The selected part numbers for major components as well was listed and the cost of building the prototype was determined. When compared to the two-level inverter with 400 V DC-link, the multilevel topology with 800 V DC-link is about 35% more expensive. However, when other associated costs in the inverter is taken into account, the cost of the three-level structure is reduced.

Chapter 6

Introduction of a Comprehensive Electro-Thermal Model for the Three-Level ANPC Inverter

To achieve the junction temperature minimization goal for power density improvement of the 3L-ANPC inverter, a junction temperature estimation technique, based on the energy loss in each MOSFET is needed. In this chapter, first, the loss-related parameters of a power MOSFET are investigated in different temperature, voltage, and current values. Then, two different loss models are derived for a three-level ANPC inverter, taking into account the two available switching pattern in this structure. Finally, first and second order foster thermal equivalent models will be investigated and the most suitable network is selected for MOSFET temperature estimations. It has to be mentioned that the MOSFET characteristics in this chapter is taken from the UJ4C075018K4S MOSFET datasheet Rev. A, provided by United SiC in October 2020.

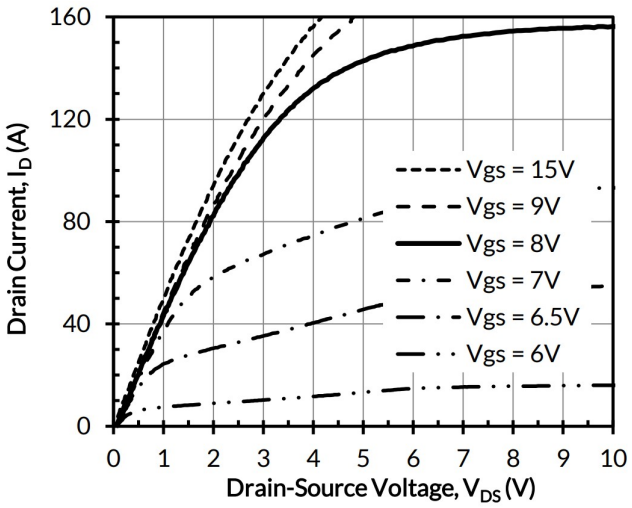


Figure 6.1: The change of V_{ds} versus changes in I_d and V_{gs}

6.1 MOSFET Loss-Related Characteristics

In a power electronic converter, usually, the majority of power losses occur in the semiconductor fast switching devices. This semiconductor power loss is divided into conduction and switching losses. The fundamentals of power loss in power electronic switching components can be found in the literature [199] and will not be further investigated here. In this section, the effects of changing operating conditions is investigated on the characteristics of the power MOSFET UJ4C075018K4S which is used in the implemented ANPC inverter.

6.1.1 On-Resistance, R_{on}

The turn-on model of a power MOSFET is equivalent to a resistor. However, the value of this resistor changes with junction temperature, gate-to-source voltage (V_{gs}), and the magnitude of drain current (I_d) flowing through the MOSFET. The effects of V_{gs} and I_d on the value of drain-to-source voltage (V_{ds}) is shown in Fig. 6.1. However,

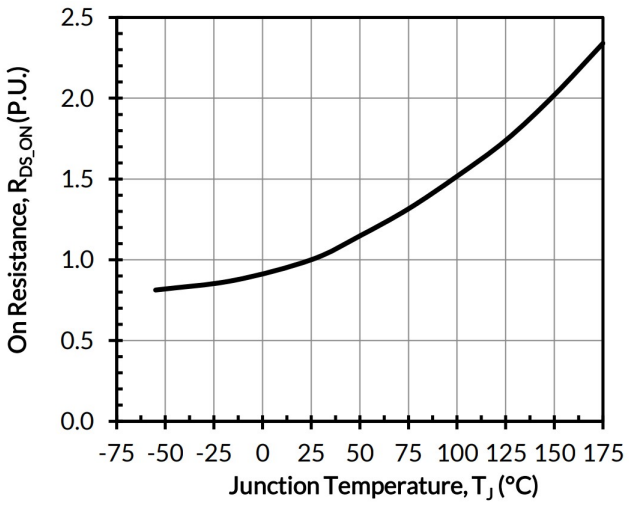


Figure 6.2: The change of R_{ds} versus change in T_j

it can be seen that when a suitably large V_{gs} is used by the gate driver circuit during T_{on}, the relation between V_{ds} and I_d remains almost linear (resistive behavior) for the majority of current range. Therefore, since the applied voltage during T_{on} period is +15 in the experimental setup, this small non-linearity between the current and voltage has been ignored and R_{on} is considered to be only temperature-dependant.

On the other hand, the junction temperature, T_j, seems to have a significant effect on the actual R_{on} value. This relation can be seen in Fig. 6.2. It can be seen that a rise in the R_{on} occurs when T_j goes up. Although the relationship in not linear, it can be estimated with a quadratic equation, shown in 6.1. The coefficients in 6.1 are found found using the MATLAB curve-fitting tool.

$$\begin{gathered} R_{on,PU} = a_1 T_j^2 + a_2 T_j + a_3 \\ a_1 = 2.81 \times 10^{-5} \quad , \quad a_2 = 3.2 \times 10^{-3} \quad , \quad a3 = 0.91 \end{gathered} \tag{6.1}$$

Eq. 6.1 can be used in the current form or as a look-up table with T_j and R_{on}

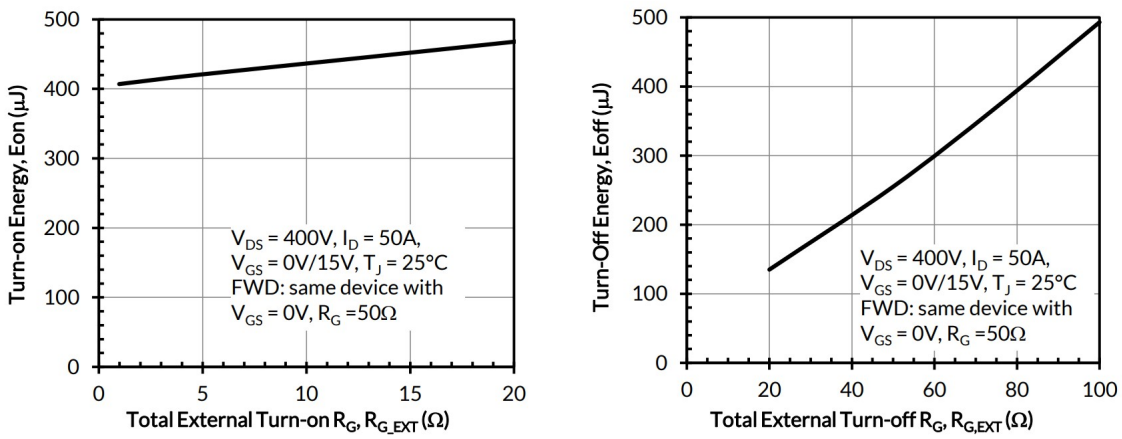


Figure 6.3: The change of E_{on} and E_{off} versus variations of $R_{g,on}$ and $R_{g,off}$

values in the next steps for loss model derivation.

6.1.2 Switching Losses

Due to the non-idealities during turn-on and turn-off of power switches, there is an energy loss in each transition. For an accurate thermal model for the three-level ANPC inverter, the effect of varying parameters on switching losses is briefly investigated in this subsection.

First of all, it can be seen from Fig. 6.3 that the gate resistors $R_{g,on}$ and $R_{g,off}$ can directly affect the switching loss by changing the switching times, t_r and t_f. However, since the values of $R_{g,on}$ and $R_{g,off}$ are not changing during normal operation of the inverter, these values can be picked from Fig. 6.3. It is important to note that the loss values are given based on 0V/15V turn-on and turn-off voltages. In case of using a negative turn-off voltage, the energies need to be modified based on the new voltages and turn-on/off threshold voltages of the MOSFET.

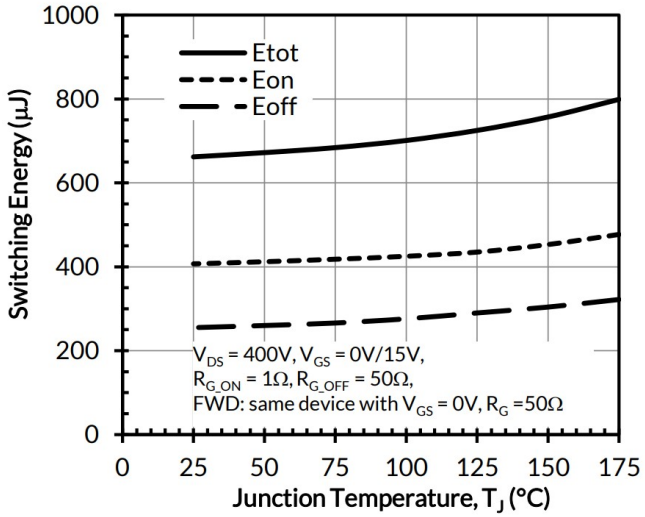


Figure 6.4: The change of E_{on} and E_{off} versus variations of T_j

Next, the effect of temperature on switching energies will be investigated. This can be seen in Fig. 6.4. Again, quadratic equation is used with the curve-fitting tool as written in 6.2. The coefficient are derived for both E_{on} and E_{off}. The derived equations will be used in the simulations for more accurate results, while lookup tables will be used in the experiment for fastest calculations in the real time.

$$\begin{gathered} E_{on,PU,1} = b_1 T_j^2 + b_2 T_j + b_3 \\ E_{off,PU,1} = c_1 T_j^2 + c_2 T_j + c_3 \\ b_1 = 7.2 \times 10^{-6} \quad , \quad b_2 = -38 \times 10^{-5} \quad , \quad b3 = 1.01 \\ c_1 = 9.6 \times 10^{-6} \quad , \quad c_2 = -11 \times 10^{-5} \quad , \quad c3 = 0.99 \end{gathered} \tag{6.2}$$

E_{on} and E_{off} will also change with current and voltage. The changes with current will be modelled as third-order equations to get accurate fitting results to Fig. 6.5. The resulting equations and coefficients for current dependency at $V_{ds} = 400V$ is written down in (6.3). It must be noted that the energy values are first turned to PU

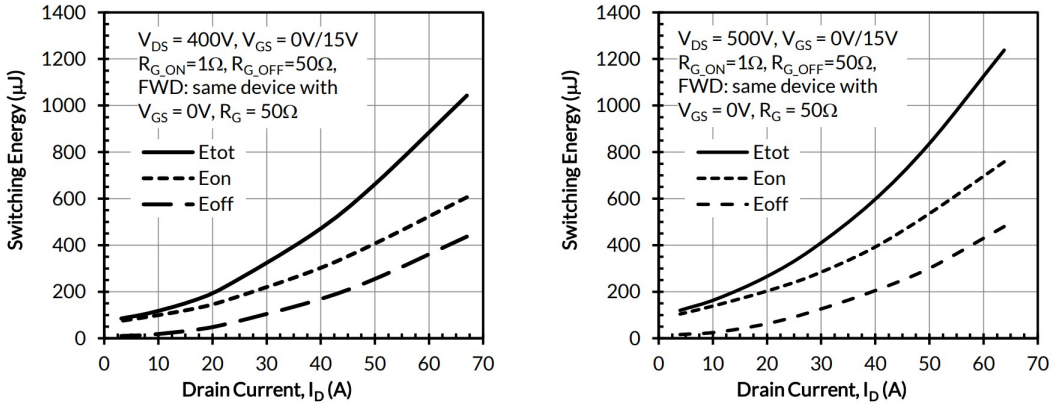


Figure 6.5: The change of E_{on} and E_{off} versus variations of I_d at $400V$ and $500V$

with the base of energy loss at $I_d = 50A$. Also, the dependency of E_{on} and E_{off} to voltage is considered linear and $\propto V_{ds}$. Therefore, since 400V is chosen as the base voltage, the dependency on voltage can be written as 6.4.

$$\begin{gathered} E_{on,PU,2} = d_1 I_d^3 + d_2 I_d^2 + d_3 I_d + d_4 \\ E_{off,PU,2} = e_1 I_d^3 + e_2 I_d^2 + e_3 I_d + e_4 \\ d_1 = -7.8 \times 10^{-7} \quad , \quad d_2 = 2.3 \times 10^{-4} \quad , \quad d3 = 7.9 \times 10^{-3} \quad , \quad d4 = 0.134 \\ e_1 = -1.5 \times 10^{-6} \quad , \quad e_2 = 4.67 \times 10^{-4} \quad , \quad e3 = 1.05 \times 10^{-3} \quad , \quad e4 = 0.012 \end{gathered} \tag{6.3}$$

$$E_{on/off,PU,3} = \frac{V_{ds}}{400} \tag{6.4}$$

For deriving accurate switching loss value, the base energy loss value is taken from Fig. 6.3 based on the gate resistor value, then multiplied by $E_{PU,1,2,3}$.

Other than E_{on} and E_{off} energy losses that were investigated above, two more

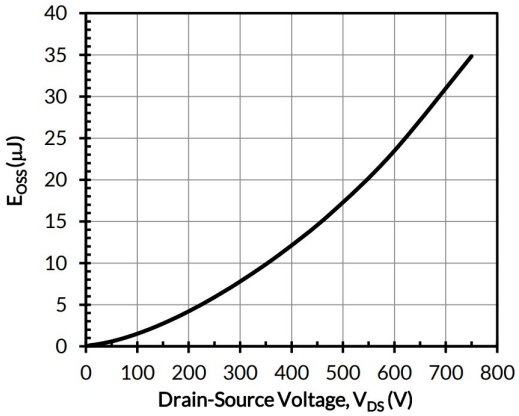


Figure 6.6: The change of E_{oss} versus variations of V_{ds}

loss components, related to the switching moments will be included in the final loss model. The E_{oss} energy is the stored energy in C_{oss}. The relationship can be seen in Fig. 6.6 and Eq. (6.5) for the selected MOSFET.

$$\begin{gathered} E_{oss} = f_1 V_{ds}^2 + f_2 V_{ds} \\ f_1 = 4.4 \times 10^{-11} \quad , \quad f_2 = 1.3 \times 10^{-8} \end{gathered} \tag{6.5}$$

Finally, Fig. 6.7 shows the reverse recovery charge, Q_{rr}, of the parallel diode versus temperature. It can be seen that the variations with temperature are negligible. Based on [199], reverse recovery energy, E_{rr} can be derived as Eq. 6.6.

$$E_{rr} = \frac{1}{4} Q_{rr} V_{ds,off} \tag{6.6}$$

6.2 Three-Level Inverter Loss Model

Having an electro-thermal model for the inverter is essential for junction temperature estimation. In section 6.1 MOSFET datasheet was used to derive the adjusted switch

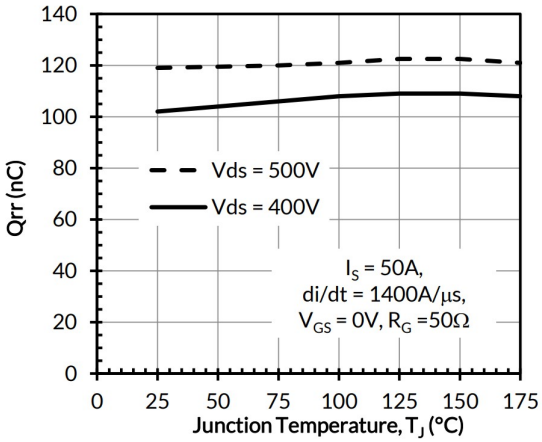


Figure 6.7: The change of Q_{rr} versus variations of T_j

characteristics. However, the current and voltage values depend on the operation conditions of the inverter. Assuming that a balanced three-phase load is connected to the output of the inverter, the power loss evaluations will be performed for one phase (phase a). The current and voltage for phase a are written in (6.7) where ω is the angular output frequency and ϕ represents the phase angle between voltage and current in each phase.

$$\begin{aligned} v_{a,ref} &= \sqrt{2}\, V_{rms} \sin(\omega t) \\ i_a &= \sqrt{2}\, I_{rms} \sin(\omega t - \phi) \end{aligned} \tag{6.7}$$

6.2.1 Three-Level Operation States of Phase a

Each leg of the three-level ANPC inverter can operate in three main states, "P", "O", and "N" as shown in Fig. 6.8. "P" state refers to the condition that both top switches, Q_1 and Q_2, are switched on. On the other hand in the "N" state tho bottom switches, Q_3 and Q_4, are switched on. It is important to mention that the direction of current can be positive or negative regardless of the state of the leg.

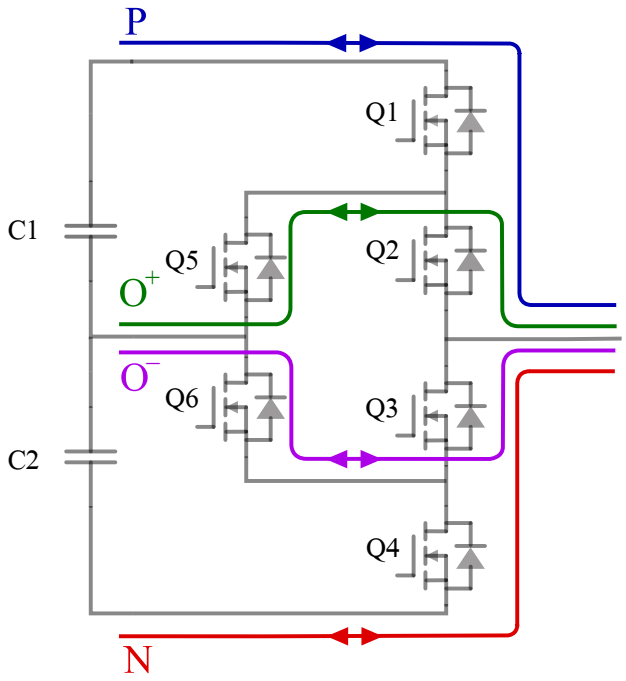


Figure 6.8: Different operating modes in one leg of ANPC inverter

Finally, state "O" refers to the condition that the output is connected to the neutral point (middle point) of the two capacitors. As shown in Fig. 6.8, in a three-level ANPC inverter, state "O" can be realized through two different paths, "O^+" and "O^-". "O^+" mode is achieved through Q_2 and Q_5 switches. On the other hand, "O^-" mode can be realized through Q_3 and Q_6 switches. This flexibility in choosing the "O" state is the main advantage of ANPC structure compared with NPC topology. Although utilizing each of these two options do not change the output waveforms and inverter output characteristics, selecting the proper "O" mode can alter the energy dissipation in the switches of each leg.

In this thesis, the term "Pattern I" is used when the outer switches (Q_1 and Q_4 in leg A) are used for switching to/from "O" state. On the other hand, the term "Pattern II" refers to inner switchings (Q_2 and Q_3 in leg A). Hence, considering a

transition from state "P" to state "O" in leg A, the switching energy is dissipated in Q_1 if pattern I is utilized and in Q_2 if pattern II is employed. Same analysis can be performed for transitions from state "N" to state "O".

In this section, two different approaches are taken for the three-level ANPC inverter loss model, namely averaged loss model (ALM) and partially averaged loss model (PALM).

6.2.2 Average Loss Model (ALM)

In the ALM method, it is assumed that the output frequency is large enough, so that the output fundamental period is larger than or close to the temperature time constant. In this case, the temperature variations during each fundamental output period is ignored and the temperature responds to the average energy loss. Therefore, it can be said that the ALM method for loss calculation is suitable for the temperatures with higher time constant, like the heatsink and the case temperatures of the MOSFET.

Conduction Loss

Calculation of the conduction loss in a power MOSFET requires both on-resistance and the current passing through the MOSFET. Hence, the RMS current and switch junction temperature are needed to be known. The latter will be estimated later in this thesis, in Chapter 7. With a conventional SPWM modulation, Fig. 6.9 depicts the modulating and carrier waveforms which determines the leg state at each instant within the positive half cycle of modulating waveform. Based on the previous discussion, after a transition from state "P" to "O" with pattern I, switches Q_2 and

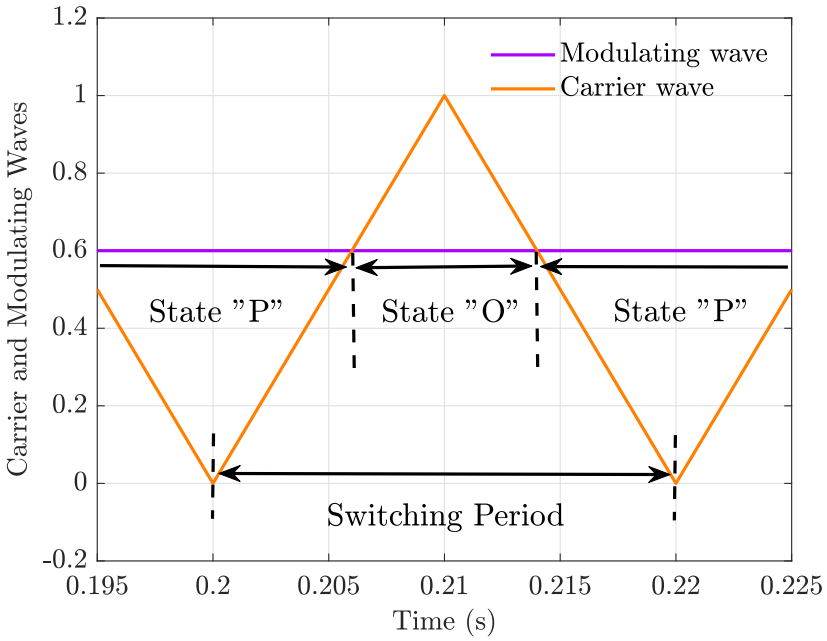


Figure 6.9: Modulating and carrier waveforms in one switching period in the positive half of modulation wave

Q_5 conduct the current, while in pattern II, switches Q_3 and Q_6 conduct. The same approach can be taken for the negative half cycle of the modulating signal, where the state is switching between states "N" and "O".

In the positive half cycle of the modulating signal, the value of duty cycle for Q_1 in phase "a", D_a, is in phase with the phase "a" reference voltage and derives from (6.8), where M is the modulation index defined by (6.9).

$$\begin{aligned} D_a(t) &= M\sin(\omega t)\ ,\ when\sin(\omega t) > 0 \\ &= 0 \qquad\qquad\ ,\ elsewhere \end{aligned} \tag{6.8}$$

$$M = \frac{\sqrt{2}V_{rms}}{V_{dc}/2} \tag{6.9}$$

Based on (6.8), (6.9), and Fig. 6.9, if pattern I is used, the RMS currents passing through each of the 6 switches in leg a, Q_1 are derived in (6.10), (6.11), and (6.12).

$$\begin{aligned} I_{rms,Q_{1,4},P1} &= \sqrt{\frac{1}{2\pi}\int_0^{\pi} D(t)\ i_a^2\ \mathrm{d}\omega t} \\ &= \sqrt{\frac{1}{2\pi}\int_0^{\pi} M\sin\omega t\ (2I_{rms}^2\sin^2(\omega t-\phi))\ \mathrm{d}\omega t} \\ &= I_{rms}\sqrt{\frac{M}{\pi}}\ \sqrt{1+\frac{1}{3}\cos 2\phi} \end{aligned} \tag{6.10}$$

$$\begin{aligned} I_{rms,Q_{2,3},P1} &= \sqrt{\frac{1}{2\pi}\int_0^{\pi} i_a^2\ \mathrm{d}\omega t} \\ &= \frac{I_{rms}}{\sqrt{2}} \end{aligned} \tag{6.11}$$

$$\begin{aligned} I_{rms,Q_1,P1}^2 + I_{rms,Q_5,P1}^2 &= I_{rms,Q_2,P1}^2 \\ \rightarrow I_{rms,Q_{5,6},P1} &= \frac{I_{rms}}{\sqrt{\pi}}\sqrt{\frac{\pi}{2}-\frac{M}{3}(3+\cos(2\phi))} \end{aligned} \tag{6.12}$$

If pattern II is used for switchings from/to "O" states in the whole fundamental period, the instantaneous loss distribution in switches change. However, here we are looking at the average energy loss in one fundamental output period which remains the same. Therefore (6.13) can be written.

$$I_{rms,Q_n,P2} = I_{rms,Q_n,P1} \tag{6.13}$$

Switching Loss

Although the average conduction loss in the switches was shown to be independent of the switching pattern, the switching distribution changes completely with different patterns. In order to determine the switching losses, a fundamental period is divided

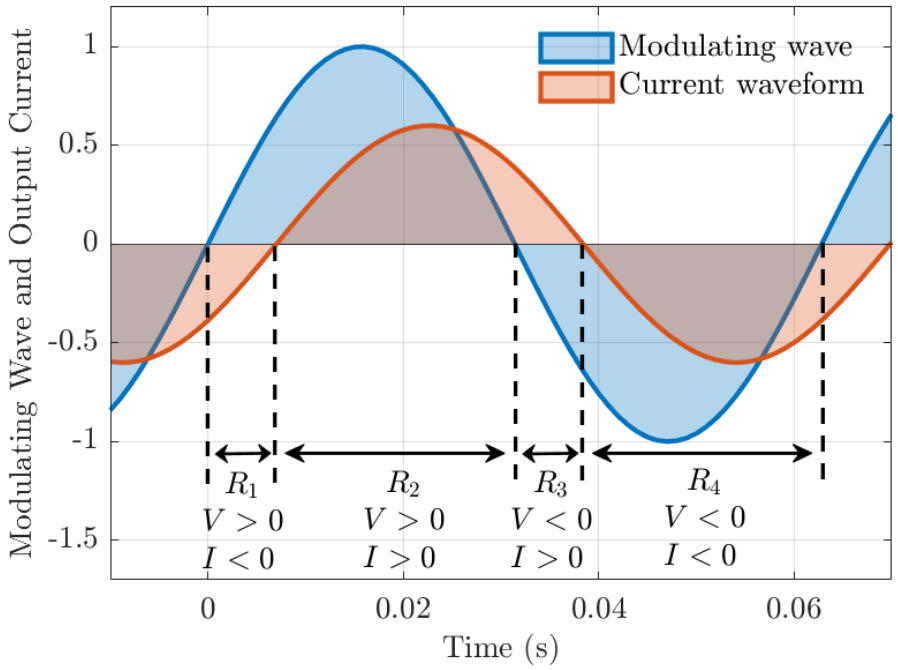


Figure 6.10: Modulating wave and current waveform in one output fundamental period

into four regions based on the sign of modulating waveform and output current of phase "a", as shown in Fig. 6.10. Using Figs. 6.8 and 6.10, the switching loss distribution is listed in Table 6.1 for different operating conditions of phase "a".

The values of E_{on}, E_{off}, and E_{rr} in Table 6.1 are derived based on the current, voltage, and temperature values as discussed in Section 6.1.2. In order to determine the total energy loss in each fundamental period, the power loss should be integrated over the period as shown in (6.14) for switch Q_1 with pattern I as a sample.

Table 6.1: Switching energy loss, E_{sw}, for switches in leg A

	R_2 , $(P \rightarrow O \rightarrow P)$		R_4 , $(N \rightarrow O \rightarrow N)$	
Switch	Pattern I	Pattern II	Pattern I	Pattern II
Q1	$E_{on}+E_{off}+E_{oss}$	0	0	0
Q2	0	$E_{on}+E_{off}+E_{oss}$	0	E_{rr}
Q3	0	E_{rr}	0	$E_{on}+E_{off}+E_{oss}$
Q4	0	0	$E_{on}+E_{off}+E_{oss}$	0
Q5	E_{rr}	0	0	0
Q6	0	0	E_{rr}	0
	R_1 , $(P \rightarrow O \rightarrow P)$		R_3 , $(N \rightarrow O \rightarrow N)$	
Switch	Pattern I	Pattern II	Pattern I	Pattern II
Q1	E_{rr}	0	0	0
Q2	0	E_{rr}	0	$E_{on}+E_{off}+E_{oss}$
Q3	0	$E_{on}+E_{off}+E_{oss}$	0	E_{rr}
Q4	0	0	E_{rr}	0
Q5	$E_{on}+E_{off}+E_{oss}$	0	0	0
Q6	0	0	$E_{on}+E_{off}+E_{oss}$	0

$$\begin{aligned} P_{sw,Q_1,P_1} &= \frac{f_{sw}}{2\pi} \times \int_0^{2\pi} E_{sw,Q_1}(\omega t)\mathrm{d}\omega t \\ &= \frac{f_{sw}}{2\pi} \times [\int_{R_1} E_{rr}(\omega t)\mathrm{d}\omega t + \int_{R_2} (E_{on}(\omega t) + E_{off}(\omega t) + E_{oss}(\omega t))\mathrm{d}\omega t] \end{aligned} \tag{6.14}$$

Eq. (6.14) can be written for all the switches.. The accurate energy loss can be obtained by replacing E_{on}, E_{off}, and E_{rr} from Eq.s (6.2, 6.3, 6.4, 6.5, 6.6) depending on the V_{dc}, T_j, and I_a values. However, for simplifications, the variations of V_{dc} during each cycle can be ignored. Also, the average values of T_j and I_a in each region can be used for deriving the switching energies.

6.2.3 Partially Averaged Loss Model (PALM)

While the ALM method can be used in the temperature model of the heatsink, the junction temperature of the semiconductor switches has a very faster dynamic, which responds to instantaneous energy loss values rather than the average loss magnitude. In other words, two MOSFETs with equal case temperatures can have an equal average energy loss values in a fundamental period, while the maximum junction temperature differs considerably. This will be considered in more details in the next sections with MOSFET equivalent thermal network.

The idea behind PALM is to calculate the energy loss in smaller time steps, called h, in order to model the dynamic behavior of junction temperature more accurately. The length of h will be calculated in a way to limit the junction temperature variations to a predefined maximum value. Then, the energy loss averaging will be done over

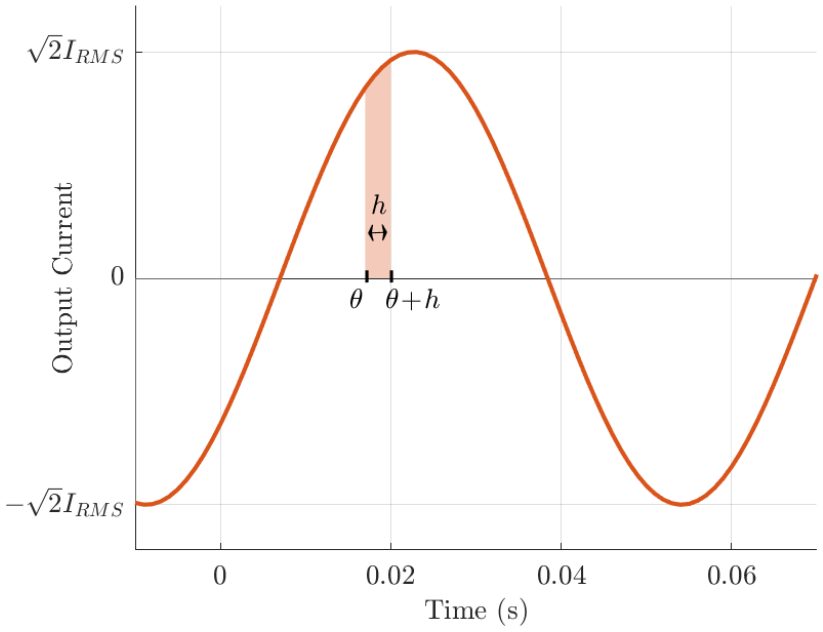


Figure 6.11: Output current waveform and averaging interval, h

these smaller steps instead of the fundamental output period.

Conduction Loss

For measuring the conduction loss over h, the RMS current for each switch must be calculated over this period. The output current waveform, Fig. 6.11, and switches' duty cycles will be used for RMS current calculations as shown in (6.15). The assumption has been made that the switching period, T_s is larger enough than h ($T_s \gg h$).

$$I_{rms,Q_n} = \sqrt{\frac{1}{h}\int_{\theta}^{\theta+h} D_{Q_n}(2I_{rms}^2 \sin^2(\omega t - \phi))\mathrm{d}\omega t} \tag{6.15}$$

By replacing the D_{Q_n} for each of the switches, the results for pattern I and pattern II are shown in (6.16) and (6.17), respectively.

$$\begin{aligned} I_{rms,Q_1,P1} &= I_1 \\ I_{rms,Q_2,P1} &= I_2 \\ I_{rms,Q_5,P1} &= I_3 \end{aligned} \tag{6.16}$$

$$\begin{aligned} I_{rms,Q_1,P2} &= I_1 \\ I_{rms,Q_2,P2} &= I_1 \quad (V_{mod} > 0) \\ I_{rms,Q_2,P2} &= I_3 \quad (V_{mod} < 0) \\ I_{rms,Q_5,P2} &= 0 \quad (V_{mod} > 0) \\ I_{rms,Q_5,P2} &= I_3 \quad (V_{mod} < 0) \end{aligned} \tag{6.17}$$

where:

$$\begin{aligned} I_1 &= I_{rms} \times \\ &\sqrt{\frac{M}{6h}[2[\sin(\frac{4\phi-6\theta-3h}{2})\sin(\frac{3h}{2})] - 6[\sin(\frac{h}{2})\sin(\frac{4\phi+h-2\theta}{2})] + 12[\sin(\frac{h+2\theta}{2})\sin(\frac{h}{2})]]} \\ I_2 &= I_{rms} \times \sqrt{1+\frac{1}{h}\sin(2h)\cos(4\theta+2h-4\phi)} \\ I_3 &= \sqrt{I_2^2 - I_1^2} \end{aligned} \tag{6.18}$$

It can be seen that the RMS values calculated in (6.18), can put a large computational burden on the processor in practice, since they have to be calculated in the short periods of h. Therefore, an approximation will be used here to lower the required calculations in practice.

Assuming that the fundamental output period is significantly larger than h, the current change is each h interval is small. Therefore, the RMS current is approximated with the average of current at the beginning and the end of interval. In other words,

the RMS current in the h interval shown in Fig. 6.11 is approximated by:

$$I_{rms,h} \approx \frac{I(\theta) + I(\theta + h)}{2} \tag{6.19}$$

A more aggressive approximation, aiming at further simplification of the experimental control system, is to approximate the RMS current with the sampled current at the moment θ:

$$I_{rms,h} \approx I(\theta) \tag{6.20}$$

The latest approximation allows for removing all mathematical operations for I_{rms} calculation. Hence, the sampled current at each moment can be used to derive an approximate conduction loss. The error magnitude of the two approximation methods introduced depends greatly on the $(\theta - \phi)$ value. When $(\theta - \phi)$ is close to zero, the rate of change of current is large which makes the approximations inaccurate. However, on the plus side, when $(\theta - \phi)$ is close to zero in phase "a", the losses in phase "a" switches are usually at their minimum. This will show its importance in the next chapters. The error magnitude of these loss models, with and without approximations, will be compared later in this chapter.

Switching Loss

For switching loss calculations, Table 6.1 and Eq. (6.14) can be used again for all switches. However, the averaging interval is h instead of $0 - 2\pi$. Therefore, (6.21) can be written.

$$P_{sw,Q_n} = \frac{f_{sw}}{h} \times \int_{\theta}^{\theta+h} E_{sw,Q_n}(\omega t)\mathrm{d}\omega t \tag{6.21}$$

Similar to the conduction loss calculations in PALM method, the accurate switching loss calculation is not practical in the experiment. Therefore, again an approximation is made to ease the computation of E_{on} and E_{off}. First, instead of integrating E_{sw} over period h, E_{sw} is considered constant with the value at the beginning of the period:

$$P_{sw,Q_n} = f_{sw} E_{sw,Q_n}(\theta) \tag{6.22}$$

Additionally, the cubic relation of E_{on} and E_{off} with respect to current in (6.3) is simplified with a linear equation:

$$E_{on/off,PU,2} = \frac{I_d}{50} \tag{6.23}$$

These simplifications reduces the processor computational burden significantly.

6.3 Verifying the Loss Model

In this section, the accuracy of the presented loss models, as well as the approximation errors are investigated. A Simulink/PLECS co-simulation is used for this purpose. The switch loss model is used in a three-level inverter simulated in PLECS, while the gate pulses are generated in the control system in the Simulink environment.

Table 6.2: Conduction loss in Q_1, $\phi = \frac{\pi}{6}$, $T_j = 60$, $M = 1$ for currents from 20 A to 60 A

Current (A)	$P_{Cond,PLECS}$	$P_{Cond,ALM}$	Error %
20	3.55	3.54	0.26
30	7.99	7.97	0.29
40	14.25	14.17	0.59
50	22.32	22.14	0.82
60	32.20	31.87	1.01

Table 6.3: Conduction loss in Q_1, $\phi = \frac{\pi}{3}$, $T_j = 60$, $M = 1$ for currents from 20 A to 60 A

Current (A)	$P_{Cond,PLECS}$	$P_{Cond,ALM}$	Error %
20	2.54	2.53	0.37
30	5.71	5.69	0.43
40	10.19	10.12	0.70
50	15.96	15.81	0.94
60	23.03	22.77	1.14

6.3.1 Average Loss Model (ALM)

For verification of the ALM method, different operating conditions are tested with different current, voltage, and temperature values. The resulting values for both conduction and switching losses for Q_1, as well as the error values are listed in Tables 6.2 to 6.5 where different operating conditions are considered.

The estimation error of conduction loss remains below 1.5% at all operating conditions with for all the switches. Also, the estimation error of switching loss remains below 2% at all operating conditions with for all the switches. However, by estimating the current with its average value at each period, which makes the calculations faster, the estimation error reaches up to 8 % of the actual switching loss value.

Table 6.4: Switching loss in Q_1, $\phi = \frac{\pi}{6}$, $T_j = 60$, $M = 1$ for currents from 20 A to 60 A

Current (A)	$P_{Sw,PLECS}$	$P_{Sw,ALM}$	Error %	$P_{Sw,ALM,Estimation}$	Error %
20	4.64	4.67	0.63	4.45	4.09
30	7.59	7.63	0.58	7.21	4.97
40	11.33	11.27	0.53	10.62	6.28
50	15.70	15.45	1.63	14.57	7.20
60	20.41	20.04	1.82	18.99	6.98

Table 6.5: Switching loss in Q_1, $\phi = \frac{\pi}{3}$, $T_j = 60$, $M = 1$ for currents from 20 A to 60 A

Current (A)	$P_{Sw,PLECS}$	$P_{Sw,ALM}$	Error %	$P_{Sw,ALM,Estimation}$	Error %
20	4.87	4.90	0.51	4.65	4.64
30	7.94	7.97	0.36	7.47	5.88
40	11.81	11.73	0.69	10.95	7.24
50	16.33	16.05	1.70	15.01	8.10
60	21.20	20.81	1.85	19.54	7.84

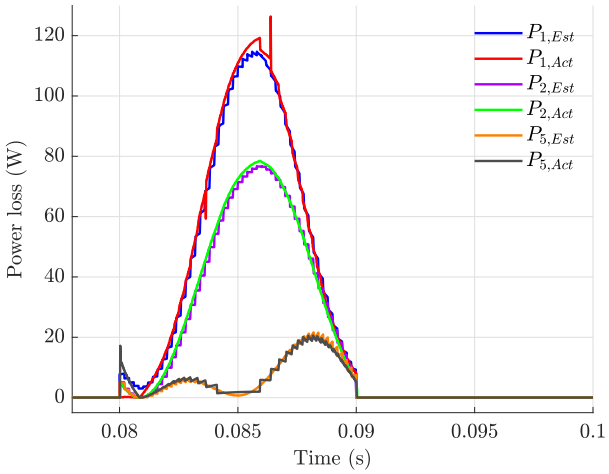


Figure 6.12: Loss comparison with Pattern I, $h = 200\mu s$ in $Q_{1,2,5}$, $\phi = \frac{\pi}{12}$, $T_j = 60$, $M = 1$ for 40 A current

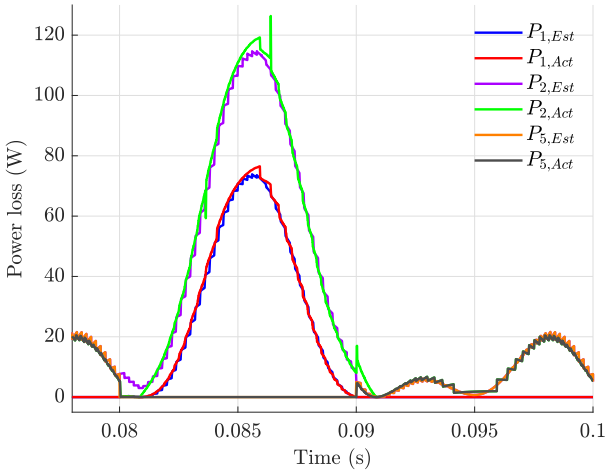


Figure 6.13: Loss comparison with Pattern II, $h = 200\mu s$ in $Q_{1,2,5}$, $\phi = \frac{\pi}{12}$, $T_j = 60$, $M = 1$ for 40 A current

6.3.2 Partially Averaged Loss Model (PALM)

In order to verify the PALM estimation, an estimation period, h, equal to 200 us, and 500 us are considered. Figures 6.12 to 6.15 shows a comparison between the accurate instantaneous loss values versus the PALM method. The most simple current

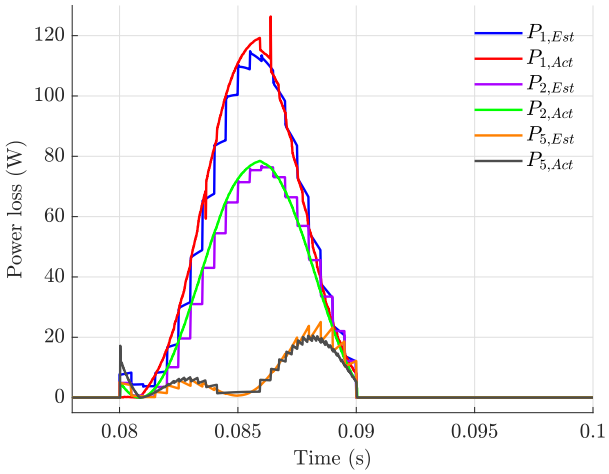


Figure 6.14: Loss comparison with Pattern I, $h = 500\mu s$ in $Q_{1,2,5}$, $\phi = \frac{\pi}{12}$, $T_j = 60$, $M = 1$ for 40 A current

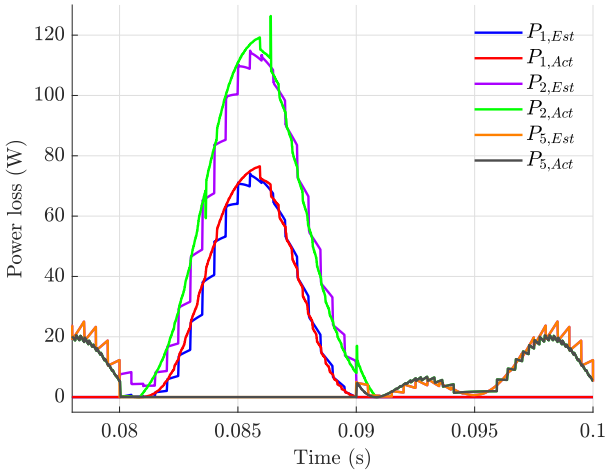


Figure 6.15: Loss comparison with Pattern II, $h = 500\mu s$ in $Q_{1,2,5}$, $\phi = \frac{\pi}{12}$, $T_j = 60$, $M = 1$ for 40 A current

estimation in (6.20) is used.

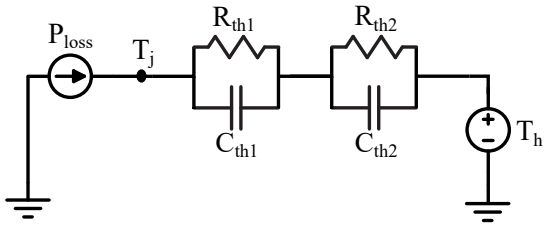


Figure 6.16: Foster equivalent thermal network

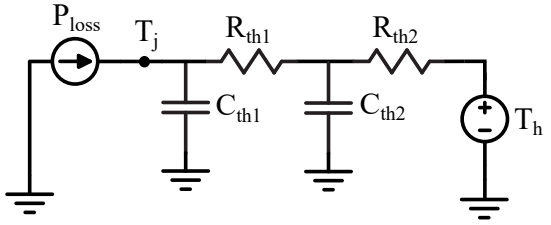


Figure 6.17: Cauer equivalent thermal network

6.4 MOSFET Junction Temperature Estimation

Traditionally, two types of equivalent thermal networks have been used to model semiconductor devices. Foster and Cauer networks, shown in Figs. 6.16 and 6.17, can be used to estimate the junction temperature when the case temperature and power loss values are known. While the equivalent voltage of each node in the cauer network indicates the actual temperature of a MOSFET layer, the *RC* blocks in foster network don't have physical meaning and it can only be used for junction temperature estimation [200]. Foster network is chosen in this thesis due to more simple calculations. Assuming a first-order foster network with a single *RC* block, the junction to case temperature, ΔT_{jc} after a period of T_{th} with power loss P can be estimated as (6.24) [201]:

$$\Delta T_{jc}^{(t_0+T_{th})} = R_{th} * (1 - e^{(\frac{-T_{th}}{R_{th}C_{th}})}) * P + (e^{(\frac{-T_{th}}{R_{th}C_{th}})}) * \Delta T_{jc}^{(t_0)} \tag{6.24}$$

Then, by adding T_c to ΔT_{jc}, junction temperature, T_j, can be obtained.

Although the first-order foster network gives an estimate of the average junction temperature of the semiconductor, it cannot accurately model the dynamic behaviour of the junction temperature. Hence, a more accurate thermal network which consists of two or three RC blocks can model the fast dynamics as well as the steady-state situation. For a second-order foster network shown in Fig. 6.16, Eq. (6.25) can be used in two steps for calculating the junction temperature of the switch.

$$\begin{aligned}\Delta T_{jm}^{(t_0+T_{th})} &= R_{th1} * (1 - e^{(\frac{-T_{th}}{R_{th1}C_{th1}})}) * P + (e^{(\frac{-T_{th}}{R_{th1}C_{th1}})}) * \Delta T_{jm}^{(t_0)} \\ \Delta T_{mc}^{(t_0+T_{th})} &= R_{th2} * (1 - e^{(\frac{-T_{th}}{R_{th2}C_{th2}})}) * P + (e^{(\frac{-T_{th}}{R_{th2}C_{th2}})}) * \Delta T_{mc}^{(t_0)}\end{aligned} \tag{6.25}$$

6.5 MOSFET Junction Temperature Measurement

There are many physical and computational limitations to directly measuring the temperatures of internal layers in a typical TO-247 package with optical and physical contact methods [202] . Due to its importance in reliability of the power converters, several indirect approaches have been proposed in the literature to measure the junction temperature in power electronic devices.

Some of the parameters of power devices are variable with temperature. These parameters are called "Temperature-sensitive electrical parameters (TSEP)" [203]. By measuring the TSEPs, the junction temperature of the device is obtained indirectly. These methods prove to be fast, accurate, and low-cost. However, dependency of TSEPs on other parameters besides temperature is the main limitations of these methods. In the past decades, many studies have been performed for using static and dynamic TSEPs to measure junction temperature of Si IGBTs [204].

While the mentioned studies have covered temperature measurement in Si IGBTs, the methods are different in SiC MOSFETs due to their different physical characteristics. Usually, following approaches can be taken to indirectly measure the junction temperature in SiC MOSFETs:

- On-Resistance (Rds(on))
- Miller plateau voltage (Vgp)
- Turn-off delay time (td(off))
- Threshold voltage (Vth)

The on-resistance is a TSEP in a SiC MOSFET which can be used to measure the junction temperature indirectly. Fig. 6.2 illustrates the change in Rds(on) for a sample SiC MOSFET, namely UJ4C075018K4S, with respect to junction temperature.

Although the resistance can not be measured straightly during the converter operation, it can be calculated once the Vds(on) and Ids(on) are known. Hence, by adding voltage and current measurement circuits to the system, internal junction temperature can be estimated. In [202], this measurement has been performed using a drain-to-source voltage measurement circuit and a lookup table to extract the temperature value. The results are compared to two direct temperature measurement techniques where they have shown accordance with the optical measurement technique.

6.6 Thermal Model of the Inverter

In the previous sections, the junction temperatures of the MOSFETs were estimated based on a known case temperature. However, the temperature at different locations on the heatsink can be estimated by extracting a thermal model for the heatsink.

Based on [205], a foster-based equivalent thermal model can be extracted for a heatsink using a foster equivalent network for modeling the temperature rise at each position due to the heat applied at other locations. By applying constant heat into each section separately, and measuring the temperature in all sections, the thermal impedance Z_{ij} is defined as the thermal impedance at section i on the heatsink, caused by the heat dissipated at location j as written in (6.26):

$$Z_{ij} = \frac{\Delta T_{H_{iC}}(t)}{P_j} \tag{6.26}$$

Consequently, an impedance matrix can be formed for a heatsink divided into n locations as shown in (6.27).

$$Z = \begin{bmatrix} Z_{11} & \dots & Z_{1n} \\ \vdots & \ddots & \vdots \\ Z_{n1} & \dots & Z_{nn} \end{bmatrix} \tag{6.27}$$

Based on [206], the temperatures at each heatsink position can be calculated at each time instant using (6.28). T_c in (6.28) is the coolant inlet temperature.

$$\begin{bmatrix} T_{HS1}(t) \\ \vdots \\ T_{HS9}(t) \end{bmatrix} = \int_0^t \begin{bmatrix} \dot{Z}_{11}(t-\tau) & \dots & \dot{Z}_{1n}(t-\tau) \\ \vdots & \ddots & \\ \dot{Z}_{n1}(t-\tau) & & \dot{Z}_{nn}(t-\tau) \end{bmatrix} \begin{bmatrix} P_1(\tau) \\ \vdots \\ P_n(\tau) \end{bmatrix} d\tau + T_C \tag{6.28}$$

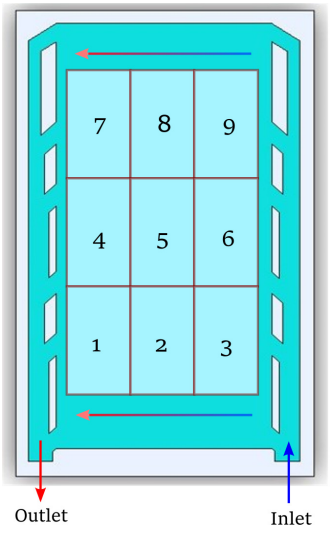


Figure 6.18: Coolant block and its sections for thermal modeling

6.7 Experimental Verification of Loss and Thermal Models

In order to apply the proposed hotspot minimization algorithm to the experimental setup (which will be discussed in Chapter 7), the actual thermal parameters of the system needs to be extracted. Although a more accurate thermal model can be extracted using intensive mechanical simulations and tests, the goal here is to obtain a less accurate but simple model that can be evaluated in real-time by the available microcontrollers on the market. Hence, based on [205] and by conducting some experimental tests, a thermal model will be extracted to be used in the next steps of the experiments. The experimental setup's fin base on which the MOSFETs are mounted is divided into 9 sections as shown in Fig. 6.18.

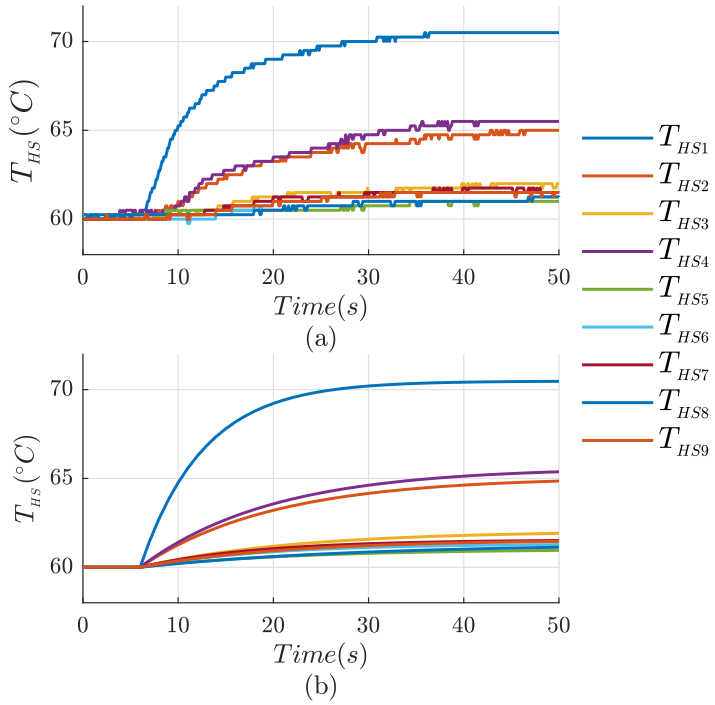


Figure 6.19: The temperature change in heatsink sections when the heat is applied to section HS1. a) Experimentally extracted temperatures and b) curve-fitted first-order foster network

Heatsink Parameters

To measure the heatsink temperature right underneath each MOSFET, thin K-type thermocouples have been placed inside the vented screws used for mounting the MOSFETs on the plate. The thermocouple amplifier circuitry along with the serial communication with the microcontroller allows for on-line temperature measurements in steps of $0.25^{\circ}C$. The coolant temperature is first set to 60° and then, to apply the heat at each position on the plate, a controlled short circuit with limited current is created using the MOSFETs at desired locations. The resulting conduction losses of the MOSFET determines the loss value. At coolant inlet temperature of 60°, a maximum of 120 W can be dissipated per MOSFET based on the MOSFET and

source capabilities. As an example, the temperature changes in all heatsink sections is plotted in Fig. 6.19(a) when 40 W power is dissipated in section 1 of the heatsink.

Since the thermal model is needed for temperature predictions, each of the thermal impedances between the two points is fitted to the response of a first-order foster network as written in (6.29).

$$f(t) = PR(1 - e^{(\frac{-t}{RC})}) \tag{6.29}$$

Fig. 6.19(b) depicts the fitted curves. An impedance matrix can be formed for the heatsink using the extracted thermal parameters as shown in (6.30).

$$\begin{bmatrix} R_{ij} \\ C_{ij} \end{bmatrix} = \begin{bmatrix} \begin{bmatrix} 0.26 \\ 25 \end{bmatrix} & \begin{bmatrix} 0.14 \\ 101 \end{bmatrix} & \begin{bmatrix} 0.06 \\ 281 \end{bmatrix} & \begin{bmatrix} 0.16 \\ 101 \end{bmatrix} & \begin{bmatrix} 0.04 \\ 397 \end{bmatrix} & \begin{bmatrix} 0.04 \\ 372 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 301 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 394 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 347 \end{bmatrix} \\ \begin{bmatrix} 0.13 \\ 110 \end{bmatrix} & \begin{bmatrix} 0.24 \\ 27 \end{bmatrix} & \begin{bmatrix} 0.14 \\ 100 \end{bmatrix} & \begin{bmatrix} 0.06 \\ 263 \end{bmatrix} & \begin{bmatrix} 0.13 \\ 134 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 244 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 410 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 402 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 369 \end{bmatrix} \\ \begin{bmatrix} 0.05 \\ 316 \end{bmatrix} & \begin{bmatrix} 0.12 \\ 140 \end{bmatrix} & \begin{bmatrix} 0.19 \\ 31 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 212 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 297 \end{bmatrix} & \begin{bmatrix} 0.11 \\ 162 \end{bmatrix} & \begin{bmatrix} 0.02 \\ 603 \end{bmatrix} & \begin{bmatrix} 0.02 \\ 659 \end{bmatrix} & \begin{bmatrix} 0.02 \\ 590 \end{bmatrix} \\ \begin{bmatrix} 0.14 \\ 98 \end{bmatrix} & \begin{bmatrix} 0.06 \\ 258 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 266 \end{bmatrix} & \begin{bmatrix} 0.25 \\ 25 \end{bmatrix} & \begin{bmatrix} 0.15 \\ 93 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 309 \end{bmatrix} & \begin{bmatrix} 0.13 \\ 94 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 402 \end{bmatrix} & \begin{bmatrix} 0.04 \\ 375 \end{bmatrix} \\ \begin{bmatrix} 0.03 \\ 649 \end{bmatrix} & \begin{bmatrix} 0.14 \\ 113 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 245 \end{bmatrix} & \begin{bmatrix} 0.12 \\ 165 \end{bmatrix} & \begin{bmatrix} 0.25 \\ 27 \end{bmatrix} & \begin{bmatrix} 0.14 \\ 97 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 284 \end{bmatrix} & \begin{bmatrix} 0.13 \\ 121 \end{bmatrix} & \begin{bmatrix} 0.06 \\ 208 \end{bmatrix} \\ \begin{bmatrix} 0.03 \\ 393 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 296 \end{bmatrix} & \begin{bmatrix} 0.12 \\ 122 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 517 \end{bmatrix} & \begin{bmatrix} 0.11 \\ 189 \end{bmatrix} & \begin{bmatrix} 0.22 \\ 30 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 346 \end{bmatrix} & \begin{bmatrix} 0.04 \\ 381 \end{bmatrix} & \begin{bmatrix} 0.09 \\ 190 \end{bmatrix} \\ \begin{bmatrix} 0.04 \\ 320 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 349 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 317 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 128 \end{bmatrix} & \begin{bmatrix} 0.04 \\ 480 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 497 \end{bmatrix} & \begin{bmatrix} 0.24 \\ 28 \end{bmatrix} & \begin{bmatrix} 0.12 \\ 131 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 243 \end{bmatrix} \\ \begin{bmatrix} 0.03 \\ 695 \end{bmatrix} & \begin{bmatrix} 0.04 \\ 309 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 284 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 284 \end{bmatrix} & \begin{bmatrix} 0.12 \\ 124 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 307 \end{bmatrix} & \begin{bmatrix} 0.11 \\ 142 \end{bmatrix} & \begin{bmatrix} 0.22 \\ 31 \end{bmatrix} & \begin{bmatrix} 0.13 \\ 295 \end{bmatrix} \\ \begin{bmatrix} 0.04 \\ 396 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 355 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 290 \end{bmatrix} & \begin{bmatrix} 0.03 \\ 312 \end{bmatrix} & \begin{bmatrix} 0.04 \\ 409 \end{bmatrix} & \begin{bmatrix} 0.13 \\ 101 \end{bmatrix} & \begin{bmatrix} 0.05 \\ 276 \end{bmatrix} & \begin{bmatrix} 0.13 \\ 314 \end{bmatrix} & \begin{bmatrix} 0.21 \\ 32 \end{bmatrix} \end{bmatrix} \tag{6.30}$$

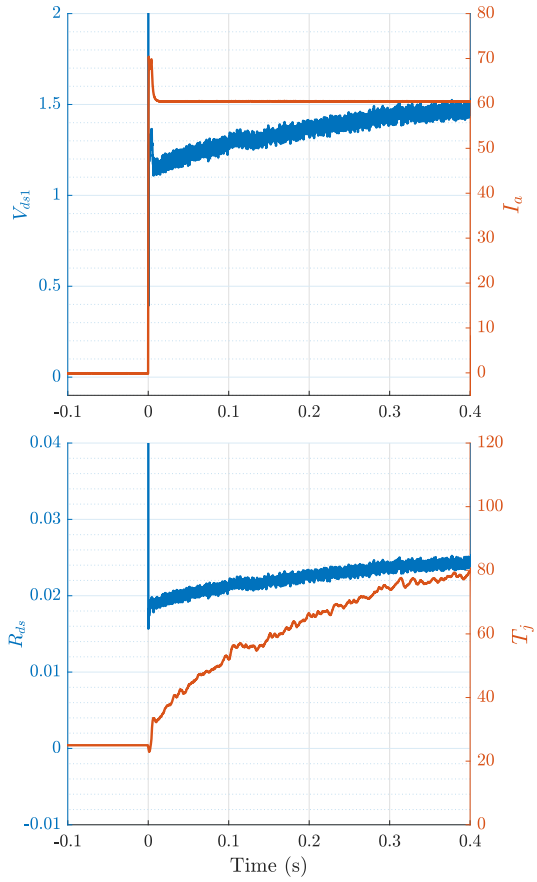


Figure 6.20: High-current pulse tests an V_{on} measurement for extracting thermal characteristics

Junction to Heatsink Parameters

The MOSFET's junction to case thermal model is usually known from the manufacturer datasheet as discussed before. However, the manufacturing uncertainties, silicone pad, and thermal grease present between the tab and the heatsink introduces additional thermal components to the previously investigated model which needs to be extracted for a more accurate thermal model.

To extract the thermal parameters, high current tests are performed on the MOSFETs, where an intentional short circuit is made in the leg, and a pulse current of up to 100 A is passed through the switches for very short periods of time as shown in Fig. 6.20. By measuring the changes in on-resistance, the changes in junction temperatures of switches are extracted versus the amount of dissipated energy in the MOSFETs. Based on the changes in the on-resistance, the junction temperature can be extracted as shown in Fig. 6.20. Curve fitting tool can be used to fit the extracted thermal impedance to a second-order foster network.

6.8 Summary

In this Chapter, an electro-thermal model was derived for the three-level ANPC inverter to be used in the following Chapter in hotspot temperature estimation of the inverter. In order to derive the electo-thermal model, first, two loss model was developed for the inverter. One is modeling the temperature rise on the heatsink plate due to average loss in the MOSFETs, while the second model which has a faster dynamic response models the junction temperature rise in the MOSFETs caused by the energy loss in smaller time intervals. These models are verified by comparing its outputs to the outputs of the PLECS model. Then, the thermal model of the inverter was derived based on the first and second-order equivalent foster networks.

Due to the tolerances in MOSFET datasheet values as well as the unmodelled components such as the thermal pad between the MOSFET tab and heatsink, the actual thermal parameters were derived based on some experimental tests, performed at the end of this Chapter. The tests were performed by adding loss to the MOSFETs by making controlled short circuits at low voltages and estimating the junction

temperatures by measuring the V_{ds}. Also, heatsink temperatures are measured using thermocouples. A second-order foster network for the MOSFETs, as well as a first-order foster matrix for the heatsink were derived and will be used in Chapter 7 for junction temperature estimation.

Chapter 7

Improving the Power Density of the Inverter using the Proposed Electro-Thermal Model and a Modified Sinusoidal Pulse-Width Modulation (SPWM) Technique

One major limiting factor for having power dense power electronic converters is the unequal maximum junction temperature among the power switches. This unequal junction temperature is a result of first, different energy loss in each switch, and second, unequal case temperatures and unsymmetrical thermal models. This issue needs even more attention in case of multilevel inverters, where the number of switches has increased compared to the conventional inverters. In case of a three-level NPC

inverter, the number of semiconductor devices has increased from 6 to 18. Moreover, an NPC inverter suffers from a lack of flexibility in distributing the power loss in the switches. This drawback leads to some switches being the limiting factor for increasing the power rating of the inverter while the other switches are not utilized with their maximum capability [207].

The three-level ANPC structure, which is the focus of this thesis, has managed to solve the aforementioned power loss sharing issue by employing two different modulation techniques, called modulation pattern I and pattern II [208]. After deriving the loss model of the three-level ANPC inverter in both operating patterns and the thermal model of the implemented inverter and verifying them in Chapter 6, this chapter deals with modifying the well-known SPWM model to be able to minimize the maximum junction temperatures of the switches in each leg of the inverter, while keeping the simplicity of the SPWM technique. After a review of existing solutions in the literature, the proposed method is explained. First, the thermal interval, T_{th}, will be derived based on the estimation equations and the maximum power loss in the switches. Then, the modified SPWM technique is proposed. The theoretical analysis will be followed by the simulation results which compares the proposed modification to the conventional SPWM, as well as previous works. The experimental results are also presented at the end of the chapter.

7.1 Existing Solutions for Junction Temperature Balancing

In [209] and [210], hybrid ANPC structures are investigated and compared to each other in terms of power loss sharing. In a hybrid structure, inner or outer IGBTs are replaced with SiC MOSFETs with low turn-on/turn-off losses. The proper modulation pattern is then utilized to ensure that the switching loss occurs in the low-loss SiC devices. Although the hybrid structures has proven to increase the power density and decrease the junction temperature gap in certain operating conditions, there is no temperature balancing algorithm which aggravates the temperature gap when the operating condition of the inverter varies.

Another modulating strategy, called double-frequency (DF) modulation, is investigated in [208]. With DF modulation method, switching events happen evenly among the inner and outer switches. Hence, switching loss is equally distributed. However, the conduction loss is higher in inner switches than outer switches which turns the inner switches to the inverter's hotspot. There is no temperature balancing algorithm to control the distribution of the instantaneous energy loss in the semiconductors. Also, this method does not consider the inverter's electro-thermal model and unbalance in the case temperatures of the switching devices.

A loss balancing algorithm is proposed in [211], named an adaptive loss distribution (ALD). In this method, the conduction losses of the inner and outer switches are derived based on the operating conditions of the inverter, mainly power factor and modulation index. Based on the gap between the switches conduction losses, a switching loss distribution ratio is derived which controls the modulation modes. Although

this method proves to be more efficient in temperature balancing, its drawback is that the thermal model of the switch is not employed for temperature estimation. Without utilizing the online temperature estimation, although the losses can be distributed evenly in a period of time, the gap between instantaneous junction temperatures in transient conditions can not be reduced effectively. Another drawback of the proposed modulation method is that the difference in the case temperatures of the switches in an actual inverter leg is not taken into account.

A more advanced junction temperature balancing is proposed in [212] and [213], where the switch foster thermal model is employed for online junction temperature estimation. The idea in [212] is to optimize the distribution of the power loss in each switching cycle by using the calculated instantaneous power loss and the foster equivalent network. Although this method is more effective than the previously discussed approaches, its main drawback is the extremely large computations required during each switching period which makes it impractical to go to high switching frequencies, especially when high-level foster networks are employed. The experimental tests in [212] are performed at the low switching frequency of 1 kHz. Also, the variations in the case temperatures of switches in an actual high-power setup is not considered.

Some studies in the literature have proposed model-predictive control (MPC) for the three-level ANPC where junction temperature balancing is added as an additional objective term to the cost function [201, 214]. One major drawback of using this control method for junction temperature balancing is the large computation burden when the temperature estimation is going to happen at each switching cycle.

7.2 Thermal Interval Derivation

A thermal interval is determined in this chapter, so that real-time thermal calculations can be performed at a lower frequency which is independent of the switching frequency. If the thermal interval is too large, the control system can not effectively reduce the maximum junction temperature. On the other hand, if the interval is small, the microcontroller can not perform the calculations due to large computational burden. Hence, using the MOSFET equivalent thermal network, the maximum allowed thermal interval is calculated to limit the junction temperature fluctuations. The first step is to determine the time step for thermal calculations, T_{th}. This interval is selected in a way to ensure that the junction temperature change in one T_{th} does not exceed a predefined limit, $\delta T_{j,lim}$, as written in 7.1:

$$\Delta T_{jc}^{(t_0+T_{th})} < \Delta T_{jc}^{(t_0)} + \delta T_{j,lim} \tag{7.1}$$

By replacing 7.1 into 6.24, T_{th} maximum value can be calculated as:

$$\Delta T_{jc}^{(t_0)} + \delta T_{j,lim} > R_{th} * (1 - e^{(\frac{-T_{th}}{R_{th}C_{th}})}) * P + (e^{(\frac{-T_{th}}{R_{th}C_{th}})}) * \Delta T_{jc}^{(t_0)} \tag{7.2}$$

Eq. 7.2 can be rewritten after some simplifications as Eq. 7.3:

$$(1 - e^{(\frac{-T_{th}}{R_{th}C_{th}})}) * [R_{th} * P - \Delta T_{jc}^{(t_0)}] < \delta T_{j,lim} \tag{7.3}$$

Since the maximum power loss in each switch is known and the minimum $\Delta T_{jc}^{(t_0)}$ is equal to zero, the only variable than can be controlled to limit the left-hand side of (7.3) is T_{th}. Hence, the proper value for T_{th} is extracted.

The calculations can be done for the two-step foster network as well. The final

simplified derived equation is shown in 7.4:

$$(1-e^{(\frac{-T_{th}}{R_{th1}C_{th1}})})*[R_{th1}*P-\Delta T_{jm}^{(t_0)}]+(1-e^{(\frac{-T_{th}}{R_{th2}C_{th2}})})*[R_{th2}*P-\Delta T_{mc}^{(t_0)}] < \delta T_{j,lim} \quad (7.4)$$

Equivalently, by knowing all the worst case values in (7.4), T_{th} is the only parameter that determines the maximum junction temperature change in a single thermal step. In the designed inverter, the maximum power loss in a single switch equals to 65 Watts. Assuming that the goal is to limit the maximum junction temperature change in a single thermal step, δT_j to 3 $^{\circ}C$, maximum T_{th} will be 400 μs. It needs to be mentioned that with a smaller T_{th}, the control will be more effective at junction temperature minimization. However, the calculations required for this method cannot be executed in the small period in the processor. Therefore, the T_{th} value is extracted based on the discussed method.

7.3 Proposed Junction Temperature Estimation

By knowing the value of T_{th} and the power loss value for each MOSFET, the junction temperature of all switches in each leg can be estimated at steps of T_{th} for each of the two patterns. For this purpose, Eq. (6.24) and (6.25) can be used for first-order and second-order foster networks, respectively.

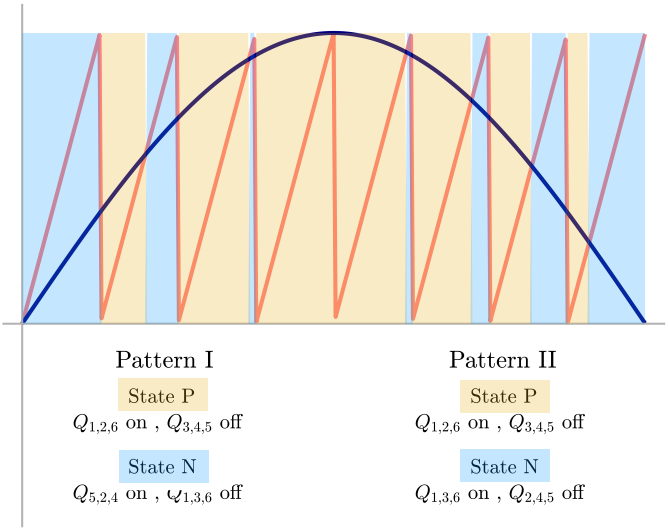


Figure 7.1: Realization of states P and O using SPWM modulation with patterns I and II

7.3.1 Proposed Method for Pattern Control

For each leg, the junction temperature of each of the switches needs to be estimated. Then, the pattern which leads to a lower maximum junction temperature will be selected and applied to the switches in the corresponding inverter leg. The method for applying the patterns using a simple SPWM modulation is depicted in Fig. 7.1. Using the proposed method in this thesis, Fig. 7.2 illustrates the modulation technique in which the utilized pattern is changing based on the junction temperature estimation at steps of T_{th}. Also, a flowchart of the proposed control technique is depicted in Fig. 7.3.

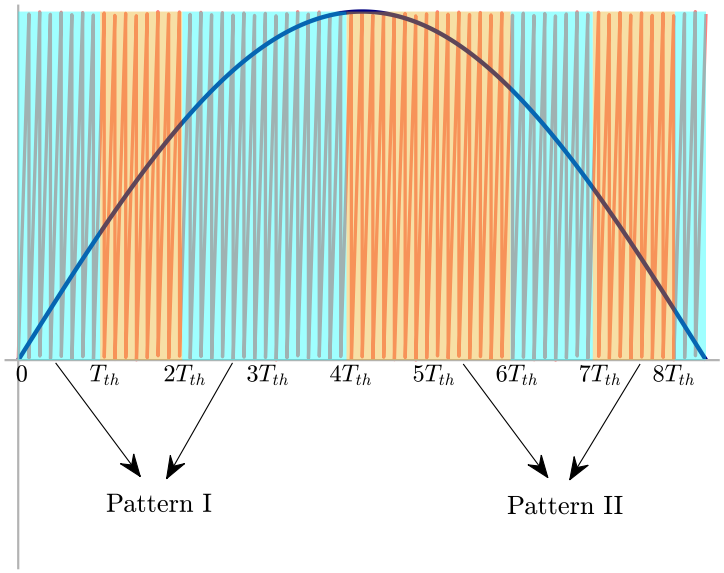


Figure 7.2: An example of switching between patterns I and II at periods of T_{th}

While Fig. 7.3 shows the junction temperature estimation based on the instantaneous voltages and currents, a second loop is also implemented in the microcontroller for case temperature estimations. In this second loop, which is performed in larger time steps, the average energy loss in all switches is used with the proposed heatsink thermal model of (6.30) to estimate the temperature on all the positions on the heatsink.

7.3.2 Sensitivity Analysis

While the derived equations for calculating ΔT across a single block of foster network are accurate and no approximation is made in their derivation, the inaccuracy of loss and thermal parameters can lead to an inexact temperature calculation. This

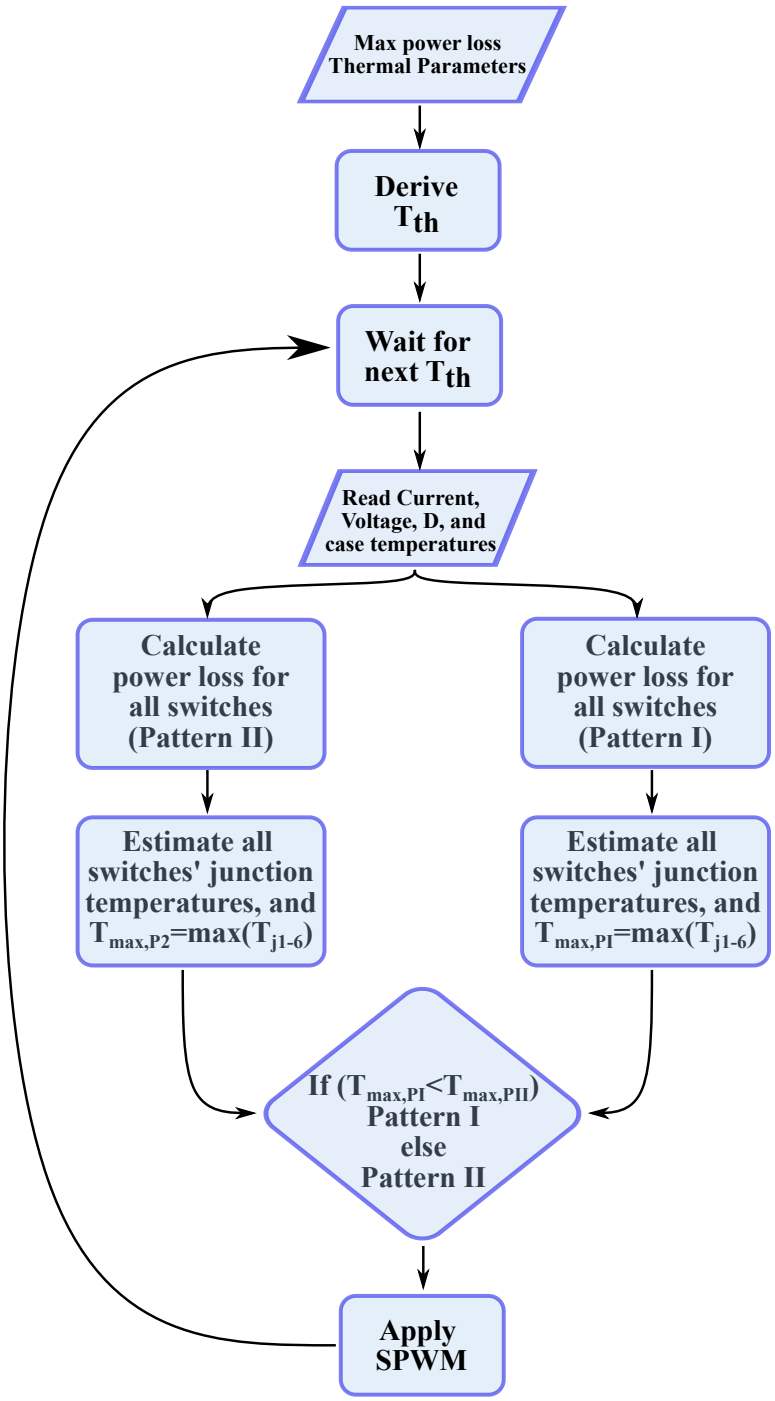


Figure 7.3: A flowchart of the proposed technique

inaccuracy in the thermal parameters results from a variety of sources. First, according to the datasheets of most industrial MOSFETs, the R_{th} values can vary by even 30% in two similar devices. Second source of uncertainty is the external factors. For example, the thermal pads which are usually placed between the MOSFET tab and the heatsink can increase the total R_{th} by an uncertain value which directly depends on the pressure on the pad.

To investigate the sensitivity of the temperature calculation to the uncertainty in thermal parameters, this subsection presents a sensitivity analysis and determines the sensitivity to different parameters in different situations.

In order to determine the sensitivity of (6.24) to the thermal variables, partial derivatives of 6.24 to R_{th} and C_{th} are calculated as shown in 7.5 and 7.6.

$$\frac{\partial(\Delta T_{jc}^{(t_0+T_{th})})}{\partial R_{th}} = P[(1-e^{(\frac{-T_{th}}{R_{th}C_{th}})}) + R_{th}(\frac{T_{th}}{R_{th}^2 C_{th}} e^{(\frac{-T_{th}}{R_{th}C_{th}})})] + \Delta T_{jc}^{(t_0)}(\frac{T_{th}}{R_{th}^2 C_{th}} * e^{(\frac{-T_{th}}{R_{th}C_{th}})}) \tag{7.5}$$

$$\frac{\partial(\Delta T_{jc}^{(t_0+T_{th})})}{\partial C_{th}} = R_{th}P(\frac{T_{th}}{R_{th}C_{th}^2} e^{(\frac{-T_{th}}{R_{th}C_{th}})}) + \Delta T_{jc}^{(t_0)}(\frac{T_{th}}{R_{th}C_{th}^2} * e^{(\frac{-T_{th}}{R_{th}C_{th}})}) \tag{7.6}$$

By replacing R_{th} and C_{th} in the equations with their values for a semiconductor device, the sensitivity values can be extracted and compared. By plugging in the $R_{th} = 0.35$ and $C_{th} = 0.0036$, which are the values of a first order foster network,

corresponding to an SiC MOSFET with TO-247 package (UJ4C075018K4S), the sensitivity values for 50 W power loss is as follows:

$$\begin{aligned} \frac{\partial(\Delta T_{jc}^{(t_0+T_{th})})}{\partial R_{th}} &= 56 \\ \frac{\partial(\Delta T_{jc}^{(t_0+T_{th})})}{\partial C_{th}} &= 1578 \end{aligned} \tag{7.7}$$

A direct outcome of calculating the sensitivity values is that a small variation in the thermal parameters can result in large deviation in accuracy of the formula. This small variations could happen due to manufacturing tolerances, thermal pad R_{th}, etc. Hence, in Chapter 6, the accurate thermal parameters of the semiconductors were extracted using some high current pulse tests on the MOSFETs to minimize the uncertainty of these parameters.

7.4 Simulation Results

The proposed control method for reducing the hotspot temperature in a three-level ANPC inverter is simulated using a Simulink/PLECS co-simulation. The main specifications of the simulated inverter is listed in Table. 7.1. The main loss-related parameters as well as the extracted thermal network components for a second-order foster network are presented in Table. 7.2. In this section, the results obtained from the proposed hotspot temperature minimization method is compared to the results of pattern I, pattern II, and equal loss distribution control methods. The dynamic response of the junction temperature controller to sudden changes in load is presented, as well as its operation under constant three-phase load.

Table 7.1: Simulated Inverter Specifications

Parameter	Value
Rated Input Voltage	800 V
Rated Output RMS Current	80 A
Selected Switch	UJ4C075018K4S
Switching Frequency	50 kHz

Table 7.2: Selected MOSFET Characteristics

Parameter	Value
Rated R_{on} at 25C (mΩ)	18
E_{on} and E_{off} at 400V, 50A (μ J)	453, 304
2nd-order Foster R_{th1}, C_{th1}	0.255, 0.027
2nd-order Foster R_{th2}, C_{th2}	0.135, 0.0014

7.4.1 Constant Load, Equal Case Temperatures

In this subsection, the simulations have been performed for an RL load with a power factor of 0.86. The modulation index, M, is set to 1 and the case temperatures for all the switches is considered to be equal to $60°C$. The control circuit is simulated in Simulink, while the power stage in simulated in PLECS. The junction temperatures of the switches are achieved based on the switching and conduction losses and thermal characteristics of the MOSFETs.

Fig. 7.4 shows the junction temperatures of the six MOSFETs in one leg of the converter for each of the four control methods. Pattern I, pattern II, equal loss distribution control, and the proposed equal junction temperature control techniques are used and compared to each other. The maximum junction temperature in the

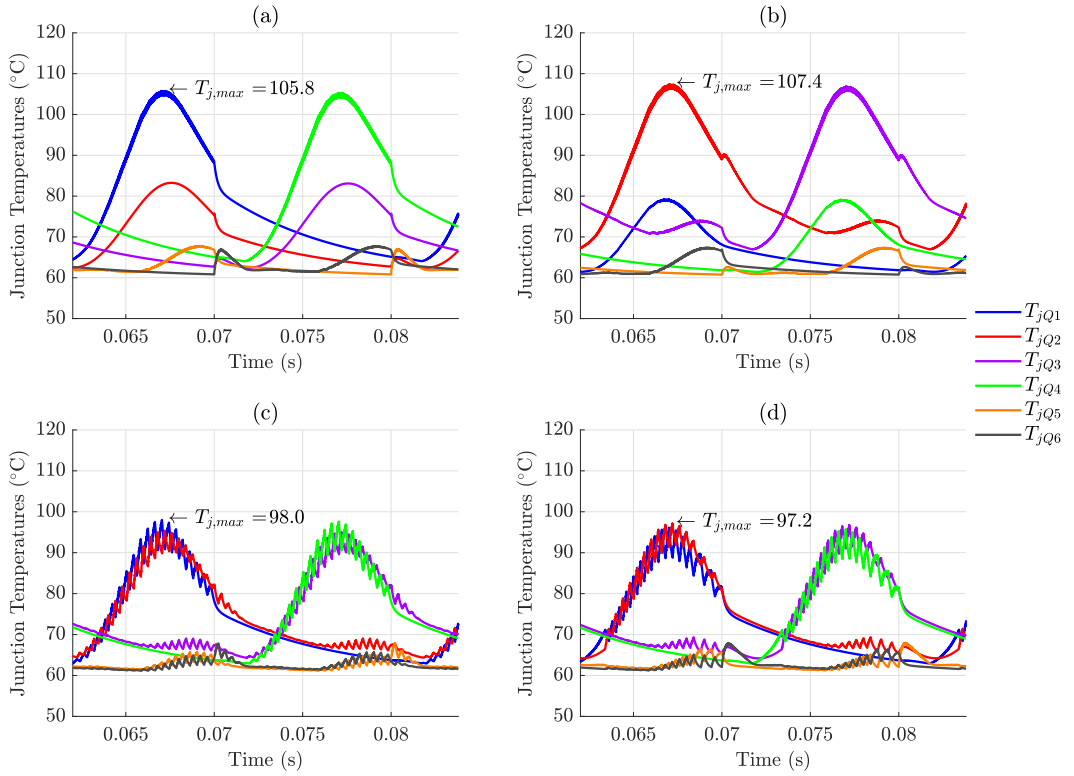


Figure 7.4: Junction temperatures of the switches with equal case temperatures in one leg of the inverter, using a) pattern I, b) pattern II, c) equal power loss distribution, and d) proposed equal junction temperature technique.

switches of each leg is specified in each case.

7.4.2 Constant Load, Unequal Case Temperatures

In the previous case, both equal loss distribution method and the proposed technique proved to result in the lowest maximum junction temperature compared to other techniques. However, in many experimental setups, the case temperatures of the MOSFETs may not be totally equal. Therefore, in the simulations in this section, the inner switches are considered to be closer to the coolant input which results in

Table 7.3: Summary of Comparison between the four control methods

	Equal T_c		Unequal T_c	
Control method	Max T_j	$P_{density}$	Max T_j	$P_{density}$
Pattern I	105.8	100%	110.5	100%
Pattern II	107.4	98.2%	102.7	108.7%
Equal loss	98.0	109.4%	102.7	108.8%
Proposed method	97.2	110%	98.3	113.7%

lower case temperature (this assumption is based on the designed cooling system for the experimental setup). Fig. 7.5 shows the junction temperatures of all the switches in one leg of the inverter. The case temperature of the outer switches, clamping switches, and inner switches are set to $63°C$, $60°C$, and $57°C$, respectively.

A direct consequence of the reduction of maximum junction temperature is increasing the maximum output power of the inverter and hence, improving the power density. Using the results of the mentioned simulations, Table 7.3 summarizes the maximum junction temperatures in each case, as well as the increase in the maximum output power that can be achieved in each case compared to the pattern I.

It can be seen that in the case of equal case temperature, both equal loss and proposed technique result in almost 10% increase in the power density of the inverter. However, when the case temperatures are not the same, the proposed minimum junction temperature method can be the most effective control method in terms of power density improvement by more than 13% increase in power density compared to pattern I.

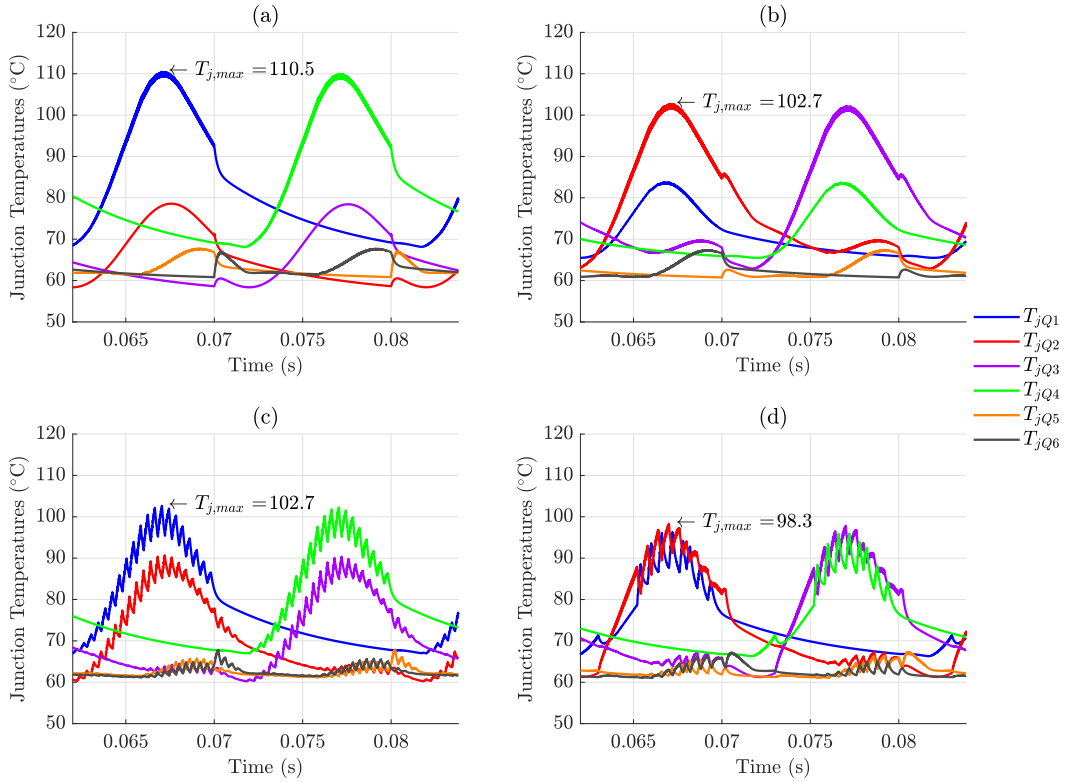


Figure 7.5: Junction temperatures of the switches with unequal case temperatures in one leg of the inverter, using a) pattern I, b) pattern II, c) equal power loss distribution, and d) proposed equal junction temperature technique.

7.4.3 Dynamic Response

In order to evaluate the dynamic response of the proposed technique and compare it to the equal loss balancing method, a dynamic scenario has been employed and simulated in which the value of M is changed at $t = 0.065s$ from 0.5 to 1. The results of equal loss balancing control, and the proposed minimum junction temperature technique in this dynamic situation is depicted in Fig. 7.6. It can be seen that in case of the equal loss balancing control, there is a considerable gap in the temperatures of the switches for one period before the new ratio is calculated. However, with the

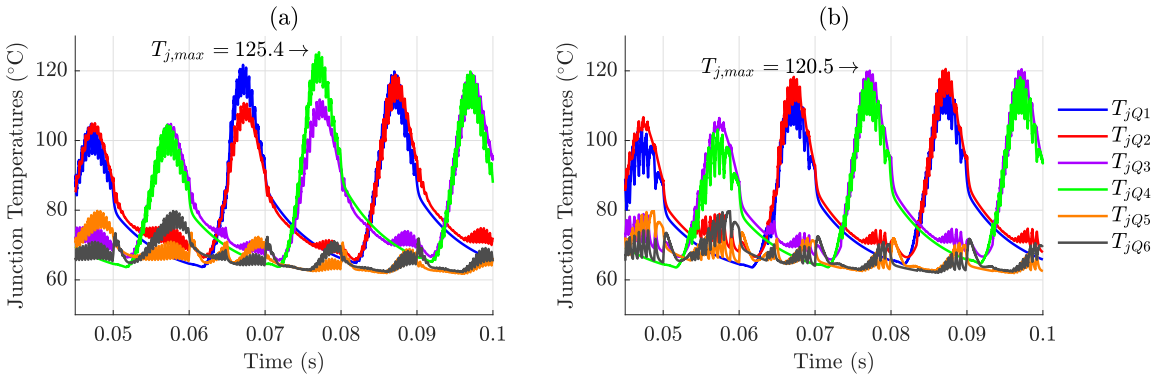


Figure 7.6: Dynamic response of the junction temperatures of the switches under two control methods for a change in M at $t = 0.065s$; a) equal loss balancing control, and b) proposed equal junction temperature technique

proposed technique, the balance between the temperatures of the hot switches is kept in the transition instances at the cost of a larger required computational burden.

7.5 Experimental Results

In this section the proposed method is implemented on the experiment setup. An RL load with power factor of 0.86, is tested. The results are presented for different output currents and DC-link voltages.

7.5.1 Junction Temperatures

The experimental tests have been run using all the four methods introduced in the simulations section. The junction temperature of the MOSFETs are monitored by measuring drain to source voltage as well as the output current. The resulting on-resistance can give an estimation of the junction temperature. The final maximum temperature results are extracted from the measured on-resistances for the two hottest

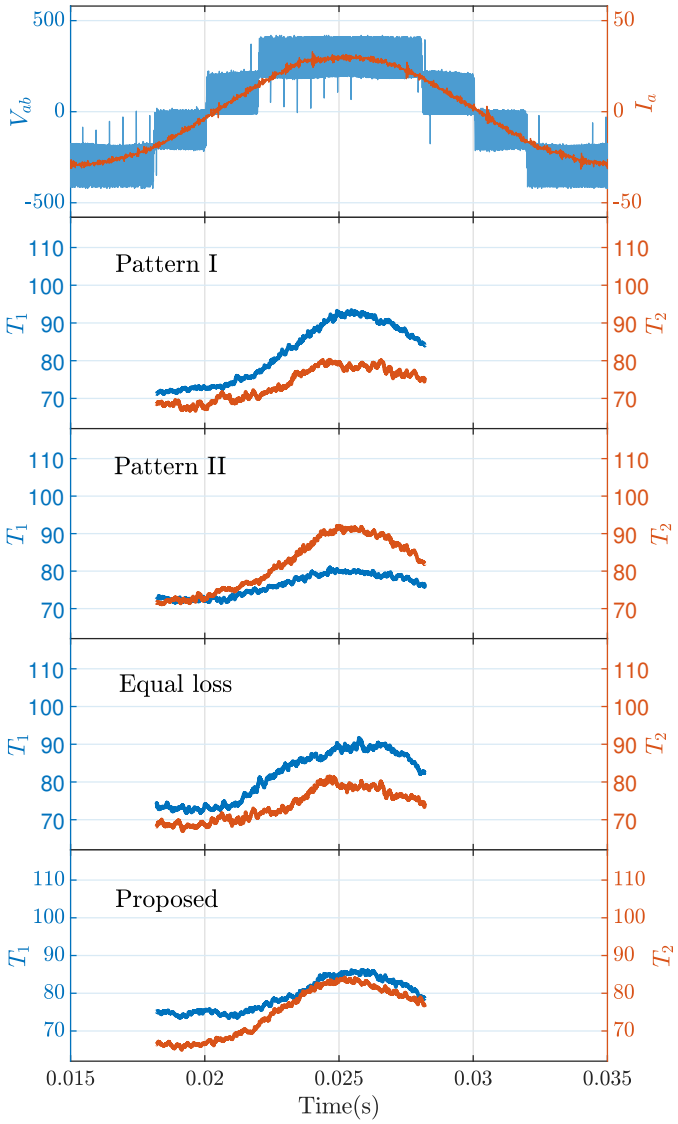


Figure 7.7: output waveforms and junction temperature measurement of two hotspot switches in leg A

switches in one leg of the converter. The results of the current waveforms and junction temperature measurements are presented for a sample operating condition in Fig. 7.7.

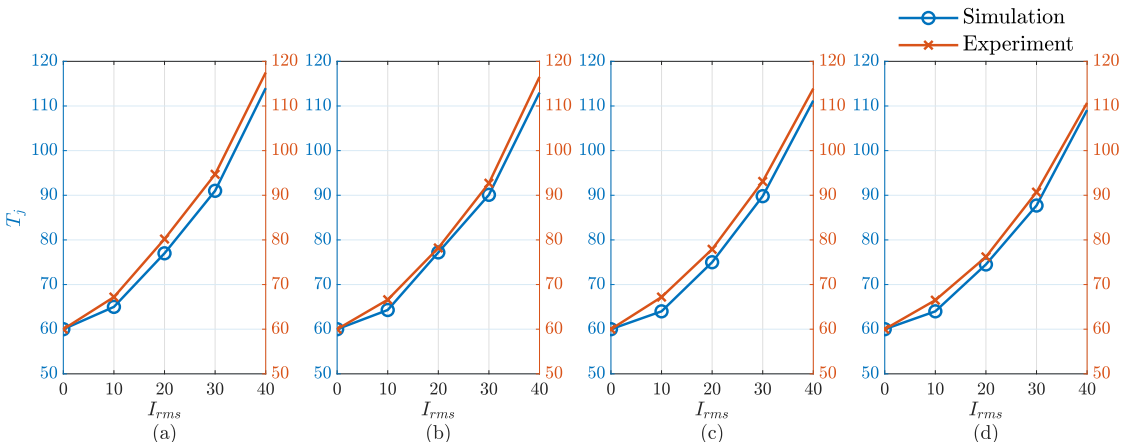


Figure 7.8: Comparison of simulation and experimental results for M=1; a) Pattern I, b) Pattern II, c) equall loss balancing, and d) proposed method

It should be mentioned that in the negative half cycle of the modulating waveform, switches Q_1 and Q_2 are not conducting for most of the period and the junction temperatures can not be measured with this technique.

Figures 7.8 and 7.9 show the maximum temperatures in different output current values for RL loads, with modulation index of 1 and 0.5, respectively. It should be mentioned that since V_{dc} and M are being kept constant in each case, the change in the output current is achieved by changing the RL load impedance. By using the proposed control method on the operating conditions, a reduction of 6.2, 5.9, and 3.8 degrees can be observed when compared to pattern I, pattern II, and equal loss distribution techniques, respectively.

7.5.2 Power Density Improvement and Protection

Two direct outcomes of the proposed technique are the power density improvement and protecting the inverter. Two major limiting factors regarding power density in an inverter are the junction temperature of the switches and the DC-link capacitors.

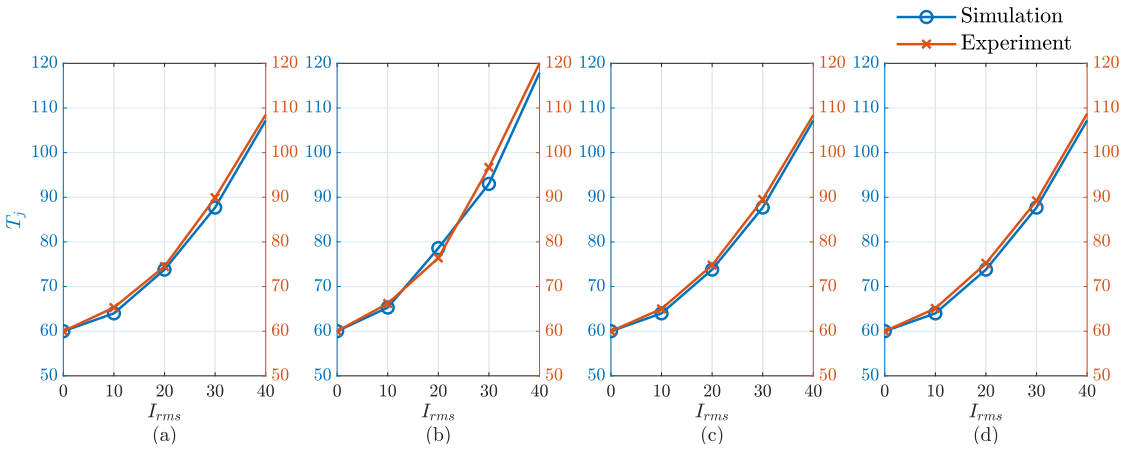


Figure 7.9: Comparison of simulation and experimental results for M=0.5; a) Pattern I, b) Pattern II, c) equall loss balancing, and d) proposed method

Assuming that the DC-link capacitors allow for higher currents, the proposed method can increase the power density by decreasing the hotspot junction temperature in the inverter. Considering the worst case scenario, an improvement of 12% was achieved when compared to Pattern I and Pattern II methods. Also, an improvement of 4.5% is achieved when compared to the equal loss balancing method. Additionally, the proposed method offers a level of protection in which the inverter's control system has the junction temperatures information. If the junction temperature in one switch exceed the limit, the inverter can limit the output current to avoid a breakdown.

7.6 Summary

With the aggressive power density requirements of the traction inverters, especially in EVs, new methods must be developed to increase the maximum power outputs in the inverters.

Junction temperatures of the switching devices are one of the major limiting

factors in power density improvement of an inverter. This effect is much more considerable in case of some multilevel inverter structures where the energy loss distribution in the MOSFETs is not equal. The NPC inverter suffers from this issue greatly due to a lack of flexibility in distributing the conduction and switching losses.

By using an ANPC structure, the flexibility in selecting state "O" results in an effective way of redistributing the energy loss in inner and outer switches of each leg. Using the electro-thermal model introduced in Chapter 6, the junction temperatures of the switches can be effectively estimated in intervals of T_{th} with both patterns I and II. The method which results in lower maximum temperature is applied to the inverter for the next T_{th} period.

The simulation and experimental results verify the effectiveness of the proposed technique where the power density of the inverter with improved by 12% and 4.5% when compared to basic patterns and equal loss balancing technique, respectively.

Chapter 8

Model Predictive Control (MPC) of a Three-Level ANPC Inverter with Reduced Control Set Elements

With the new generations of the microprocessors, DSPs, and FPGAs, some control techniques, which usually have heavier computational burden, especially for multilevel inverters, have become feasible. Hysteresis-based control, dead-beat control, and model-predictive control (MPC) are some of these control methods [215].

In MPC technique, based on the system mathematical model, the requirements, and the control objectives, a cost function (CF) is formed and the optimal values for the control variables are selected. Very fast response, satisfying multiple objectives simultaneously, and handling non-linearities are among the interesting features of

MPC technique. On the other hand, large computational burden, high sensitivity to model parameters, and varying switching frequency are the major drawbacks of MPC for drive applications compared to scalar, FOC and DTC techniques [143, 216].

In this chapter, MPC technique is used to control the three-level ANPC inverter. Different terms are added to the cost function in order to control the output current, balance the capacitor voltages, and minimize the switching transients. The computational burden of the MPC controller is reduced with some improvements to an existing MPC method. Additionally, other terms have been proposed to be added to the cost function in order to reduce the hotspot temperature in the inverter.

8.1 Literature

MPC scheme has been applied to traction drive control system in the literature [217–220]. However, some new challenges and opportunities arise when moving to multilevel inverters. This section presents a survey over these issues and the proper solution to them based on the available studies in the literature.

8.1.1 Computational Burden

In power electronic converters, unlike most MPC application in control systems, finite control set MPC (FCS-MPC) is usually used. Hence, instead of solving an optimization problem, all the feasible outcomes are plugged into the CF to determine the one that minimizes the CF. Its schematic can be seen in Fig. 8.1. Due to the larger number of levels in multilevel structures, the number of control set elements is larger. For example, the number of CF evaluations at each step increases from 8 to 27 when

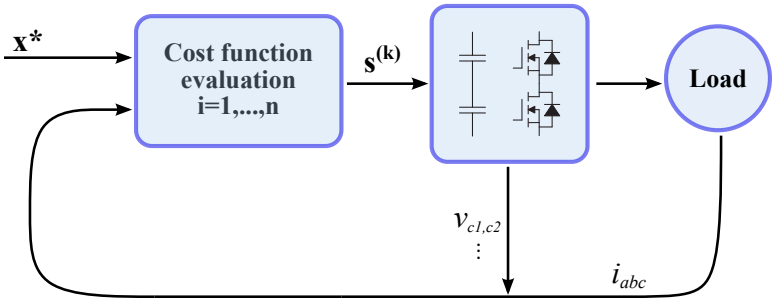


Figure 8.1: A simple FCS-MPC control schematic for drive system

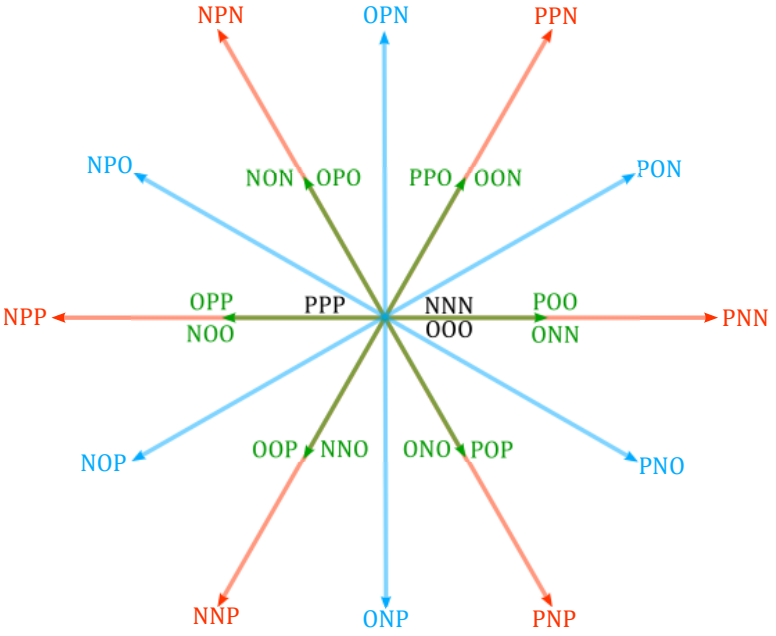


Figure 8.2: 27 Control actions in a three-level ANPC inverter

moving from a two-level inverter to a three-level structure. All possible control action in a three-level ANPC inverter can be seen in the SVD shown in Fig. 8.2.

Finding the appropriate solution to this issue, which becomes more significant as the number of levels goes higher, has been the subject of multiple studies in the literature.

In [221], the control set of a three-level inverter in for induction motor drive

application is reduced from the conventional 27 actions to 17 actions without sub-optimality. In this method, first, only the actions are evaluated which make a large vector in the as shown in Fig. 8.2 in red color. Therefore, six evaluations are performed in this stage. Using this method, the large vector that gives the minimum value of cost function will be determined. It worth mentioning that since the large vectors don't affect the voltage balancing, only the current control term determines the optimal large vector. In the second stage, all the small and medium vectors closest to the selected large vector will be evaluated in the cost function. For example, assuming that the "PNN" large vector has resulted in minimum CF in the first stage, all the vectors in the area shown in Fig. 8.3 will be examined in the second stage. Hence, in the second stage, a total of 11 control actions are evaluated. Therefore, the total number of CF calculation drops from 27 to 17. It needs to be mentioned that all three zero vectors, "OOO", "NNN", and "PPP" are considered in the second stage regardless of the section to ensure minimum switching frequency.

Another simplification method for a three-level NPC inverter is proposed in [222]. In the mentioned study, the authors have managed to reduce the total number of CF calculations in each sampling period. In the first evaluation stage, the voltage balancing is ignored. Therefore, the two redundant vectors corresponding to each small vector result in a similar CF value since they represent similar magnitude and phase on the SVD. Same procedure will be done regarding the three zero vectors. Therefore, instead of evaluating all vectors, a total of 13 control actions are evaluated in both steps.

Another efficient finite set MPC is proposed in [216] for a seven-level inverter. The control objectives are to control the output currents and maintain floating capacitors'

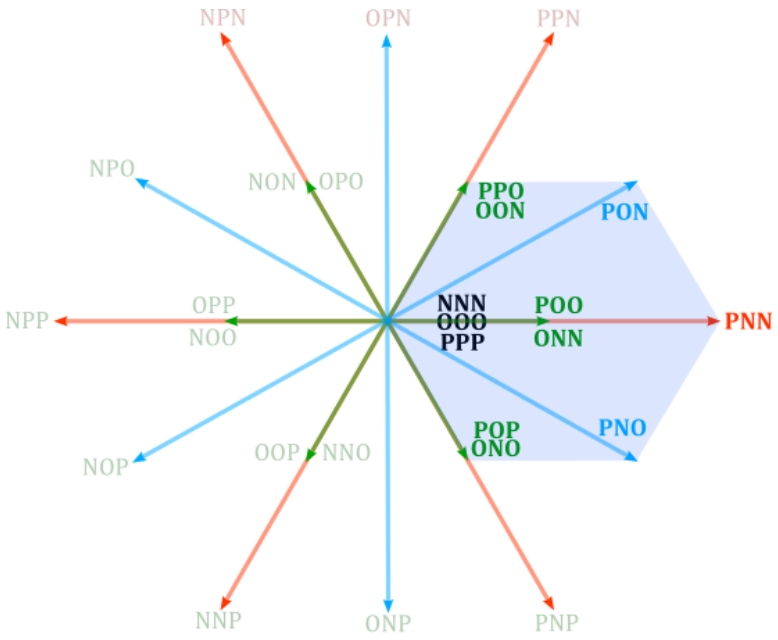


Figure 8.3: 11 Candidate control actions for stage 2 when PNN is selected in stage 1

voltage on the determined value. In the proposed method, an approximation has been made in order to separate the phase voltages, output currents, and the voltages of floating capacitors.

8.1.2 Fixed Switching Frequency

Since an MPC controller decides about the next control action regardless of the previous ones, the switching frequency of the switches is not fixed. This results in a wide switching frequency spectrum in the output. Some solutions have been proposed to address this drawback. In [223], a modulated MPC (M^2PC) is used. A SVM modulator is used with the conventional MPC scheme for a fixed output frequency. Another method for limiting the variation range of switching frequency is to introduce a bandstop digital filter into the cost function. Although effective, this

method might deteriorate the dynamic response of the controller [215].

8.1.3 Voltage Balancing

One challenge that is exclusive to the multilevel structures is the capacitor voltage balancing. The capacitor voltage balancing with MPC technique can be as simple as adding one more term with the appropriate weighting factor to the cost function. However, in an attempt to eliminate the weighting factors from the cost function, in [215] a single-objective CF for current control is used, while the voltage regulation is realized by using the redundant vectors through a modulator stage. Another method, introduced in [224], balances the capacitor voltages by injecting an offset voltage to the reference based on the capacitors' voltage difference.

8.1.4 Common-Mode Voltage Reduction

Due to the presence of redundant vectors with different generated CMVs in multilevel inverters, another term can simply be added to the CF to consider the generated CMV by each vector. Another solution is to eliminate the control actions which results in large CMV from consideration in the CF.

8.1.5 Implementation

Due to the discontinuous nature of the digital control systems, the derived states at each step will be applied to the switches in the next sampling period. This results in a one-step delay in the control. The controller, first, uses the currently applied variables to predict the system state at (t^{k+1}). Then, the CF will be evaluated for

(t^{k+2}) with all the available control actions to find out the minimum.

Another challenge in implementing the MPC controller is determining the weighting factors for each term in the CF. Since there is no theoretical way to do this for a multilevel inverter in this application, these factors are determined empirically. Also, some studies have proposed methods to eliminate the need for weighting factors. As an example, in [222], the need for determining a weighting factor for voltage balancing term is eliminated by introducing a permissible range for voltage imbalance ϵ. When the voltage imbalance is smaller than ϵ , voltage balancing is not considered in the optimal state derivation.

Another issue that needs to be addressed in the MPC scheme is to improve the robustness of the controller and reduce the effect of the parameter mismatches. Some studies have investigated this issue [225, 226].

8.2 Conventional and Simplified Finite Control Set MPC (FCS-MPC) for Three-Level ANPC Inverter

8.2.1 Conventional FCS-MPC for Three-Level Inverter with RL Load

Since the FCS-MPC technique in this thesis is going to be studied for an RL load, the model of the a three-phase RL load can be written as follows in (8.1):

$$\begin{cases} V_\alpha = Ri_\alpha + L\dfrac{di_\alpha}{dt} \\ \\ V_\beta = Ri_\beta + L\dfrac{di_\beta}{dt} \end{cases} \tag{8.1}$$

Using the Euler discretization method, the current component at the instant (k+1) can be written as (8.2):

$$\begin{cases} i_\alpha^{(k+1)} = (1 - \dfrac{RT_s}{L})i_\alpha^{(k)} + \dfrac{T_s}{L}V_\alpha^{(k)} \\ \\ i_\beta^{(k+1)} = (1 - \dfrac{RT_s}{L})i_\beta^{(k)} + \dfrac{T_s}{L}V_\beta^{(k)} \end{cases} \tag{8.2}$$

Moreover, the current passing through the neutral point (NP) in Fig. 5.1 determines the capacitors' voltage difference. Since the sum of capacitor voltage should remain constant and equal to V_{dc}, the NP current is divided into two equal currents with different directions in top and bottom capacitors. Hence, the capacitors' voltage difference at the instant (k+1) can be written as (8.3):

$$\Delta V_c^{(k+1)} = \Delta V_c^{(k)} + \frac{T_s}{C}(i_{NP}^{(k)}) \tag{8.3}$$

Where i_{NP} can be calculated based on the three-phase currents and leg states as (8.4):

$$i_{NP}^k = (1 - |S_a^k|)i_a^k + (1 - |S_b^k|)i_b^k + (1 - |S_c^k|)i_c^k \tag{8.4}$$

Due to the one-step digital delay present in the microprocessor implementation of MPC technique, (8.2) and (8.3) can be rewritten as (8.5) and (8.6):

$$\begin{cases} i_{\alpha}^{p(k+2)} = (1 - \dfrac{RT_s}{L}) i_{\alpha}^{p(k+1)} + \dfrac{T_s}{L} V_{\alpha}^{p(k+1)} \\ \\ i_{\beta}^{(pk+2)} = (1 - \dfrac{RT_s}{L}) i_{\beta}^{p(k+1)} + \dfrac{T_s}{L} V_{\beta}^{p(k+1)} \end{cases} \tag{8.5}$$

$$\Delta V_c^{(k+2)} = \Delta V_c^{(k+1)} + \frac{T_s}{C}(i_{NP}^{(k+1)}) \tag{8.6}$$

In the conventional MPC technique for three-level ANPC inverter, the CF can be written as follows (8.7):

$$\begin{aligned} CF = (i_{\alpha}^{*(k+2)} - i_{\alpha}^{p(k+2)})^2 + (i_{\beta}^{*(k+2)} - i_{\beta}^{p(k+2)})^2 \\ + \lambda_v (\Delta V_c^{(k+2)})^2 + \lambda_s (N_s)^2 \end{aligned} \tag{8.7}$$

Where N_s is the sum of number of switchings in the three legs in the transition from instant $(k+1)$ to instant $(k+2)$. Also, λ_v and λ_s are the weighting factors for minimizing NPV and the number of switchings.

In a conventional three-level MPC technique, all the feasible vectors in the SVD are replaced in (8.7) and the vector that results in the minimum CF value will be selected for applying in the next sampling period. Therefore, the number of iterations in each sampling period is 27. The improvements that have been previously proposed for this controller mainly focused on first, reducing the number of iterations and second, eliminating the weighting factors.

8.2.2 Simplified FCS-MPC for Three-Level Inverter

In [221] a two-stage simplified method is presented to reduce the number of iterations per sampling time from 27 to 17. In this method, first, all the large vectors are evaluated in the CF. The vector that brings the minimum CF value is selected for the second stage of calculations.

In the second stage, 11 adjacent vectors to the selected large vector will be evaluated with the same CF. Then, the minimum amount of the CF is compared to the CF value for the selected large vector and the smaller value determines the vector that will be applied at the instant $(k+1)$.

This simplified method has reduced the computational burden of the microcontroller to 66% of conventional approach. However, this burden is still considerably large. Also, the weighting factors for neutral point voltage balancing is still present in the CF and no mathematical method is presented to effectively choose their values.

8.3 Proposed MPC Technique

In an attempt to further simplify the MPC technique for three-level inverters and eliminate the weighting factors, a two-stage approach is proposed in here. After investigating these two stages, a third stage is also added to the method to minimize the junction temperature.

8.3.1 Stage 1

Similar to the previously introduced simplified techniques, the first stage evaluates all 6 large vectors in the CF. However, the CF is simplified by eliminating the second

and third terms as written in (8.8):

$$CF = (i_{\alpha}^{*(k+2)} - i_{\alpha}^{p(k+2)})^2 + (i_{\beta}^{*(k+2)} - i_{\beta}^{p(k+2)})^2 \tag{8.8}$$

Therefore, no weighting factor and voltage prediction calculation is present in this CF. This decreases the calculation time of each step significantly.

8.3.2 Stage 2

Based on the outcome of the first step, a set of control actions is defined for evaluation in the cost function. However, instead of evaluating 11 adjacent vectors to the selected large vector, all the redundant vectors are eliminated. Therefore, two zero vectors and three small vectors are eliminated out of 11 adjacent vectors in the second stage, and the control actions set consists of only 6 vectors. These 6 vectors are then applied to the CF in (8.8) and the final minimum CF determines the vector to be applied to the inverter in the next time instant.

The process of selecting 6 vectors out of the 11 adjacent vectors is explained here. Since the two terms with the weighting factors are eliminated from the CF, the selection process must include those terms. Hence, a maximum boundary for NPV deviation is defined by $\Delta V_{c,max}$.

Switching events' minimization

As long as $|\Delta V_c| < |\Delta V_{c,max}|$ the selection criteria for the control actions set is the minimum switching transitions in each sampling event. For this purpose, a new parameter is defined as follows in (8.9):

Table 8.1: Candidate vectors for (k+1) based on the S_{avg}^{k}

$S_{avg}^{(k)}$	-1	$\frac{-2}{3}$	$\frac{-1}{3}$	0	$\frac{+1}{3}$	$\frac{+2}{3}$	+1
$S_0^{(k+1)}$	S_{0N}		S_{0O}			S_{0P}	
$S_{S1}^{(k+1)}$	S_{S1N}			$S_{S1N/P}$	S_{S1P}		
$S_{S2}^{(k+1)}$	S_{S2N}			$S_{S2N/P}$	S_{S2P}		
$S_{S3}^{(k+1)}$	S_{S3N}			$S_{S3N/P}$	S_{S3P}		
$S_{M1}^{(k+1)}$	S_{M1}						
$S_{M2}^{(k+1)}$	S_{M2}						

$$S_{avg} = \frac{S_a + S_b + S_c}{3} \tag{8.9}$$

Out of all feasible small vectors in A_{S1}, only the ones will be added to the control actions set that possess a similar S_{avg} sign to the S_{avg}^{k}. A similar decision making approach is taken for the redundant zero vectors. Table 8.1 summarizes this approach.

NPV balancing

As soon as $|\Delta V_c| > |\Delta V_{c,max}|$ the control actions set will be selected with the purpose of reducing NPV deviation. Therefore, the set of candidate vectors for the second stage CF evaluations is selected based on the requirement for compensating the voltage deviation.

At each switching state, the neutral-point current can be calculated using (8.4). Therefore, the decision for small vector selection can be made based on the signs

Table 8.2: Candidate vectors for (k+1) based on the the sign of ΔV and the sign of the phase currents

	$(\Delta V_c * i_a) > 0$	$(\Delta V_c * i_a) < 0$	$(\Delta V_c * i_b) > 0$	$(\Delta V_c * i_b) < 0$	$(\Delta V_c * i_c) > 0$	$(\Delta V_c * i_c) < 0$
S_{s1}	S_{s1P}	S_{s1N}	X		X	
S_{s2}	X		X		S_{s2N}	S_{s2P}
S_{s3}	X		S_{s3P}	S_{s3N}	X	
S_{s4}	S_{s4N}	S_{s4P}	X		X	
S_{s5}	X		X		S_{s5P}	S_{s5N}
S_{s6}	X		S_{s6N}	S_{s6P}	X	

of the currents and voltage deviation. Table. 8.2 summarizes the selection of the candidate small vectors for evaluation in stage 2.

Stage 3

After deriving the optimum vector to be applied to the inverter in the next time step, the transition method will be determined based on the previously discussed choices in Chapter 7, for different "O" modes in each leg to minimize the maximum junction temperature. The CF in Stage 3, $CF3$, is written as (8.10):

$$CF3 = max(T_{j,a}) + max(T_{j,b}) + max(T_{j,c}) \tag{8.10}$$

where $max(T_{j,x}) = max(T_{j,\ for\ switches\ in\ phase\ "x"})$.

The transition that yields the minimum value for $CF3$ is selected to switch from current switching state, $S^{(k)}$ to the next switching state, $S^{(k+1)}$. Another point to be noted is that $CF3$ is composed from three terms which are independent of each other. In other words,

the switching transition in phase "a", only affects the first term $max(T_{j,a})$ and so on for phases "b" and "c".

8.4 Simulation Results

In this section, the performance of the proposed reduced control set MPC technique is simulated in MATLAB/Simulink and compared to the previously developed methods in the literature. Also, the two-level control of the inverter, in which only the large vectors are applied to the three-level inverter, is considered in the comparison. The simulations have been performed with two assumptions. First, like many previous studies, it is assumed that the controller is capable of performing all techniques with an equal sampling time.

However, the controller's limited computation speed weakens the validity of the results. Hence, a second assumption has been made in which an equal computational burden is considered for different methods. In this approach, the control method with fewer control set elements takes advantage of a smaller calculation time at each sample which ends up in higher switching frequency. The maximum processing capability of the selected microcontroller, TMS320F28379d is utilized for each of the MPC techniques.

8.4.1 Equal Sampling Times

First, a fixed sampling time of 52 μs is considered for all approaches. Based on the experimental implementation, which will be presented later, this time period is large enough for all techniques to evaluate all elements of their corresponding control set in the CF. The specifications of the simulated system are listed in Table 8.3. The steady-state operation of two-level MPC control, conventional three-level control, simplified control based on [221], and the proposed technique are depicted in Fig. 8.4. The comparison of voltage and current

Table 8.3: The specifications of the simulated system

Parameter	Value
Input Voltage (V)	200
Output peak current (A)	20
Load R (Ω)	2
Load L (mH)	2.5

Table 8.4: Comparison of different MPC techniques with the proposed method using equal sampling frequency

Parameter	Two-Level	Conventional	Simplified	Proposed
Control set size	7	27	17	12
Current THD	4.8	2.5	2.5	2.6
Voltage THD	87.6	41.1	41.1	44.5
V_c max deviation	1.5	10	10	19

THD values in the four mentioned approaches is summarized in Table. 8.4. In terms of voltage THD, it can be seen that the two-level approach has the highest value by 87.6%. The conventional, simplified, and the proposed method have voltage THD values of 41.1%, 41,1%, and 44,5%, respectively. With regard to the current THD, the two-level approach, conventional, simplified, and the proposed method have current THD values of 4.8%, 2.5%, 2.5%, and 2.6% respectively.

With regards to the voltage deviation of each capacitor from the $\frac{V_{dc}}{2}$, the two level technique has the best performance in which no unbalance occur in the capacitor voltages. The 1.5 V imbalance shown in Fig. 8.4 and Table. 8.4 happens due the stray inductance in the dc voltage source to capacitor path which is included in the simulations. The conventional three-level MPC, the simplified and the proposed techniques have the maximum voltage deviations of 10, 10, and 19 V respectively.

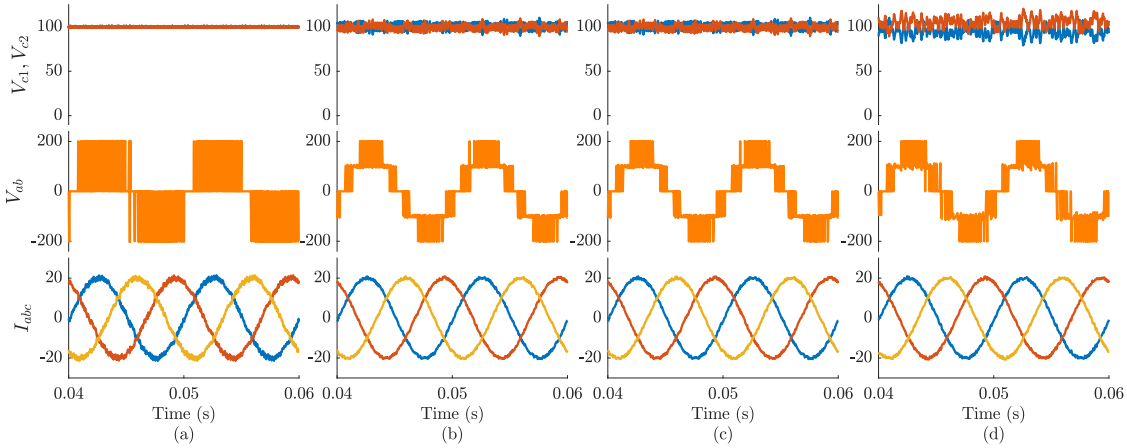


Figure 8.4: Simulation results with equal sampling time of 52 μs for a) two-level MPC, b) conventional three-level MPC, c) simplified three-level MPC, and d) proposed MPC

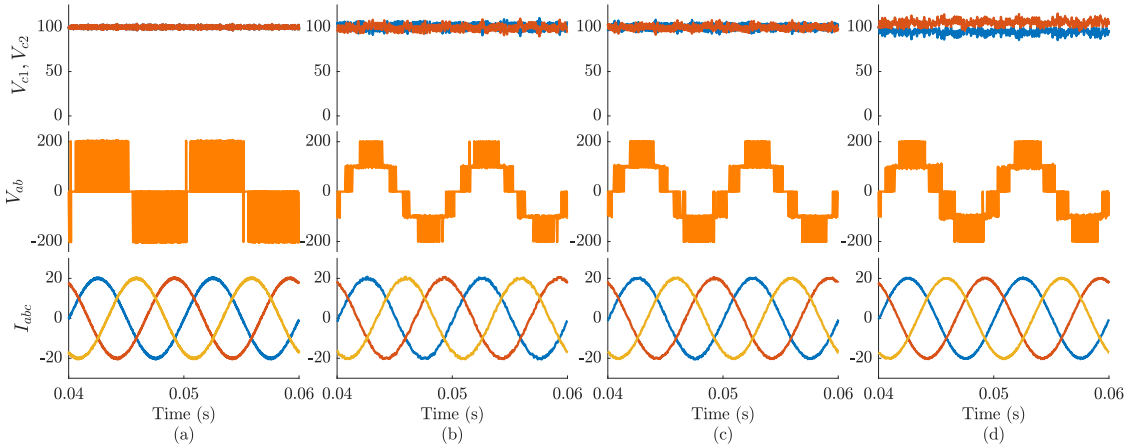


Figure 8.5: Simulation results with equal computational burden for a) two-level MPC with $F_s = 55000$, b) Conventional three-level MPC with $F_s = 19000$, c) simplified three-level MPC with $F_s = 24000$, and d) proposed MPC with $F_s = 35000$

8.4.2 Equal Computational Burden

As anticipated, with equal sampling times, the conventional three-level approach with 27 elements in its control set had the lowest THD while the two-level control approach had the largest current distortion. However, the results differ in real time owing to unequal minimum

Table 8.5: Comparison of different MPC techniques with the proposed method with equal computational burden on the microcontroller

Parameter	Two-Level	Conventional	Simplified	Proposed
Control set size	7	27	17	12
Sampling time	18 μs	52 μs	41 μs	28 μs
Sampling frequency	55000	19000	24000	35000
Weighting factor	No	Yes	Yes	No
Current THD	1.7	2.5	2.0	1.4
Voltage THD	88.2	41.1	42.2	44.2
V_c max deviation	3	10	9	14

sampling time for each method. While each sampling period of the conventional three-level method requires 52 us, this value can be as low as 18 μs for the two-level approach. Also, the simplified and the proposed techniques require 41 μs and 28 μs to evaluate all control actions respectively. Fig. 8.5 depicts the steady-state operation of all the MPC techniques with the maximum capability of the selected microcontroller. Table. 8.5 presents a summary of the major comparison criteria in this regards. In can be seen that in terms of the current THD value, the proposed technique outperforms all other solutions with a THD as low as 1.4%. On the other hand, the conventional three-level MPC technique and the simplified technique in [221] demonstrate THD values higher than the two-level MPC technique, where only large vectors are evaluated. In other words, due to the large number of vectors and added complexity of capacitor voltage predictions, the three-level inverter with MPC control can not outperform two-level structure unless the proposed simplified, weighting factor-free method is used.

8.5 Experimental Results

The obtained outcomes from MATLAB simulations are further examined in this section by implementing the control methods on a three-level ANPC inverter. The main features of the experimental setup used for these tests can be seen in Table. 8.6. The microprocessor has a key role in the operation of the MPC technique due to the large computational burden. The selected microprocessor, TMS320F28379D, takes advantage of dual cores and one independent control law accelerator (CLA) for each of the cores. In order to exploit the maximum speed for MPC calculations, one CLA module is dedicated to vector evaluations, while the gate pin assignments, peripherals, and protection functions are dedicated to the two cores. Also, the second CLA module is responsible for ADC readings and filtering.

A CPU interrupt controls the trigger for running MPC evaluations. The maximum allowed interrupt frequency can be calculated based on the maximum required time for each MPC technique. With this method, the minimum sampling time/maximum sampling frequency is achieved as previously summarized in Table. 8.5 for each technique.

In this section, the experimental results are presented for the proposed technique and a comparison is also made between the proposed method and the technique in [221] in terms of voltage imbalance and current THD. Furthermore, the operation of the proposed control with two different power factors, as well as the transient response to a step change in the reference current is explored.

8.5.1 Steady-State Studies

Fig.8.7 demonstrates the steady-state operation of the method proposed in [221] as well as the method proposed in this thesis. It is clear that a DC voltage imbalance is present in the proposed method as a consequence of eliminating the voltage balancing weighting factor. The proposed technique has a maximum voltage deviation of 14 V, while the method in

Table 8.6: The specifications of the experimental setup

Parameter	Value
Input Voltage (V)	200
Switch	UJ4C075018K4S
Microcontroller	TMS320F28379D
V_c sensors	ISO224
I_o sensors	HTFS 200-P

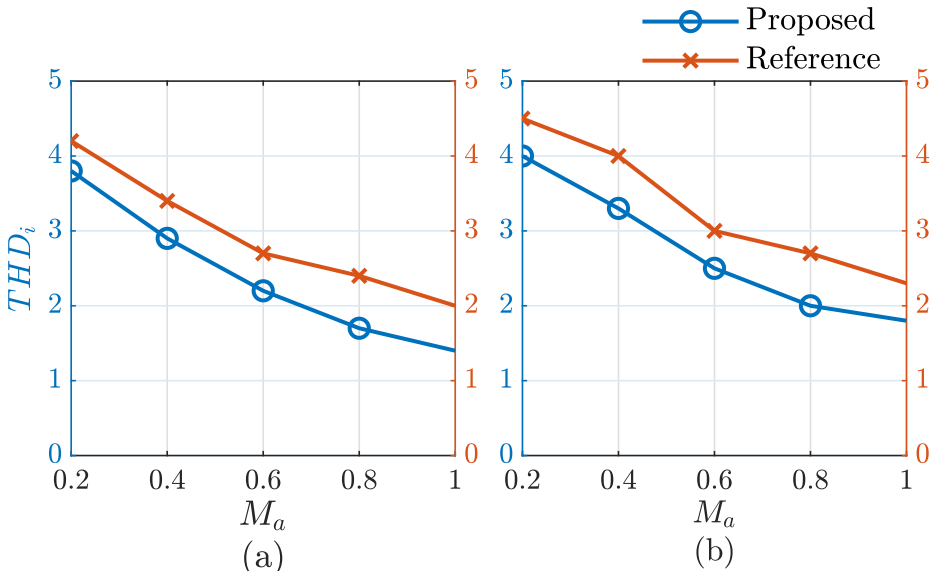


Figure 8.6: Current THD comparison in simulation and experiment results versus modulation index, M_a for a) output frequency of 50 Hz, and b) output frequency of 250 Hz

[221] showed a maximum voltage deviation of 10 V. However, the proposed method has the benefit of lowering THD from 2.0% to 1.4% owing to 46% higher sampling frequency. The higher sampling frequency is also beneficial to the passive components such as DC-link capacitors as well as output filters, if present. Fig. 8.6 depicts the changes in output current THD versus variations of M_a from 0.2 to 1 in two frequencies of 50 Hz and 250 Hz.

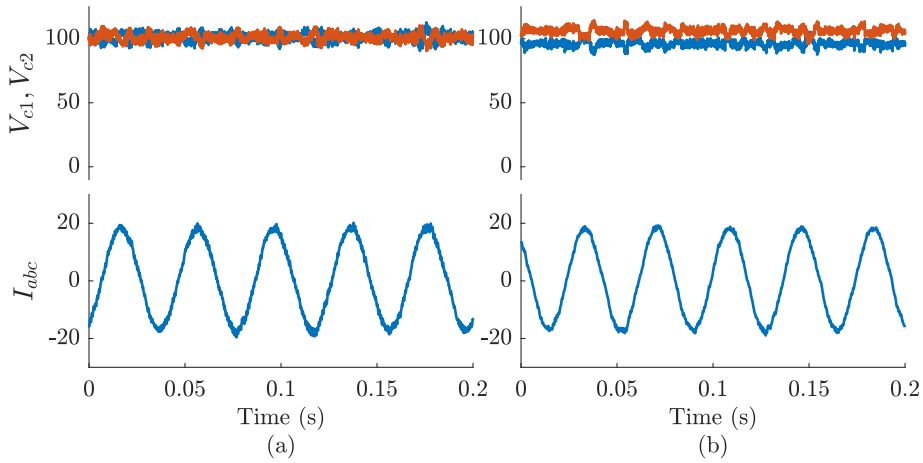


Figure 8.7: Experimental results with maximum computational burden with a) simplified three-level MPC with $F_s = 24000$, and b) proposed MPC with $F_s = 35000$

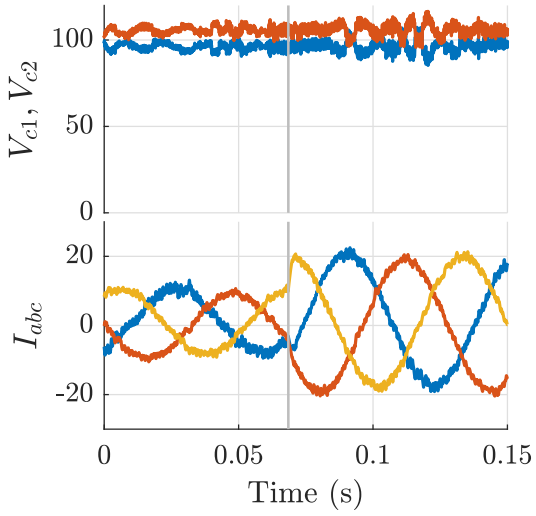


Figure 8.8: Experimental results with the proposed MPC technique with a step change in the reference current from 5 A to 10 A by changing the M_a from 0.5 to 1

8.5.2 Transient Studies

In Fig. 8.8 the result of applying a current reference change from 5 A to 10 A is shown. As a result of the reference change, the output current has settled in its new value in about

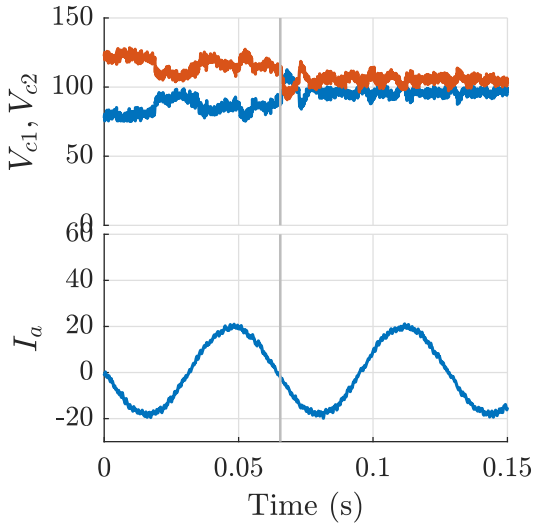


Figure 8.9: Experimental results with the proposed MPC technique; The hysteresis voltage balancing is activated at $t = 0.07$

1.5 ms. More importantly, no overshoot in the current waveform and capacitor voltage deviation is detected. However, the maximum voltage deviation has increased from 11 V to 14 V as a result of the increased current.

In a second transient test, the hysteresis voltage balancing method is tested. In Fig. 8.9, the capacitor voltages and phase a current are shown. At $t = 0.07s$, the hysteresis voltage balancing is activated. The voltage deviation falls to below 14 V in about 1 ms.

8.6 Summary

Model-predictive control (MPC) offers interesting characteristics for power electronic inverters in applications with fast response requirements. However, high computational burden of the control algorithm prevents its usage in high-frequency applications.

In this chapter, a method was introduced to first, simplify the cost function and eliminate the weighting factors, and second, minimize the required time for calculations. While the

implemented system requires 52 μs to evaluate all control actions in each switching period for the conventional MPC, the proposed method reduces this time to 28 μs by eliminating 15 out of the original 27 vectors from the evaluations. Simulation and experimental results in both steady-state and transient conditions were presented.

Chapter 9

Conclusions and Future Work

9.1 Conclusions

This thesis presented an evaluation of three-level ANPC inverter for EV application and innovative control methods for its power density improvement. Multilevel inverters have been the focus of many research studies is the past decades and with the recent trends in EVs powertrain, they have gained more interest in this particular application. The DC-link voltage in EVs has increased mostly for enabling fast charging, reducing power loss, and increasing the power density of the powertrain. However, a reliable solution is needed for the high-voltage inverter in the powertrain. The high voltage DC-link places multilevel structures as an interesting solution.

Multilevel structures have proven to be a suitable substitute for their well-known two-level counterpart. The ability to use low-voltage fast semiconductors, lower $\frac{dv}{dt}$ and $\frac{di}{dt}$ magnitude, high power density and efficiency, and high-quality output waveforms are the major advantages of these structures. The wide variety of multilevel structures offer different structures, suitable for different specific applications. Based on the results of the comparative review in this thesis, in EV applications, active neutral point clamped (ANPC) and

cascaded H-bridge (CHB) structures offer best specifications. However, the CHB topology needs a restructure in the battery pack and battery management system due to a need to isolated input sources. Hence, a three-level ANPC inverter was selected in this thesis for further investigations.

Similar to the topology selection, choosing the best control and modulation technique for multilevel topologies requires a comprehensive review of the requirements in the EV drive. Some selection criteria, such as fast dynamic response, is similar to the requirements for the two-level inverter. However, some requirements are exclusive to multilevel topologies. Voltage balancing control among different levels is a major requirement in most multilevel structures. Another issue which arises in multilevel inverters is the need to control the losses in different switches since it is not inherently equal like two-level inverters. One more concern regarding the control and modulation schemes is the large complexity and computational burden for multilevel inverters due to the larger number of available states in each leg. Therefore, several control techniques such as model predictive control (MPC) require some simplifications for being used in this application.

After the review of topologies and control systems, a three-level ANPC inverter is selected in this thesis for implementation. As mentioned, the unequal junction temperature in multilevel structures is a drawback in these topologies which inhibits achieving higher power densities. In this thesis, an electro-thermal model based on foster equivalent network was extracted for the inverter which enables online junction temperature estimation of the switches at each time instant. Based on this estimation, a modified SPWM technique was proposed which ensures that loss is distributed in a way to minimize the maximum junction temperature in the inverter. With the proposed method, the power density of the inverter increased by 12 % in experiment, while a protection algorithm is also added to the inverter by limiting the maximum junction temperature in the inverter.

The large computational burden of the FCS-MPC technique for the three-level ANPC

structure is a major drawback that limits the average switching frequency. The number of available vectors is increased to 27 which is more than three times larger than the conventional two-level structure. While several previous studies have managed to reduce the number of calculations as low as 12, this thesis introduced a method to choose the candidate vectors prior to cost function evaluations. This method takes advantage of eliminating the weighting factors and reduction of computational burden by half. This method has been tested on the experiment setup and compared to the conventional methods in terms of voltage balancing, THD, and computation time. Moreover, simulations have been performed with the previously introduced electro-thermal model for junction temperature minimization.

9.2 Future Work

Several suggestions are made in here for the future research studies:

- One major limiting factor for power density in the proposed design is the use of discrete devices. Currently, the number of available three-level SiC-based power modules on the market are very limited. Half bridge power modules can be used for three-level ANPC structure. However, 9 modules are required which, again, decreases the power density. Hence, for pushing the power density towards higher values, there is a need for power dense, compact power modules designed based on EV standards.

- The switch used in this thesis is SiC-based FET which is one of the interesting WBG options. However, GaN switches also introduce some exceptional characteristics for thermal management system of the inverter. One major limiting factor in development of GaN-based inverters is the lower breakdown voltage of them which make them unsuitable for applications with 400 V- 800 V DC-link voltage. However, as

mentioned in this thesis, multilevel inverter structures offer the voltage stress division in higher number of levels. Therefore, multilevel structure with higher number of levels can be a suitable choice for GaN-based inverters. However, the large number of discrete switches and gate driver circuits is a discouraging factor in power density improvement.

- Other conventional and advanced multilevel topologies have interesting features that worth further investigation and experimental implementation. The modular structures, for example, offer a noticeable advantage due to higher reliability and fault-tolerance.

- While the junction minimization algorithm was proposed in this thesis using SPWM technique, space vector modulation (SVM) is considered the most popular modulation technique for many high-performance applications. Therefore, using the proposed electro-thermal model, SVM technique can be used to offer an algorithm for minimizing the junction temperature and improving the power density.

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