High-Efficiency Power Electronic Converters for EV Fast-Charging Stations with Energy Storage

by

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Abstract

Electric vehicle (EV) adoption continues to rise, yet EV sales still represent a small portion of vehicle sales in most countries. An expansion of the DC fast charging (DCFC) network is likely to accelerate this revolution towards sustainable transportation, giving drivers more flexible options for charging on longer trips. However, DCFC presents a large load on the grid which can lead to costly grid reinforcements and high monthly operating costs – adding energy storage to the DCFC station can help mitigate these challenges.

This thesis first performs a comprehensive review of DCFC stations with energy storage, including motivation, architectures, power electronic converters, and a detailed simulation analysis for various charging scenarios. The review is closely tied to current state-of-the-art technologies and covers both academic research contributions and real energy storage projects in operation around the world. It is identified that the battery energy storage systems (BESSs) with active front end converter provides high efficiency with reasonable power density in a DCFC station. It is also realized that the isolated DC/DC converter interfacing BESS and EV determines the overall efficiency of a DCFC station with low grid connection.

Secondly, this thesis analyzes the impact of active front end based DCFC stations connected to a grid distorted with background voltage harmonics. In active front end based DCFC stations, background voltage harmonics produce current not only at the frequencies of the distorted voltage, but also at other coupled frequencies. Various mitigation techniques, such as increasing inner control loop gain, grid voltage feedforward, and selective harmonic compensation, have been adopted in industry to reduce the emissions originating from distorted background voltage. However, although these techniques are effective in suppressing the current at the harmonic orders present in the background voltage, they deteriorate the emission at coupled frequencies. This thesis

provides the theoretical explanation of this phenomenon, which is verified by simulation of a two-level active front end in PSCAD/EMTDC. This thesis also discusses the proper treatment of current emission due to background voltage harmonics.

Thirdly, the thesis identifies the semi dual active bridge (semi-DAB) converter as an ideal candidate as the interfacing isolated DC/DC converter between the BESS and the BEV. A novel control strategy is proposed for the semi-DAB converter to achieve wide voltage gain while increasing the efficiency at operational points with high input voltage and low output voltage, which is a commonly occurring scenario when the BESS is fully charged, and the EV battery is at low charge. Furthermore, this thesis also provides an algorithm to determine the required phase-shift in real time for any operating point, eliminating the need to devise the control trajectory offline. A 550 V, 10 kW experimental prototype is built and tested to validate the proposed control strategy. With a 25 A constant charging current, the prototype shows the proposed control strategy can improve efficiency by up to 3.5% compared to the well-known dual phase shift control at operating points with high input voltage (450 – 550 V) and low output voltage (150 – 275 V), with a peak efficiency of 97.6%.

Finally, this thesis proposes a novel variable turns-ratio semi-DAB converter to improve its overall efficiency even further when the input voltage is high and output voltage is low. Furthermore, a control law is also proposed to determine the turns-ratio, i.e., the operational structure of the converter, which reduces the converter peak and rms current. The 550 V, 10 kW prototype is modified to accommodate the variable turns-ratio high frequency transformer to test the proposed converter and control. The proposed converter with control can further improve the efficiency at many operating points compared to single turns-ratio semi-DAB with DPS control. The peak efficiency achieved is 98.5%.

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Chapter 1

Introduction

1.1. Background and Motivations

Electric vehicles (EVs) have the potential to significantly reduce greenhouse gas emissions, regulated emissions which cause local air pollution and negative health effects [1], and society's reliance on fossil fuels. Global EV sales, which include battery electric vehicles (BEVs) and plug-in hybrid electric vehicles (PHEVs), increased by 46% from the first half of 2018 to the first half of 2019, with 1.134 million EVs delivered globally in the first half of 2019 [2]. However, global EV light vehicle market share was only 2.5% for the first half of 2019 [2]. Thus, while the transition to sustainable personal transportation is accelerating, there is still much improvement needed.

The main barriers to EV adoption are high vehicle costs, range concerns, and charging infrastructure. Though range can be improved with larger and more energy-dense batteries, there is a limit to what can reasonably be achieved due to the associated increases in vehicle mass and cost-specifically, the battery can account for up to 50% of the total BEV cost [3]. The installation of comprehensive EV fast charging networks would help alleviate range and charging concerns on longer inter-city drives without requiring very costly EVs with large batteries. Though typical home chargers of AC Level 1 or Level 2 are well-suited for overnight charging for typical inner-city driving, the need for recharging away from home on days with longer driving can cause inconvenience and uncertainty for drivers. A survey among 500 Nissan customers verifies this claim: 56% of customers placed high importance on fast charging, and 62% stated that the availability of charging infrastructure was their primary concern regarding BEVs [4]. To help alleviate some of these concerns, most manufacturers offer BEVs capable of fast charging, as shown in Table 1-1 [5], with the top charging power being 150 kW for the Audi e-Tron and Tesla Model 3. Though these vehicles use 400 V battery systems, Aston Martin and Porsche are

developing BEVs with 800 V batteries to make even higher charging rates possible, due to reduced currents and losses in the charging cables [6], [7]. Therefore, various DC fast charging standards are emerging to serve this critical need for faster EV charging. Table 1-2 shows a comparison of AC home chargers and different DC fast charging options [8], assuming typical vehicle energy consumption is 177 Wh/km or 265 Wh/mile and charger efficiency is 100%. The results show that the higher charging rate options allow long-distance driving with only minimal driving interruptions for charging.

Table 1-1: Top Charging Power of Currently Available EVs [5]

EV Make and Model	Top Charging Power (kW)	Charging Speed Drops Above SOC (%)
Audi e-tron	150	80
Tesla Model 3	150	-
Mercedes-Benz EQC	110	40
Jaguar I-PACE	100	40
Hyundai Kona	77	58
Kia e-Niro	77	58
Hyundai Ioniq	70	75
BWM i3	50	85
Nissan Leaf	50	60
VW e-Golf	40	80

Table 1-2: Summary of Charging Standards [8]

	AC On-board Charging		DC Off-board Charging		
	Level 1 (120V,1.4kW)	Level 2 (240V,7.2kW)	Fast Charging (480V, 50kW)	Tesla Supercharger (480V, 140kW)	Ultrafast Charging (up to 800V, 400kW)
Typical range gained per minute of charge (km)	0.13	0.68	4.70	13.15	37.50
Time to charge for 200 km (minutes)	1332	260	37	13	4.7

However, fast and ultrafast charging directly from the grid poses a large and unpredictable load on the electric system [9]–[11] and in rural areas with weak grid connections, (ultra)fast charging directly from the grid is not even possible [12]. Since much of the need for (ultra)fast chargers is on long drives, possibly outside of cities, these charging stations should ideally be

located along highways between cities. The electrical infrastructure along some of these highways is usually far from the main distribution grid, and thus it has high impedance with low short circuit power. Moreover, only a single-phase 120 V or 240 V AC supply may be available at some rural locations along these highways. Therefore, the installation of fast charging stations is not possible at such locations without upgrading the electrical service, which usually results in high installation cost [13]. Energy storage system (ESS) can mitigate the necessity of such high cost of service upgrading by acting as buffer in between the grid and the vehicle.

Furthermore, an ESS is also often advantageous in fast charging stations with strong grid connections, as it prevents overloading the grid during charging [14]. Expensive grid reinforcement can be required with multiple fast charging ports at strong grid locations, but the use of ESSs can avoid or partially mitigate these infrastructure costs. An ESS will also help reduce the utility demand charges incurred due to fast charging and it is estimated that a charging station with six 350 kW chargers can save around $157,000 annually by using a battery storage system [15]. Further, the vision of sustainable mobility will not be fulfilled until EVs are charged with renewable energy sources such as solar and wind. ESSs can store the energy generated from these intermittent renewable sources in order to charge EVs when needed. The above-mentioned points have further been discussed below in detail.

1.1.1 Reinforcement of Grid Infrastructure

DC fast charging (DCFC) stations, especially those providing charging power over 100 kW, can require high initial investment for grid reinforcement. For instance, a 350 kW charger will require a considerably more expensive utility upgrade compared to a 50 kW charger in case of a weak grid connection [16]. Moreover, it is not always possible to be directly connected to a strong grid, for instance, along the highway and countryside roads – though these locations may be where

DCFC stations are needed the most, i.e., between cities. Furthermore, according to California Public Utilities Commissions' studies, as the fast charging network expands, the distribution lines and transformers will require more upgrades than power plants, transmission lines, and substations. For instance, a typical Electrify America highway charging station with two 350 kW and four 150 kW chargers will introduce an additional 1.2 MW power demand and will need an upgraded or additional costly distribution transformer [14]. In Norway, it is estimated that $1.6 billion will be required for grid reinforcement to accommodate the uncontrolled charging behavior of the large numbers of EVs expected on the road by 2040 [17].

Although smart-charging strategies have been proposed in [18]–[22] to garner more control over EV charging for grid benefit, they are best applied to overnight home charging where there is ample time to shift individual vehicle charging times while still providing a full charge by the following morning. In contrast, drivers requiring fast charging generally need high power charging immediately upon vehicle plug-in. A better solution for DCFC stations is to use an ESS so that the power required from the grid may be low enough to minimize or even negate the need for grid reinforcement. The ESS can be charged when the electricity demand and price is low, and EVs can be charged with higher power from the ESS without creating a burden on the grid and at a predefined flat rate. In a grid with lower grid capacity, such as those in remote areas, it can be less costly and less complex to deploy an ESS-based charging station rather than reinforcing the grid infrastructure [23].

1.1.2 Operational Cost of DCFC Stations

The high power draw of DCFC stations generates high demand charges, which can make investment in and operation of DCFC stations unappealing to investors. The utility charges demand charges based on the highest monthly peak power drawn per non-residential customer,

including charging stations, in order to recoup the fixed costs for generation, transmission, and distribution. In the U.S., demand charges can range from $2/kW to $90/kW [24]. For example, a DCFC station may have three 50 kW charging ports, a fixed energy price of $0.10/kW, a fixed monthly connection charge of $140 [10], and a monthly demand charge of $35/kW. If it is assumed that three EVs charge at the station per day, and each EV charges at 50 kW for 20 minutes (using 17 kWh of energy), then three scenarios are possible: one, two, or three EVs are charging at one time. These scenarios correspond to the monthly demand charges of $1750, $3500, and $5250, respectively.

An ESS can help reduce the monthly cost incurred due to demand charges. A battery energy storage system (BESS) can be installed such that all the energy required for charging three EVs simultaneously at the station is supplied from the BESS. In this particular example, the BESS would be characterized as high power density (capable of supplying power at a 3-C rate) and the efficiency of the BESS (from battery to EV) can be estimated at 90%. Thus, the capacity of the BESS should be around 56 kWh. If only three EVs per day are charged at the station, the BESS can be charged using a single phase 3.3 kW charger connected to the grid. Thus, the peak power requirement from the grid to the charging station would be 3.3 kW, resulting in a monthly demand charge of only $115.50.

To achieve this monthly savings, the additional cost of the BESS must be considered. The initial cost of the BESS includes power electronic converters and the battery itself. For a DCFC station without energy storage, high power AC/DC and DC/DC converters are required (as discussed in Chapter 2). For a DCFC station with energy storage, a low power AC/DC converter and a high power DC/DC converter will suffice since the AC connection will be rated for lower power. Thus, the costs of the power electronic converters between the two DCFC station types can

be considered approximately equivalent, and likely lower for the DCFC station with energy storage. Thus, in this example, only the additional cost of the battery itself will be considered. If the battery cost is estimated at $390/kWh [25], then the initial capital cost for the battery is $21,840. This capital cost of the battery will be paid back within 4 to 14 months depending on the monthly demand charges as shown in Figure. 1-1. After payback, the monthly operating cost for the charging station will include only the demand charge of $115.50, and fixed and used energy costs.

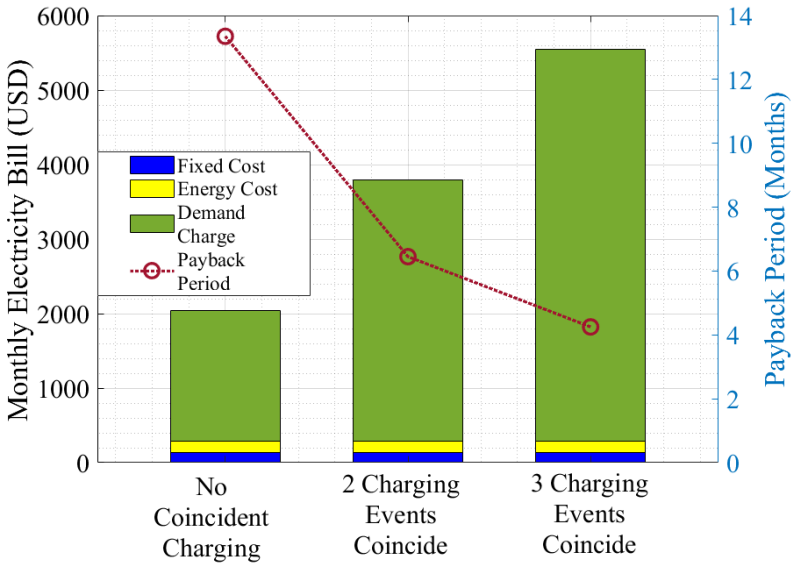


Figure 1-1. Monthly operating cost of a DCFC with different charging scenarios and payback period of the capital investment on energy storage

1.1.3 Use of Renewable Energy Sources and Services to the Grid

EVs have the potential to create a sustainable transportation system with high efficiency and greatly reduce emissions – however, this goal can only be achieved if the electricity used to charge EVs is generated from renewable sources such as solar and wind. A major challenge in achieving this goal is to match the charging demand with electricity generation from unpredictable and/or intermittent renewable sources. However, an ESS can be used as an intermediate energy buffer from the renewable generation to the somewhat unpredictable EV charging needs.

Reference [26] provides a comprehensive review of the function of ESSs at different stages within power systems with a high penetration of renewable energy sources. An ESS can help reduce voltage and frequency instability and help peak shaving by storing energy from large-scale photovoltaic (PV) plants [27]–[29]. One of the world's largest battery storage projects of 60 MWh has been implemented to integrate solar energy into the grid in Hokkaido, Japan [30]. Similar projects are also initiated for more efficient integration of wind energy. For instance, a 24 MWh BESS was integrated into a 156.6 MW wind farm in west Texas for storing power during off-peaks hours [31]. Another similar but larger 32 MWh lithium-ion BESS was installed in southern California to provided voltage support and frequency regulation near a 4500 MW wind farm [32]. Different Power to Gas (P2G) projects have been initiated to produce hydrogen with excess renewable energy. For instance, a 2 MW P2G installation has been established by E.ON, a German utility company in partnership with Swissgas and Hydrogenics in Falkenhagen, Germany [33]. A comprehensive list of other renewable power to hydrogen gas projects in Australia, Canada, China, Germany, Japan, Netherlands and the U.S. can be found in [34]. Moreover, various ESSs are being used to provide peak-shaving, frequency regulation, and improve the power quality and reliability of the electrical grid. For instance, a 24 MWh and a 14 MWh sodium-sulfur BESS from PG&E were installed in East San Jose and Vacaville, California, [35] to improve power quality and reliability of the grid. A 5 MWh/20 MW flywheel storage system was installed by Beacon Power in Hazel Township, Pennsylvania to provide frequency regulation [36].

As discussed previously, adding energy storage to DCFC stations can reduce the initial investment required (through smaller or no grid reinforcements) and can reduce the operational costs (through a reduction in monthly demand charges). The real-world installation examples above show that stationary grid energy storage can be beneficial for providing services to the grid

without even considering its use in DCFC stations – the combination of using ESSs to provide grid services with DCFC operation provides even better financial incentive to invest in and operate DCFC stations. Therefore, the ESS can act as a virtual power plant coupled with solid-state electronics interfaces [37], playing a significant role as DCFC stations and renewable energy sources become widespread.

1.2. Contributions

This thesis first provides a comprehensive review of different architectures and related power electronics in a DCFC station with three different ESS, namely Battery, Flywheel, and Hydrogen. Only common DC bus architectures are considered due to the DC nature of the load; therefore, it results in lower number of conversion stages. This thesis then provides a comprehensive analysis of efficiency, cost, and volume of DCFC stations with these three energy storage systems. This analysis is then used to identify the energy storage option and related DCFC architecture with high efficiency, low cost, and high energy and power density.

Secondly, this thesis analyzes the impact of an active front end converter based DCFC connected to a low voltage weak grid with background harmonics in terms of current emissions at coupled frequencies. It is identified that the background voltage harmonics can propagate through the phase locked loop (PLL) during reference frame transformation. Moreover, a recommendation is also provided for the treatment of current emission of coupled frequencies based on this analysis.

Thirdly, this thesis identifies the semi Dual Active Bridge (semi-DAB) converter as a suitable candidate for the isolated DC/DC converter interfacing the energy storage system and the BEV. Therefore, the reminder of the thesis tries to improve the operational efficiency of this isolated DC/DC converter with optimal control and with novel multi-winding arrangements. A novel control strategy is proposed to reduce the peak and rms current in the system. This ensures

the converter operates with high efficiency compared to the advanced dual-phase shift control, especially when the input voltage is high and output voltage is low. A 550 V, 10 kW prototype has been developed to test the proposed control.

Finally, the efficiency of the semi-DAB converter has further been improved using a variable turns-ratio multi-winding structure. The converter can operate withing reasonable voltage gain requirements even when input and output voltage vary over a wide range by adjusting the turns-ratio of the converter. The current stress and losses of the proposed converter are compared with the traditional semi-DAB and DAB converter.

1.3. Publications Related to Thesis Research

[1] M.A.H. Rafi, Y. Sun and J. Bauman, "Impact of Background Voltage Harmonic Mitigation Techniques on Coupled Frequencies in VSC-Based EV Fast Charging," *2019 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2019, pp. 1-6, doi: 10.1109/ITEC.2019.8790520.

[2]* M. A. H. Rafi and J. Bauman, "A Comprehensive Review of DC Fast-Charging Stations with Energy Storage: Architectures, Power Converters, and Analysis," in *IEEE Transactions on Transportation Electrification*, vol. 7, no. 2, pp. 345-368, June 2021, doi: 10.1109/TTE.2020.3015743.

[3] M. A. H. Rafi and J. Bauman, "Optimal Control of Semi-Dual Active Bridge DC/DC Converter with Wide Voltage Gain in a Fast-Charging Station with Battery Energy Storage," *IEEE Trans. Transp. Electrification.*, Early Access, Apr. 2022.

[4] M. A. H. Rafi and J. Bauman, "High-Efficiency Variable Turns-ratio Semi-Dual Active Bridge Converter for a Fast-Charging Station with Energy Storage," *Submitted to IEEE Trans. Transp. Electrification,* July 2022

* 2nd place prize paper award for 2022 in the IEEE Transactions on Transportation Electrification.

1.4. Other Publications

[1] M. A. H. Rafi, R. Rennie, J. Larsen and J. Bauman, "Investigation of Fast Charging and Battery Swapping Options for Electric Haul Trucks in Underground Mines," *2020 IEEE Transportation Electrification Conference & Expo (ITEC)*, 2020, pp. 1081-1087

1.5. Thesis Outline

This thesis is organized into seven chapters. Chapter 1 has introduced the background and motivation of having DC fast charging (DCFC) stations with energy storage systems. The main motivations are to reduce demand charge incurred during fast charging, minimize the required grid reinforcement to connect fast charging stations into the grid, and maximize the use of variable and intermittent renewable energy sources such as wind and solar.

Chapter 2 lays out different possible architectures and related power electronics converters in DCFC stations with three different energy storage systems, namely battery, flywheel, and hydrogen along with a hybrid energy system of battery and flywheel. The common DC bus architectures are mainly considered due to the DC nature of the load.

Chapter 3 performs a comprehensive analysis of the DCFC station architectures presented in Chapter 2 in terms of efficiency, volume, and cost for different fast charging ratings, grid connections, and charging event distributions. It is identified that the battery energy storage systems (BESS) with active front end converter provides high efficiency with reasonable power density in a DCFC station. It is also realized that the isolated DC/DC converter interfacing BESS and EV determines the overall efficiency of a DCFC station with low grid connection.

The impact of background voltage harmonics in an active front end based DCFC station is discussed in Chapter 4. It is identified that the background voltage harmonics can propagate through the phase locked loop (PLL) during reference frame transformation. Moreover, a recommendation is also provided for the treatment of current emission of coupled frequencies based on this analysis.

Chapter 5 identifies the semi dual active bridge (semi-DAB) converter as a suitable candidate interfacing BESS and EV. First, a novel control law is developed to improve the efficiency of this

converter in Chapter 5. This ensures the converter operates with high efficiency compared to the advanced dual-phase shift control, especially when the input voltage is high and output voltage is low. A 550 V, 10 kW prototype has been developed to test the proposed control.

Afterwards, the overall efficiency of this converter is further improved with the help of a novel muti-winding structure and control in Chapter 6. The converter can operate within reasonable voltage gain requirements even when input and output voltage vary over a wide range by adjusting the turns-ratio of the converter. The current stress and losses of the proposed converter are compared with the traditional semi-DAB and DAB converter. Finally, the Chapter 7 provides the summary and possible future work.

Chapter 2

Overview of Architectures and Related Power Electronics Converters

This chapter first discusses the most prominent energy storage technologies for use in DCFC stations found in the literature: batteries, flywheels, and hydrogen. Even though other technologies have also been investigated in the literature, such as superconducting magnetic energy storage (SMES) [38], [39], the high cost and low energy density of current SMES technology makes it infeasible for near-term implementation. Afterwards, different possible architectures of DCFC stations with these three ESSs and related power electronics converters used in these architectures have been discussed.

2.1 Different Storage Options

Electrochemical batteries have high efficiency, high energy density, and rapidly reducing costs. Lithium-ion technology is a top contender in these areas [40], and thus will be considered in this thesis. A typical BESS is shown in Figure. 2-1, including numerous battery packs, a battery management system (BMS), and a thermal management system. Lithium-ion based BESSs offer high efficiency in the range of 94% to 98% [41], depending on series and parallel cell connections and cell type. The calendar life often ranges from 10 to 15 years [42], but high cycling rates can lower actual lifetime, presenting replacement cost concerns. However, the use of second-life EV batteries can reduce the initial investment required but adds new challenges for integration. The power and energy density for different types of cells and arrangements are shown in Table 2-1, for Samsung SDI battery systems [43].

BESSs are currently used in numerous grid storage and DCFC station applications. EVgo, the largest fast charging network in the U.S., has BESSs at 11 of its DCFC stations across the U.S. [44]. Volkswagen's Electrify America has announced the use of Tesla Powerpack BESSs in their DCFC stations [45]. In addition, Tesla has introduced Supercharger V3 stations with PV and BESSs [46]. In terms of published research, [9] and [47] find that a BESS helps reduce the grid

impact of EV charging. Reference [48] presents a cost-benefit analysis of DCFC stations connected to the LV grid with BESS compared to MV grid connection, and finds that the short cycle life of batteries is a barrier to achieving higher cost-benefit due to the replacement cost of the batteries. However, the results show that BESSs provide better financial return compared to direct MV grid connection when the number of charging events is from 10 to 325 per day.

Table 2-1: Energy and Power Density of Different Battery Types [43]

	High Energy, Low Power		Medium Energy & Power		Low Energy, High Power	
	Module	Rack	Module	Rack	Module	Rack
Energy Density (kWh/m^3)	230	150	210	130	160	100
Power Density (kW/m^3)	120	80	210	130	480	300
Maximum Discharge Rate	0.5 C		1.0 C		3.0 C	

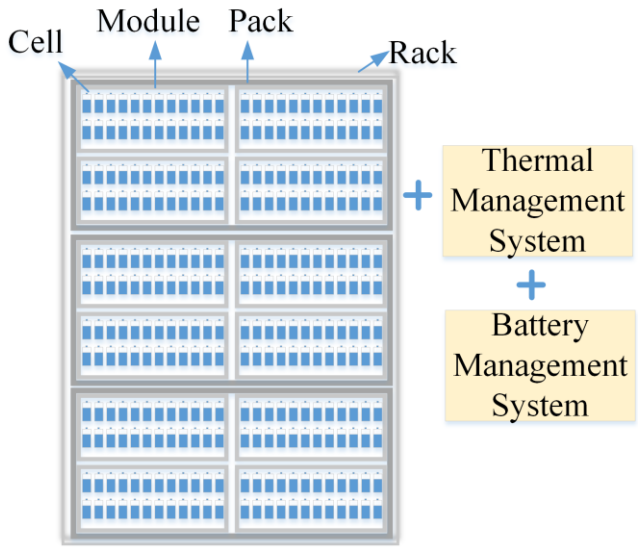


Figure 2-1. A general overview of the components in a BESS

Flywheels generally have higher power density and lower energy density than batteries, and consist of a spinning rotor, electric motor, bearings, a power electronics interface, and a vacuum housing [49], as shown in Figure. 2-2. The stored energy in the rotating rotor is proportional to the rotor's moment of inertia, I, and the square of the rotating speed, ω, as shown in (2.1). Since the

motor runs on AC power, power electronics are integrated into the flywheel system to generate the specific AC voltages needed to control the flywheel motor to store or release energy. If the flywheel is powered from DC voltage, then only a DC/AC converter is required within the flywheel system [50]. If the flywheel is powered from grid AC voltage, then an AC/DC and a DC/AC converter are required within the flywheel system [51]. Mechanical bearings contribute to high spinning losses, but the alternative lower-loss magnetic bearings [52] are generally too costly to be commercially feasible.

$$E = \frac{1}{2} I \omega^2 \tag{2.1}$$

The main advantages of FESSs are high cycle lifetimes and high power density. In general, flywheels can complete between 175,000 to 200,000 cycles over a 20 year life span [53]. Moreover, FESSs require less maintenance over their lifetime compared to BESSs [42]. However, the energy density of FESSs is less than that of BESSs, and the high self-discharge rate must be considered. Amber Kinetics has developed a flywheel system with energy storage capability of more than four hours with minimal self-discharge losses [50]. However, this technology suffers from low power output capability and would require multiple units to supply the necessary high power of a DCFC station. Table 2-2 shows the energy and power density of three commercial flywheels.

Although FESS-based DCFC stations have not yet been implemented in the real world, FESSs are used for grid storage applications due to their high power density, and [54] outlines a comprehensive list of FESSs for frequency regulation, voltage support, and renewable energy integration. In [55], the use of FESS in DCFC stations is found to give a higher payback than BESSs, and [56] presents a control algorithm for FESSs in a DCFC station. Furthermore, hybrid

ESSs can be advantageous because the high power density of FESSs can be paired with high energy density storage such as batteries. For example, [57] proposes a hybrid flywheel-battery system to compensate the power fluctuation of large scale wind farms. In [58], a hybrid system is controlled in an islanded microgrid so that the FESS provides support during transients and the BESS sustains long-term load changes. Thus, this thesis analyzes both a FESS and a hybrid flywheel-battery ESS.

Table 2-2: Commercial Flywheel Technologies [50], [51]

Manufacturer	Amber Kinetics	Beacon Power (Model 400)	Beacon Power (Model 450 XP)
Maximum Power (kW)	8	100	360
Energy (kWh)	32	25	36
Size (m^3)	1.65	1.36	1.36
Energy Density(kWh/m^3)	19.40	18.36	26.47
Power Density (kW/m^3)	4.85	75.53	264.71

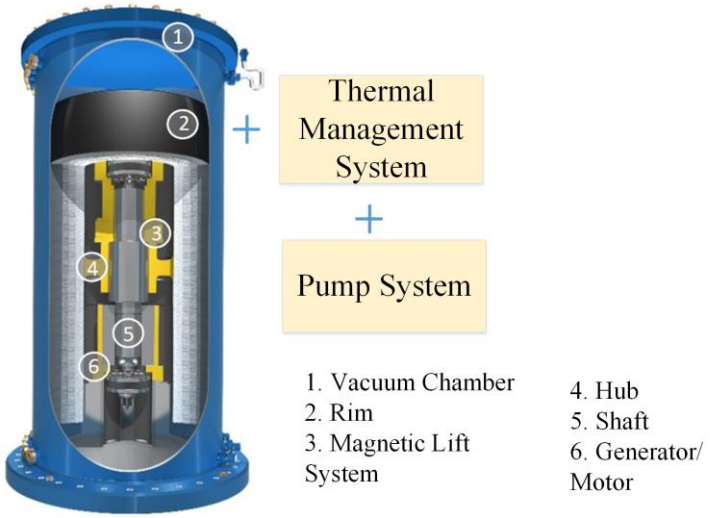


Figure 2-2. A general overview of a Beacon Power flywheel system [51]

Hydrogen storage has the advantage of high energy density and the possibility of dual use in fueling hydrogen powered vehicles as well as EVs. The energy density of compressed hydrogen gas at 700 bar is ~1300 kWh/m^3 [59] and the energy density of current 700 bar storage tank systems is ~800 kWh/m^3 [60]. Using an electrolyzer, electricity from the grid is converted to hydrogen, compressed, stored in a high-pressure gas tank, and then converted back to electricity when needed

by fuel cells, as shown in Figure. 2-3. Electrolyzers can have 85% efficiency at full load [61] and fuel cell peak efficiency ranges from about 50-60% [62], [63], thus, the round-trip efficiency is lower than that of batteries.

Though there are numerous hydrogen storage projects operating worldwide for storing excess renewable energy [33], [34], hydrogen storage has not yet been used in DCFC stations. However, there is a project on the combined operation of DCFC with a hydrogen refuelling station by the Institute of Transportation Studies at University of California, Davis [64]. Furthermore, [65] and [66] propose the use of hydrogen storage for the dual purpose of filling fuel cell vehicles and providing grid services, such as demand response.

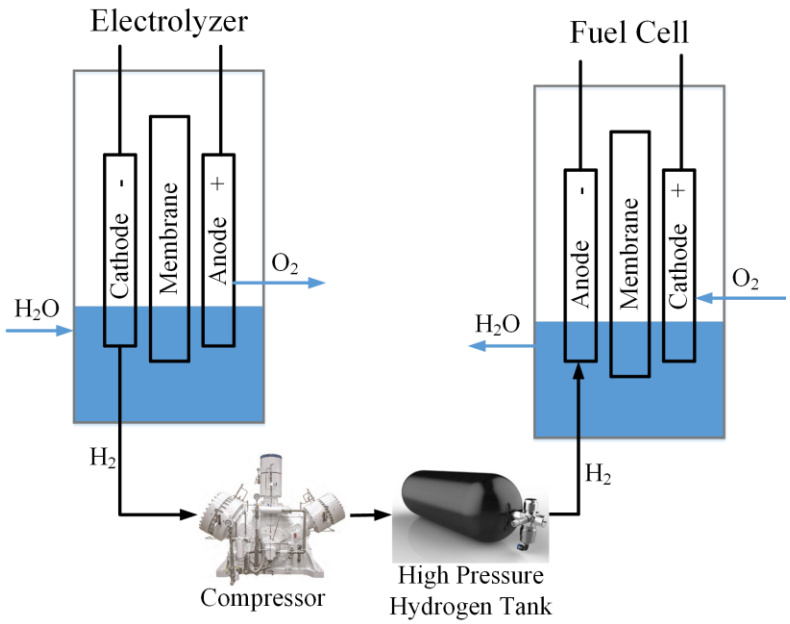


Figure 2-3. Overview of the components in a hydrogen storage system with on-site hydrogen and electricity generation

2.2 DCFC Station Architectures with ESSs

Two main architectures, AC-bus and DC-bus stations are discussed in the literature for fast charging stations. In AC-bus stations, the secondary side of a MV-LV distribution transformer is used as the common AC bus [67], [68] that the EV chargers connect to. For instance, the

commercially available DCFCs from Charge Point and ABB operate with AC input voltage of 400-480 V [69], [70] and for a multiport station using these chargers, each charger will connect to the common AC bus. Power electronic converters, which provide rectification, power factor correction (PFC), isolation, and voltage control, connect the main AC bus to the DC EV ports, and to energy storage systems and/or renewable energy sources, if used. The AC-bus architecture requires multiple power conversions to connect to DC loads and sources, and has more complex control [71]. In DC-bus stations, the EV chargers are all connected to a common DC bus, meaning only isolated DC/DC converters are required between the DC bus and the EV port. Thus, the DC-bus architecture generally has lower cost, smaller size, and better dynamic performance compared to the AC-bus architecture [72]. Therefore, this thesis focuses on the DC-bus architecture. However, it should be noted that designing protection systems for high voltage DC-bus systems is a challenge because DC current has no natural zero crossing [73], [74] and the reliability of DC-bus architectures relies on the central rectification stage [72].

The selection of the nominal DC bus voltage will depend mainly on two factors: the expected EV battery voltage and the maximum charging power (since higher powers will require higher voltages to keep current levels reasonable). Furthermore, when energy storage is to be connected directly to the bus, the voltage range of the storage system must be designed or chosen to match the desired bus voltage. For 400 V EVs (in which the battery voltage may range from about 250 V to 450 V), the DC bus voltage will generally be less than 1000 V [75], and [76] discusses a commercially-available DC/DC converter for 800 V electric buses with input voltage (i.e., DC bus voltage) up to 1200 V.

The following subsections review the most promising architectures for each considered energy storage system type, and a detailed discussion of the power electronic converters that can

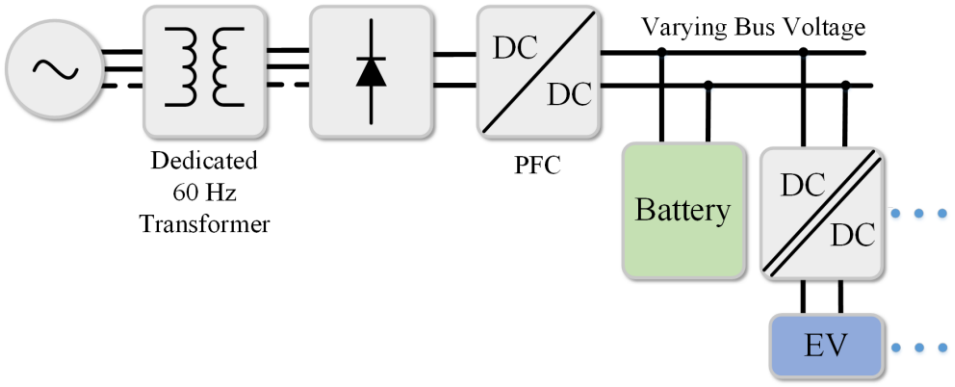
be used in these architectures is provided in the latter part of this chapter. One common requirement across all architectures is that each EV should be galvanically isolated from the DC bus so that there are no safety concerns with ground current flowing between multiple EVs plugged into the same DCFC station [75], [77]. Thus, all architectures include a high power isolated DC/DC converter between the DC bus and the EV.

2.2.1 Architectures with Battery ESSs

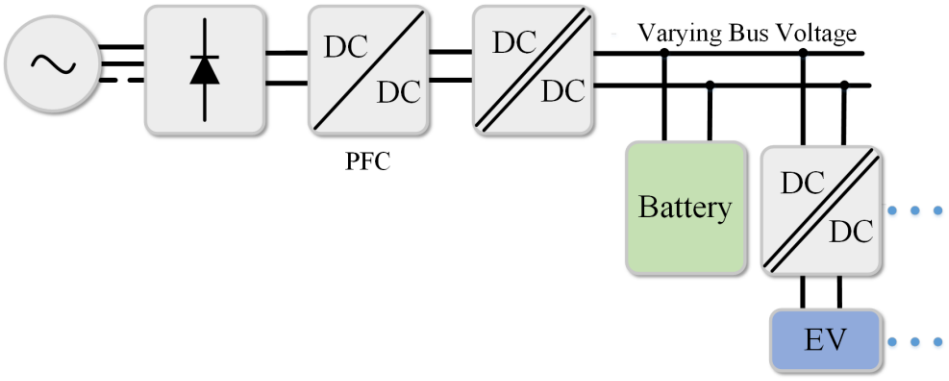
A battery ESS DCFC architecture with common DC-bus must provide AC-DC rectification, power factor correction, voltage control, and isolation between the battery and the grid [78]. This isolation is recommended to prevent any ground faults from flowing in the case of a degraded or compromised battery casing [79], [80]. This requirement for isolation between the grid and the storage battery is an additional constraint that is not present for DCFC stations without energy storage, where isolation is only required between the grid and the EV. Figure. 2-4 shows three methods for achieving isolation between the grid and the storage battery. In Figure. 2-4(a), a dedicated low-frequency transformer is used, along with a standard diode rectifier and PFC DC/DC converter. This architecture has the advantage of simplicity, as fewer power electronic converters are required compared to the other methods of achieving isolation. However, a large low-frequency transformer can add cost and volume to the system. Figure. 2-4(b) instead uses a high-frequency transformer in an isolated DC/DC converter, which will reduce system volume. In both of these architectures, the battery is directly connected to the DC bus, meaning this bus voltage will vary as the battery state-of-charge (SOC) changes and as the battery terminal voltage fluctuates with charging and discharging events. Thus, the PFC DC/DC converter in Figure. 2-4(a) and the isolated DC/DC converter in Figure. 2-4(b) must be designed to allow the output voltage swing to vary fully with the battery terminal voltage swing. Furthermore, this direct battery

connection to the DC bus means the isolated DC/DC converter which connects to the EV must have a wide input voltage range and a wide output voltage range (corresponding to the battery voltage swing in the EV as its SOC rises). The BESS voltage can vary widely depending on the battery cell and module design, for example with ranges of 730-946 V [43] and 486-756 V [81]. This constraint complicates the design of the EV DC/DC converter since soft switching is hard to achieve over a wide range of input and output voltage [82], [83].

Figure 2-4(c) shows an alternative where the DC bus voltage is fixed due to the use of an isolated DC/DC converter between the DC bus and the BESS. This fixed bus voltage simplifies the design and control of the other DC/DC converters in the system. However, in smaller DCFC stations that have a low-power connection to the grid (e.g., 10kW-50kW), the isolated DC/DC converter connected to the battery ESS would need to be sized large enough to provide the high EV charging power (e.g., 150 kW). This would result in a larger and more costly isolated DC/DC converter compared to that required in the lower-power path in Figure. 2-4(b). Each isolation strategy has advantages and disadvantages, and the strategy shown in Figure. 2-4(b) will be used in the discussion of other architecture options.



(a)



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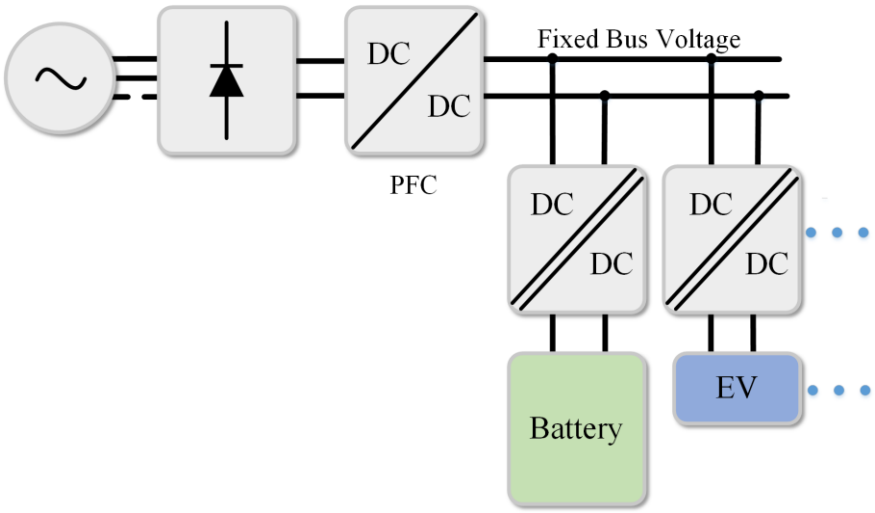


(c)

Figure 2-4. DCFC architecture with BESS where isolation is provided with (a) dedicated low frequency transformer (varying DC bus voltage), (b) isolated DC/DC converter (varying DC bus voltage), and (c) isolated DC/DC converter (fixed DC bus voltage).

One option to reduce components is to use an isolated DC/DC converter that can also perform power factor correction, as shown in Figure. 2-5(a). Different isolated DC/DC converters with PFC capability can be found in the literature for various power levels [84]–[88]. With an isolated PFC stage, the overall size and cost of the AC-DC conversion stage is reduced while improving the efficiency. In order to provide services to the grid, a DCFC station with energy storage must have a bidirectional connection to the grid, as shown in Figure. 2-5(b). This active front end can also provide power factor correction due to active control of the reactive power flow using pulse width modulation (PWM) control.

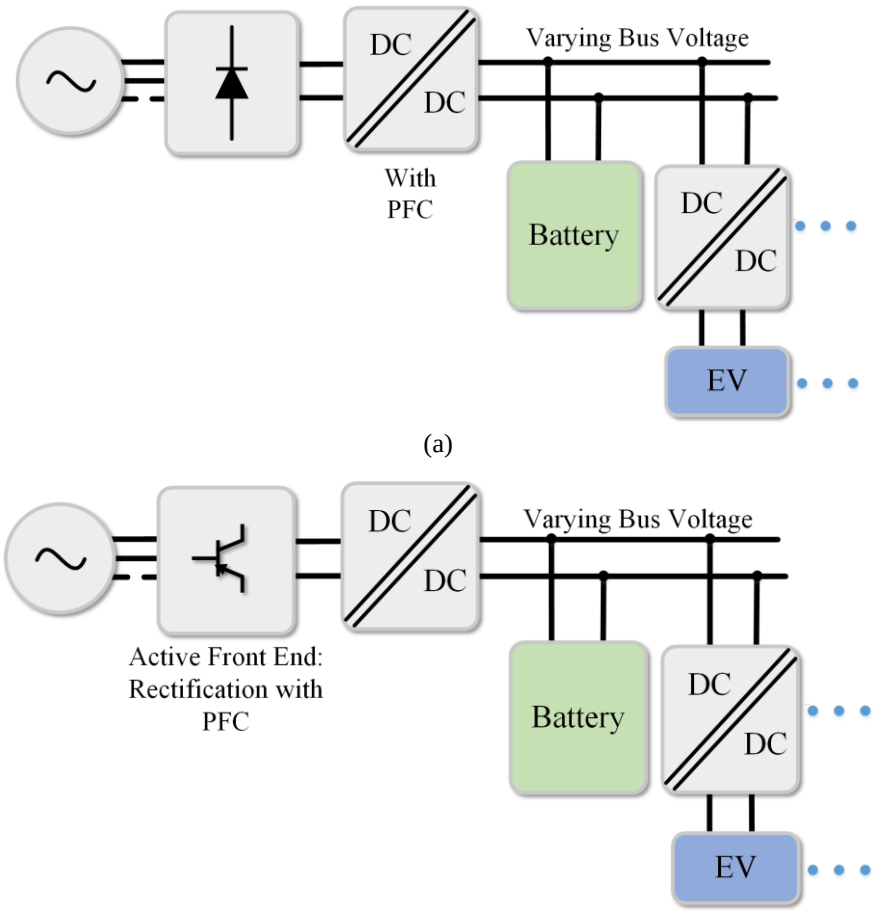


Figure 2-5. DCFC architecture with BESS where (a) PFC is provided by an isolated DC/DC converter (unidirectional) and (b) PFC is performed with active switches along with rectification (bidirectional)

2.2.2 Architectures with Flywheel ESSs

Unlike BESSs, commercial FESSs have one or more power converters integrated into the system for controlling the flywheel motor. Thus, all commercial flywheel systems include a DC-to-high frequency AC converter to control the flywheel motor. For a DC-input flywheel system, this is the only power converter included in the module, and this flywheel system connects to a DC bus which can range in voltage from about 550 V to 750 V [50]. For an AC-input flywheel system, an additional AC/DC converter (active front end) is included to allow bidirectional power flow between the flywheel and the AC grid [51]. The type of input connection of a commercial flywheel system will determine where in the architecture the FESS should be connected.

As per IEEE 1547 standard [89], galvanic isolation should also be provided between the FESS and the grid. Similar to the BESS, this isolation can be provided by a dedicated low-frequency transformer or an isolated DC/DC converter with high-frequency transformer. Figure. 2-6(a) shows a DCFC architecture for an AC-input FESS, where, due to the grid-frequency AC input requirement, it is preferable to connect the flywheel before the rectification stage rather than at the common DC bus. A low-frequency transformer is preferred for isolation in AC-input FESS-based stations to reduce the power electronic conversion stages. A diode rectifier and PFC DC/DC converter (or active front end) are used to create the DC bus for EV connection.

DC-input FESS-based DCFC stations are shown in Figures. 2-6(b) and 2-6(c). Figure. 2-6(b) shows the use of a low-frequency transformer for isolation, and Figure. 2-6(c) shows the use of an isolated DC/DC converter. For a smaller DCFC station with a lower-power grid connection, the DC-input FESS is advantageous because there are less high-power converters required in the path between the flywheel and the EV: two converters are in this path in Figures. 2-6(b) and 2-6(c), while five converters are in this path in Figure. 2-6(a). Similar to the BESS case, an active front end must be used in the DC-connected FESS architectures if the energy storage is also planned to provide services to the grid.

2.2.3 Architectures with Hydrogen ESSs

In a DCFC station with hydrogen storage, the electrolyzer does not need to be galvanically isolated from the grid, yet the fuel cell is a generation source, and thus should be isolated from the grid [89]. It is common practice to use a DC/DC converter at the output of a fuel cell because fuel cells have widely varying output voltages dependent on load and fuel cells behave like a current source with low voltage and high current [90]. Thus, the architectures considered in this thesis use a DC/DC converter at the fuel cell output.

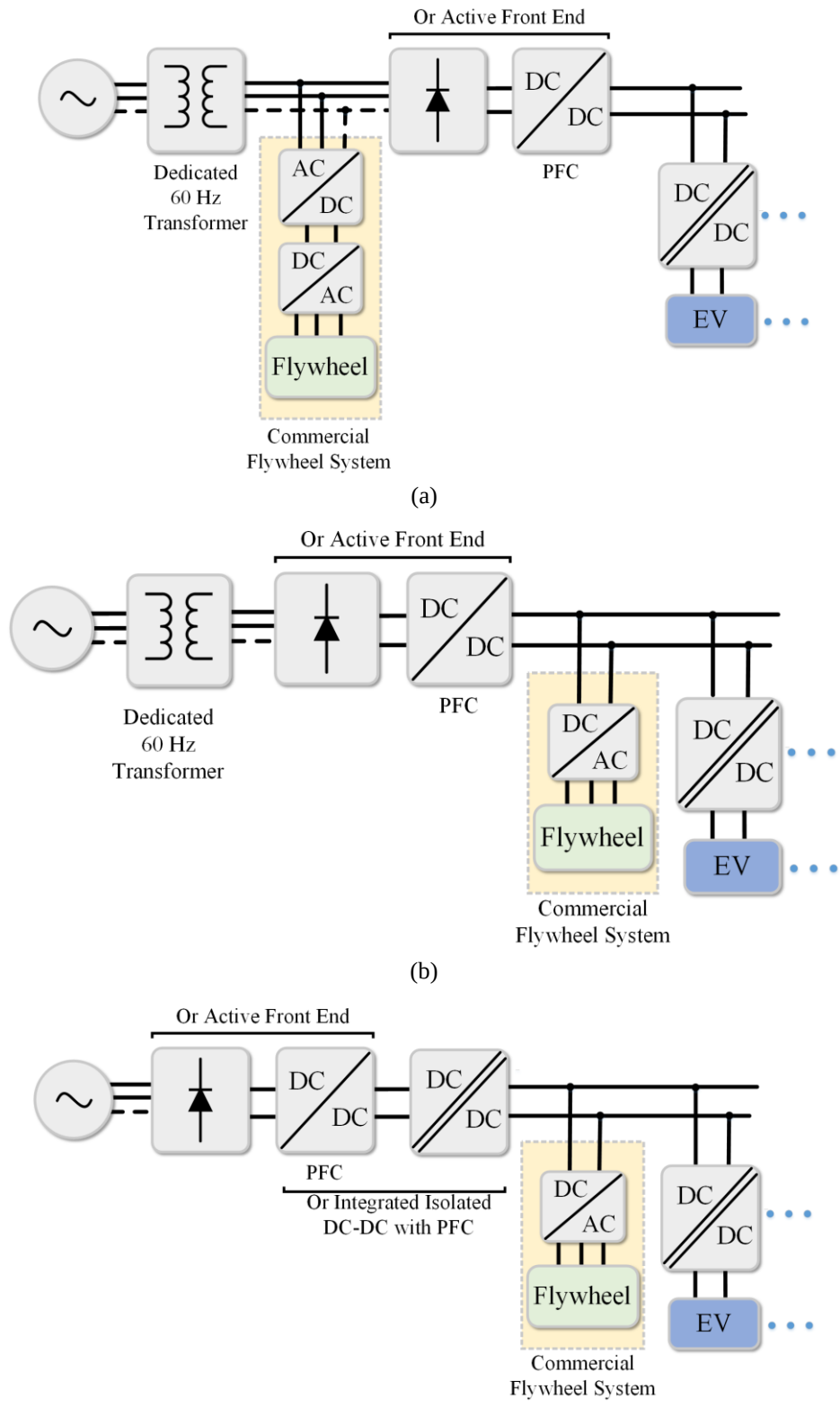
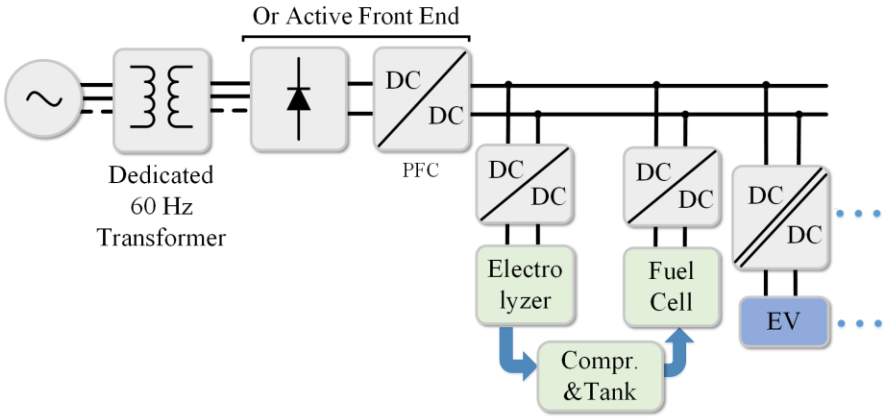


Figure 2-6. DCFC architecture with (a) AC-input FESS, (b) DC-input FESS with dedicated LF transformer, and (c) DC-input FESS with isolated DC/DC converter.

Figure. 2-7(a) shows a hydrogen storage DCFC architecture with a dedicated low-frequency transformer at the AC grid connection. In this case, a non-isolated DC/DC converter can be used at the fuel cell output, which will be lower-cost and higher-efficiency than an isolated DC/DC converter of the same power rating. Since the fuel cell to EV path is the highest power path for a DCFC station, it is advantageous to minimize the number of isolated DC/DC converters in this path to reduce the number of high-power transformers required. Figure. 2-7(b) shows another architecture option which also allows a non-isolated DC/DC converter to be used after the fuel cell. An isolated DC/DC converter is instead used in the grid interface, if a low-frequency transformer is not used. In Figure. 2-7(c), the grid connection is simplified, requiring only a rectifier and a PFC DC/DC converter, yet an isolated DC/DC converter is used at the fuel cell output. This architecture may be advantageous when the grid connection is higher power and the hydrogen storage system is used to provide smaller boosts of power during EV charging. In all these architectures, a non-isolated DC-DC converter is used at the electrolyzer terminal to control the hydrogen production [91]. The active front end options of Figure. 2-7 are required for bidirectional power flow if it is desired to use the stored hydrogen energy to provide services to the grid. The DC-bus voltage can be controlled using the fuel cell DC/DC converter; for example, [92] allows any output voltage between 375 V and 750 V.



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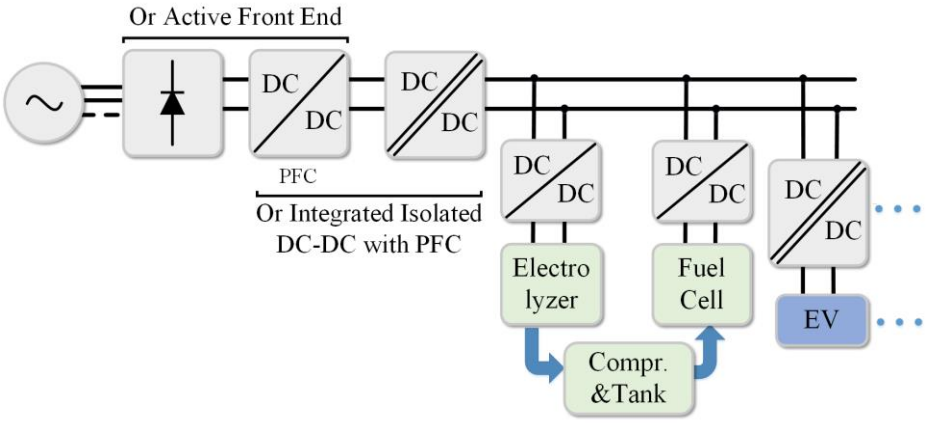

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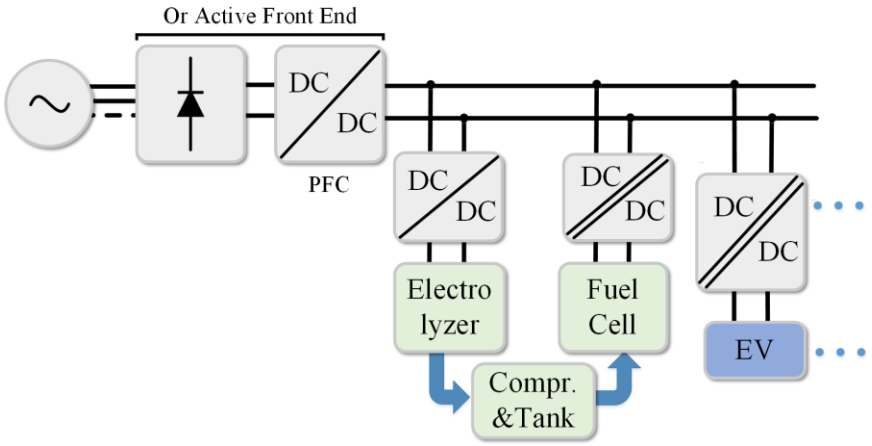
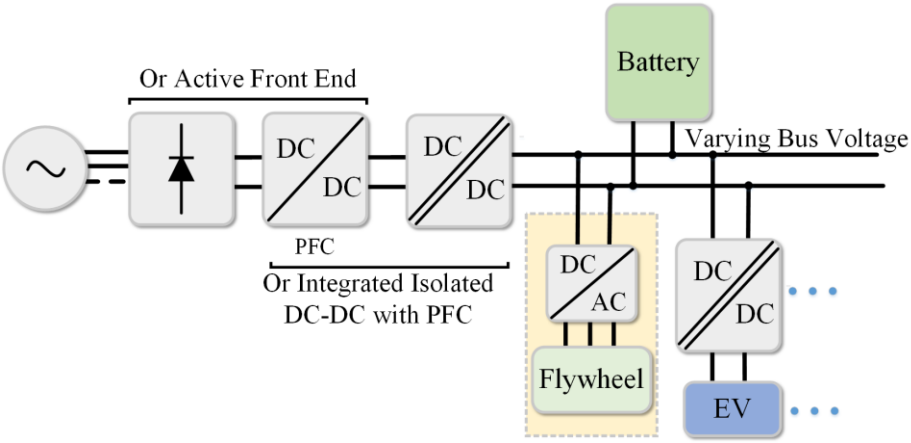


(c)

Figure 2-7. DCFC with hydrogen storage with on-site hydrogen and electricity generation with (a) dedicated LF transformer, (b) isolated DC-DC converter at the grid side, and (c) isolated DC/DC at the fuel cell terminal.

2.2.4 Architectures for Flywheel-Battery Hybrid ESSs

Similar to the DCFC architectures with BESS and FESS, there must be isolation between the grid and energy storage components in a flywheel-battery hybrid ESS. Figure. 2-8(a) shows a hybrid architecture with a DC-input flywheel, where the DC bus is allowed to vary with the battery voltage. Isolation is provided by an isolated DC/DC converter at the grid side. Figure. 2-8(b) shows an alternative where a DC/DC converter connected to the battery provides a fixed DC bus voltage, increasing losses into and out of the battery, but reducing the complexity of the DC/DC converter designs due to the fixed bus voltage. A low frequency transformer can also be used for grid isolation, though this increases system volume.



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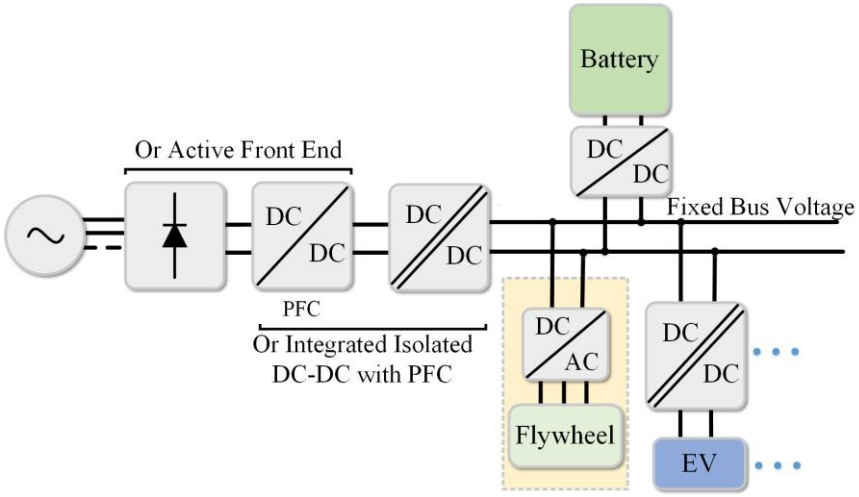


(b)

Figure 2-8. DCFC architectures for hybrid flywheel-battery ESS with (a) varying and (b) fixed DC bus voltage.

2.3 Power Electronics Converters in DCFC Stations with Energy Storage

There are three main differences to be considered in the design of power electronic converters for DCFC stations with energy storage compared to converters designed for DCFC stations without energy storage. Firstly, for a small DCFC station with only one or two vehicle charging ports, the AC/DC conversion stage (between the grid and the common DC bus) can be of a lower power rating since the high power charging comes from the ESS. Thus, single-phase topologies can be considered for the lowest AC grid power connections, and the size and cost of the AC/DC conversion stage can be reduced. Secondly, due to the potential economic payback of

utilizing a DCFC ESS for providing grid services, bidirectional AC/DC conversion stages may be merited. Thirdly, the isolated DC/DC converter between the common DC bus and the EV port may have a widely varying input and output voltage range, if a BESS is connected directly to the DC bus, as in the architectures shown in Figures. 2-4(a) and 2-4(c). With a focus on these issues, this section discusses promising power electronic converter options for the AC/DC conversion stage, and isolated DC/DC converter options.

2.3.1 AC/DC Conversion Stage

The AC/DC conversion stage is composed of all converters between the AC grid and the DC common bus. If the ESS is not isolated from the DC common bus, the AC/DC conversion stage must provide galvanic isolation, either with a dedicated low frequency transformer or with a high frequency transformer in an isolated DC/DC converter. It must also provide AC/DC rectification, power factor correction to improve power quality at the AC mains and reduce losses, and a DC bus voltage level which is suitable for the ESS and EV connections. Optionally, the AC/DC conversion stage can provide bidirectional power flow capability to allow the energy storage to provide grid services.

For unidirectional power flow and relatively low grid connection power ratings, a simple option is the single-phase full-bridge diode rectifier followed by a boost, buck, or buck-boost DC/DC converter for improved power factor [93]. For a 240 V grid voltage, a boost converter would most commonly be used after the diode rectifier, as shown in Figure. 2-9(a), in order to create a common DC bus with high enough voltage to connect to a 300 V to 400 V or higher ESS. If the ESS operates at a lower voltage, a single-switch buck-boost converter, as shown in Figure. 2-9(b), could be used. The buck-boost topology could also be based on the SEPIC converter, or another two-switch topology [93].

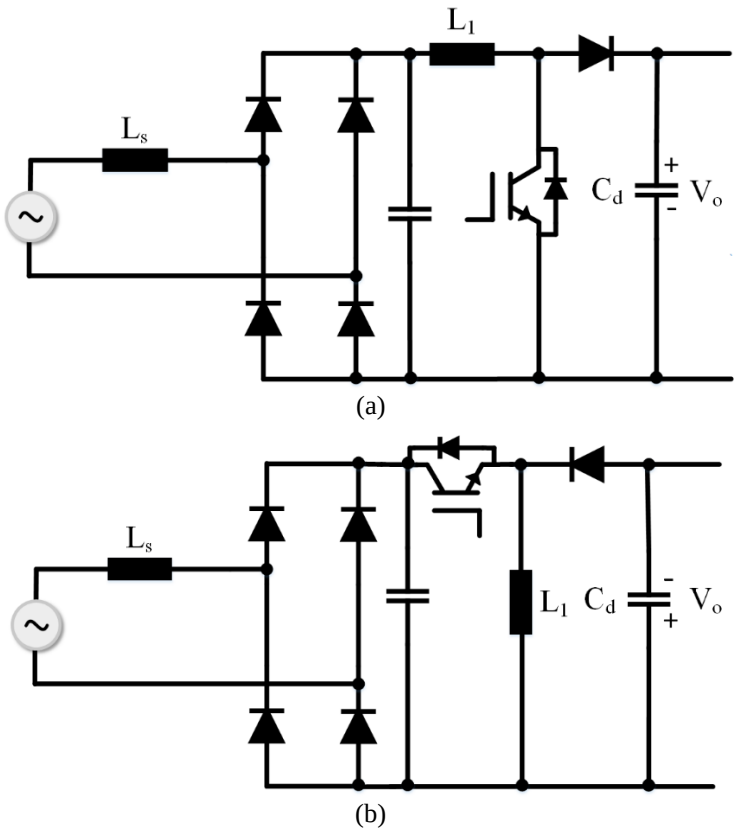
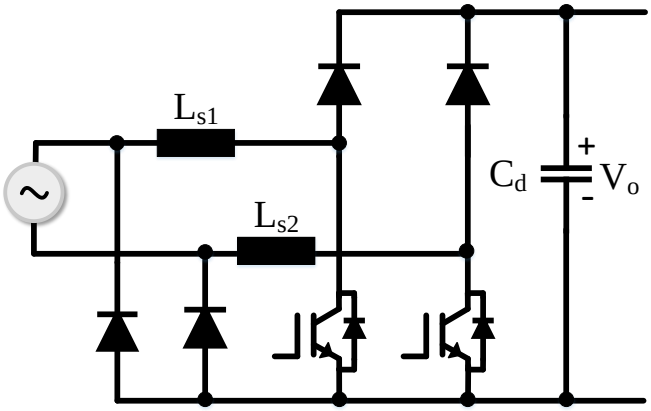


Figure 2-9. Single-phase diode bridge rectifier with (a) boost and (b) buck-boost PFC

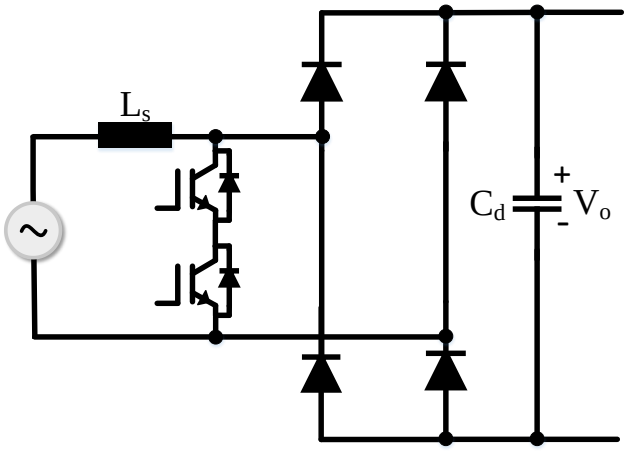
Even though the diode rectifier with boost or buck-boost PFC is capable of high power quality and power factor, these converters are susceptible to low efficiency due to high conduction losses in the diode bridge. To improve the efficiency of the AC/DC conversion stage, bridgeless topologies can be considered. The basic bridgeless boost topology suffers from large common-mode noise compared to the traditional bridge topology [94], [95]. The most practical bridgeless boost PFC converters are dual-boost bridgeless PFC and back-to-back bridgeless PFC as shown in Figures. 2-10(a) and 2-10(b), respectively. Soft-switching of these converters while operating in discontinuous conduction mode can further reduce losses. The totem-pole bridgeless PFC is also emerging as an excellent choice for low power if wide band-gap devices are used to solve the issue of severe reverse recovery losses common with the use of silicon MOSFETS [96]. Figure. 2-10(c) shows the totem-pole bridgeless PFC with gallium nitride (GaN) devices. Different multilevel

topologies are also available for further reduction of conduction losses or to deal with higher voltages. One such three-level boost PFC is presented in [95]. The bridgeless topologies of buck-boost converter are still in development since the techniques applicable to bridgeless boost topologies are more difficult to apply in bridgeless buck-boost converters [97].

Among the active front end boost topologies for reverse power flow capability, as in the DCFC architecture in Figure. 2-5(b), the full-bridge topology as shown in Figure. 2-11(a) is a common choice due to its simplicity and high power capability. In addition, different three-leg topologies with additional capacitor or inductor are also available to reduce the output DC voltage ripple [93]. The topology with a third leg and an additional inductor is shown in Figure. 2-11(b).



(a)



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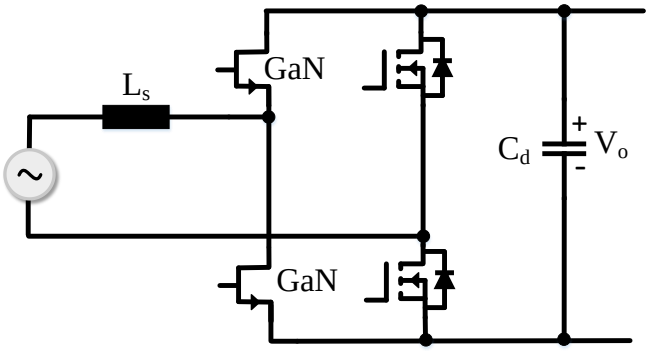
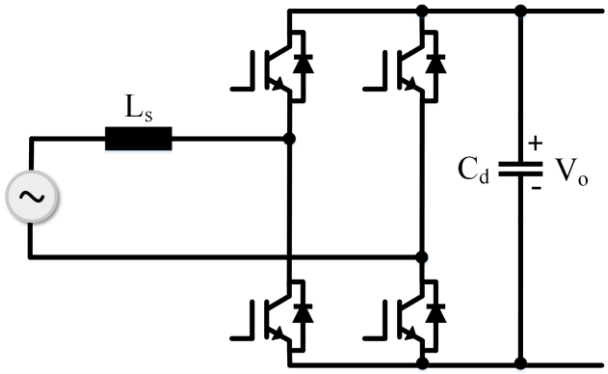
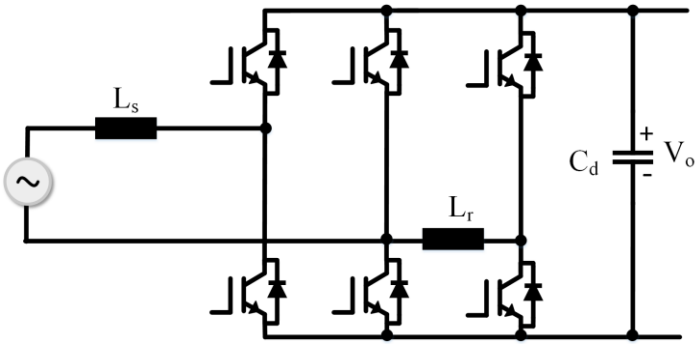


(c)

Figure 2-10. (a) Dual-boost bridgeless PFC, (b) back-to-back bridgeless PFC, and (c) totem-pole PFC with GaN switches



(a)



(b)

Figure 2-11. Single-phase bidirectional converter with (a) four and (b) six active switches

Similarly, for a higher power three-phase grid connection, boost and buck-boost DC/DC converters can be used after a three-phase diode rectifier. Figure. 2-12(a) shows a three-phase diode rectifier with a boost PFC, where the line inductance is used as the boost inductor, and Figure. 2-12(b) shows a three-phase diode rectifier with a buck-boost PFC. The main advantage of the Vienna rectifier, shown in Figure. 2-12(c), is the three-level characteristics due to split DC-

bus, and the switches, therefore, only need to block half of the peak value of mains line-to-line voltage [98]. However, the Vienna rectifier suffers from the issue of voltage balancing of three-level converters, and the reactive power controllability depends on the output voltage due to limited modulation vector [75], [98]. Bridgeless topologies are not common for three-phase systems – in most cases, three single-phase bridgeless topologies are paralleled if required [97].

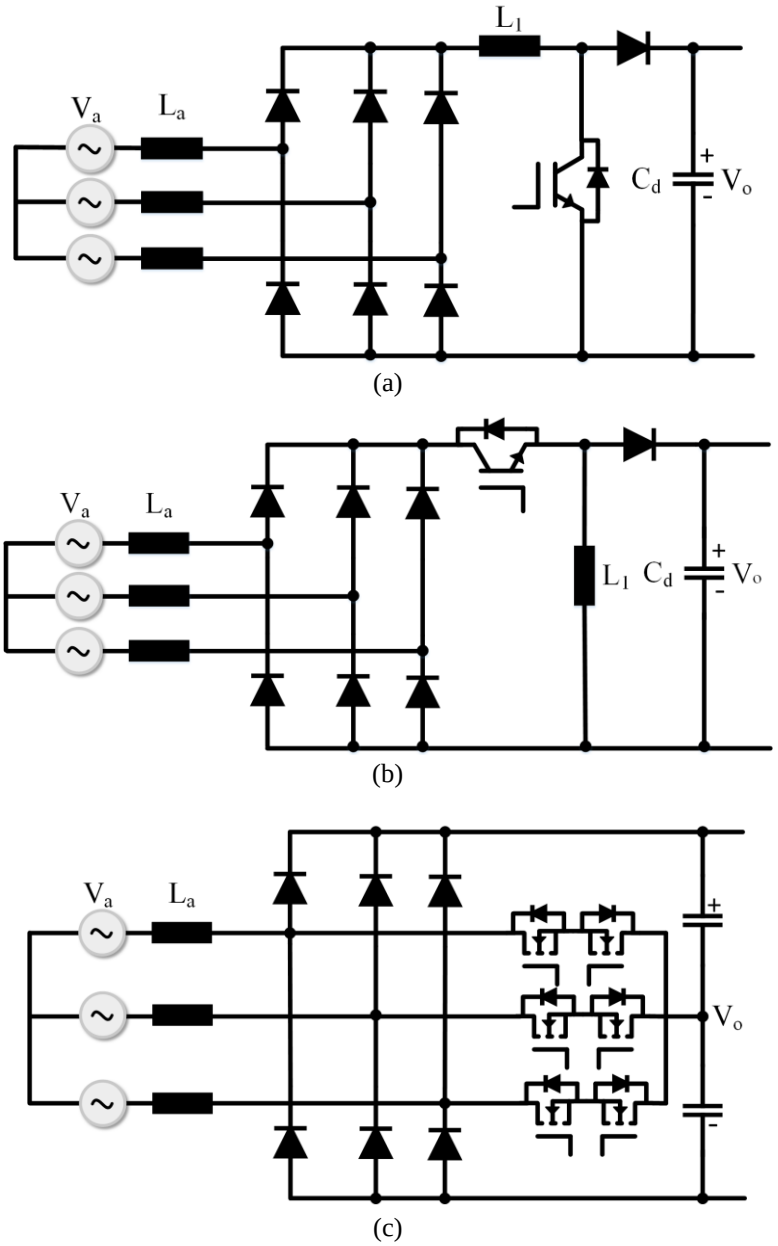


Figure 2-12. Three-phase rectifiers with (a) boost and (b) buck-boost PFC and (c) Vienna rectifier as a modification of boost topology

Three-phase active front end converters are used for high-power grid connections that require bidirectional power flow between the grid and the ESS so that the ESS can also be used to provide services to the grid such as frequency control, voltage support, and peak power [26]. One of the most common bidirectional AC/DC converter topologies is the two-level voltage source converter (2L-VSC), as shown in Figure. 2-13(a). This 2L-VSC is a six-switch boost topology and insulated-gate bipolar transistors (IGBTs) are commonly used for these higher power levels. Since this power converter is based on active switches, almost pure sinusoidal current can be generated at the grid terminal along with the required power factor.

For medium voltage (MV) grid connections, the three-level Neutral Point Clamped (3L-NPC) converter, shown in Figure. 2-13(b), is bidirectional and can solve the limited power capability of the 2L-VSC as it can handle input voltages of 2.2-6.6 kV [99]. The connection of two diodes in each phase leg results in three-level voltage waveforms, unlike the 2L-VSC, which have lower total harmonic distortion (THD). The presence of a neutral point needs attention and balancing is required for proper operation. Moreover, a bipolar DC bus operation is proposed in [100]. This will help reduce the conversion efforts of DC/DC converters as the input DC voltage will be reduced to half compared to unipolar DC bus operation. However, this bipolar DC bus operation is challenging in a fast-charging station due to the variable nature of the load; very complex DC bus voltage balancing is required in such an operation. Furthermore, higher levels such as five-level, seven-level topologies are also possible but have not been used a lot commercially.

The above-mentioned converters can be used in DCFC architectures to create a common DC bus where isolation is provided by a dedicated low frequency transformer or separate isolated DC/DC converters. Alternatively, previous research has investigated various PFC topologies

which can also provide isolation, which can be used in the architecture of Figure. 2-5(a). Even though these topologies are mainly used in industrial motor drive systems, these converters can also be used as front-end converters in DCFC stations. For instance, [84] presents a single phase isolated bridgeless Cuk converter-based PFC rectifier for DC motor drive, as shown in Figure. 2-14(a). Also, [87] presents a three-phase isolated Cuk-based PFC rectifier which uses three single phase isolated Cuk converters, as shown in Figure. 2-14(b). These converters are capable of unidirectional power flow. On the other hand, [87] describes a three-phase matrix-type Dual Active Bridge (DAB) buck-boost isolated PFC rectifier which can be used for bidirectional power flow applications, as shown in Figure. 2-14(c).

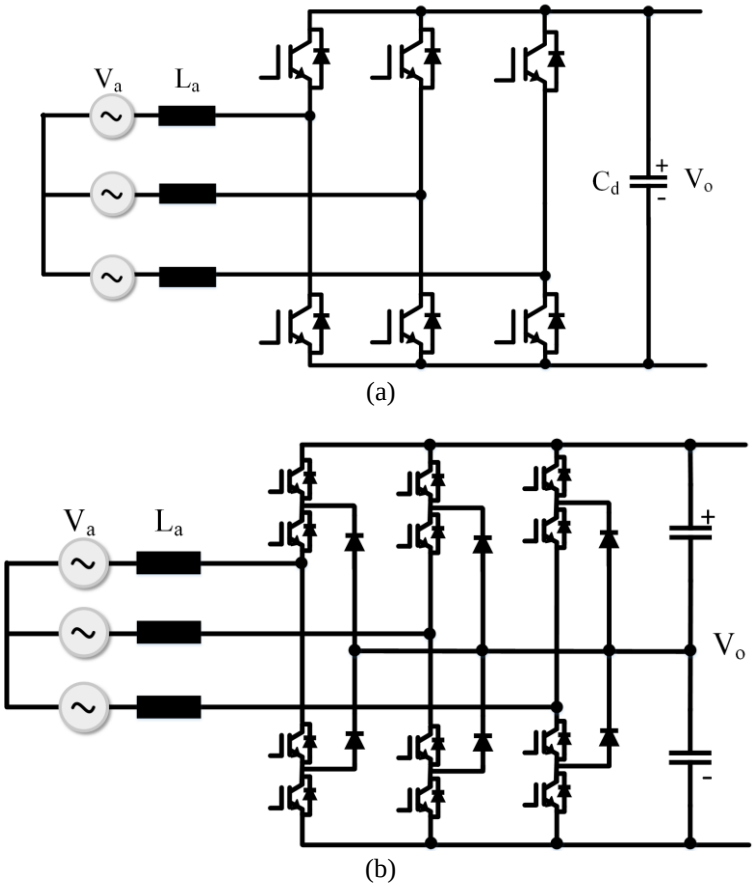


Figure 2-13. Three-phase bidirectional (a) 2-Level and (b) 3-Level NPC topology

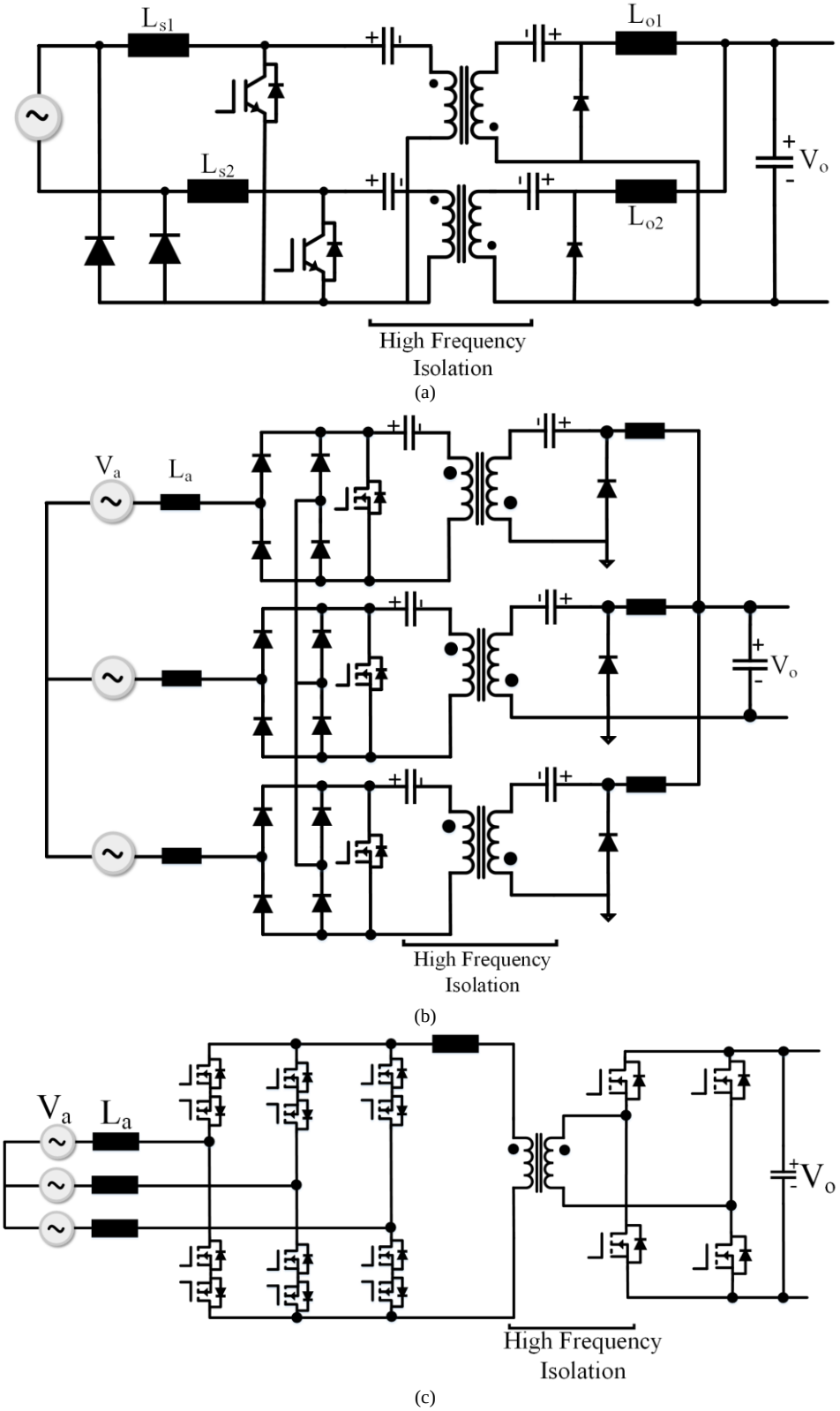


Figure 2-14. (a) Single-phase bridgeless Cuk topology based isolated PFC, (b) three-phase isolated PFC with three single-phase Cuk converter, (c) bidirectional DAB based three-phase PFC.

2.3.2 Isolated DC/DC Converter Topologies

Isolation in DC/DC converters is provided with high frequency transformers. A detailed review of various isolated DC/DC converters is presented in [75]. Isolated DC/DC converters can be used in the AC/DC conversion stage of a DCFC station if isolation is not provided by a dedicated low frequency transformer, as shown in Figure. 2-4(b). This converter can be unidirectional or bidirectional if the ESS will be required to provide grid services. A high power bidirectional converter is required for connection with the battery ESS in the architecture shown in Figure. 2-4(c). For the high power isolated DC/DC converter connecting from the DC bus to the EV battery, a unidirectional converter will generally suffice. While much research has investigated the possibility of EV batteries providing services to the grid (V2G) [101], [102], this scenario works best for idle vehicles that can be plugged in to charge/discharge for longer periods of the day (e.g., while parked at home or at work). Since DCFC stations are inherently used by drivers who need a fast charge to continue their driving plans, V2G grid services are not ideal for these on-the-go vehicles. This assumption simplifies the design of the high power isolated DC/DC converter that connects to the EV by allowing it to be unidirectional. However, the design and control can be complicated by the fact that the input voltage (DC bus in Figure. 2-5(a)) and output voltage (EV battery voltage) can vary widely, depending on the particular SOC of the storage and EV batteries. Thus, these converters should have wide input and output voltage ranges. The two prominent converter topologies for this application are discussed below.

One suitable converter is the unidirectional phase-shifted zero voltage transition full-bridge converter [103], as shown in Figure. 2-15(a). Due to the capability of zero voltage turn-on, this converter can be operated at high power and high switching frequency resulting in high power density. Even though zero-voltage switching can be guaranteed around rated power, this capability

is lost with light load in this converter topology. However, since the aim of a DCFC station is to top up the EV battery as quickly as possible, it is expected that the converter will operate at rated power most of the time, and thus this converter topology has proven to be a good candidate for DCFC applications. For the potential bidirectional isolated DC/DC converter in the AC/DC conversion stage, the related DAB phase-shifted converter is suitable, as shown in Figure. 2-15(b). Different phase-shift control methods such as single phase shift, dual phase shift, and triple phase shift are possible with DAB converters, whereas only the single phase shift method is applicable for the former unidirectional topology. Moreover, half-bridge topologies of these converters are also available which are sometimes preferred over full-bridge ones for lower power grid connections due to lower size, weight, and cost [103].

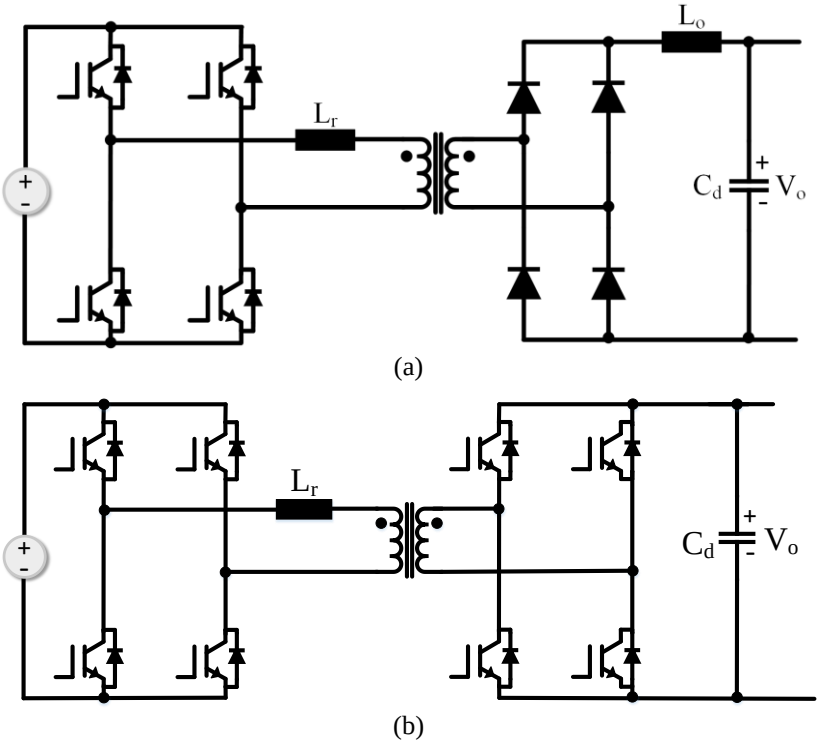
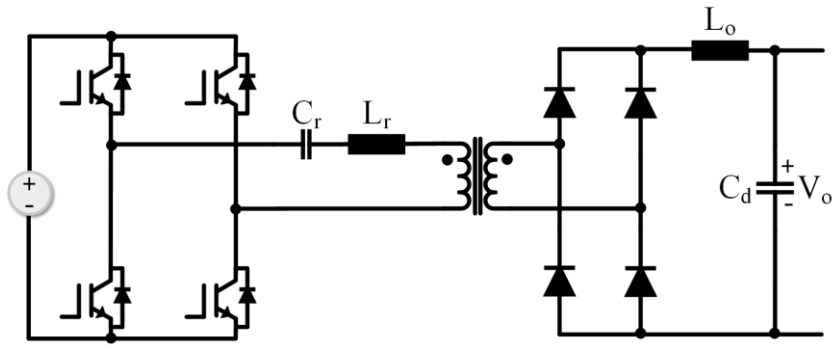


Figure 2-15. Full-bridge phase-shifted ZVS converter (a) unidirectional and (b) bi-directional.

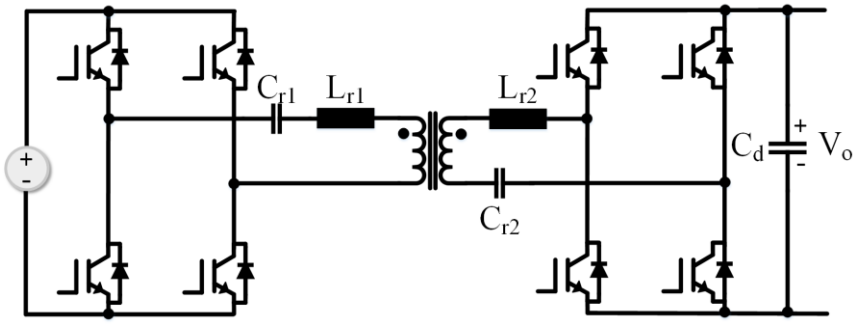
Another popular isolated topology for a DCFC station is the full-bridge LLC (FB-LLC) resonant converter [75], [103] because zero voltage switching (ZVS) is achievable over a wide load range.

The unidirectional version of the FB-LLC converter is shown in Figure. 2-16(a). A FB-LLC converter achieves voltage regulation by voltage division with frequency dependent impedance, which provides a variable voltage gain. Therefore, the switching frequency varies for the purpose of line and load regulation, which makes the design of passive components complicated. Therefore, the gain curves should be as narrow as possible, i.e., high gain variation within a small frequency range to have a wide output voltage range. The variation in the gain curve at different operating points makes the design, operation, and optimization of the FB-LLC complex. However, if the converter operates close to resonant frequency, very high efficiency is achievable due to ZVS operation. The LLC converter has some advantages over other ZVS topologies in terms of short-circuit protection, good voltage regulation at light loads, ZVS over a wide load range, ZCS for power diodes, and only a capacitor filter rather than the conventional LC filter [104]–[106].

A bidirectional LLC converter is shown in Figure. 2-16(b) and can be used within the AC/DC conversion stage, or for connecting to the ESS in the architecture shown in Figure. 2-4(c). However, the gain curve of such an LLC converter reduces to a simple series resonant converter (SRC) during bidirectional operation, i.e., regeneration mode [107]. Since the efficiency of an SRC reduces significantly as the operating switching frequency moves away from the series resonance, the efficient operation of the LLC converter in regenerative mode is limited. Even though some literature has proposed symmetrical operation of LLC converters, these converters lose their symmetry as the input and output voltage vary. For bidirectional operation, a modified LLC converter with an additional capacitor at the secondary side of the high frequency transformer is proposed, known as the CLLC converter [110], [111]. Moreover, a half-bridge topology of the LLC converter is also possible [103].



(a)



(b)

Figure 2-16. Full-bridge LLC converter (a) unidirectional and (b) bi-directional

Chapter 3

Analysis of DCFC Stations with ESSs

3.1 DCFC Layouts and Parameters

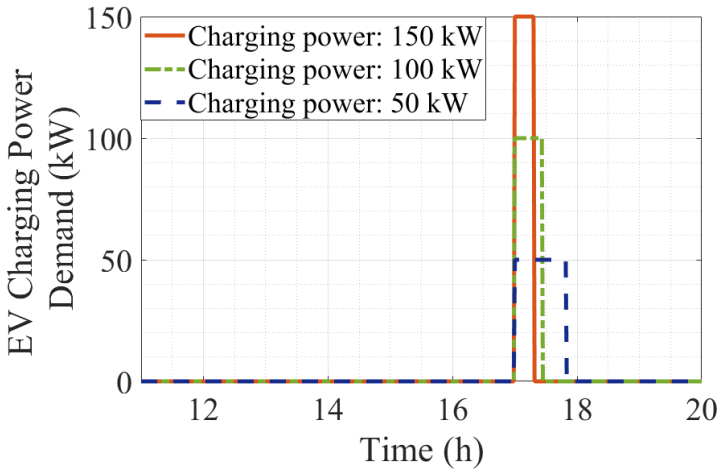
In this chapter, battery, flywheel, hydrogen, and hybrid flywheel-battery storage systems are analysed in terms of overall system efficiency, volume, and cost for three different EV charging rates: 50 kW, 100 kW, and 150 kW in three different DCFC station scenarios. The first charging station scenario is a small one with only one vehicle charging event assumed per day. This type of charging station could be found along highways in remote areas and in this study, it relies on a single-phase 15 kW grid connection. The second charging station scenario has two charging ports and is assumed to charge five vehicles per day. Moreover, two of the vehicles are assumed to charge simultaneously during the peak charging hour of 5pm. This charging station is connected to the grid via a three-phase 50 kW connection. The third charging station scenario is a large one with five charging outlets similar to the average charging outlets in an Electrify America DCFC station [109]. Various studies have predicted there could be between 11 [15] and 25 [110] daily charging events for this larger station type. Thus, this analysis assumes the large station has 20 daily charging events, with up to five vehicles charging simultaneously. This large charging station has a grid connection of 150 kW. Figure. 3-1 shows the assumed EV charging power demands for each station in this analysis, where the demands in the medium and large stations are estimated from the probability distributions in [111], [112]. Figure. 3-1 shows that higher EV charging rates cause a smaller overlap in charging events as each EV is charged more quickly. Based on these assumptions, the three DCFC stations are modelled in MATLAB/Simulink.

In the MATLAB/Simulink model, the EVs are modelled as Tesla Model S EVs with 85 kWh batteries. The battery specifications are shown in Table 3-1. It is assumed that the EVs arrive at the DCFC station when the battery SOC is 20% and that they get charged up to 70%. For simplicity, the EVs are charged with constant power, and the charging current is calculated using

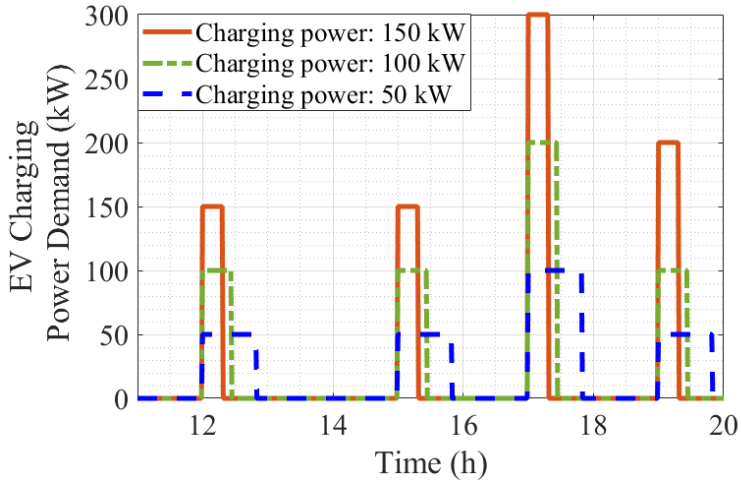
(3.1) where $P_{charg.}$ and $V_{battery}$ are the charging power and battery terminal voltage, respectively. Using the charging current, the battery SOC is calculated using (3.2) where SOC_{init} is the battery initial SOC and $C_{battery}$ is battery capacity in Ah. The SOC changes of the EV battery at different charging powers are shown in Figure. 3-2.

Table 3-1: Specification of Tesla Model S Battery

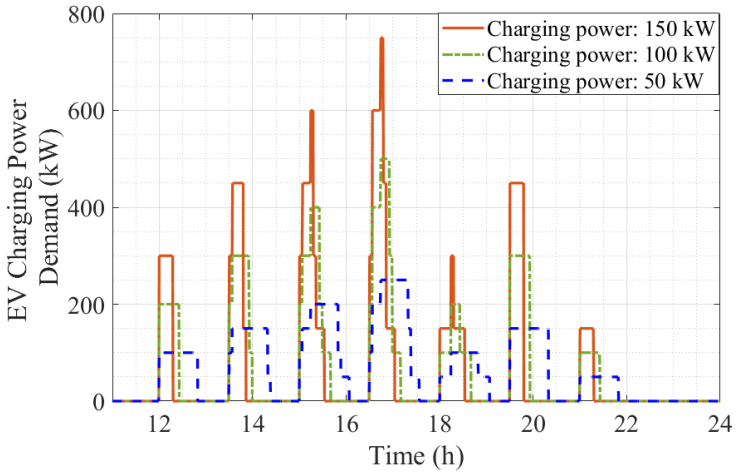
Parameter	Value
Battery Nominal Energy	85 kWh
Battery Nominal Voltage	375 V
Battery Capacity	226.67 Ah
Battery Charging Resistance	1.2 mΩ



(a)



(b)



(c)

Figure 3-1. Charging power demand along the day in the (a) small charging station, (b) medium charging station, and (c) large charging station

$$I_{charg.} = \frac{P_{charg.}}{V_{battery}} \tag{3.1}$$

$$SOC_{battery} = SOC_{init} + \frac{1}{C_{battery} \times 3600} \int_{t_{start}}^{t_{end}} I_{charging}\, dt \tag{3.2}$$

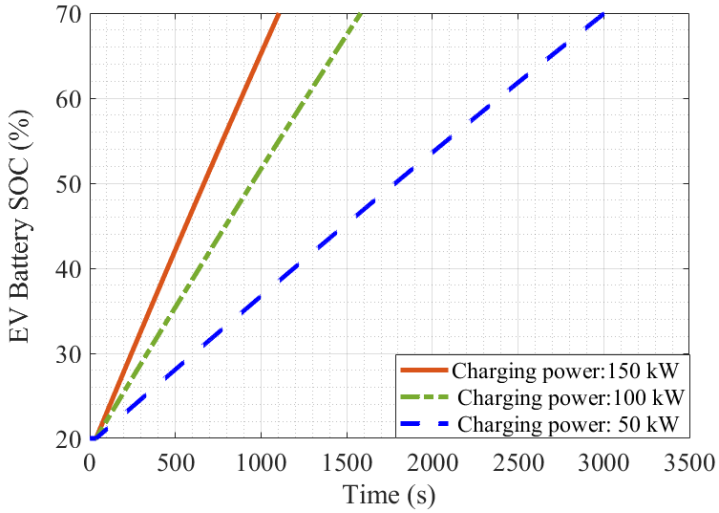


Figure 3-2. EV battery SOC change with different charging power

Table 3-2 shows the estimated efficiency and power density of the required electrical components used in the DCFC station models. Most power converters use a single average efficiency since they will often run at a single operating point. However, since the electrolyzer and

the battery operate at varying operating points, the associated power converters efficiencies are modeled as shown in Figure. 3-3 [113]. Due to the lack of available data, the power density of the diode bridge rectifier, a Vienna rectifier in this case, is estimated at 2450 kW/m^3.

Table 3-2: Specifications of Electrical Components

Component	Average Efficiency (%)	Power Density (kW/m^3)
Transformer [114]	98%	242
Diode Bridge (Vienna) Rectifier [115]	98%	2450
Active AC/DC Converter [116]	98%	2450
Non-isolated DC/DC Converter [113]	98%	9000
Isolated DC/DC Converter [117]	95%	1330

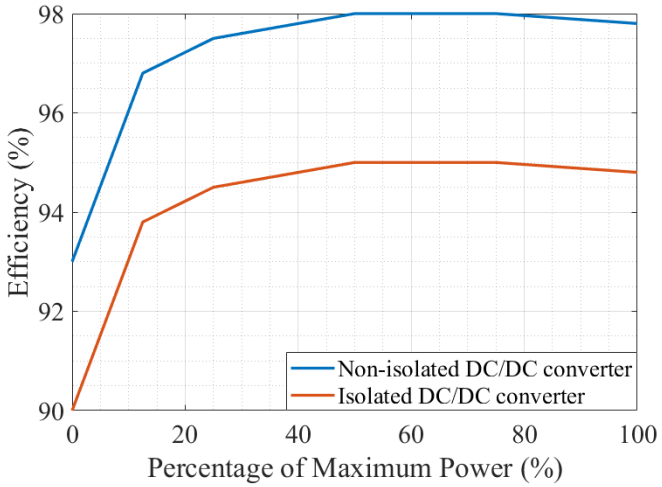


Figure 3-3. Efficiency of electrolyzer-connected non-isolated DC/DC converter [113] and estimated efficiency of battery-connected isolated DC/DC converter

3.2 Analysis of Efficiency, Cost, and Volume

3.2.1 DCFC with BESS

The Simulink model for the DCFC station with BESS is based on the architecture in Figure 2-5(b). The block diagram of the Simulink model is shown in Figure. 3-4. The storage battery is modelled based on the AKASOL 15 AKM 46 NANO NMC battery [81], as shown in Table 3-3. The charging and discharging resistance of the storage system are based on the data gathered from the company. The battery is allowed to charge up to 95% SOC and discharge down to 20% SOC to protect the health of the battery by limiting the depth of discharge (DOD). The cycle lifetime is

estimated at 7000 cycles at 80% DOD [81], and the calendar life is estimated at 12 years [42]. Moreover, the battery never exceeds its maximum C-rate during charging or discharging.

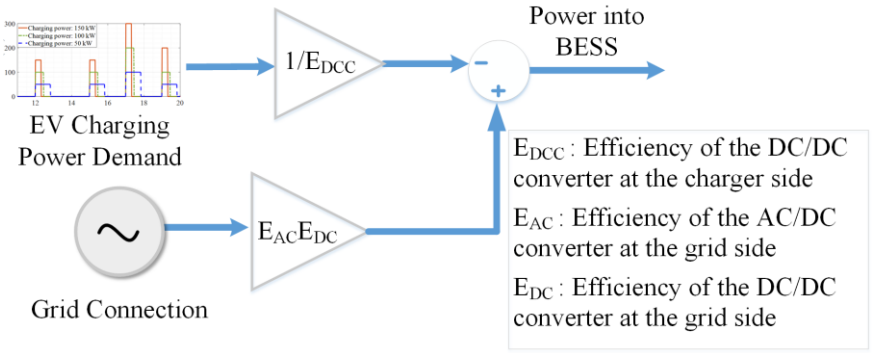


Figure 3-4. Block diagram of the Simulink model for the DCFC with BESS

Table 3-3: Specification of Stationary BESS [81]

Parameter	Value
Module Nominal Energy	30.6 kWh
Module Nominal Voltage	666 V
Module Capacity	46 Ah
C-rate	2.5
Energy Density	122.18 kWh/m^3

The minimum BESS energy requirement is found by adjusting the battery size in small steps for each daily EV charging scenario in Figure. 3-1, such that the SOC limits and C-rate limits are not exceeded. BESS energy is increased by increasing the number of battery modules from Table 3-3 in parallel, where non-integer numbers of parallel modules are accepted so that the minimum energy requirement can be found regardless of the selected battery module size in Table 3-3. The BESS simulation results are shown in Table 3-4. The system volume is found by summing the volumes of the battery and the power electronic converters calculated from battery energy density (Table 3-3) and converter power densities (Table 3-2). In addition to the energy requirement and system volume, average daily efficiency and the number of equivalent full cycles (EFC) per day is also calculated for use in the cost analysis. The EFC is calculated as (3.3), where battery capacity is adjusted to 80% because the available battery lifetime data is for 80% DOD cycles. The

efficiency results are calculated considering efficiencies of all associated power electronics and battery internal losses. The results show that the BESS has high efficiency, as expected, and that the system efficiency decreases as the charging rate increases due to higher I^2R battery internal losses.

$$EFC = \frac{TotalEnergyThroughput}{BatteryCapacity \times 0.8} \tag{3.3}$$

Table 3-4: Summary of BESS Simulation Results

DCFC Station Size	Grid Connection (kW)	EV Charging Rate (kW)	BESS Requirement (kWh)	System Efficiency (%)	System Volume (m^3)	EFC/day
Small	15	50	42.22	87.36	0.40	0.94
		100	52.63	86.37	0.52	0.93
		150	57.83	85.45	0.60	0.92
Medium	15	50	141.98	87.97	1.25	1.51
		100	163.10	87.49	1.50	1.55
		150	177.48	87.08	1.70	1.53
	50	50	63.95	87.99	0.66	1.24
		100	94.25	87.26	0.98	1.94
		150	108.02	86.59	1.17	2.07
Large	150	50	111.38	92.51	1.27	1.79
		100	186.97	87.44	2.08	2.25
		150	260.10	87.29	2.87	2.59

3.2.2 DCFC with FESS

For the FESS, the architecture from Figure. 2-6(c) is used as it has an active front end for bidirectional power flow. The block diagram of the Simulink model is shown in Figure. 3-5. The flywheel model is based on the Beacon Power flywheel system rated for 100 kW and 25 kWh from Table 2-2. The efficiency of flywheel system with integrated power electronics is 90% [51]. The self-discharge (spinning loss) with respect to speed for one flywheel module is presented in Figure. 3-6, as per communication with Beacon Power. The SOC of the flywheel is calculated using (3.4) where $E_{capacity}$ is the flywheel maximum usable energy capacity and $P_{flywheel}$ is the power into the flywheel. The flywheel operates between 16,000 rpm (ω_{max}) and 8,000 rpm (ω_{min}); therefore,

flywheel speed at a certain SOC can be found using (3.5). The flywheel system operates from 0% SOC to 100% SOC, where 0% SOC corresponds to 8,000 rpm.

$$SOC_{flywheel} = SOC_{init} + \frac{1}{E_{capacity} \times 3600} \int_{t_{start}}^{t_{end}} P_{flywheel}\, dt \tag{3.4}$$

$$\omega_{flywheel} = \sqrt{SOC \times (\omega^2{}_{\max} - \omega^2{}_{\min}) + \omega^2{}_{\min}} \tag{3.5}$$

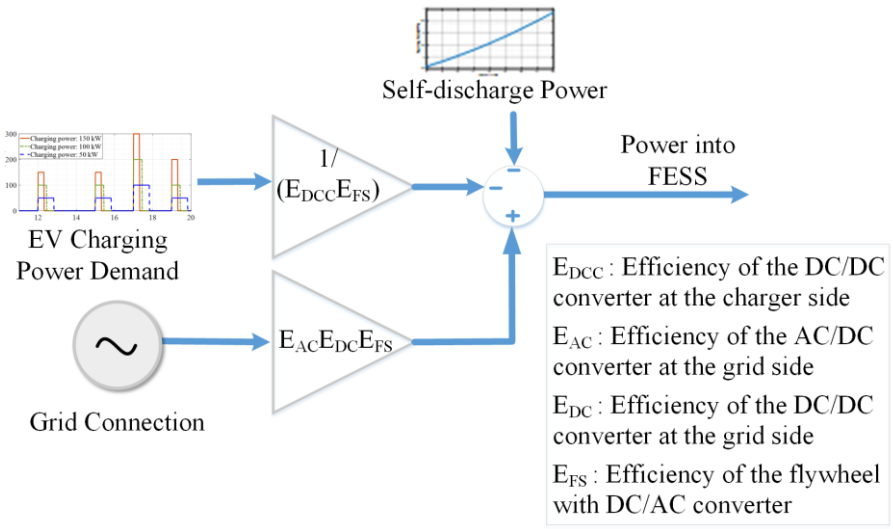


Figure 3-5. Block diagram of the Simulink model for the DCFC with FESS

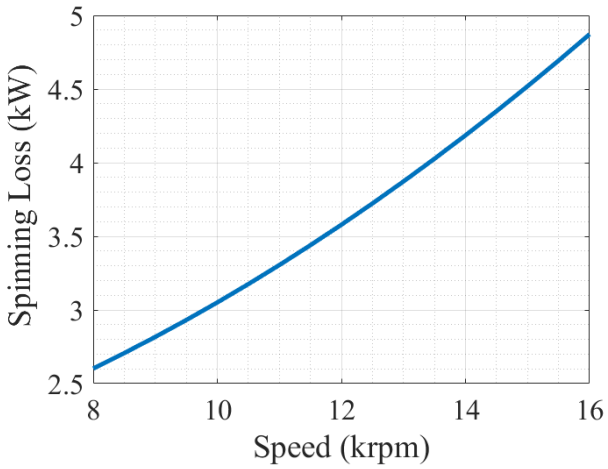


Figure 3-6. Self-discharge (spinning losses) of the FESS with respect to rotational speed

The minimum FESS energy capacity is found such that it satisfies each EV charging profile in Figure. 3-1. FESS modules are connected in parallel to model higher energy capacities. Table

3-5 shows the flywheel simulation results. The FESS system volume is calculated by summing the flywheel volume (using energy density from Table 2-2) and the associated converter power densities from Table 3-2. The high spinning losses make the FESS unsuitable for the small DCFC station due to low efficiency: the flywheel is waiting charged most of the day for the EV charging event to begin. For the medium station, two control strategies are considered: (I) same as for the small station, the FESS is kept at high SOC to be ready for any EV charge event (Figure. 3-7), and (II) the flywheel is controlled to a lower SOC during less busy times of the day, and only charged to high SOC during the predicted busy charging times of the day (Figure. 3-8). Since spinning losses increase at higher speeds, and speeds are higher at higher SOC, Control Strategy II increases system efficiency by a few percentage points compared to Control Strategy I. Also, for either control strategy, system efficiency is highest at lower EV charge rates because most EV charging power can come directly from the grid with less cycling of the FESS. Furthermore, the simulation results also show that the FESS is not suitable for the medium station with 15 kW grid connection (due to high spinning losses) and is not suitable alone for the large station as the energy storage requirement indicates an infeasible number of flywheel modules. Thus, the hybrid flywheel-battery investigation will focus on the large DCFC station.

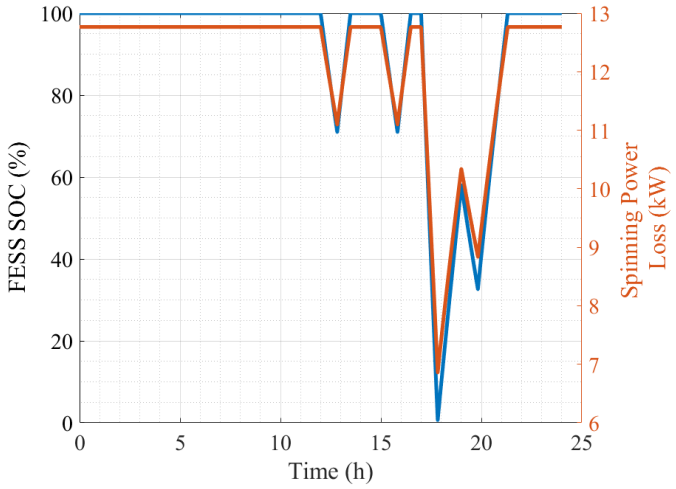


Figure 3-7. FESS SOC and spinning losses for Control Strategy I with EV charging rate of 50 kW

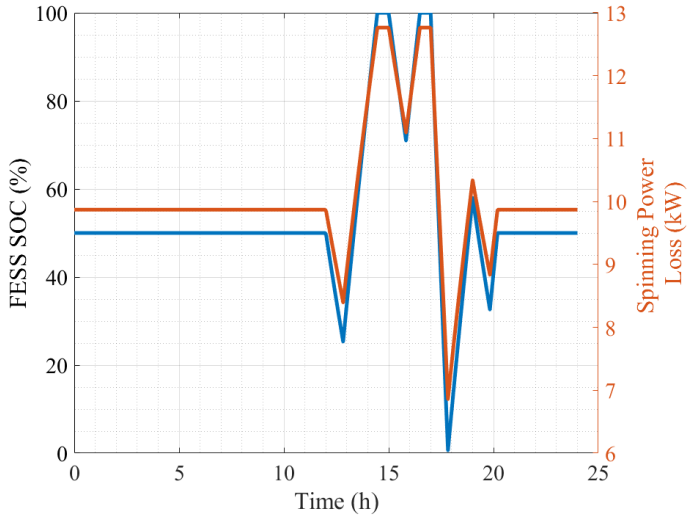


Figure 3-8. FESS SOC and spinning losses for Control Strategy II with EV charging rate of 50 kW

Table 3-5: Summary of FESS Simulation Results

DCFC Station Size	Grid Connection (kW)	Control Strategy	EV Charging Rate (kW)	FESS Energy Requirement (kWh)	FESS Power Requirement (kW)	System Efficiency (%)	System Volume (m^3)	EFC/day
Small	15	I	50	42.00	53.07	14.78%	2.41	1.25
			100	47.50	112.87	13.98%	2.75	1.25
			150	50.25	172.01	13.87%	2.95	1.25
Medium	50	I	50	63.75	80.57	33.40%	3.71	2.00
			100	85.00	202.65	28.51%	4.97	2.54
			150	94.50	321.89	27.33%	5.58	2.64
		II	50	63.75	80.57	38.52%	3.71	2.00
			100	85.00	202.65	30.78%	4.97	2.54
			150	94.50	321.89	28.51%	5.58	2.64

3.2.3 DCFC with Hydrogen Storage

The architecture in Figure. 2-7(c) is considered in this analysis, as it has an active front end and a low number of conversion stages. The block diagram of the Simulink model is shown in Figure. 3-9. The fuel cell system is modeled with the efficiency curve in Figure. 3-10 [63] and power density of 162 kW/m^3 [92]. An alkaline electrolyzer is assumed, with 94%, 90.5%, and 85% efficiency at 25%, 50%, and 100% load, respectively [61]. The electrolyzer hydrogen production rate is estimated at 0.022 kg H_2/hour per kW electrical power [61], where H_2 is produced at 35 bar. The electrolyzer volume is estimated at 0.018 m^3/kW electrical power [61]. The compressor

volume and power use is modeled from Burkhardt Compression MD2.5-V [118] with 25% added to both metrics to estimate a 700 bar system. Thus, the modeled compressor can process 3.4 kg of H_2/hour at 700 bar with an estimated volume of 5.5 m^3 while consuming 15 kW from a secondary grid connection, which is included in the efficiency calculation. Therefore, the volume of the required compressor to process hydrogen produced by the electrolyzer per kW grid connection at 100% load is 0.036 m^3. The 700 bar hydrogen tank density is 800 kWh/m^3 [60].

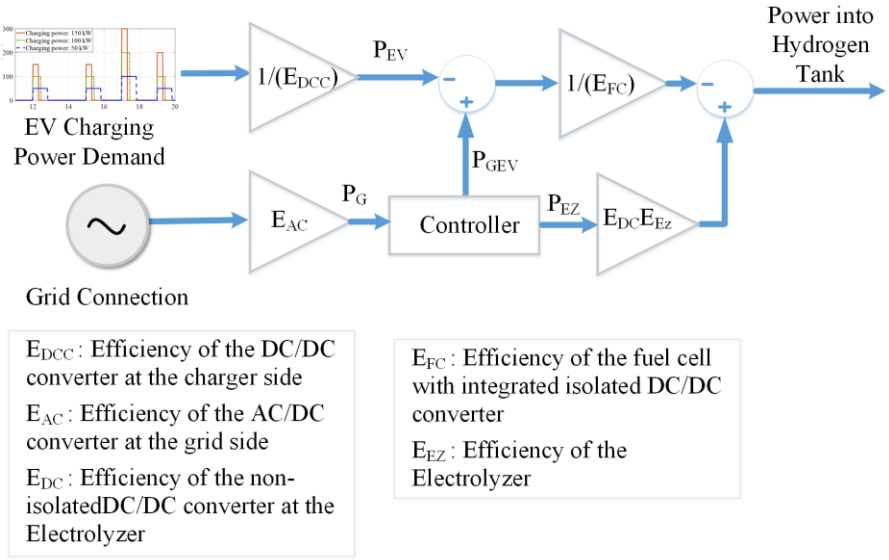


Figure 3-9. Block diagram of the Simulink model for the DCFC with hydrogen storage

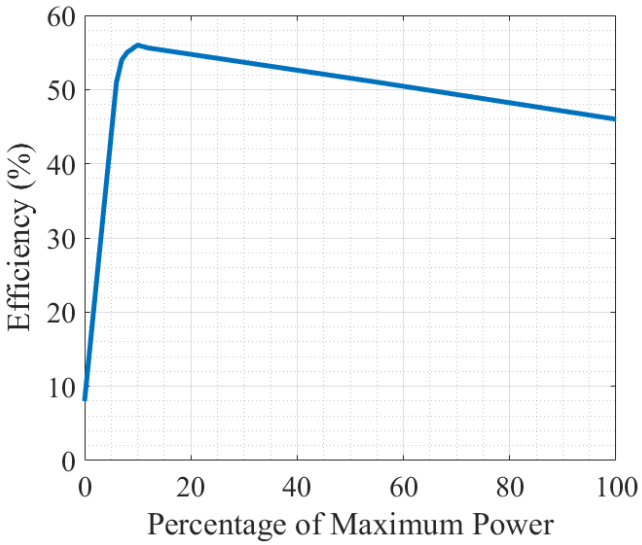


Figure 3-10. Fuel cell system efficiency at different loading condition [63]

The fuel cell is sized based on the maximum ESS power requirement, which is the difference between the maximum EV charging power and the grid connection power level. Then, the electrolyzer and compressor sizes are chosen to use the full grid connection power, except for the 150 kW grid connection case, where a 75 kW power rating is found to suffice for the considered EV charging scenarios. Then, the minimum size of the hydrogen storage tank is found by the simulation such that it can supply the required energy. The fuel cell, electrolyzer, compressor, and hydrogen tank volumes are then found using the densities in the preceding paragraph and summed with the power electronic converter volumes to obtain the system volume. Table 3-6 summarizes the simulation results. Similar to the FESS case, the medium DCFC with hydrogen storage cannot supply the required energy with a 15 kW grid connection due to low efficiency. At lower EV charging rates, the system efficiency is notably higher because less energy must be processed in the electrolyzer-fuel cell path, and more of the EV energy can come straight from the grid. Also, it was found that for the large station, the volume and cost can be optimized by using a smaller electrolyzer and compressor than the full 150 kW available from the grid – in this case a 75 kW electrolyzer was sufficient to keep the hydrogen tank adequately filled for the daily charging profile. Furthermore, based on the fuel cell efficiency curve, it is clear that fuel cell efficiency could be increased by up to 10% if a larger fuel cell was used, so that it could run at much less than maximum power. However, this would have negative cost implications as the fuel cell would be oversized for the expected load.

3.2.4 DCFC with Hybrid Storage

The architecture in Figure. 2-8(a) is considered in this analysis, with active front end and isolated DC/DC converter at the grid side. The block diagram of the Simulink model is shown in Figure. 3-11. The battery-flywheel hybrid system is only simulated for the large DCFC with an

EV charging rate of 150 kW, because the most demanding charging scenario would likely benefit the most from a hybrid ESS. Although many sizing and control strategies are possible, this analysis develops a strategy to minimize battery cycling, and thus aging, as this is a key benefit that can be exploited when combining a battery and flywheel, due to the flywheel high power capability and high cycle capability. Since battery calendar life is estimated at 12 years, the control goal is to extend battery cycle life to 12 years, so it does not need to be replaced prematurely due to high cycling.

Table 3-6: Summary of Hydrogen ESS Simulation Results

DCFC Station Size	Grid Connection (kW)	EV Charging Rate (kW)	Hydrogen Storage Requirement (m^3) (Equivalent Energy (kWh))	Fuel Cell Power Requirement (kW)	Maximum Hydrogen Production Rate by Electrolyzer (kg/hour)	System Efficiency (%)	System Volume (m^3)
Small	15	50	0.086 (69 kWh)	37.93	0.33	39.49	1.19
		100	0.106 (85 kWh)	90.56	0.33	35.52	1.58
		150	0.116 (93 kWh)	143.19	0.33	34.38	1.95
Medium	50	50	0.126 (101 kWh)	56.26	1.10	63.50	3.34
		100	0.190 (152 kWh)	161.53	1.10	45.24	4.13
		150	0.216 (173 kWh)	266.79	1.10	41.05	4.88
Large	150	50	0.256 (205 kWh)	116.16	1.65	73.46	5.38
		100	0.625 (500 kWh)	379.32	1.65	54.00	7.56
		150	0.900 (720 kWh)	642.47	1.65	47.84	9.65

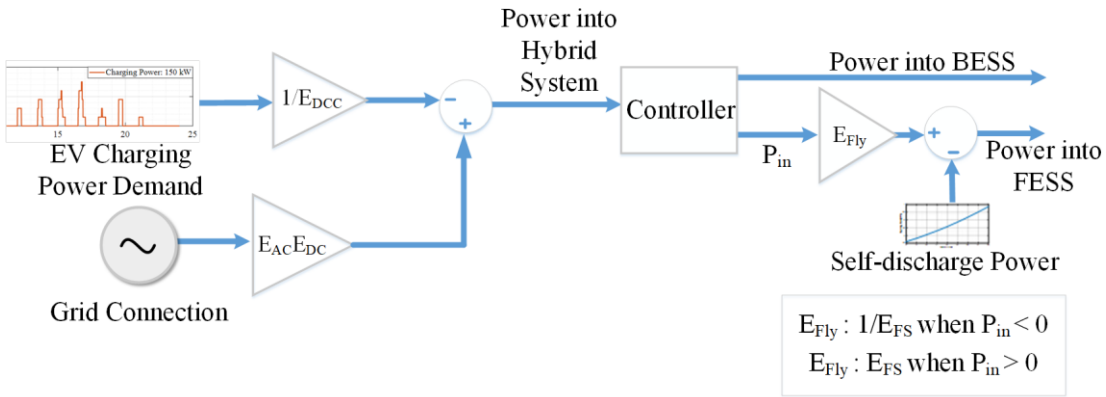


Figure 3-11. Block diagram of the Simulink model for the DCFC with hybrid storage system

It is calculated that the battery can last for 12 years if its EFC is limited to 1.6 cycles/day. To achieve this goal, a control strategy is developed such that the BESS supplies 55% of the storage power demand when this demand is less than the BESS's maximum power rating of 2.5 C. This

allows the FESS to deliver almost half of the required power when the power demand is low. When the FESS depletes to its minimum SOC, the BESS supplies all the power. When the power demand is greater than 2.5 C, the BESS supplies power at 2.25 C rate and the FESS provides the rest until it is depleted.

Choosing the sizes of components in a hybrid system has a complicated interrelation with the selected control strategy. In this case, the BESS size is selected to be the same as that from the BESS-only case (260.1 kWh), so that the flywheel can be used to reduce battery cycling (with a calculated FESS size requirement of 57.5 kWh). It should be noted that other control and sizing strategies were investigated, but when the battery is made smaller, the flywheel system must be larger, and total volume and efficiency were generally worse than the selected case described here. For the selected case, system efficiency over one day is 64.7% and the system volume is found to be 6.12 m^3. Figure. 3-12 shows the power and SOC profiles of the battery and flywheel for the proposed control strategy.

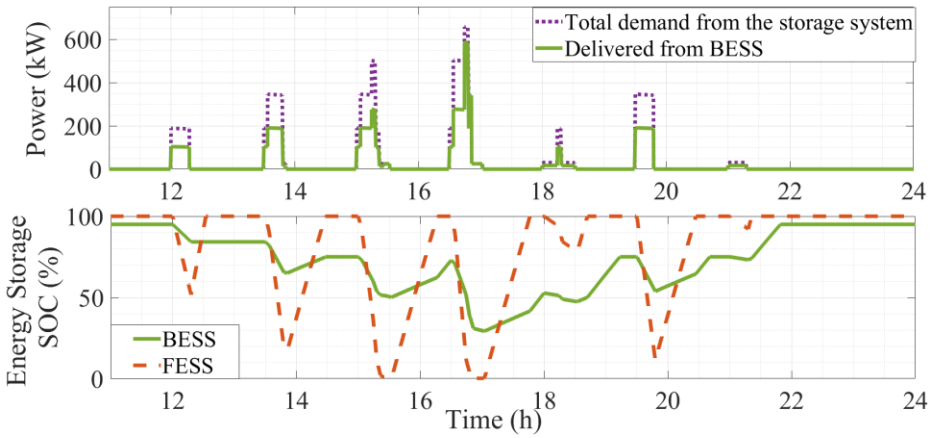


Figure 3-12. Power delivered by BESS and daily charging and discharging cycle of BESS and FESS

3.2.5 Comparison of ESSs in DCFC

The simulations provide important results on ESS sizing, efficiency, volume, and EFC. However, to complete the analysis, cost must also be considered. Costs have been estimated from

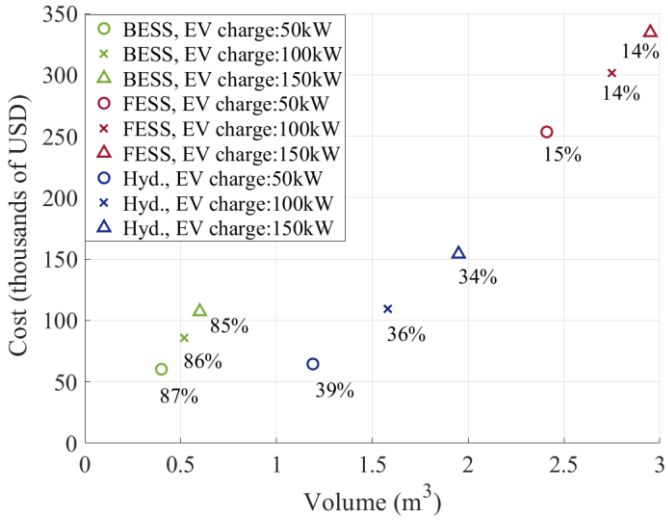
a variety of sources, as shown in Table 3-7, and include initial equipment costs and installation. The cost is estimated for a 20-year time frame. The ESS component lifetimes are considered as noted in Table 3-7 based on the simulated EFC in each DCFC scenario.

Table 3-7: ESS Cost Estimates (Capital and Installation)

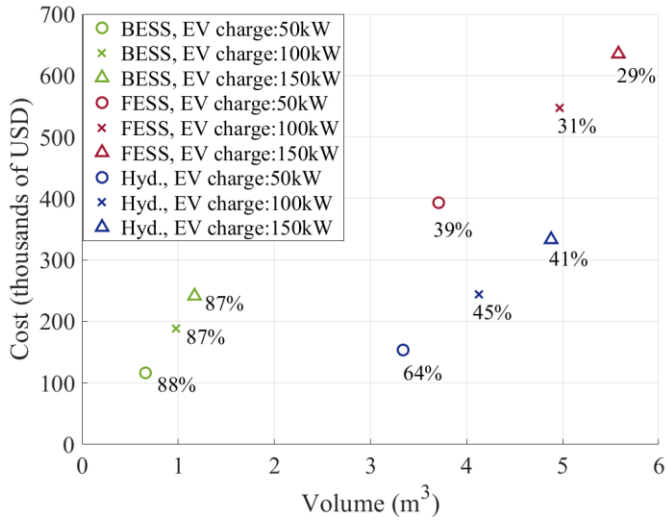
Component	Component Details	Cost (USD)	Source	Notes
EV Charger	Isolated DC/DC converter (EV port)	$345/kW	[119]	Based on whole charger cost, assume 40% is removed for front end. Small station has 1 port, medium has 2, large has 5.
Battery	Battery packs	$390/kWh	[25]	Calendar life 12 years. Attainable lifetime in each scenario calculated based on EFC. Per-year cost multiplied by 20.
	Balance of plant	$615/kW	[25]	Includes power converters, etc.
	Installation	$150/kWh	[25]	
Flywheel	Flywheel module (by power)	$1125/kW	Discussions with Beacon Power, [May 19, 2020]	Range is 650 – 1,600 $/kW. This analysis assumes the middle value. Lifetime is assumed 100,000 cycles with 80% DOD. Power electronics included.
	Flywheel module (by energy)	$4500/kWh		Based on modeling a 100 kW/25 kWh flywheel module.
	Installation	$281/kW		Range is 20% - 30% of equipment cost. This analysis assumes the middle value.
Hydrogen	Electrolyzer	$700/kW	[120]	Lifetime 10 years. Includes AC/DC converter and installation cost.
	Compressor	$275/kW	[64]	Lifetime 15 years. $/kW grid connection.
	Tank	$15/kWh	[60]	Lifetime 20 years
	Fuel cell	$260/kW	[64]	Lifetime 10 years. Includes DC/DC converter.

The results are shown in Figure. 3-13 for each station size. FESSs are not suitable for small and medium DCFC stations due to high cost. The main advantage of FESS is high power capability, and for the scenarios considered here, more energy is needed such that the FESS power is not utilized to its fullest. Thus, FESSs would be best considered only for DCFC stations that will be needing high power capability and high life cycles to provide services to the grid, which will improve the economic payback compared to the DCFC-only scenarios considered here. The hybrid FESS could be feasible for a large station that is also providing grid services. Hydrogen storage has higher volume and lower efficiency than BESS in all three metrics considered, however, the cost is only slightly higher than that of the BESS. Thus, hydrogen storage would be best considered only for DCFC stations that must also provide hydrogen for refuelling fuel cell

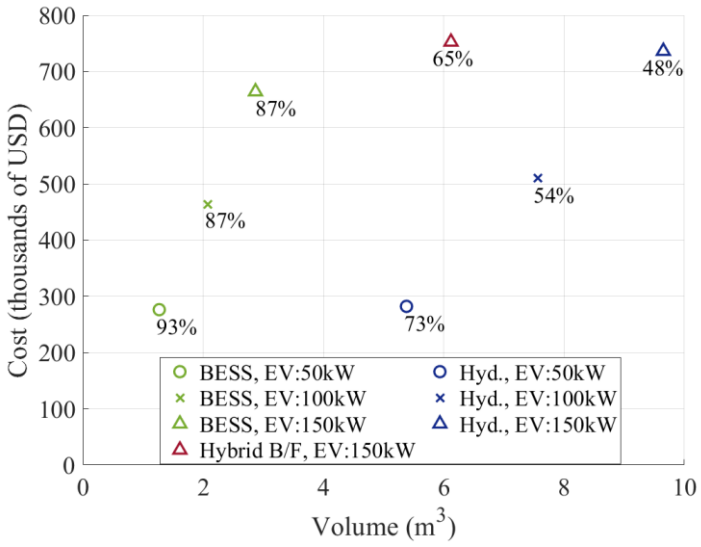
vehicles [121], such as passenger vehicles or heavy duty transportation that requires high on-board energy storage for long distance trucking – however, the cost premium compared to batteries is small. The high efficiency of the battery options will translate into lower operating costs due to less wasted electricity. Though the battery packs may have to be replaced one or two times during the 20 year life-span of the station depending on the EFC, the battery costs (which include pack replacement costs) are still lowest among the ESS options. Thus, as the BESS is the most promising ESS type for stations that provide only DCFC, the next section will perform a detailed technical analysis of BESS architectures.



(a)



(b)



(c)

Figure 3-13. Overall ESS type comparison with efficiency overlaid for (a) small station with 15 kW grid connection, (b) medium station with 50 kW grid connection, (c) large station with 150 kW grid connection.

3.3 Comparison of DCFC Architectures with BESSs

This section compares the technical details of different BESS architectures for a large DCFC station with the load profiles in Figure. 3-1(c), with a focus on efficiency and system volume. The five topologies considered in Figures. 2-4 and 2-5 are simulated using the power electronic average efficiencies in Table 3-2 for four DCFC large station scenarios: 50 kW EV charging rate with 100 kW and 150 kW grid connections, and 150 kW EV charging rate with 100 kW and 150 kW grid connections. The BESS energy requirement and volume are calculated using the same procedure as in the previous section. The architectures in Figure. 2-5(a) and 2-5(b) yield the same efficiency and volume results, so they are listed as one architecture going forward. For the isolated DC/DC converter at the battery terminals, the efficiency curve in Figure. 3-3 is used since the power rate through this converter fluctuates over the day.

Figure. 3-14 shows the 50 kW EV charging rate results for both 100 kW (circle markers) and 150 kW (triangle markers) grid connections. The green markers represent the architecture in Figure. 2-4(a), which uses a transformer for isolation between the grid and the battery. This yields

high efficiency but also high volume due to the bulky 60 Hz transformer. However, the architecture in Figure. 2-4(c), which places an isolated DC/DC converter between the battery and the high voltage bus, has the highest efficiency when the grid connection power level is high (i.e., 150 kW). This is because during vehicle charging, power for about three vehicles can come directly from the grid in this scenario, meaning most charging power over the day comes straight from the grid and does not cycle through the battery. Thus, the high efficiency path from the grid to the EV in the Figure. 2-4(c) architecture is well-suited to this DCFC scenario. However, when more use of the energy storage is required, such as if the grid connection is reduced to 100 kW, the architecture in Figure. 2-4(c) has worse efficiency because the path in and out of the battery has lower efficiency compared to all other architectures. For both grid connection levels, the two-stage architectures in Figures. 2-5(a) and Figures. 2-5(b) offer high efficiency and low volume, due to a decreased number of converters.

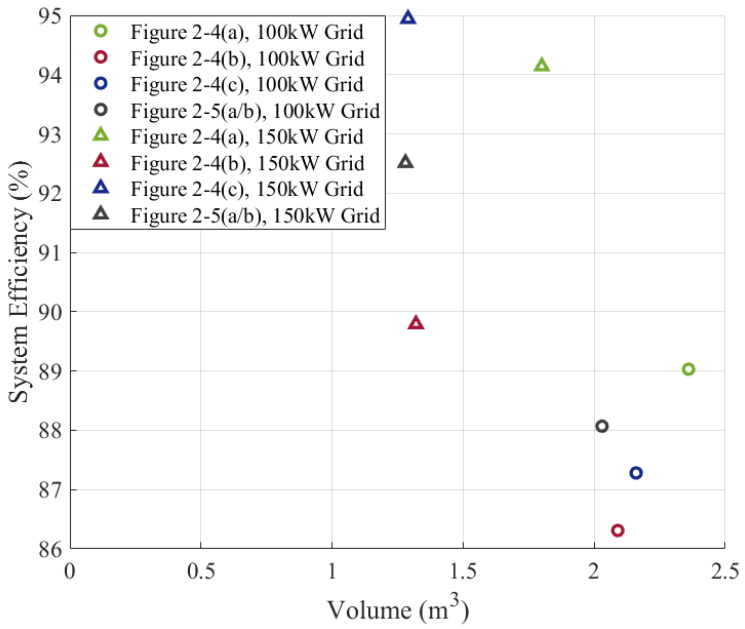


Figure 3-14. Efficiency vs. volume for the BESS architectures for 50 kW EV charging at large station

Figure. 3-15 shows similar results for the 150 kW EV charging rate at a large DCFC station. Again, the transformer option (green) gives the highest efficiency but also high volume.

Interestingly, the architecture in Figure. 2-4(c) has the lowest efficiency for both grid connection levels because for the higher EV charging rate, much more energy must be cycled in and out of the battery, generating losses in the isolated DC/DC converter connected to the battery during each charge and discharge event. Thus, for the 150 kW EV charging rate, it is most important to have a high-efficiency path from the storage battery to the EV, since this is the path most charging energy follows. Again, the architectures in Figures. 2-5(a) and 2-5(b) offer a good balance of efficiency and volume for all considered cases. For all four DCFC scenarios, the volume of the BESS increases as the grid connection level decreases, since more energy storage is required to meet the EV charging needs.

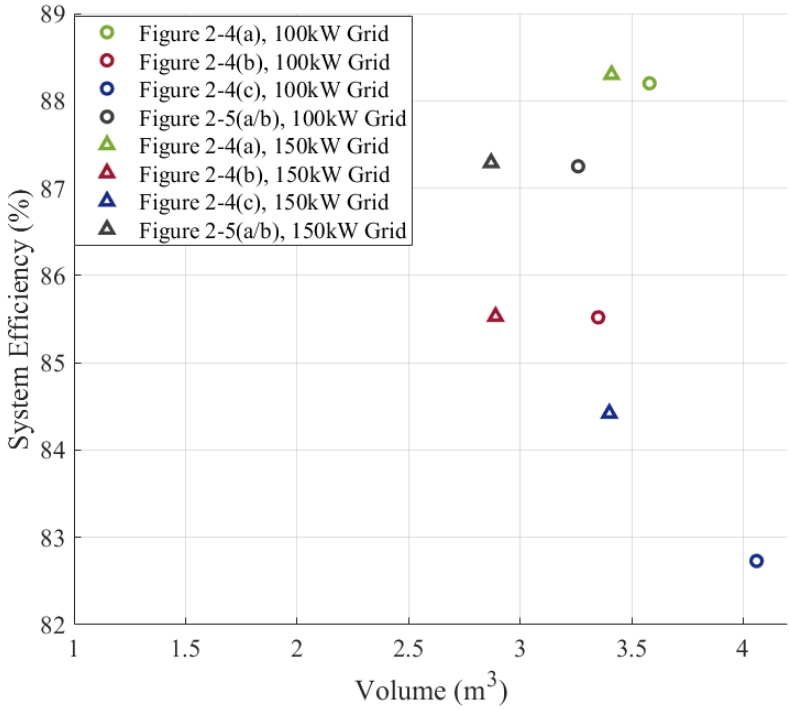


Figure 3-15. Efficiency vs. volume for the BESS architectures for 150 kW EV charging at large station

Figure. 3-16 shows the battery energy requirements for each scenario and architecture. While the average kWh requirement changes clearly between the four DCFC scenarios, there are also differences between the architectures for a given scenario, which relate to the efficiencies simulated for each architecture. For example, for 150 kW EV charging and 100 kW grid

connection, Figure. 2-4(c) requires an 11.6% larger battery than the architecture in Figure. 2-5(a) because of its lower efficiency in this scenario. Thus, the volume of the system is also partially related to the efficiency of the system.

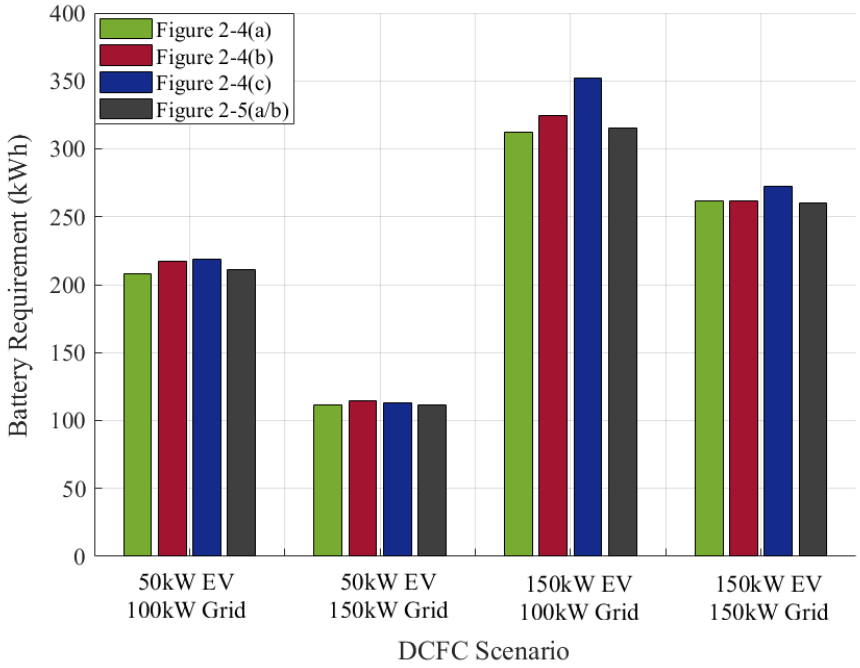


Figure 3-16. Battery energy requirement for BESS architectures at large DCFC station

3.4 Summary

This chapter has provided a comprehensive analysis of efficiency, volume, and cost for a small, medium, and large DCFC station. To do such, DCFC stations with ESSs are modelled in MATLAB/Simulink. The results show that flywheels would be best considered if high power grid services will be also provided by the energy storage, and hydrogen storage would be best considered only if refueling of fuel cell vehicles is also required. Otherwise, batteries generally exhibit the lowest cost, lowest volume, and highest efficiency. A comparison of battery architectures shows that the optimal architecture is highly dependent on the grid connection power and the EV charging power. However, it should be noted that the results presented in this chapter are greatly dependent on the selected components and the assumptions made in this study.

Chapter 4

Active Front End Converter Based DCFC

4.1 Background

The increasing connections of power electronic converters to the grid for photovoltaics, wind generation, and electric vehicle (EV) fast-charging stations are posing new power quality challenges. One such power quality problem is the distortion of the drawn or injected current waveform from or to the grid [122], which is mainly caused by the rectifier/inverter circuit [123]. DCFC stations use active front end rectifiers (bidirectional AC-DC converters) as in the architecture shown in Figure. 2-5(b) since it is advantageous for DCFCs to provide ancillary services to the grid such as frequency regulation and reactive power support [124] along with having inherent power factor correction capability. Voltage source converters (VSC) are a common choice for the active front end in DCFC stations [125]. The current drawn from the grid in a VSC-based active front end gets distorted mainly in two ways: due to modulation techniques and distorted background voltage.

Various modulation techniques are available in the literature such as sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM). Each modulation technique produces different current emissions depending on switching frequency, modulation index, blanking time, and switching sequences [126]. One potential solution is to use more complex VSC topologies [127], e.g., multi-level converters, which use the above mentioned modulation techniques to reduce the current distortion with increasing numbers of levels. However, the increasing complexity of these converters with many levels makes them non-ideal for some applications. For converters with fewer levels (e.g., three or four), further filtering is required. High order passive filters (e.g. LCL) are usually adopted to attenuate the harmonic current emission resulting from the switching in a standard two-level VSC and for low levels of multi-level converters [128].

The background voltage harmonics, however, result in current harmonics depending on the frequency dependent input impedance of the converter system. Moreover, additional current flows at the frequencies different from the background voltage harmonic orders. These additional current harmonics originate from the cross coupling of positive and negative sequence harmonic components due to the perturbation in tracked phase angle with a Phase Locked Loop (PLL) in a polluted grid [129]. For instance, 5^{th} order (negative sequence) background voltage harmonic produces an additional 7^{th} order current harmonic (positive sequence) and vice versa. These harmonics are low order harmonics as the PLL is designed to track the system frequency, i.e., the low bandwidth of PLL system results in attenuation of high order frequency components. Even though LCL filters do help reduce the current emission from background voltage harmonics by increasing the equivalent input impedance of the converter system, these high order filters become susceptible to the distorted background voltage due to resonance [130]. Therefore, standard industry practice is to design VSC systems with background voltage harmonic rejection capability, usually with the help of VSC controllers, e.g., increased inner current control loop gain, grid voltage feedforward, and selective harmonic compensator (HC) with a proportional resonant (PR) regulator [128]. These methods are effective in decreasing the current flow at the frequencies of the distorted background voltage. However, these background voltage harmonic rejection techniques are not capable of decreasing the current emission at the coupled frequency (e.g., 7^{th} order current harmonic when the grid voltage is polluted with only 5^{th} order harmonic).

This chapter explains why the standard industry practices used to reduce current emission originating from background voltage harmonics is not only ineffective in reducing the emission at the coupled frequency, but also responsible for increasing the emission in certain cases, for instance, with increasing current loop gain, or implementing a HC with PR. To do such, a two-

level VSC active front end is modelled, which helps explain the propagation of background voltage harmonics in the VSC system along with harmonic elimination techniques used in industry and their impact on current emission. Finally, simulation results are presented, which verify the theoretical explanations, and offers practical solutions.

4.2 Modeling of an AFE

A VSC based AFE is comprised of four different blocks: Phase Locked Loop (PLL), outer control loop, inner current control loop and Pulse Width Modulation (PWM) unit. A VSC-AFE with simplified DC bus is presented in Figure. 4-1 where the converter is connected to the AC grid via an LCL filter at the point of common coupling (PCC). Moreover, a two-level VSC as shown in Figure. 4-2 is considered for this analysis.

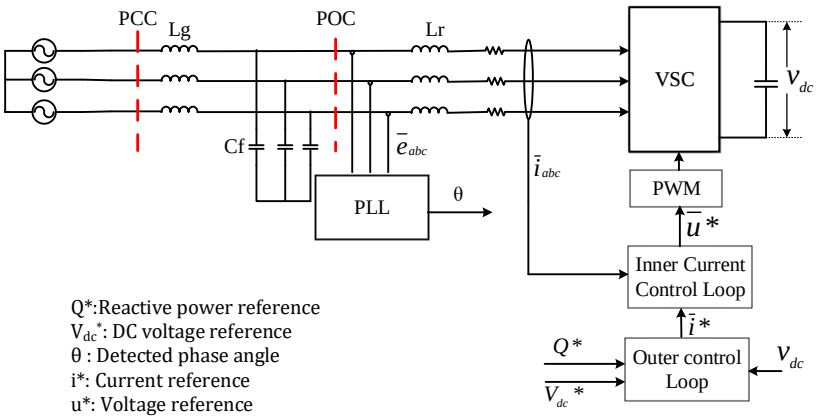


Figure 4-1. VSC-AFE with simplified DC bus

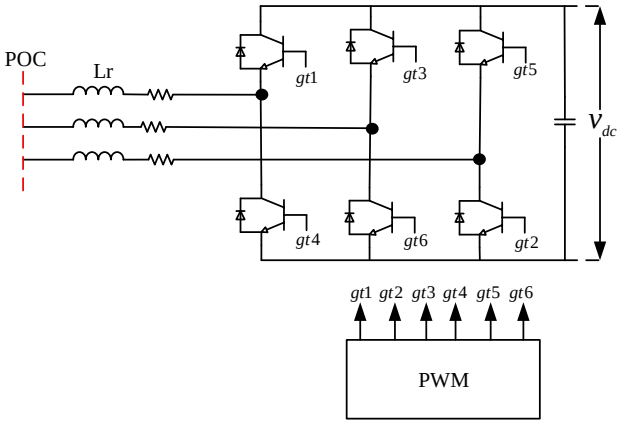


Figure 4-2. Two-level VSC with gating signals

The PLL is used for grid synchronization by tracking the voltage phase angle at the point of common coupling (POC). A PLL block diagram is shown in Figure. 4-3, where ω_1 is the fundamental angular frequency and θ is the phase angle. A PLL is usually implemented in synchronous reference frame, i.e., $dq0$ frame, and the q-axis voltage component, E_q is regulated to zero with a PI controller ($\mathrm{H_{PI}(s)}$). This makes the d-axis of the synchronous reference frame aligned with the complex voltage space vector at the POC, i.e., the complex voltage space vector becomes a constant DC quantity in the synchronous reference frame.

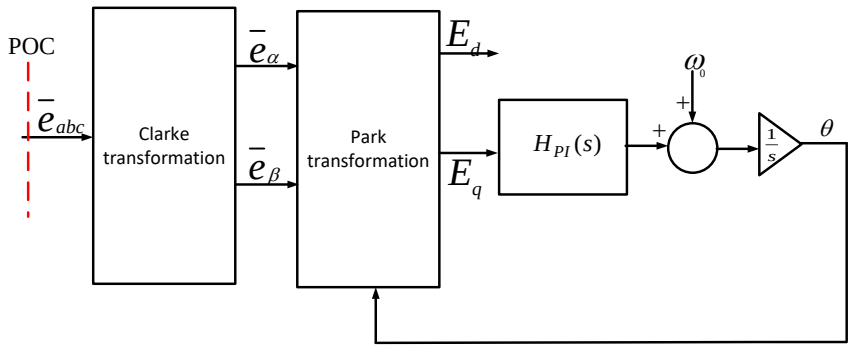


Figure 4-3. Phase Locked Loop block diagram

The current flow into a VSC system from the grid is controlled by producing the appropriate voltage at the converter terminal. Therefore, the converter system from Figure. 4-2 can be represented as a single-phase equivalent circuit as in Figure. 4-4 looking from the POC into the converter. This representation of a VSC system is valid for balanced three-phase operation and constant DC bus voltage. Equation (4.1) can be written using Kirchhoff's voltage law considering the current direction being from the grid to the converter (i.e., rectification). The inner current control loop is designed based on this equation to produce converter terminal voltage, $\bar{u}$. It is a common practice to design the current control loop in synchronous reference (i.e., *dq0*) frame [131]. However, the inner current control loop is designed in stationary (i.e., $\alpha\beta0$) frame with Proportional Resonant (PR) controllers for this analysis. This is due to the fact that the performance

of PI controllers used in synchronous reference frame have some limitations such as instability due to feedforward voltage, multiple frame transformation stages, etc., as explained in [132]. The transfer function of an ideal PR controller is given in (4.2) where the first term is the proportional gain, and the second term is a generalized integrator (GI). GI integrates a sinusoidal input without introducing any phase-delay [131] as shown in Figure. 4-5. Proportional gain, K_p is responsible for determining the dynamics of the system in terms of bandwidth, phase and gain margin [132]. On the other hand, the GI term provides an infinite gain at the resonance frequency, ω. This infinite gain can instigate instability in the power system. Furthermore, the frequency of the power system is not constant, but fluctuates within a certain limit, and the PR controller in (4.2) is sensitive to such frequency changes. To avoid such instability and sensitivity issue, the PR controller in (4.3) can be used instead [132]. The PR controller in (4.3) has finite but high enough gain at ω and the bandwidth can be adjusted by selecting a proper value of ω_c to reduce the sensitivity of the grid frequency change. In practice, ω_c is selected between 5 to 15 rad/s [133]. The magnitude bode plots of (4.2) and (4.3) are shown in Figure. 4-6 for $K_i = 10, \omega = 100\pi, \omega_c = 6$. Finally, an inner current control loop in stationary frame is shown in Figure. 4-7 where $\bar{\imath}^*_{\alpha\beta}$ is the reference current signal, PR controller is based on (4.3), $G_{ff}(s)$ is a low-pass filter or constant gain, and $\bar{u}^*_{\alpha\beta}$ is the voltage reference signal to the PWM unit.

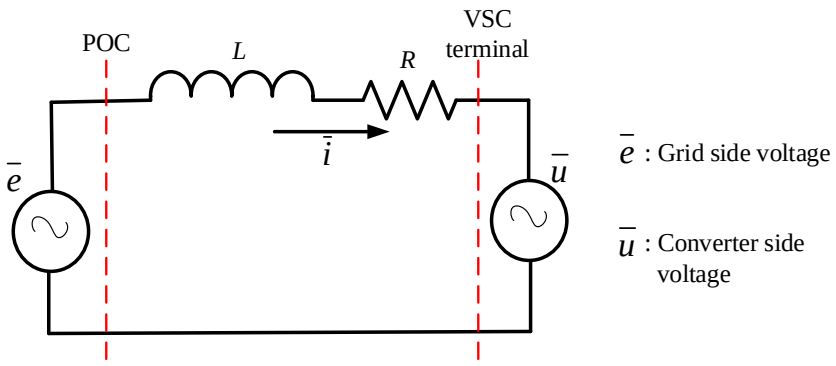


Figure 4-4. Single-phase equivalent circuit of the convert system from POC

$$\bar{u} = \bar{e} - R\bar{i} - L\frac{d\bar{i}}{dt} \tag{4.1}$$

$$G_{PR}(s) = K_p + \frac{2K_i s}{s^2 + \omega^2} \tag{4.2}$$

$$G_{PR}(s) = K_p + \frac{2K_i \omega_c s}{s^2 + 2\omega_c s + \omega^2} \tag{4.3}$$

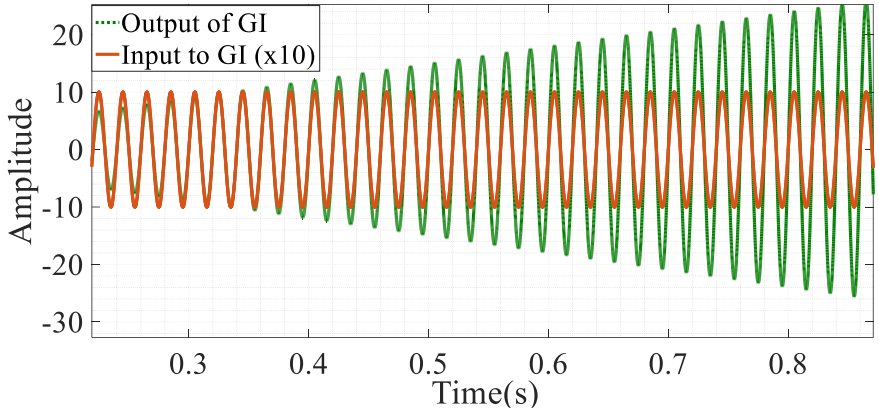


Figure 4-5. Input and output of GI

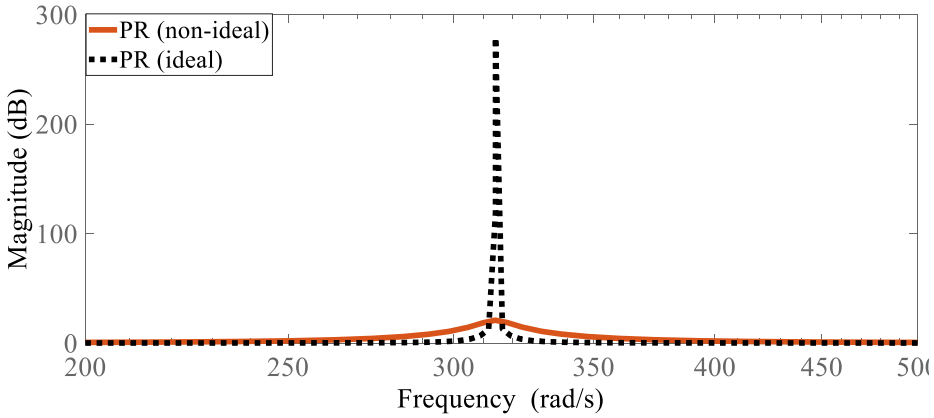


Figure 4-6. Ideal and non-ideal PR controller magnitude bode plot

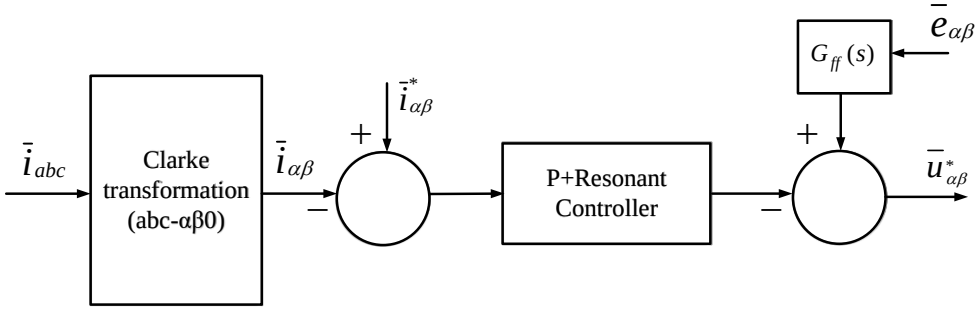


Figure 4-7. Inner current control loop in *αβ0* frame

On the other hand, the current reference signals are provided by the outer control loop. A typical outer control loop is shown in Figure. 4-8, where the DC bus voltage and reactive power are controlled. Since the controlled quantities are DC values, PI controllers can be used to control them. Furthermore, the outputs of these controllers provide the current reference in *dq0* reference frame, e.g., I_d^* and I_q^*. These reference DC signals are then transformed into sinusoidal signals (i.e., $\bar{\imath}_{\alpha\beta}^*$) using Inverse-Park transformation.

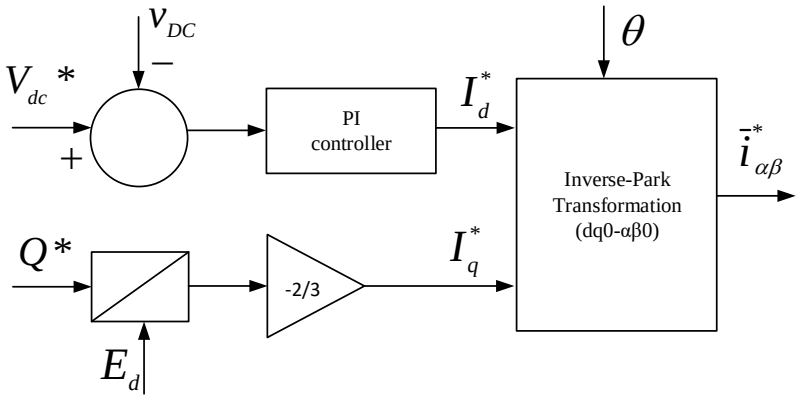


Figure 4-8. Outer control loop to produce reference current signals

4.3 Background Voltage Harmonics

This section explains the propagation of background voltage harmonics in the VSC system designed in the previous section. The origin of the sequence coupling is also derived using the concept of complex space vector to provide additional insight over the derivation using the converter input impedance matrix presented in [129],[134]. Furthermore, three background voltage harmonic mitigation methods mentioned previously are also discussed in more detail. Finally, the impact of these mitigation techniques on current emission is examined.

4.3.1 Propagation of Background Voltage Harmonics

Once there exists background voltage harmonics, i.e., the voltage at the POC, $\bar{e}_{abc}$ contains components at other frequencies along with fundamental component, these voltage harmonics will

result in current harmonics depending on the impedance seen from POC into the converter. For instance, the current flown at harmonic order h in Figure. 4-4 can be found using (4.4) when the background and converter terminal voltages at h^{th} harmonic order are $\bar{e}_h$ and $\bar{u}_h$, respectively.

$$\bar{i}_h = \frac{\bar{e}_h - \bar{u}_h}{R + jh\omega_1 L} \tag{4.4}$$

Furthermore, voltage harmonics at the POC also propagate through the PLL, and result in current harmonics. It is not obvious how background voltage harmonics produce current emission through the PLL looking at the VSC control system. However, this can be explained by looking at the PLL block presented in Figure. 4-3. A PLL is usually implemented in the synchronous reference frame. The measured three-phase voltage, $\bar{e}_{abc}$ at the point of connection (POC) is transformed into two DC quantities, E_d and E_q, using Park transformation, and q-axis voltage is regulated to track the phase angle [134]. Now, when the background voltage is distorted with high frequency components, it will show up in E_q and hence in the detected phase angle, θ. For instance, if $\Delta\bar{e}_q$ is the high frequency component in q-axis voltage, then the detected phase angle θ can be found using (4.5)-(4.7) [134] where E_{1d} is the steady-state POC voltage aligned with d-axis, ω_1 is the fundamental angular frequency, and $H_{PI}(s)$ and $H_{Pll}(s)$ are the PI controller and closed loop transfer function, respectively.

$$\theta = \omega_1 t + \Delta\theta \tag{4.5}$$

$$\Delta\theta = H_{pll}(s)\Delta\bar{e}_q \tag{4.6}$$

$$H_{pll}(s) = \frac{\frac{H_{PI}(s)}{s}}{1 + \frac{E_{1d}H_{PI}(s)}{s}} \tag{4.7}$$

It is clear from (4.5) - (4.6) that high frequency components appear in the detected phase angle in a polluted grid depending on the bandwidth ($H_{pll}(s)$) of the PLL system. This is further explained assuming the background voltage has a 5th order harmonic component, $\bar{e}_5$. Since, 5th order harmonic is considered as negative sequence, it can be written as (4.8) and (4.9) in stationary and synchronous reference frames respectively where E_5 is the amplitude. Therefore, $\Delta\bar{e}_q$ and $\Delta\theta$, in this particular case, would be as in (4.10) and (4.11), respectively.

$$\bar{e}_5 = E_5 e^{-j5\omega_1 t} \tag{4.8}$$

$$\bar{e}_{5dq} = E_5 e^{-j6\omega_1 t} = E_5\left[\cos(6\omega_1 t) - j\sin(6\omega_1 t)\right] \tag{4.9}$$

$$\Delta\bar{e}_q = -E_5 \sin(6\omega_1 t) = \frac{jE_5}{2}(e^{j6\omega_1 t} - e^{-j6\omega_1 t}) \tag{4.10}$$

$$\Delta\theta = jH_{pll}(s = j6\omega_1)\frac{E_5}{2}(e^{j6\omega_1 t} - e^{-j6\omega_1 t}) \tag{4.11}$$

This detected phase angle with high frequency components is used for various reference frame transformations within the VSC control system, e.g., the transformation of current reference values from synchronous frame to stationary frame in outer control loop in Figure. 4-8. If the current is drawn with unity power factor (i.e., $Q^* = 0$), then the transformation can be mathematically represented as (4.12). Furthermore, (4.12) can be rewritten as (4.13) using small signal approximation as $\Delta\theta$ is usually small. Finally, putting the expression of $\Delta\theta$ from (4.11) in (4.13), (4.14) is the current reference signals when the voltage at the POC is distorted with 5th order harmonic. Equation (4.14) shows the cross coupling of sequences, i.e., there exist both positive (7th order) and negative (5th order) sequence harmonics even though the background voltage is distorted with only negative sequence harmonic. Once these current reference signals

with high frequency components are used in the inner current control loop, voltages at those frequencies are generated at the converter terminal and hence, the current emission.

$$\bar{i}_{\alpha\beta}^{*} = I_d^{*} e^{j\theta} = I_d^{*} e^{j(\omega_1 t + \Delta\theta)} = I_d^{*} e^{j\omega_1 t} e^{j\Delta\theta} \tag{4.12}$$

$$\bar{i}_{\alpha\beta}^{*} = I_d^{*} e^{j\omega_1 t}(1 + j\Delta\theta) = I_d^{*} e^{j\omega_1 t} + jI_d^{*} e^{j\omega_1 t}\Delta\theta \tag{4.13}$$

$$\bar{i}_{\alpha\beta}^{*} = I_d^{*} e^{j\omega_1 t} - H_{pll}(s = j6\omega_1)\frac{I_d^{*} E_5}{2}(e^{j7\omega_1 t} - e^{-j5\omega_1 t}) \tag{4.14}$$

4.3.2 Background Voltage Harmonics Mitigation Techniques

From (4.4), it is evident that if the current controller can generate the same harmonic voltage (magnitude and phase) as the voltage at the POC at the converter terminal, i.e., $\bar{u}_h = \bar{e}_h$, there will be no current flowing at the h^{th} harmonic order. This is the main philosophy behind all the methods using VSC control system for background voltage harmonic elimination and is achieved by having appropriate gain or phase margin of the current controller at the frequency of interest. Thus, the current controller is better equipped to track higher frequency current components and to generate voltages at those frequencies at the converter terminal. Various methods are adopted in the literature to increase current control loop gain at high frequencies. One such way is to increase proportional gain, K_p of the PR controller. Another way is to provide grid voltage feedforward, i.e. $G_{ff}(s)$ is non-zero [135]. The third way is to add gain at the frequencies of interest with additional GIs, which are connected in parallel with PR controller to provide resonance at those frequencies. This technique is known as PR with harmonic compensators (HC). The modified current control loop with HC at 5th and 7th harmonic is shown in Figure. 4-9. The effectiveness of these methods can be identified by looking at the frequency response of the small signal model of the current control loop. The frequency responses of current control loop of Figure.

4-7 are plotted in Figure. 4-10 with different K_p. It should be noted that $G_{ff}(s)$ is zero in this case, i.e., no feedforward is provided. As the proportional gain increases, so does the open loop gain of the current controller. For instance, the open loop gain with $K_p = 1$ is zero at frequencies other than fundamental one, whereas this gain is about 10 dB with $K_p = 3$. The frequency responses of the current controller with feedforward are plotted in Figure. 4-11. The open loop gain, in this case, increases linearly with frequency when a voltage feedforward is provided. Figure. 4-12 shows the frequency response of the current control loop of Figure. 4-9 with $G_{ff}(s) = 0$ and $K_p = 1$. This method provides high open loop gain at selected harmonic orders, 5th and 7th in this particular case, hence the name selective harmonic compensator.

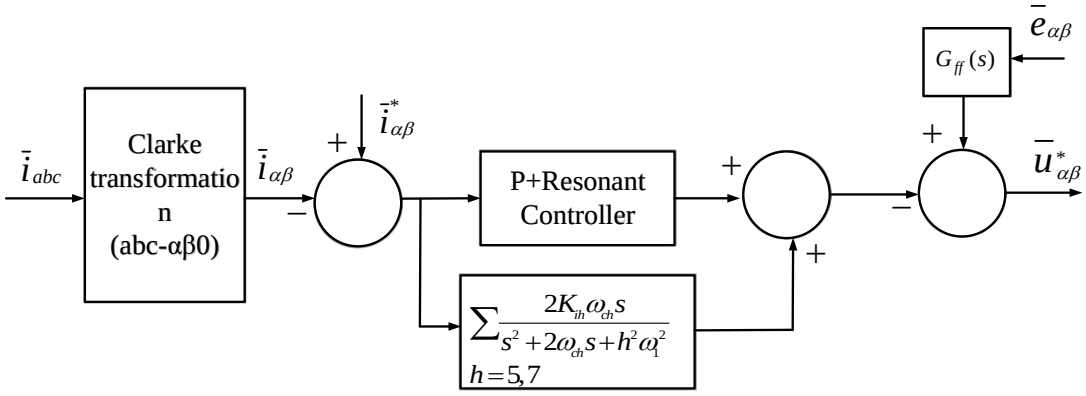


Figure 4-9. Modified inner current control loop with HC

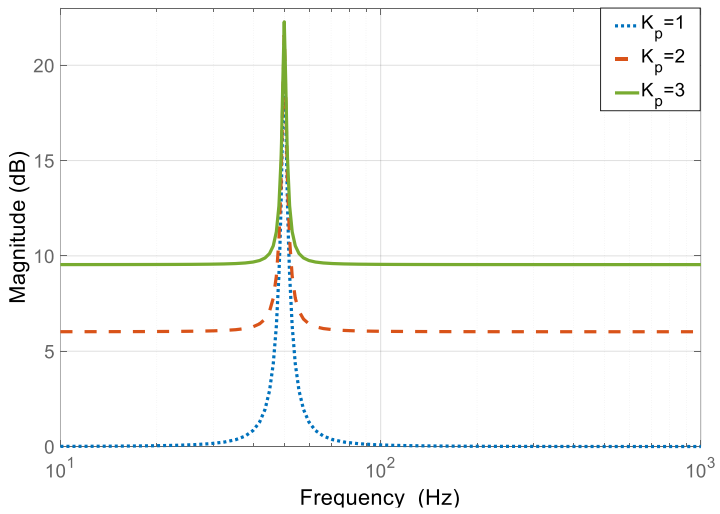


Figure 4-10. Current controller open loop frequency response with various proportional gains

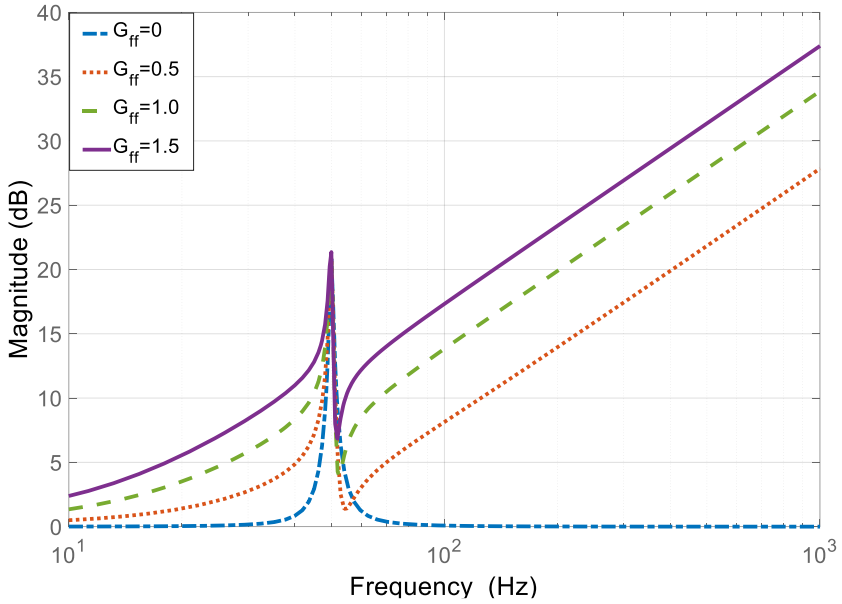


Figure 4-11. Current controller open loop frequency response with different percentage of grid voltage feed-forward

As the current controller gain increases at high frequencies, it can generate more of the line current harmonics at the converter terminal voltage. For instance, in the case of background voltage with 5th order harmonics, $\bar{u}_5$ and $\bar{u}_7$ will increase at the converter terminal since the line current has components at both 5th and 7th order harmonics as explained previously. Although this would reduce the current flow at 5th order harmonic, current emission at 7th order harmonic increases as $\bar{u}_7$ goes up since the background voltage does not contain any 7th order harmonic, i.e., $\bar{e}_7 = 0$.

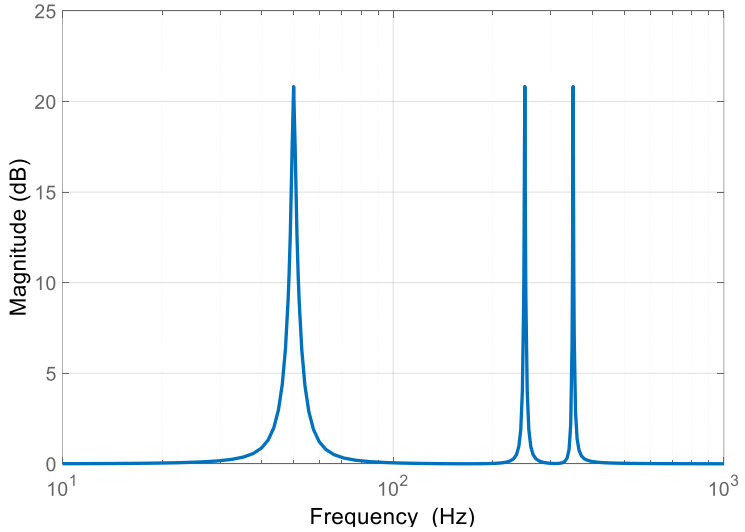


Figure 4-12. Open loop frequency response of current controller with harmonic compensator

4.4 Simulation Results

In this section, simulation results confirm the presence of sequence coupling in reference current signals, and demonstrate the impact of increasing current controller gain, using grid voltage feedforward, and using selective harmonic compensation on current emission in a VSC-based active front in an EV DCFC station. The two-level VSC based active front end described in earlier section (Section 4.1) is modelled in PSCAD/EMTDC, and the system parameters are provided in Table 4-1. All the simulations are performed when the AC grid is balanced and distorted with 5% of 5^{th} harmonics.

Table 4-1: VSC-AFE System Parameters

Parameter	Value
Grid voltage at PCC	400 V
Grid frequency	50 Hz
Output power of the rectifier system	1 MW
Power factor	1.0
Grid side inductor	16 µH
Converter side inductor	200 µH
Filter capacitor	400 µF

Figure. 4-13 shows the coupling of sequences in the reference current signal once transformed from synchronous frame to stationary frame. This validates the analytical derivation of coupling presented in (4.14) with background voltage distorted with 5^{th} order harmonic. The impact of industry practices to eliminate emissions from background voltage harmonics on coupled frequency are presented in Figures. 4-14 - 4-16. Figure. 4-14 demonstrates the impact of increasing current loop gain. Although the 5^{th} order harmonic (i.e., the frequency component in the background voltage) gets reduced in the line current, the 7^{th} order harmonic (coupled frequency) increases with increasing current loop gain. Figure. 4-15 shows that current emission decreases at the frequency the grid being distorted with as grid voltage feed-forward (G_{ff}) is added to the controller. However, the coupled frequency component is not affected in this case. A similar

result is observed with only 5th harmonic compensator added with the PR controller as shown in Figure. 4-16. Nevertheless, if additional 7th harmonic compensator is added with PR controller, emission at the coupled frequency increases.

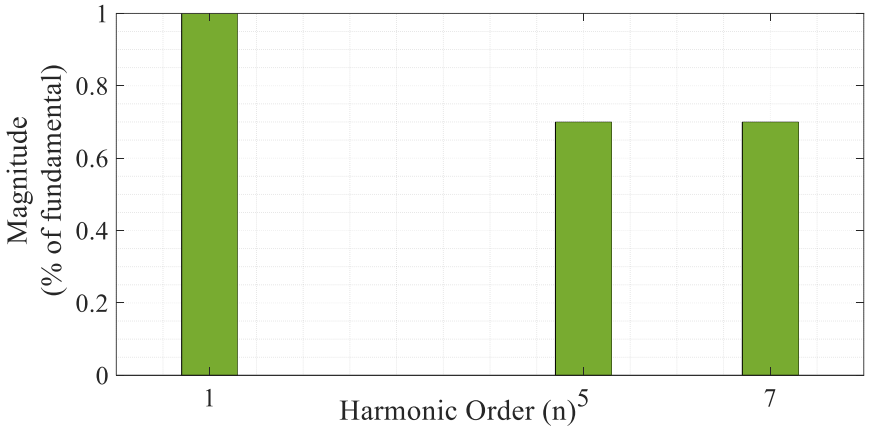


Figure 4-13. Sequence coupling due to PLL

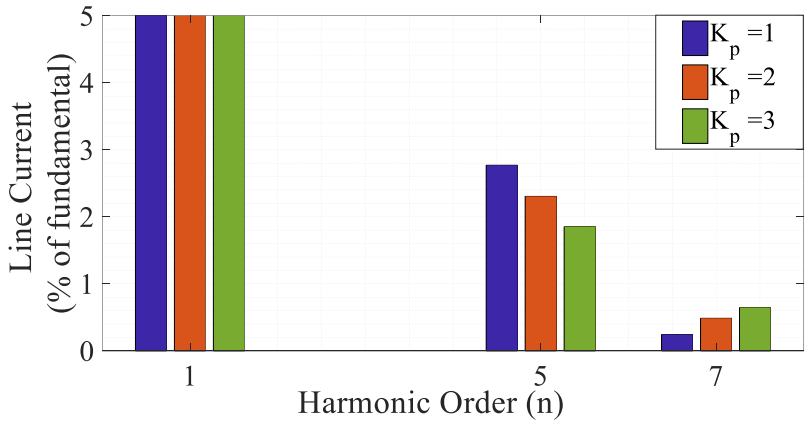


Figure 4-14. Change in current emission with increasing proportional gain of the PR controller

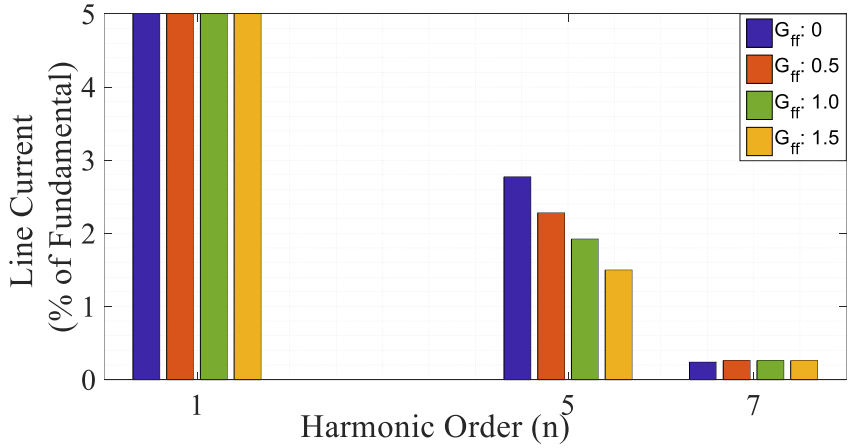


Figure 4-15. Variation in current emission with grid voltage feed-forward

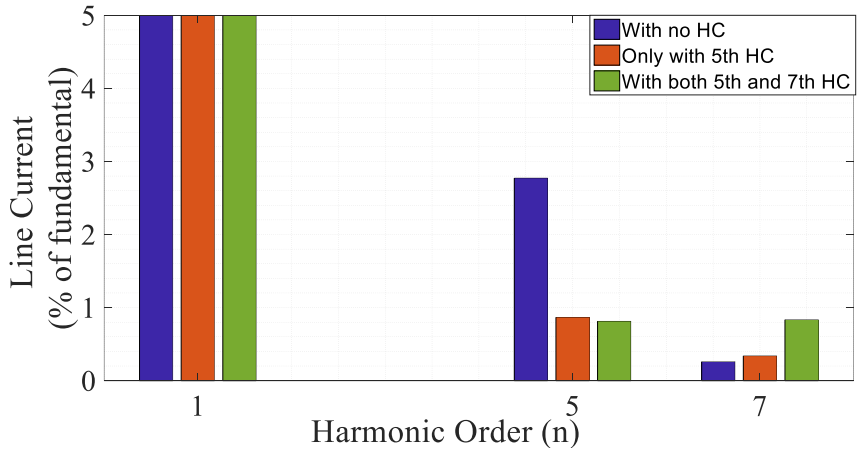


Figure 4-16. Impact of selective harmonic compensation on current emission

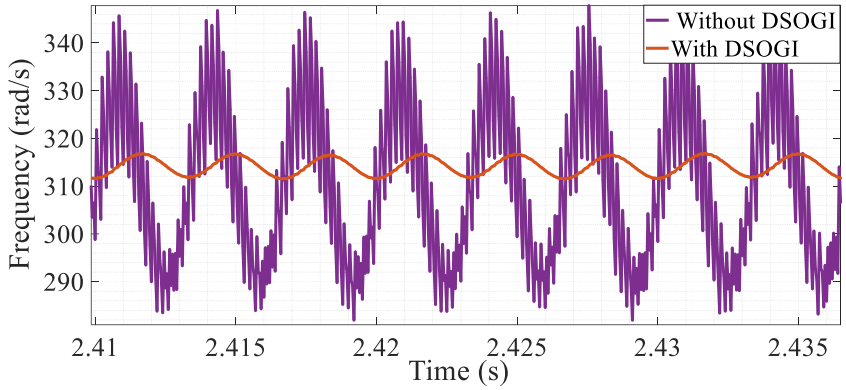


Figure 4-17. Detected angular frequency of the system with and without DSOGI

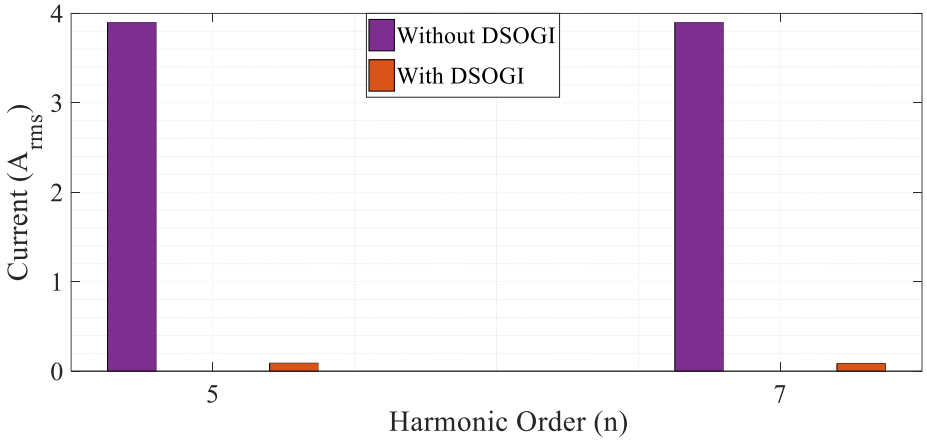


Figure 4-18. Harmonic contents in current reference signals with and without DSOGI

These results do confirm that the usual mitigation techniques of background voltage harmonics cannot reduce the emission at coupled frequency. Moreover, the emission worsens in cases where the gain of current control loop is increased at coupled frequencies. One possible

solution to this problem is to reduce the PLL bandwidth. However, this will result in poor dynamic performance of the VSC system [136]. Another solution is to use Double Second Order Generalized Integrator (DSOGI) which effectively reduces the overall bandwidth of the PLL system without compromising the dynamic response of the system [137]. This is because DSOGI filters out the high order components from the input to the PLL system without introducing any phase delay. The detected angular frequency with and without DSOGI filter is shown in Figure. 4-17. Moreover, Figure. 4-18 compares the harmonics in current reference signal with and without DSOGI. On the other hand, frequency locked loop (FLL) based converter systems have been proposed in the literature [138]–[140]. The only difference between FLL and PLL is that the FLL does not require trigonometric computation. However, DSOGI is still used to eliminate the propagation of background voltage harmonics through both PLL and FLL [141].

4.5 Summary

In a VSC-AFE, the background voltage harmonics mainly propagate depending on design of the current control loop and PLL. The current emission at the frequency the background voltage is being distorted with can be reduced with different current controller settings, grid voltage feed-forward and selective harmonic compensations. However, it is shown in this chapter that these techniques are not effective when it comes to eliminating current emission at the coupled frequency. Therefore, it is necessary to understand the origins of current emissions before implementing various mitigation techniques. This chapter has derived the origins of current emissions at coupled frequency analytically and verified the results with simulation. The effectiveness of DSOGI based PLL in eliminating the current emission at coupled frequencies is also presented in this chapter. DOSGI helps eliminate the propagation of background voltage harmonics through PLL.

Chapter 5

Optimal Control of the DC/DC Converter Interfacing BESS and BEV

5.1. The Ideal Candidate (Semi-DAB)

The architectures shown in Figures. 2-5(a/b) provide high efficiency in a DCFC station with BESS. Moreover, the isolated DC/DC converter interfacing BESS and BEV determines the overall system efficiency in the case of low grid connection due to high power transfer between BESS and BEV. On the other hand, the converter should accommodate wide variation in both input and output voltage as the voltages of the BESS and BEV change with their corresponding state-of-charge (SOC). Thus, this converter should have high efficiency over wide input and output voltage ranges. Moreover, a common fast-charging scenario with BESS is high SOC (and thus voltage) in the stationary BESS and low SOC (and thus voltage) in the BEV battery, so it is crucial to improve the operational efficiency of the converter at low output voltages.

Two prominent topologies for the high-power isolated unidirectional converter between the DC bus and the BEV are the LLC full-bridge resonant converter (FB-LLC) and the phase-shifted zero voltage transition full-bridge converter (PSFB) [75], [103]. A FB-LLC converter achieves voltage regulation by voltage division with frequency-dependent impedance, which provides a variable voltage gain. Therefore, the switching frequency varies for the purpose of voltage and load regulation, which makes the design of passive components complicated. Moreover, interleaving, which is preferred in high power applications like DCFC, is difficult with the LLC converter because voltage gain is dependant on switching frequency, and in an LLC converter, the voltage gain of each interleaved phase can be different due to component tolerances. In [142], this problem is solved using switched capacitors, which are used to control the equivalent resonant capacitance for each of the phases. However, this technique is useful with constant input and output voltage and is not suitable for the BEV fast charging with ESS application which can have widely

varying input and output voltages. In addition, the LLC converter has higher current stress at the secondary side compared to the PSFB.

Conversely, the PSFB converter operates with constant frequency, hence, interleaving multiple phases is simple. However, the traditional PSFB with passive diode rectifier at the secondary side and DC output inductor has some drawbacks. For instance, the converter only operates in buck mode and hence, has limited voltage gain, and for low conversion ratio, i.e., high input voltage and low output voltage, the freewheeling period is long. An extended freewheeling period increases the circulating current through the switches and the transformer, hence, the conduction losses increase [143]. Furthermore, the secondary side diodes suffer from high voltage stress due to high reverse recovery current if Si-based semiconductor devices are used. High voltage ringing is still present at the secondary side with wide bandgap devices such as silicon carbide (SiC) diodes. Additional passive and active-clamp circuits are used in [144]–[146] to reduce the circulating current and secondary diode voltage stress. However, these additional circuits complicate the control of the converter and losses are still significant in the auxiliary circuits.

To reduce the secondary reverse voltage stress and large output DC inductor in the traditional PSFB, the passive diode rectifier at the secondary side can be replaced with a fully controlled rectifier. This is known as the dual active bridge (DAB) converter and is widely used in bidirectional DC/DC converter applications due to its high efficiency and power density. Advanced control strategies have been extensively investigated for the DAB converter in the literature [147]–[150]. However, in the EV DCFC application, unidirectional DC/DC converters will suffice. Therefore, the semi-DAB topology, which is the unidirectional version of the DAB converter, is a better choice for DCFC applications because it retains the benefits of the DAB

converter while saving the cost of two active switches and the associated gate drivers at the secondary side [151]–[154].

Figure. 5-1 shows a typical semi-DAB converter. The DC blocking capacitor, C_{dc}, is usually used in phase-shifted converters to avoid transformer saturation with voltage mode control [155], [156]. Even though these converters can operate in both buck and boost mode, the voltage conversion ratio is limited. For instance, in the buck mode with heavy load, both the primary and secondary side phase shift, i.e., dual phase-shift control is required, and this increases the circulating current in the primary side. During boost mode operation, the Zero Voltage Switching (ZVS) range cannot be achieved over a wide voltage gain and high turn-off losses are inevitable at the secondary side active half-bridge. Moreover, the secondary side current RMS is high as in the LLC converter due to the absence of any output inductor. Nevertheless, the semi-DAB converter retains the benefit of constant frequency control of a traditional PSFB while reducing the voltage stress on the secondary side. The buck and boost operation capability of this converter extends the voltage gain range compared to the PSFB. Therefore, the semi-DAB converter is often recommended for medium to high output voltage applications [157].

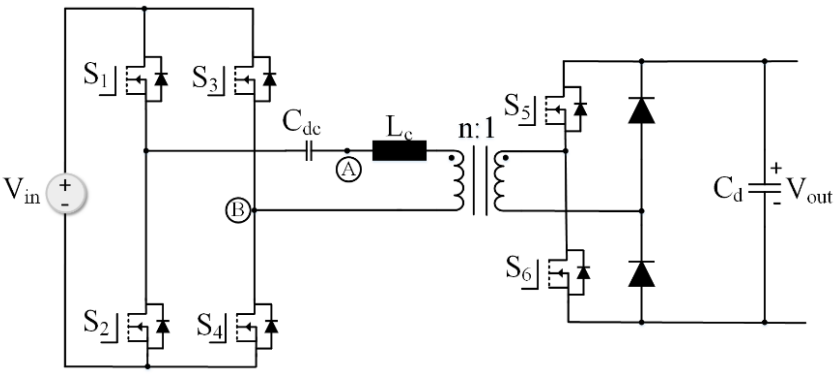


Figure 5-1. Basic semi-DAB converter

Extensive research has been conducted to improve the operation and efficiency of the semi-DAB converter. The basic operational principle of the semi-DAB converter is explained in [158]

and compared with the DAB along with experimental results. However, the authors did not provide any efficiency results in the paper. An optimal control strategy is developed in [151] to limit the peak current in the converter. In this control strategy, both the primary and secondary side phase-shift is required at any given operating point. Even though the control strategy is more complex than the traditional dual phase-shift control (DPS), the controller provides efficiency improvements at low power for some voltage gains compared to DPS whereas the efficiency is similar to DPS for most operating points. A variable frequency control strategy is used in [159] to improve efficiency mainly at light load conditions. Similarly, a multimode control strategy is developed in [154] to improve the efficiency at light load using phase-shift along with variable frequency control. The hybrid control strategy provided in [157] is essentially a modification of the DPS control, however, the efficiency results are not compared with the traditional DPS. Similarly, [160] proposes a control strategy to improve the efficiency of a semi-DAB converter by extending the ZVS operational range. However, ZVS cannot always be achieved when the input and output voltage vary widely. Again, the results are compared with SPS control, not with DPS control. Moreover, in most of these control strategies, the research is mainly focused on light load condition and the converters designed have limited voltage gain range.

Therefore, this thesis proposes an optimal control strategy to provide wide voltage gain in semi-DAB converters by reconfiguring itself to half-bridge and full-bridge structures while achieving high efficiency depending on the required voltage gain, even at higher loads. Thus, the control theory is named *Reconfigurable Bridge Optimal Control* (RBOC). With the reconfigurable bridge structure, the input voltage is effectively halved at the clamped inductor terminal in a half-bridge structure compared to in a full-bridge structure. Therefore, the voltage across the clamped inductor while the inductor current magnitude is rising is much lower than that of the full-bridge

case with high input voltages and low output voltages. This concept is somewhat related to the concept proposed in [161] for LLC converters to improve the light-load efficiency, but the proposed operation in semi-DAB converters is very different of that in LLC converters. A similar hybrid modulation strategy is presented in [162] for a DAB converter. The converter operates in half-bridge and full-bridge structure on both sides to reduce the rms current in the system depending on the transmitted power. However, the converter only operates with SPS. Moreover, the operation of the semi-DAB converter is also different than that of the DAB converter even though the semi-DAB is derived from the DAB, due to the presence of the secondary diode leg [151], [158]. Therefore, this thesis also provides an algorithm to determine the required phase-shift (single or dual) in real time at any give operating point through comprehensive analysis of load dependant operation of the semi-DAB converter. This eliminates the necessity of devising the control trajectory offline, and it can be used for any semi-DAB converter. Though the proposed control strategy is general and can be used in any application with semi-DAB, this thesis focuses on the DCFC application, with a focus on the common scenario of high voltage at the BESS and low voltage at the BEV. This chapter provides: i) a new comprehensive analysis of load dependent operation of the semi-DAB converter, which is then used in the development of, ii) the proposed RBOC control strategy, which improves efficiency of the semi-DAB converter at high input voltages and low output voltages, even at high load, without compromising the efficiency at higher output voltages. The superiority of the RBOC strategy is verified with a 10 kW prototype, and all efficiency results are compared to DPS control.

5.2. Operational Principle

A semi-DAB can operate both in buck and boost mode. Depending on the input and output voltage, i.e., voltage gain and load, the proposed control method will operate this converter in half-

bridge or full-bridge structure. The half-bridge structure allows the input voltage to be effectively halved and thus makes the voltage gain twice that of the full bridge. This is particularly helpful with high input voltage and low output voltage operating points to reduce the conversion effort of the converter. The voltage gain, M', at the primary side for the full-bridge and the half-bridge structure is defined in (5.1) and (5.2), respectively, where V_{out} and V_{in} are output and input voltage, respectively, and n is the transformer turns-ratio.

$$M' = \frac{nV_{out}}{V_{in}} \tag{5.1}$$

$$M' = \frac{2nV_{out}}{V_{in}} \tag{5.2}$$

When the converter operates with the full-bridge structure, both primary and secondary phase-shift control is possible, and they are named as internal and external phase-shifts in this thesis, respectively. However, in the half-bridge operation, the converter loses the ability of the internal phase-shift. Therefore, the proposed controller controls the output voltage with internal phase-shifts in the full-bridge structure and with variable duty cycle control in the half-bridge structure. This section explains the different operational modes of this converter in full-bridge and half-bridge structure. Even though these operational modes are well-known in the literature, this chapter further classifies the load dependent operational modes into distinctive categories to identify the required phase-shifts and duty cycles at any operating point. This reduces the required computational burden to search for optimal phase-shifts between active legs in the semi-DAB converter in real time. The derivations in this thesis do not consider the impact of dead-time nor that of the DC blocking capacitor values. Nevertheless, these derivations provide a good approximation in finding the operational mode and related phase-shift duty cycles.

5.2.1 M′<1 and Buck Mode (Type 1)

During this operational mode, while operating with the full-bridge structure, the secondary-side half-bridge can be turned off to operate as a simple full-bridge diode rectifier as shown in Figure. 5-2. In this case, the body diodes would conduct, resulting in high conduction losses. To reduce the losses in the body diodes, the switches are turned-on. These switches are susceptible to high turn-on losses due to high turn-on current. Therefore, while operating in buck mode, it is made sure to turn on the secondary switches with zero current, i.e., zero current turn-on (ZCS). Therefore, the secondary side switches should have a minimum phase-shift compared to the primary side to ensure ZCS. This is further explained in Figure. 5-3 where the gate signals along with the clamped inductor current, i_{Lc}, and voltage, v_{Lc} are shown.

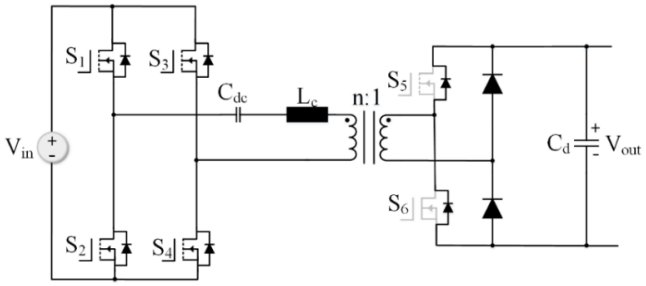


Figure 5-2. Buck mode of operation where secondary side active switches are turned-off

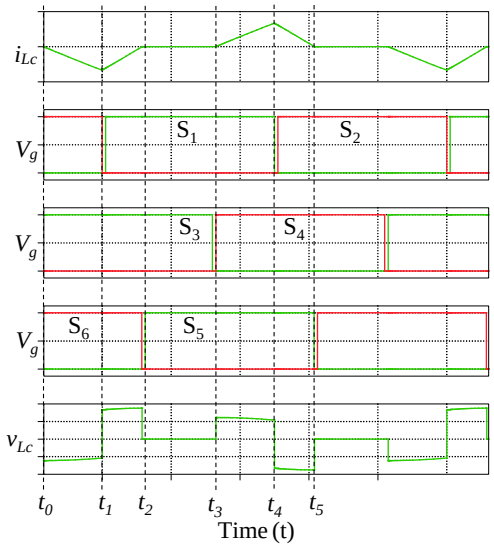


Figure 5-3. Clamped inductor current along with switching signals during buck mode of operation for a full-bridge structure

1) Full-Bridge: Stage 1 ($t_0 < t < t_1$)

Before t_1, S_2 and S_3 on the primary side and S_6 at the secondary side are conducting and the voltage across the clamped inductor, L_c is negative. Therefore, the inductor current, i_{Lc}, is negative and increasing in magnitude. The corresponding circuit schematic is shown in Figure. 5-4(a) along with equivalent circuit referred to the primary side in Figure. 5-4(b). The voltage across the clamped inductor, L_c is shown in (5.3).

$$v_{Lc} = -V_{in} + nV_{out} \tag{5.3}$$

2) Full-Bridge: Stage 2 ($t_1 < t < t_2$)

At t_1, S_2 turns off and S_1 turns on and the voltage across the clamped inductor becomes positive due to the reflected output voltage at the primary side. Therefore, the negative inductor current decreases in magnitude. The corresponding circuit schematic is shown in Figure. 5-4(c) along with equivalent circuit referred to the primary side in Figure. 5-4(d). The voltage across the clamped inductor, L_c during this interval is shown in (5.4).

$$v_{Lc} = nV_{out} \tag{5.4}$$

3) Full-Bridge: Stage 3 ($t = t_2$)

If the secondary switch S_5 turns on before the clamped inductor current becomes zero, i.e., at $t < t_2$, this negative current reflected to the secondary side will flow through S_5 at turn-on, therefore, ZCS cannot be accomplished. The corresponding circuit schematic is shown in Figure. 5-4(e) along with equivalent circuit referred to the primary side in Figure. 5-4(f). The voltage across the clamped inductor, L_c in this interval is zero. Therefore, the required minimum external phase-shift value can be found by finding the clamped inductor current zero crossing at $t=t_2$.

The phase-shift requirements for this mode of operation can be derived from Figure. 5-3. Also, it should be noted that the converter operates in discontinuous conduction mode since the external phase-shift is smaller than the internal phase-shift. From Figure. 5-3, the following equations can be derived:

$$\begin{aligned} t_4 - t_1 &= T_{s/2} \\ t_2 - t_1 &= t_5 - t_4 = D_2 T_{s/2} \\ t_3 - t_1 &= D_1 T_{s/2} \\ t_1 - t_0 &= t_4 - t_3 = (1 - D_1) T_{s/2} \end{aligned} \tag{5.5}$$

where,

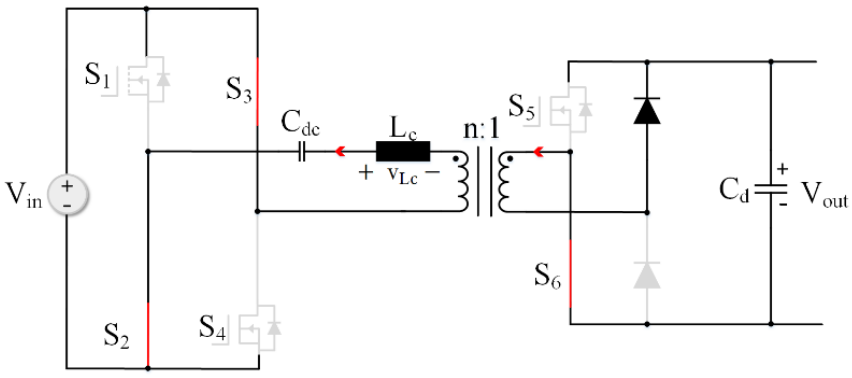
$T_{s/2}$: half of the switching period

D_1: internal phase-shift (phase-shift duty cycle between S_1 and S_4)

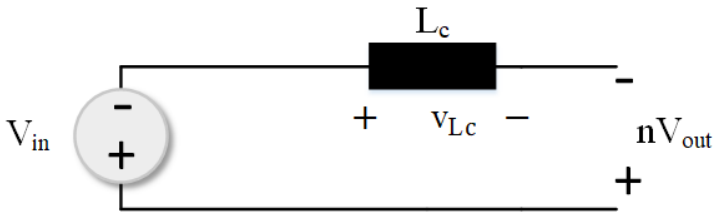
D_2: external phase-shift (phase-shift duty cycle between S_1 and S_5)

and

$D_1, D_2 < 1$



(a)



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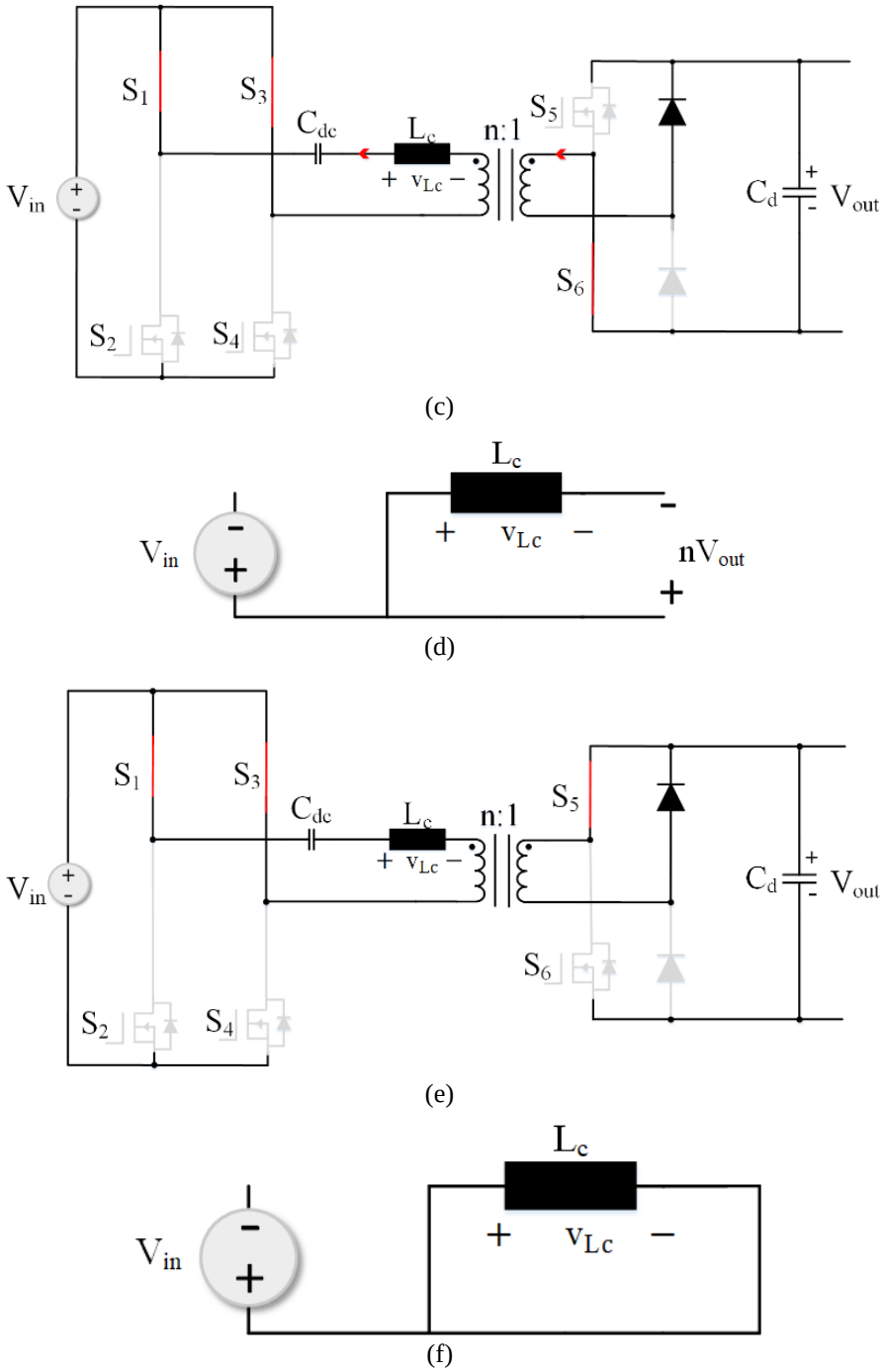


Figure 5-4. Circuit schematics and equivalent circuits for different stages of full-bridge buck operations: (a) & (b) stage 1, (c) & (d) stage 2, and (e) & (f) stage 3

The volt-second law across the clamped inductor using (5.3) - (5.5) can be written as in (5.6), and the voltage gain, M' can be derived as in (5.7) by rearranging (5.6).

$$(-V_{in} + nV_{out})(1 - D_1)T_{s/2} + nV_{out}D_2T_{s/2} = 0 \tag{5.6}$$

$$\frac{nV_{out}}{V_{in}} = \frac{1 - D_1}{1 - D_1 + D_2} = M' \tag{5.7}$$

Also, from (5.6), it is evident that the operation of this converter in this mode in each half switching period is similar to the non-isolated buck converter in discontinuous conduction mode as derived in [163]. Therefore, the voltage gain while the buck converter operates in discontinuous conduction mode can be found using (5.8).

$$M' = \frac{2}{1 + \sqrt{1 + 4K / (1 - D_1)^2}} \tag{5.8}$$

where,

$$K = \frac{2L_c}{n^2 R_{load} T_{s/2}}, R_{load} = \frac{V_{out}}{I_{out}}$$

Therefore, the required phase shifts, D_1 and D_2, can be found using (5.7) and (5.8):

$$\begin{aligned} D_1 &= 1 - \sqrt{\frac{4K}{(\frac{2}{M'} - 1)^2 - 1}} \\ D_2 &= (\frac{1}{M'} - 1)(1 - D_1) \end{aligned} \tag{5.9}$$

During the half-bridge operation, the output voltage will be controlled by varying the duty cycle of S_1 and S_2. In addition, the switch S_4 will always be turned on and S_3 will be turned off to operate in half-bridge mode. The DC blocking capacitor will prevent transformer saturation by blocking any DC component, i.e., the input voltage will be split in positive and negative halves at the transformer terminal, hence the average voltage across the transformer will be zero. The equivalent circuit is shown in Figure. 5-5 where the DC blocking capacitor is absent. Since the

difference in duty cycle of S_1 and S_2 will result in possible saturation of the transformer, S_1 and S_2 will have the same duty cycle and be phase-shifted by half of the switching period. This is further explained with Figure. 5-6.

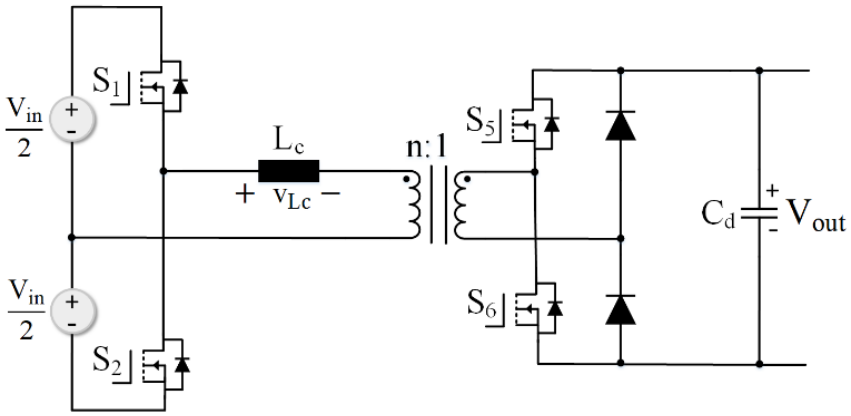


Figure 5-5. Effective converter structure during half-bridge operation

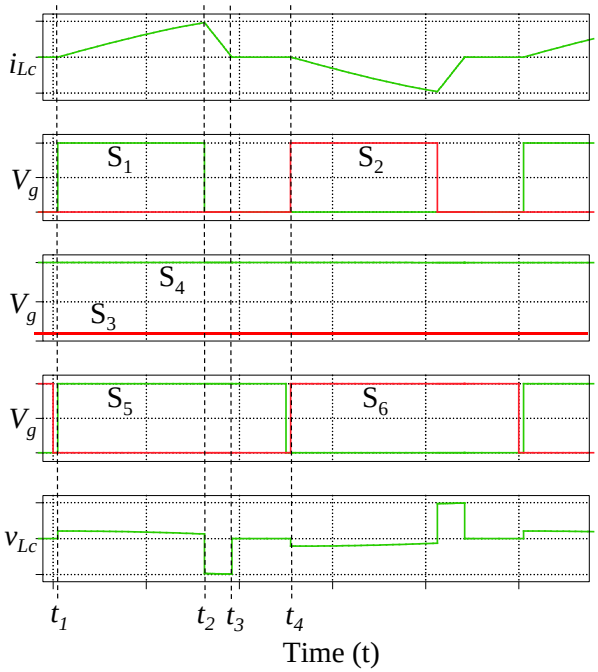


Figure 5-6. Clamped inductor current along with switching signals during buck mode of operation for a half-bridge structure

4) Half-Bridge: Stage 1 ($t_1 < t < t_2$)

At $t=t_1$, switch S_1 turns on with zero current and the clamped inductor current increases until $t=t_2$ when the switch S_1 turns off. The corresponding circuit diagram along with the equivalent

circuit referred to the primary side are shown in Figure. 5-7(a) and 5-7(b), respectively. The voltage across the inductor, v_{Lc} for this stage is as in (5.10).

$$v_{Lc} = \frac{V_{in}}{2} - nV_{out} \tag{5.10}$$

5) Half-Bridge: Stage 2 ($t_2 < t < t_3$)

At $t=t_2$ when switch S_1 turns off, the inductor current is still positive and therefore the body diode of S_2 will start conducting. The corresponding circuit diagram and equivalent circuit referred to the primary side is shown in Figure. 5.7(c) and 5.7(d). The voltage across the clamped inductor, L_c for this stage is as (5.11) and due to the negative voltage across the inductor, the current starts to decrease and reaches zero at $t = t_3$.

$$v_{Lc} = -\frac{V_{in}}{2} - nV_{out} \tag{5.11}$$

6) Half-Bridge: Stage 3 ($t_3 < t < t_4$)

In this stage, the current is zero and the converter is in off-state. At $t = t_4$, switch S_2 turns-on with zero current. Here, $t = t_4 - t_1 = \frac{T_s}{2}$ and T_s is the switching period.

The peak inductor current, i_{peak}, can be found with (5.12) and (5.13) using (5.10) and (5.11), respectively and (5.14) can be written by equating (5.12) and (5.13). Furthermore, average output current, I_0, can be found using (5.15). The required duty cycle, D_c can then be found by solving (5.14) and (5.15).

$$i_{peak} = \frac{v_{Lc} D_c T_s}{L_c} \tag{5.12}$$

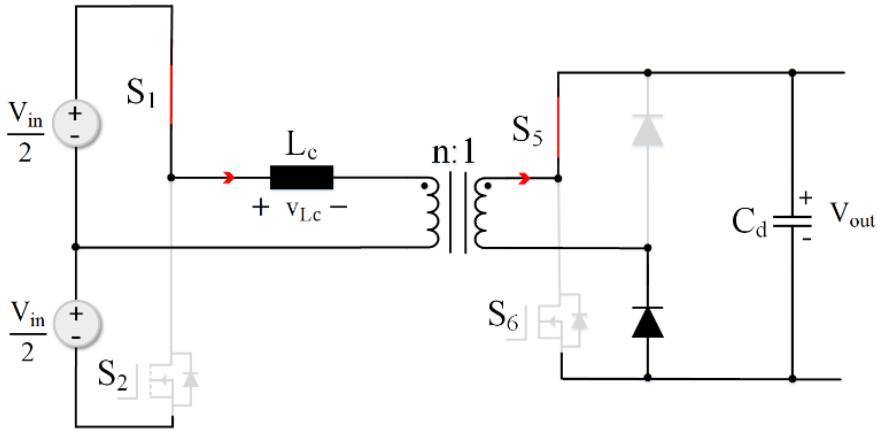
$$i_{peak} = \frac{-v_{Lc} D_{ci} T_s}{L_c} \tag{5.13}$$

where,

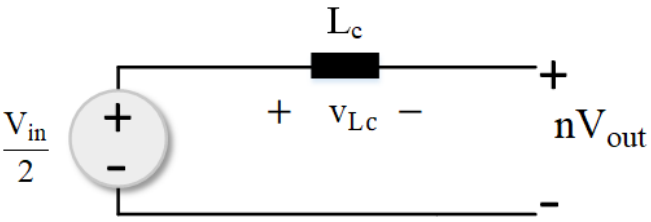
$$D_c T_s = t_2 - t_1, D_{ci} T_s = t_3 - t_2 \text{ and } D_c + D_{ci} < 0.5$$

$$M' = \frac{nV_{out}}{V_{in}/2} = \frac{D_c - D_{ci}}{D_c + D_{ci}} \tag{5.14}$$

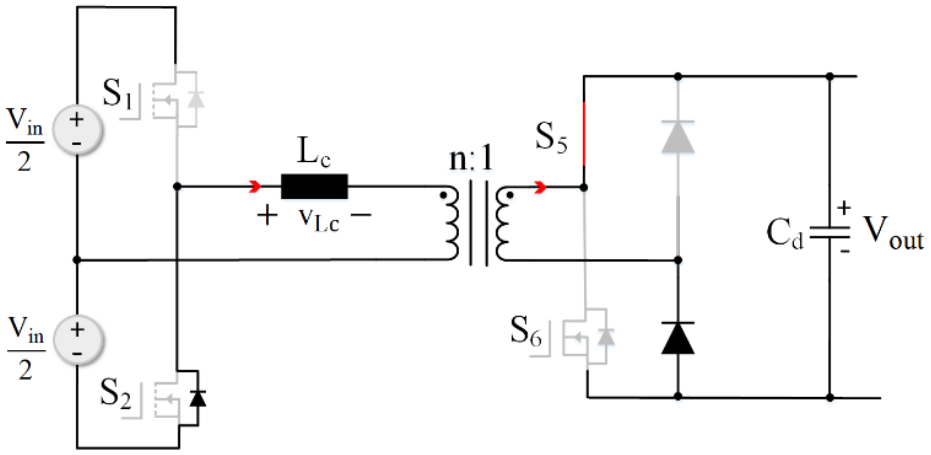
$$I_0 = ni_{peak}(D_c + D_{ci}) \tag{5.15}$$



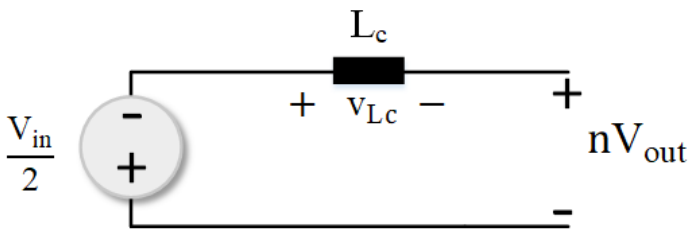
(a)



(b)



(c)



(d)

Figure 5-7. Circuit schematics and equivalent circuits for different stages of half-bridge buck operations: (a) & (b) stage 1 and (c) & (d) stage 2

5.2.2 M′<1 and Boost Mode (Type 2)

Even when the voltage gain required is less than unity, the converter can go into boost mode depending on the load. The reason is that the converter does not operate similar to a non-isolated buck converter in continuous conduction mode and the converter suffers from duty cycle loss. This is further explained in the next section. The operational principle of the converter in this case is different than the boost mode when the voltage gain is larger than unity. The converter operates with single phase-shift rather than dual phase-shift, i.e., the two half-bridge legs on the primary side for the full-bridge structure are always in phase and the secondary side is only phase-shifted unlike the buck operational mode. Hence, the internal phase-shift is zero and only the external phase-shift is adjusted. The converter operates in continuous conduction mode and is further explained using Figure. 5-8 for the full-bridge structure. Similar analysis is valid for the half-bridge structure.

1) Full-Bridge: Stage 1 ($t_1 < t < t_2$)

At $t = t_1$, switch S_2 turns off and the negative current flows through the body diode of S_1 during the dead-time which ensures Zero Voltage turn-on (ZVS) for switch S_1. The second primary side leg also works in a similar way since the diagonal switches (S_1-S_4 and S_2-S_3) are in phase. The corresponding circuit diagram and equivalent circuit are shown in Figure. 5-9 (a) and 5-9 (b), respectively. The clamped inductor voltage for this stage can be written as (5.16).

$$v_{Lc} = V_{in} + nV_{out} \tag{5.16}$$

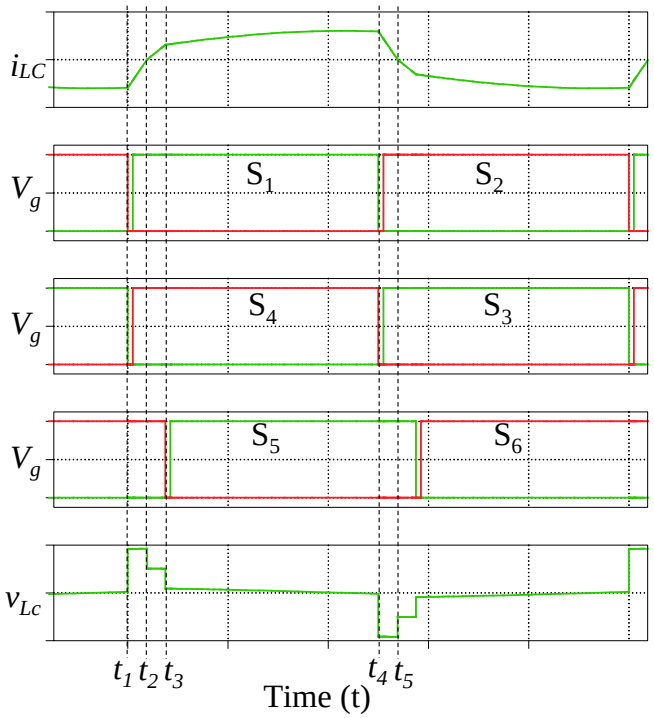


Figure 5-8. Clamped inductor current along with switching signals during continuous conduction mode for M'<1 and boost operation of the full-bridge structure

2) Full-Bridge: Stage 2 ($t_2 < t < t_3$)

At $t = t_2$, the inductor current hits zero and the current starts to increase in positive magnitude afterwards. Since the current is positive and S_6 is still on, this current circulates in the secondary side and no energy is transferred from the primary side to the secondary side. The corresponding circuit diagram and equivalent circuit are shown in Figure. 5-9 (c) and 5-9 (d), respectively. The clamped inductor voltage can be written as shown in (5.17).

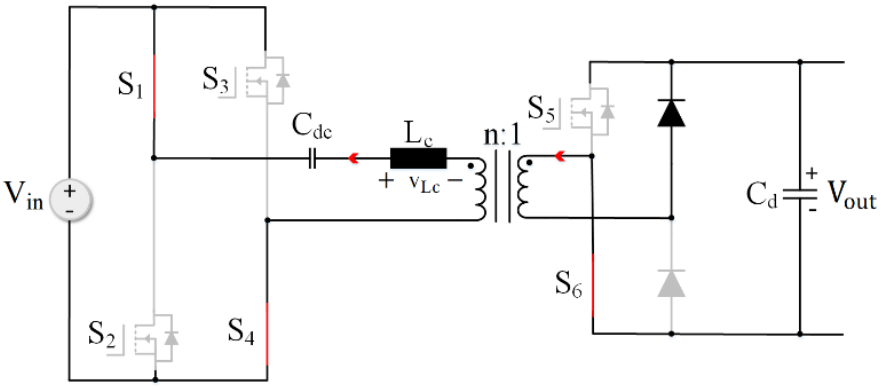
$$v_{Lc} = V_{in} \tag{5.17}$$

3) Full-Bridge: Stage 3 ($t_3 < t < t_4$)

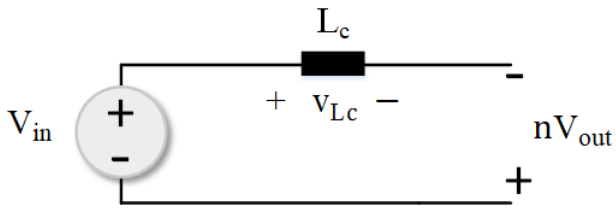
At $t = t_3$, switch S_6 turns off and S_5 turns on after the dead-time interval. In this stage, the energy is again transferred from the primary side to the secondary side. The corresponding circuit

diagram and equivalent circuit are shown in Figure. 5-9 (e) and 5-9 (f), respectively. The clamped inductor voltage can be written as (5.18) for this stage.

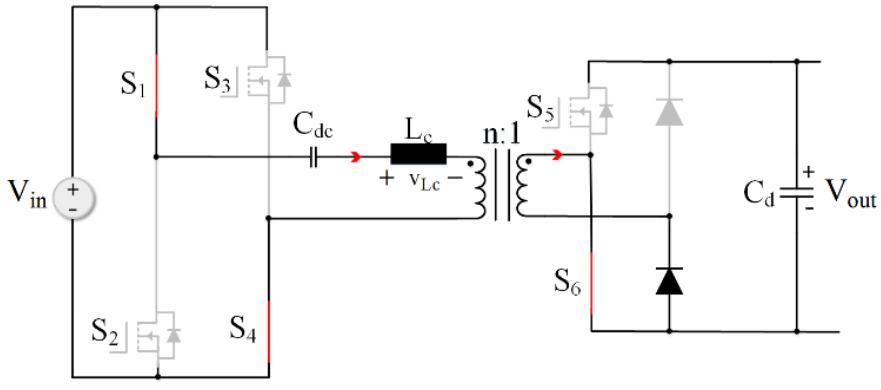
$$v_{Lc} = V_{in} - nV_{out} \tag{5.18}$$



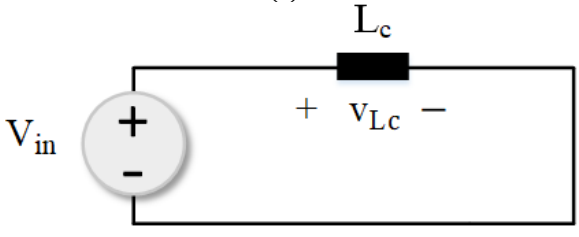
(a)



(b)



(c)



(d)

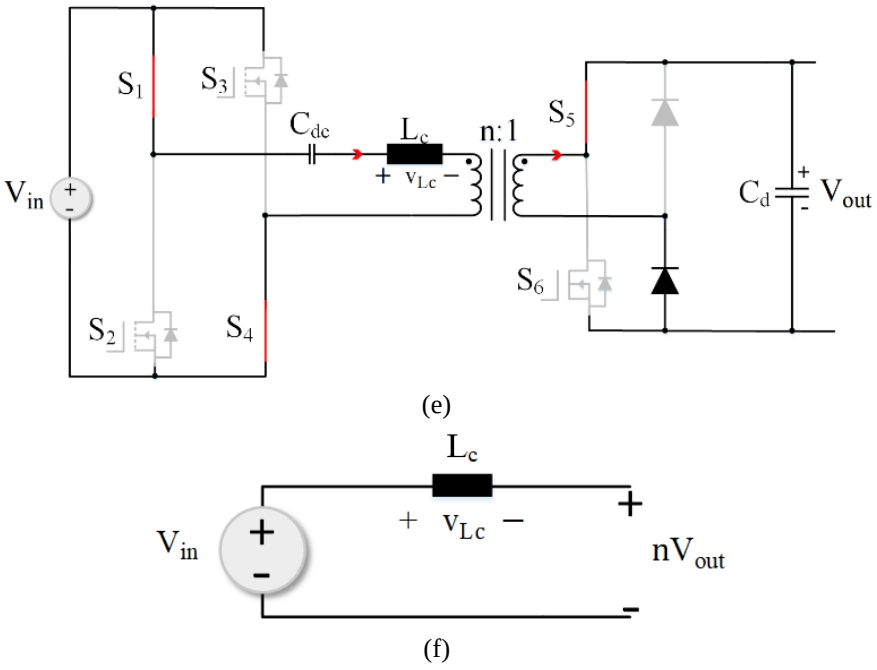


Figure 5-9. Circuit schematics and equivalent circuits for different stages of full-bridge boost operations while M'<1: (a) & (b) stage 1, (c) & (d) stage 2, and (e) & (f) stage 3

The inductor peak current, i_{peak}, can be written as (5.19) using (5.16) - (5.18) and voltage gain M' can be found from (5.20) by rearranging (5.19). Furthermore, the average output current, I_0, can be found with (5.21) by comparing the primary and output current as shown in Figure. 5-10. Finally, the required external phase-shift value, D, can be found by solving (20) and (21).

$$i_{peak} = \frac{V_{in}(D - D_a)T_{s/2}}{L_c} + \frac{(V_{in} - nV_{out})(1-D)T_{s/2}}{L_c} = \frac{(V_{in} + nV_{out})D_a T_{s/2}}{L_c} \tag{5.19}$$

$$M' = \frac{nV_{out}}{V_{in}} = \frac{1-2D_a}{1-D+D_a} \tag{5.20}$$

where,

$T_{s/2}$: Half of the switching period = t_4 - t_1,

$$D_a = (t_2 - t_1)/T_{s/2} = (t_5 - t_4)/T_{s/2}$$

$$D = (t_3 - t_1)/T_{s/2}$$

$$I_0 = \frac{1}{2} i_{peak}(1 - D + D_a) + \frac{1}{2} i_{peak1}(1 - D) \tag{5.21}$$

where,

$$i_{peak1} = \frac{V_{in}(D - D_a)T_{s/2}}{L_c} \text{ and } i_{peak} = \frac{(V_{in} + nV_{out})D_a T_{s/2}}{L_c}$$

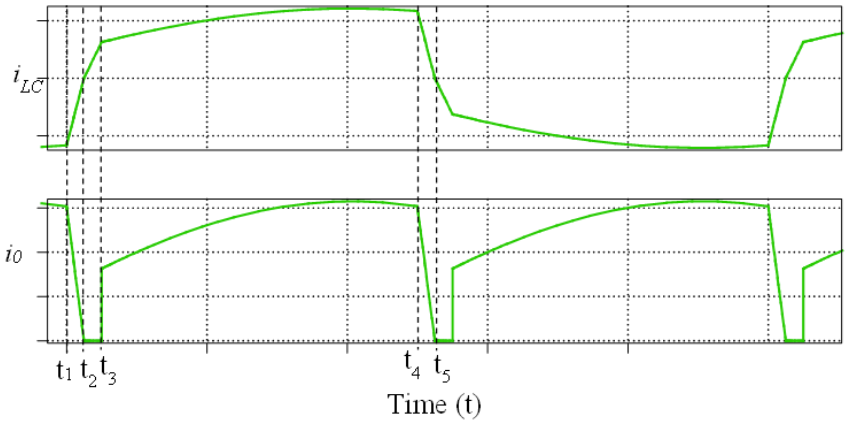


Figure 5-10. Primary side and secondary side rectified current waveforms

5.2.3 M′>1 and Boost Mode (Type 3)

When the voltage gain is greater than unity, the converter operates in boost mode. Although the converter operates with only external phase-shift, i.e., single phase-shift as in the previous case, the mode of operation can be both continuous and discontinuous conduction.

The equations derived in the previous subsection can be used to find the required phase-shift for the continuous conduction mode even though the clamped inductor current waveform, and thus the peak current, is different than the previous case. This is explained by comparing Figure. 5-8 and Figure. 5-11. For this case when $M'>1$, the peak current occurs at $t = t_3$ instead of at $t = t_4$ as in the previous case. This is due to the fact that nV_{out} is greater than V_{in} in this case and the inductor voltage, v_{Lc} as in (5.18) becomes negative during the time period: $t_3 < t < t_4$. For the discontinuous conduction mode, the duty cycle equation used for the non-isolated boost converter can be used to

find the required external phase-shift. The well-known equation to find duty cycle for the non-isolated boost converter in DCM derived in [163] can be modified for this case as in (5.22).

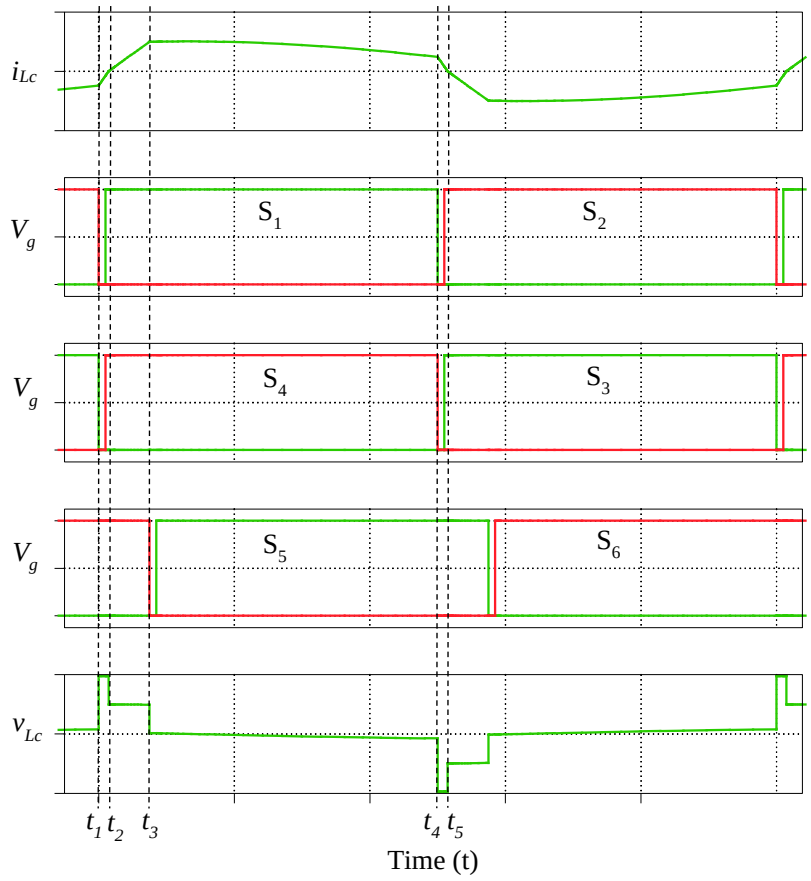


Figure 5-11. Clamped inductor current along with switching signals during continuous conduction mode for M'>1 of the full-bridge structure

$$D = \sqrt{\frac{((2M'-1)^2 - 1)K}{4}} \tag{5.22}$$

where,

D: Phase-shift duty cycle between S_1 and S_5

$$K = \frac{2L_c}{n^2 R_{load} T_{s/2}}, R_{load} = \frac{V_{out}}{I_{out}}$$

5.3. Proposed RBOC Control

5.3.1 Proposed Control Law

The primary goal is to reduce the peak clamped inductor current in order to improve efficiency. In this type of converter, most losses come from the turn-off losses due to the high turn-off currents as the switches can be turned-on with ZVS and ZCS. Therefore, turn-off losses can be reduced by limiting the peak current. Moreover, the rms current also decreases with decreasing peak current value, hence the conduction losses also decrease. Thus, the main goal of the RBOC strategy is to minimize peak clamped inductor current to reduce switch turn-off losses, and the conductions losses are reduced as an added benefit; thus, the total losses of the converter are significantly reduced. Furthermore, the phase-shift during boost operation when the gain is larger than unity, i.e., during type 3 operational mode, is also limited to a pre-defined value to reduce the secondary side losses. This phase-shift value is called D_{boost_max} for this analysis. To achieve the minimum peak current possible within the allowable phase-shift values at any operating point, the following steps are proposed to determine the converter structure and thus the required phase-shifts.

The proposed controller design is summarized in the flow chart in Figure. 5-12. First, the required voltage gains for the half-bridge, M_{half} and full-bridge, M_{full} structure are calculated as in (5.23).

$$M_{half} = \frac{nV_{out}}{V_{in}/2}$$
$$M_{full} = \frac{nV_{out}}{V_{in}} \tag{5.23}$$

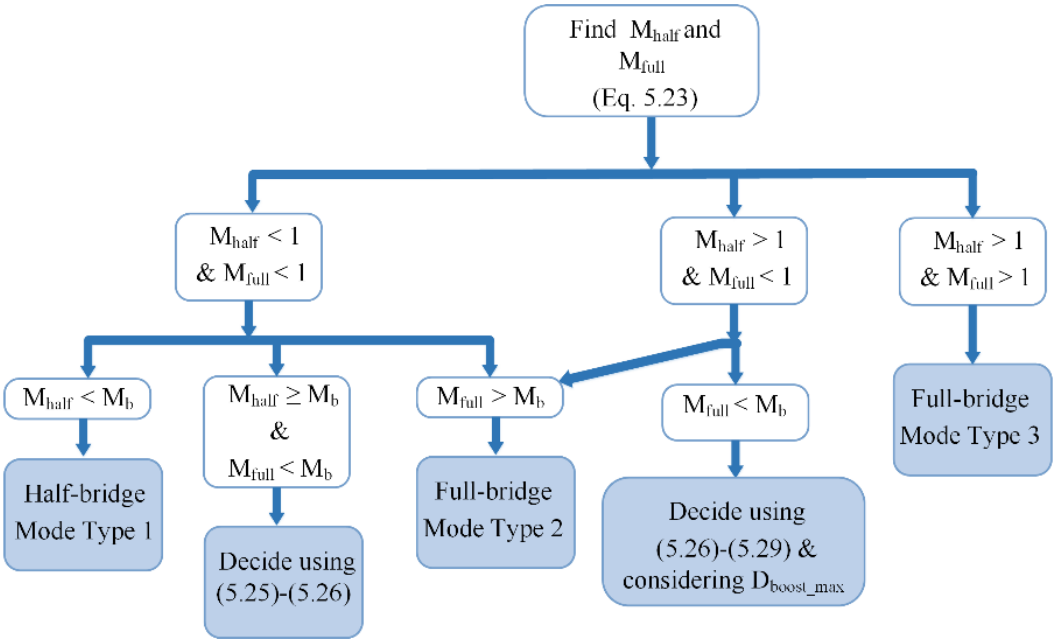


Figure 5-12. Proposed RBOC controller flow chart

If both the voltage gains are less than unity, the first step is to see if the converter needs to buck or boost in both structures. For the same voltage gain value, the converter may be required to buck or boost depending on the load condition. Therefore, it is required to find the boundary between the buck and boost operation when the gain is less than unity. This can be done by realising the fact that the maximum voltage gain achievable by the converter during buck mode is when the phase-shift at the primary side is zero and secondary side acts as a diode rectifier for the full-bridge structure. The clamped inductor current and associated switching signals are shown in Figure. 5-13. By leveraging the circuit diagrams and clamped inductor voltages from the previous sections, one can find the gain value, M_b, at the boundary of buck and boost operation by solving (5.24). Also, it should be noted that the gain value derived from (5.24) is also applicable to the half-bridge structure.

$$M_b^2 + aM_b - 1 = 0 \tag{5.24}$$

where,

$$a = \frac{4L_c}{n^2 R_{out} T_{s/2}}$$

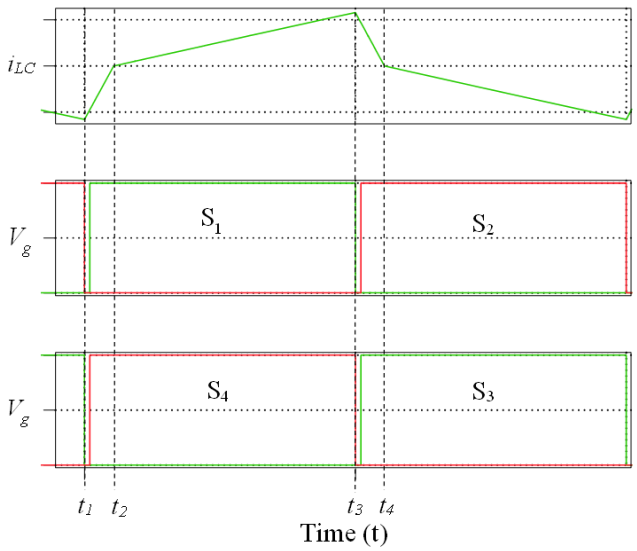


Figure 5-13. Clamped inductor current and switching signals at the maximum voltage gain point during buck operation for the full-bridge structure

If the required gain M_{full} is larger than this boundary gain value, M_b, then the full-bridge structure is chosen since the required secondary phase-shift for boost operation would be lower than the half-bridge case and will result in the optimal one for this operating point. Similarly, if the required gain M_{half} is lower than the boundary gain value, M_b, then the half-bridge structure is chosen since the required phase-shift would be lower than that of the full-bridge case and will result in the optimal one for this operating point. On the other hand, if M_b is smaller than M_{half} and larger than M_{full}, the peak clamped inductor currents for both structures are calculated. Since $M_b < M_{half}$ and $M_b > M_{full}$, the converter in half-bridge structure is in type 2 mode and the converter in full-bridge structure is in type 1 mode. Therefore, the peak inductor current for the half-bridge and full-bridge structure can be found using (5.25) and (5.26), respectively. Now, the controller chooses the converter structure and corresponding operational mode which would result in lower inductor peak current.

$$i_{peak\_half} = \frac{(V_{in}/2 + nV_{out})D_a T_{s/2}}{L_c} \tag{5.25}$$

$$i_{peak-full} = \frac{nV_{out}D_2 T_{s/2}}{L_c} \tag{5.26}$$

For the case when M_{half} is greater than unity and M_{full} is less than unity, the first check is if M_{full} is lower or larger than M_b. In the case when $M_{full} > M_b$, the proper choice is again the full-bridge structure since the phase-shift duty cycle will be much lower than the half-bridge case. For the case when $M_{full} < M_b$, the converter will be operating in type 3 and type 1 mode for the half-bridge and full-bridge structure, respectively. For this case, the half-bridge or full-bridge structure is chosen by comparing the corresponding inductor peak current values within the pre-defined phase-shift, D_{boost_max}, for the half-bridge structure. The inductor peak current for the full bridge in buck mode can again be found with (5.26). For the half-bridge case, first it is determined whether the converter operates in CCM or DCM. At the boundary between CCM and DCM, the clamped inductor current hits zero when S_1 and S_4 turn on and S_2 and S_3 turn off and vice versa. Therefore, at the boundary, the converter behaves as a non-isolated boost converter in CCM mode and the average output current at the boundary, I_{OB}, can be found using (5.27). If the average output current, I_O, is smaller than I_{OB}, then the converter operates in DCM, otherwise it is in CCM. The clamped inductor peak current for the half-bridge structure in CCM and DCM can be found using (5.28) and (5.29), respectively.

$$I_{OB} = \frac{1}{2} i_{peak}(1-D) \tag{5.27}$$

where,

$$i_{peak}\text{: inductor peak current} = \frac{nV_{in}DT_{s/2}}{4L_c}$$

$DT_{s/2}$: Phase-shift between S_1 and S_5 = t_3 - t_1 (from Figure. 5-11)

$$i_{peak-half}(CCM) = \frac{V_{in}(D - D_a)T_{s/2}}{2L_c} \tag{5.28}$$

$$i_{peak-half}(DCM) = \frac{V_{in}DT_{s/2}}{2L_c} \tag{5.29}$$

For the case when M_{half} and M_{full} are both greater than unity, the full-bridge structure is chosen as this would always result in lower phase-shift, thus lower clamped inductor current than that of the half-bridge structure. Figure. 5-14 compares the simulated clamped inductor peak current for the proposed control and DPS control for the input voltage of 550V. The output DC current is kept constant to 25 A for all these points, i.e., the converter is charging the EV battery with constant current (CC). Figure. 5-14 shows that the clamped inductor peak current is much lower with the proposed control at lower output voltages compared to using DPS control. This is because the proposed control allows bridge reconfiguration and thus the input voltage is effectively halved at the clamped inductor terminal in a half-bridge structure compared to the full-bridge structure. Therefore, the voltage across the clamped inductor while the inductor current magnitude is rising is much lower than that of the full-bridge case. For instance, when the output voltage is 200V, and the transformer turns-ratio is 1.3:1, the voltage across the clamped inductor while current is rising is 15 V with the proposed RBOC strategy in half-bridge structure. With DPS, the voltage across the clamped inductor is 290 V during the current rise in positive magnitude at the same operating point in full-bridge structure. The proposed control adopts DPS at 275 V output and over, and therefore, the clamped inductor peak current values are the same and not shown.

5.3.2 Closed-loop Control

Figure. 5-15 shows the proposed closed-loop control set-up. The EV communicates the information regarding measured battery terminal voltage, V_o, measured battery current, I_o, and

required current, I_{ref}, to the controller. The EV also provides constant current (CC)-mode termination voltage, i.e., the voltage reference value, V_{ref}, at which the battery terminal voltage will be kept constant during constant voltage (CV)-mode. Moreover, the input voltage to the converter, V_{in}, which is the output voltage of the BESS, is also communicated to the controller. The controller then uses these parameters to calculate the required duty cycles and phase-shift angles for all the active switches in the RBOC block using the algorithm in Figure. 5-12.

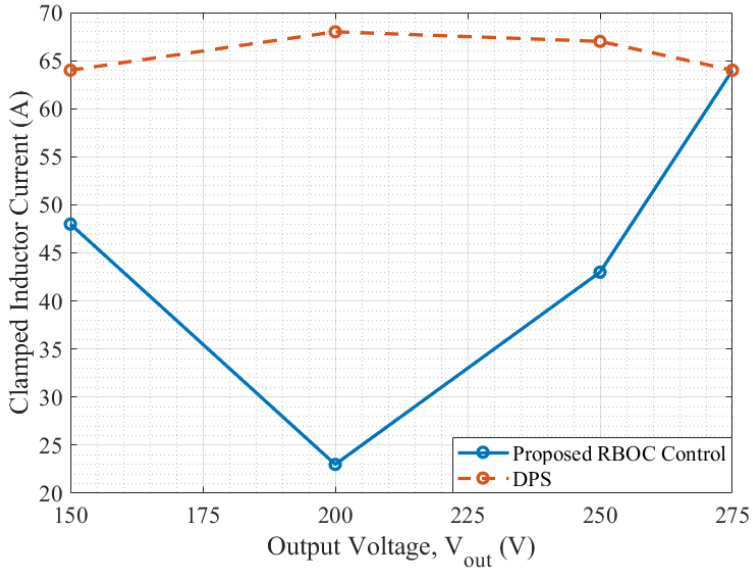


Figure 5-14. Clamped inductor peak current for the input voltage of 550V for the proposed RBOC control and DPS.

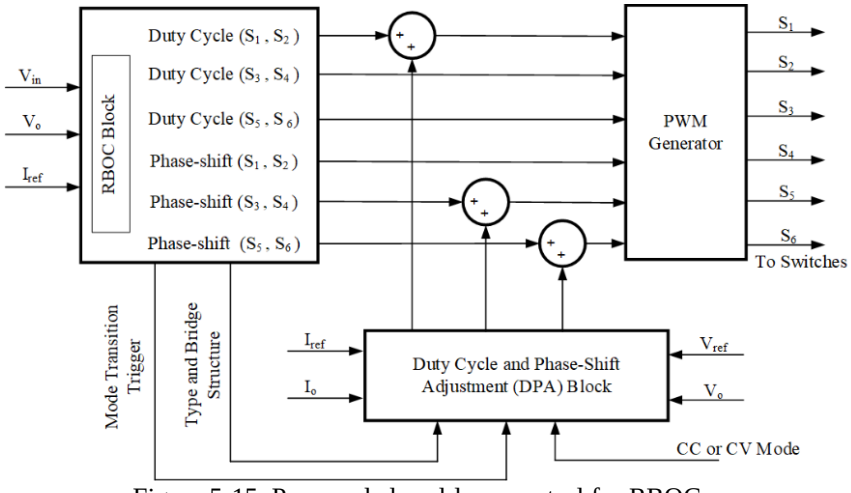


Figure 5-15. Proposed closed-loop control for RBOC

The RBOC block estimates the duty cycles and phase-shift angles very close to the required value. Precise closed-loop control can be achieved by adding small adjustments from the Duty Cycle and Phase-Shift Adjustment (DPA) Block. However, not all the duty cycles and phase-shift angles need to be adjusted in any given mode of operation. For instance, the duty cycle of the switches S_1 and S_2 should be slightly adjusted during Type-1 buck mode of operation in half-bridge structure as explained in Section 5.1.1. But in the other cases of the half-bridge structure, these switches operate with 50% duty cycle, and thus do not need adjustment. Also, in the full-bridge structure, all the switches operate with 50% duty cycle and only the phase-shift angles should be adjusted – parameters which do not need adjustment will have an output of zero from the DPA block. Table 5-1 summarizes the controlled parameters for different mode of operations.

Table 5-1: Controlled Parameters Which Require Closed-Loop Adjustment

Type and Bridge Structure	Controlled Parameter for Closed-Loop Adjustment
Type 1 (Half-Bridge)	Duty cycle of S_1 and S_2 (D_c)
Type 2 (Half-Bridge)	Phase-shift angle of S_5 and S_6 (D)
Type 3 (Half-Bridge)	Phase-shift angle of S_5 and S_6 (D)
Type 1 (Full-Bridge)	Phase-shift angle of S_3 and S_4 (D_1)
Type 2 (Full-Bridge)	Phase-shift angle of S_5 and S_6 (D)
Type 3 (Full-Bridge)	Phase-shift angle of S_5 and S_6 (D)

The DPA block consists of two PI controllers for CC and CV mode of operations. In CC-mode, the inputs to the corresponding PI controller are I_{ref} and I_o, and for CV mode, the inputs to the PI controller during CV mode are V_{ref} and V_o. The RBOC block also provides information regarding the operational mode (type and bridge structure) and a flag if mode transition is required. Moreover, the EV provides the information if the battery should be charged in CC or CV mode. These PI controllers are activated and reset using this information. The PI controllers are active during steady-state operations to fine-tune the duty cycle and phase-shifts depending on the mode and bridge structure and are reset during mode transitions, e.g., when the converter moves from

half-bridge structure to full-bridge structure. When such mode transition is triggered, the PI controllers are disabled, and the outputs of the DPA block are set to zero.

During mode transition, the RBOC block outputs the calculated duty cycles and phase shift angles in small steps for a smooth transition. For instance, when the converter operates in half-bridge structure in type 3-boost mode, the switch S_4 is always turned-on and S_3 is always turned-off, and the secondary side is phase-shifted with respect to the primary side. If the converter moves from the half-bridge to the full-bridge structure, the converter operating point will fall into type 1-buck mode. In this case, the switches S_3 and S_4 will be operated at 50% duty cycle and will be phase-shifted with respect the first leg. The secondary side is also phase-shifted as explained in Section 5.1.1. To achieve a smooth transition, the following steps are taken:

1) First, the switches S_3 and S_4 are switched with 50% duty-cycle while the internal phase-shift is 180°, i.e., the second leg is out of phase with respect to the first leg at the primary side.

2) Next, the phase shifts are decreased slowly by around 10° until the estimated duty cycle is achieved. The interval of each step can be adjusted according to the behavior of the converter.

3) Finally, the corresponding PI-controller is activated to fine tune the controlled parameter.

5.4. Simulated and Experimental Validation

In this section, the proposed RBOC strategy is validated with simulated and experimental results. For this purpose, a 10 kW semi-DAB converter is built along with a simulation model in PLECS/MATLAB. The converter specifications are provided in Table 5-2. The experimental setup is built onto a 4-layer PCB and split into primary and secondary sides as shown in Figure. 5-16 (a). A zoomed-out version of the setup is also presented in Figure. 5-16 (b). The prototype is designed carefully to reduce parasitic inductance in the DC link as increasing inductance leads to an increase in voltage overshoot during switching transients. For this purpose, high-frequency

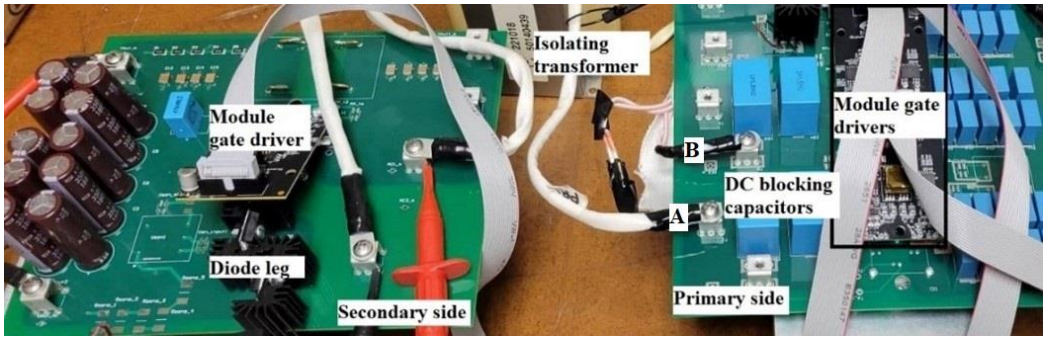
capacitors are placed in the proximity to the switching modules. These capacitors function as decoupling capacitors, and film capacitor are ideal choice for this application as they have lower parasitic inductance compared to electrolytic ones. Furthermore, copper planes are used instead of traces in the PCB design. Large copper planes can carry high current as well as lead to lower inductance due to flux cancellation between layers.

Table 5-2: Semi-DAB Converter Parameters

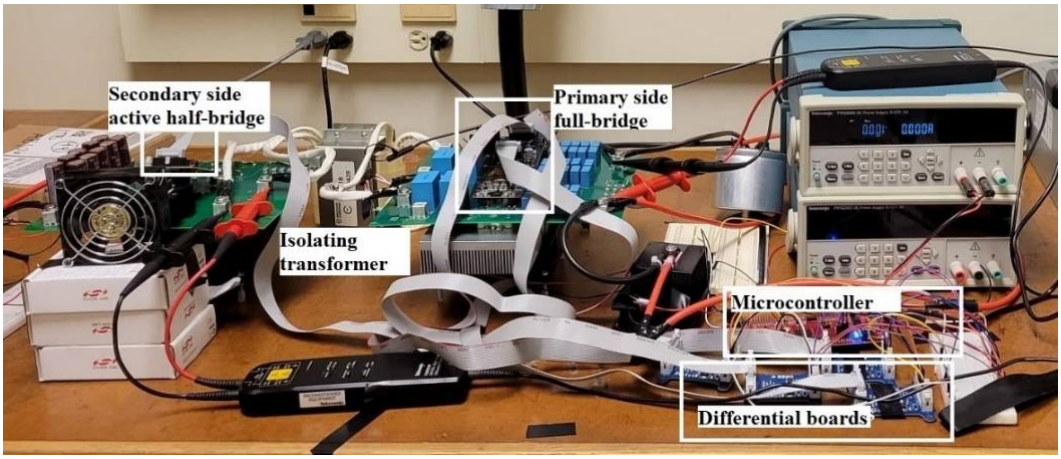
Parameters	Value
Input voltage (V_{in})	350V-550V
Output voltage (V_{out})	150V-450V
Maximum output current (I_o)	25 A
Maximum output power (P_{out})	10 kW
Switching frequency (f_s)	100 kHz
Transformer turns ratio (n)	13:10
Transformer leakage inductance (L_s)	6 µH
DC-blocking capacitor	2 µF
Primary and secondary side active half-bridges	CAB011M12FM3
Secondary side diodes (Quantity:4)	C4D40120D

A nominal 500 V BESS is connected to the input of the converter. Thus, the nominal input voltage is 500 V, and the input voltage range is 350 V to 550 V. The nominal output voltage (of the BEV battery) is 400 V, with an allowable range of 150 V to 450 V, as most of the commercially available DC fast chargers have the output voltage range of 50 - 500 V in accordance with the available standards [75]. Since a common fast-charging scenario is high SOC (and thus voltage) in the stationary BESS and low SOC (and thus voltage) in the BEV battery, it is important to improve the operational efficiency of the converter at these operating points. In general, the low output voltage efficiencies could be improved using a step-down transformer with high turns-ratio when the input voltage is high. However, this is not applicable in this application because this converter needs to accommodate wide input and output voltage variation and provide high output voltage (e.g., 400 V) even when the input voltage is low (e.g., 350 V). Therefore, the transformer turns ratio is chosen such that the converter can provide that output voltage without exceeding the

D_{boost_max} limit explained earlier when the input voltage is 400 V and the output voltage is 400 V. This turns ratio is calculated to be 1.3:1. Furthermore, the clamped inductor value is chosen such that it can be included within the transformer leakage inductance. The two terminals of the primary side, A and B in Figure. 5-15 (a) correspond to nodes A and B in Figure. 5-1.



(a)



(b)

Figure 5-16. Experimental Setup (a) primary and secondary side, and (b) experimental setup

5.4.1 Phase-shifts and Duty Cycles

In this subsection, the calculated phase-shifts from Section 5.1 are compared with the simulated and experimental results. This shows how accurately the controller can estimate the required phase-shifts and duty cycles parameters at any given operating point. This is essential to identify the operating modes of the converter at any operating point. The estimated parameters along with simulated and experimental results are tabulated in Table 5-3 for three operational

modes (Type 1-3). At all these operating points, the converter operates again in CC mode with the output current of 25 A, i.e., the output power changes with the output voltage, which is the typical mode of operation for a CC EV charger. It can be seen that the controller can determine the required phase-shifts and duty cycles and hence, clamped inductor peak current very close to ones obtained by simulation and experiment. Therefore, the DPA block is only required to finely adjust the required duty cycles and phase-shifts.

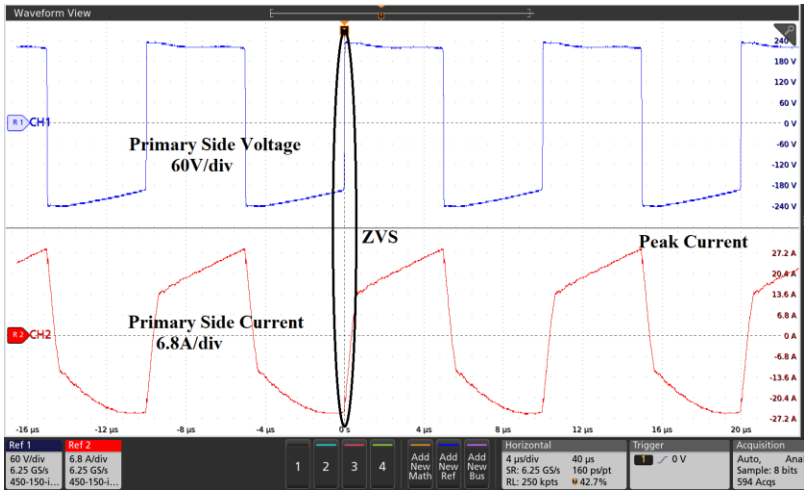
Table 5-3: Validation of Estimated Parameters with Simulation and Experiment

Input Voltage (V)	Output Voltage (V)	Controller (Estimated)	Simulation	Experimental
450	150	Structure: Half-bridge Mode: M'<1 and Boost (Type 2) D: 0.14 Inductor peak current: 31 A	Structure: Half-bridge Mode: M'<1 and Boost D: 0.11 Inductor peak current: 29 A	Structure: Half-bridge Mode: M'<1 and Boost D: 0.13 Inductor peak current: 28 A
500	200	Structure: Half-bridge Mode: M'>1 and Boost (Type 3) D: 0.17 Inductor peak current: 26 A	Structure: Half-bridge Mode: M'>1 and Boost D: 0.14 Inductor peak current: 25 A	Structure: Half-bridge Mode: M'>1 and Boost D: 0.15 Inductor peak current: 29 A
550	275	Structure: Full-bridge Mode: M' <1 and Buck (Type 1) D_1: 0.61, D_2: 22 Inductor peak current: 63 A	Structure: Full-bridge Mode: M' <1 and Buck D_1: 0.60, D_2: 22 Inductor peak current: 64 A	Structure: Full-bridge Mode: M' <1 and Buck D_1: 0.59, D_2: 22 Inductor peak current: 64 A

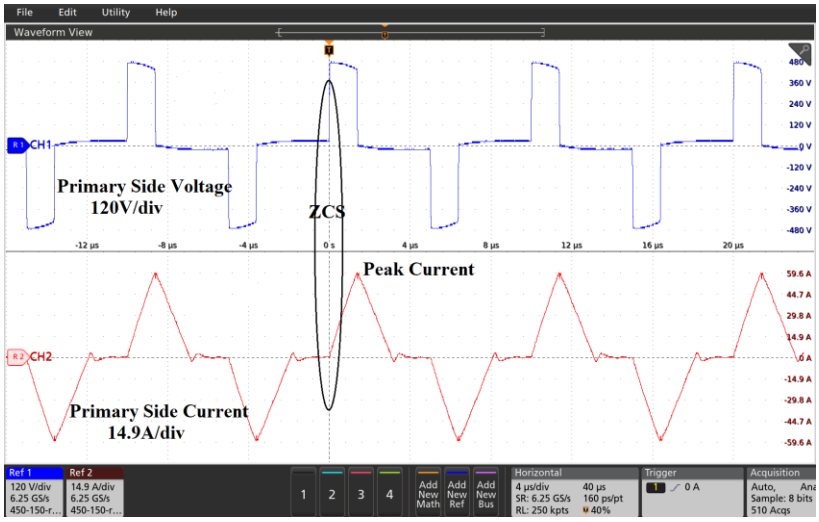
5.4.2 Experimental Waveforms

The experimental validation for the three operational modes shown in Table 5-3 are provided by the transformer primary side voltage and current, as shown in Figures. 5-17 to 5-19. For the first operating point when M'<1 and boost mode for the half-bridge structure with V_{in}=450 V and V_{out}=150 V, the experimental waveforms are shown in Figure. 5-17 (a). The converter is operating in CCM, and the switches turn on with ZVS. This is because the current is negative just before the switch turns on, and the negative current goes through the body diode. This makes the voltage

across the switch zero. Therefore, when the switch is turned on, it turns on with zero voltage, hence ZVS.



(a)



(b)

Figure 5-17. Transformer primary side voltage and current for Vin: 450 V and Vout: 150 V (a) for the half-bridge structure (M'<1 and Boost, type 2) determined using the proposed control and (b) using DPS control (full-bridge structure, M'<1 and buck, type 1)

The peak value of the voltage at the transformer primary side measured between A and B as in Figure. 5-16 (a) is half of the input voltage as explained in Section 5.1. In contrast, the waveforms generated using the regular DPS control are shown in Figure. 5-17 (b) for the same operating point. Figure. 5-17 (b) shows that the converter operates in DCM and the peak current under DPS control is more than twice that of the proposed control at this operating point. Therefore, switches S_1 and

S_2 would turn off with more than twice the current with DPS compared to the proposed control. The primary side voltage and current for the second operating point when M'>1 and boost for the half-bridge structure are shown in Figure. 5-18. For this case, the peak current occurs when then secondary side switches turn-off unlike the previous case. This results in high turn-off losses at the secondary side as explained earlier. Finally, the primary side voltage and current waveforms for the third operating point when M'<1 and buck mode for the full-bridge structure is presented in Figure. 5-19. It can be seen that the converter operates in DCM, and the peak current occurs again when the leading leg switches turn-off like the first case as explained in Section 5.1.

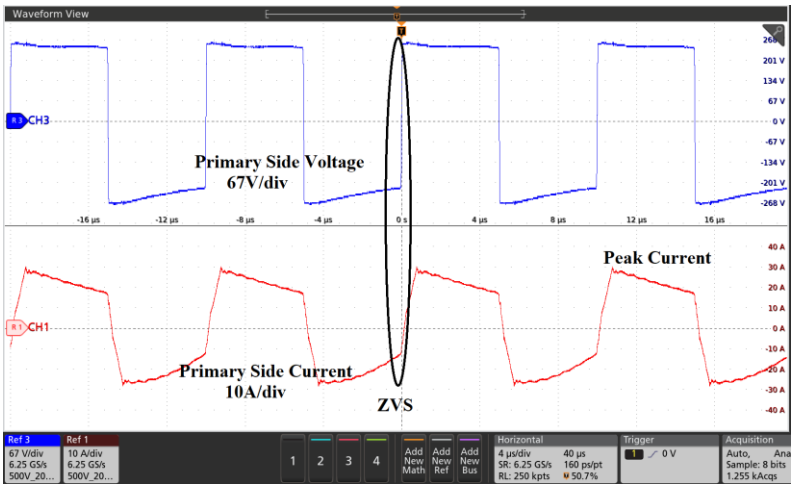


Figure 5-18. Transformer primary side voltage and current for Vin: 500 V and Vout: 200 V for the half-bridge structure (M'>1 and Boost, type 3)

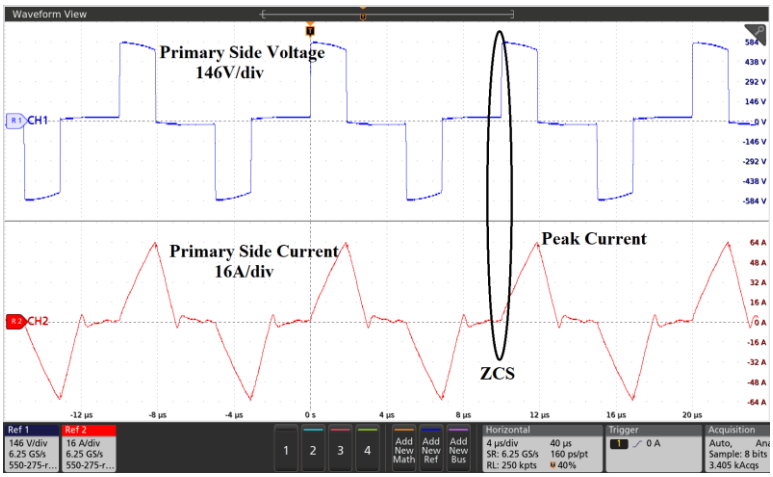
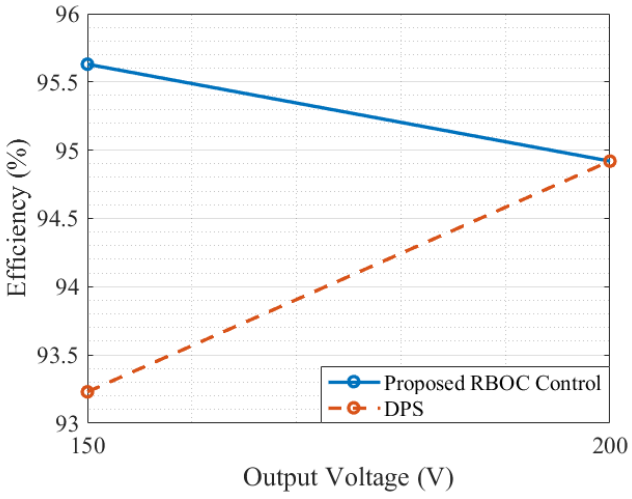


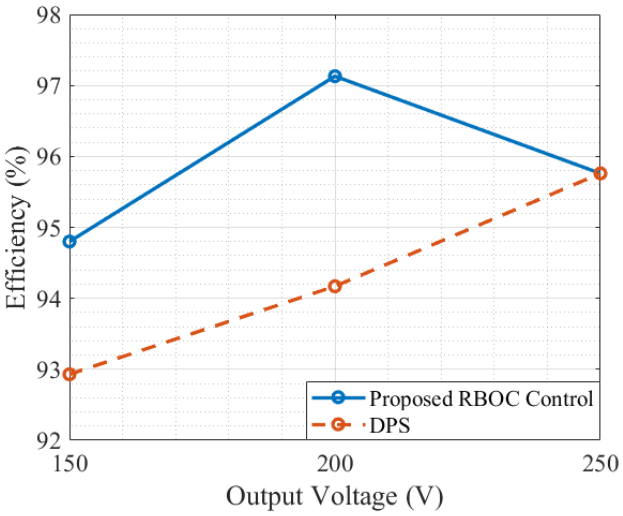
Figure 5-19. Transformer primary side voltage and current for Vin: 550 V and Vout: 275 V for the full-bridge structure

5.4.3 Efficiency

Figure. 5-20 shows the experimental efficiency results of the proposed RBOC strategy and the well-known DPS control for three different input voltages in CC mode providing 25 A output current. It should be noted that the proposed control method adopts DPS at the points where the efficiency curves intersect, i.e., the proposed control is similar to DPS at and above 200 V, 250 V, and 275 V output for input voltages of 450 V, 500 V, and 550 V, respectively. The efficiency is calculated by measuring the input power from the DC source: Sorensen SGX-600V-25 A and summing up the power consumed by three parallel connected Chroma 63800 series AC+DC loads. It is evident that the proposed control strategy results in much better efficiency of the converter when the input voltage is high and output voltage is low compared to DPS. For instance, the proposed control strategy is around 3% and 3.5% more efficient at 200 V output compared to DPS for input voltage of 500 V and 550 V, respectively. The largest improvement is at 550 V input voltage, where the proposed control has peak 97.6% efficiency at 200 V output compared to the DPS control that has 94% efficiency at this point.



(a)



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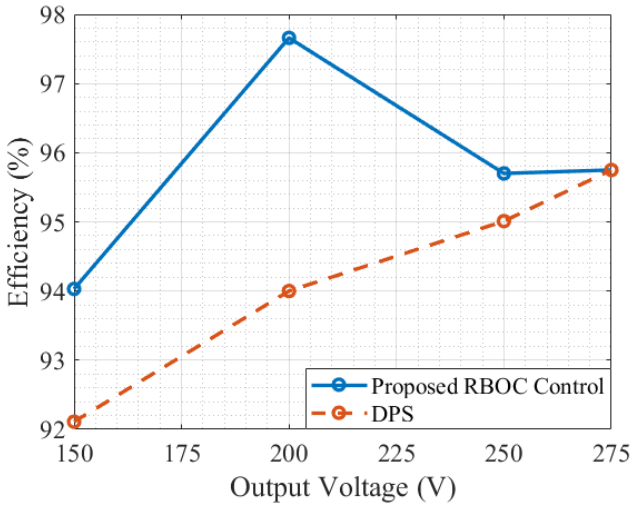


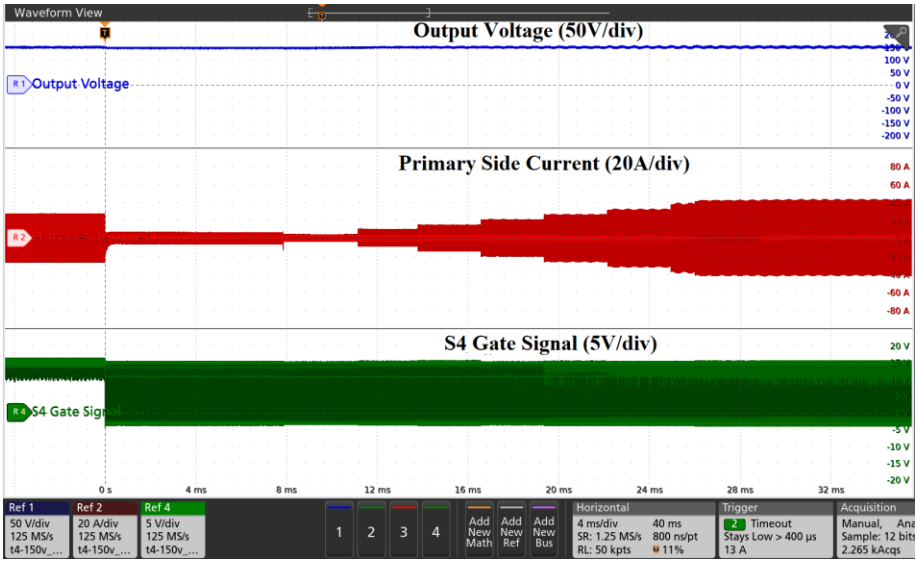
(c)

Figure 5-20. Efficiency comparison between proposed RBOC control and DPS for input voltage (a) 450 V, (b) 500 V, and (c) 550 V

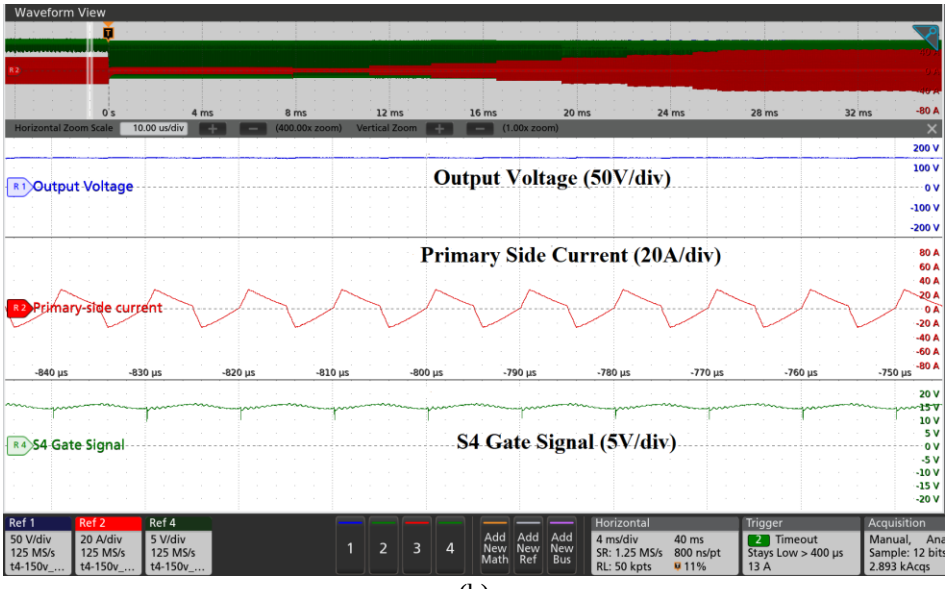
5.4.4 Dynamic Behavior

This subsection shows experimental results for an operating structure transition and a load transition. Since this converter operates in both half-bridge and full-bridge structures, the transition between these two structures should be achieved smoothly. Figure. 5-21 shows the transition from the half-bridge structure to the full-bridge structure. To achieve this transition, the steps in section 5.2.2 are taken, where phase shifts are changed in steps of 10°, and the transition is achieved in

about 26 ms. Figure. 5-21 (a) shows the entire transition process. Figure. 5-21 (b) shows the converter steady-state operation in type 3-boost mode in half-bridge structure just before the mode transition is triggered. Figure. 5-21 (c) shows the steady-state operation in type 1-buck mode in full-bridge after the mode transition is achieved. Figure. 5-22 shows the load transition during CV mode, when the current jumps from 15 A to around 6A. Again, to achieve a smooth transition, the phase shifts are adjusted by 10° in each step of 2 ms.



(a)



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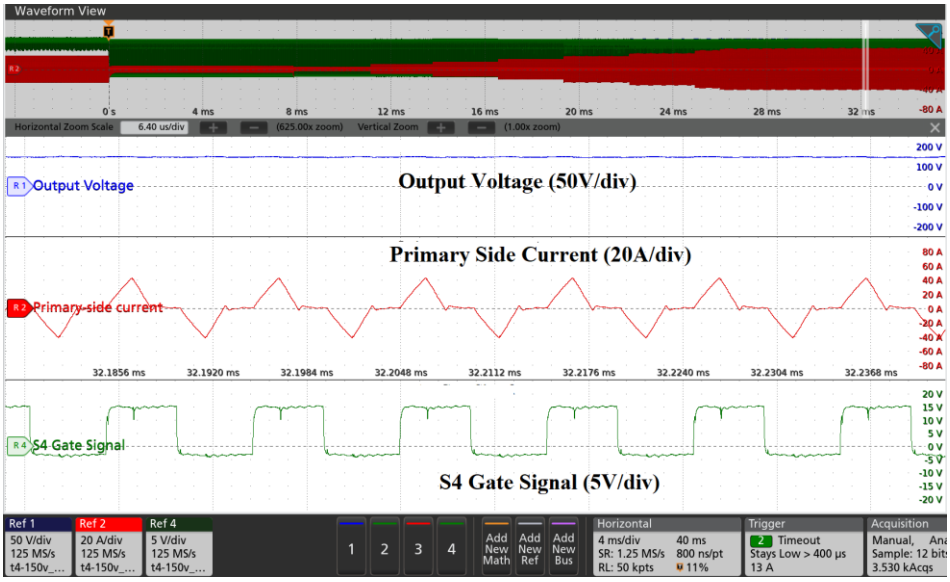


(c)

Figure 5-21. The mode transition process from half-bridge to full-bridge structure (a) the entire process, (b) steady-state just before the transition in type 3-boost mode, and (c) steady-state just after the transition in type 1- buck mode

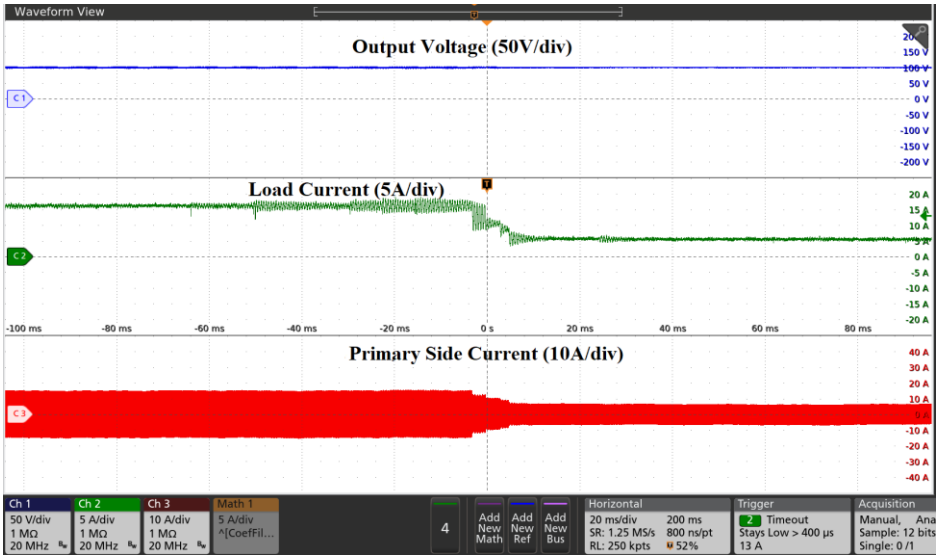


Figure 5-22. The load transition process when the load changes by 50% in CV mode

5.5. Summary

A novel control strategy for semi-DAB DC/DC converters interfacing BESS and BEV called RBOC is proposed in this chapter. The goal is to ensure high efficiency at all operating points, especially at the lower output voltages while the input voltage is high. The analysis provided in this chapter can also be used to identify the operational modes of a semi-DAB converter along

with required phase-shifts and duty cycles in real time without searching for the entire space of phase-shift duty cycles. The proposed RBOC strategy is validated with a 25 A rated prototype providing 10 kW of power at 400 V output. The control strategy is experimentally shown to have up to 3.5% higher efficiency than the well known DPS control at operational points with high input voltage and low output voltage, with a peak efficiency of 97.6%. Overall, the experimental results show higher efficiencies over an ultra-wide range of output voltages even when the input voltage varies over a wide range in comparison to the DPS control.

Chapter 6

Proposed Variable Turns-ratio Multi-Winding Semi-DAB with Optimal Control Strategy

6.1. Variable Turns-ratio Converters

Another effective solution to tackle the varying input and output voltages and high circulating current is the use of variable turns-ratio transformers using multiple windings. A variable turns-ratio DAB converter with multiple windings is built and tested in [164]. The paper also identifies different solutions to connect the windings, such as relays, MOSFETs and IGBTs. This multiple winding structure is placed at the high voltage secondary side to reduce conduction losses. However, the converter suffers from conduction losses at each turns-ratio orientation. An electromagnetic relay based multi-winding planar transformer has been used in DAB converter to enhance the efficiency in [165]. Again, each winding uses one relay, and the multiple winding structure is again placed in high voltage secondary side. However, the designed prototype is of low power of around 200 W, and thus the electromagnetic relays can be smaller. On the other hand, large relays need to be used in a high-power application with very slow dynamic response. In [166], a two-winding transformer is used, and in [167], a three-winding transformer is used with an additional secondary side diode bridge leg in the LLC resonant converter for the BEV charging application. The turns-ratios are controlled with a four-quadrant switch, i.e., two back-to-back bidirectional switches. In both of these references, the multiple winding structures are put in the secondary side even though RMS-current is high in the secondary side of the LLC converter. Since both papers demonstrated the results with a low current application (maximum current is 4A), the four-quadrant switches do not have high conduction losses. However, with the high current DCFC application, these turns-ratio controlling switches will introduce high conduction losses and the benefit of the reduced circulating current is outweighed by these additional switch losses.

Based on the literature on multi-winding converters providing variable turns-ratio, this thesis proposes the use of multi-winding transformer in a semi-DAB converter to reduce circulating

current and the switching losses during buck and boost operation. For the semi-DAB converter, each winding should be connected with a four-quadrant switch at the secondary side due to secondary side phase shift. Therefore, high conduction losses are always present irrespective of the turns-ratio. Thus, this thesis presents a new semi-DAB converter with multi-winding transformer for high power applications with widely varying input and output voltages. The proposed converter uses only one four-quadrant switch for a two-winding transformer instead of two and the multi-winding structure is located at the high voltage primary side. This eliminates the additional conduction losses at certain turn-ratio configuration and reduces losses at others due to lower primary side current. Therefore, this chapter discusses the following contributions of this thesis:

1) This thesis proposes a multi-winding configuration of the semi-DAB converter where the multiple winding structure is moved to the high voltage primary side. Moreover, the two-winding structure only uses one four-quadrant switch in such as way that the four-quadrant switch is only active when the input voltage is high and output voltage is low, i.e., with lower primary side current.

2) A control strategy is proposed to choose the appropriate turns-ratio, i.e., bridge structure at the primary side to reduce overall losses of the converter system by reducing primary side peak and rms current.

6.2. Topology and Operational Principle

6.2.1 Proposed Topology

The proposed semi-DAB converter with two windings at the primary side is presented in Figure. 6-1. The primary side consists of three half-bridge legs (HBLs) to accommodate the two

transformer windings. HBL 1 consists of switches S_{w1} and S_{w2}, HBL 2 contains S_{w3} and S_{w4}, and HBL 3 contains S_{w5} and S_{w6}. The first winding is connected to the midpoints of HBL 1 and HBL 2, and the second winding is connected between the midpoints of HBL 2 and HBL 3. Each of the windings is connected with a DC blocking capacitor (C_{dc1} and C_{dc2}) to prevent possible transformer saturation with voltage mode control. The leakage inductance of the transformer associated with the windings are used as the clamped inductors, L_{c1} and L_{c2}. At any point in time, only two HBLs are involved in creating the primary side bridge configuration. Moreover, HBL 1 is always used in the bridge formation and hence, the upper winding is always active. Therefore, the converter can provide effective turns ratios of $n_1 : n_3$ and $(n_1 + n_2) : n_3$.

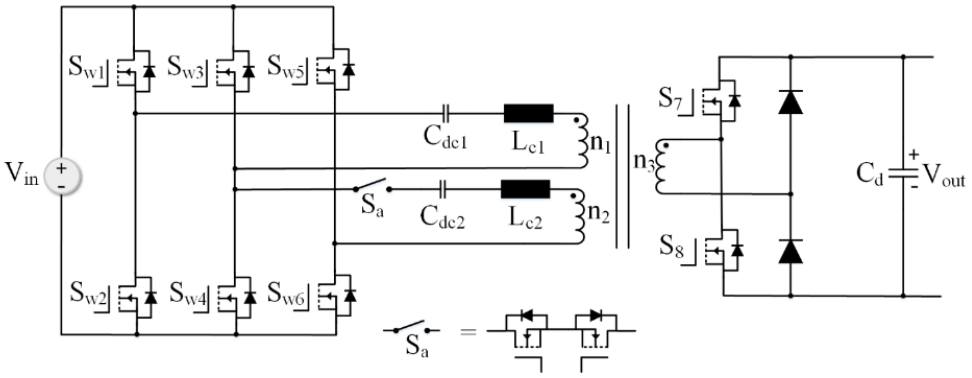
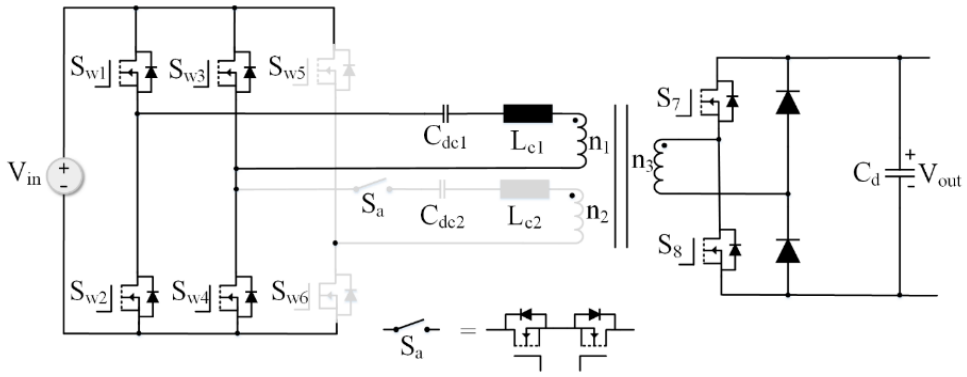


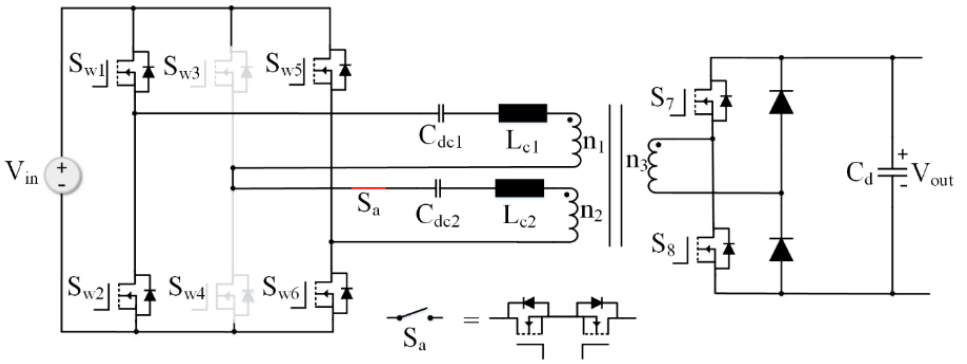
Figure 6-1. Proposed multi-tap semi-DAB converter

In order to block the current flow through the diodes of HBL 3 when only the first winding is active, an additional four-quadrant switch, S_a is used at the winding 2 terminal creating a two turns-ratio transformer. A four-quadrant switch can be composed of two back-to-back MOSFETs with their sources connected together, as shown in Figure. 6-1. This will allow the control of both MOSFETs with only one gate driver. This additional switch is turned on to activate the turns ratio of $(n_1 + n_2) : n_3$. The secondary side of the converter is the same as the standard semi-DAB converter with one active HBL and one diode bridge. Therefore, Figure. 6-2 (a) shows the converter when the upper winding is active (with switches S_{w5} and S_{w6} always off) and Figure. 6-

2 (b) shows the converter when both windings are conducting (with switches S_{w3} and S_{w4} always off). It can be seen from Figure. 6-2 that the primary side of the proposed converter behaves as the standard semi-DAB converter, i.e., only two HBLs are active at a time with varying turns-ratio, DC blocking capacitor, and clamped inductor values.



(a)



(b)

Figure 6-2. Proposed converter structures to provide (a) $n_1 : n_3$ turns ratio, and (b) $(n_1 + n_2) : n_3$ turns ratio

6.2.2 Operational Principle

A semi-DAB converter can operate in both buck and boost mode as explained in the previous chapter. Depending on the input and output voltage, the proposed control method will again operate this converter in the half-bridge or full-bridge structure with two unique turns-ratios. The voltage gain, M', referred to the primary side for the full-bridge and the half-bridge structure defined in (5.1) and (5.2), respectively can be used for this multi-winding semi-DAB structure. V_{out} and V_{in} are again output and input voltage, however, n is the effective transformer turns-ratio.

For instance, while only the first tap is active, i.e., the turns-ratio is $n_1:n_3$, n is n_1/n_3, whereas n is $(n_1+n_2)/n_3$ when the turns-ratio is $(n_1+n_2):n_3$.

In a full-bridge structure with both winding orientations, the converter can operate with dual phase-shift control, which is lost in the half-bridge structure like the single turns-ratio structure. Therefore, in the proposed control for the multi-winding structure, the converter in half-bridge structure again operates with variable duty cycle instead of phase-shift control in buck mode of operation. Moreover, the three different modes of operation of the semi-DAB converter with single turns-ratio derived in the previous chapter are still valid for the multi-winding structure. This is due to the fact that the proposed converter primary side is the same as the standard semi-DAB as shown in Figure. 6-2 at any specific turns-ratio. For the single winding case, S_1, S_2, S_3, and S_4 from Figure. 5-1 would represent S_{w1}, S_{w2}, S_{w3}, and S_{w4}, respectively, and C_{dc} is equal to C_{dc1} and L_c would be L_{c1}. For the case when both windings are active S_1 and S_2 again represent S_{w1} and S_{w2}, however, S_3 and S_4 will represent S_{w5} and S_{w6}. Moreover, L_c will be the combination of L_{c1} and L_{c2} and C_{dc} will be as if C_{dc1} and C_{dc2} are in series.

6.3. Proposed Control Strategy

In this section, a control strategy is proposed to decide on the primary side structure of the proposed converter. In this type of converter, most losses come from the turn-off losses due to the high turn-off currents as the switches can be turned on with zero voltage (ZVS) and zero current (ZCS). The primary goal is, therefore, to reduce the peak clamped inductor current in order to minimize the turn-off losses, and thus improving efficiency. Also, the rms current decreases with decreasing peak current, hence the conduction losses also decrease. Furthermore, the phase-shift duty cycle during boost operation when the gain is larger than unity, i.e., during type 3 operational mode, is also limited to a pre-defined value to reduce the secondary side losses. This value changes

depending on the turns-ratio as the secondary side current will be different at two different turns ratios.

The proposed controller design is summarized in the flow chart of Figure. 6-3. First, the required voltage gains for the half-bridge and full-bridge structure for both turns-ratio are calculated as in (6.1) for any operating point. The voltage gains M_1 and M_2 represent the voltage gains for the half-bridge and full-bridge structure, respectively when the turns ratio is $(n_1+n_2) : n_3$. The voltage gains for the half-bridge and full-bridge structure when the turns-ratio is $n_1 : n_3$ are represented by M_3 and M_4. The primary structures (PS) associated with voltage gains M_1, M_2, M_3, and M_4 are called PS_1, PS_2, PS_3, and PS_4, respectively.

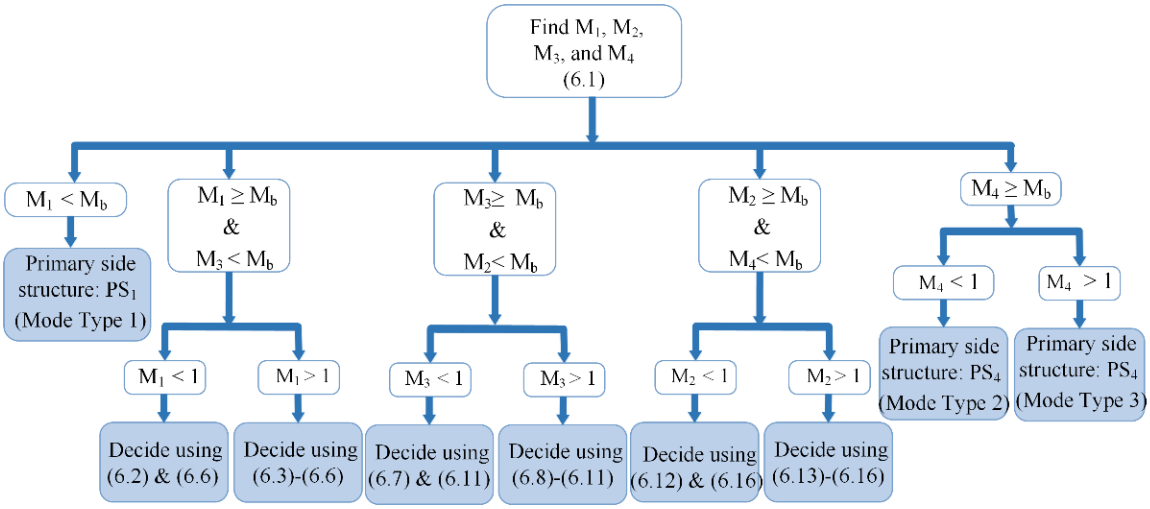


Figure 6-3. Proposed controller flow chart

$$
\begin{aligned}
M_1 &= \frac{(n_1+n_2)V_{out}}{n_3 V_{in}/2} \\
M_2 &= \frac{(n_1+n_2)V_{out}}{n_3 V_{in}} \\
M_3 &= \frac{n_1 V_{out}}{n_3 V_{in}/2} \\
M_4 &= \frac{n_1 V_{out}}{n_3 V_{in}}
\end{aligned}
\tag{6.1}
$$

The first step of the proposed control algorithm is to compare the required gains for different primary bridge structures with the boundary gain value, M_b. This is the gain value at the boundary of buck and boost operation when the required gain is less than unity. The equation presented in (5.24) can also be used for the multi-winding structure since this value is independent of the turns-ratio and bridge structure when the leakage inductance is used as the clamped inductance value. This is due to the fact that leakage inductance is proportional to the square of the turns-ratio.

If the required gain M_4 is larger than this boundary gain value, M_b, then the full-bridge structure with turns ratio $n_1 : n_3$, PS_4, is chosen since the required secondary phase-shift for boost operation would be lower than the rest of the three possible bridge structures and thus will be optimal for this operating point. Similarly, if the required gain M_1 is lower than the boundary gain value, M_b, then the half-bridge structure with turns-ratio $(n_1+n_2) : n_3$, PS_1, is chosen since the required phase-shift would be lower than that of the rest of the cases and will be optimal for this operating point. On the other hand, the boundary gain value, M_b can fall into in-between values, and three different such intervals are identified in the proposed control. For instance, the gain values in the first interval are larger than M_1 and smaller than M_3, the second interval comprises the gain values larger than M_3 but smaller than M_2, and the final interval is the gains larger than M_2 but smaller than M_4. To identify these three intervals, it is assumed that the number of turns at two primary side windings are not equal, i.e., $n_1 > n_2$, and this would be the case in such a design. For the case when the number of turns in the windings are equal, the gain values, M_2 and M_3 would be the same and therefore, the benefit of having an additional winding reduces.

When the boundary gain value is smaller than M_1 and larger than M_3, i.e., M_b falls into the first interval, the peak clamped inductor currents for both structures are calculated and compared. For the structure with voltage gain M_1, the derivation of peak current would depend on M_1 being

less or greater than unity. If M_1 <1, then the PS_1 will be in type 2 mode, otherwise it would be in type 3 mode. For the case when the PS_1 is in type 2 mode, the peak current can be found using (6.2) by leveraging (5.25). For the case when M_1 > 1, i.e., in type 3 mode, first it is determined whether it is in CCM or DCM. At the boundary between CCM and DCM, the clamped inductor current hits zero when S_{w1} and S_{w6} turn on and S_{w2} and S_{w5} turn off and vice versa. Therefore, at the boundary, the converter behaves as a non-isolated boost converter in CCM mode and the average output current at the boundary, I_{OB}, can be found using (6.3) based on the equation presented in (5.27). If the average output current, I_o, is smaller than I_{OB}, then the converter operates in DCM, otherwise it is in CCM. The clamped inductor peak current for PS_1 in CCM and DCM can be found using (6.4) and (6.5), respectively by adapting (5.28) and (5.29) for this primary structure arrangement. For the primary structure PS_3 associated with the gain M_3, the converter is in type 1 mode and the peak current can be found using (6.6) by using (5.12) for the half-bridge structure with single winding. Therefore, the appropriate primary structure is chosen from PS_1 and PS_3 that results in the lowest primary peak current within the pre-defined maximum external phase-shift for PS_1 in type 3 mode.

$$i_{peak\_ps1} = \frac{(\frac{V_{in}}{2} + \frac{n_1 + n_2}{n_3} V_{out})}{L_{c1} + L_{c2}} D_a T_{s/2} \tag{6.2}$$

$$I_{OB} = \frac{1}{2} i_{peak} (1 - D) \tag{6.3}$$

where,

i_{peak}: inductor peak current = $\frac{n_1 + n_2}{4n_3(L_{c1} + L_{c2})} V_{in} D T_{s/2}$, $DT_{s/2}$: Phase-shift between S_{w1} and $S_7 = t_1 - t_3$

$$i_{peak-ps1}(CCM) = \frac{V_{in}(D - D_a)T_{s/2}}{2(L_{c1} + L_{c2})} \tag{6.4}$$

$$i_{peak-ps1}(DCM) = \frac{V_{in} D T_{s/2}}{2(L_{c1} + L_{c2})} \tag{6.5}$$

$$i_{peak\_ps3} = \frac{(\frac{V_{in}}{2} - \frac{n_1}{n_3} V_{out})}{L_{c1}} D_c T_s \tag{6.6}$$

For the cases when the boundary gain value is smaller than M_3 and larger than M_2, i.e., M_b falls into the second interval, the peak clamped inductor currents for both structures are again calculated and compared. The above-mentioned argument for PS_1 is now valid here for PS_3. Therefore, the peak inductor current when PS_3 is in type 2 mode can be found using (6.7). Similarly, the peak current for PS_3 as in type 3 CCM and DCM can be found using (6.8) and (6.9), respectively, whereas average output current at the boundary, I_{OB}, can be found using (6.10). The converter with PS_2 operates in type 1 mode in this case and therefore, the peak inductor current would be as in (6.11) by looking at (5.26). Finally, the appropriate primary structure is chosen from PS_2 and PS_3 that results in the lowest primary peak current, however, now within the pre-defined maximum external phase-shift for PS_3 in type 3 mode of operation.

$$i_{peak\_ps3} = \frac{(\frac{V_{in}}{2} + \frac{n_1}{n_3} V_{out})}{L_{c1}} D_1 T_{s/2} \tag{6.7}$$

$$i_{peak-ps3}(CCM) = \frac{V_{in}(D - D_a) T_{s/2}}{2L_{c1}} \tag{6.8}$$

$$i_{peak-ps3}(DCM) = \frac{V_{in} D T_{s/2}}{2L_{c1}} \tag{6.9}$$

$$I_{OB} = \frac{1}{2} i_{peak}(1 - D) \tag{6.10}$$

where,

i_{peak}: inductor peak current = $\frac{n_1}{4n_3L_{c1}}V_{in}DT_{s/2}$

$$i_{peak-ps2} = \frac{(n_1+n_2)V_{out}D_2T_{s/2}}{n_3(L_{c1}+L_{c2})} \tag{6.11}$$

Finally, for the cases when the boundary gain value is smaller than M_2 and larger than M_4, i.e., M_b falls into the third interval, the peak clamped inductor currents for both structures are again calculated and compared. The above-mentioned arguments for PS_1 and PS_3 is now valid here for PS_2. Therefore, the peak inductor current when PS_2 is in type 2 mode can be found using (6.12) by using (5.19). It should be noted that both PS_2 and PS_4 are full-bridge structures. Similarly, the peak current for PS_2 as in type 3 CCM and DCM can be found using (6.13) and (6.14), respectively, and the average output current at the boundary of CCM and DCM, I_{OB} can be calculated using (6.15). The primary structure PS_4 operates in type 1 mode in this case and therefore, the peak inductor current would be as in (6.16). Finally, the appropriate primary structure is chosen from PS_2 and PS_4 that results in the lowest primary peak current, however, now within the pre-defined maximum external phase-shift for PS_2 in type 3 mode.

$$i_{peak\_ps2} = \frac{(V_{in} + \frac{n_1+n_2}{n_3}V_{out})}{L_{c1}+L_{c2}}D_aT_{s/2} \tag{6.12}$$

$$i_{peak-ps2}(CCM) = \frac{V_{in}(D-D_a)T_{s/2}}{(L_{c1}+L_{c2})} \tag{6.13}$$

$$i_{peak-ps2}(DCM) = \frac{V_{in}DT_{s/2}}{(L_{c1}+L_{c2})} \tag{6.14}$$

$$I_{OB} = \frac{1}{2}i_{peak}(1-D) \tag{6.15}$$

where,

$$i_{peak}\text{: inductor peak current} = \frac{n_1 + n_2}{2n_3(L_{c1} + L_{c2})} V_{in} D T_{s/2}$$

$$i_{peak-ps4} = \frac{n_1 V_{out} D_2 T_{s/2}}{n_3 L_{c1}} \tag{6.16}$$

Figure. 6-4 and Figure. 6-5 compare the simulated peak clamped inductor current and the rms current at the transformer, respectively, for the proposed converter with the proposed optimal control with that of the traditional semi-DAB with DPS control for the input voltage of 550 V. In this case, the traditional semi-DAB is the same as the *PS₄* structure. The output DC current is kept constant to 25 A for all points, i.e., the converter is charging the EV battery with constant current (CC). The proposed control adopts the *PS₄*, i.e., the primary side adopts the single tap full-bridge structure at 400 V output and over, and therefore, the clamped inductor peak current values are the same as for the traditional semi-DAB with DPS and are not shown. These results show that the proposed converter and proposed optimal control significantly reduce the peak clamped inductor current and converter rms current at many output voltages, and thus will lead to lower switching and conduction losses. Moreover, it also shows the benefit of moving the auxiliary four-quadrant switch to connect the second winding to the primary side due to much lower rms current compared to the secondary side.

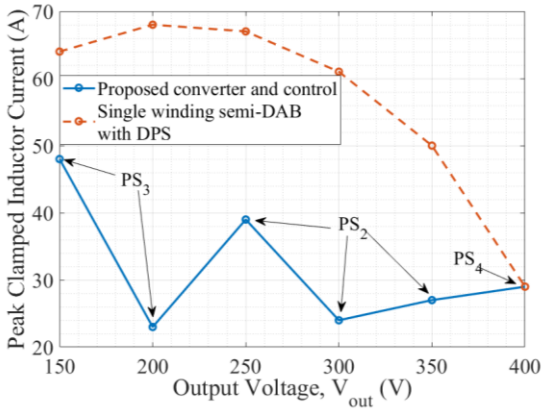


Figure 6-4. Simulated clamped inductor peak current for the input voltage of 550V for the proposed converter with proposed optimal control compared to that of traditional semi-DAB having 13:10 turns ratio with DPS.

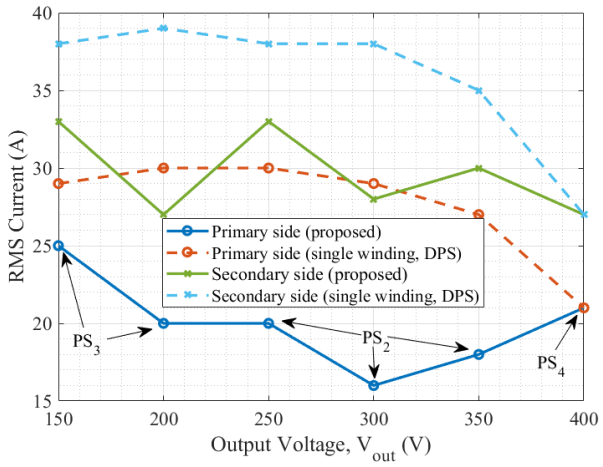


Figure 6-5. Simulated rms current at the primary and secondary side of the transformer for the input voltage of 550V for the proposed converter with n1, n2, and n3 being 13, 4, and 10 with proposed optimal control compared to that of traditional semi-DAB having 13:10

6.4. Simulated and Experimental Validation

In this section, the proposed multi-winding semi-DAB converter along with the proposed control is validated with simulated and experimental results. For this purpose, a nominal 500 V BESS is assumed to be connected to the input of the converter in the DCFC station. Thus, the nominal input voltage is 500 V, and the input voltage range is 350 V to 550 V. The nominal output voltage (of the BEV battery) is 400 V, with an allowable range of 150 V to 450 V, as most of the commercially available DC fast chargers have the output voltage range of 50-500 V in accordance with the available standards [75]. If a BESS with a different nominal voltage is used, only the input voltage range and associated clamped inductor and turns-ratio of the isolated high frequency transformer would change.

6.4.1 Prototype Design Considerations

The main design goals are to achieve ZVS at turn-on for all switches when possible and reduce turn-off and conduction losses by reducing the peak and rms currents. However, achieving all these criteria is a challenge when the input and output voltage vary over a wide range. For

instance, the converter falls into type 1 operational mode when the input voltage is high and the output voltage is low. This is because the transferred power is low at the output, hence, the average current drawn from the storage battery is low at high input voltage. Therefore, the converter will lose ZVS for the switches in the second leg at the primary side due to the lack of enough inductive current. Thus, to ensure ZVS, the converter needs to operate at least at the border of CCM and DCM when the effective voltage gain is less than unity. The required clamped inductance for this purpose can be found by modifying the equation to find the boundary gain, M_b where the voltage gain at the boundary becomes the required effective voltage gain. Figure. 6-6 shows the required clamped inductance values for three different low output voltages (150 V, 200 V, and 250 V) for different input voltages. Fig. 8 shows that the required clamped inductance value can be up to 60 µH to ensure ZVS when the input voltage is 550 V and the output voltage is 150 V.

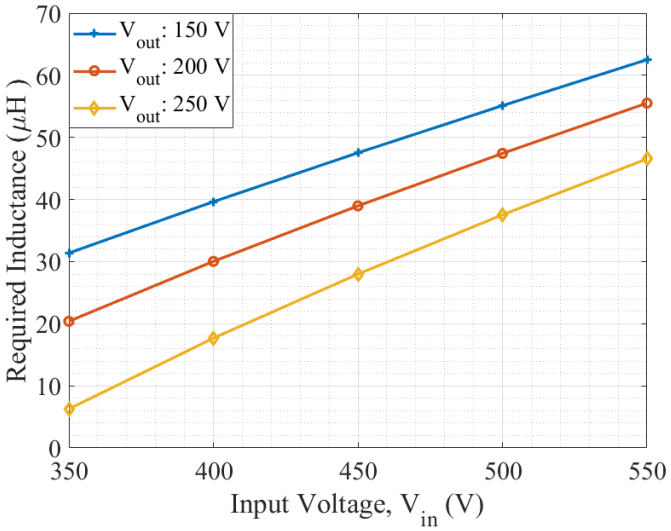


Figure 6-6. Required clamped inductance value to maintain ZVS at lower end of output voltages with turns-ratio of 13:10

However, high duty cycle loss is inevitable with high clamped inductor values as explained earlier for type 2 operational mode. Therefore, the converter may not even achieve the required voltage gain at certain operating points, for instance, when the input voltage is low and the output voltage is high. The maximum achievable voltage gain for any clamped inductance value while

ensuring ZVS at lower output voltages can be found from solving (5.20) and (5.21). Figure. 6-7 shows the maximum achievable output voltage for different clamped inductor values for two different input voltages. To provide the maximum output voltage for this converter (450 V), the maximum clamped inductance should be around 15 µH and 18 µH for input voltage of 350 V and 400 V, respectively.

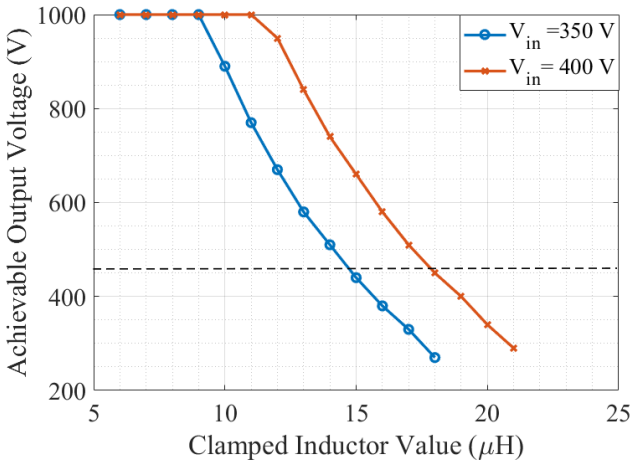


Figure 6-7. Maximum achievable output voltage with different clamped inductance values.

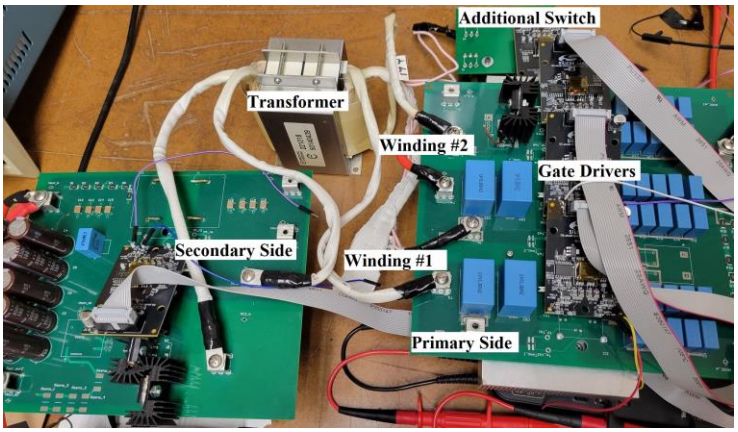
Moreover, it is usually advantageous to achieve the required clamped inductor value through the leakage inductance of the transformer since an additional AC inductor would add volume and cost. However, increasing leakage inductance values in a transformer results in higher AC resistance, increasing I^2R losses in the transformer [168]–[170]. So, it is usually preferable to limit the leakage inductance in a high current application. Therefore, the experimental prototype is designed with the minimum possible leakage inductance. This inductance is chosen to be the value that would ensure ZVS operation when both the input voltage and output voltage are low, which is about 6 µH (from Figure. 6-6) for the turns-ratio of 13:10.

An additional four turns were added to the primary side, i.e., n_2=4, to validate the concept of the proposed converter. Only four additional turns are chosen to limit total leakage inductance in the system as leakage inductance is proportional to the square of the number of turns. Also, it is

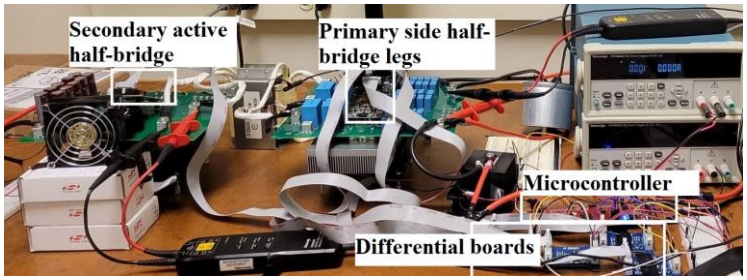
attempted to lower the voltage stress on the four-quadrant switch while only the upper winding is active. Therefore, a 10 kW semi-DAB converter with two windings at the primary side is built using the parameters and key components in Table 6-1. The converter provides the rated power when the output voltage is 400 V as the output current is kept constant at 25 A. The experimental setup is split into primary and secondary sides as shown in Figure. 6-8 (a). A zoomed-out version of the setup is also shown in Figure. 6-8 (b).

Table 6-1: Muti-winding Semi-DAB Converter Parameters

Parameters	Value
Input voltage (V_{in})	350 V-550 V
Output voltage (V_{out})	150 V-450 V
Maximum output current (I_o)	25 A
Maximum output power (P_{out})	10 kW
Switching frequency (f_s)	100 kHz
Transformer primary and secondary turns (n_1, n_2, and n_3)	13, 4, and 10
Transformer leakage inductance (L_{c1}, L_{c2})	6 µH, 10.3 µH
DC-blocking capacitors (C_{dc1}, C_{dc2})	2 µF, 2 µF
Primary and secondary side active half-bridges	CAB011M12FM3
Secondary side diodes (Quantity:4)	C4D40120D
Additional switch (Quantity:2)	IPDQ60R010S7A



(a)



(b)

Figure 6-8. Experimental Setup (a) primary and secondary side, and (b) experimental setup

6.4.2 Phase-shifts and Duty Cycles

In this subsection, the calculated phase-shifts by modifying the equations presented in section 5.1 for multi-winding structure are compared with the simulated and experimental results. This shows how accurately the proposed controller can estimate the required phase-shift and duty cycle parameters at any operating point. This is critical to identify the operating modes of the converter at any operating point. The estimated parameters along with the simulated and experimental results are tabulated in Table 6-2 for different operational modes (Type 1-3) for both turns-ratio orientations. At all these operating points, the converter operates again in CC mode with the output current of 25 A, i.e., the output power changes with the output voltage, which is the typical mode of operation for a CC EV charger. The controller can determine the required phase-shifts and duty cycles and hence, clamped inductor peak current very close to ones obtained by simulation and experiment. Any small differences in the output voltage can be adjusted by changing the phase-shifts in a very small step using the procedure mentioned in the previous chapter in section 5.2.2. Some of the differences in the peak current calculated and simulated against the results obtained by experiment are due to fact that three resistor banks have been paralleled for this experiment. Any slight variation in resistance value in any of the resistor banks, when the output voltage is high, results in small variation in the amount of current draw by the load, which in turns, results in different peak current values. Moreover, small variation in average current value may result in large difference in peak current value when large phase-shifts are required.

Table 6-2: Validation of Estimated Parameters with Simulation and Experiment

Input Voltage (V)	Output Voltage (V)	Controller (Estimated)	Simulation	Experimental
550	250	Structure: PS_2 Mode: M_2 <1 and Buck (Type 1) D_1: 0.39, D_2: 18 Inductor peak current: 37 A	Structure: PS_2 Mode: M_2 <1 and Buck D_1: 0.41, D_2: 18 Inductor peak current: 39 A	Structure: PS_2 Mode: M_2 <1 and Buck D_1: 0.42, D_2: 18 Inductor peak current: 38 A
550	300	Structure: PS_2 Mode: M_2 <1 and Boost (Type 2) D: 0.07 Inductor peak current: 24 A	Structure: PS_2 Mode: M_2 <1 and Boost D: 0.05 Inductor peak current: 24 A	Structure: PS_2 Mode: M_2 <1 and Boost D: 0.04 Inductor peak current: 20 A
500	300	Structure: PS_2 Mode: M_2 >1 and Boost (Type 3) D: 0.10 Inductor peak current: 18 A	Structure: PS_2 Mode: M_2 > 1 and Boost D: 0.09 Inductor peak current: 18 A	Structure: PS_2 Mode: M_2 > 1 and Boost D: 0.09 Inductor peak current: 20 A
450	300	Structure: PS_4 Mode: M_4 <1 and Buck (Type 1) D_1: 0.18, D_2: 0.13 Inductor peak current: 41 A	Structure: PS_4 Mode: M_4 <1 and Buck D_1: 0.22, D_2: 0.13 Inductor peak current: 40 A	Structure: PS_4 Mode: M_4 <1 and Buck D_1: 0.22, D_2: 0.13 Inductor peak current: 38 A
550	400	Structure: PS_4 Mode: M_2 <1 and Boost (Type 2) D: 0.05 Inductor peak current: 31 A	Structure: PS_4 Mode: M_2 <1 and Boost D: 0.04 Inductor peak current: 29 A	Structure: PS_4 Mode: M_2 <1 and Boost D: 0.04 Inductor peak current: 26 A
450	400	Structure: PS_4 Mode: M_2 >1 and Boost (Type 3) D: 0.12 Inductor peak current: 48 A	Structure: PS_4 Mode: M_2 > 1 and Boost D: 0.15 Inductor peak current: 49 A	Structure: PS_4 Mode: M_2 > 1 and Boost D: 0.16 Inductor peak current: 54 A

6.4.3 Loss Analysis

For type 1 operation with full-bridge structure, the switches in the first half-bridge leg turn on with ZVS as current is still negative (positive) while the top (bottom) switch turns on. These switches turn off with high current, hence, high turn-off loss occurs in these switches. The switches in the second half-bridge leg of the primary side turn on and turn-off with ZCS. For the half-bridge structure, the switches in the first leg turn on with ZCS and suffer from turn-off losses. Since the bottom switch is always turned on and the top switch is always turned off in the second leg, they have zero switching losses and the conduction loss is only present at the bottom switch. During this operational type with both bridge structures, the secondary side active switches do not have any switching losses.

For type 2 operation with full-bridge structure, all the active switches in the primary side turn on with ZVS, however turn-off losses occur for all switches. For the half-bridge structure, these losses apply to only one leg. The active switches at the secondary side turn on with ZVS, however, they turn off with less current compared to the primary side switches. Therefore, the total losses are less than those of the primary side active switches.

For type 3 operation, the switching losses depend on whether the converter is operating in CCM or DCM. For CCM, the active switches at the primary side turn on with ZVS and turn off with a small current value, and at the secondary side, they turn off with high current even though they turn on with ZVS. During DCM, the active switches at the primary side turn on and turn off with ZCS. Again, the secondary side active switches turn on with ZVS, however, turn off with high current. Therefore, the switching losses are more dominant in these switches compared to the ones at the primary side.

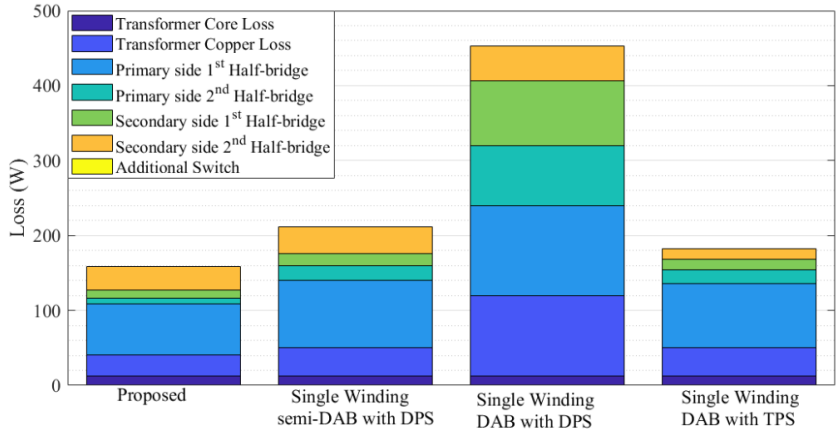
The conduction losses can be found using the on-state resistance, R_{dson} and the rms current for the active switches and the forward voltage drop and the average current for the diodes. The transformer copper loss can be found using the AC resistance of the windings and the rms current in the transformer. The transformer core loss can be estimated by using the improved generalized Steinmetz equation [171].

The losses in the proposed converter are estimated for different output voltages when the input voltage is 550 V based on simulations in PLECS (for steady state and conduction losses) and LTSpice (for switching losses). For comparison, the losses in a single winding semi-DAB with DPS are also simulated and calculated in the same way. Furthermore, since the proposed converter adds one active leg (two active switches) compared to the semi-DAB, and thus has 4 active legs, a comparison is also made to the DAB converter, which also has 4 active legs. The proposed

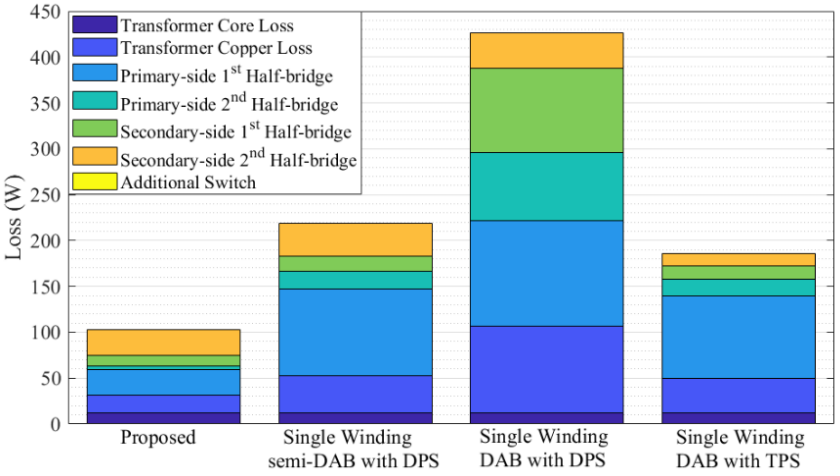
converter also adds two back-to-back tap-controlling switches to the semi-DAB topology, but these does not contribute to switching losses. For this purpose, the DPS control for DAB presented in [172] and the TPS control proposed in [173] are adopted since both of them attempt to minimize the current stress in the system.

The estimated losses are presented in Figure. 6-9. The losses in the active switches incurred in the semi-DAB converter with DPS control are very similar to the losses in the DAB converter with TPS. This is because DPS and TPS controls for DAB converter are usually equivalent to SPS and DPS, respectively, for the semi-DAB converter. This is because one of the active half-bridge legs in the DAB converter is replaced with a diode bridge leg in semi-DAB converter. Overall, the proposed converter has the lowest losses for the cases of output voltage from 150 V to 300 V. At 350 V output the proposed converter has slightly higher losses than the semi-DAB with TPS due to the small conduction losses through the tap-controlling switch, as shown in Figure. 6-9(e). At this operating point, the loss of the proposed converter is 143 W and the loss of the DAB with TPS is 140 W, which represents a difference of 0.03% in efficiency. However, identifying the optimal phase-shift ratios with TPS is a challenging task when the operating modes vary with input and output voltage variation. For instance, the fundamental component approximation (FCA) method does not result in correct phase-shift ratios when the phase-shift ratios are close to zero [174]. Furthermore, no optimal solution can be achieved if the required phase-shift between the active legs at the secondary side is lower than the phase-shift between the active legs at the primary side in a DAB converter with the iterative method based on Lagrange multiplier presented in [173]. Other iterative methods such as genetic algorithm and Newton's method presented in the literature are also computationally expensive [175]. In contrast, the proposed control for the multi-winding

semi-DAB converter is much simpler than the TPS control for DAB and can be easily implemented with a microcontroller.



(a)



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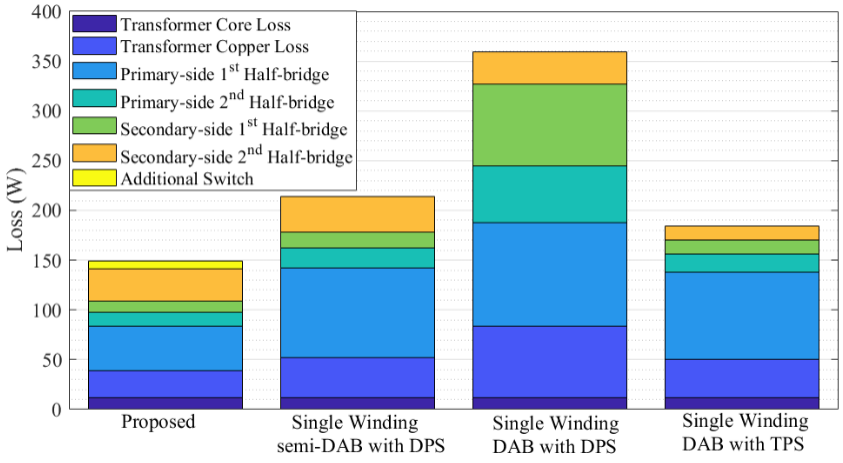

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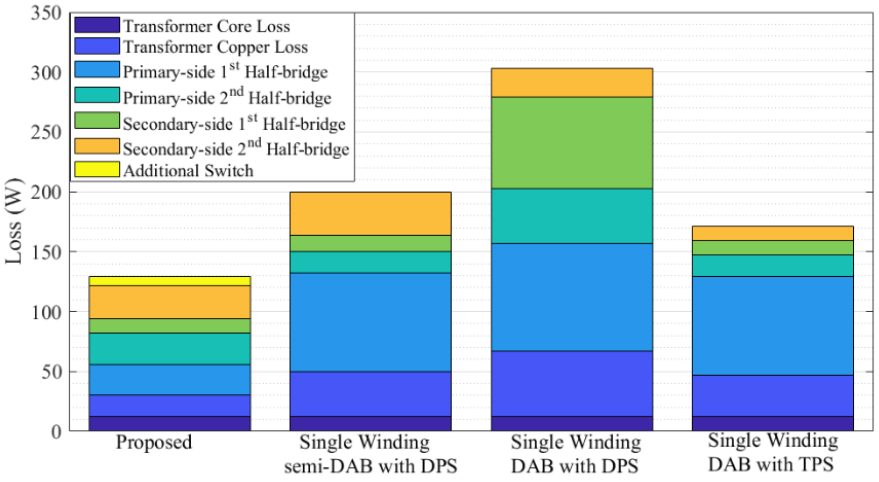

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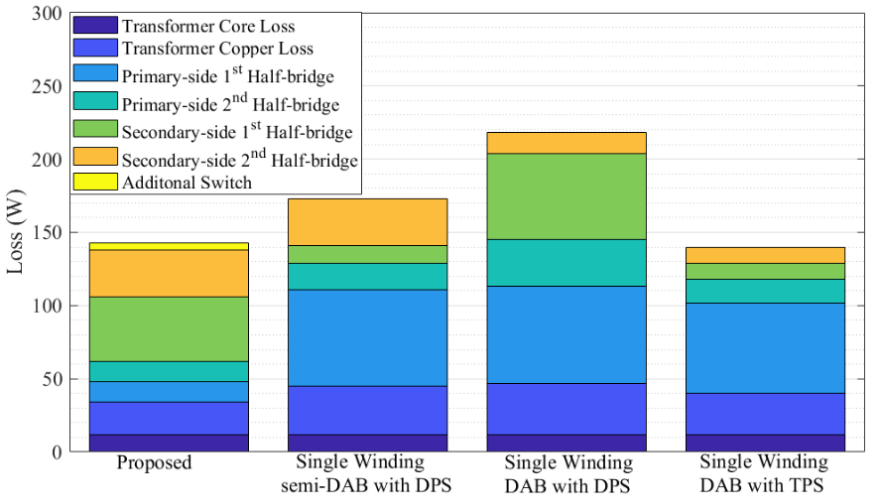


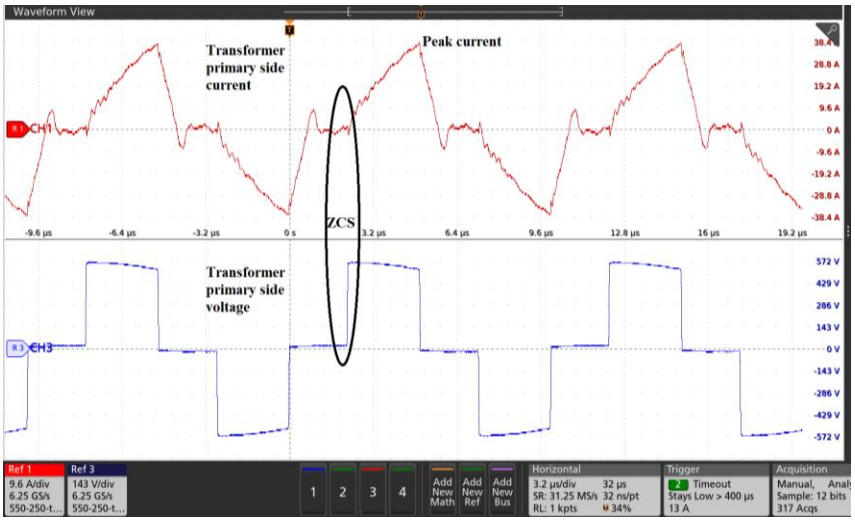
(e)

Figure 6-9. Loss estimation for proposed and standard semi-DAB converter when the input voltage is 550 V for output voltage (a) 150 V, (b) 200V, (c) 250 V, (d) 300 V, and (e) 350 V

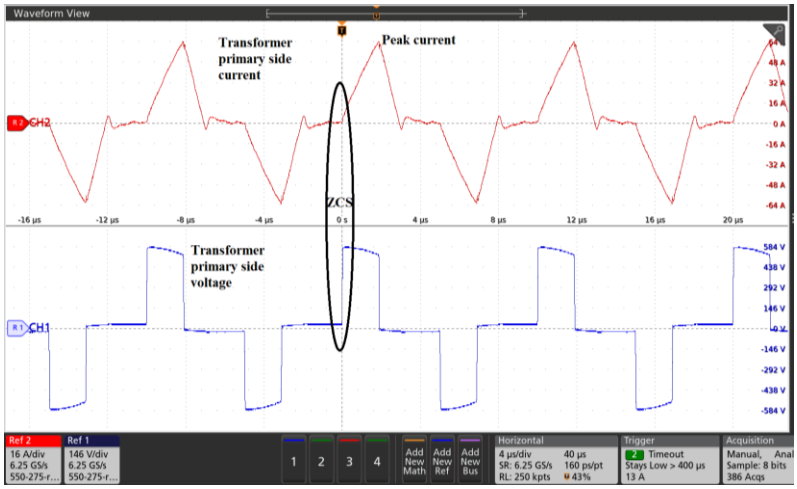
6.4.4 Experimental Waveforms

The experimental validation for the operational points in Table 6-2 are provided by the transformer primary side voltage and current, as shown in Figures. 6.10 to 6.15. For the first operating point when M_2 <1 and in buck mode for the *PS2* structure (turns-ratio 17:10) with V_{in}=550 V and V_{out}=250 V, the experimental waveforms are shown in Figure. 6.10 (a). The converter is operating in DCM, and the switches turn on with ZCS. In contrast, the waveforms generated using the regular DPS control with traditional semi-DAB with single turns-ratio of 13:10

are shown in Figure. 6.10 (b) for the same operating point. Figure. 6.10 (b) shows that the converter also operates in DCM and the peak current under DPS control is more than 1.5 times that of the proposed converter structure with optimal control at this operating point. Therefore, switches S_1 and S_2 would turn off with higher current compared to the proposed converter structure with optimal control, leading to higher switching and conduction losses. The primary side voltage and current for the second operating point when M_2 <1 and in boost mode for the PS_2 structure are shown in Figure. 6.11 (a). The same operating point with traditional semi-DAB with single turns-ratio of 13:10 with DPS control is shown in Figure. 6.11 (b). The primary side voltage and current for the operating point when M_2 >1 and in boost mode for the PS_2 structure are shown in Figure. 6.12 (a). The same operating point with traditional semi-DAB with single turns-ratio of 13:10 with DPS control is shown in Figure. 6.12 (b). The waveforms for the operating points for the PS_4 structure when M_4<1 (buck), M_4<1 (boost), and M_4>1 (boost) are shown in Figure. 6.13, 6.14, and 6.15, respectively.

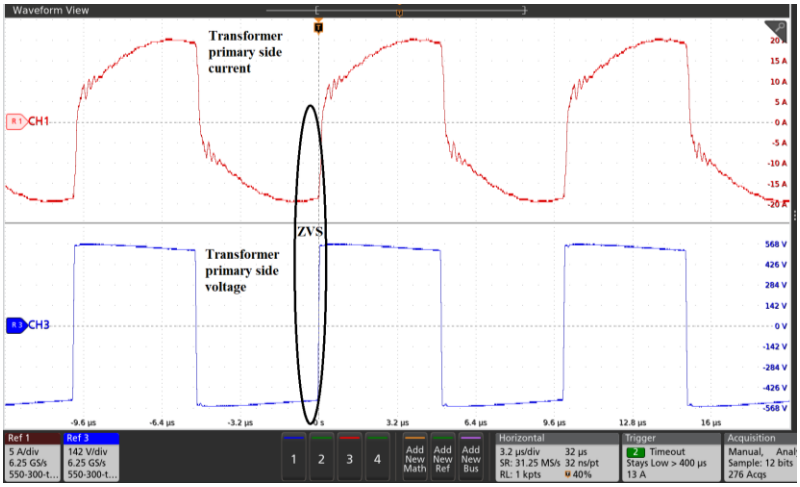


(a)

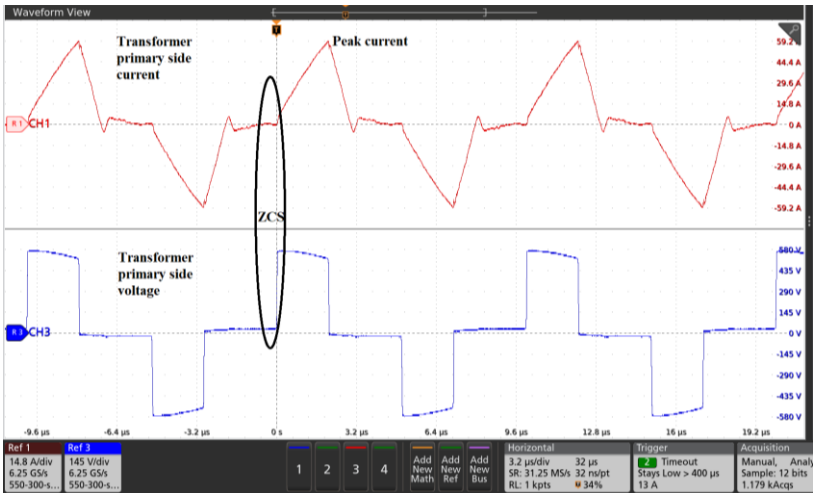


(b)

Figure 6-10. Transformer primary side voltage and current for Vin: 550 V and Vout: 250 V

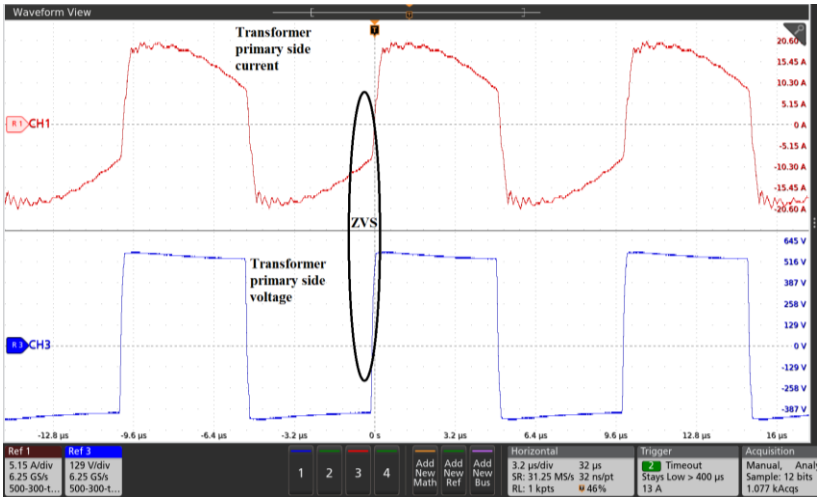


(a)

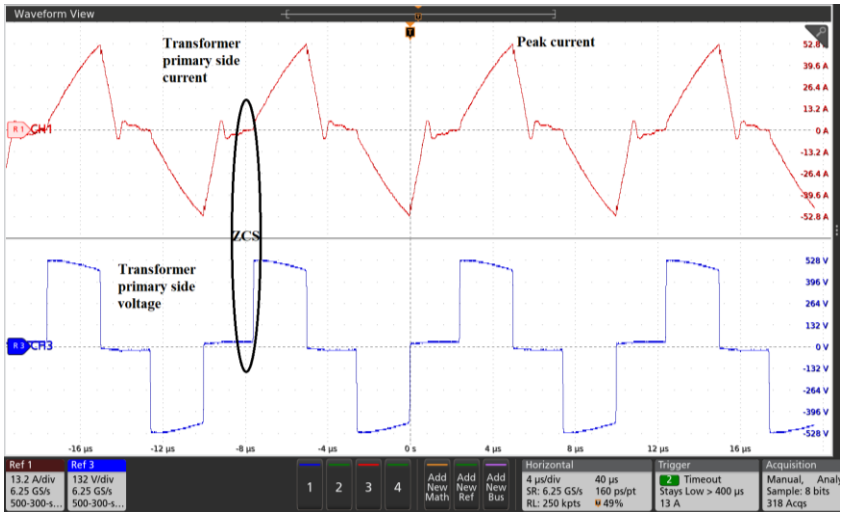


(b)

Figure 6-11. Transformer primary side voltage and current for Vin: 550 V and Vout: 300 V



(a)



(b)

Figure 6-12. Transformer primary side voltage and current for Vin: 500 V and Vout: 300 V

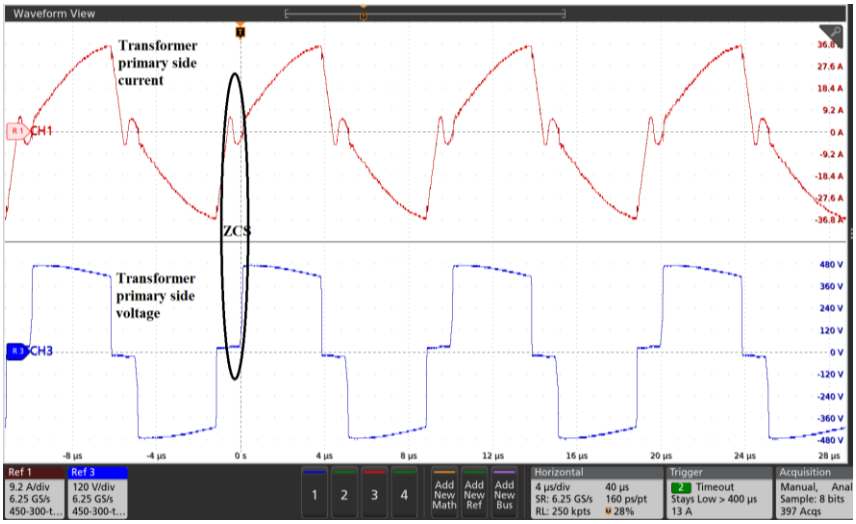


Figure 6-13. Transformer primary side voltage and current for Vin: 450 V and Vout: 300 V

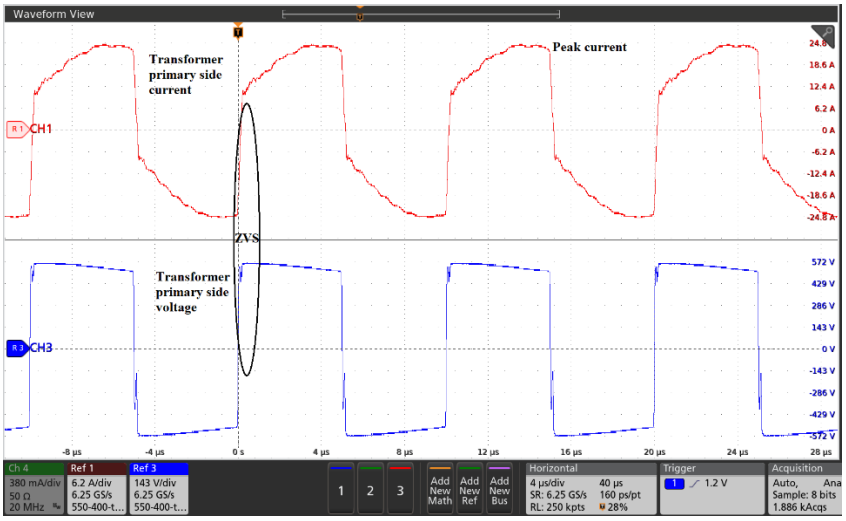


Figure 6-14. Transformer primary side voltage and current for Vin: 550 V and Vout: 400 V

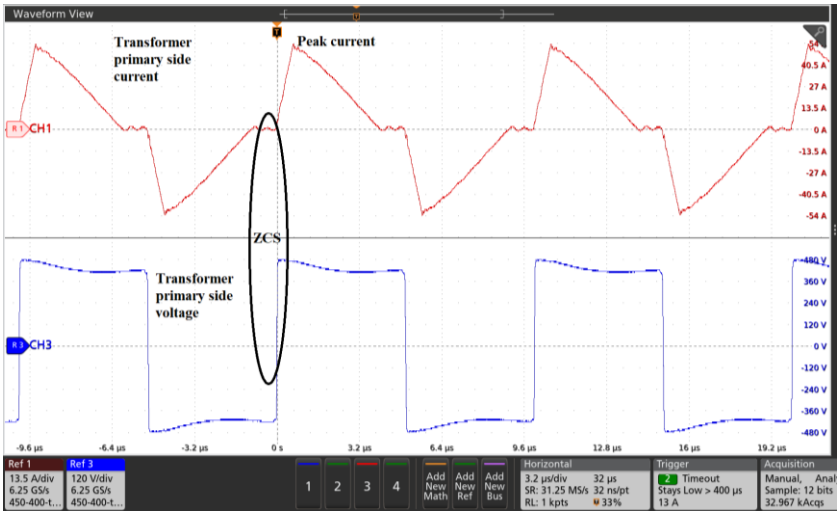
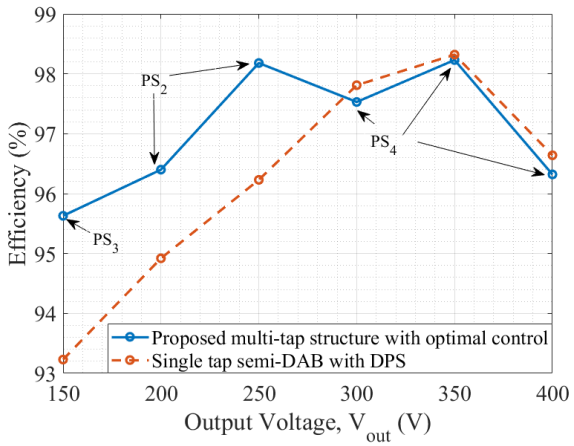


Figure 6-15. Transformer primary side voltage and current for Vin: 450 V and Vout: 400 V

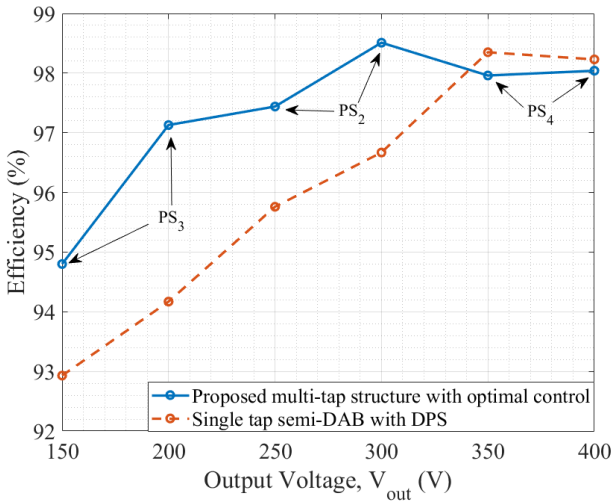
6.4.5 Efficiency

Figure. 6-12 shows the experimental efficiency results of the multi turns-ratio converter with optimal control compared with that of the traditional single winding semi-DAB having 13:10 turns ratio with DPS control for three different input voltages in CC mode providing 25 A output current. It should be noted that the proposed control method adopts DPS, and the proposed converter primary structure becomes the same as the single turns-ratio, at and above 300 V, 350 V, and 400 V output for input voltages of 450 V, 500 V, and 550 V, respectively. It is evident that the proposed

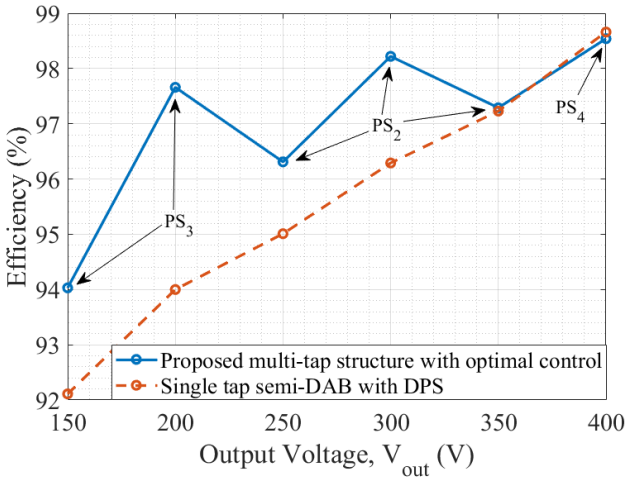
converter with optimal control strategy results in much better efficiency of the converter when the input voltage is high and output voltage is low compared to DPS, with an increase up to 3.5%. When the converter structure adopts the same structure as the traditional semi-DAB, the efficiency decreases slightly, an average of 0.23% for all the points shown in Figure. 6-12. This is due to the fact that the second winding of the proposed converter still needs to be energized even though only the first tap is carrying current. Overall, the significant efficiency gains at the lower output voltages help to flatten the efficiency curve, reducing losses at many points and helping to simplify the thermal design, since the low DPS efficiencies of 92% to 93% do not exist in the proposed converter.



(a)



(b)



(c)

Figure 6-16. Efficiency comparison between proposed control and DPS for input voltage (a) 450 V, (b) 500 V, and (c) 550 V

6.5. Summary

A novel multi-winding structure along with the control for the semi-DAB to improve efficiency in a DCFC station even further has been proposed in this chapter. The proposed converter and control have been validated with a 10 kW prototype and the results show that the proposed converter and control can reduce peak and rms current in the converter, reducing switching and conduction losses. A peak efficiency gain of 3.5% is found for the common scenario of high input (BESS) and low output (BEV) voltages, and peak efficiency of 98.5% is achieved.

Chapter 7

Conclusions and Future Work

7.1. Conclusions

This thesis first provided a comprehensive review of DCFC stations with energy storage, with three energy storage options (battery, flywheel, and hydrogen), system architectures, and power electronic converters suitable for each option. Furthermore, each option is modeled in MATLAB/Simulink to quantify efficiency, volume, and cost for a small, medium, and large DCFC station. The results show that flywheels would be best considered if high power grid services will be also provided by the energy storage, and hydrogen storage would be best considered only if refueling of fuel cell vehicles is also required. Otherwise, batteries generally exhibit the lowest cost, lowest volume, and highest efficiency. A comparison of battery architectures shows that the optimal architecture is highly dependent on the grid connection power and the EV charging power.

This thesis then investigated the impact of a VSC-AFE based DCFC station connected to an electrical grid distorted with background voltage harmonics. In a VSC-AFE, the background voltage harmonics mainly propagate depending on design of the current control loop and PLL. The current emission at the frequency the background voltage is being distorted which can be reduced with different current controller settings, grid voltage feed-forward and selective harmonic compensations. However, the analysis in Chapter 4 has shown that these techniques are not effective when it comes to eliminating current emission at the coupled frequency. Therefore, it is necessary to understand the origins of current emissions before implementing various mitigation techniques. This thesis has shown the origins of current emissions at coupled frequency analytically and verified the results with simulation. This thesis has also shown that DSOGI based PLL are effective in eliminating the current emission at coupled frequencies. Though DSOGI filters are not commonly used in industry at this time, the results in Chapter 4 indicate that DSOGI

filters are superior to other commonly used methods for reducing harmonics at the coupled frequency, and thus merit further consideration by industry.

This thesis has further identified the semi-DAB converter as a promising candidate for the DC/DC converter interfacing the BESS and the BEV. Therefore, a novel control strategy is proposed in Chapter 5 for semi-DAB converters called RBOC. The goal is to ensure high efficiency at all operating points, especially at the lower output voltages while the input voltage is high. The analysis provided in this thesis can also be used to identify the operational modes of a semi-DAB converter along with required phase-shifts and duty cycles in real time without searching for the entire space of phase-shift duty cycles. The proposed RBOC strategy is validated with a 25 A rated prototype providing 10 kW of power at 400 V output. The control strategy is experimentally shown to have up to 3.5% higher efficiency than the well known DPS control at operational points with high input voltage and low output voltage, with a peak efficiency of 97.6%. Overall, the experimental results show higher efficiencies over an ultra-wide range of output voltages even when the input voltage varies over a wide range in comparison to the DPS control.

This thesis lastly proposes a novel multi-winding structure along with the control for the semi-DAB to improve efficiency in a DCFC station with BESS even further. This is because the optimal control presented in Chapter 5 can improve the operating efficiencies to a certain extent as the converter has to adopt DPS at higher output voltages. The proposed converter and control in Chapter 6, on the other hand, reduce switching and conduction losses, and thus improve efficiency even at operating points with higher output voltages compared to DPS. The proposed converter and control have again been validated with a 10 kW prototype and the results show that a peak efficiency of 98.5% is achieved.

7.2. Future Work

New control laws could be developed to improve the operation of the converter even further at the points when the converter adopts DPS at high output voltages. Different multi-winding structures should be identified to provide variable turns-ratios to operate the converter in ZVS turn-on, and thus to improve the efficiencies even further. While doing so, it should be attempted to reduce the voltage stress on the four-quadrant switches.

The performance of higher power charging ports with multiple DC/DC converters connected in parallel should be investigated. The analysis should be in terms of both steady-state and dynamic performance of the converter systems paralleled to provide high power to a single BEV, i.e., to a single charging port. While multiple modules are connected in parallel, the optimal operation of each module should be identified. For instance, when the input voltage is high and output voltage is low, the output current of each module could be increased to ensure ZVS operation. This would improve the overall efficiency of the system.

The possibility of configuring the parallel connected DC/DC converters to provide power to multiple BEVs, i.e., the possibility of becoming a multi-port charger should also be investigated to reduce investment cost. This would particularly be useful in real-life scenarios where all the BEVs are not capable of being charged with the same power and current level.

The isolated semi-DAB converter can also be used as an isolated power factor corrector. Therefore, the analysis presented here can be modified to extend the operation of the semi-DAB converter as a power factor corrector in DCFC stations with common DC bus. Since this converter must track the connected stationary battery terminal voltage in some DCFC architectures presented in this thesis, it is necessary to ensure high efficiency over wide output voltage while providing high power factor at the grid terminal.

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