Addressing GaN Converter Challenges: False Turn-On Issues & Switching Loss Modelling

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Abstract

Wide bandgap devices are the future of this dynamically changing technological world. Considering Gallium Nitride (GaN) and Silicon Carbide (SiC), GaN has exceptional characteristics that will likely allow it to proliferate greatly in the area of low-and-mid-power power electronic converters. One of the current challenges in this context to completely utilize GaN are the reliability issues, especially false turn-on events, which is a main focus of this thesis. False turn-on due to its momentary short circuit capability deteriorates the converter performance. Furthermore, simple and accurate modeling of GaN device losses is critical to help electronic designers optimize converter designs.

This thesis focuses on three contributions to help reduce false turn-on events and improve GaN modeling efforts. First, this work uniquely investigates the optimal pulse-width-modulation (PWM) scheme to balance efficiency and false turn-on. The experimental results lead to a recommendation to use a larger negative bias than is currently recommended by device manufacturers. Secondly, the work proposes a new simplified switching loss model with high accuracy that can be used with different gate drive circuits (including negative gate bias voltages) to make it more useful for power electronics design engineers as a tool. And thirdly, since the main contributor to false turn-on events are the parasitic inductances in the switch and on the PCB, this work proposes a new parasitic inductance measurement methodology which can be implemented using only simple laboratory instruments.

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Chapter 1: Introduction

1.1 Background & Motivation

Power electronics can be simply defined as the application of solid-state electronics to condition, control, and convert electric power. Power semiconductor devices are the core solid-state components in the overall power conversion system, and they have traditionally consumed the largest portion of power losses in the overall system. Therefore, the advancement of power semiconductor devices has been a driving force in the progress of power electronics systems. Historically, silicon (Si)-based devices have dominated the power device market due to mature and well-established fabrication technology for Si [1]. But there have been applications where Si power electronics have limitations such as high losses leading to switching frequency limits, insufficient thermal capabilities limits, and voltage breakdown.

Wide bandgap devices are the most promising semiconductor device technology in the 21st century. They are best suited for achieving high switching frequency and high efficiency for next generation power conversion. Wide bandgap semiconductors include gallium nitride (GaN) and silicon carbide (SiC) have numerous advantages over conventional Si-based devices [2]. They

have higher breakdown fields which ultimately allows for optimized design with thinner drift regions and results in power devices with lower specific ON state resistance [3]. Also, they have higher switching frequency limits in the range of megahertz which reduces the power converters size significantly. Among the available wide bandgap devices for power conversion, GaN has the highest electron mobility, saturated electron velocity, energy gap and electric field breakdown limit [4]. This is the reason behind the main focus towards the GaN technology for power conversion in low-to-medium power applications. Also, the work for 1200V GaN devices is still undergoing [5] which will eventually replace the dominance of SiC making GaN the best choice in the coming years [6].

Along with the benefits of new GaN devices comes new design challenges. One main concern is the reliability of GaN devices especially in half-bridge circuits due to false turn on phenomenon. Due to fast switching transients, the effect of various parasitics involved in GaN-based bridge leg configuration has been studied in [7], [8] but without their impact on the performance of converter stability. Modelling of GaN converters for switching transients and losses, which is critical for the design phase, has been carried in recent research [8] – [15] but they all lack an accurate switching model of GaN. This makes it necessary to further develop an analytical model of GaN which includes all device parameters and their influence. Other work such as [16] – [40] suggests some measures for mitigating the problem of false turn on/off phenomena in bridge leg configuration but the device parameters responsible for these causes has not been explained.

Therefore, this thesis focuses on three contributions to help reduce false turn-on events and improve GaN modeling efforts. First, this work uniquely investigates the optimal pulse-width-modulation (PWM) scheme to balance efficiency and false turn-on. Secondly, the work proposes a new simplified switching loss model with high accuracy that can be used with different gate

drive circuits (including negative gate bias voltages) to make it more useful for power electronics design engineers as a tool. And thirdly, since the main contributor to false turn-on events are the parasitic inductances in the switch and on the PCB, which are often not detailed in datasheets by manufacturers, this work proposes a new measurement methodology which can be implemented using simple laboratory instruments.

1.2 Research Contributions

This research thesis contributes to the existing latest challenges in the field of GaN power converters. The research work mainly focuses on improving the reliability of GaN power converters and switching analysis. Therefore, the three main contributions of this thesis can be briefly summarized as:

1. Experimental investigation and recommendations to establish a tradeoff between reducing false turn-on events on low side device in half bridge configuration and balancing power converter efficiency with an optimized PWM scheme.
2. Development of a simplified and accurate hard-switching loss model involving minimal computation. The proposed model suggests a mechanism to simply analyze the multi-stage switching transition lumped into a single equation, including the dependence on different parameters. The proposed model is validated through extensive experiments.
3. The main contributor to false turn-on events is the circuit parasitic inductances, where the device inductances may be unknown if not detailed in the datasheet, and the PCB inductances are generally unknown and unique to every design. Therefore, a new measurement methodology which can be directly applied to surface mounted devices has

been developed which involves the use of simple laboratory instruments like a DC power supply, function generator, and voltage and current probes.

1.3 Thesis Organization

This thesis is organized into six chapters. Chapter 1 has given the background and motivation for the entire work and problem formulation. It also briefly describes the three main distinctive contributions of this research along with the outline.

Chapter 2 gives a literature review of the different false turn-on models and switching loss models by briefly explaining their contributions and limitations. This chapter highlights the recent research work in this area in order to motivate the need for more research based on the limitations of the existing work.

Chapter 3 presents the first contribution of this thesis not done in prior research work which is the development of an optimized PWM technique to mitigate false turn-on issues on low side device in half bridge converters while balancing the power converter overall efficiency. Extensive experimental work is performed and presented to provide details on this investigation and the resulting recommendations.

Chapter 4 presents the second contribution by proposing a new simplified hard-switching loss model that can be applied with varying gate drive parameters for high voltage GaN devices with detailed derivations. The proposed model can accurately estimate switching losses even with negative gate bias voltages. Experimental work is performed to validate the model.

Chapter 5 focuses on the third contribution of this thesis by suggesting a new measurement methodology for measuring the three different parasitic inductances namely common source inductance, gate inductance, and drain inductance by using simple laboratory instruments.

Simulations are used to validate the accuracy of the method and experimental results are also presented.

Chapter 6 summarizes the overall contributions of the thesis and suggests scope for future research work.

Chapter 2: Literature Review

2.1 History of GaN & Future Market Prediction

The gallium nitride (GaN) high electron mobility transistor (HEMT) firstly appeared in 2004 with depletion mode radio frequency by Eudyna corporation in Japan. The HEMT structure was based on the phenomenon first described in 1975 by T. Mimura. It basically demonstrates the unusual high electron mobility described as two-dimensional electron gas in the region of an aluminum gallium nitride (AlGaN) and GaN hetero structure interface. This technology was initially applicable in radio frequency but was made possible to power conversion applications by Efficient Power Conversion (EPC) in California [1]. In June 2009, EPC first developed a GaN power MOSFET which was an enhanced mode GaN on a silicon substrate. This clearly signifies how the HEMT structure for GaN has been fabricated on Si substrate. The objective of fabricating GaN on Si substrate has the advantage of producing GaN in high volumes at low cost by using the same manufacturing technologies and facilities as Si. In addition to improved thermal requirements due to efficiency improvements, generally, wide bandgap technologies demonstrate a much lower intrinsic carrier concentration compared to Si [2].

The use of GaN on silicon power transistors is rising day by day, and GaN power modules are predicted to grow quickly in the coming years. A market study in [19] suggests that GaN power devices will experience a compound annual growth rate of nearly 30% in next five years which is higher than the 20% predicted for SiC. A detailed insight is shown below in Fig. 2.1.

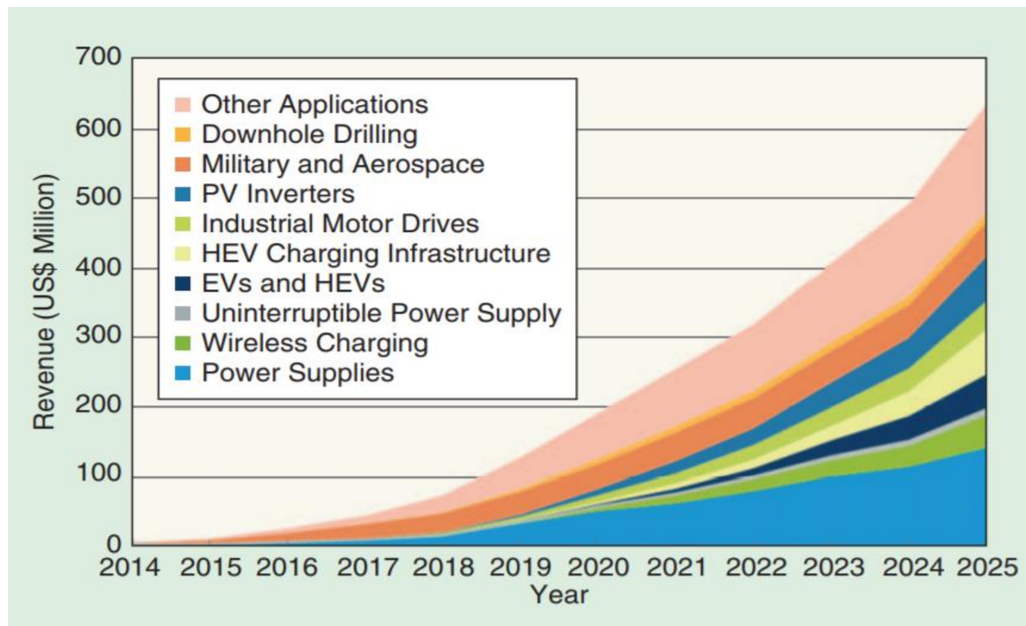


Fig. 2.1. A market study for GaN device sales revenues in coming years [4]

This trend clearly shows that increasing commercial availability of power semiconductor devices from multiple sources are factors for further accelerating the adoption of SiC and GaN. Many manufacturers like Transphorm Inc. used 650-V GaN FETs and the list also includes GaNsystems (Ottawa, Canada), Telcodium (Boucherville, Canada), Bel Power Solutions (Santa Clara, California), and Tata Power (Mumbai, India).

With bridge leg configuration used in dc–dc converters, Transphorm Inc. has also started establishing its 900-V GaN FET in a standard TO-220 package with an on-state resistance of 170 and 150 mΩ. The 900 V platform was developed by funding from the U.S. Department of Energy's

Advanced Research Projects Agency Energy. Therefore, in the coming years there will be rapid advancement in this field with the launch of high power GaN devices in the coming years by different manufacturers and thus this will widen its application.

2.2 Comparison of Si, GaN & SiC

In moving towards wide bandgap circuit design, it is important to understand characteristics of Si, GaN, and SiC and the challenges that exist. A holistic comparison of these semiconductor devices in terms of crucial parameters like electric field breakdown, energy gap, thermal conductivity, saturated electron velocity and electron mobility is needed. Fig. 2.2 clearly gives an insight to this comparative analysis. It can be easily concluded that SiC excels in high-temperature applications because of highest thermal conductivity relatively but the fact is material characteristics of GaN are superior in high-efficiency, high-frequency converters. GaN has the highest energy gap, electric field breakdown, saturated electron velocity, and electron mobility in comparison to Si and SiC as well [3].

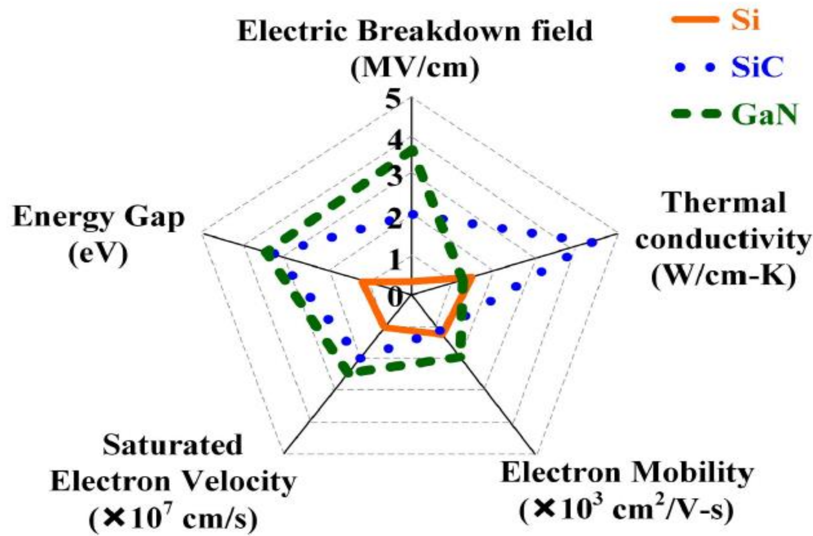


Fig. 2.2. Comparison of Si, SiC, and GaN for power semiconductor applications [3]

GaN possesses almost three times the electron mobility than SiC. This is an important material property responsible for high frequency power conversion as it decides the switching frequency limit that a device can offer. Therefore, among the available power semiconductor devices GaN is capable of providing the highest switching frequency.

Also, GaN has a better bandgap and critical electric field strength which decides the voltage rating of a power switch. With a high electron saturation velocity in comparison to Si and SiC, GaN is capable of handling large currents at the same time. All these material properties are compared in Table 2.1 shown below.

Table 2.1. Material Properties of Si, SiC and GaN [2]

Material Property	Si	SiC	GaN
Bandgap (ev)	1.1	3.2	3.4
Critical Electric Field (MV/cm)	0.3	3.2	3.5
Electron Mobility (cm^2/V.sec)	1450	700	2000
Electron Saturation Velocity (10^6cm/sec)	10	20	25
Thermal Conductivity (W/m.K)	130	700	110

Also, most importantly, the high electron mobility of GaN further reduces the ON-resistance reducing conduction losses. This allows for a smaller die size to achieve a given current capability, and therefore lower input and output capacitances. All these features clarify how the still existing Si technology is outdated compared to emerging GaN and SiC technology.

Power loss assessment is an important aspect of a well-designed power converter which is related to efficiency. Table 2.2 compares the electrical characteristics for GaN and SiC devices. For this comparison, GaNSystems 650V/30A and Cree-SiC 900V/35A devices have been taken under consideration.

Table 2.2. Electrical Characteristics of GaNSystems 650V/30A, Cree-SiC900V/35A [32]

Parameters	**GaN e-HEMT GS66508T**	**SiC MOSFET C3M0065090J**
Package	Low Inductance GaNPX^{TX}	D2PAK
V_{ds}_max	650 V	900 V
I_d at 25°C	30 A	35 A
R_{ds_on} at 25°C	50 mΩ	65 mΩ
V_{gs}	-10/+7 V	-4/+15 V
C_{iss}	260 pf	660 pf
C_{oss}	65 pf	60 pf
C_{rss}	2 pf	4 pf
Q_g	5.8 nC	30.4 nC
Q_{gs}	2.2 nC	7.5 nC
Q_{gd}	1.8 nC	12 nC
Q_{rr}	0 nC	245 nC

GaN has lower parasitic capacitances C_{iss} (input), C_{oss} (output) and C_{rss} (reverse) which enables it to achieve a stable performance at megahertz switching levels in comparison to SiC. These capacitances include capacitances between gate, drain and source junctions. These intrinsic capacitances in a basic FET structure are shown Fig. 2.3 [1]. The input capacitance C_{iss}, output capacitance C_{oss} and reverse transfer (or Miller) capacitance C_{rss} are mathematically formulated as

$$C_{iss} = C_{gs} + C_{gd} \tag{1}$$

$$C_{oss} = C_{gd} + C_{ds} \qquad (2)$$

C_{iss} is measured by shorting the drain and source, so it is the parallel combination of capacitances C_{gd} and C_{gs} whereas C_{oss} is measured by shorting gate and source so it is a parallel combination of capacitances C_{gd} and C_{ds}. But C_{rss} is measured between gate and drain (without shorting), therefore it is C_{gd} plus the series capacitance of C_{gs} and C_{ds} given by the equation

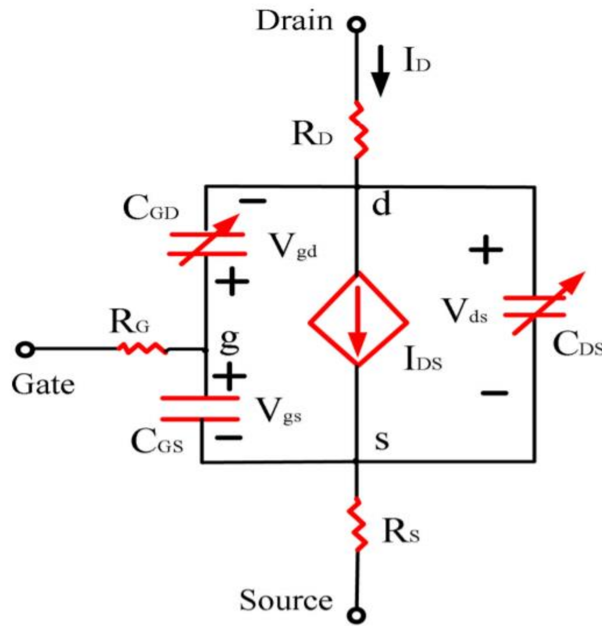


Fig. 2.3. FET structure with Device Intrinsic Capacitances [5]

$$C_{rss} = C_{gd} + \frac{1}{\left(\frac{1}{C_{gs}} + \frac{1}{C_{ds}}\right)} \qquad (3)$$

In the case of GaN-HEMT, C_{gd} plays a significant role while deriving its analytical model for switching transients. C_{gd} is a device parameter known as miller capacitance often responsible for short channel effects and in a power converter it is mainly responsible for false switching problems.

Also, C_{iss} is lower for GaN than SiC which has the advantage of providing flexibility in the gate drive circuit. Output capacitance C_{oss} is almost the same for both GaN and SiC. Interestingly GaN

has no reverse recovery issues which makes it even better than SiC. During the switching transients C_{iss} shows a dynamic change in its value. Although device datasheets from different manufactures claims it to be constant, the fact is this value is measured during standard operating conditions.

Overall losses have been primarily categorized into conduction, switching, dead time and gate charge loss. It can be seen from Table 2.3 that SiC has losses almost 3.5 times higher than GaN for the same power specifications. Analysis is based on the standard losses existing in any FET structure. For this comparison, GaNSystems GS66508T and SiC MOSFET C3M0065090J [32] have been considered as their ratings closely match.

Table 2.3. Loss comparison across each switch [1, 32]

Parameter	**GaN-HEMT GS66508T**	**SiC MOSFET C3M0065090J**
Conduction Loss	5 mW	6.5 mW
Switching Loss	1.335 W	2.4 W
Dead Time Loss	0 W	0.768 W
Gate Charge Loss	0.0812 W	0.2128 W
Total Losses	1.4212 W	3.3873 W

2.3 Instability Issues in Half Bridge GaN Circuits

Enhancement-mode GaN transistors in half bridge circuits can become instable and exhibit false turn-on. With the higher switching speed there is a more serious problem of overvoltage and parasitic ringing. Also lower on-resistance and capacitances can result in a smaller damping ratio making the power converter system unstable. This can lead to more severe instability problems for GaN-based power circuits. There are three different types of instabilities categorized as types A, B, and C [7] shown in Fig. 2.4 below.

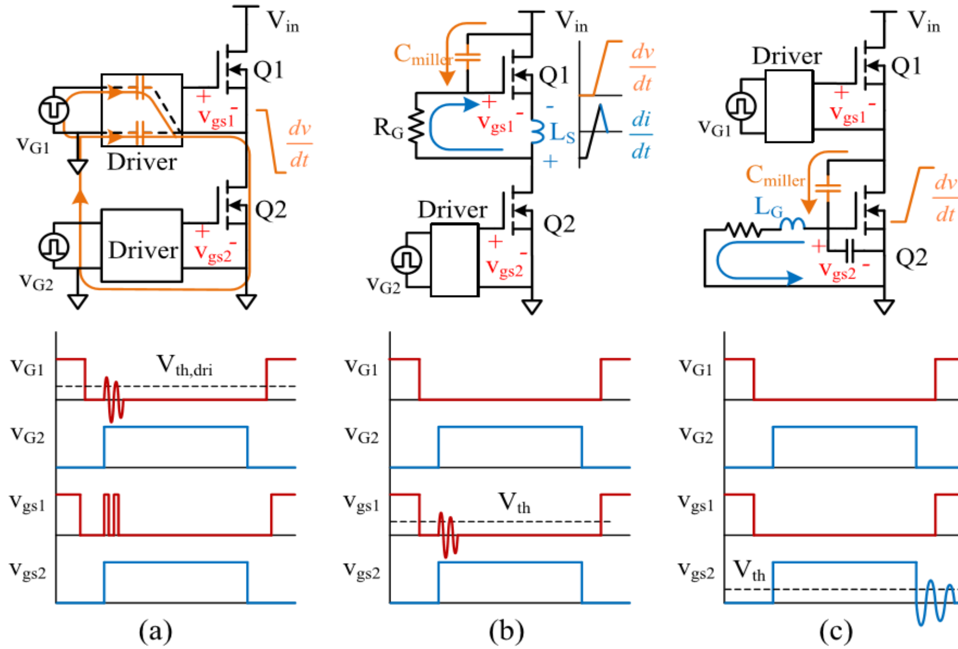


Fig. 2.4. Types of Instabilities in Half Bridge GaN Circuits [7]

1. **Type A Instability** – This type of instability occurs in RF circuits using cascode GaN devices [7]. Also, it is more common at switching frequencies higher than 10 MHz. In a cascode structure the parasitic mismatch between the depletion mode GaN transistor which is in series with enhancement mode Si MOSFET is considerable. Therefore, due to this mismatch the pulse width modulation (PWM) signal gets distorted because of the high parasitic capacitance between signal circuit and power circuit. Thus, finally the distorted PWM signal triggers the switch to falsely turn ON or turn OFF as explained in [8] – [9].
2. **Type B Instability** – The turn-on gate oscillation is induced by high dv/dt and high di/dt both during switching transients as explained in [10] – [13]. In a bridge leg configuration when the active switch turns ON, the drain to source voltage of the inactive device (synchronous switch) increases abruptly. Because of this the displacement current flows through the miller capacitance (gate to drain capacitance) of the inactive switch to its gate

node, which may cause the gate to source voltage to exceed beyond the threshold voltage. Also, a voltage is generated because of high di/dt due to common source inductance between gate and power circuits.

3. **Type C Instability** – Turn-off oscillations occur primarily because of high dv/dt and high gate loop inductance [14] and [15]. When the active switch turns off, the current through miller capacitance because of high dv/dt flows through the gate loop inductance, and the energy is ultimately stored in gate inductance. This makes both gate inductance and input capacitance in a loop, and the gate voltage of the active switch rings back and exceeds beyond the threshold voltage which ultimately results in false turn on. This gets even worse with higher slew rates i.e., dv/dt. Higher dv/dt of GaN devices is an inherent characteristic but poses the limitations of reliable operation of power converters.

Out of the above three instability A, B and C types, B and C are the main focus of this research work as type A does not exist in power converter systems. Also, the problem of type A instability can be solved by using an enhancement mode GaN device which will have no parasitic mismatch like cascode GaN devices. Even, in the case of cascode structure where the capacitance mismatch between the GaN device and Si MOSFET results in oscillations, it can be resolved to some extent by adding a proper capacitor in parallel with Si MOSFET. Now theses instabilities result in faulty converter operation. The next section details the methods used to improve the stability by looking into different methods as suggested in recent research work.

2.4 Methods to Improve Instability

The question arises what precautionary measures are needed to overcome these instabilities. There are mainly four distinct ways to overcome this instability issues as stated in papers [16] – [41]. They are classified as:

1. **Negative bias to turn off switch**: By applying negative gate bias, the gate terminal's safe operating margin can be extended by retaining high switching speed of the GaN transistor [16]. Lager safe operating margin of gate source voltage also prevents the device from being damaged. The application of negative bias during turn-off introduces more immunity to the operation by reducing the unintended Miller turn-on [16] – [18]. This negative bias controls the flow of displacement current (responsible for false turn-on) through the gate terminal [1]. Also, the negative bias has the ability to reduce the impact of threshold voltage instability which is the degradation in the device threshold voltage over a period of time.
2. **Increasing gate resistance**: An increment in gate resistance results in an increase in the damping ratio of the system [8]. This damps out the sustained oscillation but with an additional power loss.
3. **Reducing common source inductance by optimal PCB design**: Although the earlier cascode GaN devices do not have the source sense pin (which is why the common source inductance was high in them [1] – [3]), the latest enhancement mode GaN devices use a four pin structure, meaning the common source inductance is reduced. But still the common source inductance exists due to the traces in PCB and this common source inductance along with the gate to drain capacitance forms an LC path during switching transients which is responsible for false turn

on [7]. By optimally designing the PCB tracks in between gate and power loops, it is possible to reduce the common source inductance value and thus restrict the false turn on to some extent.

4. **Anti-parallel diode/cascode configuration**: Adding a Si diode in parallel does improve the problem of false turn on [7] – [11]. But again, the mismatch in the parasitic inductances of both GaN and Si is an issue. Therefore, adding a diode in parallel is less useful in comparison to methods stated above.

2.5 Contributions and Limitations of Earlier Works

This section highlights the main contributions of previous works on instability issues, primarily false turn-on, switching loss models, and measuring inductances as well as their limitations so that the basis for three main contributions of this thesis can be outlined to further contribute to this research area.

In [14] – [20] instability issues in different topologies for wide bandgap devices have been addressed but mainly [16] – [18] present an analytical approach considering both gate and power circuit parameters and derives stability based on them. The model in [20] analyzes the false turn-on problem with the help of intrinsic capacitances and relates this to high slew rate dv/dt, an inherent property of GaN devices, but with a few limitations. The work tries to explain the false turn-on issue by deriving an expression for gate voltage in relation to Miller voltage. But the phenomenon of false turn-on depends on transconductance, parasitic inductances and other parameters as well as explained in [16], [17]. The impact of false turn-on events on the switching performance of MOSFETs have been addressed in [21]-[26] but the analysis involves presence of a body diode which is absent in GaN [1], [4] thus will not be applicable.

Recent research works focusing on gate circuit design techniques and switching loss models for different types of GaN transistors (both cascode and enhancement mode) have been proposed in [27] – [40]. In [27], especially an analytical loss model is presented for cascode GaN devices, which is different from the enhancement mode GaN HEMT. Similarly, [28] and [29] have presented an analytical switching model with the detailed parasitic parameters involved but it is not suitable for high-voltage GaN HEMTs as the switching transition considers the plateau voltage as fixed which is the property of Si MOSFETs not GaN-HEMTs. In [30], [31], a switching model has been developed based on the parameters taken from the static I-V and C-V characteristic but this model can only be solved with a numerical approach. This makes the model complex to compute.

All these models still lack accuracy and require complex numerical models for computation and are being suggested for mainly low voltage GaN devices. Also, the work in [32] – [46] tries to overcome these challenges and suggests different topologies such as resonant converters subjected to false turn-on issues, loss mechanisms in these topologies, and techniques for gate circuit design to mitigate the issue of false turn-on, but none of them focuses on power converter efficiency.

The variation in either of the three main components of a PWM scheme, i.e., gate resistances, negative bias and deadtime, but not all of them together has been suggested in [47-67] to reduce the false turn-on events. Also, their impact on the converter performance especially on efficiency is missing in these studies. Moreover, they are mostly based on double pulse tests not full converter operation. This study especially focuses false turn-on issues on low side devices in half bridge configuration in the buck mode operation. A detailed discussion on the specifics of each of these studies has been presented in Chapter 3.

Most importantly, the false turn-on issues are more prominent in half-bridge topologies and have the capability of short circuit because the low and high side devices have the tendency to affects characteristics of each other during on and off transients [61], [68]. This is why in this regard, the reliability of GaN converters should be improved for better operation in various applications including electric vehicles, data centers, wireless, and others where half-bridge hard-switched topologies are widely used [69]-[74].

Another notable issue which requires attention is the accurate estimation of dominant hard switching losses for GaN converters so that better thermal designs can be made [71], [72], [75], [76]. The previous studies in [28], [29], [31], [77], [78] suggesting switching models for enhancement mode GaN devices are either limited to low voltages only or cannot be simply applicable with changing gate drive parameters especially with different negative biases. A detailed discussion on the specifics of these works is presented in Chapter 4. This forms the basis for deriving a simple multi-parameter high voltage hard-switching loss model with better accuracy which is the second contribution of this thesis.

High dv/dt related oscillations leading to false turn-on events in GaN converters occurs because of their low threshold voltages and internal capacitances compared to conventional Si devices [79], [80]. Most importantly the main contributor to false turn-on events are the parasitic inductances [81]-[96] which can usually be measured only by using specific techniques like time domain reflectometry (TDR) or network analyzers [85]-[87]. A detailed discussion on the specifics of these studies is presented in Chapter 5. Therefore, there is a need to suggest a simpler measurement algorithm for measuring parasitic inductances which can be applied using simple laboratory instruments and thus this forms the third contribution of this thesis.

Chapter 3: Balancing PWM Control for Efficiency and Reduction of False Turn-on Events in Synchronous Buck GaN Converters

3.1 Overview

Half-bridge GaN power converters are susceptible to false turn-on events, which can lead to shoot-through and potentially device-damaging currents. There are three main parameters that can be adjusted in PWM schemes to reduce the likelihood of false turn-on events: negative gate bias, gate resistance, and deadtime. However, these PWM parameters also affect converter efficiency in the inverse way, meaning less false turn-on events must be balanced with lowered efficiency.

This chapter presents a novel approach to investigate the trade-off between reducing GaN false turn-on events (by reducing the transient peak of gate to source voltage) on low side devices in half bridge configuration and maximizing the power converter efficiency, which has not been done in prior work. The investigation in this works presents a trade-off using a synchronous buck converter over numerous operating points with variation of the three key PWM parameters. Six converter scenarios are considered with input voltage of 200/400V, switching frequency of 50/100kHz, and output power of 500W/1kW. For each scenario, negative gate bias is set to -4.4V

and -5V, gate on-resistance is set to 10Ω and 12.5Ω, and deadtime is varied at 60ns, 80ns, and 110ns.

The experimental results are organized into Pareto plots to find optimal points for efficiency and reduction of false turn-on events. The experimental results in the later part of the chapter clearly show that a further negative gate bias (-5V) most significantly reduces the false turn-on voltage peak and still achieves very high efficiency with appropriate selection of gate resistance and deadtime which is the main outcome of this work.

3.2 Introduction

Due to having low losses and the capability of attaining very high switching frequencies, GaN switching devices are excellent options for power converters requiring high efficiency and low volume. A market study in [6] predicts that GaN power converters will show an annual growth rate of almost 30% in the coming years. Since their inception in the late 1970s, the GaN-HEMT structure had been mainly used in RF applications; however, in 2009, Efficient Power Conversion developed the first enhancement mode GaN on silicon (Si) FETs as power MOSFETs.

The HEMT structure demonstrates an unusually high electron mobility with two-dimensional electron gas in the region of an aluminum gallium nitride (AlGaN) layer and GaN hetero structure interface [1]. Thus, even though the GaN-HEMT structure is fabricated on a Si substrate, it is quite different than a standard MOSFET device structure [2].

Among the available wide bandgap devices for power conversion, silicon carbide (SiC) and GaN, GaN has the highest electron mobility, saturated electron velocity, energy gap, and electric

field breakdown limit, which are the prime reasons for the focus on GaN technology for low-to-mid levels of power conversion [2], [4].

However, along with the benefits of new GaN devices comes new design challenges, such as false turn-on events and threshold voltage instability. One main concern is the reliability of GaN devices especially in half-bridge circuits due to issues like sustained gate voltage ringing which can lead to false turn-on. False turn-on is problematic because it can increase switching losses and cause a short across the two switches in a half-bridge circuit, potentially allowing device-damaging currents to flow. This restricts the reliability of the converter and can affect the performance of the whole power converter.

Instabilities like false turn-on occur in GaN devices because of very high dv/dt rates and related voltage oscillations during switching transients, due to the small internal capacitances, combined with the fact that the gate threshold voltage is relatively low, and is thus easy to exceed [7,14].

Table 3.1 shows that typical GaN devices have lower gate threshold voltages compared to conventional Si MOSFETs and SiC devices. This comparison shows typical values for the three different device types, where the data has been collected over wide voltage and current ratings from different manufactures. The low threshold voltage and maximum V_{gs} for GaN makes gate driver design challenging because there is a very narrow band of allowable voltages.

In [14], three of the most prominent types of instabilities in synchronous half-bridge circuits are explained, including an analysis based on a second-order transfer function using positive feedback and Barkhausen criteria. The first type of instability arises due to distortion in the PWM signal whereas the other two arise because of turn-on and turn-off induced oscillations on account of high dv/dt and di/dt transitions. Reference [7] uses a negative conductance oscillator to suppress these self-sustained oscillations and clearly highlights for both SiC and GaN that half-bridge circuits can

have severe instability issues, especially for GaN due to its device structure and very fast switching times.

Table 3.1. Threshold Parameters for Si, SiC and GaN-HEMT Devices

Device (Rating)	Manufacturer	$V_{th,min}$ (V)	$V_{th,typ}$ (V)	$V_{gs,max}$ (V)
MOSFET (100V/600V)	Vishay, Infineon	3	3.5	20
SiC (200V/650V)	Semikron, Cree	2.5	3	18-25
GaN (100V/650V)	GaNsystems, EPC, Transform	1.1	1.7	6-10

Though soft switching reduces the voltage ringing and crosstalk [41], [42], it requires a more complicated circuit and control algorithm. In the typical synchronous buck converter, the low-side synchronous switch turns on at ZVS since reverse conduction occurs during the deadtime before the switch is turned on. However, the high-side switch operates with hard-switching, and when it turns on with high dv/dt, the voltage oscillations affect the low-side switch, potentially raising the low-side switch gate-to-source voltage above the threshold voltage when the switch should be off.

Thus, it is desirable to study how the challenges of GaN can be mitigated in the simple and widely used synchronous buck converter. This work focuses on investigating and developing a PWM switching scheme that reduces false turn-on likelihood while maintaining high efficiency in the synchronous buck converter.

Using a negative gate bias during the switch off time enhances the gate's safe operating area which reduces false turn-on to an extent [16], [43] – [46], but a larger negative gate bias voltage increases the reverse conduction losses when the switch is off during the deadtime. This effect is exacerbated when deadtime is increased to also reduce false turn-on [43]-[45].

Furthermore, gate resistance can also be increased to reduce dv/dt and thus reduce the voltage oscillations that can lead to false turn-on, but this also increases switching losses and reduces converter efficiency [10], [45]. Also, [46] has verified that false turn-on in SiC devices directly contributes to further switching losses due to the additional unwanted current flowing through the switch, and thus this is also a concern for GaN devices. Thus, there is a critical relationship between false turn-on in GaN half-bridge circuits and converter efficiency, which has not been thoroughly explored in the previous literature.

With a larger negative gate bias, threshold voltage reduces to a lesser value, which is termed *threshold voltage instability* [47], [48]. Previous studies [47]-[52] have analyzed threshold voltage instability in detail. Reference [17] shows there is an increased risk of false turn-on for GaN devices in half-bridge configuration due to threshold voltage instability.

The charging and discharging of the device output capacitance (once in each switching cycle) provokes this problem even further [49]. Also, threshold voltage instability further results in degradation of sub-threshold swing (during the transition period before the threshold point when the device is not in the on state) as well as device transconductance [50], [51], which is unrecoverable under high negative gate bias.

Moreover, GaN power converters operating at high temperatures with extreme negative bias results in significant threshold voltage shift and higher on-resistance, inducing more losses [47]-[52]. In GaN, threshold voltage shifts without applying negative bias, and is recoverable if the negative bias is not high [53], [54]. With high negative biases, such as below -10V, threshold voltage shifts are unrecoverable introducing trap defects in the device and can be understood with the help of hole induced degradation model [55]. Therefore, it is recommended to confine these negative biases within an optimal range [40], [56].

The novel contribution of this work is that it investigates the trade-off between reducing the risk of false turn-on events and achieving high converter efficiency. The proposed investigation uses the whole converter in full operation while varying all three of the critical PWM parameters: gate resistance, negative gate bias, and deadtime.

Though much prior work has analyzed GaN device performance, none has focused on a quantitative investigation of the trade-off between reliability and efficiency. For example, [14] and [7] investigate how to mitigate false turn-on events by altering gate resistance, but do not quantify the effects on efficiency. Reference [16] focuses on mitigating false turn-on by varying gate resistance and negative bias, but only considers converter operation up to 50 V and does not quantify the effect on efficiency.

References [43] – [45] focus on reducing oscillations and mitigating crosstalk by varying gate resistance, but only perform the double pulse test (which cannot account for heating effects) and do not focus on efficiency. Reference [48] considers both gate resistance and negative bias in investigating the switching transient and threshold voltage instability, but does not focus on false turn-on events or efficiency.

Dynamic on-resistance is investigated in [52], [57], and [58]. Furthermore, [59] and [60] investigates bootstrap capacitor behavior and designing gate drive respectively varies gate resistance and deadtime only without any relation to efficiency by performing full converter test. In [20] switch voltage slew rate is investigated, which is related to false turn-on events, but only variation in gate resistance is considered, and efficiency is not discussed in detail. Finally, [61] and [63] discuss the model to reduce false turn-on events based on non-linear capacitance and parasitic inductances, but focus only on gate resistance and negative bias PWM parameters, and do not consider efficiency as only double pulse tests are used.

The novelty of this work is that there is no earlier work which endorses an effective PWM strategy for half-bridge eGaN-HEMTs circuits, which can relate to both false turn-on issues and power converter efficiency with a variation in all the three critical PWM parameters: gate resistance, negative bias and deadtime. In this investigation, the trade-off between converter reliability (i.e., false turn-on from voltage oscillations) and efficiency is thoroughly analyzed in order to recommend ideal PWM strategies.

Section 3.3 describes the fundamental problem of instability of GaN in half-bridge circuits, followed by Section 3.4 which presents an analysis of how the PWM scheme affects false turn-on and efficiency, and then Section 3.5 presents experimental results and discussion. Finally, Section 3.6 presents the conclusion of this work involving the investigation of reducing false turn-on events and balancing converter efficiency at the same time.

3.3 Instability in Half bridge GaN Circuits

The half-bridge synchronous buck GaN topology poses larger instability concerns than a single switch because the characteristics of one device affects the other during on and off transients. Fig. 3.1 shows false turn-on in the low-side GaN device in a synchronous buck converter. The root cause of the false turn-on is that after the low-side switch has turned off and the deadtime has passed, the high-side switch turns on. When this occurs, the voltage across the low-side switch rises very quickly. C_{ds_l} is charged, which results in C_{gd_l} and C_{gs_l} being charged as well. The displacement current from the high *dv/dt* flows through C_{gd_l} to the gate node, and then some of this current flow through C_{gs_l}. Due to the Miller Effect, enough displacement current may flow such that V_{Cgs_l} exceeds the gate threshold voltage, hence the term *Miller Turn-On*.

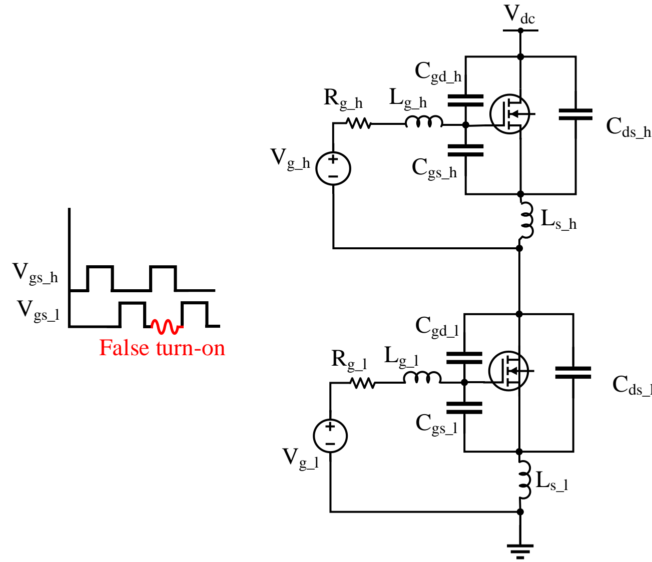


Fig. 3.1. False turn-on of GaN in half bridge circuits

Furthermore, with the high *di/dt*, a voltage is created across the common-source inductance, which increases the effective V_{gs}, pushing the gate-source voltage closer to the threshold voltage. In general, the fast-switching transients of GaN combined with the low device capacitances, the capacitive coupling between the high-side and low-side devices in the half-bridge configuration, and the inevitable parasitic inductances create voltage oscillations during the switching transient period. Fig. 3.2 shows the displacement current paths in the low-side switch (in blue) that result from the high *dv/dt* event of the high-side switch turning on while the low-side switch is off. In this case, the off-state gate voltage is shown as zero, meaning a negative gate bias is not used. This current can result in the charging of C_{gs} above the threshold voltage. Current will also flow in the red path through the gate driver, and the value of this current will depend on the impedance of the gate drive circuit, including the off resistance, $R_{g,off}$. By using KCL,

$$i_{Cgd} = i_{Cgs} + i_{Rg,off} \quad (1)$$

Thus, $R_{g,off}$ should have a low value to minimize the displacement current flowing through C_{gs}. This is one way of providing Miller compensation [40,56]. Therefore, in this work $R_{g,off}$ is kept at a constant low value (2 Ω). Fig. 3 (b) shows another, generally more effective approach for Miller compensation, which is to use a negative gate bias during the off time of the device [63]. The negative gate voltage bias charges C_{gs} to a negative voltage, which adds immunity to false turn-on because this negative voltage partially cancels out the positive voltage generated across the common source inductance during the high *di/dt* event.

Thus, the effective V_{gs} oscillations during the high-side switch turn-on transient will have a lower peak voltage, reducing the chance for false turn-on. However, since using a lower negative gate bias voltage also increases device reverse conduction losses during the deadtime, this paper performs an in-depth investigation of negative gate bias values considering converter efficiency.

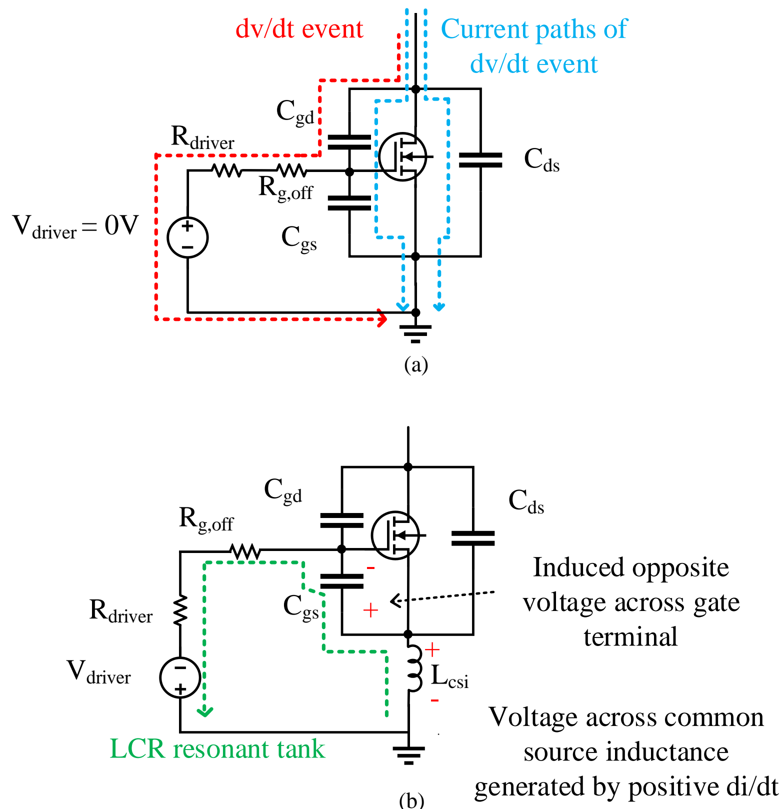


Fig. 3.2. (a) High dv/dt event current paths (b) High di/dt event due to LCR resonant tank

3.4 PWM Strategy

This section presents the three critical aspects of an effective PWM to balance converter efficiency with a reduction of false turn-on events in the synchronous buck converter: gate turn-on resistance ($R_{g,on}$), negative gate bias, and dead time selection.

3.4.1 Gate Turn-on Resistance

Since it is the turn-on of the high-side switch which causes the high *dv/dt* across the low-side switch and thus induces the gate oscillations leading to false turn-on, this paper investigates the effect of changing $R_{g,on}$ of both switches. With a larger $R_{g,on}$, the high-side switch will turn on more slowly, inducing a lower *dv/dt* across the low-side switch. Furthermore, a larger $R_{g,on}$ in the low-side switch gate drive circuit will add more damping to the resulting oscillations from the switch internal capacitances and the circuit stray inductances. Thus, it is clear that a larger $R_{g,on}$ will reduce the chances of false turn-on events. However, a larger $R_{g,on}$ will also increase turn-on switching losses in both devices due to a slower turn-on event and thus a larger overlap of voltage and current during the turn-on transition.

This work will quantify these benefits and drawbacks of using a larger $R_{g,on}$ by considering 10 Ω and 12.5 Ω values for $R_{g,on}$. The 10 Ω value is selected because it is the default recommended value by GaN Systems for use with the evaluation board [64]. The value of 12.5 Ω is selected as a 25% increase from the default value to aim to still achieve high converter efficiency while dampening switching oscillations.

3.4.2 Negative Bias

Using a negative gate bias during the off-time is a well-known method to reduce false turn-on events [16], [43]-[46], though the negative bias must be kept within a safe operating area such as higher than -10 V to prevent device damage and significant gate threshold instability. As discussed, the negative bias lowers the V_{gs_l} false turn-on peak voltage as it partially cancels out with the positive voltage generated across the common-source inductance during the high *di/dt* event.

However, a negative gate bias also increases reverse conduction losses. Though GaN devices do not contain a body diode, they can conduct reverse current through the main channel when off, similar to a body diode. A lower negative gate bias will increase the voltage drop across the switch while in the reverse conduction mode, V_{sd,rev_cond}, increasing losses [64]. Equation (2) describes this reverse conduction power loss that is proportional to V_{sd,rev_cond}, which is in turn a function of the negative gate bias, $V_{gs,off}$. In (2), I_{sd} is the reverse conducting current, t_{dead} is the deadtime, and f_{sw} is the switching frequency.

$$P_{loss,rev_cond} = V_{sd,rev_cond}(V_{gs,off}) \cdot I_{sd} \cdot 2t_{dead} f_{sw} \tag{2}$$

Thus, a moderate negative gate bias of around -3V is often recommended to minimize the extra losses associated with this reverse conduction characteristic [63,64]. This paper will quantify the benefits and drawbacks of using further negative gate biases of -4.4 V and -5 V on both false turn-on likelihood and converter efficiency.

3.4.3 Dead Time

The selection of the deadtime affects converter efficiency and false turn-on events. With a longer deadtime, the low-side switch will conduct in the reverse direction for a longer period of time in each switching cycle and these losses will also be dependent on the negative gate bias [2], as shown

in (2). However, a longer deadtime will leave more time for intrinsic capacitances in the switch to completely discharge before the high-side switch turns on, and thus can reduce false turn-on voltage oscillations.

The lower limit on a desirable deadtime is that which allows the low-side synchronous switch to turn on at ZVS, as operating without ZVS would decrease efficiency. Equation (3) shows the calculation of this limit [65], [66], [67], as the deadtime must be long enough to allow the current flowing through the switch, I_{out}, to discharge the effective device output capacitance, $C_{o(effective)}$, to discharge V_{ds} from V_{in} to zero.

$$t_{dead} \geq \frac{C_{o(effective)} V_{in}}{I_{out}} \quad (3)$$

However, modelling $C_{o(effective)}$ during the switching transient has always been an issue as the C-V curve follows a nonlinear relationship. The most conventional ways are to consider energy-related and time-related output capacitances. $C_{o(er)}$ is the capacitance which gives the same stored energy as output capacitance C_{oss} while V_{ds} increases from zero to V_{in} based on the principle of conservation of energy, and $C_{o(tr)}$ is the capacitance which gives the same charging time as C_{oss} while V_{ds} increase from zero to V_{in}. Choosing the maximum of $C_{o(tr)}$ and $C_{o(er)}$ gives a reasonable approximation of Co(effective) as shown in (4).

$$C_{o(effective)} = \max(C_{o(er)}, C_{o(tr)}) \quad (4)$$

The GS66516T datasheet gives the values of $C_{o(er)}$ = 207 pF and $C_{o(tr)}$ = 335 pF, meaning $C_{o(effective)}$ should be 335 pF. This research investigates three combinations of V_{in} and I_{out} (400V/5A, 200V/5A, and 200V/10A). According to (3), the most stringent limit on deadtime is 400V/5A, which requires a minimum deadtime of 27 ns. The GaN Systems' evaluation board used in this investigation has a lower deadtime limit of 60 ns, thus these experiments will start at this

lower limit and step up in small increases, also testing 80 ns and 110 ns deadtime. The calculations from (3) and (4) show that all experiments will have ZVS turn-on for the synchronous switch for deadtimes of 60 ns or higher.

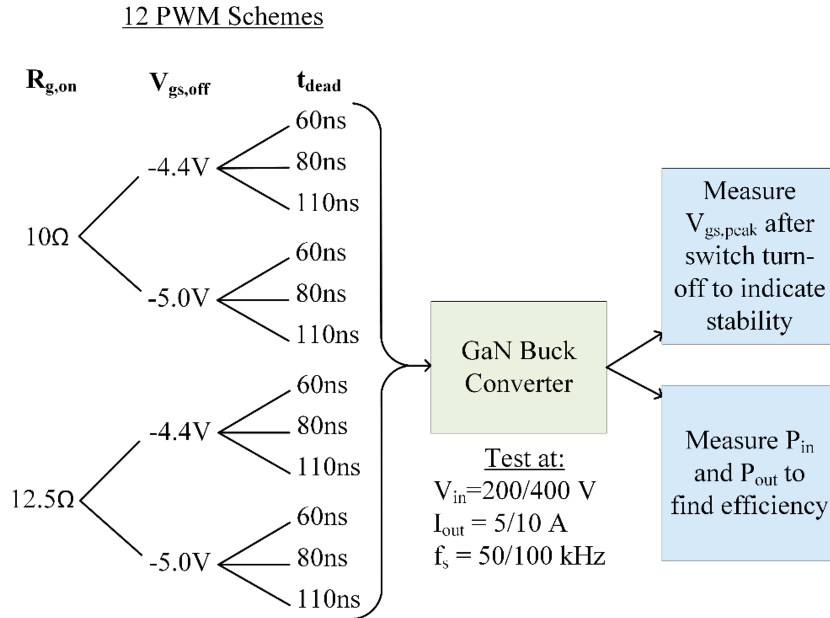


Fig. 3.3. Summary of the investigational method

3.5 Experimental Results and Discussion

The experimental circuit is a synchronous buck converter, as shown in Fig. 3.4. The circuit uses GaN Systems' GS665MB-EVB evaluation board [64] with GS66516T 650V/60A rated devices and ACPL-346 gate drivers. Table 3.2 summarizes the experimental setup parameters. Two CWS high frequency power inductors of 60 μH each are used in series along with a 20μF output capacitor.

Fig. 3.5 shows the whole experimental setup whereas Fig. 3.6 shows a closer view of the buck converter and the measurement probes. In Fig. 3.5, the experimental setup includes a Sorensen SGX

programmable DC power supply and a Chroma 63804 programmable AC/DC electronic load, which is used to maintain either a constant 5 A load current (for tests with

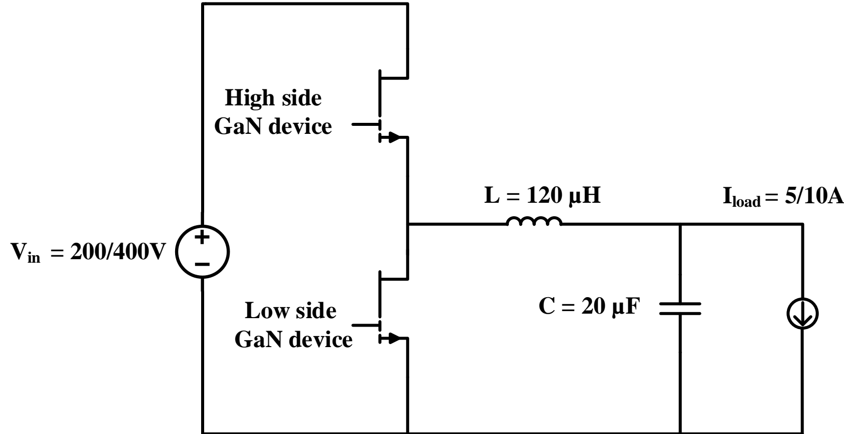


Fig. 3.4. Synchronous Buck converter test circuit

400 V and 200 V input voltage) or a constant 10 A load current (for tests with 200 V input voltage). The Tektronix MSO54 4-channel 500 MHz mixed signal oscilloscope is used. The high-side switch V_{gs} and V_{ds} are measured with TMDP0200 differential probes with 200 MHz bandwidth. The low-side switch V_{gs} is measured with the ISoVu 500 MHz probe (tripod) as shown in Fig. 3.6.

Table 3.2. Experimental Setup Parameters

Parameter	**Value**
DC input voltage	200, 400 V
DC load output	5, 10 A
Switching frequency	50, 100 kHz
Duty cycle	50%
Power inductor	2 × 60 µH
Input/output capacitor	20 µF
Gate turn-on resistance	10, 12.5 Ω
Gate turn-off resistance	2 Ω
Negative bias	-4.4, -5.0 V
Dead time	60, 80, 110 ns

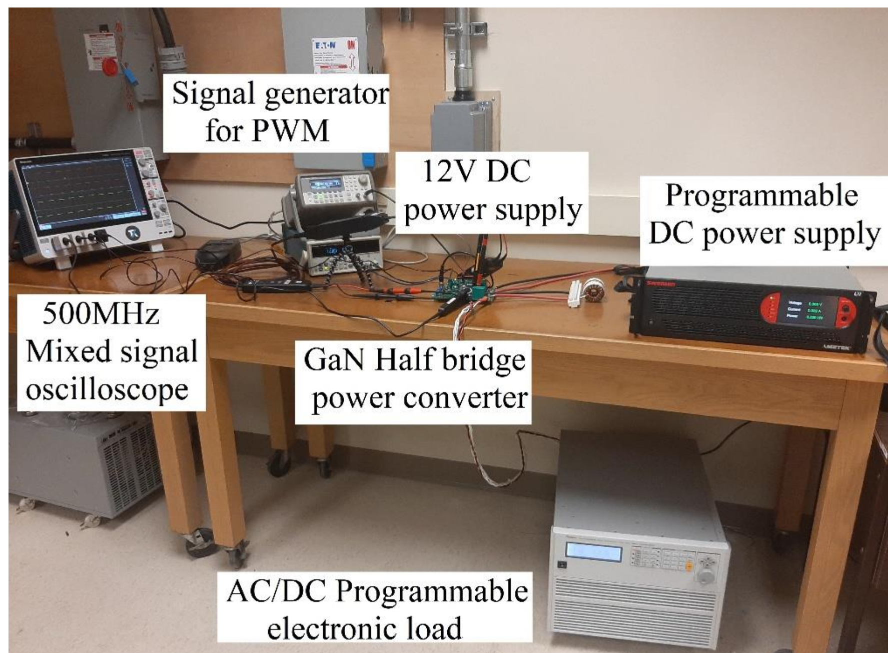


Fig. 3.5. Experimental setup

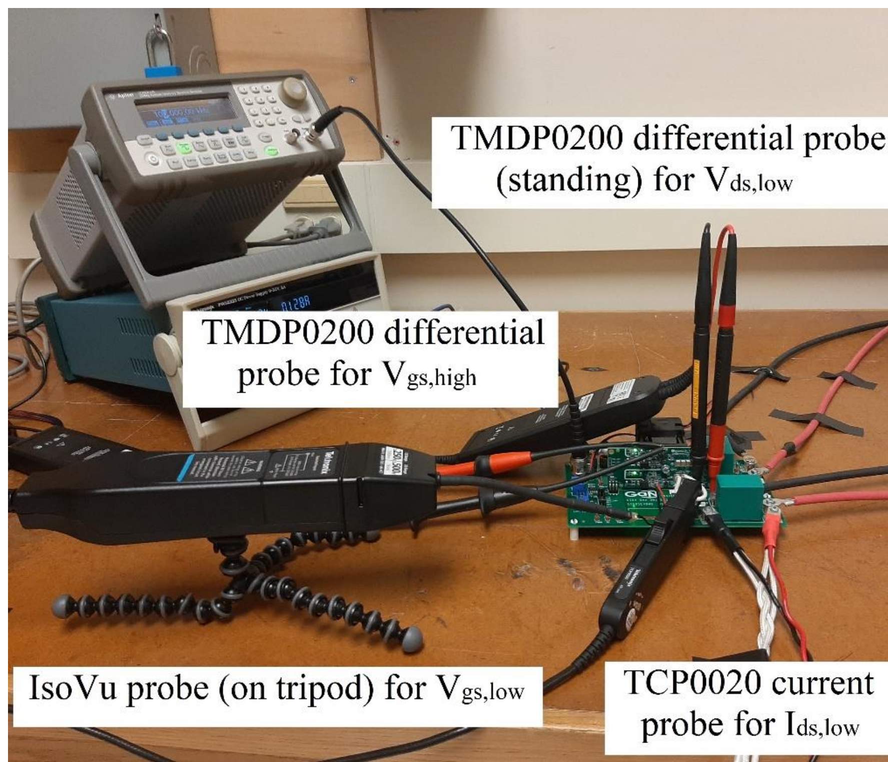
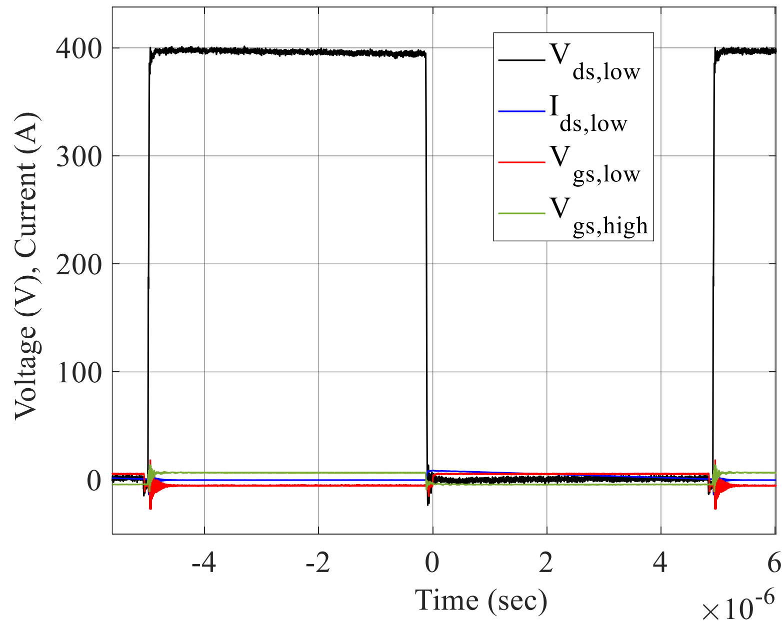


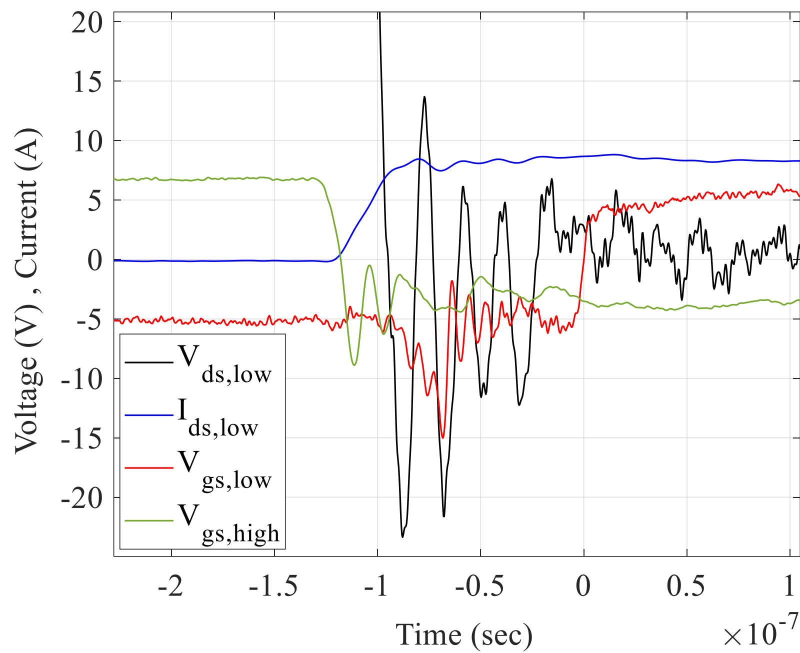
Fig. 3.6. Measurement setup with different probes

The low-side switch current is measured with the TCP0020 current probe with 50 MHz bandwidth. The bipolar gate drive signal is produced using a 5-11V DC/DC converter which generates a dc rail that is split into positive and negative terminals. The positive terminal is set by a Zener regulator circuit which has an RC divider branch coupled to it. The output of the DC/DC converter is fed into the isolated ACPL-P346 gate driver which drives the high and low eGaN-HEMTs separately. The Zener regulator provides a particular bipolar PWM signal so that two different bipolar PWM signals +6.2/-4.4V and +5.6/-5V can be generated.

Fig. 3.7 (a) shows the measured switching waveforms of the circuit for V_{in} = 400 V, f_{sw} = 100 kHz, $R_{g,on}$ = 10 Ω, and $V_{gs,off}$ = -5 V. Fig. 3.7 (b) and (c) show zoomed-in version of the turn- on and turn-off transitions for the low-side switch.



(a)



(b)

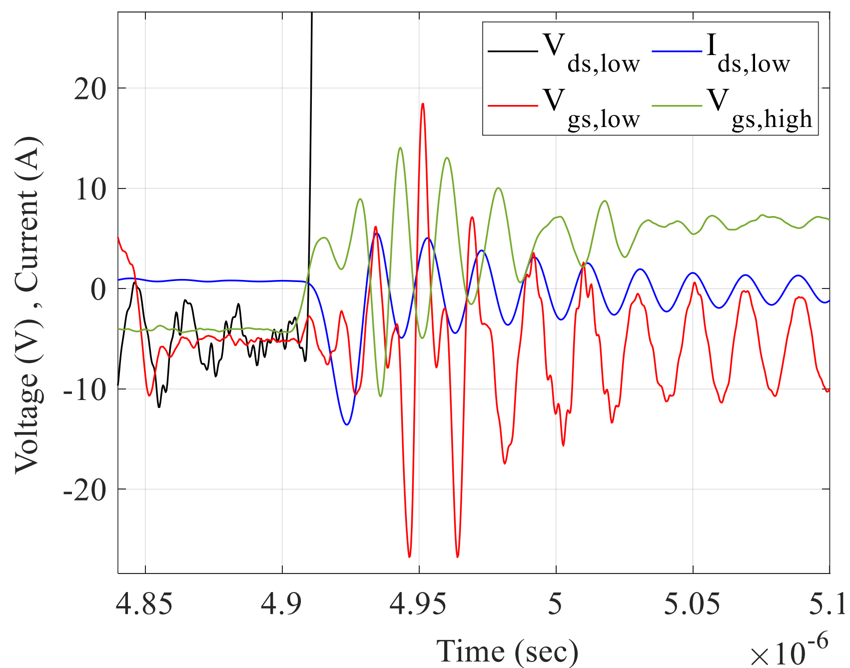


Fig. 3.7. (a) Voltage and current switching waveforms for Vin = 400V, Rg,on = 10 Ω, Vgs,off = -5 V, (b) Zoomed-in view of low-side switch turn-on, (c) Zoomed-in view of low-side switch turn-off

In Fig. 3.7 (c), it can be seen that when the low-side switch has turned off and the high-side switch turns on, $V_{gs,low}$ has a voltage oscillation peak of 19.5 V, well above the typical threshold voltage of 1.7 V. Also, in Fig. 3.7 (b), when the high-side switch has turned off and the low-side switch turns on, $V_{gs,high}$ oscillations are not significant. This result shows that the low-side switch is the primary concern for false turn-on events and agrees with findings [10], [45]. The rate of rise of the voltage of the low-side switch is primarily determined by the turn-on speed of the high-side switch, which is dependent on $R_{g,on}$.

(c)

Table 3.3 shows how the drain-to-source dv/dt of the low-side switch varies with V_{in}, $R_{g,on}$, $V_{gs,off}$, and t_{dead} for 100 kHz switching frequency at 200 and 400 V input and at 1 kW output power. For V_{in} = 200 V, $R_{g,on}$ = 10 Ω produces an average $dV_{ds\text{-}low}/dt$ of 27.7 V/ns and $R_{g,on}$ = 12.5 Ω produces an average $dV_{ds\text{-}low}/dt$ of 25.7 V/ns. For V_{in} = 400 V, $R_{g,on}$ = 10 Ω produces an average $dV_{ds\text{-}low}/dt$ of 49.8 V/ns and $R_{g,on}$ = 12.5 Ω produces an average $dV_{ds\text{-}low}/dt$ of 45.8 V/ns.

Fig. 3.8 shows the $V_{gs,low}$ waveforms for V_{in} = 400 V, f_{sw} = 100 kHz, I_{load} = 5 A, and deadtime = 80 ns for four different test cases of negative gate bias and $R_{g,on}$ after the low-side switch is turned off and when the high-side switch is turned on (after the deadtime). The peak $V_{gs,low}$ voltage value during this time is selected as a metric to measure the likelihood of a false turn-on event occurring. Fig. 3.8 shows that the -4.4 V gate bias leads to a higher $V_{gs,low}$ peak for both $R_{g,on}$ values tested, and that this peak is well over the nominal threshold voltage of 1.7 V. However, the -5 V gate bias reduces these oscillation peaks.

Fig. 3.9 summarizes the efficiency results for all six test cases. Increasing the deadtime (within the selected range) had the smallest effect on efficiency for all cases. Increasing the negative gate bias from -4.4 V to -5 V (solid lines to dashed lines) causes a moderate drop in efficiency.

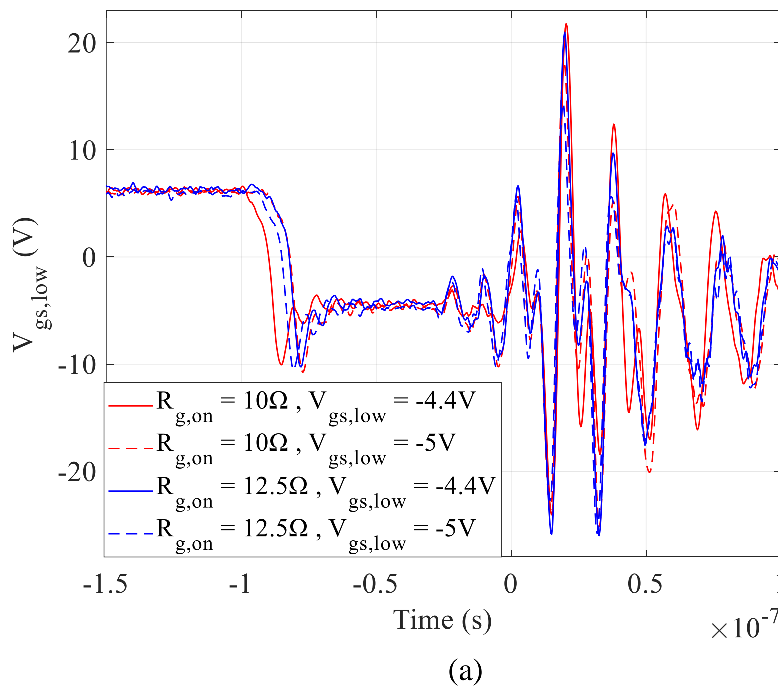
Table 3.3. Slew Rates of the Low-Side Switch for 1kW Tests

V_{in} (V)	$R_{g,on}$ (Ω)	$V_{gs,off}$ (V)	t_{dead} (ns)	$dV_{ds\text{-}low}/dt$ (V/ns)
200V	10 Ω	-4.4 V	60	28.571
			80	28.231
			110	27.891
		-5 V	60	27.431
			80	27.106
			110	26.872
	12.5 Ω	-4.4 V	60	26.456
			80	26.167
			110	26.002
		-5 V	60	25.992
			80	25.739
			110	24.981
400V	10 Ω	-4.4 V	60	51.003
			80	50.988
			110	50.124
		-5 V	60	49.862
			80	49.013
			110	48.567
	12.5 Ω	-4.4 V	60	47.891
			80	47.040
			110	46.845
		-5 V	60	45.745
			80	44.934
			110	43.687

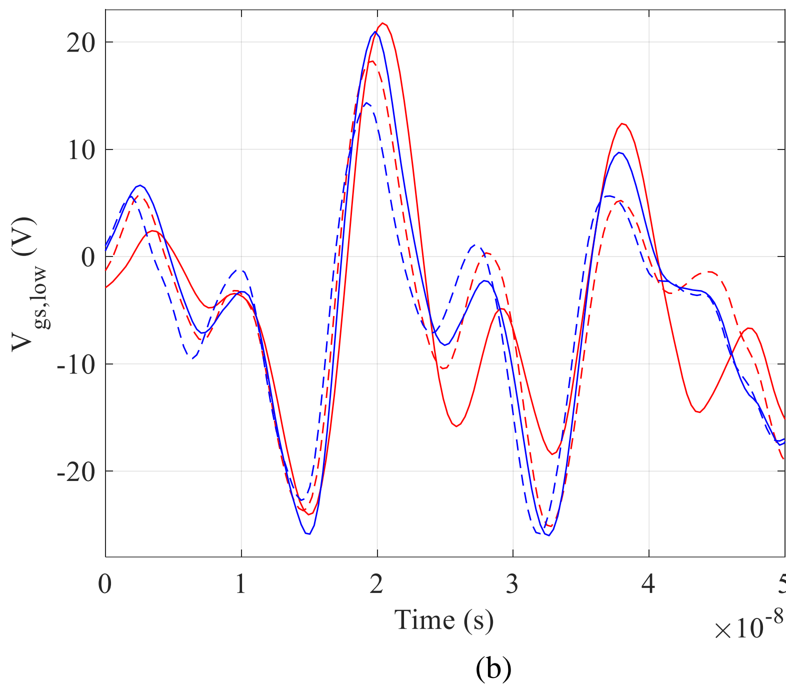
Fig. 3.10 presents the results in Pareto plots such that the lower left corner is the optimal operating point of high efficiency and low false turn-on peak voltage. Thus, it combines the efficiency results with measured peak V_{gs} values of the low-side switch measured at the moment when the high-side switch turns on, i.e., after the low-side switch has turned off and the dead time has passed. Fig. 3.10 shows that for the 200 V test at both 500 W and 1 kW power levels, increasing the deadtime makes little difference in peak V_{gs} (less than 1V), but lowers efficiency, so is not recommended. Thus, the minimum deadtime of 60 ns is recommended for 200 V operation at either power level or switching frequency.

For the 200 V cases, lowering $V_{gs,off}$ from -4.4 V to -5 V has the largest influence on reducing the false turn-on peak voltage, and thus on reducing the potential for false turn-on events. Increasing $R_{g,on}$ to 12.5 Ω (blue lines vs. red lines) slows down the switch transition at turn-on, increasing turn-on switching losses, and leading to lower efficiency compared to $R_{g,on}$ = 10 Ω.

These results show that the value of $R_{g,on}$ has a relatively large influence on efficiency, compared to the effects of increasing deadtime or negative bias. By keeping the deadtime low (at 60 ns) it is possible to achieve very high efficiency even at the lower value of negative gate bias i.e -5V, despite with the larger reverse conduction losses. The highest efficiency is obtained with 60 ns deadtime, $R_{g,on}$ = 10 Ω, and $V_{gs,off}$ = -4.4 V.

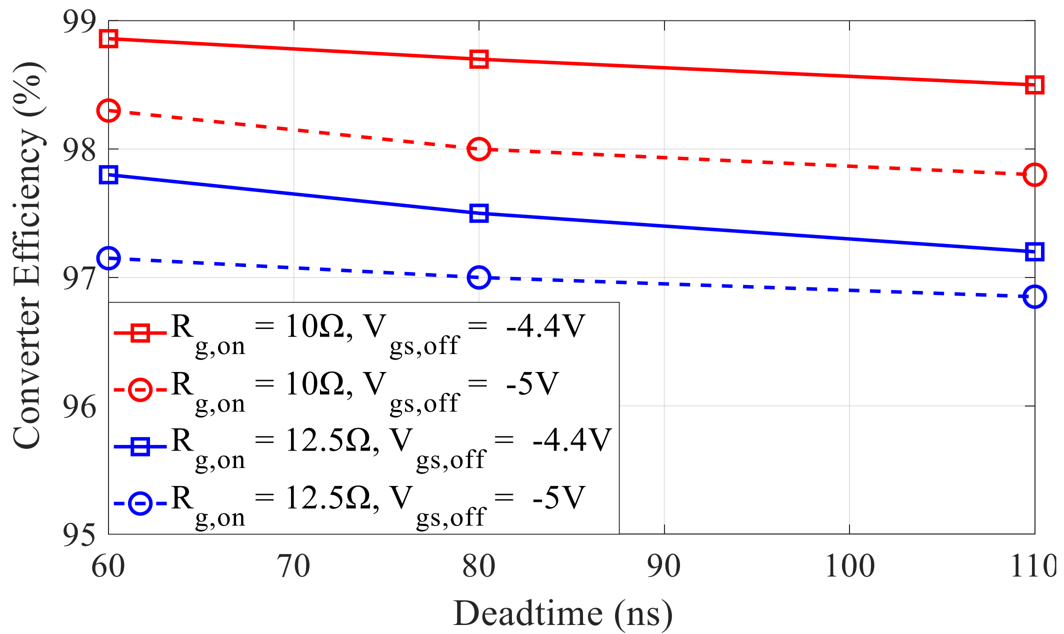


(a)

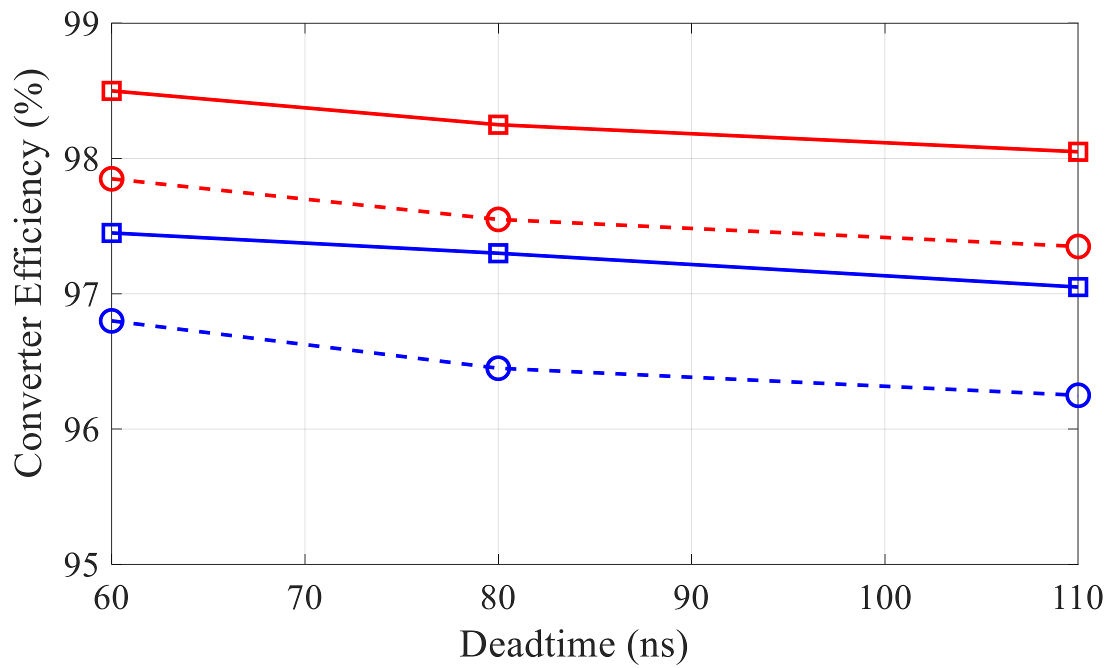


(b)

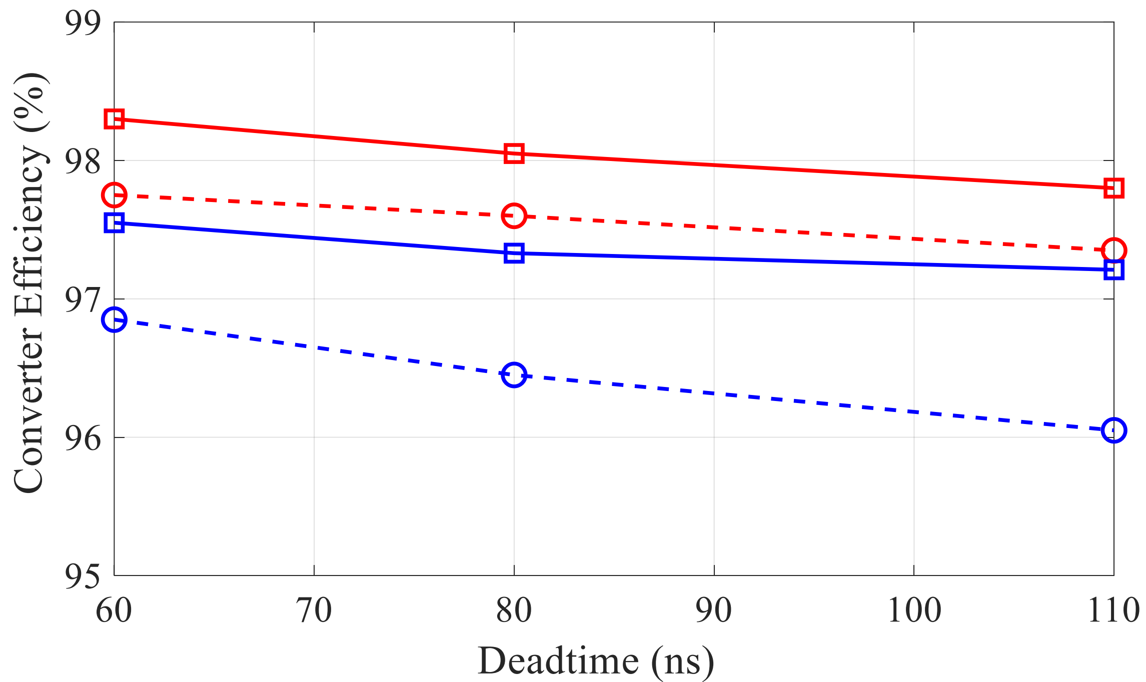
Fig. 3.8. $V_{gs,low}$ measurements for Vin = 400V and fsw = 100 kHz for four different test cases of negative bias and Rg,on (a) zoomed out (top) (b) zoomed-in (bottom)



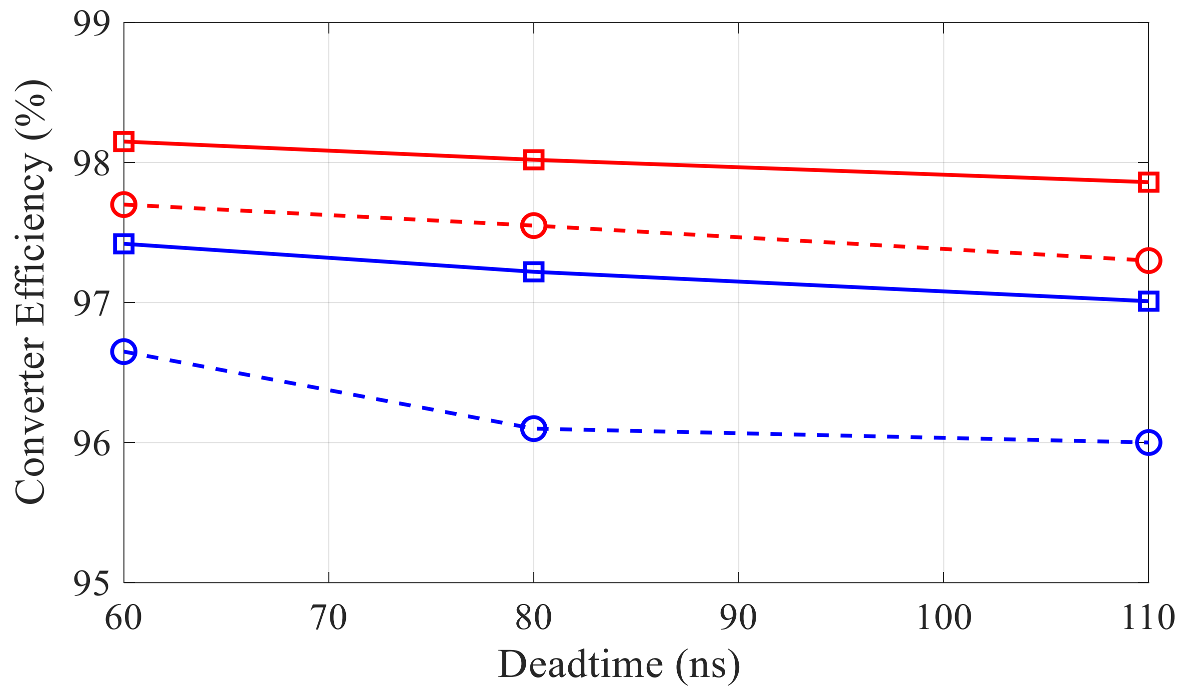
(a) V_{in} = 200V, f_{sw} = 50 kHz, I_{out} = 5A, P_{out} = 500 W



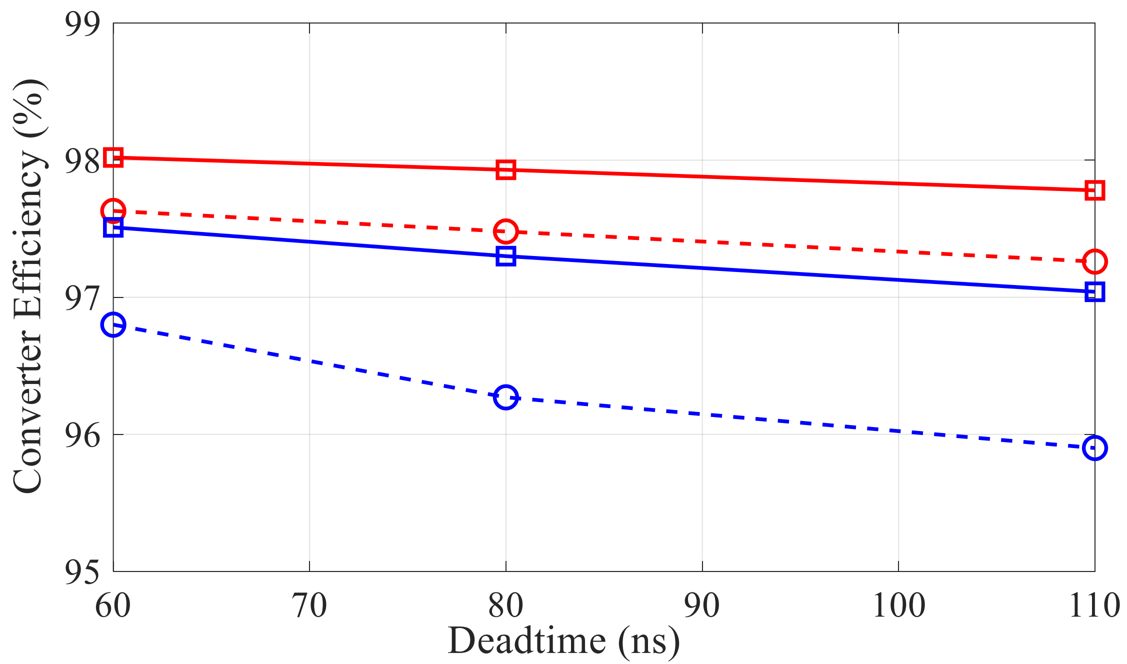
(b) V_{in} = 200V, f_{sw} = 100 kHz, I_{out} = 5A, P_{out} = 500 W



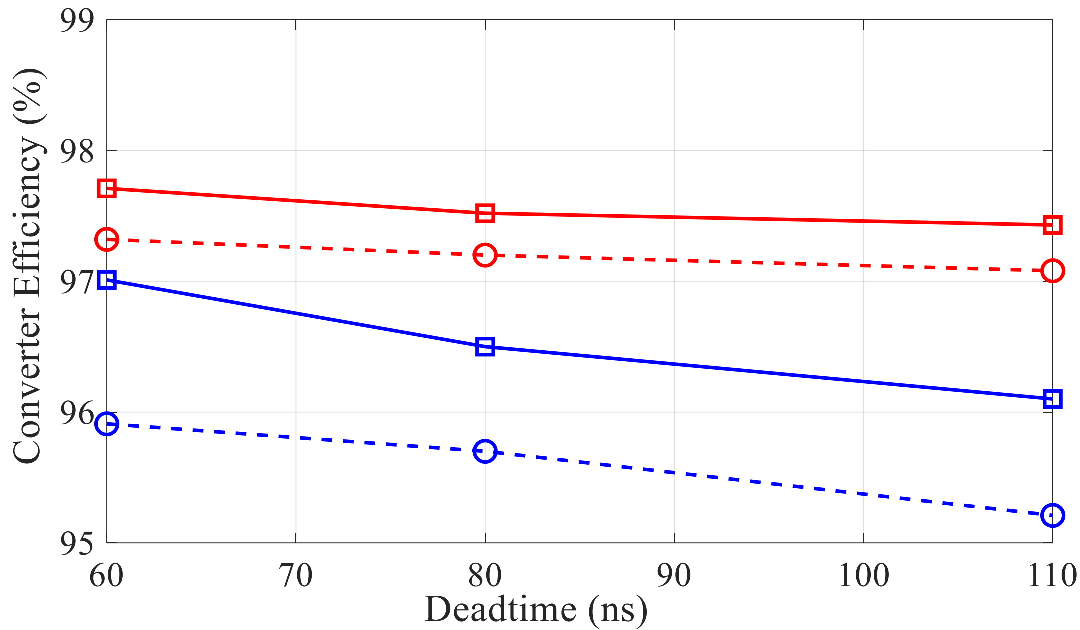
(c) V_{in} = 200V, f_{sw} = 50 kHz, I_{out} = 10A, P_{out} = 1kW



(d) V_{in} = 200V, f_{sw} = 100 kHz, I_{out} = 10A, P_{out} = 1k



(e) V_{in} = 400V, f_{sw} = 50 kHz, I_{out} = 5A, P_{out} = 1kW



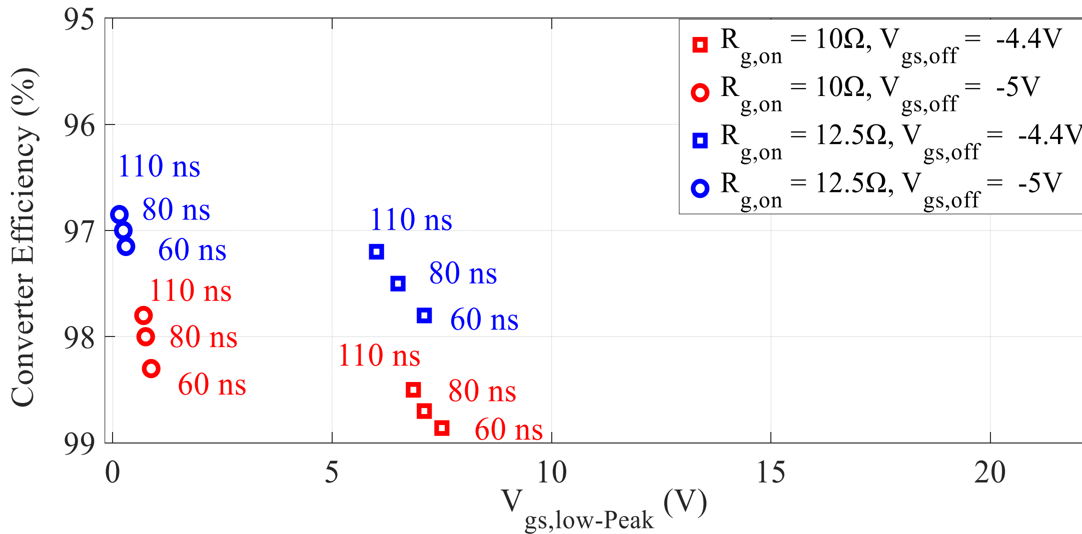
(f) V_{in} = 400V, f_{sw} = 100 kHz, I_{out} = 5A, P_{out} = 1kW

Fig. 3.9. Converter efficiency measurements for different values of converter input voltage, switching frequencies and output power.

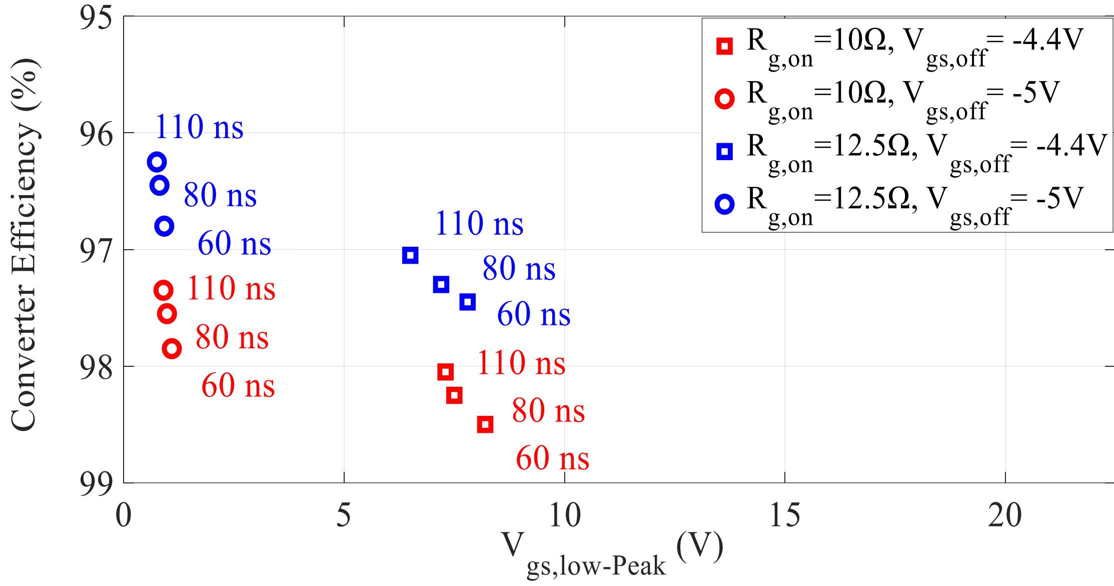
It can be seen in Fig. 3.10 that at 200 V and at both power levels, the average reduction in peak $V_{gs,low}$ by using $V_{gs,off}$ = -5 V is 6 to 7 V. For the 200V/500W case (Fig. 3.10 (a) and (b)) all tests with $V_{gs,off}$ = - 4.4 V (square markers: all deadtimes, both $R_{g,on}$ values) had peak $V_{gs,low}$ values over 6 V, meaning over the device threshold voltage, and instead using $V_{gs,off}$ = -5 V lowered all peak $V_{gs,low}$ values to below the threshold voltage (circle markers). For 200 V at both power levels, using higher $R_{g,on}$ = 12.5 Ω (compared to 10 Ω) makes little difference in peak $V_{gs,low}$, but reduces efficiency by about 1%, and is thus not recommended. Thus, $R_{g,on}$ = 10 Ω is recommended. Overall, for 200 V operation, to achieve a good balance of reliability and efficiency, the Pareto plot results indicate a recommendation of $V_{gs,off}$ = -5V, $R_{g,on}$ = 10 Ω, and deadtime = 60 ns. For 400 V operation, Fig. 3.10 shows that increasing the deadtime makes a more significant reduction in peak $V_{gs,low}$ than for 200V operation. Thus, at 400V, it is recommended the engineer use deadtime as a

fine adjustment for favoring either reliability or efficiency. For 400 V operation, the use of $V_{gs,off}$ = -5 V (compared to -4.4 V) improves peak $V_{gs,low}$, lowering it by about 2 to 4 V, while decreasing efficiency slightly. The largest influence on peak $V_{gs,low}$ is by gate resistance, where using $R_{g,on}$ = 12.5 Ω (compared to 10 Ω) reduces peak $V_{gs,low}$ by about 3 to 5V.

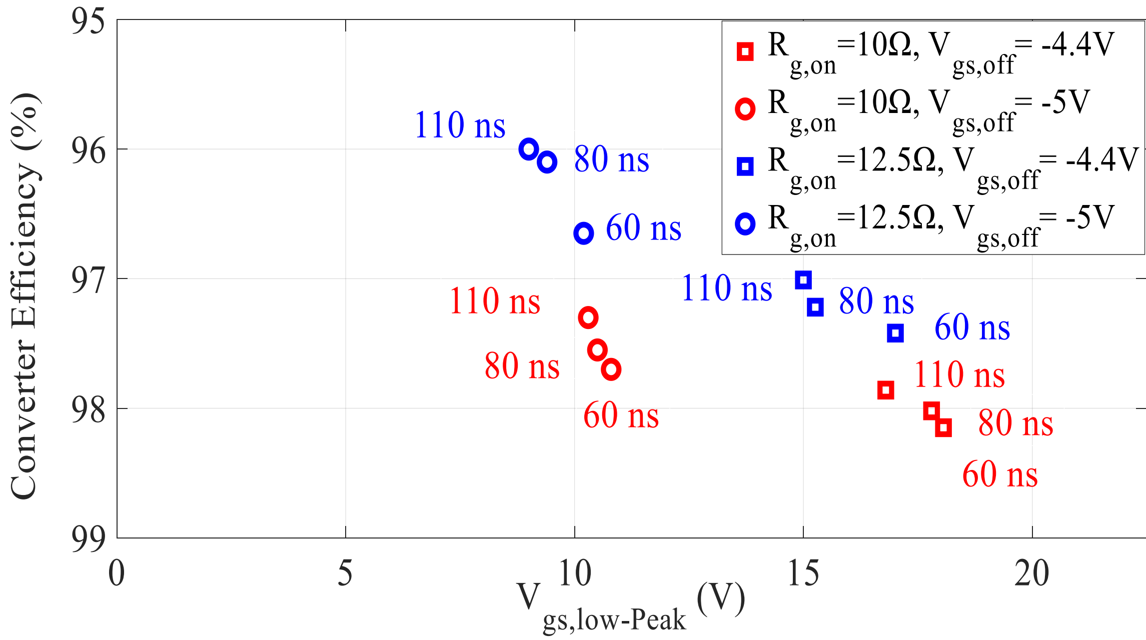
However, it also has the largest influence on efficiency, with the higher $R_{g,on}$ (12.5 Ω) reducing efficiency by up to 1.5%. Overall, the 400V Pareto plots indicate the following: If reliability is of the highest concern, it is recommended to use $V_{gs,off}$ = -5 V, $R_{g,on}$ = 12.5 Ω, and deadtime =110 ns. If it is most important to have a good balance between reliability and efficiency, the recommended PWM strategy is $V_{gs,off}$ = -5V, $R_{g,on}$ = 10 Ω, and to completely remove the false turn-on $V_{gs,low}$ peak for 400 V operation.



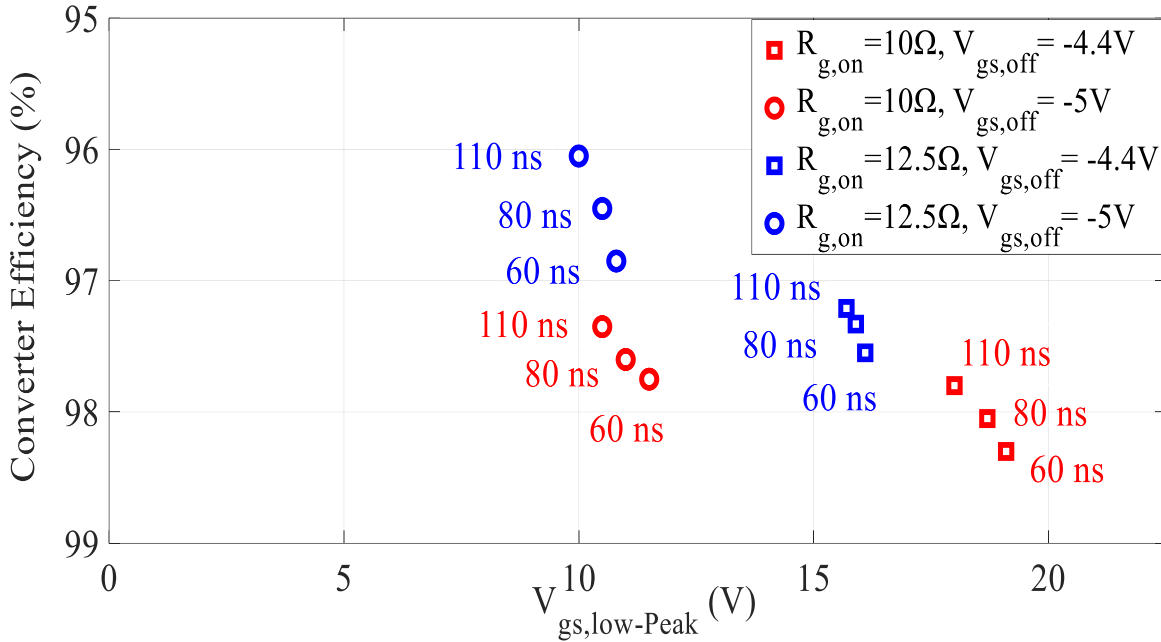
(a) V_{in} = 200V, f_{sw} = 50 kHz, I_{out} = 5A, P_{out} = 500 W



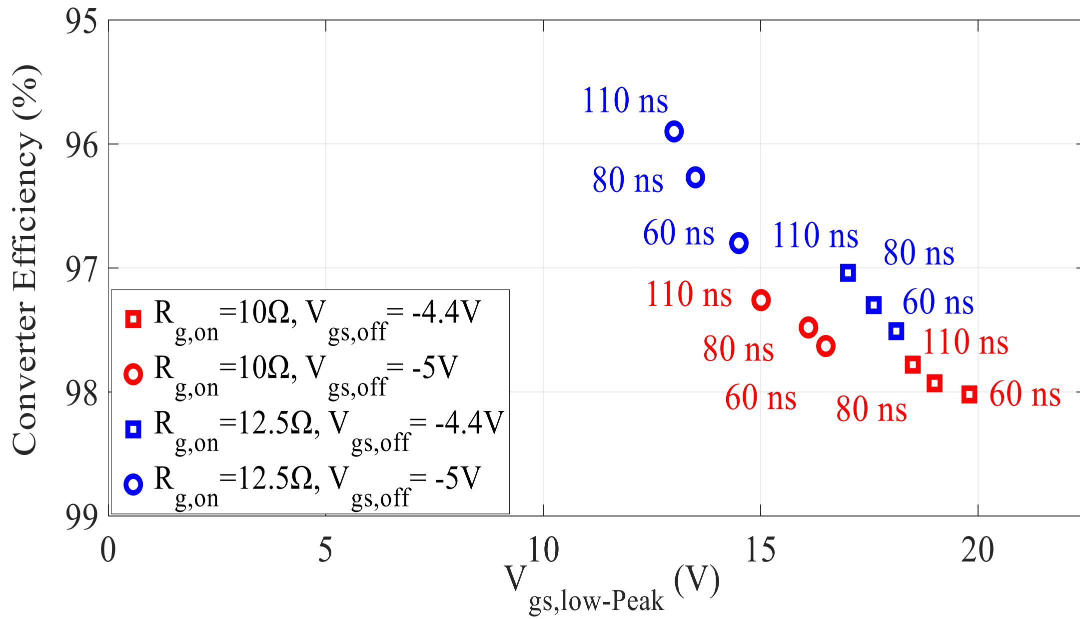
(b) V_{in} = 200V, f_{sw} = 100 kHz, I_{out} = 5A, P_{out} = 500 W



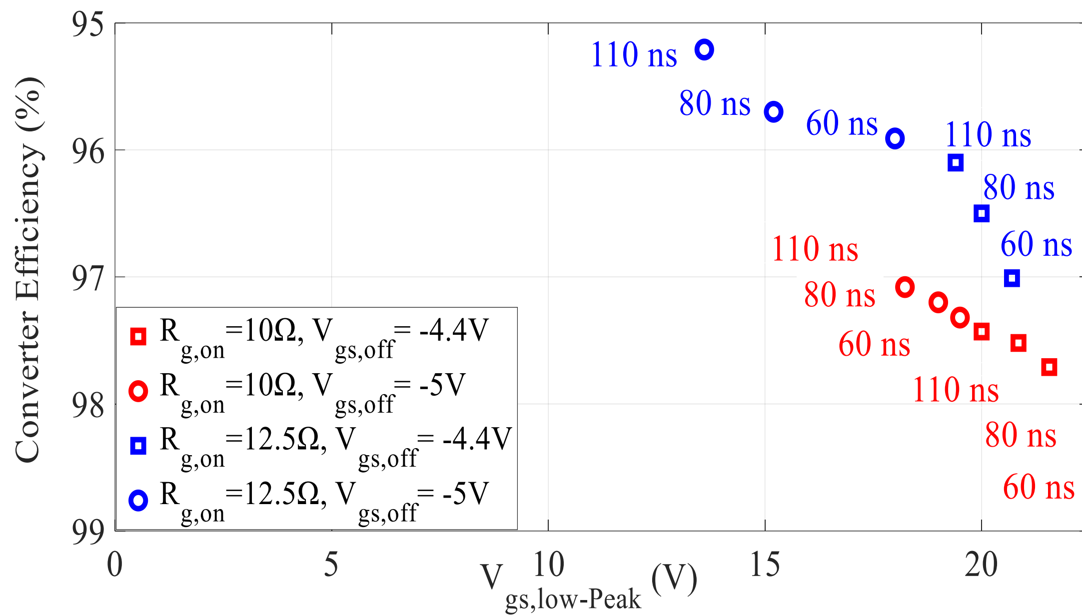
(c) V_{in} = 200V, f_{sw} = 50 kHz, I_{out} = 10A, P_{out} = 1kW



(d) V_{in} = 200V, f_{sw} = 100 kHz, I_{out} = 10A, P_{out} = 1kW



(e) V_{in} = 400V, f_{sw} = 50 kHz, I_{out} = 5A, P_{out} = 1kW



(f) V_{in} = 400V, f_{sw} = 100 kHz, I_{out} = 5A, P_{out} = 1

Fig. 3.10. Pareto plots of converter efficiency vs. Vgs,low false turn on peak voltage at different operating points

To move further in this direction, gate resistance can be increased past 12.5 Ω, however, this will have a significant impact on converter efficiency, as evidenced by the 1.5% efficiency drop from using $R_{g,on}$ = 12.5 Ω (compared to $R_{g,on}$ = 10 Ω), and may start to erode the benefits of using GaN devices. Overall, the use of a further negative gate bias of $V_{gs,off}$ = -5 V is found to be an important part of an ideal PWM strategy balancing efficiency and reliability, and thus it is recommended that engineers should consider using more negative gate biases than the commonly recommended -3 to -4 V.

The experimental results show that, as expected, switching frequency does not play a major role in determining the dV_{ds}/dt slew rate (which impacts stability), as evidenced by the similar V_{gs} peak voltages at both 50 kHz and 100 kHz for the same other conditions. Thus, the general findings of this work are applicable to lower and higher switching frequencies commonly used in power converters.

3.6 Summary

The novelty of this work is that it investigates the tradeoffs between reducing GaN false turn-on events in low side devices in half bridge configuration and achieving high power converter efficiency, which has not been covered in prior work. The proposed investigational method includes varying all three main PWM parameters (gate resistance, negative bias, and deadtime) over a wide range of operating points in a synchronous GaN-based buck converter (where false turn-on is a more prevalent issue compared to other topologies). Reliability is estimated based on the measured peak gate voltage oscillation that occurs on the low-side switch while the high-side switch is turning on.

Overall, for 200V operation, to achieve a good balance of reliability and efficiency, it is recommended to use $V_{gs,off}$ = -5V, $R_{g,on}$ = 10 Ω, and deadtime = 60 ns. At the lower power level (500 W), this PWM strategy completely removes any risk of false turn-on, as the peak gate voltage oscillation is below the device threshold voltage.

Similarly, for 400V operation, if reliability is of the highest concern, it is recommended to use $V_{gs,off}$ = -5 V, $R_{g,on}$ = 12.5 Ω, and deadtime =110 ns. If it is most important to have a good balance between reliability and efficiency, the recommended PWM strategy is $V_{gs,off}$ = -5 V, $R_{g,on}$ = 10 Ω, and deadtime = 110 ns.

In summary, the use of a further negative gate bias of $V_{gs,off}$ = -5 V was found to be an important part of an ideal PWM strategy balancing efficiency and reliability, and thus it is recommended that engineers should consider using more negative gate biases (to -5 V) than the commonly recommended -3 to -4 V.

Future work will include expanding the investigation to other converter topologies. Furthermore, active gate drivers will be investigated to further reduce the chances of false turn-on events by dampening the gate oscillations.

Chapter 4: A Simple Multi Parameter Hard Switching Loss Model for High Voltage GaN Devices

4.1 Overview

An accurate estimation of GaN hard-switching power losses is crucial for power electronics engineers in order to predict converter performance and design optimal thermal management systems. The main contribution of this chapter lies in (1) deriving an accurate, simple, and easy to compute hard-switching loss estimation which can be used with different types of gate driver circuits and in different power operating conditions, and (2) the proposed model simply classifies the switching transition into different stages lumped into a simple equation. It clearly expresses the change at different power and device parameters. The proposed model has been compared with other works with experimental results up to 400V and 1kW output power and at numerous operating points which clearly shows its superiority.

4.2 Introduction

Gallium nitride (GaN) power converters are providing immense capabilities for a wide range of applications [2], [4], [68] especially in electric vehicles (EVs), renewable energy, data centers, and consumer electronics. GaN's fast switching speed allows for high switching frequency, leading to power converters with high power density, which is crucial for use in EVs [69], [70]. In comparison to conventional silicon (Si) MOSFETs GaN has the advantage of zero reverse recovery, negligible capacitive losses, and high transconductance which is why the switching rise and fall times are very low [14], [71], [72]. Hard-switched converters in various applications involve half-bridge circuits where the hard-switching losses deteriorate converter efficiency and performance, especially at high voltage and high switching frequency [56], [73], [74]. Power design engineers require a simple and accurate assessment of switching losses at the design stage to be able to optimize the design of the converter and the thermal management system [44], [53], [75].

The GaN-HEMT structure unlike conventional Si devices demonstrates an unusually high electron mobility with two-dimensional electron gas in the region of an aluminium gallium nitride (AlGaN) layer and GaN hetero structure interface [1], [76]. Thus, even though the GaN-HEMT structure is fabricated on a Si substrate, it is quite different than a standard MOSFET [7,15] which is why the switching analysis needs a different approach.

Fig. 4.1 shows the comparison of the overlapping period, specifically voltage and current transition time during hard-switching for conventional Si MOSFETs and GaN devices. As shown in Fig. 3.1 during the turn-on transient when the drain to source voltage falls the gate plateau voltage linearly increases in GaN devices from the minimum to maximum whereas in the Si devices it is constant. Similarly, during the turn-off when the drain to source voltage rises the gate plateau voltage

linearly decreases in GaN devices while it is constant for the gate plateau voltage. This is due to the reason that non-flat Miller plateau voltage is a characteristic feature of GaN devices [1]. Also, the gate to drain capacitance (which decides the voltage rise or fall during switching) of GaN is much lower than Si device of the same rating [2,68,71].

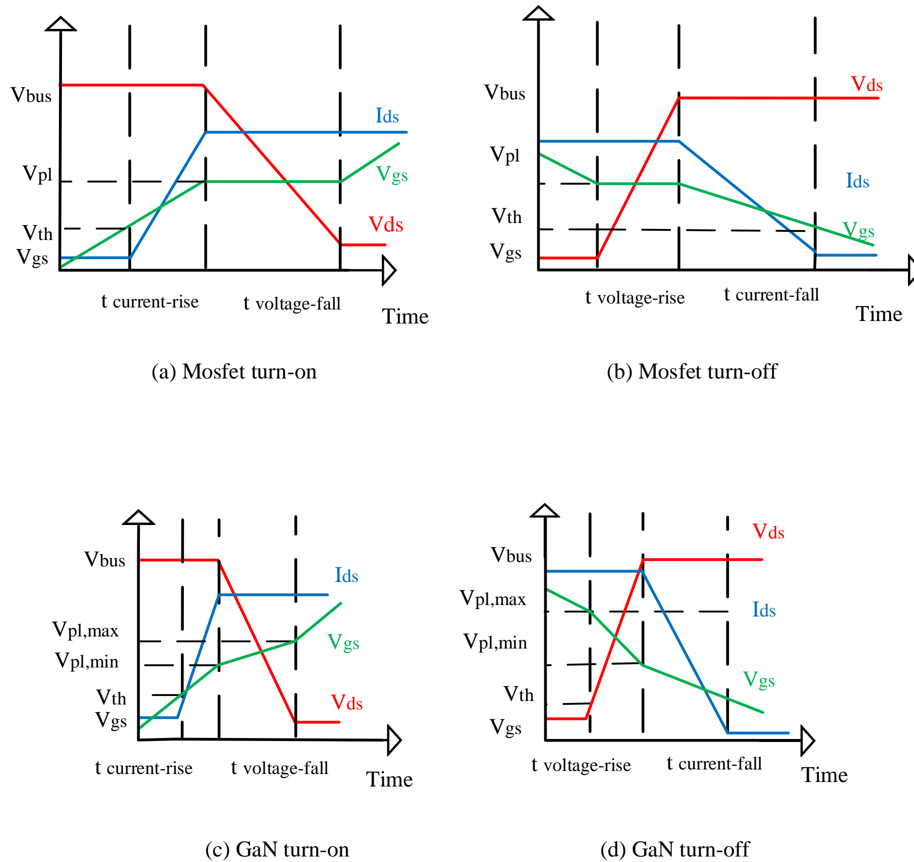


Fig. 4.1. Comparison of typical hard-switching waveforms for Si and GaN devices

In [28] an analytical model for 12-3.3V buck regulators has been proposed where the turn-on losses relate to gate resistance and voltage only. In [77], for a 48-5V buck regulator, an analytical model has been suggested which has low accuracy at higher voltages. Similarly, in [78] for a 12-

3.3V buck regulator an analytical model considering the non-linearity of capacitances has been suggested consisting of seven different stages of switching processes. All these previously derived models are applicable for low voltage applications with limited accuracy and at higher voltages their accuracy reduces due to the non-linearity of internal capacitances.

This work proposes a model with good accuracy over a wide voltage range (100-400V) as it considers the effect of variation in different gate drive and power circuit parameters on hard-switching losses. There is no earlier work which suggests a switching loss model for high voltage GaN devices, where the model can be simply applied with changing gate drive parameters which is the main focus of this paper.

Therefore, the main contributions of this work are:

1. The derivation of a hard-switching loss model for high voltage GaN devices up to 400V and 1kW of power with variation in several gate drive and power circuit parameters which is being compared over a wide experimental operating range, and has not been covered to date in prior research. The novelty of this work lies in extending the previous works to a hard-switching model which can be used simply and directly with minimum computation.
2. An analysis of switching losses with variation of gate resistance and negative gate bias voltage using the proposed model, which has also not been previously covered.
3. An in-depth experimental investigation of converter efficiency with changing gate drive parameters.

The next section, Section 4.3 discusses the fundamental aspects and basis of the model and explains the proposed model in detail with derived equations for turn-on and turn-off transients. Section 4.4, describes a comparison with prior works. Further, Section 4.5 presents the

experimental results and a comparison with other earlier models to clearly show the accuracy and superiority of the proposed model over a wide range. Finally, Section 4.6 summarizes this work.

4.3 Proposed Model

The half-bridge synchronous boost GaN topology as shown in Fig. 4.2 has been taken under consideration for switching transition analysis. GaN devices have very high dv/dt rates and related voltage oscillations during switching transients, which is due to the very small internal capacitances [10,41,43,79,80] while for conventional Si devices the internal capacitances are comparatively high. Also, due to the non-linear relationship of C-V at higher voltages there is a considerate change in the internal capacitances. Using data extraction software, Fig. 4.3 has been drawn which shows the non-linear relationship of internal capacitances with the device drain to source voltage and the corresponding values have been used for the analysis.

This section highlights equations and analysis of the turn-on and turn-off transients overlap period of current and voltage transitions in detail. As shown in Fig. 4.1 the hard-switching loss belongs to the transition period which is the rise and fall of both voltage and current. Therefore, switching losses are simply the summation of losses during voltage and current transitions occurring during both turn-on and off and can be expressed by using the equation below:

$$P_{sw} = P_{vt} + P_{ct} = \frac{1}{2} V_{dc} I_L (t_r + t_f) f_{sw} \tag{1}$$

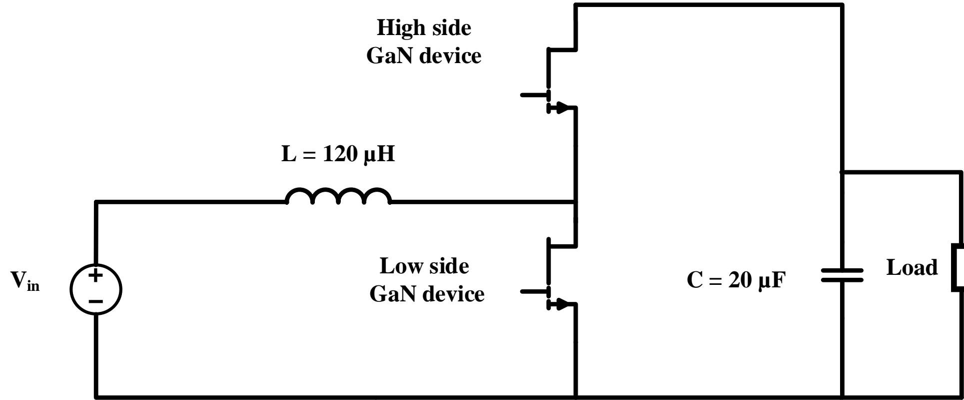


Fig. 4.2. Half bridge boost converter test circuit

Where P_{vt}, P_{ct} are voltage and current transition power losses, V_{dc} is the input voltage, I_L is inductor current, f_{sw} is the switching frequency, and t_r and t_f are the voltage and current rise and fall times during the turn-on and turn-off transient.

Ideally the gate charge plays a key role in the different stages of the switching process and for any of the internal capacitances it is given by

$$\frac{dQ}{dt} = I = C\frac{dV}{dt} \tag{2}$$

Also, variation in negative biases and gate resistances changes the slew rate dv/dt and thus affects the converter performance in terms of losses and efficiency. The proposed model tries to relate the t_r and t_f to charge for simplicity of the computation by using:

$$t = \frac{Q}{I} \tag{3}$$

Similarly, Miller charge (Q_{gd}), which is the amount of charge needed to change the drain to source voltage from the blocking state (almost negligible dead time zone) to near zero value, decides the slew rate by (4) [41], [43].

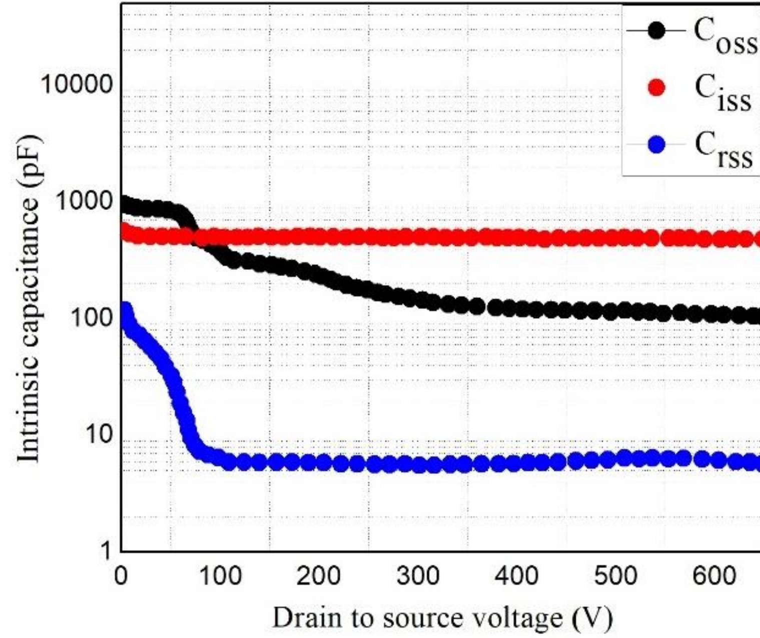


Fig. 4.3. Non-linear capacitance obtained by data acquisition software [27]

$$Q_{gd} = \int_{0}^{V_{dc}} C_{rss} V_{ds} dV_{ds} \quad (4)$$

Equation (4) also represents the relationship between the internal capacitance and drain to source voltage. Other than P_{ct}, P_{vt} is dependent on Q_{gd} because the voltage rise and fall depends the charge and thus gives:

$$P_{vt} = \frac{1}{2} V_{dc} I_L t_{vf} f_{sw} \quad (5)$$

$$t_{vf} = \frac{Q_{gd}}{I_g} \quad (6)$$

$$Q_{gd} = C_{gd} V_{gd} \quad (7)$$

Where $C_{gd} = C_{rss}$ (reverses transfer capacitance) which is also referred to as Miller capacitance in device datasheets.

$$t_{vf} = \frac{C_{gd} V_{gd}}{I_g} \tag{8}$$

By the principle of conservation of energy at the gate drain terminal using KVL,

$$V_{gs} = V_{gd} + V_{ds} \tag{9}$$

$$t_{vf} = \frac{C_{rss}(V_{gs} - V_{ds})}{I_g} \tag{10}$$

Combining (5) – (10) gives,

$$P_{vt} = \frac{1}{2} V_{dc} I_L f_{sw} \frac{C_{rss}(V_{gs} - V_{ds})}{I_g} \tag{11}$$

During the whole turn-on transition, the drain to source voltage has to vary from the applied DC value to zero. If it is assumed that during this transition, the driver voltage and plateau voltage can be best estimated as a constant as there is very variation in both of them therefore the average value of the gate current can be formulated as:

$$I_{g,on} = \frac{V_{driver} - V_{pl}}{R_{g,on}} \tag{12}$$

Where $R_{g,on}$ is the gate turn-on resistance. The proposed estimation is better in the sense that different gate resistance values can be used in this model for turn-on and turn-off which is usually practised by gate drive design engineers.

Similarly, during the turn-off transition, (13) can be used. Also, in the previously published models, no negative bias is considered during turn-off, i.e., $V_{gs,off}$ = 0V. However, this model relates switching losses to plateau voltage so that bipolar PWM can be used in the proposed model as well. Although gate plateau voltage depends on the gate to drain charge in the case of Si MOSFETs, it is a constant value; however, in GaN devices, plateau voltage varies linearly.

$$I_{g,off} = \frac{V_{driver} - V_{pl}}{R_{g,off}} \tag{13}$$

Since GaN devices are driven in the same manner as other power devices, the current transition can be estimated in this model like the voltage transition, and is dependent on gate charge as well. During this transition, charge is being accumulated and has being modeled in a range by different works but more precisely can be expressed as,

$$Q_{gs,avg} = \int_{initial}^{final} \frac{Q_{gs,range}}{V_{pl}} dV_{pl} \tag{14}$$

Similar to how the voltage transition is expressed in (4) – (11), the current transition can be expressed as,

$$P_{ct} = \frac{1}{2} V_{dc} I_L t_{cr} f_{sw} \tag{15}$$

$$t_{cr} = \frac{Q_{gs,avg}}{I_g} \tag{16}$$

$$Q_{gs,avg} = C_{gs} V_{gs} \tag{17}$$

$$C_{gs} = C_{iss} - C_{rss} \tag{18}$$

Where C_{iss} is the input capacitance and C_{rss} is the reverse transfer capacitance, and the value corresponding to each operating drain to source voltage can be accurately estimated by using Fig. 4.3.

$$t_{cr} = \frac{C_{gs}V_{gs}}{I_g} = \frac{C_{iss} - C_{rss}}{I_g} \tag{19}$$

Combining (14) – (19) gives the power loss during current transition as,

$$P_{ct} = \frac{1}{2}V_{dc}I_L f_{sw}\left(\frac{C_{iss} - C_{rss}}{I_g}\right) \tag{20}$$

The value of the gate current as included in the above equations contributes to the power loss. Therefore, current into the gate terminal affects both the voltage and current transitions. An increase in the gate current will reduce the transition time which is why the proposed model is useful with different gate drive circuits, i.e., it can be used with both voltage or current based drivers.

Typical datasheets of different power devices can be difficult to use as they provide information for only one switching condition and the plateau region is not well defined. In this model, it assumed on the basis of average over the time scale which leads to the point that the gate current during the turn-on and turn-off can be accurately expressed as:

$$I_{g,on} = \frac{V_{driver} - \left(\frac{V_{pl} + V_{th}}{2}\right)}{R_{g,on}} \tag{21}$$

$$I_{g,off} = \frac{V_{driver} - \frac{V_{pl}}{2}}{R_{g,off}} \tag{22}$$

Thus, total device loss during the overlapping for both during turn-on and turn-off can be expressed as

$$P_{sw} = P_{vt,on} + P_{ct,on} + P_{vt,off} + P_{ct,off} = P_{on} + P_{off} \tag{23}$$

By combining the equations above the loss during the turn-on and turn-off can be separately written as:

$$P_{on} = \frac{1}{2} V_{dc} I_L f_{sw} R_{g,on} [\frac{C_{rss}(V_{gs} - V_{ds})}{(V_{driver} - V_{pl})} + \frac{(C_{iss} - C_{rss}) V_{gs}}{V_{driver} - (\frac{V_{pl} + V_{th}}{2})}] \tag{24}$$

$$P_{off} = \frac{1}{2} V_{dc} I_L f_{sw} R_{g,off} [\frac{C_{rss}(V_{gs} - V_{ds})}{(V_{driver} - V_{pl})} + \frac{(C_{iss} - C_{rss}) V_{gs}}{V_{driver} - \frac{V_{pl}}{2}}] \tag{25}$$

Equations (24) and (25) can be used to calculate switching losses in many different operating conditions. The terms inside the brackets relate to the device whereas the terms outside the bracket relates to power converter operating conditions.

4.4 Comparison with Previous Works

This section reviews previous similar models in order to clarify the comparison with the model presented in this paper. This will show the contribution of the proposed model. Table 4.1 presents this comparison based on some of the critical parameters.

Table 4.1. Comparison with Previous Models

Parameter	Ref [76]	Ref [28]	Ref [78]	This work
Simple computation	Yes	No	No	Yes
Accuracy over 100-400V	No	No	No	Yes
Gate resistance	Yes	Yes	Yes	Yes
Gate bias	No	No	No	Yes
Gate inductance	No	No	No	No
Circuit modeling	Yes	Yes	Yes	Yes
Intrinsic capacitances	No	Yes	Yes	Yes

Moreover, the proposed model and other prior models are derived based on the basic GaN-HEMT structure as shown in Fig. 4.4 showing the relation of different intrinsic capacitances. One of the simplest models for GaN switching losses in [16] has the equation for voltage and current transition losses as

$$P_{tvx} = \frac{1}{2}\frac{V_{ds} I_{ds} Q_{gd}}{I_g} \tag{26}$$

$$P_{tcx} = \frac{1}{2}\frac{V_{ds} I_{ds} Q_{gs2}}{I_g} \tag{27}$$

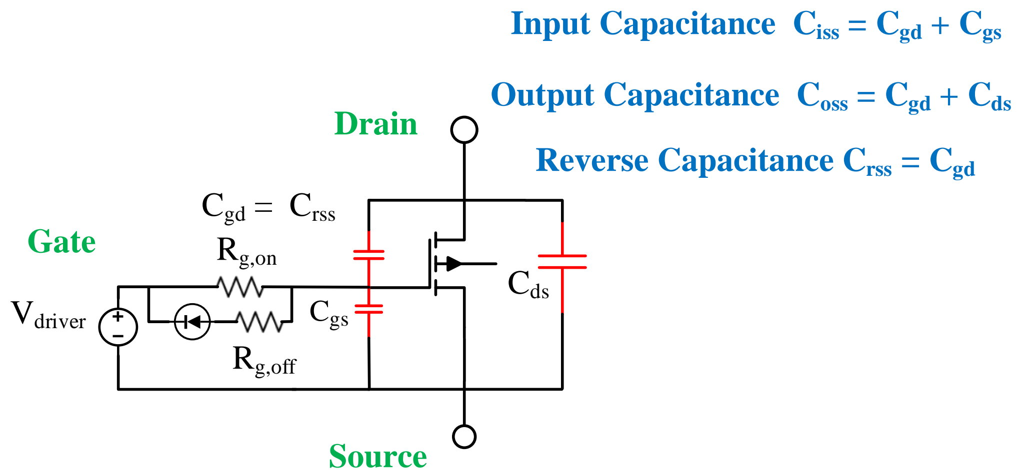


Fig. 4.4. GaN-HEMT structure with intrinsic capacitances

Where P_{tvx} and P_{tcx} are voltage and current transition losses during switching. Q_{gd} and Q_{gs2} are gate to drain charge and the charge needed to increase gate voltage to the plateau voltage. These parameters play a crucial role during switching transition. The equations above show the dependency of switching losses on gate circuit parameters but to calculate the losses with different gate bias and resistances has not been modeled. Moreover, with different values of $R_{g,on}$ and $R_{g,off}$, the value of I_g changes. In [28] an analytical model for 12-3.3V buck converter switching losses with a complexity of four different stages has the equation

$$P_{sw} = \int_{t_0}^{t_4} V_{in} I_{ds} dt \tag{28}$$

The above equation is further extended into four different stages from t_0 - t_4 and each stage has various exponential and trigonometric terms which although improves accuracy at low voltages, also adds computational complexity.

In [77] similarly for a 48-5V buck converter an analytical model with two different stages which is inaccurate as per Fig. 1 has the equation for each stage as

$$P_{sw} = \frac{1}{2} V_{ds} I_L t_r f_{sw} \tag{29}$$

But with the complex expression for rise time as

$$t_r = \Delta V_{gs}(L_s g_{fs} + R_g C_{iss}) + \sqrt{\frac{\Delta V_{gs}(L_s g_{fs} + R_g C_{iss})^2 + 4\Delta V_{gs}(V_{dd} - V_{gsr}) R_g L_{loop} g_{fs}}{2V_{gsr}}} \tag{30}$$

Where V_{gsr} is the rise in gate voltage, L_{loop} is loop inductance, g_{fs} are transconductance and C_{iss} is device input capacitance. The square root term in the above equation restricts the range of different

gate drive parameters with which it can be used. Also, in [78] an analytical model with seven different stages and different equations at each stage has been proposed. It considers the intrinsic capacitances and parasitic inductance which further increase complexity compared to the models discussed above.

Based on the shortcomings of previous models this work presents a model which is simple in computation with minimum parameters, has high accuracy over 100-400V range and is better for high voltage devices unlike prior models, and shows the dependence on different gate circuit parameters, where switching losses can be calculated with changing gate resistance and gate bias.

Furthermore, this work also shows the effect on converter overall efficiency with the variation in different parameters by means of wide experiments as well the change in switching losses. This is important in the sense that hard-switching losses are the dominant among other type of losses associated with the switching process. Overall, the contribution of the proposed model will help design engineers to easily compute even with the variation in different gate drive and power circuit parameters.

4.5 Experimental Results and Discussion

The experimental circuit is a synchronous boost converter, as shown in Fig. 4.2 earlier. Two CWS high frequency power inductors of 60µH each are used in series along with a 20 µF output capacitor. Table 4.2 summarizes the experimental setup parameters. Fig. 4.5 shows the experimental set up and Fig. 4.6 shows the measurement set up involving different probes.

As shown in Fig. 4.5, the experimental setup includes a Sorensen SGX programmable DC power supply, Chroma 63804 programmable AC/DC electronic load, Tektronix AFG1022 programmable function generator, and Tektronix MSO54 4-channel 500MHz mixed signal oscilloscope. The circuit uses GaN Systems' GS665MB-EVB evaluation board [64] with GS66516T 650V/60A rated devices and ACPL-346 gate drivers. The devices use ultra-low inductance packaging and a dedicated source sense connection is used on the PCB to minimize the gate loop inductance. This helps in the sense that the affect due to loop and parasitic can be neglected especially at high voltages.

Table 4.2. Experimental setup parameters

Parameter	**Value**
DC input voltage	50-200V
DC load output	100-400V
Switching frequency	50 kHz
Duty cycle	50%
Power inductor	2 × 60 μH
Input/output capacitor	20 μF
Gate turn-on resistance	10, 12.5 Ω
Gate turn-off resistance	2 Ω
Negative bias	-4.4, -5.0 V

As shown in Fig. 4.6 the high-side and low side switch V_{gs} are measured with TMDP0200 differential probes with 200 MHz bandwidth. The low-side V_{ds} is measured with the ISoVu probe (on tripod) having bandwidth up to 800 MHz (tripod) and the low-side switch current is measured using SDN-414 current shunt having 2Ghz bandwidth shown in Fig. 4.6. The gate drive circuit involves different stages like the bipolar gate drive signal is generated using a 5-11V DC/DC converter having a dc rail that is split into positive and negative terminals. This helps in providing isolation and thus generating a safer way to generate the bipolar pulse width modulation signal for gate drive. The positive terminal is set by a Zener regulator circuit which has an RC divider branch

coupled to it. The output of the DC/DC converter is fed into the isolated ACPL-P346 gate driver which drives the high and low eGaN-HEMTs separately. A Zener regulator provides a particular bipolar PWM signal so that two different bipolar PWM signals +6.2/-4.4V and +5.6/-5V can be generated. This is important that two different negative biases can be easily applied

Fig. 4.7 (a) shows the circuit waveforms at 400V, 1kW operation with $R_{g,on} = 10\Omega$ and $V_{gs,off} = -5V$. Fig. 4.7 (b) and (c) shows V_{ds} turn-on and turn-off respectively. It is also important to notice that prior studies [22-25] have suggested that the slew rate of V_{ds} varies considerably even with a slight variation in gate resistance and gate bias which affects the hard-switching losses.

The switching losses are calculated for the hard-switched low side device in the half bridge boost converter as shown in Fig. 4.3 earlier. The boost converter is operated from 100-400V at 50kHz switching frequency and up to 1kW of output power. There are a total of 16 operating points in experiments being compared by varying voltages = 100-400V, $R_{g,on} = 10/12.5\Omega$ and $V_{gs,off} = -4.4/-5V$. The values of the internal capacitances at respective V_{ds} are taken from the C-V curve as shown in Fig. 4.4 earlier. $V_{pl} = 3V$ and $V_{th}=1.7V$ values are taken from the datasheet [27]. V_{driver} is a bipolar signal with values +6.2/-4.4V and +5.6/-5V. Gate turn-on and off resistances are $R_{g,on} = 10/12.5\Omega$ and $R_{g,off} = 2\Omega$.

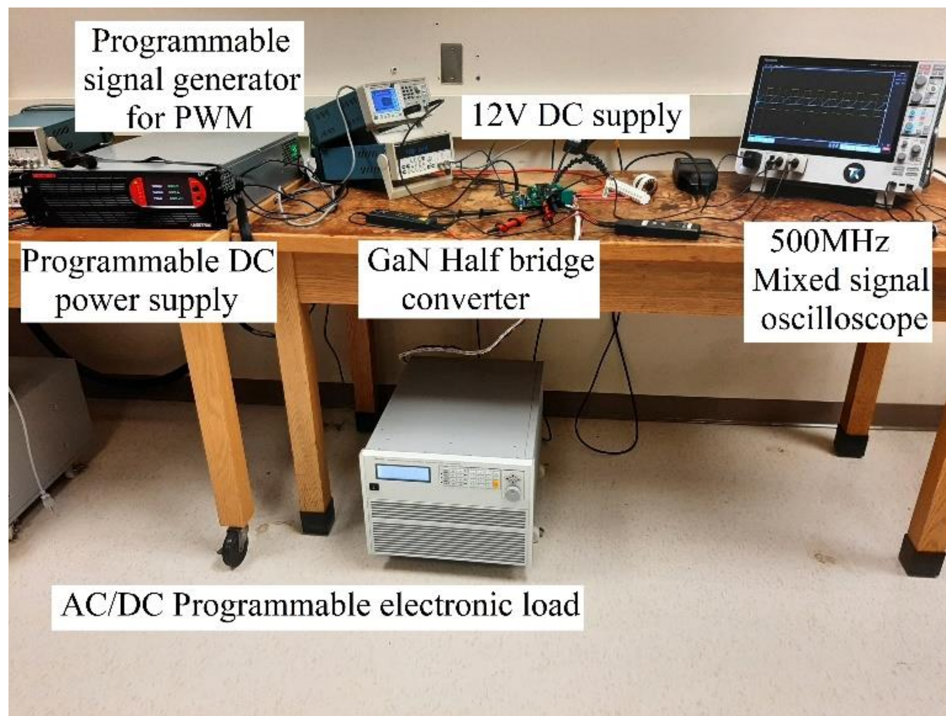


Fig. 4.5. Experimental setup

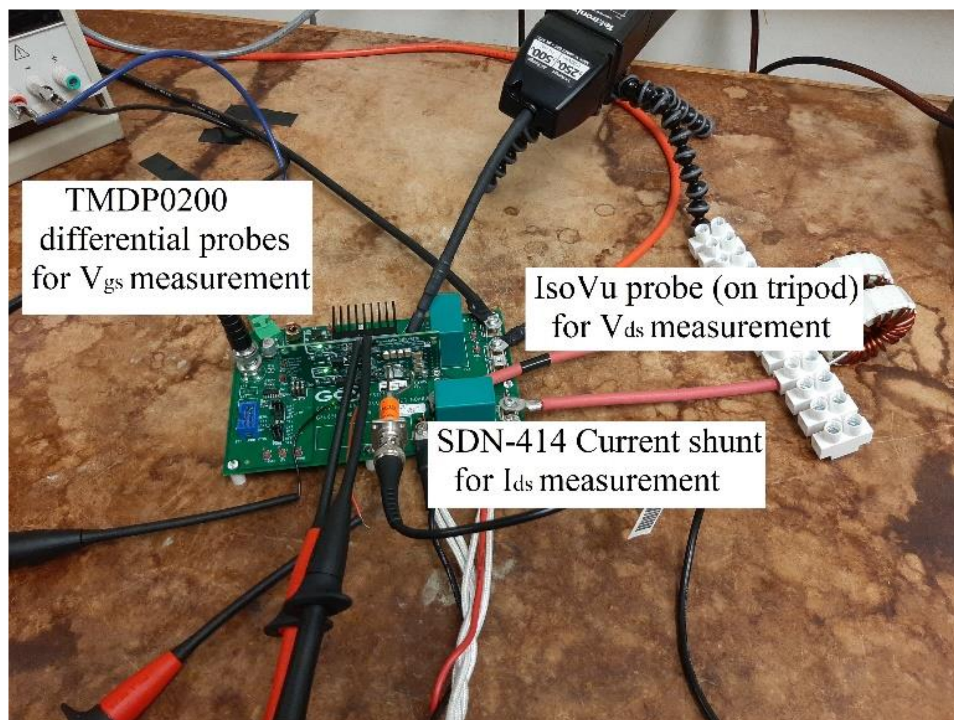
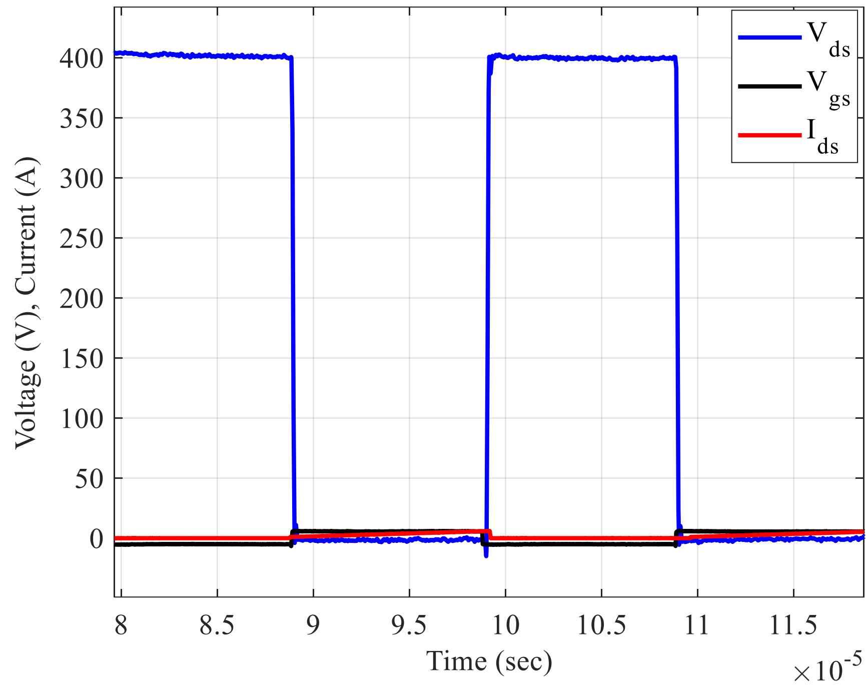
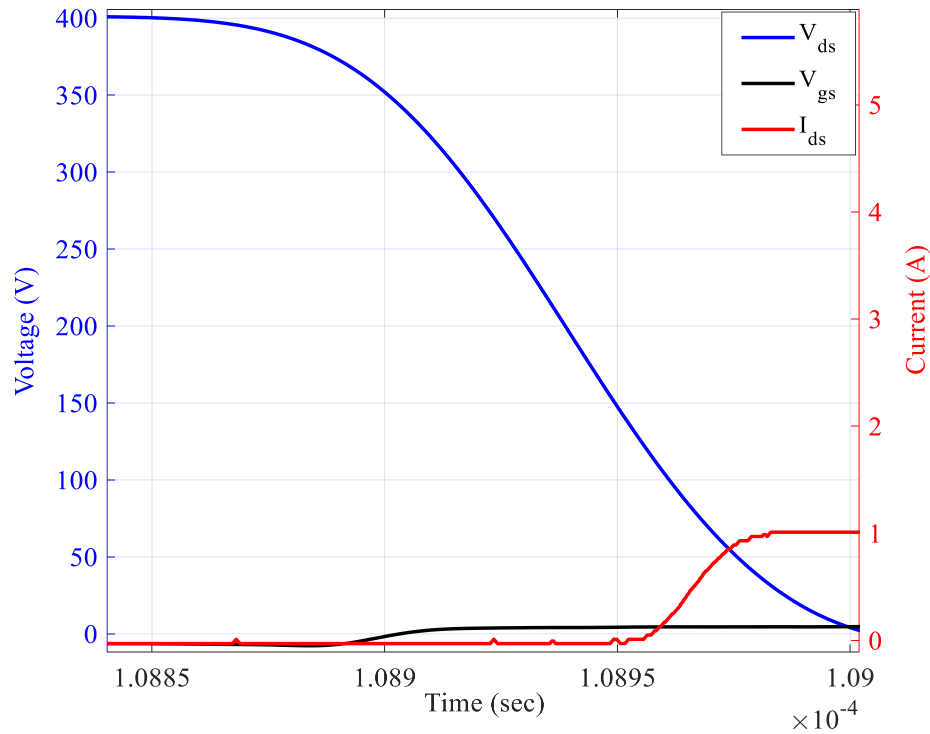


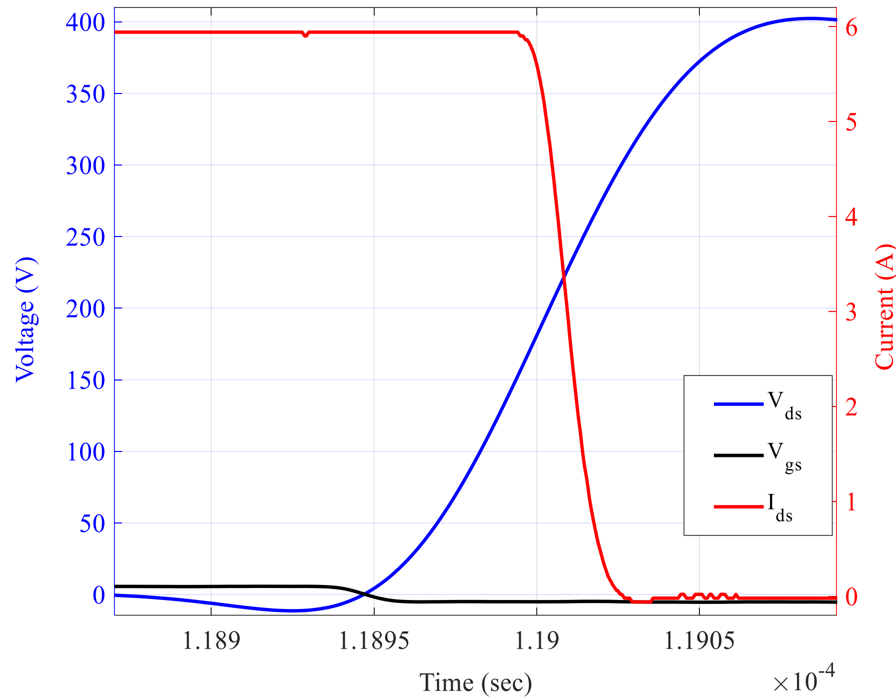
Fig. 4.6. Measurement setup



(a)



(b)



(c)

Fig. 4.7. Circuit waveforms (b) turn-on and (c) turn-off at 400V,1kW operation with Rg,on = 10Ω , Vgs,off = -5V

Table. 4.3 quantifies the error % at different voltages for Models A, B and the proposed model. For each voltage (100-400V) average error of all the four combinations has been calculated and the rightmost column presents the mean over the entire range for the respective models as shown in Table. 4.3.

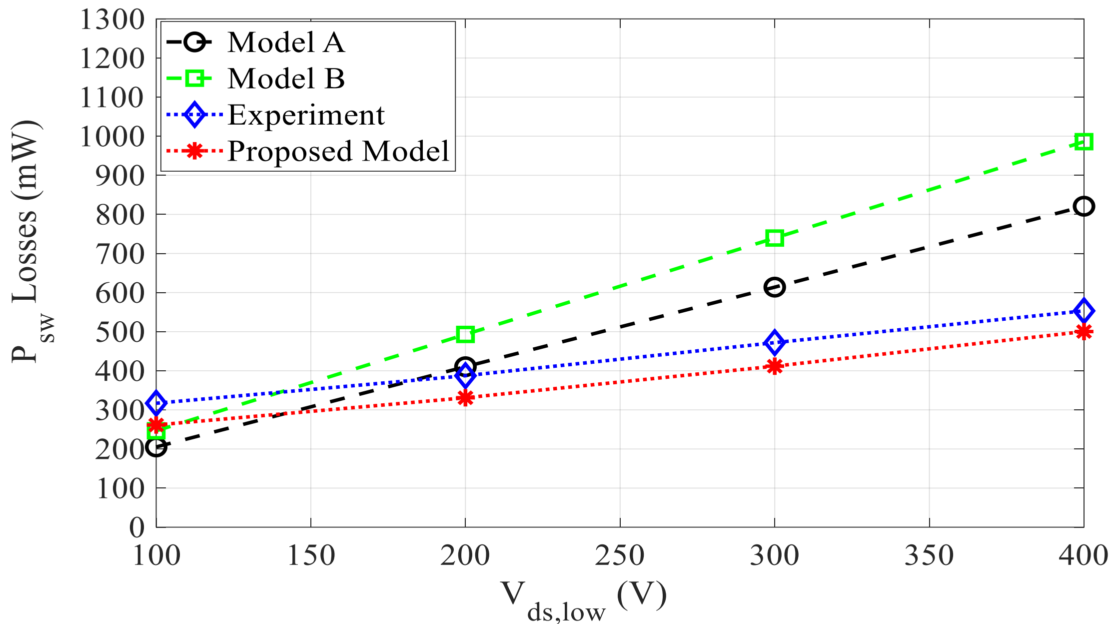
Compared to model A and B which has a mean error of 38.62% and 45.44% the proposed model has a low error of 15.29% over the entire range. Models A and B has a large error at higher voltages as they are only suitable for low voltages. The proposed model has a better accuracy because the derived equations allows it to use with different gate biases.

Table 4.3. Comparison of Models in % Mean Error

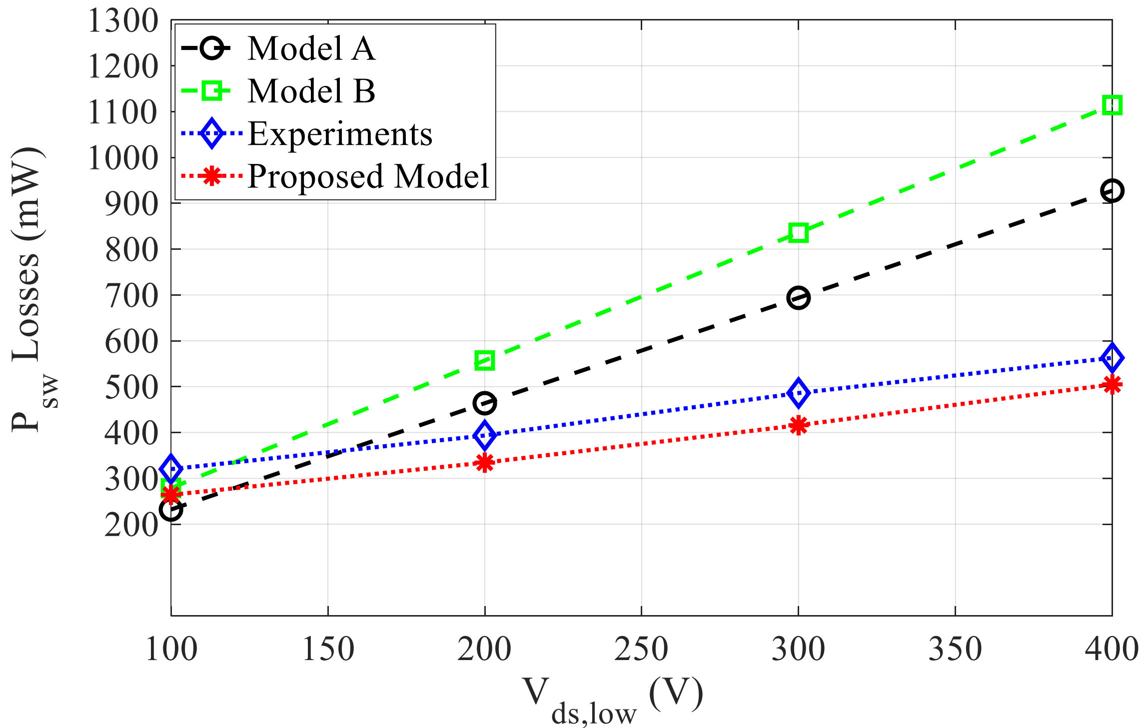
Models	**100V**	**200V**	**300V**	**400V**	**Mean error**
Model A	17.69%	34.26%	43.74%	58.79%	38.62%
Model B	22.39%	41.25%	48.94%	69.20%	45.44%
Proposed	11.68%	14.74%	15.63%	19.11%	15.29%

Fig. 4.8 shows the comparison of the calculated switching losses from the proposed model with those of related prior works and experiments for all four cases of gate drive parameters i.e with $R_{g,on}$ = 10/12.5Ω , $V_{gs,off}$ = -4.4/-5V. Model A and B in Fig. 4.8 corresponds to [28] and [76] respectively. The proposed model has been compared over 100 – 400 V with these models and experiments. Fig. 4.8 (a) and (b) compares the proposed model at $R_{g,on}$ = 10Ω, $V_{gs,off}$ = -4.4/-5V. Similarly, Fig. 4.8 (c) and (d) compares the proposed model at $R_{g,on}$ = 12.5Ω , $V_{gs,off}$ = -4.4/-5V and shows the same trend. This study shows that the hard-switching losses varies considerably with the changing gate drive parameters which makes it important to notify its relative impact on the converter overall efficiency.

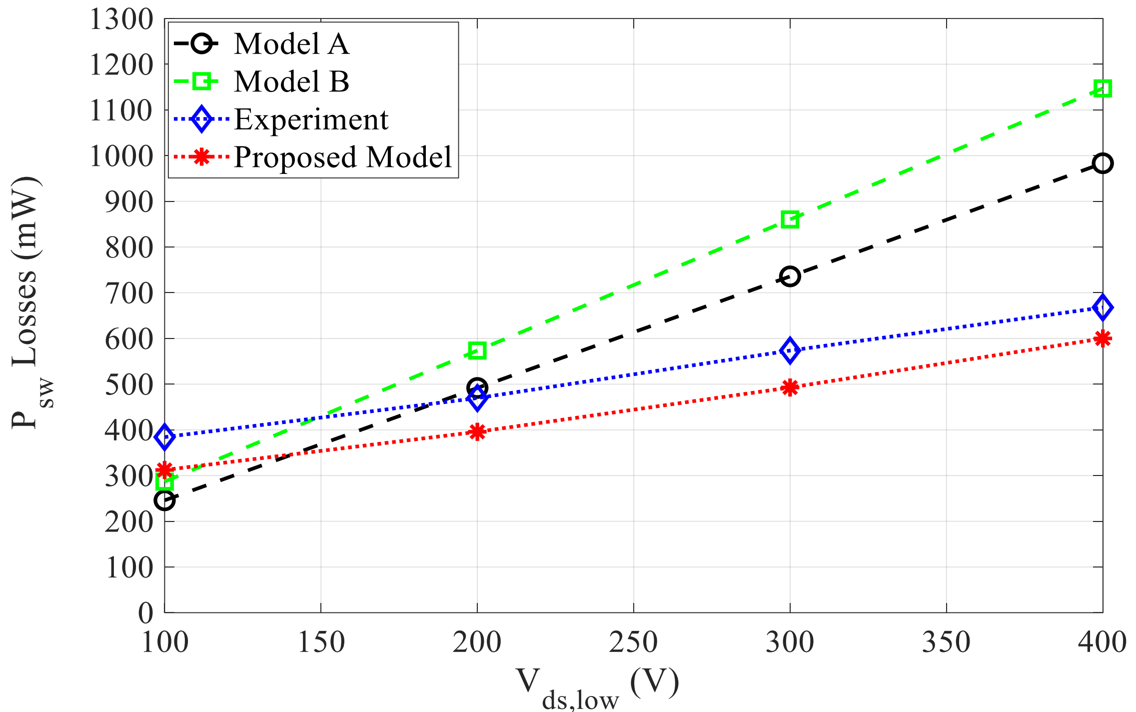
Fig. 4.9 shows the boost converter overall efficiency with the changing gate drive parameters and clearly shows that even a slight variation in gate drive parameters affects the converter overall efficiency. To, summarize and relate the hard-switching losses at the same operating point to the boost converter overall efficiency each of the Fig. 4.8 (a), (b), (c) and (d) relates to each of the four lines in Fig. 4.9.



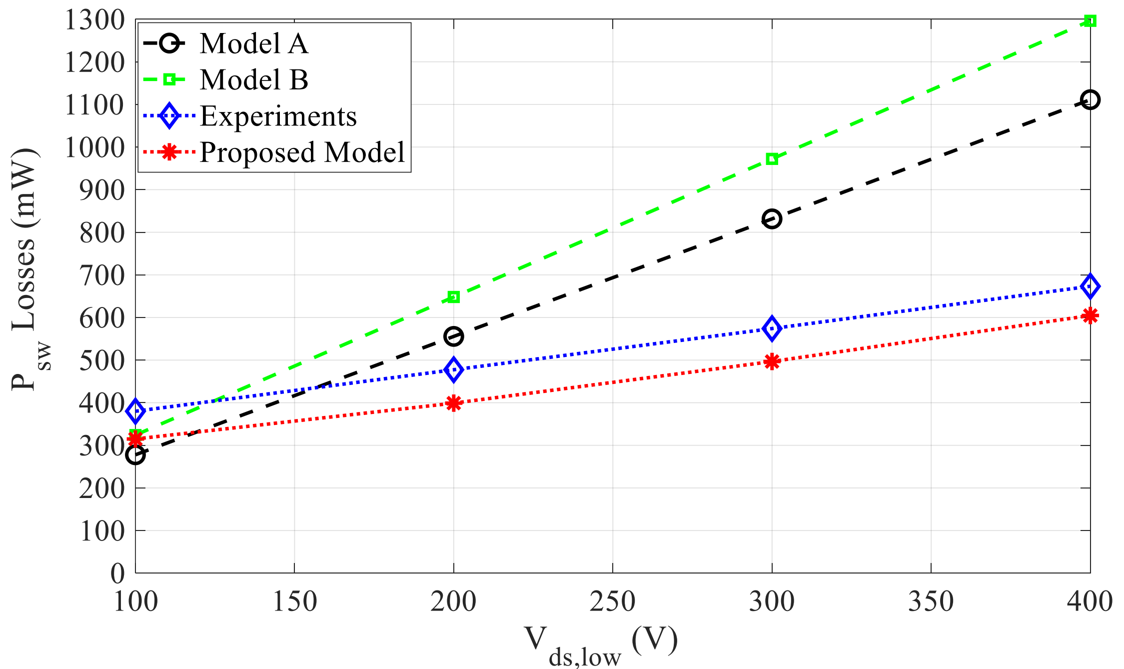
(a) $R_{g,on} = 10\Omega$, $V_{gs,off}$= -4.4V



(b) $R_{g,on} = 10\Omega$, $V_{gs,off}$= -5V



(c) $R_{g,on} = 12.5\Omega$, $V_{gs,off} = -4.4V$



(d) $R_{g,on} = 12.5\Omega$, $V_{gs,off} = -5V$

Fig. 4.8. Comparison of proposed model for calculating switching losses

Power devices needs to have low dynamic losses to drive high frequency in a hard-switched converter. Moreover, among these dynamic losses hard-switching losses is the most dominant one. This is the reason why converter overall efficiency needs to be investigated as well.

This is important in the sense that an accurate estimation of dominant hard-switching losses with the changing gate drive parameters especially with different negative biases allows power electronics design engineers to analyze converter dynamics so that improvements can be made significantly.

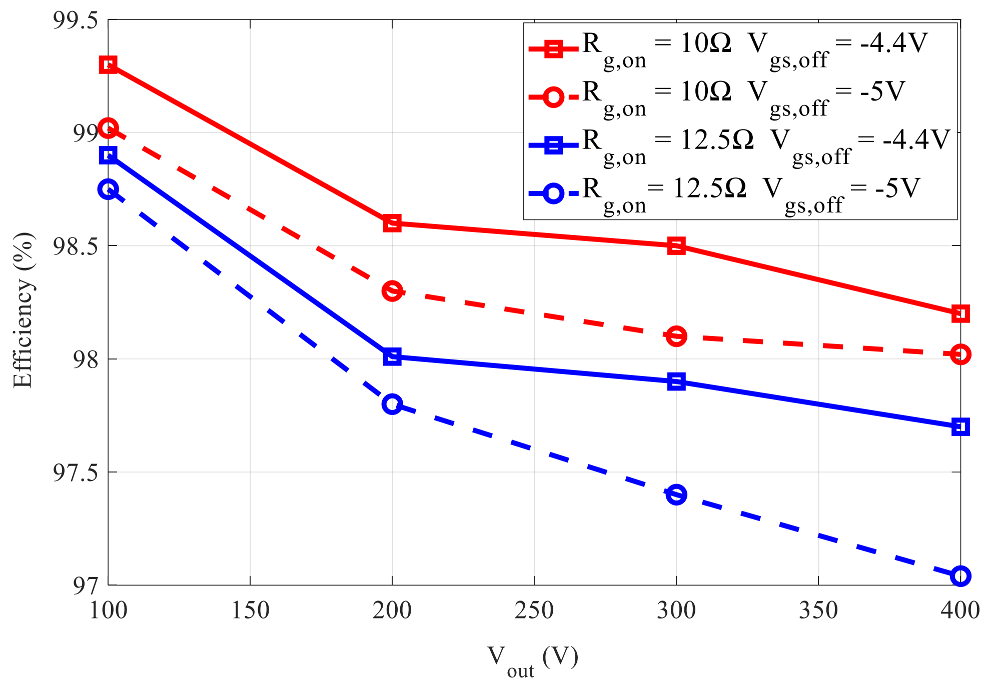


Fig. 4.9. Converter efficiency at different operating points

4.6 Summary

This work has proposed a simple and accurate model with minimum computation for estimation of hard-switching losses for high voltage GaN devices over a wide voltage range which has not been suggested in prior works. The derived equations present a mechanism to simply analyze the switching transition and their dependence on different parameters. The proposed model has been compared with closely related research with extensive experimental results 100-400V and up to 1kW and with variation in different gate drive parameters.

Most importantly, this work with the help of derived equations shows the dependence on different gate circuit parameters on switching losses and has been calculated with variation in both gate resistance and gate bias (i.e with different negative gate biases during turn-off) which has not been covered in previous research works.

In hard-switched converters switching transitions leads to significant losses and the main metrics affecting converters performance is its efficiency which is why this work also shows the effect on converter overall efficiency with the variation in different parameters by means of extensive experiments along with the estimation of hard-switching losses.

Chapter 5: A New Quantification and Analysis of Parasitic Inductances for Surface Mounted GaN Devices

5.1 Overview

Device manufactures sometimes don't provide information about inductances of the device and also the PCB inductance is unknown both of them are the main cause for ringing in high frequency GaN power converters. There are practical challenges to accurately measure these parasitic inductances because of their low value, shared common source inductance between gate and power circuit, and need of special instruments like network analyzers or time-domain reflectometry (TDR) techniques. The main contribution of this work is to suggest 1.) a new measurement method with a novel theoretical approach involving DC and AC equivalent circuit presented with the help of two port Z-parameter model. 2). The proposed method can be applied to surface mounted devices using simple laboratory instruments like a small DC power supply, function generator, and voltage and current probes without the use of vector network analyzer (VNA) or network analyzer etc. The experimental results have been included to support the proposed hypothesis.

5.2 Introduction

Wide bandgap devices like GaN/SiC have low losses and the capability of attaining very high switching frequencies, which makes them excellent options for power converters with high efficiency and high-power density. Unfortunately, the inductance in the device package and on the PCB board can cause stability problems. However, along with the benefits of GaN mentioned earlier there are serious reliability issues of GaN power converters due to voltage overshoots during turn-off which increases switching losses and causes a short across the two switches in bridgeless topologies [7], [10], [14], [45].

The main contributor to voltage overshoots is parasitic inductances [10], [84] most precisely the gate, drain and common source inductance (which is shared between gate and power circuit) shown in Fig. 5.1. Since the parasitic inductance affects the performance, an accurate and simple measurement is required. There are practical problems in measuring these inductances 1) due to their smaller value compared to power inductance, 2) because of the hidden wiring path, and 3) due to the requirement of instruments like network or impedance analyzers, TDR techniques etc.

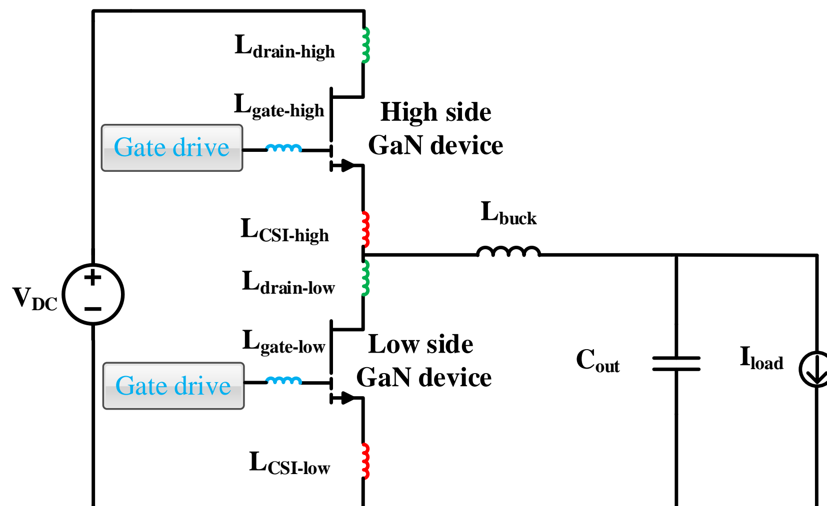


Fig. 5.1. Parasitic inductances in half bridge GaN converters

Moreover, time-domain reflectometry (TDR) has been suggested to be a technique in measuring inductances by employing a complicated LC ladder network [85]-[87] but in in measuring parasitic inductances which cannot be assumed as a lumped inductance TDR will be inaccurate.

In [88] – [90] a measurement method has been suggested to measure only the common source inductance. But in the case of high frequency power converters all the three parasitic inductances i.e, gate, drain and common source inductances are important as they are the main reasons behind frequent false turn-on events [1], [6], [16], [68]. Also, other parasitic inductances like drain inductance and gate inductance are comparatively lower in GaN than Si MOSFETs. Firstly, the common source inductance contributes to false turn-on in all topologies [1], [2], [5], [10], [14], [68]. Secondly, the gate inductance contributes to false turn-on in high frequency converters especially with isolated gate drivers [7], [10], [45], [81]. Thirdly, the drain inductance contributes to false turn-on especially in half bridge circuits where both high and low side devices are in series [7], [10], [14], [45].

The models suggested in earlier works [7], [10], [14], [45], [81] includes all the three parasitic inductances for analyzing false turn-on events. In [91] an analysis relating the probe input impedance has been presented to show the significance of the error occurring at very high frequencies for measuring inductances which is why this paper accommodates experiments within a considerable frequency range 50-350kHz for better accuracy in comparison to prior works.

Moreover, finite element analysis or simulation-based studies have complexity. A simulation model has been suggested in [92] for estimating the common source inductance of cascode GaN devices. But it is inappropriate in the sense that simulation needs information regarding wiring of the molded device package. This restricts the accuracy of simulation-based models and finite element method as this physical wiring information is absent in datasheets [64,93].

Thus, there is a need to suggest a new measurement principle using simple laboratory equipment for measuring the parasitic inductances (not mentioned in datasheets) responsible for instabilities like false turn-on. The proposed approach with the help of Z-parameter model (Fig. 5.2) involving both AC and DC circuit equivalent presents such an accurate measurement method.

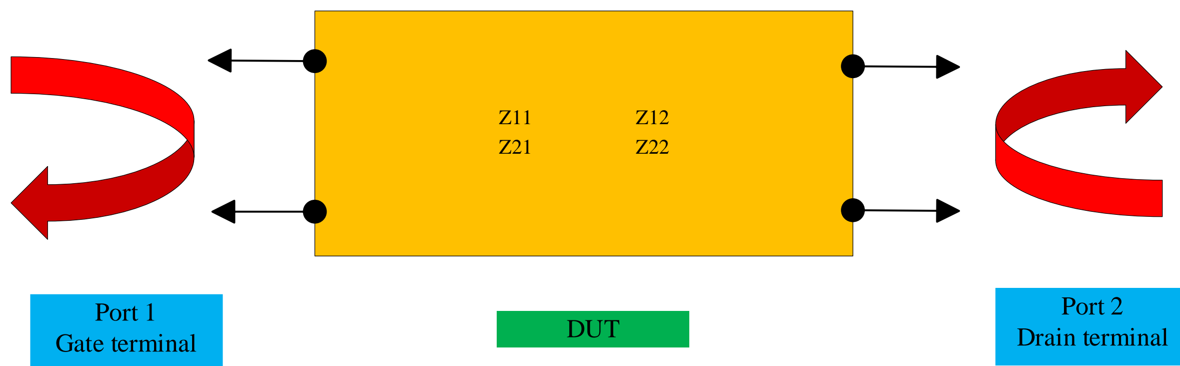


Fig. 5.2. Z-parameter model

Table 5.1 present a comparison of this work in relation to previous works. The effect due to the traces in the PCB also contributes to the parasitic inductance which is not possible with these earlier methods. To conclude there are certain difficulties and limitations associated with these methods.

Firstly, impedance or network analyzers needs source chip to be connected to the instrument. Secondly, TDR method with the assumption that wiring path to be tested is equivalent to an LC circuit doesn't consider the effect of resistances involved and this will affect the accuracy. Thirdly, in resonance methods there is a requirement to form a close loop for accuracy which makes it experimentally complex.

The main issue arising from these parasitic inductances are voltage overshoots during switching. In [82], [83] dependence of the common source inductance has been analyzed in this regard. The

detrimental effects of these inductances in relation to power converter performance has been discussed in detail in [46], [94] – [96].

Table 5.1. Comparison with Previous Work

Parameter	**[17]**	**[21]**	**This work**
AC & DC equivalents	No	No	Yes
Common source inductance	Yes	Yes	Yes
Drain inductance	No	No	Yes
Gate inductance	No	No	Yes
Intrinsic Capacitances	Yes	Yes	Yes
Gate internal resistance	No	No	Yes
Gate turn-on resistance	Yes	Yes	Yes
Gate turn-off resistance	No	No	Yes
Small signal stability	No	No	Yes

To summarize, there is no prior work measuring all these parasitic inductances with a straightforward approach and having better accuracy by using simple laboratory equipment. Therefore, the main contribution of this work can be summarized as:

1. In suggesting a new measurement principle to measure parasitic inductances (L_{CSI}, L_{drain}, L_{gate}) not mentioned by manufacturers with the help of simple laboratory instruments like signal generator, auxiliary DC supply, voltage and current probes.
2. The proposed method can be implemented with help of an experiment set up based on a simple AC and DC equivalent circuit which is theoretically presented with the help of Z-parameter model and is applicable to both surface mounted or through hole devices.

Therefore, Section 5.3 highlights the measurement principle with equations and the procedure for extraction of parasitic inductances. Section 5.4 presents simulation results and Section 5.5 focuses

on the experimental set up and results for measuring parasitic inductances. Finally, Section 5.6 summarizes this chapter.

5.3 Proposed Methodology for Quantification of Parasitic Inductances

The proposed method by means of hybrid approach analyzing AC and DC equivalent model presents a new methodology for quantification of common source inductance by using simple laboratory instruments. Fig. 5.3 shows the circuit of the proposed method including all possible parasitic elements which makes it more accurate than other earlier models. The method requires simple instruments like signal generator, small DC power supply, voltage and current probes. For better accuracy specific voltage and current probes have been used as discussed in the later section. This method can be applied to any type of gate drive circuits i.e voltage or current based drivers.

As shown in Fig. 5.4 Z-port network analysis forms the basis for the proposed measurement. The input port is the gate terminal while the output port is the drain terminal of the device. The equivalent impedances consisting of respective RLC components at both the terminals satisfies the condition:

$$Z_{11} = \frac{V_I}{I_1}\bigg|_{I_2=0} \qquad Z_{12} = \frac{V_I}{I_2}\bigg|_{I_1=0}$$

$$Z_{21} = \frac{V_2}{I_1}\bigg|_{I_2=0} \qquad Z_{22} = \frac{V_2}{I_2}\bigg|_{I_1=0}$$

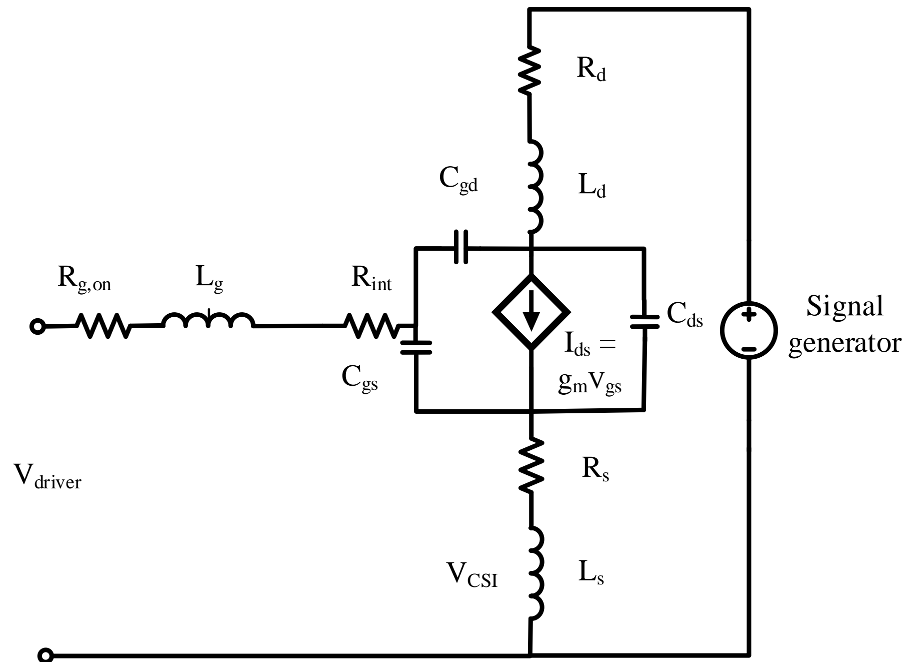


Fig. 5.3. Proposed circuit for measuring common source inductance

Following are the steps to measure the different parasitic inductances.

1. To apply the Z-network analysis either of the ports needs to be open circuited. In the case of input port this can be ensured by using a very large gate turn-on resistor (preferably in megaohms) to make the gate loop to be open circuit i.e almost no current flows through it.
2. Firstly, a DC signal is applied to different ports one by one to accurately measure the various resistances involved as shown in Fig. 5.3. A small DC signal applied with the help of signal generator will measure the voltage drops in the different loops of the above circuit. This will particularly help to measure the resistances R_d and R_s (R_{ds_on} is available in the datasheets). Also, these voltage drops takes into effect the drop in the measuring wires, R_{int} (which is the gate contact resistance or simply gate internal resistance) etc. thus thereby brings more accuracy.

$$V_{DC} = (R_d + R_{ds,on} + R_s) I_{ds,on} \quad (1)$$

3. The above relation irrespective of the applied DC voltage will provide the value of respective resistances. Important here to notify is that R_{ds_on} and R_{int} is available in the datasheets.
4. GaN device is kept in the on state when a small DC signal is applied to any of the ports 1 or 2 using signal generator.
5. Again, a small AC signal at port 2 i.e drain terminal with help of signal generator is applied when the GaN device is kept in the on-state. Firstly, the frequency of the applied AC signal is 50kHz same as power converter switching frequency.
6. Then after, the same measurements steps are followed at higher frequencies 50,100,150,200,250,300,350kHz is performed.
7. The voltage applied at any of the ports 1 or 2 and the current measured through the device will provide the impedance in the path.
8. The applied DC signal will provide the equivalent resistances in the path and an applied AC signal will provide equivalent impedance.
9. Based on the inductances involved voltage between the positive of the gate terminal and negative of the power source terminal is measured which is V_{driver} in the above circuit.
10. Secondly, the current through the device is measured i.e flowing through R_s and the common source inductance L_{CSI}.
11. Particularly for measuring the common source inductance following equations can be used by open circuiting the port 1 i.e gate terminal and applying the AC signal on port terminal i.e drain terminal:

$$V_{driver} = (R_s + jwX_{L,CSI}) I_{ds,on} \quad (2)$$

$$L_{CSI} = \frac{X_{L_{CSI}}}{2\pi f} \tag{3}$$

$$X_{L_{CSI}} = \sqrt{Z^2 - R_S{}^2} \tag{4}$$

$$Z = \frac{V_{driver}}{I_{ds,on}} e^{i\theta} \tag{5}$$

The equation (5) will provide the value of common source inductance. The equivalent resistances at the gate terminal are R_g and R_{int} and at the drain terminal is R_d, similarly respective inductances and capacitances at the gate terminal are L_g, C_g and at the drain terminal are L_d, C_d which can be expressed with the help of star-delta transformation using equations (10) - (11).

For example, Z_{11} is the impedance obtain by open circuiting the port 2 i.e drain terminal and applying at port 1 i.e gate terminal first the DC signal for obtaining the equivalent resistances and then an AC signal to obtain equivalent reactance comprising inductances and capacitances. Therefore, the overall equivalent impedances are as follows:

$$Z_{11} = R_g + R_{\text{int}} + jX_{L_g} + jX_{L_{CSI}} + jX_{C_g} + jX_{C_s} \tag{6}$$

$$Z_{12} = R_s + jX_{L_{CSI}} + jX_{C_s} \tag{7}$$

$$Z_{21} = R_s + jX_{L_{CSI}} + jX_{C_s} \tag{8}$$

$$Z_{22} = R_d + R_s + jX_{L_d} + jX_{L_{CSI}} + jX_{Cd} + jX_{C_s} \tag{9}$$

Where the capacitances C_g, C_d and C_s after star-delta transformation can be written in terms of intrinsic capacitances C_{gs}, C_{gd} and C_{ds} of the GaN device as

$$C_{gs} = \frac{C_g C_s + C_g C_d + C_s C_d}{C_d} \tag{10}$$

$$C_{ds} = \frac{C_g C_s + C_g C_d + C_s C_d}{C_g} \tag{11}$$

The above equations (10)-(11) formulates the respective capacitances C_g, C_s and C_d at ports 1 and 2 into device capacitances C_{gs}, C_{gd} and C_{ds}. Therefore, the values of the C_{gs}, C_{gd} and C_{ds} can be converted into C_g, C_s and C_d using the above equations for the calculation of the impedances.

Moreover, Fig. 5.5 shows the non-linear relationship of intrinsic capacitances C_{ISS}, C_{RSS} and C_{OSS} of the GaN device being used with the drain to source voltage and are related to C_{gs}, C_{gd} and C_{ds} by the relation.

$$C_{ISS} = C_{gs} + C_{gd} \tag{12}$$

$$C_{RSS} = C_{gd} \tag{13}$$

$$C_{OSS} = C_{gd} + C_{ds} \tag{14}$$

The real line in the Fig. 5.5 above corresponds to datasheet while dotted are the extracted values. Therefore, in this work the values for capacitances used in calculations are extracted using data extraction software and values of the involved resistances are those which is on the pcb. Therefore, to summarize firstly the capacitances C_{ISS}, C_{RSS} and C_{OSS} converted into C_{gs}, C_{gd} and C_{ds} using equations (12)-(14) then into C_g, C_s and C_d using (10)-(11).

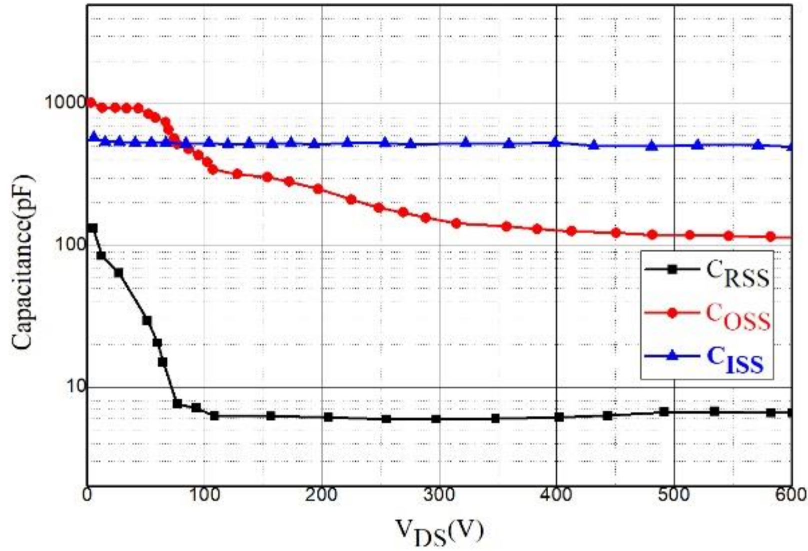


Fig. 5.4. Non-linear capacitance obtained by data acquisition software the real line is datasheet and dotted line is extracted data

5.3.1 Precise Measurement Steps

The proposed method by using Z-port mathematical analysis uses the measurement set up to extract the theses parasitic inductances. Dependence of these inductances on higher order frequencies are explained in the later section. The procedure for different inductances is as follows:

A. Common Source Inductance L_{CSI}

The most important among another parasitic inductance the common source inductance. It is different than drain and gate inductance because common source inductance is shared between gate and power loops whereas drain inductance is part of only power loop while gate inductance is part of gate drive. It can be measured by the equation

$$Z_{12} = Z_{21} = R_s + jX_{L_{CSI}} + jX_{C_s} \tag{15}$$

Firstly, by keeping the input gate terminal open and an AC signal on the port-2 drain terminal is applied. The phase difference between the gate voltage and the current through the device with the cosine function will give the value of R_s by the equation

$$R_s = \frac{V_{driver}}{I_{ds,on}} \mathrm{Cos}\, e^{i\theta} \tag{16}$$

With the calculated value of R_s using the earlier equation (7) for Z_{11} can be used to find the value of $L_{CSI.}$ The value for X_{cs} can be calculated using the equations (10)-(11) and values for the intrinsic capacitance using Fig. 4.5 These calculations are first done using a fundamental frequency and same approach can be used at higher frequencies.

The other contemporary approach can be used through Z_{21} where the drain port is kept constant and gate terminal is short circuited by using a low value of gate resistance. This will change the phase angle, voltage and current accordingly.

B. Drain Inductance L_d

The drain inductance among others is the biggest and is the inductance in series with the power loop. The earlier equation (9) is being used for calculating it.

$$Z_{22} = R_d + R_s + jX_{L_d} + jX_{L_{CSI}} + jX_{Cd} + jX_{C_s} \tag{17}$$

Gate terminal is kept open circuited with a large value of gate resistance while the ac signal is applied at the drain terminals. The current through the device and voltage in the loop decides the calculation. The value of R_s +R_d is calculated like previously using the cosine of the phase angle difference between the voltage and current.

$$R_s + R_d = \frac{V_{driver}}{I_{ds,on}} \text{Cos}\, e^{i\theta} \tag{18}$$

Finally, the value of the common source from the previous calculation can be used to solve for the drain inductance.

C. Gate Inductance L_g

Gate inductance is the smallest among others and is the inductance in series with the gate resistance i.e part of the gate drive circuit. The earlier equation (6) can be used for calculating it.

$$Z_{11} = R_g + R_{\text{int}} + jX_{L_g} + jX_{L_{CSI}} + jX_{C_g} + jX_{C_s} \tag{19}$$

In this measurement there is no measurement or signal to be applied at the drain the terminal only gate terminal while in the on-state is sufficient. The resistances R_g is the applied gate drive on resistance R_{int} is the gate terminal internal resistance or contact resistance is provided in the datasheet. An AC signal at the gate terminal will provide the value of the phase angle which will give the value of X_{LCS}+X_{cg}+X_s by the equation

$$X_s = \frac{V_{driver}}{I_{ds,on}} \text{Sin}\, e^{i\theta} \tag{20}$$

With the similar approach the value for X_{cg}+X_{cs} is calculated using the equations (10)-(11) and values for the intrinsic capacitance using Fig. 5.5 Finally, the value of the common source from the previous calculation can be used to solve for the gate inductance.

5.3.2 Selection of Optimal Frequency Range

The power converters due to pulsed switching are prone to higher order harmonics. Also, at the same time parasitic impedances due to inductances increase linearly with the frequency whereas

the capacitive impedance decreases linearly. At high frequency inductive impedance dominates in comparison to capacitive impedance. This is why an analysis and impact at higher order frequency is required. As shown in earlier equations the impedance due to common source inductance at higher frequencies makes the power converter operation worse.

There are two parameters that decide the optimal frequency range for measurement. First is the input impedance and second the gate resistance which are interrelated. Moreover, the input port impedance has dependence on the frequency and considerably affects the measurement as well so there needs to be an analysis for optimal selection of the frequency range. As per the small signal circuit shown earlier the input impedance as seen from port 1 i.e gate terminal can be formulated as:

$$Z_{input} = \frac{V_{gs}}{I_{ds}} \tag{21}$$

$$Z_{input} = (R_g + R_{\text{int}} + R_s) + \frac{R_s C_{gd}}{(C_{gd} + C_{gs})(1 + w^2 C_{eq}{}^2 R_d{}^2)} +$$

$$jw(L_{CSI}{}^3 - \frac{R_d{}^2 C_{gd} C_{eq}}{(C_{gd} + C_{gs})(1 + w^2 C_{eq}{}^2 R_d{}^2)}) \tag{22}$$

Where $C_{eq} = C_{gs}C_{gd}/(C_{gs}+C_{gd}) + C_{ds}$. The above equation clearly suggests that a very high value of the gate turn-on resistance R_g (in megaohms) makes the other two frequency dependent terms negligible at very high frequency. So, a higher gate resistance acts as a filter to remove any ringing introduced by the intrinsic capacitances, parasitic inductances and the impedance of the probe during measurement. A normalized curve between the input impedance and the frequency of the applied signal as shown in Fig. 5.5 has been used for selecting the frequency range for better accuracy. It clearly shows that the measurement up to 350kHz which is the 7th order harmonic for a fundamental frequency of 50kHz will serve the best possible accuracy especially with the voltage probes up to 20-40MΩ of bandwidth which are usually available in laboratories.

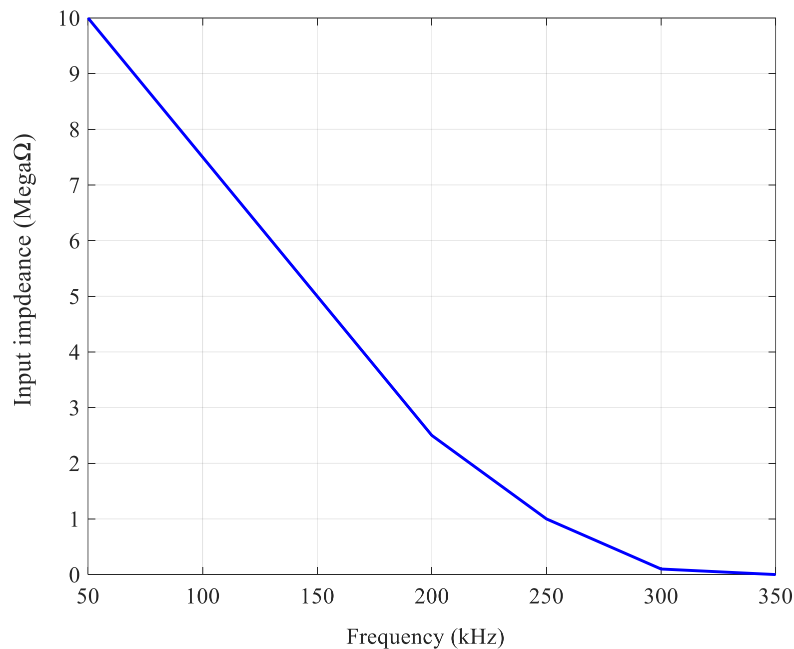


Fig. 5.5. Input impedance vs frequency variation

Therefore, this work incorporates the measurements not only at the fundamental (switching) frequency of 50kHz but also at frequencies 100,150,200,250,300 and 350khZ covering up to seventh order of harmonics. Other higher order frequency will introduce measurement error due to the reduction in the input impedance considerably which will be even worse in measuring particularly drain and gate inductances as they are higher than the common source inductance.

5.4 Simulation Verification

Since the package inductance information is missing from datasheets, there is a fundamental challenge to validate the method experimentally. Thus, simulation is used to validate the proposed method. Also, the simulation studies require information of package inductances. Thus, the presented theoretical approach has been verified with a simulation model using Ltspice software as shown in Fig. 5.6 with the parameter values of the small signal circuit (shown earlier in Fig. 5.3).

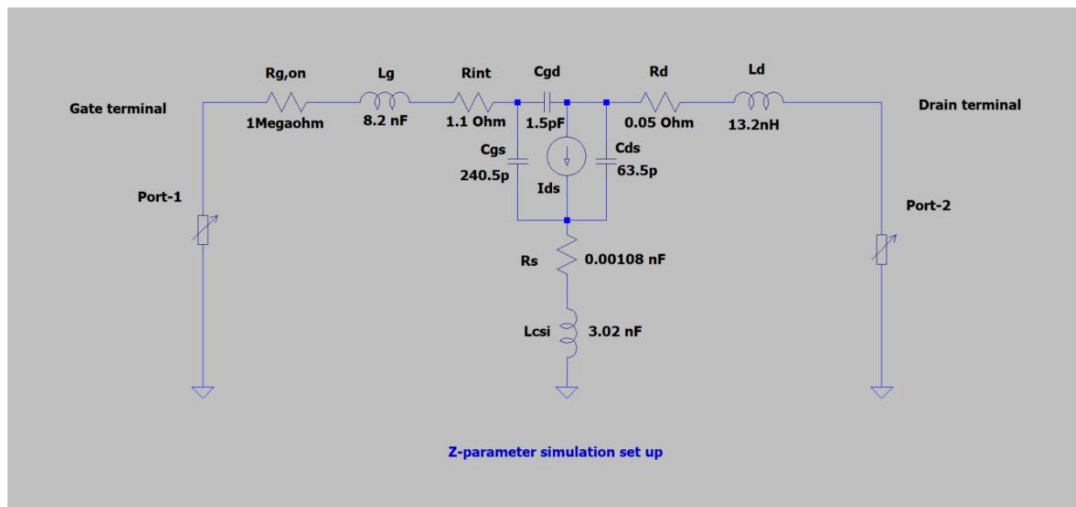
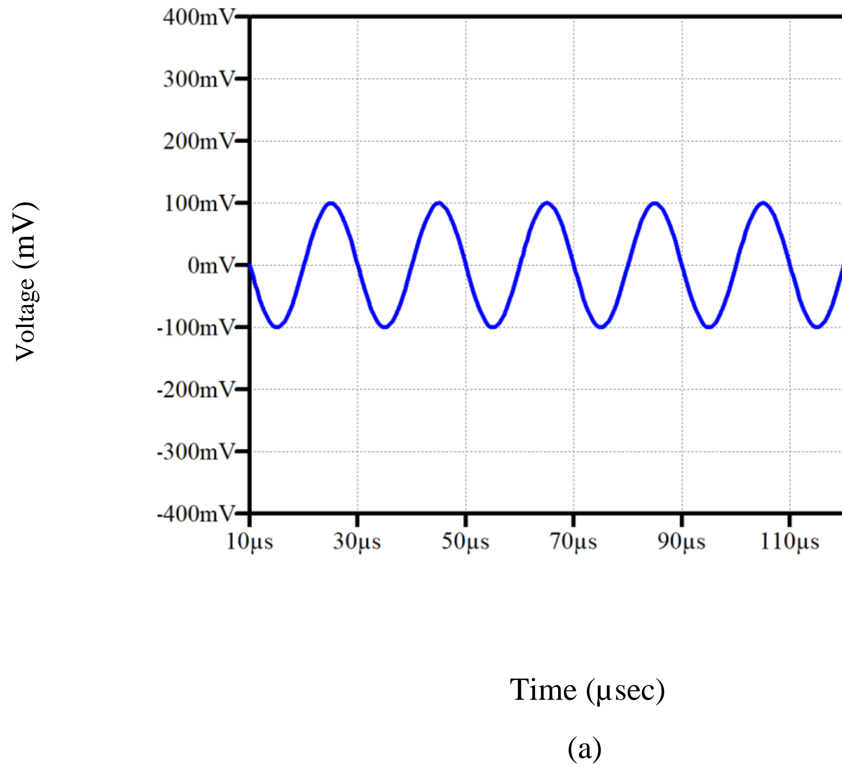
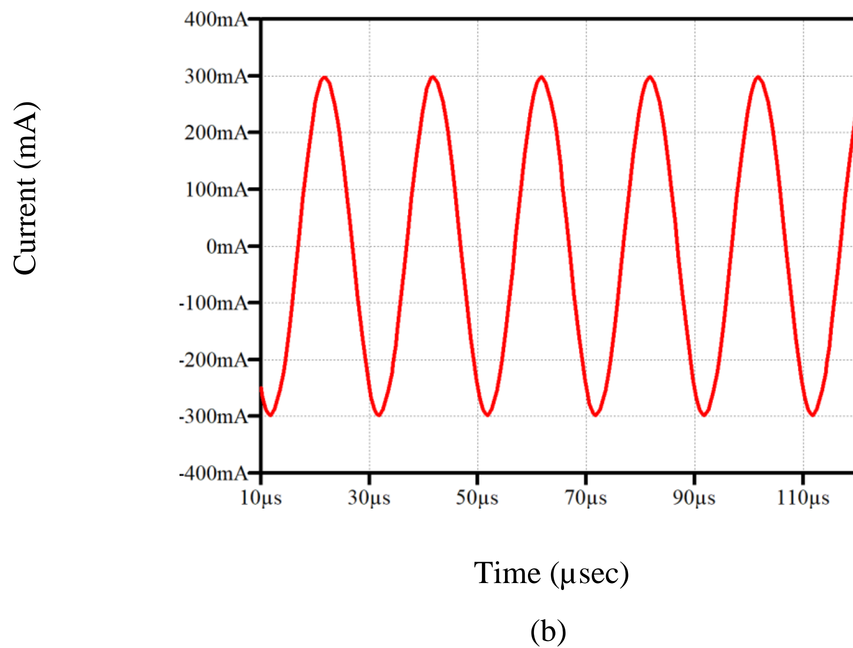


Fig. 5.6. Simulation set up and parameters



(a)



(b)

Fig. 5.7. Simulation waveforms for (a) Vg (b) Ids at 50kHz

The parameters used are taken from the datasheet [64] and the values of the different parasitic inductances in the model are actual inductances. Fig. 5.7 shows the simulation results at 50kHz of frequency. Based on this a comparison between the actual and calculated values of the different parasitic inductances using the proposed method has been presented in Table 5.2 in terms of percentage error. Thus, the values of the different parasitic inductances obtained by using the proposed method are validated through simulation in the Ltspice package as shown in Table 5.2.

Table 5.2. Validation by Simulation

Parameter	**Actual inductance in simulation**	**Calculated inductance using proposed model**	**Error%**
L_{CSI} (nH)	3.47	3.80	8.68%
L_g (nH)	9.70	10.80	10.18%
L_d (nH)	14.40	16.20	11.11%

The actual values are the means for the frequency range 50-350 kHz and similarly compared with the mean obtained with the simulation model for the same frequency range. It can be seen that the percentage error for the three parasitic inductances L_g, L_g and L_d comes out to be 8.68%, 10.18% and 11.11% respectively. There is limited literature available on simulation studies for evaluation of parasitic inductances. Precisely the most closely related literature using complex finite element-based simulation studies are presented in [7], [16], [81] for measuring GaN devices parasitic inductances. Also, these works have the limitation since the device structure related information is missing in the manufacturer datasheets.

5.5 Experiment Setup and Results

The measurement circuit shown in Fig. 5.8 comprises a surface mounted GaN systems GS66508T 650V/30A rated devices along with different probes. As shown in Fig. 5.8 for the purpose of accurate measurement of common source inductance the low-side V_{gs} is measured with the ISoVu probe (on tripod) having bandwidth up to 800 MHz (tripod) and the low-side switch current is measured using SDN-414 current shunt having 2Ghz bandwidth.

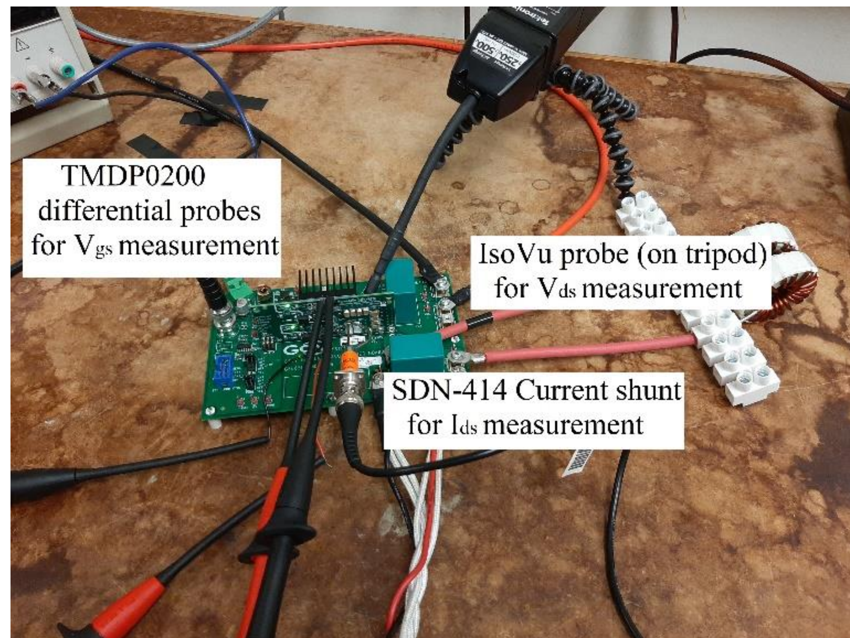


Fig. 5.8. Measurement set up for parasitic inductance

Table 5.3 summarizes the measurement setup parameters. The values for gate resistance as shown in Table 5.3 are 1 MΩ as per the analysis shown Fig. 5.6 earlier. The experimental setup includes a Tektronix AFG1022 programmable function generator, and Tektronix MSO54 4-

channel mixed signal oscilloscope. The measurement circuit uses GaN Systems' GS665MB-EVB evaluation board with GS66508T 650V/30A rated devices and ACPL-346 gate drivers.

Fig. 5.9 shows the experimental waveforms at 50 kHz. For the measurement of parasitic inductances, the mounted device has been operated by applying DC and AC signals using Tektronix AFG1022 programmable function generator and 12V auxiliary DC supply.

Measurements results at 50 kHz is shown in Fig. 5.9. The results obtained experimentally at different frequencies are shown in Table 5.4. The mean of the values at all seven frequencies are shown to present a value that is most accurate along with standard deviation and coefficient of variation.

Since the finite element simulation in [16] uses the same device GaNsystems GS66508T 650V/30A, it has been taken as a basis for comparison with prior work at 50kHz as shown in Table. 5.5. Therefore, the accuracy of the experiments is comparable with the results obtained through earlier [16] complex finite element simulation for parasitic inductance quantification.

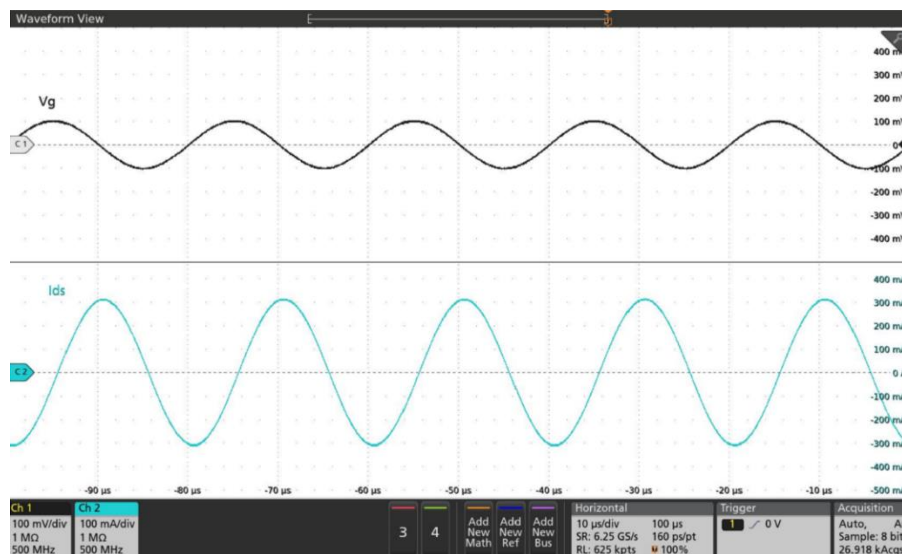


Fig. 5.9. Measurement waveforms at 50kHz

Table 5.3. Measurement Setup Parameters

Parameter	Value
AC input voltage	0.1-1V
DC input voltage	5.6/6.2V
Switching frequency	50-350 kHz
Gate turn-on resistance	1 MΩ
Gate turn-off resistance	1 MΩ

Table 5.4. Experimental Results

Parameter	Mean (50-350kHz)	Standard Deviation	Coefficient Of Variation
L_{CSI} (nH)	3.47	0.25	0.072
L_g (nH)	9.70	0.72	0.074
L_d (nH)	14.4	0.82	0.056

Table 5.5. Comparison with Previous Work

Parameter	This Work	[16]	Variation (%)
L_{CSI} (nH)	3.02	4.00	32.45
L_g (nH)	8.22	12.30	49.63
L_d (nH)	13.02	16.00	21.21

5.6 Summary

All the three parasitic inductances which are not mentioned in datasheets are a contributor to false turn-on issues particularly in high frequency GaN converters and have been measured with a straightforward method not covered in prior works. This work therefore presents a new technique for quantization of these parasitic inductances which can be directly applied to surface mounted devices. By means of two port Z-parameter analysis the measurement methodology has been

presented which requires simple laboratory instruments like auxiliary DC power supply, function generator, voltage and current probes. The simplicity of the measurement principle has been presented with detailed equations and steps that allows the accurate measurement of 1) common source inductance which is the inductance shared between gate circuit and power circuit, 2) drain inductance which is part of the power circuit, 3) gate inductance which is part of the gate circuit. The utility of this work allows power electronics design engineers to include the packaging parasitic inductances in their design for better performance of the converter.

Chapter 6: Conclusions and Future Scope

6.1 Summary of Contributions

In summary, this thesis makes contributions to three main areas related to the current challenges in the field of GaN power converters which haven't been done in previous research works. First among them is the reliability issues of GaN devices particularly in developing an optimized PWM scheme to balance potential false turn-on events which deteriorates the converter performance while at the same time maintaining high power converter efficiency. An investigation for the tradeoffs between reducing GaN false turn-on events and balancing power converter efficiency resulted in an optimized PWM scheme which comprises of variation in the all three main PWM parameters namely gate resistance, negative bias, and deadtime. This study especially focuses false turn-on issues on low side devices in half bridge configuration. Secondly, the thesis proposed a simplified hard-switching loss model comprising of both device and power circuit parameters which can be used in different operating conditions and changing gate drive configurations. This is a simple and accurate model with minimum computation for estimation of dominant hard-switching losses for high voltage GaN devices. The proposed model suggests a mechanism to

simply analyze the multi-stage switching transition lumped into a single equation and their dependence on different parameters. Thirdly, the main contributor to false turn-on issues are the different parasitic inductances which are not mentioned by manufactures so a measurement methodology which can be used by simple laboratory instruments is the third contribution. The three parasitic inductances which are not mentioned in datasheets by manufactures and are the main reason to false turn-on events particularly in high frequency GaN converters has been measured with a new measurement methodology. The proposed measurement approach can be directly applied to surface mounted devices by using simple laboratory instruments like a DC power supply, function generator, voltage and current probes.

The work clearly suggests that the use of a further negative gate bias is an important part of an ideal PWM strategy balancing efficiency and reliability. The work also show that the proposed hard-switching loss model has dependence on different gate circuit parameters on switching losses which has been calculated with variation in both gate resistance and gate bias. Moreover, the simplicity of the proposed measurement principle has been presented for common source inductance which is the inductance shared between gate circuit and power circuit. Secondly, for drain inductance which is part of the power circuit and thirdly, for gate inductance which is part of the gate circuit.

6.2 Publications

The research performed during this PhD resulted in the following publications:

[1] N. Kashyap, M. Narimani and J. Bauman, "Modified Lyapunov-Based Model Predictive Direct Power Control of an AC-DC Converter with Power Ripple Reduction," *2019 IEEE 28th International Symposium on Industrial Electronics (ISIE)*, 2019, pp. 926-931, doi: 10.1109/ISIE.2019.8781201.

[2] N. Kashyap and J. Bauman, "Optimizing PWM Control for Efficiency and Reduction of False Turn-On Events in Synchronous Buck GaN Converters," *in IEEE Access*, vol. 9, pp. 146000-146009, 2021, doi: 10.1109/ACCESS.2021.3121633.

[3] N. Kashyap and J. Bauman, "A Simple Multi Parameter Hard Switching Loss Model for High Voltage GaN Devices," *in progress.*

[4] N. Kashyap and J. Bauman, " A New Quantification and Analysis of Parasitic Inductances for Surface Mounted GaN Devices," *in progress.*

6.3 Scope for Future Research Work

Since a high voltage GaN device is still in the early development stages and existing devices still faces severe reliability issues when operating at high power and frequency, the following suggestions are proposed for future research in this area:

1. Research on active gate drivers is required to reduce the chances of false turn-on events by dampening the gate oscillations.
2. Research is required to relate false turn-on events to acknowledge change in the GaN device structure which results in degradation of the threshold voltage over a period of time.
3. Improvement in existing switching loss models to include the effect of parasitics in high voltage devices and a mechanism to include losses occurring due to momentary false turn-on events.
4. The utility of this work allows power electronics design engineers in the future to include the packaging parasitic inductances in their design for better performance of the converter.
5. Research on other factors like heating, dynamic variation in drain on-resistance and losses in the output capacitance that affects the reliability of high frequency GaN power converters.
6. Research is needed on developing a model to predict the gate voltage peak for false turn-on of normally off GaN devices in different operating conditions.
7. The proposed method for measuring parasitic inductances can be experimentally verified by using a vector network analyzer and characterizing the proposed circuit into the similar two port networks. Another method is by using a time-domain reflectometry technique and applying both small DC and AC signals as incident signals to the device and measure the reflected output signal to calculate the respective resistances and impedances.

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