DEVELOPMENT OF AN OPTIMIZATION TOOL FOR THE GEOMETRY OF INTEGRATED POWER MODULE PIN FIN ARRAYS EMPLOYED IN ELECTRIFIED VEHICLES

DEVELOPMENT OF AN OPTIMIZATION TOOL FOR THE GEOMETRY OF INTEGRATED POWER MODULE PIN FIN ARRAYS EMPLOYED IN ELECTRIFIED VEHICLES

BY

HASSAN ALEIAN, B.Eng.

A THESIS

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

AND THE SCHOOL OF GRADUATE STUDIES

OF MCMASTER UNIVERSITY

IN PARTIAL FULFILMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

Master of Applied Science

Master of Applied Science (2021) McMaster University

(electrical and computer engineering) Hamilton, Ontario, Canada

TITLE: Development of an Optimization Tool for the Geometry of Integrated Power Module Pin Fin Arrays Employed in Electrified Vehicles

AUTHOR: Hassan Aleian

B.Eng. (Electrical Engineering),

McMaster University, Hamilton, Ontario, Canada

SUPERVISOR: Dr. Ali Emadi

Dr. Mehdi Narimani

NUMBER OF PAGES: xv, 156

Abstract

The mass-market adoption of electrification in the transportation sector mandates stringent and aggressive requirements in terms of cost, power rating, efficiency, power density, and specific density of power electronics. Modular packaging of power electronics is advantageous and thus ubiquitously used by the automotive industry. A trend of shrinking die sizes and increased integration is evident and will inevitably continue. The thermal management system has become ever more significant as it is one of the main obstacles to higher power densities. The cooling system must be cost-effective, simple, efficient, reliable, and compatible with system requirements.

Pin fins are a reliable and effective means of augmenting heat transfer. They rely on inducing turbulence, increasing the effective wetted surface, and accelerating fluid velocity. Unavoidably the pin fin array also produces an undesirable pressure drop that is commensurate to the pumping power required for the system. In this thesis, a tool is developed for the geometry optimization of pin fin arrays to dissipate the heat at a rate large enough to ensure junction temperatures do not exceed the maximum value possible at a minimal pressure drop. It is hoped that this tool would contribute to the multi-physics optimization and integration of power electronics for electrified vehicles. This optimization is confined to equalaterally spaced short pin fins, aspect ratios less than three. The tool employs empirical correlations since flow

is too complex to solve analytically and numerical solutions or CFD-simulations are too time and computationally extensive.

The tool development is done in a comprehensive manner. Starting from the first principles of a two-level voltage source inverter's operation. Next, the inevitable power losses from the operation are explained and a method for their calculations is presented. Correlations in the literature related to both pressure drop and heat transfer are reviewed afterward. Then the methodology of the construction of the tool is explicated in detail. Employing a commercial power module to benchmark results; three scenarios with different flow rates and inlet temperatures are optimized for. Simulations in ANSYS Fluent are run to verify the accuracy of correlations used in the tool. Comparing the optimized geometry of pin fins to the original benchmarking geometry it is evident that employing this tool on a per-application basis provides superior performance.

Acknowledgements

In part, this research is possible thanks to funding from the Natural Sciences and Engineering Research Council of Canada (NSERC). Special thanks goes to my supervisors Dr. Ali Emadi, and Dr. Mehdi Narimani, for all the guidance, advice, support, and mentorship that they provided to me. All of the things I learned during my Master's degree is primarily due to the opportunities made possible by them. I also want to thank everyone who is a member of the McMaster Automotive Resource Center (MARC) team, working as a part of this team was both a pleasure, and an honour for me.

Also, I would like to express my gratitude for being provided an opportunity to work in the power electronics research thrust area (PE RTA) project at MARC in collaboration with Fiat Chrysler Automobile (FCA). This project, lead by Dr. Berker Bilgin, was one of the highlights of my Master's degree. I am very thankful to Dr. Berker Bilgin, working on his team we gained a lot from both the technical and project management sides. He had unbounded faith in the team and managed to teach, lead, and inspire us through challenges, allowing us to always deliver results by the deadlines we had set. Even during the unprecedented COVID virus pandemic, the team continued to make progress, while, of course, taking all the safety precautions necessary. Fatemeh Abolqasemi, Alex Wang, and Jigar Mistry were also members of

this team who contributed to my learning and overall experience at MARC. Although the overlap of Dr. Jing Guo and my time in this project didn't last long, she generously taught me an abundance of things in the early days of my work in the FCA PE RTA. After Dr. Jing Guo left the group, Dr. Peter Azer, a very good friend, took a more leading role in the PE RTA. I want to thank Peter for generously and frequently giving his time, knowledge, and advise, and I found that going to Dr. Azer was always fruitful.

I really appreciate Maryam Alizadeh who was very helpful in my early days working on thermal design for PE. This was when I became very interested in thermal design, leading me to do my thesis in this area of study. I am grateful to my good friend Sobhan Kashfi; he and I had many discussions related to thermal design, and he proved to be very helpful throughout my journey in this fascinating field. I would also like to take this opportunity to remember my dear friends and colleagues at MARC, Mehdi Eshaghian and Iman Aghabali, who perished in flight PS752, they were both close friends who will live on in our hearts and memories.

Lastly, a special thanks goes to my beloved parents, and siblings, for their unconditional love, and support, throughout my life.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Background

Mobility is a very basic and critical factor in our lives. It is central to the economy and the living standard of all. Conventional internal combustion engine-based vehicles (ICE) are unsustainable and inefficient. Generating close to one-third of the total green house gas emissions, our current transportation sector is unsustainable. Additionally, ICE based vehicles peak at efficiencies less than 30 %, making them inefficient. In contrast, the electric energy storage system, the electric machines, and power electronic converters operate at much higher efficiencies; making electrified power trains the favoured transportation solution to our sustainability goals. As grid infrastructure is not yet prolifically adapted a transitional phase has come about. Ergo, in addition to fully electric vehicles (EVs), many automotive original equipment manufacturers have introduced Hybrid Electric Vehicles (HEVs) and Plug-in Hybrid Electric Vehicles (PHEVs) to mitigate the issue of inadequate grid infrastructure.

All electrified vehicle powertrains have an electric machine (EM) that works either

with an ICE or replacing it entirely to improve fuel economy. Today, the EMs most ubiquitous in EVs are of either the AC permanent magnet (PM) or AC induction machines (IM) types [1, 2]. To drive EMs, a traction inverter is required to convert direct current from the battery pack to alternating current with controllable frequency and amplitude. Also the inverter is required to be bidirectional as to operate EMs in both motoring and generative modes. Focus is on the power electronics exclusively here in this thesis.

In 2012, the U.S. Department of Energy (DOE) defined a long term technological road map to cost effective, reliable, and high performance electrified vehicles [3]. The DOE intends to catalyze the development of compact and cost-effective electric traction drives that are competitive with the performance and reliability requirements of ICE-based vehicles, thereby, facilitating the mass market adaption of electrified vehicles of at least light-duty vehicle types. By 2020, power electronics were required to attain a continuous power rating of 30 KW (peak-power of 55KW for 18 seconds), a specific density of 14.1 KW/kg, a power density of 13.4 kW/L, at a cost of \$3.3/kW per 100,000 units [3]. Later, in 2017, requirements were updated for the year of 2025, the goal is to achieve a power density of 100kW/L at a cost of \$2.7/kW for power electronics with peak power rating of 100kW [4]. In other words, there is supposed to be an 18% cost reduction and 87% volume reduction with respect to the objectives of 2020. This implies an immense need for technological advancements as to meet such objectives and facilitate the mass market penetration of EVs.

1.2 Motivation

Wide band gap (WBG) semiconductors can operate at a higher switching frequencies as compared to silicon-based semiconductors. Operating at higher switching frequencies allows for smaller dc-link capacitors and magnetic components, improving power density significantly. WBG semiconductors have higher thermal conductivity, higher allowable junction temperatures, higher breakdown voltage, and less switching losses than silicon-based semiconductors consolidating their superiority. The only thing that detracts from the utility of WBG devices is their higher costs. Anyways, a trend is seen where power ratings is increased as chip size is shrinking; the high heat flux introduces challenges to thermal management of power converters.

For every 10^oC rise in operating temperature the rate of failure is shown to nearly double [5]. Thermal issues make up nearly 55% of electronic component failures [6], highlighting the importance of thermal management. Thermal behavior of power electronics influences the life time and reliability of electronic components in two ways that may be classified as destruction damage and fatigue of the components. Long-term exposure to junction temperatures exceeding the maximum possible value causes destruction damage. Fatigue of the components is mainly caused by the repetitive tensile and compressing stresses incurred by repetitive thermal stress due to fluctuating temperatures induced by power cycling and different coefficients of thermal expansion in materials [7].

There are many techniques to augment heat transfer. However, as was conveyed in the road-map of 2025 by the DOE, the thermal technique must be compatible with thermal techniques of other elements found in the vehicles. The coolant of Glycol-50 is selected as coolant, therefore, two-phase cooling methods are excluded.

When it comes to single-phase cooling techniques there are many possibilities that are promising, yet there is always a trade off. Direct cooling finned heat sinks remain a simple, reliable, and effective cooling method that entails relatively low pressure drop.

As component-level integration is expected to increase, a tool is devised that optimizes circular pin fin array geometry to be integrated into baseplates. The focus is not on transient thermal behavior but steady-state thermal behavior, this means that thermal requirements are tailored to prevent destruction damage. So for any module, with any power electronic converter topology sub-optimal pin fin arrays can be designed.

1.3 Thesis Objectives

Design of power electronics in the Electrified vehicle market tend to follow one of two philosophies [8]. Separately packaged or modular inverters used by many OEMs, for instance in the Nissan Leaf and Toyota Prius. These usually come in six-pack configurations but they can also come in customized configurations with charger or DC/DC-Booster typologies included, for example the Nissan Almera Hybrid. Alternatively, the inverter can be composed of discrete small and encapsulated components with single switch or half-bridge topology packages positioned in the mechanical compartment of the drive-train. Here it is common for the inverter to be integrated with the EM in same housing. The latter strategy requires the inverter to be exposed to the same climate and vibrational loading as the EM posing robustness risks and reliability issues for the inverter. Also, every discrete component is packaged and this does not allow for the optimal utility of volume. As such, in this thesis, only packaged

or modular inverters are considered.

With the trend of increased integration and ever-growing power ratings, this thesis aims to design a tool capable of detailing the optimized geometry of pin fin array to be integrated into baseplate for any topology. Though the aim is that this design tool can be extended for use in any topology it is applied to a two-level voltage source inverter here. The scope of optimization is for cylindrical pins of uniform diameter and heights in the staggered configuration. ANSYS Steady-State Thermal Analysis is used to find the minimum possible value for the effective heat transfer coefficient given worst-case calculated power loss of assumed application and power module's chip layout of representative commercial benchmarking power module as to consider heat spreading. Our approach employs empirical correlations found in literature to optimize the geometry using the genetic algorithm for a given flow rate, coolant temperature, and minimum value of effective heat transfer coefficient. ANSYS-Fluent is later used to verify solution and results are compared to benchmarking commercial hybrid pack with integrated pins.

Note in addition to power loss and chip layout the pin fin array is optimized for a given flow rate and inlet coolant temperature this is because the cooling strategy must be compatible with the cooling strategy of other component in the EV.

There are restrictions in the geometry of pin fin arrays enforced by the nature of the empirical correlations that the tool depends on. The array is defined to have pin fins that are equalaterally spaced, spacing between adjacent pins may range from 1.5 to 4 diameters, length of pins range from 2 to 3 diameters long, and diameter of pins ranges from 1.5mm to 3mm. Defining the array in terms of the diameter, pin length, and distance between pins allows for the use of empirical correlations and

genetic algorithm to ensure junction temperatures remains below the maximum value allowed while ensuring pressure drop is minimal.

1.4 Thesis Outline

This thesis begins by explaining the operation of a two-level voltage source inverter in Chapter 2. This includes the topology and modulation scheme that converts dc-current from the battery pack into AC-current with controllable amplitude and frequency. Inverter operation provides a basis that make calculating the power loss possible.

Next, in Chapter 3, Power losses are explained. This includes how losses arise during operation. Also method to calculate losses of a given application using data sheet is explicated. In addition, to provide reader a better understanding, the methodology of how the data sheet data is ascertained using an experimental setup called the double pulse test is provided.

In Chapter 4, a summary of the experimental correlations found in literature is given for both heat transfer and hydraulic friction factor. This forms the foundation of our optimization problem definition. Correlations facilitate a way to estimate pressure drop and heat transfer for a given pin fin array geometry allowing for optimization. CFD/numerical methods are very time and computationally extensive and because of the complex nature of flow analytical solutions are impossible.

Chapter 5 enunciates the optimization methodology used in the tool where for a maximum heat transfer coefficient value, flow rate, and coolant inlet temperature the optimized geometry can be found. In this chapter power losses for a given assumed application are also given.

Lastly, in Chapter 6, three different scenarios are optimized for. It begins by defining the problem using a commercial hybrid pack power module in which the pin fin array is meant to be integrated into the bottom of baseplate. Using this representative power module and maximum expected calculated power loss calculated in chapter 5 the minimum value for the effective heat transfer coefficient is found using ANSYS Steady-State Thermal Analysis. The tool is employed to optimize for the three scenarios. Lastly CFD simulations are run as to validate results and evaluate the accuracy of the modelling in the optimization tool. Results are benchmarked to a commercially available Hybrid pack that is designed for.

Chapter 2

Operation of Two-Level Voltage Source Inverter

2.1 Introduction

Electrified vehicle powertrains are mainly composed of an electric machine, an inverter, a controller, and a battery pack, as shown in Figure 2.1. Electric machines convert electrical energy into mechanical energy and vice versa. The battery pack supplies electrical power, which the inverter manipulates to form specific current waveforms. When applying these current waveforms to stator windings, the motor outputs desired torque. The controller ensures that the inverter produces current waveforms that correlate to the motor's desired torque.

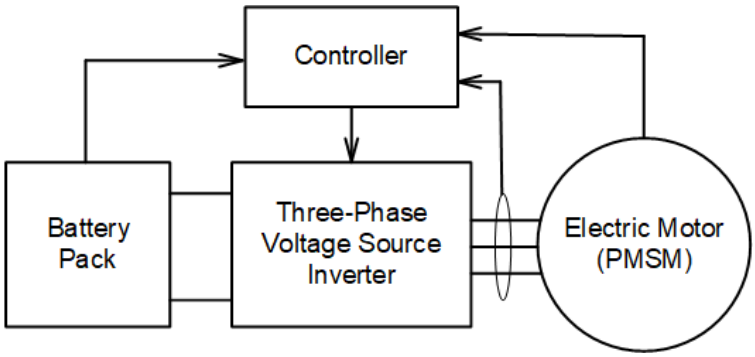


Figure 2.1: Typical Electrified Vehicle Powertrain

Due to high power density, high torque, relatively simple control, and high efficiency over a wide operating range, Permanent Magnet Synchronous Motors (PMSMs) are generally the favored electric machine. Despite these advantages, PMSMs are costly and require rare earth materials to make permanent magnets. In addition, owing to their maturity, reliability, simple control, and relative low component count, three-phase Voltage Source Inverters (VSIs) are the most ubiquitously used traction inverter topology in automotive motor drive applications.

Although the battery pack is usually connected directly to the inverter, adding a DC-DC converter between the VSI and battery, as in Fig.2.2, has many benefits. These advantages include:

- Battery packs that are smaller and less expensive are permitted when utilizing a DC-DC converter because the output voltage only needs to meet the requirements of the DC-DC converter [9–11].

- When the VSI's DC-link bus is connected directly to the battery, the drive's performance can degrade as the state of charge drops. DC-DC converters can mitigate this issue [12].

- DC-DC converters add a degree of freedom, the DC-link voltage. Adjusting the DC-link voltage to an optimal value for all operating points can improve overall drive efficiency regardless of the losses generated by the DC-DC converter [9–11].

Despite this, the increased component count and cost usually detract from their utility. For the sake of minimizing the volume of power electronics (PE) and simplicity, it is assumed the inverter connects directly to the battery pack.

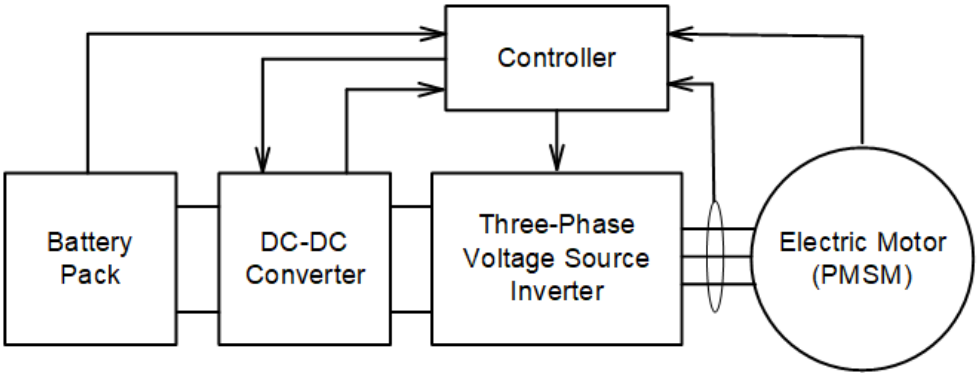


Figure 2.2: Electrified Vehicle Powertrain with DC-DC Converter

2.2 Topology

As displayed vividly in Fig.2.3, each of the three legs consists of a high-side (HS) and low-side (LS) switch. Switches are composed of semiconductor transistors with accompanying anti-parallel free-wheeling diodes (FWD). Inductive loads like electric machines cause phase currents to lag phase-voltage waveforms by some angle ϕ. Moreover, inductive loads lead to considerable voltage spikes when the current experiences abrupt change. FWDs assure a continuous flow of current protecting transistors from deterioration or potential destruction due to voltage spikes. Also, FWDs facilitate a current path making regenerative braking feasible.

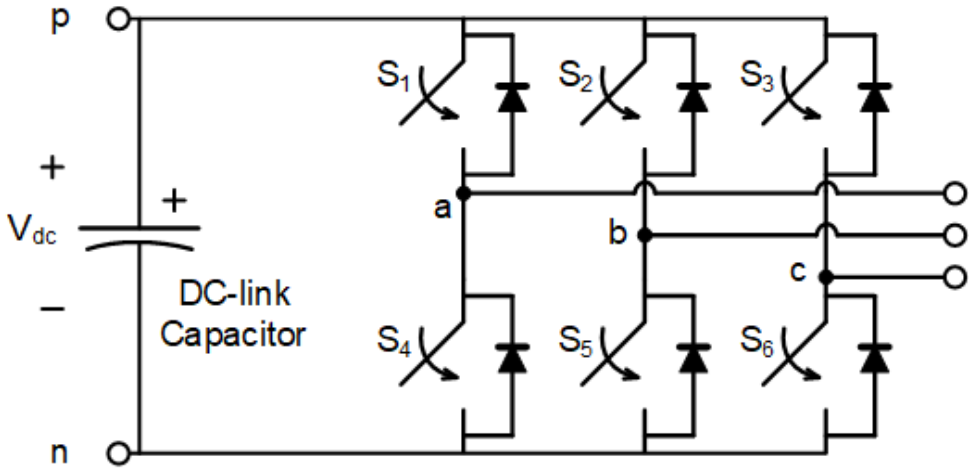


Figure 2.3: Three-Phase Voltage Source Inverter

A switch comprises of multiple semiconductor transistors in parallel and or in series to realize high current and voltage ratings in demanding applications. Power switch devices in inverters do not operate in the active region of i-v characteristics. Active region operation does exhibit a favorable attribute where line-to-ground voltage can be continuously varied, from $0 \rightarrow V_{dc}$, by applying a matching gate voltage. Despite this advantage, the active region suffers high power loss since both a high voltage drop across semiconductors and considerable current through the switching device coincide. On the other hand, if operating in saturation (On) region or cutoff region (Off), power losses remain relatively low. Although a high current traverses across the transistor, the voltage drop is negligible in the on-state region. Conversely, in the off-state region, a high voltage drop is applied across semiconductors, but the current is negligible. Since either voltage or current is negligible, losses remain low, the inverter consequently operates only in saturation or cutoff regions.

It follows that switches can either be on or off; a leg can therefore be in one of four states. However, there are only two permissible states due to practical restrictions.

To elaborate, the HS switch and LS switch for a given leg must not have the same switching state. Turning both HS and LS switches simultaneously on leads to a short circuit across the dc-link. In contrast, turning both HS and LS switches off the phase voltage is undefined. In the latter scenario, phase voltage is undefined because it can be clamped, by a free-wheeling diode, to either the upper dc-link rail or lower dc-link rail, depending on the polarity of phase current at that instant. Therefore, each leg has two possible states, leaving the three-phase inverter with a total of eight switching states. Modulation techniques achieve desired waveforms by traversing between these eight different switching states.

The majority of EV traction inverters today are 400V based, Insulated-Gate Bipolar Transistor (IGBT) devices easily meet this requirement. IGBTs are inexpensive, well-established, and reliable, justifying their dominance in traction inverter applications. Upcoming Wide-bandgap semiconductors (WBG) can withstand higher temperatures, breakdown voltages, lower losses, and higher switching frequencies than Si-based IGBTs. Namely, the Silicon-Carbide (SiC) and Gallium Nitride (GaN) semiconductors are auspicious materials and are getting much attention. For now, IGBTs remain adequate, and unlike WBG devices, cheap.

DC-link capacitors enable the switching operations by providing reactive power.They also serve to suppress voltage ripples, attenuate current ripple, and reduce electromagnetic interference (EMI) emissions. They are heavy, expensive, and oversized, causing a significant obstacle for attaining high power density. Extensive studies have been conducted on analyzing and modeling the capacitor as not to overdesign it [13–17]. In the automotive industry, because of the high RMS current handling requirements of dc-link capacitor film capacitors are preferred to their electrolytic counterparts [18].

2.3 Modulation Schemes

Three-phase voltage source inverters produce three-phase output voltage waveforms that are 120° electrically phase-shifted concerning each other. Phase, amplitude, and frequency of said waveforms are controllable. An inverter chops the dc-voltage into a pattern of pulses with deliberately varying pulse widths by switching, constituting a desired fundamental waveform with unavoidable harmonic components. This process is called pulse width modulation (PWM). Different PWM techniques are used to elicit the desired output phase voltage waveforms. Many studies have been undertaken to form vast works on the subject of modulation schemes. However, the main techniques include: Sinusoidal Pulse Width Modulation (SPWM), Space Vector Pulse Width Modulation (SVPWM), Sinusoidal Pulse Width Modulation with Zero-Sequence Signal Injection,and Square Wave Modulation. Notation and circuit in figure 2.4 is used to explain different modulation schemes.

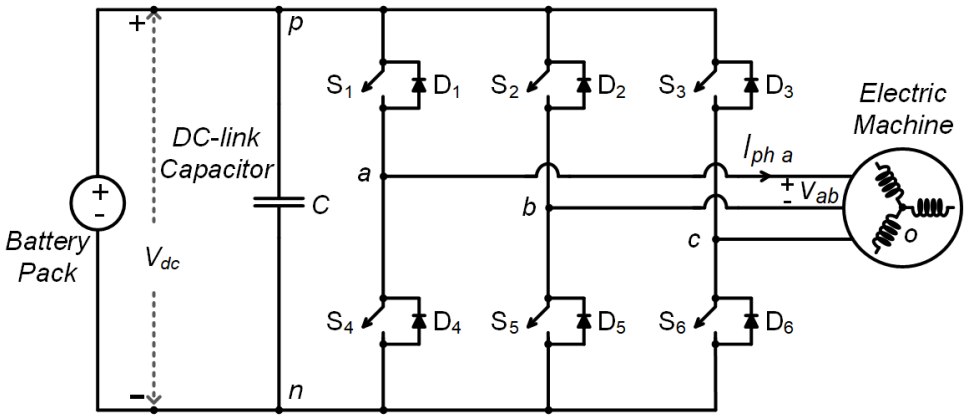


Figure 2.4: Three-Phase Voltage Source Inverter, PMSM, and battery pack schematic used for following discussions

2.3.1 Sinusoidal Pulse Width Modulation (SPWM)

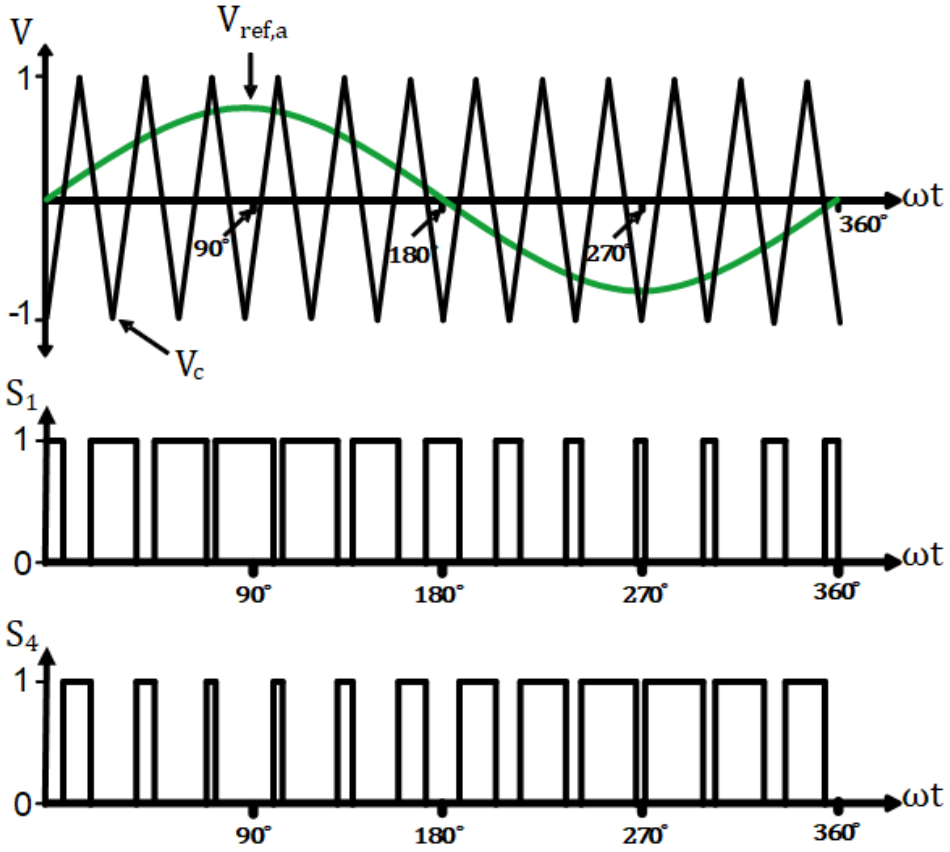


Figure 2.5: Illustration of SPWM pertaining to phase leg-a with resulting switch states. S_1 and S_4 are HS and LS switch of phase leg-a. A logic 1 denotes turned on and a logic 0 denotes switch being off.

SPWM is a classic technique, and the implementation is relatively straightforward. For simplicity, the discussion commences considering only a single phase-leg, namely leg-a. To produce a desired ac output phase voltage, a reference sinusoidal signal V_{ref} is compared to a high frequency triangular carrier signal V_c. Furthermore, when reference signal is greater than the carrier signal ($V_{ref} > V_c$), the HS power switch is switched on and consequently the LS switch is off, this results in $V_{an} = V_{dc}$. Where,

V_{an} is the voltage across the point labeled 'a', the output of leg-a, and point 'n,' the LS dc bus rail, as illustrated in figure 2.3. Alternatively, when the reference signal is less than the carrier ($V_{ref} < V_c$), LS switch is conducting, and the HS switch is off leading to $V_{an} = 0$.

Carrier signals have a high frequency ($f_c >> f_{ref}$), such that within a period of the carrier signal, the instantaneous value of the reference signal can be approximately assumed constant. When a reference signal is near its crest, the HS switch is turned on for the lengthiest duration of a carrier's period. On the other hand, in the proximity of a reference signal's trough, the HS switch conducts for the shortest duration for that given reference signal. Assuming the carrier signal oscillates between 1 and -1, the reference signal is defined as in eq 2.1.

$$V_{ref} = m \sin(\omega t) \tag{2.1}$$

Where ω is the angular frequency of desired output waveform and can be described in terms of fundamental frequency of output phase voltage waveform (f_1) as $\omega = 2\pi f_1$ and m is called a modulation index and is defined by eq 2.2.

$$m = \frac{\hat{V}_{ref}}{\hat{V}_c} \tag{2.2}$$

Where $\hat{V_{ref}}$ and $\hat{V_c}$ denote peak values of reference and carrier signals, respectively.

Any point along the reference signal corresponds to a pulse with a pulse duration

given by the duty cycle eq 2.3.

$$d = \frac{1 + m\sin(\omega t)}{2} \tag{2.3}$$

From equation 2.3 it is found that the train of pulses generated by this modulation technique is such that every pulse varies in pulse width proportionally to the instantaneous value of the reference wave. As time is traversed, the resulting fundamental component of the train of pulses has the same frequency as the reference waveform. Additionally, changing the modulation index within the range $0 \leq m \leq 1$, increases pulse widths of all points linearly. Modulation index can therefore control the amplitude of the fundamental component as conveyed in

$$\hat{V_{an\ 1}} = m \cdot \frac{V_{dc}}{2}. \tag{2.4}$$

Until now, only a single phase-leg was discussed, to establish three-phase voltage waveforms, three identical reference signals are used with a phase shift of $\pm 120\,\text{deg}$ between them as shown below. Each reference wave is compared to the carrier signal and controls the switching of HS/LS power switches of the respective leg exactly in same manner as was discussed on leg-a.

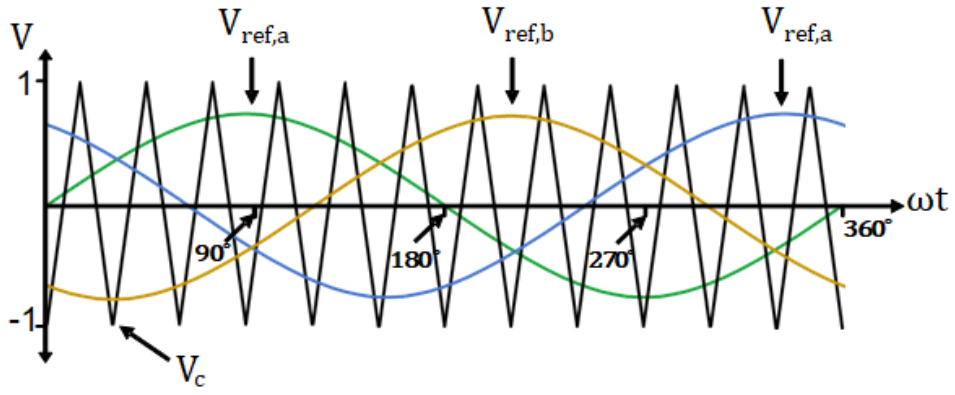


Figure 2.6: Waveforms used to implement SPWM

2.3.2 Space Vector Modulation (SVM)

Two-level VSIs have eight possible switching states. Recall, the high-side and low-side switches must have alternative states to eliminate shoot-through current and undefined instantaneous phase voltage values. Here we will discuss the SVM modulation scheme based on [19]. The different switching states are denoted with three binary bits [b_1, b_2, b_3], standing for the HS switching states of phase-a, phase-b, and phase-c, respectively. For each phase, the corresponding bit with a logic 1 means the HS switch is turned on, and the phase terminal is connected to the upper dc-link rail. In contrast, a logic 0 means the LS switch is turned on, and the corresponding phase terminal is connected to the lower dc-link rails. Referring to Fig.2.3, the voltage of phase with respect to lower dc-link rails "n" can be easily deduced. For example; if $b_1 = 1$ than $V_{an} = V_{dc}$, conversely, if $b_1 = 0$ than $V_{an} = 0$. Similarly, voltages of the phase terminals with respect to lower dc-link rail can be constructed from the switching states.

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = V_{dc} \begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} \tag{2.5}$$

Focusing on relating between phase voltages and voltage across output phase terminals to lower dc-link rails. Inverter is assumed three-phase balanced $V_{ao} + V_{bo} + V_{co} = 0$ (no zero sequence component). Neutral of EM stator winding is denoted as point 'o' as is shown in 2.4. Performing KVL than yields equations 2.6.

$$\begin{aligned} V_{an} - V_{on} - V_{ao} &= 0 \\ V_{bn} - V_{on} - V_{bo} &= 0 \\ V_{cn} - V_{on} - V_{co} &= 0 \end{aligned} \tag{2.6}$$

Adding equations of 2.6 and recalling that inverter is three-phase balanced V_{on} is found(i.e. voltage between neutral of machine's stator windings and lower dc-link rail)

$$V_{on} = \frac{(V_{an} + V_{bn} + V_{cn})}{3}. \tag{2.7}$$

Substituting eq 2.7 in eq 2.6; instantaneous output three-phase voltages are described:

$$\begin{bmatrix} V_{ao} \\ V_{bo} \\ V_{co} \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & \frac{-1}{3} & \frac{-1}{3} \\ \frac{-1}{3} & \frac{2}{3} & \frac{-1}{3} \\ \frac{-1}{3} & \frac{-1}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \tag{2.8}$$

Until now, given a switching state the resulting instantaneous phase voltages can be computed. For example, by applying the switching state [1, 1, 0]. Using eq 2.5, it is found that $V_{aN} = V_{dc}$, $V_{bN} = V_{dc}$, and $V_{cN} = 0$. Subbing the voltages of phase terminals with respect to lower dc-link rail into eq 2.8, it follows that $V_{ao} = \frac{-V_{dc}}{3}$, $V_{bo} = \frac{-V_{dc}}{3}$, and $V_{co} = \frac{2V_{dc}}{3}$. Note that any phase voltage is equal to the negative sum of other two, a direct consequence of having three-phase balanced load. Hence computing all three phase voltages is redundant.

Since three-phase variables are not independent, they can be expressed as two-phase variables and therefore can be elegantly described by a planar vector. Using the complex plane, it is possible to construct a space vector containing two components a real component (α) and imaginary (β). Space vectors are similar to phasors with the distinction that their magnitudes can be time-varying. Converting from three-phase voltages to the α, β - phase voltages can be performed through the Amplitude Invariance Clarke Transform eq 2.9.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{ao} \\ V_{bo} \\ V_{co} \end{bmatrix} \tag{2.9}$$

A constant of 2/3 is employed in order that amplitude of V_α and V_β matches that of balanced three-phase load voltages. Balanced 3-phase ac voltages can now be represented as $V = V_\alpha + jV_\beta$. Taking advantage of Euler's formula ($e^{jx} = cos(x) + j\ sin(x)$), it follows.

$$V = \frac{2}{3} \left(V_{ao} \ + V_{bo}\, e^{j2\pi/3} + V_{co}\, e^{j4\pi/3} \right) \tag{2.10}$$

Remarking that the two switching states [0, 0, 0] and [1, 1, 1] are redundant and constitute Zero Vectors. Later the importance of redundant zero vectors in how they facilitate lower switching frequency will become more obvious. The remaining space vectors for other switching states, V_1 through V_6, are termed Active Vectors.

To summarize because balanced loads elicit three-phase voltage waveforms with inherent dependence between them that can be wholly described with two variables in a complex plane. Thus far, the instantaneous three-phase ac voltage waveform values generated by all possible switching states has been converted into stationary space vectors. Moving forward, recall that the objective is to produce controllable three-phase ac-voltage waveforms with variable amplitude, phase, and frequency. Expressed in equation 2.3.2 is a definition for the target waveforms. Where the asterisk denotes

Space Vectors		
Switching State [b1, b2, b3]	Instantaneous 3ϕ -Voltages $[V_{aO}, V_{bO}, V_{cO}]$	Space Vector
0, 0, 0	0, 0, 0	$V_0 = 0$
1, 1, 1	0, 0, 0	$V_0 = 0$
1, 0, 0	$\frac{2V_{dc}}{3}$, $\frac{-V_{dc}}{3}$, $\frac{-V_{dc}}{3}$	$V_1 = \frac{2V_{dc}}{3}\ e^{j0}$
1, 1, 0	$\frac{V_{dc}}{3}$, $\frac{V_{dc}}{3}$, $\frac{-2V_{dc}}{3}$	$V_2 = \frac{2V_{dc}}{3}\ e^{j\pi/3}$
0, 1, 0	$\frac{-V_{dc}}{3}$, $\frac{2V_{dc}}{3}$, $\frac{-V_{dc}}{3}$	$V_3 = \frac{2V_{dc}}{3}\ e^{j2\pi/3}$
0, 1, 1	$\frac{-2V_{dc}}{3}$, $\frac{V_{dc}}{3}$, $\frac{V_{dc}}{3}$	$V_4 = \frac{2V_{dc}}{3}\ e^{j\pi}$
0, 0, 1	$\frac{-V_{dc}}{3}$, $\frac{-V_{dc}}{3}$, $\frac{2V_{dc}}{3}$	$V_5 = \frac{2V_{dc}}{3}\ e^{j4\pi/3}$
1, 0, 1	$\frac{V_{dc}}{3}$, $\frac{-2V_{dc}}{3}$, $\frac{V_{dc}}{3}$	$V_6 = \frac{2V_{dc}}{3}\ e^{j5\pi/3}$

Table 2.1: Summary of switching states for Space Vector Modulation Scheme

that these are the target or desired waveforms, $\hat{V}$ is the desired amplitude of said waveforms, ϕ is desired phase shift, and lastly, ω^* is the desired angular frequency. $\omega^* = 2\pi f^*$, f^* is desired frequency of waveforms.

$$\begin{aligned} V_{ao}^* &= \hat{V} sin(\omega^* t + \phi) \\ V_{bo}^* &= \hat{V} sin(\omega^* t - 2\pi/3 + \phi) \\ V_{co}^* &= \hat{V} sin(\omega^* t + 2\pi/3 + \phi) \end{aligned} \tag{2.11}$$

If eq 2.3.2 is applied into eq 2.10, the expression simplifies into

$$V^* = \hat{V} e^{j(\omega^* t + \phi)}. \tag{2.12}$$

Unlike vectors representing switching states, the reference vector rotates with time at an angular frequency ω^* and has a length equivalent to the amplitude of target phase voltages (Amplitude invariant transform). Specifically, the phase angle at instant t of reference vector with respect to the positive real axis is defined by

$$\theta(t) = \int_0^t \omega^* dt + \phi. \tag{2.13}$$

As commanded target phase voltages are embodied in a rotating reference vector, the vector is sampled periodically at a prescribed sampling frequency and synthesized by two adjacent stationary active vectors and the stationary Zero vector. Standard switching frequency in automotive motor drive applications typically ranges between 10-15 kHz. Stationary space vectors relating to eight switching states produce discrete instantaneous three-phase voltage values (0, $\pm 1/3$, and $\pm 2/3$); however, sinusoidally varying values are desired. A compromise is made where reference vector adjacent space vectors are applied such that the average over a sampling period equals voltage values equivalent to the instantaneous sinusoidally varying target three-phase voltage output values. The compromise is that the fundamental component obtains the target ac three-phase voltage, but additionally, undesired higher-order components are presented as harmonic losses. Mathematically the technique is termed "Volt-Second Balancing". Initially, the stationary active vectors divide the complex plane into six sectors; the sector is denoted by k, depending on θ.

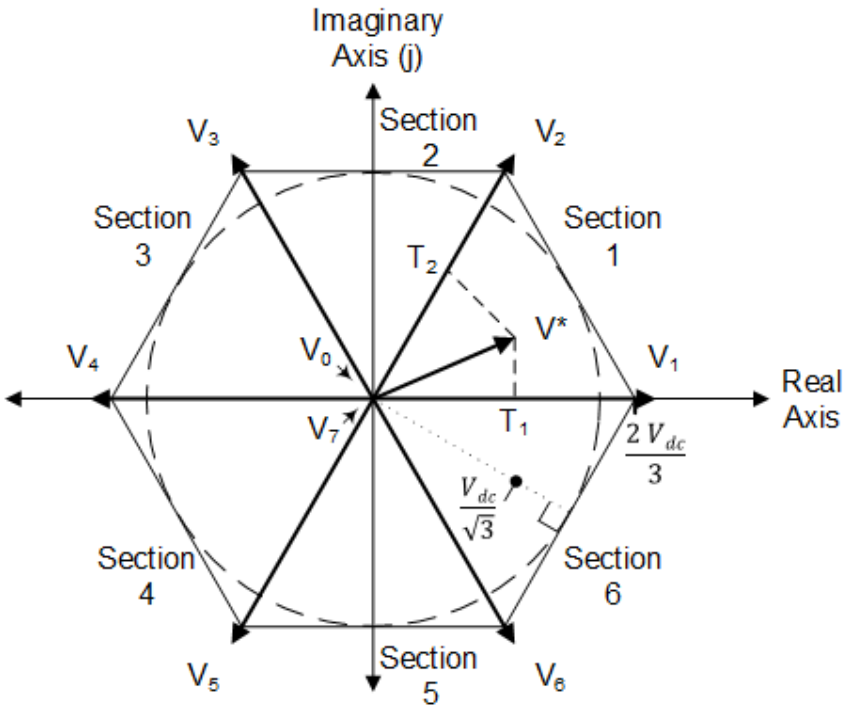


Figure 2.7: Modulation range for space-vectr modulation

$$k(\theta) = \begin{cases} 1 & \text{if } 0 \leq \theta \leq \frac{\pi}{3} \\ 2 & \text{if } \frac{\pi}{3} \leq \theta \leq \frac{2\pi}{3} \\ 3 & \text{if } \frac{2\pi}{3} \leq \theta \leq \pi \\ 4 & \text{if } \pi \leq \theta \leq \frac{4\pi}{3} \\ 5 & \text{if } \frac{4\pi}{3} \leq \theta \leq \frac{5\pi}{3} \\ 6 & \text{if } \frac{5\pi}{3} \leq \theta \leq 2\pi \end{cases} \tag{2.14}$$

Stationary active vectors V_k and V_{k+1} are applied when reference vector is sampled. While reference vector traverses in sector "k", V_k and V_{k+1} are applied for durations

derived by projecting the reference vector onto respective active vectors. Durations are denoted as T_k and T_{k+1} and are calculated using equations of 2.15.

$$T_k = \frac{\sqrt{3}\, T_s\, V_{ref}}{V_d}\; sin(\frac{\pi}{3}\,(2-k) - \theta) \tag{2.15}$$
$$T_{k+1} = \frac{\sqrt{3}\, T_s\, V_{ref}}{V_d}\; sin(\frac{\pi}{3}\,(2-k) - \theta)$$
$$T_0 = T_s\; - T_k\; - T_{k+1}$$

Furthermore, sequence of applied switching states are selected to minimize switching frequency and optimize harmonic performance. Every switch must turn-on and turn-off a maximum of one time this establishes a switching frequency equating to sampling frequency. Meeting this requirement dictates that the sequence must start with a zero vector and toggle between active states until alternate zero vector is applied, then it sequence reverses ending with initial zero vector. For instance when in sector 1, a sequence of [0,0,0], [1,0,0], [1,1,0], [1,1,1], [1,1,0], [1,0,0], and [0,0,0]. The durations are based on eq 2.15; both [0,0,0] state is applied for $T_0/4$, [1, 1, 1] for $T_0/2$, each [1,0,0] and [1,1,0] for $T_k/2$ and $T_{k+1}/2$, respectively.

2.3.3 SPWM with Zero Sequence Signal Injection

SVM requires a considerable amount of calculations, leading to an alternate modulation technique that is simpler to implement; SPWM with zero-sequence signal injection (third harmonics). Both modulation techniques extend the linear range by 15% and result in the same DC-bus voltage utilization. SPWM with zero-sequence

signal injection is detailed in a simple and elegant manner in [20], based on this dissertation, a brief and concise description of this modulation scheme is provided here. Implementation of SPWM with zero-sequence signal injection is the same as SPWM with a minor distinction. Three reference signals ($V_{ref,a}$, $V_{ref,b}$, and $V_{ref,c}$) are compared to a triangular carrier signal (V_c), except here, adding a term to the reference signals unlike in the standard SPWM.

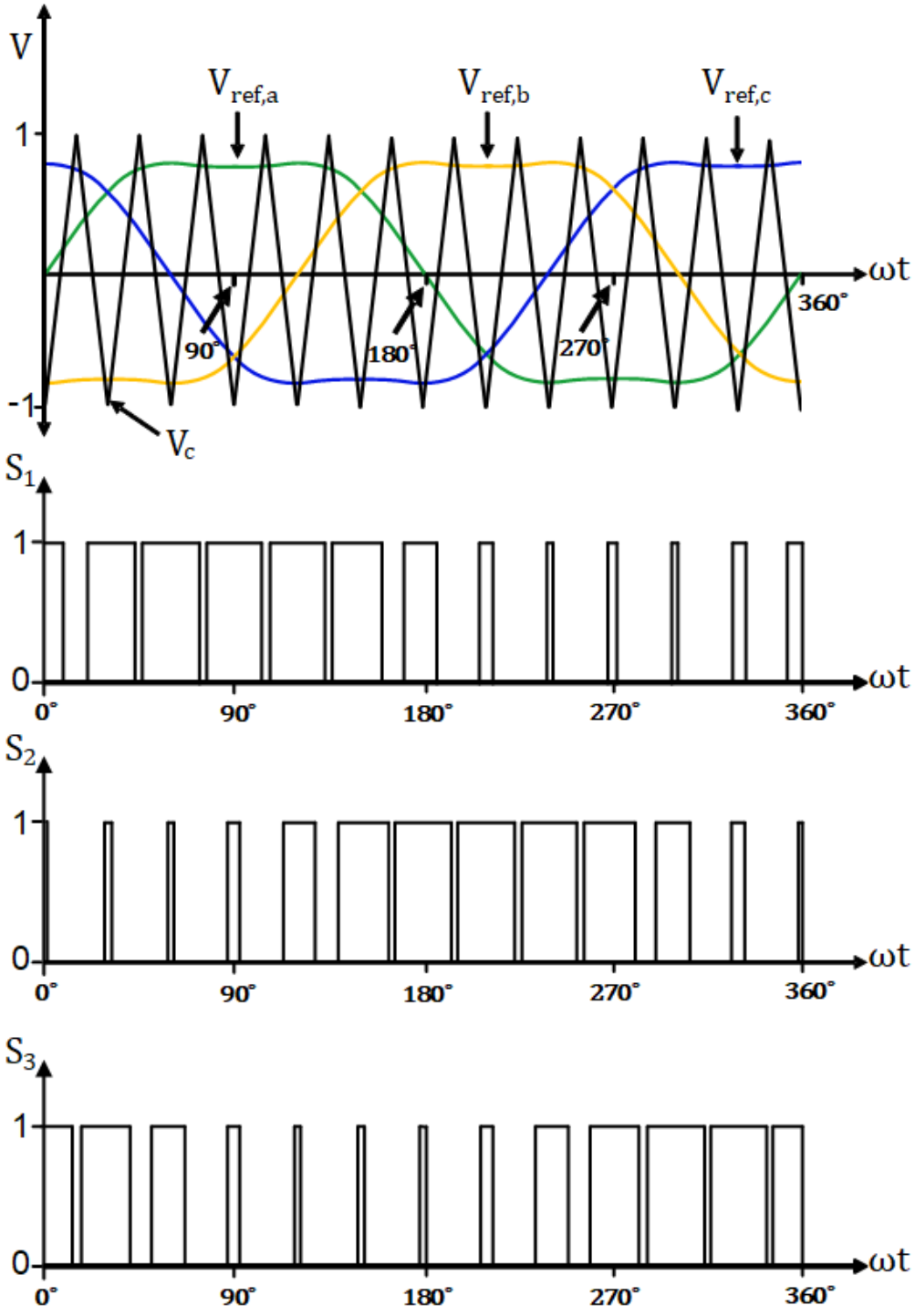


Figure 2.8: Waveforms used to implement SPWM with Zero-Sequence Injection and resulting gate pulse for HS switches for three-phase legs

$$V_{ref,a} = m\ sin(\omega t) + V_0 \tag{2.16}$$
$$V_{ref,b} = m\ sin(\omega t - \frac{2\pi}{3}) + V_0$$
$$V_{ref,c} = m\ sin(\omega t + \frac{2\pi}{3}) + V_0$$

V_0 is the zero sequence signal, where

$$V_0 = -\frac{1}{2}(V_{max} + V_{min}) \tag{2.17}$$

and

$$V_{max} = max(sin(\omega t), sin(\omega t - \frac{2\pi}{3}), sin(\omega t + \frac{2\pi}{3})) \tag{2.18}$$
$$V_{min} = min(sin(\omega t), sin(\omega t - \frac{2\pi}{3}), sin(\omega t + \frac{2\pi}{3})).$$

By adding the zero-sequence signal, the fundamental component of the reference signal is the same while reducing the peak of the reference signal. Instead of the modulation index capping at 1 for linear range, like in SPWM, the modulation index now is limited to $\frac{2}{\sqrt{3}}$. The amplitude of the line-to-line fundamental voltage waveform for VSI in the linear range is delineated as

$$V_{ab} = m\frac{\sqrt{3}}{2}V_{dc}. \tag{2.19}$$

Recall V_{dc} is the dc-link voltage, or voltage across point 'p' and 'n' in fig 2.3. Pushing the modulation index 15.5% higher results in 15.5% higher dc-link voltage utilization.

2.3.4 Six Pulse Modulation

Previously, a carrier based sinusoidal pulse width modulation technique was discussed. The discussion was restricted to linear range of modulation, that is where modulation index linearly controls amplitude of resulting fundamental three-phase voltage waveforms. Further increasing modulation index beyond $M_a = 1$ prompts a non-linear rise in fundamental phase voltage amplitude and unavoidable low-order harmonics. Accompanied by a modulation index of 3.24,"full over-modulation", the largest fundamental phase voltage amplitude ($\frac{4}{\pi}\sqrt{3}\frac{V_{dc}}{2}$) attainable by a two-level three-phase inverter is realized. Full over-modulation is also known as square-wave or six-pulse operation.

Six-pulse operation results in every switch conducting for π radians periodically [21]:

$$S_1 \text{ conducts from : } 0 \rightarrow \pi \text{ radians}$$
$$S_2 \text{ conducts from : } \frac{2\pi}{3} \rightarrow \frac{5\pi}{3} \text{ radians}$$
$$S_3 \text{ conducts from : } 0 \rightarrow \frac{\pi}{3} \quad and \quad \frac{4\pi}{3} \rightarrow 2\pi \text{ radians}$$

Figure below displays the switching states, ones denote on-state, and resulting phase voltage (V_{ao}) produced from leg-a. Despite six-pulse operation maximizing fundamental phase voltage amplitude for given dc-link voltage, the higher non-contributing harmonic content are responsible for losses in system. Harmonics degrade efficiency, increase thermal load, and cause torque pulsations in machine (significant at low

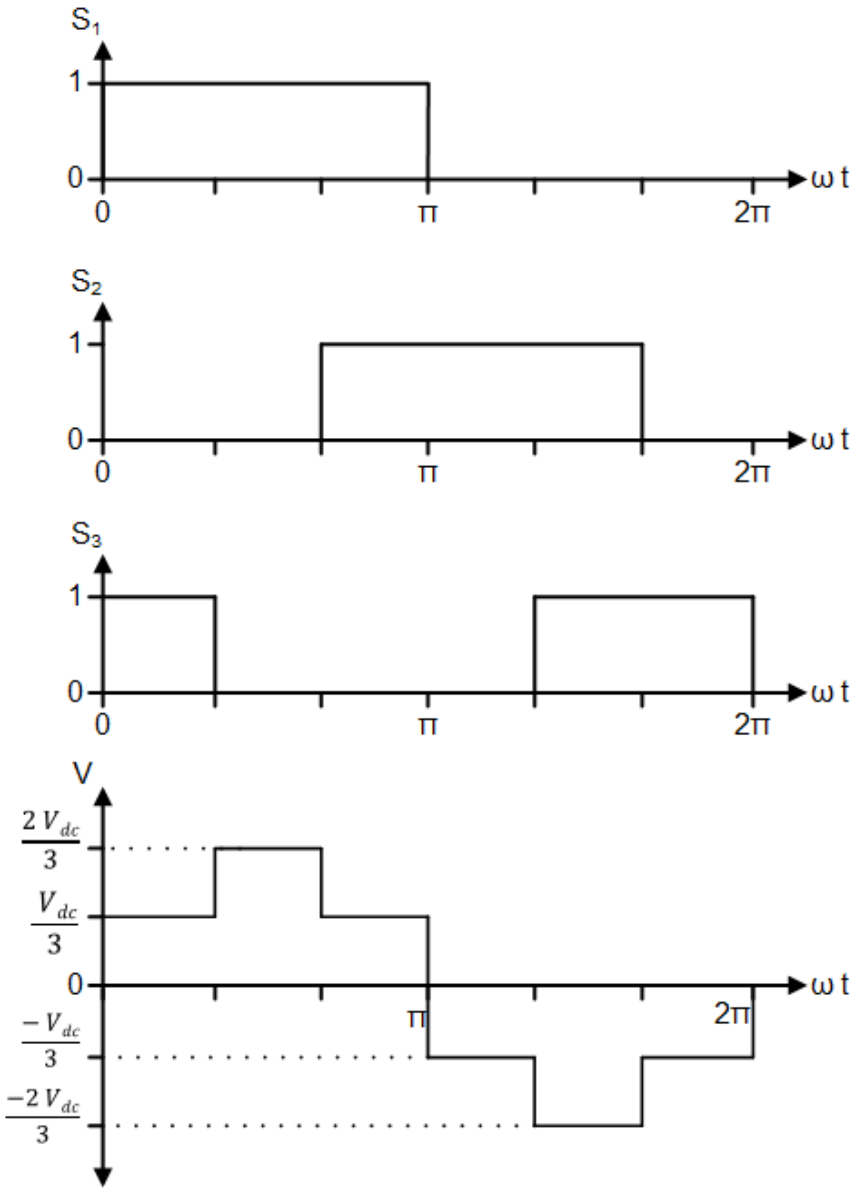


Figure 2.9: Waveforms used to implement 6-step modulation, and phase voltage of leg-a (V_{ao}).

speeds). Line-to-line voltage harmonics have amplitudes inversely related to order of harmonic eq 2.20. Harmonics are found at orders "h" of fundamental, where h = 6 k

$\pm$ 1 (k = 1,2,3, ...).

$$\hat{V}_{ab} = \frac{4}{h\pi}\sqrt{3}\frac{V_{dc}}{2} \tag{2.20}$$

2.4 Summary

Our development of the pin fin geometry optimization tool is tailored specifically for a basic two-level voltage source inverter. As such, it is valuable to begin our development from first principles such that power losses can be understood in detail and the thermal management system is described thoroughly. Two level-voltage source inverters are the main topology utilized in traction inverters for electrified vehicles and this is expected to remain true for the foreseeable future as a consequence of their reliability, efficiency, and low costs. Converting dc-current from battery pack to AC-current for EM operation is the responsibility of the traction inverter. This chapter detailed the topology along with the modulation schemes that facilitate the desired current manipulation. The operation of inverters comes with undesirable yet unavoidable losses. These losses take the form of heat, this heat must be estimated and dissipated as to ensure inverter components do not acquire temperatures beyond their limitations. If temperatures exceed the maximum value allowed for prolonged interval of time, semiconductor switches will get destroyed and the inverter will suffer failure. Power losses are the main topic of next chapter, it build on the concepts of this chapter.

Chapter 3

Power Losses in Two-Level Voltage Source Inverters

3.1 Introduction

Converting DC voltage into controllable AC waveforms results in higher undesired harmonics and generated heat. Inverters inadvertently convert electrical energy into heat commensurate to the inverter's instantaneous operating point. Cooling systems are entrusted with keeping semiconductors inside an operable temperature range by rapidly transmitting the generated heat to the ambient. Hence, accurately estimating the power losses provides a benchmark for the cooling system. Discussions are confined to IGBT based VSIs.

Losses in the semiconductors dominate power loss generated by the VSI. Said losses comprise both conduction and switching losses for IGBT devices and their FWD counterparts. Manufacturers provide datasheets that encompass, among other things, the conduction and switching characteristics of semiconductor devices. This

chapter aims to comprehensively explain how to utilize datasheets in estimating power losses for IGBT modules applied to motor drives.

3.2 Switch Operation

Without a brief explication of the behavior of semiconductors forming a switch featuring their different regions of operation, a review of estimating power loss remains lacking. Switches of IGBT-based VSI comprise of IGBT Transistors and their freewheeling diode counterparts. First, pondering the diode's operation then considering the IGBT transistor's behavior.

3.2.1 Diode Operation

Diodes are semiconductors that serve as electrical valves conducting current in one direction. They have two electrodes, an anode, and a cathode, as is made apparent by Figure 3.1.

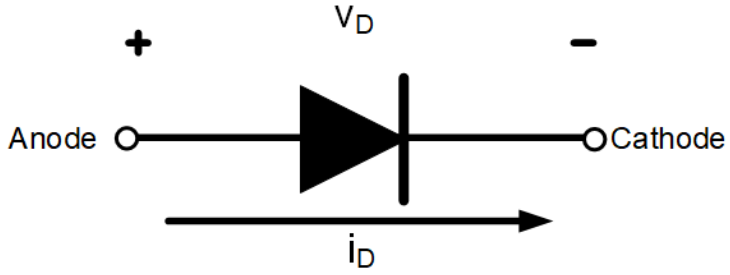


Figure 3.1: Representative circuit diagram symbol for Diodes

Outlining a diode's behavior, manufacturers supply a graphed asymmetric I/V characteristics of the diode, similar to Fig.3.2. Only the first quadrant is relevant in some applications, and other quadrants are not provided.

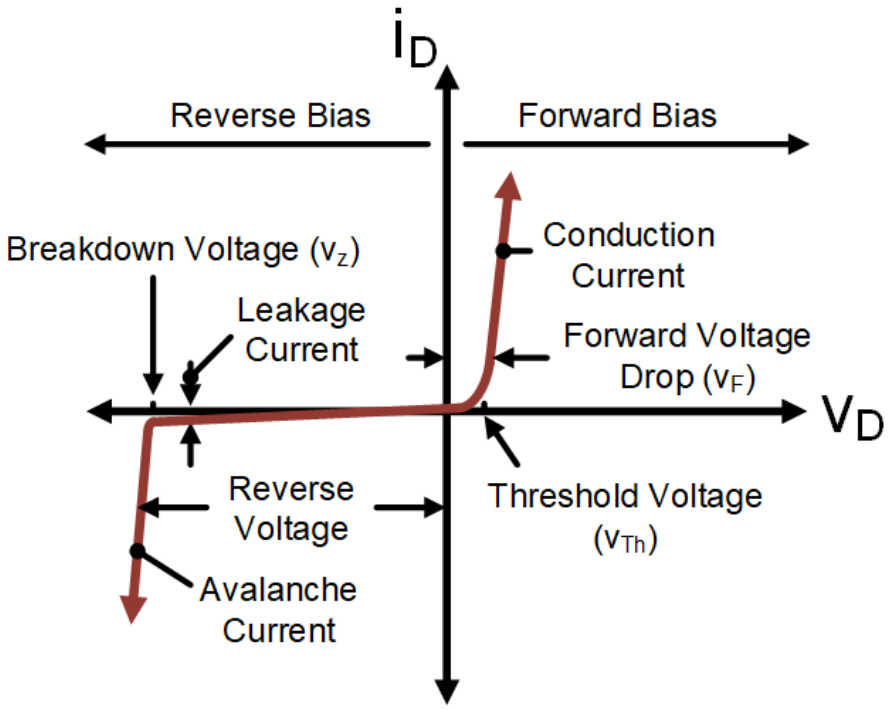


Figure 3.2: I/V Characteristics For a Diode portraying the different regions of operation

Referring to the illustrative I/V characteristic plot, two regions of operation for diodes arise, namely Forward Bias and Reverse Bias modes. The voltage across a diode, v_D, is the potential difference between the anode and cathode terminals. If voltage is positive, $v_D > 0$, diode operates in Forward Bias mode. Conversely, if voltage is negative, $v_D < 0$, diode is in Reverse Bias mode.

In reverse bias operation, diodes block applied reverse voltage while conducting leakage current. Leakage current is typically small enough to ignore, and here it is neglected. An application's operating conditions should never impose on a diode to block voltage beyond the breakdown voltage level, v_Z, to not incur Avalanche current. Diodes in reverse bias can be considered an open circuit. Consequently, diodes

in Reverse bias mode are assumed to have negligible power loss.

In contrast, while in forward bias mode, a diode begins conducting current when a voltage beyond the threshold voltage level is applied, $v_D > v_{D,Th}$. Above threshold voltage, the current flowing through the diode is commensurate to the applied voltage on the device. The relation between current and Forward Voltage Drop, $v_{D,FB}$, is conventionally approximated by a linearization of the curve intercepting Voltage axis, i.e., x-axis, at the threshold voltage with a slope $\frac{1}{R_D}$. Thereby, diodes in the forward bias mode may be modeled as a resistor in series with a voltage source. Forward

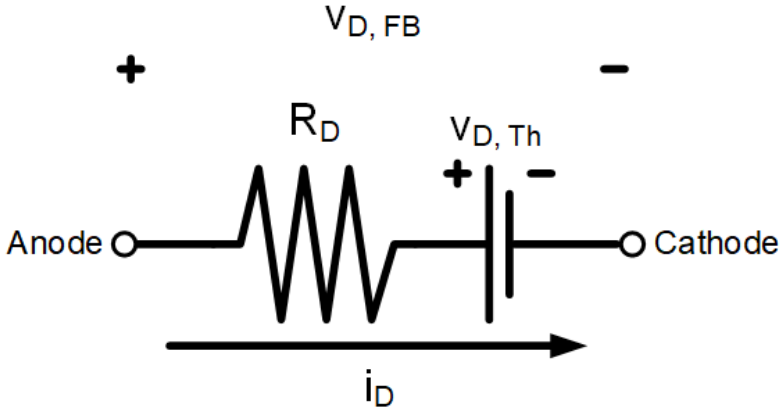


Figure 3.3: Diode Equivalent Circuit in Forward Biased Mode

voltage drop is then a function of a diode's flowing current,

$$v_{D,FB} = R_D\, i_D + v_{D,Th}. \tag{3.1}$$

3.2.2 IGBT Operation

IGBT's have three electrodes, namely the Gate, Emitter, and Collector as is accentuated in Fig.3.4. Acting like a voltage-controlled switch, voltages applied across

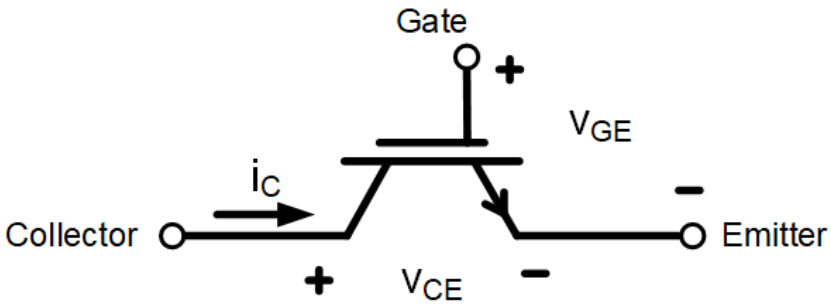


Figure 3.4: IGBT Circuit Diagram Symbol

collector-emitter (v_{CE}) and gate-emitter (v_{GE}) determine the amount of current flowing through IGBT, i.e., into collector node and out of emitter node (by convention). Furthermore, output Characteristics for an IGBT like the typical plot shown in Fig.3.5 are necessary when inspecting an IGBT's operation.

By examining the plot, it becomes evident that there are three modes of operation: Cut-off, Active, and Saturation (on-state) regions of operation.

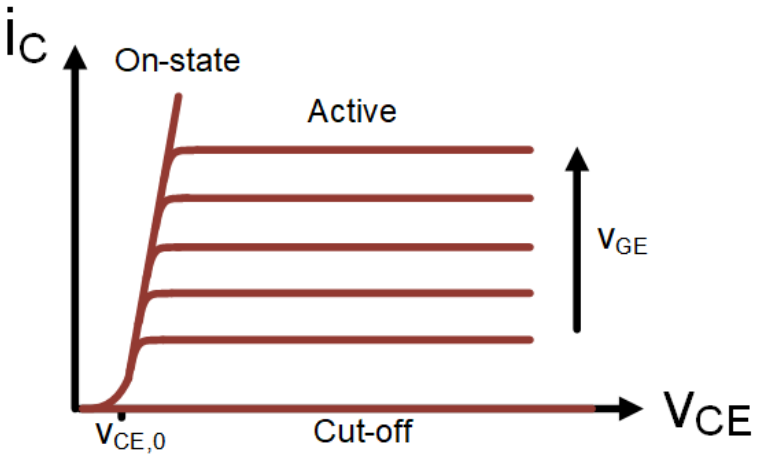


Figure 3.5: Typical Output Characteristics of IGBT

- Cut-off

When gate voltage (across gate-emitter terminals ,v_{GE}) is less than the threshold voltage level $v_{GE} < v_{GE,Th}$ IGBTs won't conduct any current $i_C = 0$.

- Active regime

  If the gate voltage is larger than the threshold level, i.e., $v_{GE} > v_{GE,Th}$, and the applied collector-emitter voltage is large concerning gate voltage, then IGBT behaves according to its active region characteristics. Collector-emitter voltage is specifically defined as large when $v_{CE} > v_{GE} - v_{GE,Th}$. Interestingly, the IGBT current traversing through can be controlled with gate voltage, while the collector-emitter voltage has no influence. In Figure 3.5 the association between collector current i_C, gate voltage v_{GE}, and collector-emitter voltage v_{CE} is given by horizontal lines, where collector current stays constant with changing collector-emitter voltage magnitudes but shifts up with higher gate voltage levels. In the active regime, a transfer characteristic plot can be more meaningful. Referring to the graph of Fig. 3.6, one can promptly discern some basic points. Below the threshold voltage level (i.e., in cut-off), there is no collector current. However, a further increase of gate voltage beyond threshold level makes the collector current rise practically linearly, explaining why the active region is also called the linear region. Indeed, it is standard to linearize the curve over the active region for simplicity. The associated slope gives the IGBT's transconductance, g_m. As such, the collector current is prescribed by

$$i_C = g_m \left(v_{GE}(t) - v_{GE,Th} \right). \tag{3.2}$$

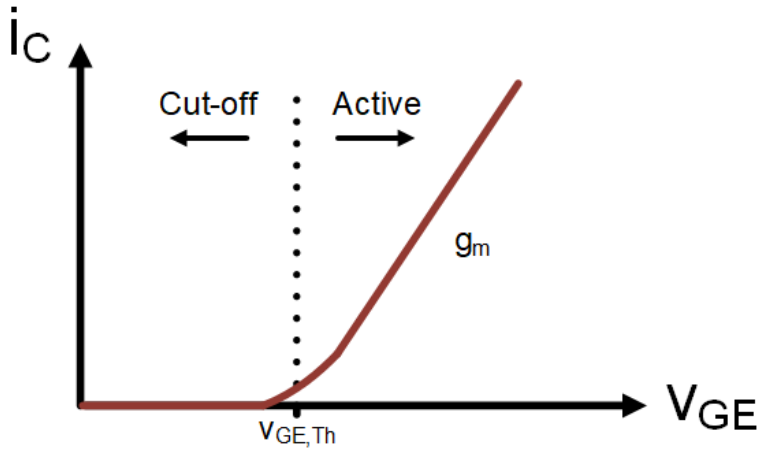


Figure 3.6: Typical Transfer Characteristics of IGBT depicting both the Active and Cut-off regions with the a Transconductance g_m

- Saturation Region (on-state)

  Similar to the active region, an IGBT must have a gate voltage larger than the threshold value $v_{GE} > v_{GE,Th}$. However, for the saturation regime to take effect, the collector-emitter voltage must be small. Precisely, collector-emitter voltage is said to be small, in this context, if $v_{CE} < v_{GE} - v_{GE,Th}$. An equivalent model, Figure 3.7, may be used to explicate IGBT's behavior. The model comprises a diode in series with a MOSFET in linear operation [22]. The diode in this model has a voltage drop of $v_{CE,0}$, and since MOSFET is in linear operation, it can be represented as a resistor R_I.

  The IGBT has a low on-state voltage, and the current limit is based on thermal considerations. The collector-emitter voltage across IGBT is described by

$$v_{CE}(t) = v_{CE,0} + i_c(t)R_I, \tag{3.3}$$

  where resistance R_I accounts for the linear, "Ohmic," dependence between i_c

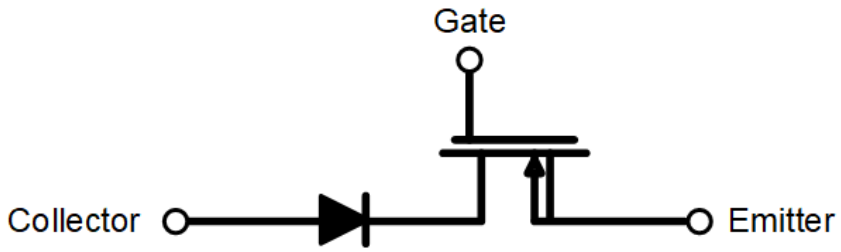


Figure 3.7: IGBT on-state equivalent model, includes a diode in series with a MOSFET in linear operation

and v_{CE}.

In the previous chapter, it was made clear that only the on-state and cut-off modes are utilized for traction inverters. There is negligible leakage current in cut-off mode, and power losses can be assumed zero. In contrast, the on-state mode has a large current but a tiny on-state voltage drop resulting in considerably low power losses. Although the active region can be controlled simply by adjusting gate voltage, which has practical implications, the high current and voltage make this mode undesirable, as mentioned in the previous chapter. Albeit the active mode is not used in static operations, it inevitably arises during dynamic switching.

3.3 Conduction Losses

Pertaining to the on-state of semiconductors, conduction losses contribute to total power losses and must be ascertained. Assuming SPWM is implemented to operate a 3-phase VSI, symmetry can simplify conduction analysis to a single phase current half cycle. Because switching frequency is much larger than output fundamental frequency, treating switching frequency as infinite is justifiable and has advantageous

implications. Deriving an elegant expression for conduction losses starts with considering a sing phase current,

$$i_a = \hat{i}\ sin(\omega\ t). \tag{3.4}$$

Over the positive half cycle when reference wave is larger than the carrier waveform high-side IGBT T_1 conducts, in contrast, if carrier is larger than reference waveform than low-side Diode conducts (refer to Chapter 1 for more thorough description). An infinite switching frequency implies that a switching event occurs at every infinitesimal point along the current waveform and that the current value remains constant for a switching period. Thereby, at every point along the waveform, a corresponding magnitude of current traverses through high-side IGBT for a time span $\tau(t)$ normalized to switching period , where

$$\tau_{IGBT}(t) = \frac{1}{2}\left[1 + m\ sin\left(\omega\ t + \phi\right)\right], \tag{3.5}$$

and for the remainder time of the normalized switching period the current passes through low-side Diode,

$$\tau_{Diode}(t) = \frac{1}{2}\left[1 - m\ sin\left(\omega\ t + \phi\right)\right] \tag{3.6}$$

[20, 22–26].

3.3.1 Diode Conduction Losses

Average conduction losses of diode over an output fundamental period is found by integrating instantaneous current through and voltage across a Diode over a half-period, as shown in eq. 3.7 [20, 22–26].. Where forward voltage drop was given in eq. 3.1 previously.

$$\begin{aligned} P_{cond,\,D} &= \frac{1}{2\,\pi}\int_0^{\pi}\left(R_D\; i_D(t) + v_{Th,D}\right)\; i_D(t)\; d\left(\omega t\right) \\ &= \frac{1}{2\,\pi}\int_0^{\pi}\left(R_D\; i_a(t) + v_{Th,D}\right)\; i_a(t)\; \tau_{Diode}\; d\left(\omega t\right) \\ &= \frac{1}{2}\left(v_{Th,D}\;\frac{\hat{i}_a}{\pi}\;+\;R_D\frac{\hat{i}_a^2}{4}\right)\;-m\;cos(\phi)\left(v_{Th,D}\;\frac{\hat{i}_a}{8}\;+R_D\frac{\hat{i}_a^2}{3\pi}\right) \end{aligned} \tag{3.7}$$

3.3.2 IGBT Conduction Losses

Average conduction losses for an IGBT is analogous to that of Diode. The forward voltage drop was given before eq. 3.3 and by employing same methodology the expressions can be derived to be

$$P_{cond,\,I} = \frac{1}{2}\left(v_{CE,0}\;\frac{\hat{i}_a}{\pi}\;+\;R_I\frac{\hat{i}_a^2}{4}\right)\;+m\;cos(\phi)\left(v_{CE,0}\;\frac{\hat{i}_a}{8}\;+R_I\frac{\hat{i}_a^2}{3\pi}\right). \tag{3.8}$$

In order to find the total on-state losses for a 3-phase VSI, expressions of conduction

loss for both IGBT and Diode (eq. 3.7 and eq. 3.8) which pertain to a fundamental half-period ought to be summed and multiplied by six,

$$P_{Total,\,cond} = 6\ \left(P_{cond,\,D}\ +\ P_{cond,\,I}\right). \tag{3.9}$$

3.4 Switching Losses

Estimating the switching losses is more complex than conduction losses. Switching energies, provided in datasheets, are required to calculate the switching losses. Manufacturers use empirical data extracted from a double pulse test (DPT) to obtain switching energies for turn on and turn off at a range of operating points. The subsequent subsection describes the double pulse test. Following the double pulse test, a brief explication of the switching phenomenons during turn on and turn off is explained. This description of switching phenomenons provides valuable insight into behavior within the internal structure of semiconductor devices and the interplay between different devices of VSI. Lastly, to end the section dealing with switching losses, the employment of switching energies in estimate switching losses is delineated.

3.4.1 Double Pulse Test

Energies pertaining to the turn on and turn off switching of an IGBT and diode are given in datasheets by manufacturers for specified applied current and DC-link voltage. Inside a half-bridge configuration, a semiconductor‘s behavior is impacted by the

operation of other semiconductor devices. This interplay is accounted for by manufacturers when they are obtaining the energies. A half-bridge setup employing an inductor load is used in a Double Pulse Test (DPT) to evaluate the switching energies experimentally. Only the switching energies of one IGBT switch and its complementary FWD is needed due to symmetry. A typical testing setup characterizing IGBT T_2 and Diode D_1 is depicted in Figure 3.8.

Since the DPT setup experimentally measures the switching energies of IGBT T_2 and FWD D_1, IGBT T_1 is forced to be off by gating signal, and D_1 happens to remain in blocking mode due to testing conditions. Because IGBT T_1 is always off, it will be discarded from the discussion on the DPT.

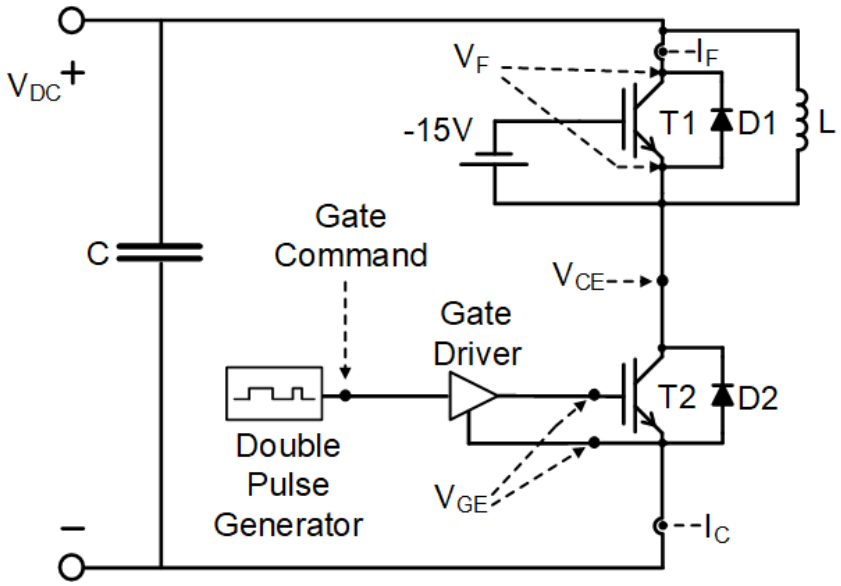


Figure 3.8: Double Pulse Testing Setup

In pursuit of obtaining the switching energies of diode D_1 and IGBT T_2 two pulses are applied as gating signals to IGBT T_2 triggering turn on and turn off for both IGBT

T_2 and diode D_1. A double pulse test can be divided into three intervals, as conveyed in Figure 3.9.

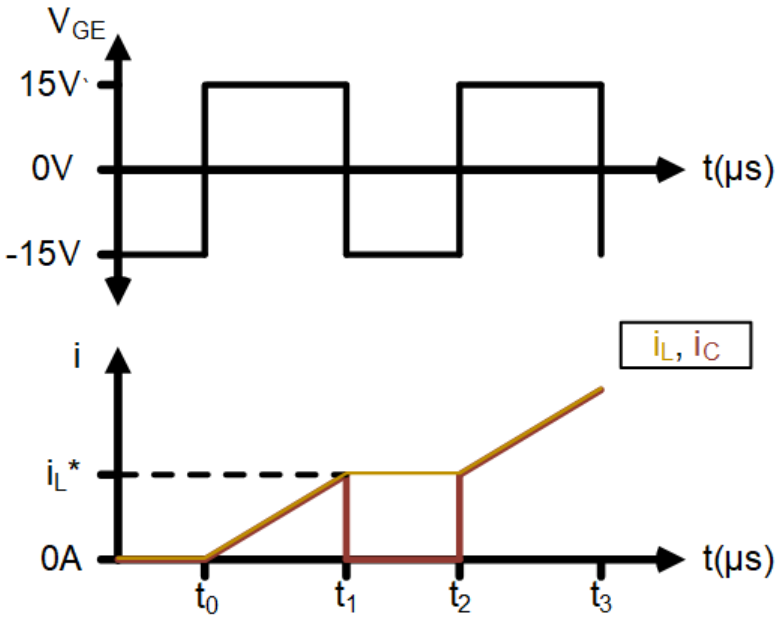


Figure 3.9: Double Pulse Testing Intervals defining turn on and turn off instants

- Interval i (spanning from t_0 to t_1)

  IGBT T_2 is turned on for a time span of Δt_1, i.e. $t_1 - t_0$. For a given DC-link voltage and load inductance, the time period Δt_1 is calculated to generate desired load current (i_L) for both turn on and turn off. Load current's dependence on the load inductance, DC-link voltage, and the time elapsed is encapsulated by

$$i_L(t) = \frac{v_{DC}\,\Delta t_1}{L}. \tag{3.10}$$

  The current flows from DC-link into the load and IGBT T_2 as shown in Figure 3.10.

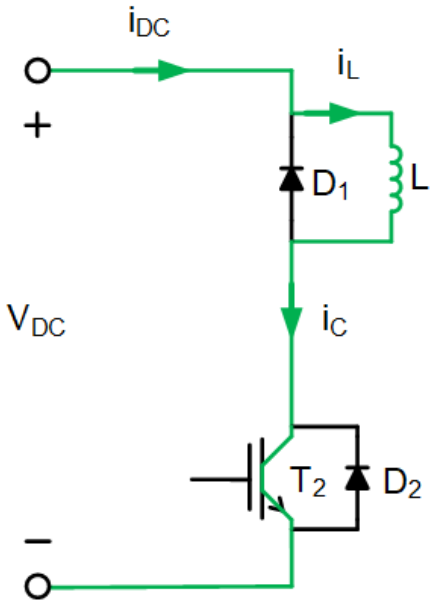


Figure 3.10: Interval i of Double Pulse Test in static operation ($t_0 < t < t_1$)

- Interval ii (spanning from t_1 to t_2)

  At t_1, IGBT T_2 is turned off for a time period ending at t_2. The gate-driver sends a gating signal instructing IGBT T_2 to turn off, i.e. at t_1, initiating the dynamic transition where the load current commutates from entirely flowing through the IGBT T_2 to free-wheeling via complementary diode D_1. Moreover, the turn off interval for the IGBT T_2 inducing a negative voltage on the inductive load turning diode D_1 on. This transient dynamic behavior initiated at t_1 simultaneously constitutes the turn off and turn on intervals where the energies are estimated for IGBT T_2 and diode D_1, respectively. As previously explained, interval i produces a desired current, this means that the switching transitions used to evaluate the switching energies ,turn on and turn off of IGBT T_2 and diode D_1 respectively, are with respect to this current.

When IGBT T_2 is completely off due to the short time span and low parasitic resistance of commutation path a constant current circulates entirely between the free-wheeling diode D_1 and the load as conveyed in Figure 3.11 and Eq. 3.10.

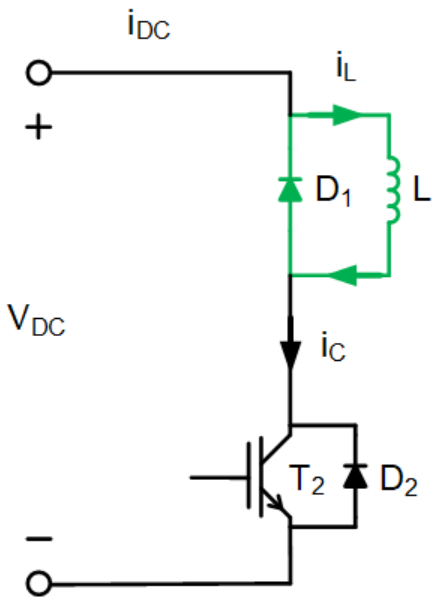


Figure 3.11: Interval ii of Double Pulse Test in static operation ($t_1 < t < t_2$)

- Interval iii (spanning from t_2 to t_3)

  Prior to t_2 the current generated in interval i constantly circulates between the diode D_1 and load. At t_2 another positive gating signal is applied turning IGBT T_2 on and diode D_1 off. A current commutation does not occur instantaneously. Instead, the current flowing through the diode D_1 drops off, and the collector current correspondingly rises. These transient behaviors constitute the turn-off and turn-on periods of diode D_1 and IGBT T_2, respectively, where the energies are calculated. After the diode is completely off and the IGBT T_2 is on, the load current traverses entirely through IGBT T_2, that is, no current flows through

diode D1; this is visually shown in Figure 3.12. Load current resumes rising at the same rate as interval i until t_3,

$$i_L(t) = \frac{v_{DC}\ (\Delta t_1 + t - t_3)}{L}. \tag{3.11}$$

This interval establishes the end of a double pulse test for a given dc-link voltage and collector current.

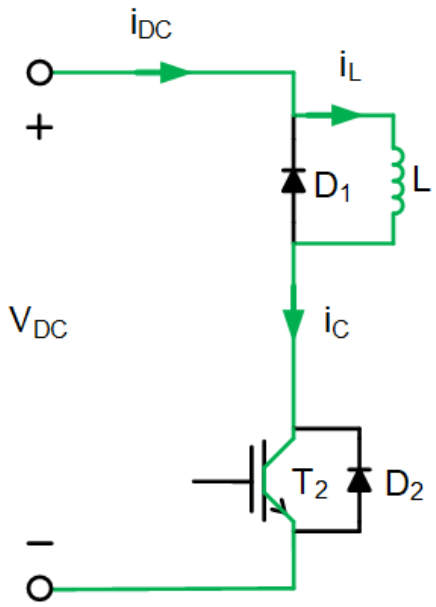


Figure 3.12: Interval iii of Double Pulse Test in static operation ($t_2 < t < t_3$)

To recap, listed below are main points to take from DPT:

- Tester applies desired DC-link voltage
- By selecting inductance of load and time duration in interval i ,i.e., Δt_1, tester can apply desired load current for switching
- time $t = t_1$ is when turn off of IGBT T_2 and turn on of complementary FWD

D_1 is initiated

- time $t = t_2$ is when turn on of IGBT T_2 and turn off of complementary FWD D_1 is initiated

Basically, in a DPT, switching for both an IGBT and a complementary Diode are induced at controllable load current and selectable DC-link voltage.

3.4.2 Dynamic Switching Behavior

At present, dynamic characteristics during switching instants are explicated, encapsulating the complex interplay between an IGBT and its complementary FWD. Figure 3.13 is employed to better elucidate the switching phenomenon. This section is based off of [24].

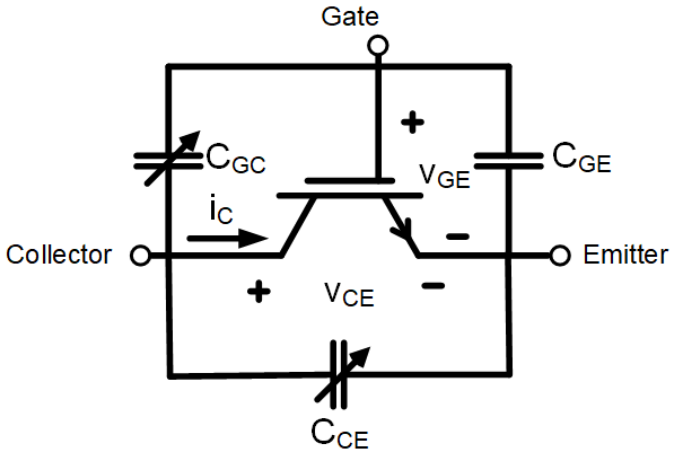


Figure 3.13: Equivalent circuit of the IGBT during switching

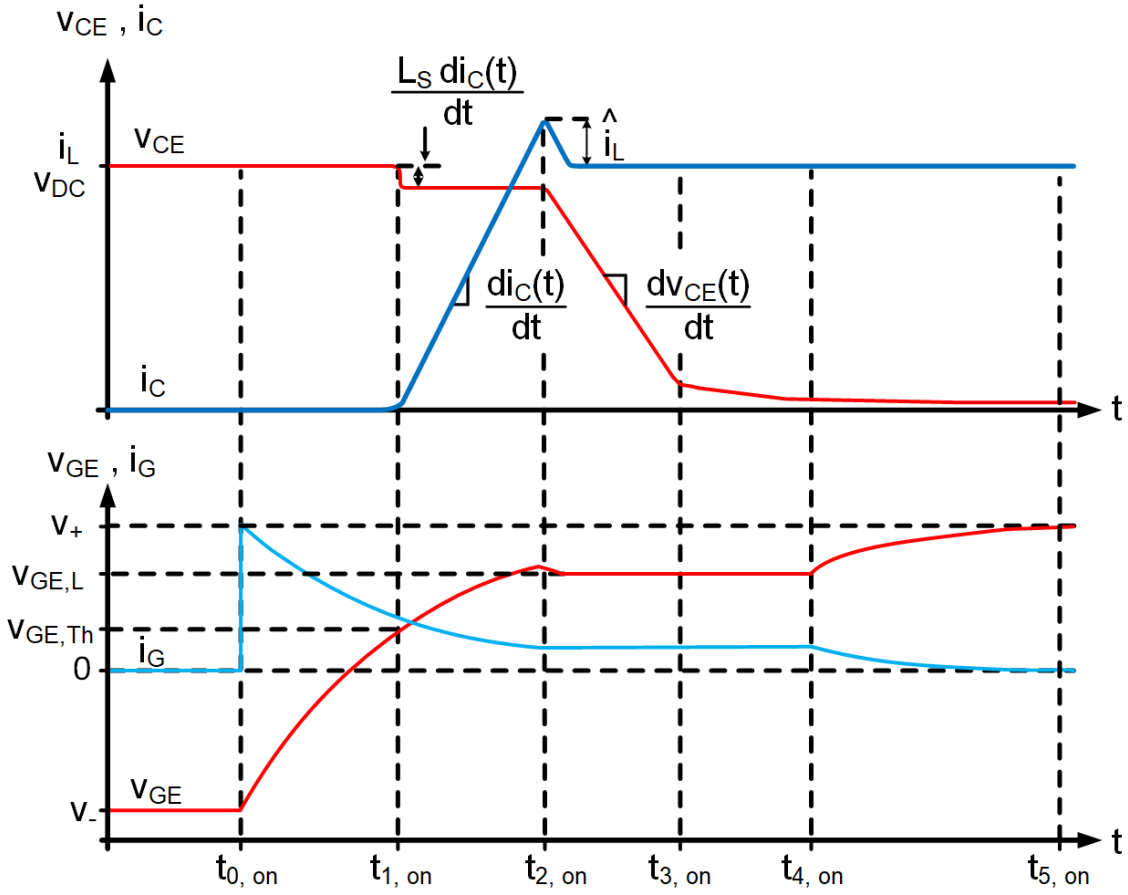


Figure 3.14: Switching Waveform of IGBT T_2 Turn ON [24]

Turn ON of IGBT and Turn OFF of FWD

To start, load current flows through FWD D_1 and IGBT T_2 blocks DC-link voltage. Turn on of IGBT is characterized as the transition where the load current is made to conduct through IGBT as opposed to Diode, and the Diode blocks DC-link voltage instead of IGBT, as suggested by Figure 3.14. Further, turn on can be partitioned into six intervals as is enumerated next.

1: OFF state ($t < t_{0,on}$)

Prior to $t_{0,on}$, IGBT T_2 is assumed to be blocking entire DC-link voltage, $v_{CE} = V_{DC}$, with no collector current conduction $i_c = 0$, in turn, load current traverses through complementary FWD D_1 only. Mind you, load current is controllable and defined by, $i_L = \frac{V_{DC}\,\Delta t_1}{L}$ (From DPT section). Deemed unsubstantial both leakage current of IGBT T_2 and forward voltage drop of FWD D_1 are not considered here. Capacitor C_{GE} has discharged completely, gaining constant negative voltage v_- applied by gate-driver so $v_{GE} = v_-$ and $i_G = 0$.

Keeping in mind established conditions, the moment $t = t_{0,on}$ gate-driver applies a constant positive voltage v_+ commencing IGBT T_2's turn on.

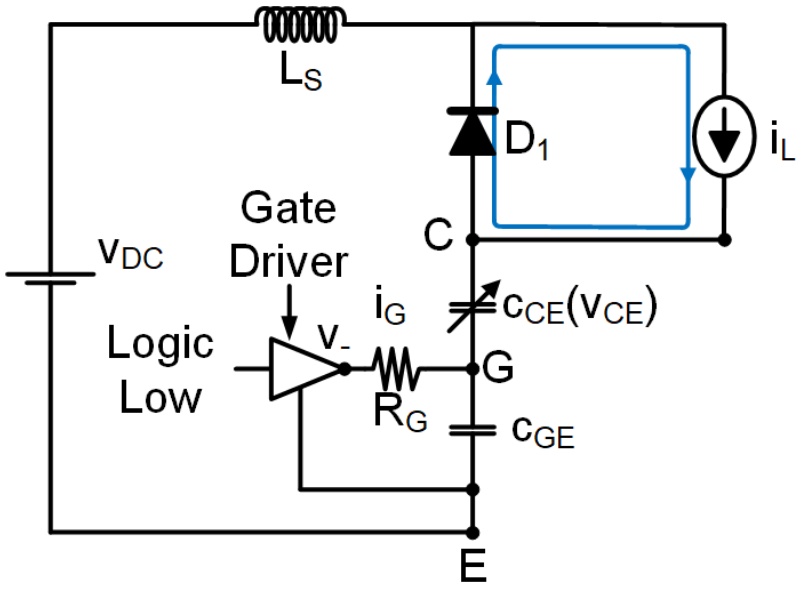


Figure 3.15: Interval 1 of turn on: ($t < t_{0,on}$) of equivalent circuit with current commutation path [24]

2: Rising Gate Voltage To Threshold Voltage ($t_{0,on} < t_{1,on}$)

By virtue of a resistive gate-driver applying voltage v_+, the Gate capacitor C_{GE} charges up while Miller capacitor C_{GC} is discharged. Miller capacitor discharges because the collector node is clamped to the upper DC-link rail as complementary FWD D_1 still conducts. Like in interval 1, FWD D_1 bears full burden of load current and IGBT T_1 blocks full DC-link voltage as long as gate voltage is below threshold value $v_{GE,Th}$ or equivalently IGBT is in cutoff mode. Here the Gate-Emitter voltage rise is dependent on the Gate-Emitter capacitance and gate-driver's resistance,

$$v_{GE}(t) = v_- + (v_+ - v_-)\left[1 - e^{-\frac{\left(t-t_{0,on}\right)}{\tau_G}}\right], \tag{3.12}$$

where the time constant of input capacitance $C_{ies} = C_{GE} + C_{GC}$ charging is defined below,

$$\tau_{G1} = R_G\left(C_{GE} + C_{GC}\right) \tag{3.13}$$

Recognizing the Miller capacitance as a function of v_{CE} where high collector-emitter voltage values correlate to a small Miller capacitance explains why Gate-Emitter voltage is not influenced significantly by it. Where the time constant of input capacitance $C_{ies} = C_{GE} + C_{GC}$ charging is defined below,

$$\tau_{G1} \approx R_G\left(C_{GE}\right) \tag{3.14}$$

Gate current is what charges the input capacitors, it begins with its highest value

then decays as the capacitors charges,

$$i_G(t) = \frac{v_+ - v_{GE}(t)}{R_G} = \frac{v_+ - v_-}{R_G}\left[e^{-\frac{(t-t_{0,on})}{\tau_G}}\right]. \tag{3.15}$$

As soon as v_{GE} reaches $v_{GE,Th}$, IGBT becomes in active mode of operation. Hence, t_1, on is defined as the moment gate voltage gains threshold value, $v_{GE}(t_1, on) = v_{GE,Th}$.

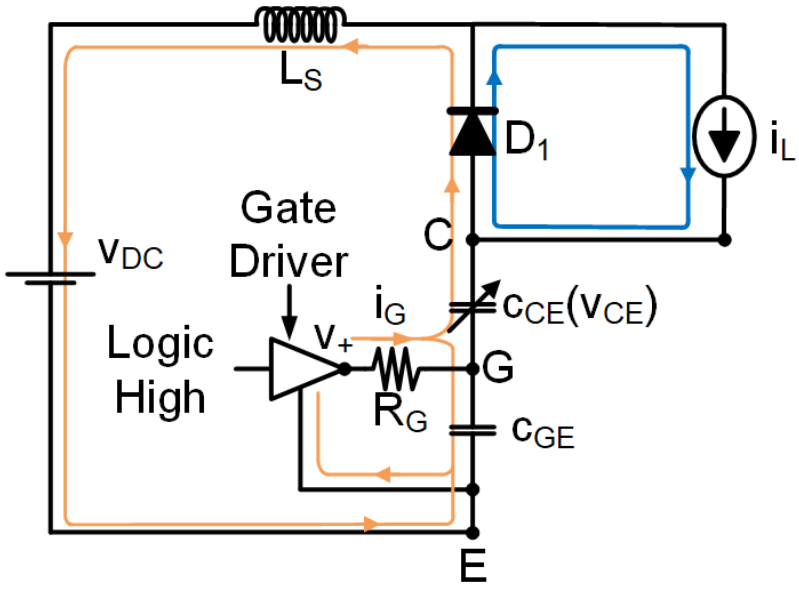


Figure 3.16: Interval 2 of turn on: $(t_{0,on} < t < t_{1,on})$ of equivalent circuit with current commutation path [24]

3: Current Rise ($t_{1,on} < t < t_{2,on}$)

Gate voltage and current continue to rise and decay, respectively, with the same precedented rate and behavior described in interval II. Here, distinguishably, the gate voltage v_{GE} has surpassed threshold value $v_{GE} > v_{GE,Th}$ in conjunction with v_{CE}

remaining greater than $v_{GE} - v_{GE,Th}$, IGBT becomes governed by transfer characteristics related to active region operation. Ergo, the collector current is delineated as

$$i_C(t) = g_{m,s}(v_{GE}(t) \; - \; v_{GE,Th}), \tag{3.16}$$

and $g_{m,s}$ denotes IGBT's linearized transconductance.

Persisting inside active region of operation collector current $i_c(t)$ is controlled by instantaneous gate voltage $v_{GE}(t)$, which is rising. Moreover, the rise of collector current, found by differentiating eq.3.16, is portrayed as

$$\frac{d\, i_C(t)}{dt} \; = \; g_{m,s} \, \frac{d\, v_{GE}(t)}{dt} \tag{3.17}$$

$$= \; g_{m,s} \, i_G(t) \, C_{ies} \tag{3.18}$$

$$\approx \; g_{m,s} \, i_G(t) \, C_{GE}. \tag{3.19}$$

To compensate, complementary FWD D_1 current decreases at an equivalent rate

$$\frac{d\, i_D(t)}{dt} \; = \; -\frac{d\, i_C(t)}{dt}. \tag{3.20}$$

Basically because collector current i_C rises while complimentary FWD current i_D falls, a transition is realized where load current i_L starts flowing through IGBT T_2 instead of free-wheeling across Diode D_1.

FWD D_1 never acquires voltage blocking capabilities during this interval, and collector potential is still clamped to the upper DC-link rail. Additionally, parasitic

inductance within the commutation loop and the rising collector current impresses a voltage drop across inductance. Since inductance exhibits a voltage drop, IGBT blocks a reduced voltage,

$$v_{CE} \;=\; v_{DC} - \; L_S \; \frac{d\, i_C(t)}{dt}. \tag{3.21}$$

The end of this interval at $t = t_{1A,on}$, is when collector current equates to load current $i_C(t_{1A,on}) = i_L$.

Rearranging eq. 3.16 and equating collector current to load current, $i_C = i_L$, gate voltage is found to be;

$$v_{GE,L} \;=\; v_{GE,Th} \;+\; \frac{i_L}{g_{m,s}}. \tag{3.22}$$

4: Reverse Recovery Effect ($t_{2,on} < t < t_{3,on}$)

When IGBT T_2 collector current builds up to carry full load current (at $t = t_{2,on}$), FWD D_1 cannot yet block voltage until internally stored charge carriers (Q_{rr}) are dispensed with. FWD D_1 elicits the removal of its charge carriers by conducting a negative current. This phenomenon in Diodes is called Reverse Recovery Effect and dominates the Diode switching losses. Collector current now consists of both reverse recovery current and load current. For simplicity, the Reverse Recovery current is estimated to take the symmetric triangular shape as portrayed by Fig. 3.18. Implying that collector current continues rising reaching a cap at the peak of the reverse recovery current $\hat{i}_{rr}$, that is $i_c = i_L + \hat{i}_{rr}$. Diode finally becomes able to block voltage at

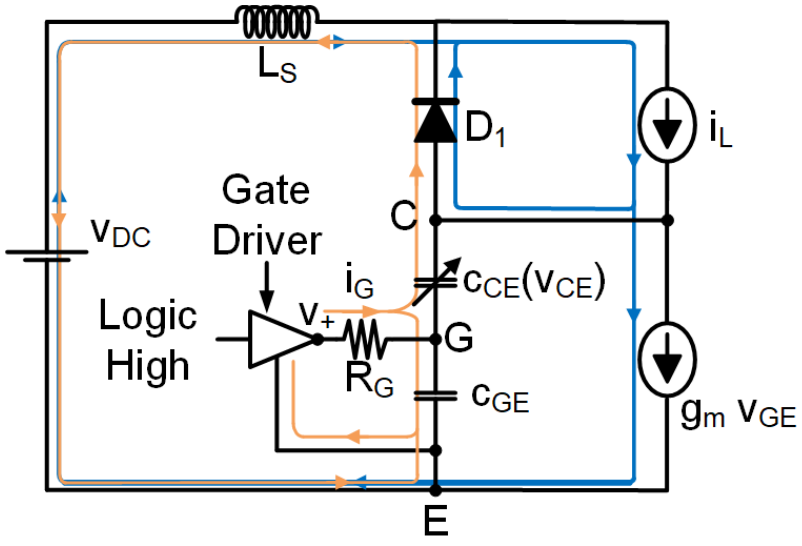


Figure 3.17: Interval 3 of turn on: ($t_{1,on} < t < t_{2,on}$) of equivalent circuit with current commutation path [24]

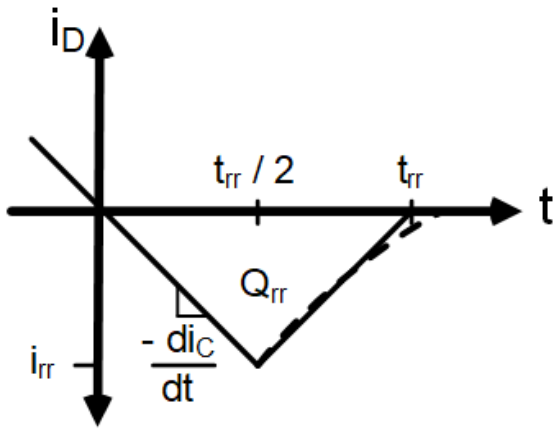


Figure 3.18: Reverse Recovery Current that ejects stored charges in diode allowing for blocking

this maximum collector current magnitude. Thereby, collector potential is no longer clamped to the upper DC-link rail permitting the voltage across IGBT v_{CE} to start falling. Completing the discharge of Diode's charge carriers, collector current returns to conducting load current exclusively, i.e. at $t = t_{3,on}$.

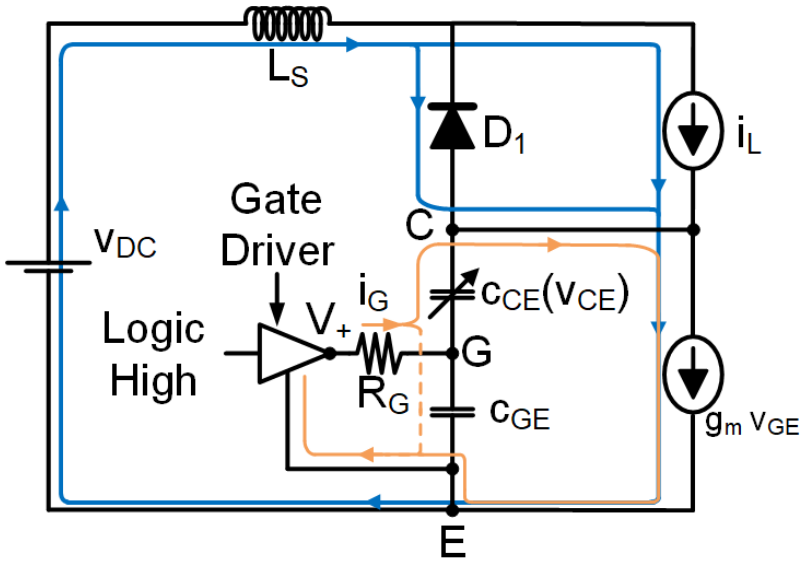


Figure 3.19: Interval 4 of turn on: ($t_{2,on} < t < t_{3,on}$) of equivalent circuit with current commutation path [24]

5: IGBT Voltage Decay ($t_{3,on} < t < t_{4,on}$)

Recall that when $v_{GE}(t) > v_{GE,Th}$ and $v_{CE}(t) \geq v_{GE,Th} + v_{GE}(t)$, IGBT is confined to behave according to transfer behavior of active region operation. Ergo, since v_{CE} is still high during this interval, remaining in active region, and because of having a constant load current traversing via IGBT, prescribed by application, the gate voltage v_{GE} is clamped to $v_{GE,L}$ of eq. 3.22. This constant Gate voltage level is denominated as Miller Plateau. Employing a resistive gate-driver a constant Gate current,

$$i_G = \frac{v_+ - v_{GE,L}}{R_G}, \tag{3.23}$$

discharges Miller capacitor and consequently decays voltage v_{CE},

$$\frac{dv_{CE}(t)}{dt} = -\frac{dv_{GC}(t)}{dt} = -\frac{i_G}{C_{GC}}. \tag{3.24}$$

Miller capacitance is highly dependent on v_{CE}; the capacitance increases abruptly when the collector-emitter voltage decreases in the proximity of Gate voltage value $v_{GE,L}$. In turn, as v_{CE} approaches the vicinity of Gate voltage, i.e., at $t = t_{4,on}$, the drastically increased Miller capacitance will slow down the decay of v_{CE} significantly as can be inferred by eq. 3.24.

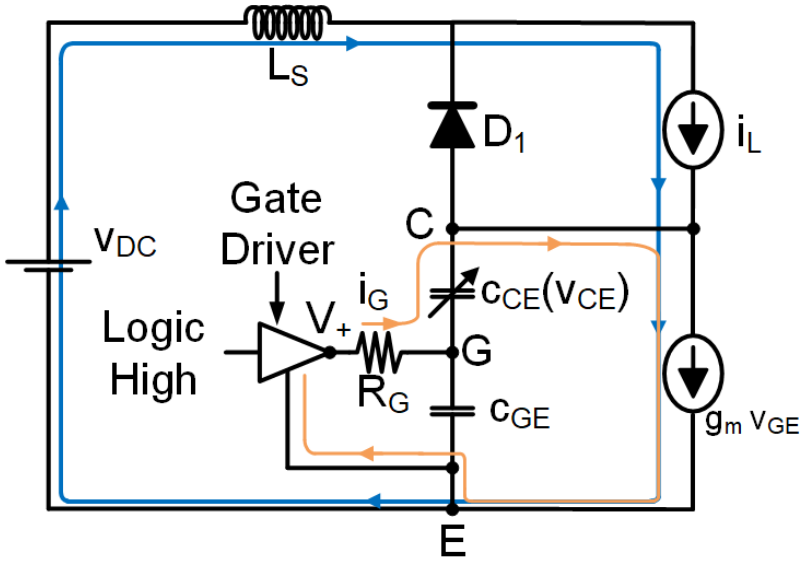


Figure 3.20: Interval 5 of turn on: ($t_{3,on} < t < t_{4,on}$) of equivalent circuit with current commutation path [24]

6: Rising Gate Charge ($t_{4,on} < t < t_{5,on}$)

As collector-emitter voltage v_{CE} decays, be it at a slow rate, it becomes smaller than $v_{GE,L}$–$v_{GE,Th}$, i.e. at $t = t_{4,on}$, transitioning IGBT into the saturation region. When in Saturation region, Gate voltage becomes non-clamped allowing Gate capacitor to

charge again. Like interval 2, Gate voltage can be expressed as

$$v_{GE}(t) = v_{GE,L} + [v_{+} - v_{GE,L}]\left(1 - e^{-\frac{(t-t_{4,on})}{\tau_G}}\right). \tag{3.25}$$

Notice, the R-C circuit charging can be assumed to start with initial voltage of $v_{GE,L}$ at time $t = t_{4,on}$. Time constant is also larger due to v_{CE} dependent Miller Capacitor being much larger in this interval with respect to Interval 2,

$$\tau_G = R_G\left(C_{GC} + C_{GE}\right). \tag{3.26}$$

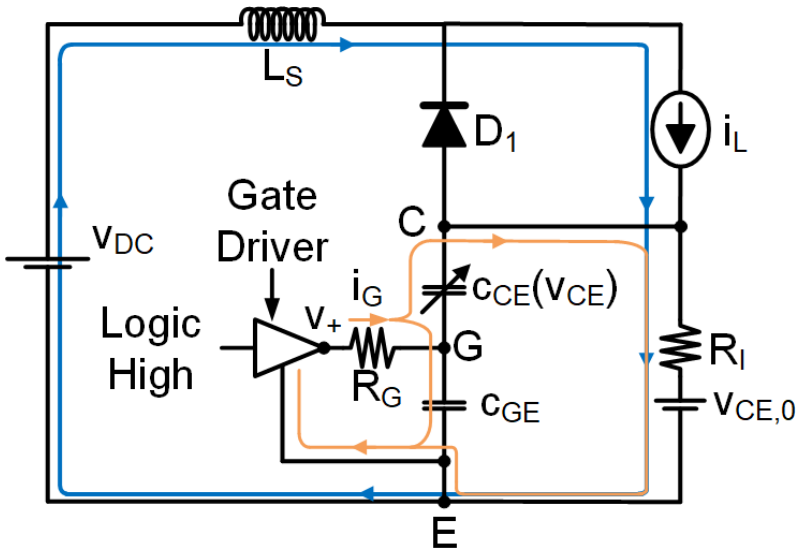


Figure 3.21: Interval 6 of turn on: $(t_{4,on} < t < t_{5,on})$ of equivalent circuit with current commutation path [24]

In conclusion, the gate voltage rises until v_{+}, at $t = t_{5,on}$, at a rate slower than in

interval 2. IGBT becomes characterized with a low forward voltage drop corresponding to an on-state value and a collector current equating to the entire load current; meanwhile, complementary FWD D_1 blocks the entire DC-link voltage.

Turn OFF of IGBT and Turn ON of Diode

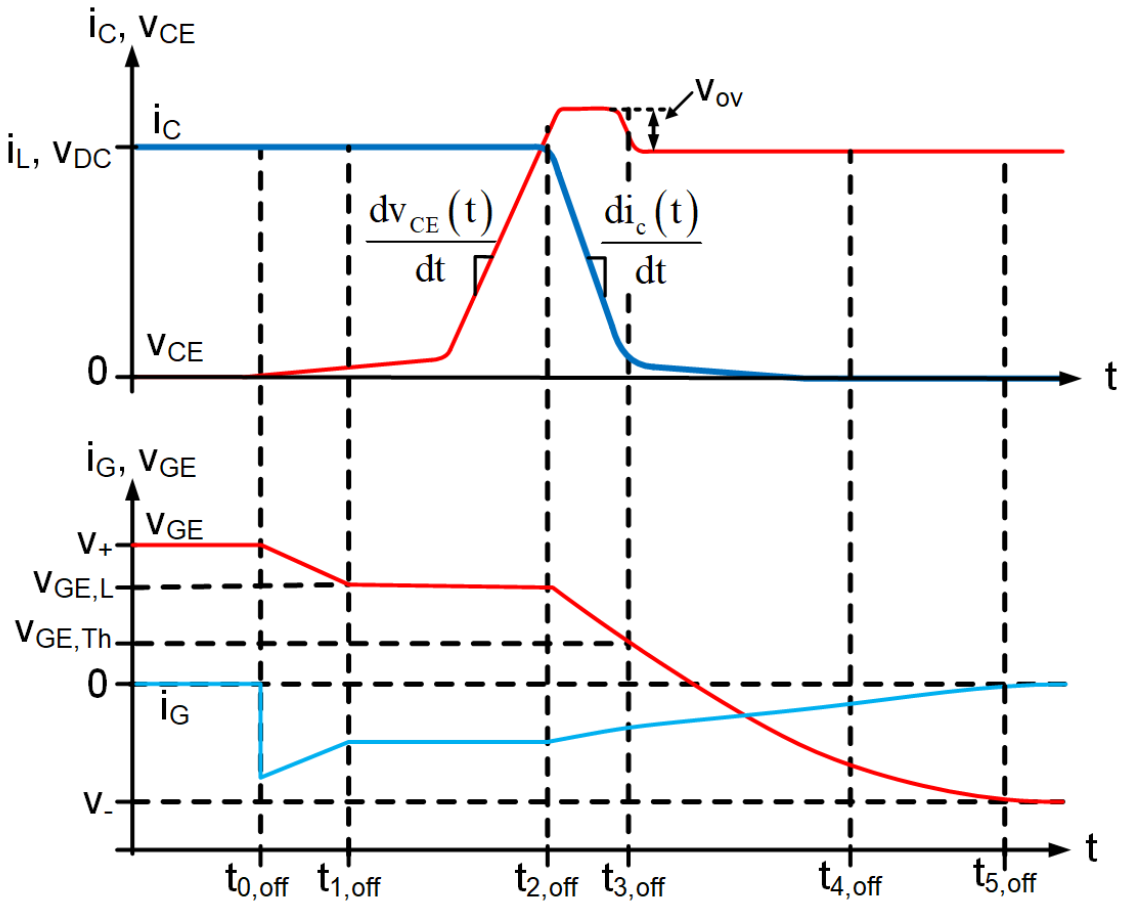


Figure 3.22: Switching Waveforms when IGBT T_2 is turned off [24]

Firstly, current traverses via IGBT, and complementary FWD blocks the DC-link voltage. Turn off of IGBT is characterized as the transition that makes current flow through FWD instead of the IGBT and has IGBT block DC-link voltage instead of

FWD. Turn off like turn on can be described with an equivalent circuit diagram. The dynamic behavior can be divided into six sections, as discussed below.

1: ON-State ($t < t_{0,off}$)

Assuming IGBT T_2 is turned-on, i.e. in Saturation operation, load current passes through IGBT impressing low on-state voltage $v_{CE} = v_{CE\,Sat,\,i_C=i_L}$, while FWD D_1 blocks the whole DC-link voltage $v_{D1} = v_{DC}$ with negligible leakage current flowing through it. Regarding IGBT T_2 Gating circuitry, it is assumed that Gate voltage has set to pre-applied gate-driver's output voltage level $v_{GE} = v_+$, correspondingly no charging or discharging takes place $i_G = 0$. At $t = t_{0,off}$ a negative voltage v_- is applied by gate-driver, triggering the IGBT's turn-off. Although the gate-driver applying a low voltage would be sufficient (e.g., $0V$), a negative voltage value is used to mitigate the likelihood of parasitic turn-on and the entailed shoot-through current.

2: Gate Discharge Delay ($t_{0,off} < t < t_{1,off}$)

Applied gate-driver voltage v_- commences the discharge of input capacitors $C_{ies} = C_{GC} + C_{GE}$, leading to the Gate voltage decaying,

$$v_{GE}(t) = v_+ - (v_+ - v_-)\left[1 - e^{\frac{-(t - t_{0,off})}{\tau_{G,L}}}\right]. \tag{3.27}$$

Associated Gate current is negative and monotonically reduces in magnitude,

$$i_G(t) = \frac{v_- - v_{GE}(t)}{R_G} = \frac{v_- - v_+}{R_G} e^{\frac{-(t - t_{0,off})}{\tau_{G,L}}}. \tag{3.28}$$

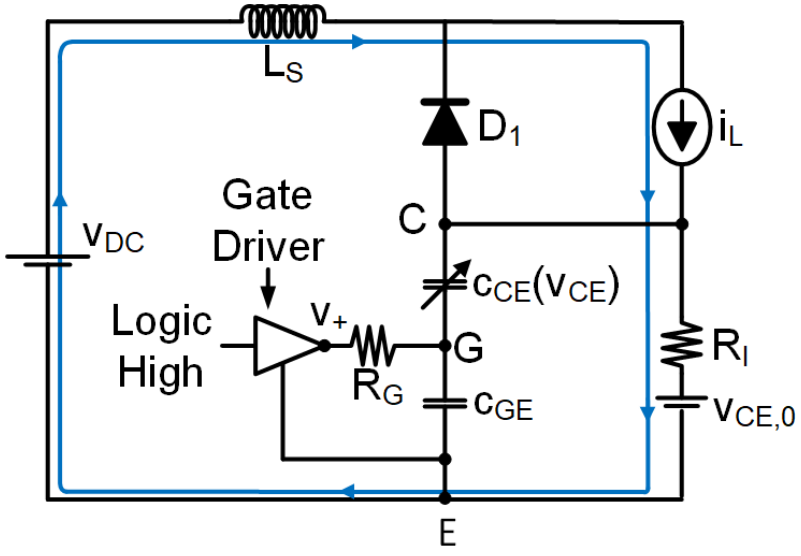


Figure 3.23: Interval 1 of turn off: $(t < t_{0,off})$ of equivalent circuit with current commutation path [24]

This interval is concerned with discharging of Gate capacitor and charging of Miller capacitor to the point where IGBT falls into Active region, i.e. at $t = t_{1,off}$. Moreover, Gate capacitor is discharged leading to a Gate voltage decay, when Gate voltage arrives at minimum value with respect to its collector current $v_{GE,\,L}$ it reaches active region of operation.

3: Rising Voltage $(t_{1,off} < t < t_{2,off})$

Since at $t = t_{1,off}$ IGBT is in Active region having constant load current pass through, Gate voltage becomes clamped as $v_{GE} = v_{GE,L}$. Owing to the small collector-emitter voltage, Miller capacitor exhibits large capacitance and gets charged slowly by Gate current. Charging of Miller capacitor makes IGBT's collector-emitter voltage rise,

$$\frac{dv_{CE}(t)}{dt} = -\frac{dv_{GC}(t)}{dt}, \tag{3.29}$$

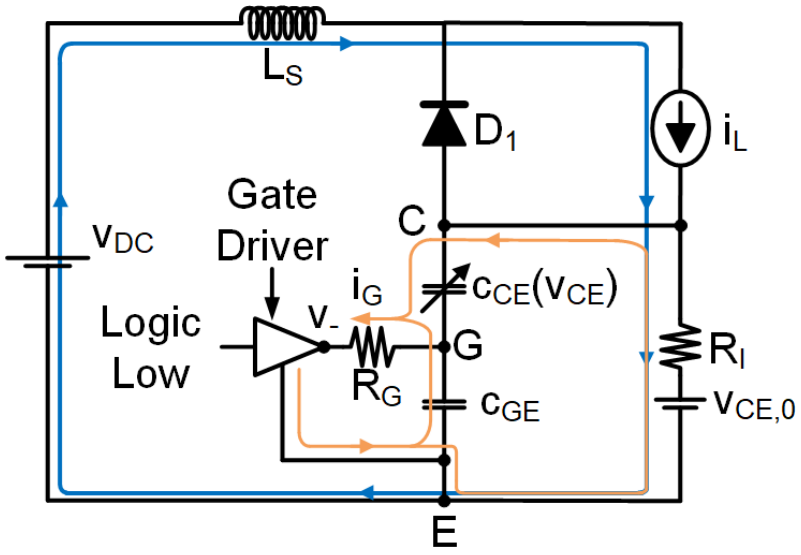


Figure 3.24: Interval 2 of turn off: ($t_{0,off} < t < t_{1,off}$) of equivalent circuit with current commutation path [24]

where $v_{GC}(t)$ is decaying.

Rising slowly the collector-emitter voltage surpasses the Gate voltage level resulting in a sharp decrease of Miller capacitance. With a relatively small capacitance the Miller capacitor begins charging faster raising collector-emitter voltage even quicker. The end of this interval is characterized by collector-emitter voltage reaching DC-link voltage, $v_{CE} = v_{DC}$.

4: IGBT Current Decays ($t_{2,off} < t < t_{3,off}$)

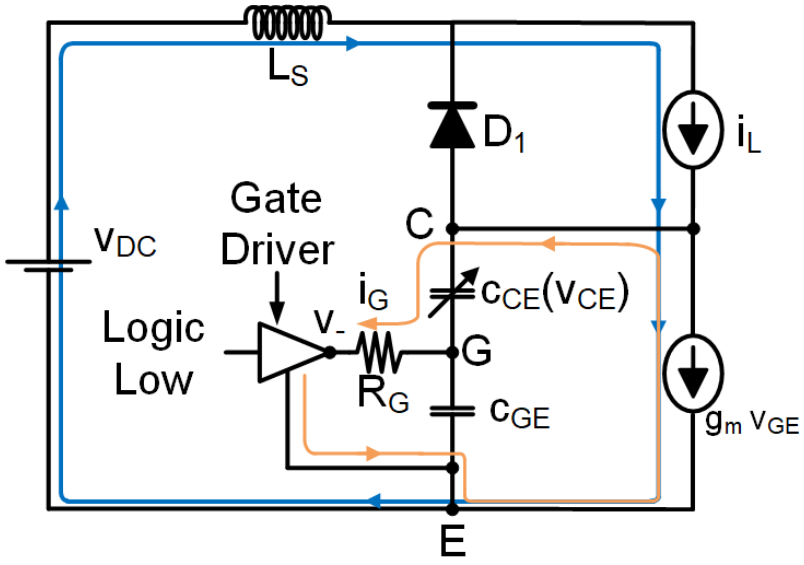


Figure 3.25: Interval 3 of turn off: ($t_{1,off} < t < t_{2,off}$) of equivalent circuit with current commutation path [24]

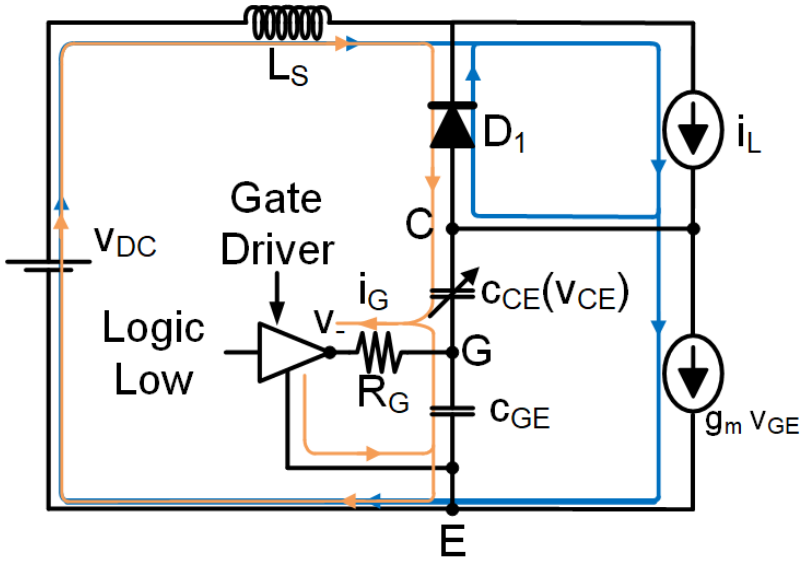


Figure 3.26: Interval 4 of turn off: ($t_{2,off} < t < t_{3,off}$) of equivalent circuit with current commutation path [24]

Gaining a voltage drop equivalent to DC-link voltage value across IGBT, $v_{CE} =$

v_{DC}, complementary FWD D_1 becomes able to conduct current. Current flowing through Diode can be characterized as

$$i_D = i_L – i_C, \tag{3.30}$$

conveying that the diode shares the load current. No longer is there a restriction on collector current releasing the clamping of IGBT Gate voltage. Gate current i_G resumes discharging Gate capacitor C_{GE} causing Gate voltage to fall again, picking up where it left off $v_{GE,L}$.

$$v_{GE}(t) \;=\; v_{GE,L} – (v_{GE,L} - v_{–}) \left[1 – e^{\dfrac{-(t-t_3)}{\tau_{G,S}}} \right] \tag{3.31}$$

The active region of IGBT defines the collector current in terms of the instantaneous Gate voltage,

$$i_C(t) = g_{M,S} \left(v_{GE}(t) - v_{GE,Th} \right). \tag{3.32}$$

Additionally, having a forward biased mode FWD D_1 implies that collector node's potential is clamped to that of upper DC-link rail. Decaying collector current induces a voltage across parasitic inductance of commutation path, it follows that IGBT must block a voltage larger than DC-link voltage,

$$v_{CE}(t) = v_{DC} - L_s \frac{di_C(t)}{dt}, \tag{3.33}$$

where the second term is positive because of decaying collector current. Notice this voltage spike is what makes the stray inductance in commutation loop important to

minimize and why IGBT modules are conventionally selected to withstand 1.5 to 2 times the DC-link voltage.

5: Tail Current $(t_{3,off} < t < t_{4,off})$

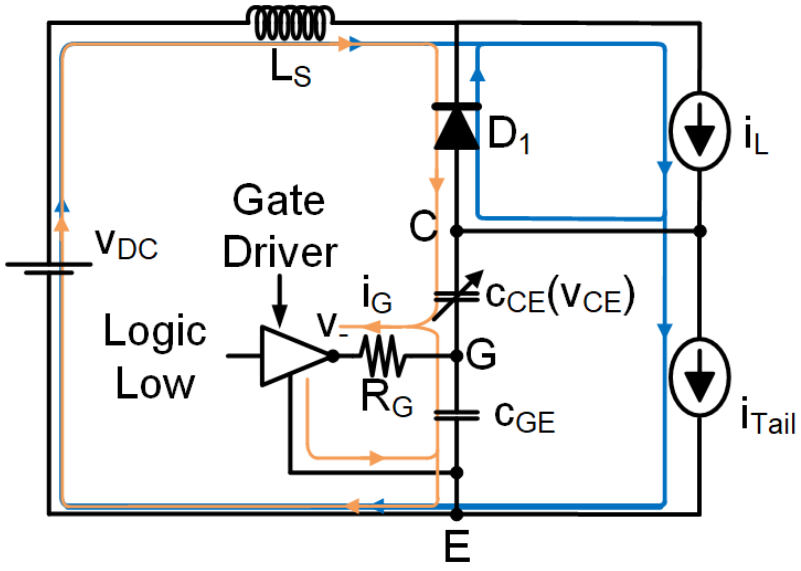


Figure 3.27: Interval 5 of turn off: $(t_{3,off} < t < t_{4,off})$ of equivalent circuit with current commutation path [24]

Both Gate voltage and collector current are decreasing. When collector current arrives at the Tail current level,i.e., $t = t_{3,off}$, it no longer is controlled by the gate-driver's circuit. Both the applied DC-link voltage and the recombination process play their parts to remove charge carriers inside IGBT. Nevertheless, at $t = t_{4,off}$ tail current has become negligible.

6: Gate Capacitor Discharge $(t_{4,off} < t < t_{5,off})$

Gate voltage continues to discharge until the gate voltage sets to the gate-driver's output voltage v_{-}. Here the current is officially flowing through FWD D_1 and the IGBT is blocking DC-link voltage. Also the gate current is zero $i_G = 0$.

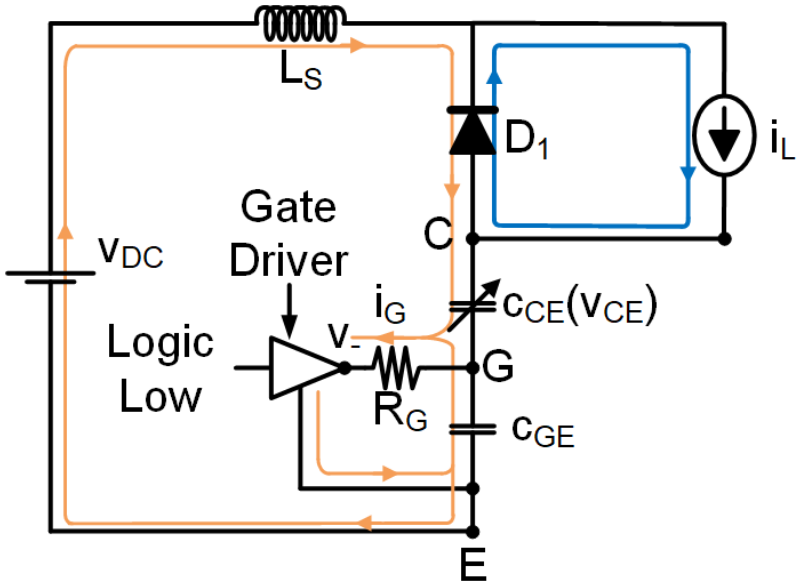


Figure 3.28: Interval 6 of turn off: ($t_{4,off} < t < t_{5,off}$) of equivalent circuit with current commutation path [24]

3.4.3 Ascertaining Switching Energy

Having briefly outlined the switching phenomenon taking place during transitions between on-state and off-states of IGBTs and their Diode counterparts finding their switching energies naturally follows. Remember, in the DPT at $t = t_1$ IGBT T_2 is turned off meanwhile Diode D_1 is turned on and at $t = t_2$ IGBT T_2 is turned on meanwhile Diode D_1 is turned off. Also, both load current and applied DC-link voltage are controllable. Thereby, employing an oscilloscope the current and voltage

waveforms are measured across both Diode and IGBT. Ascertaining the energies for associated waveforms can be done by multiplying the waveforms and integrating the result [23]. In comparison to other sources of switching loss, Diodes turn on losses are insubstantial and thus are often not supplied in datasheets. For turn on of IGBT integration bounds start when collector current reaches 10% of the imposed load current and end when collector-emitter voltage drops to 2% of the DC-link voltage. For turn off both IGBT and Diode integration limits begin when the device is blocking 10 % of DC-link voltage and concludes when current flowing through device falls to 2% of the prescribed load current.

3.5 Switching Power Losses

Manufacturers provide data plots of switching energies that they get through the processes explained earlier. Switching energies for an IGBT and Diode can be delineated as the sum of turn-on and turn-off energies (although for Diodes turn-on energy can be neglected),

$$E_{SW,x} = E_{on,x} + E_{off,x}. \tag{3.34}$$

Instead of linearly approximating the energy as is typical, having a polynomial function fitted to the data-plots bring about a more accurate estimation of switching losses [23, 25].

$$E_{SW,x} = A_x \ + \ B_x \ I_C \ + \ C_x \ {I_C}^{\,2} \tag{3.35}$$

Subscript "x" is a variable representing either an "I" or "D" for IGBT or Diode, respectively. Moving forward, evaluating the average switching power loss for a respective device can be sought as

$$P_{SW,x} = f_{SW} \frac{1}{2\pi} \int_0^{\pi} E_{SW,x} \, d(\omega t) \tag{3.36}$$

A relatively succinct analytical equation emerges if a linear interpolation is used to compensate for the fact that operating conditions of inverter is seldom equal to applied voltage employed to formulate switching energies in double pulse test [23, 25],

$$P_{SW,x} = f_{SW} \, \frac{v_{DC}}{V_{nom}} \, \left[\frac{A_x}{2} \, + \, \frac{B_x \, \hat{i}}{\pi} \, + \, \frac{C_x \, \hat{i}^{\,2}}{4} \right]. \tag{3.37}$$

DC-link voltage v_{DC} and peak output phase current $\hat{i}_a$ come from operating condition of inverter. Looking back to the very symmetry of operation that initially was taken advantage of, the total switching power loss is portrayed as

$$P_{Total,SW} = 6 \, [\, P_{SW,\,I} \, + \, P_{SW,\,D}] \, .$$

3.6 Total Power Loss

Finally, the total power loss is the sum of both conduction and switching losses,

$$P_{Total} = P_{Total,SW} + P_{Total,cond}.$$

Here $P_{Total,SW}$ and $P_{Total,cond}$ represents switching losses and conduction losses of all transistors of VSI, respectively.

3.7 Summary

This chapter elucidates how to estimate power losses of a VSI. Estimating power losses accurately provides precise design requirements of heatsinks enabling reduced over-engineering and more optimal solutions.

Chapter 4

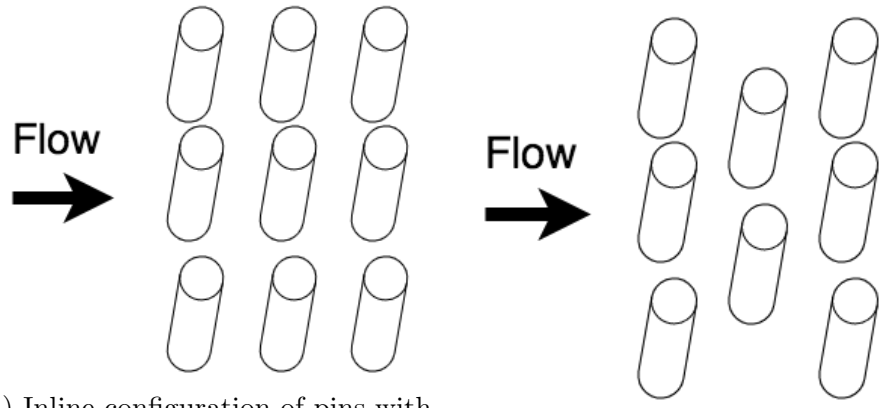
Review of The Heat Transfer and Flow Characteristics of Staggered Pin Fins Used for Power Module Cooling Applications

4.1 Introduction

Pin fin arrays are one method of augmenting heat transfer for power modules. Mechanisms that improve convective heat transfer for pin fins are:

- The increase of effective surface area.
- Induction of turbulence.
- Acceleration of flow by constricting passage cross-section.

Inevitably, however, the contractions and expansion of the fluid caused by the pin fin array also increase hydraulic resistance. Consequently, the larger pressure drop requires a commensurately sized pump. Pumping power must be kept minimal to reduce expense and achieve a compact system design. Ergo the art of implementing pin fin arrays is an optimization problem where pressure drop is minimized while achieving desired thermal performance. Pin fins have two configurations, the staggered and inline arrangement. Staggered arrangements are preferable to the inline pattern due to superior heat transfer. Stringent power density requirements constrict pin fin lengths in applications like automotive traction inverters where volume is very expensive.



(a) Inline configuration of pins with three rows of three pins

(b) Staggered configuration of pins with three rows; note that pins in adjacent rows are offset

Figure 4.1: Difference illustrated between pin fin configurations, namely between inline and staggered

Flow field due to pin fins are characterized as having wake regions behind the pins, vortexes, possible vortex shedding, and many phenomenons that cannot be analyzed analytically and are common to turbulent flow regimes. Pins also obstruct

flow, changing available flow passage area, leading to acceleration and deceleration of flow's velocity. Additionally, pins are close enough to each other such that pins adjacent and upstream affect the flow field downstream. The bottom line is that flow through a pin fin array cannot be analytically studied because it is too complex; instead, it is investigated experimentally. The optimized pin fin geometry design demands experimental correlations that accurately detail average heat transfer and friction factor for arrays with the relevant range of geometric parameters.

The availability of information for pin fins is scarce. The closest work to our application of cooling power modules is the internal cooling of turbine blades, especially near the trailing edge, where pin lengths are generally short, less than four diameters long ($H/D < 4$). Internal turbine blade cooling is also concerned with minimizing the pressure drop while cooling blades adequately. Air is compressed in a turbine engine for combustion, therefore the air flow expenditure into blades for cooling reduces engine performance as it is no longer being used for combustion [27]. Before the works on short pin fin arrays for the sake of turbine applications, tube banks were studied thoroughly. Tube banks operate in a manner where one fluid flows inside the tubes, and another fluid flows perpendicular to the tubes outside (tubes are hollow inside). In the early 1970s, Zukauskas summarized the works conducted in past decades (e.g. [28], [29], and [30]) on tube banks [31]. Tubes of a tube bank are very long (H/D $>$ 8); the heat transfer of the tube bank is characterized as the heat convected by the cylindrical surface area of tubes endwall heat transfer is negligible and seldom considered. Conversely, the heat convected off of the endwalls cannot be neglected for short pin fin arrays. Furthermore, the addition of pins may decrease wetted heat surface area relative to the plain channel case, depending on the efficiency

and length of pins. Lastly, since fluid flows through tubes, the surface temperature of tubes is assumed to be axially constant. In short, pin fins' temperature decreases axially with distance from the endwall. Thus, short pin fins and tube banks have different boundary conditions, and results obtained in [31] are not transferrable to short pin fins.

Turbine application thus pushed for the study of short pin fins. However, when it comes to the heat transfer of short pin fins, two systematic experimental programs distinguish themselves and stand out by their scope and comprehensiveness. That is the independent yet concurrent programs conducted at the NASA-Lewis Research Center and Arizona State University. The results of these programs are detailed in this chapter with a focus on the array's average heat transfer. On the other hand, there seems not to have been a proportionate interest in flow resistance as the works are limited in number. Also, the experimental results for hydraulic resistance of the pin fin arrays are to be delineated in this chapter. Further, only pin lengths from two to four diameters are of interest here.

4.2 Heat Transfer

4.2.1 Average Array Heat Tranfer Assuming Uniform Flow

Case Study in NASA-Lewis Research Center

In 1982, VanFossen [32] found no data for short pins fins, i.e., lengths to diameter ratios less than four ($H/D < 4$). He aimed to study short pin fins for heat transfer augmentation applied to turbine blades, expressly the trailing edge where the passage becomes narrow. Limitations in casting technology enforced a minimum pin diameter

of 1 mm. Naturally, the need arises to assess whether established experimental works and correlations based on longer pins are transferable to shorter pin fin arrays.

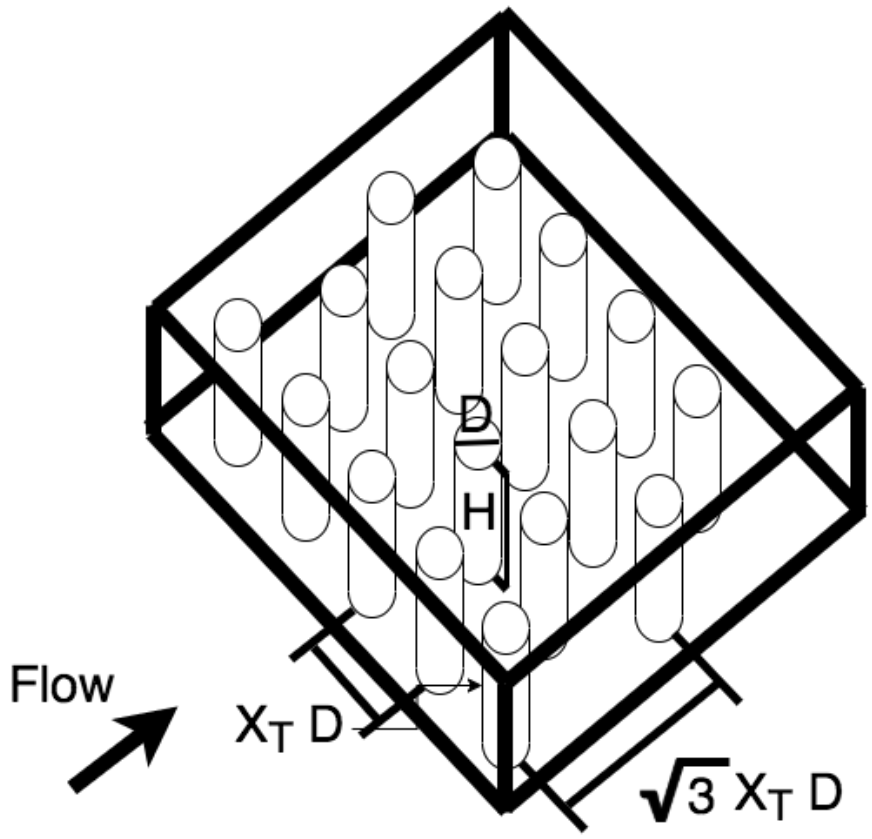


Figure 4.2: Generalized setup used to study heat transfer of short pin fins

VanFossen experimentally investigated four different cases. These cases incorporated two geometrically varying scenarios. A large model containing pins with a diameter of 6.35 mm, a pin length of two diameters, spaced four diameters apart in an equilateral triangular fashion. Equilateral spacing is visually illustrated in Fig.4.3, showing a two-by-two staggered array from top-view with pins equilaterally spaced.

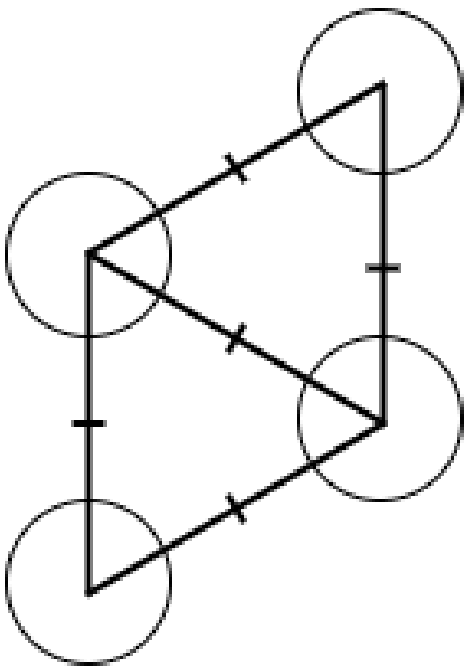


Figure 4.3: Depiction of equilateral spacing between pins in staggered configuration

There are three variations of this larger model:

- One had copper pins perpendicular to the endwall (Case A).
- Another had wooden pins perpendicular to the endwall (Case B).
- The third had copper pins at an incline to the endwall (Case C).

The smaller model has copper pins with a diameter of 3.175 mm, a pin length of one-half the diameter, equilaterally spaced two diameters apart (Case D). All tested cases have four rows in the streamwise direction. In the traverse or spanwise direction, the number of pins alternates between five and four, starting with a row comprising of five pins.

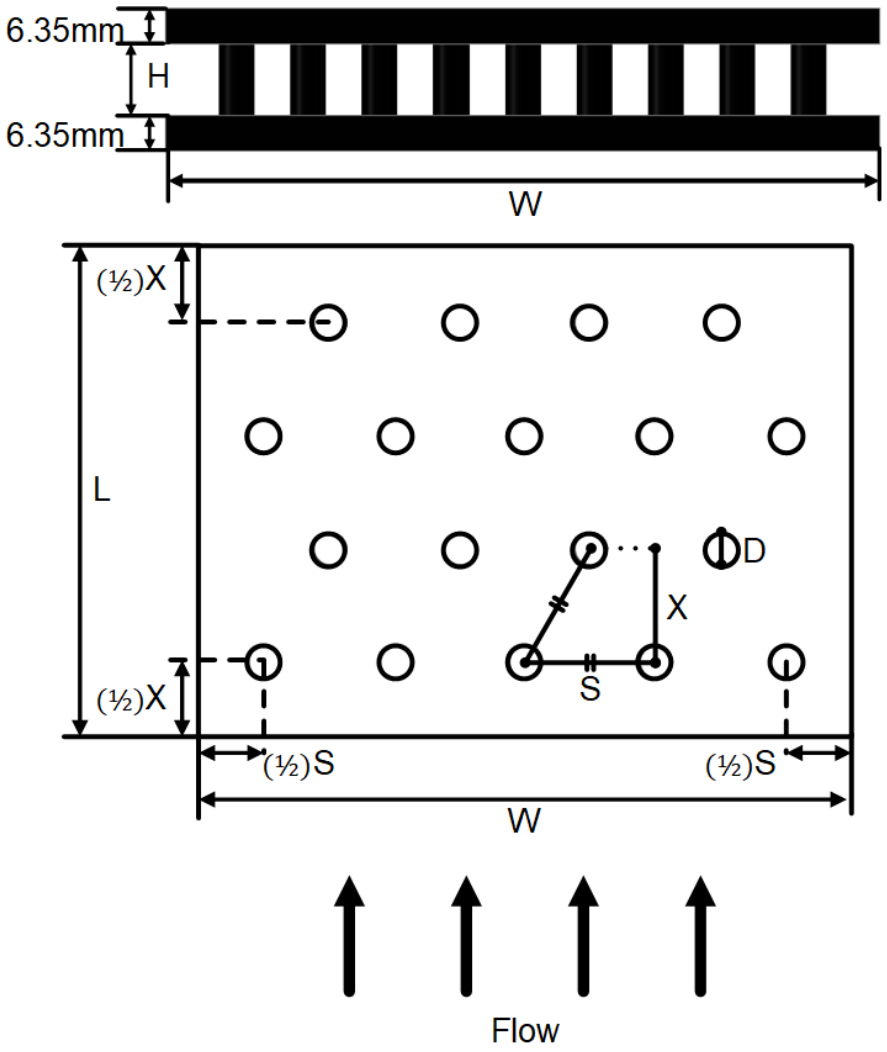


Figure 4.4: Pin Fin Channel Geometry Definition in VanFossen et. al.'s work

Pin Fin Geometries								
Case	$D\ [mm]$	H/D	S/D	X/D	θ deg	Material	$L\ [mm]$	$W\ [mm]$
A	6.35	2	4	$\sqrt{3}*2$	0	Copper	95.76	127
B	6.35	2	4	$\sqrt{3}*2$	0	Wood	95.76	127
C	6.35	2	4	$\sqrt{3}*2$	30	Copper	95.76	127
D	3.175	0.5	2	$\sqrt{3}$	0	Copper	24.69	31.75

Table 4.1: Geometries used in the case study of [32] to study heat transfer

VanFossen sought to estimate the average pin and endwall heat transfer coefficients [32]. Case B only differed from Case A in that the pin fins were constructed from wood instead of copper. Having the same geometry meant that the endwall heat transfer coefficients were the same for both models; the different conductivities of the pins enabled him to determine the ratio of the heat transfer coefficient of pins to the heat transfer coefficient of the endwall. He concluded that pins exhibited a higher heat transfer coefficient than the endwalls by approximately 35 % [32].

VanFossen hypothesized that setting pins at an incline to the endwall might result in superior heat transfer performance. Case C had copper pins oriented 30 degrees from the normal of the endwall surface, successive rows in streamwise direction alternated between positive and negative 30 degrees. He suspected that the wake shed from an inclined row would stretch to the next downstream row and intensify due to the downstream row's opposite angle inclination. Inclined pins, however, were found to have the same average heat transfer coefficient as their perpendicular counterparts,

namely, case A. Nevertheless, more remains to be investigated on inclined pins; it is possible that the pin spacing of this single test case diminished the advantages of inclined pins.

Experimental data conducted on the aforementioned test cases over Reynolds numbers ranging from 300 to 60,000 elucidate that short pin fins (H/D<4) have lower heat transfer than longer pin fins (H/D > 4). His heat transfer results for both the large and small models, Case A and Case D, in the non-dimensionalized form of Nusselt number versus Reynolds number all fit on a single correlation line. The least-square fit for the dimensionless heat transfer Nusselt number of small pin fins is given in [32] as

$$Nu = 0.153 Re^{0.685}, \tag{4.1}$$

where Reynolds number (Re) is defined as

$$Re = \frac{(m'/\tilde{A})D'}{\mu}. \tag{4.2}$$

Definitions that VanFossen employs in his analysis:

- m' = mass flow rate.
- V = open volume of test section.
- L = length of test section in direction of flow.
- $\tilde{A}$ = average flow area in test section; $\tilde{A} = V/L$.
- S = wetted surface area.
- D' = characteristic length of test section; $D' = 4V/S$.

Pin Fin Geometries							
Case	D $[mm]$	H/D	S/D	X/D	Material	L $[mm]$	W $[mm]$
8 rows	3.18	4	4	$\sqrt{3}*2$	Copper	95.8	127
4 rows	3.18	4	4	$\sqrt{3}*2$	Copper	47.65	127

Table 4.2: Experimental geometries used to study effect of number of rows on heat transfer [33]

.

- μ = coolant viscosity.

With regards to said correlation it is cautioned that the correlation might be fortuitous since the study was limited to only two models.

Brigham and VanFossen, in 1984 [33], sought to comparatively investigate the effect of the number of streamwise rows and length of pins on the heat transfer in short pin fin arrays. An experiment used in tandem with the previous study was designed and conducted to ascertain the answer. The diameter of pins is 3.18mm, the length of said pins is four diameters long (H/D = 4), spacing between pins is also four diameters apart in an equilateral fashion. Eight rows of pins in the streamwise direction. The model was then cut in half retaining only the four upstream rows, effectively constructing the other model. Endwall plates were constructed of copper 6.35mm thick. Indeed the figure earlier applied to detail the testing models from which the correlation is extracted. Indeed the figure earlier applied to detail the testing models from which the correlation is extracted. Also all definition are the same as in [32].

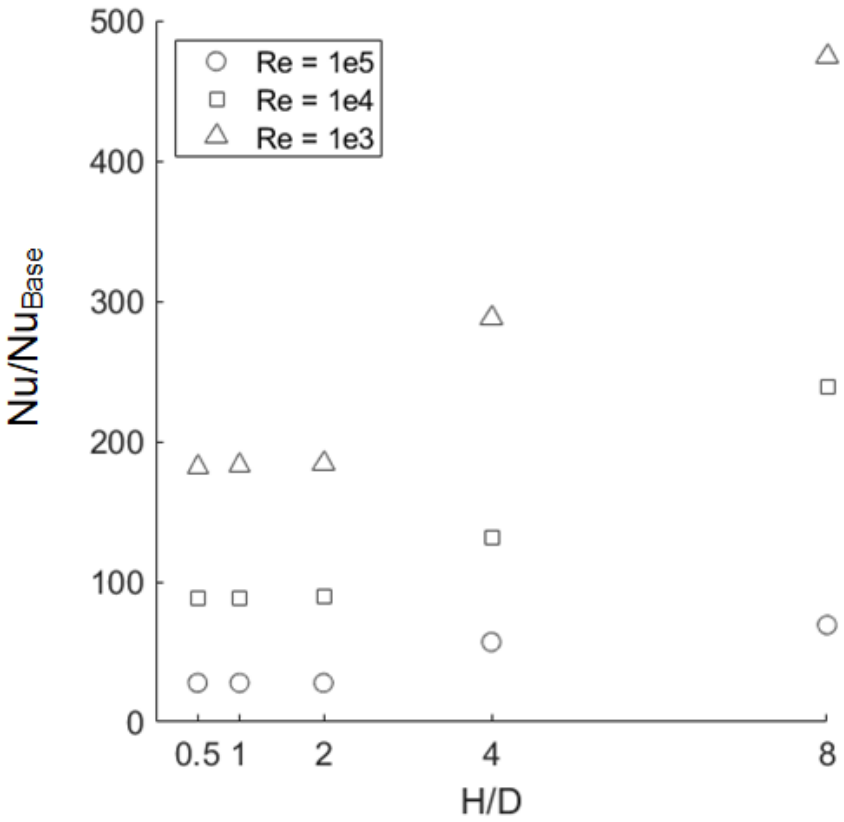


Figure 4.5: Nusselt number gain; referenced to plain channel correlation versus pin length

It is observed in the results that heat transfer of the four diameter long pins is higher than the two diameter and half diameter long pin fins of [32]. Also, the model with eight rows had a slightly higher heat transfer than the model with four rows. The latter point is consistent with the study in [34]; Simoneau et al. analyzed the effect of a pin fin's location relative to pin fin array. Strictly, in staggered pin fin arrays, pins that have; one, two, three, and four or more rows of pins upstream corresponded to a 21, 64, 58, and 46 percent increase in heat transfer. Therefore the eight-row model makes sense to have a slightly larger heat transfer than the four-row model.

Finally, [33] conveys that the effect of the pin length plays a more dominant role in the heat transfer than the number of rows. Further, [34] plots the gain of Nusselt number with respect to the correlation presented in [32] versus pin length (H/D), this is conveyed in Fig. 4.5. Expressly, [32] gives the base Nusselt number, relating to plain channel case, and is given as

$$Nu_{Base} = 0.023\ Re^{0.8}\ Pr^{\frac{1}{3}}\{1.11\{\frac{Re^{0.2}}{(\frac{L}{D'})^{0.8}}\}^{0.275}\}.$$

Case Study in Arizona State University

Independent of the studies conducted by VanFossen and associates, Metzger and associates took part in similar studies. Also motivated to improve internal cooling of turbine blades, Metzger et al. remarks that detailed knowledge of heat transfer and flow friction characteristics of short pin fin arrays are necessary for pin fins' rational design and achieving cooling objectives. Further, they highlight that the expense and time required to construct different geometries of pin fins have hindered establishing a coherent aggregate body of work on short pin fins. A comparative analysis in [35] between using wooden pins, and [36], using copper pins, with the same geometry resulted in Nusselt number agreement within 10%. In [36] pins are made of balsa wood while the endwall plates were made of copper. Figure 4.6 and table. 4.3 coalesce to detail the testing models geometry used in [36] and [35]. In [36] average Nusselt number of array is based on the uncovered endwall surface area neglecting pins, [35] is different in that they include the conducting copper pin heat transfer surface area. Nevertheless, these results confirmed the validity of utilizing non-conducting pins reducing the expense of testing model manufacturing, at least

for the Reynolds number ranging from $5x10^3 > Re > 5x10^4$ with Reynolds number being defined based on minimum flow cross-section area velocity given later.

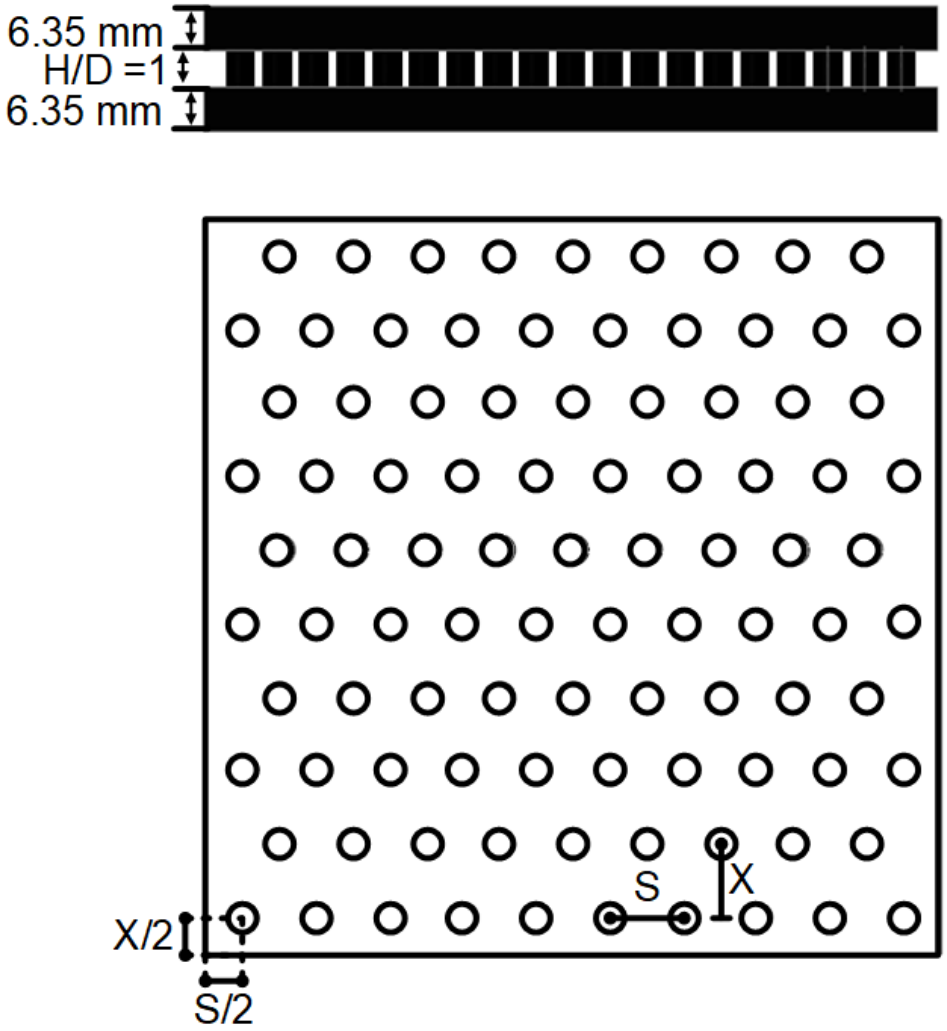


Figure 4.6: Parametric geometry used by Metzger et al. for experimental testing

Pin Fin Geometries

Case	$D\ [mm]$	H/D	S/D	X/D
i	5.08	1	2.5	2.5
ii	8.46	1	2.5	1.5

Table 4.3: Metzger et al. Non-dimensional Parameters for [36] and [35]

Moreover, [36] analyzed the row-by-row Nusselt number variation based on the location of pins in relation to array, similar to [34]. Results for the investigation are illustrated below in figures 4.7 and 4.8.

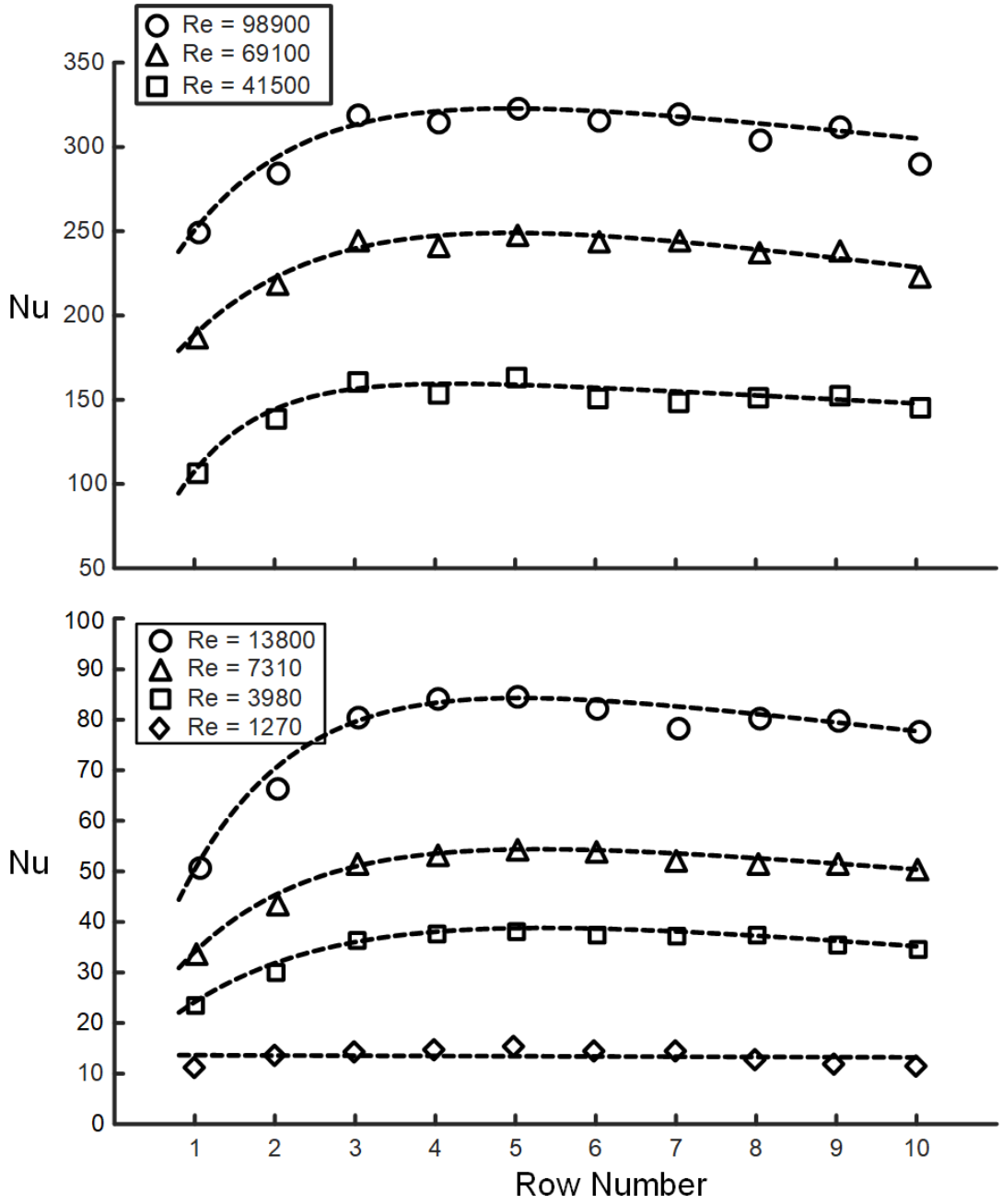


Figure 4.7: Nu development for S/D = 2.5, X/D = 1.5, and H/D = 1

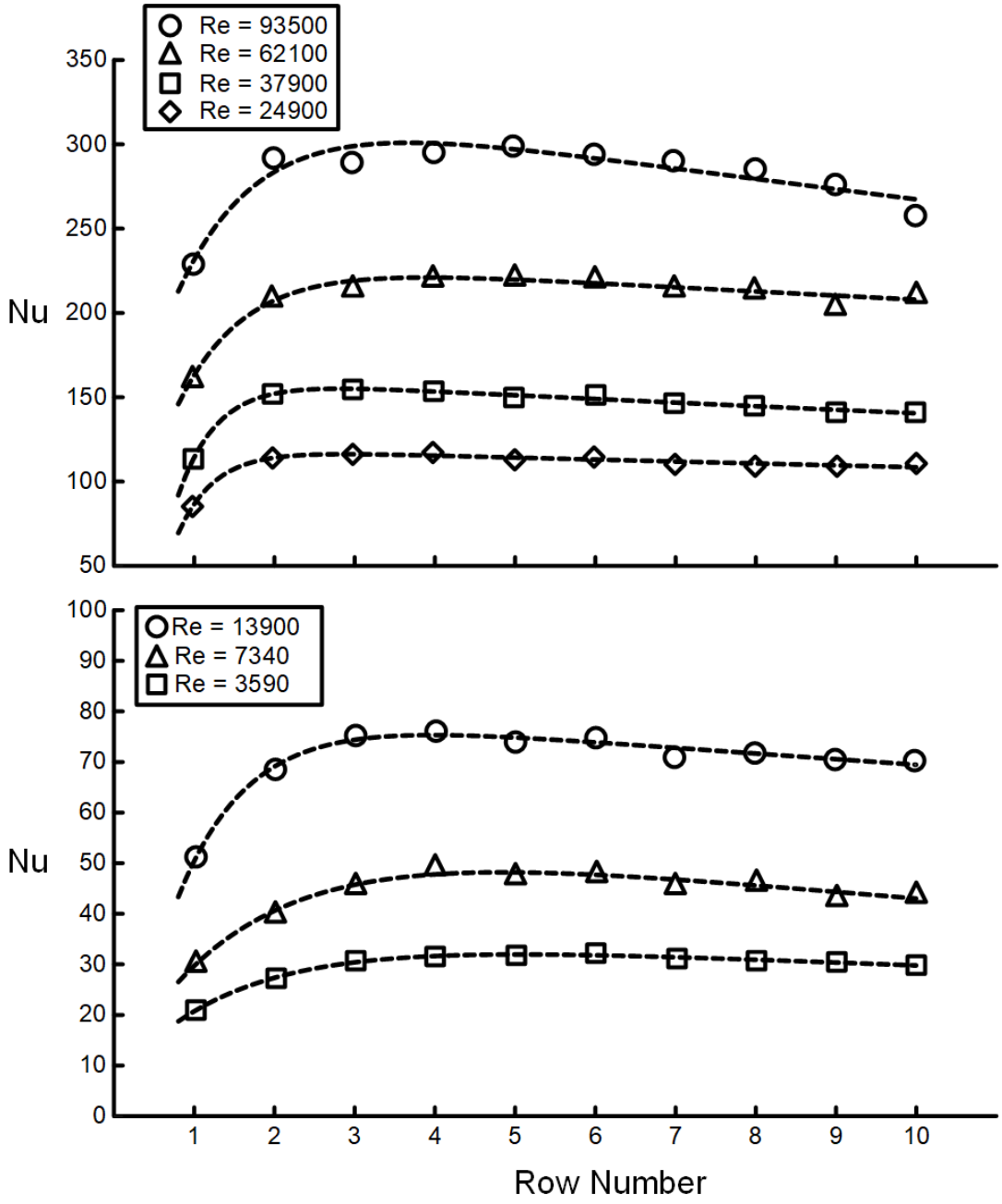


Figure 4.8: Nu development for S/D = 2.5, X/D = 2.5, and H/D = 1

Later in 1986, Metzger et al. published another paper [37] where the original experiment in [35] was amended to. Originally in [35], only two configurations were

Pin Fin Geometries ([37] and [35])

Case	H/D	S/D	X/D
i	1	2.5	2.5
ii	1	2.5	1.5
iii	1	2.5	3.0
iv	1	2.5	4.5
v	1	2.5	5.0

Table 4.4: Metzger et al. Non-dimensional Parameters for [36] and [35]

tested, namely those of Table. 4.3. In the paper presently being addressed [37] an additional three configurations were added. Premised on the work of [33], Metzger et al. states that for pin lengths under three diameters heat transfer is independent of pin length which is why he didn't study effect of different pin lengths. For the three additional configurations, it is said that the same diameters used in [35] are used, however with two different pin diameters this leaves a point of confusion. This is justified because of the independence of heat transfer on pin length, provided that length is less than three diameters. Assuming all pins are the same, Nusselt number is given in eq. 4.3 [37].

$$Nu = 0.135\ {Re_D}^{0.69}\ (X/D)^{-0.34} \tag{4.3}$$

Unlike the work conducted during case study of NASA-Lewis Research Center, Reynold number is defined here differently according to the pin diameter [27, 35–37].

$$Re_D = \frac{\rho\, V_{max}\, D}{\mu} \tag{4.4}$$

- ρ = density of coolant
- V_{max} = channel mean velocity at minimum flow area
- D = pin diameter
- μ = viscosity of coolant

4.3 Pressure Drop

Exiguous efforts have addressed the hydraulic resistace of short pin fin arrays. Damerow et al. [38], in 1972, performed experiments on various models containing ten streamwise rows and a model of pin array in converging duct a prevalent topic in turbine applications pin fin cooling. These models conform to Fig. 4.6 with parameters given in Table 4.5.

Pin Fin Geometries

Case	Number of Rows [N]	$D\ [mm]$	H/D	S/D	X/D
A	10	0.51	3.75	5	3.54
B	10	2.54	2	3	2.12
C	10	2.54	4	3	2.12
D	10	2.54	2	5	3.54
E	10	2.54	4	5	3.54
F	5	2.54	2.3 to 1.7	3	2.12

Table 4.5: Array geometry for Damerow's work

To the end of making data independent of the upstream and the downstream conditions, the friction factors are based on the measured total pressure drop from the first row to the last row. This means that for an 'N' row array the friction losses caused by $(N-1)$ flow constrictions and expansions are considered and the results are not dependent on upstream or downstream conditions. Friction factor measured from experiments are based on the following definition [38],

$$f = \frac{\Delta P_T\ \rho}{2[N-1]\ V_{max}^2}. \tag{4.5}$$

The friction factor was next expressed by Damerow et al. [38] to best correlate by the expression

$$f = [2.06\ (\frac{S}{D})^{-1.1}]\ Re_D^{-0.16}. \tag{4.6}$$

It is mentioned that the friction factor is found to be substantially lower than the long tube correlation, namely that of Jacob [28], predicted. Friction factor was not influenced by pin length (H/D) in the range of the study.

In 1982, Metzger et al. [27] investigated the hydraulic resistance in short pin fin arrays. Experiments investigating the effect of streamwise pitch (X/D) on friction factor was obtained for single spanwise pitch ($S/D = 2.5$). Seven different configurations were analyzed, Table. details the geometry of said configurations. Rows in the direction of coolant flow alternate between having nine and ten pins constituting ten streamwise rows of either nine or ten pins in spanwise direction.

Pin Fin Geometries

Case	H/D	S/D	X/D	D $[mm]$
i	1	2.5	1.05	5.08
ii	1	2.5	1.5	4.24
iii	1	2.5	1.5	8.46
iv	1	2.5	1.79	5.08
v	1	2.5	2.5	5.08
vi	1	2.5	3	4.24
vii	1	2.5	5	2.54

Table 4.6: Metzger's pressure drop based experimental setup

Interestingly the pins here are made of balsa wood, this causes a difference in thermal boundary conditions, leading to an expected difference in the heat transfer coefficients. Moreover, it is found that at low Reynolds number the heat transfer coefficient for the non-conducting pin case over-predicts that of the conducting pin case. Conversely, at high Reynolds numbers non-conducting pin fins, balsa wood, under-predicts heat transfer of conducting pin fin case, copper. Over the range of Reynolds numbers ($5x10^3 > Re_D > 5x10^4$), non-conducting pins estimate heat transfer to within 10% of conducting pins.

Albeit employment of non-conductive pins is controversial in terms of their thermal study, they have same flow field as their conducting counterparts validating their employment for analyzing hydraulic resistance characteristics. Obtained from the experiments conducted on the seven configurations, data was fitted into two expressions depending on Reynolds number range.

at $10^3 \leq Re_D \leq 10^4$:

$$f = 0.317\ Re_D^{-0.132} \tag{4.7}$$

for $10^4 \leq Re \leq 10^5$:

$$f = 1.76\ Re_D^{-0.318} \tag{4.8}$$

4.4 Summary

Our objective is to estimate average heat transfer and pressure drop for arrays of staggered uniform pin fins with length of two to four diameters. Pin diameter must be larger than 1mm for manufacturing feasibility. Both the studies on heat transfer

explicated in this chapter provide accuracy for a specific range of parameters. For the case of the study conducted at the NASA-Lewis Research Center the array of pins where limited to equilateral spaced pins, with spanwise (traverse) distances from two to four diameters (S/D = 2 to 4), and pin lengths from half to four diameters (H/D = 0.5 to 4). Alternatively, the study conducted at the Arizona State University is based on pin lengths of one diameter, spanwise pitch of two and a half (S/D = 2.5), and streamwise pitch from one to five (X/D = 1 to 5). Based on the range of parameters, the correlation based on the studies at NASA-Lewis Research Center are found to be more unrestraining. Also the validity of using the average heat transfer is shown in that there is a difference in Nusselt number over only the first few rows then the nussult number is constant. It naturally follows that if an array has many rows of pins (N¿8) then the average Nusselt number is a good estimate.

Comparing the correlation of Metzger et al. and Damerow et al. it is portrayed that in the former case the friction factor is only a function of reynold number, conversely the latter case shows a dependence on spanwise distance between pins as well as reynold number. This is explained in that the spanwise pitch is kept constant in Metzger et al.'s work. Hence, the scope of Damarow et al.'s correlation is advantageous; it allows for varying spanwise pitch an important parameter.

Ergo, the correlation for non-dimensional heat transfer, Nusselt number, is taken based on the work of the NASA-Lewis Research Center, and Damarow et al.'s work gives the friction factor correlation.

Chapter 5

Design of Pin Fin Heat Sink

5.1 Introduction

The methodology used to create a tool based on MATLAB is delineated in this chapter. Application-based parameters, the volumetric flow and inlet temperature of the coolant, are applied as inputs, from which three parameters are optimized. These three parameters are the diameter of the pins of the staggered pin fin heat sink, the length of the pins, and the pin spacing factor that establishes the distance from pin to pin. Some assumptions are made, some of which are due to restrictions from the experimental correlations, others so that there is consistency when variables are changed. Pins are spaced in an equilateral manner, and all pins have the same length and diameter. The coolant used is the glycol-50 mixture. Although performance is slightly inferior to distilled water, Glycol-50 is very commonly used, being as how it does not freeze at 0^oC at atmospheric pressure. A fluid volume is defined where this glycol-50 mixture is given a uniform velocity at the inlet boundary condition. It is important to realize that the pin fin array is being optimized, not the coolant

chamber. Methodology described herein is tailored so that results can be validated with the commercial ANSYS Fluent software in the last chapter. This chapter begins with a commercially available, IGBT-based, representative Hybrid pack on which our optimization is based. Intentionally, this module is chosen because it already comes with an integrated pin fin heatsink for validation purposes, considering it is optimized by industry. The methodology of generating a pin fin heatsink geometry for application such as power modules where discrete chips on a substrate dissipate heat and are attached to heatsinks does not exist, at least to my best knowledge, having done an extensive review. The ones found either had the entire surface have a uniform heat flux applied, assumed laminar flow, or dealt with really long or micro-pin fins. Short pin fins with aspect ratios (H/D) greater than two and less than four were not found, despite this being the most interesting and favorable range. That said, the works that have amassed in the literature make the methodology used herein possible. The goal is to develop a tool that will optimize a pin fin array for any power converter that employs modules, and here it is designed for a two-level voltage source traction inverter as a proof of concept.

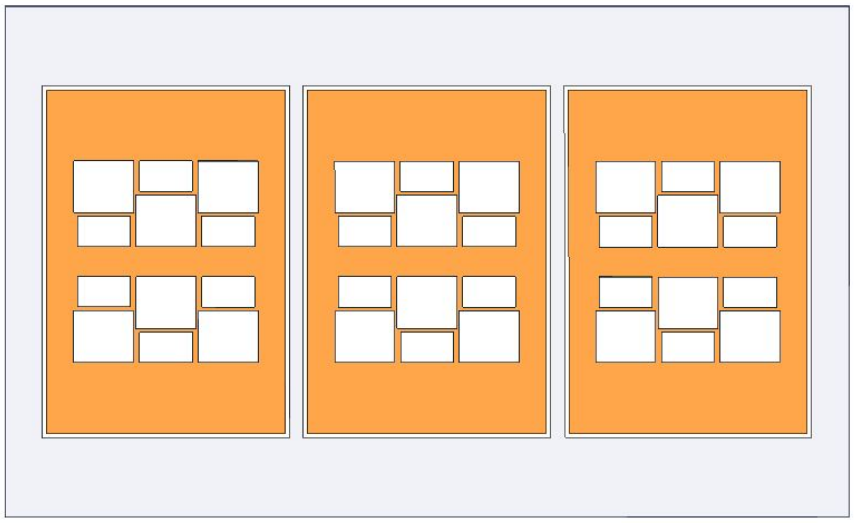
This chapter begins by defining the problem based on a representative module that is used as a benchmark. Then pin fin geometry is determined based on the variables being optimized for. Later power losses are given for an assumed application. An explanation and the theoretical basis for the models estimating maximum heatsink wetted surface temperature and pressure drop are outlined thoroughly. Finally, the formulation of an objective function being solved for is defined.

5.2 Problem Setup and Objectives

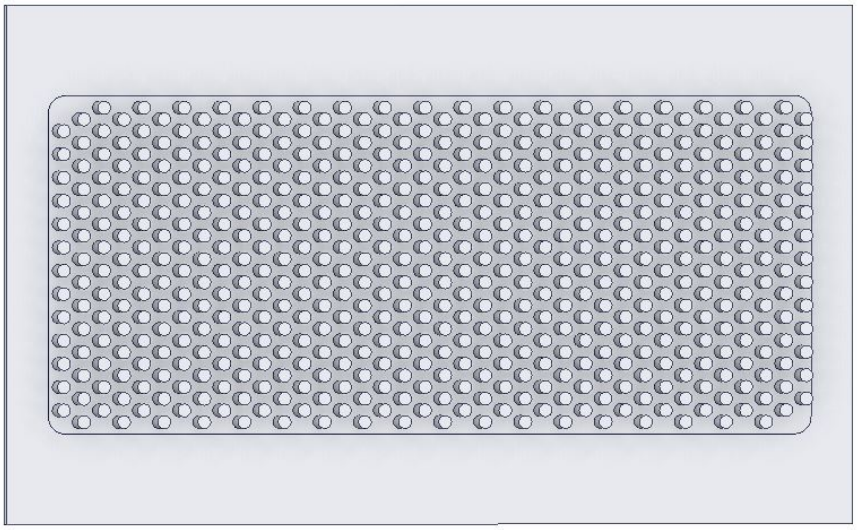
First and foremost, the optimization problem ought to be defined. This tool is intended to be extended to any power electronics converter that employs a modular approach, power modules. However, preliminarily it is applied to the two-level voltage source traction inverter. Moreover, it is used for geometric constraints that coincide with the commercially available hybrid pack to validate the methodology used herein. A CAD model is made of a commercially available hybrid pack, namely the FS380R12A6T4B IGBT module fig 5.1. Dimensions of the representative power module have been estimated or measured as accurately as possible; still, some assumptions had to be made. Focus on the cooling pin-fin heat sink that also serves as base-plate is of primary importance.

As a side note, integrating the pin-fin heat sink as the base-plate is referred to as direct cooling and is advantageous compared to the alternative method of having them separate. Instead of direct cooling, a base-plate with a flat bottom is mechanically attached to a heat sink by screws. A problem arises where due to imperfections of the flat surfaces at the bottom of the base-plate and top of the heat sink, small pockets of air are trapped between the two adjacent surfaces; these small cavities of air increase the thermal resistance of the module drastically as static air has a very low thermal conductivity. Similarly, the surfaces can be concave or convex causing inadequate contact. A thermal interface material (TIM) is applied to circumvent this problem, decreasing the thermal resistance of the power module. Still, the TIM has a low thermal conductivity and is found to increase the thermal resistance by as much as 30%, although it is preferable to the case with no TIM. Hence, by integrating the

heat sink as the base-plate, a substantial decrease in thermal resistance is found.



(a) Uncovered Power Module top view



(b) Power Module bottom view

Figure 5.1: CAD model of representative power module

The representative commercial Hybrid Pack exhibits a pin fin array spanning the dimensions 137 mm by 60 mm, as is accentuated in the figure below. Our Pin Fin

array must also reside within this space for a fair comparison.

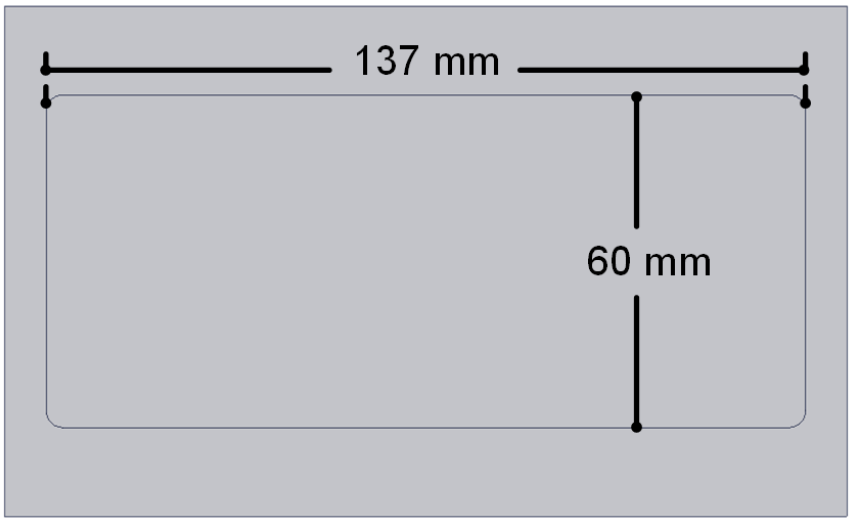


Figure 5.2: Optimization Geometric Space

The pin fin geometric variables that are optimized for are the spanwise (S_Y) and streamwise (S_X) distance between pin axes as well as the uniform length of pins (H).

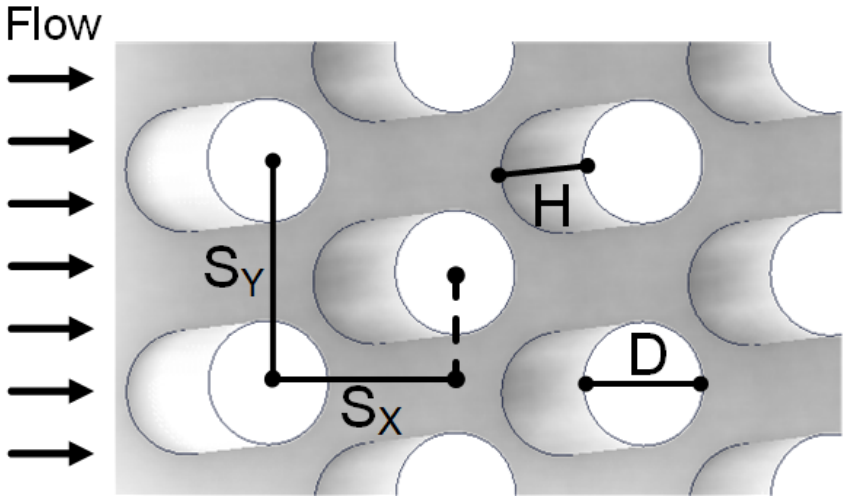


Figure 5.3: Optimization Variables

Constraints are also placed by the empirical correlations:

- Length of pins range from two to three diameters long ($2 \leq H/D \leq 3$)
- Diameter of pins should be greater than 1.5 mm ($D \geq 1.5mm$)
- Distance between pins must be equilateral ($S_X = \frac{\sqrt{3}}{2} S_Y$)

Because the spanwise and streamwise distances are not independent, they can both be expressed by a single variable, X_T, multiplied by the pin diameter, D.

$$\begin{aligned} S_Y &= X_T \; D \\ S_X &= \frac{\sqrt{3}}{2} X_T \; D \end{aligned} \tag{5.1}$$

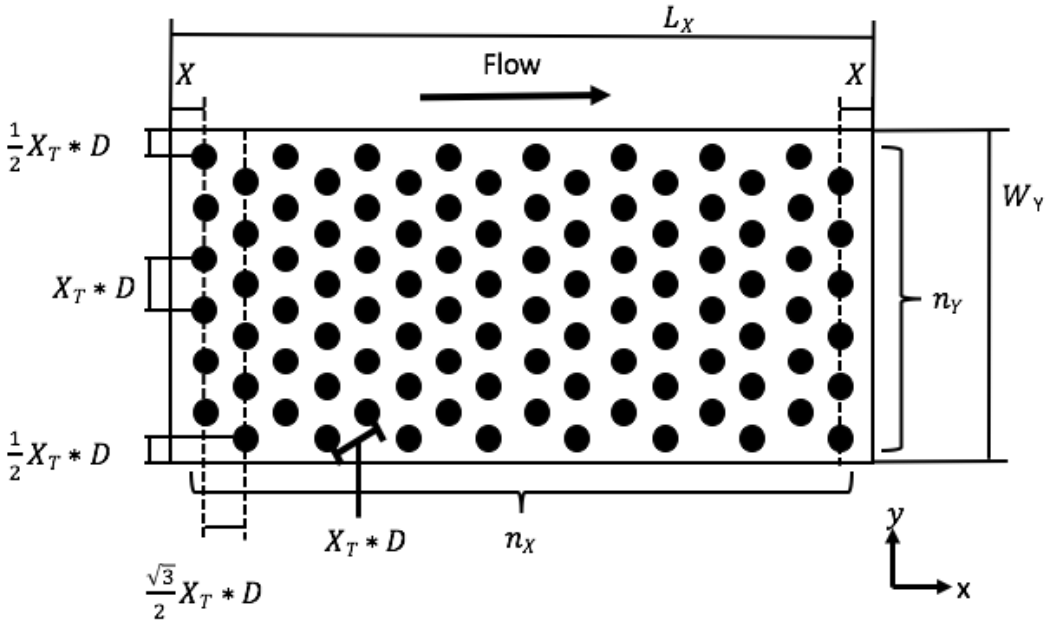


Figure 5.4: Geometric Dimension Constraints

For pins not to intercept X_T must be greater than one, this is a physical constraint to make sure pins remain cylindrical. From the side of empirical correlations, X_T

ought to be greater than 1.5 and less than 4. Width of array cannot exceed 60 mm, in Y- direction, therefore, in staggered arrays for a given diameter of pins, D, and a pin distance factor of X_T, the maximum number of pins per streamwise row (n_Y) is given as by the governing equation

$$W_Y = (n_Y + 0.5)\ X_T\ D. \tag{5.2}$$

Here, W_Y is the width in Y-direction. Number of pins per streamwise row is iteratively increased in a while-loop up to an integer where the next increment results in a width, W_Y, greater than 60mm. An array's length in the streamwise direction, X-direction, must be less than 137 mm as dictated by the benchmarking representative IGBT module. Thereby, using the governing equation below the number of rows in streamwise direction (n_X) is increased iteratively by one such that the maximum amount of pin rows is found while remaining within the constraint. To add, the distance from axis of first row to the boundary of the 137mm and the axis of the last row pins to the end boundary are intently made to be equal, this is denoted by x in fig. 5.4 and the actual distance is not a constraint only that at both ends same distance exists.

$$L_X = (\frac{\sqrt{3}}{2} X_T\ n_X + 1)\ D \tag{5.3}$$

This concludes how the pin fin array is constructed based on three geometric variables; uniform length of pin (H), pin distance factor of (X_T), and pin diameter (D).

Table 5.1: Variable constraints on Pin Fin Array

Variables	Minimum	Maximum
Diameter (D)	1.5 mm	4mm
Dimensionless pin length (H/D)	2	3
Pin distance factor (X_T)	1.5	4

5.2.1 power losses

The objective is to design a tool capable of optimizing a pin fin heat sink geometry specifically tailored for the thermal management of an IGBT power module employed for traction inverters. The use of the commercial IGBT module, namely the FS380R12A6T4B $HybridPack^{TM}$ Drive Module, is specifically applied in a two-level voltage source inverter. It is assumed that the inverter will drive a 160 kW Permanent Magnet Synchronous Motor (PMSM); this is a four-pole pair machine rated for a maximum speed of 3000 rpm, and the base speed of the traction motor is 1800 rpm. Additionally, the DC-link voltage is 600 V(dc), and the power factor at full load is assumed not to fall below 0.9. Thereby the maximum output current is 242 A RMS. Strictly, only the SVPWM modulation scheme for the constant power range of the motor's operation is considered. Power losses are implemented using MATLAB/Simulink and the PLECS library. Relevant data from the datasheet is inputted into the IGBT and FWD diodes parameters. These parameters are temperature dependent, and the PLECS library enables the use of a one-dimensional thermal model where the junction temperature is fed back to attain the correct parameters. From

this model, instantaneous power loss values can be ascertained then averaged over a fundamental electrical frequency. Naturally, the fundamental frequency is 60 Hz which corresponds to the maximum base speed of the motor. Results of the analysis are provided in the table below.

Table 5.2: Power Loss Results at worst-case scenario

Power Loss	IGBT	Diode
Conduction Loss per switch (W)	193.90	14.10
Switching Loss per switch (W)	269.26	60.09
Total Switch Losses per switch (W)	463.16	74.19
Total Inverter Loss (W)	3254.1	

5.3 Modelling

To rationally design pin fin geometries, detailed knowledge of heat transfer and flow resistance is required. As the previous chapter elucidated, analytical methods are not practical due to the innate complexity of the physical phenomenon. Empirical correlations are thus used; the last chapter presented the most comprehensive of the structured investigations. Also, the preceding chapter concluded that the program undertaken by the NASA-Lewis Research Center provided heat transfer correlation, and Damarow et al.'s work details the flow resistance well for a suitable and overlapping range of parameters.

5.3.1 Basis for Heat Transfer Model

To commence with the estimation of the heat transfer, the correlation from the NASA-Lewis Research Center is employed. The point here is to estimate the effective heat transfer coefficient of the equivalent wetted surface area of baseplate for a given geometry of pin fins. The immense work conducted to define correlations using experimental results describing heat transfer entails a set of varying definitions, assumptions, and different levels of experimental error margins. Data from experiments is analyzed through a lens of a theoretical model. Achieving accuracy calls for the employment of the correlation in a way that is consistent with the assumptions that produced the correlation.

Before running a data run, VanFossen et al. ran a set of calibration runs to estimate the heat lost to surroundings. Sealing off the inlet and outlet of a test section minimizes natural convection; simply cutting off airflow with the inlet flow control valves does not decrease the encapsulated volume as much, where fluid flows, allowing for higher natural convection. Following this, the heater power is adjusted to achieve desired endwall-plate temperatures. After a waiting period that allows the test section to find equilibrium and reach steady-state, end-wall plate temperatures (T_w), ambient air temperature (T_a), and the heater power level (Q_{loss}) are measured. The overall heat transfer coefficient (h_{loss}) is then defined as

$$h_{loss} = \frac{Q_{loss}}{S_h\,(T_w - T_a)}. \tag{5.4}$$

Calculating the overall loss heat transfer coefficient for a range of endwall-plate to ambient air temperature differences enunciated the relationship between heat transfer coefficient and temperature differences. The required heater power level with no airflow to achieve the desired endwall-plate temperature can now be computed. So for a desired endwall-plate temperature, the observers apply heater power appropriate, then the desired airflow is set. Due to forced convection, the endwall-plate temperature drops, so the heater power level is adjusted, giving a new heater power (Q), maintaining the desired endwall-plate temperature. Once equilibrium is reached, measurements are taken (five samples).

The effective heat transfer coefficient is given by

$$h_{eff} = \frac{Q \ - \ Q_{loss}}{S_h \ (T_w - T_{aw})}, \tag{5.5}$$

where the adiabatic wall temperature T_{aw} is the temperature of the endwall-plate wall temperature assuming no forced convection (T_w in eq. 5.4 correlating to a given Q_{loss}). Technically it isn't adiabatic, but since natural convection is minimized, it is assumed negligible.

Although given in the previous chapter, the definitions used for the test sections is reiterated here. Reynolds number is given as

$$Re = \frac{(m'/\tilde{A})D'}{\mu}. \tag{5.6}$$

Other relavent definitions:

- m' = mass flow rate.
- V = open volume of test section.

- L = length of test section in direction of flow.
- $\tilde{A}$ = average flow area in test section; $\tilde{A} = V/L$.
- S = wetted surface area.
- D' = characteristic length of test section; $D' = 4V/S$.
- μ = coolant viscosity.

The analysis is conducted on a per pin basis. The heater applies heat flux (Q_{total}), and heat flux is convected out from endwall (Q_{wall}) and pin surfaces(Q_{pin}), assuming steady-state conditions. Also, the heat flux going into the pin is equivalent to the heat flux convected out of the pin's surfaces. Heat lost by a pin and endwall surfaces through convection is also equal to the heat lost by plain surface (A_w)with the heat transfer coefficient h_{eff} (notice that in equation 5.5 heater surface is used). The theoretical model can be delineated by the mathematical expressions

$$Q_{total} = Q_{wall} + Q_{pin}, \tag{5.7}$$

$$Q_{total} = h_w(A_w - A_p)(T_w - T_{aw}) + \sqrt{P\ h_p\ k_p\ A_p}\ tanh(m_{eff}l)(T_w - Taw), \tag{5.8}$$

$$and\ Q_{total} = h_{eff}\ A_w(T_w - T_{aw}). \tag{5.9}$$

Definitions used are listed below.

- h_w = average heat transfer coefficient of endwall surface.

- h_p = average heat transfer coefficient of pin surface.
- A_w = area of endwall associated with one pin. $A_w = \frac{\sqrt{3}}{2}(X_T\ D)^2$
- A_p = cross-section area of pin. $A_p = \frac{\pi}{4}\ D^2$
- P = perimeter of pin. $P = \pi\ D$
- k_p = thermal conductivity of pin
- m_{eff} = fin parameter defined as $m_{eff} = \sqrt{\frac{h_p\ P}{k_p\ A_p}}$.
- l = half length of pin
- T_w = wall temperature
- T_{aw} = adiabatic wall temperature

The resulting equation is summarized as

$$h_w(A_w\ -\ A_p)\ + \sqrt{P\ h_p\ k_p\ A_p}\ tanh(m_{eff}l) -\ h_{eff}\ A_w = 0 \tag{5.10}$$

For every effective heat transfer coefficient calculated from measured experimental data, the average heat transfer coefficient of pins and endwalls can be found by the Newton-Raphson iterative technique. It is assumed that the endwall and pin heat transfer coefficients are the same, $h_w = h_p = h$. The Nusselt number was calculated from the heat transfer coefficient h as

$$Nu = \frac{h\ D'}{k_f}. \tag{5.11}$$

Using the modified correlation for plain channels given in [32] and the table constructed in [33] to account for pin lengths from one-half to four diameters long (linear interpolation). For convenience they are reiterated below.

$$Nu_{Base} = 0.023\ Re^{0.8}\ Pr^{\frac{1}{3}}\{1.11\{\frac{Re^{0.2}}{(\frac{L}{D'})^{0.8}}\}^{0.275}\}.$$

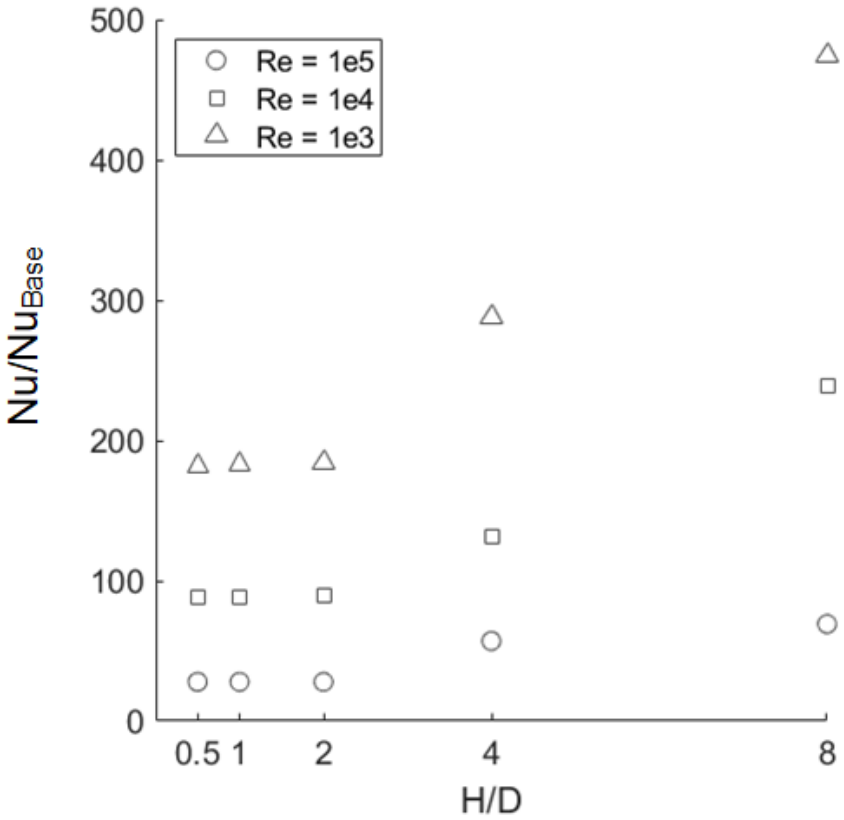


Figure 5.5: Nusselt number gain; referenced to plain channel correlation versus pin length

Here; L is the length of the test section in streamwise direction; and Pr is the Prandlt number of fluid is defined as the heat capacity (C_p), the fluid's viscosity (μ),

and thermal conductivity of fluid (k_f) as $Pr = \frac{C_p\,\mu}{k_f}$. Please note that for VanFossen et al.'s work, both the top and bottom endwall-plates had a heater attached to the top and lower side, respectively. However, due to symmetry, the analysis is done based on a half-pin length. For our work, heat is applied only to one endwall plate, namely the top side. Since for the application of concern, power module cooling, the heat flux is applied only on the top endwall-plate, therefore the correlation is modified such that instead of using a pin's half length, the entire pin length is used.

5.3.2 Implementation of Heat transfer Model

Implementing a model in MATLAB, that can estimate the effective heat transfer coefficient of the wetted surface area of baseplate/heat sink, based on experimental correlation of the NASA-Lewis Research Center is the subject of this section. As was previously elucidated in a prior section the pin fin array has three input variables (i.e. D, H, and X_T) from which an array is constructed. Additionally the glycol-50 mixture coolant inlet temperature and volumetric flow rate are application specific input variables. To employ the correlation some definitions must be formulated. The open volume of pin fin array is given as

$$V = H\,(W_Y \cdot L_X - n_X \cdot n_Y \cdot \frac{\pi \cdot D^2}{4}). \tag{5.12}$$

Wetted surface area is found using

$$S = W_Y \cdot L_X - (n_X \cdot n_Y)\,\frac{\pi D^2}{4} + H\,(n_X \cdot n_Y)\,\pi \cdot D.$$

Characteristic length can be ascertained from the wetted surface area and array's open volume by

$$D' = \frac{4 \cdot V}{S}. \tag{5.13}$$

Next, the average flow area is characterized as

$$\tilde{A} = \frac{V}{L_x}. \tag{5.14}$$

For a given volumetric flow rate $\tilde{V}$, the Reynolds number is

$$Re = \frac{\rho(\tilde{V}/\tilde{A})D'}{\mu}. \tag{5.15}$$

Where, ρ and μ are the fluid's density and viscosity, respectively. In addition, the Prandtl number is a dimensionless number quantifying the ratio of the momentum diffusivity over the thermal diffusivity. The formula of the Prandtl number is based on the specific heat capacity (C_p), the dynamic viscosity (μ), and the thermal conductivity of the coolant(k_f).

$$Pr = \frac{C_p \cdot \mu}{k_f} \tag{5.16}$$

By now everything is available as to utilize the correlation giving us the base Nusselt number that is then multiplied by the gain Nu/Nu_{Base} based on the dimensionless length of pins (H/D) which is linearly interpolated from figure 5.5.

$$Nu_{Base} = 0.023\ Re^{0.8}\ Pr^{\frac{1}{3}}\{1.11\{\frac{Re^{0.2}}{(\frac{L_X}{D'})^{0.8}}\}^{0.275}\}.$$

Having found the Nusselt number, the average heat transfer coefficient $\tilde{h}$ on a per pin basis can be calculated using

$$\tilde{h} = \frac{Nu \cdot k_f}{D'}. \tag{5.17}$$

Power losses calculated give the worst-case average losses or equivalently the heat load of IGBT and Diode per switch. This switch is composed of three IGBT dies in parallel and three Diode dies in parallel; the heat load (Q) of IGBT and Diode is thus distributed among the dies, respectively (it is assumed that the heat flux (q'') is evenly distributed on the die's top surface area (A)).

$$q''_{IGBT} = \frac{Q_{IGBT,Sw}}{3 * (A_{IGBT,Sw})} \tag{5.18}$$

$$q''_{Diode} = \frac{Q_{Diode,Sw}}{3 * (A_{Diode,Sw})} \tag{5.19}$$

Due to the IGBTs having a higher heat flux as compared to Diodes and because of the flow direction, the last IGBT die in streamwise direction has coolant absorb heat from all the upstream dies. As a result, the last set of IGBT dies are the critical dies that the per pin analysis is done on. Moreover, premised on equations (5.7- 5.9), working backwards to find effective heat transfer coefficient given the pin and endwall surface average heat transfer coefficient.

$$h_w(A_w \ - \ A_p) \ + \sqrt{P \ h_p \ k_p \ A_p} \ tanh(ml) - h_{eff} \ A_w = 0 \tag{5.20}$$

Effective heat transfer coefficient is calculated using the Ralph-Newton's numerical approach. So far for a given set of input variables the effective heat transfer coefficient

for the equivalent wetted surface area on a per pin basis can be estimated using this model that is implemented in MATLAB.

5.3.3 Basis of Pressure Drop Correlation

Unlike, heat transfer the pressure drop can be found relatively easily, and the theoretical basis is very simple. Damarrow et al. published a correlation for friction factor based on total pressure difference (ΔP_T) measured from the centerline of the first row of pins to the centerline of the last row of pins in a streamwise direction. This is said to make the data independent of the inlet and outlet duct section. The same pin array geometry constraints of the previous heat transfer section were used, except that pins were not restrictively made equalaterally spaced (a restriction made for the sake of accurate heat transfer estimation according to experiments which correlation predicates on). For n_X rows, the friction losses is based on equation

$$f = \frac{\Delta P_T}{0.5(n_X - 1)(v_{max})^2 \cdot \rho}. \tag{5.21}$$

The maximum velocity in a pin fin array is defined as the volumetric flow rate divided by the minimum flow cross-section area (A_{min}).

$$v_{max} = \frac{\tilde{V}}{A_{min}} \tag{5.22}$$

Damarrow et al. fitted his data to a correlation given as

$$f = [2.06(X_T)^{-1.1}]Re_D^{-0.16} \tag{5.23}$$

where Reynolds number is defined in different manner than in case of heat transfer correlation. The maximum velocity (v_{max}) is used instead of average and the characteristic length is the diameter of pin (D).

$$Re_D = \frac{\rho v_{max} D}{\mu} \tag{5.24}$$

5.3.4 Implementation of a pressure drop model

The optimized array geometry for a given flow rate and inlet temperature are to be validated in ANSYS Fluent. As such, the fluid chamber is going to have a coolant volume of 141mm in length, a width of W_Y, and a height equal to the pins length (H). One, when running a CFD simulation on the module, the obstructing pins must be a little distant from inlet boundary otherwise mesh issues arise. Second the width, W_Y is used as opposed to 60 mm because different pin diameters (D) and pin distance factor(X_T) will have a varying side bypass flow influencing results drastically. Instead, a width of W_Y makes sure distance between side walls and adjacent pins is always equal to $0.5 \cdot X_T \cdot D$ as to attain a fair solution based solely on input variables. Lastly the fluid volume must have a height equal to the length of pins (H) for consistency so that bypass flow underneath pin doesn't influence results. These are also imposed so that the models used herein provide accurate estimation of optimized results. Further optimization of these parameters can be a secondary study and optimization problem for the coolant chamber itself.

Without further preamble, to implement a model estimating pressure drop first the maximum velocity of flow must be calculated using eq. 5.22. This requires the

minimum flow cross-section area, that is

$$A_{min} = H(W_Y - n_Y \cdot D) \tag{5.25}$$

The Reynolds number from eq. 5.24 along with the pin distance factor X_T make calculating the friction factor (f) in equation 5.23 a trivial matter. Pressure Drop is finally found as

$$\Delta P_T = 0.5 \cdot f \cdot \rho \cdot n_X \cdot v_{max}^2. \tag{5.26}$$

Clearly, there was a slight modification where $(n_X - 1)$ is changed to n_X, that is because our inlet boundary condition simply applies uniform flow velocity at inlet correlating to a desired volumetric flow rate. Plus, it is not necessary to ignore the first contraction and the last expansion of flow because the fluid volume is defined in a consistent manner to input variables.

5.4 Optimization

So far, for a given set of inputs; namely, the pin diameter (D), the uniform pin length (H), pin distance factor (X_T), volumetric flow rate ($\tilde{V}$), and inlet coolant temperature (T_{inlet}); generating the pin fin heatsink geometry and estimating it's pressure drop and equivalent heat transfer coefficient. With our reference power module, the heat load given by power losses is applied to the dies of the CAD module in an FEA steady-state thermal simulation using ANSYS Steady-State thermal package found in ANSYS Workbench. The minimum allowable effective heat transfer coefficient is found such that junction temperatures don't exceed allowable value. Without any fluid or even a pin fin array, the geometric space at the bottom of the baseplate (the 137mm by 60mm area), which encompasses the pin fins, is ascribed a heat transfer coefficient at a reference temperature value. This heat transfer coefficient is tweaked until the desired silicon die junction temperature of 150° C is attained. This is what was define to be the minimum effective heat transfer coefficient value that ensures junction temperatures remain below the maximum prescribes operation value of 150^oC. Further details of this process is given in the following chapter.

5.4.1 Optimization Metric

This is a constrained optimization problem, variables must remain in acceptable range defined previously and under the worst-case heat load the wetted surface area of baseplate must have a heat transfer coefficient exceeding the minimum heat transfer coefficient value $h_{eff,desired}$. The primary objective of a heatsink is to augment heat transfer such that the junction temperatures of semiconductor switch dies remains below prescribed value of 150 ^oC. It is a secondary objective to minimize pressure

drop. This is the methodology used herein, thereby pin fins array is designed specific to application and for provided chip-layout.

Alternatively, some design pin fin geometry for overall performance in a generic sense. For instance, a performance index can be designed for, the coefficient of performance (COP),it evaluates both the pumping power and the dissipated power or Heat load together. Increased pressure drop for a given flow rate means increased pumping power and pump size, this operational expenditure is undesirable because of stringent system requirements in most applications and especially those of electrified vehicles. To this end, a performance index is employed, the coefficient of performance (COP),it evaluates both the pumping power and the dissipated power or Heat load. The pumping power is both a function of the coolant flow rate and the pressure drop across heatsink [39, 40]. Indeed, the pumping power (Q_{pump}) required for a heatsink can be calculated as the product of the pressure drop (ΔP_T) and the volumetric flow rate of the coolant($\tilde{V}$).

$$Q_{pump} = \Delta P_T \cdot \tilde{V} \tag{5.27}$$

Let Q_{load} denote the module's total power loss or heat load dissipated by heatsink. The COP is defined as the ratio of the power dissipated to the power expense required for operation of cooling system.

$$COP = \frac{Q_{load}}{Q_{pump}} \tag{5.28}$$

This is a good metric because it relates both quantities having the same units making them comparable. Pressure should be in Pascals and volumetric flow rate should

be in cubic meters per second such that the pumping power is in watts. Heat load, naturally, should also be in watts. COP is a metric used to evaluate performance, where a higher value means better performance. Optimization problems are minimization problems therefore employing its inverse is required, the inverse coefficient of performance (ICOP).

$$ICOP = \frac{1}{COP} \tag{5.29}$$

Using such an approach is advantageous because it provides a geometry that has great performance and could be used in a modular way facilitating multiple chip layouts. As long as heat flux in critical regions does not exceed the heat flux that the pin fin geometry can handle the same baseplate can be used. This translates to lower costs because the same baseplate can be used for multiple modules with varying power and current ratings taking advantage of economy of scale. Albeit this is a good approach, it does not provide the optimal baseplate performance for a given application. It is hoped that our tool be extended in future in many ways, one of which is for it to optimize pin fin array and compare results to other optimized heat transfer augmentation techniques. Our methodology in optimization provides the most rigorous approach to comparison studies for heat transfer augmenting techniques. Plus, instead of designing chip layout in accordance with thermal requirements the baseplate/heatsink can be designed in accordance with the chip-layout. In either case it is not difficult to switch approaches as it only requires minor modifications to objective function.

Objective functions for constrained optimization problems can be solved by minimizing an objective function with penalty terms enforcing the constraints. The constraints where given in table 5.1. In addition to the optimization variable (D,H,

and X_T), the application specific inlet coolant temperature (T_{inlet}) and volumetric flow rate ($\tilde{V}$) are also required, but inside model they are treated as given and not optimized for. In MATLAB the following equation is implemented as the objective function. Three functions are made; one for estimating effective heat transfer coefficient on a per fin basis at critical position, one that estimates pressure drop, and lastly one that gives necessary pin fin array geometric variables used internally in formerly mentioned functions.

$$\begin{aligned} f_{obj}(D,H,X_T) = \quad & 1e10 \cdot abs\Bigg(min\Bigg(\Big(0.8 \cdot geth_{eff}(D,H,X_T) - h_{eff,desired} \Big), 0 \Bigg) \Bigg) \\ & + 1e5 \Bigg(\; abs\Big(min\big(D - 1.5,\; 0\big) \Big) \; + \; max\big(D - 3,\; 0\big) \\ & + \; abs\Big(min\big(\frac{H}{D} - 2,\; 0\big) \Big) \; + \; max\big(\frac{H}{D} - 3,\; 0\big) \\ & + \; abs\Big(min\big(X_T - 1.5,\; 0\big) \Big) \; + \; max\big(X_T - 4,\; 0\big) \Bigg) \\ & + getPressure(D,H,X_T) \end{aligned} \tag{5.30}$$

Both flow rate and inlet coolant temperature are assigned internally. It should be accentuated, that the MATLAB function that estimates effective heat transfer coefficient is multiplied by 0.8, this is due to the fact that in [41], Armstrong et al. applied the correlation used by us to a large set of experimental data found in literature where he found that the correlation estimated Nusselt number well with a margin of $\pm 20\%$ for short pin fins with aspect ratio less than 3. Therefore, conservatively the estimated heat transfer coefficient is multiplied by 0.8 so that the heat transfer coefficient is not over-predicted. Also this is why length of pins does not exceed 3-diameters.

5.4.2 optimization method

The problem can be formulated as

$$\min_{D,\, H,\, X_T} f_{obj}(D,\ H,\ X_T), \tag{5.31}$$

for a given flow rate and inlet coolant temperature. The built in Genetic Algorithm Optimization function in MATLAB is used. MATLAB comes with a built in GA algorithm. Lower and upper bounds are defined for the variables, although the objective function already contains penalty terms. Population size is assigned to be 2000, algorithm is run for 100 generations. Initial population variables are arbitrary chosen as D = 2.5 mm, H = 7.5 mm, and X_T=2. Variables must be in vector form for this algorithm to work, therefore a MATLAB function containing the objective function is used (getObj(X); where X(1)= D, X(2)=H, and X(3)=X_T).

5.5 Summary

The methodology of designing an optimized pin fin array geometry has been explicated in this chapter. Optimization problem has been tailored so that it is easily validated with CFD simulation, in ANSYS Fluent. Power losses have been calculated for an assumed application. Minimum allowable wetted surface heat transfer coefficient value of baseplate is to be first obtained with FEA thermal simulation on ANSYS Workbench Steady-state Thermal Analysis package, addressed in next chapter more thoroughly, this ensures silicon dies don't exceed operational temperature limit. Description of MATLAB model estimating heat transfer coefficient of baseplate's wetted surface for given heat load, coolant flow rate, inlet temperature, and

pin fin geometry is given. Pressure drop model is also explained in depth. Objective function with penalty terms ensuring that both variable constraints and temperature requirements (equivalently heat transfer coefficient requirements) are met has been introduced which also minimizes pressure drop concurrently. For a given coolant flow rate and inlet temperature a pin fin array's geometry is optimized by the GA algorithm using models based on short pin fin array heat transfer and pressure drop empirical correlations.

Chapter 6

Results and Simulations

6.1 Introduction

At this point, all that is left is to validate the optimization tool developed thus far. To this end, the tool is applied to various application-based scenarios. In previous chapter, worst-case power losses where calculated for a two-level voltage source traction inverter premised on application requirements, provided therein. A representative commercially available hyrbrid pack IGBT module with integrated pin fins is employed to benchmark this study. Given the worst-case power losses prescribed by inverter's requirements, the chip layout, as well as stack-up details of representative power module, designing an optimized pin fin geometry achieving minimal pressure drop while maintaining semiconductor die junction temperatures below 150^0C. Application-based requirements related to geometry of pin fin array only includes flow rate and inlet coolant temperature; where power losses and module are unchanged, apart from the pin fin array.

First, the methodology used to find the minimum effective heat transfer coefficient

required is explained, this requires simulations in ANSYS Workbench using Steady-State Thermal Analysis component. Thermally relevant properties of the module are given. Three different scenarios, differing in flow rates and inlet coolant temperatures, are studied. Geometry of pin fin array is next optimized for the different scenarios using MATLAB tool. Lastly, the CAD model of module with the optimized pin fin geometry integrated is used to run CFD-simulations in ANSYS Fluent. Simulation results allow for the evaluation of the optimization tool's accuracy.

6.2 Defining Optimization Problem

The optimization tool developed takes the coolant's inlet temperature and flow rate as input variables. This is because the flow rate and inlet temperature are design parameters dependent on system level requirements. The same coolant can be used to cool multiple devices, one of which being the traction inverter. Our objective is to optimize the pin fin geometry that is integrated onto bottom of baseplate. Three different cases are optimized for:

- Case 1: $Flowrate = 5LPM$ and $T_{inlet} = 65^oC$
- Case 2: $Flowrate = 10LPM$ and $T_{inlet} = 75^oC$
- Case 3: $Flowrate = 15LPM$ and $T_{inlet} = 85^oC$

The thermal design of pin fin array geometry is also dependent on the power module layout, stack-up construction, and heat load. All of these details are held constant for all our optimization cases.

CAD model

A CAD model is approximated of the FS380R12AT4B module by Infineon. Figure 5.1 illustrated the approximated CAD model. The stack-up details are provided next.

Power Module Stack-up details

Nothing in the power module is altered with respect to the commercially available hybrid pack, with the exception of the pin fin array geometry that is integrated at the bottom of the 3 mm thick copper baseplate. Thermally relevant properties of the stack-up are enunciated by table 6.1 and figure 6.1 provides a visual depiction of a typical power module's stack-up construction. These properties are assumed based on [42–47].

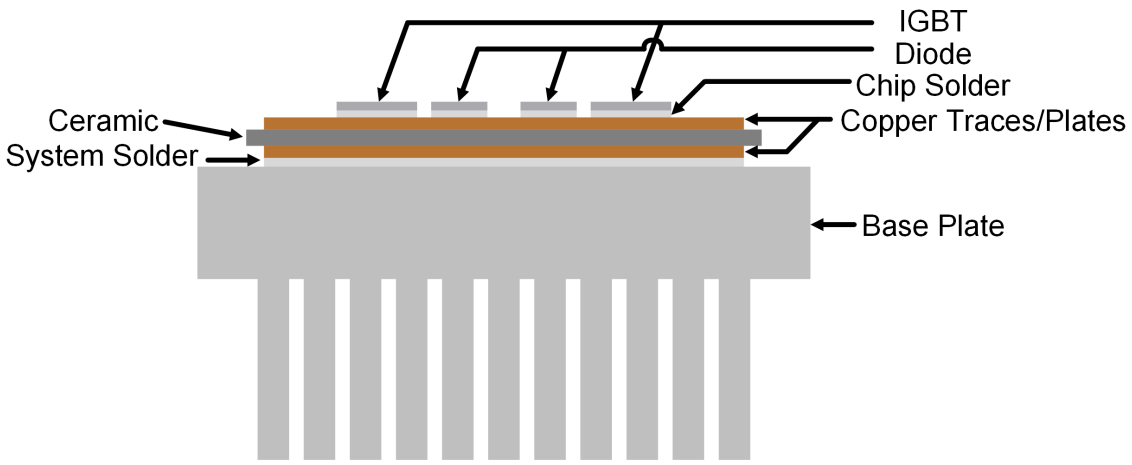


Figure 6.1: Typical power module stack-up

Stack-up Thermal Details of Power Module					
Layer	Material	Thickness $[mm]$	ρ $[kg/m^3]$	C_p $[J/kg \cdot K]$	$k[W/m \cdot K]$
IGBT	Si	0.07	2330	710	150
Die Attach	Sn-based	0.09	8580	235	200
Traces/Plate	Cu	0.3	8700	385	385
Ceramic	Si3N4	0.32	3300	660	78
System Solder	Sn-based	0.25	9000	228	62
Base Plate	Cu	3	8700	385	385

Table 6.1: Stack-up Thermal Details

Defining Heat Load Based on Power losses

The power loss and power module is held constant for all optimization scenerios. In practice, because there is error in power loss calculations a factor of 1.5 is taken to ensure inverter operates safely. On a per switch basis, the IGBT and diode were found in previous chapter to have a power loss of 463.16 W and 74.19W, respectively. To address the safety margin, thermal design is for an IGBT and diode power loss of 694.74 W and 111.285 W, respectively. For every switch there are three IGBT and Diode chips connected in parallel as shown in previous chapter. These chips share current equally and block same DC-link voltage; the heat generated is then distributed equally among chips. Each IGBT and diode chip has a cross-section area of 100.362 mm^2 and 53.734 mm^2, respectively. Consequently, a heat load can be

approximated as a uniform heat flux applied on the top surface of chips. A heat flux of 2307452 [W/m^2] and 717027.7 [W/m^2] is applied on the top surface of all IGBT and diode chips, respectively.

Defining Pin Fin Array Geometry

Pin Fins arrays are designed based on three variables the diameter of pins(D), the Length of Pins (H), the pin distance factor (X_T). Where the pin distance factor defines distance between adjacent pin's axes. In the spanwise and streamwise directions distance between pins adjacent pins is given as $X_T\ D$ and $0.5 \cdot \sqrt{3} X_T\ D$, respectively. Number of pins in both directions is the maximum number that keeps pin fin array inside the wetted surface area, spanning a 137mm by 60mm dimensions at the center of baseplate bottom surface. A Fluid domain is defined with a height equal to that of pin fin lengths, the length in streamwise direction is 141mm, and the width in spanwise direction is defined such that minimum distance between sides and pin axes is $0.5\ X_T\ D$ from both ends. The width is made sure to be less that 60mm. Ofcourse, the pin fin array is centered with respect to baseplate. More detail was given back in section 5.2.

6.3 Results

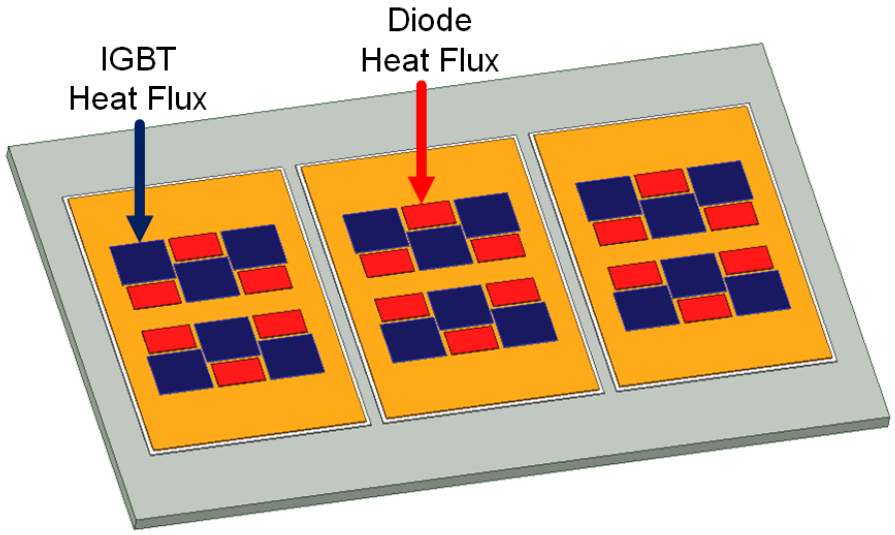
Our optimization takes a hybrid approach and can be broken down into two steps. Step one is finding the minimum effective heat transfer coefficient at the bottom of baseplate. Next, using the minimum allowed heat transfer coefficient and with the MATLAB code and GA algorithm the optimized geometry is found. Lastly, simulations are run in ANSYS to verify the results, simulation results are shown in

next section.

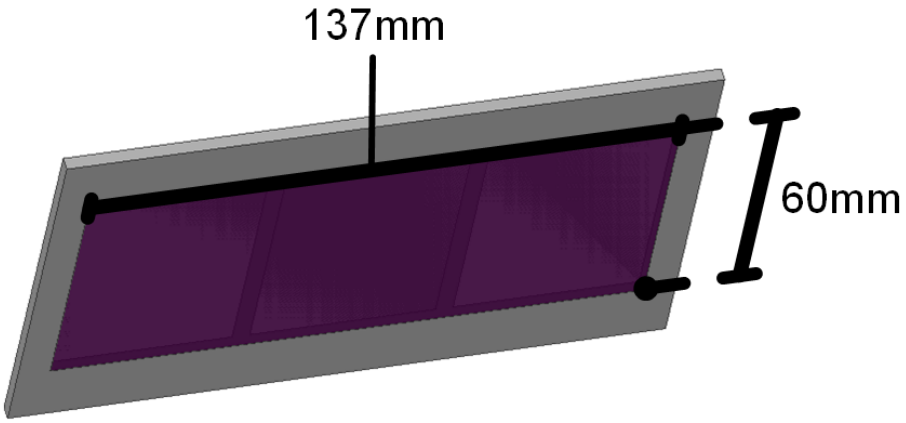
6.3.1 Finding Minimum Acceptable Effective Heat Transfer Coefficient

Simulation in the Steady-state thermal analysis system in ANSYS Workbench are done to find the minimum allowable effective heat transfer coefficient at the effective wetted surface area of baseplate. All material properties are inputted into Engineering data Component system of ANSYS Workbench. CAD approximated in accordance with representative power module is inputted, bottom of baseplate was modified as is explained shortly. All materials are assigned. Automatic contacts are used in Steady-State Thermal Analysis system, only overlapping contacts are redefined. Meshing was done on CAD where element size was chosen to be 8e-4, there is 0.458 million elements. Heat load is applied as heat flux on the top of all dies. Implementing heat load is shown in figure below; IGBT and diode heat flux of 2307452 [W/m^2] and 717027.7 [W/m^2] is applied to all the IGBT and Diode Top surfaces, respectively. In figure 6.2a, IGBT and Diode Surfaces are colored blue and red, respectively.

Instead of pin fins a flat surface extruded only 0.1mm is made at the bottom of baseplate with dimensions 137mm by 60mm constituting the effective wetted sureface area. Figure 6.2b illustrates the effective wetted surface area of baseplate. On the effective wetted surface area a heat transfer coefficient is applied as well as an ambient temperature.



(a) Applying respective heat fluxes on IGBT and Diode surfaces, colored blue and red,respectively



(b) Effective wetted surface of baseplate where effective heat transfer coefficient is optained

Figure 6.2: Boundary conditions for finding minimum allowable heat transfer coefficient

Theoretically the ambient temperature in our simulation should be defined as the adiabatic wall temperature (T_{aw}) as in section 5.3.1. However, because the adiabatic

wall temperature is dependent on the velocity of the fluid a function of the pin fin array's geometry, the average outlet temperature of fluid (T_{outlet}) is used. The average temperature of fluid at outlet is always higher than the adiabatic wall temperature. So the minimum effective heat transfer coefficient found herein is conservative, being higher than it needs to be.

- Case 1: $T_{out} = 80.93^oC$
- Case 2: $T_{out} = 82.85^oC$
- Case 3: $T_{out} = 90.28^oC$

The minimum allowable effective heat transfer coefficient ($h_{eff,\,min}$) is found manually in a binary search fashion such that the maximum junction temperature is as close to 150^{o}C as possible.

- Case 1: $h_{eff,min} = 18625\ [W/m^2K]$ results in $T_{j,max} = 149.96^oC$
- Case 2: $h_{eff,min} = 19593.75\ [W/m^2K]$ results in $T_{j,max} = 149.98^oC$
- Case 3: $h_{eff,min} = 24453.13\ [W/m^2K]$ results in $T_{j,max} = 150.00^oC$

6.3.2 Obtaining Optimum Geometry Variables

The MATLAB based tool takes advantage of the GA algorithm searching for geometric variables that result in an effective heat transfer coefficient greater than the minimum acceptable value at the minimum pressure drop possible. The optimization

problem is mathematically reiterated as

$$\begin{aligned} \min_{D,H,X_T} \quad & Pressure(D,H,X_T) \\ \text{s.t.} \quad & h_{eff}(D,H,X_T) \ \geq \ h_{eff,\,min} \\ & 1.5 \ \leq \ D \ \leq \ 4 \\ & 2 \ \leq \ \frac{H}{D} \ \leq \ 3 \\ & 1.5 \ \leq \ X_T \ \leq \ 4 \end{aligned} \tag{6.1}$$

Where the effective heat transfer coefficient and pressure drop of array are calculated based on experimental correlations described in Chapter 4. The genetic algorithm is set to 100 generations and population size of 2000, solution is found to always converge.

Case 1:

The optimized pin fin array's geometry for our thermal design, given a flow rate of 5 LPM and coolant inlet temperature of 65^oC, is described by the variables

$$\begin{aligned} D &= 2.07\ mm \\ H &= 6.22\ mm \\ X_T &= 1.54 \\ \text{Number of streamwise pins} &= 50 \\ \text{Number of spanwise pins} &= 18 \end{aligned} \tag{6.2}$$

The fluid domain is defined as having dimensions

$$\begin{aligned} \text{length in streamwise direction} &= 148\ mm \\ \text{width in spanwise direction} &= 58.97\ mm \\ \text{height} &= 6.22\ mm \end{aligned} \tag{6.3}$$

Case 2:

The optimized pin fin array's geometry for our thermal design, given a flow rate of 10 LPM and coolant inlet temperature of 75^oC, is described by the variables

$$\begin{aligned} D &= 3.13\ mm \\ H &= 9.38\ mm \\ X_T &= 1.5 \\ \text{Number of streamwise pins} &= 34 \\ \text{Number of spanwise pins} &= 12 \end{aligned} \tag{6.4}$$

The fluid domain is defined as having dimensions

$$\begin{aligned} \text{length in streamwise direction} &= 148\ mm \\ \text{width in spanwise direction} &= 58.7\ mm \\ \text{height} &= 9.38\ mm \end{aligned} \tag{6.5}$$

Case 3:

The optimized pin fin array's geometry for our thermal design, given a flow rate of 15 LPM and coolant inlet temperature of 85^oC, is described by the variables

$$\begin{aligned} D &= 2.86\ mm \\ H &= 8.49\ mm \\ X_T &= 1.51 \\ \text{Number of streamwise pins} &= 37 \\ \text{Number of spanwise pins} &= 13 \end{aligned} \tag{6.6}$$

The fluid domain is defined as having dimensions

$$\begin{aligned} \text{length in streamwise direction} &= 148\ mm \\ \text{width in spanwise direction} &= 58.3\ mm \\ \text{height} &= 8.49\ mm \end{aligned} \tag{6.7}$$

6.4 CFD-Simulation Studies

ANSYS-Fluent is used to simulate the results of our optimized geometries for all three cases. The different layers of the Power Module, except for baseplate are meshed, using swept meshing elements, such that there are at least two layers of mesh for smallest dimension (i.e., thickness of each layers). Baseplate and the fluid domain are meshed with tetrahedral element due to complexity of shapes. The behavior of fluid near the walls is complex and non-linear, therefore, the mesh must be refined such that it can capture the physics well. Ergo, inflation layers are applied to the wetted

surface between fluid domain and baseplate, for both the baseplate and fluid domain. Inflation contains 5 layers with a first mesh thickness of 1e-5 mm.

Material properties are inputted into Fluent and assigned to respective material. The simulation is coupled, that is it solves for both energy and hydraulics. The commonly used two equation k-ω SST model is used for our simulations. In reality, it is the Navier-Stokes Equation that governs flow (for all flow regimes), but for CFD-simulations reduced-order turbulence models are employed resulting in unavoidable errors.

For simulation results to be considered accurate several metrics are checked. One, the relevant outputs must converge, for our case maximum temperature of both IGBT and Diode as well as the pressure drop across array. To verify this convergence of results, the results are plotted in console and only if results converge could they be taken seriously; otherwise the results become dependent on the number of iterations of simulation. Additionally, the residuals must be monotonically going downwards and below a certain value otherwise one would have a residual convergence error. Convergence criteria of the residuals is set as 1e-3 for continuity, x-velocity, y-velocity, z-velocity, k, and ω. For energy simulation convergence condition is reached if residual falls below 1e-6. Another aspect that is critical is that the results should be mesh independent. Refining the mesh further should not influence your results. To check for mesh independence, the same simulations are run multiple times with varying degrees of mesh refinement (different size mesh elements) if relative error of results are less than 5% solution is deemed mesh independent. Lastly, the computed y+ value should be less than 10% to model boundary layer accurately for SST modeling (Ω - based models in general). Results of the simulations for all three optimizations cases

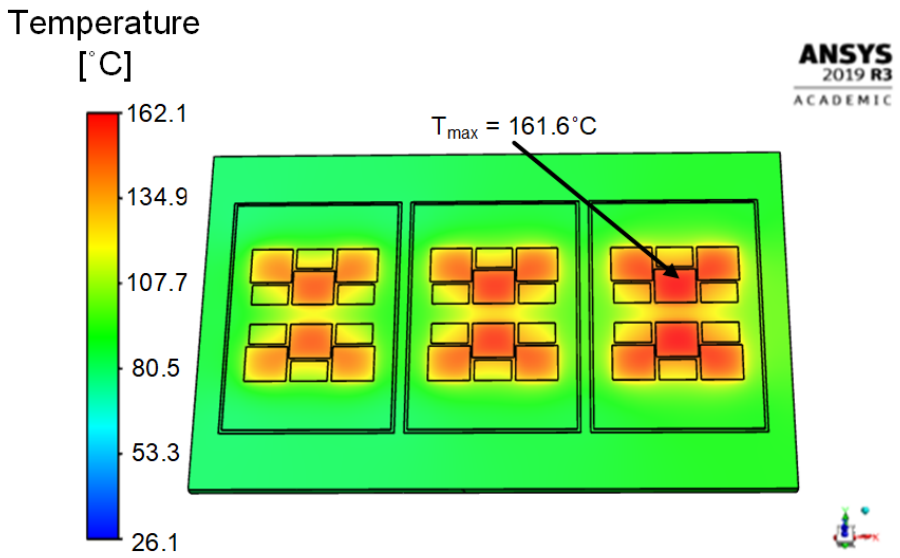
is conveyed next and used to verify efficacy of our optimization tool and methodology.

6.4.1 Benchmarking Pin Fin Geometry Simulation

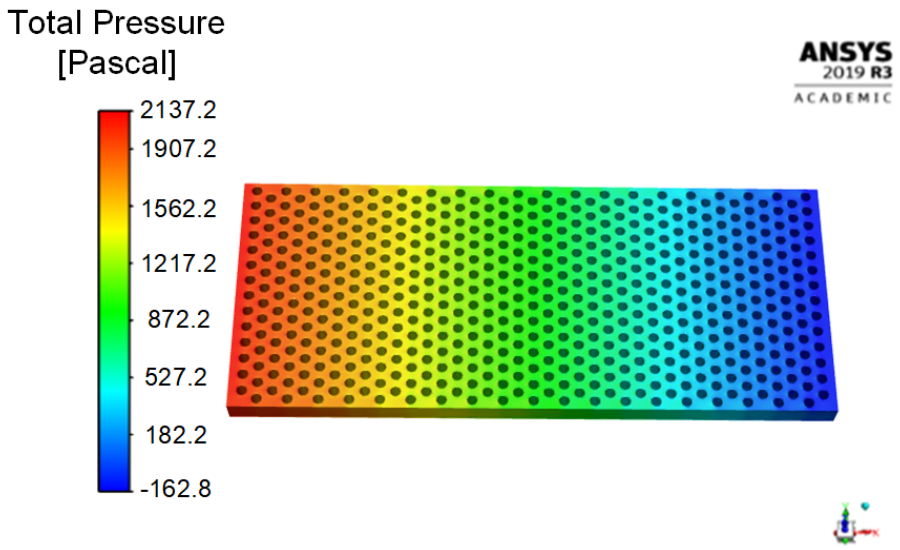
Simulation are run for the three cases using the original pin fin array that is integrated into the Hybrid Pack baseplate. The pin fin array is estimated to have pins with a 2.3 mm diameter, 6 mm length pin, and a pin distance factor of 1.8. There are 14 pins in the spanwise direction and 38 pins in the streamwise direction. These simulation results are used to later compare to the results of optimized geometry pin fin arrays designed by implementing our method.

Hybrid Pack Case 1: 5 LPM and 65^oC

Maximum Junction temperature of IGBT and diode dies is 161.60^oC and 142.16^oC, respectively. Total pressure drop between inlet to outlet is 2065.56 Pa.



(a) Temperature contour for benchmarking representative module (Case 1)

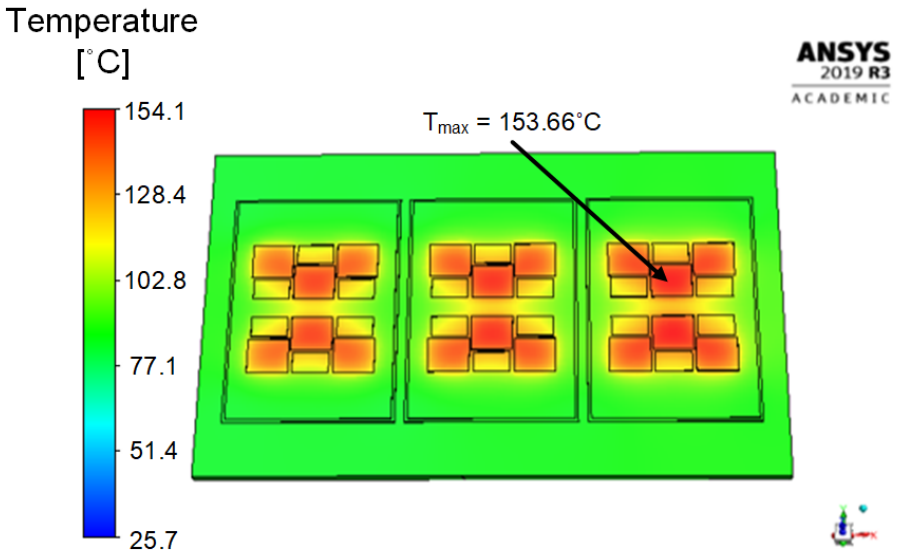


(b) Pressure contour for benchmarking representative module (Case 1)

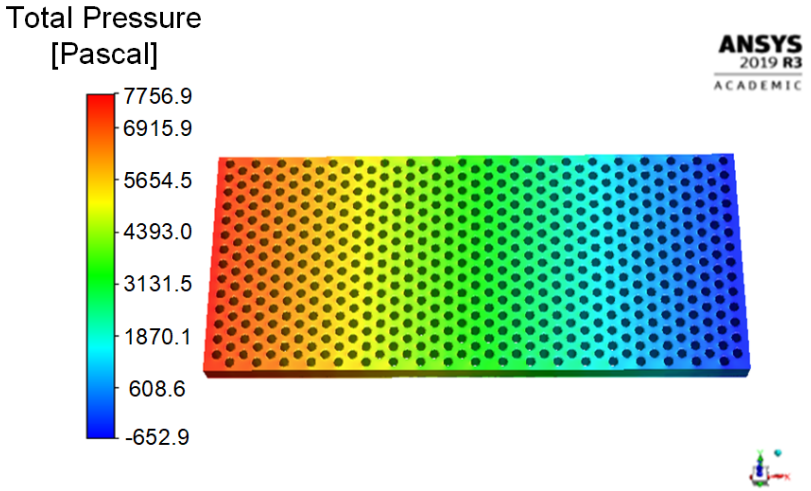
Figure 6.3: Contours of benchmarking representative module for inlet temperature 65^oC and a 5 LPM flow rate

Hybrid Pack Case 2: 10 LPM and 75^oC

Maximum Junction temperature of IGBT and diode dies is 153.66^oC and 134.29^oC, respectively. Total pressure drop between inlet to outlet is 7478.41 Pa.



(a) Temperature contour for benchmarking representative module (Case 2)

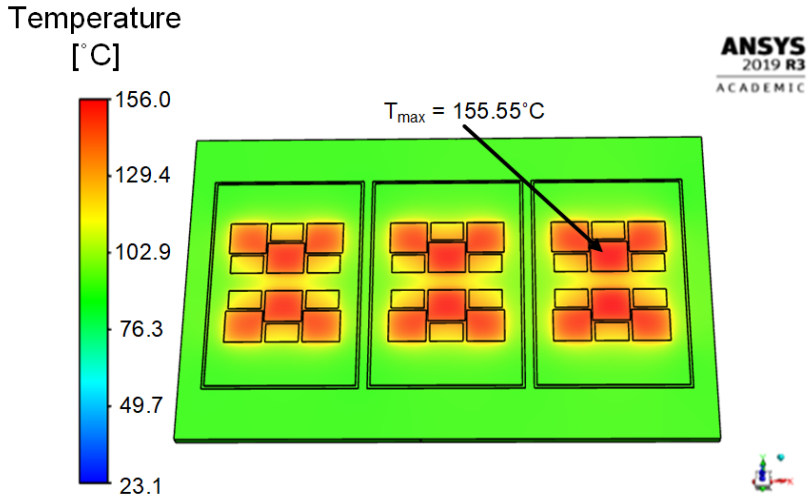


(b) Pressure contour for benchmarking representative module (Case 2)

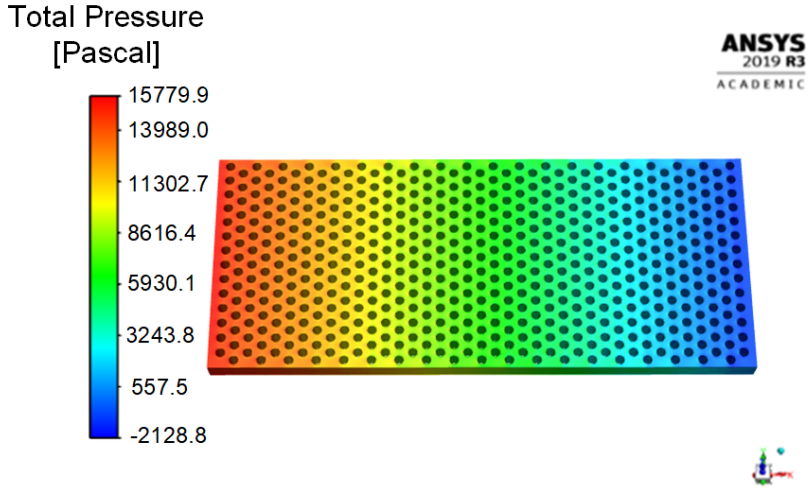
Figure 6.4: Contours of benchmarking representative module for inlet temperature 75^oC and a 10 LPM flow rate

Hybrid Pack Case 3: 15 LPM and 85^oC

Maximum Junction temperature of IGBT and diode dies is 155.55^oC and 136.28^oC, respectively. Total pressure drop between inlet to outlet is 15156.34 Pa.



(a) Temperature contour for benchmarking representative module (Case 3)



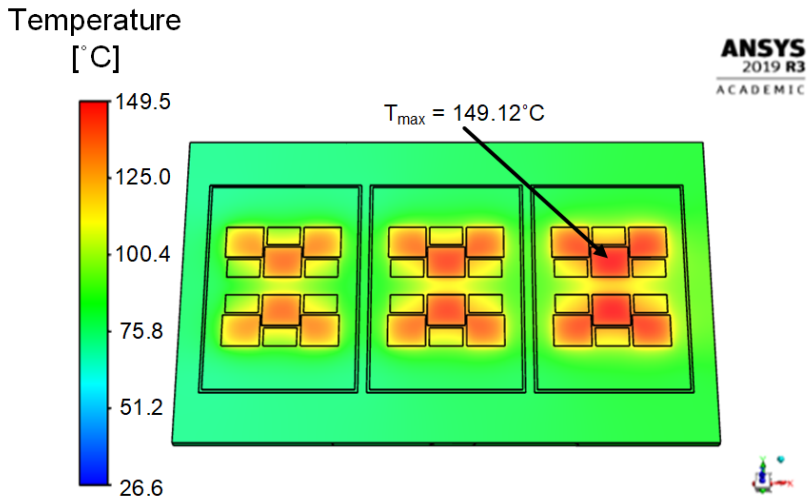
(b) Pressure contour for benchmarking representative module (Case 3)

Figure 6.5: Contours of benchmarking representative module for inlet temperature 85^oC and a 15 LPM flow rate

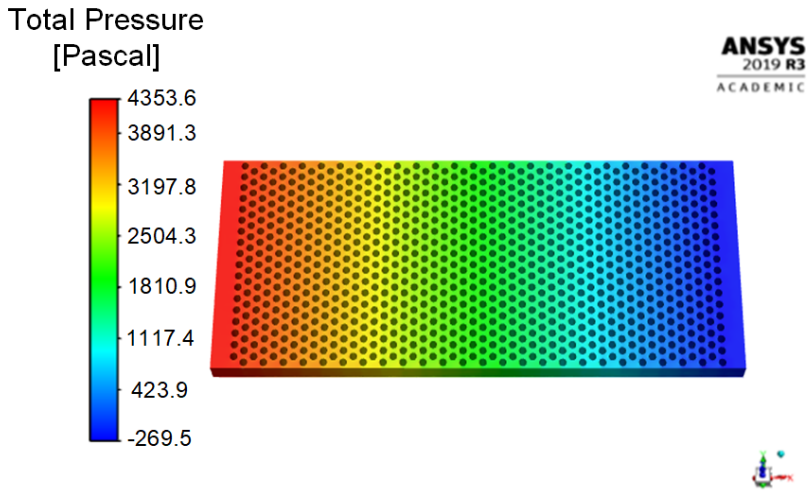
6.4.2 Optimized Pin Fin Geometry Simulation

Optimized Geometry Case 1: 5 LPM and 65^oC

Simulating this geometry of pin fin array the maximum junction temperature of IGBT dies and diode dies is found to be 149.11852 ^oC and 130.61774 ^oC, respectively. Temperature contour is provided below. Similarly, the total pressure drop was calculated in simulation from inlet to outlet to be 4290.3 Pa. Pressure contour of fluid domain is illustrated below.



(a) Temperature contour for optimized geometry (Case 1)



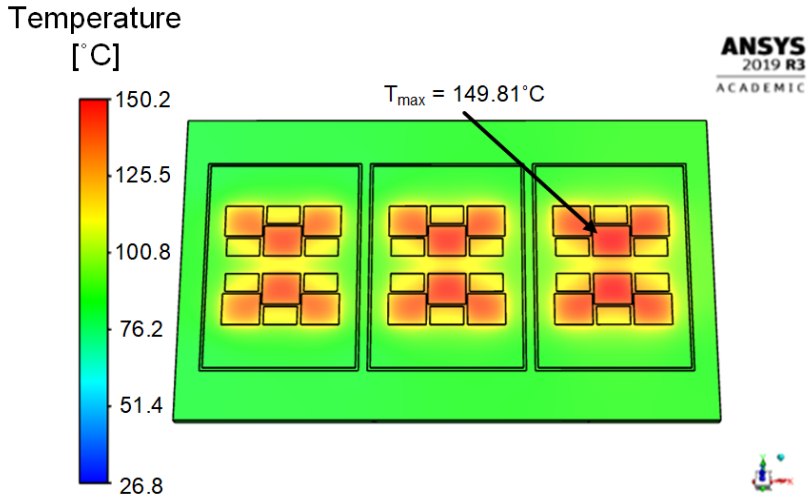
(b) Pressure contour for optimized geometry (Case 1)

Figure 6.6: Contours of optimized geometry for inlet temperature 65^oC and 5 LPM flow rate

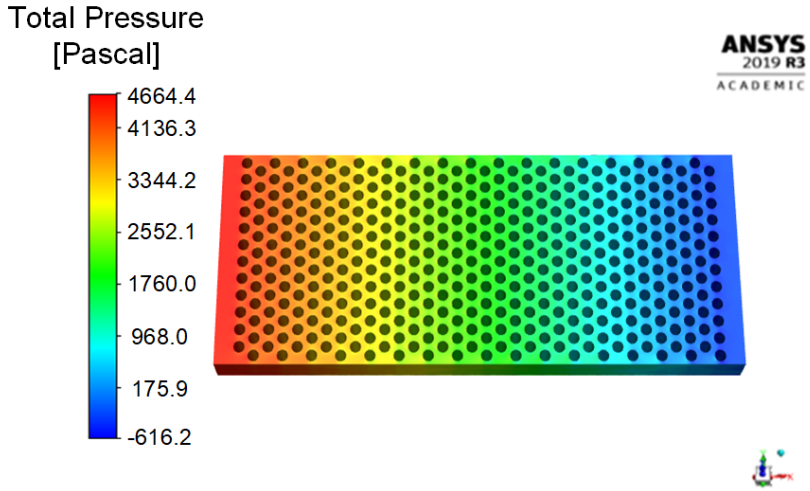
Optimized Geometry Case 2: 10 LPM and 75^oC

Maximum junction temperature of IGBT dies and diode dies is found to be 149.81 ^oC and 133.76 ^oC, respectively. Temperature contour is illustrated below. Simulations estimate total Pressure difference from inlet to outlet to be 4535.62 Pa. Pressure

contour of fluid domain is shown below. At the stagnation point of of first row the pressure is higher than at inlet, conversely, in wake region of most downstream pins pressure is lower than at outlet, this is expected.



(a) Temperature contour for optimized geometry (Case 2)

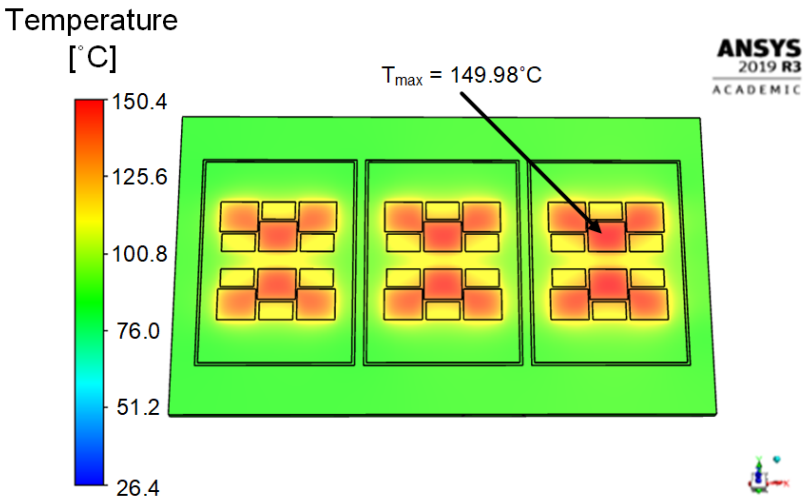


(b) Pressure contour for optimized geometry (Case 2)

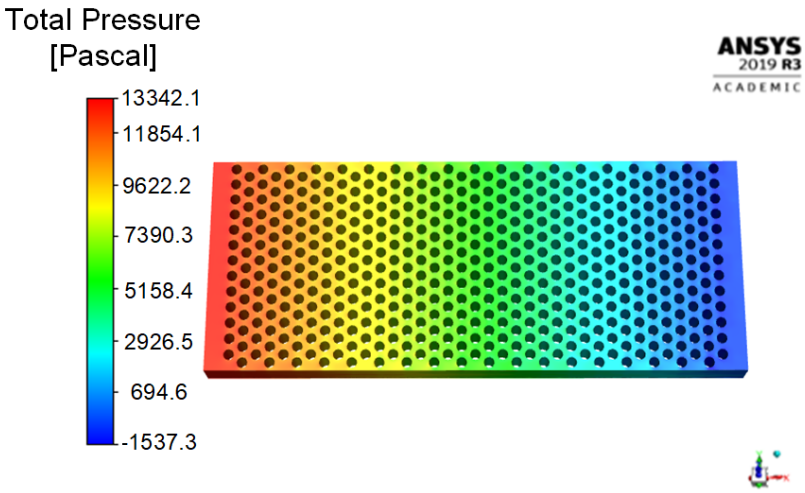
Figure 6.7: Contours of optimized geometry for inlet temperature 75^oC and 10 LPM flow rate

Optimized Geometry Case 3: 15 LPM and 85^oC

Simulating this geometry of pin fin array the maximum junction temperature of IGBT dies and diode dies is found to be 149.98 ^oC and 131.00 ^oC, respectively. Temperature contour is provided below. Similarly, the total pressure drop was calculated in simulation from inlet to outlet to be 12979.56 Pa. Pressure contour of fluid domain is illustrated below.



(a) Temperature contour for optimized geometry (Case 3)



(b) Pressure contour for optimized geometry (Case 3)

Figure 6.8: Contours of optimized geometry for inlet temperature 85^oC and 15 LPM flow rate

6.5 Discussion

For three different flow rates and inlet temperatures, the geometry of cylindrical pin fin array has been optimized. For the assumed inverter application, power losses were

calculated and a safety factor of 1.5 was employed. Using the FS380R12AT4B commercial power module the analysis was conducted changing only pin fins. Simulations were run on both the unmodified pin fin array of the representative Hybrid Pack and the optimized geometry that our tool outputted. It was made clear that optimizing a pin fin array for a given application results in superior performance. In addition our optimization tool is based on estimating the effective heat transfer coefficient for an array as well as the accompanying pressure drop; simulation results are thus compared to model's estimations to evaluate accuracy.

Summary of thermal performance:

Table 6.2: Summary of Results

	Case	$h_{eff,est}$ $[W/m^2K]$	$h_{eff,sim}$ $[W/m^2K]$	$T_{j,IGBT,est}$ $[^oC]$	$T_{j,IGBT,sim}$ $[^oC]$
Benchmarking Geometry	Case 1	15612.92	14180.83	157.19	161.6
	Case 2	21006.63	17786.67	147.51	153.66
	Case 3	24744.59	20642.47	149.63	155.55
Optimized Geometry	Case 1	22740.81	19040.0	142.93	149.12
	Case 2	22521.06	19687.5	145.17	149.81
	Case 3	29019.16	24468.75	145.09	149.98

It should be made clear that the estimated effective heat transfer calculated above

is not the one used in the optimization. Indeed the effective heat transfer used for optimization is 0.8 times the minimum effective heat transfer coefficient values given back in section 6.3.1. The reason for this is that in Armstrong et. al. [41], Vanfossen et. al.'s correlation is shown to predict the heat transfer coefficient of a set of experimental data in literature to ±20%. Only the IGBT die temperatures are considered because the diode dies max temperature is always found to be less, and thus the critical temperature is that of the IGBTs.

Table 6.3: Summary of Pressure Drop Modelling Accuracy:

	Case	ΔP_{est} $[Pa]$	ΔP_{sim} $[Pa]$
Benchmarking Geometry	Case 1	2031.48	2065.56
	Case 2	7120.14	7478.41
	Case 3	14577.56	15156.34
Optimized Geometry	Case 1	4096.58	4290.30
	Case 2	4645.79	4535.62
	Case 3	12530.78	12979.56

The relative error is calculated in terms of the simulated results. Below is a table enunciating the relative error in both pressure and effective heat transfer coefficient between the correlation based results and the simulated results.

Table 6.4: Accuracy of Both Thermal and Pressure Drop Models

	Case	$RE_{pressure}$ (%)	$RE_{h_{eff}}$ (%)	RE_{T_J} (%)
Benchmarking Geometry	Case 1	1.65	10.10	2.73
	Case 2	4.79	18.10	4.00
	Case 3	3.82	19.87	3.81
Optimized Geometry	Case 1	4.52	19.44	4.15
	Case 2	2.43	14.39	3.10
	Case 3	3.46	18.60	3.26

In terms of the effective heat transfer coefficient, the maximum relative error is found to be 19.87 %, less than 20% ,this is expected and consistent with the finding found in [41]. In terms of the pressure drop, the maximum relative error is 4.79 %. Similarly, for the temperature the maximum relative error is 4.15 %. The difference between error in effective heat transfer coefficient and temperature is due to the effect on heat spreading.

In terms of pin fin array performance, it is found that the representative benchmarking hybrid pack pin fin geometry does not achieve our stringent thermal requirements of keeping the junction temperature below the operating temperature of 150 ^oC. In contrast, the optimized geometry keeps the junction temperatures below the maximum operating temperature of 150^oC. Still for both case 2 and case 3 the pressure drop of the optimized pin fin geometry is lower than the representative module's

pin fin array geometry. This implies superior performance because it has higher heat transfer yet a lower pressure drop. For case 1, the pressure of optimized geometry is higher than the benchmarking geometry but has an inferior heat transfer capability.

6.6 Summary

A tool is developed capable of designing optimized pin fin array meeting the steady state thermal considerations of a two-level voltage source inverter using modular packaging. In this chapter the tool was implemented to design optimized pin fin array geometry for three different flow rates and inlet coolant temperatures. Simulations in ANSYS-fluent are conducted to evaluate the efficacy and accuracy of our design tool. Additionally, simulations were run for the original FS380R12AT4B with their integrated pin fins as reference. It was found that our tool was able to provide superior performance to that of the original (benchmarking) pin fin array of representative module.

Chapter 7

Conclusions and Future Work

This chapter begins by giving a recap of everything done. Afterwards, the contributions are of the work is presented. Lastly, promising future works related to this thesis are suggested.

7.1 Summary

A tool is developed to optimize pin fin array geometry of cylindrical pins with restrictions based on the experimental correlations found in literature. Thereby a suboptimal geometry for the pins defined by pin diameter, pin length, and distance between adjacent pins limited to equilaterally spaced staggered configurations. To verify the tool; the development was done based on a preexisting commercial IGBT-based hybrid pack, namely the FS380R12AT4B module. The chip layout and stack-up layers are unmodified, only the pin fin array geometry is altered such that results can be benchmarked. Further the development of tool was focused on two-level voltage

source inverters as to provide a comprehensive example. The thesis began by reviewing the operation of two-level voltage source traction inverters used for automotive electric drive-trains. By doing so the development of tool starts from first principles. of course this tool is not meant to be specific for inverters, exclusively, indeed for significant improvement in system efficiency this tool will enhance performance to a higher degree when applied to customized power module. For instance, chargers and DC-DC booster converters may be integrated into one module. Nevertheless, the proof of concept was done on a simple two-level voltage source inverter, as the tool is still in its preliminary stage.

After reviewing the basics of a two-level voltage source inverter's operations, the power loss that is generated during operation is explained. A method for calculating power losses from data supplied in data sheets is presented. The information found in data sheets is generated from a double pulse test, and this experimental setup and the transient behavior of switches is described in detail.

Pin fin technology relies on increasing the wetted surface area and inducing turbulence as to augment heat transfer, as with most thing there is a penalty here that comes in the form of pressure loss. Numerical and CFD-based optimization is very time and computationally extensive making it unpractical and unrealistic. To this end, many have come up with expirement based correlations as to describe the heat transfer and hydraulic resistance caused by pin fins. A detailed and comprehensive review is conducted on the most wholesome studies found in literature. Studies found in literature can be categorized into three topics; long tubes, short pin fins, and micro-pin fins. Of the three, short pin fins were considered advantageous and hence

used. Using the correlations in literature semi-analytical correlations based expressions were used to predict heat transfer and flow friction factor (pressure drop). Since these correlations were based on experiments it was ensured that the pin fin array was defined to be agreeable with these studies.Consequently, the distance between pins was limited to equalaterally spaced a distance ranging from 1.5 to 4 diameters apart. Also the length of pins was limited to ranging from 2 to 3 diameters long. The GA algorithm is then used to find the pin diameter, pin length, and distance between adjacent pins such that the effective heat transfer coefficient of array is larger than the minimum value possible while minimizing pressure drop. It is in this chapter that an assumed application is used to estimate worst-case power losses.

Lastly, using the chip layout and stack-up details of the FS380R12AT4B module along with the power losses calculated, the minimum value of effective heat transfer coefficient of array is found. A factor of 1.5 times the worst-case estimated power losses is employed as a safety margin. Running FEA simulations in ANSYS Steady-State Thermal Analysis allowed for finding the minimum value of heat transfer coefficient, by using a CAD model of the FS380R12AT4B Pack and applying a heat flux commensurate to the heat load based on 1.5 times the power losses onto the dies of module and ensuring that dies remain with junction temperature not exceed 150^oC operating temperature. Taking the minimum value of heat transfer coefficient at three different inlet coolant temperatures and flow rate the optimization tool find the optimal geometry of pin fin array. CFD-simulations were run in ANSYS-Fluent to verify our optimized geometries and the accuracy of our models therein, they were compared to the representative module with the original unaltered pin fins. It was found that the tool provided optimized geometry and that the models used therein

were accurate validating our methodology and tool.

7.2 Contributions

The main contributions of this thesis are enumerated herein. To achieve the objectives laid out by the DOE for EVs; multi-physics based modelling and optimization of power electronics along with further power electronics integration is required. Our thesis focuses on the thermal aspect as to address one of many aspects needed to push the mass market adoption of EVs.

The devoloped optimization tool focuses on pins of short aspect ratios as opposed to the majority of studies conducted on micro-pin fin arrays and long pin fins which have different thermal and hydraulic characteristics. The optimization tool is also developed in a comprehensive manner. Beginning with the operation of a two-level voltage source inverter, going through power losses, then finding minimum possible effective heat transfer coefficient value, and lastly optimizing geometry such that heat transfer is sufficient and pressure drop is minimized. This allows for customizable power modules. In contrast, most works focus on pin fins where a uniform heat load is applied to the top surface. Conversely, when the dies are the main generators of heat hot spots cause added complexity.

Our tool also specifically designs for a given application, a lot of studies or optimization is conducted in a general manner where the pin fins are designed according to a metric that compares heat transfer to pressure drop. This is not the best approach because at the end of the day the job of a heatsink is to dissipate the heat load, this comes first, then minimizing pressure drop is a critical yet secondary objective. In other word, if the heat load is not adequately dissipated reduced pressure drop

is of no consequence. When comparing pin fins to other heat transfer augmentation techniques both techniques ought to be optimized and the more advantageous technique is application dependent, therefore our tool can also facilitate this comparative study for future endeavors.

Another advantage of this tool is that it takes the inlet coolant temperature and flow rate as inputs. This is significant because the cooling mechanism of the traction inverter, or the drive-train's power electronics in general, must be compatible with cooling techniques of other components found in electrified vehicle. So both the inlet temperature and flow rate are dependent on system level requirement of vehicles.

7.3 Future Work

There are many directions in which this optimization tool could be expanded. Some of the directions this tool could be taken are presented next.

7.3.1 Heat Spreading Model

In this tool, ANSYS Steady-State Thermal Analysis is usued to find the minimum value possible for the effective heat transfer coefficient as to maintain junction temperatures below prescribed requirements. It is not the ideal method because it is done manually which can be tedious and labor-some. Alternatively, this could be modelled such that heat spreading and heat transfer coefficient are coupled and solved numerically. There is some works that study such modelling, for instance in [42] the 3-D heat diffusion equations are solved to estimate junction temperature of chips given heat load and baseplate temperature boundary conditions. A more coupled approach

where instead of assuming that baseplate temperature is some constant value, one could use an effective heat transfer coefficient. In this manner one could further optimize stack-up layer thicknesses and materials as well as the chip layout for a given application. However, steady-state thermal behaviour is only one aspect when it comes to the multi-physics nature of designing a module. Later, iteratively, other physics-based considerations could be modelled.

7.3.2 Transient Thermal Analysis

As was initially explained in introduction, when it comes to thermal requirements for reliability, there is the steady state thermal requirement of maintaining junction temperature below maximum value possible and thermal transient requirement of ensuring that module is resilient to the thermal cycling that takes place during operation. Materials of a module ought to have very close coefficients of thermal expansion to minimize the stresses and compression that occur during operations. In addition when designing for steady-state, designer is usually forced to use a safety factor giving an over-designed solutions. This is inconsistent with the need to push the technology to the ever increasing power density requirements desired. Transient thermal analysis can be integrated to design optimal stack-up layers and chip layout in terms of reliability and also can be used as to ensure cooling solution is not unnecessarily over-designed, that is if heat load profile could be estimated accurately there is no need for over design.

7.3.3 Vapor Chamber Baseplate

One of the advantages of pin fins is after the first few rows downstream the heat transfer coefficient remains constant, this allows for variable chip layouts with minimal modifications. One drawback is that the heat flux when applied on chips creates hot spots that must be compensated for, this causes a bottleneck for heat transfer. Furthermore, the heat transfer of pins, on a per pin basis, is most critical directly underneath the chips. To improve the heat transfer drastically, instead of using a solid copper baseplate with integrated pins it would be very favourable to use a copper-based vapor chamber with integrated pins that can distribute the heat uniformly over the entirety of the pin fin array. Costs will be increased but the power rating will also be increased so there is potential here, requires study. Today vapor chamber heat distribution techniques is found in abundance in things like laptops and desktops.

7.3.4 Cooling techniques Studies

In this thesis a methodology for optimizing cylindrical pin fins has been presented. Thereby, it is feasible to design pin fins for power modules that are optimal or sub-optimal. Similarly, if other cooling techniques are optimized for, then comparative studies including pin fins have more conclusive results. So, this tool can also assist in comparing cooling strategies.

7.3.5 Empirical Correlation Improvements

Our optimization tool is based on empirical correlations, however as the experiments conducted to derive the correlations were limited the scope of the empirical correlation is limited. For instance, for our tool the geometry was limited to equilaterally

spaced pins. Also, for short pin fins the correlation is accurate to ±20% for heat transfer. Further improvement of accuracy will result in potentially improves solutions. Therefore, more comprehensive and accurate studies would result in potentially improved solutions. With more comprehensive correlations, the tool may no longer be restricted to equalaterally spaced pins or pins with uniform diameters and lengths.

References

[1] B. Bilgin, P. Magne, P. Malysz, Y. Yang, V. Pantelic, M. Preindl, A. Korobkine, W. Jiang, M. Lawford, and A. Emadi, "Making the case for electrified transportation," *IEEE Transactions on Transportation Electrification*, vol. 1, no. 1, pp. 4–17, 2015.

[2] A. Emadi, *Advanced electric drive vehicles*. CRC Press, 2014.

[3] "U.s. drive electrical and electronics technical team roadmap," U.S. Department of Energy, Washington, DC, USA, Report, Jun. 2013.

[4] "U.s. drive electrical and electronics technical team roadmap," U.S. Department of Energy, Washington, DC, USA, Report, Oct. 2017.

[5] P. Fabis, D. Shum, and H. Windischmann, "Thermal modeling of diamond-based power electronics packaging," in *Fifteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (Cat. No. 99CH36306)*. IEEE, 1999, pp. 98–104.

[6] S. S. Anandan and V. Ramalingam, "Thermal management of electronics: A review of literature," *Thermal science*, vol. 12, no. 2, pp. 5–26, 2008.

[7] M. Musallam and C. M. Johnson, "Real-time compact thermal models for health management of power electronics," *IEEE Transactions on Power Electronics*, vol. 25, no. 6, pp. 1416–1425, 2010.

[8] K. O. L. P. Ole Mühlfeld, Rüdiger Bredtmann, "Compact power module for integrated traction inverters with highest power density," *Proc. APEC*, pp. 2420–2423, 2015.

[9] K. K. Prabhakar, M. Ramesh, A. Dalal, C. U. Reddy, A. K. Singh, and P. Kumar, "Efficiency investigation for electric vehicle powertrain with variable dc-link bus voltage," in *IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society*. IEEE, 2016, pp. 1796–1801.

[10] T. Schoenen, M. S. Kunter, M. D. Hennen, and R. W. De Doncker, "Advantages of a variable dc-link voltage by using a dc-dc converter in hybrid-electric vehicles," in *2010 IEEE Vehicle Power and Propulsion Conference*. IEEE, 2010, pp. 1–5.

[11] S. Tenner, S. Gimther, and W. Hofmann, "Loss minimization of electric drive systems using a dc/dc converter and an optimized battery voltage in automotive applications," in *2011 IEEE Vehicle Power and Propulsion Conference*. IEEE, 2011, pp. 1–7.

[12] D. Kok, A. Morris, and M. Knowles, "Novel ev drive train topology — a review of the current topologies and proposal for a model for improved drivability," 09 2013, pp. 1–10.

[13] X. Pei, W. Zhou, and Y. Kang, "Analysis and calculation of dc-link current and voltage ripples for three-phase inverter with unbalanced load," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5401–5412, 2014.

[14] X. Lu, H. Cha, and F. Z. Peng, "Optimizing capacitance in spwm converter/inverter for series hybrid electric bus systems," in *2009 IEEE Vehicle Power and Propulsion Conference*. IEEE, 2009, pp. 852–858.

[15] B. P. McGrath and D. G. Holmes, "A general analytical method for calculating inverter dc-link current harmonics," *IEEE Transactions on Industry Applications*, vol. 45, no. 5, pp. 1851–1859, 2009.

[16] X. Lu and F. Z. Peng, "Minimizing dc capacitor current ripple and dc capacitance requirement of the hev converter/inverter systems," in *2009 IEEE Energy Conversion Congress and Exposition*. IEEE, 2009, pp. 1191–1198.

[17] P. A. Dahono, Y. Sato, and T. Kataoka, "Analysis and minimization of ripple components of input current and voltage of pwm inverters," *IEEE Transactions on Industry Applications*, vol. 32, no. 4, pp. 945–950, 1996.

[18] J.-S. Lai, H. Kouns, and J. Bond, "A low-inductance dc bus capacitor for high power traction motor drive inverters," in *Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No. 02CH37344)*, vol. 2. IEEE, 2002, pp. 955–962.

[19] B. Wu and M. Narimani, *High-power converters and AC drives*. John Wiley & Sons, 2017.

[20] J. Guo, "Modeling and design of inverters using novel power loss calculation and dc-link current/voltage ripple estimation methods and bus bar analysis," Ph.D. dissertation, 2017.

[21] K. Bimal, *Modern power electronics and AC drives*. Prentice-Hall, 2001.

[22] A. Volke, J. Wendt, and M. Hornkamp, *IGBT modules: technologies, driver and application*. Infineon, 2012.

[23] B. Backlund, R. Schnell, U. Schlapbach, R. Fischer, and E. Tsyplakov, "Applying igbts," *ABB. Semiconductors*, 2007.

[24] Y. Lobsiger, "Closed-loop igbt gate drive and current balancing concepts," Ph.D. dissertation, ETH Zurich, 2014.

[25] R. Schnell and U. Schlapbach, "Realistic benchmarking of IGBT-modules with the help of a fast and easy to use simulation-tool," in *PCIM proceedings*, 2004.

[26] "Dimensioning program IPOSIM for loss and thermal calculation of Infineon IGBT modules," Infineon Technologies AG, Tech. Rep., 2008.

[27] D. Metzger, Z. Fan, and W. Shepard, "Pressure loss and heat transfer through multiple rows of short pin fins," in *International Heat Transfer Conference Digital Library*. Begel House Inc., 1982.

[28] M. Jakob, "Heat transfer and flow resistance in cross flow of gases over tube bank," *Trans. ASME*, vol. 60, p. 384, 1938.

[29] E. Grimson, "Correlation and utilization of new data on flow resistance and heat transfer cross-flow of gases over tube banks," *Trans. ASME*, vol. 59, pp. 583–594, 1937.

[30] G. Theoclitus, "Heat-transfer and flow-friction characteristics of nine pin-fin surfaces," 1966.

[31] A. Žukauskas, "Heat transfer from tubes in crossflow," in *Advances in heat transfer*. Elsevier, 1972, vol. 8, pp. 93–160.

[32] G. J. VanFossen, "Heat-transfer coefficients for staggered arrays of short pin fins," 1982.

[33] B. Brigham and G. VanFossen, "Length to diameter ratio and row number effects in short pin fin heat transfer," 1984.

[34] R. Simoneau and G. Vanfossen Jr, "Effect of location in an array on heat transfer to a cylinder in crossflow," *NASA STI/Recon Technical Report N*, vol. 82, p. 19493, 1982.

[35] D. Metzger and S. Haley, "Heat transfer experiments and flow visualization for arrays of short pin fins," in *Turbo Expo: Power for Land, Sea, and Air*, vol. 79597. American Society of Mechanical Engineers, 1982, p. V004T09A007.

[36] D. Metzger, R. Berry, and J. Bronson, "Developing heat transfer in rectangular ducts with arrays of short pin fins," *American Society of Mechanical Engineers*, 1981.

[37] D. Metzger, W. Shepard, and S. Haley, "Row resolved heat transfer variations in pin-fin arrays including effects of non-uniform arrays and flow convergence,"

in *Turbo Expo: Power for Land, Sea, and Air*, vol. 79313. American Society of Mechanical Engineers, 1986, p. V004T09A015.

[38] W. Damerow, J. Murtaugh, and F. Burggraf, "Experimental and analytical investigation of the coolant flow characteristics in cooled turbine airfoils," 1972.

[39] B. Agostini, M. Fabbri, J. E. Park, L. Wojtan, J. R. Thome, and B. Michel, "State of the art of high heat flux cooling technologies," *Heat Transfer Engineering*, vol. 28, no. 4, pp. 258–281, 2007.

[40] A. C. Kheirabadi and D. Groulx, "Cooling of server electronics: A design review of existing technology," *Applied Thermal Engineering*, vol. 105, pp. 622–638, 2016.

[41] J. Armstrong and D. Winstanley, "A review of staggered array pin fin heat transfer for turbine cooling applications," 1988.

[42] J. Reichl, J. M. Ortiz-Rodriguez, A. Hefner, and J.-S. Lai, "3-d thermal component model for electrothermal analysis of multichip power modules with experimental validation," *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3300–3308, 2014.

[43] H. Cui, F. Hu, Y. Zhang, and K. Zhou, "Heat spreading path optimization of igbt thermal network model," *Microelectronics Reliability*, vol. 103, p. 113511, 2019.

[44] X. Liu, G. Tian, Y. Chen, H. Luo, J. Zhang, and W. Li, "Non-contact degradation evaluation for igbt modules using eddy current pulsed thermography approach," *Energies*, vol. 13, no. 10, p. 2613, 2020.

[45] M. Du, Q. Guo, Z. Ouyang, K. Wei, and W. G. Hurley, "Effect of solder layer crack on the thermal reliability of insulated gate bipolar transistors," *Case Studies in Thermal Engineering*, vol. 14, p. 100492, 2019.

[46] H. S. Dow, W. S. Kim, and J. W. Lee, "Thermal and electrical properties of silicon nitride substrates," *AIP Advances*, vol. 7, no. 9, p. 095022, 2017.

[47] P. Semiconductors, "Application manual power semiconductors."

[48] A. R. Hefner, "An improved understanding for the transient operation of the power insulated gate bipolar transistor (igbt)," in *20th Annual IEEE Power Electronics Specialists Conference*. IEEE, 1989, pp. 303–313.

[49] E. Hudlicka, "This time with feeling: Integrated model of trait and state effects on cognition and behavior," *Applied Artificial Intelligence*, vol. 16, no. 7-8, pp. 611–641, 2002.