# Reliability Improvement of Regenerative Cascaded H-bridge (CHB) Medium-Voltage Drive

# RELIABILITY IMPROVEMENT OF REGENERATIVE CASCADED H-BRIDGE (CHB) MEDIUM-VOLTAGE DRIVE

BY

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*To God*

*, and my family*

# ABSTRACT

High power converters are widely used in many industries. At power levels in the range of Mega Watt (MW), power conversion at medium voltage (MV) is preferred due to better efficiency and lower cost. For medium voltages applications, multilevel converters are widely adopted due to the features they offer with respect to two-level converters. Cascaded H-bridge topology is a widely adopted multilevel topology because of its modularity, scalability, and reliability. The conventional cascaded H-bridge topology allows two-quadrant operation. In order to allow four-quadrant operation, an active front end version of the cascaded H-bridge topology has been proposed in literature and recently commercialized.

In the field, power converters operates under harsh loading and environmental conditions. The resulting stresses imposed on converter components cause their gradual degradation. In cascaded H-bridge converters, typically power cell components such as power modules, DC-bus capacitors, and control PCBs are

highly stressed. Under these stresses power cell components degrade and require replacement in the field, otherwise unexpected failures may occur.

The thesis aim is to address power cell components reliability through proposing novel regenerative cascaded H-bridge converter control schemes to reduce components stresses and failure probability without increasing size, cost, or complexity. First, a novel PWM active front end control scheme has been proposed to reduce the inherent ripple current stresses on the DC-bus capacitors. Second, the thesis proposes a novel grid or near grid switching frequency front end control scheme to reduce stresses on power modules and the power cell cooling requirements. Third, novel cascaded H-bridge front end control schemes are proposed to reduce the sensor count, thereby decreasing failure rate and cutting down cost. The proposed work has been thoroughly validated through detailed 9-cell regenerative cascaded H-bridge system simulation and experimentation.

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# Chapter 1

# Introduction

## 1.1. Motivation

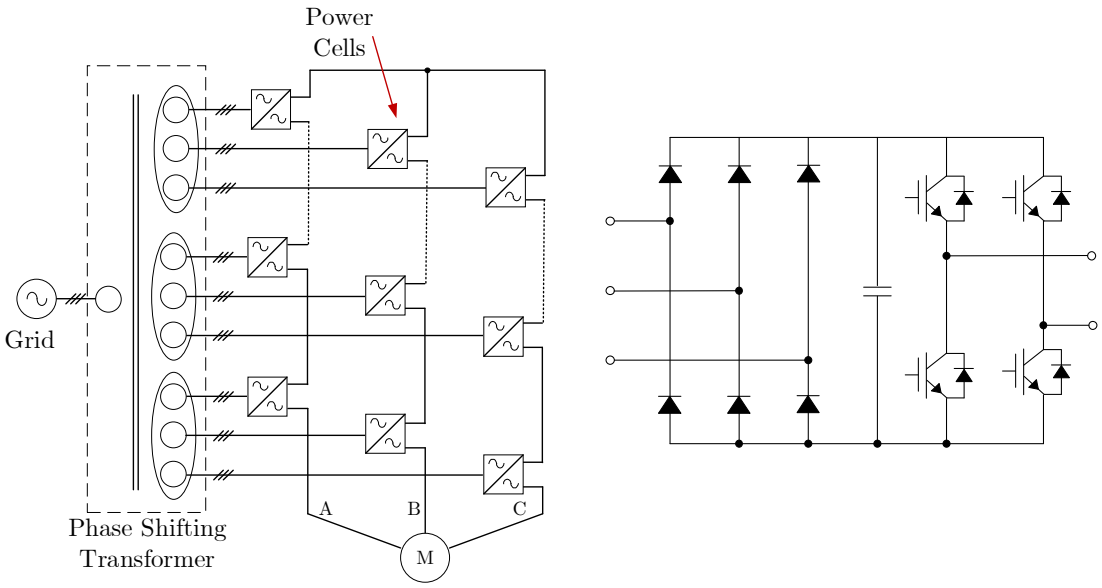
High power converters are widely used in many industries, such as oil and gas, chemical and petrochemical, mining, metal, cement, power generation and utility, water treatment, marine propulsion, railway traction, special machinery, etc [1]. In most of these industries, the main application of power converters is motor drives, in which they are used to control the torque and the speed of the electric machine by controlling the fixed voltage and frequency provided by the utility line [1].

Voltage source topologies dominate the high power converter market. High power voltage sources converters can be categorized into two-level converters and multilevel converters. For power levels in the range of Mega Watt (MW), nominal currents reach levels where power conversion at medium voltages is more efficient than at low voltages [2].

At medium voltages, multilevel converters are widely adopted due to the features they offer with respect to two-level converters such as reduction in the total harmonic distortion of output AC voltage waveforms, switching losses, $(dv/dt)$ voltage stresses [2]. Cascaded H-bridge (CHB) [2, 6, 7], Neutral point clamped (NPC) [2, 6, 7], and Modular multilevel (MMC) [2, 6, 7] are examples of widely adopted multilevel converter topologies, which are offered by several manufacturers in medium voltage power conversion market [8-17].

Because of its near sine output AC waveform, modularity, scalability, ease of maintenance, and fault tolerant capability; CHB converters are widely offered by almost all the manufacturers [18-28]. The conventional CHB topology is composed of multiple isolated H–bridges power cells with diode front ends (DFE). The H-bridges are connected in series to synthesize the required medium voltage as shown in Fig. 1.1 [28].

DFE power cells allows the CHB drives to operate in two quadrants. This does not cover industrial drive applications which require braking capability such as fast braking of high inertia fans or negative torque capability such as downhill conveyors as shown in Fig. 1.2 [29-33]. In order to allow regeneration capability in CHB topology, diode front-ends (DFE) are replaced with active front-ends (AFE) in power cells as shown in Fig. 1.3 [34-38].




(a) Topology (b) Conventional Power Cell

Fig. 1.1 Conventional CHB Converter in Drives Application [29-33]

Fig. 1.2 Downhill Conveyor System [1].

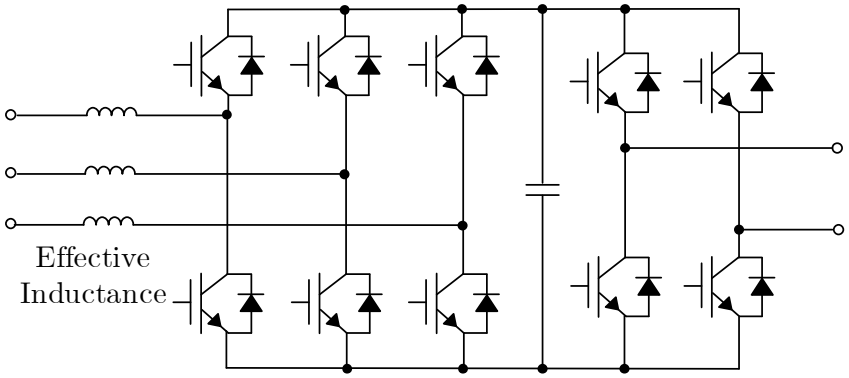



Fig. 1.3 Regenerative CHB Converter Power Cell Equipped with AFE [34-38].

Although various power cell topologies have been proposed in literature [34-42], the first CHB drives with regenerative capability have been introduced in the market recently [39]. This has opened the door for CHB converters to compete strongly against other converter topologies in regenerative market segment

Typically, medium voltage power converters in general and motor drives in specific operate under harsh loading and environmental conditions [43]. Accordingly, degradation and failures take place in the field. Failures may result in

extended down times and production loss, property loss, or safety hazard situations. Typically, a converter fault or failure results from a fault or a failure in its components and these faults and failures are attributed to overstress and gradual wear-out [43]. Commonly, components overstress arise from the unexpected loading conditions either related to the grid or the load, or related to system issues such as control system or ventilation system issues [43-56]. Effective protection schemes are employed to limit the possibility of these overstress events. Regarding components wear-out, various factors such as converter topology, application, and field conditions play an important role in accelerating wear-out, which compromises converters long-term reliability [43-57] According to field failure surveys, thermal stresses are the main cause for converters' components degradation followed by humidity, and contamination [45].

Considering CHB converters, high portion of converter faults are attributed to power cell failures, significant portion of these failures are due to overstress of power semiconductors, DC-bus capacitors, and other power cell components such as gate drivers, and cell controllers [28-30, 57-109]. Aside from overstress, the long-term reliability of the power cell components is crucial as stresses imposed on power cell components are intense. The reason is that power cell components are densely packed inside the cell and are required to operate under demanding conditions [33,

59, 61]. In addition, the specifics of the CHB topology add more stresses on power cell components such as DC-bus capacitors [58].

Addressing these power cell long-term reliability challenges is of a significant importance practically and academically as it helps reducing down times, production loss, maintenance costs, in addition to prevention of catastrophic failures. Addressing reliability issues is performed either in design stage or in field operation [45, 110-120]. At design stage, better designs that suffer less stresses and as a result less degradation effects are been searched for [45, 110-116]. At the field, the aim is to prevent failures before happening through tracking converters' conditions [117-120].

## 1.2. Research Objectives and Challenges

The thesis work focuses on addressing regenerative CHB topology reliability during design stage through developing novel front ends control schemes to:

1. Reduce components stresses to improve long-term reliability
2. Reduce component count to reduce failure random probability
3. Other system benefits (e.g., Cost, Size)

The significant reliability challenges facing typical regenerative power cells to be covered in the thesis work are as follows:

1. Capacitors are one of the most vulnerable components in the power converters [45-47, 83]. This vulnerability is more critical in the CHB topology. In order to achieve the required total energy storage, cost-effective high-capacitance capacitor technologies such as Aluminum electrolytic are employed [83-85]. This capacitor technology degrades in an accelerated fashion under ripple current stresses. Accordingly, CHB drives manufacturers are required to employ stringent preventive maintenance routines to prevent unscheduled downtime caused by DC-buses capacitors degradation [28, 58-60]. One solution is to reduce these stresses is through increasing the capacitance value; however, this leads to increase in power cell size and cost.

2. Typical active front ends employ sinusoidal PWM modulators to satisfy grid connection harmonic requirements. Commonly switching frequency is set up to 2 kHz to 4 kHz [32, 34-38]. On one side, this reduces additional cell input filter requirements. On the other side, this leads to increased switching losses of power devices resulting in high cycling temperature stresses on power devices, which degrades the mechanical packaging of power switches, and eventually leads to power switches failures [77, 78].

One solution is to increase the heat sinks and cooling requirements; however, this leads to increase in power cell and system size, and cost.

3. The conventional active front end control employs AC voltage sensing for grid synchronization, current sensing for current control and DC voltage sensing for DC-bus voltage regulation [34-38]. Scaling up these sensing requirements to n-cells per phase CHB drive results in a huge addition of circuitry in comparison to the DFE CHB topology, which increases random failure probabilities.

   In addition, transmitting these additional measurement signals to a centralized control as in the case of DFE CHB is not practical, therefore, cell based AFE controller implementation is the preferred option. However, embedding additional sensing and control circuitry to the densely-packed power cell operating in harsh conditions compromises power cell's circuitry reliability. To mitigate possible reliability issues, one solution is to employ larger size or higher cost power cell designs, which is practically undesirable.

## 1.3. Contributions

This thesis focuses on improving the power cell reliability of the regenerative CHB drive. The author has contributed to several original developments, which are presented in the thesis and briefly summarized as follows:

1. A regenerative 9-cell CHB drive experimental setup has been developed for testing and validation.

2. A novel AFE controller with pulsating power flow control to reduce thermal stresses induced by ripple currents in DC-bus capacitors.

3. A novel front end based on grid or near grid frequency switching to reduce thermal stresses induced by high switching frequency in switches and reduce heat sink size.

4. A novel front end control to reduce sensors count and minimize modification for the existing diode front ends through centralized control.

In addition to the thesis work, the author has participated in other industrial research projects.

Below is a list of the journal and conference papers, and patents generated from the thesis work or other related research projects:

**Journal Papers:**

[J1] **A. Abuelnaga**, M. Narimani and A. S. Bahman, "A Review on IGBT Module Failure Modes and Lifetime Testing", IEEE Access, vol. 9, pp. 9643-9663, 2021.

[J2] **A. Abuelnaga**, M. Narimani, and A. S. Bahman, "Power electronic converter reliability and prognosis review focusing on power switch module failures", J. Power Electron. 21, 865–880, 2021.

[J3] Z. Ni, **A. Abuelnaga**, and M. Narimani "A Novel High-Performance Predictive Control Formulation for Multilevel Inverters", IEEE Transactions on Power Electronics, vol. 35, no. 11, pp. 11533 - 11543, 2020.

[J4] Z. Ni, **A. Abuelnaga**, and M. Narimani "A New Fault-Tolerant Technique based on Non-Symmetry Selective Harmonic Elimination for Cascaded H-Bridge Motor Drives", in IEEE Transactions on Industrial Electronics, vol. 68, no. 6, pp. 4610-4622, 2021.

[J5] Z. Ni, **A. Abuelnaga**, S. Yuan, S. Badawi, M. Narimani, Z. Cheng, and N. Zargari, "A New Approach to Input Filter Design for Regenerative Cascaded-H-Bridge (CHB) Drives", in IEEE Transactions on Industrial Electronics, Early Access.

[J6] Z. Ni, **A. Abuelnaga**, S. Badawi, S. Yuan, M. Narimani, N. Zargari, "DC-link Voltage Ripple Control of Regenerative CHB Drives for Capacitance Reduction", in IEEE Transactions on Industrial Electronics, Early Access.

[J7] S. Yuan, Z. Ni, **A. Abuelnaga**, S. Badawi, M. Narimani, and N. Zargari, "A New Method to Reduce Current Harmonics of DC-link Capacitors in Grid-tied Cascaded H-bridge Converters, " submitted to IEEE Transaction on Industry Application, under review.

[J8] S. Badawi, **A. Abuelnaga**, Z. Ni, S. Yuan, M. Narimani, Z. Cheng, N. Zargari, "Reduced Switch-Count Topology for Regenerative Cascaded H-Bridge (CHB) Medium-Voltage Drives", submitted to IEEE Transaction on Power Electronics, under review.

[J9] M. Norambuena, F. Carnielutti, A. Mokhtar, M. Narimani, Z. Ni, and **A. Abuelnaga**, "Finite Control Set Model Predictive Control for Multilevel Converters with Reduced Switching Frequency", submitted to IEEE Transaction on Industrial Electronics, under review.

[J10] **A. Abuelnaga**, Z. Ni, S. Badawi, S. Yuan and M. Narimani, "A New AFE Control for Pulsating Power Flow for Regenerative CHB Drives", IEEE Transactions on Industrial Electronics. (to be submitted)

[J11] **A. Abuelnaga**, Z. Ni, S. Badawi, S. Yuan, and M. Narimani "A New Front End Based on Grid or Near Grid Frequency Switching for Regenerative CHB Drives", IEEE Transactions on Industrial Electronics. (to be submitted)

[J12] **A. Abuelnaga**, Z. Ni, S. Badawi, S. Yuan, and M. Narimani "A Reduced Sensor Count Front End Control Scheme for Regenerative CHB Drives", IEEE Transactions on Industrial Electronics. (to be submitted)

**Conference Papers:**

[C1] **A. Abuelnaga**, M. Narimani, M. Chis, K. Kandasamy and N. R. Zargari, "Investigation of a Reduced Cost Solution to Implement Integrated Safe Torque-OFF Function in Cascaded H-Bridge Induction Motor Drives", in IEEE Energy Conversion Congress and Exposition (ECCE), pp. 2982-2987, 2020.

[C2] **A. Abuelnaga** and M. Narimani, "Open Circuit IGBT Fault Classification using Phase Current in a CHB Converter", IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, pp. 4636-4641, 2019.

**Patents:**

[P1] **A. Abuelnaga**, Z. Ni, M. Narimani, Z. Cheng, and N. Zargari, "CAPACITOR SIZE REDUCTION AND LIFETIME EXTENSION FOR CASCADED H-BRIDGE DRIVES", US2021091681A1.

[P2] **A. Abuelnaga**, M. Narimani, Z. Cheng, and N. Zargari, "REGENERATIVE MEDIUM VOLTAGE DRIVE (CASCADED H BRIDGE) WITH REDUCED NUMBER OF SENSORS", (Filed RA Patent)

[P3] **A. Abuelnaga**, M. Narimani, Z. Cheng, and N. Zargari, "SYSTEMS AND METHODS OF MULTI-MOTOR REGENERATIVE DRIVE", (Filed RA Patent)

## 1.4. Thesis Outlines

The thesis structure is as follows:

Chapter 2 provides a review on medium voltage converters topologies in general and cascaded H-bridge converter in particular.

Chapter 3 presents a review on failures and reliability of cascaded H-bridge converters. First, it discusses field failures of medium voltage converters followed by field failure of cascaded H-bridge converter. Then it discusses long-term reliability issues arising in CHB power cell due to the degradation of power semiconductor modules, DC-bus capacitors, and signal PCBs.

Chapter 4 discusses the experimental implementation of a scaled-down version of a 7-level regenerative CHB drive. The discussion covers both the hardware and the firmware aspects of the setup.

Chapter 5 introduces power cell inherent power unbalance and the consequent impact of ripple currents on DC-bus capacitors lifetime. Subsequently, it discusses the specifics of design new AFE controller with pulsating power flow capability. This part includes the theory and the state-of the art, a discussion about multi-frame of reference current control, and a discussion about pulsating power angle estimation. Afterwards, the proposed AFE control structures involving the proposed multi-frame of reference current control and the proposed pulsating power

angle estimator are illustrated in details. Finally, simulation and experimental validation are provided.

Chapter 6 reviews the conventional PWM-based AFE control and consequent thermal stresses, power switches lifetime, and cooling requirements. Afterwards, it discusses the specifics of designing a new front end based on grid or near grid frequency switching. This part includes the theory and the state-of the art, and a discussion about integration to the phase shifting transformer. Then, the proposed novel front end control structures involving a proposed asymmetric delay angle control and a proposed voltage angle control are illustrated in details. Finally, simulation and experimental validation is provided.

Chapter 7 reviews sensors and communication links requirements for the conventional AFE, with either centralized or decentralized CHB front end control schemes. Then, it discusses the specifics of designing a new CHB front end with reduced sensor count. This part includes front ends input voltage sensors and input current sensors elimination. Afterwards, a proposed novel centralized CHB front end control structure involving a proposed AFE-based control with front ends input voltage measurements elimination, a proposed AFE-based control with front ends input current measurements elimination, and a proposed grid switching frequency

AFE-based control with front ends input measurements elimination are discussed in details. Finally, simulation and experimental validation are provided.

Chapter 8 provides conclusions of the thesis and the future work.

# Chapter 2

# Medium-Voltage Converters and Motor Drives

This chapter presents an overview on high power converters in general with focus on cascaded H-bridge topology in motor drives applications.

## 2.1. Variable Frequency Motor Drives

High power converters serve in converting power from AC to DC and DC to AC in many industries such as oil and gas, chemical and petrochemical, mining, metal, cement, power generation and utility, water treatment, marine propulsion, railway traction, etc. [1]. In these industries, power converters are utilized in different

applications including pumps, fans, compressors, conveyors, hoists, extruders, mills, reactive power compensation, utility energy storage, wind power generation, oil tankers, container ships, high-speed trains, locomotives, etc. [1]. Most of these applications involve electromechanical energy conversion, thereby; they use electric motors or generators. In these applications, the role of the power converter is to control the torque and the speed of the electric machine by manipulating the fixed voltage and frequency provided by the utility line and providing variable voltage and frequency to the electric machine. Accordingly, process goals such as controlling the fluid flow in a pump or the power generated from a wind turbine is achieved. Commonly, power converters that control motors in a process are referred to as variable-frequency drive (VFD) or motor drives. Fig. 2.1 shows an illustration for a motor drive in an industrial process. A more detailed illustration of the motor drive components is shown in Fig. 2.2.

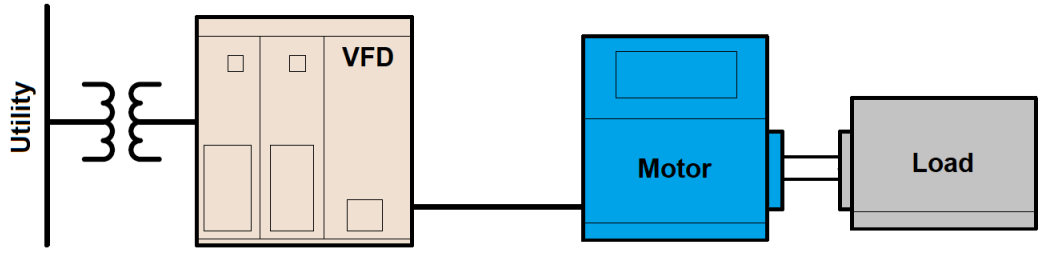



Fig. 2.1 Motor Drive in Industrial Process.

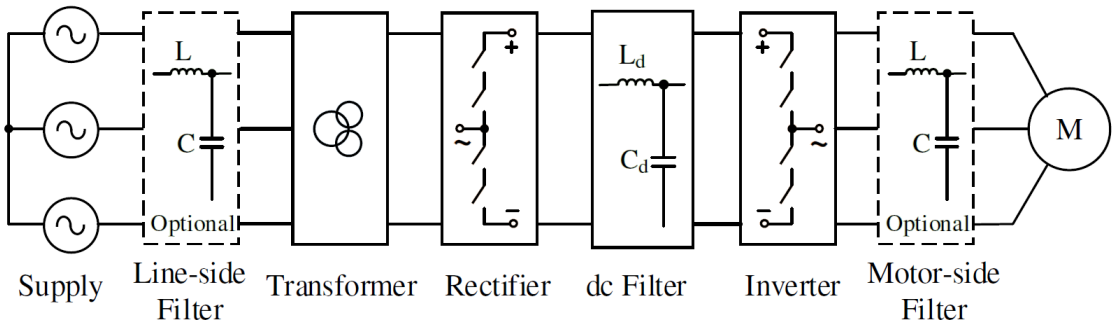



Fig. 2.2 Motor Drive Structure [2, 3].

Typically, motor drives' power converters consist of:

- A transformer, depending on the power converter topology, it can be two-winding mainly used for stepping up or down the voltage and preventing zero sequence currents; or phase shifted multi-winding used for reducing line currents distortion or other topology specific reasons. The transformer may be placed in the same enclosure with the converter or placed in a separate compartment.
- A converter, used for converting AC voltage to DC voltage. It can be either uncontrolled or controlled depending on the system requirements. In addition, it can allow bi-directional power flow if sending power back to the grid (regeneration) capability is required.
- A DC filter, used for de-coupling, smoothing, and energy storage. It can be either a capacitor to provide stiff DC voltage, or an inductor to provide stiff DC current depending on the topology. Converters relying mainly on DC

bus capacitors for bus storage are referred to as voltage sources converters (VSC), while converters relying mainly on DC bus inductors for bus storage are referred to as current sources converters (CSC).

- An inverter, a voltage source inverter (VSI) is used for synthesizing variable magnitude and frequency AC voltage from DC bus voltage, while a current source inverter (CSI) synthesizes variable magnitude and frequency AC current from DC bus current.
- An input line filter, used for reducing input line currents distortion in order to comply with the grid connection harmonic standards such as IEEE 519-2014 [3, 4], if this cannot be achieved through the converter structure itself.
- An output line filter, used for reducing output current harmonics or limiting $dv/dt$ on the motor terminals. This is required if the converter itself cannot achieve the motor voltage waveform requirements or if long cables are required to connect the converter to the machine.

In addition, optional input and output contactors, not shown in Fig. 2.2, may be added to some installations based on drive system requirements.

High power voltage sources motor drives can be categorized into two-level converters (2L-VSCs) and multilevel converters. High power 2L-VSCs as shown in Fig. 2.3 are connected to low voltage (LV) motors and grid in the range from 400

to 690 V. Their power ratings range from few hundred kW to around few MW. Beyond these power ratings, current ratings will reach uneconomical values, therefore; medium voltage (MV) motors and grid connection is the optimal choice.

There are several drawbacks when adopting 2L-VSCs for MV motors and grid. Fig. 2.4 shows MV 2L-VSC and its associated waveform. Motors will suffer from high voltage and current THD, high $dv/dt$, and high common mode voltage. These cause detrimental effects on the reliability of the motors, highly valuable asset, due to increased thermal and voltage stresses on motors windings and electrochemical stresses on motors' bearings. In addition, under medium voltage, 2L-VSCs should consider the tradeoff between using high voltage power switches or using series-connected lower voltage power switches, given the required switching frequency and the switching losses.

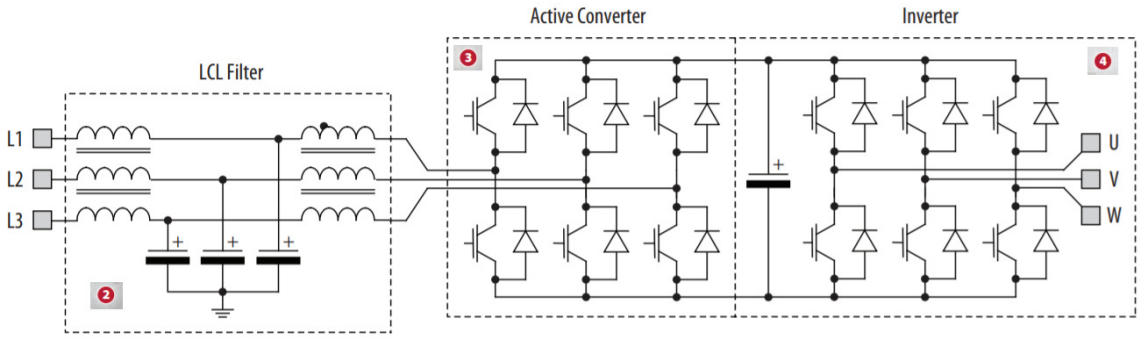
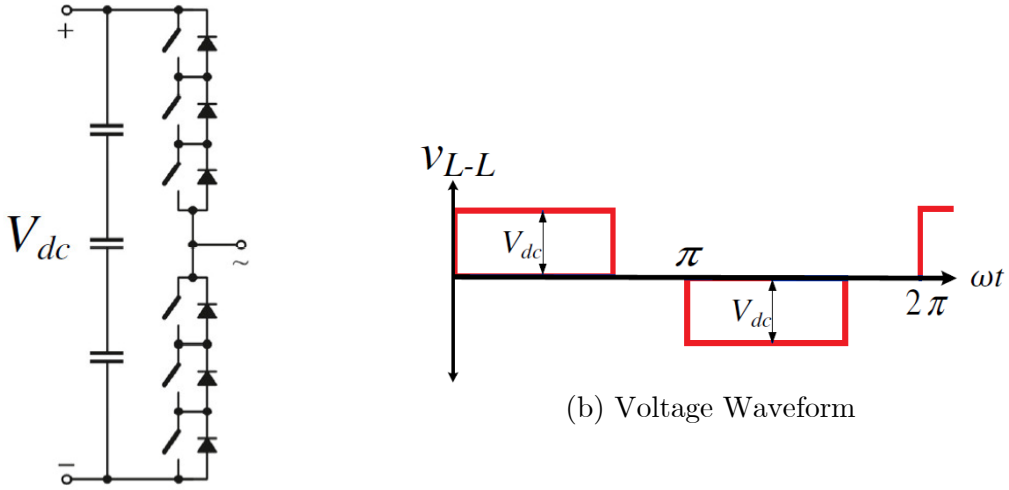



Fig. 2.3 Structure of a LV Converter in PowerFlex 750 Series [5]: 1) AC pre-charger, 2) LCL filter, 3) Two-level Grid Connection Converter, 4) Two-level Inverter, 5) Cooling, 6) Controller Processor.




(a) Topology

(b) Voltage Waveform

Fig. 2.4 Medium Voltage Two-level Converter [2].

All these factors in addition to the ability for retrofitting, advocate for the adoption of multilevel voltage source topologies. Compared to MV 2L-VSCs, MV multilevel topologies achieve lower motor side *dv/dt*, lower common mode voltage, lower harmonic distortion, lower devices' switching frequency, higher system efficiency, and almost no power switches series connection requirement. Fig. 2.5 shows voltage waveform associated with multilevel topologies.

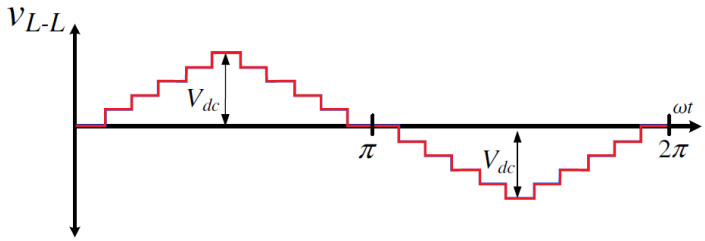
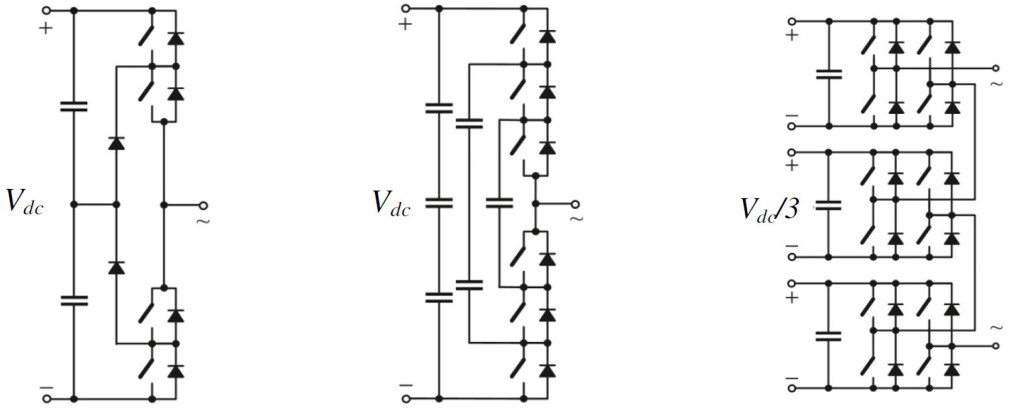



Fig. 2.5 Medium Voltage Multilevel Voltage Waveform [2].

Fig. 2.6 presents three topologies representing fundamental means for synthesizing multilevel voltage waveforms. These three topologies are neutral-point clamp (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) [2]. Building upon these fundamental means, several medium voltage multilevel topologies exist in literature and industry such as neutral point clamped (NPC), neutral point piloted (NPP) or (T type), nested neutral point piloted (NNPP) or (stacked multi-cell), flying capacitor (FC), five-level active NPC (5L ANPC), nested neutral point clamped (NNPC); cascaded H-bridge (CHB), five-level NPC/H-bridge, modular multilevel (MMC) [6, 7].




(a) NPC (b) FC (c) CHB

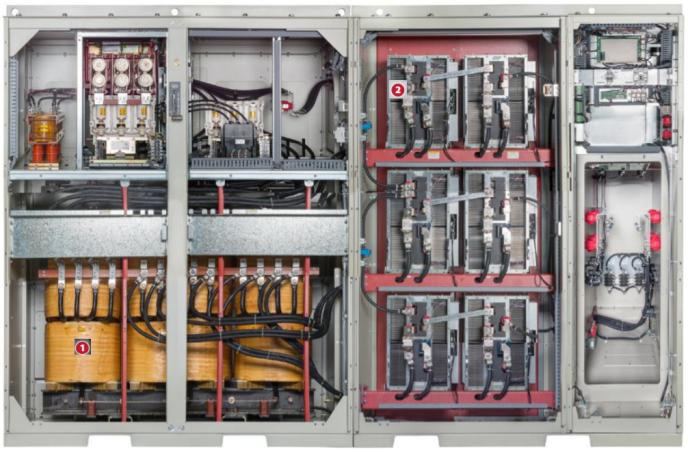
Fig. 2.6 Basic Multilevel Topologies [2, 6, 7].

Table 2.1 summarizes voltage source MV drive offerings and their topologies from leading motor drives manufactures. Fig. 2.7 provides the structure and topology for one offering.

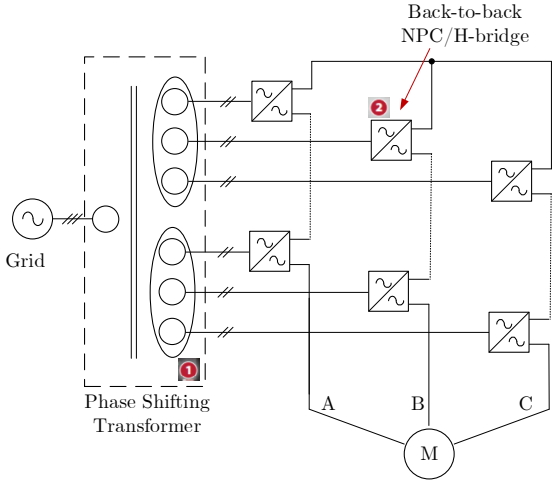
Table 2.1 Examples for Voltage Source MV Drives Offerings in the Market.

| Manufacturer | Product | Topology | Rating (Air - cooled) |
|---|---|---|---|
| **Siemens** [8] | GM 150 | NPC | 1 - 10 MW<br>2.3 - 4.16 kV |
| | SM 150 | Bi-directional NPC | 3.4 - 5.8 MW<br>3.3 - 4.16 kV |
| | GH180 | CHB,<br>Regenerative CHB | - 10 MW<br>2.3 - 11 kV |
| | GH150 | MMC | 4 - 35 MW<br>4.16 - 13.8 kV |
| | SH 150 | Bi-directional<br>MMC | 4 - 16 MW<br>3.3 - 7.2 kV |
| **ABB** [9] | ACS1000 | NPC | 325 kW- 5 MW<br>2.3 - 4.16 kV |
| | ACS2000 | ANPC<br>Bi-directional<br>ANPC | 250 kW- 3.68 MW<br>4 - 6.9 kV |
| | ACS5000 | 5L-NPC/H-bridge | 200 kW- 36 MW<br>6 - 13.8 kV |
| | ACS6000/6080 | NPC | 3 kW- 36 MW<br>- 3.3 kV |
| | ACS580MV | CHB | 200 kW- 6.8 MW<br>6 - 11 kV |
| **Rockwell Automation** [10] | PowerFlex 6000 | CHB | - 13 MW<br>2.3 - 11 kV |
| **GE** [11] | MV6 | NNPP<br>Bi-directional<br>NNPP | 200 kW - 6.6 MW<br>3.3 - 6.9 kV |
| | MV7000 | NPP,<br>Bi-directional NPP | 700 kW - 10 MW<br>3.3 - 6.6 kV |
| **Toshiba** [12] | T300MV2 | NPC | 220 kW - 2.2 MW<br>2.4 kV |
| | | NPC/H-bridge | 220 kW - 8.2 MW<br>- 4.16 kV |
| | | Hybrid CHB | 220 kW - 6.7 MW - 6.6 kV |
| | | 5L-NPC/H-bridge | 5.2 MW - 7.5 MW<br>- 6.9 kV |

| | | | |
|---|---|---|---|
| **TMEIC** [13] | TMdrive-MVE2 | Cascaded 5L-NPC/H-bridge, Bi-directional Cascaded 5L-NPC/H-bridge | - 6 MW<br>3 - 11 kV |
| | TMdrive-MVG2 | CHB | - 20 MW<br>3 - 11 kV |
| **Yaskawa** [14] | MV1000 | Cascaded 5L-NPC/H-bridge | 150 kW- 12 MW<br>2.3 - 11 kV |
| **Schneider** [15] | Altivar1200 | CHB | 315 kW- 16 MW<br>2.4 – 13.8 kV |
| **Danfoss** [16] | VACON3000 | NPC | 2.4 - 7 MW<br>3.3 – 4.16 kV |



(a) TMdrive-MVE2 Structure




(b) TMdrive-MVE2 Topology

Fig. 2.7 Example for Medium Voltage Drives Offerings [17].

## 2.2. Cascaded H-Bridge Drives

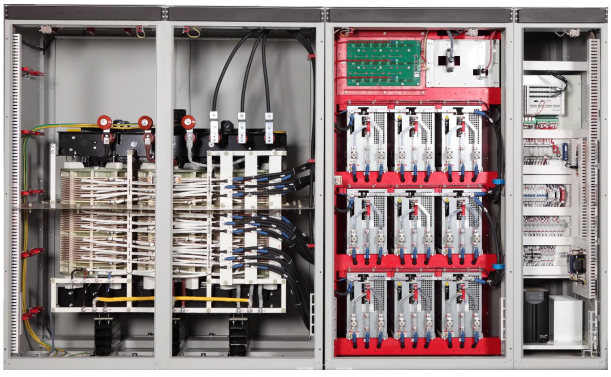
### 2.2.1. Introduction

As shown in Fig. 2.6, the CHB topology relies on series connected low voltage H-bridges that are supplied from isolated power supplies in order to synthesize multilevel voltage waveform. Typically, three branches of the cascaded H-bridges representing the phases are connected in Star connection to form the three-phase inverter structure. This structure gives CHB topology some advantages over other MV multilevel topologies. The CHB topology employs low voltage IGBTs and DC-bus capacitors compared to other topologies that employ medium voltage IGBTs, IGCTs, and DC-bus capacitors. In addition, the CHB topology does not have DC-bus capacitors voltages balancing issues associated with neutral point connections. Moreover, it is a scalable topology, where increasing the number of levels and the inverter output voltage is achieved through adding more H-bridges in series. Furthermore, CHB modular structure simplifies converter design, easies maintenance, reduces repair downtime, and provides fault tolerant capability. All these benefits have led to the wide adoption of CHB topology in the medium voltage drive arena. In the market, there are several CHB motor drives offerings such as GH180 from Siemens [18], ACS580MV from ABB [19], PowerFlex6000 from Rockwell Automation [20], TMdrive-MVG2 from TMEIC [21], Altivar1200 from

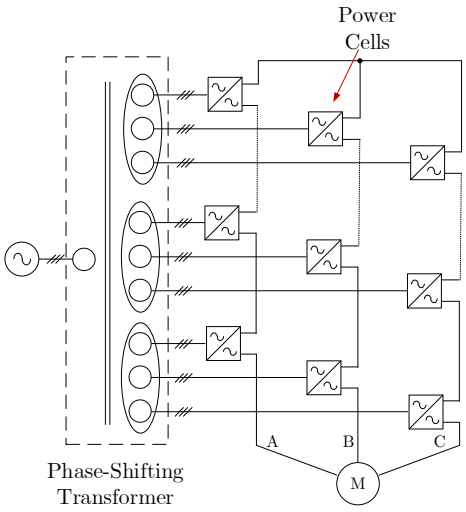
Schneider [22], MVW3000 from WEG [23], HIVECTOL-HVI from Hitachi [24], VersaBridge from TECO-Westinghouse [25], N5000 from Hyundai [26], SILCOVERT TH from Nidec [27], etc.

**a) Structure**

Practically, the CHB topology combines a phase-shifting isolation transformer and cascaded power cells. Fig. 2.8 shows a commercial CHB converter enclosure including a transformer section, power cells section, and control section. At the input side of the converter, the integration of isolation transformer serves three goals. First, it steps down the input voltage. Second, it provides multiple isolated secondaries. Third, it cuts down the input current total harmonic distortion (THD), due to the effect of phase shifting between secondary windings.



(a) Enclosure Structure from left to right: Transformer section, Power Cells Section, and Control Section.

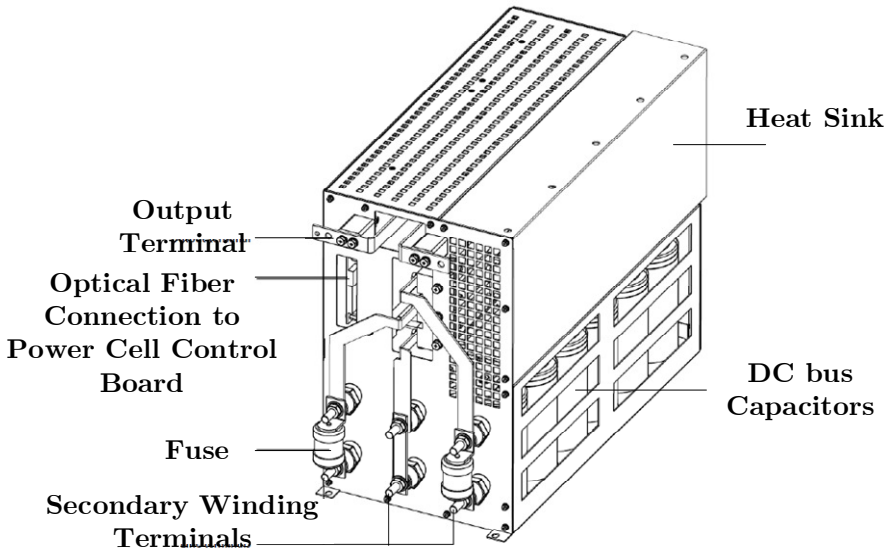



(b) Topology

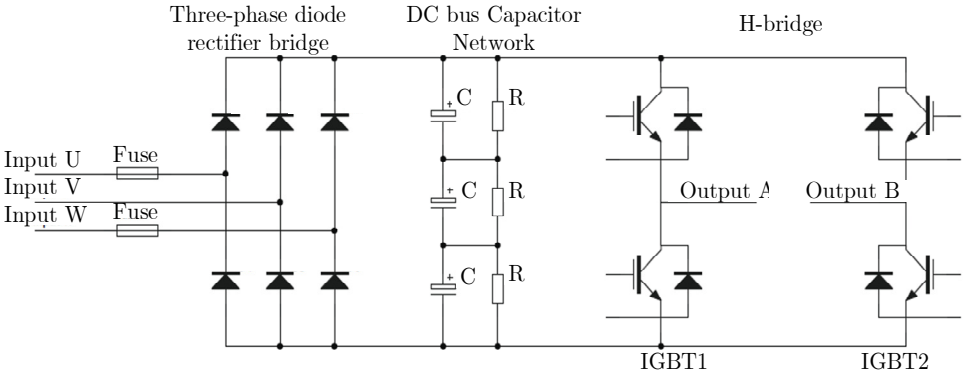
Fig. 2.8 PowerFlex6000 CHB [28].

Therefore, the input side complies with IEEE 519 grid connection harmonic current standards with reduced sized or even without input side filter.

The common CHB drives in the market are capable of two-quadrant operation or non-regenerative. Accordingly, the power cells are composed of diode front-end (DFE), DC-bus capacitors, and H-bridge as shown in Fig 2.9.




(a) Power Cell Enclosure Structure.




(b) Basic DEF Power Cell Topology.

Fig. 2.9 PowerFlex6000 CHB Power Cell [28].

The rectifier is responsible for sustaining the DC voltage on the DC-bus capacitors, while the H-bridge inverter synthesizes the DC voltage to produce AC voltage with variable frequency and magnitude.

The output terminals of the power cells are series-connected in order to produce the voltage at motor terminal. Each power cell produces a low voltage step, which can be pulse width modulated to further reduce motor side THD. As a result, near sinusoidal motor voltage can be achieved, reducing *dv/dt*, harmonic currents, and torque pulsations at the motor, even at lower speed operation. The typical power cells ratings are presented in Table 2.2.

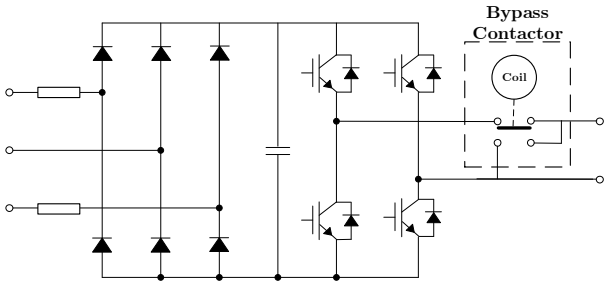
Table 2.2 Typical Air Cooled Power Cell Ratings Ranges [28, 29].

| Input Voltage | DC-bus Voltage | Switch Frequency | Output Current |
|---|---|---|---|
| 600 - 750 Vac | 848 - 1060 Vdc | 600 - 1200 Hz | 40 - 680 A |

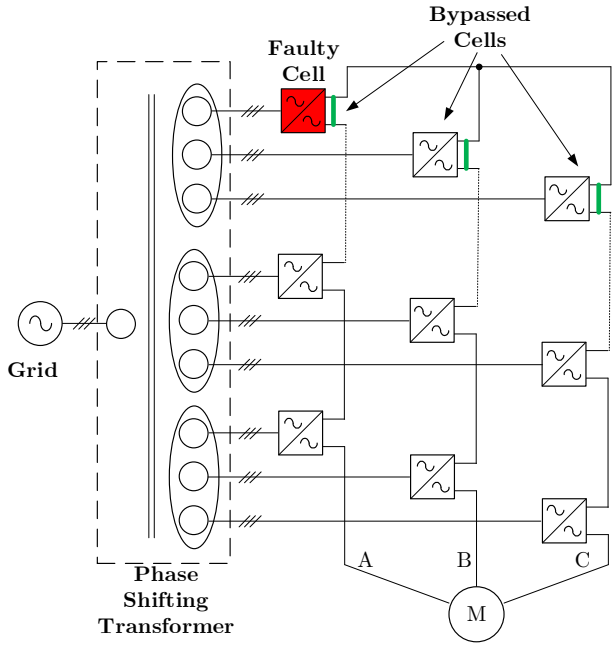
**b) Fault Tolerant Capability**

Each power cell has built-in diagnostic features. In case of power cell fault, the fault is detected and the faulty cell is identified and isolated from the rest of the converter by the means of the bypass contactor. If the converter is not equipped with redundant power cells, still it can operate at reduced output voltage. Fig. 2.10 illustrates fault tolerant capability of CHB topology. This feature maximize drive availability significantly and is considered an important merit of CHB topology

compared to other topologies such NPC or NPC/H-bridge which require the whole converter shutdown for all converter faults.




(a) Cell Bypass Contactor




(b) Basic Bypass Capability

Fig. 2.10 CHB Fault Tolerant Capability [30].

### c) Cell Control

Fig. 2.11 illustrates the basic control structure of the DFE-based power cells [31-33]. Typically, the cell controller board and gate drivers receive their power supply from power cell's DC-bus through an isolated switch-mode power supply. The cell

controller relays H-bridge PWM signals coming from the motor controller in the centralized controller to the gate drivers. In addition, the controller monitors DC-bus voltage, gate drivers' status, IGBT modules case temperature, heat sink temperature, etc. In case of abnormal condition, the controller identifies the cell fault and acknowledge the centralized controller through the communication link. Based on the bypass order from the centralized controller, the cell controller activates the bypass contactor and monitors the success of cell bypass process.

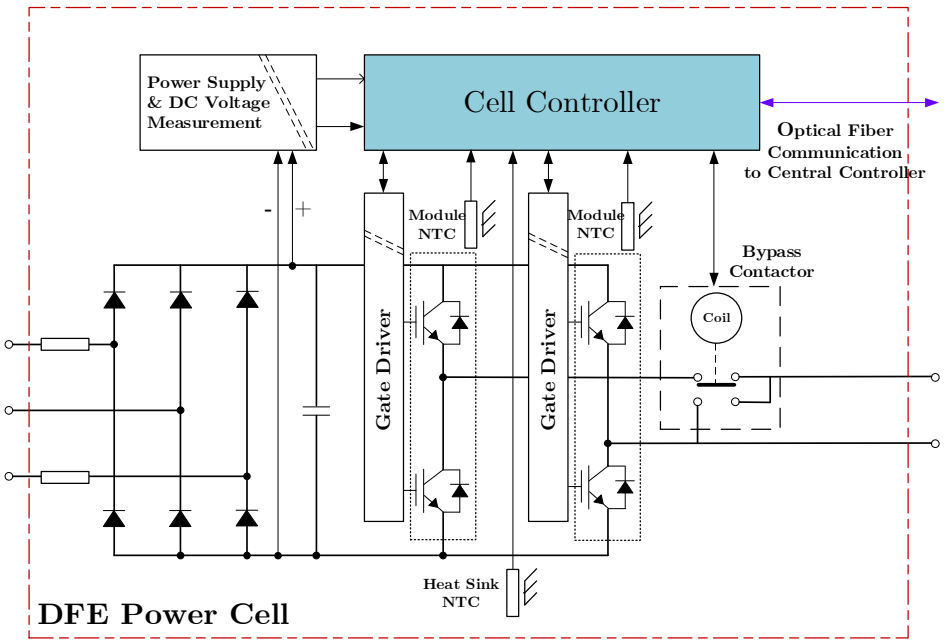



Fig. 2.11 Basic Diagram of the Control Structure of Typical DFE-based Power Cell.

### d) Drive Control

The central control unit, shown in Fig. 2.12, is responsible for the core functionality of the variable frequency drive [31-33]. It runs motor control algorithms such as

$V/f$ control, field-oriented control (FOC) based on speed encoder and motor current, or sensor-less FOC based on the motor currents and voltages. It generates synchronized PWM signals to reduce motor current harmonics. The PWM signals are sent through the communication links to the power cells to produce the required output voltage and frequency. The central controller monitors the power cells, motor voltage and current, and grid voltage and current to generate operational data beneficial for process optimization, or to generate alarms, protection trip signals, and cell bypass in case of abnormal and faulty conditions.

### 2.2.2. Regenerative CHB Drives

DFE-based power cells allow the CHB drives to operate in two quadrants. This covers the majority of medium voltage motor drive market. Yet, an important portion requires braking capability such as fast braking of high inertia fans, or negative torque capability such as downhill conveyors [1]. For motor braking, one method is to allow the dissipation of motor inertia power inside the motor windings. However, temperature rise during this process may cause reliability issues to the motor especially if the braking process is frequent. Another method is to damp the inertia power into external resistor banks. Although this method prevents previous method's reliability issues, resistor banks require extra space and cost for placing and cooling.

For applications where regeneration is possible, regenerative braking is a more efficient and cost effective method. In this method, inertia power is sent back. This results in significant efficiency increase and cost reduction especially for applications that require negative torque for a considerable portion of their load cycle.

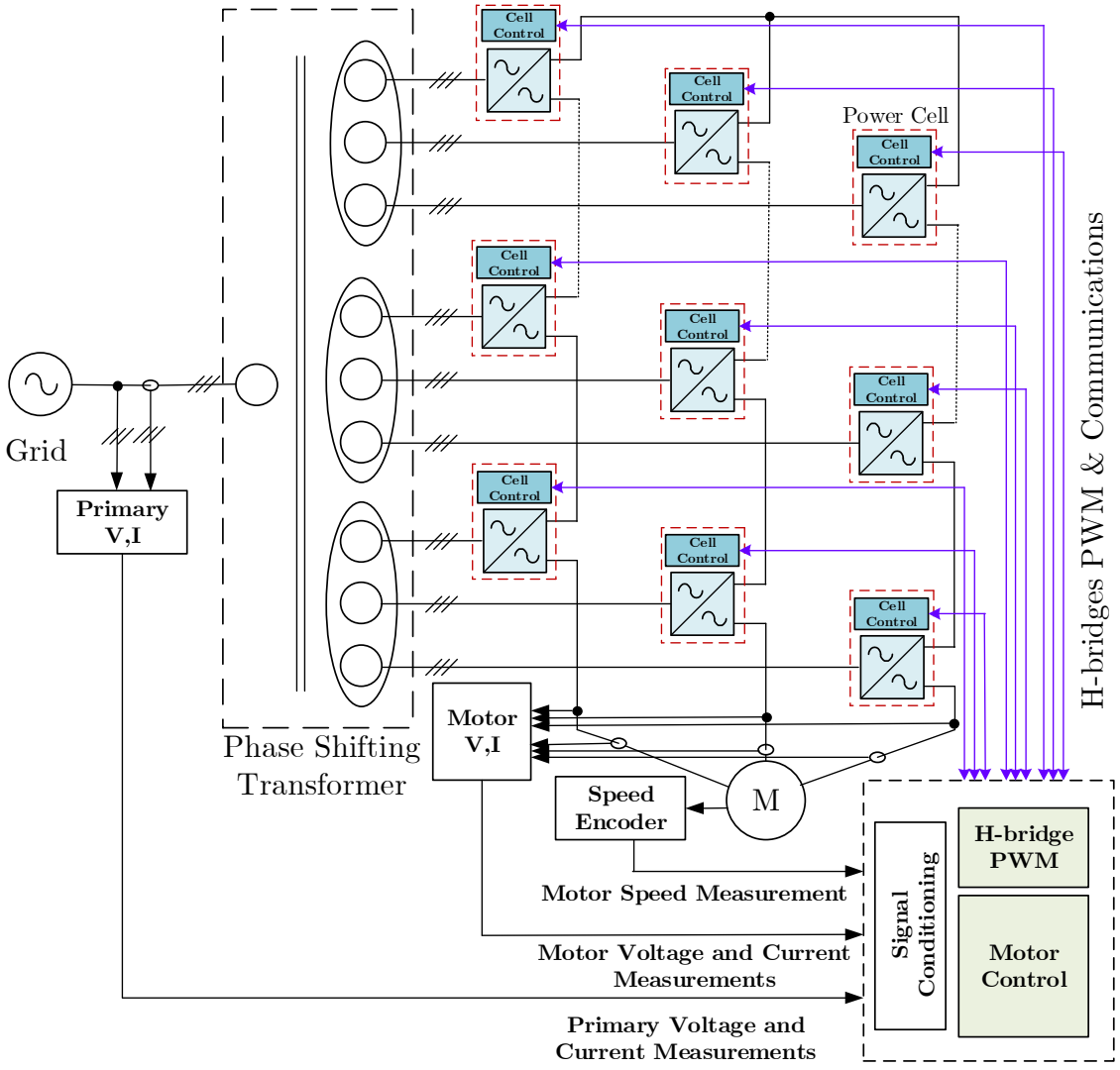



Fig. 2.12 Basic Diagram of the Control Structure of Typical DFE-based CHB Drive.

### a) Cell Structure

In order to allow regeneration capability in CHB topology, the straightforward way is to replace diode front-end (DFE) with active front-end (AFE) in power cells as shown in Fig. 2.13. In addition, cell inductors may be required for filtering and control purposes. Regenerative CHB drives with this cell topology or even newly proposed ones have been addressed in several publications and patents [34-38]. Nonetheless, it was not until the last quarter of 2020 when Siemens announced the first regenerative CHB drive in the market [39]. Accordingly, this next generation CHB drives are able to compete in regenerative market segment that was dominated by the whole DC-bus drives such as NPC and its variants.

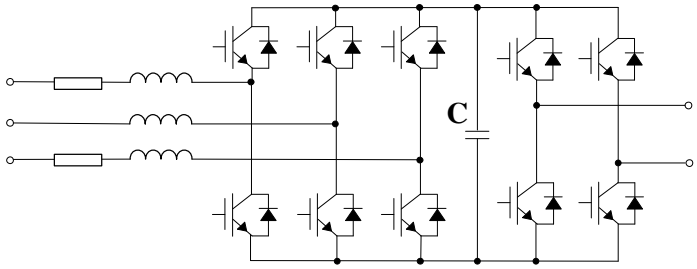



Fig. 2.13 Common AFE-based Power Cell.

### b) Cell Control

Regenerative CHB does not only require the modification of the power cell topology, but also the modification of the power cell controller. Fig. 2.14 shows basic block diagram of a common AFE-based power cell controller proposed in literature [32, 34-38]. An AFE controller is added to the power cell, its main task is to regulate

DC-bus voltage during regeneration preventing DC-bus overvoltage. Other tasks may include front-end input current control and reactive power compensation.

The controller responses by synthesizing sinusoidal PWM three-phase voltage waveform at the input of the AFE. The generated SPWM signals are then transmitted to cell controller to be relayed to the AFE gate drivers. Typically, the switching frequency of the AFE is set up to 2 kHz to 4 kHz [32, 34-38].

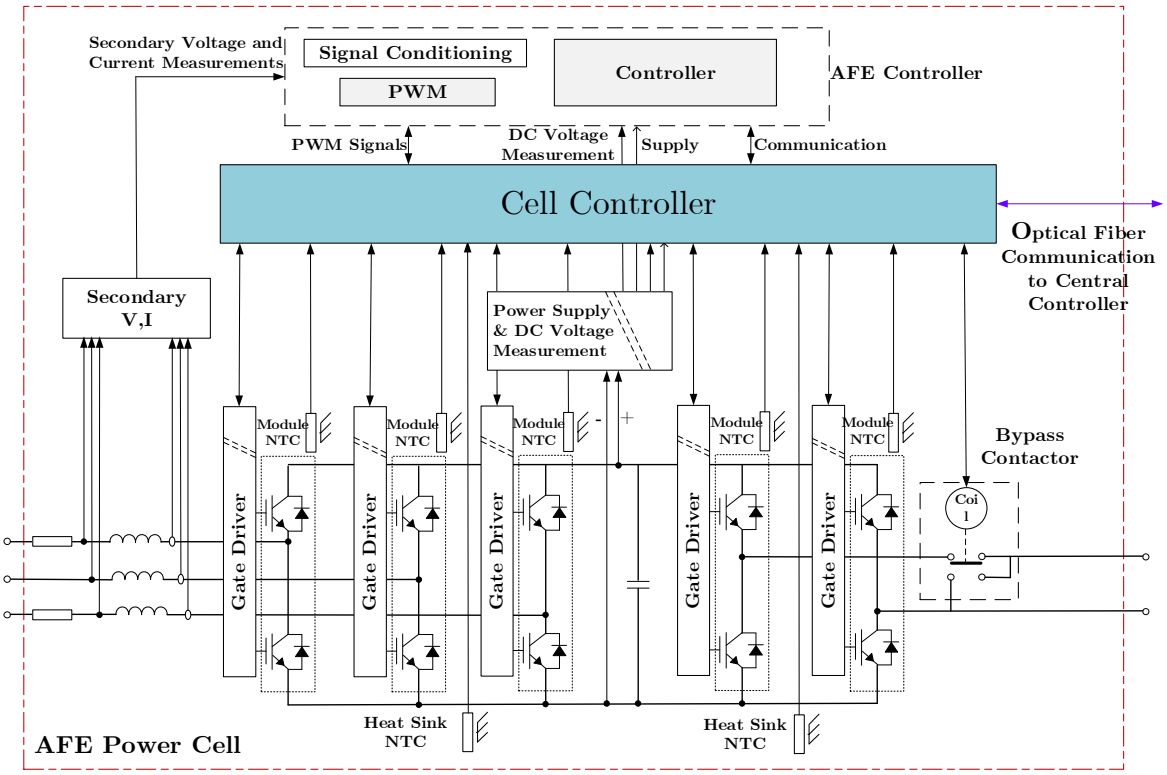



Fig. 2.14 Basic Diagram of a Common Control Structure of AFE-based Power Cell.

To perform its control tasks, the AFE controller requires secondary winding voltage measurements for grid synchronization and reactive power compensation,

input current measurements for input current control, and DC-bus voltage measurement for DC bus regulation.

For the purpose of diagnosis, protection, and taking corrective actions, the AFE controller is required to communicate with the cell controller in case of abnormal AFE power cell conditions.

**c) Drive Control**

Drive system control and performance optimization may require establishing communication link between the central controller and the AFE controllers. For example, AFE controllers may utilize information about motor frequency and power to improve AFE dynamic performance, and so the whole motor drive performance. Fig. 2.15 presents a common control structure of AFE-based CHB drive illustrating modifications in the power cell structure and communication links [38, 40-42].

Beside the additional tasks and communication requirements imposed by the AFE functionality, the central control unit is responsible for the core functionality of the variable frequency drive as in the DFE-based CHB. It runs motor control algorithms such as $V/f$ and FOC based on speed encoder and motor current, or sensor-less FOC based on the motor currents and voltages. It generates

synchronized PWM signals and transmit them through communication links to power cells to produce the required output voltage and frequency. In addition, it monitors power cells, motor voltage and current, and grid voltage and current for drive system diagnosis, protection, and operation monitoring.

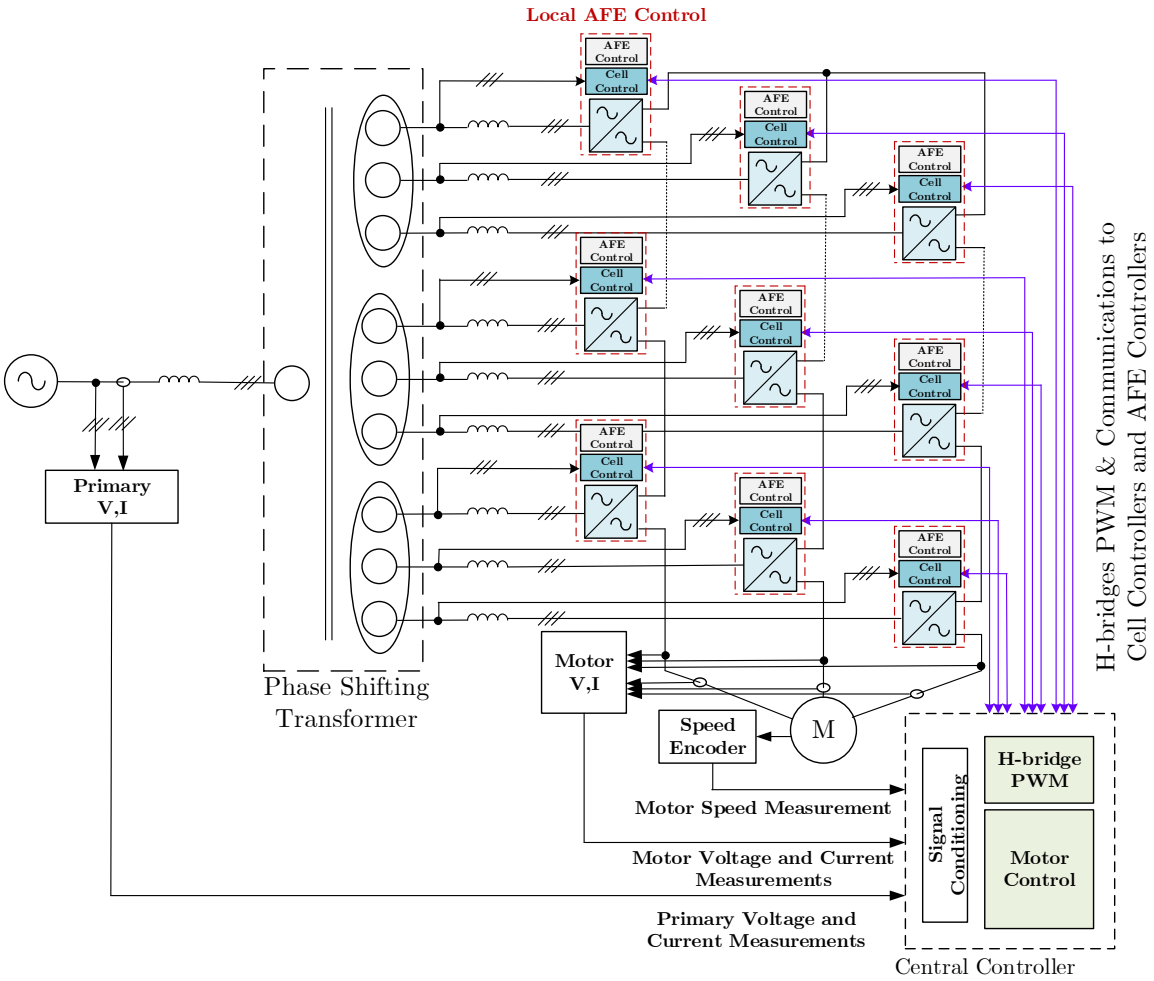



Fig. 2.15 Basic Diagram of a Common Control Structure of AFE-based CHB drive.

## 2.3. Summary

This chapter provided necessary high power converters background and basis upon which thesis work has been developed. A review on high power voltage source converter topologies was introduced. The position of the CHB drives among other high power voltage source converter topologies was highlighted considering various perspectives such as applications, features, and structures. Then, a detailed discussion about non-regenerative CHB drives, widely used drive topology in industry, including topology, structure, and control was presented.

The limitations of non-regenerative CHB drives, the importance of next generation CHB drives with regeneration capability, and the industry status was reviewed. Finally, a detailed discussion about the topology, the structure, and the control of common regenerative CHB drives in literature is presented.

# Chapter 3

# Field Failures and Reliability of Medium-Voltage Power Converters and Motor Drives

This chapter provides a detailed discussion on industrial high power converters field failures. In addition, long-term reliability of semiconductors, electrolytic capacitors, and PCBs under power cell's thermal stresses is presented. Furthermore, the approaches to tackle these reliability issues during converter design stage and during field operation are discussed.

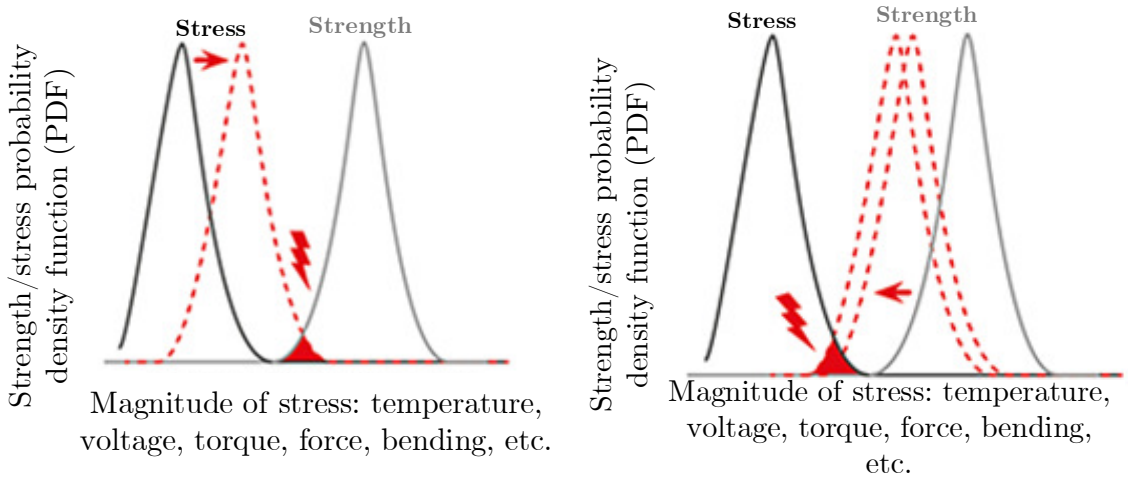
## 3.1. Field Failures of Power Converters

Typically, medium voltage motor drives or high power converters operate under harsh loading and environmental conditions. According to [43], drives may operate in extreme temperatures, intense vibrations, corrosive environment, etc. In addition, they may be subjected to intense or even unexpected loading conditions. Accordingly, faults (degradation or partial loss of function), and failures (loss of function) take place in the field [44]. If the failure is associated with extended down times and production loss, property loss, or safety hazard situation; it is considered a catastrophic failure.

### 3.1.1. Causes of Failures and Faults

Converters are systems of integrated assemblies, and components. A converter system fault or failure may result from a component failure, an assembly failure, or a faulty interaction between different components of the converter. According to [43], there are two reasons for field faults and failure: overstress and wear-out. They are related to the power converter's strength as shown in Fig. 3.1. Components overstress fault or failure may happen if they are subjected to stress that exceeds their strength. On the other hand, wear-out is a long-term progressing fault that eventually turns into failure. Each time a component or an assembly is subjected to stress, this causes a gradual damage. Under continuous exposure to stress, a

build up of damage takes place through time. This causes a continuous degradation of strength and as a result, failure happens at the end.




(a) Overstresses

(b) Wear-out

Fig. 3.1 Causes of Faults and Failures [43].

The important lesson taught by field forensic analysis is that there is no one specific failure mode (how a fault or a failure takes place) to blame for the converter systems faults [43- 47]. Various factors such as converter topology, application, and field conditions play an important role in accelerating some of failure mechanisms (the underlying causes), which determine the dominant failure modes on case-by-case basis. The following subsection provides an extensive discussion on reported failure studies from the field for medium voltage motor drives or high power converters in general.

### 3.1.2. Converters Field Failure Studies

In [47], a survey involving a number of respondents from several industries such as components manufacturers, aerospace, automotive, motor drives, utility, and others was provided. According to the survey, power electronics components are the first when it comes to fragility, succeeded by capacitors, gate drivers, and connectors. In addition, system transients, overloading, and environmental conditions are the main causes to component failures and converters faults and failures. In another study [45], thermal issues are the main cause for components and assemblies failures, followed by mechanical vibration, moisture and humidity, then dust and contamination.

In [48], a detailed field failure analysis considering IGBT modules failures in an offshore MW application was performed. The converter topology was 2L-VSI. It was shown that more IGBT module failures due to overstress have been reported in sites, which are characterized by a higher frequency of unexpected loading events. Fig. 3.2 shows a sample of IGBT modules failures caused by overstresses due to grid faults, machine faults or control system faults [48-50]. In addition, the study found that protection of the converter hardware against the environment is insufficient.

Conductive paths can be formed by traces of salt and corrosion products on a driver board and power supplies circuitry as shown in Fig. 3.3. Furthermore, the study reported that deteriorated thermal paste was found in several IGBT modules. This is in addition to the presence of fretting corrosion in the IGBT modules' baseplate and heat sink caused by mechanical pressure and thermal cycling as shown in Fig. 3.4.

Fig. 3.2 Failures of IGBT Modules due to Overstresses due to Grid Faults, Machine Faults or Control System Faults [49, 50].

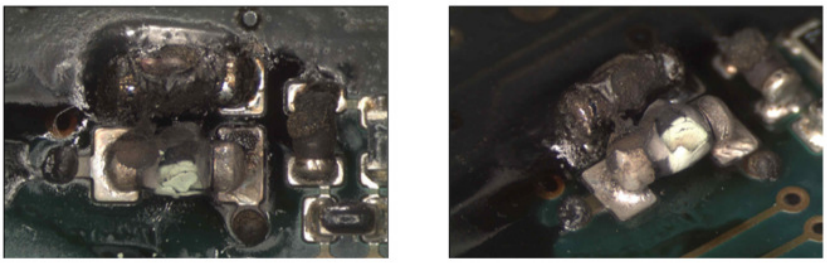


Fig. 3.3 Gate Driver PCB Faults.

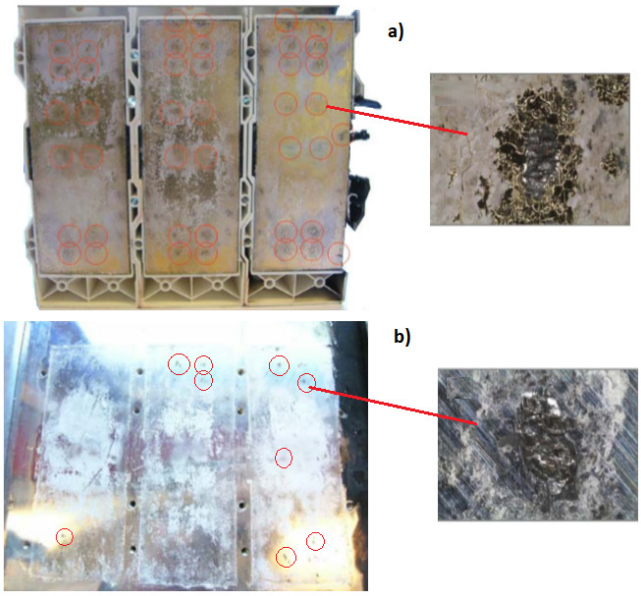



Fig. 3.4 IGBT Package-Related Degradation Issues [50]: a) Fretting Corrosion of DBC Bottom Layer, b) Degradation of Thermal Paste and DBC Bottom Layer.

In [51, 52], field failures for a bi-directional medium voltage IGCT-based 3-level NPC converter have been investigated. Fig. 3.5 shows the converter system under study. IGCTs are more rugged than IGBT. In addition, IGCTs have better power cycling capability than LV IGBT modules, as IGCTs use press-pack packages that are bond wire free. According to the study, control system failures are dominant with 35% of converter faults and failures related to control systems and sensors. Semiconductor failures result in 25% of converter's faults and failures. Cooling system failures cause 18% of converter's faults and failures. RLC filter issues, auxiliary supply failures, and relays and breakers failures lead to 11%, 10%, and 1% of converter failures, respectively.

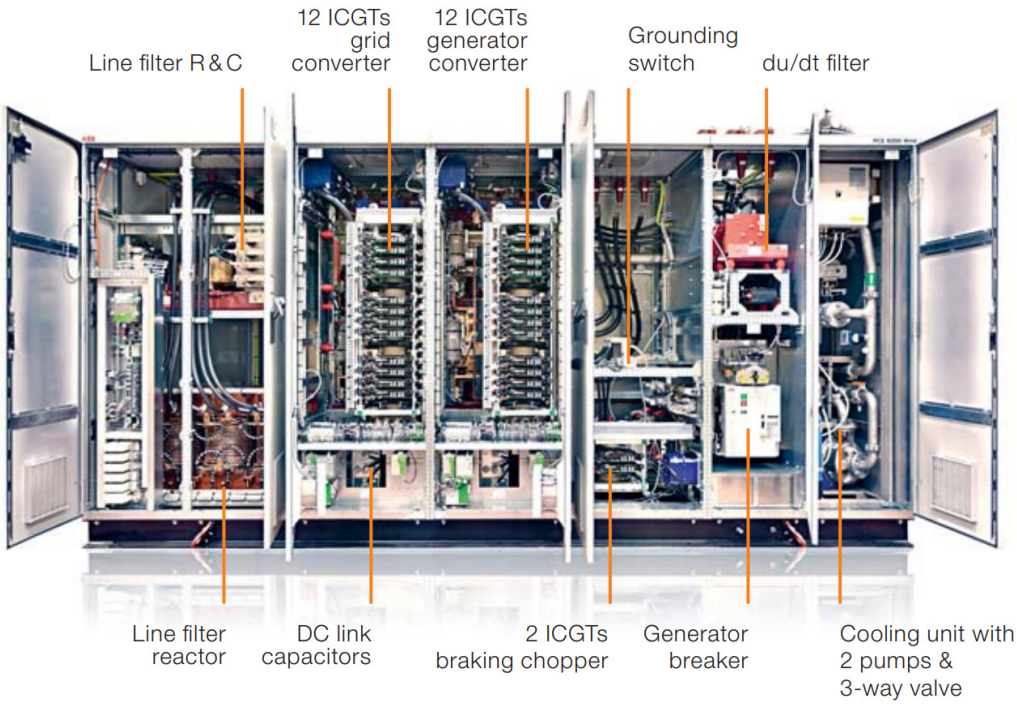



Fig. 3.5 Bi-directional Medium Voltage NPC Power Converter [51].

In another study [53, 54], a unidirectional medium voltage IGCT-based 3-level NPC converter is considered as shown in Fig. 3.6. Given the specific application, 65% of converter system faults and failures are attributed to failures in inverter unit (INU). This is the highest contributor to the overall system failures, followed by 9% in control and sensors unit (COU), 7% in line supply unit (LSU), 7 % in water-cooling unit (WCU), 6% in capacitor bank unit (CBU), and 6% in terminal unit (TEU), respectively. According to the study, there are 203 identified failure modes: 95 are of low likelihood, 59 are of medium likelihood, and 49 are of high likelihood. For INU, there are 15 identified possible components failures. Examples for these failures are gate driver unit failure, clamp capacitor failure,

clamp resistor failure, loss of auxiliary voltage, gate driver unit supply failure, loss of optical fiber control signal, and loose connections.

It is important to note the low percentage of DC-bus capacitors failures in NPC topology. The reason for that is the usage of high voltage dry film capacitor banks that are characterized by self-healing capability and high reliability in comparison to other capacitor technologies such as the Aluminum electrolytic capacitors.

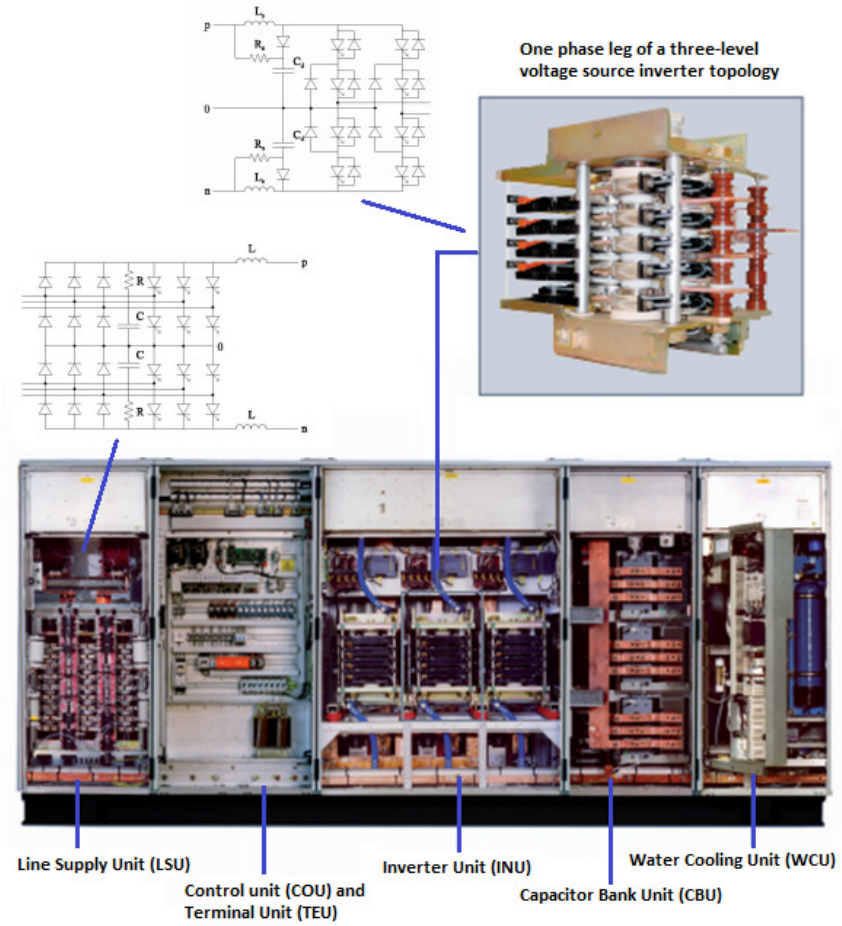



Fig. 3.6 Unidirectional Medium Voltage NPC Power Converter [53].

### 3.1.3. Drive Faults and Failures Classification

A modular drive system with three shunt-interleaved bi-directional NPC converters has been analyzed in [55]. Fig. 3.7 presents converter system layout.

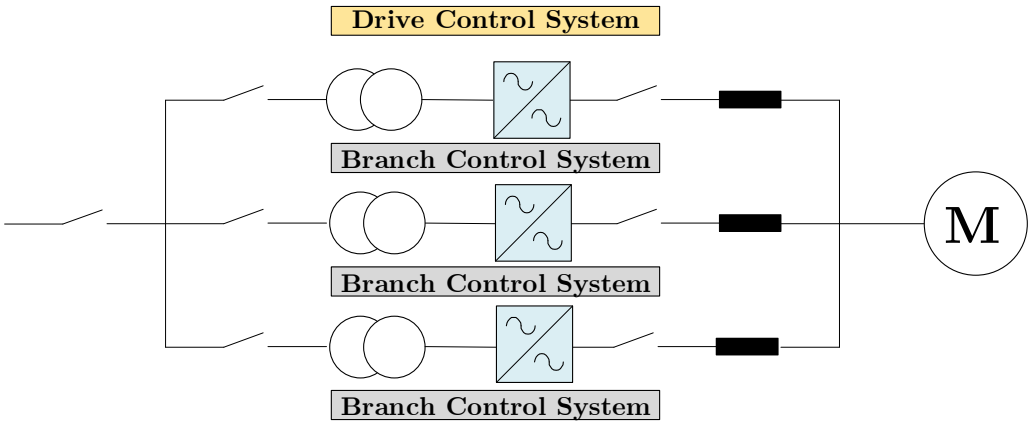



Fig. 3.7 Modular Drive System Under Study in [55].

Drive faults and failures are classified into two categories: "common" subsystem and "branch" subsystem faults and failures. Failures in machine, drive control system, and main breaker are examples of "common" subsystem failures, which represent 20% of drive system faults. The motor failures represent about 64% of the subsystem faults and failures, followed by about 23% attributed to drive control system failures. On the other hand, examples for severe "branch" subsystem faults and failures are IGCTs, diodes, snubbers, DC-bus capacitor failures. This category represents 10% of drive system faults and failures. Typically, these failures require fast protective actions to limit consequences and prevent safety issues. Cooling system failure, gate drivers failures, "branch" subsystem control and sensors

failures, and protection trips due to thermal overload, over-current, over-voltage, etc. are examples for less-severe "branch" subsystem faults and failures. These failures represent about 70% of converter system faults and failures, 50% of these failures are attributed to protection trips due to unallowed operation conditions. Protection trip failures do not require maintenance unlike hardware-related failures.

### 3.1.4. Fault/Failure Handling

A Fault/Failure-handling strategy for modular power converter has been discussed in [55]. Fig. 3.8 illustrates this strategy under three scenarios: "No Redundancy", "Fault Tolerance", and "Redundancy".

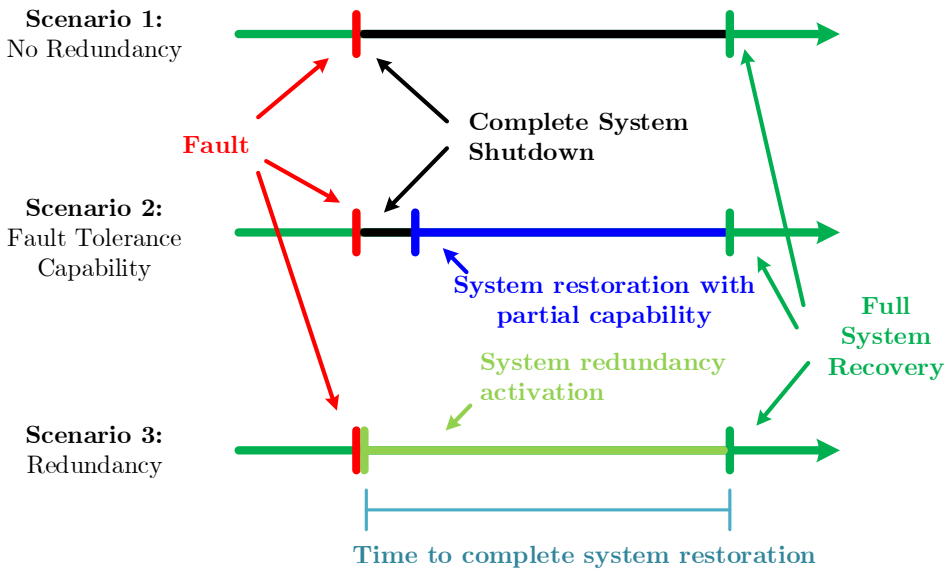


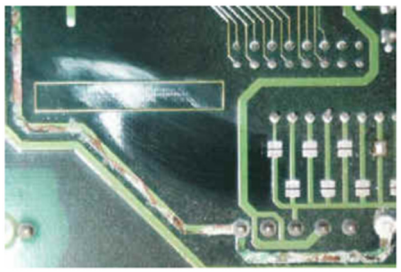

Fig. 3.8 Different Fault/Failure Handling Scenarios in Power Converters [55].

"No Redundancy" scenario represents the case when the fault or the failure occurs in the "common" subsystem. In this case, the system is not enable to continue

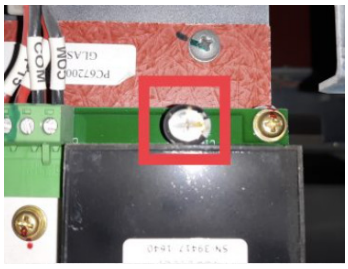
operation. Therefore, complete converter system shutdown is required. In case of "branch" subsystem failures, a partial or complete system shutdown takes place until failure diagnosis routines are executed and the "branch" subsystem with the determined failure is isolated. On completing the isolation, system restoration with partial capability can take place. This represents the fault tolerant scenario. In case of redundant hardware availability, on detecting failure in a "branch" subsystem, the faulty branch is isolated and a redundant branch is then connected to the system. This allows momentary complete system restoration.

### 3.1.5. Additional Fault/Failure Reasons

According to [56], regarding low and medium voltage power converters in general, failures may occur due several reasons other than issues related to overloading or system transients. Fig. 3.9 shows some of these reasons: loose connections, moisture, line disturbance, defective insulation, foreign objects and materials, and collision.



(a) Corrosion on PCB Caused by Moisture



(b) An Exploded Capacitor on a PCB

(c) Arcing Caused by Loose Contacts

(d) Burns on Heat Sink due to Flashovers

(e) Cooling Fan Clogging

(f) Dust Accumulation into Drive Enclosure

Fig. 3.9 Samples of Converter's Faults and Failures [56].

## 3.2. Field Failures and Reliability of CHB

In CHB drives as shown in Fig 3.10, high portion of drive system faults are attributed to power cell failures [28-30, 57]. Due to the modularity of the CHB topology, in case of power cell failure, the failed cell can be bypassed and partial

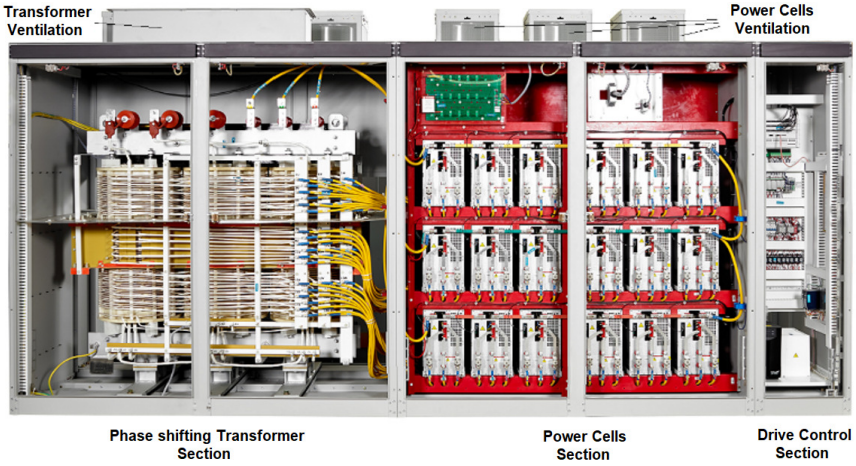



Fig. 3.10 DFE CHB Medium Voltage Drive, Courtesy of Rockwell Automation [2].

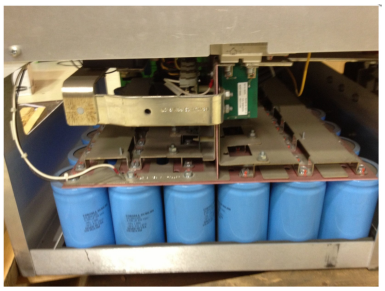
system restoration is achieved after a short interruption. In addition, if N+1 cell redundancy is employed, full restoration is achieved almost no interruption.

IGBT modules, power diodes modules, and fuses failures are the main contributors to severe power cell failures. The main causes of these failures are over-voltage, overcurrent, and flashovers due to formation of conductive paths because of corrosion and environmental conditions.

DC-bus capacitors are critical as well, they may fail due to over-voltages and flashovers. Moreover, they require strict preventive maintenance routines. Some CHB drives manufacturers require replacing the whole DC-bus capacitors every 7 years based on operation conditions [28, 58, 59]. The reason is that the CHB power cells are low voltage DC-Buses, which requires cost-effective high-capacitance technologies to achieve the required total energy storage. Typically, Aluminum electrolytic capacitor technology is widely used for commercially available CHB drives. However, the current and thermal stresses specific to the CHB power cells topologies result in accelerating their degradation.

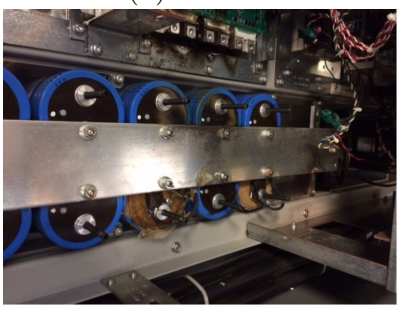
In [59], a study was performed by a medium voltage drives maintenance company on CHB DC-bus capacitor failures. Fig. 3.11 shows samples of DC-bus capacitor failures for Siemens/Robicon power cells.

(a) Power Cell



(b) DC-bus

(c) Capacitor explosion caused by electrolyte evaporation



(d) Burning signs on capacitors and the bus bar due to overheating

Fig. 3.11 Samples of Failed DC-bus Capacitors [59].

According to the study, the actual lifespan of DC-bus capacitors depends on several aspects. Temperature and ripple current cause an increase in electrolyte loss through evaporation. This loss results in overheating which in turn causes more electrolyte losses. Overvoltage degrades the Aluminum oxide causing internal short circuits coupled with severe overheating which may result in violent explosions. Improper mounting and clamping may lead to mechanical degradation to the capacitor packaging. Loose contacts or short screws can cause arcing effects while long screws may penetrate capacitor active materials leading to short circuits. This could lead to severe overheating coupled with explosion. Another important aspect

is the electrolytic capacitors shelf life. Storage conditions has a strong effect on capacitor lifetime. Lifetime issues of electrolytic capacitors in CHB lead some manufactures to offer higher power cells models with longer lifetime using film capacitors such as Siemens GH180, WEG MVW300, and TECO Westinghouse VersaBridge.

Aside from semiconductor and capacitor failures, the largest percentage of power cell failures are due to failures in gate drivers, power supplies, power cell controllers, and communications. The reason is there are numerous possible failure modes. Although these failures are less severe, they result in a complete loss of power cells' functionality [57, 59, 60].

The following discussion illustrates few examples of these failures applied to ABB ACS580 MV power cell shown in Fig. 3.12. The power circuit is composed of input fuses, a diode rectifier, a pre-charging circuit, electrolytic DC-bus capacitance, and H-bridge as illustrated in Fig. 3.13. The part of the power circuit after the fuses until the IGBTs is implemented on a power PCB as shown in Fig. 3.14, while the connection of the IGBTs to the output is implement using cables as shown in Fig. 3.12.

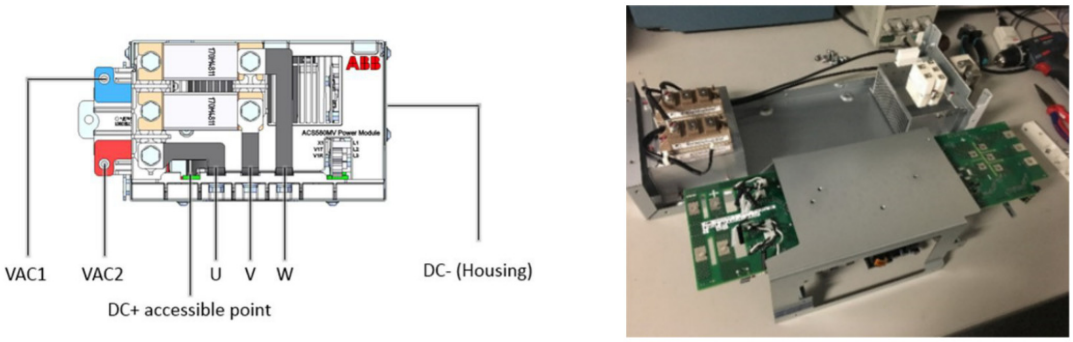



Fig. 3.12 Frame R1-R3 ABB ACS580 MV Power Cell [58, 60].

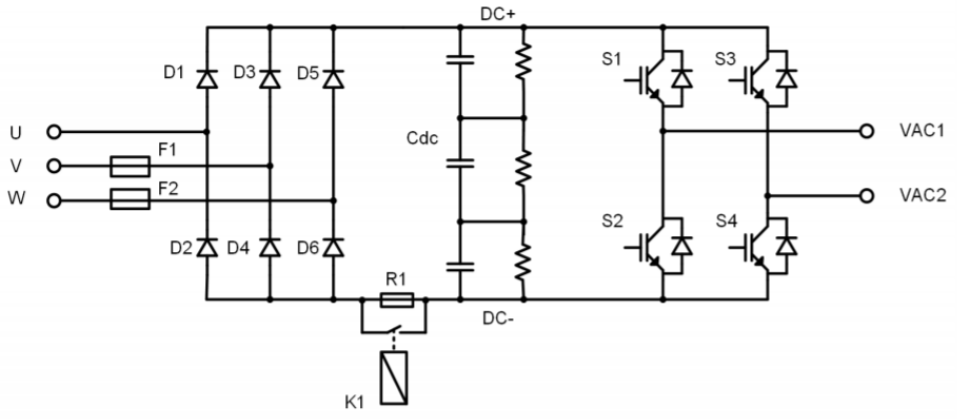



Fig. 3.13 Frame R1-R3 ABB ACS580 MV Power Cell Circuit [58, 60]

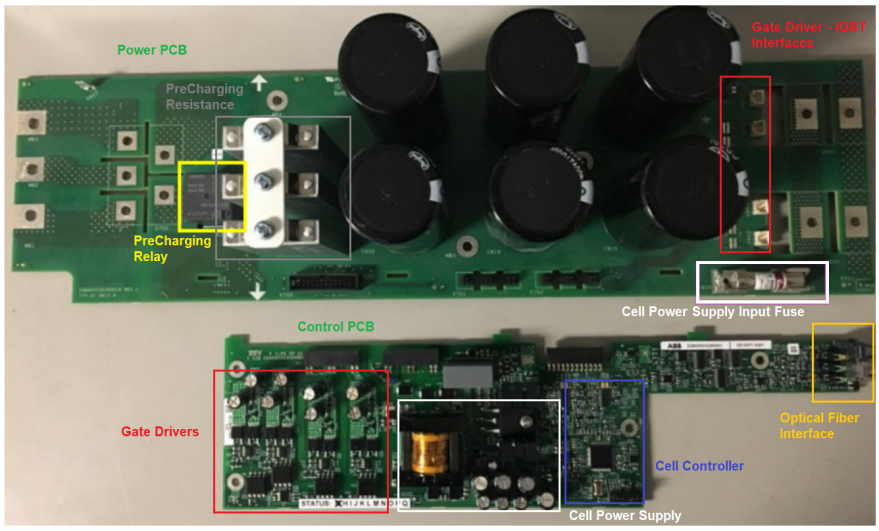
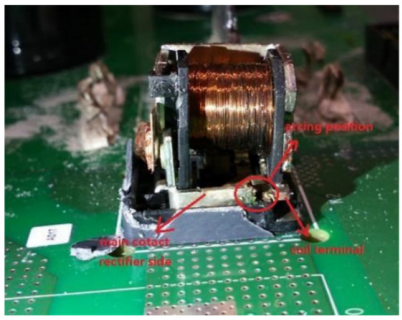
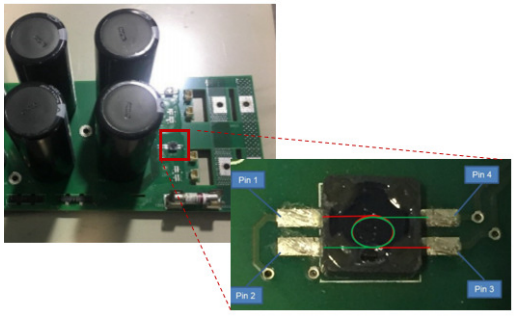



Fig. 3.14 Frame R1-R3 ABB ACS580 MV Power Cell PCB and Control PCB [58, 60].

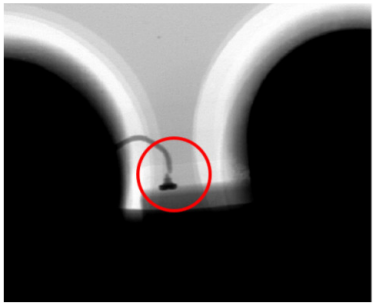
Given the shown complexity of the power cell, various faults and failures may take place. Fig. 3.15 presents some of the important component failures that may happen in either the power or the control PCB due to unexpected loading, or wearing under harsh conditions.



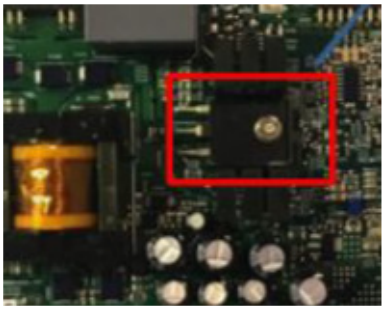

(a) Failure of the Pre-Charging Relay due to Internal Arcing



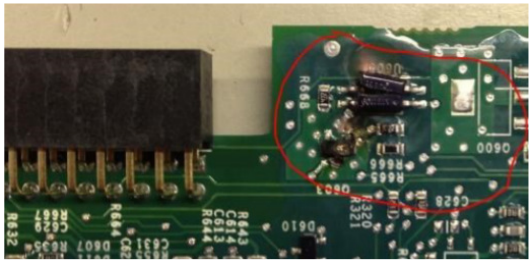

(b) Failure of the Common Mode Choke at Gate Driver - IGBT Interface



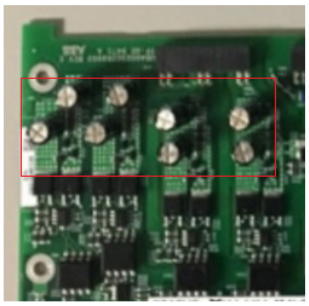
(c) Delamination of Optical Fiber under Environmental Conditions



(d) Failure of Power Supply's MOSFET



(e) Failure at Some of Control Circuitry



(f) Degradation of Gate Driver Capacitance

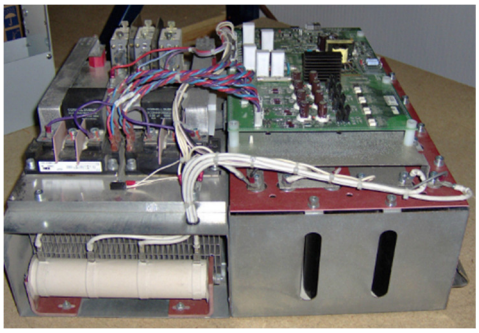
Fig. 3.15 Frame R1-R3 ABB ACS580 MV Power and Control PCBs failures [58, 60].

## 3.3. CHB Power Cells Long-term Reliability

An important point to focus on is the long-term reliability (lifetime) of the power cell components. Typically, power cell designs consider two aspects to gain a competitive advantage: size and cost. Fig. 3.16 and Fig 3.17 present examples for power cells designs from different manufactures. Power semiconductors; DC-bus capacitors; heatsinks; and circuitry for gate driving, cell control, power supply, and communications are packed densely in a power cell. As a result, thermal and environmental stresses imposed on power cell components are intensified. These stresses cause degradation of power cell components and eventually cause significant percentage of power cell faults and failures as illustrated in the previous sections. Other factors may result in increasing these stresses as shown in Fig. 3.9 such as cooling system and other issues due to operation in harsh environments.

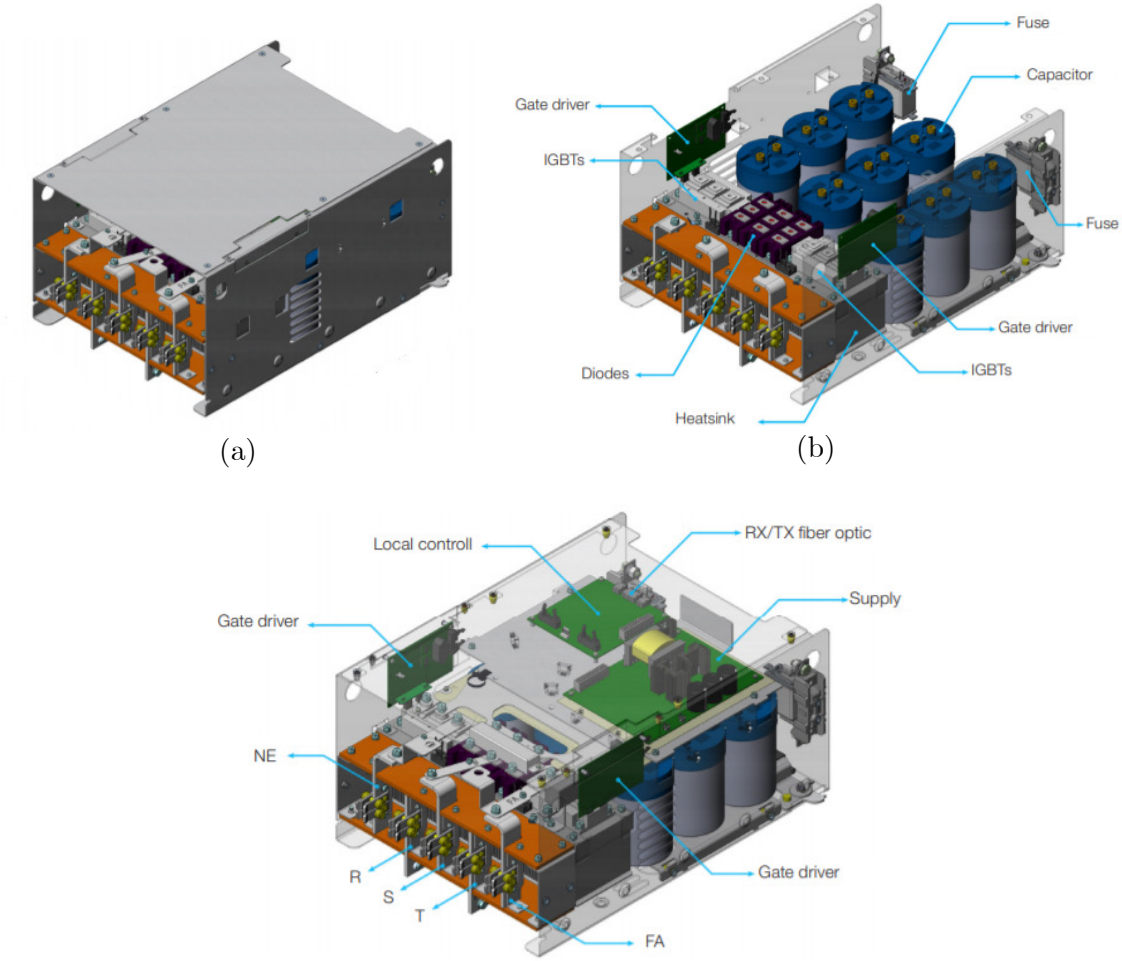
Another factor is the reluctance of some customers to follow the routine maintenance instructions such as changing the inlet air filter or preserving good operational conditions and environmental protection for the converter. These issues and unrecommended practices may result in over-temperature events, which is taken care of by the converter protection system through over-temperature trip of power cells. However, such protective action does not counteract the long-term degradation effects of power cells components, which cause components failures.

(a) Hiconics HIVERT [61]



(b) Legacy Robicon [59]

Fig. 3.16 Examples for Power Cell Designs.




(a) (b)

(c)

Fig. 3.17 MVW3000 Power Cell from WEG [33].

The long-term reliability of power cell is dictated by the reliability of its constituents such as power semiconductors, DC-bus capacitors, PCBs and low power and signal electronic components. Typically, these components are required to function in harsh conditions that are determined by application specific loading profile and operating environment from one side and converter design choices on the other side [45]. Operating under harsh thermal stresses is one of the conditions to which significant percentage of components' faults and failures are attributed.

The rest of the section presents a detailed discussion on thermally excited long-term reliability issues of IGBTs, DC-bus, low power and signal electrolytic capacitors, and control PCBs.

### 3.3.1. Power Semiconductors Long-term Reliability under Thermal Stresses

#### a) Failure Mechanism

CHB power cells employ bond-wire diode and IGBT modules as shown in Fig. 3.18. Typically, more thermal stresses are exerted on IGBT modules than grid frequency rectifying diode modules due to switching at higher frequency.

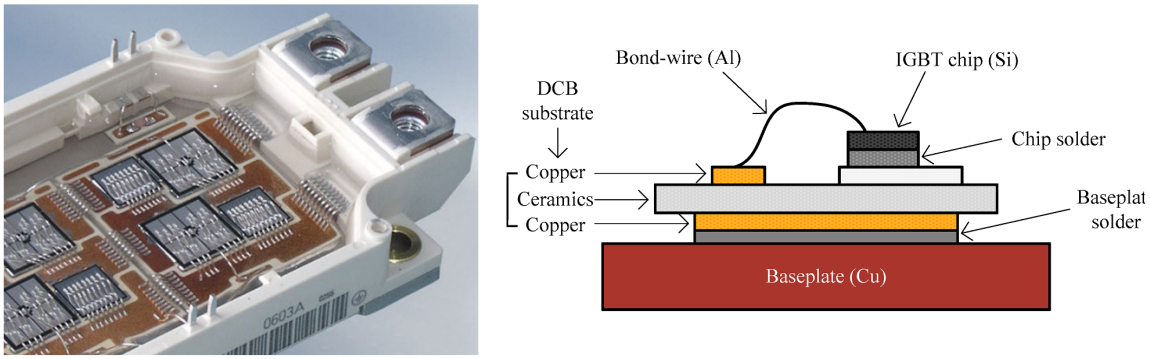



Fig. 3.18 IGBT Module Structure [62].

In normal operation, IGBT modules keep switching between on and off states. Conduction and switching power losses associated with IGBT modules operation generate pulsating heat flux at the chip (junction). The repetitive heating and cooling of the junction results in temperature cycling. The heat flux produced at the junction flows through the thermal path across the different layers of the IGBT modules towards the case (or heat sink). Since different layers of IGBT modules have different thermal conductivity and capacitance as shown in Fig. 3.18, a temperature gradient along the thermal path takes place [62, 63]. Fig. 3.19 shows the temperature cycles at the junction and the case under power cycling. At the junction, average and the peak-to-peak temperature fluctuations are higher than that at the case. Temperature fluctuations along the thermal path cause repetitive expansion and contraction of the layers forming the path. Due to the difference in the coefficient of thermal expansion (CTE) between adjacent layers in the package as shown in Fig. 3.18, shear stresses are exerted on interfaces between different

material layers [64, 65]. These stresses result in thermo-mechanical fatigue of material layers of the package [66, 67].

**b) Failure Modes**

Fig. 3.20 shows several important package failure modes caused by thermo-mechanical fatigue. These failure modes degrade the mechanical structure of the package and eventually cause IGBT module to fail [68 - 73]. Fig. 3.20a shows bond-wire degradation in the form of lift-off, heel cracks, or pad cracks taking place depending on several factors including the geometry of the bond-wires and the inherent manufacturing defects [68, 74]. Solder degradation takes the form of solder cracks or solder delamination as shown in Fig. 3.20b [75, 76]. Metallization degradation takes the form of metallization reconstruction as shown in Fig. 3.20c.

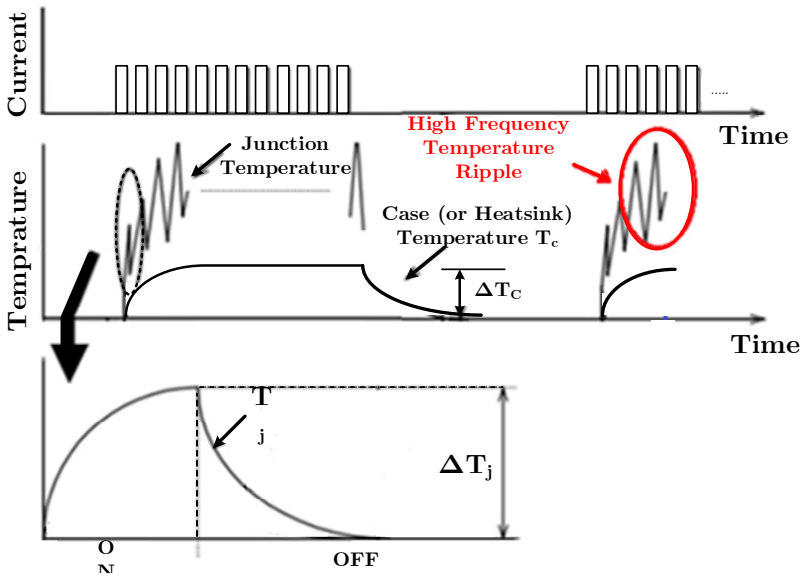



Fig. 3.19 Temperature Fluctuations at the Junction and the Case Under Repetitive Heating and Cooling of the Junction.

Bond-wire degradation raises the current density in the intact bond-wires. This may cause hot spots formation in the intact bond-wires and finally lead to their melting as shown in Fig. 3.20d. Another possibility is the formation of the hot spots at the bond-wire pads. As a result, melting of the metallization near the intact bond-wire takes place as seen in Fig. 3.20e [77]. Another possibility for the formation of the local hot spots is shown in Fig. 3.20f, the current distribution formed by interaction of bond-wire degradation and metallization reconstruction results in sporadic melting across the metallization [77]. The damage, shown in Fig. 3.20g, may happen when junction temperature reaches the level at which widespread melting of the metallization layer starts**.** This mainly happens due to severe degradation of the solder or wide scale metallization reconstruction.

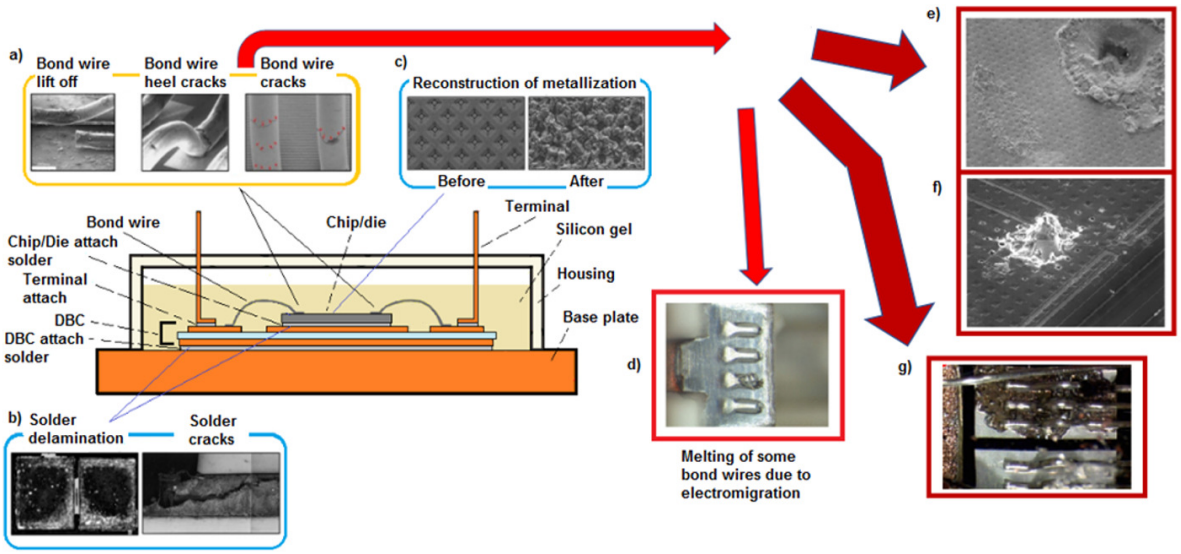



Fig. 3.20 IGBT Module Degradation and related Failures under Thermal Stresses [62, 68, 74, 77].

### c) Lifetime Estimation

Fig. 3.21 summarizes the process required to estimate the lifetime of a converter considering power switches thermal-mechanical failure modes for a given mission profile. Operation conditions are used to calculate losses and junction temperatures of power switches. The Junction temperature is then used to estimate the junction temperature cycles at $\Delta T_j$ through a cycle counting algorithm such as Rainflow [77-79]. Then, number of cycles-to-failure at $\Delta T_j$ is calculated using one of the lifetime model given in Table 3.1. For industrial IGBT modules, CIPS 2008 model is commonly employed [77-79]. Finally, by means of a cumulative damage model such as Miner's law [77,-79], calculated junction temperatures cycles at $\Delta T_j$ and number of cycles-to-failure are used to estimate lifetime of the converter given the mission profile. Estimated lifetime only considers the impact of thermo-mechanical stresses.

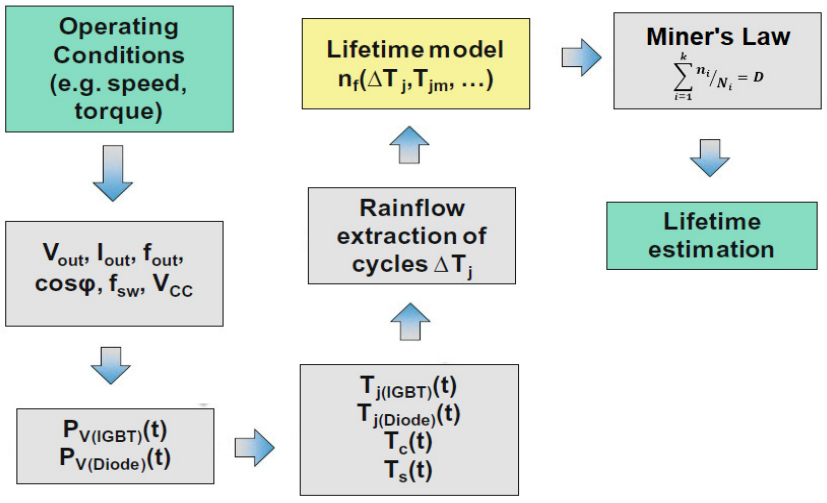



Fig. 3.21 Converter Lifetime Prediction under Thermo-Mechanical Failure [78].

Table 3.1 Lifetime Models of Power Modules under Power Cycling [77].

| | **LESIT [80]** | **CIPS 2008 [81]** | **SKiM63 [82]** |
|---|---|---|---|
| **Life Equation** | $A\Delta T_j^{\alpha} \times e^{\left(\frac{E_a}{k_B \cdot T_{jmean}}\right)}$ | $A\Delta T_j^{\beta_1} t_{on}^{\beta_3} I^{\beta_4} V^{\beta_5} \times D^{\beta_6} e^{\left(\frac{\beta_2}{T_{j\min}+273}\right)}$ | $A\Delta T_j^{\alpha} ar^{\beta_1 T_j+\beta_0} \times \left(\frac{C+t_{on}^{\gamma}}{C+1}\right) e^{\left(\frac{E_a}{k_B \cdot T_{jmean}}\right)} f_{Diode}$ |
| **Usage** | Standard modules with $Al_2O_3$ substrates.<br>Packages built with 1990 technology | Standard modules with $Al_2O_3$ substrates.<br>Not valid for modules built with AlN and AlSiC.<br>Packages built with 2000 technology | Solder-free module.<br>Packages built with 2000 technology |
| **Para-meters** | $k_B$ [JK$^{-1}$] = 1.380 x 10$^{-23}$<br>$E_a$ [eV] = 0.618<br>$a$ = -5.039 | $\beta_1$ = -4.416, $\beta_2$ = 1285<br>$\beta_3$ = -0.463, $\beta_4$ = - 0.716<br>$\beta_5$ = -0.761, $\beta_6$ = -0.5 | $\beta_1$ = -4.416, $\beta_2$ = 1285<br>$\beta_3$ = -0.463, $\beta_4$ = - 0.716<br>$\beta_5$ = -0.761, $\beta_6$ = -0.5 |

### 3.3.2. DC-bus Electrolytic Capacitors Long-term Reliability under Thermal Stresses

As discussed before, CHB power cells employ DC-link Aluminum electrolytic capacitors. In addition, they may utilize small signal aluminum electrolytic capacitors in their control boards, power supplies, and gate drivers. Fig. 3.22 presents examples for those capacitors. The wide application range of Aluminum electrolytic are due to their high volumetric efficiency, high ripple current capability, good reliability, and their excellent price/performance ratio.

(a) Screw Terminals Power Capacitor from EPCOS.


(b) Snap-in Terminal Power Capacitor from Jianghai.

(c) Small Signal capacitors from Panasonic.

Fig. 3.22 Electrolytic Capacitors.

**a) Construction**

Fig. 3.23 shows the basic construction of an aluminum electrolytic capacitor. As all capacitors, an Aluminum electrolytic capacitor consists of two electrically conductive material layers, which are separated by a dielectric material layer. The anode is an aluminum foil with an enlarged surface area. The dielectric layer is Aluminum oxide layer ($Al_2O_3$); it is built up on the anode during a forming process. The cathode, different from other capacitors, is a conductive liquid, which is the electrolyte. In order to pass current from capacitor's terminal to the electrolyte, a second aluminum foil used to form a large surface contact area called the cathode foil. The electrolytic material is contained in absorbent paper layer. In addition, the paper layer works as a separator between the two aluminum foils. This prevents electric short-circuits and ensures the required dielectric strength between the two foils.

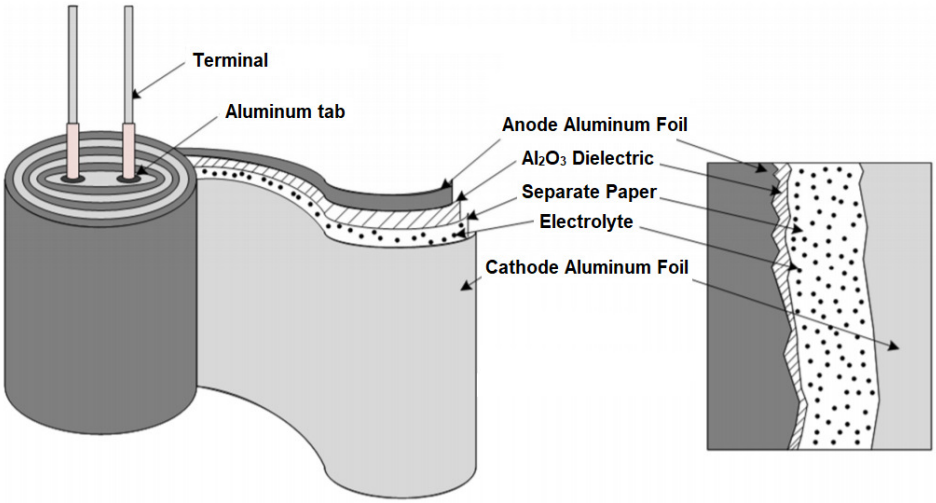



Fig. 3.23 Electrolytic Capacitors Structure: Winding and Layers [83-86].

**b) Equivalent Circuit**

From a simplified equivalent circuit point of view, a series connection of an ideal capacitor C, resistor ESR, and inductor ESL as shown in Fig. 3.24 can capture the terminal electrical characteristics of a capacitor. The capacitor element represents capacitance. ESR represents the dielectric losses and resistance of the electrolyte, foils and the terminals. ESL represents parasitic inductance of capacitor winding and the terminals. The ESL only depends on the frequency, whereas C and ESR depend on frequency and on temperature as shown in Fig. 3.25.


Fig. 3.24 Simplified Equivalent Circuit of a Capacitor [83-86].

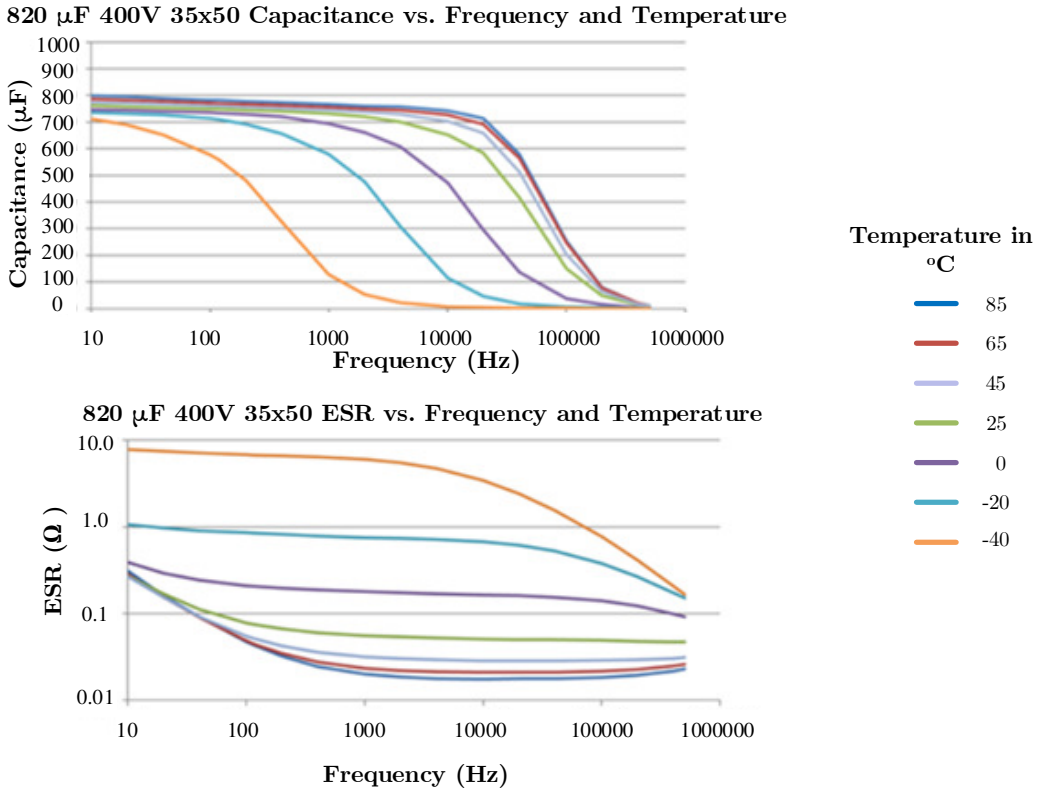



Fig. 3.25 Equivalent Circuit Parameters Variation with Frequency and Temperature [84].

### c) Failure Mechanisms and Modes

In CHB power cells, electrolytic capacitors in either DC-bus, control, or power supply circuits experience high temperature and current stresses. These stresses result in long-term reliability issues due to electro-chemical degradation of the capacitors. This eventually leads to failures. From equivalent circuit perspective, electro-chemical degradation results in shifts in C and ESR values with respect to the healthy case measured under same temperature and frequency conditions.

Electrolyte evaporation is considered the primary cause for capacitor's parameter shifts. It causes increased capacitor's parameter shifts, which leads to more losses and increased internal temperature. This in turn causes more electrolyte evaporation and more gas pressure, and may eventually lead to capacitor's can explosion [83, 86, 87].

Other important causes are degradation of the oxide layer and the degradation of the anode and cathode foil. Typically, under combination of voltage, temperature and current stresses, all these causes interact and accordingly result in shifts in C and ESR values. Fig. 3.26 presents the 20 % shift in C and ESR due to electro-chemical degradation, which marks capacitor end-of-life.

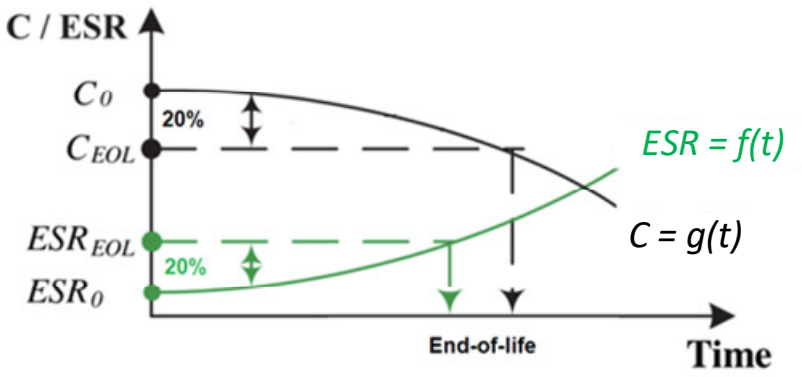



Fig. 3.26 Shifts in C and ESR Values due to Degradation [83, 88].

**d) Lifetime Estimation**

Electrolyte capacitor manufacturers provide empirical formulas to estimate the lifetime of their products based on statistical analysis of accelerated life tests

performed on their products [89-91]. These formulas follow the well-known 10ºC rule, which is a version of Arrhenius rule. In addition, these formulas take into account the effect of applied voltage and self-heating caused by the total ripple current.

Eqns. 3.1-3.6 present Aluminum electrolytic capacitor lifetime model provided by Jianghai Europe [89]:

$$L_e = L * K_r * K_T * K_V \tag{3.1}$$

,where $L_e$ is the expected lifetime under the actual conditions, $L$ is the lifetime under rated ripple current and rated temperature, $K_r$ is the ripple factor, $K_T$ is the temperature factor, and $K_V$ is the voltage factor. The ripple current factor $K_r$ equation is as follows:

$$K_r = K_i^{A*\frac{\Delta T_0}{10K}}, A = 1-(\frac{I}{I_0})^2 \tag{3.2}$$

,where $I$ is the actual current, and $I_0$ is the rated ripple current at the rated temperature, $\Delta T_0$ is the core temperature rise of the capacitor (typically 5 ºK for $T_0 =$ 105ºC and 10ºK for $T_0 =$ 85ºC), and $K_i$ is defined as (for $T_0 =$ 105ºC, $I > I_0$, and $K_i = 4$; $I < I_0$ and $K_i = 2$, for $T_0 =$ 85ºC, $K_i = 2$). If the actual ripple current component is at a frequency different from that of the rated ripple current, weighting factors are used to refer the actual current ripple components at different

frequencies to the frequency of the rated ripple current. The following equation calculate the effective actual ripple referred to the frequency of the rated ripple current:

$$I = \sqrt{\left(\frac{I_{f1}}{F_{f1}}\right)^2 + \left(\frac{I_{f2}}{F_{f2}}\right)^2 + \ldots + \left(\frac{I_{fn}}{F_{fn}}\right)^2} \tag{3.3}$$

,where $I_{f1}....I_{f2}$ are the ripple current components at different frequencies, and $F_{f1}....F_{fn}$ are the frequency weighting factors at different frequencies.

The temperature factor $K_T$ equation is:

$$K_T = 2^{\frac{T_0 - T}{10K}} \tag{3.4}$$

,where $T_0$ is the rated temperature, and $T$ is the actual temperature.

The voltage factor $K_V$ is as follows:

- For radial electrolytic capacitor,

$$K_V = 1 \tag{3.5}$$

- For Snap-In and Screw-Terminal electrolytic capacitor,

$$K_V = (\frac{U_0}{U})^n \tag{3.6}$$

,where $U_0$ is the rated voltage, $U$ is the actual voltage, n is defined as: for $1 < U_0/U < 1.25$, n = 5; $1.25 < U_0/U < 2$, n = 3; $2 < U_0/U$, n = 1.

### 3.3.3. PCB Long-term Reliability under Thermal Stresses

#### a) Failure Mechanisms and Modes

As discussed previously, faults or failures may occur in power cell due to failures in control, signal conditioning, power supply, or other auxiliary circuitry. Important portion of these failures are attributed to issues in PCB assembly such solder joint fatigue, corrosion, and vias fractures as shown in Fig. 3.27. Temperature cycling are the root cause for solder fatigue and vias fractures, while harsh environmental conditions are the root causes for corrosion. Solder degradation at surface-mount sites accounts for a high percentage of PCB long-term reliability issues. Therefore, solder joints are considered one of the weakest points in the electronic assembly.

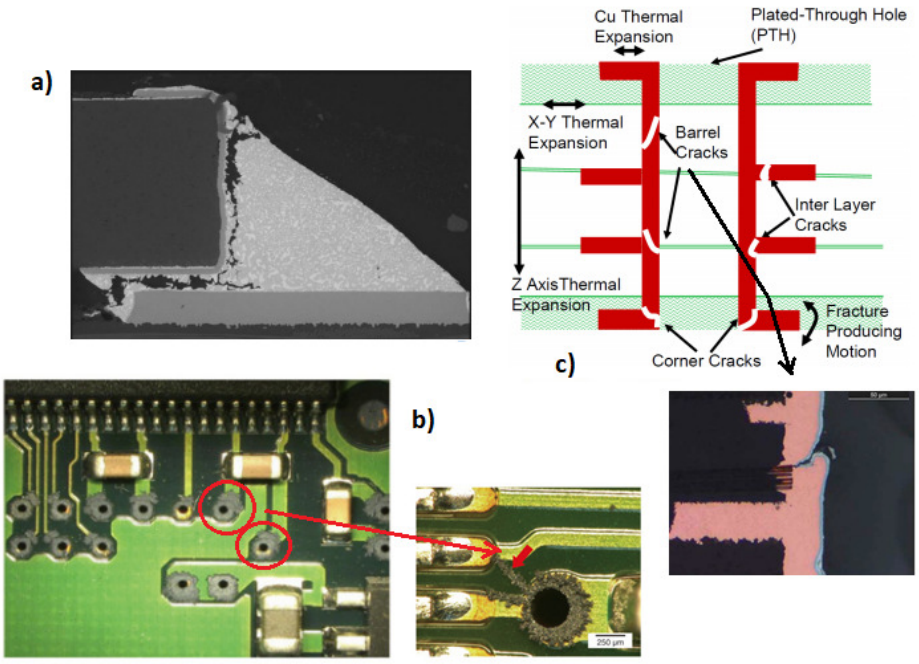



Fig. 3.27 PCB Failures due to Long-Term Stresses [92-96].

Fig. 3.28a shows a surface-mount component (SM) soldered to a printed circuit board (PCB). During normal operation, the power loss inside the component produces a heat flux that flows out of the component's package to the PCB tracks through component's leads. As a result, a temperature gradient is set up such that temperatures at the package, leads and solder joints, and the PCB are different. Cyclic power losses give rise to cyclic temperature fluctuations. Since the coefficient of thermal expansion of package, lead, solder, and PCB materials are different, therefore cyclic thermomechanical forces are generated at material interfaces. Fig. 3.28b shows the thermomechanical forces acting on the solder. A cyclic shear stress is imposed on the solder layer. In addition, other temperature-related effects play an important role in degrading the solder joint through fatigue.

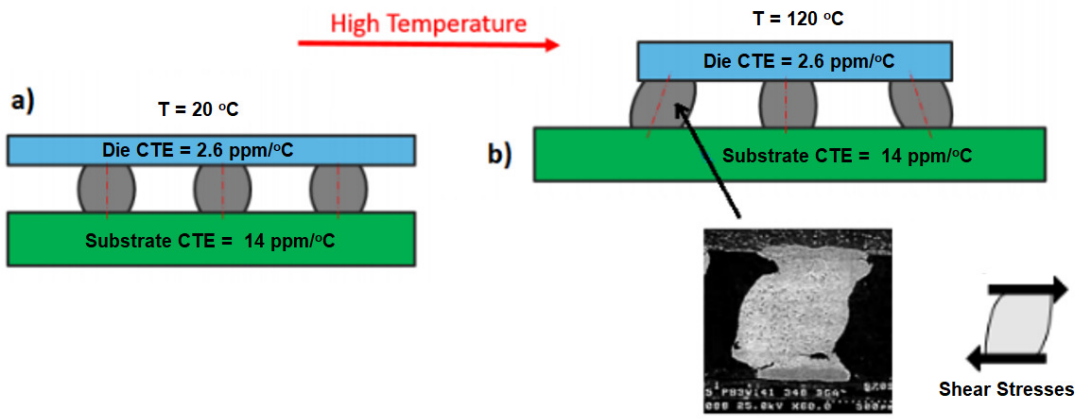



Fig. 3.28 Classical PCB Solder Joint Fatigue [97-99].

Lead and package geometries affect the response of solder joint to different stresses. In addition, solder geometry dictates the stress distribution across the interface between the PCB and the solder joint. Moreover, due to solder defects and system effects, real stresses are multimodal as shown in Fig. 3.29 [100]. This is in contrast to the classical shear stress assumed in literature while analyzing solder degradation [97-99].

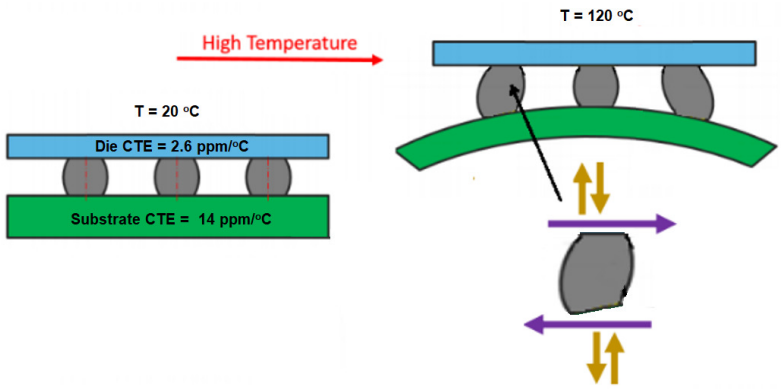
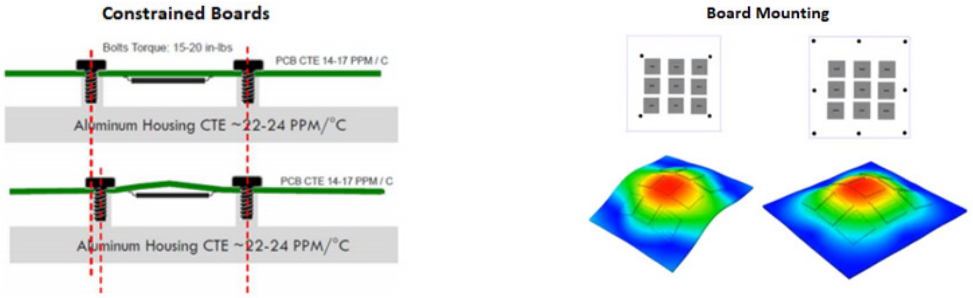



Fig. 3.29 Real Case PCB Solder Joint Fatigue [100].

Fig. 3.30 presents some of these system effects such as over-constrained boards, housing interaction, and mirroring; potting, coating, and under-filling; glass styles, and board thickness.




(a) (b)

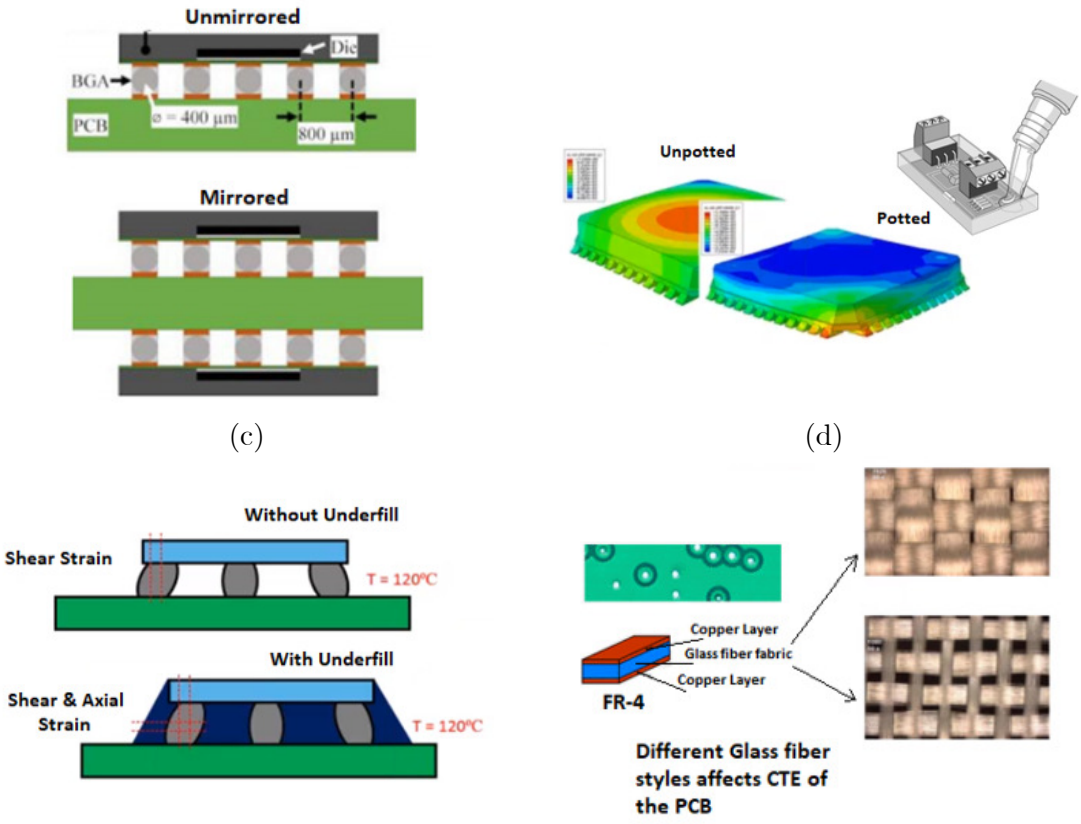



Fig. 3.30 Causes on PCB Solder Joint Degradation [100, 101]

Traditionally, Pb-based solder alloys were used in the electronics industry. However, due to RoHS requirements, Pb-free solder alloys such as SAC305 and others become more common these days [93, 102]. Solder microstructure governs how it reacts to stresses, therefore, it has a significant effect on the long-term reliability of the solder joint. Fig. 3.31 shows the microstructure of aging SAC305 solder. The figure shows a crack at the intermetallic layer formed at the interface of the PCB substrate metallization and the solder bulk, as interfacial layer is more

brittle than elsewhere in the solder. It also shows bulk intermetallic regions formed in the solder bulk affecting the mechanical integrity of the solder and behavior against cyclic stresses.

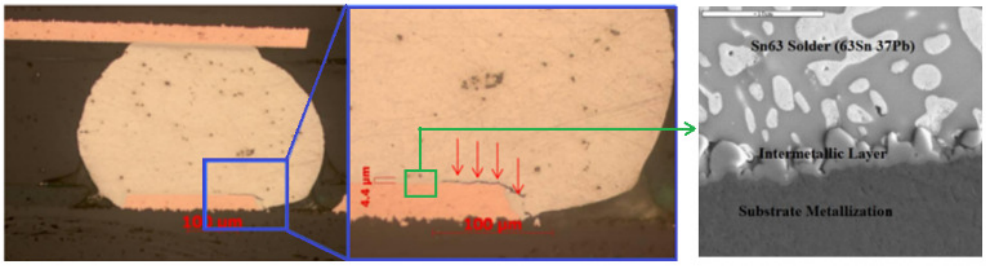



Fig. 3.31 Degradation of SAC Solder [97, 102].

**b) Lifetime Prediction**

Several empirical, semi-empirical, and physics-based models have been proposed in literature for solder joint fatigue lifetime prediction. Eqn. 3.7 presents Norris and Landzberg model [99-106]. It is a famous empirical model, which makes solder fatigue life prediction more applicable. In addition, it is adopted in the JEDEC qualifications [107]. Since it is an empirical formula, it requires performing accelerated life test for parameterization. The form given in Eqn. 3.7 represents the acceleration factor format, which computes lifetime consumption under condition $B$ with respect to the case under condition $A$.

$$AF = \frac{N_B}{N_A} = \left(\frac{\Delta T_A}{\Delta T_B}\right)^a * \left(\frac{f_B}{f_A}\right)^b * \exp^{(c*[\frac{1}{T_{\max\_B}} - \frac{1}{T_{\max\_A}}])} \quad (3.7)$$

Typically, solder fatigue starts at local discontinuities such as stress concentration areas near solder-to-substrate interface. Plastic strain accumulates each cycle resulting in failure. In Norris and Landzberg model, plastic strain range is assumed proportional to the temperature excursion range. In addition, the model introduces two more factors to account for the effects of temperature-cycling frequency ($f$) and the maximum temperature ($T_{\max}$) of the solder material. Table 3.2 presents Norris and Landzberg model parameters for Sn/Pb solder and Pb-free solder.

Table 3.2 Norris and Landzberg model parameters [108, 109].

| | |
|---|---|
| **Sn/Pb solder**<br>63Sn37Pb | a = 1.9, b = 0.33, and c = 1414 |
| **Pb-free solder**<br>Sn3Ag0.5Cu(SAC305) | a = 2.3, b = 0.3, and c = 4562 |

### 3.3.4. Addressing Long-term Reliability under Thermal Stresses

Addressing thermally induced long-term reliability issues of a converter or a power cell can be done either in the design stage or in the field operation. Fig. 3.32 presents means to address converter's or power cell's long-term reliability. In design stage, the aim is to produce better designs that suffer less thermally induced degradation effects in the field. Given a design, the aim in the field is to prevent failures and possible catastrophic consequences before happening if these degradation effects take over.

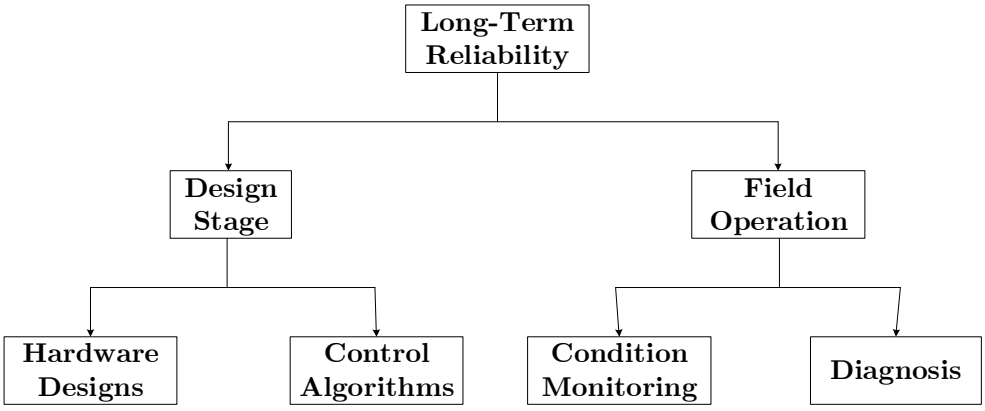



Fig. 3.32 Addressing Thermally Induced Long-Term Reliability [45, 110-120].

Converters or power cells should be designed while considering long-term reliability under application-specific thermal stresses. The design task includes the power circuit topology, the control strategy, components ratings and technologies, circuit layout, cooling system, and mechanical packaging. Reliability of different designs needs to be quantified to allow for making comparisons based on expected reliability. This design approach is commonly referred to as Design-for-Reliability approach [45, 110-116]. Fig. 3.33 illustrates the reliability assessment process for a design considering thermal stresses.

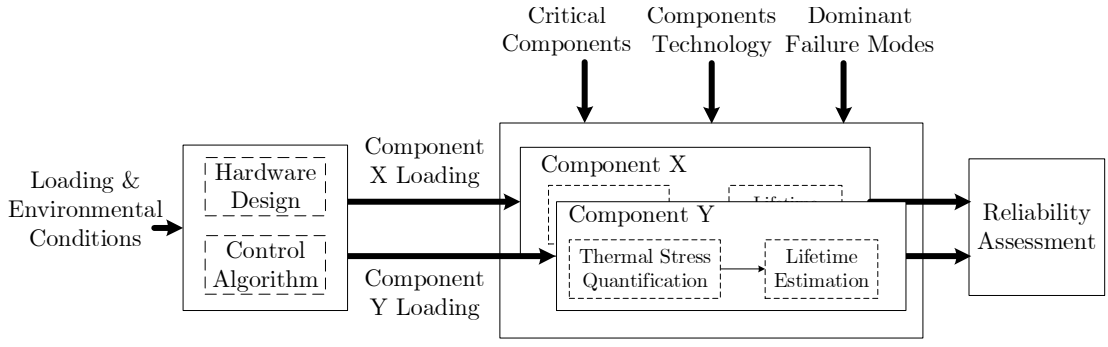



Fig. 3.33 Long-Term Reliability Assessment under Thermal Stresses [45, 110-116].

Given a converter or a power cell design, loading, and environmental conditions; electrical and thermal loading on critical components are quantified and then long-term reliability of the design is assessed based on the long-term reliability of the critical components. The assessment is conducted through calculating the expected lifetime of the critical components under the application-specific stresses. The critical components are the components whose calculated lifetime is the lowest, whose degradation can turn into a catastrophic failure, or whose preventive maintenance process is complicated and expensive. The components with minimum lifetime determine the upper bound of the converter's or the power cell's lifetime. The significance of the calculated lifetime in absolute sense differs from one application to another. For example, general industrial drive applications that employ CHB converters are required to change the full electrolytic DC-bus capacitance every 7 years as recommended by drive manufacturers' lifetime calculations. These applications can afford this relatively demanding preventive maintenance routine in favor of initial investment cost. However, for applications that cannot afford similar maintenance routines, the required expected lifetime is 10-15 years. The converter manufacturer may provide a solution based on another power circuit topology, a special control algorithm, a different capacitor technology, or an oversized design with the same capacitor technology [110-116].

It should be noted that in addition to long-term degradation of the converter's components, they may experience random failures due to recognized or unrecognized causes. Typically, the failure rate is used to quantify random failure reliability, in which failure rate of a converter is less than failure rates of its components. It is important to consider random failure reliability in converter reliability assessment. The work will touch upon reducing the random failure probability through reducing the system complexity.

The design-for-reliability approach is based on assumed application loading profile and operating environment. Nonetheless, converter's components may end up operating in harsher conditions. This is because of inaccurate application loading assumptions, or operational issues and unrecommended practices that converter experiences in the field as discussed in the previous section. Another important aspect of the design-for-reliability approach that it is statistical. That is even under the ideal field assumptions; the approach does not take into account unit-to-unit inherent strength variability [110, 117-120].

Consequently, for critical applications, relying solely on design-for-reliability approach is not sufficient to tackle thermally induced long-term reliability issues. As it provides means to produce reliable designs that suffer less degradation effects, but not to eliminate them and their associated possible failures. This raises the

need for tools to detect faults (degradation of performance or partial loss of function) before turning into failures (complete loss of function). This requires assessing the health of the asset (the converter and its components) in the field through the monitoring operation conditions, key performance parameters, or degradation precursors [110, 117-120]. Accordingly, catastrophic failures prevention and maintenance optimization are achieved. Fig. 3.34 summaries asset health tracking and compares between different failure prevention methodologies.

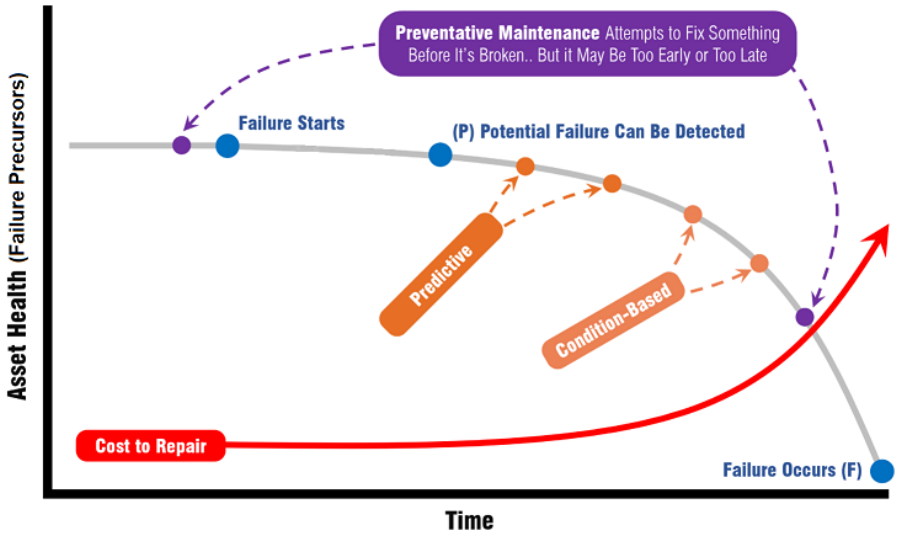



Fig. 3.34 Early Detection of Faults before Turning into Failures [121]

The thesis work focuses on addressing regenerative CHB topology reliability during design stage, while further discussion about reliability addressing during field operation is out of scope of the present work.

The proposed thesis work is meant to address regenerative CHB topology reliability through proposing novel front ends control schemes in order to:

1. Reduce Components Stresses to Improve Long-term Reliability
2. Reduce Component Count to Reduce Failure Random Probability
3. Achieve Other System Benefits (e.g., Cost, Size)

## 3.4. Summary

This chapter provided the necessary background on the failures and reliability of high power converters upon which thesis work has been developed. First, the chapter begins with a review on some failures and reliability related definitions. Afterwards, a detailed presentation of field failures of high power converters in general and CHB converter in specific has been covered. A detailed discussion on long-term reliability of CHB power cells has been addressed with focus on thermal induced long-term reliability issues. This discussion includes long-term reliability of power modules, electrolytic DC-bus capacitors, and PCBs and signal electronics. Subsequently, means to address long-term reliability issues of CHB power cells have been presented. Finally, thesis objective and the reliability challenges to be addressed have been stated.

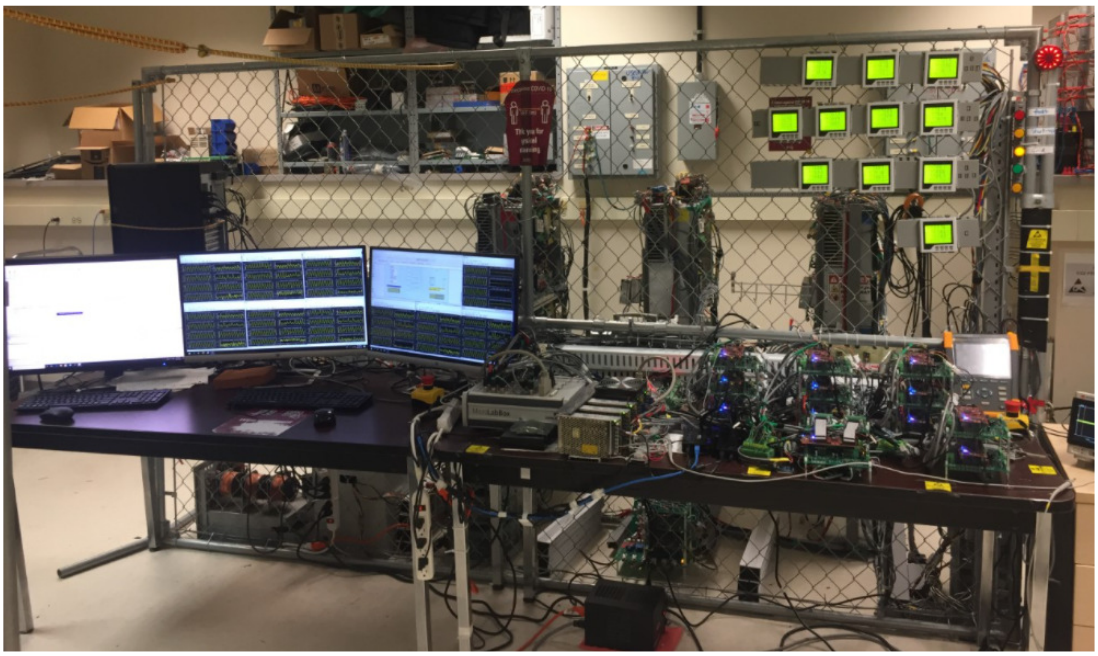
# Chapter 4

# Regenerative CHB Drive Lab Prototype

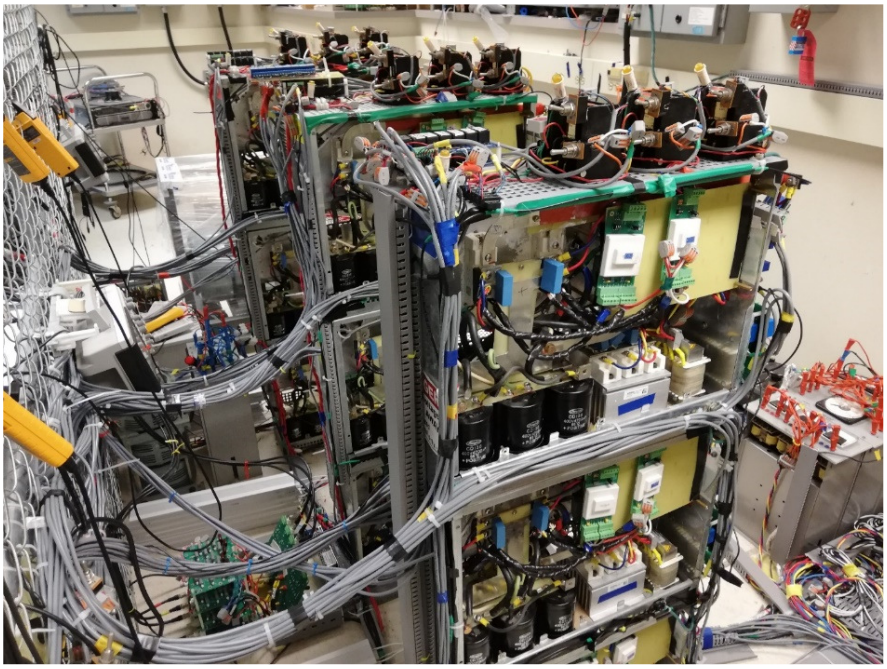
## 4.1.Prototype Overview

Fig. 4.1 presents an overview on the developed hardware prototype. It is a scaled down a 9-cell 7-level regenerative CHB drive. It has been developed for the experimental validation of research outcomes. The prototype is divided into two sections: power section and the control section. The power section includes phase shifting transformers; grid, load, and power circuit reconfiguration contactors;

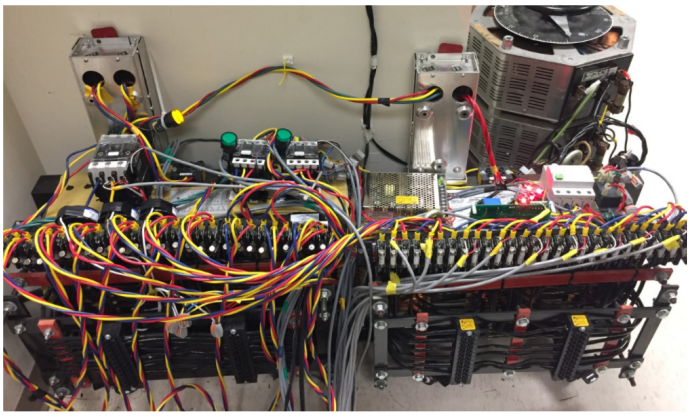
power cells; sensors boards; and power supplies. The control section includes controller boards, SCADA, interface boards, and power supplies.



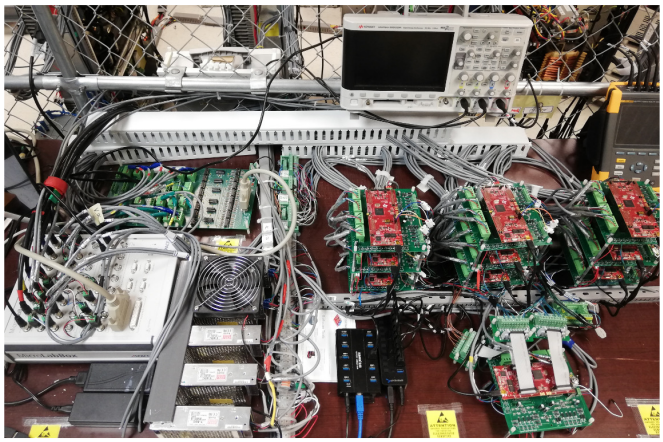
(a) Prototype Front View (Control – SCADA – Monitoring)



(b) CHB Power Cells (Power Section)



(c) Grid Connection Phase Shifting Transformers, Grid and Load Contactors, Grid Measurements (Power Section)



(d) Master Controller, Motor Controller, Cell Controllers, Power Supplies, and Interfacing Boards (Control Section)

Fig. 4.1 Prototype Overview.

## 4.2.Grid Connection Layout

Fig. 4.2 presents the grid connection layout including power circuit layout, protection, primary measurements, monitoring, and safety. The grid connection section consists of two phase-shifting transformers: 18-pulse transformer and 54-pulse transformer. The transformers operate mutually exclusive through switches.

The input to both transformers comes from a grid connection contactor, which is controlled by the master control board. Upstream of the grid contactor, primary measurements for voltages and currents are performed. They are sent to the master controller board for control and protection purposes, and are sent to meters for monitoring. Corresponding secondaries of each transformer are protected through fuses then connected in parallel to the respective power cell. The secondary voltages and currents measurements are sent to meters for monitoring.

A hardware safety circuit override the grid contactor in case of emergency or loss of power supply. An auxiliary grid connection cell was implemented for topology reconfiguration purpose.

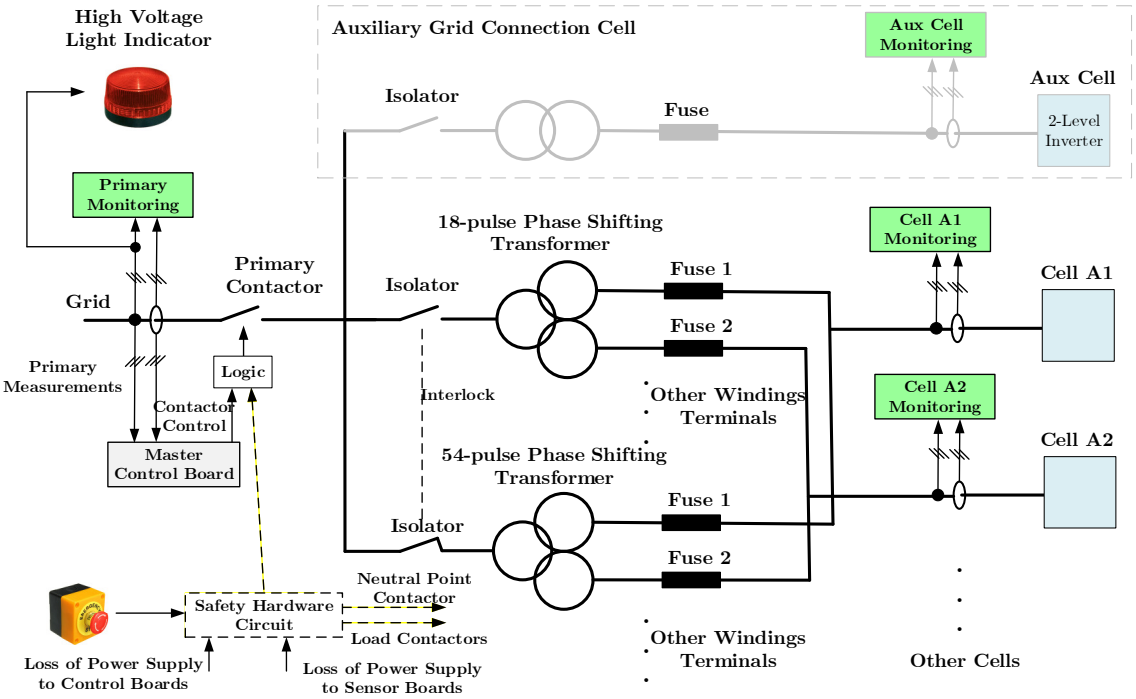



Fig. 4.2 Grid Connection Layout.

## 4.3.Converter Power Circuit Layout

Fig. 4.3 presents the power circuit layout including converter circuit layout, load connection, contactors, measurements, and safety. The power circuit is reconfigurable 9-cell cascaded H-bridge converter with auxiliary neutral point 2-level converter, auxiliary grid connection 2-level inverter, auxiliary 2-level inverter driving a load, and an auxiliary DC-bus tying these three converters. Two mutually exclusive contactors namely the neutral point contactor and the neutral point cell contactor are used to configure the power circuit.

To connect the CHB converter to the load, another two mutually exclusive contactors are used: the R-L load contactor and the motor load contactor. In addition, each power cell is placed between two mutually exclusive contactors: the cell input contactor and the bypass contactor. These contactors are used to isolate or bypass a power cell. All these contactors are controlled through the motor controller board.

Voltage and current measurements at the converter terminal, in addition to speed signal in case of motor load, are sent to the motor controller board for load side control and protection.

The auxiliary grid connection cell has its own grid connection contactor, and input voltages and currents, and DC-bus voltage measurements. The measurements

are sent to auxiliary grid connection controller board for control and protection, while the contactor is controlled by the auxiliary grid connection controller board.

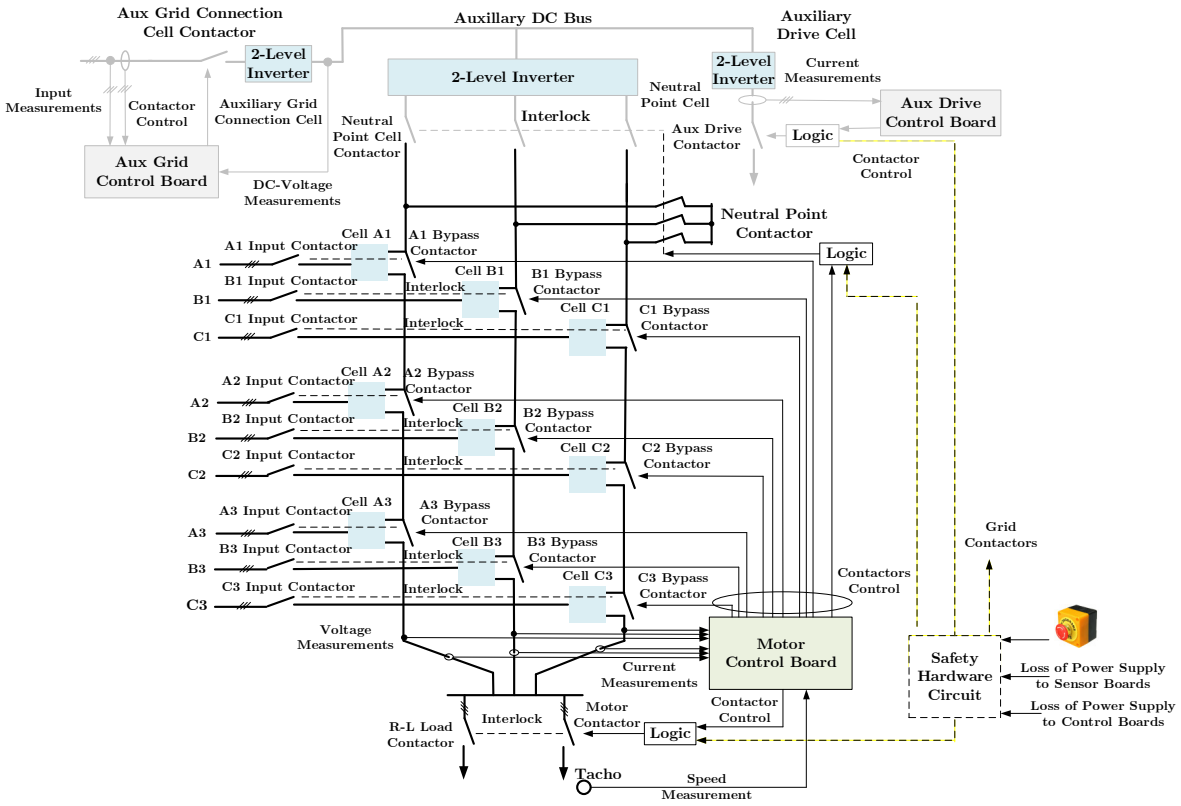



Fig. 4.3 Converter Power Circuit and Load Connection Layout.

The auxiliary drive cell also has its own load contactor and currents measurements. The measurements are sent to auxiliary drive controller board for control and protection, while the contactor is controlled by the auxiliary drive controller board.

The same hardware safety circuit discussed in previous section overrides the load contactors and auxiliary drive contactor in case of emergency or loss of power supply. An auxiliary grid connection cell is implemented for topology reconfiguration purpose.

## 4.4.Gating Signals Layout

Fig. 4.4 presents the power switches gating architecture including gating for power cell H-bridges, power cells AFEs, auxiliary grid connection converter, auxiliary drive converter, and the neutral point converter. The motor controller board is responsible for generating timely synchronized gating signals for power cells H-bridges and the neutral point converter.

Power cells AFEs receive gating signals from cells controller boards. The master controller is responsible for generating a synchronization signal to a cell controller board in each of the CHB phase. These cells are A2, B2, and C2 cell controller boards. Afterwards, cell A2 controller board generates a synchronization signal to the rest of the A cells controller boards, cell B2 controller board generates a synchronization signal to the rest of the B cells controller boards, and cell C2 controller board generates a synchronization signal to the rest of the C cells controller boards.

The auxiliary grid connection cell controller board generates gating signals for the auxiliary grid connection cell. This gating signal is synchronized with rest of the CHB AFEs gating signals based on the synchronization signal generated at the master controller board.

The auxiliary drive cell controller board generates gating signals for the auxiliary drive cell. It is not synchronized with the rest of the system.

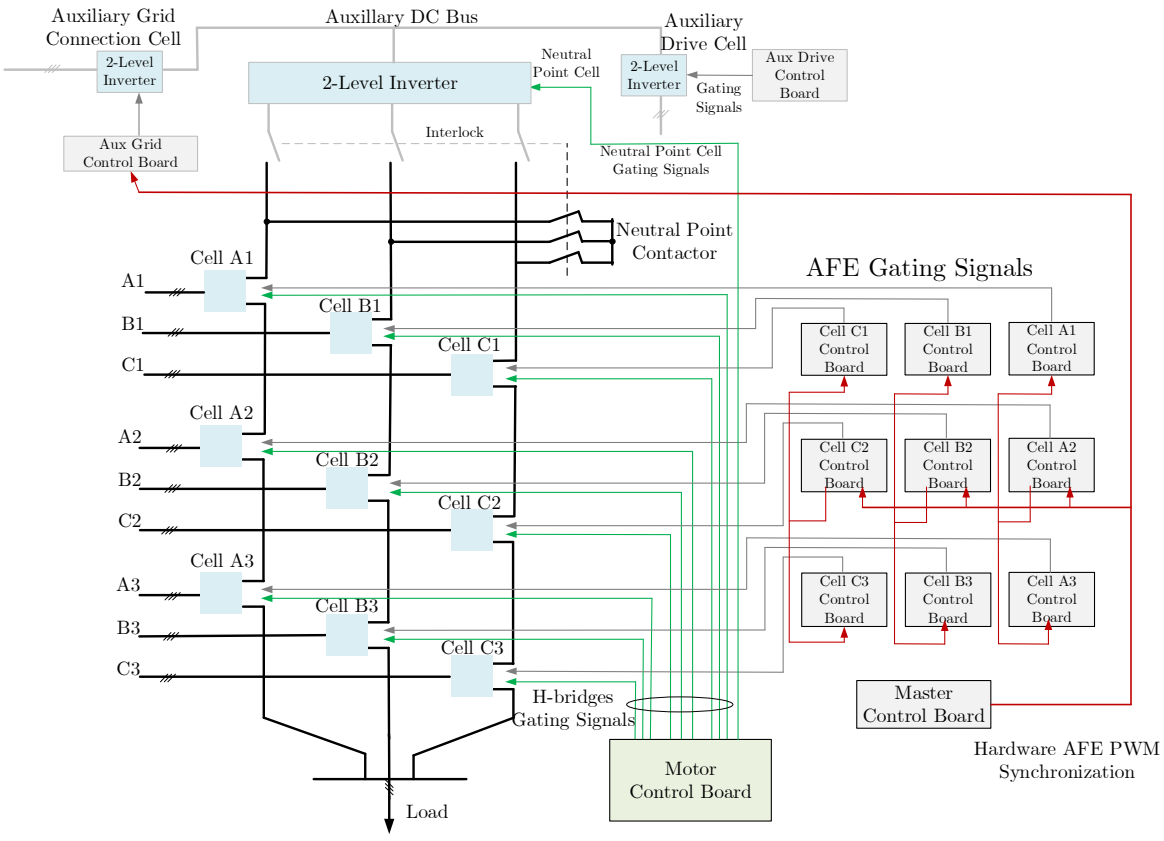



Fig. 4.4 Gating Signals Layout.

## 4.5. CHB Power Cell Layout

Fig. 4.5 presents the CHB power cell layout including power circuit layout, contactors, and cell measurements. The power circuit consists of DFE, H-bridge, DC-bus capacitance, AFE, cell AFE inductance, DC-bus chopper, chopper resistance.

Upstream of the cell lies the cell input contactor and at the output terminal of the cell lies the bypass contactors. These contactors are controlled by the motor controller board as mentioned in section 4.3. The motor controller board is as well responsible for generating gating signals for the H-bridge as illustrated in section 4.4.

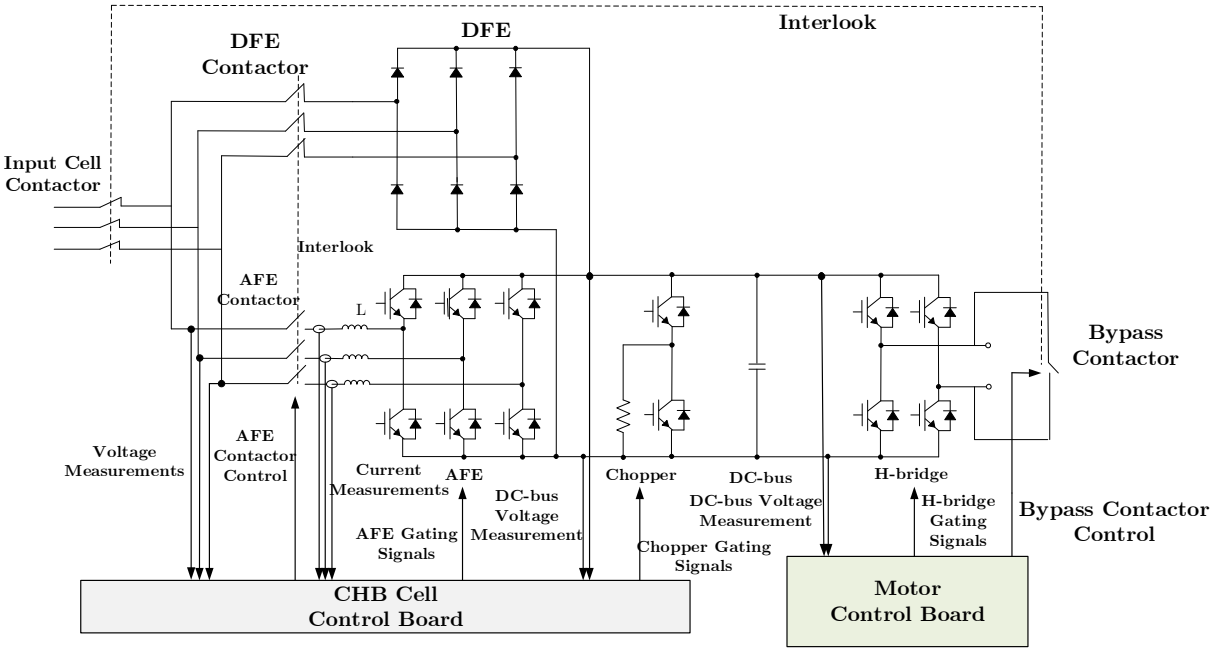



Fig. 4.5 CHB Power Cell Layout.

After the input contactor, the cell terminals are connected to both the DFE and the AFE. Two mutually exclusive contactors namely AFE contactor and DFE contactor are used to configure the cell as a diode front cell or an active front cell. Also, the AFE contactor is employed for AFE starting up and protection. The control of these two contactors is performed at the cell controller board.

Fig. 4.5 shows several measurements performed inside the cell. Input voltage is measured after the input cell contactor and before the AFE contactor. Input current measurements are performed after the AFE contactor. In addition, DC-bus voltage is measured. All these measurements are sent to the cell controller board for cell front end control and protection. Extra DC-bus voltage measurement is sent to the motor controller for advanced control.

For DC-bus overvoltage protection especially for motor load, a DC-bus chopper is used to connect a chopper resistance to the DC bus. The chopper gating signals are generated at the cell controller board.

## 4.6. Control System Layout and Tasks

Fig. 4.6 presents the control system architecture including controller boards, communication links between controller boards, and SCADA. There are three types of communication links employed in the control system: board-to-board digital

communication links for control variables transmission; board-to-board for logic communication links for modes setting and acknowledging; and board-to-Desktops for system configuration, supervisory control, and data acquisition.

The master board lies at the core of the control system architecture, in which it is involved in all the board-to-board communication, i.e. a star topology. Master-to-motor controller boards communication is based on bidirectional digital and the logic communication links. Master-to-cell controller boards communication is based on a broadcast of unidirectional digital and a cell specific bidirectional logic communication links. Board-to-desktop controller communication is based on bidirectional digital communication links. Light indicators are driven by the master controller and motor controller boards to indicate system important system states, and warning and fault conditions.

The motor controller is implemented on dSPACE MicroLabBox. The 11 cells controllers implemented on 11 TMS320F28379D boards. The master controller is implemented on TMS320F28379D. The SCADA is implemented using dSPACE ControlDesk for the motor controller, and Matlab/Simulink instrument control toolbox for master controller and cells controllers.

Table 4.1 illustrates the implementation and function details of the different control firmware components.

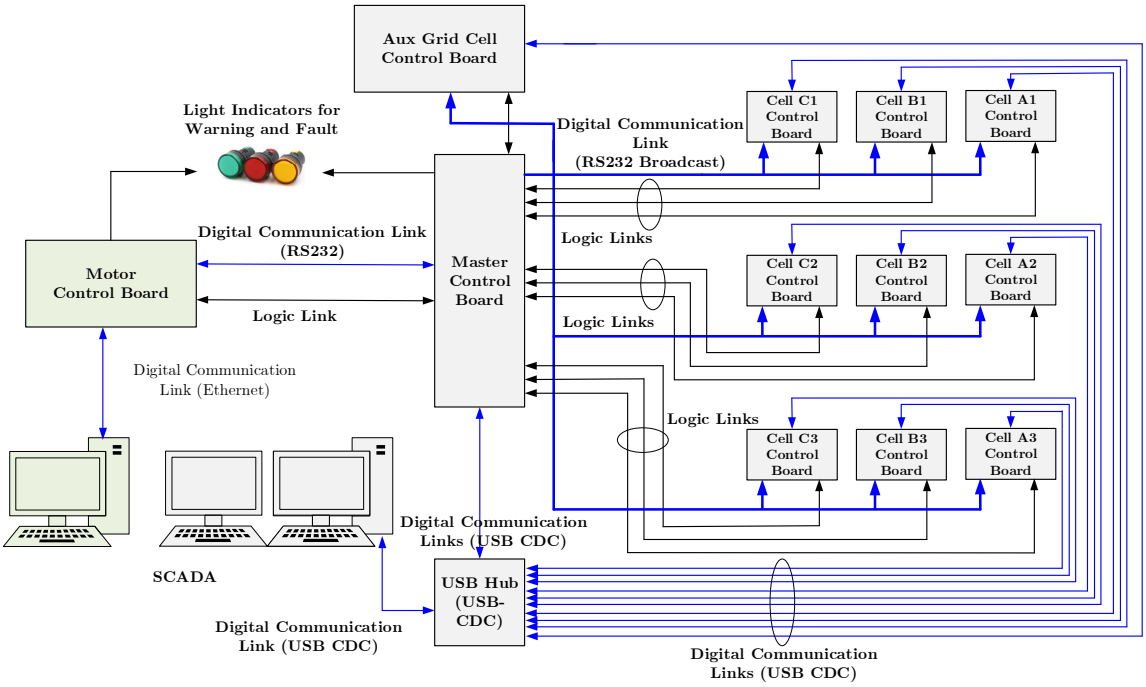



Fig. 4.6 Control system Layout.

Table 4.1. Firmware Implementation and Function in the Experimental Setup.

| Firmware | Implementation in System | Functions |
|---|---|---|
| **Motor Controller** | dSPACE dual Core and FPGA | - Motor/load-side state machine<br>- Phase-shifted multilevel PWM<br>- V/f and field oriented control (FOC)<br>- Motor protection functions<br>- Communications to master controller board (digital and Logic communication links)<br>- Communications to SCADA<br>- Various power-related, control-related, and communication-related faults diagnosis |
| **Cells Controller Tasks** | TMS32F28 Dual Core and CLA | - Cell state Machine<br>- Global 9 cells PWM Synchronization<br>- Regeneration control<br>- Cell Protection functions<br>- Communications to master controller board<br>- Communication to SCADA<br>- Various power related, control-related, and communication-related faults diagnosis |

| | | |
|---|---|---|
| **Master Board** | TMS32F28 Dual Core and CLA | - System State Machine<br>- Source for Global AFEs PWM Synchronization<br>- Centralized Synchronization and the multi-winding transformer model<br>- Control variables transmission between the motor side and AFEs<br>- Grid-side protection functions<br>- System protection coordination<br>- System Fault Diagnosis: Motor-side fault, a power cell fault, communication-related fault, and grid-related fault |
| **SCADA** | • Matlab/ Simulink instrument control toolbox<br>• dSPACE ControlDesk | - Comprehensive system monitoring<br>- System fault logging: Motor-side faults, power cells faults, and transformer and grid-related fault<br>- System Startup and shutdown coordination<br>- System configuration:<br>o Set operation modes<br>o Set parameters<br>o Override contactors<br>o Software emergency stop |

## 4.7. Summary

This chapter has presented an overview on the lab prototype utilized for experimental validation of the proposed research work in the coming chapters. The overview has included detailed schematic drawings for power circuit layout and control system architecture.

# Chapter 5

# Improvement of DC-Bus Capacitors Reliability for Regenerative CHB Motor Drives

## 5.1.Introduction

As discussed, capacitors are one of the most vulnerable components in the power converters [59, 83]. This vulnerability is more critical in the CHB topology. The CHB topology consists of multiple low voltage DC-buses. Thereby, to achieve the

required total energy storage, cost-effective high-capacitance capacitor technologies are employed.

Typically, Aluminum electrolytic capacitor technology is widely used for commercially available CHB drives [18-27, 59]. This capacitor technology degrades in an accelerated fashion under ripple current stresses. In the CHB topology, DC-bus capacitors experience high ripple current stresses due to the inherent instantaneous power unbalance existing in the CHB cells. Thus, CHB drives manufacturers are required to replace DC-bus capacitors every 7 years as a preventive maintenance routine against unscheduled downtime caused by DC-buses capacitors degradation [28, 58].

To enable regenerative capability, commonly, the CHB topology rely on AFEs to transfer power back to the grid, while during motoring condition, only diode rectification is required. However, in order to reduce Aluminum electrolytic capacitors degradation by mitigating capacitor current ripples, this chapter proposes a new control scheme for regenerative motor drives, in which AFE controller is utilized during motoring as a rectifier and during regeneration as an inverter. The AFE controller has two tasks: DC-bus voltage regulation, and DC-bus ripple reduction. Several research work have been done to achieve this [122-

130]. Nonetheless, rooms for improvement still exists to match motor drives requirements.

The proposed AFE controller is meant to address three main challenges:

1. High performance to suit the demanding performance requirements of the motor drives.
2. Compliance with grid connection harmonic requirements without the addition of costly, space consuming, and resonance prone harmonic filtering solutions.
3. No addition of extra measurement hardware, which increases cost and complexity.

## 5.2. Background

The following subsections discusses power cells inherent instantaneous power unbalance ripple currents' impact on Aluminum electrolytic capacitors lifetime.

### 5.2.1. Power Cell Inherent Instantaneous Power Unbalance

Fig. 5.1 shows instantaneous power flow during motor and regeneration for DFE and AFE power cells. $P_{\mathrm{DEF}}$ is the power flow in DFE, $P_{\mathrm{AFE}}$ is the power flow in the AFE, $P_{\mathrm{HB}}$ is the power flow in the H-bridge, $P_{\mathrm{C}}$ is the power flow through the DC-bus capacitor, and $i_{\mathrm{HB}}$ and $v_{\mathrm{HB}}$ are the H-bridge output current and voltage.

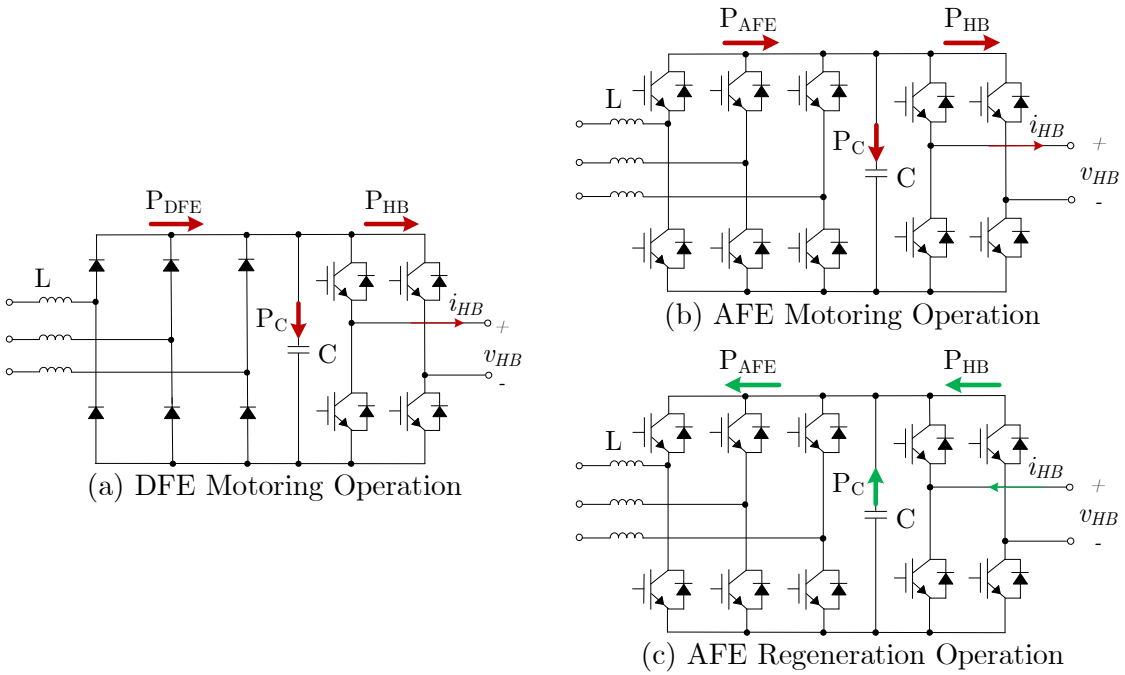



Fig. 5.1 Instantaneous Power Flow in Power Cell.

Assuming the power cell output operates at angular frequency $\omega_m$ and power factor angle $\phi$, $P_{\text{HB}}$ can be computed for either case of the DFE or the AFE as:

$$\begin{aligned} P_{HB}(t) &= v_{HB}(t)i_{HB}(t) = V_{HB}\sin(\omega_m t+\phi_v)I_{HB}\sin(\omega_m t+\phi_i) \\ &= \frac{1}{2}V_{HB}I_{HB}\cos(\phi_v-\phi_i)-\frac{1}{2}V_{HB}I_{HB}\cos(2\omega_m t+\phi_v+\phi_i) \end{aligned} \tag{5.1}$$

,where power factor angle $\phi$ is the angle difference between voltage angle $\phi_v$ and current angle $\phi_i$.

Eqn. 5.1 shows that H-bridge instantaneous power can be decomposed into two components: a zero frequency component and a pulsating component with double the H-bridge output frequency. Instantaneous power components due to switching harmonics have not been considered. On the other side, three-phase full-

bridge DFE instantaneous power can be decomposed into a zero frequency component and a pulsating component with six-times the grid frequency due to the six-pulse operation. This causes instantaneous power unbalance between DFE and the H-bridge. Since instantaneous power balancing holds by the laws of physics, the instantaneous power mismatch between DFE and H-bridge is supplied by the DC-bus capacitors as shown in Fig. 5.1a. Zero-frequency power mismatch results in ongoing increase or decrease of DC-bus voltage, while, pulsating power mismatch leads to DC-bus voltage ripples. Eqn. 5.2 presents an expression of DC-bus voltage ripple in which the DFE pulsating component is not considered. It shows that the angular frequency of the DC-bus voltage ripple is double the H-bridge output angular frequency. In addition, the magnitude of the voltage ripples is proportional to the output voltage and current magnitudes of the H-bridge, while inversely proportional to the H-bridge output angular frequency, DC-bus capacitance, and zero frequency component of DC-bus voltage.

$$\Delta v_{dc}(t) = -\frac{V_{HB} I_{HB} \sin(2\omega_m t + \phi_v + \phi_i)}{4\omega_m C V_{dc}} \tag{5.2}$$

Power cells operate in variable loading conditions, where $V_{HB}$, $I_{HB}$, and $\omega_m$ vary in a wide range. In order to maintain DC-bus voltage ripple within permissible range (typically $< 10\%$), especially at lower power cell output angular frequency, large DC-bus capacitance values have to be used.

For the conventional AFE controller, similar analysis holds. As mentioned in Chapter 2, the conventional AFE controller main tasks are DC-bus voltage regulation and reactive power compensation, which are achieved through manipulating the zero frequency power component. Typically, these control tasks are performed on d-q reference frame as illustrated by the controller diagram in Fig. 5.2 Neglecting the switching harmonics instantaneous power components from both the AFE and the H-bridge, pulsating component with double the H-bridge output frequency is taken care by the DC-bus capacitors as shown in Fig. 5.1b and Fig. 5.1c.

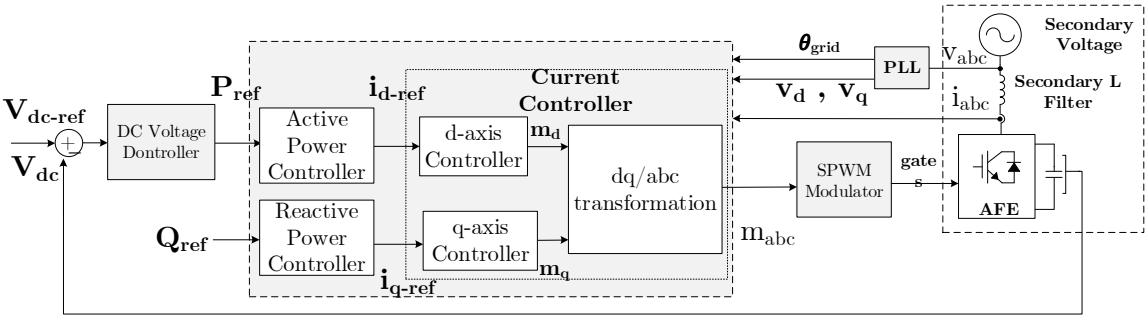



Fig. 5.2 Typical AFE Controller Block Diagram.

DC-bus voltage ripples are accompanied with ripple currents that flows through the capacitors. Double H-bridge output frequency ripple current flowing through the DC-bus capacitor is expressed by Eqn. 5.3 as follows:

$$\Delta i_{cap}(t) = -\frac{V_{HB} I_{HB} \cos(2\omega_m t + \phi_v + \phi_i)}{2V_{dc}} \tag{5.3}$$

As discussed before, Aluminum electrolytic capacitors are widely used in the CHB topology and the degradation of this capacitor technology is accelerated by ripple currents. The next subsection presents an analysis to highlight effect of ripple currents on lifetime of DC-bus Aluminum electrolytic capacitors in CHB topology.

### 5.2.2. Impact of Ripple Currents on Aluminum Electrolytic Capacitors Lifetime

A real case study has been performed on a 650V, 215A DFE power cell [28]. The power cell was operated at its rated conditions. Cell input voltage was 650V, and so the DC-bus voltage was about 900V. H-bridge output current, output frequency, and modulation index were about 215A, 60Hz, and 0.9, respectively. The H-bridge utilized unipolar sinusoidal PWM modulation with switching frequency of 600Hz. In this study, 400V, 7.9A, 1800µF, 85°C CD29L series capacitors from Jianghai were employed [131]. In order to achieve 1200V, ~8600µF DC-bus, a scheme of 3 series groups of 15 parallel capacitors were used as shown in Fig. 5.3.

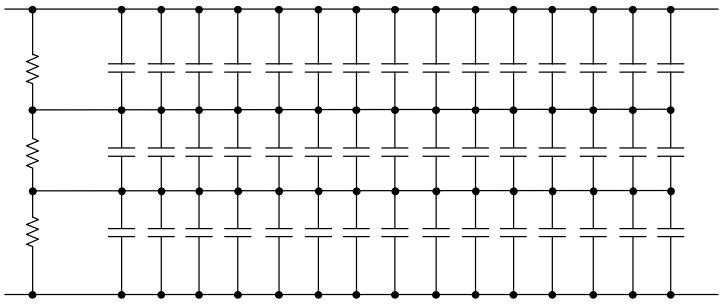


Fig. 5.3 DC-bus Capacitance Connection.

Fig. 5.4 presents the harmonic analysis of the DC-Bus capacitor unit current from the case study. As mentioned before, capacitor RMS current is dominated by the double H-bridge's output frequency component (1st order), and the six-time grid frequency component coming from the DFE (3rd order). In addition, the harmonics analysis shows that current components at double and quadrant of H-bridge's switching frequency are significant. In order to assess lifetime under this loading condition, a similar lifetime estimation process to what has been discussed in Chapter 2 is adopted. Lifetime model and ripple current multipliers suggested by Jianghai for the specified capacitor has be used. Fig. 5.5 presents RMS current components reflected to 120 Hz as required by the model.

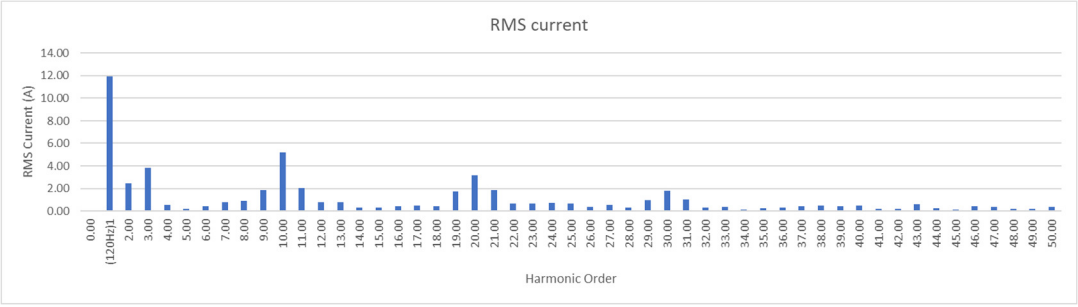



Fig. 5.4 Harmonic Analysis of the DC-Bus Capacitor Unit Current.

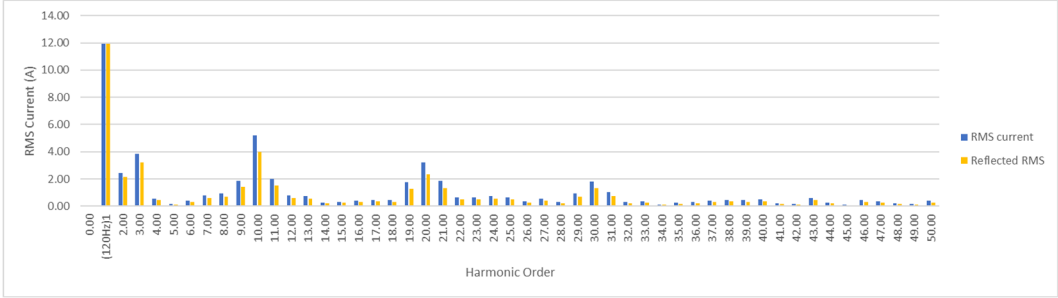



Fig. 5.5 Harmonic Analysis of DC-Bus Capacitor Current Reflected to 120 Hz.

It is clear how the double H-bridge output frequency component dominates the current stresses. Focusing on lifetime consumption due to ripple currents, other factors regarding the DC voltage bias and the ambient temperature are fixed. Accordingly, the estimated lifetime of an aluminum electrolytic capacitor as function of ripple current loading can be expressed as [89]:

$$L_e = L \times K_r \, , K_r = 2^{A \times \frac{\Delta T_o}{10}} , A = 1 - \left( \frac{I}{I_o} \right)^2 \tag{5.4}$$

, where $\Delta T_o$ is set 10℃, and $I_o$ is 7.9A. Applying RMS summation of the reflected current components as shown in Fig. 5.5 results in a capacitor unit current $I$ of about 14A. This results in $A$ of -2.14, and consequently $K_r$ of 0.23. Eliminating the double H-bridge output frequency component in capacitor current results in $A$ of 0.15, and so $K_r$ of 1.01. This leads to a significant improvement in capacitor's expected lifetime of about 4 times.

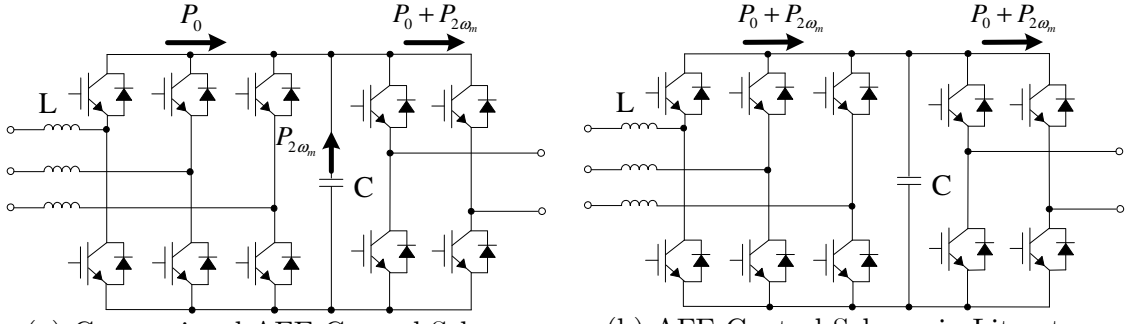
Because of this significant lifetime improvement, several research works have been conducted in the effort of eliminating the double H-bridge output frequency component in capacitor current. The subsequent section presents a review on the ongoing research effort.

## 5.3. Designing a New AFE Control Scheme for Pulsating Power Flow

### 5.3.1. Theory and State-of-the-Art

The double H-bridge output frequency component arises in capacitor current because either the DFE or AFE with conventional control scheme are unable to satisfy the instantaneous power requirement of the H-bridge. The sole solution in the case of DFE is to add more capacitance to the DC-bus or to use longer lifetime grade capacitors, which comes at the expense of increased size and cost.

On the other side, it is possible through adding modification to the AFE controller to divert the double H-bridge output frequency power component from flowing through the capacitor to the AFE. As a result, elimination of the double H-bridge output frequency component in capacitor current is achieved. Fig. 5.6 summarizes this approach, which has been adopted by the majority of the research work in literature [122-130].




(a) Conventional AFE Control Scheme (b) AFE Control Scheme in Literature

Fig. 5.6 Instantaneous Power Flow.

Although this approach provides a promising means to reduce ripple current stresses on the DC-bus capacitors, diverting instantaneous pulsating power component to the AFE then to the grid is not an appealing idea, as the grid connection regulations are not satisfied. However, this is not the case for the CHB topology. The reason is that the phase shifting transformer in the CHB topology is equivalent to a local bus bar to which AFEs are connected equivalently in parallel before interfacing to the grid as shown in Fig. 5.7. There is 120$^{o}$ shift between instantaneous pulsating power flows in AFEs connected to the same secondary winding group, e.g. $Z_{-20}$ secondary windings. Thereby, AFEs exchange their instantaneous pulsating power in between locally to eliminate pulsating power flow at the primary side of the transformer connected to grid.

The simplest modification to the AFE control scheme to allow pulsating power flow is through direct addition of the pulsating power load requirement of the H-bridge into the *d*-axis reference [123, 125]. This is right in principal because the *d*-axis represents the zero frequency power component. Therefore, the component to be added should be with double the H-bridges output frequency. This results in instantaneous power flow through the AFE with required pulsating frequency to match the H-bridge pulsating power.

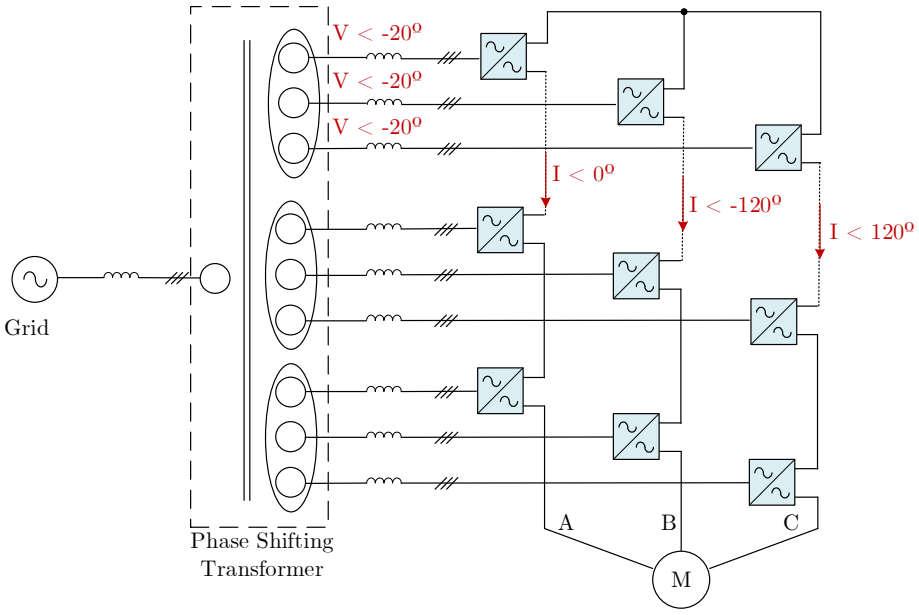



Fig. 5.7 CHB Topology.

Nonetheless, typically, AFE controllers employ proportional-integral (PI) regulators for implementing current control, which achieve poor responses while tracking AC steady state reference signals [123, 125]. Utilizing model predictive current control instead results in high performance tracking [126, 135]. However, for average switching frequencies less than 2000 Hz, AFE current harmonic profiles associated with model predictive current controllers, likewise hysteresis and deadbeat controllers, do not satisfy grid connection requirements [132-135]. Therefore, AFE controllers based on PI current control and SPWM modulation are preferable.

In order to realize better current tracking performance for PI current control, AFE control scheme based on multiple frame of references is to be used [130, 137].

In this control scheme, the conventional task for DC-bus voltage regulation is performed on a frame of reference aligned with one reference frame, while the added task for pulsating power flow is performed on another reference. There is a dedicated current controller for each frame of reference to control the corresponding current component. The outputs of these currents controllers are then transformed to the *abc*-frame, added together, and then send to the SPWM modulator. Fig. 5.8 provides an abstracted block diagram for an AFE control scheme based on this approach, which is further explained in the following subsection.

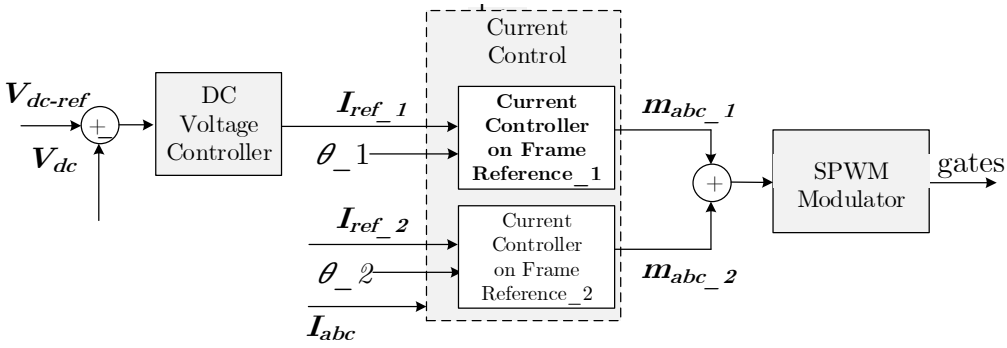



Fig. 5.8 Multi-Frame of Reference AFE Controller Conceptual Block Diagram.

### 5.3.2. Multi-frame of Reference AFE Control Scheme

According to the instantaneous power theory considering the three-phase side of the AFE [138, 139], any current vector $i$ aligned with voltage vector $v_g$ (secondary voltage of the transformer at nominal conditions) gives rise to active instantaneous power and any current vector $i$ aligned with the perpendicular voltage vector $v_{g\perp}$

generates instantaneous reactive power. If the current vector has zero speed compared to voltage vector, the active and reactive instantaneous power flows have only zero frequency component. If there is relative speed between the current vector and the voltage vector, the active and reactive instantaneous power flows have pulsating power components. To set the AFE for pulsating power flow with the required frequency with the zero frequency component, currents are computed as:

$$i^* = \left( \frac{P_0}{V_g^{\,2}} - \frac{P_{2\omega_m}}{V_g^{\,2}} \right) v_g = \left( \frac{V_{HB} I_{HB} \cos(\phi_v - \phi_i)}{2V_g^{\,2}} - \frac{V_{HB} I_{HB} \cos(2\omega_m t + \phi_v + \phi_i)}{2V_g^{\,2}} \right) v_g \tag{5.5}$$

$$\begin{aligned} i^* &= \left( \frac{V_{HB} I_{HB} \cos(\phi_v - \phi_i)}{2V_g} - \frac{V_{HB} I_{HB} \cos(2\omega_m t + \phi_v + \phi_i)}{2V_g} \right) \begin{bmatrix} \cos(\omega_g t + \theta_g) \\ \cos(\omega_g t + \theta_g - 120^o) \\ \cos(\omega_g t + \theta_g + 120^o) \end{bmatrix} \\ &= \frac{V_{HB} I_{HB} \cos(\phi_v - \phi_i)}{2V_g} \begin{bmatrix} \cos(\omega_g t + \theta_g) \\ \cos(\omega_g t + \theta_g - 120^o) \\ \cos(\omega_g t + \theta_g + 120^o) \end{bmatrix} \\ &- \frac{V_{HB} I_{HB}}{4V_g} \begin{bmatrix} \cos(2\omega_m t + \phi_v + \phi_i - \omega_g t - \theta_g) \\ \cos(2\omega_m t + \phi_v + \phi_i - \omega_g t - \theta_g + 120^o) \\ \cos(2\omega_m t + \phi_v + \phi_i - \omega_g t - \theta_g - 120^o) \end{bmatrix} \\ &- \frac{V_{HB} I_{HB}}{4V_g} \begin{bmatrix} \cos(2\omega_m t + \phi_v + \phi_i + \omega_g t + \theta_g) \\ \cos(2\omega_m t + \phi_v + \phi_i + \omega_g t + \theta_g - 120^o) \\ \cos(2\omega_m t + \phi_v + \phi_i + \omega_g t + \theta_g + 120^o) \end{bmatrix} \end{aligned} \tag{5.6}$$

Eqns. 5.5 and 5.6 show that the AFE control scheme should be designed to track three current components. A current component at the grid fundamental frequency $\omega_g$ is responsible for DC-bus voltage regulation through zero component power flow control. In addition, two extra current components at $2\omega_m - \omega_g$ and $2\omega_m + \omega_g$ are responsible for the required pulsating power flow at double the H-bridge output

frequency. Decomposing AFE current measurement into the three components requires complex filtering. Moreover, adding these complex filters to the current controls compromises the performance.

Fortunately, it can be shown that setting the AFE for instantaneous pulsating reactive power flow along with the required instantaneous active power flow cuts down the required extra current components to only one component as illustrated by Eqns. 5.7 to 5.10. This leads to significant complexity reduction of the AFE current decomposition as it is required to decompose the current to only two components at $\omega_g$ and $2\omega_m - \omega_g$ or $\omega_g$ and $2\omega_m + \omega_g$.

$$i^* = \left(\frac{P_0}{\|v_g\|^2} - \frac{P_{2\omega_m}}{\|v_g\|^2}\right) v_g \pm \left(\frac{Q_{2\omega_m}}{\|v_g\|^2}\right) v_g^{\perp} = \left(\frac{V_{HB} I_{HB} \cos(\phi_v - \phi_i)}{2V_g^{\,2}} - \frac{V_{HB} I_{HB} \cos(2\omega_m t + \phi_v + \phi_i)}{2V_g^{\,2}}\right) v_g \pm \left(\frac{V_{HB} I_{HB} \sin(2\omega_m t + \phi_v + \phi_i)}{2V_g^{\,2}}\right) v_g^{\perp} \tag{5.7}$$

$$i^* = \left(\frac{V_{HB} I_{HB} \cos(\phi_v - \phi_i)}{2V_g} - \frac{V_{HB} I_{HB} \cos(2\omega_m t + \phi_v + \phi_i)}{2V_g}\right) \begin{bmatrix} \cos(\omega_g t + \theta_g) \\ \cos(\omega_g t + \theta_g - 120^o) \\ \cos(\omega_g t + \theta_g + 120^o) \end{bmatrix} \pm \left(\frac{V_{HB} I_{HB} \sin(2\omega_m t + \phi_v + \phi_i)}{2V_g}\right) \begin{bmatrix} \sin(\omega_g t + \theta_g) \\ \sin(\omega_g t + \theta_g - 120^o) \\ \sin(\omega_g t + \theta_g + 120^o) \end{bmatrix} \tag{5.8}$$

$$
\begin{aligned}
i^* &= \left( \frac{V_{HB} I_{HB} \cos(\phi_v - \phi_i)}{2V_g} - \frac{V_{HB} I_{HB} \cos(2\omega_m t + \phi_v + \phi_i)}{2V_g} \right) \begin{bmatrix} \cos(\omega_g t + \theta_g) \\ \cos(\omega_g t + \theta_g - 120^o) \\ \cos(\omega_g t + \theta_g + 120^o) \end{bmatrix} \\
&\quad - \left( \frac{V_{HB} I_{HB} \sin(2\omega_m t + \phi_v + \phi_i)}{2V_g} \right) \begin{bmatrix} \sin(\omega_g t + \theta_g) \\ \sin(\omega_g t + \theta_g - 120^o) \\ \sin(\omega_g t + \theta_g + 120^o) \end{bmatrix} \\
&= \frac{V_{HB} I_{HB} \cos(\phi_v - \phi_i)}{2V_g} \begin{bmatrix} \cos(\omega_g t + \theta_g) \\ \cos(\omega_g t + \theta_g - 120^o) \\ \cos(\omega_g t + \theta_g + 120^o) \end{bmatrix} \\
&\quad - \frac{V_{HB} I_{HB}}{4V_g} \begin{bmatrix} \cos(2\omega_m t + \phi_v + \phi_i - \omega_g t - \theta_g) \\ \cos(2\omega_m t + \phi_v + \phi_i - \omega_g t - \theta_g + 120^o) \\ \cos(2\omega_m t + \phi_v + \phi_i - \omega_g t - \theta_g - 120^o) \end{bmatrix} \\
&= \frac{V_{HB} I_{HB} \cos(\phi_v - \phi_i)}{2V_g} \begin{bmatrix} \cos(\omega_g t + \theta_g) \\ \cos(\omega_g t + \theta_g - 120^o) \\ \cos(\omega_g t + \theta_g + 120^o) \end{bmatrix} \\
&\quad - \frac{V_{HB} I_{HB}}{4V_g} \begin{bmatrix} \cos(-2\omega_m t - \phi_v - \phi_i + \omega_g t + \theta_g) \\ \cos(-2\omega_m t - \phi_v - \phi_i + \omega_g t + \theta_g - 120^o) \\ \cos(-2\omega_m t - \phi_v - \phi_i + \omega_g t + \theta_g + 120^o) \end{bmatrix}
\end{aligned}
\tag{5.9}
$$

$$
\begin{aligned}
i^* &= \left( \frac{V_{HB} I_{HB} \cos(\phi_v - \phi_i)}{2V_g} - \frac{V_{HB} I_{HB} \cos(2\omega_m t + \phi_v + \phi_i)}{2V_g} \right) \begin{bmatrix} \cos(\omega_g t + \theta_g) \\ \cos(\omega_g t + \theta_g - 120^o) \\ \cos(\omega_g t + \theta_g + 120^o) \end{bmatrix} \\
&\quad + \left( \frac{V_{HB} I_{HB} \sin(2\omega_m t + \phi_v + \phi_i)}{2V_g} \right) \begin{bmatrix} \sin(\omega_g t + \theta_g) \\ \sin(\omega_g t + \theta_g - 120^o) \\ \sin(\omega_g t + \theta_g + 120^o) \end{bmatrix} \\
&= \frac{V_{HB} I_{HB} \cos(\phi_v - \phi_i)}{2V_g} \begin{bmatrix} \cos(\omega_g t + \theta_g) \\ \cos(\omega_g t + \theta_g - 120^o) \\ \cos(\omega_g t + \theta_g + 120^o) \end{bmatrix} \\
&\quad - \frac{V_{HB} I_{HB}}{4V_g} \begin{bmatrix} \cos(2\omega_m t + \phi_v + \phi_i + \omega_g t + \theta_g) \\ \cos(2\omega_m t + \phi_v + \phi_i + \omega_g t + \theta_g - 120^o) \\ \cos(2\omega_m t + \phi_v + \phi_i + \omega_g t + \theta_g + 120^o) \end{bmatrix}
\end{aligned}
\tag{5.10}
$$

### 5.3.3. Angles Estimation of Reference Frame

The multi-frame of reference AFE control scheme shown in Fig. 5.8 requires angle information. Based on Eqn. 5.9 and 5.10, grid angle information $\omega_g + \theta_g$ is required for reference frame alignment with the grid, which is typically implemented in conventional AFE control schemes. In addition, H-bridge pulsating power angle $2\omega_m + \phi_v + \phi_i$ is required to synthesize the extra current component. Angle information can be calculated at the motor control being responsible for controlling the H-bridges, then transmitted to the AFE controllers as shown in Fig. 5.9.

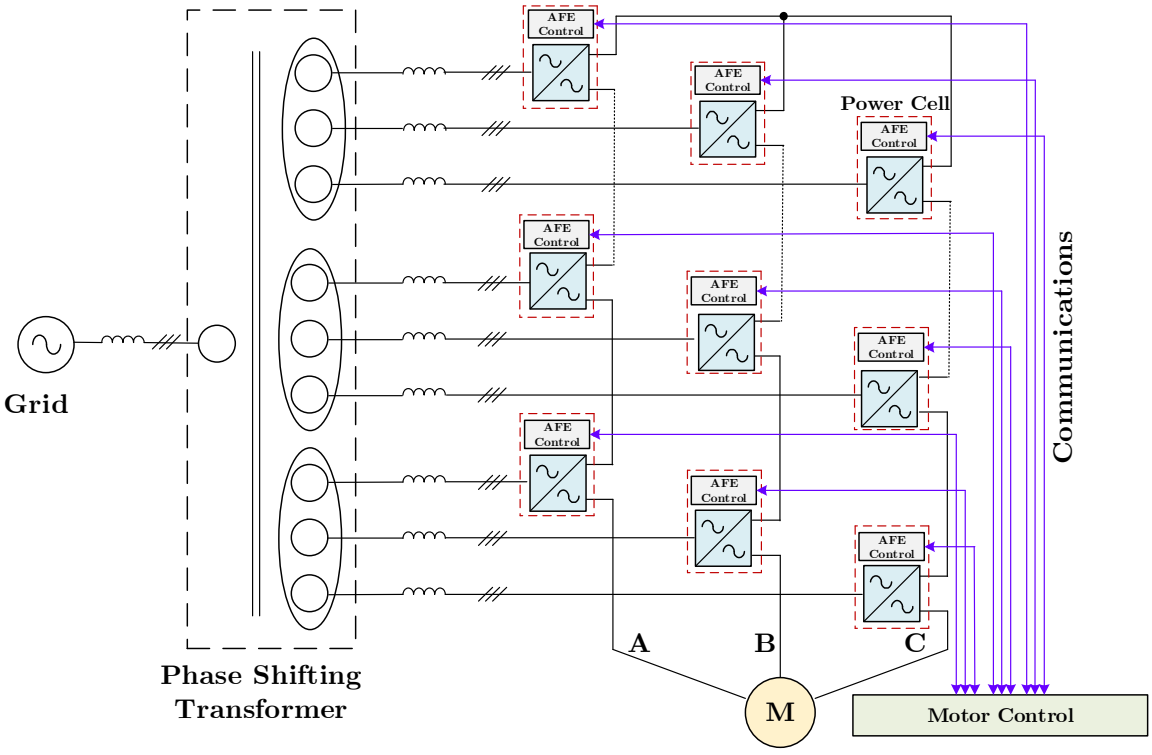



Fig. 5.9 A Conceptual Diagram Showing Communications Lines between AFEs Controllers in Power Cells and the Centralized Motor Control.

One implementation for the pulsating angle estimation is illustrated in Fig. 5.10, in which the pulsating angle information is estimated from a normalized pulsating power waveform transmitted for the communication links from the centralized controller. This waveform is calculated based on measured motor current and motor control output voltage reference. The diagram also shows other signals such as motor frequency $\omega_m$ signal and zero frequency cell power $P_{0\_cell}$ signal, which are used to improve the dynamic performance of the pulsating power flow control of the AFE. Most of the communication burden is attributed to the normalized pulsating power due to its high sampling requirement in comparison to $\omega_m$ and $P_{0\_cell}$ which have slower frequency components.

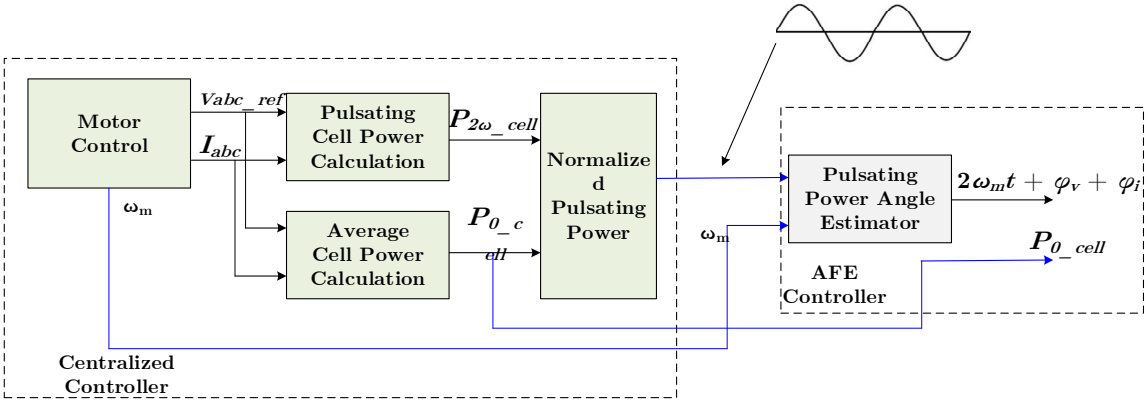



Fig. 5.10 Pulsating Power Angle Estimation from Pulsating Power Information.

In order to reduce that communication burden between the power cells and the centralized motor controller, the possibility of direct estimation of H-bridge pulsating power angle information from DC-bus ripples has been addressed [127-

129]. This approach utilizes the $90^o$ phase shift between H-bridge's pulsating power angle and the DC-bus ripple angle as given in Eqn. 5.1 and Eqn. 5.2.

Based on the previous discussion, the main challenges for designing a novel AFE control scheme capable of controlling the pulsating power flow required by the H-bridge and diverting it away from DC-bus capacitors can be summarized as follows:

1. Designing a high performance current control based on multiple rotating frames and SPWM Modulation.
2. Designing a high performance instantaneous pulsating power estimator.

## 5.4. Proposed AFE Control Scheme

### 5.4.1. AFE Control Scheme Structure

The proposed AFE control scheme is required to perform two control tasks. The first task is to control the flow of zero frequency active and reactive power into or out of the AFE, in order to regulate the DC-bus voltage and prevent high reactive circulating currents between transformer secondaries. The second task is to control the flow of instantaneous pulsating active and reactive power at double H-bridge output frequency, to divert the pulsating power away from the DC-bus capacitors into the AFEs and transformer secondaries or reduce the DC-bus voltage.

As shown in Fig. 5.11, the proposed AFE control scheme is implemented in the power cell. It is a decentralized control scheme that relies on power cell local measurements to perform the control tasks. The exception is for feedforward signals transmitted through the communication links from the motor control, such as motor frequency $\omega_m$ and zero frequency cell power $P_{0\_cell}$ signals, that may be required to improve the dynamic performance of the instantaneous pulsating power flow control of the AFE. In addition, the grid synchronization task performed by the PLL block that can be implemented in the centralized controller, thereby; the voltage magnitude and angle information are to be transmitted to the AFEs through the communication links.

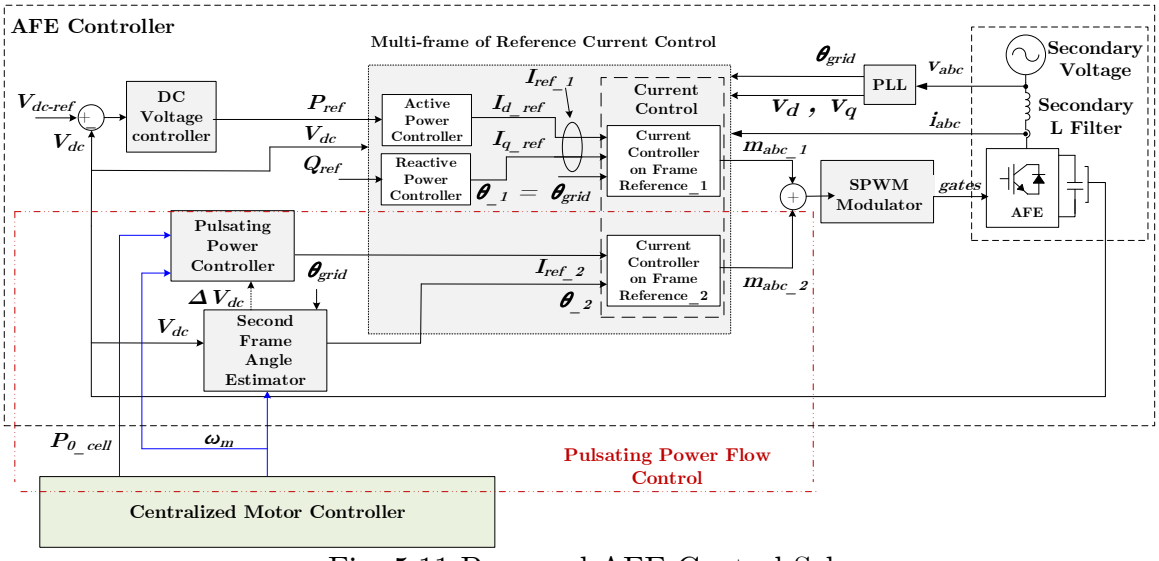



Fig. 5.11 Proposed AFE Control Scheme.

The proposed scheme employs SPWM modulator as shown in Fig. 5.11. This is a key advantage, as SPWM modulators result in AFE input currents with specific harmonic components given the AFE switching frequency. This simplifies the task for designing filters to comply with grid connection harmonic standards. Furthermore, the multi-AFE structure of the AFE-based CHB topology provides more degrees of freedom to vary the harmonic components of the AFEs with respect to each other. This variation is designed in a way to reduce the filtering requirements while still complying with the grid connection requirements at the primary of the transformer. For example, it permits the usage of only inductors as filters at the secondaries and possibly at the primary of the transformer.

In order to achieve the DC-bus voltage regulation task, the control scheme employs typical PID-based DC-bus voltage regulator as shown in Fig. 5.11. The DC-bus regulator provides zero frequency active power reference to the multi-frame of reference current control. In addition, based on the required power factor at the primary side of the transformer or other drive system requirements, the zero frequency reactive power reference is provided to the multi-frames of reference current control.

DC-bus capacitors ripple reduction is performed by a proposed instantaneous pulsating power flow control task marked by the red dotted line in

Fig. 5.11. First, this task employs a proposed angle estimator to extract the instantaneous pulsating power angle information from the DC-bus voltage ripple. This angle information $\theta_{\_2}$ and the grid angle, $\theta_{grid} = \omega_g t + \theta_g$, estimated by the PLL are required by the multi-frame of reference current control to achieve instantaneous pulsating power flow control task. In order to improve the dynamic responsiveness of the instantaneous pulsating power angle estimator, a motor frequency $\omega_m$ feedforward signal is employed. Second, a proposed instantaneous pulsating power controller is used to determine the required instantaneous pulsating active and reactive power to be allowed to flow in the AFE at different motor loading conditions. It produces a current reference to the multi-frame of reference current control to achieve instantaneous pulsating power flow control task based on motor frequency $\omega_m$, zero frequency cell power $P_{0\_cell}$, and DC-bus voltage ripple $\Delta V_{dc}$ signals.

At the core of the proposed AFE control scheme presented in Fig. 5.11 lies the proposed multi-frame of reference current control. It consists of two current controllers formulated at two different frames of references. The first current controller is aligned to the grid voltage vector generated from the PLL and it is responsible for tracking current references provided by zero frequency power and reactive power controller. The second current controller is aligned to a reference

frame generated by the second frame angle estimator and it is responsible for tracking current references provided by the instantaneous pulsating power controller. Each current controller produces modulation index in *abc*-frame, which are added together and provided to the SPWM modulator.

The details of the multi-frame of reference current control, and instantaneous pulsating power controller and angle estimation are presented in subsequent subsections

### 5.4.2. Multi-Frame of Reference Current Control

Fig. 5.12 illustrates the detailed structure of the proposed multi-frame of reference current controller. The controller is composed of two sets of *d*-*q* axes PI-based current regulators with their associated frame-of-reference transformations aligned to two different frames. Each set represents a current controller block as shown in Fig. 5.11. In addition, it includes a current components decomposition block residing at the core of multi-frame of reference current control scheme.

The current controller at the frame 1 is responsible for the zero frequency active and reactive power flow through the AFE. It receives a current reference in the form of a *d*-axis and *q*-axis reference current components representing reference active and reactive powers determined by the decoupled active and reactive power controllers blocks shown in Fig. 5.11, respectively.

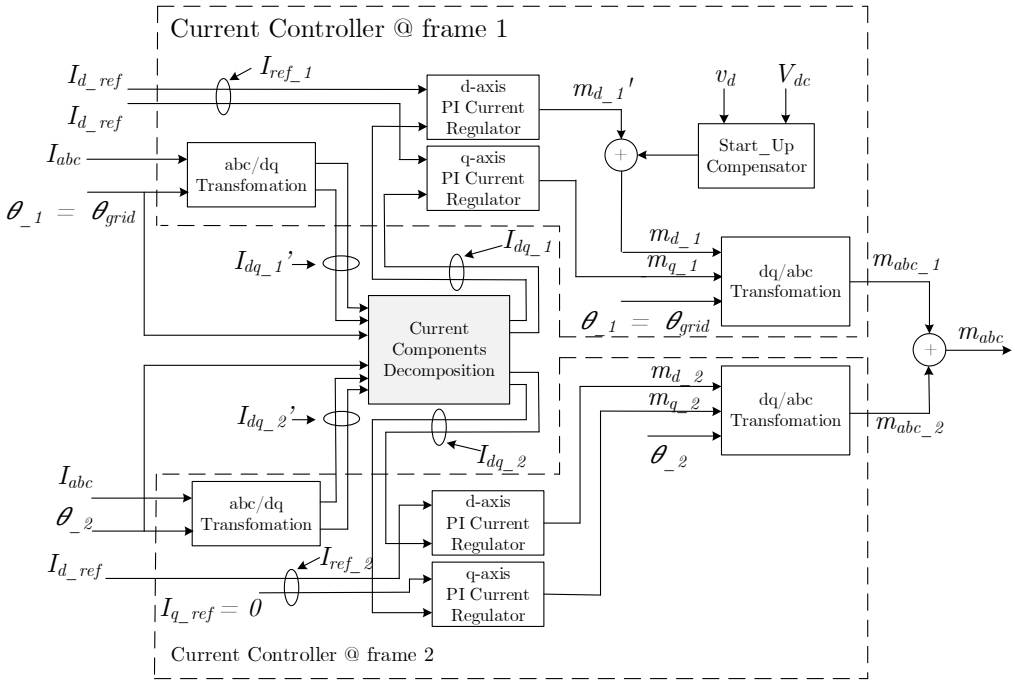



Fig. 5.12 Proposed Multi-Frame of Reference Current Control.

This active and reactive power decoupling is due to the alignment of frame 1 to the grid voltage vector and thus zeroing $q$-axis component of grid voltage vector $v_q$. The two PI current regulators are used to force the $d$-axis and $q$-axis current components of the AFE on frame 1 to track the reference current components. In order to improve the transient and the startup responses against grid voltage, a feedforward block is used to modify the $d$-axis modulation index component based on DC-bus voltage $V_{dc}$ and $d$-axis grid voltage component $v_d$ signals. The resultant $d$ and $q$-axes modulation indices in frame 1 are transformed to the $abc$-frame using grid angle to form the first part of the final modulation to be provided to the SPWM modulator.

The current controller at the frame 2 is responsible for the instantaneous pulsating active and reactive power flow through the AFE. It receives a current reference in the form of a *d*-axis and *q*-axis reference current components representing reference instantaneous pulsating active and reactive powers determined by the pulsating power controller block shown in Fig. 5.11, respectively. As illustrated by Eqns. 5.9 and 5.10, allowing instantaneous pulsating reactive power in conjunction with instantaneous pulsating active power flow reduces the required pulsating current components to be controlled by AFE to one current component at either with angle $-2\omega_m - \phi_v - \phi_i + \theta_{grid}$ or $2\omega_m + \phi_v + \phi_i + \theta_{grid}$. Therefore, by aligning the current control in frame 2 to $-2\omega_m - \phi_v - \phi_i + \theta_{grid}$ or $2\omega_m + \phi_v + \phi_i + \theta_{grid}$, pulsating current in *abc*-frame results in DC value $d$ and $q$ current components in frame 2. Furthermore, this alignment implies that the control of both the reactive and active power flow is performed by setting the *d*-axis current references based on the pulsating power controller block while putting *q*-axis current references to zero as illustrated in Fig. 5.11 and 5.12. The two PI current regulators are used to force the *d*-axis and *q*-axis current components of the AFE on frame 2 to track the reference current components. The resultant $d$ and *q*-axes modulation indices in frame 2 are transformed to the *abc*-frame using the second frame of reference angle

to form the second part of the final modulation to be provided to the SPWM modulator.

Fig. 5.13 shows the AFE input side phasor diagram under the proposed multi-frame of reference current control. The main assumption is the effective decomposition of the AFE input current into the two current components $I_{\_1}$ and $I_{\_2}$. However, the coupling between the frequency of the current component $I_{\_2}$ and motor frequency highly complicates the current components decomposition. Table. 5.1 provides an example for the two current components calculated in different frames at two motor frequencies, where negative frequency values represent negative sequence. On frame 1, current component 2 has to be filtered out without affecting the frequency response of current component 1; while on frame 2, current component 2 has to be filtered out without influencing the frequency response of current component 1. In this case, it is obvious that simple low pass filters does not provide the sufficient current components decomposition. More complex filter structures such as variable notch filters can be employed. These frequency adaptive filters provide efficient current components decomposition. Nonetheless, these filter structures have undesirable dynamic responses, which does not satisfy the current controller dynamic performance requirements for motor drive applications.

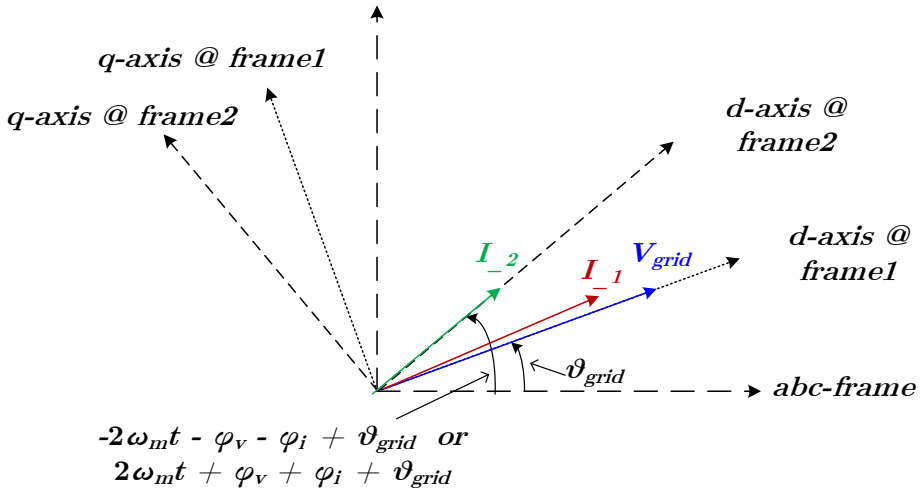



Fig. 5.13 AFE Operation Phasor Diagram under the Proposed Control Scheme.

Table. 5.1. Example for Current Components in Different Frames at Different Motor Frequencies.

| **Motor Frequency = 60 Hz** | ***abc* Frame** | **Frame 1** | **Frame 2 @ $-2\omega_m t - \varphi_v - \varphi_i + \vartheta_{grid}$** |
|---|---|---|---|
| Current Component 1 | 60 Hz | 0 Hz | 120 Hz |
| Current Component 2 | -60 Hz | -120 Hz | 0 Hz |

| **Motor Frequency = 20 Hz** | ***abc* Frame** | **Frame 1** | **Frame 2 @ $-2\omega_m t - \varphi_v - \varphi_i + \vartheta_{grid}$** |
|---|---|---|---|
| Current Component 1 | 60 Hz | 0 Hz | 40 Hz |
| Current Component 2 | 20 Hz | -40 Hz | 0 Hz |

In order to address this challenge, a current components decomposition network is proposed as presented in Fig. 5.12. The goal of this network is to receive the output of transformation of AFE input current to frame 1 as $I_{dq\_1}$' and frame 2 as $I_{dq\_2}$'. As shown in the example presented in Table 5.1, the two components of the AFE input current reflect on transformation to frame 1 and 2 to appear in

$I_{dq\_1}$' and $I_{dq\_2}$'. The network filters out the extra current component in each frame as illustrated by the example in Table 5.2 and outputs the effectively decomposed current components $I_{dq\_1}$ and $I_{dq\_2}$ to their respective current regulators.

Table. 5.2 Example Illustrating the Filtering Effect of the Proposed Decomposition Network.

| **Motor Frequency = 20 Hz** | ***abc* Frame** | **Frame 1** $I_{dq\_1}$' | **Frame 2** $I_{dq\_2}$' | **Frame 1** $I_{dq\_1}$ | **Frame 2** $I_{dq\_2}$ |
|---|---|---|---|---|---|
| Current Component 1 | 60 Hz | 0 Hz | 40 Hz | 0 Hz | - |
| Current Component 2 | 20 Hz | -40 Hz | 0 Hz | - | 0 Hz |

Fig. 5.14 presents the detailed structure of the proposed current components decomposition network. The core concept behind this network is to use the filtered output in one frame to cancel the extra current component in the other frame through the transformation of this filtered output to the other frame and adding the result of the transformation to the input of the other frame. Fig. 5.15 shows internal working of decomposition network under the example given in Table. 5.2.

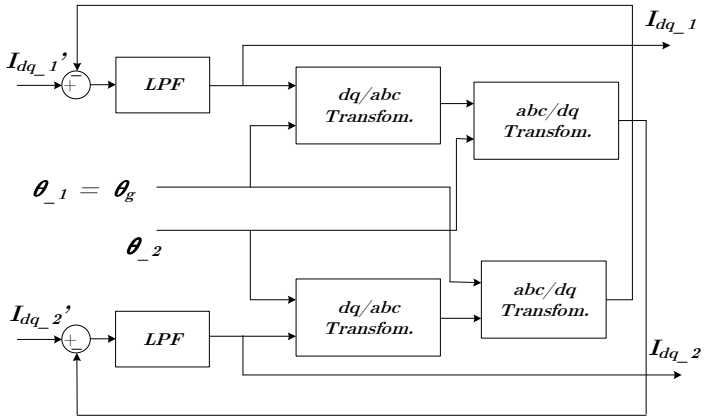



Fig. 5.14 Proposed Current Component Decomposition Network.

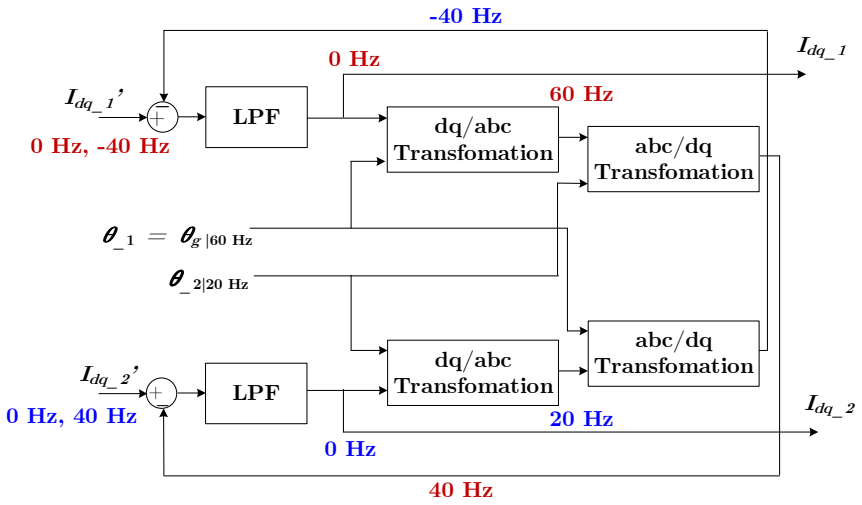



Fig. 5.15 Illustration of the Internal Working of the Decomposition Network.

### 5.4.3. High Performance Instantaneous Pulsating Power Estimator

It is clear that the performance of the instantaneous pulsating power flow control task in particular and the performance of the whole AFE control scheme depend on the accurate estimation of instantaneous pulsating power angle and accordingly the determination of the second frame of reference angle. In addition, the determination of amount and the frequency of pulsating power to flow through the AFE given motor drive loading condition has significant implications on AFE control scheme performance on one hand, and drive system reliability on the other hand. In order to tackle these challenges beside other challenges such as reducing the communication burden between AFE local controllers and the centralized controller, a decentralized pulsating power estimator is proposed as presented in

Fig. 5.16. The proposed estimator reduces the communication requirements by relying only on low frequency feedforward signals transmitted from the centralized controller such as motor frequency $\omega_m$ signal and zero frequency cell power $P_{0\_cell}$ signal. The proposed estimator includes pulsating power angle estimator, control logic for determining second frame angle, and pulsating power controller for determining the current reference for current controller on frame 2.

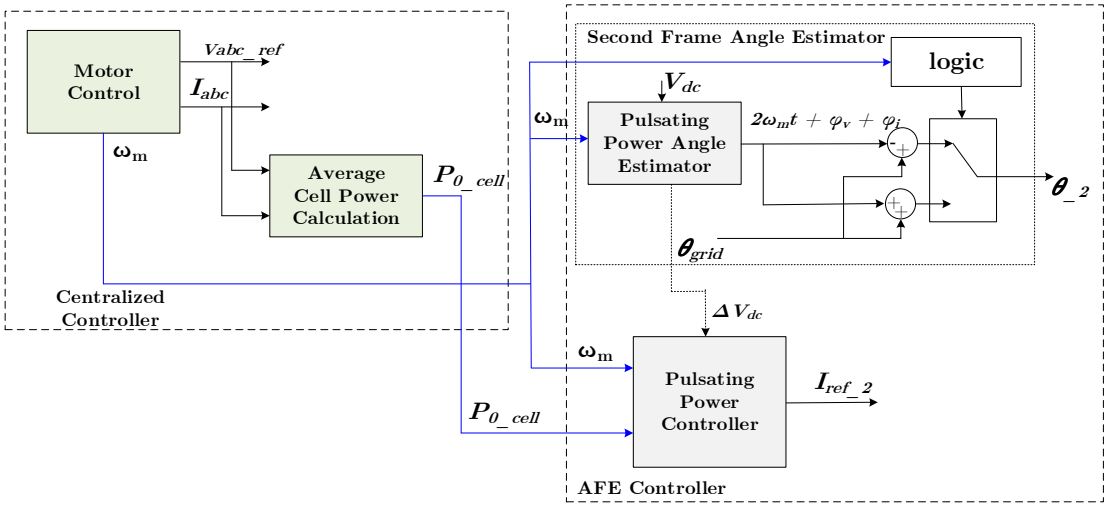



Fig. 5.16 Proposed Decentralized Pulsating Power Estimator.

Fig. 5.17 presents the detailed structure of the decentralized pulsating power angle estimator based on power cell DC-bus voltage measurement. The proposed structure represents a variable frequency PLL structure. An adaptive gain is utilized to improve the PLL locking capability for different DC-bus voltage ripple frequencies and magnitudes under different motor drive operating conditions. The gain is function of motor frequency and optionally the DC-bus voltage ripple

magnitude. Moreover, motor frequency is used as feedforward to assist the dynamic performance of the PID controller. In order to prevent the average value of DC-bus voltage and high order switching harmonics from getting into the PLL feedback loop, a variable cycle moving average block is used. The estimated pulsating power angle $2\omega_m t+\varphi_v+\varphi_i$ is then used in the determination of second frame angle $\theta_{\_2}$.

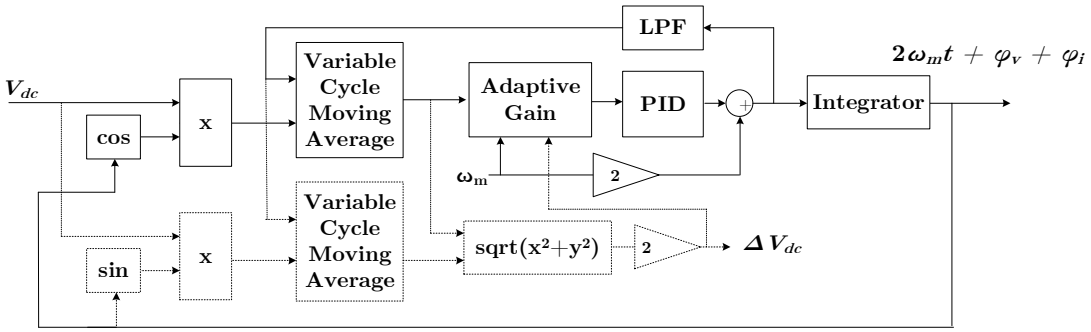



Fig. 5.17 Proposed Decentralized Pulsating Power Angle Estimator.

A control logic based on motor frequency $\omega_m$ signal is employed to compute second frame angle $\theta_{\_2}$ out of pulsating power angle $2\omega_m t+\varphi_v+\varphi_i$ and grid angle $\theta_{grid}$ . Based on Eqn. 5.9 and 5.10, given motor frequency $\omega_m$ and grid frequency $\omega_g$, the input AFE pulsating current frequency is set to $\omega_g \pm 2\omega_m$ in order to allow pulsating active and reactive power flow. Table 5.3 presents the two current components frequencies under different motor frequencies given the input AFE pulsating current frequency is set to $\omega_g \pm 2\omega_m$. The table reveals important points to consider, where negative frequency values represent negative sequence.

Table. 5.3 The Two Current Components Frequencies under Different Motor Frequencies.

| **Motor Frequency** | **Ripple power Frequency** | $\omega_g - 2\omega_m$ | | $\omega_g + 2\omega_m$ | |
|---|---|---|---|---|---|
| | | **1st Current in *abc* Frame** | **2nd Current in *abc* Frame** | **1st Current in *abc* Frame** | **2nd Current in *abc* Frame** |
| 60 Hz | 120 Hz | 60 Hz | - 60 Hz | 60 Hz | 180 Hz |
| 50 Hz | 100 Hz | 60 Hz | - 40 Hz | 60 Hz | 160 Hz |
| 40 Hz | 80 Hz | 60 Hz | - 20 Hz | 60 Hz | 140 Hz |
| 35 Hz | 70 Hz | 60 Hz | - 10 Hz | 60 Hz | 130 Hz |
| 30 Hz | 60 Hz | 60 Hz | 0 Hz | 60 Hz | 120 Hz |
| 25 Hz | 50 Hz | 60 Hz | 10 Hz | 60 Hz | 110 Hz |
| 20 Hz | 40 Hz | 60 Hz | 20 Hz | 60 Hz | 100 Hz |
| 10 Hz | 20 Hz | 60 Hz | 40 Hz | 60 Hz | 80 Hz |

First, under some range of motor frequency, if the input AFE pulsating current frequency is set to $\omega_g - 2\omega_m$, this causes low frequency current components that have undesirable magnetic and thermal effects on transformer. Second, under some range of motor frequency, if the input AFE pulsating current frequency is set to $\omega_g + 2\omega_m$, this gives rise to high frequency current components that require higher PWM frequency and controller bandwidth. As a result, to address these issues one possible implementation of control logic can be designed as shown in Table 5.4.

Table. 5.4 A Possible Control Logic for $\theta_{\_2}$ Calculation.

| **Motor Frequency** | $\theta_{\_2}$ |
|---|---|
| $>$ 35 Hz | $-2\omega_m t - \varphi_v - \varphi_i + \vartheta_{grid}$ |
| $<$ 35 Hz | $2\omega_m t + \varphi_v + \varphi_i + \vartheta_{grid}$ |

How much pulsating active and reactive power to flow through the AFE in order to reduce the pulsating power through the DC-bus capacitor is determined by setting the current reference $I_{ref\_2}$ for current controller on frame 2. The determination of $I_{ref\_2}$ is performed by the pulsating power controller as shown in Fig. 5.16. The detailed structure of the proposed pulsating power controller is presented in Fig. 5.18. It consists of a feedforward component based on motor frequency $\omega_m$ signal and zero frequency cell power $P_{0\_cell}$ signal, and an optional feedback component based on estimated DC-bus voltage ripple magnitude. Extra attention should be paid while designing the feedback component because it highly possible to give rise to controller instability. One aspect is that DC-bus voltage ripple reference $\Delta V_{dc\_ref}$ cannot be zeroed. As the pulsating power angle estimator relies on DC-bus voltage ripple to estimate the pulsating power angle. Otherwise, the pulsating angle estimation is inaccurate, which causes controller instabilities. Another aspect is that the calculated $I_{ref\_2}$ should be limited because there are points beyond which increasing $I_{ref\_2}$ leads to increase in DC-bus voltage ripple. If the feedback component reaches these points, control instabilities occur. Considering these control stability challenges, the proposed controller suggests relying only on a feedforward component as shown in Fig. 5.18 to determine $I_{ref\_2}$

based on motor frequency $\omega_m$ and zero frequency cell power $P_{0\_cell}$ signals transmitted from the centralized control and the d-axes component of grid voltage $v_d$ representing grid voltage magnitude.

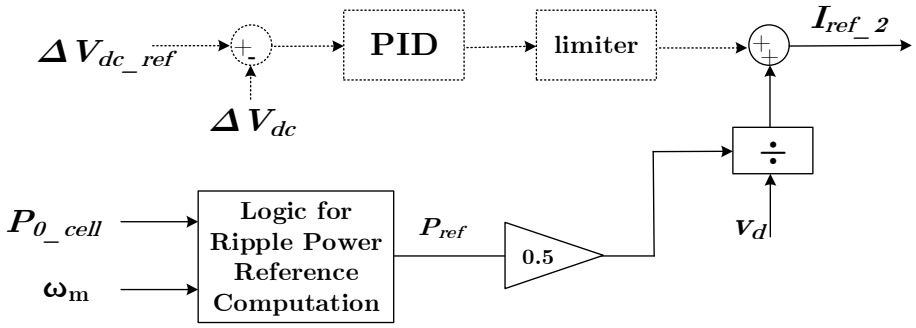



Fig. 5.18 Proposed Pulsating Power Controller.

Three aspects should be considered while designing the logic for generating the reference pulsating power $P_{ref}$. First, a near zero motor frequency, controlling the AFE to allow pulsating power flow may cause control instabilities. Therefore, $P_{ref}$ should be set to zero at near zero motor frequencies. Second, adding extra current component in the AFE input current results in higher current peaks and increased losses in the AFE semiconductor devices and the transformer compared to the case of conventional AFE control. In addition, these extra stresses may lead to long-term reliability issues in AFE semiconductor devices and the transformer. If all the pulsating power is diverted from DC-bus capacitors to the AFEs and the transformer, significant modifications should be made in AFE power cell including

semiconductor devices selection, heatsinks and cooling design in addition to changes in transformer designs. There should be a compromise between the long-term reliability gains in the DC-bus capacitors versus the increased costs and possible long-term reliability issues that may arise in the other parts of the drive. Accordingly, $P_{ref}$ may be computed so that a portion of the pulsating power based on a value $w$ is diverted from the DC-bus capacitors to the AFEs and the transformer as shown in Fig. 5.19.

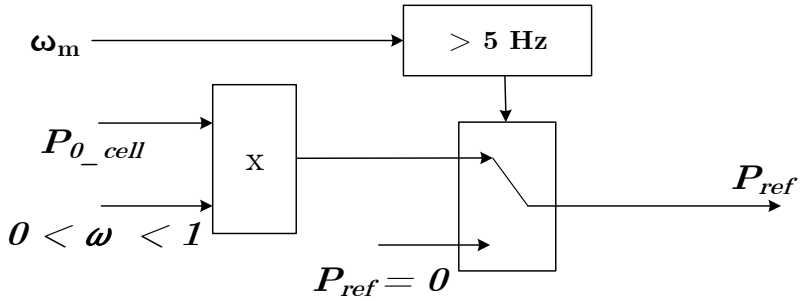



Fig. 5.19 A Simple Implementation for Pulsating Power Reference Computation Logic.

## 5.5. Simulation Studies and Experimental Validation

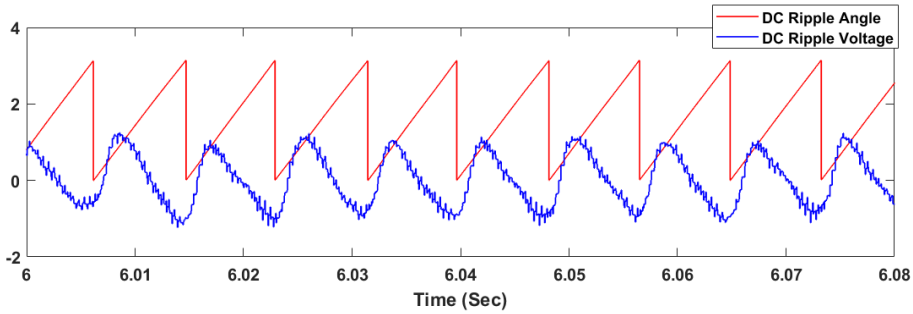
In order to validate effectiveness the proposed AFE control scheme in achieving the stated objectives, simulation and experimental studies have been performed on a 9-cell regenerative CHB converter with parameters given in Table 5.5. System model have been built in MATLAB/Simulink.

Table 5.5 CHB Converter Main Parameters.

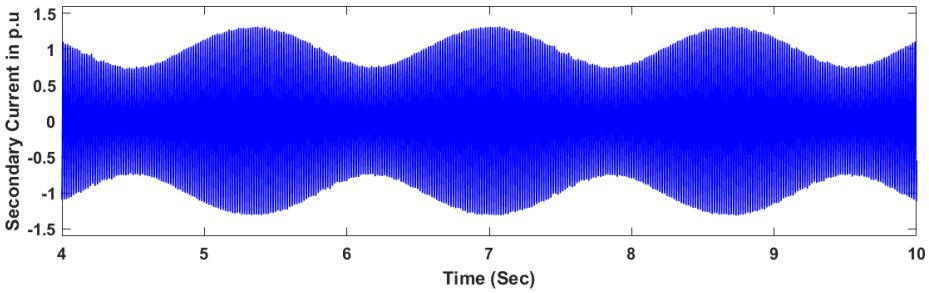
| Converter parameter | Simulation Value | Experimental Value |
|---|---|---|
| **Cell DC-bus voltage (V)** | 1100 | 170 |
| **Transformer Secondary Side Voltage (V)** | 650 | 80 |
| **Equivalent Secondary Inductance (mH)** | 4 | 4 |
| **DC-Bus Capacitance (µF)** | 8600 | 2300 |
| **Base Current (A)** | 200 | - |

### 5.5.1. Simulation Studies

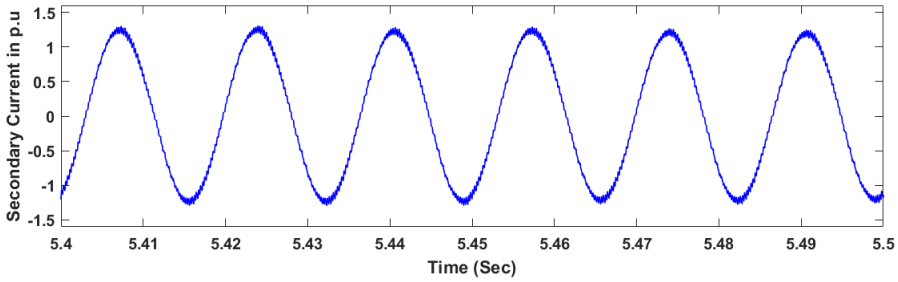
Simulation results for H-bridge output frequency at 60 Hz and 40 Hz are presented in Fig. 5.20 and 5.21, respectively. According to Tables 5.3 and 5.4, at 60 Hz H-bridge side frequency, the AFE control scheme is required to control two current components at 60 Hz and -60 Hz in order to divert the 120 Hz pulsating power away from the DC-bus capacitor. The phase angle of the 60 Hz component is calculated from the AFE input voltage through a PLL. In order to calculate the phase angle of -60 Hz current component, the phase angle of the DC-bus voltage ripple is estimated through the proposed estimator given in Fig. 5.17. Then the estimated phase angle is subtracted from the grid angle to get the phase angle of -60 Hz current component as given in Table 5.4. Fig. 5.20a shows the estimated DC-bus voltage ripple phase angle.



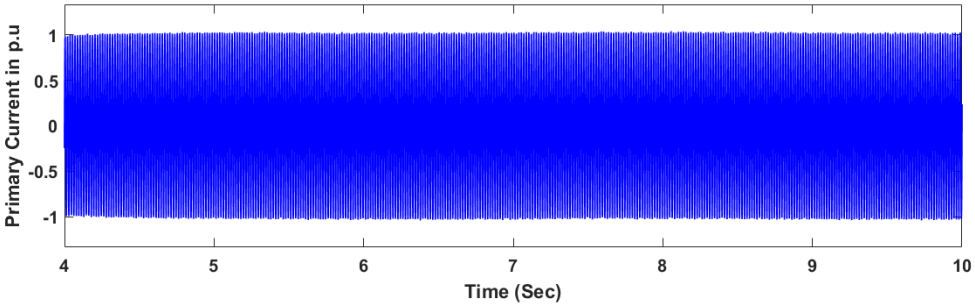

(a) DC-bus Voltage Ripple Phase Angle



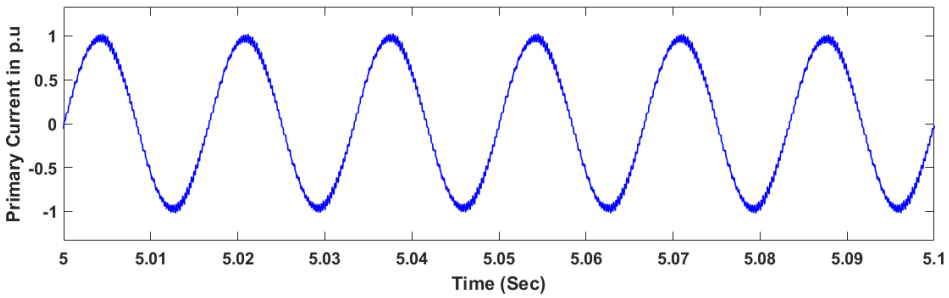

(b) Secondary Current




(c) Zooming at the Peak Period of Secondary Current




(d) Primary Current



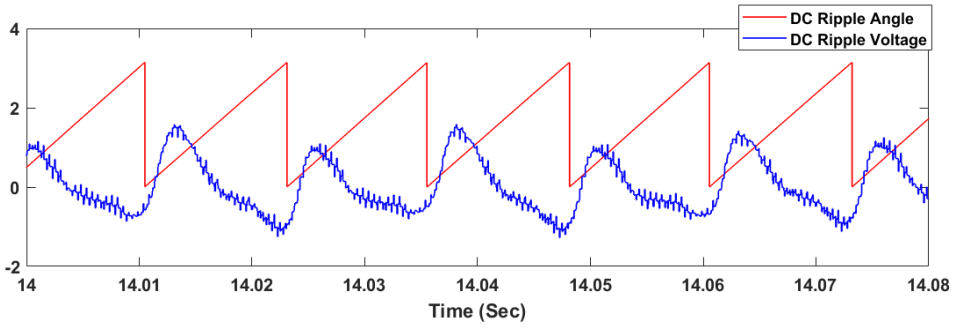

(e) Zoomed Primary Current

Fig. 5.20 Simulation Results for H-bridge Output Frequency at 60 Hz.

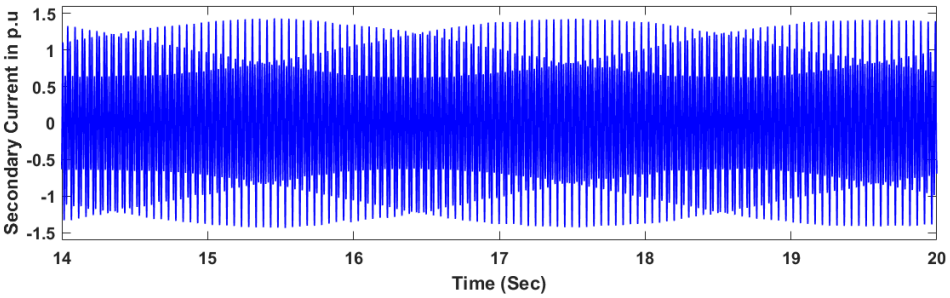
Fig. 5.20b and 5.20c show the AFE input current (transformer secondary current). A current profile of peaks and valleys resulted from the superposition of the current components. The additional current peaks and r.m.s. add stresses on the transformer. Therefore, a tradeoff should be made between how much pulsating power to be kept flowing in the DC-bus capacitor and how much to be diverted away to the secondary of the transformer. Fig. 5.20d and Fig. 5.20e present the primary current waveform. The -60 Hz current components at the secondaries cancel out at the transformer primary.

Again, based on Tables 5.3 and 5.4, at 40 Hz H-bridge side frequency, the AFE control scheme is required to control two current components at 60 Hz and -20 Hz in order to divert the 80 Hz pulsating power away from the DC-bus capacitor. In order to calculate the phase angle of -20 Hz current component, the phase angle of the DC-bus voltage ripple is estimated through the proposed estimator. Then

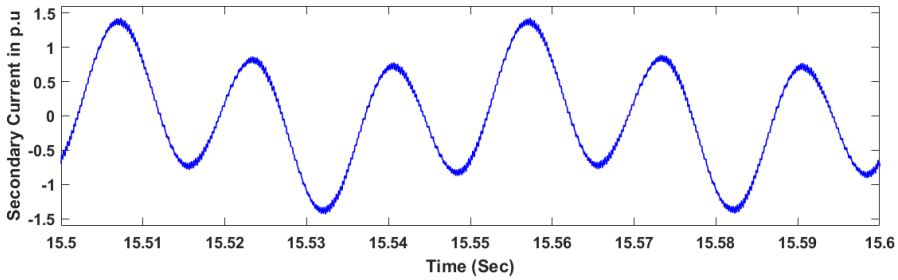
the estimated phase angle is subtracted from the grid angle to get the phase angle of -20 Hz current component as given in Table 5.4. Fig. 5.21a shows the estimated DC-bus voltage ripple phase angle.



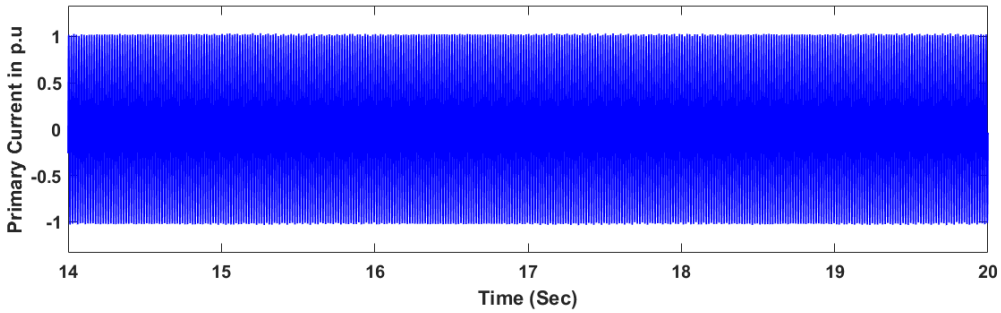

(a) DC-bus Voltage Ripple Phase Angle



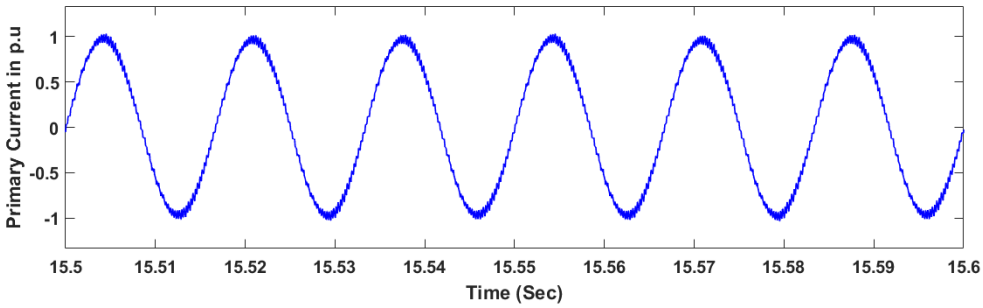

(b) Secondary Current




(c) Zooming at the Peak Period of Secondary Current




(d) Primary Current

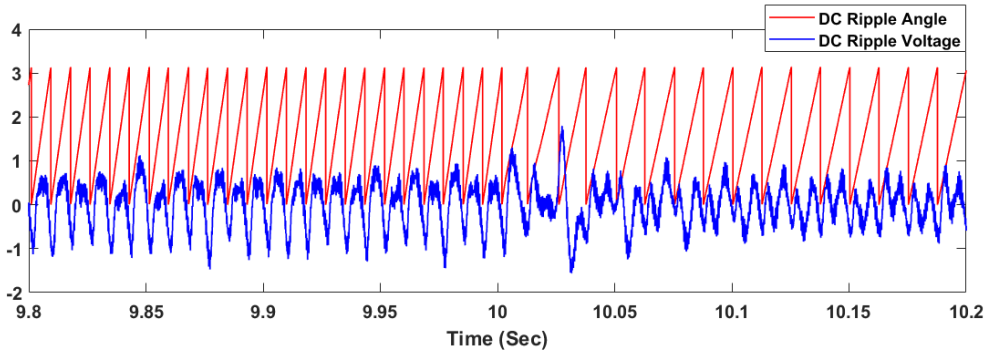



(e) Zoomed Primary Current

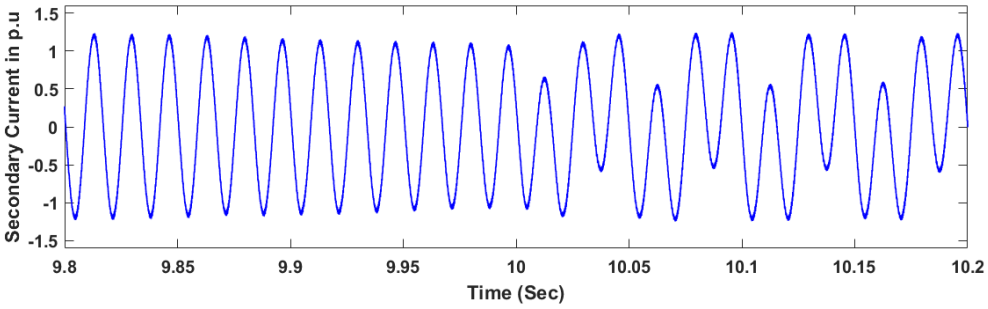
Fig. 5.21 Simulation results for H-Bridge Output Frequency at 40 Hz.

Fig. 5.21b and 5.21c show the AFE input current (transformer secondary current). Similar to the 60 Hz H-bridge output frequency case, the current waveform shows additional currents peaks, which impose more stresses on the transformer. Therefore, a tradeoff should be made between how much pulsating power to be kept flowing in the DC-bus capacitor and how much to be diverted away to the secondary of the transformer. Fig. 5.21d and 5.21e present the primary current waveform. It is clear that -20 Hz current components at the secondaries cancel out and do not show at the transformer primary.

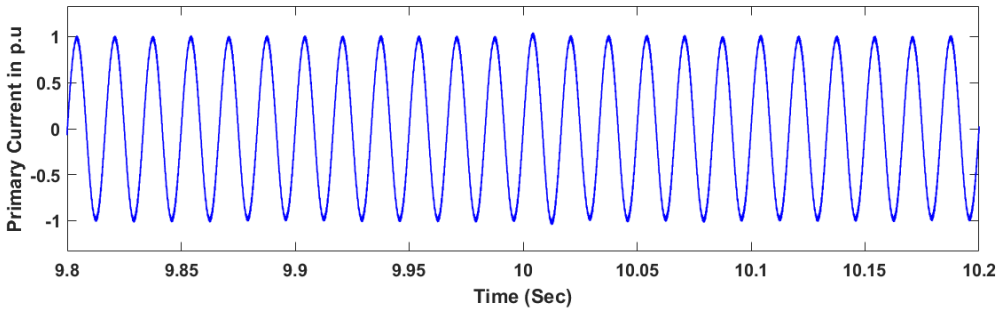
In order to validate the fast dynamic performance of the proposed AFE control system including the pulsating power angle estimator and multi-frame current control, simulation for step response in H-bridge output frequency was conducted. Results for a step change in H-bridge output frequency from 60 Hz to 40 Hz are illustrated in Fig. 5.22. Fig. 5.22a shows pulsating angle tracking given the step change in H-bridge output frequency from 60 Hz to 40 Hz. Fig. 5.22b shows secondary current during this step change. There are almost no overshoots in current.




(a) DC-bus Voltage Ripple Angle and Voltage




(b) Secondary Current



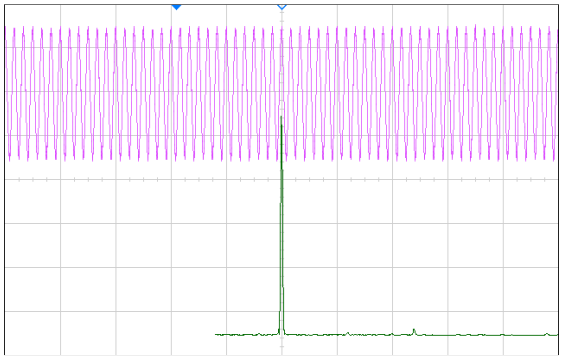

(c) Primary Current

Fig. 5.22 Waveforms during the Step Change in Output Frequency.

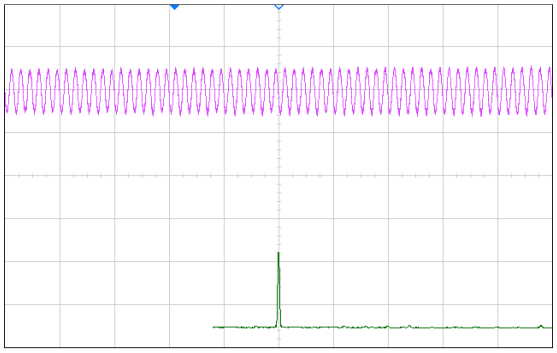
Fig. 5.22c shows secondary current during this step change. There is almost no change in the primary current during the step frequency change, which advocates for the near optimal decoupling of the two current components within the current control.

### 5.5.2. Experimental Validation

Experimental studies have been conducted based on the given system parameters to validate the ability of the current controller to decouple and control the two required current components across a wide H-bridge output frequency range. Fig 5.23 to 5.29 show the secondary current waveforms and FFT for H-bridges of output frequency from 60 Hz to 5 Hz, respectively. In this study, the proposed current controller follows the pulsating power angle calculation scheme given in Table 5.4. Fig. 5.23 shows one current component at 60 Hz. In fact, they are two current components: one at 60 Hz and the other at -60 Hz.



(a) Peak of the Current Profile
(10A / div)(100ms / div)
(60Hz FFT Center)



(b) Valley of the Current Profile
(10A / div)(100ms / div)
(60Hz FFT Center)

Fig. 5.23 Secondary Current at 60 Hz H-bridge Output Frequency.

At 50 Hz output frequency, Fig. 5.24 shows two current components: 60 Hz and -40 Hz. At 40 Hz output, Fig. 5.25 shows current components: 60 Hz and -20 Hz. At 30 Hz output, Fig. 5.26 shows current components: 60 Hz and 120 Hz. At 20 Hz output, Fig. 5.27 shows current components: 60 Hz and 100 Hz. At 10 Hz output, Fig. 5.28 shows current components: 60 Hz and 80 Hz. At 5 Hz output, Fig. 5.29 shows current components: 60 Hz and 70 Hz.

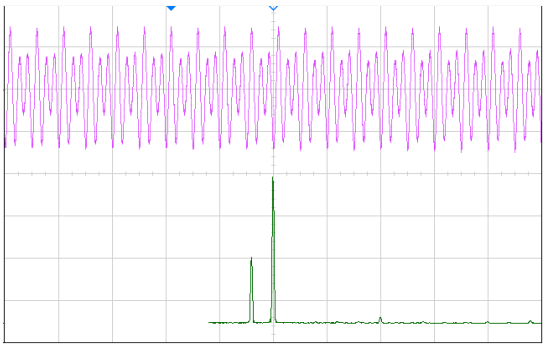


Fig. 5.24 Secondary Current at 50 Hz
H-bridge Output Frequency
(10A / div)(100ms / div)
(60Hz FFT Center)

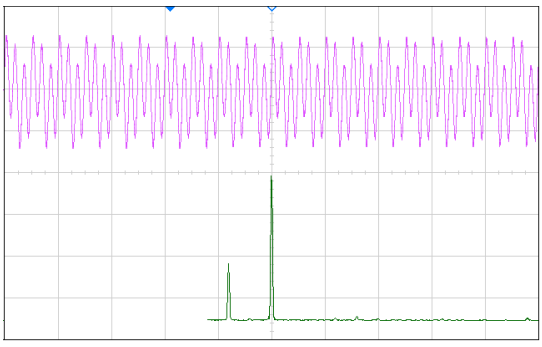


Fig. 5.25 Secondary Current at 40 Hz
H-bridge Output Frequency
(10A / div)(100ms / div)
(60Hz FFT Center)

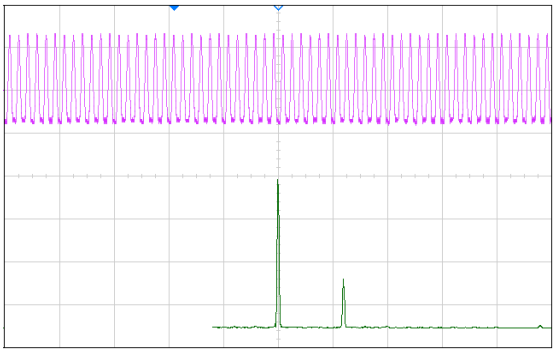


Fig. 5.26 Secondary Current at 30 Hz H-bridge Output Frequency (10A / div)(100ms / div) (60Hz FFT Center)

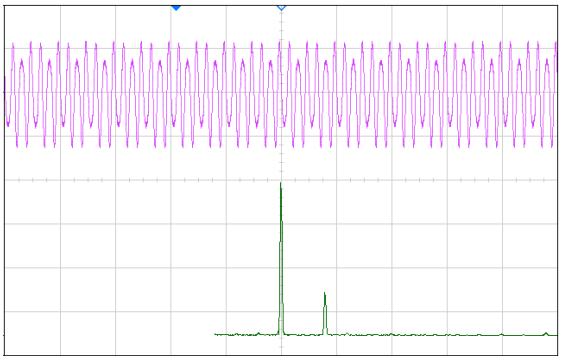


Fig. 5.27 Secondary Current at 30 Hz H-bridge Output Frequency (10A / div)(100ms / div) (60Hz FFT Center)

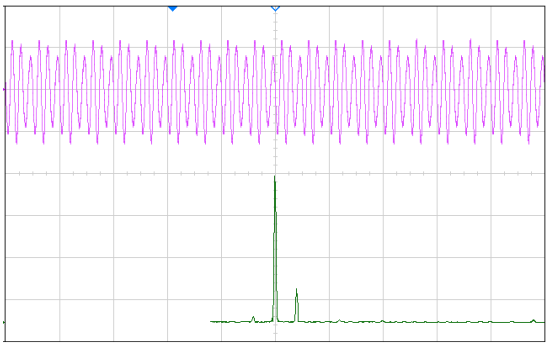


Fig. 5.28 Secondary Current at 10 Hz H-bridge Output Frequency (10A / div)(100ms / div) (60Hz FFT Center)

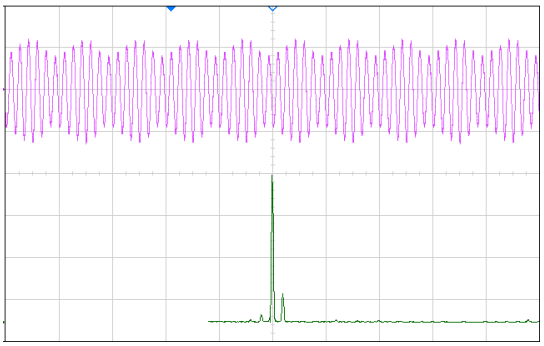
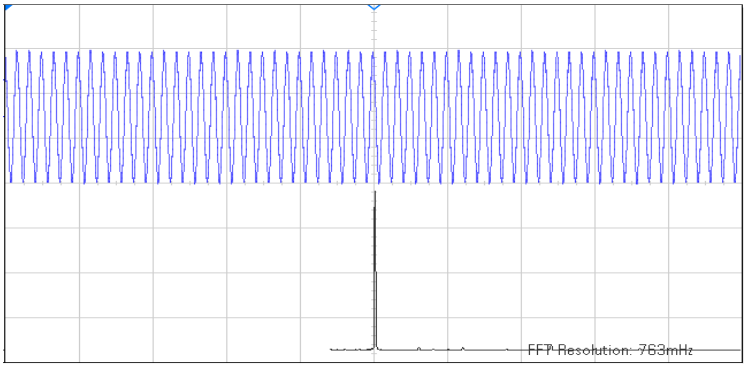
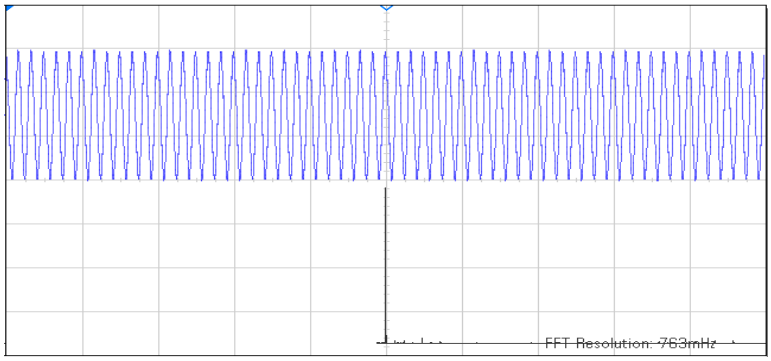


Fig. 5.29 Secondary Current at 5 Hz H-bridge Output Frequency (10A / div)(100ms / div) (60Hz FFT Center)

An important aspect that requires experimental validation is the cancelation of additional injected current components between the secondaries of the phase shifting transformer. Otherwise, grid connection requirement is going to be violated. Fig. 5.30 presents experimental results for the CHB input current at the transformer primary for 40 Hz and 20 Hz H-bridge output frequencies. It is clear from the results, only the 60 Hz component flows at primary of the transformer.




(a) 40 Hz H-bridge Output Frequency
(20A / div)(100ms / div)(60Hz FFT Center)

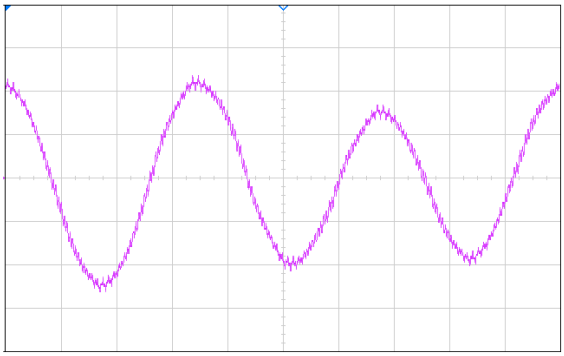



(b) 20 Hz H-bridge Output Frequency
(20A / div)(100ms / div)(60Hz FFT Center)

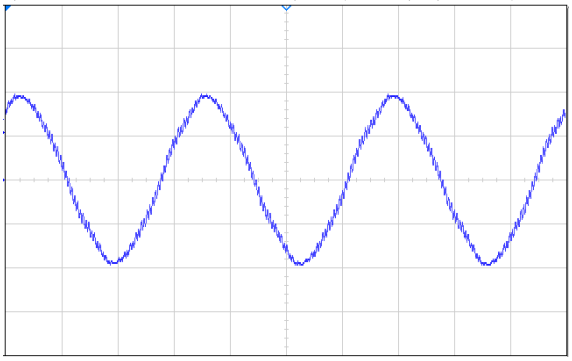
Fig. 5.30 Primary Current

A main advantage of SPWM based current controllers is the generation of specific patterns of harmonic currents, which can be cancelled out within the secondaries through phase shifting the PWM carriers within the AFEs with respect to each other [140]. This reduces the size of filtering requirement while complying with grid connection requirements for switching harmonics current components. A typical carrier shift scheme is $120^o$ between AFEs with the same voltage angle [140]. Fig. 5.31 provides a zooming on current waveforms at the secondary and the primary sides. The results show that the harmonic cancellation between AFEs is

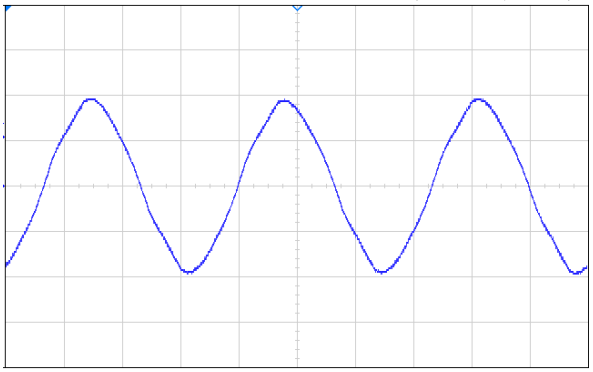
still intact even with injection of additional current components at the secondaries. This confirms the compliance of the proposed AFE control with the grid connection harmonic requirements.



(a) Secondary Current (5 A/ div) (5 ms / div)



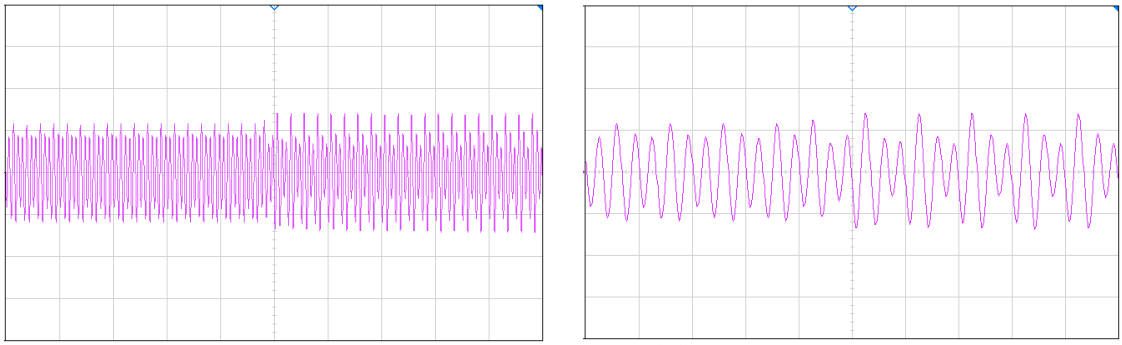
(b) Primary Current with No Carrier Shift (15.2 A/ div) (5 ms / div)



(c) Primary Current with Carrier Shift (15.2 A/ div) (5 ms / div)

Fig. 5.31 Secondary and Primary Current Waveforms at 20 Hz H-bridge Output Frequency.

Another important aspect to be validated experimentally is the dynamic performance of the multi-frame current control. Being employed in motor drive application, the proposed AFE control scheme should meet demanding dynamic performance requirements. The AFE controller is subjected to a step change in H-bridge output frequency representing a demanding condition, which is harsher than typical situations in motor drives applications. Fig. 5.32 presents the secondary current dynamics during a step change in output frequency from 10 Hz to 50 Hz. The results shows smooth transition without overshoots in the current waveform.



(a) Secondary Current (10 A / div) (200 ms / div)

(b) Zoomed Secondary Current (10 A / div) (50 ms / div)

Fig. 5.32 Step Change in Output Frequency from 10 Hz to 50 Hz.

In order to validate the ability of the proposed AFE control to divert the pulsating power away from the DC-bus capacitors, and so improve capacitor's lifetime can be achieved, a simulation study considering the real case stresses has been conducted. Table 5.6 provides system and cell parameters used in the study.

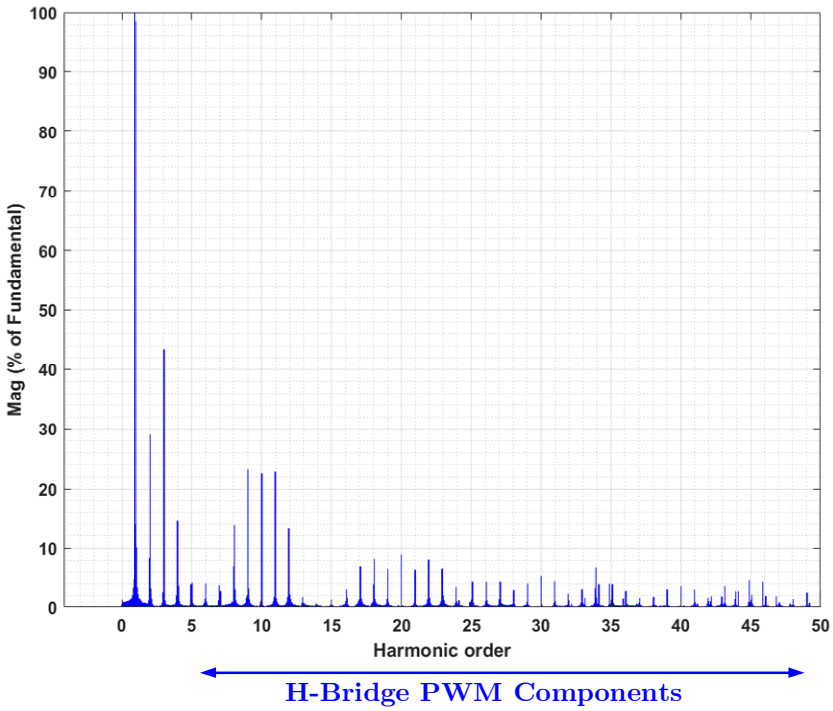
The study compares the stresses in case of conventional AFE power cell with respect to DFE power cell. Then it quantifies the gain achieved in capacitor lifetime when AFE diverts pulsating power away from the capacitor.

Table 5.6 Power Cell Parameters

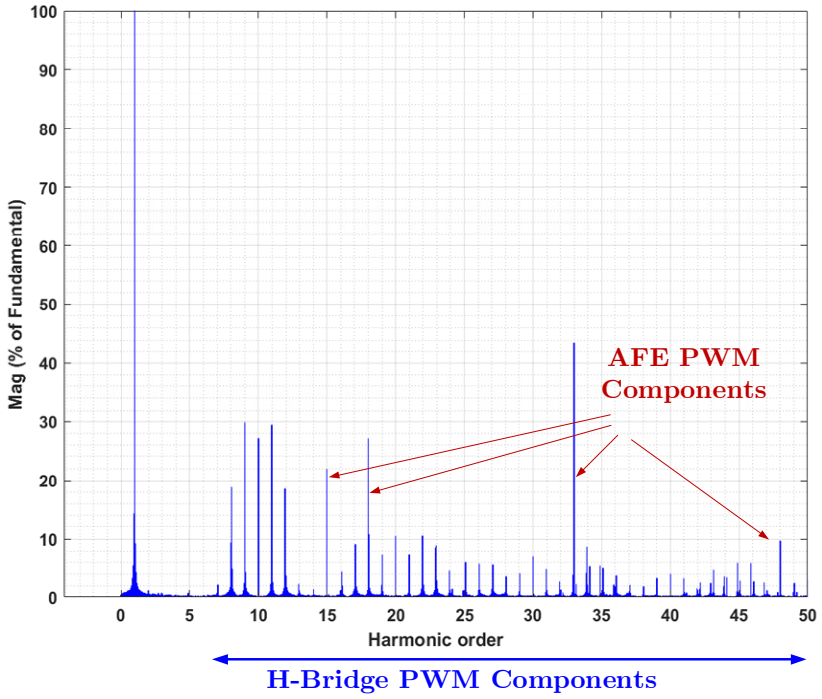
| Converter Parameter | DFE | AFE |
|---|---|---|
| **Cell DC-bus voltage (V)** | 1100 | 1100 |
| **Transformer Secondary Side Voltage (V)** | 780 | 650 |
| **Equivalent Secondary Inductance (mH)** | 4 | 4 |
| **DC-Bus Capacitance (µF)** | 8600 | 8600 |
| **Switching Frequency** | 600 Hz (H-bridge) | 600 Hz (H-bridge)<br>1980 Hz (AFE) |

Fig. 5.33 shows the FFT of capacitor current. Fig. 5.33a presents the FFT in case of DFE power cell. The dominant components in the capacitor current are the double H-bridge frequency near 120 Hz ($1^{st}$ order) of 12 A, the six times H-bridge frequency ($3^{rd}$ order) of 5.2 A, and the double H-bridge PWM frequency ($10^{th}$ order) of 2.6 A. Fig. 5.33b presents the FFT in case of AFE power cell with conventional control. The dominant components in the capacitor current are the double H-bridge frequency near 120 Hz ($1^{st}$ order) of 9.5 A, the double H-bridge PWM frequency ($10^{th}$ order) of 2.85 A, the AFE first harmonic group ($15^{th}$ and $18^{th}$ orders) of about 2 and 2.6 A, and the AFE second harmonic group ($33^{rd}$ order) of about 4.18 A.

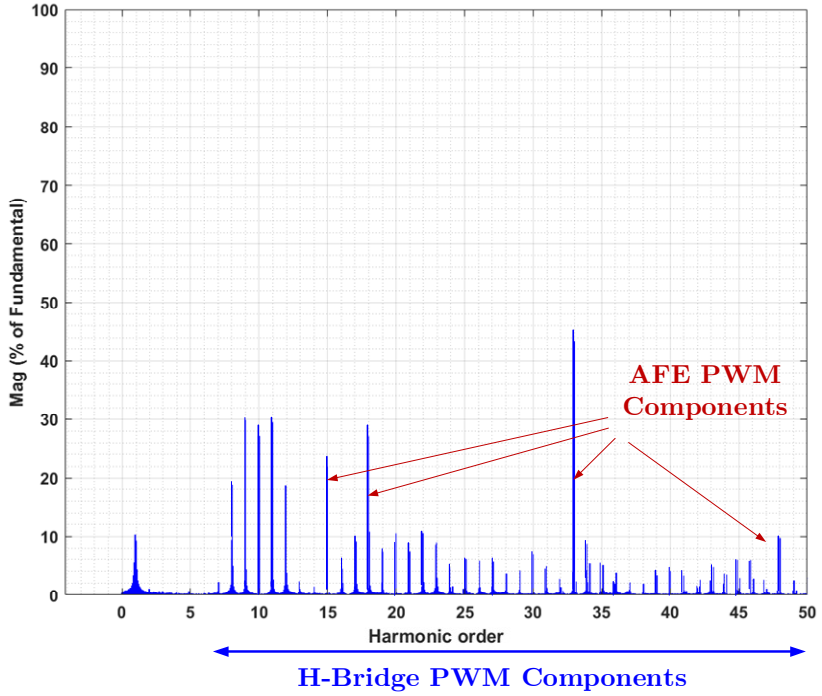
Fig. 5.33c presents the FFT in case of AFE power cell with the proposed pulsating power injection. The dominant components in the capacitor current are the double H-bridge PWM frequency ($10^{th}$ order) of 3 A, the AFE first harmonic group ($15^{th}$ and $18^{th}$ orders) of about 2.1 and 2.8A, and the AFE second harmonic group ($33^{rd}$ order) of about 4.2 A.




(a) DFE Capacitor Current FFT




(b) Conventional AFE Capacitor Current FFT




(c) Proposed AFE Capacitor Current FFT

Fig. 5.33 Capacitor Current FFT

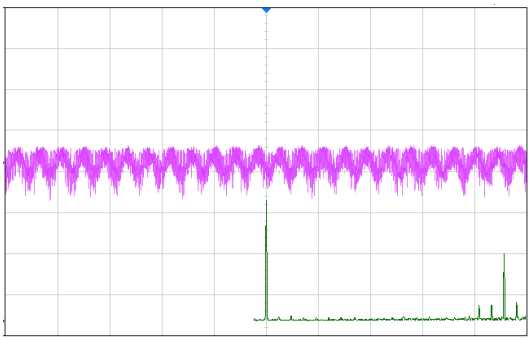
In order to quantify the gain in capacitor lifetime achieved through the proposed AFE control scheme compared to DFE and conventional AFE control scheme, analysis similar to the one presented in subsection 5.2.2 has been conducted. Similarly, in this study, a 400V, 7.9A, 1800µF, 85℃ CD29L series capacitors from Jianghai were employed.

Considering lifetime consumption due to ripple currents, other factors such as the DC voltage bias and the ambient temperature are fixed. Accordingly, the estimated lifetime as function of ripple current of electrolytic capacitors is given in Eqn. 5.4, where $\Delta T_o$ is set 10℃, and $I_o$ is 7.9A. For the DFE, the reflected rms current is about 14 A. This results in $A$ of -2.14, and consequently $K_r$ of 0.25. For the AFE with conventional control scheme, the reflected rms current is about 11.8 A. This results in $A$ of -1.23, and consequently $K_r$ of 0.4. For the AFE with the proposed pulsating power flow control, the component at double the H-bridge frequency is almost eliminated. Thereby, the reflected rms current is about 7 A. This results in $A$ of 0.2, and consequently $K_r$ of 1.1. Table 5.7 summarizes the relative gain lifetime between the three cases.

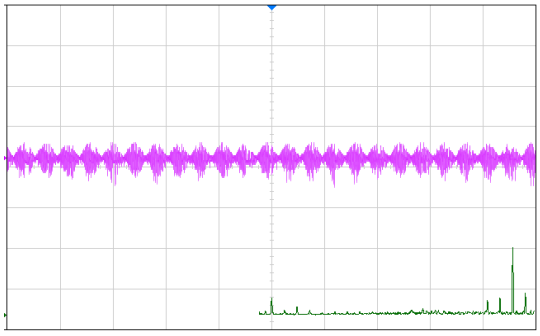
Table 5.7 DC-bus Capacitor Lifetime Improvement

| **Front End Type** | **DC-bus Capacitor PU Lifetime (Improvement %)** |
|---|---|
| DFE | 1 (Base Case) |
| Conventional AFE Control Scheme | 1.5 (50% improvement) |
| Proposed AFE Control Scheme with Pulsating Power Flow Control | 4 (300% improvement) |

The ability of the proposed AFE control to divert the pulsating power away from the DC-bus capacitors, has been validated experimentally through analyzing the DC-bus capacitors ripple current. Fig. 5.34 shows capacitor current at 60 Hz H-bridge output frequency. For the case of AFE without pulsating power flow, a 2nd order current component at 120 Hz flows through the capacitor as shown in Fig. 5.34a. Fig. 5.34b shows the huge reduction of the 2nd component through diverting it to the AFE.



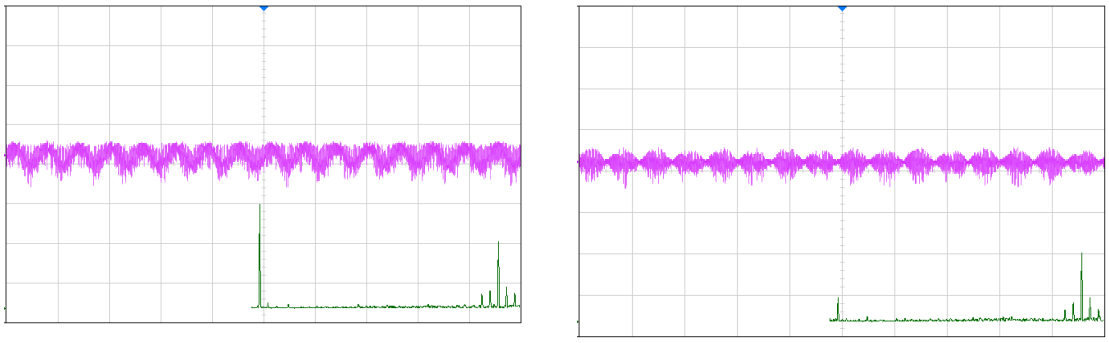
(a) AFE with No Pulsating Power Flow
(20A / div)(20ms / div)
(120Hz FFT Center)



(b) AFE with Pulsating Power Flow
(20A / div)(20ms / div)
(120Hz FFT Center)

Fig. 5.34 Capacitor Current at 60 Hz H-bridge Output Frequency.

Fig. 5.35 shows capacitor current at 40 Hz H-bridge output frequency. A 2nd order current component at 80 Hz flows through the capacitor as shown in Fig. 5.35a for AFE without pulsating power flow. With pulsating power flow capability, huge reduction of the 2nd component flowing in the capacitor is achieved in Fig. 5.35b.

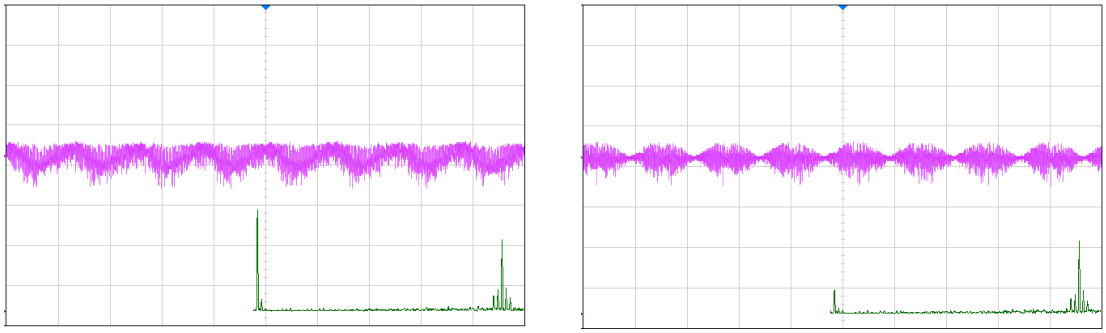


(a) AFE with No Pulsating Power Flow
(20A / div)(20ms / div)
(120Hz FFT Center)

(b) AFE with Pulsating Power Flow
(20A / div)(20ms / div)
(120Hz FFT Center)

Fig. 5.35 Capacitor Current at 40 Hz H-bridge Output Frequency.

Fig. 5.36 shows capacitor current 20 Hz H-bridge output frequency. For the case of AFE without pulsating power flow, a 2nd order current component at 40 Hz flows through the capacitor as shown in Fig. 5.36a. With pulsating power flow capability, huge reduction of the 2nd component flowing in the capacitor is achieved as shown in Fig. 5.36b. This huge reduction in low order current stresses has a significate positive effect on DC-bus capacitor lifetime.



(a) AFE with No Pulsating Power Flow
(20A / div)(20ms / div)
(120Hz FFT Center)

(b) AFE with Pulsating Power Flow
(20A / div)(20ms / div)
(120Hz FFT Center)

Fig. 5.36 Capacitor Current at 20 Hz H-bridge Output Frequency.

## 5.6.Summary

In the CHB topology, DC-bus capacitors experience high ripple current stresses due to the inherent instantaneous power unbalance existing in the CHB cells. Typically, CHB converters employ aluminum electrolytic capacitors for energy density requirements. Under these current stresses, capacitors degrade in accelerated fashion. AFEs provide a degree of freedom to control the power flow compared to DFEs. This chapter proposes a control scheme for AFEs to allow pulsating power flow without the addition of extra components. Accordingly, pulsating powers are diverted from the DC-bus capacitors to the secondary of the transformer. The proposed control scheme is based on SPWM to comply with the grid connection harmonic requirements with reduced filtering requirements. In addition, the control scheme employ multi-frame of reference current controller to achieve high

performance. Furthermore, the harmonic cancellation at the primary of the transformer including both the injected ripple current related to the diverted pulsating power and high frequency components related to switching harmonics have been addressed. Simulation studies and experimental validation have been performed on a 9-cell CHB system. The results have validated the effectiveness and the performance of the proposed control scheme while achieving the desired objectives.

# Chapter 6

# New Control Schemes Based on Grid Frequency or Near Grid Frequency Switching for AFE CHB

## 6.1.Introduction

As discussed in Chapter 2, AFEs employ sinusoidal PWM modulators to satisfy grid connection harmonic requirements. Commonly switching frequency is set up to 2 kHz to 4 kHz to reduce the size of L filters required (assuming only L filters

are used in this case). However, this reduction in filters size comes at the cost of increased switching losses of power devices. This results in high cycling temperature stresses on power devices. Numerous studies in literature have shed light on acceleration effects of these stresses on degradation of the mechanical packaging of power switches, which eventually leads to power switches failures [77-79].

Typically, for practical and cost effectiveness reasons, power modules are chosen for AFEs implementation. Switching frequency has a huge impact on modules power losses. Bringing switching frequency at nominal loading conditions down to the grid frequency or near the grid frequency results in significant improvement of modules reliability. In addition, there are other important system benefits, such as the ability of cell heat sink size reduction and the prevention of high frequency emissions into the grid caused by PWM operation that may excite resonance modes [39].

The proposed new front end (FE) control schemes address three main challenges:

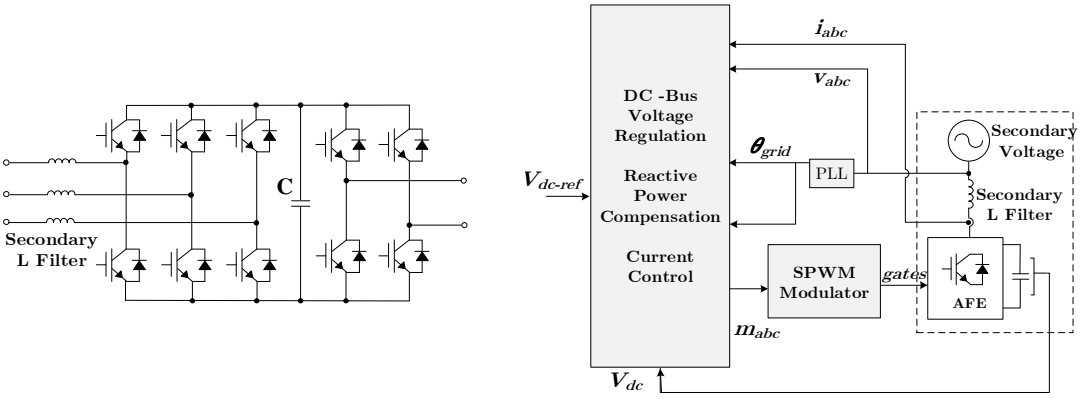
1. Improvement of power switches reliability through switching loss reduction.
2. Compliance with grid connection harmonic requirements without the addition of costly and space consuming harmonic filtering solutions.

3. Providing the performance required to suit the demanding requirements of the motor drives.

## 6.2. Background

### 6.2.1. Conventional AFE Power Cells

Fig. 6.1 presents the typical AFE CHB power cell and its typical AFE control scheme. Commonly, AFE control employs sinusoidal PWM modulators to satisfy grid connection harmonic requirements given in Table 6.1 [3, 4].




(a) AFE Power Cell (b) AFE Control Scheme Block

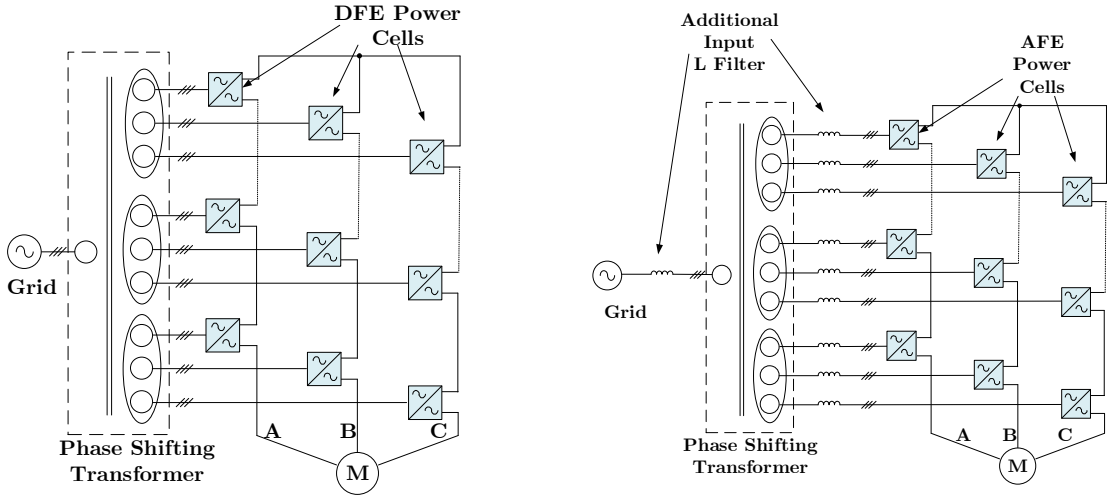
Fig. 6.1 Typical AFE.

Table 6.1 Current Distortion Limits for General Distribution Systems (120V through 69kV), IEEE std. 519-2014 [3, 4]

| **Maximum Harmonic Current Distortion in Percentage of $I_L$ Individual Harmonics Order (Odd Harmonics)** | | | | | | |
|---|---|---|---|---|---|---|
| $\mathbf{I_{sc}/I_L}$ | $\mathbf{< 11}$ | $\mathbf{11 \leq h < 17}$ | $\mathbf{17 \leq h < 23}$ | $\mathbf{23 \leq h < 35}$ | $\mathbf{35 \leq h}$ | **TDD** |
| $< 20$ | 4.0 | 2.0 | 1.5 | 0.6 | 0.3 | 5.0 |

TDD: Total demand distortion, harmonic current distortion % of maximum demand load current.
$I_{sc}$: maximum short circuit current at the point of common coupling (PCC).
$I_L$: maximum demand load current.
Even harmonics are limited to 25% of the odd harmonics limits above.

The PWM switching frequency is set up to 2 kHz to 4 kHz to reduce the size of additional input L filter distributed between the primary and the secondaries power circuities compared to the DFE CHB as shown in Fig. 6.2. Given this switching frequency range, in addition, to other aspects such as cost, reliability, and ruggedness, IGBTs modules are the common choice among CHB drives manufacturers for AFE implementations [32, 34-38, 122].



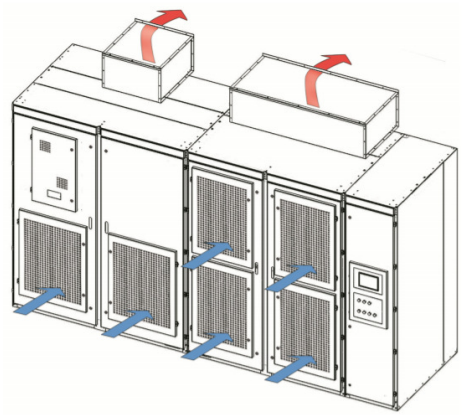

(a) DFE CHB (b) AFE CHB

Fig. 6.2 CHB Drive Grid Interface.

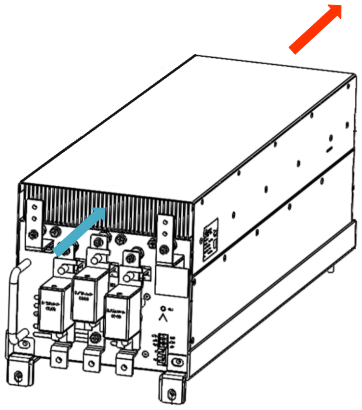
### 6.2.2. Thermal Stresses, Power Switch Modules Lifetime, and Cooling Requirements

Fig. 6.3 presents forced air-cooled DFE CHB [28-31], it shows the demanding heat sink requirement to keep the heatsink temperature at full load typically between 70 and 85☒. Going from DFE operating at grid frequency to AFEs operating at

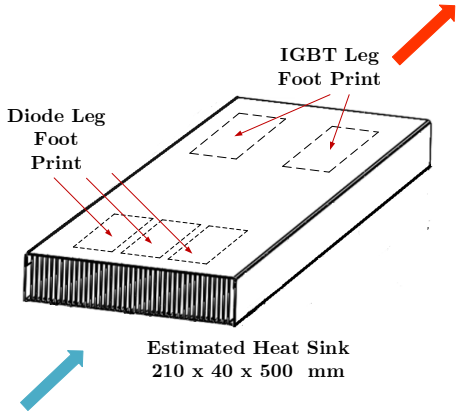
33 to 66 times the grid frequency, has huge implications on heat sink design and IGBTs' mechanical packaging long-term reliability. These implications become even stricter for applications that does not allow the usage of cooling liquids or where the usage of cooling liquids requires costly measures.



(a) Frame-H DFE CHB



(b) Frame-A 215A DFE Power Cell




(c) DFE Power Cell Heat Sink Layout

Fig. 6.3 Forced Air Cooling PowerFlex 6000 [28, 31].

For applications with forced air-cooling, in order to access the heat sink requirement for AFE power cell, an approximate comparative study between DFE and AFE power cells for power losses and junction temperature rise has been

conducted. In this study, a 1 MW, 3 kV, 7-level CHB drive driving a 3 kV, 200 A motor has been considered. For the DFE, three DD160N (34mm dual line frequency diode package) have been selected [141]. Three FF200R17KE4 (62mm half bridge IGBT module) [142] have been selected for AFE and two FF400R17KE4 (62mm half bridge IGBT module) [143] have been chosen for the H-bridge. In addition, the possibility to run the front end at grid frequency switching (referred to as FFE) has been included to the study. For comparison purposes, the FFE case uses the same switches used in the conventional AFE case. IPOSIM software from Infineon has been used to calculate devices power losses and junction temperatures [144]. Tables 6.2 summarizes the simulation conditions for DFE, H-bridge, AFE, and FFE, respectively.

Table 6.2 Inputs for DFE, H-Bridge, AFE, and FFE Simulations on IPOSIM

| **Simulation** | **DFE** | **H-Bridge** | **AFE** | **FFE** |
|---|---|---|---|---|
| **DC Link Voltage** | 950 V | 1000 V | 1000 V | 950 V |
| **Current ($I_{AC}$)** | 100 Arms | 200 Arms | 100 Arms | 110 Arms |
| **Fundamental Frequency** | 60 Hz | 60 Hz | 60 Hz | 60 Hz |
| **Switching Frequency** | N/A | 600 Hz | 2000 Hz | 60 Hz |
| **Modulation Index** | N/A | 0.9 | 0.9 | 0.9 |
| **Heat Sink Temperature** | 85 ☒ | 85 ☒ | 85 ☒ | 85 ☒ |

Table 6.3 summarizes the thermal simulation results for DFE, H-bridge (HB), AFE, and FFE, respectively. The results show large difference in total power losses per switch or diode. This leads to significant differences in estimated switch modules lifetime and cooling requirements. Comparing AFE and FFE cases, conduction losses are similar. However, AFEs switching losses are about 20 times higher than FFEs losses. As a result, using the same switch such as FF200R17KE4, FFE can be 5 times as efficient as AFE. Even FFE can achieve more efficiency gain if switch technologies optimized for conduction are employed instead. The reason is that for IGBT technologies there is a compromise between conduction efficiency and switching efficiency.

Table 6.3 Thermal Simulation Results DFE, H-Bridge, AFE, and FFE on IPOSIM.

| **Simulation** | | **DFE** | **H-Bridge** | **AFE** | **FFE** |
|---|---|---|---|---|---|
| **Conduction Losses** | *Switch* | N/A | 125.6 W | 64.1W | 64.3W |
| | *Diode* | 47.5 W | 24.0 W | 10.7 W | 19.8 W |
| **Switching Losses** | *Switch* | N/A | 34.9 W | 64.5 W | 3.0 W |
| | *Diode* | | 18.0 W | 26.6 W | 2.0 W |
| **Total Losses per Module** | *Switch* | N/A | 160.5 W | 128.6 W | 67.3 W |
| | *Diode* | 47.5 W | 42.0 W | 37.3 W | 21.9 W |
| **Maximum Junction Temperature** | *Switch* | N/A | 102.0 °C | 107.4 °C | 96.8 °C |
| | *Diode* | 98 °C | 91.5 °C | 93.7 °C | 90.1 °C |
| **Minimum Junction Temperature** | *Switch* | N/A | 97.5 °C | 102 °C | 94.25 °C |
| | *Diode* | 96 °C | 89.8 °C | 91.8 °C | 89 °C |

Typically, AFEs employ IGBT technologies that optimize both such as IGBT4 technology. For FFEs, only optimization for conduction is required such as IGBT3 technology [145].

Another important comparison point is the junction temperature. As discussed in Chapter 3, junction temperature has significant implications on the long-term reliability of IGBT modules. In order to compare the effect of thermal stresses between AFE and FFE cases, CIPS 2008 model representing IGBT module's lifetime discussed in subsection 3.4.1 can be re-expressed as follows:

$$L \simeq L_0 \ * \Delta T^{-4.46} * \ \mathrm{e}^{\frac{1285}{273+T}} \tag{6.1}$$

, where other terms in model have been neglected as they do not contribute to a significant difference in the lifetime estimation for both AFE and FFE cases. Substituting the values of the maximum junction temperature and junction temperature ripple for switches given in Table 6.3 in Eqn. 6.1:

$$\frac{L_{AFE}}{L_{FFE}} \simeq \left(\frac{5}{2}\right)^{-4.46} * \ \frac{\mathrm{e}^{\frac{1285}{273+107}}}{\mathrm{e}^{\frac{1285}{273+96}}} \simeq 0.0167 * 0.9 \ \simeq \ 0.015 \tag{6.2}$$

,this indicates that FFE can achieve about 60 times, improvement on IGBT module's lifetime in comparison to AFE. This improvement would not be important if $L_0$ is much larger than the projected lifetime of the drive, which is typically not the case. Industrial medium voltage drive systems incur large capital

investments. Thereby, their lifetime is commonly projected for 20 years and more which is comparable to $L_0$ . In this case, FFEs provide a significant reliability benefit compared to AFEs.

To access cooling requirements for DFE, AFE, and FFE, an approximate heat sink thermal simulation has been done on Mersen R-TOOLS online heatsink simulator [146]. The total power losses per IGBT or diode calculated in Table 6.3 have been fed into the simulator and the maximum allowed heat sink temperature has been set to 85 ☒ to match the previous study. Fig. 6.4 shows heat sink temperature distribution for the DFE case. The DFE is considered as the base case for which the base case heat sink dimensions and base case cooling airflow are determined. The base heat sink dimensions have been used for the AFE and the FFE, while the cooling airflow has been varied from the base case to match the power loss in each case. The results presented in Fig. 6.5a show that the FFE requires cooling airflow with 235 cfm (17% more than DFE) to limit the maximum heat sink temperature at 85☒. This causes a 23% increase in the pressure drop compared to the DFE. On the other side, the results presented in Fig. 6.5b show that the AFE needs cooling airflow with 275 cfm (37% more than DFE) to limit the maximum heat sink temperature at 85☒. The required airflow for AFE causes a 68% increase in the pressure drop compared to the DFE. Contrary to FFE, the

huge increase in both airflow and pressure drop indicates the need for a complete new heat sink and cooling designs for the AFE, which is undesirable practically.

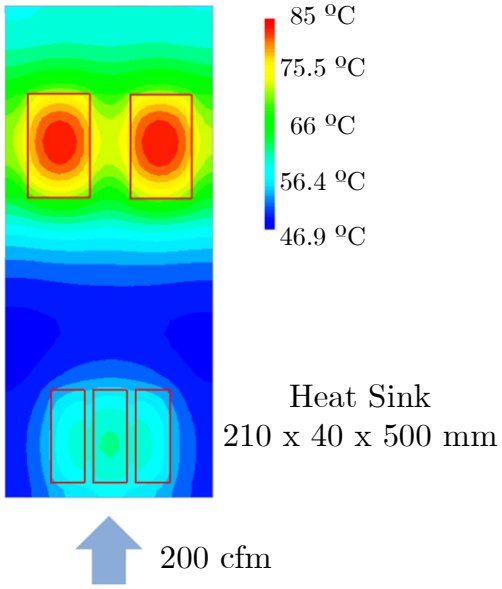



Fig. 6.4 Heatsink Simulation Results for DFE [28-31].

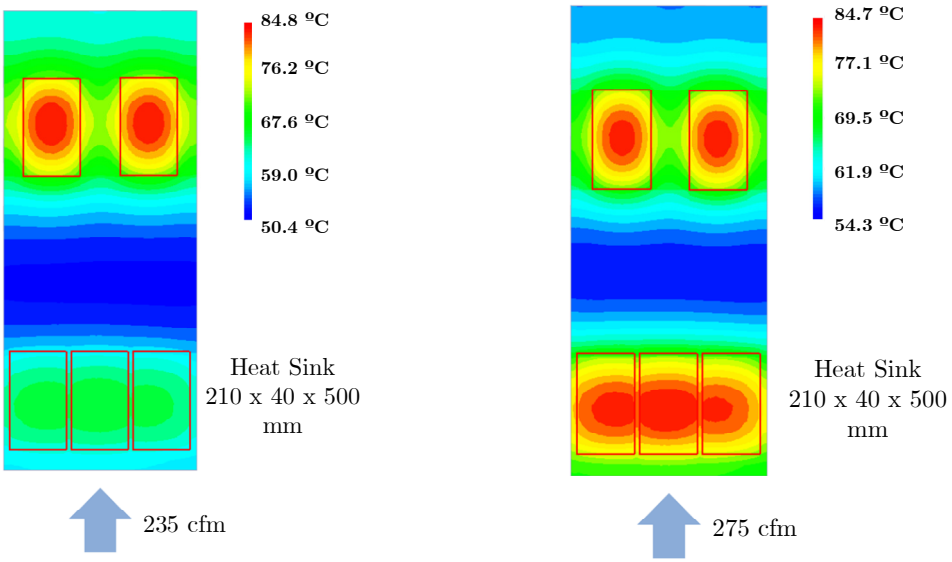



Fig. 6.5 Heatsink Simulation Results for FFE and AFE.

Based on previous discussion, huge improvement in reliability and reduction in cost, footprint and complexity can be achieved through reducing IGBTs switching frequency. Therefore, two new front end control schemes operating at grid or near grid frequency switching are proposed in the subsequent section.

## 6.3. Designing a New Front End Based on Grid or Near Grid Frequency Switching

### 6.3.1. Theory and State-of-the-Art

Grid or near grid frequency switching were introduced in two-level converter topology, shown in Fig. 6.6, for low cost regenerative low voltage drive solutions [147-152]. Commonly, under nominal conditions, IGBT modules are turned on and off once per grid frequency. The following discussion introduces different modulation and control schemes existing in the state-of-the-art to implement grid or near grid frequency switching for two-level front ends.

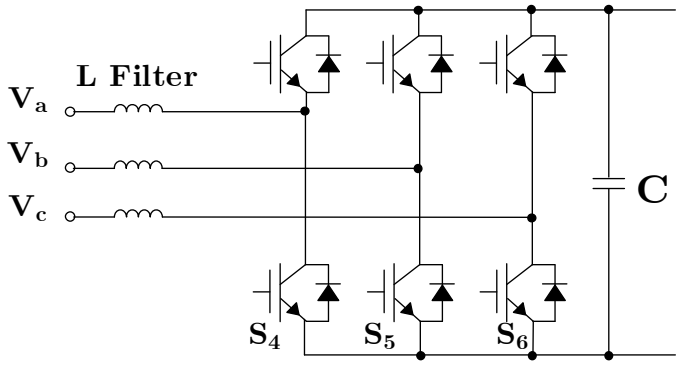



Fig. 6.6 Two-Level Front End.

### a) Natural Triggering Control

One approach is discussed in [147-151], in which diodes operate and IGBTs are deactivated during motoring mode, while diodes are reverse-biased and IGBTs are triggered during regeneration mode. IGBTs are triggered at their natural triggering instants at the intersections of the front end input line voltage waveforms during regeneration mode. Fig. 6.7 illustrates the natural triggering process. This mimics diode operation but in regeneration mode. Fig. 6.7 shows that under natural triggering, each switch conducts for $120°$ per grid frequency cycle.

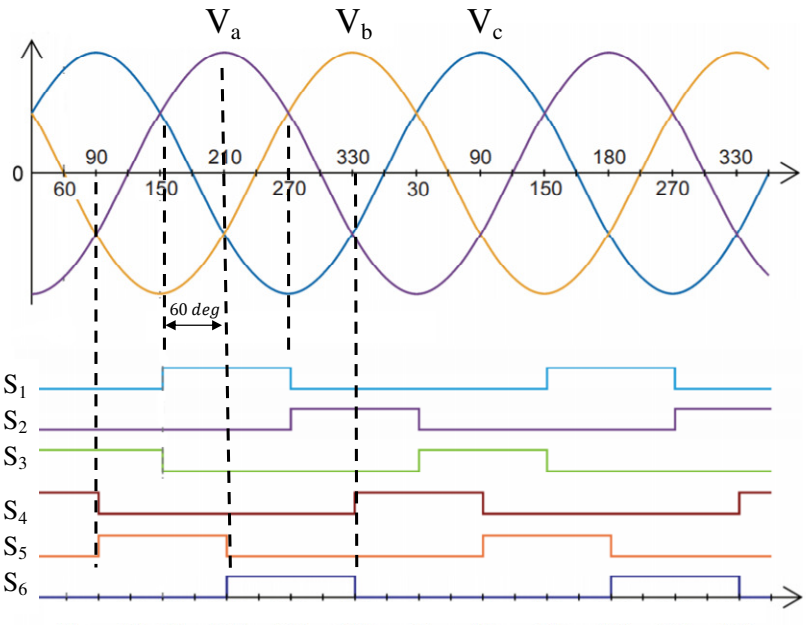



Fig. 6.7 IGBTs Natural Triggering Instants During Regeneration [147].

The DC-bus voltage utilization ($V_{LL(r.m.s.)}/V_{DC}$) for the two-level front end under this modulation scheme with respect to input line-to-line voltage is about

70%, which is similar to the case of the diode bridge. A simple control scheme employing this modulation scheme is shown in Fig. 6.8 [147]. It utilizes a PLL to estimate the triggering instants based on the input voltage angle. Although this control scheme is simple, it is vulnerable to input voltage disturbances, as it does not involve a means for DC-bus voltage regulation.

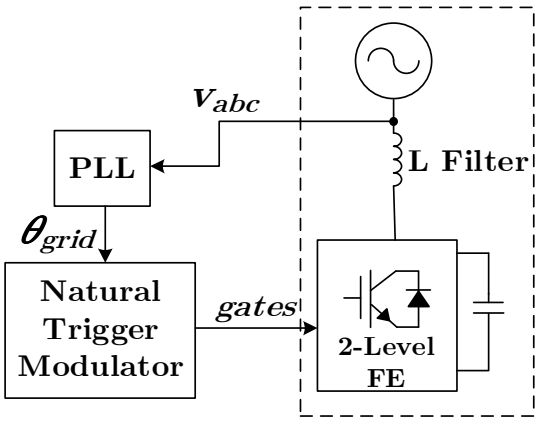



Fig. 6.8 A Simple Control Based on IGBTs Natural Triggering at Regeneration [147].

In order to improve the performance of natural triggering during input voltage disturbances, a degree of freedom is added to the modulator to provide means for DC-bus voltage regulation. A triggering delay angle ($\alpha$) is used to reduce the IGBT conduction from $120°$ to $120°-2\alpha$. The delay angle is measured from instants at the intersections of the front end input line voltage waveforms as shown in Fig. 6.9 [149, 150]. Through the manipulation of $\alpha$, the DC-bus voltage utilization is varied according to Eqn. 6.3. This relationship between input voltage,

DC-bus voltage, and delay angle $\alpha$ can be utilized to regulate the DC-bus voltage during input voltage disturbances.

$$V_{dc} = \sqrt{2} * V_{LL} * f(\alpha) + \Delta V \tag{6.3}$$

, where $\Delta V$ is the voltage drop on equivalent inductance seen by the front end including transformer reactances and any added filter inductances.

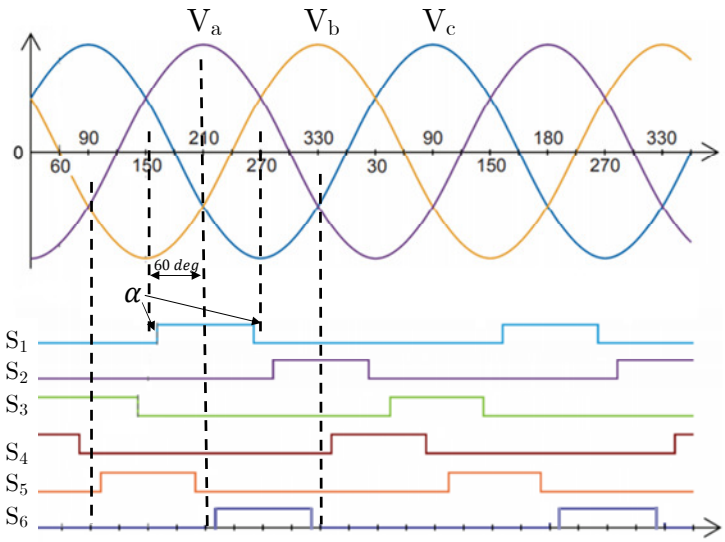



Fig. 6.9 IGBTs Triggering Based on Delay Angle ($\alpha$) during Regeneration [149, 150].

A control scheme based on the delay angle triggering is presented in Fig. 6.10. The modulator requires the input voltage angle and delay angle $\alpha$. The input voltage angle is estimated through a PLL. The delay angle $\alpha$ is determined based on the control action of a PI control regulating the DC-bus voltage to a set point.

There are two main disadvantages associated with this control scheme. First, this form of delay angle control is only suitable for symmetric input voltage disturbances. However, asymmetric input voltage disturbances are more probable. Under this control scheme, high unbalanced current peak flow under asymmetric input voltage disturbances. Second, the conduction period reduction associated with the delay angle control leads to higher current peaks if the RMS value of the current is kept the same. For example, the voltage drop on equivalent inductance seen by the front end varies with load current. This leads to variations in DC-bus voltage as given in Eqn. 6.3. Utilizing this form of DC-bus voltage regulation to regulate these load-driven variations gives rise to higher peak currents, which is undesirable.

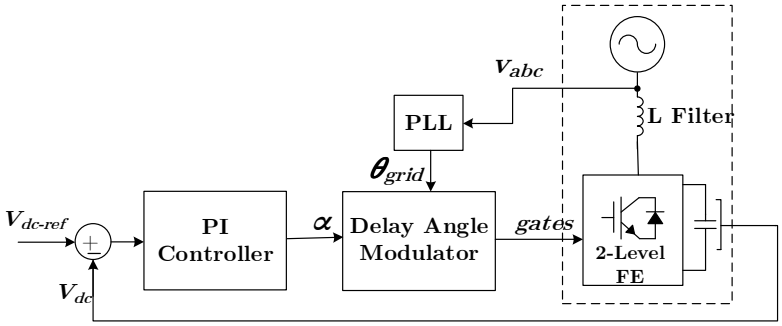


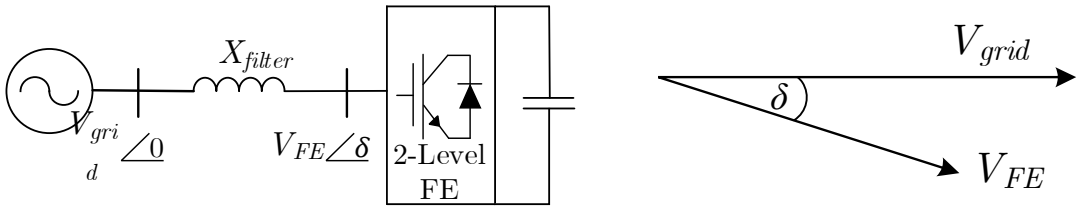

Fig. 6.10 DC-bus Voltage Regulation Based on Delay Angle Triggering at Regeneration [149, 150].

**b) Voltage Angle Control**

Another approach discussed in [150], in which the front end is set to regulate the DC-bus voltage during both motoring and regeneration modes. IGBTs operate during both motoring and regeneration to perform voltage angle control. Fig. 6.11

illustrates the concept of voltage angle control. Eqn. 6.4 shows the relation between the power flow $P$ and voltage angle $\delta$. There is no power flow if the voltage angle $\delta$ is set to zero.

The power flow is from the grid to the front end if the voltage angle $\delta$ is set to a positive value, which represents motoring mode. The power flow is from the front end to the grid if the voltage angle $\delta$ is set to a negative value, which represents regeneration mode. This relation between the power flow and voltage angle is used for DC-bus voltage regulation at no load, motoring, and regeneration.




(a) FE Circuit Diagram (b) FE Vector Diagram

Fig. 6.11 Voltage Angle Control Concept [152].

$$P \approx \frac{|V_{grid}|*|V_{FE}|}{X_{filter}} * \delta \tag{6.4}$$

, where grid voltage represents the input voltage for the front end and $\delta_{\max} = \pm 30^{o}$ to guarantee the correctness of the linear approximation in Eqn. 6.4.

Fig. 6.12 presents a possible implementation for this approach. It consists of a DC-bus controller and current-based voltage angle control. A PLL is used to estimate grid voltage angle required for modulation and $dq$ current transformation.

The DC-bus voltage controller produces $q$-axis reference current to the voltage angle controller. The voltage angle controller is comprised of a PI controller that produces a control signal $m$ based on the comparison between the reference and the measured $q$-axis current. In addition, the voltage angle controller uses the produced control signal $m$ to compute the voltage angle $\delta$ based on grid frequency, grid voltage, and the lumped equivalent resistance and filter inductance seen by the front end. The generated voltage angle $\delta$ along with the grid voltage angle are fed into the modulator to generate the gating signals to the front end based on six-step modulation as shown in Fig. 6.13. Each IGBT operates for $180°$ per grid frequency cycle. Accordingly, the DC-bus voltage utilization for the two-level front end under this modulation scheme with respect to input line-to-line voltage is about 78%.

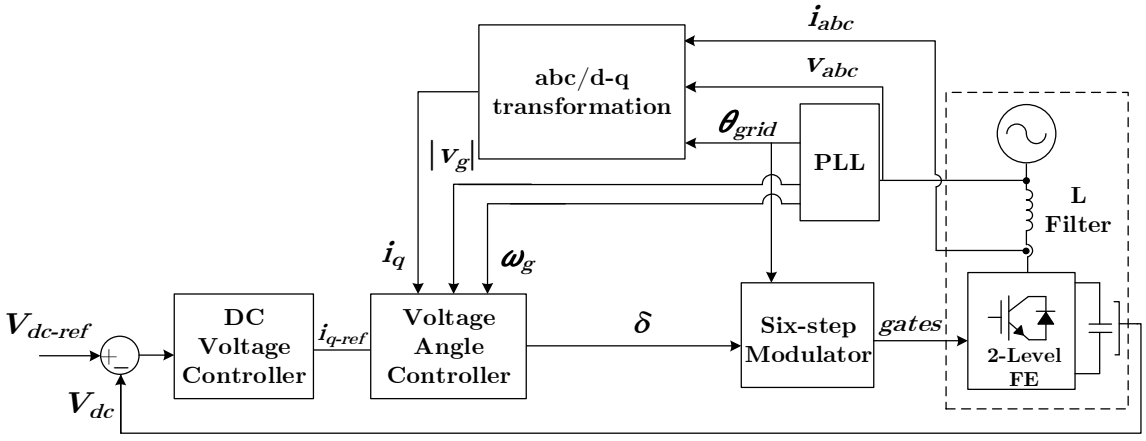
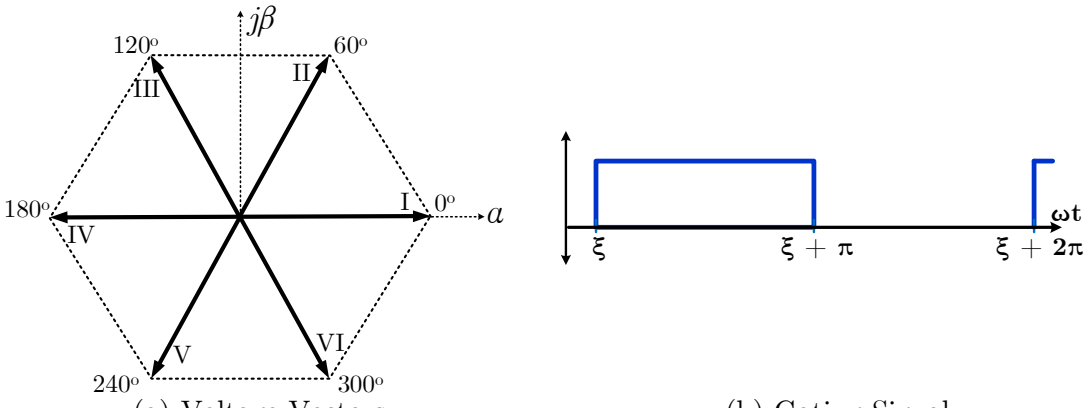



Fig. 6.12 DC-bus Voltage Regulation Based on Delay Angle Triggering at Regeneration [151].




(a) Voltage Vectors (b) Gating Signal

Fig. 6.13 Six-Step Modulation [151].

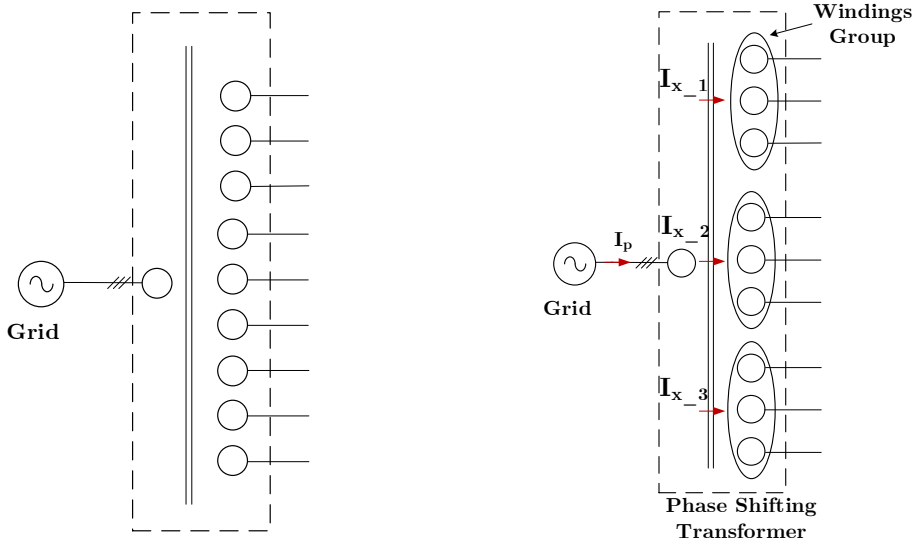
There are three main disadvantages associated with this control scheme. One of the drawbacks of this method is that it is based on current controller. Six-step front end voltages result in low order harmonic currents. These harmonic currents are difficult to filter out without affecting the controller bandwidth. This significantly reduced the motor control bandwidth. Another limitation of this control scheme is that it is highly dependent on the system parameters. In addition, there is no means for deliberate reactive power compensation, which is crucial for riding through input voltage disturbances.

### 6.3.2. Integration to the Phase Shifting Transformer

As discussed in Chapter 2, one of the important merits of the DFE CHB drives is its compliance to grid connection harmonic standards without the need for additional filters. On replacing DFEs with conventional AFEs, additional filters are

required to be added at the secondaries and may be to the primary. However, these filters can be limited to simple L filters as shown in Fig. 6.2. Going from a conventional AFE to new FE at grid or near grid frequency switching, the input harmonic profile and filtering requirement need investigation. This subsection investigates the harmonic emissions of front ends control approaches discussed in previous subsections: the $120°$ conduction natural trigger control and the $180°$ voltage angle control, considering their integration to the phase shifting transformer.

The investigation begins with revisiting the concept of harmonic cancellation in phase shifting multi-winding transformers. Fig. 6.14 compares between the multi-winding transformer and phase shifting multi-winding transformer.




(a) Multi-winding (b) Multi-winding Phase Shifting

Fig. 6.14 Grid Connection Transformers [2].

In general, the phase shifting multi-winding transformer consists of three phase-shifted winding groups, and each winding group includes $N$ phase-shifted windings. For the multi-winding transformer, the primary current equals to $N$ times the secondary current, where $N$ is the number of secondary currents. Thereby, no harmonic cancellation is achieved at the primary. On the other side, the common phase shifting multi-winding transformers employed in DFE CHB utilize two possible degrees of freedom to achieve harmonic current cancellation at the primary of the transformer with respect to the secondaries. The conventional phase shifting transformer utilizes one degree of freedom, which is phase shift angle $\delta$ between windings within each group. Given this inter-group phase shift, the primary current can be expressed as follows [2]:

$$I_{x\_1} = \sum_{i=1}^{N/3} \left[ \sum_{n=1,7,13,19,\ldots}^{\infty} I_n \sin(n(\omega t - \varphi + \delta_i) - \delta_i) + \sum_{n=5,11,17,\ldots}^{\infty} I_n \sin(n(\omega t - \varphi + \delta_i) + \delta_i) \right] \quad (6.5)$$

$$I_p = I_{x\_1} + I_{x\_2} + I_{x\_3} = 3I_{x\_1} \quad (6.6)$$

Given these harmonic current expression, for a transformer with three windings per group, this angle $\delta$ is set to $20°$. As a result, cancellation of the 5th, 7th, 11th, and 13th harmonic components is achieved. In general for *N/3* windings per group, the phase shift angle $\delta$ between windings in each group is set to $180°/N$, where $N$ is

the total number of windings. Consequently, harmonic current components of order $6i \pm 1$, where $i$ is an integer not multiple of *N/3*, are cancelled in the primary current. Thus, for a conventional phase shifting transformer with three windings per group, the highest low order harmonic current component cancelled is the 13th.

In order to achieve higher harmonic order cancelation, another degree of freedom is incorporated in the phase-shifting transformer as well, in which additional phase shift angle $\chi$ is introduced between the winding groups [30, 155]. Given this intra-group phase shift in addition to the inter-group phase shift, the primary current can be expressed as:

$$I_{x\_k} = \sum_{i=1}^{N/3} \left[ \begin{array}{l} \sum_{n=1,7,13,19,\ldots}^{\infty} I_n \sin(n(\omega t - \varphi + \delta_i + \chi_k) - \delta_i - \chi_k) \\ + \sum_{n=5,11,17,\ldots}^{\infty} I_n \sin(n(\omega t - \varphi + \delta_i + \chi_k) + \delta_i + \chi_k) \end{array} \right] \tag{6.7}$$

$$I_p = \sum_{k=1}^{3} \left[ \begin{array}{l} \sum_{n=19,37,\ldots}^{\infty} I_n \sin(n(\omega t - \varphi + \delta + \chi_k) - \delta - \chi_k) \\ + \sum_{n=17,35,\ldots}^{\infty} I_n \sin(n(\omega t - \varphi + \delta + \chi_k) + \delta + \chi_k) \end{array} \right] \tag{6.8}$$

From eqns. (6.7) and (6.8), for a transformer with three windings per group, this angle $\chi$ is set to $6.6°$, while angle $\delta$ is kept equal to $20°$. Thus, cancelation of the 17th, 19th, 35th, and 37th harmonic components is achieved, in addition to what are cancelled based on the phase shift angle $\delta$. In general, the phase shift angle $\chi$

between the three windings groups in each group is set to $20°/N$, where $N$ is the total number of windings. Consequently, harmonic current components of order $6i \pm 1$, where $i$ is an integer multiple of $N/3$, are cancelled in the primary current in addition to what are cancelled based on the phase shift angle $\delta$.

The next step is to analyze the harmonic emissions of front ends control approaches discussed in previous subsections. In the $120°$ conduction natural trigger control, the IGBTs mimics diode operation. Therefore, the front end input current can be simplified to quasi square wave as shown in Fig. 6.15. The harmonic content of this current waveform is as follows [154]:

$$\left|I_n\right| = \frac{2\sqrt{3}I_{\max}}{n\pi}, \quad n \in [1,5,7,11,13,...] \tag{6.9}$$

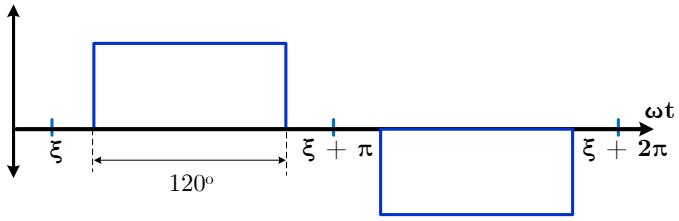



Fig. 6.15 Simplified Front End Input Current under Natural Triggering.

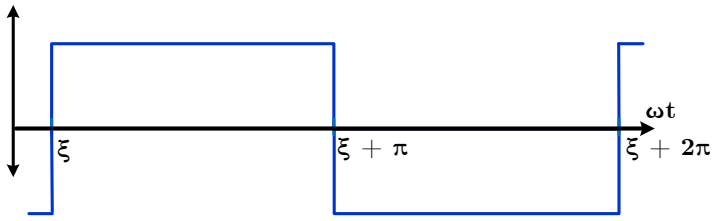
Eqn, 6.9 shows that the input front end current includes harmonic components of order $6i \pm 1$, where $i$ is an integer. Fortunately, as discussed before, the phase shifting multi-winding transformer has the capability to cancel these current harmonic on the primary. Therefore, on interfacing the $120°$ conduction natural

trigger front end to the secondary of the phase shifting multi-winding transformer, the filtering requirement required to satisfy the grid connection harmonic requirements are significantly reduced.

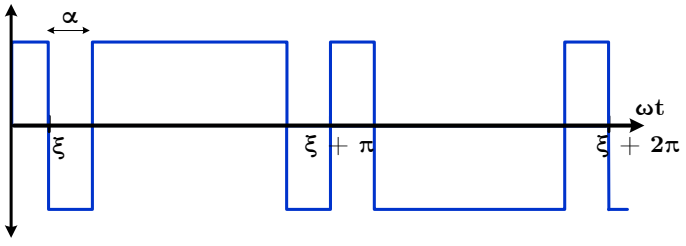
In the $180°$ voltage angle control front end, each IGBT conducts for a half a cycle, which results into a phase voltage waveform as shown in Fig. 6.16a. However, a more general switching scheme, which is to be discussed later, results into a phase voltage waveform as shown in Fig. 6.16b. The harmonic content of this front end voltage waveform and the respective input current are as follows [154]:

$$V_n = \frac{2V_{dc}}{n\pi}\left[1+2\sum_{k=1}^{N}(-1)^k \cos n\alpha_k\right], \quad n \in [1,3,5,7,9,...] \tag{6.10}$$

$$I_n = \frac{2V_{dc}}{\omega L n^2 \pi}\left[1+2\sum_{k=1}^{N}(-1)^k \cos n\alpha_k\right], \quad n \in [1,5,7,11,13...] \tag{6.11}$$




(a) 180 Conduction (Six-Step Modulation)




(b) Quasi Square Wave with Single α Angle Control

Fig. 6.16 Phase Voltage for Voltage Angle Control Front End.

Similar to the case for $120°$ conduction natural trigger control, for the $180°$ voltage angle control, the expression shows that the input front end current includes harmonic components of order $6i \pm 1$, , where $i$ is an integer. As a result, on interfacing the $180°$ voltage angle control front end to the secondary of the phase shifting multi-winding transformer, the filtering requirement required to satisfy the grid connection harmonic requirements are significantly reduced. Ideally, the harmonic current requirement at the primary can be satisfied solely through the phase shifting transformer without the need for extra filtering. However, extra filter inductances at the secondaries, as shown in Fig. 6.2b, are required to reduce the secondary current harmonics affecting both the front ends and the transformer, and reduce control interactions between the front ends.

## 6.4. Proposed New Front End Control Schemes

In this section, new control schemes are proposed for both grid frequency front end approaches presented in subsection 6.3.1.

### 6.4.1. Asymmetric Delay Angle Control

For the first approach, the objective is to address two main challenges. First, the high unbalanced current peak flow under asymmetric input voltage disturbances. Second, the sustained higher than nominal current peaks associated with DC-bus

voltage regulation function. Fig. 6.17 presents the proposed control scheme for delay angle natural triggered front end.

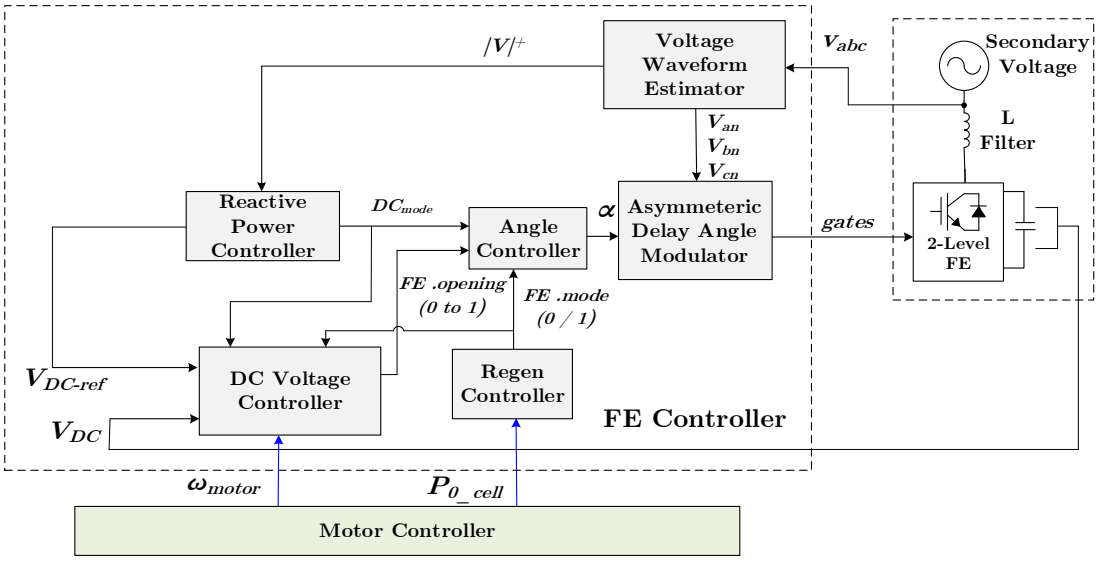



Fig. 6.17 Proposed Control Scheme for Delay Angle Natural Triggered Front End.

The proposed controller includes voltage waveform estimator, reactive power controller, DC-bus voltage controller, regen controller, angle controller, and delay angle modulator. The voltage waveform estimator utilizes a positive sequence PLL, a negative sequence estimator and waveform generators to estimate the positive sequence voltage magnitude $|V|^{+}$ and filtered phase voltage waveforms $V_{an}$, $V_{bn}$, and $V_{cn}$ as shown in Fig. 6.18. This estimation is required instead of direct measurement of voltage waveform, if to synchronize the front end to a distorted AC input, which is the typical case for industrial electrical supply. The reactive power controller

provides a DC-bus voltage control mode signal $DC_{mode}$ and DC-bus voltage reference $V_{DC\_ref}$ based on the estimated positive sequence voltage magnitude signal $|V|^{+}$. The DC-bus voltage controller provides a front end opening signal *FE. Opening* in a range of 0 to 1 based on DC-bus voltage reference $V_{DC\_ref}$, DC-bus voltage measurement $V_{DC}$, the front end mode signal *FE. Mode*, DC-bus voltage control mode signal $DC_{mode}$, and the positive sequence voltage magnitude signal $|V|^{+}$.

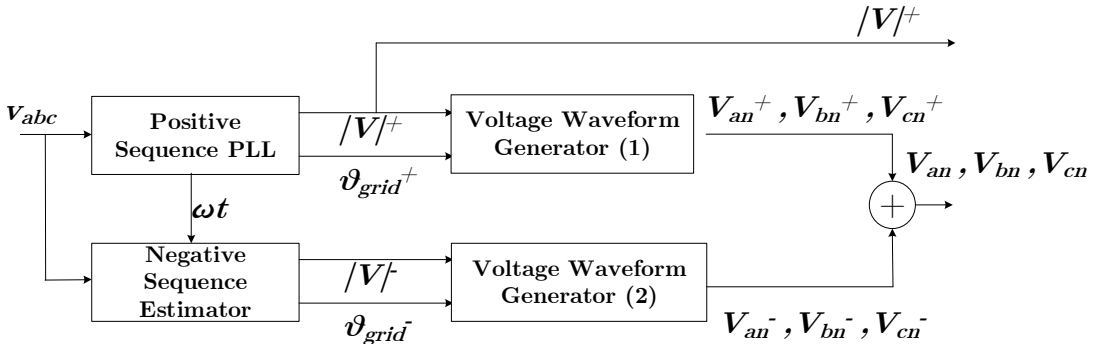



Fig. 6.18 Proposed Voltage Waveform Estimator.

DC-bus voltage controller may use $\omega_m$ information for DC-bus voltage filtration. A regen controller provides a front end mode signal *FE. Mode* having a value of 0 or 1 based on the direction of motor side power $P_{0\_cell}$ calculated at the motor controller. The DC-bus voltage controller structure is shown in Fig. 6.19. Its main task is to regulate the DC-bus voltage to the reference value only during input voltage disturbance events. This results in reduction of peak currents during nominal input voltage in trade of load-driven variations of the average DC-bus

voltage caused by the voltage drop on inductances between the front end and the supply. DC-bus voltage regulation during input voltage disturbances is performed through the signal value *FE. Opening* to a value between 0 and 1 based on the error between the reference DC-bus voltage $V_{DC\_ref}$ and the measured DC-bus voltage, the front end mode signal *FE. Mode*, and DC-bus voltage control mode signal $DC_{mode}$. In order to improve the transient response of DC-bus voltage controller, a feedforward compensator is employed based on the estimated positive sequence voltage magnitude signal $|V|^{+}$. The controller includes a range conversion from [1, 2] to [0, 1], where *FE. Opening* equals to 0 represents full obstruction against the back power flow to the grid while *FE. Opening* equals to 1 represents full permissibility for back power flow. The Logic block shown in Fig. 6.19 determines the modes of operation of the DC-bus voltage controller. The controller output *FE. Opening* is set to 1 when $DC_{mode}$ is 1, *FE. Opening* is set between 0 and 1 when $DC_{mode}$ is between 0 and 1, *FE. Opening* is set 0 when *FE. Mode* is 0.

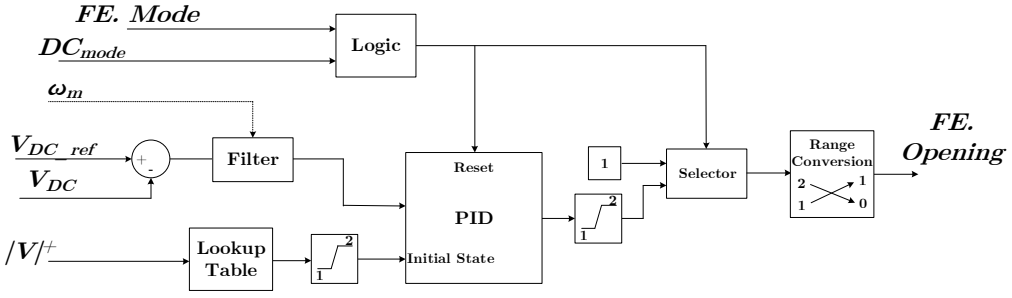



Fig. 6.19 Proposed DC-bus Voltage Controller.

The angle controller provides a delay angle signal $\alpha$ based on the front end opening signal *FE. Opening*, the front end mode signal *FE. Mode*, and DC-bus voltage control mode signal $DC_{mode}$. Table 6.4 illustrates the operational modes of the front end. At motoring, *FE. Mode* equals to 0 forces $\alpha$ to be equal to $60°$ or higher, which is sufficient to assure no current flow in the IGBTs. At regeneration, during normal operation, *FE. Opening* is set to 1, which results in $\alpha$ equals to $0°$ . At regeneration, during input voltage disturbance, if the input voltage magnitude is between 0.9 and 1.1 pu, *FE. Opening* is set to 1, which results in $\alpha$ equals to $0°$ , while the DC-bus reference is manipulated between $V_{DC\_ref,\min}$ and $V_{DC\_ref,\max}$ .

Table 6.4 FE Operational Modes for Delay Angle Control

| **Input Voltage** $\lvert V \rvert^{+}$ | **Reactive Power Controller Action** $DC_{mode}$, $V_{DC\_ref}$ | **Angle Controller Action** $\alpha$ |
|---|---|---|
| 90% - 110% | $DC_{mode} = 1$, $V_{DC\_ref,\min} < V_{DC\_ref} < V_{DC\_ref,\max}$ | $\alpha = 0°$ |
| < 90% | $0 < DC_{mode} < 1$, $V_{DC\_ref} = V_{DC\_ref,\min}$ | $0° < \alpha < 30°$ |

At regeneration, during input voltage disturbance if the input voltage magnitude is below 0.9 pu, *FE. Opening* is set between 0 and 1, which results in $\alpha$ between $0°$ and $30°$, while the DC-bus reference is set to $V_{DC\_ref,\ min}$. This allows the front end to regulate the DC link voltage according to the following expression:

$$V_{dc} = \sqrt{2} * V_{LL} * g(\alpha) + \Delta V \tag{6.12}$$

, where $\Delta V$ is the voltage drop on equivalent inductance as seen by the front end, $g(a)$ is a factor relating the delay angle ∝ and corresponding DC-bus voltage at regeneration during voltage sag, where $g(0^o) = 1$ and $g(120^o) \rightarrow \infty$.

The modulator generates the gating signals based on the delay angle signal $\alpha$ and the estimated voltage waveforms signals $V_{an}$, $V_{bn}$, and $V_{cn}$. As shown in Fig. 6.20, the delay angle is asymmetric, that is the triggering of the IGBTs is delayed by $\alpha$ from the instants of the intersection of the input voltage waveforms.

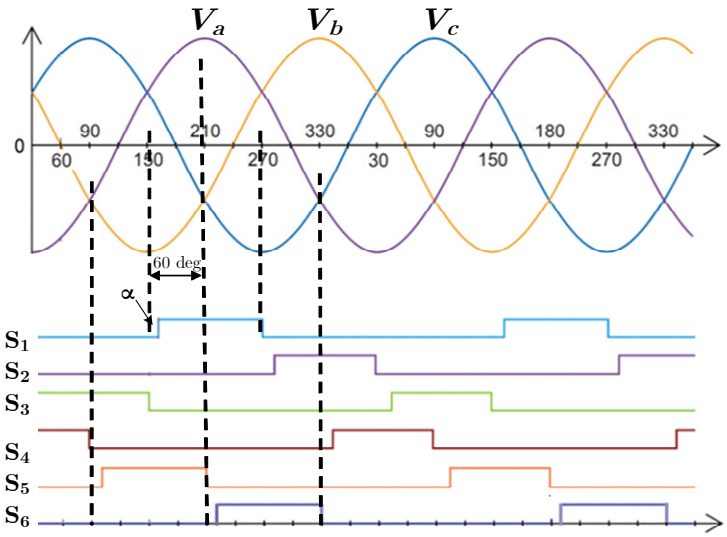



Fig. 6.20 IGBTs Triggering Based on the Asymmeteric Delay Angle Modulation.

The delay angle $\alpha$ results in reduction of the IGBT conduction from 120° to $120°-\alpha$. This is different from the symmetrical delay angle modulator presented in subsection 6.3.1. In this scheme, the triggering of the IGBTs is delayed by $\alpha$ from the instants of the intersection of the input voltage waveforms from one side.

In addition, triggering of the IGBTs is advanced by $\alpha$ from the instants of intersection of input voltage waveforms from the other side. This advanced triggering requires the prediction of the instants of intersection of input voltage waveforms, which is only possible if waveforms are symmetric. In case of asymmetric input voltage waveforms as shown in Fig. 6.21, which is more probable for input voltage disturbance events [157-163], instants of intersection of input voltage waveforms cannot be predicted. Thus, the proposed asymmetrical delay angle modulator causes lower input current unbalance in case of input voltage disturbances compared to the symmetric delay angle modulator. Fig. 6.22 shows the proposed asymmetric delay angle modulation under input voltage unbalance.

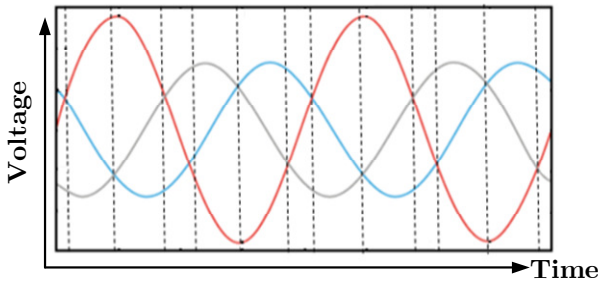



Fig. 6.21 Estimated Voltage Waveform under Asymmetric Input Voltage Disturbance.

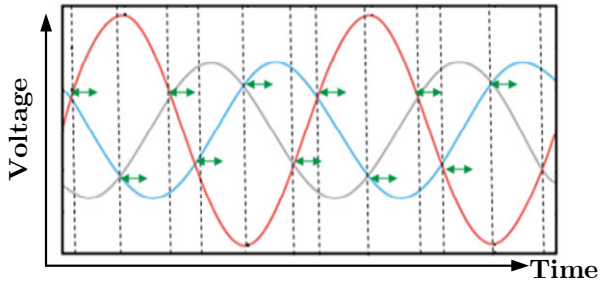



Fig. 6.22 Proposed Asymmetric Delay Angle Modulation under Asymmetric Voltage Disturbance.

### 6.4.2. Proposed Voltage Angle Control

For the second approach, the objective is to address three main challenges. First, the low control bandwidth caused by the inherently sluggish current control. Second, the high dependence of the controller on system parameters. Third, the lack for means for deliberate reactive power compensation, which is crucial for riding through input voltage disturbances [164-170]. Fig. 6.23 presents the proposed control scheme for voltage angle control. The proposed controller includes a positive and negative sequence PLL, reactive power controller, DC-bus voltage controller, active power controller, waveform generator and negative sequence compensator, and voltage waveform modulator. The PLL block provides positive and negative sequence voltage magnitudes $|V|^{+}$ and $|V|^{-}$, angles $\theta_{grid}{}^{+}$ and $\theta_{grid}{}^{-}$, and an intermediate angle $\omega t$ as shown in Fig. 6.24. The reactive power controller provides modulation index mode signal $m_{mode}$ and DC-bus voltage reference $V_{DC\_ref}$ based on the estimated positive sequence voltage magnitude signal $|V|^{+}$.

As shown in Fig. 6.25, the DC-bus voltage controller provides active power reference $P_{ref}$ based on DC-bus voltage reference $V_{DC\_ref}$, measured DC-bus voltage $V_{DC}$, motor power $P_{0\_cell}$, and speed $\omega_m$ calculated at the motor controller. The controller employs a gain scheduled PID with bump-less transfer capability based

on motor speed signal $\omega_m$. More aggressive controller response is used for high motor speeds for better DC-bus voltage disturbance rejection while less aggressive controller response is used for low motor speeds. Feedforward component based on motor side power $P_{0\_cell}$ is another degree of freedom for enhancing DC-bus voltage disturbance rejection and reducing input current overshoots.

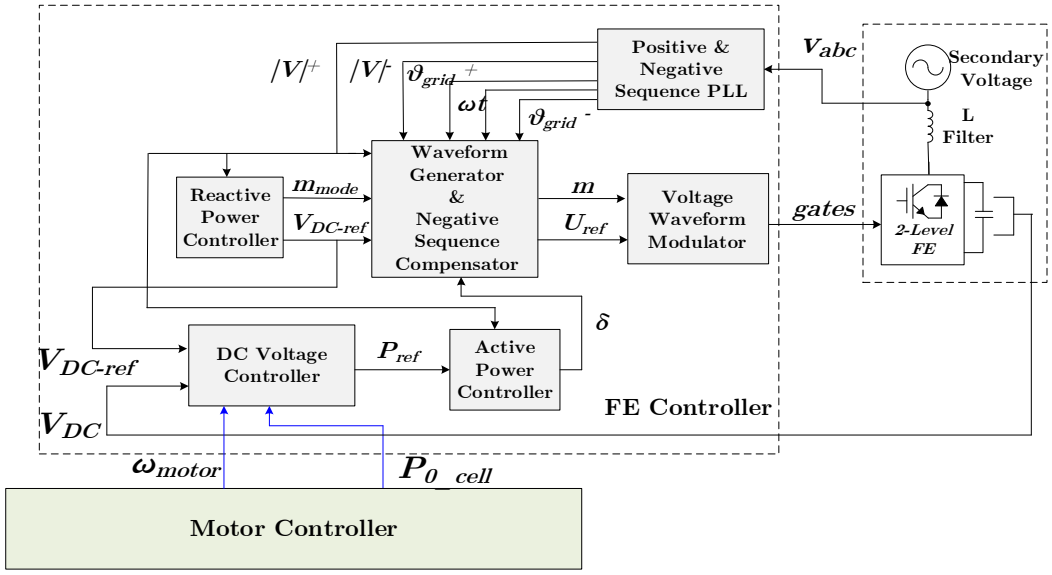



Fig. 6.23 Proposed Control Scheme for Voltage Angle Controlled Front End.

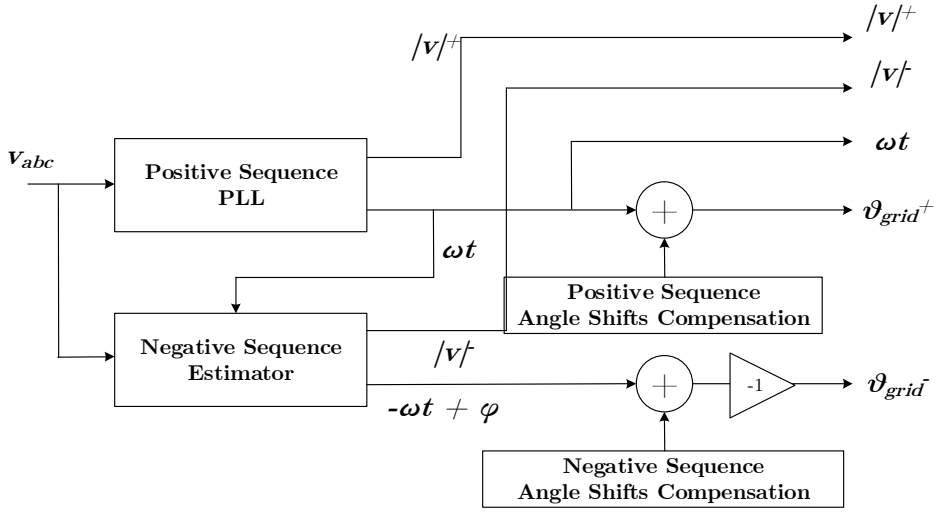



Fig. 6.24 Proposed Positive and Negative Sequence PLL.

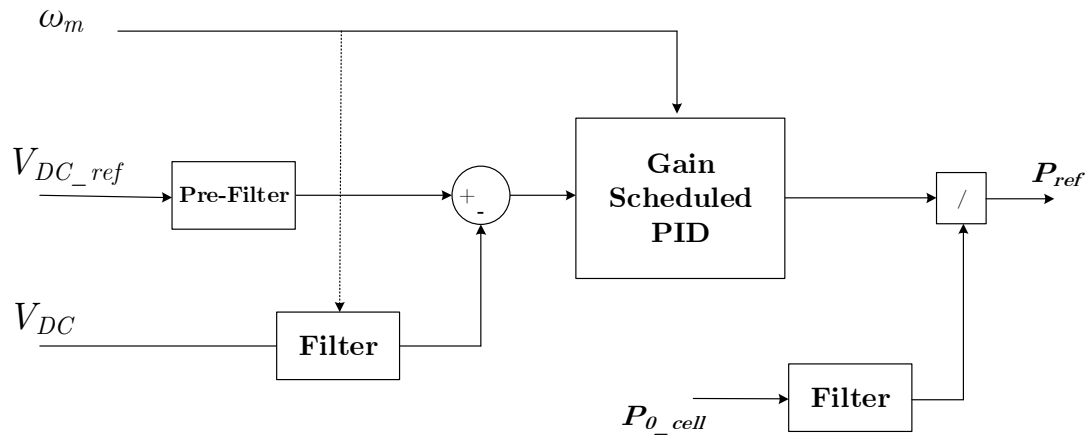



Fig. 6.25 Proposed DC-bus Voltage Controller.

In order to improve the transient response of the controller during DC-bus voltage startup, a Pre-Filter is utilized with the DC-bus voltage reference $V_{DC\_ref}$. DC-bus voltage controller may use $\omega_m$ information for DC-bus voltage filtration. The active power controller provides a power angle signal $\delta$ based on the power reference signal $P_{ref}$ and the secondary positive sequence voltage magnitude signal $|V|^+$. The power angle $\delta$ is computed according to the following approximate expression:

$$\delta \approx \frac{P_{ref} * X_{filter}}{\left(|V|^+\right)^2} \tag{6.13}$$

The voltage waveform generator and negative sequence compensator are presented in Fig. 6.26. It takes as inputs the positive and negative sequence voltage magnitudes $|V|^+$ and $|V|^-$, the angles $\theta_{grid}{}^+$ and $\theta_{grid}{}^-$, the intermediate angle $\omega t$, the DC-bus voltage reference $V_{DC\_ref}$, and the power angle $\delta$ as inputs to generate

modulation signal $m$ and the unity reference waveforms $U_{ref}$. Given these inputs, the negative sequence compensator computes the required three phase voltage magnitudes $|V_a|, |V_b|, |V_c|$ and their respective angles $\angle V_a, \angle V_b, \angle V_c$ to be produced by the front end.

Fig. 6.27 presents the details of the proposed compensator block. It implements a means to calculate the front end voltage vector: magnitude and angle for each phase, based on positive and negative sequence information. The three phase voltage magnitudes $|V_a|, |V_b|, |V_c|$; in addition to the DC-bus voltage reference $V_{DC\_ref}$ and the modulation mode $m_{mode}$ calculated at the reactive power controller are supplied to the modulation index calculator to determine the front end modulation index. The reference waveform generator receives the three phase voltage angles $\angle V_a, \angle V_b, \angle V_c$ and generates a corresponding three unity reference sinusoids $U_{ref}$.

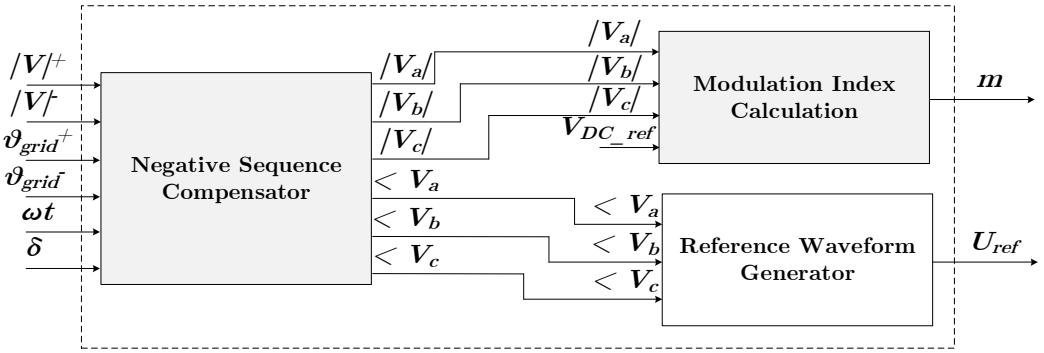



Fig. 6.26 Proposed Voltage Waveform Generator and Negative Sequence Compensator.

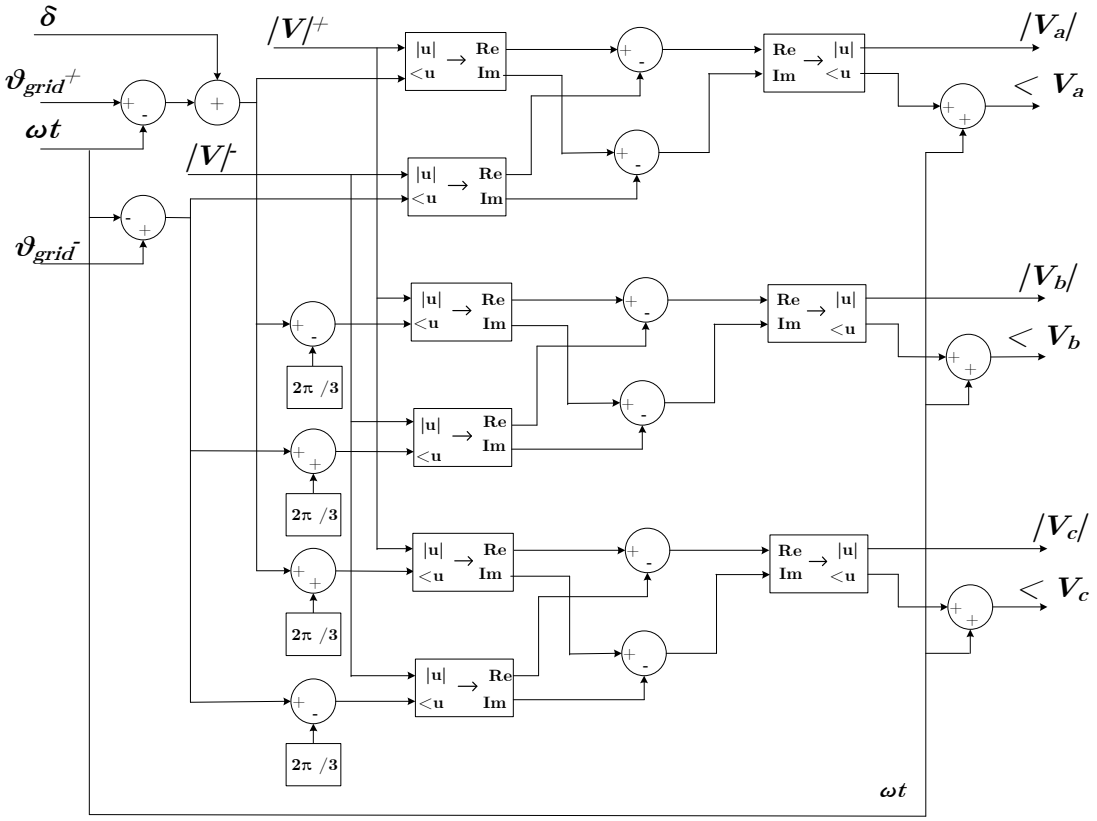



Fig. 6.27 Proposed Negative Sequence Compensator.

Fig. 6.28 illustrates the proposed modulation index calculation block. It calculates the modulation index for each phase based on Eqns. 6.14 and 6.15 assuming quasi square voltage waveform with single angle $\alpha$ as shown in Fig. 6.29. The selector block sets the modulation index either to a fixed mode ($m=1$) or variable mode ( $0<m<1$) based on $m_{mode}$ signal generated from the reactive power controller. Table 6.5 summarizes front end operation modes as implemented in the reactive power controller. The reactive power controller minimizes the difference between supply voltage magnitude and front end terminal voltage magnitudes, where the

reactive power is proportional to their difference. This is achieved by controlling the DC-bus voltage reference $V_{DC\_ref}$ and/or modulation index $m$ as given in Eqn. 6.14. During normal operation, $m_{mode}$ is set to 0, which results in $m$ equals to 1.

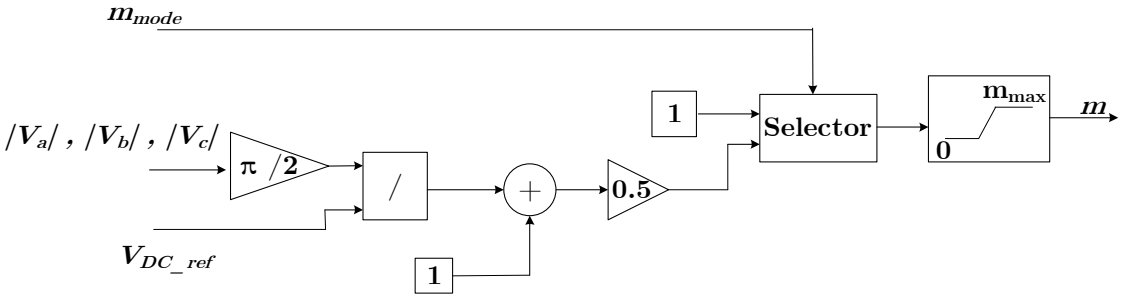
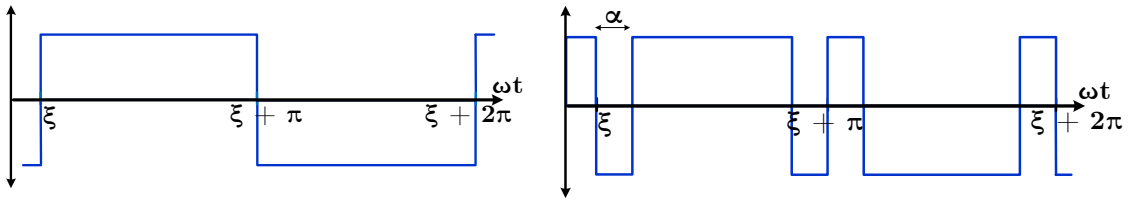



Fig. 6.28 Proposed Modulation Index Calculation.

$$m_i = [\frac{\pi}{2}\frac{|V_i|}{V_{DC\_ref}} + 1]/2, \quad i \in \{a,b,c\} \tag{6.14}$$

$$m = \cos\alpha \tag{6.15}$$




(a) $m=1$ (60 Hz) (b) $0<m<1$ (180 Hz)

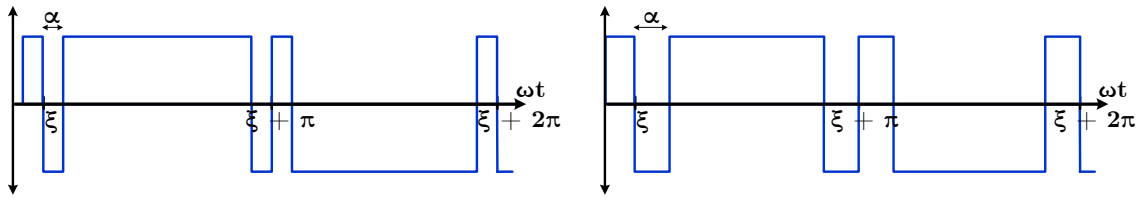
Fig. 6.29 Phase Voltage for the Proposed Voltage Angle Control Front End.

Table 6.5 FE Operational Modes for Voltage Angle Control

| **Input Voltage** $\|V\|^+$ | **Reactive Power Controller Action** $m_{mode}$ , $V_{DC\_ref}$ | **Modulation Index** $m$ |
|---|---|---|
| 90% - 110% | $m_{mode} = 1$, $V_{DC\_ref,min} < V_{DC\_ref} < V_{DC\_ref,max}$ | $m = 1$ |
| < 90% | $0 < m_{mode} < 1$, $V_{DC\_ref} = V_{DC\_ref,min}$ | $0 < m < 1$ |

During input voltage disturbance if the input voltage magnitude is between 0.9 and 1.1 pu, $m_{mode}$ is set to 0, which results in $m$ equals to 1, while the DC-bus reference is manipulated between $V_{DC\_ref,\min}$ and $V_{DC\_ref,\max}$. During input voltage disturbance if the input voltage magnitude is below 0.9 pu, $m_{mode}$ is set to 1, which results in $m$ between 0 and 1, while the DC-bus reference is set to $V_{DC\_ref,\min}$. Fig. 6.29 shows that the modulation index calculation block includes a saturation block. It can be used to limit the maximum modulation index to $m_{\max} < 1$. The $m_{\max}$ is to be chosen so that minimum secondary harmonic current THD is achieved when $m_{mode}$ is set to 1.

Fig. 6.30 shows the phase voltage for the proposed voltage angle control front end with the optimized modulation scheme. Table 6.6 summarizes front end operation modes as implemented in the reactive power controller under the optimized modulation scheme.




(a) $m = m_{\max}$ (180 Hz) (b) $0 < m < m_{\max}$ (180 Hz)

Fig. 6.30 Phase Voltage for the Proposed Voltage Angle Control Front End.

Table 6.6 FE Operational Modes for Voltage Angle Control with Optimized Modulation Index.

| **Input Voltage** $\lvert V \rvert^{+}$ | **Reactive Power Controller Action** $m_{mode}$ , $V_{DC\_ref}$ | **Modulation Index** $m$ |
|---|---|---|
| 90% - 110% | $m_{mode} = 1$, $V_{DC\_ref,\min} < V_{DC\_ref} < V_{DC\_ref,\max}$ | $m = m_{\max}$ |
| < 90% | $0 < m_{mode} < 1$, $V_{DC\_ref} = V_{DC\_ref,\min}$ | $0 < m < m_{\max}$ |

The modulator synthesizes the gating signals based on the modulation index $m$, and the unity reference waveforms $U_{ref}$ generated from the voltage waveform generator and negative sequence compensator. Fig. 6.31 illustrates a proposed implementation for the modulator block. The modulation index $m$ for each phase is converted to corresponding $\sin\alpha$ values, which are compared with the unity reference waveforms $U_{ref}$ to synthesize the required gating signals.

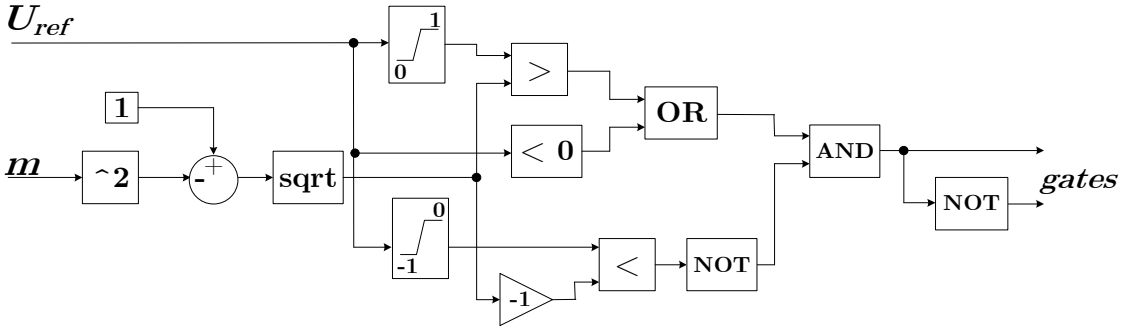



Fig. 6.31 Proposed Modulator.

## 6.5. Simulation and Experimental Validation

In order to validate effectiveness of the proposed grid or near grid frequency switching FE control schemes in achieving the stated objectives, simulation and experimental studies have been performed on a 9-cell regenerative CHB converter with parameters given in Table 6.7. System model have been built in MATLAB/Simulink.

Table 6.7 CHB Converter Simulation and Experimental Studies Main Parameters

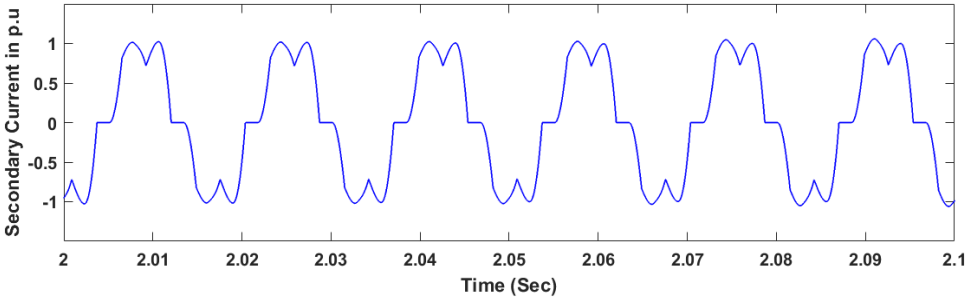
| Converter parameter | Simulation Value | Experimental Value |
|---|---|---|
| **Cell DC-bus voltage (V)** | 830 (0.93 p.u)<br>or<br>919 (1.02 p.u) | 100 or 110 |
| **Transformer Secondary Side Voltage (V)** | 650 | 80 |
| **Equivalent Secondary Inductance (mH)** | 1 | 4 |
| **DC-Bus Capacitance (μF)** | 8600 | 2300 |
| **Base Current (A)** | 200 | - |

### 6.5.1. Proposed Delay Angle Control

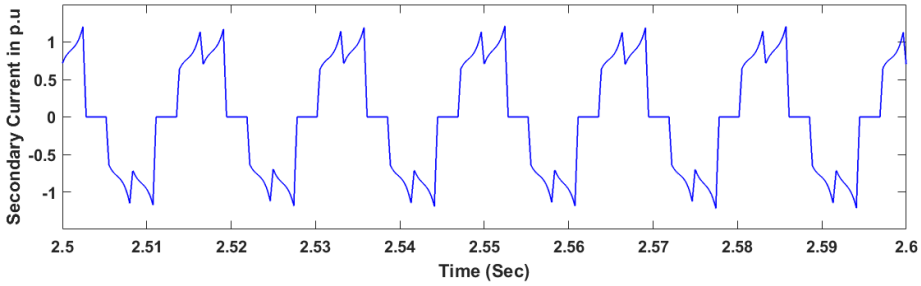
#### a) Simulation Studies

Simulation results for the proposed delay angle control under nominal input voltage are presented in Fig. 6.32. The equivalent secondary inductance used in simulation studies for this control scheme is about 1 mH to test performance at low inductance. Fig. 6.32a shows the secondary current during motoring, only back diodes conduct.

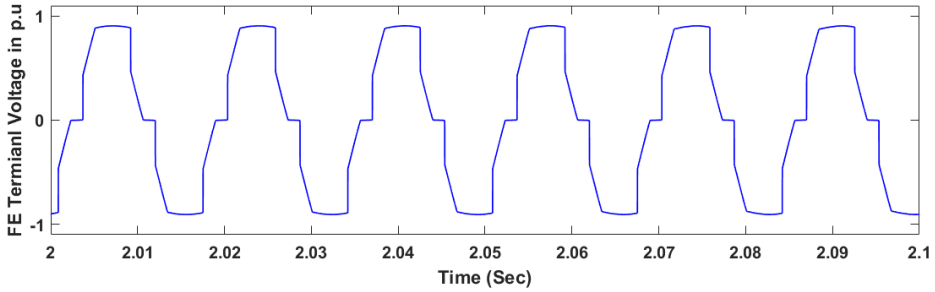
Fig. 6.32b shows the secondary current during regeneration, the current flows in the IGBTs and freewheel in the back diodes. Fig. 6.32c and 6.32d compare the line voltages at the front end terminals during both motoring and regeneration. Terminal voltage during regeneration is higher than during motoring due to the increase of DC-bus voltage during regeneration with respect to case in motoring as shown in Fig. 6.32e and 6.32f.



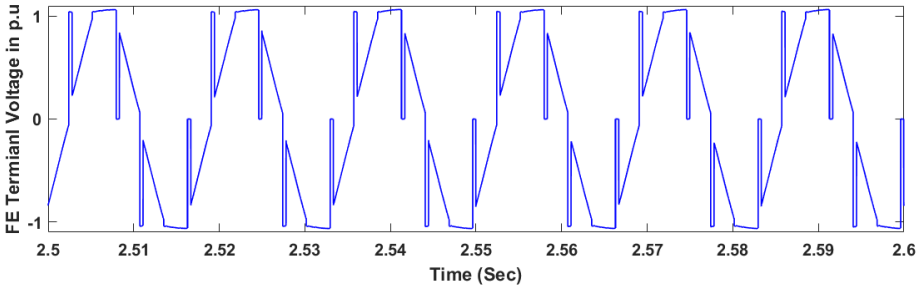

(a) Secondary Current at Motoring



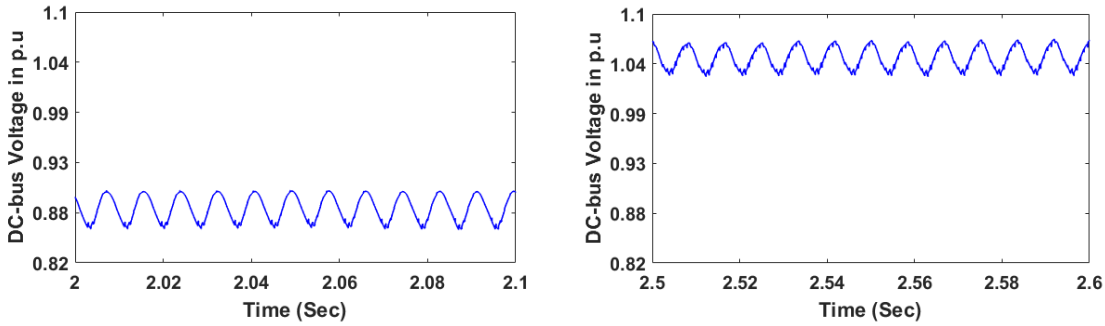

(b) Secondary Current at Regeneration




(c) Front End Terminal Voltage at Motoring




(d) Front End Terminal Voltage at Regeneration




(e) DC-bus Voltage at Motoring (f) DC-bus Voltage at Regeneration

Fig. 6.32 Simulation Results for Delay Angle Control under Nominal Input Voltage.

The dynamic performance of the proposed control scheme is important aspect to be validated. Fig. 6.33 shows the secondary current under a 1 p.u change in the regeneration power. The simulation result shows a fast dynamic response without current overshoots.

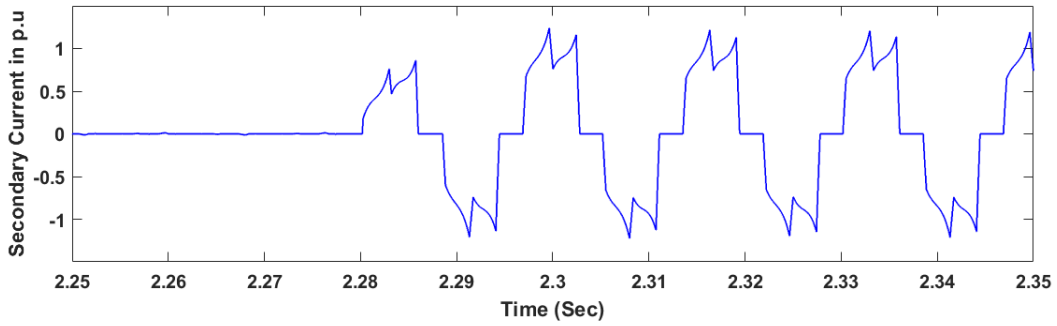
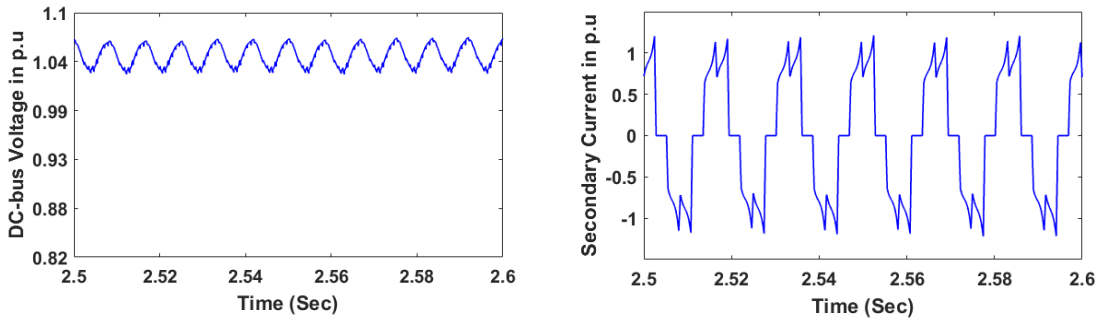



Fig. 6.33 Secondary Current during 1 p.u Step Regeneration.

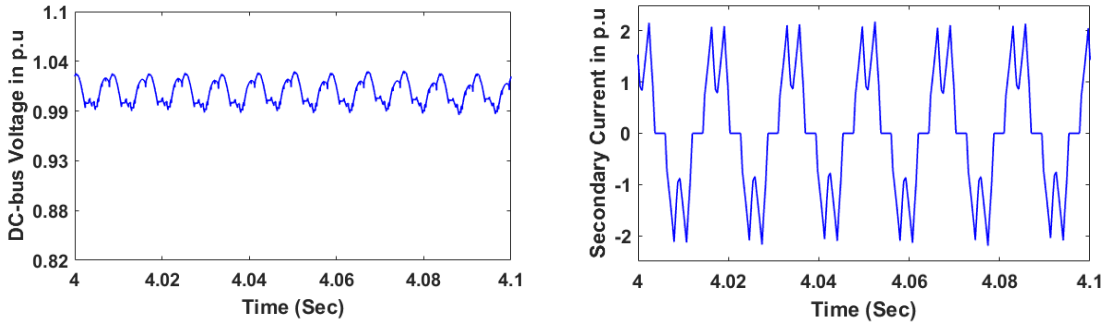
Another important aspect to be validated is that capability of the proposed control scheme to regulate the DC-bus voltage in case of voltage sag condition, either symmetric or asymmetric voltage sag. In case of asymmetric voltage sag, the proposed control scheme should be able to limit the current unbalance. Fig. 6.34 shows DC-bus voltage and secondary current at nominal conditions, where the delay angle is set to zero resulting in $120^o$ conduction of the IGBTs. At this condition, the DC-bus voltage is not regulated and the increase in the DC voltage beyond the no-load condition (1 p.u) is determined by the equivalent inductance in front of the front end and the amount of the regenerative power.




(a) DC-bus Voltage (b) Secondary Current

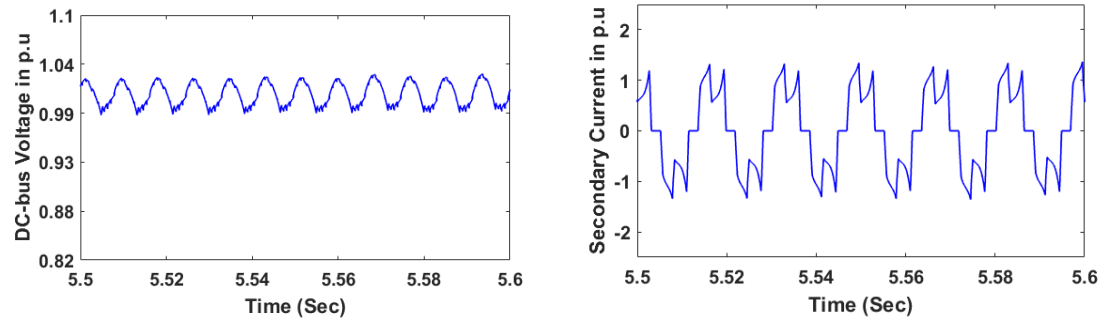
Fig. 6.34 Regeneration at Nominal Conditions.

Fig. 6.35 shows DC-bus voltage and secondary current at sag conditions. The delay angle increases to constraint the conduction of IGBTs and thereby regulating the DC-bus to its reference value (1.02 p.u). Fig. 6.36 shows DC-bus voltage and secondary current at asymmetric sag conditions. Similar to the case in Fig. 6.35 the control has managed to regulate the DC-bus through setting the delay angle.




(a) DC-bus Voltage (b) Secondary Current

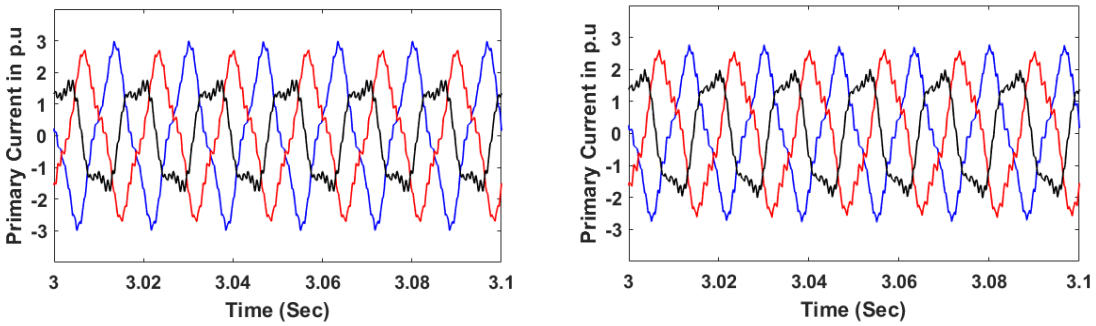
Fig. 6.35 Regeneration at Symmetric Sag Condition.




(a) DC-bus Voltage (b) Secondary Current

Fig. 6.36 Regeneration at Asymmetric Sag Condition

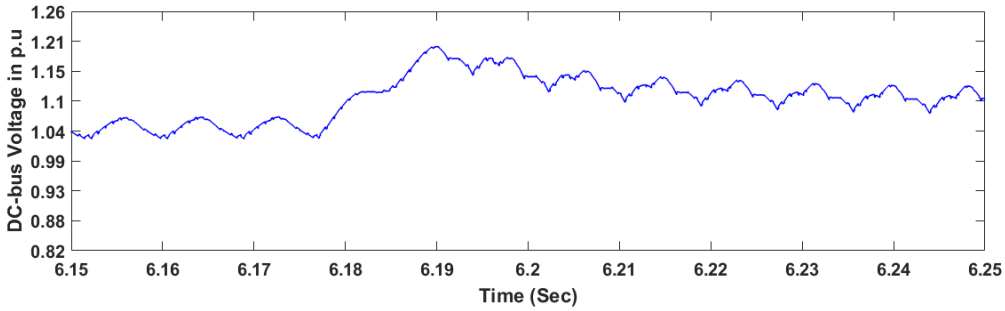
Fig. 6.37 compares primary current in case of conventional delay angle versus the proposed delay angle controller. Current unbalance in the latter case is lower.



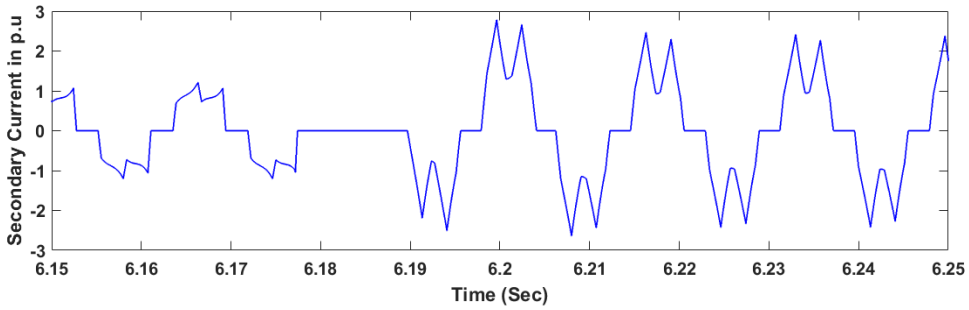

(a) Conventional Delay Angle (b) Asymmetric Delay Angle

Fig. 6.37 Primary Current at Regeneration during Asymmetric Sag Condition.

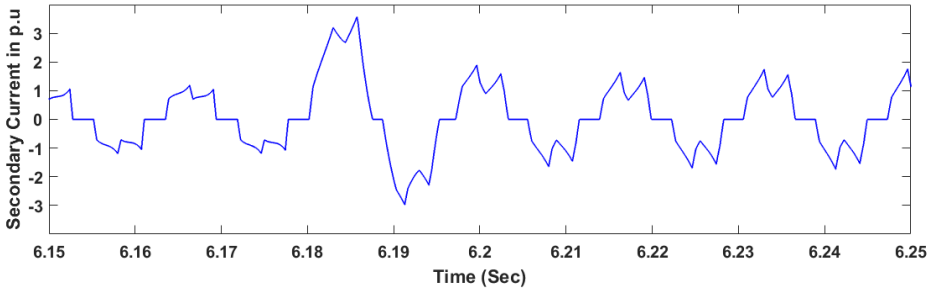
Additional important aspect to consider is the transient response accompanying change in input voltage level. Fig. 6.38 presents the dynamic response of DC-bus voltage and secondary current when input voltage changes symmetrically from 1 p.u to 0.7 p.u. Fig. 6.38a shows the dynamics of DC-bus voltage, where it reaches 1.2 p.u. Fig. 6.38b shows the secondary current transient when the sag is detected. Current is cut off for less than a cycle then it is restored. The feedforward component in Fig. 6.19 first reacts then the feedback component starts reacting. Through this procedure, the current overshoots can be limited compared to the case without this procedure as shown in Fig. 6.38c.




(a) DC-bus Voltage Transient at Voltage Sag




(b) Secondary Current Transient at Voltage Sag



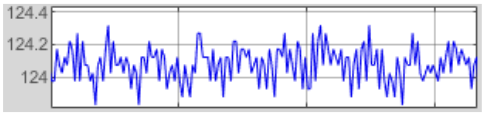

(c) Secondary Current Transient at Voltage Sag Without the Overshoot Limiting

Fig. 6.38 Transient Response of DC-bus Voltage and Secondary Current in a Sag.

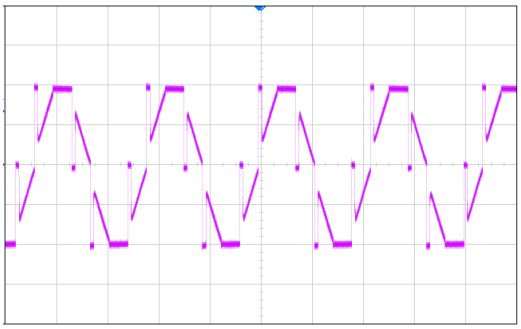
### b) Experimental Validation

Experimental validation results for the proposed delay angle under nominal and sag conditions are given in Fig. 6.39 to Fig. 6.41. DC-bus voltage, front end input terminal voltage, IGBT gating signals, and secondary current are shown respectively in Fig. 6.39. Although the no-load DC-bus voltage is about 110 V, DC-bus voltage reaches 124 V at regeneration due to the additional 4 mH in front of the front end. At sag condition, DC-bus voltage reference has been set to 110 V. Fig. 6.40 presents waveforms at about 0.7 p.u input voltage, and Fig. 6.41 presents waveforms at about 0.5 p.u input voltage. In both cases, the proposed control scheme has managed to regulate DC-bus voltage through manipulating delay angle.

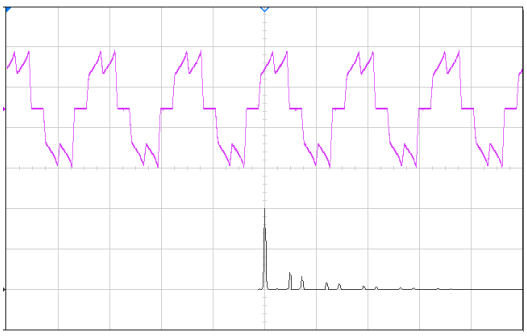
In addition, Fig 6.40 and 6.41 show that as the regenerative power is kept the same, increasing the sag depth results in larger current peaks due to corresponding decrease in conduction time. Change of conduction time is seen through comparing Fig. 6.40c and 6.41c.



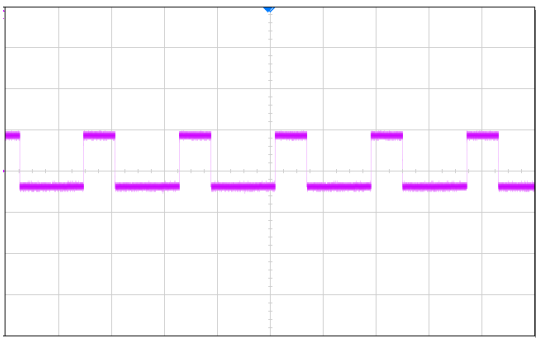

(a) SCADA Result of DC-bus Voltage



(b) FE Terminal Input Voltage
(62 V / div) (7.6 ms / div)

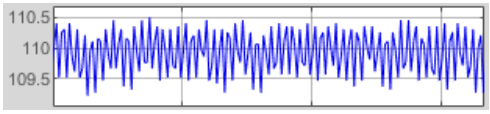


(c) Secondary Current
(5A / div)(10ms / div)
( 60Hz FFT Center)

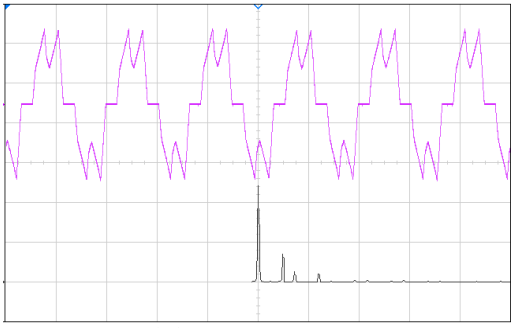


(d) Gating Signal
(18 V / div) (9.2 ms / div)

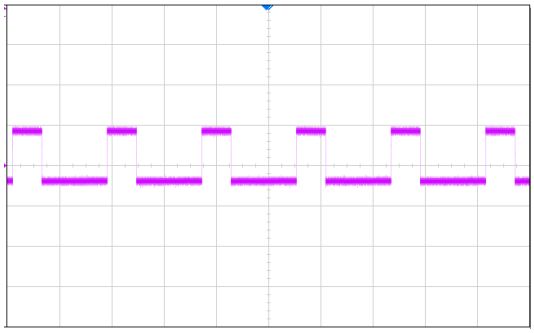
Fig. 6.39 Regeneration at Nominal Input Voltage.




(a) SCADA Result of DC-bus Voltage

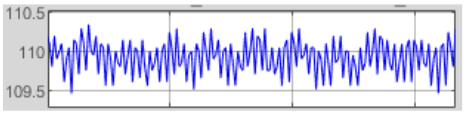


(b) Secondary Current
(5A / div)(10ms / div)

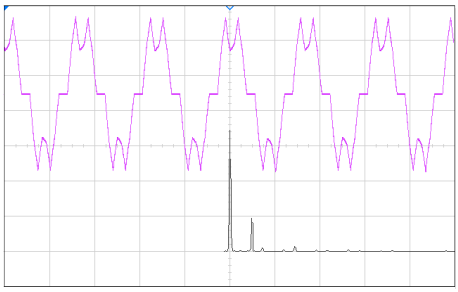


(c) Gating Signal
(18 V / div) (9.2 ms / div)

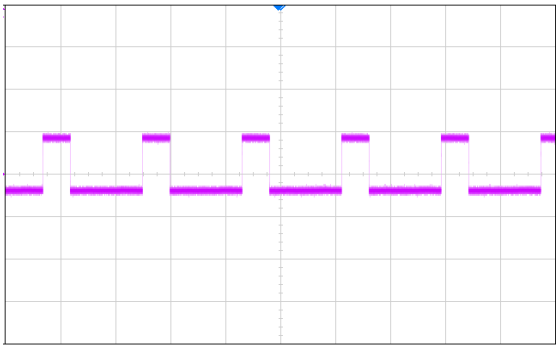
Fig. 6.40 Regeneration at Voltage Sag (0.7 p.u Input Voltage).




(a) SCADA Result of DC-bus Voltage



(b) Secondary Current
(5A / div)(10ms / div)



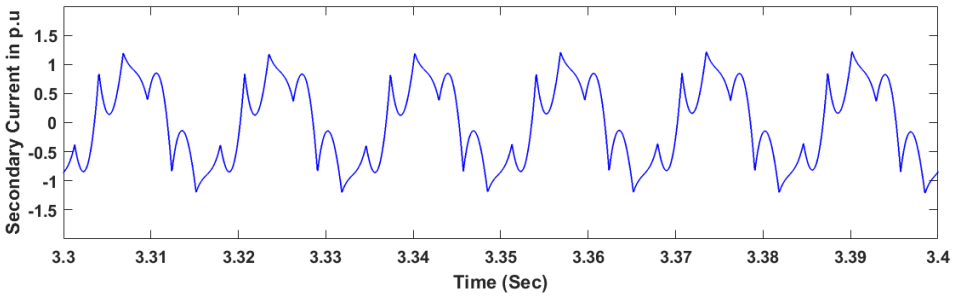
(c) Gating Signal
(18 V / div) (9.2 ms / div)

Fig. 6.41 Regeneration at Voltage Sag (0.5 p.u Input Voltage).

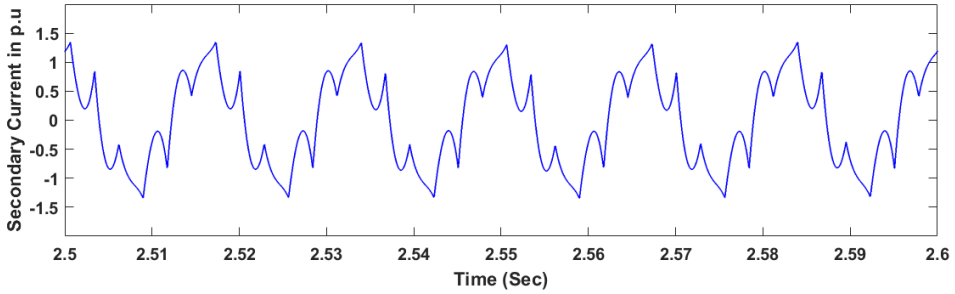
### 6.5.2. Proposed Voltage Angle Controller

#### a) Simulation Studies

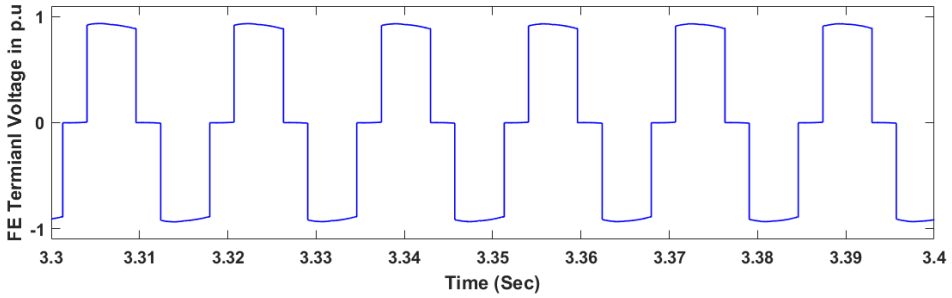
Simulation results for the proposed voltage angle controller under nominal input voltage is presented in Fig. 6.42. The equivalent secondary inductance used in simulation studies for this control scheme is about 1 mH to test performance at low inductance. Fig. 6.42a and 6.42b show secondary current during motoring and regeneration conditions respectively. In both cases, current flows in the IGBTs and freewheel in the back diodes. Fig. 6.42c and 6.42d compare the line voltages at the front end terminals during both motoring and regeneration. The peak of the terminal voltage in both cases is almost equal because DC-bus voltage is regulated to the reference (0.93 p.u) in both cases as shown in Fig. 6.42e and 6.42f.



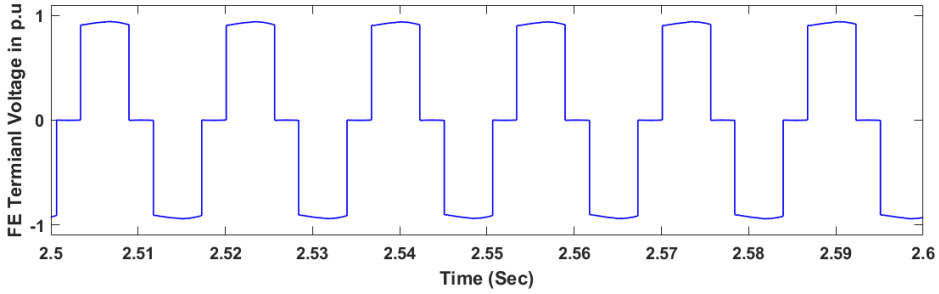

(a) Secondary Current at Motoring



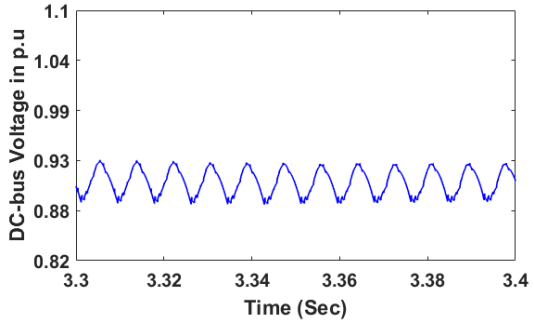

(b) Secondary Current at Regeneration



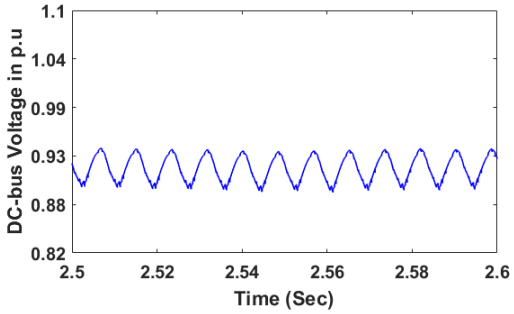

(c) Front End Terminal Voltage at Motoring




(d) Front End Terminal Voltage at Regeneration




(e) DC-bus Voltage at Motoring




(f) DC-bus Voltage at Regeneration

Fig. 6.42 Simulation Results for Voltage Angle Control under Nominal Input Voltage.

The dynamic performance of the proposed control scheme is important aspect to be validated. Fig. 6.43 shows secondary current under a 1 p.u change in regeneration power. The simulation result shows a fast smooth dynamic response without overshoots in the current. In addition, it is important to note that there is current flow at no load conditions. However, this current is composed of harmonic components and does not contain fundamental component. Given a DC voltage reference value, the magnitude of these harmonic components depends on the equivalent secondary inductance. The modulation scheme illustrated in Table 6.6 can be employed to reduce the harmonic current at no load.

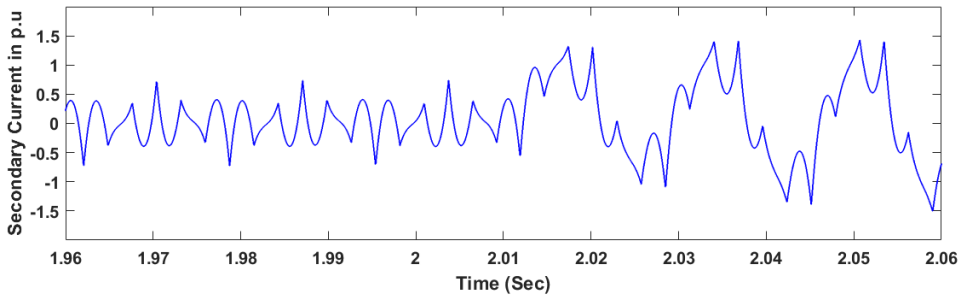
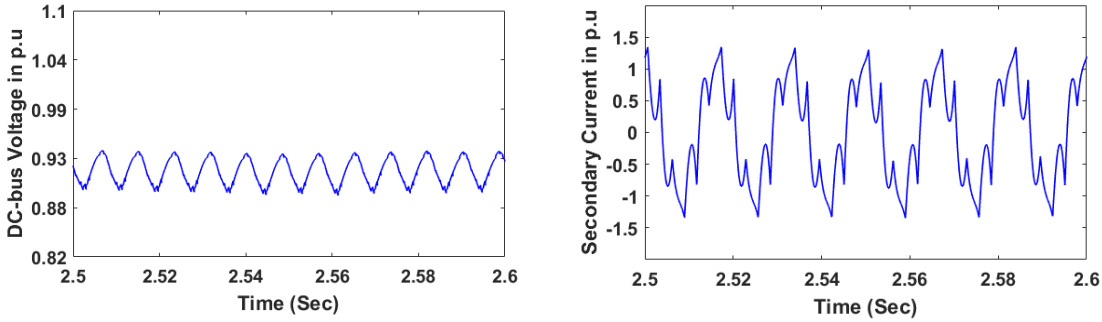



Fig. 6.43 Secondary Current during 1 p.u Step Regeneration.

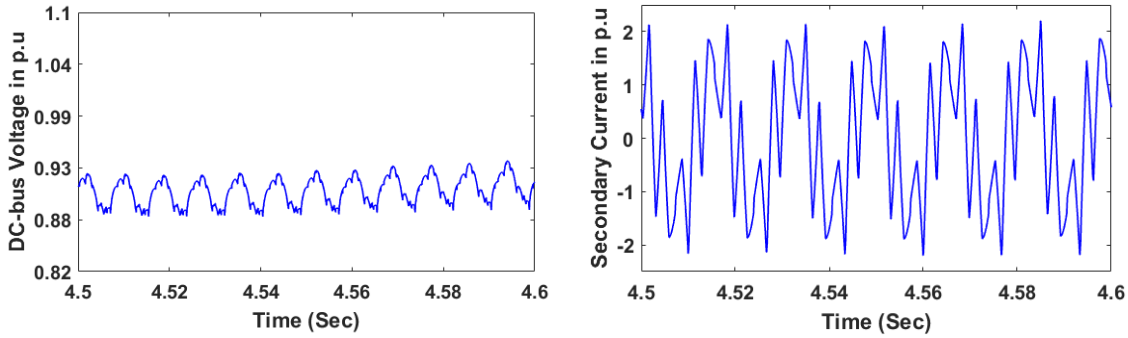
Another important aspect to be validated is the capability of the proposed control scheme to regulate the DC-bus voltage in case of voltage sag condition, either symmetric or asymmetric voltage sage. In case of asymmetric voltage sag, the proposed control scheme should be able to limit the current unbalance. Fig. 6.44 shows DC-bus voltage and secondary current at nominal conditions. At nominal conditions, the modulation index is set to one resulting in $180^o$ conduction of the IGBTs. At this condition, the DC-bus voltage is regulated to the given reference value at 0.93 pu as shown in Fig. 6.44a

Fig. 6.45 shows DC-bus voltage and secondary current at sag conditions. The modulation index decreases to reduce the fundamental voltage generated at the terminal of the front end to match the secondary voltage.




(a) DC-bus Voltage (b) Secondary Current

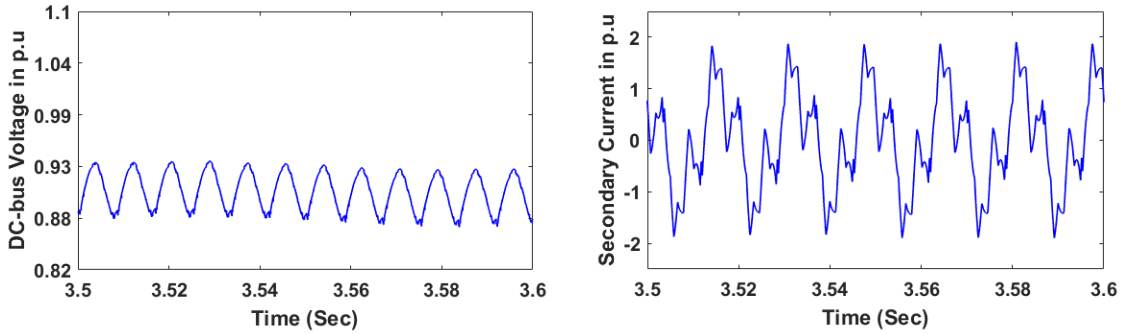
Fig. 6.44 Regeneration at Nominal Conditions.




(a) DC-bus Voltage (b) Secondary Current

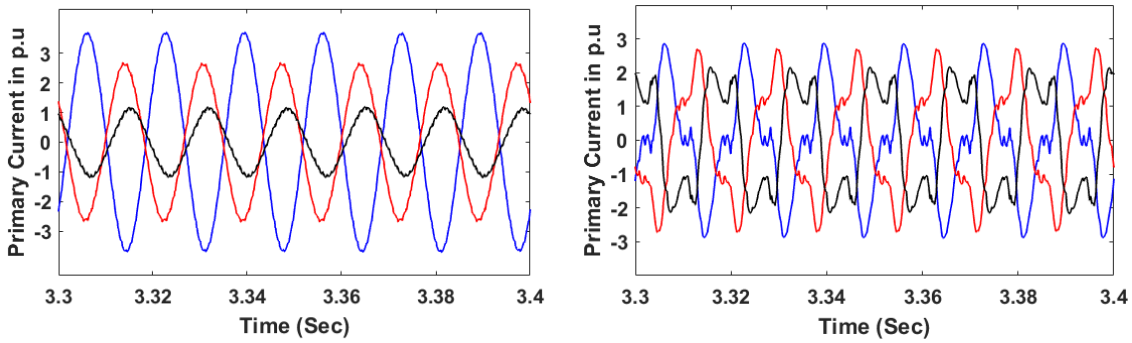
Fig. 6.45 Regeneration at Symmetric Sag Condition.

This reduction of the fundamental component of the front end terminal voltage is achieved through producing gating pattern based on the modulation index as shown in Fig. 6.29. Fig. 6.46 shows DC-bus voltage and secondary current at asymmetric sag conditions. Similar to the case in Fig. 6.45, the control has managed to regulate the DC-bus through setting the modulation index. Fig. 6.47 compares the primary current for the cases without and with the negative sequence compensator. The current unbalance in the latter case is lower.




(a) DC-bus Voltage (b) Secondary Current

Fig. 6.46 Regeneration at Asymmetric Sag Condition.




(a) Symmetrical Delay Angle (b) Asymmetric Delay Angle

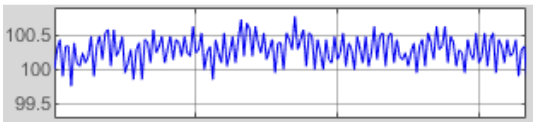
Fig. 6.47 Primary Current at Regeneration during Asymmetric Sag Condition.

**b) Experimental Validation**

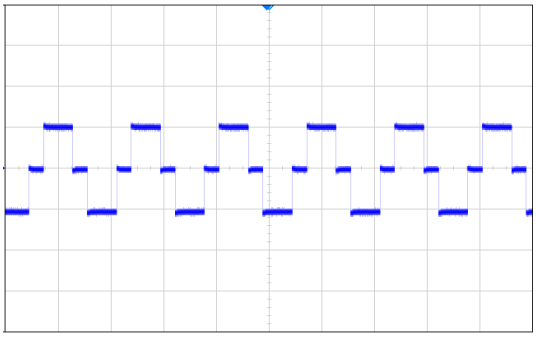
Experimental validation results for the proposed voltage angle under nominal and sag conditions are given in Fig. 6.48 to Fig. 6.50. Equivalent secondary inductance is about 4 mH in the front end. DC-bus voltage reference is set to 100 V. DC-bus voltage, front end input terminal voltage, and secondary current are shown respectively in Fig. 6.48. DC-bus voltage is regulated around 100 V as shown in Fig. 6.48a. Front end terminal voltage is quasi-square wave as shown in Fig. 6.48b.

Fig. 6.49 presents waveforms at about 0.7 p.u input voltage, and Fig. 6.50 presents waveforms at about 0.5 p.u input voltage. In both cases, the proposed control scheme has managed to regulate the DC-bus voltage to the reference value through manipulating the modulation index. In addition, Fig 6.49 and 6.50 show that as the regenerative power is kept the same, increasing the sag depth results in

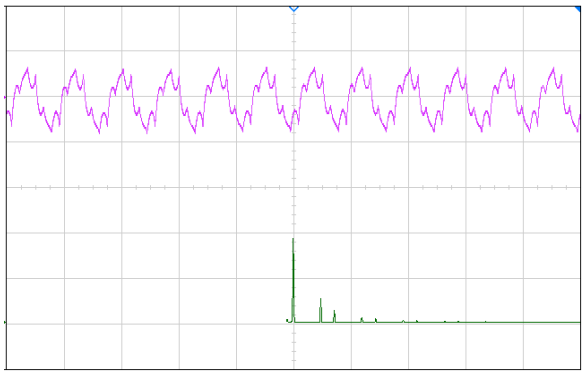
larger current peaks due to corresponding decrease in conduction time. Change of conduction time can be seen through comparing Fig. 6.49b and 6.50b.




(a) SCADA Result of DC-bus Voltage

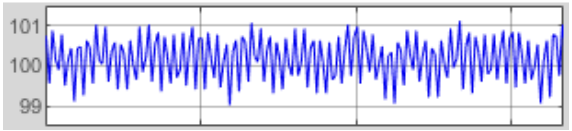


(b) FE Terminal Input Voltage
(100 V / div) (10 ms / div)

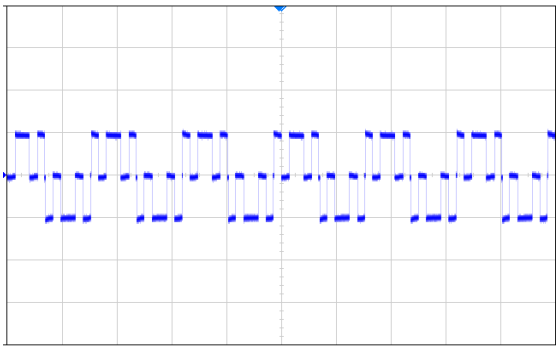


(c) Secondary Current
(10A / div)(20ms / div)( 60Hz FFT Center)

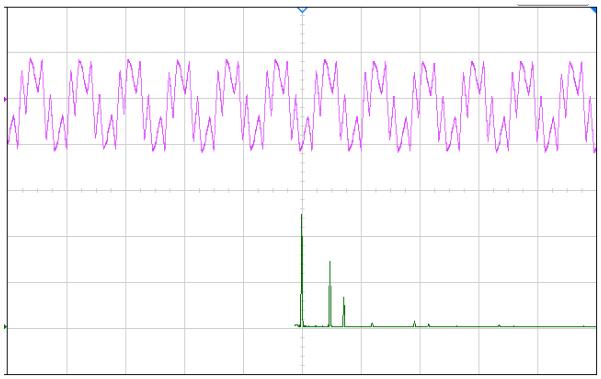
Fig. 6.48 Regeneration at Nominal Input Voltage.




(a) SCADA Result of DC-bus Voltage

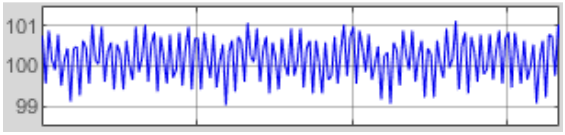


(b) FE Terminal Input Voltage
(100 V / div) (10 ms / div)

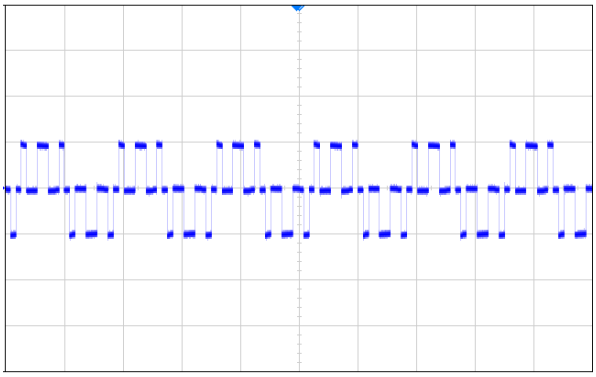


(c) Secondary Current
(10A / div)(20ms / div)( 60Hz FFT Center)

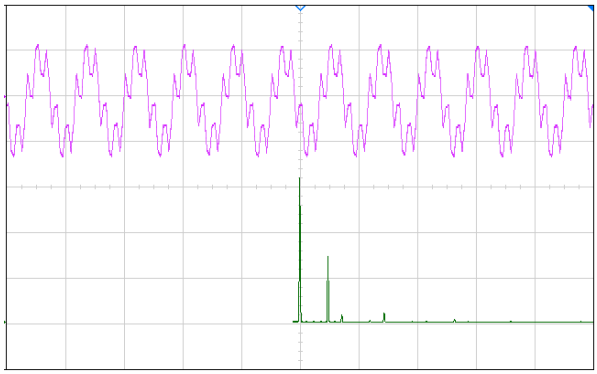
Fig. 6.49 Regeneration at Voltage Sag (0.7 p.u Input Voltage).




(a) SCADA Result of DC-bus Voltage



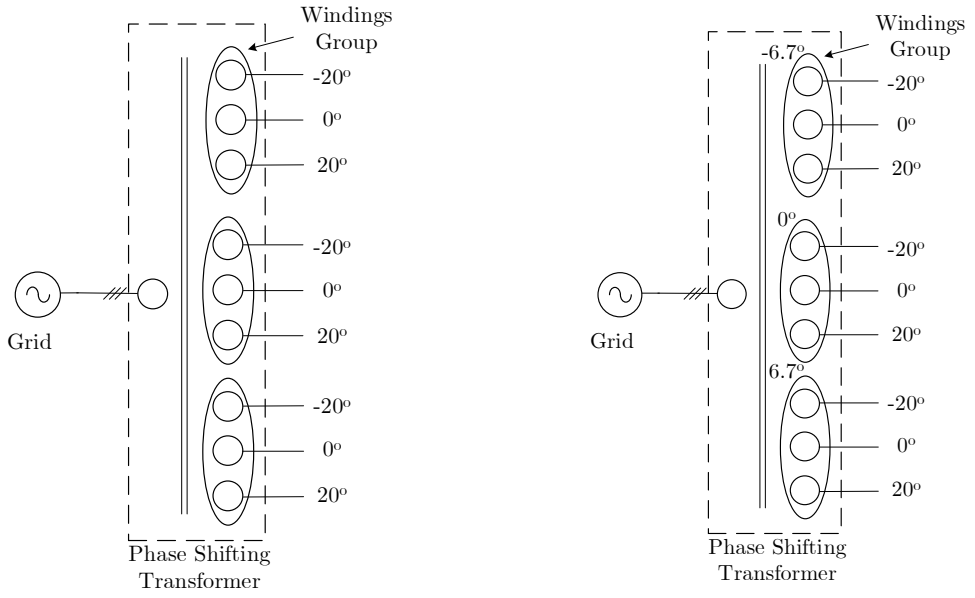
(b) FE Terminal Input Voltage
(100 V / div) (10 ms / div)



(c) Secondary Current
(10A / div)(20ms / div)( 60Hz FFT Center)

Fig. 6.50 Regeneration at Voltage Sag (0.5 p.u Input Voltage).

Another important aspect to validate is the harmonic cancellation at the transformer primary. In this experiment, the front ends have been operated in reactive power supply mode, which provides a less involving means to test harmonic cancellation at the primary of the transformer. The test has been conducted at nominal input voltage and under sag conditions. In addition, two windings configurations of the phase shifting transformers discussed in subsection 6.3.2 have been employed in the experiment as shown in Fig. 6.51. Fig. 6.51a shows the conventional 18- pulse phase shifting transformer. Fig. 6.51b shows a modified phase shifting transformer with phase shift between winding groups resulting in an equivalent 54-pulse transformer.

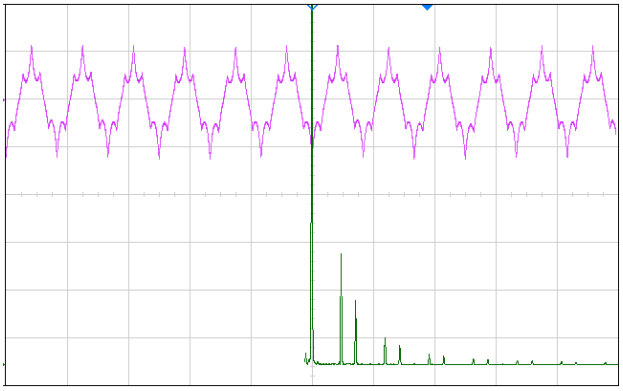



(a) 18-pulse (b) 54-pulse

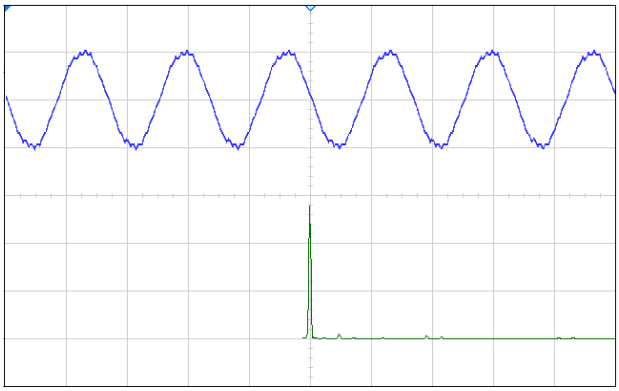
Fig. 6.51 Phase Shifting Transformer Configuration.

Fig. 6.52 shows secondary current and respective primary current under nominal conditions for the two transformer winding configurations. The secondary current FFT shows presence $17^{th}$ and $19^{th}$ harmonic components as shown in Fig. 6.52a, which are not cancelled out at the primary of the 18-pulse transformer configuration. Presence of $17^{th}$ and $19^{th}$ harmonic components at the primary current can be seen in Fig. 6.52b. These harmonic components are cancelled out in primary current in case of the 54-pulse configuration as shown in Fig. 6.52c.

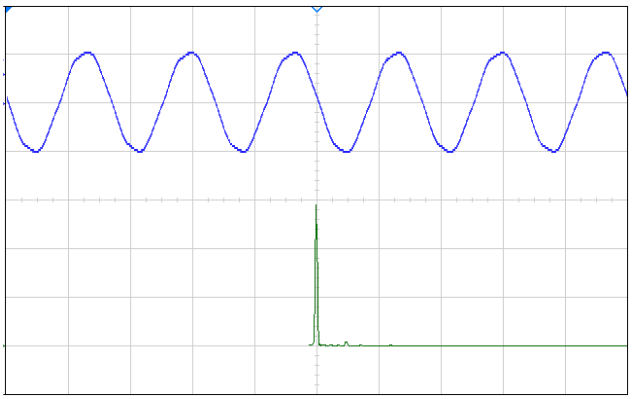
Fig. 6.53 to Fig. 6.55 show secondary and primary currents under nominal, 0.7 p.u, and 0.5 p.u input voltages for 54-pulse transformer. Results show the ability of the transformer to cancel low order harmonics at the primary in all conditions.



(a) Secondary Current
(100V / div)(10ms / div)( 60Hz FFT Center)

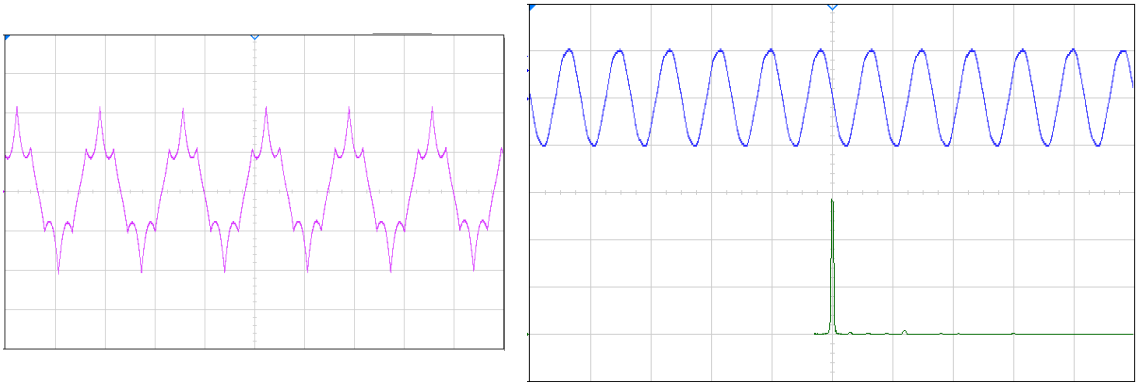


(b) Primary Current of the 18-pulse Transformer
(20A / div)(10ms / div)( 60Hz FFT Center)



(c) Primary Current of the 54-pulse Transformer
(20A / div)(10ms / div)( 60Hz FFT Center)

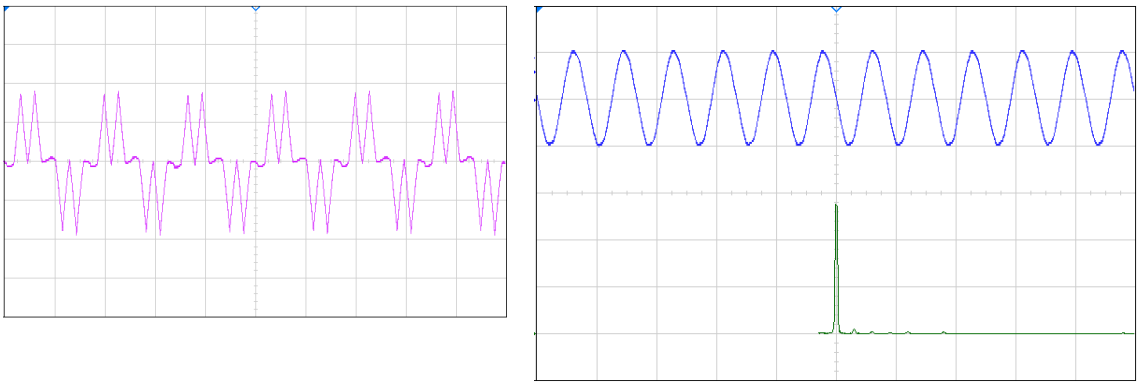
Fig. 6.52 Harmonic Cancellation at the Primary.



(a) Secondary Current (5A / div)(10ms / div)

(b) Primary Current of 54-pulse Transformer (20A / div)(20ms / div)( 60Hz FFT Center)

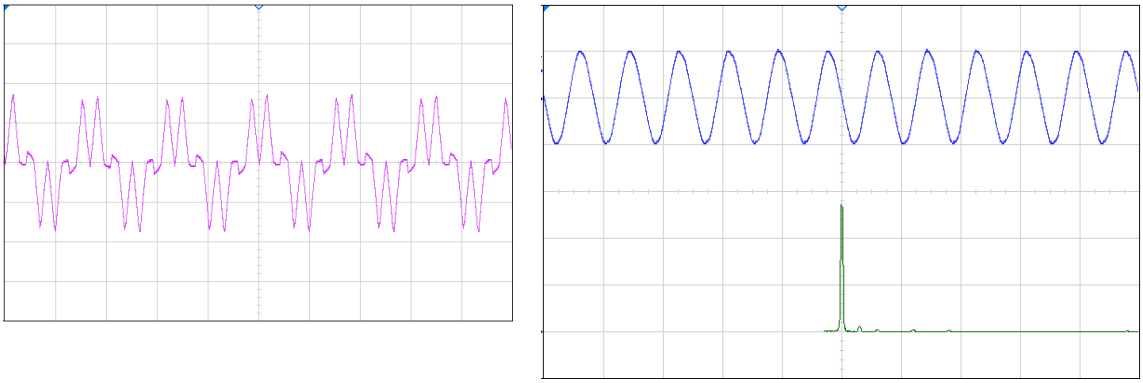
Fig. 6.53 Harmonic Cancellation at the Nominal Input Voltage.



(a) Secondary Current (7A / div)(10ms / div)

(b) Primary Current of 54-pulse Transformer (20A / div)(20ms / div)( 60Hz FFT Center)

Fig. 6.54 Harmonic Cancellation at the 0.7 p.u Input Voltage.



(a) Secondary Current (7A / div)(10ms / div)

(b) Primary Current of 54-pulse Transformer (20A / div)(20ms / div)( 60Hz FFT Center)

Fig. 6.55 Harmonic Cancellation at the 0.5 p.u Input Voltage.

## 6.6. Summary

To satisfy grid connection harmonic requirements and reduce filter size, PWM-based AFE use switching frequency up to 2 kHz to 4 kHz. This increases switching losses of power device leading to higher cycling temperature stresses on power devices. These stresses accelerate mechanical packaging degradation of power switches, which leads to power switches failures. To tackle this challenge, Chapter 6 proposes two front ends modulation and control schemes in which the FE is switched at grid or near grid switching frequency. It has been presented that significant reduction in losses, and so significant improvement in power modules lifetime has been achieved. In addition, there are other important system benefits such as reduction of per cell heat sink size and prevention of high frequency emissions into the grid that may excite resonance modes. The chapter proposed a delay angle-based and a voltage angle-based grid or near grid switching frequency FEs. Harmonic cancellation at the primary of the transformer under the proposed modulation schemes has been covered. In addition, dynamic performance under load change and the performance under input voltage disturbances of the proposed control schemes have been addressed. 9-cell CHB system simulation and experimental studies have validated the effectiveness and the performance of the proposed modulation and control schemes while achieving the desired objectives.

# Chapter 7

# Regenerative CHB with Reduced Sensor Count

## 7.1. Introduction

An important aspect to be considered is the number of additional sensors required by the conventional AFE control schemes. Typically, they employ AC voltage sensing for grid synchronization, current sensing for current control, and DC voltage sensing for DC-bus voltage regulation [34-42]. Scaling up these sensing requirements to n-cells per phase CHB drive results in a huge addition of circuitry in comparison to the DFE CHB topology. In addition, transmission of these additional measurement signals to a centralized control as in the case of DFE CHB is not

practical, therefore, cell based AFE controller implementation is the preferred option [34-42]. However, embedding additional sensing and control circuitry to the densely-packed power cell operating in harsh conditions such as elevated temperatures, compromises power cell's circuitry reliability [33, 59, 61, 77, 83, 84]. These possible reliability issues may be mitigated through larger size or higher cost power cell designs, which may not be desirable. Reducing the sensor count and employing a centralized control scheme with minimum modifications to the existing DFE CHB control scheme is of a huge benefit leading to improvement of system reliability and reduction system complexity [33].

The proposed new centralized control scheme with reduced sensor count is meant to address three main challenges:

1. Improvement of power cells reliability.
2. Reduction of power cell cost.
3. Providing the performance required to suit the demanding requirements of the motor drives.

## 7.2. Background

As explained in Chapter 2, the conventional AFE control scheme requires five to seven measurements per cell to perform the required control tasks [34-42]. Fig. 7.1 revisits the conventional AFE control system to highlight these measurements. These measurements are one DC-bus voltage for DC-bus voltage regulation, two or three AC-line currents for inner loop current control, and two or three AC-line voltages for grid synchronization and reactive power compensation. If a centralized control scheme is to be used likewise the DFE CHB; for n-cells per phase AFE CHB, large number of signals at high sampling rate need to be transmitted from cells to the centralized controller as shown in Fig. 7.2.

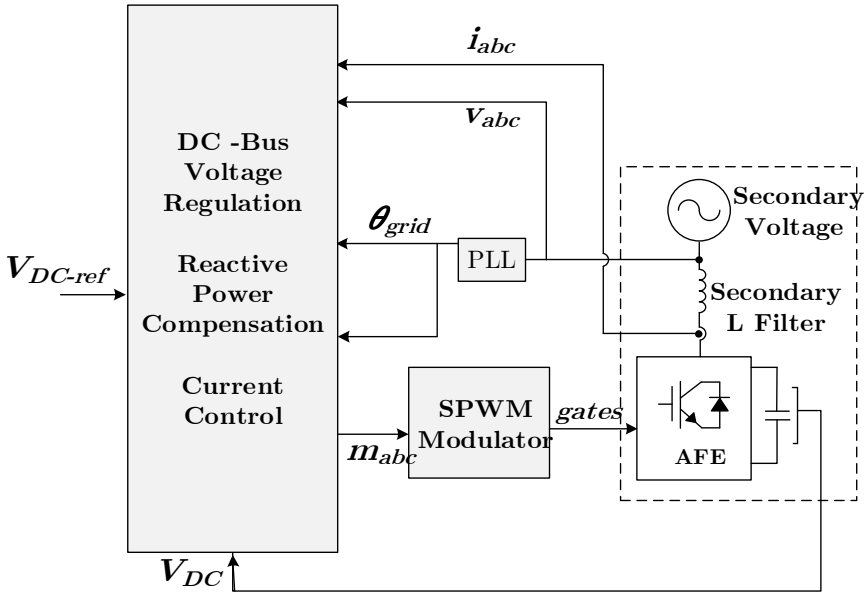



Fig. 7.1 Conventional AFE Control Scheme Block.

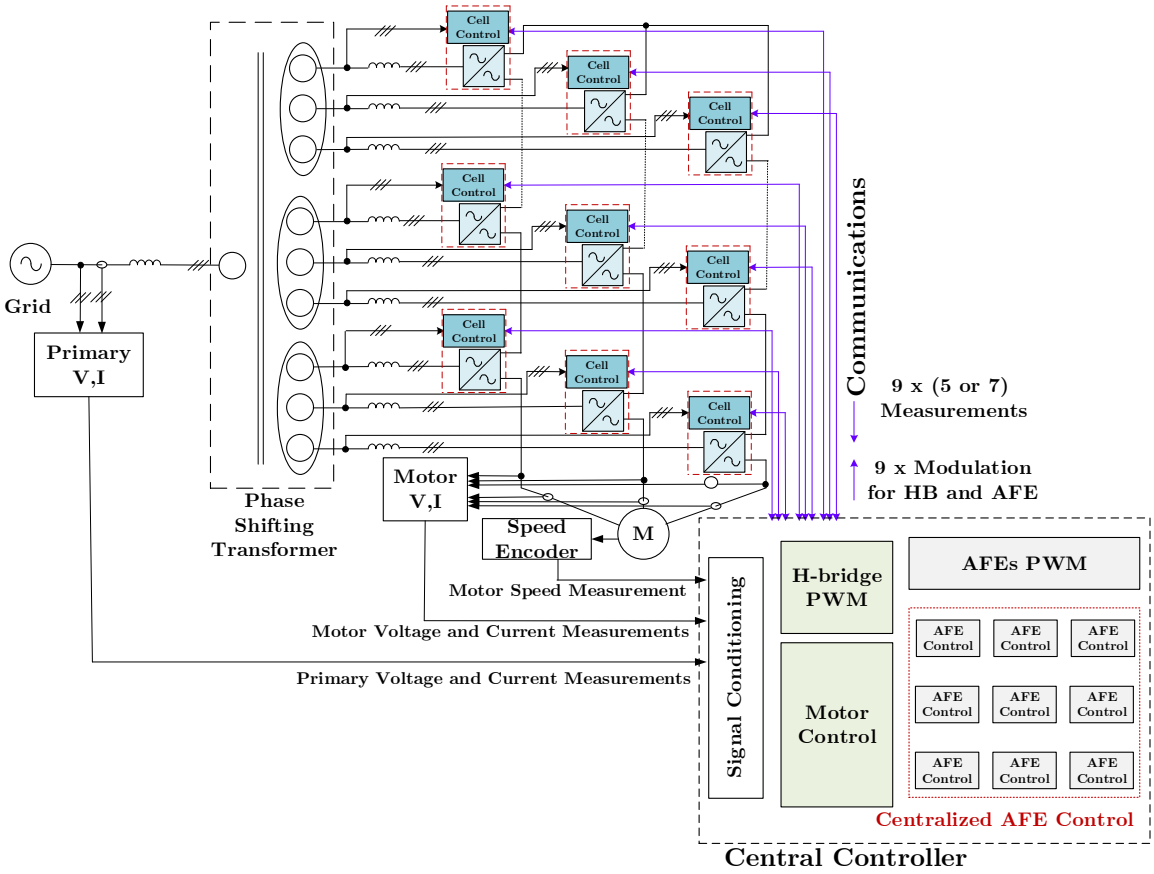



Fig. 7.2 AFE Centralized Control.

This large data transmission requirement makes implementing conventional AFE control in a centralized manner less preferable or even impractical for high n-cells per phase CHBs. A more preferable approach is to implement AFE control locally in power cells as shown in Fig. 7.3 [34-42]. This reduces the data transmission requirement near to what is required in the DFE CHB.

Furthermore, advanced AFE control schemes, similar to what has been proposed in Chapter 5, include feedforward signals from the motor controller.

These signals are transmitted to the power cells adding burden on the communication links. Still from communication links burden point of view, AFE local control is preferable.

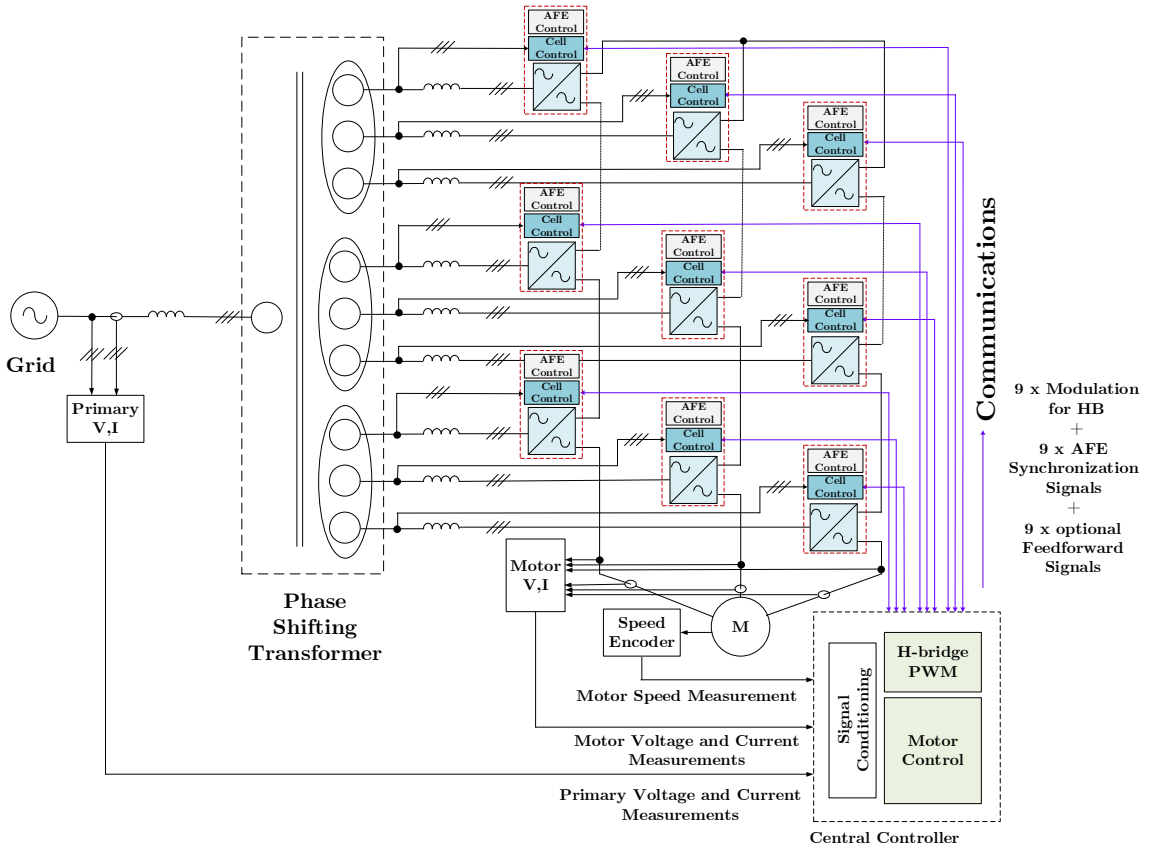



Fig. 7.3 AFE Local Control.

However, local implementation of AFE control requires adding extra sensing and control circuitry to the power cells. Already, DEF power cells are densely packed as shown in Fig. 7.4, and they are supposed to operate in harsh conditions due to elevated temperatures. Embedding extra circuitry to these power cells

exposes circuitry to high thermal and mechanical stresses [33, 77, 83, 84]. As discussed in section 3.4, these stresses challenge power cell circuitry reliability, and so, the drives system reliability. In order to tackle these challenges, new power cell designs for AFE CHB are required, which may not be desirable.


Fig. 7.4 WEG MVW3000 DFE Power Cell
(650 V, 140 A, 361 x 255 x 505 mm) [33].

Another important aspect to consider the compliance with grid connection current harmonic standard. Commonly, AFEs PWM switching frequency is set to 2 kHz to 4 kHz to reduce the size of L filters required (assuming only L filters are used in this case) [32, 34-38, 140]. However, from cost, size, and reliability perspectives it is desirable to keep the switching frequency less than 2 kHz while keeping the size of L filters as minimum as possible. In order to achieve this, it is proposed to perform PWM carrier shifting between the AFEs in the power cells [140]. One approach is to introduce $120°$ carrier phase shift between AFEs in different CHB phases as shown in Fig. 7.5 [140]. In order to implement this carrier

shift between AFEs in different power cells, a centralized synchronizer is required to transmit synchronization signals to the power cells. This is illustrated in Fig. 7.3 and in more details in Fig. 7.6. The quality and precision of these signals is crucial for correct AFEs carrier synchronization process. This adds a significant burden on the communication links between the centralized controller and the power cells.

A centralized AFE control scheme as shown in Fig. 7.2 allows the implementation of AFEs PWM carrier synchronization in the centralized controller. Fig. 7.7 illustrates the centralized AFEs PWM synchronization. It is similar to the H-bridges PWM synchronization and generation. In both cases, PWM signals are synchronized and generated in the centralized controller, then are transmitted through the communication links to the power cells.

It is a system design decision to select between transmitting the AFEs PWM synchronization signals to local PWM modulators in power cells, or synchronizing and generating AFEs PWM signals in the centralized control and transmitting the PWM signals to the AFEs. Both add burden on the communication links to the power cells and there is no clear advantage of one over the other in this regard.

Therefore, for AFEs, in order to realize the benefits offered by the centralized control scheme; the control scheme should rely on reduced sensor count.

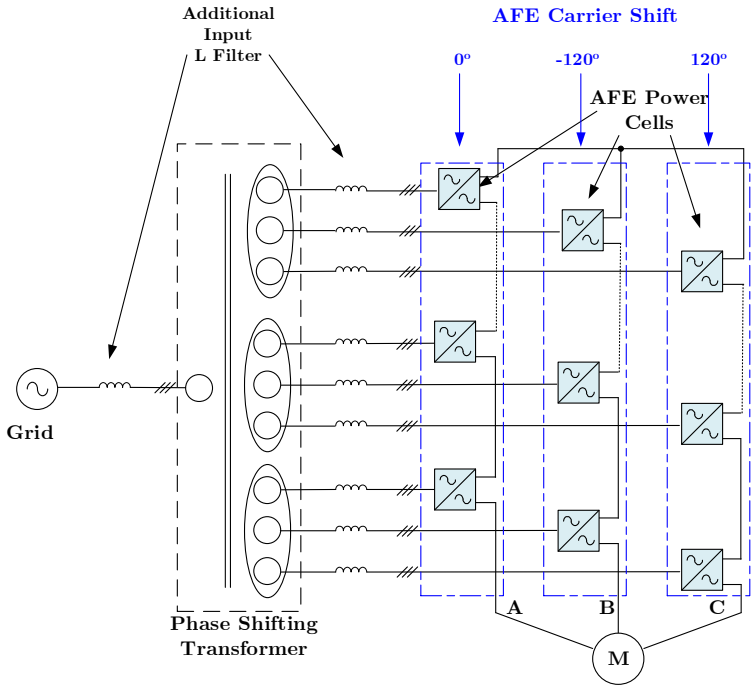



Fig. 7.5 AFE 120° Carrier Phase Shift [140].

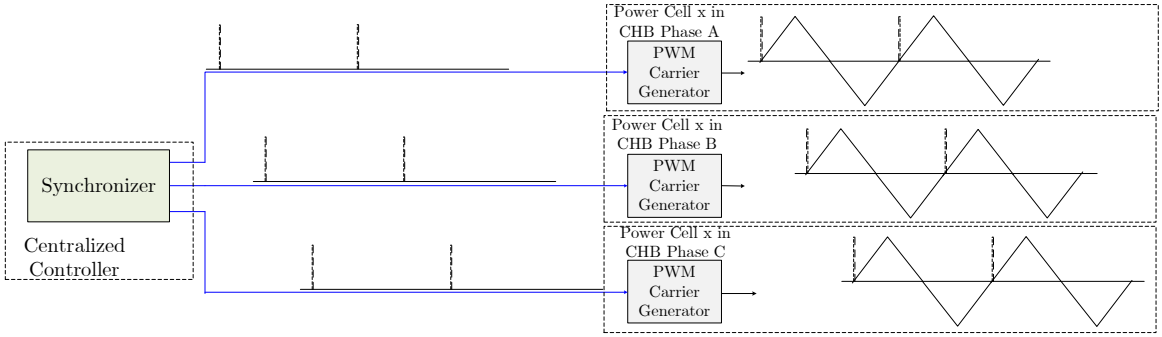



Fig. 7.6 Decentralized AFEs PWM synchronization (120° carrier shift).

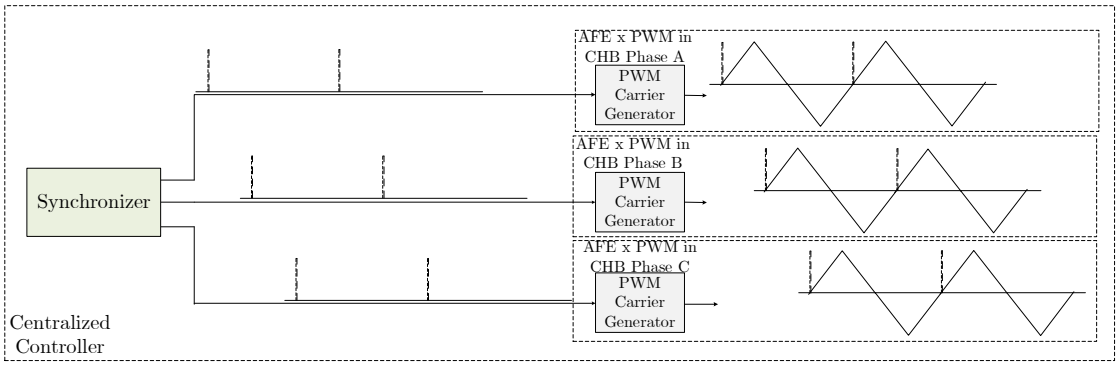



Fig. 7.7 Centralized AFEs PWM synchronization (120° carrier shift).

Regarding grid frequency switching front ends discussed in Chapter 6, beside the benefits they offer namely the improved IGBTs reliability and reduced cooling requirement; they provide other system advantages. For example, grid frequency switching front ends do not require gating synchronization among each other in comparison to the AFEs. Fig. 7.8 presents the grid or near grid frequency switching local control scheme. However, as illustrated in Chapter 6, different approaches for grid frequency switching front ends show the possibility of reducing the sensors count.

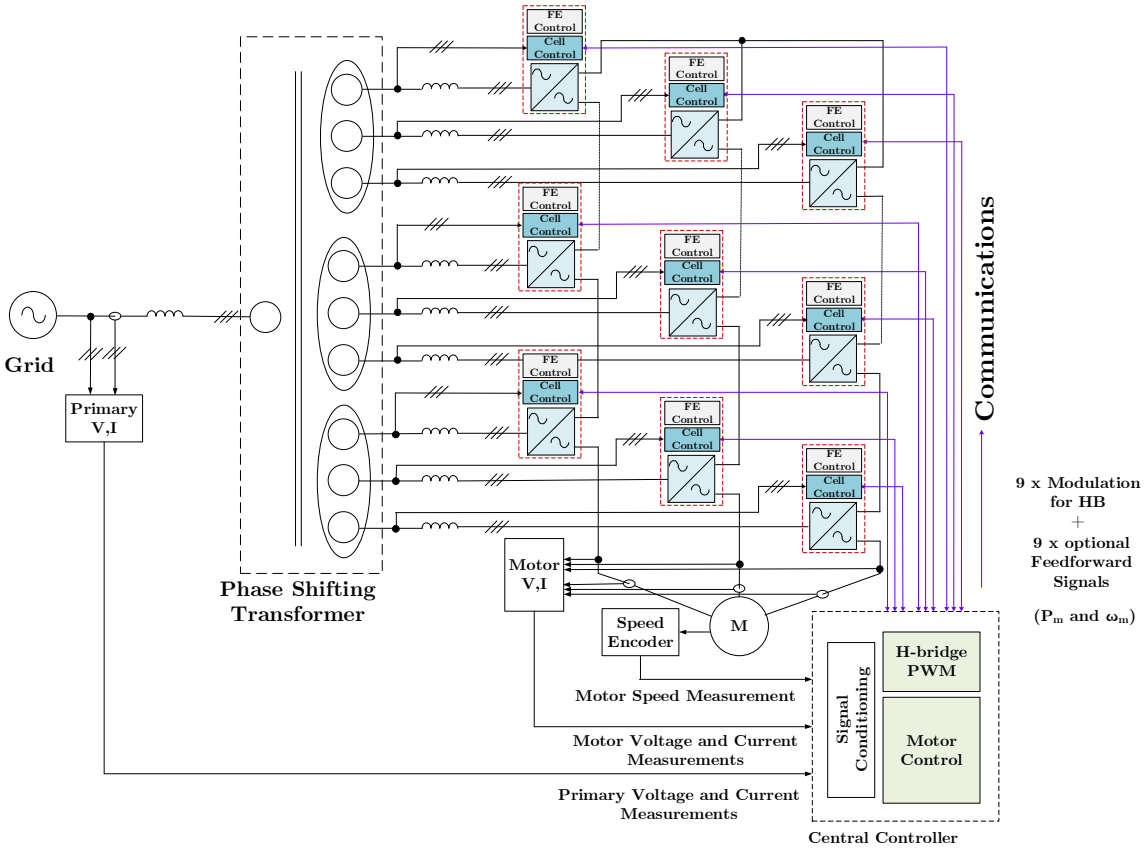



Fig. 7.8 Grid or Near Grid Frequency Switching Local Control.

Thus, adoption of centralized grid frequency switching front end control scheme with minimum modifications without adding burden on communication links to power cells is of significant potential compared to AFE counterpart. Fig. 7.9 shows a grid or near grid frequency switching centralized control.

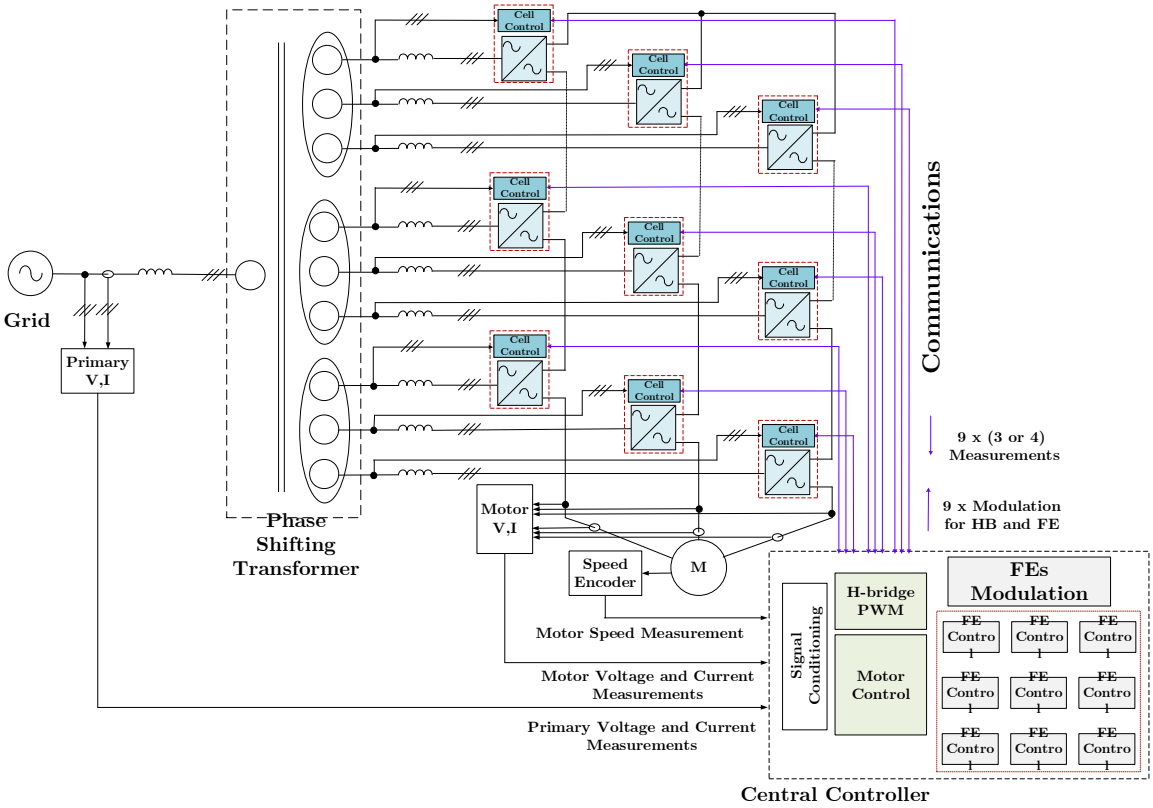



Fig. 7.9 Grid or Near Grid Frequency Switching Centralized Control.

Accordingly, in the search for cost effective front end, it is desirable to reduce sensor count and employ a centralized control scheme with minimum modifications to the existing DFE CHB power cells. This leads to huge improvement of reliability and reduction in complexity and cost. In the next section, centralized control

schemes with reduced sensor counts for both AFEs and grid or near grid frequency switching front ends are proposed.

## 7.3. Designing a New CHB Front End Control Scheme

Conventionally, the control system design philosophy behind previously discussed CHB front ends control schemes assume independent operation of the front ends. That is, they assume the front ends are interfaced to independent voltage supplies and the front ends regulate the DC-bus voltages under different loads with arbitrary response as illustrated conceptually in Fig. 7.10.

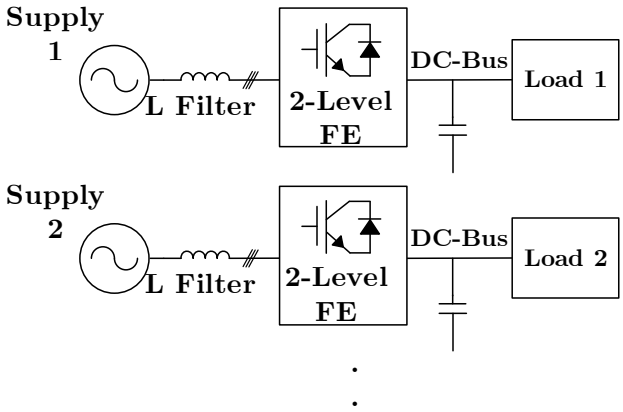
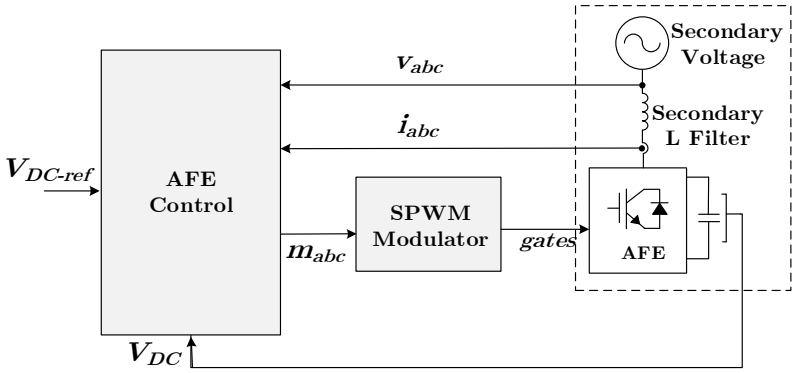


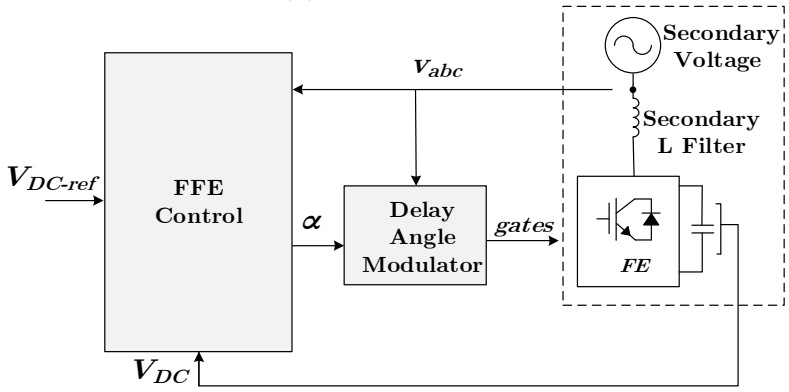

Fig. 7.10 Independent Operation Concept of CHB Front Ends.

Accordingly, the front ends control strategies rely on local measurements: input voltages, input currents, and DC-bus voltage to perform the required control tasks, while meeting the high performance requirements. Fig. 7.11 revisits some of these control strategies discussed previously. Local input voltage measurements are utilized by PLLs for grid synchronization and grid voltage magnitude calculation.

In addition, some control strategies utilize current measurements to achieve high performance control independent of load dynamics.




(a) AFE Control




(b) FFE Control

Fig. 7.11 Examples of Front End Control Schemes Based on Independent Operation Concept of CHB Front Ends.

### 7.3.1. Front Ends Input Voltage Measurements Elimination

From system perspective, the voltage supplies to which the front ends are interfaced are phase- and magnitude- related based on the phase shifting multi-winding transformer. Fig. 7.12 shows the CHB converter with front ends [34-42]. The voltage angles between windings are shown, where $\delta$ represents the secondary voltage angle

with respect to the primary. In principal, through the fixed voltages angles phase shift between windings, it is sufficient to determine the primary voltage angle to be able to estimate secondary voltages angles. In addition, secondary voltages magnitudes can be estimated from fixed turns ratio between the primary and secondary windings and the primary voltage measurement. Accordingly, secondary voltage measurements can be eliminated, while only relying on primary voltage measurements, which typically exist in CHB motor drives, for estimating secondary voltages angles.

Practically, transformer angles are not ideal. The tolerance in transformer angles may result in degradation in harmonic cancellation capability of the phase-shifting transformer at the primary especially for very low inductance systems. This is beyond the reach of the controller. However, from controller perspective, angles need not to be ideal for typical systems. For very low inductance cases, the performance of the control system is compromised. The estimating secondary voltages angles is illustrated in Fig. 7.13, where secondary voltages angles are expressed as follows:

$$\begin{aligned}
&\theta_{1A} = \theta_{grid} - 20°,\ \theta_{1B} = \theta_{grid} + 0°,\ \theta_{1C} = \theta_{grid} + 20° \\
&\theta_{2A} = \theta_{grid} - 20°,\ \theta_{2B} = \theta_{grid} + 0°,\ \theta_{2C} = \theta_{grid} + 20° \\
&\theta_{3A} = \theta_{grid} - 20°,\ \theta_{3B} = \theta_{grid} + 0°,\ \theta_{3C} = \theta_{grid} + 20°
\end{aligned} \tag{7.1}$$

These angles relations represent simple positive sequence model of phase shifting multi-winding transformer. This model is suitable for nominal symmetric primary voltage. However, practically, the incoming primary voltages may include sustained unbalance component; for instance, 5% unbalance where the voltage unbalance is expressed as follows:

$$\text{Voltage Unbalance} = \frac{\text{Maximum Deviation from the mean of } V_{ab}, V_{bc}, V_{ca}}{\text{The mean of } V_{ab}, V_{bc}, V_{ca}} \quad (7.2)$$

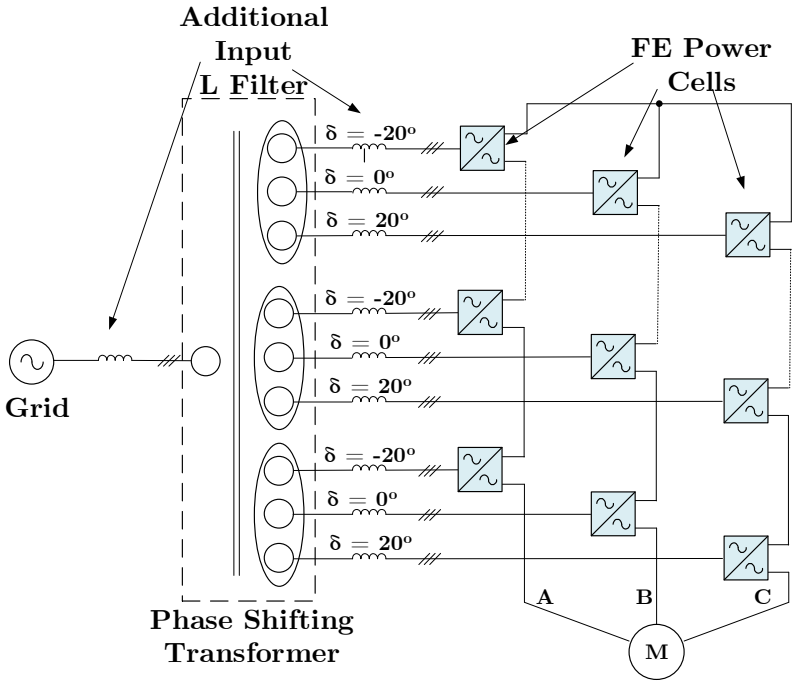



Fig. 7.12 Primary and Secondary Voltages Angles Relation.

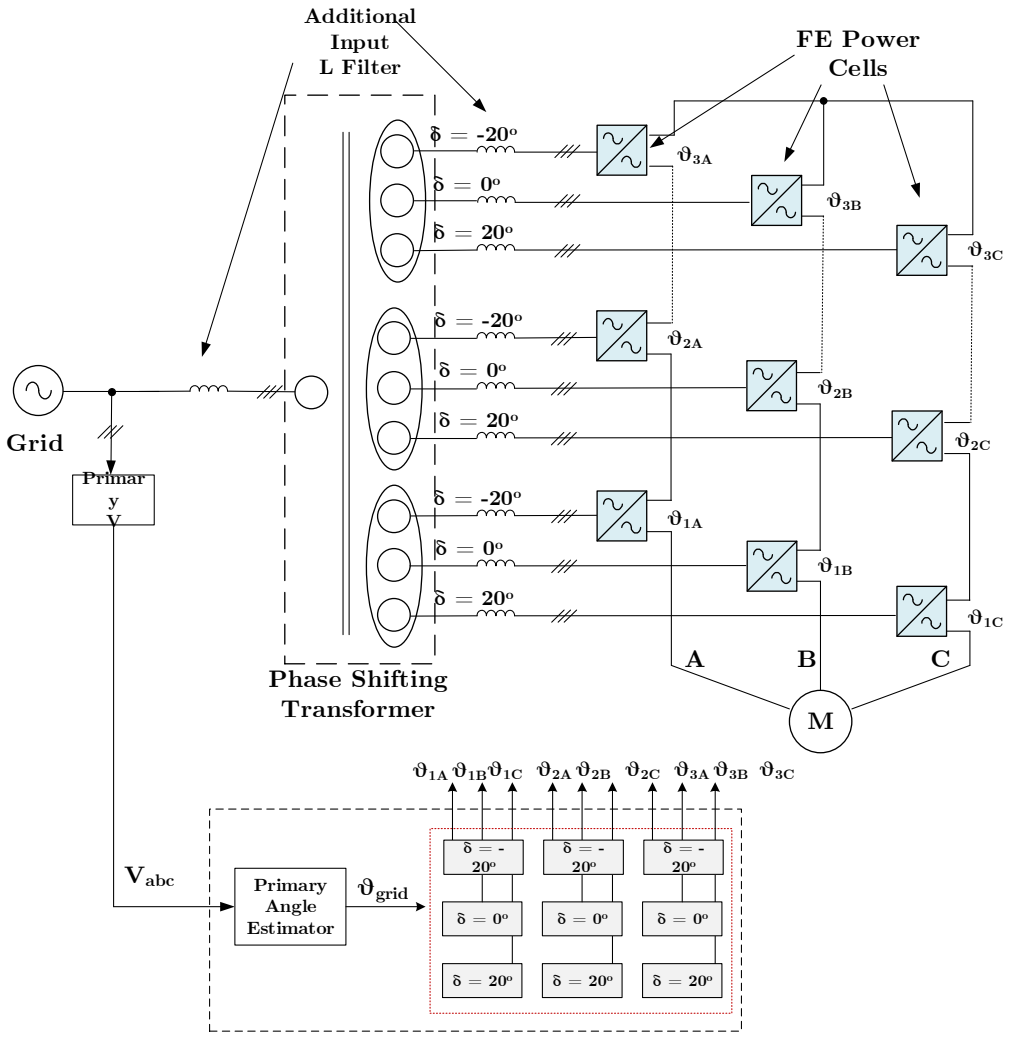



Fig. 7.13 Concept of Secondary Voltages Angles Estimation Based on Primary Voltage Measurement.

Moreover, the incoming primary voltages may suffer disturbances resulting in transient symmetric or asymmetric off-nominal voltage conditions. Fig. 7.14 shows primary voltage transient unbalance condition. Typically, asymmetric conditions are more frequent compared to symmetric conditions [156-163]. The phase shifting

transformer model shown in Fig. 7.13 is capable of estimating the angle of the positive sequence voltage component.

However, the primary unbalanced voltage can by decomposed into three sets of three-phase voltage as illustrated in the example shown in Fig. 7.15 [157]. The corresponding positive and negative sequence show up at the secondaries as shown in Fig. 7.16, while the zero sequence is blocked at the primary.

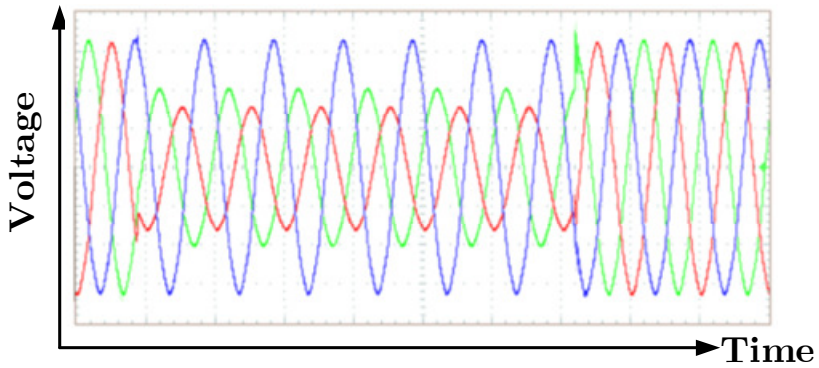



Fig. 7.14 Example for Primary Voltage Transient Unbalance Condition [157].

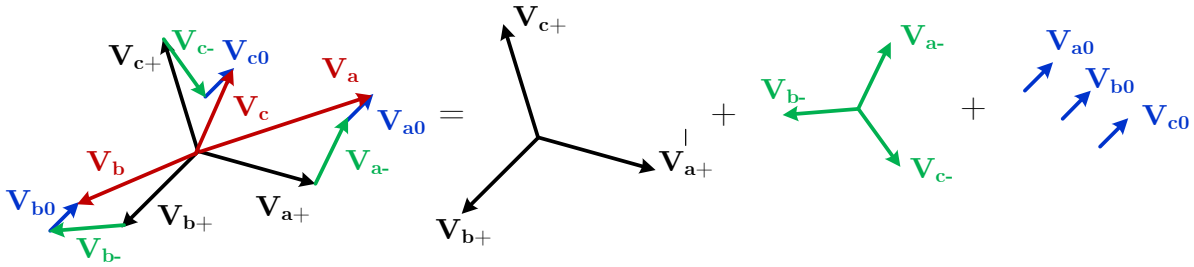



Fig. 7.15 Example for Primary Voltage Sequence Components Decomposition [157].

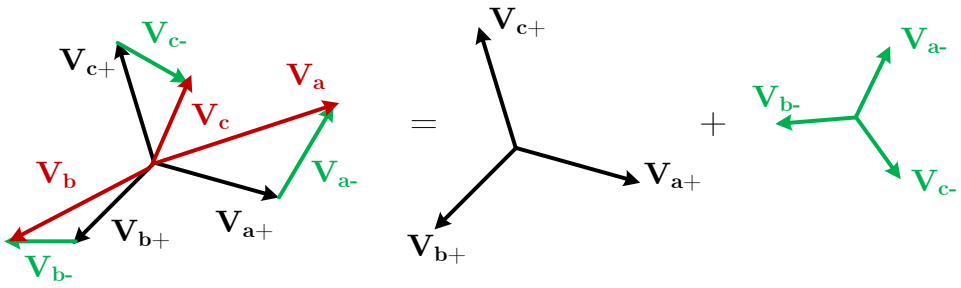
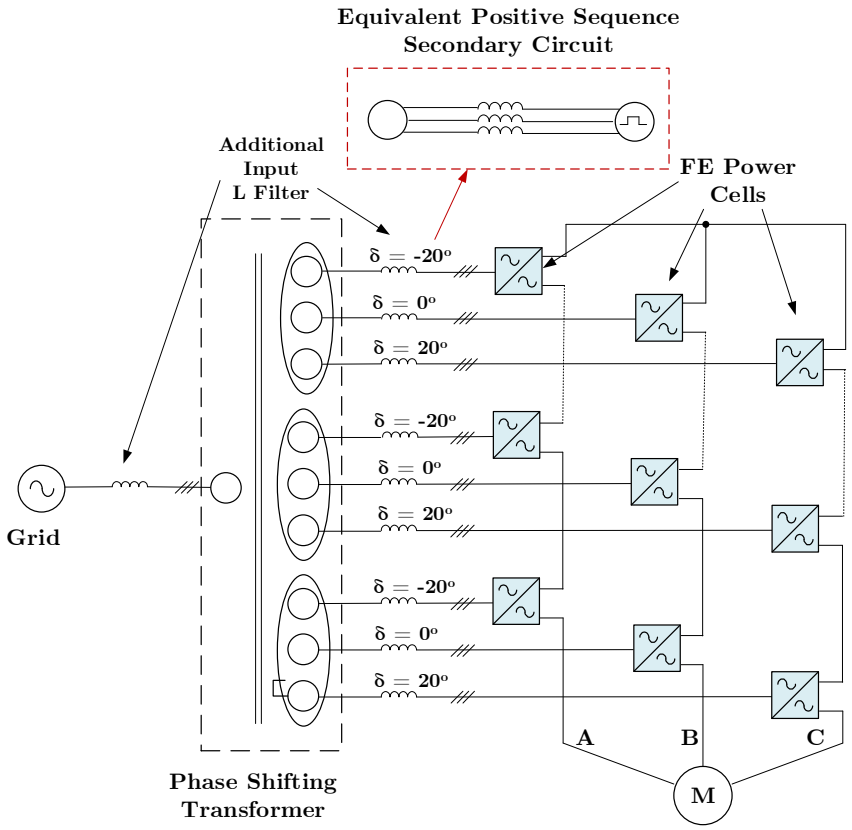


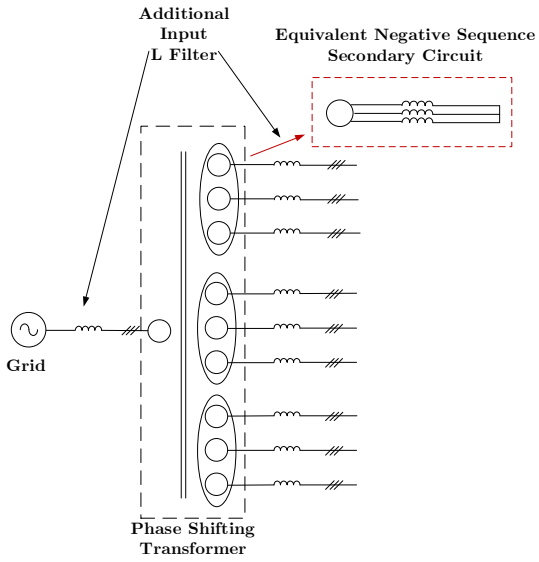

Fig. 7.16 Example for Reflected Secondary Voltage Sequence Components Decomposition at Middle Windings ($Cell_{2A}$, $Cell_{2B}$, $Cell_{2C}$) [157].

Under this condition, the response of a front end control scheme based on positive sequence voltage angle estimation can be illustrated as shown in Fig. 7.17. Fig. 7.17a shows the positive sequence equivalent circuit of the front ends. The front ends synthesize voltage at their AC terminals based on positive sequence voltage angle estimation performed through the positive sequence transformer model as shown in Fig. 7.13 to control the fundamental active and reactive power flows. However, under the positive sequence control, the front ends react as short circuits in response to input negative sequence voltage as illustrated in Fig. 7.17b. This results in significant uncontrollable negative sequence current flow in the secondary windings [164-170], which is reflected to the primary windings. This additional current component can cause overcurrent conditions and trigger system protection in case of transient input voltage disturbance, which is undesirable as it limits the ride through capability of the front ends and the converter as whole. Moreover, under sustained unbalanced input voltage condition, the corresponding

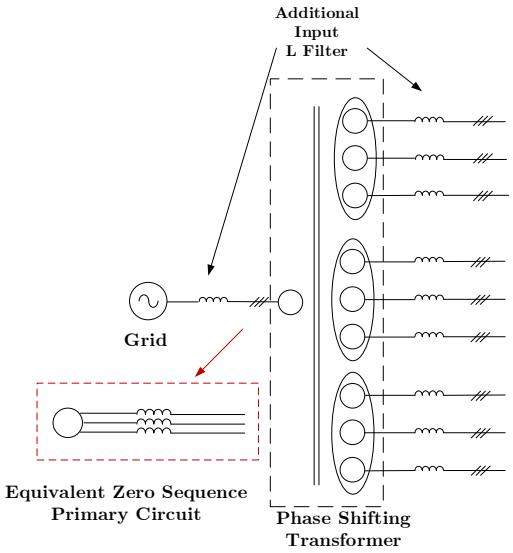
additional current component causes sustained overstress on the power devices, which may cause undesirable long-term reliability issues. In order to solve this issue, the front ends control require information about reflected positive and negative sequence voltage components at secondaries. Accordingly, the front ends are able to synthesize the required voltage at their AC terminals to control the fundamental active and reactive power flows, and to counteract the reflected negative sequence voltage to eliminate the negative sequence current component. The transformer model is required to estimate both the positive and negative sequence voltage angles instead of the model used in Fig. 7.13.




(a) Positive Sequence Equivalent Circuit




(b) Negative Sequence Equivalent Circuit




(c) Zero Sequence Equivalent Circuit

Fig. 7.17 Positive Sequence Controlled Front Ends Response to Asymmetric Primary Voltage Disturbance.

In principal, through the fixed voltages angles phase shift between windings, it is sufficient to determine the primary voltage angle to be able to estimate both secondary positive and negative sequence voltage angles as illustrated in Fig. 7.18. The voltage angles relation between the primary and the secondaries can be expressed as follows:

$$\begin{aligned}
&\theta_{\text{sec_1}A}{}^{+} = \theta_{grid}{}^{+} - 20°,\ \theta_{\text{sec_1}B}{}^{+} = \theta_{grid}{}^{+} + 0°,\ \theta_{\text{sec_1}C}{}^{+} = \theta_{grid}{}^{+} + 20° \\
&\theta_{\text{sec_2}A}{}^{+} = \theta_{grid}{}^{+} - 20°,\ \theta_{\text{sec_2}B}{}^{+} = \theta_{grid}{}^{+} + 0°,\ \theta_{\text{sec_2}C}{}^{+} = \theta_{grid}{}^{+} + 20° \\
&\theta_{\text{sec_3}A}{}^{+} = \theta_{grid}{}^{+} - 20°,\ \theta_{\text{sec_3}B}{}^{+} = \theta_{grid}{}^{+} + 0°,\ \theta_{\text{sec_3}C}{}^{+} = \theta_{grid}{}^{+} + 20°
\end{aligned} \tag{7.3}$$

$$\begin{aligned}
&\theta_{\text{sec_1}A}{}^{-} = \theta_{grid}{}^{-} + 20°,\ \theta_{\text{sec_1}B}{}^{-} = \theta_{grid}{}^{-} - 0°,\ \theta_{\text{sec_1}C}{}^{-} = \theta_{grid}{}^{-} - 20° \\
&\theta_{\text{sec_2}A}{}^{-} = \theta_{grid}{}^{-} + 20°,\ \theta_{\text{sec_2}B}{}^{-} = \theta_{grid}{}^{-} - 0°,\ \theta_{\text{sec_2}C}{}^{-} = \theta_{grid}{}^{-} - 20° \\
&\theta_{\text{sec_3}A}{}^{-} = \theta_{grid}{}^{-} + 20°,\ \theta_{\text{sec_3}B}{}^{-} = \theta_{grid}{}^{-} - 0°,\ \theta_{\text{sec_3}C}{}^{-} = \theta_{grid}{}^{-} - 20°
\end{aligned} \tag{7.4}$$

In addition, secondary positive and negative voltages magnitudes can be estimated using fixed turns ratio between the primary and secondary windings, the primary positive sequence voltage, and the primary negative sequence voltage, where

$$\left|V_{\text{sec}\_ij}\right|^{+} = N_t * \left|V_{pri}\right|^{+}, \quad \text{i} \in \{1,2,3\} \text{ and } \text{j} \in \{\text{A,B,C}\} \tag{7.5}$$

$$\left|V_{\text{sec}\_ij}\right|^{-} = N_t * \left|V_{pri}\right|^{-}, \quad \text{i} \in \{1,2,3\} \text{ and } \text{j} \in \{\text{A,B,C}\} \tag{7.6}$$

, where $N_t$ is the turns ratio.

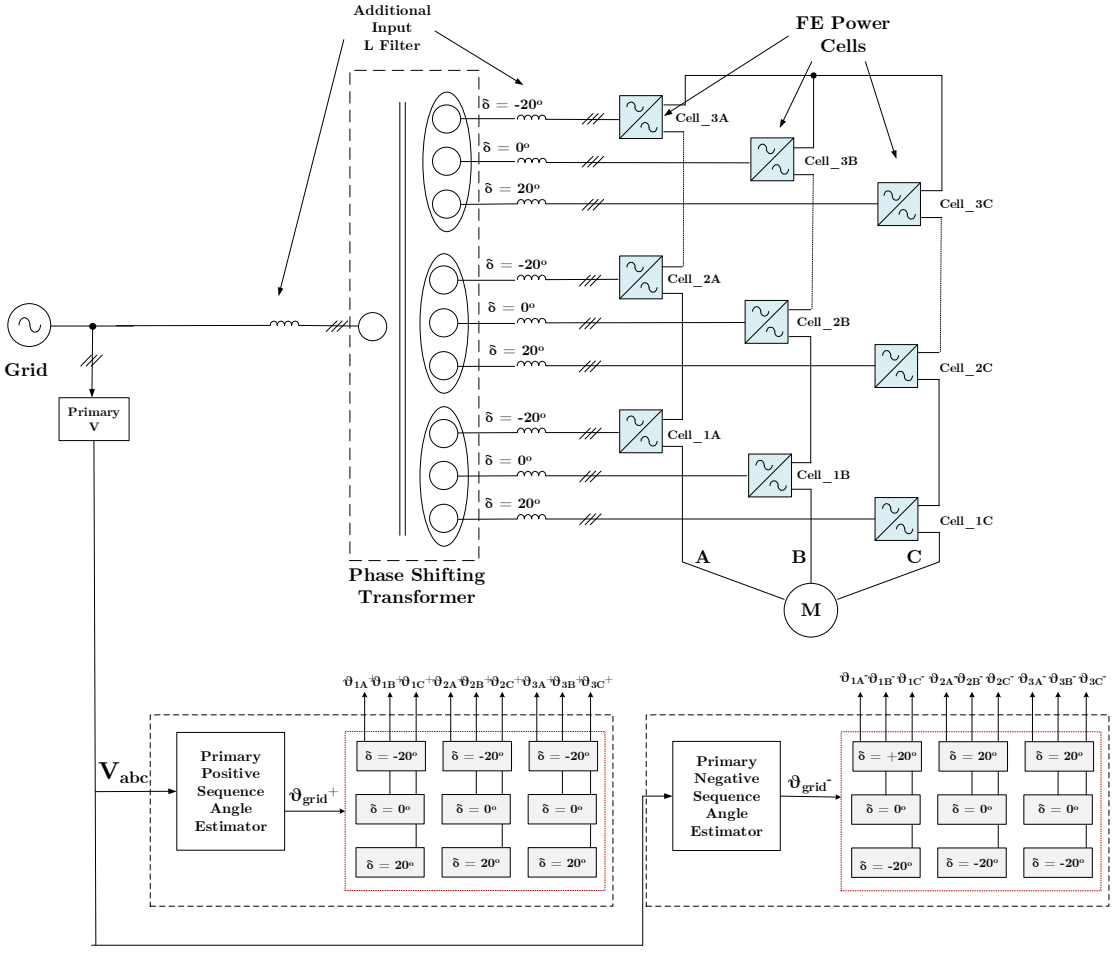



Fig. 7.18 Concept of Secondary Positive and Negative Voltages Angles Estimation Based on Primary Voltage Measurement.

Fig. 7.19 shows a proposed realization of a centralized secondary voltages estimator based on primary voltage measurements and transformer model. It consists of a positive sequence PLL, a negative sequence PLL, a positive sequence transformer angle model, a negative sequence transformer model, and additional secondary voltage waveform generator per cell if required. The positive sequence PLL provides the primary positive sequence voltage angle signal $\theta_{grid}^{+}$ and magnitude of the primary positive sequence voltage $\left|V_{pri}\right|^{+}$. The negative sequence PLL provides the primary negative sequence phase angle $\theta_{grid}^{-}$ and magnitude of the negative sequence primary voltage $\left|V_{pri}\right|^{-}$. The positive sequence transformer model models the positive sequence magnitude and angle relationship of phase shift transformer. Based on Eqns. 7.3 and 7.5, it estimates secondary positive sequence voltage magnitudes $\left|V_{\text{sec}_ij}\right|^{+}$and secondary positive sequence angles $\theta_{\text{sec}\_ij}^{+}$ given the primary positive sequence voltage magnitude and angle. The negative sequence transformer model models the negative sequence magnitude and angle relationship of phase shift transformer. Based on Eqns. 7.4 and 7.6, it estimates secondary negative sequence voltage magnitudes $\left|V_{\text{sec}_ij}\right|^{-}$and secondary negative sequence angles $\theta_{\text{sec}\_ij}^{-}$ given the primary negative sequence voltage magnitude and angle. Some front ends control schemes require the estimated secondary voltage in the

form of voltage waveform instead of voltage magnitude and angle. In this case, secondary voltage waveform generators per cell as shown in Fig. 7.19 are employed to produce secondary voltage waveforms $V_{an\_ij}, V_{bn\_ij}, V_{cn\_ij}$ based on the estimated secondary voltage positive and negative sequence magnitudes and angles. Fig. 7.20 illustrates the detailed structure of the waveform generator. It consists of positive and negative sequence voltage waveform generators. The total voltage waveform is calculated as the addition of the two sequence components.

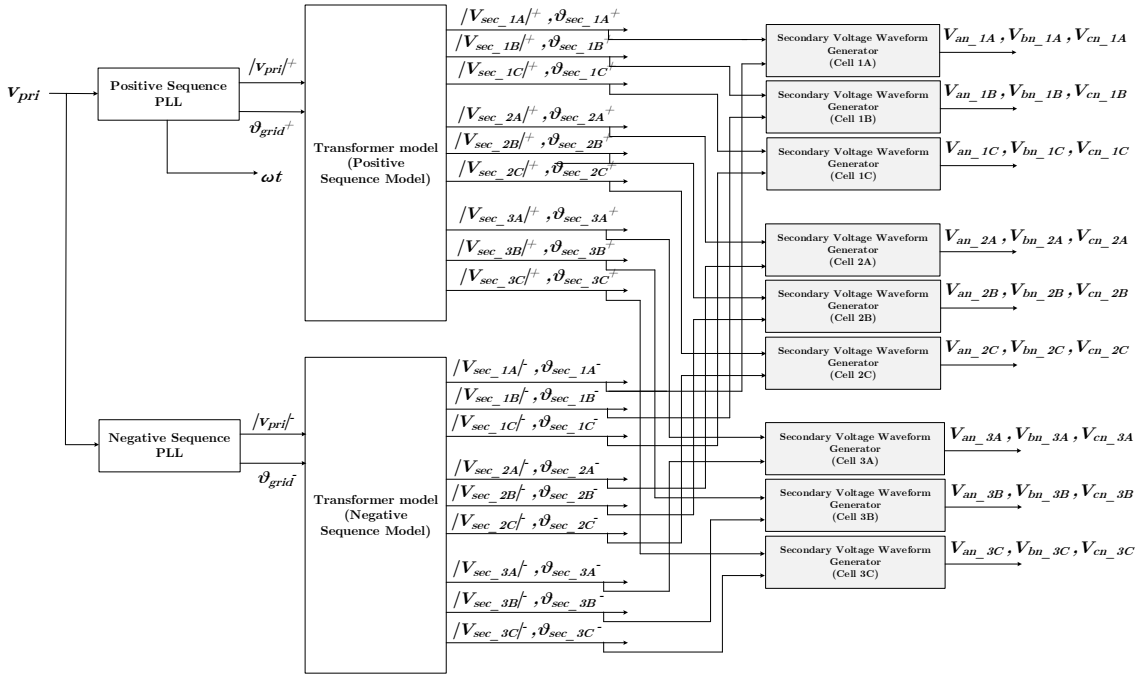



Fig. 7.19 Proposed Centralized Secondary Voltages Estimator.

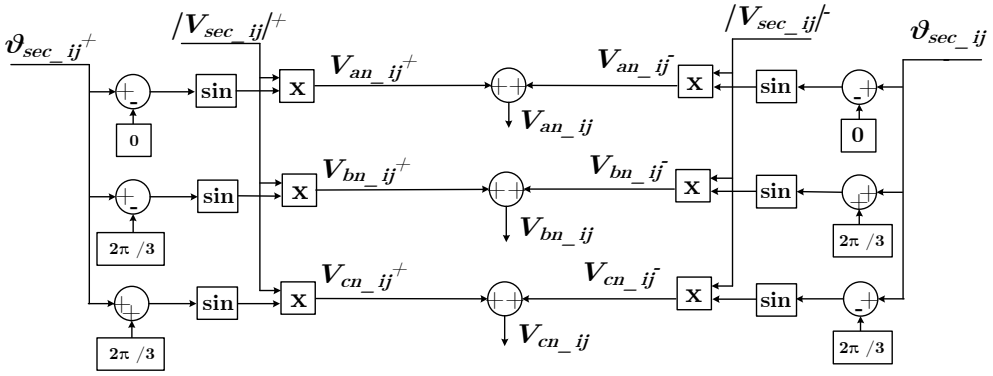



Fig. 7.20 Secondary Voltages Generator.

### 7.3.2. Elimination of Current Measurements from Front Ends

In Fig. 7.10, the conventional control system design philosophy behind CHB front ends control schemes assumes independent operation of the front ends, in which the front ends regulate DC-bus voltages under different loads with arbitrary response. In order to perform the control objectives while meeting the dynamic performance requirements, some front ends control strategies as shown in Fig. 7.11a rely on input front end current [34-43]. However, from system point of view, front ends in a CHB converter does not operate independently. In fact, the loading that the front ends see on their DC-bus is similar as shown in Fig. 7.21, where:

$$P(t) = -\left( 1/N_{Cells} \right) P_{motor}(t) \tag{7.7}$$

, and $N_{Cells}$ is the number of cells in the CHB converter. In addition, the load response is dictated by the motor control algorithm.

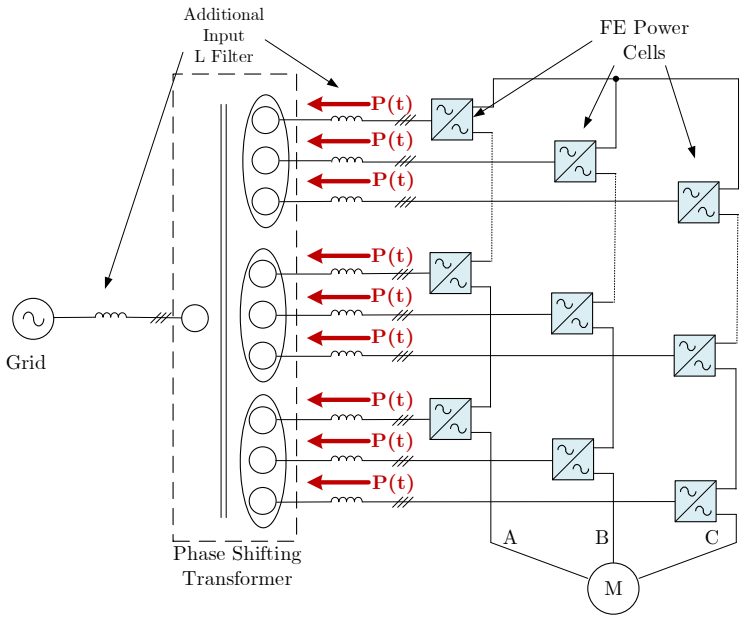



Fig. 7.21 Power Flow Distribution in the CHB Converter.

A widely employed motor control algorithm used in CHB drive is the FOC algorithm as presented in Chapter 2. In order to achieve high performance AC machines control, the concept behind the FOC control for AC machines is to mimic the DC machines control, which have two separate windings currents: the armature and field, to control magnetic flux and torque independently [171-172]. In AC machines, the stator current affects both the flux and the torque of the AC machine. Field oriented control is meant to provide means to decouple the manipulation of the flux and the torque of the AC machine. Several variants of field oriented control algorithms exist [171-172]. For the sake of the discussion, Fig.7.22 presents indirect FOC as one of these variants [171-172]. It includes speed controller that provides the torque reference, torque controller that provides the torque-controlling current

reference, flux controller that provides the flux-controlling current reference, current controller to provide the modulation indices to the SPWM modulator. In addition, the controller includes a motor model to estimate the orientation angle based on which the motor currents are transferred and decomposed. In general, FOC algorithms involve a current control loop in which the measured motor current is decomposed into flux-controlling and torque-controlling components.

Typically, regenerative applications such as cranes and conveyors require high performance motor, in contrast to applications such as fans and pumps. Therefore, commonly CHB converters assigned to the regenerative application employ motor control algorithms based on FOC [29-35]

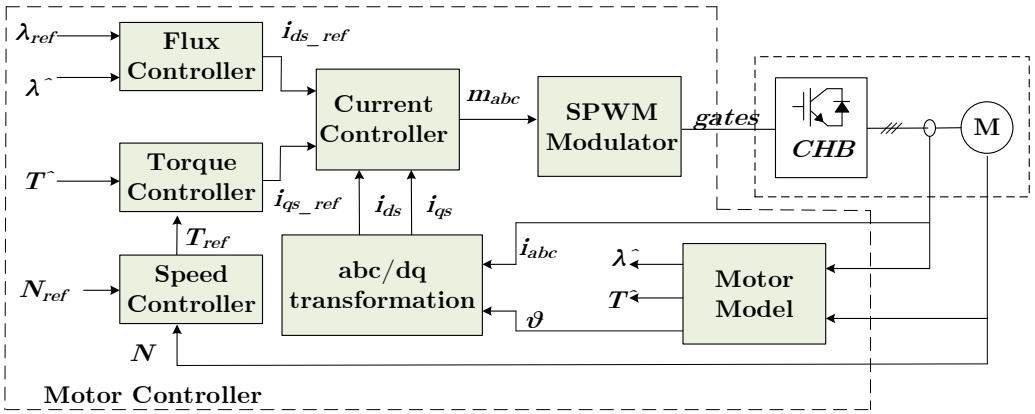



Fig. 7.22 Indirect FOC [171-172].

In CHB converters, high performance motor controller dictates the loading dynamics on DC-buses. Fig. 7.23 presents CHB converter with current-based controllers for both motor side and the front ends side to control power cell input and output currents. However, given the current controlled output, it is sufficient

to rely on voltage-based front end control for DC-bus voltage regulation while achieving the required dynamic performance. Removing current sensors may result in an unsatisfactory front end current response under severe voltage sags especially for low inductance system. This compromises between cost and performance under supply dependent events. This control strategy is illustrated in Fig. 7.24.

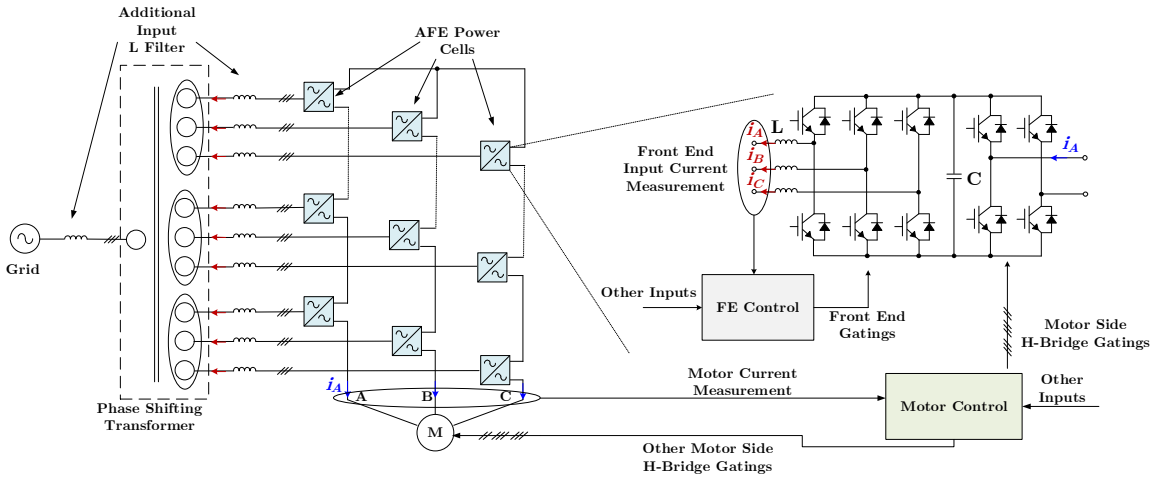



Fig. 7.23 Current-based Controllers for Both Motor Side and Front Ends Side.

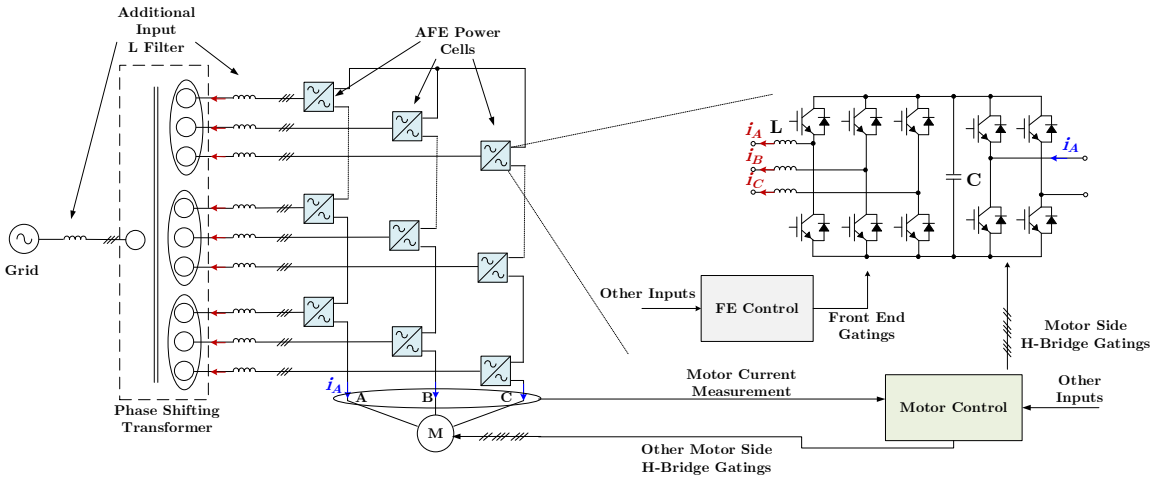



Fig. 7.24 Current-based Controller for Motor Side and Voltage–based Controller for Front Ends Side.

A proposed front end control scheme to replace the one in Fig. 7.11a after the front end input current sensors elimination is shown in Fig. 7.25. The proposed controller includes a DC-bus voltage controller, active power controller, waveform generator and negative sequence compensator, and SPWM modulator. The controller receives the respective positive and negative sequence voltage magnitudes $\left|V_{\text{sec}\_ij}\right|^{+}$ and $\left|V_{\text{sec}\_ij}\right|^{-}$, and angles $\theta_{\text{sec}\_ij}{}^{+}$ and $\theta_{\text{sec}\_ij}{}^{-}$, which are estimated based on primary voltage measurements and the transformer model. The DC-bus voltage controller and the active power controller are similar to the structures proposed in 6.4.2. The voltage waveform generator and negative sequence compensator is presented in Fig. 7.26. It takes as inputs the positive and negative sequence voltage magnitudes $\left|V_{\text{sec}\_ij}\right|^{+}$ and $\left|V_{\text{sec}\_ij}\right|^{-}$, the angles $\theta_{\text{sec}\_ij}{}^{+}$ and $\theta_{\text{sec}\_ij}{}^{-}$, the DC-bus voltage reference $V_{DC\_ref}$, and the power angle $\delta$ as inputs to generate modulation signal $m_{abc}$. This control strategy is meant for DC-bus voltage regulation. However, some front end control strategies such as the one proposed in Chapter 5 employs front end input current sensing to perform control tasks and not only the DC-bus voltage regulation. For these control strategies front ends input current measurements are required, while front input voltage measurements can be eliminated as discussed in the previous subsection.

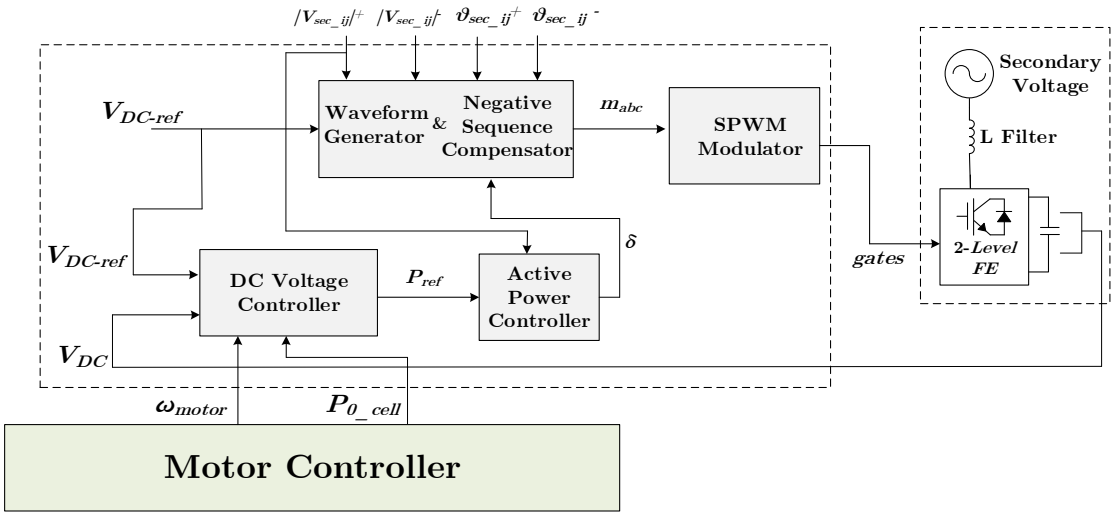



Fig. 7.25 Proposed Voltage-based AFE Control.

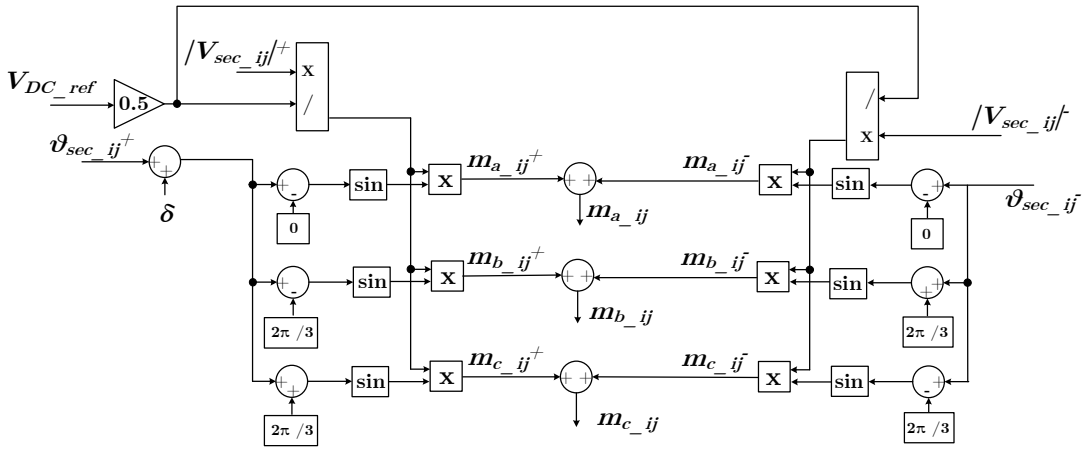



Fig. 7.26 Proposed Waveform Generator and Negative Sequence Compensator.

## 7.4. Proposed Centralized Front End Control Schemes

In this section, three proposed centralized control schemes are presented to incorporate the front ends control schemes discussed previously with partial or full sensor reduction depending on the specifics of the front ends control schemes.

### 7.4.1. Proposed Centralized Control Scheme with AFE Current Control and Eliminated Secondary Voltage Sensors

Fig. 7.27 presents a proposed centralized control scheme for AFEs with current control. Power cells input currents and DC-bus voltages information are transmitted to the centralized control through the communication links. AFE PWM gating signals are generated and synchronized before being transmitted back to the power cells through the communication links. The details of the control tasks and interface signals of the centralized control scheme is illustrated in Fig. 7.28. In order to eliminate the need for secondaries voltage sensors as discussed in the previous section, primary PLLs and transformer model are used to estimate the secondary voltages magnitudes and angles. Then these estimated signals are sent to the AFE controller instances.

Fig. 7.29 and Fig. 7.30 present two possible variants for current controlled AFE controllers: conventional current controlled AFE, and current controlled AFE with pulsating power flow capability. Despite the system merits of the centralized control scheme, current controlled AFEs require sending secondaries currents through the communication links as shown in Fig. 7.28, which is disadvantageous as extra links are required.

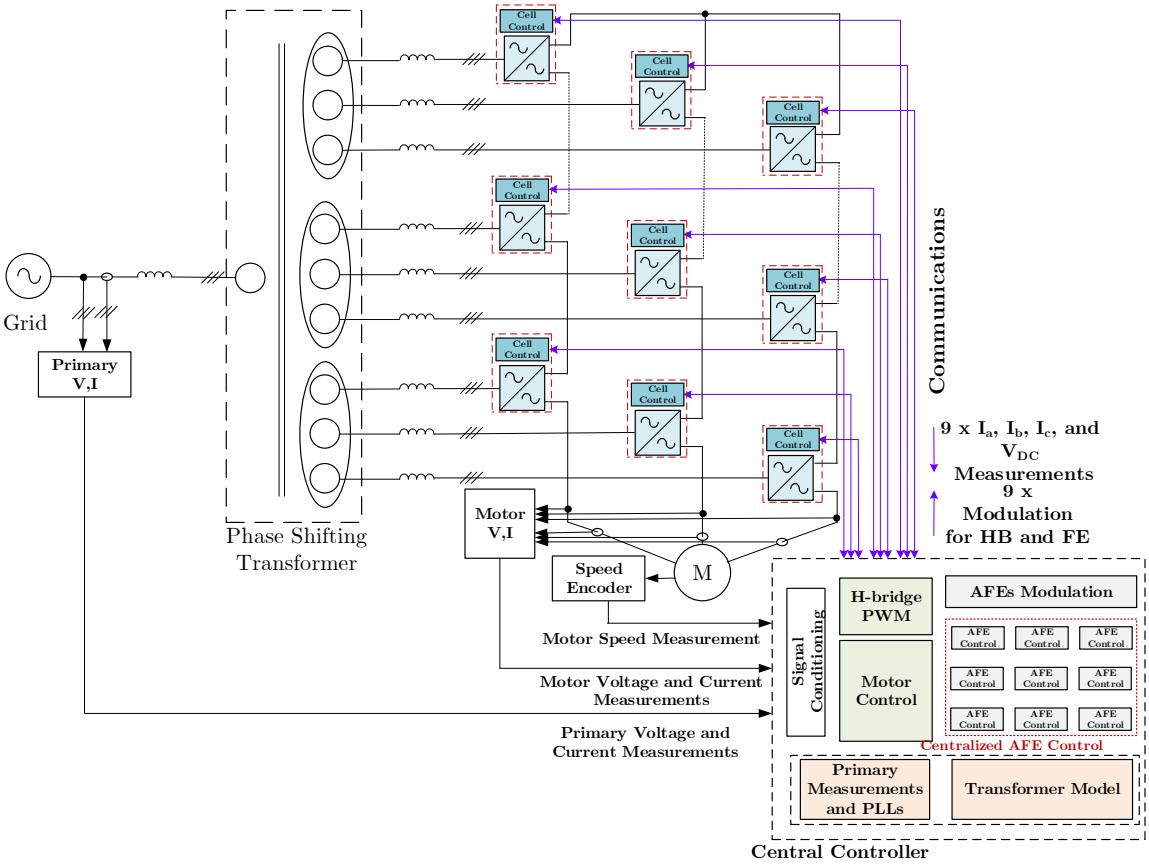



Fig. 7.27 Proposed Centralized Control Scheme with AFE Current Control and Eliminated Secondary Voltage Sensors.

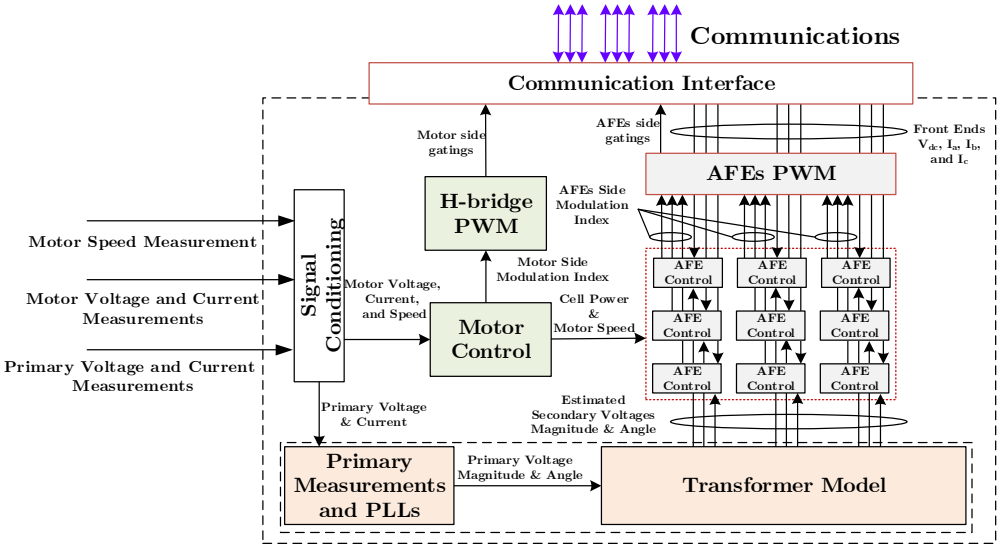



Fig. 7.28 Detailed Control Tasks and Signal Interfaces of Centralized Control Scheme with Current Controlled AFEs.

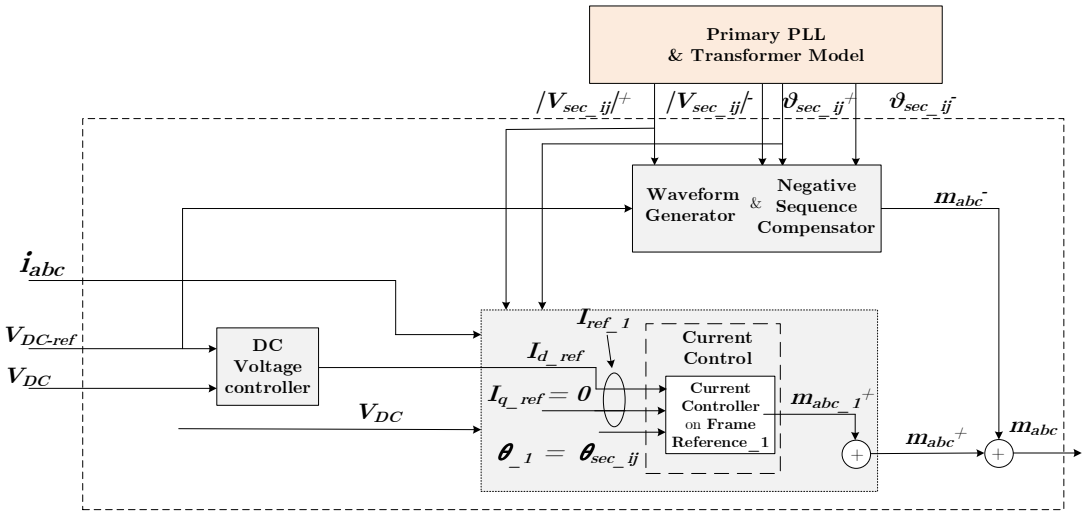



Fig. 7.29 Detailed AFE Control Scheme based on Current Control.

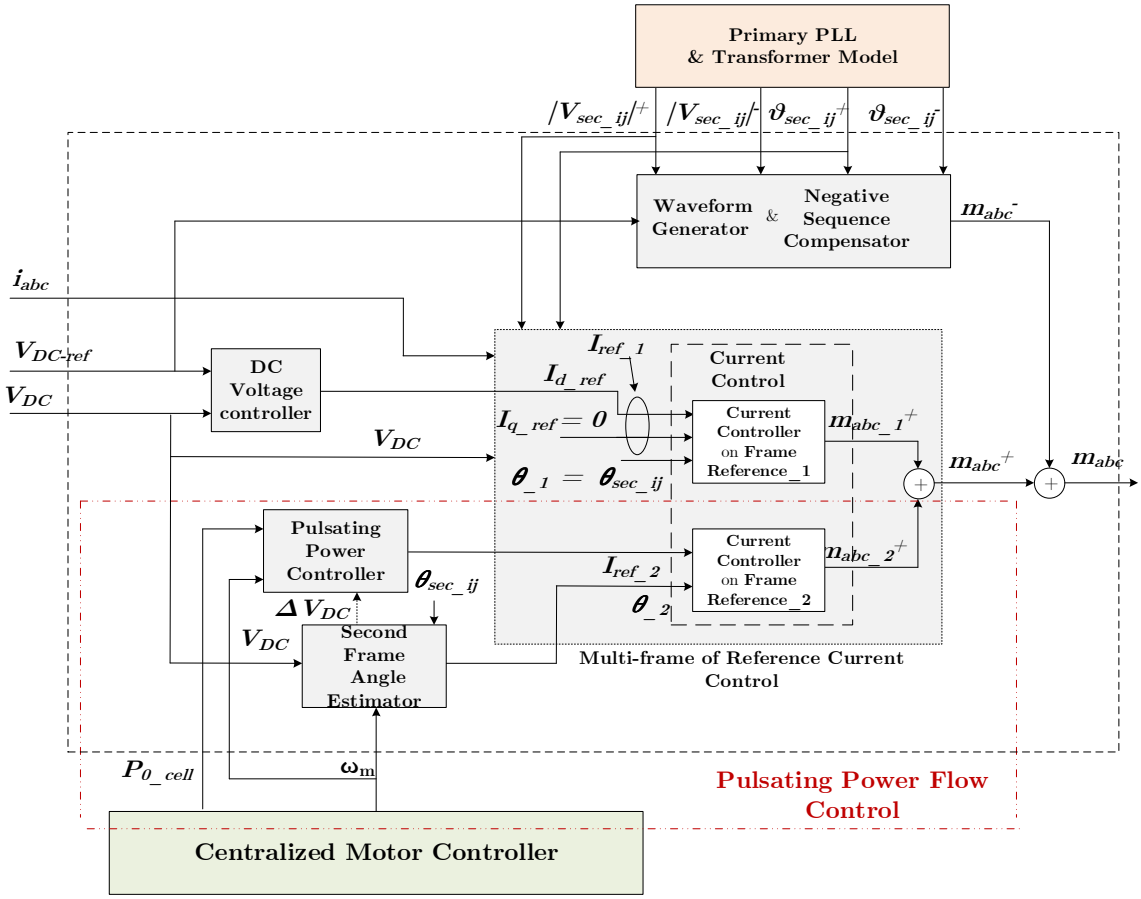



Fig. 7.30 AFE Controller based on Current Control and 2nd Order Pulsating Power Flow Control.

### 7.4.2. Proposed Centralized Control Scheme with AFE Voltage Angle Control and Eliminated Secondary Voltage and Current Sensors

Fig. 7.31 presents a proposed centralized control scheme for AFEs with voltage angle control with elimination of secondaries voltage and current information requirements. Only DC-bus voltages information are transmitted to the centralized control through the communication links.

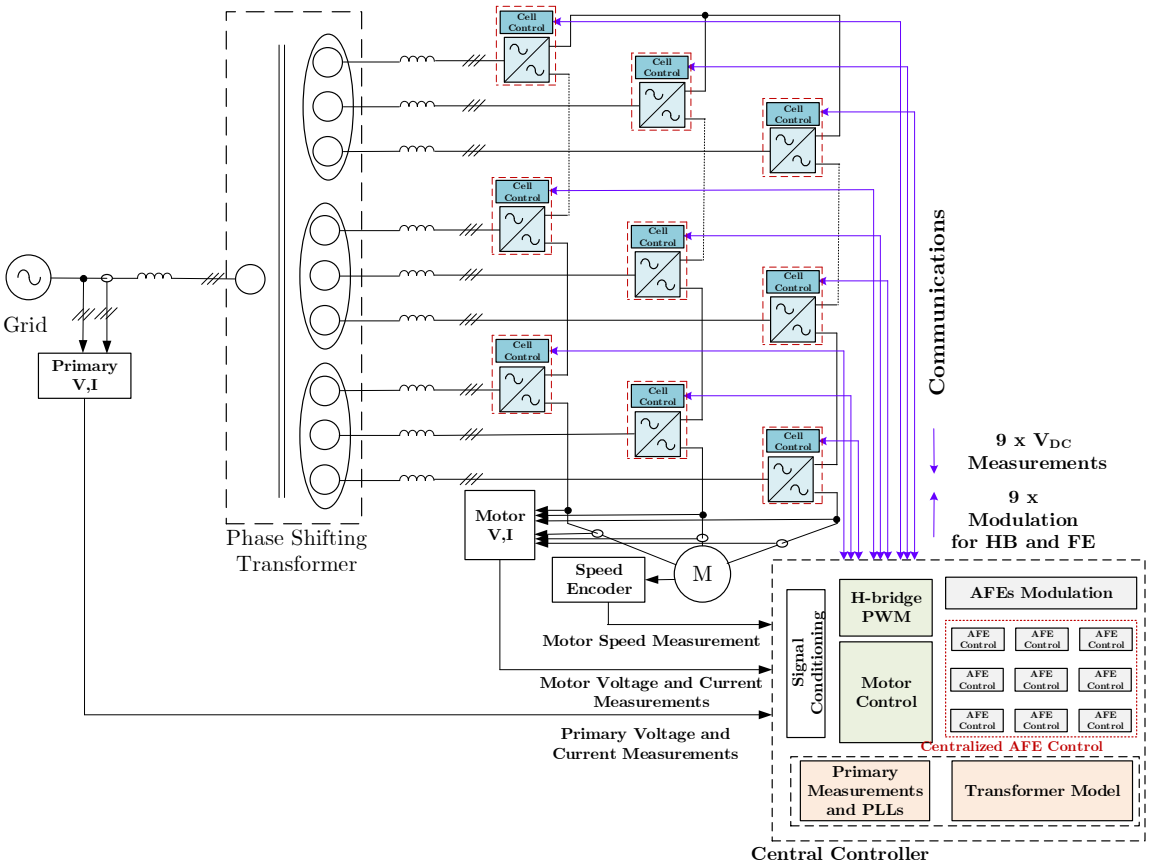



Fig. 7.31 Proposed Centralized Control Scheme with AFE Voltage Angle Control and Eliminated Secondary Voltage and Current Sensors.

AFE PWM gating signals are generated and synchronized before transmitted back to the power cells through the communication links. Fig. 7.32 shows the details of the control tasks and interface signals of the centralized control scheme. In order to eliminate the need for secondaries voltage sensors as discussed in the previous section, primary PLLs and transformer model are used to estimate the secondary voltages magnitudes and angles. Then these estimated signals are sent to the AFE controller instances. The voltage angle AFE controller structure is shown in Fig. 7.33.

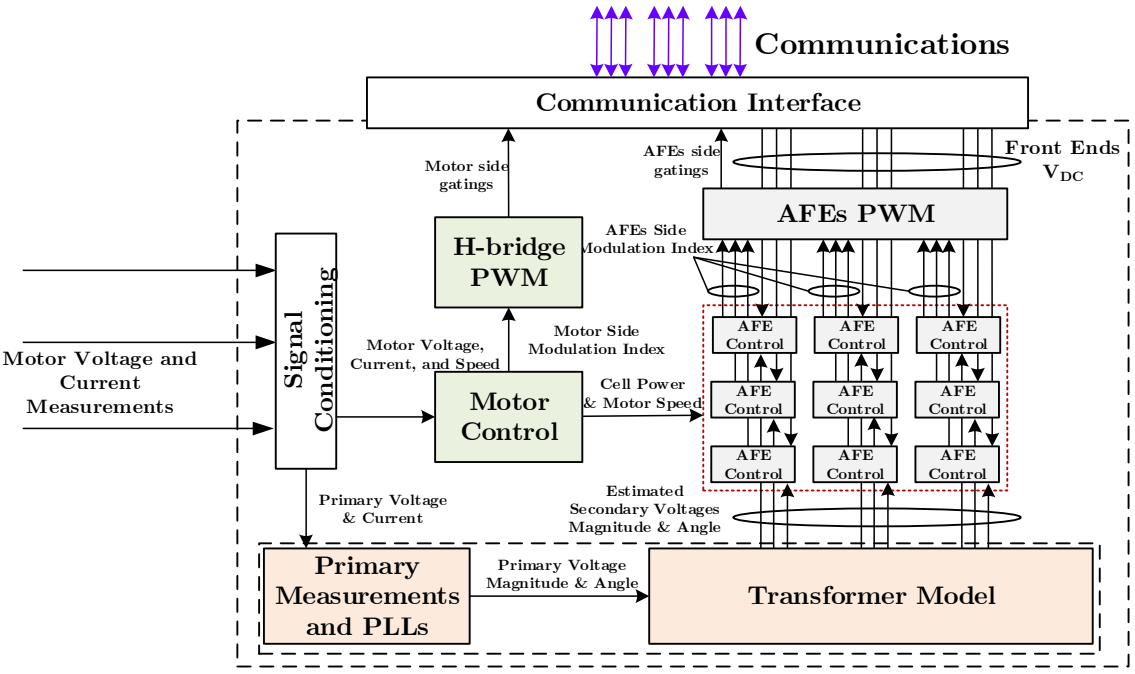



Fig. 7.32 Detailed Control Tasks and Signal Interfaces of Centralized Control Scheme based on Voltage Angle Control.

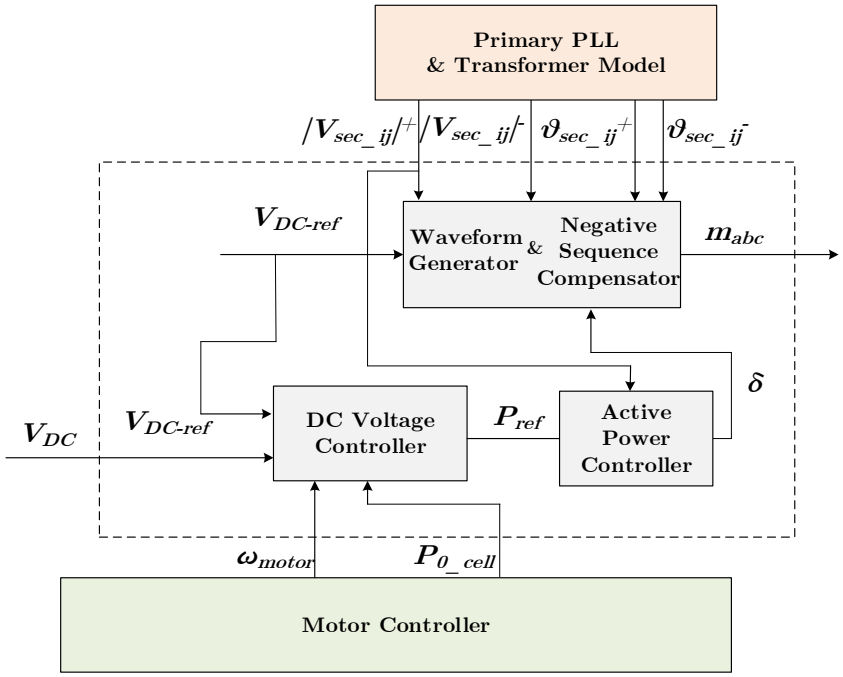



Fig. 7.33 Detailed AFE Control Scheme based on based on Voltage Angle Control

### 7.4.3. Proposed Centralized Control Scheme with FE Control and Eliminated Secondary Voltage and Current Sensors

Fig. 7.34 presents a proposed centralized control scheme for grid or near grid frequency switching front ends (FFEs) with elimination of secondaries voltage and current information requirement. Only DC-bus voltages information are transmitted to the centralized control through the communication links. Grid or near grid frequency switching gating signals are generated and transmitted back to the power cells through the communication links.

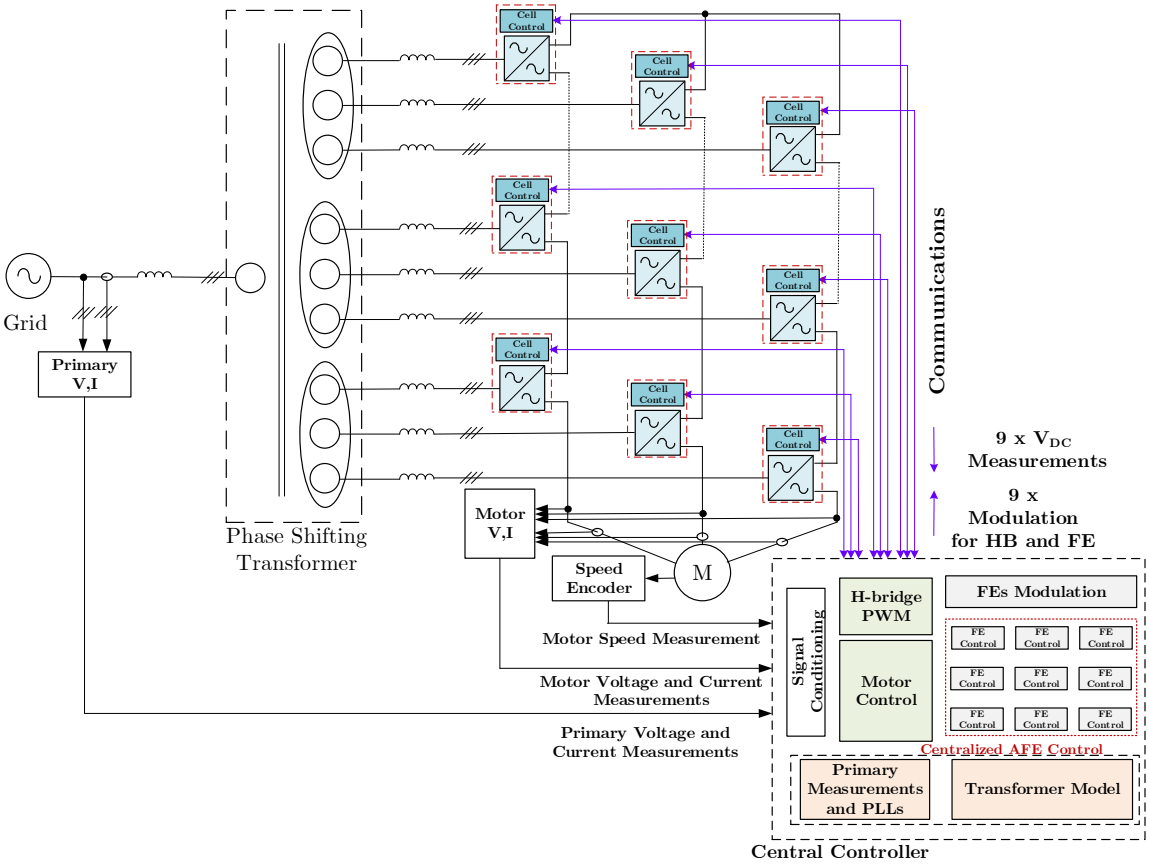



Fig. 7.34 Proposed Centralized Control Scheme with FE Control and Eliminated Secondary Voltage and Current Sensors.

The details of the control tasks and interface signals of the centralized control scheme is illustrated in Fig. 7.35. In order to eliminate the need for secondaries voltage sensors as discussed in the previous section, primary PLLs and transformer model are used to estimate the secondary voltages magnitudes and angles. Then these estimated signals are sent to the FE controller instances.

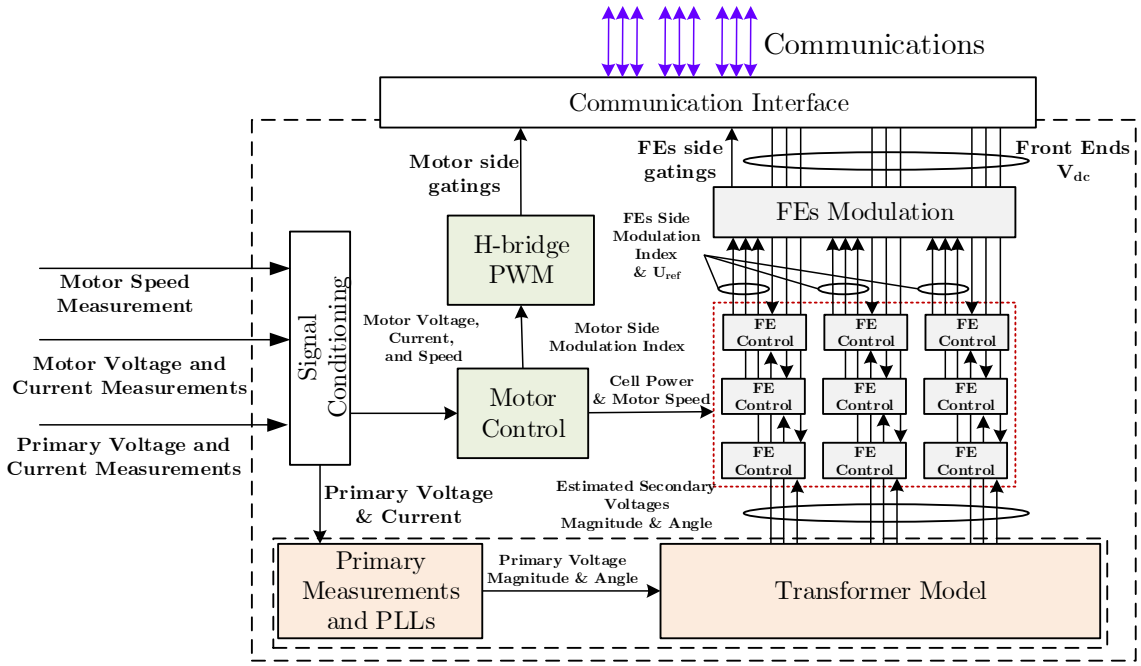



Fig. 7.35 Detailed Control Tasks and Signal Interfaces of Centralized Control Scheme based on Voltage Angle Control.

Fig. 7.36 and Fig. 7.37 present two possible variants for FE controllers: delay angle control and voltage angle. An advantage for the grid or near grid switching frequency is the low bandwidth requirement of the FEs gating signals compared to the bandwidth requirement of PWM gating signals. This decreases burden on the communication links between the central controller and the power cell.

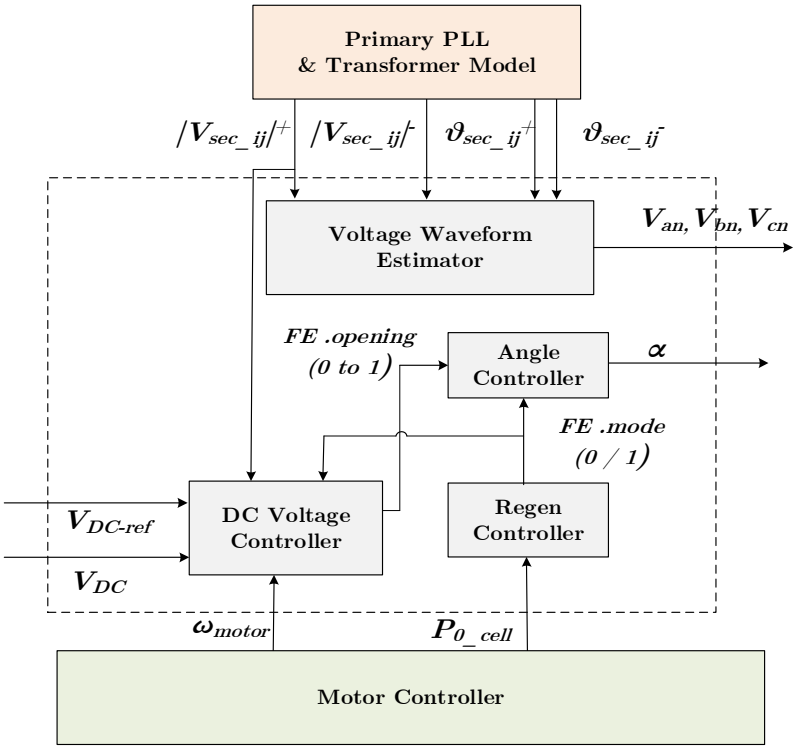



Fig. 7.36 Detailed FE Control Scheme based on Delay Angle Control.

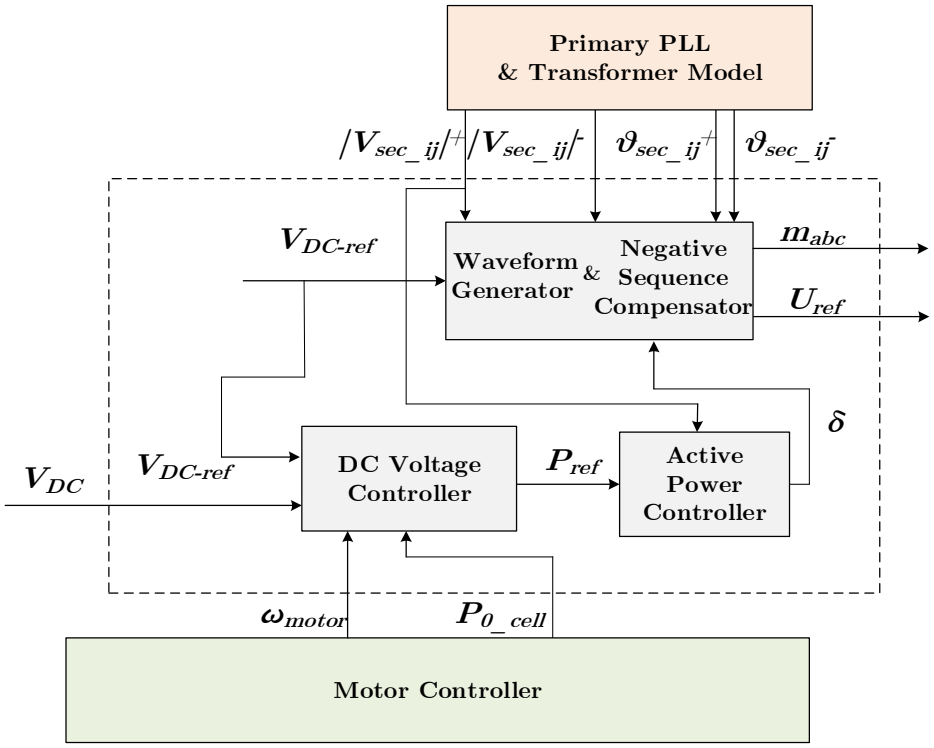



Fig. 7.37 Detailed FE Control Scheme based on Voltage Angle Control.

## 7.5.Simulation and Experimental Validation

Simulation and experimental studies have been conducted to validate effectiveness of the proposed front end control scheme based on employing a proposed transformer model for voltage angle estimation instead of front ends input voltages sensors as discussed in subsection 7.3.1. Simulation and experimental studies have been on a 9-cell regenerative CHB converter with parameters given in Table 7.1. System model has been built in MATLAB/Simulink.

Table 7.1 CHB Converter Simulation and Experimental Studies Main Parameters

| Converter parameter | Simulation Value | Experimental Value |
|---|---|---|
| **Cell DC-bus voltage (V)** | 830 (1 p.u for FFE) or 1100 (1 p.u for AFE) | 100 or 170 |
| **Transformer Secondary Side Voltage (V)** | 650 | 80 |
| **Equivalent Secondary Inductance (mH)** | 1 | 4 |
| **DC-Bus Capacitance (µF)** | 8600 | 2300 |
| **Base Current (A)** | 200 | - |

### 7.5.1. Simulation Studies

The objective is to validate that despite angles tolerances in the transformer model, fronts ends share almost equal currents without performance degradation of the DC-bus voltage regulation, and without degradation of harmonic cancellation at the primary of the transformer. Simulation results under the angles tolerances given

in Table 7.2 and Table 7.3 for the voltage angle controlled PWM-based AFEs discussed in subsection 7.4.2, and the grid or near grid frequency switching AFE discussed in subsection 7.4.3 have been performed. Parameters in Table 7.2 have been used with voltage angle controlled PWM-based AFEs simulations, while for grid or near grid frequency switching FEs parameters in Table 7.3 have been used.

Table 7.2 Angle Tolerance for 18-pulse Transformer in Simulation Studies (3 degrees)

| **Cell** | **Transformer** | | | **Transformer Model** | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **1** | **2** | **3** |
| **A** | -18 | -1 | 21 | -20 | 0 | 20 |
| **B** | -22 | 1 | 20 | -20 | 0 | 20 |
| **C** | -17 | 0 | 19 | -20 | 0 | 20 |

Table 7.3 Angle Tolerance for 54-pulse Transformer in Simulation Studies (3 degrees)

| **Cell** | **Transformer** | | | **Transformer Model** | | |
|---|---|---|---|---|---|---|
| | **1** | **2** | **3** | **1** | **2** | **3** |
| **A** | -25 | -7 | 12 | -27 | -7 | 13 |
| **B** | -20 | 1 | 21 | -20 | 0 | 20 |
| **C** | -14 | 5 | 28 | -13 | 7 | 27 |

Results for the power angle controlled PWM-based AFEs are presented in Fig. 7.38 to Fig. 7.41. Fig. 7.38 shows the secondary currents and DC-bus voltages of cells A1, A2, and A3, respectively. Fig. 7.39 shows the secondary currents and DC-bus voltages of cells B1, B2, and B3, respectively. Fig. 7.40 shows the secondary currents and DC-bus voltages of cells C1, C2, and C3, respectively. It

can been seen that secondary currents magnitudes and the DC-bus voltage magnitudes of the front ends are almost equal. This indicates that despite the angles tolerances, a front end controller based on elimination of secondary voltage sensors and relying of transformer model instead is effective. It should be noted that the slow oscillatory component present in the secondary waveform is attributed to the voltage angle controller action. Fig. 7.41 presents the primary current of the transformer. It should be noted that the PWM carriers are shifted by $120^o$ as illustrated in subsection 5.5. Primary current waveform shows that the harmonic cancellation at primary is still intact.

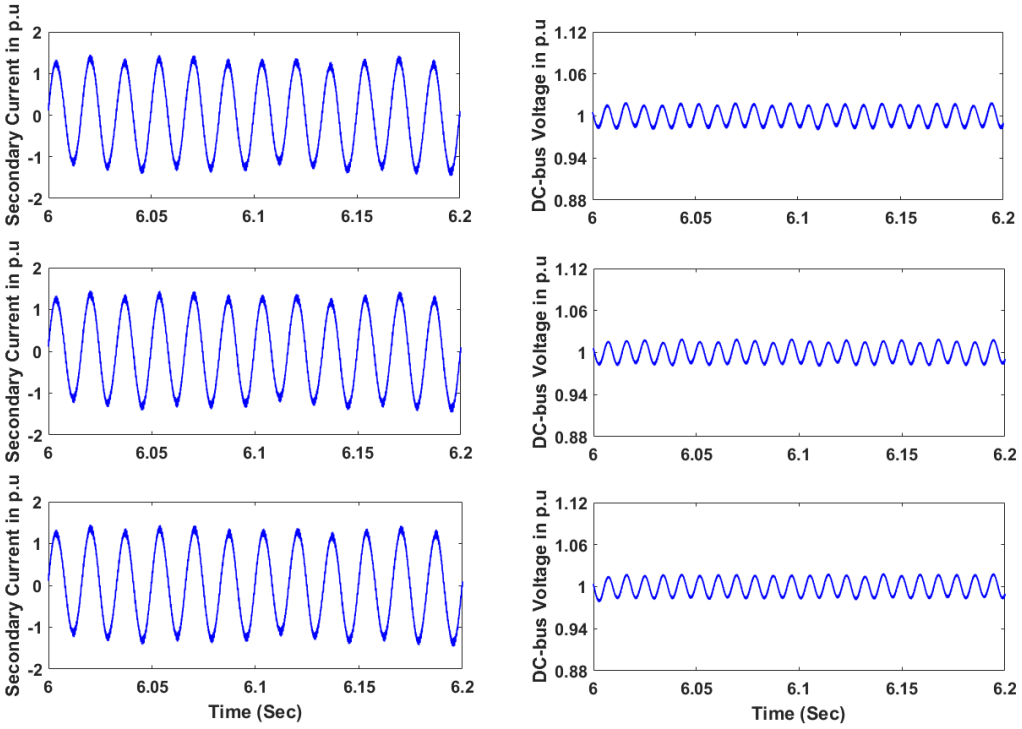



Fig. 7.38 Secondary currents and DC-bus voltages of PWM AFE cells A1, A2, A3.

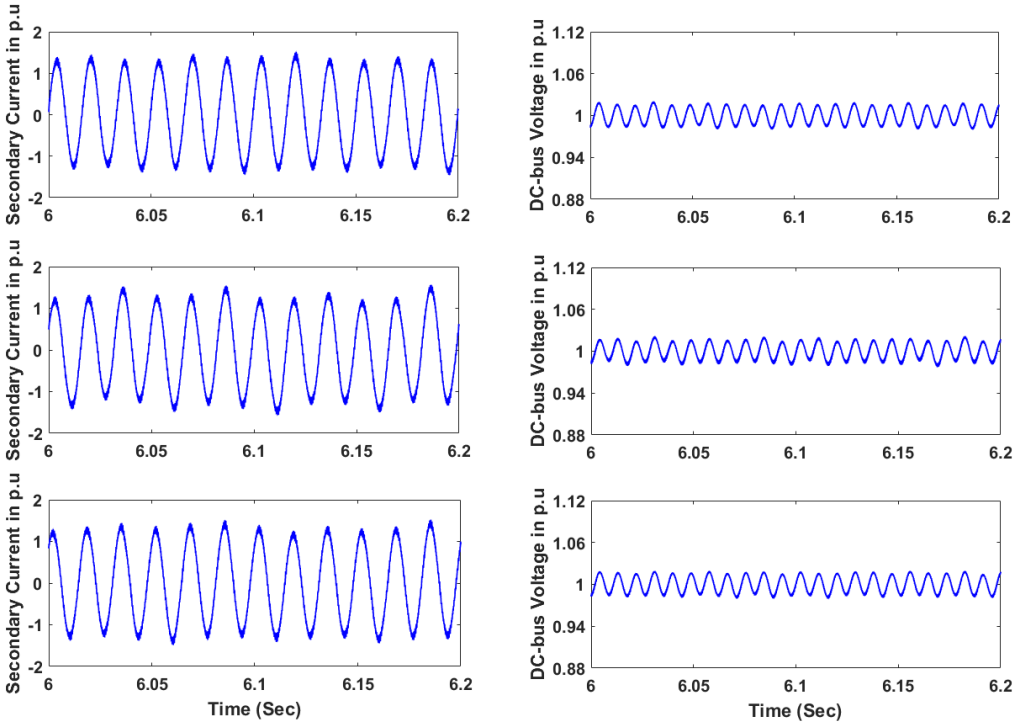



Fig. 7.39 Secondary currents and DC-bus voltages of PWM AFE cells B1, B2, B3.

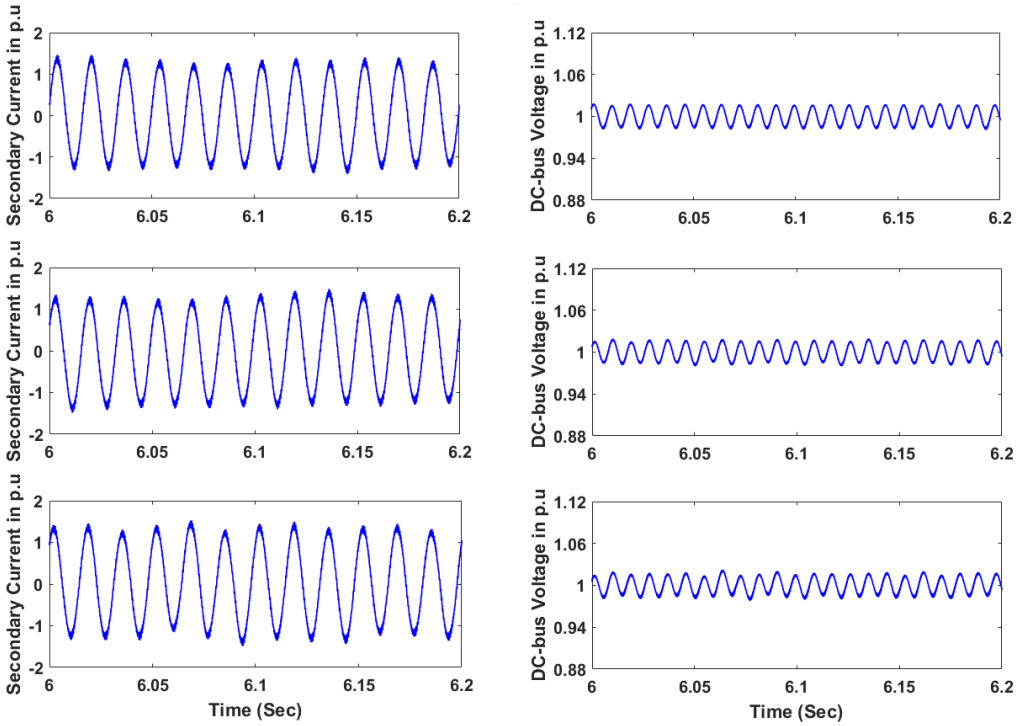



Fig. 7.40 Secondary currents and DC-bus voltages of PWM AFE cells C1, C2, C3.

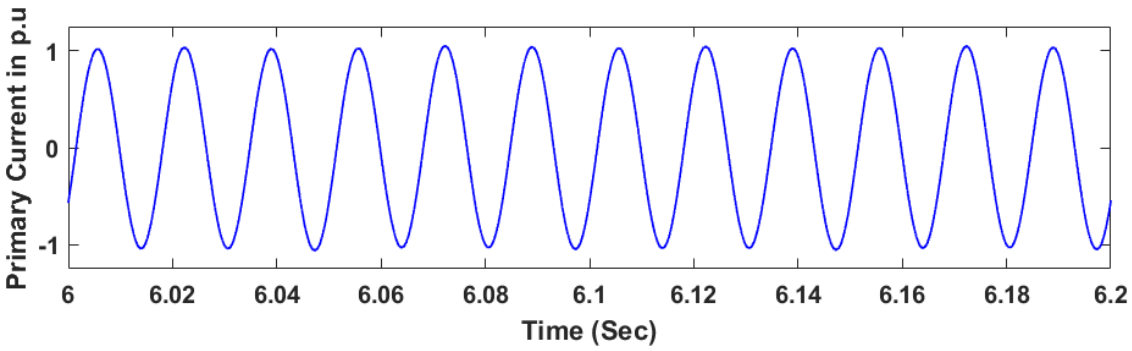



Fig. 7.41 Primary Current of PWM AFE CHB.

Accordingly, the CHB front end is able to satisfy the grid connection harmonic requirements while employing the transformer model for grid synchronization instead of the secondary voltage sensors. In addition, the slow oscillatory component in the secondary currents attributed to the voltage angle controller action does not show up in the primary currents.

Results for the voltage angle controller for grid or near grid frequency switching FEs (FFEs) are presented in Fig. 7.42 to Fig. 7.45. Fig. 7.42 shows the secondary currents and DC-bus voltages of cells A1, A2, and A3. Fig. 7.43 shows the secondary currents and DC-bus voltages of cells B1, B2, and B3. Fig. 7.44 shows the secondary currents and DC-bus voltages of cells C1, C2, and C3. The secondary currents magnitudes and the DC-bus voltage magnitudes of the front ends are almost equal. This validates the effectiveness of reliance on transformer model, despite of the angle tolerances, instead of secondary voltage sensors for the

front ends synchronization with the input voltages. Similar to the case of the voltage angle controlled PWM AFEs, slow oscillatory component is present in the secondary waveform, due to the voltage angle controller action. As shown in Fig. 7.45, the harmonic cancellation at primary is still intact. The CHB front end is able to satisfy the grid connection harmonic requirements while employing the transformer model for grid synchronization instead of the secondary voltage sensors. As in the case of PWM AFE CHB, the primary current is free of the slow oscillatory component, which caused by the voltage angle controller action and shows up at the secondary current.

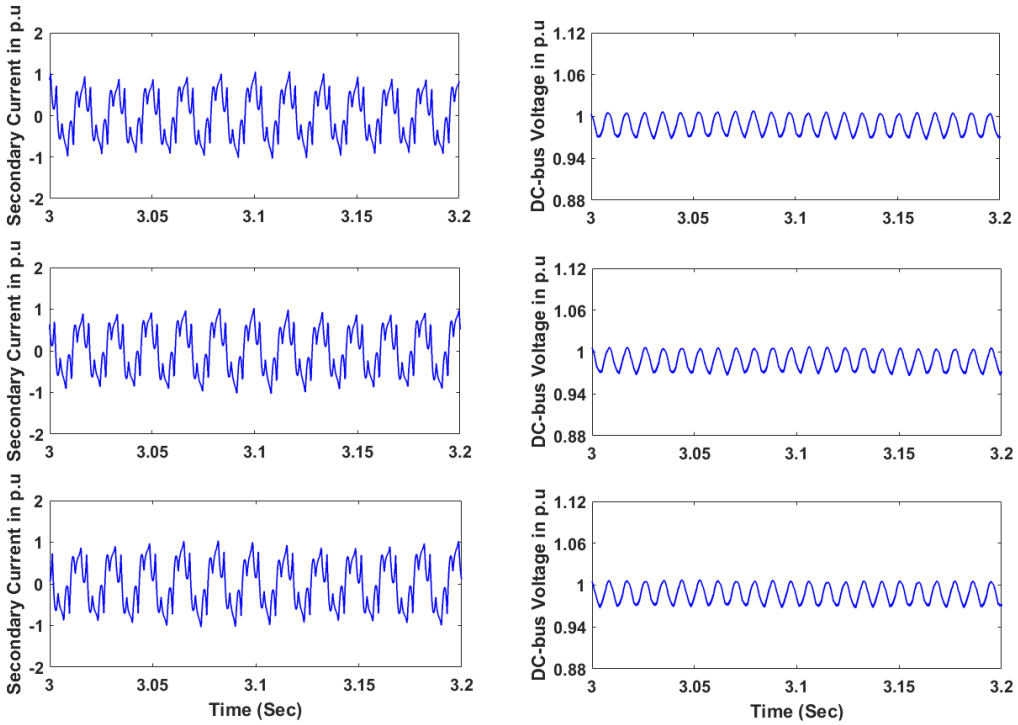



Fig. 7.42 Secondary currents and DC-bus voltages of FFE cells A1, A2, A3.

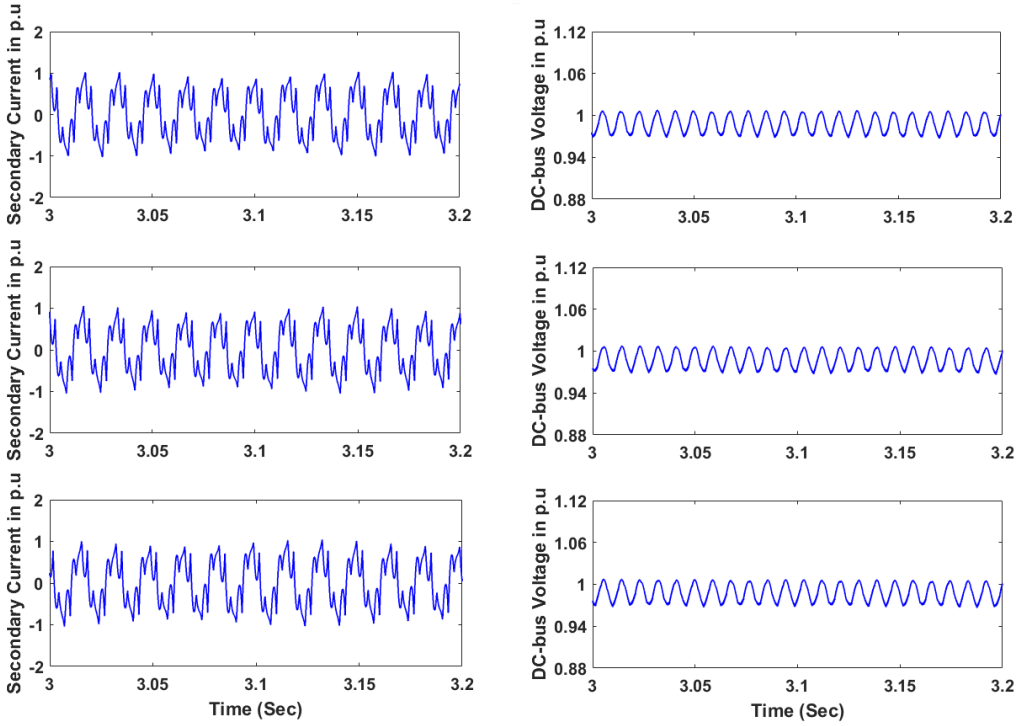



Fig. 7.43 Secondary currents and DC-bus voltages of FFE cells B1, B2, B3.

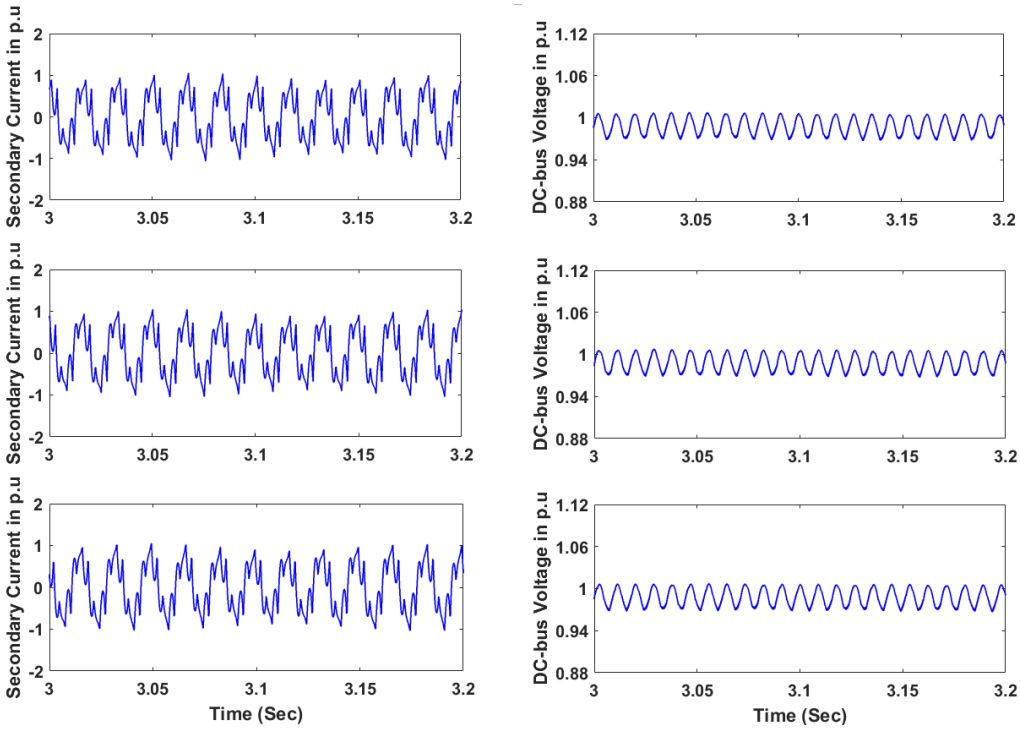



Fig. 7.44 Secondary currents and DC-bus voltages of FFE cells C1, C2, C3.

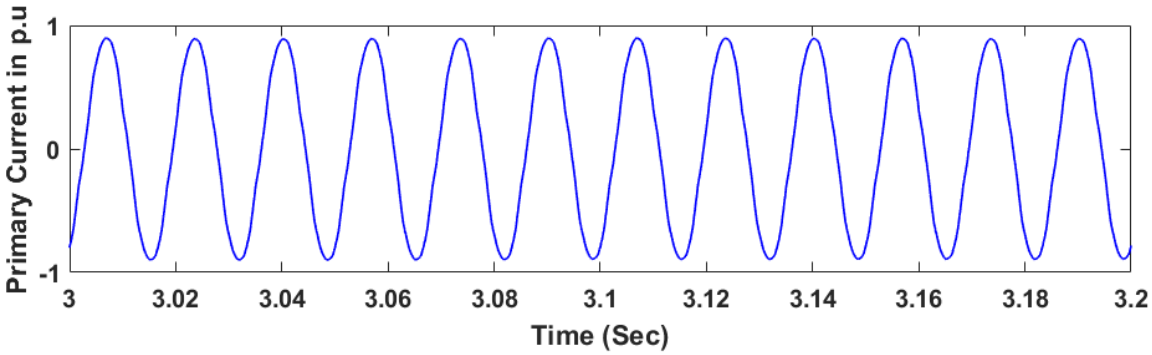



Fig. 7.45 Primary Current of FFE CHB.

### 7.5.2. Experimental Validation

Experimental studies have been performed to validate the effectiveness of employing a transformer model for front ends synchronization with input voltages instead of secondary voltage sensors. Practically, angle tolerances do exist in phase shifting transformers. Table 7.4 and Table 7.5 provide the phase shifting of 18-pulse and 54-pulse transformers utilized in the experimental studies for the voltage angle controlled PWM-based AFEs discussed in subsection 7.4.2, the current controlled PWM-based AFEs discussed in subsection 7.4.2, and the grid or near grid frequency switching AFE discussed in subsection 7.4.3. Parameters in Table 7.4 have been used with voltage angle controlled and current controlled PWM-based AFEs experiments, while for grid or near grid frequency switching FEs parameters in Table 7.5 have been used.

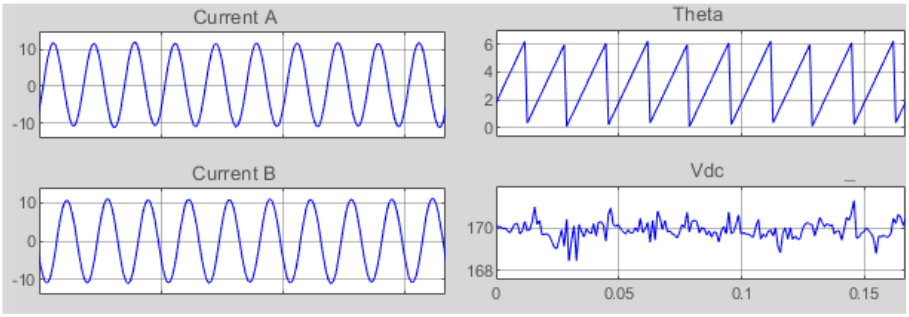
Table 7.4 Angle Tolerance for 18-pulse Transformer in Experiment

| Cell | Transformer | | | Transformer Model | | |
|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 1 | 2 | 3 |
| A | -22 | 0 | 18 | -20 | 0 | 20 |
| B | -22 | 0 | 18 | -20 | 0 | 20 |
| C | -22 | 0 | 18 | -20 | 0 | 20 |

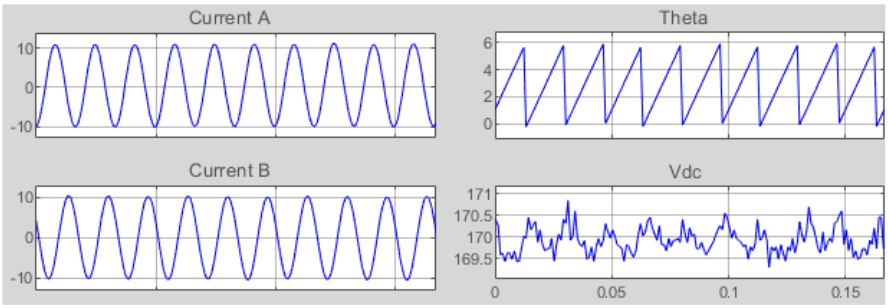
Table 7.5 Angle Tolerance for 54-pulse Transformer in Experiment

| Cell | Transformer | | | Transformer Model | | |
|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 1 | 2 | 3 |
| A | 25 | 6 | -15 | -27 | -7 | 13 |
| B | 18 | 0 | -21 | -20 | 0 | 20 |
| C | 13 | -8 | -28 | -13 | 7 | 27 |

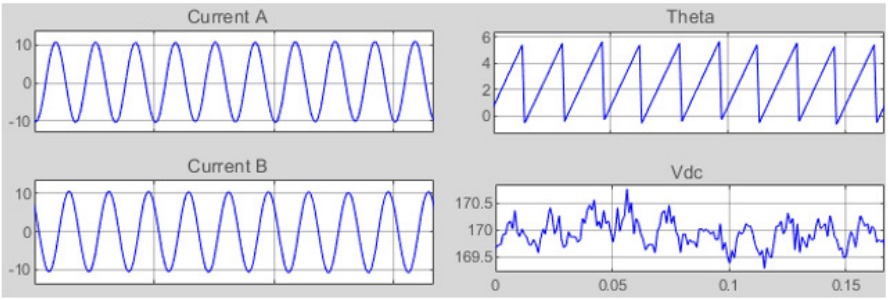
Experimental results for the voltage angle controlled PWM AFEs are presented in Fig. 7.46 to Fig. 7.49. Fig. 7.46 shows SCADA results for the secondary currents and DC-bus voltages of cells A1, A2, and A3, respectively. Fig. 7.47 shows the SCADA results for B1, B2, and B3, respectively. Fig. 7.48 shows the SCADA results for cells C1, C2, and C3, respectively.




(a) Cell A1

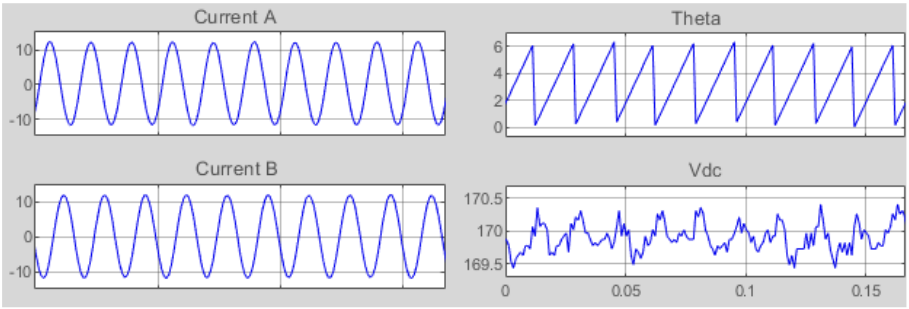



(b) Cell A2

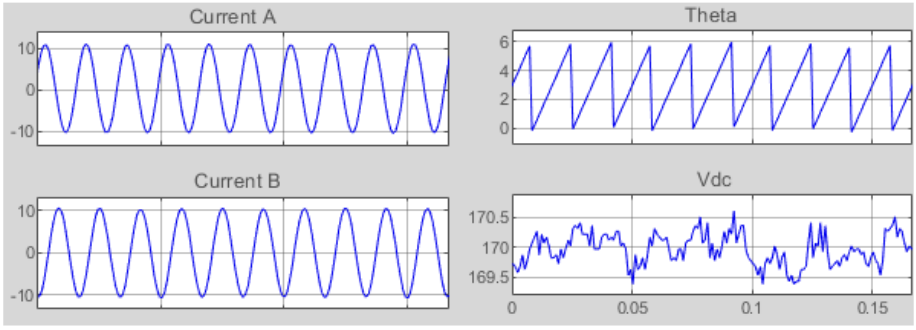



(c) Cell A3

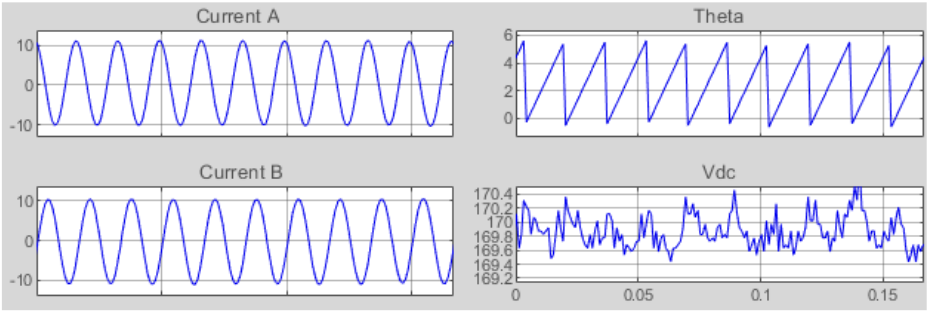
Fig. 7.46 SCADA Secondary Currents and DC-bus Voltages of AFE cells A1, A2 and A3




(a) Cell B1

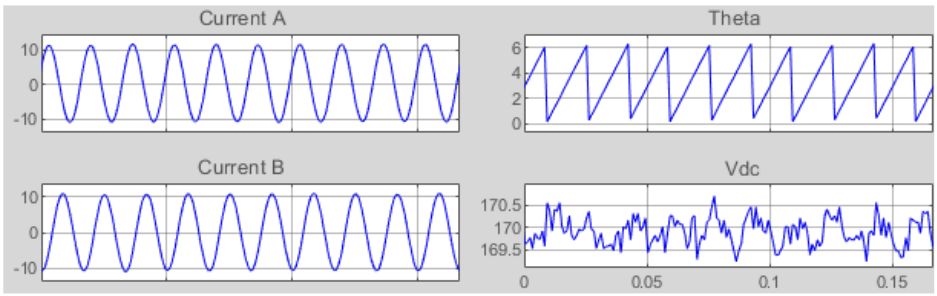



(b) Cell B2

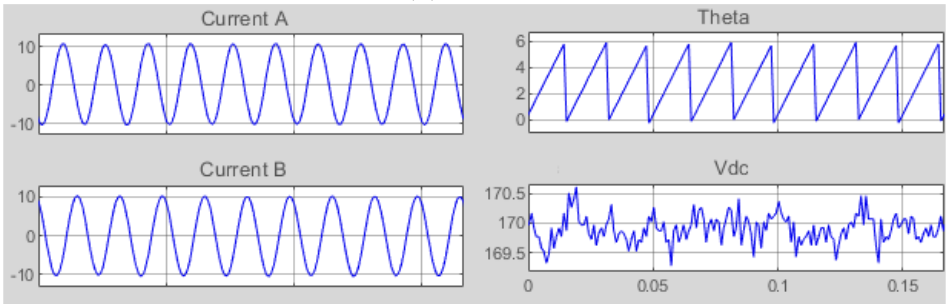



(c) Cell B3

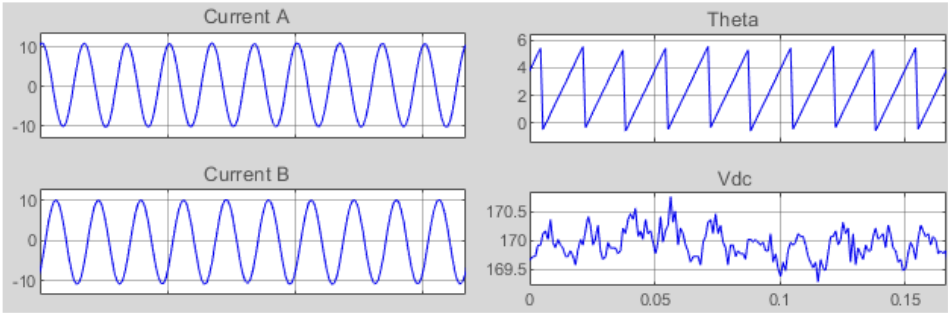
Fig. 7.47 SCADA Secondary Currents and DC-bus Voltages of AFE cells B1, B2 and B3.




(a) Cell C1




(b) Cell C2

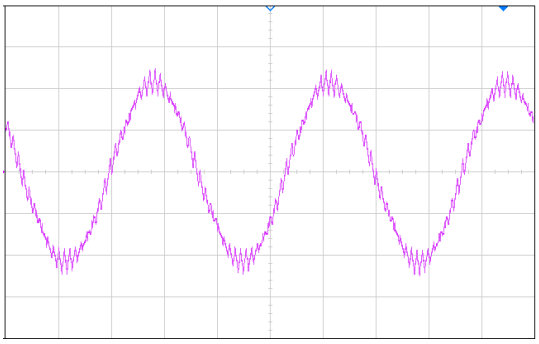



(c) Cell C3

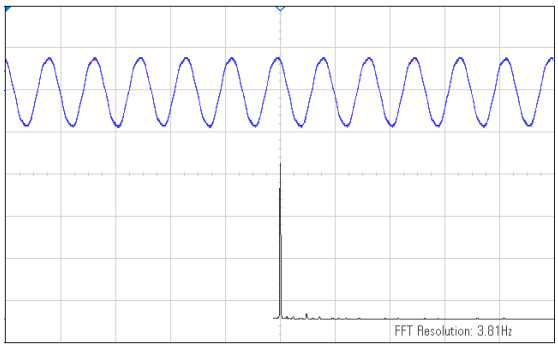
Fig. 7.48 SCADA Secondary Currents and DC-bus Voltages of AFE cells C1, C2 and C3.

Despite the angle tolerances, the secondary currents magnitudes and the DC-bus voltage magnitudes of the front ends are almost equal. This confirms the effectiveness of utilizing the transformer model for synchronization instead of the secondary voltage sensors.

The currents waveforms presented in Fig. 7.49 shows that the harmonic cancellation at the primary is still intact under $120^o$ shift between PWM carriers. This validates the CHB front end is able to satisfy the grid connection harmonic requirements while employing the transformer model for grid synchronization instead of the secondary voltage sensors.



(a) Secondary Current
(5 A / div) (5ms / div)

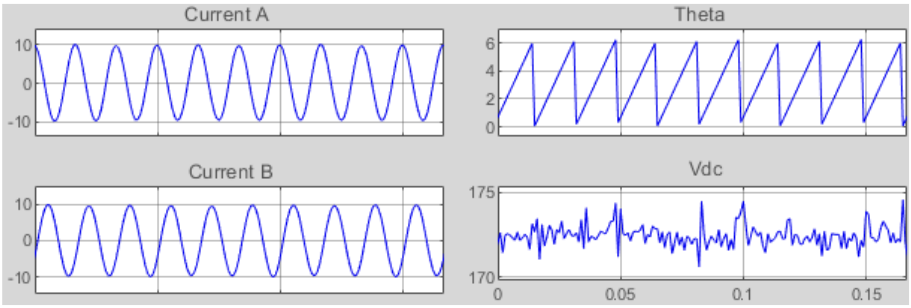



(b) Primary Current
(35A / div)(20ms / div)
( 60Hz FFT Center)

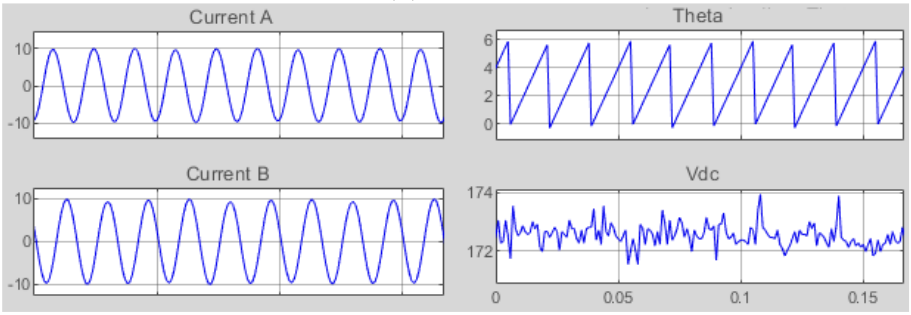
Fig. 7.49 Voltage Angle Controlled AFE CHB

Experimental results for the current controlled PWM AFEs are presented in Fig. 7.50 to Fig. 7.53. Fig. 7.50 shows SCADA results for the secondary currents and DC-bus voltages of cells A1, A2, and A3, respectively. Fig. 7.51 shows the

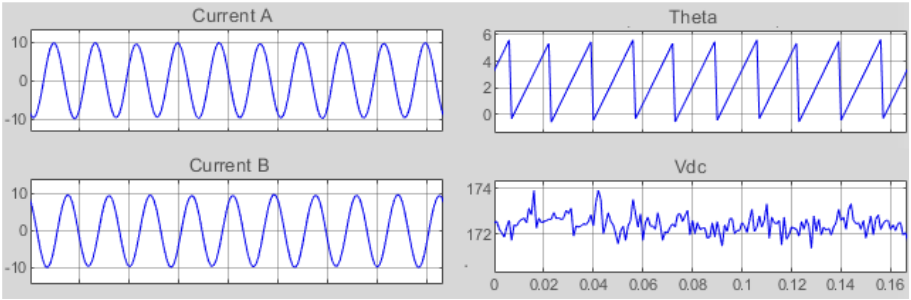
SCADA results for cells B1, B2, and B3, respectively. Fig. 7.52 shows the SCADA results for cells C1, C2, and C3, respectively. The secondary currents magnitudes and the DC-bus voltage magnitudes of the front ends are almost equal in spite of transformer angles tolerance, which validates the effectiveness of utilizing the transformer model for synchronization instead of the secondary voltage sensors.




(a) Cell A1

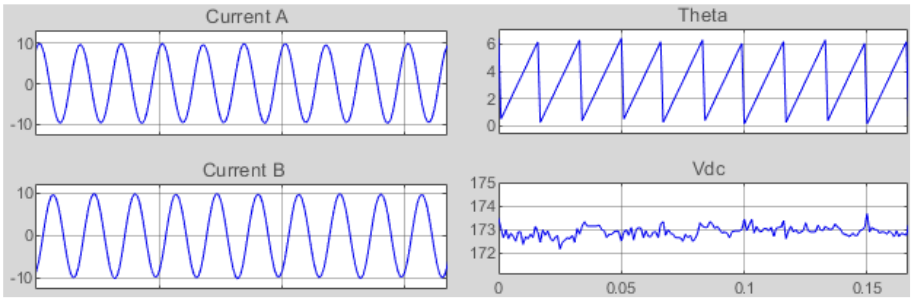



(b) Cell A2

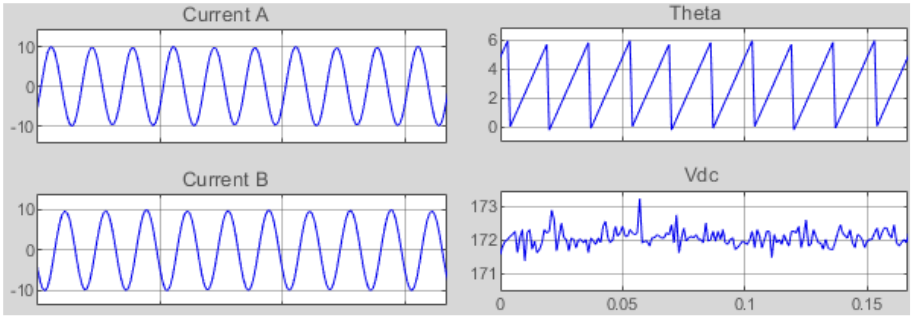



(c) Cell A3

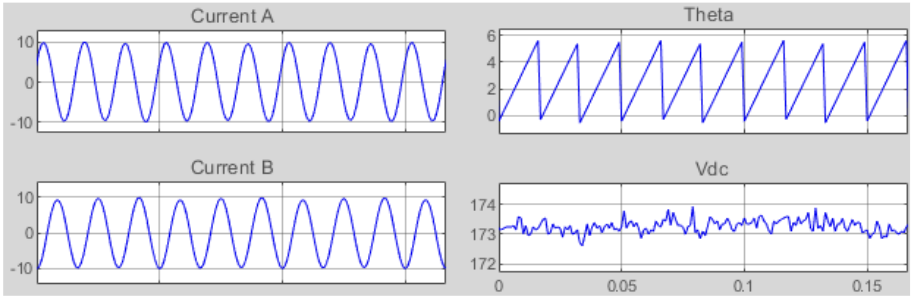
Fig. 7.50 SCADA Secondary Currents and DC-bus Voltages of AFE cells A1, A2 and A3.




(a) Cell B1

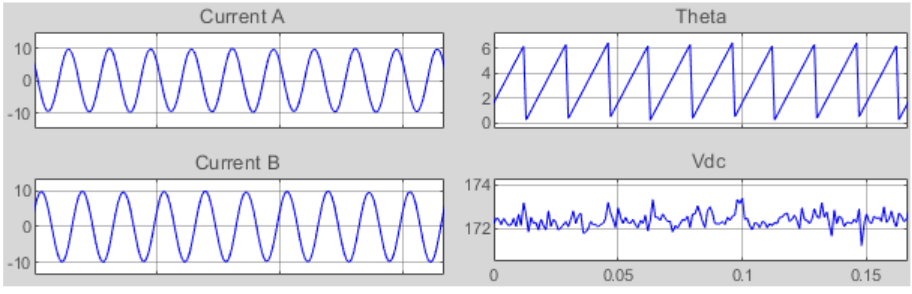



(b) Cell B2

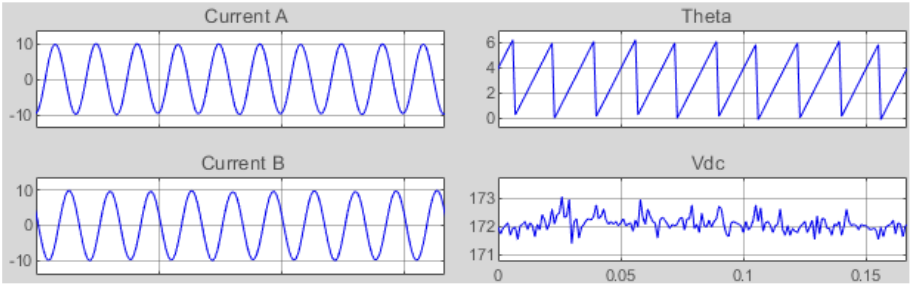



(c) Cell B3

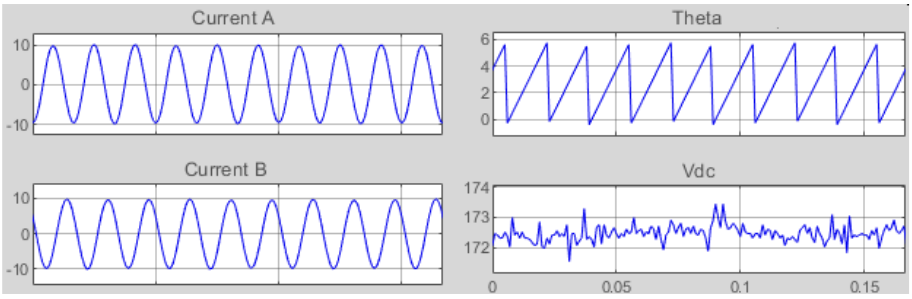
Fig. 7.51 SCADA Secondary Currents and DC-bus Voltages of AFE cells B1, B2 and B3.




(a) Cell C1



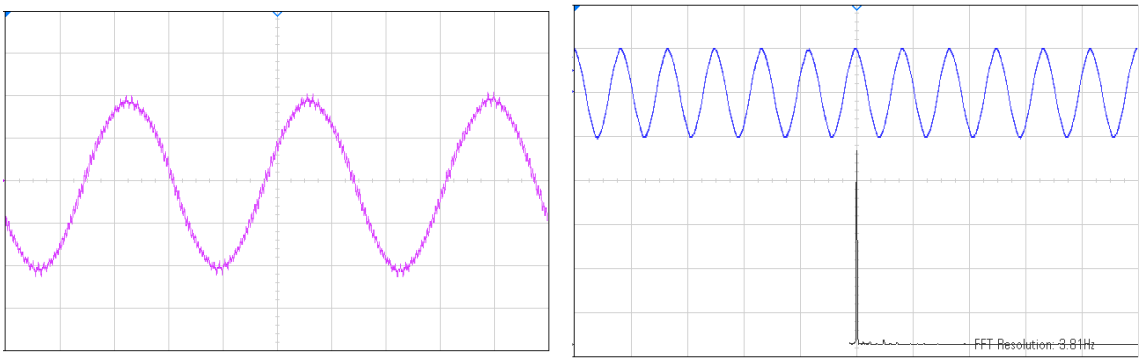

(b) Cell C2




(c) Cell C3

Fig. 7.52 SCADA Secondary Currents and DC-bus Voltages of AFE cells C1, C2 and C3.

The currents waveforms presented in Fig. 7.53 shows that the harmonic cancellation at primary is still intact under $120^{o}$ shift between PWM carriers. This confirms that using a transformer model for synchronization, CHB front end satisfies the grid harmonic requirements.

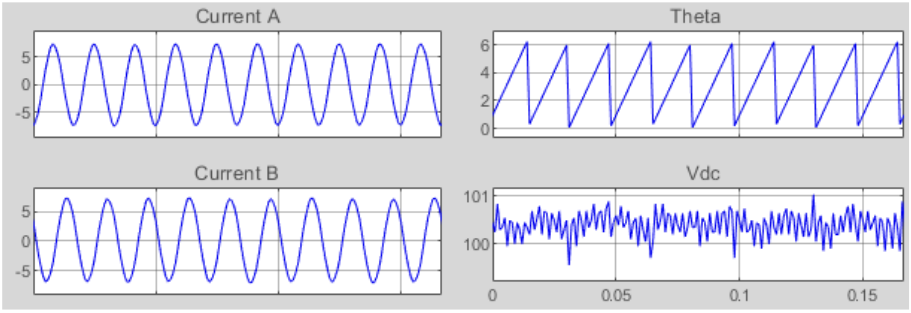



(a) Secondary Current
(5 A / div) (5 ms / div)

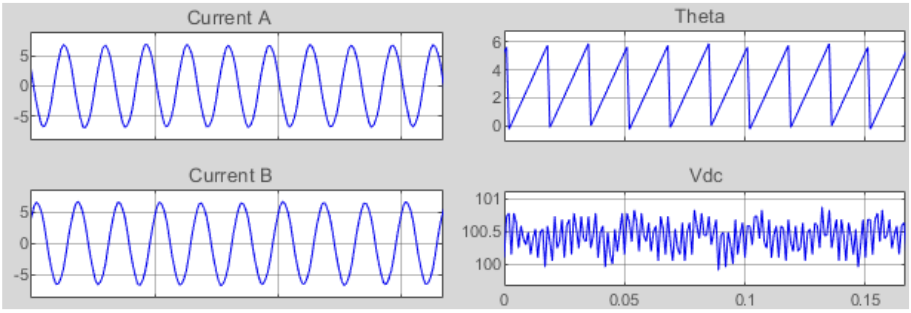
(b) Primary Current
(35A / div)(20ms / div)
( 60Hz FFT Center)

Fig. 7.53 Current Controlled AFE CHB

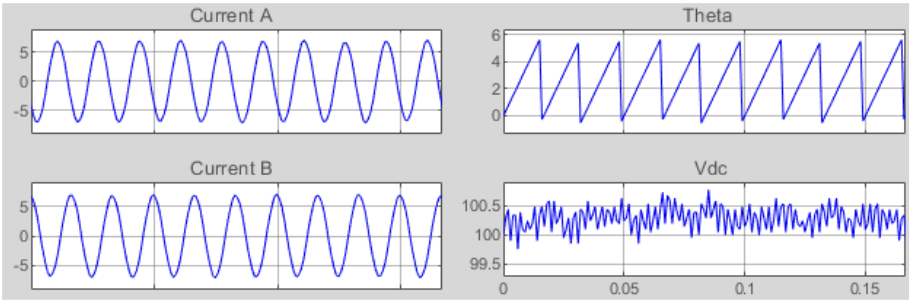
Experimental results for the voltage angle controlled grid or near grid frequency switching FEs (FFEs) are presented in Fig. 7.54 to Fig. 7.57. Fig. 7.54 to Fig. 7.56 show SCADA results for filtered secondary currents and DC-bus voltages of cells in phases A, B, and C, respectively. Fig. 7.54 shows results cells A1, A2, and A3, respectively; Fig. 7.55 shows results cells B1, B2, and B3, respectively; and Fig. 7.56 shows results cells C1, C2, and C3, respectively. The SCADA waveforms show that the secondary currents magnitudes and the DC-bus voltage magnitudes of the front ends are almost equal. This validates the effectiveness of employing a transformer model instead of secondary voltage sensors for synchronization despite of the angle tolerances.




(a) Cell A1

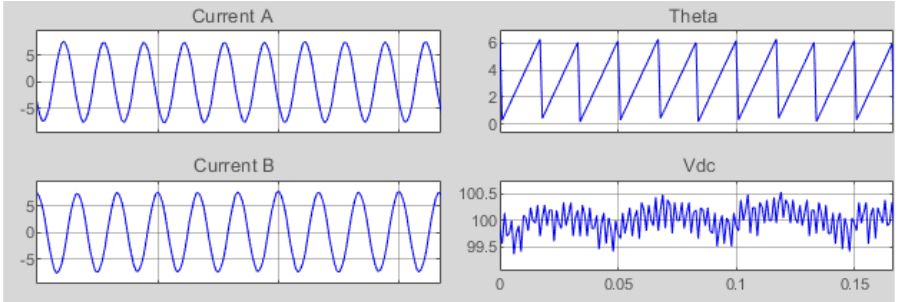



(b) Cell A2

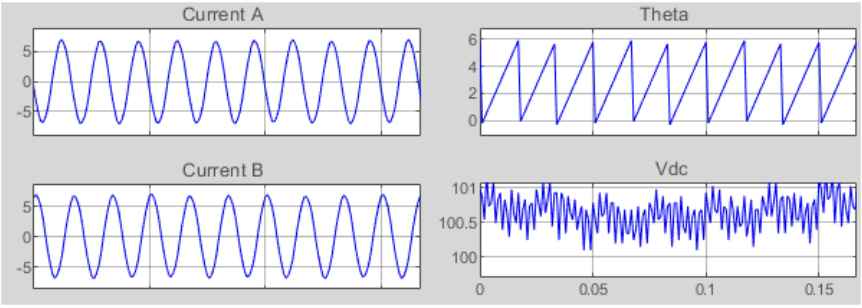



(c) Cell A3

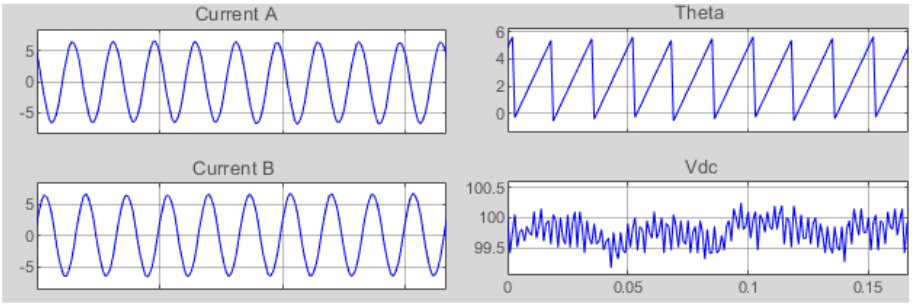
Fig. 7.54 SCADA Secondary Currents (low pass filtered at 120 Hz) and DC-bus Voltages FFE cells A1, A2 and A3.




(a) Cell B1

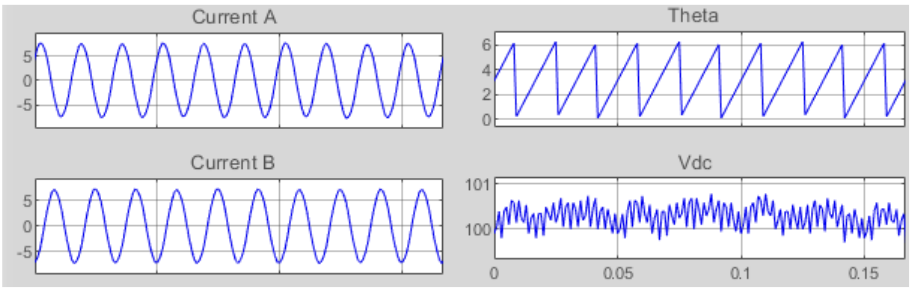



(b) Cell B2

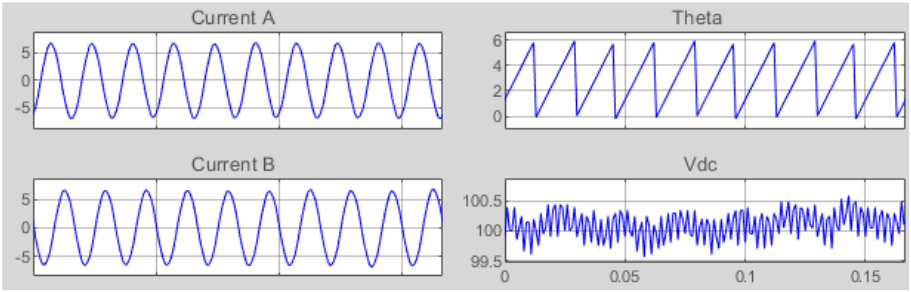



(c) Cell B3

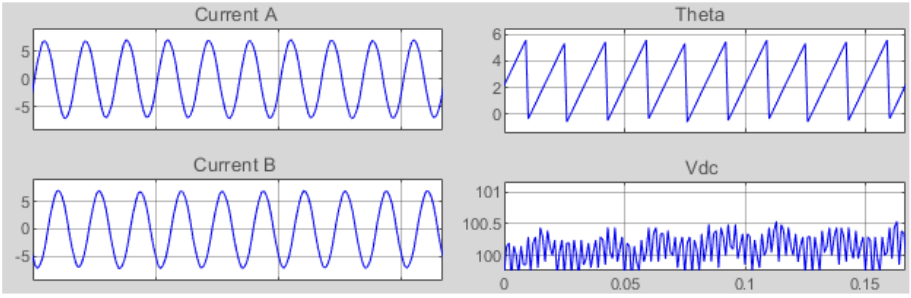
Fig. 7.55 SCADA Secondary Currents (low pass filtered at 120 Hz) and DC-bus Voltages of FFE cells B1, B2 and B3.




(a) Cell C1



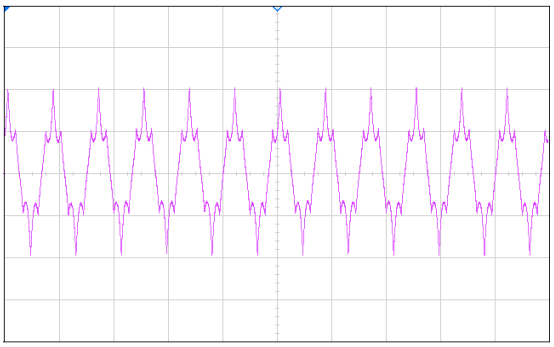

(b) Cell C2



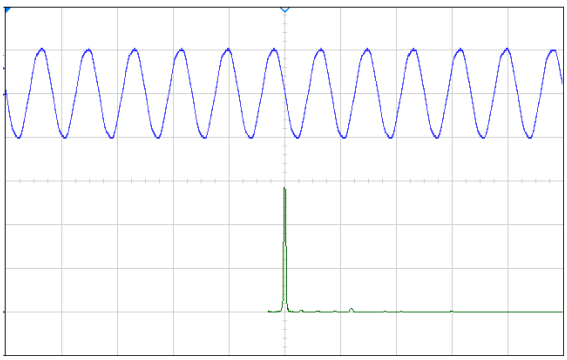

(c) Cell C3

Fig. 7.56 SCADA Secondary Currents (low pass filtered at 120 Hz) and DC-bus Voltages of FFE cells C1, C2 and C3.

Fig. 7.57 presents the current at the primary of the transformer and compares it to the secondary current. The primary current waveform shows that the harmonic cancellation at primary is still intact. Thereby, the CHB front end ability to satisfy the grid connection harmonic requirements while employing the transformer model for grid synchronization is validated.



(a) Secondary Current
(5 A / div) (20 ms / div)



(b) Primary Current
(35A / div)(20ms / div)
( 60Hz FFT Center)

Fig. 7.57 Voltage Angle Controlled FFE CHB.

## 7.6. Summary

The number of additional sensors required by the conventional AFE CHB front end with respect to DFE CHB is an aspect that affects the reliability and the cost of the regenerative CHB converters. In addition, embedding additional sensing and control circuitry to the densely-packed power cell operating in harsh conditions such as elevated temperatures, compromises power cell's circuitry reliability. To tackle this challenge, Chapter 7 proposes a reduced sensor count centralized CHB front end control scheme. This is to achieve minimum modifications to the existing DFE CHB control scheme, which is of a huge benefit leading to improvement of system reliability and reduction of system complexity. Detailed discussion has been included about the proposed transformer model employed to provide the angle information for the cell front end controllers for input voltage synchronization instead of relying on secondary voltage sensors. In addition, the chapter has provided detailed signal flow and control tasks schematics for proposed centralized current controlled PWM based AFEs, voltage angle controlled PWM based AFEs, delay angle controlled grid or near grid switching frequency FEs, and voltage angle controlled grid or near grid switching frequency FEs. Furthermore, the communication requirements between the central controller and the power cells have been addressed. 9-cell CHB system simulation and experimental validation

have been performed using a centralized transformer model for input voltage synchronization instead of secondary voltage sensors. The results have validated the effectiveness and the performance of the centralized input voltage synchronization.

# Chapter 8

# Conclusions and Future Work

## 8.1.Thesis Summary

Cascaded H-bridge (CHB) multilevel inverters are extensively used in different motor drives applications due to different features such as the modular structure and fault tolerant capability. A typical CHB power cell employs diode front end (DFE), which allow only power flow to be from the grid to the load side. In order add regenerative capability to CHB drives, power cells that employ active front ends (AFEs) have been introduced and are still being under continuous development in the industry to integrate the CHB drives in the regenerative markets.

A detailed literature review on the CHB structure, and the field failures and long reliability has shed light on the thermal induced long-term reliability issues of power modules, electrolytic DC-bus capacitors, PCBs and signal electronics in CHB drives.

The thesis work has addressed regenerative CHB topology reliability during design stage through proposing novel regenerative cascaded H-bridge converter control schemes to:

1. Reduce Components Stresses to Improve Long-term Reliability
2. Reduce Component Count to Reduce Failure Random Probability
3. Achieve Other System Benefits (e.g., Cost, Size)

A novel PWM active front end control scheme has been proposed to reduce the inherent ripple current stresses on the DC-bus capacitors. In addition, the thesis has proposed a novel grid or near grid switching frequency front end control scheme to reduce stresses on power modules and the power cell cooling requirements. Furthermore, a novel cascaded H-bridge front end control scheme is proposed to reduce the sensor count, thereby decreasing failure rate and cutting down cost.

In addition to simulation studies, an experimental hardware setup was implemented to validate the proposed control schemes. The setup is a scaled down 9-cell 7-level regenerative CHB drive. It has been developed in part of research

collaboration with the MV drives R&D in Rockwell Automation for the experimental validation of research outcomes.

### 8.1.1. Reduction of Stresses on DC-bus Capacitors

DC-bus capacitors experience high ripple current stresses due to the inherent instantaneous power unbalance existing in the CHB cells. For energy density reasons, CHB converters employ aluminum electrolytic capacitors. Under these current stresses, electrolytic capacitors degrade in accelerated fashion. Taking the advantage of the degrees of freedom offered by AFEs compared to DFEs, Chapter 5 proposes an AFE control scheme to control pulsation power flow with no additional components. Hence, pulsation power are diverted from the DC-bus capacitors to the secondary of the transformer. To achieve high performance, the control scheme employs multi-frame of reference current controller. In addition, to comply with the IEEE 519-2014 grid harmonic currents standards with reduced filtering requirements, proposed control scheme employs SPWM. Simulation and experimental studies have been performed on a 9-cell CHB system. Current stress and lifetime analyses of real case power cell have showed that up to 300 % improvement in DC-bus capacitors lifetime can be achieved.

### 8.1.2. Reduction of Stresses on Active Front Ends Power Modules and Cut down of Power Cell Cooling Requirements

In order to satisfy IEEE 519-2014 grid harmonic currents standard with reduced filter size, PWM-based AFE use switching frequency up to 2 kHz to 4 kHz. As a result, power modules suffer increased switching losses, and so higher cycling temperature stresses.

Temperature stresses accelerate power modules degradation causing power module to reach end-of-life. To tackle this challenge, chapter 6 proposes two front end (FE) modulation and control scheme based on grid or near grid switching frequency. Power loss, thermal, and lifetime analyses of real case power cell have shown a reduction of about 50% in power loss, about 10 °C decrease in maximum junction temperature, and about 60-70 % improvement in power modules lifetime. In addition, there are other important system benefits such as the ability of per cell heat sink size reduction and the prevention of high frequency emissions into the grid caused by PWM operation that may excite resonance modes. The chapter proposed a delay angle-based and a voltage angle-based grid or near grid switching frequency front ends. The harmonic cancellation at the primary of the transformer under the proposed modulation schemes has been discussed thoroughly. Moreover,

the dynamic performance of the proposed control scheme under load step change and input voltage disturbances has been addressed. 9-cell CHB system simulation and experimental studies have validated the effectiveness and the performance of the two proposed modulation and control schemes while achieving the objectives.

### 8.1.3. Decrease of Failure Rate, Cost, and the Complexity of Active Front End Power Cell through Reducing the Number of Sensors and Adopting Centralized Front End Control Scheme

The large number of additional sensors required by the conventional regenerative CHB front ends with respect to DFE-CHB affects the reliability and the cost of the regenerative CHB converter. In addition, embedding additional sensing and control circuitry to the densely-packed power cell operating in harsh conditions, such as elevated temperatures, compromises power cell circuitry reliability. To tackle these challenges, chapter 7 proposes a reduced sensor count centralized CHB front end control schemes to achieve minimum modifications to the existing DFE CHB control scheme. Instead of relying on secondary voltage sensors for input voltage synchronization, a transformer model to provide the angle information for the cell front end controllers has been proposed. In addition, detailed signal flow and control tasks schematics for proposed centralized current controlled PWM based AFEs,

voltage angle controlled PWM based AFEs, delay angle controlled grid or near grid switching frequency FEs, and voltage angle controlled grid or near grid switching frequency FEs have been presented. Moreover, detailed discussion about communication requirements between the central controller and the power cells have been included. 9-cell CHB system simulation and experimental studies have been performed to validate using a centralized transformer model for input voltage synchronization instead of secondary voltage sensors despite existence of angle tolerance. Through adopting combining voltage angle based or delay angle based front ends controllers with centralized input voltage synchronization the number of sensor can be reduced from 54 secondary sensors (27 voltage sensors and 27 current sensors) to zero.

## 8.2. Future Work

To extend and further validate the proposed work, future work considers operational conditions that were not covered in the current work. In addition, as discussed in Chapter 2, addressing long-term reliability issues can be done either in the design stage or in the field operation. The thesis work has considered designing control schemes to reduce stresses in the field. The future scope is also to prevent

power cells failures before happening through condition-based and predictive methods. The future directions can be summarized as:

- Operation the experimental prototype at full regenerative motor power.
- Experimental implementation of the proposed algorithms at full regenerative motor power, and under various system disturbances.
- Research and development of condition-based and predictive methods for early detection of degradation and anomalies.

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