Advanced Multilevel Topologies and Control for EV Ultra-Fast Charging Applications

ADVANCED MULTILEVEL TOPOLOGIES AND CONTROL FOR EV ULTRA-FAST CHARGING APPLICATIONS

BY

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To My Parents

ABSTRACT

The inevitable choice for the automotive industry to suppress the greenhouse gas emissions is zero-emission vehicles such as battery electric vehicles. Some of the main barriers regarding the adoption of electric vehicles are range anxiety, and lack of charging infrastructure, which can be addressed by ultra-fast chargers or charging stations. The conventional ultra-fast chargers are low-voltage (LV) connected through line-frequency transformers, which pose disadvantages such as low efficiency, high cost, and large footprints. The medium-voltage (MV) connected charging station is proposed by the researchers to overcome the challenges regarding the conventional chargers by eliminating the line-frequency transformer and direct connection to the medium voltage.

The most challenging part of the medium-voltage ultra-fast chargers is the AC/DC stage connection to the medium voltage. Different medium-voltage multilevel converters have been proposed to facilitate the direct connection to the medium-voltage grid. However, disadvantages such as a high number of components and control complexity weaken the strength of medium-voltage connected stations.

The main focus of this thesis is on novel advanced medium-voltage multilevel topologies and control techniques for medium-voltage connected ultra-fast EV charging applications. First, a novel controller based on SPWM is proposed to control the flying capacitor voltages of a four-level T-type Nested Neutral Point Clamped (NNPC) topology. Second, a new five-level T-type NNPC topology is proposed that has a minimum number of components in comparison to other existing five-level topologies. To extend the voltage and power rating, a novel seven-level topology is proposed that has the lowest number of components in comparison to other existing topologies. Moreover, three different controllers are developed to control the voltages of the seven-level topology based on Model Predictive Control (MPC), where the challenges regarding significant computational burden and weighting factor elimination are addressed.

Finally, an MV-connected ultra-fast charging station architecture is proposed, where the proposed seven-level topology is considered as the AC/DC stage. Comparison of the proposed topology to the LV-connected stations shows that the efficiency, cost, and power quality of the charging stations can be improved significantly.

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Finally, special thanks must go to my dearest parents. I would like to thank them for their endless love, care, and support throughout my entire life.

Notation

Abbreviations

ANPC	Active Neutral Point Clamped
BEV	Battery Electric Vehicle
CCS	Combined Charging System
CHB	Cascaded Half-Bridge
CMV	Common-Mode Voltage
DAB	Dual-Active Bridge
EV	Electric Vehicle
FC	Flying Capacitor
GHG	Greenhouse Gas
HEV	Hybrid Electric Vehicle
HF	High-Frequency
HVDC	High-Voltage Direct Current
IB	Intermediate Buffer

ICE	Internal Combustion Engine
IEC	International Electrotechnical Commission
IGBT	Insulated-Gate Bipolar Transistor
L	Level
LDV	Light-Duty Vehicle
LF	Low-Frequency
LV	Low-Voltage
MMC	Modular Matrix Converter
MPC	Model Predictive Control
MV	Medium Voltage
NNPC	Nested Neutral Point Clamped
NPC	Neutral Point Clamped
PCC	Point of Common Coupling
PFC	Power Factor Correction
RMS	Root Mean Square
SAE	Society of Automotive Engineers
SHE	Selective Harmonic Elimination
SIS	Split Integrated Storage

SoC	State-of-Charge
SPWM	Sinusoidal Pulse Width Modulation
SRDAB	Series Resonant Dual Active Bridge
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
VOC	Voltage-Oriented Control
WHO	World Health Organization
ZEV	Zero Emission Vehicle

Symbols

C_{xi}	Flying capacitors capacitance
f	Fundamental frequency
i_{Cxi}	Flying capacitors current
i_{ref}	Reference current
i_x	Phase current
I_{gx}	Grid line current
J	Cost function
L	Filter inductance

m	Modulation Index
PF	Power factor
R	Load resistance
S_{xi}	Switching state
t_i	Switch dwell time
T_s	Switching period
V_{DC}	DC-link Voltage
V_{gx}	Grid voltage
V_P	Peak value of reference voltage
V_{ref}	Modulation reference voltage
V_{xN}	Phase voltage
w_{fcap}/λ	Weighting factor

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Chapter 1

Introduction

1.1 Background and Motivation

Chronic exposure to air pollution from greenhouse-gas-emitting activities is killing an estimated 7,142 Canadians a year, and 2.1 million people worldwide [1]. According to World Health Organization (WHO), in 2016 alone, some 600,000 children died from acute lower respiratory infections caused by polluted air [2], and the prediction for the future is much worse. Moreover, other harmful damages of air pollution to the environment, human health, and the economy is well-known and studied in recent years. According to Transport Canada [3], Transportation is the second-largest source of greenhouse gas (GHG) emissions in Canada. This accounts for a quarter of Canada's total GHG emissions and almost half of those emissions come from cars and light trucks.

The promising solution to overcome these challenges regarding GHG in the automotive industry is zero-emission vehicles such as Battery Electric Vehicles (BEV), and Hybrid Electric Vehicles (HEVs).

Canada is committed to decarbonizing the country's transportation sector and becoming a global leader in zero-emission vehicles. That is why the Government of Canada has set ambitious federal targets for zero-emission vehicles (ZEV) reaching 10% of new light-duty vehicles (LDV) sales per year by 2025, 30% by 2030, and 100% by 2040 [4], however, at the current pace, Canada is not on track to achieve these goals [5]. According to Transport Canada, without any further action, the achievable selling targets for zero-emission vehicles are sales of 4% to 6% of all new light-duty vehicles purchased by 2025, 5% to 10% by 2030, and 48 % by 2040 as can be seen in Figure 1.1. Therefore, significant efforts are required to achieve the selling targets set by the government of Canada.

It is well-known that the main barriers regarding wide EV adoption by society are high cost, range anxiety, and lack of charging infrastructures. The last factor is one of the main barriers since it significantly affects the other barriers. Without low-cost EV charging stations across the country, the range anxiety and the high cost of EVs cannot be addressed.

Figure 1.1 Selling targets of ZEVs in Canada without any further actions [3]

EV chargers are mainly divided into two main categories, AC and DC chargers, where the formers are low-power EV chargers that are mounted inside the vehicle and only require to be connected to the power outlets. However, the charging time with AC chargers can take up to several hours. Here is where the DC chargers also called fast/ultra-fast EV chargers come into play, where the chargers are at fixed locations and provide DC power which is fed directly to the EV batteries and can reduce the charging time as low as 30 minutes. Therefore, having a vast number of ultra-fast EV charging stations across the highways is a necessity to address the charging time and range anxiety challenges.

All of the ultra-fast EV chargers in the market are connected to the Low-Voltage (LV) grid through line-frequency transformers, which transform Medium-Voltage

(MV) to LV and provide galvanic isolation between the chargers and the grid. Then, the isolated AC voltage is transformed to a DC voltage by AC/DC power converters, and lastly, the DC voltage is fed through DC/DC converters to the EV batteries.

The main challenge of this structure is its high cost and volume due to the bulky, expensive, line-frequency transformer, and low efficiency due to the significant current required to deliver high power to the EV batteries. To overcome these challenges, an MV-connected ultra-fast charger was proposed by the researchers, where the line-frequency is eliminated and the AC/DC stage is directly connected to the MV grid, and the galvanic isolation between the grid and the charger is achieved through high-frequency transformers of isolated DC/DC converters. The MV-connected ultra-fast charging leads to significant improvements in terms of cost, efficiency, and footprint in comparison to LV-connected charging by elimination of the line-frequency transformer and reduction of the required current to deliver the high power to the EV batteries. The most challenging part of this structure is the AC/DC stage, which requires to be directly connected to the MV-grid. Due to the limitation of power semiconductor devices in terms of their blocking voltage, multilevel topologies are the first choice to serve as the AC/DC stage of the MV-connected ultra-fast chargers.

Multilevel converters have gained significant attention during recent years in MV high power applications due to their advantages such as lower power loss, higher power quality, and lower voltage stress on the power semiconductor devices. Multilevel topologies were first introduced by classic converters such as Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascaded H-bridge (CHB) converters. These topologies have limitations such as a high number of devices and complex control especially when the number of voltage levels increases that limit their practical applications. Advanced multilevel topologies have been proposed to overcome the aforementioned barriers regarding the classic multilevel topologies. The main focus of this project is on advanced multilevel topologies for MV-connected ultra-fast charging applications.

1.2 Research Objectives and Contributions

The main research objective of this thesis is to enrich the research on medium-voltage high-power multilevel topologies for MV-connected ultra-fast charging and facilitate the design of low-cost, efficient, and low-volume ultra-fast EV charging stations that can eventually lead to wider adoption of EVs. This can be considered as a small step toward the path of the green automotive industry.

This thesis consists of five main contributions on advanced medium-voltage high-power multilevel topologies and ultra-fast EV charging architecture. As discussed

in the previous section, the main goal of advanced multilevel topologies is to overcome the challenges such as a high number of devices and control complexity that leads to low-cost and simple multilevel topologies.

An interesting medium-voltage high-power four-level T-type NNPC topology was proposed recently, which had the minimum number of devices in comparison to other existing advanced and classic topologies. However, the four-level T-type NNPC requires a sophisticated controller to balance its flying capacitors voltages for proper operation and equal voltage stress on the power semiconductor devices of the aforementioned topology. Therefore, a controller based on SPWM is developed to control the voltages of the flying capacitors of the four-level T-type NNPC in this thesis.

Interestingly, the four-level T-type NNPC can operate as a five-level topology by balancing the voltage of its flying capacitors at one-fourth of the DC-link voltage. The five-level T-NNPC has a fewer number of devices in comparison to other existing five-level topologies that leads to a lower manufacturing cost. However, conventional controllers based on SPWM and SVM are not able to regulate the voltages of the flying capacitors at different operating conditions such as high power factor and low-frequency operations. Therefore, as the second contribution, the five-

level T-type NNPC is proposed, where the challenge regarding its flying capacitor voltage control is addressed by an MPC-based controller.

To extend the operating voltage and power rating of the medium voltage multilevel converters and to achieve higher power quality, topologies with a higher number of levels are favorable. A seven-level topology is proposed in this thesis as the third contribution, which has the lowest number of components in comparison to existing seven-level topologies. To ensure proper operation and equal voltage stress on the active devices of the proposed topology, an MPC-based controller is developed to control the flying capacitor voltages of the proposed seven-level topology.

One of the disadvantages of the MPC-based controllers applied to multilevel topologies with a high number of voltage levels is the computational burden due to the high number of switching states. This is the main challenge regarding the MPC-based controller for the proposed seven-level topology. Therefore a reduced computational burden MPC is developed that significantly reduces the execution time of the developed controller by a simple assumption in the common-mode voltage calculation.

Lastly, an MV-connected ultra-fast EV charging station architecture is proposed based on the proposed seven-level topology as its AC/DC stage converter. The

proposed architecture has a fewer number of components in comparison to other MV-connected architectures in the literature. To demonstrate the advantage of the proposed architecture, it has been compared to two different LV-connected ultra-fast chargers in terms of cost, and efficiency, where these factors are improved significantly.

1.2.1 Publications

Journal Papers (published):

1. Chen, A. Bahrami, M. Narimani "A New Seven-Level Topology for High-Power Medium-Voltage Application," IEEE Trans. Ind. Electron, Early Access, 2020.
2. A.Bahrami, M. Norambuena, M. Narimani and J. Rodriguez, "Model Predictive Current Control of a Seven-Level Inverter With Reduced Computational Burden" in IEEE Transactions on Power Electronics, vol. 35, no. 6, pp. 5729-5740, June 2020.
3. Bahrami, M. Narimani, M. Norambuena and J. Rodriguez,"Current Control of a Seven-Level Voltage Source Inverter," in IEEE Transactions on Power Electronics, vol. 35, no. 3, pp. 2308-2316, March 2020.

4. Bahrami and M. Narimani, "A New Five-Level T-Type Nested Neutral Point Clamped (T-NNPC) Converter," in IEEE Transactions on Power Electronics, vol. 34, no. 11, pp. 10534-10545, Nov. 2019.
5. Bahrami and M. Narimani, "A Sinusoidal Pulsewidth Modulation (SPWM) Technique for Capacitor Voltage Balancing of a Nested T-Type Four-Level Inverter," IEEE Trans. Power Electron., vol. 34, no. 2, pp. 1008–1012, 2019.

Journal Papers (under review):

6. A. Bahrami, M. Narimani "A New Medium-Voltage Connected Ultra-Fast EV Charging Station Architecture," IEEE Trans. Industry Applications, 2021.

Conference papers:

7. Bahrami, G. Chen and M. Narimani, "Sinusoidal PWM for Flying Capacitor Voltage Balancing of a Six-Level Inverter," IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal, 2019, pp. 1979-1984.
8. Bahrami and M. Narimani, "Capacitor Voltage Balancing of a Nested T-type Four-level Inverter Using Space Vector Modulation," in Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, 2018, vol. 2018-March, pp. 1668–1672

1.3 Thesis Outline

Chapter II is regarding the ultra-fast EV chargers. First, the fundamentals of EV charging and definitive standards regarding charging levels are reviewed. Second, the different types of EV charging stations, AC-connected and DC-connected, and their advantages and drawbacks are discussed. Moreover, the LV and MV-connected charging station architectures in the literature are reviewed and their strength, and weaknesses are discussed.

In Chapter III, a brief review has been done on multilevel topologies. First, the applications and advantages of multilevel inverters are explained. Second, the classic multilevel topologies and their drawbacks are investigated. Moreover, the advanced multilevel topologies and the modulation techniques to generate the gating signals for their power semiconductor devices in the literature are reviewed to identify the knowledge gap and drawbacks of these topologies.

In Chapter IV, a capacitor voltage balancing scheme based on SPWM is developed to control the flying capacitor voltages of the four-level T-type NNPC, and the five-level T-type NNPC topology is proposed alongside the MPC-based controller to balance its flying capacitor voltages. In this chapter, the operation principle and advantages of the four-level and five-level T-type NNPC are discussed, while simulation and experimental results are provided to evaluate the performance

and demonstrate the feasibility of the developed controllers and proposed five-level T-NNPC topology.

In Chapter V, the seven-level topology with a minimum number of components is proposed. First, the operation principles and advantages of the proposed topology are discussed. Then, the mathematical model required to develop the controller of the proposed topology is determined. Moreover, the MPC-based controller and reduced computational MPC-based controllers are developed to control the flying capacitors of the proposed topology. The performance and feasibility of the developed controllers and the proposed topology are evaluated by simulation and experiment studies.

In Chapter VI, an MV-connected charging station architecture is proposed, where the seven-level topology in Chapter V is employed as its AC/DC conversion stage. A controller for the proposed seven-level topology as the AC/DC and power factor correction (PFC) stage of the charging station is developed to control the DC-link voltage and adjust the power factor of the charging station. In the end, the cost, and efficiency of the proposed architecture are compared to two different case studies where three-phase PFC converter and four-level T-type NNPC converters are considered as the AC/DC stage of an LV-connected charging station.

In the last chapter, Chapter VII, the conclusion of the research in this thesis is discussed alongside the possible steps to continue this work in the future.

Chapter 2

Ultra-Fast Chargers for Electric Vehicle Applications

2.1 Introduction

Hydrocarbon fuels are required to drive conventional vehicles with an internal combustion engine. These fuels are expensive, irreversible, and combustion of them causes air pollution, which leads to global warming, and can be harmful to humans, and the environment. The inevitable choices for the future, to overcome these concerns, and lowering the dependence on hydrocarbon fuels, are full or hybrid electric vehicles where electrical energy stored in the batteries is used for propulsion [6]. As shown in Figure 2.1, the approximate number of EVs sold worldwide until 2019 is 7.2 million vehicles, while in 2020 alone 3 million units are sold, and the projected growth would be 130 million by 2030 [7]. The predicted growth of selling targets shows the importance of finding solutions for the EV industry challenges.

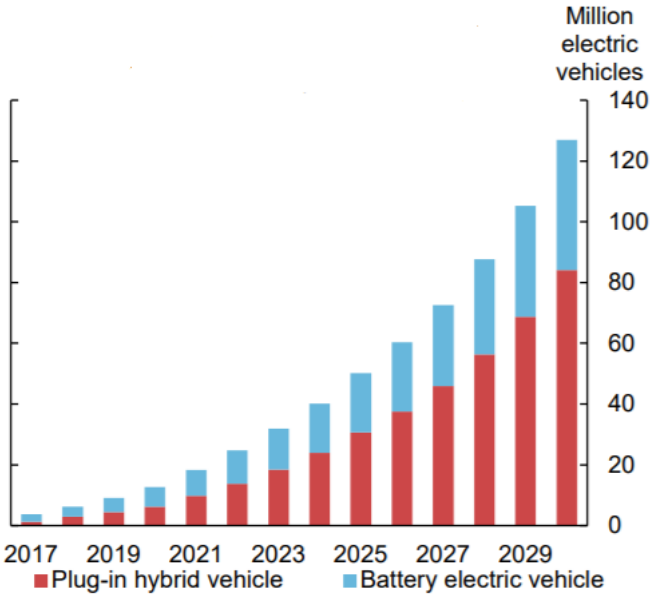


Figure 2.1 The predicted number of EVs sold worldwide by 2030 [7]

The challenges facing EV growth can be mentioned as; high battery cost, range anxiety, charging time, and lack of charging infrastructures [8]. The challenges regarding charging time and lack of charging infrastructures can be addressed by ultra-fast EV charging stations. In this chapter, a review have been done on ultra-fast EV chargers to investigate the benefits and challenges of this research topic.

2.2 EV Charging Fundamentals

EV chargers are mainly categorized into AC and DC charging systems. AC charging systems are implemented by charging units mounted inside the EVs, connected to AC voltage power-sockets, while DC charging systems are referred to off-board charging units mounted at fixed locations that provide DC power and are connected to the EV through DC voltage terminals [9]. Ultra-fast EV chargers are based on

DC-charging systems since high charging power levels increase the weight and volume of the charging units, where it is not practical to be mounted inside the EVs.

2.2.1 Charging level standards

Definitive standards regarding EV charging power levels have been proposed by the International Electrotechnical Commission (IEC), CHadeMO (Japan), and Society of Automotive Engineers (SAE) also called Combined Charging System (CCS) usually used in Europe and North America. As shown in Table 2.1 Fast DC charging levels also called Ultra-fast charging is defined for chargers with up to 350/400 kW charging power.

TABLE 2.1 CHARGING LEVEL STANDARDS

Standard	Version/power class	Max Power rating (kW)
IEC	AC level 1	4-7.5
	AC level 2	8-15
	AC level 3	60-120
	Fast DC charging	200
CHAdeMO	1.0	62.5 (500 V × 125 A)
	1.2	200 (500 V × 400 A)
	2	400 (1 kV × 400 A)
CCS	DC 5	5 (500 V × 10 A)
	DC 10	10 (500 V × 20 A)
	DC 20	20 (500 V × 40 A)
	FC 50	50 (500 V × 100 A)
	HPC 150	150 (500 V × 300 A, 920 V × 163 A)
	HPC 250	250 (500 V ×500 A, 920 V × 271 A)
	HPC 350	350 (500 V × 500 A, 920 V × 380 A)

The main limitation of EV charging power capability is regarding the charging cable weight and EV battery C-rate. The charging cable weight versus the power delivered to the battery pack is shown in Figure 2.2.

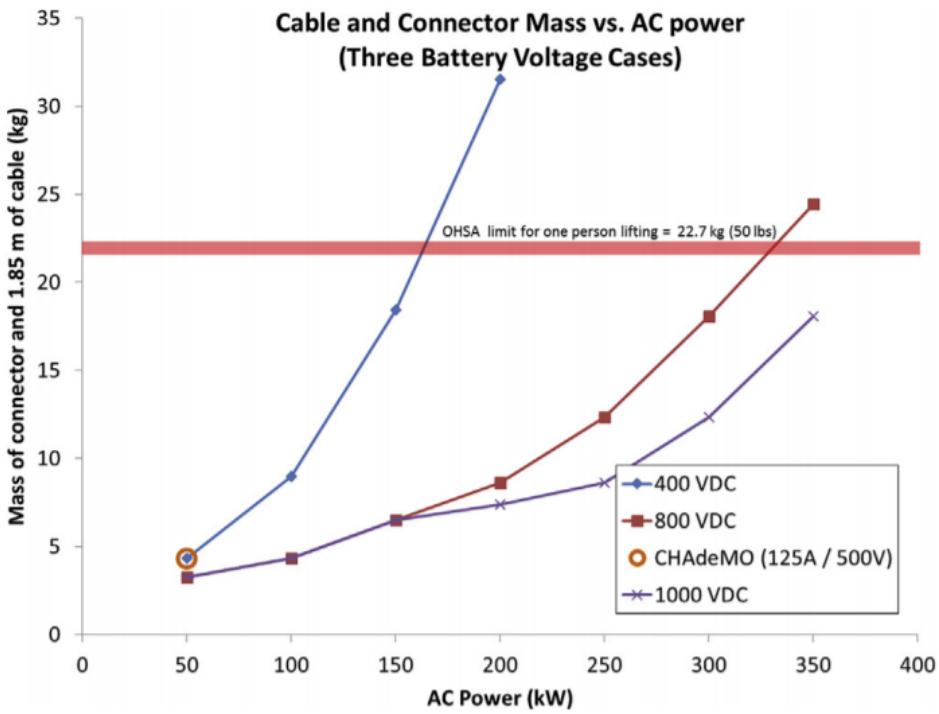


Figure 2.2 The charger cable weight vs. the charging power [10]

As can be seen, there is a safety limit for charging cable that can be lifted by one person which is around 22 kg. In vehicles with 400 V battery packs, the cable weight hits the limit where the power is around 150 kW, and for 800 V battery packs the limit would be close to 350 kW. There are some solutions such as liquid-cooled cables or robotic charging cables which would increase the manufacturing cost. Both approaches have been used by some companies such as ABB. Liquid-

cooled cables in Terra HP products of ABB (350 kW), and robotic charging for heavy-duty vehicles such as E-bus (400 kW) are among those examples [10].

TABLE 2.2 CHARGING RATE OF BATTERY CELLS IN EVS; TODAY VS. FUTURE [11]

	Today			Future
Charger Voltage	400 V	400-100 V		
Vehicle	400V, 125 A, 50 kW 400 V, 350 A, 140 kW	600V,400A,240 kW	800V,400A,320 kW	1000 V, 400 A, 400kW
Battery	1.5-2 C	2-3.3 C	3.3 – 4.6 C	4.6 -6 C

The other limitation is the charging rate of battery cells. As shown in Table 2.2, today for 400 V battery packs the charging rate is around 1.5 to 2 C-rate which limits the charging power to 140 kW, and for the 800V battery packs which are already released in the market would be around 350 kW and 3.3-4.6 C-rate. Moreover, it is predicted that the charging rate in the future can be as high as 6-C rate.

2.2.2 Off-board Chargers Building Blocks

The building blocks of today's off-board chargers are shown in Figure 2.3. As can be seen, there are three main stages for each charger unit. The first stage is the line-frequency transformers which is responsible transfer the Medium-Voltage (MV) grid, and is typically between 13.8-4.16 kV to Low-Voltage (LV) grid that is around

480 V. Moreover, the transformer provides galvanic isolation between the grid and the charger/charging station.

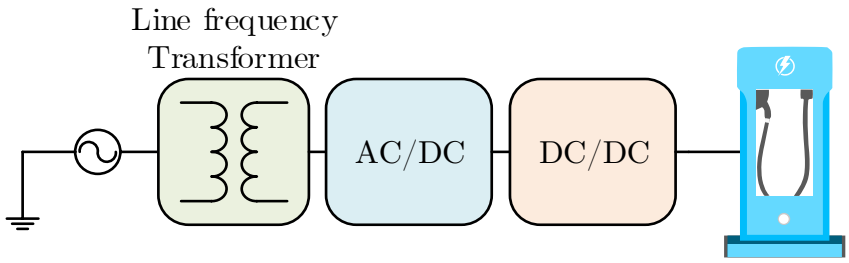


Figure 2.3 Off-board charger building blocks

The second stage is the AC/DC converter, which rectifies the input AC voltage, and serves as a Power Factor Correction (PFC) stage to ensure efficient operation of the charger/charging station. The conventional topology for this stage is a three-phase boost converter. The third and last stage is the DC/DC converter, which is responsible for providing the DC voltage and current required to charge the EV battery. Typically the battery must be floating with respect to the charger/charging station equipment. Therefore, isolated DC/DC converters such as Dual Active Bridge (DAB), and Series Resonant DAB (SRDAB) are employed for this stage.

2.3 Ultra-Fast EV Chargers

As discussed, ultra-fast chargers are referred charging powers up to 400 kW according to definitive standards such as CHAdeMO, and CCS. In this section, first, the necessity of ultra-fast chargers is discussed, then the ultra-fast chargers in the

market are investigated in terms of specifications, and finally, the main architectures of the ultra-fast EV charging stations are reviewed.

2.3.1 The Necessity of Ultra-Fast EV Chargers

The two main challenges of EVs worldwide adoption are the limited range of EVs causing the range anxiety and charging time of the EVs, which is significantly longer than fuel filling of the ICE vehicles. The EVs available in the market with a driving range higher than 200 miles, and the time required to recharge the battery to add an extra 200-mile range with different available chargers is shown in Figure 2.4. As can be seen, charging the EVs with level-1 charging can take 7-8 hours, and DC-fast charging can take as high as 72 or 27 minutes which is still higher than the time required to full the ICE vehicle's gas tank.

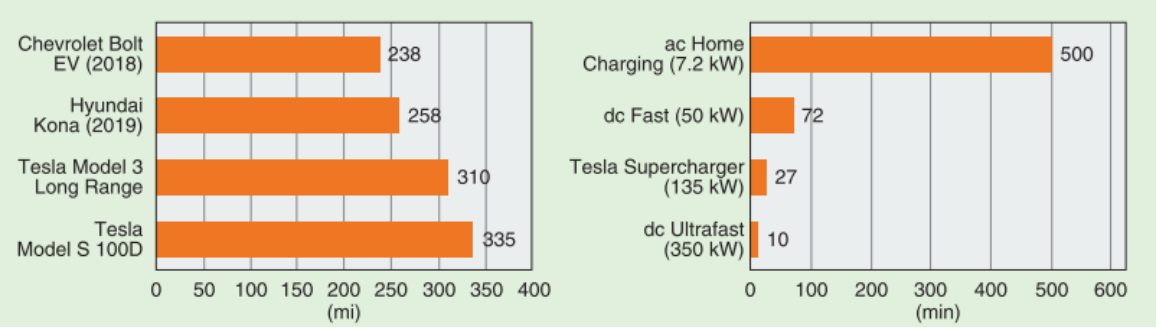


Figure 2.4 The EVs with a driving range of more than 200 miles, and the charging time required to add an extra 200 miles range [12]

As can be seen in Figure 2.4, the ultra-fast chargers are able to add an extra 200-mile range in only 10 minutes, which is closer to the time required to full the ICE vehicle's gas tank.

Therefore to address the challenges regarding range anxiety, and charging time, various ultra-fast EV charging stations are required on highways between the cities with approximately 200-mile distance to overcome one of the barriers in the path of EV worldwide adoption.

2.3.2 Ultra-fast EV Chargers in the Market

Many companies recently have manufactured ultra-fast EV charging systems up to 350 kW. The list of the companies and the specification of their charging systems are shown in Table 2.3. An interesting aspect revealed by some companies' products is the modularity of the chargers. For instance, ABB terra which is a 50 kW charger contains five 10 kW modules that provide the 50 kW output, and Tesla V.2 charger which delivers 135 kW is constructed by twelve 11 kW modules, which these modules are used as onboard chargers in Tesla EVs as well. These examples demonstrate the modularity advantages of chargers in terms of cost, efficiency, and performance.

As can be seen in Table 2.3, all the chargers available in the market are low-voltage connected systems, where the input voltage is either 480 or 400 V depending

on the electrical grid that the charger is used. The challenge facing this approach is the high input current of these systems which decreases the efficiency of the overall system and challenges the charger's design due to high current stress on the chargers devices such as input filter and active switches such as IGBT and MOSFET used in the AC/DC stage of the charger. This shows an opportunity to increase the input voltage to lower the current rating of the station and increasing the efficiency. This has been done by proposing a direct connection of the charger to the MV grid and is investigated in detail later in this chapter.

TABLE 2.3 ULTRA-FAST CHARGERS' SPECIFICATION IN THE MARKET

Manufacturer/Model	Rated Power	Module Power	Input Voltage	Output Voltage	Output Current	Efficiency
ChargePoint Express Plus	500 kW	31.25 kW	-	200-1000	-	-
ABB Terra HP	350 kW	-	400 V	150-920 V	375 A	95%
Veefil-PK	350 kW	-	480 V	Up to 920 V	Up to 500 A	96%
EVbox EVtronic	350 kW	-	400 V	50-950 V	500A@700V 368A@950V	95%
Hypercharger	300 kW	-	480/400	150-1000 V	500 A	94%
Tesla V2. Supercharger	135 kW	10 kW	200-480 V	50-410 V	330 A	92%
EVteQ	200 Kw	10 kW	380 V	350-750 V	200 A	-
PhiHong	350 kW	-	400	150-950V	500A@720V, 379A@950V	94.68%

2.3.3 AC and DC Connected Charging Stations

It is well known that ultra-fast chargers in most situations should form a charging station such as gas stations available for ICE vehicles nowadays. By this consideration, an ultra-fast charging station can be categorized into AC-connected, and DC-connected structures as shown in Figure 2.5 and Figure 2.6.

As can be seen in Figure 2.5, all the charging units are connected to a common AC bus. Therefore each charging unit has its own AC/DC converter.

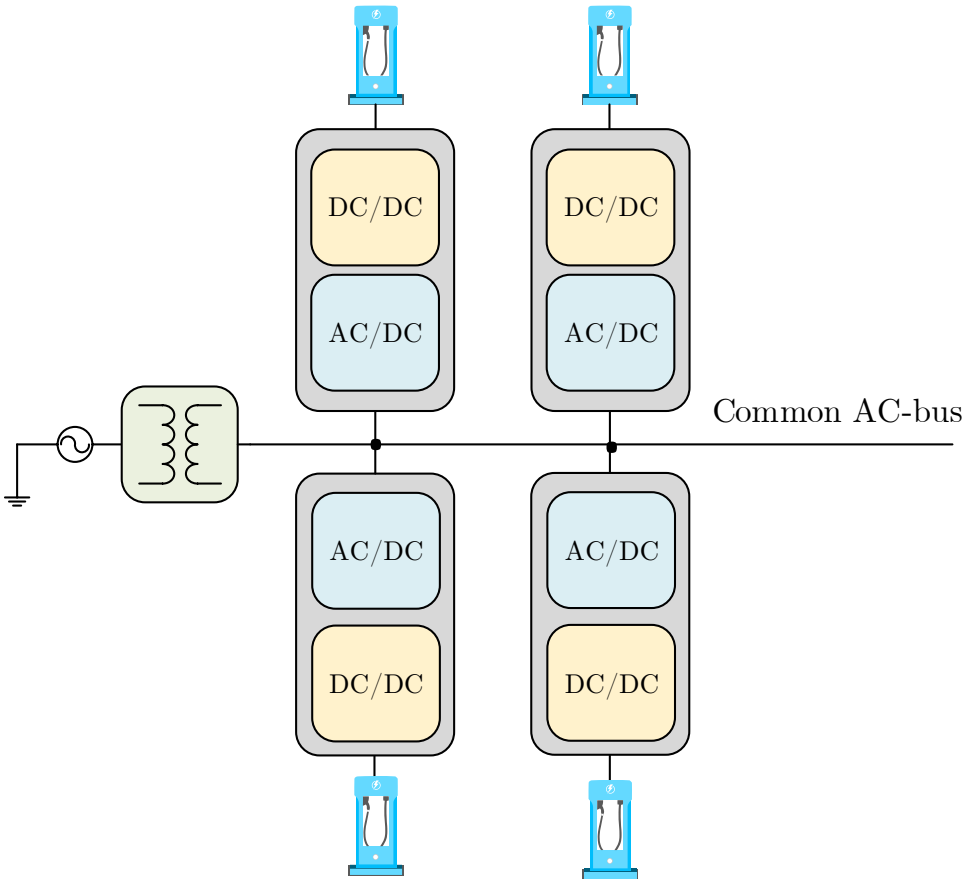


Figure 2.5 AC-connected charging station

The advantages of this approach include; the maturity of the inverter technology, availability of the ac switchgear and protective devices, and mature standards for the ac power distribution systems. Despite the aforementioned advantages, there are some technical disadvantages such as; increased complexity and cost due to the high number of conversion stages [12].

The other structure, the common DC bus, as shown in Figure 2.6, has a central AC/DC which forms a common DC bus where charging unit is connected to it through DC/DC units.

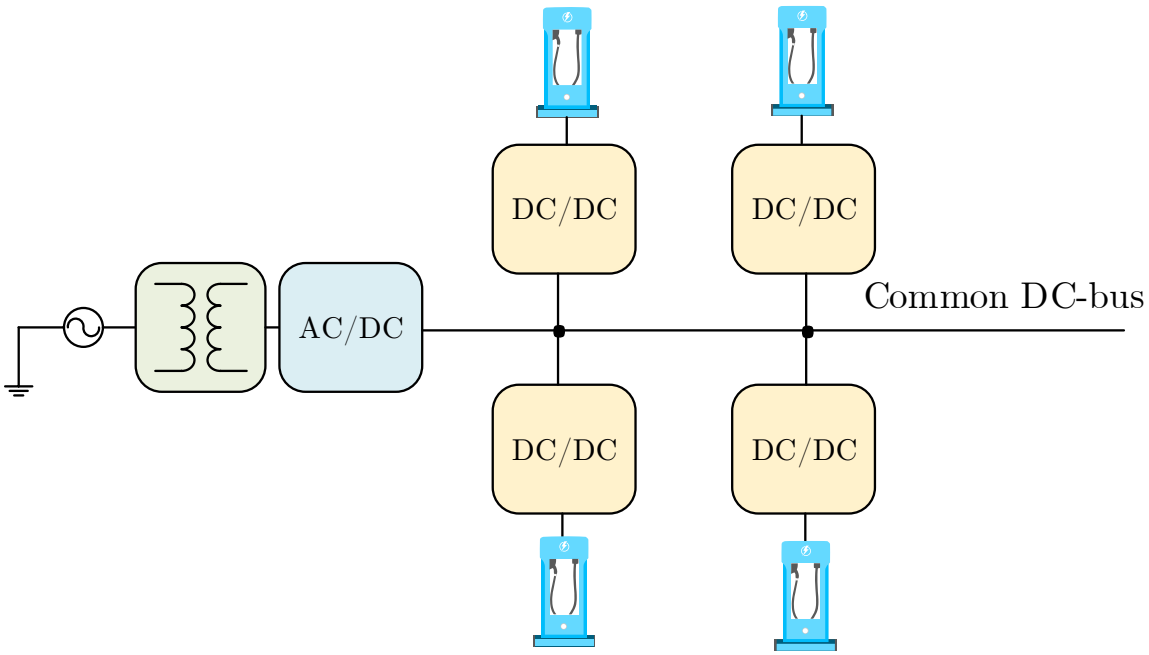


Figure 2.6 DC-connected charging station

The advantages of this structure in comparison to the previous structure can be mentioned as; fewer conversion stages, single grid connection, absence of reactive power in DC systems, and the possibility to derate the central AC/DC unit due to load diversification in EV charging. The challenge for this architecture is dc protection and DC metering, and there are no established standards for protection coordination in the DC-connected EV charging stations. Also, this structure requires fast fault clearance due to the limited inertia of the system [12].

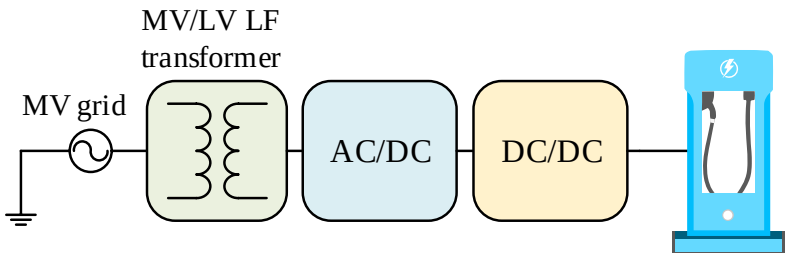
Another challenge facing the DC bus structure is the reliability of the overall system since a fault in the central AC/DC unit can interrupt the functionality of the whole station. However, on the other hand, possible faults on the grid in the common AC bus structure are more likely to happen compared to the DC bus structure since there is more grid connection in the common AC bus structure.

Currently what is observed in the market and implemented by different companies is the common AC bus structure due to the aforementioned challenges for the common DC bus structure.

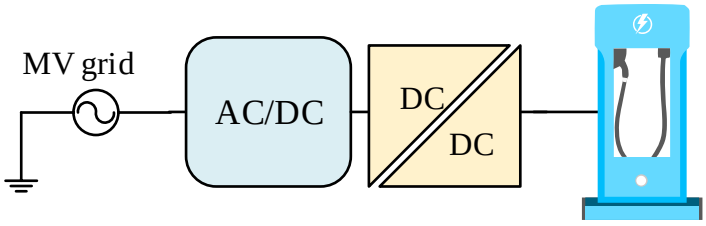
Due to the technical advantages of the DC-connected systems over the AC-connected systems, the former structure is chosen for further analysis in the continuation of this project. Since the challenges regarding protection, metering, and fault clearances can be solved in the future.

2.4 MV and LV Connected Ultra-Fast Charging Stations

As discussed in Section 2.3.2, the ultra-fast chargers in the market are connected to the LV grid through an MV/LV line-frequency transformer as shown in Figure 2.7 (a), where due to the high current required for ultra-fast charging, the efficiency of these chargers are limited to around 92% [12]. To overcome this challenge, an MV-connected architecture was first proposed in [13], as shown in Figure 2.7 (b), where the line-frequency is eliminated and the ultra-fast charger is directly connected to the MV grid. This structure is also called the Solid-State Transformers (SST), which has been proposed for different MV-connected applications.



(a) LV-connected



(b) MV-connected

Figure 2.7 MV and LV connected ultra-fast charging station

In the LV-connected stations, the galvanic isolation is achieved through the Line-Frequency (LF) transformer, where the galvanic isolation in MV-connected station is achieved through High-Frequency (HF) transformers in the DC/DC stage, and the AC/DC stage of the charging station is directly connected to the MV-grid.

2.4.1 Benefits of MV-Connected Charging Stations

Eliminating the line-frequency transformer and direct connection to the MV grid introduces several advantages for the ultra-fast charging stations in terms of efficiency, volume, and cost. As investigated in [12], the power losses can be halved and the efficiency can be increased from 94% to 97.6%, while the volume can be reduced up to 30 times. Moreover, due to the elimination of bulky, expensive transformers, the manufacturing cost of the charging station can be almost halved and decrease from $75,000 to $35,000. The summary of the comparison between the MV and LV connected stations is shown in Figure 2.8.

On the other hand, there are some challenges regarding MV-connected fast chargers, for instance, fast protection for overvoltage, and short circuits, lack of fast circuit breakers for MV connection, and lack of any standards regarding MV connected chargers [12].

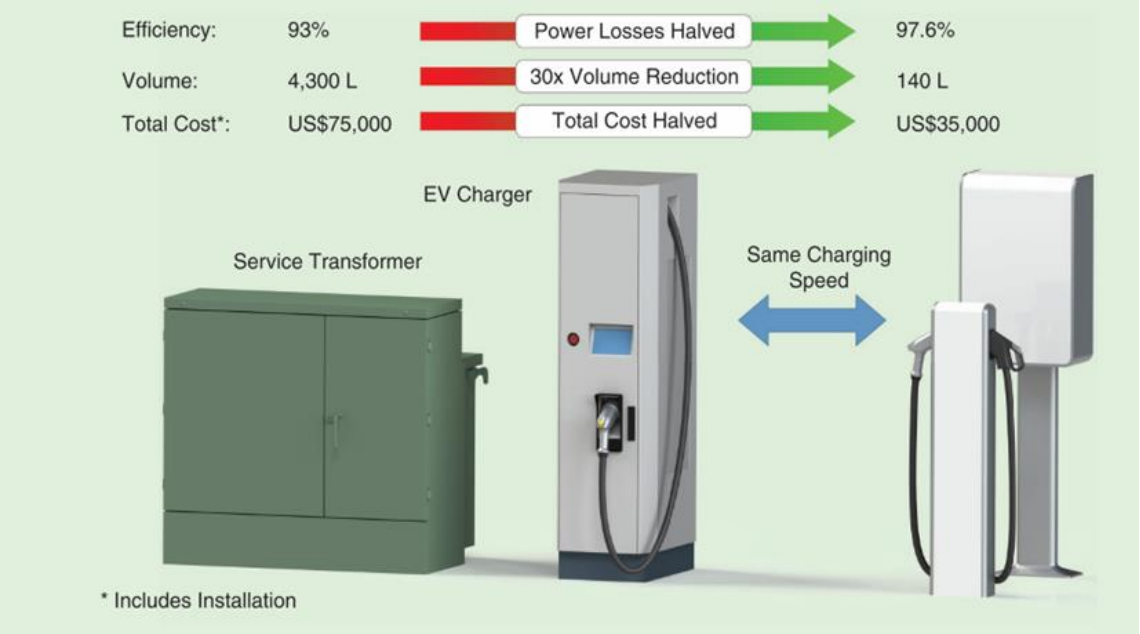


Figure 2.8 MV-connected charging stations vs LV-connected charging stations [12]

2.4.2 Review of LV-Connected Ultra-Fast Chargers

In this section, a review has been done on some of the studied LV-connected ultra-fast chargers to investigate different architectures of these stations and identify their strengths and weaknesses.

In the literature such as [14], and, [15] a power architecture for a fast DC charging station is proposed where the low voltage grid (480 V AC), renewable energy sources such as photovoltaics, and the EV charger are connected to a common DC-bus, as shown in Figure 2.9. The renewable energy source can be used for EV charging and grid support, however, the ultra-capacitors capacity is limited which limits the grid support in many scenarios. The main challenge for using the

architecture shown in Figure 2.9 is the high conduction loss for ultra-fast charging, and increased stress on the LV grid.

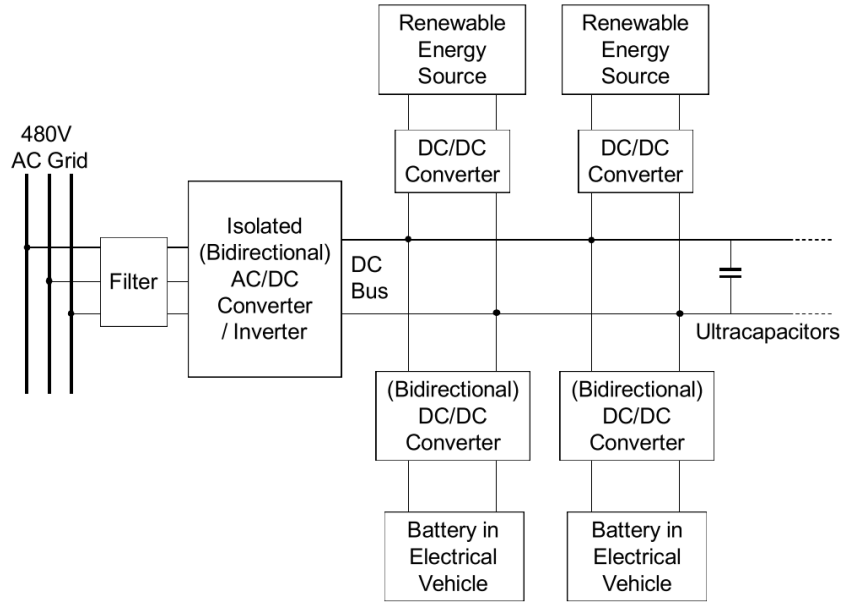


Figure 2.9 Ultra-Fast charging station architecture based on a common DC-bus connected to LV grid [15]

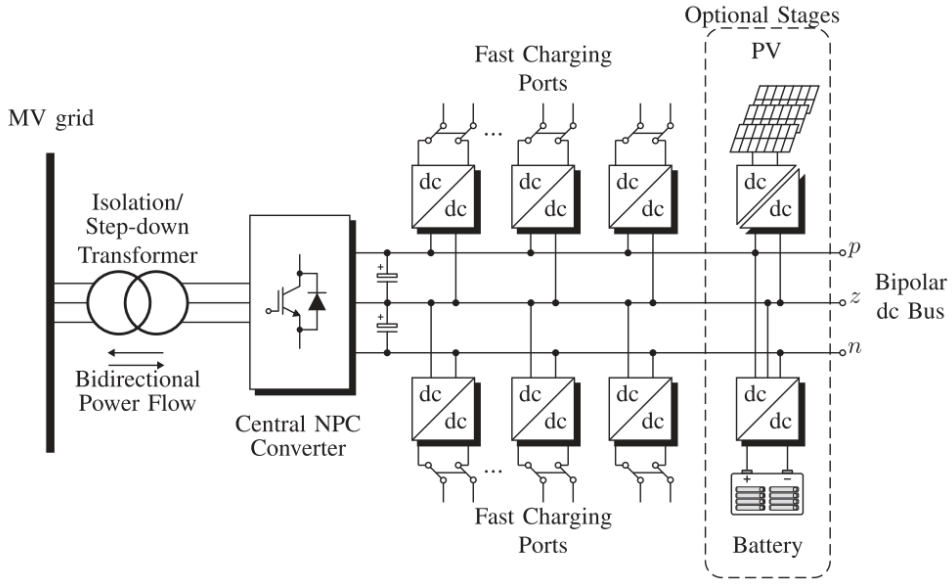


Figure 2.10 Fast charging station using a three-level NPC and bipolar DC bus [16]

In [17], a DC-connected ultra-fast charging station architecture has been built based on a central three-level Neutral Point Clamped (NPC) converter, and a bipolar DC-bus the architecture is shown in Figure 2.10. The main advantage of this topology, reported in [17], is the use of a bipolar DC-bus where multiple DC/DC stages can be used to charge the vehicle and the possibility of connection to MV grid which can handle more power in the cost of higher central converter and transformer rating. The main challenge of the proposed architecture would be the unbalanced neutral point which cannot be resolved by the balancing techniques using modulation schemes. Therefore, an extra leg is added to the central converter which can balance the mid-point by adding a virtual impedance in any operating condition [17]. Despite the advantages, a step-down transformer is required which will be bulky and costly. Since it must handle high power flow, and since it does not have any stationary storage, the stress on the grid would be the main challenge for the proposed architecture.

In [18], the mid-point unbalance voltage of the architecture shown in Figure 2.10 is addressed by a voltage balance control and a three-level DC-DC converter connected to the bipolar DC-link which eliminates the need for an extra leg for the NPC converter. The proposed architecture is shown in Figure 2.11.

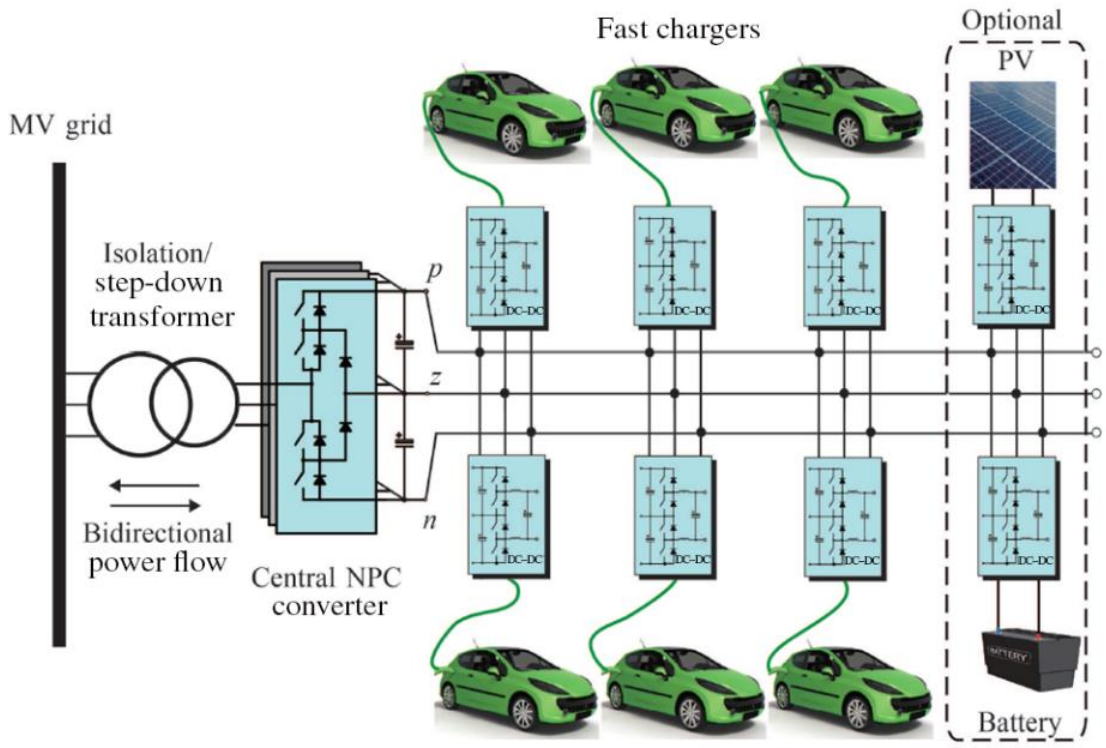


Figure 2.11 Ultra-fast charging station using three-level NPC and bipolar DC bus [18]

Using a 3L DC-DC converter can reduce the device stress and increase power rating as well as the reduction in the output filter size. Also, it is reported that the voltage balancing on the 3L DC-DC side is faster with lower fluctuation which is more suitable for fast charging applications. However, the line frequency transformer is still required for isolation purposes which is bulky and costly. Also, a circulation current flows in 3L DC/DC converter which causes higher losses and stress on the active switches.

In [19], a different architecture among the ones discussed has been proposed consisting of a three-phase active rectifier as the AC/DC stage where each phase

has three interleaved half-bridges. For the DC/DC stage, the same configuration is repeated as can be seen in Figure 2.12. It is reported that the ripple-free output current is achieved while the input current ripple is reduced. The advantage of such an architecture is its modularity due to using the standard three-phase two-level converter cell, which decreases the manufacturing cost. Also, it is reported that the filter size can be reduced by magnetic coupling among the phases. The significant disadvantage still would be the number of inductors for filtering purposes, and the high number of active switches.

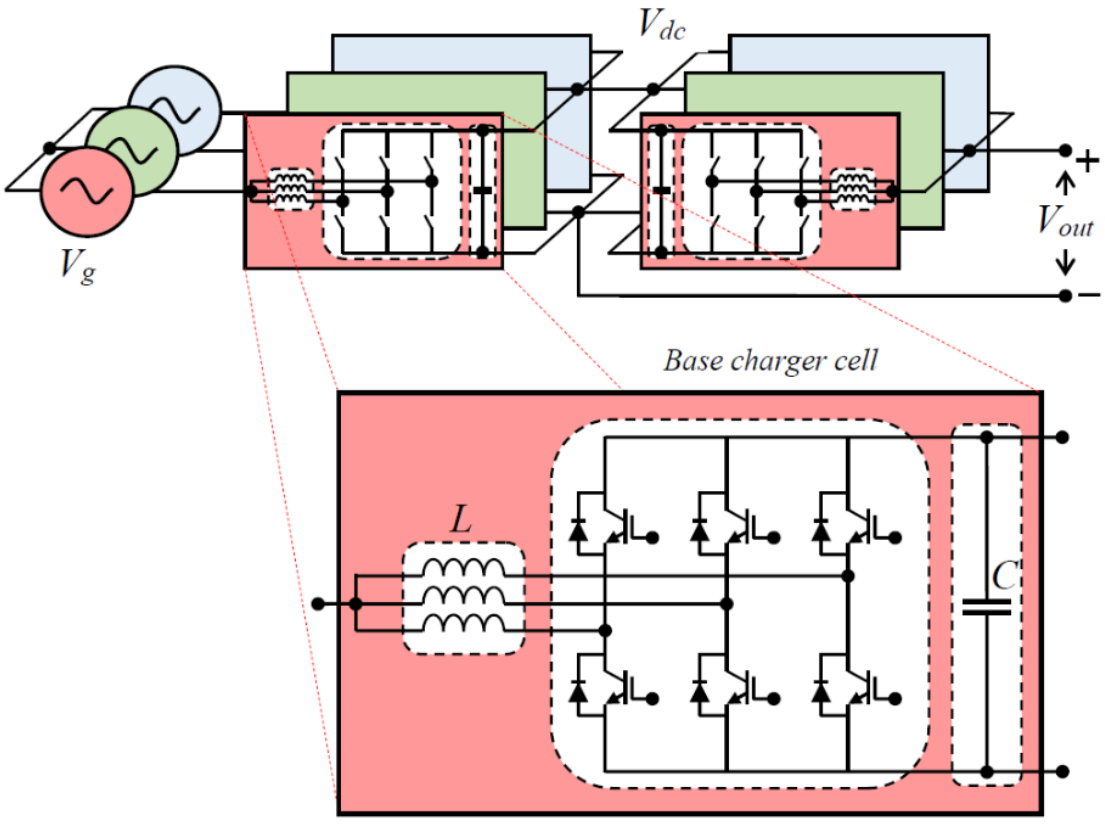


Figure 2.12 DC Fast charger using interleaved three-leg cells [19]

2.4.3 Review of MV-Connected Ultra-Fast Chargers

In this section, a review has been done on some of the studied MV-connected ultra-fast chargers to investigate the different architectures of these stations and identify their strengths and weaknesses.

In [20], it is stated that a direct connection to the MV grid (4.8 kV) for an architecture similar to the architecture shown in Figure 2.9, will reduce 90% of the conduction loss. Moreover, it is proposed that the stress caused by the MV grid on the AC/DC stage can be addressed by Modular Multilevel Converters (MMC). In addition, a battery bank as a storage element increases the grid support functionality of the fast charger. The proposed architecture in [20] is shown in Figure 2.13. As can be seen, the isolated bidirectional DC/DC converters connected to each cell of the MMC are paralleled to increase the power and reduce the current ripple. In this architecture, the line frequency transformer is avoided which is significantly cost beneficial, and smaller.

Both architectures that are shown in Figure 2.9 and Figure 2.13, by using bidirectional stages can achieve the vehicle-to-grid (V2G) function as well as other grid support functions such as reactive power compensation, harmonic filtering, and peak shaving using the storage element connected to DC-bus. However, as mentioned, the first architecture due to using ultra-capacitor would have issues

regarding this matter. On the other hand, the battery bank in the second architecture would face a significant stress since it is stated that the ultra-fast charger should be able to deliver more than 400 kW.

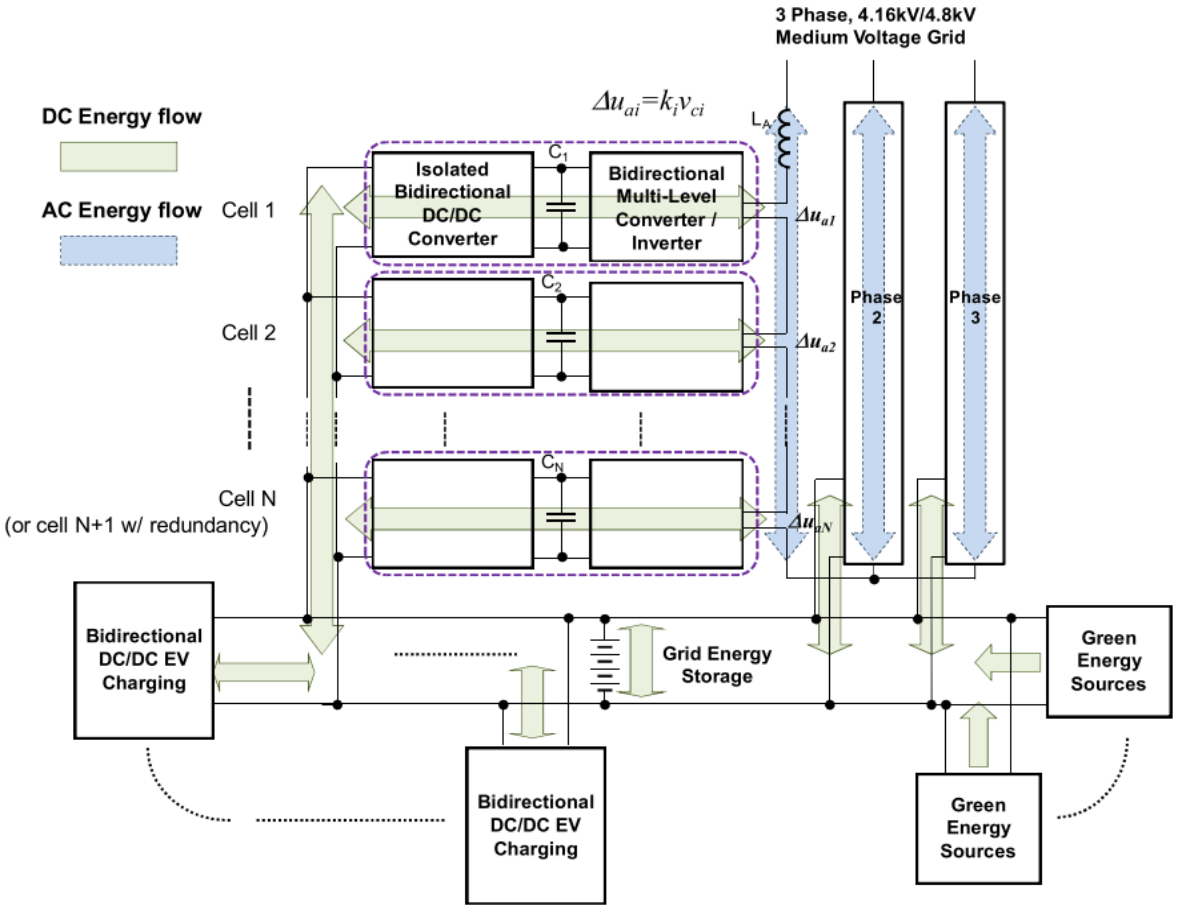


Figure 2.13 An MV-connected station with MMC as the AC/DC stage [20]

In [21], it is proposed that by considering the possibility of simultaneous charging of the vehicles in a charging station, the peak power required for charging can go up to 1,600 kW, and aggregation of power required for charging during a day from

the grid can be a large number. Therefore, a power architecture using a Medium Voltage (MV) grid is proposed which is shown in Figure 2.14.

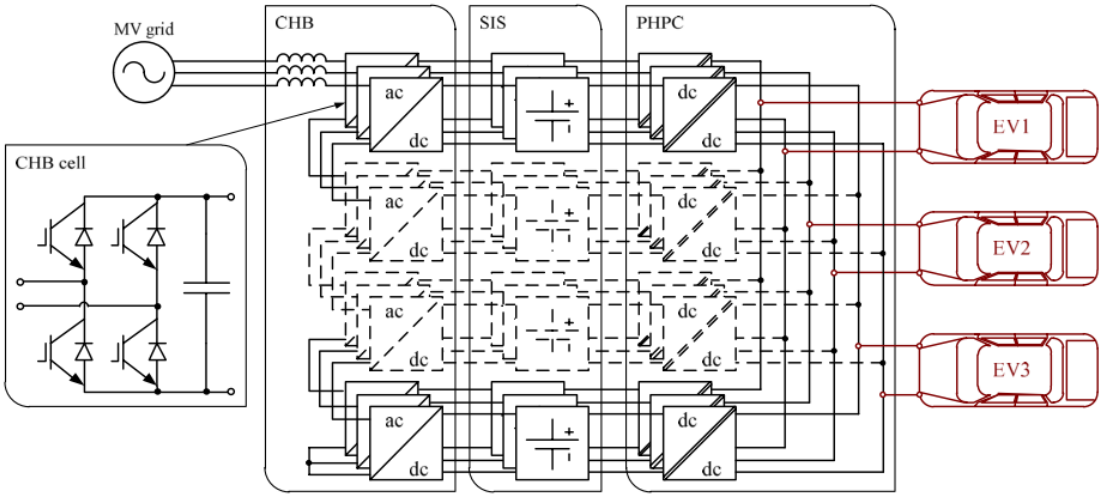


Figure 2.14 The ultra-fast charging system based on CHB converter and an intermediate buffer as energy storage elements [21]

The system has a low-power charger to limit the power drawn from the grid, an intermediate buffer (energy storage element), and a high-power charger to charge the vehicles. The reason for proposing such a system is to limit the power drawn from the grid by using the energy stored in the intermediate buffer. The CHB Split Integrated Storage (SIS) [22] multilevel topology is a good choice in terms of providing multiple Intermediate Buffer (IB) and charging ports for the vehicles, lower harmonic injection to the grid, and low stress on the active switches connected

to MV grid. However, the challenges regarding the control of such a system and balancing the buffers are not addressed.

The proposed architecture is shown in Figure 2.14 and is elaborated with more details in [23], a CHB with 13 cells per phase is designed to connect the MV grid (11 kV) to charge three EVs simultaneously, and deliver 250 kW to each vehicle by connecting the DC/DC stage in parallel. Also, the connection of the IB to each cell is discussed using either passive components forming a high-order filer or active interface converter to avoid injection of low-frequency harmonics to the IB that degrades its lifetime. It is concluded in [23] that the active cell provides more control on the power flow to charge/discharge the buffer however the passive components are more simple and cheaper. Since the control on the buffer is necessary for power management, using a buck converter is unavoidable.

In [24], the control strategies for different stages of the configuration shown in Figure 2.14 are discussed. For the active and reactive power control of the interfacing AC/DC converter with the gird, a decoupled current control is proposed. In addition, the SoC balancing control has been proposed for the energy storage element of each cell, and at the end, an EV charging control based on PI controllers are proposed. The control strategies proposed in [24] seem to be incomplete in terms

of bidirectional power control and is not well organized in terms of the SoC balancing control since different scenarios are possible during charging vehicles.

In [25], for the DC/DC stage of the configuration shown in Figure 2.14, a dual half-bridge isolated DC/DC converter is used due to its features which also enables V2G operation. It is stated that this converter is suitable to satisfy the requirements for battery fast charging such as low output ripple current, output voltage and current controllability, and galvanic isolation. Moreover, a controller based on convex optimization is proposed which is useful for surpassing the second-order harmonic coming from MMC cells.

In [26], an active connection between each submodule using a buck converter is discussed which secures an stable voltage at the output of each cell and current control for charging the stationary storage units. This will increase the complexity of the controller and the cost of the system as a buck converter is required for each cell connected to the stationary battery. Moreover, self-balancing of the storage elements is discussed in the delta connection of the CHB with the grid, in which the circulating current is used to balance the SoC of different stationary batteries of the system.

In [27], an ultra-fast charger connected to the MV is proposed using CHB topology as the AC/DC stage interfaced by the DC-link capacitor to a dual active

bridge as its DC/DC stage shown in Figure 2.15. The authors in [27], proposed a controller for the CHB that balances the DC link in both charging and discharging mode, and a decentralized controller for DABs. However, since there is no energy storage element, the grid-supported functionality does not seem to be practical since the EVs are fast-charged within a few minutes.

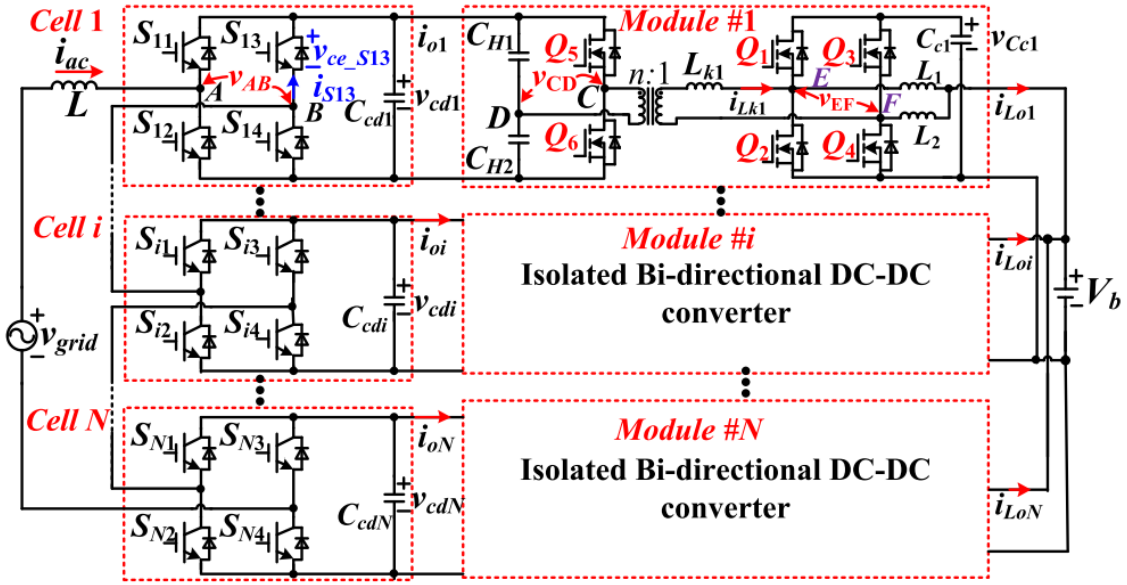


Figure 2.15 The Ultra-fast charger connected to the MV using CHB and DAB [27]

In [28], a 1 MW fast-charging station is proposed based on MMC topology as the central AC/DC unit, providing an MV DC link. The contribution of the authors is an optimization algorithm to design the MMC topology for a specific power level considering different voltage rating IGBTs, and film and electrolyte capacitors. In the design procedure, the acceptable harmonic at the PCC, cost, power density,

and the ability for reactive power injection to the grid to regulate the grid voltage is considered. It is worth mentioning that the results shown in [28], for a 1MW AC/DC unit which provides 10 kV DC link, has 90 submodules using 1.7 kV IGBTs and 90 electrolyte capacitor. These numbers seem to be extremely high which affects cost and volume, while the inductors of the system are not considered.

An interesting comparison has been done regarding three architectures for a fast-charging stations in [29], the architectures with shown in Figure 2.16.

It is based on a central AC/DC CHB topology connected to the MV grid, where the DC/DC stage configuration is different. The quadrant active bridges DC/DC [30] are connected through a common magnetic core, as shown in Figure 2.16, three bridges are the input and one bridge is LV output. It is reported in [29] that the first configuration named the individual QAB lacks natural balancing between the phases, and therefore, is not comparable to the other two configurations. For the second Paralleled QAB and third configuration called interphase QAB, it is mentioned that the efficiency and cost for the number of chargers higher than 8 are better for the IQAB topology and for lower number chargers us better for the PQAB topology. Also, the number of semiconductors in the IQAB is lower than other topologies, which will bring the power density and cost advantages. However, to reach a higher current rating, the PQAB topology is more suitable since the

DC/DC stages are paralleled at the output, which makes it a suitable topology for ultra-fast charging architecture.

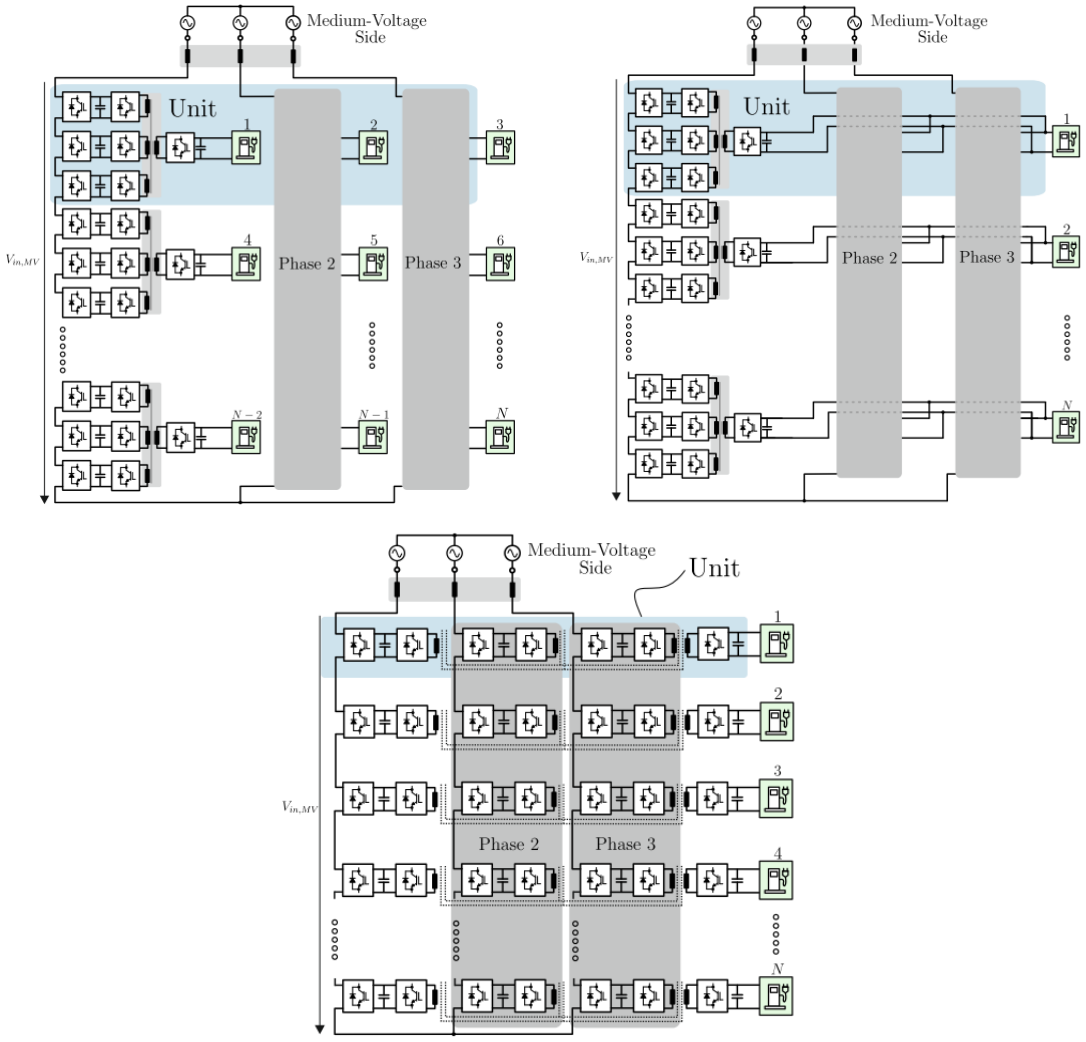


Figure 2.16 Medium voltage connected fast charger station with quadrant active bridge DC/DC stage [29]

An MV grid-connected fast-charging station is proposed in [31], where a delta connected CHB topology performs the AC/DC conversion, and DABs are paralleled at DC/DC stage to make ultra-fast charging available at one port. The authors

studied a station that is able to charge three different battery voltage ratings, as shown in Figure 2.17. The unbalanced load causes unbalanced operation of the system which is addressed by a dynamic zero-sequence current to balance the converter operation. This feature is only available at delta connected configuration. The zero sequence current injection causes an increase in the semiconductor's current rating which will impose higher costs on the system.

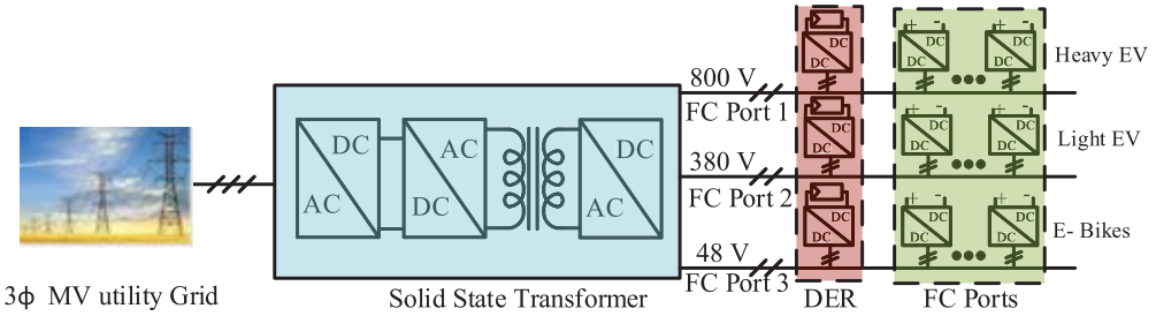


Figure 2.17 . Medium voltage connected fast charger station with different voltage rating charger [31]

A 50 kW MV connected charger is designed in [32], as shown in Figure 2.18, which is connected to a 2.4 kV grid. The input AC voltage is rectified by a diode bridge, then the DC voltage is fed to three input-series output-parallel modules. Each module consists of a three-level boost PFC stage, and a three-level NPC-based isolated DC/DC converter. The efficiency of the proposed charger is estimated to be 3.5% higher than conventional LV-connected chargers. The main challenges regarding this architecture are the switching losses associated with inner switches of the NPC and the required voltage control for the mid-point of the DC-

link. To extend the power rating of such an architecture, the number of the components will significantly increase, which introduces a disadvantage regarding the manufacturing cost.

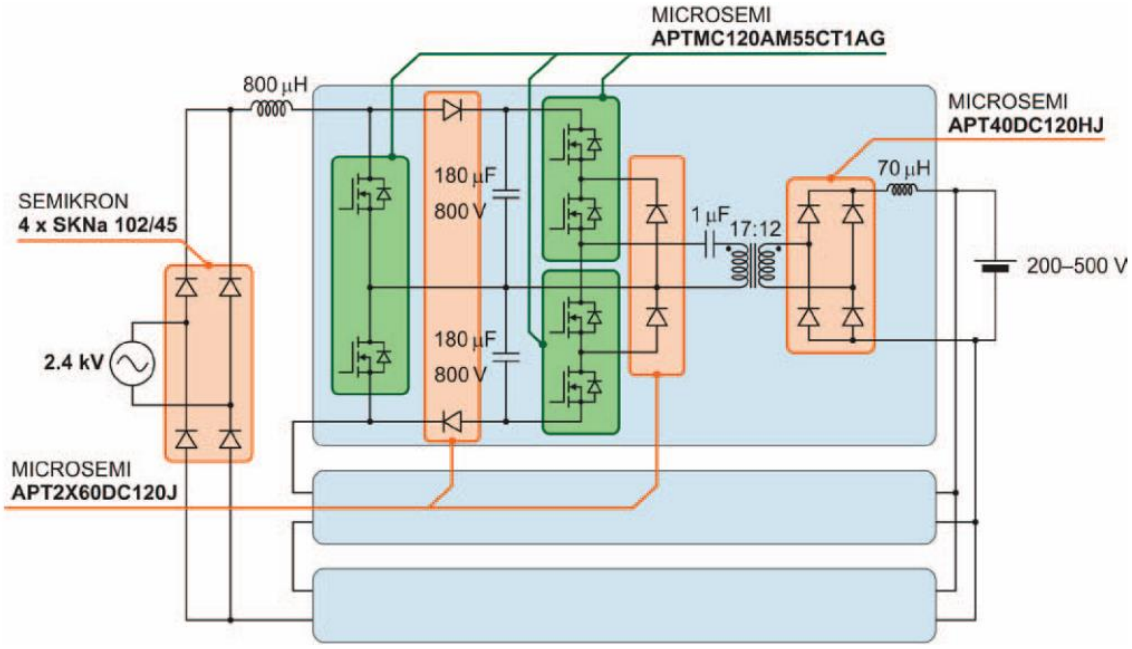


Figure 2.18 A 50 kW MV-Connected charger [32]

In [33], a 350 kW charger is designed to connect to a 12.47 kV MV grid, using 10 kV SiC modules. The architecture of the mentioned 350 kW charger is shown in

Figure 2.19 and is similar to the previous case study. The main difference is the DAB converter which is designed with a primary active NPC-based, and active switch for the second bridge to achieve soft-switching for the inner switches of the NPC. It is reported that due to hard switching of the PFC stage, a 10 kHz switching frequency is chosen for this stage. For the DC/DC stage, an optimization regarding

switching loss and leakage inductance feasibility has been done which resulted in a 25 kHz switching frequency for this stage. Moreover, it is reported that the charger has 98.1% efficiency and the power density equals 1.6 kW/L.

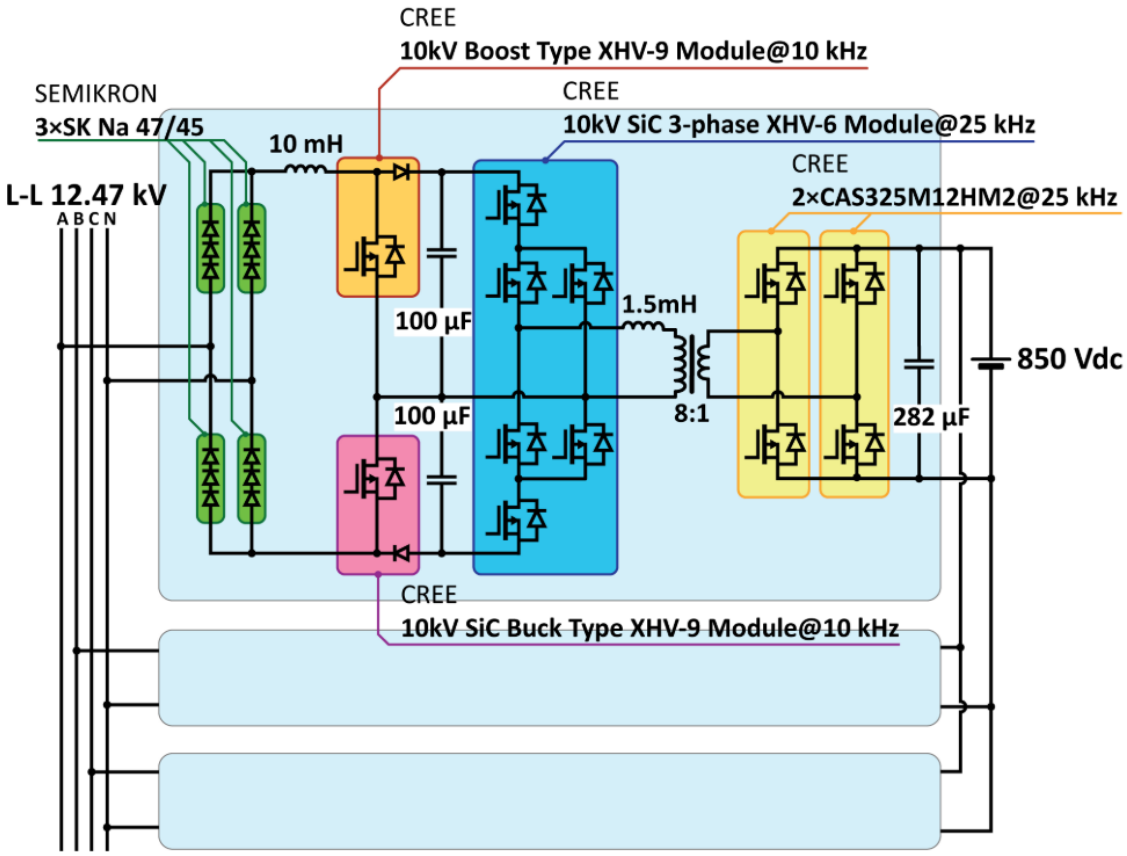


Figure 2.19 350 kW charger topology using SiC modules [33]

Delta Electronics has announced designing a 400 kW MV-connected ultra-fast charging station by 2021 [34]. The architecture of the proposed charging station is shown in Figure 2.20, where input-series output-parallel modules are used for direct connection to the MV grid (4.16/ 13 kV) to provide the common DC-link, where

EV chargers and renewable energy sources are interconnected. The common DC-link is set to be 1000 V, and the charging unit outputs 200-900 V through paralleled interleaved buck converter.

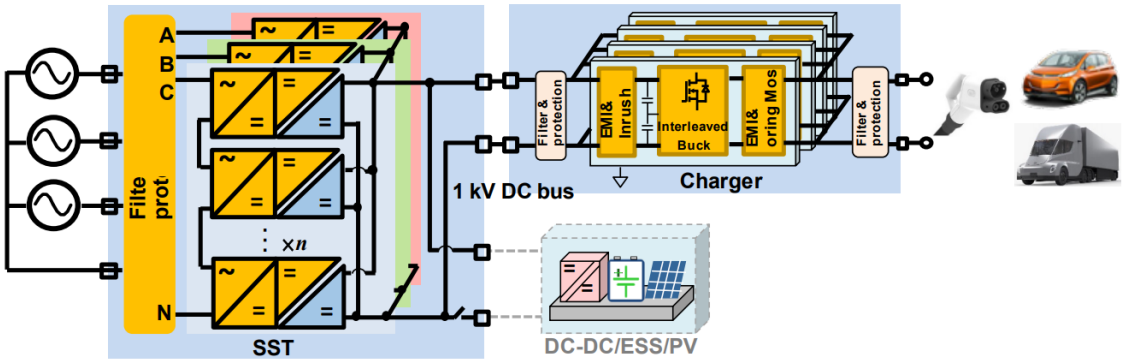


Figure 2.20 400kW MV-connected ultra-fast charging station [34]

The module topology of the SST stage of the proposed charging station is shown in Figure 2.21. As can be seen, the full-bridge NPC converters are used for the AC/DC stage, and an isolated three-level-based SRDAB is used for galvanic isolation. The three-level-based topologies help to reduce the number of components and reduce the stress on the active switches. The main disadvantage of this structure is the number of active switches which introduces challenges regarding manufacturing cost and reliability of the system.

Alongside the proposed MV-connected architecture by Delta electronics, a comparison has been done between the LV-connected and MV-connected charging stations. As shown in Figure 2.22, it is expected that the efficiency of the MV-

connected station increases by 3%, and the footprint of the station reduces by 60% in comparison to LV-connected stations [34].

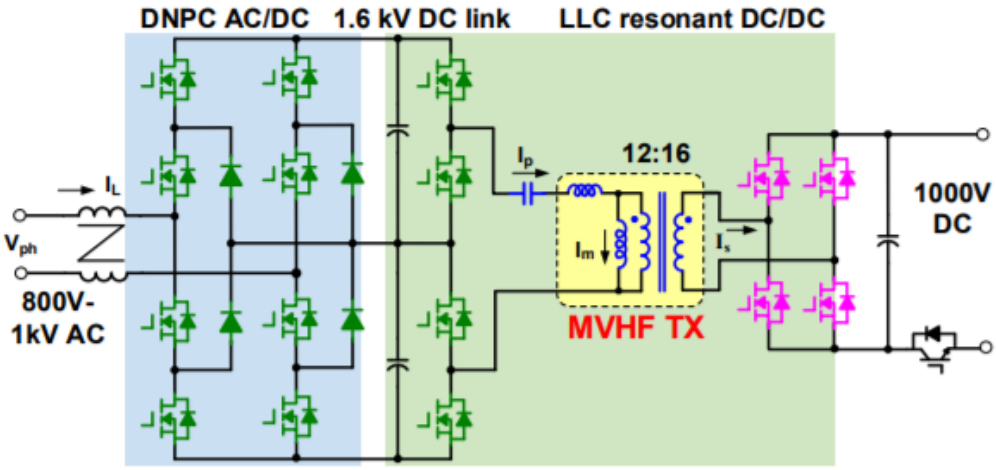


Figure 2.21SST stage of the 400 kW charging station [34]

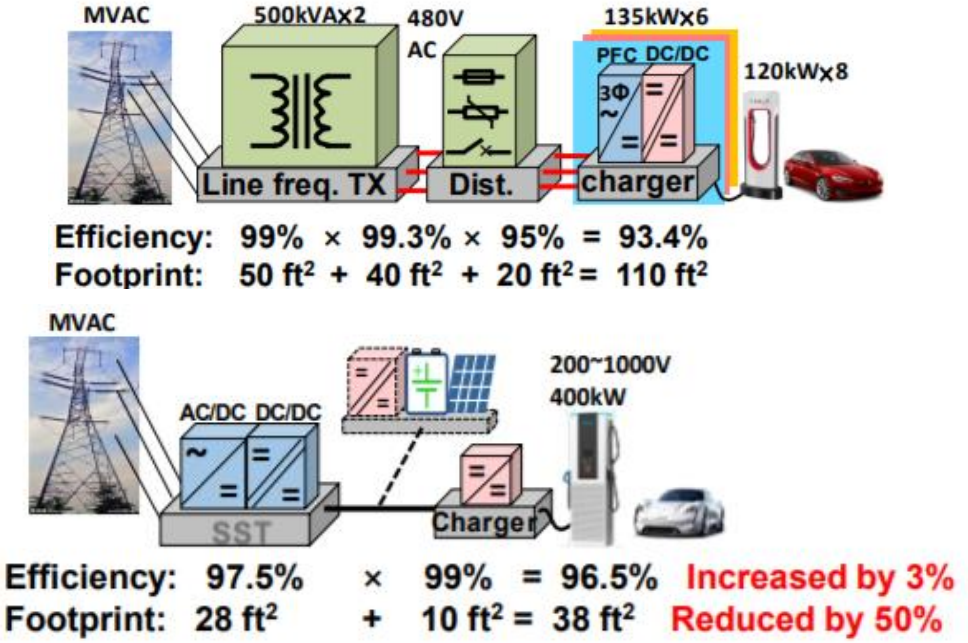


Figure 2.22 MV-connected Vs LV-connected charging station by Delta electronics [34]

As can be seen in the review of different MV-connected charging station architectures, the main focus of different studied architectures is on the AC/DC stage of the charging station and the direct connection to the MV grid. The main challenge regarding the AC/DC stage of the studied architectures is the high number of components and control complexity of the AC/DC converters considered as the rectifying stage of the charging stations, which leads to weakening the cost advantage of these architectures. The main goal of this thesis is to address this challenge by proposing new multilevel topologies with a fewer number of components and control complexity that can reduce the manufacturing cost of the MV-connected stations and simplify their controllers.

2.5 Summary

Human lives are in danger because of the environmental crisis triggered by the consumption of hydrocarbon fuels in different industries such as the automotive industry in recent centuries. It is well-known that EVs are one of the best candidates to overcome the challenges of air pollution in the automotive industry. As discussed in this chapter, some of the main barriers to the worldwide adoption of EVs are range anxiety, charging time, and lack of charging infrastructures. One of the main solutions to overcome these barriers is the ultra-fast charging of EVs. Moreover, it is well-known that cost, efficiency, and in some cases footprint of the

power electronics are the main factors that must be considered in different applications. As investigated in this chapter, the available ultra-fast chargers in the market are LV-connected, where the efficiency is low due to the high current rating of the station, and the cost is high due to the required line-frequency transforms for galvanic isolation. It was shown that the MV-connected ultra-fast charging station can improve these factors significantly.

It is shown in this chapter that the popular candidates for direct connection to the MV grid are multilevel topologies. Therefore, in the next chapter, different MV multilevel converters and their control are investigated.

Chapter 3

Multilevel Converters and their Control Techniques

3.1 Introduction

As discussed in the previous section, the MV-connected ultra-fast chargers are superior to the LV-connected chargers in terms of efficiency, cost, power quality, and footprint. The main stage of the MV-connected chargers is the front-end medium-voltage AC/DC converters. Due to high voltage stress and the limitation of the power semiconductor devices in terms of operating voltage, multilevel topologies have been a popular choice for MV-connected applications such as renewable energy conversion, motor drives, reactive-power compensation, and transportation applications, where not only the voltage stress on the active switches reduces but also higher power quality can be achieved through generating multilevel voltages.

In this chapter, different classic and advanced multilevel topologies and their control techniques are investigated to identify the knowledge gap and challenges regarding these converters. Moreover, different modulation schemes to operate multilevel converters are investigated.

3.2 Multilevel Converters' Applications and their Advantages

Multilevel converters have received significant attention during recent years in high-power medium-voltage applications. These converters have been commercialized and used in different applications in the industry where high-power, medium-voltage converters are required [35]. Among the multilevel converter applications, a few can be mentioned as; compressors, extruders, pipeline pumps in petrochemical industries, pumps in water pumping stations, fans in the cement industry, grinding mills, rolling mills, conveyors, crushers, blast furnace blowers, gas turbine starters, mixers, mine hoists, reactive power compensation, marine propulsion, high-voltage direct-current (HVDC) transmission, hydro pumped storage, wind energy conversion, and railway traction [36]–[43].

The conventional two-level converters face significant limitations for MV high-power applications. Due to the limited operating voltage of power semiconductor devices, active switches must be connected in series to withstand the medium voltage which can lead to low reliability and efficiency. This structure also suffers

from voltage sharing between the switches and requires static and dynamic voltage sharing. Multilevel converters have several advantages in comparison to the conventional two-level three-phase converters, some of these advantages can be mentioned as [40]–[43];

- reduction in total harmonic distortion of the AC output/input waveforms
- lower switching losses
- lower switching stresses (dv/dt)
- increase in the operating voltage of the converter
- reduction in the size of interface transformers and output filters

3.3 Classic Multilevel Topologies

Multilevel topologies can be divided into two main categories, classic and advanced topologies. The classic topologies are the first multilevel converters that were introduced for medium-voltage high-power applications. The flying capacitor (FC) converter, neutral point clamped (NPC) converter, and Cascaded H-bridge (CHB) converter are classified as the classic multilevel topologies [44], [45]. In this section, these topologies are reviewed to identify their strengths and weaknesses.

3.3.1 Cascaded H-Bridge (CHB) Converter

Multilevel topologies first were emerged by the introduction of series-connected H-bridges in late 1960, also known as the CHB converters [45], [48]. The CHB converter is constructed by a series connection of two or more identical H-bridges, where each bridge can produce three voltage levels; V_{dc},-V_{dc}, and 0. The output voltage of these series-connected H-bridges can be combined to form different voltage levels [42]. A CHB converter with N number of H-bridges can generate $2\times N+1$ voltage levels at the output. The single-phase diagram of a nine-level CHB converter and its output voltage are shown in Figure 3.1. As can be seen, four H-bridges are connected in series to form the nine-level CHB converter.

Some of the main advantages of the CHB converter are its scalability and modularity, where the converter is expandable for higher voltage and power ratings by adding more H-bridges to the converter's structure while keeping the same voltage stress on the power semiconductor devices. Moreover, the switching state redundancies of the CHB converter resulted from the H-bridge module redundancy increases the fault-tolerant capability of this converter [42].

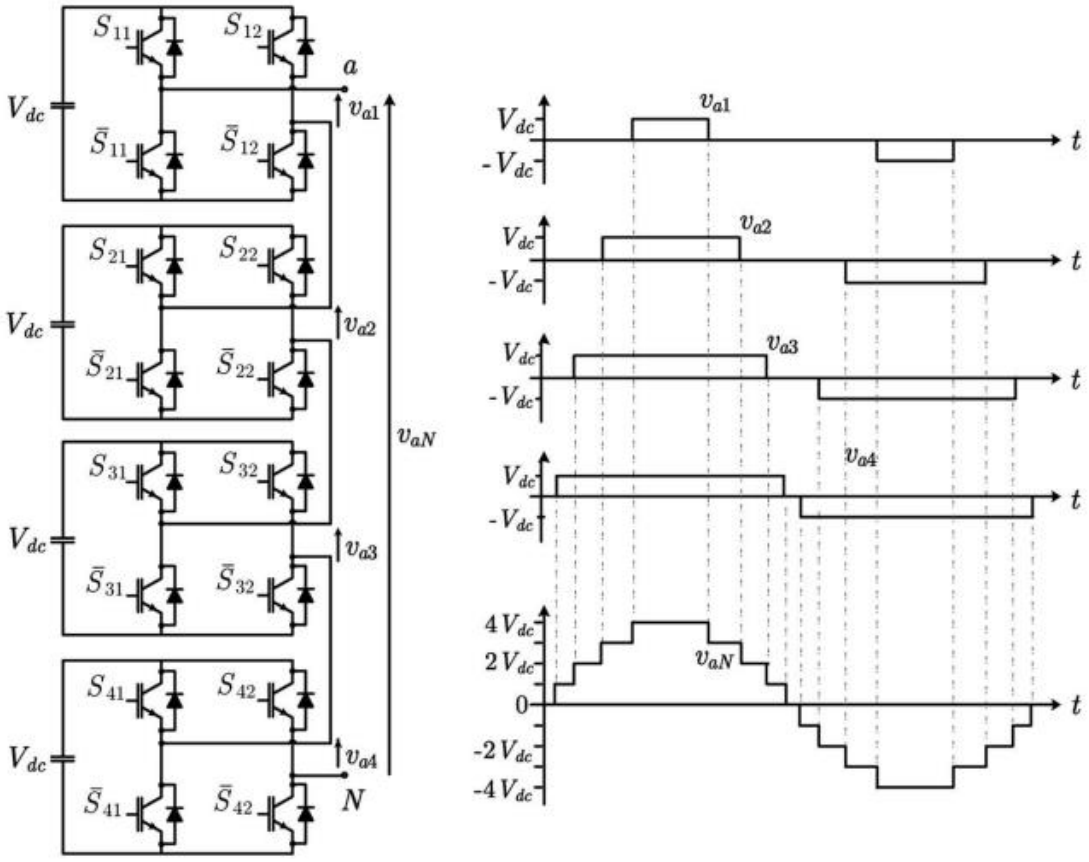


Figure 3.1 A nine-level CHB converter and its output voltage [42]

The main disadvantage of the CHB converter is the requirement for bulky phase-shifting transformers and three-phase rectifiers to provide isolated DC-link voltage for each H-bridge module in DC/AC conversion mode. This will increase the cost and volume of the converter [42]. To add the bidirectional capability to the CHB converter, active power semiconductor switches must be employed for the rectifiers which will add extra cost and volume to the converter. However, the AC/DC conversion mode of the CHB converter does not require the phase-shifting

transformers, therefore, these converters are popular for applications such as MV-connected ultra-fast charging stations.

3.3.2 Neutral Point Clamped (NPC) Converter

The three-level NPC converter also known as Diode-Clamped Converter (DCC) was first proposed in the late 1980s [49]. The three-level NPC converter, as shown in Figure 3.2, is formed by stacking two legs of the conventional two-level voltage source converters on top of each other, where the midpoint of each leg is connected to the mid point of the DC-link through clamping diodes.

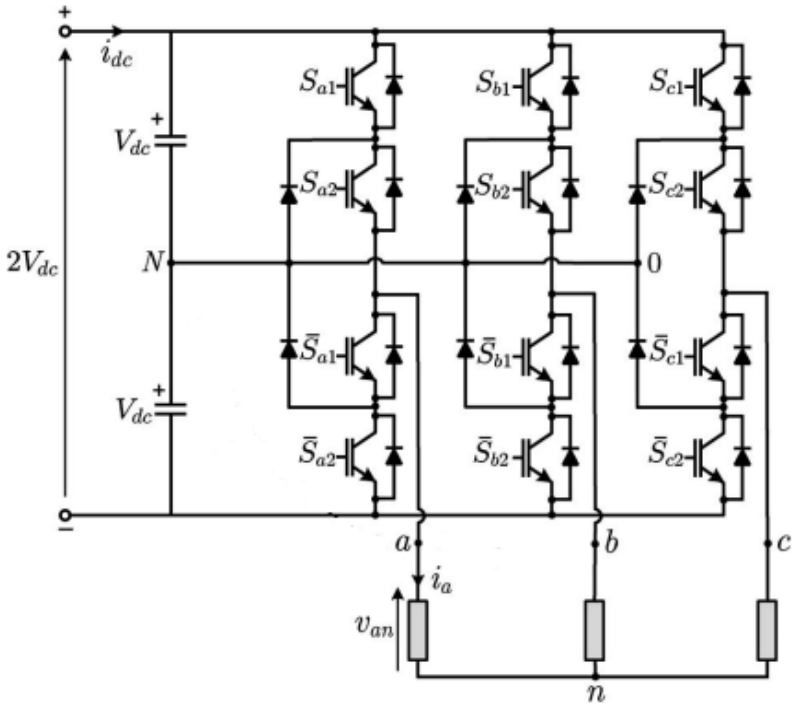


Figure 3.2 Three-level NPC converter [42]

This structure makes it possible to generate a three-level voltage at the output while reducing the voltage stress on the active power semiconductors to half of the DC-link voltage. This can extend the voltage and power rating of two-level voltage source converters that their ratings are limited by the blocking voltage capability of power semiconductor devices [39], [45].

It is possible to increase the number of voltage levels at the output of NPC converters and extend the operating voltage and power rating of these converters by increasing the number of active switches and clamping diodes. This will results in lower voltage stress on the power semiconductor switches [45].

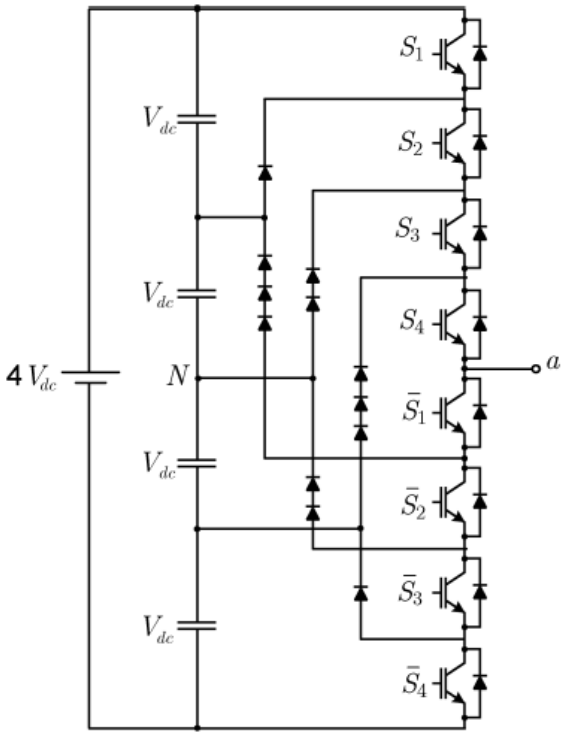


Figure 3.3 Five-level NPC converter [45]

The five-level NPC converter is shown in Figure 3.3, where it has four power semiconductors and six extra diodes in comparison to a three-level NPC converter which add to the cost and volume of the inverter. The increased number of devices and the challenge regarding the control of voltage-clamping nodes have limited the practical application of NPC converters to three-level NPC [45].

3.3.3 Flying Capacitor (FC) Converters

Similar to the CHB converter, a low-power FC converter was first developed in the late 1960s [45]. Unlike the NPC converter, the FC topology does not have any connection to the mid-points of the DC-link, and the clamping diodes of the NPC converter are replaced with the flying capacitors in the FC topology, therefore, different voltage levels are achieved through the flying capacitors [42]. The diagram of a three-level FC converter is shown in Figure 3.4.

The FC topology can be extended for higher power and higher voltages by adding extra active power semiconductor switches and flying capacitors. For instance, a four-level FC topology can be achieved by adding one flying capacitor and two active devices to the three-level topology as can be seen in Figure 3.5.

An interesting feature of the FC topology is its modularity. As can be seen in Figure 3.5, each flying capacitor and active device can be considered as a module, where the series connection of them can add extra voltage levels and extend the

power and voltage rating of this topology. Moreover, the addition of power cells increases the switching states redundancies and can be used for control or optimization purposes [42].

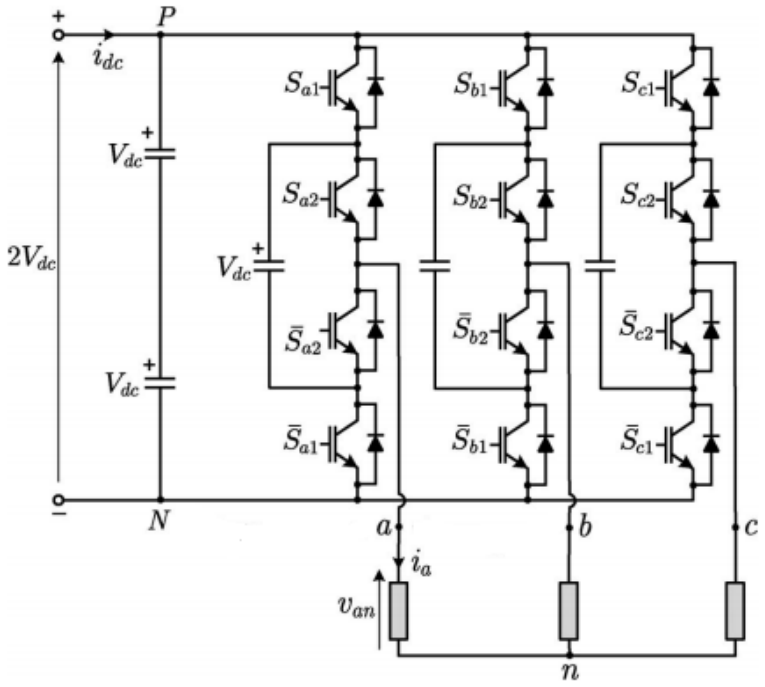


Figure 3.4 Three-level FC converter [42]

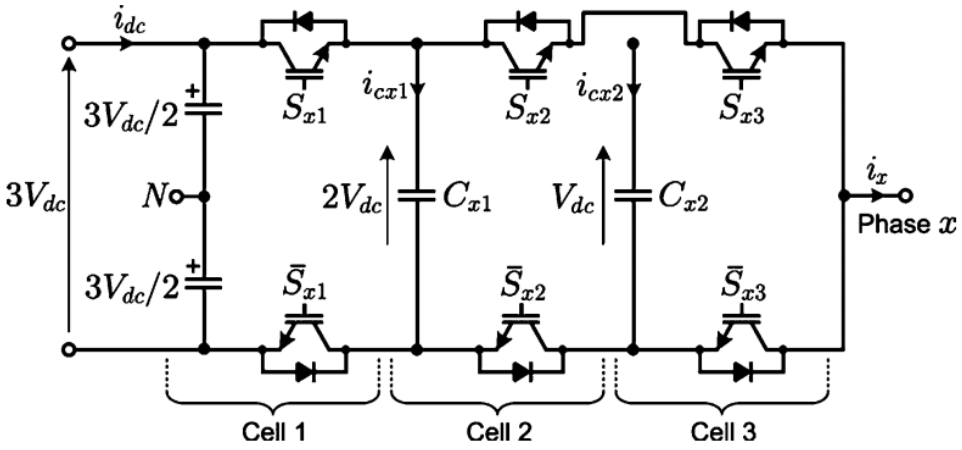


Figure 3.5 Four-level FC topology [42]

For proper operation of the FC topology and equal voltage stress on the active devices, the flying capacitor voltages must be controlled at the desired voltage levels. For instance, in the three-level FC-topology shown in Figure 3.4, the flying capacitor voltages must be controlled at half of the DC-link voltage. This can be considered the main disadvantage of the FC topology, especially in topologies with a higher number of voltage levels. Moreover, the extra cells to extend the power and voltage of the FC topology increase the manufacturing cost, where more active devices, flying capacitors, gate drivers, and heatsink are required.

3.4 Advanced Multilevel Topologies

As discussed in the previous section, the NPC converter, FC converter, and CHB converter are classical multilevel converters. However, these classic topologies have some disadvantages which limit their applications. For the NPC topologies, voltage balancing of the dc-link capacitors is a challenge especially for a higher number of levels. The number of clamping diodes also increases significantly with the higher number of levels. For the FC topology, a higher switching frequency is needed to keep the capacitor voltages balanced. Also, the FC topology with a higher number of levels has a higher number of capacitors which reduces the reliability and lifetime of the converter. The cascaded H-bridge converter has a modular structure, which can get to higher voltages and number of levels with increasing the number of cells.

However, the CHB topology needs several isolated DC sources provided by a bulky, expensive phase-shifting transformer. The number of switches in CHB topology increases significantly in a higher number of output levels.

To overcome the challenges regarding the classic multilevel topologies, advanced multilevel topologies have been proposed. Most of them are combinations of the main classic topologies or modified classic topologies, which try to eliminate or mitigate the disadvantages of the classic topologies. In this section, some of the popular advanced topologies are reviewed to identify their advantage and disadvantages.

3.4.1 Active NPC Topology

The Active NPC (ANPC) topology was proposed to improve the performance of the NPC topology. A three-level A-NPC topology is shown in Figure 3.6, where the clamping diodes in the NPC topology are replaced by active power semiconductor switches [50], [51]. One of the disadvantages of NPC converter is the unequal losses between the inner and outer switching devices. Replacing clamping diodes with active power semiconductor switches in the ANPC topology provides a controllable path for neutral current and thus loss distribution between switches is balanced. However, the number of active switches is increased compared to a conventional

NPC converter which increases the cost of producing the converter and decreases the reliability of the converter.

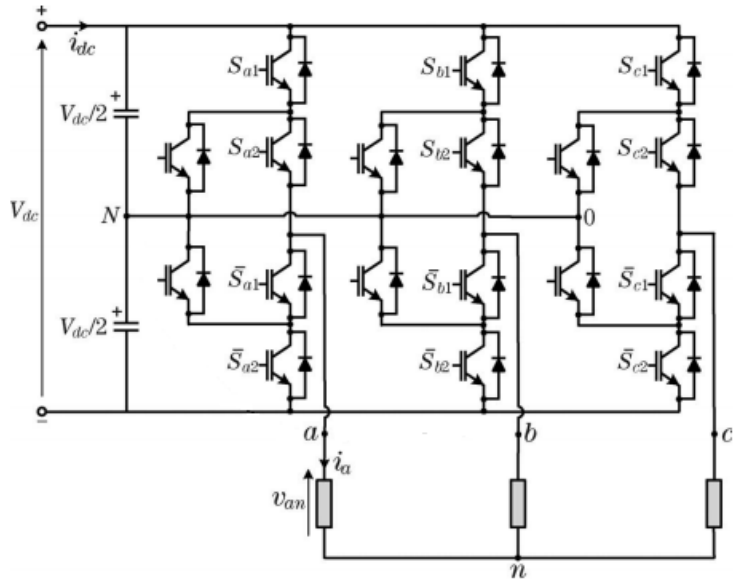


Figure 3.6 Three-level A-NPC topology [39]

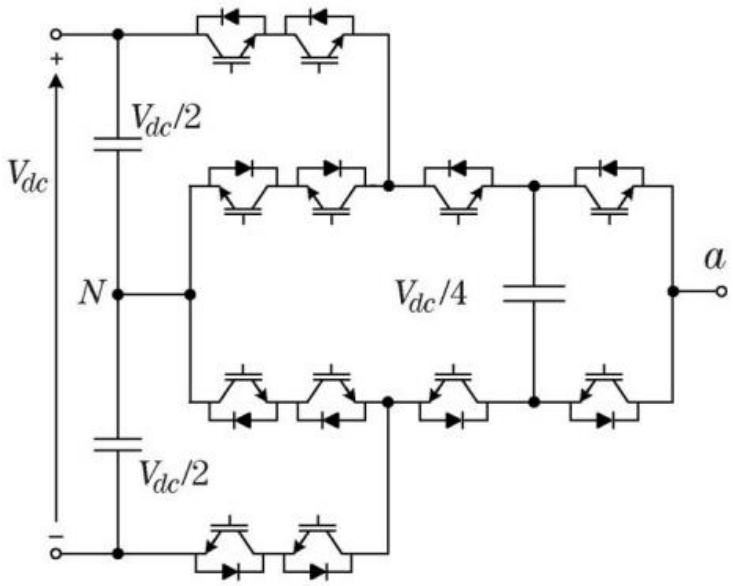


Figure 3.7 Five-level ANPC topology [45]

Another popular NPC-based advanced topology is the five-level ANPC [52]–[56], which is the combination of the three-level ANPC and three-level FC topologies as shown in Figure 3.7. The Five-level active ANPC topology can generate a higher number of levels and improve the output voltage quality, however, the voltage rating of the switches are different, the outer switches are subjected to $V_{dc}/2$, and the inner switches have only $V_{dc}/4$, which leads to a higher number of components that adds to the manufacturing cost of the converter.

A new modified five-level ANPC, as shown in Figure 3.8, is proposed in [57] to solve the different voltage ratings of power switches in the conventional 5L-ANPC. Although the number of switches remains the same as conventional 5L-ANPC, the modified topology requires six more flying capacitors, which causes an increase in cost and control complexity.

Recently, a seven-switch 5L-ANPC (7S-5L-ANPC), as shown in Figure 3.9, is proposed in [58] that requires 21 switches, 6 clamping diodes, and 3 flying capacitors. However, the voltage rating of power switches varies from $V_{dc}/4$ to $3\,V_{dc}/4$. This leads to the need for three power switches in series with the same voltage rating of $V_{dc}/4$, which is not desired for medium voltage applications.

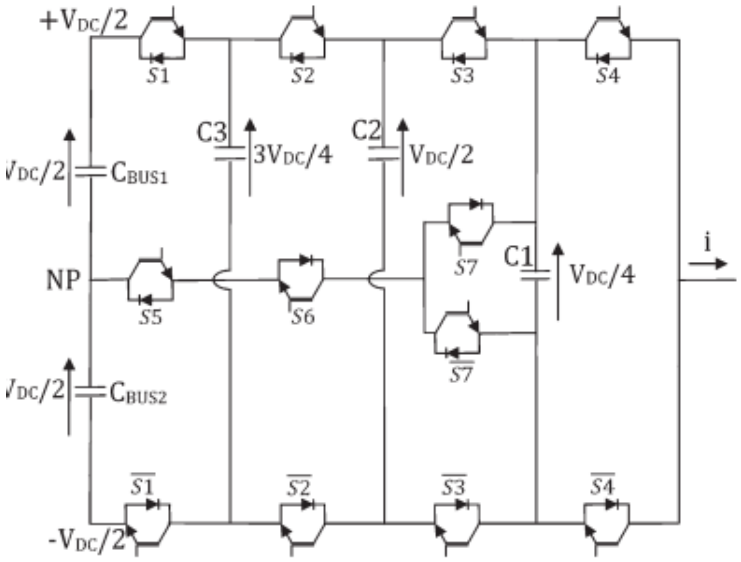


Figure 3.8 Modified 5L-ANPC topology [57]

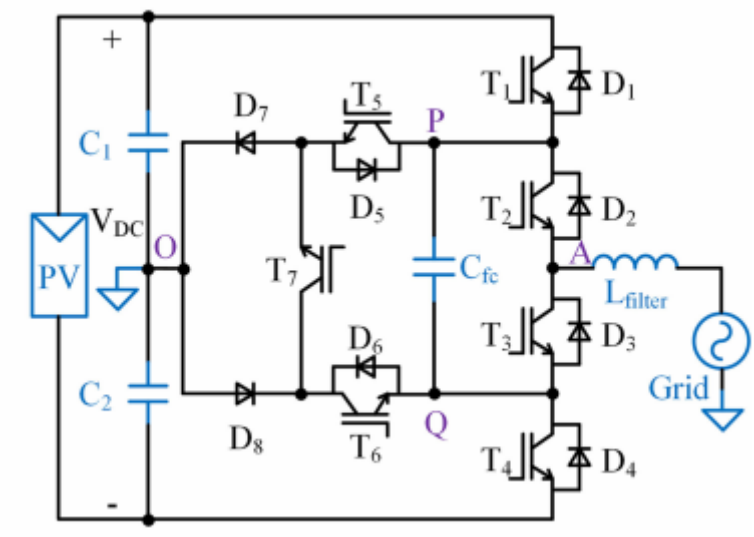


Figure 3.9 Seven Switch 5L-ANPC topology [58]

3.4.2 H-NPC Topology

Combining the NPC and CHB topologies resulted in the H-NPC topology in the late 1990s [59], where each phase of the converter consists of two NPC arms.

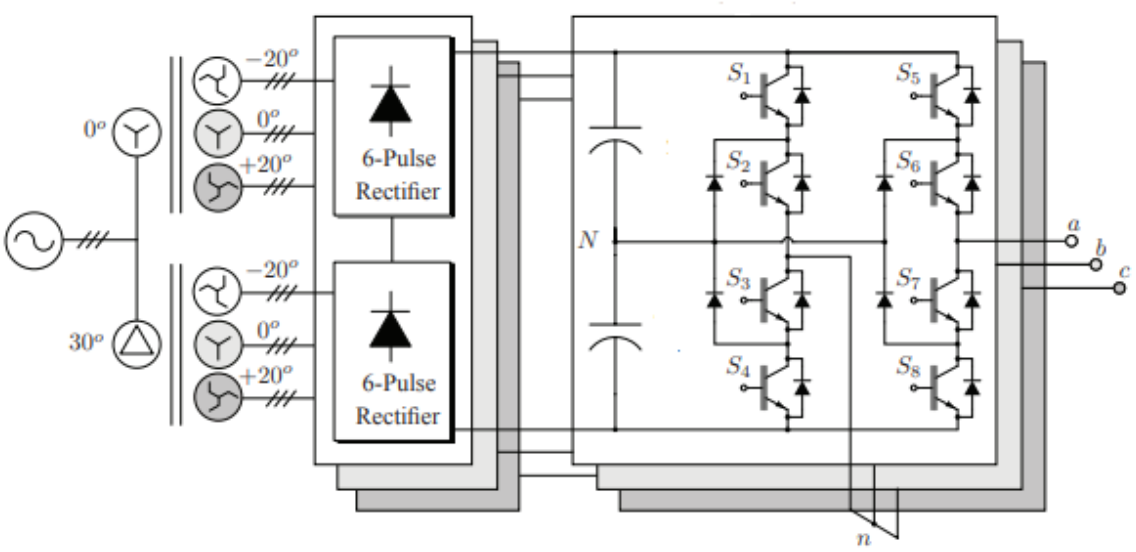


Figure 3.10 Five-level H-NPC topology [60]

The H-bridge connection of two classic 3-level NPC presents a 5-Level HNPC converter as shown in Figure 3.10 that can operate at higher voltage levels than a conventional NPC converter. However, this topology needs several isolated DC sources provided by a bulky and expensive phase-shifting transformer [47], [60]–[62].

3.4.3 T-type NPC Topology

Another NPC-based topology is the three-level T-type NPC converter[63], [64], where the clamping diodes are replaced with a bidirectional switch connecting the mid-point of the DC-link to the mid-point of the H-bridge leg in each phase as shown in Figure 3.11. As shown in Figure 3.11, the bidirectional switch can be built based upon the back to back connection of the active switches.

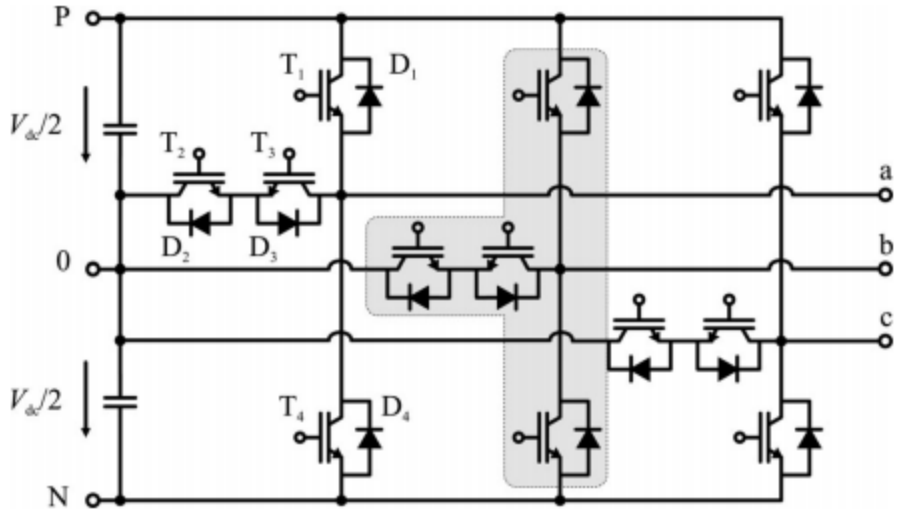


Figure 3.11 Three-level T-type NPC topology [63]

In comparison to the NPC converter, the T-type NPC has a fewer number of devices, however, the blocking voltage of the active power semiconductor switches is equal to the DC-link voltage, which makes it necessary to series active devices in MV applications. In comparison to the two-level inverters, it has lower switching loss and noise, and in comparison to the NPC converter has lower conduction losses. Therefore, it is more efficient than these topologies. Moreover, similar to the NPC, the neutral-point voltage must be controlled to ensure the proper operation of the converter [63].

3.4.4 Nested Neutral-Point Clamped (NNPC) Converter

An interesting recently published advanced topology is the four-level Nested Neutral-Point Clamped (NNPC) converter [65], which is resulted from the combination of the NPC and FC topologies as shown in Figure 3.12. For proper

operation and equal voltage stress on the devices of the five-level topology, its flying capacitors must be controlled at one-third of the DC-link voltage. This topology can operate without the need for series connection of the devices over a wide range of 2.4-7.2 kV, and the blocking voltage of its devices are the same, equal to one-third of the DC-link capacitor. Moreover compared to most of the four-level topologies has fewer components [65].

An interesting feature of this topology is the ability to operate as a five-level converter by controlling the flying capacitors at one-fourth of the DC-link voltage [66]. Therefore, a five-level voltage is generated at the output, which increases the power quality at the cost of unequal voltage stress on the active switches.

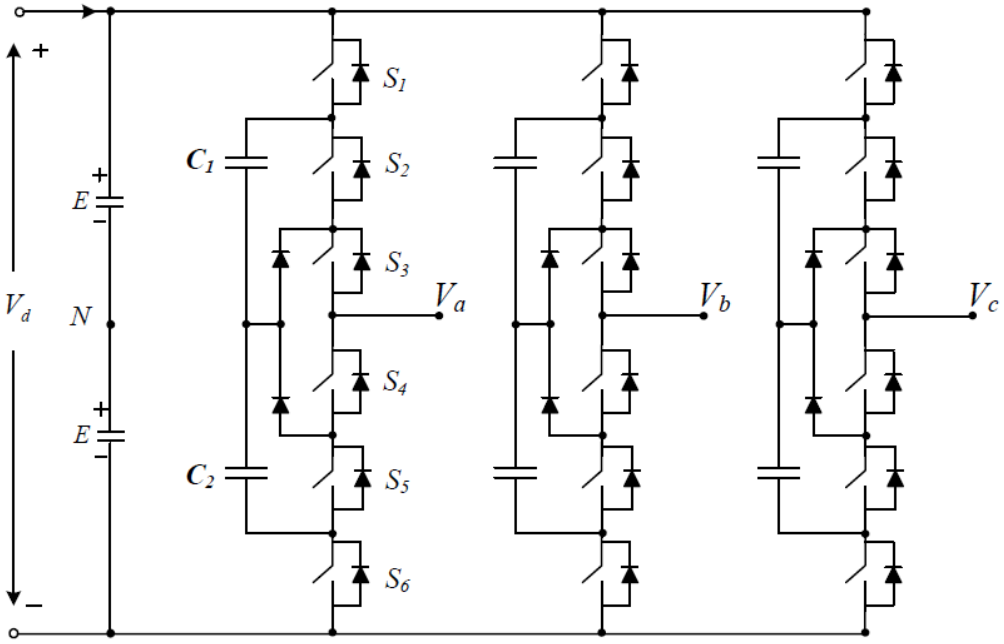


Figure 3.12 Four-level NNPC converter [59]

Similar to the four-level topology, the five-level NNPC has a fewer number of components in comparison to classic five-level topologies.

Another variation of the NNPC converter is the cascaded NNPC or H-NNPC converter [67], shown in Figure 3.13, where each phase consists of two four-level NNPC arms that can generate seven-level voltage at the output of the converter. With this configuration, the operating voltage of the converter can be extended to 10 kV, while improving the power quality at the expense of a higher number of components.

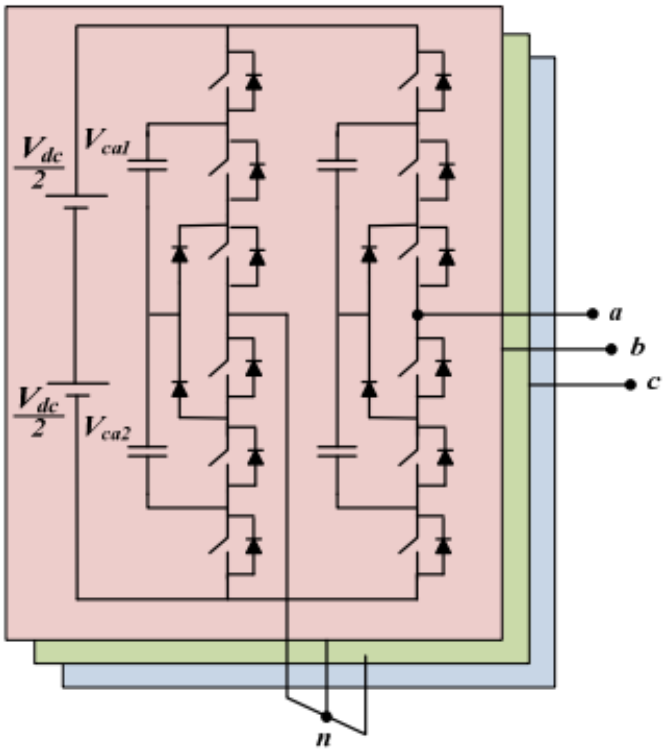


Figure 3.13 Seven-level H-NNPC converter

3.5 Modulation and Control Techniques

With the introduction of multilevel inverters, the conventional modulation methods are adopted and developed for multilevel inverters. On one hand, the increased complexity due to the higher number of switching combinations, and on the other hand, the extra freedom degree to control the converter are the challenges and benefits of developed modulation and control methods for multilevel inverters [42]. The goal of these modulation and control methods is to generate the gating signals for the power semiconductor devices in order to achieve the control objectives such as current, frequency, and voltage control while ensuring minimum power losses and maximum power quality [68].

The main developed modulation and control methods for multilevel converters are Sinusoidal Pulse Width Modulation (SPWM), Space Vector Modulation (SVM), Selective Harmonic Elimination (SHE), and Model Predictive Control (MPC) which are investigated in this section to identify their advantages and drawbacks.

3.5.1 Sinusoidal Pulse Width Modulation (SPWM) algorithms

The most popular developed modulation methods for multilevel converters are based on SPWM, where the reference voltage is compared with high-frequency carriers to generate the gating for power semiconductor devices. The reference

voltage of an N-level multilevel converter is compared to N-1 carriers (typically triangle waveform) to obtain the desired voltage and power quality, however, depending on the type of SPWM based algorithm, multiple reference voltage can be used as well. The SPWM algorithm can be divided into two main categories; Phase Shifted PWM (PS-SPWM) and Level Shifted SPWM (LS-SPWM) [68].

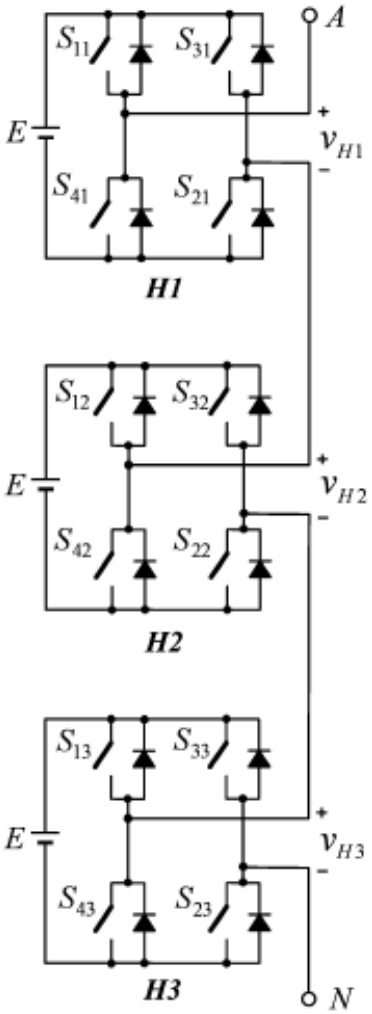


Figure 3.14 Seven-level CHB converter [44]

A. Level-Shifted SPWM (LS-SPWM)

In this method, the carrier waveforms are vertically distributed over the range of the DC-link voltage, for instance, an N-level converter with V_{dc} as the DC-link voltage, N-1 levels are equally distributed over the range of $V_{dc}/2$ to $-V_{dc}/2$. The gating of the power semiconductor devices are determined by comparison of the reference voltage and the carriers. To demonstrate the principles of LS-PWM, the reference voltage, carriers, and gating signals for the seven-level CHB converter shown in Figure 3.14 are shown in Figure 3.15.

As can be seen in Figure 3.15, one reference waveform (v_{ma}) and six carriers (v_{cr}) are used to generate the gating signals for the seven-level CHB converter. To generate the gating signals for S_{11} and S_{31}, the reference voltage is compared to v_{cr1} and $v_{cr1\text{-}}$ respectively, where the reference waveform is higher than the carrier the switch is turned on and vice versa. Similarly, the gating signals for other switches are determined to generate the seven-level phase voltage (V_{AN}). The main disadvantage of this approach is the unequal conduction intervals which lead to unequal loss distribution among the power semiconductor devices.

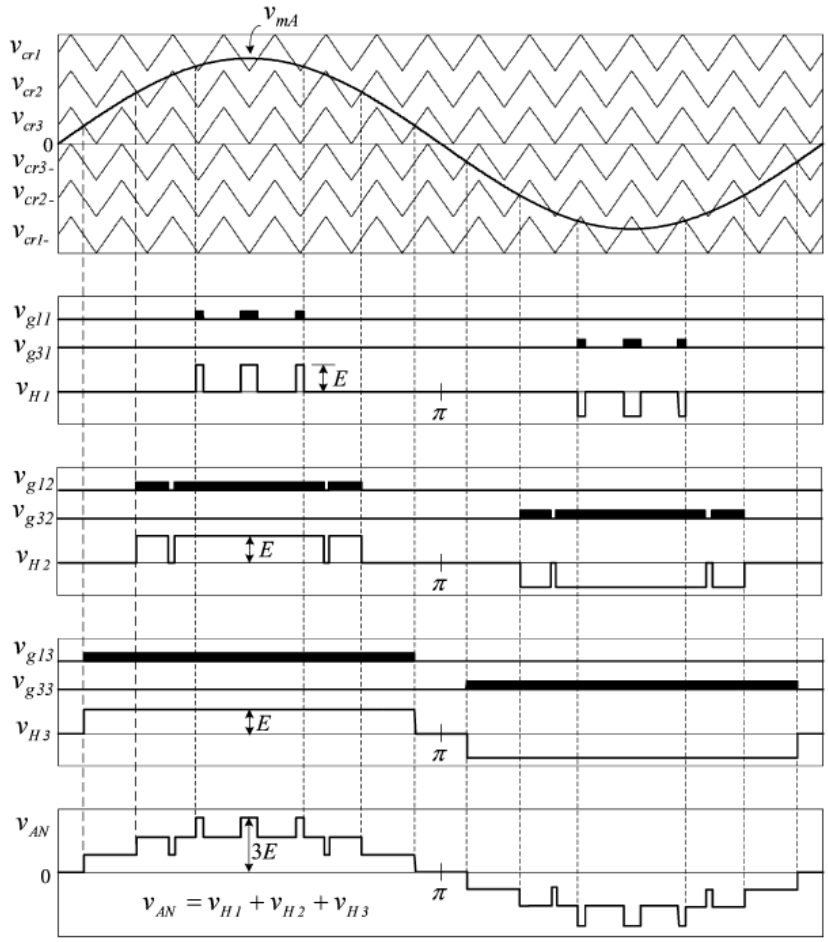


Figure 3.15 LS-SPWM for seven-level CHB converter [44]

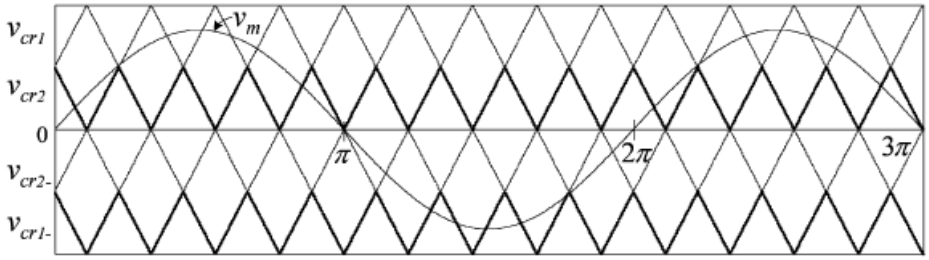


Figure 3.16 APOD LS-SPWM [44]

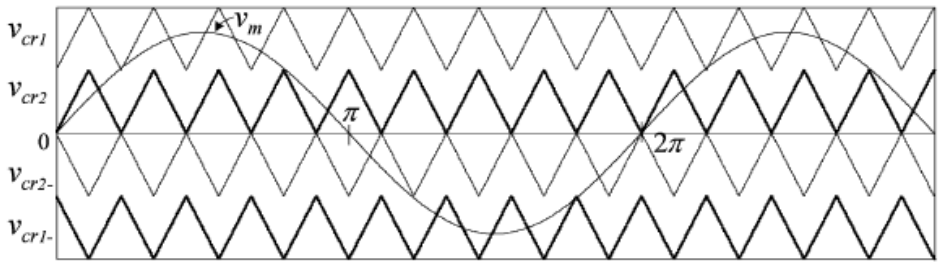


Figure 3.17 POD LS-SPWM [44]

The method shown in Figure 3.15 is called In Phase Disposition (IPD) LS-SPWM, where the carrier waveforms are in phase with each other. The other variations of LS-PWM are shown in Figure 3.16 and Figure 3.17 called Alternative Phase Opposite Disposition (APOD) and Phase Opposite Disposition (POD) respectively. However, the most used approach is IPD since it results in a better harmonic profile and power quality [44].

B. Phase-Shifted SPWM (PS-SPWM)

Although LS-SPWM can be applied to modular topologies, the PS-SPWM method is popular to control the modular multilevel topologies such as CHB, and FC topologies. It has been observed that if a phase shift equal to $360/m$, where m is the number of cells in a modular topology is applied to the carriers, the lowest harmonic distortion can be achieved. The applied phase shift generates a phase-shifted voltage for each cell, where the sum of them generates a stepped voltage waveform [42].

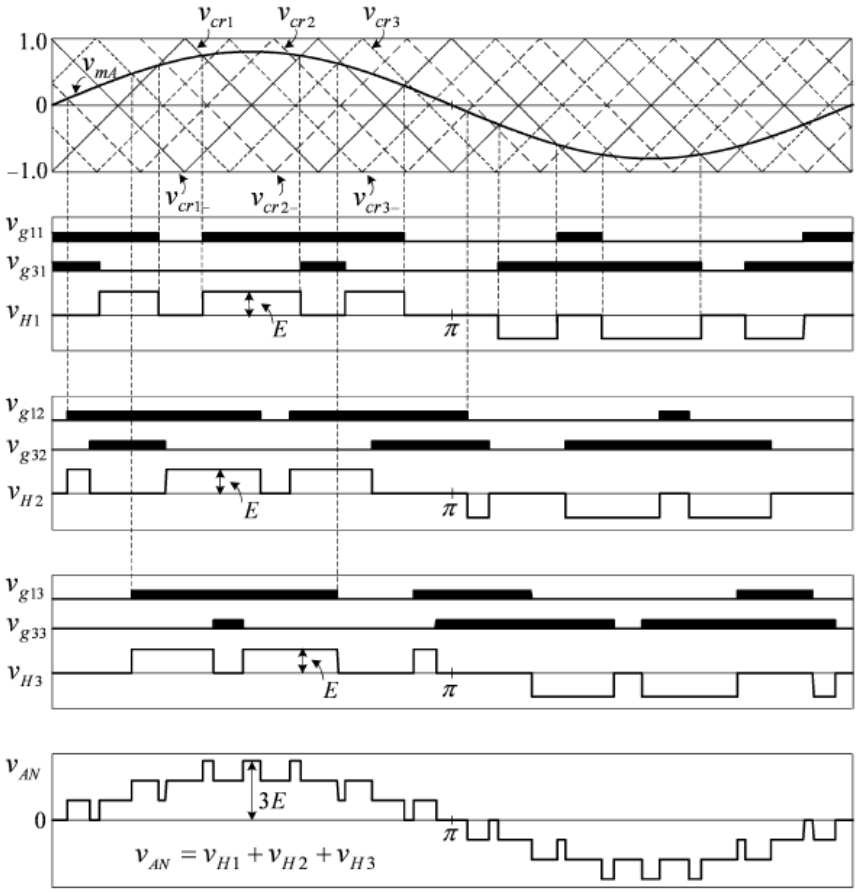


Figure 3.18 PS-SPWM applied to a seven-level topology [44]

The PS-SPWM applied to the seven-level topology shown in Figure 3.14, is shown in Figure 3.18. As can be seen, a 60-degree phase shift is applied between the six carriers to generate the stepped phase voltage (V_{AN}).

To compare LS-SPWM and PS-SPWM, it can be mentioned that less line voltage distortion can be achieved through LS-SPWM since the carriers are in phase. Moreover, LS-SPWM can be applied to any multilevel topology since it is based on the output voltage levels of the topology. However, PS-SPWM is preferred

for modular topologies since LS-SPWM causes uneven loss distribution among different cells [42]. Another disadvantage of LS-SPWM is the different device switching frequencies.

3.5.2 Space Vector Modulation (SVM) Technique

In this approach, the three-phase reference voltage and output voltages resulted from possible switching states of the multilevel topologies are transferred to α-ß stationary frame through Clarke transformation and the dwell time of each device is calculated using three adjacent vectors that can be summed up to be equal to the reference voltage as shown in Figure 3.19 for a three-level converter [69]–[72].

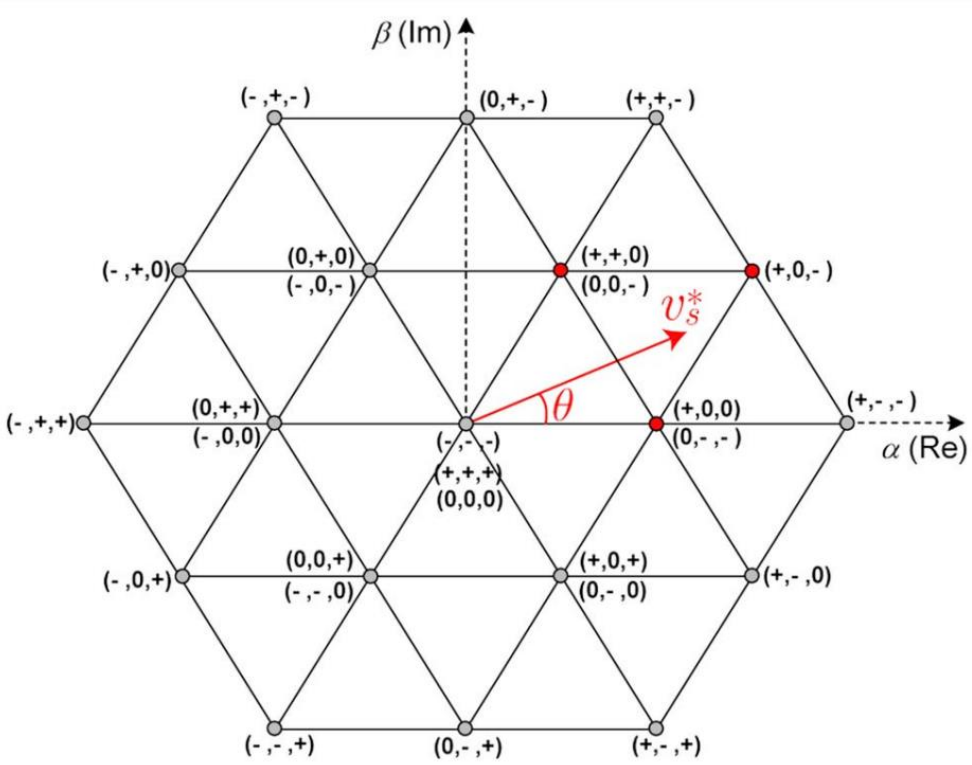


Figure 3.19 Space Vectors of a three-level converter [42]

The most important advantage of SVM to control multilevel inverters is the extra degree of freedom due to line redundant switching states that generate the same output voltage. These redundant switching states can be used to control the voltages of the flying capacitors, DC voltage balance, common-mode voltage, and switching losses [68].

3.5.3 Selective Harmonic Elimination (SHE) Technique

Due to power losses of power semiconductor devices, high-power multilevel converters typically have low switching frequency, which leads to significant low order harmonic distortions. This is the main motivation behind developing SHE methods for multilevel converters, where predefined switching angles are calculated based on Fourier analysis to target the elimination of low-order harmonics [42].

To obtain the desired switching angles, first, the Fourier series of the output voltage based on the converters operating condition is calculated, then the coefficients of the undesired harmonics are solved to be equal to zero, while the fundamental component is made equal to the amplitude of the desired reference voltage.

The voltage waveforms of a seven-level CHB controlled by SHE is shown in Figure 3.20, where three predefined switching angles are used for each cell per phase

to generate the seven-level voltage at the output while eliminating the undesired harmonics [73]–[76].

The main advantages of SHE are low switching losses due to low switching frequency and the elimination of the undesired harmonic distortions, which leads to a reduction of filter weight, cost, and volume. On the other hand, solving equations for multiple operating points is impossible in real-time, therefore, look-up tables are used to store the desired calculated switching angles. These data then are used to obtain the desired switching angles by interpolation for different operating points. This is a disadvantage for applications that require high dynamic performance [42].

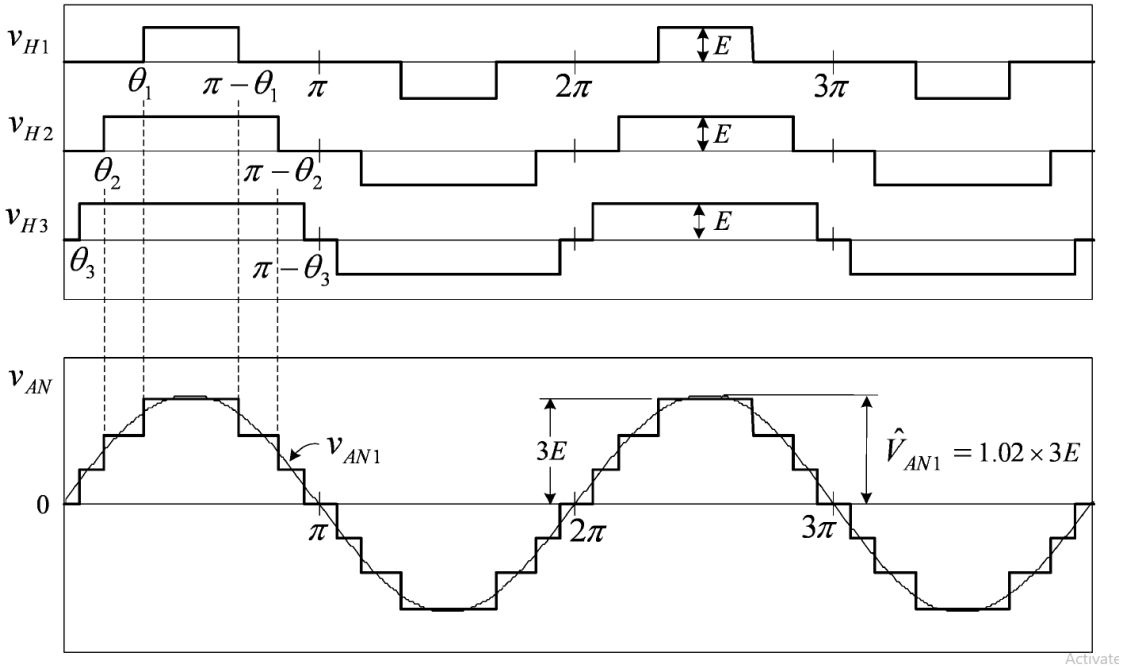


Figure 3.20 SHE applied to a seven-level converter

3.5.4 Model Predictive Control (MPC)

Due to the development of fast microprocessors, MPC has gained considerable attention in power electronics recently. Easy digital implementation, nonlinearity inclusion, fast dynamic response, simultaneous satisfaction of multi-control objectives without PID controllers, and PWM blocks, are the advantages of MPC which caused its' emergence into power electronics. The concept of MPC in power electronics is based on the mathematical model of the converter in terms of switching states, and predicting the systems variables' behavior in the future states. A cost function is used to force the control objectives to track the predefined references, by selecting an appropriate switching state that minimizes the cost function. For the digital implementation of the control method, the discrete mathematical model of the converter is required [77]–[81]. These modulation and control methods are discussed and implemented in detail in the next chapters.

3.6 Summary

As discussed in the previous chapter, multilevel converters are the essential building blocks of the MV-connected ultra-fast charging station, where they serve as the AC/DC and PFC in the charging system. In this chapter, different multilevel converters, such as classic and advanced topologies and their modulation and control methods were reviewed. As discussed, multilevel converters were first

introduced with the classic topologies, which these topologies have drawbacks that limit their applications. Then, the advanced topologies were introduced to overcome the challenges regarding the classic topologies. It is observed that the efforts are in the path to reduce the number of components and control the complexity of multilevel topologies in the literature, to make it possible to reduce cost, weight, and increase the efficiency of these converters. Moreover, it was found that due to extra redundancies in the multilevel topologies, the complexity of the modulation methods and controllers is increased. These points justify the efforts required to propose new multilevel topologies and controllers with a fewer number of devices and simplified controllers to address the drawbacks of multilevel topologies so that they can be employed in practical applications such as MV-connected ultra-fast charging stations.

Chapter 4

The Proposed Five-Level T-Type NNPC Topology and its Controller

4.1 Introduction

As discussed in previous chapters, medium-voltage converters have gained considerable attention in various applications such as medium-voltage connected ultra-fast EV chargers. In this chapter, first, the operation of a four-level T-type NNPC is reviewed. The 4-level T-type NNPC topology has a fewer number of devices compared to the existing 4-level topologies. A controller based on the SPWM technique is proposed and developed to control flying capacitors voltages. In this chapter, an advanced 5-level topology is also proposed based on the aforementioned 4-level topology. The proposed topology has a fewer number of active switches and flying capacitors in comparison to the existing 5-level topologies.

Moreover, an MPC based controller is also developed for the proposed 5-level topology to control the flying capacitor voltages and output current simultaneously without the need for PI controllers.

These topologies are the building block for medium-voltage applications and can be used either as DC-AC converters for different applications including, but not limited to, wind/solar energy integration, power transmission, and industrial motor drivers or as AC-DC converters for medium-voltage ultra-fast chargers applications. Therefore, in this chapter, the operation of the proposed topologies is investigated for both applications in simulation studies, while experimental results are given for industrial motor drive application since the performance of the topologies can be examined over a wider range of operating conditions.

4.2 A 4-Level T-type NNPC Topology

Recently, a 4-level T-type NNPC is proposed in [82], [83] and shown in Figure 4.1, which offers various advantages compared to the conventional and existing advanced four-level topologies. For proper operation and limiting voltage stress on the active switches, the flying capacitor of the 4-level T-type NNPC must be controlled at one-third of the DC-link voltage ($V_{dc}/3$). However, the 4-level T-type NNPC was proposed in [82] considering constant DC-sources instead of flying capacitors, which is not practical.

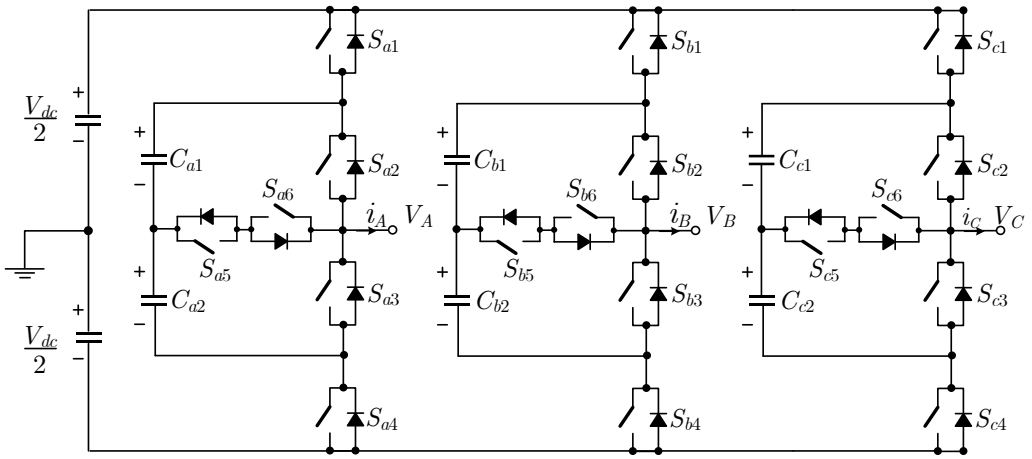


Figure 4.1 T-type four-level nested neutral point clamped (T-NNPC) Inverter [82]

Therefore, a controller is required to balance the flying capacitors at the desired level of $V_{dc}/3$. In this chapter, the advantages and challenges of the 4-level T-type NNPC are investigated, then a controller based on SPWM is proposed to balance the flying capacitor voltages at $V_{dc}/3$. Simulation and experimental results are provided to demonstrate the feasibility of the proposed controller.

4.2.1 Advantage and challenges

The Nested T-Type four-level NNPC is very attractive for high-power and medium-voltage applications due to the fewer number of devices as compared with other 4-level topologies shown in Table 4.1. As can be seen from Table 4.1, T-type NNPC has a lower number of components compared to the existing 4-level topologies such as NPC, FC, and NNPC topologies and thus the size, weight, cost, and reliability of the converter can be improved compared to the existing four-level topologies.

TABLE 4.1 NUMBER OF DEVICES IN 4-LEVEL TOPOLOGIES

Topology	No. of switches	No. of diodes	No. of capacitors
NPC	18	18	-
FC	18	-	9
NNPC	18	6	6
T-Type NNPC	18	-	6

As can be seen in Table 4.1, the diodes are eliminated compared to NPC and NNPC, and the number of flying capacitors has been reduced compared to the FC topology. On the other hand, as discussed previously the challenge regarding this topology is to control the flying capacitor voltages at the desired level to output 4-level voltage and balance the voltage stress on the active switches. To develop a controller for the 4-level T-type, it is required to investigate the operation of the topology in detail.

4.2.2 Converter's Operation

A four-level T-type NNPC topology is a combination of a flying capacitor topology and a T-type inverter. The capacitors C_{x1} and C_{x2}, $x = a,b,c$ are charged to one-third of the total DC-link voltage ($V_{dc}/3$). Six switching states can generate four output voltage levels as can be seen in Table 4.2. A controllable current path is provided by the bidirectional switches to control the direction of the output current.

TABLE 4.2 SWITCHING STATES OF THE T-TYPE FOUR-LEVEL INVERTER AND CONTRIBUTION OF THE AC-SIDE CURRENTS TO THE FLYING CAPACITOR VOLTAGES

S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	V_{Cx1}	V_{Cx2}	V_{xn}	Level	State
1	1	0	0	1	0	No Impact	No Impact	$\frac{V_{dc}}{2}$	3	3
1	0	0	0	1	1	Charging (ix>0) Discharging (ix < 0)	No Impact	$\frac{V_{dc}}{6}$	2	2B
0	1	0	1	1	0	Discharging (ix > 0) Charging (ix < 0)	Discharging (ix > 0) Charging (ix< 0)			2A
1	0	1	0	0	1	Charging (ix >0) Discharging (ix < 0)	Charging (ix > 0) Discharging (ix < 0)	$-\frac{V_{dc}}{6}$	1	1B
0	0	0	1	1	1	No Impact	Discharging (ix > 0) Charging (ix< 0)			1A
0	0	1	1	0	1	No Impact	No Impact	$-\frac{V_{dc}}{2}$	0	0

As shown in Table 4.2, level 2 and level 3 have two redundant switching states which generate medium voltage level $1/6\,V_{dc}$ and -$1/6\,V_{dc}$ with respect to the mid-point of the DC source. Each of these redundant switching states has a specific charging and discharging effect for each flying capacitor. The method for controlling the capacitors' voltages is based on choosing the best redundant switching state which makes the capacitor charge or discharge to the desired voltage which is one-third of the total DC-link voltage.

It is worth mentioning that the operation of the converter for both industrial motor drives, and ultra-fast charging station is identical, and only the power flow direction is different.

4.3 An SVM Based Modulation Technique to Control Flying Capacitor Voltages of the Four-Level T-NNPC

A space vector modulation (SVM) technique has been developed in this section in order to control the voltage of flying capacitors of the four-level T-NNPC.

The space vector diagram of a four-level is a hexagon. The hexagon is divided into six sectors, Sector I to Sector VI, and each sector is divided into nine triangles. Sector one is shown in Figure 4.2.

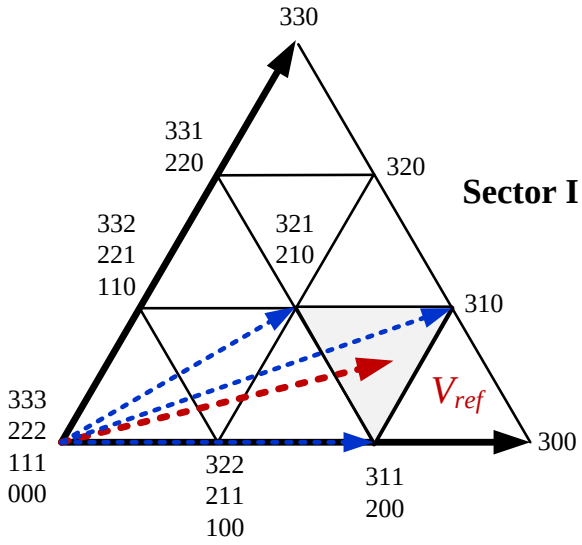


Figure 4.2 Space vector diagram of the four-level T-NNPC

The triangle vertices indicate the switching state of each converter phase i.e. *a, b,* and *c* respectively. The reference vector can be synthesized by the three adjacent switching vectors [84] described as;

$$\begin{gathered}\vec{V}_1 t_1 + \vec{V}_2 t_2 + \vec{V}_3 t_3 = \vec{V}_{ref} T_s \\ t_1 + t_2 + t_3 = T_s \\ \vec{V}_{ref} = \left|\vec{V}_{ref}\right| e^{j\theta}, \qquad \theta = \omega * t\end{gathered} \tag{4.1}$$

where T_s is the switching period, $\vec{V}_1, \vec{V}_2$ and $\vec{V}_3$ are the three switching vectors adjacent to V_{ref} and t_1, t_2 and t_3 are the calculated dwell-time of the corresponding switching vectors [84]. ω is the rotational speed of the reference vector.

A cost function, J, is defined based on the energy deviation of the flying capacitors to minimize the voltage deviation of the capacitors from their desired values. Therefore, the cost function can be expressed as:

$$\begin{gathered}J = J_a + J_b + J_c \\ J = \sum_{x} \sum_{i=1}^{2} \frac{1}{2} C_{cxi} (V_{C_{cxi}} - {V_{Dc}}/{3})^2 \\ x=a,b,c.\end{gathered} \tag{4.2}$$

To balance the capacitor voltage at the desired value ($V_{dc}/3$), the switching states among available redundant switching states that minimize the cost function should be selected in each sampling time. The following condition is required to be satisfied in order to minimize the cost function;

$$\begin{gathered}\frac{dJ_x}{dt} = \sum_{i=1}^{2} C_{cxi} \left(V_{C_{cxi}} - {V_{Dc}}/{3}\right) \frac{dV_{C_{cxi}}}{dt} \leq 0 \\ x = a, b, c\end{gathered} \tag{4.3}$$

where;

$$i_{C_{cxi}} = C_{cxi}\frac{dV_{C_{cxi}}}{dt} \tag{4.4}$$

and $i_{C_{cxi}}$, is the current of the capacitor C_{cxi}, x=a,b,c , i=1,2. Equation 4.3 can be rewritten as;

$$\sum_{i=1}^{2}\left(V_{C_{cxi}} - {}^{V_{Dc}}/_{3}\right) i_{C_{cxi}} \leq 0 \tag{4.5}$$

The best switching states should be select to minimize Equation (4.5) over one sampling period and thus;

$$\sum_{i=1}^{2}\left(V_{C_{cxi}} - {}^{V_{Dc}}/_{3}\right) \bar{\imath}_{C_{cxi}} \leq 0 \tag{4.6}$$

where, $\bar{\imath}_{C_{cxi}}$ is the average value of capacitor (C_{cxi}) current. This current can be calculated based on the switching states and their relationship to AC-side currents i_a, i_b, and i_c. The average current for each capacitor is calculated based on the output line current, and the charging or discharging effect of each switching state. 0, 1, -1 is assigned to each switching state base on the effect of charge (1), discharge (-1), no impact (0) on the capacitor's voltages, so $\bar{\boldsymbol{\imath}}_{\boldsymbol{C_{cxi}}}$ is calculated as;

$$\tilde{i}_{Cxi} = \frac{t_1 \times \operatorname{sgn} xi(S_1) + t_2 \times \operatorname{sgn} xi(S_2) + t_3 \times \operatorname{sgn} xi(S_3)}{T_s} \times I_x \tag{4.7}$$

where; *sgnxi* (S) is a function that outputs {1,0-1} based on the effect of each switching state on each capacitor voltage. S_1, S_2, S_3 are the switching states corresponding to the three switching vectors adjacent. I_x is the output line current for phases a, b, and c.

In order to select the best switching state that can minimize the cost function, first, the average current of each capacitor is calculated for all the possible switching states, and thus the switching state that minimizes the cost function J will be selected and then applied to the converter for the next sampling time.

4.3.1 Simulation Studies

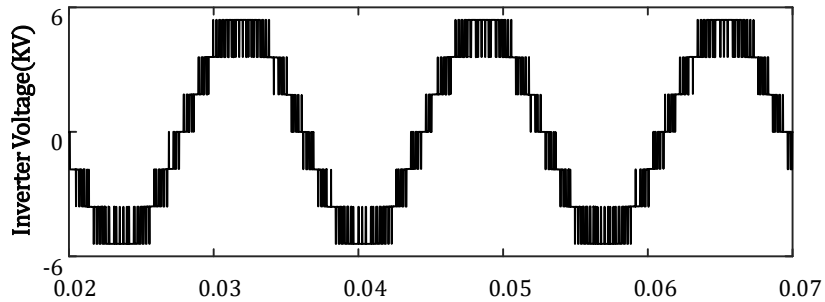
To show the performance of the proposed control technique for the nested T-type inverter, simulation studies have been done in MATLAB/Simulink environment for a 1 MVA/3.3 kV inverter. The parameters of the system under the study are shown in Table 4.3.

TABLE 4.4 PARAMETERS OF THE STUDY SYSTEM

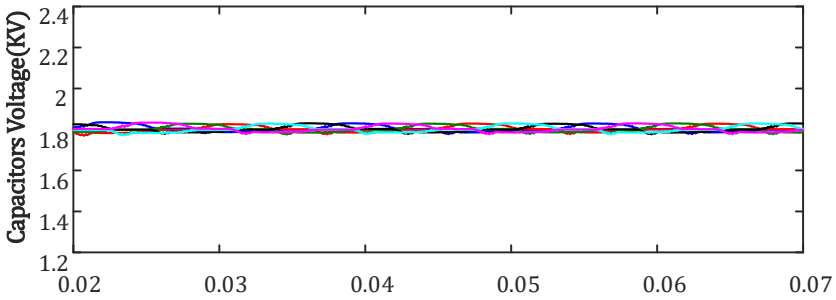
Converter Parameters	Values
Converter Rating	1 MVA
Output Voltage	3.3 kV
Flying Capacitors	3300 µF
Input DC Voltage	5.4 kV
Output Frequency	60 Hz
Output Inductance	5.5 mH
Output Load	10.5 Ω

The simulation also demonstrates the effectiveness of the developed SVM to generate output voltages and to regulate and balance the voltage of flying capacitors. The performance of the developed control technique has been studied during both steady-state and transient conditions.

Figure 4.3 and Figure 4.4 show the performance of the developed control techniques based on the SVM strategy for different operating conditions. Figure 4.3 shows the inverter output voltage and flying capacitor voltages where modulation index $m = 0.95$ and load PF is 0.9. Figure 4.4 shows the output voltage and flying capacitors when the modulation index changes from 0.5 to 0.95.

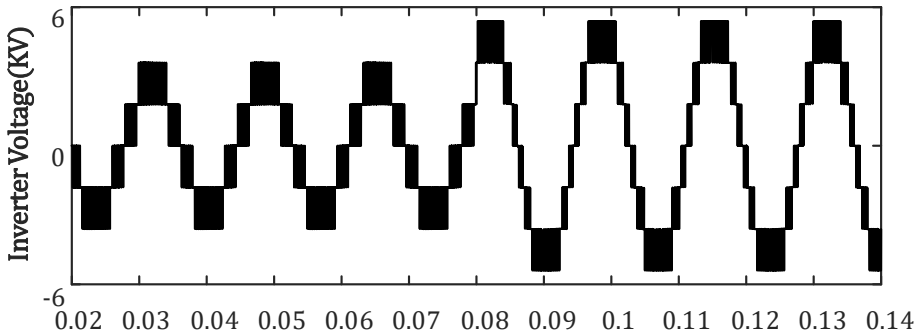


(a) Inverter voltage

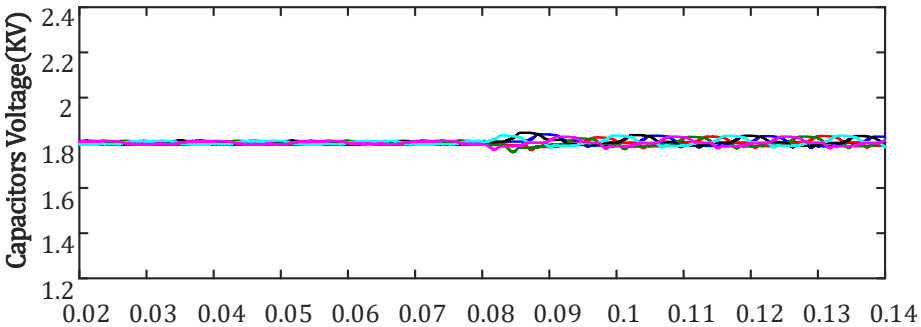


(b) Flying capacitor voltages

Figure 4.3 Steady-state simulation with m=0.95, PF=0.9



(a) Inverter voltage



(b) Flying capacitor voltages

Figure 4.4 Step change from m=0.5 to m=0.95

As can be seen from the simulation studies, capacitor voltages are well balanced at different load power factors and different modulation indices. It is worth mentioning that all the power switches have the same voltage rating that is equal to one-third of DC input voltage which is 1800V.

4.3.2 Experimental Results

The feasibility of the converter with the developed controller is evaluated experimentally. The parameters of Table 4.5 were used for experiments on a scaled-down prototype.

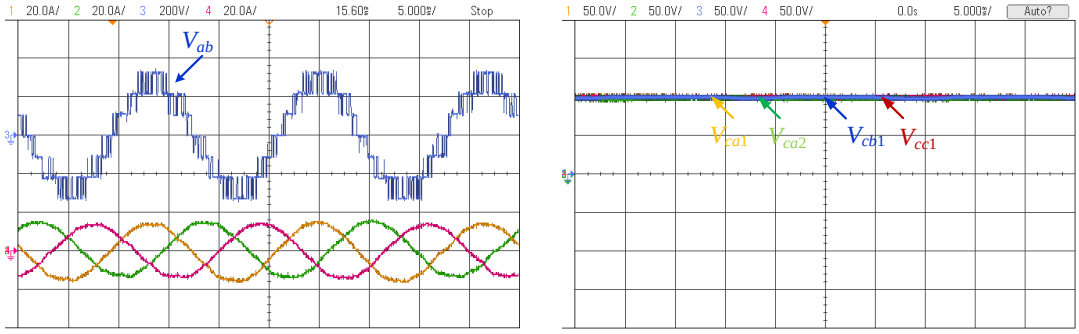
TABLE 4.5 PARAMETERS OF THE STUDY SYSTEM

Converter Parameters	**Values**
Converter rating (kVA)	5
Capacitor Value (μF)	2200
Input dc voltage (V)	320
Output frequency (Hz)	60
Output inductance (mH)	5
Output load (**Ω**)	12

The switching frequency of the converter was set to 2 kHz, and the developed control method is implemented in the dSPACE Microlab Box. The execution time was set to 100 μs.

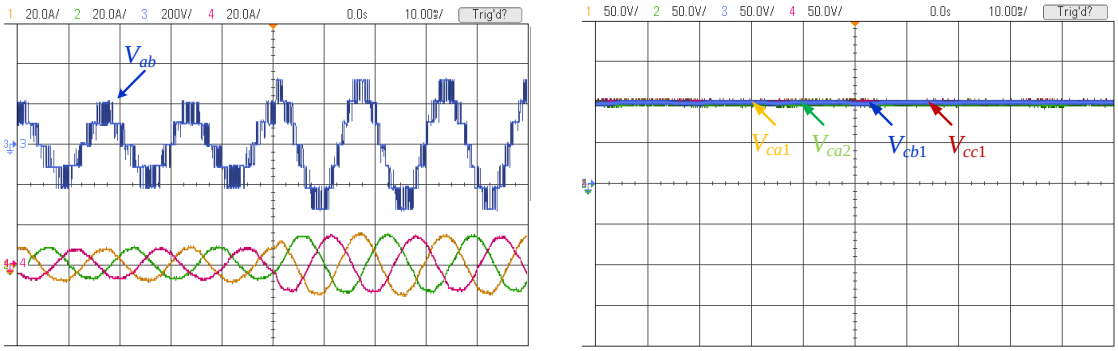
Figure 4.5 and Figure 4.6 show the performance of the proposed controller under different operating conditions. Figure 4.5 shows the inverter output voltage, output currents, and flying capacitor voltages where modulation index $m = 0.95$ and load power factor PF=0.9.

Figure 4.6 also shows the inverter output voltage, output currents, and flying capacitor voltages where modulation index changes from $m = 0.9$ to $m = 0.5$. As can be seen from the experimental results, all the capacitors are well balanced during the steady-state and transient conditions.



(a) inverter voltage and output currents (b) voltage of flying capacitors

Figure 4.5 Steady-state condition with $m = 0.95$, PF=0.9



(a) inverter voltage and output currents (b) voltage of flying capacitors

Figure 4.6 Transient condition where modulation index changes from m=0.9 to 0.5

Despite the excellent performance of the developed SVM-based control technique, the complexity of the SVM-based control technique due to the high number of switching states of the four-level T-NNPC is its main disadvantage. This challenge can limit the practical application of the developed control technique, where other control objectives must be satisfied. Such as DC-link voltage and PF control in charging applications. Therefore, a simpler controller based on SPWM is developed in the next section.

4.4 The Proposed SPWM Based Modulation Technique to Control Flying Capacitor Voltages of the Four-Level T-NNPC

Capacitor voltage balancing of a T-Type NNPC converter is a technical challenge to make sure that the converter can operate properly under different operating conditions. If there is no control, the flying capacitors will be charged or discharged during the converter operation and the capacitors' voltages will deviate from the desired values and thus the converter cannot generate a four-level output voltage. In this Section, a new control technique based on the SPWM scheme is explained.

The deviation of the capacitor voltages from the desired value (V_{dc} / 3) can be written as:

$$\Delta V_{Cxi} = V_{Cxi} - V_{dc}/3 \qquad x = a,b,c \quad i = 1,2 \tag{4.8}$$

To balance the capacitor voltages, ΔV_{CXi} (x=a,b,c, i=1,2) should be zero or close to zero under all operating conditions. If the voltage deviation is positive, a switching state should be selected to discharge the capacitor and if the deviation is negative, the switching state should be selected to charge the capacitor.

However, as it can be seen from Table 4.2, for some switching states, capacitors of a phase are jointly charged and discharged which is a challenge for controlling the capacitor voltages. For example, assuming the voltage level is 1, if the deviation

for C_1 is positive and the deviation of C_2 is negative, and the output current is larger than zero, choosing state 1A will charge C_2 toward the desired value but also it charges C_1 more, and deviation for C_1 will increase, which is not desirable.

To solve this problem, Table 4.6 is developed that shows the procedure of selecting the best switching state to balance the voltages of the capacitors at $V_{dc}/3$. For levels 0 and 3, there is no redundant switching state and these two levels do not affect the capacitor voltages. However, for levels 1 and 2, there are redundant switching states, and based on the current direction and voltage deviation of the capacitors, the best switching states will be selected from Table 4.6.

TABLE 4.6 THE PROPOSED VOLTAGE CONTROL METHOD

Output Level	i_x	ΔV_{CX1}	ΔV_{CX2}	Condition	State
1	≥ 0	≥ 0	≥ 0	-	1A
			< 0	-	1B
		< 0	≥ 0	$\lvert\Delta V_{CX1}\rvert < \lvert\Delta V_{CX2}\rvert$	1A
				$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX2}\rvert$	1B
			< 0	-	1B
	< 0	≥ 0	≥ 0	-	1B
			< 0	$\lvert\Delta V_{CX1}\rvert < \lvert\Delta V_{CX2}\rvert$	1A
				$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX2}\rvert$	1B
		< 0	≥ 0	-	1B
			< 0	-	1A
2	≥ 0	≥ 0	≥ 0	-	2A
			< 0	-	2A
		< 0	≥ 0	$\lvert\Delta V_{CX1}\rvert < \lvert\Delta V_{CX2}\rvert$	2A
				$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX2}\rvert$	2B
			< 0	-	2B
	< 0	≥ 0	≥ 0	-	2B
			< 0	$\lvert\Delta V_{CX1}\rvert < \lvert\Delta V_{CX2}\rvert$	2A
				$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX2}\rvert$	2B
		< 0	≥ 0	-	2A
			< 0	-	2A

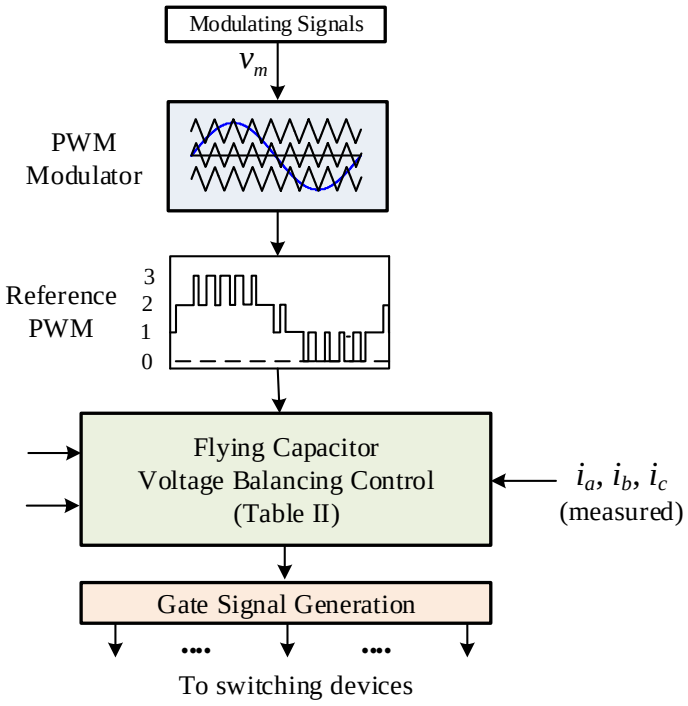


Figure 4.7 Block diagram of capacitor voltage balancing

For instance, when the output voltage level is 1, and $i_x \geq 0$, $\Delta V_{Cx1} \leq 0$, $\Delta V_{Cx2} \leq 0$, both capacitors need to be charged, and thus switching state 1B should be selected.

The flowchart shown in Figure 4.7 shows the procedure to control the voltage of flying capacitors in each phase:

- First, by comparing carriers (three carriers for a four-level converter) and the modulation signal, the desired output voltage level is determined.
- The direction of the phase currents and capacitor voltages should be measured.

- Based on the output voltage level, the current direction, and capacitor voltage deviations, the proper switching state will be selected from Table 4.6.
- And finally, the gate signals are generated and applied to the switching devices.

4.4.1 Simulation Studies

Simulation studies have been done in the MATLAB/Simulink environment to show the performance and the effectiveness of the proposed control method implemented by SPWM for a 1 MVA/4.16 KV converter. Simulation studies have been done for both AC/DC and DC/AC applications such as ultra-fast charging stations and motor drives respectively.

A. 4-Level T-NNPC as an AC/DC Converter in Charging Applications

In this part, the performance of the four-level T-NNPC converter and the developed controller is examined for AC/DC conversion mode in MV-connected ultra-fast charging applications. A 1 MVA charging station is considered, where the grid voltage is 4.16 kV. The AC/DC converter works as a boost converter, therefore the DC-link voltage must be greater than the peak of the input voltage and is selected to be 8 kV, however, depending on the DC/DC configuration, other voltage levels can be selected. The parameters of the system under study are shown in Table 4.7.

TABLE 4.7 PARAMETERS OF THE STUDY SYSTEM

Converter parameters	Values
Converter rating (MVA)	1
Capacitor Value (µF)	2200
grid voltage (kV)	4.16kV
Output frequency (Hz)	60
Line inductance (mH)	5

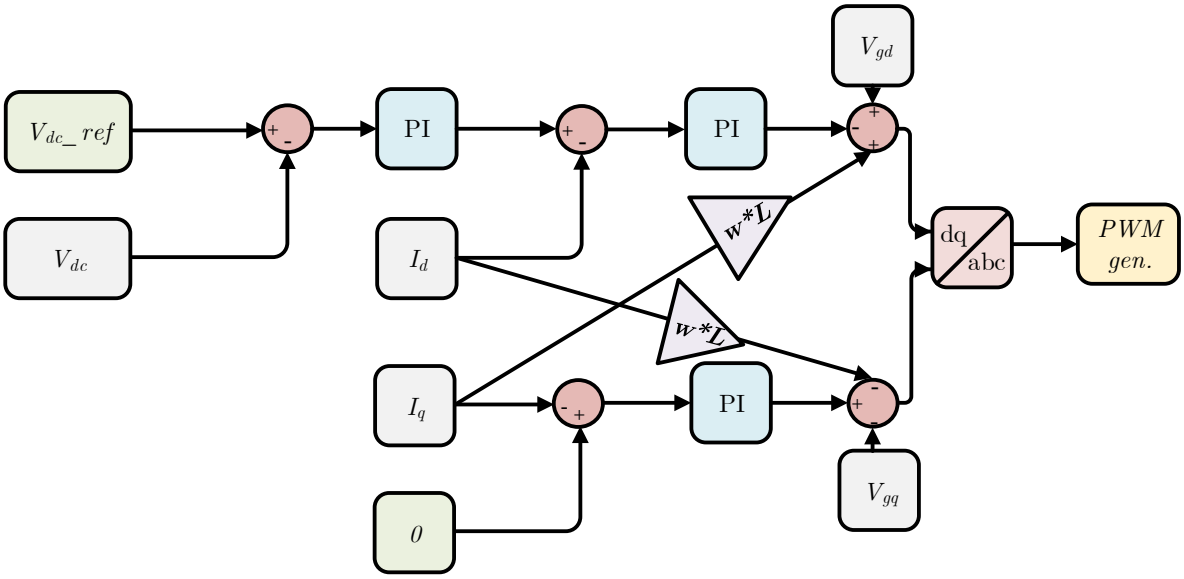


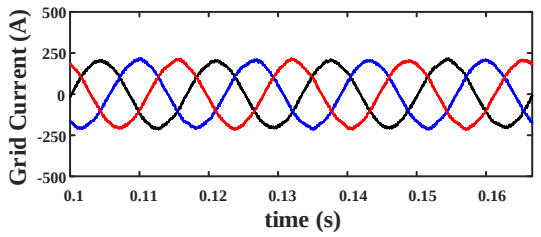
Figure 4.8 Developed Controller for the MV connected charging station

The AC/DC rectifier in an MV-connected charging station acts as a power factor correction stage while providing a regulated DC-link voltage. Therefore, a controller is developed to set the power factor of the charging station close to 1 and balance the DC-link at 8 kV as shown in Figure 4.8.

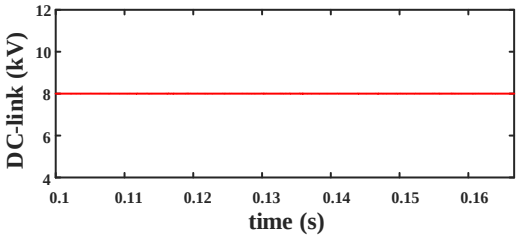
As can be seen in Figure 4.8, a PI controller is used to generate the *d*-component of the current reference of the grid current, and the *q*-component is set

to 0 to set the power factor to 1. Moreover, the d-q components of the grid voltage and line reactance are used as compensation for the PI regulators.

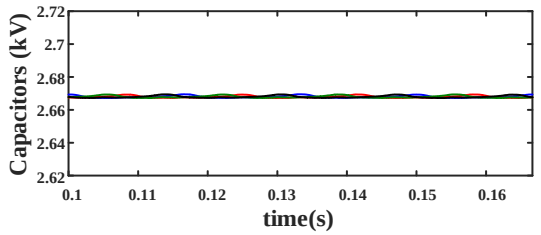
The performance of the four-level topology and the controller is examined in two operating conditions in Figure 4.9. In Figure 4.9, the load power is set to 1 MVA, as can be seen the DC-link voltage and flying capacitors are balanced at 8kV and 2667 V (=8000/3) respectively while the q-component of the grid current is 0, and the THD of the grid currents are less than 3.37%.



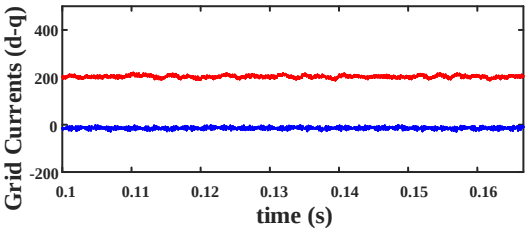
(a) Grid current



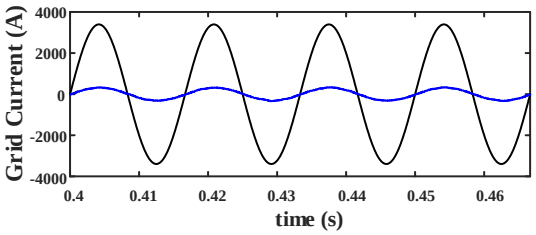
(b) DC-link voltage



(c) Flying capacitor voltages



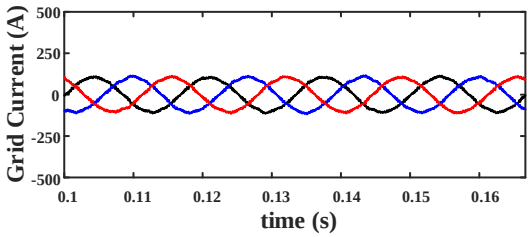
(d) Grid current d-q components



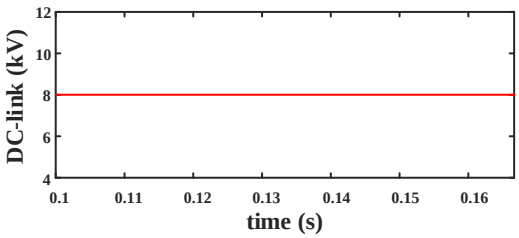
(e) Grid voltage and Current (phase a)

Figure 4.9 AC/DC conversion mode for ultra-fast charging station, 1 MW

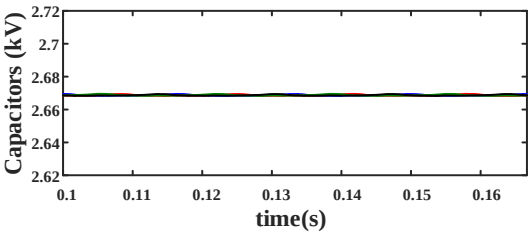
Since the AC/DC converter of a charging station must be able to deliver the power based on the power required to charge the vehicles at any time, the performance of the four-level topology and the developed controller is examined at half of the charging station power rating (0.5 MW) shown in Figure 4.10. As can be seen, all the voltages are well regulated and the q-component of the grid current is set to 0 while the THD is limit to 5%.



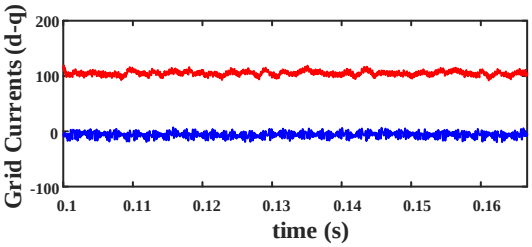
(a) Grid current



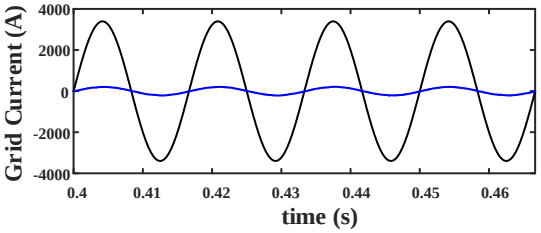
(b) DC-link voltage



(c) Flying capacitor voltages



(d) Grid current d-q components



(e) Grid voltage and Current (phase a)

Figure 4.10 AC/DC conversion mode for ultra-fast charging station, 500 kW

B. 4-Level T-NNPC as a DC/AC converter in Industrial Motor Drives

To investigate the performance of the four-level topology and the developed controller in a wider range of operating conditions, simulation studies have been done for DC/AC conversion mode for applications such as industrial motor drives. The parameter of the system under the study are shown in Table 4.8.

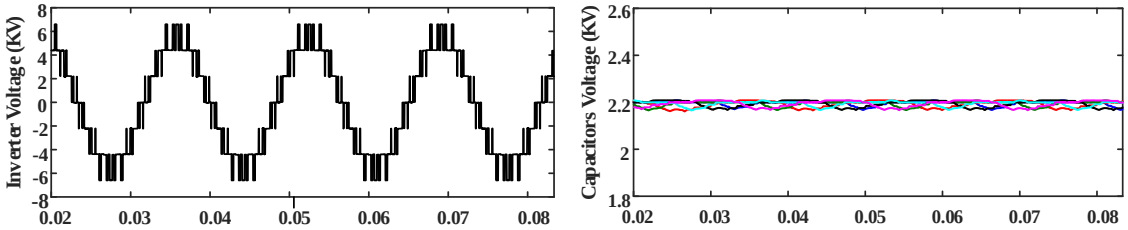
TABLE 4.8 PARAMETERS OF THE STUDY SYSTEM

Converter parameters	Values
Converter rating (MVA)	1
Capacitor Value (μF)	2200
Output frequency (Hz)	60
Output inductance (mH)	5.5
Output load (Ω)	64

Figure 4.11 shows the output voltage and capacitor voltages where the modulation index is m = 0.95, load PF = 0.95. Figure 4.12 shows the same results for m = 0.7 and PF = 0.7. As it is shown in Figure 4.11 and Figure 4.7 capacitors voltages are well balanced at the desired value which is one-third of total DC-link voltage (2.2 kV).

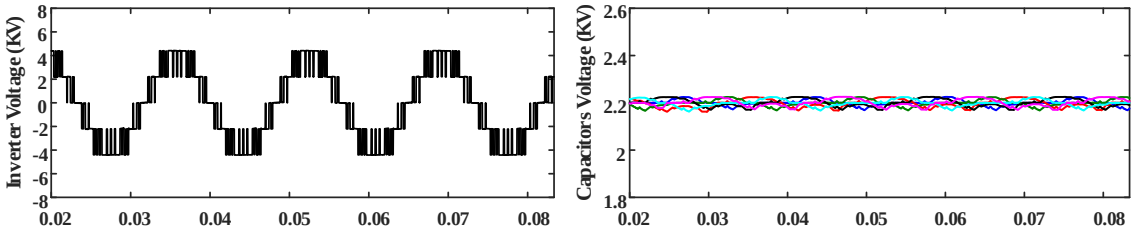
Figure 4.13 shows the output and capacitor voltages when the modulation index changes from m = 0.95 to m = 0.55. As can be seen, the controller can maintain the capacitor voltages at 2.2 kV which is desired value. Figure 4.14, shows the performance of the controller when the controller is deactivated and activated. Without the controller,

capacitors start to diverge and when the controller is activated, the capacitor will be converged.



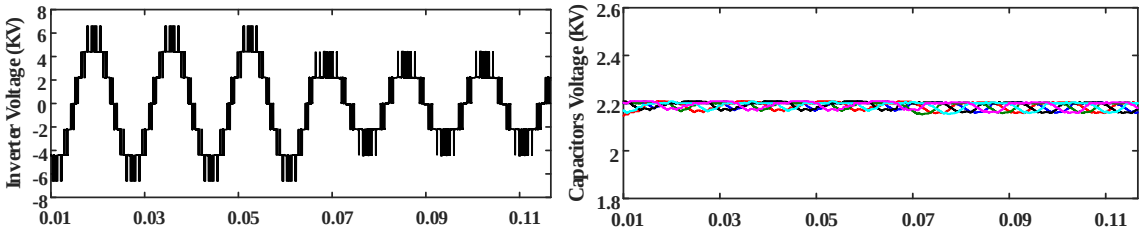
(a) Inverter voltage (b) Flying capacitor voltages

Figure 4.11 Steady-state simulation with m=0.95, PF=0.95



(a) Inverter voltage (b) Flying capacitor voltages

Figure 4.12 Steady-state simulation with m=0.7, PF=0.7



(a) Inverter voltage (b) Flying capacitor voltages

Figure 4.13 Step change from m=0.95 to m=0.55

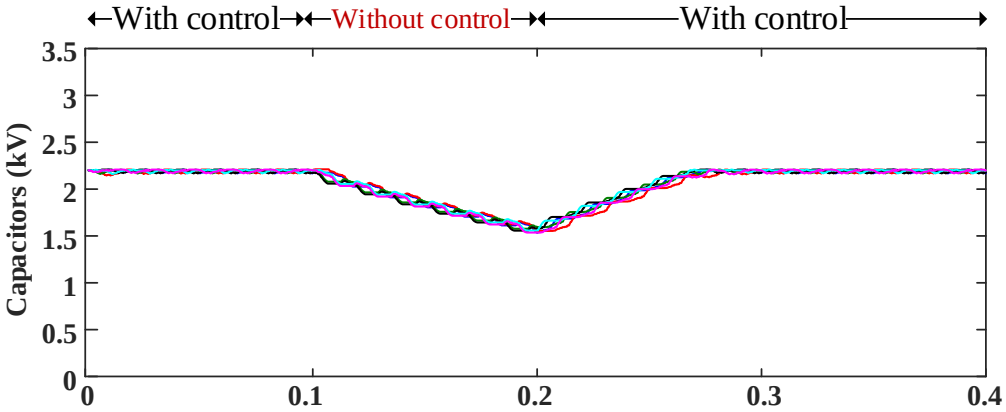


Figure 4.14 Voltage of flying capacitor when the controller is deactivated and activated

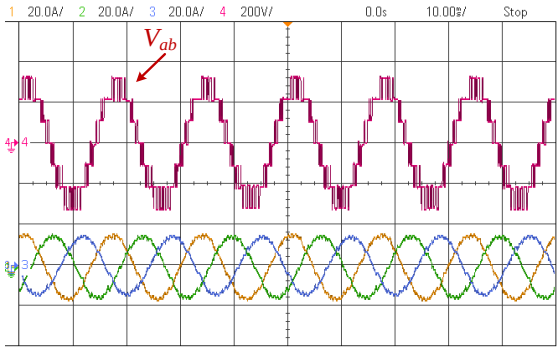
4.4.2 Experimental Results

The feasibility of the proposed control technique based on the SPWM scheme is evaluated experimentally for a DC/AC conversion mode since a wider operating range can be examined. The parameters shown in TABLE 4.9 are used to obtain the experimental results on a scaled-down prototype.

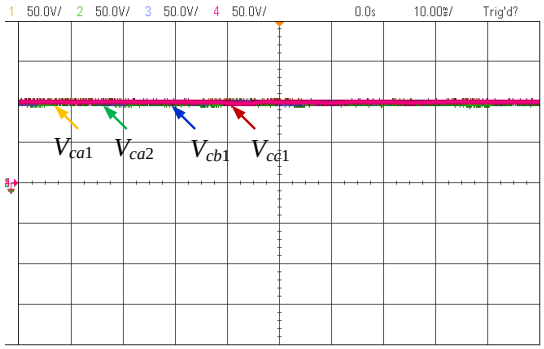
TABLE 4.9 PARAMETERS OF THE STUDY SYSTEM

Converter parameters	Values
Converter rating (kVA)	5
Capacitor Value (μF)	2200
Input dc voltage (V)	320
Output frequency (Hz)	60
Output inductance (mH)	5
Output load (Ω)	12

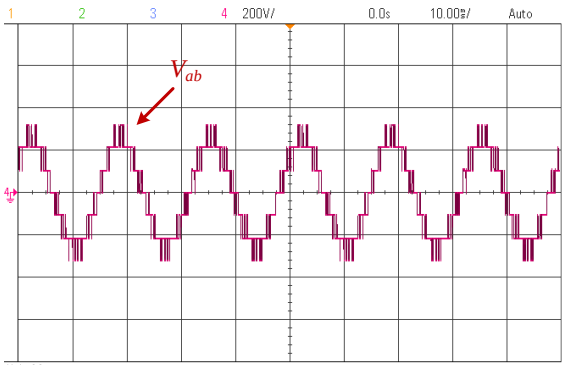
Figure 4.15 to 4.18 show the performance of the proposed control technique under steady-state and transient conditions.



(a) line voltage and output currents (200V/div, 10A/div, 10ms/div)

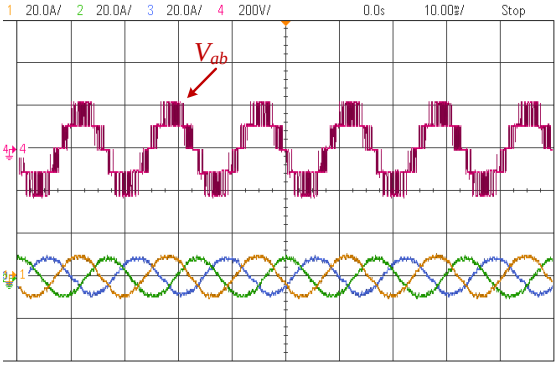


(b) voltages of flying capacitors (50V/div, 10ms/div)

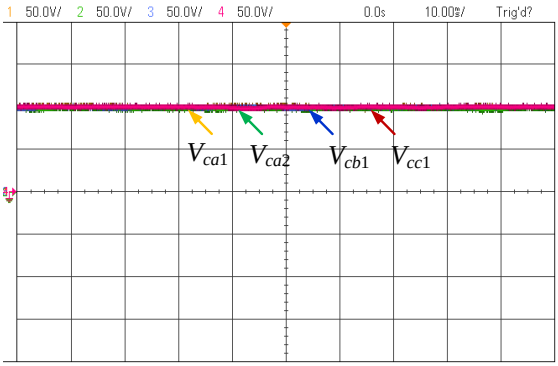


(c) line voltage with dc sources (200V/div, 10ms/div)

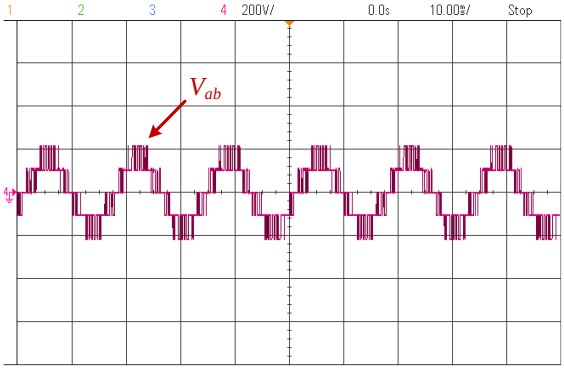
Figure 4.15 Experimental results, $m = 0.9$ and PF=0.9



(a) line voltage and output currents (200V/div, 10A/div, 10ms/div)

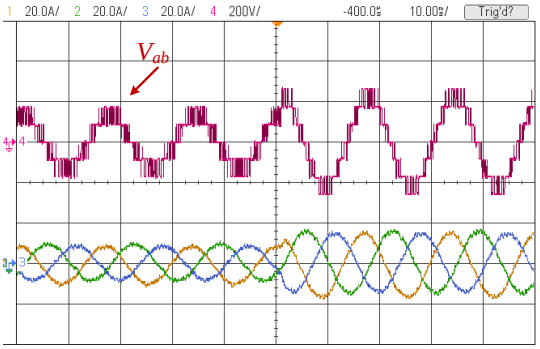


(b) voltages of flying capacitors (50V/div, 10ms/div)

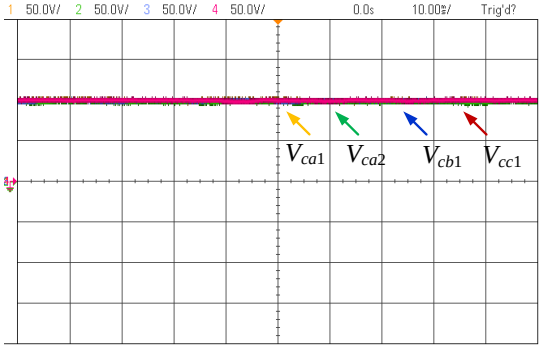


(c) line voltage with dc sources (200V/div, 10ms/div)

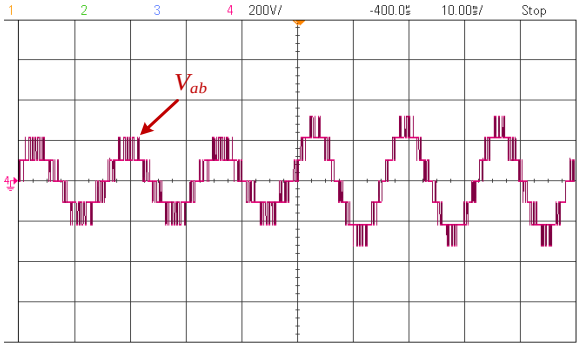
Figure 4.16 Experimental results, $m = 0.55$ and PF=0.9.



(a) line voltage and output currents
(200V/div, 10A/div, 10ms/div)



(b) voltages of flying capacitors(50V/div, 10ms/div)



(c) line voltage with dc sources
(200V/div, 10ms/div)

Figure 4.17 Experimental results, modulation change from m=0.9 to m=0.5

Figure 4.15 shows the inverter output voltage, output currents, and flying capacitor voltages where modulation index $m = 0.9$ and load $PF = 0.9$. The inverter output voltage THD is 24.7%. Figure 4.15 (c) shows the inverter output voltage

with constant dc sources and is based on the controller in [82]. In this case, the output voltage THD is 24%. Figure 4.16 also shows the inverter output voltage, output currents, and flying capacitor voltages where modulation index $m = 0.55$ and load $PF = 0.9$. The inverter output voltage THD is 40.7%. Figure 4.16 (c) shows the inverter output voltage with constant dc sources and is based on the controller in [82]. In this case, the output voltage THD is 40.4%.

Figure 4.17 shows the performance of the converter when the modulation index changes from $m = 0.55$ to $m = 0.9$. Figure 4.17 (c) shows the inverter output voltage with constant dc sources and is based on the controller in [82].

Figure 4.18 shows the performance of the controller when the controller is deactivated and reactivated. Without the controller, capacitors start to diverge and when the controller is activated, the capacitor will be converged. As can be seen from Figure 4.15 to Figure 4.18 show the effectiveness of the proposed controller and demonstrate that all capacitor voltages are well balanced at different operating conditions.

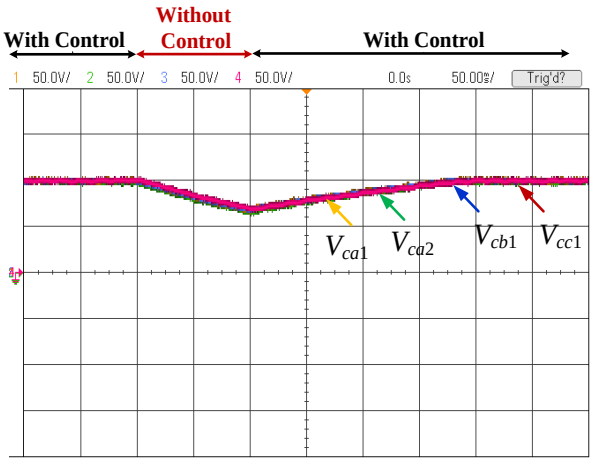


Figure 4.18 Voltage of flying capacitor when the controller is deactivated and activated

4.5 A New Proposed 5-level T-Type NNPC Topology

In this section, a new 5-level T-type NNPC topology shown in Figure 4.19 is proposed. This topology is an upgraded version of the 4-level topology in the previous section. The proposed 5-level T-NNPC topology is very attractive for medium-voltage applications such as MV-connected ultra-fast EV chargers and industrial motor drives. This topology can work in a wide range of voltages (2.4 kV-7.2 kV) without the need for devices in series, and fewer components compared to the other 5-level topologies. A model predictive control strategy (MPC) is also developed for the proposed converter to control the flying capacitor voltages.

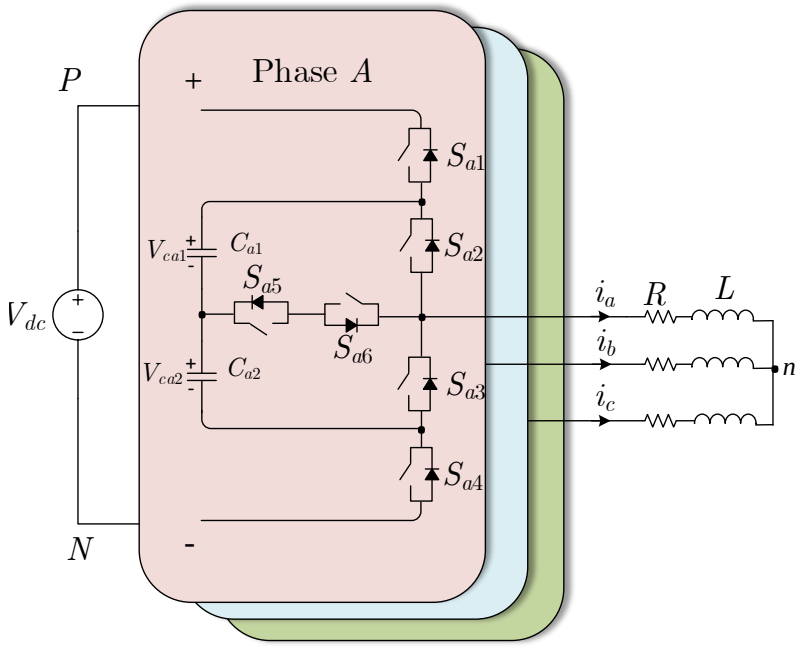


Figure 4.19 Proposed five-level T-type nested neutral point clamped (T-NNPC) converter

A discrete-time model of the converter is developed and the control objectives are defined to regulate the output currents and flying capacitors voltages are.

A cost function is defined to minimize the deviation of the predicted values of the control objectives from their desired values. During each sampling time, the best switching state is selected and applied to the converter. The performance of the proposed 5-level T-NNPC and developed MPC strategy is studied in the MATLAB/Simulink environment for both AC/DC and DC/AC conversion modes, and the feasibility of the converter is evaluated experimentally.

4.5.1 Operation of the Proposed 5-Level T-NNPC Topology

The 5-level T-type NNPC topology is shown in Figure 4.19. This topology is based on the upgraded version of a four-level T-NNPC topology [82] and is a combination of a flying capacitor topology and a T-type converter. In the proposed five-level T-NNPC, to ensure equally spaced steps in the output voltages, the capacitors C_{x1} and C_{x2}, $x = a,b,c$, should be charged and regulate at one-fourth of the dc-link voltage ($V_{dc}/4$) to generate five different voltage levels.

Table 4.10 shows the switching states of the proposed 5-Level converter and the effects of the output currents on the flying capacitor voltages. As can be seen in Table 4.10, six distinct switching states can produce a 5-level voltage at the output. For the Intermediate levels, there are two redundant switching states.

TABLE 4.10 THE SWITCHING STATES OF THE PROPOSED 5-LEVEL T-TYPE NNPC

S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	Vc_{x1}	Vc_{x2}	V_{xN}	level
1	1	0	0	0	0	No impact	No impact	V_{dc}	4
1	0	0	0	1	1	Charging (i_x >0) Discharging (i_x <0)	No impact	$3V_{dc}/4$	3
1	0	1	0	0	0	Charging (i_x >0) Discharging (i_x <0)	Charging (i_x >0) Discharging (i_x <0)	$V_{dc}/2$	2B
0	1	0	1	0	0	Discharging (i_x >0) Charging (i_x <0)	Discharging (i_x >0) Charging (i_x <0)		2A
0	0	0	1	1	1	No impact	Discharging (i_x >0) Charging (i_x <0)	$V_{dc}/4$	1
0	0	1	1	0	0	No impact	No impact	0	0

Each of these switching states has a charging or discharging effect on the flying capacitor voltages with respect to the direction of the current. To balance capacitor voltages at their desired values, the best switching state among all the possible redundant switching states needs to be employed to charge or discharge the flying capacitors.

4.5.2 Advantages and Challenges

A. Advantages

To demonstrate the advantages of the proposed 5-level topology, it is compared to existing advanced 5-level topologies in terms of the number of devices and the voltage ratings of the devices. The proposed 5-level T-NNPC has 18 switches. The voltage rating of each bidirectional switch is $V_{dc}/4$, and it is $V_{dc}/2$ for other switches. This means that 5-level T-NNPC requires 30 switches with the same blocking voltage of $V_{dc}/4$. This topology also requires 6 flying capacitors.

As can be seen from Table 4.11, the proposed 5-level T-NNPC has fewer components in comparison to other classical and advanced five-level topologies. The comparison in Table 4.11 is based on the number of active switches and the number of switches with the same blocking voltage in each topology. The per-unit value is $V_{dc}/4$ (=1p.u). This demonstrates the advantages of the proposed topology in terms of power density, bill of material cost, reliability, and maintenance.

TABLE 4.11 NUMBER OF COMPONENTS IN 5-LEVEL TOPOLOGIES

Topology	switches (1 pu= $V_{dc}/2$)	Diodes	FCs	Blocking voltage p.u.	Switches (1 pu= $V_{dc}/4$)
5-level ANPC [53]	24	0	3	1 to 2	36
New 5-level ANPC [57]	36	0	9	1	36
7-switch 5L-ANPC [58]	27	6	3	1 to 3	39
5-level NNPC [85]	18	6	6	1 to 2	30
5L-FC NNPC [86]	24	6	15	1	24
5-level HC [87]	30	0	6	1	30
Proposed 5-level T-NNPC	18	0	6	1 to 2	30

B. Challenges;

In the proposed 5-level T-NNPC, the voltages of the flying capacitors need to be controlled at one-fourth of the dc-link voltage. SPWM and SVM control schemes are not able to regulate capacitor voltages when the converter operates at low frequency or high power factors. This is due to the lack of enough redundant switching states in this topology.

The SPWM technique can only use phase redundant switching states to charge/discharge the capacitors. However, there is only one redundant switching state for mid-level in each phase. At low-frequency operation, the controller applies the switching state for a longer time and because there is not enough redundant switching state for every level, therefore there is no control on the voltages of the

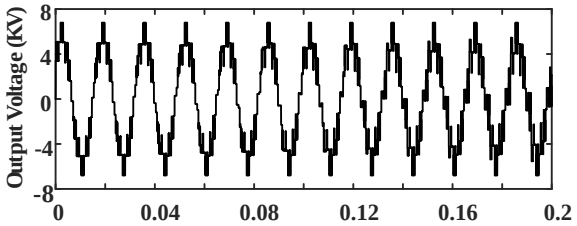
capacitors for a long interval. This will cause deviation of the flying capacitor voltages from their desired values.

Although the SVM technique employs line-to-line redundant switching states to control capacitor voltages, still the switching states are limited to the three adjacent vectors, and they are not enough to control capacitor voltages.

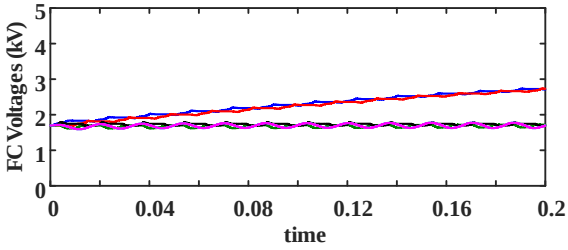
Figure 4.20 shows the outputs of the converter and flying capacitor voltages, where the controller is developed based on the SPWM scheme, the power factor is 0.90, and the frequency is 60 Hz. As can be seen from Figure 4.20, the flying capacitor voltages cannot be balanced at their desired values. Figure 4.21 shows the results when the frequency is 5Hz, and the power factor is 0.7. Figure 4.21 (b) illustrates that the capacitor voltages have large voltage fluctuations around their nominal values.

In Figure 4.22, the controller is based on the SVM scheme, and the power factor is 0.9. Figure 4.22 (b) shows that flying capacitor voltages deviate from nominal values when the power factor is 0.9.

It can be seen from Figure 4.20 to Figure 4.22 that where the SPWM or SVM controller is used for the proposed converter, the capacitor voltages are not regulated at high power factor or low-frequency operation.

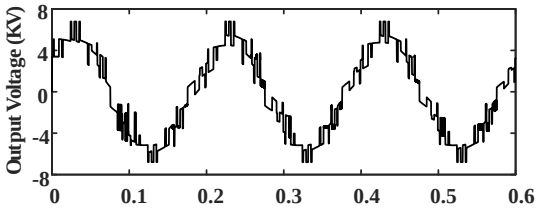


(a) Output currents

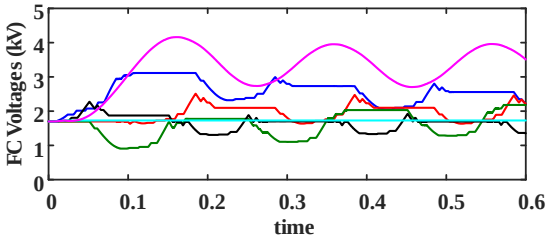


(b) Flying capacitor voltages

Figure 4.20 Steady-state: controller based on SPWM, f=60Hz, PF = 0.9

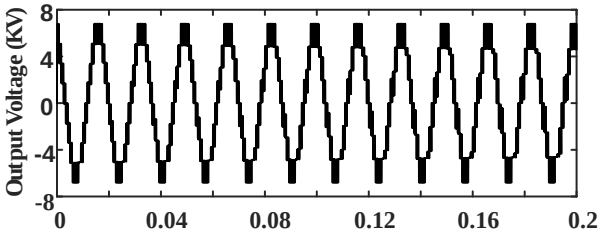


(a) Output currents

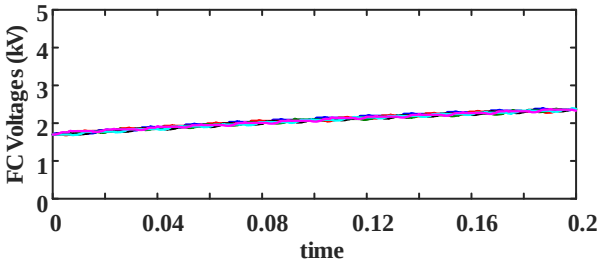


(b) Flying capacitor voltages

Figure 4.21 Steady-state: controller based on SPWM, f=5Hz, PF=0.7



(a) Output currents



(b) Flying capacitor voltages

Figure 4.22 Steady-state: controller based on SVM, f=60Hz, PF = 0.90

A finite control set model predictive control (FCS-MPC) is a technique that has been widely used in power electronics and motor drive applications [88]. The

concept of this control scheme is achieving the control goals, using a cost function, and selecting the best switching state, which minimizes the cost function during the next sampling interval.

An FCS-MPC method is developed to control the capacitor voltages at one-fourth of dc-link voltage while controlling the output currents at the desired amplitude and frequency. Load currents and flying capacitor voltages, which are control objectives, are modeled in the discrete-time domain regarding the switching states. A cost function is defined to minimize the deviation of each control objective from its nominal values. In each sampling interval, predicted values of the control objectives are calculated for the next interval, and the best switching state that minimizes the cost function is selected, and then applied to the converter.

4.5.3 Mathematical Model of the Currents and Voltages

In this section, the continuous-time mathematical model of the power converter output current, and the flying capacitor voltages are obtained. Kirchhoff's voltage law is applied to the converter circuit shown in Figure 4.19 to obtain the converter voltage in term of load currents as the following equations;

$$\begin{aligned} V_{aN} &= Ri_a + L\frac{di_a}{dt} + V_{nN} \\ V_{bN} &= Ri_b + L\frac{di_b}{dt} + V_{nN} \\ V_{cN} &= Ri_c + L\frac{di_c}{dt} + V_{nN} \end{aligned} \tag{4.9}$$

where, V_{xN}, $x = a, b,$ and $c,$ is the converter phase voltage with respect to the negative dc-link voltage (N). R and L is the sum of load and filter resistance and inductance, with the assumption of the same value for all three phases. i_a, i_b, and i_c are load currents of phase a, b, and c respectively. V_{nN} is the voltage difference between the neutral point of the load and negative dc-link voltage, and can be calculated as;

$$\begin{aligned} V_{nN} &= \frac{1}{3}(V_{aN} + V_{bN} + V_{cN}) \\ V_{xn} &= V_{xN} - V_{nN} \\ x &= a, b, c \end{aligned} \tag{4.10}$$

The equation 4.9) can be rewritten as;

$$V_o = Ri_o + L\frac{di_o}{dt}; \quad \begin{aligned} V_o &= \begin{bmatrix} V_{an} & V_{bn} & V_{cn} \end{bmatrix}^T \\ i_o &= \begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^T \end{aligned} \tag{4.11}$$

The continuous-time model of load current can be obtained from (4.11);

$$\frac{di_o}{dt} = \frac{1}{L}[V_o - Ri_o] \tag{4.12}$$

And the flying capacitor mathematical model can be obtained as follow;

$$
\begin{aligned}
v_{Cx1}(t) &= v_{Cx1}(0) + \int_{0^+}^{t} i_{Cx1}(\tau)d\tau \\
v_{Cx2}(t) &= v_{Cx2}(0) + \int_{0^+}^{t} i_{Cx2}(\tau)d\tau \\
x &= a,b,c
\end{aligned}
\tag{4.13}
$$

where; V_{Cx}, x= *a, b, c,* is the capacitors' voltages, and i_{Cx}, is the current passing through each capacitor.

4.5.4 Model Predictive Control of the Proposed 5-level T-type NNPC

The finite control set model predictive control (FCS-MPC) has gained more interest in power electronics applications due to its capability of controlling multivariable systems with constraints and nonlinearity, and the existence of an accurate mathematical model of the power converters. This control method is an optimization algorithm that can be easily implemented on digital control platforms, and it does not require linear regulators and modulators.

The block diagram of the developed model predictive control for the 5-level T-NNPC is shown in Figure 4.23, where i_o is the three-phase output currents and V_c represents flying capacitors' voltages.

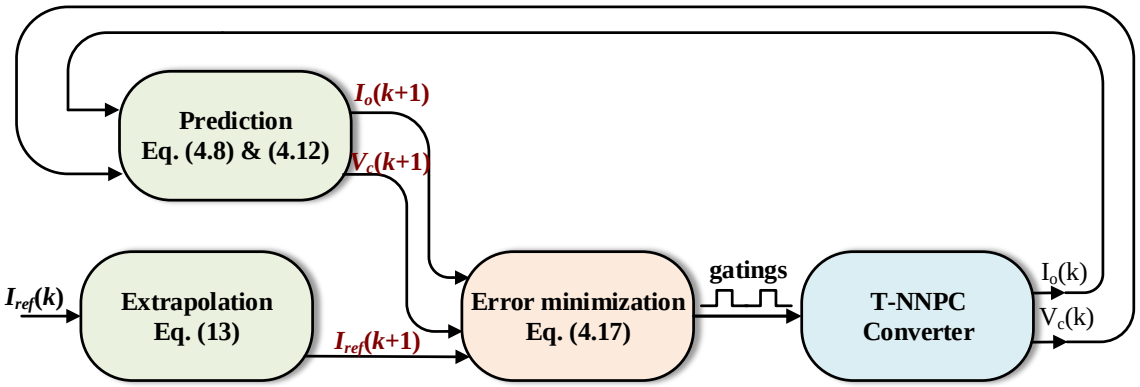


Figure 4.23 Model predictive control strategy for the 5-level T-NNPC converter

For implementing FCS-MPC, the discrete-time mathematical model of the power converter and load is needed. All control objectives should be represented in terms of the power converter parameters and the switching states. MPC first predicts each control objective for the next sampling interval, then compares the predicted values with reference values and selects the best switching state for the next sampling time to minimize the error between the control objectives and reference values. In the following, the discrete-time model of the power converter, and the prediction of the control objectives are obtained.

A. Discrete-time mathematical model of the power converter;

Implementing the model predictive control algorithm in digital controllers requires conversion of the continuous-time model to discrete-time model. To convert the continuous-time model of the output current (4.12) to discrete-time model, the backward Euler method can be used to obtain the first-order derivative as follow;

$$\frac{di_o}{dt} = \frac{i_o(k+1) - i_o(k)}{T_s} \tag{4.14}$$

T_s is the sampling interval. Combination of (4.12) and 4.14), results in the discrete-time model of output current [88];

$$i_o(k+1) = K_v V_o(k+1) + K_i i_o(k) \tag{4.15}$$

where;

$$\begin{aligned} K_v &= \frac{T_s}{L + RT_s} \\ K_i &= \frac{L}{L + RT_s} \end{aligned} \tag{4.16}$$

Based on 4.15), predicting output current for the next sampling interval (k+1) requires the value of the output current at time instant k and predicted output voltage ($V_o(k+1)$). Output current at time instant k can be obtained by using current sensors.

The output voltage can also be calculated in terms of the switching states. Table 4.12 shows the phase voltage respected to the negative point of the dc-link at different switching states. Equation (4.17) is extracted from Table 4.12 to show the relationship between the phase voltage, with respect to negative dc-link voltage (N), and switching states.

$$V_{xN} = S_{x1}(v_{dc} - v_{Cx1} - v_{Cx2}) + S_{x2}(v_{Cx1} + v_{Cx2}) + S_{x5}(v_{Cx2}) \tag{4.17}$$

Replacing 4.17) in (4.10) results in the predicted value of the output voltage for the next sampling interval. Flying capacitors in 5-level T-NNPC should be regulated at one-fourth of the dc-link voltage. This is to make sure that the converter can operate properly to generate five levels at the output and the voltage stress of all switches is the same that is $V_{dc}/4$.

TABLE 4.12 OUTPUT VOLTAGE FOR THE POSSIBLE SWITCHING STATES. X=A, B, C

S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	V_{xN}
1	1	0	0	0	0	V_{dc}
1	0	0	0	1	1	V_{dc} - V_{Cx1}
1	0	1	0	0	0	V_{dc} - V_{Cx1} - V_{Cx2}
0	1	0	1	0	0	V_{Cx1} + V_{Cx2}
0	0	0	1	1	1	V_{Cx2}
0	0	1	1	0	0	0

In this part, a discrete-time mathematical model for the flying capacitor voltages is obtained in terms of switching states, to predict the capacitors' voltages for the next sampling interval.

From Table 4.10, the capacitors current in each phase can be determined regarding switching state as follow;

$$\begin{aligned} &i_{Cx1}(k) = (S_{x1} - S_{x2})i_x(k) \\ &i_{Cx2}(k) = (S_{x3} - S_{x4})i_x(k) \\ &x = a,b,c \end{aligned} \tag{4.18}$$

where; i_x, $x=a,\ b,\ c,$ is the output current of each phase.

Same as the procedure to obtain the discrete-time model for output current, the discrete-time model for capacitors voltage can be calculated using 4.13), and the predicted value for capacitors voltages can be obtained as;

$$\begin{aligned} v_{Cx1}(k+1) &= v_{Cx1}(k) + \frac{T_s}{C_{x1}} i_{Cx1}(k) \\ v_{Cx2}(k+1) &= v_{Cx2}(k) + \frac{T_s}{C_{x2}} i_{Cx2}(k) \\ x &= a,b,c \end{aligned} \qquad 4.19)$$

B. Developing a model predictive algorithm for the proposed converter

In the last section, a discrete-time model for the output currents and flying capacitors voltages are obtained to predict their values for the next sampling interval. To develop a model predictive control strategy, the following steps should be considered;

B1. References: The output current reference is defined based on the application. For instance, for electric motor drives, the current should be defined to meet the requirements for controlling the torque and speed of the motor. For grid-connected applications, the current reference should be defined to control the real and reactive power. To keep the generality of the control method, the current reference is set by the user.

As the predicted value for the next sampling instant needs to be calculated, Langrage extrapolation is used to determine the reference value for the next sampling interval in each sampling time as [89];

$$i_o^*(k+1) = 4i_o^*(k) - 6i_o^*(k-1) + 4i_o^*(k-2) - i_o^*(k-3) \quad 4.20)$$

The reference for flying capacitor voltage is constant during the operation of the converter as explained in the last sections, which is one-fourth of the dc-link voltage;

$$v_{Cx}^* = \frac{V_{dc}}{4} \quad 4.21)$$

B2. Measurements and predictions: As explained earlier, for the prediction of the control objectives, equations (4.14) to are used (4.19), and the values for the output current and flying capacitor voltage at k^{th} instant is required, so three current sensors and six voltage sensors is required to obtain the values of the output currents and capacitor voltages.

B.3 Cost function: To minimize the error between the control objectives and reference values, a cost function should be defined with two control objectives; output currents and flying capacitors voltages. As explained, the output current and capacitors voltages are modeled in terms of the switching states. In each sampling interval, 216 predictions (due to six distinguish switching states for each phase) were obtained for the output current and then compared with references and finally, the best switching states are selected and applied to the converter. The

selected switching states minimize the cost function. First, two cost function is defined for each control objective as follow;

$$J_{current}(k+1) = \sum_{x=A,B,C} \left[i_x^*(k+1) - i_x(k+1) \right]^2$$
$$J_{cap}(k+1) = \sum_{x=a,b,c} \left\{ \sum_{i=1}^{2} \left[v_{Cx}^* - v_{Cxi}(k+1) \right]^2 \right\} \quad 4.22)$$

Then the main cost function is defined with a weighting factor to consider the priority of the minimizing goal, as follow;

$$J(K+1) = J_{cap}(k+1) + \lambda J_{current}(k+1) \quad 4.23)$$

where; λ is the weighting factor. The main goal is to make the cost function close to zero, however as explained, the switching state which minimizes the cost function is selected and then applied to the converter.

4.5.5 Simulation Studies

To examine the performance of the 5-level T-NNPC converter and the developed model predictive controller, simulation studies have been done in MATLAB/Simulink environment for AC/DC and DC/AC conversion modes. The rated value for the converter in the simulation result is 1MVA/4.16KV. The sampling time for the simulation results is 100 µs, and the average calculated switching frequency is around 2000 Hz. The performance of the developed control method to control the output current, output frequency, and regulation of the

capacitor's voltage has been studied during both steady-state and transient operations. Output current and flying capacitors voltages are shown for each case of study in the simulation results.

A. Capacitor Sizing

The flying capacitors values are chosen based on the allowable ripple on the capacitor voltages and the output current THD. The voltage ripple on the flying capacitors and output current THD are considered to be less than 5 %. Ripple analysis has been done for different capacitor values and the results are shown in Table 4.13.

Table 4.13 demonstrates that for smaller values of the flying capacitor, voltage ripple on capacitors and output current THD will increase. Large values for the capacitors will cause less ripple and THD at the output, but it will increase the manufacturing cost as well. Therefore a trade-off is required. To guarantee that the voltage ripple and current THD is less than 5%, the capacitor values are chosen to be 612 µF (=4 pu) for the given parameters in the simulation studies. In this case, the voltage ripple is 1.88 %, and the current THD is 4.24 %.

TABLE 4.13 RIPPLE ANALYSIS

C (μF)	C (pu)	Voltage Ripple (%)	Output current THD (%)
3300	21.5	1.76	2.27
2142	14	1.64	2.50
612	4	1.88	4.24
306	2	2.38	4.99
153	1	2.94	5.43
76	0.5	4.7	5.57
50	0.32	5.2	5.68

B. Performance of the 5-Level T-NNPC in Ultra-Fast Charging

The performance of the proposed 5-level topology is investigated for a 1MVA charging station where the grid voltage is 4.16 kV and the DC-link is 8 kV. The parameters of the system are shown in Table 4.14.

TABLE 4.14 PARAMETERS OF THE STUDY SYSTEM

Converter rating (MVA)	1
Capacitor Value (μF)	612 (4 pu)
Input dc voltage (kV)	6.8
Output frequency (Hz)	60
Line inductance (mH)	5
Output load (Ω)	64

As previously discussed, the control objective for the AC/DC rectifier in a charging station is to provide a regulated DC-link voltage while keeping the power factor close to 1. The block diagram of the developed controller is shown in Figure

4.24. As can be seen, a PI controller is used to generate the *d*-component reference of the grid current from the DC-link voltage error while *the q*-component is set to zero. Then, the current reference is passed to the MPC block to generate the gating that ensures flying capacitors voltages are well balanced.

The simulation results for the rated power and half of the rated power of the charging station are shown in Figure 4.25, and Figure 4.26. As can be seen, in both cases the flying capacitors and DC-link capacitors are well-balanced at 8kV, and 2 kV respectively. Moreover, the q-component of the grid current is set to zero to ensure the high power factor operation of the rectifier. The grid current THD for the rated power is 4.43 % while for half of the rated power is 4.45 %.

These results demonstrate the feasibility and proper performance of the proposed topology as the AC/DC rectifier of an MV-connected ultra-fast charging station.

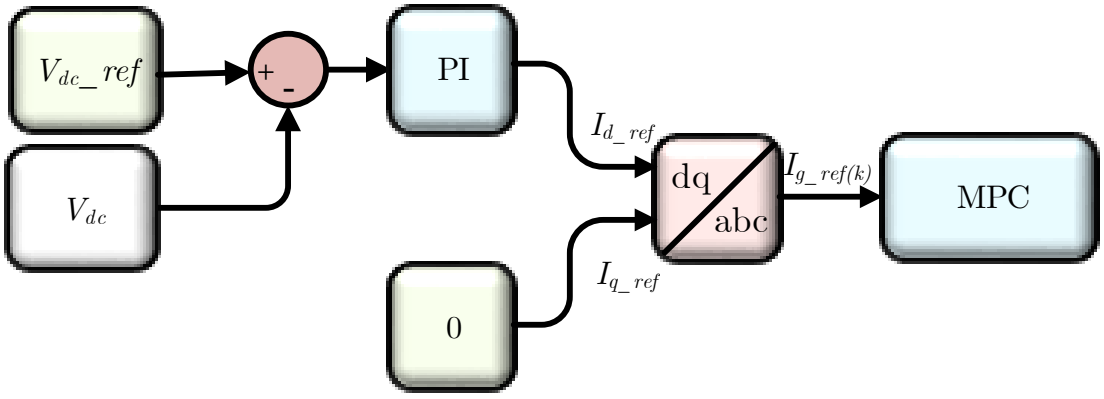
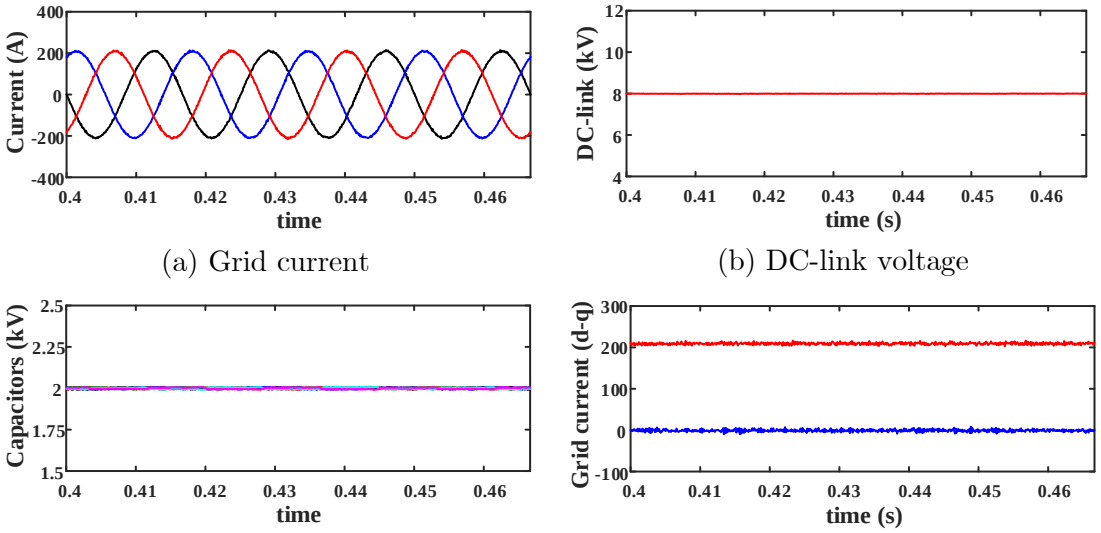


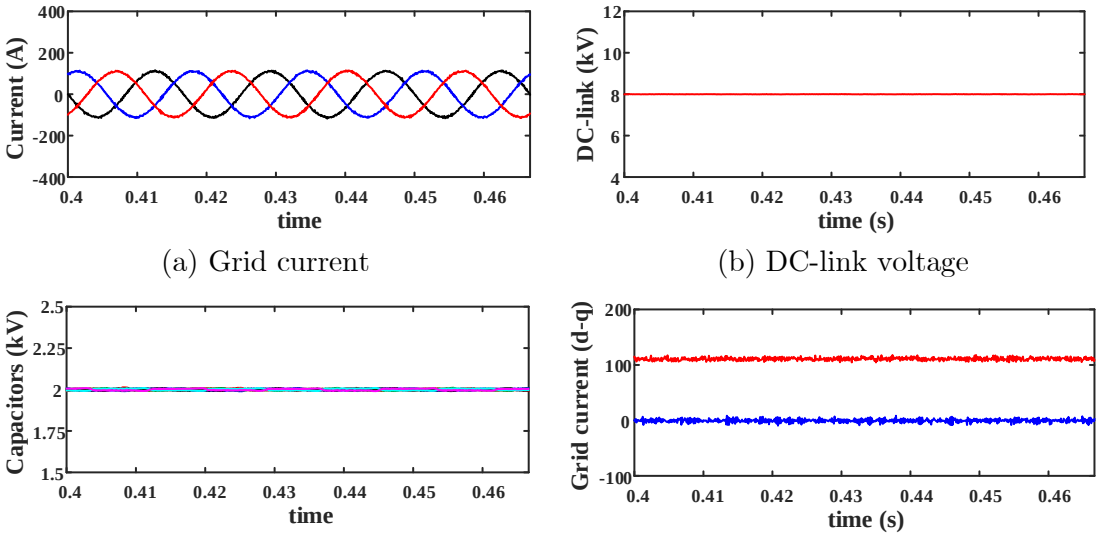
Figure 4.24 Controller Block Diagram for the proposed 5-level TNNPC for MV ultra-fast charging stations



(a) Grid current (b) DC-link voltage

(c) Flying capacitor voltages (d) Grid current d-q components

Figure 4.25 5-Level TNNPC; AC/DC conversion mode for ultra-fast charging station, 1 MW



(a) Grid current (b) DC-link voltage

(c) Flying capacitor voltages (d) Grid current d-q components

Figure 4.26 5-Level TNNPC; AC/DC conversion mode for ultra-fast charging station, 0.5 MW

Compared to the four-level T-NNPC, the voltage stress on the active switches of the five-level T-NNPC is reduced to 2000 V and the THD with the same filter size is reduced by almost 1 %.

C. Industrial motor drives

In this part, the performance of the proposed 5-level TNNPC is evaluated for industrial motor drive application to examine the feasibility of the proposed topology in a wider operating range. The parameters of the study system are shown in Table 4.15.

The reference current predicted current, and the output current in one cycle is shown in Figure 4.27 The reference current predicted current and the output current. The output current follows the reference perfectly and the predicted current. This shows the effectiveness of the developed control technique.

TABLE 4.15 THE PARAMETERS OF THE STUDY SYSTEM

Converter rating (MVA)	1
Capacitor Value (µF)	612 (4 pu)
Input dc voltage (kV)	6.8
Output frequency (Hz)	60
Output inductance (mH)	10.5
Output load (**Ω**)	15.5

Figure 4.28 shows the performance of the 5-level T-type NNPC, in which the output current reference is set to 0.9pu of the rated output current (i.e., i_o=176 A)

and load power factor (PF) is set to 0.9. Figure 4.29 shows the simulation results where the output current is 0.2pu (i_o =39.2 A) and PF=0.9. Figure 4.29 shows the simulation results where the reference is set to 0.9 pu and PF is 0.3. As can be seen from the simulation results, the output current can track the reference currents at different power factors. Moreover, the controller can balance the flying capacitor voltages at their reference values, $V_{dc}/4$=1700 V, under different operating conditions.

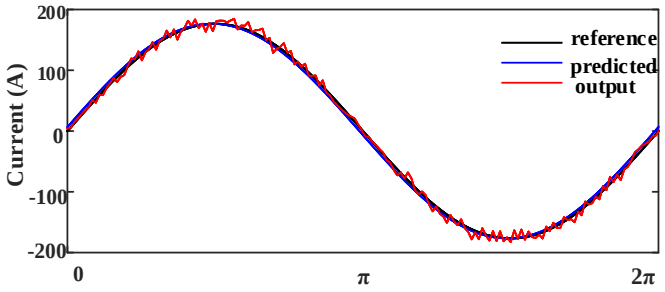
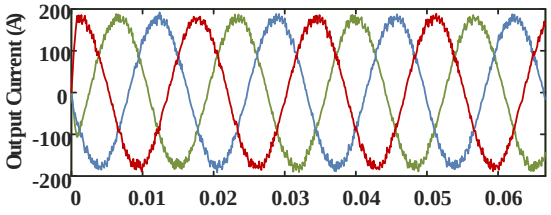
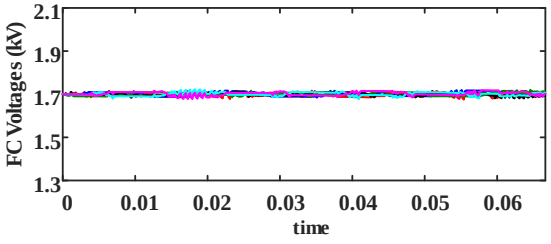


Figure 4.27 The reference current predicted current and the output current

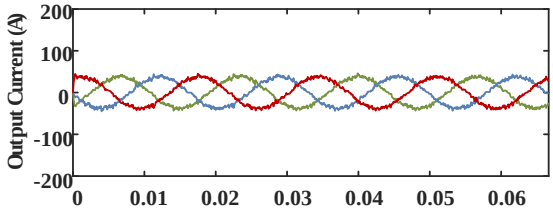


(a) Output currents

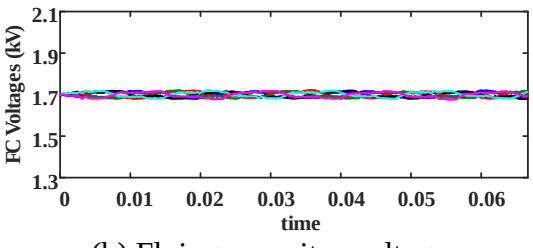


(b) Flying capacitor voltages

Figure 4.28 Steady-state: i_{ref} = 0.9pu, PF = 0.9

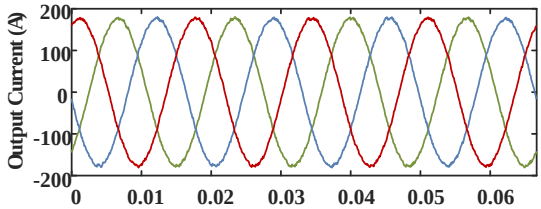


(a) Output currents

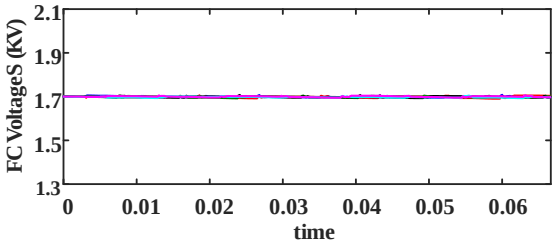


(b) Flying capacitor voltages

Figure 4.29 Steady-state: i_{ref} = 0.2pu, PF = 0.9



(a) Output currents



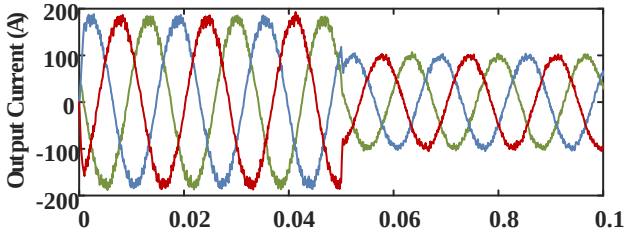
(b) Flying capacitor voltages

Figure 4.30 Steady-state: i_{ref} = 0.9pu, PF = 0.3

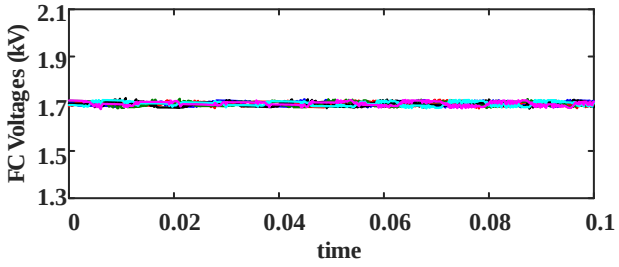
Figure 4.31 shows the output current and flying capacitor voltages where current reference changes from 0.9pu (176A) to 0.5pu (98A). As can be seen from Figure 4.31, the controller can follow the reference current and maintain the flying capacitor voltages at the reference value of 1.7kV.

Figure 4.32 shows the performance of the controller when output frequency changes from 5Hz to 30Hz, 60Hz, and 90Hz. As can be seen from Figure 4.32, the controller can track the reference currents from low frequency (5Hz) to high frequency (90Hz). The capacitor voltages are also maintained at reference values during the frequency changes. This study shows that the 5L- TNNPC converter with the developed controller could be a good candidate for motor drive applications where the motor runs from low speed to rated speed.

Figure 4.33, shows the performance of the controller. Figure 4.33, the controller is deactivated at t=0.05s and then reactivated at t=0.1s. It can be seen that when the controller is deactivated, the capacitors' voltages deviate from the desired values, and after t=0.1s when the controller is activated, the capacitors' voltages start converging to their desired values. This study shows the effectiveness of the controller.



(a) Output currents



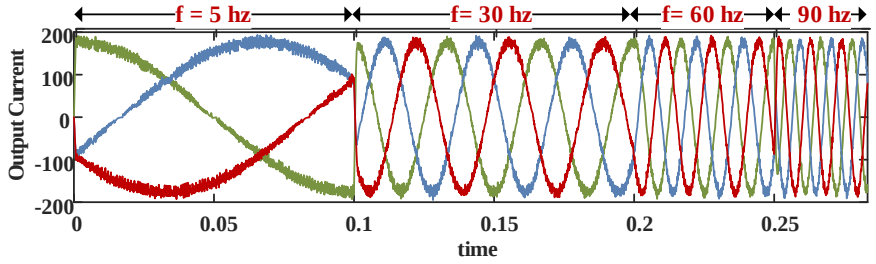
(b) Flying capacitor voltages

Figure 4.31 Transient study: step change of the current reference i_{ref} = 0.9 to 0.5 pu and PF = 0.9

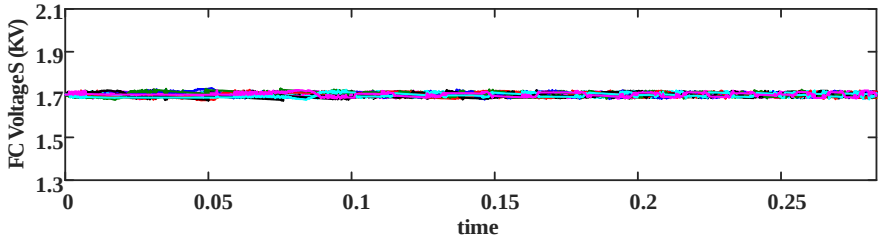
D. THD Analysis

In this section, the Total Harmonic Distortion of the output voltage and current has been examined with respect to the output frequency where $i_{o,ref}$ =I_{rated}, and $i_{o,ref}$ =0.2I_{rated}. The results are shown in Figure 4.34 and Figure 4.35.

Figure 4.34 shows that the output current THD for rated current is around 3%, and the line-to-line voltage is around 22%. As the frequency decreases, the voltage THD increases. For $i_{o,ref}$=0.2I_{rated}, the current THD is around 8%, and the voltage THD is around 100%.



(a) Output currents



(b) Flying capacitor voltages

Figure 4.32 Transient study: current reference change from 0.9pu to 0.5pu and PF = 0.9

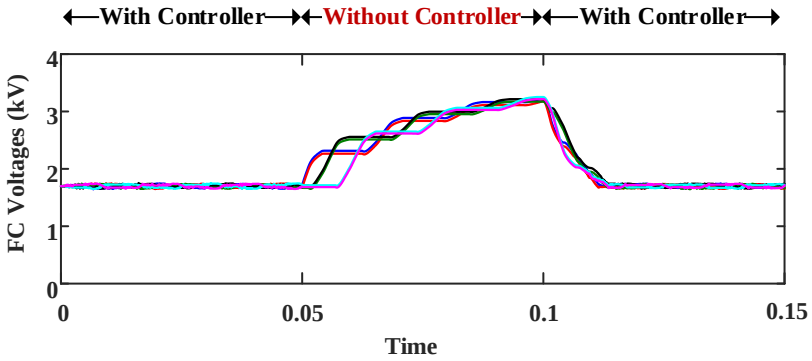


Figure 4.33 Transient study: flying capacitor voltages, the controller deactivated at t=0.05 and reactivated at t=0.1

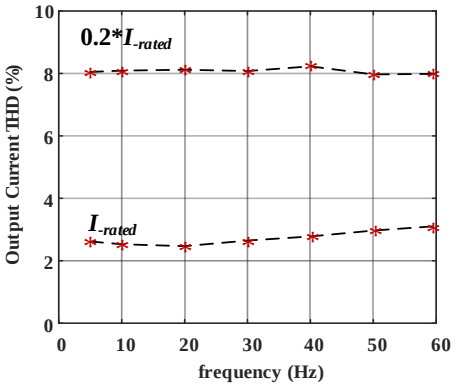


Figure 4.34 Output current THD

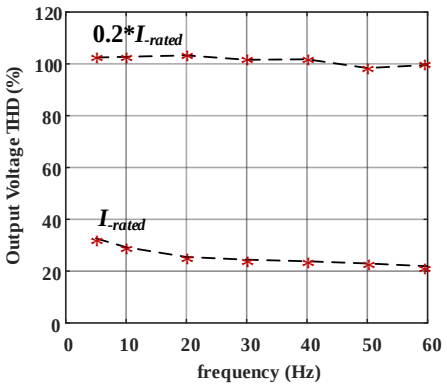


Figure 4.35 Output voltage THD

4.5.6 Experimental Results

The feasibility of the proposed converter and developed model predictive control is evaluated experimentally with DC/AC conversion mode. The parameters used to obtain the experimental result are shown in Table 4.16.

Figure 4.36 to Figure 4.41 show the performance of the converter and developed control technique under steady-state and transient conditions. Figure 4.36 shows the ability of the developed control method in control of the output current, by comparing the reference current and the output current.

TABLE 4.16 PARAMETERS OF THE STUDY SYSTEM

Converter parameters	Values
Converter rating (kVA)	4
Capacitor Value (μF)	4700
Input dc voltage (V)	300
Output frequency (Hz)	60
Output inductance (mH)	6.3
Output load (Ω)	12.7

Figure 4.37 and 4.38 are the experimental results in steady-state conditions and the reference currents are set to i_o = 15 A and 10 A respectively.

Figure 4.39 shows the performance of the converter and the controller in transient conditions. In Figure 4.39, the step change is applied in reference current from i_o = 15 A to i_o =10 A. As can be seen from Figure 4.39, the output current follows the reference current when the reference current changes.

The performance of the proposed topology is evaluated for transient in fundamental frequency as shown in Figure 4.40, which demonstrates the feasibility of the proposed topology for variable frequency applications such as motor drive applications. As can be seen, the FCs are well balanced during and after the transient while the current's frequency smoothly adjusts itself.

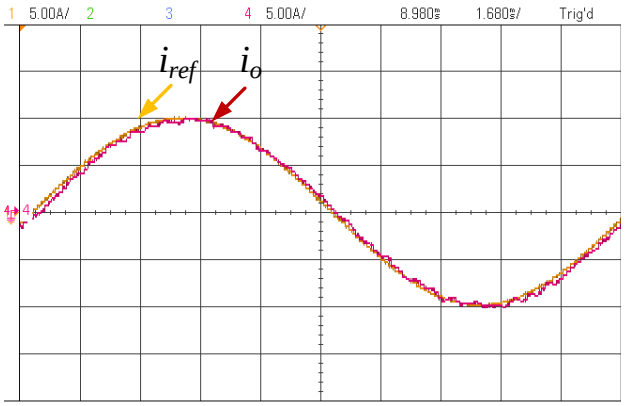
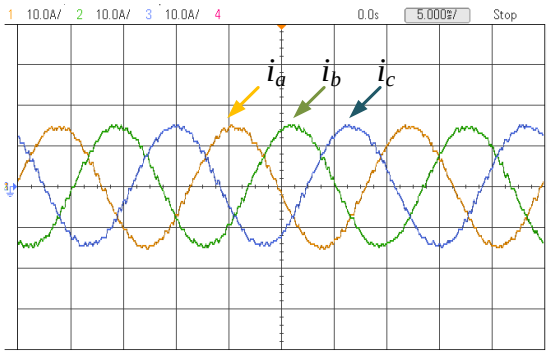
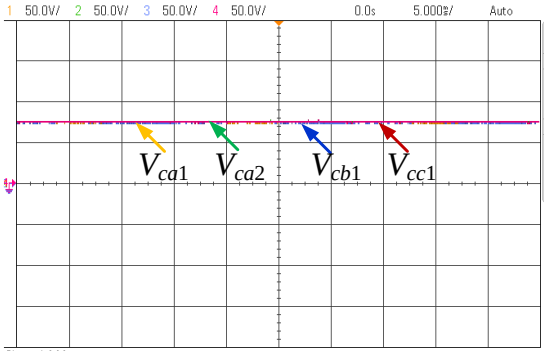


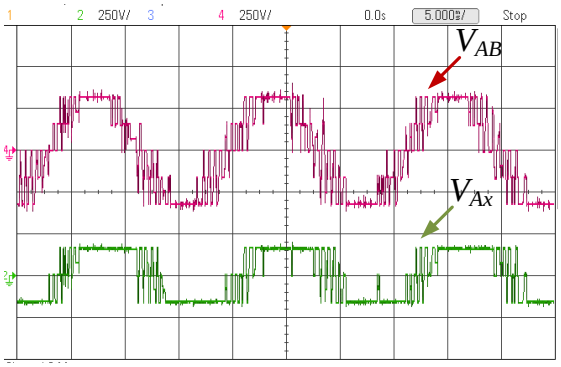
Figure 4.36 Experimental results, output, and reference current



(a) inverter output currents
(10A/div, 5ms/div)

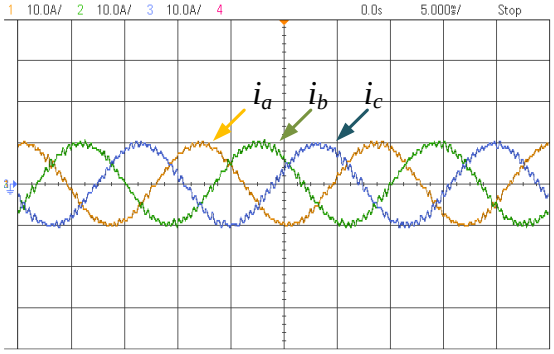


(b) voltage of flying capacitors
(50V/div, 5ms/div)

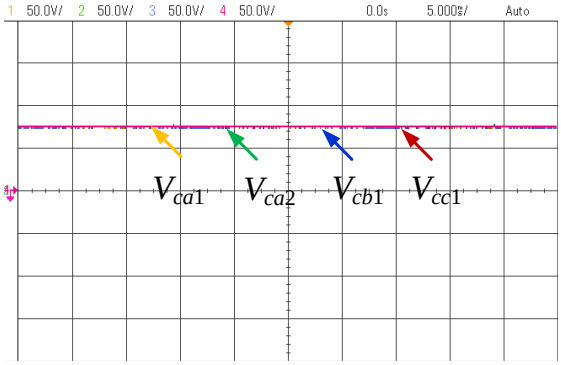


(c) Line and phase voltage
(250V/div, 5ms/div)

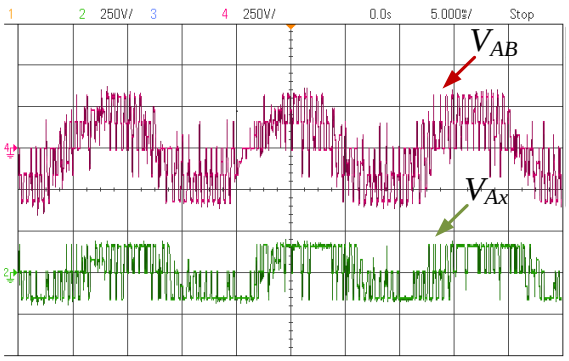
Figure 4.37 Experimental results, i_{oref} = 15 A, f= 60Hz



(a) inverter output currents
(10A/div, 5ms/div)

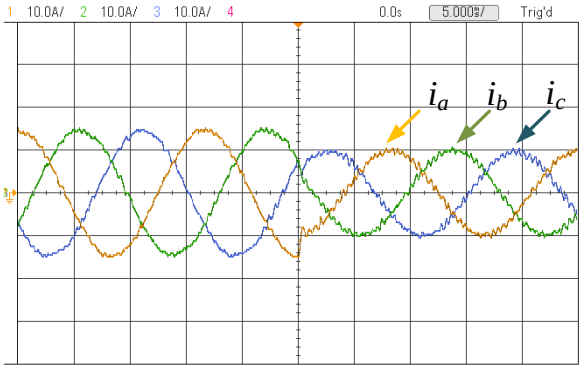


(b) voltage of flying capacitors
(50V/div, 5ms/div)

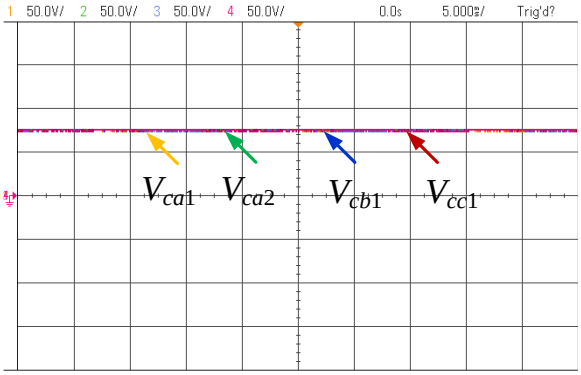


(c) Line and phase voltage
(250V/div, 5ms/div)

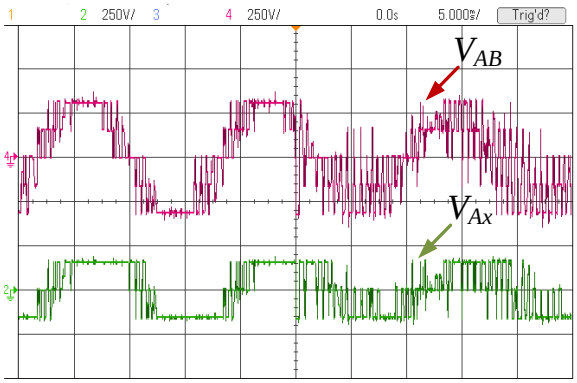
Figure 4.38 Experimental results, i_{oref} = 10 A, f= 60Hz



(a) inverter output currents
(10A/div, 5ms/div)

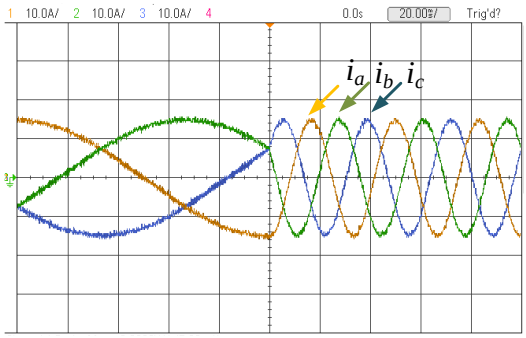


(b) voltage of flying capacitors
(50V/div, 5ms/div)

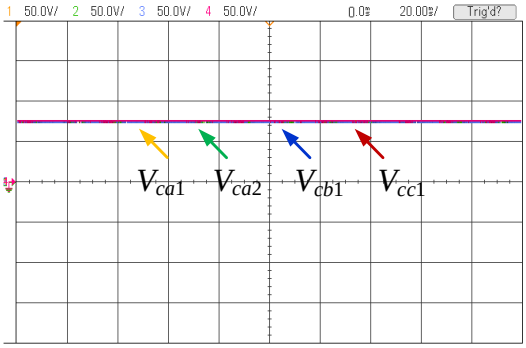


(c) Line and phase voltage
(250V/div, 5ms/div)

Figure 4.39 Experimental results, i_{oref} changes from 15 to 10 A



(a) inverter output currents
(10A/div, 5ms/div)



(b) voltage of flying capacitors
(50V/div, 5ms/div)

Figure 4.40 Experimental results, frequency changes from 5Hz to 30Hz

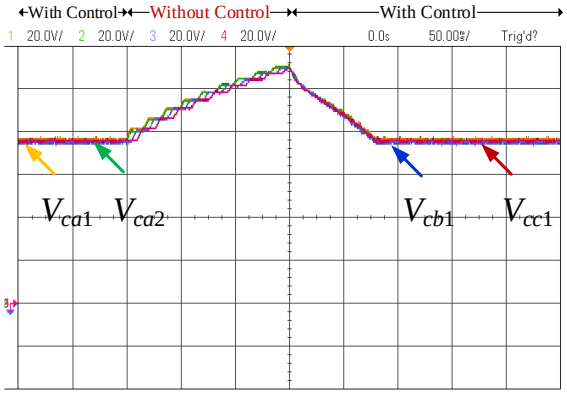


Figure 4.41 Voltage of flying capacitors, the controller is deactivated and activated

In Figure 4.41, the controller is deactivated for a few cycles and then reactivated to show the effectiveness of the controller. Figure 4.39 to Figure 4.41 illustrate that the capacitor voltages are well balanced at their desired values in the transient conditions.

Figure 4.36 to Figure 4.41 demonstrate the feasibility of the proposed power converter and the effectiveness of the proposed controller at different operating conditions.

4.6 Summary

In this chapter, first, a new method to control flying capacitor voltages of a four-level T-type NNPC inverter base on sinusoidal pulse width modulation (SPWM) is proposed. The four-level T-type NNPC topology is very attractive for medium-voltage applications due to the fewer components compared to the existing topologies. The proposed control method selects the best switching state among the redundant switching states to charge and discharge the flying capacitors and minimize the voltage deviations of the capacitors from the desired values. As the proposed controller is based on the SPWM technique, is very simple to implement. The feasibility of the proposed control technique is evaluated by simulation studies and experimentally. The results demonstrate the effectiveness of the proposed technique.

Second, a new 5-level T-NNPC is proposed in this chapter. The proposed 5-level T-NNPC has a fewer number of components in comparison to other classical and advanced 5-level topologies, which makes it a suitable choice for high-power medium-voltage applications among other topologies. A model predictive control strategy is developed to control the capacitors voltages and the output currents at their desired values. To implement the model predictive control, a discrete-time model of the converter is developed in terms of switching states to predict the values of flying capacitor voltages and output currents. A cost function is used to minimize the error between the predicted and reference values.

The operation of the 5-level T-NNPC converter was studied in MATLAB/Simulink at different power factors and different output frequencies. The feasibility of the converter was evaluated experimentally at different operating conditions including steady-state and transient. The simulation and experimental results validate the operation of the proposed converter and the performance of the developed control technique.

The four-level and five-level T-type NNPC are attractive choices for medium-voltage connected ultra-fast charging since the number of components and control complexity of the aforementioned topologies are their advantage in comparison to existing topologies.

These topologies can be used as grid-connected AC/DC converter in medium-voltage (2.4-4 kV) connected ultra-fast charging applications, in the same manner, explained in this chapter with the same controllers. The only difference is grid current control which can be developed by PI controllers as explained in the next chapters.

For higher voltage levels, higher-level topologies must be used due to the limitation of active devices in terms of voltage rating which is the motivation for the next chapter.

Chapter 5

Propose Seven-Level Medium-Voltage Topology and its Controllers

5.1 Introduction

As discussed, multilevel topologies have advantages such as; lower device voltage stress, higher power quality, lower power loss, etc... that make these topologies attractive for medium-voltage applications. A higher number of levels magnifies these advantages while increasing the bill of material, therefore, there is a trade-off between cost and the number of levels. Seven-level topologies such as CHB converter have been used in industry for different applications, which demonstrates the feasibility of these converters in terms of the aforementioned trade-off.

In this chapter, a new seven-level topology is proposed which is superior in terms of the number of devices in comparison to other seven-level topologies such as CHB.

An SVM-based controller is developed for the proposed topology to control the voltages of the flying capacitors to ensure proper and safe operation of the proposed topology.

Due to the limitation of the SVM-based controller in balancing the flying capacitor voltages in a wide range of operating conditions. A controller based on MPC is also developed for the proposed topology to control the voltage of the flying capacitor in a wide range of operating conditions.

MPC-based controller requires a significant computational power to control the flying capacitors of the proposed topology, therefore, a computational efficient MPC is proposed which significantly reduces the required computational burden to control the flying capacitor voltages.

Since the operation of the proposed topology as the AC/DC stage of an MV connected ultra-fast charging station is investigated in the next chapter, this chapter dedicates to evaluating the performance of the proposed topology as the DC/AC stage for industrial motor derives which validates the feasibility of the proposed topology for various applications.

5.2 A New Seven-Level Topology for Medium-Voltage Application

In this section, a new seven-level voltage source converter (VSC) topology, shown in Figure 5.1, is proposed for medium-voltage (MV) applications. The proposed converter has a fewer number of components in the circuit compared to the existing advanced 7-level topologies. The space vector modulation (SVM) technique is developed for the proposed topology to balance the flying capacitors voltage. The performance of the proposed converter is evaluated at both steady-state and transient conditions in MATLAB/Simulink. A scaled-down prototype is also built to verify the feasibility and performance of the proposed converter at different operating conditions.

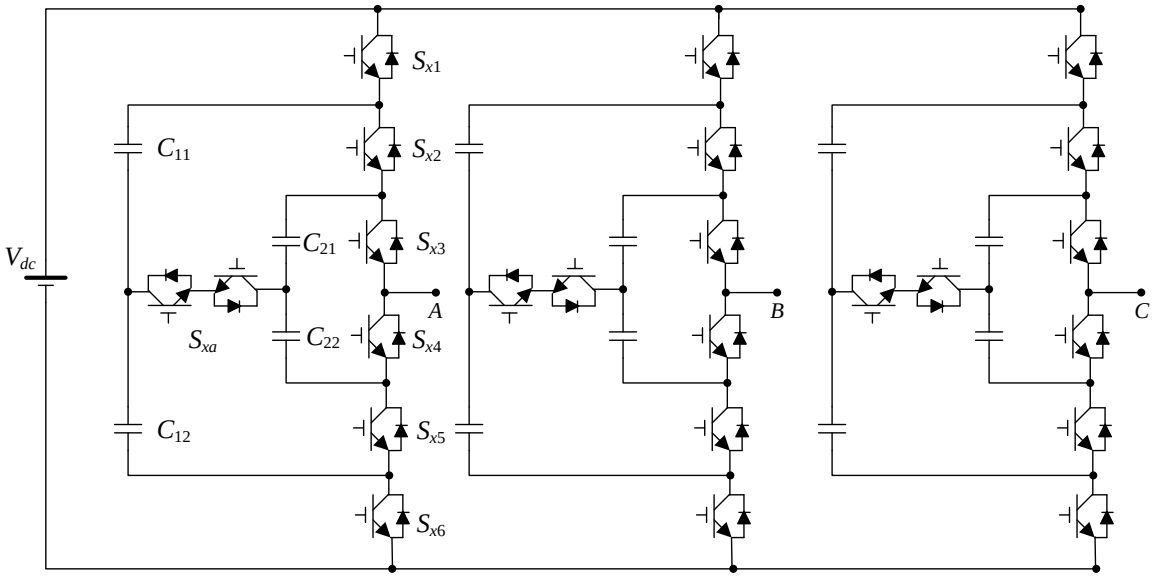


Figure 5.1 Proposed new seven-level topology

5.2.1 Converter operation

The topology of the proposed converter is shown in Figure 5.1. As can be seen, each phase consists of six switches, four flying capacitors, and one bi-directional switch. The flying capacitors C_{x11}, C_{x12} are charged to $V_{dc}/3$ and C_{x21}, C_{x22} are charged to $V_{dc}/6$ where x = phase a, b, c. It can be found that these pairs of switches: (S_{x1}, S_{x6}), (S_{x2}, S_{x5}), and (S_{x3}, S_{x4}) are complementary and cannot be turned on at the same time. Also, switches S_{x2}, S_{x4}, and S_{xa} cannot be turned on at the same time. Otherwise, the flying capacitors are short-circuited. The proposed converter has twelve switching states, which are listed in Table 5.1.

TABLE 5.1 THE SWITCHING STATES OF THE PROPOSED CONVERTER

Sx_1	Sx_2	Sx_3	Sx_4	Sx_5	Sx_6	Sx_a	V_{cx11}		V_{cx12}		V_{cx21}		V_{cx22}		V_{ax}	Output Level
							$i_x>0$	$i_x<0$	$i_x>0$	$i_x<0$	$i_x>0$	$i_x<0$	$i_x>0$	$i_x<0$		
1	1	1	0	0	0	0	-	-	-	-	-	-	-		$\frac{V_{dc}}{2}$	6
1	0	1	0	0	0	1	C	D	-	-	D	C	-	-	$\frac{V_{dc}}{3}$	5
1	1	0	1	0	0	0	-	-	-	-	C	D	C	D	$\frac{V_{dc}}{6}$	4
1	0	1	0	1	0	0	C	D	C	D	D	C	D	C		
0	1	1	0	0	1	0	D	C	D	C	-	-	-	-		
1	0	0	1	0	0	1	C	D	-	-	-	-	C	D	0	3
0	0	1	0	0	1	1	-	-	D	C	D	C	-	-		
1	0	0	1	1	0	0	C	D	C	D	-	-	-	-	$-\frac{V_{dc}}{6}$	2
0	1	0	1	0	1	0	D	C	D	C	C	D	C	D		
0	0	1	0	1	1	0	-	-	-	-	D	C	D	C		
0	0	0	1	0	1	1	-	-	D	C	-	-	C	D	$-\frac{V_{dc}}{3}$	1
0	0	0	1	1	1	0	-	-	-	-	-	-	-	-	$-\frac{V_{dc}}{2}$	0

These twelve switching states generate seven different output voltages with equally spaced step $V_{dc}/6$. By applying these switching states to switches, the converter is capable of outputting seven different phase voltages. As can be seen from Table 5.1, each switching state has a distinct impact on the voltage of the flying capacitors. Without controlling the flying capacitors voltage, the capacitors might be fully charged to V_{dc} or discharged to reach zero. The uncontrolled charging/discharging results in losing output levels, increasing total harmonic distortion (THD), and affecting the voltage stress of the switches, which may result in damaging the switches. To solve this problem, a space vector modulation (SVM) technique is developed to regulate the flying capacitors voltage and converter output.

5.2.2 Advantages and challenges

The proposed seven-level topology benefits from combining the feature of flying capacitor (FC) topology and a neutral point piloted (NPP) topology to increase the number of output voltage levels. This topology has the following features:

1) All power switches have the same voltage rating.
2) The proposed topology has a fewer total number of components compared to the conventional and recently proposed converters. The comparison is shown in Table 5.2.

TABLE 5.2 NUMBER OF DEVICES IN SEVEN-LEVEL TOPOLOGIES

Topology	**Switches**	**Floating Capacitors**	**Blocking Voltage (1 pu= V_{dc}/6)**	**Switches with equal Blocking Voltage**	**Isolated DC Sources**
7L-FC [44]	36	45	1	36	1
7L-CHB [44]	36	-	1	36	9
7L-MMC [90]	72	36	1	72	1
7L-ANPC [91]	30	9	1 and 3	54	1
7L-Converter (2010) [92]	36	18	1 and 2	54	1
Modified 7L-NPC (2012) [46]	36	6	1 and 2	54	1
Modified 7L-ANPC (2015)[93]	30	9	1 and 3	54	1
7L-HB-NPC (2016) [94]	24	-	2 and 6	96	3
A Novel 7L-ANPC (2018) [95]	45	27	1 and 3	54	1
A New 7L-HC(2018) [96]	30	9	1 and 2	60	1
Proposed 7LTopology	21	18	2	42	1

For some of the topologies, the voltage rating of the switches is not the same. To fairly compare the number of components in the converters, the blocking voltage of each device is considered $V_{dc}/6$ and then the total number of switches with the same blocking voltage ($V_{dc}/6$) are calculated and listed in Table 5.2. As can be seen from Table 5.2, the proposed topology has a fewer total number of switches even under the same blocking voltage.

Although the proposed topology has the previous advantages, the main challenge is the low-frequency operation (<20Hz), where the voltage ripple of the flying capacitors must be kept below 10%. The proper operation of the topology at low-frequency requires either increase in the capacitance value or the switching frequency, and thus keeps the flying capacitor voltages balanced with low voltage ripples (<10%). Therefore, the proposed topology is more suitable for fixed

frequency applications such as grid-tied applications like MV-connected fast-charging stations, FACTS devices, and renewable energy integration.

Another challenge is the complexity of the calculations that need to be done by the micro-controller. To balance the flying capacitors, the micro-controller needs to enumerate all possible combinations of switching estates and determine the best value in a very short period of time. This computational burden affects the controller performance when the controller is also responsible to control other parameters than only flying capacitor voltages.

To balance the flying capacitors voltages, space vector modulation (SVM) is developed. The SVM takes advantage of the redundant switching states to control the voltage on flying capacitors based on a minimum-energy cost function.

5.2.3 SVM for the proposed seven-level converter

The space vector modulation (SVM) is a classical control method of power converter realized by tracing a rotating reference vector at α-β plane. The reference vector at α-β plane can be calculated by Clarke's transformation as shown in (5.1) [97].

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ 0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{5.1}$$

where;

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} V_p \sin(wt) \\ V_p \sin(wt - \frac{2}{3}\pi) \\ V_p \sin(wt - \frac{4}{3}\pi) \end{bmatrix} \tag{5.2}$$

v_a, v_b, and v_c are three-phase reference voltages and v_a and v_β are the x and y projection of $\overrightarrow{V_{ref}}$ on the α-β plane. Vp is the peak value of the reference phase voltages and ω is the angular velocity of the reference voltage. Substituting v_a, v_b, and v_c into (5.1), the reference vector $\overrightarrow{V_{ref}}$ can be found as a circle around the center of the α-β plane, defined as (5.3) [19]–[22].

$$\begin{aligned} \overrightarrow{V_{ref}} &= |\overrightarrow{V_{ref}}| e^{j\theta} \quad , \qquad \theta = \omega \times t \\ |\overrightarrow{V_{ref}}| &= \sqrt{{v_\alpha}^2 + {v_\beta}^2} \end{aligned} \tag{5.3}$$

The proposed converter generates seven different output voltages for each phase, which provides 73 combinations of switching states for a three-phase converter. Substituting these switching states into (5.1), the corresponding switching vector can be calculated. The space vector diagram of a seven-level converter is a hexagon on the a-β plane centered at the origin of the plane, as shown in Figure 5.2. As the seven-level hexagon has a highly complex geometry, only Sector I is showed in Figure 5.2. The numbers in the hexagon denote the output level of each phase by numbers 0 to 6.

Assuming the reference vector is located in Sector I, as can be seen from Figure 5.2, three adjacent switching vectors $\overrightarrow{V_1}$, $\overrightarrow{V_2}$ and $\overrightarrow{V_3}$ synthesize the reference vector. The volt-second balancing equation is:

$$\overrightarrow{V_1}t_1 + \overrightarrow{V_2}t_2 + \overrightarrow{V_3}t_3 = \overrightarrow{V_{ref}}\,T_s$$
$$t_1 + t_2 + t_3 = T_s \tag{5.4}$$

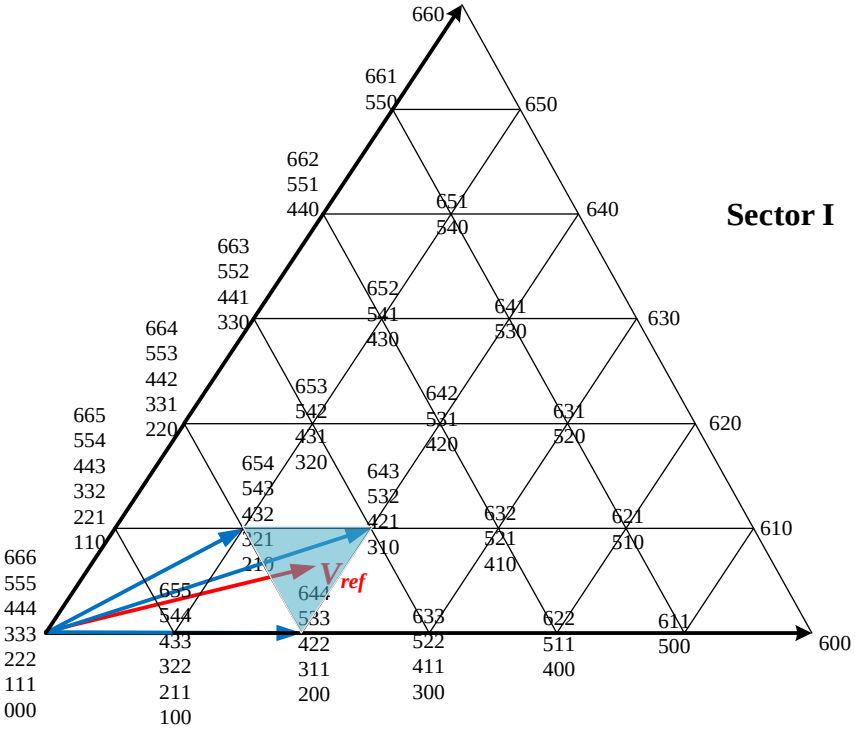


Figure 5.2 Space vector diagram of a seven-level converter

where T_s is sampling period and t_1, t_2 and t_3 are the dwell time of the three switching vectors. As the reference vector rotating around the center, it is sampled at each switching period and the dwell time of three adjacent switching vectors is calculated depending on the sampling vector. At each switching period, the

controller applies these three switching vectors to the converter for the determined dwell time and thus produces the output voltage [70], [98], [99].

As can be noticed from Figure 5.2, there are more than one switching vector that produce the same line-to-line voltage (except for the large vectors in the hexagon). Also, Table 5.2 shows that levels 2, 3, and 4 have redundant switching states that produce the same voltage level. When the reference vector is located in a triangle, there are multiple combinations of line-to-line switching vectors.

Moreover, for a given level in each phase, there are multiple redundant switching states. Each of these redundant switching states provides a different impact on the flying capacitors voltage.

In order to select the best switching state among the possible switching states to balance the voltage of the flying capacitors, a cost function J is introduced. The cost function is defined to minimizes the deviation of the flying capacitors voltage from their nominal values which is $V_{dc}/3$ for C_{x11}, $C_{x12,}$ and $V_{dc}/6$ for C_{x21}, C_{x22}. The cost function can be defined as:

$$\begin{aligned} \mathrm{J} = J_a + J_b + J_c &= \sum_{x} \sum_{i=1}^{4} \frac{1}{2} C_{xi} (\Delta V_{cxi})^2 \\ \Delta V_{cxi} &= \sum_{i=1}^{2} \left(V_{cxi} - \frac{V_{dc}}{3} \right) + \sum_{i=3}^{4} \left(V_{cxi} - \frac{V_{dc}}{6} \right) \\ & \qquad x = a, b, c \end{aligned} \tag{5.5}$$

The cost function J is equivalent to a deviation of energy stored in the flying capacitors from their nominal values. J_a, J_b and J_c is the corresponding energy deviation of phases *a, b* and *c*. C_{xi} and V_{cxi} is the capacitance and measured voltage of the flying capacitors. To minimize the cost function J, the following condition needs to be satisfied:

$$\begin{aligned}\frac{dJ_x}{dt} &= \sum_{i=1}^{2} C_{xi}\left(V_{cxi} - \frac{V_{dc}}{3}\right)\frac{dV_{cxi}}{dt} + \sum_{i=3}^{4} C_{xi}\left(V_{cxi} - \frac{V_{dc}}{6}\right)\frac{dV_{cxi}}{dt} \\ &= \sum_{i=1}^{2}\left(V_{cxi} - \frac{V_{dc}}{3}\right) i_{cxi} + \sum_{i=3}^{4}\left(V_{cxi} - \frac{V_{dc}}{6}\right) i_{cxi} \le 0, \\ &\qquad x = a, b, c\end{aligned} \tag{5.6}$$

where i_{cxi} is the current of the corresponding capacitor C_{xi}. The average current for each capacitor in each sampling time is calculated based on the output line current, and charging or discharging effect of each switching state. 0, 1, -1 is assigned to each switching state base on the effect of charge (1), discharge (-1), no impact (0) on the capacitor's voltages, so $\bar{\imath}_{C\,cxi}$ is calculated as the equation in follow;

$$\begin{aligned}\tilde{i}_{C_{cxi}} &= \frac{t_1 \times \mathrm{sgn}\, xi(S_1) + t_2 \times \mathrm{sgn}\, xi(S_2) + t_3 \times \mathrm{sgn}\, xi(S_3)}{T_s} \times I_x \\ x &= a, b, c \\ i &= 1, 2, 3, 4\end{aligned} \tag{5.7}$$

where; *sgnxi* (S) is a function that outputs {1,0-1} based on the effect of each switching state on each capacitor voltage. S_1, S_2, S_3 are the switching states

corresponding to the three switching vectors adjacent. I_x is the output line current for phases a, b, and c.

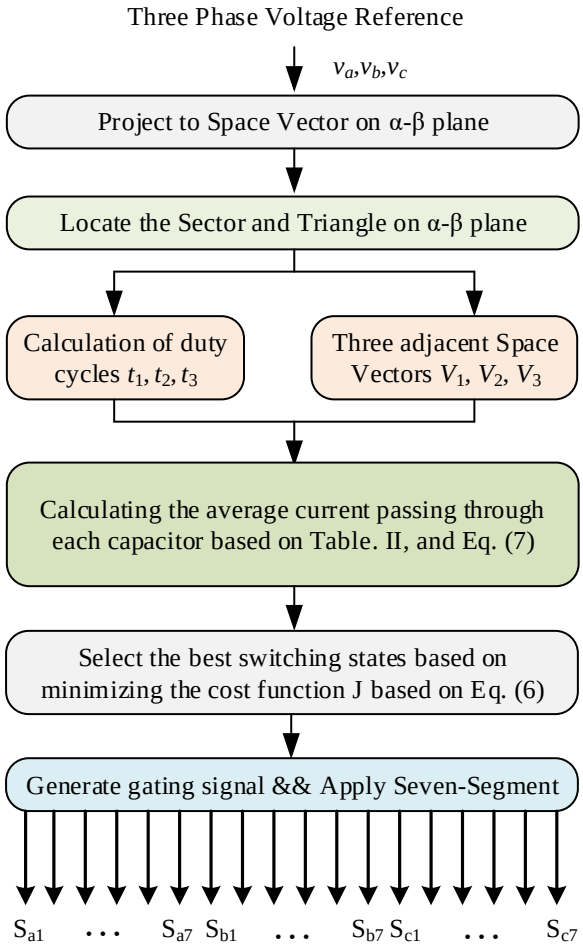


Figure 5.3 Block diagram of the developed control method

At the start of each sampling period, the voltage of the flying capacitors and the current of each phase is sampled. At each sampling period, the controller considers the measured voltage of the flying capacitors and output currents are constant values because their values do not change much at a short period of sampling time.

The best switching state that minimizes the cost function J and satisfies (5.5) will be selected and then applied to the converter. The block diagram of the developed control method is shown in Figure 5.3.

5.2.4 Simulation Studies

To investigate the performance of the proposed topology and the developed control technique, a simulation study has been done in MATLAB/Simulink. The system parameters are shown in Table 5.3. The simulation results are given under different steady-state and transient conditions and at different modulation indices and load power factors.

TABLE 5.3 SIMULATION PARAMETERS

Converter Parameters	Values	Values (p.u)
Power rating	1 MVA	1
Output Voltage (Line-to-Line)	7.2KV	1
Flying Capacitors	1200µF	0.05
Input DC Voltage	10.2KV	-
Output Frequency	60Hz	1
Sampling Frequency	2400 Hz	
Load Impedance	27.2 Ω	

A. Steady-State Studies

Figure 5.4 shows the simulation results with modulation index m is 0.90, and the load PF is 0.95. The output voltage has thirteen levels, and the capacitor voltages are well balanced at their nominal values that are 3400V and 1700V. The THD of

the voltage waveform is 12.86%, and the output current 1.73%. The voltage ripple on the FCs is 4.2 %.

Figure 5.5 shows the simulation results where the modulation index is 0.7, and the load PF is 0.7. The result of steady-state simulation shows that the proposed topology can operate in different load power factors and modulation indices while the flying capacitors voltage are regulated at their nominal values. The THD of the voltage waveform is 16.36%, and the output current 1.27%. The voltage ripple on the FCs is 4.4%

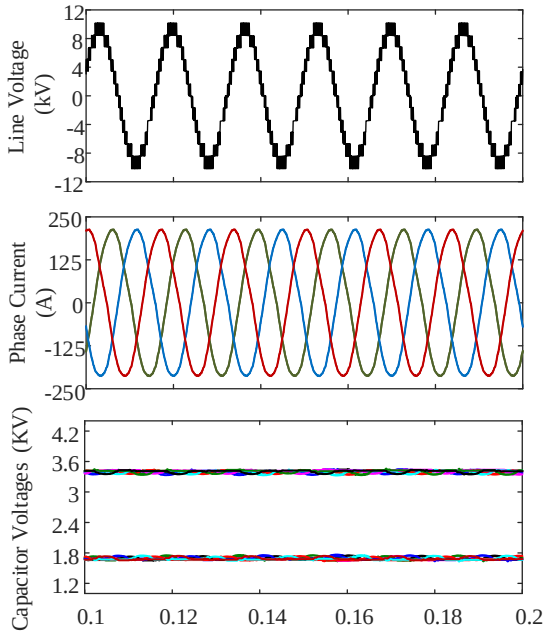


Figure 5.4 Steady-state simulation with m = 0.90, PF = 0.95

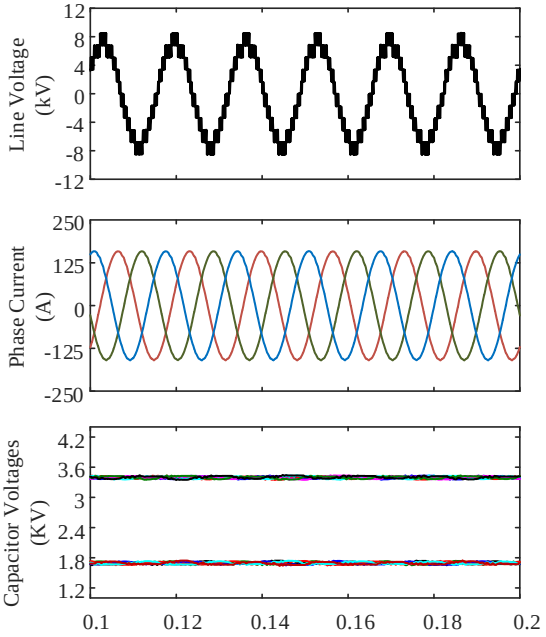


Figure 5.5 Steady-state simulation with m = 0.7, PF=0.7

B. Transient Studies

In the transient studies, the load changing and modulation index changing are studied where *PF* is 0.8. Figure 5.6 shows the results when the load changes from half-load to full-load at $t = 0.15$ sec. As can be seen from Figure 5.6, the capacitors are balanced during the load changes. Figure 5.7 shows the output voltage, output currents, and flying capacitors voltage where the modulation index changes from $m = 0.95$ to $m = 0.6$ at $t = 0.15$ sec.

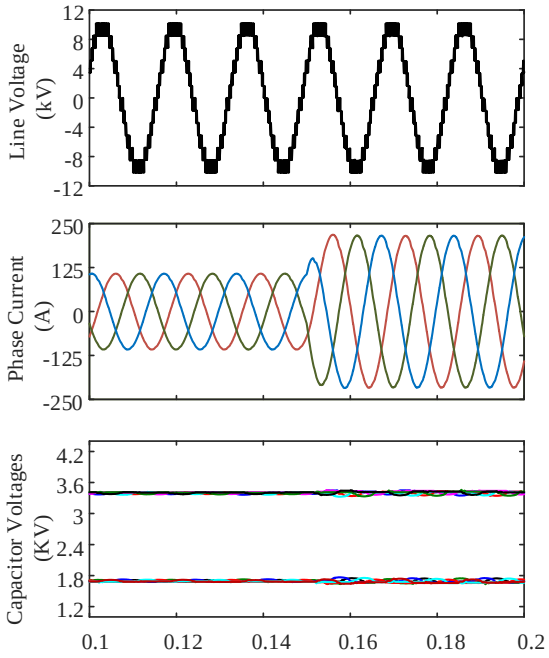


Figure 5.6 Transient studies: load changes from half-load to full- load with m=0.95, PF = 0.8

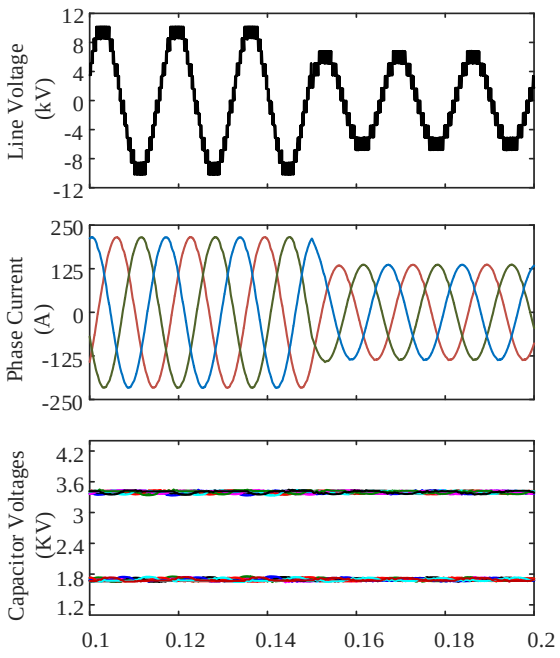


Figure 5.7 . Transient studies: modulation index changes from m=0.95 to m=0.6 with PF = 0.8

It can be seen from Figure 5.7 that when the modulation index changes from 0.95 to 0.6, the number of levels will change from thirteen to nine and the voltage

of the capacitors remains stable during the transient. The THD of the voltage waveform changes from 12.22% to 19.41%, while the output current THD changes from 1.28% to 1.65%.

C. Low-frequency Operation

In this section, the low-frequency operation of the proposed topology is investigated. In Figure 5.8 the flying capacitors voltages in different frequency ranges are shown. As can be seen, the fundamental frequency is decreased from 60 Hz to 20 Hz and all the capacitors are well-regulated at different frequencies. It can be seen that as the fundamental frequency decreases the FCs voltage ripple increases. For low-frequency applications, to have lower ripple, there are two solutions; first, increasing the capacitance of the FCs, and the second one is to increase the switching frequency. Since increasing the switching frequency in high power applications increases the switching losses, increasing the capacitance of the FCs is preferred.

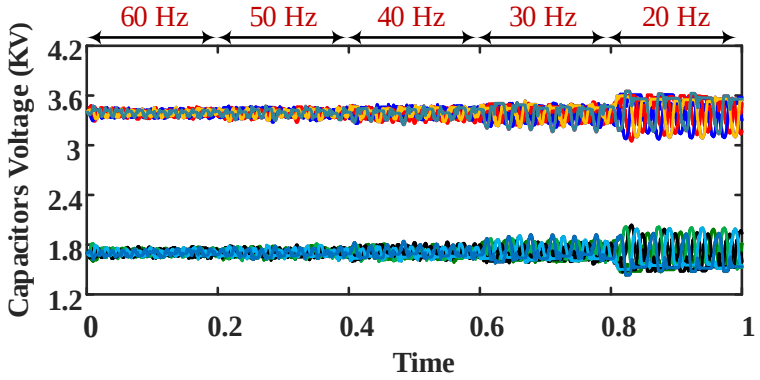


Figure 5.8 Flying capacitors voltages where fundamental frequency is decreased from 60 Hz to 20 Hz

D. Controller Evaluation

To evaluate the performance of the controller, the converter operates in a steady-state, and the controller deactivated at t=0.08sec and then reactivated at t=0.17sec. Figure 5.9 shows the flying capacitors voltage where the modulation index $m = 0.95$ and PF $= 0.8$. When the controller is deactivated, the voltage of the capacitor deviates from the nominal values. When the controller is reactivated, the flying capacitor voltages start converging to nominal values.

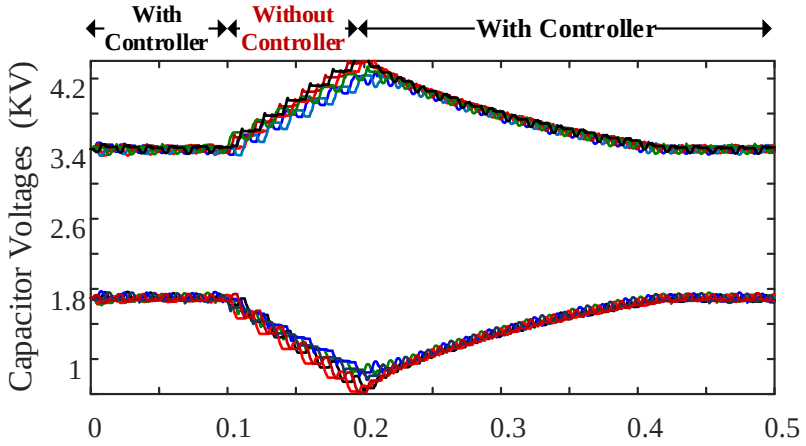


Figure 5.9 Controller evaluation where m=0.95, PF $= 0.8$; Voltage of flying capacitors

E. Stress of the Active Switches

In this section, the stress on the active switches is investigated in terms of conduction, and switching losses. In Table 5.4, the RMS current of each switch is shown for different operating conditions, and in Table 5.5, the average frequency of each switch is shown for the same operating conditions. As can be seen from

Table 5.4 and Table 5.5, for S_2, S_5, and S_7, the conduction losses are a bit lower than other switches while the average switching frequency is higher. Therefore, in terms of power losses, almost all the active switches will have the same stress.

TABLE 5.4 RMS CURRENT OF EACH SWITCH (WHERE 1PU =10 A)

Condition	I_{S1}	I_{S2}	I_{S3}	I_{S4}	I_{S5}	I_{S6}	I_{S7}
m=0.95, PF=0.95,	0.71	0.64	0.72	0.71	0.64	0.72	0.46
m=0.9, PF=0.8,	0.65	0.56	0.64	0.65	0.57	0.64	0.56
m=0.9, PF=0.5,	0.66	0.54	0.66	0.64	0.56	0.63	0.54
m=0.7, PF=0.8,	0.50	0.43	0.51	0.50	0.44	0.52	0.43

TABLE 5.5 AVERAGE SWITCHING FREQUENCY OF EACH SWITCH (WHERE 1PU = 2400 HZ)

Condition	f_{S1}	f_{S2}	f_{S3}	f_{S4}	f_{S5}	f_{S6}	f_{S7}
m=0.95, PF=0.95,	0.18	0.62	0.17	0.17	0.64	0.18	0.63
m=0.9, PF=0.8,	0.47	0.72	0.52	0.52	0.72	0.47	0.56
m=0.9, PF=0.5,	0.48	0.87	0.49	0.49	0.87	0.48	0.54
m=0.7, PF=0.8,	0.53	0.87	0.53	0.53	0.87	0.53	0.43

F. Flying Capacitor Selection

Since the voltage ripple of the flying capacitors has a direct effect on the output power quality of the converter, the selection of flying capacitors is very important.

Moreover, high voltage ripple can increase the stress on the active switches. The capacitance can be selected based on the following [100];

$$C = \frac{I_p}{f_{sw}\Delta V_c} \tag{5.8}$$

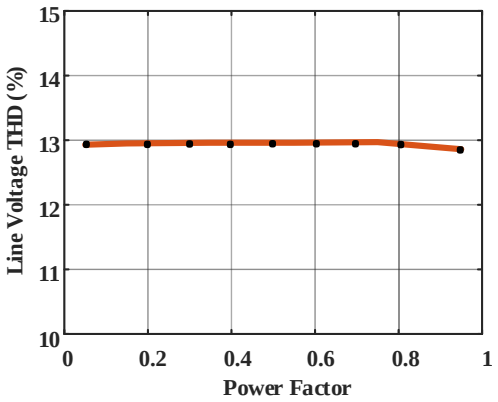
where; C is the flying capacitors capacitance, I_p is the phase peak current, f_{sw} is the switching frequency, and ΔV_c is the allowable peak to peak ripple voltage. With the parameters given in Table 5.3, and maximum acceptable voltage ripple of 10%, which is a practical standard, the capacitance for flying capacitors is calculated as 1200 µF

G. Flying Capacitor Voltage Ripple, and Line Voltage THD

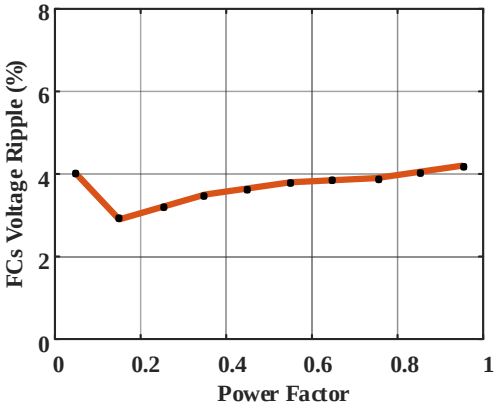
In this section, the FCs voltage ripple and line voltage THD are analyzed in different power factors and modulation indexes. The results where the modulation index is constant and power factor changes from 0.95 to 0.05 are shown in Figure 5.10. It can be seen from Figure 5.10 (a) that line voltage THD remains almost constant, while in Figure 5.10 (b) the FCs voltage ripple is decreasing as the power factor decreases which shows more control on the FCs voltages in lower power factor.

The results where the power factor is constant (PF= 0.9), and the modulation index decreases from 0.99 to 0.1 is shown in Figure 5.11. As can be seen in Figure

5.11 (a), the line voltage THD increases as the modulation index decreases, which is due to the lower number of levels in lower modulation indexes. In the modulation index equal to 0.99, line voltage has 13 steps and the THD is equal to 11.4% while when the modulation index is 0.1, line voltage has 5 levels and the THD is equal to 120%.

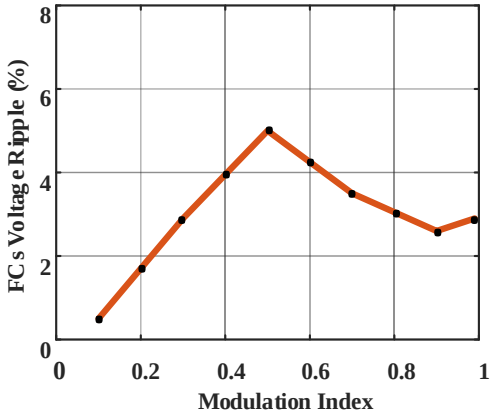


(a) Ripple vs PF

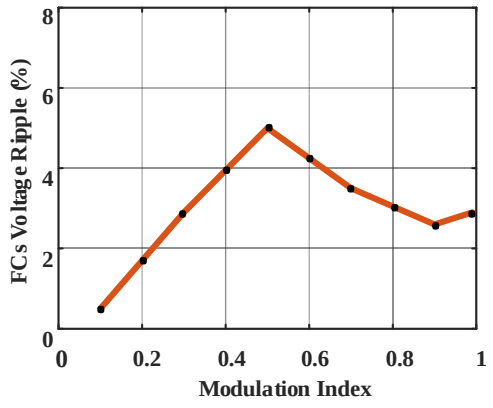


(b) THD vs PF

Figure 5.10 Line Voltage THD and FCs voltage ripple versus power factor



(a) Voltage Ripple vs m



(b) THD vs m

Figure 5.11 Line voltage THD and FCs voltage ripple

Moreover, it can be seen from Figure 5.10 (b), and Figure 5.11 (b) that the flying capacitors voltage ripple is kept below 5% for different modulation indices and power factors where the fundamental frequency is 60 Hz.

5.2.5 Experimental Results

The feasibility of the proposed converter with the developed SVM scheme is evaluated experimentally. The experimental setup for the proposed 7-level converter is shown in Figure 5.12.

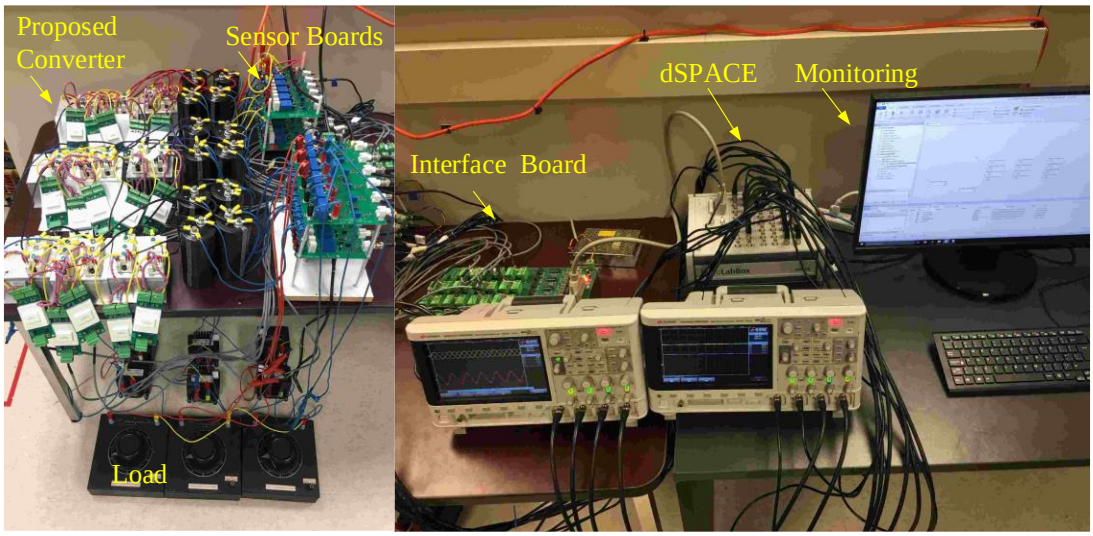


Figure 5.12 Experimental setup for the proposed 7-level converter

The controller was programmed inside Microlab Box, dSPACE-ds1202. The flying capacitor voltages and output currents were measured by LV 25-P and LEM LA 100-P transducers, respectively. The power switches were IGBT SKM50GB12V, and the gate drivers were SKHI22B. A signal conditioner board was designed to

interface and isolate the output of dSPACE and gate drivers. The parameters shown in Table 5.6 are the configuration of the scaled-down prototype.

TABLE 5.6 SCALE-DOWN EXPERIMENTAL PARAMETERS

Converter Parameters	Values
Power rating	2KVA
Flying Capacitors	2000μF
Input DC Voltage	400V
Output Frequency	60Hz
Output Inductance	6mH
Output Load	10Ω
Sampling Frequency	2400 Hz

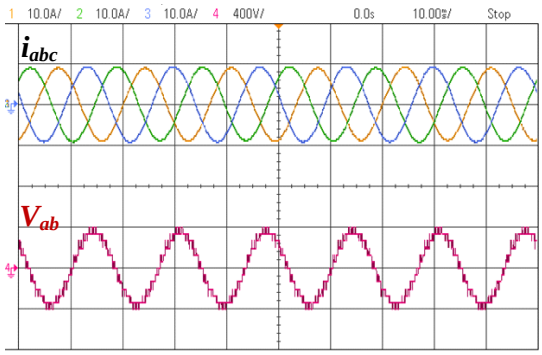
A. Steady-State Operation

Figure 5.13 to Figure 5.16 show the performance of the proposed 7-level converter under steady-state conditions. Figure 5.13 shows the output voltage, output currents, and flying capacitor voltages where the modulation index is 0.9 and the power factor is 0.6. The output voltage is thirteen levels, and the capacitors are well balance around their nominal values which are 133V and 66V.

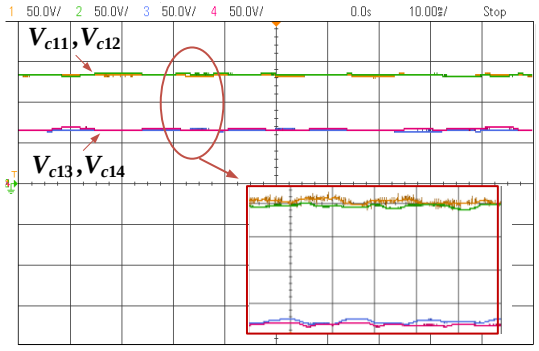
Figure 5.14 shows the operation of the proposed converter where the power factor index is increased to 0.95. It is known that regulating the FCs voltages of multilevel converters in high power factor is more challenging and is a critical operating point. As can be seen, the capacitors are well balanced which demonstrates the

effectiveness of the controller in regulating the FCs voltages in high power factor load conditions.

Figure 5.15 shows the operation of the proposed converter where the modulation index is reduced to 0.6 and the power factor is 0.6. As can be seen, the number of levels of the line voltage is reduced to 9 due to a reduction in the modulation index. The experiment verifies the converter and controller's proper operation in lower power factor and modulation indices.

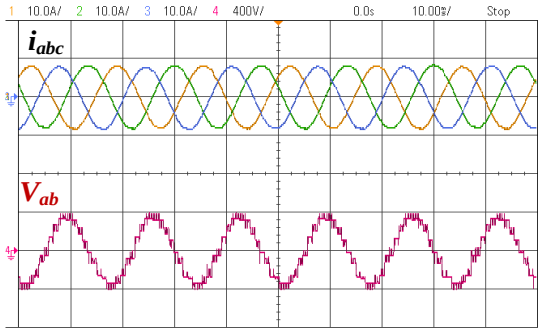


(a) Output voltage

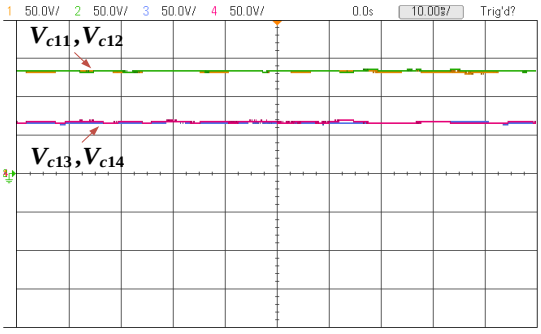


(b) Voltage of flying capacitors

Figure 5.13 Steady-State experiment, where $m = 0.9$ and PF $= 0.6$

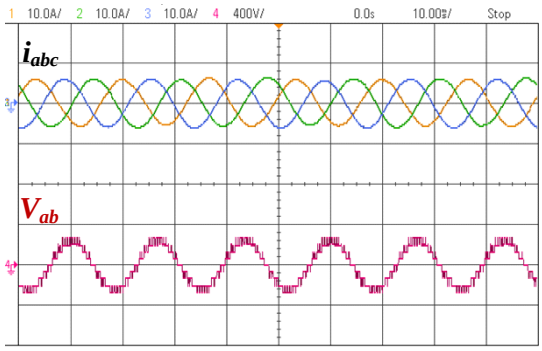


(a) Output voltage
(400V/div, 10A/div, 10ms/div)

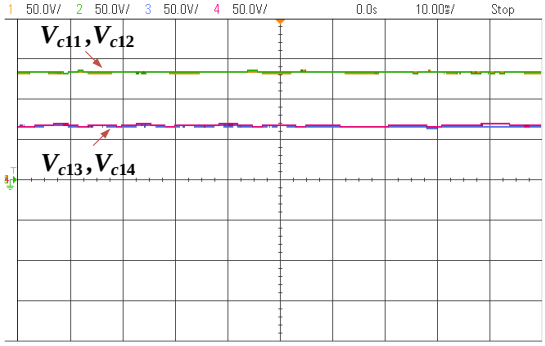


(b) Voltage of flying capacitors
(50V/div, 10ms/div)

Figure 5.14 Steady-State experiment, where $m = 0.9$ and PF $= 0.95$



(a) Output voltage
(400V/div, 10A/div, 10ms/div)



(b) Voltage of flying capacitors
(50V/div, 10ms/div)

Figure 5.15 Steady-State experiment where m = 0.6 and PF = 0.6

Figure 5.16 shows the result with the modulation index is 0.9 and the power factor is 0.75. As mentioned earlier, the power factor has a direct effect on the converter and controller's ability to maintain the FCs voltages regulated.

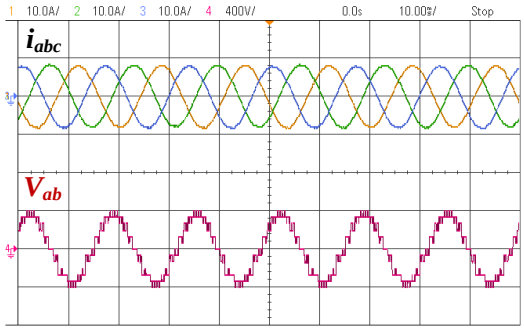
As can be seen from Figure 5.13 to Figure 5.16, the output currents are balanced, and the flying capacitors voltages are regulated around their nominal values at different load power factors and modulation indices.

B. Transient Operation

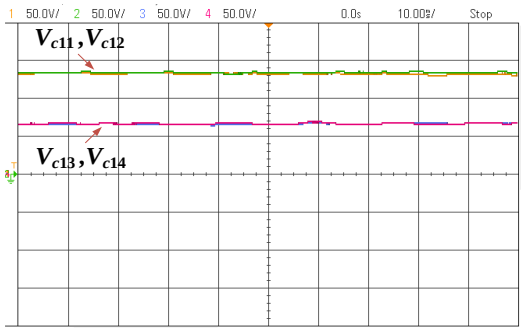
The performance of the proposed converter is verified under transient conditions. Figure 5.17 shows the output voltage, output currents, and flying capacitor voltages where PF is 0.75 and the modulation index, m, changes from 0.6 to 0.9. The results show that the flying capacitors voltages are well-regulated during the transition.

C. Controller Evaluation

Figure 5.18 shows that the voltage of the flying capacitors are deviating from their nominal values when the controller is deactivated, and when the SVM controller is reactivated, the voltage of the capacitors starts converging to their nominal values. This result shows the effectiveness of the controller to regulate the flying capacitors voltage. The performance obtained in experimental studies is in close relationship with the simulation studies at all operating conditions.

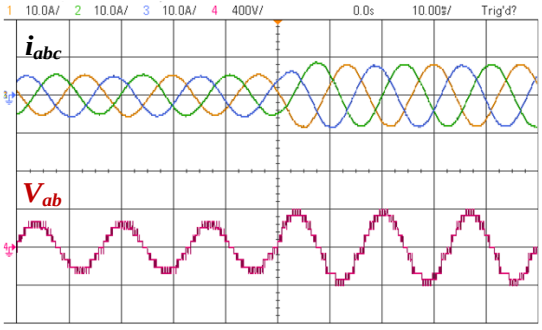


(a) Output voltage
(400V/div, 10A/div, 10ms/div)

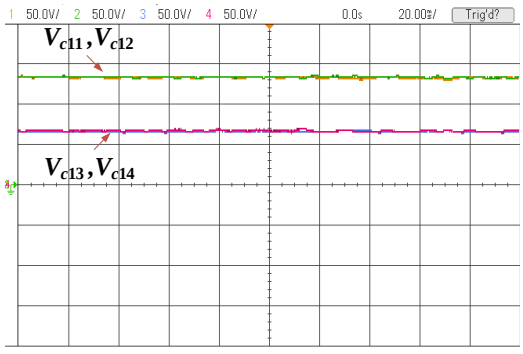


(b) Voltage of flying capacitors
(50V/div, 10ms/div)

Figure 5.16 Steady-State experiment where $m = 0.9$ and PF $= 0.75$



(a) Output voltage
(400V/div, 10A/div, 10ms/div)



(b) Voltage of flying capacitors
(50V/div, 10ms/div)

Figure 5.17 Transient experiment, m changes from 0.6 to 0.9, PF $= 0.75$

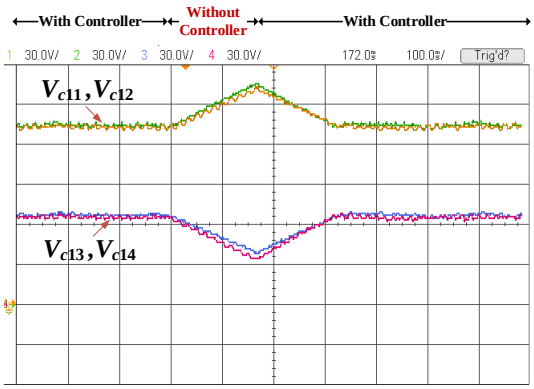


Figure 5.18 Controller evaluation, with and without controller

5.3 Current Control of the Proposed Seven-Level Topology

Due to the low number of redundant switching states in this topology, controllers based on SPWM and SVM schemes are not able to regulate the FCs voltages' in low frequency and high power factors. In SPWM, the redundant switching states of each level, are used to balance the FCs voltages, however, in this topology redundant switching states are available only for mid-levels. In addition, in the SVM modulation scheme, the available switching states for regulating the FCs voltages are limited to the adjacent vectors, and cannot guarantee FCs voltages balancing in all operating conditions.

Similar to the discussion in Section 4.5.2, SVM cannot guarantee capacitors voltage balancing at high power factors or low-frequency operation, which is critical for grid-tied applications such as EV ultra-fast charging stations and applications

such as low-speed industrial motor drives. On the other hand, SPWM faces similar challenges.

Therefore, in this section, a universal controller based on MPC is developed that is able to overcome the challenges regarding flying capacitor voltage control in all operating conditions and is applicable to the proposed seven-level topology in different applications.

Here, the performance of the developed controller is evaluated for motor drive applications, while the next chapter is dedicated to the application of the proposed seven-level topology and the developed controller in ultra-fast charging applications.

In the next sections, first, the mathematical model of the converter is obtained and the structure of MPC for the proposed topology is developed, then the performance of the developed controller is investigated by simulation studies in MATLAB/Simulink environment. Finally, the feasibility of the developed controller is demonstrated by experimental results obtained from a scaled-down prototype.

5.3.1 Model Predictive Control of the Proposed Seven-Level Topology

Due to the development of fast microprocessors, model predictive control has gained considerable attention in power electronics recently. Easy digital implementation, nonlinearity inclusion, fast dynamic response, simultaneous satisfaction of multi-control objectives without PID controllers, and PWM blocks, are the advantages of MPC which caused its' emergence into power electronics [77]. The concept of MPC in power electronics is based on the mathematical model of the converter in terms of switching states, and predicting the systems variables' behavior in the future states. A cost function is used to force the control objectives to track the predefined references, by selecting an appropriate switching state that minimizes the cost function. For the digital implementation of the control method, the discrete mathematical model of the converter is required.

The control objectives for the proper operation of this seven-level converter are output currents, and FCs voltages'. In this section, the control objectives mathematical models are obtained in terms of switching states and converters parameters'. In each sampling time, control objectives values and their references are predicted for the next sample time, and then a cost function is used to select the best switching state that minimizes the error between the control objective values and their references.

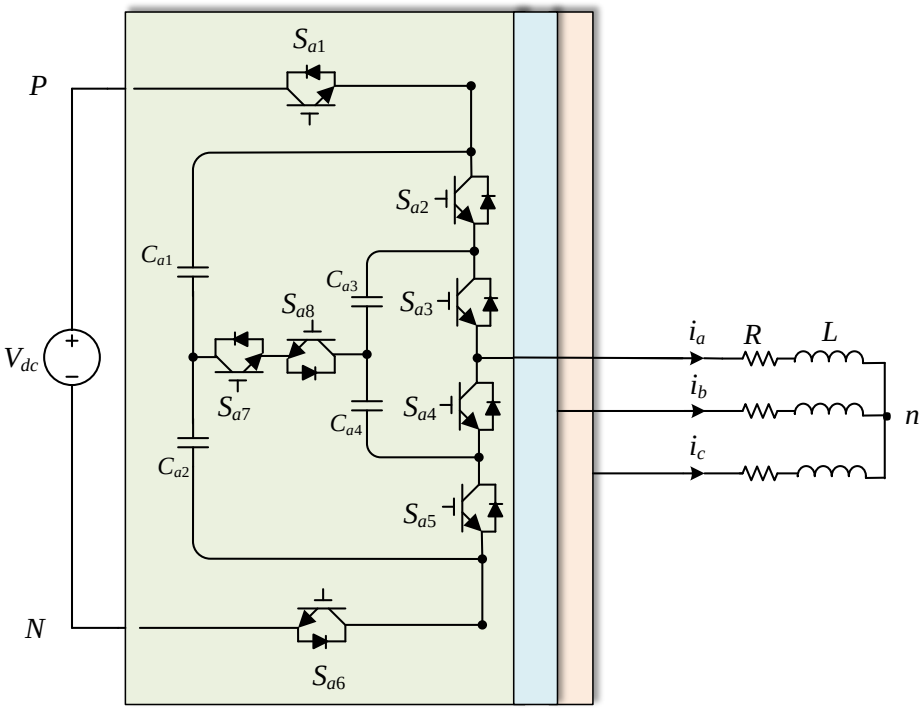


Figure 5.19 Circuit diagram of the proposed seven-level topology

Kirchhoff's voltage law is applied to the circuit diagram, shown in Figure 5.19, to obtain the phase voltage of the converter in terms of load current that results in;

$$V_{xN} = Ri_x + L\frac{di_x}{dt} + V_{nN} \tag{5.9}$$

where; $x = a,\ b,\ c,$ and V_{xN} is the phase voltage of the converter respect to the negative dc-link voltage (N). i_x is the output current of the converter. To simplify the equations filter and load resistance and inductance are shown as R and L. V_{nN} is the common mode voltage, which can be obtained as;

$$V_{nN} = \frac{1}{3}\left(\sum_{x=a,b,c} V_{xN}\right)$$
$$V_{xn} = V_{xN} - V_{nN} \tag{5.10}$$

From (5.9) and (5.10), and first order derivative of the output current (5.11), the discrete mathematical model of the output current in term of phase voltage and converter parameters can be obtained as;

$$\frac{di_x}{dt} = \frac{i_x(k+1) - i_x(k)}{T_s} \tag{5.11}$$

$$i_x(k+1) = \frac{T_s}{L + RT_s} V_{xn}(k+1) + \frac{L}{L + RT_s} i_x(k) \tag{5.12}$$

where k, and k+1 refer to present and next sampling interval, and T_s is sample time. As shown in (5.12), to calculate the output current ($i_x\,(k+1)$) in the next sampling interval, the output current at k_{th} instant which is obtained from output current sensors, and phase voltages in $(k+1)_{\text{th}}$ instant are required. Phase voltage in $(k+1)_{\text{th}}$ is calculated in terms of all switching states, which is a prediction of the phase voltage for the next sampling interval using equation (5.10).

Equation (5.13) from Table 5.1 shows the relationship between the output voltage and switching states of the converter where 0 and 1 represent if the switch is OFF or ON respectively;

$$\begin{aligned} V_{xN} = {} & V_{dc}(S_{x1}) + V_{Cx1}(S_{x2} - S_{x3} - S_{x4} + S_{x6}) + \\ & V_{Cx2}(S_{x6} - S_{x5}) + V_{Cx3}(S_{x3} - S_{x2}) \\ & + V_{Cx4}(S_{x5} - S_{x4}) \end{aligned} \tag{5.13}$$

where $V_{Cx1\text{-}4}$ are FCs voltages obtained from voltage sensors. Therefore, equations (5.10), (5.12), and (5.13), with the obtained output currents obtained from current sensors, will result in the output current in next sampling interval in terms of all switching states.

To predict the FCs voltages in the next sampling interval, the following equations are used. First order derivation is used to obtain the discrete-time mathematical model for the FCs voltages';

$$\begin{aligned} & i_{Cxi}(k) = C_{xi}\frac{dV_{Cxi}}{dt} \\ & \frac{dV_{Cxi}}{dt} = \frac{V_{Cxi}(k+1) - V_{Cxi}(k)}{T_s} \\ & V_{Cxi}(k+1) = V_{Cxi}(k) + \frac{T_s}{C_{x1}} i_{Cxi}(k) \\ & x = a,b,c \_ i = 1,2,3,4 \end{aligned} \tag{5.14}$$

As shown in equation (5.14), to calculate the FCs voltages at $(k+1)_{\text{th}}$ instant, the FCs voltages obtained from voltage sensors, and the capacitor currents ($i_{C\text{xi}}$) are required. The capacitor currents in terms of switching states can be calculated as;

$$\begin{aligned} & i_{Cx1}(k) = (S_{x1} - S_{x2}) i_x(k) \\ & i_{Cx2}(k) = (S_{x1} - (S_{x2} \parallel S_{x7})) i_x(k) \\ & i_{Cx3}(k) = (S_{x2} - S_{x3}) i_x(k) \\ & i_{Cx4}(k) = ((S_{x2} \parallel S_{x7}) - S_{x3}) i_x(k) \end{aligned} \tag{5.15}$$

The references for the control objectives, which are the output currents and FCs voltages, are predefined. As mentioned before reference for V_{Cx1} and V_{Cx2} is $V_{dc}/3$,

and for V_{Cx3}, and V_{Cx4} is $V_{dc}/6$. Since the dc-link voltage is constant, the references for FCs voltages do not require prediction for the next sampling interval. The output currents references are user-defined, and are predicted for the next sampling interval by Langrage extrapolation as follow, where the user-defined output current reference is i^*_x [77];

$$i_x^*(k+1) = 4i_x^*(k) - 6i_x^*(k-1) + 4i_x^*(k-2) - i_x^*(k-3) \tag{5.16}$$

The goal of the controller is to minimize the error between the predicted control objectives and their references. Therefore, a cost function is used to select the switching state that minimizes the error between the output current and their references and FCs voltages references and their actual values. Since there are 12 switching states, as shown in Table 5.1, to generate seven-level voltages at the output terminal, in each sampling time, all the possible switching states (12^3) are examined by the cost function and the best switching state which minimizes the cost function is selected and applied during next sampling interval. When the best switching state is selected, then the gate signals corresponding to these switching states will be extracted from Table 5.1 and then applied to power switches of the inverter.

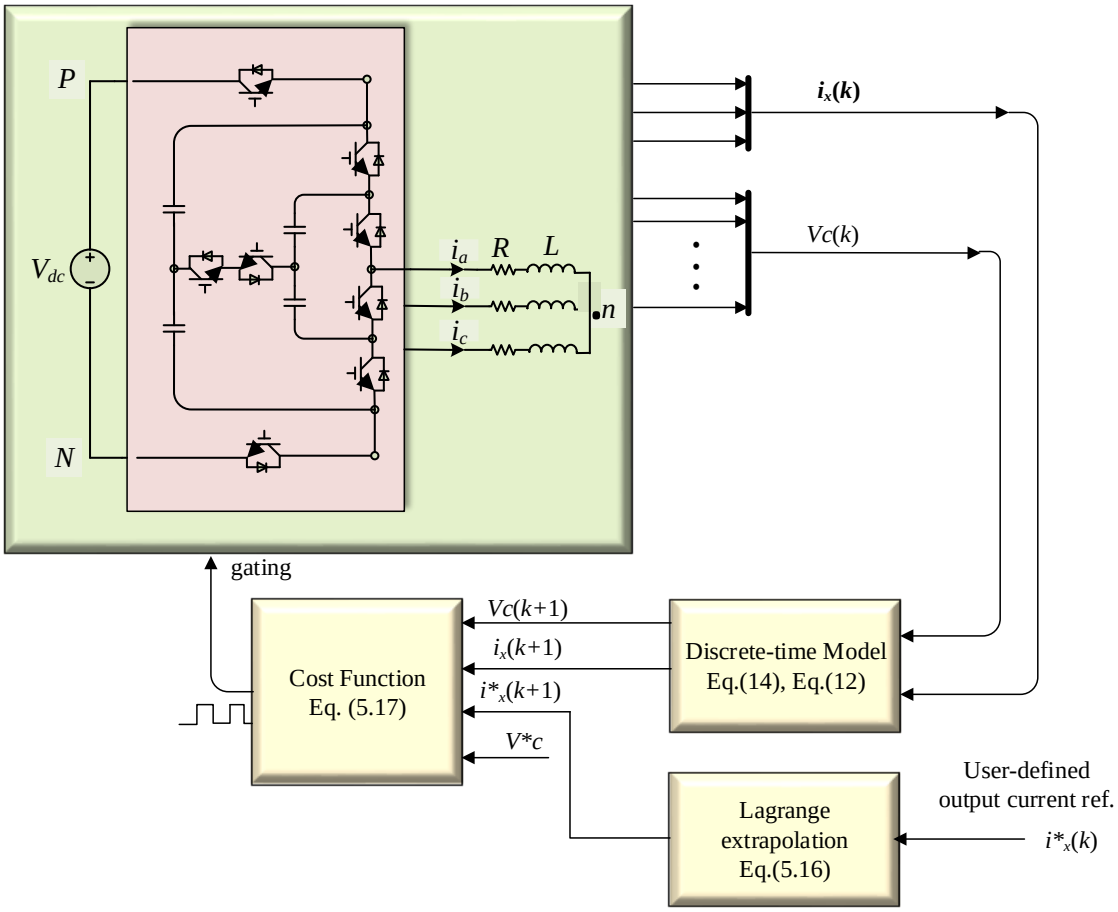


Figure 5.20 Finite control set model predictive control strategy for the seven-level converter

$$CF = \sum_{x=a,b,c} \left[i_x^*(k+1) - i_x(k+1) \right]^2 + wfcap \sum_{x=a,b,c} \left\{ \sum_{i=1}^{4} \left[v_{Cxi}^* - v_{Cxi}(k+1) \right]^2 \right\} \quad (5.17)$$

where wf_{cap} is the weighting factor. As the current control and FCs voltage balancing have equal importance for the proper operation of this topology, the weighting factor is calculated in terms of the rated output current and capacitor

voltage references to compensate for the difference in nature of the control objectives.

The following equation is used to calculate the weighting factor [101];

$$wfcap = \frac{i_{o,rated}}{V_{cap,ref}} \tag{5.18}$$

The block diagram of the developed control method based on MPC is shown in Figure 5.20. The developed control method is convenient to implement on digital controller platforms, and both control objectives are satisfied simultaneously.

5.3.2 Experimental Results

The effectiveness of the developed control method and the feasibility of the seven-level topology are evaluated experimentally on a scaled-down prototype of this topology. The experimental results are shown for steady-state and transient conditions. The parameters used to obtain the experimental result are shown in Table 5.7. The sample time is 100 µs.

TABLE 5.7 PARAMETERS OF THE STUDY SYSTEM

Converter parameters	**Values**
Converter rating (kVA)	4
Capacitor Value (µF)	1000
Input dc voltage (V)	330
Output inductance (mH)	11
Output load (**Ω**)	17

A. Steady-State Condition

The steady-state experimental results are shown in Figure 5.21, and Figure 5.22, where the reference for the output currents are $i_{ref} = 10$ A, and 5 A respectively. The FCs voltages are shown, and as it can be seen the FCs capacitors are well balanced at their desired values, which are $V_{dc}/3 = 110$ V, and $V_{dc}/6 = 55$ V. In addition, the performance of the converter is evaluated for the low-frequency operation which is shown in Figure 5.23, for $i_{ref} = 10$ A, and f= 5 Hz. As can be seen from Figure 5.22, at low-frequency operation, the FCs voltages are well balanced, which makes it a suitable choice for low-speed drive applications.

B. Transient Conditions

The output current reference and frequency step change are experimented with in this section, to show the dynamic performance of the developed control method, and the 7-level topology operation during transients.

Figure 5.24 shows the current reference step change from $i_{ref} = 10$ A to $i_{ref} = 5$ A, as it is shown as the reference changes, it is followed by the output current perfectly, which demonstrates the fast dynamic response of the developed control method. In Figure 5.25 the frequency is changed from 5 to 30 Hz, as it is shown, the flying capacitors are well balanced during the transition. As it can be seen in the transient conditions, the capacitor voltages are controlled at the desired values,

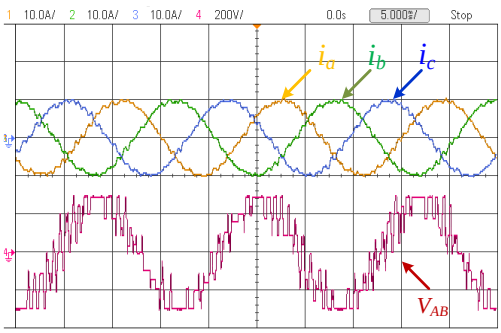
and any change in the system is followed by the controller perfectly and makes this seven-level topology an attractive choice for drive applications.

C. Controller Evaluation

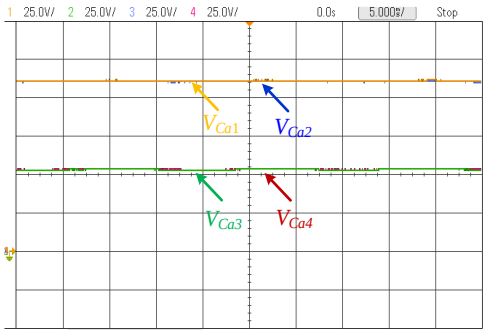
Figure 5.26 shows the experimental results to evaluate the controller performance when the controller is interrupted and after a few cycles (150 ms), the controller is reactivated again.

As can be seen from Figure 5.26, the FCs voltages deviated from their desired values due to the lack of control, then after the controller reactivation, the FCs voltages are converged to their desired value.

This experiment determines the effectiveness of the controller to balance capacitor voltages.

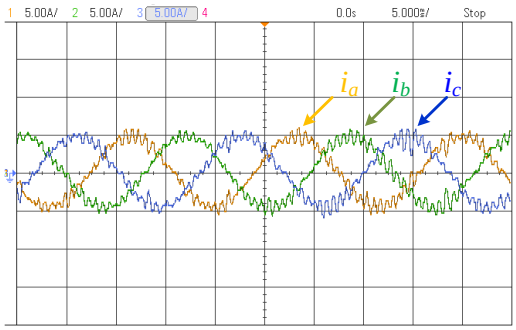


(a) Inverter output currents, and voltage (10A/div, 200V/div 5ms/div)

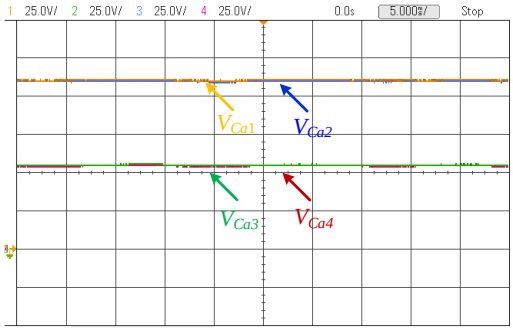


(b) Voltage of flying capacitors (25V/div, 5 ms/div)

Figure 5.21 Experimental results, i_{ref} = 10 A, f= 60Hz

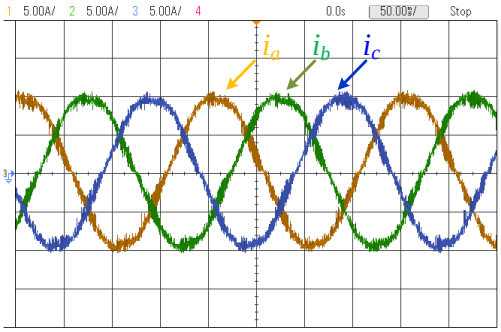


(a) Inverter output currents (5A/div, 5ms/div)

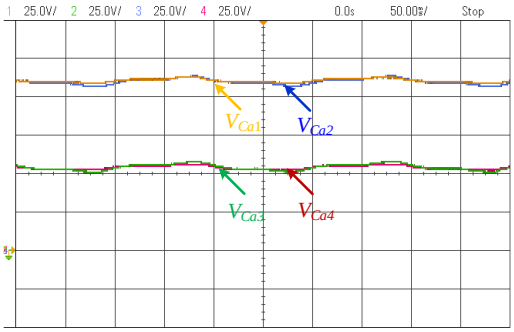


(b) Voltage of flying capacitors (25V/div, 5ms/div)

Figure 5.22 Experimental results, i_{ref} = 5 A, f= 60Hz

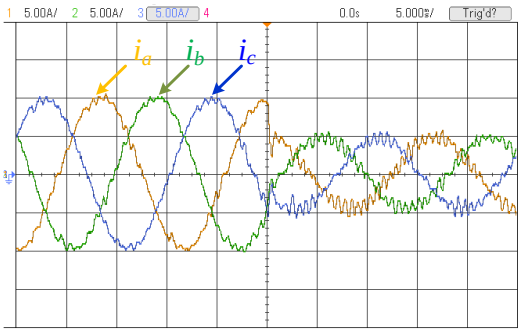


(a) Inverter output currents, and voltage (5A/div, 50V/div 5ms/div)

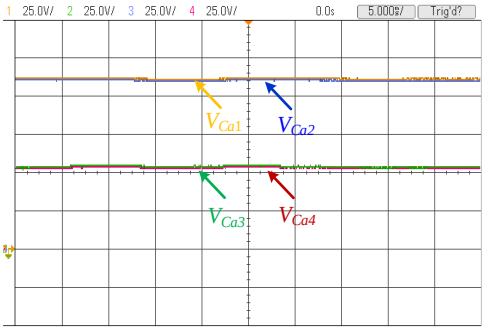


(b) Voltage of flying capacitors (25V/div, 50ms/div)

Figure 5.23 Experimental results, i_{ref} = 10 A, f= 5 Hz

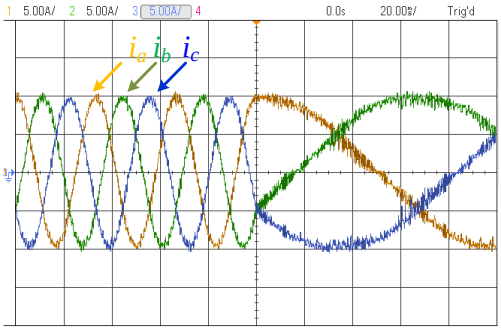


(a) Inverter output currents, and voltage (5A/div, 5ms/div)

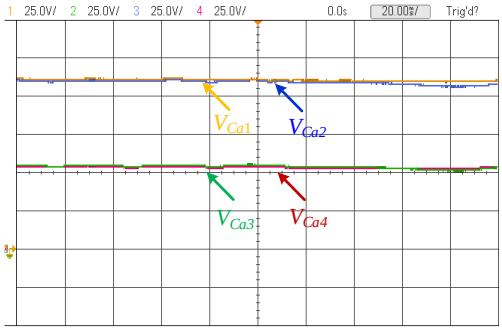


(b) Voltage of flying capacitors (50V/div, 10ms/div)

Figure 5.24 Experimental results, i_{oref} changes from 10 A to 5 A



(a) Inverter output currents, and voltage (5A/div, 20ms/div)



(b) Voltage of flying capacitors (25V/div, 20ms/div)

Figure 5.25 Experimental results, frequency changes from 5 Hz to 30 Hz

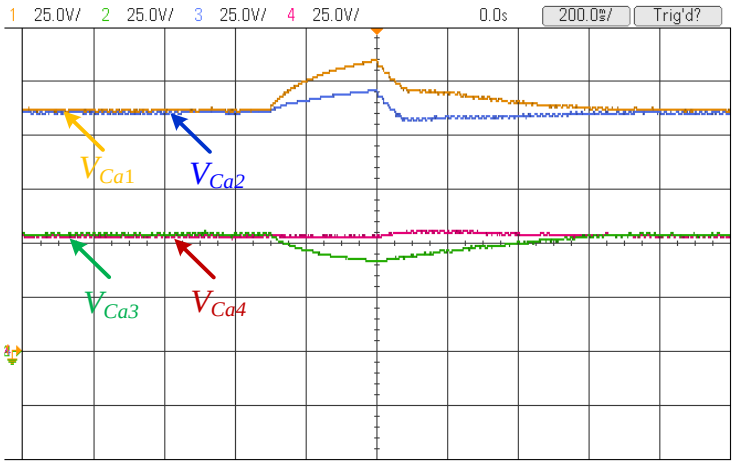


Figure 5.26 Voltages of flying capacitor when the controller is deactivated and activated

This section has presented the application of model predictive control in a seven-level voltage source inverter. The strategy is easy to understand and implement. The steady-state and transient results confirm that the proposed MPC strategy controls effectively the load currents while keeping balanced capacitor voltages'. This is an important advantage in comparison to classical modulation and control

strategies, which cannot keep balanced voltages for all operating conditions. As a general conclusion, it can be also affirmed that this topology is able to provide a high-quality voltage to the load while having a smaller amount of power semiconductors than other topologies.

5.4 Model Predictive Current Control of the Proposed Seven-Level Converter with Reduced Computational Burden

Recently, in power electronics, vast research has been done in order to improve the control of the power converters to achieve more efficient and simple controllers. Model predictive control is one of the control techniques that has been widely used in power electronics recently due to its advantages such as; fast dynamic response, no need for PI regulators and PWM blocks, and capability of nonlinearity inclusion, etc. On the other hand, the high number of calculations especially for higher-level topologies is the disadvantage of this approach.

As previously discussed, for proper operation, and equal voltage stress on active switches of the presented seven-level topology, the outer and inner flying capacitors of each phase must be balanced at $V_{dc}/3$ and $V_{dc}/6$ respectively. A control technique based on conventional FCS-MPC was developed in order to control the FCs voltages in the previous section. The disadvantage of this approach is the high number of calculations of the developed control method based on FSC-MPC, due

to the correlation between the control objectives of each phase with each other. The higher number of calculations results in a slower controller, and longer sampling times, which can affect the performance and output quality of the converter. This will be a significant challenge, where the controller has other tasks to perform in each sampling time in a practical application. In this section, a new controller is proposed to address this challenge.

In this section, a computational efficient FSC-MPC (RED MPC) is developed that significantly reduces the number of calculations required to control the output current and the FCs voltages' of the seven-level topology. The developed control technique reduces the number of computations by an approximation in the power converter's circuit, where the control objectives of each phase can be controlled independently.

The number of calculations to control the output current and FCs voltages of the seven-level topology for the conventional FCS-MPC is 12^3, however, based on the computational efficient FCS-MPC is 36, which shows the effectiveness of the new MPC in limiting the number of calculation.

In the following sections, a review has been done on other computational efficient MPC approaches to investigate the superiority of the proposed controller. Then the mathematical model of the proposed RED MPC is obtained and the controller is

developed for the proposed seven-level topology. Moreover, simulation and experimental results have been shown to demonstrate the performance and feasibility of the developed control method applied to a seven-level topology.

5.4.1 Advantages of the New FCS-MPC over Other Computational Efficient MPC Approaches

Recently, Model predictive control has gained significant attention as a tool to control high-power multilevel converters with the development of fast digital control platforms. The fast dynamic response [102] due to no need for PI regulators and PWM blocks, robustness to the variation of system parameters, system's nonlinearity inclusion, and multiple control objectives simultaneous satisfaction, are the advantages of control techniques developed based on MPC. Due to the aforementioned advantages, the MPC strategies have been applied to various multilevel topologies [103].

The conventional FCS-MPC [88] requires the discrete mathematical model of the power converter in terms of switching states and parameters of the multilevel power converter to predict the values of the control objectives in each sampling time for the next sampling interval. Then, a cost function is used to determine the best switching state of each phase that minimizes the error between the predicted values of the control objectives and their pre-defined references. The disadvantage

of this approach is the computational burden of the controller based on FSC-MPC due to a large number of switching states in multilevel converters, especially in the higher level topologies, since in each sampling time, the control objectives must be predicted for all of the possible switching states of the three-phase. This is due to the correlation between the control objectives of each phase with each other.

In [104], a new MPC algorithm to reduce the number of calculations for multilevel CHB topologies is presented. In this approach, the triangular region that the reference voltage vector resides in is determined, and then only the three nearest voltage vectors are used, which reduces the number of calculations. However, determining the triangle region in higher-level topology significantly increases the complexity of the control method.

In [105], the computational burden of MPC is reduced by a priority sorting approach for modular multilevel converters. The control objectives in this approach are the grid-side current, and circulating current, which are satisfied by separate cost functions, and the capacitor voltage balancing objective is satisfied using a priority sorting approach. The computational burden for each control objective is reduced in this approach, however, the complexity of the overall control method is increased. Also, the computational load of the MPC strategy is reduced in [106] for

modular multilevel converters where submodule capacitor voltage control is decoupled from the cost function and balanced using a sorting algorithm.

In [107], a computationally efficient FCS-MPC method is proposed for nested neutral point converters. In this approach, undesired switching states are ignored by using Lyapunov principle in the sector distribution method-based space vector modulation scheme. In addition, the weighting factor is eliminated by using an optimization strategy based on fuzzy decision-making. The improvement in computational efficiency is achieved in this approach by using complex mathematics, which in a sense removes the simplicity of the FCS-MPC.

The model predictive control approaches discussed above increase the complexity of the overall control method by introducing complex algorithms into the controller in order to reduce the number of calculations. However, the computational efficient FSC-MPC presented in this section reduces the number of calculations by an approximation in the power converter's circuit equations. In a multilevel converter, with output current control, and FCs voltage balancing as the control objectives, there is a correlation between the control objectives of the three phases due to the Common Mode Voltage (CMV) of the power converter circuit. Applying Kirchhoff's voltage law to the power converter circuit shown in Figure 5.19, the

phase voltage of the converter with respect to the negative of the dc-link source can be obtained as;

$$V_{xN} = Ri_x + L\frac{di_x}{dt} + V_{nN} \tag{5.19}$$

where; $x = a,\ b,\ c,$ and i_x is the output current passing through the star-connected load shown as R, and L. the V_{nN} term is the CMV which can be calculated as;

$$V_{nN} = \frac{1}{3}(V_{aN} + V_{bN} + V_{cN}) \tag{5.20}$$

As can be seen from (5.19), and (5.20), the three-phase output currents are related to each other through the CMV, which will force the controller to take into account the three-phase simultaneously that increases the number of calculations. Assuming symmetrical sinusoidal output currents, the phase voltages can be rewritten in terms of their spectral components, as the following equations state;

$$V_{xN} = \frac{V_{dc}}{2} + A\sin(\omega t + \varphi + \Phi_x) + HF_x \tag{5.21}$$

where; $V_{dc}/2$ is the dc component of the phase voltage, A is the fundamental component of the phase voltage (V_{xN}), φ is the phase displacement of the output current and voltage fundamentals, $\varphi = \{2\pi/3, -2\pi/3, 0\}$ for $x=a,b,\ c$ respectively, and HF_x is the high-frequency component that depends on selected switching pattern. Replacing (5.21) in (5.20) will result in;

$$V_{nN} = \frac{V_{dc}}{2} + HF_a + HF_b + HF_c \tag{5.22}$$

The approximation takes place in equation (5.23), where due to the low pass filtering of most loads, the high-frequency component can be neglected, therefore;

$$V_{nN} \approx \frac{V_{dc}}{2} \tag{5.23}$$

And by replacing (5.23) in (5.19);

$$V_{xN} \approx Ri_x + L\frac{di_x}{dt} + \frac{V_{dc}}{2} \tag{5.24}$$

As demonstrated by (5.24), the phase voltage and respectively the output current of each phase can be controlled independently by the approximation in (5.23), which will result in the possibility of controlling the output currents separately that reduces the number of calculations of FCS-MPC significantly. In the next section, the controller based on this approach is developed to control the output current and the FCs voltages' of the seven-level topology and it is explained, how the above approach reduces the number of calculations.

5.4.2 Developed FCS-MPC with Reduced Number of Calculation for the Seven-Level Topology

To apply the RED-MPC to the seven-level topology, the discrete-time mathematical model of the power converter in terms of the switching states, and the system parameters are required. The discrete-time mathematical model of the

power converter was obtained in 5.3.1 and is not repeated here since the model is identical to the previously obtained model. The only difference is in (5.10), where the common-mode voltage is calculated.

Therefore, replacing (5.23) and (5.24) in (5.10) will result in;

$$V_{xN}(k+1) \simeq Ri_x(k+1) + L\frac{di_x}{dt} + \frac{V_{dc}}{2} \tag{5.25}$$

By replacing (5.25) in (5.12), the predicted current for the next interval is calculated;

$$i_x(k+1) \simeq \frac{T_s}{L+RT_s}V_{xN}(k+1) + \frac{L}{L+RT_s}i_x(k) - \frac{V_{dc}}{2}\frac{T_s}{L+RT_s} \tag{5.26}$$

As a result, it can be seen that each predicted phase current is independent of other phase currents and consequently the flying capacitors voltages' of each phase can are decoupled from other phases.

The cost function of the conventional MPC for the proposed seven-level topology is obtained in (5.17). As shown in (5.17), due to the correlation between the phase voltage of different phases, the output currents, and respectively the FCs voltages are related to each other. Since the control objectives are related, the switching state of each phase affects the control objectives of other phases. Therefore, the cost function in (5.17) is implemented by three loops that in each loop cost function

is calculated for 12 switching states of the seven-level topology for each phase, to find the best switching pattern among 12^3=1728 switching combination.

By approximation in (5.23), as discussed before the control objectives of the three-phase system can be controlled separately for each phase by the following cost functions;

$$\begin{aligned} CF_a &= \left[i_a^*(k+1) - i_a(k+1) \right]^2 + wf \sum_{i=1}^{4} \left\{ \left[v_{Cai}^* - v_{Cai}(k+1) \right]^2 \right\} \\ CF_b &= \left[i_b^*(k+1) - i_b(k+1) \right]^2 + wf \sum_{i=1}^{4} \left\{ \left[v_{Cbi}^* - v_{Cbi}(k+1) \right]^2 \right\} \\ CF_c &= \left[i_c^*(k+1) - i_c(k+1) \right]^2 + wf \sum_{i=1}^{4} \left\{ \left[v_{Cci}^* - v_{Cci}(k+1) \right]^2 \right\} \end{aligned} \tag{5.27}$$

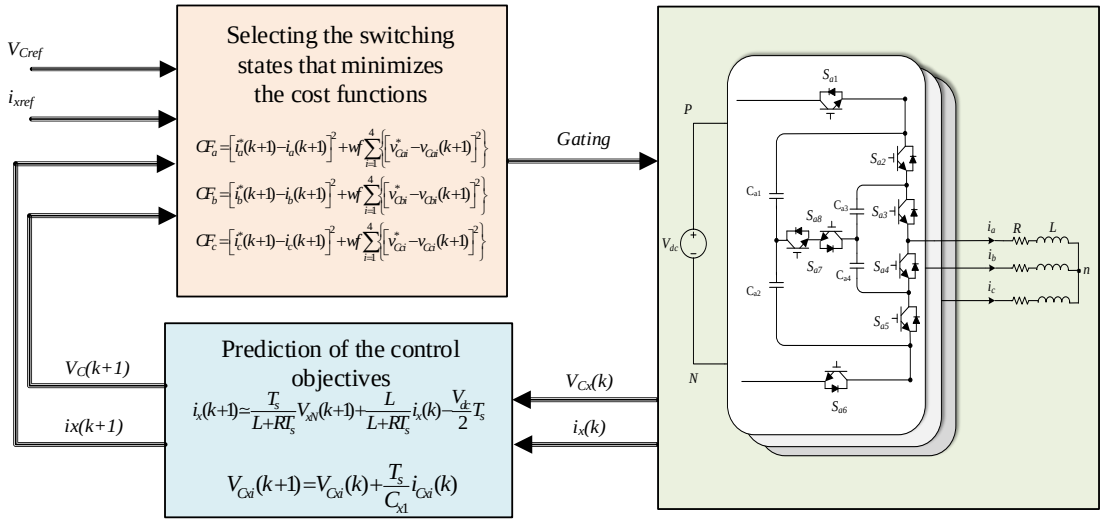


Figure 5.27 The block diagram of the developed RED-MPC control method

As it is shown in (5.27), the best switching pattern for each phase is selected separately, which results in the 12× 3 number of calculations, which is significantly

reduced compared to conventional FSC-MPC. The block diagram of the developed control method is shown in Figure 5.27.

5.4.3 Simulation Studies

The simulation results are shown for steady-state and transient conditions, and the output current and FCs voltages are shown in the results. Moreover, a comparison has been done regarding the output power quality, and prediction error between the conventional FCS-MPC and the controller developed for reducing the number of calculations. The system parameters in the simulation results are shown in Table 5.8. The sampling time in simulation results is 50 µs. The developed controller in the results is referred to as RED MPC.

TABLE 5.8 PARAMETERS OF THE SIMULATION STUDY SYSTEM

Converter parameters	Values
Converter rating (MVA)	2
Capacitor Value (µF)	1000
Input dc voltage (kV)	10.2
Output frequency (Hz)	60
Output inductance (mH)	22.4
Output load (Ω)	28.4

A. Steady-state Studies with reduced number of calculations

In this part, the steady-state performance of the developed control method is evaluated in different load conditions, power factors, and output frequencies.

In Figure 5.28, the output current is set to 0.9pu (i_{ref} =211 A) while the power factor and output frequency are set to 0.9, and 60 Hz respectively. In Figure 5.29, the PF is set to 0.5, with the same condition as the results shown in Figure 5.28. In Figure 5.30, the output current is set to 0.5pu (i_{ref}=117) A, and in Figure 5.31, the output frequency is set to 5 Hz to determine the controller performance in low-frequency operation while the PF is set to 0.9. As it can be seen in the results, the FCs voltages and output currents tracked their references perfectly

B. Transients of the strategy with the reduced number of calculations

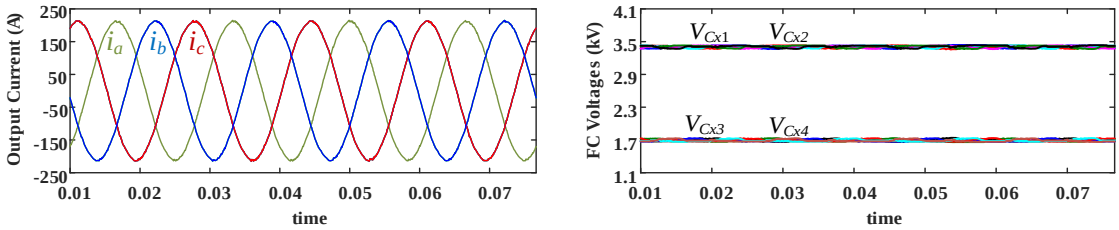
In this section, transient conditions are simulated by a step-change in current reference and output frequency.

The output current is changed from 0.9pu to 0.5pu in Figure 5.32, and the frequency is changed from 20 to 40 Hz in Figure 5.33, while the power factor is set to 0.9.

As it is shown the FCs voltages are well balanced during the transients, and the output current magnitude and frequency followed the references immediately, which is due to the fast dynamic response feature of the FCS-MPC.

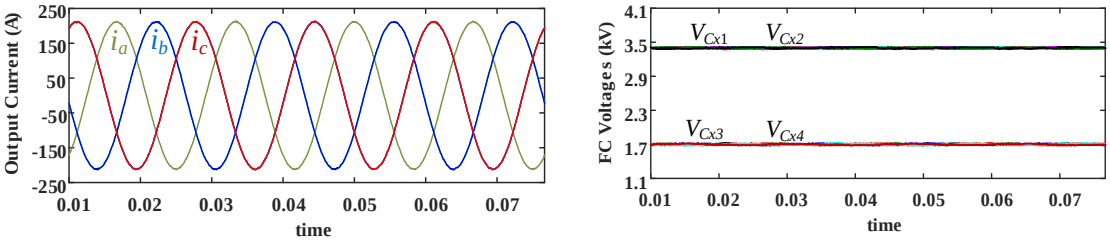
In addition, in Figure 5.34, the controller is deactivated for 0.05 s, and reactivated, to evaluate the controller after a fault that causes an interruption in

the controller operation, as is shown after the controller is reactivated the FCs voltages are converged to their desired value after a few cycles.



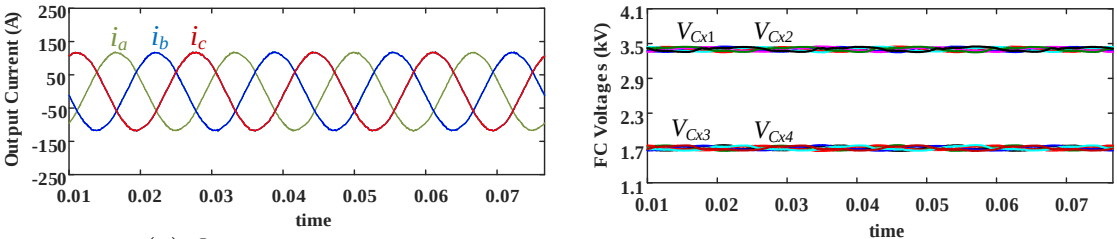
(a) Output currents (b) Flying capacitor voltages

Figure 5.28 Steady-state simulation, i_{ref} = 0.9pu and PF = 0.9, f = 60 Hz



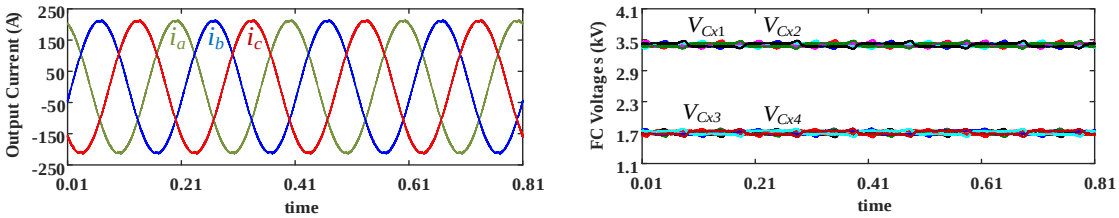
(a) Output currents (b) Flying capacitor voltages

Figure 5.29 Steady-state simulation, i_{ref} = 0.9pu and PF = 0.5, f = 60 Hz



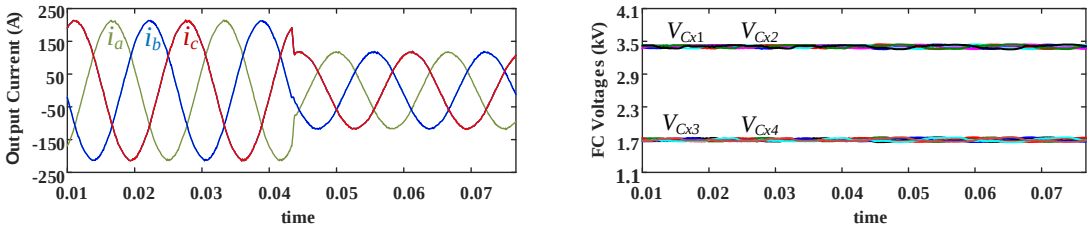
(a) Output currents (b) Flying capacitor voltages

Figure 5.30 Steady-state simulation, i_{ref} = 0.5pu and PF = 0.9, f =60 Hz



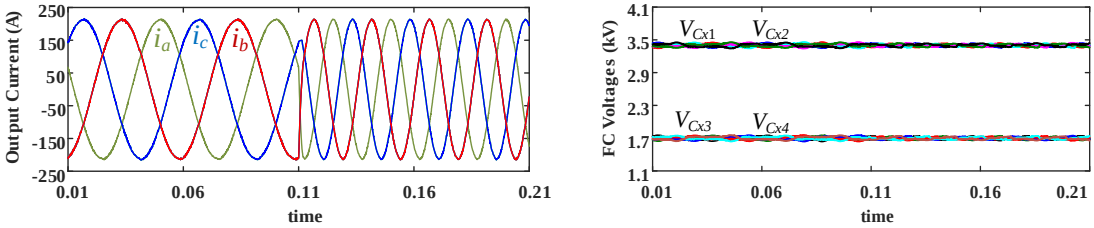
(a) Output currents (b) Flying capacitor voltages

Figure 5.31 Steady-state simulation, i_{ref} = 0.9pu and PF = 0.9, f =5 Hz



(a) Output currents (b) Flying capacitor voltages

Figure 5.32 Transient simulation, i_{ref} changed from 0.9pu to 0.5pu



(a) Output currents (b) Flying capacitor voltages

Figure 5.33 Transient simulation, i_{ref} changed from $f = 20$ Hz to 40 Hz

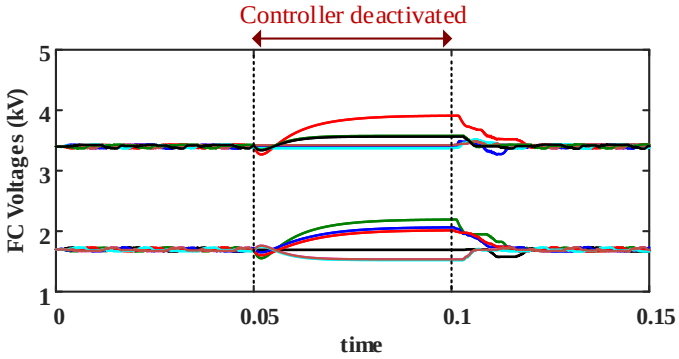


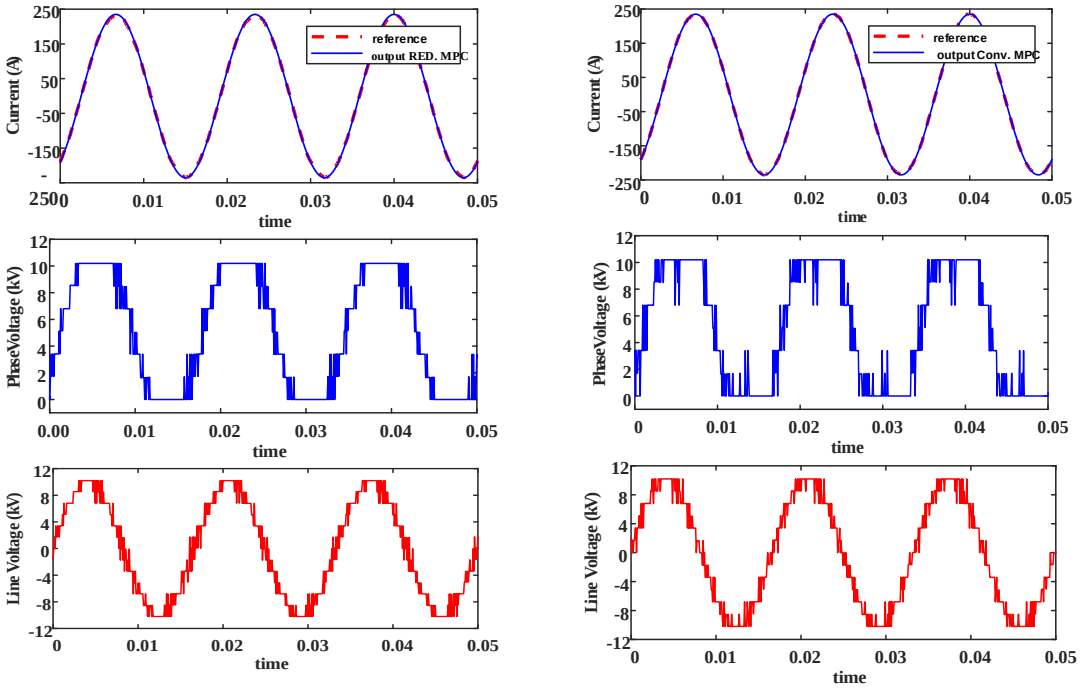
Figure 5.34 Transient simulation, controller evaluation

C. conventional and efficient MPC comparison

In this section, a comparison has been done regarding reference tracking, output power quality, and estimation accuracy between FSC-MPC conventional, and reduced number of calculation approach applied to the seven-level topology.

In Figure 5.35, the output current of phase A, with its reference, and phase and line voltage of the 7-level topology are shown for conventional and computational efficient FSC-MPC. As it is shown in both control methods the output reference is tracked perfectly, and approximation in the power circuit did not affect the reference tracking capability of the developed control method. In addition, as can be seen in Figure 5.35, the phase voltage in the reduced number of calculations has fewer jumps to different levels since the control of each phase has been done separately, which reduces the dv/dt over the active switches.

Moreover, THD analysis has been done for output voltage and current of the seven-level topology, to compare conventional and computational efficient FCS-MPC. The acceptable THD is dependent on the application. For instance, the acceptable THD for a grid-connected application at the Point of Common Coupling (PCC), is set by IEEE_std519-2014, which is related to the bus voltage level of PCC for voltage THD, and to maximum short circuit current, and maximum load demand current at PCC for current THD. Typically, the current THD should be less than 5%. For motor drive applications, high voltage distortion can cause core losses which can affect the efficiency of the system and thus requires additional filter before applying the voltage to the motor.



(a) RED MPC (b) Conv. MPC

Figure 5.35 Reference tracking, Phase voltage, Line Voltage

The results are shown in Table 5.9, as can be seen, the outputs THD of the conventional approach is better than computational efficient, which is due to the approximation in the mathematical model of the converter to reduce the number of calculations. However the output THD of the computational efficient approach is still acceptable, and the number of calculations has reduced significantly as discussed in the experimental result section, which can be assumed as an acceptable trade-off.

TABLE 5.9 THD ANALYSIS COMPARISON

Output Current	**Line Current THD Red. MPC**	**Line Current THD Conv. MPC**	**Line Voltage THD Red. MPC**	**Line Voltage THD Conv. MPC**
1pu	1.05 %	0.66 %	14.84 %	13.94 %
0.8pu	1.20 %	0.82 %	29 %	19.51 %
0.6pu	1.67 %	1.04 %	43.6 %	25 %
0.4pu	1.56 %	1.25 %	39.43 %	29 %
0.2pu	2.97 %	1.98 %	80 %	44 %

The results in Table 5.9 show that the current and voltage THD is decreasing when the operating point in RED. MPC changes from 0.6 p.u. to 0.4 p.u., however, this is not the case for conventional MPC. The reason is that this range of the operating point is where there are more flexible and redundant switching states to control the flying capacitor, therefore controlling the capacitors is easier which results in more focus of the controller on the output current that leads to lower THD for RED. MPC. However, in the conventional method, since there is a single cost function to control all of the FCs voltages, and output currents of the converter, the focus of the controller would be more on the flying capacitors which lead to an increase of the THD of the output current in the aforementioned range.

To investigate the prediction error, the root mean square error of the reference and output current in different load conditions is calculated for both methods, which is shown in Table 5.10.

TABLE 5.10 PREDICTION ERROR COMPARISON

Output Current	RMSE Red. MPC	RMSE Conv. MPC
1pu	2.426	2.425
0.8pu	1.657	1.074
0.6pu	1.656	1.021
0.4pu	1.061	0.829
0.2pu	1.008	0.699

As can be seen, the RMSE for Red. MPC is almost equal to Conv. MPC in rated load, and is slightly higher in lower load conditions. Therefore, the effect of approximation is not significant in the prediction error.

D. Frequency spectrum of the common mode voltage

Theoretically, the CMV must contain the switching frequency components and third-order harmonics. The frequency spectrum of the CMV mainly contains the DC value, and the 3^{rd}, 9^{th}, 15^{th}, 21^{st}, 27^{th} order harmonics, however, the DC value is dominant.

In order to investigate the frequency spectrum of the CMV, FFT analysis has been done in MATLAB\Simulink, which the results are shown in Table 5.11. As can be seen, the CMV mainly contains the DC component. These results alongside the simulation and experimental studies show that approximation of the CMV as a DC value is valid, and does not have a significant effect on the performance of the controller based on MPC.

TABLE 5.11 FREQUENCY SPECTRUM OF CMV

Frequency spectrum	CMV
DC component	1.00
3rd order	0.12
9th order	0.02
15th order	0.03
21st order	0.01
27th order	0.02

5.4.4 Experimental results

Similar to the simulations, experimental results for steady-state and transients are shown. The parameters used in the experiments are shown in Table 5.12. The scaled-down prototype is shown in Figure 5.36. The IGBT modules are from Semikron model SKM50GB12T4. LEM current sensors (LA55-P) and voltage sensors (LV25-P) are used, and the capacitors are 1000 µF 450 VDC from Cornell Dubilier. Gate drivers, model L501252, from Semikron is used.

TABLE 5.12 PARAMETERS OF THE EXPERIMENTAL STUDY SYSTEM

Converter parameters	Values
Converter rating (kVA)	2
Capacitor Value (µF)	1000
Input dc voltage (V)	210
Output frequency (Hz)	60
Output inductance (mH)	10
Output load (Ω)	13

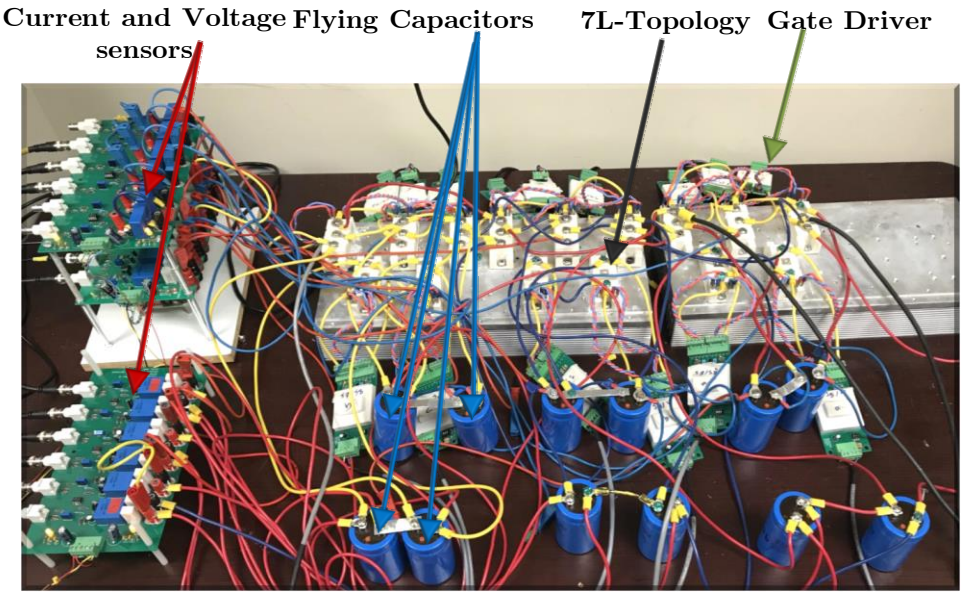


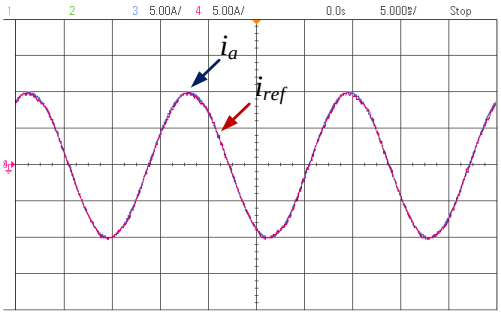
Figure 5.36 The scaled-down prototype setup

A. Steady State

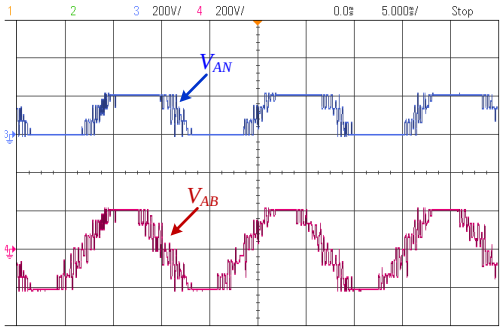
In this part, steady-state studies have been done to evaluate the performance of the seven-level topology controlled by the developed control method. In Figure 5.37 the reference and output current of the seven-level topology and the phase and line voltage is shown, to show the ability of the developed control method in reference tracking experimentally for a frequency of 60 Hz.

In Figure 5.38 to Figure 5.40 the output currents and FCs voltages are shown where the reference current is set to i_{ref}=10A and the power factor is 0.96, 0.46, and 0, respectively which demonstrate the perfect operation of the converter and controller in different power factors. In Figure 5.39, the resistor is changed to 2

ohms, and in Figure 5.40 to 0 ohm in order to change the power factor. In Figure 5.41, the current is set to 5A, to show the converter performance in half-load condition, in Figure 5.42 the frequency is set to f =5 Hz while the output current is set to i_{ref}=10A, and the power factor is 0.96. As can be seen in the results, the FCs voltages are well balanced at their desired values, which are 70 V and 35 V for outer and inner capacitors respectively.

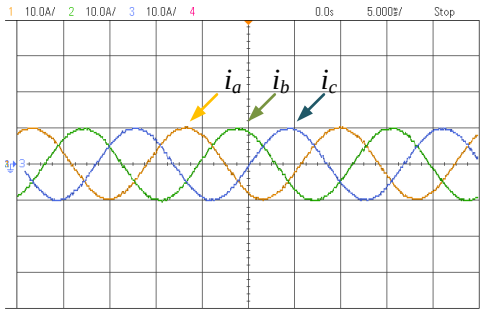


(a) Output and ref. current

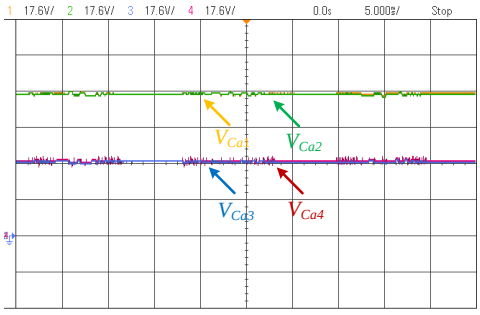


(b) Phase and line voltage

Figure 5.37 Experimental results, reference and actual output current, Phase and Line voltage (5A/div, 200V/div time: 5ms/div)

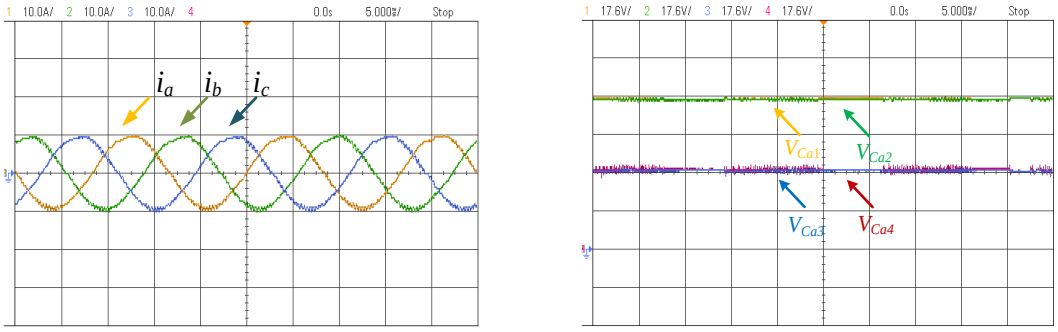


(a) inverter output currents



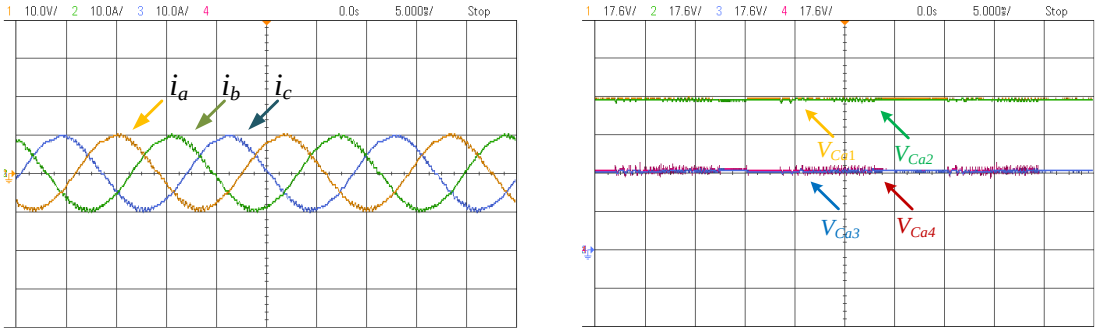
(b) voltages of flying capacitors

Figure 5.38 Experimental results, i_{ref} = 10 A, f_o= 60Hz, PF= 0.96. (10A/div, 17.6V/div, 5ms/div)



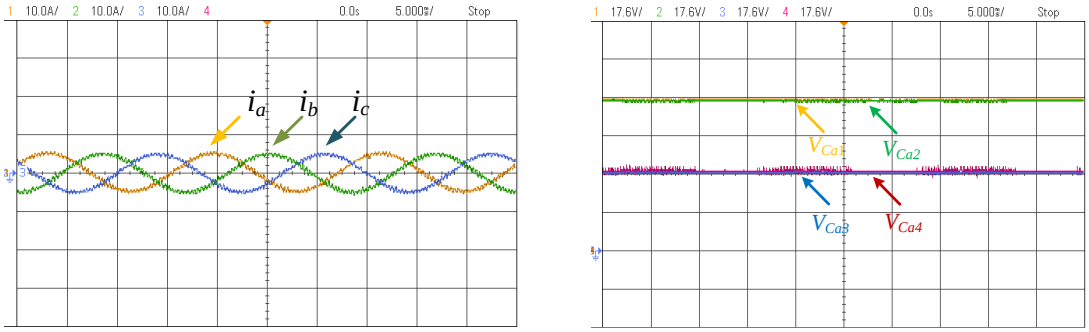
(a) inverter output currents (b) voltages of flying capacitors

Figure 5.39 Experimental results, i_{ref} = 10 A, f_o=60Hz, PF= 0.46. (10A/div, 17.6V/div, 5ms/div)



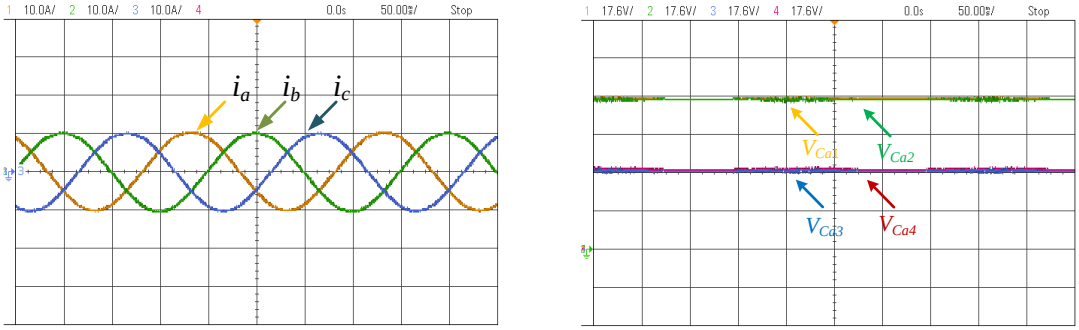
(a) inverter output currents (b) voltages of flying capacitors

Figure 5.40 Experimental results, i_{ref} = 10 A, f_o=60Hz, PF= 0 (10A/div, 17.6V/div, 5ms/div)



(a) inverter output currents (b) voltages of flying capacitors

Figure 5.41 Experimental results, i_{ref} = 5 A, f_o =60Hz, PF=0.96. (10A/div, 17.6V/div, 5ms/div)



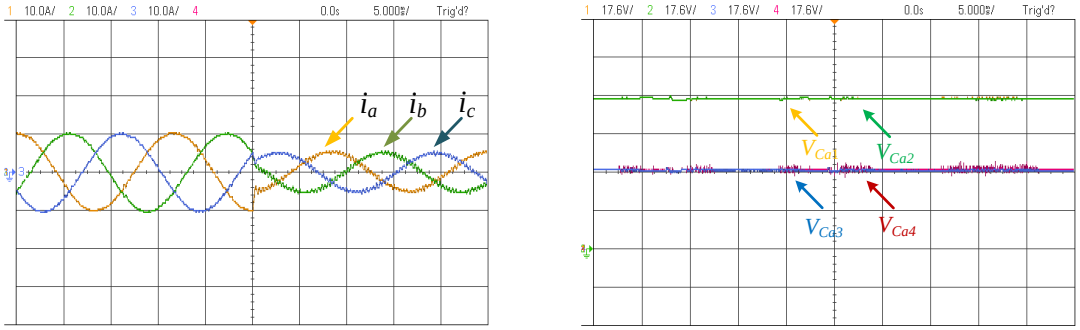
(a) inverter output currents (b) voltages of flying capacitors

Figure 5.42 Experimental results, i_{ref} = 10 A, f_o = 5 Hz, PF=0.96. (10A/div, 17.6V/div, 50ms/div)

B. Transients

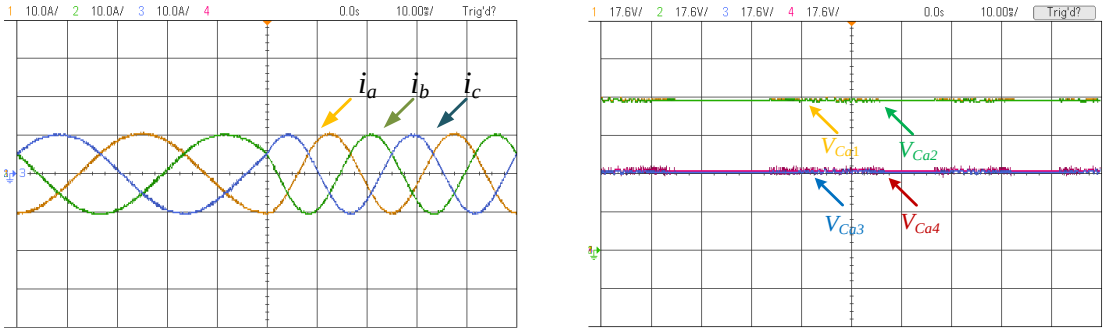
In this section, as in the simulation results, the performance of the developed control method is evaluated while the output current magnitude and frequency change.

In Figure 5.43 the output current reference is changed from i_{ref}=10A to 5A, and in Figure 5.44 the frequency is changed from 20 to 40 Hz. As it is shown the FCs voltages are well balanced during and after the transients, and the output currents followed the change in the current reference perfectly. Moreover, in Figure 5.45 the developed control method is evaluated while the controller is deactivated for 50 ms, as it is shown the FCs voltages deviate from their desired value while the controller is deactivated, and after a few cycle that the controller is reactivated the FCs voltages' are well balanced at their desired value.



(a) inverter output currents (b) voltages of flying capacitors

Figure 5.43 Experimental results, i_{ref} changes from 10 A to 5 A, PF=0.96. (10A/div, 17.6V/div, 5ms/div)



(a) inverter output currents (b) voltages of flying capacitors

Figure 5.44 Experimental results, frequency changes from 20 Hz to 40 Hz, PF=0.96. (10A/div, 17.6V/div, 10ms/div)

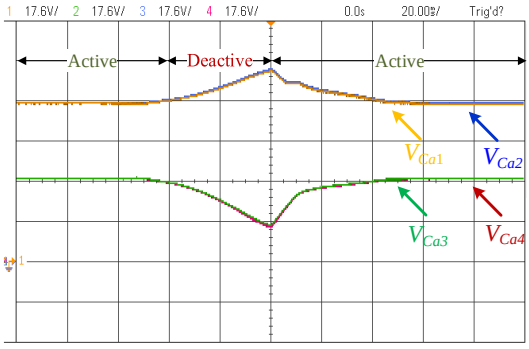


Figure 5.45 Voltages of flying capacitor when the controller is deactivated and activated

C. Calculation Time Comparison

As mentioned, the dSPACE is used to implement the controller to regulate the FCs voltages of the seven-level topology and to control the output current. The step-time of the controller can be understood in terms of the calculation time of the control method since the dSPACE terminates the controller if it is not able to do the calculation in the specified fixed step-time. In this case, the minimum step-time to run the controller for conventional MPC is 60 µs, while for the reduced number of calculation MPC is 10 µs, therefore the minimum step-time required for implementing the controller based on the reduced number of calculation MPC is reduced to 1/6 times of the time required for the conventional MPC. The execution time is not linear with respect to the reduction of the computations, since other tasks such as feedbacks from the FCs and output currents, gating generators, and initializations require some time that is common for both approaches and affects the overall execution time. Therefore the execution time is decreased only six times.

This demonstrates the effectiveness of the developed control method in reducing the number of calculations. This is an advantage for applications with more control objectives. The controller can satisfy more objectives in a shorter time since the number of calculations to control the converter is reduced.

5.5 Summary

A novel seven-level topology is proposed in this chapter, which has a fewer number of components in comparison to other existing advanced and classic topologies. First, to ensure the proper operation of the proposed converter topology, an SVM-based controller is developed to control the flying capacitors of the proposed topology. The flying capacitor voltage balancing ensures the seven-level voltage output and equal voltage stress on the active devices of the proposed topology.

Despite the excellent performance of the developed SVM-based controller in regulating the flying capacitors voltages in a wide range of operating conditions, demonstrated by the experimental results, the SVM-based controller cannot control the capacitors voltages in all operating conditions. This challenge rises in high power factors or low-frequency operation, which limits the application of the proposed topologies for grid-tied applications such as EV ultra-fast charging stations, and applications such as low-speed industrial motor drives.

To overcome the aforementioned barrier, a universal controller based on MPC is proposed to balance the flying capacitor voltages of the proposed topology and control the currents at the AC-side terminals of the proposed topology. Therefore, the proposed topology can be employed in different applications such as MV-connected ultra-fast charging stations, and industrial motor drives.

The challenge regarding the proposed MPC-based controller is the high computational burden of the controller due to the high number of switching states applicable to the proposed seven-level topology. To solve this problem, an efficient MPC-based controller is proposed that reduces the number of calculations required to balance the flying capacitors significantly.

Chapter 6

A New Architecture for MV-Connected EV Charging Stations

6.1 Introduction

As discussed in the previous chapters, the MV-connected EV charging station has received significant attention from researchers and manufacturers due to its advantages in comparison to the low voltage (LV)-connected EV charging stations in terms of efficiency, cost, and power density. On the other hand, as discussed previously, advanced MV multilevel topologies are an attractive choice for the AC/DC stage in grid-tied applications due to their advantages such as low voltage stress, high efficiency, and high power quality.

In this chapter, a new MV-connected EV charging station architecture is proposed based on the seven-level topology proposed in Chapter 5.

The proposed charging station architecture is compared to the LV-connected charging station architecture that uses a conventional three-phase PFC converter, and the four-level topology presented in Chapter 4 as the AC/DC stage. In this comparison study, performance, efficiency, and cost are investigated.

First, an LV-connected charging station is studied that employs the conventional three-phase PFC converter as the AC/DC stage. Then, the presented four-level topology is investigated to be used as the AC/DC stage to evaluate the application of advanced multilevel topologies in LV-connected EV charging stations. Finally, the proposed new MV-connected EV charging station based on the seven-level topology is presented and compared to the aforementioned LV-connected architectures.

6.2 LV Connected EV Charging Station with three-phase PFC as the AC/DC stage

In this section, an LV-connected ultra-fast EV charging station with a three-phase AC/DC PFC converter is studied in terms of efficiency, cost, and power quality. The charging station considered in this chapter, as shown in Figure 6.1, is a 1.4 MVA station with 4 charging stalls, and 8 terminals that are able to charge four EVs simultaneously at the maximum power of 350 kW, or eight EVs at the maximum power of 175 kW.

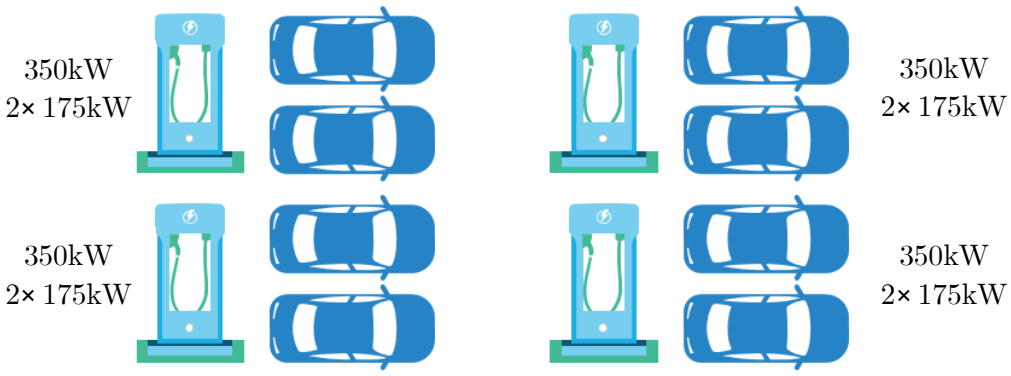


Figure 6.1 Studied charging station overall architecture

The maximum power of each charging unit is selected according to the latest charging standards as discussed in Chapter 1, which is 350 kW for EV ultra-fast charging. First, the operation and control of the LV connected charging station is discussed as well as the sizing of the line inductors, and the DC-link capacitor, then the efficiency, power quality, and cost of the AC/DC stage are determined.

6.2.1 Operation, and Control

The circuit diagram of the LV connected station is shown in Figure 6.2. As can be seen, the three-phase active front-end PFC converter is connected to the LV grid (480 V), through the line inductors to provide a DC-link equal to 1 kV. As discussed in the first chapter, the battery voltage of EVs are in the range of 200-900V DC, therefore to facilitate the design of DC/DC converters of the charging units, the DC-link voltage of the AC/DC stage is typically selected to be 1 kV.

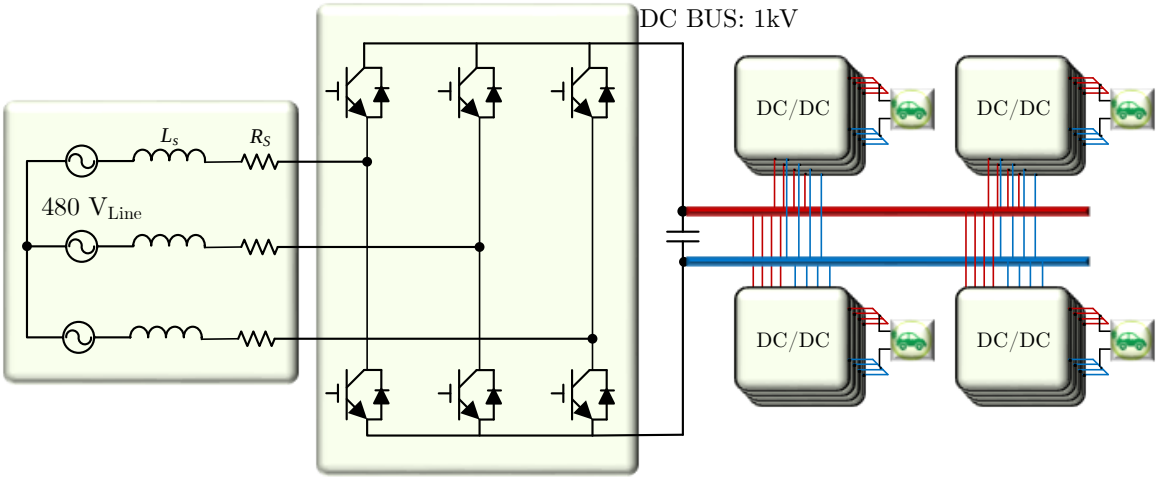


Figure 6.2 Circuit diagram of LV connected charging station

A. Requirements, and Design

The charging station must be able to draw pure active power from the grid, which means that the PF of the AC/DC stage must be close to 1, therefore, the AC/DC stage must act as a PFC as well. Moreover, the charging station must be able to provide reactive power compensation for grid regulating actions when it is required, which results in the requirement of reactive power control of the charging station.

Regarding power quality absorbed from the grid, according to IEEE Std 519-2014, the THD of the current drawn from the grid must be limited to 5 %, which is a baseline to design the line inductors connecting the PFC stage to the grid.

The DC-link voltage must be well regulated and provide a constant DC voltage to ensure the proper operation of the charging units. The maximum voltage ripple of the DC-link voltage is limited to 5-10 % of the DC-link voltage, which is the

baseline for DC-link capacitor sizing. The parameters and specifications of the AC/DC stage of the LV connected station are shown in Table 6.1.

TABLE 6.1 PARAMETERS OF THREE-PHASE PFC STAGE

	Actual Value	Per Unit Value
Rated Power	1.4 MW	1
Input Voltage	480 V	1
Line Reactor	180 µH	0.41
Line resistance	10 mΩ	0.061
DC-link Capacitance	2000 µF	0.12

As shown in Table 6.1, the base power of the station is 1.4 MW, while the base voltage is 480 V. Accordingly the base impedance of the three-phase PFC stage would be equal to 0.16 Ω. To have less than 5% THD at the rated condition the line inductors value are selected 180 µH (41%), and to have voltage ripple of 5-10 % across the DC-link capacitor, a 2000 µF capacitor is selected.

B. Control of the three-phase PFC stage

The main objectives that must be satisfied by the controller are DC-link voltage control and real/reactive power control. The controller for the LV connected station is developed considering the ac-side as a balanced three-phase ideal system, linear line inductors, and lossless ideal switching devices.

The ac source voltage is shown as V_{ga}, V_{gb}, and V_{gc} while R and L are the line reactor inductance and resistance. The grid three-phase currents are shown as I_{ga},

I_{gb}, I_{gc}, and load current is shown as I_L, while S_a, S_b, and S_c are the switching functions of each leg. Therefore, according to KVL, and KCL applied to the circuit diagram shown in Figure 6.2, the following equations can be obtained [108];

$$\begin{aligned} V_{ga} &= L\frac{dI_{ga}}{dt} + RI_{ga} + V_{dc}\left[S_a - \frac{1}{3}(S_a + S_b + S_c)\right] \\ V_{gb} &= L\frac{dI_{gb}}{dt} + RI_{gb} + V_{dc}\left[S_b - \frac{1}{3}(S_a + S_b + S_c)\right] \\ V_{gc} &= L\frac{dI_{gc}}{dt} + RI_{gc} + V_{dc}\left[S_c - \frac{1}{3}(S_a + S_b + S_c)\right] \\ C\frac{dV_{dc}}{dt} &= I_{ga}S_a + I_{gb}S_b + I_{gc}S_c - I_L \end{aligned} \tag{6.1}$$

To facilitate the control of real, and reactive power and DC-link voltage of the three-phase PFC, the mathematical model of the grid-connected AC/DC stage can be transferred from stationary a-b-c time frame to a synchronous rotating frame (dq frame) by using Park transformation, where I_{gd}, I_{gq}, V_{gd}, and V_{gq} are the d-q components of the grid current, and voltage respectively, and ω is the angular frequency of the grid voltage [109];

$$\begin{aligned} L\frac{dI_{gd}}{dt} - \omega LI_{gq} + RI_{gd} &= V_{gd} - V_{dc}S_d \\ L\frac{dI_{gq}}{dt} + \omega LI_{gd} + RI_{gq} &= V_{gq} - V_{dc}S_q \\ C\frac{dV_{dc}}{dt} &= \frac{3}{2}(I_{gd}S_d + I_{gq}S_q) - I_L \end{aligned} \tag{6.2}$$

The terms $V_{dc}S_d$, and $V_{dc}S_q$ can be written as V_d, and V_q respectively where represents the reference modulation waveforms.

The classic approach of regulating the DC-link voltage and controlling real/reactive power is Voltage-Oriented Control (VOC), which employs two control loops; a grid-side current inner loop for PF correction (two PI controllers) and a dc-side voltage outer loop (one PI controller). Moreover, an upgraded form of VOC is called dual-closed-loop control [110], where two feedforward terms are added to the controller in comparison to VOC.

The equations describing the dual-closed-loop control applied to (6.2) can be written as;

$$\begin{aligned} V_d &= -\left(K_{iP} + \frac{K_{iI}}{S}\right)(I_{gd}^* - I_{gd}) + \omega L I_{gq} + V_{gd} \\ V_q &= -\left(K_{iP} + \frac{K_{iI}}{S}\right)(I_{gq}^* - I_{gq}) - \omega L I_{gd} + V_{gq} \end{aligned} \tag{6.3}$$

$$\begin{aligned} I_{gd}^* &= \left(K_{vP} + \frac{K_{vL}}{S}\right)(V_{dc} - V_{dc}^*) \\ I_{gq}^* &= 0 \end{aligned} \tag{6.4}$$

where K_{iP}, K_{iI}, K_{vP}, and K_{vI} are the PI parameters of the current control and DC-link voltage control loops, and $I_{gd}{}^*$, and $I_{gq}{}^*$ are the grid d-q component reference current, where the latter is zero to force the reactive power drawn from the grid to zero, and the former is the output of the DC-link voltage control. The block diagram of the developed controller is shown in Figure 6.3.

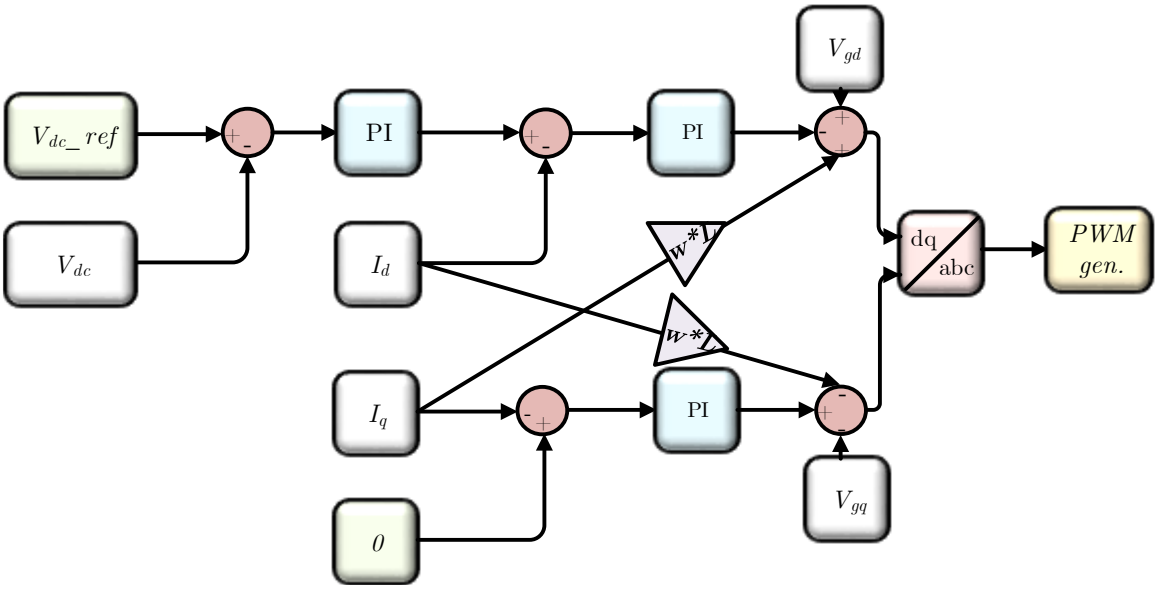


Figure 6.3 Block diagram of LV connected charging station controller

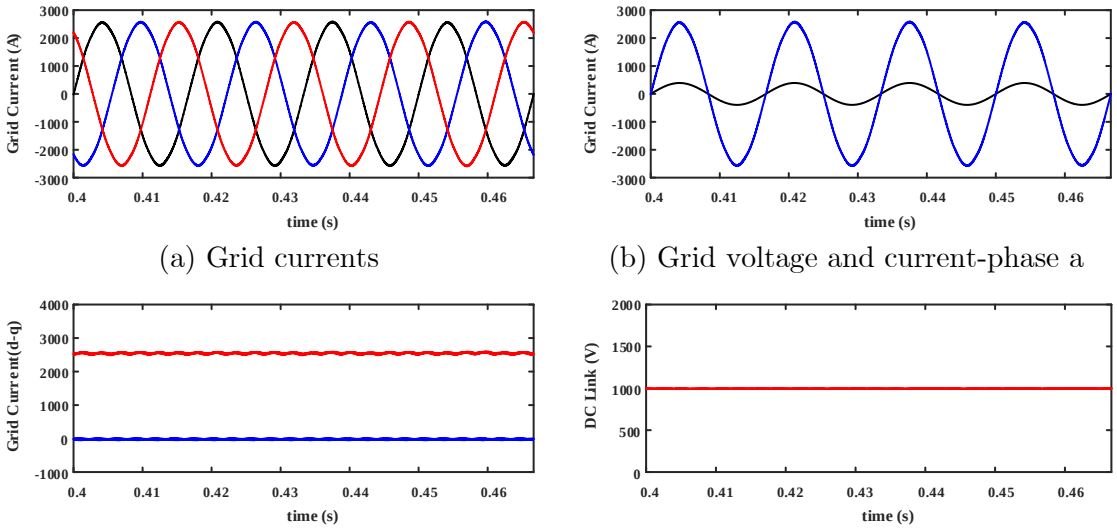
The generated modulation waveforms from the developed controller are then passed to the SPWM block to generate the gating for the active devices.

6.2.2 Simulation Studies, Efficiency, and Power Quality

In this section, simulation studies have been done in MATLAB/Simulink environment to investigate the performance of the three-phase PFC as the AC/DC stage of the EV charging station shown in Figure 6.1. The developed controller shown in Figure 6.3 is applied to the AC/DC stage to control the DC-link voltage at 1 kV and keep the PF close to one.

A. Simulation Results

Since the charging station must be able to regulate the DC-link voltage, and power factor in different power loads, the simulation results are shown in Figure 6.4, and Figure 6.5 for 1.4 MVA, and 150 kW.



(a) Grid currents

(b) Grid voltage and current-phase a

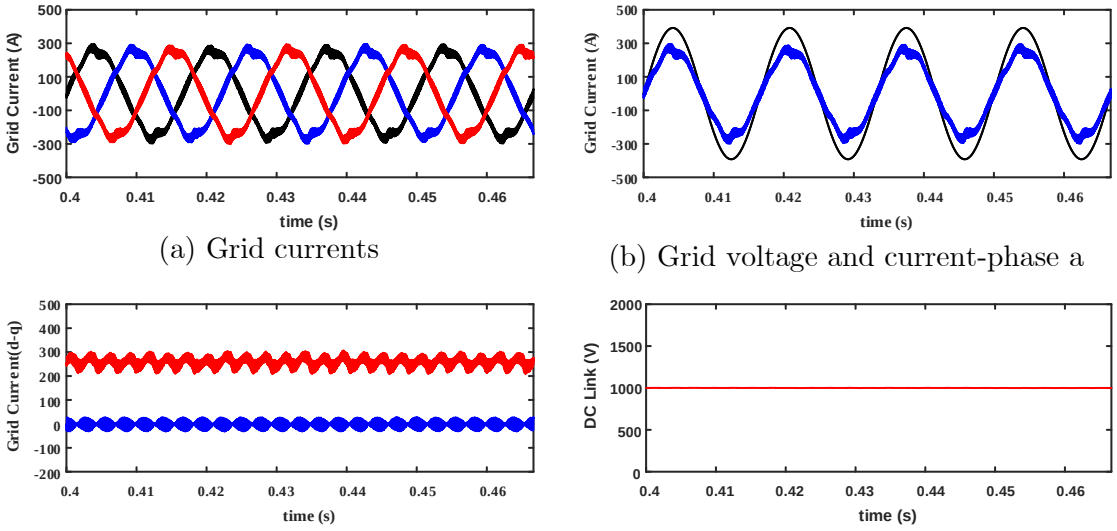
(c) d-q components of the grid current

(c) DC-link voltage

Figure 6.4 AC/DC stage of the LV-connected station at 1.4 MW

As shown in Figure 6.4 (a), the current supplied from the grid is a three-phase balance current, which has a THD less than 5% that complies with the grid connection THD requirement. Figure 6.4 (b) shows phase-a of the grid voltage, and current, which demonstrate that the PF is kept close to one, while Figure 6.4 (c) shows the d-q components of the grid current that confirms the ability of the controller to control the d-q components of the grid current at the desired levels.

Moreover, Figure 6.4 (d) shows the DC-link voltage that is well balanced at 1 kV that is the station predefined voltage.



(a) Grid currents

(b) Grid voltage and current-phase a

(b) d-q components of the grid current

(d) DC-link voltage

Figure 6.5 AC/DC stage of the LV-connected station at 150 kW

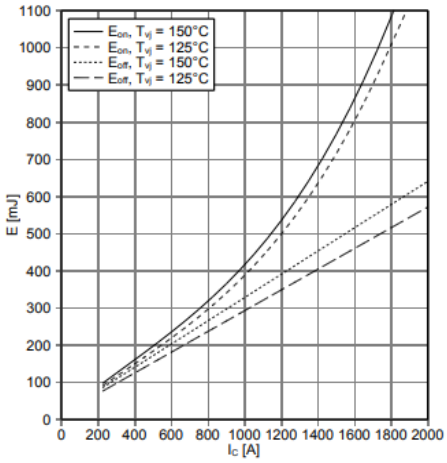
The same explanation applies to the results shown in Figure 6.5. As can be seen, the controller objectives are satisfied, however, the THD of grid current is increased, which is due to the operation of the converter in lower power levels. The study on the grid power quality is given in the next section.

B. Efficiency and Power Quality

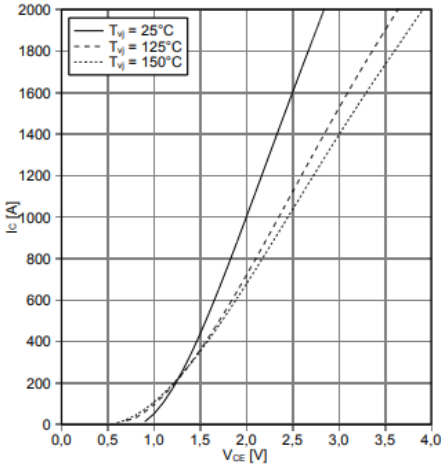
In this section, the efficiency of the three-phase AC/DC PFC stage and the power quality drawn by the AC/DC stage are investigated for different load powers.

The efficiency of the three-phase PFC is calculated by simulation studies using PLECS blockset in MATLAB/Simulink environment. The IGBT considered for the

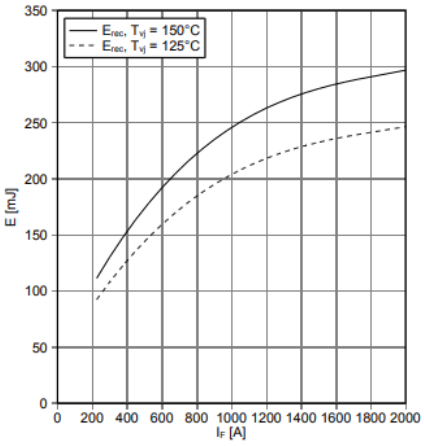
three-phase PFC is FF1000R17IE4 from Infineon, where for each upper and bottom leg three devices are paralleled, the reason behind this selection is explained in the next section. The losses considered for efficiency calculation are line inductor losses, IGBT losses including switching and conduction losses of IGBTs.



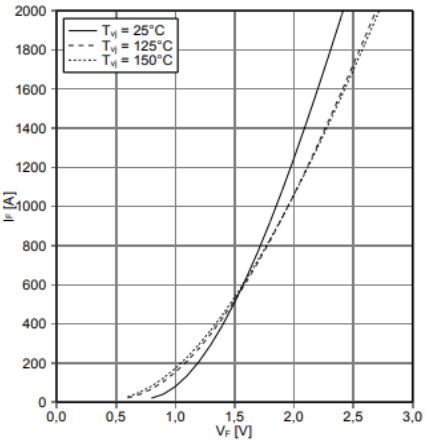
(a) IGBT switching energy loss



(b) IGBT output characteristics



(c) Diode reverse recovery energy loss



(c) Diode forward characteristics

Figure 6.6 FF1000R17IE4 datasheet information [111]

The power losses are calculated through the PLECS blockset, and by the thermal description of the PLECS simulation tool that uses the information in the IGBT datasheet. The thermal description is developed for the FF1000R17IE4 based on the information shown in Figure 6.6.

The IGBT switching losses are calculated using the IGBT switching ON and OFF energy losses provided in the datasheet as shown in Figure 6.6 (a). PLECS blockset uses this graph as a look-up table where the input is the IGBT current, voltage, and junction temperature, while the output is the energy losses at the current IGBT operating point. Then the extracted energy losses are averaged through a user-defined time frame to obtain the switching power losses. The same approach is applied to calculate the diode reverse recovery power loss using the graph shown in Figure 6.6 (c).

The IGBT conduction loss is calculated from the IGBT output characteristics as shown in Figure 6.6 (b), where the IGBT collector current versus collector-emitter voltage is shown. This graph is also used as a look-up table, where the input is the IGBT current, and the output is the IGBT on-state voltage. Then by multiplication of the IGBT current, and diode and integrating the result over a user-defined time frame, the conduction power loss is calculated at the desired interval. The same approach can be used to calculate the diode conduction losses.

The THD of the grid current is determined in MATLAB/Simulink environment for different power ratings. The calculated efficiency and the grid current THD are shown in Table 6.2 for different load power from the rated power of the station to 150 kW load power.

TABLE 6.2 EFFICIENCY, AND POWER QUALITY OF THE THREE-PHASE PFC CONVERTER

Power	Efficiency	THD
1400 kW	92.2 %	4.12 %
1050 kW	93.9 %	5.75 %
700 kW	95.5 %	8.76 %
350 kW	97 %	16.92 %
150 kW	97.3 %	38.8 %

As can be seen, the efficiency at rated power is 92.2 %, and the THD of the line current is 4.12 % to comply with the grid standard. As the load power decreases, the efficiency, and the grid current THD increase. The increase in efficiency demonstrates the fact that the dominant inverter loss is associated with the conduction losses. Needless to say that increasing the source voltage can improve the efficiency significantly as shown in the next sections of this chapter. Moreover, the high grid current THD shows an opportunity to use multilevel inverters that can improve the THD significantly.

6.2.3 Cost Analysis

In this section, the costs of the components, and devices required to design a 1.4 MVA three-phase PFC as the AC/DC stage of the LV connected charging station are determined. The cost estimation in this section is solely for the comparison between different cases studied in this chapter. Therefore, it cannot be treated as the actual manufacturing cost of the three-phase PFC, since estimating the actual manufacturing cost is a challenging task and extensive details must be considered in the process. Moreover, it is tried to select the components that have a minimum cost to reach a fair comparison. The components considered for the cost estimation are the IGBT devices, gate drivers, capacitors, and transformer.

Regarding the IGBT devices, since the DC-link voltage is regulated at 1 kV, the voltage stress on each IGBT is equal to 1000 V, therefore a 1700V IGBT must be used as the active switch of the three-phase PFC to ensure that the voltage and current spikes do not damage the devices. The rated power of the station is 1.4 MVA, and the grid voltage is 480 V, therefore the rated line current that flows into the IGBT switches is equal to 1680 A. The IGBT current rating must be double the aforementioned value. Therefore, three FF1000R17IE4D IGBT module is considered for each leg, which means three IGBT would be paralleled to handle the maximum current rating of the IGBT. The selected IGBT is a 1700 V IGBT class

with a maximum current rating of 1000 A. The gate driver considered is 2SP0320V2A0 from Power Integration.

Moreover, a 1.4 MVA line transformer is required to convert 4160 V grid voltage to 480 V. A quote from Maddox Industrial Transformer was obtained, which specified the cost of a 1500 MVA 4160/480 V transformer around $37,000.

Therefore, the total cost of the considered three-phase PFC converter is estimated at around $48,000. As predicted, the major cost of such an AC/DC stage for the LV-connected charging station is related to the line transformer, which is one of the main reasons to move toward MV-connected charging stations.

6.3 LV Connected Charging Station with Four-Level T-Type NNPC as the AC/DC Stage

The conventional three-phase PFC performance was investigated as the AC/DC stage of an LV-connected charging station in the previous section. The results of the study show that the three-phase PFC suffers from relatively low efficiency, high cost, and low power quality. Moreover, it was shown that despite employing large line inductors (41% per unit) the THD of the grid currents increases significantly with the decrease of load power.

The aforementioned challenges of the three-phase PFC flash an opportunity for the advanced multilevel topologies as the AC/DC stage of a charging stage due to

its advantages such as lower device voltage stress (lower device loss), higher power quality, etc... In this section, the four-level T-type NNPC performance is studied as the AC/DC stage of the LV connected station shown in Figure 6.1 to investigate its possible advantages over the three-phase PFC.

6.3.1 Operation, and Control

The circuit diagram of the four-level T-type NNPC as the AC/DC stage of an LV-connected charging station is shown in Figure 6.7.

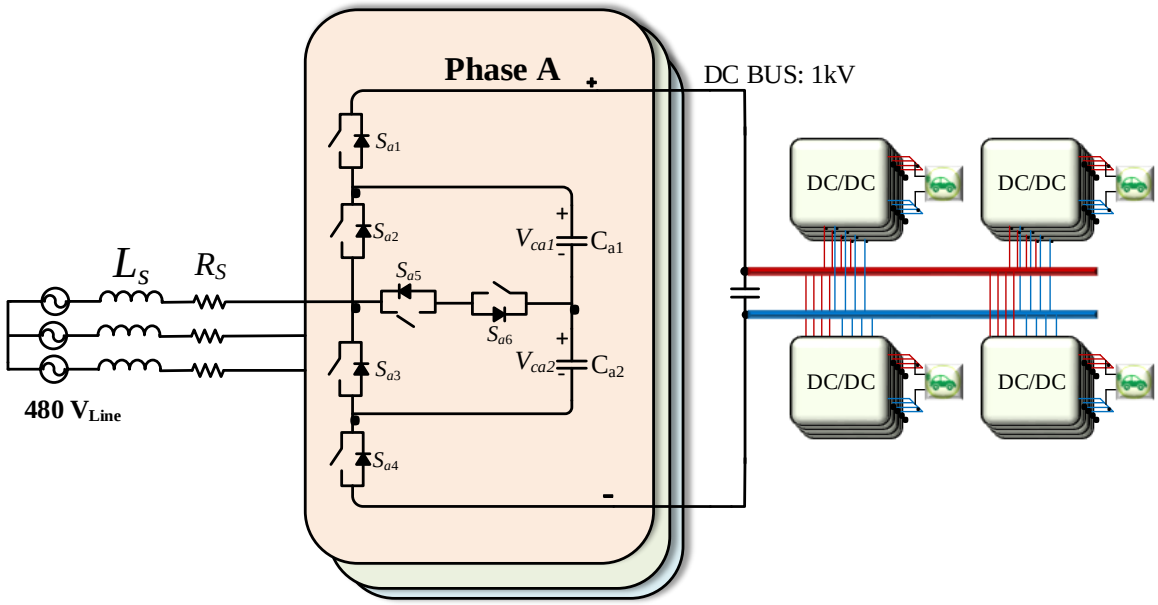


Figure 6.7 Circuit diagram of the four-level T-type NNPC as the AC/DC stage of the LV connected charging station

The charging station specification is the same as the previous section to enable a fair comparison, where the rated power of the station is 1.4 MVA that feeds four

charging units with 350 kW maximum power capability. The grid voltage is 480 V, which is connected to the four-level T-type NNPC through line inductors. As discussed previously, since the battery voltage of different electric vehicles is in the range of 200-900 V DC, the DC-link is considered to be equal to 1 kV to facilitate the design of charging units DC/DC converter.

A. Requirements, and Design

The requirements for the four-level T-type NNPC as the AC/DC stage of the charging station are similar to the requirements of the three-phase boost PFC discussed in the previous section. The four-level T-type NNPC must regulate the DC-link voltage at 1 kV while balancing its flying capacitors and keeping the power factor close to 1. The parameters and specifications of the AC/DC stage of the LV connected station are shown in Table 6.3.

TABLE 6.3 FOUR-LEVEL T-TYPE NNPC PARAMETERS

	Actual Value	**Per Unit Value**
Rated Power	1.4 MW	1
Input Voltage	480 V	1
Line Reactor	75 µH	0.17
Line resistance	10 m**Ω**	0.061
DC-link Capacitance	2000 µF	0.12
Flying Capacitor	100 mF	6.12

Similarly, the line inductors are sized according to IEEE Std 519-2014, where the THD of the line currents must be limited to 5%, and the DC-link and flying capacitors are sized to limit their voltage ripple to 5-10 % of the DC-link voltage and the desired flying capacitor voltages.

As can be seen, the line inductors are 75 µH to limit the line current THD, which is equal to 17 % per unit. The line inductor for the connection of the grid to the AC/DC stage is 58% less than the line inductor required for the conventional three-phase PFC converter, which demonstrates the advantage of using multi-level topologies in terms of power quality. Moreover, the DC-link capacitor has the same value for both converters, since the load power and currents are similar in both cases. A more detailed comparison between the four-level T-type NNPC and the conventional three-phase PFC converter is given at the end of this section in terms of efficiency, power quality, and cost.

B. Control of the Four-Level T-type NNPC

The control of the four-level T-type NNPC is a bit different with the three-phase PFC converter as the AC/DC stage of the LV connected station. In addition to control the DC-link voltage and real/reactive power, the flying capacitors of the four-level T-type NNPC must be balanced at one-third of the DC-link voltage (1000 V/3= 333 V). However, the flying capacitor control can be implemented at the

modulation level, while DC-link voltage and real/reactive power control are implemented outside the modulation scheme.

Similar to the discussion regarding the control of the conventional three-phase PFC converter, the four-level T-type NNPC control is based on the dual-closed-loop method; where a PI controller is used for the DC-link voltage control, and two PI controller are used to adjust the d-q components of the grid current. The generated modulation waveforms from the dual-closed-loop control are passed to the modulation scheme, where the gating for the IGBTs is generated based on SPWM to control the flying capacitor voltages as explained in Section 4.4.

The block diagram of the developed controller for the four-level T-type NNPC converter as the AC/DC stage of the LV connected station is shown in Figure 6.8. The ac source voltage d-q components are shown as V_{gd}, and V_{gq}, while R and L are the line reactor inductance and resistance. The d-q components of the grid currents are shown as I_{gd}, and $I_{gd,}$ while the DC-voltage, and DC-voltage references are shown as V_{dc}, and V_{dc_ref} respectively.

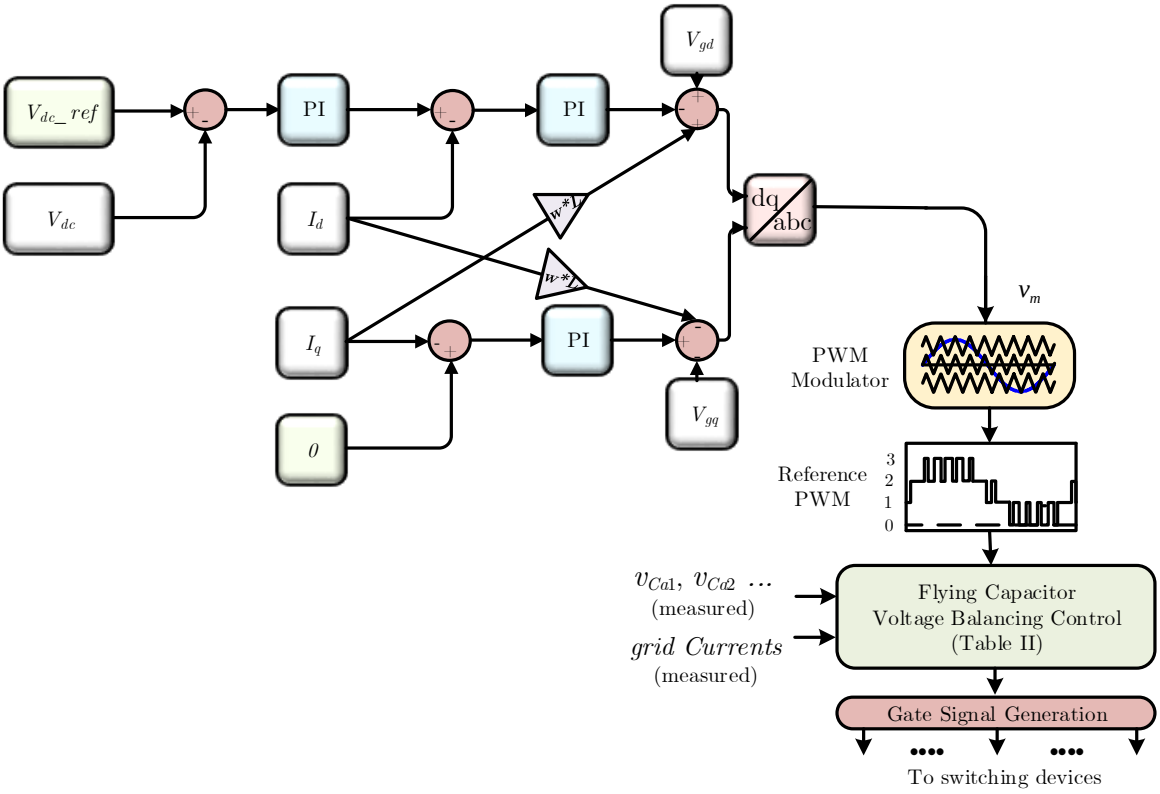


Figure 6.8 Block diagram of the developed controller for the four-level T-type NNPC

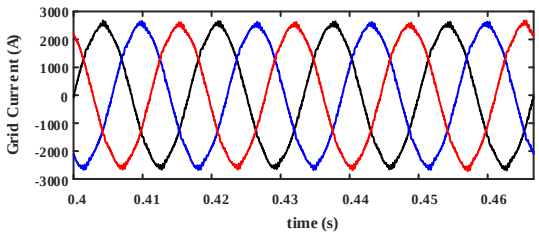
6.3.2 Simulation Studies, Efficiency, and Power Quality

In this section, simulation studies have been done in MATLAB/Simulink environment to investigate the performance of the four-level T-type NNPC as the AC/DC stage of the EV charging station shown in Figure 6.7. The developed controller shown in Figure 6.8 is applied to the AC/DC stage to control the DC-link voltage at 1 kV, flying capacitors at 333 V, and keep the PF close to one.

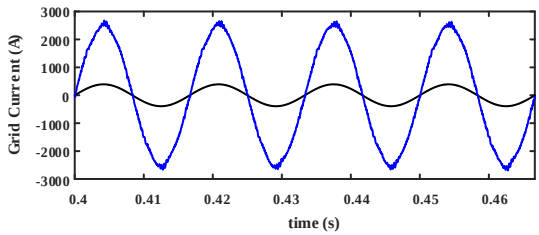
A. Simulation Results

Since the charging station must be able to regulate the DC-link voltage, and power factor in different power loads, the simulation results are shown in Figure 6.9, and Figure 6.10 for 1.4 MVA and 150 kW to demonstrate the effectiveness of the developed controller in different load powers.

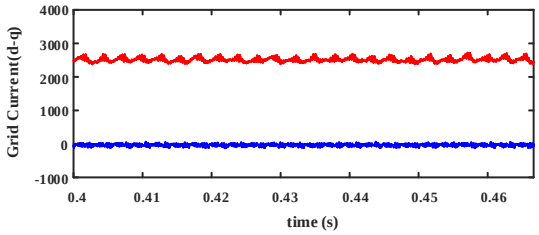
As shown in Figure 6.9 (a), the current supplied from the grid is a three-phase balance current, which has a THD less than 5% that complies with the grid connection THD requirement. Figure 6.9 (b) shows phase-a of the grid voltage, and current, which demonstrate that the PF is kept close to one, while Figure 6.9 (c) shows the d-q components of the grid current that confirms the ability of the controller to control the d-q components of the grid current at the desired levels. Figure 6.9 (d) shows the DC-link voltage that is well balanced at 1 kV that is the station predefined voltage. Moreover, Figure 6.9 (e) shows the flying capacitor voltages of the four-level T-type NNPC, as can be seen, the capacitor voltages are well regulated at the desired voltage level, which is one-third of the DC-link voltage (333 V).



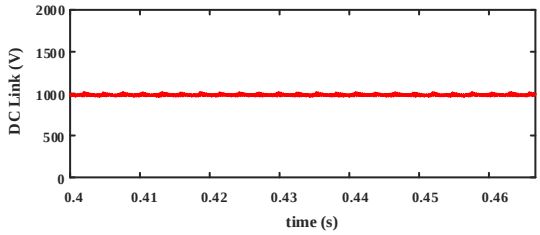
(a) Grid currents



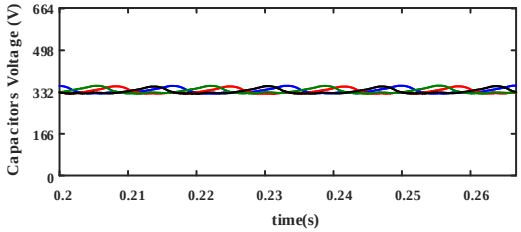
(b) Grid voltage and current-phase a



(c) d-q components of the grid current



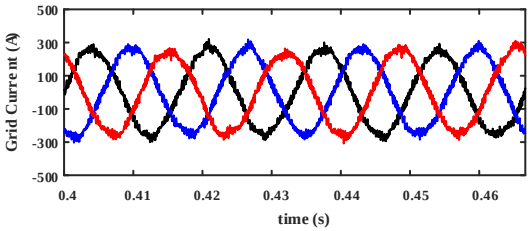
(c) DC-link voltage



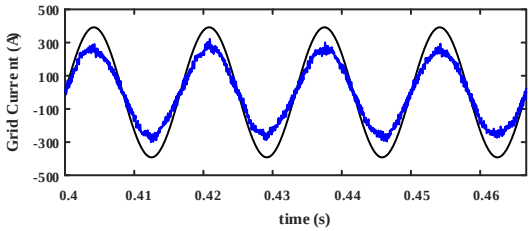
(e) Flying capacitors voltages

Figure 6.9 AC/DC stage of the LV connected station at 1.4 MW

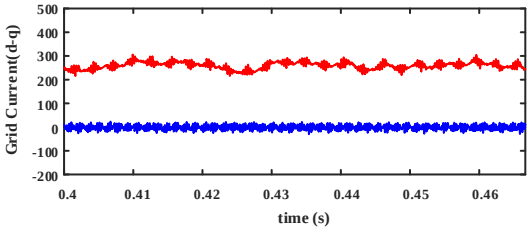
As can be seen, the controller objectives are satisfied, however, the THD of grid current is increased, which is due to the operation of the converter in lower power levels. It is worth noting that the voltage ripple across the DC-link and flying capacitors in Figure 6.10 are reduced in comparison to Figure 6.9 due to low current operation. The study on the grid supply power quality is given in the next section.



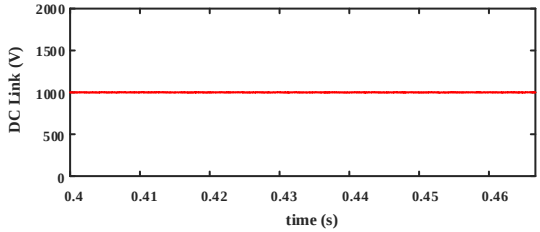
(a) Grid currents



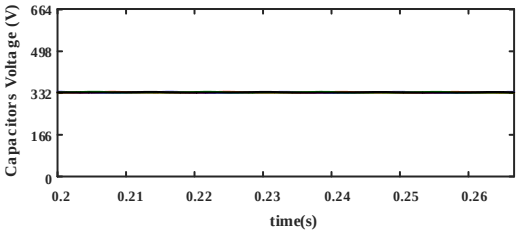
(b) Grid voltage and current-phase a



(b) d-q components of the grid current



(d) DC-link voltage



(e) Flying capacitors voltages

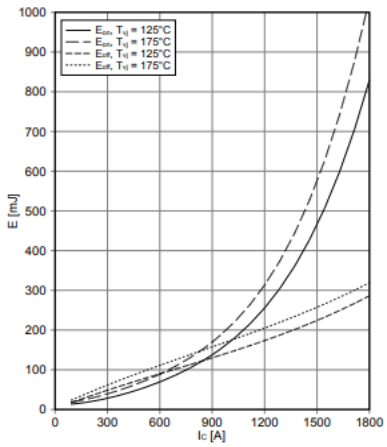
Figure 6.10 AC/DC stage of the LV connected station at 150 kW

B. Efficiency, and Power Quality

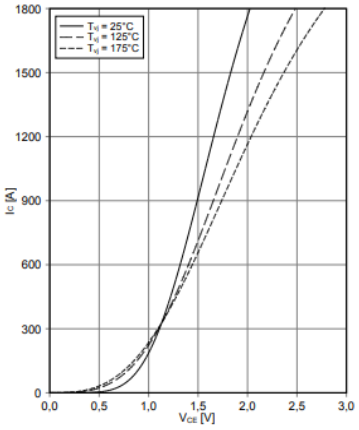
In this section, the efficiency, and power quality of the four-level T-type NNPC as the AC/DC stage of a 1.4 MVA LV connected charging station are investigated for different load powers. A similar approach described in Section 6.2.2 B is employed to calculate the efficiency of the four-level T-type NNPC in PLECS software.

As discussed earlier, the main power losses are the conduction loss, switching loss, and reverse recovery loss for the IGBTs and their antiparallel diodes. The

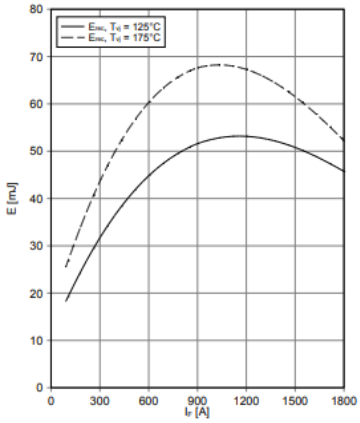
IGBT module considered for the 1.4 MVA four-level T-type NNPC is FF900R12ME7. The power losses are calculated based on the IGBT datasheet information as shown in Figure 6.11.



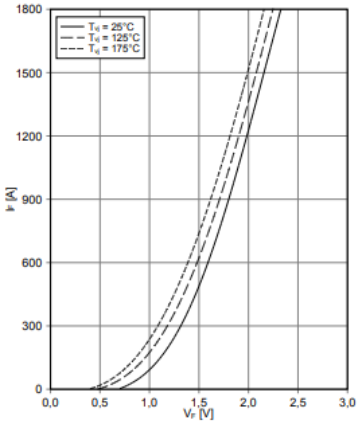
(a) IGBT switching energy loss



(b) IGBT output characteristics-



(c) Diode reverse recovery energy loss



(c) Diode forward characteristics

Figure 6.11 FF900R12ME7 datasheet information

Due to the lower IGBT voltage stress in the four-level T-type NNPC, a 1200V class IGBT is used, a comparison between Figure 6.11, and Figure 6.6 demonstrates the fact that the devices selected for the four-level T-type NNPC are superior to

the 1700 V IGBT class selected for the conventional three-phase PFC in terms of switching and conduction losses.

The efficiency, and grid current THD of the four-level T-type NNPC for different power loads are shown in Table 6.4. Similar to the conventional three-phase PFC, the efficiency of the four-level T-type NNPC is reduced with the increase of the load power, which demonstrates the fact that the conduction losses are dominant in comparison to switching losses of the converter. On the other hand, the THD of the grid current is increased with the decrease of the load power, however, the overall power quality is increased significantly with lower line reactance compare to the conventional three-phase PFC. A comparison between the four-level T-type NNPC and the conventional three-phase PFC has been done later in this chapter.

TABLE 6.4 FOUR-LEVEL T-TYPE NNPC EFFICIENCY AND POWER QUALITY

Power	Efficiency	THD
1400 kW	91.5 %	4.3 %
1050 kW	93.5 %	4.72 %
700 kW	95.2 %	5.77 %
350 kW	96.8 %	10.79 %
150 kW	97 %	23.84 %

6.3.3 Cost Analysis

In this section, the costs of the components, and devices required to design a 1.4 MVA three-phase four-level T-type NNPC as the AC/DC stage of the LV-connected charging station are determined. Similar to Section6.2.3, the components considered for the cost estimation are the IGBT devices, gate drivers, capacitors, and the line transformer.

As discussed in 6.2.3, the rated current of the charging station is 1680 A, and the IGBT device must be almost rated twice this value. On the other hand, the maximum voltage stress on each IGBT, due to the advantages of the four-level T-type NNPC, is two-third of the DC-link voltage, which would be equal to 666 V. Therefore, a 1200 V class IGBT can be selected.

It is found that the cost of three-parallel IGBT per switch for the four-level T-type NNPC results in the lower final cost. Therefore, 27 IGBT FF900R12ME7 from Infineon must be used to handle the rated power of the charging station. The cost of the IGBT module will be around $10,280. The 2SP0115T2A0 gate driver from Power Integration can be used to drive the IGBT modules which results in a total cost of $3,860.

The cost of the line transformer is the same as the three-phase PFC case and is around $37,000 for a 1.5 MVA 4.16 kV/480V transformer. Moreover, the cost of

the capacitor bank for the flying capacitors of the four-level T-type NNPC topology is estimated to be $7200. Therefore, the total cost of the 1.4 MVA is estimated to be around $58300.

6.3.4 Four-Level T-type NNPC VS Conventional Three-Phase PFC

In this section, the four-level T-type NNPC is compared to the conventional three-phase PFC converter in terms of efficiency, power quality, and cost as the AC/DC stage of the charging station. The efficiency and grid current THD, cost, and line reactance size for the four-level T-type NNPC, and the three-phase PFC are shown in Table 6.5.

TABLE 6.5 FOUR-LEVEL T-TYPE NNPC VS THREE-PHASE PFC

	Efficiency at 1.4 MW	**Efficiency at 150 kW**	**THD at 1.4 MW**	**THD at 150 kW**	**Line Inductance**	**Cost**
Four-level T-type NNPC	91.5 %	97 %	4.3 %	23.84 %	17 %	$58,300
Conventional three-phase PFC	92.2 %	97.3 %	4.12 %	38.8 %	41 %	$48,000

The efficiency and grid current are shown for rated and low load powers to compare the extreme cases of efficiency and power quality.

As can be seen, the efficiency of the three-phase PFC is slightly higher even though lower voltage class IGBT is considered for the four-level T-type NNPC, where it has lower conduction and switching losses. However, due to the higher

number of IGBTs in the four-level T-type NNPC topology, the total loss is slightly higher. This observation demonstrates the fact that the advantages of the four-level topology in terms of efficiency could be achieved in a lower current rating.

Regarding the grid current THD, it is shown that the THD for the four-level T-type NNPC is increased from 4 to 23 % with the decrease in the load power, however, for the three-phase PFC, the THD is increased from 4 % to 38 %. This demonstrates the advantage of generating multilevel voltage by the four-level T-type NNPC. Not only the grid current is improved with the use of four-level T-type NNPC, but also lower line inductance (17 % per unit) is used in comparison to the three-phase PFC converter (41 % per unit).

Regarding the cost of both converters, the four-level T-type NNPC is more expensive. The difference in the cost of the line inductance is not considered, however, it can be estimated around 500$ considering the cost of high and low impedance line inductors with high current rating is around $3800-$4300 [112], which does not affect the cost comparison significantly. The main reason that leads to the costly four-level T-type NNPC is the large capacitor banks required for the flying capacitors to achieve the required capacitance, which is due to the high current rating of the charging station that leads to higher voltage ripple across the capacitor.

Therefore, in this case, the four-level T-type is superior to the three-phase PFC in terms of power quality, and line inductance sizing, however, suffers from slightly lower efficiency and higher cost. As discussed, the main challenges for the efficiency and cost are the high current rating of the charging station, which leads to the use of parallel devices and large capacitor banks for the four-level topology. As shown in the next section, moving toward MV connected charging station that decreases the current rating of the charging station overcomes these challenges.

6.4 A New Architecture for MV-Connected Ultra-Fast EV Charging Station

The studies in the previous sections suggest that the LV-connected ultra-fast EV charging stations with common DC-bus suffer from low efficiency, low power quality, and high cost which are the result of the high current rating of the station, and the line frequency transformer. As discussed in Chapter 2, MV-connected charging stations are superior to LV-connected stations in terms of efficiency, cost, and power density due to the connection to the MV-grid, and eliminating the line frequency transformer. The former decreases the current required to deliver the same amount of power, and the latter maximizes the power density while decreasing the cost.

Moreover, as explained in Chapters 3 to 5, the advanced multilevel topologies are excellent choices for MV grid connection due to the lower device voltage stress, higher power quality, and higher efficiency. It was shown that the higher the number of voltage levels, the better the power quality with a trade-off between cost and efficiency.

Based on these analyses, an MV-connected ultra-fast EV charging station architecture, based on the proposed seven-level topology in Chapter 5 is proposed in this section and shown in Figure 6.12.

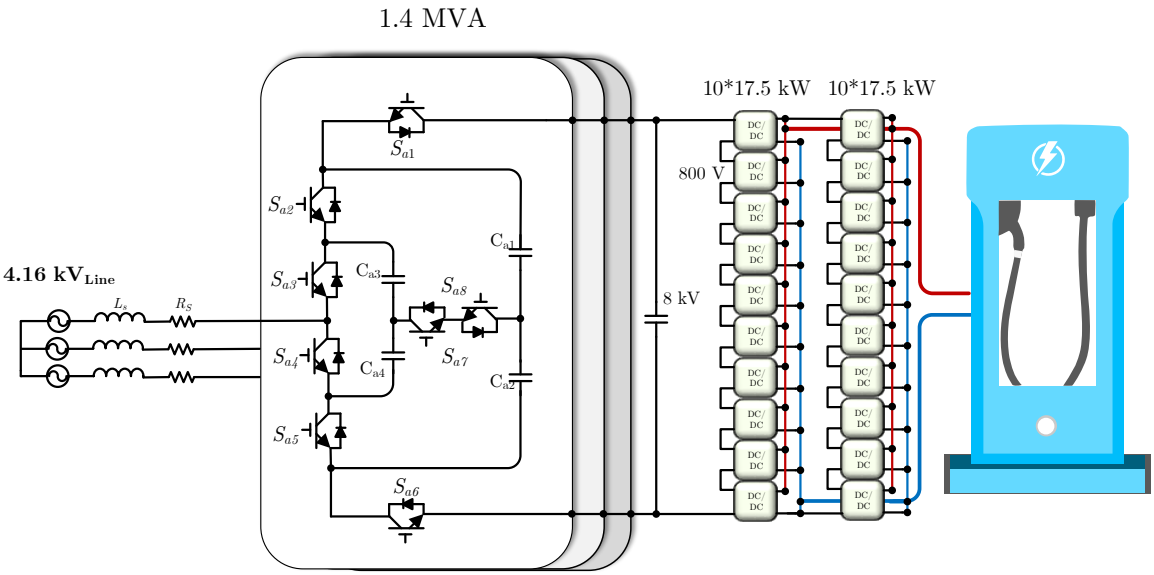


Figure 6.12 Proposed MV connected ultra-fast EV charging station architecture

The layout of the charging station is shown in Figure 6.12, where a 1.4 MVA charging station connected directly to MV grid (4.16 kV) delivers power to four charging units with maximum 350 kW power rating. The proposed charging station

architecture employs the seven-level topology as the AC/DC stage, and a network of DC-DC converters connected to the medium voltage DC-link as the charging units.

The proposed charging station has a fewer number of conversion stages and fewer components in comparison to the existing solid-state-transformer-based charging stations, where two stages of DC conversion are required for providing regulated DC-link, and delivering power to the EVs connected to the station. On the other hand, as shown in Chapter 5, the seven-level topology has a fewer number of components in comparison to the other seven-level topologies such as CHB, which is used in the AC/DC stage of most of the existing charging stations architecture in the literature.

The operation and control of the proposed topology are explained in Section 6.4.1. The efficiency, power quality, and cost of the proposed architecture are investigated in Section Error! Reference source not found., and 6.4.3 respectively. Finally, the proposed topology is compared to the LV-connected architectures studied in the previous sections in terms of efficiency, cost, and power quality.

6.4.1 Operation, and Control

As shown in Figure 6.12, the seven-level topology, connected to the MV grid (4.16 kV) acts as the AC/DC stage of the proposed MV-connected charging station to regulate the DC-link voltage at 8 kV. The main challenge of the connection of the seven-level topology to the MV grid is the obligation of having an MV DC-link at the output of the AC/DC stage.

As it was discussed in Chapter 2, the EV charger must be isolated from the grid for safety purposes, therefore, an isolated DC/DC converter must be used. There are two approaches to deal with the regulated MV, first is to include an isolated DC/DC stage where the MV DC-link is converted to the LV DC-link, then the DC/DC converters of the charging units deliver the power to the EV batteries. The challenge of this approach is the design of such a high-power DC/DC converter where the voltage gain is significantly high and results in affecting cost, efficiency, and power density.

The other approach considered in this chapter is the series input, paralleled output branches of isolated DC/DC converters to interface between the MV DC-link and the EV battery terminals. As shown in Figure 6.12, 10 series DC/DC converter is considered to deal with the 8 kV DC-link voltage, and two branches are paralleled, where each is responsible for delivering 175 kW to the EV terminals.

The DC-link voltage, number of series DC/DC converter, and parallel branches can be optimized to find the optimal pattern in terms of cost, efficiency, and power density, which is not in the scope of this work and can be considered as the future steps.

A. Requirements, and Design

The requirements of the seven-level topology as the AC/DC stage of the 1.4 MVA charging station is similar to the requirements described in Sections 6.2.1 and 6.3.1, where the DC-link must be regulated at the desired value (8 kV), the power factor must be kept close to 1, the flying capacitor voltage ripple must be limited to 5-10 % of the voltages of the flying capacitors, and the grid current THD must be limited to 5 % according to IEEE Std 519-2014. Based on these requirements, the parameters of the system are selected, and shown in Table 6.6.

TABLE 6.6 SEVEN-LEVEL TOPOLOGY PARAMETERS

	Actual Value	**Per Unit Value**
Rated Power	1.4 MVA	1
Input Voltage	4.16 kV	1
Line Reactor	5 mH	0.15
Line resistance	100 mΩ	0.01
DC-link Capacitance	200 µF	0.93
Flying Capacitor	250 µF	1.16

Two important advantages of the seven-level topology as the AC/DC stage of the MV connected charging station in comparison to the conventional three-phase PFC and four-level T-type NNPC are regarding the line reactor and flying capacitors. As can be seen, the line reactor is reduced 63%, and 11% in comparison to the three-phase PFC, and four-level T-type NNPC respectively. On the other hand, the capacitance of the flying capacitor is reduced by 83% in comparison to the four-level T-type NNPC due to the lower current rating of the station. A more detailed comparison is given at the end of this chapter.

B. MPC based control of the seven-level topology

The control objectives of the seven-level topology as the AC/DC stage of the charging station are; balancing the flying capacitor voltages, regulating the DC-link voltage, and real/reactive power control to keep the power factor close to 1. As discussed in chapter 5, the SVM-based controller is not able to regulate the flying capacitor voltages of the seven-level topology at high power factors, therefore, the MPC-based controller developed in Section 5.4 is applied to the seven-level topology.

The developed MPC controller in Section 5.4 is for the DC/AC conversion mode of the seven-level topology. The AC/DC mode is similar, however, small changes

are required. Since the seven-level topology is connected to the grid, the phase voltage equation must include the grid voltage (different from Equation (5.9));

$$V_{xN} = Ri_x + L\frac{di_x}{dt} + V_{gx} + V_{nN} \tag{6.5}$$

where; $x = a,\ b,\ c,$ and V_{gx} is the grid voltage, V_{xN} is the phase voltage of the converter with respect to the negative dc-link voltage (N). i_x is the grid current, R and L are line reactor, V_{nN} is the common-mode voltage according to Figure 6.13. Therefore, the predicted current (equation (5.12)) is rewritten as follow;

$$i_x(k+1) = \frac{T_s}{L+RT_s}V_{xn}(k+1) + \frac{L}{L+RT_s}i_x(k) - \frac{T_s}{L+RT_s}V_{gx}(k) \tag{6.6}$$

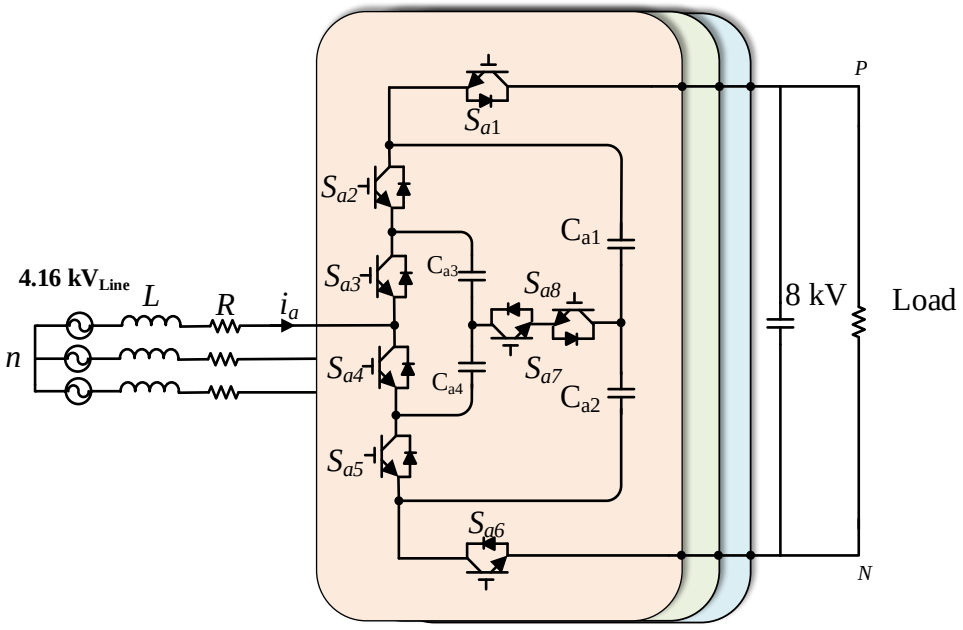


Figure 6.13 Seven-level topology, AC/DC conversion mode

The rest of the controller is identical to the developed MPC in Section 5.4. To control the DC-link voltage, and the PF, only one PI regulator is required as shown in Figure 6.14, the output of the PI controller is the d-component of the grid reference current, while the q-component is zero to ensure that the PF is close to 1. Then the produced d-q components of the grid current reference are transformed to abc frame and passed to the MPC controller. Then the predicted current from Equation (6.6), and the reference current are used in the cost function alongside the capacitor voltage to determine the best switching state that minimizes the error between the predicted control objectives.

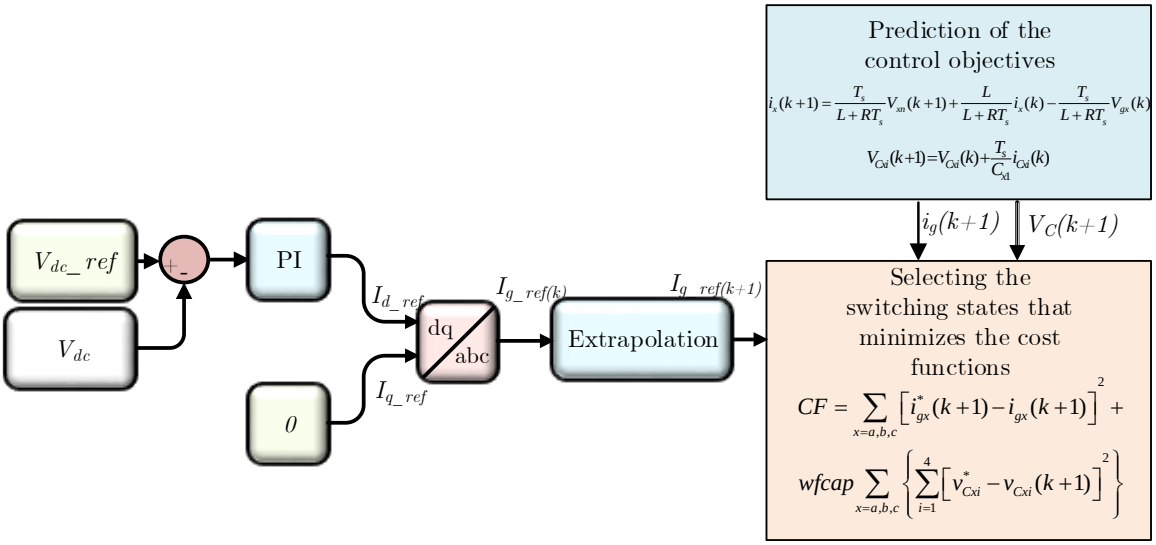


Figure 6.14 Seven-level topology MPC based developed controller block diagram for AC/DC conversion mode

C. Computational efficient sequential MPC for the seven-level topology

As discussed previously, one of the major disadvantages of the MPC-based control for the seven-level topology is the high computational burden due to the high number of switching states. This issue was addressed in Section 5.4.2, where an approximation in a common-mode voltage equation decouples the control of the three-phase and reduces the computational burden significantly.

Another disadvantage of MPC-based controllers is the manual tuning of the weighting factor of the cost function, which determines the priority of the objectives. The weighting factor must be tuned manually for multiple operating points to results in the proper performance of the inverter, which is a challenging task.

In [113], a sequential MPC strategy is proposed, where the weighting factor is eliminated by cascading the cost functions. A cost function with two control objectives is divided into two separate cascaded cost functions, then n-number of switching states that minimizes the first cost function is selected and passed to the other cost function, where among the selected vectors, the one that minimizes the second cost function is applied to the converter.

In this section, a computational efficient sequential MPC strategy is proposed, where not only the computational burden is decreased but also the weighting factor

is eliminated through cascading the cost function. The block diagram of the proposed strategy is shown in Figure 6.15.

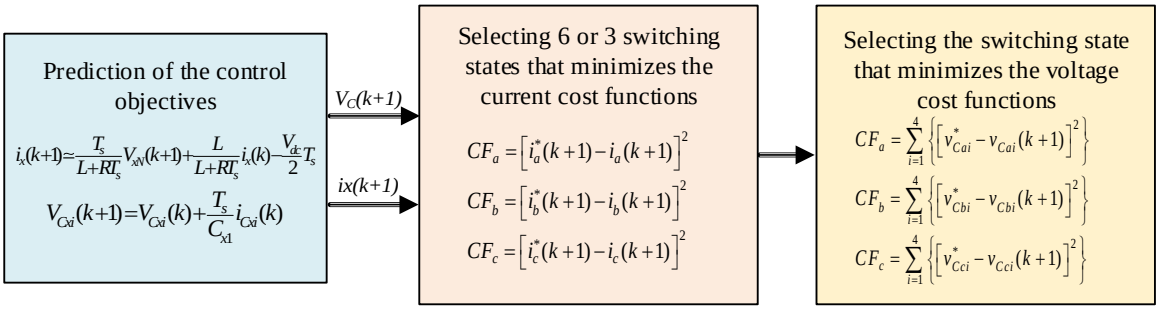
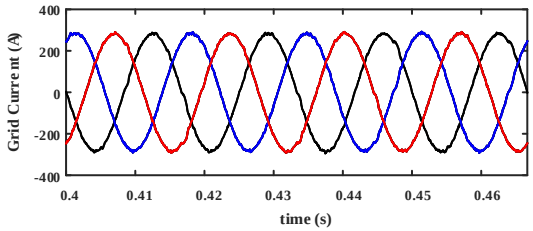


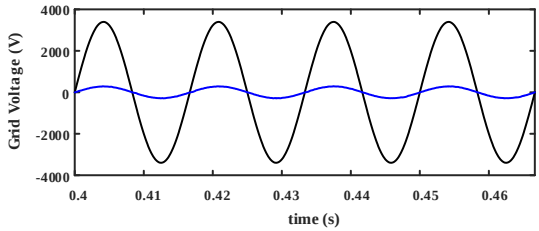
Figure 6.15 Proposed Computational efficient sequential MPC strategy

As can be seen, first the three-phase cost function is decoupled to three separate cost functions for each phase through the approximation in the common-mode voltage calculation that reduces the number of calculations significantly. Then, the cost functions are divided into cascaded current and voltage cost functions. First, 6 or 3 vectors depending if the load power is higher or lower than half of the rated load power is selected that minimizes the current cost function. Then among the 6/3 selected vector, one that minimizes the voltage cost function is selected and applied to the converter.

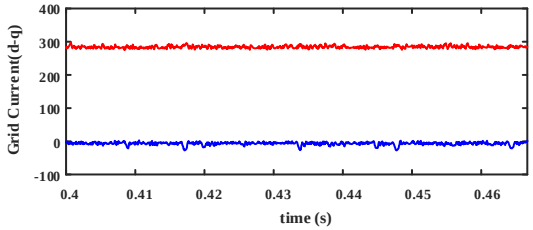
Figure 6.16 shows the simulation results for the developed controller at the rated power of 1.4 MW. The parameters of the system are shown in Table 6.6.



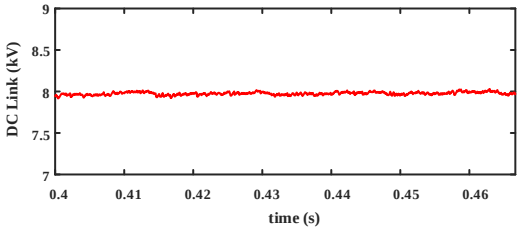
(a) Grid currents



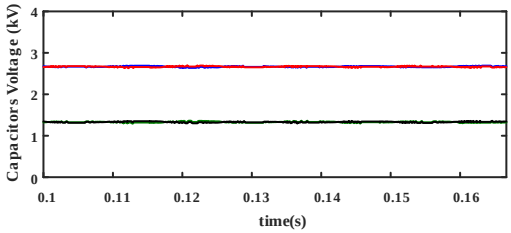
(b) Grid voltage and current-phase a



(c) d-q components of the grid current



(c) DC-link voltage



(e) Flying capacitors voltages

Figure 6.16 Computational efficient sequential MPC applied to the seven-level topology

The grid current, DC-link voltage, flying capacitors voltages, and grid current alongside the grid phase voltage are shown in Figure 6.16. The grid voltage THD is limited to 4% in rated condition (1.4 MW). As can be seen in Figure 6.16 (b), and (c), the power factor of the power absorbed from the grid is kept close to 1 through controlling d-q components of the grid current. Moreover, the DC-link voltage and flying capacitors voltages are well balanced at the desired values, which are 8 kV for the DC-link voltage, and [1.33kV, 2.66 kV] for the voltages of the flying capacitors.

Despite the advantages of the proposed strategy, the selected vectors that minimize the cascaded cost function are not optimal in terms of line current control or capacitor voltage balancing. This is due to the fact that cost functions are cascaded and the vectors selected in the first cost function do not consider the second one. Due to this fact, in comparison to the conventional MPC approach, either the line reactor or the flying capacitors must be increased to compensate for this phenomenon. Therefore, for the comparison studies in this chapter, the conventional MPC is applied to generate the gating signal of the seven-level converter and calculating efficiency and power quality.

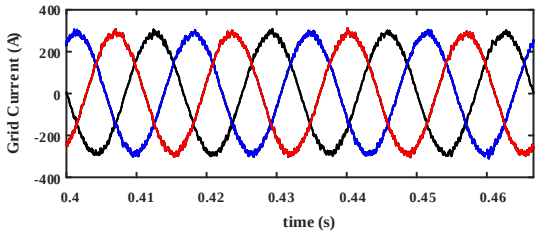
6.4.2 Simulation Studies, Efficiency, and Power Quality

In this section, simulation studies have been done in MATLAB/Simulink environment to investigate the performance of the seven-level topology as the AC/DC stage of the proposed EV charging station shown in Figure 6.13. The developed controller shown in Figure 6.14 is applied to the AC/DC stage to control the DC-link voltage at 8 kV, flying capacitors at 1.33 kV, and 2.66 kV while keeping the PF close to one.

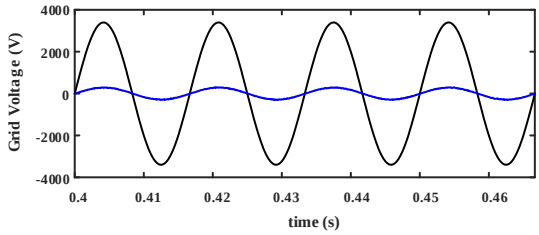
A. Simulation Results

Since the charging station must be able to regulate the DC-link voltage, and power factor in different power loads, the simulation results are shown in Figure 6.17, and

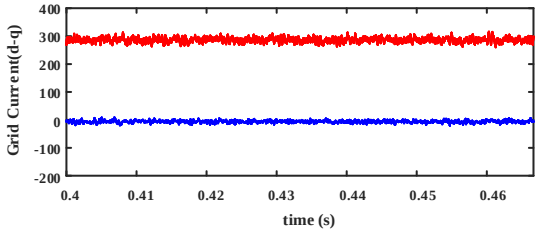
Figure 6.18 for 1.4 MVA (rated power), and 150 kW (low power) to demonstrate the effectiveness of the developed controller in different load powers.



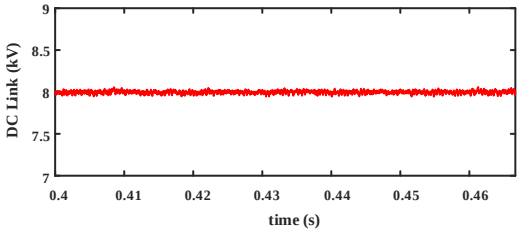
(a) Grid currents



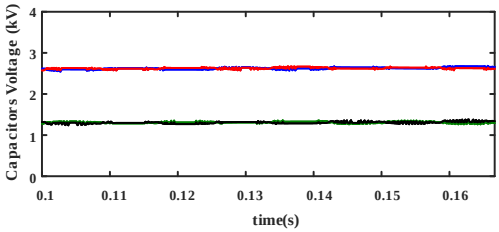
(b) Grid voltage and current-phase a



(c) d-q components of the grid current



(c) DC-link voltage



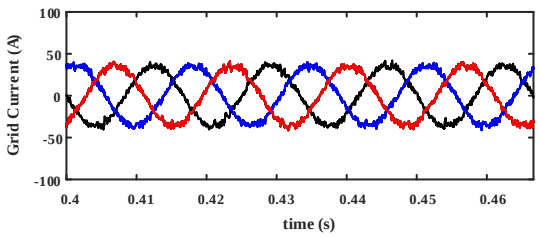
(e) Flying capacitors voltages

Figure 6.17 AC/DC stage of the proposed charging station at 1.4 MW

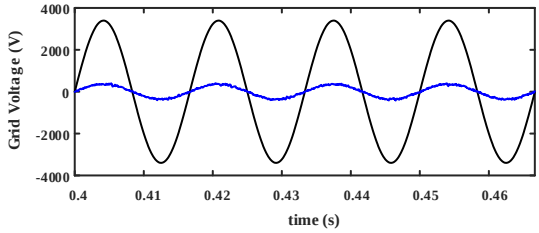
The grid current, DC-link voltage, flying capacitors voltages, and grid current alongside the grid phase voltage are shown in Figure 6.17. The grid voltage THD is limited to 4% in rated condition (1.4 MW). As can be seen in Figure 6.17 (b), and (c), the power factor of the power absorbed from the grid is kept close to 1 through controlling d-q components of the grid current. Moreover, the DC-link voltage and flying capacitors voltages are well balanced at the desired values, which

are 8 kV for the DC-link voltage, and [1.33kV, 2.66 kV] for the voltages of the flying capacitors.

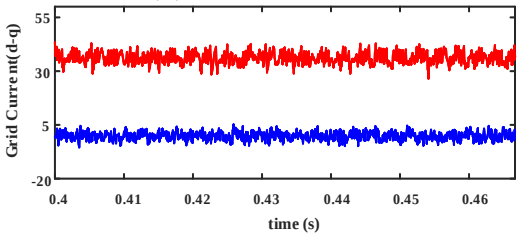
Figure 6.18 shows the same information at 150 kW, to demonstrate the performance of the seven-level AC/DC stage at low power ratings. As can be seen, the objectives of the controller such as; controlled DC-link voltage, balanced flying capacitor voltages, and PF close to 1 are achieved very well. The only difference in low power is the grid current THD that is 15 % in this case, which shows significant improvement compare to the previous case studies.



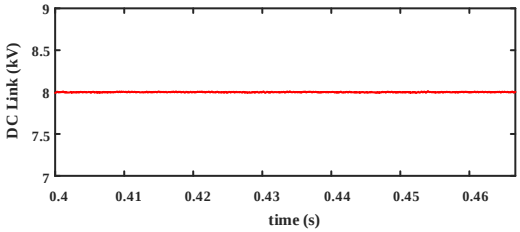
(a) Grid currents



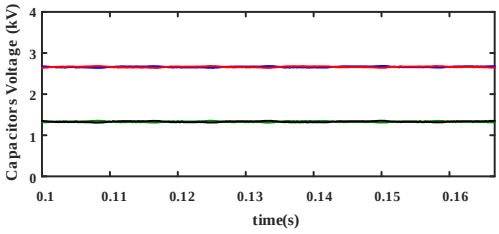
(b) Grid voltage and current-phase a



(b) d-q components of the grid current



(d) DC-link voltage



(e) Flying capacitors voltages

Figure 6.18 AC/DC stage of the proposed charging station at 150 kW

B. Efficiency, and Power Quality

In this section, the efficiency, and grid current THD of the seven-level topology as the AC/DC stage of the proposed charging station are investigated for different load powers. Same as previous case studies, PLECS software is used to calculate the efficiency of the seven-level topology as the AC/DC stage of the proposed charging station is shown in Figure 6.12. The IGBT module considered as the active switch of the seven-level topology for loss calculation is FF650R17IE4 from Infineon.

Moreover, the grid current THD for different load power is obtained from the seven-level topology as the AC/DC stage of the proposed MV-connected charging station in MATLAB/Simulink environment. The efficiency, and grid current THD of the seven-level topology as the AC/DC stage of the proposed charging station for different load powers are shown in Table 6.7.

TABLE 6.7 EFFICIENCY AND POWER QUALITY OF THE SEVEN-LEVEL TOPOLOGY

Power	Efficiency	Grid current THD
1400 kW	97.9 %	4.10 %
1050 kW	98.0 %	4.55 %
700 kW	98.1 %	5.67 %
350 kW	97.8 %	9 %
150 kW	96.6 %	16 %

As can be seen, similar to the previous case, the grid current THD is increased with the decrease of the load power, however, the THD is improved significantly in

comparison to three-phase PFC, and the four-level T-type NNPC with worst-case THD of 38.8 %, and 23.8 % respectively. This observation demonstrates the advantage of the seven-level topology over the two-level and four-level topologies in terms of power quality.

On the other hand, the efficiency of the seven-level topology, the opposite of the previous case study, does not decrease with the increase of the load power. This demonstrates the fact that the dominant power loss is not conduction losses. The efficiency of the AC/DC stage reaches 98.1 % at the half-rated load condition.

6.4.3 Cost Analysis

In this section, the costs of the components, and devices required to design the 1.4 MVA seven-level topology shown in Figure 6.12 as the AC/DC stage of the proposed MV-connected charging station are determined. As stated previously, the cost estimation is solely for the comparison between different cases studied in this chapter. Therefore, it cannot be treated as the actual manufacturing cost. The components considered for the cost estimation are the IGBT devices, gate drivers, capacitors, and transformer.

Since the maximum voltage stress on each device of the seven-level topology is one-third of the DC-link voltage, each IGBT must be able to handle approximately 2600 V, therefore, two 1700 V class IGBT is considered for each IGBT device.

Moreover, the rated current of the MV connected station is 194 A. Hence, the FF650R17IE4 from Infineon is considered as the IGBT device of the seven-level topology, which is a 1700 V class, 650 A IGBT. Therefore, 21 IGBT module is required with the cost of approximately $13,200. 2SP0320x2Ax gate driver from Power Integration is selected to drive the IGBTs, which has a total cost of approximately $5,200.

The cost of the flying capacitors is estimated to be $6,100 to build up a capacitor bank with 250 µF capacitance rated for 2600 V (the voltage across the flying capacitors). Therefore, the total cost is estimated to be $25,000, which is significantly lower than the previous case studies as compared in the next section. It is worth mentioning that since the proposed charging station is MV connected, there is no need for a line-frequency transformer, which is a significant advantage of the proposed charging station in terms of cost.

6.4.4 Advantages of the proposed MV connected charging station

In this section, the seven-level topology shown in Figure 6.12 is compared to the conventional three-phase PFC, and four-level T-type NNPC in terms of efficiency, power quality, and cost as the AC/DC stage of the charging station shown in Figure 6.1. The efficiency, grid current THD, cost, and line reactance inductance are shown in Table 6.5 for the case studies investigated in this chapter.

TABLE 6.8 PROPOSED MV CHARGING STATION VS LV CONNECTED CHARGING STATIONS

	Efficiency at 1.4 MW	Efficiency at 150 kW	THD at 1.4 MW	THD at 150 kW	Line Inductance	Cost
LV connected station- Four-level T-type NNPC	91.5 %	97 %	4.3 %	23.84 %	17 %	$58300
LV connected station- Conventional three-phase PFC	92.2 %	97.3 %	4.12 %	38.8 %	41 %	$48000
Proposed MV connected station-Seven-level Topology	97.9 %	96.6 %	4.10 %	16 %	15 %	$25000

The efficiency and grid current are shown for rated and low load powers to compare the extreme cases of efficiency and power quality.

As can be seen from Table 6.8, the efficiency of the seven-level topology as the AC/DC stage of the proposed MV connected charging station is significantly higher than the three-phase PFC, and the four-level topology at the rated condition due to the MV connection of the proposed charging station architecture and elimination of the line frequency transformer.

On the other hand, not only the worst-case THD of the grid current of the proposed charging station is reduced significantly in comparison to the three-phase PFC converter, and the four-level T-type converters, but also smaller line reactance is required. This is due to the seven-level output voltage of the seven-level topology,

which demonstrates the advantage of the proposed charging station in terms of power quality.

Moreover, the cost of the AC/DC of the proposed charging station is almost half of the LV-connected charging stations studied in this chapter, thanks to eliminating the line frequency transformer, lower current rating of the charging station, and the seven-level topology. The other cost factor such as line reactance can have a small impact on the cost comparison since increasing the voltage rating of the line inductors increases the cost and on the other hand decrease the current rating and impedance decreases the cost.

6.5 Summary

In this chapter, an MV-connected charging station architecture is proposed with the proposed seven-level topology in the previous chapter as the AC/DC stage of the charging station. The proposed charging station requires a network of series and parallel branches of DC/DC converter as the interface of the MV DC-link, and EV terminals, which reduces the number of conversion stages in comparison to other MV-connected charging stations in the literature. Moreover, as investigated in Chapter 6, the seven-level topology has a fewer number of components in comparison to other seven-level topology candidates.

To demonstrate the advantages of the proposed charging station architecture over LV connected stations, two LV connected charging stations were studied with the three-phase PFC, and four-level T-type NNPC as the AC/DC stage. It was shown that the proposed charging station is superior in terms of cost, efficiency, and power quality, due to the elimination of the line frequency transformer, lower current rating, and multilevel voltage of the AC/DC stage.

The results of the studies in this chapter demonstrate the advantage of the MV-connected charging station over LV connected station in terms of efficiency, cost, and power quality.

Chapter 6

Conclusions and Future Work

7.1 Conclusions

This thesis presents new advanced multilevel topologies, control techniques, and a new MV-connected ultra-fast EV charging station.

As discussed, to escape from a disaster regarding the environmental crisis in the near future, different industries must move toward the elimination of greenhouse gas emissions. In the case of the automotive industry, this can be achieved by the wide adoption of EVs by society. The main barriers regarding EV adoption at the time of writing this thesis are high cost, range anxiety, and lack of charging infrastructures. Therefore, significant efforts are required to overcome these barriers. Low-cost, efficient ultra-fast EV charging is proven to be one of the answers to the range anxiety, and lack of charging infrastructure barriers.

It was shown in this work, that the available ultra-fast chargers in the market are connected to the LV grid through expensive bulky line-frequency transformers. Due to the connection to the LV-grid, a significant amount of current is required to deliver the power to the EV batteries, which causes high power losses and low efficiency of the charging station. On the other hand, the need for line-frequency transformers increases the cost and footprint of the charging station significantly.

It was shown that the solution for these challenges is an MV-connected charging station, where the line-frequency is eliminated and the AC/DC stage of the charging station is directly connected to the MV-grid, while the galvanic isolation is achieved through high-frequency transformers of the DC/DC stage of the charging station. The MV-connected charging stations introduce many benefits in terms of efficiency, cost, and footprint. The increase of the input voltage results in the reduction of the required current to deliver high power to the EV battery, hence, the losses can be reduced significantly, which leads to a more efficient charging station. On the other hand, the elimination of the line-frequency transformer reduces the manufacturing cost of the charging station significantly, while decreasing the footprint of the charging station, which is an advantage for dense population areas.

An extensive literature review has been done on MV-connected ultra-fast EV charging station architectures in this thesis. It is shown that the main focus of the

researchers, is on the direct connection of the charging station to the MV-grid by medium-voltage high power multilevel converters due to their advantages such as lower power losses, higher power quality, and reduced voltage stress of the active power semiconductor devices. It is shown that the low-cost, efficient multilevel converters with low control complexities are the knowledge gap regarding the MV-connected ultra-fast EV charging stations.

An extensive literature review has been done on multilevel converters and their controllers. It is shown that the advanced multilevel topologies are proposed in the literature to overcome the drawbacks of conventional topologies in terms of the number of components and developing advanced simple controllers for their proper operation.

In this thesis, first, a control technique based on SPWM is developed to control the voltage of the flying capacitor of the four-level T-type NNPC, which has the lowest number of components among existing advanced and classic multilevel topologies. The simulation studies and experimental tests show that the developed controller can successfully control the voltage of the flying capacitors of the four-level T-type NNPC and overcome the barrier for its practical application.

It is found that the operating voltage and power rating of the four-level topology can be extended by developing an MPC-based control technique to control its flying

capacitors voltages at one-fourth of the DC-link voltage and operate the topology as a five-level converter. Therefore, the five-level T-NNPC is proposed, where simulation and experimental studies demonstrate its feasibility and performance. The proposed topology has the lowest number of components in comparison to existing advanced and classic multilevel topologies.

Since for higher voltage and power ratings, multilevel topologies with a higher number of voltage levels are favorable, a seven-level topology is proposed that has the lowest number of components among the existing topologies. An MPC-based controller is developed to control the voltages of the flying capacitors of the proposed seven-level topology. Due to the extensive computational burden of the developed MPC controller because of the higher number of redundancies of the proposed topology, an advanced computational efficient MPC controller is developed, which reduces the execution time of the seven-level topologies significantly. Simulation and experimental studies have been done to demonstrate the performance and feasibility of the proposed seven-level topology.

Finally, an MV-connected ultra-fast EV charging station is proposed, where the proposed seven-level topology serves as its AC/DC stage. Moreover, two other case studies are considered where a conventional three-phase boost converter and the

four-level T-NNPC are considered as the AC/DC stage of an LV-connected ultra-fast charging station.

It is found that for the case of LV-connected stations, a multilevel topology can improve the power quality absorbed from the grid, and reduce the line reactance significantly, while the cost and efficiency remain similar. However, it is shown that the proposed seven-level topology as the AC/DC stage of the MV-connected charging station, not only increases the efficiency and power quality significantly, it can reduce the manufacturing cost of the station to half of the LV-connected station. The main conclusion of this thesis would be the potential of the advanced multilevel topologies such as the proposed seven-level topology in reduction of the cost and increasing the efficiency and power quality of the MV-connected charging stations.

7.2 Future work

The work on the proposed multilevel topologies, control techniques, and the MV-connected ultra-fast EV charging station can be continued in several aspects. The first, and the most important one, is the integration of renewable energies into the charging station through the AC/DC multilevel topology. This can be done by either integration of these sources through the flying capacitor voltage of the

proposed topologies or innovating ways to interact with the MV DC-link provided by the multilevel AC/DC stage.

Another possible aspect is the interaction of the MV DC-link provided by the proposed topology with the DC/DC stage of the charging stage. The proposed architecture suggests a network of parallel series branches of isolated DC/DC converters to provide the constant LV DC-link for the charging station or directly charging the vehicles. One can face this matter regarding the controller side, where the parallel and series branches are controlled to provide the charging power for the EV batteries, or finding innovative structure/topology of DC/DC converter to solve the challenge regarding transforming MV voltage to LV voltage.

Another aspect from the AC/DC side is the fault-tolerant capability of the proposed topology or any advanced topology as the AC/DC stage of an MV-connected charging station. This can solve the main concern of these charging stations, which is the reliability of direct connection to the MV grid.

The other possible path can be researched on pre-charging of the flying capacitor voltages of the proposed topology in the MV-connected ultra-fast charging station reliably and safely.

Heat dissipation is one of the areas that has not been investigated extensively for advanced multilevel topologies. The cooling system design and heat dissipation

in AC/DC stage of the MV-connected stations can be a hot research topic that facilitates the practical application of the advanced multilevel topologies.

Lastly, the dynamic response of MPC can be examined to shed light on the advantages of employing MPC based controllers in MV-connected charging station, which suffers from high dynamic load.

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