

DESIGN AND ANALYSIS OF A 70KW 3-LEVEL  
ACTIVE NEUTRAL POINT CLAMPED (ANPC)  
INVERTER FOR TRACTION APPLICATIONS

DESIGN AND ANALYSIS OF A 70KW 3-LEVEL ACTIVE  
NEUTRAL POINT CLAMPED (ANPC) INVERTER FOR  
TRACTION APPLICATIONS

BY  
YICHENG WANG, B.Eng.

A THESIS  
SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING  
AND THE SCHOOL OF GRADUATE STUDIES  
OF MCMASTER UNIVERSITY  
IN PARTIAL FULFILMENT OF THE REQUIREMENTS  
FOR THE DEGREE OF  
MASTER OF APPLIED SCIENCE

© Copyright by Yicheng Wang, May 2021

All Rights Reserved

Master of Applied Science (2021)  
(Electrical Engineering)

McMaster University  
Hamilton, Ontario, Canada

TITLE: Design and Analysis of a 70KW 3-Level Active Neutral  
Point Clamped (ANPC) Inverter for Traction Applica-  
tions

AUTHOR: Yicheng Wang  
B.Eng. (Electrical Engineering),  
McMaster University, Hamilton, Canada

SUPERVISORS: Dr. Mehdi Narimani, Dr. Ali Emadi

NUMBER OF PAGES: xiv, 122

# Abstract

For an Electrical Vehicle, the power is delivered from the battery pack to the electric motor through the use of power converter. Many research projects has been conducted in improving the efficiency of traction inverters. Inverter topologies are categorized based on the number of voltage levels of the inverter output phase voltage. The conventional 2-level Voltage Source Inverter (VSI) is commonly used as a traction inverter due to its simple structure. Due to the recent trend in utilizing higher DC-link voltage in traction motor drives to achieve a higher power rating, multi-level inverters are gaining attention to replace the conventional VSI in EV powertrain.

Multi-level voltage source inverters (MLVSI) has been widely adopted in the high-power converters and medium-voltage drives. There are four major categories of MLVSI: the Flying Capacitor (FC), Neutral Point Clamped (NPC), Cascaded and Hybrid. The power rating of the MLVSI increases with the increase of inverter levels, but the size, number of switching devices, cost and control difficulty also increases. Due to the above reasons, 3-level NPC can be a good solution for traction inverters. Due to the structure and control limitation, Diode Clamp NPC suffers from uneven loss distribution and neutral point voltage balancing issues. This issue can be resolved with Active Clamped NPC (ANPC). In this thesis, the design, simulation, prototyping and testing of a 70kw 3-level ANPC traction is introduced.



# Acknowledgements

I would first like to express my deep appreciation to Dr. Mehdi Narimani and Dr. Ali Emadi for their guidance and support throughout my graduate studies. As my supervisor and co-supervisor, they both played an important role in getting me to where I am now as a researcher and I am very grateful for the opportunities that they have provided for me.

Additionally, my sincere appreciation also goes to Dr. Berker Bilgin who I could also always rely on for advice and assistance. His confidence in my work and willingness to always support me has helped me to achieve my goals both academically and professionally.

My gratitude also goes to my colleagues from the Department of Electrical and Computer Engineering, especially Amirreza Poorfakhraei, who has been a great leader in this project and a great friend. His guidance, knowledge and leadership has played a key role in the success of this project. I would also like to express my deep appreciation to Dr. Peter Azer, Dr. Alan Callegaro, Dr. Sumedh Dhale, Jacob Gareau, Dr. Romina Rodriguez, Fatemeh Abolqasemi Kharanaq, Dr. Atriya Biswas , Xiaoqian Xing and Yuhang Yang who would never hesitate to stop what they are doing to assist me.

Last but not least, I would like to give a special thank you to my family. I would

not be here without the love and support from my parents, Shansong Wang and Xiaochan Li, as they have helped to shape the person I am today. A very special thank you to my fiancée, Rose Song, who has shown me unconditional love and patience through my graduate studies and has always been by my side through this journey.

This research was undertaken thanks to funding from the Natural Sciences and Engineering Research Council of Canada (NSERC). I would also like to thank ANSYS for their support with ANSYS workbench, Mathworks for their support with Matlab and Simulink, and Plexim for their support with PLECS.

This work is dedicated to the memory of Iman Aghabali and Mehdi Eshaghian-two friends that truly made the workplace a more enjoyable place to be and are dearly missed.

# Contents

<b>Abstract</b>	<b>iii</b>
<b>Acknowledgements</b>	<b>iv</b>
<b>1 Introduction</b>	<b>1</b>
1.1 Background and Motivation . . . . .	1
1.2 Contributions . . . . .	2
1.3 Thesis Structure . . . . .	3
<b>2 Introduction to Multi-Level Inverters for Traction Applications</b>	<b>5</b>
2.1 Conventional Two-level Three-phase Voltage Source Inverters . . . . .	5
2.1.1 Structures of Two-level Three-phase Voltage Source Inverters . . . . .	6
2.1.2 Control of Two-Level Three-Phase Voltage Source Inverters . . . . .	8
2.2 Multi-level Inverters . . . . .	21
2.2.1 Structures of Multi-Level Inverters . . . . .	21
2.2.2 Control of Multi-Level Inverters . . . . .	25
2.3 Summary . . . . .	38
<b>3 Analysis and Study of 2-Level and 3-Level Voltage Source Inverters</b>	

<b>for Traction Applications</b>	<b>39</b>
3.1 Introduction . . . . .	40
3.2 Switch Selection . . . . .	42
3.2.1 Device Voltage rating . . . . .	43
3.2.2 Number of Switches . . . . .	43
3.3 Power Loss Calculation . . . . .	45
3.3.1 Switch Power Loss . . . . .	45
3.3.2 Diode Power Loss . . . . .	47
3.4 Simulation Results . . . . .	48
3.4.1 Drive Cycle Simulation . . . . .	52
3.4.2 Inverter Output Current and Voltage THD Simulation . . . . .	59
3.5 Summary . . . . .	60
<b>4 Design of a 70kW 3-Level Active Neutral Point Clamped (ANPC)</b>	
<b>Inverter for Traction Applications</b>	<b>62</b>
4.1 Introduction . . . . .	62
4.2 Components Selection . . . . .	63
4.2.1 Switch Selection . . . . .	63
4.2.2 Gate Driver Selection . . . . .	65
4.2.3 Capacitor Selection . . . . .	67
4.2.4 Sensor Selection . . . . .	71
4.3 ANPC Power PCB Design . . . . .	71
4.3.1 PCB Layer Stack . . . . .	73
4.3.2 Simulation and Analysis of ANPC Power PCB . . . . .	75
4.4 Summary . . . . .	87

<b>5</b>	<b>Experimental Implementation and Validation of a 3-Level ANPC</b>	
	<b>Prototype</b>	<b>88</b>
5.1	Introduction . . . . .	88
5.2	Inverter Assembly . . . . .	89
5.3	Low Power Resistive Preliminary Testing . . . . .	91
	5.3.1 Fault Detection . . . . .	92
	5.3.2 Low Power Output Voltage and THD . . . . .	95
5.4	Summary . . . . .	101
<b>6</b>	<b>Conclusions and Future Work</b>	<b>102</b>
6.1	Future Work . . . . .	103
	<b>References</b>	<b>105</b>

# List of Figures

2.1	Two-level voltage source inverter . . . . .	6
2.2	The components of a typical film capacitor bank . . . . .	7
2.3	Closed loop current control scheme of an EM . . . . .	8
2.4	Sinusoidal Pulse Width Modulation for 2-level VSI . . . . .	9
2.5	SPWM gating signals and output phase voltage . . . . .	10
2.6	SPWM output phase voltage and line-to-line voltage . . . . .	12
2.7	Phase A modulating signal for THISPWM . . . . .	14
2.8	Space vector diagram of a 2-level VSI . . . . .	15
2.9	Equivalent circuit for switching state POO . . . . .	16
2.10	Reference vector in Sector I . . . . .	18
2.11	Seven-segment switching sequence in Sector I . . . . .	19
2.12	Structure of 3-level NPC . . . . .	23
2.13	Structure of 3-level ANPC . . . . .	24
2.14	Structure of 4-level and 5-level NPC . . . . .	25
2.15	IPD SPWM . . . . .	26
2.16	IPD SPWM gating signal generation and inverter output voltage . . . . .	27
2.17	APOD SPWM . . . . .	27
2.18	APOD SPWM gating signal generation and inverter output voltage . . . . .	28

2.19	Space vector diagram of 3-level inverter . . . . .	29
2.20	Space vectors of 3-level inverter in Sector I . . . . .	30
2.21	Region 1 and 3 in Sector I . . . . .	33
2.22	The gating signals for four popular modulation schemes: (a) Diode-clamped ANPC modulation scheme, (b) Same-side modulation scheme, (c) Opposite-side modulation scheme, and (d) Full-path modulation scheme. . . . .	36
3.1	Switch voltage and current transient during a switching period. . . . .	45
3.2	Efficiency results for each inverter topology at 10kHz and 100kHz under four motor operating conditions: (a) motor low speed and low torque, (b) motor low speed and high torque, (c) motor high speed and low torque, and (d) motor high speed and high torque. . . . .	51
3.3	Drive Cycle Simulink block . . . . .	52
3.4	Driver Simulink block . . . . .	53
3.5	Motor Control Simulink block . . . . .	54
3.6	Motor Simulink block . . . . .	54
3.7	Final Drive Simulink block . . . . .	55
3.8	Wheel Simulink block . . . . .	55
3.9	Chassis Simulink block . . . . .	56
3.10	Battery Simulink block . . . . .	57
3.11	Simulation of battery SOC for different topologies in UDDS drive cycle. . . . .	58
3.12	Simulation of battery SOC for different topologies in HWFET drive cycle. . . . .	58
3.13	Performance overview of different inverter topologies. . . . .	61
4.1	UJ4C075018K4S typical output characteristics at $T_j=175^\circ$ . . . . .	65

4.2	Equivalent gate drive circuit. . . . .	66
4.3	Equivalent circuits for switching states PNN and PPN. . . . .	68
4.4	Capacitor rms current ripple is a function of modulation index M and load power factor $\cos\phi$ . . . . .	69
4.5	Minimum capacitance required for the desired voltage ripple is a function of modulation index M and load power factor $\cos\phi$ . . . . .	70
4.6	Schematic of ANPC power PCB phase A leg. . . . .	72
4.7	3D view of ANPC power PCB. . . . .	73
4.8	ANPC phase A MOSFET and capacitor connections. . . . .	74
4.9	ANPC power PCB layer stack. . . . .	74
4.10	ANPC power PCB polygon pours in each layer. . . . .	76
4.11	ANPC power PCB design procedures. . . . .	77
4.12	Equivalent circuit used in the overshoot analysis and calculation of PCB polygon pour stray inductance limit. . . . .	79
4.13	DC current density analysis. . . . .	83
4.14	AC current density analysis. . . . .	84
4.15	Polygon pour connection type. . . . .	84
4.16	ANSYS CFD solver set-up for steady-state and transient thermal simulation. . . . .	85
4.17	Polygon pour connection type. . . . .	86
4.18	Clearance and creepage distance. . . . .	87
5.1	Gate driver PCB. . . . .	89
5.2	SMD291AX10T5 recommended reflow temperature profile. . . . .	90
5.3	Mounting the MOSFETs onto the inverter housing. . . . .	91



5.4	Mounting the power PCB onto the inverter housing. . . . .	91
5.5	Preliminary low power testing setup. . . . .	92
5.6	Controller used in the preliminary low power testing setup. . . . .	92
5.7	Shut down by changing the duty cycles of all EPWM gating signals to 0%. . . . .	94
5.8	Shut down using the Trip-Zone Submodule. . . . .	94
5.9	Inverter output line voltages ( $V_{AB}, V_{BC}$ and $V_{CA}$ ) at modulation index of 0.9. . . . .	95
5.10	Transition of phase voltage $V_{AO}$ from modulation index of 0.1 to 0.9.	96
5.11	Transition of line voltage $V_{AB}$ from modulation index of 0.1 to 0.9. . .	96
5.12	Harmonic spectrum phase voltage of $V_{AO}$ . . . . .	97
5.13	Harmonic spectrum phase voltage of $V_{AB}$ . . . . .	98
5.14	Measured and simulated voltage THD at various fundamental frequen- cies. . . . .	100
5.15	Measured and simulated voltage THD at various modulation index ma. 100	

# List of Tables

2.1	2-level VSI SPWM switching pattern . . . . .	11
2.2	SVPWM space vectors and switching states . . . . .	16
2.3	Seven-segment switching sequence for all six sectors . . . . .	20
2.4	Four categories of multi-level voltage source inverter . . . . .	22
2.5	Switching states of 3-level NPC . . . . .	29
2.6	Switching states of 3-level NPC . . . . .	32
2.7	7-segment switching sequence in Sector I . . . . .	34
2.8	Sector loop-up table . . . . .	34
2.9	Region loop-up table . . . . .	35
3.1	Selected switches . . . . .	42
3.2	System Parameters . . . . .	42
3.3	Switch Selection for 2-level VSI . . . . .	44
3.4	2015 Spark EV Parameters . . . . .	52
3.5	Battery SOC at the end of simulation and SOC drop for the drive cycle	59
3.6	Output THD comparison . . . . .	60
4.1	ANPC Inverter Parameters . . . . .	63
4.2	Short list of available switches . . . . .	64
4.3	UCC21750 features . . . . .	67

4.4	3-level ANPC switching states for Same-side modulation scheme . . .	78
4.5	Larger commutation loop stray inductance components . . . . .	80
4.6	Parameters for determining the maximum allowable PCB polygon stray inductance . . . . .	81
4.7	PCB polygon pour stray inductance . . . . .	81
5.1	Low power testing parameters . . . . .	95
5.2	Harmonic order and magnitude for phase voltage at $m_a = 0.9$ . . . . .	98
5.3	Harmonic order and magnitude for line voltage at $m_a = 0.9$ . . . . .	99

# Chapter 1

## Introduction

### 1.1 Background and Motivation

For any technology, there is a tipping point in time when its path towards market dominance is a certainty. Electric vehicles are certainly a technology that will become dominant over their predecessor, the internal combustion vehicles. For an EV, the power is delivered from the battery pack to the motor through the use of power converters. There are many losses associated with this process. When current passes through conductors, it creates losses in the form of heat. And higher currents result in a higher power loss, and thus a lower efficiency in the powertrain. This thesis is focused on improving the efficiency of the electrical powertrain, in particular, the efficiency of the power converter. The design, prototyping, and testing of an 70kW ANPC traction inverter is explained in this thesis.

Compare with the convectional 2-level VSI that is wildly adopted by auto-makers such as Tesla, the ANPC is able to operate at a much higher voltage level. And for the same power rating, higher voltage results in a lower current, thus results in better

efficiency. The ANPC is able to operate at high efficiency when the motor operates at low speed and low torque, unlike the conventional inverters that usually have an efficiency worse than 70% at this condition. The vehicles also benefit from lighter and thinner cables, lower weight, lower manufacturing cost, higher power throughput, faster charging, and more efficient motors. In a comparison of cost, ANPC is usually more expensive due to the additional components. However, considering the savings in the cost of battery, filters, and heatsink results in an almost equal price for the two structures. In terms of reliability, although the higher number of components in ANPC increases the failure rate, the intrinsic fault-tolerance of ANPC structures compensates for the low reliability. Using the ANPC, we can improve the overall efficiency of the vehicles and save energy for our future generations.

## 1.2 Contributions

The main contributions of this thesis are summarized as:

1. An in-depth literature review of the existing 2-level and multi-level VSI. The structure and control technique of 2-level VSI, 3-level NPC and ANPC are discussed in details. The algorithms for Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) is summarized and compared.
2. A comprehensive analysis and comparison of 2-level VSI, 3-level NPC and ANPC in traction application. An analytical method for calculating the inverter power loss is proposed, and the results are verified in MATLAB/Simulink

and PLECS simulation. The comparison focuses on the efficiency, output current/voltage THD, system cost, stress across switches and system reliability.

3. A detailed drive cycle simulation model is proposed. The model is build in MATLAB/Simulink, and the performance of 2-level VSI, 3-level NPC and ANPC in the drive cycle analysis are compared.
4. A detailed design procedure for a 70kW 3-level ANPC is proposed. The design procedure can be implemented to any inverter systems with both busbar and PCB as the current carrying medium. An analytical method for calculating the voltage overshoot during switch turn-OFF transient is proposed. Finite element analysis for calculating the stray inductance, current density and thermal performance is discussed in details.
5. A discussion of the low power preliminary testing. The method for handling faults in the DSP controller and results for output voltage THD is discussed.

### 1.3 Thesis Structure

This thesis is organized as follows:

Chapter 2 provides a comprehensive literature review of the existing 2-level and multi-level VSI. This chapter focus on the structure and control of 2-level VSI, 3-level NPC and ANPC. Two popular pulse width modulation methods are discussed: SPWM and SVPWM. Four modulation scheme of 3-level ANPC is discussed and compared, they are Diode-clamped ANPC modulation, Same-side modulation, Opposite-side modulation and Full-path modulation.

Chapter 3 presents a comprehensive analysis and comparison between the 2-level VSI, 3-level NPC and ANPC in traction application. In this comparison, Silicon Carbide MOSFET, Gallium Nitride MOSFET and Silicon IGBT are employed. An analytical method for calculating the power loss is discussed in detail. A power loss simulation is built in MATLAB/Simulink and loss curves from the device datasheets are utilized by the PLECS. A permanent magnet synchronous motor is used as the load. The performance of each inverter topology is investigated in different load conditions and switching frequencies. Moreover, a vehicle model is employed to study the performance of each inverter topology for different drive cycles.

Chapter 4 presents a detailed design procedure of a 70kW 3-level ANPC. A detailed components selection includes semiconductor, capacitor, gate driver and sensors is first discussed. Next, the design of the ANPC power PCB is introduced. The communication loop of the inverter is analysed and an analytical method for calculating the voltage overshoot is proposed. The analysis and simulation of stray inductance, current density and PCB thermal performance is conducted in ANSYS using the PCB CAD model. Finally, the creepage/clearance and PCB coating method is discussed.

Chapter 5 presents the assembly process and low power preliminary testing of the first prototype. Results for gate driver fault detection and inverter output voltage THD is also discussed in this chapter.

Chapter 6 concludes the overall contribution of this thesis. Proposed future work with higher power testing plan is also discussed in this chapter.

# Chapter 2

## Introduction to Multi-Level Inverters for Traction Applications

### 2.1 Conventional Two-level Three-phase Voltage Source Inverters

This chapter presents the the structures and control methods for 2-level VSI, 3-level NPC and ANPC. Two pulse width modulation techniques are discussed: Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM). SPWM is the simplest PWM scheme used in adjustable speed drives. Compare with SVPWM, SPWM results in reduced DC-link voltage utilization without 3rd harmonic injection and greater output THD. Hence, SVPWM are most widely used for controlling traction inverters [1, 2]. 3-level inverter in traction application has attracted special attention for the last few decades. For the same DC-link voltage, the power rating of the switching devices in 3-level inverters are lower than 2-level



VSI, and this results in a lower switching losses especially in high switching frequencies [3]. 3-level inverters also produce a lower total harmonic distortion (THD), and lower EMI emission [4].

### 2.1.1 Structures of Two-level Three-phase Voltage Source Inverters

Inverter topologies are categorized based on the number of voltage levels of the inverter output phase voltage. The conventional 2-level VSI is commonly used as a traction inverter due to its simple structure, as shown in Figure 2.1. There are 6 switches in total in a 2-level VSI, and each inverter leg has 2 switches [5]. Laminated busbar has been commonly used in electric vehicle traction inverters. It connects the DC power source, DC-link capacitor, and semiconductor devices. A DC/DC boost converter can be connected between the DC input and the inverter to step-up the input DC voltage to the desired value before it connects to the inverter [6].

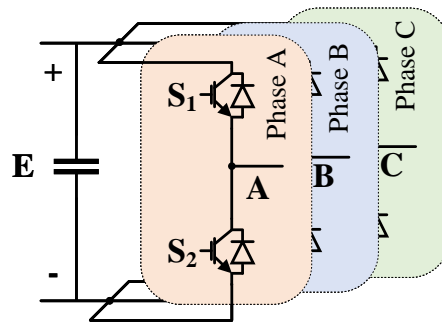


Figure 2.1: Two-level voltage source inverter.

Three-phase IGBT and MOSFET power modules have been widely adopted for

the automotive industry. Semiconductor manufactures are able to produce 2-level traction power modules with upto 200KW power rating, and having a break-down voltage of upto 1200V [7]. Compared with discrete power semiconductors, using power modules improves the inverter power density and reliability.

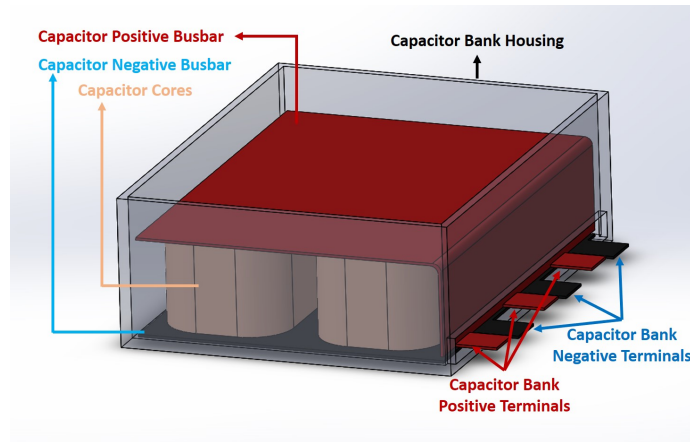


Figure 2.2: The components of a typical film capacitor bank.

The DC-link capacitor is used to provide low impedance path for high frequency ripple current, and decouple the stray inductance effect from the DC voltage source to the power module [8], [9]. Electrolytic capacitors and film capacitors are commonly used in traction inverters. The two types of capacitors have different energy densities and current ripple capabilities [10]. The electrolytic capacitors offers a better capacitance per volume and a cheaper price. However, its lifetime is shorter than a film capacitor, and many studies have focused on replacing the electrolytic capacitors with film capacitor to improve the system reliability [11], [12]. A typical structure of a film capacitor bank is shown in Figure 2.2 [13]. The capacitor cores are sandwiched in between the capacitor's positive and negative busbars, and the rest of the space inside the capacitor bank housing is filled with epoxy resin to secure the components inside, and provide electrical isolation [14]. It is desirable to have a capacitor bank with a

lower equivalent series inductance (ESL) to reduce the voltage overshoot across the semiconductor device, and to minimize the electromagnetic interference (EMI).

### 2.1.2 Control of Two-Level Three-Phase Voltage Source Inverters

The switching pattern of the power semiconductors are generated using pulse width modulation (PWM) techniques. The two most popular PWM techniques will be discussed in this section, namely the sinusoidal PWM (SPWM) and space vector PWM (SVPWM).

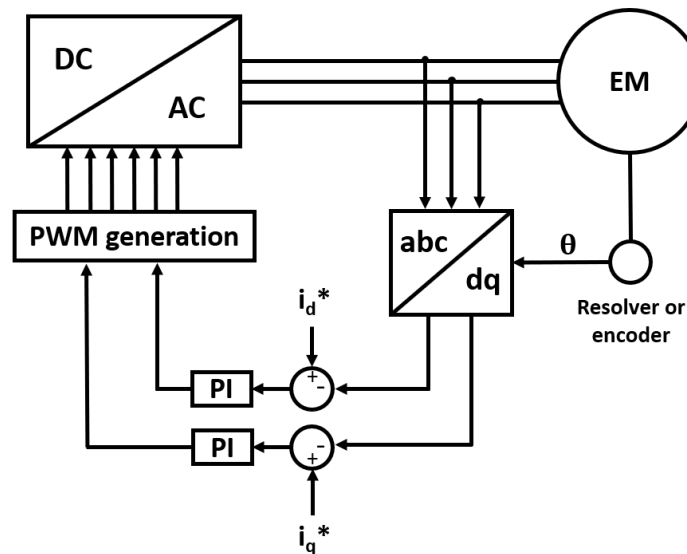


Figure 2.3: Closed loop current control scheme of an EM.

Figure 2.3 shows the closed loop current control for an electrical motor (EM) [15]. The three phase currents are sampled with at least two current sensors, and then converted into its dq currents. The electrical phase angle used in the abc to dq transformation calculation is converted from the mechanical position of the motor shaft,

which is usually sampled from a resolver or encoder. Sometimes, the encoder and resolver will provide the mechanical speed of the motor instead. Then the mechanical speed needs to be converted to the electrical phase angle first. The sampled dq current values are compared with the reference values, and the errors are passed to two PI controllers. The output voltage reference of the PI controllers are used for the PWM generations.

Due to the switching effect of the inverter, the output phase current will have total harmonic distortion (THD). The current harmonics are undesirable since it contributes to the copper losses in the motor winding, and creates torque ripple. Many factors contribute to the inverter current THD such as the inverter topology, switching frequency, load condition and modulation techniques.

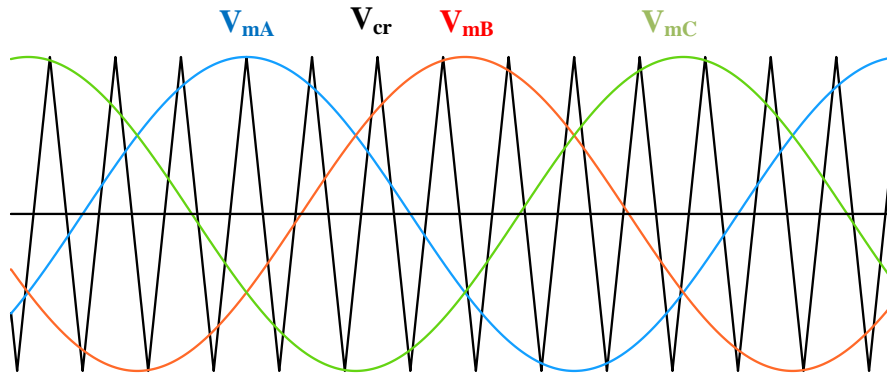


Figure 2.4: Sinusoidal Pulse Width Modulation for 2-level VSI.

### Sinusoidal Pulse Width Modulation

SPWM has been widely implemented in the industry for inverter control due to its simplicity [16]. Back in the days, SPWM was implemented using analog circuits.

Thanks to the advancement of the microcontroller unite (MCU) and digital signal controller (DPS), the software implementation of SPWM has become the industry standard. The SPWM for 2-level VSI is a carrier based modulation technique. As it can be seen from Figure 2.4, the SPMW consists of 3 sinusoidal modulating waves and one high frequency triangular carrier wave. At every switching cycle, the modulating wave is compared with the carrier wave to determine the switching states of each switches. The three modulating waves ( $V_{mA}$ ,  $V_{mB}$ ,  $V_{mC}$ ) are 120 degrees out of phase to each other, and their frequencies determine the fundamental frequency of the inverter output AC waveform. The carrier wave  $V_{cr}$  is usually a triangular wave, and its frequency determines the switching frequency of the inverter. The modulating signals can be expressed as:

$$\begin{aligned} v_{ma} &= m_a \sin(\omega t) \\ v_{mb} &= m_a \sin\left(\omega t - \frac{2\pi}{3}\right) \\ v_{mc} &= m_a \sin\left(\omega t + \frac{2\pi}{3}\right) \end{aligned} \quad (2.1.1)$$

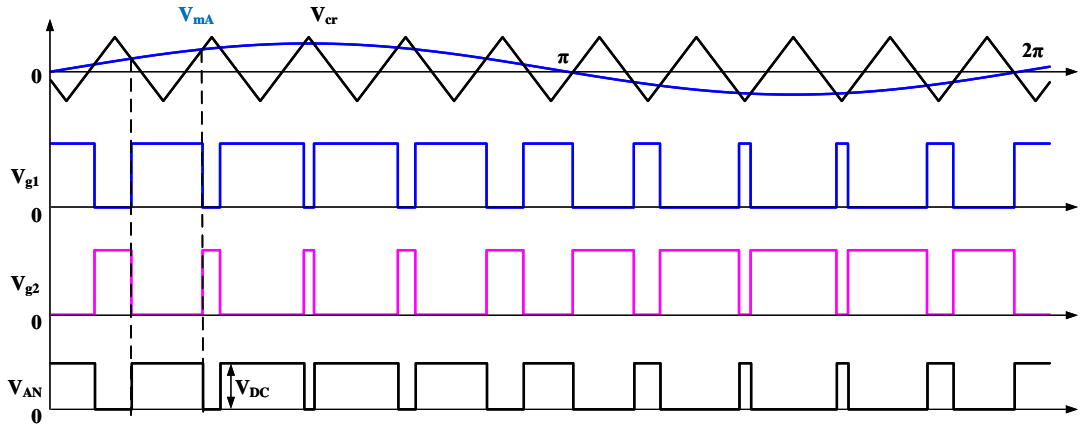


Figure 2.5: SPWM gating signals and output phase voltage.

In a 2-level VSI, there are six switches in total, and 2 switches in each inverter leg as shown in Figure 2.1. In each inverter leg, the top and bottom switches ( $S_1$  and  $S_2$ ,  $S_3$  and  $S_4$ ,  $S_5$  and  $S_6$ ) are complementary, and they can not be switched on at the same time. Otherwise, a short circuit will occur on the input DC link. The gating signal ( $V_{g1}$  and  $V_{g2}$ ) for switches  $S_1$  and  $S_2$  in inverter phase A leg is shown in Figure 2.5. When the phase A modulating wave ( $V_{mA}$ ) is larger than the carrier wave ( $V_{cr}$ ),  $S_1$  is switched on and  $S_2$  is switched off, and the resulting inverter output phase A voltage ( $V_{AN}$ ) is equal to the DC-link voltage  $V_{DC}$ ; when the phase A modulating wave ( $V_{mA}$ ) is less than the carrier wave ( $V_{cr}$ ),  $S_1$  is switched off and  $S_2$  is switched on, and the resulting inverter output phase A voltage ( $V_{AN}$ ) is equal to 0 [17]. Similarly for phase B and phase C, and the switching pattern is summarized in Table 2.1 [18].

Table 2.1: 2-level VSI SPWM switching pattern

Phase A	$V_{mA} > V_{cr}$	$S_1$ ON, $S_2$ OFF	$V_{AN} = V_{DC}$
	$V_{mA} < V_{cr}$	$S_1$ OFF, $S_2$ ON	$V_{AN} = 0$
Phase B	$V_{mB} > V_{cr}$	$S_3$ ON, $S_4$ OFF	$V_{BN} = V_{DC}$
	$V_{mB} < V_{cr}$	$S_3$ OFF, $S_4$ ON	$V_{BN} = 0$
Phase C	$V_{mC} > V_{cr}$	$S_5$ ON, $S_6$ OFF	$V_{CN} = V_{DC}$
	$V_{mC} < V_{cr}$	$S_5$ OFF, $S_6$ ON	$V_{CN} = 0$

The inverter output line-to-line voltage  $V_{AB}$  is shown in Figure 2.6, and the line-to-line voltage for all three phases can be calculated using the equation:

$$\begin{aligned}
 V_{AB} &= V_{AN} - V_{BN} \\
 V_{BC} &= V_{BN} - V_{CN} \\
 V_{AC} &= V_{AN} - V_{CN}
 \end{aligned} \tag{2.1.2}$$

The amplitude modulation index  $m_a$  and frequency modulation index  $m_f$  can be

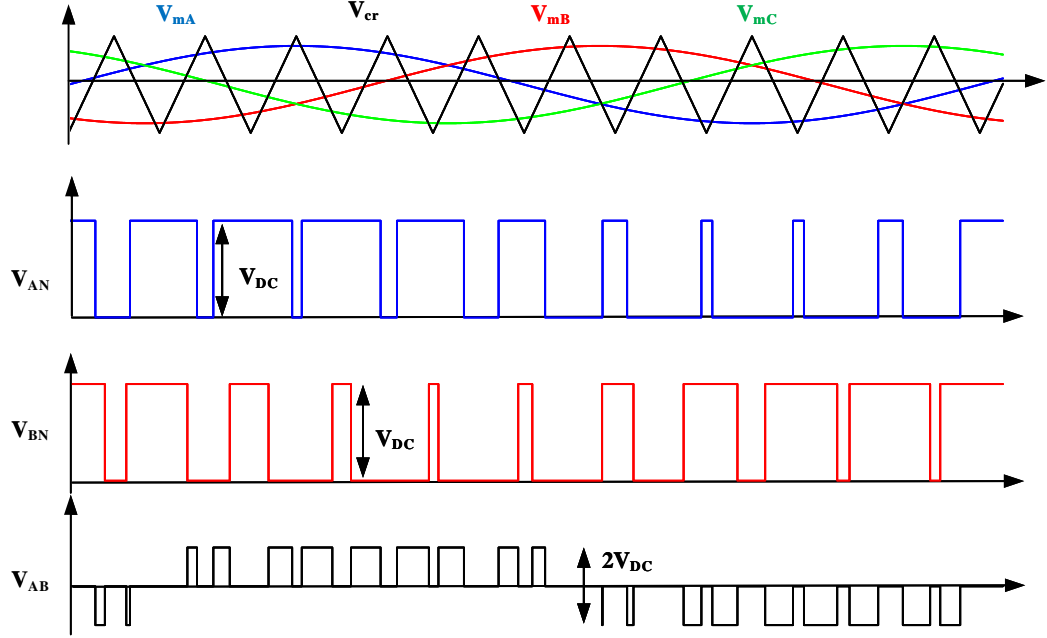


Figure 2.6: SPWM output phase voltage and line-to-line voltage.

calculated using equations:

$$\begin{aligned}
 m_a &= \frac{\hat{V}_m}{\hat{V}_{cr}} \\
 m_f &= \frac{f_{cr}}{f_m}
 \end{aligned}
 \tag{2.1.3}$$

Where  $\hat{V}_m$  and  $\hat{V}_{cr}$  is the amplitude of modulating waves and carrier wave respectively.  $f_{cr}$  and  $f_m$  is the frequency of the carrier wave and modulating waves respectively. The magnitude and the fundamental frequency of the inverter line-to-line voltage can be controlled by  $m_a$  and  $f_m$  independently.

The linear modulation range is defined as when ( $m_a \leq 1$ ), and over modulation is defined as when ( $m_a > 1$ ). The amplitude of the line-to-line voltage fundamental

$V_{LL}$  can be calculated using equation:

$$\begin{aligned} V_{LL} &= 0.612m_a V_{DC}, \text{ Linear Modulation when } m_a \leq 1 \\ V_{LL} &= 0.78V_{DC}, \text{ Over Modulation when } m_a > 1 \end{aligned} \quad (2.1.4)$$

The maximum amplitude of the line-to-line voltage in linear modulation and over modulation are  $0.612V_{DC}$  and  $0.78V_{DC}$  respectively. Despite the simplicity of SPWM, the biggest draw back is the maximum output line-to-line voltage is limited to  $0.612V_{DC}$  at linear modulation, and operating at over modulation increases the output THD significantly.

### **Sinusoidal Pulse Width Modulation with Third Harmonic Injection**

In order to improve the DC bus supply voltage utilization, the Third Harmonic Injection SPWM (THISPWM) was developed to improve the inverter performance [19]. In THISPWM, a common mode 3rd harmonic content,  $v_3$ , is added into each modulation signals shown in (2.1.1). And the modulation signals for THISPWM can be expressed as:

$$\begin{aligned} v_{ma,THI} &= m_a \sin(\omega t) + v_3 \\ v_{mb,THI} &= m_a \sin\left(\omega t - \frac{2\pi}{3}\right) + v_3 \\ v_{mc,THI} &= m_a \sin\left(\omega t + \frac{2\pi}{3}\right) + v_3 \end{aligned} \quad (2.1.5)$$

Where,  $v_3 = \frac{1}{6} \sin(3\omega t)$

The resulting modulating signal appears as saddle-like shape as shown in Figure



2.7 [20]. The magnitude of the modulating signals are decreased after the 3rd harmonic injection, but there are two maximum points at each half fundamental period at  $\frac{\pi}{3}$  and  $\frac{2\pi}{3}$ .

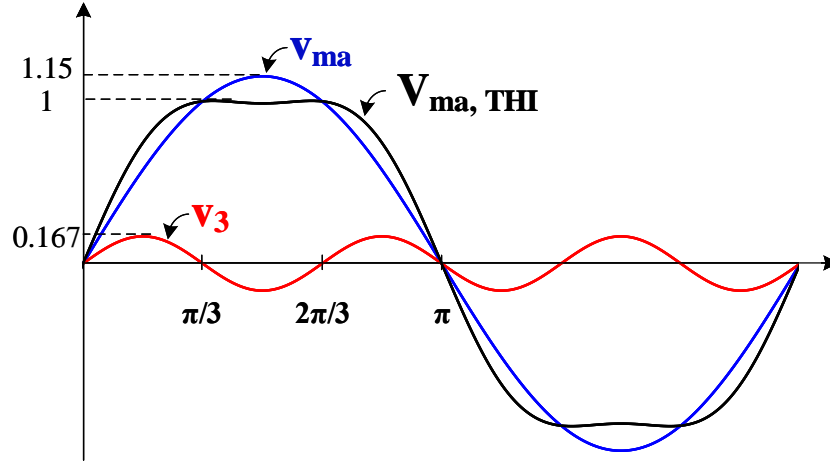


Figure 2.7: Phase A modulating signal for THISPWM.

In order to stay within the linear modulation, the peak of the THISPWM modulating signals are equal to 1 at the maximum modulation index. At  $\frac{\pi}{3}$ , the maximum modulation index ( $m_{a,max,THI}$ ) calculated using equation (2.1.5) is 1.155. And the inverter line to line voltage is increases by 15.5% compared to SPWM, while the THD is not increased [21].

### Space Vector Pulse Width Modulation

SVPWM has become the industry standard for traction inverter control. Compare with SPWM, SVPWM requires intensive computation with a fast, reliable, and precise DSP controller for the digital implementation of this modulation technique [22].

From Figure 2.1, if we use letter P to denote the upper switch in a leg is ON,

and letter O to denote the upper switch is OFF. Then the three upper switches in the three legs of the inverter will give us eight switching states as shown in 2.2. For example, for the switching state of  $[OPO]$ , top switch in leg A ( $S_1$ ) is OFF, leg B top switch ( $S_3$ ) is ON, and top switch in leg C  $S_5$  is OFF. Note for the switching state of  $[OOO]$  and  $[PPP]$ , the top switches of all three legs are OFF and ON respectively. And this results in a open circuit in all 3 inverter legs, and the inverter output 3-phase voltages is 0. In contrast, the rest of the six switching states enable the inverter to produce 3-phase voltages at the output. The eight switching states can be represented by eight stationary vectors in the vector diagram as shown in Figure 2.8. The two switching states ( $[OOO]$  and  $[PPP]$ ) that produces zero output voltage forms two zero vectors that are located in the center. The rest of the six switching states form six active vectors that are  $60^\circ$  out of phase with each other. These six active vectors forms a hexagon in the space vector diagram, and the hexagon is divided into six sectors (Sector I to Sector VI). Each sector is enclosed by two active vectors and the zero vectors are located in the center.

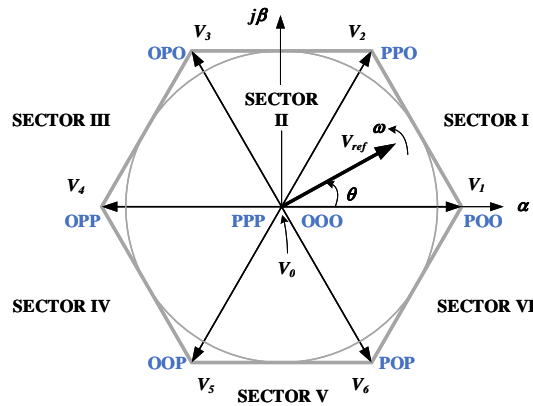


Figure 2.8: Space vector diagram of a 2-level VSI.

Table 2.2: SVPWM space vectors and switching states

Space Vector		Switching States	On-state Switch
Zero Vector	$V_0 = 0$	$[PPP]$	$S_1, S_3, S_5$
		$[OOO]$	$S_2, S_4, S_6$
Active Vector	$V_1 = \frac{2}{3} V_{DC} e^{j0}$	$[POO]$	$S_1, S_4, S_6$
	$V_2 = \frac{2}{3} V_{DC} e^{j\frac{\pi}{3}}$	$[PPO]$	$S_1, S_3, S_6$
	$V_3 = \frac{2}{3} V_{DC} e^{j\frac{2\pi}{3}}$	$[OPO]$	$S_2, S_3, S_6$
	$V_4 = \frac{2}{3} V_{DC} e^{j\frac{3\pi}{3}}$	$[OPP]$	$S_2, S_3, S_5$
	$V_5 = \frac{2}{3} V_{DC} e^{j\frac{4\pi}{3}}$	$[OOP]$	$S_2, S_4, S_5$
	$V_6 = \frac{2}{3} V_{DC} e^{j\frac{5\pi}{3}}$	$[POP]$	$S_1, S_4, S_5$

Consider the switching state  $[POO]$  for vector  $V_1$ , when switch  $S_1, S_4, S_6$  is ON, phase A is connected to the positive DC source, phase B and C are connected to the negative of the DC source. considering the inverter is connected to a symmetrical load, then the equivalent circuit is shown in Figure 2.9. From the voltage divider circuit indicates that  $V_{AN} = \frac{2}{3} V_{DC}$ ,  $V_{BN} = V_{CN} = -\frac{1}{3} V_{DC}$ .

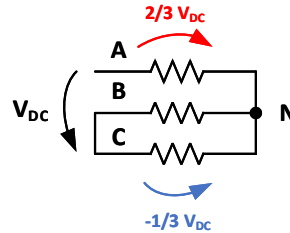


Figure 2.9: Equivalent circuit for switching state POO.

To transform the 3-phase abc phase voltage into the rotating complex space vector, the Clark Transformation is used:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} \quad (2.1.6)$$

The space vector is then calculated using equations:

$$\begin{aligned} V &= V_\alpha + jV_\beta \\ V &= \frac{2}{3} [V_{AN} e^{j0} + V_{BN} e^{j\frac{2\pi}{3}} + V_{CN} e^{j\frac{4\pi}{3}}] \end{aligned} \quad (2.1.7)$$

Where  $e^{jx} = \cos x + j \sin x$

And the vector  $V_1$  can be calculated as:

$$\begin{aligned} V_1 &= \frac{2}{3} \left[ \frac{2}{3} V_{DC} e^{j0} - \frac{1}{3} V_{DC} e^{j\frac{2\pi}{3}} - \frac{1}{3} V_{DC} e^{j\frac{4\pi}{3}} \right] \\ V_1 &= \frac{2}{3} V_{DC} e^{j0} \end{aligned} \quad (2.1.8)$$

The rest of the active vectors can be calculated using the same equations, and they are summarized in Table 2.2.

The output of the PI controllers in Figure 2.3 is the reference dq voltage  $V_{d,ref}$  and  $V_{q,ref}$ . Using the inverse Park Transformation, the dq voltage references can be transformed in to its  $\alpha\beta$  values:

$$\begin{bmatrix} V_{\alpha,ref} \\ V_{\beta,ref} \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} V_{d,ref} \\ V_{q,ref} \end{bmatrix} \quad (2.1.9)$$

Where  $\theta$  is the reference electrical angle. The reference vector in Figure 2.8 can be calculated using equation:

$$V_{ref} = V_{\alpha,ref} + jV_{\beta,ref} \quad (2.1.10)$$

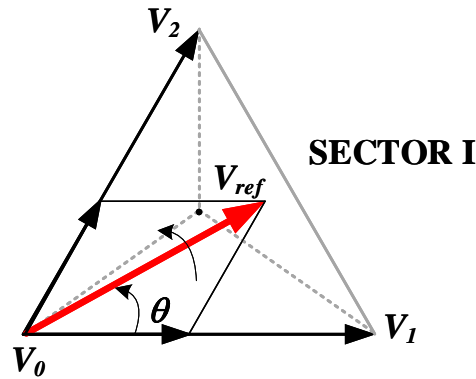


Figure 2.10: Reference vector in Sector I.

The reference vector rotates in the complex space with an angular speed of  $\omega = 2\pi f_e$ , where  $f_e$  is the inverter output voltage fundamental frequency. The voltage reference vector can be reconstructed on the average by using the eight possible switching states of the inverter. The reconstruction is done by sampling the reference voltage at a given period  $T_s$  and computing periods of time to be in certain states so that on the average, the reference voltage is attained. At each sector, the reference voltage can be approximated by using the two adjacent active vectors and the zero vectors. In Figure 2.10, the reference voltage within a sampling period at sector I is

reconstructed using equations:

$$V_{ref}T_s = V_1T_a + V_2T_b + V_0T_0 \quad (2.1.11)$$

$$T_s = T_a + T_b + T_0$$

Where  $T_s$  is the sampling period,  $T_a$ ,  $T_b$  and  $T_0$  are the dwell time for voltage vector  $V_1$ ,  $V_2$  and  $V_0$ . The dwell time at Sector I can be calculated using equations:

$$T_a = \frac{\sqrt{3}T_s V_{ref}}{V_d} \sin\left(\frac{\pi}{3} - \theta\right)$$

$$T_b = \frac{\sqrt{3}T_s V_{ref}}{V_d} \sin(\theta) \quad 0 \leq \theta \leq \frac{\pi}{3} \quad (2.1.12)$$

$$T_0 = T_s - T_a - T_b$$

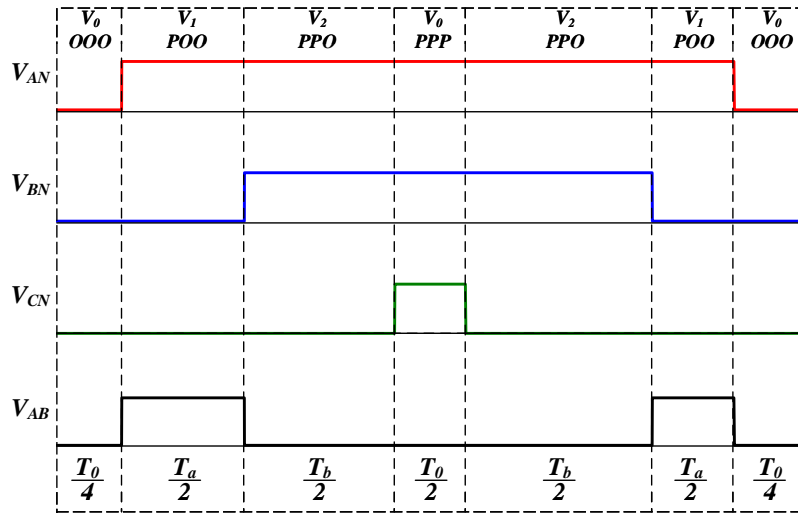


Figure 2.11: Seven-segment switching sequence in Sector I.

The switching sequence shall be designed to minimize the number of switching per sampling period [23]. Figure 2.11 illustrates a typical seven-segment switching sequence in Sector I. The switching sequence within a sampling period is:  $V_0 \rightarrow V_1 \rightarrow$

$V_2 \rightarrow V_0 \rightarrow V_2 \rightarrow V_1 \rightarrow V_0$ . The transition from each segment to the next only requires two switches in the same leg to be turned ON and OFF [24]. For example, from the first segment to the second, only the top switch from inverter phase A leg is switched ON, and the bottom switch is switched OFF. Table 2.3 summarizes the seven-segment switching sequence for all six sectors. Note that in the odd number of sectors, the lower number of the two adjacent vector is selected first, but in the even number of sectors, the higher number vector is selected first. For example, in Sector I,  $V_1(POO)$  is selected before  $V_2(PPO)$ ; in Sector II,  $V_3(OPO)$  is selected before  $V_2(POO)$ . By selecting vectors in this way, the number of switching per sampling period in the even number of sectors are minimized.

Table 2.3: Seven-segment switching sequence for all six sectors

Sector	Space Vector						
	1	2	3	4	5	6	7
I	OOO	POO	PPO	PPP	PPO	POO	OOO
II	OOO	OPO	PPO	PPP	PPO	OPO	OOO
III	OOO	OPO	OPP	PPP	OPP	OPO	OOO
IV	OOO	OOP	OPP	PPP	OPP	OOP	OOO
V	OOO	OOP	POP	PPP	POP	OOP	OOO
VI	OOO	POO	POP	PPP	POP	POO	OOO

When the end of the reference vector in Figure 2.8 is right on the circle, the modulation index is maximum, which equals to 1. At maximum modulation index, the maximum output line-to-line RMS voltage using SVPWM is  $V_{AB,max,SVM} = 0.707V_{DC}$ ,

and compare with SPWM, this is 1.155 times larger, which is equivalent to 3rd order harmonic injection in SPWM method [25].

## 2.2 Multi-level Inverters

### 2.2.1 Structures of Multi-Level Inverters

Multi-level voltage source inverters (MLVSI) has greatly increased in popularity in recent years [26, 27, 28], and they utilize array of switches and capacitors to generates multi-level voltage output. Due to the voltage and current limits of semiconductors, MLVSI has been developed in order to reach high voltage and high power with available devices, and improve the quality of output voltages [29]. It has been widely adopted in the high-power converters and medium-voltage drives [30],[31]. The MLVSI is able to operate at high efficiency when the motor operates at low speed and low torque, unlike the convectional 2-level VSI that usually have an efficiency worse than 70% at this condition. The vehicles also benefit from lighter and thinner cables, lower weight, lower manufacturing cost, higher power throughput, faster charging, and more efficient motors. In a comparison of cost, MLVSI is usually more expensive due to the higher number of components. However, considering the savings in the cost of battery, filters, and heatsink results in an almost equal price compare with 2-level VSI. In terms of reliability, although the higher number of components increases the failure rate, the intrinsic fault-tolerance of MLVSI structures compensates for the low reliability

There are four major categories of multi-level VSI as shown in Table 2.4. The



Neutral Point Clamped Multi-level was first developed in 1973 [32], and the diode-clamped inverter was first introduced in early and mid 1990s [33]. Cascaded H Bridge (CHB) is a good solution for applications require separate DC sources [34], but to extract separate connections from the battery pack in a electric vehicle is not feasible [35]. The control for CHB needs to take in consideration of balancing the inverter cells, which increases the control complexity [36, 37]. The flying Capacitor (FC) inverters was first introduced in 1992. In order to produce  $n$  levels, the FC generally requires  $3(n-1)$  number of capacitors. FC offers low THD, but the biggest drawback is the large number of capacitors, and a complex pre-charging circuit and voltage balancing control algorithm is required to balance the capacitors voltage [38, 39]. Comparing the space, weight and complexity of control, NPC and ANPC are more suitable for traction application [40].

Compare with 2-level VSI, MLVSI is able to operate with higher voltage and power, but the control and voltage balancing problem is inherent to MLVSI [41]. The detailed comparison between them is discussed in Chapter 3. In this section, the 3-level Neutral Point Diode Clamped VSI and 3-level Neutral Point Active Clamped is discussed in details.

Table 2.4: Four categories of multi-level voltage source inverter

Multi-level Voltage Source Inverter			
1. Flying Capacitor (FC)	2. Neutral Point Clamped (NPC)	3. Cascaded	4. Hybrid
Stacked FC	Diode Clamp	Cascaded H Bridge (CHB)	NPC+CHB
	Active Clamp	Asymmetric CHB	Cascade NPC Bridge
	T-type	Modular Multi-level Converter (MMC)	

### 3-Level Neutral Point Clamped Inverter

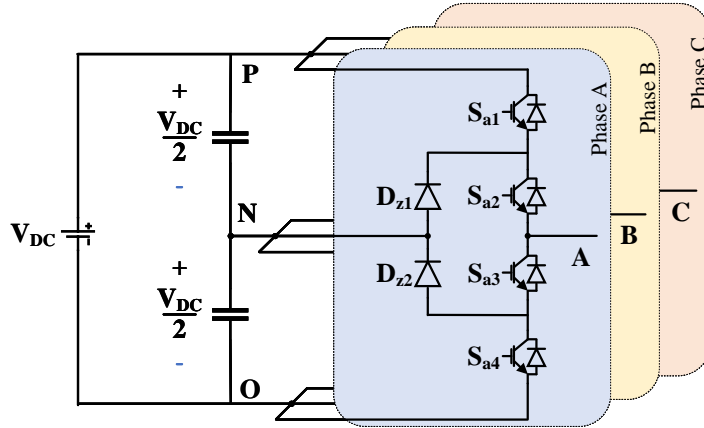


Figure 2.12: Structure of 3-level NPC.

A 3-level Neutral Point Clamped (3LNPC) inverter is shown in Figure 2.12. Two conventional 2-level half bridge cells are stacked together to form a NPC phase leg, and two clamping diodes are connected to the neutral point. It consists of 12 switches and 6 diodes in total, and each leg has 4 switches and 2 clamping diodes [42]. There are two DC-link capacitors in a 3L-NPC, one is connected between the positive (P) and the neutral (N), and the other one is connected between N and the negative (O). Each capacitor has half of the DC-link voltage ( $\frac{V_{DC}}{2}$ ) across it. Due to the structure and control limitation of the inverter, the NPC has intrinsically uneven loss and current distribution for each switch on the phase leg. The DC-link neutral point voltage balancing is still a major concern and considered as a disadvantage from a control standpoint. The voltage level at the neutral point can significantly fluctuate when the voltage across the two capacitors are not balanced. This causes over voltage stress on the semiconductors and capacitors [43].

Inner switch  $S_{a2}$  and  $S_{a3}$  in Figure 2.12 experiences more stress than the two outer switches within in a sampling period. The uneven power loss distribution each switching device in NPC may limit the system power capacity and decrease system reliability. The power loss of each switching device in 3-level NPC is derived in [44].

### 3-Level Active Neutral Point Clamped Inverter

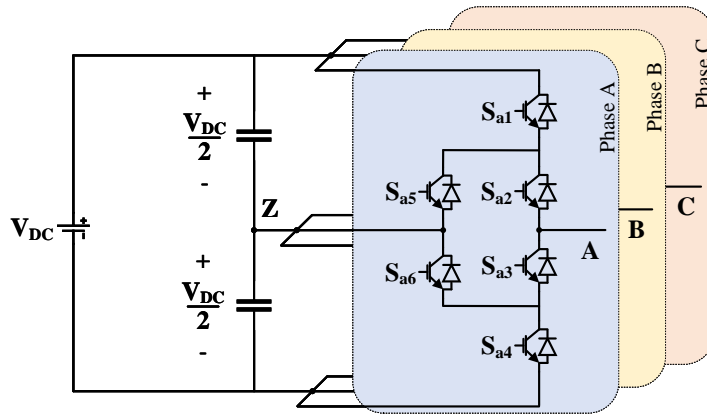


Figure 2.13: Structure of 3-level ANPC.

A 3-level Active Neutral Point Clamped (ANPC) inverter is shown in Fig. 2.13, where the clamping diodes in the NPC are replaced by fully controlled switches (i.e., MOSFET or IGBT) [45]. It consists of 18 switches in total, and each leg has 6 switches. Compare with NPC, the problem with the uneven stress distribution for each switch can be solved by a proper control.

### High-level Neutral Point Clamped Inverter

The structure of 4-level and 5-level NPC is shown in Figure 2.14. In general, for a  $m$ -level NPC, there are  $6(m-1)$  number of switches,  $3(m-1)(m-2)$  clamping diodes,

and  $(m - 1)$  DC capacitors. The number of components increases substantially with the voltage levels, and the inverter structure becomes very complex. The voltage balancing issue is almost unattainable with higher level. 3-level NPC is widely used in medium-voltage (MV) industries, while the practical use of 4 or higher level NPC inverters are not common [46].

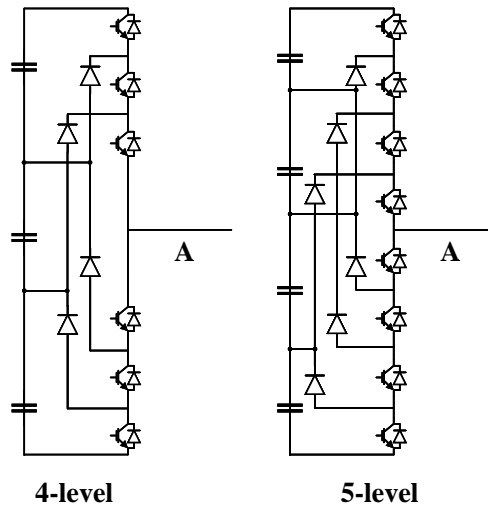


Figure 2.14: Structure of 4-level and 5-level NPC.

## 2.2.2 Control of Multi-Level Inverters

In this section, two popular SPWM techniques and SVPWM technique are discussed.

### In-phase Disposition Pulse Width Modulation

In-phase Disposition (IPD) is a carrier based level-shifted SPWM technique [47]. In-phase Disposition for 3-level NPC is shown in Figure 2.15, the two carrier waves ( $V_{cr1}$  and  $V_{cr2}$ ) are in phase.  $V_{cr1}$  is level shifted by  $+0.5$ , and the signal goes from 0 to

1;  $V_{cr2}$  is level shifted by  $-0.5$ , and the signal goes from 0 to -1. The three sinusoidal modulation waves ( $V_{mA}$ ,  $V_{mB}$  and  $V_{mC}$ ) are 120 degrees out of phase to each other.

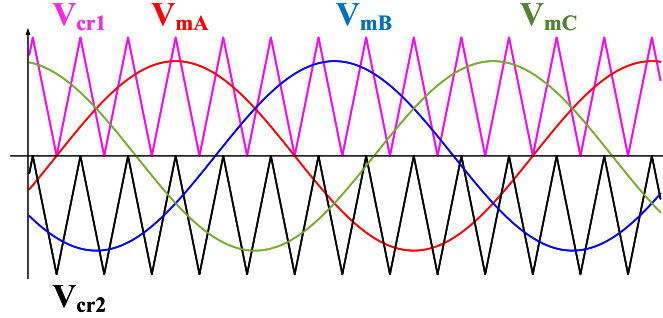


Figure 2.15: IPD SPWM.

Figure 2.16 shows the gating signal generation for inverter phase A leg. The two pairs of complementary switches in leg A are:  $S_{a1}$  and  $S_{a3}$ ;  $S_{a2}$  and  $S_{a4}$ . When the modulating signal  $V_{mA}$  is larger than  $V_{cr1}$ , the top switch  $S_{a1}$  is switched ON, and the bottom switch  $S_{a3}$  is switched OFF. When the modulating signal  $V_{mA}$  is larger than  $V_{cr2}$ , the top switch  $S_{a2}$  is switched ON, and the bottom switch  $S_{a4}$  is switched OFF.

### Alternate-phase Opposition Disposition Pulse Width Modulation

The alternate-phase Opposition Disposition (APOD) is a carrier based level-shifted SPWM technique. APOD for 3-level NPC is shown in Figure 2.17, the two carrier waves ( $V_{cr1}$  and  $V_{cr2}$ ) are  $180^\circ$  out of phase with each other.  $V_{cr1}$  goes from 0 to 1, and  $V_{cr2}$  goes from 0 to -1. The three sinusoidal modulation waves ( $V_{mA}$ ,  $V_{mB}$  and  $V_{mC}$ ) are 120 degrees out of phase to each other.

Figure 2.18 shows the gating signal generation for inverter phase A leg. When the modulating signal  $V_{mA}$  is larger than  $V_{cr1}$ , the top switch  $S_{a1}$  is switched ON, and the bottom switch  $S_{a3}$  is switched OFF. When the modulating signal  $V_{mA}$  is larger than

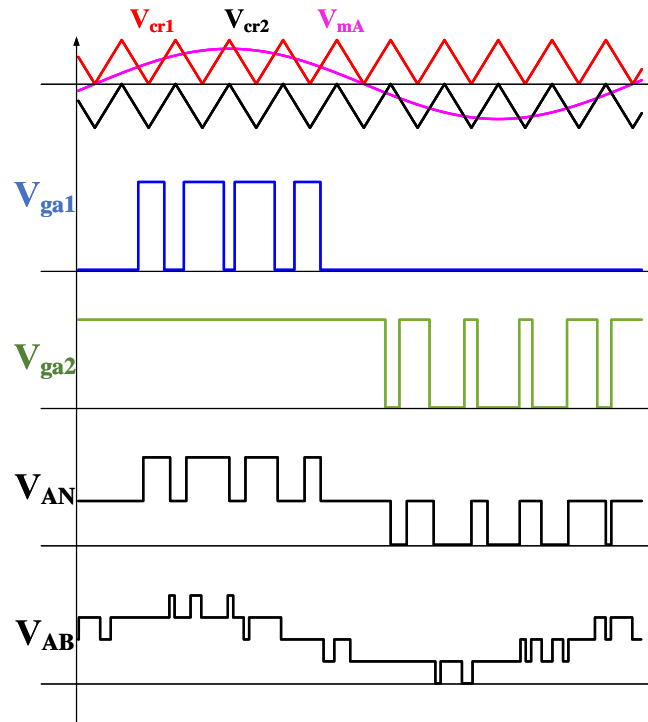


Figure 2.16: IPD SPWM gating signal generation and inverter output voltage.

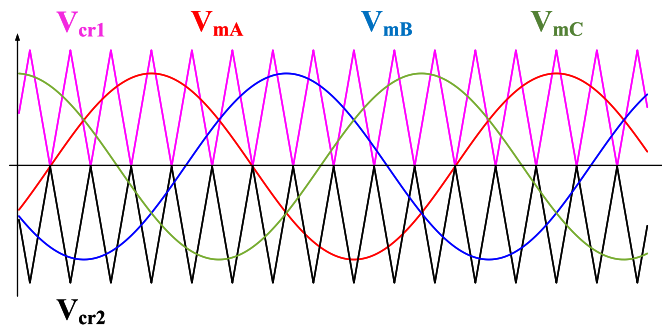


Figure 2.17: APOD SPWM.

$V_{cr2}$ , the top switch  $S_{a2}$  is switched ON, and the bottom switch  $S_{a4}$  is switched OFF. The two pairs of complementary switches in leg A are:  $S_{a1}$  and  $S_{a3}$ ;  $S_{a2}$  and  $S_{a4}$ .

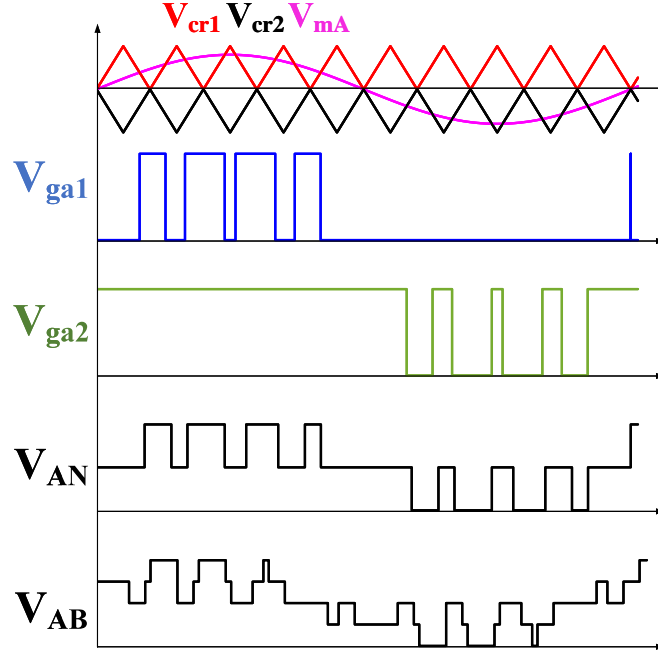


Figure 2.18: APOD SPWM gating signal generation and inverter output voltage.

### Space Vector Modulation of a 3-level NPC Inverter

Three possible switching states for one leg of a NPC is shown in Table 2.5. Compare with the conventional 2-level SVPWM, the 3-level has an extra switching state "O" besides the "P" and "N" [48]. The "O" corresponds to a 0 terminal voltage, while the "P" and "N" produce  $+V_{DC}$  and  $-V_{DC}$  respectively. The space vector diagram is shown in Figure 2.19. There are 27 switching states in 3-level NPC, and they corresponds to 19 active space vectors and 3 Zero space vectors in the sapce vector diagram. These active space vectors are categorized into small vectors, medium vectors, and large vectors based on their magnitude [49]. Zero vector ( $V_0$ ) has three redundant switching states, each small vector ( $V_1 \sim V_6$ ) has two redundant switching states, each medium ( $V_7 \sim V_{12}$ ) and large vector ( $V_{13} \sim V_{18}$ ) only has one switching

states. These redundant switching states have different effect on the neutral point voltage, and it creates the flexibility with voltage balancing at the neutral point [50].

Table 2.5: Switching states of 3-level NPC

Switching State	Device Switching Status in leg A				Terminal Voltage
	$S_{a1}$	$S_{a2}$	$S_{a3}$	$S_{a4}$	
P	ON	ON	OFF	OFF	$V_{DC}$
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	$-V_{DC}$

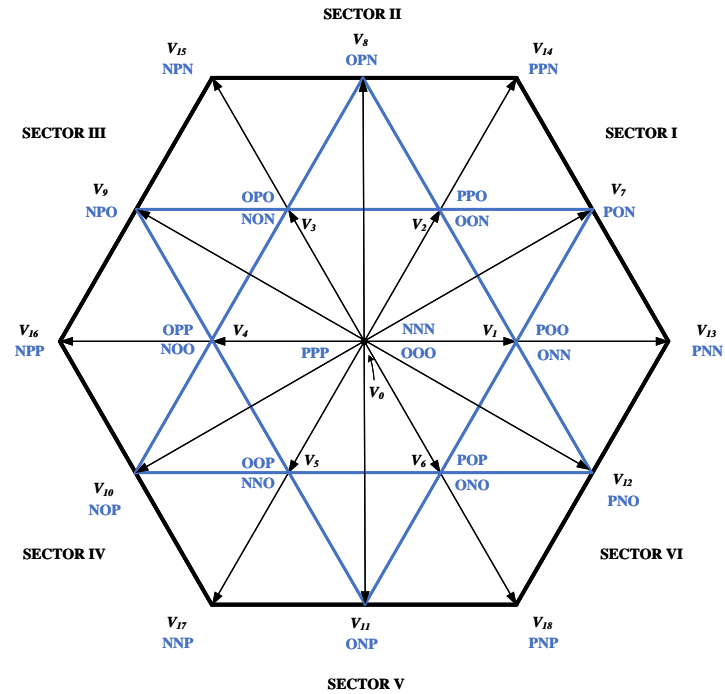


Figure 2.19: Space vector diagram of 3-level inverter.

The space vector diagram is divided into six sectors (Sector I to Sector VI), and each sector is divided into 4 regions. The four regions in Sector I are shown in Figure 2.20. At each sector, the reference voltage can be approximated by using the three adjacent active vectors. When the reference vector falls into region 3 as shown in



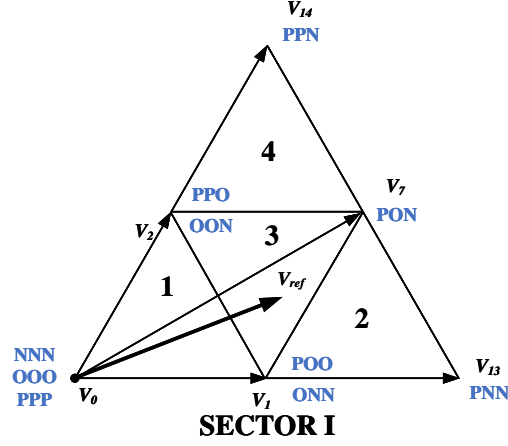


Figure 2.20: Space vectors of 3-level inverter in Sector I.

Figure 2.20, active vectors  $V_1$ ,  $V_2$  and  $V_7$  can be selected to estimate  $V_{ref}$ . Based on the volt-second balancing principle, the following equations can be concluded:

$$\begin{aligned} V_1 T_a + V_7 T_b + V_2 T_c &= V_{ref} T_s \\ T_a + T_b + T_c &= T_s \end{aligned} \quad (2.2.1)$$

Where  $T_a$ ,  $T_b$ ,  $T_c$  are the dwell time for vectors  $V_1$ ,  $V_7$  and  $V_2$  respectively. The dwell time can be calculated using the following equations:

$$\begin{aligned} T_a &= T_s [1 - 2m_a \sin(\theta)] \\ T_b &= T_s [-1 + 2m_a \sin(\frac{\pi}{3} + \theta)] \\ T_c &= T_s [1 - 2m_a \sin(\frac{\pi}{3} - \theta)] \\ m_a &= \sqrt{3} \frac{V_{ref}}{V_{DC}} \end{aligned} \quad (2.2.2)$$

Where  $m_a$  is the modulation index. In the  $\alpha - \beta$  plane,  $V_{ref}$  can be expressed as:

$$\begin{aligned} V_{ref} &= V_\alpha + jV_\beta \\ V_\beta &= V_{ref}\sin(\theta) \\ V_\alpha &= V_{ref}\cos(\theta) \end{aligned} \tag{2.2.3}$$

Solving equations 2.2.2 and 2.2.3, the dwell time can be expressed as:

$$\begin{aligned} T_a &= T_s \left[ 1 - \frac{2\sqrt{3}V_\beta}{V_{DC}} \right] \\ T_b &= T_s \left[ -1 + \frac{3}{V_{DC}} \left( V_\alpha + \frac{V_\beta}{\sqrt{3}} \right) \right] \\ T_c &= T_s \left[ 1 - \frac{3}{V_{DC}} \left( V_\alpha - \frac{V_\beta}{\sqrt{3}} \right) \right] \end{aligned} \tag{2.2.4}$$

To simplify the expression, we can define the following variables:

$$\begin{aligned} X &= \frac{2\sqrt{3}V_{ref}}{V_{DC}} \\ Y &= \frac{3}{V_{DC}} \left( V_\alpha + \frac{V_\beta}{\sqrt{3}} \right) \\ Z &= \frac{3}{V_{DC}} \left( V_\alpha - \frac{V_\beta}{\sqrt{3}} \right) \end{aligned} \tag{2.2.5}$$

And the dwell time in Sector I region 3 can be simplified as:

$$\begin{aligned} T_a &= (1 - X)T_s \\ T_b &= (-1 + Y)T_s \\ T_c &= (1 - Z)T_s \end{aligned} \tag{2.2.6}$$

The dwell time for all four of the regions are summarized in Table 2.6.

Table 2.6: Switching states of 3-level NPC

Region	$T_a$		$T_b$		$T_c$	
1	$V_0$	$(1 - Y)T_s$	$V_2$	$XT_s$	$V_1$	$ZT_s$
2	$V_1$	$(2 - Y)T_s$	$V_7$	$XT_s$	$V_{13}$	$(-1 + Z)T_s$
3	$V_1$	$(1 - X)T_s$	$V_7$	$(-1 + Y)T_s$	$V_2$	$(1 - Z)T_s$
4	$V_2$	$(2 - Y)T_s$	$V_{14}$	$(-1 + X)T_s$	$V_7$	$ZT_s$

Small and medium vectors have effects on the voltage level at the Neutral point, while zero and large vectors has no effect. The effect of smaller vectors have the dominant effect, and it can be categorized as P-type and N-type small vectors [51]. Selecting the P-type small vector will cause the neutral point voltage  $V_Z$  to rise, while the N-type makes it to decline. The effect of medium vectors is undefined, therefore only the small vectors are used for voltage balancing. To minimize the effect of small vectors on the neutral-point voltage deviation, the dwell time shall be divided evenly for N-type and P-type small vectors during a sampling period [52]. In the same time, the switching transition from one switching state to the next one shall only involve two switches, and the transition for  $V_{ref}$  moving from one sector (or one region) to the next one requires minimum numbers of switching [53], [54].

There are two cases for the 7-segment switching sequence design. Case 1 is when the reference voltage is in region 2 or 4. There are only one small vector within these two regions, and the dwell time of the switching states should be distributed evenly for selecting the P-type and N-type small vectors. For example, when  $V_{ref}$  is in region 4 of Sector I, the three vectors selected are  $V_2$ ,  $V_7$  and  $V_{14}$ . The total dwell time for  $V_{2P}$  (PPO) and  $V_{2N}$  (OON) should be both  $\frac{T_c}{2}$ . And the switching sequences is:  $V_{2N} \rightarrow V_7 \rightarrow V_{14} \rightarrow V_{2P} \rightarrow V_{14} \rightarrow V_7 \rightarrow V_{2N}$ . This satisfies the rules mentioned above.

Case 2 is when the reference voltage is in region 1 or 3. There are two small vectors within these two regions. As shown in Figure 2.21, the two regions can be further divided into 4 subregions  $1_a$ ,  $1_b$ ,  $3_a$ ,  $3_b$ . When the reference vector is in region  $1_a$  or  $3_a$ , the dwell time of  $V_1$  is larger than  $V_2$  ( $T_a > T_c$ ), and  $V_1$  is referred to as dominant small vector. The dwell time is equally divided between  $V_{1P}$  and  $V_{1N}$  to minimize the voltage deviation [55], [56]. For example, when  $V_{ref}$  is in region  $3_a$  of Sector I, the total dwell time for  $V_{1P}$  (POO) and  $V_{1N}$  (ONN) should be both  $\frac{T_a}{2}$ , and the switching sequence is:  $V_{1N} \rightarrow V_{2N} \rightarrow V_7 \rightarrow V_{1P} \rightarrow V_7 \rightarrow V_{2N} \rightarrow V_{1N}$ .

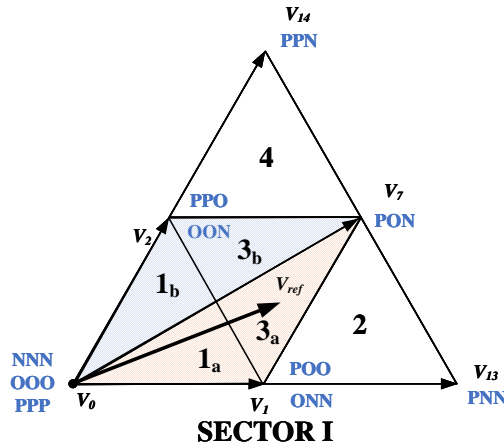


Figure 2.21: Region 1 and 3 in Sector I.

The switching sequence for all of the regions in Sector I is summarized in Table 2.7. It can be seen the transition from region  $1_a$  to  $1_b$ , only one switching is required to switch from ONN to OON. And the transition from region  $1_b$  to  $2_b$ , no switching is required. Thus, this switching sequence satisfies the rules mentioned above.

Table 2.7: 7-segment switching sequence in Sector I

Segment	$1_a$		$1_b$		$3_a$		$3_b$		2		4	
1	$V_{1N}$	ONN	$V_{2N}$	OON	$V_{1N}$	ONN	$V_{2N}$	OON	$V_{1N}$	ONN	$V_{2N}$	OON
2	$V_{2N}$	OON	$V_0$	OOO	$V_{2N}$	OON	$V_7$	PON	$V_{13}$	PNN	$V_7$	PON
3	$V_0$	OOO	$V_{1P}$	POO	$V_7$	PON	$V_{1P}$	POO	$V_7$	PON	$V_{14}$	PPN
4	$V_{1P}$	POO	$V_{2P}$	PPO	$V_{1P}$	POO	$V_{2P}$	PPO	$V_{1P}$	POO	$V_{2P}$	PPO
3	$V_0$	OOO	$V_{1P}$	POO	$V_7$	PON	$V_{1P}$	POO	$V_7$	PON	$V_{14}$	PPN
2	$V_{2N}$	OON	$V_0$	OOO	$V_{2N}$	OON	$V_7$	PON	$V_{13}$	PNN	$V_7$	PON
1	$V_{1N}$	ONN	$V_{2N}$	OON	$V_{1N}$	ONN	$V_{2N}$	OON	$V_{1N}$	ONN	$V_{2N}$	OON

### SVPWM algorithm of 3-level NPC Inverter

During each sampling period, the sector and region of the reference voltage is first calculated, then the dwell time is calculated based on the position of the reference vector. And finally the switching sequence is selected.

To determine the sector for the reference voltage, the following equation can be used [23]:

$$N = \text{sign}(V_\beta) + 2\text{sign}\{V_\alpha \sin(60^\circ) - V_\beta \sin(30^\circ)\} + 4\text{sign}\{V_\alpha - \sin(60^\circ) - V_\beta \sin(30^\circ)\} \quad (2.2.7)$$

Where  $\text{sign}$  is the Signum function, and  $N$  is the variable used to determine the sector number. The sector number can be determined based on the following look-up table:

Table 2.8: Sector loop-up table

Sector	I	II	III	IV	V	VI
N	3	1	5	4	6	2

To determine the regions of reference vector in any sector, the following equations

can be defined:

$$\begin{aligned}
 a &= \text{sign}\left\{\frac{V_{DC}}{3} - V_{\alpha} - \frac{\sqrt{3}}{3}V_{\beta}\right\} \\
 b &= \text{sign}\left\{-\frac{V_{DC}}{3} + V_{\alpha} - \frac{\sqrt{3}}{3}V_{\beta}\right\} \\
 c &= \text{sign}\left\{V_{\beta} - \frac{\sqrt{3}}{6}V_{DC}\right\}
 \end{aligned} \tag{2.2.8}$$

And the regions can be determined based on the following loop-up table:

Table 2.9: Region loop-up table

Region	a	b	c
1	1 or 0	–	–
2	-1	1 or 0	–
3	-1	-1	1 or 0
4	-1	-1	-1

After the position of the reference is determined, the dwell time and switching sequence can be determined using Table 2.6 and Table 2.7.

### Modulation scheme of 3-level ANPC

There are two neutral current paths presents in the 3-level ANPC. The first one is formed by  $S_2$  and  $S_5$ , and the other one is formed by  $S_3$  and  $S_6$ . The neutral point voltage can be clamped by taking these two current paths [57]. There are four popular modulation schemes for 3-level ANPC, and each one utilizes a unique current path to clamp the neutral voltage [58]. The gating signals for each switch under the four modulation schemes are shown in Figure 2.22. The complementary switch pairs are different for each scheme, and the current stress is also different.

Figure 2.22a shows the Diode-clamped ANPC (DNPC) modulation scheme. The inverter simply operates as a 3-level NPC in this case. Switch  $S_5$  and  $S_6$  will be kept

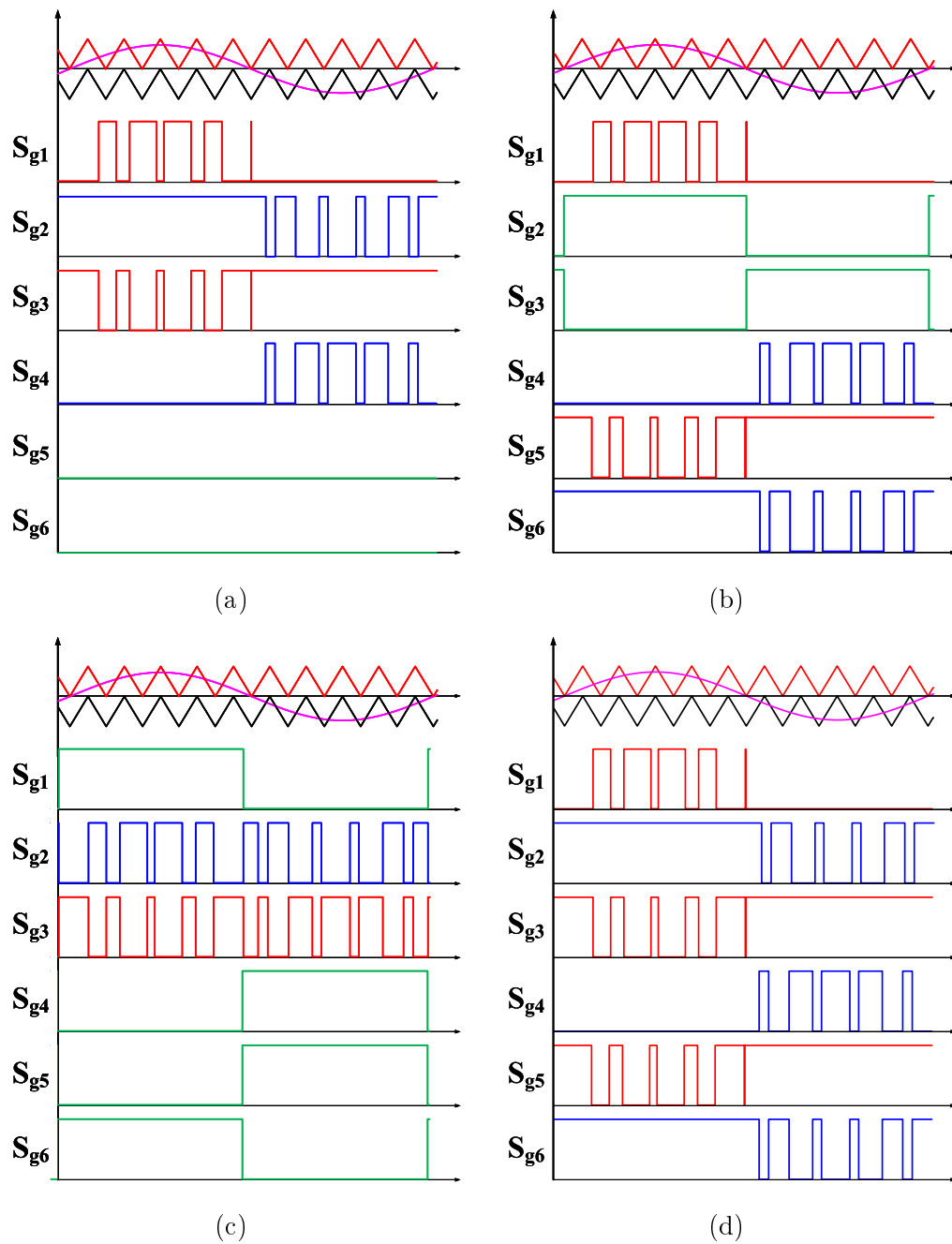


Figure 2.22: The gating signals for four popular modulation schemes: (a) Diode-clamped ANPC modulation scheme, (b) Same-side modulation scheme, (c) Opposite-side modulation scheme, and (d) Full-path modulation scheme.

OFF at all time, and the neutral current passes through their anti-parallel diodes instead.  $S_1$  and  $S_3$  forms a complementary switch pair, and  $S_2$  and  $S_4$  forms another pair. For the positive half cycle of the inverter,  $S_1$  and  $S_3$  are operating at the switching frequency while  $S_2$  is kept at ON and  $S_4$  is kept at OFF. This is reversed for the inverter negative half cycle. The neutral current path is determined by the load current direction. Switch  $S_1$  and  $S_3$  generates both switching losses during the positive half cycle, but for the negative half cycle,  $S_3$  generates mostly conduction while  $S_1$  generates no loss since it is being turned OFF. This unbalanced current stress also applies to the other complementary switch pair, just like the 3-level NPC.

Figure 2.22b shows the Same-side clamping (SSC) modulation scheme. The three complementary switch pairs are:  $S_1$  &  $S_5$ ,  $S_2$  &  $S_3$ , and  $S_4$  &  $S_6$ . Switch  $S_2$  and  $S_3$  operates at line frequency while the rest of the switches operate at the switching frequency for each half cycle.  $S_2$  and  $S_3$  generates mostly conduction loss, while the rest switches generates both switching loss and conduction losses.  $S_5$  and  $S_6$  experience the most stress since they are kept ON for half of the cycle while their complementary switches are kept OFF. For SSC, ANPC takes the top neutral current path for the upper cell commutation, and the bottom neutral current path for the lower cell commutation.

Figure 2.22c shows the Opposite-side clamping (OSC) modulation scheme. The OSC complementary switch pair is the same as SSC.  $S_2$  and  $S_3$  operates at switching frequency for the entire time, while the rest of the switches operates at line frequency the entire time. The OSC choice of neutral path is opposite as SSC. For OSC, ANPC takes the bottom neutral current path for the upper cell commutation, and the upper neutral current path for the lower cell commutation.



Figure 2.22d shows the Full-path clamping (FPC) modulation scheme. The upper and lower neutral current path is utilized together in parallel at the neutral switching state for the FPC. The switching pattern for  $S_3$  and  $S_5$  is the same, and in complementary to  $S_1$ ; the switching pattern for  $S_2$  and  $S_6$  is the same, and in complementary to  $S_4$ .  $S_2$  &  $S_6$  and  $S_3$  &  $S_5$  are kept ON during the neutral switching state, while  $S_1$  and  $S_4$  are kept at OFF. Since all of the switches are operating at the switching frequency for half of the fundamental period, the conduction loss is reduced compare to the rest of the modulation scheme.

## 2.3 Summary

This chapter provides a review on the existing 2-level and multi-level inverter topologies and a comparison of each inverter for traction application. The structure of 2-level VSI, 3-level NPC and ANPC is discussed. The algorithm of SPWM and SVPWM for both 2-level VSI and 3-level NPC and ANPC are discussed in details.

## Chapter 3

# Analysis and Study of 2-Level and 3-Level Voltage Source Inverters for Traction Applications

This chapter presents a comprehensive analysis and comparison between the 2-level VSI, 3-level NPC, and 3-level ANPC inverters in traction inverters. In this comparison Silicon Carbide MOSFET, Gallium Nitride MOSFET and Silicon IGBT are employed. An analytical method for calculating the inverter power loss is also presented. Simulation results are conducted using MATLAB/Simulink and PLECS at different operating conditions. A permanent magnet synchronous motor is used as the load. The analysis and comparison have been conducted at different operating points regarding the speed and torque. The performance of each inverter topology is also investigated at different switching frequencies for these operating conditions. Moreover, two drive cycle analyses are also studied and included in this chapter.

### 3.1 Introduction

Recently, the progress in the development of SiC transistors [59] and GaN devices has brought a wide range of transistors in higher voltage and higher current classes, both in discrete packages and modules [60], [61]. This is due to the increasing demand for high efficiency and high power density traction inverters.

Most of today's traction inverters operate at a 400-800V battery voltage, and the trend is moving to a higher voltage DC-link [62]. 2020 Porsche Taycan and 2020 Aston Martin Rapide E have both adopted 800V DC-link, and many other auto manufactures are following this trend. Higher DC-link voltage enables faster charging time and makes modern electric vehicles more practical for long-range travel. At the same output power, a higher voltage will result in a lower current flowing through the inverter and the motor. A smaller current usually results in a higher inverter and motor efficiency which leads to higher overall efficiency in the powertrain [63]. Moreover, a smaller current allows a smaller conductor size which reduces the system cost and weight. However, a higher DC-link voltage results in higher voltage stress on the semiconductor devices. In recent developments, many conventional 2-level VSI are replaced with 3-level inverters in traction application to reduce the voltage stress on the semiconductor devices and decrease the voltage and current THD [64],[65]. But the 3-level inverter has a more complex structure with more components. Therefore, the inverter cost is usually higher for the 3-level inverter [66], [67]. A review of the multilevel inverter structures and control techniques in electric transportation applications is presented in [68] and [69].

MOSFET has the natural ability to conduct current bidirectionally, while IGBT needs anti-parallel diodes to conduct the current in the reverse direction. Due to the

fact that MOSFETs have lower conduction loss than diodes, the anti-parallel diode with MOSFET only conducts during the dead-time to prevent the shoot-through. On the other hand, the anti-parallel diode with IGBT provides the negative current path for the IGBT. As a result, the total conduction loss using a MOSFET-based inverter is less than that of an IGBT-based inverter. The switches that are chosen in this chapter are summarized in Table 3.1. The voltage ratings of commercially available SiC and GaN MOSFETs are limited to 1700V and 650V, respectively. Connecting multiple SiC and GaN MOSFETs in series can achieve a higher voltage rating. However, it leads to the increased power loss, complexity, cost, as well as reduced reliability. Although GaN devices offer higher efficiency, higher power density, and the ability to operate at higher switching frequencies [70], the current limit for commercially available GaN MOSFETs is 60A. Thus, multiple switches are needed in parallel to achieve a higher current capability.

In this chapter, the 2-level VSI, 3-level NPC and 3-level ANPC inverter topologies will be compared based on the following performance criteria:

1. Number of switching components including the total number of switches and diodes,
2. Switch selection including voltage and current ratings and the cost of the switching devices,
3. Power loss analysis and inverter efficiency,
4. Output line to line voltage and phase current THD.

Table 3.1: Selected switches

Switch Type	Part Name	Manufacture	Voltage Rating (V)	Current Rating (A)	Price (USD)
SiC MOSFET	CAB450M12XM3	CREE	1200	450	\$906
SiC MOSFET	C3M0015065K	CREE	650	120	\$42
Si IGBT	FF450R12KE4P	INFINEON	1200	450	\$110
Si IGBT	FF450R07ME4 B11	INFINEON	650	450	\$153
GaN MOSFET	GS66516B	GaN SYSTEMS	650	60	\$51

## 3.2 Switch Selection

The selection of the switches is based on a traction inverter with the parameters listed in Table 3.2. The performance of each switch is investigated in 10KHz and 100KHz switching frequencies. operating at high switching frequency results in high motor efficiency, fast control response, lower motor torque ripple and smaller filter size [71]. Most of the commercial traction inverter operates at 10-30 KHz switching frequency due to the increase of switching loss at higher switching frequency. The motor parameter is based on a off-the-shelf motor designed by the company BorgWarner [72].

Table 3.2: System Parameters

DC-Link Voltage (V)	$V_{dc}$	800
Rated Output Power (KW)	$P_{out}$	200
Switching Frequency (kHz)	$f_{sw}$	10, 100
PMSM Pole Pair	$P$	5
PMSM d-axis Inductance (mH)	$L_d$	0.88
PMSM q-axis Inductance (mH)	$L_q$	0.88
PMSM Phase Resistance (ohms)	$R_{ph}$	0.03
PMSM Rated Phase Current (Arms)	$I_{rated}$	400

### 3.2.1 Device Voltage rating

In 2-level VSI, the maximum voltage across each switch at steady-state equals the DC-link voltage. However, it is  $\frac{1}{2}$  of the DC-link voltage for 3-level NPC and 3-level ANPC. At transient operation, the parasitic inductances of the busbar, cables, and the DC-link capacitor create a voltage spike at switching-off actions [73]. Consequently, the voltage rating of the switches should be higher than the transient spikes. As a result, for 800V DC-link voltage, 1200V switches are used for 2-level VSI, and 650V switches are used for 3-level NPC and 3-level ANPC.

### 3.2.2 Number of Switches

Table 3.3 summarizes the costs for each 3-level NPC and ANPC inverter option. The price listed includes the semiconductor devices, clamping diodes, and gate drivers. SILICON LABS SI8271AB-ISR is chosen as the gate driver. To estimate the cost of gate drivers, the retail price of the evaluation board is used as a reference. The evaluation board SI8273ISO-KIT is based on the reference design provided in the gate drive IC technical reference manual [74]. The gate driver IC only has the strength to drive a single switch. The evaluation board SI8273ISO-KIT has one gate driver circuitry, and each costs \$28.67 USD.

Single diode with forward current ratings around 450A is generally expensive and bulky. For example, APTDF400U120G from MICROCHIP TECHNOLOGY has a footprint of 62mm by 81mm, and it's priced at \$92 USD. Therefore, 6 of IDW75D65D1 from INFINEON are connected in parallel to achieve a 450A forward current rating. The unit price for the clamping diode is \$4 USD.

For the 2-level VSI, both Si IGBTs and SiC MOSFETs are half-bridge modules.

Table 3.3: Switch Selection for 2-level VSI

Option	Topology	Switch Type	Total Cost (USD)
1	2-Level	1200V SiC MOSFET	\$2,851
2		1200V Si IGBT	\$502
3	NPC	650V SiC MOSFET	\$3,536
4		650V Si IGBT	\$1,779
5		650V GaN MOSFET	\$6,836
6	ANPC	650V SiC MOSFET	\$5,040
7		650V Si IGBT	\$1,893
8		650V GaN MOSFET	\$9,954

Each inverter uses 1 switch module at each leg, and 3 switch modules in total.

Options 3 to 5 in Table 3.3 are for NPC. The 650V Si IGBT is in half-bridge modules with 450A current rating. Thus, 2 Si IGBT modules are used per phase and, hence, 6 modules for the 3-phases. The SiC and GaN MOSFETs are in discrete packages. To satisfy the rated system phase current of 400A, multiple discrete SiC and GaN switches are required to be connected in parallel to increase the current capability. The current capability of each 650V SiC MOSFET is 120A, and 4 of such switches are connected in parallel to achieve 480A of current capability. The current capability of each 650V GaN MOSFET is 60A, and 7 of such switches are connected in parallel to achieve 420A current capability. In practice, connecting 4 or 7 discrete switches in parallel is impractical, but for the sack of comparison, this configuration is analysed in theory. As the technology evolves, the current limit of semiconductors will become larger and larger. The total number of discrete SiC MOSFETs used in option 3 is 48; the total number of Si IGBT modules used in option 4 is 6; the total number of GaN MOSFETs used in option 5 is 84.

Options 6 to 8 in Table 3.3 are for ANPC. The total number of discrete SiC MOSFETs used in option 6 is 72; the total number of Si IGBT modules used in

option 7 is 9; the total number of GaN MOSFETs used in option 8 is 126.

As it can be noticed from Table 3.3, the most expensive option is ANPC using GaN; the second is NPC using GaN; the third is ANPC using SiC. The cheapest option is 2-level VSI using 1200V IGBT.

### 3.3 Power Loss Calculation

Fig. 3.1 shows the current and voltage waveforms of a switch during a switching period. Where  $v_{sw}$  is the voltage across the switch and  $i_{sw}$  is the current going through the switch.  $I_{on}$  is the average phase current of the inverter and  $V_{on}$  is the switch turn-on voltage.

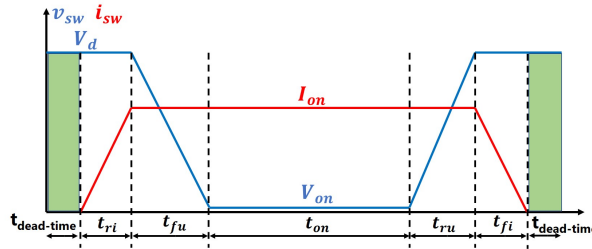


Figure 3.1: Switch voltage and current transient during a switching period.

#### 3.3.1 Switch Power Loss

##### Switching Loss

During switch turn on period, switch current first rises from 0 to  $I_{on}$ , and then voltage drops from  $V_d$  to  $V_{on}$ . During switch turn off period, voltage first rises from  $V_{on}$  to  $V_d$ , and then currents drops from  $I_{on}$  to 0. The switch turn-on time  $T_{on}$  and turn off



time  $T_{off}$  are calculated as follow:

$$\begin{aligned} T_{on} &= t_{ri} + t_{fu} \\ T_{off} &= t_{ru} + t_{fi} \end{aligned} \quad (3.3.1)$$

Where  $t_{ri}$  is the current rise time,  $t_{fu}$  is the voltage fall time,  $t_{ru}$  is the voltage rise time, and  $t_{fi}$  is the current fall time. The switching energy of the device is calculated as:

$$E_{sw} = 0.5V_d i_{on}(T_{on} + T_{off}) \quad (3.3.2)$$

Average switching power loss ( $P_{sw}$ ) is the product of switching energy ( $E_{sw}$ ) and switching frequency ( $f_{sw}$ ):

$$P_{sw} = E_{sw} f_{sw} \quad (3.3.3)$$

From the device datasheet, the switching energy is usually given as a function of current at a specific junction temperature ( $T_1$ ) and the blocking voltage ( $V_C$ ). The switching energy at any temperature and voltage ( $E_{v1}(T_j)$ ) is calculated as [75]:

$$\begin{aligned} E_{v1}(T_j) &= \beta \frac{E_{sw}(T_1, V_2) V_1}{\alpha V_2} \\ \beta &= a_1 T_j^2 + b_1 T_j + c_1 \\ \alpha &= a_2 T_j^2 + b_2 T_j + c_2 \end{aligned} \quad (3.3.4)$$

Where  $\alpha$  is the voltage coefficient;  $\beta$  is the temperature coefficient and  $a_1, b_1, c_1, a_2, b_2, c_2$  can be obtained through curve fitting.

### Conduction Loss

The average switch conduction loss is calculated as:

$$P_{cond} = I_{on} V_{on} \frac{t_{on}}{T} \quad (3.3.5)$$

Where  $\frac{t_{on}}{T}$  is the duty cycle. It is assumed that the switch current during the conduction period is constant. The current value  $I_{on}$  is used to estimate  $V_{on}$  from the datasheet. This relation is given by the device datasheet at two junction temperatures  $T_1$  and  $T_2$ . The voltage at any temperature ( $V_{on}(T_j)$ ) can be calculated using the weighted average method:

$$V_{on}(T_j) = V_{on}(T_2) \frac{T_1 - T_j}{T_1 - T_2} + V_{on}(T_1) \frac{T_j - T_2}{T_1 - T_2} \quad (3.3.6)$$

### 3.3.2 Diode Power Loss

#### Conduction Loss

The average diode conduction loss  $P_{D,cond}$  is calculated as:

$$P_{D,cond} = V_f I_f t_{dead-time} \quad (3.3.7)$$

Where  $V_f$  is the diode forward voltage;  $I_f$  is the diode forward current and  $t_{dead-time}$  is the switch dead-time. The same weighted average method from equation 3.3.6 can be used to calculate the diode voltage at any junction temperature.

### Reverse Recovery Loss

The reverse recovery energy of the diode is calculated as:

$$E_{rr} = 0.25Q_{rr}|V_B| \quad (3.3.8)$$

Where  $Q_{rr}$  is the reverse recovery charge and  $V_B$  is the maximum negative voltage across the diode during diode turn-off. The diode reverse recovery energy ( $E_{rr}$ ) can be found in the device datasheet at specific currents. The diode reverse recovery power loss is calculated as:

$$P_{rr} = E_{rr}f_{sw} \quad (3.3.9)$$

On the device datasheet, the diode reverse recovery energy is usually given as a function of current at a specific junction temperature and voltage. The same method from equation 3.3.4 can be used to calculate the diode reverse recovery energy at any temperature and voltage.

## 3.4 Simulation Results

The inverter models are built in MATLAB/Simulink and used to calculate the output THD. The loss is calculated in PLECS using the manufacturer device datasheet. SPWM modulation is used for 2-level VSI and IPD PWM modulation is used for NPC and ANPC.

In 2-level VSI, currents going through each of the switches are identical; power loss and generated heat are intrinsically balanced across each switch in the same inverter leg. However, it is not balanced for 3-level NPC and 3-level ANPC. During

the positive phase A current,  $S_{a2}$  and  $S_{a3}$  generate mostly conduction loss and low switching loss due to the lagging current. The power losses of the clamping diodes and switches  $D_{z1}$ ,  $D_{z2}$ ,  $S_{a5}$ ,  $S_{a6}$  are evenly distributed.

The simulation is run at four motor operating conditions: low-speed low-torque, low-speed high-torque, high-speed low-torque and high-speed high-torque. The performance of each topology listed in Table 3.3 is investigated at 10kHz and 100kHz switching frequencies.

At motor low speed and low torque conditions, the speed and torque of the motor are 300RPM and 100Nm respectively, and the results are shown in Fig. 3.2a. At 10kHz switching frequency, both 3-level ANPC using SiC MOSFET and using GaN MOSFET produce efficiency over 99%, and SiC MOSFET has slightly better efficiency. 2-level inverter using Si IGBT has the worst efficiency of 84.8%. At 100kHz switching frequency, 3-level ANPC using GaN MOSFETs has the best efficiency. Both of the 2-level options produce low efficiency at high switching frequency, and the Si IGBT option only has an efficiency of 34%.

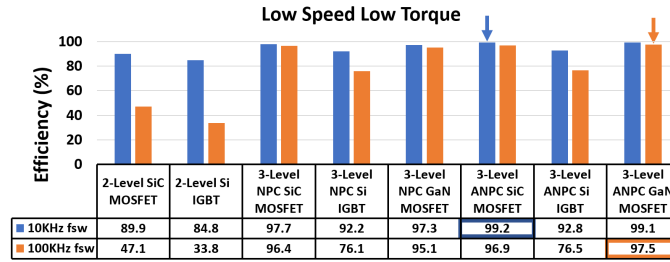
At motor low speed and high torque condition, the speed and torque of the motor are 300RPM and 800Nm respectively, and the results are shown in Fig. 3.2b. The results are similar to the low speed and low torque condition. The 3-level ANPC using SiC MOSFETs and GaN MOSFETs are the two most efficient options at 10kHz and 100kHz switching frequencies respectively. The 2-level inverter using Si IGBTs is not able to sustain a reasonable junction temperature at 100kHz switching frequency, thus its efficiency is not recorded. As seen from the results, 2-level VSI is very inefficient at high switching frequency.

At motor high speed and low torque condition, the speed and torque of the motor are 2000RPM and 100Nm, respectively. The results are shown in Fig. 3.2c. At 10kHz switching frequency, 3-level ANPC using both SiC MOSFETs and GaN MOSFETs produce efficiency over 99.8%, and SiC MOSFET has slightly better efficiency. At 100kHz switching frequency, the 3-level NPC using SiC MOSFET has the best efficiency at 99.4%.

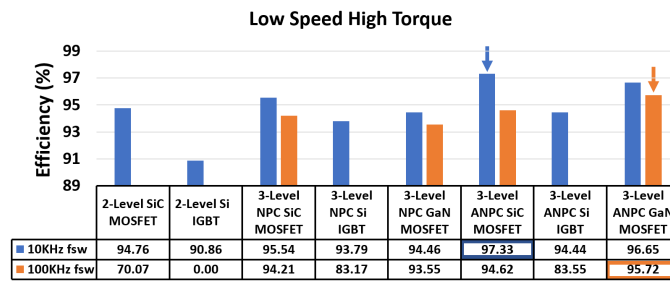
At motor high speed and high torque condition, the speed and torque of the motor are 2000RPM and 800Nm, respectively, and the results are shown in Fig. 3.2d. All of the options offer great efficiency above 95%, except for the 2-level inverter using Si IGBTs at 100 kHz, which only has an efficiency of 69.4%. The two most efficient options at 10kHz and 100kHz switching frequencies are the 2-level VSI using SiC MOSFETs and 3-level NPC using SiC MOSFETs, respectively.

It can be seen from the results that all of the 3-level options using SiC and GaN MOSFETs offer efficiencies higher than 93% at all motor conditions and at both high and low switching frequencies.

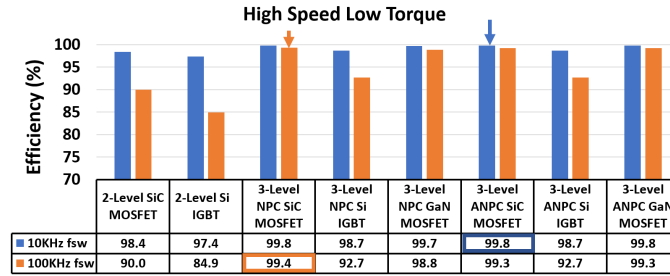
At 10kHz switching frequency, the average loss of clamping diode is large than the active switch. By replacing the clamping diodes with the active switches in 3-level NPC, the 3-level ANPC results in a better efficiency. At 100kHz switching frequency, the switching loss of the active switches is increased significantly, and the efficiency of 3-level ANPC is almost equal to or slightly higher than the 3-level NPC.



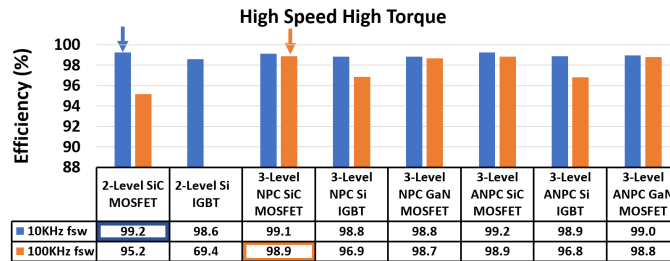
(a)



(b)



(c)



(d)

Figure 3.2: Efficiency results for each inverter topology at 10kHz and 100kHz under four motor operating conditions: (a) motor low speed and low torque, (b) motor low speed and high torque, (c) motor high speed and low torque, and (d) motor high speed and high torque.

### 3.4.1 Drive Cycle Simulation

#### Drive Cycle Simulink Model

A 2015 Spark EV system-level model is developed in MATLAB/Simulink as shown in Fig. 3.3. The model consists of multiple blocks including driver, motor control, motor, final drive, wheel, chassis and battery. The parameters of the vehicle are provided by Argon National Laboratory (ANL)[76], and they are listed in Table 3.4.

Table 3.4: 2015 Spark EV Parameters

Vehicle Mass ( $K_g$ )	1432	Motor Inertia ( $K_g * m^2$ )	0.05
Tire Radius ( $m$ )	0.2945	Battery Capacity ( $Ah$ )	54
Final Drive Raio	3.9	Vehicle Height ( $m$ )	1.59
Final Drive Inertia ( $K_g * m^2$ )	0.01	Vehicle Length ( $m$ )	1.41
Ratio of Vehicle Mass on Driven Axles	0.64	Aerodynamic Drag Coefficient ( $N_s^2/K_g * m$ )	0.326

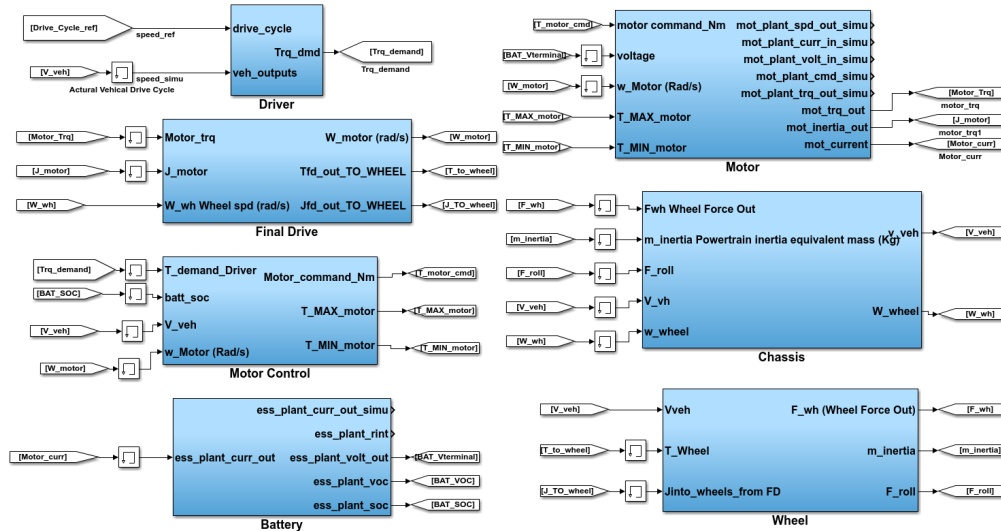


Figure 3.3: Drive Cycle Simulink block.

The vehicle reference speed and the sample time is stored in a look-up table. The data is sampled every 0.02 seconds. The reference speed is converted to meters per

second and then feed to the Driver block.

The Driver block is shown in Figure 3.4. Inside the driver block is a simple PID controller. The error between the reference speed and the feed-back simulated speed is feed into the PID controller, and the output is the torque requested by the driver. The requested torque is then feed into the motor control block.

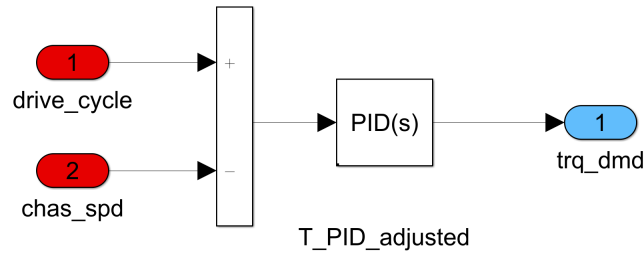


Figure 3.4: Driver Simulink block.

The Motor Control block is shown in Figure 3.5. Two speed-torque curve of the motor is stored in a look-up table, and the maximum and minimum torque is calculated depending on the vehicle speed. The requested torque from the driver is split into propelling torque and break torque. The propelling torque is limited to the no slip torque and maximum torque at the current speed. The brake torque is a combination of friction breaking and regenerative braking. The regenerative brake torque is limited by the motor minimum torque.

The Motor block is shown in Figure 3.6. The efficiencies of the motor and inverter is stored in two efficiency tables. The efficiency is calculated based on the motor speed and torque. The propelling and regenerative power is calculated and saturated by the mechanical power. Motor current is calculated based on the electrical power and battery terminal voltage.



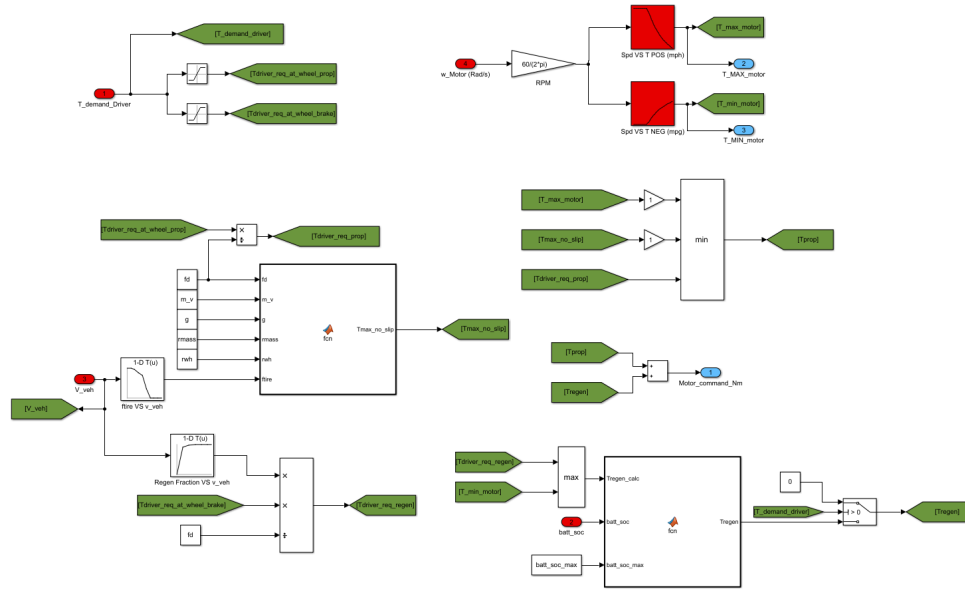


Figure 3.5: Motor Control Simulink block.

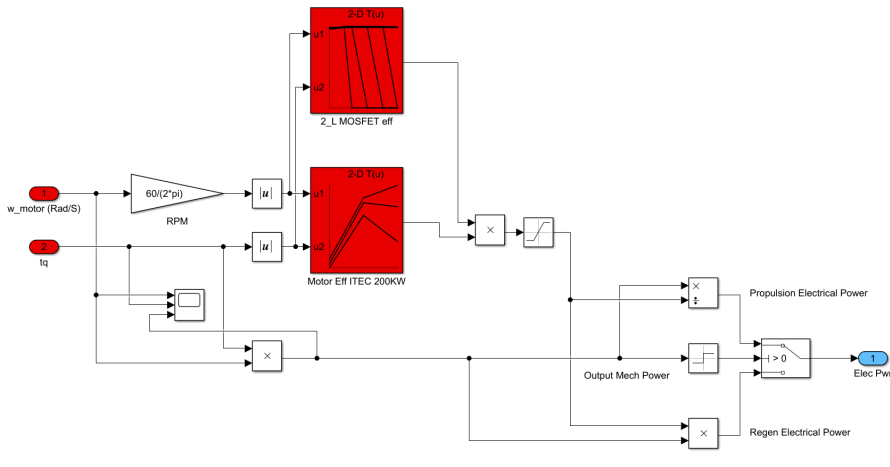


Figure 3.6: Motor Simulink block.

The Final Drive block is shown in Figure 3.7. In this block, the motor speed, torque to wheel and final drive inertia is calculated based on the final drive ratio.

The Wheel block is shown in Figure 3.8. In this block, the wheel force and rolling

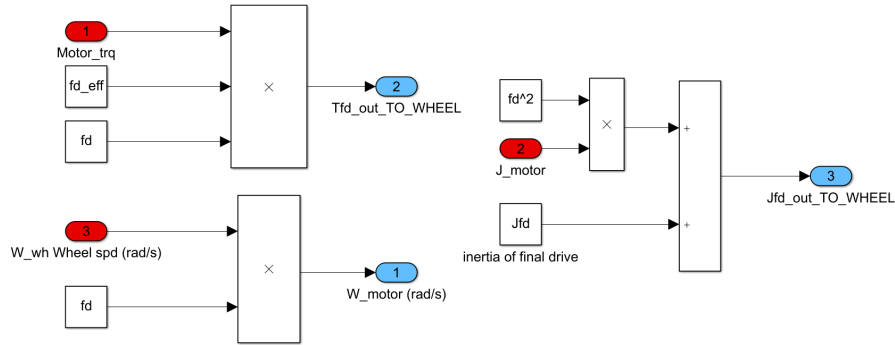


Figure 3.7: Final Drive Simulink block.

force is calculated by dividing torque by the size of the wheel.

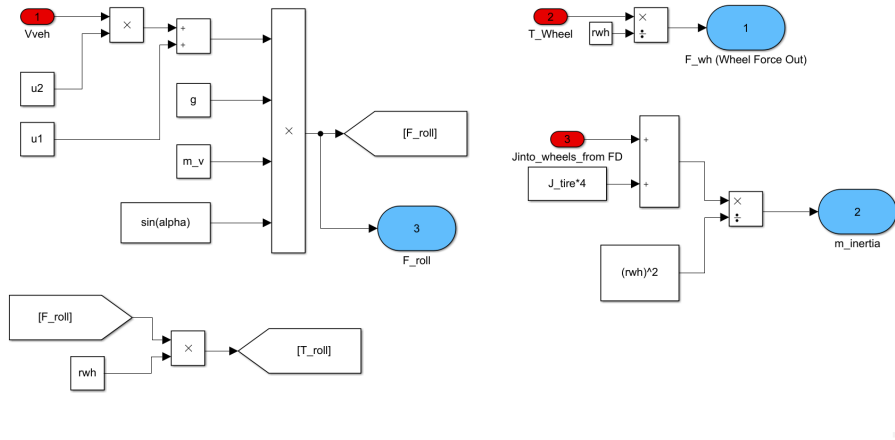


Figure 3.8: Wheel Simulink block.

The Chassis block is shown in Figure 3.9. The rolling force, grade force and aero force is calculated as the total loss. The net force is calculated and speed is calculated based on the Newton’s law through a integrator.

The Battery block is shown in Figure 3.10. Battery SOC is calculated based on the battery current, battery capacity and initial SOC. The charging and discharging resistance from the equivalent battery model is calculated based on the look-up tables.

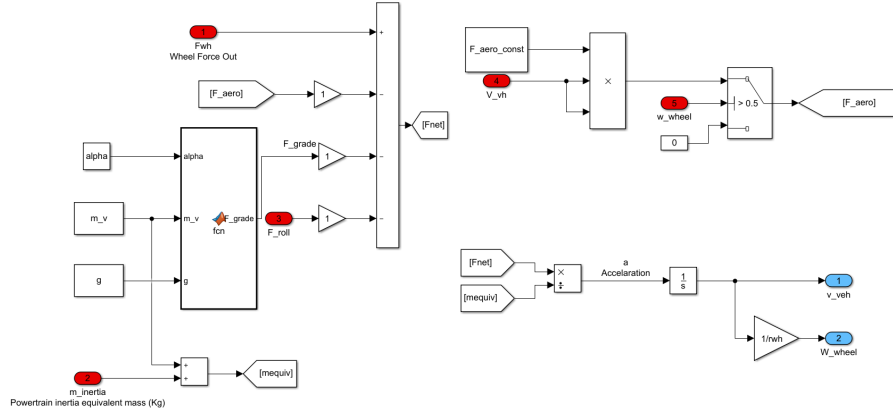


Figure 3.9: Chassis Simulink block.

Battery Open Circuit Voltage (OCV) is also calculated based on the battery SOC-OCV curve. The battery terminal voltage is calculated based on the OCV and voltage across the equivalent resistance.

## Drive Cycle Simulation Results

The motor in the model is replaced with the 200kW motor in Table 3.2, and the model is tuned so that the vehicle driving behaviour matches the experimental data provided by ANL. The motor and motor drive are modelled as efficiency maps and stored as 3D look-up tables. The input of the 3D look-up tables are motor speed and torque, and the output is the efficiency. To analyze the efficiency of each inverter topology listed in Table 3.3, the battery state-of-charge (SOC) for each drive cycle is recorded. Two standard drive cycles are used for this simulation: Urban Dynamometer Driving Schedule (UDDS) and Highway Fuel Economy Test (HWFET). For each of the drive cycle simulations, the switching frequency is set to 100kHz, and the performance of each inverter topology is inspected from the battery SOC at the end of the drive

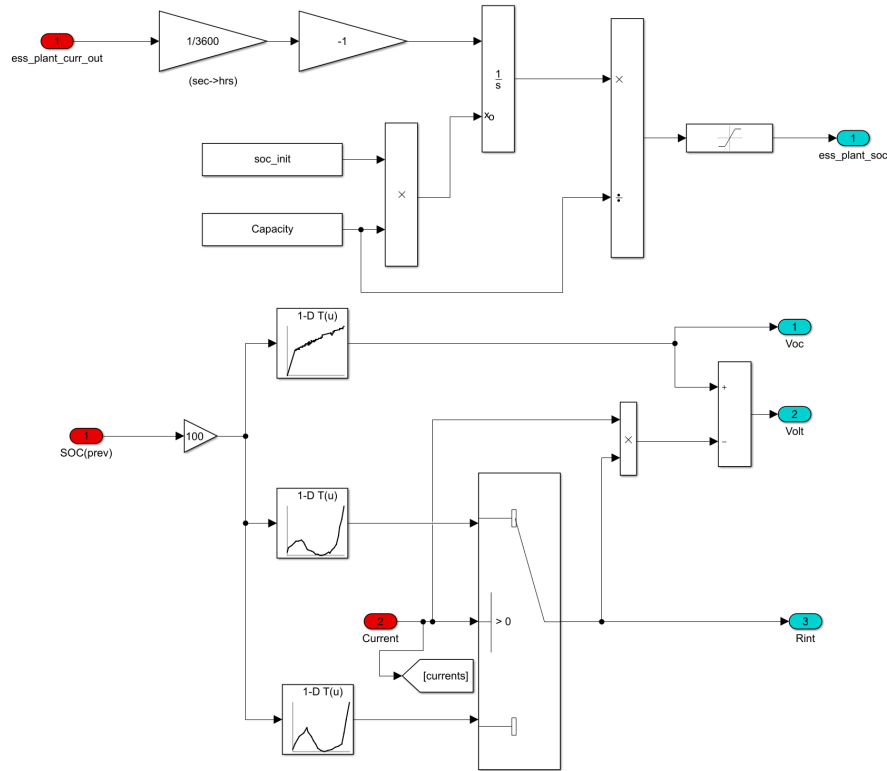


Figure 3.10: Battery Simulink block.

cycle.

The UDDS drive schedule simulates city driving condition [77], and the initial battery SOC is set to 38%. The battery SOC for each inverter topology is shown in Fig. 3.11, and the battery SOC at the end of the simulation for each inverter topology is shown in Table 3.3. ANPC using SiC MOSFETs is the most efficient, and 2-level VSI using Si IGBT is the least efficient. Almost 5% battery capacity can be saved by using ANPC with SiC MOSFETs instead of the 2-level structure with SI IGBTs.

The HWFET drive schedule simulates highway driving with a total driving distance of 10.26 miles, and the average vehicle speed is 48.3 mph. The initial battery

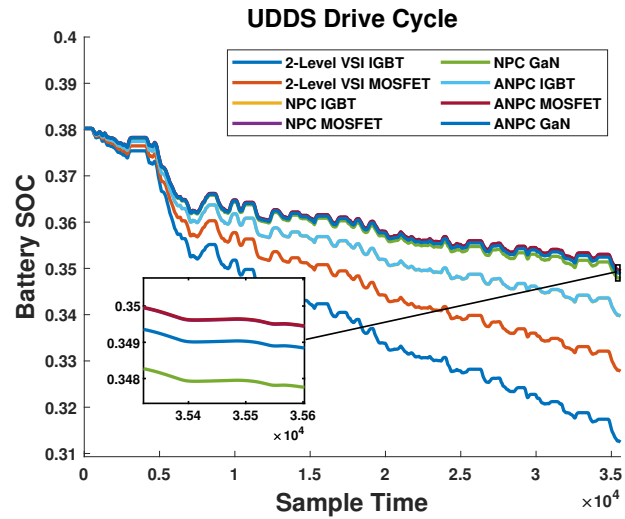


Figure 3.11: Simulation of battery SOC for different topologies in UDDS drive cycle.

SOC is set to 63%. The battery SOC for each inverter topology is shown in Fig. 3.12. NPC using SiC MOSFETs is the most efficient, and 2-level VSI using Si IGBT is the least efficient. Almost 20% battery capacity can be saved by using ANPC with SiC MOSFETS instead of the 2-level structure with SI IGBTs.

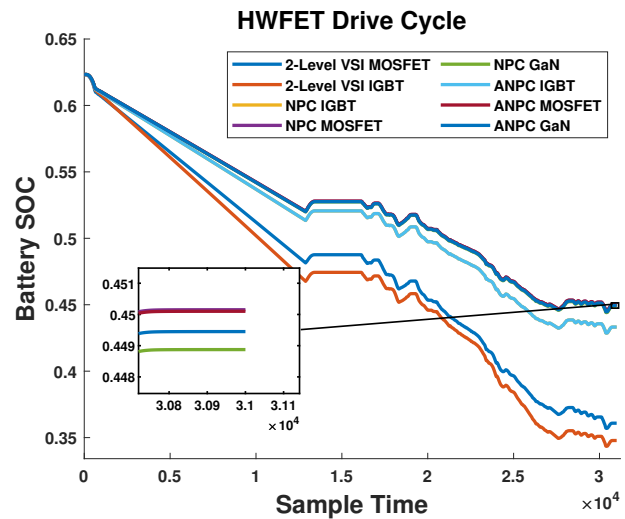


Figure 3.12: Simulation of battery SOC for different topologies in HWFET drive cycle.

The battery SOC at the end of simulation and the SOC drop for the drive cycle for each inverter topology are shown in Table 3.5. All of the multilevel inverters have significant advantages over the 2-level VSI for both city and highway driving. ANPC and NPC have similar efficiency for both of the drive cycles at 100kHz switching frequency as shown in Figure 3.2. The SOC drop for ANPC is slightly lower than NPC for all three type of switches. The 2-level VSI with IGBT has the worst efficiency for both drive conditions.

Table 3.5: Battery SOC at the end of simulation and SOC drop for the drive cycle

Inverter Topology	Switch Type	UDDS		HWFET	
		Final SOC	$\Delta SOC$	Final SOC	$\Delta SOC$
2-Level	1200V SiC MOSFET	33.026%	4.974%	36.085%	26.915%
	1200V Si IGBT	31.513%	6.487%	34.782%	28.218%
NPC	650V SiC MOSFET	35.159%	2.841%	45.015%	17.985%
	650V Si IGBT	34.194%	3.806%	43.318%	19.682%
	650V GaN MOSFET	34.995%	3.005%	44.887%	18.113%
ANPC	650V SiC MOSFET	35.161%	2.839%	45.011%	17.989%
	650V Si IGBT	34.201%	3.799%	43.321%	19.679%
	650V GaN MOSFET	35.102%	2.898%	44.945%	18.055%

### 3.4.2 Inverter Output Current and Voltage THD Simulation

The total harmonic distortion (THD) of the output phase current and line to line voltage is shown in Table 3.6.

As can be seen from the results, both the current and voltage THD for the 3-level inverters are lower than the 2-level VSI. The difference of current THD is not significant, and both the 2-level VSI and the 3-level inverter offer reasonably low output current THD at all operating conditions. However, the voltage THD is improved by 33% to 50% by using the 3-level inverter.

Table 3.6: Output THD comparison

Motor Condition	Inverter Topology	Current THD (%)	Voltage THD (%)
Low Speed Low Torque	2 Level 10kHz	2.8	321
	3 Level 10kHz	2.3	214
	2 Level 100kHz	2.2	421
	3 Level 100kHz	0.94	217
Low Speed High Torque	2 Level 10kHz	0.44	255
	3 Level 10kHz	0.37	166
	2 Level 100kHz	0.3	273
	3 Level 100kHz	0.21	172
High Speed Low Torque	2 Level 10kHz	6.49	87.1
	3 Level 10kHz	2.94	41.3
	2 Level 100kHz	2.13	86.3
	3 Level 100kHz	1.26	41.3
High Speed High Torque	2 Level 10KHz	1.16	62.6
	3 Level 10kHz	0.75	32.6
	2 Level 100kHz	0.34	76
	3 Level 100kHz	0.2	34.2

### 3.5 Summary

An overview of the performance for each 2-level, 3-level NPC and 3-level ANPC inverters are shown in Fig. 3.13, and is summarized as follow:

1. The 3-level NPC and ANPC have lower output THD than 2-level VSI due to the additional output voltage levels.
2. The 2-level VSI with SiC MOSFETs offers the best inverter efficiency when the motor operates at high torque and low switching frequency. When the motor operates at low speed, ANPC with SiC has the best efficiency at both low and high switching frequencies. ANPC with GaN has the best efficiency when the motor is operating at high torque and with a high inverter switching frequency.
3. The 3-level inverter has additional switching devices compared to 2-level VSI.

When a fault occurs to a switch in a 3-level inverter, the inverter is still able to operate as a 2-level VSI, and the low readability caused by the additional components can be compensated by this property.

4. The system cost of the 3-level inverter is more than 2-level VSI. NPC and ANPC have uneven power loss distribution across each active switching component and the cooling system needs to incorporate it. Additional gate drivers, DC-link capacitors and larger, more complex busbars also increase the system cost.
5. The blocking voltage of any switch in the 2-level inverter is equal to the DC-link voltage, while it is  $\frac{1}{2}$  of the DC-link voltage for the 3-level structures.
6. The 3-level NPC and ANPC can save more battery energy compare with the 2-level VSI.

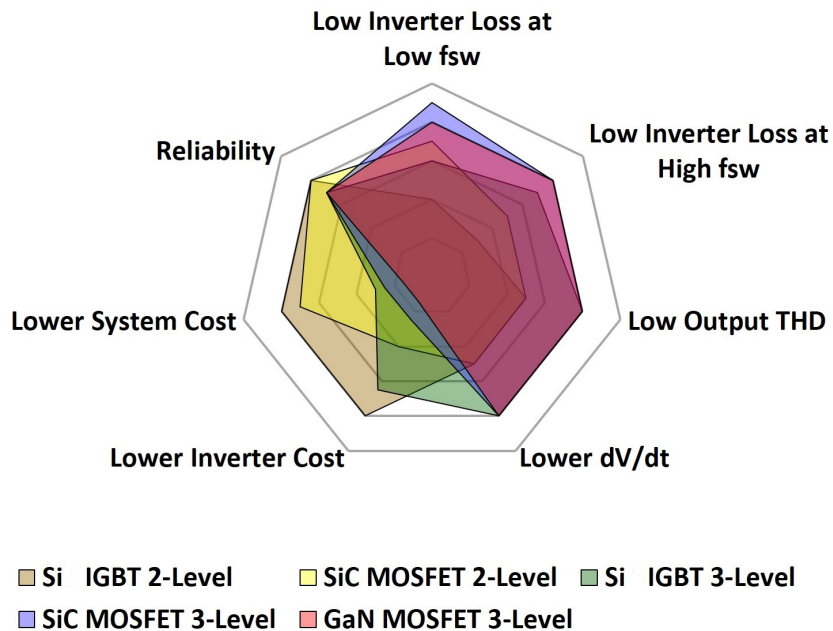


Figure 3.13: Performance overview of different inverter topologies.



## Chapter 4

# Design of a 70kW 3-Level Active Neutral Point Clamped (ANPC) Inverter for Traction Applications

### 4.1 Introduction

The advantage of 3-level NPC and ANPC is discussed in Chapter 3. The inverter efficiency and output THD of the 3-level topologies are improved significantly compared to the conventional 2-level VSI. The average loss of the active switches in ANPC is lower than the clamping diodes in NPC at 10kHz of switching frequency, and the resulting efficiency of the ANPC is higher than NPC. The active switches in ANPC creates flexibility in the capacitor voltage balancing, and the uneven loss distribution problem inherited from NPC can also be improved by using ANPC as discussed in Chapter 2. Due to the reasons mentioned above, a 3-level ANPC is chosen for prototyping.

In this Chapter, the detailed design procedure of a 70kW 3-level ANPC is discussed. The specifications of the inverter is listed in Table 4.1. The minimum DC-link voltage of the inverter is 800V, and the design will be capable for 900V. The continuous power rating of the inverter is 70kW, and the 10 second overload power rating is 120kW. The first section will discuss the component selection, and followed by the design and simulation of the proposed design.

Table 4.1: ANPC Inverter Parameters

DC-link Voltage	$V_{DC}$	800V
Continuous Power Rating	$P_{continuous}$	70kW
Overload Power Rating (10 second)	$P_{overload}$	120kW
Load Power Factor	pf	0.9
Inverter Housing Ambient Temperature	$T_{amb}$	100°C

## 4.2 Components Selection

### 4.2.1 Switch Selection

Based on the inverter parameters listed in Table 4.1, the maximum output line-to-line voltage  $V_{AB,max,svm}$  can be calculated using the equation:

$$\begin{aligned} V_{AB,max,svm} &= 0.7V_{DC} \\ &= 560V \end{aligned} \tag{4.2.1}$$

Consider the load power factor as 0.9, the output rms phase current ( $I_{rms}$ ) using SVPWM can be calculated using the equations:

$$I_{rms} \cos\phi = \frac{P}{\sqrt{3}V_{AB}} \tag{4.2.2}$$

Where  $P$  is the output power. Using the equations above, the rms current at continuous and overload power rating are 109A and 188A respectively. For ANPC, the voltage across each switch is half of the DC-link voltage. During the switching off transition, the stray inductance present in the communication loop causes voltage overshoot across the switches. And the voltage rating of the switches needs to be large enough to prevent breakdown due to the voltage overshoot. The voltage rating for all of the selected switches are larger than 650V.

Around 30 off-the-shelf semiconductor products are summarized and compared. Due to the package size, only discrete switches are considered. Most of the power modules has a large package size, and using those will decrease the power density of the inverter dramatically. From the analysis discussed in Chapter 3, SiC and GaN MOSFETs are considered to get the best possible inverter efficiency. The short-list of the best candidates are shown in Table 4.2 [78, 79, 80, 81, 82, 83]. Those switches are from companies like Cree, Infineon, ROHM, ST Micro, United SiC and GaN Systems.

Table 4.2: Short list of available switches

Part Number	C3M0015065K	IMZA65R027M1H	SCT3030ALHR	SCTW90N65G2V	UJ4C075018K4S	GS66516T
Total number of switches	18	36	36	36	36	36
Manufacture	CREE	Infineon	ROHM	ST Micro	United SiC	GaN Systems
Technology	SiC MOSFETs	SiC MOSFETs	SiC MOSFETs	SiC MOSFETs	SiC MOSFETs	GaN MOSFETs
Voltage Rating (V)	650	650	650	650	750	650
Current Rating (A)	120	59	70	119	81	60
$R_{ds,ON}$ (mOhms)	15	27	30	18	18	25
Rise time (ns)	32	4.2	41	38	35	12.4
Fall time (ns)	15	8.4	27	16	21	22
Maximum Operating Temperature (C°)	175	150	175	200	175	175
Extended Price (USD)	540	1080	1512	720	610	1512

Some of the important parameters are compared. The drain to source resistance  $R_{ds,ON}$  determines the conduction loss, and larger  $R_{ds,ON}$  will decrease the inverter efficiency [84]. The rise and fall time determines the minimum switching time, and also affects the voltage overshoot [85]. The maximum operating temperature is also

a very important specification, it affects the cooling design and the safety and fault-tolerant of the inverter. UJ4C075018K4S from United SiC is selected for this ANPC inverter. Two of this device is connected in parallel to increase the current capacity. It offers a small  $R_{ds,ON}$ , larger breakdown voltage and at a cheaper price. Another important reason for choosing this product is because it is well stocked on distributors like Digikey. Due to the global pandemic, many products in Table 4.2 are in shortage, and backorder for some of those are as long as 16 months.

#### 4.2.2 Gate Driver Selection

The selected MOSFETs typical output characteristics at  $T_j=175^\circ$  is shown in Figure 4.1, the current capability increases with the increase of gate source voltage  $V_{GS}$ . From the MOSFETs data sheet, the maximum  $V_{GS}$  is 20V. Since the stray inductance in the gate path will cause voltage overshoot, there should be some room left for the  $V_{GS}$ . Therefore 15V is selected for the MOSFETs gate source turn-on voltage.

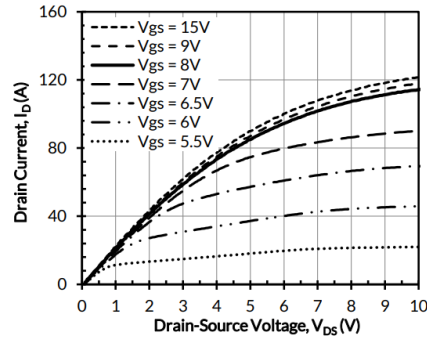


Figure 4.1: UJ4C075018K4S typical output characteristics at  $T_j=175^\circ$ .

The equivalent gate drive circuit can be seen from Figure 4.2.  $R_{GD,int}$  is the gate driver internal pull-up resistance, it has a value of 0.7 ohms from the device datasheet. After the gate output pin, there is a common resistance  $R_{G,com}$  for the

two parallel MOSFETs, and its value is 0.5 ohms. Each MOSFETs also has a gate resistance  $R_{G,ext}$  connected in series with the MOSFETs gate pin, and its value is 0.25 ohms.  $R_{G,com}$  and  $R_{G,ext}$  are placed on the gate driver PCB.  $R_{G,int}$  is the internal gate resistance in the MOSFETs gate pin, and its value is 4.5 ohms. A small gate resistance provides better EMI suppression with high efficiency, and a small delay time, and less switching loss.

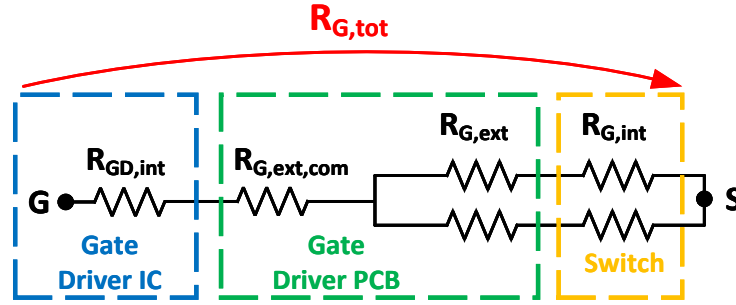


Figure 4.2: Equivalent gate drive circuit.

The peak gate current during turn ON can be calculated using equations:

$$R_{G,Total} = R_{GD,int} + R_{G,com} + \frac{R_{G,ext} + R_{G,int}}{2} = 3.575\text{ohms}$$

$$I_g = \frac{V_{GS}}{R_{G,Total}} = 4.2A \quad (4.2.3)$$

Texas Instruments UCC21750 is chosen for the gate driver [86]. This is a isolated drive with a drive strength of 10A, therefore no output current buffer is required, and the footprint for the gate driver circuitry is reduced. This gate driver IC has the strength to drive any 2 parallel switches from Table 4.2, therefore, if the selected switch needs to be replaced, this gate driver design can be kept as same. It also has

fast DESAT over-current protection with 200ns response time. Some other features includes: input deglitch filter, 4A internal active miller clamp, AEC-Q100 qualified for automotive application and a maximum operating temperature of 150°. The features of the gate driver is summarized in Table 4.3.

Table 4.3: UCC21750 features

Features	Value
Isolation rating	$5.7kV_{rms}$
SiC MOSFETs peak voltage	$2121 V_{pk}$
Drive strength	10A
DESAT protection response time	200 ns
Internal miller clamp current rating	4A
Soft turn-off current during fault	400mA
Reset type	Software reset
Operating junction temperature	-40° to 150°

### 4.2.3 Capacitor Selection

The DC-link capacitor is used to provide low impedance path for high frequency ripple current, to provide reactive power and reduce the emission of the electromagnetic interference [87, 88]. Electrolytic capacitors and film capacitors are commonly used in the inverter DC link. These two types of capacitors have different energy densities and current ripple capabilities [89]. The electrolytic capacitors offer higher capacitance per volume, and they are lower in price. However, their lifetime is shorter than the film capacitors. Many studies have focused on replacing the electrolytic capacitors with film capacitors to improve the system reliability [90, 91].

The techniques for determining the size of the DC-link capacitor for 2-level VSI have been discussed in [92, 93, 94]. Calculating the capacitor sizing for ANPC can be done in a similar way. From the space vector diagram shown in Figure 2.19, at

the maximum modulation index, the ANPC only utilizes large vectors. The capacitor ripple is at maximum and the ANPC operates as a 2-level VSI. In Sector I as shown in Figure 2.20, the two large vectors are  $V_{13}$  (PNN) and  $V_{14}$  (PPN). The equivalent circuits for these two switching states are shown in Figure 4.3. For both switching states, the voltage at the midpoint  $V_Z$  is not affected, both upper capacitor  $C_1$  and lower capacitor  $C_2$  charge and discharge at the same time.

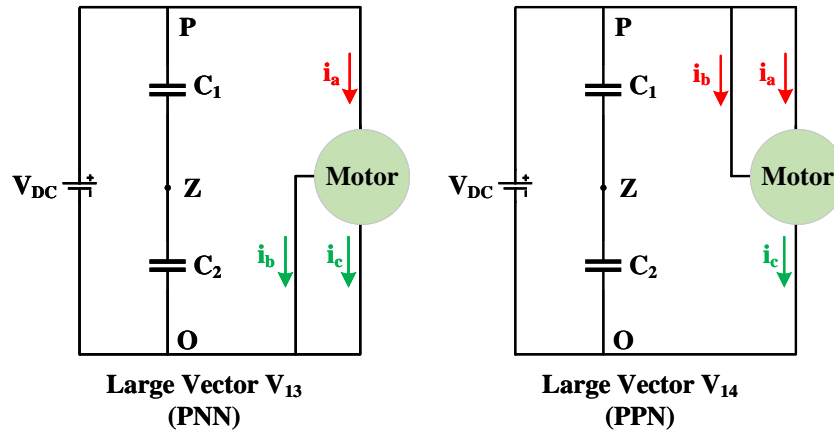


Figure 4.3: Equivalent circuits for switching states PNN and PPN.

When the modulation index is small, and small vector are utilized, the voltage unbalance issue causes voltage ripple. However, the large vector has a dominant effect on the voltage ripple, and the size of the capacitors shall be considered at the maximum modulation index.

The rms capacitor ripple current can be expressed as [95]:

$$I_{cap} = I_N \sqrt{\frac{M}{32\pi} [4\sqrt{3}(4\cos 2\phi + 6) - 9\pi M(\cos 2\phi + 1)]} \quad (4.2.4)$$

Where  $I_N$  is the output phase current amplitude,  $\phi$  is the power factor angle and

M is the modulation index. Capacitor ripple current is a function of power factor and modulation index, and Figure 4.4 illustrates this dependence.

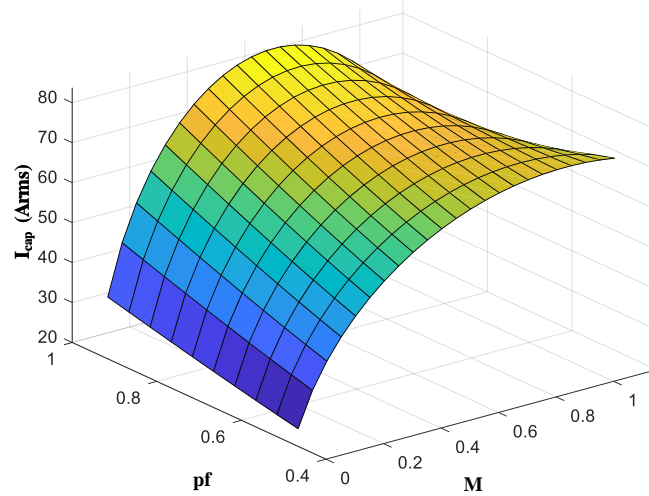


Figure 4.4: Capacitor rms current ripple is a function of modulation index M and load power factor  $\cos\phi$ .

Figure 4.4 is considered for DC-link voltage of 800V, and rms output phase current of 188A. The maximum rms capacitor ripple current is 83.77A, the corresponding modulation index is 0.65 and power factor is 0.95. The capacitor voltage ripple using SVPWM can be calculated using [96]:

$$V_{cap,ripple} = \frac{I_N M}{C_{total} f_{sw} 16} \left[ \left( 6 - \frac{96\sqrt{3}}{5\pi} M + \frac{108\pi - 81\sqrt{3}}{16\pi} M^2 \right) \cos^2\phi + \frac{8\sqrt{3}}{5\pi} M \right] \quad (4.2.5)$$

Where  $C_{total}$  is the total DC-link capacitor required to achieve the desired voltage ripple, and  $f_{sw}$  is the switching frequency. The voltage ripple increases with the decreasing of switching frequency, the worst case shall be considered at the minimum switching frequency. 10kHz switching frequency is considered as the worst case. The



rule of thumb DC-link capacitor voltage ripple tolerance is less than 5% [97], and for 800V DC-link voltage, the maximum voltage ripple shall be 40V.

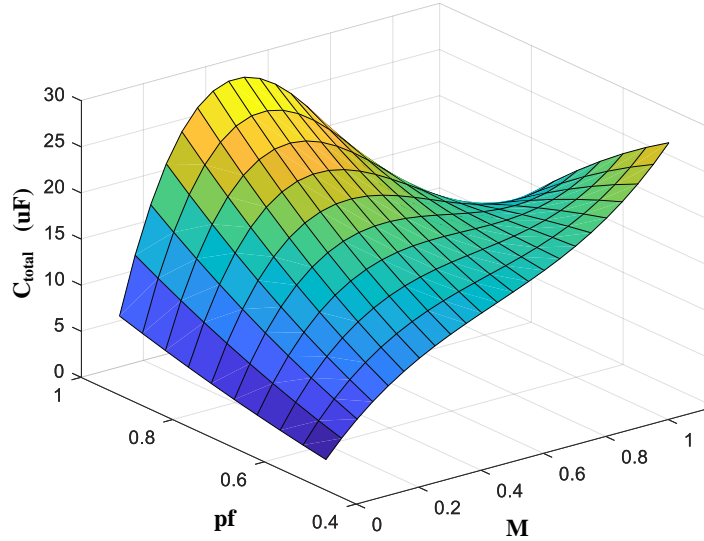


Figure 4.5: Minimum capacitance required for the desired voltage ripple is a function of modulation index  $M$  and load power factor  $\cos\phi$ .

The minimum capacitance required for the desired voltage ripple is a function of power factor and modulation index, and Figure 4.5 illustrates this dependence. Based on the design parameters mentioned above, the total capacitance shall be at least 29.6 $\mu$ F. And the upper ( $C_1$ ) and lower ( $C_2$ ) capacitance shall be at least 60 $\mu$ F. Considering even current distribution and decrease the current density at the capacitor leads, 9 of MKP1848580704K2 manufactured by VISHAY are connected in parallel for each upper and lower capacitor, and the total number is 18. Each one has a capacitance of 8 $\mu$ F, and the rated voltage and rms current are 700V and 8.5A respectively [98]. Compared with using a single capacitor, this arrangement decreases the total capacitor equivalent series resistance (ESR). The current are distributed

evenly across each capacitor leads, this decrease the maximum current density dramatically, and hot spot due to concentrated current density is avoided. The detailed arrangement and current density analysis is discussed in the next section.

#### 4.2.4 Sensor Selection

In order to implement voltage balancing on the DC-link capacitors, 2 voltage sensors are needed. Texas Instruments ISO224BDWV is chosen. The output bandwidth (BW) is upto 275KHz, which is large enough to capture the high frequency dynamics of the voltage ripple. Some other features include reinforced isolation, 0.3% linear error, single supply and a maximum working temperature of 125°.

### 4.3 ANPC Power PCB Design

The schematic of phase A leg is shown in Figure 4.6, and the layout design is duplicated for the other phase legs. The 18 capacitors are placed on the left side of the board. There are 3 capacitors on each row, and 2 rows in each inverter phase leg. The 36 MOSFETs are placed on the right side of the capacitors. Each row has 6 MOSFETs and 2 rows in each inverter leg.

The 3D view of the ANPC inverter power PCB design is shown in Figure 4.7. The MOSFETs pins are bent 90°, and the body of the MOSFETs are screwed onto the heatsink on the bottom of the housing. During assembly, the MOSFETs are first mounted onto the housing, and then the power PCB is mounted onto the housing on top of the MOSFETs. Once the MOSFETs and power PCB are both secured onto the housing, the MOSFETs are then soldered onto the PCB. MOSFETs mounting holes on

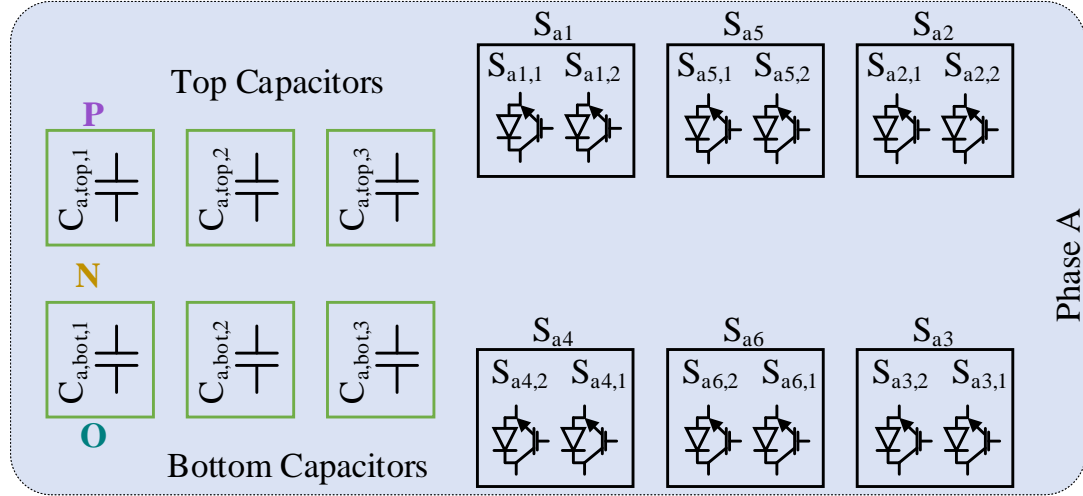


Figure 4.6: Schematic of ANPC power PCB phase A leg.

the power PCB are used to pass through the screw driver to unscrew the MOSFETs from the housing. The location of these holes on the PCB has very little current goes through, and they do not affect the current density on the PCB. However, the temperature rise is slightly affected due to the reduced copper area on the PCB. The detailed current density and temperature finite element analysis (FEA) is discussed in detail at later section.

The DC-input connectors are placed on the left side of the capacitors. The top and bottom connectors are connected to the positive and negative of the DC input power supply. The connector in the middle is connected to the neutral point of the inverter, its purpose is to utilize two DC-sources during the initial testing. For initial testing, two DC-sources will be used, one supplies DC voltage to the top leg, and the other one to the bottom leg of the inverter. By doing this, the balancing of the neutral voltage can be ignored. For normal operation, a single DC supply is connected to the top and bottom connectors, and the middle one is not used. The output AC

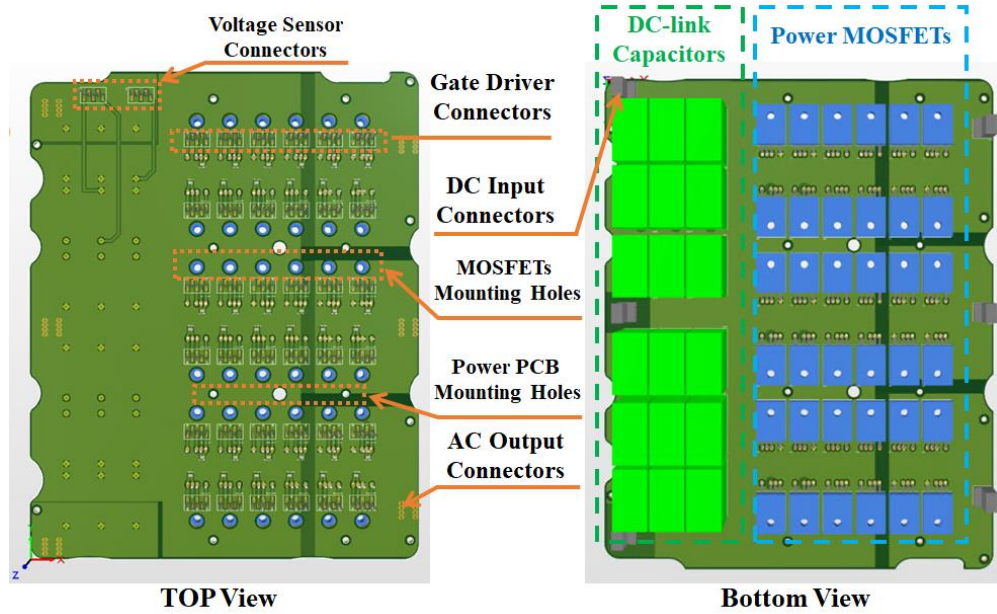


Figure 4.7: 3D view of ANPC power PCB.

connectors are placed on the right side of the board. The power PCB has multiple layers, thus through-hole connectors are selected to ensure the connection of multiple layers. REDCUBE 7461103 manufactured by Würth is chosen for the connectors. The current rating of the connector is  $160A_{rms}$ , and the temperature rating is up to  $150^{\circ}C$  [99]. The size of the PCB is 206mm by 267mm.

### 4.3.1 PCB Layer Stack

The power PCB has six layers in total, and the copper weight of each layer is 6OZ. Figure 4.8 shows the connections between capacitors and MOSFETs in the inverter phase A leg. The upper MOSFETs ( $S_{a1}$ ,  $S_{a2}$ ,  $S_{a5}$ ,) are placed in the same row, and lower MOSFETs ( $S_{a3}$ ,  $S_{a4}$ ,  $S_{a6}$ ,) are placed in the same row below the upper MOSFETs. The two parallel switches are placed next to each other, and as close as

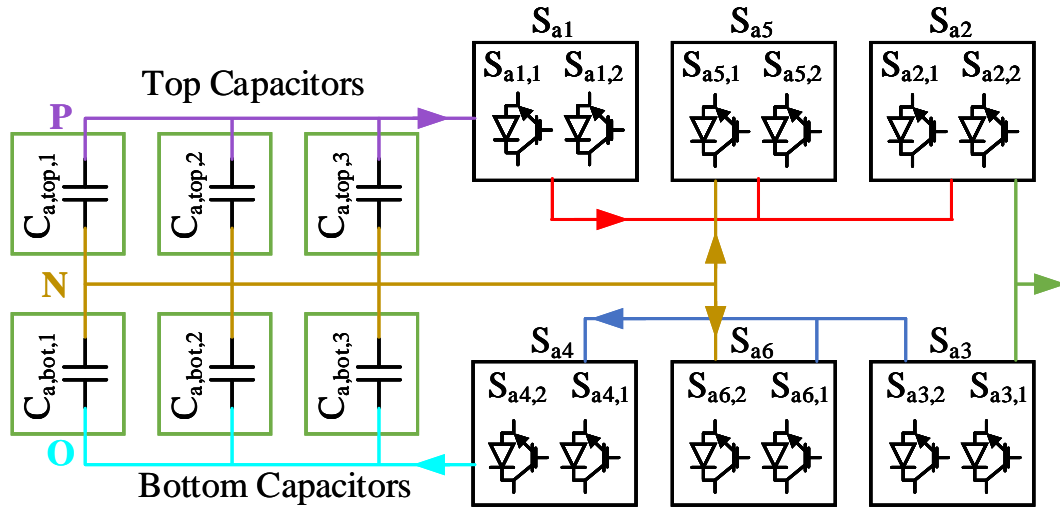


Figure 4.8: ANPC phase A MOSFET and capacitor connections.

possible to minimize the stray inductance in the gate path. The connection of each MOSFETs are shown as the coloured lines in Figure 4.8. Each line represents a layer on the PCB as shown in Figure 4.9, and the connection is done using polygon pours. The size of the polygon pours at each layer is maximized to achieve optimum thermal dissipation.

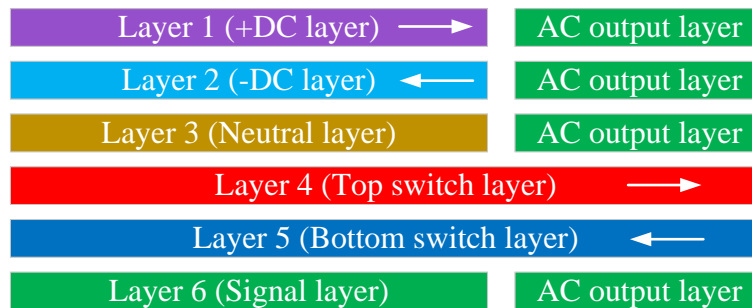


Figure 4.9: ANPC power PCB layer stack.

The purple line shows the connection from top capacitors to switch  $S_{a1}$ , and this

is on the first layer. The second layer is used for connecting the bottom capacitors to switch ( $S_{a,4}$ ) as shown in cyan line. The current direction in these two layers are opposite to each other, and placing them in adjacent layers increases the mutual inductance, thus the total stray inductance is reduced. The brown line indicates the connection of the neutral path, and it's placed on the third layer. The red line shows the connection between switch  $S_{a1}$  to  $S_{a2}$ , and the blue line shows the connection from switch  $S_{a3}$  to  $S_{a4}$ . Similarly, these two connections are placed on two adjacent layers (Layer 4 and Layer 5) to reduce the total stray inductance, since the current direction in these two layers are opposite. The AC output connection utilizes space on layer 1, 2, 3 and 6 as shown in green line. since the polygon pour on layer 4 and 5 extends all the way to the edge of the PCB, no AC output connections are made in these two layers.

The connection between the gate driver to the MOSFETs are placed in the last layer. The gate driver connectors are placed closely to the MOSFETs to reduce the stray inductance in the gate path. Since the current density in each layer is high around the MOSFET pins, surface mounted connectors are used. Using through hole connectors will increase the total stray inductance and cause worse thermal performance.

The polygon pours in all six layers are shown in Figure 4.10.

### 4.3.2 Simulation and Analysis of ANPC Power PCB

The PCB design procedure is shown in Figure 4.11.

First, the power switching devices and DC-link capacitor are chosen based on the inverter topology and power rating. The components selection has been explained

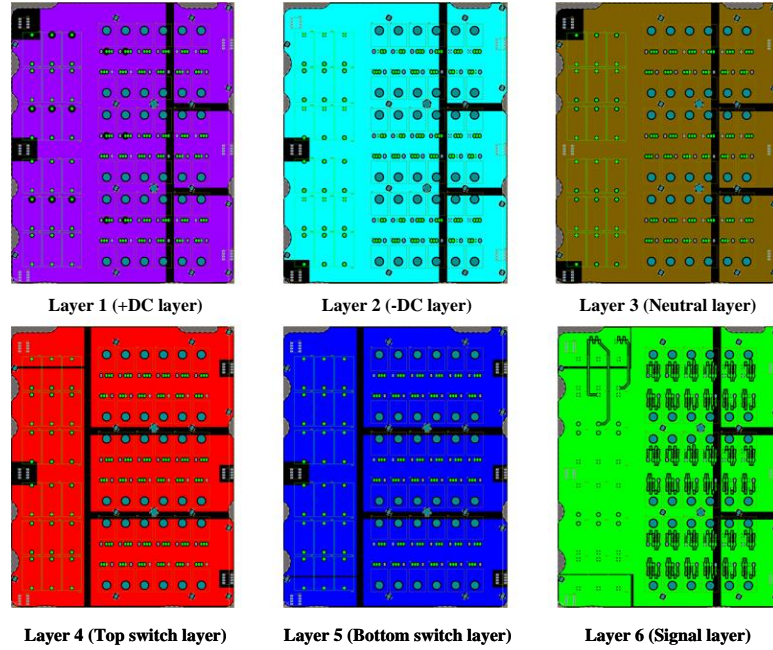


Figure 4.10: ANPC power PCB polygon pours in each layer.

in previous section. In the second step, the voltage overshoot analysis is conducted. The maximum allowed PCB polygon pour stray inductance is calculated analytically to ensure that the voltage spikes do not exceed the switch breakdown voltage. This value is then used as a guideline for the PCB layout design. In the next step, the stray inductance of the proposed design is calculated to ensure that it is less than the threshold value calculated in the previous step. After satisfying the overshoot conduction, the next two steps involve the busbar thermal aspects by estimating the maximum current density and the maximum temperature rise. This is accomplished by importing the 3D model into FEA models. ANSYS Maxwell is used for this purpose. Finally, the coating methods for the PCB are discussed, and the best method is selected to meet the clearance and creepage requirements.

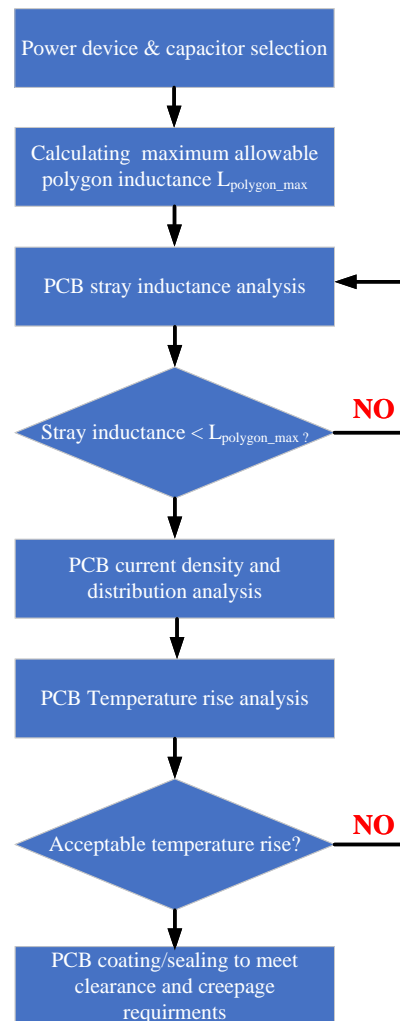


Figure 4.11: ANPC power PCB design procedures.

### Voltage Overshoot and the Maximum Allowable Stray Inductance Analysis

Stray inductance that is present in the power converter commutation loop causes voltage spike across the semiconductor devices during the switch turn-off transient [100]. The source of stray inductance comes from three parts: the DC-link capacitor equivalent series inductance, the PCB polygon pour, and the semiconductor device self inductance. The voltage spike increases if the total stray inductance gets higher,



and this can cause failure of the switching devices if the breakdown voltage of the device is exceeded.

Considering the 3-ANPC is operating in the Same-side modulation scheme, the gating signals for all 6 switches in phase leg A is shown in Figure 2.22b. During the negative half cycle,  $S_4$  &  $S_6$  are operating at the switching frequency, while  $S_1$  &  $S_2$  are kept at OFF, and  $S_3$  &  $S_5$  are kept at ON. The switching states are summarized in Table 4.4 [101]. During negative half cycle, the inverter is switching between state  $N$  and  $O^-$ . Two commutation loops can be found as shown in Figure 4.12.

Table 4.4: 3-level ANPC switching states for Same-side modulation scheme

Inverter State	$S_1$	$S_2$	$S_3$	$S_4$	$S_5$	$S_6$	Phase Voltage
P	1	1	1	0	0	1	$+0.5V_{DV}$
$O^+$	0	1	1	0	1	1	0
$O^-$	0	0	1	0	1	1	0
N	0	0	0	1	1	0	$-0.5V_{DV}$

The smaller commutation loop is marked as pink, and it goes through the lower capacitor,  $S_6$  and  $S_4$ . The bigger commutation loop is marked as green, and the current goes through the lower capacitor,  $S_5$ ,  $S_2$ ,  $S_3$  and  $S_4$ . When  $S_3$  and  $S_5$  are ON,  $S_2$  is in parallel with  $S_6$ . The drain to source voltage of  $S_2$  follows  $S_6$  even  $S_2$  is kept at OFF. The parasitic inductance resonates with the output capacitance of  $S_2$  [102]. The larger loop involves more components, and it contains more stray inductance than the smaller loop. Therefore, as long as the overshoot caused by the total stray inductance in the larger loop does not exceed the threshold value, the smaller loop will also be satisfied [103]. The stray inductance from each components in the larger is summarized in Table 4.5.

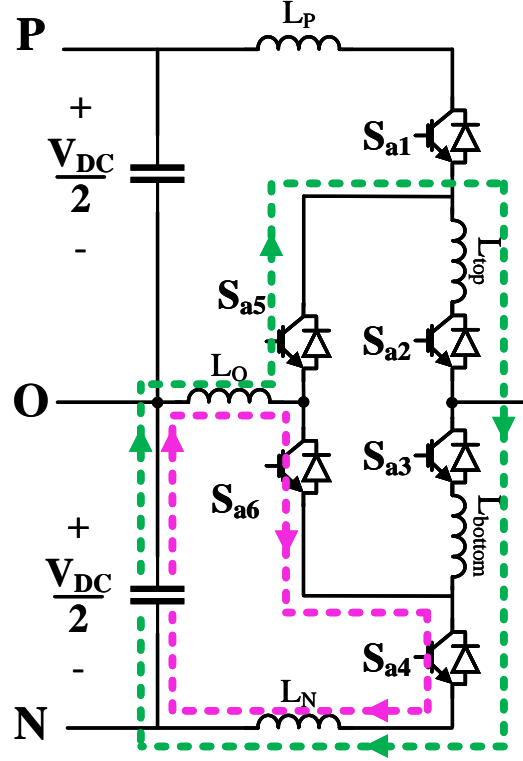


Figure 4.12: Equivalent circuit used in the overshoot analysis and calculation of PCB polygon pour stray inductance limit.

The total loop stray inductance can be calculated using equations:

$$\begin{aligned}
 L_{loop} &= L_{cap} + 4L_{sw} + L_{poly} \\
 L_{poly} &= L_N + L_O + L_{bottom} + L_{top} - 2L_{top-bottom} + 2L_{top-O} \\
 &\quad - 2L_{top-N} - 2L_{O-bottom} + 2L_{N-bottom} - 2L_{O-N}
 \end{aligned} \tag{4.3.1}$$

Where  $L_{poly}$  is the total stray inductance of the PCB polygon pour connection. The sign of the mutual inductances are determined by the direction of current flow through each polygon pours. When the direction of current flow is the same in two

Table 4.5: Larger commutation loop stray inductance components

Components	Stray inductance	Symbol
Lower Capacitor	Capacitor ESL	$L_{cap}$
MOSFETs	MOSFETs ESL	$L_{sw}$
PCB Polygon Pour Inductance	Top Switches Connection	$L_{top}$
	Bottom Switches Connection	$L_{bottom}$
	Neutral Switches Connection	$L_O$
	Negative Switches Connection	$L_N$
	Mutual between Top and Bottom	$L_{top-bottom}$
	Mutual between Top and Neutral	$L_{top-O}$
	Mutual between Top and Negative	$L_{top-N}$
	Mutual between Neutral and Bottom	$L_{O-bottom}$
	Mutual between Negative and Bottom	$L_{N-bottom}$
Mutual between Neutral and Negative	$L_{O-N}$	

polygons, the sign of the mutual inductance is positive; and if the current flow is in the opposite direction between them, then the sign of the mutual inductance is negative. The voltage drop across the switch  $V_{sw}$  during the turn off transient is calculated as:

$$V_{sw} = \frac{1}{2}V_{DC} + L_{loop}\left|\frac{di_a}{dt}\right| \quad (4.3.2)$$

Where  $\left|\frac{di_a}{dt}\right|$  is the current rate of change. During the transition between switching state N to O<sup>-</sup>, the current going through  $S_4$  reduces from the phase current  $i_a$  to 0 within the switch current fall time. The voltage across each active switch is  $\frac{1}{2}V_{DC}$ . The maximum allowable stray inductance to keep  $V_{sw}$  lower than the switch breakdown voltage can be calculated using Equation 4.3.2 and parameters from Table 4.6. And the calculated theoretical maximum PCB polygon pour stray inductance  $L_{poly,max}$  is 31nH. This number is then used as a guideline for the PCB layout design.

Table 4.6: Parameters for determining the maximum allowable PCB polygon stray inductance

Parameter	Symbol	Value
Capacitor ESL	$L_{cap}$	3nH
MOSFETs ESL	$L_{sw}$	5nH
DC link Voltage	$V_{DC}$	800V
MOSFETs Voltage Rating	$V_{sw,max}$	750V
MOSFETs Current Fall Time	$t_{fall}$	28ns
Overload peak phase current	$i_{a,overload,peak}$	188A

### Stray Inductance Simulation, Current Density and Current Distribution

After the proposed PCB design shown in Figure 4.7 is modelled, the stray inductance of the polygon pour is calculated using ANSYS Maxwell. The simulation results is shown in Table 4.7. And the total stray inductance of the PCB polygon pour connection  $L_{poly}$  is calculated as 11nH using Equation 4.3.1. This value is less than the 31nH maximum allowed value calculated in the previous section, and the amount of overshoot will not cause the breakdown of the switches.

Table 4.7: PCB polygon pour stray inductance

Components	Symbol	Value
Top Switches Connection	$L_{top}$	7.9nH
Bottom Switches Connection	$L_{bottom}$	26.7nH
Neutral Switches Connection	$L_O$	37.1nH
Negative Switches Connection	$L_N$	19.3nH
Mutual between Top and Bottom	$L_{top-bottom}$	8.9nH
Mutual between Top and Neutral	$L_{top-O}$	4.8nH
Mutual between Top and Negative	$L_{top-N}$	2.2nH
Mutual between Neutral and Bottom	$L_{O-bottom}$	21.1nH
Mutual between Negative and Bottom	$L_{N-bottom}$	7.7nH
Mutual between Neutral and Negative	$L_{O-N}$	20.3nH

The proposed PCB design shown in Figure 4.7 conducts both DC and AC currents. The polygon that connects the DC input to the capacitors conducts DC currents, and

the polygon that connects the capacitors and MOSFETs conducts AC current. Hence, both DC and AC current densities are analysed using 3D FEA models.

For the DC analysis, the current distribution between the DC input connectors and the capacitors are investigated [104]. For this analysis, the PCB is shorted at the capacitor terminals, and the DC connectors are injected with DC current. The amount of current injected is the root mean square (rms) value of the inverter input current,  $I_{in,rms}$ . The injected current is calculated in Equation 4.3.3 assuming that the inverter is controlled with SVPWM. The injected current is a function of the inverter output phase rms current  $I_{a,rms}$ , modulation index  $m_a$ , and power factor  $\cos\theta$  [95].

$$I_{in,rms} = I_{a,rms} \sqrt{\frac{2\sqrt{3}}{\pi} m_a (0.25 + \cos^2\theta)} \quad (4.3.3)$$

The DC current density simulation result is shown in Figure 4.13. The maximum current density is 1.14A/mm<sup>2</sup>, which is much lower than the rule of thumb 5A/mm<sup>2</sup> [105]. Since the top row of capacitors are closer to the DC connectors on the top left corner, so the current is more concentrated on the top left corner of the PCB. However, since the maximum current is small, this distribution is acceptable, and the thickness of the PCB is able to dissipate the heat generated by this contraction of current.

For the AC analysis, the current distribution between the capacitors and the MOSFETs is investigated. The PCB is shorted at the AC terminals, and the amount of current injected is equal to the capacitor rms current. The injected current is calculated in Equation 4.3.4 assuming that the inverter is controlled with SVPWM. The injected current is a function of the inverter output phase rms current  $I_{a,rms}$ ,

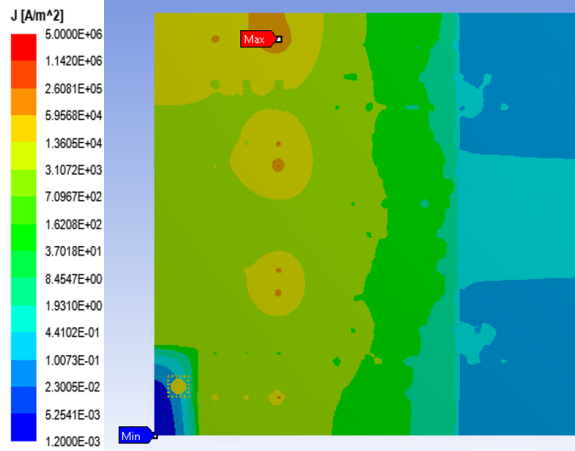


Figure 4.13: DC current density analysis.

modulation index  $m_a$ , and power factor  $\cos\theta$  [87].

$$I_{cap,rms} = I_{a,rms} \sqrt{\frac{m_a}{32\pi} [4\sqrt{3}(4\cos^2\theta + 6) - 9\pi m_a(\cos 2\theta + 1)]} \quad (4.3.4)$$

The AC current density simulation result is shown in Figure 4.14. The maximum current density is  $0.89\text{A}/\text{mm}^2$ . For each leg of the inverter, the current travels mostly in the area between the two row of MOSFETs. Therefore, all the mounting hoses as shown in Figure 4.7 are located outside of this area. The current is contracted around the MOSFETs pins, this is normal for through hole components. The type of polygon connection type is a key factor for determining the maximum current density around the MOSFETs pins.

Figure 4.15 shows the two common types of polygon pour connection. For the relief connection shown on the left, the polygon and the soldering pad have an air gap in between. And for the direct connection shown on the right, the polygon extends all the way to the solder pad. The relief connection offers better current density, and the heat caused by the current density contraction around the pad can be dissipated by

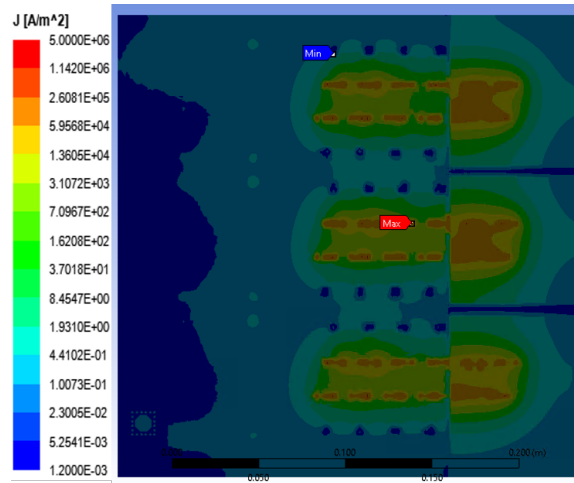


Figure 4.14: AC current density analysis.

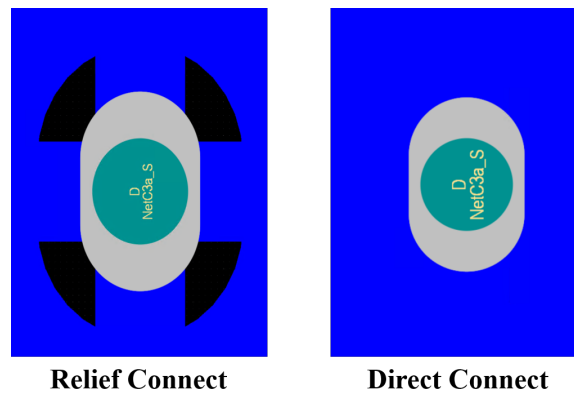


Figure 4.15: Polygon pour connection type.

the polygon more efficiently. However, the copper thickness for this PCB is 6OZ, and using direct connection will make the soldering of the MOSFETs extremely difficult. The heat applied by the soldering iron will be absorbed by the surrounding polygon quickly, and the pad will not be heat up enough to melt the solder. For this reason, the relief connection is used, and the maximum current density is slightly increased, but still way less than  $5\text{A}/\text{mm}^2$ .

## PCB Thermal Analysis

The PCB temperature rise is simulated in ANSYS CFD at two conditions. The PCB thermal performance at the 70kW continuous power rating is analysed using steady-state thermal analysis, and the 120kW (10s) overload power condition is analysed using transient thermal analysis as shown in Figure 4.16.

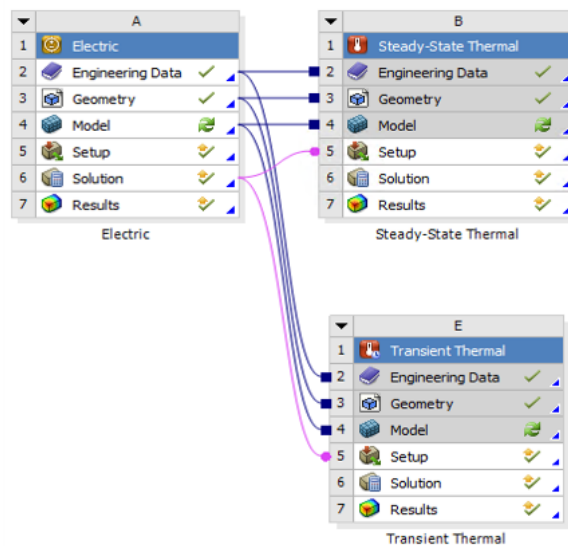


Figure 4.16: ANSYS CFD solver set-up for steady-state and transient thermal simulation.

For both analysis, the ambient temperature is set to  $85^{\circ}\text{C}$ , and the film coefficient of free air is set to  $1\text{W}/\text{m}^2\text{C}$  to simulate the worst case scenario. The result of the steady-state thermal analysis is shown in Figure 4.17.

For the 70kW continuous power rating, the maximum temperature of the PCB at steady-state is  $122^{\circ}\text{C}$ . And for the 10s transient thermal analysis of 120kW overload condition, the maximum temperature increases to  $132^{\circ}\text{C}$ . FR4 is commonly used as PCB insulation layer. Normal FR4-TG150 has a glass transition temperature of  $150^{\circ}\text{C}$ , this is the temperature for which the FR4 starts to deform, and this is considered as



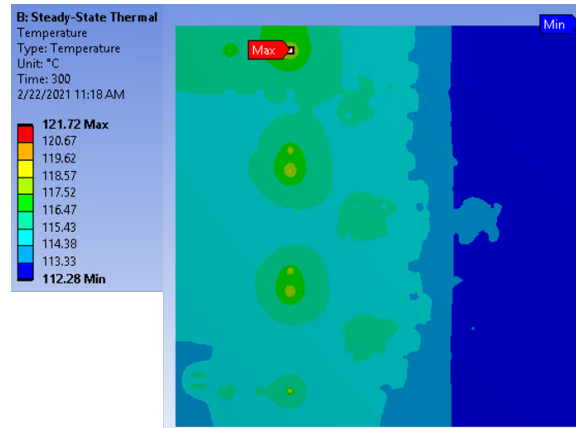


Figure 4.17: Polygon pour connection type.

the absolute maximum working temperature. For this PCB design, FR4-TG170 is used as the insulation layer. It has a increased glass transient temperature of  $170^{\circ}\text{C}$  [106]. For the maximum PCB temperature of  $132^{\circ}\text{C}$  at the worst case scenario, using FR4-TG170 allows a room of  $38^{\circ}\text{C}$ , this ensures the proper functioning of the PCB even without active cooling applied.

### Clearance, Creepage Distance and Insulation of the PCB

Clearance and creepage distance are the minimum distances to prevent a short circuit between two live conductors. As shown in Figure 4.18, the creepage distance is the shortest path between two conductive materials measured along the surface of an isolator. Clearance distance is the shortest distance between two conductive materials measured through the air. Clearance and creepage distance depend on the operating voltage, pollution degree, and insulation material. Pollution degree classifies the amount of dust and moisture present in the equipment operating environment [107]. Pollution degree affects the clearance and creepage distance significantly. If the PCB operates in a moisture and debrided environment, the current can track along the

PCB surface and create a short-circuit. Pollution degree ratings are defined by safety standards developed by organizations such as Underwriters Laboratories (UL) and International Electrotechnical Commission (IEC). Traction inverters generally fall under pollution degree 2. To protect the electronic device from corrosive chemical species, an ALD protective coating can be applied to the PCB.

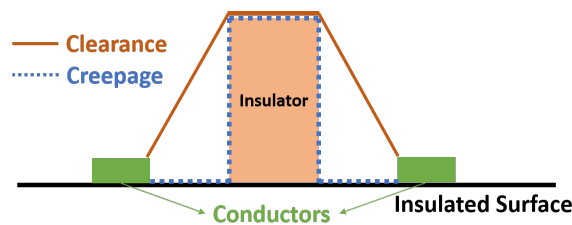


Figure 4.18: Clearance and creepage distance.

## 4.4 Summary

A comprehensive ANPC power PCB design procedure is presented in this Chapter. A detailed components selection based on the inverter specifications is discussed first, then the detailed analysis of the voltage overshoot, current density and distribution, and temperature rise are discussed.

# Chapter 5

## Experimental Implementation and Validation of a 3-Level ANPC Prototype

### 5.1 Introduction

Due to the global pandemic, the lab access and equipments are limited, and the experimental test setup is not constructed for high power testing. The ANPC power PCB, gate driver PCB, PCB components, and the inverter housing are sourced from many different manufactures, and the shipping for varies parts are delayed. The low power test setup was constructed for maximum 30V DC-link voltage and three 10ohms 500W resistors are used as the resistive load. The test setup utilizes a Texas Instruments TMS320F28377D dual-core microcontroller which is attached to a custom-built control board. This control board handles all signal conditioning between the DSP and the mechanical components so that the suitable signals at the correct voltages are

input and output for the DSP.

## 5.2 Inverter Assembly

The first step for the inverter assembly process is to assemble the gate driver PCB.

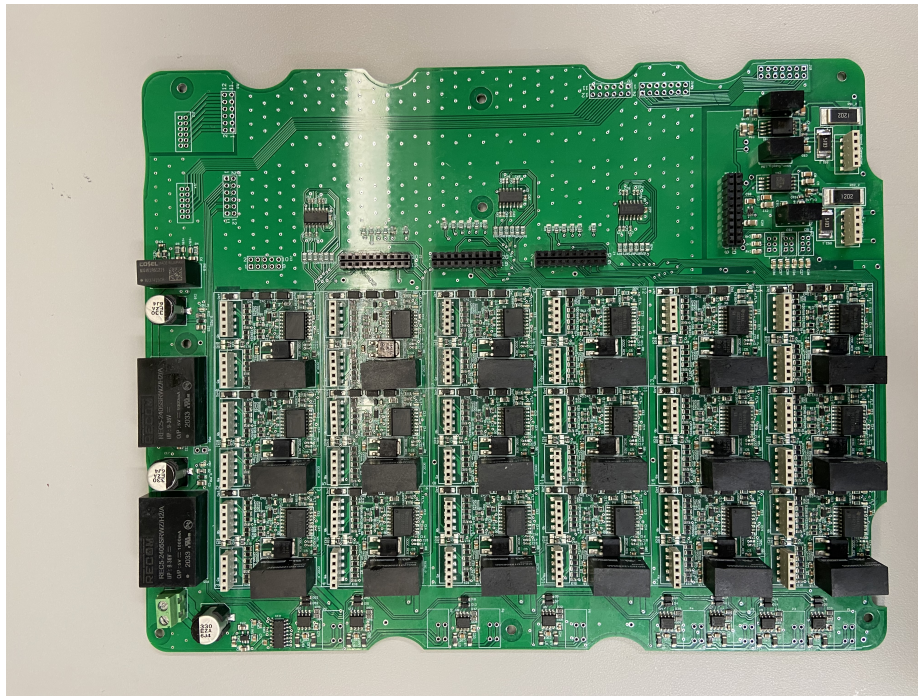


Figure 5.1: Gate driver PCB.

A stencil is used for applying the solder paste onto the soldering pads. The solder paste used is SMD291AX10T5 manufactured by CHIPQUIK [108], this no clean solder paste has a melting point of  $183^{\circ}$ . This allows a low reflow temperature to protect the components during the soldering process, and it is also high enough so that the solder joint does not liquefy during normal operation. The recommended reflow profile is shown in Figure 5.2, and this temperature curve is programmed into the reflow oven for the soldering process. The finished PCB is shown in Figure 5.1.

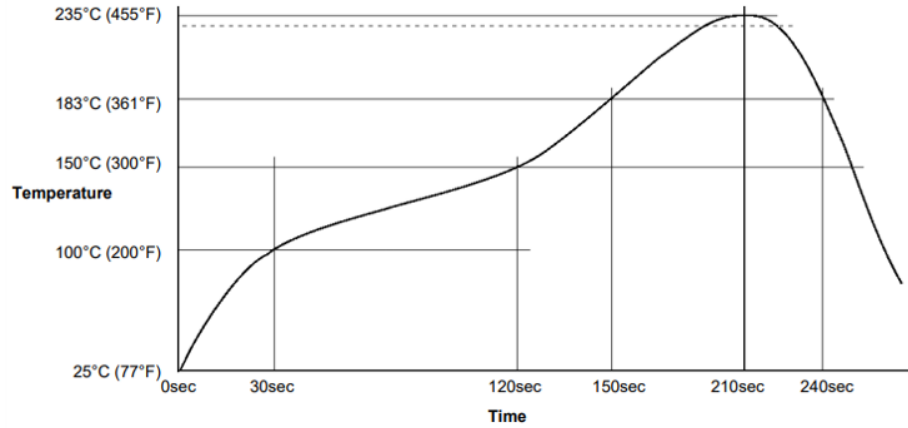


Figure 5.2: SMD291AX10T5 recommended reflow temperature profile.

The next step is to screw the MOSFETs onto the cooling block that is located at the bottom of the inverter housing as shown in Figure 5.3. For the low power testing, only one of the two parallel MOSFETs are used to avoid any issues associated with the current sharing of the two parallel MOSFETs. Special calibration in the gate driver and gating signal connection is needed later to synchronize the two MOSFETs. If the two MOSFETs are not turned ON or turned OFF at the same time, the entire phase current could go through a single MOSFETs and damage it [109]. After the MOSFETs are soldered

After the MOSFETs are mounted onto the housing, the leads are bent 90°, then the power PCB is placed on top of the MOSFETs as shown in Figure 5.4. The final step is to placed the gate driver PCB on top of the power PCB, and the gate driver PCB is mounted onto the standoffs on the inverter housing.

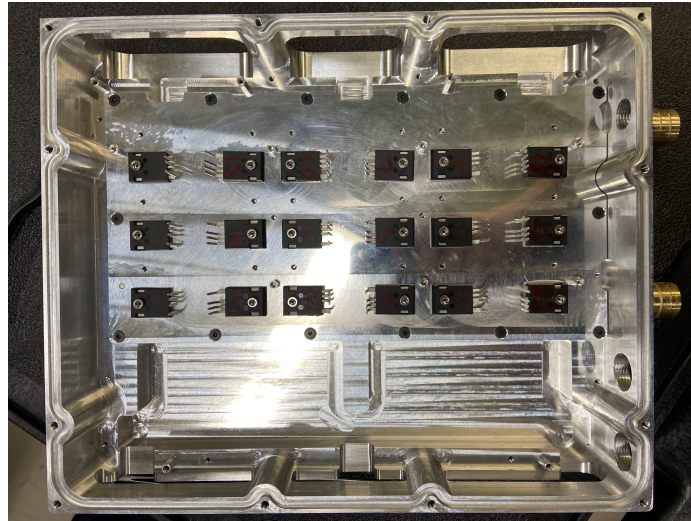


Figure 5.3: Mounting the MOSFETs onto the inverter housing.

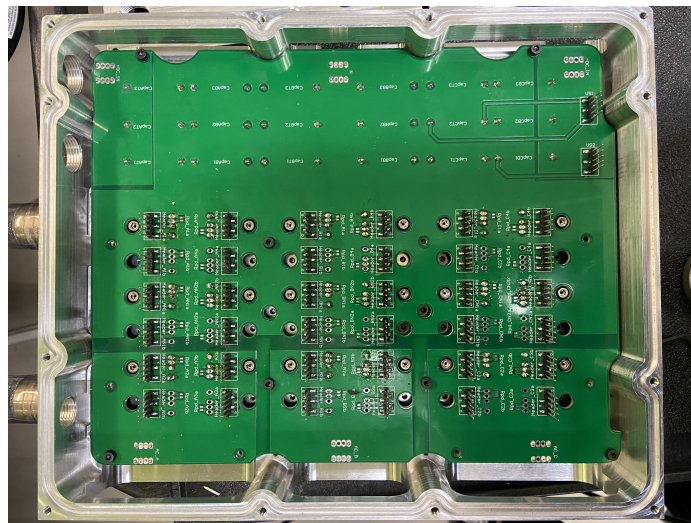


Figure 5.4: Mounting the power PCB onto the inverter housing.

### 5.3 Low Power Resistive Preliminary Testing

The preliminary low power testing setup is shown in Figure 5.5. The gating signals are connected to the gate driver using jumper wires as a temporary solution, since the shipping of the custom designed controller board is delayed. The gating signals



and the fault detection connection is connected to an available controller board that is based on the same DSP IC as shown in Figure 5.6.

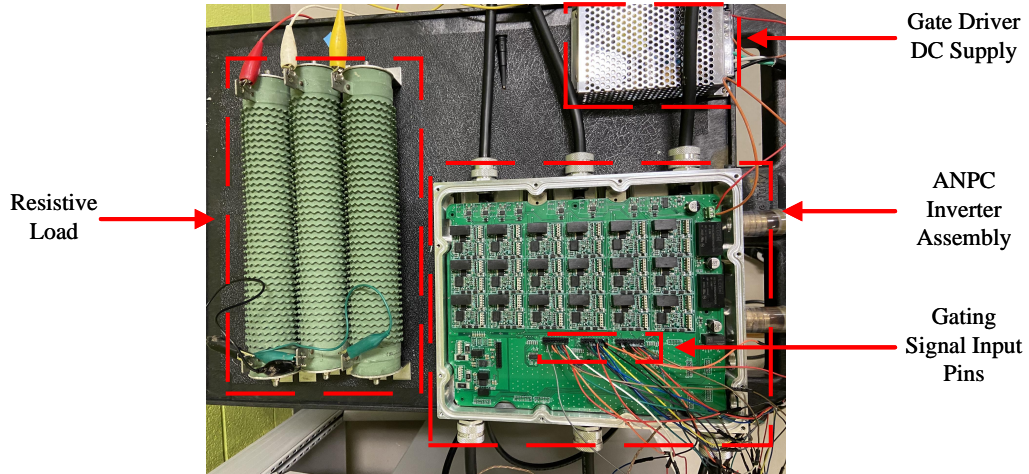


Figure 5.5: Preliminary low power testing setup.

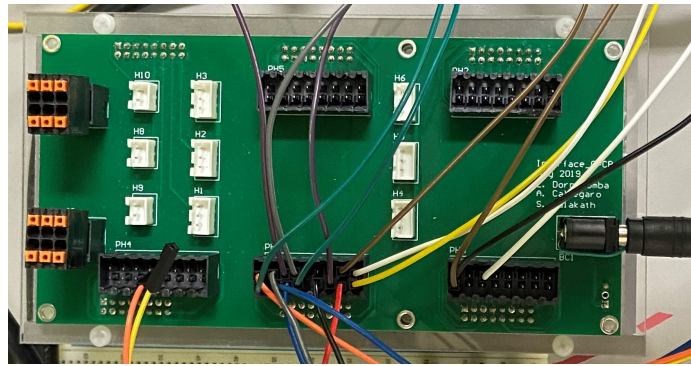


Figure 5.6: Controller used in the preliminary low power testing setup.

### 5.3.1 Fault Detection

The DESAT protection pin of each gate driver is triggered from 1 to 0 when a over current is detected. On the gate driver, the FAULT pin of all the gate drivers in the same phase leg is ANDed with an AND gate. If a fault is detected on any gate

driver in a phase leg, the AND gate for that phase is triggered from 1 to 0. There are three AND gates in total, and each one is used as an external interrupt to trigger a shut down in the control software. The shut down will turn off all of the MOSFETs once the interrupt is triggered. There are two methods for the control software to implement this shut down. The first method is to change the CMPA registers of all EPWM gating signals to 0, this configures the duty cycles of all EPWM signals to 0% as shown in Figure 5.7. The signals are captured by setting a fall edge trigger on the Fault signal on the oscilloscope. The red signal is the Fault pin measured from the gate driver, and the blue curve is the inverter line to line voltage  $V_{AB}$ . The time between a fault is detected and the MOSFETs being shut down for this method is 1.072us. The problem with this method is that the duty cycle of the EPWM signals are set at the next switching period, and as the switching frequency decreases, this shut down delay increases.

The other method is to use the Trip-Zone Submodule (TZ) on the TMS320F28377D DSP controller [110]. TZ provides a software forced tripping, it support for one-shot trip (OSHT) for major short circuits or over-current conditions. Upon a fault condition, EPWM signals can be forced to LOW right away. The time between a fault is detected and the MOSFETs being shut down for this method is 0.559us as shown in Figure 5.8. This method results in a faster reaction time when a over current is detected. Once the Fault is cleared, the TZ resister can be configured to allow the EPWM signals to bypass the trip zone, and this allows the signals to get back to normal operation without recompiling or re-upload the code to the DPS controller.



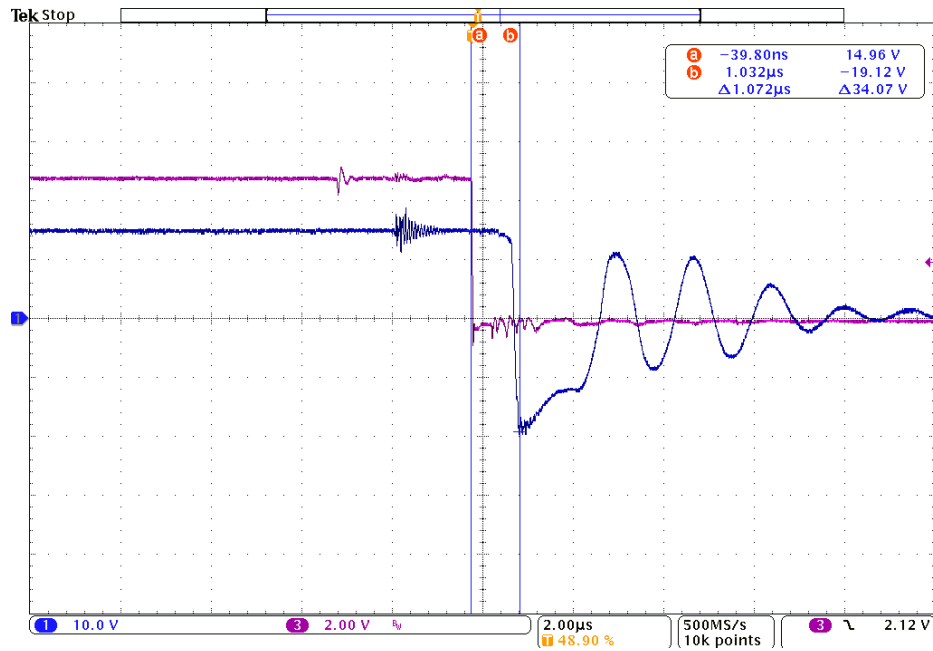


Figure 5.7: Shut down by changing the duty cycles of all EPWM gating signals to 0%.

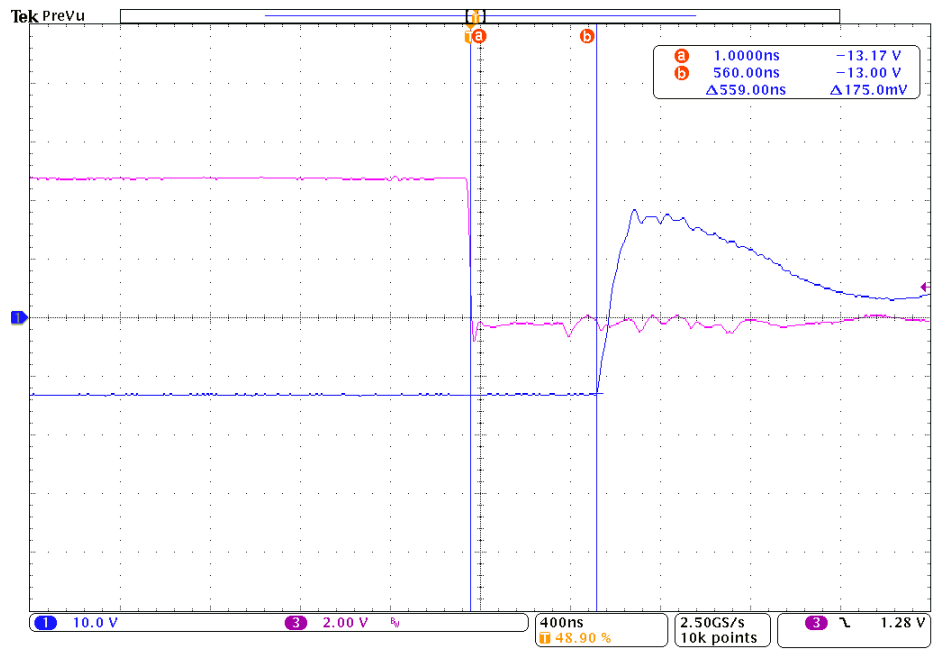


Figure 5.8: Shut down using the Trip-Zone Submodule.

Table 5.1: Low power testing parameters

DC-Link Voltage	30V
Resistive Load	10ohms
Switching frequency	10kHz
Modulation Technique	Full-path clamping IPD SPWM
Controller	TI TMS320F28377D

### 5.3.2 Low Power Output Voltage and THD

The low power experimental testing parameters are shown in Table 5.1. The DC-link voltage is 30V, and the load are three 10ohms, 500W rated resistive load. Full-path clamping IPD SPWM modulation is implemented using the TMS320F28377D DSP controller. The three phase line voltages ( $V_{AB}$ ,  $V_{BC}$  and  $V_{CA}$ ) at modulation index of 0.9 is shown in Figure 5.9.

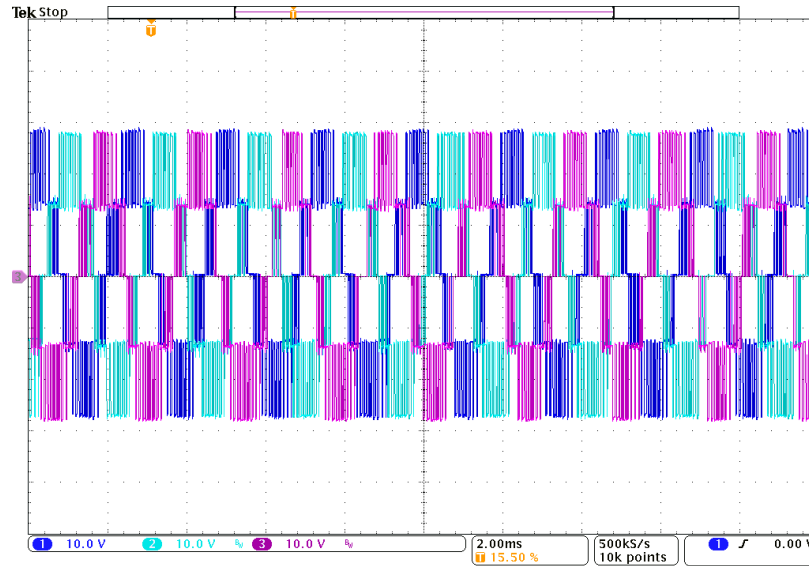


Figure 5.9: Inverter output line voltages ( $V_{AB}$ ,  $V_{BC}$  and  $V_{CA}$ ) at modulation index of 0.9.

The transition of the phase voltage ( $V_{AO}$ ) from modulation index ( $m_a$ ) of 0.1 to 0.9 is shown in Figure 5.10, and the transition of the line voltage ( $V_{AB}$ ) from modulation

index ( $m_a$ ) of 0.1 to 0.9 is shown in Figure 5.11.

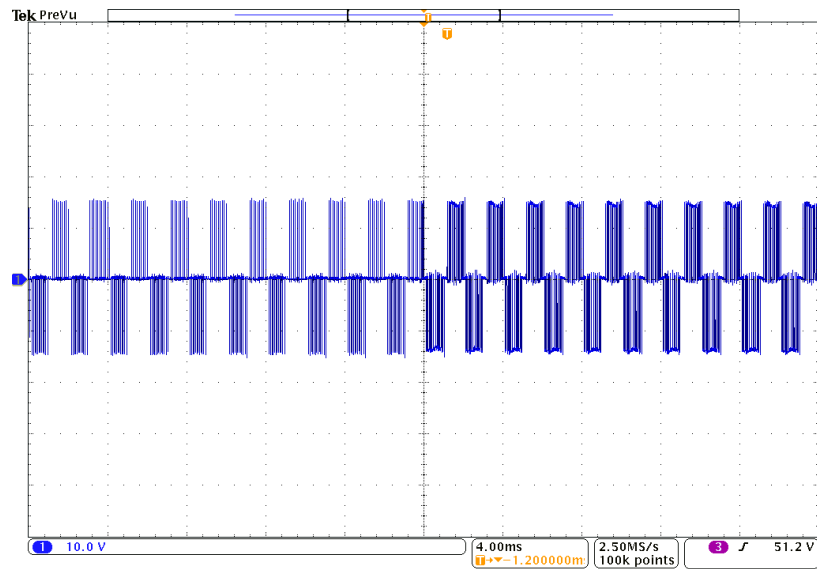


Figure 5.10: Transition of phase voltage  $V_{AO}$  from modulation index of 0.1 to 0.9.

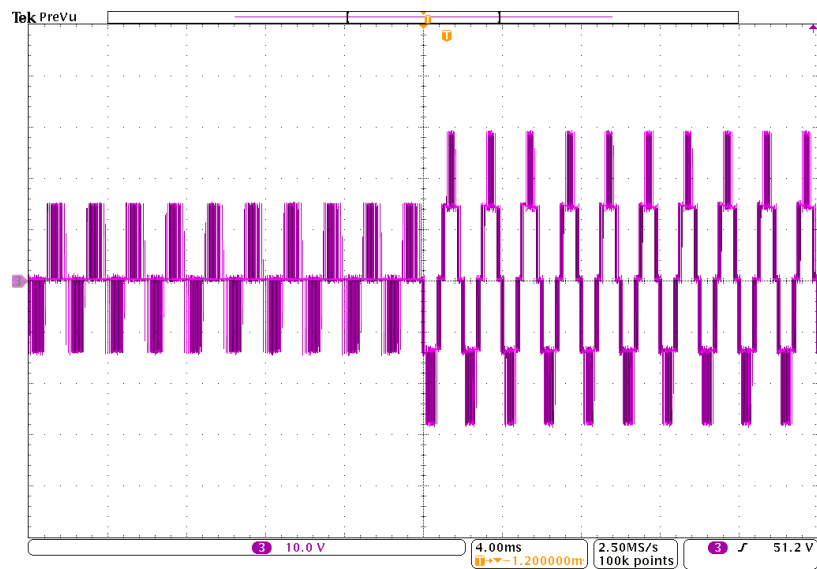


Figure 5.11: Transition of line voltage  $V_{AB}$  from modulation index of 0.1 to 0.9.

The waveforms are recorded using Tektronix MDO3000 oscilloscope. The sampling frequency of the oscilloscope is 2.5MS/s, and 100K data points are sampled. The

sampled data is imported into Matlab for calculating the THD, and 50 fundamental cycles are used as the window for calculating the THD. The fundamental frequency is 500Hz, which is equivalent to 6000RPM for a motor with 5 pole pairs, and the switching frequency is 10kHz. The phase-A phase voltage  $V_{AO}$  and its harmonic spectrum at modulation index of 0.9 is shown in Figure 5.12, and the THD is 68.06%. The phase voltage contains 3 voltage levels as shown in the waveform.

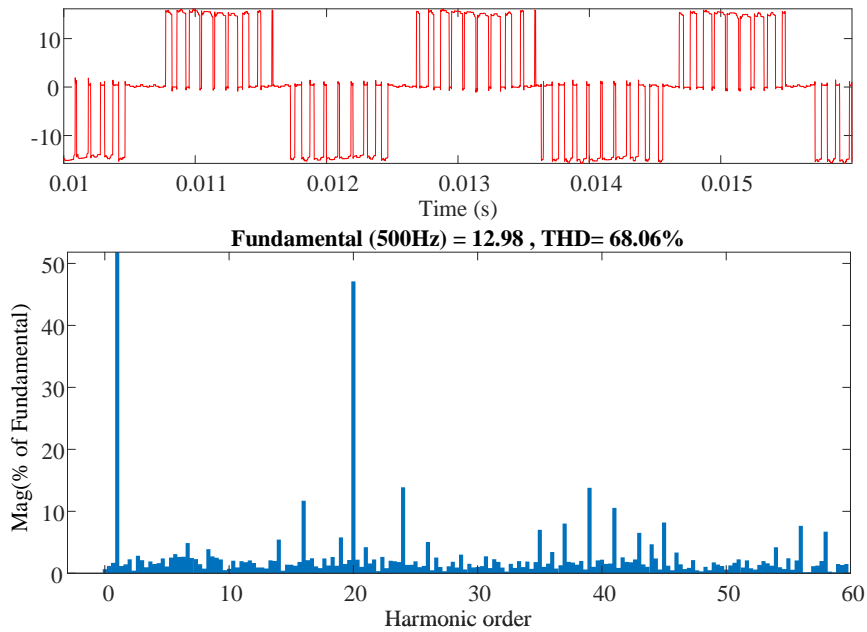
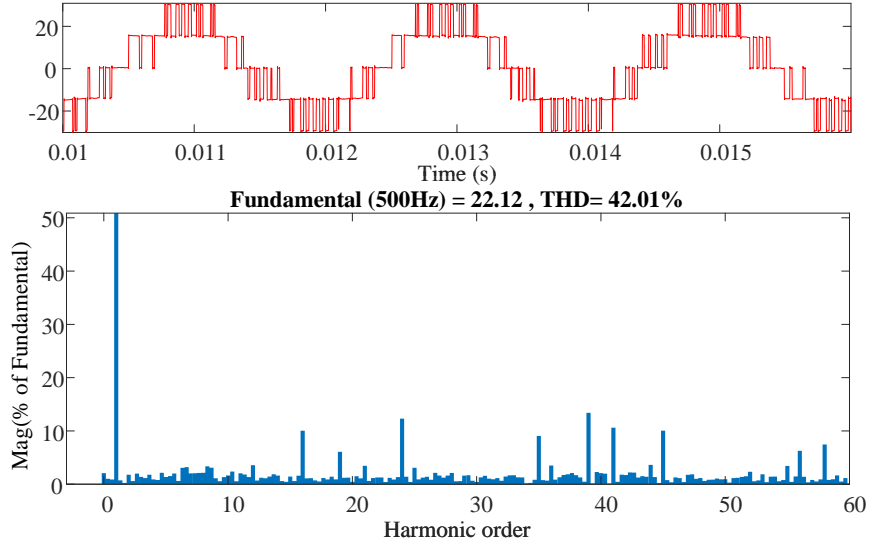


Figure 5.12: Harmonic spectrum phase voltage of  $V_{AO}$ .

The line voltage  $V_{AB}$  and its harmonic spectrum at modulation index of 0.9 is shown in Figure 5.13. The THD is 42.01%, and it is smaller compared to the phase voltage. The Line voltage has 5 voltage levels as shown in the waveform.

The frequency modulation index  $m_f$  can be calculated as 20. The significant harmonic order and its magnitude for the phase and line voltage are listed in Table 5.2 and 5.3 respectively.

Figure 5.13: Harmonic spectrum phase voltage of  $V_{AB}$ .Table 5.2: Harmonic order and magnitude for phase voltage at  $m_a = 0.9$ .

Harmonic Order	$V_{AO}THD$
$m_f - 4$	16 <sup>th</sup> 10.4%
$m_f - 1$	19 <sup>th</sup> 5.2%
$m_f$	20 <sup>th</sup> 47.8%
$m_f + 1$	21 <sup>th</sup> 4.4%
$m_f + 4$	24 <sup>th</sup> 12.25%

It can be observed that the line and phase voltage have both even and odd harmonic orders around  $m_f$  and  $2m_f$ , but line voltage has no harmonic contents at those two exact frequencies. The largest harmonic in the phase voltage is the 20<sup>th</sup> ( $m_f$ ), and the largest harmonic in the line voltage is 39<sup>th</sup> ( $2m_f - 1$ ).

In order to investigate the effect of switching frequency on voltage THD, the same experiment is conducted at 20kHz switching frequency. The resulting phase and line voltage THD are 69.4% and 40%. The phase voltage THD is increased slightly while the line voltage THD is decreased compared to 10kHz switching frequency. The

Table 5.3: Harmonic order and magnitude for line voltage at  $m_a = 0.9$ .

Harmonic Order	$V_{AB}THD$
$m_f - 4$	16 <sup>th</sup> 9.1%
$m_f - 1$	19 <sup>th</sup> 5.6%
$m_f + 1$	21 <sup>th</sup> 4.3%
$m_f + 4$	24 <sup>th</sup> 10.95%
$2m_f - 5$	35 <sup>th</sup> 9.8%
$2m_f - 1$	39 <sup>th</sup> 13.6%
$2m_f + 1$	41 <sup>th</sup> 10.4%
$2m_f + 5$	45 <sup>th</sup> 10.2%

effect of switching frequency will be more significant to the output current THD when driving a motor load, as it shown in the simulations in Chapter 3. The high power set up with motor load is in construction, and the current THD will be investigated when the setup is ready.

In order to investigate the effect of fundamental frequency on voltage THD, the same experiment is conducted at various fundamental frequencies. The range of fundamental frequencies is from 83.3Hz to 833.3Hz, which corresponds to a mechanical speed from 1000RPM to 10000RPM for a motor with 5 pole pairs. The modulation index is kept at 0.9 constant, and the switching frequency is 20kHz. The results of the measured and simulated voltage THD is shown in 5.14.

Both the line and phase voltage THD improves with the increase of fundamental frequency, but the change is not significant. The measured THD is close to the simulation results.

In order to investigate the effect of modulation index on voltage THD, the same experiment is conducted at various modulation index. For this experiment, the fundamental frequency is 500Hz, and the switching frequency is 20kHz. The measured and simulated THD results are shown in Figure 5.15.

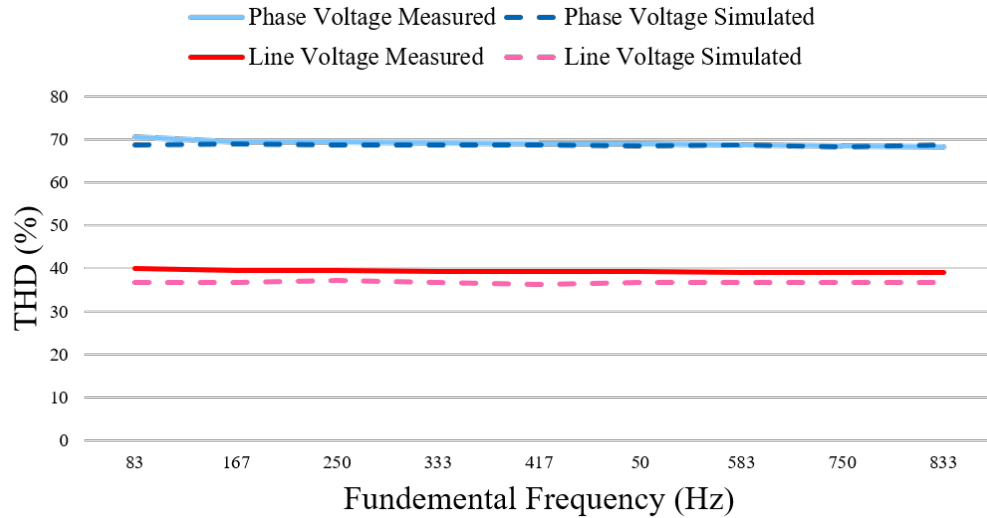


Figure 5.14: Measured and simulated voltage THD at various fundamental frequencies.

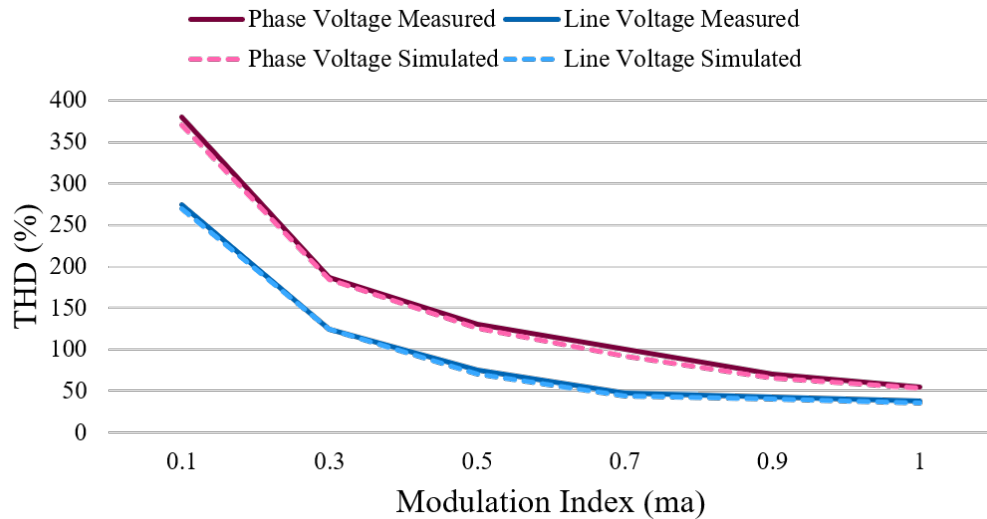


Figure 5.15: Measured and simulated voltage THD at various modulation index ma.

The modulation index has a significant effect on both the line and phase voltage THD. The quality of the output voltage increases drastically with the increase of the modulation index. The rate of change for the THD is large when the modulation

index is small, and it becomes smaller and smaller as the modulation index gets larger. The measured THD is close to the THD results from simulation.

## 5.4 Summary

The inverter assembly process and preliminary testing results is presented in this chapter. Due to the global pandemic, the lab access and equipments are very limited. The preliminary testing is only performed with 30V maximum DC-link voltage and resistive load. The high power testing with motor load will be performed once the equipments are available. The preliminary testing is able to verify the proper working of the gate driver PCB, power PCB and control algorithm.



# Chapter 6

## Conclusions and Future Work

This thesis focus on the design and performance of a 70kW 3-level ANPC traction inverter. An overview of the existing traction inverter topologies and various modulation techniques are presented to give an overview of the operation principle of traction inverters. A comprehensive analysis and comparison of 2-level VSI, 3-level NPC and ANPC in traction application is presented. The simulation results shows that the 3-level ANPC provides better efficiency even when the motor is running at low speed and low torque, and the output THD is improved drastically. The voltage stress of the switching device is reduced in an ANPC, and the reliability of the inverter is improved. Furthermore, the drive cycle simulation shows that the 3-level ANPC can save upto 20% battery energy compare with the 2-level VSI.

A detailed design procedure for a 70kW 3-level ANPC is proposed in this thesis. The component section highlights some key considerations for selecting the switch, gate driver, capacitor and various sensors. The DC-link capacitor usually takes the largest volume within a inverter, and to increase the power density of the inverter, an analytical calculation for determining the capacitance value and its current stress

is provided in this thesis. The switch is selected carefully based on the drain to source resistance, current and voltage ratings, the rise and fall time and the maximum operating temperatures. The device selected for building the prototype is not the optimum solution, but it is well stocked on distributors like Digikey, unlike many products that are in shortage due to the global pandemic. The gate driver selected has the strength to drive two parallel MOSFETs, and it also has the protection features.

The 3-level ANPC power PCB design focus on reducing the stray inductance in the commutation loop. An analytical method for determining the voltage overshoot is presented in this thesis, and the stray inductance is simulated using ANSYS MAXWELL. The components layout plays a key role in the stray inductance, and the design of the polygon pour ensures a balanced current distribution across each DC-link capacitors. The current density of the PCB and its effect on the PCB thermal performance is simulated in ANSYS Workbench. Both steady-state thermal and transient thermal analysis are conducted to ensure a safe operating temperature at both continuous and overload condition. Finally, the inverter assembly process and the preliminary low power testing results are presented.

## 6.1 Future Work

An immediate next step in this research includes the design and construction of a high-power experimental testing setup to allow back-to-back motor testing. The simulation results for the output THD and efficiency analysis discussed in Chapter 3 can be tested and verified. The setup will allow us to derive the combined motor inverter efficiency in the full load range at different frequencies. Various algorithms

will be tested for the neutral point voltage balancing and loss distribution balancing among semiconductor devices.

Next step also includes operating the ANPC when a fault occurs to test the fault tolerant of the ANPC. The fault tolerant capability of the ANPC is very important considering system availability, safety and reliability. Control algorithms will be tested to keep the neutral point voltage balanced and stable during both open circuit and short circuit fault.

Lastly, the future work also includes implementing other multi-level inverter topologies that are mentioned in Chapter 2, and compare their performance with the 3-level ANPC. The results will produce a guideline for selecting the optimum multi-level inverters for the EV powertrain.

# References

- [1] Z. Shu, J. Tang, Y. Guo, and J. Lian, “An efficient svpwm algorithm with low computational overhead for three-phase inverters,” *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 1797–1805, 2007.
- [2] M. A. Jabbar, A. M. Khambadkone, and Zhang Yanfeng, “Space-vector modulation in a two-phase induction motor drive for constant-power operation,” *IEEE Transactions on Industrial Electronics*, vol. 51, no. 5, pp. 1081–1088, 2004.
- [3] R. Teichmann and S. Bernet, “A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications,” *IEEE Transactions on Industry Applications*, vol. 41, no. 3, pp. 855–865, 2005.
- [4] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, “Medium-voltage multilevel converters—state of the art, challenges, and requirements in industrial applications,” *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581–2596, 2010.
- [5] P. Azer, S. Ounie, and M. Narimani, “A new post-fault control method based on sinusoidal pulse width modulation technique for a neutral point clamped (npc)

- inverter,” in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 2499–2504.
- [6] D. G. Holmes, B. P. McGrath, D. Segaran, and W. Y. Kong, “Dynamic control of a 20kw interleaved boost converter for traction applications,” in *2008 IEEE Industry Applications Society Annual Meeting*, 2008, pp. 1–8.
- [7] T. Evans, T. Hanada, Y. Nakano, and T. Nakamura, “Development of sic power devices and modules for automotive motor drive use,” in *2013 IEEE International Meeting for Future of Electron Devices, Kansai*, 2013, pp. 116–117.
- [8] M. Salcone and J. Bond, “Selecting film bus link capacitors for high performance inverter applications,” in *2009 IEEE International Electric Machines and Drives Conference*, 2009, pp. 1692–1699.
- [9] M. Khan, P. Magne, B. Bilgin, S. Wirasingha, and A. Emadi, “Laminated busbar design criteria in power converters for electrified powertrain applications,” in *2014 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2014, pp. 1–6.
- [10] N. Feng, W. Qian, and L. Fei, “Research on hybrid dc-link capacitor bank with high efficiency and long-life time,” *2019 3rd International Conference on Electronic Information Technology and Computer Engineering (EITCE)*, pp. 611–615, 2019.
- [11] H.-C. In, S.-M. Kim, and K.-B. Lee, “Design and control of small dc-link capacitor-based three-level inverter with neutral-point voltage

- balancing,” *Energies*, vol. 11, no. 6, 2018. [Online]. Available: <https://www.mdpi.com/1996-1073/11/6/1435>
- [12] H. In, S. Kim, and K. Lee, “Design and control of small dc-link capacitor-based three-level inverter with neutral-point voltage balancing,” *Energies*, vol. 11, p. 1435, 2018.
- [13] Y. Wang, J. Mistry, P. Azer, and B. Bilgin, “Integrated busbar design for stray inductance and volume reduction in a high-power sic traction inverter,” in *2021 SAE International*, 2021.
- [14] Y. Gao, S. Chen, B. Kong, W. Wang, and Y. Cheng, “Epoxy/pvdf/epoxy composite film with concurrent enhancement in energy density and charge-discharge efficiency,” in *2020 5th Asia Conference on Power and Electrical Engineering (ACPEE)*, 2020, pp. 866–870.
- [15] H. Gashtil, V. Pickert, D. Atkinson, D. Giaouris, and M. Dahidah, “Comparative evaluation of field oriented control and direct torque control methodologies in field weakening regions for interior permanent magnet machines,” in *2019 IEEE 13th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, 2019, pp. 1–6.
- [16] D. G. Holmes and T. A. Lipo, *CarrierBased PWM of Multilevel Inverters*, 2003, pp. 453–530.
- [17] B. Wu and M. Narimani, *Two-Level Voltage Source Inverter*, 2017, pp. 93–117.
- [18] S. Haghbin and T. Thiringer, “Dc bus current harmonics of a three-phase pwm

- inverter with the zero sequence injection,” in *2014 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2014, pp. 1–6.
- [19] J. K. Sahu, S. K. Mishra, and K. Hariharan, “Harmonic analysis of three phase inverter by using particle swarm optimization technique,” in *2019 International Conference on Smart Systems and Inventive Technology (ICSSIT)*, 2019, pp. 1158–1162.
- [20] B. Tan, Z. Gu, K. Shen, and X. Ding, “Third harmonic injection spwm method based on alternating carrier polarity to suppress the common mode voltage,” *IEEE Access*, vol. 7, pp. 9805–9816, 2019.
- [21] J. Jose, G. Goyal, and M. Aware, “Improved inverter utilisation using third harmonic injection,” in *2010 Joint International Conference on Power Electronics, Drives and Energy Systems 2010 Power India*, 2010, pp. 1–6.
- [22] D. G. Holmes and T. A. Lipo, *Modulation of ThreePhase Voltage Source Inverters*, 2003, pp. 215–258.
- [23] Shanmei Cheng, Yajun Liu, and Bing Wu, “Svm algorithm of three-level npc inverter,” in *2008 3rd IEEE Conference on Industrial Electronics and Applications*, 2008, pp. 2194–2198.
- [24] A. Mbarushimana and X. Ai, “Real time digital simulation of pwm converter control for grid integration of renewable energy with enhanced power quality,” in *2011 4th International Conference on Electric Utility Deregulation and Restructuring and Power Technologies (DRPT)*, 2011, pp. 712–718.

- [25] X. Liu and A. M. Cramer, “Three-phase inverter modeling using multifrequency averaging with third harmonic injection,” in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–6.
- [26] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, “Recent advances and industrial applications of multilevel converters,” *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, 2010.
- [27] R. Marquardt, “Modular multilevel converters: State of the art and future progress,” *IEEE Power Electronics Magazine*, vol. 5, no. 4, pp. 24–31, 2018.
- [28] B. K. Bose, “Power electronics and motor drives recent progress and perspective,” *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2, pp. 581–588, 2009.
- [29] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. . M. Prats, and M. A. Perez, “Multilevel converters: An enabling technology for high-power applications,” *Proceedings of the IEEE*, vol. 97, no. 11, pp. 1786–1817, 2009.
- [30] J. Rodriguez, Jih-Sheng Lai, and Fang Zheng Peng, “Multilevel inverters: a survey of topologies, controls, and applications,” *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, 2002.
- [31] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, “Multilevel voltage-source-converter topologies for industrial medium-voltage drives,” *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 2930–2945, 2007.



- [32] T. A. Meynard and H. Foch, “Multi-level conversion: high voltage choppers and voltage-source inverters,” in *PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, 1992, pp. 397–403 vol.1.
- [33] A. Nabae, I. Takahashi, and H. Akagi, “A new neutral-point-clamped pwm inverter,” *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518–523, 1981.
- [34] Z. Du, L. M. Tolbert, B. Ozpineci, and J. N. Chiasson, “Fundamental frequency switching strategies of a seven-level hybrid cascaded h-bridge multilevel inverter,” *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 25–33, 2009.
- [35] F. Khoucha, S. M. Lagoun, K. Marouani, A. Kheloui, and M. E. H. Benbouzid, “Hybrid cascaded h-bridge multilevel-inverter induction-motor-drive direct torque control for automotive applications,” *IEEE Transactions on Industrial Electronics*, vol. 57, no. 3, pp. 892–899, 2010.
- [36] S. J. Lee, H. S. Bae, and B. H. Cho, “Modeling and control of the single-phase photovoltaic grid-connected cascaded h-bridge multilevel inverter,” in *2009 IEEE Energy Conversion Congress and Exposition*, 2009, pp. 43–47.
- [37] Z. Du, B. Ozpineci, L. M. Tolbert, and J. N. Chiasson, “Dc-ac cascaded h-bridge multilevel boost inverter with no inductors for electric/hybrid electric vehicle applications,” *IEEE Transactions on Industry Applications*, vol. 45, no. 3, pp. 963–970, 2009.
- [38] A. Shukla, A. Ghosh, and A. Joshi, “Flying-capacitor-based chopper circuit

- for dc capacitor voltage balancing in diode-clamped multilevel inverter,” *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2249–2261, 2010.
- [39] Jing Huang and K. A. Corzine, “Extended operation of flying capacitor multilevel inverters,” *IEEE Transactions on Power Electronics*, vol. 21, no. 1, pp. 140–147, 2006.
- [40] J. Häring, M. Gleissner, W. Wondrak, and M. M. Bakran, “Efficiency and cost comparison of b6 and hybrid anpc converters for traction drives,” in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, 2020, pp. 1–10.
- [41] F. Z. Peng, W. Qian, and D. Cao, “Recent advances in multilevel converter/inverter topologies and applications,” in *The 2010 International Power Electronics Conference - ECCE ASIA -*, 2010, pp. 492–501.
- [42] H. Shin, K. Lee, J. Choi, S. Seo, and J. Lee, “Power loss comparison with different pwm methods for 3l-npc inverter and 3l-t type inverter,” in *2014 International Power Electronics and Application Conference and Exposition*, 2014, pp. 1322–1327.
- [43] K. Cai, B. Liu, Z. Xu, Y. Kang, and S. Cheng, “General analysis on imbalanced voltage of dc capacitors in npc three-level inverter,” in *2011 International Conference on Electrical Machines and Systems*, 2011, pp. 1–6.
- [44] J. Artal-Sevil, J. Lujano-Rojas, C. Bernal-Ruiz, and I. Sanz-Gorrachategui, “Analysis of power losses in a three-phase inverter 3l-npc. comparison with different pwm modulation techniques,” 06 2018, pp. 1–9.

- [45] P. Azer, S. Ouni, and M. Narimani, “A novel fault-tolerant technique for active-neutral-point-clamped inverter using carrier-based pwm,” *IEEE Transactions on Industrial Electronics*, vol. 67, no. 3, pp. 1792–1803, 2020.
- [46] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, “The age of multilevel converters arrives,” *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28–39, 2008.
- [47] M. Tariq, M. Meraj, A. Azeem, A. I. Maswood, A. Iqbal, and B. Chokkalingam, “Evaluation of level-shifted and phase-shifted pwm schemes for seven level single-phase packed u cell inverter,” *CPSS Transactions on Power Electronics and Applications*, vol. 3, no. 3, pp. 232–242, 2018.
- [48] B. Wu and M. Narimani, *Diode-Clamped Multilevel Inverters*, 2017, pp. 143–183.
- [49] M. Hari, A. Verma, R. R. Halakurki, R. R. Ravela, and P. Kumar, “A dynamic analysis of svm based three-level npc for a 3-phase induction motor,” in *2018 International Conference on Power Energy, Environment and Intelligent Control (PEEIC)*, 2018, pp. 162–167.
- [50] Zhang Yingchao, Zhao Zhengming, Lu Ting, Zhang Yongchang, and Yuan Liqiang, “A novel control scheme for three-level npc back-to-back converter,” in *2008 IEEE Vehicle Power and Propulsion Conference*, 2008, pp. 1–5.
- [51] K. Li, M. Wei, C. Xie, F. Deng, J. M. Guerrero, and J. C. Vasquez, “A generalized discontinuous pwm based neutral point voltage balancing method for three-level npc voltage source inverter with switching losses reduction,” in *2017*

- IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 1816–1820.
- [52] X. Lin, S. Gao, J. Li, H. Lei, and Y. Kang, “A new control strategy to balance neutral-point voltage in three-level npc inverter,” in *8th International Conference on Power Electronics - ECCE Asia*, 2011, pp. 2593–2597.
- [53] F. Guo, T. Yang, S. Bozhko, and P. Wheeler, “A novel virtual space vector modulation scheme for three-level npc power converter with neutral-point voltage balancing and common-mode voltage reduction for electric starter/generator system in more-electric-aircraft,” in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 1852–1858.
- [54] B. Fan, W. Zhao, W. Yang, and R. Li, “A simplified svpwm algorithm research based on the neutral-point voltage balance for npc three-level inverter,” in *2012 IEEE International Conference on Automation and Logistics*, 2012, pp. 150–154.
- [55] H. Kitidet and Y. Kumsuwan, “A cb-svpwm control strategy for neutral-point voltage balancing in three-level npc inverters,” in *TENCON 2017 - 2017 IEEE Region 10 Conference*, 2017, pp. 1766–1771.
- [56] K. Anuradha and G. R. Krishna, “Neutral point voltage level stabilization and dc link capacitors voltage balance in neutral point clamped multilevel inverters,” in *2016 11th International Conference on Industrial and Information Systems (ICIIS)*, 2016, pp. 838–843.

- [57] D. Pan, M. Chen, X. Wang, H. Wang, F. Blaabjerg, and W. Wang, “Emi modeling of three-level active neutral-point-clamped sic inverter under different modulation schemes,” in *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*, 2019, pp. 1–6.
- [58] A. C. Schittler and C. Mueller, “Loss-optimized active neutral-point clamped inverter in a lowinductive power-module design,” in *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2020, pp. 1–7.
- [59] J. Rąbkowski and T. Płatek, “Comparison of the power losses in 1700v si igt and sic mosfet modules including reverse conduction,” in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 2015, pp. 1–10.
- [60] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, “A survey of wide bandgap power semiconductor devices,” *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155–2163, 2014.
- [61] J. Rabkowski, D. Peftitsis, and H.-P. Nee, “Silicon carbide power transistors: A new era in power electronics is initiated,” *IEEE Industrial Electronics Magazine*, vol. 6, pp. 17–26, 2012.
- [62] C. Jung, “Power up with 800-v systems: The benefits of upgrading voltage power for battery-electric passenger vehicles,” *IEEE Electrification Magazine*, vol. 5, no. 1, pp. 53–58, 2017.
- [63] J. de Santiago, H. Bernhoff, B. Ekergård, S. Eriksson, S. Ferhatovic, R. Waters,

- and M. Leijon, “Electrical motor drivelines in commercial all-electric vehicles: A review,” *IEEE Transactions on Vehicular Technology*, vol. 61, no. 2, pp. 475–484, 2012.
- [64] J. I. Leon, S. Vazquez, and L. G. Franquelo, “Multilevel converters: Control and modulation techniques for their operation and industrial applications,” *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2066–2081, 2017.
- [65] D. Ronanki and S. S. Williamson, “Modular multilevel converters for transportation electrification: Challenges and opportunities,” *IEEE Transactions on Transportation Electrification*, vol. 4, no. 2, pp. 399–407, 2018.
- [66] A. Edpuganti and A. K. Rathore, “A survey of low switching frequency modulation techniques for medium-voltage multilevel converters,” *IEEE Transactions on Industry Applications*, vol. 51, no. 5, pp. 4212–4228, 2015.
- [67] F. Richardeau and T. T. L. Pham, “Reliability calculation of multilevel converters: Theory and applications,” *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4225–4233, 2013.
- [68] A. Poorfakhraei, M. Narimani, and A. Emadi, “A review of multilevel inverter topologies in electric vehicles: Current status and future trends,” *IEEE Open Journal of Power Electronics*, vol. 2, pp. 155–170, 2021.
- [69] —, “A review of modulation and control techniques for multilevel inverters in traction applications,” *IEEE Access*, vol. 9, pp. 24 187–24 204, 2021.
- [70] B. Wang, S. Dong, S. Jiang, C. He, J. Hu, H. Ye, and X. Ding, “A comparative study on the switching performance of gan and si power devices for bipolar

- complementary modulated converter legs,” *Energies*, vol. 12, no. 6, 2019. [Online]. Available: <https://www.mdpi.com/1996-1073/12/6/1146>
- [71] K. Shirabe, M. Swamy, J. Kang, M. Hisatsune, Y. Wu, D. Kebort, and J. Honea, “Advantages of high frequency pwm in ac motor drive applications,” in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 2977–2984.
- [72] BorgWarner. (2019) Hvh series electrical motor. [Online]. Available: <https://www.borgwarner.com/technologies/electric-drive-motors/hvh-series-electric-motor>
- [73] G. Park, J. Song, S. Jung, Y. Kim, H. Shim, and J. Kim, “analysis of power inverter parasitic inductances effect on switching characteristics for accurate electromagnetic interference (emi) estimation,” in *2017 IEEE International Symposium on Electromagnetic Compatibility Signal/Power Integrity (EMCSI)*, 2017, pp. 277–282.
- [74] S. Labs. (2019) Si827x data sheet. [Online]. Available: <https://www.silabs.com/documents/public/data-sheets/Si827x.pdf>
- [75] P. Azer, R. Rodriguez, H. Ge, J. Bauman, P. S. Ravi, and A. Emadi, “Time efficient integrated electro-thermal model for bidirectional synchronous dc-dc converter in hybrid electric vehicles,” in *2018 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2018, pp. 55–62.

- [76] A. N. Laboratory. (2015) Dynamometer database 2015-chevrolet-spark-ev. [Online]. Available: <https://www.anl.gov/es/energy-systems-d3-2015-chevrolet-spark-ev>
- [77] R. Tarvirdilu-Asl and J. Bauman, “Efficiency analysis of induction motor control strategies using a system-level ev model,” in *2019 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2019, pp. 1–6.
- [78] Cree. (2019) C3m0015065k. [Online]. Available: <https://www.wolfspeed.com/media/downloads/1632/C3M0015065K.pdf>
- [79] Infineon. (2019) Imza65r027m1h. [Online]. Available: [https://www.infineon.com/dgdl/Infineon-IMZA65R027M1H-DataSheet-v02\\_00-EN.pdf?fileId=5546d4626f229553016f85d997f90532](https://www.infineon.com/dgdl/Infineon-IMZA65R027M1H-DataSheet-v02_00-EN.pdf?fileId=5546d4626f229553016f85d997f90532)
- [80] ROHM. (2019) Sct3030alhr. [Online]. Available: <https://fscdn.rohm.com/en/products/databook/datasheet/discrete/sic/mosfet/sct3030alhr-e.pdf>
- [81] ST. (2019) Sctw90n65g2v. [Online]. Available: <https://www.st.com/resource/en/datasheet/sctw90n65g2v.pdf>
- [82] G. SYSTEMS. (2019) Gs66516t. [Online]. Available: <https://gansystems.com/wp-content/uploads/2018/04/GS66516T-DS-Rev-180422.pdf>
- [83] U. SiC. (2019) Uj4c075018k4s. [Online]. Available: [https://unitedsic.com/datasheets/DS\\_UJ4C075018K4S.pdf](https://unitedsic.com/datasheets/DS_UJ4C075018K4S.pdf)
- [84] Infineon. (2019) Infineon optimostmpower mosfet datasheet explanation. [Online]. Available: <https://www.infineon.com/dgdl/Infineon+-+Application+>



Note+-+OptiMOS+Power+MOSFET+Datasheet+Explanation+-+English.  
pdf?fileId=db3a30433b47825b013b6b8c6a3424c4

- [85] E. Related. (2019) How to read a power mosfet datasheet. [Online]. Available: <https://www.embeddedrelated.com/showarticle/809.php>
- [86] T. Instruments. (2019) Ucc21750-q1 10-a source/sink reinforced isolated single channel gate driver for sic/igbt with active protection, isolated analog sensing and high-cmti. [Online]. Available: [https://www.ti.com/lit/ds/symlink/ucc21750-q1.pdf?ts=1618683179351&ref\\_url=https%253A%252F%252Fwww.google.com%252F](https://www.ti.com/lit/ds/symlink/ucc21750-q1.pdf?ts=1618683179351&ref_url=https%253A%252F%252Fwww.google.com%252F)
- [87] H. Wen, W. Xiao, X. Wen, and P. Armstrong, “Analysis and evaluation of dc-link capacitors for high-power-density electric vehicle drive systems,” *IEEE Transactions on Vehicular Technology*, vol. 61, no. 7, pp. 2950–2964, 2012.
- [88] Jih-Sheng Lai, H. Kouns, and J. Bond, “A low-inductance dc bus capacitor for high power traction motor drive inverters,” in *Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344)*, vol. 2, 2002, pp. 955–962 vol.2.
- [89] N. Feng, W. Qian, and L. Fei, “Research on hybrid dc-link capacitor bank with high efficiency and long-life time,” in *2019 3rd International Conference on Electronic Information Technology and Computer Engineering (EITCE)*, 2019, pp. 611–615.
- [90] H.-C. In, S.-M. Kim, and K.-B. Lee, “Design and control of small dc-link

- capacitor-based three-level inverter with neutral-point voltage balancing,” *Energies*, vol. 11, p. 1435, 06 2018.
- [91] Y. A. I. Mohamed, A. A. A. Radwan, and T. K. Lee, “Decoupled reference-voltage-based active dc-link stabilization for pmsm drives with tight-speed regulation,” *IEEE Transactions on Industrial Electronics*, vol. 59, no. 12, pp. 4523–4536, 2012.
- [92] Jih-Sheng Lai, H. Kouns, and J. Bond, “A low-inductance dc bus capacitor for high power traction motor drive inverters,” in *Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344)*, vol. 2, 2002, pp. 955–962 vol.2.
- [93] M. Anwar, M. K. Alam, S. E. Gleason, and J. Setting, “Traction power inverter design for ev and hev applications at general motors: A review,” in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 6346–6351.
- [94] S. Chowdhury, E. Gurpinar, and B. Ozpineci, “High-energy density capacitors for electric vehicle traction inverters,” in *2020 IEEE Transportation Electrification Conference Expo (ITEC)*, 2020, pp. 644–650.
- [95] J. W. Kolar, T. M. Wolbank, and M. Schrodler, “Analytical calculation of the rms current stress on the dc link capacitor of voltage dc link pwm converter systems,” in *1999. Ninth International Conference on Electrical Machines and Drives (Conf. Publ. No. 468)*, 1999, pp. 81–89.
- [96] P. A. Dahono, Y. Sato, and T. Kataoka, “Analysis and minimization of ripple

- components of input current and voltage of pwm inverters,” in *IAS '95. Conference Record of the 1995 IEEE Industry Applications Conference Thirtieth IAS Annual Meeting*, vol. 3, 1995, pp. 2444–2450 vol.3.
- [97] P. Mantzanas, C. Hasenohr, T. Duerbaum, A. Bucher, A. Pawellek, D. Kuebrich, and H. Hofmann, “A fast and accurate calculation method for predicting the dc-link voltage ripple in battery-fed pwm inverter systems,” in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2018, pp. 1–8.
- [98] VISHAY. (2019) Metallized polypropylene film capacitors dc-link capacitor. [Online]. Available: <https://www.vishay.com/docs/28164/mkp1848dcl.pdf>
- [99] W. Electronic. (2019) Redcube press-fit right angled with two rows pin-plate wp-ratr. [Online]. Available: <https://www.mouser.ca/datasheet/2/445/7461103-1723527.pdf>
- [100] X. Zhu, D. Su, Y. Zhang, and L. Wei, “Bus bar design for emc performance of power converters in fuel cell electric vehicles,” in *2006 IEEE International Conference on Vehicular Electronics and Safety*, 2006, pp. 144–147.
- [101] H. Gui, Z. Zhang, R. Chen, R. Ren, J. Niu, B. Liu, H. Li, Z. Dong, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, and B. B. Choi, “A simple control to reduce device over-voltage caused by non-active switch loop in three-level anpc converters,” in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 1337–1343.
- [102] H. Gui, R. Chen, J. Niu, Z. Zhang, F. Wang, L. M. Tolbert, D. J. Costinett,

- B. J. Blalock, and B. B. Choi, “Design of low inductance busbar for 500 kva three-level anpc converter,” in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 7130–7137.
- [103] R. Ren, Z. Zhang, B. Liu, R. Chen, H. Gui, J. Niu, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, and B. B. Choi, “Multi-commutation loop induced over-voltage issue on non-active switches in fast switching speed three-level active neutral point clamped phase leg,” in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 1328–1333.
- [104] A. D. Callegaro, J. Guo, M. Eull, B. Danen, J. Gibson, M. Preindl, B. Bilgin, and A. Emadi, “Bus bar design for high-power inverters,” *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2354–2367, 2018.
- [105] J. Allocco, “Laminated bus bars for power system interconnects,” in *IEE Colloquium on Passive Components for Power Electronic Systems (Digest No. 1998/261)*, 1998, pp. 5/1–5/7.
- [106] PCBWay. (2019) Advanced pcb-fr4 tg170. [Online]. Available: [https://www.pcbway.com/pcb-products/Advanced\\_PCB\\_FR4\\_TG170.html](https://www.pcbway.com/pcb-products/Advanced_PCB_FR4_TG170.html)
- [107] N. Instruments. (2019) Pollution degree rating for electrical equipment. [Online]. Available: <http://www.ni.com/>
- [108] CHIPQUIK. (2019) Solder paste no-clean sn63/pb37 in 10cc syringe 35g t5 mesh. [Online]. Available: <http://www.chipquik.com/datasheets/SMD291AX10T5.pdf>

- [109] J. Ao, Z. Wang, J. Chen, L. Peng, and Y. Chen, “The cost-efficient gating drivers with master-slave current sharing control for parallel sic mosfets,” in *2018 IEEE Transportation Electrification Conference and Expo, Asia-Pacific (ITEC Asia-Pacific)*, 2018, pp. 1–5.
- [110] T. Instruments. (2019) Tms320f2837xd dual-core microcontrollers technical reference manual. [Online]. Available: <https://www.ti.com/lit/pdf/spruhm8>