Advanced Control of Regenerative Cascaded H-Bridge (CHB) Motor Drives

ADVANCED CONTROL OF REGENERATIVE CASCADED H-BRIDGE (CHB) MOTOR DRIVES

BY

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To my parents, Youlin & Guiying.

Abstract

Medium-voltage (MV) motor drives have found widespread applications in various heavy industries, such as in the oil and gas sectors, production plants, and process industries. Conventional cascaded H-bridge (CHB) multilevel inverters dominate the medium-voltage industrial drives domain due to their modularity, scalability, and reliability. The most prevalent CHB topology in the drive industry is based on the diodes-front-end (DFE) rectifier, which greatly limits the industrial application of the conventional CHB drives where the ability of handling regeneration is required. The main objective of this thesis is to develop a low-cost, high performance, reliable regenerative CHB drive. The thesis is concentrating on reducing the grid-tied filter size, shrinking the DC-link capacitors, improving the system's performance and reliability through advanced control techniques.

First, to reduce the number of passive filter components, a new sideband harmonic active filtering strategy based on the carrier-shifting method is proposed for regenerative CHB drives. This proposed approach extends the carrier shifted PWM method for regenerative CHB drives to further reduce the required passive filter size significantly and thus improves the overall size, cost, and efficiency while complying with IEEE Std 519-2014 grid standard. Second, a novel voltage ripple controller is proposed to reduce the dc-link capacitance in the three-phase regenerative CHB drive without adding extra measurements. Third, to achieve a faster dynamic

response and the multi-objective performance during the control of CHB drives, a novel high-performance predictive control with long prediction horizons is proposed to improve the control performance of the CHB multilevel inverters. The formulation of the proposed high-performance finite control set model predictive control (FCS-MPC) is explained in detail and analyzed to reduce the real-time computation burden. Last, when a fault is detected in the regenerative CHB drive system, the reliability and fault-tolerant ability are considered as the main issues. To improve the drive system reliability, a non-symmetrical selective harmonic elimination (SHE) formulation is proposed to extend the output voltage range with a good harmonic profile under post-fault conditions.

Experimental validation of the proposed algorithms is presented for the operation of a scaled-down seven-level regenerative CHB drive system. These proposed techniques make the regenerative CHB drive a promising solution for future medium-voltage regenerative drive applications in terms of cost, performance, and reliability.

Acknowledgments

First and foremost, I would like to express my sincere gratitude to my supervisor, Dr. Mehdi Narimani, for his generous supports during my whole Ph.D. career. He teaches me how to become a good researcher and how to deal with different dilemmas in my life. This would be a priceless treasure for me.

Many thanks also to my colleagues in HiPEL, especially Ahmed Hisham, Sarah Badawi, and Shaoyi Yuan, for their generous help in my research and common efforts in building up the experimental prototype and discussing the new ideas. I cannot forget the days and nights we worked together in HiPEL.

I would also like to thank Dr. Navid Zargari and Dr. George Cheng from Rockwell Automation Canada for their guidance and support. They generously share with us their opinions from an industrial perspective. Their discussions motivate me to widen my knowledge to deal with real-world challenges.

Great thanks go to my parents: Mr. Youlin Ni and Mrs. Guiying He. But for them, it is impossible to complete my Ph. D degree abroad.

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Chapter 1

Introduction

1.1. Motivation

Medium-voltage (MV) motor drives have found widespread applications in various high power industries, such as in the oil and gas sectors, production plants, and process industries. The design of controlled high power MV drives is faced with a number of challenges that relate to the topologies and control of grid-side and motor-side converters [1]. On the one hand, high quality of voltage and current waveforms both at the input and output terminals is important, particularly with MV drives. Many different control schemes are applied to the converter to operate at low switching frequency with good performance [2]-[4]. On the other hand, to overcome the voltage and current limitation of power semiconductor devices, numerous different converter topologies have been developed for MV application in recent years [5].

Unlike the low voltage range application, where the two-level voltage source inverter has become the dominant solution, different MV converter topologies are available in the market.

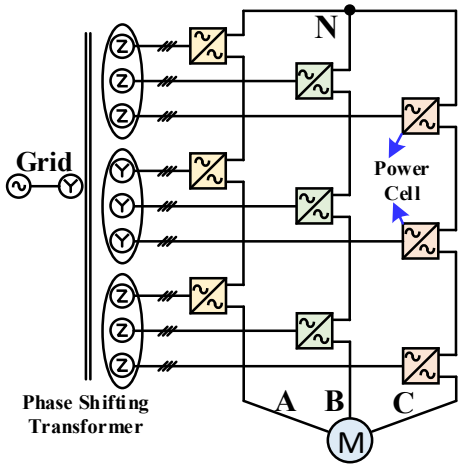
The circuit topologies used in MV industrial converters are divided into three categories: voltage source inverters (VSIs), current source inverters (CSIs), and cycloconverters (CCs). The insulated gate bipolar transistor (IGBT) and insulated gate-commutated transistor (IGCT) are usually adopted in the VSIs. In CSIs and CCs, gate-commutated transistors (GCTs) and symmetrical blocking thyristors are employed.

With the rapid development of power semiconductor devices, multilevel voltage-source converters have gained more interest due to their improvement in overall performance [1]. Some of the features of multilevel converters are a reduction in the total harmonic distortion of the AC output waveforms, less switching losses, less switching stresses (dv/dt), an increase in the operating voltage of the converter, and a reduction in the size of interface transformers and output filters [6][7]. Neutral point clamped (NPC) converter, modular multilevel converter (MMC) and Cascaded H-bridge (CHB) converter are the well-established multilevel converters, which are already commercialized by manufacturers in MV drive applications.

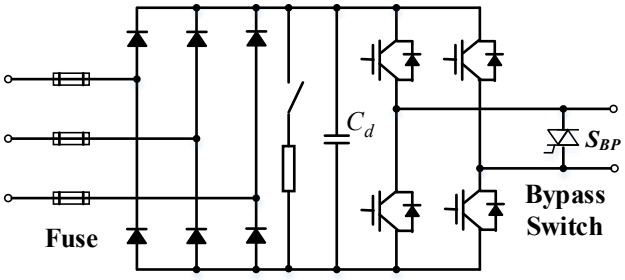
Siemens, ABB, and Rockwell Automation are the market leaders in medium voltage multilevel voltage source drives. In Siemens, the NPC topology-based drives GM150 are equipped with the high voltage IGBT/IGCT. The output voltage range of GM150 drives is from 2.3 kV to 4.16 kV [8]. There are two main issues for NPC topology operating at a higher number of levels: dc-link capacitor voltage balancing issue and a significant increase in the number of clamping diodes. At the same time, both the MMC drives GH150 and CHB drives GH180 can reach 11 kV with low voltage IGBTs due to their modular structures. The modular structure, which connects more devices in series and clamps the voltages between respective devices, are highly attractive due to their scalability in terms of voltage range and power levels. Modular technology is capable of reaching medium output voltage levels using only standard low-voltage

mature technology components. This characteristic allows one to achieve high-quality output voltages, input currents. However, the MMC converter has a voltage balancing issue for the motor operating at a lower speed. What's more, the ABB releases the counterparts CHB drives ACS580MV drives [9]. The converter output voltage range of ABB is the same as those at Siemens. Meanwhile, Rockwell Automation produces the PowerFlex 6000 CHB MV drives for the motor rated from 2.3 kV to 11 kV up to 11 MW [10]. From the industry perspective, CHB multilevel inverters are the most popular solution in the high-power MV drive industry.

CHB inverter is composed of a number of H-bridge power cells, which are cascaded in the motor side to achieve the full medium voltage range with low harmonic distortion as shown in Fig. 1(a). An isolated DC supply is required to feed each H-bridge cell. The most prevalent CHB topology in the drive industry is based on the diodes-front-end (DFE) H bridge cell, shown in Fig. 1(b) [11].



(a) CHB Diagram



(b) DFE(non-regen) Power cell

Fig. 1. 1 Seven Level CHB Drive [1]

The isolated DC supplies are obtained through a phase-shifting transformer and three-phase diode rectifiers. The phase-shifting transformer can produce a three-phase set of secondary voltages shifted by a certain angle (depends on the number of secondaries) with respect to the primary voltage. The three-phase rectifiers are fed by secondary windings with phase angle shifted. The angles of the phase-shifting transformer help to eliminate low order harmonics on the primary currents. With a high number of secondaries (typically higher than 9), no additional passive filter or active filter is needed to satisfy the harmonics standards [12].

Due to the DFE, the most prevalent CHB medium-voltage drive illustrated can only operate in two quadrant modes. This limits the industrial application of the conventional CHB drives where the ability of handling regeneration is desired, such as downhill belt conveyors [13] and high power shovel applications [14]. The downhill conveyor is shown in Fig. 1.2 which transports the mineral from the mine to the concentrator.

Fig. 1. 2 Downhill Conveyor [13]

During the downhill moving, the motor will regenerate a large amount of electrical energy to the DC-link capacitors through the H-bridges. To protect the system, this regenerative energy

is wasted on the damping resistor in the DC-link of the CHB drives, which leads to the low efficiency where regeneration happens for a long period. When the amount of ore to be handled is in the range of 100,000 tons/day, the power generated by the conveyor may exceed several megawatts and are wasted [13] [15].

Another example is the industry shovel as is shown in Fig. 1.3, which is a piece of critical high power equipment in every mining industry and their operational availability has an important impact on production. The regenerated energy is wasted during shovel cycle operation when the conventional CHB drives are adopted.

Fig. 1. 3 Mine Shovel [14]

The power regenerated by the load may exceed several megawatts and thus must be delivered to the electrical utility for saving energy. The drive system must be able to transmit the energy of the load back to the three-phase source. Therefore, the next generation of medium voltage CHB drives is preferred to be equipped with the regeneration ability to meet the diverse requirements from the industrial markets.

1.2. Research Objectives and Contributions

Regeneration capability can be achieved by adding an active front end (AFE) rectifier at the input side instead of the DFE in each power cell of the CHB drives as shown in Fig. 1.4. With the existing phase-shifting transformer, the IGBT anti-diodes can still work as the three-phase rectifiers to provide the isolated DC supplies for the power cells during motoring operation.

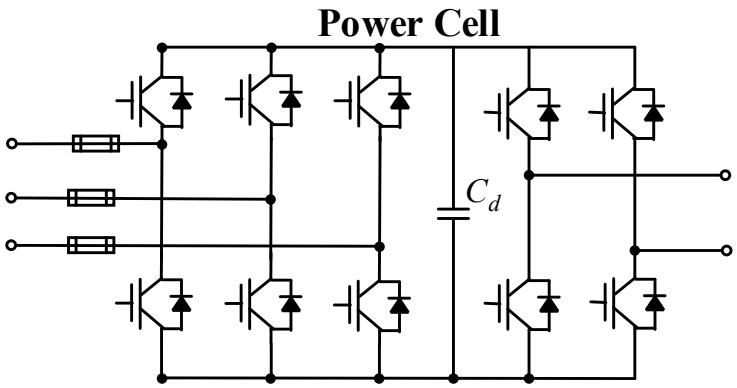


Fig. 1. 4 Three-phase AFE Power Cell

The IGBT based AFE also allows a power flow from the load to the source during regeneration operation. With this regenerative CHB topology, however, there are several emerging challenges required to be tackled:

1. In regeneration operation, AFE introduces the switching harmonics that may deteriorate the grid current quality to the extent that violates the IEEE 519-2014 harmonic standard. Therefore, a filter bank is required between the AFE and the grid, to attenuate current harmonics. Reducing the required filter bank is the crucial point to the CHB drive system cost, volume, and thermal dissipation. However, it has been observed that there is very little information available describing the design of a filter bank for the

regenerative CHB drives. Therefore, designing and optimizing the filter bank for the CHB regenerative drive is a challenge.

2. During regeneration operation, a DC-link voltage controller is required to stabilize the DC-bus voltage and avoid overvoltage damage. However, with the conventional DC-link voltage controller, the instantaneous power in each power cell between the three-phase AFE and the single-phase H bridge is not balanced. This unbalanced power ripple leads to a large designed DC-link capacitance, which increases the system's volume and cost and reduces the system reliability. DC-link capacitance reduction for the CHB regenerative drive is another challenge considering the system cost and life expectancy.

3. To achieve a faster dynamic response and the multi-objective performance during the control of the regenerative CHB drives, the finite control set model predictive control (FCS-MPC) method has been considered one of the most promising alternatives. However, the MPC method requires a high number of computations especially for higher-level power converter topologies due to the existence of a huge amount of switching combinations and redundancies. Real-time searching for the optimal switching state at a high sampling rate is sometimes impossible with the standard commercial processors. Thus, designing a high-performance predictive current controller for the regenerative CHB drive is a challenge.

4. The CHB converters have been widely used for high-power medium-voltage motor drives due to their reliability features. A significant indicator of the reliability is the maximum balanced line-to-line voltage amplitude under fault conditions. It is challenging to improve the fault-tolerant ability for the CHB drives with a good

harmonic profile under different fault situations after the fault is detected in the CHB drives.

1.3. Publications

This thesis researches the feasibility of the regenerative CHB drive for future medium-voltage regenerative industrial drive domain. The author contributes to several original developments, which are presented in the dissertation and briefly summarized as follows:

1. New sideband harmonic active filtering strategies are proposed for regenerative CHB drives to reduce the number of passive filter components, and thus improves the overall size, cost, and efficiency while complying with IEEE std 519-2014 grid standard.
2. A novel voltage ripple controller is proposed to reduce the dc-link capacitance in the three-phase AFE based regenerative CHB drive without adding extra measurements.
3. A novel high-performance finite control set model predictive control (FCS-MPC) with long prediction horizons is proposed to improve the control performance of the CHB multilevel inverters.
4. In extremely high power applications where reliability and switching power loss are critical, the selective harmonic elimination (SHE) technique is more suitable for CHB drives which can eliminate a higher number of harmonics with a lower switching number. To improve the system reliability under high power applications, a non-symmetrical SHE formulation is proposed for CHB drives to extend the

output voltage range with a good harmonic profile under different post-fault conditions.

5. An experimental setup is developed to validate the feasibility of the proposed algorithms.

During the time spent working on the thesis, I was also involved in other research projects. Below is a list of all the journal papers and conferences as a result of my work during the Ph. D.:

Journal Papers:

[J1] **Z. Ni**, A. Abuelnaga, and M. Narimani "A Novel High-Performance Predictive Control Formulation for Multilevel Inverters", IEEE Transactions on Power Electronics, vol. 35, no. 11, pp. 11533 - 11543, 2020.

[J2] **Z. Ni**, A. Abuelnaga, and M. Narimani "A New Fault-Tolerant Technique based on Non-Symmetry Selective Harmonic Elimination for Cascaded H-Bridge Motor Drives", IEEE Transactions on Industrial Electronics, April 2020 (Early Access, DOI: 10.1109/TIA.2020.3000712), 11 pages.

[J3] **Z. Ni**, A. Abuelnaga, S. Yuan, S. Badawi, M. Narimani, Z. Cheng, and N. Zargari, "A New Approach to Input Filter Design for Regenerative Cascaded-H-Bridge (CHB) Drives," accepted in IEEE Transactions on Industrial Electronics.

[J4] **Z. Ni**, A. Abuelnaga and M. Narimani, N. Zargari, "DC-link Voltage Ripple Control of Regenerative CHB Drives for Capacitance Reduction," accepted in IEEE Transactions on Industrial Electronics.

[J5] S. Yuan, **Z. Ni**, A. Abuelnaga, B. Sarah, M. Narimani, and N. Zargari, "A New Method to Reduce Current Harmonics of DC-link Capacitors in Grid-tied Cascaded H-bridge Converters, " submitted to IEEE Transaction on Industry Application, under review.

[J6] S. Badawi, A. Abuelnaga, **Z. Ni**, S. Yuan, M. Narimani, Z. Cheng, N. Zargari, "Reduced Switch-Count Topology for Regenerative Cascaded H-Bridge (CHB) Medium-Voltage Drives," submitted to IEEE Transaction on Power Electronics, under review.

[J7] M. Norambuena, F. Carnielutti, A. Mokhtar, M. Narimani, **Z. Ni**, and A. Abuelnaga, "Finite Control Set Model Predictive Control for Multilevel Converters with Reduced Switching Frequency," submitted to IEEE Transaction on Industrial Electronics, under review.

Conference Papers:

[C1] **Z. Ni** and M. Narimani, "A New Fast Formulation of Model Predictive Control for CHB STATCOM," IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal, pp. 3493-3498, 2019.

[C2] **Z. Ni**, M. Narimani and N. R. Zargari, "Optimal LCL Filter Design for a Regenerative Cascaded H-Bridge (CHB) Motor Drive," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, pp. 3038-3043, 2020.

[C3] **Z. Ni**, and M. Narimani, "A New Model Predictive Control Formulation for CHB Inverters," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, pp. 2462-2466, 2020.

[C4] **Z. Ni**, M. Narimani, J. Rodriguez. "A New Model Predictive Control to Reduce Common-Mode Voltage (CMV) of a Four-Level T-NNPC Inverter ", accepted in Applied Power Electronics Conference (APEC), 2021.

The following project is under development and will be published soon:

[1] **Z. Ni**, M. Narimani, and J. Rodriguez "A Novel Fast MPC Formulation Considering Line-to-Line Redundancy based on 5L T-NNPC", to be submitted to IEEE Transaction on Power Electronics.

[2] **Z. Ni**, M. Narimani " A Filterless Control of Regenerative CHB Drives with Maximum DC Voltage Utilization", Under developing, to be submitted to IEEE Transactions on Industrial Electronics.

1.4. Thesis Outlines

This thesis will be concentrated on the advanced control techniques to tackle the illustrated four challenges of the three-phase AFE based regenerative CHB drives. The thesis is comprised of the following six chapters to targeting the mentioned issues one by one. Following is a brief of each chapter:

Chapter 1 provides the motivation and challenges regarding regenerative CHB MV drives and outlines the contributions.

Chapter 2 conducts a review of the conventional CHB drives and analysis the requirements for grid-tied filter size, challenges of the size of the DC-link capacitors, and reliability issue of the CHB drives.

In Chapter 3, first of all, an optimal LCL filter design procedure for a regenerative CHB motor drive is proposed to satisfy the grid harmonic requirement of IEEE Std 519-2014. To take system performance (such as grid impedance, PLL performance, controller saturation) into consideration while minimizing the LCL filter, an optimization framework based on the genetic algorithm (GA) is proposed directly based on the Simulink nonlinear model instead of the tedious mathematical model. Simulation validates the performance of the designed LCL filter using a seven-level regenerative CHB motor drive. Moreover, to further reduce the number of passive filter components, new sideband harmonic active filtering strategies based on the carrier-shifting method are proposed for regenerative CHB drives. This proposed approach extends the carrier shifted PWM method for regenerative CHB drives to further reduce the required passive filter size significantly and thus improves the overall size, cost, and efficiency while complying

with IEEE Std 519-2014 grid standard. The proposed optimal active filtering strategy method is validated experimentally using a seven-level regenerative CHB drive with only small L filters.

In Chapter 4, the relation between the DC-link capacitance and the instantaneous power flow is researched in detail for the regenerative CHB drives. Then a novel voltage ripple controller is proposed to reduce the dc-link capacitance in the three-phase AFE based regenerative CHB drive without adding extra measurements. A high-performance adaptive filter is proposed to accurately detect the dc-bus voltage ripple amplitude and phase angle, which are later employed to determine the reference current of the AFE. Moreover, the potential instability issue is pointed out and discussed. The proposed voltage ripple controller can avoid unstable operation points, which is ignored by the existing control strategies. The effectiveness of the proposed controller is validated on a regenerative seven-level CHB drive to reduce the dc-link capacitance and dc-link voltage ripple.

In Chapter 5, to achieve a faster dynamic response and the multi-objective performance during the control of CHB drives, a novel high-performance predictive control with long prediction horizons is proposed to improve the control performance of the CHB multilevel inverters. First of all, the conventional cost function based FCS-MPC for the seven-level CHB drive is illustrated. Then the formulation of the proposed high-performance FCS-MPC is explained in detail and analyzed to reduce the real-time computation burden. Experimental results obtained from a prototype are represented to confirm the effectiveness and feasibility of the proposed FCS-MPC formulation. The proposed FCS-MPC controller in Chapter 5 for the CHB drives is targeting at improving the system dynamic performance and the multi-objective performance. However, in some applications, reliability is the main objective for the controller,

especially when operating with extremely high power applications. This leads to the reliability research of chapter 6 when the faults are detected in the CHB drives.

When a fault is detected in the regenerative CHB drive system, the reliability and fault-tolerant ability are considered as the main issues. To improve the drive system reliability in high power applications, Chapter 6 proposed a non-symmetrical SHE formulation to extend the output voltage range with a good harmonic profile under post-fault conditions. The conventional fault-tolerant method fundamental frequency phase-shifted compensation method (FPSC) is extended with the third-order harmonic injection technique to improve the output voltage range. The mathematical formulation of the proposed FPSC non-symmetrical SHE method under different fault situations is introduced and analyzed in detail. The effectiveness of the proposed method is validated through experiments based on a seven-level CHB drive under fault situations.

Different modulation schemes such as SPWM, MPC and SHE are adopted at the motor side in this thesis to satisfy different industrial requirements. For extremely high power MV CHB drives, it is preferrable to operate at a low switching frequency where SHE is a better solution compared with SPWM and MPC. When high dynamic performance is desired, the MPC is a better solution at a higher switching frequency. It is noted that, in a real MV CHB drive product, different modulation schemes can be adopted for different application purposes. In Chapter 7, the contents of the thesis are summarized and the conclusions that have been reached as a result of the work are presented. The main contributions of the thesis are illustrated. The chapter also concludes by suggesting potential future research that can be done based on the thesis work.

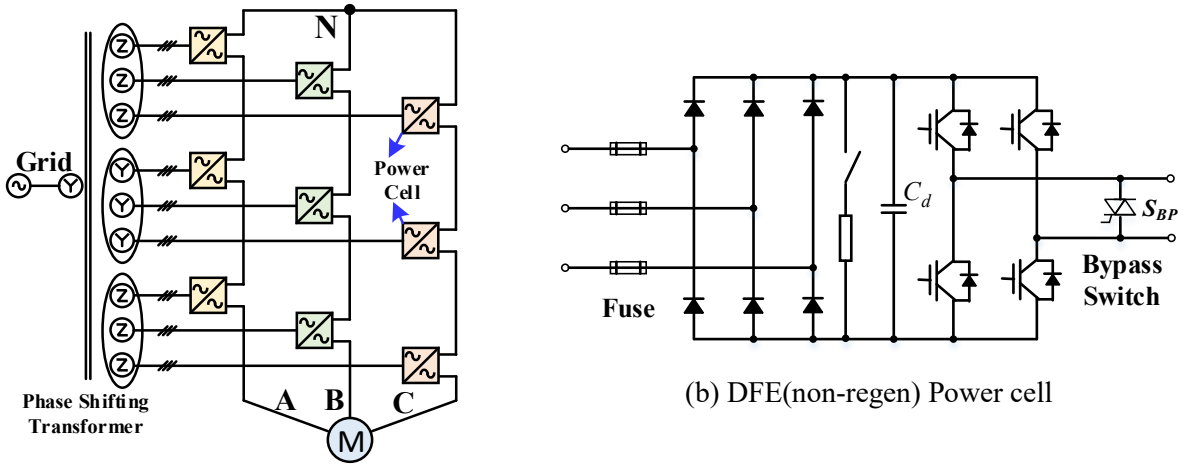
Chapter 2

Introduction to Regenerative CHB Motor Drives

2.1. Introduction

The general structure block diagram of the conventional CHB MV drive is shown in Fig. 2.1. It is comprised of a phase-shifting transformer and a number of H-bridge power cells. The output of the H-bridge power cells is series-connected (cascaded) together on the motor side to achieve the full medium voltage range with low harmonic distortion. The output voltage step for each power cell is relatively small and a phase-shifted pulse width modulation (PSPWM) switching pattern is used, so output harmonics and torque pulsations at the motor are minimal, even at lower speeds. This technology allows standard motors to be used for new applications without the requirement for output filtering. The number of the cascaded power cells is mainly

determined by the desired output voltage, harmonic content, and cost. In commercial CHB drive products [10], the number of power cells ranges from 9 cells at 2.3 kV to 24 cells at 11 kV up to 11 MW.



(a) CHB Diagram

(b) DFE(non-regen) Power cell

Fig. 2. 1 Seven Level CHB Drive

An isolated DC supply is required to feed each H-bridge cell. As it is shown in Fig. 2.1 (b), the most prevalent CHB topology in the drive industry is based on the three-phase diodes-front-end (DFE) H bridge power cell. The isolated DC supplies are obtained through a phase-shifting transformer and three-phase diode rectifiers. The phase-shifting transformer can produce a three-phase set of stepping-down secondary voltages shifted by a certain angle with respect to the primary voltage. The three-phase diode-rectifiers are fed by secondary windings with phase angle shifted. The angles of the phase-shifting transformer help to eliminate low order harmonics on the primary currents. In the case of CHB MV drives, the phase-shifting transformer is feeding 6-pulse diode rectifiers in each cell. Typically, the secondary winding groups are designed to be shifted from each other by (60^o/m), where m is the number of cells in each phase. With a high

number of secondaries (typically higher than 9), no additional passive filter or active filter is needed to satisfy the IEEE std 519-2014 harmonic standard.

Due to the DFE, the most prevalent CHB medium voltage drive illustrated in Fig 2. 1 can only operate in two quadrant modes. This limits the industrial application of the conventional CHB drives where the ability of handling regeneration is desired, such as downhill belt conveyors and high power shovel applications. The power generated by the load may exceed several megawatts and thus must be delivered to the electrical unity. Therefore, the next generation of medium voltage CHB drives is preferred to be equipped with the regeneration ability to meet the diverse requirements from the industrial markets.

Regeneration capability in conventional CHB drives can be achieved by replacing the diode-ridge front end (DFE) with either a single-phase or three-phase active front end (AFE) rectifier at the input of each power cell of the CHB drives. An AFE rectifier allows a bidirectional power flow between load and source. The drive system can transmit the energy of the motor back to the three-phase power source. Different topologies for the regenerative CHB drives are proposed in the existing literature.

As is shown in Fig. 2.2, a regenerative power cell for CHB drives is proposed in [16]. In this structure, instead of a three-phase DFE in Fig. 2.1 (b), a single H-bridge rectifier is adopted in the AFE. The single-phase transformers, instead of three-phase transformers, are utilized for the isolation.

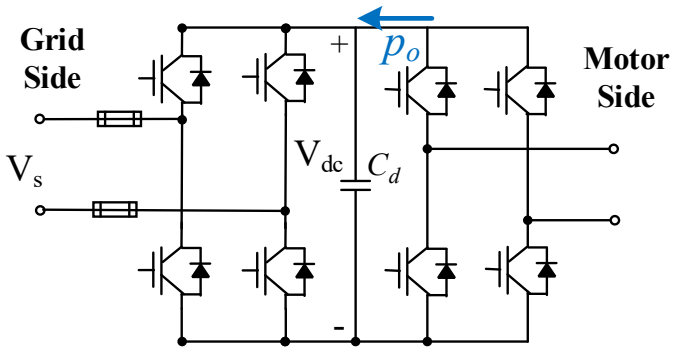


Fig. 2. 2 Single-phase H-bridge AFE Regenerative Power Cell

As is shown in Fig. 2. 2, any amount of the regenerative power p_o that comes from the load motor has to be delivered by the single-phase AFEs immediately. If not, the reversal of regenerative power flow will accumulate at the DC-link and consequently raise the DC link voltage above the system safety range, which is very dangerous for the drive system. Therefore, a DC-link voltage controller is required to be designed for the AFEs to stabilize the DC-bus voltage and avoid overvoltage damage during regeneration. The main objective of the DC-link voltage controller is to control the DC-link voltage within the system safety range by delivering the "suitable" amount of power to the grid.

The block diagram of the control system for the single-phase AFE is shown in Fig. 2.3, where V_{dc} is the dc voltage measurement and Vs is the grid voltage. PI-1 is adopted to control the dc capacitor voltage by setting a "suitable" current reference to be injected to the grid. PI-2 is employed to track the reference current generated by the PI-1 through modulation waveform. The modulator generates the gating signals for the AFE based on the modulation waveform. The control strategy of the PWM single-phase rectifier is well known and is explained with more details in [16].

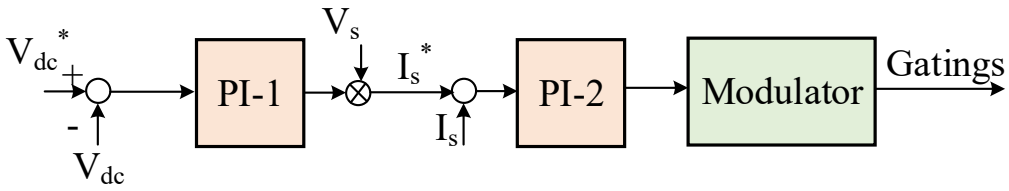


Fig. 2. 3 Control Scheme of Full bridge AFE [16]

Beyond the full-bridge AFE topology, in [17] and [18], the single-phase half-bridge PWM rectifiers shown in Fig. 2. 4 are utilized as the front end of cascaded H-bridge modules. Only two power semiconductors are needed in each of the rectifiers. The single-phase transformers are utilized for isolation. An extra dc offset compensation control loop is required to tackle the voltage imbalance issue between the capacitors C_1 and C_2.

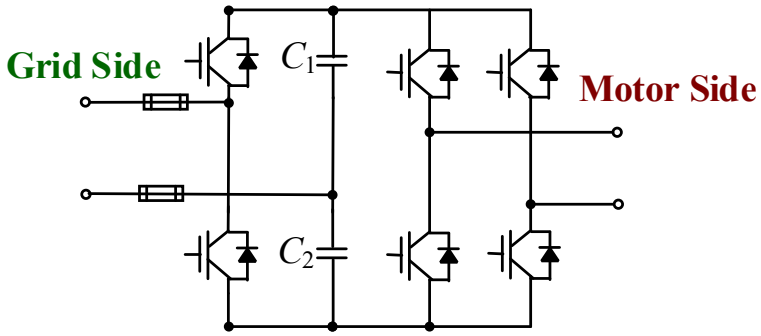


Fig. 2. 4 Half-bridge AFE Regenerative Power Cell

However, the CHB inverters comprised of single-phase front-end power cells are vulnerable to grid disturbance [19], which increases the concerns related to harmonic pollution [20]. On the other hand, CHB drives with a three-phase PWM rectifier front end had gained a lot of attention from the manufacturers.

In [21]-[23], the three-phase two-level PWM rectifiers are utilized as the front end of cascaded H-bridge modules shown in Fig. 2. 5. During the motoring operation, the IGBTs are kept off-state to avoid switching loss. The IGBT anti-diodes work as the three-phase rectifiers to

provide the isolated DC supplies for the power cells, which is equivalent to the conventional DFE CHB drives. Meanwhile, during the regeneration mode, the AFEs start to operate to deliver the energy from the motor side to the grid. The bidirectional power flow between the motor and the grid is achieved with the minimum changed to the conventional CHB drives, which is a big advantage to manufacturers.

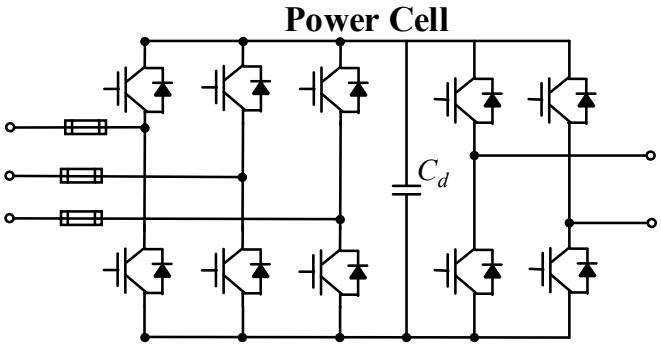


Fig. 2. 5 Three-phase AFE Regenerative Power Cell

As mentioned, a DC-link voltage controller is required to be designed for the AFEs to stabilize the DC-bus voltage and avoid overvoltage damage during regeneration. It is shown in Fig. 2.6, the DC voltage controller is implemented with the help of the *dq* rotating frame, where the measured grid voltage and current are denoted as V_{sx} and I_{sec_rx}, where x=(a, b, c). The voltage controller is adopted to control the dc capacitor voltage by injecting a suitable amount of I_d^*. The current controller does nothing more than tracking the reference current by generating the modulation waveform. The reference currents are represented in *dq* axis as I_d^* and I_q*. The reference current in *q* axis I_q* is set to zero to avoid reactive power injection. The sinusoidal pulse width modulation (SPWM) modulation is adopted to generate the IGBTs gating of the AFEs. The dc-link voltage is controlled both in regeneration mode, which allows a bidirectional power flow between load and source.

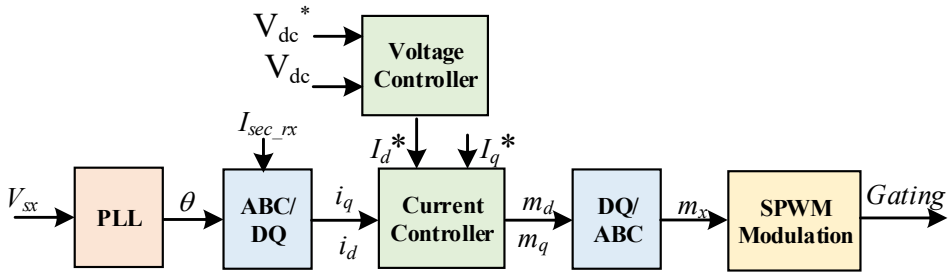


Fig. 2. 6 Three-phase AFE Control Scheme

The main focus of the research for this thesis has been focused on the three-phase AFE based regenerative CHB drives shown in Fig. 2. 7. This is because this power cell configuration can provide four-quadrant operation with minimal changes to the conventional DFE CHB drives with the same transformer structure. Meanwhile, the IGBT anti-diodes work as the three-phase rectifiers to provide the isolated DC supplies for the power cells during motoring. With the phase-shifting transformer, the merits of the conventional DFE CHB drives are kept in the regenerative drives, which is desirable from the engineering perspective [24].

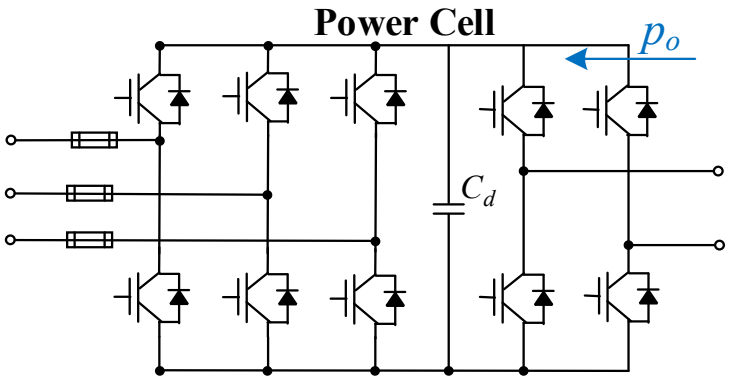


Fig. 2. 7 Three-phase AFE Regenerative Power Cell

2.2. Grid-Tied Filter Design Challenges

Although the regeneration capability can be achieved by the three-phase AFE regenerative CHB drives. However, in regeneration mode, AFE introduces the switching harmonics that may not be canceled by the phase-shifting transformer. The resulting harmonics may deteriorate the grid current quality to the extent that violates the IEEE 519-2014 harmonic standard [25]. Therefore, a filter bank is required between the AFE and the grid, to attenuate current harmonics [26], which is shown in Fig. 2.8. Reducing the required filter bank is the crucial point to the CHB drive system cost, volume, and thermal dissipation. However, it has been observed that there is very little information available describing the design of a filter bank for the regenerative CHB drives.

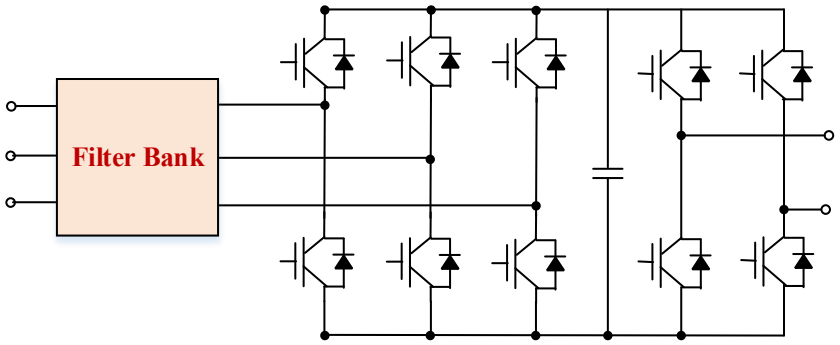


Fig. 2. 8 Filters for the Three-phase AFE

2.2.1. Optimal LCL Filter Design Challenge for CHB AFEs

An L filter is simple, but it is relatively bulky to achieve a good filtering performance. The alternative solution is the LCL filter [26], which achieves a good filtering performance with a smaller size due to its third-order transfer function. LCL filter suffers from resonance problem and active or passive damping methods should be adopted to stabilize the resonance area of the

LCL filter. In practice, as is shown in Fig. 2. 9, the damping resistor in series with a filter capacitor has been widely adopted to suppress the resonance since the power loss in the damping resistor is low [27]. There are other high order filters such as LTCL and LLCL filter [28][29]. The higher-order filters usually possessed a relatively better frequency attenuation performance, which is suitable for the power inverters. However, it involved more passive components that increase the cost and complexity of the system. Thus, in general, the LCL filter is the most adopted solution since it provides the best trade-offs between the different features.

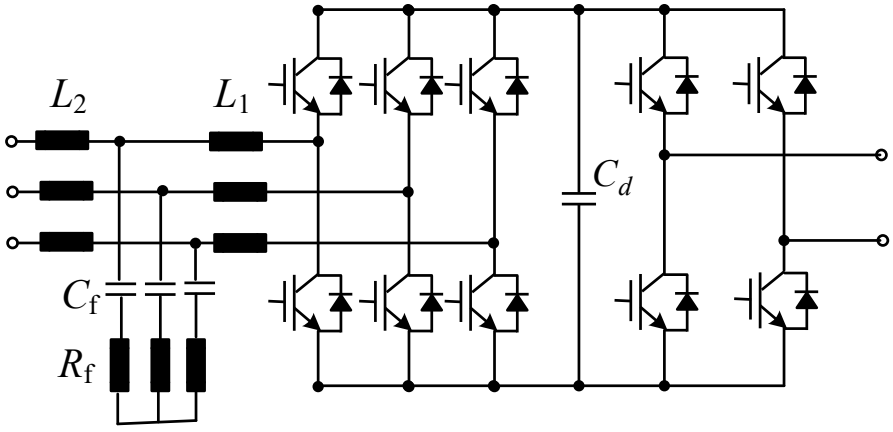


Fig. 2. 9 LCL Filter with Passive Damping Resistor for AFE

In terms of designing the passive damping LCL filters, there are several criteria and design methods discussed in the previous literature. The majority of these proposed methods [26]-[30] are based on the harmonic current amplitude and resonance frequency. It can be summarized as the following steps [26] [30]:

1. Select the converter side inductance L_1 based on the desired maximum current ripple in the inductor.
2. Select the filter capacitance C_f to be no more than 5 % of the base capacitance.

3. Select grid side inductance L_2 based on harmonic current suppression at the switching frequency.
4. Select passive damping resistor R_f based on the resonance frequency.

These LCL filter designing procedures are easy to follow. It is worth mentioning that following these design procedures only based on maximum current ripple suppression may result in a "bad" solution that doesn't necessarily meet the system requirements in different applications. First of all, the designed LCL filter is not necessarily satisfy the IEEE std 512-2014 standard since only the current ripple magnitude is considered in the designing process. Moreover, this design process doesn't take the DC-link voltage capability and power ability limitation [31] into consideration. It may sometimes lead to excess inductance which requires a higher DC-link voltage to deliver the full power. This point has to be taken into consideration since the DC-link voltage is limited by the IGBT rating. Another critical point is that the calculated LCL filter through these procedures is not optimized since minimizes the total inductance and the total capacitance is the ultimate goal.

The LCL filter design procedures applied to the regenerative CHB drives are seldom mentioned. The existing LCL design and optimization methods can be applied to a voltage source inverter. But they cannot be directly applied to the regenerative CHB drives LCL filter design due to the following reasons:

1. To assure the Point of Common Coupling (PCC), the point the power converter connects to the grid, satisfies the grid harmonic requirement of IEEE STD 519 2014. It is required to obtain the current harmonic content at the PCC point (the primary side of the phase-shifting transformer). The existing LCL filter design

methods only consider the current profile at the transformer secondary. The phase-shifting transformer for a seven-level CHB inverter can eliminate the low order harmonics under 17th order harmonics [1]. Moreover, the leakage inductance of the transformer can be considered as an extra filtering inductor;

2. With the phase-shifting transformer, as is shown in Fig. 2. 1, the equivalent grid inductance L_{leak} exists between the ideal power grid and the inverter which cannot be neglected. This inductance can deteriorate the harmonic performance, PLL performance, or even the system stability [32].
3. The DC-link voltage capability and power ability should be taken into consideration [31] to assure that the maximum power can be delivered to the grid with the determined DC voltage.

All in all, to design an optimal LCL filter for a given regenerative CHB inverter, beyond the harmonic performance and filter size, it is necessary to take system performance (such as grid impedance, PLL performance, controller saturation) into consideration due to the existence of the transformer. To consider all these factors while minimizing the LCL filter, a new LCL filter design framework is required to be investigated.

2.2.2. Optimal Filter Design Challenge for CHB AFEs

Increasing the switching frequency can effectively reduce the output current ripple and, thus decrease the filter bank size. However, in high-power applications, a high switching frequency increases the switching loss of the power switches, which leads to low efficiency and the increased heat sink size. Switching frequencies higher than 1 kHz is not desirable in high-

power applications [33]. Therefore, designing and optimizing the filter bank for the CHB regenerative drive operating at a low switching frequency is a challenge.

Second, an extensive amount of literature is available describing filter design for the grid-tied AFE rectifier to satisfy the grid harmonic standard [26],[34]-[36]. Generally speaking, a high order filter is better since it can achieve a better filtering performance with a smaller size such as LCL [26] [34] and LTCL filters [35]. A high-order filter is often adopted to interconnect to the utility grid to suppress the harmonic currents. However, the inherent resonance of the high order filter may trigger the potential instability problem of the system [36]. Moreover, considering the number of power cells in a CHB drive, a large number of passive components increase the overall cost and size of the drive system. Although, with a good filtering performance, these high-order filters are not desirable for the regenerative CHB drives.

All in all, there is a demand for the new filtering strategy for the regenerative CHB drives that tackle the previous challenges. It should allow the system to operate at a low switching frequency with a good grid current quality satisfying the IEEE std 519-2014. More important is that the number and the size of the passive filter components are required to be reduced at the same time.

Researchers have attempted to eliminate the PWM sideband harmonic using the active filtering strategies for parallel-interleaved rectifier/inverters [37]-[39]. With n identical parallel AFEs, where n is the cell number per phase, switching current harmonics can be effectively attenuated when carriers are evenly phase-shifted $360^0/n$ [40]. Carrier interleaving is an effective strategy to improve the input waveform quality of the parallel-connected converters [41]. [41] minimizes the grid current distortion in interleaved grid-connected converters with unequal

terminal voltages. An enhanced carrier interleaved strategy is proposed in [42] to improve both the current THD and line-to-line voltage quality. [43] [44] propose to optimize the harmonic profile by real-time calculating the phase-shifting carrier angles.

It is important to recognize that, in parallel rectifiers, carrier sideband harmonic cancellation is done with the inverters supplied from the equal transformer secondary terminal voltages. But the phase-shifting transformers in the regenerative CHB drive can affect the phase of current sideband harmonics in an unfavorable manner. Although intensive work has been done on the carrier shifting strategies, not enough work has been done on carrier shifting PWM methods with filter reduction for regenerative CHB drives in the existing literature.

2.3. DC-Link Capacitor Size Reduction Challenge

As is shown in Fig. 2. 8, during regeneration, the reversal of regenerative power flow p_o from the load motor has to be delivered by the three-phase AFEs to the grid immediately. Otherwise, this reversal energy can accumulate at the DC-bus and consequently raise the DC link voltage above the system safety range, which is very dangerous for the drive system. Therefore, a DC-link voltage controller is required to be designed for the AFEs to stabilize the DC-bus voltage and avoid overvoltage damage during regeneration. The main objective of the DC-link voltage controller is to control the DC-link voltage within the system safety range by delivering the "suitable" amount of power to the grid.

With the conventional DC-Link voltage controller [45], only a constant power is delivered by the three-phase AFE. The instantaneous power in each power cell between the three-phase AFE and the single-phase H-bridge is not balanced. This unbalanced power ripple has to be absorbed by designing a large DC-link electrolytic capacitor to maintain a stable dc voltage,

which increases the system's volume and cost [46]. Moreover, the pulsating power ripple flowing through the DC-link electrolytic capacitors raises the DC-link voltage fluctuation with twice the output frequency. The temperature rise caused by voltage ripple accelerates the evaporation of the electrolyte, thus reducing the capacitor's life expectancy and the system reliability as well [47],[48].

To reduce the size of the DC-link electrolytic capacitor and to suppress DC-link voltage fluctuation, it is desirable to deliver both the average power and pulsating ripple power through the three-phase AFE in each power cell [46]. In this way, the ripple power is prevented from flowing across the DC-link capacitors, which reduces the required dc-link capacitance to maintains a stable dc voltage. Beyond that, it is worth mentioning that the pulsating ripple power from all the secondary power cells cancels out with each other at the primary side of the transformer in the regenerative CHB [49]. This superb merit allows for injecting the pulsating ripple power to reduce the capacitance in each power cell without deteriorating the grid harmonic profile at the transformer primary side.

Although different control algorithms have been proposed to reduce the dc-link capacitance of regenerative CHB drives, however, the theory beneath these control algorithms is identical: deliver the instantaneous ripple power through the three-phase AFE instead of flowing across the dc capacitors. The control procedure involves the following two stages:

1. The reference input current waveforms of the three-phase AFE is determined based on the instantaneous power [46][49][50][51] or DC-link voltage [52] assuring that the instantaneous power is provided by the AFE instead of the dc-link capacitors;

2. The current controller tracks the determined reference current to suppress the DC-link voltage ripple. It is noted that the reference current may contain different frequency components such as ω_g , $2\omega_m$-ω_g and $2\omega_m$+ω_g [49], where ω_m is the H-bridge output frequency and ω_g is the grid frequency.

[46][51] propose to direct inject the instantaneous power of the H-bridge into the *d*-axis of the current controller (I_d) of the three-phase AFE. But the capacitance reduction is not as good as expected since the proportional-integral (PI) based current controller can not track fast enough the generated reference [46]. [51] improves the performance by adopting the high-performance model predictive current controller. The dc-link voltage ripple is reduced significantly. [49] propose to open-loop inject the instantaneous power using a proportional (P) based current controller. However, in these controllers, it is assumed that the motor side instantaneous power is known. The current and power angle of the motor is required to be measured to determine the reference currents. But these measurements are rarely available in a typical induction motor control system such as *V*/*F* control.

Recently, to avoid adding extra sensors while reducing the DC-link capacitance, [52] proposed to determine the reference current for the three-phase AFE based on the DC-link voltage measurement directly. This concept is developed from [53], where one more control loop is established for the voltage ripple. However, a resonant controller with a lead-compensated phase is required to be tuned to gain enough stability margin [52]. This is not an easy task due to the load frequency variation.

Design a high-performance current tracking controller is an important stage for capacitor reduction. The high-performance current controllers have been extensively researched, which is

not consider as the main challenge so far. A multitude of solutions have been developed includes: hysteresis control [54][55], dead-beat control [56], model predictive control [57], resonant control [58], multiple rotating frames control [59]. These control algorithms can be directly implemented to improve current tracking performance.

To shrink the DC-link capacitance, determining the reference currents for the three-phase AFE directly based on the DC-link voltage ripple is a promising solution when the instantaneous power at the motor side is not measured [52]. A voltage ripple controller can be designed to deliver the instantaneous ripple power through the AFE. However, this voltage ripple controller should be carefully designed since it may impact system stability. This potential instability issue hasn't been given enough attention. Two main challenges of implementing the voltage ripple controller to reduce the DC-link capacitance are:

1. The DC-link voltage ripple frequency varies with the motor speed, which makes it difficult to real-time detect the voltage ripple amplitude and phase angle with accuracy. But these parameters are critical for the three-phase AFE to deliver "suitable" instantaneous ripple power.

2. A more critical issue is the fact that the voltage ripple control system may lose stability in some operation range when excess pulsating power ripple is injected by the AFE.

To tackle the ahead mentioned problems, a novel voltage ripple controller to reduce the dc-link capacitance in the regenerative CHB drive is developed which is explained in Chapter 4 in detail.

2.4. High-Performance Controllers for CHB drives

Besides the filter and capacitor design challenges for the grid-side AFEs in the regenerative CHB drives, there are other challenges for the motor-side cascaded H bridge multilevel inverters in terms of high-performance control. The commercial multilevel inverters are available for decades, however, there is still undergoing research mainly on the new control strategies and modulation techniques to improve the performance [60]-[62] and to achieve multi-objective such as suppressing common-mode voltage (CMV) [63], increasing fault-tolerant ability [64], and balancing floating capacitors [65].

To achieve a faster dynamic response and multi-objective performance during the control of power converters, the finite control set model predictive control (FCS-MPC) method has been considered one of the most promising alternatives in recent years [65]. FCS-MPC predicts the future behavior of the power converter based on the "transient" mathematic model. The switching states of the power converters are determined through a cost function, which represents the system performance. FCS-MPC actually searches the best switching state with minimal cost function among all the available switching states at each sampling step. Compared with classical linear control strategies and modulation techniques based on the average small-signal model and rotating frame [66][67], FCS-MPC combines the current control and modulation into a single computational problem, providing a powerful alternative to conventional proportional-integral (PI) and proportional-integral-resonant (PIR) controllers with a very fast dynamic response.

The implementation challenge in multilevel inverters has motivated the researchers to study different fast computationally efficient MPC formulations. Several model predictive

control schemes are proposed to reduce the computational load by only estimating a reduced subset of redundant switching states or a subset of redundant voltage vectors. In [68][69], Petri nets are introduced to accomplish both current tracking and voltage balancing objectives by estimating only a subset of the switching combinations. However, it requires to calculate the best output voltage level for current regulation in the design process. Instead of estimating the subset of the switching states, [70] proposed to estimate the output voltage vectors to reduce the calculation load. Furthermore, [71] proposed to use the non-redundant voltage vectors instead of all the voltage vectors to shrink the candidate pool of the MPC formulation. For example, a seven-level CHB inverter, all the available switching combinations reach 49 (around 0.26 million). And the available voltage vectors reach 73 (343), 127 of which are non-redundant voltage vectors [71]. With the increase of the output voltage levels, searching for the optimal output voltage vector still remains an issue. To tackle this issue, recently, an online sphere decoding algorithm (SDA) is discussed to speed up the process of searching the optimal output voltage vector [72][73]. The MPC problem is reformulated as an integer least-square optimization problem and then solve by SDA, which is more efficient than exhaustive enumeration methods. But this algorithm requires significant storage of the processor [74]. Beyond that, [75] proposed to replace the optimization problem by solving Diophantine equations over a large set of output voltage vectors. However, this method hasn't been extended into long horizon prediction MPC situations. In the existing MPC formulations, a considerable real-time computation burden is required and the determination of the weighting factors may affect the MPC performance.

It has been recently shown that power converters with long prediction horizon MPC can improve the system steady-state performance, by either reducing the switching frequency or the

total harmonic distortion of output currents when compared to the basic single-step MPCs [76]. However, using long prediction horizons FCS-MPCs in multilevel inverters increases the computation burden for the already exhausted processors. Only limited literature and reference are available on long-horizon prediction FCS-MPC on multilevel inverters due to its huge computation burden. One existing long horizon prediction method is named simplified model predictive direct current control (MPDCC) [77]-[80]. The switch positions are frozen and switching is not allowed when the output currents are within the designed bounds. The number of switching sequences to be evaluated is greatly reduced as a result [79]. Another known long prediction horizon length FCS-MPC adopts enhanced SDA for accelerating the voltage vector optimization process [72]-[74]. The existing algorithm has been demonstrated on a three-level NPC inverter.

Besides the feature of high dynamic performance, FCS-MPC can also achieve multi-objective capability. Especially in the medium-voltage drive application, a large common-mode voltage (CMV) can result in large leakage currents which may cause electromagnetic interference (EMI) problems and bearing failure [63]. In recent years, MPC-based CMV reduction strategies have been studied in different multilevel topologies. In [81][82], a separate cost function is added and designed to suppress CMV. The theory has been tested on a dSPACE based on a matrix converter. The execution time under this case is 80 μs for single-step FCS-MPC. At the same time, to reduce the complexity while reducing the CMV, [63] and [83] proposed to select only part of the adjacent voltage vectors and zero vectors during the MPC optimization. But this means an extra estimation process is still required for the adjacent voltage vectors, which will hinder the application of this method when the inverter output voltage levels increase.

To obtain multi-objective with the long prediction horizon length MPC, a modified long prediction horizon SDA-MPC formulation is explored with reduced CMV in [84]. The experimental validation of the proposed method has been implemented on a dSPACE system. By adopting the SDA optimization in the MPC formulation [84], the execution time of a five-level CHB inverter is 92.2 μs when the prediction length to be 3. In [85], the SDA-MPC formulation is implemented on a three-level converter with dSPACE system, the minimum sampling interval was set to 125 μs in order to real-time find the optimal voltage vector solution when the prediction time step is 4. However, it has to be mentioned that an extra weighting factor is required in the modified SDA optimization process. The chosen of the weight factor for the cost function directly affects the system's stability and performance. A large number of simulations or experiments are required to be done to design the suitable weight factors in order to achieve expected objectives [84][86].

A CHB drive is composed of a number of modular H-bridge power cells and isolated DC voltage sources. The H-bridge cells are cascaded on the load side to achieve medium-voltage with low harmonic distortion. Due to its structure, the CHB inverter is known to have a huge number of switching combinations and voltage vectors. For a 2C+1 level CHB inverter, the number of non-redundancy voltage vectors will boost up to $12C^2+6C+1$ [71], which poses a challenge for implementing the online FCS-MPC algorithm at a high performance!

In summary, to implement high-performance FCS-MPC on CHB drives, there are several challenges to be improved: 1) reduction of the computational loads on microcontrollers, 2) the extension to long prediction horizons, 3) satisfaction of multi-objective simultaneously such as output current control, CMV suppression, and 4) design of weighting factors and cost function.

To address the aforementioned problems, a novel high-performance MPC formulation is proposed and explained in detail in Chapter 5.

2.5. Fault-Tolerant Techniques for CHB drives

As previously explained, the FCS-MPC controller can bring a better control performance for regenerative CHB drives. However, in extremely high power applications where reliability and switching power loss are more critical for the regenerative CHB drives, compared with predictive controllers and conventional phase-shift PWM (PSPWM), the SHE-PWM technique can eliminate a much higher number of harmonics with a low switching frequency and higher reliability. This advantage makes the SHE technique more suitable for CHB drives for extremely high-power applications. This section discussed improving the reliability of the regenerative CHB drives under faults for extremely high-power applications.

The cascaded H-bridge (CHB) converters have been widely used for medium-voltage motor drives due to their scalability and reliability features. The modular configuration offers more possibilities for the medium voltage drive system to operate during faulty conditions [87]. A significant indicator of the reliability is the maximum balanced line-to-line voltage amplitude under fault conditions. In the case of an internal fault in power cells, the cascaded multi-cell converter will shut down the output currents, meanwhile, the faulty cells will be bypassed and then isolated from the system through external switches. The converter will supply the load again if the converter can provide enough balanced line-to-line voltages required by the load under the fault. This fault-tolerant property increases the reliability of the CHB drives.

A seven-level CHB drive system is shown in Fig. 2.1 (a) as an example. In normal operation, the amplitude of the phase voltage generated is equal to 3 V_{dc} (referred to as 3 p.u

hereinafter), where V_{dc} is the dc bus voltage of each power cell. In the case of one cell failure, the achievable voltage levels by the faulty phase are reduced from seven-level (3 p.u) to five levels (2 p.u). As a result, the asymmetrical inverter will provide unbalanced voltages to the load under the fault event. To keep feeding symmetrical line-to-line voltages to the load even under fault conditions, as is discussed in [88], one simplest solution is to bypass an equal number of healthy cells per phase. The symmetry output voltages are achieved with a 33% amplitude reduction, which limits the operation range under fault. To overcome this limitation, alternatives have been presented in the literature under fault cases [89]-[91]. These methods can achieve balanced line-to-line voltages through the renowned fundamental frequency phase-shifted compensation method (FPSC) [92]. Different PWM modulation schemes [93]-[95] have been developed based on the FPSC method. But, in the FPSC method, a set of FPSC nonlinear equations has to be solved. It is worth mentioning that these equations may have multiple solutions, which do not result in the maximum possible value of the output line-to-line voltages with a good harmonic profile. More critical is the fact that, under some fault conditions, the set of nonlinear equations may have no solution by direct assigning the phase voltages amplitude [88] [96].

To overcome the first problem, one alternative solution is to revise the PWM modulation scheme, a new PWM modulation scheme named peak-reduction SPWM modulation is proposed in [91][97]. Compared FPSC-SPWM method [87][88], the peak-reduction method can extend the converter's output voltage region range. An average of the maximum and minimum values of the reference phase voltages are injected into the common-mode voltages to extend the converter's maximum output region. However, this method may introduce a significant output harmonic

distortion since it may force the converter to work in the overmodulation region by injecting excess common-mode voltage [88].

To solve the illustrated overmodulation problem under fault, [88] and [98] proposed an enhanced FPSC SPWM modulation approach under fault conditions to reduce the overmodulation region as much as possible while achieving the maximum amplitude by restricting the injected common-mode voltage. However, small overmodulation may appear in some cases [88]. Another technique maximizing the linear modulation operation region is to inject a common mode component into SPWM references [99]. The injected common-mode components are required to be real-time suppressed to avoid overmodulation operation and unexpected harmonics. Similar methods are found in the FPSC SVM method [94][100], which can get similar output line voltages within the linear operation region under fault. These improved fault-tolerant methods based on FPSC SPWM and FPSC SVM techniques are very powerful to suppress the low harmonic content if the switching frequency is at least around 1 kHz or higher [101]. Injecting common-mode harmonics at low switching frequency using SPWM or SVM modulation can lead to an unacceptable harmonic distortion.

SHE-PWM offers a considerably lower equivalent switching frequency compared to carrier-based PWM techniques, resulting in lower switching power loss and good harmonic performance [102]. In [103], the SHE-PWM technique and conventional phase-shift PWM (PSPWM) technique were compared in detail in CHB inverter applications. It has been proved that the SHE-PWM technique can eliminate a much higher number of harmonics than the conventional PSPWM technique with the same switching number. To further minimize the output current THD, a current reference-based SHE PWM technique is proposed in [104] to eliminate the current THD influenced by grid voltage harmonics. In [105], a new SHM-PWM

control strategy is capable of meeting the harmonic requirement even under nonequal DC link voltages with optimized THD performance.

To expand the symmetry SHE application under the fault condition, [106] and [107] combine the half-wave symmetry SHE method with FPSC method to achieve maximum balanced inverter output line voltage under the fault condition with a good harmonic profile. But the method in [106][107] needs to solve FPSC nonlinear equation to obtain the phase-shifted angle. This angle may not be the optimal angle for extending the maximum output line voltages. Moreover, it is known that the FPSC nonlinear equation may result in no solution under certain fault conditions [88][96], which may hinder the application of this method.

To overcome the problem when solving the FPSC equations, an extension of the FPSC method has been mathematically proposed in [96], the angle between the shorter inverter output voltages is fixed to 180° and the magnitude of the largest vector is adjusted to avoid no solution problem. However, this extension can only be applied to the cases when the converter neutral point is located outside the triangle of the output line-to-line voltage [88]. [88][96] proposed a carrier-based enhanced FPSC-SPWM approach suitable for all fault conditions meanwhile extending the inverter output voltage range and avoid no solution problem. But these methods are not suitable for the medium voltage drives operating at the low switching frequency. There is a need for an implementation technique that can maximize the output line voltages at the low switching frequency operation with a good harmonic profile and achievable for different fault situations.

A non-symmetrical SHE method is adopted for a two-level voltage source inverter in [108]. With the extra degree of freedom from the non-symmetrical SHE, this method is reported

to offer a better harmonic profile compared to the other two symmetrical methods in two-level voltage source inverters [109]. Under the fault situation, the CHB drive is not capable of regenerating rated full power to the grid during braking. The reversal of power flow will consequently raise the DC link voltage above its safety range. Alternatively, DC braking is adopted in commercial drives [110][112]. A DC current is superimposed on the output current. Part of the regenerated energy is dissipated on the electrical machine instead of coming to the DC link [113]. However, the existing symmetrical SHE PWM methods cannot provide a DC component due to the symmetry constraints.

To avoid ahead mentioned problems, a new advanced fault-tolerant technique for the regenerative CHB drive is proposed in Chapter 6 based on the nonsymmetrical SHE method to improve the CHB drive system reliability.

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Chapter 3

Optimal Filter Design for Regenerative CHB Drives

3.1. Introduction

To obtain the regeneration ability, an IGBT-based active front end (AFE) has been developed to replace the diode-based rectifier in the conventional CHB drive. When an AFE power cell is used to regenerate the energy back to the grid, to meet the stringent harmonic requirement from IEEE std 519-2014, an external filter is required to attenuate the switching harmonics generated from pulse-width modulation (PWM). Reducing the required filter bank is the crucial point to the CHB drive system cost, volume, and thermal dissipation. However, it has been observed that there is very little information available describing the design of a filter bank for the regenerative CHB drives.

The IEEE 519-2014 standard of current harmonic limitation is shown in Table 3.1, where total demand distortion (TDD) is the harmonic current distortion against the full load demand of the electrical system. IEEE std 519-2014 set 5% TDD limit for the harmonics below 50th order, which is not difficult to satisfy. However, more critical is the fact that the standard also sets the limit for the individual current harmonic component at the point of common coupling (PCC point. The limit for the individual current harmonic component depends on the component harmonic order. Generally speaking, a more stringent harmonic limit is set for higher-order harmonics below 50th order. Meanwhile, the even harmonics are limited to 25% of the odd harmonic limits. For example, the limitation for the odd and even harmonics between 35th and 50th order becomes as low as 0.3% and 0.075% respectively. This limit for individual harmonics is difficult to achieve for the medium voltage high power converters which usually operating at a low switching frequency. The designed filter should meet the limit of each harmonic component subscribed by the IEEE std 519-2014.

Table 3.1Current Distortion Limits for General Distribution Systems (120V through 69kV) IEEE std 519-2014

Maximum Harmonics Current Distortion in Percent of I_L						
Individual Harmonics Order (Odd Harmonics)						
I_{sc}/I_L	< 11	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	TDD
< 20	4.0	2.0	1.5	0.6	0.3	5.0

TDD: Total demand distortion, harmonic current distortion % of maximum demand load current.

I_{sc}: maximum short current at the point of common coupling (PCC) and I_L: maximum demand load current

Even harmonics are limited to 25% of the odd harmonics limits above

To reduce the cost and volume, there is a demand for a new optimal filtering strategy based on the regenerative CHB drives. It should allow the system to operate at a low switching frequency with a good grid current quality satisfying the IEEE std 519-2014. More important is that the number and the size of the passive filter components are required to be reduced at the same time. To achieve these objectives, five types of filters are studies and investigated for a regenerative CHB drive in this Chapter:

1. An L filter is designed for each power cell on the secondary of the phase-shifting transformer, its performance is studied to investigate whether the L filter can meet the IEEE std 519-2014 requirement.

2. An optimized LCL filter is designed for each regenerative cell on the secondary of the phase-shifting transformer. A new design process combining the genetic algorithm (GA) optimization algorithm is proposed to shrink the size of the designed LCL filter.

3. A new filter design, called ***Method* 1**, is proposed with the L filter on the secondary of the phase-shifting transformer. Meanwhile, a trap filter is adopted on the primary side of the transformer and a carrier-shifting technique is proposed to eliminate certain harmonic content.

4. Another filter design, called ***Method* 2**, is proposed with only the L filter on the transformer secondary side. A novel carrier-phase shifted technique is proposed to eliminate the dominant switching sideband contents injected into the grid and meet the IEEE std 519-2014.

5. Finally, the optimal filter design, called ***Method* 3**, is proposed with an L filter on the transformer secondary side. A new carrier-phase shifted strategy is proposed not only to

satisfy the IEEE std 519-2014 standards but extend the harmonics elimination to a higher-order harmonic profile as well.

In this chapter, the different optimal filters are designed based on a seven-level regenerative CHB drive system. It should be noted that the proposed filter design strategies can be extended to any level of regenerative CHB drives without losing generality. The proposed optimal filter design strategies can be easily extended to any-level regenerative CHB drive system with different system parameters. To further quantify the analysis, some key parameters of the seven-level regenerative CHB drive are specified here. The main parameters of the typical seven-level regenerative CHB drive system are summarized in Table 3.2. These parameters are directly obtained from the main industrial sponsor for this project.

Table 3. 2 Seven-Level Regenerative CHB Drive Filter Design Requirement

Converter parameter	Value
Cell DC bus voltage (V)	1100
Transformer secondary side voltage(V)	650
Transformer primary side voltage (V)	3000
Rated primary side current (A)	135
Switching Frequency(Hz)	1980
Motor Power Rating (MW)	0.7
Modulation Scheme	Sinusoidal Pulse Width Modulation(SPWM)
Inductance (mH)	Less than 5
Primary Current Harmonics Requirement	IEEE std 519-2014

The line-to-line voltage of the primary side phase-shifting transformer is 3000 V (RMS), and its secondary side line-to-line voltage is 650V (RMS). The motor power rating is 0.7 MW. Motor rated voltage is 3000 V (RMS). The primary leakage inductance is 0.048 p.u. of the transformer primary base and the secondary leakage inductance is 0.032 p.u. of its transformer

secondary base. The per-unit base based on the primary transformer is shown in equation (3.1)-(3.3).

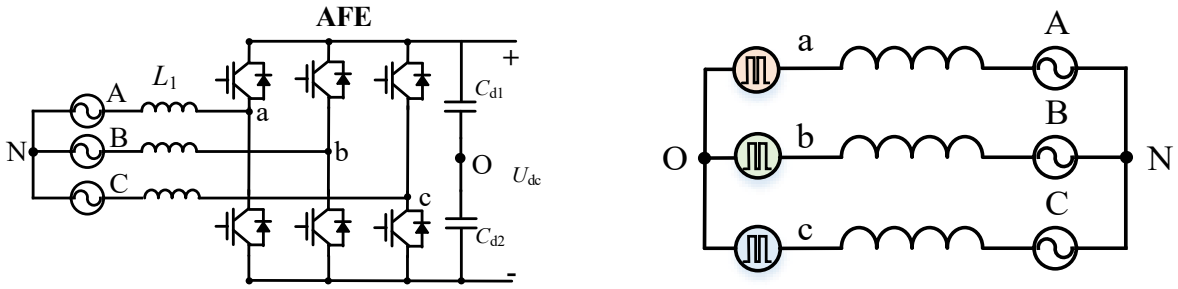
$$Z_{pri} = \frac{U_{pri}^2}{S} = \frac{3000^2}{0.7*10^6} = 12.85\Omega \tag{3.1}$$

$$L_{pri\_mb} = Z_{pri\_mb} / \omega_b = 34.1mH \tag{3.2}$$

$$C_{pri\_mb} = 1/(Z_{pri\_mb}\omega_b) = 0.206mF \tag{3.3}$$

3.2. L Filter Design for a Seven-level Regenerative CHB Drive

In this section, to satisfy the IEEE std 519-2014, an L_1 filter is designed for each power cell between the secondary of the phase-shifting transformer and the AFE. The regenerative power cell AFE side is illustrated in Fig. 3.1 (a). The grid three-phase voltages are V_{AN}, V_{BN}, and V_{CN} respectively. Meanwhile, the output phase voltages of the three-phase AFE are denoted as V_{aO}, V_{bO}, and V_{cO}. The AFE output voltages can be determined by the switching states. For example, when the upper leg of the A-phase IGBT is ON, then the output phase voltage of the AFE V_{aO} $=U_{dc}/2$. Otherwise, $V_{aO} =-U_{dc}/2$ when the bottom leg of the A-phase IGBT is on. The L type grid-connected AFE equivalent model is shown in Fig. 3.1 (b). The designed L_1 filters suffer the voltage difference between the grid and three-phase AFE. Moreover, to satisfy the IEEE std 519-2014, the designed filters should be large enough to suppress the current harmonics flowing into the grid.



(a) L filter type AFE (b) Equivalent Circuit

Fig. 3. 1 L-type grid-connected AFE

As is shown in Fig. 3.1, for the three-phase two-level AFE in the regenerative cell, assume the AFE output phase voltage V_{aO}, V_{bO}, and V_{cO} are generated through the natural sampled SPWM modulation process. The voltage harmonics profile through the modulation process can be expressed in equation (3.4) [37].

$$v_{pn_k} = V_{dc} M \cos(\omega_0 t + \theta_0 - k\frac{2\pi}{3}) + \frac{4V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}\left\{\begin{array}{l}\sin([m+n]\frac{\pi}{2})J_n(m\frac{\pi}{2}M)\cdot \\ \cos(m[\omega_c t+\theta_c]+n[\omega_0 t+\theta_0-k\frac{2\pi}{3}])\end{array}\right\} \tag{3.4}$$

$$m \in N^+, \{n \in Z \mid \mathrm{mod}(n,3) \neq 0\}, k = 0,1,2$$

where M is the modulation index, V_{dc} is the DC voltage, m and n are index integer numbers, J denotes the Bessel function. The frequency and phase angle of the modulation waveform and carrier are θ_o, ω_o and θ_c, ω_c respectively. The triplen sideband harmonics around each carrier multiple are canceled when n is the multiple of 3. From equation (3.4), it is noted that the significant harmonics exist at the switching sideband frequencies such as $f_s \pm 2f_0, 2f_s \pm f_0$,

$3f_s \pm 2f_0, ..., mf_s \pm nf_0$, where f_s is switching frequency and f_0 is output frequency. For instance, when the AFE operates at f_s = 1980 = (33*60) Hz, the voltage sideband harmonics generated by the AFE can be estimated through equation (3.4). There is one significant sideband voltage harmonic group (31th and 35th) located below the 50th order, which contributes to a major part of the grid harmonics. With the determined voltage harmonics profile, the designed L_1 filter should suppress the resulting current harmonics to meet the stringent IEEE standards.

3.2.1. Conventional L Filter Design Procedure

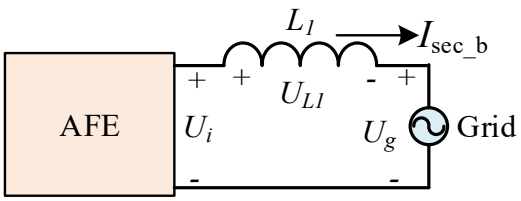
In the full power regeneration situation, the power rating of each cell equals. In this case, the power rating for each cell is 77.8 kW (=0.7MW/9). The secondary line current can be calculated under the full regeneration situation:

$$I_{\text{sec}\_b} = \frac{77.8kW}{\sqrt{3}*650} = 69.1 \text{ A} \tag{3.5}$$

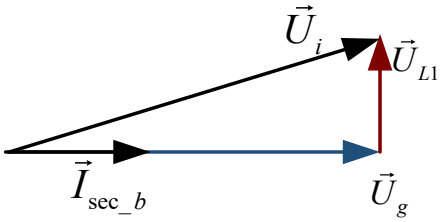
Assume no extra filter is attached for the inverter, during the SPWM scheme without third-order harmonic injection, the minimum DC voltage for each cell is calculated:

$$U_{dc\_\min} = \frac{650}{0.612} = 1062 \text{ V} \tag{3.6}$$

When L_1 filter is designed and attached between the power inverter and the grid, the minimum required dc-link voltage needs to increase since a portion of the voltage will drop on the designed filter.



(a)Phase equivalent circuit



(b) phase vector

Fig. 3. 2 Simplified Single-Phase Equivalent Circuit

The single-phase equivalent circuit of the AFE is shown in Fig. 3.2 (a). The phase vector diagram is shown in Fig. 3.2 (b) when the unit power factor is achieved. Based on Kirchhoff's law, the output phase voltage of the inverter U_i under the rated current situation is

$$\vec{U}_i = \vec{U}_g + j\omega_b I_{sec\_b} L_1 \tag{3.7}$$

where the U_g is the grid phase voltage, I_{sec_b} is the current flows into the grid. When SPWM modulation is adopted with no third-order harmonic injection, the minimum required DC voltage U_{dc_req} with the designed L_1 filter can be calculated through equation (3.8). It should be noted that, if the DC-link voltage is less than $U_{dc\_req,}$ the rated power cannot be regenerated to the grid. This should be taken into consideration in the filter design procedure.

$$\begin{aligned} U_{dc\_req} &= 2\sqrt{2}\sqrt{U_g^2 + (\omega_b I_{sec\_b} L_1)^2} \\ &= 2\sqrt{2}\sqrt{(\frac{650}{\sqrt{3}})^2 + (377 * 69.1 * L_1)^2} \end{aligned} \tag{3.8}$$

The relation between the minimum required DC voltage U_{dc_req} and the designed filter L_1 is shown in Fig. 3.3. With the increase of the designed inductor L_1, the required DC bus voltage is supposed to increase to compensate for the voltage drop on the inductor. However, in practical applications, it is not desirable to increase the DC-link voltage. A higher DC voltage usually means more voltage stress on the IGBTs and a higher insulation level requirement for the power converters. This critical point has to be taken into consideration since the dc-link voltage is usually limited by the IGBT rating and DC capacitor voltage rating. Increasing the IGBT rating or the DC bus capacitors' voltage rating will boost up the system's overall cost. As a result, in this chapter, the maximum allowed DC-link voltage is considered as a critical design constraint when designing the optimal L filter.

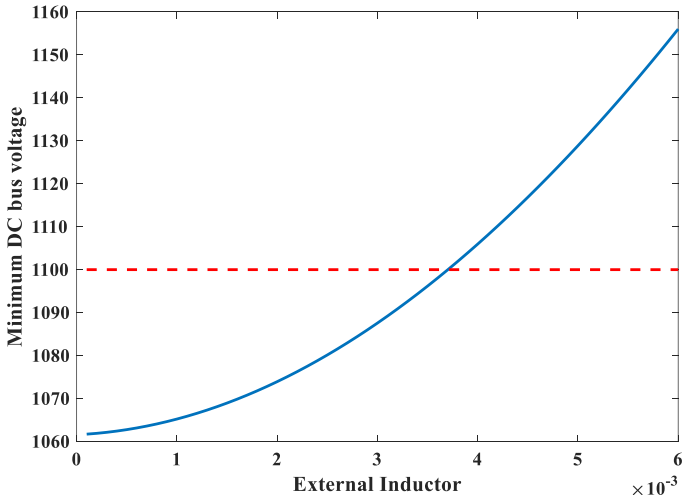


Fig. 3. 3 Relation Between the L_1 Inductance and Minimum Required DC voltage

For the regenerative CHB system, the IGBT rating is assumed to be 1700 V. Then the maximum allowed DC link voltage is limited up to 1100 V considering enough voltage margin. From Fig. 3.3, the maximum allowed inductance under 1100 V DC-link voltage is 3.8 mH.

Considering the transformer leakage inductance, the maximum allowed designed inductance L_1 is 9.9% p.u. (3.4 mH). As the maximum allowed inductance is limited, it should be noted that there might be no L filter solution for the regenerative CHB drive that satisfies the IEEE std 519-2014 at different switching frequencies. This is understandable since the designed L_1 inductor may exceed the maximum allowed inductor if the switching frequency is low. To further investigate this problem, the optimal L_1 filters are designed at different switching frequencies including the desired switching frequency which is 1980 Hz (=33×60Hz).

3.2.2. L Filter Design with 1980 Hz Switching Frequency

The desirable switching frequency for a medium voltage high power regenerative CHB drive system is no more than 1980 Hz, this is due to the reduction in power losses at high power applications. When the switching frequency is fixed at 1980Hz, the optimal L_1 filter is designed for the given CHB regenerative system. The simulation result is shown in Table 3.3 with the maximum allowed L_1 filter (3.4 mH). The current TDD at the transformer primary side is 3.37% meanwhile the current TDD on the secondary side of the transformer is 5.01%, which satisfies the total TDD requirement of the IEEE std 519-2014. However, as is shown in Fig. 3.4, the 31^{th} and 35^{th} order harmonics (switching frequency sideband where m=1 and n=2) exceed the limitation prescribed by IEEE std 519-2014 at the PCC. The 31^{th} and 35^{th} order harmonics are 2.24% and 1.97% with respect to the fundamental component. However, they are required to be suppressed to 0.6% and 0.3% respectively. As is shown in Table 3.4, the individual current harmonic component at the PCC cannot meet the IEEE std 519-2014 with only 1980 Hz switching frequency.

Table 3. 3 L_1 Per unit value for 1980 Hz under 1100V DC voltage

Frequency	L_1 (p.u.)	TDD_pri	TDD_sec
1980	9.9%	3.37%	5.01%

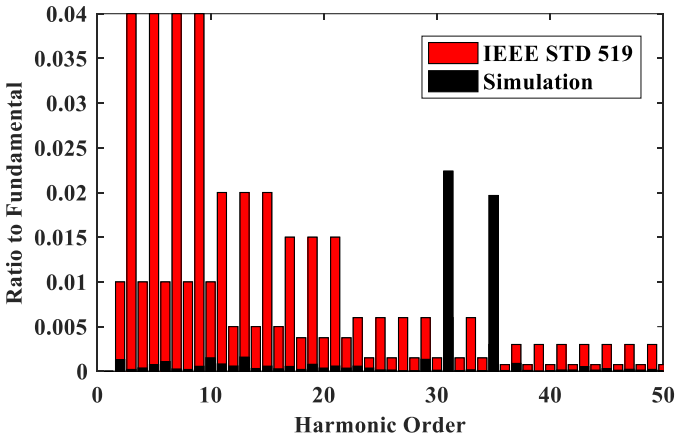
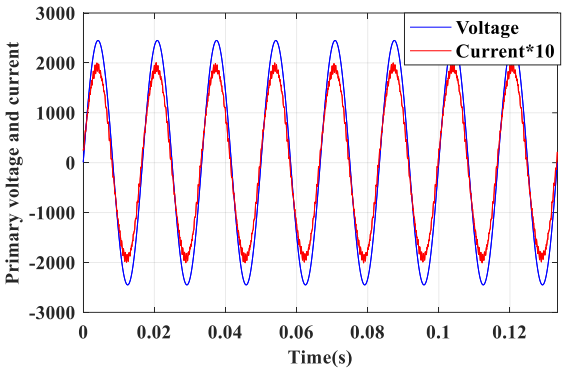


Fig. 3. 4 Individual Harmonic Contents at 1980 Hz

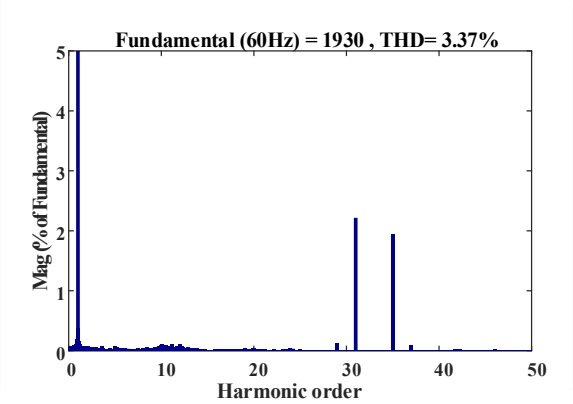
Table 3. 4 Harmonics Exceed the IEEE std 519 2014 Standards under 1980 Hz

Harmonics	31th order	35th order
Limitation	0.6%	0.3%
Simulation	**2.24%**	**1.97%**

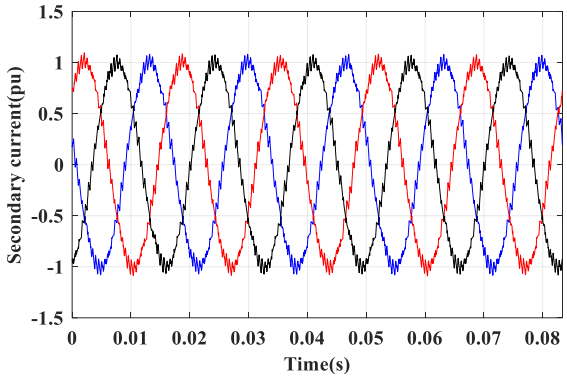
The voltage and current simulation waveforms with the maximum allowed L_1 inductance under 1980 Hz switching frequency are shown in Fig.3.5.



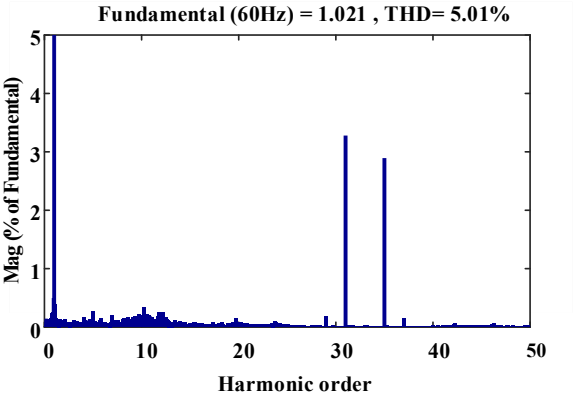
(a)Primary voltage and current waveform



(b)Primary current THD contents



(c)Secondary current waveforms



(d)Secondary current THD contents

Fig. 3. 5 Simulation Result under 1980Hz

Compared with the phase-shifting transformer primary side current and secondary side current shown in Fig. 3.5, the phase-shifting transformer can improve the harmonic profile under 17th order harmonics. However, the 31th and 35th order switching frequency sidebands exceed the limit of the IEEE std 519-2014 standards. With a fixed 1980Hz switching frequency, the *L* filter cannot satisfy the IEEE std 519-2014 harmonic standards with exceeding 31th order and 35th order harmonic components. To meet the IEEE std 512-2014 with an L filter, a higher switching frequency should be adopted under the same operating condition.

3.2.3. L Filter Design with 3000 Hz Switching Frequency

In this section, the switching frequency is increased from 1980 Hz to 3000 Hz. The optimal L_1 filter is designed for the same CHB regenerative system illustrated before where the DC bus voltage remains to be 1100 V. However, there is still no L filter candidate satisfying the current harmonics limits prescribed by IEEE std 519-2014. The simulation under maximum inductor 9.9% p.u. is performed with a 3000 Hz switching frequency. As is shown in Table 3.5, by increasing the switching frequency, the current THD on the primary side of the transformer reduces to 2.27% meanwhile the current THD on the secondary side of the transformer decreases to 3.63%.

Table 3. 5 L_1 Per Unit Value for 3000 Hz under 1100V DC voltage

Frequency	L_1(p.u.)	TDD_pri	TDD_sec
3000	9.9%	2.27%	3.63%

However, the individual current harmonic components at the transformer primary side are shown in Fig. 3.6 and Table 3.6. All other harmonic contents except 48th order are within the limit of the requirement. The 48th order harmonics (switching frequency sideband where m=1, n=2) is 1.44% of the rated current which exceeds the limit of the IEEE std 519-2014. As a result, the maximum allowed inductors could not satisfy the requirement with a 3000 Hz switching frequency.

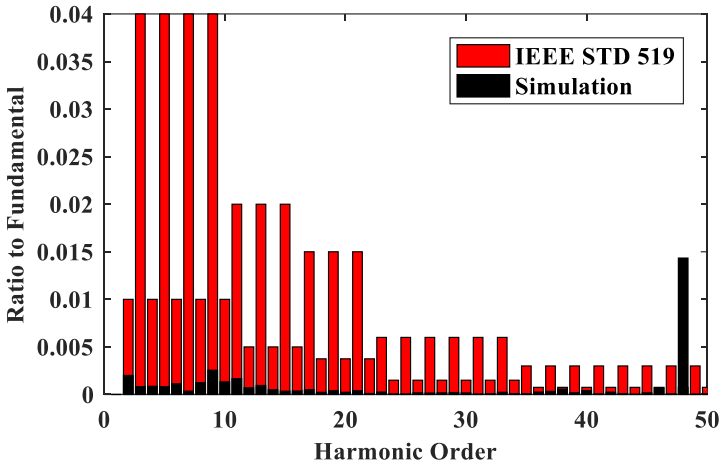
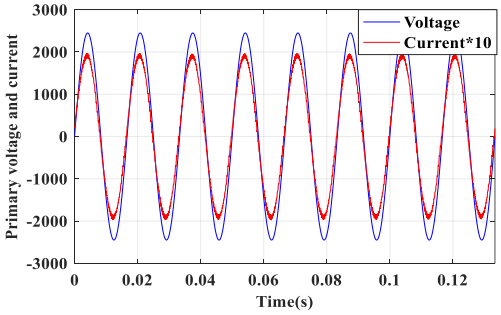


Fig. 3. 6 Individual Harmonic Contents at 3000 Hz

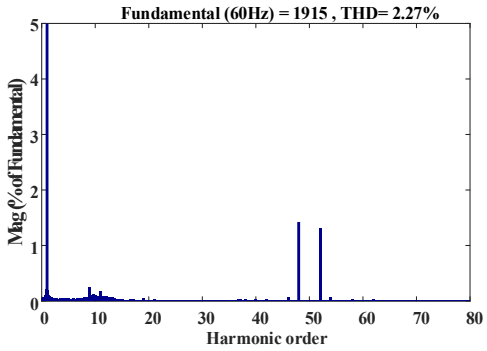
Table 3. 6 Harmonics exceed the IEEE std 519 2014 standards under 3000 Hz

Harmonics	48th order
Limitation	0.075%
Simulation	**1.44%**

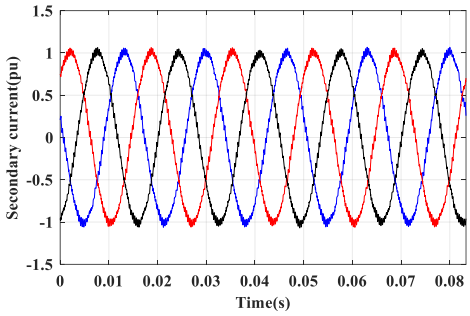
The simulation voltage and current waveforms with the maximum allowed L_1 filter are shown in Fig 3.7. Compare the phase-shifting transformer primary side current with the secondary side current, the harmonic components below 17th order frequency are suppressed with the existence of the phase-shifting transformer. However, the 48th order switching frequency sideband (around 1.44%) exceeds the limit of the IEEE std 519-2014 standards. This denotes that, with a 3000Hz switching frequency, only the L filter cannot satisfy the IEEE standards due to the large switching sideband harmonics. To satisfy the IEEE std 519-2014, the switching frequency is required to be increased over 3 kHz even with the maximum allowed L filter.



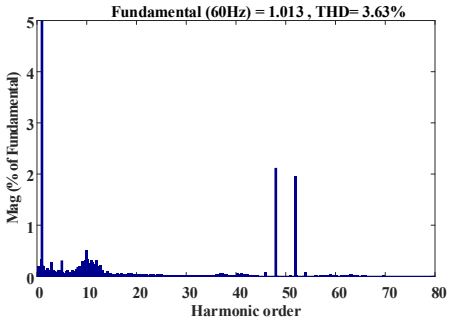
(a)Primary voltage and current waveform



(b)Primary current THD contents



(c)Secondary current waveform



(d)Secondary current THD contents

Fig. 3. 7 Simulation Result under 3000 Hz Switching Frequency

3.2.4. L Filter Design Summary

To satisfy the IEEE std 519-2014 with the conventional L filter, the switching frequency is required to increase to over 3000 Hz for the seven-level regenerative CHB drive. In this section, the optimal L filter is designed under different switching frequencies such as 4020, and 9900 Hz. The design criteria are based on the IEEE std 519-2014 and the DC bus voltage limitation. The simulation results are summarized in Table 3.7.

Table 3. 7 Filter Comparison under Different Switching Frequency with 1100 V DC Bus Voltage

Switching frequency(Hz)	L_1	TDD_P Max=5%	TDD_S Max=20%	31th harmonic	35th harmonic	48th harmonic	Satisfy
1980	9.9%	3.37%	5.01%	2.24%	1.97%	-	No
3000	9.9%	2.27%	3.63%	-	-	1.44%	No
4020	3.08%	4.98%	7.24%	-	-	-	Yes
9900	2.6%	2.25%	3.8%	-	-	-	Yes

The numbers in the red font show that the harmonic content is larger than the limit mentioned in the standard.

As is shown in Table 3.7, to satisfy the IEEE standard, the required inductor L_1 size could shrink to 3.08% p.u with 4020Hz switching frequency and 2.6% p.u. when the switching frequency increases to 9900Hz. When the switching frequency is over 3000 Hz, the carrier frequency sideband falls out of the scope of the 50th order harmonics which is not prescribed by the IEEE std 519-2014. As a result, the IEEE std 519-2014 can be met when the switching frequency is over 3000 Hz.

In summary, for the regenerative CHB system, the 18 pulse phase-shifting transformer can suppress the baseband harmonics under 17th harmonics. When the switching frequency is less than 3000 Hz, the carrier frequency sideband harmonics fall into the domain below 50th order. It is difficult to satisfy the IEEE std 519-2014 standards with only a maximum allowed L_1 filter. Increasing the switching frequency over 3000 Hz can meet the IEEE standard with the same design constraints. However, it is desirable to operate the high-power medium-voltage CHB drive at a low switching frequency. The conventional L filter design strategy cannot meet this requirement since it requires the AFE IGBTs to operate at over 3000 Hz. This lead to the investigation of a new filtering strategy.

3.3. Optimal LCL Filter Design of Regenerative CHB Drives

To satisfy grid harmonic code IEEE std 519-2014, a suitable filter is required to be designed. As investigated before, the conventional L filter solution cannot meet the requirement when the switching frequency is below 3000 Hz. An alternative filtering solution is the LCL filter. In this section, an optimal passive damping LCL filter is designed for regenerative CHB motor drives. However, with the existence of the phase-shifting transformer in CHB drives, the

existing LCL filter design methods cannot be applied directly. To tackle this problem, a new LCL filter design framework using genetic algorithm (GA) optimization is proposed based on the Simulink model. Unlike the conventional design procedures based on the mathematical model, the CHB Simulink model can take DC voltage constraint, PLL performance, transformer factors, and harmonics profile into consideration while designing the LCL filters. With the proposed filter design framework, the designed LCL filter can guarantee both the harmonic performance and the system performance with minimum passive component size, which cannot be achieved through the existing methods. Finally, the proposed method is validated on a seven-level CHB inverter with simulation.

3.3.1. Proposed Optimal LCL Filter Design for Regenerative CHB Inverter

As shown in Fig. 3.8, an LCL filter is designed and attached between the power inverter and the secondary side of the transformer in each phase. The leakage inductance of the transformer is modeled as L_{leak}. The measured phase voltage and current are denoted as U_{m_x} and I_{sec_x}, where x=(a, b, c). The passive resistor R_f is introduced in the system to avoid the potential resonance problem in the LCL filter.

The current control scheme of the AFE is illustrated in Fig. 3.8. The current control does nothing more than tracking the reference current. The reference currents are controlled in dq axis as I_{d_ref} and I_{q_ref}. The reference current in q axis I_{q_ref} is set to zero to avoid reactive power injection to the grid. The reference current in d axis I_{d_req} is set based on the regeneration power to the grid.

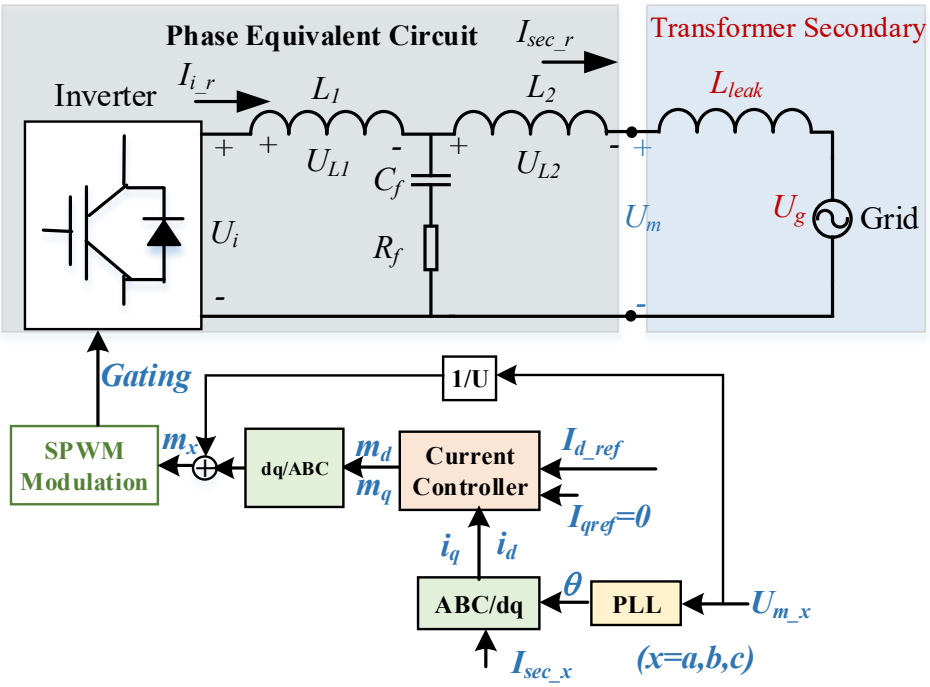


Fig. 3. 8 Phase Equivalent Circuit and Control Scheme

There are many possible combinations for the LCL filter that can satisfy the harmonic requirement. However, one LCL combination with high inductance and less capacitance will impose an inappropriate voltage drop in the designed filter, which forces to increase the DC bus voltage to compensate for the filter voltage drop to provide the rated current [31]. To tackle this issue, some constraints on the LCL filter inductance based on the DC voltage is required to be derived based on rated output currents. Based on Kirchhoff's law, the inverter output current I_{i_r} and the output phase voltage of the inverter U_i can be estimated in equation (3.9) and (3.10) under the rated current situation with the unity power factor.

$$\vec{I}_{i\_r} = \vec{I}_{sec\_r} + \frac{\vec{U}_g + j\omega_b(L_2 + L_{leak})\vec{I}_{sec\_r}}{1/\, j\omega_b C_f + R_f} \tag{3.9}$$

$$\vec{U}_i = \vec{U}_g + j\omega_b(L_2 + L_{leak})\vec{I}_{\text{sec}\_r} + j\omega_b L_1 \vec{I}_{i\_r} \tag{3.10}$$

where I_{sec_r} and I_{i_r} are the rated output current at the inverter side and grid side respectively, U_g is the transformer secondary phase voltage, ω_b is the grid frequency. The SPWM scheme is adopted without third-order harmonic injection, the following inequality for the DC bus voltage should be satisfied if rated power can be delivered:

$$U_{dc\_\max} - 2\sqrt{2}\left|\vec{U}_i\right| \geq 0 \tag{3.11}$$

where the U_{dc_max} is the maximum allowed DC bus voltage of the system, which is usually limited by the power switch's rating. The selection of the passive damping LCL filter should satisfy the DC bus constraints in equation (3.11) to assure that rated power can be delivered through the AFEs.

The selection of the LCL filter and damping resistor influences the system's stability and performance. To take the system stability and performance into consideration, as is shown in Fig. 3.9, the inverter control system with PI current controller in *dq* axis is modeled mathematically in the frequency domain. In the low-frequency region, the LCL filter behaves approximately as an equivalent L-filter neglecting the capacitor branch [114]. The optimal PI parameter of the

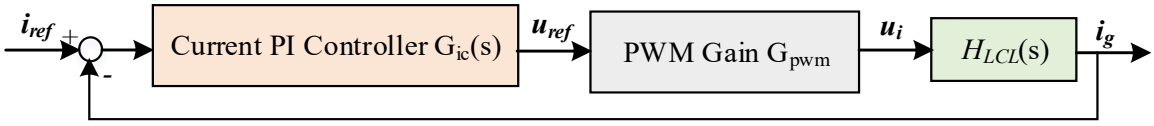


Fig. 3. 9 Current Control Transfer Function on *dq* axis

current controller can be designed through reference [36] [115] if the filter parameters are determined. The designed PI controller G_{ic} is:

$$G_{ic}(s) = k_p + \frac{k_i}{s} \tag{3.12}$$

With the following proportional gain and integration time:

$$k_p = \frac{(L_1 + L_2 + L_{leak}) f_{sw}}{3} \tag{3.13}$$

$$k_i = \frac{(L_1 + L_2 + L_{leak})}{(R_1 + R_2 + R_{leak})} \tag{3.14}$$

where f_{sw} is the switching frequency and R_1, R_2, R_{leak} is the resistance on the inductors L_1, L_2, L_{leak} respectively.

The transfer function is $H_{LCL}=i_g/u_i$ can be calculated with an ideal voltage source assumption capable of dumping all the harmonics. The transfer function H_{LCL} of LCL filter with damping resistor is

$$H_{LCL}(s) = \frac{i_g}{u_i} = \frac{1}{s^2 + \omega_n^2 C_f R_f s + \omega_n^2} * \frac{C_f R_f s + 1}{L_1 (L_2 + L_{leak}) C_f s} \tag{3.15}$$

where

$$\omega_n = \sqrt{\frac{L_1 + (L_2 + L_{leak})}{C_f (L_1 * (L_2 + L_{leak}))}} \tag{3.16}$$

According to Fig. 3.9, the system open-loop transfer function in the frequency domain is shown in equation (3.17).

$$G_{op} = G_{ic}(s) H_{LCL}(s) G_{pwm}(s) \tag{3.17}$$

where $G_{pwm}(s) = \frac{U_{dc}}{2}$. To assure the system stability and dynamic performance, the phase margin (PM) and gain margin constraints (GM) of the open-loop transfer function G_{op} should be estimated in the filter design process. Reasonable constraints of the PM and GM of the open-loop transfer function G_{op} are shown in equation (3.18) [116].

$$PM(G_{op}(s)) > 45^{o}$$
$$GM(G_{op}(s)) > 3dB \tag{3.18}$$

A smaller damping resistor usually with better filter performance, however, may not enough to damp the system at the resonance frequency. The choice of the damping resistor is weighing between system stability at the resonance frequency and filter performance at high frequency. The passive damping resistor is at least one-third of the impedance of the filter capacitor C_f at the resonance frequency [26]. A reasonable searching domain of the damping resistor R_f constraint is shown in equation (3.19).

$$\frac{2}{\omega_n * C_f} \geq R_f \geq \frac{1}{3\omega_n * C_f} \tag{3.19}$$

The design procedure of the LCL filter with GA optimization is demonstrated in Fig. 3.10. First of all, the searching domain of the design filter is defined according to the system specification based on allowed dc-link voltage, switching frequency, rated voltage, and current. Second, different nonlinear constraints such as the DC bus voltage constraint, system performance phase margin and gain margin constraints, and damping resistor constraints are considered to further narrow down the searching domain. Third, the Simulink model comprised of a seven-level CHB inverter, and a phase-shifting transformer is called by the GA. The synchronization with the grid voltage is obtained by means of moving average filter based PLL

[117]. The simulation result at the PCC point is examined according to the IEEE std 519-2014 standards. GA will automate find out the minimum objective value in the entire narrowed down available searching domain in a "biology" way.

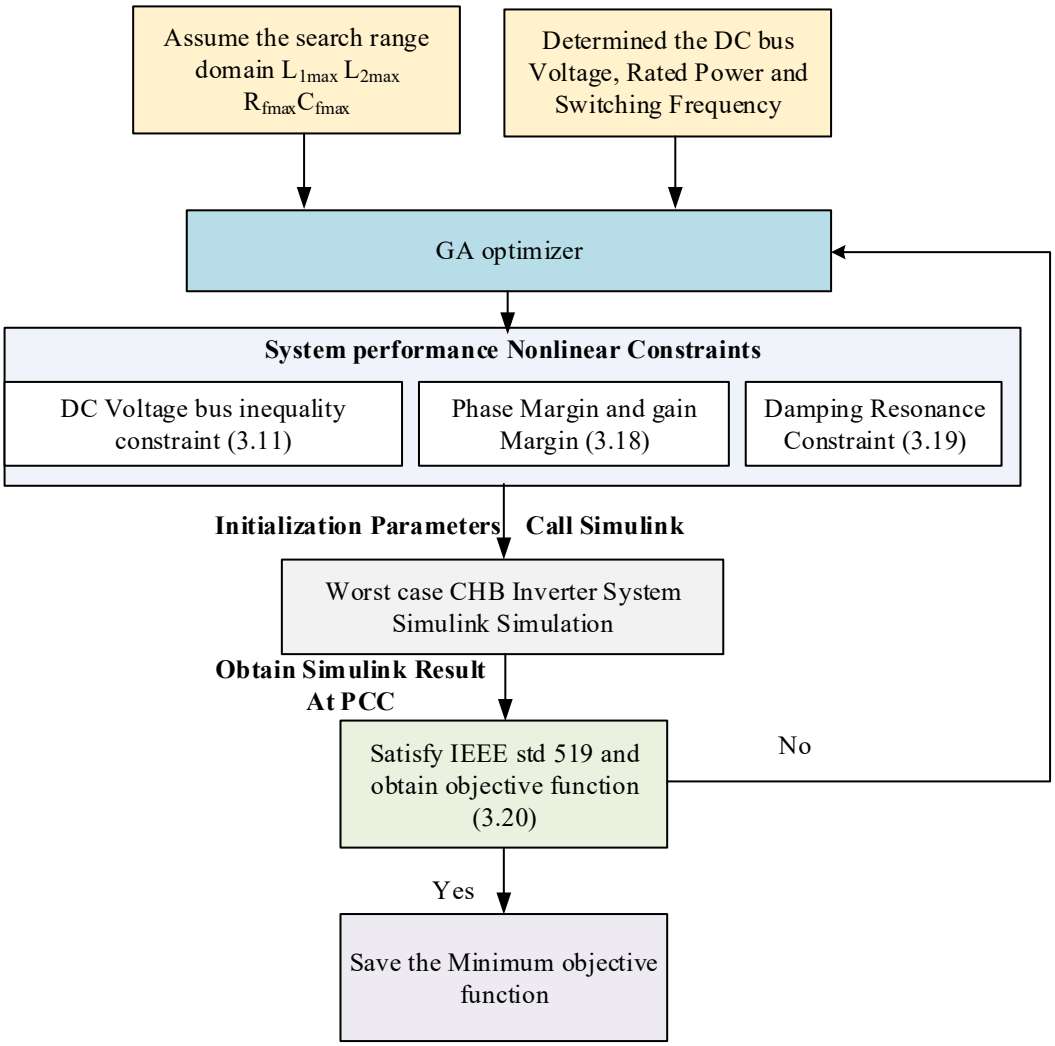


Fig. 3. 10 Proposed Design Procedure of the LCL filter with GA

The objective function for the GA optimization is shown in equation (3.20).

$$obj = \begin{cases} \frac{1}{2}L_1 I^2 + \frac{1}{2}L_2 I^2 + K\frac{1}{2}C_f U^2 & if\ satisfy\ IEEE\ standard \\ infinity & if\ not\ satisfy\ IEEE\ standard \end{cases} \quad (3.20)$$

When the current in the PCC point satisfies the IEEE standard, the objective value equals the stored energy in the inductors and capacitor. Otherwise, the objective value is infinity to abandon the candidate. The parameter K is introduced to add weight between inductance and capacitance. The GA automated searches the minimum objective value among all possible combinations for inductors and capacitors in the available searching domain.

To further accelerate the optimization process, the chosen of inductor, capacitor and resistor are integer numbers discretized with 0.1 mH, 0.1μF and 0.1ohm step. It is meaningless to go with further accuracy from the engineering perspective. This function can be easily achieved with an integer programming GA toolbox in MATLAB. Moreover, the proposed optimization framework is well-suited for the use of parallel computation with multiple computing cores in MATLAB. This is effective to reduce the computation time.

3.3.2. Simulation Result and Discussion

This section highlights the effectiveness of the proposed LCL filter design optimization framework based on a seven-level regenerative CHB multilevel inverter. To compare with the conventional LCL filter design process, an LCL filter is designed from the existing method [26] for the same seven-level regenerative CHB drives at the 1980 Hz frequency. The designed passive damping LCL filters are summarized in Table 3.8 under different design strategies.

As is shown in Table 3.8, the designed filter through [26] violates the DC bus limit and a power constraint. The rated current cannot be regenerated to the grid by each power cell due to the oversize of the designed inductor and lack of enough DC voltage. This is easy to understand since the DC bus voltage constraint is not taken into consideration in the LCL design process.

Table 3. 8 LCL Filter Design for a seven-level regenerative CHB Drive for 1980 Hz

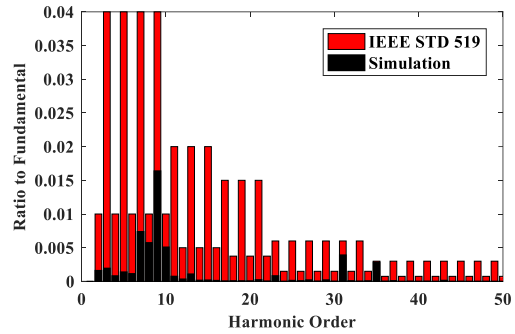
LCL Type	L_1(mH)	L_2(mH)	C_f(μF)	R_f(Ω)	TDD_pri	TDD_sec	Standard Satisfied
LCL [26]	9.5	1.6	24.4	2.5	-	-	NO, the DC bus constraints cannot be met
LCL (Case 1)	2.2	0.8	79	1.6	3.5%	7.4%	Yes
LCL (Case 2)	2.1	2.1	38.8	1.8	1.3%	2.2%	Yes

Unlike the conventional filter design strategy based on the mathematic model, the proposed optimization framework directly uses the Simulink model for the LCL filter design. Different constraints including the DC bus voltage constraint can be considered in the filter design process, which cannot be achieved with the conventional filter design process.

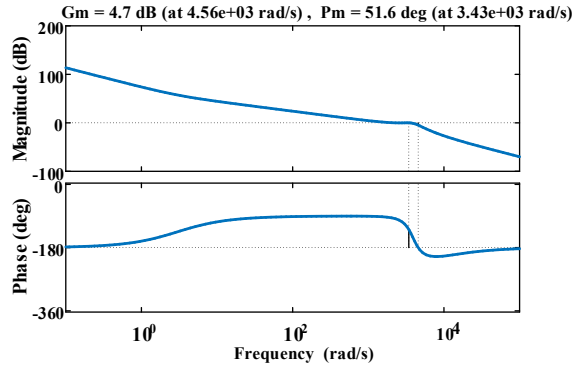
Two LCL filter candidates are optimized through the proposed optimization framework with different K parameters in the objective function shown in equation (3.20). Case 1 LCL filter is optimized with K=1 in the objective function which results in a large capacitance. The designed L_1, L_2, R_f and C_f are 2.2mH, 0.8mH, 79 μF and 1.6 Ω respectively. From the Simulink simulation result, the TDD at the primary and secondary side of the transformer are 3.5% and 7.5% respectively. The simulation waveforms with designed filters are shown in Fig. 3.11.

As is shown in Fig 3.11 (a), the designed Case1 LCL filter can satisfy the stringent IEEE std 519-2014 for each order harmonics. Meanwhile, the phase margin is 51.6 degrees at 3430 rad/s. The gain margin is 4.7 dB at 4560 rad/s. The LCL filter resonance frequency is around 545Hz. The system dynamic performance is guaranteed according to Fig. 3.11 (b) with the designed filter. The current and voltage waveforms at the PCC point is shown in Fig. 3.11 (c). Rated power can be delivered by the AFE with the designed LCL filter operating at 1100V dc-

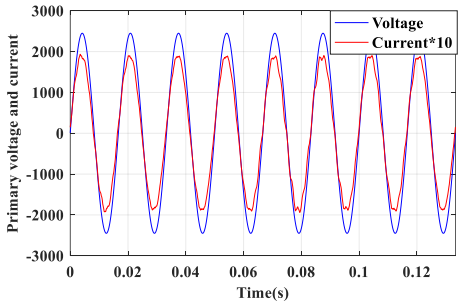
link voltage. The DC voltage limitation, current harmonic profile constraints, and the system dynamic constraints are all satisfied by adopting the proposed LCL filter design strategy.



(a) Harmonic Profile vs STD 519

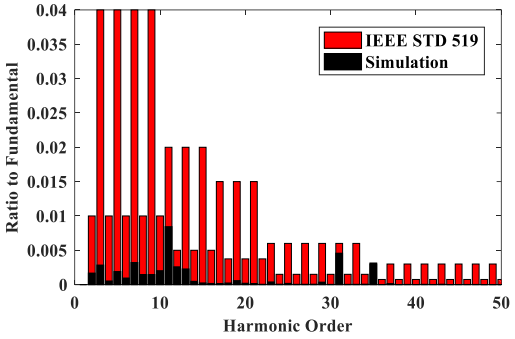


(b) Open Loop Bode figure

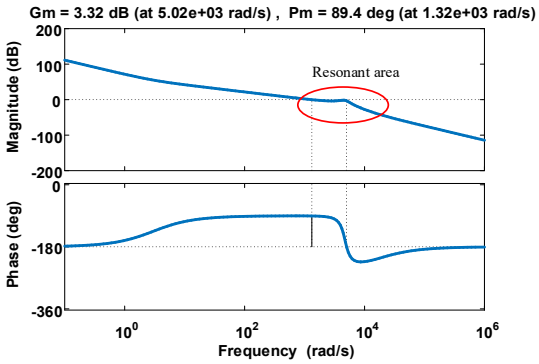


(c) Current at PCC

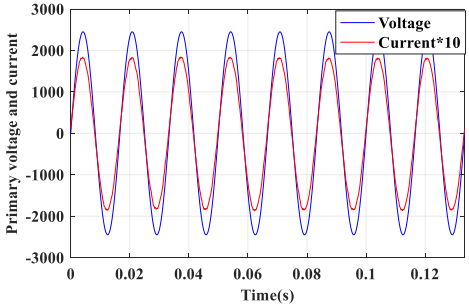
Fig. 3. 11 Case 1 LCL Filter Designed with K=1



(a) Harmonic Profile vs STD 519



(b) Open Loop Bode figure



(c) Current at PCC

Fig. 3. 12 Case 2 LCL Filter Designed with K=8

Case 2 filter candidate is designed with K=8 to add more weight to reduce the capacitor size. The designed L_1, L_2, R_f and C_f are 2.1mH, 2.1mH, 38.8 uF and 1.8 Ω respectively. From the

Simulink simulation result, the TDD at the primary and secondary sides of the transformer are 1.3% and 2.2% respectively. The simulation waveforms with a designed filter are shown in Fig.3.12. The designed case2 LCL filter can satisfy the stringent IEEE std 519-2014 for each order harmonics. Meanwhile, the phase margin is 89.4 degrees at 1320 rad/s. The gain margin is 3.32 dB at 5020 rad/s. The current and voltage waveforms at the PCC point is shown in Fig. 3.12 (c). Rated power can be delivered by the AFE with the designed LCL filter operating at 1100V dc-link voltage.

To design an optimal LCL filter for a regenerative CHB inverter, beyond the harmonic performance and filter size, it is necessary to take system performance (such as grid impedance, PLL performance, controller saturation) into consideration due to the existence of the transformer. To consider all these factors while minimizing the LCL filter, an optimization framework is proposed directly based on the Simulink nonlinear model instead of the tedious mathematical model. Simulation validates the performance of the designed LCL filter using a seven-level regenerative CHB motor drive.

The designed LCL can meet the IEEE std 519-2014 filtering harmonics requirements operating with 1980 Hz switching frequency and 1100 V DC voltage, which cannot be achieved with the conventional L filter strategy. However, considering the number of power cells in a CHB drive, a large number of passive components are required for the system, which increases the overall cost and size of the CHB regenerative drive system. Although, with a good filtering performance, these LCL filters are not best suitable for the regenerative CHB drives in terms of cost, weight, and heat issue.

To achieve a better filtering performance, a higher-order filter can be designed for the AFEs to satisfy the IEEE std 519-2014. This would further increase the number of passive filtering components, which is not a desirable strategy for the regenerative CHB system. In the following section, the new filter design strategies are proposed with a simplified filter structure and minimum filter size.

3.4. Proposed Active Filter Design (Method 1)

As discussed earlier, when the L filters or LCL filters are designed for the regenerative CHB drive system, the low order baseband harmonics are mitigated with the phase-shifting transformer, however, switching sideband harmonics are difficult to filter out using the traditional passive filters to satisfy the IEEE std 519-2014. This may result in filter oversize for the regenerative CHB drive system. To solved this problem, a new active filtering strategy (named Method 1) is proposed for the regenerative CHB drive.

In Method 1, to filter out the switching sideband harmonics, when the switching frequency is 1980Hz (=33×60), the carrier-shift active filtering technique is applied to mitigate the 31^{st} order harmonics. Meanwhile, the 35^{th} order harmonic component is mitigated with an extra trap filter on the primary side of the transformer. The proposed filter structure is shown in Fig. 3.13.

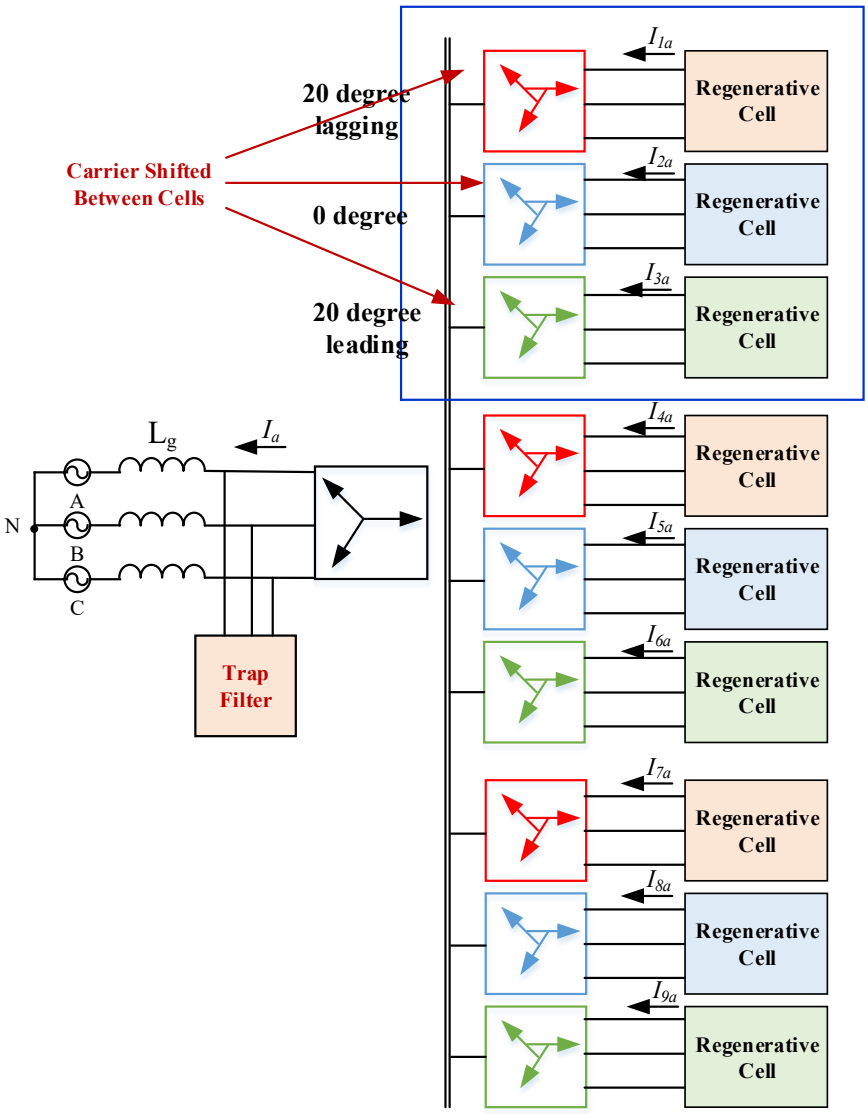


Fig. 3. 13 Proposed Filter Structure (Method 1)

3.4.1. Carrier Shifted Control Scheme to Eliminate 31st Order Harmonics

Consider three regenerative cells in phase A, as shown in Fig. 3.13, the 31st order harmonic components in I_{1a}, I_{2a} and I_{3a} are coming from the SPWM modulation process. The output voltage U_{1a}, U_{2a}, and U_{3a} contain the 31st order harmonic, which leads to current harmonics on the secondary side of the transformer.

During the natural sampled SPWM scheme, the harmonics of the voltage PWM waveform can be calculated through the equations (3.21)-(3.23). The sideband voltage harmonics are related to the carrier phase angle θ_{xc} (x=1, 2, 3 for different cells) and modulation waveform.

$$v_{1a} = \frac{MV_{dc}}{2}\cos(\omega_o t - 20) + \frac{2V_{dc}}{\pi} J_{-2}(\frac{\pi}{2}M)\cos(31\omega_o t + \theta_{1c} + 40) \tag{3.21}$$

$$v_{2a} = \frac{MV_{dc}}{2}\cos(\omega_o t) + \frac{2V_{dc}}{\pi} J_{-2}(\frac{\pi}{2}M)\cos(31\omega_o t + \theta_{2c}) \tag{3.22}$$

$$v_{3a} = \frac{MV_{dc}}{2}\cos(\omega_o t + 20) + \frac{2V_{dc}}{\pi} J_{-2}(\frac{\pi}{2}M)\cos(31\omega_o t + \theta_{3c} - 40) \tag{3.23}$$

where M is the modulation index, V_{dc} is the DC voltage, J denotes the Bessel function. With an arbitrary designed L_1 filter, the phase angle between the voltage and current waveform at the fundamental frequency and 31st order harmonics can be illustrated in Fig.3.14.

(a) Fundamental component (b) 31st order harmonic

Fig. 3. 14 Phase Angle Relation between Voltage and Current

The corresponding current on the secondary of the transformer is calculated as:

$$I_{1a} = I_1\cos(\omega_o t - 20 - \alpha) + I_{31}\cos(31\omega_o t + \theta_{1c} + 40 - \beta) \tag{3.24}$$

$$I_{2a} = I_1\cos(\omega_o t - \alpha) + I_{31}\cos(31\omega_o t + \theta_{2c} - \beta) \tag{3.25}$$

$$I_{3a} = I_1\cos(\omega_o t + 20 - \alpha) + I_{31}\cos(31\omega_o t + \theta_{3c} - 40 - \beta) \tag{3.26}$$

Due to the phase-shifting transformer, the current on the secondary side can be reflected to the primary side of the phase-shifting transformer with 20-degree phase shifting. The total reflected current on the primary side of the transformer I_A is calculated as:

$$I_A = 3I_{1A}\cos(\omega_o t - \alpha) + I_{31A}(\cos(31\omega_o t + \theta_{1c} + 60 - \beta) + \cos(31\omega_o t + \theta_{2c} - \beta) + \cos(31\omega_o t + \theta_{3c} - 60 - \beta)) \tag{3.27}$$

Therefore, the 31st order harmonic of the primary side of the phase-shifting transformer will be canceled out if and only if :

$$\cos(31\omega_o t + \theta_{1c} + 60 - \beta) + \cos(31\omega_o t + \theta_{2c} - \beta) + \cos(31\omega_o t + \theta_{3c} - 60 - \beta) = 0 \tag{3.28}$$

To eliminate the switching sideband harmonics at 31st order, the following angles will be used to shift the angles of the carriers between the three cells in the same phase:

$$\begin{aligned} \theta_{1c} &= 60^\circ \\ \theta_{2c} &= 0^\circ \\ \theta_{3c} &= -60^\circ \end{aligned} \tag{3.29}$$

3.4.2. Trap Filter Design for 35th Order Harmonics

Once the 31th order harmonic is eliminated by the proposed active filtering strategy, the trap filter is then further designed to remove the 35th order harmonics coming from the SPWM modulation. The typical trap filter for 35th order harmonic is illustrated in Fig. 3.15. The inductor and capacitor will be designed at the resonant frequency of 35th order harmonic (2100 Hz), which provides a low impedance current flow for the 35th order harmonic. In this way, the 35th order harmonics could be mitigated with the minimum passive components and will not show up at the PCC point.

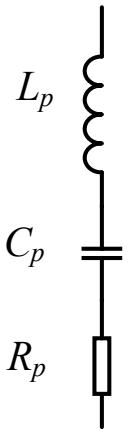


Fig. 3. 15 Trap Filter for 35th order Harmonic (single-phase diagram)

The equivalent impedance for the trap filter is calculated in equation (3.30),

$$Z_{eq} = j\omega L_p + 1/(j\omega C_p) + R_p \tag{3.30}$$

The trap filter parameters designed for 35th harmonic are shown in Table 3.9. The bode diagram for the equivalent impedance is shown in Fig. 3.16. The equivalent impedance is 0.64 Ω at the 35th harmonics. The grid impedance L_g is 0.68mH for the simulation.

Table 3. 9 Trap Filter for 1980 Hz under 1100V DC Voltage

Frequency	L_p(mH)	C_p(uF)	R_p(Ω)
1980	0.97	5.8	0.64

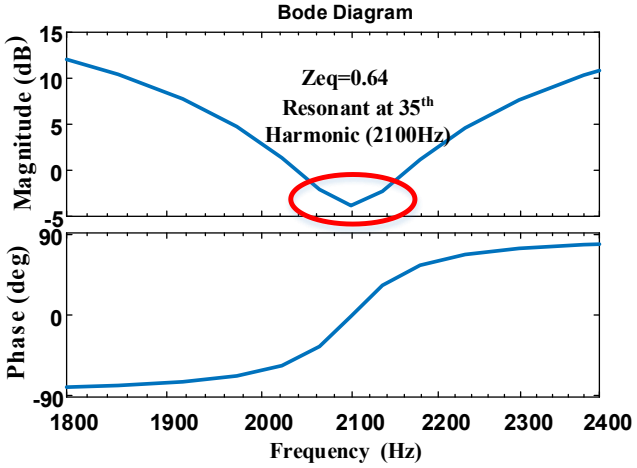


Fig. 3. 16 Impedance Bode Figure for Trap Filter

3.4.3. Simulation Result for the Proposed Filter (Method 1)

To satisfy the IEEE standard 519-2014, the carrier phase-shifting strategy and the trap filter are proposed in Method 1 to reduce the minimum required filter of the regenerative CHB drive system. The minimum required L_1 between the transformer secondary and the AFE is reduced to 2 mH (5.87% p.u.) with proposed method 1. The harmonic content at the PCC point with a minimum L_1 filter (2 mH) is shown in Fig. 3.17. The 31th and 35th order harmonics are suppressed below the limits given in the IEEE std 519-2014 standard.

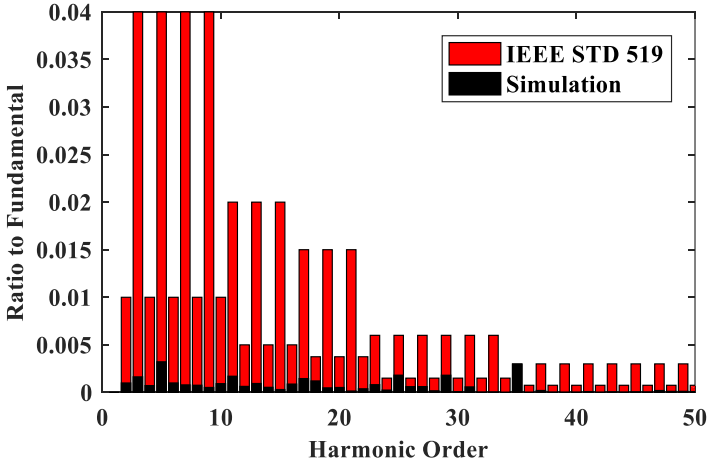
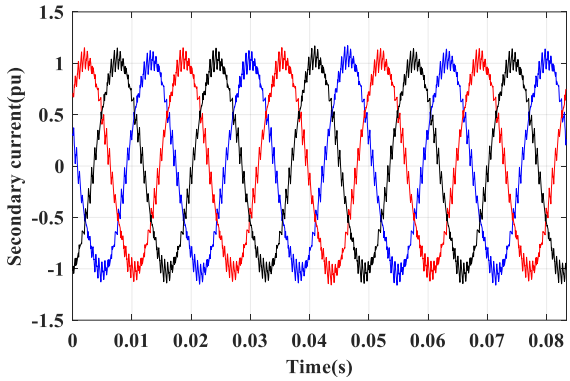


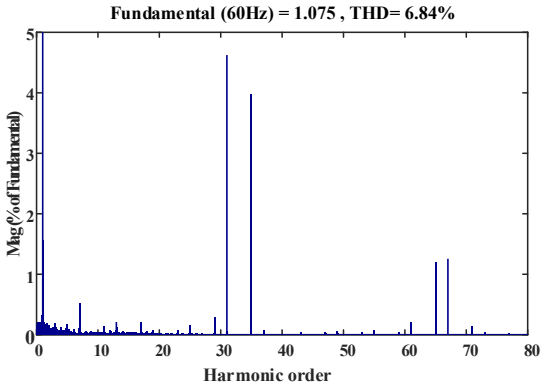
Fig. 3. 17 Current Harmonic Content at PCC (Method 1)

With the designed filter, the current and voltage waveforms are shown in Fig. 3.18. Comparing Fig. 3.18 (b) with (d), the 31st order harmonic component ratio reduces from 4.64% to 0.08% with the carrier phase angle shifting strategy. Comparing Fig.33 (b) with 33(f), the 35th order harmonic component ratio reduces from 3.85% to 0.30% with the help of the designed trap filter. What's more, with the proposed phase-shifting angles, as shown in Fig. 33(d), the second group sideband harmonics (65th and 67th order harmonics) are also eliminated at the transformer primary side. This could benefit the harmonic profile at the PCC point.

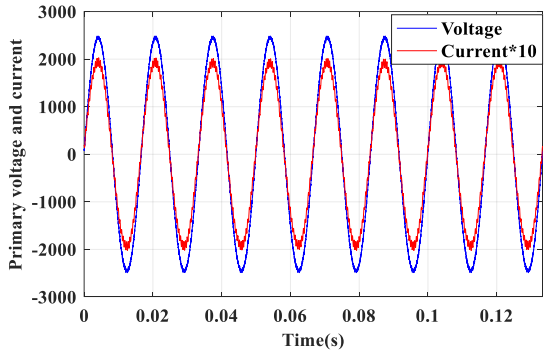
Although the filter designed through the proposed filter design method 1 can satisfy the IEEE standard 519-2014 with a small L_1 inductance (5.87% pu). However, the required trap filter on the primary side transformer is costly and bulky due to the high voltage, which is not desirable.



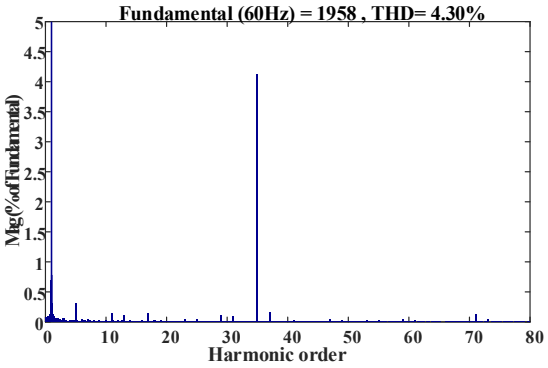
(a)Secondary side current



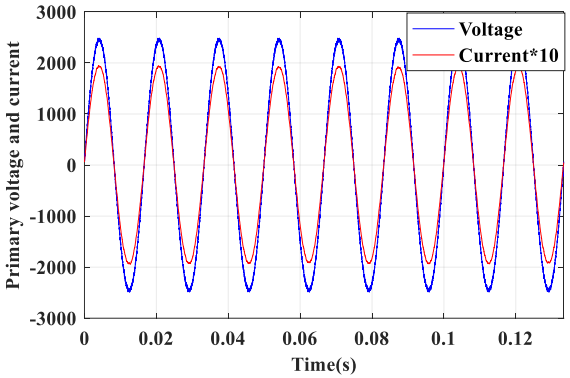
(b)Secondary side current TDD



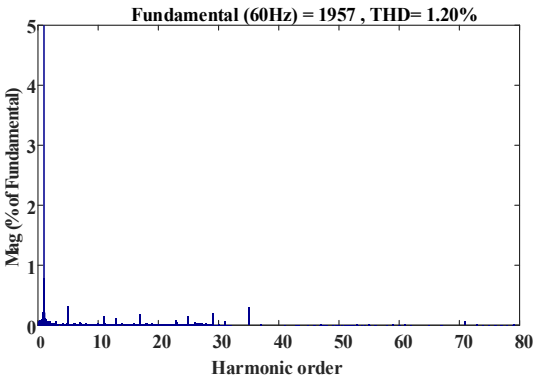
(c)Primary side current and voltage waveform



(d)Primary side current TDD



(e)PCC point current and voltage waveform



(f)PCC point TDD

Fig. 3. 18 Current and Voltage Waveforms for Filter Design (Method 1)

3.5. Proposed Active Filter Design (Method 2)

As illustrated previously, in the proposed Method 1 strategy, a trap filter is required at the transformer primary side to remove the 35th order harmonics which can be costly and bulky since it has to be located at the medium voltage side. To avoid this problem, another carrier phase-shifted strategy called Method 2 is proposed for the regenerative CHB drive system. In the proposed Method 2, the carrier angles are shifted among the cells in different phases to eliminate both the 31st and 35th order harmonics simultaneously. In this way, compared with Method 1, the bulky and costly trap filter can be removed. Only a small inductor L_1 is required to be added between the transformer secondary side and the AFE.

The proposed filter design method 2 is illustrated in Fig. 3.19.

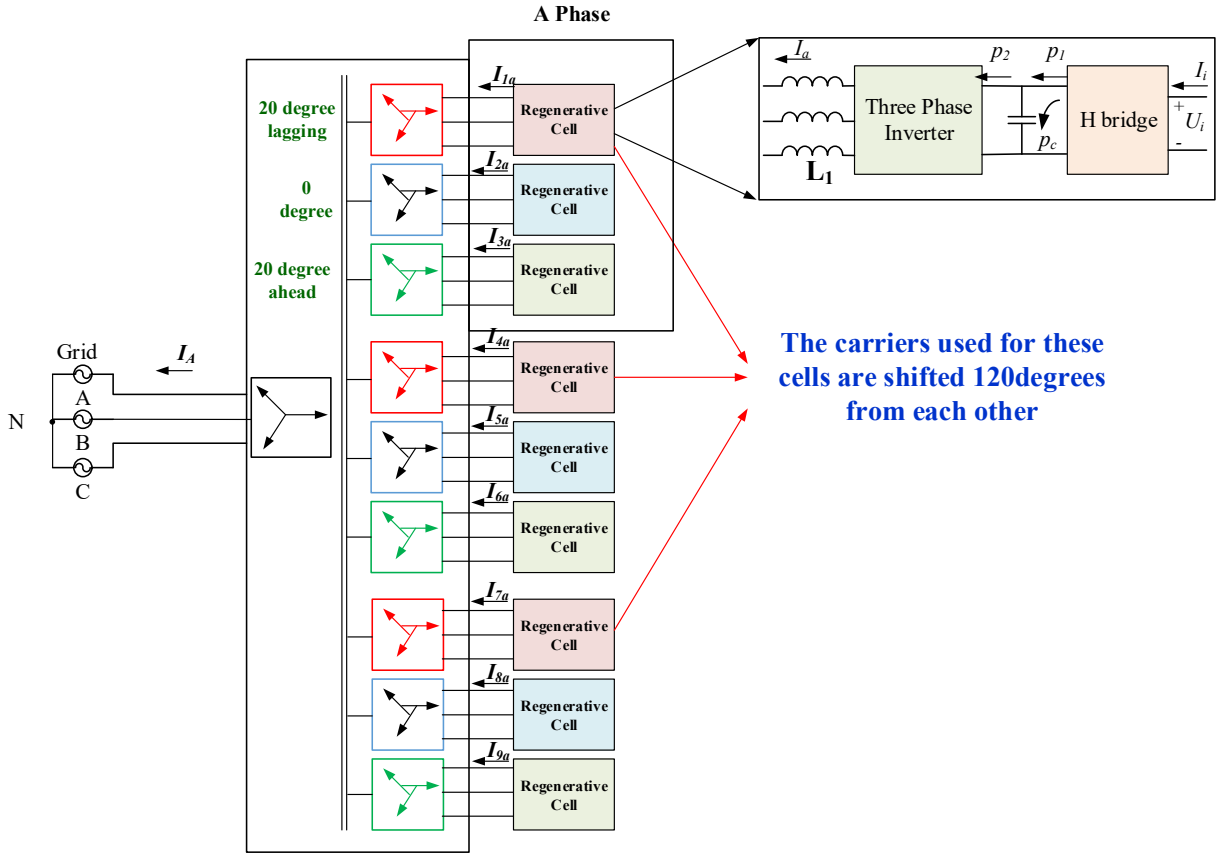


Fig. 3. 19 Filter Design System Structure (Method 2)

According to the natural sampled SPWM scheme, the harmonics of the voltage PWM waveform can be calculated. This is related to the carrier phase angles and modulation waveform phase angle as described in equations (3.31)-(3.33).

$$v_{1a} = \frac{MV_{dc}}{2}\cos(\omega_o t - 20) + \frac{2V_{dc}}{\pi}J_{-2}(\frac{\pi}{2}M)\cos(31\omega_o t + \theta_{1c} + 40) + \frac{2V_{dc}}{\pi}J_2(\frac{\pi}{2}M)\cos(35\omega_o t + \theta_{1c} - 40) \quad (3.31)$$

$$v_{4a} = \frac{MV_{dc}}{2}\cos(\omega_o t - 20) + \frac{2V_{dc}}{\pi}J_{-2}(\frac{\pi}{2}M)\cos(31\omega_o t + \theta_{4c} + 40) + \frac{2V_{dc}}{\pi}J_2(\frac{\pi}{2}M)\cos(35\omega_o t + \theta_{4c} - 40) \quad (3.32)$$

$$v_{7a} = \frac{MV_{dc}}{2}\cos(\omega_o t - 20) + \frac{2V_{dc}}{\pi}J_{-2}(\frac{\pi}{2}M)\cos(31\omega_o t + \theta_{7c} + 40) + \frac{2V_{dc}}{\pi}J_2(\frac{\pi}{2}M)\cos(35\omega_o t + \theta_{7c} - 40) \quad (3.33)$$

The 31st and 35th order harmonic of the primary side of the phase-shifting transformer will be canceled out if the following angels are chosen for the phase angles of the carriers.

$$\begin{aligned} \theta_{1c} &= 0^\circ \\ \theta_{4c} &= 120^\circ \\ \theta_{7c} &= 240^\circ \end{aligned} \quad (3.34)$$

To satisfy the IEEE standard 519-2014, by adopting the proposed Method 2, the minimum required L_1 between the transformer secondary and the inverter is 0.5mH (1.47% p.u.). Fig. 3.20 shows the harmonic content at PCC in the simulation where the minimum filter is employed. As can be seen, both the 31st and 35th order harmonics are suppressed under the limits given in the IEEE std 519-2014 standard with the proposed control technique.

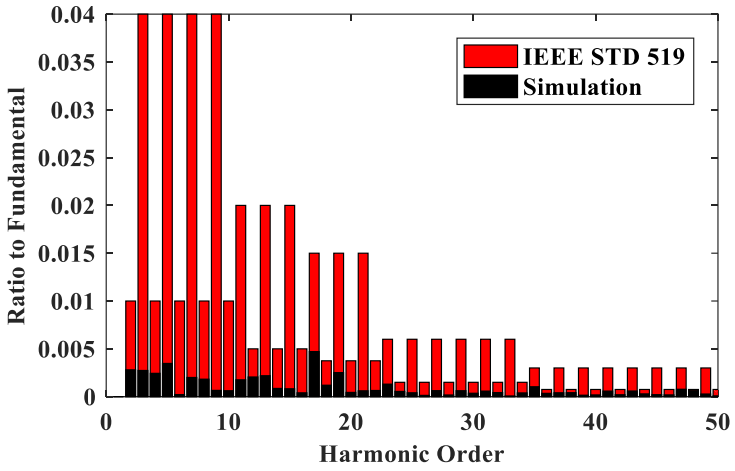
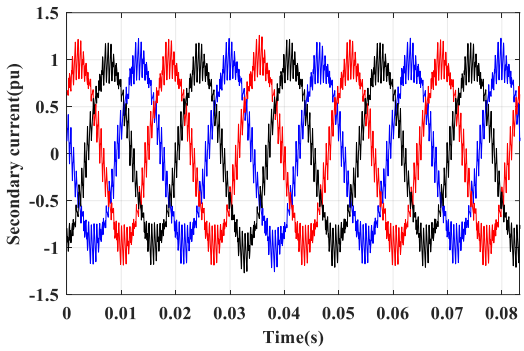
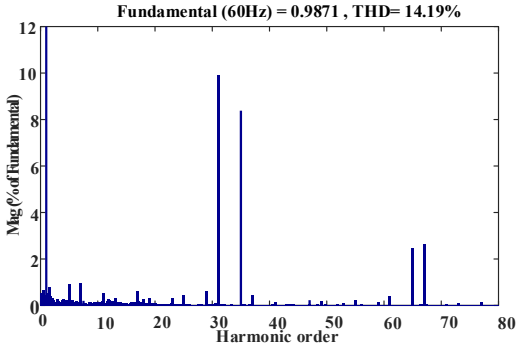


Fig. 3. 20 Current Harmonic Content at PCC (Method 2)

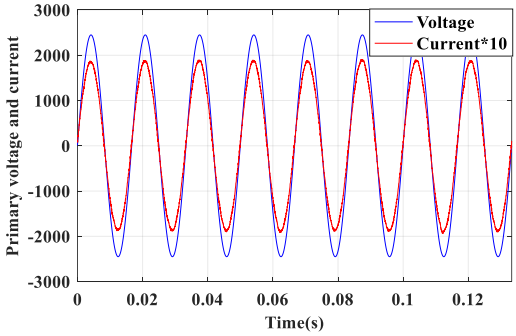
With the designed minimum filter (0.5mH), the current and voltage waveforms are shown in Fig. 3.21. The secondary side current TDD directly from the AFE is 14.19% due to a large amount of 31^{th} and 35^{th} order harmonic components, which can be validated from the current waveform in Fig. 3.21 (a) and (b). These current harmonics are coming from the modulation process. However, when the proposed carrier shifting angles are used, both the 31^{st} and 35^{th} order harmonics are mitigated. The TDD at the transformer primary side is only 1.86% with the proposed method 2. In rated power conditions, the unit power factor could be achieved as is shown in Fig 3.21 (c). Beyond that, the second group sideband harmonics (65^{th} and 67^{th} order harmonics) are also eliminated in the transformer primary side current. This could benefit the harmonic profile at the PCC point.



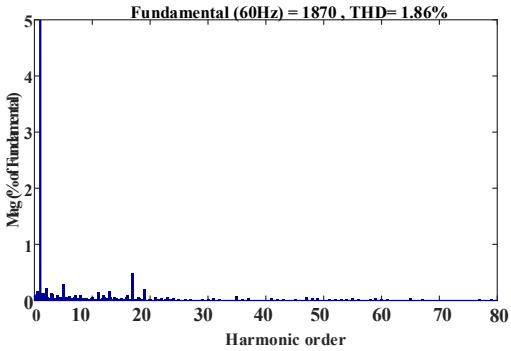
(a) Secondary side current



(b) Secondary side current TDD



(c) Primary side current and voltage waveform



(d) Primary side current TDD

Fig. 3. 21 Current and Voltage Waveforms for Filter Design (Method 2)

3.6. Proposed Active Filter Design (Method 3)

As is illustrated, two carrier-shifted methods for filter designing are introduced for the regenerative CHB drive system. The proposed Method 1 adopts the carrier shifted method and meanwhile requires an extra trap filter on the transformer primary side to satisfy the IEEE standard. The proposed Method 2 further removes the extra trap filter by adopting the new carrier shifting angles. Only a small L_1 filter 0.5mH (1.47% p.u.) is required for each power cell to satisfy the same IEEE standard.

In this section, an optimal filter design strategy for the regenerative CHB drive is introduced (named Method 3). Only a smaller L_1 filter is required between the transformer and the power cell. Moreover, a new phase-shifting method is proposed to eliminate all the harmonic sideband below 100th order harmonics at the PCC point. Compared with Method 2, the proposed method 3 further improves the harmonic profile at the PCC point.

The proposed Method 2 and its design strategy for the regenerative CHB drive system is illustrated in the last section. With the same designed parameter illustrated, the simulation is repeated with the current harmonic content extended to 100th order of the grid frequency at the PCC point. From Fig. 3.22, the switching sideband harmonics around 99th order frequency will appear at the primary side of the phase-shifting transformer. Although, Method 2 can satisfy the IEEE std 519 2014 standard with a smaller L filter. However, Method 2 also gives rise to the extra switching harmonics around 99 order which is not desired.

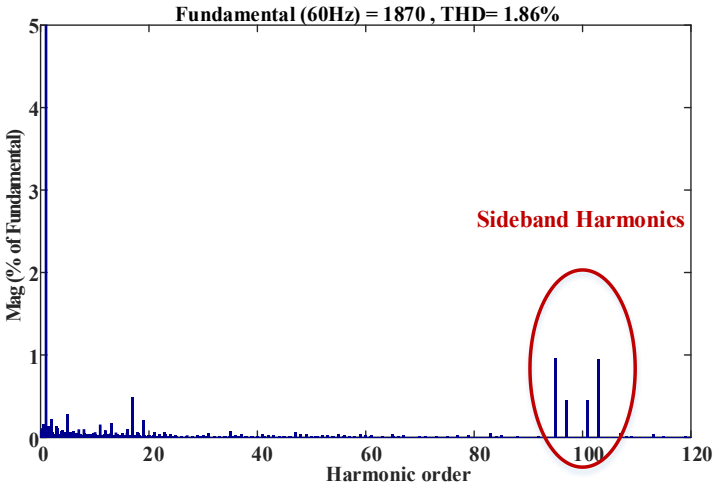


Fig. 3. 22 Current Harmonic Profile at the PCC with the Proposed Method 2

To avoid this problem, Method 3 is proposed by adopting the new phase-shifting angles. As is shown in Fig. 3.23, the carrier phase angle within the same phase and between different

phases are all interleaved. Through this configuration, compared with method 2, a similar harmonic profile can be obtained below 50th order harmonics to satisfy the IEEE std 519-2014. Moreover, the switching sideband harmonics at 99th frequency can be further eliminated as a result. This can further improve the harmonic profile at the PCC point.

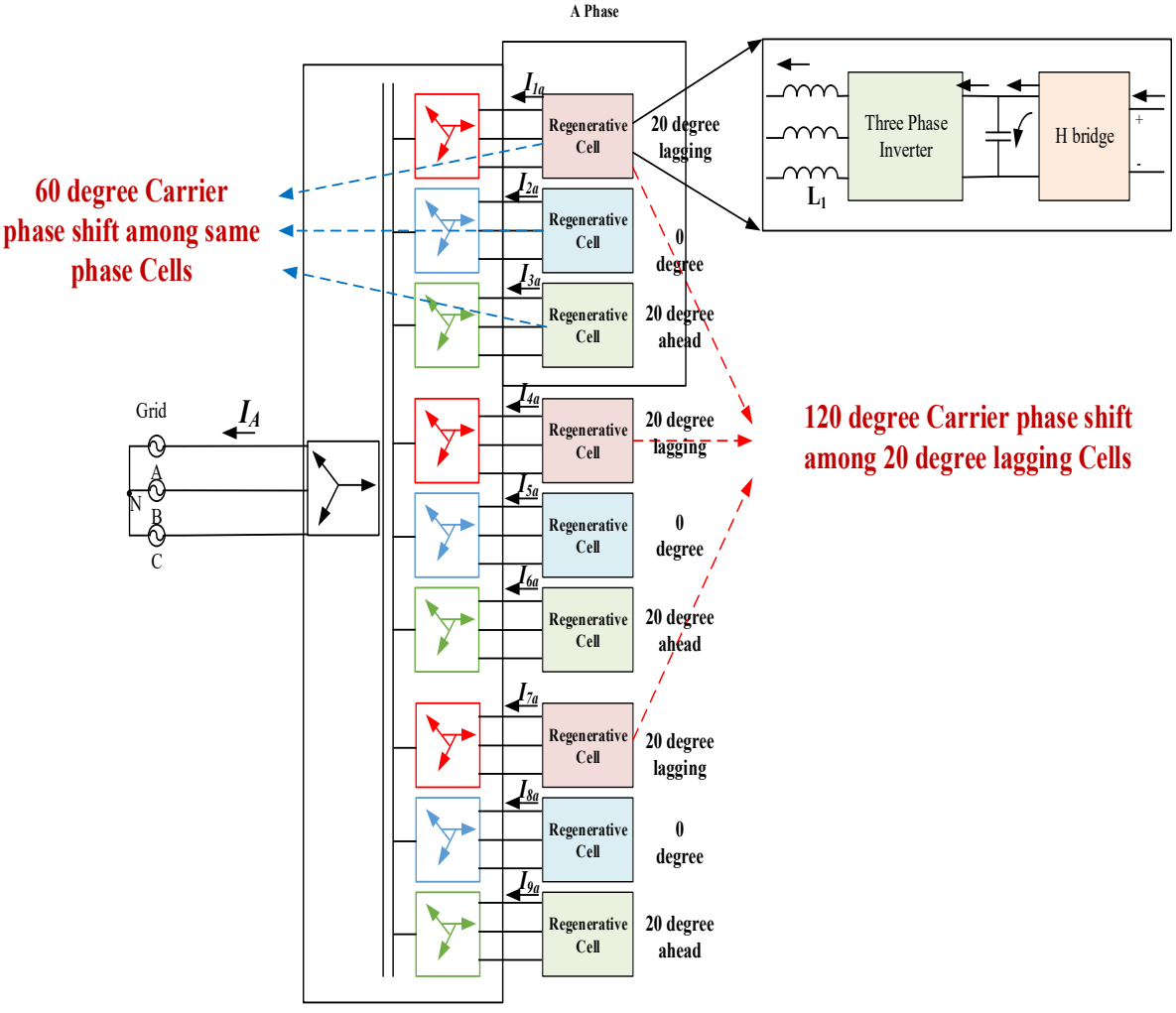


Fig. 3. 23 Proposed Filter Structure (Method 3)

Considering the natural sampled SPWM scheme, the harmonics of the voltage PWM waveform is calculated in equation (3.35)-(3.38). A similar analysis procedure can be employed.

$$v_{1a} = \frac{MV_{dc}}{2}\cos(\omega_o t - 20) + \frac{2V_{dc}}{\pi}J_{-2}(\frac{3\pi}{2}M)\cos(97\omega_o t + 3\theta_{1c} + 40) + \frac{2V_{dc}}{\pi}J_2(\frac{3\pi}{2}M)\cos(101\omega_o t + 3\theta_{1c} - 40) \quad (3.35)$$

$$v_{2a} = \frac{MV_{dc}}{2}\cos(\omega_o t) + \frac{2V_{dc}}{\pi}J_{-2}(\frac{3\pi}{2}M)\cos(97\omega_o t + 3\theta_{2c}) + \frac{2V_{dc}}{\pi}J_2(\frac{3\pi}{2}M)\cos(101\omega_o t + 3\theta_{2c}) \quad (3.36)$$

$$v_{3a} = \frac{MV_{dc}}{2}\cos(\omega_o t + 20) + \frac{2V_{dc}}{\pi}J_{-2}(\frac{3\pi}{2}M)\cos(97\omega_o t + 3\theta_{3c} - 40) + \frac{2V_{dc}}{\pi}J_2(\frac{3\pi}{2}M)\cos(101\omega_o t + 3\theta_{3c} + 40) \quad (3.37)$$

The corresponding current on the secondary of the transformer is calculated as:

$$I_{1a} = I_1\cos(\omega_o t - 20 - \alpha) + I_{97}\cos(97\omega_o t + 3\theta_{1c} + 40 - \beta_1) + I_{101}\cos(101\omega_o t + 3\theta_{1c} - 40 - \beta_2) \quad (3.38)$$

$$I_{2a} = I_1\cos(\omega_o t - \alpha) + I_{97}\cos(97\omega_o t + 3\theta_{2c} - \beta_1) + I_{101}\cos(101\omega_o t + 3\theta_{2c} - \beta_2) \quad (3.39)$$

$$I_{3a} = I_1\cos(\omega_o t + 20 - \alpha) + I_{97}\cos(97\omega_o t + 3\theta_{3c} - 40 - \beta_1) + I_{101}\cos(101\omega_o t + 3\theta_{3c} + 40 - \beta_2) \quad (3.40)$$

Due to the phase-shifting transformer, the current on the secondary side can be reflected to the primary side of the phase-shifting transformer with 20-degree phase shifting. The total reflected current at 97th and 101th order harmonics on the primary side of the transformer I_A is calculated as

$$\begin{aligned} I_A = {} & 3I_{1A}\cos(\omega_o t - \alpha) + I_{97A}(\cos(97\omega_o t + 3\theta_{1c} + 60 - \beta) + \cos(97\omega_o t + 3\theta_{2c} - \beta) + \cos(97\omega_o t + 3\theta_{3c} - 60 - \beta)) \\ & + I_{101A}(\cos(101\omega_o t + 3\theta_{1c} - 60 - \beta) + \cos(101\omega_o t + 3\theta_{2c} - \beta) + \cos(101\omega_o t + 3\theta_{3c} + 60 - \beta)) \end{aligned} \quad (3.41)$$

For later simulation, one solution pair is used. To eliminate the switching sideband harmonics at 97th and 101th order frequency, the following angles will be used to shift the angles of the carriers.

$$\begin{aligned}\theta_{1c} &= 60^{\circ} \\ \theta_{2c} &= 0^{\circ} \\ \theta_{3c} &= -60^{\circ}\end{aligned} \tag{3.42}$$

The carrier shifting angle between the power cells in different phases is the 120 degree, which is the same with that in the proposed method 2.

3.6.1. Simulation Result for the Proposed Filter Method 3

By adopting the proposed Method 3, the inductor L_1 is designed to meet the IEEE standard. Fig. 3.24 shows the harmonic content at PCC where L_1 is designed to be 0.5mH (1.47% p.u.). As can be seen, the current harmonics are under the limits given in the IEEE std 519-2014 standard with the proposed control technique Method 3.

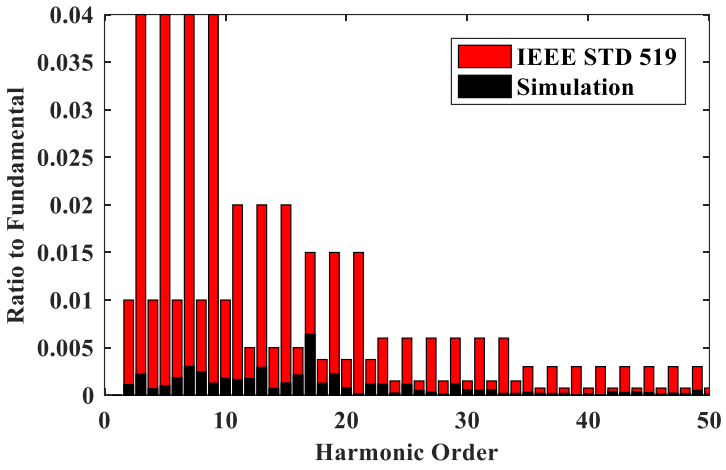
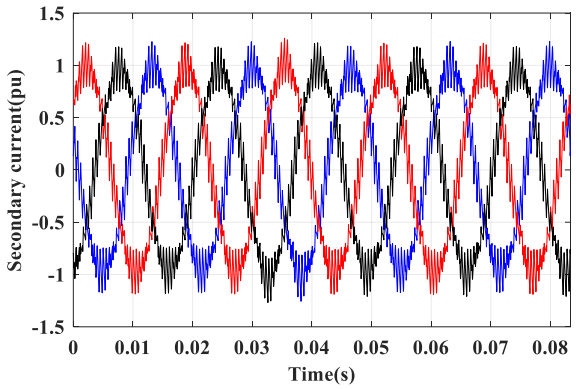


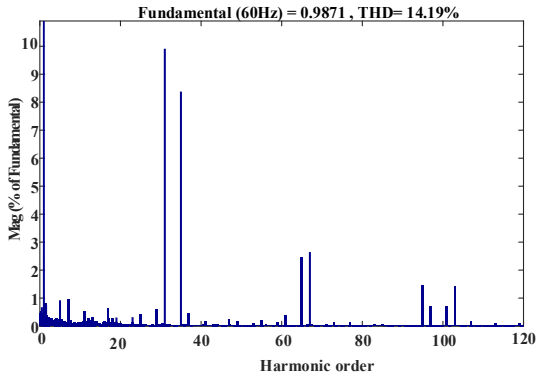
Fig. 3. 24 Current Harmonic Content at PCC (Method 3)

The current and voltage waveforms are shown in Fig.3.25. As is shown, the secondary side current TDD is 14.19% due to the small filter L_1. However, the primary side TDD reduces to 1.17% with the proposed method 3. The 31st and 35th order harmonics are mitigated with the new carrier shifted angles. What's more, the switching sideband around 99th order (mainly 97 and 101

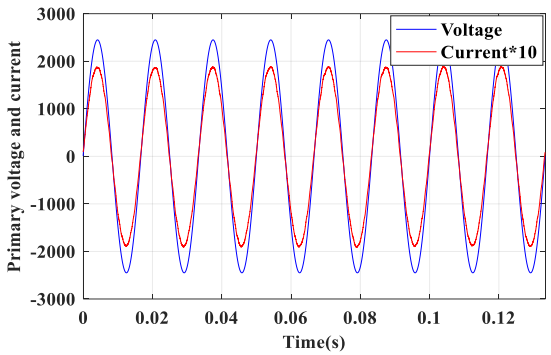
order) current harmonics are also eliminated with the extra carrier shifted angles, which matches the analysis illustrated before.



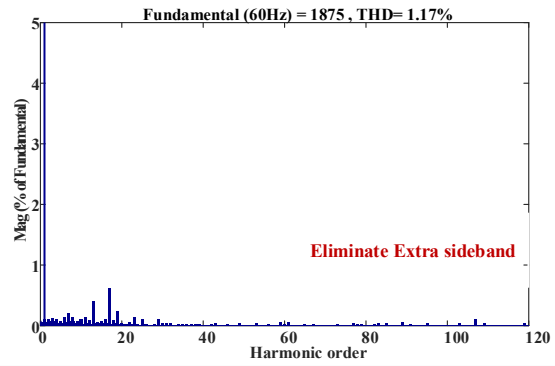
(a)Secondary side current



(b)Secondary side current TDD



(c)Primary side current and voltage waveform



(d)Primary side current TDD

Fig. 3. 25 Current and Voltage Waveforms for Filter Design (Method 3)

Compared with the proposed Method 2, more carrier shifting angles are introduced into the regenerative CHB drives in proposed Method 3. The emerging sideband harmonics around 99th order are further eliminated. As a result, with the same amount of the filter L_1, compared with method 2, the TDD at the PCC point in method 3 is reduced from 1.86% to 1.17%. This further improves the TDD harmonic profile of the regenerative CHB drives, which is considered as the optimal filter design for the regenerative CHB drive system.

Table 3. 10 Comparison among the designed filters under 1980 Hz (pu) 1100V DC Bus voltage (pu)

Filter Type	L_1	R_f	C_f	L_2	Lp	Cp	Rp	Lg	TDD_P Max=5%	TDD_S Max=20%	31th harmonic	35th harmonic	Satisfy
L	9.9%	-	-	-	-	-	-	-	3.37%	5.01%	2.24%	1.97%	No
LCL (case 1) Large Cap.	6.69%	12.86%	38.4%	2.42%	-	-	-	-	3.48%	7.41%	0.39%	0.29%	Yes
LCL (case 2) Smaller Cap.	6.2%	14.24%	18.8%	6.07%	-	-	-	-	1.4%	2.2%		0.3%	Yes
Proposed Method 1 (L+ PS controller +Trap Filter)	5.87%	-	-	-	2.84%	2.82%	4.95%	2%	1.2%	6.85%		0.3%	Yes
Proposed Method 2 (L with PS Controller)	1.47%	-	-	-	-	-	-	-	1.86%	14.17%			Yes
Proposed Method 3 (L with PS Controller)	**1.47%**								**1.17%**	**14.17%**			**Yes**
Note: - =Not needed													

3.7. Filter Design Summary for Regenerative CHB Drives

In this chapter, to design an optimal filter for a seven-level regenerative CHB drive, five types of filters have been studied including L Filter, LCL Filter, proposed Methods 1, 2, and 3. As is summarized in Table 3.10, due to the low filtering performance, the conventional L filters cannot meet the IEEE std 519-2014 standard with the low switching frequency. The LCL filter can satisfy the IEEE standard with a large number of passive components, which is not desirable for the high power medium voltage regenerative CHB drives. The proposed Method 1 removes the sideband harmonics through the active filtering strategy by interleaving the carrier shifting angles. But it requires a trap filter at the primary side of the transformer, which is not desirable. The proposed Method 2 can satisfy the IEEE standard with a small L filter by interleaving the carrier angle between different phases. However, it also gives rise up to higher-order harmonics around 99^{th} order frequency. To solve the emerging high order sideband harmonics, method 3 is proposed which is considered the optimal design. The IEEE standards can be satisfied with a small L filter (1.47% p.u) and meanwhile, the high-order sideband harmonics around 99^{th} are removed as well with the switching frequency to be 1980 Hz.

3.8. Experiment Result

This section highlights the effectiveness of the proposed filtering methods on a scaled-down 10 kVA seven-level CHB multilevel prototype. As is illustrated in Fig. 3.26, the regenerative CHB system consists of nine regenerative power cells, an 18 pulse phase-shifting transformer, a Ti DSP cloud control system, and a dSPACE control system.

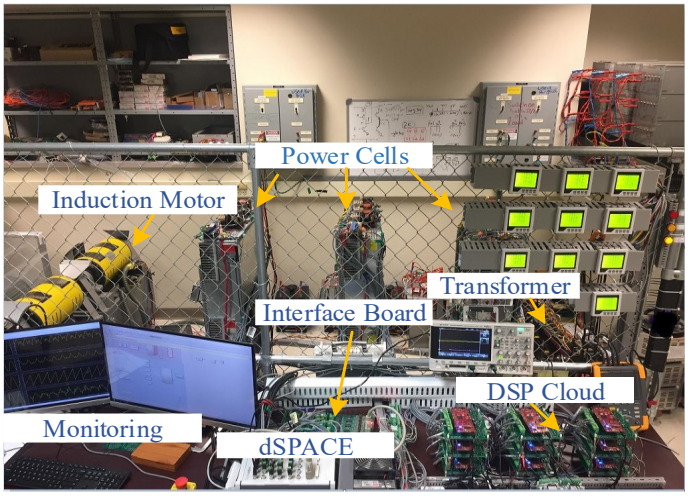
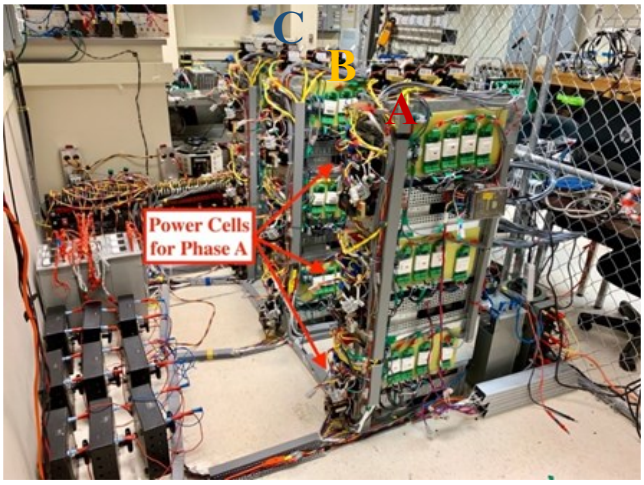


Fig. 3. 26 Prototype of the Seven-level Regenerative CHB Drive System

3.8.1. Prototype Description

As is shown in Fig. 3.27 (a), there are nine regenerative power cells for the seven-level regenerative CHB drive. Each phase is cascaded by three regenerative power cells, which generate multi-level output voltages on the motor side to achieve medium voltage.

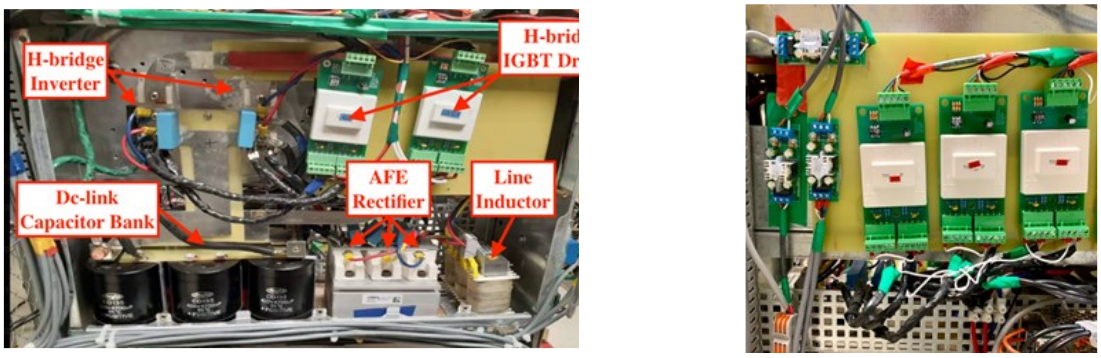


(a) Regenerative power cells layout

(b)Phase-shifting Transformer

Fig. 3. 27 Prototype of the Seven-level CHB Inverter

The 18 pulse phase-shifting transformer is shown in Fig. 3.26 (b), the phase-shifting angle between the power cells in the same phase is 20 degrees. The low order harmonics below 17th order harmonics can be removed by this phase-shifting angle. The transformer primary side input voltage is 240 V, the secondary side output voltage is 80 V.



(a)Hardware Layout (b) AFE Gatings

Fig. 3. 28 One Regenerative Power Cell

The hardware layout in one generative power cell is shown in Fig. 3.28 (a). A line inductor is designed for the three-phase AFE. The DC-link capacitance can be set to different values by setting different capacitor configurations. The H-bridge inverter consists of two IGBT modules, which are controlled by two IGBT drivers. Each IGBT module is parallel connected with a snubber capacitor in case of voltage spikes currents. The AFE gatings are positioned at the back of the power cell, which is shown in Fig. 3.28 (b).

The motor side H bridge inverters are controlled through the dSPACE controller and its signal conditioning board. The proposed active filtering strategies of the AFEs are achieved by building a cloud DSP control system. The PWM carrier synchronization among the different power cells is achieved through the EPWM modules. The cloud DSP control system is shown in

Fig. 3.29. The cloud DSP system can communicate with the user interface and the dSPACE through serial communication, which is critical for system protection and advanced control.

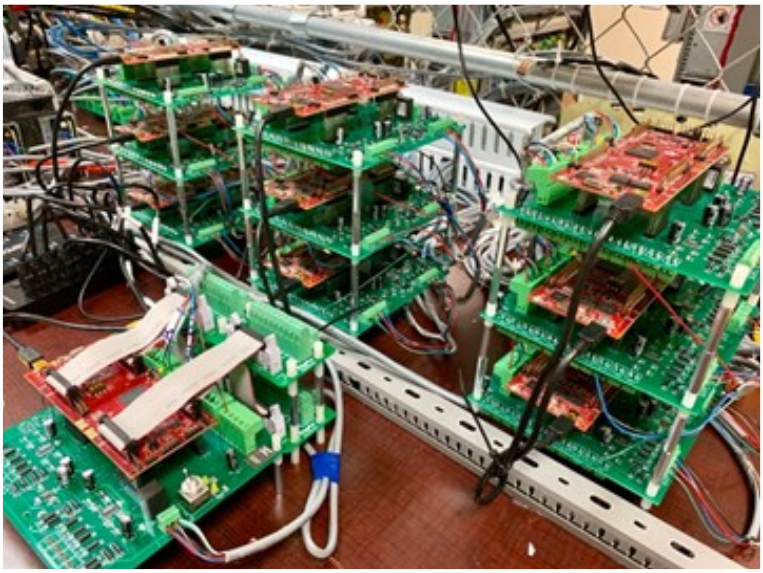


Fig. 3. 29 Cloud DSP System for AFEs

The prototype parameters for the experiment are shown in Table 3.11. The DC-link voltage is selected to be 165 V. Different IGBT switching frequencies are tested in the prototype to validate the proposed filtering strategies.

Table 3. 11 Seven-Level Regenerative CHB Inverter Prototype Parameters

Converter parameter	Value
Regenerative Power Cell DC bus voltage (V)	165
DC Capacitance (mF)	2.3
Inductor (mH)	4
Transformer primary side voltage (V)	240
Transformer secondary side voltage(V)	80
Modulation Strategy	SPWM

3.8.2. Experiment Results under 1980Hz Switching Frequency

The AFE switching frequency f_s is fixed to be 1980 Hz. The experimental validation of the proposed optimal filtering strategies (Method 3) is performed with a cloud DSP system. Experiments are carried out on a scaled-down 10 kVA seven-level CHB inverter.

As shown in Fig. 3.30, the AFE input current is highly distorted due to the low switching frequency and small inductance. From the FFT diagram in Fig. 3.30, the significant sideband harmonics under 50th order are 31th and 35th order components, which violate the IEEE std 519-2014 if not adopting the proposed optimal filtering strategy.

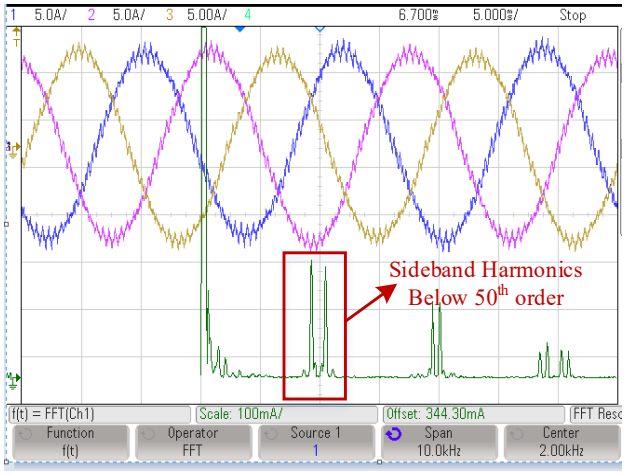


Fig. 3. 30 AFE Three-phase Current at 1980 Hz

The proposed active filtering strategy cancels out the significant sideband current harmonics for the regenerative CHB drives. To extend the proposed strategy for any given CHB drive with N cascaded H cell per phase, the carrier phase shifting angles among the cells in the same phase is $180^0/N$. Meanwhile, the carrier interleaved angle between different phases is 120^0. The AFE input currents of A1, A2, and A3 regenerative cells are shown in Fig. 3.31. The 20

degrees difference is from the phase-shifting transformer. The carrier phase shifting angles among these cells are 60 degrees for seven-level regenerative CHB drives.

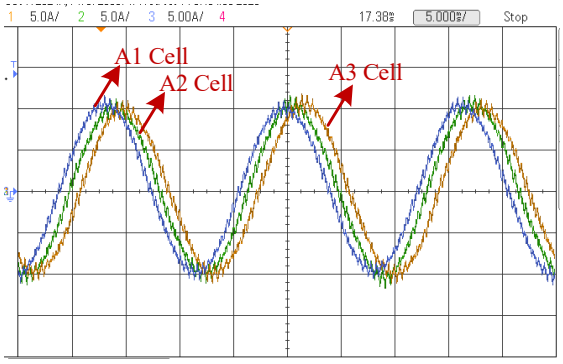


Fig. 3. 31 Power Cells Input Currents in the Same Phase

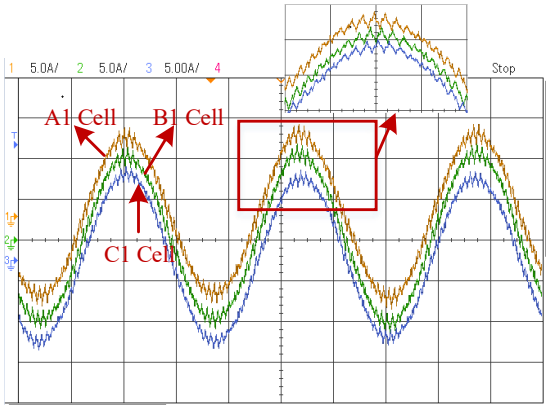
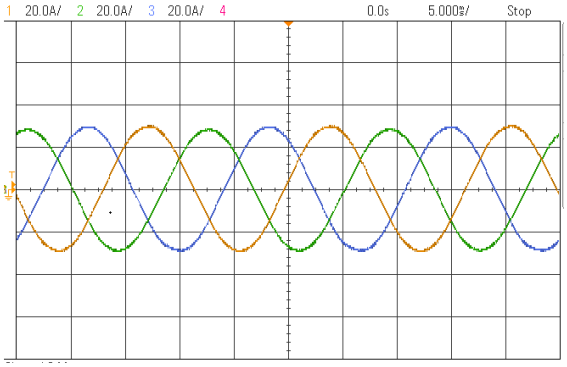
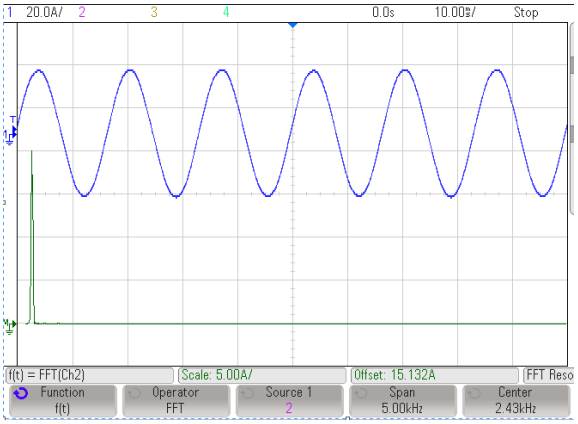


Fig. 3. 32 Power Cell Input Current among ABC Phases

The power cell input current among A1, B1 and C1 cells are illustrated in Fig. 3.32. It is noted that the carrier interleaved angle between different phases is 120 degrees, which can be validated from Fig. 3.32.



(a)PCC input current



(b) FFT diagram of PCC current

Fig. 3. 33 Current at PCC

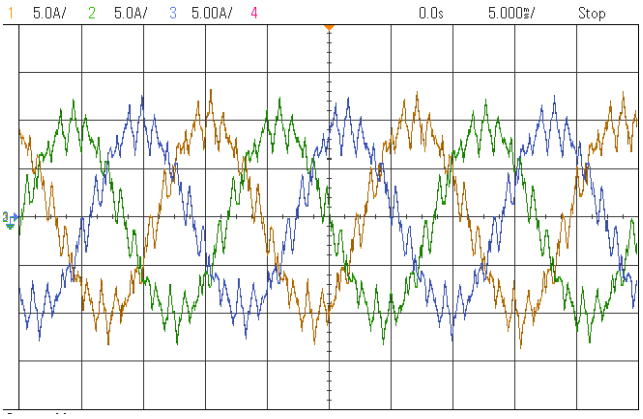
According to Fig. 3.33, the seven-level regenerative CHB drives can satisfy the IEEE std-519 2014 when operating at 1980 Hz with a 4 mH secondary L_1 filter. This cannot be achieved through the conventional filtering method without the proposed carrier angle interleaving strategy. To further demonstrate the effectiveness of the proposed optimal filtering strategy, the regenerative CHB will operate at an even lower switching frequency.

3.8.3. Experiment Results under 900 Hz Switching Frequency

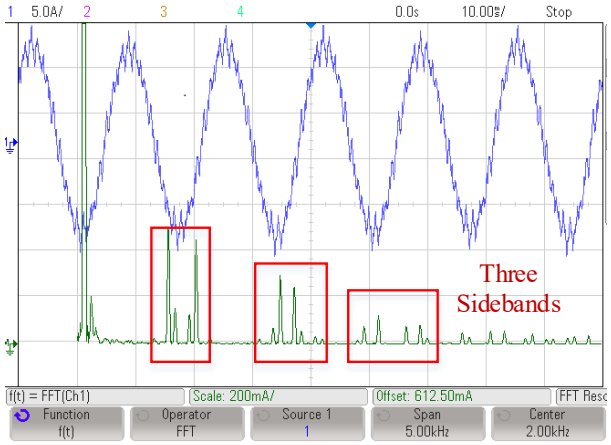
To further demonstrated the effectiveness of the proposed optimal filtering strategy, the switching frequency of the AFEs is fixed at 900 Hz for the same seven-level regenerative CHB drive. The AFE current waveform from a CHB regenerative power cell is highly distorted due to

the low switching frequency, which is illustrated in Fig.3.34 (a). The FFT of the AFE current waveform is shown in Fig.3.34 (b). It should be noted that the first three switching sideband harmonics reside under 50th order frequency. To meet the requirement of the IEEE std-519 2014, all the first three switching sideband harmonics are required to be attenuated dramatically without increasing the inductance.

By adopting the proposed optimal filtering strategy, these three significant sideband harmonics group are all eliminated at the primary side of the transformer. This is verified by the transformer primary side current waveform shown in Fig. 3.34 (c). Furthermore, the FFT analysis is performed on the transformer's primary side current. According to Fig. 3.34 (d), the seven-level regenerative CHB drives can satisfy the IEEE std-519 2014 when operating at a low switching frequency of 900Hz with a 4 mH secondary L_1 filter. This cannot be achieved through other filtering methods.

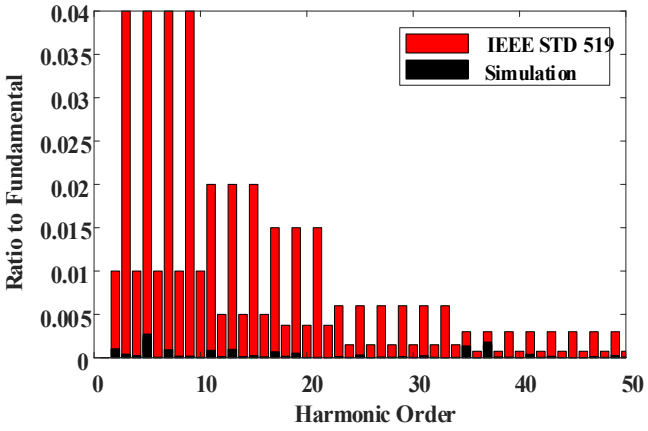


(a) Cell three-phase currents



(b) FFT of the cell currents

(c)PCC three-phase currents



(d) FFT of the PCC current

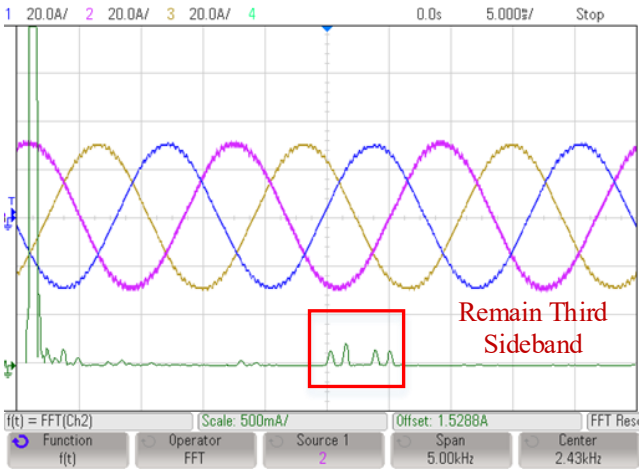
Fig. 3. 34 Experimental Waveforms of the Proposed Optimal Filtering Strategy (Method 3)

In summary, as shown in Table 3.12, to meet the requirement of the IEEE std 519, by adopting the proposed optimal filtering strategy, the inductor L_1 designed for the regenerative power cell is as low as 4 mH operating at 900Hz switching frequency. The current THD at the PCC point is 0.9%.

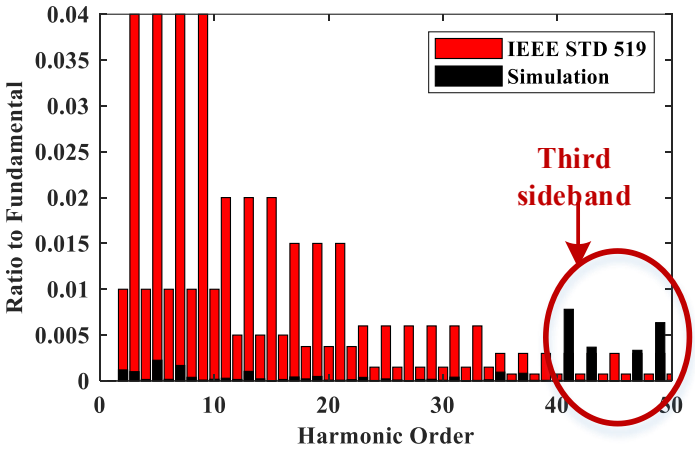
Table 3. 12 Performance of the Proposed Filtering Strategy at 900Hz Switching Frequency

Filter Type	L_1	THD_P Max=5%	Satisfy Standard
Proposed Method 3	4mH	**0.9%**	**YES**
Proposed Method 2	4mH	**1.3%**	**NO**

The carrier shifting strategy (method 2) carrier shifting strategy is adopted for the same regenerative CHB drives operating at 900 Hz switching frequency. Compared with the proposed optimal filtering strategy (Method 3), as is shown in Table 3.12, the proposed optimal shifting strategy improves slightly the current THD at the PCC point from 1.3% to 0.9%. More critical is that the current harmonic at the PCC point does not meet the requirement of the IEEE 519-2014 standard by adopting the proposed method 2 at 900 Hz switching frequency. This is because the third sideband harmonics cannot be canceled out at the PCC point with the proposed method 2 carrier shifting method, which is further validated in Fig. 3.35. The remaining third-order sideband harmonics at the PCC point violates the IEEE standards, which requires further to increase the designed filter size. Therefore, the proposed optimal filtering strategy (method 3) is more efficient to improve the grid current quality and extends the harmonic elimination to satisfy the IEEE std 519-2014 standard.



(a) PCC Current



(b) FFT of the PCC current

Fig. 3. 35 Current Harmonic Adopting the Proposed Method 2 at 900 Hz

3.9. Conclusion

To meet the IEEE std 519-2014 requirement, a filter bank is required to be designed for the regenerative CHB regenerative power cell to suppress the current harmonics. The reduction of the required filter bank is a crucial point for the drive system in terms of cost, volume, and thermal. This chapter proposed a comprehensive study on the filtering strategies for regenerative CHB, thus decreasing the filter size and cost significantly.

Five types of filters have been studied including L Filter, LCL Filter, proposed Methods 1, 2, and 3 in this chapter. It is demonstrated that the proposed Method 3 is an optimal filtering solution for the regenerative CHB drives. Compared with the other filtering strategies, the proposed optimal filtering strategy (Method 3) is more efficient and extends the harmonic elimination further to the third significant sideband harmonics group. It further improves the grid current quality and makes it possible for the regenerative drive system to operate at low switching frequency with a reduced filter while complying with the IEEE standard.

Chapter 4

A New DC-Link Ripple Voltage Controller for Regenerative CHB Drives to Reduce the DC-link Capacitance

4.1. Introduction

As is illustrated previously, the regeneration capability of the CHB drives can be achieved by replacing the three-phase diode rectifier with the PWM rectifiers at the input side in the power cell. This regenerative CHB topology with active front ends (AFEs) attracts a lot of attention from manufacturers. However, with the conventional dc bus voltage controller [45], only a constant power is delivered through the three-phase AFE. The instantaneous power in each power cell between the three-phase AFE and the single-phase H-bridge is not balanced. This

unbalanced power ripple has to be absorbed by a large dc-link electrolytic capacitor to maintain a stable dc voltage, which increases the system's volume and cost [46]. Moreover, the pulsating power ripple flowing through the dc-link electrolytic capacitors raises up the dc-link voltage fluctuation with twice the output frequency. The temperature rise caused by voltage ripple accelerates evaporation of the electrolyte, thus reducing the capacitor's life expectancy and the system reliability as well.

To shrink the dc-link capacitance, direct determining the reference currents for the three-phase AFE based on the voltage ripple is a promising solution especially when the instantaneous power at the motor side is not measured. However, the voltage ripple controller should be carefully designed since it may impact the system's stability. The potential instability issue hasn't been given enough attention before. Two main challenges for implementing the dc bus voltage ripple controller are summarized:

1. The dc-link voltage ripple frequency varies with the motor speed, which makes it difficult to real-time detect the voltage ripple amplitude and phase angle.
2. More critical issue is the fact that the voltage ripple control system may lose stability in some operation range when excess pulsating power ripple is injected by the AFE. This large-signal instability issue cannot be found in small-signal stability analysis tools.

To avoid aforementioned problems, this chapter proposes a novel voltage ripple controller to reduce the dc-link capacitance in the regenerative CHB drive without extra measurements. A high-performance adaptive filter is proposed to accurately detect the dc-bus voltage ripple amplitude and phase angle, which are later employed to determine the reference current of the AFE. Moreover, the potential instability issue is pointed out and discussed. The proposed voltage

ripple controller can avoid unstable operation points, which is ignored by the existing control strategies.

4.2. Instantaneous Power Flow Analysis

In this section, the root cause of a large dc-link capacitor in the regenerative power cell is studies based on the instantaneous power flow analysis. Then the relation between the current and instantaneous power is derived based on the instantaneous power theory.

4.2.1. Root Cause of Large dc-link Capacitance

As is shown in Fig. 4.1, in regeneration mode, the instantaneous power p_0 comes from the motor through the H-bridge.

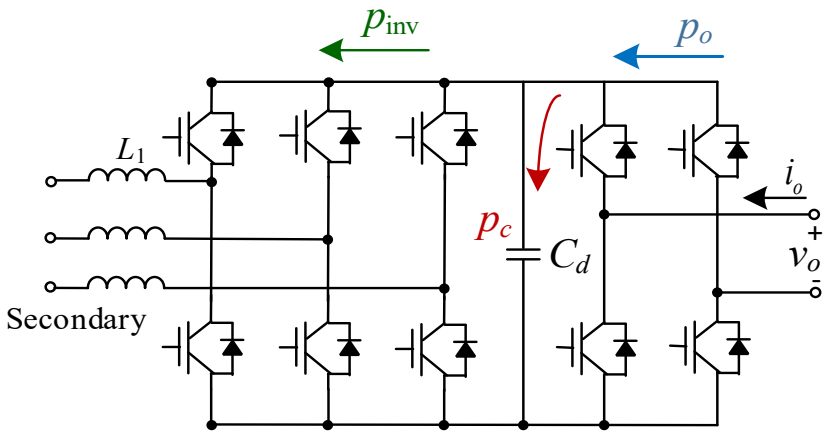


Fig. 4. 1 Instantaneous Power Flow during Regeneration

The output voltage and current of the H-bridge are v_o and i_o at the output frequency ω_m. The instantaneous power coming from the H bridge is:

$$\begin{aligned} p_o &= v_o i_o = V_o \sin(\omega_m t + \phi_1) I_o \sin(\omega_m t + \phi_1 - \phi_2) \\ &= \frac{1}{2} V_o I_o \cos(\phi_2) - \frac{1}{2} V_o I_o \cos(2\omega_m t + 2\phi_1 - \phi_2) \\ &= P_o + \tilde{p}_o \end{aligned} \tag{4.1}$$

where ϕ_1 is the initial phase angle of the output voltages, ϕ_2 is the motor power factor angle. As is shown in equation (4.1), the instantaneous power coming from the H-bridge contains an average component P_o and a large second-order pulsating power ripple $\tilde{p}_o$. Meanwhile, the AFE allows for regenerating the power into the grid, which is denoted as p_{inv}. As is shown in Fig 4.1, the DC-link capacitor C_d is the only energy storage element between the AFE and H bridge. This capacitor has the responsibility to absorb all the instantaneous power differences between the AFE and H bridge. This indicates:

$$p_c = p_o - p_{inv} \tag{4.2}$$

where p_c is the instantaneous power that flows into the dc capacitor. When an average power P_o is delivered to the grid by the AFE in steady-state, which indicates $P_{inv}=P_o$, the pulsating power ripple $\tilde{p}_o$ has to be absorbed by the dc capacitor C_{dc}. Equation (4.2) becomes

$$p_c = \tilde{p}_o = -\frac{1}{2} V_o I_o \cos(2\omega_m t + 2\phi_1 - \phi_2) \tag{4.3}$$

The pulsating power ripple interacts with the DC-link capacitor, raising up the second-order harmonic voltage ripple on the capacitors. The dc voltage ripple $\tilde{u}_{dc}$ is calculated in steady-state as:

$$\tilde{u}_{dc} = -\frac{V_o I_o \sin(2\omega_m t + 2\phi_1 - \phi_2)}{4\omega_m C_d U_{dc}} \tag{4.4}$$

where U_{dc} is the dc-link voltage average DC component. To maintain a stable dc bus voltage, the design of the dc-link capacitor should provide storage for the pulsating power ripple. According to equation (4.4), an oversized designed capacitor C_d is required to suppress the dc voltage ripple $\tilde{u}_{dc}$, especially when the drive operates at lower frequencies below the nominal value.

To reduce the dc capacitance and voltage ripple, instead of delivering only the average constant power into the grid, the alternative solution is to deliver both the average power and the pulsating power ripple to the grid as well through the AFE. In this way, the pulsating power ripple p_c that flows across the capacitors is reduced. Thus, the required dc capacitance is reduced significantly to achieve a stable dc voltage.

4.2.2. Constant Average Power Delivered through AFE

Assume the transformer secondary ac voltages in the power cell is ideal. As is shown in the equation (4.5), the three-phase grid voltage vector for *xi* cell is denoted as $\mathbf{v}_{xi}^{+}$ and $\mathbf{v}_{xi\perp}^{+}$ presents an orthogonal vector of $\mathbf{V}_{xi}^{+}$, where *xi* presents the location of the power cell in the regenerative CHB drive (*x* denote the phase index and *i* denotes the cascaded cell index).

$$\mathbf{v}_{xi}^{+} \triangleq \begin{bmatrix} v_{axi} \\ v_{bxi} \\ v_{cxi} \end{bmatrix} = \begin{bmatrix} V\cos(\omega_s t + \theta_s) \\ V\cos(\omega_s t + \theta_s - \frac{2\pi}{3}) \\ V\cos(\omega_s t + \theta_s + \frac{2\pi}{3}) \end{bmatrix} \tag{4.5}$$

$$\mathbf{v}_{xi\perp}^{+}=\begin{bmatrix}\sin(\omega_g t+\theta_a)\\ \sin(\omega_g t+\theta_a-\frac{2\pi}{3})\\ \sin(\omega_g t+\theta_a+\frac{2\pi}{3})\end{bmatrix}$$

According to instantaneous power theory, if an average active power P_o coming from the H-bridge is delivered by the three-phase AFE, the injected current $\mathbf{i}_{\mathbf{r0}\_xi}^{*}$ at grid frequency ω_g is derived in equation (4.6). An arbitrary amount of reactive power Q_0 can be injected to the grid simultaneously without influencing the instantaneous power flow across the dc-link since the summation of the three-phase reactive power is zero.

$$\begin{aligned}\mathbf{i}_{\mathbf{r0}\_xi}^{*}&=\frac{P_0}{\left|\mathbf{v}_{xi}^{+}\right|^2}\mathbf{v}_{xi}^{+}+\frac{Q_0}{\left|\mathbf{v}_{xi}^{+}\right|^2}\mathbf{v}_{xi\perp}^{+}\\&=\frac{V_o I_o\cos(\phi_2)V}{2\left|\mathbf{v}_{xi}^{+}\right|^2}\begin{bmatrix}\cos(\omega_g t+\theta_a)\\ \cos(\omega_g t+\theta_a-120^o)\\ \cos(\omega_g t+\theta_a+120^o)\end{bmatrix}+\frac{Q_0 V}{\left|\mathbf{v}_{xi}^{+}\right|^2}\begin{bmatrix}\sin(\omega_g t+\theta_a)\\ \sin(\omega_g t+\theta_a-120^o)\\ \sin(\omega_g t+\theta_a+120^o)\end{bmatrix}\end{aligned}\tag{4.6}$$

4.2.3. Pulsating Power Ripple Delivered through AFE

To reduce the dc-link capacitance, an extra pulsating power ripple $\tilde{p}_o$ shown in equation (4.3) is required to be delivered through the AFE as well. As is illustrated in equation (4.7), the pulsating ripple power $\tilde{p}_o$ is compensated by injecting an extra current component $\mathbf{i}_{\mathbf{r1}\_xi}^{*}$ at $2\omega_m$-ω_g. It is noted that an arbitrary amount of instantaneous reactive power $\tilde{q}_o$ can be injected together with ripple power $\tilde{p}_o$ without impacting the power flow across the dc bus. This is due to the fact that the summation of the three-phase instantaneous reactive power is zero. The injected

instantaneous reactive power $\tilde{q}_o$ is 90° interleaved with the instantaneous active power $\tilde{p}_o$ in equation (4.7) to minimize the increase of the modulation index.

$$\begin{aligned}\mathbf{i}^*_{\mathbf{r1}\_xi} &= \frac{\tilde{p}_o}{\left|\mathbf{v}^+_{xi}\right|^2}\mathbf{v}^+_{xi} + \frac{\tilde{q}_o}{\left|\mathbf{v}^+_{xi}\right|^2}\mathbf{v}^+_{xi\perp} \\ &= \frac{-\frac{1}{2}V_o I_o \cos(2\omega_m t + 2\phi_1 - \phi_2)V}{\left|\mathbf{v}^+_{xi}\right|^2}\begin{bmatrix}\cos(\omega_g t+\theta_a)\\ \cos(\omega_g t+\theta_a-120^o)\\ \cos(\omega_g t+\theta_a+120^o)\end{bmatrix} + \frac{-\frac{1}{2}V_o I_o \sin(2\omega_m t + 2\phi_1 - \phi_2)V}{\left|\mathbf{v}^+_{xi}\right|^2}\begin{bmatrix}\sin(\omega_g t+\theta_a)\\ \sin(\omega_g t+\theta_a-120^o)\\ \sin(\omega_g t+\theta_a+120^o)\end{bmatrix} \\ &= -\frac{V_o I_o V}{2\left|\mathbf{v}^+_{xi}\right|^2}\begin{bmatrix}\cos(2\omega_m t + 2\phi_1 - \phi_2 - \omega_g t - \theta_a)\\ \cos(2\omega_m t + 2\phi_1 - \phi_2 - \omega_g t - \theta_a + 120^o)\\ \cos(2\omega_m t + 2\phi_1 - \phi_2 - \omega_g t - \theta_a - 120^o)\end{bmatrix}\end{aligned} \tag{4.7}$$

4.2.4. Ripple Current Component Cancellation

To eliminate the dc bus voltage ripple in the regenerative CHB power cells, both the average power P_o and pulsating power ripple $\tilde{p}_o$ are delivered to the grid by injecting two current components: $\mathbf{i}^*_{\mathbf{r0}\_xi}$ at ω_g and $\mathbf{i}^*_{\mathbf{r1}\_xi}$ at $2\omega_m$-ω_g frequency at the transformer secondary side. It is important to note that the $\mathbf{i}^*_{\mathbf{r1}\_xi}$ current component from the power cells in different phases cancel out with each other at the transformer primary side. This is:

$$\sum_{x=a,b,c}\mathbf{i}^*_{\mathbf{r1}\_xi} = 0 \tag{4.8}$$

where x denotes the phase index and i denotes the cascaded cell index. For a seven-level regenerative CHB shown in Fig. 4.2, three power cells (i=1, 2, or 3) are cascaded in each phase (x= a, b, or c phase). As a result, only the current component $\mathbf{i}^*_{\mathbf{r0}\_xi}$ at ω_g frequency is reflected in

the transformer's primary side in each power cell. This superb merit allows the AFEs to deliver the pulsating ripple power to reduce the dc-link capacitance without deteriorating the grid harmonic profile at the transformer primary side.

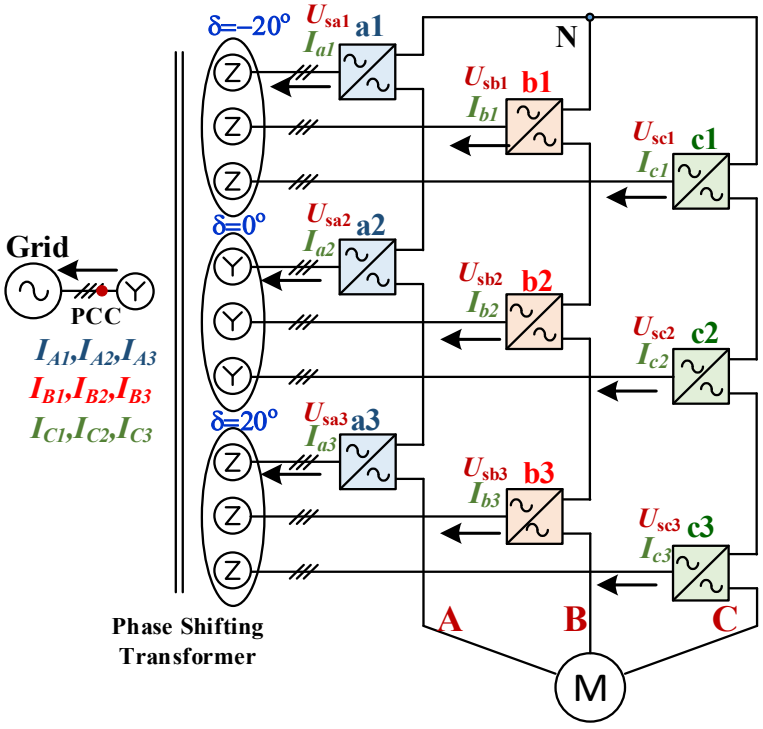


Fig. 4. 2 Seven-level CHB Drive Illustration for Capacitor Reduction

4.3. Proposed Voltage Ripple Controller

4.3.1. Structure of the Proposed Voltage Ripple Controller

The dc-link voltage ripple at $2\omega_m$ can be completely eliminated by injecting an extra current component $\mathbf{i}^*_{\mathbf{r1}\_xi}$. However, as is shown in equation (4.7), the measurements of the motor power factor angle ϕ_2 and the motor side current RMS value I_o are required to determine the

injected current component. To avoid adding extra measurements, this paper proposes a novel dc capacitance reduction strategy based on the adaptive filter.

As is shown in Fig. 4.3, the phase angle of the injected current component $\mathbf{i}_{\mathbf{r1}\_xi}$ is estimated from the dc voltage ripple phase angle and grid voltage phase angle according to equation (4.7). Meanwhile, the amplitude of the current component $\mathbf{i}_{\mathbf{r1}\_xi}$ can be determined by the proposed voltage ripple controller based on the detected voltage ripple amplitude. The voltage controllers provide the current reference for the current controller based on the dc average voltage $\bar{u}_{dc}$ or its ripple $\tilde{u}_{dc}$. The current controller does nothing more than tracking the current references. A multitude of solutions has been developed for current tracking control in the existing literature. Hysteresis current tracking controller is adopted in this paper. Other current controllers will not be discussed since it is not the main challenge.

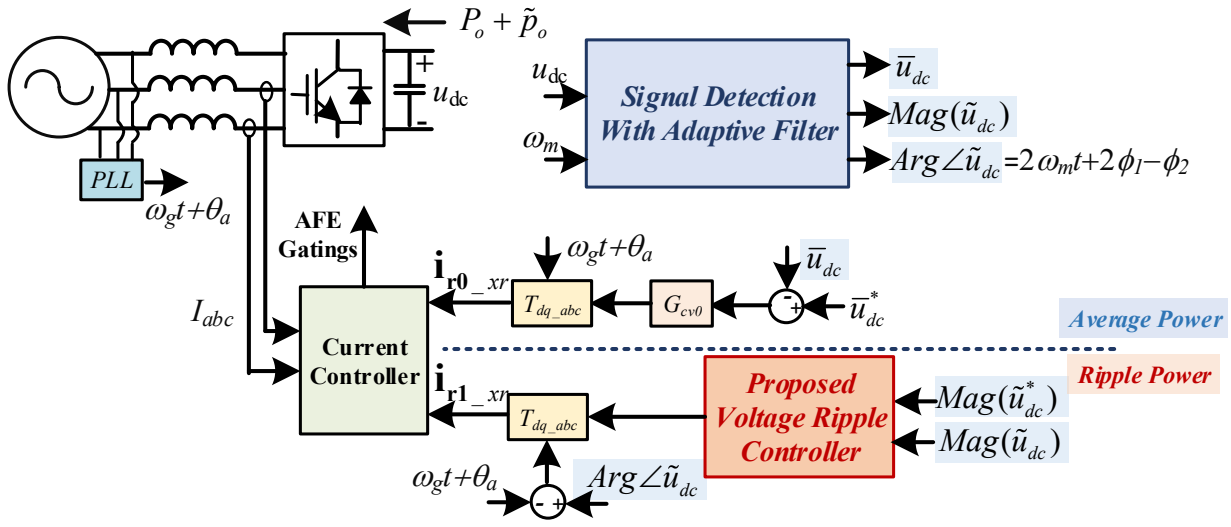


Fig. 4. 3 Proposed DC Bus Voltage Control Scheme

4.3.2. Stability Problem Illustration

There are two main challenges for implementing the controller to reduce the dc-link capacitance. First of all, as is shown in Fig. 4.3, the voltage ripple amplitude $mag(\tilde{u}_{dc})$ and voltage ripple phase angle $Arg\angle\tilde{u}_{dc}$ are required to be extracted from the dc bus voltage measurement. However, the dc bus voltage ripple varies with the motor speed, which makes it difficult to detect the phase angle from the dc bus voltage measurement without phase delay. A high-performance adaptive signal detection strategy should be designed to take the frequency variation into consideration in the controller. A more critical issue is that the voltage ripple control system may even lose stability in some operation range, which didn't draw enough attention.

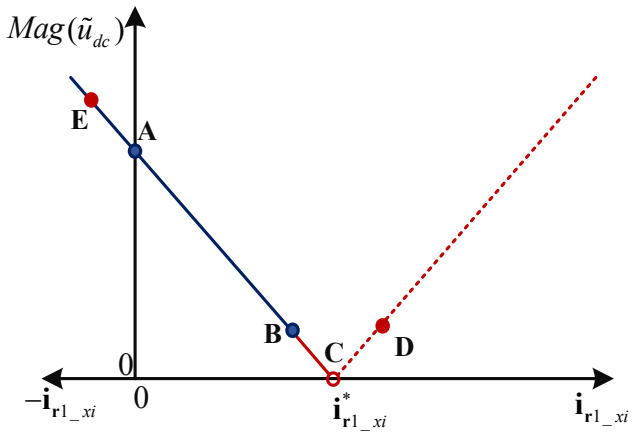


Fig. 4. 4 Potential Operation Condition

As is shown in Fig. 4.4, the power cell first operates at point A with a substantial voltage ripple. As the injected $\mathbf{i}_{\mathbf{r1}\_xi}$ increases, the dc-link voltage ripple starts to decrease. When the operation point comes to C, as is shown in Fig. 4.4, the second-order harmonic of the voltage ripple is eliminated. This optimal operation point, however, unfortunately, is not stable. Because

the voltage ripple phase angle $Arg\angle\tilde{u}_{dc}$ cannot be extracted from the voltage measurement anymore as the dc voltage ripple is completely eliminated at point C. The phase angle information of the injected current component $\mathbf{i}_{\mathbf{r}1\_xi}$ cannot be calculated out, which leads to controller corruption. To avoid this potential issue, the proposed voltage ripple controller set the power cell operation point at B such that the voltage ripple is reduced to a reasonable value still allowing for phase angle detection of $Arg\angle\tilde{u}_{dc}$.

Moreover, during transient dynamics of the current tracking controller, an extra amount of the current $\mathbf{i}_{\mathbf{r}1\_xi}$ may be injected by AFE. As is shown in Fig. 4.4, the transient operation point may be moved from B point to D point when an overshot excess pulsating ripple power is delivered by the AFE. This transient state has to be avoided since dc voltage ripple phase angle $Arg\angle\tilde{u}_{dc}$ is shifted 180 degrees when the excess power ripple is delivered. With phase-shifted angle flipped, the current component $\mathbf{i}_{\mathbf{r}1\_xi}$ will inversely tend to increase the voltage ripple. The power cell power operating point is moved from D to E as the power ripple delivered by the AFE flipped over. The system loses stability and a new voltage ripple controller should tackle this potential stability issue by preventing excess power ripple injection in a transient state.

4.3.3. Signal Detection with Adaptive Filter

As is shown in Fig. 4.3, the voltage ripple amplitude $mag(\tilde{u}_{dc})$ and voltage ripple phase angle $Arg\angle\tilde{u}_{dc}$ are required to be extracted from the dc bus voltage measurement. However, the dc bus voltage ripple varies with the motor speed, which makes it difficult to detect the phase angle from the dc bus voltage measurement without phase delay. To tackle this challenge, an adaptive filter shown in Fig. 4.5 is proposed.

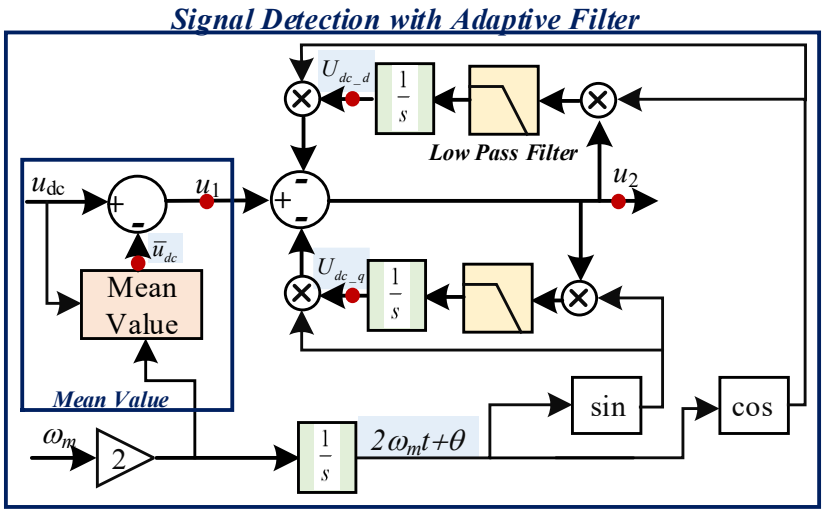


Fig. 4. 5 Signal Detection with Adaptive Filters

The voltage ripple contains a large $2\omega_m$ component in steady operation. The average dc voltage component $\bar{u}_{dc}$ can be calculated by integral the dc voltage measurement u_{dc} over a period of $1/2f_m$, The mean value at the variable frequency is shown in equation (4.9).

$$\bar{u}_{dc} = 2f_m \int_{t-1/2f_m}^{t} u_{dc}\,dt \tag{4.9}$$

The dc-bus voltage signal $u_1(t)$, illustrated in Fig. 4.5, is a continuous periodic signal without the dc component. The significant component of $u_1(t)$ signal shown in equation (4.4) can be further rewritten on an arbitrary rotating frame $2\omega_m+\theta$ as

$$\begin{aligned} u_1(2\omega_m t) &= |\tilde{u}_{dc}|\sin(2\omega_m t + 2\phi_1 - \phi_2) \\ &= A_1\sin(2\omega_m t+\theta) + B_1\cos(2\omega_m t+\theta) \end{aligned} \tag{4.10}$$

The phase angle $2\omega_m t + 2\phi_1 - \phi_2$ of the dc voltage ripple component $u_1(t)$ should be estimated accurately to control the injected current component. As is shown in Fig. 4.5, the

voltage ripple u_1(t) is projected to a rotating frame rotating at $2\omega_m+\theta$. The proposed method estimates the projected coefficients A_1 and B_1 on the arbitrary rotating frame rotating $2\omega_m t+\theta$. Once the projected coefficients $A1$ and $B1$ are estimated through the adaptive filter, the phase angle $2\omega_m t+2\phi_1-\phi_2$ is determined based on equation (4.10).

If a $2\omega_m$ frequency component exists in the residual signal u_2, as is shown in Fig. 4.5, multiplying the signal u_2 with the $\cos(2\omega_m t+\theta)$ or $\sin(2\omega_m t+\theta)$ results in a dc constant component value and a $4\omega_m$ high-order frequency signal ripple. The $4\omega_m$ component is eliminated by the designed low pass filter. The dc component is obtained to further estimate the projected coefficients A_1 and B_1. A simple first-order filter can be designed:

$$H(s)=\frac{G}{T_1 s+1} \tag{4.11}$$

Where G is the gain parameter and T_1 is the filter parameter. The transfer function H(s) between u_2 and u_1 can be calculated:

$$H(s)=\frac{u_2(s)}{u_1(s)}=\frac{2G(T_1 s^2+s-4T_1\omega_m^2)}{(s^2+4\omega_m^2)(T_1 s^2+2T_1 s+4T_1^2\omega_m^2+1)} \tag{4.12}$$

The frequency response of adaptive filter H(s) in the stationary frame is represented in Fig. 4.6 on linear scales for two selected values T_1 and ω_m to be 0.5 and 60*2π.

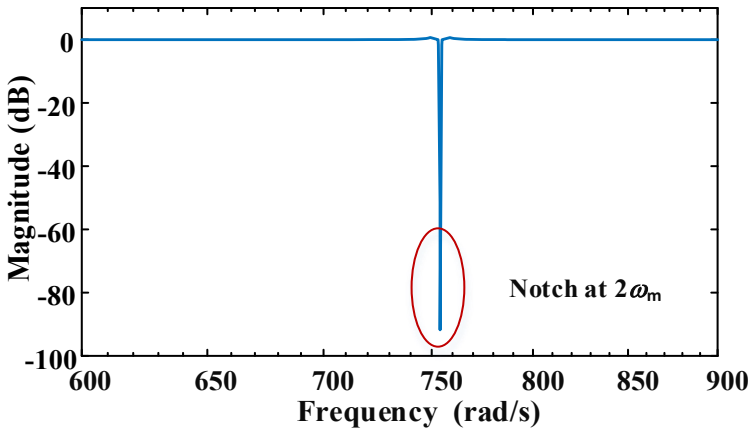


Fig. 4. 6 Frequency Response of Adaptive Filter H(s) T_1=0.1, ω_m=60*2π

As is shown in the bode figure, the transfer function H(s) between signals u_2 and u_1 is a notch filter at $2\omega_m$. The $2\omega_m$ frequency component in u_1 is removed by the adaptive filter. This indicates, in steady-state, the estimates of A_1 and B_1 are U_{dc_q} and U_{dc_d} respectively. The equation (4.10) can be rewritten as

$$\begin{aligned} u_1(2\omega_m t) &= U_{dc\_q}\sin(2\omega_m t+\theta)+U_{dc\_d}\cos(2\omega_m t+\theta) \\ &= \sqrt[2]{U_{dc\_q}^2+U_{dc\_d}^2}\sin(2\omega_m t+\theta+\varphi) \end{aligned} \tag{4.13}$$

Where

$$\varphi = arc\tan\left(\frac{U_{dc\_d}}{U_{dc\_q}}\right)$$

Compared with equation (4.10) and (4.13), the dc voltage ripple amplitude and phase angle at $2\omega_m$ can be estimated in Fig. 4.7. It should be noted that the signal detection of the voltage ripple amplitude and phase angle is adaptive based on the ω_m.

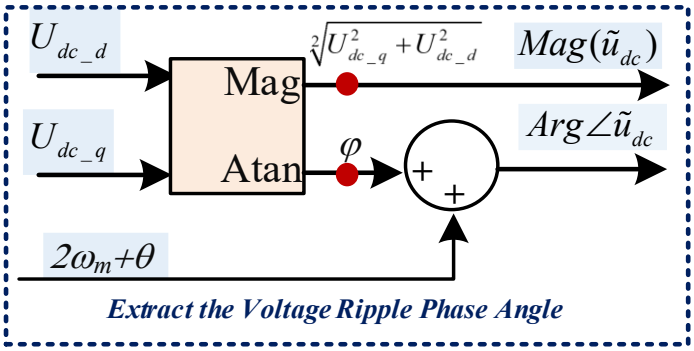


Fig. 4. 7 DC Voltage Ripple Phase Angle Estimation

4.3.4. Proposed Voltage Ripple Control

Determining the amplitude of the ripple current is challenging due to the potential instability. To avoid the ahead mentioned stability problem, the proposed voltage ripple control strategy is shown in Fig. 4.8.

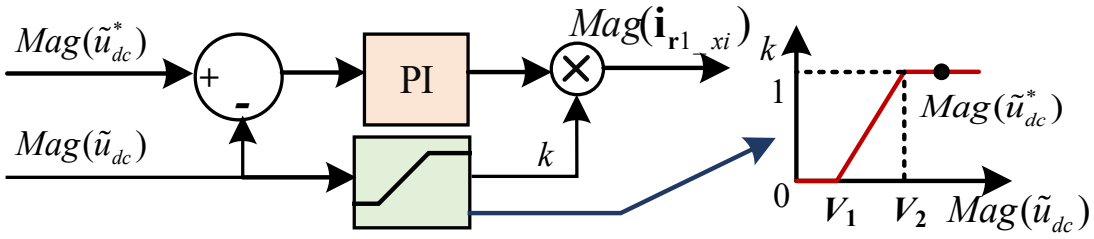


Fig. 4. 8 Proposed Voltage Ripple Controller

First of all, the voltage ripple magnitude reference $Mag(\tilde{u}_{dc}^*)$ cannot be set to near zero. This is because the voltage ripple phase angle $Arg\angle\tilde{u}_{dc}$ cannot be extracted from the voltage measurement once the dc voltage ripple is near zero. The phase angle of the injected current component $\mathbf{i}_{r1\_xi}$ to reduce the dc-bus voltage ripple cannot be determined as a result. To avoid

the instability operation region, in the proposed controller, $Mag(\tilde{u}_{dc}^{*})$ is chosen as 3%~5% of the dc bus average voltage depends on the measurement accuracy.

Second, during transient dynamics, the system may lose stability when an extra amount of the current $\mathbf{i}_{\mathrm{rl\_}xi}$ may be injected by AFE. Excess power ripple injection in the transient state should be avoided as much as possible. To tackle this, as is shown in Fig. 4.8, if the measured voltage ripple is reduced to a low value below V_2, a parameter k selected between [0, 1] is introduced to restrict the output current amplitude of $\mathbf{i}_{\mathrm{rl\_}xi}$ based no the designed slope. This forces the operation point away from the unstable region.

4.4. Simulation Studies

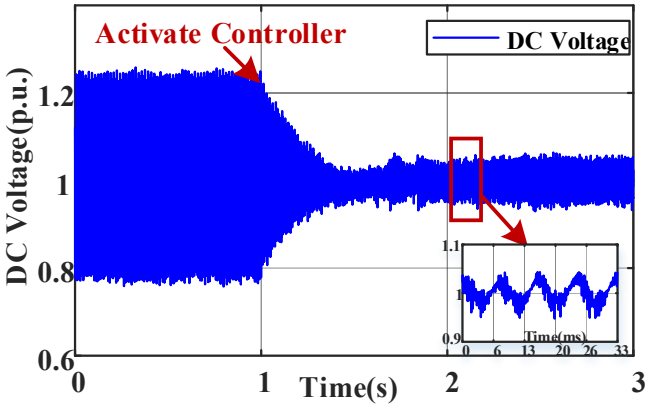
To validate the proposed method a set of simulation studies have been conducted to assess the extent of the capacitor ripple reduction and capacitor size reduction at different load frequencies. System parameters are presented in Table 4.1.

Table 4. 1 Seven-level CHB Inverter Main Parameters for Simulation

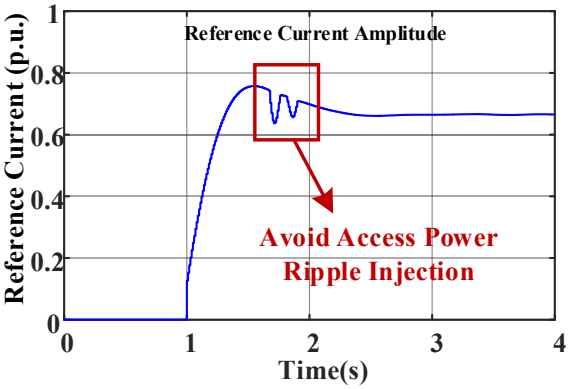
Converter parameter	Value
Cell Dc-link voltage (V)	1600
Transformer secondary side voltage(V)	650
Transformer Leakage Inductance (mH)	0.3mH
Grid-Tied Inductance L_1 (mH)	4 mH
Grid Side Rated Current Per Cell	70A
DC-Link Capacitance	240 μF

A simulation model with the parameters listed in Table 4.1 was built in MATLAB/Simulink. A constant series RL load with a 0.9 power factor was used in this model. The H bridge output frequency is 60 Hz. As is shown in Fig. 4.9 (a), the ripple power injection control loop is not activated, the dc voltage ripple achieves more than 0.4 p.u. After 1 second, the

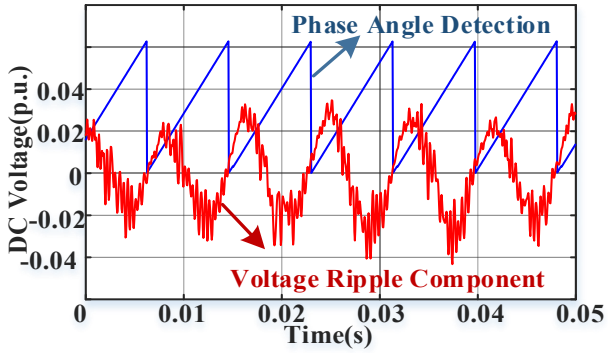
proposed voltage ripple controller takes over and suppresses the dc voltage ripple under 3% with the same capacitance. It is noted that, instead of 240 μF, more than 2000 μF capacitance is needed in each cell to restrict the steady-state dc voltage ripple under 3% without the proposed voltage ripple controller.



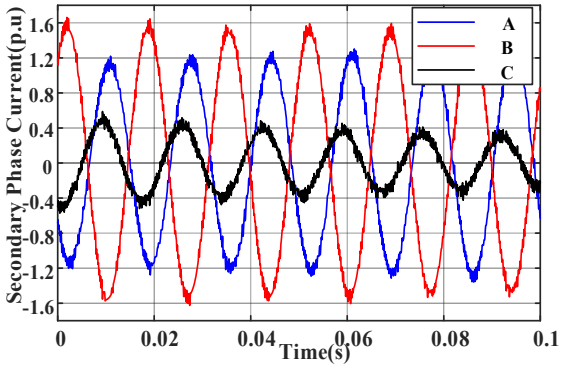
(a)DC Voltage Dynamics



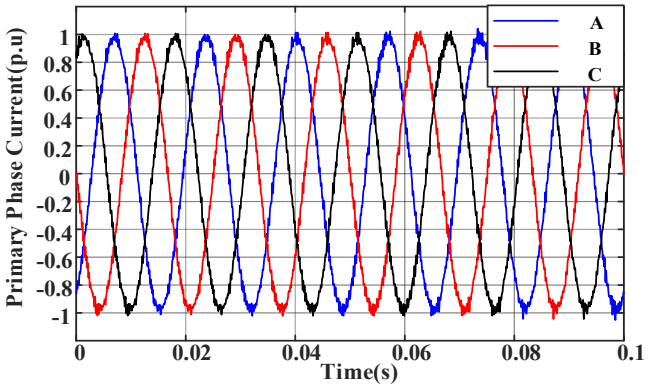
(b)Proposed Voltage Ripple controller Dynamics



(c) Phase Detection with Adaptive Filter



(d) Secondary Current



(e)Primary side Current

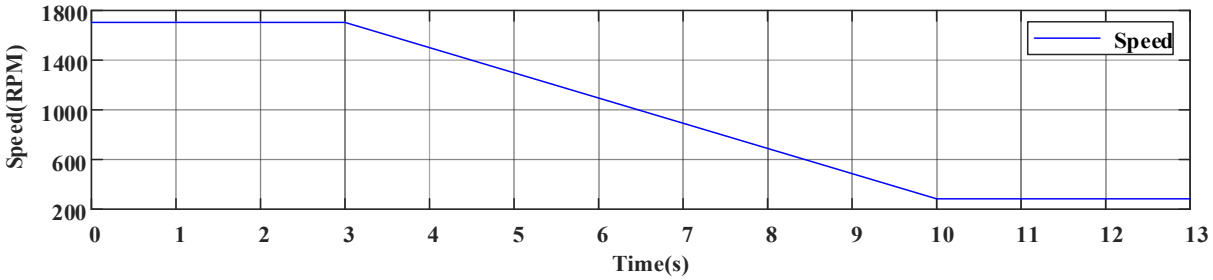
Fig. 4. 9 Performance of the Proposed Capacitor Reduction Controller

The dynamics of the voltage ripple controller is shown in Fig. 4.9(b). After it is activated at 1 second, the voltage ripple controller starts to inject the current component $\mathbf{i}_{\mathbf{r}1\_xi}$ to suppress the dc-link voltage ripple. With more current component $\mathbf{i}_{\mathbf{r}1\_xi}$ injected, the voltage ripple reduces accordingly. However, during the critical dynamics, the excess current is injected which prompts the voltage ripple to be less than 3%. To avoid excess ripple power injection, the proposed voltage controller reduces the output current amplitude of $\mathbf{i}_{\mathbf{r}1\_xi}$ forcing the operation point away from the unstable region if the dc voltage ripple goes to the near-zero region. This is verified in curves shown in Fig.4.9 (b).

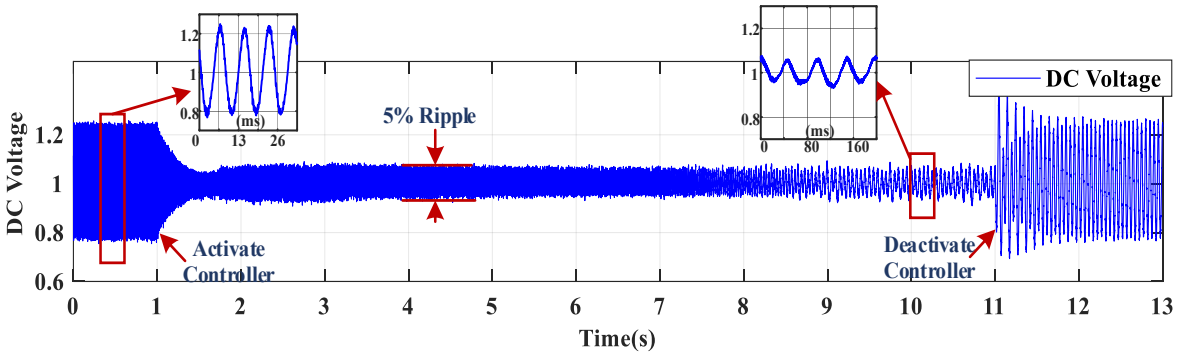
The phase angle of the injected current component $\mathbf{i}_{\mathbf{r}1\_xi}$ is derived from the dc voltage phase angle. The proposed adaptive filter can accurately extract the phase angle of the dc-link voltage ripple even under noise, which is shown in Fig. 4.9 (c) in steady-state. The simulation results for the cell secondary current and primary current waveforms are also shown in Fig. 4.9 (d) and (e) respectively. There are two current components $\mathbf{i}_{\mathbf{r}0\_xi}$ and $\mathbf{i}_{\mathbf{r}1\_xi}$ in the secondary current waveform in each cell. The injected $\mathbf{i}_{\mathbf{r}1\_xi}$ is a negative sequence current at 60Hz. The

$\mathbf{i}_{r1\_xi}$ current component in different cells cancels out at the primary side of the transformer, which is validated in Fig. 4.9 (e) that only the current component $\mathbf{i}_{r0\_xi}$ remains.

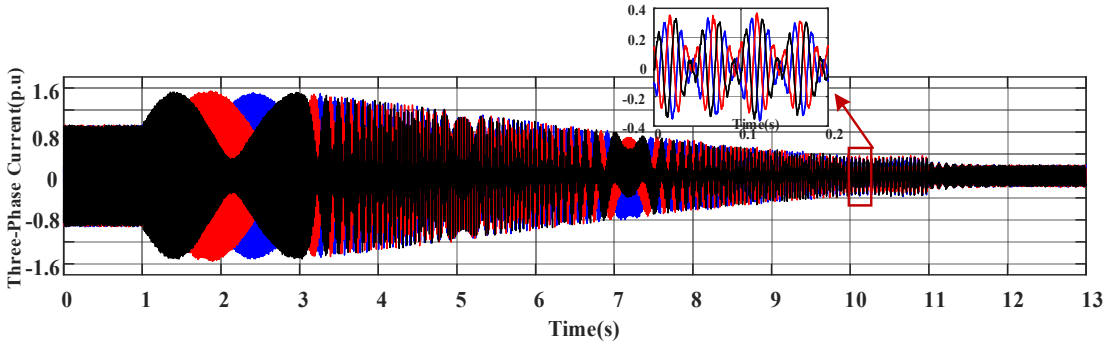
Moreover, as is illustrated before, the proposed voltage ripple control strategy can consider the frequency variation. The same regenerative CHB inverter is then tested on an induction motor operating with V/F controller. The dc-link voltage and secondary currents waveforms during the motor deceleration period are shown in Fig.4.10 (a) and (b). Before 1 s, the motor side



(a)Motor Speed



(b) DC Votlage Ripple



(c) Second Current in the power cell

Fig. 4. 10 Simulation Result with Frequency Variation

output frequency is operating at 60 Hz with a rated negative torque load without voltage ripple suppression. After that, the proposed voltage ripple controller is activated and then starts to inject the current component $\mathbf{i}_{r1\_xi}$ to suppress the dc-link voltage ripple to 5%. From 3 seconds to 10 seconds, the motor side output frequency changes from 60 Hz to 10 Hz. As shown in Fig. 4.10 (a), the dc ripple is restricted to 5% during the whole deceleration period with the injected

secondary currents shown in Fig. 4.10 (b). It is evident that the proposed voltage ripple control strategy is adaptive to the frequency variation.

As is shown in Fig. 4.10, the proposed voltage ripple controller is stabilized between 10 s to 11 s where the output frequency remains 10 Hz. After that, the proposed controller is deactivated at 11 s where a large dc-bus voltage ripple starts to appear. This matches the analysis as the dc voltage ripple becomes larger in the case of the very low output frequency.

4.5. Experiment Result

The proposed voltage ripple control strategy is further validated on a seven-level regenerative CHB prototype system with a cloud DSP controller, which is shown in Fig. 4.11. The prototype parameters for the experiment are shown in Table 4.2.

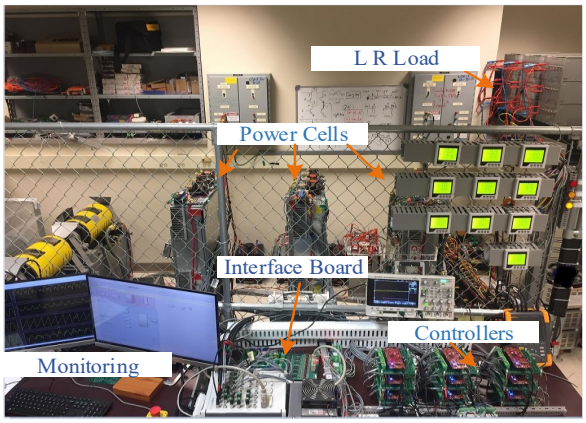
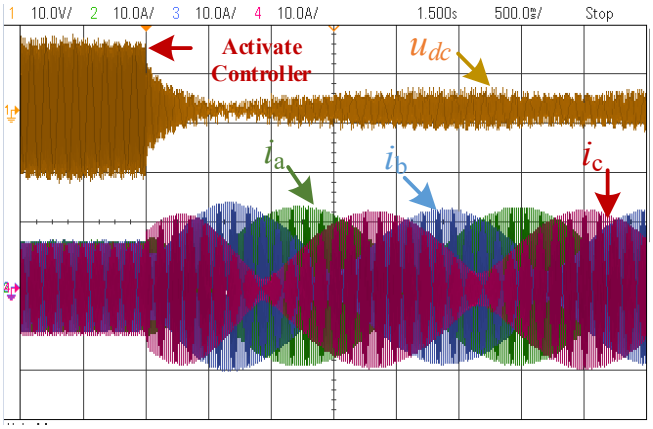


Fig. 4. 11 Prototype of the seven-level CHB system

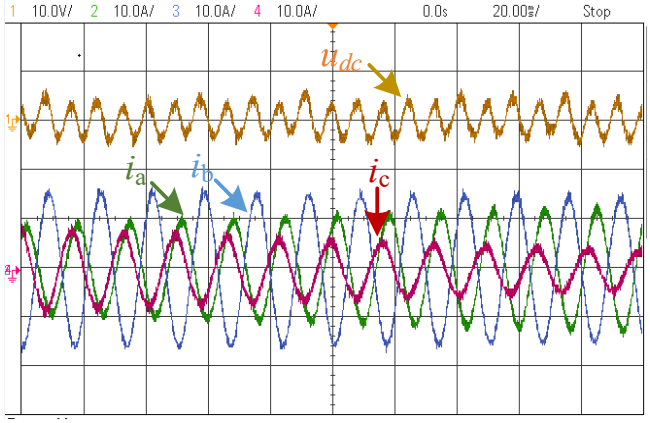
Table 4. 2 Seven-level CHB Prototype Parameters

Converter parameter	Value
Cell Average dc-link voltage	160 V
Transformer secondary side voltage	80 V
Grid-Tied Inductance	4 mH
Transformer primary side voltage	240 V
Transformer secondary side voltage	80 V
dc-Link Capacitance	500 μF

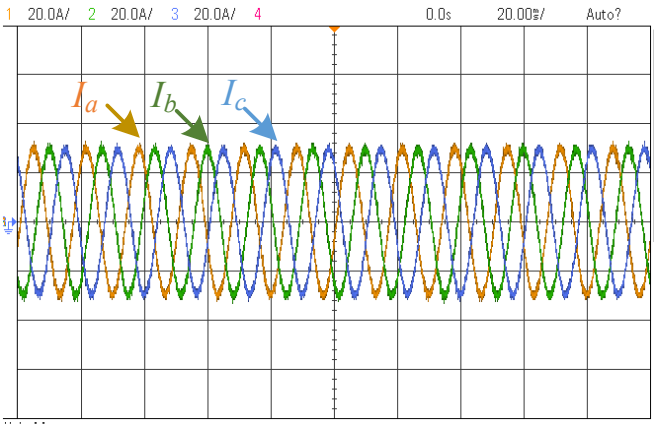
As it is shown in Fig. 4.12 (a), with a 500 μF dc-link capacitor, the power cell cannot maintain a low ripple dc-bus with the existence of a 28 V peak to peak voltage ripple due to instantaneous power unbalanced. After activating the proposed voltage ripple controller at t=1s, the voltage ripple is quickly decreased to 8V (5% referred to the average dc voltage 160 V) by injecting an extra current component. The AFE current waveforms are shown in Fig. 4.12 (a) and (b). There are two current components in the AFE input current: a 60 Hz positive sequence component to balance average dc-link voltage and a 60 Hz negative sequence current component to balance the instantaneous power across the dc-link capacitors. These experimental current waveforms match the simulation result shown in Fig. 4.10. The extra injected current component cancel out with each other between cells at the transformer primary side. This is understandable since the instantaneous power cancel with each other between cells in different phases of a regenerative CHB system. This is validated by the transformer primary side current waveforms shown in Fig. 4.12 (c) in a steady-state.



(a) Cell DC-link Voltage Ripple Dynamics



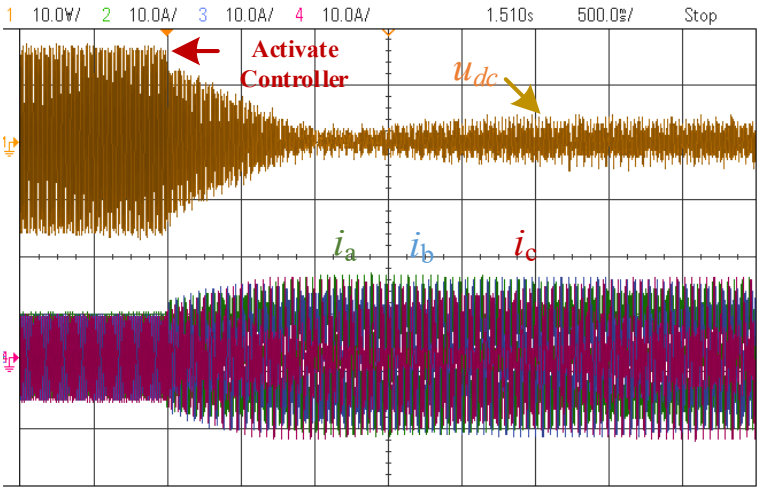
(b) Cell Output Currents



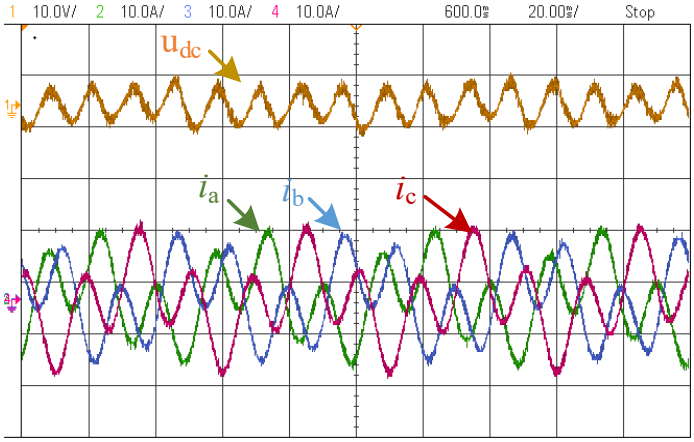
(c) Steady Transformer Primary Side Current

Fig. 4. 12 Experiments at 60 Hz load

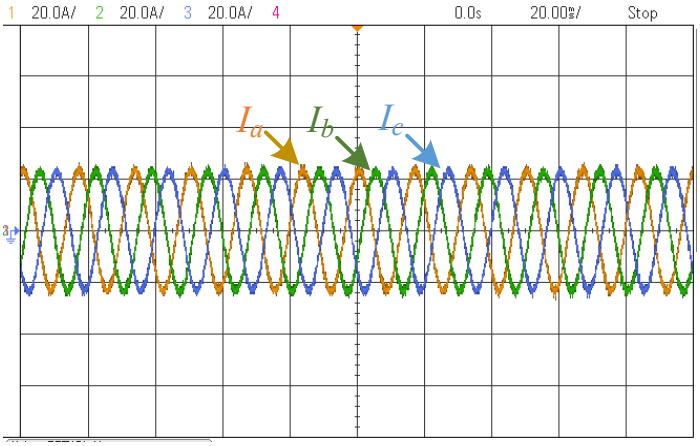
The adaptive filter strategy can extract the phase angle and amplitude from the dc-link voltage at different operating conditions. As is shown in Fig. 4.13, when the CHB output frequency is 40 Hz, the ripple reaches 30 V with a reduced load. After activating the proposed voltage ripple controller, the dc voltage ripple is reduced to under 5%. The dc-link voltage ripple and AFE currents are shown in Fig. 4.13 (b). The dc voltage ripple frequency is 80 Hz under 40 Hz output frequency. There are two current components in the AFE input current: a 60 Hz positive sequence component to balance average dc-link voltage and a 20 Hz negative sequence current component to balance the instantaneous power across the dc-link capacitors. As is shown in Fig. 4.13 (c), the 20 Hz negative sequence current components cancel out between different cells at the transformer primary side. The proposed control scheme is adaptive to the change of output frequency variation.



(a) Cell DC-link Voltage Ripple Dynamics



(b) Cell Output Currents



(c) Steady Transformer Primary Side Current

Fig. 4. 13 Experiments at 40 Hz load

4.6. Discussion

A critical issue for the voltage ripple controller is that the system may even lose stability when an excess pulsating power ripple is injected. The simulation result with the conventional PI voltage ripple controller instead of the proposed voltage controller under 60 Hz load frequency is shown in Fig. 4.14. The system loses stability in the transient state due to excess pulsating ripple power injection such that the measured dc voltage ripple phase angle $Arg\angle\tilde{u}_{dc}$ is shifted 180 degrees. With the new measured phase-shifted angle flipped, the calculated current component

i_{rl_xi} will inversely tend to increase the voltage ripple. This can be seen in Fig. 4.14 where the dc voltage ripple is even larger than the case without a voltage ripple controller. The system loses stability with the conventional PI voltage controller.

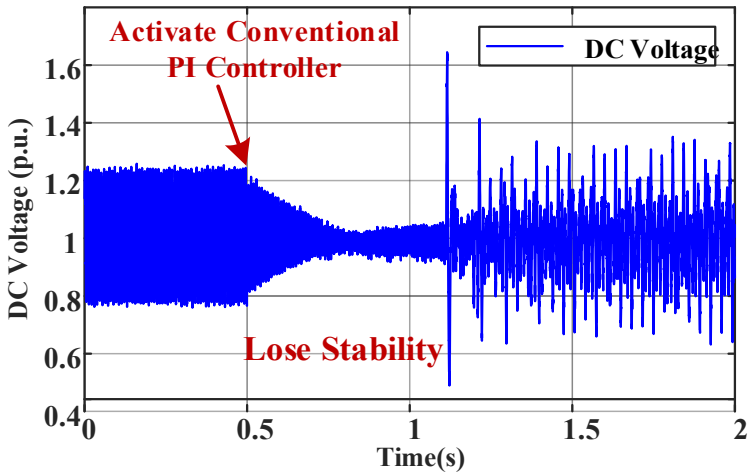


Fig. 4. 14 Performance Under Conventional PI Controller

4.7. **Conclusion**

Due to the unbalanced instantaneous power flow, an oversized dc-link capacitor is required in each power cell to achieve a stable dc-link voltage in the regenerative CHB drives. To reduce the dc-link capacitance, this paper proposes a novel closed-loop ripple voltage controller for the regenerative CHB drive without adding extra sensors. The dc-bus voltage ripple amplitude and phase angle are accurately detected with a high-performance adaptive filter. Moreover, a latent instability issue is pointed out and is avoided in the proposed controller.

The proposed capacitance reduction strategy is validated on a seven-level regenerative CHB drive with good steady and dynamic performance. It was verified that the dc capacitance can be reduced to less than 25% of its original design while a 5% dc voltage ripple is allowed.

This value further decreases to 15% when a 3% voltage ripple is allowed in the system. Therefore, the size and cost of the cell can be greatly reduced, while the lifetime and reliability of the motor drive are improved.

Chapter 5

A Novel High-Performance Predictive Control Formulation for CHB Drives

5.1. Introduction

Multilevel inverters are the preferred choice for medium-voltage (MV) applications due to the advantages of high power quality waveforms, low electromagnetic compatibility concerns, and high-voltage capability. To achieve a faster dynamic response and the multi-objective performance during the control of power converters, the finite control set model predictive control (FCS-MPC) method has been considered one of the most promising alternatives in recent years.

However, to implement FCS-MPC on CHB drives, there are several challenges to be improved such as 1) reduction of the computational loads on microcontrollers, 2) the extension to long prediction horizons, 3) satisfaction of multi-objective simultaneously such as output

current control, common-mode voltage (CMV) suppression, and 4) design of weighting factors and cost function. To address the aforementioned problems, this chapter proposes a novel high-performance MPC formulation with a long horizon prediction length extension. In the proposed method, the FCS-MPC is reformulated mathematically to an l^2 norm optimization problem and is then solved through matrix theory. The contribution of this chapter is summarized by substantiating the following statements. First, the FCS-MPC problem is solved in a computationally efficient way by adopting the proposed novel MPC matrix formulation. Performance can be assured through the proposed MPC formulation with less computation burden. Second, CMV can be reduced without the need for any cost functions or weighting factors. This can result in a simplified MPC design process without tuning the weighting factors which is essential for the cost-function-based MPC formulation.

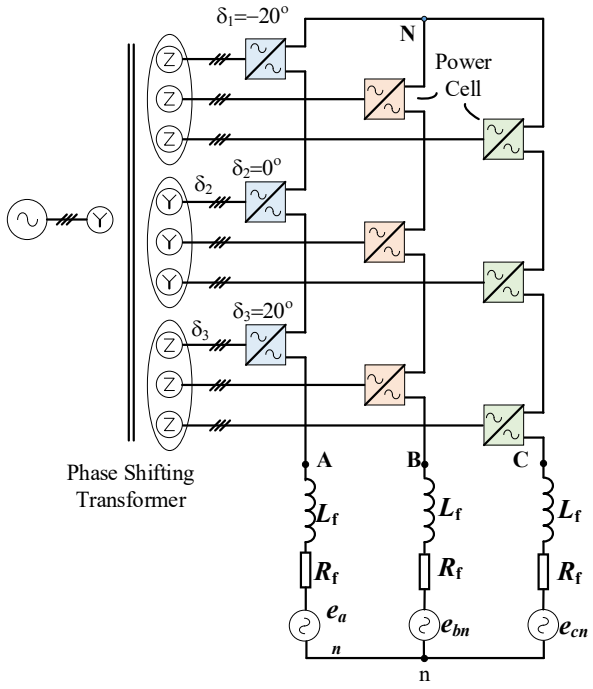
In this chapter, the proposed algorithm is implemented on a seven-level CHB inverter as shown in Fig. 5.1. A CHB inverter is composed of a number of modular H-bridge power cells and isolated DC voltage sources. The H-bridge cells are cascaded on the load side to achieve medium-voltage with low harmonic distortion. Due to its structure, the CHB inverter is known to have a huge number of switching combinations and voltage vectors. For a 2C+1 level CHB inverter, the number of non-redundancy voltage vectors will boost up to $12C^2+6C+1$. which poses a challenge for implementing the online FCS-MPC algorithm at a high performance! In this chapter, the performance of the proposed method is evaluated experimentally on a seven-level CHB inverter.

The remainder of this chapter is organized as follows. Section 5.2 describes the cost function based FCS-MPC for a seven-level CHB inverter. Section 5.3 presents a new fast high-performance FCS-MPC scheme for multilevel inverters to reduce the real-time computational

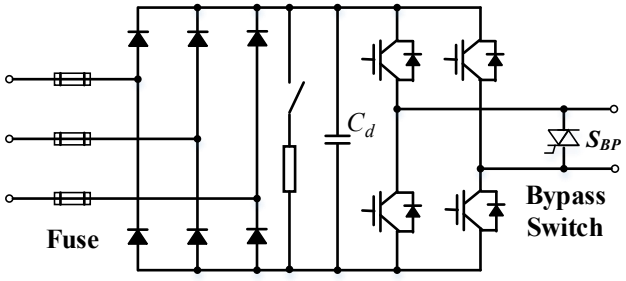
burden with suppressed CMV without cost functions. In section 5.4, the proposed FCS-MPC formulation is validated experimentally on a seven-level CHB inverter. Conclusions are provided in Section 5.5.

5.2. Cost Function Based FCS-MPC for a Seven-level CHB Inverter

Fig. 5.1 shows the schematic of a three-phase star-connected seven-level CHB inverter system.



(a) A Seven-Level CHB Motor Drive



(b) Power Cell

Fig. 5. 1 Diode-Front-End Seven-Level CHB Inverter

In each power cell, there are four switching devices and one DC-link capacitor. The output voltage of each cell can be denoted as an integer variable $s_{(a,b,c)i} \in (-1,0,1)$, where -1, 0, 1 represents three output voltages positive DC voltage, zero and negative DC voltage, respectively. The subscript *i* indicates the order of the cascaded H-bridge cells, i.e, $i = 1, 2, 3$ for a seven-level CHB inverter.

5.2.1. Discrete Model of a Seven-level CHB Inverter

In a CHB inverter, output phase voltage with respect to neutral point *N*, $v_{(a,b,c)N}$, is the summation of the output voltage of all the cells located in that phase and can be expressed as equation (5.1):

$$v_{(a,b,c)N} = \sum_{i=1}^{n} s_{(a,b,c)i} V_{dc} \tag{5.1}$$

where

$$s_{(a,b,c)i} \in (-1,0,1)$$

V_{dc} is the dc-link voltage of each cell. The output phase $v_{(a,b,c)N}$, is an integer value and bounded within [$-nV_{\mathrm{dc}}$, nV_{dc}] based on the applicable switching states.

Using Kirchhoff's voltage law at the output of the CHB inverter, the load current model in the *continuous-time* domain is given as:

$$L_f \frac{d\mathbf{i}_{\mathbf{a,b,c}}}{dt} + R_f \mathbf{i}_{\mathbf{a,b,c}} + \mathbf{e}_{\mathbf{abcn}} = \mathbf{v}_{\mathbf{(a,b,c)N}} + v_{Nn} \tag{5.2}$$

where L_f and R_f represent the phase inductance and resistance of the load, and the current and output phase voltage vectors are:

$$\mathbf{i}_{\mathbf{a,b,c}} = \begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^T$$

$$\mathbf{v}_{(\mathbf{a,b,c})N} = \begin{bmatrix} V_{aN} & V_{bN} & V_{cN} \end{bmatrix}^T$$

$\mathbf{e_{abcn}}$ is the back electromotive force (EMF) of the motor, which can be estimated from the motor observer:

$$\mathbf{e}_{\mathbf{abcn}} = \begin{bmatrix} e_{an} & e_{bn} & e_{cn} \end{bmatrix}^T$$

and v_{Nn} is the common-mode voltage and denoted as the voltage between the inverter neutral point, *N*, and load neutral point *n*. Equation (5.2) can be rewritten as:

$$\begin{bmatrix} \frac{di_a}{dt} \\ \frac{di_b}{dt} \\ \frac{di_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & & \\ & -\frac{R_f}{L_f} & \\ & & -\frac{R_f}{L_f} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{1}{L_f} \begin{bmatrix} V_{aN} - e_{an} \\ V_{bN} - e_{bn} \\ V_{cN} - e_{cn} \end{bmatrix} + \frac{1}{L_f} v_{Nn} \tag{5.3}$$

The CMV is given by (5.4), which holds for a balanced three-phase three-wire system where $i_a + i_b + i_c = 0$:

$$v_{Nn} = -\frac{1}{3}(v_{aN} + v_{bN} + v_{cN}) \tag{5.4}$$

Substitute equation (5.4) in (5.3), the state-space model for the CHB converter is further simplified as (5.5):

$$\begin{bmatrix} \frac{di_a}{dt} \\ \frac{di_b}{dt} \\ \frac{di_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & & \\ & -\frac{R_f}{L_f} & \\ & & -\frac{R_f}{L_f} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{1}{3L_f} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{bmatrix} - \frac{1}{L_f} \begin{bmatrix} e_{an} \\ e_{bn} \\ e_{cn} \end{bmatrix} \tag{5.5}$$

The essence of MPC controller is to predict the behavior of the system for each possible output voltage vector. The prediction of the load current vector depends on the discrete mathematical model of the converter. From the Euler approximation, the continuous state-space model (5.5) of the CHB converter, can be expressed in the *discrete-time* domain and results in:

$$\mathbf{i_{a,b,c}}(k+1) = \mathbf{A}\mathbf{i_{a,b,c}}(k) + \mathbf{B}\mathbf{v}_{(\mathbf{a,b,c})N}(k) + \mathbf{C}\mathbf{e_{abcn}}(k) \tag{5.6}$$

where T_s is the sampling period and

$$\mathbf{A} = diag\left[1-\frac{T_s R_f}{L_f} \quad 1-\frac{T_s R_f}{L_f} \quad 1-\frac{T_s R_f}{L_f}\right]$$

$$\mathbf{B} = \frac{T_s}{3L_f}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \quad \mathbf{C} = -\frac{1}{L_f}$$

5.2.2. Cost Function Based FCS-MPC Formulations

The cost function-based FCS-MPC strategy is formulated to consider multi-objective over single-step prediction horizon based on the system *discrete-time* model. If the load current

tracking performance is considered, then the control target is to minimize the error between the predicted load currents $\mathbf{i}_{\mathbf{a,b,c}}(k+1)$and their references $\mathbf{i}^*_{\mathbf{a,b,c}}(k+1)$ at k+1 time step. In this case, the current tracking cost function is shown in equation (5.7):

$$J_1 = \left\| \mathbf{i}^*_{\mathbf{a,b,c}}(k+1) - \mathbf{i}_{\mathbf{a,b,c}}(k+1) \right\|_2 \tag{5.7}$$

The cost function can be extended for an arbitrary prediction horizon m as shown in (5.8). The selection of the output voltage vector at k time interval should consider the current tracking trajectory of future time steps from k+1 to k+m. Thus, the long horizon prediction length MPC cost function becomes:

$$J_2 = \sum_{p=1}^{m} \left\| \mathbf{i}^*_{\mathbf{a,b,c}}(k+p) - \mathbf{i}_{\mathbf{a,b,c}}(k+p) \right\|_2 \tag{5.8}$$

The CMV can be suppressed by formulating the multiobjective control problem in the *abc* framework. The importance of the CMV suppression can be substantiated together with the main objective of load current track by the weighting factor λ_p. The multiobjective MPC cost function with m prediction step length is described in (5.9).

$$J_3 = \sum_{p=1}^{m} \left(\left\| \mathbf{i}^*_{\mathbf{a,b,c}}(k+p) - \mathbf{i}_{\mathbf{a,b,c}}(k+p) \right\|_2 + \lambda_p \left| v_{Nn}(k+p) \right| \right) \tag{5.9}$$

The first part of the cost function is related to the current tracking performance. The second part is involved with the CMV suppression.

From equation (5.6) and (5.9), the multiobjective long prediction horizon FCS-MPC is mathematically formulated to an optimization problem that real-time finds out the optimal output voltage vector at each time step that assures the minimum cost function value. However, since the

multilevel inverters have a huge amount of voltage levels and redundancies, a huge number of calculations need to be done to find the best output voltage vector that minimizes the cost function. For example, a seven-level CHB inverter 7^3 (343) output voltage vectors, and 127 nonredundancy voltage vectors for only one single-step prediction. It requires lots of computations to find out the optimal output voltage vector at each sampling step. Therefore, when it comes to implementation, it requires a very powerful microcontroller to take care of all these calculations in real-time. If the number of levels or the number of voltage level increase, this might be impossible to implement in a real-time controller. Beyond that, if the long prediction horizon FCS-MPC (prediction length m>1) is required to achieve a balanced sinusoidal current with a reduced CMV by minimizing equation (5.9), the number of calculations increases significantly compared with a single-step prediction horizon FCS-MPC.

To overcome the illustrated shortcomings of the cost function based FCS-MPC algorithm, some existing methods have been studied, such as modified SDA MPC formulation, MPDCC and hierarchy MPC formulation. The modified SDA MPC formulation and MPDCC formulation can alleviate the real-time computation burden efficiently. But choosing the weighting factors influences the system performance, which decreases the system reliability. On the other hand, hierarchy MPC formulation can eliminate weighting factors while achieving multi-objectives. However, the computational load is still high with long horizon prediction length MPC. In this chapter, a new MPC formulation is proposed to further reduce the real-time computation load without the need for the weighting factors or cost functions, which further simplifies the MPC control implementation.

5.3. Proposed Fast High-performance FCS-MPC Formulation

Instead of estimating all the possible voltage vectors at each sampling step, the essence of the proposed FCS-MPC method is to directly calculate the optimal output voltage vector that best tracks the reference currents while keeping CMV minimum. By doing so, even though a huge number of the voltage vectors exist with the increasing of the inverter voltage levels, the optimization process and computation burden of the proposed MPC method will not increase. This features the proposed method especially suitable for multilevel inverters with high voltage levels.

5.3.1. Reference Current Prediction

To start with the MPC scheme, the future current reference vector $\mathbf{i}^*_{\mathbf{a,b,c}}$ is required to be predicted at different time steps. The future current references can be obtained through the linear prediction (extrapolation) method or rotating prediction method. The current reference vector $\mathbf{i}^*_{\mathbf{a,b,c}}(k+m)$ at any k+m time-step can be predicted based on the $\mathbf{i}^*_{\mathbf{a,b,c}}(k)$ with the following equation:

$$\begin{aligned}\begin{bmatrix} i_a^*(k+l) \\ i_b^*(k+l) \\ i_c^*(k+l) \end{bmatrix} &= R_{\alpha\beta-abc}\begin{bmatrix} \cos(\omega m T_s) & \sin(\omega m T_s) \\ -\sin(\omega m T_s) & \cos(\omega m T_s) \end{bmatrix} R_{abc-\alpha\beta}\begin{bmatrix} i_a^*(k) \\ i_b^*(k) \\ i_c^*(k) \end{bmatrix} \\ &= \frac{2}{3}\begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} \cos(\omega m T_s) & \sin(\omega m T_s) \\ -\sin(\omega m T_s) & \cos(\omega m T_s) \end{bmatrix}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} i_a^*(k) \\ i_b^*(k) \\ i_c^*(k) \end{bmatrix}\end{aligned} \tag{5.10}$$

where T_s is the sampling step, ω is the reference current frequency and m is the prediction length.

5.3.2. Proposed formulation for single-step prediction MPC

With a single-step MPC method, the current vector $\mathbf{i}_{\mathbf{a,b,c}}(k+1)$ is required to be repetitively estimated through equation (5.6) among all possible voltage vectors. The essence of the proposed MPC controller is to achieve the reference current tracking by directly calculating the optimal output voltage vector as follow:

First, Eq. (5.6) can be written as:

$$\begin{bmatrix} i_a(k+1) \\ i_b(k+1) \\ i_c(k+1) \end{bmatrix} = \begin{bmatrix} 1-\frac{T_s R_f}{L_f} & & \\ & 1-\frac{T_s R_f}{L_f} & \\ & & 1-\frac{T_s R_f}{L_f} \end{bmatrix} \begin{bmatrix} i_a(k) \\ i_b(k) \\ i_c(k) \end{bmatrix} + \frac{T_s}{3L_f} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{aN}(k) \\ v_{bN}(k) \\ v_{cN}(k) \end{bmatrix} - \frac{T_s}{L_f} \begin{bmatrix} e_{an} \\ e_{bn} \\ e_{cn} \end{bmatrix} \quad (5.11)$$

(5.11) can be rewritten as:

$$\frac{T_s}{3L_f} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{aN}(k) \\ v_{bN}(k) \\ v_{cN}(k) \end{bmatrix} = \begin{bmatrix} i_a(k+1) \\ i_b(k+1) \\ i_c(k+1) \end{bmatrix} - \begin{bmatrix} 1-\frac{T_s R_f}{L_f} & & \\ & 1-\frac{T_s R_f}{L_f} & \\ & & 1-\frac{T_s R_f}{L_f} \end{bmatrix} \begin{bmatrix} i_a(k) \\ i_b(k) \\ i_c(k) \end{bmatrix} - \frac{T_s}{L_f} \begin{bmatrix} e_{an} \\ e_{bn} \\ e_{cn} \end{bmatrix} \quad (5.12)$$

Assume the output current at k+1 is equal to the reference current, which indicates that $\mathbf{i}_{\mathbf{a,b,c}}(k+1)=\mathbf{i}^{*}_{\mathbf{a,b,c}}(k+1)$. The optimal output voltage vector $\mathbf{v}^{*}_{(\mathbf{a,b,c})N}$, at k time step should be calculated as the following equation:

$$\frac{T_s}{3L_f}\begin{bmatrix}2&-1&-1\\-1&2&-1\\-1&-1&2\end{bmatrix}\begin{bmatrix}v^{*}_{aN}(k)\\v^{*}_{bN}(k)\\v^{*}_{cN}(k)\end{bmatrix}=\begin{bmatrix}i^{*}_{a}(k+1)\\i^{*}_{b}(k+1)\\i^{*}_{c}(k+1)\end{bmatrix}-\begin{bmatrix}1-\frac{T_sR_f}{L_f}&&\\&1-\frac{T_sR_f}{L_f}&\\&&1-\frac{T_sR_f}{L_f}\end{bmatrix}\begin{bmatrix}i_a(k)\\i_b(k)\\i_c(k)\end{bmatrix}-\frac{T_s}{L_f}\begin{bmatrix}e_{an}\\e_{bn}\\e_{cn}\end{bmatrix} \quad (5.13)$$

If the inverter optimal output voltage vector $\mathbf{v}^{*}_{(\mathbf{a,b,c})N}(k)$ at time step k satisfies equation (5.13), the load currents at k+1 step will be exactly equal to the reference current at k+1 sampling time interval ($\mathbf{i}_{\mathbf{a,b,c}}(k+1)=\mathbf{i}^{*}_{\mathbf{a,b,c}}(k+1)$). However, as is shown in equation (5.13), the rank of the matrix $\begin{bmatrix}2&-1&-1\\-1&2&-1\\-1&-1&2\end{bmatrix}$ is 2, which means that only two out of three equations in (5.13) are independent. Since only two equations contain valid information, the last row equation is removed and the equation (5.13) can be simplified as:

$$\frac{T_s}{3L_f}\begin{bmatrix}2&-1&-1\\-1&2&-1\end{bmatrix}\begin{bmatrix}v^{*}_{aN}(k)\\v^{*}_{bN}(k)\\v^{*}_{cN}(k)\end{bmatrix}=\begin{bmatrix}i^{*}_{a}(k+1)\\i^{*}_{b}(k+1)\end{bmatrix}-\begin{bmatrix}1-\frac{T_sR_f}{L_f}&\\&1-\frac{T_sR_f}{L_f}\end{bmatrix}\begin{bmatrix}i_a(k)\\i_b(k)\end{bmatrix}-\frac{T_s}{L_f}\begin{bmatrix}e_a(k)\\e_b(k)\end{bmatrix} \quad (5.14)$$

Another objective is to find the optimal output voltage vector to make CMV zero, which means:

$$v_{Nn}(k)=-\tfrac{1}{3}\left(v^{*}_{aN}(k)+v^{*}_{bN}(k)+v^{*}_{cN}(k)\right)=0 \quad (5.15)$$

To integrate CMV control in the MPC formulation, the equation (5.14) can be extended to (5.16) by adding equation (5.15) in the last row, which becomes:

$$\frac{T_s}{3L_f}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} v_{aN}^*(k) \\ v_{bN}^*(k) \\ v_{cN}^*(k) \end{bmatrix} = \begin{bmatrix} i_a^*(k+1) \\ i_b^*(k+1) \\ 0 \end{bmatrix} - \begin{bmatrix} 1-\frac{T_s R_f}{L_f} & & \\ & 1-\frac{T_s R_f}{L_f} & \\ & & 0 \end{bmatrix}\begin{bmatrix} i_a(k) \\ i_b(k) \\ i_c(k) \end{bmatrix} - \frac{T_s}{L_f}\begin{bmatrix} e_a(k) \\ e_b(k) \\ 0 \end{bmatrix} \tag{5.16}$$

(5.16) can be rewritten as:

$$\frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} v_{aN}^*(k) \\ v_{bN}^*(k) \\ v_{cN}^*(k) \end{bmatrix} = \frac{L_f}{T_s}\begin{bmatrix} i_a^*(k+1) \\ i_b^*(k+1) \\ 0 \end{bmatrix} - (\frac{L_f}{T_s} - R_f)\begin{bmatrix} i_a(k) \\ i_b(k) \\ 0 \end{bmatrix} - \begin{bmatrix} e_a(k) \\ e_b(k) \\ 0 \end{bmatrix} \tag{5.17}$$

or

$$\mathbf{T}\begin{bmatrix} v_{aN}^*(k) \\ v_{bN}^*(k) \\ v_{cN}^*(k) \end{bmatrix} = \mathbf{b_1}$$

where

$$\mathbf{T} \triangleq \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ 1 & 1 & 1 \end{bmatrix} \tag{5.18}$$

$$\mathbf{b}_1 \triangleq \frac{L_f}{T_s}\begin{bmatrix} i_a^*(k+1) \\ i_b^*(k+1) \\ 0 \end{bmatrix} - (\frac{L_f}{T_s} - R_f)\begin{bmatrix} i_a(k) \\ i_b(k) \\ 0 \end{bmatrix} - \begin{bmatrix} e_a(k) \\ e_b(k) \\ 0 \end{bmatrix}$$

It can be seen that the rank of constant matrix **T** is 3. If optimal output voltage vector $\mathbf{v}^*_{(\mathbf{a,b,c})N}(k)$ is calculated to satisfy equation (5.18), therefore the current at *k*+1 step exactly will be equal to the reference current while the CMV is set to equal to zero.

As the current reference vector $\mathbf{i}^*_{\mathbf{a,b,c}}(k+1)$ at *k*+1 can be calculated through equation (5.10) and $\mathbf{i}_{\mathbf{a,b,c}}(k)$ is the measured load current at *k* time step, back EMF can be estimator out in the motor control, $\mathbf{b}_1$ is a known vector.

Finally, the optimal voltage vector, $\mathbf{v}^*_{(\mathbf{a,b,c})N}(k)$, can be directly calculated out through equation (5.18) for single-step prediction.

5.3.3. Proposed Formulation for *m*-step Prediction MPC

A similar process can be applied for a long prediction time step. For any prediction time-step *m*, the reference current vector at any time step *k*+*m* (*m* is the prediction length) can be acquired through equation (5.10).

Eq. (5.17) can be revised to consider the current tracking problem which is $\mathbf{i}_{\mathbf{a,b,c}}(k+m)=\mathbf{i}^*_{\mathbf{a,b,c}}(k+m)$ and considering CMV to zero. This results in Eq. (5.19) to calculate the optimal voltage vector $\mathbf{v}^*_{(\mathbf{a,b,c})N}(k)$ at time *k*.

$$\frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} v^*_{aN}(k) \\ v^*_{bN}(k) \\ v^*_{cN}(k) \end{bmatrix} = \frac{L_f}{mT_s}\begin{bmatrix} i^*_a(k+m) \\ i^*_b(k+m) \\ 0 \end{bmatrix} - \left(\frac{L_f}{mT_s} - R_f\right)\begin{bmatrix} i_a(k) \\ i_b(k) \\ 0 \end{bmatrix} - \begin{bmatrix} e_a(k) \\ e_b(k) \\ 0 \end{bmatrix} \tag{5.19}$$

Eq. (5.19) can be rewritten as:

$$\mathbf{T}\begin{bmatrix} v_{aN}^{*}(k) \\ v_{bN}^{*}(k) \\ v_{cN}^{*}(k) \end{bmatrix} = \mathbf{b}_l$$

(5.20)

Where

$$\mathbf{T} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ 1 & 1 & 1 \end{bmatrix} \qquad \mathbf{b}_l \triangleq \frac{L_f}{mT_s}\begin{bmatrix} i_a^{*}(k+m) \\ i_b^{*}(k+m) \\ 0 \end{bmatrix} - \left(\frac{L_f}{mT_s} - R_f\right)\begin{bmatrix} i_a(k) \\ i_b(k) \\ 0 \end{bmatrix} - \begin{bmatrix} e_a(k) \\ e_b(k) \\ 0 \end{bmatrix}$$

In order to calculate the optimal voltage vector for *m*-step horizon, the following equations should be solved:

$$\mathbf{T}\begin{bmatrix} v_{aN}^{*}(k) \\ v_{bN}^{*}(k) \\ v_{cN}^{*}(k) \end{bmatrix} = \mathbf{b}_p \tag{5.21}$$

for p=1,2,3,,..., m

For long prediction horizon MPC, it is not possible to find an optimal voltage vector to satisfy (5.21). This is because there are more constraint equations than the state variables.

To obtain the optimal voltage vector for long-horizon prediction, the matrix solution can be converted to a l^2 norm optimization problem which finds the desired optimal output voltage vector $\mathbf{v}_{(\mathbf{a},\mathbf{b},\mathbf{c})N}^{*} = [v_{aN}^{*}\ v_{bN}^{*}\ v_{cN}^{*}]^{\mathrm{T}}$ to minimizes the l^2 norm of the tracking errors. This is shown in equation (5.22).

$$\text{Min} \left\| \begin{bmatrix} \mathbf{T} \\ \mathbf{T} \\ \dots \\ \mathbf{T} \end{bmatrix} \begin{bmatrix} v_{aN}^{*}(k) \\ v_{bN}^{*}(k) \\ v_{cN}^{*}(k) \end{bmatrix} - \begin{bmatrix} \mathbf{b}_1 \\ \mathbf{b}_2 \\ \dots \\ \mathbf{b}_m \end{bmatrix} \right\|_2 \tag{5.22}$$

To solve the optimization problem formulated in (5.22) for the proposed reformulated long prediction horizon FCS-MPC with suppressed CMV, the least-square solution can be obtained through equation (5.23). The details of the least-square solution could be found in reference [118].

$$\begin{bmatrix} v_{aN}^{*}(k) \\ v_{bN}^{*}(k) \\ v_{cN}^{*}(k) \end{bmatrix} = \left(\begin{bmatrix} \mathbf{T} \\ \mathbf{T} \\ \dots \\ \mathbf{T} \end{bmatrix}^{T} \begin{bmatrix} \mathbf{T} \\ \mathbf{T} \\ \dots \\ \mathbf{T} \end{bmatrix} \right)^{-1} \begin{bmatrix} \mathbf{T} \\ \mathbf{T} \\ \dots \\ \mathbf{T} \end{bmatrix}^{T} \begin{bmatrix} \mathbf{b}_1 \\ \mathbf{b}_2 \\ \dots \\ \mathbf{b}_l \end{bmatrix} = \boldsymbol{\Psi} \begin{bmatrix} \mathbf{b}_1 \\ \mathbf{b}_2 \\ \dots \\ \mathbf{b}_l \end{bmatrix} \tag{5.23}$$

Where

$$\boldsymbol{\Psi} = \left(\begin{bmatrix} \mathbf{T} \\ \mathbf{T} \\ \dots \\ \mathbf{T} \end{bmatrix}^{T} \begin{bmatrix} \mathbf{T} \\ \mathbf{T} \\ \dots \\ \mathbf{T} \end{bmatrix} \right)^{-1} \begin{bmatrix} \mathbf{T} \\ \mathbf{T} \\ \dots \\ \mathbf{T} \end{bmatrix}^{T} \tag{5.24}$$

The matrix $\boldsymbol{\Psi}$ is a constant matrix and can be calculated off-line and stored in the memory to alleviate the real-time computation burden. For example, for the proposed MPC formulation with the prediction length m, the $\boldsymbol{\Psi}$ is only a $3\times 3m$ matrix. The optimal voltage vector can be directly obtained through equation (5.23). Both the current tracking performance and the CMV reduction is guaranteed with the calculated optimal voltage vector.

Even though the optimal voltage vector is now calculated through equation (5.23), however, it is not necessary that the calculated desired optimal voltage vector is an integer within the inverter's maximum output ability. The normalization process shown in (5.25) is required when the calculated optimal vector is a non-integer or out of the inverter's maximum output voltage.

$$\begin{bmatrix} v_{aN}(k) \\ v_{bN}(k) \\ v_{cN}(k) \end{bmatrix} = \begin{cases} round(\mathbf{v}^*_{(\mathbf{a},\mathbf{b},\mathbf{c})N} / V_{dc}) & if \left\| \mathbf{v}^*_{(\mathbf{a},\mathbf{b},\mathbf{c})N} \right\|_\infty \le nV_{dc} \\ round(n \dfrac{\mathbf{v}^*_{(\mathbf{a},\mathbf{b},\mathbf{c})N}}{\left\| \mathbf{v}^*_{(\mathbf{a},\mathbf{b},\mathbf{c})N} \right\|_\infty} V_{dc}) & if \left\| \mathbf{v}^*_{(\mathbf{a},\mathbf{b},\mathbf{c})N} \right\|_\infty > nV_{dc} \end{cases} \tag{5.25}$$

If the calculated optimal output voltage vector infinity norm is within the inverter output ability nV_{dc}. The *round* function is used to find the nearest voltage level of the optimal output voltage vector $\mathbf{v}^*_{(\mathbf{a},\mathbf{b},\mathbf{c})N}(k)$ as the output voltage vector $\mathbf{v}_{(\mathbf{a},\mathbf{b},\mathbf{c})N}(k)$. On the other hand, when the optimal output voltage vector infinity norm is higher than the inverter output range. The optimal output voltage needs to be normalized to nV_{dc} first and then use the round function to find out the nearest output voltage levels.

As can be seen, instead of estimating all the possible voltage vectors at each sampling step, the proposed FCS-MPC method directly calculated the optimal output voltage vector to best track the reference currents while keeping CMV minimum. Unlike the existing MPC methods, the cost function and weighing factors are eliminated in the optimization process. The MPC designed process is thus simplified with more reliability. The computation efficiency is improved greatly, which makes it possible for long-horizon prediction in the multilevel inverter with high voltage levels.

5.4. Simulation Results

The feasibility of the proposed fast FCS-MPC method is evaluated on a seven-level CHB inverter through simulations in this section. To begin with, the proposed FCS-MPC algorithm is first implemented with the RL load to demonstrate the dynamic performance. Beyond that, the proposed FCS-MPC is then implemented with an interior permanent magnet motor (IPM). The speed controller sets the reference currents for the IPM. The proposed FCS-MPC controller is designed to track the reference currents prescribed by the previous speed controller. The effectiveness of the proposed FCS-MPC is validated on the IPM, which can be extended to other types of motors. The prediction length l is selected to be 3 for the simulations.

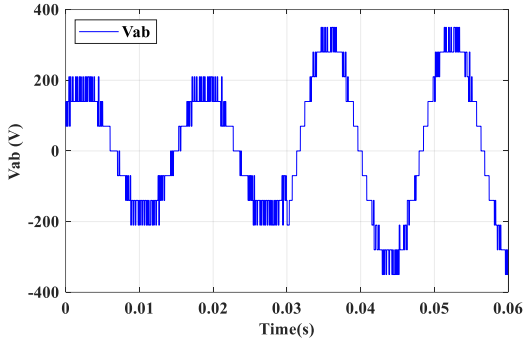
The feasibility of the proposed fast FCS-MPC method is evaluated through the simulation on a seven-level CHB inverter. The DC voltage of each CHB cell remains 70 V during the operation. The inverter output inductance and resistance is 5 mH and 13 Ω respectively. The sampling time of the MPC controller is 100 us. The prediction length l is selected to be 3. The system main parameter are shown in Table 5.1.

Table 5. 1 Seven-level CHB Prototype Parameters for Experiment

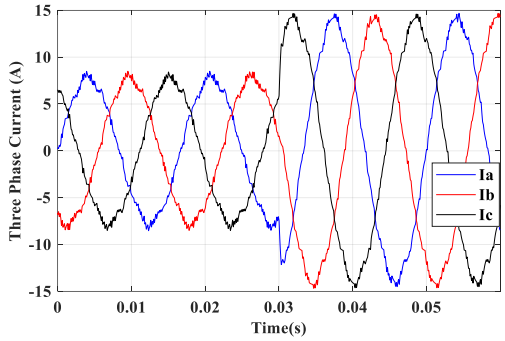
Converter parameter	Value
Cell DC-link voltage (V)	70
Load Inductance L_f (mH)	5
Load Resistor (Ω)	13

The MPC controller is designed through the previous matrix formulation. The current tracking performance of the proposed FCS-MPC is validated in this section by setting the reference currents amplitude and frequency. Beyond that, the CMV performance of the proposed multistep FCS-MPC is also studied.

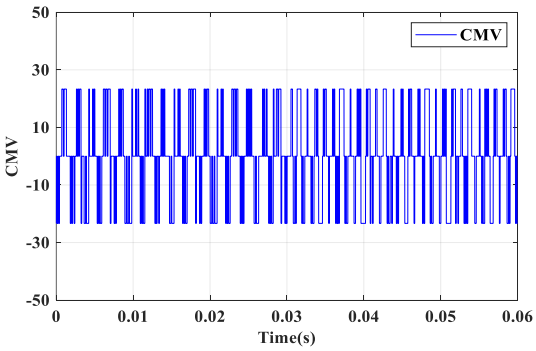
Fig. 5.2 shows the dynamic performance of the proposed MPC formulation under the reference load currents amplitude stepping up. Initially, the inverter output peak current is controlled at 8 A. The output frequency is 60 Hz. At 30 ms, the peak reference current i_{ref} is step up to 14 A while keeping the output frequency to be the same.



(a)Line Voltage

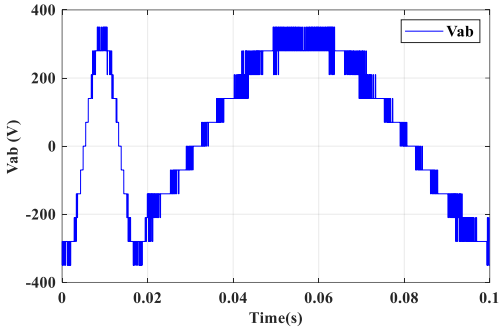


(b)Three Phase Currents

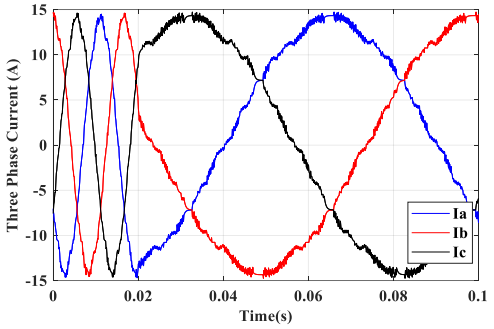


(c)CMV

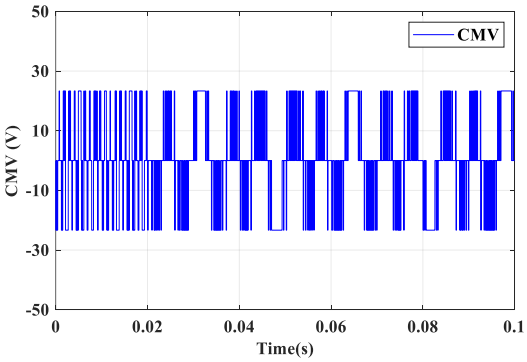
Fig. 5. 2 Performance under Current Amplitude Change



(a)Line Voltage



(b)Three Phase Currents



(c)CMV

Fig. 5. 3 Performance under Current Frequency Change

The inverter line-to-line voltage levels are increased due to the increase of the modulation index. The line-to-line voltage and three-phase load currents under the transient period are shown in Fig. 5.2 (a) (b). When the controller is stable at 8A peak currents, the line voltage THD and output currents THD are 26.6% and 5.4% respectively. Meanwhile, the line voltage and output current THD are 13.9% and 3.6% when the output current is stable at 14 A.

Fig. 5.3 illustrates the dynamic performance of the proposed multistep MPC controller under the frequency stepping down situation. The peak reference current remains to be 14 A and the frequency is kept to be 60 Hz at the beginning. At 20ms, the output current frequency steps down to be 10 Hz. The output voltage quickly changes in order to keep track of the new current reference. The line voltage and three-phase current under this case are shown in Fig. 5.3 (a) and (b). From both amplitude and frequency step change situations, the output voltage can react to the reference changes in one sampling time step and force the output current track the new reference currents. The proposed multistep prediction MPC controllers show good current tracking performance. It has to be emphasized that the number of computation is greatly reduced. Only one multiplication of one 3*9 matrix and one 9*1 matrix is required in each sampling step for the proposed FCS-MPC with the prediction length to be 3, which can be seen in equation (5.23).

The CMV voltages under the previous situations are shown in Fig. 5.2 (c) and Fig 5.3 (c). The CMV peak value is suppressed under $V_{dc}/3$ (23.3 V) under both cases. With limited dv/dt value at the motor terminals, leakage currents caused by the stray capacitors are well suppressed. Conducted and radiated electromagnetic interference (EMI) problem is mitigated. It should be noted that the CMV remains good performance even during the transient period without the need for any extra weighting factors or extra estimation process in the proposed MPC controller.

The proposed long horizon prediction FCS-MPC shows good current tracking performance with less real-time computation number. Only one matrix multiplication is required to be real-time computed in each sampling interval for a long prediction horizon. Moreover, the CMV is reduced during the steady and dynamic period by introducing the new MPC formulation. Both the current tracking and CMV reduction are achieved in the new MPC formulation without the need of cost function or weighting factors. This offers the proposed MPC formulation more efficiency and reliability compared with the conventional MPC formulation whose performance depends on the designing of the cost function and weighting factors.

The effectiveness of the proposed FCS-MPC is further validated on the IPM, which can be extended to other types of motors. The DC voltage of each CHB cell remains 100 V during the operation. The sampling time of the MPC controller is 50 μs. The seven-level CHB drive system's main parameters are illustrated in Table 5. 2.

Table 5. 2 Seven-level CHB Drive System Simulation Main Parameters

Converter parameters	Value
Cell DC-link voltage (V)	100
Stator Phase Resistance (Ω)	0.18
Armature Inductance (mH)	0.835
Flux Linkage (Wb)	0.55
Pole Pair	2
Rated Load Torque(N*m)	50
Sampling time of MPC (μs)	50
Load inertia (kg*m^2)	0.006

The IPM mathematic model can be denoted as on the *dq* rotating frame as:

$$\begin{cases} u_d = R_f i_d + L_f \dfrac{di_d}{dt} - \omega_e L_f i_q \\ u_q = R_f i_q + L_f \dfrac{di_q}{dt} + \omega_e L_f i_d + \omega_e \psi_f \end{cases} \tag{5.26}$$

Where L_f and R_f are the IPM armature inductance and stator phase resistance. The back EMF vector $\mathbf{e_{abcn}}$ of the IPM can be calculated by the flux linkage (ψ_f) and the motor rotating speed (ω_e) as:

$$\mathbf{e}_{\mathbf{abcn}} \triangleq \begin{bmatrix} e_{an} \\ e_{bn} \\ e_{cn} \end{bmatrix} = \begin{bmatrix} \cos\theta_e & -\sin\theta_e & 1 \\ \cos(\theta_e - (2\pi/3)) & -\sin(\theta_e - (2\pi/3)) & 1 \\ \cos(\theta_e + (2\pi/3)) & -\sin(\theta_e + (2\pi/3)) & 1 \end{bmatrix} \begin{bmatrix} 0 \\ \omega_e \psi_f \\ 0 \end{bmatrix} \tag{5.27}$$

Where θ_e is the rotor angle position of the IPM. The rotor angle position can be obtained from an IPM position sensor. The motor rotating speed can be derived from the rotor angle position signal. The flux linkage ψ_f of the IPM is a constant value (0.55 Wb for the simulation). After calculating the back EMF $\mathbf{e_{abcn}}$, the IPM mathematic model on *dq* rotating frame shown in equation (5.26) can be expressed in *abc* frame as:

$$\mathbf{v}_{\mathbf{(a,b,c)N}} + v_{Nn} = L_f \frac{d\mathbf{i}_{\mathbf{a,b,c}}}{dt} + R_f \mathbf{i}_{\mathbf{a,b,c}} + \mathbf{e}_{\mathbf{abcn}} \tag{5.28}$$

This is the same format with equation (5. 2). With the equation (5. 28), the proposed FCS-MPC can be easily implemented with IPM for the CHB drives following the same design procedure illustrated in 5. 2 and 5. 3 sections.

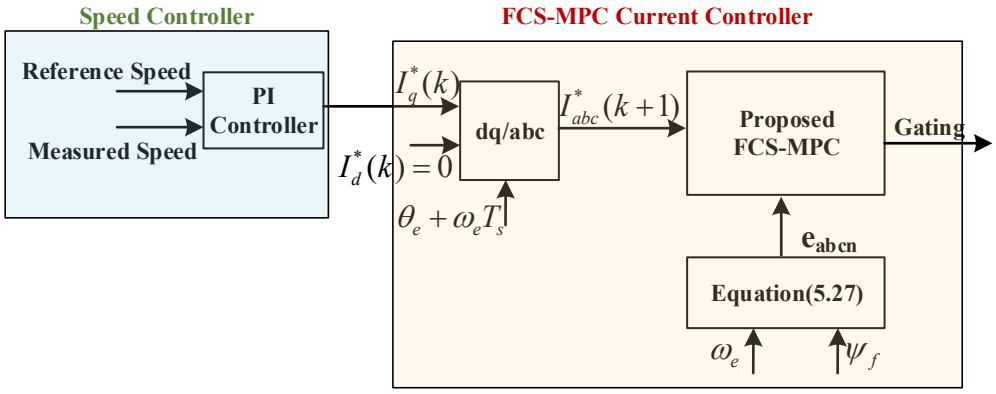
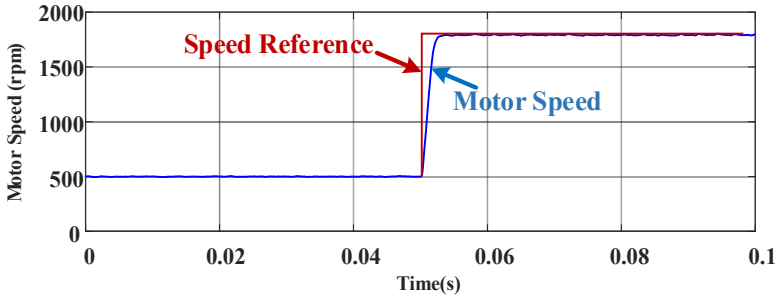


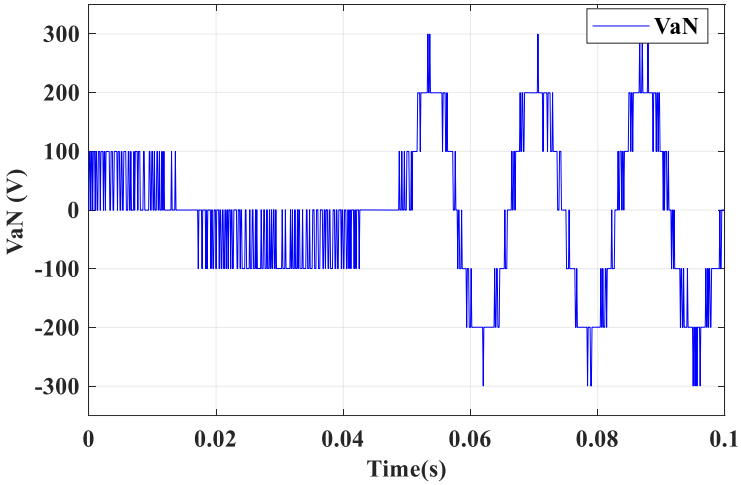
Fig. 5. 4 FCS-MPC Controller Structure based on IPM

The proposed FCS-MPC controller is shown in Fig. 5. 4. The speed PI controller sets the reference currents for the FCS-MPC current controller based on the speed error between the motor's reference speed and measured speed. The back EMF of the IPM is estimated through equation (5.27), which is required for the FCS-MPC. The proposed FCS-MPC controller is to track the reference currents prescribed by the previous speed controller.

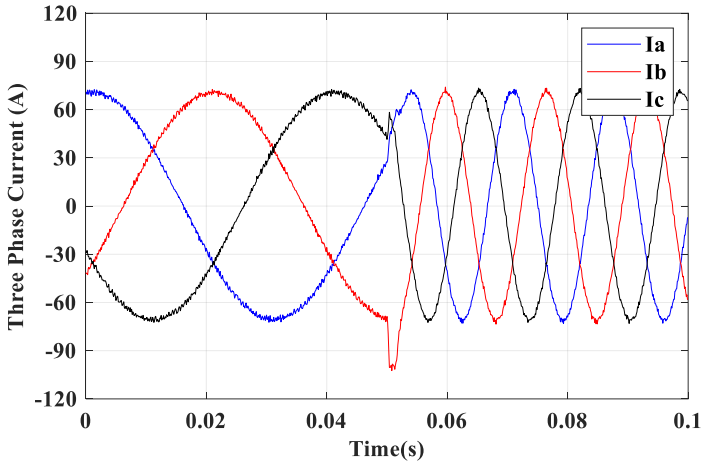
The dynamic performance of the proposed FCS-MPC controller is shown in Fig. 5. 5. As is shown in Fig 5. 5 (a), the motor is first rotating at 500 rpm with rated torque load. At 0.05s, the speed reference steps up to 1800 rpm immediately. The proposed FCS-MPC quickly responses and increases the CHB inverter output voltage and output frequency to the IPM, which is shown in Fig. 5.3 (b). The inverter output phase voltage V_{aN} increases from two levels at 500 rpm to seven levels at 1800 rpm immediately. The motor current response is shown in Fig 5.5 (c). Before 0.05 s, the CHB drive output peak current is 70 A with the rated torque load. At 0.05 s, the peak current jumps up to 100 A to accelerate the motor from 500 rpm to 1800 rpm within 0.002 s. The speed of the motor can quickly increase to the rated speed at 1800 rpm within 0.002 seconds, which indicates a good dynamic performance for the drive system.



(a)Motor Speed



(b)CHB Inverter Output Voltage



(c)Motor Current

Fig. 5. 5 Motor Acceleration Response

5.5. Experimental Results and Discussions

This section highlights the effectiveness of the proposed FCS-MPC method under different horizon prediction length based on a seven-level CHB multilevel inverter. The experimental validation of the proposed FCS-MPC formulation is performed on a dSPACE Microlab system. Experiments are carried out on a scaled-down 10 kVA seven-level CHB inverter shown in Fig. 5.6. The prototype parameters are shown in Table 5.3.

Table 5. 3 Seven-level CHB Inverter Prototype Parameters

Converter parameter	Value
Cell DC bus voltage (V)	70
DC Capacitance (mF)	2.3
Output inductance (mH)	5
Output load (Ω)	13

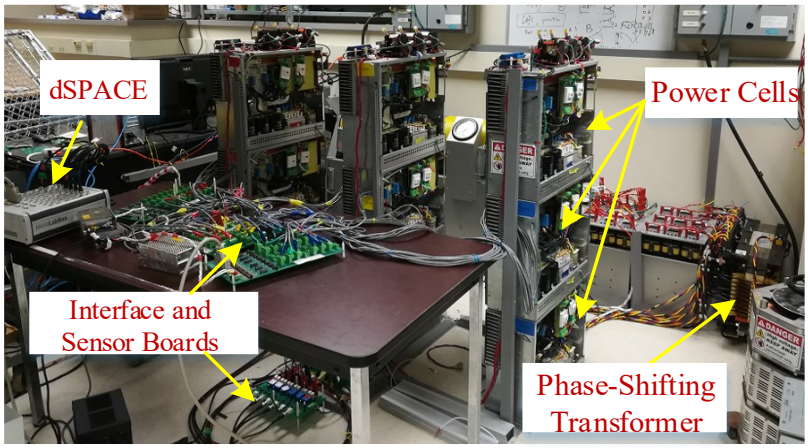


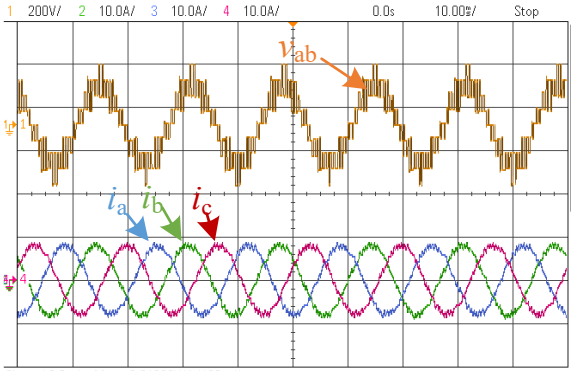
Fig. 5. 6 Prototype Seven-level CHB Inverter

First, the cost-function based MPC method and the proposed MPC formulation are performed and compared with single time step prediction. The current tracking and CMV suppression performance with the proposed method are illustrated and discussed. Second, the

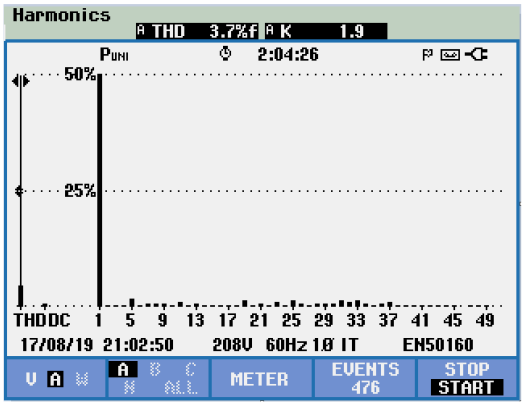
proposed MPC formulation is validated at a long prediction horizon. The comparison and conclusion are given at the end of this Section.

5.5.1. Single Step Prediction MPC Comparison

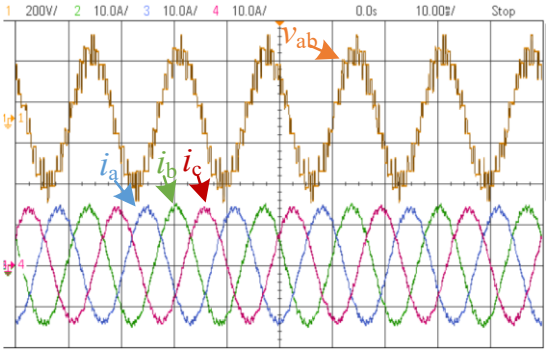
To validate the steady-state performance of the proposed MPC formulation, the experimental result of the conventional MPC method is first obtained by evaluating all possible voltage vectors in the seven-level CHB based on a defined cost function. Due to the large real-time computational burden from the cost function based MPC method [67], the minimum sampling time T_s that can be achieved is around 100 μs for the dSPACE Microlab system. It has to be mentioned that the over-current protection scheme is also included in the processor. To compare the steady performance between the proposed MPC formulation and cost function based MPC method on a seven-level CHB inverter, the sampling time T_s is fixed at 100 μs at first. The current and voltage waveforms are acquired under 8A and 14A peak reference current. As is shown in Fig. 5.7 for the conventional MPC method, the steady output load current THD at 8A and 14 A reference current are 3.7% and 2.5% respectively. The counterparts under the proposed single step MPC method at the same sampling time T_s are 2.4% and 1.7% shown in Fig 5.8. The current THD performance is improved with the proposed single-step time MPC formulation under the same sampling time. It is because the proposed MPC formulation performance is independent of the selection of the cost function or designing of the weighting factors while reducing the CMV. The best performance is guaranteed during the MPC formulation process. However, the performance of the cost-function based MPC method depends on the selection of the weighting factors in the cost function. It takes effort to tune the cost functions in experiments instead.



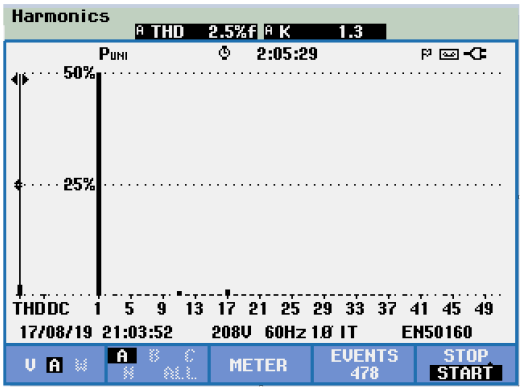
(a) Line-to-line Voltage and load currents at 8A



(b)THD of the load Current at 8A

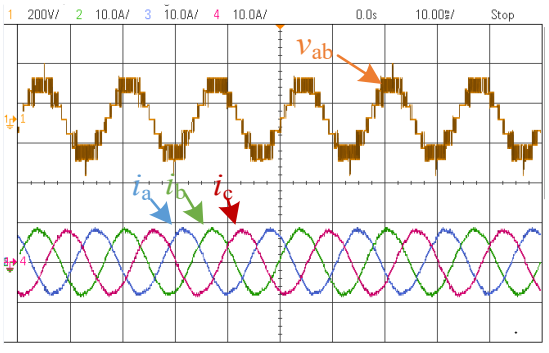


(c) Line-to-line Voltage and load currents at 14A

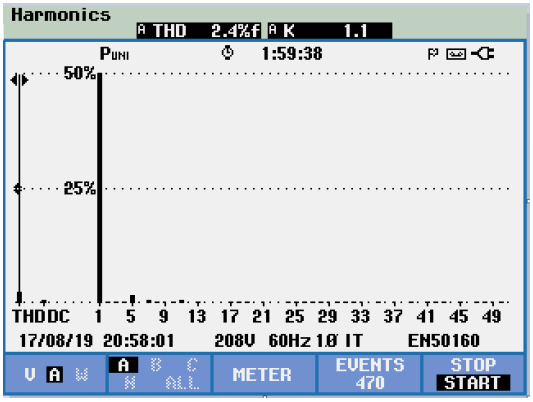


(d)THD of the load Current at 14A

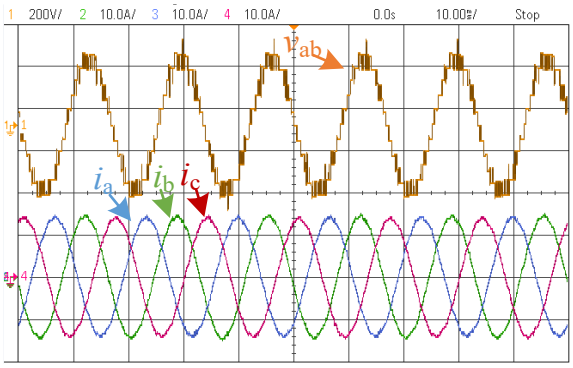
Fig. 5. 7 Conventional Single-step prediction MPC Performance at T_s 100 µs



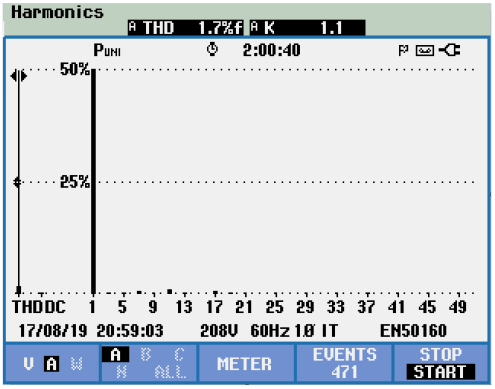
(a) Line-to-line Voltage and load currents at 8A



(b)THD of the load current at 8A



(c) Line-to-line Voltage and load currents at 14A

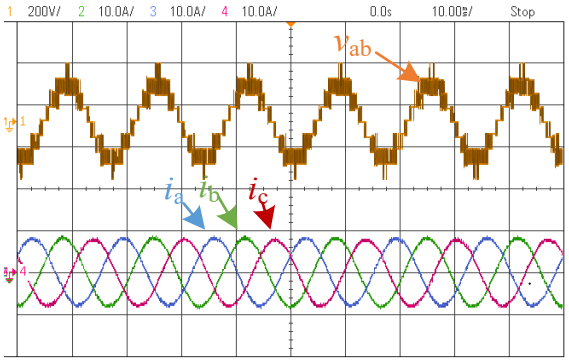


(d)THD of the load Current at 14A

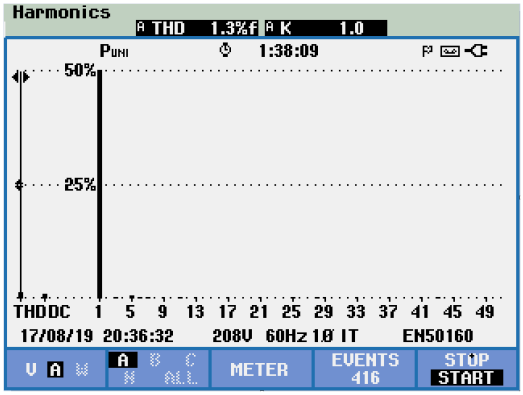
Fig. 5. 8 Proposed single-step prediction MPC Performance at T_s 100 µs

It is known that the current THD performance under the MPC controller can be further improved by reducing the sampling time T_s. However, this is not possible for the conventional cost function based MPC method due to its great demand for real-time computation resources. On the other hand, with the proposed MPC formulation, the real-time computational burden is significantly reduced, which allows to further decrease the sampling time T_s. When the sampling time T_s is reduced from 100 µs to 50 µs under the proposed single-step MPC formulation, the voltage and current waveforms are obtained in Fig. 5.9. The load current THD continues to decrease to 1.3% and 0.9% under 8A and 14A peak reference current respectively, which outperformance the previous two cases. The result proves that the proposed MPC formulation can greatly reduce the real-time computation burden. With the same computational resource, it is expected that the proposed MPC formulation can be implemented with a higher sampling rate to achieve better harmonic performance.

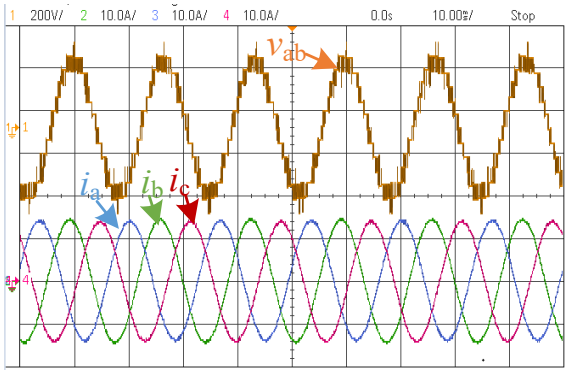
Compared with Fig. 5.7 (a), Fig. 5.8 (a), and Fig.5.9(a), the proposed MPC formulation can offer a good voltage THD and reduced the multiple voltage level jumps, which alleviate the potential EMI problem and cabling problem. The unnecessary multiple voltage level jumps are reduced to a large extent.



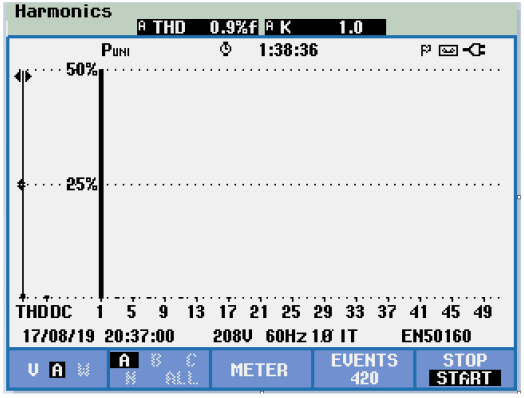
(a) Line-to-line Voltage and load currents at 8A



(b)THD of the load current at 8A



(c) Line-to-line Voltage and load currents at 14A



(d)THD of the load Current at 14A

Fig. 5. 9 Proposed Single-Step Prediction MPC Performance at T_s 50 µs

5.5.2. Dynamic Performance

The sampling time T_s is fixed at 50 µs for single-step prediction MPC. The dynamic behavior of the proposed MPC formulation for a step transient change in the amplitude of current reference is shown in Fig. 5.10. Initially, the inverter output peak current is controlled at 8A.

After 50 ms, the peak reference current i_{ref} is step up to 14A. The inverter line-to-line voltage steps are increased from 9-steps to 13-steps with the increase in modulation index. The load current quickly reaches the desired reference with approximately 0.5 ms. The proposed formulation does not affect the fast dynamic performance of the FCS-MPC. In the proposed FCS-MPC, the CMV is considered during the MPC formulation process.

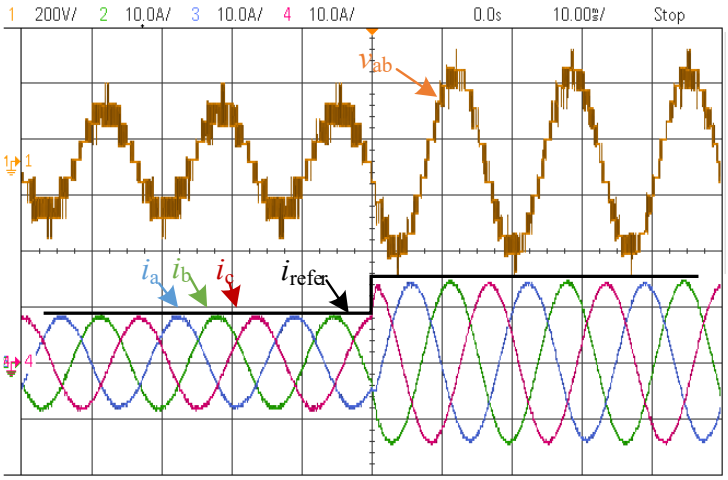


Fig. 5. 10 Current Tracking Dynamic Performance

The CMV voltage and inverter phase output voltage waveforms are shown in Fig. 5.11. The inverter phase voltage is symmetrical along time-axis. And the peak CMV voltage is controlled under one-third of the cell DC voltage $V_{dc}/3$ (around 23V). Moreover, the CMV remains the same peak value even during the transient period. Although a similar result can be obtained through cost-function based MPC formulation by tuning weighting factors in the cost function shown in equation (5.9), however, in the proposed FCS-MPC formulation, the CMV voltage is reduced without the need of any weighting factors or estimation of any cost function. The real-time computation burden and design procedures are thus reduced on a large scale, which allows one to further increase the sampling rate to achieve a better control performance.

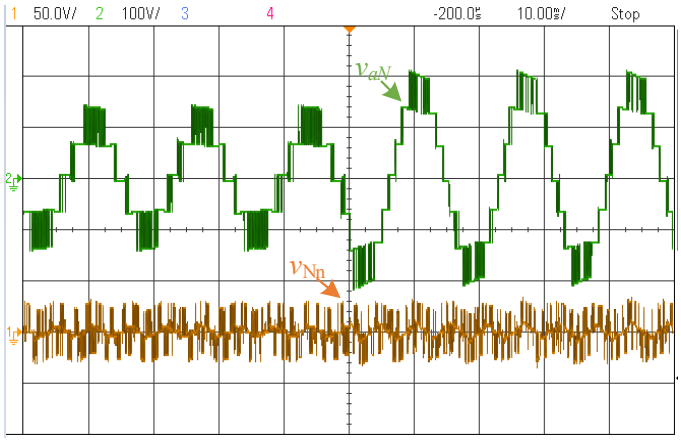
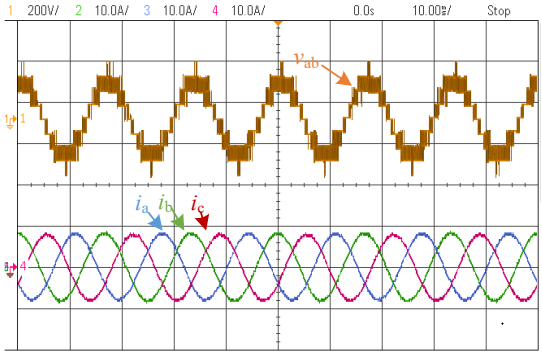


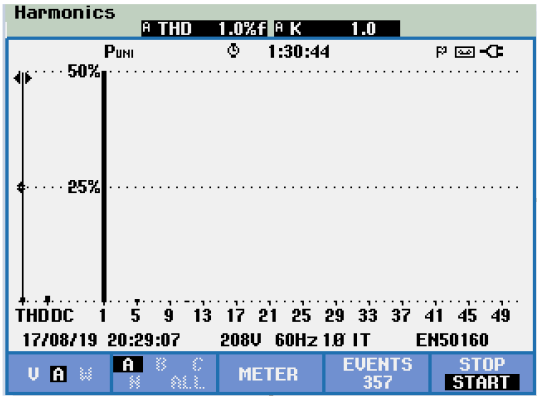
Fig. 5. 11 CMV and Phase Output Voltage

5.5.3. Long Prediction Horizon MPC Performance

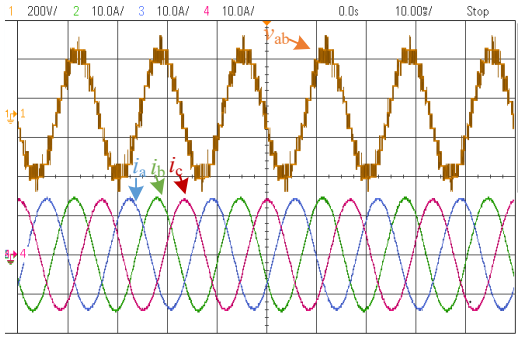
Till now, the long horizon prediction length MPC on a seven-level CHB is not reported yet due to its huge real-time computation burden through existing methods. With the proposed MPC formulation, it is now available to implement the long prediction horizon MPC on a seven-level inverter at a high sampling rate. When the prediction length is chosen to be 3, the proposed MPC can be implemented on a seven-level CHB inverter with the sampling time at 30 μs. In order to fairly compare the output performance, the experiment is performed with 8A and 14A peak reference current. As is shown in Fig. 5.12, the load current THD achieve as low as 1.0% at 8A and 0.7% at 14A peak reference current. The result is reasonable since a higher sampling rate can be adopted in the proposed long prediction horizon MPC to obtain a better control performance due to its low requirement of computation resources.



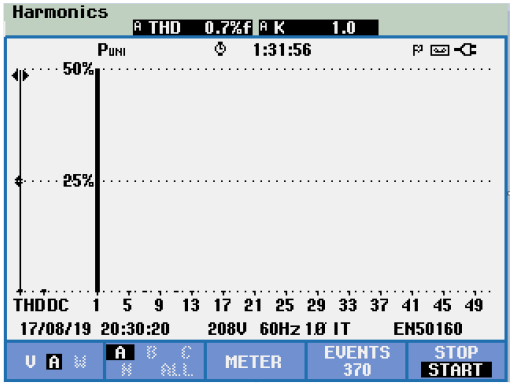
(a) Line-to-line Voltage and load currents at 8A



(b)THD of the load current at 8A



(c) Line-to-line Voltage and load currents at 14A



(d)THD of the load Current at 14A

Fig. 5. 12 Proposed MPC Performance with Prediction Length to be 3

5.5.4. Sensitivity Analysis of the proposed MPC formulation

As the quality of the MPC algorithm depends on the parameter accuracy of the system, the modeling error effect of the load inductance is quantitively studied for the proposed MPC formulation. The result is shown in Fig. 5.13. $L_{estimate}$ is the inductance value used in designing the proposed MPC controllers. L_{real} is the actual inductance in the system. The current tracking error is the ratio between the current tracking error (rms) and the reference current (10A rms). As

can be seen from Fig. 5.13, the overestimation of the load inductor for the MPC controller can increase the current tracking error for both situations at different sampling time and different prediction length. However, in both scenarios, the proposed MPC still keeps a low tracking error performance which keeps the current THD is still below 5%.

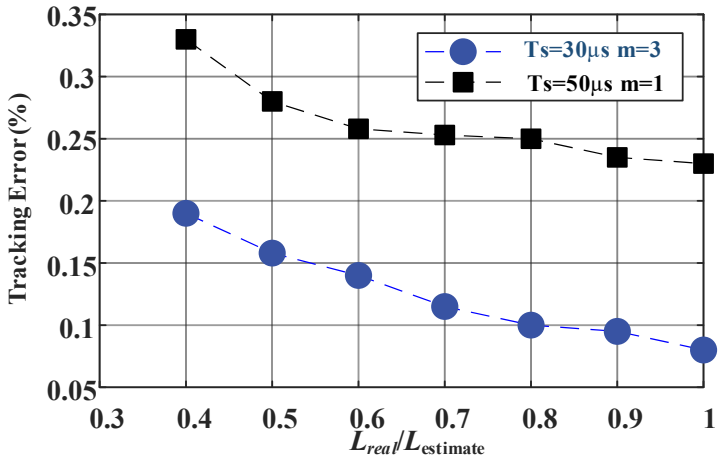


Fig. 5. 13 Effect of the Modeling Error for the proposed MPC Formulation

5.5.5. Discussion

The multilevel inverters are known to have a large number of voltage vectors. Due to the limited real-time computation resource, it is not possible to adopt a high sampling rate in the conventional MPC method. This can deteriorate the current performance of the conventional MPC method. For an illustrated seven-level CHB inverter system, the minimum sampling time can be achieved with the cost function based MPC method [67] is around 100μs. The best current THD performance can be achieved is 3.7% at 8A and 2.5% at 14A peak reference current. Instead of repetitively estimating the cost function among all the possible voltage vectors in the conventional MPC method, this chapter proposed a novel high-performance MPC formulation with reduced computation burden. With the identical micro-controller, a higher

sampling rate can be adopted in the proposed MPC formulation. The current tracking performance can be greatly improved and the CMV reduction can be achieved without any cost function or weighting factor. The performance comparison under different MPC method is illustrated and summarized in Table 5.4.

Table 5. 4 MPC Performance Summary based on a Seven-level CHB Inverter Prototype

MPC	***m* =1 [67]**	***m*=1 Proposed**	***m*=1 Proposed**	***m* =3 Proposed**
Sampling Time(μs)	100 (minimum sampling time)	100	50	30
THD i^*_{ref} = 8A	3.7%	2.4%	1.3%	1.05%
THD i^*_{ref} = 14A	2.5%	1.7%	0.9%	0.7%
Need Cost Function	YES	NO	NO	NO
CMV suppression	YES (with Weighting factor)	YES	YES	YES

Beyond that, compared with the recently published MPC formulation in [84], a prediction step of 3 was achieved on a dSPACE system for a five-level CHB inverter, the sampling interval was chosen as 100 μs. And the MPC formulation required 92.2 μs to find the optimal output voltage vector. In this chapter, a prediction horizon 3 is achieved on a dSPACE system for a seven-level CHB inverter. The control algorithm required less than 30 μs to find the output voltage levels on a dSPACE system. In terms of the robust and simplicity, the proposed MPC formulation doesn't require any cost function or any weighting factors in the design process to track the current trajectory and meanwhile suppress the CMV to 1/3 V_{dc}.

5.6. **Conclusion**

Due to the large real-time computation burden, it is difficult to implement the MPC on the multilevel inverters with high voltage levels. In this chapter, a novel high-performance FCS-MPC formulation scheme is proposed for the multilevel inverters. In the proposed MPC method, MPC is reformulated and is then transformed into an l^2 norm optimization problem. The least-square output voltage vector can be directly calculated out for the optimization problem. Both the reference current tracking and CMV reduction can be achieved without any cost function or weighting factors. Experimental results have shown that for the single-step case, the proposed MPC formulation can achieve a good current THD performance with less computation load. Meanwhile, the CMV is suppressed and minimized in the proposed MPC formulation with good dynamic performance. Moreover, with less real-time computational load, a higher sampling rate can be adopted with the proposed MPC formulation. The current tracking THD performance can be improved significantly as a result without introducing any cost function or weighting factors, which is impossible with existing cost-function based MPC formulations. The proposed high-performance MPC formulation is extended to a long prediction horizon for a seven-level CHB inverter. It takes less than 30 μs for the proposed MPC formulation to find the optimal output voltage solution on a dSPACE controller with a long prediction horizon, which is not reported so far. Future research is to implement the proposed MPC algorithm on the other multilevel inverter topologies with reduced power switches or with less redundancy.

Chapter 6

A New Fault-Tolerant Technique based on Non-Symmetrical Selective Harmonic Elimination (SHE) for CHB Motor Drives

6.1. Introduction

The cascaded H-bridge (CHB) converters have been widely used for medium-voltage motor drives due to their scalability and reliability features. It is composed of a number of modular H-bridge power cells and isolated dc voltage power sources. The H-bridge cells are cascaded on the motor side to achieve medium-voltage with low harmonic distortion. This modular configuration offers more possibilities for the medium voltage drive system to operate during faulty conditions. In the case of an internal fault in power cells, the cascaded multi-cell

converter will shut down the output currents, meanwhile, the faulty cells will be bypassed and then isolated from the system through external switches. The converter will supply the load again if the converter can provide enough balanced line-to-line voltages required by the load under the fault. This fault-tolerant property increases the reliability of the CHB drives.

As previously discussed, in extremely high power applications where reliability and switching power loss are more critical for the regenerative CHB drives, the SHE-PWM technique can eliminate a much higher number of harmonics with a low switching frequency and higher reliability. This advantage makes the SHE technique more suitable for CHB drives for extremely high-power applications. A significant indicator of the reliability is the maximum balanced line-to-line voltage amplitude under fault conditions. This chapter adopts a non-symmetrical SHE formulation to further extend the output voltage range with a good harmonic profile under fault conditions. The DC current component can be regulated for the dynamic braking operation under faults. Based on the non-symmetrical SHE formulation, the fault-tolerant problem that achieves the maximum output voltage range and good harmonic profile is converted to an optimization problem, which can be solved by the proposed optimization framework. By properly selecting the output voltage waveforms, the entire converter voltage capability can be achieved under fault conditions with a good harmonic profile. The performance of the proposed method is evaluated experimentally on a 7-level CHB motor drive.

The rest of this chapter is organized as follows. Section 6.2 introduces the mathematical formulation of the proposed fundamental frequency phase-shifted compensation (FPSC) non-symmetrical SHE method under fault. Section 6.3 demonstrates the effectiveness of the proposed method through experiments based on a seven-level CHB drive. Finally, conclusions are drawn in Section 6.4.

6.2. Proposed Fault Tolerant Design Framework

In this section, the concepts of the proposed frequency phase-shifted compensation (FPSC) non-symmetrical SHE method is introduced. The FPSC method and non-symmetrical SHE method are reviewed. Then an optimization framework design process is presented to achieve maximum output balanced line-to-line voltage under fault conditions based on the proposed method.

6.2.1. Fundamental Frequency Phase-Shifted Compensation

Without losing the generality, a seven-level CHB drive system is considered, as is shown in Fig. 6.1.

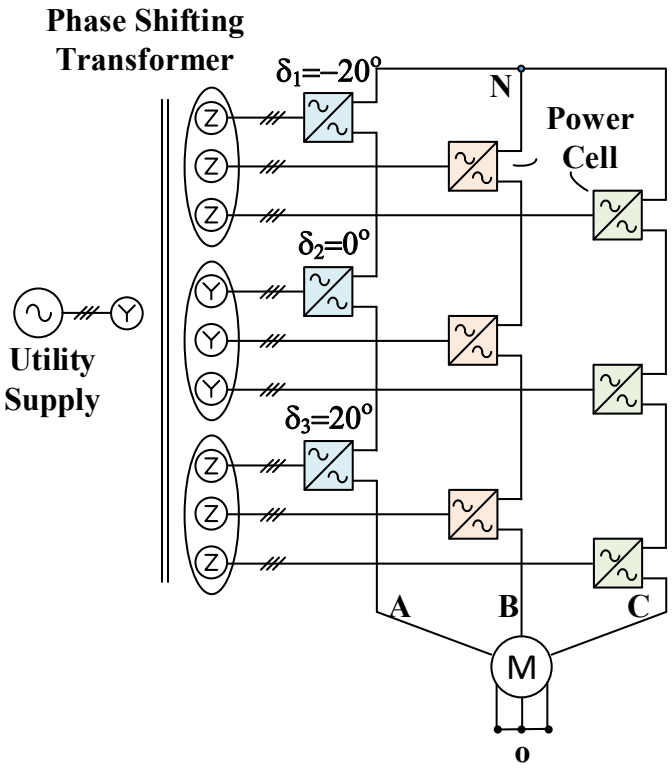


Fig. 6. 1 A Seven-level CHB drive Illustration for Fault Tolerant

In normal operation, the amplitude of the phase voltage generated is equal to 3 V_{dc} (referred to as 3 p.u hereinafter), where V_{dc} is the dc bus voltage of each power cell. The output

maximum balanced line-to-line voltage is 5.19 p.u. When one cell fails in phase A, it will be bypassed, and then the maximum achievable voltage level by the faulty phase A is reduced from 3 p.u to 2 p.u. As is shown in Fig. 6.2, the magnitudes and phase angles of the converter fundamental frequency phase voltages V_{AN1}, V_{BN1}, V_{CN1} θ_{AN1}, θ_{BN1} and θ_{CN1} are recalculated to assure that the load fundamental voltage amplitude V_{AO1} V_{BO1} and V_{CO1} are identical and the phase angles between load phase voltages V_{AO1} V_{BO1} and V_{CO1} are exactly 120 degrees.

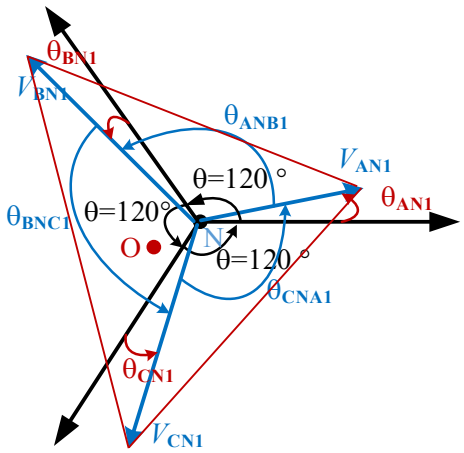


Fig. 6. 2 FPSC Method Voltage Vector Illustration

Based on the definition shown in Fig. 6.2, the constraints (6.1) should be satisfied to achieve the balanced three-phase load voltages V_{AO1} V_{BO1} and V_{CO1}.

$$\begin{cases} \theta_{ANB1} = \theta_{BN1} - \theta_{AN1} + 120^o \\ \theta_{BNC1} = \theta_{CN1} - \theta_{BN1} + 120^o \\ \theta_{ANB1} + \theta_{BNC1} + \theta_{CNA1} = 360^o \\ V_{AN1}^2 + V_{BN1}^2 - 2V_{AN1}V_{BN1}\cos(\theta_{ANB1}) = V_{BN1}^2 + V_{CN1}^2 - 2V_{BN1}V_{CN1}\cos(\theta_{BNC1}) \\ V_{BN1}^2 + V_{CN1}^2 - 2V_{BN1}V_{CN1}\cos(\theta_{BNC1}) = V_{AN1}^2 + V_{CN1}^2 - 2V_{AN1}V_{CN1}\cos(\theta_{ANC1}) \end{cases} \tag{6.1}$$

The first three equations illustrate the angular relations among the inverter output phase voltage vectors V_{AN1}, V_{BN1}, V_{CN1}. The last two equations are derived by assuring that the output

line-to-line voltage vector can compose an equilateral triangle. The load neutral point O will reside in the central point of the composed equilateral triangle. The load voltage vector at fundamental frequency V_{AO1} V_{BO1} and V_{CO1} are thus balanced if and only if the equilateral triangle requirements are satisfied. However, to obtain the maximum balanced output voltage, directly applying the maximum output fundamental phase voltages V_{AN1} V_{BN1} and V_{CN1} to the equation (6.1) may result in no available angles solution [88] [96].

6.2.2. Third-Harmonic Injection

As is known, a one-sixth of third-harmonic injection in the inverter phase voltages can increase the maximum possible inverter output line voltage. But when the FPSC method is applied under fault cases, the third-order harmonic in phase voltages will not be naturally canceled out and thus appear in the load line voltages.

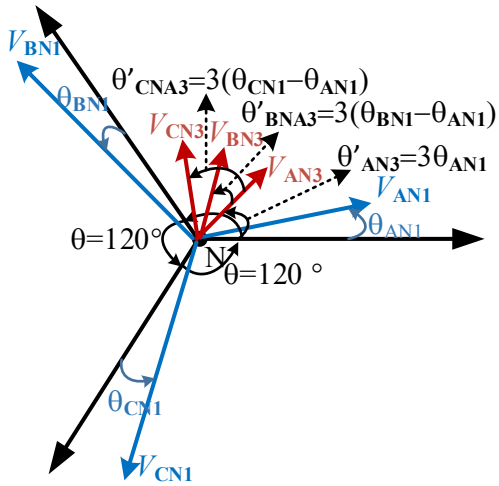


Fig. 6. 3 Unbalanced Third-order Harmonic under FPSC Method

As shown in Fig. 6.3, the fundamental frequency output voltages calculated from the FPSC method are V_{AN1}, V_{BN1}, V_{CN1}. The inverter output third-order harmonic voltage components without extra angle shifted V_{AN3}, V_{BN3}, V_{CN3} can be expressed as:

$$\begin{cases} v_{AN3} = V_{AN3}\sin(3\omega t + 3\theta_{AN1}) \\ v_{BN3} = V_{BN3}\sin(3\omega t + 360^o + 3\theta_{BN1}) \\ v_{CN3} = V_{CN3}\sin(3\omega t - 360^o + 3\theta_{CN1}) \end{cases} \tag{6.2}$$

where θ_{AN1}, θ_{BN1} and θ_{CN1} are determined through FPSC method in equation (6.1), which are not identical under fault situation. The third-order harmonic in phase voltages cannot cancel in the line voltages due to the unequal phase-shifting angles of the fundamental frequency phase voltages. The resulting third-order harmonic currents will circulate among three phases, which causes power loss and vibration in the machines.

To cancel out the third-order harmonic in the line-to-line voltages under fault, the extra phase angles of third-order harmonic content θ_{BN3} and θ_{CN3} are required to be intentionally shifted [107] to compensate for the misalignment angle θ'_{BNA3}, θ'_{CNA3} caused by FPSC method shown in Fig. 6.3. The third-order harmonic component with extra angle shifted θ_{BN3} and θ_{CN3} can be expressed as:

$$\begin{cases} v_{AN3} = V_{AN3}\sin(3\omega t + 3\theta_{AN1}) \\ v_{BN3} = V_{BN3}\sin(3\omega t + 2\pi + 3\theta_{BN1} + \theta_{BN3}) \\ v_{CN3} = V_{CN3}\sin(3\omega t - 2\pi + 3\theta_{CN1} + \theta_{CN3}) \end{cases} \tag{6.3}$$

Based on previous analysis, to achieve both balanced fundamental frequency component and balanced third-order harmonic component under fault events, the inverter output voltage constraints shown in equation (6.1) are further extended to the inequality (6.4), where ε is the function tolerance. The phase voltage magnitude and phase-shifting angles of both fundamental frequency and third-order harmonic components are variables that can be adjusted to optimize the output line voltages and output line voltage harmonic profile.

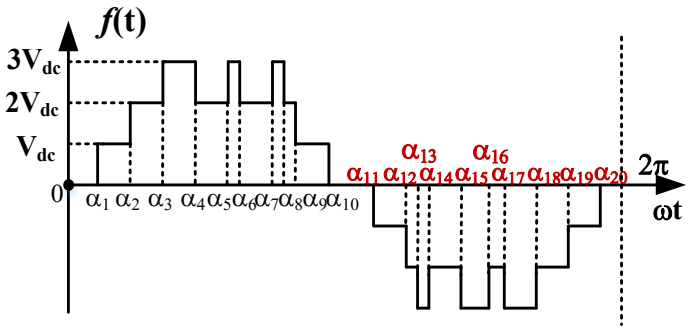
$$\begin{cases} \theta_{ANB1} = \theta_{BN1} - \theta_{AN1} + 120^o \\ \theta_{BNC1} = \theta_{CN1} - \theta_{BN1} + 120^o \\ \left| V_{AN1}^2 + V_{BN1}^2 - 2V_{AN1}V_{BN1}\cos(\theta_{ANB1}) - (V_{BN1}^2 + V_{CN1}^2 - 2V_{BN1}V_{CN1}\cos(\theta_{BNC1})) \right| \le \varepsilon \\ \left| V_{BN1}^2 + V_{CN1}^2 - 2V_{BN1}V_{CN1}\cos(\theta_{BNC1}) - (V_{AN1}^2 + V_{CN1}^2 - 2V_{AN1}V_{CN1}\cos(2\pi - \theta_{ANB1} - \theta_{BNC1})) \right| \le \varepsilon \\ \left| V_{BN3}\angle(\theta_{BN3} + 3\theta_{BN1})) - V_{AN3}\angle 3\theta_{AN1}) \right| \le \varepsilon \\ \left| V_{CN3}\angle(\theta_{CN3} + 3\theta_{CN1})) - V_{AN3}\angle 3\theta_{AN1} \right| \le \varepsilon \end{cases} \quad (6.4)$$

For the special case when V_{AN3}=V_{BN3}=V_{CN3}=0 (no third-order harmonic injection) and function constraint ε=0, the constraint inequality (6.4) is degraded to the FPSC equation (6.1). Although inequality (6.4) assures the balanced output voltages, however, the available output voltage region cannot be determined directly from (6.4). First, the FPSC nonlinear equations set (1) may have no solution under some faulty situations by directly assigning V_{an1}, V_{bn1} and V_{cn1} amplitude, such as 3-1-1 case (two cells in phase B and C are bypassed) [88][96]. Direct solving the equation (1) to obtain the phase-shifted angles is not available for some fault situations. More important is that the fundamental phase-shifted angles calculated in (6.1) are not necessarily the optimal value to extend the maximum output voltage range if third-order harmonics are injected. Second, an insufficient third-order harmonics injection will limit the inverter output voltage range. On the other hand, an excess third-order harmonic injection can deteriorate the output voltage harmonic profile due to the overmodulation. The proper amplitude of the third-order harmonic cannot be directly determined. As a result, it is a challenge to extend the inverter output range under faulty situations and still keep the inverter in the linear modulation operation range with good harmonic profile.

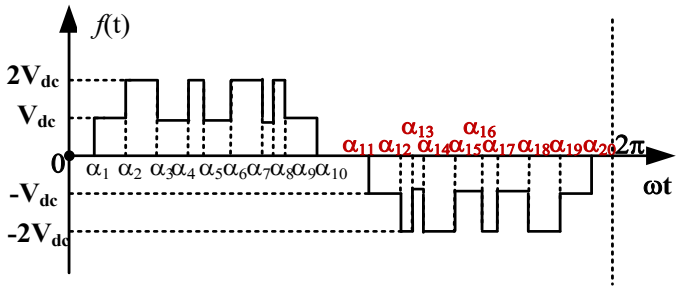
6.2.3. Proposed Automated Fault Tolerant Design Optimization Framework

To solve the ahead mentioned problems, instead of solving the equation (6.1) directly under a variety of faulty situations, in this section, the fault tolerant problem is converted to an optimization problem through non-symmetrical SHE formulation and then optimized by the GA to avoid the no solution problem and overmodulation problem. The proposed automated design process can guarantee the maximum output voltage range with a good harmonic profile. The proposed optimization framework is illustrated in this section.

First of all, the non-symmetrical SHE is adopted to achieve maximum balanced output voltages with a good harmonic profile under fault conditions. In the non-symmetrical SHE formulation, the switching angles are relaxed to the region between 0 to 2π as shown in Fig. 6.4 (a). The variable switching angles in non-symmetrical SHE are four times than the quarter-symmetry SHE (switching angles found between [0 π/2]) and two times than the half-wave symmetry SHE (switching angles found between [0 π]) while the same orders of harmonics can be eliminated.



(a)Healthy seven-level phase voltage waveform



(b)Faulty five-level phase voltage waveform with one cell bypassed

Fig. 6. 4 Non-symmetrical SHE for CHB Drive

Assuming the set of switching angles for phase voltage A are denoted as (α_1 to α_l), phase B as (β_1 to β_l), and phase C as (γ_1 to γ_l) hereinafter, where l is the number of the available switching firing angles per phase. To facilitate the illustration, in this section, the total available switching angles l is selected to be 20. The proposed method can be implemented with any number of switching firing angles without losing the generality. In the case of one cell fault, to achieve the maximum balanced output voltages, each healthy phase of a seven-level CHB converter can generate a seven-level voltage waveform shown in Fig. 6.4(a), while the faulty phase can generate only a five-level waveform, shown in Fig.6.4 (b).

The line-to-neutral point N voltage waveform V_{XN} (X=A,B,C) could be expressed by Fourier series in equation (6.5).

$$\begin{aligned} V_{XN} &= \frac{A_0}{2} + \sum_{n=1}^{\infty} \sqrt{A_{Xn}^2 + B_{Xn}^2} \sin(n\omega t + \theta_{XNn}) \\ &= V_{XN0} + \sum_{n=1}^{\infty} V_{XNn} \sin(n\omega t + \theta_{XNn}) \end{aligned} \tag{6.5}$$

where the A_{Xn} and B_{Xn} are Fourier coefficients of phase voltage waveform $V_{XN,}$ θ_{XNn} is the nth order harmonic phase-shifted angle. V_{XNn} is the nth harmonic amplitude for the phase voltage V_{XN}. The A_{Xn} and B_{Xn} are determined by the voltage waveform f(t) through the equation (6.6).

$$\begin{cases} A_{Xn} = \dfrac{1}{\pi}\int_{-\pi}^{\pi} f(t)\sin(n\omega t)d\omega t, n = 0,1,2,3... \\ B_{Xn} = \dfrac{1}{\pi}\int_{-\pi}^{\pi} f(t)\cos(n\omega t)d\omega t, n = 1,2,3... \end{cases} \tag{6.6}$$

To guarantee the balanced output line voltages, the FPSC constraint inequality (6.4) should be satisfied while determining the switching angles. With 20 available switching angles in non-symmetrical SHE PWM formulation, the phase voltage harmonic components under the 10th order can be controlled respectively. To achieve an excellent harmonic spectrum with the limited number of gating switch angles, the low order harmonics others than the DC component and third-order harmonics are all set to zero. To comply with the previous notations, the mathematic expression is shown in equation (6.7). The variable δ indicates injected DC voltage component which depends on the required braking torque.

$$\begin{cases} |V_{XNn}| \le \varepsilon, (n = 2,4,5,6,7,8,9) \\ |V_{XN0} - \delta| \le \varepsilon, (n = 0) \end{cases} \tag{6.7}$$

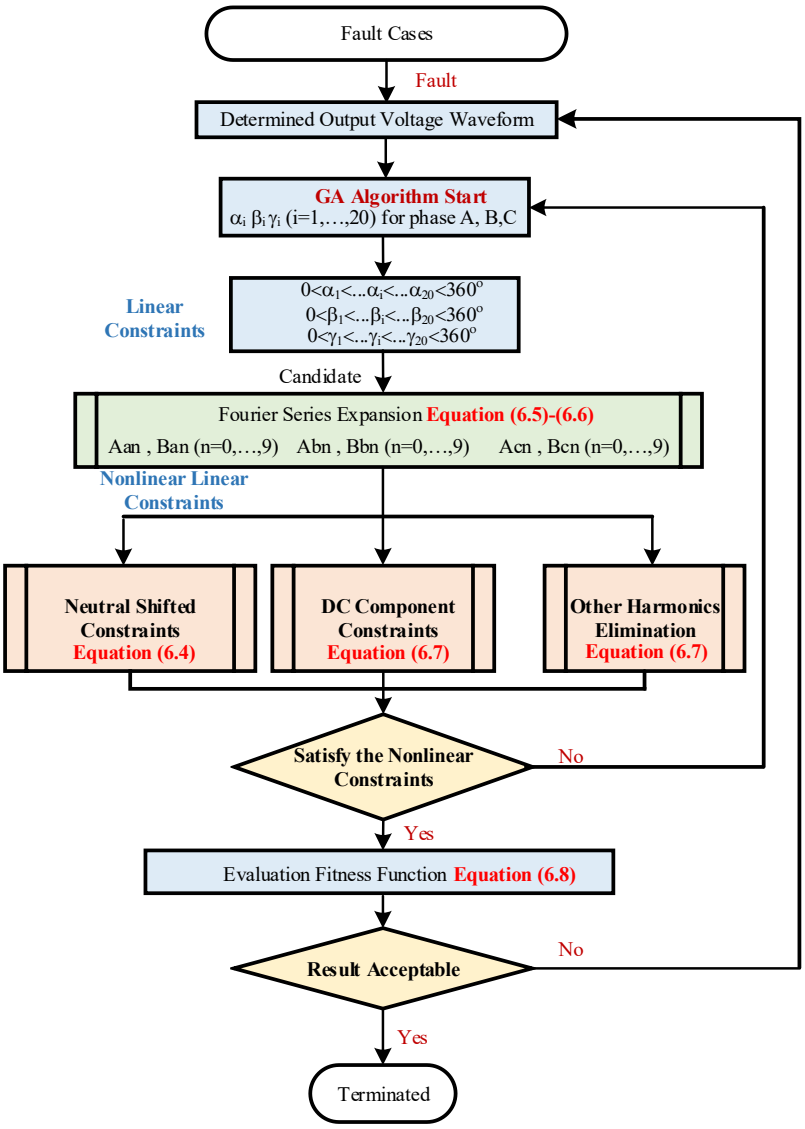


Fig. 6. 5 Automated Optimization Framework for the FPSC Non-symmetrical SHE Method under Fault

With the non-symmetrical SHE formulation, the post fault tolerant problem can be described as: optimizing the switching angle (α_1 to α_l), (β_1 to β_l), and (γ_1 to γ_l) for phase A, B, C that can generate maximum balanced output voltage range with a good harmonic profile under the determined voltage waveforms. Instead of solving the FPSC equations directly, a global optimization algorithm GA is adopted to optimize the switching angle (α_1 to α_l), (β_1 to β_l), and

(γ_1 to γ_l) for phase A, B, C that can generate balanced output line voltage with a good harmonic profile under the determined voltage waveforms. In this way, no solution problem is avoided by this formulation.

The fault tolerant optimization design process is shown in Fig. 6.5. It integrates non-symmetrical SHE formulation and FPSC method to obtain the maximum balanced output voltage under cell failures with a good harmonic profile. The selection of the switching firing angles in the proposed optimization framework is required to satisfy the balanced line-to-line voltage constraint shown in (6.4), the harmonics elimination constraints and the DC component constraints shown in equations (6.5-6.7). The GA is used to search within the switching angle spaces that satisfied all the listed constraints until the minimum objective function value *f* is found. Different output voltage including the maximum output voltages can be achieved by the following cost function *f*, where *M* is the expected fundamental frequency balanced line-to-line voltage.

$$f = \left| (V_{AN1}^2 + V_{BN1}^2 - 2V_{AN1}V_{BN1}\cos(\theta_{ANB1}) - M^2) \right| \tag{6.8}$$

Although the searching space for GA will boost with the increasing of the switching angles, however, this is not a big issue since the SHE firing angles are off-line calculated and then stored in the processor's memory [31-32]. GA is a heuristic search algorithm that mimics the procedure of natural selection, which explores the design spaces to find solutions to the optimization problem. The candidate solution is searched in the solution domain by mutation, inheritance, selection, and crossover [117].

Beyond the fault tolerant optimization framework, the advantages of the proposed FPSC non-symmetrical SHE formulation under fault is significant compared with quarter-symmetry SHE and half-wave symmetry SHE. On one hand, extra shifted angle θ_{BN3} and θ_{CN3} in the third-order harmonic component shown in equation (6.4) cannot be achieved with quarter-symmetry SHE formulation. This is because the quarter-symmetry constraints assure B_{Xn} under any harmonics in equation (6.6) to be zero. Meanwhile, the DC current injection cannot be realized with the half-wave symmetrical SHE formulation during braking. This can be justified through equation (6.6), the DC component A_{X0} is zero with half-wave symmetry constraint. On the other hand, both the quarter-symmetry SHE and half-wave symmetry SHE can be regarded as the special case of the non-symmetrical SHE by adding symmetry constraints. The non-symmetrical provides more flexibility for choosing the switching angles, which is beneficial for extending the output voltage range and meanwhile keeping a good harmonic profile.

In summary, the proposed fault tolerant automated optimization framework based on non-symmetrical SHE formulation assures maximum balanced output voltage range with a good harmonic profile if the output voltage waveforms are determined under different fault situations. And the DC current injection feature can be achieved, which is impossible with half-wave symmetry SHE formulation.

6.3. Simulation Results

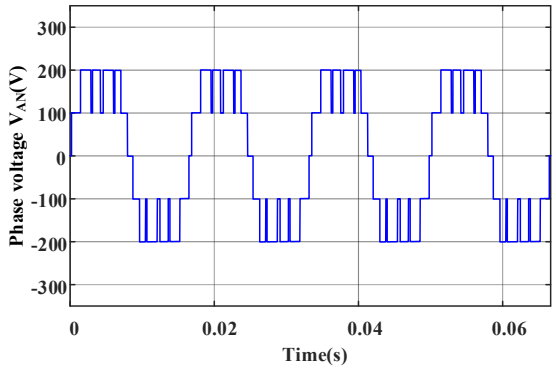
Two simulations are carried out to validate the feasibility of the proposed fault tolerant strategy. In the case of one cell failure in phase A, the switching angles and neutral shifted angles for all phases are calculated offline according to the proposed method. Then Matlab/Simulink is

then used for verifying the effectiveness of the solution. The maximum line-to-line voltage designed from the proposed method will increase by 7% compared with those designed from the previous methods. Beyond that, to further validate the DC component injection ability of the proposed method during a fault, the switching angles and neutral shifted angles are again calculated with -5% p.u DC component in phase B and +5% p.u in phase C. The three-phase current with DC component is then obtained through Simulink simulation, which will be later used for machine braking under one cell fault. In the following simulations, each H bridge inverter cells have a DC voltage source of 100 V that makes up total 300 V in each phase. The RL load is used to emulate the electrical machine, in which R=0.5ohm, L=8mH.

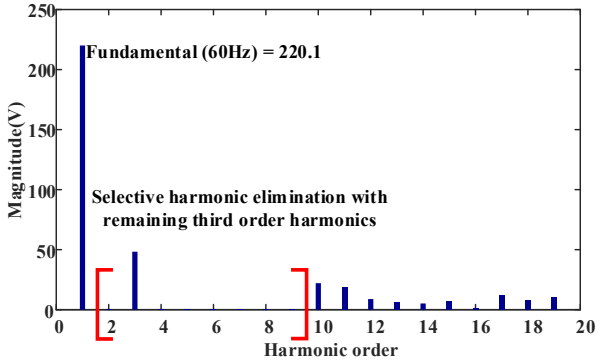
6.3.1. Maximum Line-to-line voltages without DC Component

The switching angles and neutral shifted angles are off-line calculated with help of MATLAB GA toolbox [27]. The population size of the searching candidate in GA is chosen to be 12000. The maximum generation in GA is 800. The gating switching angles are shown in Appendix Table 6.5.

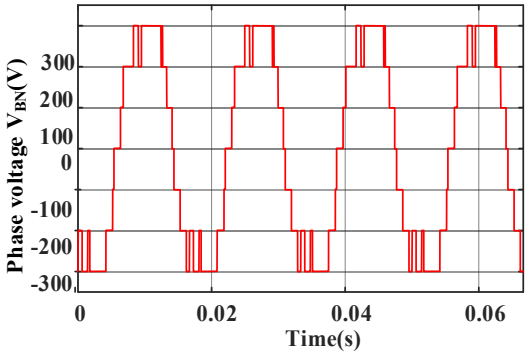
The converter's phase voltages, as well as their harmonic spectrum, are plotted in Fig.6.6 (a)-(f). As is previously presented, the faulty phase A continues operation with five levels and two healthy phases still generate seven levels. According to Fig. 6.6 (b),(d),(f), the amplitude of the fundamental component of A,B,C phase voltage are equal to 220.1V, 324.8V, and 324.8V.



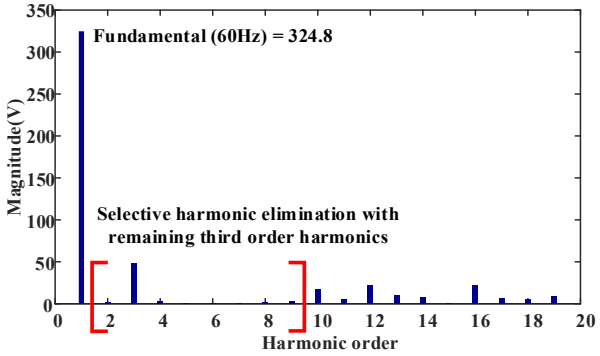
(a)phase voltage of the faulty phase A



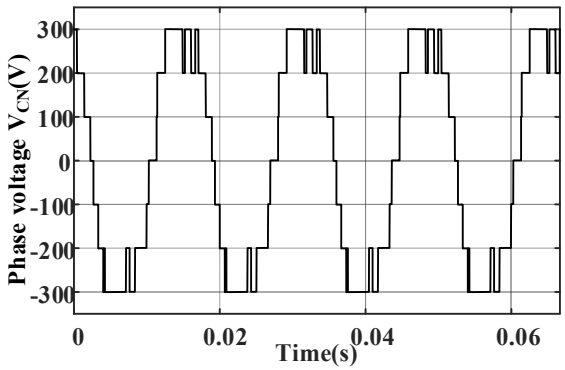
(b)Harmonic content of V_{AN}



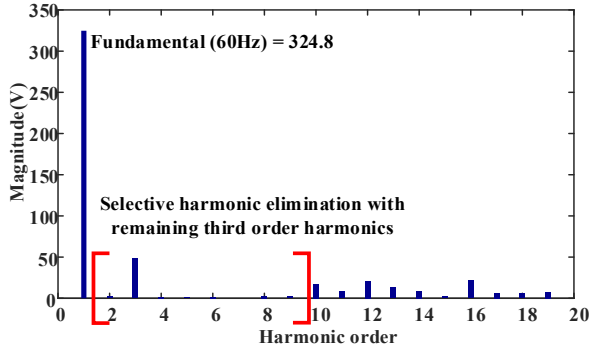
(c)phase voltage of phase B



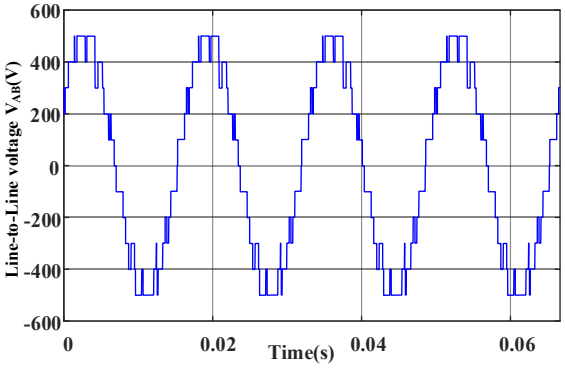
(d) Harmonic content of V_{BN}



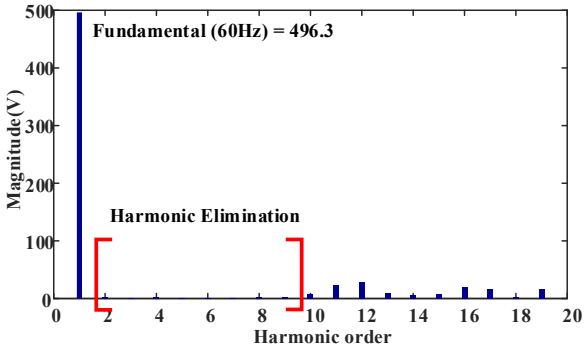
(e) phase voltage of phase C



(f) Harmonic content of V_{CN}



(g)line-to-line voltage of V_{AB}



(h) Harmonic content of V_{AB}

Fig. 6. 6 CHB Output Voltage in case of One Cell Failure

As is previously discussed, to achieve a maximum voltage level, the third-order harmonics have remained. The third-order harmonics magnitude in both phase A, B and C are identical 47.9V. All the other harmonics under 10^{th} order are eliminated which proves the harmonic elimination ability of the proposed design strategy. The THD (total harmonic distortion) of A, B and C three phases are 31.65%, 21.33%, and 21.35%.

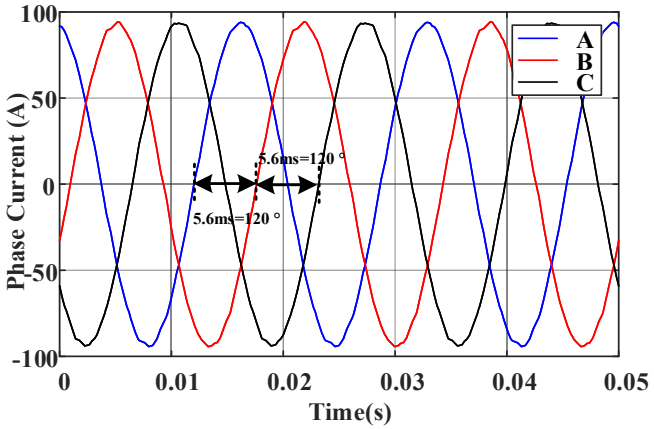


Fig. 6. 7 Load Current Supplied by CHB with Fault Cell

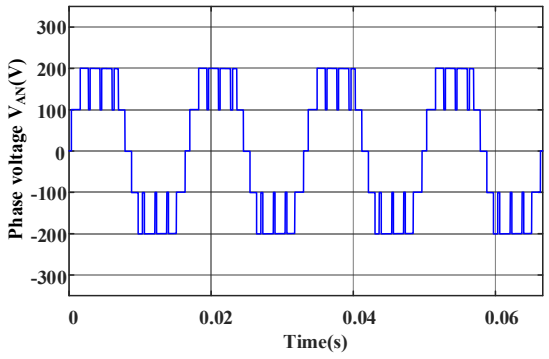
The three-phase currents waveforms are presented in Fig 6.7. The amplitudes of the line current are equal and the phase shifts between the three phases are 120 °. To achieve this balanced three-phase current, the fundamental frequency neutral shifted angles are $\theta_{ANB}=\theta_{CNA}=$ 130.2°. The line-to-line voltage V_{AB} waveform and its harmonic spectrum are shown in Fig. 6.6 (g) (h). The third-order harmonics in-phase voltages are completely eliminated with the extra phase shifted in the third-order harmonics. The balanced three-phase current and 'clean' line voltage confirm the validity of the proposed fault-tolerant strategy.

For a healthy seven-level CHB inverter, the maximum fundamental line-to-line voltage is 300*1.73=519V (5.19 p.u) without third-order harmonic injection. However, if one of the nine-cell in seven level CHB inverter is in fault and bypassed, the fundamental frequency of line-to-

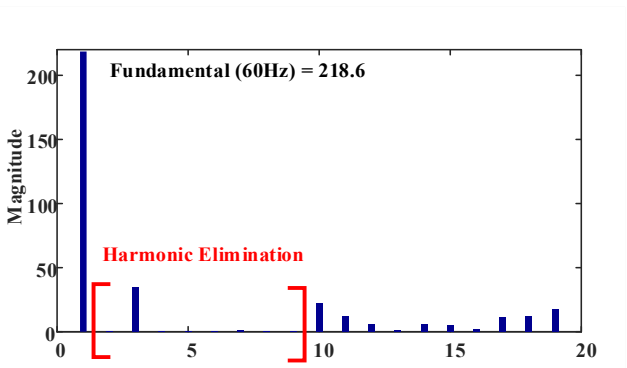
line voltage calculated from the proposed method is 496 V (4.96 p.u) shown in Fig. 6.6 (h). The reduction in the voltage during fault when using the proposed method is 4.4%, which is smaller than previous ever reported.

6.3.2. Maximum Line-to-line Voltages with DC Component Control for Braking

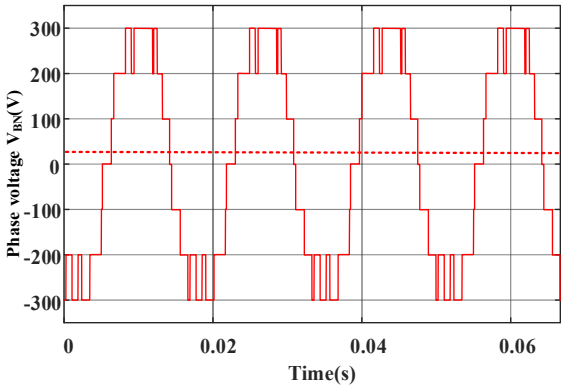
A DC current and a field-excited component current are usually injected into the stators to obtain the optimum braking performance of stopping an induction machine for the AC drives with a diode rectifier front end. The conventional quarter- and half-wave SHE is not able to generate DC current component due to its symmetrical waveform. To control the DC voltage component, the symmetrical constraints are relaxed to form the asymmetrical SHE in the proposed design strategy. With -5% p.u. DC component in phase B and +5% p.u DC component in phase C, the maximum balanced line-to-line voltage achieved by the proposed method is 476V (4.76 p.u) in case of one cell fault in phase A. The gating switching angles for each phase are shown in Appendix Table 6.6.



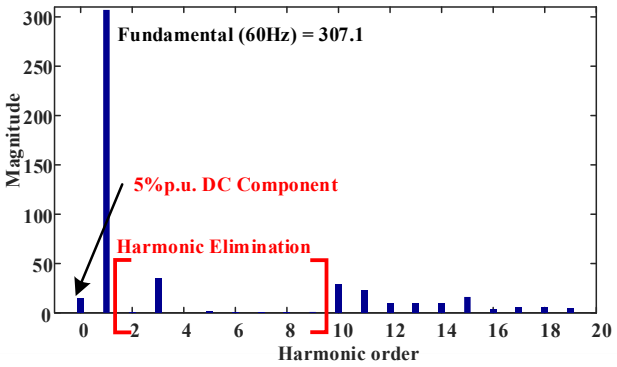
(a)phase voltage of the faulty phase A



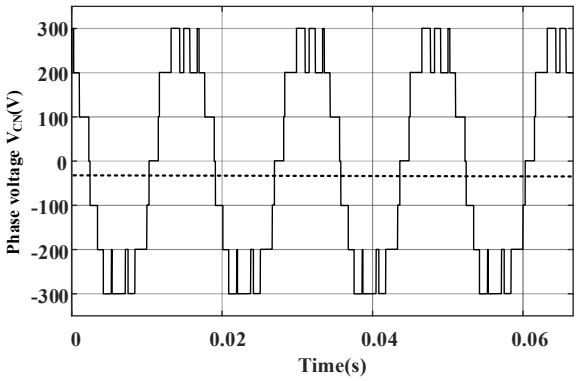
(b) Harmonic content of V_{AN}



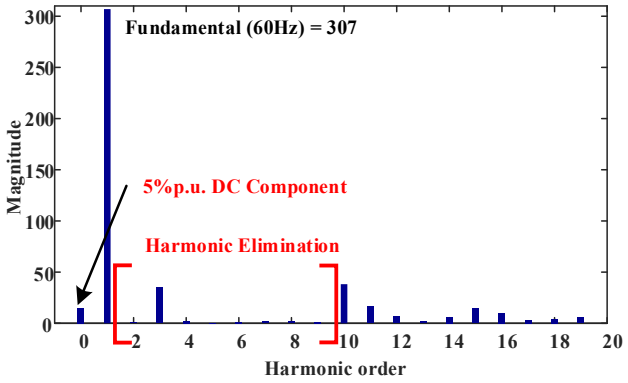
(c) phase voltage of the phase A



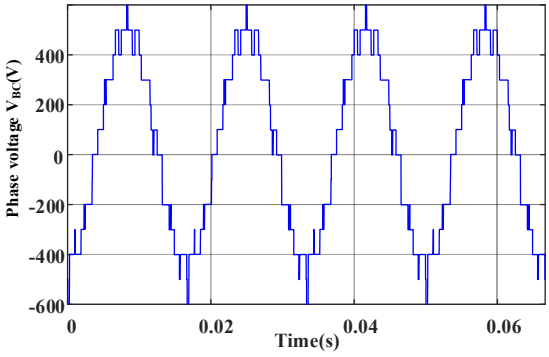
(d) Harmonic content of V_{BN}



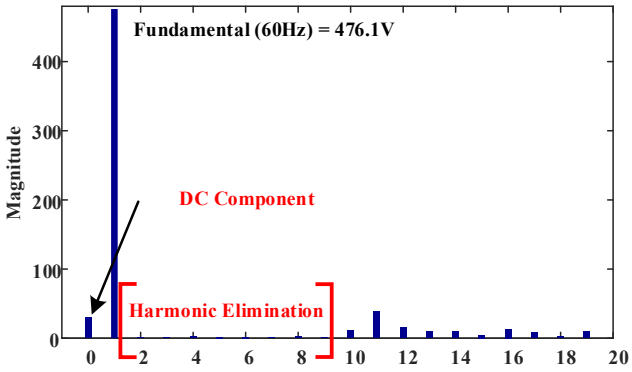
(e) phase voltage of the phase C



(f) Harmonic content of V_{CN}



(g) line voltage of V_{AB}



(h) Harmonic content of V_{AB}

Fig. 6. 8 CHB Voltage in case of One Cell Failure with DC Braking Situation

Both three-phase voltages and their harmonic contents are shown in Fig. 6.8. According to Fig. 6.8 (b),(d),(f), the amplitude of the fundamental component of A,B,C phase voltages are equal to 218.6V, 307V, and 307V. To achieve this balanced three-phase current, the fundamental frequency neutral shifted angles are $\theta_{ANB}=\theta_{CNA}=$ 130.2°. The third-order harmonics in both

phases A, B and C are 34.8V. The DC voltage components are controlled with the asymmetrical SHE method. As is presented in Fig. 6.8 (g), (h), the DC voltage component exists in line-to-line voltage while third-order harmonics are eliminated. The three-phase currents are shown in Fig. 6.9. With 0.5 ohm resistance per phase, there is a 30 A DC circulating current between B and C phase which is beneficial for the motor braking.

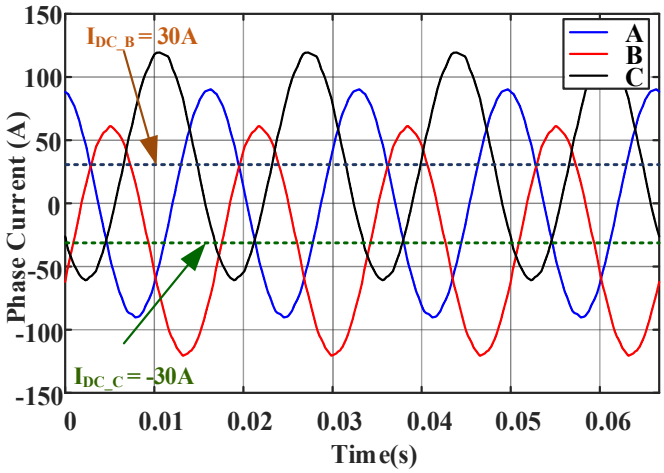


Fig. 6. 9 Load Current with DC Circulating Current

The maximum balanced line-to-line three-phase voltages under fault is a very important indicator for the CHB drive reliability. To validate the proposed fault tolerant method, the maximum balanced line-to-line three-phase voltages are obtained for both motoring and braking situations of a diode-front end seven-level CHB drive system. As is shown in Fig. 6.10, the maximum voltage modulation of a seven-level CHB is 5.19 p.u if not over-modulation. In the conventional neutral shifted method [106-107], the maximum achievable line voltage is 4.6 p.u. However, with the proposed design method of asymmetrical gating switching angles, the maximum achievable line voltage is 4.96 p.u with one of nine cell failure in a seven-level CHB drive. Moreover, the DC component is controlled to brake the induction machine even under fault

situation. The maximum achievable line-to-line voltage is 4.76 p.u. with a 5% p.u DC component in the healthy phase.

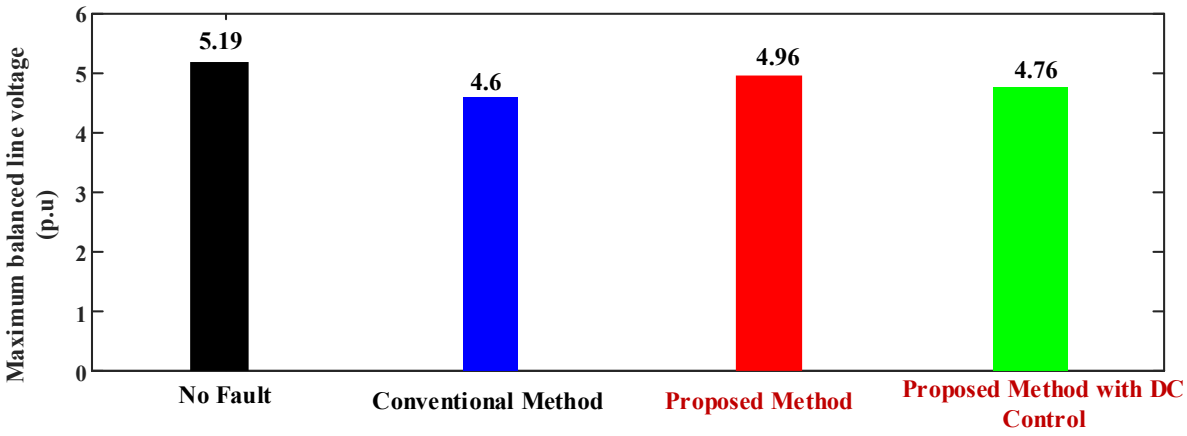


Fig. 6. 10 Maximum Output Line Voltages Comparison

6.4. Experimental Results and Discussion

In this section, the implementation of the proposed non-symmetrical SHE on a seven-level CHB drive under cell failure is studied. Experiments are carried out to validate the feasibility of the proposed fault tolerant strategy with DC component injection and without DC component injection under cell failures. The maximum balanced output line-to-line voltages for both situations are obtained to validate the effectiveness of the proposed method. The 10 kVA seven-level CHB inverter setup is shown in Fig. 6.11. The DC link voltage of each cell is provided by the phase-shifting transformer and the diode rectifiers. The output of the CHB is connected to a balanced three-phase resistive/reactive load. It is assumed that the fault has been detected in phase A. The prototype parameters are shown in Table 6.1.

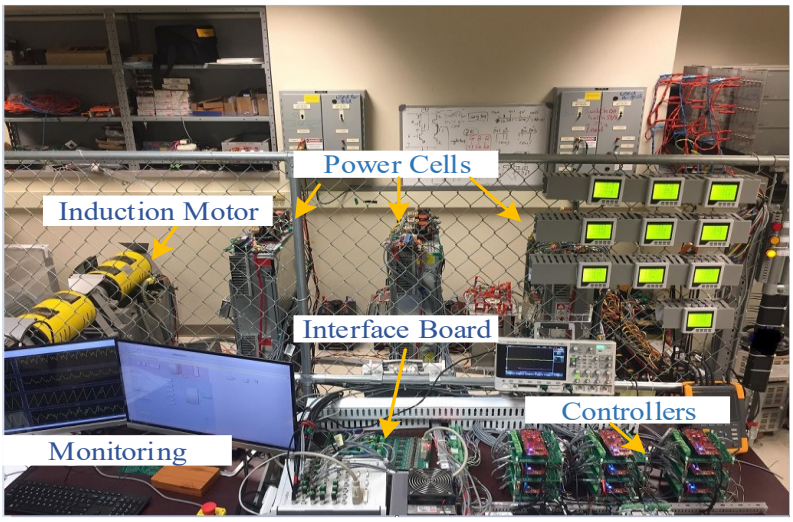


Fig. 6. 11 Prototype Seven-level CHB Inverter for Fault Tolerant

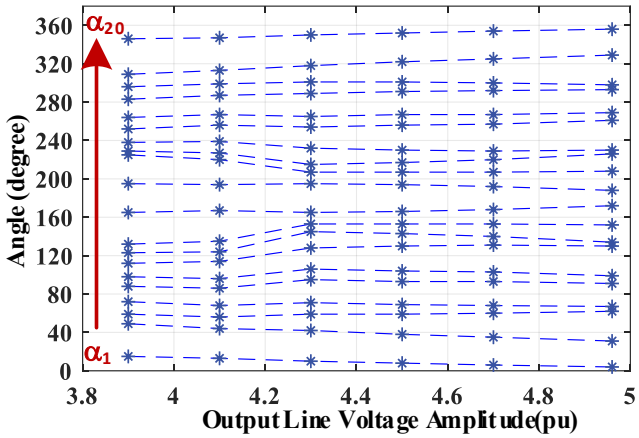
Table 6. 1 Seven-level CHB inverter Prototype parameters

Converter parameter	Value
Cell DC bus voltage (V)	100
Output frequency (Hz)	60

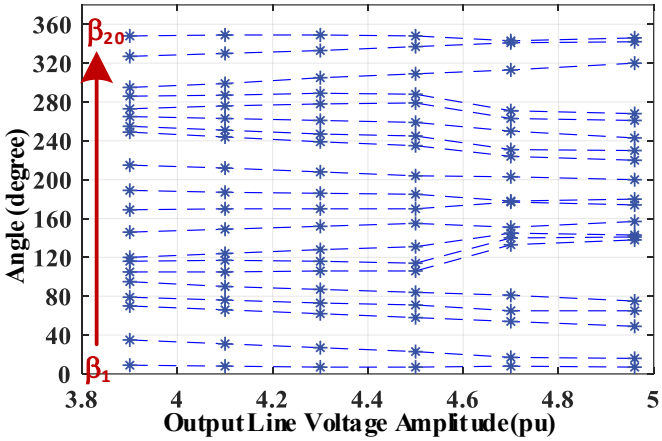
6.4.1. Maximum Output voltages without DC component Injection

The optimization framework in Fig. 6.5 is implemented using MATLAB GA global optimization toolbox [117]. DC components in the phase voltages are all set to zero. The gating switching angles of the proposed non-symmetrical SHE method are calculated through the proposed optimization framework and the result are shown in Appendix Table 6.5.

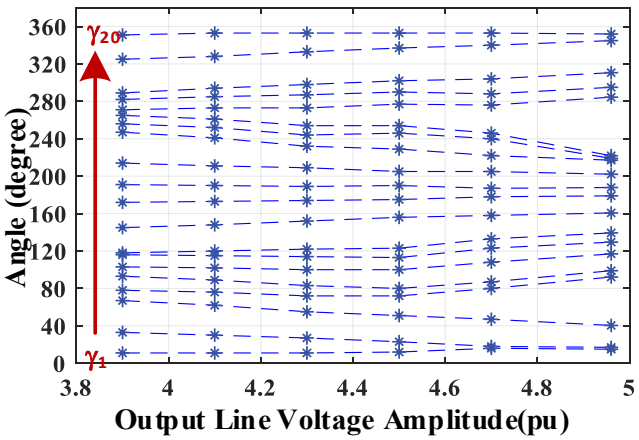
With the determined output voltage waveforms shown in Fig 6. 4, the switching angle map under different balance output line voltage amplitude (from 3.9 p.u to 4.96 p.u)is obtained and shown in Fig. 6.12. No need to use the FPSC fault tolerant method if the demanded output line voltage is less than 3.9 p.u.



(a)Phase A



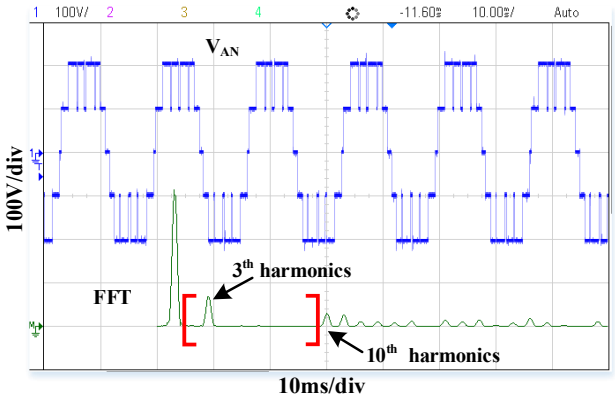
(b) Phase B



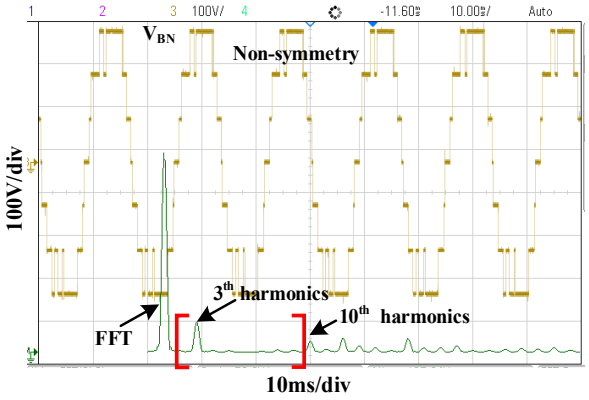
(c) Phase C

Fig. 6. 12 Switching Angle Map under Different Output Line Voltages

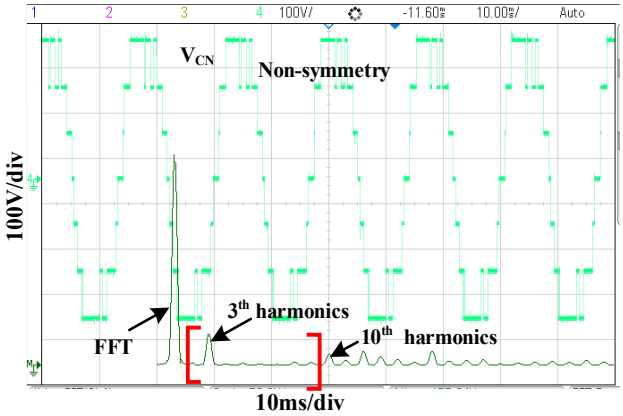
Considering one of the cells in Phase A failed, and then a contactor bypassed the faulty cell. As is shown in Fig. 6.13 (a), (b), and (c), the switching angles are not symmetrical and the 3^{th} order harmonic is remained in the phase voltages to achieve the maximum possible fundamental phase voltage. With the 20 available switching angles for each phase, the DC component and the harmonics under 10^{th} order are eliminated through the proposed non-symmetrical SHE PWM method. With the extra phase-shifted of the 3^{th} order harmonic, the 3^{th} order harmonic will also cancel out in the line-to-line voltage shown in Fig. 6.13 (d) and (e). The total harmonic distortion (THD) of phases A, B, and C are 31.7%, 21.3%, and 21.4% respectively. The output three-phase voltages are balanced at the load side. This can be validated by the balanced three-phase currents are shown in Fig. 6.13 (f). It should be emphasized that during the fault event the phase-shifted angles of both the fundamental frequency and the third-order harmonics are recalculated, such that a higher output voltage at the fundamental frequency is achieved with no third-order harmonics appears in the load side. This is one of the main advantages of the proposed method using the non-symmetrical SHE approach.



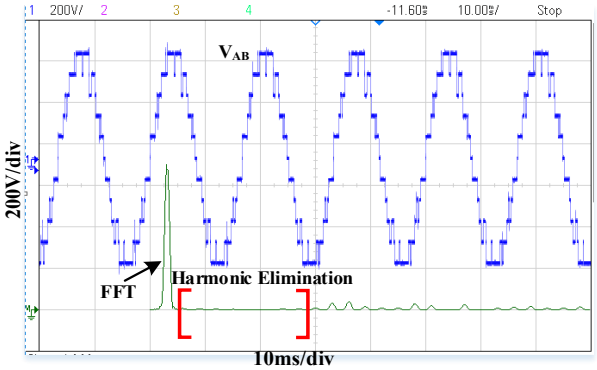
(a)Phase voltage V_{AN}



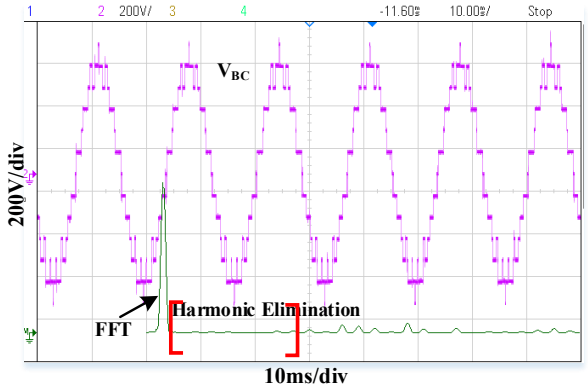
(b)Phase voltage V_{BN}



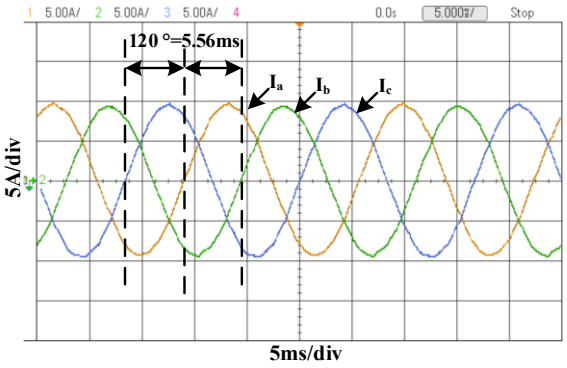
(c)Phase voltage V_{CN}



(d)Line-to-line voltage V_{AB}



(e)Line-to-line voltage V_{BC}



(f)Three-phase currents

Fig. 6. 13 Fault-tolerant Non-symmetrical SHE Method without DC Component Injection

The maximum output voltage with the proposed post-fault method is illustrated in Table 6.2. For a healthy seven-level CHB inverter in normal operation, the maximum fundamental line-to-line voltage amplitude is 519V (5.19 pu). If one cell fails, the cell bypass method can generate 3.47p.u output voltage which is equivalent to 33.3% reduction in the output voltage. The FPSC-PWM method [87][96] can help to improve the output voltage with 12.1% reduction of the output voltage. The FPSC symmetry SHE method can slightly improve this and has a voltage drop of 11.6%. The maximum line-to-line voltage amplitude under one cell fault when using the proposed non-symmetrical SHE method is 4.96 p.u, and the voltage drop is only 4.4% compared with the normal healthy operation. This is better than the existing half-wave symmetry SHE method which shows 11.6% voltage drop under the same fault situation [106] [107].

Table 6. 2 Maximum Balanced Output Voltage Amplitude without DC Injection under One Cell bypassed

	BYPASSED CELL	**FPSC-PWM [87][96]**	**SYMMETRY SHE [106][107]**	**PROPOSED NON-SYMMETRICAL SHE**
MAX. OUTPUT VOLTAGE	3.47 pu	4.56 pu	4.59 pu	**4.96 pu**
VOLTAGE DROP	33.3%	12.1%	11.6%	**4.4%**

In the proposed method, the fault tolerant problem is converted to an optimization problem based on a non-symmetrical SHE formulation. The proposed automated optimization can provide a solution for all other fault situations with determined output voltage waveforms. The maximum balanced output line voltage under 1-3-3 and 3-1-1 fault cases is shown in Table 6.3. The notation A-B-C is used to denote different fault operation cases, where A, B, and C indicate the number of operative cells in the respective phase. It is noted that the set of nonlinear FPSC equations has no solution in this fault situation by direct assigning the phase voltages amplitude [88][96].

Table 6. 3 Maximum Balanced Output Voltage Amplitude without DC Injection under Different Fault cases

CASE	CELLS IN A	CELLS IN B	CELLS IN C	FPSC-PWM [87][96]	SYMMETRY SHE[106][107]	PROPOSED METHOD
I	2	3	3	**4.56**	**4.59**	**4.96 pu**
II	1	3	3	**3.83**	**3.82**	**3.97 pu**
III	3	1	1	**2**	**-**	**2 pu**

6.4.2. Maximum Line-to-line voltages with DC component Control under fault

Besides the advantage of higher achievable balanced output voltage under fault, the proposed FPSC non-symmetrical SHE method is also able to control the output DC voltage component which will be beneficial for the diode-front-end CHB drive during the dynamic braking operation under fault situation. This cannot be achieved with the symmetry SHE methods.

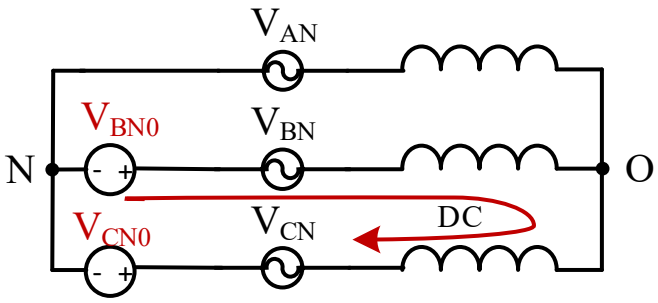
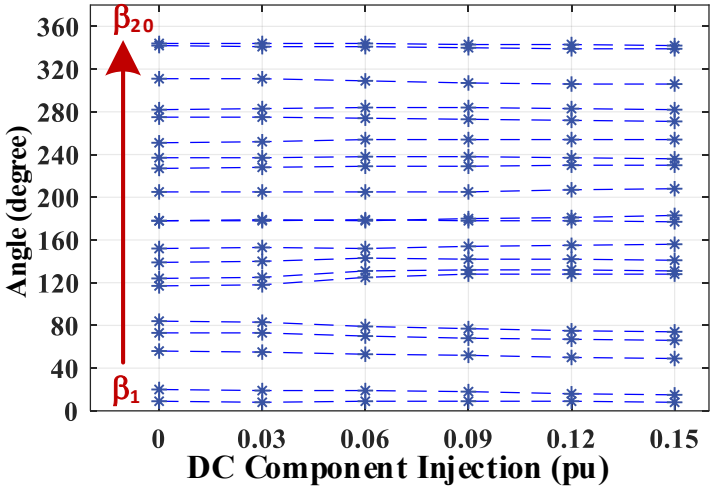


Fig. 6. 14 DC Component Injection between Healthy Phase B and C

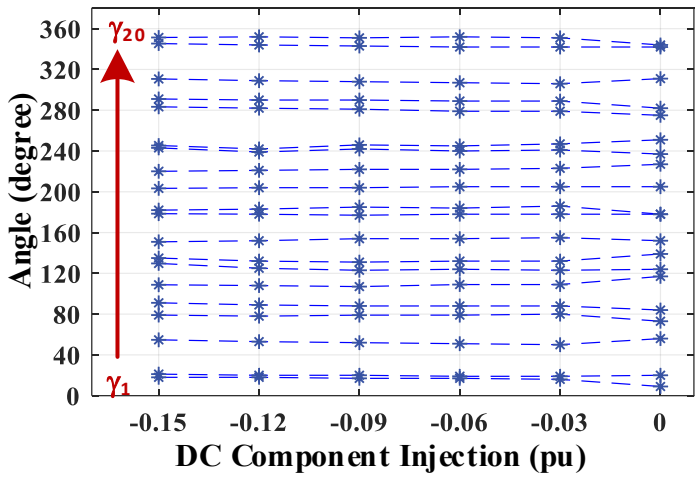
Assume that one of the cells in Phase A failed, after that, a contactor bypassed the faulty cell. The faulty phase A continues operation with five levels and two healthy B, C phases still generate seven levels. A DC voltage component is injected into the healthy phases B and C to generate a DC current circulating between healthy B and C phases. The circulating current between B and C phase is demonstrated in Fig. 6.14. To avoid the DC current flows into the fault phase A, the injected DC voltage component of phase B and phase C is shown as follow:

$$V_{BN0} = -V_{CN0} \tag{6.9}$$

To validate the DC component injection ability of the proposed method, the switching angles and FPSC shifted angles are again calculated with ±15% p.u DC component in phase B and C. Gating switching angles optimized with the proposed GA framework and the switching firing angles are shown in Appendix Table 6.6. The switching angle map under variation of the DC injection voltage while keeping the output line voltage a 4.76 pu is shown in Fig. 6.15.



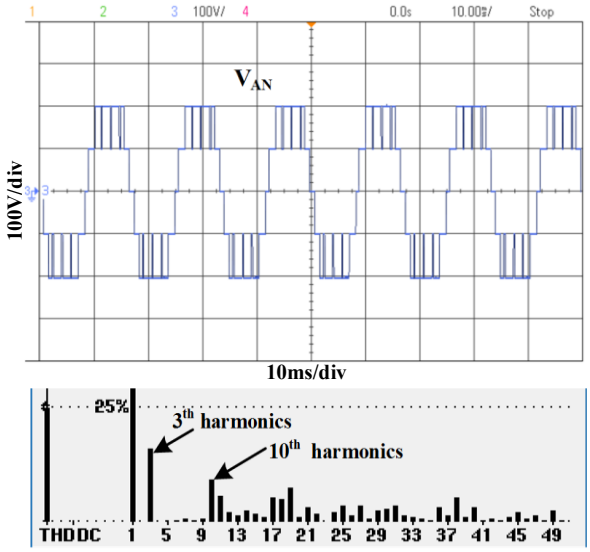
(a)Phase B



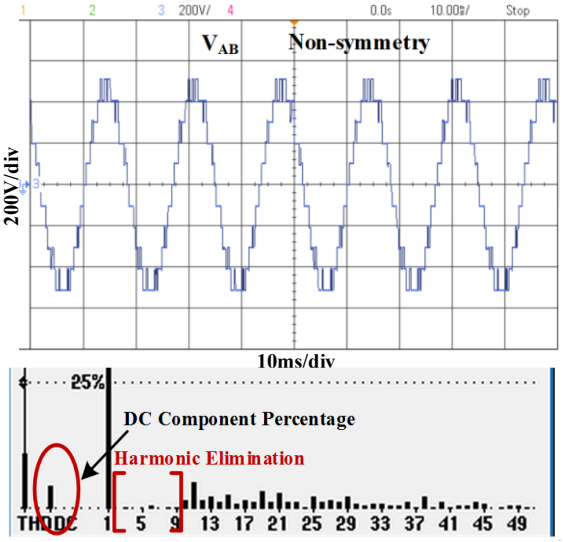
(b)Phase C

Fig. 6. 15 Switching Angle under different DC Injection while Output Voltage is 4.76pu

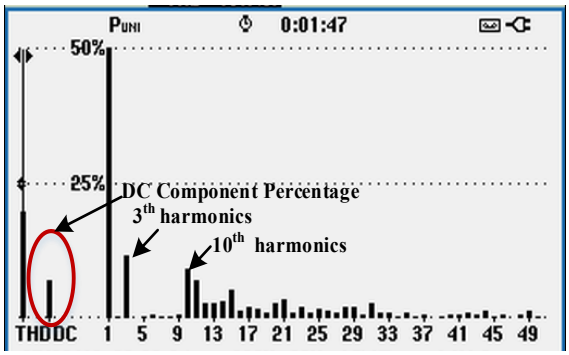
As it is shown in Fig. 6.16 (a), (b), and (c), the 3th order harmonic is remained in the phase voltages to achieve maximum possible fundamental phase voltages.



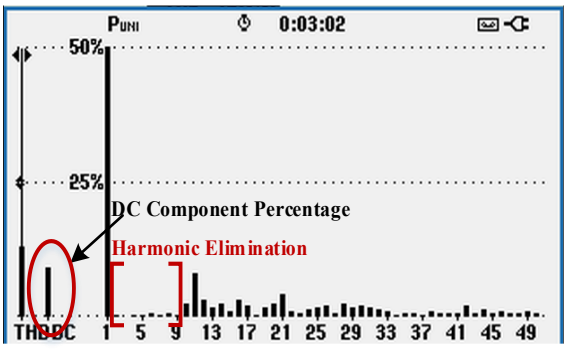
(a) Phase voltage V_{AN}



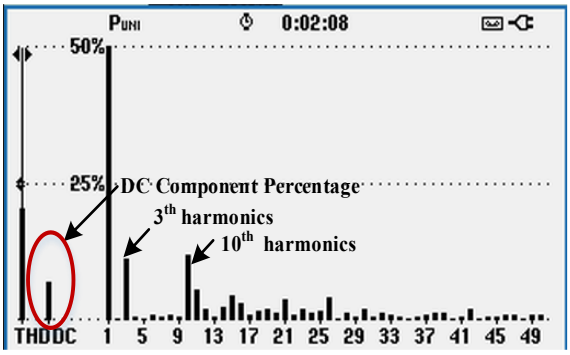
(d) Phase voltage V_{AB}



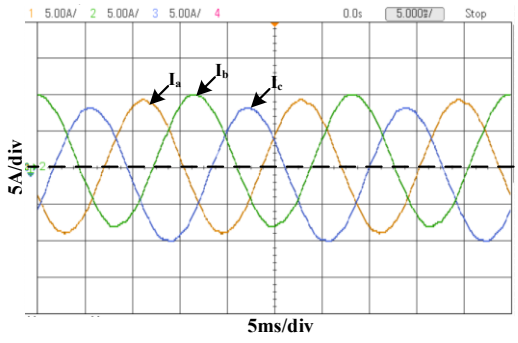
(b) Phase voltage V_{BN}



(e) Phase voltage V_{BC}



(c) Phase voltage V_{CN}



(f)Three-phase currents

Fig. 6. 16 Fault-tolerant Non-symmetrical SHE method with DC Component Injection

The amplitude of the fundamental component of A, B, C phase voltage amplitude equal to 219 V, 307V, and 307V respectively. The total harmonic distortion (THD) of A, B, C phase voltages are 27.6%, 21.2%, and 21.8% respectively. The third-order harmonics amplitude in both phases A, B and C are 34.8V and canceled out in the load voltages. The DC component injection in B and C phase are illustrated in their voltage FFT figure.

The FPSC shifted angles are $\theta_{ANB1}=\theta_{CNA1}=129.2°$ to achieve the maximum balanced output voltages. The waveforms of the line voltages V_{AB} and V_{BC} are shown in Fig. 6.16 (d), (e). The harmonic elimination feature is also achieved for harmonics under the 10^{th} order. From the three-phase current waveform shown in Fig. 6.16 (f), no DC current appears in the faulty A phase and around 1 A circulating current is found between healthy phases B and C which is consistent with the previous analysis. The maximum balanced line voltage amplitude is 476V (4.76 p.u) in this case, which extends the operation of the CHB under fault with DC voltage injection ability to provide DC breaking feature under fault conditions.

6.4.3. Dynamic Performance with the Induction Motor

To investigate the dynamics performance of the proposed fault tolerant method, the proposed fault tolerant non-symmetrical SHE strategy is adopted for induction motor control. It is noted that the proposed method is a post-fault tolerant method for the modulation process which assumes the fault situation is ahead detected. Different motor control algorithms (both V/F and flux oriented control) can be implemented with the proposed modulation scheme under fault situations.

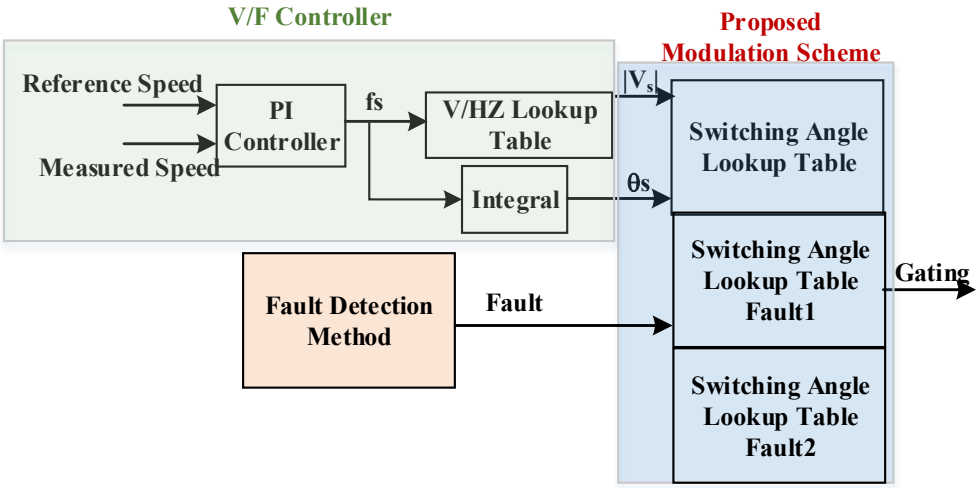
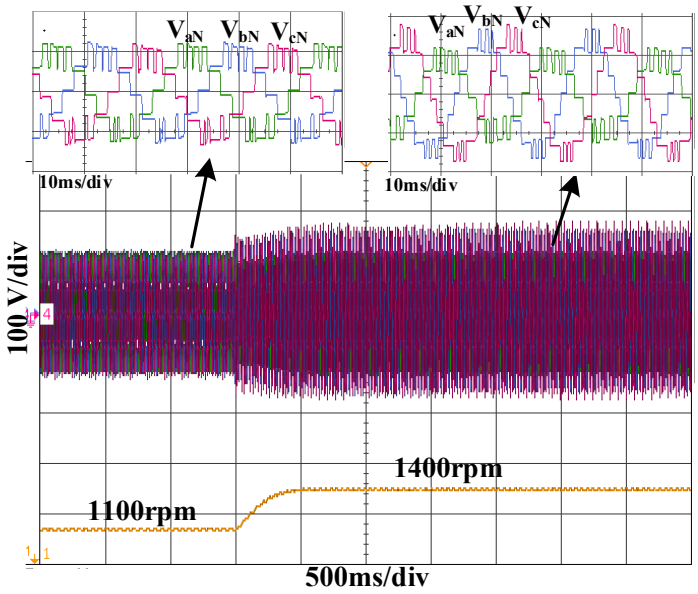


Fig. 6. 17 Fault Tolerant Controller with the Proposed Modulation Schemes

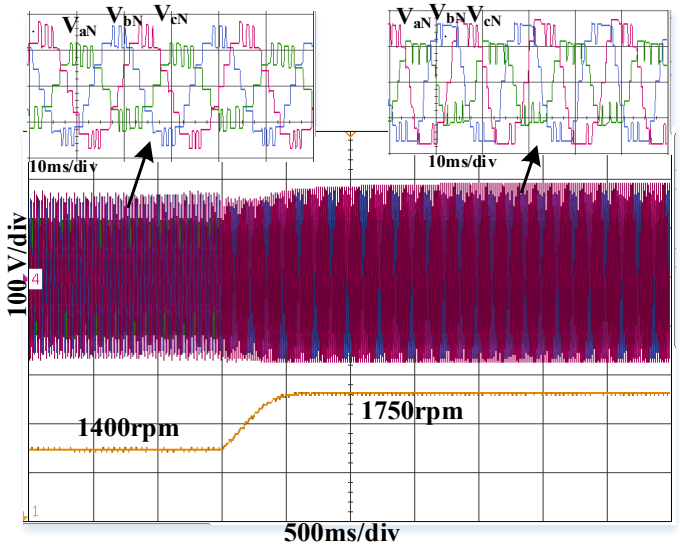
As is shown in Fig. 6.17, the V/F motor controller is adopted with the proposed fault tolerant modulation scheme. The V/F controller provides the output voltage amplitude and phase angle to the modulation process. The fault detection module offers the fault information, based on which to determine a suitable switching angle table. The switching angle lookup tables are off-line pre-calculated and stored in the memory ahead with different fault cases.

The proposed fault tolerant method is performed on an inductance motor with one cell failure in phase A. The average DC bus voltage of the healthy cell is kept at 60 V to match the induction machine voltage rating. As is shown in Fig. 6.18 (a), the speed of the induction machine can increases from 1100 rpm to 1400 rpm within 0.5 s. The output voltage waveforms respond quickly to achieve a higher balanced output voltage under the fault situation. The output voltage frequency increases from 37 Hz to 47 Hz. In Fig. 6.18 (b), the output line voltage magnitude further increases to the maximum output voltage at 60Hz under one cell failure. The induction machine is rotating at rated speed 1750 rpm. The proposed fault tolerant method shows a good

dynamic performance under fault case. The DC bus contains voltage ripple, which is caused by instantaneous power unbalance [34]. This voltage ripple is minor compared with the DC component and can be alleviated by increasing the DC voltage and the DC capacitance.



(a) 1100rpm to 1400 rpm



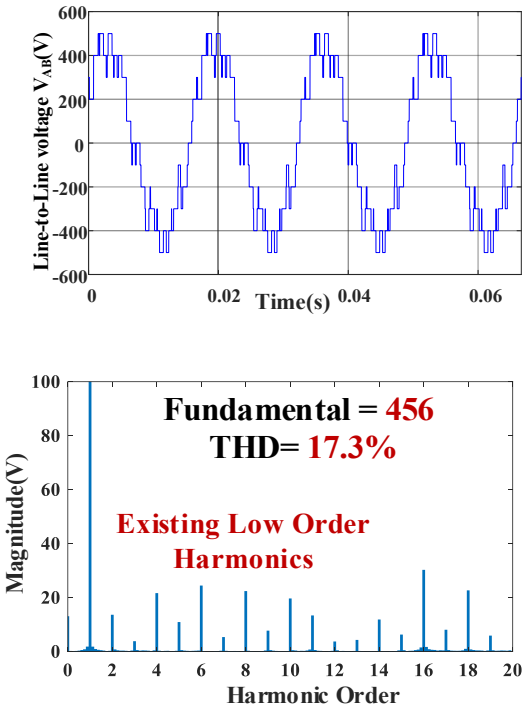
(b)1400 to 1750 rpm

Fig. 6. 18 Dynamic performance of the Proposed Motor Control Scheme

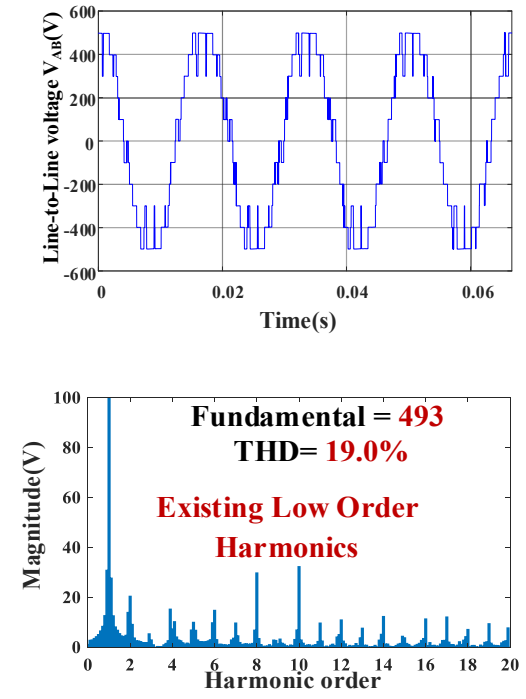
6.4.4. Discussion

To make a fair comparison between different post-tolerant state-of-art techniques in CHB drives, the maximum output voltage waveforms and line voltage harmonic profile are obtained under the one cell fault case under the same average switching frequency 100 Hz.

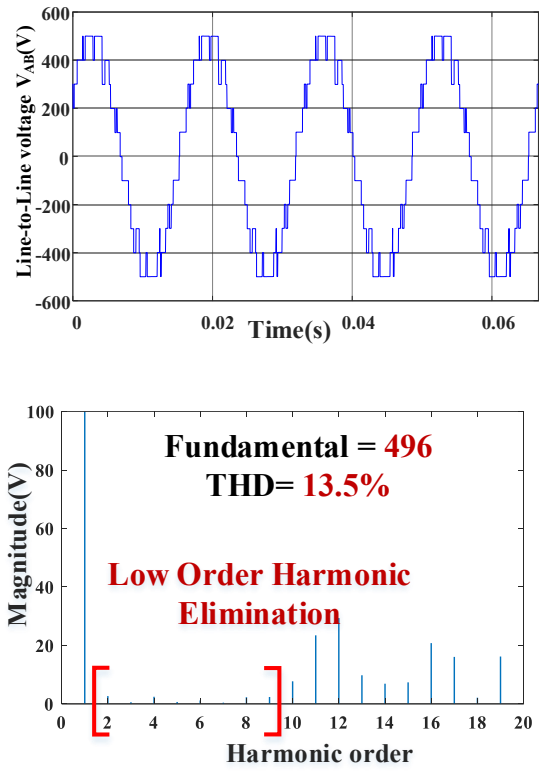
As is shown in Fig. 6.19 (a) (b), one cell failure in a seven-level CHB drive, the FPSC-PWM method [87] [96]can provide 4.56 p.u line voltages with a line voltage THD to be 17.3%. The enhanced FPSC-PWM technique [88] [98] can maximize the linear modulation region and extend the maximum line voltage to 4.93 p.u with the sacrifice of the output harmonic profile. The output line voltage THD deteriorates to 19%. This is understandable since harmonics are directly injected into modulation waveforms during the modulation process to extend the output voltage range. With a low switching frequency, both the FPSC-SPWM method and the enhanced FPSC-PWM method will lead to unacceptably low order harmonics and thus high THD. It has to be mentioned that a higher line voltage can be achieved if overmodulation operation is allowed. However, overmodulation is not considered for all methods in this comparison. The proposed FPSC non-symmetrical SHE method can provide the maximum output line voltage at 4.96 p.u with a reduction on the output line voltage THD to 13.2%. Compared with the FPSC-SPWM [87] [96] and enhanced FPSC-SPWM method [88][98], the proposed fault tolerant method is more desirable for medium voltage drives operating at a low switching frequency in terms of both the output line voltage range and the harmonic profile.



(a) FPSC-PWM Method [87][96]



(b) Enhanced FPSC-PWM Method[88][98]



(c) Proposed FPSC non-symmetrical SHE Method

Fig. 6. 19 Line Voltage Harmonic Profile Comparison under the Same Fault Case

Compared with the existing FPSC half-wave symmetry SHE method in [106][107], the variable switching angles in non-symmetrical SHE are two times than half-wave symmetry SHE while the same orders of harmonics can be eliminated. With an extra degree of freedom provided by the non-symmetrical SHE method, the obtained maximum balanced output line-to-line voltages are increased from 4.59p.u to 4.96p.u while keeping a good harmonic profile. Meanwhile, the DC braking current between healthy two phases can be provided to support the machine during the braking operation. The comparison of different fault tolerant methods under a low switching frequency operation (100Hz) is summarized in Table 6.4.

Table 6. 4 Comparison of Different Fault Tolerant Methods under One Cell Failure

	Bypassed Cell	FPSC-PWM[87][12]	Symmetry SHE [22][23]	Enhanced FPSC-PWM[4][14]	Proposed Method
Max. Output Voltage	3.47 p.u	4.56 p.u	4.59 p.u	4.93 p.u	**4.96 p.u**
Voltage Drop	33.3%	12.1%	11.6%	5%	**4.4%**
Line Voltage THD	27.2%	17.3%	13.2%	19%	**13.2%**
DC Component Control	Yes	Yes	No	Yes	**Yes**

6.5. Conclusion

This chapter proposes an automated post-tolerant optimization framework based on the non-symmetrical SHE technique to improve the reliability of CHB drives in high power application. Compared with existing post fault-tolerant methods, the proposed method is more desirable for medium voltage drives working with a low switching frequency in terms of the output line voltage range and the harmonic profile.

The non-symmetrical SHE formulation is adopted in this chapter because the non-symmetrical SHE formulation can provide an extra degree of freedom in choosing the switching firing angles, which can extend the maximum output voltage range under fault situations. And it also can provide the DC circulating current between healthy phases during braking which is not possible with the symmetrical SHE method.

Instead of direct solving the FPSC equations by assigning phase voltages, the fault tolerant problem is converted to an optimization problem based on the non-symmetrical SHE formulation. The automated optimization framework can assure the maximum balanced output voltage range with a good harmonic profile if the proper output voltage waveforms are

determined. Furthermore, the proposed method can be easily implemented with the lookup tables for motor control under fault cases.

APPENDIX

Appendix Table 6. 5. Optimized Gate Switching Angles with no DC Injection

i	1	2	3	4	5	6	7	8	9	10
α_i(degree)	4	31	62	67	91	99	130	134	151	172
β_i(degree)	7	16	49	65	75	138	141	143	157	174
γ_i(degree)	15	17	40	92	99	117	130	139	161	179
i	11	12	13	14	15	16	17	18	19	20
α_i(degree)	188	208	226	230	261	269	294	299	329	356
β_i(degree)	180	200	220	230	243	261	268	320	342	346
γ_i(degree)	188	202	217	219	222	284	295	311	345	352

Appendix Table 6. 6. Optimized Gate Switching Angles with DC Injection

i	1	2	3	4	5	6	7	8	9	10
α_i(degree)	7	34	59	64	94	99	131	137	150	170
β_i(degree)	8	15	49	66	74	128	131	141	156	177
γ_i(degree)	18	21	55	79	91	109	130	134	151	179
i	11	12	13	14	15	16	17	18	19	20
α_i(degree)	190	210	223	229	261	266	297	302	326	353
β_i(degree)	183	208	230	236	254	271	282	306	339	342
γ_i(degree)	182	203	220	243	245	283	291	311	345	351

Chapter 7

Summary and Future Work

7.1. Summary

This dissertation researches the feasibility of the regenerative CHB drive for future medium-voltage regenerative industrial drive domain in terms of reducing the grid-tied filter size, shrinking the DC link capacitors, improving the system's performance and reliability through advanced control techniques.

7.1.1. Optimal Filter Design

To comply with IEEE std 519-2014 grid harmonic standard, a filter bank is required to be designed between the AFE and the grid in each power cell of the regenerative CHB drives to attenuate current harmonics. Reducing the required filter bank is the first challenge for the regenerative CHB drive system in terms of cost, volume, and thermal dissipation. To design an optimal filter for a seven-level regenerative CHB drive, five types of filters have been studied including L Filter, LCL Filter, proposed Methods 1, 2, and 3.

This dissertation first studies the conventional L filter design strategy at different switching frequencies. It is shown that it requires the AFE IGBTs to operate at over 3000 Hz with a largely designed L filter to meet this IEEE std 519-2014 requirement. However, to reduce the system cost and increase the system efficiency, it is desirable to operate the high-power MV CHB drive at a lower switching frequency with a smaller filter bank. This lead to the investigation of an LCL filter solution.

To design an optimal LCL filter for a regenerative CHB inverter, an optimization framework is proposed directly based on the Simulink nonlinear model and genetic algorithm (GA). Instead of the tedious mathematical model, the proposed optimal LCL filter design strategy takes grid interaction, PLL performance, controller saturation into consideration while designing the filter. Simulation validates the performance of the designed LCL filter using a seven-level regenerative CHB motor drive. The designed LCL can meet the IEEE std 519-2014 filtering harmonics requirements operating with 1980 Hz switching frequency and 1100 V DC voltage, which cannot be achieved with the conventional L filter strategy. However, considering the number of power cells in a CHB drive, a large number of passive components are required for the system, which increases the overall cost and size of the CHB regenerative drive system. Although, with a good filtering performance, these LCL filters are not best suitable for the regenerative CHB drives in terms of cost, weight, and heat issue. This lead to the study of new filter design strategies with a simplified filter structure and minimum filter size as well.

For conventional passive filtering strategies, the current harmonics are determined by the voltage harmonics and the filter transfer function. However, it is noted that the output voltage harmonics from the SPWM modulation only locate at specific sideband frequencies. In other

words, to meet the IEEE std 519-2014 current harmonics standard, high filtering capability is only required around the specific sideband frequency. Instead of building a conventional passive filter for the full frequency domain, three new active filtering strategies are proposed in this dissertation only to "selectively" cancel out the significant switching sideband harmonics to reduce the required filter size for regenerative CHB drives meanwhile satisfying IEEE std 519-2014. The proposed method 1 removes the sideband harmonics through the active filtering strategy by interleaving the carrier shifting angles. But it requires a trap filter at the primary side of the transformer, which is not desirable. The proposed method 2 can satisfy the IEEE standard with a small L filter by interleaving the carrier angle between different phases. However, it also gives rise up to higher-order harmonics. To solve the emerging high order sideband harmonics, method 3 is proposed which is considered the optimal design. The IEEE standards can be satisfied with a small L filter (1.47% p.u) and meanwhile, the high-order sideband harmonics around 99^{th} are removed as well with the switching frequency to be 1980 Hz. The proposed active filtering strategies are validated on a scaled-down version of a seven-level regenerative CHB drive under different switching frequencies.

7.1.2. DC-Link Capacitance Reduction

During regeneration, the reversal of regenerative power from the load motor has to be delivered by the three-phase AFEs to the grid. Otherwise, this reversal energy can accumulate at the DC-bus and consequently raise the DC link voltage above the system safety range, which is very dangerous for the drive system. Therefore, a DC-link voltage controller is required to be designed for the AFEs to stabilize the DC-bus voltage and avoid overvoltage damage during regeneration. However, with the conventional DC-Link voltage controller, only a constant power is delivered by the three-phase AFE. The instantaneous power in each power cell between the

three-phase AFE and the single-phase H-bridge is not balanced. Due to the instantaneous power unbalance, the dc-link capacitors of the regenerative power cell need to be overdesigned to maintain a stable low ripple dc-link voltage.

To reduce the dc-link capacitance, this dissertation proposes a novel closed-loop voltage ripple controller for the regenerative CHB drive without adding extra sensors. In the proposed method, dc-link voltage ripple amplitude and phase angle are accurately detected with a high-performance adaptive filter. Moreover, a latent instability issue is discussed and is avoided in the proposed controller. Through this, both the average power and pulsating ripple power are delivered through the three-phase AFE in each power cell. In this way, the ripple power is prevented from flowing across the DC-link capacitors, which reduces the required dc-link capacitance to maintains a stable dc voltage. The performance of the proposed control strategy is validated experimentally on a seven-level regenerative CHB drive. It is shown that the dc-link capacitance and dc-link voltage ripple are reduced significantly, which reduces the system's cost and improves the system's reliability.

7.1.3. High-performance FCS-MPC

Besides the filter and capacitor design challenges for the grid-side AFEs in the regenerative CHB drives, there are challenges for the motor-side cascaded H bridge multilevel inverters in terms of high-performance control. To achieve a faster dynamic response and the multi-objective performance during the control of the regenerative CHB drives, the finite control set model predictive control (FCS-MPC) method has been considered one of the most promising alternatives due to its advantages of high dynamic performance, multi-objective capability, no

need for PI regulators and PWM modulators. However, the MPC method requires a high number of computations especially for higher-level power converter topologies due to the existence of a huge amount of switching combinations and redundancies. Real-time searching for the optimal switching state among a large candidate pool at a high sampling rate is sometimes impossible with the standard commercial processors. This limitation also prevents real-time implementation of an MPC for multilevel converters with step prediction of more than one. To solve the aforementioned issues, this dissertation presents a novel high-performance FCS-MPC scheme. The proposed FCS-MPC is reformulated mathematically MPC approach to an l^2 norm optimization problem, which can be solved on-line through matrix theory. Compared with the existing MPC optimization algorithms, the proposed MPC formulation has the advantage of a substantial reduction in computational burden, no need for the weighting factors or cost functions, and thus can operate at long horizon prediction length. The proposed method is verified experimentally on a seven-level CHB inverter prototype with a three-step prediction length to demonstrate the ability and performance of the proposed method for multilevel inverters.

7.1.4. Improving the Fault-tolerant Ability

The cascaded H-bridge (CHB) converters have been widely used for medium-voltage motor drives due to their scalability and reliability features. Especially in extremely high power applications where reliability and switching power loss are more critical for the CHB drives, the SHE-PWM technique can eliminate a much higher number of harmonics with a low switching frequency and higher reliability. This advantage makes the SHE technique more suitable for CHB drives for extremely high-power applications.

A significant indicator of the reliability is the maximum balanced line-to-line voltage amplitude under fault conditions. A new fault-tolerant technique based on non-symmetry selective harmonic elimination is proposed in this dissertation. The proposed fault-tolerant strategy can increase the maximum balanced line-to-line output voltage of the CHB motor drives with a good harmonic profile under fault conditions. Moreover, a DC current component can be regulated for the dynamic braking operation besides the regeneration braking under fault. Based on the non-symmetrical SHE formulation, the fault-tolerant problem that achieves the maximum output voltage range and good harmonic profile is converted to an optimization problem, which can be solved by the proposed optimization framework. By properly selecting the output voltage waveforms, the entire converter voltage capability can be achieved under fault conditions with a good harmonic profile. The performance of the proposed method is evaluated experimentally on a 7-level CHB motor drive. The CHB drives' fault-tolerant ability and reliability performance is thus improved by adopting the proposed control technique.

These proposed advanced control techniques make the regenerative CHB drive a promising solution for future medium-voltage regenerative drive applications in terms of cost, performance, and reliability.

7.2 Future Work

There is future work to be done exploring the optimal solution for the regenerative CHB drives in terms of lower cost, higher performance, and better reliability. The research represented in this dissertation has addressed some of the fundamental problems, which gives direction for future work. This section provides an overview of some areas of future interest.

- Experimental implementation of the proposed algorithms on the regenerative CHB drive with a regenerative back-to-back induction motor system.
- Extend the proposed carrier-shifting method under unbalanced load conditions for the regenerative CHB drives. The carrier-shifting angles between different power cells can be adaptive through reinforce learning. The overall harmonic performance can be improved for the regenerative CHB drives under different working conditions.
- To further reduce the cost of the regenerative CHB drives, other new topologies can be researched in the future such as three-phase silicon-controlled rectifier (SCR).

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