

# GaN-based Non-isolated On-board Charger with Active Filtering

# **GaN-based Non-isolated On-board Charger with Active Filtering**

by

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## Descriptive Note

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## **Abstract**

Air pollution is one of the world's leading risk factors for death. And transportation is one of the largest pollution sources. Therefore, electrification becomes a necessary step in reducing air pollution and save lives. As a result, electric vehicles are becoming the future trend in automotive industries. However, there are still some of the concerns which stop consumers from purchasing electric vehicles. Charging faster and longer driving range are two factors that consumers care most. So how to solve these concerns? A high-efficiency charger could be one solution. Level 2 charger takes less time in charging than level 1. But with the lack of charging facilities right now, charging should be available in all situations.

This thesis investigates a high-efficiency on-board charger (OBC) that could be used both at residences and at charging stations. The OBC is able to operate at a wide output battery range as well. High efficiency means low losses. Therefore, the proposed topology uses the least number of components to minimize the losses as much as possible. The efficiency is further optimized by using wide bandgap device Gallium Nitride. Since Gallium Nitride shows superior performance in high power applications. The proposed OBC combines a GaN-based bridgeless totem-pole PFC with a synchronous buck converter with innovative active filtering to allow a much smaller dc-link capacitance. The carefully designed passive components occupy less space and help improve power density. Film capacitors are used to replace the conventional electrolytic capacitors since the latter do not have good reliability for automotive applications. The proposed OBC is designed with small current ripple percentage and small output voltage ripple percentage. The simulation

results show a high peak efficiency over 98% at both level 1 and level 2 charging mode. The power factor (PF) is over 0.998 and the total harmonic distortion percentage (THD %) is less than 5% at full load condition (3.3 kW). In one sentence, the charger is simple, high efficiency, works with a universal charging system, with a wide output range, and compact.

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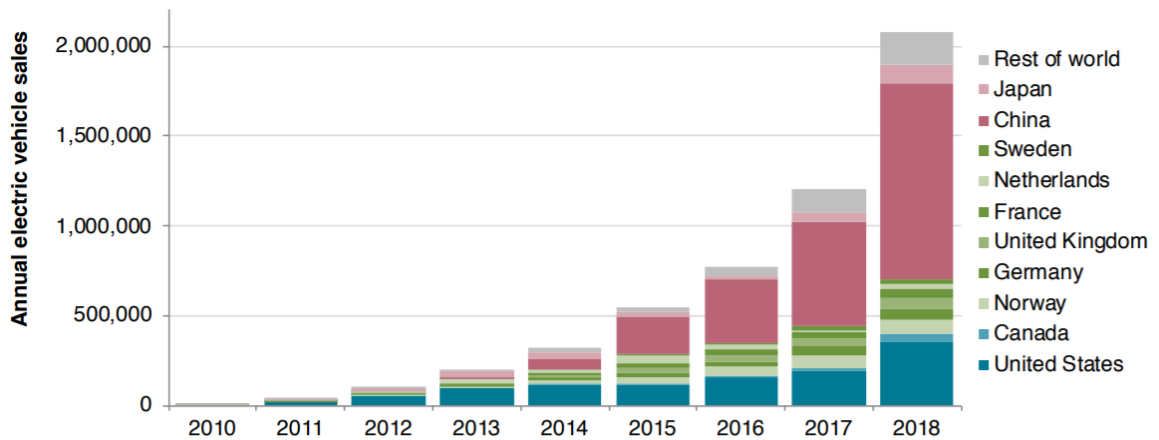
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# Chapter **1**

## Introduction

## 1.1 Background and Motivations

In the past decade, the Electric Vehicles (EVs) market is growing rapidly. Statistic reports from The International Council on Clean Transportation have shown an exponentially increasing annual sales of EVs globally, as shown in Figure 1-1. As the technology becoming more matured, previous drawbacks of EVs such as high cost, limited driving range, and long charging time are being improved continuously.



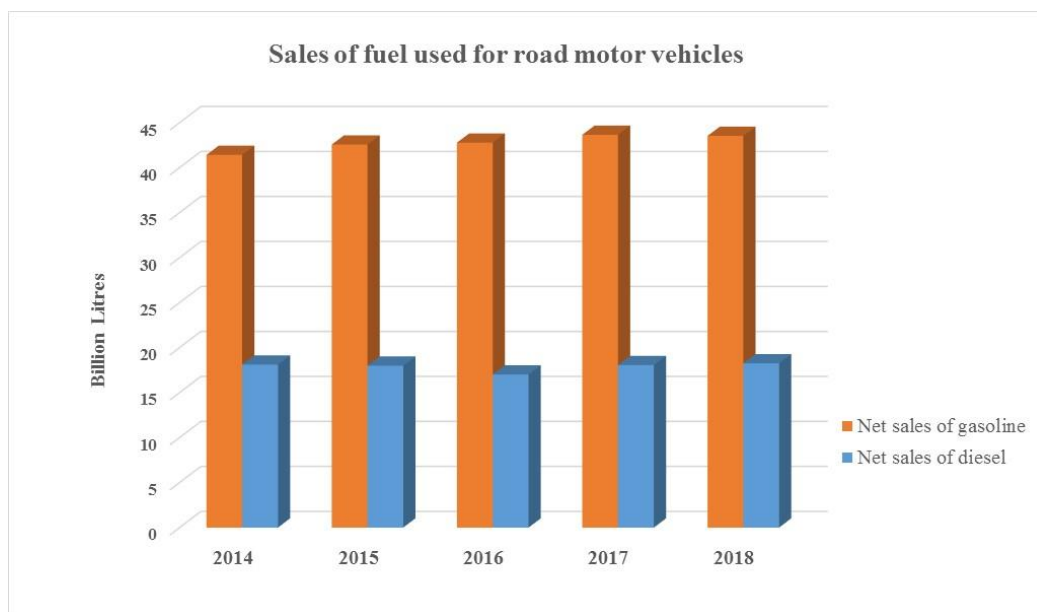
**Figure 1-1: Annual EV sales by ICCT [1]**

The major advantage of EVs is to reduce gaseous emissions. Unlike fuel-powered vehicles, the electricity that powers EVs can come from zero-emission sources like wind, solar, hydro, and nuclear power. Therefore, electrification can dramatically reduce greenhouse gas emissions to slow down global warming. A report from Statistics Canada “Sales of fuel used for road motor vehicles, annual” summarize the annual sales in liters of gasoline and diesel oil, liquefied petroleum gas from the year 2014 to the year 2018 as shown in Figure 1-2. Natural Resource Canada states that gasoline engines will produce 2.3 kg of CO<sub>2</sub> per liter of gasoline consumed and diesel engines will produce 2.7 kg of CO<sub>2</sub>



per liter of diesel fuel consumed [3]. The total amount of CO<sub>2</sub> produced from gasoline and diesel in 2018 was approximated over 150 billion kg using equation (1 - 1). The replacement of fuel power vehicles is a necessary step to protect the environment in the near future.

$$CO_2 = 44.53 \text{ billion } L \times 2.3 \text{ kg } / L + 18.26 \text{ billion } L \times 2.7 \text{ kg } / L = 151.721 \text{ billion } kg \quad (1 - 1)$$



**Figure 1-2: Sales of fuel used for road motor vehicles from Statistics Canada [2]**

The key components of EVs are demonstrated in Figure 1-3 from the source of the office of Energy Efficiency & Renewable Energy [4]. Battery charger is one of the essential modules in EVs. There is a growing interest in high-power-density and high-efficiency battery chargers for EVs, particularly OBCs in terms of energy efficiency and space savings in the vehicle. OBCs with high efficiency will shorten the charging time for a given driving distance. For example, the average vehicle efficiency for Chevrolet Spark EV 21 kWh is around 16.1 kWh/100km [5]. The time to charge an EV in order to drive for 300km with a

90% and a 98% efficiency OBC is calculated in (1 - 2) and (1 - 3), respectively. In another point of view, OBCs with high efficiency will extend the driving distance within a fixed charging time. After 3 hours charging with a 90% and a 98% efficiency OBC, the driving distance can reach 110.68 km and 120.52 km, respectively. The calculation is shown in (1 - 4) and (1 - 5). The limitation of the driving range or long charging time is the major concern for customers not choosing EVs. Therefore, a good OBC makes a critical step in making the EVs market more competitive. Furthermore, an efficient OBC will make the electric grid more efficient which allows the savings in both costs and emissions.

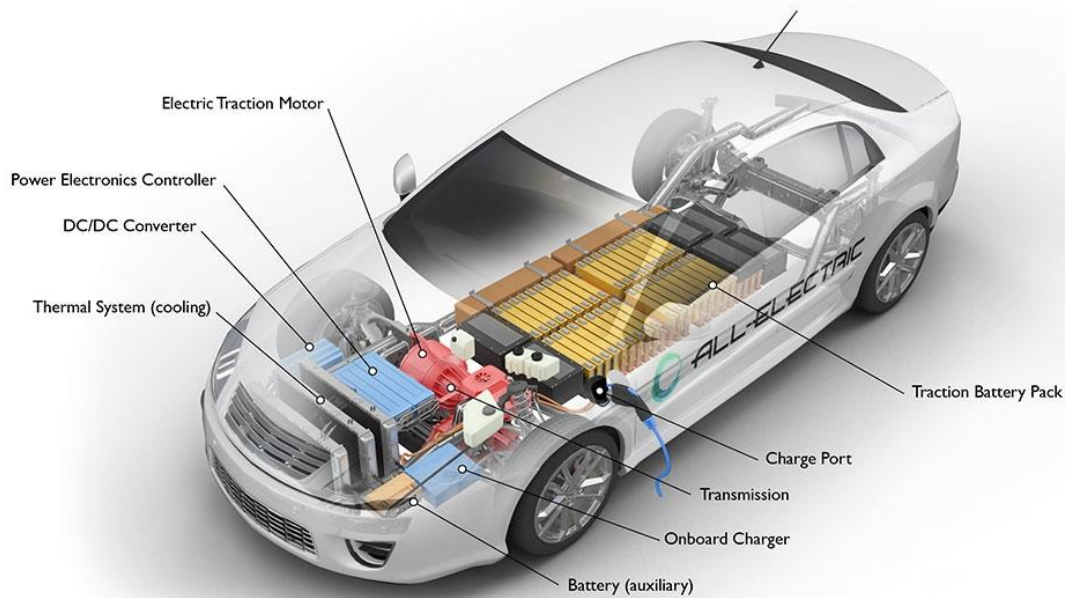
Moreover, the highly efficient OBC would allow a more compact design that is not limited to the EVs market. It can be applied to broader applications in electro-mobility. For example, e-bikes, e-scooters, electric hoverboards, etc. are other possible applications since these applications are especially sensitive to efficiency, weight, and cost. In terms of energy saving, and efficient OBC also means less waste from the grid.

$$T_{charging} = \frac{16.1kWh \times 300km}{100km \times 6.6kW \times 0.9} = 8h8m \quad (1 - 2)$$

$$T_{charging} = \frac{16.1kWh \times 300km}{100km \times 6.6kW \times 0.98} = 7h28m \quad (1 - 3)$$

$$D = \frac{3h \times 100km \times 6.6kW \times 0.9}{16.1kWh} = 110.68km \quad (1 - 4)$$

$$D = \frac{3h \times 100km \times 6.6kW \times 0.98}{16.1kWh} = 120.52km \quad (1 - 5)$$



**Figure 1-3: Key Components of an All-Electric Car [4]**

## 1.2 Contributions

This thesis presents a non-isolated OBC topology which gets rid of the large and costly transformer in conventional isolated OBCs. The safety concerns are analyzed to ensure that the proposed topology can meet the EVs' safety standards. The proposed OBC can be used for level 1 or level 2 charging systems. Level 1 charging (120 Vac) has a maximum of 1.92 kW output power because the current that can be drawn from the grid is limited to 16 A. It may take 16 hours until fully charged. Level 2 charging (208 Vac~240 Vac) is often run at 3.3 kW or 6.6 kW. The experimental prototype is built for the 3.3 kW power level, and two converters in parallel can be used to achieve the 6.6 kW level. At 3.3 kW, it takes approximately 8 hours until fully charged [6].

The proposed topology has used the least number of components to achieve a high efficiency compared to other OBC topologies. The total number of switches used is six,

where two of them are power MOSFETs, and four of them are GaN E-HEMTs. No diodes are used in this proposed topology. For passive components, there is one input power inductor, one dc-link capacitor, one output inductor, and one output capacitor. The reduced number of components help to eliminate cooling systems, lower the costs, and save the space.

This work proposes an active filtering strategy at the intermediate DC bus to reduce capacitance requirements. Thus, film capacitors can be used instead of electrolytic capacitors. This is a major advantage as electrolytic capacitors have poor reliability, meaning they are a poor option for automotive converters. Since film capacitors are generally large, allowing a small portion of ac voltage across the capacitor reduces the capacitor size a lot. The output voltage ripples are canceled by utilizing part of the proposed topology rather than adding additional compensators. Additional components always come along with additional costs. Therefore, the proposed topology is highly efficient.

### **1.3 Outline of the Thesis**

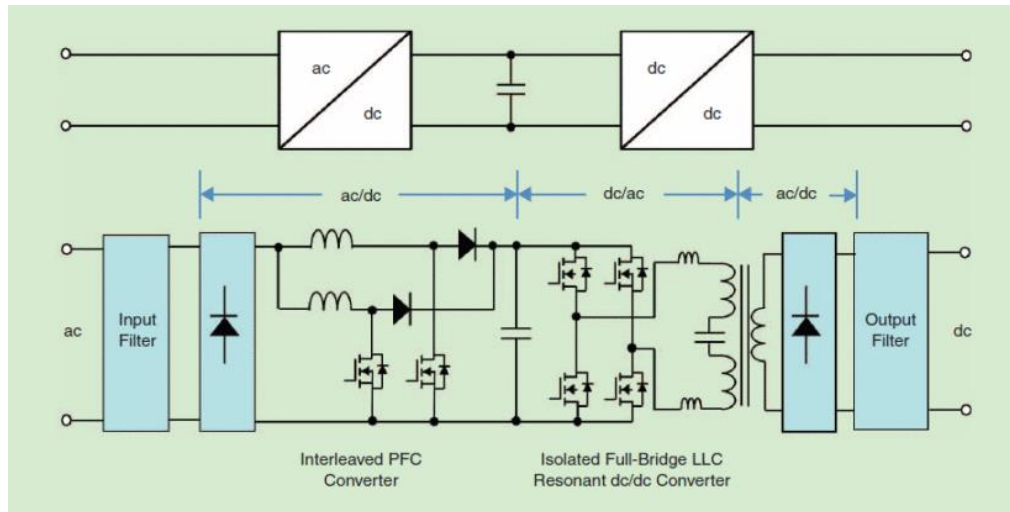
This thesis is organized into six chapters. Chapter 1 has given the background and motivation for the design of OBCs in EVs. Chapter 2 introduces the review of isolated and non-isolated OBCs that have been proposed in the literature. The topologies are analyzed based on advantages and disadvantages, or potential for improvements. Some of the topologies have shown superior performance over the others and can be used as part of the proposed topology in this thesis. Chapter 2 also includes some of the active filtering techniques as well as synchronous rectification. Chapter 3 discusses the proposed single-phase non-isolated OBC for EVs. The uniqueness of the proposed topology is clarified from

different aspects, including efficiency, number of components used, the use of film capacitors, ease of implementation, control strategy, etc. Chapter 3 also explains the principles of topology in detail. Chapter 4 discusses the design process and completes topology validation in PLECS, an electronic circuit simulation software. The electrical component models have been modified to match the real components, especially the GaN E-HEMTs. PLECS model from GaN Systems with model number: GS66516T is used in the simulation to ensure the accuracy of the simulation results. Simulation results that including efficiency, PF, THD%, are presented in Chapter 4 as well. Chapter 5 discusses the hardware design process, including printed circuit boards (PCBs) design, design layouts considerations and thermal management. The proposed topology is built in Altium Designer, an electronic design automation software package for PCBs. Chapter 5 also included open-loop experimental results. Chapter 6 gives the summary and future work.

# Chapter 2

## Review of EV On-Board Chargers

Most commonly, OBCs contains two power converter stages: ac-dc power factor correction (PFC) stage and isolated dc-dc converter stage that transforms the intermediate dc voltage to the required output dc voltage, as shown in Figure 2-1: A typical application is described in [7] where General Motor's second-generation (Gen2) OBC for the 2016 Chevrolet Volt is introduced. A diode bridge and interleaved boost PFC converter are used for ac-dc conversion and PFC. A resonant LLC converter is used as a better dc-dc converter candidate compared to Phase Shifted Full Bridge Converter (PSFB) [7]. PSFB converter uses a fixed frequency pulse-width modulation (PWM) switching technique that makes use of parasitic elements to achieve zero voltage switching (ZVS) to eliminate turn-on switching loss. While LLC converter uses a more complex control technique to achieve both ZVS and zero current switching (ZCS) over the entire operating range to further reduce the switching loss at turn-off. Besides, the LLC converter requires a smaller filter size and has a more compact design compared to the PSFB converter. The total number of diodes and MOSFETs used in this topology are ten and six, respectively. Other components including two input power inductors, one dc-link capacitor, one transformer as well as input and output filters. The efficiencies at full load (3.65 kW) are 93% for the 120 Vac system and 95% for the 240 Vac system, respectively. Often, there can be a tradeoff between efficiency and the number of components. The next sections perform a literature review to discuss different PFC topologies and different dc-dc converters that can be considered to improve the efficiency, power density, or cost (by lowering component count).

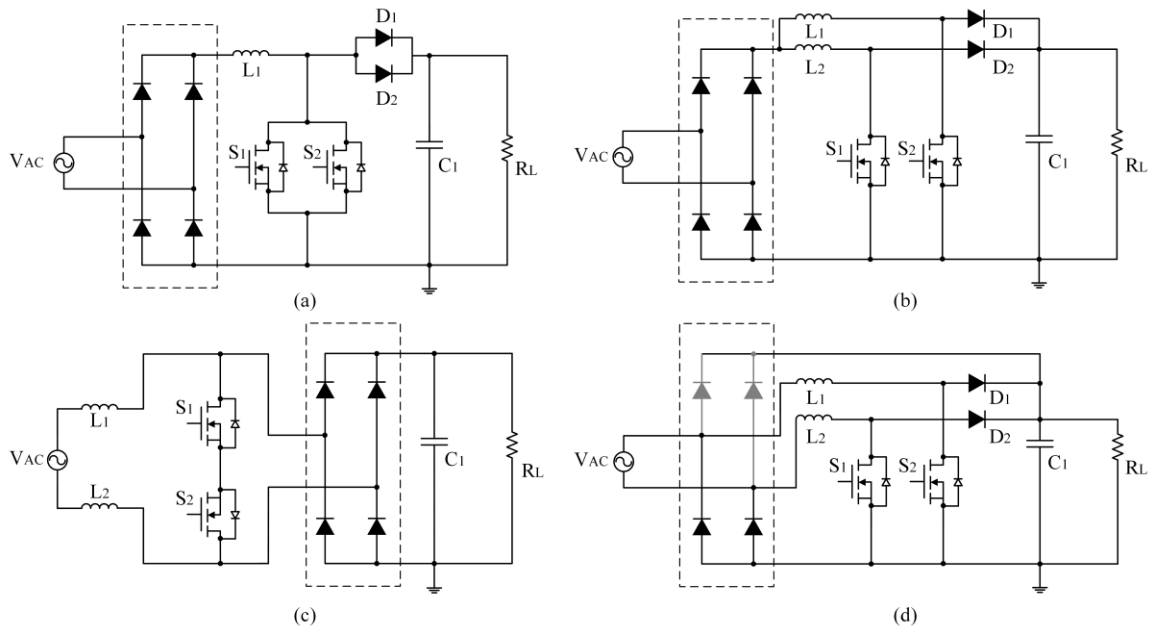


**Figure 2-1: General Motor's second-generation (Gen2) OBC for the 2016 Chevrolet Volt [7]**

## 2.1 PFC Topologies for Single-Phase OBCs

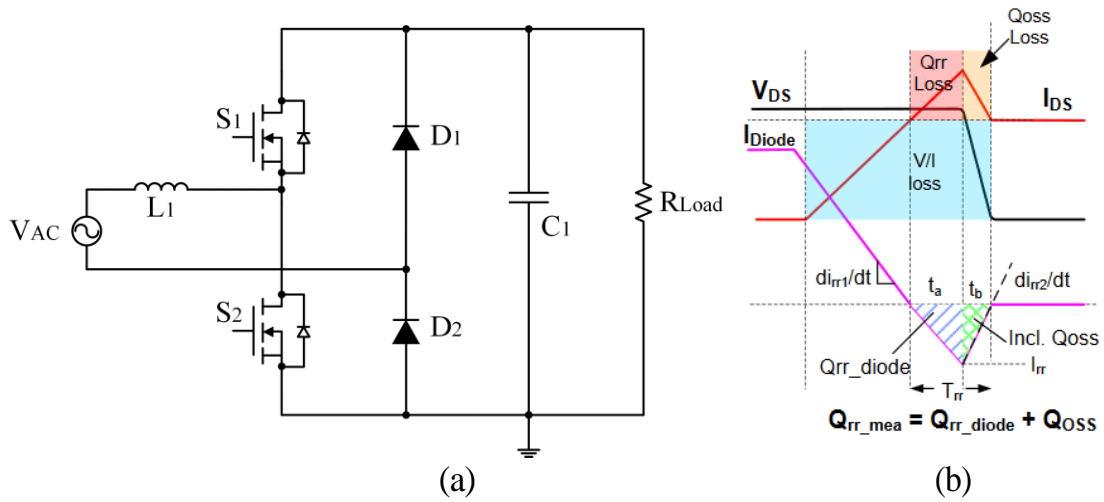
Reference [8] presents a comparative analysis of different types of PFC topologies, including a conventional average current mode control boost (ACM) PFC, an interleaved boost PFC, a back-to-back bridgeless (BTBBL) boost PFC, and a semi-bridgeless (SBL) boost PFC as shown in Figure 2-2. ACM PFC has the best performance in terms of PF. BTBBL PFC shows the lowest input ripple current. Reference [8] concludes that SBL PFC is the best option in terms of overall performance. SBL PFC has the highest efficiency over the entire load range, with a peak efficiency of 98.14% and full load (2 kW) efficiency 97.91%. However, this topology needs six diodes and two MOSFETs, as shown in Figure 2-2 (d). The two diodes on the common cathode side of the H-Bridge are used as inrush diodes. The total number of switches and diodes are the same as in the interleaved boost PFC. There are no apparent improvements in terms of component numbers.





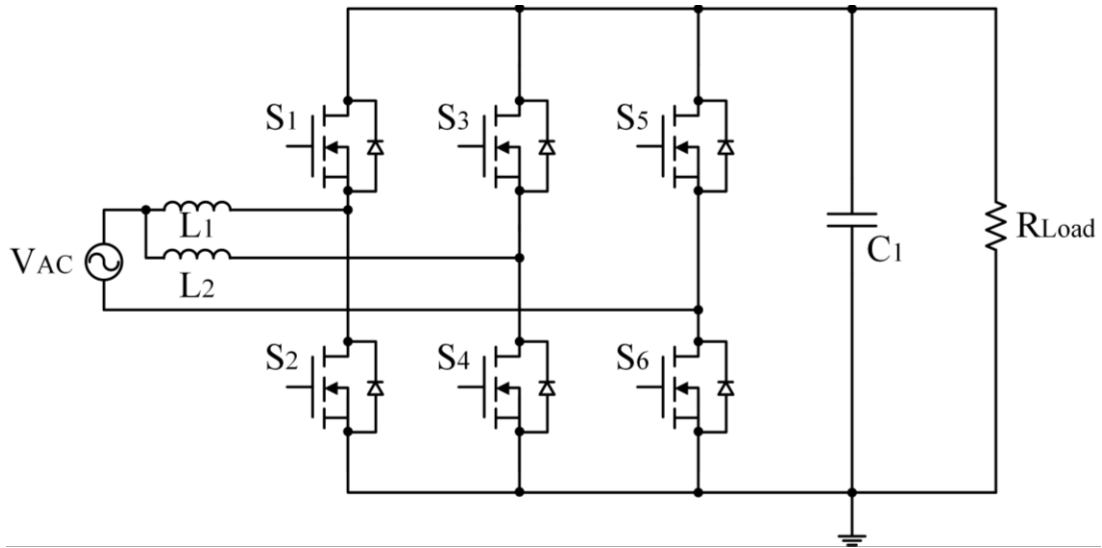
**Figure 2-2: (a) ACM PFC; (b) Interleaved PFC; (c) BTBBL PFC; (d) SBL PFC [8]**

To further reduce the total number of components and to boost the efficiency even more for the PFC stage, a bridgeless totem-pole PFC converter can be used as the front-end stage of an OBC. The conventional bridgeless totem-pole PFC topology is shown in Figure 2-3 (a). This topology has the least number of components: two silicon (Si) MOSFETs and two-line rectification diodes. While operating in continuous conduction mode (CCM) under hard switching conditions, huge turn-on loss and parasitic ringing due to the reverse-recovery effect of the intrinsic body diode of Si MOSFETs make this topology impracticable for high power applications. Figure 2-3 (b) demonstrates the impact on turn-on loss due to body diode reverse recovery. To avoid body diode conduction, totem-pole PFC with Si MOSFETs must work in CRM/DCM modes [9]. However, the increased current ripple still leads to higher conduction and turn-off loss [10].



**Figure 2-3: (a) Conventional bridgeless totem-pole PFC with Si MOSFETs; (b) Body diode reverse recovery loss [9]**

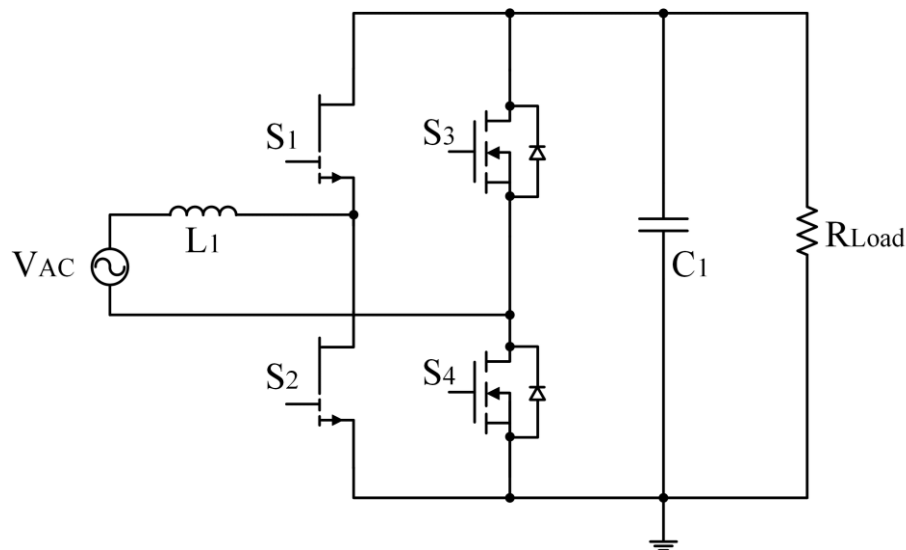
The introduction of wide bandgap (WBG) devices such as Silicon-Carbide (SiC) and Gallium-Nitride (GaN) have made this nearly abandoned totem-pole topology popular again. A SiC-based bridgeless totem-pole interleaved PFC is implemented in [11], as shown in Figure 2-4. Six SiC MOSFETs are used in total, with two SiC MOSFETs working as the replacements of line rectification diodes. The maximum efficiency of the converter can reach up to 99.2% with a 0.99 PF. The efficiency at full load (3.3 kW) for a 220 Vac system can reach 98.5%. However, hard switching frequency is restricted in CCM because switching loss is directly related to switching frequency. The same PFC topology using SiC MOSFETs, which operates in the CRM to realize zero-voltage switching (ZVS), is implemented in [12]. The soft switching technique allows the switching frequency to go beyond 300 kHz compared with 100 kHz at hard switching. The efficiency is around 98.2% at full load (6.6 kW).



**Figure 2-4: SiC-based bridgeless totem-pole interleaved PFC [11]**

Similar to the advantages of SiC MOSFETs, GaN has lower gate and output capacitance, shorter turn-on/turn off time, and lower conduction loss due to smaller turn-on resistance  $R_{ds(on)}$  [13]. One unique property that makes GaN an even better candidate in totem-pole topology is that GaN has zero reverse recovery charge. A typical GaN-based totem-pole bridgeless PFC is shown in Figure 2-5, where  $S_1$  and  $S_2$  are GaN E-HEMTs,  $S_3$  and  $S_4$  are power MOSFETs. Reference [14] provides a review of GaN-based totem-pole bridgeless PFC. A detailed comparison between hard switching and soft switching is included. The hard-switching totem-pole PFC utilizes the constant frequency pulse width modulation (PWM). Thus, the hardware design and controller is simpler. GaN-based totem-pole PFC has been proven to be able to work under hard switching mode with a 99% peak efficiency in references [9] and [15]. The efficiency at full load (3 kW) is around 98.7% in [9], while the efficiency at full load (2.4 kW) is 98.5% in [15]. However, one drawback of totem-pole PFC in CCM is that switching frequency is limited to be around or below 100 kHz to maintain a high efficiency [10]. Soft switching can improve the power density by

raising the switching frequency to a higher [16] or even to the MHz-level. GaN-based MHz CRM PFC converters are demonstrated in [10], [17], [18], and [19]. However, one issue is that only partial ZVS can be achieved when the input voltage is lower than half of the output voltage. Thus, soft switching for totem-pole PFC requires more complex controls with dual-mode operation [14]. Reference [20] proposes an adaptive soft-switching method, with a hybrid dual-loop current control, which consists of high speed instantaneous current comparison, time-based calculation, and zero current detection (ZCD) signal. Therefore, the complexity of control implementation is much higher than that of hard switching.



**Figure 2-5: GaN-based totem-pole bridgeless PFC**

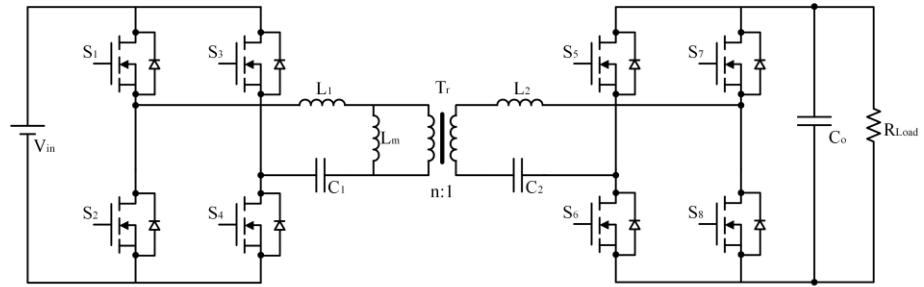
Another advantage of soft switching is to reduce the size of passive components. However, the high-frequency inductor design becomes a new challenge [14], [21]. Another issue that comes with soft switching is the high current ripple. Multiphase interleaving is a possible solution but increases the number of components and control complexity.

Therefore, both switching techniques have their advantages and disadvantages, and which one to select is based on design specifications.

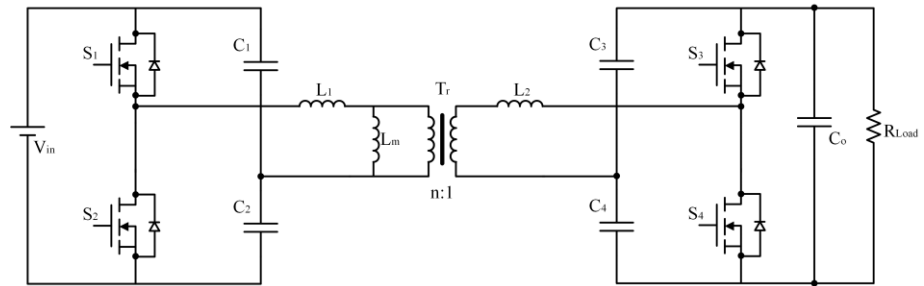
## **2.2 Isolated DC-DC Converter Topologies for OBCs**

For isolated dc-dc converters, CLLC and dual active bridge (DAB) dc-dc converters are commonly used for bidirectional EV charging systems due to high power density, efficiency, and bidirectional power flow.

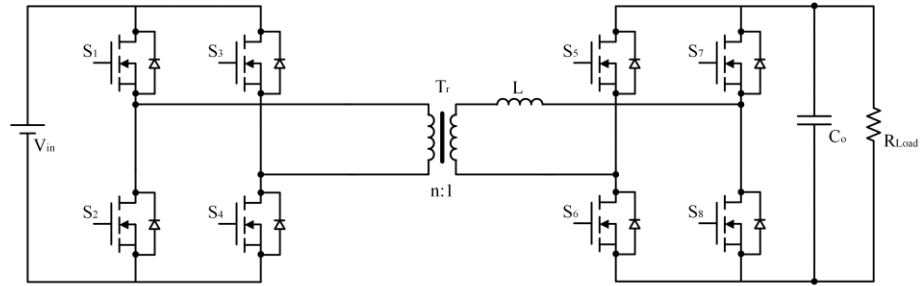
Reference [22] introduces a comprehensive analysis and comparison between full bridge CLLC (FBCLLC), half bridge CLLC (HBCLLC), full bridge DAB (FBDAB), and half bridge (HBDAB). These four topologies are shown in Figure 2-6, using enhancement-mode SiC Power MOSFETs. Based on the comparison, the efficiencies of the CLLC converters are higher than DAB converters because DAB loses ZVS at light load conditions. Besides, the single-phase shift (SPS) control strategy used by DAB creates large reactive power, which also reduces efficiency. The half-bridge structure has higher efficiency than the full-bridge structure due to the reduction of the total number of switches and, therefore, results in a smaller size and less weight. In conclusion, the HBCLLC converter has the best performance in terms of efficiency, power density, size, and cost. The efficiencies are around 96% in both charging and discharging mode at 1 kW. The power density is around 90 W/in<sup>3</sup>. However, one drawback is that the current stress is twice larger than that in the full-bridge structure. GaN based CLLC converters have been demonstrated in [23], [24] with improved efficiency.



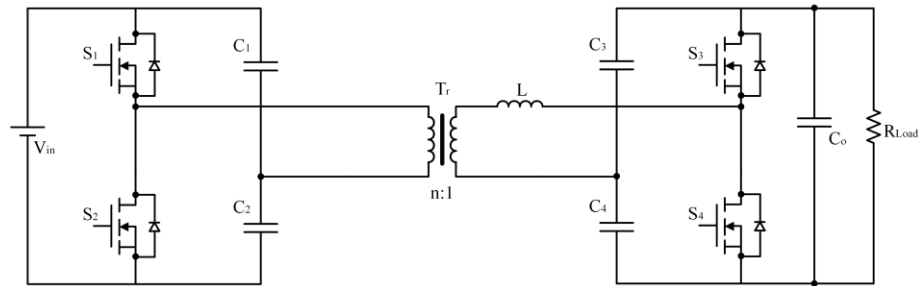
(a)



(b)



(c)

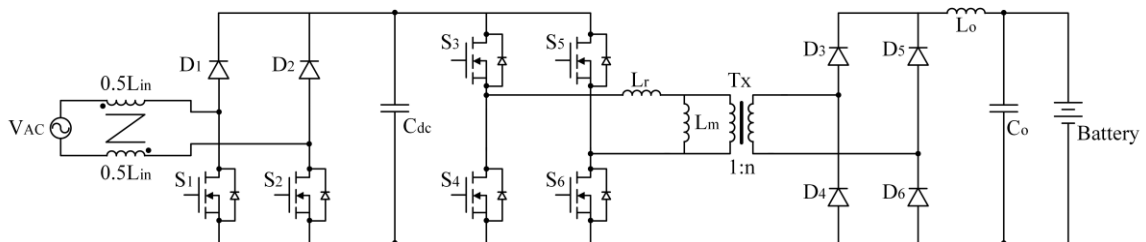


(d)

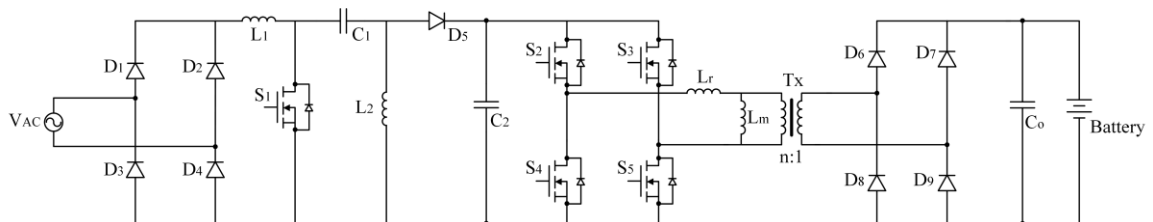
**Figure 2-6: (a) FBCLLC converter; (b) HBCLLC converter; (c) FBDAB converter; (d) HBDAB converter [22]**

### 2.3 OBCs Combining PFC and Isolated DC-DC Converters

Different combinations of PFC and dc-dc converters, as well as the use of WBG devices, make up most of the recent OBC topologies published in the literature. Reference [25] presents a topology combining a bridgeless boost ac-dc converter, and a PSFB dc-dc converter shown in Figure 2-7, utilizing SiC MOSFETs with 94% efficiency at 6.1 kW. However, PSFB dc-dc converter shows poor performance at the higher switching frequency and is forced to lower down to 200 kHz to obtain 96% efficiency. Reference [26] proposes a SiC based OBC using a single-ended primary-inductor converter (SEPIC) PFC converter, and LLC resonant converter shown in Figure 2-8. This topology has the capability of providing an ultra-wide range for the dc-link voltage to ensure the LLC converter can operate at the resonant frequency to maximize total efficiencies over the wide range of the battery pack voltage. Only one MOSFET is used in the SEPIC PFC. However, the number of passive components is doubled. The overall efficiency can only reach 93% at 1 kW.

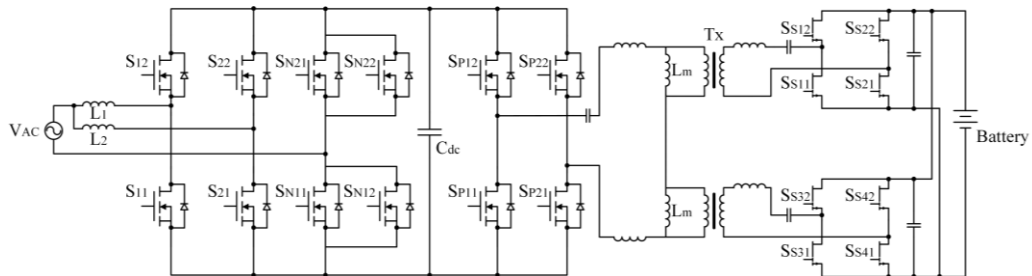


**Figure 2-7: Bridgeless boost ac-dc converter and PSFB dc-dc converter [25]**



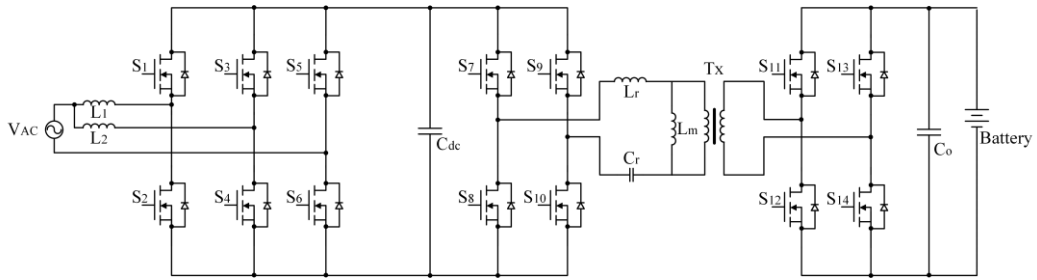
**Figure 2-8: SEPIC PFC and LLC resonant converter [26]**

Reference [12] proposes an OBC with variable dc-link voltage, which combines a totem-pole PFC with a CLLC resonant converter, as shown in Figure 2-9. This topology uses both SiC and GaN devices to achieve  $37 \text{ W/in}^3$  power density and efficiency above 96%. However, the total number of SiC MOSFETs and GaN are twenty in total. Reference [27] proposes a SiC-based bidirectional OBC with totem-pole interleaved PFC and LLC resonant converter with a similar layout as the reference [12]. And a slightly reduced number of components are used, as shown in Figure 2-10. Reference [28] presents a SiC-based three-phase interleaved totem-pole PFC with CLLC resonant converter. This topology shows a 98.9% peak efficiency and less than 2% THD. However, two more SiC MOSFETs are required in the totem-pole PFC stage compared to [27]. Reference [29] proposes a SiC-based OBC combing a boost-type PFC with two half-bridge LLC resonant converter shown in Figure 2-11. The total number of SiC MOSFETs and diodes used are ten and eight, respectively. WBG based isolated OBCs in [12], [27], [28], and [29] are costly due to the number of components used compared to other topologies at the same efficiency level. Reference [30] proposes the same idea [12] by combining a totem-pole PFC and a CLLC resonant converter but with a reduced number of switches, as shown in Figure 2-12. The power density is  $36 \text{ W/in}^3$ , and the peak efficiency is above 97%.

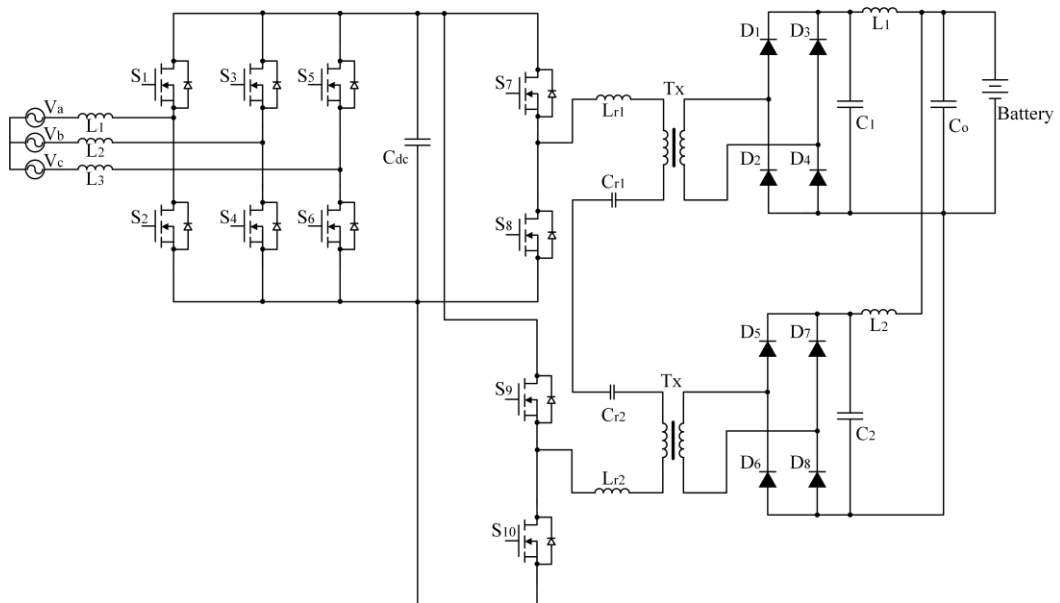


**Figure 2-9: Bridgeless totem-pole interleaved PFC and CLLC resonant converter [12]**

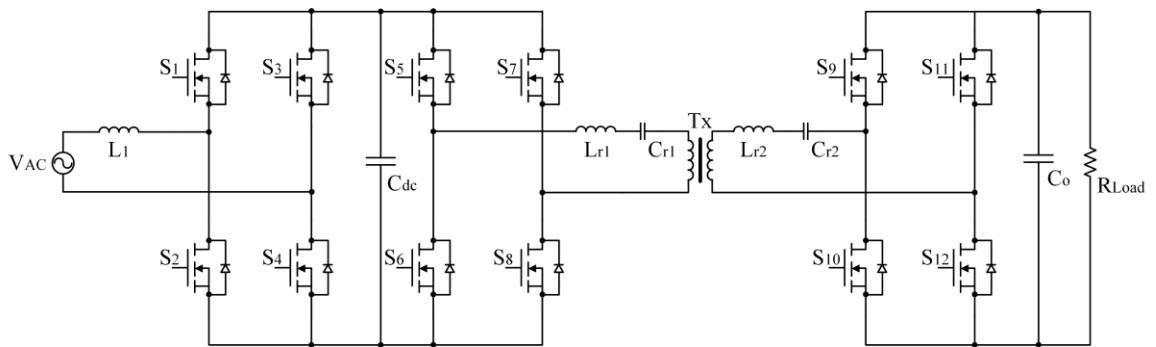




**Figure 2-10: Bridgeless totem-pole interleaved PFC and LLC resonant converter [27]**



**Figure 2-11: Three-phase boost PFC and two half-bridge LLC resonant converter [29]**



**Figure 2-12: Bridgeless totem-pole and CLLC resonant converter [30]**

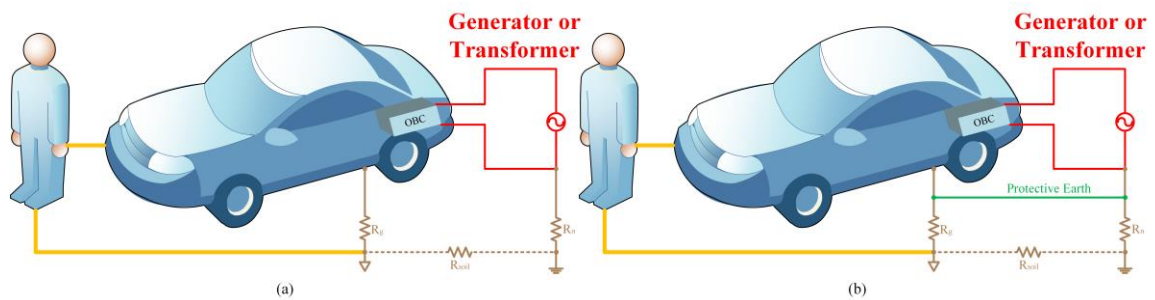
## 2.4 Safety Considerations and Solutions for Non-isolated OBCs

Low dc-dc converter efficiency is the main reason for the overall low efficiency of OBCs with isolated dc-dc converters, even with a 98-99% efficiency PFC converter, and most of the loss comes from the transformer. Non-isolated topologies can be considered since there is no requirement for isolation in standards for the safety of EVs as specified in SAE J1772 (from the North American standard for electrical connectors for EVs maintained by the Society of Automotive Engineers). Besides, there is no electrical reason that the high-voltage battery should be isolated from AC input power because its poles are generally floating with the vehicle chassis [31]. And the failure of the basic insulation of the exposed conductive parts (ECPs) does not threaten the safety of anyone in case of contact with the vehicle [32].

Safety risks must be concerned with direct contact and indirect contact. Direct contact occurs when the part that is normally live becomes accessible to touch; indirect contact happens when a piece of equipment that is not normally live becomes energized because of the failure of its basic insulation [32]. The protection against direct contact is done by providing enough insulation of live parts within the EVs, such as insulated wires and enclosures. To protect against indirect contact, the most effective way is to disconnect the EVs from the grid by means of detecting current faults all the time.

Ford discusses the negative influence and safety risks from the leakage current for integrated non-isolated OBCs [33]. The paper introduces two grounding systems: (TT) Terra–Terra or Earth–Earth grounding system, and Terra–Neutral (TN) or Earth–Neutral grounding system as shown in Figure 2-13. TN grounding system is widely adopted in

U.S.A, Canada, China, Germany, U.K, etc., where a protective earth (PE) conductor is connected with a minimum impedance between the neutral point of the substation and the vehicle chassis. The human body is always protected by the PE conductor as most of the leakage currents will go through the PE conductor rather than the human body. Therefore, ground-fault circuit interrupters (GFCIs) are optional in TN grounding system. Many manufacturers suggest GFCIs not installed at all due to nuisance tripping, unwarranted circuit breaker trips [33]. However, it is strongly recommended to have GFCIs in case of the breakdown of insulation. But, GFCIs are required in TT grounding system since they are the only protection layer to the users.

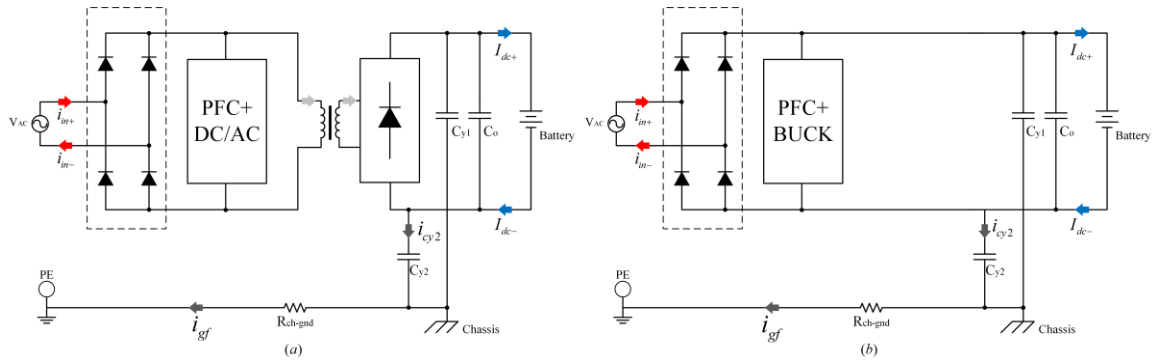


**Figure 2-13: (a) TT grounding system; (b) TN grounding system [33]**

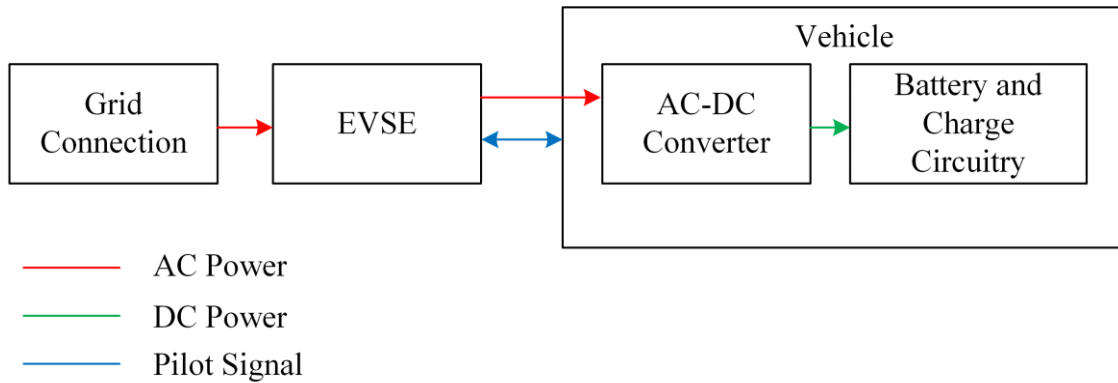
To explain the sources of ground fault current, GM compares both isolated and non-isolated OBCs with respect to ground fault current detection and interruption [34]. Ground fault current in isolated OBCs is very small due to the galvanic isolation but is relatively large in non-isolated OBCs. The ground fault current path for both cases is shown in Figure 2-14. For any grid-connected converters, electromagnetic interference (EMI) filters are installed on both sides to satisfy EMI requirements. The on-board Y capacitors ( $C_{y1}$  and  $C_{y2}$ ) are connected to the vehicle chassis as the common ground. For isolated OBCs, when current flows into the load, it also charges the capacitors  $C_{y1}$  and  $C_{y2}$ . The capacitor voltages

add up to the battery voltage. The difference in the secondary side current does not change the primary side current. Therefore, the difference between  $i_{in+}$  and  $i_{in-}$  is zero. For non-isolated OBCs,  $C_{y2}$  will be physically connected to the full bridge. The DC current,  $i_{dc-}$  will eventually charge the capacitor  $C_{y2}$ , hence the return AC current,  $i_{in-}$  will always be less than the input current  $i_{in+}$ . The RMS value of the ground current,  $i_{gf}$  will then trigger the GFCI circuit if it exceeds the threshold, normally 4~6 mA [34]. The paper also explains and compares the GFCI circuit in both cases based on the standards set by UL [35], [36]. The paper emphasizes the importance of a good GFCI circuit in both isolated and non-isolated OBCs. GFCI is a part of the electric vehicle supply equipment (EVSE) now.

EVSE can provide full protection to the vehicle from all possible faults to the ground. The position of EVSE is shown in Figure 2-15 [37]. The major function of EVSE including check whether a vehicle is connected, determine when to deliver energy, and transmit to the vehicle the infrastructure's current rating, detect hardware faults, detect electrical faults, and disconnect from the power grid to prevent battery damage. A level 1 or 2 EVSE must provide a threshold of 5 mA or 15–20 mA to meet the UL [34]. For charging in a residence, if normal non-dedicated wall power-outlets are being used, a residual current device (RCD) or GFCI should be used to ensure a safety operation. If a dedicative socket-outlet is being used, leakage current monitoring is optional, and a charging cord must have GFCI inbuilt to continuously measure the leakage current instead [34].



**Figure 2-14: Ground fault current path for: (a) isolated; (b) non-isolated [34]**



**Figure 2-15: EVSE position in power flow [37]**

## 2.5 Non-isolated OBCs

Getting rid of the transformer allows designers to combine two stages as a single one. Topologies that can achieve PFC as well as dc-dc conversions seem to become good options. A list of non-isolated topologies, including conventional buck boost (with PFC), SEPIC (with PFC), and CUK (with PFC), are compared in [31]. These topologies are shown in Figure 2-16. However, the semiconductor switches (including diodes) are under high voltage stress in conventional buck boost, SEPIC, and CUK, since they tolerate the summation of the input voltage and the output voltage during operation. Furthermore, a higher voltage rating device will have a higher on-resistance and, therefore, higher

conduction loss. And the high voltage stress leads to higher switching loss as well. To overcome the drawbacks of single-switched PFC converters, a cascaded buck boost converter with three modes of operation: buck, boost, and cascade buck-boost shown in Figure 2-17, is presented in [31]. However, the region of operation modes needs to be carefully considered following a flowchart in accordance with the input and output conditions. Reference [39] presents a two-switch buck-boost converter in average current mode (ACM), as shown in Figure 2-18. The boost and buck switches are controlled independently to provide wide output voltages. This topology shows advantages, including less number of components, wider output voltage range, and simpler mode selection compared to other existing isolated and non-isolated converters in ACM. However, the converter in buck mode has shown poor performance on PFC than boost mode, as well as high conduction loss produced by the diode bridge structure.

A study on the PFC using the buck topology by Texas Instruments indicates that there is an inherent “cross-over” distortion in the AC line current when the buck PFC stage is reverse biased. Therefore, the distortion will limit achievable THD% and PF performance. The cross-over distortion becomes less significant at a higher input voltage but more severe at a lower input voltage [39]. Experimental results from papers also show that operation in the boost mode has higher PF than in the buck-boost mode [31], [38], [40].

Another drawback is that the front-end bridge rectifier contributing to power loss which can easily consume 2% to 3% of the output power at low line voltages and at full load.

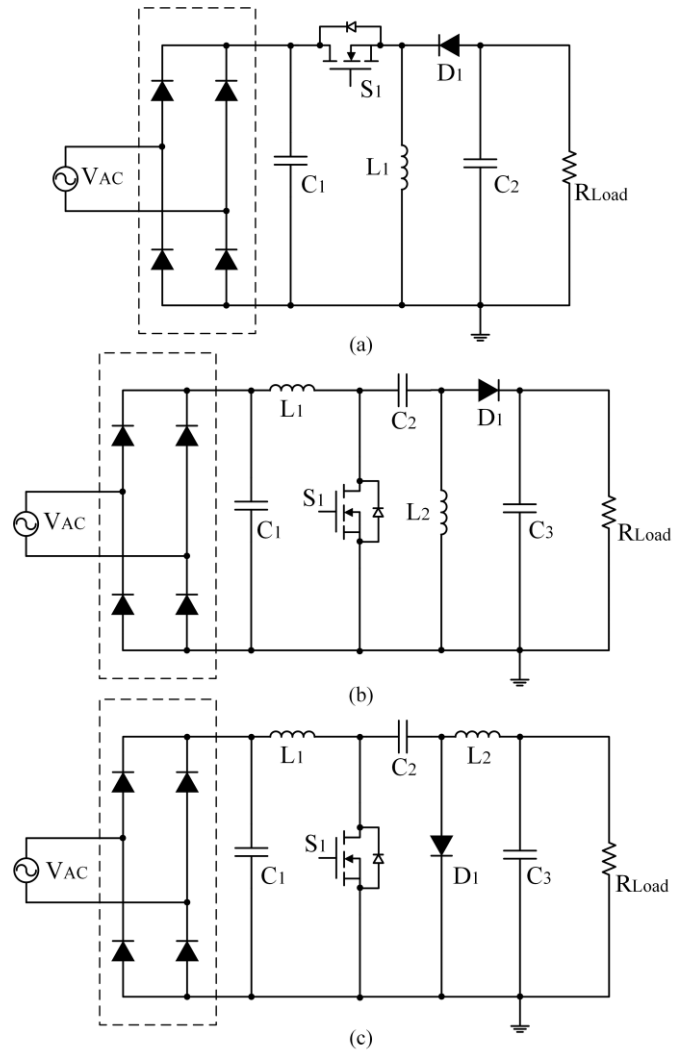


Figure 2-16: (a) Conventional buck-boost PFC; (b) SEPIC PFC; (c) CUK PFC [31]

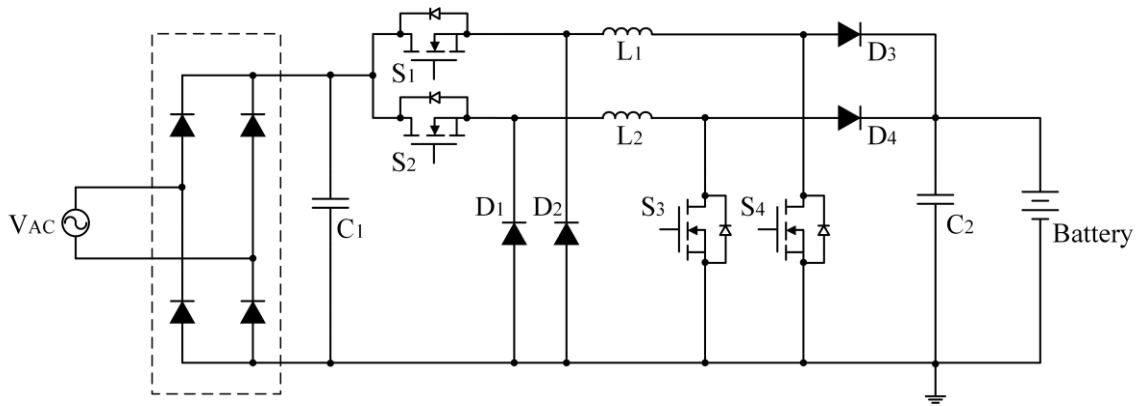
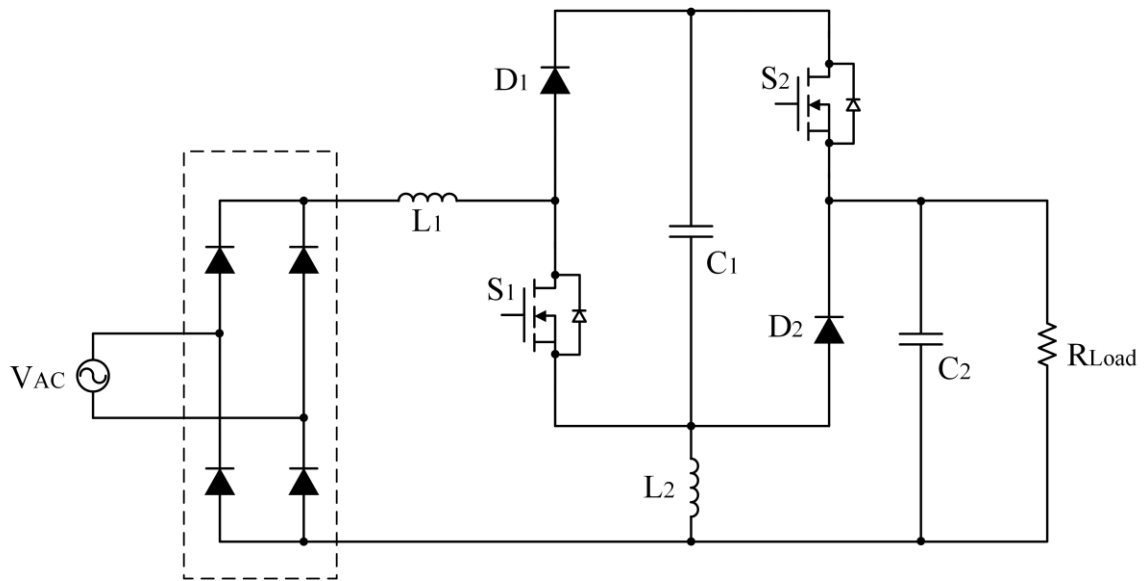


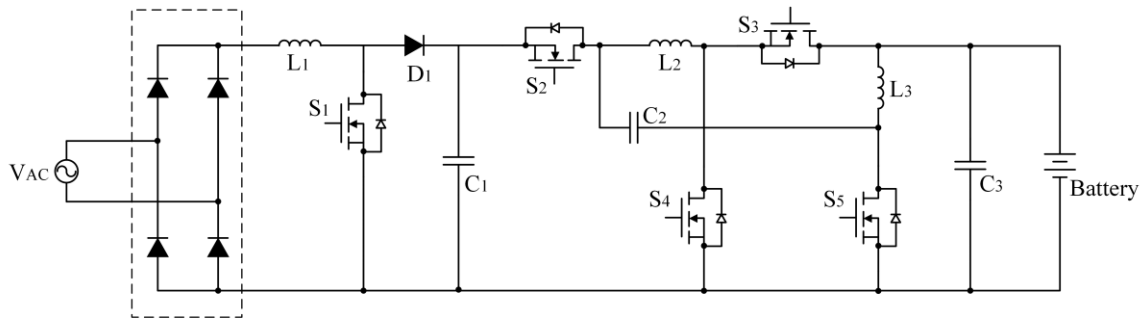
Figure 2-17: Interleaved cascaded buck-boost converter [31]



**Figure 2-18: Two-switch buck-boost converter [38]**

Because OBCs require a wide range of input and output voltages, non-isolated single-stage topologies have to utilize the buck PFC when the required output voltage is lower than the input voltage, which will impact the THD% and PF performance, as mentioned above. To avoid this issue, two stages can be used the same way as isolated OBCs by replacing isolated dc-dc converters by buck-boost converter [41], as shown in Figure 2-19, or bidirectional cascaded buck-boost converter [42]. The topology in [41] can maintain an excellent PFC performance by using boost-type PFC, as well as a wide range of output voltage with different modes of operation: buck, boost, or buck-boost. However, experimental results are not included to prove the theory. Besides, this topology uses additional passive components compared to [31] and [38]. Both the capacitor and the inductor numbers are three, therefore, a larger space is required and the power density will be reduced. Until now, few papers have discussed two-stage non-isolated OBCs.





**Figure 2-19: Two-stage non-isolated OBC [41]**

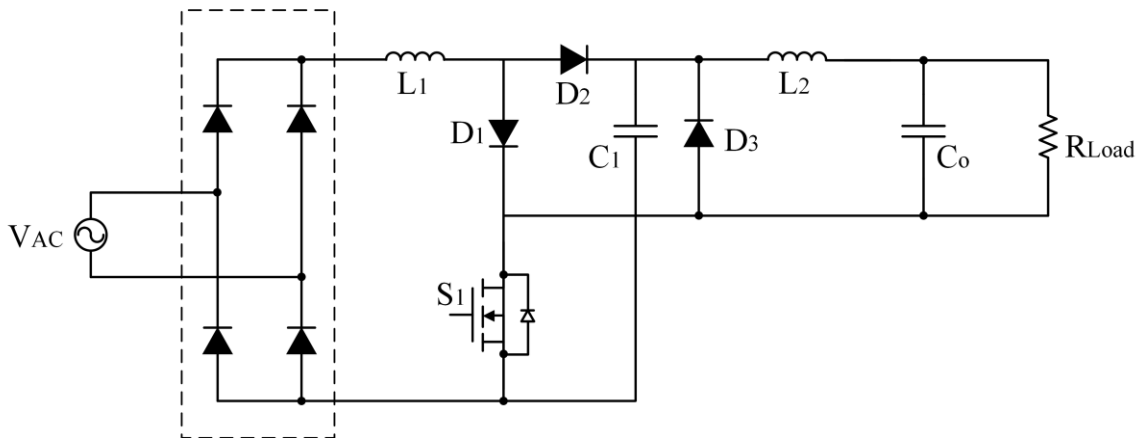
## 2.6 Active Filtering

In the design of high power density OBCs, the size of passive components must be considered. While increasing switching frequency will reduce the size of inductors, the dc-link capacitors in a two-stage topology must filter ripples at double the line frequency in a dc current charging system. Therefore, the capacitor size becomes one of the major barriers to higher power density. Film capacitors are replacing the conventional electrolytic bulk capacitors in automotive applications due to several advantages. The primary advantages of the film capacitors include higher insulation resistance, a lower dissipation factor, high-current carrying capabilities in pulse applications, better capacitance stability, and small equivalent series resistance (ESR), which contributes to the loss when high AC current is flowing. Electrolytic capacitors have a limited life expectancy to 10,000 hours, while film capacitors allow the life expectancy to be extended to more than 100,000 hours [43]. Researches have shown that the ability to handle the ripple current of film capacitors is stronger than electrolytic capacitors [44]. The main drawback of film capacitors is their low dielectric constant, which means they tend to be large in physical size than the electrolytic capacitor [45]. Researches have made continuous efforts in replacing the electrolytic

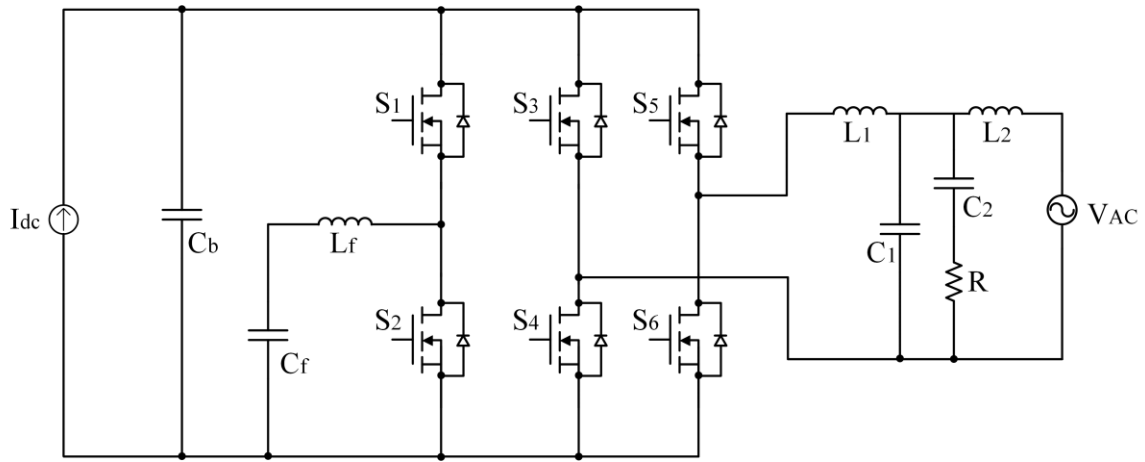
capacitors with film capacitors to improve input power quality and to enhance reliability but also with active filtering to overcome the drawback of large physical size [46], [47].

This paragraph focuses on different methods to help to reduce the size of capacitors. Reference [48] proposes a method for single-phase PFC rectifiers by merging two converters that are duty and frequency controlled. For example, integrating a boost converter and a buck converter, as shown in Figure 2-20. The number of the switch is minimum, but the number of diodes is increased compared to other PFC topologies. The capacitance of  $C_1$ ,  $C_o$  are  $30 \mu\text{F}$  and  $5 \mu\text{F}$ , respectively. However, the switching frequency is changed based on modes of operation. The calculation of switching frequencies and duty cycles for boost and buck converter is quite complicated. The experimental results show that the efficiency at 100 W output power is only 89.5%. Reference [49] achieves the active filtering with an additional compensator block but at the cost of adding more components. The compensator consists of a cascaded combination of boost and zeta converters with an energy buffer between them. When input double-frequency power is greater than the average output power, the boost converter will store the excess energy into the energy buffer capacitor. When input double-frequency power is less than the average output power, the zeta converter will release back the energy stored in the buffer capacitor to the output. Reference [50] and [51] propose the method by redistributing the unbalanced power between two series-connected intermediate capacitors to make the capacitor voltage ripple complementary to each other to cancel the ripples. However, this ripple cancellation method requires a duty ratio adjustment of four additional switches and one extra energy storage component (inductor). Reference [52] used a bidirectional buck-boost converter to

achieve active filtering by two additional switches, one capacitor, and one inductor, as shown in Figure 2-21. This paper uses a similar idea as [50], [51], where inductor  $L_f$  behaves as an energy transfer. Reference [53], [54] also use inductive storage to replace the low-lifetime capacitors. However, it will reduce the overall power density due to its lower energy density as compared to capacitive storage. All of the methods mentioned above achieve active filtering by increasing the total number of components. Without adding additional components, the dc-link capacitance will be significantly reduced if the battery pack can take the low frequency charging current ripple. This idea has been proven in [55], [56], with the result of a minor difference in battery capacity under dc charging and pulse charging. Based on these findings, reference [57] uses sinusoidal charging and allows the double line frequency ripples on the battery side. However, this may not be a good solution when considering battery life in the long run.



**Figure 2-20: Non-isolated topology by integrating a boost converter and a buck converter [48]**



**Figure 2-21: DC-AC stage with active filtering [52]**

## 2.7 Synchronous Rectification

Designers began adopting Synchronous Rectification (SR) in 1990s and use MOSFETs to achieve the rectification function which are conventional performed by diodes. SR can improve efficiency, thermal performance, power density, and decrease the overall system cost of power supply system [59].

Diodes have physical limitations that prevent the forward voltage drop goes below approximately 0.3 V. Even for SiC diode, the forward voltage is above 1.5 V as shown in Table 2-1 [60]. In contrast, the  $R_{ds(on)}$  of MOSFETs are much smaller than diodes and therefore, have a significantly smaller voltage drop at a given current than the diode [59]. The totem-pole topology as shown in Figure 2-5 is an example of SR.

SR can be applied to dc-dc converters such as boost, buck-boost, CUK, SEPIC, and zeta as well. One typical application is the buck converter. Compared to the asynchronous buck converter, the synchronous buck converter reduces power losses by substituting a power MOSFET for the commutating diode [61]. This reduces the diode drop and increases system efficiency. Reference [62] analyzed the zero-voltage-transition (ZVT) buck

converter with SR. This paper concludes that applying SR to ZVT converters can reduce conduction losses and also result in a wide soft-switching range. Reference [63] proposed a ZVS synchronous buck converter with a coupled inductor which improved the efficiency by 1.6% compared to the conventional synchronous buck converter. The low efficiency in conventional buck converter is because of the moment that the upper switch turns on, it provokes the reverse recovery of the body diode of the synchronous switch. This issue can be solved with the introduction of GaN since there is no body diode and reverse recovery effect as mentioned in the early sections. Reference [64] compared the efficiency of Si-based synchronous buck and GaN-based synchronous buck. With GaN, efficiency is increased by up to 8%. The efficiency is further boosted up with the soft switching technique proposed in [65], as well the improved thermal performance with integrated planner inductor.

**Table 2-1: SiC Schottky Diode AIDW40S65C5 [60]**

Parameter	Symbol	Values			Unit	Note/Test condition
		Min.	Typ.	Max.		
DC blocking voltage	$V_{DC}$	650	-	-	V	$T_j=25^\circ\text{C}$ , $I_R=0.12\text{ mA}$
Diode forward voltage	$V_F$	-	1.5	1.7		$T_j=25^\circ\text{C}$ , $I_F=40\text{ A}$
		-	1.8	2.1		$T_j=150^\circ\text{C}$ , $I_F=40\text{ A}$

# Chapter 3

## Proposed Non-Isolated On-Board Charger

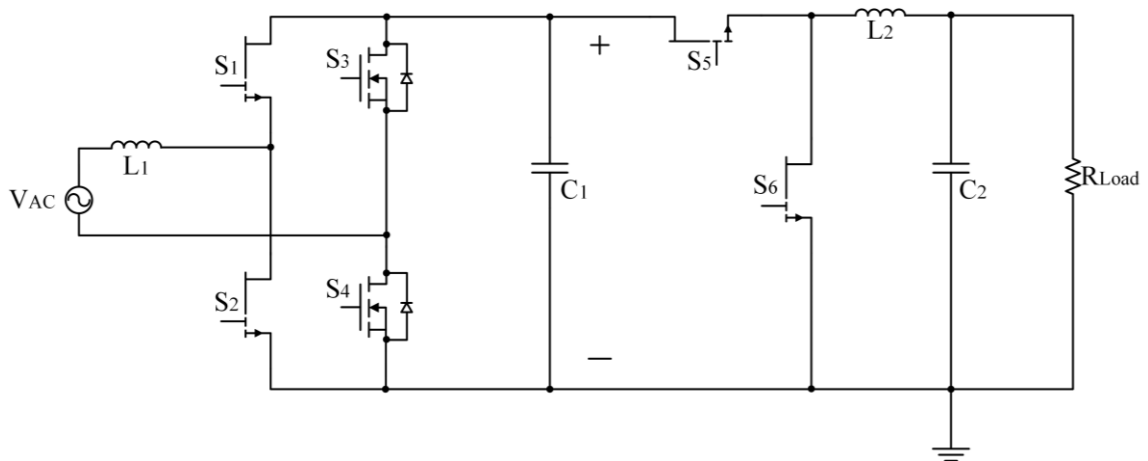
### 3.1 Proposed Topology

The goals of the proposed topology are to achieve high efficiency, high power density, excellent PFC, low THD%, and use a low number of components. An active filtering technique is introduced to lower the capacitance required, thus allowing the use of film capacitors rather than electrolytic capacitors, due to the reliability of electrolytic capacitors. Automotive industry would not use electrolytic capacitors in OBCs, so that the proposed OBC has advantage to other papers that use electrolytic capacitors in their experiments. Compared to the automotive industry that use film capacitors, the proposed OBC has the advantage of smaller size.

The proposed topology is shown in Figure 3-1. The topology consists of two stages: the totem-pole PFC stage and the dc-dc buck converter stage. The two-stage structure is chosen to avoid the buck PFC, as explained in Chapter 2. Switches  $S_1$ ,  $S_2$ ,  $S_5$ , and  $S_6$  are GaN E-HEMTs with  $25\text{ m}\Omega$   $R_{ds(on)}$ . Switches  $S_3$  and  $S_4$  are power MOSFETs with  $17\text{ m}\Omega$   $R_{ds(on)}$ . GaN-based totem-pole PFC is chosen due to its better PF performance as well as high efficiency property that has been discussed in Chapter 2. GaN-based totem-pole PFC has not been used in non-isolated OBCs yet when this thesis is written. Therefore, a non-isolated dc-dc converter combined with GaN-based totem-pole PFC has gained considerable interest in this thesis.

The totem-pole PFC operates in CCM with a 100 kHz switching frequency in the proposed topology because GaN-based totem-pole PFC has been proven with high efficiency even in hard switching mode. Therefore, hard switching is a better option to reduce complexity and peak current values compared to soft switching. For the non-isolated

dc-dc converter, the synchronous buck converter is used. The switch  $S_6$  is GaN E-HEMT, replaces the low-side diode that is used in the conventional buck converter. Utilizing GaN E-HEMT's lower drain-source resistance  $R_{ds(on)}$  can help to reduce conduction loss significantly to optimize conversion efficiency as discussed in section 2.7. Since the buck converter should always be connected to cancel out the voltage ripples at the battery side, the dc-link voltage level should always be higher than the output (battery) voltage. The battery pack voltage ranges typically from 250 V to 450 V. The selection of the dc-link voltage level will be discussed in the following sections. The proposed topology uses the least number of components, smaller passive components, and a more straightforward control strategy compared to other non-isolated OBCs. Besides, the efficiency is better since there is no half bridge structure which increases the conduction losses in the circuit. The comparison between the proposed OBC and the other two non-isolated OBCs is shown in Table 3-1.



**Figure 3-1: The proposed GaN-based Non-isolated OBC**



**Table 3-1: Comparison between the proposed OBC and other non-isolated OBCs**

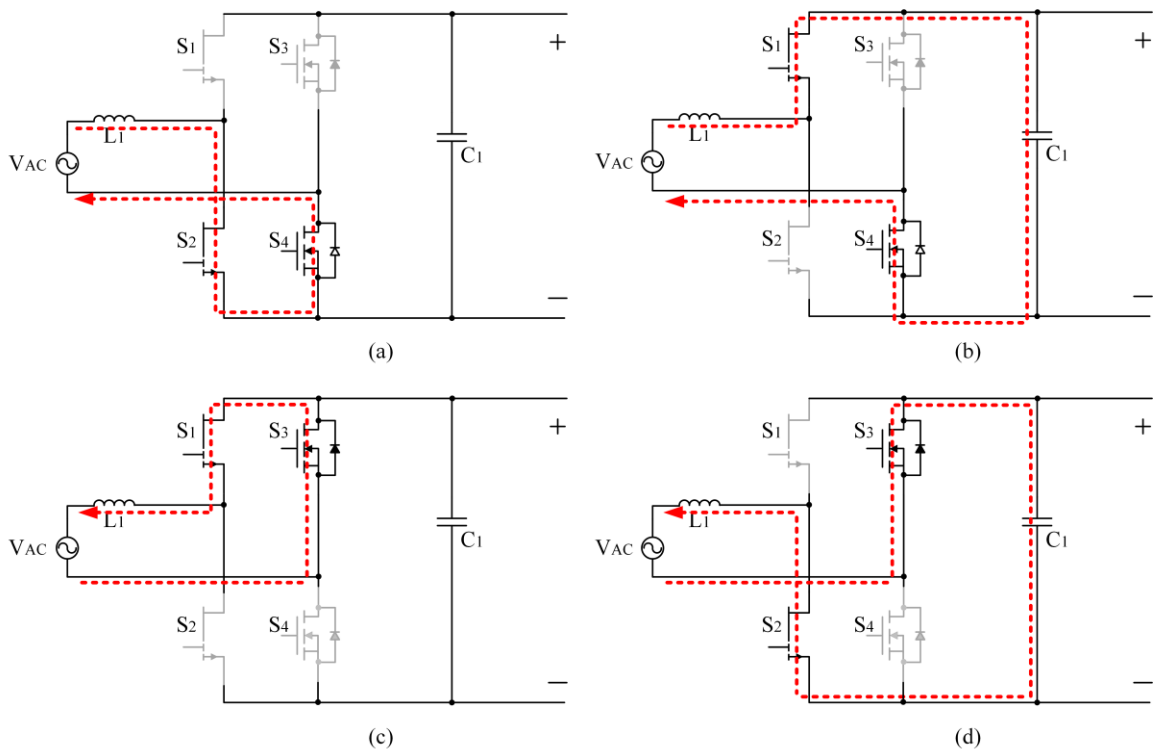
	Proposed OBC	OBC [38]	OBC [41]
No. of Switches	6	2	5
No. of Diodes	0	6	5
No. of Inductors	2	2	3
Inductor Size	L <sub>1</sub> : 500 $\mu$ H L <sub>2</sub> : 340 $\mu$ H	L <sub>1</sub> : 3mH L <sub>2</sub> : 2.52mH	L <sub>1</sub> /L <sub>2</sub> /L <sub>3</sub> : 4mH
No. of Capacitors	2	2	3
Capacitor Size	C <sub>1</sub> : 480 $\mu$ F C <sub>2</sub> : 2 $\mu$ F	C <sub>1</sub> : 8 $\mu$ F C <sub>2</sub> : 950 $\mu$ F	C <sub>1</sub> : 4400 $\mu$ F C <sub>2</sub> : 20 $\mu$ F C <sub>3</sub> : 2200 $\mu$ F
Control Method	CCM	ACMC+IVFF	N.A
Galvanic Isolation	No	No	No
Power level	3.3kW	1kW	1kW

## 3.2 Proposed Control Method

### 3.2.1 First Stage – GaN-based Totem-Pole PFC

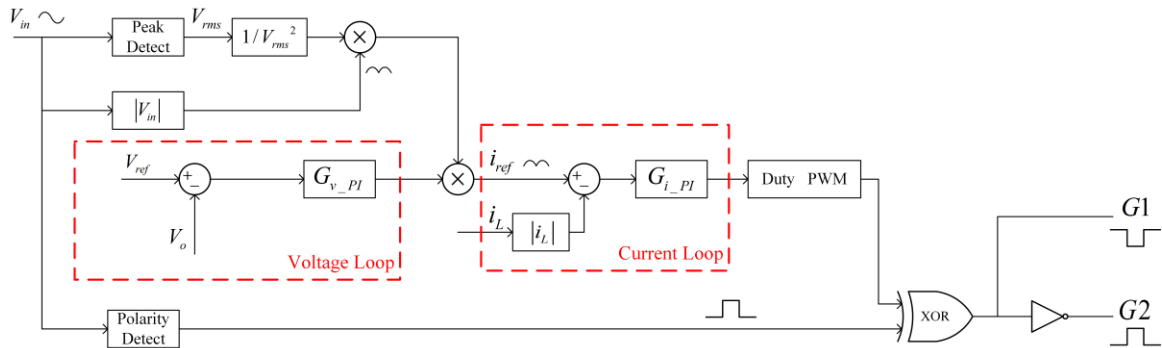
The working principle of the proposed topology can be explained stage by stage. The first stage is the totem-pole PFC converter, as shown in Figure 3-2. During the positive half cycle as indicated in Figure 3-2 (a) and (b),  $S_2$  is the active switch,  $S_1$  is driven with a complementary PWM signal.  $S_4$  is turned on,  $S_3$  is always inactive. They work as a pair of boost converters as switch  $S_2$  increases the boost inductor's current first, then the current flows to the output meanwhile releasing energy. During the negative half-cycle as indicated

in Figure 3-2 (c) and (d), the operation is similar, except the role of top and bottom switches are swapped. Now,  $S_1$  becomes the active switch,  $S_2$  is free-wheeling.  $S_3$  is turned on,  $S_4$  is always inactive.



**Figure 3-2: GaN-based totem-pole PFC working principle**

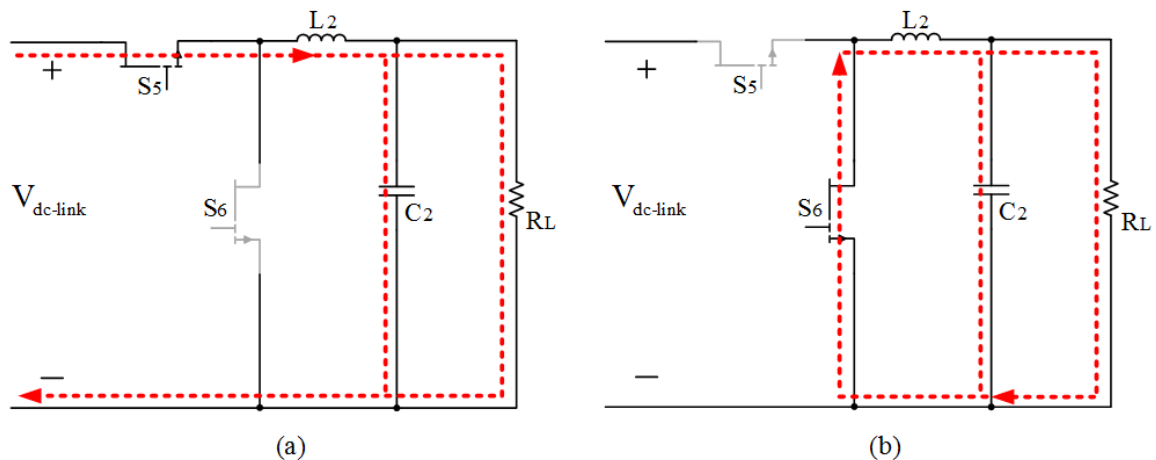
The PFC control loop includes the outer voltage loop and the inner current loop. The outer voltage loop controls the output voltage equal to the reference voltage. The inner current loop controls inductor current, which makes the current sinusoidal and maintains the same phase as the input voltage. The control algorithm is shown in Figure 3-3.



**Figure 3-3: Totem-pole PFC control strategy**

### 3.2.2 Second Stage – GaN-based Synchronous Buck Converter

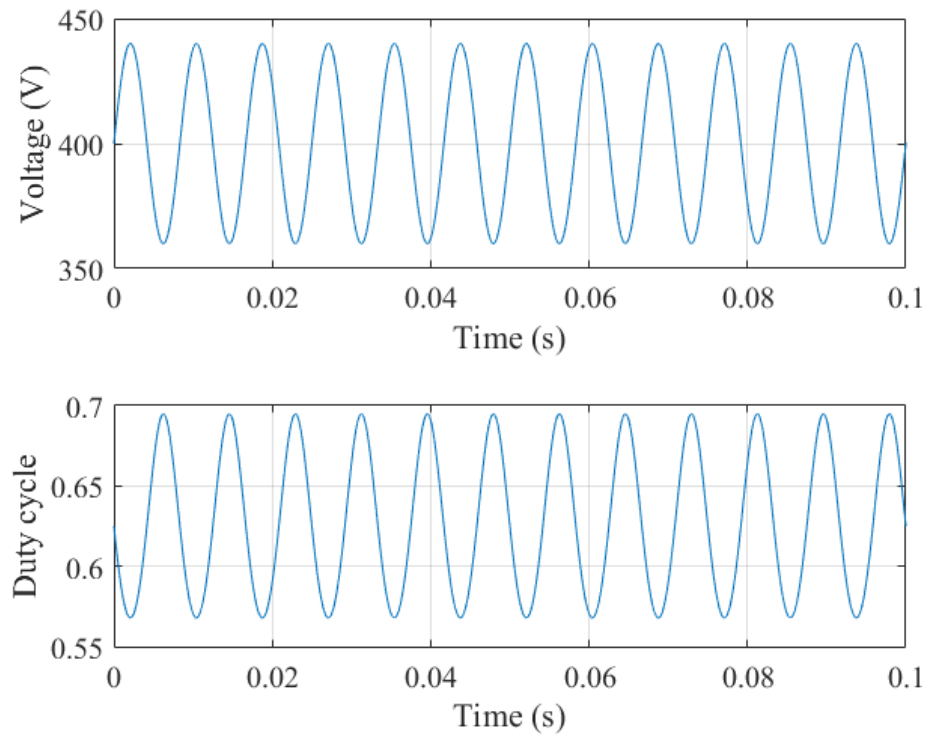
The second stage is the synchronous buck dc-dc converter, as shown in Figure 3-4. When  $S_5$  is turned on and  $S_6$  is turned off, the current is supplied to the load through  $S_5$ . During this time, the current flows through the inductor  $L_2$  increases, charging the LC filter. When  $S_5$  is turned off and  $S_6$  is turned on, the current is supplied to the load through  $S_6$ . During this time, the current through the inductor  $L_2$  decreases, discharging the LC filter.



**Figure 3-4: GaN-based synchronous buck converter in: (a) charging stage; (b) discharging stage**

### 3.2.3 Proposed Active Filtering Technique

The other function of the buck converter in the proposed topology is to cancel the output voltage ripples. Different from conventional OBCs, the ‘dc-link’ voltage (the input to the buck converter) in the proposed topology is not a pure dc value, as shown in Figure 3-5 (top). The “dc-link” voltage mentioned in the following sections refers to the average value. For example, the dc-link voltage in Figure 3-5 is 400 V. This dc-link voltage is at the double-line frequency and is relatedly slow, which allows a complementary duty cycle to be calculated, as shown in Figure 3-5 (bottom).

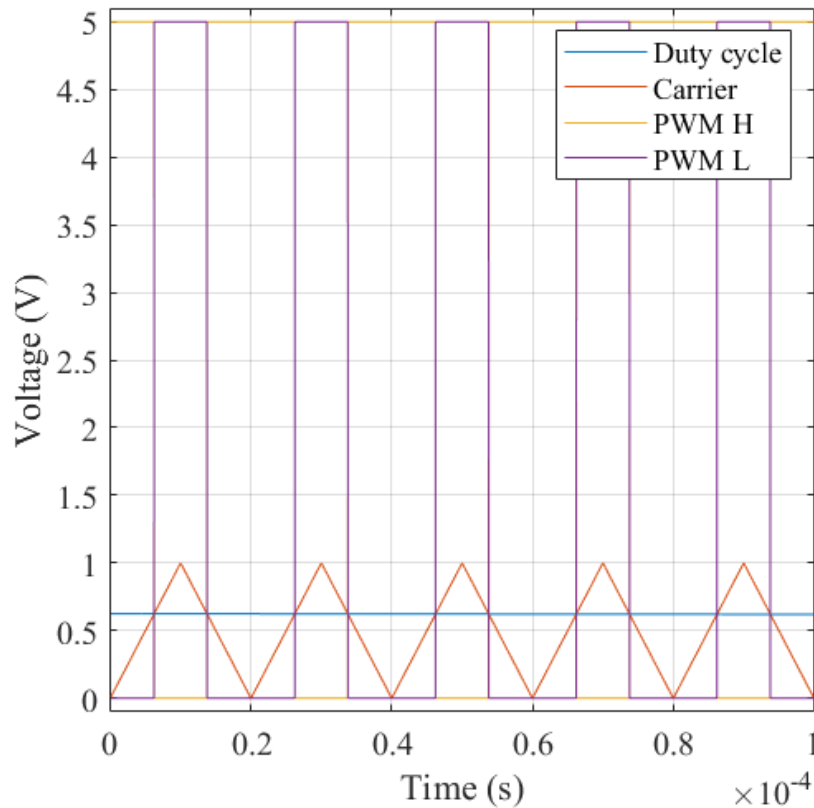


**Figure 3-5: Active filtering using a complementary duty cycle**

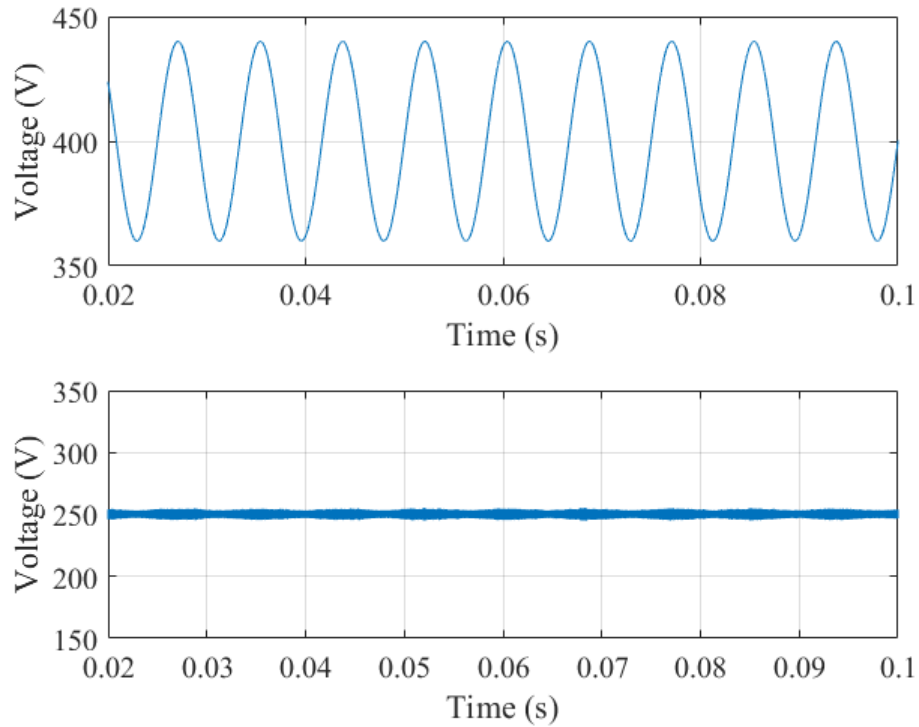
The duty cycle can be expressed as a function of input and output voltages as shown in (3 - 1) where  $V_{HS}$  is the voltage drop across the high side switch when it is conducting

and  $V_{LS}$  is the voltage drop across the low side switch when it is conducting [58]. The values of  $V_{HS}$  and  $V_{LS}$  are small which can be neglected in the equation.  $V_{out}$  is set to be equal to the output voltage,  $V_{in}$  is the dc-link voltage. The duty cycle is then compared to the high-frequency carrier to generate the PWM to turn on/off the top and bottom switch synchronously as shown in Figure 3-6. The ripple-free output voltage is shown in the bottom figure of Figure 3-7 with the corresponding dc-link voltage shown on the top.

$$D = \frac{V_{out} + V_{LS}}{V_{in} - V_{HS} + V_{LS}} \approx \frac{V_{out}}{V_{in}} \quad (3 - 1)$$



**Figure 3-6: PWM generation for synchronous buck converter**



**Figure 3-7: Voltage waveforms of dc-link voltage (top); output voltage (bottom)**

This approach acts as active filtering without adding any further components. The downside of allowing an ac component across the dc-link is increasing the rated voltage of dc-link film capacitors. The later analysis shows there will still be an overall net reduction in size when film capacitors are used.

# Chapter **4**

## Design and Simulation

#### 4.1 Design of Proposed Converter

The proposed OBC is designed for both level 1 and level 2 charging systems. The charger has a wide output voltage range. The detailed specifications are listed in Table 4-1. The designed input inductor current ripple percentage is 15%. There is no strict rule for this percentage. Normally, the full load current ripple is around 20-40% of the average input current in CCM PFC [66]. A lowered number would allow an even better THD%. The output voltage ripple percentage is normally around 5%. A lowered value of percentage would have positive impact on battery life.

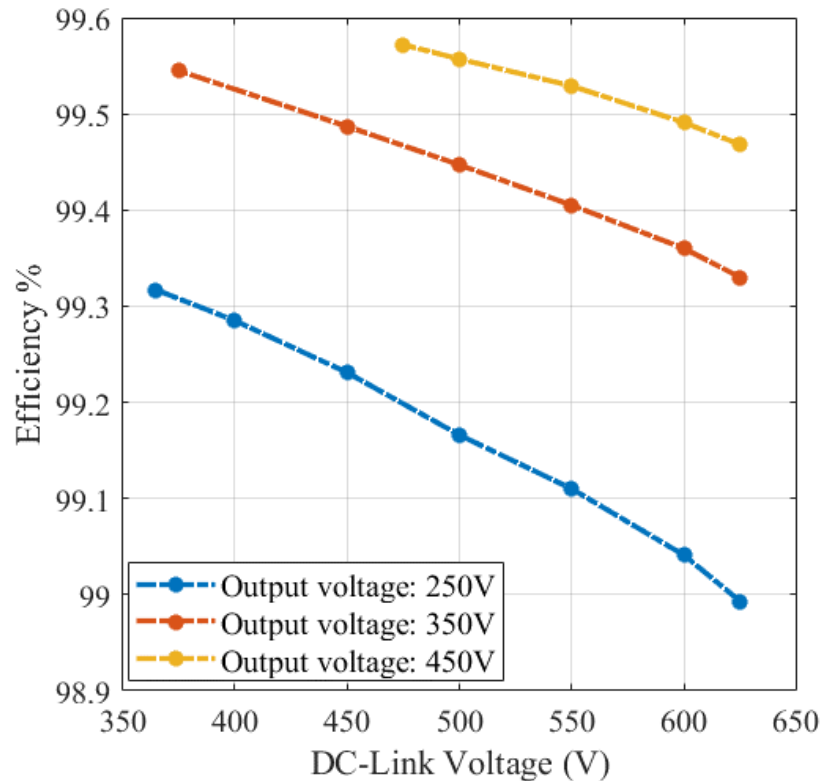
**Table 4-1: Specifications of the power stage**

Input voltage	120 to 240 Vac, at 60 Hz
Output voltage	250 V to 450 V
Maximum power	1.92 kW at 120 Vac, 3.3 kW at 240 Vac
Switching frequency	100 kHz
Input inductor current ripple (full load)	< 15%
Output voltage ripple	< 2%

The selection of dc-link voltage is crucial in the proposed topology and will be clarified step by step in the following sections. First, a separate GaN-based synchronous buck converter operating at 100 kHz has been modeled in PLECS. The simulation uses GS66516T with the thermal model provided by GaN Systems, ideal output capacitor in series with 1.9 m $\Omega$  ESR (Equivalent Series Resistance), and ideal output inductor model in series with 14 m $\Omega$  DCR (Direct Current Resistance). PLECS build-in periodic average block is used to calculate the average conduction loss. PLECS build-in periodic impulse



average block is used to calculate the average switching loss. The efficiency curves are generated with varying input voltages, as shown in Figure 4-1.

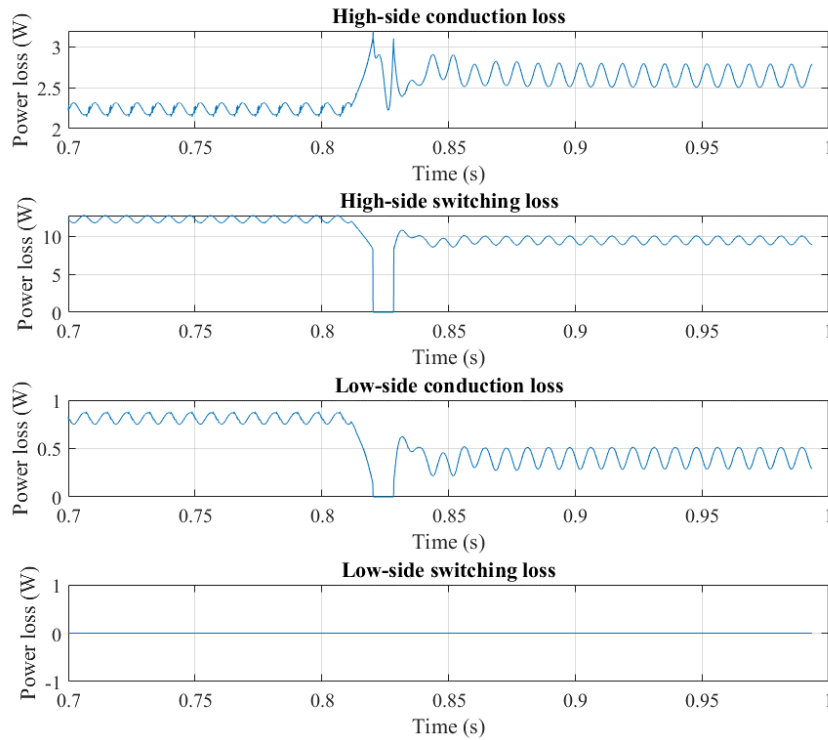


**Figure 4-1: DC-link voltage vs. efficiency for synchronous buck converter**

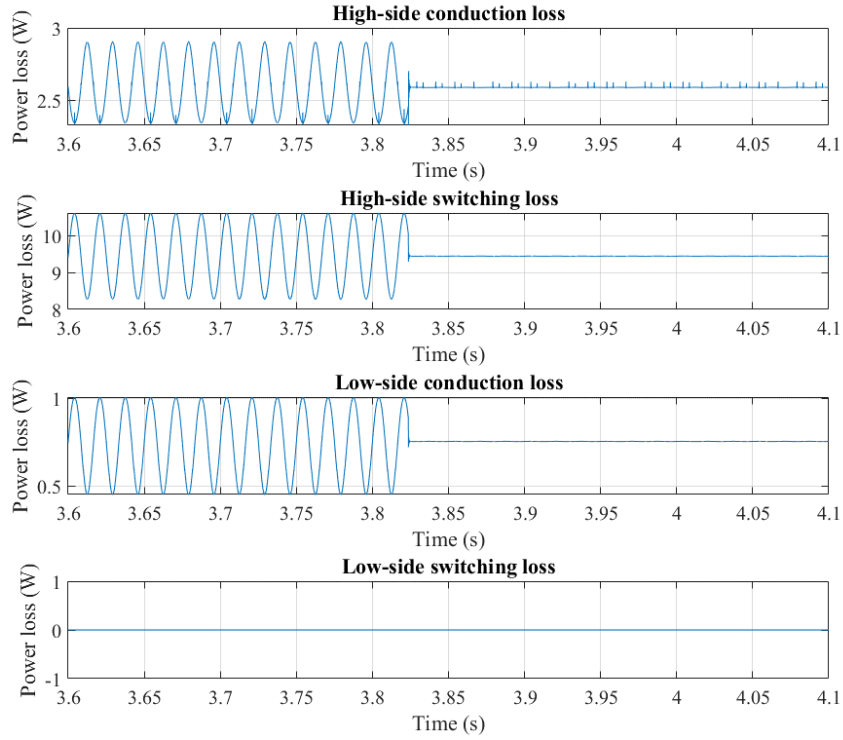
All of the data points are simulated at a full load of 3.3 kW since this is expected to be a common charging load. The results show that the higher the duty cycle or the lower the dc-link voltage, the higher the efficiency will be when output voltage (battery) and power are held constant. At the higher duty cycle, the conduction loss of the high-side switch is increased, while at the meantime, the conduction loss of the low-side switch is reduced. The switching loss of the low-side switch is very small which is negligible. The switching loss of the high-side switch is decreased. As a result, the total loss is reduced at

lower dc-link voltage, as shown in Figure 4-2 (a), where the duty cycle is increased after 0.81 seconds.

The ac components on top of the dc-link voltages increase the instantaneous power loss but not the average power loss, as shown in Figure 4-2 (b), where ac components are removed after 3.82 seconds. Therefore, the efficiency curve can be plotted without adding the ac source in simulation.



(a)



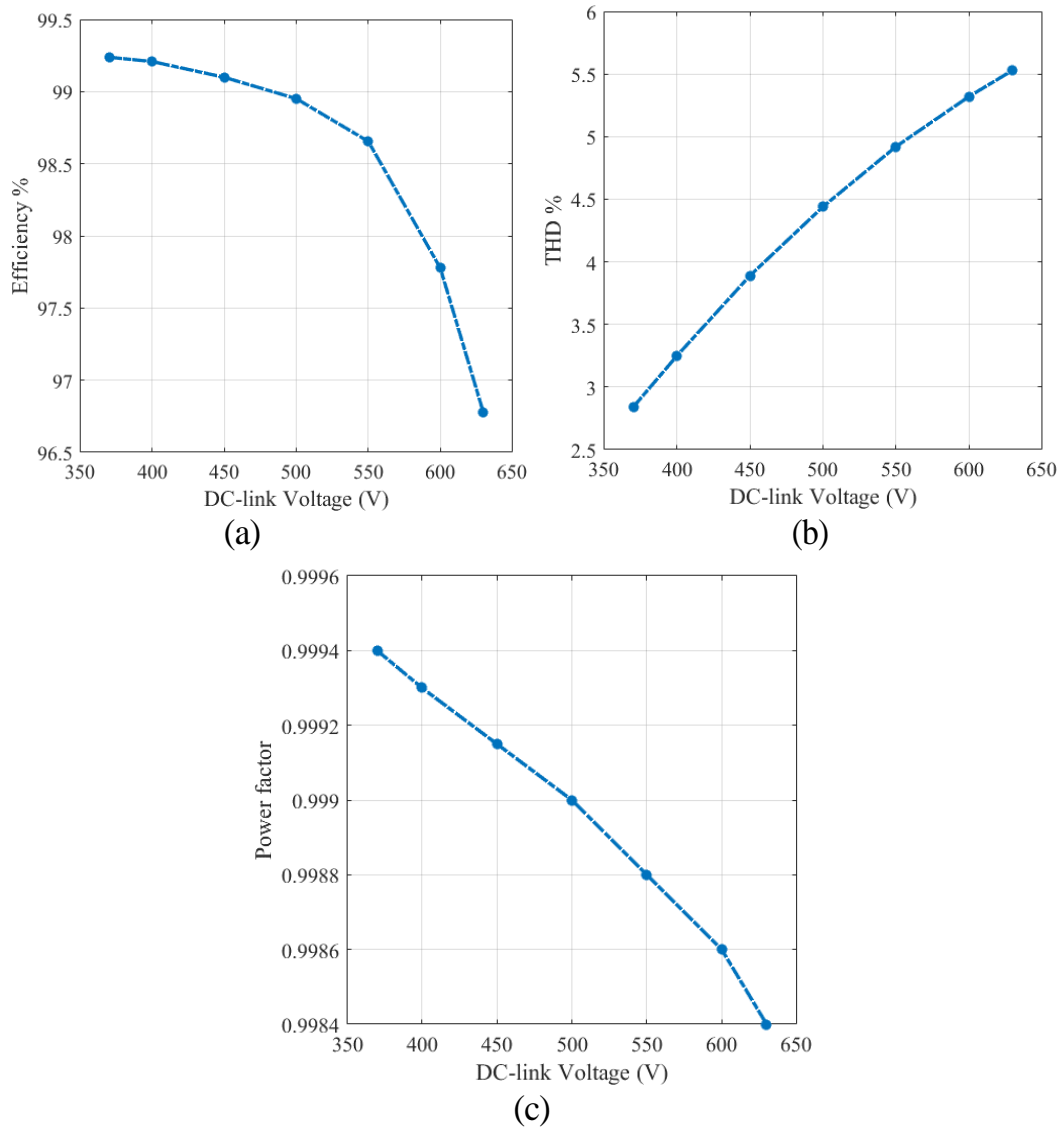
(b)

**Figure 4-2: Power loss of GaN-based synchronous buck converter when: (a) increasing duty cycle; (b) removing ac components**

Since the totem-pole is a boost-type PFC converter, the dc-link voltage has to be greater than the peak value of the AC input voltage. And the dc-link voltage cannot exceed the voltage rating of the switch. The GaN E-HEMT used in this design is rated at 650 V. The ranges of dc-link voltage at different output voltage levels are shown in (4 - 1), where 25 V ripple margins are added.

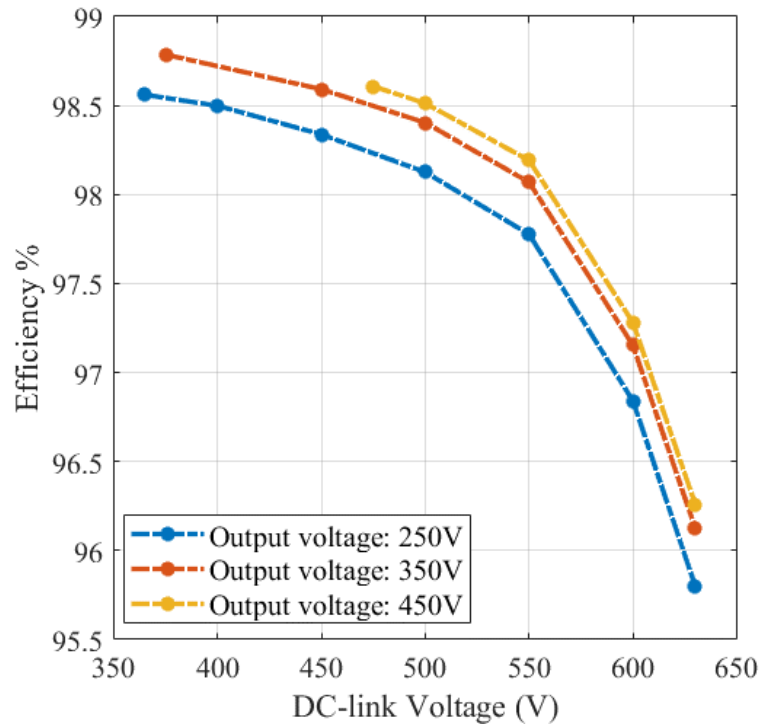
$$\begin{aligned}
 340V < V_{dc,250V,pk-pk} < 650V & \quad 365V < V_{dc,250V,avg} < 625V \\
 350V < V_{dc,350V,pk-pk} < 650V & \quad 375V < V_{dc,350V,avg} < 625V \\
 450V < V_{dc,450V,pk-pk} < 650V & \quad 475V < V_{dc,450V,avg} < 625V
 \end{aligned}
 \tag{4 - 1}$$

A separate totem-pole PFC has been simulated in PLECS as well to demonstrate the relationship between dc-link voltage and efficiency, THD%, and PF. The simulation results are shown in Figure 4-3. The performance is better at lower dc-link voltage level with higher efficiency, low THD%, and good PF. Therefore, the dc-link voltage should be set as closed to the lower boundary as possible.



**Figure 4-3: Totem-pole PFC dc-link voltage vs.: (a) efficiency; (b) THD%; (c) PF**

Now combining the results from synchronous buck dc-dc converter with totem-pole PFC. The overall efficiency curve is shown in Figure 4-4. The rule of thumb for selecting dc-link voltage is to follow the lower boundary in (4-1). However, modification is made in 4.1.1 when considering the dc-link capacitor size.



**Figure 4-4: DC-link voltage vs. efficiency for the proposed OBC**

#### 4.1.1 Calculation of $C_1$

The calculation of the dc-link capacitor depends on both the voltage level as well as the voltage ripples. The equations (4 - 2) and (4 - 3) are used to calculate the capacitance.

$$\Delta V_{dc} = V_{dc,avg} - V_{in,pk} \quad (4 - 2)$$

$$C_1 = \frac{P_o}{2 \cdot \pi \cdot f_{line} \cdot \Delta V_{dc} \cdot V_{dc}} \quad (4 - 3)$$

Separate calculations are given for better comparison between the cases with/without active filtering. The dc-link capacitor allowing 5% peak-to-peak voltage ripples without active filtering is calculated in equation (4 - 4). The dc-link capacitor with active filtering is calculated in equation (4 - 5). At the same average dc-link voltage level, the one with active filtering has much smaller capacitance. If we want to further reduce the capacitance in (4 - 5), we should notice that there is a tradeoff between efficiency and capacitor size. 1. By relaxing the voltage ripples, the capacitor size can be reduced. 2. By relaxing the voltage ripples, the average dc-link voltage must be shifted up. 3. The average dc-link voltage goes up, the efficiency drops, as shown in Figure 4-4.

$$C_{1,240Vac} \geq \frac{P_o}{2 \cdot \pi \cdot f_{line} \cdot \Delta V_{dc} \cdot V_{dc}} = \frac{3300W}{2 \cdot \pi \cdot 60Hz \cdot 9.125V \cdot 365V} = 2628\mu F \quad (4 - 4)$$

$$C_{1,120Vac} \geq \frac{P_o}{2 \cdot \pi \cdot f_{line} \cdot \Delta V_{dc} \cdot V_{dc}} = \frac{1920W}{2 \cdot \pi \cdot 60Hz \cdot 4.875V \cdot 195V} = 5358\mu F$$

$$C_{1,240Vac} \geq \frac{P_o}{2 \cdot \pi \cdot f_{line} \cdot \Delta V_{dc} \cdot V_{dc}} = \frac{3300W}{2 \cdot \pi \cdot 60Hz \cdot 25V \cdot 365V} = 960\mu F \quad (4 - 5)$$

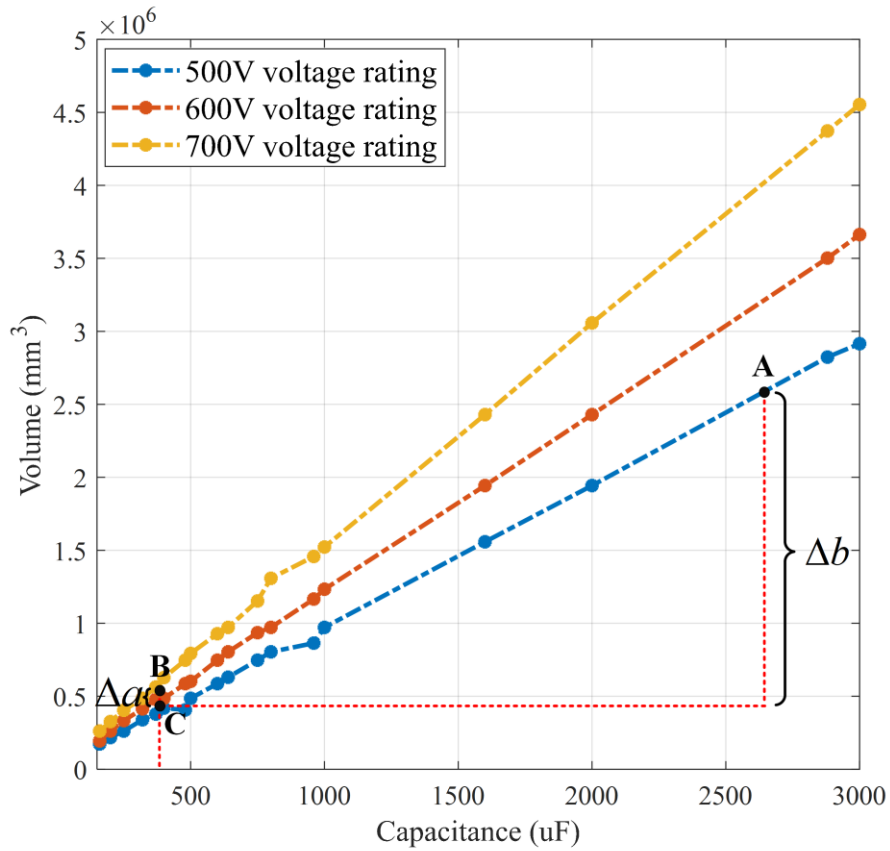
$$C_{1,120Vac} \geq \frac{P_o}{2 \cdot \pi \cdot f_{line} \cdot \Delta V_{dc} \cdot V_{dc}} = \frac{1920W}{2 \cdot \pi \cdot 60Hz \cdot 25V \cdot 195V} = 1045\mu F$$

The final decision is made by relaxing the voltage ripples but not sacrificing the efficiency too much. With an extra 35 V ripple relaxation, the updated dc-link capacitance is calculated in (4 - 6). At level 2 charging mode, the capacitance is reduced by half

compared to the capacitance in (4 - 5) and by one-seventh compared to the capacitance in (4 - 4). The reduction is even more at level 1 charging mode.

$$\begin{aligned}
 C_{1,240Vac} &\geq \frac{P_o}{2 \cdot \pi \cdot f_{line} \cdot \Delta V_{dc} \cdot V_{dc}} = \frac{3300W}{2 \cdot \pi \cdot 60Hz \cdot 60V \cdot 400V} = 365 \mu F \\
 C_{1,120Vac} &\geq \frac{P_o}{2 \cdot \pi \cdot f_{line} \cdot \Delta V_{dc} \cdot V_{dc}} = \frac{1920W}{2 \cdot \pi \cdot 60Hz \cdot 60V \cdot 230V} = 369 \mu F
 \end{aligned}
 \tag{4 - 6}$$

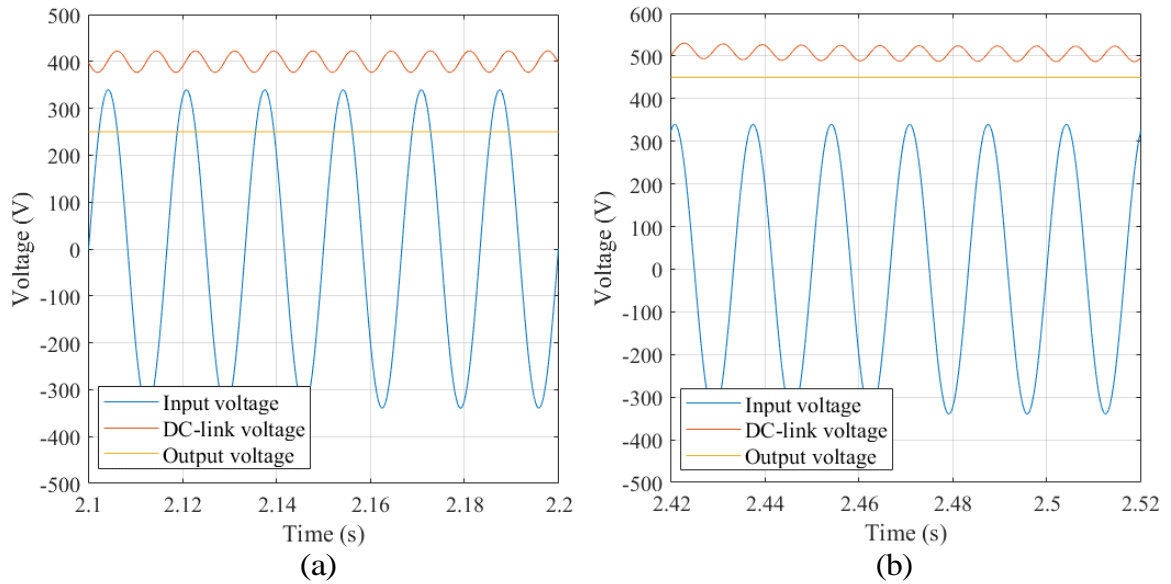
The lower the capacitance, the smaller the physical size will be. But the increased voltage rating will increase the volume at the same time. The capacitance vs. volume curves at different voltage ratings have been generated in Figure 4-5 in order to see whether the capacitance value or the voltage rating has more impact on the capacitor size. The data is from VISHAY “Metallized Polypropylene Film Capacitors Datasheet” [67]. Modifications are made by paralleling film capacitors to increase the capacitance range. The comparison is made between two capacitances: 370  $\mu$ F and 2650  $\mu$ F as calculated in (4 - 4) and (4 - 6) at level 2 charging mode. The impact of reduced capacitance on film capacitor size is represented by  $\Delta b$ , from point A to point C. The impact of increased voltage rating on film capacitor size is represented by  $\Delta a$ , from point C to point B. The conclusion is that the reduced capacitance has much more impact than that from the increased voltage rating.



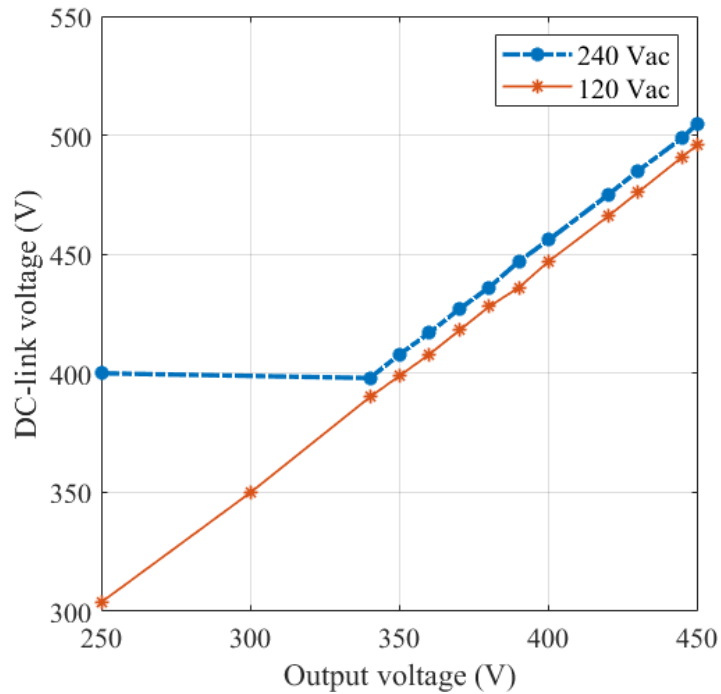
**Figure 4-5: Capacitance vs. volume at different voltage ratings**

In this design, a final 480  $\mu\text{F}$  film capacitor is used for  $C_1$  when considering the derating of the capacitor and safety margins. The dc-link voltage waveforms are shown in Figure 4-6. The dc-link voltages are selected based on a look-up table in Figure 4-7 to maintain a 35 V safety margin at each voltage level. For example, the gap between the peak input voltage and the bottom peak of dc-link voltage is 35 V in Figure 4-6 (a), the gap between the bottom peak of the dc-link voltage and output voltage is 35 V in Figure 4-6 (b). The same rule is applied to the level 1 charging mode with the dc-link voltage look-up table shown in Figure 4-7.





**Figure 4-6: DC-link voltage at: (a) 250 V output; (b) 450 V output**



**Figure 4-7: DC-link voltage selection look-up table**

#### 4.1.2 Calculation of $L_1$

The minimum input inductance at full load with a 15% current ripple is calculated from (4 - 7) to (4 - 11) [68]. The minimum input inductance is calculated at the maximum dc-link voltage. In this design, a 500  $\mu\text{H}$  inductor is selected when considering 24% inductor de-rating. The rated peak current is 50 A.

For level 2 charging mode:

$$L_{1,\min} \geq \frac{1}{\%Ripple} \cdot \frac{V_{ac}^2}{P_o} \left(1 - \frac{\sqrt{2} \cdot V_{ac}}{V_{dc}}\right) \cdot \frac{1}{f_{sw}} \quad (4 - 7)$$

$$L_{1,\min} \geq \frac{1}{0.15} \cdot \frac{(240V)^2}{3300W} \left(1 - \frac{\sqrt{2} \cdot 240V}{505V}\right) \cdot \frac{1}{100kHz} = 382\mu H \quad (4 - 8)$$

$$I_{L1} \geq \frac{\sqrt{2} \cdot P_o}{V_{ac}} \cdot \left(1 + \frac{\%Ripple}{2}\right) = \frac{\sqrt{2} \cdot 3300W}{240V} \cdot \left(1 + \frac{0.15}{2}\right) = 20.9A \quad (4 - 9)$$

For level 1 charging mode:

$$L_{1,\min} \geq \frac{1}{0.15} \cdot \frac{(120V)^2}{1920W} \left(1 - \frac{\sqrt{2} \cdot 120V}{496V}\right) \cdot \frac{1}{100kHz} = 329\mu H \quad (4 - 10)$$

$$I_{L1} \geq \frac{\sqrt{2} \cdot P_o}{V_{ac}} \cdot \left(1 + \frac{\%Ripple}{2}\right) = \frac{\sqrt{2} \cdot 1920W}{120V} \cdot \left(1 + \frac{0.15}{2}\right) = 24.3A \quad (4 - 11)$$

### 4.1.3 Calculation of L<sub>2</sub> and C<sub>2</sub>

The values of the output inductor and output capacitor depend on several factors, including the duty cycle, the power level, input/output voltage, the switching frequency, allowable inductor current ripple ratio (LIR), and capacitor voltage ratio (CVR). Due to the variable dc-link voltage and wide output voltage, the calculation of LC is considered at two boundary conditions: 250 V output voltage and 450 V output voltage. The detailed calculation is shown from (4 - 12) to (4 - 27). The largest inductance is required at level 1 charging and 450 V output voltage. The largest capacitance is required at level 2 charging and 250 V output voltage. In this design, the final selections of LC values are 340 μH and 2 μF while consider the inductor and capacitor de-rating.

Level 1 charging, 250 V output voltage:

$$D = \frac{250V}{304V} = 0.8224 \quad (4 - 12)$$

$$I_{out,max} = \frac{P_o}{V_{o,min}} = \frac{1920W}{250V} = 7.68A \quad (4 - 13)$$

$$L_{2,min} \geq \frac{(V_{dc} - V_o) \cdot D}{LIR \cdot I_{out,max} \cdot f_{sw}} = \frac{(304V - 250V) \cdot 0.8224}{0.4 \cdot 7.68A \cdot 100kHz} = 145\mu H \quad (4 - 14)$$

$$C_{2,min} \geq \frac{LIR \cdot I_{out,max}}{8 \cdot f_{sw} \cdot CVR \cdot V_o} = \frac{0.4 \cdot 7.68A}{8 \cdot 100kHz \cdot 0.02 \cdot 250V} = 0.77\mu F \quad (4 - 15)$$

Level 1 charging, 450 V output voltage:

$$D = \frac{450V}{496V} = 0.9073 \quad (4 - 16)$$

$$I_{out,max} = \frac{P_o}{V_{o,min}} = \frac{1920W}{450V} = 4.27A \quad (4 - 17)$$

$$L_{2,min} \geq \frac{(V_{dc} - V_o) \cdot D}{LIR \cdot I_{out,max} \cdot f_{sw}} = \frac{(496V - 450V) \cdot 0.9073}{0.4 \cdot 4.27A \cdot 100kHz} = 245\mu H \quad (4 - 18)$$

$$C_{2,min} \geq \frac{LIR \cdot I_{out,max}}{8 \cdot f_{sw} \cdot CVR \cdot V_o} = \frac{0.4 \cdot 4.27A}{8 \cdot 100kHz \cdot 0.02 \cdot 450V} = 0.24\mu F \quad (4 - 19)$$

Level 2 charging, 250 V output voltage:

$$D = \frac{250V}{400V} = 0.625 \quad (4 - 20)$$

$$I_{out,max} = \frac{P_o}{V_{o,min}} = \frac{3300W}{250V} = 13.2A \quad (4 - 21)$$

$$L_{2,min} \geq \frac{(V_{dc} - V_o) \cdot D}{LIR \cdot I_{out,max} \cdot f_{sw}} = \frac{(400V - 250V) \cdot 0.625}{0.4 \cdot 13.2A \cdot 100kHz} = 178\mu H \quad (4 - 22)$$

$$C_{2,min} \geq \frac{LIR \cdot I_{out,max}}{8 \cdot f_{sw} \cdot CVR \cdot V_o} = \frac{0.4 \cdot 13.2A}{8 \cdot 100kHz \cdot 0.02 \cdot 250V} = 1.32\mu F \quad (4 - 23)$$

Level 2 charging, 450 V output voltage:

$$D = \frac{450V}{505V} = 0.8911 \quad (4 - 24)$$

$$I_{out,max} = \frac{P_o}{V_{o,min}} = \frac{3300W}{450V} = 7.33A \quad (4 - 25)$$

$$L_{2,min} \geq \frac{(V_{dc} - V_o) \cdot D}{LIR \cdot I_{out,max} \cdot f_{sw}} = \frac{(505V - 450V) \cdot 0.8911}{0.4 \cdot 7.33A \cdot 100kHz} = 167 \mu H \quad (4 - 26)$$

$$C_{2,min} \geq \frac{LIR \cdot I_{out,max}}{8 \cdot f_{sw} \cdot CVR \cdot V_o} = \frac{0.4 \cdot 7.33A}{8 \cdot 100kHz \cdot 0.02 \cdot 450V} = 0.41 \mu F \quad (4 - 27)$$

## 4.2 Simulation

Circuit simulation is done in PLECS, as shown in Figure 4-8. GaN Systems provide the GaN E-HEMT PLECS model. GS66516T with 650 V voltage rating and 60 A current rating is used in this design. The thermal models, including turn-on loss, turn-off loss, and conduction loss, are shown in Figure 4-9.

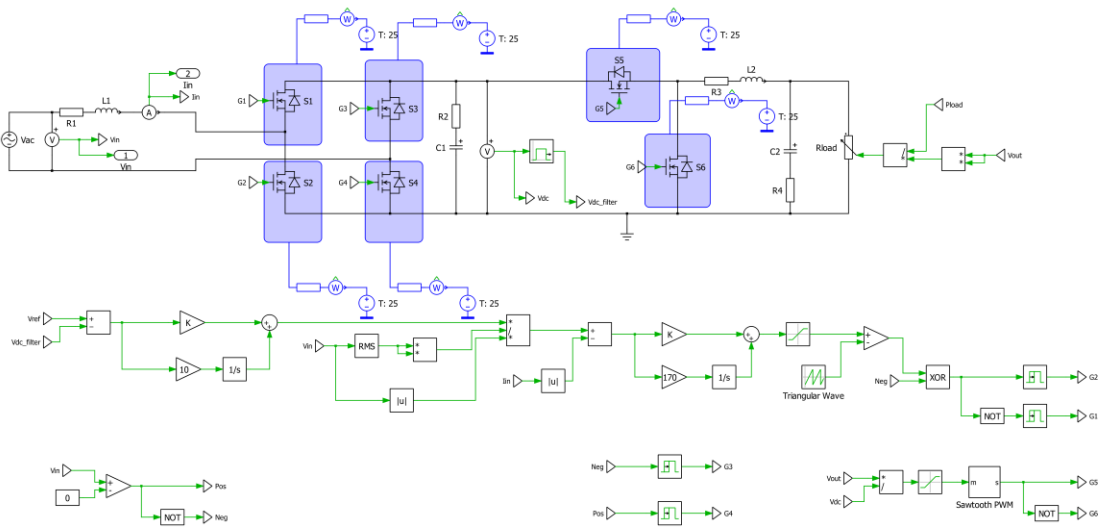
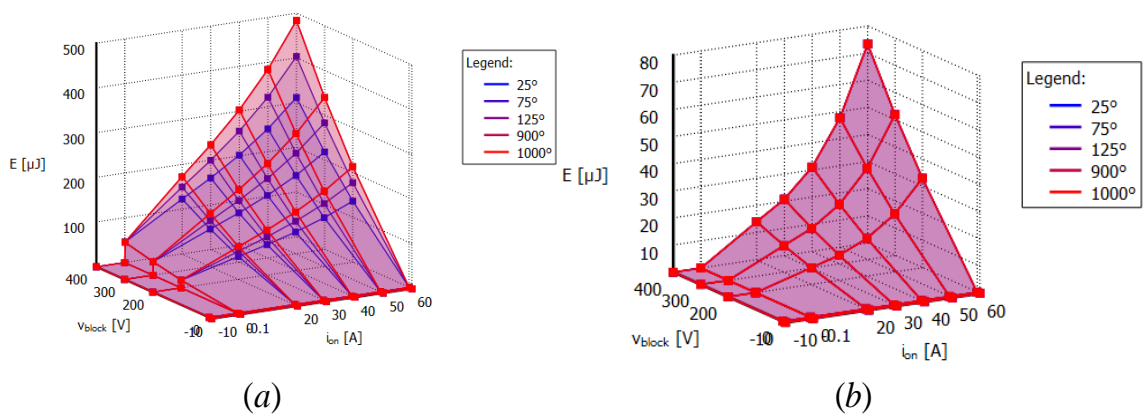
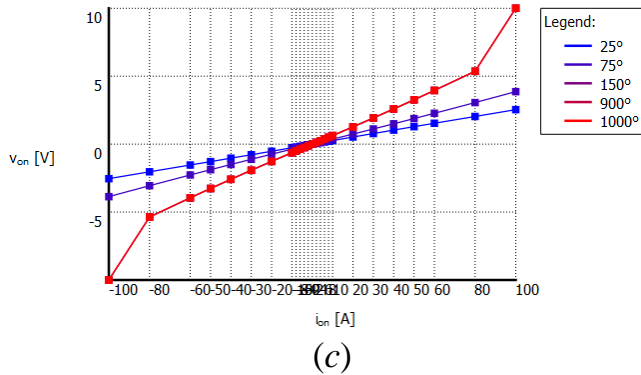


Figure 4-8: Schematic of the proposed topology

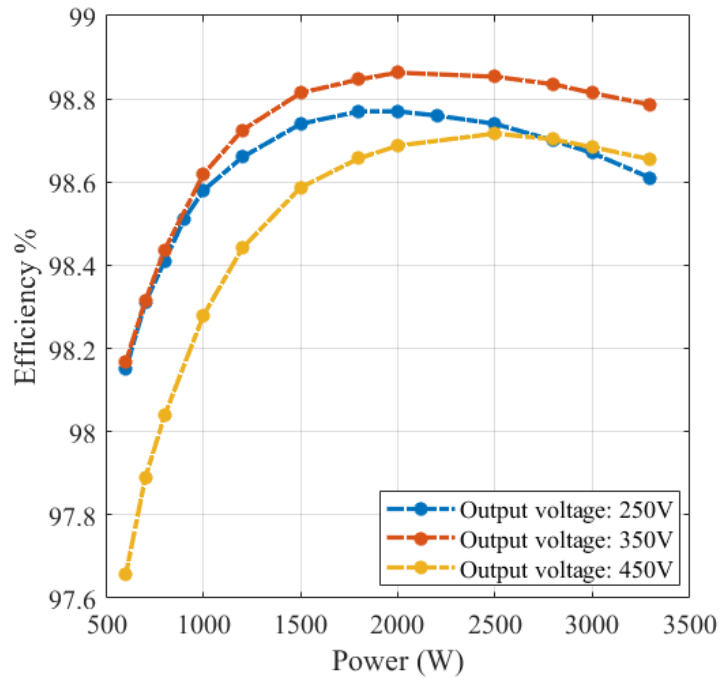




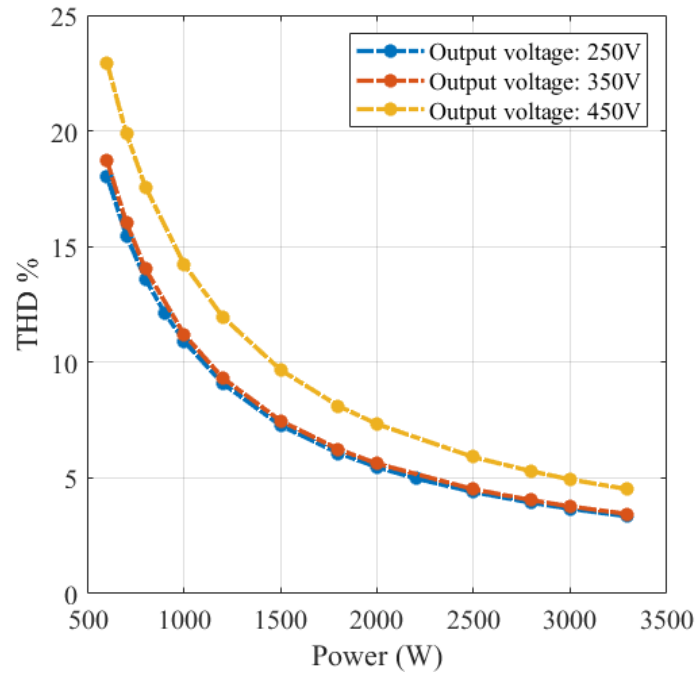
**Figure 4-9: GS66516T thermal model: (a) turn on loss; (b) turn off loss; (c) conduction loss**

### 4.3 Simulation Results

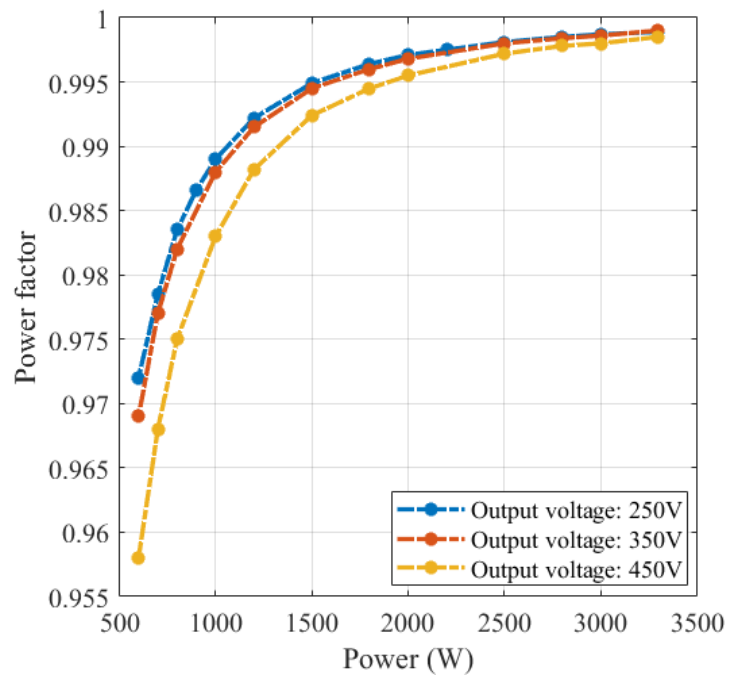
The simulation results of efficiency, THD%, and PF for the proposed level 2 OBC at different loads are shown in Figure 4-10, Figure 4-11 and Figure 4-12, respectively. The results show the overall performance is getting worse at light load. The peak efficiency reaches over 98.8%. And the efficiency at full load is over 98.6%.



**Figure 4-10: Efficiency curve of the proposed level 2 OBC**



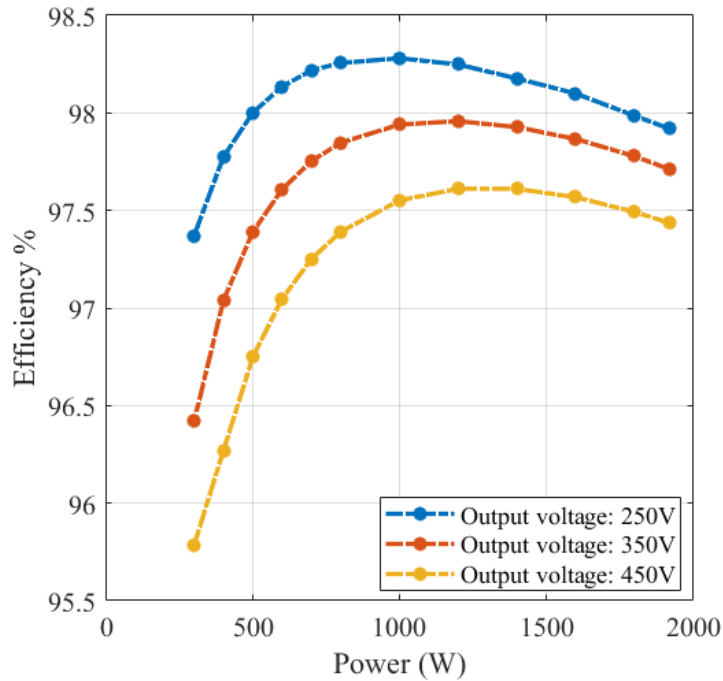
**Figure 4-11: THD% of the proposed level 2 OBC**



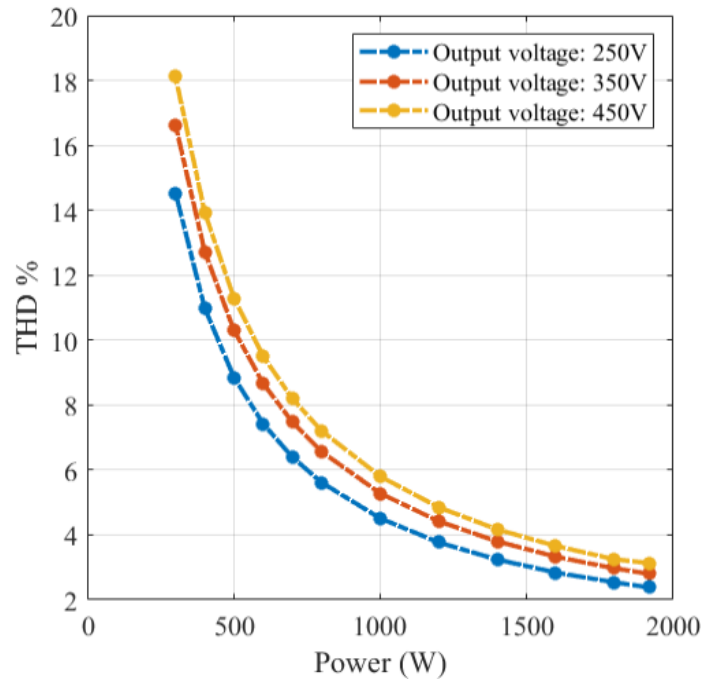
**Figure 4-12: PF of the proposed level 2 OBC**



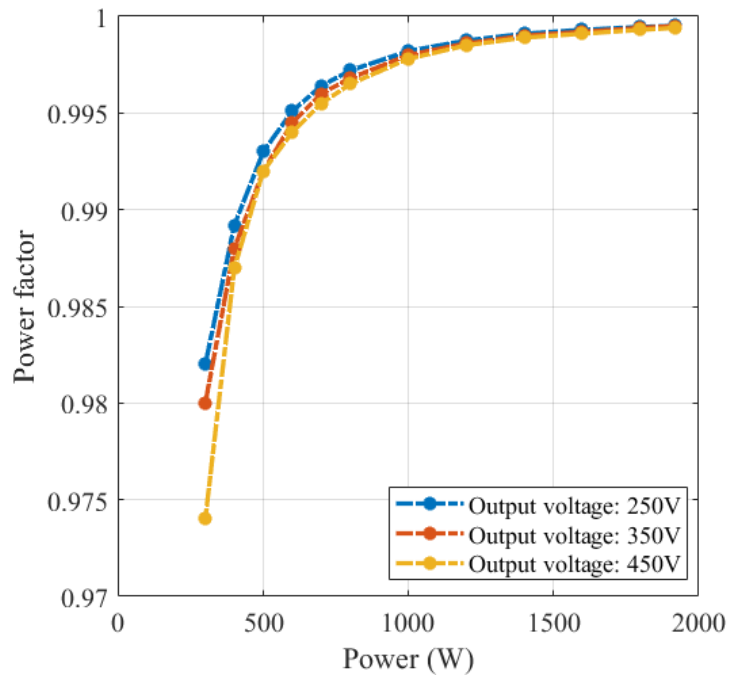
The simulation results of efficiency, THD%, and PF for the proposed level 1 OBC at different loads are shown Figure 4-13, Figure 4-14, and Figure 4-15, respectively. The results show the overall performance is getting worse at light load. The peak efficiency reaches over 98.3%. And the efficiency at full load is over 97.4%.



**Figure 4-13: Efficiency curve of the proposed level 1 OBC**

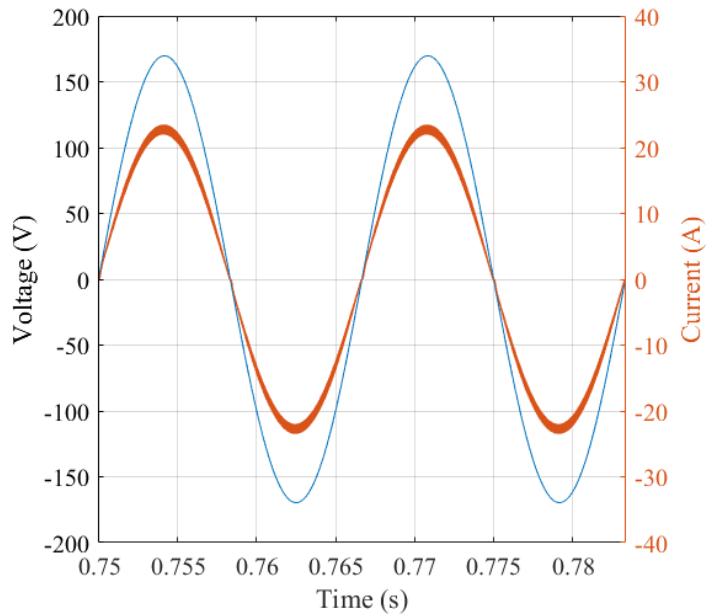


**Figure 4-14: THD% of the proposed level 1 OBC**

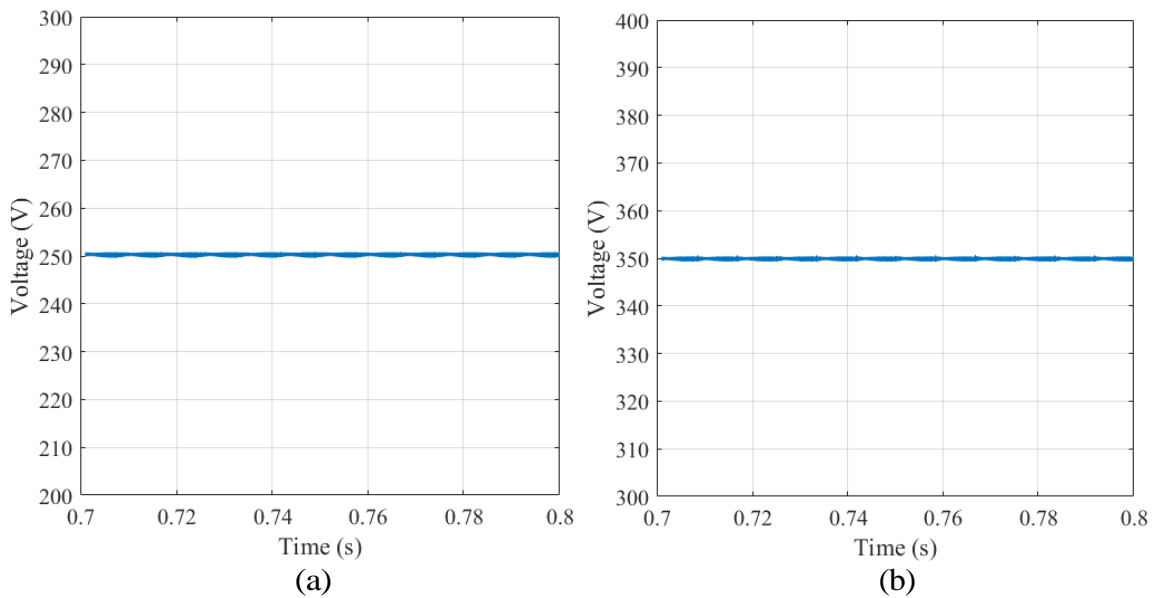


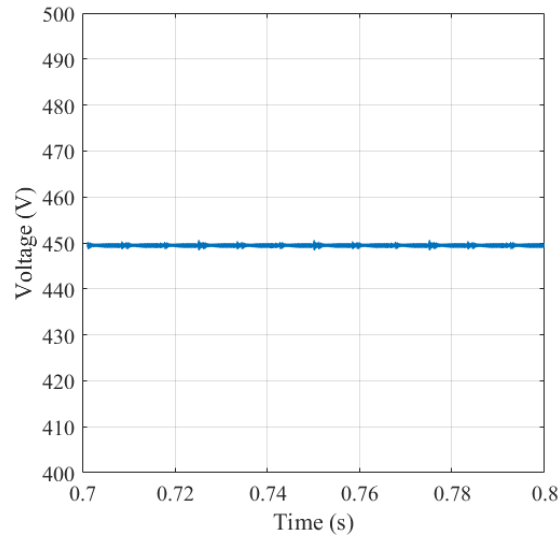
**Figure 4-15: PF of the proposed level 1 OBC**

The input current waveform at full load at level 1 charging mode is shown in Figure 4-16. The output voltage waveforms at 250 V, 350 V, and 450 V are shown in Figure 4-17 (a), (b), and (c), respectively. The simulation results validate the designed requirement for less than 15% input current ripple and less than 2% output voltage ripple.



**Figure 4-16: Level 1 OBC input current waveform at full load**

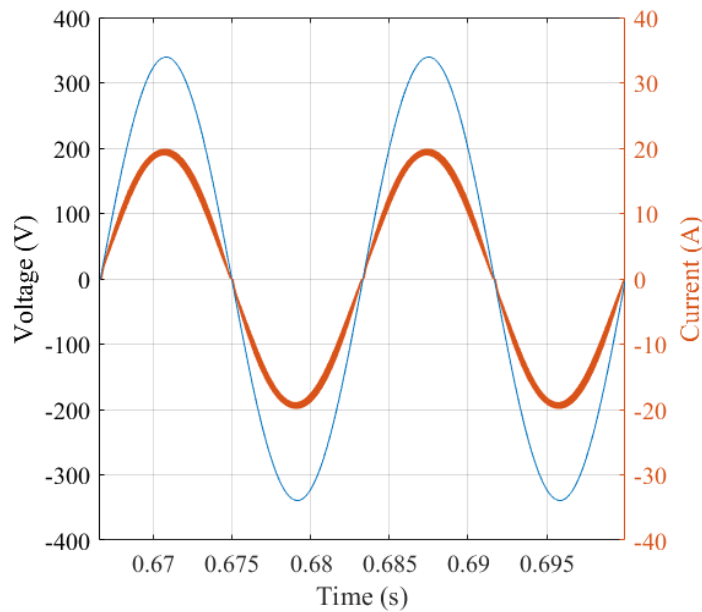




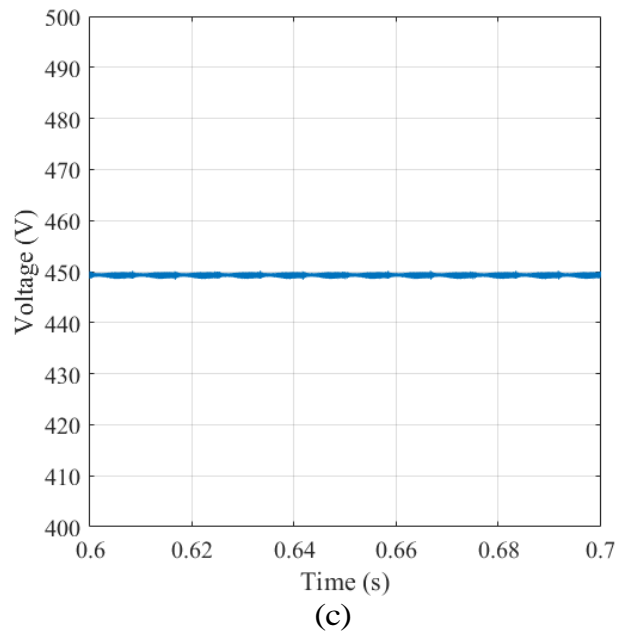
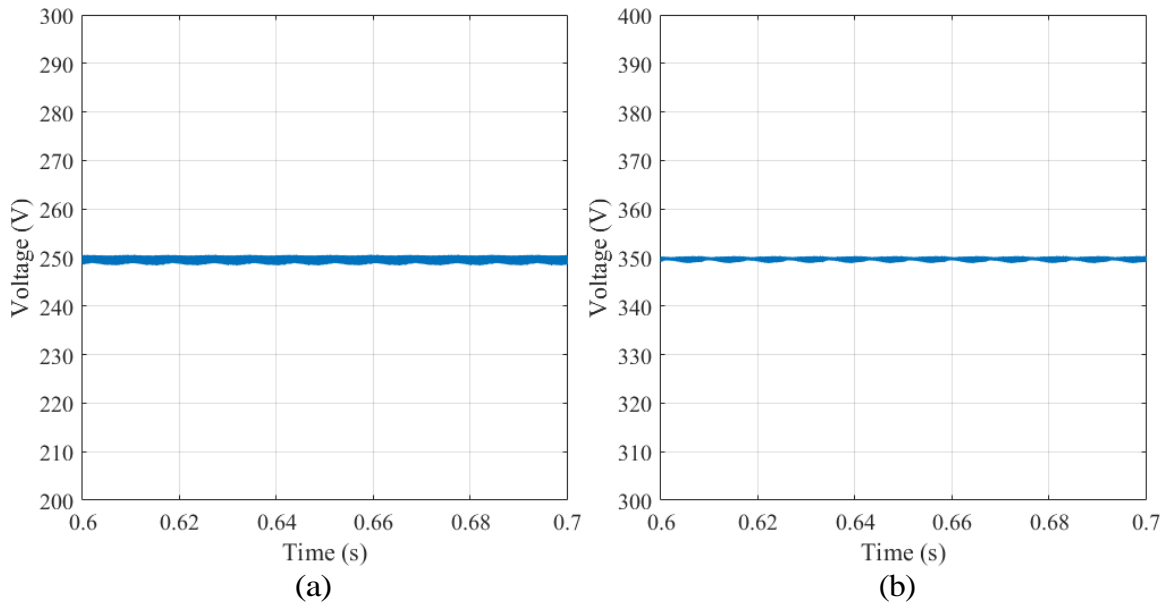
(c)

**Figure 4-17: Level 1 output voltage: (a) 250 V; (b) 350 V; (c) 450 V**

The input current waveform at full load at level 2 charging mode is shown in Figure 4-18. The output voltage waveforms at 250 V, 350 V, and 450 V are shown in Figure 4-19 (a), (b), and (c), respectively. The simulation results validate the designed requirement for less than 15% input current ripple and less than 2% output voltage ripple.



**Figure 4-18: Level 2 OBC input current waveform at full load**



**Figure 4-19: Level 2 OBC output voltage: (a) 250 V; (b) 350 V; (c) 450 V**

# Chapter 5

## Experimental Verification

## 5.1 Dead Time

For hard switching, the dead time  $td_{PWM}$  must be greater than  $t_{delay\_skew} + (td_{(off)} - td_{(on)})$  [69], where  $t_{delay\_skew}$  is gate driver's propagation delay,  $td_{(off)}$  is switch turn-off delay and  $td_{(on)}$  is switch turn-on delay. The gate driver selected for GaN E-HEMT is from Silicon Labs, Si8271GB-IS. The gate driver's maximum propagation delay is 60 ns. Turn-off and turn-on delay time is 14.9 ns and 4.6 ns, respectively, as shown in Figure 5-1. 100 ns dead time is used in the experiment to satisfy the requirement as calculated in (5 - 1) to (5 - 3).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Turn-On Delay	$t_{D(on)}$		4.6		ns	$V_{DD} = 400\text{ V}$ $V_{GS} = 0 - 6\text{ V}$ $I_D = 16\text{ A}$ , $R_{G(ext)} = 5\ \Omega$ $T_J = 25\text{ }^\circ\text{C}$ (note 4)
Rise Time	$t_R$		12.4		ns	
Turn-Off Delay	$t_{D(off)}$		14.9		ns	
Fall Time	$t_F$		22		ns	
Output Capacitance Stored Energy	$E_{OSS}$		17		$\mu\text{J}$	$V_{DS} = 400\text{ V}$ $V_{GS} = 0\text{ V}$ $f = 100\text{ kHz}$
Switching Energy during turn-on	$E_{on}$		134.1		$\mu\text{J}$	$V_{DS} = 400\text{ V}$ , $I_{DS} = 20\text{ A}$ $V_{GS} = 0-6\text{ V}$ $R_{G(on)} = 10\ \Omega$ , $R_{G(off)} = 1\ \Omega$ $L = 120\ \mu\text{H}$ $L_P = 2\text{ nH}$ (notes 5, 6)
Switching Energy during turn-off	$E_{off}$		17		$\mu\text{J}$	

**Figure 5-1: GS66516T data sheet [69]**

$$td_{PWM} > td_{gate} + (td_{(off)} - td_{(on)}) \quad (5 - 1)$$

$$td_{PWM} > 60ns + (14.9ns - 4.6ns) = 70.3ns \quad (5 - 2)$$

$$td_{PWM} = 100ns \quad (5 - 3)$$

## 5.2 Thermal Management

For thermal management, good thermal conductivity with minimum thermal resistance in the heat flow path should be considered. The heat flow path is shown in Figure 5-2. The GS66516T is a top-side cooled transistor. Therefore, the thermal resistance of PCB is not part of the heat flow. Total thermal resistance can be calculated with equation (5 - 4) [70]. Where  $R_{\theta_{jc}}$  is the thermal resistance between junction and case,  $R_{\theta_{TIM}}$  is the thermal resistance of the TIM (Thermal Interface Material), and  $R_{\theta_{HS}}$  is the thermal resistance of the heat sink.

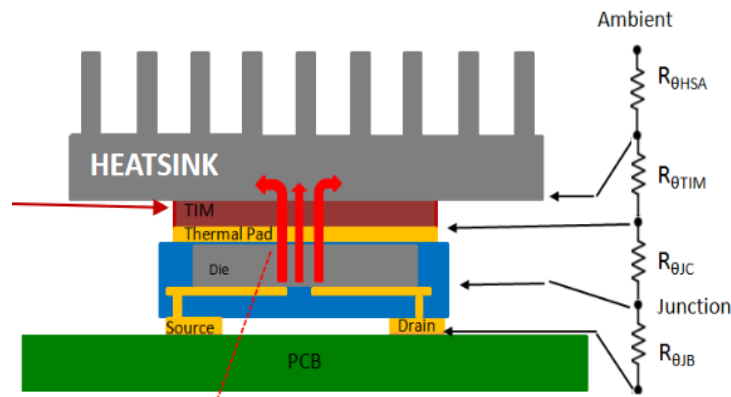


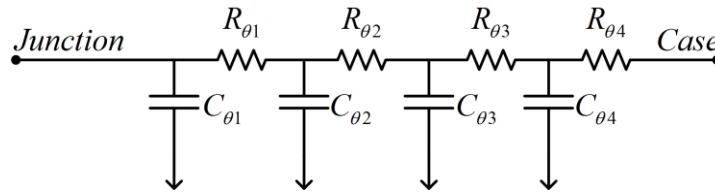
Figure 5-2: Direction of heat flow [70]

$$R_{\theta_{ja}} = R_{\theta_{jc}} + R_{\theta_{TIM}} + R_{\theta_{HS}} \quad (5 - 4)$$

### 5.2.1 Junction-to-Case Thermal Resistance

The RC thermal model for GS66516T is shown in Figure 5-3. The thermal resistance between junction and case is calculated to be  $0.27^{\circ}\text{C}/\text{W}$  with equation (5 - 5) and (5 - 6). All of the numbers are from the GS66516T datasheet.





**Figure 5-3: GS66516T RC thermal model [69]**

$$R_{\theta_{jc}} = R_{\theta_1} + R_{\theta_2} + R_{\theta_3} + R_{\theta_4} \quad (5 - 5)$$

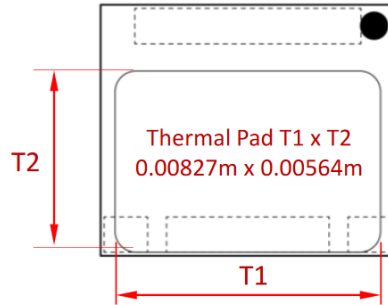
$$R_{\theta_{jc}} = 0.008^{\circ}\text{C}/\text{W} + 0.124^{\circ}\text{C}/\text{W} + 0.130^{\circ}\text{C}/\text{W} + 0.008^{\circ}\text{C}/\text{W} = 0.27^{\circ}\text{C}/\text{W} \quad (5 - 6)$$

### 5.2.2 TIM Thermal Resistance

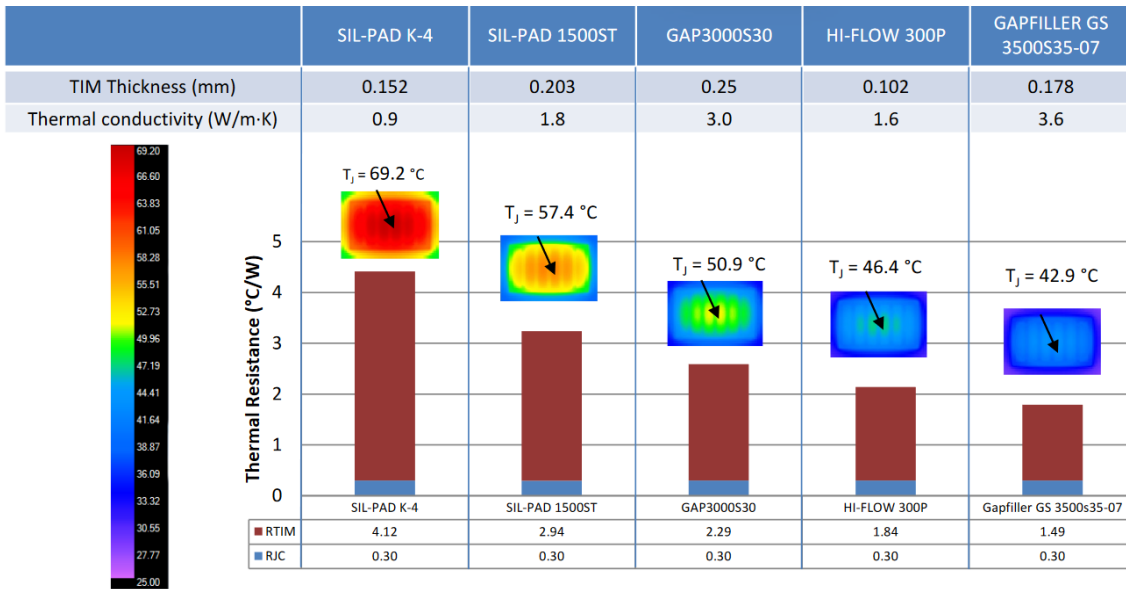
The thermal resistance of TIM depends on the material thermal conductivity, thickness, and contact area as shown in equation (5 - 7). Where  $h$  is the thickness in m,  $A$  is the contact area in  $\text{m}^2$  and  $k$  is thermal conductivity in  $\text{W}/\text{m}\cdot\text{K}$ .

GS66516T has a smaller physical size than other power MOSFETs so as the thermal pad contact area. The contact area is shown in Figure 5-4. Based on the equation (5 - 7), the smaller the contact area, the larger the thermal resistance is. Therefore, the TIM for GS66516T should either show excellent thermal conductivity or thinner or both. But these two factors are hard to be achieved at the same time. A comparison between different types of TIM is done by GaN Systems, as shown in Figure 5-5. The TIM used in this experiment is HI-FLOW 300P. The thermal resistance of this TIM is around  $1.84^{\circ}\text{C}/\text{W}$ .

$$R_{\theta TIM} = \frac{h}{A \times k} \quad (5 - 7)$$



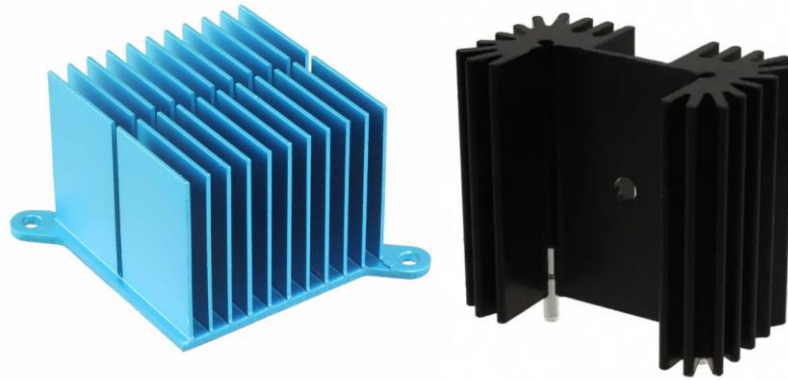
**Figure 5-4: Contact area of thermal pad [70]**



**Figure 5-5: TIM selection for GS66516T [70]**

### 5.2.3 Heat Sink Thermal Resistance

The heat sinks used for GaN E-HEMTs in this experiment are from Advanced Thermal Solutions Inc. as shown in Figure 5-6 (a). The heat sink has a thermal resistance of 1°C/W at 400 LFM airflow. The heat sinks used for power MOSFETs have the same thermal resistance, as shown in Figure 5-6 (b).



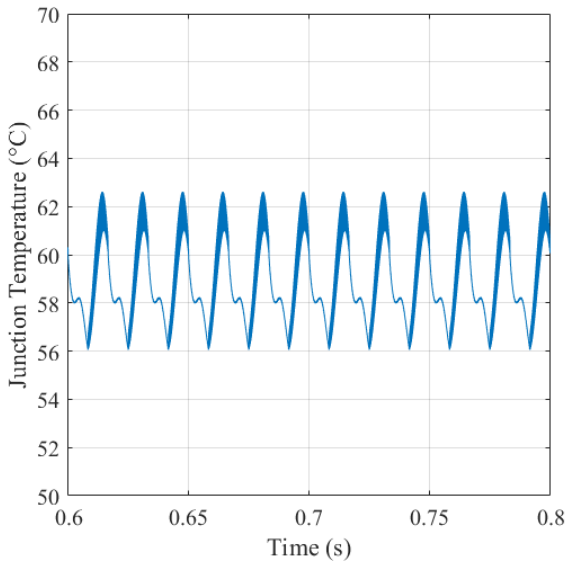
**Figure 5-6: Heat sink used for: (a) GaN E-HEMTs [71]; (b) MOSFETs [72]**

#### **5.2.4 Junction Temperature**

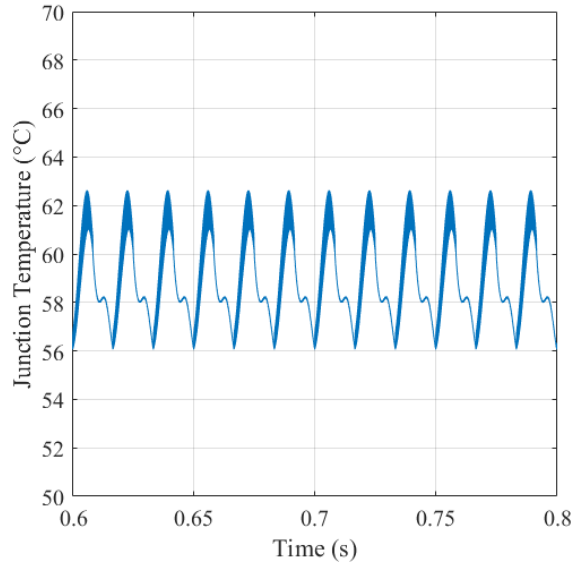
The total thermal resistance is  $3.11^{\circ}\text{C}/\text{W}$  as calculated in (5 - 8). After the estimation of the total thermal resistance, the junction temperature can be calculated using equation (5 - 9). Where  $T_j$  is the junction temperature,  $P_{Loss}$  is the total dissipated power,  $R_{\theta ja}$  is the total thermal resistance, and  $T_{amb}$  is the ambient temperature. Assume the ambient temperature is  $25^{\circ}\text{C}$ . Instead of calculation, the junction temperature is simulated in PLECS at level 2 charging mode full load condition, as shown in Figure 5-7. The junction temperature of GaN transistors  $S_1$  and  $S_2$  in totem-pole is below  $70^{\circ}\text{C}$ , as shown in Figure 5-7 (a) and (b). The junction temperature of MOSFETs  $S_3$  and  $S_4$  is below  $50^{\circ}\text{C}$ , as shown in Figure 5-7 (c) and (d). The junction temperature of GaN transistors  $S_5$  and  $S_6$  in the synchronous buck converter is below  $70^{\circ}\text{C}$  and  $30^{\circ}\text{C}$ , as shown in Figure 5-7 (e) and (f).

$$\begin{aligned}
 R_{\theta ja} &= R_{\theta jc} + R_{\theta TIM} + R_{\theta HS} \\
 &= 0.27^{\circ}\text{C}/\text{W} + 1.84^{\circ}\text{C}/\text{W} + 1^{\circ}\text{C}/\text{W} \\
 &= 3.11^{\circ}\text{C}/\text{W}
 \end{aligned}
 \tag{5 - 8}$$

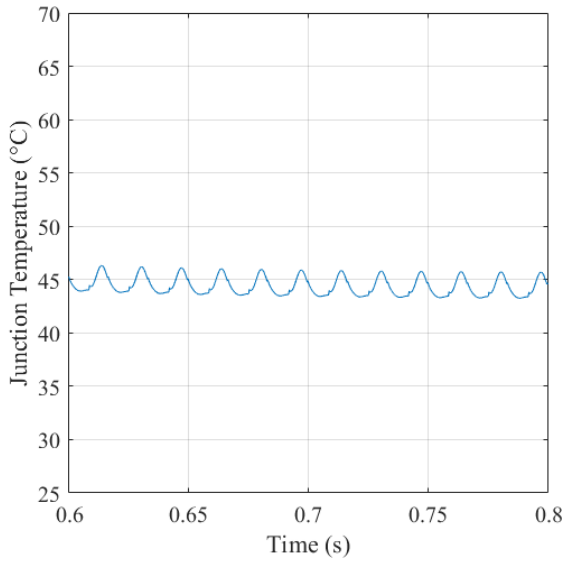
$$T_j = P_{Loss} \times R_{\theta ja} + T_{amb}
 \tag{5 - 9}$$



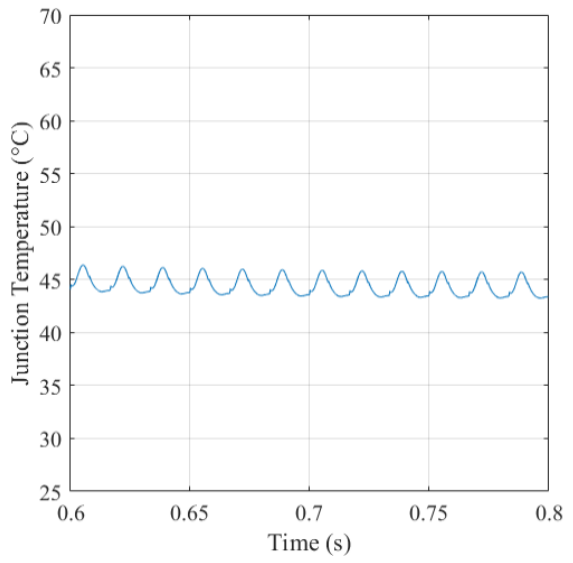
(a)



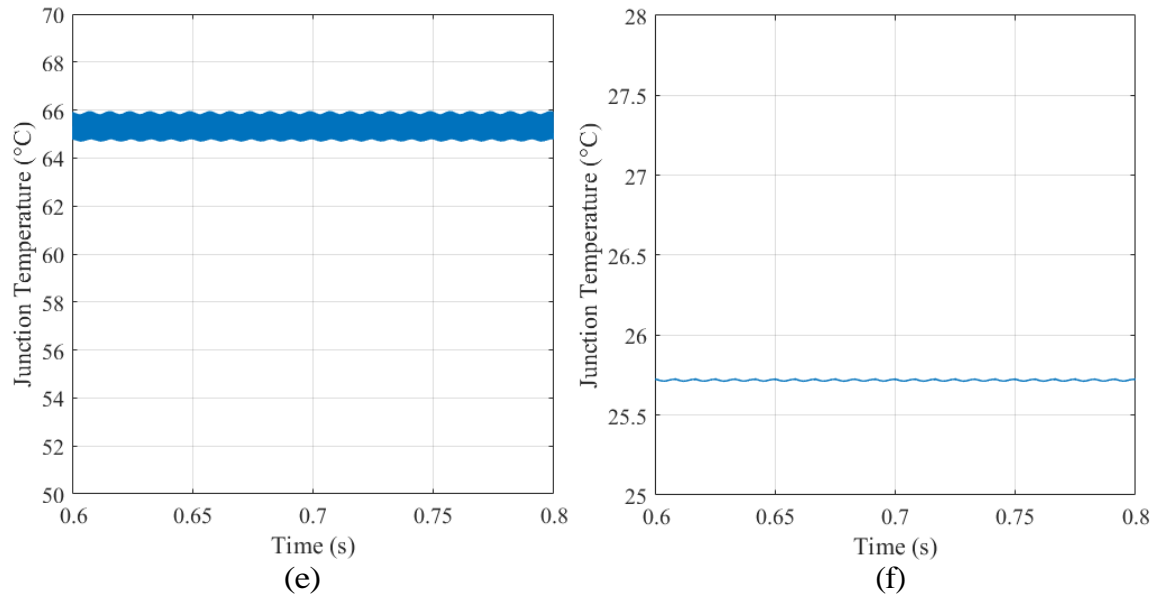
(b)



(c)



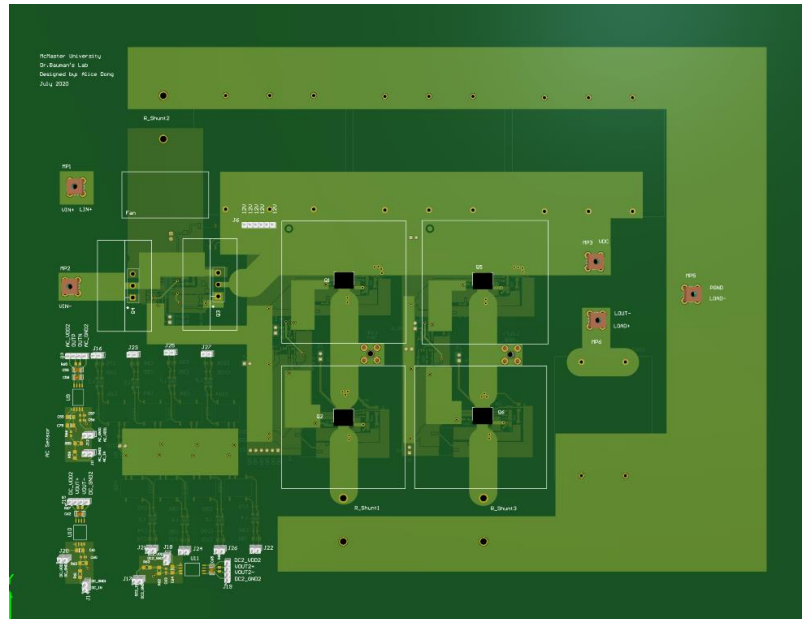
(d)



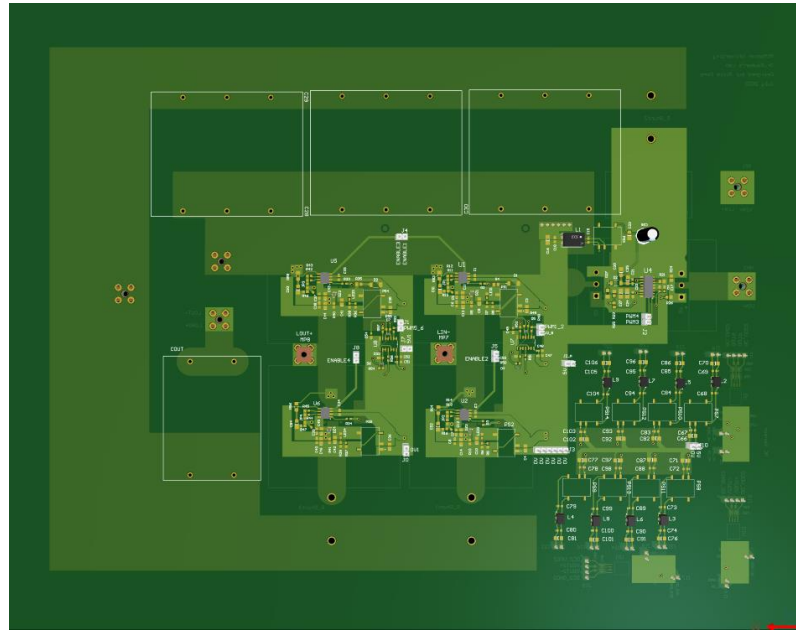
**Figure 5-7: Junction temperature of: (a) S<sub>1</sub>; (b) S<sub>2</sub>; (c) S<sub>3</sub>; (d) S<sub>4</sub>; (e) S<sub>5</sub>; (f) S<sub>6</sub>**

### 5.3 PCB Design

A complete overview of the two-layer PCB is shown in Figure 5-8 (a) and (b) for the top layer and bottom layer, respectively.



(a)

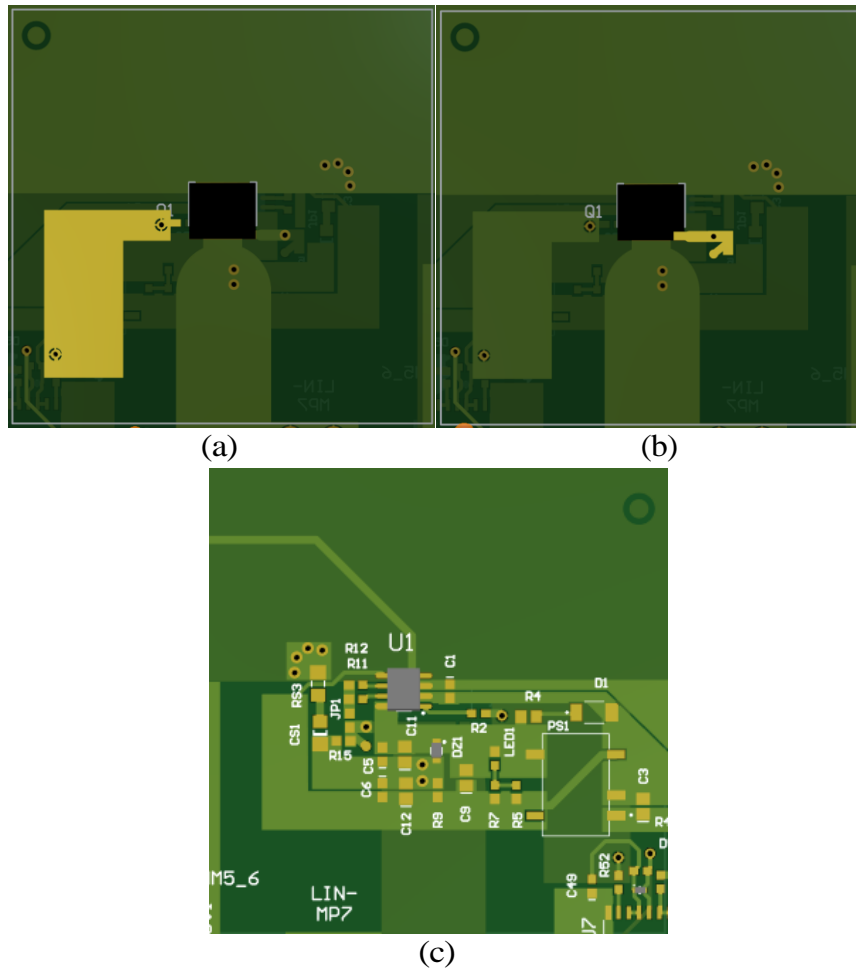


(b)

**Figure 5-8: PCB layout of the proposed OBC: (a) top layer; (b) bottom layer**

### 5.3.1 Gate Driver and PWM

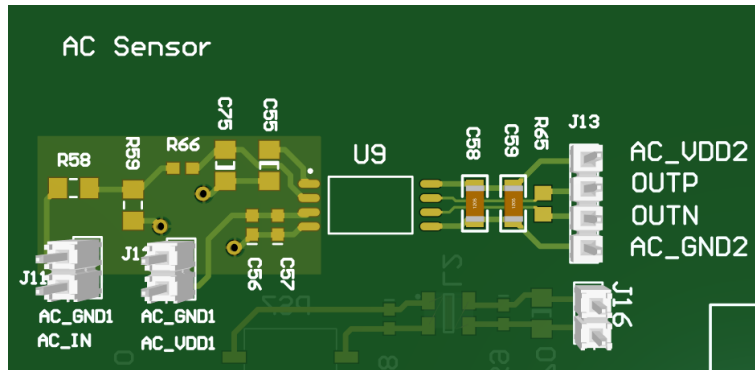
The gate driver should be located as close to the GaN transistor to minimize parasitic inductance. Besides, the gate and PWM trace paths must be kept short to provide the best noise performance. Therefore, separate planes are used in designing the PCB. The GaN transistor is top side cooled transistor and is located in the top layer of the PCB. The gate driver circuits are located at the bottom layer of the PCB. The 3D model of GS66516T with highlighted PWM trace path and gate trace path is shown in Figure 5-9 (a) and (b), respectively. The gate driver circuit is shown in Figure 5-9 (c).



**Figure 5-9: PCB design of: (a) PWM path; (b) gate path; (c) gate driver**

### 5.3.2 AC Voltage Sensor

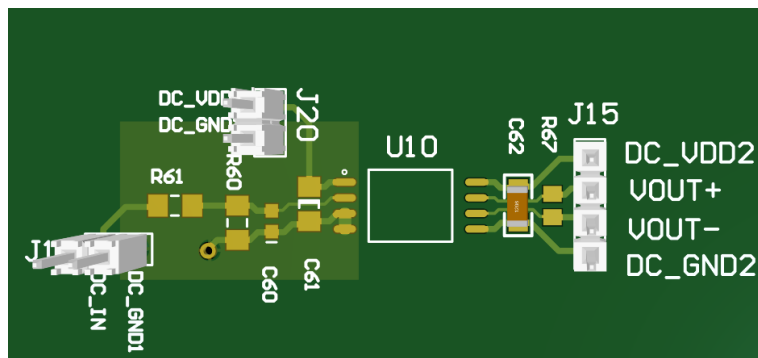
The isolated AC voltage sensor used to measure the 60 Hz line voltage is chip ISO224 from TI. The PCB design layout for the AC voltage sensing circuit is shown in Figure 5-10. The output voltage of the sensor is between -4 V to 4 V. The results are used for polarity detection and peak detection in the control.



**Figure 5-10: AC voltage sensor PCB design**

### 5.3.3 DC Voltage Sensor

The isolated DC voltage sensor used to measure the dc-link voltage and output voltage is chip ACPL-C87A from Broadcom. The PCB design layout for the DC voltage sensing circuit is shown in Figure 5-11.

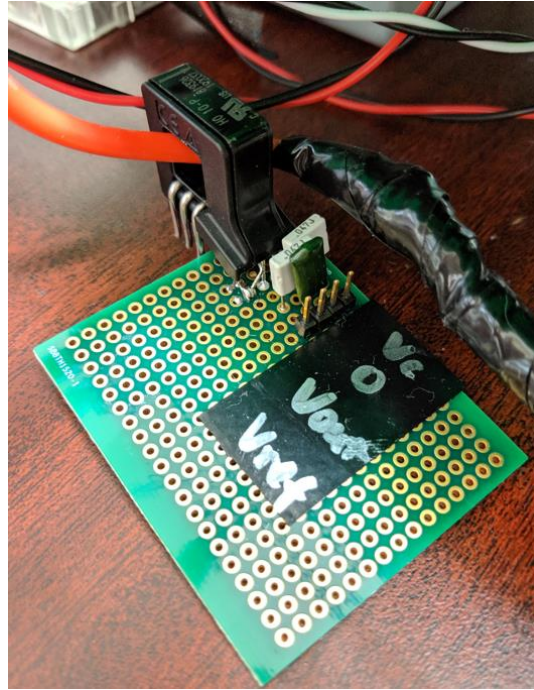


**Figure 5-11: DC voltage sensor PCB design**

### 5.3.4 Current Sensor

The current sensor chosen in this design is from LEM HO-25-P and is built on the small prototype board shown in Figure 5-12.



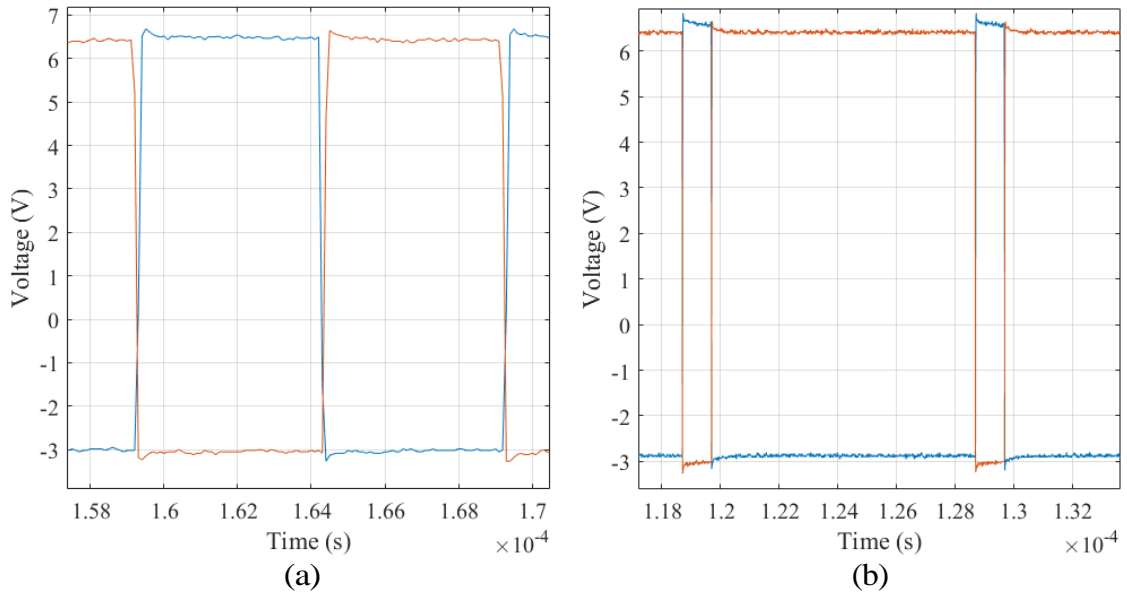


**Figure 5-12: Current sensor**

## **5.4 Experimental Results**

### **5.4.1 Gate-to-Source Voltage**

The gate-to-source voltage ( $V_{gs}$ ) waveform for top and bottom GaN transistors is examined at 100 kHz switching frequency and at different duty cycles. The results are shown in Figure 5-13 (a) and (b) at 50% duty cycle and 10% duty cycle, respectively. The complementary PWM pair is generated internally with 74VHC132, Quad 2-Input NAND Schmitt Trigger.  $V_{gs}$  is regulated with isolated 5 V to 9 V dc-dc converter and 6.2 V zener diode. Therefore, the gate drive should produce around 6V positive gate bias for turn on and around 3V negative gate bias for turn off, as shown in Figure 5-13. The negative gate bias is to prevent false turn-on.



**Figure 5-13:  $V_{gs}$  waveforms at: (a) 50% duty cycle; (b) 10% duty cycle**

#### 5.4.2 Polarity Detection

The polarity detection algorithm is implemented in Simulink with zero-crossing noise issue considered. It should be high when the input voltage is greater than zero and be low when the input voltage is less than zero. The experimental result is shown in Figure 5-14. Channel 1 is AC voltage sensor output. Channel 2 is polarity detection. Channel 7 is the input line voltage after the AC line filter and transformer. The results show that the polarity algorithm gives a clear waveform even with sensor noise at zero-crossing.

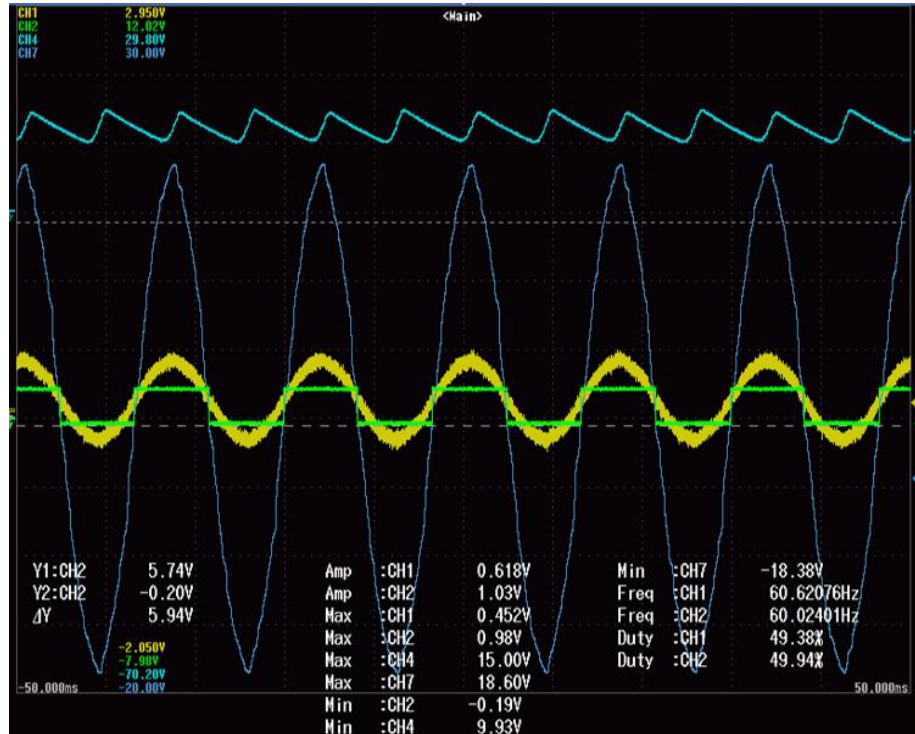
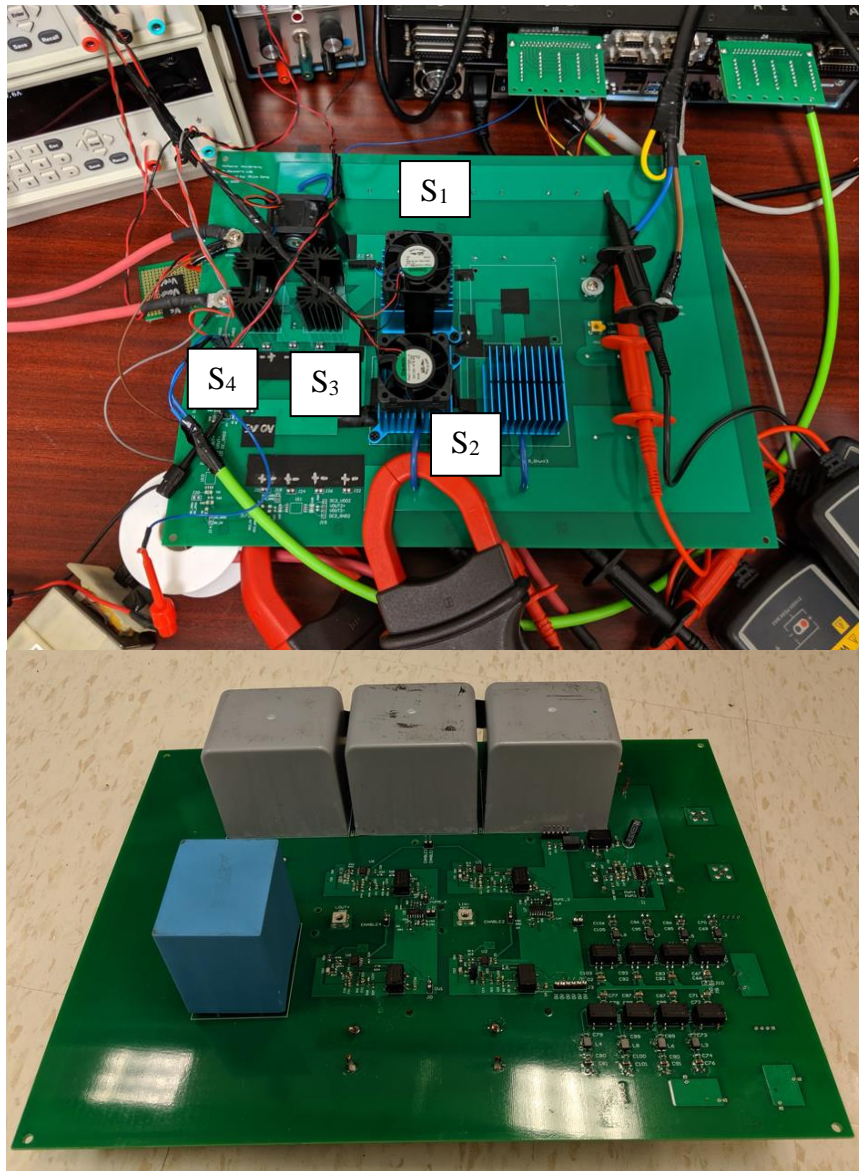


Figure 5-14: Polarity detection

### 5.4.3 Open-Loop Test

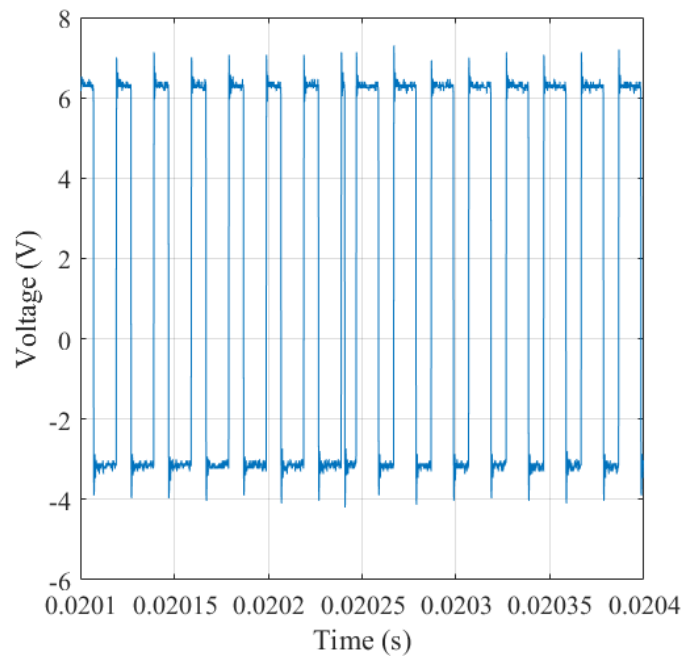
The experimental setup is shown in Figure 5-15. The control is implemented with Opal-RT. The open-loop test is implemented on the totem-pole PFC stage first. ITEC electronic DC load is connected across the dc-link.



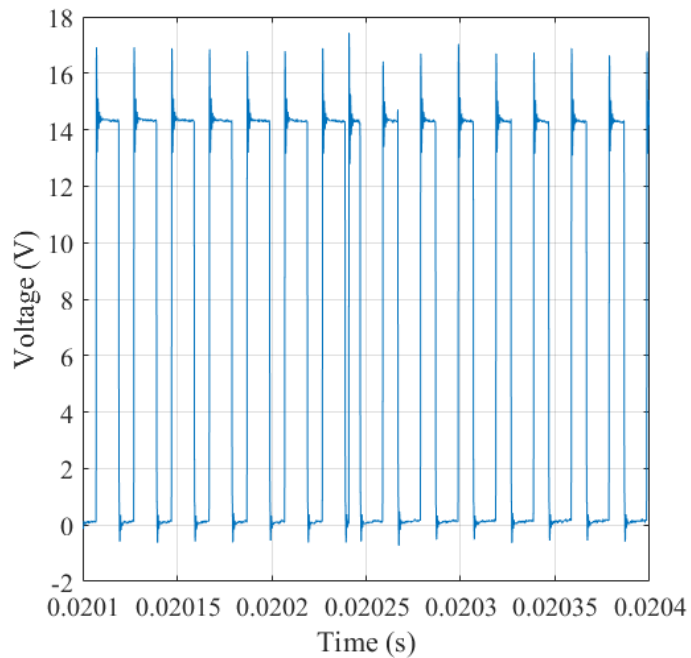
**Figure 5-15: Experimental setup**

The pre-charge stage of the dc-link capacitor is done by keeping  $S_1$ ,  $S_2$ ,  $S_3$ , and  $S_4$  off and the circuit works as a rectifier.  $S_1$  and  $S_2$  are switching complementary after the pre-charge. The experimental results of  $V_{gs}$  and drain-to-source voltage ( $V_{ds}$ ) switching at 50 kHz with 40% duty cycle are shown in Figure 5-16 and Figure 5-17, respectively. The waveforms show that the open-loop is working well as  $V_{ds}$  equals zero when the switch is

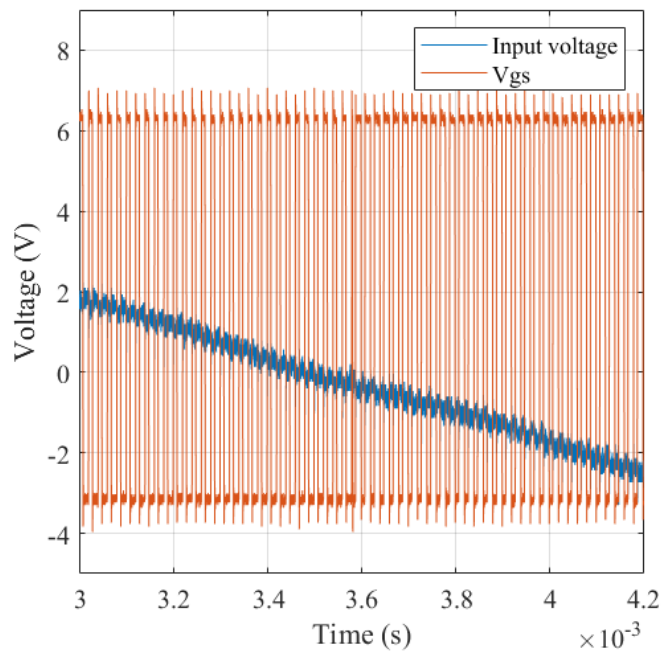
on and  $V_{ds}$  equals the output voltage when the switch is off. The change in the middle in Figure 5-16 and Figure 5-17 happens where the polarity of the input voltage changes. The polarity change is easier to be seen when comparing with the input voltage, as shown in Figure 5-18. The input voltage and current waveform are shown in Figure 5-19. The output voltage is shown in Figure 5-20.



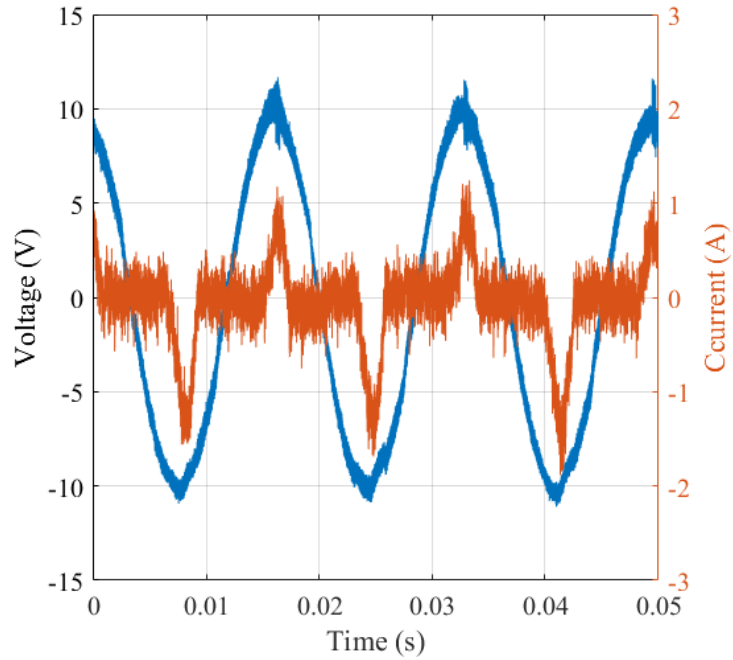
**Figure 5-16:  $V_{gs}$  for  $S_2$  switching at 50 kHz with 40% duty cycle**



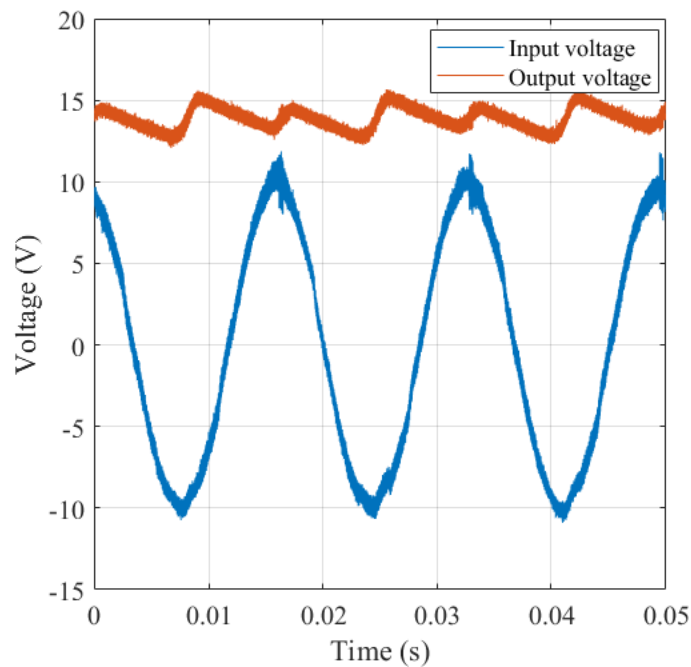
**Figure 5-17: Vds for S<sub>2</sub> switching at 50 kHz with 40% duty cycle**



**Figure 5-18: Vgs when polarity changes with 40% duty cycle**



**Figure 5-19: Input voltage and current waveform with 40% duty cycle**



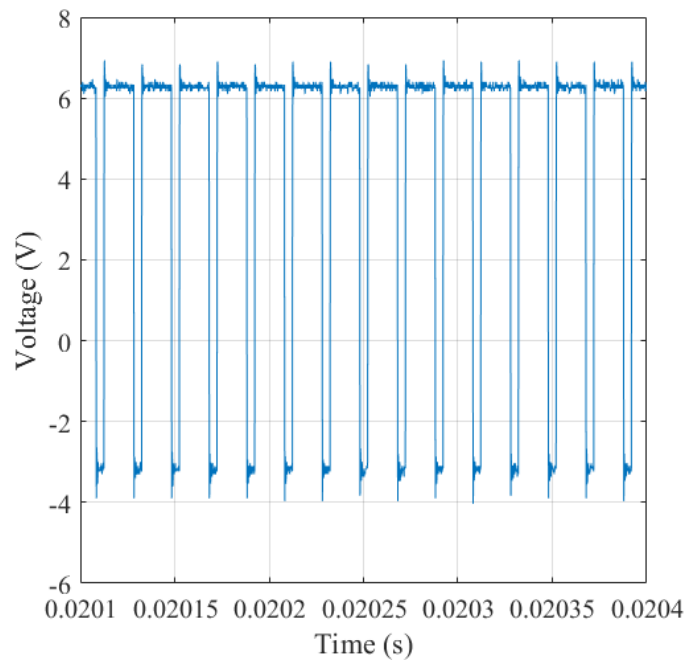
**Figure 5-20: Input voltage and output voltage with 40% duty cycle**

The same open-loop test is done with 20% duty cycle.  $V_{gs}$  waveform for the bottom switch  $S_2$  switching at 50 kHz is shown in Figure 5-21.  $V_{ds}$  waveform is shown in Figure

5-22. The polarity change is shown in Figure 5-23. The input current and voltage waveform is shown in Figure 5-24. The input and output voltage is shown in Figure 5-25. Comparing the output voltage at two duty cycles. The average output voltage at 20% duty cycle is around 10.5 V and the average output voltage at 40% duty cycle is around 14 V. These numbers match the boost converter equation as shown in equation (5 - 10) and (5 - 11).

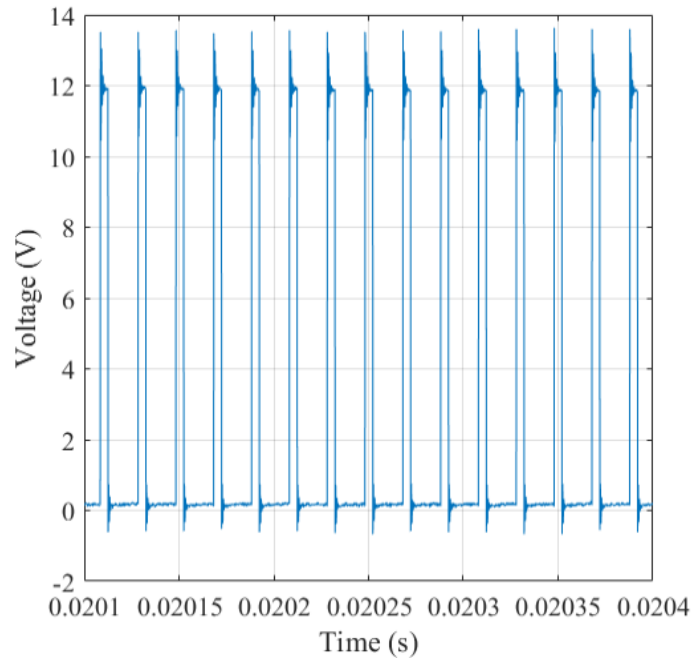
$$V_{out} = \frac{V_{in}}{1-D} \quad (5 - 10)$$

$$\frac{V_{out_1}}{V_{out_2}} = \frac{1-D_2}{1-D_1} = \frac{1-0.4}{1-0.2} = \frac{3}{4} = \frac{10.5V}{14V} \quad (5 - 11)$$

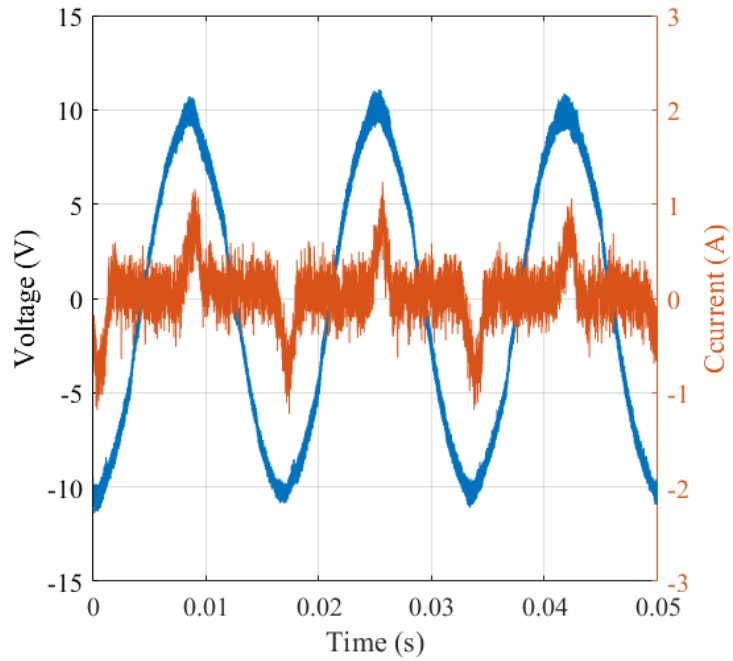


**Figure 5-21: Vgs for S2 switching at 50 kHz with 20% duty cycle**

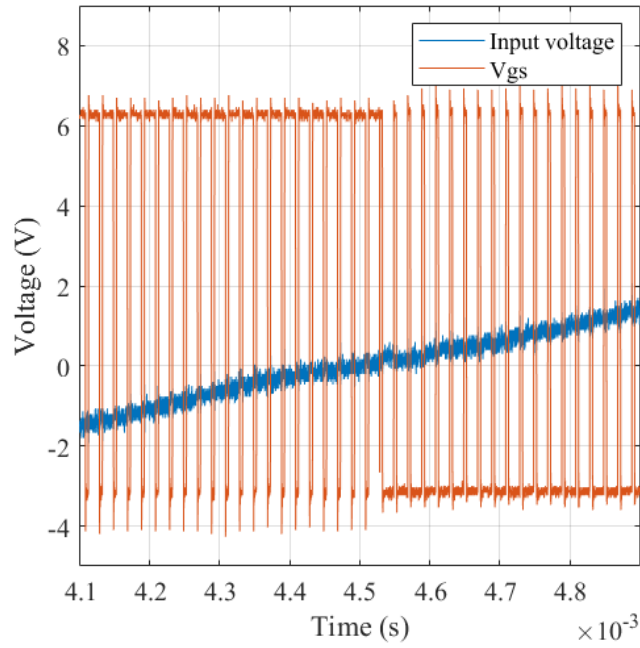




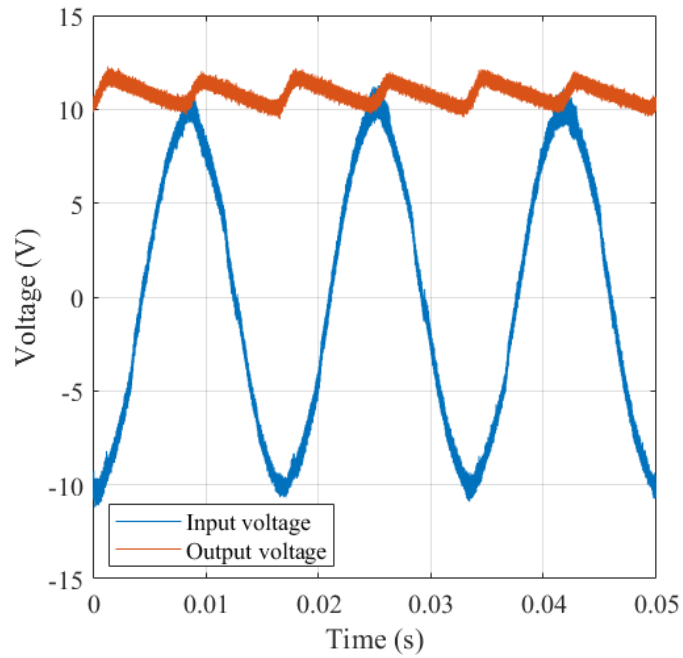
**Figure 5-22: Vds for S<sub>2</sub> switching at 50 kHz with 20% duty cycle**



**Figure 5-23: Input voltage and current waveform with 20% duty cycle**



**Figure 5-24: Vgs when polarity changes with 20% duty cycle**



**Figure 5-25: Input voltage and output voltage with 20% duty cycle**

# Chapter 6

## Conclusion and Future Work

## 6.1 Summary

The OBC is one of the essential parts of EVs. A high efficiency, high power density, and compact OBC can shorten the charging time or expand the driving range. This thesis gives a review of isolated and non-isolated OBC topologies in Chapter 2. The non-isolated OBC is considered as an option to go transformer-less and therefore, boost up the efficiency and reduce the cost. Chapter 2 introduces different approaches to reduce the size of dc-link capacitors with active filtering techniques. Chapter 2 also introduces the advantage of synchronous rectification.

In Chapter 3, GaN-based Non-isolated OBC with Active Filtering is introduced as the proposed topology. The proposed OBC uses the minimum number of components, improved efficiency and PF, reduces the size of the dc-link film capacitor without adding additional components, and provides the wide operation range. The active filtering is achieved by allowing ac components across the dc-link and uses a synchronous buck converter to create the complementary duty cycle to cancel out the voltage ripple.

Chapter 4 includes the detailed design process of dc-link capacitance. Look-up tables are generated for level 1 and level 2 charging separately to ensure the optimal efficiency at each output voltage level. Chapter 4 provides the simulation results of level 1 and level 2 charging in terms of efficiency, THD%, and PF. At level 2 charging mode, the peak efficiency is over 98.8% and full load efficiency is around 98.6%. The THD% is less than 5% and the PF is over 0.998 at full load. At level 1 charging mode, the peak efficiency is over 98.3% and the full load efficiency is around 97.4%. The THD% is less than 4% and

PF is over 0.998 at full load. The input current ripple is less than 15% and the output voltage ripple is less than 2%.

Chapter 5 shows the PCB design layout and design considerations to ensure the best performance. The Gate driver circuit and PWM trace path have been carefully designed. The high power trace path and control trace path is designed on the opposite layer. Chapter 5 also includes a design layout of an isolated AC voltage sensor, an isolated DC voltage sensor, and a current sensor as control inputs. Thermal management is also part of the design including the selection of TIM, heat sink, and fan. Open-loop experimental results are included at the end.

## **6.2 Future Work**

The future work is to close the loop. The closed-loop experiments include an inner current loop and an outer voltage loop. The inner current loop needs to be tested first to ensure the input current will follow the change of reference current. Then the outer voltage loop can be added to regulate the output voltage level. After the validation of the totem-pole PFC in the experiment, the synchronous buck converter can be added to the circuit to achieve active filtering. At level 1 charging mode, efficiency map, THD%, and PF can be generated. After the level 1 experiment, the same experiment can be implemented at the level 2 charging mode.

The non-isolated chargers should have further investigation. Many papers support the non-isolated structure. However, not too many have been put into production in the EVs market. Furthermore, a more compact electro-thermal design can be done in the future to compress the product size.

Broader applications in electro mobility can be considered in the future. The proposed non-isolated OBC is designed for but not limited to electric vehicles. Other potential products include e-bikes, e-scooters, electric hoverboards, etc. can also be included. Future work will involve design and prototyping the proposed topology for lower voltage and power levels suitable for smaller electro-mobility applications.

## 7 References

- [1] "Global and U.S. electric vehicle trends," ICCT, [Online]. Available: [https://theicct.org/sites/default/files/Drew%20Kodjak\\_Canada%20global%20EV\\_12June2019\\_0.pdf](https://theicct.org/sites/default/files/Drew%20Kodjak_Canada%20global%20EV_12June2019_0.pdf).
- [2] "Sales of fuel used for road motor vehicles, annual (x 1,000)," Statistics Canada, 2020. [Online]. Available: <https://www150.statcan.gc.ca/t1/tbl1/en/tv.action?pid=2310006601>.
- [3] "Learn the facts: Emissions from your vehicle," Natural Resources Canada, [Online]. Available: [file:///C:/Users/dongjx/Documents/Thesis/autosmart\\_factsheet\\_9\\_e.pdf](file:///C:/Users/dongjx/Documents/Thesis/autosmart_factsheet_9_e.pdf).
- [4] "How Do All-Electric Cars Work?," U.S Department of Energy, [Online]. Available: <https://afdc.energy.gov/vehicles/how-do-all-electric-cars-work>.
- [5] "Electric Car Charging Cost and Time Calculator," [Online]. Available: <https://evcompare.io/charging-calculator/>.
- [6] X. Gong, J. Rangaraju, "Taking charge of electric vehicles – both in the vehicle and on the grid," Texas Instruments, 2018. [Online]. Available: <http://www.ti.com/lit/wp/szzy007/szzy007.pdf>.
- [7] D. Cesieli, C. Zhu, "A Closer Look at the On-Board Charger: The development of the second-generation module for the Chevrolet Volt," *IEEE Electrification Magazine*, vol. 5, no. 1, p. 36 - 42, 2017.
- [8] Y. Kim, W. Sung, B. Lee, "Comparative Performance Analysis of High Density and Efficiency PFC Topologies," *IEEE Transactions on Power Electronics*, vol. 29, no. 6, p. 2666 - 2679, 2014.
- [9] "High Efficiency CCM Bridgeless Totem Pole PFC Design using GaN E-HEMT," GaN Systems, 2017. [Online]. Available: <https://gansystems.com/wp-content/uploads/2018/01/GS665BTP-REF-rev170905.pdf>.
- [10] Z. Liu, F. Lee, Q. Li, Y. Yang, "Design of GaN-Based MHz Totem-Pole PFC Rectifier," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, p. 799 - 807, 2016.
- [11] Y. Tang, W. Ding, A. Khaligh, "A bridgeless totem-pole interleaved PFC converter for plug-in electric vehicles," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016.
- [12] Z. Liu, B. Li, F. Lee, Q. Li, "High-Efficiency High-Density Critical Mode Rectifier/Inverter for WBG-Device-Based On-Board Charger," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, p. 9114 - 9123, 2017.
- [13] A. Huang, "Wide bandgap (WBG) power devices and their impacts on power delivery systems," in *2016 IEEE International Electron Devices Meeting (IEDM)*, 2016.

- [14] Q. Huang, A. Huang, "Review of GaN totem-pole bridgeless PFC," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 3, p. 187 - 196, 2017.
- [15] L. Zhou, Y. Wu, J. Honea, Z. Wang, "High-efficiency True Bridgeless Totem Pole PFC based on GaN HEMT: Design Challenges and Cost-effective Solution," in *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2015.
- [16] N. Korada, R. Ayyanar, "A 3kW, 500 kHz E-mode GaN HEMT based Soft-switching Totem-pole PFC," in *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2019.
- [17] Z. Liu, X. Huang, M. Mu, Y. Yang, F. Lee, Q. Li, "Design and evaluation of GaN-based dual-phase interleaved MHz critical mode PFC converter," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014.
- [18] Z. Liu, Z. Huang, F. Lee, Q. Li, "Digital-Based Interleaving Control for GaN-Based MHz CRM Totem-Pole PFC," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, p. 808 - 814, 2016.
- [19] J. Sun, N. Strain, D. Costinett, L. Tolbert, "Analysis of a GaN-Based CRM Totem-Pole PFC Converter Considering Current Sensing Delay," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019.
- [20] Q. Huang, R. Yu, A. Huang, W. Yu, "Adaptive zero-voltage switching control and hybrid current control for high efficiency GaN-based MHz Totem-pole PFC rectifier," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017.
- [21] J. Sun, X. Huang, N. Strain, D. Costinett, L. Tolbert, "Inductor Design and ZVS Control for a GaN-Based High Efficiency CRM Totem-Pole PFC Converter," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019.
- [22] P. He, A. Khaligh, "Comprehensive Analyses and Comparison of 1 kW Isolated DC-DC Converters for Bidirectional EV Charging Systems," *IEEE Transactions on Transportation Electrification*, vol. 3, no. 1, p. 147 - 156, 2017.
- [23] P. He, A. Mallik, A. Sankar, A. Khaligh, "Design of a 1-MHz High-Efficiency High-Power-Density Bidirectional GaN-Based CLLC Converter for Electric Vehicles," *IEEE Transactions on Vehicular Technology*, vol. 8, no. 1, p. 213 - 223, 2019.
- [24] T. Schobre, K. Siebke, R. Mallwitz, "Design of a GaN based CLLC converter with synchronous rectification for on-board vehicle charger," in *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2019.
- [25] B. Whitaker, A. Barkley, Z. Cole, B. Passmore, D. Martin, T. McNutt, A. Lostetter, J. Lee, K. Shiozaki, "A High-Density, High-Efficiency, Isolated On-



- Board Vehicle Battery Charger Utilizing Silicon Carbide Power Devices," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, p. 2606 - 2617, 2014.
- [26] C. Shi, H. Wang, S. Dusmez, A. Khaligh, "A SiC-Based High-Efficiency Isolated Onboard PEV Charger With Ultrawide DC-Link Voltage Range," *IEEE Transactions on Industry Applications*, vol. 53, no. 1, p. 501 - 511, 2017.
- [27] H. Li, S. Wang, Z. Zhang, J. Tang, X. Ren, Q. Chen, "A SiC Bidirectional LLC On-Board Charger\*," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019.
- [28] X. Gong, G. Wang, M. Bhardwaj, "6.6kW Three-Phase Interleaved Totem Pole PFC Design with 98.9% Peak Efficiency for HEV/EV Onboard Charger," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019.
- [29] P. Johnson, Kevin. Bai, "A dual-DSP controlled SiC MOSFET based 96%-efficiency 20kW EV on-board battery charger using LLC resonance technology," in *2017 IEEE Symposium Series on Computational Intelligence (SSCI)*, 2017.
- [30] C. Wei, J. Shao, B. Agrawal, D. Zhu, H. Xie, "New Surface Mount SiC MOSFETs Enable High Efficiency High Power Density Bi-directional On-Board Charger with Flexible DC-link Voltage," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019.
- [31] C. Oh, D. Kim, D. Woo, W. Sung, Y. Kim, B. Lee, "A High-Efficient Nonisolated Single-Stage On-Board Battery Charger for Electric Vehicles," *IEEE Transactions on Power Electronics*, vol. 28, no. 12, p. 5746 - 5757, 2013.
- [32] F. Freschi, M. Mitolo, R. Tommasini, "Electrical Safety of Plug-In Electric Vehicles: Shielding the Public from Shock," *IEEE Industry Applications Magazine*, vol. 24, no. 3, p. 58 - 63, 2018.
- [33] Y. Zhang, G. Yang, X. He, M. Elshaer, W. Perdikakis, H. Li, C. Yao, J. Wang, K. Zou, Z. Xu, C. Chen, "Leakage Current Issue of Non-Isolated Integrated Chargers for Electric Vehicles," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018.
- [34] A. Albanna, M. Arafat, A. Gupta, M. Anwar, M. Teimor, "Analysis of ground fault currents in isolated and non-isolated charging modules in electric vehicles," in *2015 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2015.
- [35] "Underwriters Laboratories Inc. Standard for Safety Personnel Protection Systems for Electric Vehicle (EV) Supply Circuits: Particular Requirements for Protection Devices for Use in Charging Systems," *UL 2231-2*, Feb 2011.
- [36] "Underwriters Laboratories Inc. Standard for Safety Ground-fault circuit-interrupters," *UL 943*, May 2010.
- [37] "Level1 and Level2 Electric Vehicle Service Equipment (EVSE) Reference Design," Texas Instruments Incorporated, Feb 2016. [Online]. Available: [www.ti.com/lit/ug/tidub87/tidub87.pdf](http://www.ti.com/lit/ug/tidub87/tidub87.pdf).
- [38] A. Praneeth, S. Williamson, "Modeling, Design, Analysis, and Control of a Nonisolated Universal On-Board Battery Charger for Electric Transportation,"

- IEEE Transactions on Transportation Electrification*, vol. 5, no. 4, pp. 912-924, 2019.
- [39] B. Keogh, "Power Factor Correction Using the Buck Topology—Efficiency Benefits and Practical Design Considerations," *2010 Texas Instruments Power Supply Design Seminar*, 2010.
- [40] S. Yu, H. Chen, "A comparison study of boost and Buck-boost power factor corrector for ultra-wide input voltage range applications," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014.
- [41] A. Singh, M. Pathak, "An improved two-stage non-isolated converter for on-board plug-in hybrid EV battery charger," in *2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*, 2016.
- [42] M. Khan, A. Ahmed, I. Husain, Y. Sozer, M. Badawy, "Performance Analysis of Bidirectional DC–DC Converters for Electric Vehicles," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, p. 3442 - 3452, 2015.
- [43] H. Wen, X. Wen, J. Liu, X. Guo, F. Zhao, "A low-inductance high-frequency film capacitor for electric vehicles," in *2007 International Conference on Electrical Machines and Systems (ICEMS)*, 2007.
- [44] H. Wen, W. Xiao, Xuhui Wen, "Comparative evaluation of DC link capacitors for electric vehicle application," in *2012 IEEE International Symposium on Industrial Electronics*, 2012.
- [45] H. Dornecker, B. Engelhard, "Selecting and Applying Film Capacitors," EDN, 2001. [Online]. Available: <https://www.edn.com/selecting-and-applying-film-capacitors/>.
- [46] M. Hinkkanen, J. Luomi, "Induction Motor Drives Equipped With Diode Rectifier and Small DC-Link Capacitance," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 1, p. 312 - 320, 2008.
- [47] W. Lee, S. Sul, "DC-Link Voltage Stabilization for Reduced DC-Link Capacitor Inverter," *IEEE Transactions on Industry Applications*, vol. 50, no. 1, p. 404 - 414, 2014.
- [48] S. Li, W. Qi, J. Wu, S. Tan, S. Hui, "Minimum Active Switch Requirements for Single-Phase PFC Rectifiers Without Electrolytic Capacitors," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, p. 5524 - 5536, 2019.
- [49] D. Patil, V. Agarwal, "Compact Onboard Single-Phase EV Battery Charger With Novel Low-Frequency Ripple Compensator and Optimum Filter Design," *IEEE Transactions on Vehicular Technology*, vol. 65, no. 4, p. 1948 - 1956, 2016.
- [50] Y.i Huang, Y. Zhang, C. Rui, J. Liu, "An Automatic Power Decoupling Control Method on Three Level DC-AC Converter to Suppress the Double-Line-Frequency Ripple," in *2019 IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2019.

- [51] Y. Huang, Y. Zhang, X. Li, J. Liu, P. Fang , "A Novel Double-Line-Frequency Ripple Suppression Method for Single Phase DC-AC Converter Based on Three-Level Topology," in *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2018.
- [52] G. Knabben, L. Schmitz, O. Custodio, R. Medeiros, A. Bettiol, D. Martins, R. Coelho , "Photovoltaic micro-inverter with active filtering and thin-film capacitors," in *2017 Brazilian Power Electronics Conference (COBEP)*, 2017.
- [53] T. Shimizu, Y. Jin, G. Kimura , "DC ripple current reduction on a single-phase PWM voltage-source rectifier," *IEEE Transactions on Industry Applications*, vol. 36, no. 5, p. 1419 - 1429, 2000.
- [54] Y. Qin, H. Chung, D. Lin, S. Hui , "Current source ballast for high power lighting emitting diodes without electrolytic capacitor," in *2008 34th Annual Conference of IEEE Industrial Electronics*, 2008.
- [55] T. Kim, J. Jeong, B. Lee, D. Shin, H. Song, B. Kim, H. Kim , "Analytical study on low-frequency ripple effect of battery charging," in *2012 IEEE Vehicle Power and Propulsion Conference*, 2012.
- [56] H. Beh, G. A. Covic, J. Boys , "Effects of pulse and DC charging on lithium iron phosphate (LiFePO<sub>4</sub>) batteries," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013.
- [57] L. Xue, Z. Shen, D. Boroyevich, P. Mattavelli, D. Diaz , "Dual Active Bridge-Based Battery Charger for Plug-in Hybrid Electric Vehicle With Charging Current Containing Low Frequency Ripple," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, p. 7299 - 7307, 2015.
- [58] "LC Selection Guide for the DC-DC Synchronous Buck Converter," ON Semiconductor, [Online]. Available: <https://www.onsemi.com/pub/Collateral/AND9135-D.PDF>.
- [59] "Synchronous rectification in high-performance power converter design," Texas Instruments, [Online]. Available: [https://www.ti.com/lit/wp/snva595a/snva595a.pdf?ts=1600897147016&ref\\_url=https%253A%252F%252Fwww.google.com%252F](https://www.ti.com/lit/wp/snva595a/snva595a.pdf?ts=1600897147016&ref_url=https%253A%252F%252Fwww.google.com%252F)
- [60] "CoolSiC™ Automotive Schottky Diode 650V G5," Infineon, [Online]. Available: [https://www.infineon.com/dgdl/Infineon-AIDW40S65C5-DS-v01\\_03-EN.pdf?fileId=5546d462675a6972016773c2f4e4568c](https://www.infineon.com/dgdl/Infineon-AIDW40S65C5-DS-v01_03-EN.pdf?fileId=5546d462675a6972016773c2f4e4568c).
- [61] "SLVP089 Synchronous Buck Converter Evaluation Module, User's Guide" Texas Instruments, [Online]. Available: [https://www.ti.com/lit/ug/slvu001a/slvu001a.pdf?ts=1600877842857&ref\\_url=https%253A%252F%252Fwww.google.com%252F](https://www.ti.com/lit/ug/slvu001a/slvu001a.pdf?ts=1600877842857&ref_url=https%253A%252F%252Fwww.google.com%252F)
- [62] E. Adib and H. Farzanehfard, "Zero-Voltage-Transition PWM Converters With Synchronous Rectifier," in *IEEE Transactions on Power Electronics*, vol. 25, no. 1, pp. 105-110, Jan. 2010.

- [63] H. Do, "Zero-Voltage-Switching Synchronous Buck Converter With a Coupled Inductor," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 8, pp. 3440-3447, Aug. 2011.
- [64] G. Maumiciale et al., "Efficiency of state-of-the-art GaN devices in a synchronous-rectifier buck converter," *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal*, 2019, pp. 1726-1731.
- [65] W. Lee, D. Han, D. Bobba and B. Sarlioglu, "Design of Single-Turn Air-Core Integrated Planar Inductor for Improved Thermal Performance of GaN HEMT-Based Synchronous Buck Converter," in *IEEE Transactions on Industry Applications*, vol. 56, no. 2, pp. 1543-1552.
- [66] "CCM PFC Boost Converter Design," Infineon Technologies, 2013. [Online]. Available: <https://www.mouser.com/pdfdocs/2-7.pdf>.
- [67] "Metallized Polypropylene Film Capacitors," VISHAY, 2020. [Online]. Available: <https://www.vishay.com/docs/28164/mkp1848dcl.pdf>.
- [68] S. Abdel-Rahman and E. Persson, "CoolGaN™ totem-pole PFC design guide and power loss modeling," [Online]. Available: [https://www.infineon.com/dgdl/Infineon-Design\\_guide\\_Gallium\\_Nitride-CoolGaN\\_totem-pole\\_PFC\\_power\\_loss\\_modeling-ApplicationNotes-v01\\_00-EN.pdf?fileId=5546d4626d82c047016d95daec4a769a](https://www.infineon.com/dgdl/Infineon-Design_guide_Gallium_Nitride-CoolGaN_totem-pole_PFC_power_loss_modeling-ApplicationNotes-v01_00-EN.pdf?fileId=5546d4626d82c047016d95daec4a769a).
- [69] "650V Enhancement Mode GaN Transistor," GaN Systems, [Online]. Available: <https://gansystems.com/gan-transistors/gs66516t/>.
- [70] "GN002 Application Note, Thermal Design for GaN Systems' Top-side cooled GaNPX®-T packaged devices," GaN Systems, 30 Oct 2018. [Online]. Available: [https://www.mouser.ca/pdfDocs/GN002\\_Thermal-Design-Guide-for-Top-Side-Cooled-GaNpx-T-Devices\\_Rev-181030.pdf](https://www.mouser.ca/pdfDocs/GN002_Thermal-Design-Guide-for-Top-Side-Cooled-GaNpx-T-Devices_Rev-181030.pdf).
- [71] "Heat Sinks," Digikey, [Online]. Available: <https://www.digikey.ca/products/en/fans-thermal-management/thermal-heat-sinks/219?k=ATS-CPX045045035&k=&pkeyword=ATS-CPX045045035&sv=0&pv625=127674&sf=0&quantity=&ColumnSort=0&page=1&pageSize=25>.
- [72] "Ohmite RA-T2X-38E," Digikey, [Online]. Available: [https://www.digikey.ca/product-detail/en/ohmite/RA-T2X-38E/RA-T2X-38E-ND/2416488?utm\\_adgroup=Thermal%20-%20Heat%20Sinks&utm\\_source=google&utm\\_medium=cpc&utm\\_campaign=Shopping\\_Product\\_Fans%2C%20Thermal%20Management\\_NEW&utm\\_term=&productid=2416488&gclid=EAI](https://www.digikey.ca/product-detail/en/ohmite/RA-T2X-38E/RA-T2X-38E-ND/2416488?utm_adgroup=Thermal%20-%20Heat%20Sinks&utm_source=google&utm_medium=cpc&utm_campaign=Shopping_Product_Fans%2C%20Thermal%20Management_NEW&utm_term=&productid=2416488&gclid=EAI).