Modeling and Improvement of DC-link Capacitor Lifetime in a Regenerative Cascaded H-bridge Motor Drive

MODELING AND IMPROVEMENT OF DC-LINK CAPACITOR LIFETIME IN A REGENERATIVE CASCADED H-BRIDGE MOTOR DRIVE

BY

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To my beloved.

Abstract

Motor drives represent electric equipment used for speed control of electric motors. Varieties of industrial applications, such as assembly, pumps, fans etc., require motors and they consume huge amount of electric energy. Compared with traditional motor drives, which can only send energy from grid to motor, a regenerative motor drive can achieve bi-directional power flow control between motors and utility grid. Regenerative motor drives are excellent candidates for reducing power loss in motor-related applications. One of the most essential parts of a regenerative motor drive power cell is dc-link capacitors. They create suitable dc-link voltages and smooth the voltage waveforms. Reliability, or lifetime of dc-link capacitors highly affect power cell lifetime, and power loss in dc-link capacitor is also another issue that worth noticing.

This thesis focuses on the lifetime modeling and lifetime improvement of dc-link capacitors in a regenerative cascaded H-bridge medium-voltage motor drive. The lifetime modeling bases itself on the mechanisms of dominant lifetime stresses in practical

operations. A proposed method is used to reduce a dominant current harmonic component in dc-link capacitors. With the proposed lifetime model and harmonic-reduction method, dc-link capacitor lifetime improvement can be anticipated in this motor drive model. Less power losses in those dc-link capacitor banks can also be achieved.

Acknowledgements

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Great thanks go to my parents and other family members, for their selfless moral support and encouragement when I was far away from home and pursued my master degree abroad.

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Chapter 1

Introduction

1.1 Motivation

Electricity, a splendid gift that presented by nature, has been in the service of human society for centuries after the second industrial revolution. Electricity can be noticed in everywhere in our daily lives. As we benefit from electricity at our pleasure but are requited with environmental issues such as global warming, questions that are worthy of consideration are raised up: Where are electric power consumed? How to reduce electric power dissipation?

Motor drives have become one kind of the top energy-consuming objects in industry, since human society came into the age of electricity. Take the United States for instance, 60~65% of electric power is used for driving ac motors [1]. [2] announced that 230 million

3-phase medium-voltage (MV) ac motors existed in USA in 2009 and they counted on 70% of electric power consumption. In the family of MV ac motors, induction motors occupy 90% of market share thanks to their simpler structures, higher reliability and cheaper pricings. Effective methods to reduce power dissipation in MV motor drives (MVMDs) for induction motors receive incessant concerns recently.

One of the most attractive solutions is regenerative capability. Power regeneration finds its place on many applications: Vertical elevators can transform kinetic energy to electric power during deceleration, replacing braking resistors with suitable power regeneration devices, surplus power can be send back to public utility gird. In an electric vehicle, braking energy during vehicle brake can be collected through drive shaft, and used for charging vehicle batteries.

Compared with non-regenerative (non-regen) MVMDs, regenerative (regen) MVMDs avail themselves with regenerative capabilities. Similar to non-regen ones, a regen MVMD has ac-dc-ac power converter. Dc-link capacitor banks maintain suitable dc-link voltages and smooth the voltage waveforms. A multilevel voltage source inverter (VSI) topology is tied with ac-side induction motor. VSI feeds motor with tunable ac voltages and control the motor speed and electromagnetic torque. The main difference between regen and non-regen MVMDs is front-side converter topology: Non-regen MVMDs utilize power diode rectifiers in the front, known as diode-front-end (DFE) rectifier, to perform

unidirectional change of input ac voltages to dc voltages. Regen MVMDs are equipped with fully-controlled switching devices (e.g. IGBTs) in active-front-end (AFE) rectifier, bidirectional power flow between grid and motor is available with proper control.

Regenerative brake is a kind of dynamic braking method that without dc-link braking resistors, it can send motor's power to the power grid, so as to reduce considerable amount of power loss. Conventional electric braking methods for non-regen MVMDs usually use dc voltage injection or reversed plugging, a reversed braking torque can be applied to induction motor, braking energy will be dissipated in rotor's internal impedance. Compared with traditional methods, much less thermal loss appears in braking progress of regen MVMDs. System energy conservation capability can be significantly improved. What's more, a regen MVMD can control induction motor in pure regeneration mode, motor can even run as a generator if needed.

Varieties of multilevel inverter topologies can be used in regen MVMDs. Four typical inverter topologies in MV industries are shown in Fig. 1.1. MVMDs require more voltage levels to reduce total harmonic distortion (THD) in output voltages, thus two-level inverter isn't qualified enough. Flying-capacitor (FC) inverter needs more clamping capacitors with different voltage ratings which is less economical. The most widely-used ones in MVMD applications are neutral point clamped (NPC) inverter and Cascaded H-bridge (CHB) inverter. NPC inverter requires less isolated dc-link capacitors in one phase, less switching

devices in series and it has good voltage THD performance. However, the number of voltage levels is restricted to avoid overuse of clamping diodes, less voltage levels means higher voltage ratings are mandatory for switching devices. And potential neutral-point voltage derivation may challenge controllers. CHB inverter distinguishes itself with excellent modularity, less switches in series, low voltage THD, simpler controllers and less troublesome issues on isolated dc-link capacitors. Even though phase-shifting transformer and more rectifier topologies are needed to create isolated dc voltages, advantages of CHB inverter makes it a good candidate for regen MVMD applications.

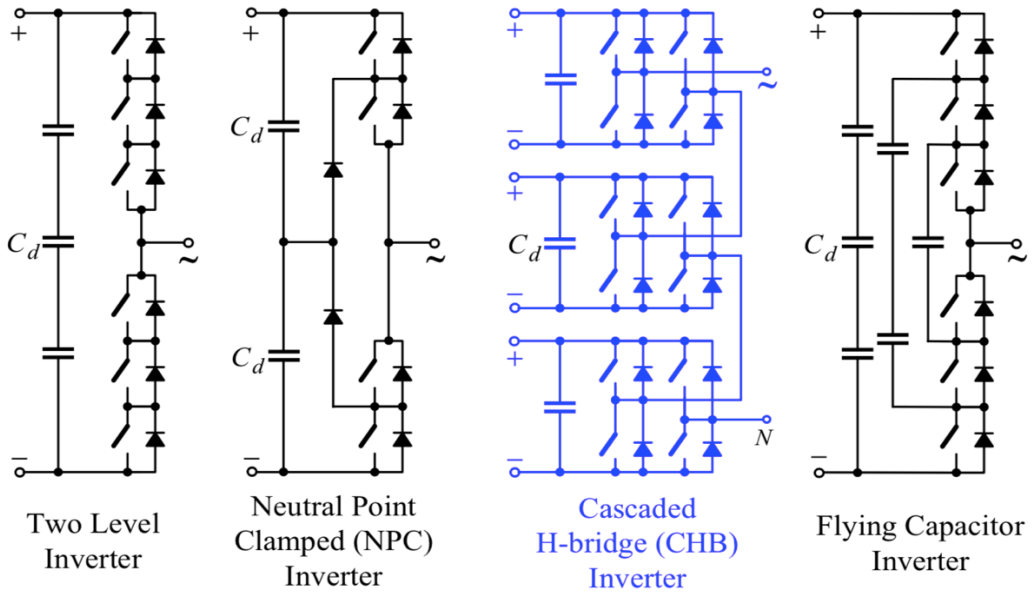


Fig. 1.1 Per phase topologies of typical multilevel inverters [3].

As a big group of passive components in regen CHB power cells, dc-link capacitors occupy significant space in power cells. Their reliabilities critically determine the lifetime of regen CHB MVMDs. A survey given by Toshiba EMC Inc. declared that most of the

drastic failures in motor drives are because of dc-link capacitors failures [4]. Failure mechanisms of dc-link capacitors can be case deformation, terminal disconnection, electrolyte loss, dielectric breakdown etc. Reliability or lifetime of a dc-link capacitor strongly depends on interactive impacts from several factors, such as ripple current, ambient temperature, applied voltage and humidity. And the power loss on dc-link capacitors' internal resistances is not to be ignored.

1.2 Contributions

This thesis concerns itself with the dc-link capacitor issues in regen CHB MVMDs. The main contributions of the presented work can be summarized as follows:

In depth study of two types of capacitors for dc-link applications: aluminum electrolytic (Al-Elec) capacitors and metallized polypropylene film (MPPF) capacitors, which are suitable candidates for regen CHB MVMD applications. Configurations and electrochemical characteristics of them are well studied. Reliability analysis of dc-link capacitors is emphasized in terms of failures classification, capacitor modeling for failure-related parameter, and research ideologies.

In order to prognosticate the reliability of dc-link capacitors, the estimated useful lifetime (EUL) models for Al-Elec capacitors and MPPF capacitors are proposed with the consideration of ripple current, ambient temperature, applied voltage and humidity. The feasibility and accuracy of proposed models are certified with manufacturers' testing data.

A pulse width modulation (PWM) carrier shifting technique (CST) is also proposed to mitigate the dominant 2nd carrier harmonic component in dc-link current. The rms current performance of dc-link capacitors is ameliorated. Simulation studies of the proposed CST verifies the effectiveness.

Four groups of dc-link capacitor banks are designed for a 3 kV regen CHB MVMD model, with different Al-Elec and MPPF capacitors products from two leading capacitor manufacturers.

Combining the proposed EUL models and the proposed CST, the lifetime analysis and power loss calculation are given for these dc-link capacitor banks. The effects of CST in EUL improvement and power loss reduction is proved.

1.3 Thesis Structure

Thesis chapters are arranged as follows:

Chapter 2 outlines non-regen and regen CHB MVMDs. Basic structure and sinusoidal PWM (SPWM) patterns for CHB inverter topology is given. Induction motor modelling and corresponding field-oriented control (FOC) technique is introduced. Simulation studies of a 3-phase, 3 kV, 140 A, 7-level CHB MVMD in non-regen model and regen model are also delivered and analyzed in details.

In chapter 3, two typical types of dc-link capacitors - Al-Elec capacitors and MPPF capacitors, which are suitable candidates for regen CHB MVMD applications, are listed.

Configurations and electrochemical characteristics of them are introduced, along with pros and cons comparisons. Ripple current, ambient temperature, applied voltage and humidity are discussed as capacitor reliability stress factors. Reliability analysis of dc-link capacitors is emphasized in terms of failures classification, capacitor modeling for failure-related parameter, and research ideologies.

Chapter 4 establishes itself on one of the research ideologies - physical-based estimation (PE method). The influences of aforementioned reliability stress factors are categorized and modelled by estimating their behavior mechanisms. Features of them are illustrated through stress factor curves. Affiliations between failure and reliability are presented with the help of reliability analysis concepts. By integrating individual stress factors into a combined stress factor, EUL models for Al-Elec capacitors and MPPF capacitors are proposed as approaches to deliver lifetime forecast, 4-D images of the models are demonstrated. Feasibility and accuracy of the proposed EUL models are verified by manufacturer lifetime diagrams of capacitor products.

In chapter 5, targeting on ripple current stress factor, a CST that can reduce the 2nd carrier harmonic on dc-link capacitor current is proposed. Mathematical modeling of dc-link capacitor current components were introduced by analyzing SPWM patterns. Optimization ideology is involved, in order to change the current harmonic reduction issue into an one-variable optimization problem. Simulation studies for dc-link capacitor bank

on 3 kV, 140 A, 7-level regen CHB MVMD model are presented. Effectiveness of the proposed CST is verified.

Chapter 6 makes use of the proposed EUL models and CST. 4 dc-link capacitor banks are designed with different types of capacitors from two manufacturers. Simulation analysis on one capacitor unit in every bank is elaborated, so as to compare the EUL performances between capacitor banks with/without proposed CST. Total power losses of capacitor banks are calculated in system level, comparisons are also given.

Chapter 7 gives an introduction of experimental prototype, which is a scaled-down setup based on a commercial CHB MVMD. Layout of the prototype, main components and control platforms of the system are demonstrated.

Chapter 8 summarizes the research objectives in this thesis, future research orientations are outlined as well.

Chapter 2

Introduction of Non-regenerative and Regenerative Cascaded H-bridge Medium Voltage Motor Drives

2.1 Introduction

Motor drives (MD) are integrated electric systems that carry through power conversion in order to achieve electric motor control. Medium voltage motor drives (MVMDs) is also known as variable speed drives (VSDs) that are designed for medium-voltage level motors which have an output voltage varying from 2.3~13.8 kV. The power ratings of them can reach up to 100 MW. Nowadays, MVMDs can find a wide application possibility in industry, especially in electric traction, oil and gas pumping, mining and minerals, marine and chemical etc. [5].

Based on the capability of bi-directional power exchanging between MV drives and grid, MV drives can be categorized into non-regenerative (non-regen) and regenerative

(regen) MVMDs. Non-regen MVMDs utilize passive-front-end, or diode-front-end (DFE) grid-side diode rectifier which can only transfer ac power to dc power. Regen MVMDs use active-front-end (AFE) grid-side converter which can realize ac/dc conversion in motoring condition and dc/ac conversion in regeneration condition.

As one of the most popular motor-side converter topologies in MVMDs, cascaded H-bridge (CHB) multilevel inverter with equal dc voltages finds a lot applications in this domain thanks to its high modularity, simple modulation and high power ratings [6]. The rectifier unit and CHB inverter unit, with a dc-link power capacitor bank in the middle, comprising the basic structure of a power cell for CHB MVMD. For the motor itself, there are varieties of electric ac motor types available on the market, among which induction motor find their predominant positions in industrial applications due to their stable structure, economical pricing and easy-to-maintain features.

In this chapter, basic structures of CHB converter topology, sinusoidal pulse width modulation (SPWM) patterns, induction motor modelling and corresponding field-oriented control (FOC) technique will be introduced for a non-regen and regen CHB MVMDs for induction motor. A 3-phase, 3 kV, 140 A, 7-level CHB MVMD which has a structure shown in Fig. 2.1 will be used for simulation illustration in this chapter.

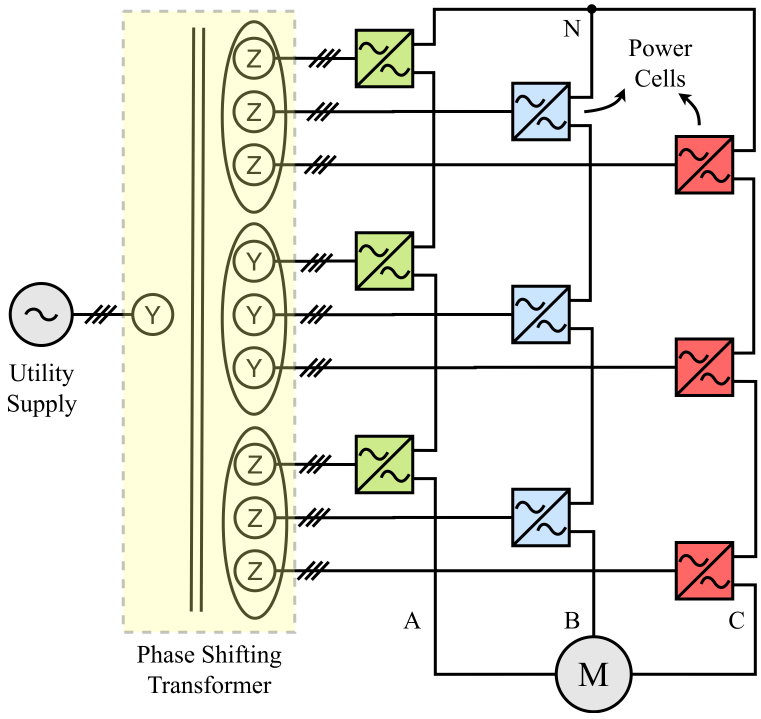


Fig. 2.1. A 3-phase 7-level CHB motor drive.

2.2 Cascaded H-Bridge Multilevel Inverter

A CHB multilevel inverter is made up with a series of single-phase H-Bridge inverters. Their ac output sides are connected in series in every leg of CHB multilevel inverter, in order to increase the number of voltage levels. The output voltage waveform can approach a sinusoidal shape. This reduce the total harmonic distortion (THD) in CHB inverter ac output side, which is the input voltage of induction motor.

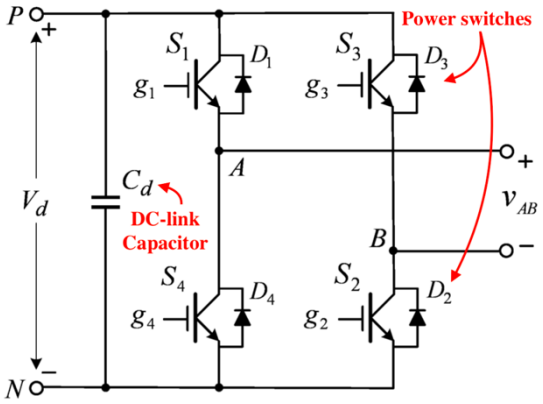


Fig. 2.2 A single-phase H-Bridge inverter [7].

Three single-phase H-Bridge inverter is connected in cascade in this topology in each CHB inverter leg. A single-phase H-Bridge inverter requires an isolated dc power supply which can be fed from the phase-shifting transformer's secondary windings followed up by a 3-phase rectifier. Phase-shifting transformer can also reduce the secondary line voltage harmonics by introducing phase voltage angle displacement in every phase of it, and create excellent electric isolation [8].

2.2.1 Single-Phase H-Bridge Inverter

Basic structure of a single-phase H-Bridge inverter is given in Fig. 2.2. A fully-controlled power semiconductors (e.g. IGBTs) locates on every half leg of the H-Bridge inverter. The two IGBTs in the same leg cannot be conducted at the same time, that is to avoid short circuit of dc-link power capacitor. An opposite logic on the IGBT gating signals given by Eq. (2.1) and Eq. (2.2) can be applied.

$$v_{g1} = \overline{v_{g4}} \tag{2.1}$$

$$v_{g3} = \overline{v_{g2}} \tag{2.2}$$

where v_{g1}, v_{g2}, v_{g3}, v_{g4} are gating signals for corresponding S_1, S_2, S_3, S_4 IGBTs.

IGBTs that have cater corner locations should be turned on simultaneously, in order to build full path for the voltage, so by analyzing the conducting states of IGBTs, the H-Bridge inverter output voltage shows 3 levels: $+V_d$, 0, $-V_d$, a staircase-shape voltage waveform can be expected.

Fig. 2.3 shows the SPWM pattern for a single-phase H-Bridge inverter. SPWM is a modulation technique that uses a fundamental-frequency (60 Hz) reference sinusoidal wave v_m to represent the desired voltage shape on the ac output side. Triangular carriers v_{cr} with higher frequency are introduced for making comparison with sinusoidal wave and create chopped waves.

The IGBT gating signals' operating sequences and duration follow these chopped staircase waves. Two carriers are needed for one inverter, each of them controls two IGBTs in one inverter leg. Finally, the ac output side of a single-phase H-Bridge inverter shows a 3-level staircase waveform that approaches the rms value of desired sinusoidal waveform.

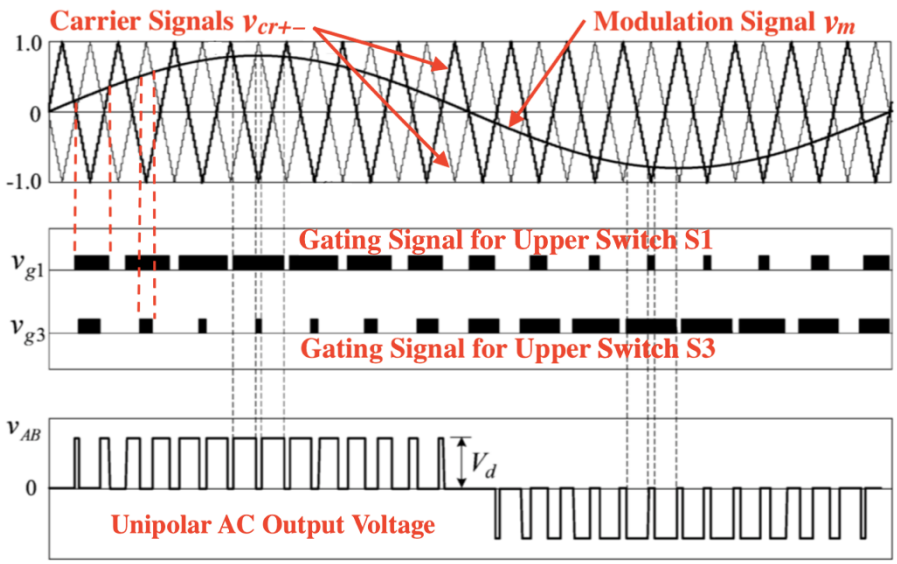


Fig. 2.3 SPWM pattern for a single-phase H-Bridge inverter [7].

2.2.2 H-Bridge Cascaded Structure

One phase leg of a 7-level CHB inverter in CHB MVMD is shown in Fig. 2.4. Three H-Bridge inverter show a cascaded structure. Phase voltage of the CHB inverter leg is:

$$v_{AN} = v_{H1} + v_{H2} + v_{H3} \tag{2.3}$$

where v_{H1}, v_{H2}, v_{H3} are output voltages of sequenced H-Bridge inverters,

Generally, any multilevel inverter with m voltage levels on its phase leg requires $m-1$ carriers in its PWM patterns. Therefore, for a 7-level CHB inverter, 6 carriers are needed. Each of the carriers has a shifted phase angle between its adjacent carrier φ_{cr}, which can be given as:

$$\varphi_{cr} = \frac{360°}{m-1} \tag{2.4}$$

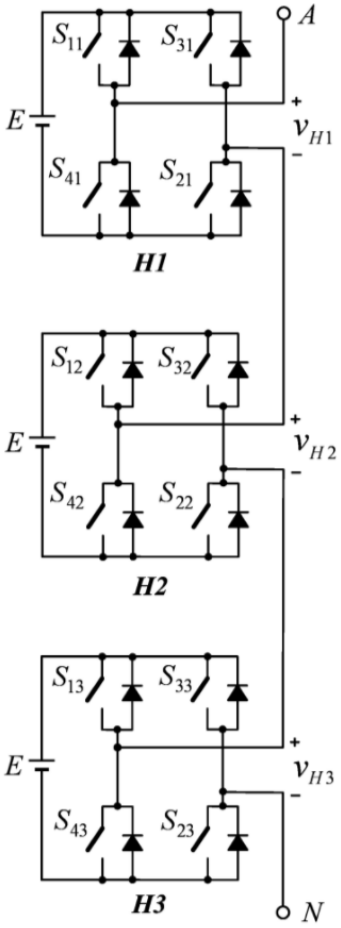


Fig. 2.4 A phase leg of 7-level CHB inverter [7]: 3 single-phase H-bridge inverter are cascaded in series.

Even distribution of carriers in one modulation period can enhance the symmetry of integrated phase voltage, avoiding simultaneous turn-on/off of IGBTs in different H-Bridge inverters. This helps mitigating the voltage waveform distortion and reducing the voltage THD. Smaller dv/dt reduces the surge voltage that applied to induction motor's rotor winding, the electromagnetic inference (EMI) characteristic can be improved as well.

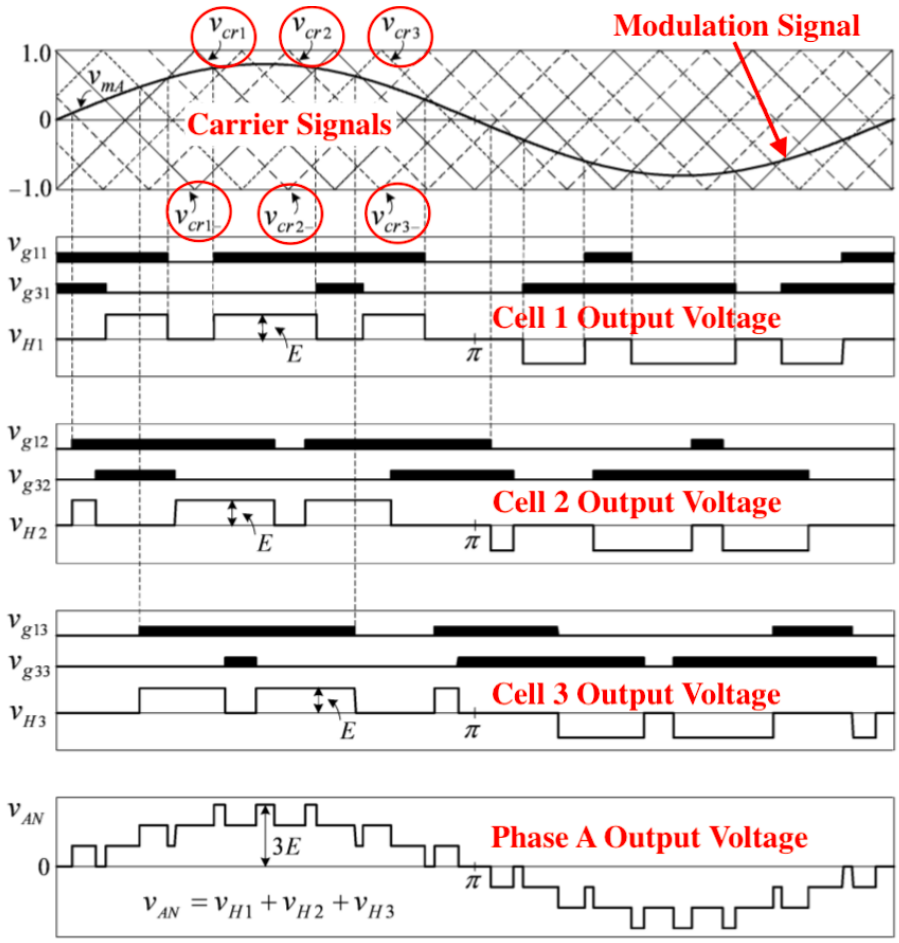


Fig. 2.5 SPWM pattern of a phase leg of 7-level CHB inverter [7].

Based on Eq. (2.4), 60° shifted phase angle between any two adjacent carriers can be applied for 7-level CHB inverter. Fig. 2.5 shows the phase-shifted SPWM patterns of phase A of 7-level CHB inverter, in terms of cells output voltages and inverter phase voltage.

v_{cr1}, v_{cr2}, v_{cr3} are carriers that specified for upper IGBTs in left legs, S_{31}, S_{32}, S_{33} respectively. v_{cr1-}, v_{cr2-}, v_{cr3-} are carriers that specified for upper IGBTs in right legs, S_{11}, S_{12}, S_{13}. Remaining lower IGBTs behave opposite conducting logics regarding to their upper ones in the same leg. It is apparent that any output phase voltage of CHB

inverter (v_{AN} in the case of Fig. 2.4) shows the following 7 levels of voltage steps: $+3E, +2E, +E$ 0, $-3E, -2E, -E$. Output line voltage of a 7-level CHB inverter has 13 voltage levels.

2.2.3 Non-Regen CHB MVMD Power Cell

As illustrated in Fig. 2.1, power cells are fundamental components of the converter topology in a CHB MVMD. A power cell can be seen as the combination of rectifier unit, dc-link power capacitor and inverter unit.

Simplified circuit of a non-regen CHB can be given as Fig. 2.6. Typically, it is consisted of a 3-phase 6-pulse DFE rectifier, a dc-link power capacitor and a 3-phase H-Bridge inverter.

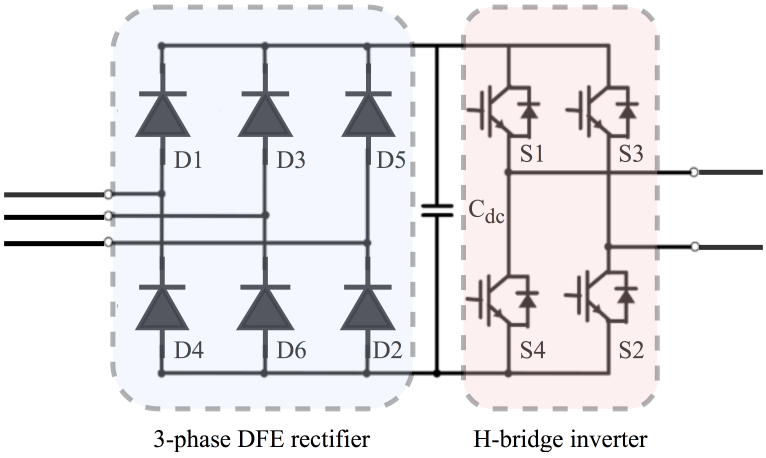


Fig. 2.6 A non-regen CHB power cell.

Due to the one-directional conducting ability of power diode, conduction of these uncontrolled power devices dependently rely on the applied voltage upon two terminals.

Fig. 2.7 shows the conducting states of 3-phase DFE rectifier in a non-regen CHB power cell. 3-phase line voltages waveform can be used for illustration, in section I, v_{AB} has higher value compared with other line voltages, power diodes D_1 and D_6 are taking forward-biased voltages and can be turned on. Other diodes receive backward-biased voltages and keep on closed. In section II, v_{AC} is the biggest one and the voltage path is built by turning on diodes D_1 and D_6. The rest conducting patterns can be determined in the same way. A dc voltage can be produced as a result.

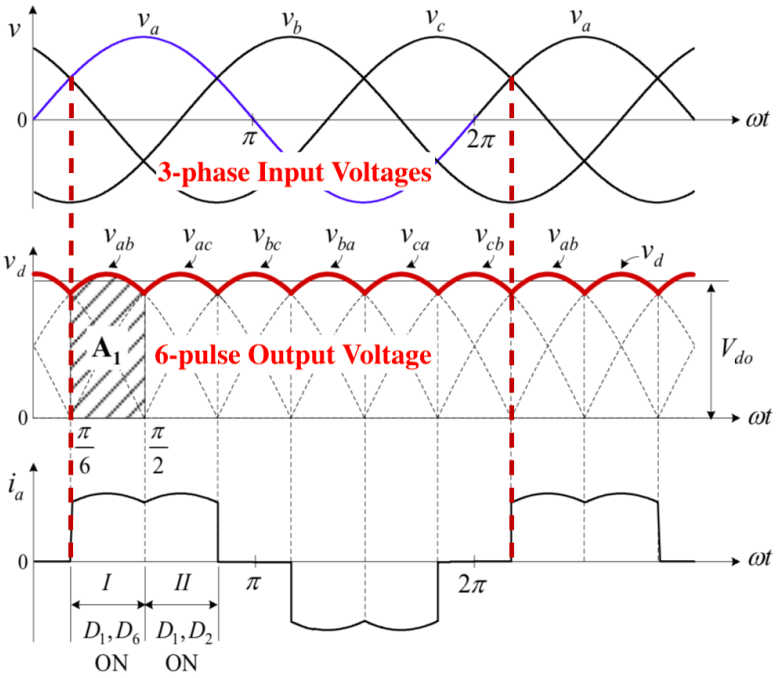


Fig. 2.7 Conducting states of 3-phase 6-pulse DFE rectifier [9].

Dc-link power capacitor C_{dc} is used for isolating the ac side and dc-side, storing the converted energy from rectifier, creating a suitable dc-bus voltage for inverter, and smooth the dc-link voltage waveforms. Dc voltage control can find its place in practical

implementation, that is to avoid abnormal dc inrush voltage. If the instantaneous reaches to the safety threshold, a dc chopper will operate and bypass the dc power capacitor, all the energy injected to the cell will be dissipated in braking resistor. Generally, in order to reduce rush dv/dt that may appear in operation, dc-link power capacitors need to be pre-charged before the running of entire converter, an extra auxiliary ac/dc charging circuit is needed.

For the inverter-side of a non-regen CHB power cell, the operating concepts of it is identical to a single-phase H-Bridge inverter and has the same topology. Three non-regen CHB power cells are connected in cascade in inverter-side, to create a non-regen 7-level CHB MVMD inverter phase.

2.2.4 Regen CHB MVMD Power Cell

Configuration of a normal 6-switch/4-switch regenerative power cell is shown in Fig. 2.8. Compared with non-regen CHB power cell, the rectifier-side of it is replaced by a 3-phase AFE inverter. Thanks to the bi-directional conducting characteristics of IGBTs, ac/dc/ac conversion can be done from grid to motor in motoring condition, from motor to grid in regeneration condition.

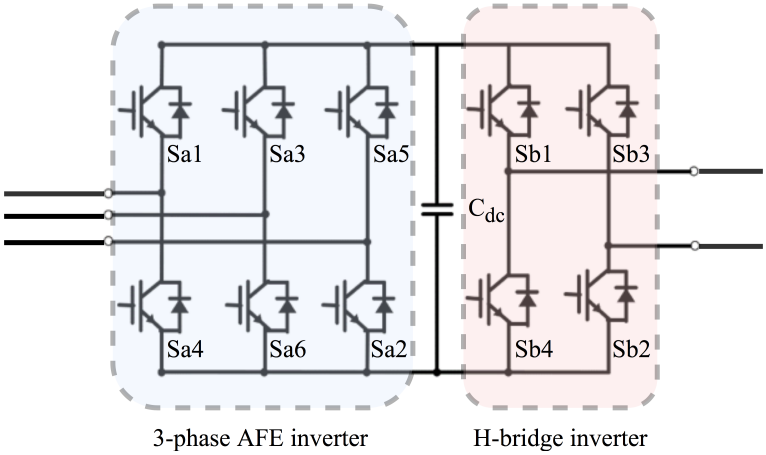


Fig. 2.8 A regen CHB power cell.

The operation of 3-phase AFE inverter can be categorized into two modes: conventional DFE operation, PWM AFE operation. For conventional DFE operation, by keeping low-levels for the gating signals for S_{a1}, S_{a2}, S_{a3}, S_{a4}, S_{a5}, S_{a6} IGBTs, those IGBTs are turned off in operating duration. Diodes that parallel-connected with IGBTs can operate as normal power diodes in a 3-phase DFE rectifier.

In PWM AFE operation mode, an outer closed-loop control for actual dc voltage can produce a desired active power reference for the system. With a demanded reactive power, *dq*-axis current controllers can be added. Considering the voltage distributed to impedance of line filter, *dq*-axis reference voltages can be obtained, the phase angle of grid-side voltage is captured by phase-locked loop (PLL) and is used for creating unit reference sinusoidal signal. Then a carrier-based SPWM modulation pattern can be introduced for generating gating signals for IGBTs in 3-phase AFE inverter.

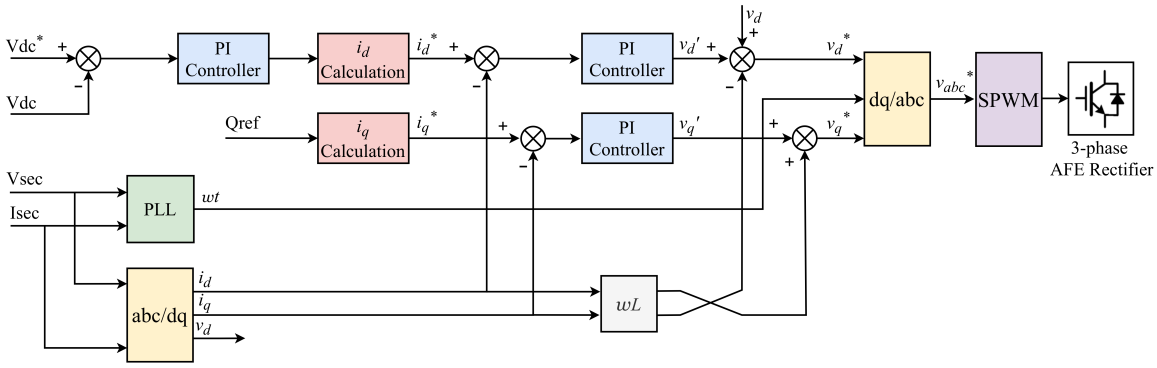


Fig. 2.9 3-phase AFE rectifier controller.

Fig. 2.9 shows a typical 3-phase AFE rectifier controller. The phase difference between grid-side voltages and currents can be fully controlled. In motoring condition, if they are aligned with 0° phase shifted, a power factor of 1.0 can be expected, which takes full advantages of power utility efficiency in power conversion. In regeneration condition, by tuning the phase shifting angle to adjust the actual power distribution, the power injected back into grid can be controlled. If the voltages and currents are aligned with 180° phase shifted, a power factor of "−1.0" can be expected for full regeneration.

Similar to a non-regen CHB MVMD, three regen CHB power cells are connected in cascade in inverter-side, to create a full phase of regen CHB MVMD converter.

2.3 Modeling and Control of Induction Motors

These section will cover the modelling of induction motor and corresponding FOC technique for induction motor control.

2.3.1 Coordinates Transformation

Generally, control strategy of a dc motor is much more simple than a 3-phase ac motor. The expression of electromagnetic torque T_e for a dc motor can be easily given as:

$$T_e = K_a \psi_f i_a \tag{2.7}$$

in which K_a is armature constant, ψ_f is the generated flux and i_a is the armature current. ψ_f and i_a can be decoupled in control point of view.

As a 3-phase electric motor, induction motor can be modelled by using 3-phase circuit theory to show its sophisticated highly-coupled fluxes and torque, then a 3-phase stationary frame can be transformed into a 2-phase orthogonal rotational frame. This helps to decouple the complex interaction in an induction motor. Finally, a simpler control theory that similar to dc motor control can be applied for induction motor.

The basic idea of coordinates transformations is two simplify the variables analysis of induction motor. Generally, two transformation are involved: the Clarke transformation and the Park transformation.

A. Clarke Transformation

Clarke transformation converts a 3-phase stationary (3s) frame to a 2-phase stationary (2s) frame, it is also named as 3s/2s transformation. The basic concept of 3s/2s transformation can be illustrated in Fig. 2.10.

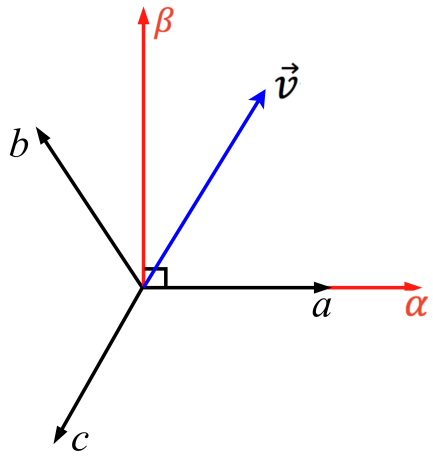


Fig. 2.10 Clarke (3s/2s) transformation.

For a space vector $\vec{v}$, it can be formed in either 3s frame or 2s frame with a corresponding transforming matrix:

$$\begin{bmatrix} \overrightarrow{v_\alpha} \\ \overrightarrow{v_\beta} \end{bmatrix} = K \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} \overrightarrow{v_a} \\ \overrightarrow{v_b} \\ \overrightarrow{v_c} \end{bmatrix} \tag{2.8}$$

where $\overrightarrow{v_\alpha}$, $\overrightarrow{v_\beta}$ are vectors of $\vec{v}$ on 2s frame, $\overrightarrow{v_a}$, $\overrightarrow{v_b}$, $\overrightarrow{v_c}$ are vectors of $\vec{v}$ on 3s frame.

Considering $\overrightarrow{v_\alpha}$ as an example, the following equations can be applied:

$$\overrightarrow{v_\alpha} = V_{2s}\cos(wt) = K\overrightarrow{v_a} - \frac{1}{2}\overrightarrow{v_b} - \frac{1}{2}\overrightarrow{v_c} \tag{2.9}$$

$$\overrightarrow{v_a} = V_{3s}\cos(wt), \overrightarrow{v_b} = V_{3s}\cos\left(wt - \frac{2}{3}\pi\right), \overrightarrow{v_c} = V_{3s}\cos\left(wt - \frac{4}{3}\pi\right) \tag{2.10}$$

where V_{2s}, V_{3s} are amplitude of $\vec{v}$ in 2s frame and 3s frame respectively.

Taking Eq. (2.10) into Eq. (2.9), it is clear that:

$$\overrightarrow{v_\alpha} = V_{2s}\cos(wt) = \frac{3}{2}KV_{3s}\cos(wt) \tag{2.11}$$

In order to have a constant amplitude transformation, $K = 2/3$ is given. The complete 3s/2s transformation is:

$$\begin{bmatrix} \overrightarrow{v_\alpha} \\ \overrightarrow{v_\beta} \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} \overrightarrow{v_a} \\ \overrightarrow{v_b} \\ \overrightarrow{v_c} \end{bmatrix} \tag{2.12}$$

B. Park Transformation

Park transformation converts a 2s frame to a 2-phase rotational (2r) frame, it is also named as 2s/2r transformation. The basic concept of 2s/2r transformation can be illustrated in Fig. 2.11.

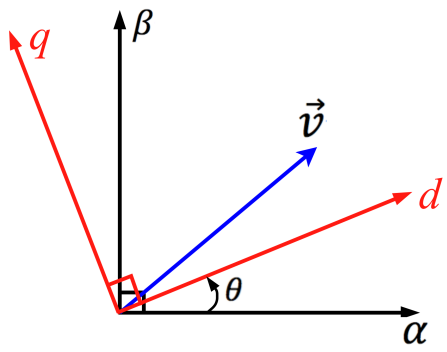


Fig. 2.11 Park (2s/2r) transformation.

The expression of 2s/2r transformation is given as:

$$\begin{bmatrix} \overrightarrow{v_d} \\ \overrightarrow{v_q} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} \overrightarrow{v_\alpha} \\ \overrightarrow{v_\beta} \end{bmatrix} \tag{2.13}$$

where θ is angular displacement between 2s frame and 2r frame.

C. 3s/2r Transformation

The concept of 3s/2s transformation is shown in Fig. 2.12. Note that after the transformation, the 2r frame (*dq*-axis rotational frame) can be seen as the synchronous frame of the induction motor which rotates with a synchronous electrical angular speed ω_s (rad/s). $\vec{v}$ can be seen as either currents, voltages or fluxes. Building the decoupled model for induction motor in *dq*-axis will be the leading idea for motor control in this thesis.

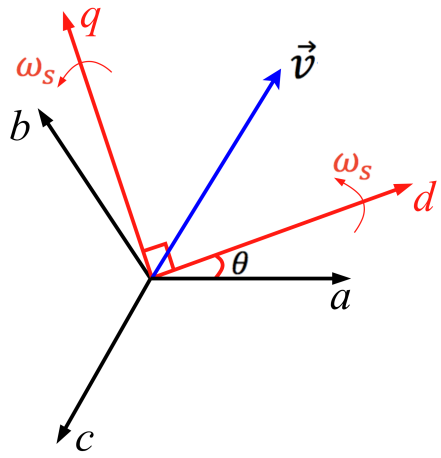


Fig. 2.12 3s/2r transformation.

Combining Eq. (2.12) and Eq. (2.13), 3s/2r transformation can be expressed as:

$$\begin{bmatrix} \overrightarrow{v_d} \\ \overrightarrow{v_q} \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2}{3}\pi\right) & \cos\left(\theta - \frac{4}{3}\pi\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2}{3}\pi\right) & -\sin\left(\theta - \frac{4}{3}\pi\right) \end{bmatrix} \cdot \begin{bmatrix} \overrightarrow{v_a} \\ \overrightarrow{v_b} \\ \overrightarrow{v_c} \end{bmatrix} \tag{2.14}$$

2.3.2 *dq*-Axis Modeling for Induction Motor

The induction motor circuit is shown in Fig. 2.13.

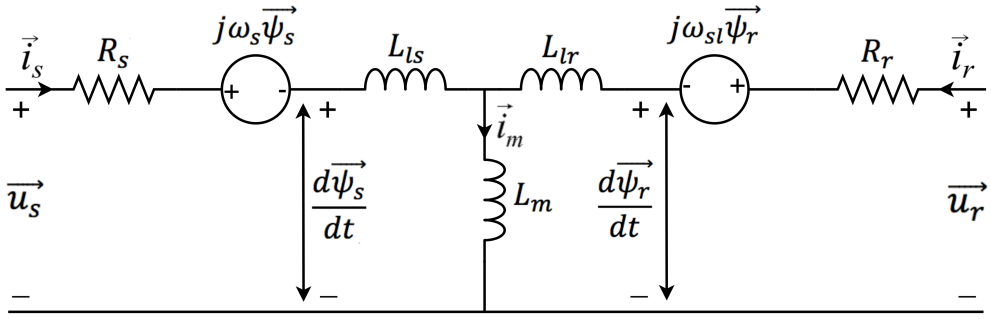


Fig. 2.13 Induction motor circuit.

Some equations for induction motor [10] can be obtained from the circuit. The voltage equation can be given as:

$$\overrightarrow{u_s} = R_s\overrightarrow{\imath_s} + \frac{d\overrightarrow{\psi_s}}{dt} + j\omega_s\overrightarrow{\psi_s} \tag{2.15}$$

$$\overrightarrow{u_r} = R_r\overrightarrow{\imath_r} + \frac{d\overrightarrow{\psi_r}}{dt} + j\omega_{sl}\overrightarrow{\psi_r} \tag{2.16}$$

where $\overrightarrow{u_s}$, $\overrightarrow{u_r}$ are voltage vectors for induction motor's stator and rotor, respectively. $\overrightarrow{\imath_s}$, $\overrightarrow{\imath_r}$ are stator and rotor current vectors. $\overrightarrow{\psi_s}$, $\overrightarrow{\psi_r}$ are stator and rotor flux vectors. $\omega_{sl} = \omega_s - \omega_r$ is the angular slip frequency, where $\omega_r = p \cdot \omega_m$ is rotor electrical angular speed, and ω_m is the mechanical angular speed, p is the number of pole pairs.

The flux equations are expressed as:

$$\overrightarrow{\psi_s} = L_{ls}\overrightarrow{\imath_s} + L_m(\overrightarrow{\imath_s} + \overrightarrow{\imath_r}) = L_s\overrightarrow{\imath_s} + L_m\overrightarrow{\imath_r} \tag{2.17}$$

$$\overrightarrow{\psi_r} = L_{ls}\overrightarrow{\imath_r} + L_m(\overrightarrow{\imath_s} + \overrightarrow{\imath_r}) = L_r\overrightarrow{\imath_r} + L_m\overrightarrow{\imath_s} \tag{2.18}$$

where $L_s = L_{ls} + L_m$ is stator self-inductance, $L_r = L_{lr} + L_m$ is rotor self-inductance. L_{ls}, L_{lr} represent the leakage inductances of stator and rotor. L_m is the mutual inductance.

The motion equations are expressed as:

$$\frac{J}{p}\frac{d\omega_r}{dt} = T_e - T_L \tag{2.19}$$

$$T_e = \frac{3p}{2}\mathrm{Re}\left(j\overrightarrow{\psi_s}\overrightarrow{i_s^*}\right) = -\frac{3p}{2}\mathrm{Re}\left(j\overrightarrow{\psi_r}\overrightarrow{i_r^*}\right) \tag{2.20}$$

where J is the inertia of rotor and motor load, T_e is electromagnetic torque, T_L is load torque.

Taking advantages of *dq*-axis modeling idea and decoupling of these vectors, the following equations can be obtained:

$$\overrightarrow{u_s} = u_{ds} + ju_{qs} \qquad \overrightarrow{i_s} = i_{ds} + ji_{qs} \qquad \overrightarrow{\psi_s} = \psi_{ds} + j\psi_{qs} \tag{2.21}$$

$$\overrightarrow{u_r} = u_{dr} + ju_{qr} \qquad \overrightarrow{i_r} = i_{dr} + ji_{qr} \qquad \overrightarrow{\psi_r} = \psi_{dr} + j\psi_{qr} \tag{2.22}$$

Substituting Eq. (2.15-2.20) with Eq. (2.21, 2.22), the *dq*-axis modeling of an induction motor can be expressed as follows. The voltage equations are given as:

$$\begin{aligned} u_{ds} &= R_s i_{ds} + \frac{d\psi_{ds}}{dt} - \omega_s \psi_{qs} \\ u_{qs} &= R_s i_{qs} + \frac{d\psi_{qs}}{dt} + \omega_s \psi_{ds} \\ u_{dr} &= R_r i_{dr} + \frac{d\psi_{dr}}{dt} - \omega_{sl} \psi_{dr} \\ u_{qr} &= R_r i_{qr} + \frac{d\psi_{qr}}{dt} + \omega_{sl} \psi_{dr} \end{aligned} \tag{2.23}$$

Flux equations can be expressed as:

$$\begin{aligned} \psi_{ds} &= L_{ls} i_{ds} + L_m (i_{ds} + i_{dr}) \\ \psi_{qs} &= L_{ls} i_{qs} + L_m (i_{qs} + i_{qr}) \\ \psi_{dr} &= L_{lr} i_{dr} + L_m (i_{ds} + i_{dr}) \\ \psi_{qr} &= L_{lr} i_{qr} + L_m (i_{qs} + i_{qr}) \end{aligned} \tag{2.24}$$

Electromagnetic torque equation can be given as:

$$T_e = \begin{cases} \frac{3}{2}p\left(i_{qs}\psi_{ds} - i_{ds}\psi_{qs}\right) \\ \frac{3pL_m}{2}\left(i_{qs}i_{dr} - i_{ds}i_{qr}\right) \\ \frac{3pL_m}{2L_r}\left(i_{qs}\psi_{dr} - i_{ds}\psi_{qr}\right) \end{cases} \tag{2.25}$$

2.3.3 Field-Oriented Control Theory

As shown in Eq. (2.7), a decoupled characteristic of stator magnetic field and rotor electromagnetic torque can be found in dc motor control. Magnetic field produced by field current component can create the stator flux, rotor torque can be generated by rotor (armature) current.

Field-oriented control (FOC) takes advantages of dc motor control. By setting a field orientation for either stator flux, airgap flux or rotor flux, the flux-generating and torque-generating current components can be separated and controlled independently for induction motor.

Usually, rotor flux field orientation is widely applied in practice, its concept is shown in Fig. 2.14.

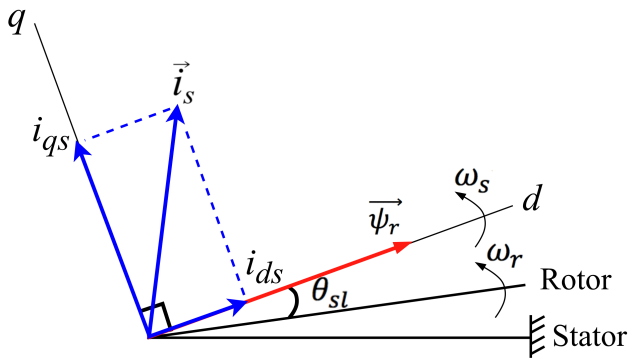


Fig. 2.14 Rotor flux orientation.

Rotor flux $\overrightarrow{\psi_r}$ is aligned with *d*-axis, thus considering

$$j\psi_{qr} = 0 \qquad \psi_{dr} = \psi_r \tag{2.26}$$

The last expression of T_e in Eq. (2.25) can be rearranged as:

$$T_e = \frac{3pL_m}{2L_r}\psi_r i_{qs} \tag{2.27}$$

Because the perpendicular relationship between stator flux-generating current i_{ds} and torque-generating current i_{ds}. Electromagnetic torque T_e is solely controlled by i_{qs} in Eq. (2.27) if i_{ds} can be well-controlled to produce a constant rotor flux ψ_r. The idea of dc motor decoupled control can be realized in an induction motor. This is the ultimate goal of FOC.

The rotor flux electrical angular speed ω_s and corresponding rotor flux angle θ_s can be expressed as:

$$\theta_s = \int \omega_s \, dt = \int (\omega_r + \omega_{sl}) dt = \theta_r + \theta_{sl} \tag{2.28}$$

where θ_r, θ_{sl} are rotor position electrical angle and slip electrical angle respectively.

2.3.4 Indirect FOC for Induction Motor

FOC can be categorized into direct FOC and indirect FOC depending on how θ_s is obtained. Indirect FOC determines θ_s with measured θ_r and calculated θ_{sl}, as shown in Eq. (2.28), which skips the motor-side sensory devices in direct FOC. The block diagram of indirect FOC is shown in Fig. 2.15. Some calculation blocks will be discussed in detail in this subsection.

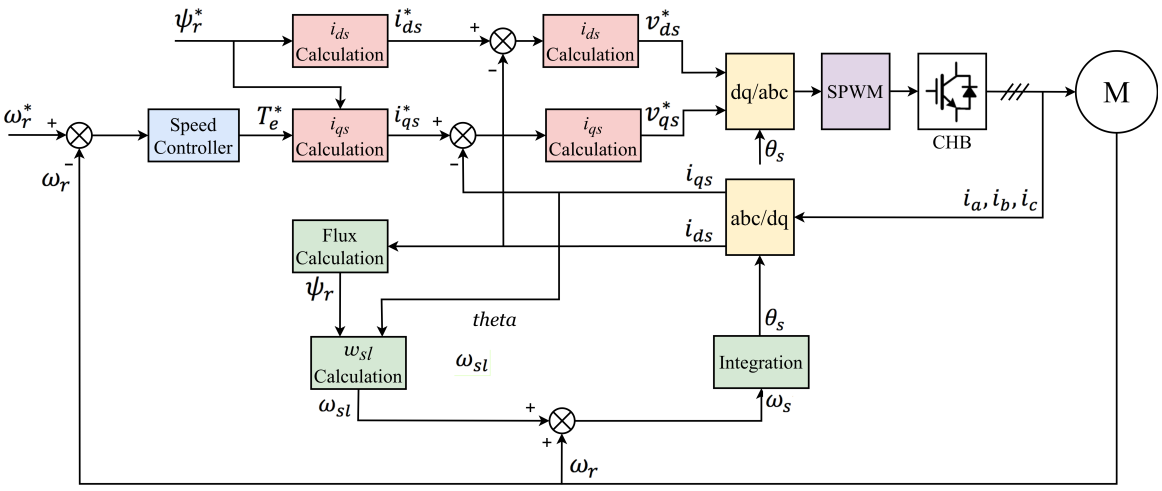


Fig. 2.15 Indirect FOC for rotor flux orientation.

A. ω_{sl} Calculation

Considering Eq. (2.16) with a short-circuit connection of rotor winding ($\overrightarrow{u_r} = 0$)

$$j\omega_{sl}\overrightarrow{\psi_r} = -R_r\overrightarrow{\imath_r} - \frac{d\overrightarrow{\psi_r}}{dt} \tag{2.29}$$

According to Eq. (2.18), Eq. (2.29) can be transformed into

$$j\omega_{sl}\overrightarrow{\psi_r} = -R_r\frac{\overrightarrow{\psi_r} - L_m\overrightarrow{\imath_s}}{L_r} - \frac{d\overrightarrow{\psi_r}}{dt} \tag{2.30}$$

Defining a rotor time constant $\tau_r = L_r/R_r$:

$$\begin{aligned} j\omega_{sl}\overrightarrow{\psi_r} &= \frac{\left(L_m\overrightarrow{i_s} - \overrightarrow{\psi_r}\right)}{\tau_r} - \frac{d\overrightarrow{\psi_r}}{dt} \\ \tau_r\frac{d\overrightarrow{\psi_r}}{dt} &= \left(L_m\overrightarrow{i_s} - \overrightarrow{\psi_r}\right) - j\tau_r\omega_{sl}\overrightarrow{\psi_r} \\ \overrightarrow{\psi_r}\left[1 + \tau_r\left(\frac{d}{dt} + j\omega_{sl}\right)\right] &= L_m\overrightarrow{i_s} \end{aligned} \tag{2.31}$$

Introducing Eq. (2.26) for rotor flux orientation on *dq*-axis:

$$\psi_r\left(1 + \frac{d}{dt}\tau_r\right) + j\tau_r\psi_r\omega_{sl} = L_m i_{ds} + jL_m i_{qs} \tag{2.32}$$

Then basing on the corresponding relations of *dq*-axis components, it can be given that:

$$\psi_r\left(1 + \frac{d}{dt}\tau_r\right) = L_m i_{ds} \tag{2.33}$$

$$\tau_r\psi_r\omega_{sl} = L_m i_{qs} \tag{2.34}$$

Ultimately the ω_{sl} calculation part is expressed as:

$$\omega_{sl} = \frac{L_m}{\tau_r\psi_r} i_{qs} \tag{2.35}$$

B. Flux Calculation

Actual rotor flux ψ_r is calculated from Eq. (2.33):

$$\psi_r = \frac{L_m}{\left(1 + \frac{d}{dt}\tau_r\right)} i_{ds} = \frac{L_m}{1 + \tau_r \cdot s} i_{ds} \tag{2.36}$$

where s is the derivative operator.

C. i_{ds} Calculation

For i_{ds} calculation, Eq. (2.37) can be derived from Eq. (2.33) as well:

$$i_{ds} = \frac{\left(1 + \frac{d}{dt}\tau_r\right)}{L_m}\psi_r \tag{2.37}$$

Usually ψ_r is kept constant as the rated value ψ_r^*, a simpler form of i_{ds} calculation is derived as:

$$i_{ds}^* = \frac{1}{L_m}\psi_r^* \tag{2.38}$$

where i_{ds}^* is a desired constant value of flux-generating current i_{ds} in control scheme.

D. i_{qs} Calculation

Expression of i_{qs} calculation is directly reformed by Eq. (2.27):

$$i_{qs}^* = \frac{2L_r}{3pL_m\psi_r^*}T_e^* \tag{2.39}$$

in which T_e^* is the desired electromagnetic torque which depends on the desired rotor speed, i_{qs}^* is the desired value of torque-generating current i_{qs} in control scheme. i_{qs}^* is proportional to T_e^*.

2.4 Simulation Studies of a CHB MVMD

In this thesis, for simulation studies of a 3 kV, 140 A, 7-level CHB MVMD for both regen and non-regen condition. A phase-shifting transformer and a squirrel-cage induction motor are selected. Table 2.1 shows the general ratings of these two devices.

TABLE 2.1. RATINGS FOR PHASE-SHIFTING TRANSFORMER AND INDUCTION MOTOR

Phase-shifting Transformer	
Rated Power	0.7 MW
Line-to-line Primary Voltage (V_{pri})	3000 V (rms)
Line-to-line Secondary Voltage (V_{sec})	650 V (rms)

Squirrel-cage Induction Motor	
Nominal Power (P_n)	0.7 MW
Nominal Voltage V_n (Vrms)	3000 V (rms)
Nominal Current I_n (Arms)	160 V (rms)

Parameter of induction motor's stator and rotor is given in Table. 2.1. Base value calculations for per unit (p.u.) system in induction motor simulation configuration and control scheme are listed here:

$$f_{mb} = 60 \text{ Hz} \text{ (motor base frequency)}$$

$$\omega_{mbe} = 2\pi f_{mb} = 120\pi \text{ rad/s} \text{ (motor base electrical frequency)}$$

$$\omega_{mbm} = \frac{\omega_{mbe}}{p} = 125.66 \text{ rad/s} \text{ (motor base mechanical speed)}$$

$$T_{mb} = \frac{P_n}{\omega_{mb}/p} = 618.94 \text{ N·m} \text{ (motor base torque)}$$

$$V_{mb} = \frac{V_n}{\sqrt{3}} = 1732.05 \text{ V} \text{ (motor base voltage)}$$

$$I_{mb} = I_n = 160 \text{ A} \text{ (motor base current)}$$

$$Z_{mb} = \frac{V_{mb}}{I_{mb}} = 10.83 \ \Omega \text{ (motor base impedance)}$$

$$L_{mb} = \frac{Z_{mb}}{\omega_{mb}} = 28.72 \text{ mH} \text{ (motor base inductance)}$$

$$C_{mb} = \frac{1}{Z_{mb} \cdot \omega_{mb}} = 0.245 \text{ mF} \text{ (motor base capacitance)}$$

TABLE 2.2. SIMULATION PARAMETER CONFIGURATION FOR INDUCTION MOTOR

Induction Motor Parameters	
Stator Resistance (p.u.)	0.0067
Stator Leakage Inductance (p.u.)	0.1358
Rotor Resistance (p.u.)	0.0109
Rotor Leakage Inductance (p.u.)	0.1358
Mutual Inductance (p.u.)	6.038
Inertia ($k_g m^2$)	9.783
Number of Pole Pairs	3

2.4.1 Simulation Results of a 3 kV Non-Regen CHB MVMD

For non-regen CHB MVMD, simulation results in respect to voltage and current performance of 7-level CHB inverter, dc-link capacitor and phase-shifting transformer, as well as the speed and torque performance of induction motor are shown in the following figures.

A. 7-Level CHB Inverter and DC-link Capacitors

Fig. 2.16 shows the steady states of output line-to-line voltage V_{AB} and phase A output current I_A of non-regen CHB inverter. V_{AB} shows 13 voltage levels to approach a sinusoidal waveform. Every voltage level has a magnitude of dc-link voltage V_{dc}, the peak value of V_{AB} is around 5000 V. I_A shows a sinusoidal shape with a 200 A peak value.

Fig. 2.17 shows three dc-link capacitor voltages in three non-regen CHB power cells in phase A. Dc voltages are generated with the help of 6-pulse diode rectifier and are kept around 850 V.

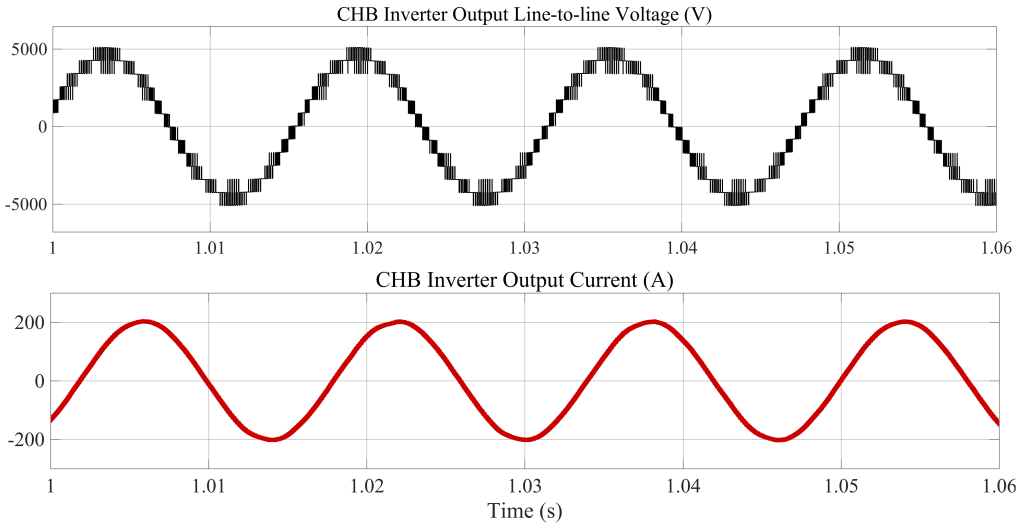


Fig. 2.16 Non-regen CHB inverter output line-to-line voltage and output current.

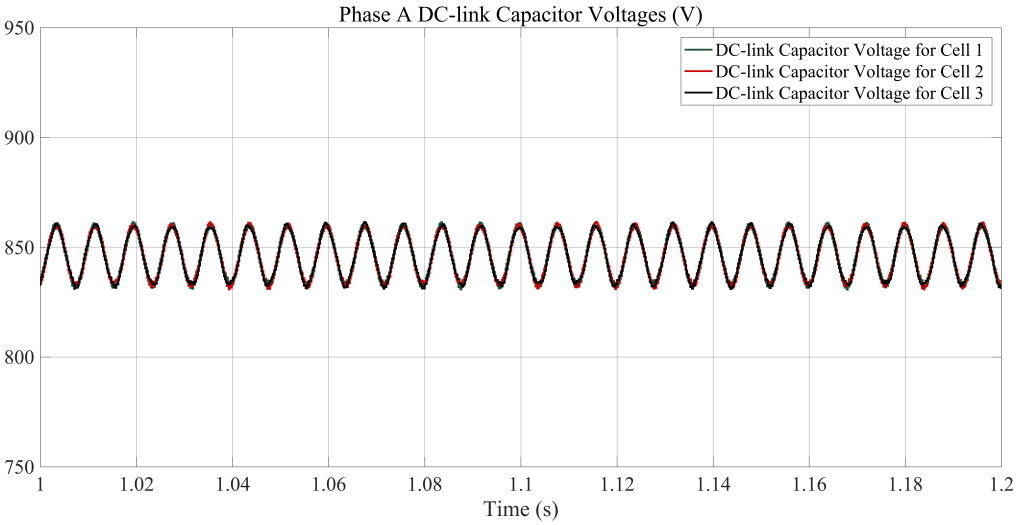


Fig. 2.17 Dc-link capacitor voltages for three non-regen CHB power cells in phase A.

B. Phase-shifting Transformer

Fig. 2.18 presents the primary-side phase voltage and phase current of the phase-shifting transformer in non-regen condition, which are also the waveforms for power grid. Phase current is magnified for 5 times for better illustration.

It can be observed that the variation of voltage leads the variation of current, and a power factor < 1 can be given. This is because the primary-side line impedances of phase-shifting transformer show inductiveness. Since the conduction of power diodes is beyond control, no reactive power control can be added for diode rectifier to manipulate the primary-side power factor.

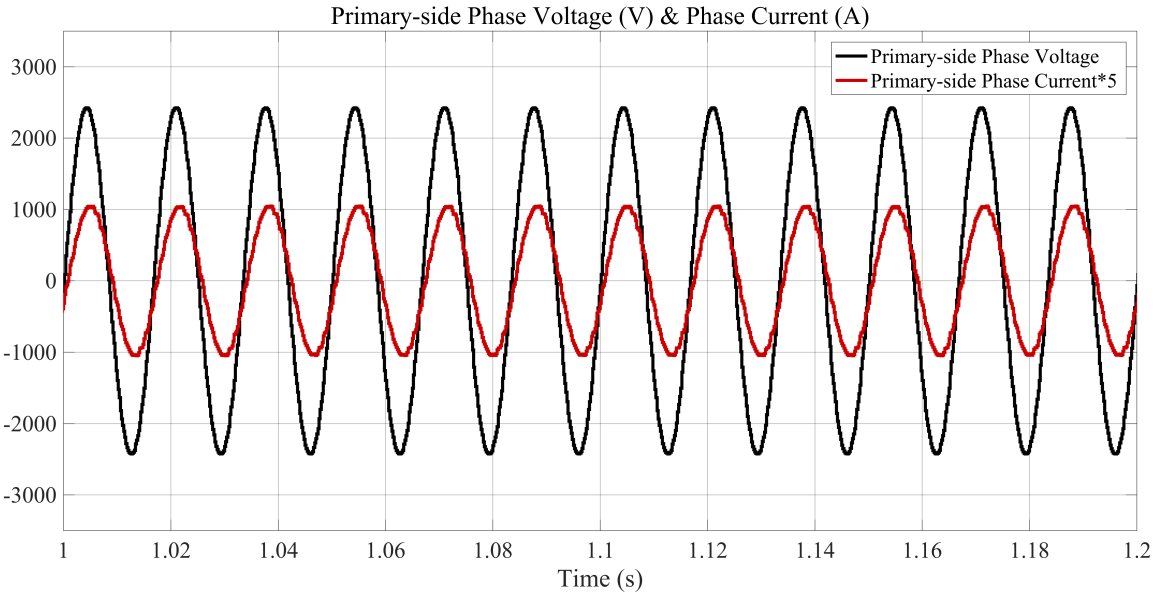


Fig. 2.18 Primary-side phase voltage and phase current of phase-shifting transformer in non-regen condition.

C. Induction Motor

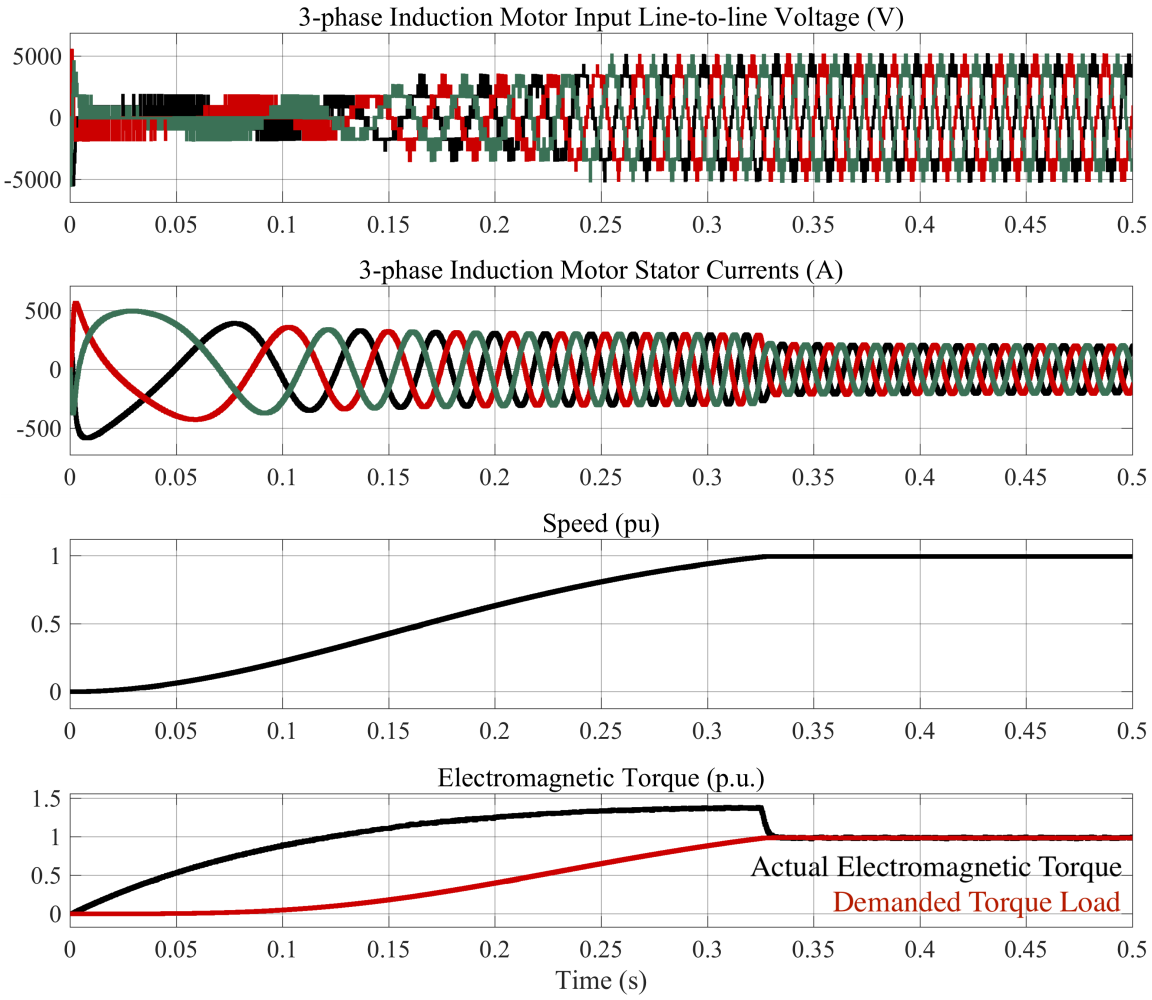


Fig. 2.19 Induction motor waveforms in non-regen condition.

Fig. 2.19 are typical waveforms of induction motor in non-regen condition, including 3-phase input line-to-line voltages, 3-phase stator currents, actual speed and electromagnetic torque. The input voltage of induction motor is the output voltage of 7-level CHB MVMD.

The speed reference is set to 1.0 p.u. when $t = 0$ s, it is obvious that the speed of induction motor accelerates and can be steadily controlled to the reference speed after around 0.32 s.

The demanded mechanical torque T_m is shown as the pink curve in the fourth picture, which gradually increases from 0 p.u. to 1.0 p.u., blue curve represents the electromagnetic torque T_e of induction motor. T_e is higher than T_m in initial stage, which is because the starting torque is higher in order to resist against motor inertia. T_e follows the demanded T_m in steady state.

2.4.2 Simulation Results of a 3 kV Regen CHB MVMD

In the simulation study of regen-CHB MVMD, the drive is controlled and operated in regeneration mode in initial stage with a negative demanded mechanical torque for induction motor, and then shifted to motoring mode as a positive torque applied upon. Similar to the non-regen CHB MVMD, simulation results for regen CHB MVMD cover the voltage and current waveforms of CHB inverter, dc-link capacitors and phase-shifting transformer, as well as the speed and torque performance of induction motor.

A. 7-Level CHB Inverter & DC-link Capacitors

Fig. 2.20 shows the shifting states of output line-to-line voltage V_{AB} and phase A output current I_A of the 7-level CHB inverter in regen CHB MVMD. Due to higher dc-link voltages, V_{AB} appears less voltage levels to build up overall voltage outlet.

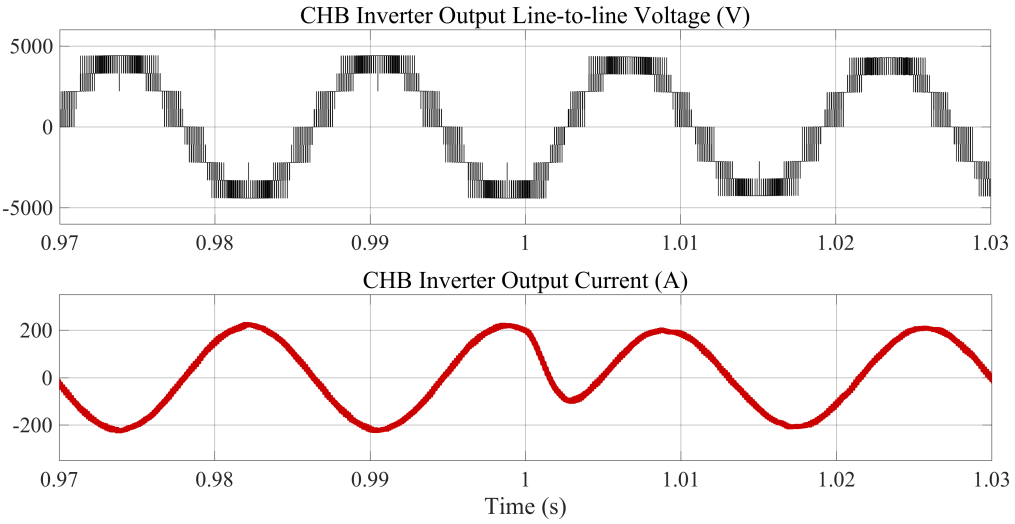


Fig. 2.20 Regen CHB inverter output line-to-line voltage and output current.

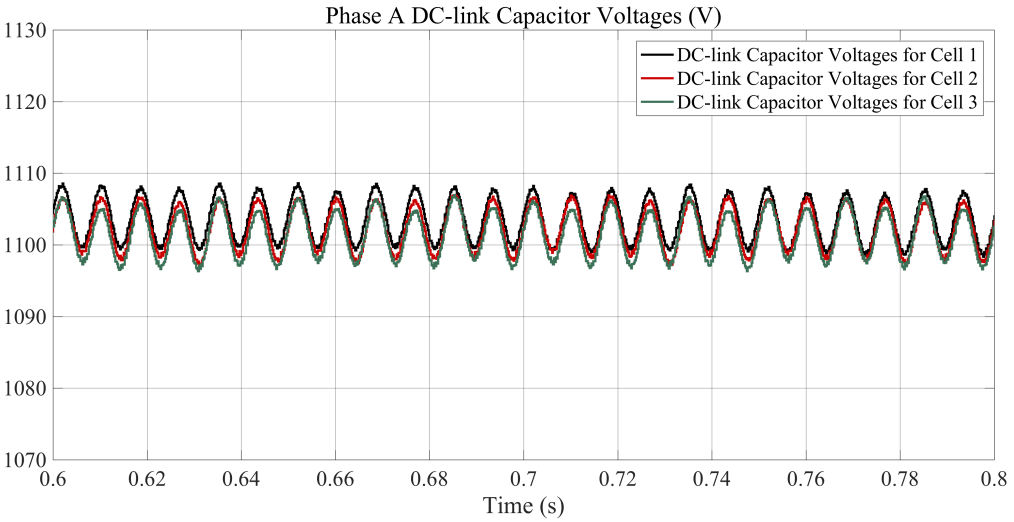


Fig. 2.21 Dc-link capacitor voltages for three regen CHB power cells in phase A.

Dc-link capacitor voltages in regen CHB power cells are controlled to around 1100 V as shown in Fig. 2.21, so as to compensate the influence from secondary-side line filter of phase-shifting transformer.

B. Phase-shifting Transformer

Primary-side phase voltage and phase current of the phase-shifting transformer in regen CHB MVMD are presented in Fig. 2.22. In regeneration mode, the phase difference between voltage and current is controlled as 180°, a reserved power factor $= 1$, or power factor $= "-1"$ can be expected, showing a full active power is sent back to the power grid. In motoring mode, the phase difference between voltage and current is controlled as 0°, power grid can operated with a power factor $= 1$.

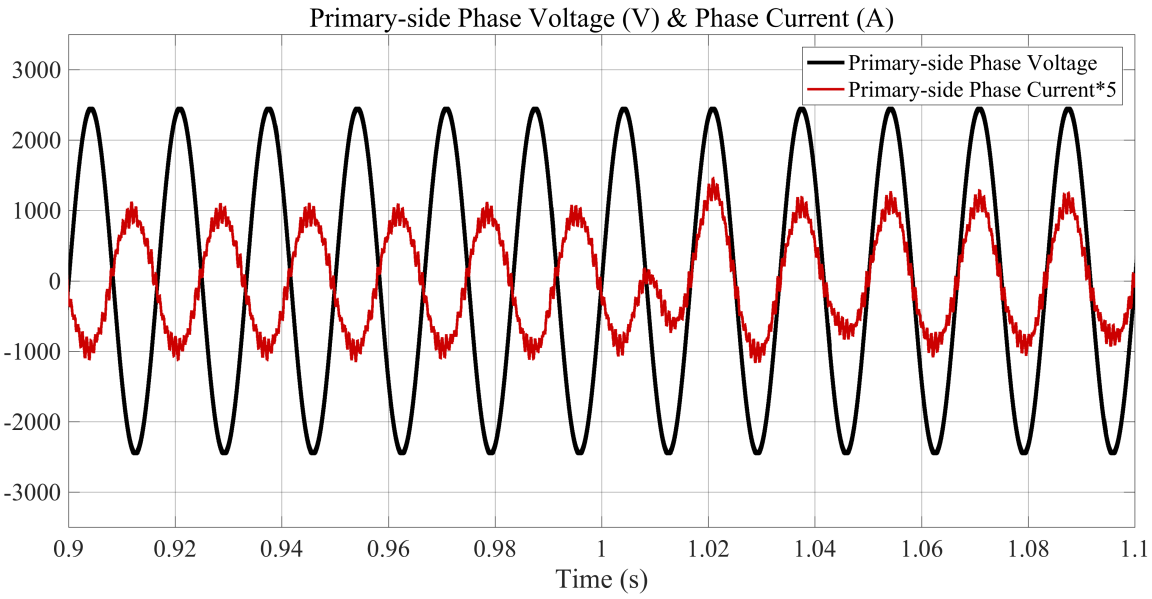


Fig. 2.22 Primary-side phase voltage and phase current of phase-shifting transformer in regen condition.

C. Induction Motor

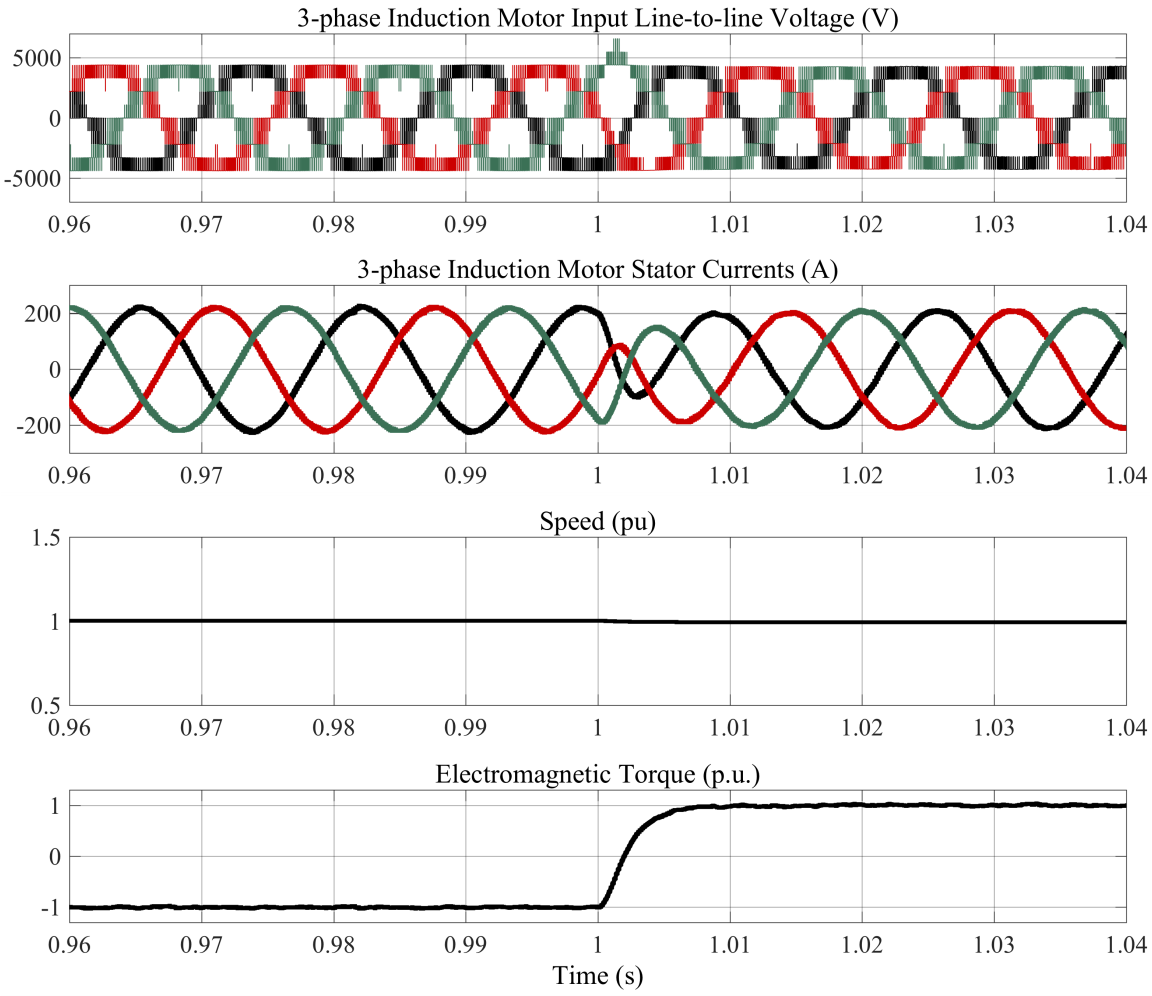


Fig. 2.23 Induction motor waveforms in regen condition.

Fig. 2.23 are waveforms of induction motor in shifting state of the regen CHB MVMD, including 3-phase input line-to-line voltages, 3-phase stator currents, actual speed and electromagnetic torque.

Initially, a -1.0 p.u. demanded mechanical torque is applied to the induction motor, the motor operates as a generator in practice. At $t = 2$ s, the applied torque is set to 1.0

p.u. and the induction motor works in motoring condition. The speed of induction motor is well-controlled as 1.0 p.u. in shifting stage.

2.5 Summary

This chapter gave introductions for both non-regen and regen CHB MVMDs. A CHB inverter is composed of H-bridge inverters connected in cascade. The SPWM patterns for individual single-phase H-bridge inverter and CHB inverter phase leg were illustrated. The constructions and differences between non-regen CHB power cell and regen CHB power cell were mentioned. Regen CHB power cell has a control freedom of grid-side power factor by adjusting the sinusoidal reference of 3-phase AFE inverter.

Then the introduction for induction motor, especially squirrel-cage induction motor were presented. Necessary coordinates transformations and *dq*-axis modeling for induction motor were discussed. A common but efficient control technique for induction motor – FOC technique is mentioned, in terms of its concepts and indirect FOC implementation method.

Finally, simulation studies for a 3 kV, 140 A, 7-level CHB MVMD were presented regarding to non-regen condition and regen condition.

Chapter 3

DC-link Power Capacitors for Motor Drive Applications

3.1 Introduction

Capacitors, along with resistors and inductors, are a kind of passive components widely used in electrical and electronic applications, deservedly, in a regen CHB motor drive. DC-link power capacitors for regen CHB motor drives are a cluster of capacitors with higher unit capacitance, higher voltage rating and higher ripple current rating etc., which perform as electrical energy containers in the dc-bus of a regen CHB converter. Regardless of whether they are bulky terminal-screwed capacitors connected via bus bars, or smaller snap-in capacitors mounted on power PCBs, dc-link power capacitors are clearly distinguished from those ones used for signal coupling, circuit tuning, electronic filtering etc. in lower-voltage applications.

A pair of electrical conductors known as electrodes, between which insulating layer acting as dielectric is sandwiched. Even though different types of dc-link power capacitors possess this similar construction, they diverse not only in physical shapes and structures, but also in capacitor material used in manufacturing process.

In this thesis, two types of dc-link power capacitors: electrolytic capacitors and film capacitors, will be considered. The rest of sections in this chapter will deliver basic introductions, framework for capacitor comparison, as well as dc-link capacitor reliability analysis methodologies for both electrolytic capacitors and film capacitors.

3.2 Electrolytic Capacitors

Electrolytic capacitors have an anode and a cathode electrodes. Metalized anode attached by an oxide formation acting as the dielectric. Cathode is represented by the internal electrolyte, either liquid or solid type are available. This construction makes electrolytic capacitors a kind of polarized capacitors. Based on the chemical composition of dielectric used, there are three types of electrolytic capacitors available in market: aluminum electrolytic capacitors, tantalum electrolytic capacitors, and niobium electrolytic capacitors.

Due to their excellent performance/price ratio and wide available range of capacitance and voltage ratings, aluminum electrolytic (Al-Elec) capacitors are those,

which are well-known and dominate in electrolytic capacitors market share, especially for power electronics. The introduction of Al-Elec capacitors will be presented as an example.

3.2.1 Aluminum Electrolytic Capacitors

Fig. 3.1 shows the basic construction of an aluminum electrolytic capacitor. It consists of two electrode parts: the anode and the cathode, a nanoscale forming anodic oxidation (Al_2O_3) layer sprawls on anode, performing as dielectric. In addition, an absorbent paper spacers is sunk in electrolyte to avoid short circuit, the electrolyte serves as the true cathode. Another aluminum cathode foil having contact with electrolyte also makes physical connection with capacitor negative terminal and acts as nominal physical cathode. Some main components in an Al-Elec capacitor will be discussed.

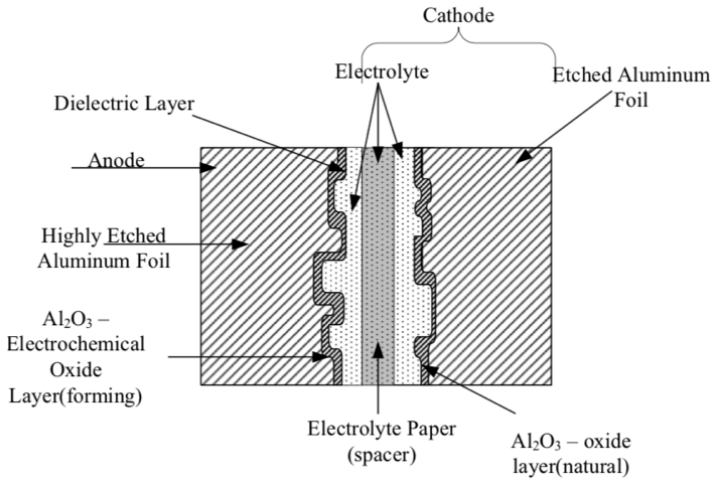


Fig. 3.1 Structure of an aluminum electrolytic capacitor [11].

A. Anode

Anode electrode is basically made up with nearly 100% pure aluminum foil with a 20~100 μm thickness. The foil is a surface-enlarged one processed with electrochemical etching, which is shown in Fig. 3.2 for an anode foil with high voltage rating. The effective surface area of an etched aluminum foil can be hundred times of those of flat surface [12]. This is to make the utmost of possible maximum capacitance for anode, and passing desirable electron flow for cathode [13].

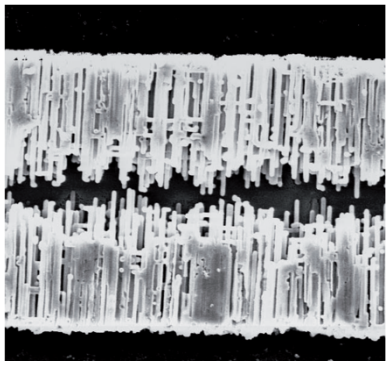


Fig. 3.2 An etched foil for high voltage anode [14].

B. Dielectric

Dielectric is an insulating layer consisted of Al_2O_3 attached on the anode aluminum foil. It is formed in the process when the anode generates a group of electrons and it flows to the cathode side with surroundings of electrolyte. Two main chemical reaction steps exist:

$$2\,Al + 6\,H_2O \rightarrow 2\,Al(OH)_3 + 3\,H_2\uparrow$$

$$2\,Al(OH)_3 \rightarrow 2\,Al_2O_3 + 3\,H_2O$$

The first oxidation step transfer aluminum to aluminum hydroxide ($Al(OH)_3$), generating heat and producing hydrogen gas, which will accumulate the internal pressure of Al-Elec capacitors. The second reaction transforms $Al(OH)_3$ into Al_2O_3, which effects as dielectric. This kind of compact Al_2O_3 layer can keep anode aluminum foil from corrosion and avoid persistent oxidation reaction. The dielectric ratio of Al_2O_3 is around 1.0 nm/V, so the voltage rating of an Al-Elec. capacitor is influenced by how strong the forming of Al_2O_3 is, i.e., the thickness of Al_2O_3.

Fig. 3.3 shows a 100 k times zoomed-in picture of an etched anode foil pore, the dark grey area in a circle is Al_2O_3 dielectric.

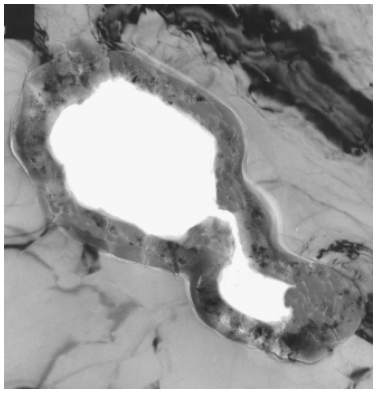


Fig. 3.3 An etched pole on anode foil. Light grey: aluminum. Dark grey: Al_2O_3 [15].

C. Cathode

Cathode foil of an Al-Elec capacitor is also an etched aluminum foil with very tiny thickness, having contact with electrolyte. The required purity of aluminum for cathode is about 99.8%, relatively lower than the requirement for anode. It has a naturally formed

Al_2O_3 layer on the surface. Considering the contact resistance between cathode foil and electrolyte, surface metallization of copper, titanium etc. can be applied upon cathode foil.

D. Electrolyte

Electrolyte of an Al-Elec capacitor is a liquid or solid conductive materials, made up with dissolvent accompanied with add-ons, to reduce the dissolvent corrosion towards aluminum. Major effect of electrolyte is conducting the electrons, but some other characteristics such as electrochemical stability, lower evaporating rate, wider operating temperature range, less hazardous to environment also count much on determining which type of electrolyte shall be used. The most common-used types of electrolytes include ethylene glycol-based, anhydrous organics-based, water-based and solid polymer-based.

E. Spacer

Spacer made of absorbent fiber is used to protect two electrodes from contacting directly with each other, in which circumstance a short-circuit problem might occur. Another role of spacer is storage tank of electrolyte to reduce the loss of electrolyte during operation.

3.2.2 Why Aluminum Electrolytic (Al-Elec) Capacitors?

Electrolytic capacitors under different categories of anode materials possess disparate in-duty characteristics, which has essential influence on deducing if a group of capacitors are competent enough to be dc-link power capacitors for regen CHB motor drives.

For example, in a 4.16 kV medium voltage regen CHB motor drives, its secondary voltage of phase-shifting transformer can be around 600~700 Vac. This means that the dc-link voltage level can reach up to ~1000 Vdc during motoring period, taking no account of the motor drive will extract power from braking motor and boost the dc-link voltage up during regeneration. The dc-link power capacitors generally need to be connected into series and parallel as capacitor banks to sustain overall inflicted voltage and meet capacitance requirements. Also capacitors with decent ratings could keep a good balance between number of in-built capacitors, volumes, cost and reliability of capacitor banks.

In summary, the voltage rating of a dc-link power electrolytic capacitor is one of the dominant factors that needs to be considered. Moreover, the available capacitance of a dc-link power electrolytic capacitor should be high enough to ensure adequate power reserving capability. With regard to the working environments, a regen CHB motor drive may devote themselves into harsh working conditions with high ambient temperature, especially in metallurgy, mining etc., hence operating temperature range is another criterion that worth a notice.

Table 3.1 summarizes three types of electrolytic capacitors grouped by anode materials and electrolytes that utilized inside capacitors. The available capacitance range, maximum rated voltage and category temperature are listed. Based on information in Table 3.1, it is apparent that Al-Elec capacitors with liquid electrolyte are much more superior to other types of capacitors in respect of available capacitance, along with satisfying voltage rating and moderate category temperature.

TABLE 3.1 COMPARISON BETWEEN DIFFERENT ELECTROLYTIC CAPACITORS [16]

Electrolytic Capacitor Type	**Electrolyte Material**	**Available Capacitance Range (μF)**	**Threshold Rated Voltage (V)**	**Threshold Category Temperature (℃)**
Aluminum Electrolytic Capacitors	Liquid: glycol-based	0.1~2,700,000	630	85/105
	Liquid: organics-based	0.1~1,000,000	550	105/125/150
	Liquid: water-based	1~18,000	100	85/105
	Solid: polymer-based	10~1,500	25	105
Tantalum Electrolytic Capacitors	Liquid: sulfuric acid	0.1~18,000	630	125/200
	Solid: manganese dioxide	0.1~3,300	125	125/150
	Solid: polymer	10~1,500	25	105
Niobium Electrolytic Capacitors	Solid: manganese dioxide	1~1,500	10	105
	Solid: polymer	4.7~470	16	105

Compared with tantalum and niobium as rare metals demanding complex preparation craft, aluminum is a common light metal upon which mature and economical processing techniques have developed for hundred years.

Table 3.2 presents a comparison on oxidation dielectrics for these three electrolytic capacitors. Three criteria are introduced here:

Relative permittivity reveals the capacitor attribute on electric conduction; Breakdown voltage indicates the intensity of forming voltage that can be applied on dielectric; Dielectric ratio shows the relationship between dielectric thickness versus forming voltage, impacting actual volume of capacitors.

TABLE 3.2 COMPARISON BETWEEN DIFFERENT TYPES OF DIELECTRICS [17,18]

Dielectric Type	**Oxide Crystalline**	**Maximum Relative Permittivity**	**Maximum Breakdown Voltage (V/μm)**	**Minimum Dielectric Ratio (nm/V)**
Aluminum Oxide (Al_2O_3)	Yes	14.2 [19]	1000 [20]	1.0
	No	9.6	710	1.4
Tantalum Pentoxide (Ta_2O_5)	No	27	625	1.6
Niobium Pentoxide (Nb_2O_5)	No	41	400	2.5

Although excellent relative permittivity possessed, oxide of tantalum and niobium are restrained by relatively lower breakdown voltage and higher dielectric ratio, making it unfavorable to yield good products for dc-link power electrolytic capacitors.

Al-Elec power capacitors have occupied a great portion of market share on motor drives and their performances have been proved. Therefore, it is appropriate to draw a

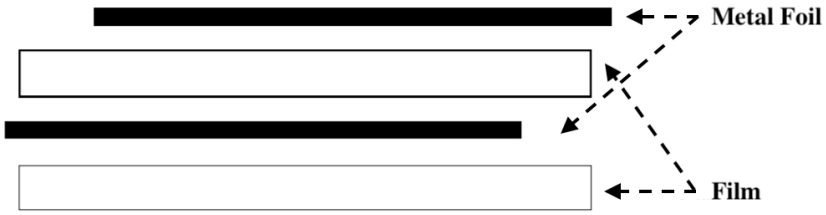
conclusion here that for regen CHB motor drives' dc-link implementation, Al-Elec capacitors are good candidates under electrolytic capacitor category, with respects of capacitance, voltage rating and operating temperature, as well as economic indicators such as cost and volume.

However, due to the reliability issues such as electrolyte evaporation and capacitance drift under higher temperature, the actual lifetime expectancy of Al-Elec capacitors is usually less than a decade, which prompts a trend on ameliorating the lifetime of Al-Elec capacitors, or even finding a substitute to create a new possibility for motor drives' dc-link solution.

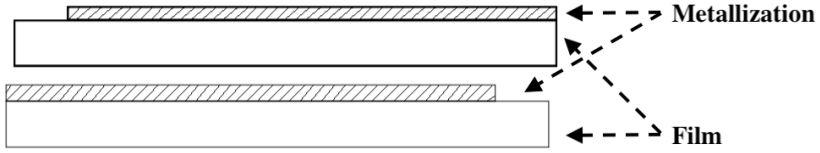
3.3. Film Capacitors

Film capacitors, as name presenting, is a kind of capacitors which make use of a pair of polymer plastic film as dielectric materials. The dielectric film is a very thin layer but still maintain a good dielectric strength. The Electrode pair of film capacitors are metallic, usually aluminum and zinc will be used and connected with two external terminals. Metal electrodes and dielectric films will be wound into cylindric shape during processing for power film capacitors. Direct electric connection can be made between electrodes which can significantly reduce contact resistance. In excuse of no distinction of anode and cathode, consequently a film capacitor is non-polarized.

Two methods of metallization arrangement of electrode on dielectric film are commonly used by capacitor manufacturers and can be used for clarification: foil/film and metallized film, as shown in Fig. 3.4.



(a) Foil/film structure.



(b) Metallized film structure.

Fig. 3.4 Two metallization arrangement of electrodes [21].

For a foil/film-structured film capacitor, the polymer film is attached with a thin metal foil, in order to increase the electric conduction. A metallized film capacitor has polymer plastic films coated with an extremely thin, nanoscale metallization layer instead. This kind of structure proudly behaves a “self-healing” attribute, which avoids damage of capacitor due to localized breakdown spots on dielectric films. With a view to this advantage, metallized film (MF) capacitors will be introduced as an example.

3.3.1 Metallized Film (MF) Capacitors

MF capacitors utilize attached metallization layers instead of individual metal foils as the electrodes. The most extraordinary feature of a MF capacitor compared with a film/foil one is self-healing.

If a MF capacitor faces a surge voltage stress or any defect such as puncture, external particulate contamination on metallized film, a breakdown on the defect location might appear, leading to stored energy discharge and causing extreme localized temperature rise. The produced heat vaporizes that tiny metallized electrode part and the discharge process will be suspended in consequence in an instant. The entire procedures can be fulfilled within microseconds, leaving negligible impact on overall operation. Finally, the MF capacitor can get back to normal with a small capacitance loss, as the so-called "self-healing" process, which is shown in Fig. 3.5.

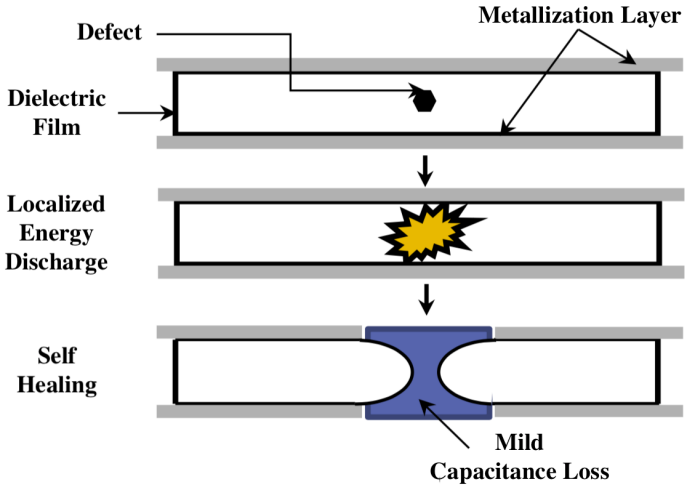


Fig. 3.5 Self-healing process of a metallized film [22].

Notwithstanding a mild degradation on capacitance might occur, which is one of the sources of capacitance wear-out mechanisms for MF capacitors, self-healing avoids extreme breakdown in most circumstances and is often used in the course of processing as an film purifying approach to eliminate contaminators. Thanks to self-healing process, generally a MF capacitor requires no additional protection for film materials and contributes an excellent volumetric efficiency for themselves. Nevertheless, if voltage stress is too high and the film is not robust enough to sustain energy discharge, a MF capacitor can perform deformation even explosion due to intense self-healing, as shown in Fig. 3.6.

Fig. 3.6 Intense self-healing causes film explosion [23].

3.3.2 Why Metallized Polypropylene Film (MPPF) Capacitors?

The characteristics and application of MF capacitors vary between different dielectric materials. Usually four types of dielectric polymer can be used by MF capacitors and dominate the market share: polyethylene terephthalate (PET), polypropylene (PP), polyethylene naphthalene (PEN) and polyphenylene sulfide (PPS). PP material is the most-

welcomed film material in power capacitor applications. The comparison between metallized polypropylene film (MPPF) capacitors with other three polymer plastic dielectric films will be delivered in this section.

Different polymer dielectric films and the corresponding key characteristics are listed in Table 3.3. It is clear enough to figure out the reason why MPPF capacitors can be dominant in power application. The first row in the list shows the maximum breakdown voltage, i.e. dielectric strength, of those film materials. Clearly, PP material is equipped with the best performance, which makes it the least vulnerable-to-voltage polymer film among the film family. In reality the possible rated voltage of a MPPF power capacitor can reach to 2000 VDC. For a regen CHB motor drive with a ~1000 VDC dc-link voltage, merely one single powerful MPPF capacitor is sufficient to satisfy the voltage requirement.

TABLE 3.3 CHARACTERISTICS OF DIFFERENT POLYMER DIELECTRIC FILMS [24]

Film Type / Characteristics	PP	PET	PEN	PPS
Max. Breakdown Voltage (V/μm)	650	580	500	470
Max. Relative Permittivity	2.2	3.2	3.0	3.0
Max. Operating Temperature (℃)	105	125	150+	150+
Max. Dielectric Absorption (%)	0.1	0.5	1.2	0.1
Max. Moisture Absorption (%)	0.05	0.4	1.2	0.1
Capacitance Drift	± 2.5%	± 5%	± 5%	± 1.5%
Dissipation Factor at 1 kHz (tanδ)	0.05%	0.5%	0.4%	0.15%
Self-healing Capability	Superior	Moderate	Moderate	Inferior

Dissipation factor (tanδ) and self-healing capability are another two important criteria that make MPPF capacitors surpass others. PP material has the lowest tanδ, leading to a relatively lower internal resistance. Less thermal power loss will be generated when a ripple current flows into a MPPF capacitor. It is important for keeping capacitor banks from over-heating and improving the lifetime performance of regen CHB motor drives. What's more, the superior self-healing is a plus for overall reliability. PEN and PPS materials are not qualified enough to meet those requirements.

Ambient temperatures greater than +105 ℃ are usually quite rare in motor drive applications, while PET, PEN and PPS materials are more specific for higher temperature in-duty conditions or surface mount device (SMD) packaging for smaller-scale capacitor products.

In summary, all these judges and weighing serve as a basis to determine the preponderant status of MPPF capacitors on power applications under film capacitor category. Even though the prices of MPPF capacitors are usually higher than Al-Elec capacitor, there is a trend to make them potential candidates to replace Al-Elec capacitors for a regen CHB motor drive's dc-link solution regarding to system reliability and power loss. This is because of MPPF capacitors' less-vulnerable to thermal influence and relatively lower dissipation factor.

3.4 Capacitors Behavior Influence Factors

Either Al-Elec capacitors or MPPF capacitors will be posed threats when they are put into different types of behavior influence factors from an actual regen CHB motor drive. These might change the behaviors of a capacitor in terms of state of health (SOH) and useful lifetime (UL) compared with ideal situation, even worse, impact the capacitor lifetime or cause an irreversible failure. Therefore, some pivotal behavior influence factors need to be mentioned.

A. Applied Voltage

The applied voltage of a dc-link power capacitor means the actual electric potential difference that being applied upon two electrodes of a capacitor. Usually it is calculated as rms voltage for alternating voltage, to be in accordance to the capacitor's dc rated voltage. The applied voltage of a dc-link power capacitor is mainly restricted by the breakdown voltage of capacitor's dielectric and can be expressed as:

$$V_a \leq V_R < V_b = E \cdot d \tag{3.1}$$

where V_a is applied voltage, V_R is rated voltage and V_b is dielectric breakdown voltage, E is dielectric strength, and d is the dielectric thickness. Breakdown voltage appoints the voltage threshold that a capacitor dielectric can sustain but without performing an electrical conductivity, to make sure the energy containing capability of the dielectric. A huge inrush voltage variation (dV_a/dt) can lead to an intensive self-healing process for MPPF capacitor

particularly. A long-term reversed applied voltage can cause rapid and catastrophic breakdown of an Al-Elec capacitor's oxide dielectric and must be eschewed in reality.

The applied voltage of a dc-link power capacitor might can have an impact on capacitor's leakage current as well, which indicates a small residual dc current component in steady state of capacitor charging process, especially when the voltage level exceed the rated value. This process is more obvious in high-temperature environments.

B. Ripple Currents

Ripple currents are defined as those current components whose locations on frequency spectrum are different from dc component. Usually they appear as a result of ripple voltage or voltage pulsation. In the dc-links of a regen CHB motor drive, the ripple currents can be derived from the switching patterns of power semiconductor devices in modulation, the source energy (grid, motor etc.) and control technique (3^{rd}-order harmonics injection etc.).

Ripple currents take a significant position on contributing total thermal power loss of a dc-link power capacitor, as well as influencing the lifetime due to consequent self-heating which rises core temperature of a capacitor. The equation for thermal power loss can be expressed as:

$$W_{th} = W_r + W_l$$
$$= I_r^2 \cdot ESR + V_a \cdot I_l \tag{3.2}$$

where W_{th} represents the total thermal power loss, W_r, W_l are ripple-current-caused power loss, leakage-current-caused power loss respectively. I_r is equivalent overall ripple current on a specific base frequency, ESR is the equivalent series resistance. I_l is the leakage current.

Leakage current of a capacitor mainly depends on the dielectric material quality and can be minimized in manufacturing process, while ripple-current behavior of a capacitor strongly lies on actual operating conditions. Consequently, the ripple current's order of magnitude is way more than that for leakage current in most cases and is one of the chief culprits in affecting a capacitor's thermal behavior and harming its lifetime.

Consequently, neglecting the influence of leakage current, the ripple-current-generated thermal power W'_{th} can be derived as:

$$W'_{th} \cong W_r = I_r^2 \cdot ESR \tag{3.3}$$

I_r is defined as equivalent overall ripple current. That's because ripple currents of a regen CHB motor drive's dc-link power capacitor locate on different places on frequency spectrum, with diverse amplitudes. Operating temperature and cooling methods can influence the effect of ripple currents as well. Therefore, a tuned form of ripple current expression $\hat{I}_{ri}$ can be applied as:

$$\hat{I}_{ri} = \frac{I_{ri}}{f_i \cdot \mu_t \cdot \mu_a} \quad (i = 1, \cdots, n) \tag{3.4}$$

in which I_{ri} are rms values of actual ripple current components which has different frequencies, f_i are frequency multipliers introduced to scale those harmonics' effects and equivalently transfer them upon a base frequency, μ_t, μ_a are temperature multiplier and air cooling multiplier respectively, which are used to adjust the self-heating strength. n is total number of involved ripple current components.

In order to reflect the overall impacts from those ripple current components, total equivalent ripple current on a base frequency can be defined as:

$$I_r = \sqrt{\sum_{i=1}^{n} \hat{I}_{ri}^{\,2}} = \sqrt{\sum_{i=1}^{n} \left(\frac{I_{ri}}{f_i \cdot \mu_t \cdot \mu_a}\right)^2} \tag{3.5}$$

Then I_r is equivalent root-sum-square ripple current on that specific base frequency. For a universal grid with 60 Hz frequency, 120 Hz is set as the base frequency, and utilized as a criterion.

C. Core Temperature

Core temperature of power capacitors is understood as the equivalent temperature on the physical center of a capacitor. The core temperature is related to ambient temperature, ripple current, and thermal conducting efficiency of cooling methods.

The core temperature of a power capacitor has prominent correlations with capacitor's current behaviors and dielectric deformation (for MPPF capacitors) or

electrolyte evaporation (for Al-Elec capacitors). The relationships between capacitor core temperature and ambient temperature is shown in Fig. 3.7 and defined as Eq. (3.6).

$$T_{core} = T_{amb} + \Delta T_{core} \tag{3.6}$$

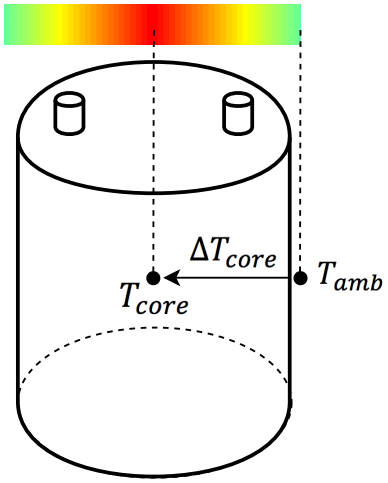


Fig. 3.7 Definition of a capacitor's core temperature.

where T_{core} is core temperature [K], T_{amb} is ambient temperature [K], ΔT_{core} is core temperature rise (CTR) [K].

Recalling Eq. (3.3) and assuming the ripple-current-generated thermal energy transforms to temperature variation inside the capacitor, which means:

$$\Delta T_{core} = W'_{th} \cdot R_{th} = {I_r}^2 \cdot ESR \cdot R_{th} \tag{3.7}$$

where R_{th} is thermal resistance [K/W], therefore Eq. (3.6) can be derived as:

$$T_{core} = T_{amb} + \Delta T_{core} = T_{amb} + {I_r}^2 \cdot ESR \cdot R_{th} \tag{3.8}$$

Or as:

$$T_{core} = T_{amb} + \left(\frac{I_r}{I_r^*}\right)^2 \cdot \Delta T_{core}^* \tag{3.9}$$

where ΔT_{core}^{*} is the nominal CTR [K] caused under nominal ripple current condition, I_r^* is nominal ripple current on base frequency at category maximum temperature. According to the accessible datasheets and technical documentations from capacitor manufacturers, R_{th} is a more common parameter for MPPF capacitors, meanwhile ΔT_{core}^{*} is more specified for Al-Elec capacitors.

Eq. (3.8), Eq. (3.9) reveal the core temperature behavior of a power capacitor with reflections of ambient temperature and ripple-current-caused self-heating. It is obvious that the core temperature for a capacitor receives impacts from both ambient temperature and ripple currents.

D. Humidity

The ambient humidity of power capacitors have sophisticated electrochemical impacts on capacitor's behaviors, not only for operating conditions but also for storage. Usually the humidity degree of an environment is illustrated by relative humidity (RH), defined as the ratio of absolute humidity and maximum humidity, as Eq. (3.10).

$$RH = \frac{AH}{MH} \cdot 100\% \tag{3.10}$$

where AH is absolute humidity (total mass of water vapor in a constant volume of air), MH is maximum humidity (maximum water vapor mass that a certain volume of air can hold without condensation). RH represents the saturation level of water vapor.

For environments of high relative humidity (>95%), or having direct contact with liquid water or water vapor. Moisture may penetrates into the capacitor cases and gradually removes the metallization layer of MPPF capacitors, or corrodes the aluminum electrodes of Al-Elec capacitors. Additional coating protection can availably control this process, and usually a range of permissible relative humidity would be set by manufacturers.

Moderate relative humidity levels (50~95%) can be a kind of stress that influence capacitor lifetime in long-term aspect, particularly for a MPPF capacitor. A polymer plastic film can absorb moisture and undergo a reversible linear capacitance variation. The capacitance change caused by humidity can be described by a humidity coefficient α_{RH}, indicating the capacitance change under every 1% relative humidity change, which is defined as:

$$\alpha_{RH} = \frac{2 \cdot (C_b - C_a)}{(C_a + C_b) \cdot (RH_b - RH_a)} \tag{3.11}$$

in which C_b is the capacitor's capacitance under relative humidity RH_b, C_a is the capacitor's capacitance under relative humidity RH_a, the maximum α_{RH} of a MPPF capacitor is ~$1.0 \times 10^{-4}/\%RH$. For relative humidity that less than 30% the humidity coefficient is relatively nontrivial and can be neglected.

E. Other Behavior Stresses

There also exist some behavior stresses that can have influences but mild or neglectable ones for power capacitors' performance and lifetime. For example, dielectric

absorption is a hysteresis appearance that a capacitor can still possess a small voltage even after discharging or disconnection. Pulsed charging/discharging, which means frequent charging/discharging alternating cycles, may contribute to capacitance drop. Such less-important behavior stresses are more common to small capacitors in electric circuits but trivial for a normally-operating regen CHB motor drive. Non-operation factors such as design defect, manufacturing, storage, mounting are also sources for capacitor behavior stresses but relates with subjective human manipulation. Thus, these behavior stresses will not be covered in this thesis.

3.5 Reliability Analysis of Power Capacitors

The reliability of regen CHB motor drives is counted on different aspects of issues. For a regen CHB power cell, as discussed before, is mainly consisted of semiconductors (i.e. IGBTs) topologies and dc-link power capacitors, along with corresponding gate drivers, contactors, sensors, and controllers. Even though semiconductor failures come to the top on power cell failures [25], due to overvoltage or overcurrent caused by incorrect operation of gate drivers. However, a failure from semiconductors usually leads to voltage waveforms distortion or inrush current which can be detected by sensors then triggers the security mechanism, such as switching off the semiconductors' contactors or activating by-passing,

even system shut-downs. None catastrophic failures would happen due to semiconductor failures in most circumstances.

Capacitors, as the only energy storage components in power cells, can perform extremely hazardous failures caused by arcing and explosion, as shown in Fig. 3.8, which pose threats upon system safety, even worse, harming human lives. Long-term and costly overhaul in a motor drive maintenance period, commonly known as meantime between failures (MTBF) is required as a consequence. Although oversizing design for capacitors is a usual methods to reduce the electrical failure possibility for dc-link power capacitors, it is done at the expense of power cell volumes and cost. There is a trend in industry to take a notice of the trade-off design of dc-link power capacitors, in order to develop a cluster of new-generation power cells with compact sizes, and maintaining a good reliability in the same time.

Capacitors in motor drives are facing more harsh operating environments than before, such as high ambient temperature and high humidity in emerging applications [26]. In terms of accurate decision making for reliability, repair and replacement [11], it is appropriate to comment that the necessity on diagnosing and prognosing reliability of dc-link power capacitors [27] in a regen CHB motor drive is essential and will be introduced in following sections.

(a) Arcing-caused burns [28].

(b) Explosion [29].

Fig. 3.8 Extreme hazards of dc-link power capacitors.

3.5.1 Failures Classification

As mentioned before, capacitor reliability is influenced by varieties of failure mechanisms and corresponding stress factors. Generally, failures come down to a dc-link power capacitor can be classified into two kinds: abrupt breakdowns and wear-out issues.

Usually sudden breakdowns are defined as open-circuit or short-circuit failures, caused by random catastrophic externality (mounting fault, disconnection, etc.). Wear-out issues weigh more in capacitor reliability because the degradation of circuit parameters such as series capacitance C_s and equivalent series resistance ESR dominantly determine the end-of-life (EOL) criteria and state-of-health (SOH) monitoring of a capacitor unit in practical operations.

Table 3.4 summarizes crucial failure modes, failure mechanisms and corresponding reliability stress factors of Al-Elec capacitors and MF capacitors. Stress factors marked with red are those have relatively significant influences [26]. It can be noticed that as

discussed in subsection 3.2, ambient temperature, ripple current, applied voltage, and humidity appear dominance on affecting capacitor reliability, especially on parameter wear-out problem compared with sudden breakdowns.

TABLE 3.4 FAILURES CLASSIFICATION OF TWO DC-LINK POWER CAPACITOR TYPES

Capacitor Type	Failure Modes	Failure Mechanisms	Stress Factors
Al-Elec Capacitors	Open-circuit Failure	Terminal Disconnection	Mounting, Vibration
		Electrolyte Dry-out	Electrolyte Leakage
	Short-circuit Failure	Breakdown of Al_2O_3 Layer:	Weak Points on Al_2O_3 Layer
		Breakdown of Paper Spacers	Conductive Particle on Paper
	Parameter Wear-out	Electrolyte Evaporation: Pressure↑, C↓, ESR↑	T_{amb}, i_{RC}, V_a, Pulsed Discharge
		Degradation of Al_2O_3 Layer: T_{core}↑, i_{LC}↑, C↓, ESR↑	T_{amb}, i_{RC}, V_a, Pulsed Discharge
		Degradation of Anode Foil: i_{LC}↑, C↓, ESR↑	T_{amb}, i_{RC}, V_a, Pulsed Discharge
		Degradation of Cathode Foil: C↓, ESR↑	i_{RC}, V_a, Pulsed Discharge
MF Capacitors	Open-circuit Failure	Terminal Disconnection	Mounting, Vibration
		Breakdown of Metallization (Intense Oxidation)	Humidity
	Short-circuit Failure	Breakdown of Polymer Film (Intense Self-healing)	V_a, dV_a/dt, T_{amb}, i_{RC}, Humidity
	Parameter Wear-out	Degradation of Polymer Film: T_{core}↑, C↓, ESR↑	T_{amb}, i_{RC}, V_a, Humidity
		Degradation of Metallization:	T_{amb}, i_{RC}, Humidity

3.5.2 Capacitor Circuit Modelling

The modelling of power capacitors should be introduced to calculate some essential parameters that required in further capacitors reliability analysis.

Fig. 3.9 shows an ubiquitous model for capacitor circuit, where C_{is} is ideal series capacitance between two electrodes, R_s is series resistance, in terms of Al-Elec capacitors it represents contacts of terminals, electrolyte and paper spacers; for MPPF capacitor, it reveals attributes of leads, sprayed metal and metallization layer on polymer film [21]. L_s

is series inductance containing information of connection and winding for Al-Elec Capacitors, skin and proximity effect [30] for MPPF capacitors. R_p is parallel insulation resistance considering leakage current performance, R_d and C_d show dielectric loss and inherent dielectric relaxation caused by molecular polarization [31].

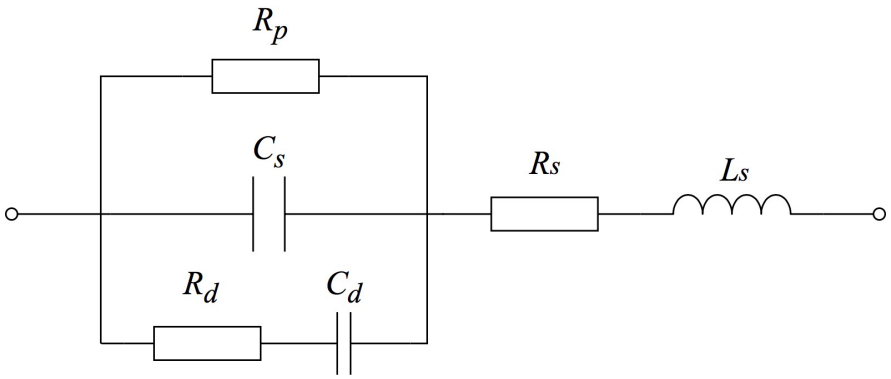


Fig. 3.9 Ubiquitous circuit model for dc-link power capacitors.

In order to simplify the electrical analysis, an equivalent circuit model for dc-link power capacitors as shown in Fig. 3.10 is commonly used, which is consisted of series capacitance C_s, equivalent series resistance ESR and equivalent series inductance ESL.

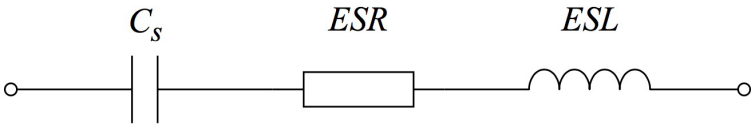


Fig. 3.10 Equivalent circuit model for dc-link power capacitors.

Based on the impedance equality [30,32] the detailed expression of these three parameters' non-degraded values can be derived as:

$$C_{S0} = \frac{\omega^2 p^2 + q^2}{\omega^2 R_p R_d \cdot (C_d q - p)} \tag{3.12}$$

$$ESR_0 = R_s + \frac{R_p R_d \cdot (\omega^2 C_d p + q)}{\omega^2 p^2 + q^2} \tag{3.13}$$

$$ESL_0 = L_s \tag{3.14}$$

where ω is circuit angular frequency depended on source frequency, p, q are two operators defined as:

$$p = R_p C_d - R_p C_{is} + R_d C_d \in \mathbb{R}^- \tag{3.15}$$

$$q = \omega^2 R_p R_d C_d C_{is} + 1 \in \mathbb{R}^+ \tag{3.16}$$

3.5.3 Reliability Analysis Methodologies

In order to estimate or predict power capacitors reliability, physics-based estimation (PE) [32-35] and data-driven monitoring (DM) [30,36-44] are two methodologies that well-embraced by researchers.

Integrated methods which take advantages of both aforementioned techniques are also proposed and applied [45,46]. Instead of directly building physical models of capacitor lifetime, integrated methods try to obtain physical expression of capacitor parameters, briefly C_s and ESR, then cooperate with aging experiment data to fit corresponding lifetime models, actualizing SOH monitoring as well as estimated useful lifetime (EUL).

A. Physics-based estimation (PE Methods)

PE method bases itself on acceleration models which customarily calculates EULs of capacitors by revealing the physics of failure mechanisms. It requires actual applied stress factors in a certain condition, a basic useful lifetime (UL) and nominal parameter values which are usually derived from actual testing under specified operating conditions, and some other empirical or statistic-oriented parameters.

Svante Arrhenius, a Swedish chemist, proposed a chemical kinetics equation that indicates how chemical reaction rates change along with temperature [47]. The equation was named as "Arrhenius law" and has been applied widely as a basic PE method for reliability analysis. It will be discussed in detail in chapter 4.

H. Eyring etc. expanded Arrhenius law and involved other stress factors besides temperature, Eq. (3.17) shows an Eyring PE equation with consideration of other two stresses [48]:

$$EUL_{Eyring}(T_i, S_1, S_2) = A_E T_i^{\alpha} \exp\left(\frac{E_a}{kT_i} + \left(B_E + \frac{C_E}{T_i}\right) S_1 + \left(D_E + \frac{E_E}{T_i}\right) S_2\right) \quad (3.17)$$

where EUL_{Eyring} is estimated useful lifetime of Eyring equation, T_i is temperature stress [K], S_1, S_2 are two supplementary stresses, α, A_E, B_E, C_E, D_E, E_E are constants that need to be determined.

L. Simoni [49] proposed a general PE equation to combine thermal stress with electrical stress. The equation is based on inverse-power law for electrical stresses and Arrhenius law for thermal aging, which is given as:

$$\begin{cases} EUL = L_0 \cdot exp(-B \cdot DT)\left(\frac{E}{E_0}\right)^{-n^*} \\ n^* = n - b \cdot DT \\ DT = \frac{1}{T_0} - \frac{1}{T} = \frac{T - T_0}{T \cdot T_0} \end{cases} \tag{3.18}$$

where L_0 is lifetime at temperature T_0 [K] and $E \leq E_0$, T is applied temperature [K], n is an electrical endurance coefficient, B is a constant in thermal part, E_0 is an electrical stress threshold below which the electrical aging is neglectable, E is actual electrical stress.

Experimental results showed that the combined model was in agreement with actual lifetime curves.

B. Data-driven monitoring (DM Methods)

PE methods can predict how long can a dc-link capacitor be sufficiently competent under an operation, but it is not proposed for delivering real-time estimation of capacitor degradation. On contrary, data-driven monitoring (DM) method analyzes the statistical data to estimate the SOH of a dc-link capacitor basing on the real-time fitted curves of C_s, ESR at any specific time. It needs empirical modelling of capacitor parameters, and then real-world testing data can be used in parameter confirmation and further modifications of

models. DM methods can predict the lifetime of dc-link capacitor as well if EOL criteria are determined in advance. The major limitation of DM method is its modelling relies highly on statistics and it is empirics-oriented, which may vary a lot for different capacitor products.

C_s and ESR, as two indicator, EOL thresholds (C_{EOL}, ESR_{EOL} respectively) of which need to be determined. Those thresholds are essential to define SOH monitoring range, which indicates the time domain interval that a dc-link power capacitor can be applied with surveillance, meanwhile showing EOL spot (t_{EOL}) of it, as shown in Fig. 3.11.

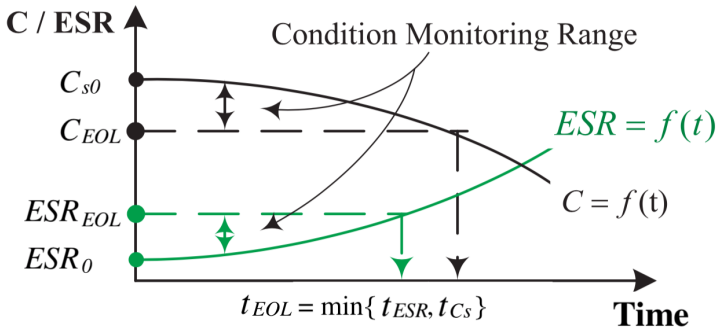


Fig. 3.11 Indicators condition monitoring range [50] and EOL spot determination.

For Al-Elec capacitors, according to the relationship between electrolyte volume loss deteriorated by evaporation and actual available capacitance [51], a 20% capacitance drop or 2.8~3 times of ESR_0 are treated as the thresholds. For MF capacitors, maximum tolerance of capacitance reduction is 5%, the criterion for ESR follows Al-Elec capacitors as a rule of thumb [50,52].

A. Hayek etc. in [35] delivered a 3200 h accelerated aging for a cluster of electrolytic capacitors under 50 °C temperature, 500 V applied voltage and 2.3 A (120 Hz) ripple current condition, a cubic approximation DM model is used to match the experimental data whose universal form is:

$$C_s(t), ESR(t) = a + bt + ct^2 + dt^3 \tag{3.19}$$

where a, b, c, d are parameters that need to be acquired from experiment data.

Hua Li etc. in [38] tested 25 MPPF capacitors in a high-humidity, high-temperature environment for 1000 h, which showed C_s and ESR performed linear variation at initial stage and behaved faster decrease due to moisture penetration after transition time point, DM models for these two indicators can be fitted as:

$$\begin{cases} \dfrac{\Delta C_s(t)}{C_{s0}} = \begin{cases} at & t \le t_1 \\ m(t-t_1)^n & t > t_1 \end{cases} \\ \dfrac{ESR(t)}{ESR_0} = \begin{cases} 1+bt & t \le t_2 \\ 1+p(t-t_2)^q & t > t_2 \end{cases} \end{cases} \tag{3.20}$$

where a, b, m, n, p, q are constant parameters, t_1, t_2 are two ingress time points specified for C_s and ESR respectively.

C. Integrated Methods

Making use of both PE and DM methods, instead of obtaining data to fit the changing curves, integrated methods exploit the change of C_s and ESR in detailed expression upon principal understandings of capacitor materials. The base values of those two indicators are

derived from capacitors' structural, electrochemical or geometrical nature, while the acquisition of wear-out characteristics still relies on experiment data.

Here follows an example in which a kind of electrolytic capacitor with ethyl glycol along with trialkyl amines and carboxylic acid as electrolyte is tested [53]. The initial value of ESR is assumed equal to electrolyte resistance and is related on effective area of oxide layer:

$$ESR_0 = \frac{1}{2}\left(\frac{\rho_E d_C P_E}{A_S}\right) \tag{3.21}$$

where ρ_E is electrolyte resistivity, d_C is oxide layer thickness, P_E is correlation factor, A_S effective oxide layer area of the capacitor. The modelling of C_{s0} is based on geometrical analysis and can be computed as:

$$C_{S0} = \frac{2\epsilon_R \epsilon_0 A_S}{d_C} \tag{3.22}$$

where ϵ_R is relative dielectric constant, ϵ_0 is free space permittivity.

Then the data-driven models can be determined as:

$$\begin{cases} ESR(t) = \frac{1}{2}(\rho_E d_C P_E)\left(\frac{j_{eo} \cdot w_e \cdot t}{V_{e0} - V_e(t)}\right) \\ C_S(t) = \left(\frac{2\epsilon_R \epsilon_0}{d_C}\right)\left(\frac{V_{e0} - V_e(t)}{j_{eo} \cdot w_e \cdot t}\right) \end{cases} \tag{3.23}$$

where j_{eo} is the rate of evaporation treated as a constant in fixed ambient temperature, w_e is ethyl glycol volume, $V_e(t)$ is real-time dispersion volume, V_{e0} is initial electrolyte volume which is calculated as:

$$V_{e0} = \pi r_C^2 h_C - A_S(d_A + d_C) \tag{3.24}$$

where r_C, h_C are radius and height of capacitor, d_A, d_C are thicknesses of anode oxide layer and cathode oxide layer respectively.

The accelerated thermal aging experiment collected data which were used for estimating parameter and enforcing clarification upon the model, in which losing volume of electrolyte was predicted by a second-order polynomial function.

3.6 Summary

This chapter listed two types of capacitors that can be used as candidates for dc-link power capacitors in a regen CHB motor drive: aluminum electrolytic (Al-Elec) capacitors and metallized polypropylene film (MPPF) capacitors. Basic structures, main components and some characteristics of them were introduced. Pros and cons were discussed as well. Al-Elec capacitors have high available capacitance range, moderate voltage ratings and operating temperature limits, as well as excellent unit price/performance ratio. However, having reliability issues such as electrolyte evaporation and capacitance drift under higher temperature, the actual lifetime expectancy is relatively lower than MPPF power capacitors. Thanks to smaller dissipation factors, MPPF capacitors have less generated thermal loss when being applied with same ripple currents as Al-Elec capacitors, they can bear more temperature stress taking advantage of their solid structures.

Four typical behavior (reliability) influence factors: applied voltage, ripple current, core temperature and humidity were outlined and analyzed, these factors are common stresses that a dc-link power capacitor might face during the actual operation of a regen CHB motor drive.

Failure classification of dc-link power capacitors were presented as a framework to deliver reliability analysis. The circuit modelling for dc-link power capacitors and calculation for corresponding circuit parameters which can be used as reliability indicators were delivered. Finally, two reliability analysis methodologies: physics-based estimation (PE) and data-driven monitoring (DM) were introduced, as well as integrated methods that combines these two techniques. Some existing models were presented as references.

PE methods can find use in chapter 4 as proposed lifetime models for regen CHB motor drives' dc-link power capacitors.

Chapter 4

Reliability Analysis and Proposed Lifetime Model for DC-link Power Capacitors

When designing the capacitor banks for a regen CHB motor drive, the forecast of estimated useful lifetime of dc-link power capacitor unit, instead of monitoring real-time state of health, is a critical criterion to predict the overall reliability of power cells, as well as of the motor drive itself. Therefore, physics-based estimation (PE) methodology will be introduced in this chapter to propose a lifetime model for dc-link power capacitors in a regen CHB motor drive.

4.1 Behavior (Reliability) Stresses Modelling

Due to high-coupled characteristics of those aforementioned capacitor behavior stresses, in respects of material structure, electrochemistry and thermodynamics, degradation of capacitors' parameters such as wear-out on capacitance, internal resistance,

dielectric resistance etc. are sophisticated to be analyzed.

Two PE-based modelling methods can be used for expressing the reaction rates of reliability stresses in dc-link power capacitor reliability analysis: Arrhenius law and inverse power law. The Arrhenius law can takes care of thermal depends in physical chemistry. Therefore, ripple currents and ambient temperature stress factors that influence the core temperature (CT) of a dc-link power capacitor, should be taken care by Arrhenius law in analysis. The inverse-power law is commonly used for non-thermal depends on the contrary. For applied voltage and humidity, inverse-power law will be introduced to express the effects of theirs.

4.1.1 Thermal Stress Factor Based on Arrhenius Law

As a PE model, Arrhenius law uncovers the thermal-produced reaction mechanisms in physical chemistry, which shows the relationship between reaction rates and temperature stresses. This impacts capacitor reliability in thermal point of view.

The original equation of temperature-dependent Arrhenius law can be expressed as [54]:

$$\lambda(T) = Ae^{\frac{-E_a}{k_B T}} \tag{4.1}$$

where λ is the reaction rate, E_a is activation energy for reaction [eV], k_B is the Boltzmann constant, which is defined as 8.617e-5 eV/K, T is the thermodynamic temperature of reaction [K], A is a pre-exponential constant for every reaction.

Assuming an inversely proportional relationship holds good for capacitor reliability, or in other words, EUL and reaction rate. Which means higher the reaction rate, lower the EUL. Then the expression of EUL can be derived as:

$$EUL = \frac{\lambda(T^*)}{\lambda(T_a)} \cdot L^* \tag{4.2}$$

where T^* is the nominal temperature content [K], L^* is the base useful lifetime of a capacitor defined under nominal condition, T_a is applied thermodynamic temperature content which can be specified to ambient temperature or ripple-current-caused core temperature. Assigning Eq. (4.1) to Eq. (4.2):

$$\begin{aligned} EUL &= \frac{Ae^{\frac{-E_a}{k_B T^*}}}{Ae^{\frac{-E_a}{k_B T_a}}} \cdot L^* \\ &= exp\left(\frac{E_a}{k_B}\left(\frac{1}{T_a} - \frac{1}{T^*}\right)\right) \cdot L^* \end{aligned} \tag{4.3}$$

Then a thermal stress factor K_{th} can be introduced to estimate the thermal-dependent lifetime variation:

$$K_{th}(T_a) = exp\left(\frac{E_a}{k_B}\left(\frac{1}{T_a} - \frac{1}{T^*}\right)\right) \tag{4.4}$$

Notice that if T^* in Eq.(4.4) is aligned with a category maximum temperature content of a dc-link power capacitor, then $T_a \leq T^*$, $K_T \geq 1$, the stress factor can be used as a multiplier to prolong the capacitor's EUL on actual temperature conditions compared with basic useful lifetime on the harshest temperature condition.

The derivations of ripple current stress and ambient temperature stress for Al-Elec

capacitors and MPPF capacitors will be explained based on Arrhenius law in the following:

4.1.1.1 Derivation of Ripple Current Stress Factor

Thermal stress factor K_{th} builds a direct connection between EUL and thermal stresses. For ripple current reliability stress, based on Arrhenius law, K_{th} indicates the influence of actual CTR originating from in-operation ripple currents on capacitor reliability issue by building the connection of it with category nominal CTR specified by capacitor manufacturers.

Then the expression of CT can be given as:

$$T_{core} = \Delta T_{core} + T_{amb} \tag{4.5}$$

$$T_{core}^{*} = \Delta T_{core}^{*} + T_{amb} \tag{4.6}$$

where ΔT_{core}, T_{core} are actual CTR [K] and CT [K] in a given T_{amb}, ΔT_{core}^{*},and T_{core}^{*} is category nominal CTR [K] and CT [K] in a given T_{amb}.

Therefore, Eq. (4.4) can be rewritten as:

$$\begin{aligned} K_{RC}(\Delta T_{core}) &= \exp\left(\frac{E_a}{k_B}\left(\frac{1}{T_{core}} - \frac{1}{T_{core}^{*}}\right)\right) \\ &= \exp\left(\frac{E_a}{k_B}\left(\frac{1}{\Delta T_{core} + T_{amb}} - \frac{1}{\Delta T_{core}^{*} + T_{amb}}\right)\right) \end{aligned} \tag{4.7}$$

A. Al-Elec Power Capacitors

Recalling the CTR function regarding ripple current for Al-Elec capacitors:

$$\Delta T_{core} = \left(\frac{I_r}{I_r^{*}}\right)^2 \cdot \Delta T_{core}^{*} \tag{4.8}$$

Then the ripple current stress factor assigned for Al-Elec power capacitors can be expressed by combining Eq. (4.7) and Eq. (4.8):

$$K_{RC,Al-Elec}(I_r) = \exp\left(\frac{E_a}{k_B}\left(\frac{1}{\left(\frac{I_r}{I_r^*}\right)^2 \Delta T_{core}^* + T_{amb}} - \frac{1}{\Delta T_{core}^* + T_{amb}}\right)\right)$$
$$= \exp\left(\frac{E_a}{k_B}\left(\frac{I_r^{*2}}{{I_r}^2 \Delta T_{core}^* + I_r^{*2} T_{amb}} - \frac{1}{\Delta T_{core}^* + T_{amb}}\right)\right) \quad (4.9)$$

The activation energy E_a for aluminum oxide usually is 0.94 eV [55], then Eq. (4.9) can be derived as:

$$K_{RC,Al-Elec}(I_r) = \exp\left(10908.7\left(\frac{I_r^{*2}}{{I_r}^2 \Delta T_{core}^* + I_r^{*2} T_{amb}} - \frac{1}{\Delta T_{core}^* + T_{amb}}\right)\right) \quad (4.10)$$

Fig. 4.1.1 shows ripple current stress factor curves for 3 Al-Elec power capacitor products that are available in the manufacturers' brochure when the ambient temperature is 40 ℃. The corresponding information and ratings for them are listed in Table 4.1.1.

TABLE 4.1.1 RIPPLE CURRENT RATINGS FOR THREE AL-ELEC POWER CAPACITORS

Manufacturer	**MPNs**	**Unit Capacitance (μF)**	**I_r^* on 85 ℃, 120 Hz (Arms)**	**ΔT_{core}^* (℃/K)**
Jianghai	ECS2GQL182MVB350090V	1800	7.3	7.5/280.65
Hitachi	PL12G182QSBS17WPEC	1800	6.37	10/283.15
	PL12W132QSBS17WPEC	1300	5.41	10/283.15

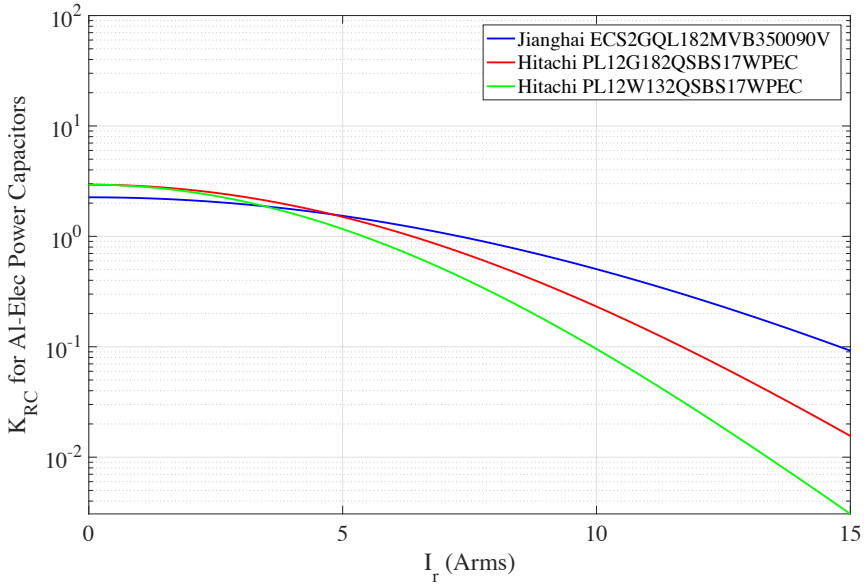


Fig. 4.1.1 Ripple current stress factor curves for 3 Al-Elec power capacitors.

It can be seen that the trajectories of $K_{RC,Al-Elec}$ are degressive with a faster speed when actual equivalent ripple current I_r increases, showing the lifetime degradation. If $I_r > I_r^*$, $K_{RC,Al-Elec} < 1.0$, a vulnerable EUL compared with L^* can be expected, vice versa.

B. MPPF Power Capacitors

Recalling the CTR function regarding ripple current for MPPF capacitors here:

$$\Delta T_{core} = \left({I_r}^2 \cdot ESR\right) \cdot R_{th} \tag{4.11}$$

$$\Delta T_{core}^* = \left(I_r^{*2} \cdot ESR\right) \cdot R_{th} \tag{4.12}$$

Then the ripple current stress factor assigned for MPPF power capacitors can be expressed by combining Eq. (4.7) and Eq. (4.11):

$$K_{RC,MPPF}(I_r) = \exp\left(\frac{E_a}{k_B}\left(\frac{1}{{I_r}^2 ESR \cdot R_{th} + T_{amb}} - \frac{1}{I_r^{*2} ESR \cdot R_{th} + T_{amb}}\right)\right) \quad (4.13)$$

The activation energy E_a for PP polymer film diverse from 0.6~1.7 eV due to different technological processes [56,57] , meaning:

$$K_{RC,MPPF}(I_r) = \exp\left(7k\sim 20k\left(\frac{1}{{I_r}^2 ESR \cdot R_{th} + T_{amb}} - \frac{1}{I_r^{*2} ESR \cdot R_{th} + T_{amb}}\right)\right) \quad (4.14)$$

Fig. 4.1.2 presents ripple current stress factor curves for 3 MPPF power capacitor products that are available in the manufacturers' brochure. The corresponding information and ratings are listed in Table 4.1.2.

It can be noticed that even though MPPF power capacitors ripple current stress factors $K_{RC,MPPF}$ perform similar characteristics with those for Al-Elec capacitors, but due to their significantly higher ripple current ratings, $K_{RC,MPPF} > 1$ it can be expected in a much wider range of actual ripple currents, and better reliability performances would be anticipated compared with Al-Elec power capacitor.

TABLE 4.1.2 RIPPLE CURRENT RATINGS FOR THREE MPPF POWER CAPACITORS

Manufacturer	**MPNs**	**Unit Capacitance (μF)**	$\frac{E_a}{k_B}$	I_r^* **on 1k~10k Hz (Arms)**	ESR **(mΩ)**	R_{th} **(K/W)**
Jianghai	FCC03DL107*H09503*	800	10800	92(40℃)	1.5	2.7
Hitachi	MLC1300V138KB140225	1300	12000	72(50℃)	1.6	2.4
	MLC1300V907KB116225	900	12000	69(50℃)	2.1	2.0

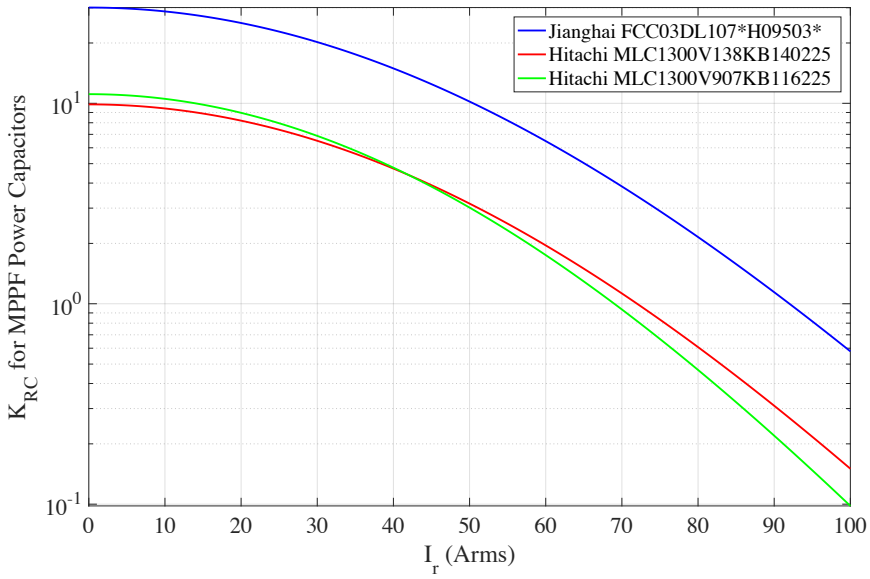


Fig. 4.1.2 Ripple current stress factor curves for 3 MPPF power capacitors.

4.1.1.2 Derivation of Ambient Temperature Stress Factor

K_{th} reveals the impact from the actual temperature of the ambient environment to which capacitors are devoted. Assuming the correlation of actual temperature with a nominal maximum operating ambient temperature that a capacitor can endure, then Eq. (4.4) can be rewritten as:

$$K_{T_{amb}}(T_{amb}) = \exp\left(\frac{E_a}{k_B}\left(\frac{1}{T_{amb}} - \frac{1}{T^*_{amb}}\right)\right) \tag{4.15}$$

where T_{amb} is actual ambient temperature [K], T^*_{amb} is nominal maximum ambient temperature [K].

A. Al-Elec Power Capacitors

Similarly, the ambient temperature stress factor for Al-Elec power capacitor can be

presented as:

$$K_{T_{amb},Al-Elec}(T_{amb}) = \exp\left(10908.7\left(\frac{1}{T_{amb}} - \frac{1}{T^*_{amb}}\right)\right) \tag{4.16}$$

Eq. (4.16) is a normal form of Al-Elec capacitor ambient temperature stress factor, which can be rearranged as:

$$K_{T_{amb},Al-Elec}(T_{amb}) = \exp\left(10908.7\left(\frac{\tau}{T_{amb}\cdot T^*_{amb}}\right)\right) \tag{4.17}$$

in which $\tau = T^*_{amb} - T_{amb}$ [K].

If we set the maximum temperature T^*_{amb}, as a common value for commercial Al-Elec power capacitor products in the market, 125°C (398 K) and assume $T_{amb}\cdot T^*_{amb} \cong {T^*_{amb}}^2$, then a rule of thumb that widely accepted in industry can be formed as:

$$K_{T_{amb},Al-Elec}(\tau) = \exp\left(\frac{109087}{398^2}\cdot\frac{\tau}{10}\right) \cong \exp\left(\ln 2\cdot\frac{\tau}{10}\right) = 2^{\tau/10} \tag{4.18}$$

Eq. (4.15) establishes the change of ambient temperature stress factor along with every 10°C difference between T_{amb} and T^*_{amb}, known as "10-kelvin Rule of Thumb".

Two Al-Elec power capacitor products from two capacitor manufacturers with different T^*_{amb} ratings are listed in Table. 4.1.3. Fig. 4.1.3 shows corresponding "10-kelvin Rule" $K_{T_{amb},Al-Elec}$ curves for them.

TABLE 4.1.3 AMBIENT TEMPERATURE RATINGS FOR TWO AL-ELEC POWER CAPACITORS

Manufacturer	**MPNs**	**Unit Capacitance (μF)**	$\boldsymbol{T^*_{amb}}$ **(°C)**
UCC	ELXR351LGC332MDB5U	3300	105
Jianghai	ECS2GQL182MVB350090V	1800	85

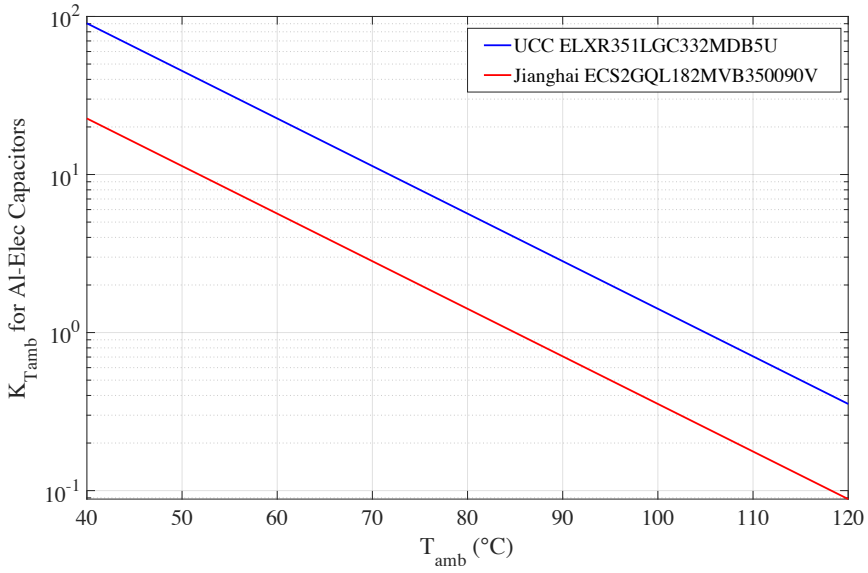


Fig. 4.1.3 Ambient temperature stress factor curves for 2 Al-Elec power capacitors.

B. MPPF Power Capacitors

In the same way, the ambient temperature stress factor for MPPF power capacitor can be presented as:

$$K_{T_{amb},MPPF}(T_{amb}) = \exp\left(7k{\sim}20k\left(\frac{1}{T_{amb}} - \frac{1}{T^*_{amb}}\right)\right) \tag{4.19}$$

Three MPPC power capacitor examples from three capacitor manufacturers with different T^*_{amb} ratings are listed in Table. 4.1.4. Fig. 4.1.4 shows $K_{T_{amb},MPPF}$ curves.

TABLE 4.1.4 AMBIENT TEMPERATURE RATINGS FOR THREE MPPF POWER CAPACITORS

Manufacturer	**MPNs**	**Unit Capacitance (μF)**	$\boldsymbol{\frac{E_a}{k_B}}$	$\boldsymbol{T^*_{amb}}$ **(°C)**
Jianghai	FCC03DL107*H09503*	800	10800	85
Hitachi	MLC1300V138KB140225	1300	12000	80
ICAR	LNK-M3-1-1900-130	1900	8100	75

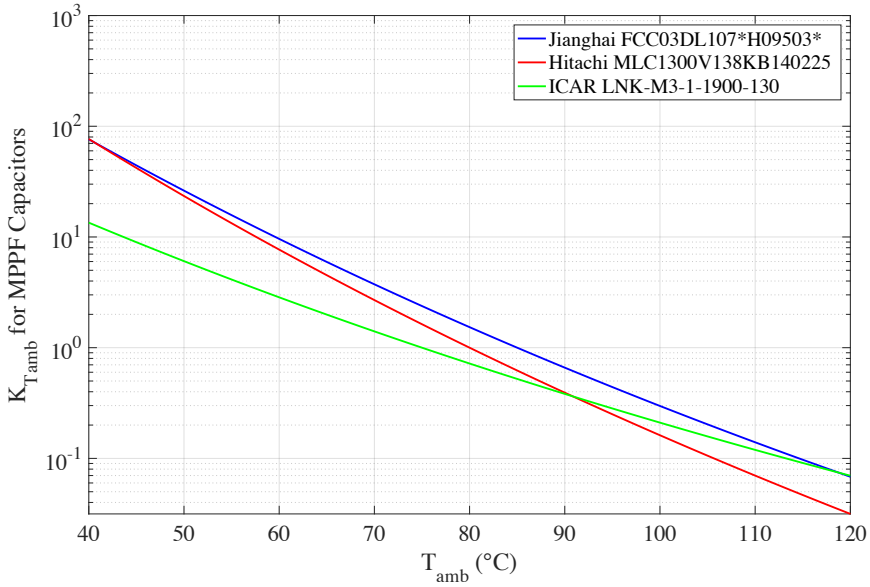


Fig. 4.1.4 Ambient temperature stress factor curves for 3 MPPF power capacitors.

4.1.2 Non-thermal Stress Factor Based on Inverse Power Law

A stress estimation model built with the help of inverse power law (IPL) denotes attributes of non-thermal stress factors and is commonly implemented in accelerated testing and reliability analysis [58,59].

The normal form of IPL model can be given as:

$$L(N) = EUL = \frac{1}{B \cdot N^{\alpha}} \tag{4.20}$$

where L indicates a quantitative life representative, here EUL is assigned for L in capacitor reliability estimation. B is a pre-defined positive scaler for different stress model, N represents the stress level of any non-thermal influence on the overall EUL, α is another model parameter to be determined which acts as the exponent in IPL.

If the IPL as Eq. (4.20) is reformed into a log-log expression, which is shown as:

$$\ln(EUL) = -\ln(B) - \alpha \cdot \ln(N) \tag{4.21}$$

It is apparent that the shape of log-log IPL is a linear plot. The derivation of B and α can be achieved by calculating the intercept and slope.

Model parameter α explains how intense the applied non-thermal stresses can effect EUL. Because all the possible stresses for power capacitors in a regen CHB motor drive inflict harm on capacitors' lifetime, so $\alpha > 0$ is used to indicate a negative slope for injured EUL in reality.

Similar to thermal stresses, a non-thermal stress factor K_{non-th} can be introduced to estimate the non-thermal-dependent lifetime variation:

$$K_{non-th}(N_a) = \frac{EUL}{L^*} = \frac{\frac{1}{B \cdot {N_a}^{\alpha}}}{\frac{1}{B \cdot {N^*}^{\alpha}}} = \left(\frac{N_a}{N^*}\right)^{-\alpha} \tag{4.22}$$

Again, L^* is the base useful lifetime of a capacitor defined under nominal condition. N_a is the applied non-thermal stress level, N^* is the nominal non-thermal stress level, which usually represents the maximum voltage that can be constantly applied upon a capacitor.

$N_a \leq N^*$ comes into existence in actual operating conditions as a safety margin. Therefore, $K_{non-th} \geq 1$ is a practical criterion showing a potential lifetime extension under actual operations compared with the most rigorous condition.

Eq. (4.22) shows an inversed power relationship between applied stress and nominal

stress. Applied voltage and humidity, as two non-thermal stress elements that involved in this thesis, stress factors for them will be analyzed by utilizing IPL model with the form of Eq. (4.22).

4.1.2.1 Derivation of Applied Voltage Stress Factor

Inspired by Eq. (4.22), stress factor for applied voltage for power capacitors in a regen CHB motor drive can be expressed as:

$$K_{V_a}(V_a) = \left(\frac{V_a}{V^*}\right)^{-\alpha_{V_a}} \tag{4.23}$$

where V_a, V^* are actual applied voltage and nominal rated voltage. Note that the designed voltage ratings for power capacitors are dc values, therefore rms values of V_a need to be determined for unit aligning. α_{V_a} is exponent parameter specified for applied voltage.

Stress factor in Eq. (4.23) has no principal modeling parameters involved, which means power capacitor categories will not influence the form of stress factor.

A. Al-Elec Power Capacitors

Applied voltage stress factor for Al-Elec power capacitor, $K_{V_a,Al-Elec}$, can be simply given by:

$$K_{V_a,Al-Elec}(V_a) = \left(\frac{V_a}{V^*}\right)^{-\alpha_{V_a,Al-Elec}} \tag{4.24}$$

in which $\alpha_{V_a,Al-Elec}$ is α_{V_a} for Al-Elec power capacitors. Some Al-Elec power capacitor manufacturers have unique description and distribution of this exponent parameter,

especially for some large companies.

For example, Jianghai Capacitor Co., Ltd provides self-defined distribution of $\alpha_{V_a,Al-Elec}$ for snap-in and screw-terminal types of Al-Elec power capacitors with medium and large sizes [60], which is shown as:

$$\alpha_{V_a,Al-Elec} = \begin{cases} 1, & \frac{V_a}{V^*} < 0.5 \\ 3, & 0.5 \leq \frac{V_a}{V^*} < 0.8 \\ 5, & 0.8 \leq \frac{V_a}{V^*} \leq 1 \end{cases} \tag{4.25}$$

Hitachi AIC Inc. utilizes a constant $\alpha_{V_a,Al-Elec}$ for Al-Elec power capacitors in medium-to-high voltage applications, but with an auxiliary restriction of applied voltage level [61]:

$$\alpha_{V_a,Al-Elec} = 2.5 \tag{4.26}$$

$$if\ \frac{V_a}{V^*} < 0.6,\ \ \frac{V_a}{V^*} = 0.6 \tag{4.27}$$

United Chemi-Con (UCC) claims that $\alpha_{V_a,Al-Elec} = 0$ for their capacitors used at or below rated voltages [62], which means $K_{V_a,Al-Elec} = 1$.

Three Al-Elec power capacitor products from the mentioned manufacturers are used as examples to illustrate diagrams of $K_{V_a,Al-Elec}$ as shown in Fig. 4.1.5, corresponding ratings for those capacitors are displayed in Table 4.1.5.

TABLE 4.1.5 APPLIED VOLTAGE RATINGS FOR THREE AL-ELEC POWER CAPACITORS

Manufacturer	**MPNs**	**Unit Capacitance (μF)**	V^***(Vdc)**
Jianghai	ECS2GQL182MVB350090V	1800	400
Hitachi	PL12W132QSBS17WPEC	1300	450
UCC	E37L501CPN682MFF5U	6800	500

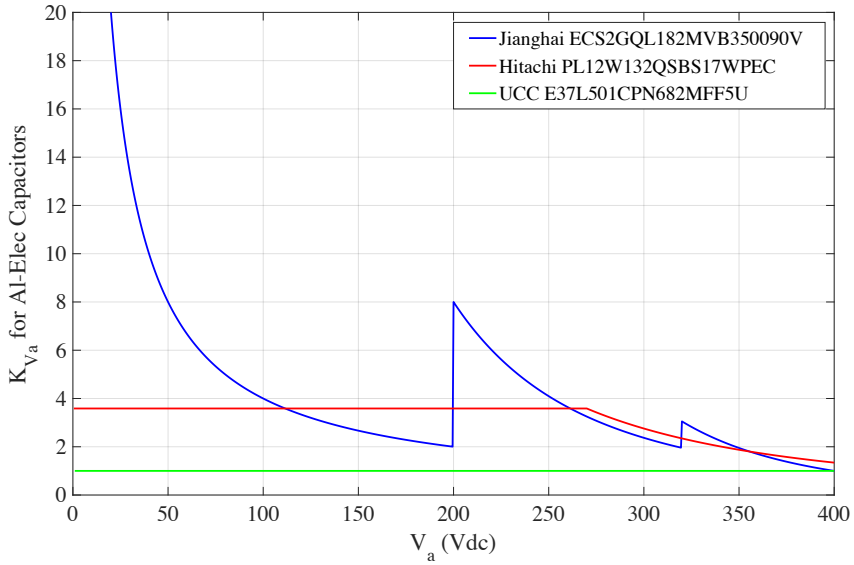


Fig. 4.1.5 Applied voltage stress factor curves for 3 Al-Elec power capacitors.

It is obvious that the $K_{V_a,Al-Elec}$ curves of capacitor samples from Jianghai and Hitachi shows partition features, from which we can assume the Al-Elec power capacitor with high voltage ratings wouldn't behave a sharp decrease on $K_{V_a,Al-Elec}$ along with increasing V_a. UCC's capacitor example hypothesizes that as long as $V_a \leq V^*$, the reliability impact from V_a can be neglected.

B. MPPF Power Capacitors

In the same way, applied voltage stress factor for MPPF power capacitor, $K_{V_a,MPPF}$, can be expressed as:

$$K_{V_a,MPPF}(V_a) = \left(\frac{V_a}{V^*}\right)^{-\alpha_{V_a,MPPF}} \tag{4.28}$$

where $\alpha_{V_a,MPPF}$ is α_{V_a} for MPPF power capacitors, which is also a statistics-oriented parameter decided dissimilarly between manufacturers.

$\alpha_{V_a,MPPF}$ varies from 7 to 12 in some leading capacitor manufacturers [63], while some companies might use other values, $\alpha_{V_a,MPPF}$ is usually bigger than $\alpha_{V_a,Al-Elec}$ for most existing power capacitor products.

Three MPPF power capacitors are listed in Table 4.1.6 for showing different $K_{V_a,MPPF}$ characteristics, which are presented in Fig. 4.1.6.

For Jianghai's MPPF capacitor, $\alpha_{V_a,MPPF} = 11.7$ is used, Hitachi introduces a $\alpha_{V_a,MPPF} = 11.6$ and restriction of applied voltage level in Eq. (4.27) works for MPPF capacitors, $\alpha_{V_a,MPPF} = 8$ is set for ICAR.

As Fig. 4.1.6 shows, MPPF capacitor products with higher $\alpha_{V_a,MPPF}$ have a bigger $K_{V_a,MPPF}$ compared with those have smaller $\alpha_{V_a,MPPF}$ under the same V_a, meaning a longer *EUL* can be expected under a specified applied voltage condition. Nevertheless, higher $\alpha_{V_a,MPPF}$ demonstrates a more rapid decaying rate as V_a increases, showing a more voltage-vulnerable feature.

TABLE 4.1.6 APPLIED VOLTAGE RATINGS FOR THREE MPPF POWER CAPACITORS

Manufacturer	**MPNs**	**Unit Capacitance (μF)**	V^***(Vdc)**
Jianghai	FCC03DL107*H09503*	800	1300
Hitachi	MLC1300V138KB140225	1300	1300
ICAR	LNK-M3-1-1900-130	1900	1300

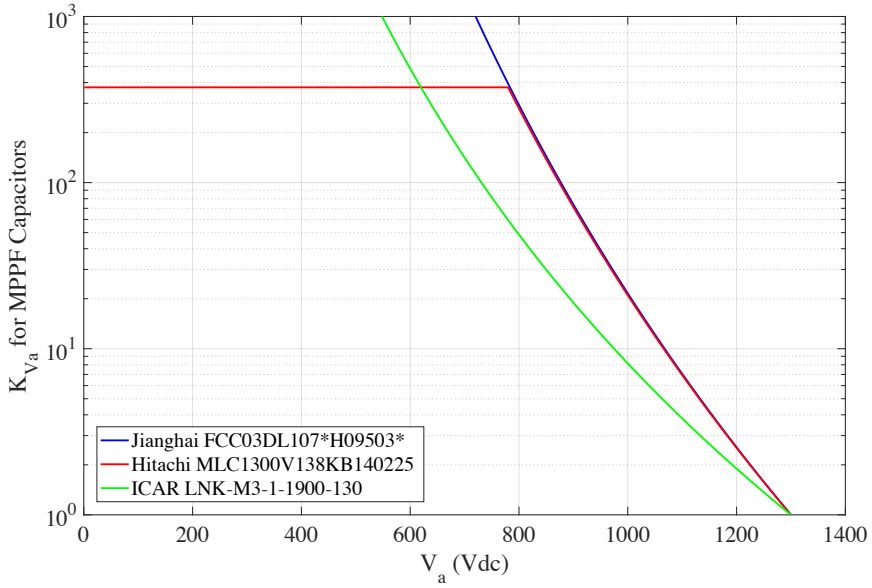


Fig. 4.1.6 Applied voltage stress factor curves for 3 MPPF power capacitors.

4.1.2.2 Derivation of Humidity Stress Factor

Researchers in [64-66] had some insights on integrating RH with IPL in doing lifetime analysis for some given materials.

But as a less critical stress factor in dc-link power capacitor applications, humidity stress factor K_{RH} is treated as a subordinate lifetime influencer with smaller α. That's because power capacitor products for industrial uses are generally equipped with enclosed capsulation which have adequate ingress protection (IP) ratings for humidity.

Influence from K_{RH} might be neglected under most ordinary humid circumstances, especially when a basic UL is not determined under a specified humidity condition by manufacturers. So in this thesis, only $RH_a \geq RH^*$ will be considered as a watershed to define K_{RH} can do harm to capacitors' lifetime, for any environment that $RH_a < RH^*$, $K_{RH} = 1$.

Then expression of K_{RH} is written as:

$$K_{RH}(RH_a) = \begin{cases} 1 & , RH_a < RH^* \\ \left(\frac{RH_a}{RH^*}\right)^{-\alpha_{RH}} & , RH_a \geq RH^* \end{cases} \tag{4.29}$$

In which RH_a, RH^* are actual RH and nominal RH of a dc-link power capacitor, α_{RH} is IPL exponent for RH.

Generally, there is no precise ratings for RH^* that provided by manufacturers, but recommended RH level for storage can be used as a replacer of RH^*, which is 80% for Al-Elec power capacitors, 75% for MPPF power capacitors.

A. Al-Elec Power Capacitors

Humidity stress factor for Al-Elec power capacitors is expressed as:

$$K_{RH,Al-Elec}(RH_a) = \begin{cases} 1 & , RH_a < RH^* \\ \left(\frac{RH_a}{RH^*}\right)^{-\alpha_{RH,Al-Elec}} & , RH_a \geq RH^* \end{cases} \tag{4.30}$$

[64] delivered extrapolation of $\alpha_{RH,Al-Elec}$ for aluminum metallization that suffered corrosion caused by humidity. Researchers claimed 2.5~3.0 can be an estimated range for $\alpha_{RH,Al-Elec}$.

Fig. 4.1.7 presents diagrams for derivation of $K_{RH,MPPF}$ based on Eq. (4.30) with an aforementioned range of $\alpha_{RH,MPPF}$.

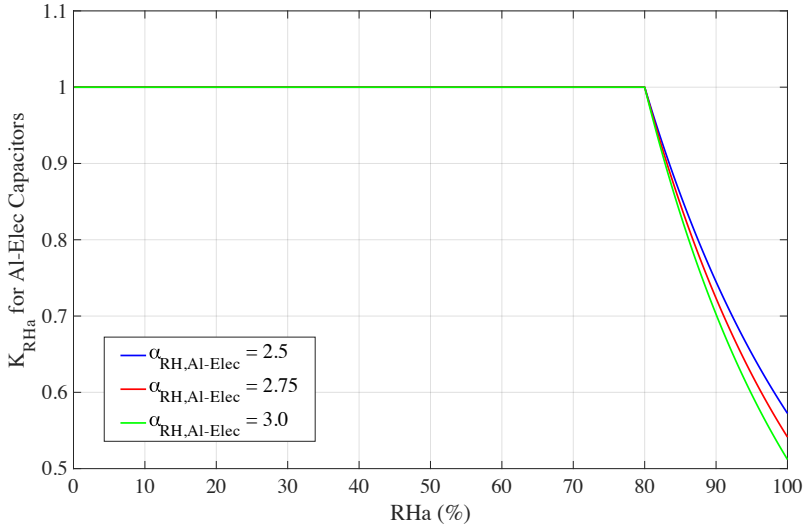


Fig. 4.1.7 Humidity stress factor curves for different $\alpha_{RH,Al-Elec}$.

B. MPPF Power Capacitors

Humidity stress factor for MPPF power capacitors is given as:

$$K_{RH,MPPF}(RH_a) = \begin{cases} 1 & , RH_a < RH^* \\ \left(\frac{RH_a}{RH^*}\right)^{-\alpha_{RH,MPPF}} & , RH_a \geq RH^* \end{cases} \tag{4.31}$$

In [45] 3 groups of metallized film capacitors were used as testing samples under different RH conditions and same ambient temperature, $\alpha_{RH,MPPF}$ vary from 1.8 to 2.3 were obtained.

Fig. 4.1.8 shows the corresponding $K_{RH,MPPF}$ curves derived from Eq. (4.31), with varying range of $\alpha_{RH,MPPF}$.

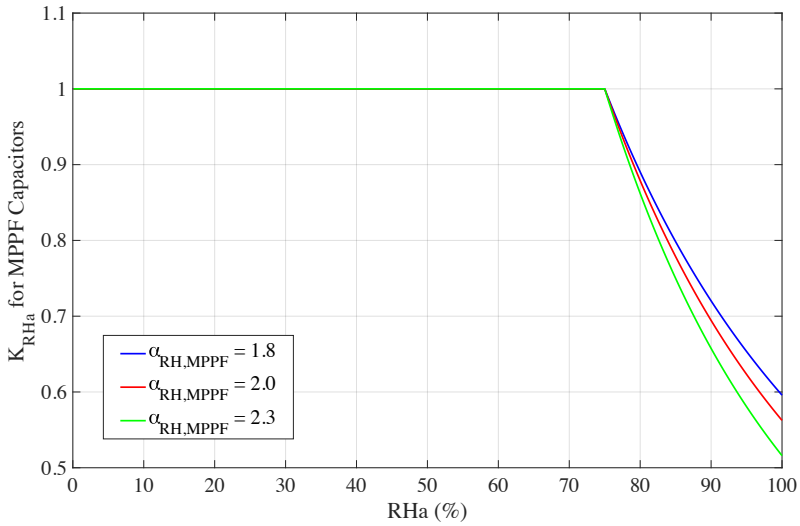


Fig. 4.1.8 Humidity stress factor curves for different $\alpha_{RH,MPPF}$.

4.2 Reliability Concepts for DC-link Power Capacitors

It has always been capacitor manufacturers' target to make full use of highest accessible efficiency of their power capacitor products, which takes longer lifetime and energy dissipation into consideration. From reliability's point of view, a longer lifetime means a better reliability, indicating a possibility that capacitors hold effectivity at a given time before a failure happens. The failures can be caused by all the mentioned reliability stresses in Chapter 3. Some concepts have been defined by researchers to evaluate the relationship between failure and reliability, such as failure rate or failure in time (FIT), mean time to failure (MTTF), mean time to repair (MTTR), mean time between failure (MTBF), and availability which will be discussed in following contents:

4.2.1 Failure Rate

Failure rate, λ, of power capacitors shows the frequency which a power capacitor fails, usually expressed in number of failure occurrence per unit of time. FIT is defined as a failure rate that presents while a billion hours, which means:

$$FIT = 1\ Failure/10^9\ hours \tag{4.32}$$

λ can be defined as the probability that a failure occurs in a time-domain interval $(t, t+\Delta t]$, when no failure happens before time t, which can be described as [67] (p. 52):

$$\lambda = \frac{P(A|B)}{\Delta t} = \frac{P(A)}{\Delta t \cdot P(B)} \tag{4.33}$$

where $A = t < T \leq t + \Delta t$, $B = T > t$. $P(A)$ indicates the failure probability of a time spot T in interval $(t, t+\Delta t]$, $P(B)$ indicates the probability that failures sorely happen after t $(T > t)$.

Let's introduce cumulative distribution function (CDF) for failure as failure distribution $F(t)$. $F(t)$ describes the probability of failure until time t. Then an attribute can be obtained:

$$P(T \leq t) = F(t) = 1 - R(t), \quad t \geq 0 \tag{4.34}$$

where $R(t)$ is reliability distribution representing that non-appearance of failure, then $F(t)$ can be defined as the difference between the sum of all possible events (=1) and $R(t)$.

Another formula is derived as Eq. (4.35) if the probability density function (PDF) for $F(t)$ is defined as failure density function $f(t)$. This is because CDF of a continuous random variable can be treated as the integral of its PDF:

$$P(t < T \leq t + \Delta t) = F(t + \Delta t) - F(t) = \int_{t}^{t+\Delta t} f(\tau) d\tau \tag{4.35}$$

Then Eq. (4.33) can be rearranged as:

$$\lambda = \frac{R(t) - R(t + \Delta t)}{\Delta t \cdot R(t)} = \frac{\int_{t}^{t+\Delta t} f(\tau) d\tau}{\Delta t \cdot R(t)} \tag{4.36}$$

Assuming Δt is small enough and is close to zero, then the expression of λ is given as:

$$\lambda(t) = \lim_{\Delta t \to 0} \frac{\int_{t}^{t+\Delta t} f(\tau) d\tau}{\Delta t \cdot R(t)} = \frac{f(t)}{R(t)} \tag{4.37}$$

Because $f(t)$ is the mathematical derivative of $F(t)$ thus defines the changes of it with time:

$$f(t) = \frac{dF(t)}{dt} = -\frac{dR(t)}{dt} \tag{4.38}$$

Then Eq. (4.37) can be given as:

$$\lambda(t) = -\frac{dR(t)}{dt} \cdot \frac{1}{R(t)} \tag{4.39}$$

The most widely accepted plot model for failure rate $\lambda(t)$ over time t is the bathtub curve as shown as the blue solid line in Fig. 4.2.1. A typical bathtub consists of three sections with three indications of failure rate: decreasing failure rate, constant failure rate and increasing failure rate; which are contributed by early failures (red dashed line), constant (random) failures (green solid line) and wear out failures (yellow dashed line).

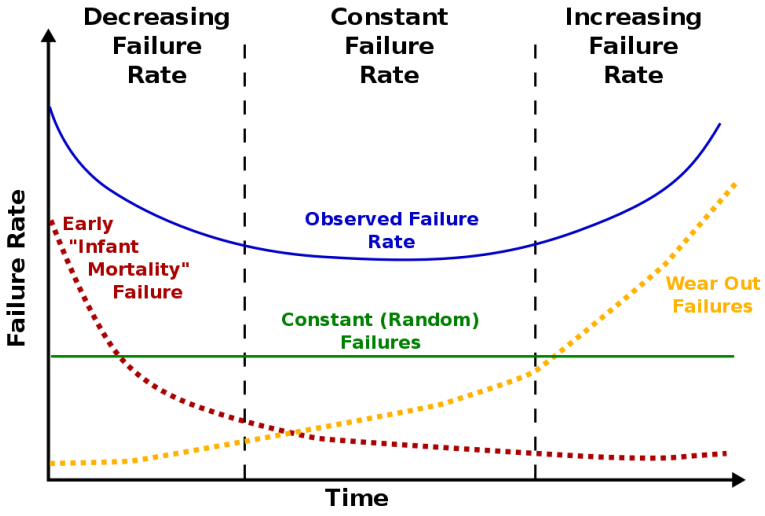


Fig. 4.2.1 Bathtub curve with three failure rate sections [68].

Characteristics of these three sections are summarized as:

Decreasing failure rate section: This section behaves with a decreasing $\lambda(t)$, which is caused by early failures or infant mortality failures. This type of failures are usually led by non-operation defects, such as capacitor manufacturing deficiencies that come from insufficient quality inspection and factory testing. $\lambda(t)$ drops in this section because those power capacitors with less or even none defectives can keep their functions during operations.

Constant failure rate section: This section has a constant $\lambda(t)$, caused by random failures when power capacitor are in operation. These random, or intrinsic failures are caused by superposition of every possible stress factor that a power capacitor might meet. This section is very critical to dc-link power capacitors' reliability analysis since it only

reflect reliability performances on practical actions.

Increasing failure rate section: This section has an increasing $\lambda(t)$, contributed by wear out failures which significantly appear on the EOL period of a power capacitor. These failures are caused by screwed terminals' fatigues, aging of dielectric and electrolyte, metal rustiness etc.

4.2.2 Mean Time to Failure

MTTF represents average time, or mean time of a dc-link power capacitor before the first breakdown failure after the capacitor is in duty. MTTF is a guideline of capacitors' reliability and can be treated as EUL for non-repairable lifetime issues which are caused by in-operation stresses. It is not a guaranteed value that an item must fail after it, or must not fail before it.

MTTF is expressed as the integral of reliability distribution [67] (p. 50) as:

$$MTTF = \int_0^{+\infty} R(t) \cdot dt \tag{4.40}$$

As constant failure rate section will be used in this thesis for reliability analysis, by analyzing of Eq. (4.39), an exponential form of $R(t)$ can be used:

$$R(t) = e^{-\lambda t} \tag{4.41}$$

Then Eq. (4.40) can be given as:

$$MTTF = EUL = \int_0^{+\infty} e^{-\lambda t} \cdot dt = -\frac{1}{\lambda} e^{-\lambda t} \Big|_0^{+\infty} = \frac{1}{\lambda} \tag{4.42}$$

Eq. (4.42) is very important, since it directly express MTTF or EUL as the reciprocal of failure rate, which is a effective connection between these two reliability terms and allows simple conversion between them.

Relationship between MTTF, failure and reliability distribution function with exponential form is shown in Fig. 4.2.2.

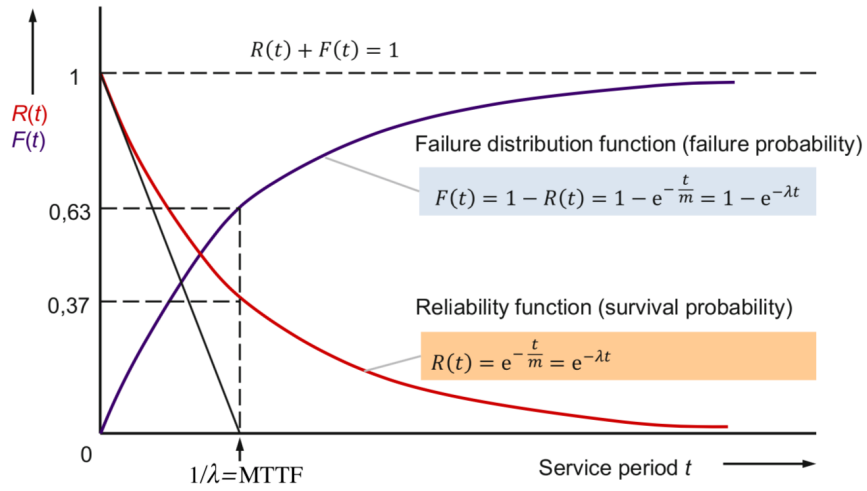


Fig. 4.2.2 MTTF, failure and reliability function with exponential form [67].

One thing that worth a note is, if $t = \frac{1}{\lambda} = MTTF$, assume that corresponding reliability and failure distribution is 0.37 and 0.63 respectively, meaning only 63% of the involved capacitor units might fail at MTTF statistically and 37% of them might still survive at this point. Again emphasizing MTTF or EUL is not a certain criterion to determine practical lifetime of any individual power capacitor.

4.2.3 Mean Time to Repair

MTTR means the average time it takes to resume normal functionality [69] of a failed dc-link power capacitor caused by repairable issues. It is a kind of reliability concept that strongly related with former maintenance states and repairing techniques and operators' proficiency. As an empirics-oriented factor, MTTR is quite sophisticated to be obtained in practice.

4.2.4 Mean Time between Failure

MTBF is a good concept to indicate the reliability performance (MTTF) as well as repair performance (MTTR) of a power capacitor in the same time. It means average time between two successive occurring time spots of failures including required repair duration, defined as Eq. (4.43) for repairable system:

$$MTBT = MTTF + MTTR \tag{4.43}$$

And for non-repairable system:

$$MTBF = MTTF \tag{4.44}$$

4.2.5 Availability

Availability of a power capacitor, A, describes the probability of a capacitor unit that will be in operation with good degree of satisfaction. It is critically based on EUL (MTTF) and maintenance downtimes (MTTR) of a power capacitor, which can be given as [67]:

$$A = \frac{MTTF}{MTTF + MTTR} = \frac{1}{1 + \frac{MTTR}{MTTF}} \tag{4.45}$$

Since a dc-link power capacitor in a regen-CHB motor drive is usually designed for normally operating for thousand hours, and a MTTR is generally counted with a couple of hours in reality. Therefore, $MTTR \ll MTTF$ and can be plugged into Eq. (4.45), then $A \to 1$ holds for most practical circumstances.

An availability close to 1 means the functionality or actual reliability of a power capacitor is not vulnerable for casual repairable failures during operation. It also indicates that EUL can availably reflect capacitors' predicted lifetime, because repairable issues will not pose much threat to capacitors.

In summary, the constant failure rate section in bathtub curve is the most suitable situation to estimate capacitors' reliability in stable operating conditions. An exponential form of reliability distribution function can be used for this phase. MTTF (EUL) is an important reliability concept for regen-CHB motor drive's dc-link power capacitor reliability analysis, that's because the availability of practical power capacitors is very high, meaning capacitor unit takes neglectable impact from repairable failures. EUL is sufficient for describing reliability performance of dc-link power capacitors and this is the guideline for following proposed reliability model in section 4.3.

4.3 Proposed Reliability Model for DC-link Power Capacitors

As discussed in section 4.2, reliability of dc-link power capacitors in a regen-CHB motor drive can be represented by EUL. In this thesis, an EUL model is proposed for reliability analysis of both aluminum electrolytic power capacitors and metallized polypropylene film power capacitors.

4.3.1 Proposed EUL Model

Based on the modelling of those reliability stresses in section 4.1 that dominant on capacitors' reliability performance in real operation, an EUL model for power capacitor can be proposed as:

$$EUL = K_{RC} \cdot K_{T_{amb}} \cdot K_{V_a} \cdot K_{RH} \cdot L^* \tag{4.46}$$

where L^* is base useful lifetime derived on nominal conditions for ripple current, ambient temperature, applied voltage and relative humidity, K_{RC}, $K_{T_{amb}}$, K_{V_a}, K_{RH} are stress factors for those 4 critical reliability stresses, defined by Eq. (4.7), Eq. (4.15), Eq. (4.23), Eq. (4.29) respectively, listed here again:

$$K_{RC}(\Delta T_{core}) = \exp\left(\frac{E_a}{k_B}\left(\frac{1}{T_{core}} - \frac{1}{T_{core}^*}\right)\right)$$

$$= \exp\left(\frac{E_a}{k_B}\left(\frac{1}{\Delta T_{core} + T_{amb}} - \frac{1}{\Delta T_{core}^* + T_{amb}}\right)\right)$$

$$K_{T_{amb}}(T_{amb}) = \exp\left(\frac{E_a}{k_B}\left(\frac{1}{T_{amb}} - \frac{1}{T_{amb}^*}\right)\right)$$

$$K_{V_a}(V_a) = \left(\frac{V_a}{V^*}\right)^{-\alpha_{V_a}}$$

$$K_{RH}(RH_a) = \begin{cases} 1 & , RH_a < RH^* \\ \left(\frac{RH_a}{RH^*}\right)^{-\alpha_{RH}} & , RH_a \geq RH^* \end{cases}$$

Every capacitor product has a theoretical upper limit of its useful lifetime, usually specified by manufacturers. That's because EUL is still a statistical parameter whose value cannot exceed physical cognition, so an important constraint can be set as:

$$EUL \leq UL_{max} \tag{4.47}$$

where UL_{max} represents the theoretical maximum useful lifetime of a power capacitor.

A. Al-Elec Power Capacitors

For Al-Elec power capacitors, proposed EUL model can be given as:

$$EUL_{Al-Elec} = K_{RC,Al-Elec} \cdot K_{T_{amb},Al-Elec} \cdot K_{V_a,Al-Elec} \cdot K_{RH,Al-Elec} \cdot L^*_{Al-Elec} \tag{4.48}$$

The proposed EUL model can be given by using a combined stress factor $K_{combined,Al-Elec}$ to substitute the mathematical product of those stress factors:

$$EUL_{Al-Elec} = K_{combined,Al-Elec} \cdot L^*_{Al-Elec} \tag{4.49}$$

An Al-Elec power capacitor product from Jianghai Capacitor Co., Ltd in Table 4.3.1 will be used again as a provider of modeling information.

TABLE 4.3.1 COMPREHENSIVE RATINGS FOR AN AL-ELEC POWER CAPACITOR

Manufacturer	**MPNs**	**Unit Capacitance (μF)**	I_r^* **on 85 C°, 120 Hz (Arms)**	ΔT^*_{core} **(C°/K)**	T^*_{amb} **(C°)**	V^* **(Vdc)**	RH^*
Jianghai	ECS2GQL182MVB350090V	1800	7.3	10/283	85	400	80%

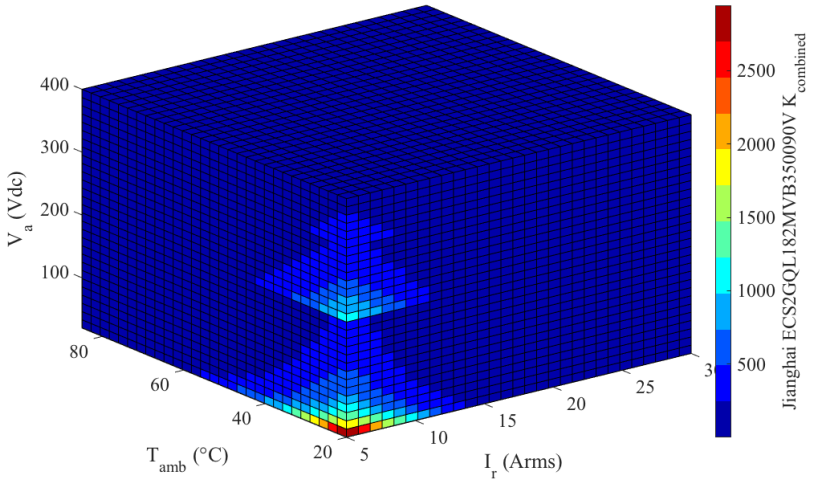
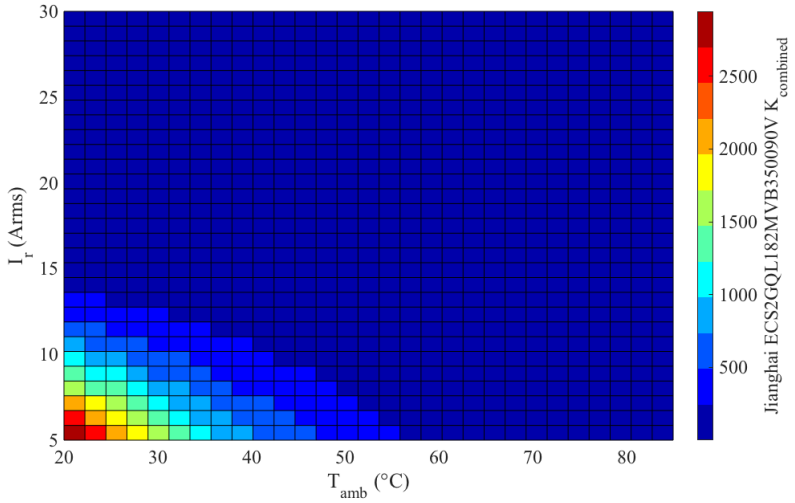


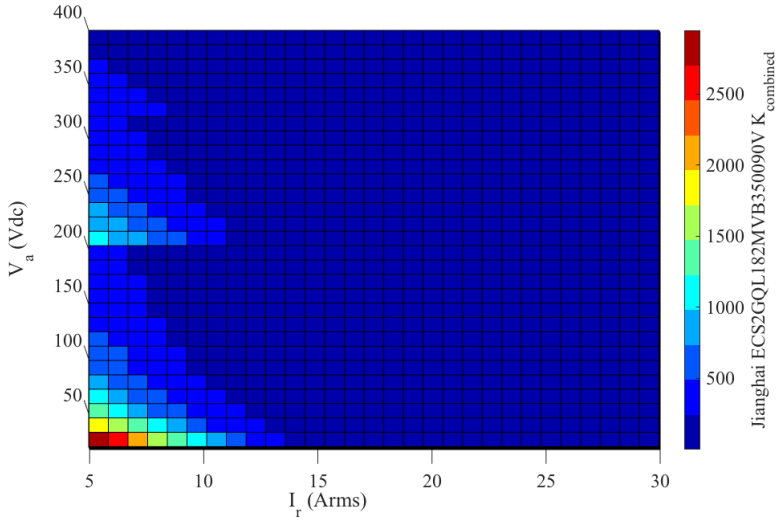
Fig. 4.3.1 4-D image of $K_{combined}$ for Jianghai ECS2GQL182MVB350090V.

Fig. 4.3.1 shows the characteristics of the combined stress factor of this capacitor. The less dominant stress factor $K_{RH,Al-Elec}$ is set to 1 for normal humid environments ($RH \leq 80\%$), so 4-D information is shown in this figure, in which x-axis represents the range of ripple currents I_r (Arms), y-axis indicates the range of ambient temperatures T_{amb} (°C) and z-axis shows the range of applied voltage V_a (V_{dc}), the magnitude of $K_{combined}$ is denoted by the color bar on the right.

It can be seen that the higher values of $K_{combined}$ would approximate the locations where stress factors are less rigorous. This is because for both thermal stress factors and non-thermal stress factors. The estimated values of stress factors appear exponential-form increases as the stresses decrease, ending up with a relatively high $K_{combined}$.



(a) $I_r - T_{amb}$ view.



(b) $I_r - V_a$ view.

Fig. 4.3.2 Different views of $K_{combined}$ for Jianghai ECS2GQL182MVB350090V.

Fig. 4.3.2 shows two different viewing directions of $K_{combined}$. In Fig. 4.3.2 (a) $I_r - T_{amb}$ view is displayed. There is an apparent conclusion can be settled that highest values of $K_{combined}$ located on the left-bottom corner of the diagram which capacitor receives the least impacts from I_r and T_{amb} in this situation. Note that as the stress values

increases along both axes, $K_{combined}$ decays faster in I_r-axis compared with T_{amb}-axis when $I_r > 15$ Arms. T_{amb} has no more capability to change the value of $K_{combined}$, which remains the least value. It implies that Al-Elec power capacitors' EUL is more vulnerable to ripple current compared with ambient temperature.

$I_r - V_a$ view is shown in Fig. 4.3.2 (b). V_a has a relatively mild impact on $K_{combined}$, especially because of its section features as shown in Eq. (4.25), which avoid quick attenuation as applied voltage goes up. Similarly, $I_r > 15$ Arms will limit the performance of V_a as well.

B. MPPF Power Capacitors

For MPPF power capacitor, proposed EUL model is expressed as:

$$EUL_{MPPF} = K_{RC,MPPF} \cdot K_{T_{amb},MPPF} \cdot K_{V_a,MPPF} \cdot K_{RH,MPPF} \cdot L^*_{MPPF} \tag{4.50}$$

In the same way, the proposed EUL model can be given by using a combined stress factor $K_{combined,Al-Elec}$ to substitute the mathematical product of those stress factors:

$$EUL_{MPPF} = K_{combined,MPPF} \cdot L^*_{MPPF} \tag{4.51}$$

An MPPF power capacitor product from Hitachi Inc. will be used for $K_{combined,MPPF}$ modeling, corresponding ratings are given in Table 4.3.2. Fig. 4.3.3 shows the features of the combined stress factor of this MPPF capacitor for normal operating situations, the humidity stress factor $K_{RH,MPPF}$ is set to 1 for normal humid environments ($RH \leq 75\%$), This diagram contains 4-D information for $K_{combined}$.

TABLE 4.3.2 COMPREHENSIVE RATINGS FOR A MPPF POWER CAPACITOR

Manufacturer	**MPNs**	**Unit Capacitance (μF)**	**I_r^* on 50 C°, 1k~10k Hz (Arms)**	***ESR* (mΩ)**	**R_{th} (K/W)**	**T_{amb}^* (C°)**	**V^* (Vdc)**	***RH****
Hitachi	MLC1300V138 KB140225	1300	72	1.6	2.4	80	1300	75%

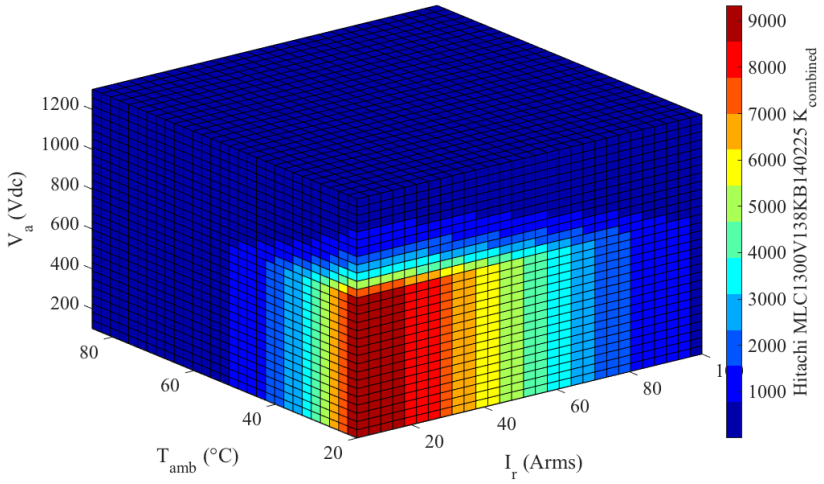
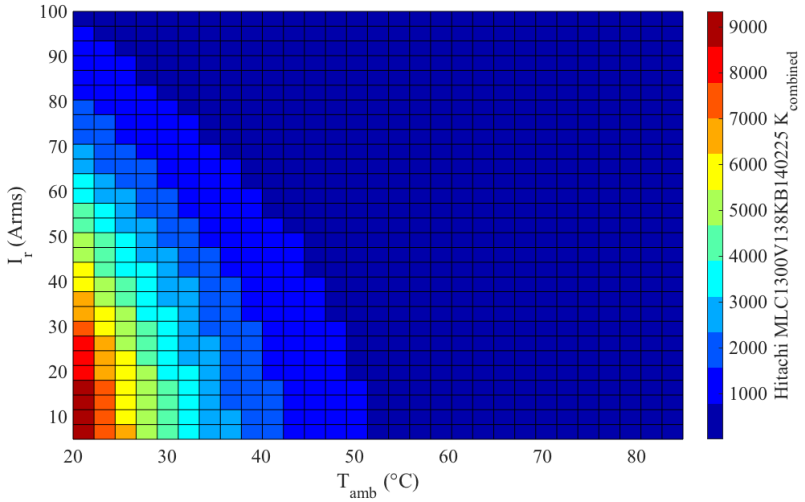


Fig. 4.3.3 4-D image of $K_{combined}$ for Hitachi MLC1300V138KB140225.

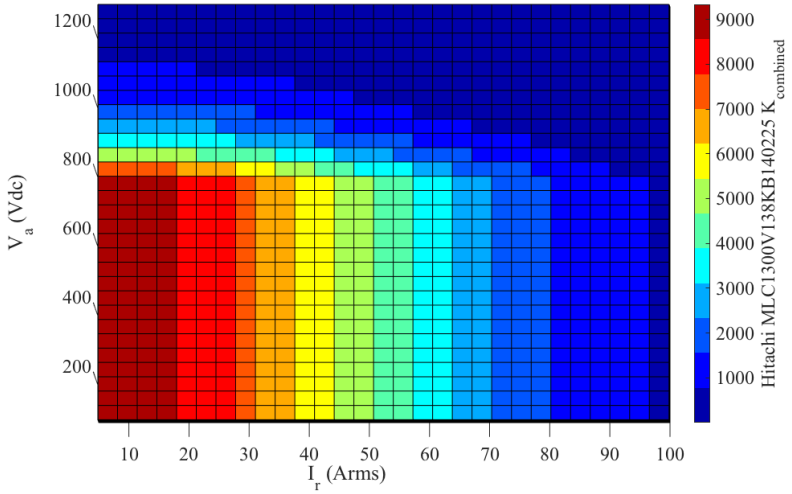
Likewise, higher values of $K_{combined}$ reflect lower levels of those three stresses, $K_{combined}$ will appear a diminution when stresses become harsher.

Fig. 4.3.4 has two different viewing directions of $K_{combined}$, in (a) $I_r - T_{amb}$ view is showed, in (b) $I_r - V_a$ view is showed. For (a), It is apparent that $K_{combined}$ decreases slower with an increasing I_r compared with T_{amb}, therefore for MPPF power capacitors I_r has less influence on capacitor's lifetime, indicating a better performance of MPPF capacitors in sustaining ripple currents.

In (b), $K_{combined}$ can retain the highest value when $I_r < 20$ Arms, even V_a reaches to 800 Vdc, showing the weight of V_a is smaller than I_r. Even though T_{amb} appears the most obvious influence, but it is an uncontrollable stress that entirely depends on the surroundings. Thus, I_r should be the stress that receives the top concern.



(a) $I_r - T_{amb}$ view.



(b) $I_r - V_a$ view.

Fig. 4.3.4 Different views of $K_{combined}$ for Hitachi MLC1300V138KB140225.

4.3.2 Model Feasibility Verification

In section 4.3.1, EUL models were proposed for both Al-Elec power capacitors and MPPF power capacitors. Their characteristics were illustrated by plotting the combined stress factor $K_{combined}$ for two capacitor products on their normal operating conditions.

The feasibility of the proposed EUL model can be verified by making comparison between the EULs obtained by applying proposed method with those provided by manufacturer lifetime diagrams (MLD) created by capacitor companies, which can be seen as standard official guidelines for capacitor reliability analysis. Usually MLD directly indicates the estimated lifetime, or lifetime multiplier of a capacitor under specified circumstances. The estimated lifetime can be seen as useful lifetime, while lifetime multiplier requires an appendant basic useful lifetime to be multiplied.

A. Al-Elec Power Capacitors

For Al-Elec power capacitor category, two candidates from two capacitor companies are chosen for testing: ECS2GQL182MVB350090V from Jianghai Capacitor Co., Ltd and VFL2G103YQE188 from Hitachi AIC Inc. Ratings for these two capacitors are shown in Table 4.3.3.

TABLE 4.3.3 COMPREHENSIVE RATINGS FOR TWO AL-ELEC POWER CAPACITORS

Manufacturer	**MPNs**	I_r^* **on 85 °C, 120 Hz (Arms)**	ΔT_{core}^* **(°C/K)**	T_{amb}^* **(°C)**	V^* **(Vdc)**	RH^*	L^* **(h)**
Jianghai	ECS2GQL182MVB350090V	7.3	7.5/280.65	85	400	80%	5000
Hitachi	VFL2G103YQE188	27.6	6.1/279.25	85	400	85%	8000

1) Jianghai ECS2GQL182MVB350090V: $I_a = 9.125$ Arms (120 Hz, 85°C), $T_{amb} = 60°C$, $V_a = V^*$, $RH_a < RH^*$

In this condition, ripple current and ambient temperature can be summarized as:

$$\begin{cases} \dfrac{I_r}{I_r{}^*} = \dfrac{9.125}{7.3} = 1.25 \\ T_{amb} = 60°C \end{cases}$$

For this capacitor, MLD is shown in Fig. 4.3.5. In this condition it can be localized as:

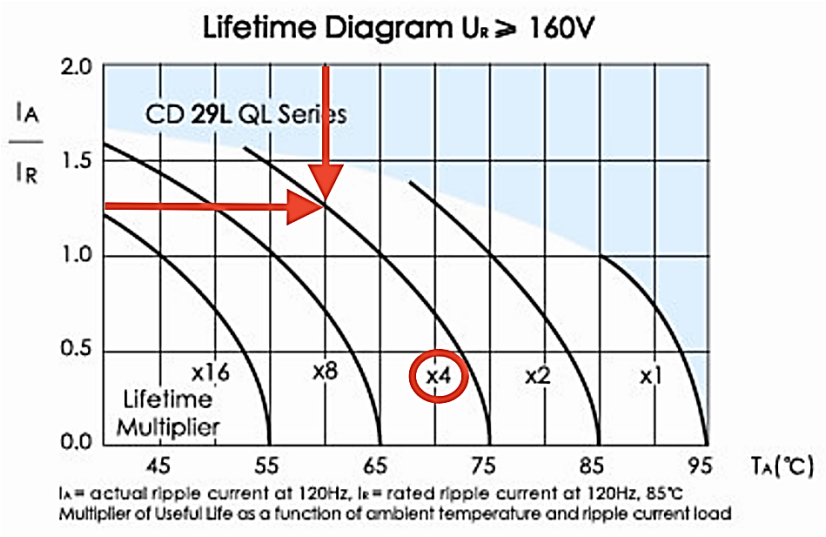


Fig. 4.3.5 Lifetime multiplier location 1) in Jianghai ECS2GQL182MVB350090V's MLD.

Basic lifetime $L^*_{Al-Elec}$ is designed as 5000 h, the EUL determined by MLD can be given as:

$$EUL_{MLD} = Lifetime\ Multiplier \times L^*_{Al-Elec} = 4 \times 5000\ h = 20000\ h$$

In this condition, $K_{V_a,Al-Elec}$, $K_{RH,Al-Elec}$ are set to 1, for $K_{RC,Al-Elec}$ and $K_{T_{amb},Al-Elec}$:

$$K_{RC,Al-Elec}(I_r) = \exp\left(10908.7\left(\frac{I_r^{*2}}{I_r{}^2\Delta T^*_{core} + I_r^{*2}T_{amb}} - \frac{1}{\Delta T^*_{core} + T_{amb}}\right)\right)$$

$$= exp\left(10908.7\left(\frac{7.3^2}{9.125^2 \cdot 7.5\text{K} + 7.3^2 \cdot 333.15\text{K}} - \frac{1}{7.5\text{K} + 333.15\text{K}}\right)\right)$$

$$= 0.676$$

$$K_{T_{amb},Al-Elec}(\tau) \cong 2^{\tau/10} = 2^{\frac{85-60}{10}} = 5.657$$

$$K_{combined,Al-Elec} = K_{RC,Al-Elec} \cdot K_{T_{amb},Al-Elec} \cdot K_{V_a,Al-Elec} \cdot K_{RH,Al-Elec} = 3.824$$

Then the EUL calculated by the proposed EUL model can be calculated as:

$$EUL_{Model} = K_{combined,Al-Elec} \cdot L^*_{Al-Elec} = 3.824 \times 5000\ h = 19120\ h$$

The relative error (RE) in this condition is given as:

$$RE = \frac{EUL_{Model} - EUL_{MLD}}{EUL_{MLD}} = -4.40\%$$

2) Jianghai ECS2GQL182MVB350090V: $I_a = 3.65$ Arms (120 Hz, 85°C), $T_{amb} = 52.5$°C, $V_a = V^*$, $RH_a < RH^*$

In this condition, ripple current information and ambient temperature can be summarized as:

$$\begin{cases} \dfrac{I_r}{I_r^*} = \dfrac{3.65}{7.3} = 0.5 \\ T_{amb} = 52.5°\text{C} \end{cases}$$

Then the lifetime multiplier in MLD can be localized in Fig. 4.3.6 :

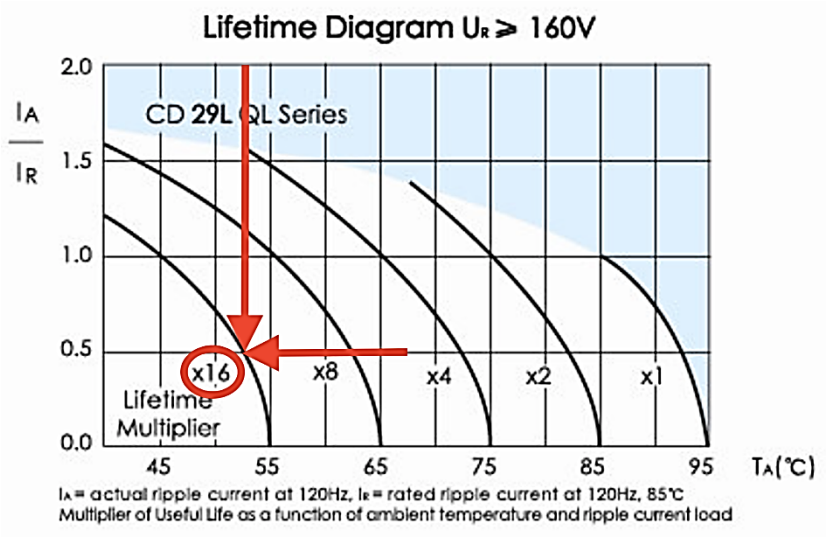


Fig. 4.3.6 Lifetime multiplier location 2) in Jianghai ECS2GQL182MVB350090V's MLD.

The EUL determined by MLD can be given as:

$$EUL_{MLD} = Lifetime\ Multiplier \times L^*_{Al-Elec} = 16 \times 5000\ h = 80000\ h$$

In this condition, $K_{V_a,Al-Elec}$, $K_{RH,Al-Elec}$ are set to 1, for $K_{RC,Al-Elec}$ and $K_{T_{amb},Al-Elec}$:

$$K_{RC,Al-Elec}(I_r) = \exp\left(10908.7\left(\frac{I_r^{*2}}{{I_r}^2\Delta T^*_{core} + I_r^{*2}T_{amb}} - \frac{1}{\Delta T^*_{core} + T_{amb}}\right)\right)$$

$$= exp\left(10908.7\left(\frac{7.3^2}{3.65^2 \cdot 7.5\text{K} + 7.3^2 \cdot 325.65\text{K}} - \frac{1}{7.5\text{K} + 325.65\text{K}}\right)\right)$$

$$= 1.754$$

$$K_{T_{amb},Al-Elec}(\tau) \cong 2^{\tau/10} = 2^{\frac{85-52.5}{10}} = 9.514$$

$$K_{combined,Al-Elec} = K_{RC,Al-Elec} \cdot K_{T_{amb},Al-Elec} \cdot K_{V_a,Al-Elec} \cdot K_{RH,Al-Elec} = 16.687$$

Then the EUL calculated by the proposed EUL model is determined as:

$$EUL_{Model} = K_{combined,Al-Elec} \cdot L^*_{Al-Elec} = 16.687 \times 5000\ h = 83435\ h$$

RE in this condition is given as:

$$RE = \frac{EUL_{Model} - EUL_{MLD}}{EUL_{MLD}} = 4.29\%$$

For ECS2GQL182MVB350090V Al-Elec power capacitor from Jianghai, the proposed EUL model can effectively represent the lifetime information that derived from MLD, with a $RE < \pm 5\%$.

3) Hitachi VFL2G103YQE188: $I_a = 13.8$ Arms (120 Hz, 85°C), $T_{amb} = 60°C$, $V_a = V^*$, $RH_a < RH^*$

In this condition, ripple current information and ambient temperature can be summarized as:

$$\begin{cases} \dfrac{I_r}{I_r^*} = \dfrac{13.8}{27.6} = 0.5 \\ T_{amb} = 60°C \end{cases}$$

MLD of this capacitor presents estimated lifetime directly as the useful lifetime, in this situation it can be localized as Fig. 4.3.7:

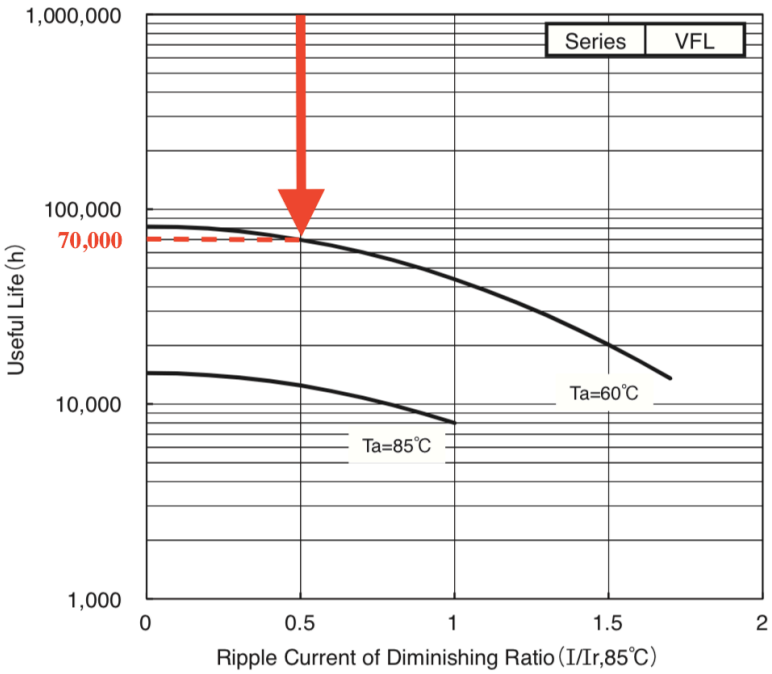


Fig. 4.3.7 Lifetime multiplier location 3) in Hitachi VFL2G103YQE188's MLD.

EUL determined by MLD can be given as:

$$EUL_{MLD} = 70000\ h$$

For this condition, $K_{V_a,Al-Elec}$, $K_{RH,Al-Elec}$ are set to 1, so $K_{RC,Al-Elec}$ and

$K_{T_{amb},Al-Elec}$:

$$K_{RC,Al-Elec}(I_r) = \exp\left(10908.7\left(\frac{I_r^{*2}}{{I_r}^2\Delta T_{core}^* + I_r^{*2}T_{amb}} - \frac{1}{\Delta T_{core}^* + T_{amb}}\right)\right)$$

$$= exp\left(10908.7\left(\frac{27.6^2}{13.8^2 \cdot 6.1\text{K} + 27.6^2 \cdot 333.15\text{K}} - \frac{1}{6.1\text{K} + 333.15\text{K}}\right)\right)$$

$$= 1.552$$

$$K_{T_{amb},Al-Elec}(\tau) \cong 2^{\tau/10} = 2^{\frac{85-60}{10}} = 5.657$$

$$K_{combined,Al-Elec} = K_{RC,Al-Elec} \cdot K_{T_{amb},Al-Elec} \cdot K_{V_a,Al-Elec} \cdot K_{RH,Al-Elec} = 8.779$$

Basic lifetime $L^*_{Al-Elec}$ is designed as 8000 h, then the EUL calculated by the proposed EUL model:

$$EUL_{Model} = K_{combined,Al-Elec} \cdot L^*_{Al-Elec} = 8.779 \times 8000\ h = 70232\ h$$

RE in this condition is given as:

$$RE = \frac{EUL_{Model} - EUL_{MLD}}{EUL_{MLD}} = 0.33\%$$

4) Hitachi VFL2G103YQE188: $I_a = 21.25$ Arms (120 Hz, 85°C), $T_{amb} = 80$°C, $V_a = V^*$, $RH_a < RH^*$

Similarly, ripple current and ambient temperature conditions can be summarized as:

$$\begin{cases} \dfrac{I_r}{I_r^*} = \dfrac{21.25}{27.6} = 0.77 \\ T_{amb} = 80\text{°C} \end{cases}$$

The estimated lifetime in MLD can be localized as Fig. 4.3.8:

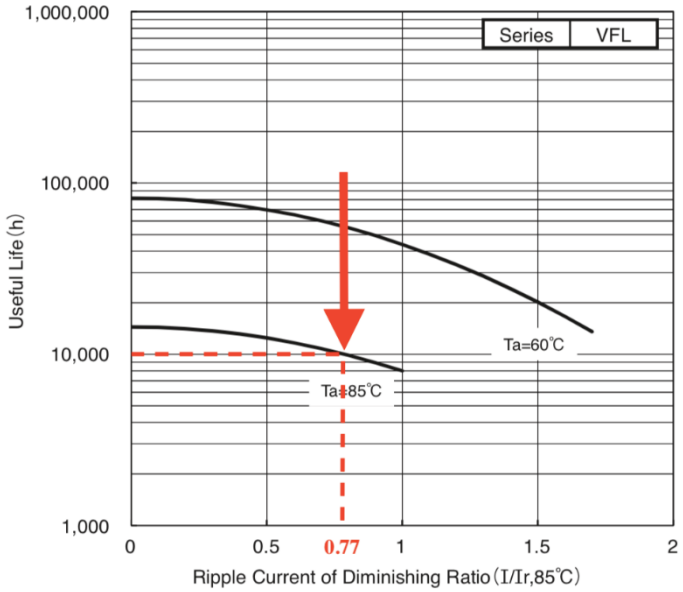


Fig. 4.3.8 Lifetime multiplier location 4) in Hitachi VFL2G103YQE188's MLD.

EUL determined by MLD can be given as:

$$EUL_{MLD} = 10000\ h$$

For this condition, $K_{V_a,Al-Elec}$, $K_{RH,Al-Elec}$, $K_{T_{amb},Al-Elec}$ are set to 1, so $K_{RC,Al-Elec}$ is given as:

$$K_{RC,Al-Elec}(I_r) = \exp\left(10908.7\left(\frac{I_r^{*2}}{{I_r}^2\Delta T_{core}^{*} + I_r^{*2}T_{amb}} - \frac{1}{\Delta T_{core}^{*} + T_{amb}}\right)\right)$$

$$= exp\left(10908.7\left(\frac{27.6^2}{21.25^2 \cdot 6.1\text{K} + 27.6^2 \cdot 358.15\text{K}} - \frac{1}{6.1\text{K} + 358.15\text{K}}\right)\right)$$

$$= 1.228$$

$$K_{combined,Al-Elec} = K_{RC,Al-Elec} \cdot K_{T_{amb},Al-Elec} \cdot K_{V_a,Al-Elec} \cdot K_{RH,Al-Elec} = 1.228$$

Then the EUL calculated by the proposed EUL model:

$$EUL_{Model} = K_{combined,Al-Elec} \cdot {L^*}_{Al-Elec} = 1.228 \times 8000\ h = 9824\ h$$

RE in this condition is given as:

$$RE = \frac{EUL_{Model} - EUL_{MLD}}{EUL_{MLD}} = -1.76\%$$

For VFL2G103YQE188 Al-Elec power capacitor from Hitachi, the proposed EUL model still can maintain an excellent lifetime estimation with a $RE < \pm 2\%$ of standard lifetime given by manufacturers.

B. MPPF Power Capacitors

Two MPPF capacitor products from two companies are selected as well for verification: ECS2GQL182MVB350090V from Jianghai Capacitor Co., Ltd, VFL2G103YQE188 from Hitachi AIC Inc., E37L401CPN562MF92U from UCC Inc. Ratings for these three capacitors are shown in Table 4.3.4.

TABLE 4.3.4 COMPREHENSIVE RATINGS FOR A MPPF POWER CAPACITOR

Manufacturer	**MPNs**	$\frac{E_a}{k_B}$	I_r^* **on 1k~10k Hz (Arms)**	ESR **(mΩ)**	R_{th} **(K/W)**	T_{amb}^* **(℃)**	V^* **(Vdc)**	RH^*	L^***(h)**
Jianghai	FCCC3DL107*H09503*	10800	92(40℃)	1.3	2.7	50	1300	75%	100000
Hitachi	MLC1300V138KB140225	12000	72(50℃)	1.6	2.4	40	1300	75%	130000

*1) Jianghai FCCC3DL107*H09503*:* $V_a = 1495$ Vdc, $T_{core} = 70$°C, $T_{amb} = T_{amb}^*$, $RH_a < RH^*$

In this condition, applied voltage information and capacitor core temperature

information that derived from ripple current can be summarized as:

$$\begin{cases} \dfrac{V_a}{V^*} = \dfrac{1495}{1300} = 1.15 \\ T_{core} = 70°\text{C} \end{cases}$$

MLD provides the estimated lifetime and it is localized as Fig. 4.3.9:

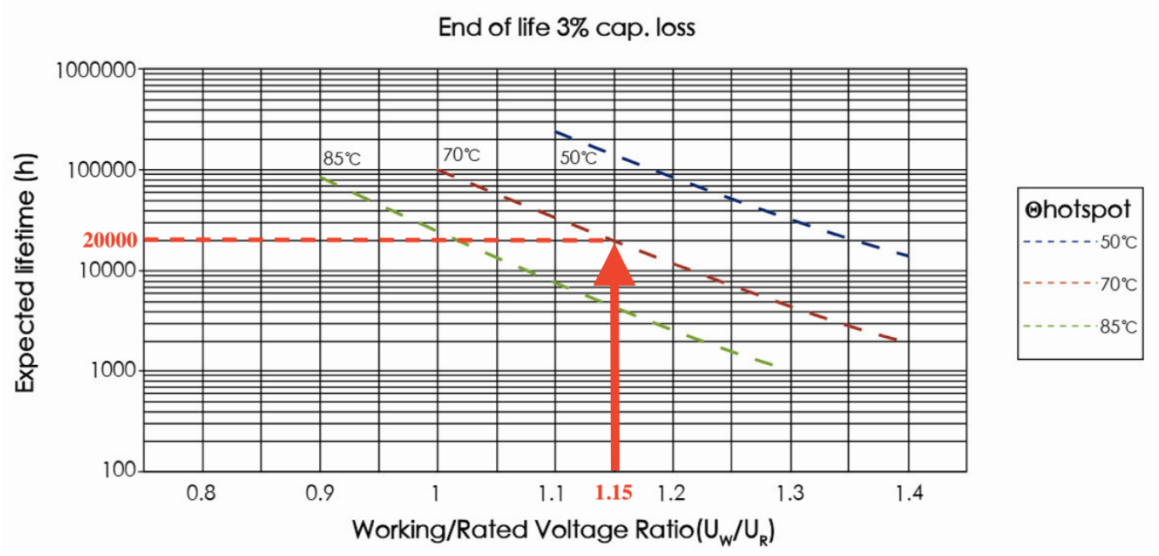


Fig. 4.3.9 Lifetime multiplier location 1) in Jianghai FCCC3DL107*H09503*'s MLD.

EUL determined by MLD can be given as:

$$EUL_{MLD} = 20000\ h$$

For this condition, $K_{RH,MPPF}$ and $K_{T_{amb},MPPF}$ are set to 1, so $K_{V_a,MPPF}$, $K_{RC,MPPF}$ are given as:

$$K_{V_a,MPPF}(V_a) = \left(\frac{V_a}{V^*}\right)^{-\alpha_{V_a,MPPF}} = 1.15^{-11.7} = 0.1949$$

$$K_{RC,MPPF}(I_r) = \exp\left(10800\left(\frac{1}{{I_r}^2 ESR \cdot R_{th} + T_{amb}} - \frac{1}{{I_r^*}^2 ESR \cdot R_{th} + T_{amb}}\right)\right)$$

$$= \exp\left(10800\left(\frac{1}{T_{core}} - \frac{1}{{I_r^*}^2 ESR \cdot R_{th} + T_{amb}}\right)\right)$$

$$= \exp\left(10800\left(\frac{1}{343.15K} - \frac{1}{92^2 \cdot 0.0013 \cdot 2.7 + 313.15}\right)\right) = 0.9736$$

$$K_{combined,MPPF} = K_{RC,MPPF} \cdot K_{T_{amb},MPPF} \cdot K_{V_a,MPPF} \cdot K_{RH,MPPF} = 0.1898$$

Basic lifetime L^*_{MPPF} is given as 100000 h, Then the EUL calculated by the proposed EUL model:

$$EUL_{Model} = K_{combined,MPPF} \cdot L^*_{MPPF} = 0.1898 \times 100000\ h = 18980\ h$$

RE in this condition is given as:

$$RE = \frac{EUL_{Model} - EUL_{MLD}}{EUL_{MLD}} = -5.1\%$$

2) *Jianghai FCCC3DL107*H09503*:* $V_a = 1625$ Vdc, $T_{core} = 50$°C, $T_{amb} = T^*_{amb}$, $RH_a < RH^*$

In this condition, applied voltage and capacitor core temperature produced by ripple current can be summarized as:

$$\begin{cases} \frac{V_a}{V^*} = \frac{1625}{1300} = 1.25 \\ T_{core} = 50℃ \end{cases}$$

Estimated lifetime in MLD can be localized as:

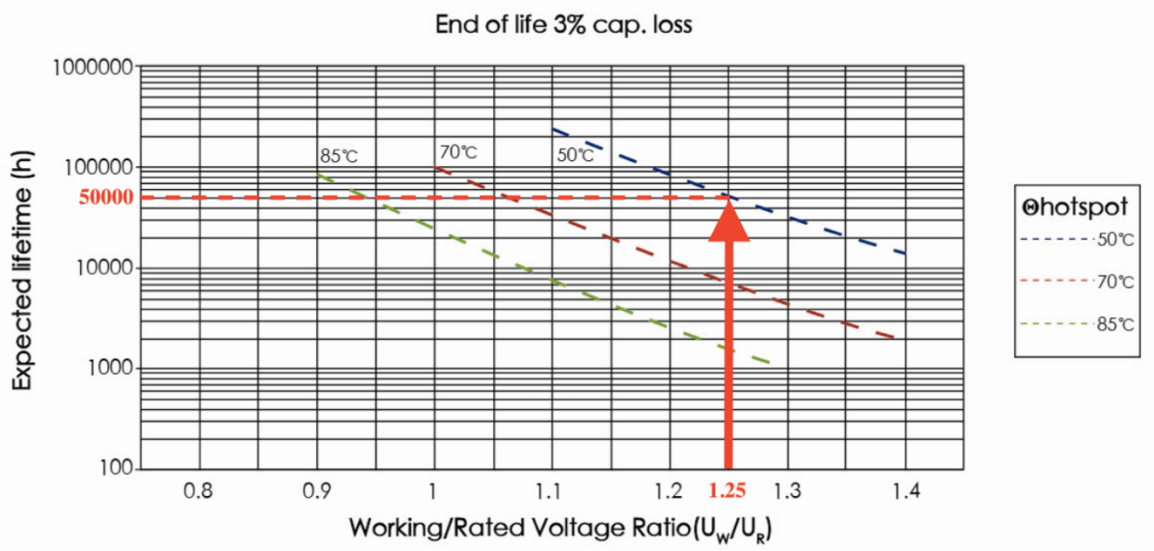


Fig. 4.3.10 Lifetime multiplier location 2) in Jianghai FCCC3DL107*H09503*'s MLD.

EUL determined by MLD can be given as:

$$EUL_{MLD} = 50000\ h$$

$K_{RH,MPPF}$ and $K_{T_{amb},MPPF}$ are set to 1, and $K_{V_a,MPPF}$, $K_{RC,MPPF}$ are given as:

$$K_{V_a,MPPF}(V_a) = \left(\frac{V_a}{V^*}\right)^{-\alpha_{V_a,MPPF}} = 1.25^{-11.7} = 0.0735$$

$$K_{RC,MPPF}(I_r) = \exp\left(10800\left(\frac{1}{T_{core}} - \frac{1}{I_r^{*2} ESR \cdot R_{th} + T_{amb}}\right)\right)$$

$$= \exp\left(10800\left(\frac{1}{323.15K} - \frac{1}{92^2 \cdot 0.0013 \cdot 2.7 + 313.15}\right)\right) = 6.8288$$

$$K_{combined,MPPF} = K_{RC,MPPF} \cdot K_{T_{amb},MPPF} \cdot K_{V_a,MPPF} \cdot K_{RH,MPPF} = 0.5019$$

$$EUL_{Model} = K_{combined,MPPF} \cdot L^*_{MPPF} = 0.5019 \times 100000\ h = 50190\ h$$

RE in this condition is given as:

$$RE = \frac{EUL_{Model} - EUL_{MLD}}{EUL_{MLD}} = 0.38\%$$

For FCCC3DL107*H09503* MPPF power capacitor from Jianghai, the proposed EUL model can handle the lifetime estimation which matches the results that derived from MLD, with a $RE < \pm 6\%$.

3) Hitachi MLC1300V138KB140225: $V_a = 1378$ Vdc, $T_{core} = 70°C$, $T_{amb} = T^*_{amb}$, $RH_a < RH^*$

In this condition, information of applied voltage and ripple-current-caused core temperature of the capacitor can be summarized as:

$$\begin{cases} \dfrac{V_a}{V^*} = \dfrac{1378}{1300} = 1.06 \\ T_{core} = 70°C \end{cases}$$

Then the estimated lifetime in MLD is localized as:

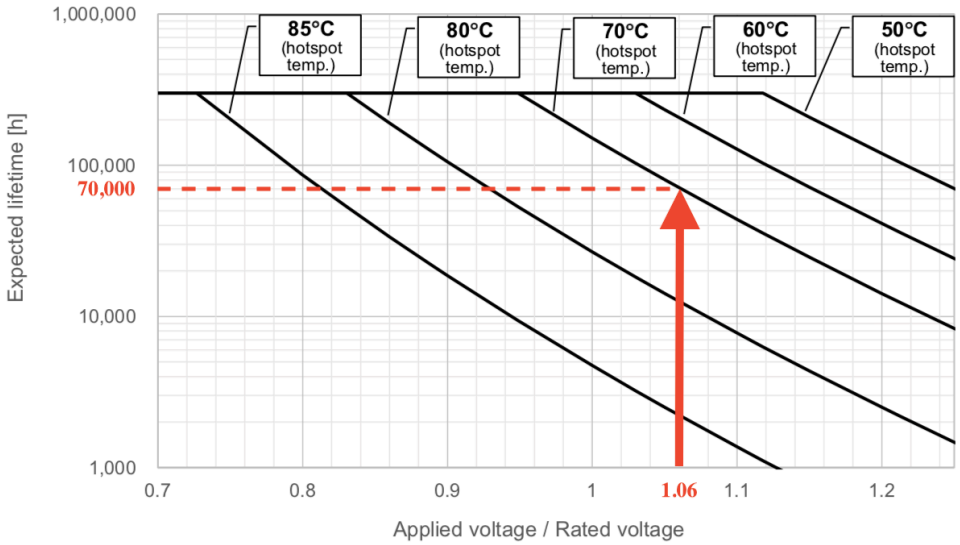


Fig. 4.3.11 Lifetime multiplier location 3) in Hitachi MLC1300V138KB140225's MLD.

EUL determined by MLD can be given as:

$$EUL_{MLD} = 70000\ h$$

$K_{RH,MPPF}$ and $K_{T_{amb},MPPF}$ are set to 1, and $K_{V_a,MPPF}$, $K_{RC,MPPF}$ are given as:

$$K_{V_a,MPPF}(V_a) = \left(\frac{V_a}{V^*}\right)^{-\alpha_{V_a,MPPF}} = 1.06^{-11.6} = 0.5087$$

$$K_{RC,MPPF}(I_r) = \exp\left(12000\left(\frac{1}{T_{core}} - \frac{1}{I_r^{*2} ESR \cdot R_{th} + T_{amb}}\right)\right)$$

$$= \exp\left(12000\left(\frac{1}{343.15K} - \frac{1}{72^2 \cdot 0.0016 \cdot 2.4 + 323.15}\right)\right) = 0.991$$

$$K_{combined,MPPF} = K_{RC,MPPF} \cdot K_{T_{amb},MPPF} \cdot K_{V_a,MPPF} \cdot K_{RH,MPPF} = 0.5042$$

Basic lifetime L^*_{MPPF} is given as 130000 h, Then EUL calculated by the proposed EUL model is given as:

$$EUL_{Model} = K_{combined,MPPF} \cdot L^*_{MPPF} = 0.5019 \times 130000\ h = 65536\ h$$

RE in this condition is given as:

$$RE = \frac{EUL_{Model} - EUL_{MLD}}{EUL_{MLD}} = -6.377\%$$

4) *Hitachi MLC1300V138KB140225:* $V_a = 1482$ Vdc, $T_{core} = 60$°C, $T_{amb} = T^*_{amb}$, $RH_a < RH^*$

In this situation, applied voltage and core temperature stresses of the capacitor can be summarized as:

$$\begin{cases} \frac{V_a}{V^*} = \frac{1482}{1300} = 1.14 \\ T_{core} = 60°\text{C} \end{cases}$$

Estimated lifetime in MLD can be localized as:

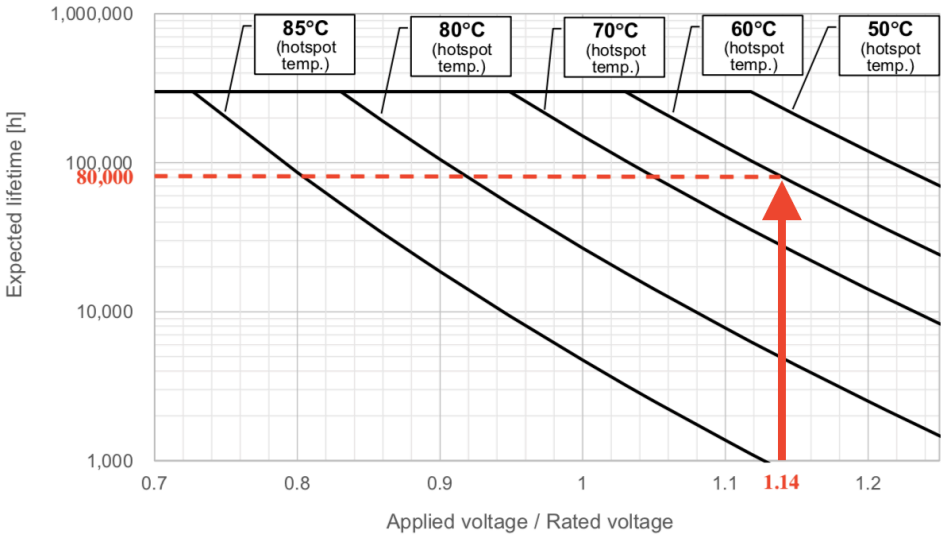


Fig. 4.3.12 Lifetime multiplier location 4) in Hitachi MLC1300V138KB140225's MLD.

EUL determined by MLD can be given as:

$$EUL_{MLD} = 80000\ h$$

$K_{RH,MPPF}$ and $K_{T_{amb},MPPF}$ are set to 1, and $K_{V_a,MPPF}$, $K_{RC,MPPF}$ are given as:

$$K_{V_a,MPPF}(V_a) = \left(\frac{V_a}{V^*}\right)^{-\alpha_{V_a,MPPF}} = 1.14^{-11.6} = 0.2187$$

$$K_{RC,MPPF}(I_r) = \exp\left(12000\left(\frac{1}{T_{core}} - \frac{1}{I_r^{*2} ESR \cdot R_{th} + T_{amb}}\right)\right)$$

$$= \exp\left(12000\left(\frac{1}{333.15K} - \frac{1}{72^2 \cdot 0.0016 \cdot 2.4 + 323.15}\right)\right) = 2.8297$$

$$K_{combined,MPPF} = K_{RC,MPPF} \cdot K_{T_{amb},MPPF} \cdot K_{V_a,MPPF} \cdot K_{RH,MPPF} = 0.6189$$

$$EUL_{Model} = K_{combined,MPPF} \cdot L^*_{MPPF} = 0.5019 \times 130000\ h = 80457\ h$$

RE in this condition is given as:

$$RE = \frac{EUL_{Model} - EUL_{MLD}}{EUL_{MLD}} = 0.571\%$$

For MLC1300V138KB140225 MPPF power capacitor from Hitachi, the proposed EUL model is still capable to indicate the lifetime, which fits the results that derived from MLD with a $RE < \pm 7\%$.

4.4 Summary

In this chapter, stress factors are categorized and modelled. If they are relative to thermal influence, ripple current stress factor and ambient temperature stress factor that show thermal characteristics were modelled by the Arrhenius law. The inverse power law takes care of non-thermal stress factors, i.e., applied voltage and humidity stress factors. Features of them are summarized with the help of corresponding curves of those stress factors.

Reliability analysis was also deployed for power capacitors. Some concepts have been introduced to evaluate the relationship between failure and reliability. Mean time to failure, also can be seen as estimated useful lifetime for unrepairable capacitors, is proved to be a good indicator for capacitor reliability representation.

Then the proposed estimated useful lifetime models for both Al-Elec power capacitors and MPPF power capacitors took full advantage of aforementioned stress factors and integrate them into a combined stress factor. 4-D images of the combined stress factor reveals that MPPF power capacitors generally have better lifetime performances than Al-Elec power capacitors, while ripple current is noteworthy due to its apparent weight on

determining lifetime for both capacitor types. The feasibility of the proposed model is also verified by making comparisons with manufacturer lifetime diagrams of some in-market power capacitor products.

In chapter 5, aiming at suppressing ripple current stress, relevant analysis of dc-link ripple current in a regen CHB motor drive will be presented, and a new ripple current reduction method will be proposed.

Chapter 5

Proposed Current Harmonics Reduction Method for DC-Link Power Capacitors in Regenerative Cascaded H-bridge Power Cells

5.1 Introduction

As discussed in chapter 4, ripple current performance of a dc-link power capacitor stands for an essential position on determining the reliability of the capacitor unit. If a relatively high ripple current flows into a capacitor, an unpleasant estimated lifetime would be anticipated as a penalty, thermal loss might increase due to a higher rms current. Investigating methods to achieve ripple current suppression for dc-link power capacitors is one of the most critical issues in power cell design and corresponding lifetime improvement.

In this chapter, a new approach to reduce ripple currents in the dc-link power capacitors of a regen CHB power cells is proposed. In order to suppress the 2nd carrier

dominant harmonic current injected into dc-link capacitors, a SPWM carrier shifting technique (CST) is proposed. This proposed method is based on an optimization ideology, which can promote dc-link capacitor's performance on ripple current rating and power loss.

Some existing literatures aim at reducing converter input current harmonics to suppress the dc-link harmonics. In [70], a new method is presented to optimize combinations of voltage space vector for a 2-level VSI under different modulation indices. However, the chosen switching states infect harmonic performance on line-to-line voltage. In [71], a model reference adaptive system for a 2-level rectifier with a distorted grid voltage is proposed to reduce baseband harmonics. The effectiveness is obvious; however, higher-order carrier band harmonics are still significant.

PWM carrier manipulation also attracts some researchers on dc-link harmonic reduction. In [72], carrier shifts for both converter sides on a 2-level back-to-back converter is applied and the first carrier band harmonic on dc link is eliminated. [73] introduced PWM carrier interleaving method on a 48V belt-driven starter-generator and achieved phase current ripple reduction, but two parallel 3-phase motor-inverter topologies need to be integrated, which limits the application. There are also some other methods introduced against this problem, such as third harmonic zero-sequence current injection [74], multi-phase loads mixing method [75], analytical expression of dc-link capacitor rms current in PWM-based converter [76] etc.

All these existing methods claimed effectiveness on specific applications, but due to the actual implementation possibility, they are not suitable for medium voltage motor drive applications.

5.2 Modeling of DC-Link Current Harmonics

As discussed before, a regen CHB power cell is consisted of a 3-phase AFE converter acting as the rectifier, an H-bridge converter acting as the inverter, and a dc-link capacitor. The basic current flow of a regen CHB power cell is indicated in Fig. 5.1 where the current flowing into the capacitor comes from the subtraction of rectifier dc current $i_{dc,rec}$ and inverter current $i_{dc,inv}$ as:

$$i_{cap}(t) = i_{dc,rec}(t) - i_{dc,inv}(t) \tag{5.1}$$

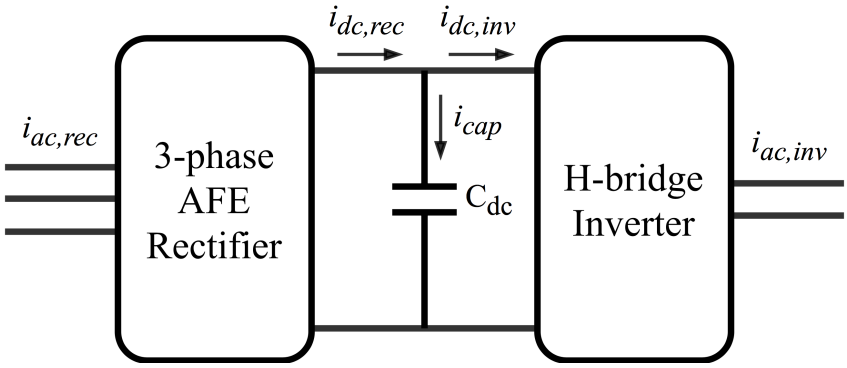


Fig. 5.1 Current flow of a regen CHB power cell.

For both input rectifier side and output inverter side of a regen CHB power cell, the currents are ac signals, which can be derived as:

$$i_{ac,rec\text{ or }inv}(t) = I_{ac}\cos(2\pi f t + \beta) \tag{5.2}$$

where I_{ac} represents the amplitude of 3-phase AFE rectifier or H-bridge inverter ac current. f is the ac current base frequency, β is the skewing angle between ac voltage and ac current. The relationship between the ac-side currents and capacitor dc current is intrinsically determined by the SPWM switching pattern functions.

5.2.1 SPWM Scheme Analysis for One Converter Phase Leg

As mentioned in chapter 2, the basic idea of SPWM modulation scheme for a converter leg is to use a triangular carrier waveform with high-frequency to compare with a low-frequency (base-frequency) sinusoidal reference waveform, in terms of magnitude. The sinusoids can be actual desired ac waveform for inverter, or homologous ac waveform representing the desired dc signal with a PLL-adjusted angle, for rectifier. The results of comparison, either high or low level, are control signals to manipulate the turn-on/off states of two IGBTs in a phase leg, as shown in Fig. 5.2, where M is the modulation index.

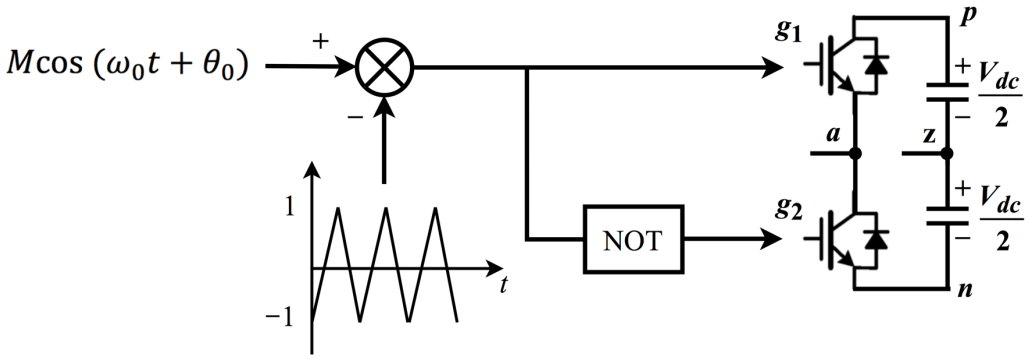


Fig. 5.2 SPWM scheme for one converter phase leg.

A. Double-Variable Fourier Transform Analysis

The converter phase leg output current is a clutch of modulated source signal which are composed of a fundamental desired component, as well as a group of undesired harmonics generated as a consequence of intrinsic switching pattern. An effective way to analyze SPWM-generated harmonics is Fourier Transform analysis. In Fourier Transform theory, any time-domain signal $f(t)$ can be given as a superposition of all harmonic components [77]:

$$f(t) = \frac{a_0}{2} + \sum_{m=1}^{\infty} [a_m \cos(m\omega t) + b_m \sin(m\omega t)] \tag{5.3}$$

where

$$a_m = \frac{1}{\pi} \int_{-\pi}^{\pi} f(t) \cos(m\omega t)\ d\omega t \quad m = 0, 1, \cdots, \infty \tag{5.4}$$

$$b_m = \frac{1}{\pi} \int_{-\pi}^{\pi} f(t) \sin(m\omega t)\ d\omega t \quad m = 1, 2, \cdots, \infty \tag{5.5}$$

In Appendix 1 (pp. 623-628) of [78] the author claimed that a double-variable function $f(x, y)$ shown in Eq. (5.6) can be applied for any $f(t)$ which has a formation like Eq. (5.3):

$$f(x,y) = \frac{A_{00}}{2} + \sum_{n=1}^{\infty} [A_{0n} \cos(ny) + B_{0n} \sin(ny)] + \sum_{m=1}^{\infty} [A_{m0} \cos(mx) + B_{m0} \sin(mx)] + \sum_{m=1}^{\infty} \sum_{n=-\infty(n\neq 0)}^{\infty} [A_{mn} \cos(mx + ny) + B_{mn} \sin(mx + ny)] \tag{5.6}$$

where

$$A_{mn} = \frac{1}{2\pi^2} \iint_{-\pi}^{\pi} f(x,y) \cos(mx + ny)\ dx\ dy \tag{5.7}$$

$$B_{mn} = \frac{1}{2\pi^2} \iint_{-\pi}^{\pi} f(x,y) \sin(mx + ny)\ dx\ dy \tag{5.8}$$

and using a complex formation:

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2} \iint_{-\pi}^{\pi} f(x,y) e^{j(mx+ny)}\ dx\ dy \tag{5.9}$$

Defining x and y as $x(t) = \omega_c t + \theta_c$, $y(t) = \omega_0 t + \theta_0$, in which ω_c is the triangular carrier's angular frequency, θ_c is the arbitrary shifting angle for carrier waveform. ω_0 is the fundamental angular frequency of reference waveform, θ_0 is the offset angle between fundamental waveforms. $\theta_0 = 2k\pi/3$ for 3-phase AFE rectifier where $k = 0, 1, 2$. $\theta_0 = k\pi$ for 2-phase H-bridge inverter where $k = 0, 1$.

Thus $x(t)$ and $y(t)$ can be treated as two time-domain periodic variables that can indicate the angular variation of carrier and reference. By considering the output SPWM-modulated waveform in one converter phase leg as $f(t)$ and combining it with Eq. (5.6):

$$\begin{aligned} f(x,y) = \frac{A_{00}}{2} &+ \sum_{n=1}^{\infty} [A_{0n} \cos(n[\omega_0 t + \theta_0]) + B_{0n} \sin(n[\omega_0 t + \theta_0])] \\ &+ \sum_{m=1}^{\infty} [A_{m0} \cos(m[\omega_c t + \theta_c]) + B_{m0} \sin(m[\omega_c t + \theta_c])] \\ &+ \sum_{m=1}^{\infty} \sum_{n=-\infty(n\neq 0)}^{\infty} [A_{mn} \cos(m[\omega_c t + \theta_c] + n[\omega_0 t + \theta_0]) \\ &+ B_{mn} \sin(m[\omega_c t + \theta_c] + n[\omega_0 t + \theta_0])] \end{aligned} \tag{5.10}$$

where m, n are carrier index and baseband index respectively, showing the location of every component of output phase leg current on frequency spectrum.

Fig 5.3 illustrate the arrangements of these two indices. For instance, $m = -3$ and $n = 1$ appoints the left 3rd sideband harmonic that within the 1st carrier sideband group. This harmonic component has a frequency of $(\omega_c - 3\omega_0)$ rad/s.

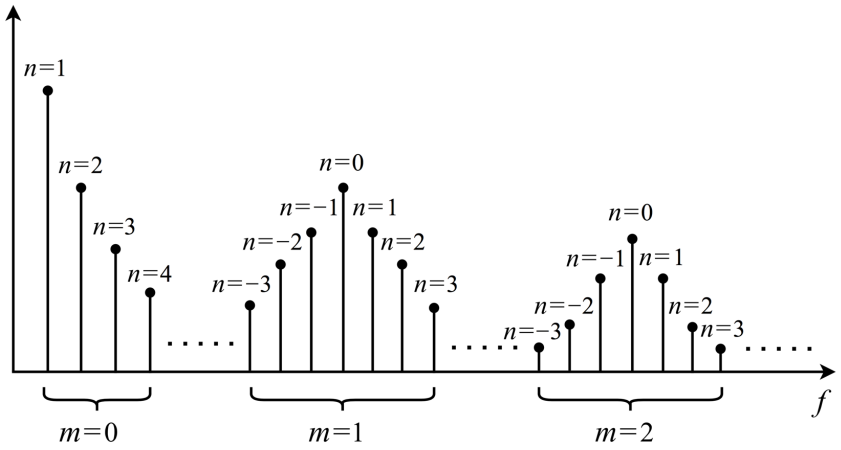


Fig. 5.3 Carrier index and baseband index arrangements.

In Eq. (5.10), $A_{00}/2$ represents the potential dc offset when $m = 0$ and $n = 0$. The first summation part, where $m = 0$ and $n \geq 1$, includes the fundamental component $(n = 1)$ and baseband harmonics $(n > 1)$. The second summation part, where $m \geq 1$ and $n = 0$, corresponds to the central carrier harmonics. The last double summation term, where $m > 1$ and $n \neq 0$, represents several groups of sideband harmonics, which surround their corresponding carrier harmonics.

B. Intrinsic Switching Components Analysis

Defining switching instants for SPWM basing on unit cell theory [80] (pp. 115):

$$x = 2\pi p - \frac{\pi}{2}(1 + M\cos\omega_0 t) \qquad p = 0, 1, 2, \cdots, \infty \tag{5.11}$$

for positive half cycle, and

$$x = 2\pi p + \frac{\pi}{2}(1 + M\cos\omega_0 t) \qquad p = 0, 1, 2, \cdots, \infty \tag{5.12}$$

for negative half cycle.

Then Eq. (5.9) can be substituted as the voltage expression:

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\frac{\pi}{2}(1+M\cos y)}^{\frac{\pi}{2}(1+M\cos y)} V_{dc}e^{j(mx+ny)}\,dx\,dy \tag{5.13}$$

For the dc offset $(m = 0, n = 0)$ in Eq. (5.10), Eq. (5.13) simplifies to:

$$\begin{aligned} A_{00} + jB_{00} &= \frac{V_{dc}}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\frac{\pi}{2}(1+M\cos y)}^{\frac{\pi}{2}(1+M\cos y)} dx\,dy \\ &= \frac{V_{dc}}{2\pi}\int_{-\pi}^{\pi}(1 + M\cos y)dy = V_{dc} \end{aligned} \tag{5.14}$$

For the 1st summation term for fundamental component and baseband harmonics $(m = 0, n \geq 1)$ in Eq. (5.10), Eq. (5.13) can be written as:

$$\begin{aligned} A_{0n} + jB_{0n} &= \frac{V_{dc}}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\frac{\pi}{2}(1+M\cos y)}^{\frac{\pi}{2}(1+M\cos y)} e^{jny}\,dx\,dy \\ &= \frac{V_{dc}}{2\pi}\int_{-\pi}^{\pi}(1 + M\cos y)e^{jny}\,dy \end{aligned} \tag{5.15}$$

Introducing Euler's formula:

$$\cos y = \frac{e^{jy} + e^{-jy}}{2} \tag{5.16}$$

then Eq. (5.15) can be reformed as:

$$A_{0n} + jB_{0n} = \frac{V_{dc}}{2\pi} \int_{-\pi}^{\pi} \left[e^{jny} + \frac{M}{2} e^{j(n+1)y} + \frac{M}{2} e^{j(n-1)y} \right] dy \tag{5.17}$$

Since for every odd function, its integration within an origin-symmetric interval should be zero, which means $\int_{-\pi}^{\pi} e^{jny}\, dy = 0$. Thus $A_{0n} + jB_{0n} = 0$ is set true for all $n > 1$. Except for $n = 1$, in which:

$$A_{01} + jB_{01} = \frac{V_{dc}}{2\pi} \int_{-\pi}^{\pi} \frac{M}{2}\, dy = \frac{V_{dc}}{2} M \tag{5.18}$$

Eq. (5.18) matches the amplitude of reference sinusoidal waveform which is modulation index times half of the dc-link voltage. It is noteworthy that no baseband harmonics exist in actual spectrum.

For the 2nd summation term of central carrier harmonics $(m \geq 1,\ n = 0)$ in Eq. (5.10), Eq. (5.13) can be written as:

$$\begin{aligned} A_{m0} + jB_{m0} &= \frac{V_{dc}}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\frac{\pi}{2}(1+M\cos y)}^{\frac{\pi}{2}(1+M\cos y)} e^{jmx}\, dx\, dy \\ &= \frac{V_{dc}}{2jm\pi^2} \int_{-\pi}^{\pi} \left[e^{jm\frac{\pi}{2}(1+M\cos y)} - e^{-jm\frac{\pi}{2}(1+M\cos y)} \right] dy \end{aligned} \tag{5.19}$$

Introducing a Bessel function integrational relationship in Appendix 2 (pp. 629-633) of [80]:

$$\int_{-\pi}^{\pi} e^{\pm j\xi\cos\theta}\cos n\theta \; d\theta = 2\pi j^{\pm n} J_n(\xi) \tag{5.20}$$

where $J_n(\xi)$ are Bessel functions whose first kind is an even function:

$$J_0(\xi) = J_0(-\xi) \tag{5.21}$$

And Euler's formula can also be given as:

$$j\sin m\frac{\pi}{2} = \frac{e^{jm\frac{\pi}{2}} - e^{-jm\frac{\pi}{2}}}{2} \tag{5.22}$$

Applying Eq. (5.20-22) to Eq. (5.19):

$$\begin{aligned} A_{m0} + jB_{m0} &= \frac{V_{dc}}{jm\pi^2}\left[e^{jm\frac{\pi}{2}} J_0\left(m\frac{\pi}{2}M\right) - e^{-jm\frac{\pi}{2}} J_0\left(-m\frac{\pi}{2}M\right)\right] \\ &= \frac{2V_{dc}}{m\pi} J_0\left(m\frac{\pi}{2}M\right)\sin m\frac{\pi}{2} \end{aligned} \tag{5.23}$$

Similarly, for the 3rd summation term of sideband harmonics $(m > 0,\ n \neq 0)$ in Eq. (5.10), Eq. (5.13) can be ultimately given as:

$$A_{mn} + jB_{mn} = \frac{2V_{dc}}{m\pi} J_n\left(m\frac{\pi}{2}M\right)\sin\left([m+n]\frac{\pi}{2}\right) \tag{5.24}$$

The entire voltage full-component expression of a converter phase leg can be given by combining Eq. (5.14, 5.18, 5.23, 5.24) with Eq. (5.10):

$$\begin{aligned} v_{an}(t) &= \frac{V_{dc}}{2} + \frac{V_{dc}}{2} M\cos(\omega_0 t + \theta_0) \\ &+ \frac{2V_{dc}}{m\pi}\sum_{m=1}^{\infty} J_0\left(m\frac{\pi}{2}M\right)\sin m\frac{\pi}{2}\cos(m[\omega_c t + \theta_c]) \\ &+ \frac{2V_{dc}}{m\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty(n\neq 0)}^{\infty} J_n\left(m\frac{\pi}{2}M\right)\sin\left([m+n]\frac{\pi}{2}\right) \\ &\quad \times\cos(m[\omega_c t + \theta_c] + n[\omega_0 t + \theta_0]) \end{aligned} \tag{5.25}$$

Ignoring the dc offset and integrating the central carrier harmonics and sideband harmonics into carrier band harmonics $(m > 0,\ n \in \mathbb{Z})$, and extracting the intrinsic switching harmonics $f_{sw}(t)$:

$$\begin{aligned} f_{sw}(t) = {} & M\cos(\omega_0 t + \theta_0) \\ & + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{4}{m\pi} J_n\left(m\frac{\pi}{2}M\right)\sin\left([m+n]\frac{\pi}{2}\right) \\ & \times \cos(m[\omega_c t + \theta_c] + n[\omega_0 t + \theta_0]) \end{aligned} \tag{5.26}$$

Defining a magnitude operator $A_{m,n}$:

$$A_{m,n} = \frac{4}{m\pi} J_n\left(m\frac{\pi}{2}M\right)\sin\left([m+n]\frac{\pi}{2}\right) \tag{5.27}$$

Thus Eq. (5.26) can be simplified as:

$$\begin{aligned} f_{sw}(t) = {} & M\cos(\omega_0 t + \theta_0) \\ & + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} A_{m,n}\cos(m[\omega_c t + \theta_c] + n[\omega_0 t + \theta_0]) \end{aligned} \tag{5.28}$$

Eq. (5.28) gives the complete analysis in one converter phase leg of SPWM intrinsic switching components, containing fundamental component and carrier band harmonics.

5.2.2 DC-Link Capacitor Current Harmonics Derivation

DC-bus converter currents $i_{dc,rec}(t)$ and $i_{dc,inv}(t)$ are dc signals that can be treated as the converter ac currents $i_{ac,rec}(t)$ and $i_{ac,inv}(t)$ being modulated by SPWM switching scheme.

For one converter phase leg, the generated dc current can be obtained via multiplying Eq. (5.2) and Eq. (5.28):

$$i_{dc,ph}(t) = i_{ac,ph}(t) \cdot f_{sw}(t) = \tag{5.29}$$

$$I_{ac}\left\{\begin{matrix} M\{\cos(2\omega_0 t + \theta_0 + \beta) + \cos(\theta_0 - \beta)\} \\ +\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} A_{m,n}\left\{\begin{matrix}\cos(2[m\omega_c + n\omega_0]t + m\theta_c + n\theta_0 + \beta)\\ +\cos(m\theta_c + n\theta_0 - \beta)\end{matrix}\right\}\end{matrix}\right\}$$

Then the dc-bus converter current is derived as the summation of every phase leg's current of corresponding rectifier or inverter. The difference between dc-bus rectifier current and dc-bus inverter current determines the dc-link capacitor current as shown in Eq. (5.1), thus it can be given as:

$$i_{dc,cap}(t) = i_{dc,rec}(t) - i_{dc,inv}(t) = \tag{5.30}$$

$$= I_{ac,rec}\sum_{k=0}^{2}\left\{\begin{matrix} M\left\{\cos\left(2\omega_0 t + \frac{2k\pi}{3} + \beta\right) + \cos\left(\frac{2k\pi}{3} - \beta\right)\right\} \\ +\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} A_{m,n}\left\{\begin{matrix}\cos\left(2[m\omega_{cr} + n\omega_0]t + m\theta_{cr} + n\frac{2k\pi}{3} + \beta\right)\\ +\cos\left(m\theta_{cr} + n\frac{2k\pi}{3} - \beta\right)\end{matrix}\right\}\end{matrix}\right\}$$

$$-I_{ac,inv}\sum_{k=0}^{1}\left\{\begin{matrix} M\{\cos(2\omega_0 t + k\pi + \beta) + \cos(k\pi - \beta)\} \\ +\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} A_{m,n}\left\{\begin{matrix}\cos(2[m\omega_{ci} + n\omega_0]t + m\theta_{ci} + nk\pi + \beta)\\ +\cos(m\theta_{ci} + nk\pi - \beta)\end{matrix}\right\}\end{matrix}\right\}$$

For either rectifier and inverter, since only one carrier is used in a converter and modulates all legs, no offset angle exist within a converter.

5.3 Proposed CST for DC-Link Capacitor Current 2nd Carrier Harmonic Reduction

The 2nd central carrier harmonic takes dominance on dc-link capacitor current spectrum, this component can be obtained by setting $m = 2$, $n = 0$ for double summation terms in Eq. (5.30), which is given as:

$$\begin{aligned} i_{dc,cap\ 2^{nd}}(t) &= i_{dc,rec}(t) - i_{dc,inv}(t) \\ &= 3I_{ac,rec}\left\{A_{2,0}\begin{Bmatrix}\cos(4\omega_{cr}t + 2\theta_{cr} + \beta)) \\ +\cos(2\theta_{cr} - \beta)\end{Bmatrix}\right\} \\ &\quad -2I_{ac,inv}\left\{A_{2,0}\begin{Bmatrix}\cos(4\omega_{ci}t + 2\theta_{ci} + \beta)) \\ +\cos(2\theta_{ci} - \beta)\end{Bmatrix}\right\} \end{aligned} \tag{5.31}$$

If a SPWM carrier shifted angle $\Delta\theta_c$ is defined as:

$$\Delta\theta_c = \theta_{cr} - \theta_{ci} \tag{5.32}$$

where θ_{cr} is the offset angle of the carrier in 3-phase AFE rectifier, θ_{ci} is the offset angle of the carrier in H-bridge inverter. $\Delta\theta_c$ uses H-bridge inverter's carrier as the reference and can be shown in Fig. 5.4.

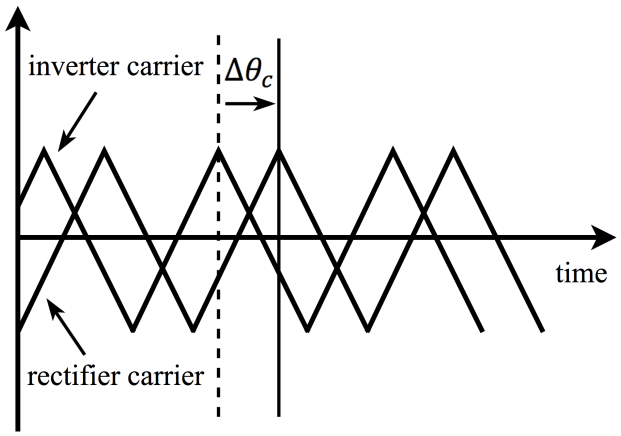


Fig. 5.4 Definition of carrier shifted angle $\Delta\theta_c$.

Then Eq. (5.31) can be substituted as:

$$\begin{aligned} i_{dc,cap\ 2^{nd}}(t) &= i_{dc,rec}(t) - i_{dc,inv}(t) \\ &= 3I_{ac,rec}\left\{A_{2,0}\begin{Bmatrix}\cos(4\omega_{cr}t + 2\Delta\theta_c + 2\theta_{ci} + \beta)) \\ +\cos(2\Delta\theta_c + 2\theta_{ci} - \beta)\end{Bmatrix}\right\} \\ &\quad -2I_{ac,inv}\left\{A_{2,0}\begin{Bmatrix}\cos(4\omega_{ci}t + 2\theta_{ci} + \beta)) \\ +\cos(2\theta_{ci} - \beta)\end{Bmatrix}\right\} \end{aligned} \tag{5.33}$$

It is appropriate to claim that $\Delta\theta_c$ can take the role of adjusting the phase location of the 2nd carrier current harmonic, which can manage the amplitude of this dominant current harmonic component that flows into dc-link capacitors.

This ideology brings on the target of the proposed method: Transferring the dc-link capacitor current harmonic reduction aiming at the 2nd carrier harmonic to an one-variable optimization problem.

For the optimization problem that inspired by Eq. (5.31), an optimization-form expression as Eq. (5.32) can be introduced for showing harmonic reduction ideology.

$$\Delta\theta_c{}^* = \arg\min_{\Delta\theta_c} i_{dc,cap\ 2^{nd}}(t) \tag{5.34}$$

where $\Delta\theta_c{}^*$ is the optimal value of carrier shifted angle $\Delta\theta_c$ that can perform the best harmonic reduction performance. $\Delta\theta_c$ can be any available value in its feasible region. The optimization problem combines both Eq. (5.33) and Eq. (5.34).

Note that because of the periodicity of SPWM scheme, the variation range of $\Delta\theta_c$ should be 180°. In order to avoid repeated equivalent angles, the feasible region of $\Delta\theta_c$ in this thesis is set as:

$$-\frac{\pi}{3} \leq \Delta\theta_c \leq \frac{2\pi}{3} \tag{5.35}$$

Thus the overall optimization problem can be given as a constrained minimization problem:

$$\begin{aligned} \Delta\theta_c{}^* &= \arg\min_{\Delta\theta_c} i_{dc,cap\ 2^{nd}}(t) \\ \text{subject to} \quad & -\frac{\pi}{3} \leq \Delta\theta_c \leq \frac{2\pi}{3} \end{aligned} \tag{5.36}$$

In order to normalize the proposed CST optimization ideology, a detailed procedure of it is summarized as a guideline, the flowchart of optimization procedure is given in Fig. 5.5.

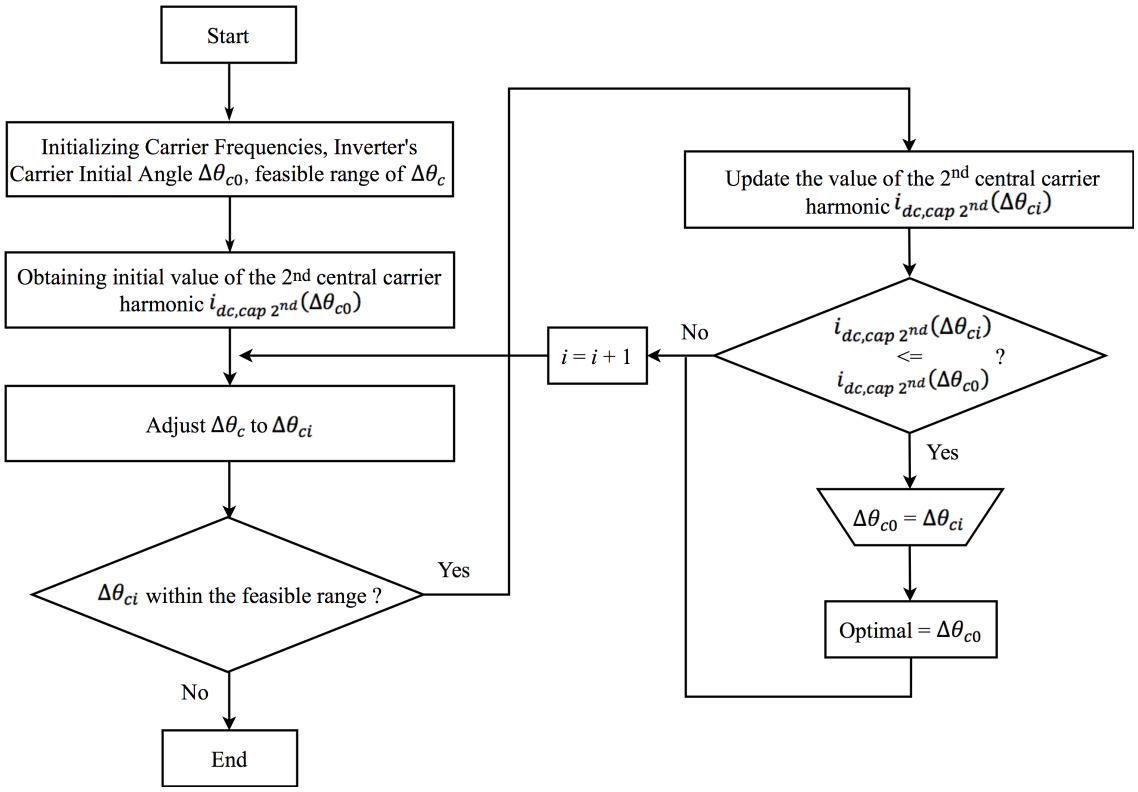


Fig. 5.5 Flowchart of proposed CST with optimization ideology.

Steps of the procedure can be summarized as:

1) Adjust the PWM carrier frequencies of for both 3-phase AFE rectifier and H-bridge inverter.
2) Set the feasible range of carrier shifted angle basing on Eq. (5.35).
3) Set initial inverter's PWM carrier angle and specify it as the reference.
4) Select an initial carrier shifted angle $\Delta\theta_{c0}$ by adjusting rectifier's PWM carrier angle.
5) Obtain the initial value of 2nd central carrier harmonic $i_{dc,cap\ 2^{nd}}(\Delta\theta_{c0})$.
6) Select an available value of carrier shifted angle $\Delta\theta_{ci}$ within feasible range.
7) Update the new value of target harmonic $i_{dc,cap\ 2^{nd}}(\Delta\theta_{ci})$ and compare it with $i_{dc,cap\ 2^{nd}}(\Delta\theta_{c0})$.
8) If it is not the minimum, $\Delta\theta_{c0} = \Delta\theta_{ci}$, $i_{dc,cap\ 2^{nd}}(\Delta\theta_{c0}) = i_{dc,cap\ 2^{nd}}(\Delta\theta_{ci})$; if yes, go to Step 10).
9) $i = i + 1$ and go back to Step 6).
10) Output the optimal carrier shifted angle.

5.4 Simulation Studies of the Proposed Method

Because it is vital to determine the performance of a dc-link capacitor in general long-term motoring condition, the effectiveness of the proposed method is verified in the 3 kV regen CHB MVMD model in motoring mode as shown in chapter 2. Table 5.1 lists the

switching frequencies of PWM carriers that used for dc-bus converters, as well as the total capacitance on dc-link.

TABLE 5.1. SIMULATION PARAMETER CONFIGURATION FOR DC PART

Parameter	Value
3-phase AFE Rectifier Carrier Frequency	1200 Hz
H-bridge Inverter Carrier Frequency	1200 Hz
DC-link Total Capacitance	11300 μF

A. DC-bus Converter Current Carrier Band Harmonics

Fig. 5.6 and Fig. 5.7 show the carrier band harmonics magnitudes on spectrum of $i_{dc,rec}$ and $i_{dc,inv}$ currents on two dc-bus converter. The first three carrier bands are presented.

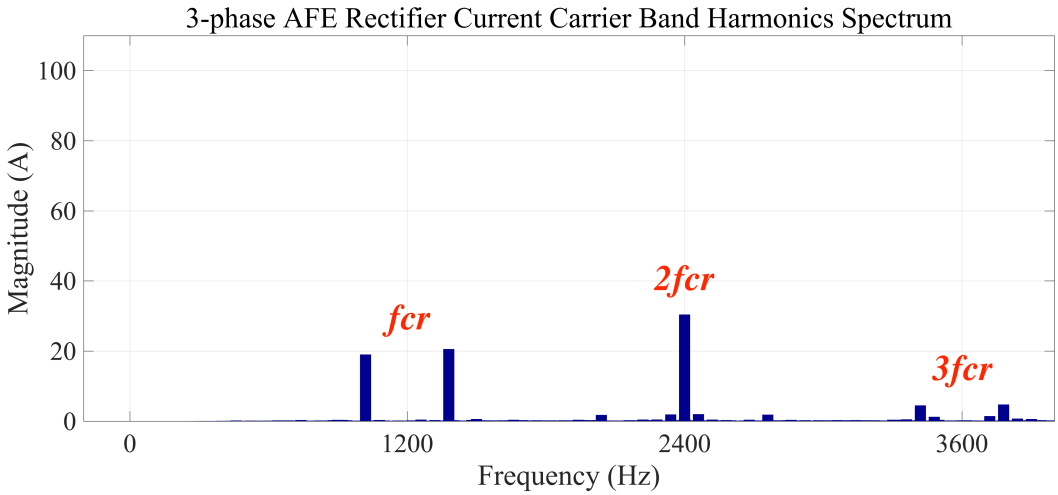


Fig. 5.6 3-phase AFE rectifier current carrier band harmonics spectrum.

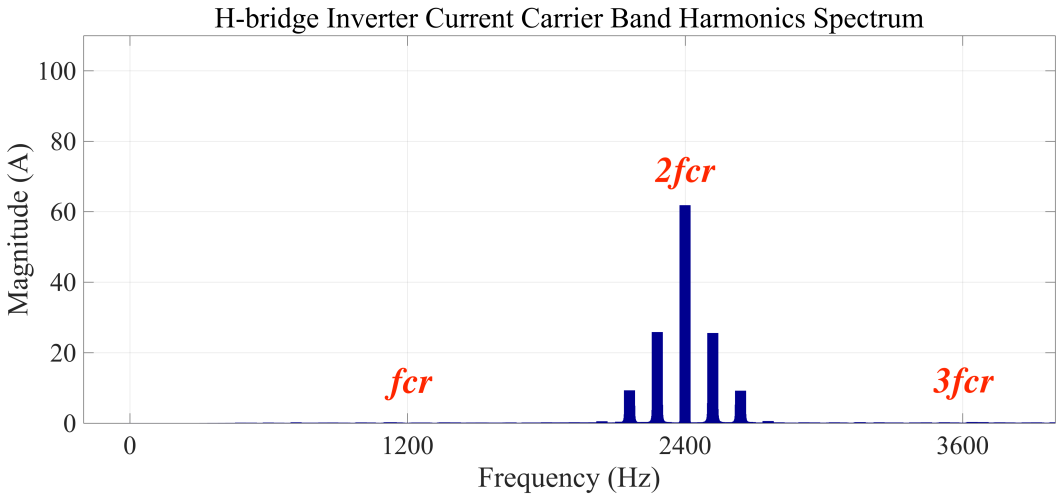


Fig. 5.7 H-bridge inverter current carrier band harmonics spectrum.

For 3-phase AFE rectifier, dominant harmonics locate on the first two carrier bands. There are two main components in the 1st carrier band which locate on 1020 Hz and 1380 Hz, which are $\pm 3^{rd}$ side band $(m = 1,\ n = \pm 3)$ harmonics. In the 2nd carrier band, the central carrier harmonic $(m = 2,\ n = 0)$ is significant and locates on 2400 Hz.

For H-bridge inverter, all the obvious components are in the 2nd carrier band. This group of components is composed with the $\pm 4^{th}$ side band $(m = 2,\ n = \pm 4)$ harmonics on 2160 Hz and 2640 Hz, the $\pm 2^{nd}$ side band $(m = 2,\ n = \pm 2)$ harmonics on 2280 Hz and 2520 Hz, and the 2nd central carrier $(m = 2,\ n = 0)$ harmonic on 2400 Hz.

It is apparent for both dc-bus converter, the 2nd central carrier component appears dominance on entire carrier band harmonics spectrum in terms of magnitude.

B. DC-link Capacitor Current Carrier Band Harmonics

Dc-link capacitor current carrier band harmonics magnitudes without proposed CST are displayed in Fig. 5.8. It can be seen as the combination of two dc-bus converter harmonics.

It is noteworthy that the 2nd central carrier harmonic on dc-link capacitor current indicates a superposition of those two corresponding components in dc-bus converters. Without proposed method, even though they are on the same frequency location, due to the phase difference a significant 2nd central carrier harmonic can be observed.

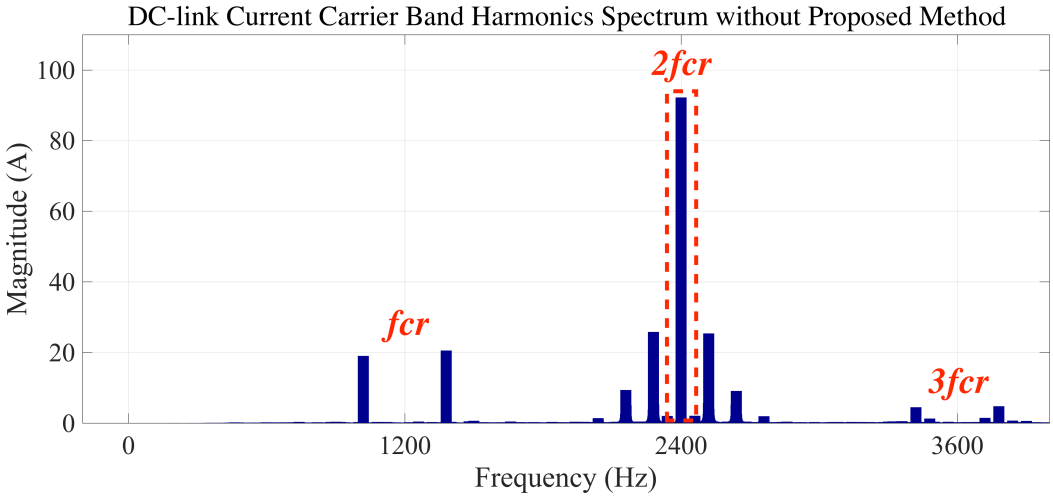


Fig. 5.8 Dc-link capacitor current carrier band harmonics spectrum without CST.

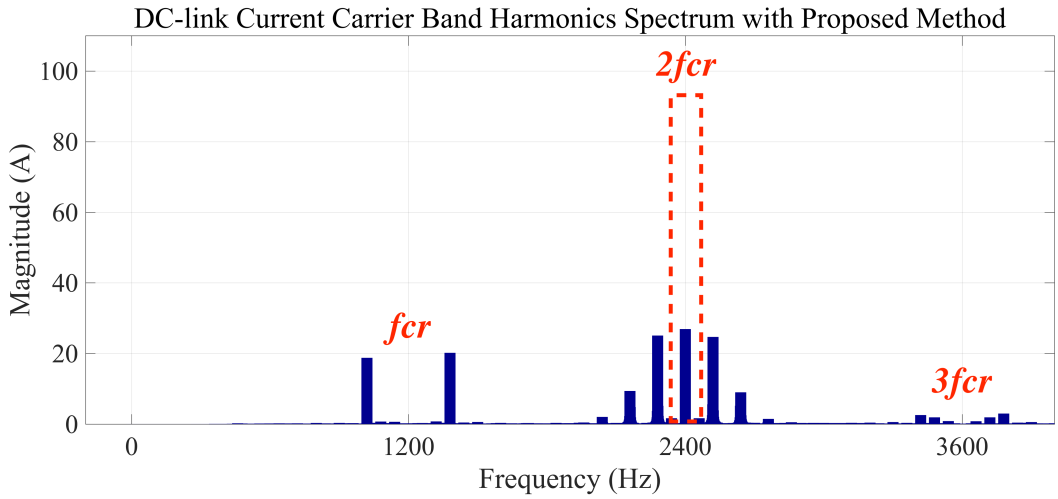


Fig. 5.9 Dc-link capacitor current carrier band harmonics spectrum with CST.

The spectrum with proposed method is shown in Fig. 5.9, by introducing the proposed CST and finding out the optimal value, two dc-bus converter 2nd central carrier harmonics can be subtracted with each other. The final dc-link capacitor 2nd central carrier harmonics is reduced signally.

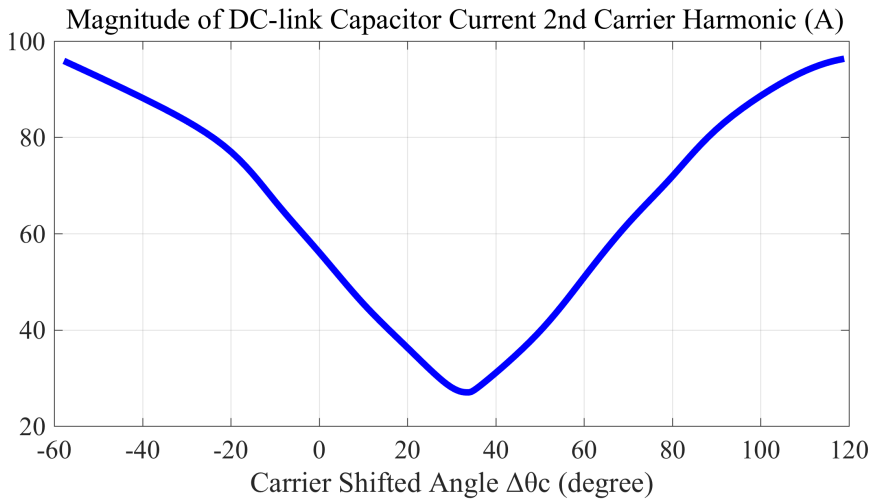


Fig. 5.10 Magnitude of 2nd central carrier harmonic vs. carrier shifted angle.

Varying magnitudes of the dc-link capacitor 2nd carrier harmonic vs. carrier shifted angles $\Delta\theta_c$ is shown in Fig. 5.10. One optimal value of can be found in the feasible range between $[-\pi/3\,,2\pi/3]$. The maximum magnitude of 2nd carrier harmonic is around 95 A without carrier shifted angle optimization method, the minimum magnitude of 2nd carrier harmonic is 25 A, which locates on the optimal $\Delta\theta_c$, a 73.68% reduction on target harmonic component can be achieved.

C. DC-link Capacitor Real Current Comparison

Fig. 5.11 and Fig. 5.12 denote the real currents of dc-link capacitor with/without proposed CST. In Fig. 5.11 some obvious high-order harmonics with considerable magnitudes can be seen in the waveform and they distort the shape of real current waveform. As a comparison, the current waveform with proposed method has less obvious harmonic components, a better real current performance is approved.

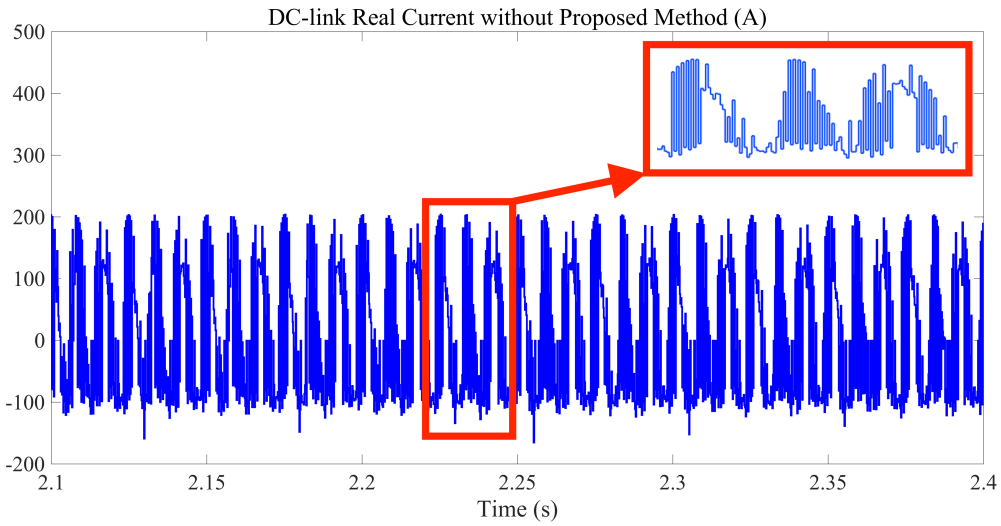


Fig. 5.11 Dc-link capacitor real current without CST.

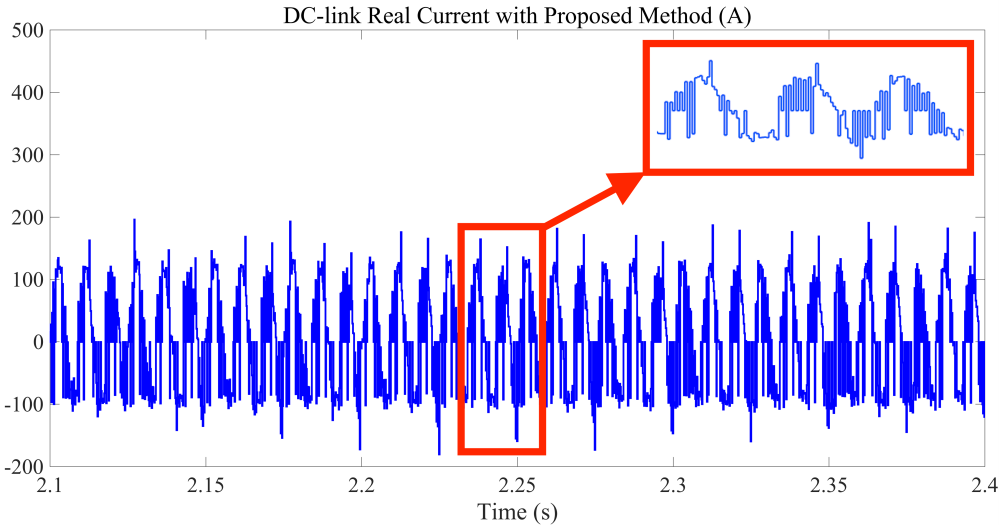


Fig. 5.12 Dc-link capacitor real current with CST.

D. DC-link Capacitor General RMS Current Comparison

General rms currents of dc-link capacitor are shown in Fig. 5.13 as a criterion to judge the effect of proposed method. When the carrier shifted angle optimization doesn't operates, a 103 A rms current is observed in dc-link; with the help of proposed method, dc-link rms

current reduces to 81 A. Proposed CST mitigates the rms current of dc-link capacitor for 21.36%.

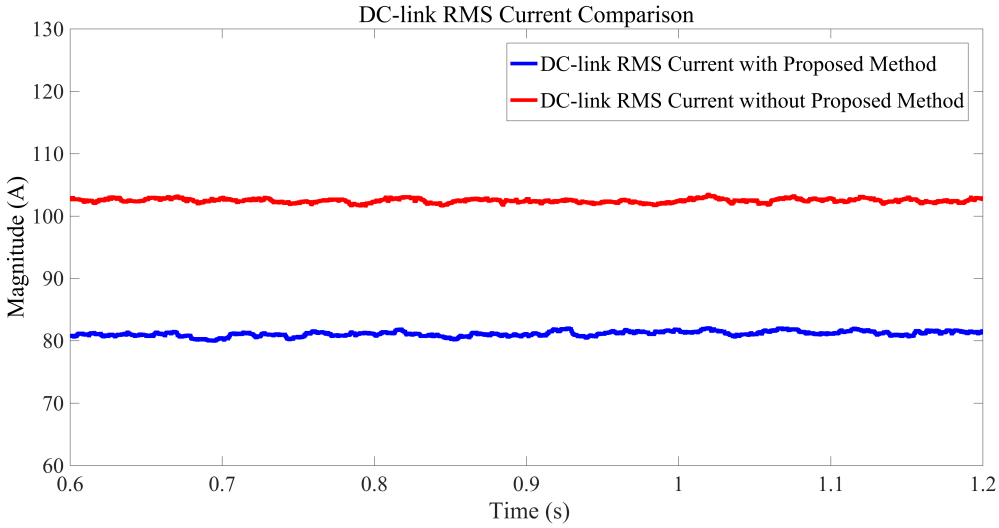


Fig. 5.13 Dc-link capacitor rms current with/without CST.

Simulation results prove the feasibility and effectiveness of the proposed SPWM CST among 3-phase AFE rectifier and H-bridge inverter for a 3 kV regen CHB power cell. By utilizing the method, the 2nd central carrier component on dc-link capacitor can be reduced, and less high-order harmonics appear in real current waveform. The total rms current on dc-link can be reduced by 21.36%.

5.5 Summary

Focusing on the dc-link capacitor current harmonics in regen CHB MVMD power cells, this chapter proposed a 2nd carrier harmonic reduction method by adjusting the SPWM carrier shifted angle between 3-phase AFE rectifier and H-bridge inverter.

First, some existing literatures that proposed by researchers for suppressing dc-link capacitor currents were reviewed. Then the modeling of dc-link capacitor current components were introduced, SPWM scheme one converter phase leg was proposed by using double-variable Fourier transform, intrinsic switching harmonics was extracted to form the harmonic expression for dc-link capacitor current. Successively, an optimization ideology of current harmonic reduction was proposed in order to eliminate the 2nd carrier harmonic of dc-link capacitor current. The proposed method needs less in-computation parameter updates and burdensome algorithms, only requires adjustment of one variable.

Finally, simulation studies for dc-link capacitor bank on a 3 kV 7-level CHB MVMD's power cell were presented. The simulation results proved the feasibility and effectiveness of the proposed method.

In the next chapter, by integrating the proposed CST and the proposed lifetime model for dc-link power capacitors in chapter 4, a trade-off design and analysis of dc-link power capacitor banks in a regen CHB MVMD will be brought forward.

Chapter 6

Lifetime and Power Loss Analysis in DC-link Capacitor Banks for Regenerative Cascaded H-bridge Power Cells

6.1 Capacitor Bank Design for Regen CHB Power Cells

Reasonably stable dc-link voltage on every power cell is a design requirement for induction motor drives. In order to maintain a stable 1100 V dc-link voltage with affordable ripples and good performances of controllers, a total capacitance of 11333 μF is selected for the 3 kV, 140 A, 7-level regen CHB MVMD model that used for simulation studies in Chapter 2. This section will explain design of capacitor banks using Al-Elec capacitors and MPPF capacitors for the given model.

In industry applications, the design of capacitor banks needs to satisfy the demanded total capacitance and sustain the required dc-link voltage. The design concept can be expressed by Eq. (6.1).

$$s = \left\lceil \frac{V_{dc} + V_{safe}}{V_{unit}} \right\rceil$$
$$p = \left\lceil \frac{s \times C_{dc}}{C_{unit}} \right\rceil \quad (6.1)$$

where V_{dc} is required dc-link voltage, V_{safe} is safety margin voltage, V_{unit} is rated voltage of individual capacitor unit. C_{dc} is demanded total capacitance, C_{unit} is rated capacitance of capacitor unit. p, s are number of capacitors in parallel and series respectively.

6.1.1 Al-Elec Capacitor Bank Design

Two Al-Elec capacitor candidates from Jianghai Capacitor Co., Ltd and Hitachi AIC Inc. are selected to build up Al-Elec capacitor banks for the 3 kV, 140A regen CHB MVMD model. Ratings for these two Al-Elec capacitor candidates are listed in Table 6.1.

TABLE 6.1 RATINGS FOR AL-ELEC POWER CAPACITOR CANDIDATES

Manufacturer	MPNs	Unit Capacitance (μF)	Rated Voltage (V)
Jianghai	ECS2GQL182 MVB350090V	1800	400
Hitachi	PL12W132QS BS17WPEC	1300	450

a) Al-Elec Capacitor Bank with Jianghai Capacitors

Considering $V_{dc} = 1100$ V, $V_{safe} = 10\% \cdot V_{dc}$ and $C_{dc} = 11333\ \mu$F, applying Jianghai capacitor's ratings to Eq. (6.1):

$$s = \left\lceil \frac{1100 + 110}{400} \right\rceil = 4$$
$$p = \left\lceil \frac{4 \times 11333}{1800} \right\rceil = 26 \tag{6.2}$$

4 capacitors are needed in series and 26 are needed in parallel to create a reasonable dc-link capacitor bank with Jianghai Al-Elec capacitor candidate. 104 capacitors are required in total.

b) Al-Elec Capacitor Bank with Hitachi Capacitors

Considering $V_{dc} = 1100$ V, $V_{safe} = 10\% \cdot V_{dc}$ and $C_{dc} = 11333\ \mu$F, applying Hitachi capacitor's ratings to Eq. (6.1):

$$s = \left\lceil \frac{1100 + 110}{450} \right\rceil = 3$$
$$p = \left\lceil \frac{3 \times 11333}{1300} \right\rceil = 27 \tag{6.3}$$

3 capacitors are needed in series and 27 are needed in parallel to create a reasonable dc-link capacitor bank with Hitachi Al-Elec capacitor candidate. 81 capacitors are needed in total.

6.1.2 MPPF Capacitor Bank Design

Similarly, two MPPF capacitor candidates from Jianghai Capacitor Co., Ltd and Hitachi Inc. are chosen to create MPPF capacitor banks. Ratings for these two MPPF capacitor candidates are listed in Table 6.2.

TABLE 6.2 RATINGS FOR MPPF POWER CAPACITOR CANDIDATES

Manufacturer	MPNs	Unit Capacitance (μF)	Rated Voltage (V)
Jianghai	FCC03DL107 *H09503*	800	1300
Hitachi	MLC1300V90 7KB116225	900	1300

a) MPPF Capacitor Bank with Jianghai Capacitors

Applying Jianghai MPPF capacitor's ratings into Eq. (6.1) with the demanded values for dc-link:

$$\begin{aligned} s &= \left\lceil \frac{1100 + 110}{1300} \right\rceil = 1 \\ p &= \left\lceil \frac{1 \times 11333}{800} \right\rceil = 15 \end{aligned} \tag{6.4}$$

1 capacitor is needed in series and 15 are needed in parallel to create a reasonable dc-link capacitor bank with Jianghai MPPF capacitor candidate. 15 are required in total.

b) MPPF Capacitor Bank with Hitachi Capacitors

Applying Hitachi MPPF capacitor's ratings into Eq. (6.1) with the demanded values for dc-link:

$$\begin{aligned} s &= \left\lceil \frac{1100 + 110}{1300} \right\rceil = 1 \\ p &= \left\lceil \frac{1 \times 11333}{900} \right\rceil = 13 \end{aligned} \tag{6.5}$$

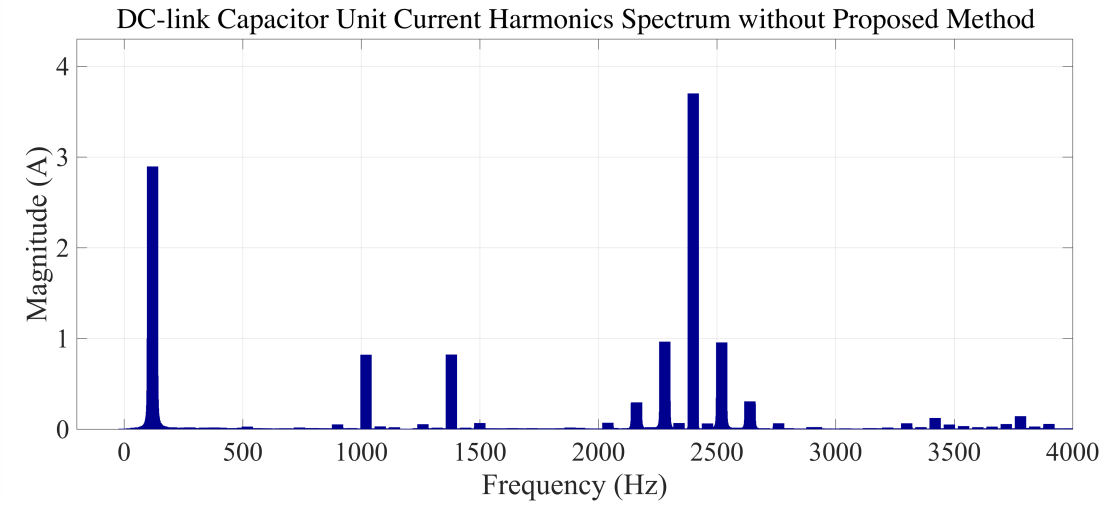
1 capacitor is needed in series and 13 are needed in parallel to create a reasonable dc-link capacitor bank with Hitachi MPPF capacitor candidate. 13 are required in total.

6.2 Analysis of the Proposed CST on DC-link Capacitor Banks

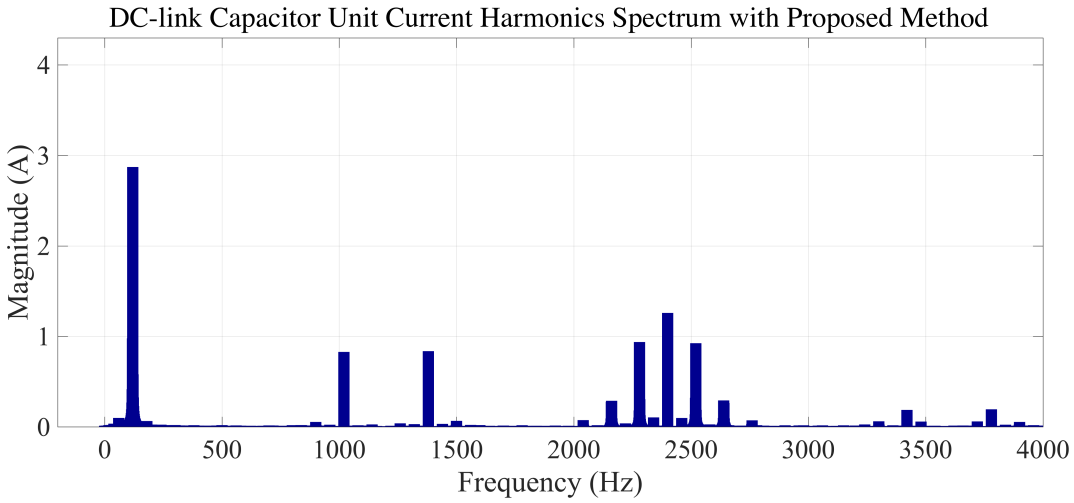
The proposed dc-link current harmonic reduction method (CST), introduced in Chapter 5, is implemented on capacitor banks here. The simulation studies of one capacitor unit in each of the 4 different capacitor banks is used for analysis.

6.2.1 Simulation Studies of Jianghai Al-Elec Capacitor Unit

Fig. 6.1 compares the dc-link capacitor unit current spectrums ranging from 0~4000 Hz of Jianghai Al-Elec capacitor bank, with/without the proposed CST. Detailed values of dominant harmonics are listed in Table 6.3.



(a) Harmonic spectrum without CST.



(b) Harmonic spectrum with CST.

Fig. 6.1 Dc-link current harmonics spectrums of Jianghai Al-Elec capacitor unit.

TABLE 6.3 DOMINANT HARMONICS OF JIANGHAI AL-ELEC CAPACITOR UNIT

Frequency (Hz)		**120**	**1020**	**1380**	**2160**	**2280**	**2400**	**2520**	**2640**
Without CST	**Amplitude (A)**	2.895	0.822	0.823	0.285	0.965	3.699	0.957	0.307
	RMS Value (Arms)	2.047	0.581	0.582	0.202	0.682	2.616	0.677	0.217
With Proposed CST	**Amplitude (A)**	2.870	0.827	0.836	0.276	0.937	1.259	0.924	0.291
	RMS Value (Arms)	2.029	0.585	0.591	0.195	0.663	0.890	0.653	0.206

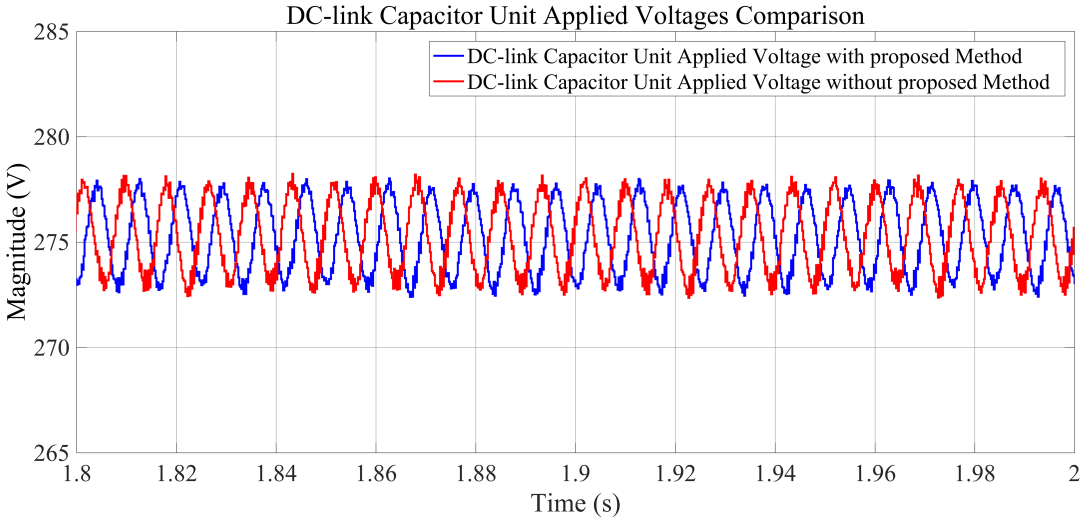
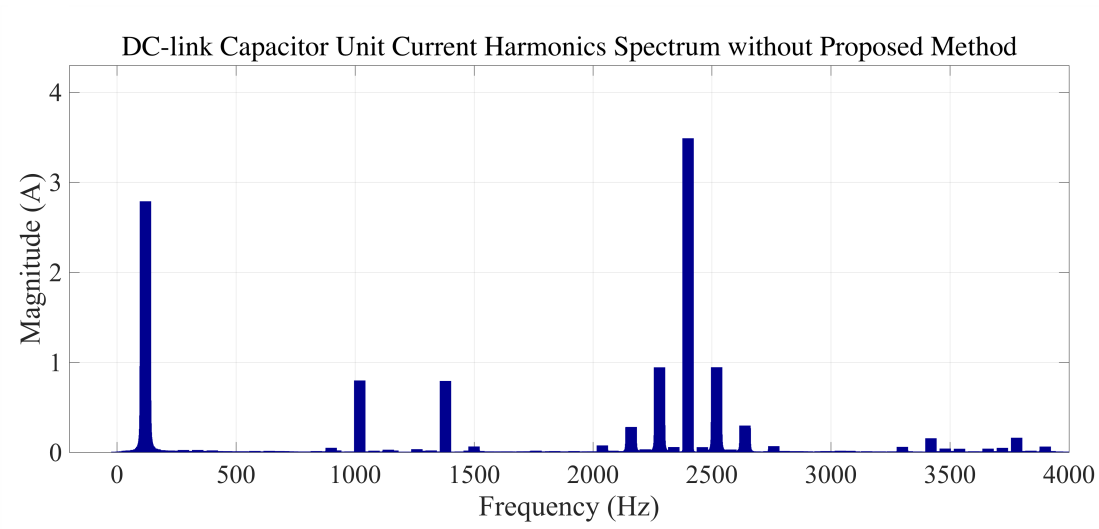


Fig. 6.2 Dc-link applied voltages of Jianghai Al-Elec capacitor unit.

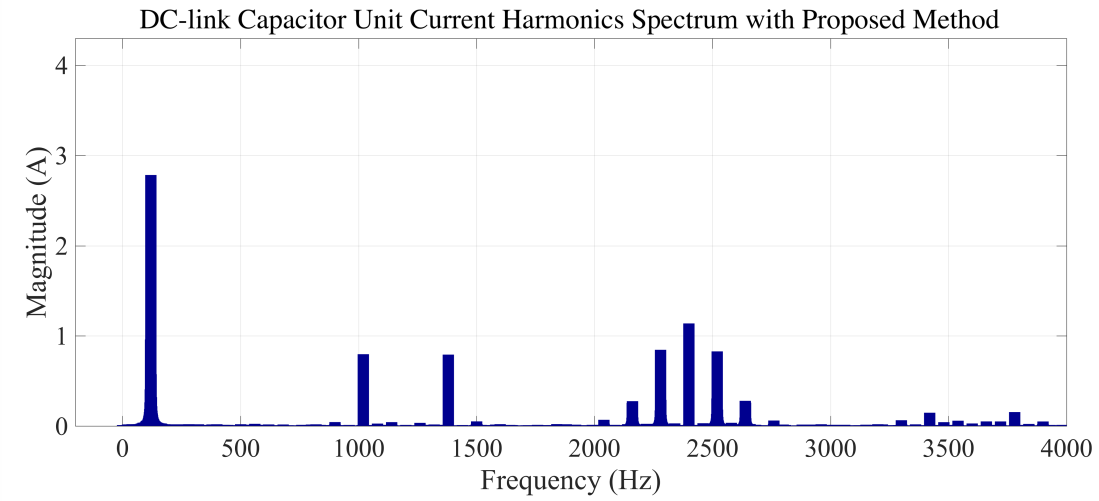
The applied voltages of Jianghai Al-Elec capacitor unit is shown in Fig. 6.2. For both scenarios, a 275 V average value of applied voltage can be seen here.

6.2.2 Simulation Studies of Hitachi Al-Elec Capacitor Unit

Fig. 6.3 shows the dc-link capacitor unit current spectrums of Hitachi Al-Elec capacitor bank, with/without the proposed CST. Detailed values of dominant harmonics are listed in Table 6.4.



(a) Harmonic spectrum without CST.



(b) Harmonic spectrum with CST.

Fig. 6.3 Dc-link current harmonics spectrums of Hitachi Al-Elec capacitor unit.

TABLE 6.4 DOMINANT HARMONICS OF HITACHI AL-ELEC CAPACITOR UNIT

Frequency (Hz)		120	1020	1380	2160	2280	2400	2520	2640
Without CST	**Amplitude (A)**	2.788	0.798	0.793	0.277	0.944	3.489	0.945	0.297
	RMS Value (Arms)	1.971	0.564	0.561	0.196	0.667	2.467	0.668	0.210
With Proposed CST	**Amplitude (A)**	2.783	0.796	0.792	0.255	0.845	1.138	0.828	0.278
	RMS Value (Arms)	1.968	0.563	0.560	0.180	0.598	0.805	0.585	0.197

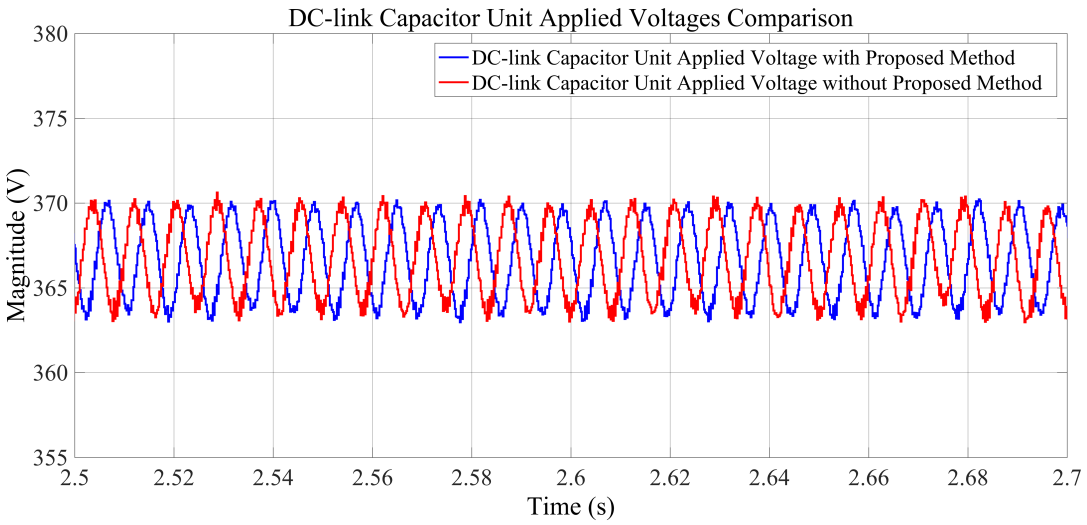
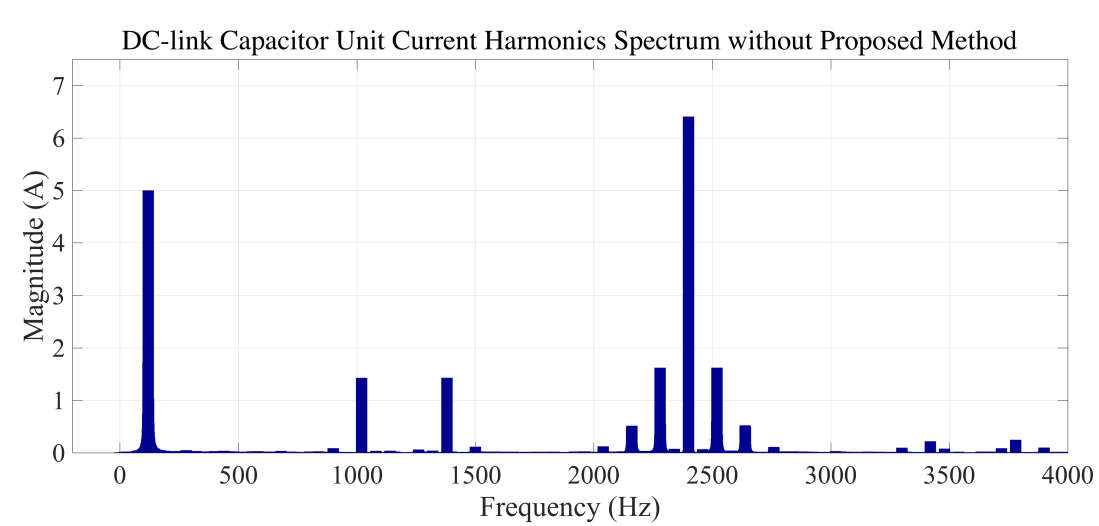


Fig. 6.4 Dc-link applied voltages of Hitachi Al-Elec capacitor unit.

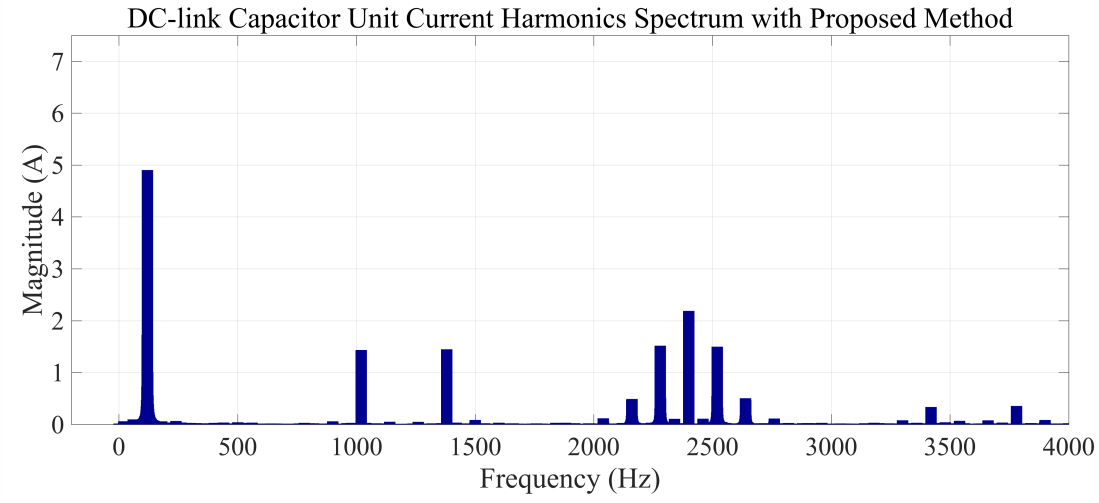
The applied voltages of Hitachi Al-Elec capacitor unit is shown in Fig. 6.4. For both scenarios, a 367 V average value of applied voltage can be seen.

6.2.3 Simulation Studies of Jianghai MPPF Capacitor Unit

Fig. 6.5 shows the capacitor unit current spectrums of Jianghai MPPF capacitor bank, with/without the proposed CST. Dominant harmonics are listed in Table 6.5.



(a) Harmonic spectrum without CST.



(b) Harmonic spectrum with CST.

Fig. 6.5 Dc-link current harmonics spectrums of Jianghai MPPF capacitor unit.

TABLE 6.5 DOMINANT HARMONICS OF JIANGHAI MPPF CAPACITOR UNIT

Frequency (Hz)		**120**	**1020**	**1380**	**2160**	**2280**	**2400**	**2520**	**2640**
Without CST	**Amplitude (A)**	5.017	1.424	1.440	0.510	1.728	6.386	1.728	0.534
	RMS Value (Arms)	3.548	1.007	1.018	0.360	1.222	4.516	1.222	0.378
With Proposed CST	**Amplitude (A)**	4.902	1.435	1.449	0.476	1.518	2.189	1.499	0.505
	RMS Value (Arms)	3.466	1.015	1.025	0.337	1.073	1.548	1.060	0.357

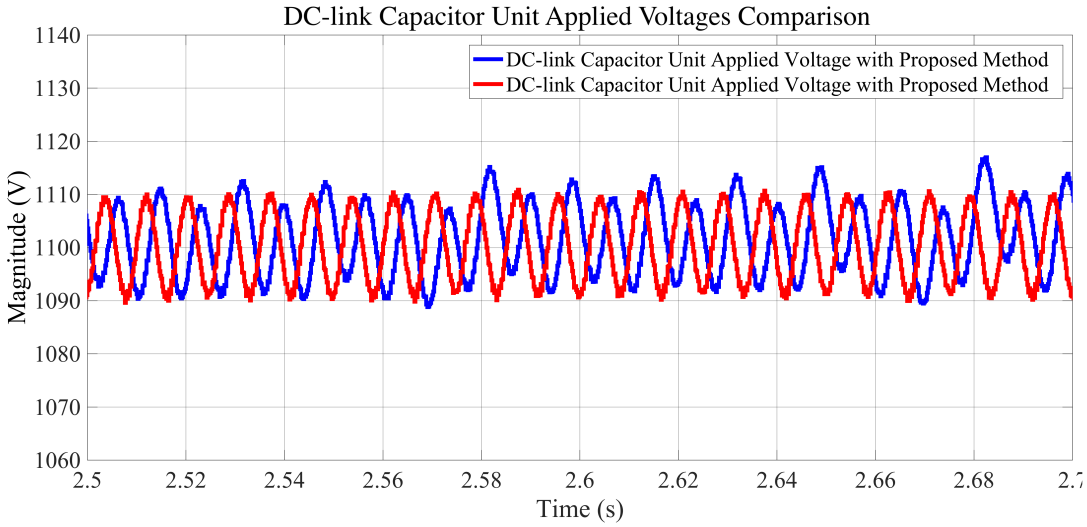
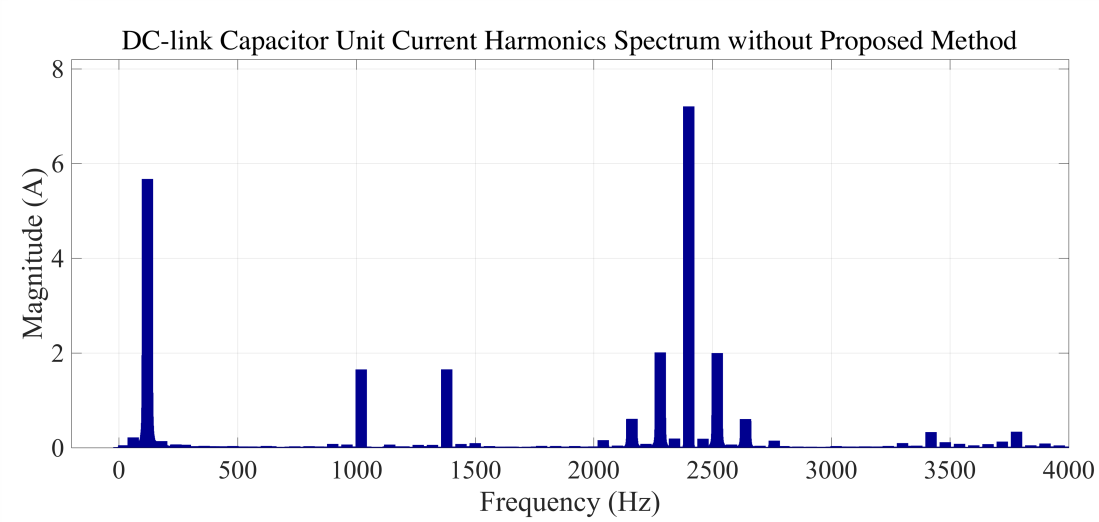


Fig. 6.6 Dc-link applied voltages of Jianghai MPPF capacitor unit.

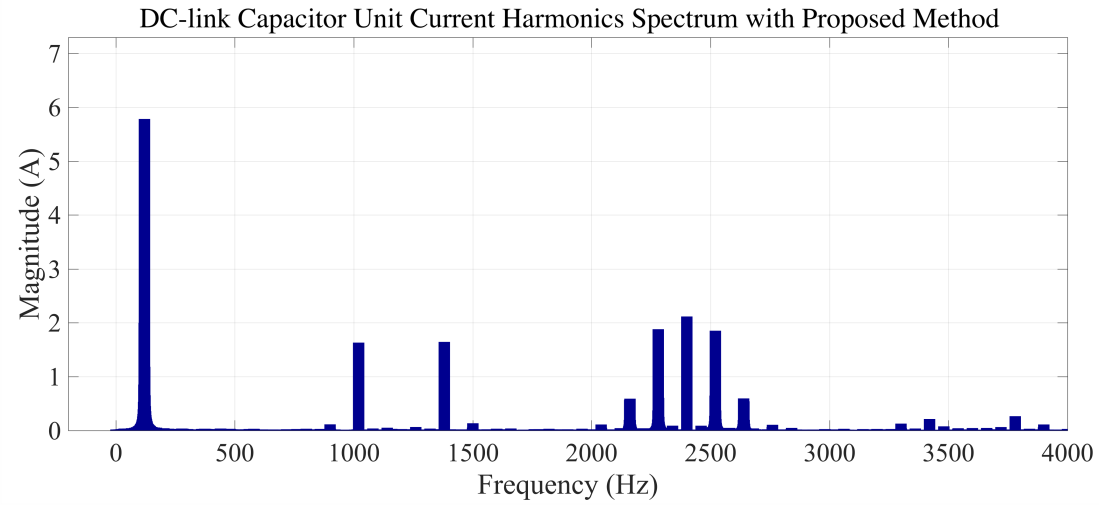
The applied voltages of Jianghai MPPF capacitor unit is shown in Fig. 6.6. For both scenarios, a 1100 V average value of applied voltage can be given.

6.2.4 Simulation Studies of Hitachi MPPF Capacitor Unit

Fig. 6.7 shows the capacitor unit current spectrums of Hitachi MPPF capacitor bank, with/without the proposed CST. Dominant harmonics are listed in Table 6.6.



(a) Harmonic spectrum without CST.



(a) Harmonic spectrum with CST.

Fig. 6.7 Dc-link current harmonics spectrums of Hitachi MPPF capacitor unit.

TABLE 6.6 DOMINANT HARMONICS OF HITACHI MPPF CAPACITOR UNIT

Frequency (Hz)		120	1020	1380	2160	2280	2400	2520	2640
Without CST	**Amplitude (A)**	5.695	1.637	1.643	0.586	2.005	7.177	2.023	0.615
	RMS Value (Arms)	4.027	1.158	1.162	0.414	1.418	5.075	1.430	0.435
With Proposed CST	**Amplitude (A)**	5.795	1.654	1.657	0.560	1.824	2.223	1.791	0.600
	RMS Value (Arms)	4.098	1.169	1.172	0.396	1.290	1.572	1.266	0.424

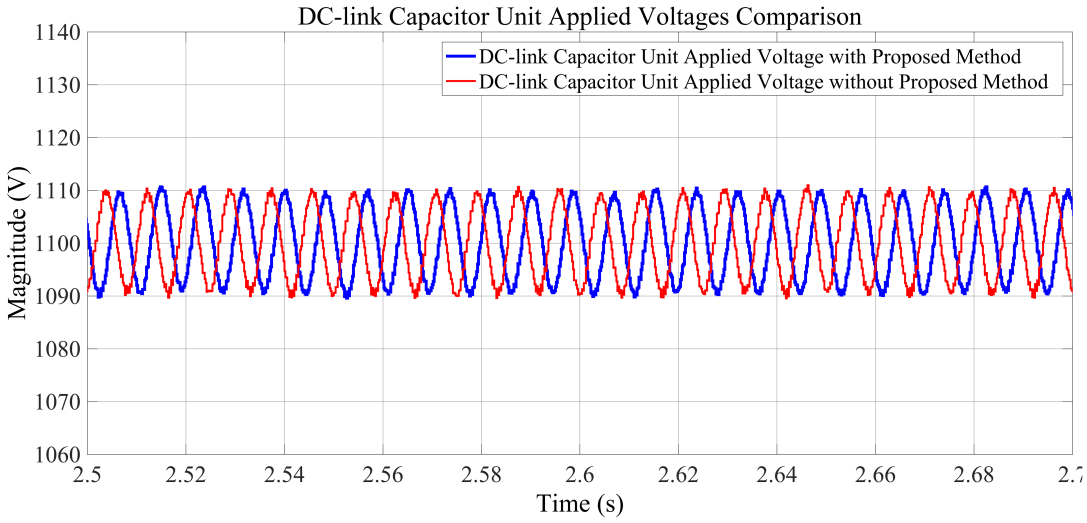


Fig. 6.8 Dc-link applied voltages of Hitachi MPPF capacitor unit.

The applied voltages of Hitachi MPPF capacitor unit is shown in Fig. 6.8. For both scenarios, a 1100 V average value of applied voltage can be given.

6.3 EUL Analysis of DC-link Capacitor Banks

Making use of the proposed EUL model in Chapter 4, effectiveness of the proposed CST in improving capacitor lifetime will be verified in this section. Since the lifetime of capacitor banks relies on the behavior of every individual capacitor, analysis will be done on one capacitor unit in each capacitor bank.

This section will also cover the EUL differences between Al-Elec capacitors and MPPF capacitors.

6.3.1 EUL Analysis of Jianghai Al-Elec Capacitor Unit

6.3.1.1 EUL without Proposed CST

A. Ripple Current Stress Factor

In order to derive the ripple current stress factor, some necessary parameters need to be given first. Recalling Eq. (3.5), equivalent 120-Hz ripple current can be given as:

$$I_r = \sqrt{\sum_{i=1}^{n} \left(\frac{I_{ri}}{f_i \cdot \mu_t \cdot \mu_a} \right)^2} = 1.7774 \text{ A}_{\text{rms}} \tag{6.6}$$

where I_{ri} are 8 dominant current harmonics with different frequencies ($n = 8$), shown as corresponding items in Table 6.3. f_i, μ_t, μ_a are frequency multipliers, temperature multiplier and air cooling multiplier specified by manufacturer.

Considering ambient temperature T_{amb} as 40 °C, so all the necessary parameters are summarized in Table 6.7.

TABLE 6.7 RIPPLE CURRENT RATINGS FOR JIANGHAI AL-ELEC CAPACITOR

Manufacturer	MPNs	I_r^* (Arms)	I_r (Arms)	T_{amb} (°C/K)	ΔT_{core}^* (K)
Jianghai	ECS2GQL182MVB350090V	7.3	1.7774	40/313.15	7.5

Ripple current stress factor for Jianghai Al-Elec capacitor $K_{RC,J,Elec}$ can be calculated by Eq. (4.8):

$$K_{RC,J,Elec} = \exp\left(10908.7\left(\frac{I_r^{*2}}{{I_r}^2\Delta T_{core}^* + I_r^{*2}T_{amb}} - \frac{1}{\Delta T_{core}^* + T_{amb}}\right)\right) = 2.1499 \quad (6.7)$$

B. Ambient Temperature Stress Factor

The necessary parameters for deriving ambient temperature stress factor are summarized in Table 6.8.

TABLE 6.8 AMBIENT TEMPERATURE RATINGS FOR JIANGHAI AL-ELEC CAPACITOR

Manufacturer	MPNs	T_{amb} (°C/K)	T_{amb}^* (°C/K)
Jianghai	ECS2GQL182MVB350090V	40/313.15	85/358.15

Ambient temperature stress factor for Jianghai Al-Elec capacitor $K_{T_{amb},J,Elec}$ can be calculated by Eq. (4.15):

$$K_{T_{amb},J,Elec} \cong 2^{\tau/10} = 2^{\frac{85-40}{10}} = 22.6274 \quad (6.8)$$

C. Applied Voltage Stress Factor

As shown in the conditions of Jianghai Al-Elec capacitor unit, an average applied voltage as 275 V is used here. The necessary parameters for deriving applied voltage stress factor are summarized in Table 6.9.

TABLE 6.9 APPLIED VOLTAGE RATINGS FOR JIANGHAI AL-ELEC CAPACITOR

Manufacturer	**MPNs**	V^* **(V)**	V_a **(V)**
Jianghai	ECS2GQL182MVB350090V	400	275

According to Eq. (4.21), Eq. (4.22), applied voltage stress factor for Jianghai Al-Elec capacitor $K_{V_a,J,Elec}$ can be calculated as:

$$K_{V_a,J,Elec} = \left(\frac{V_a}{V^*}\right)^{-3} = 3.0774 \tag{6.9}$$

D. Humidity Stress Factor

45%~60% relative humidity is the most common situation for general purpose MVMD's working environment, based on Eq. (4.27), humidity stress factor is given as:

$$K_{RH,J,Elec} = 1 \tag{6.10}$$

Combining Eq. (6.7) to (6.10), for this Jianghai Al-Elec capacitor with a 5000 h base lifetime L^*, EUL without the proposed CST can be expressed as:

$$EUL = K_{RC} \cdot K_{T_{amb}} \cdot K_{V_a} \cdot K_{RH} \cdot L^* = 748525.96 \text{ h} \tag{6.11}$$

6.3.1.2 EUL with the Proposed CST

A. Ripple Current Stress Factor

Equivalent 120-Hz ripple current in this condition can be given as:

$$I_r = \sqrt{\sum_{i=1}^{n} \left(\frac{I_{ri}}{f_i \cdot \mu_t \cdot \mu_a} \right)^2} = 1.3833 \text{ A}_{\text{rms}} \quad (6.12)$$

Considering ambient temperature T_{amb} as 40 ℃, so all the necessary parameters are summarized in Table 6.10.

TABLE 6.10 RIPPLE CURRENT RATINGS FOR JIANGHAI AL-ELEC CAPACITOR

Manufacturer	MPNs	I_r^* (Arms)	I_r (Arms)	T_{amb} (℃/K)	ΔT_{core}^* (K)
Jianghai	ECS2GQL182MVB350090V	7.3	1.3833	40/313.15	7.5

With proposed CST, the ripple current stress factor for Jianghai Al-Elec capacitor $K_{RC,J,Elec}$ can be calculated as:

$$K_{RC,J,Elec} = \exp\left(10908.7 \left(\frac{I_r^{*2}}{{I_r}^2 \Delta T_{core}^* + I_r^{*2} T_{amb}} - \frac{1}{\Delta T_{core}^* + T_{amb}} \right) \right) = 2.1921 \quad (6.13)$$

Because the ambient temperature, applied voltage condition and selected relative humidity remain the same, EUL with the proposed CST can be expressed as:

$$EUL = K_{RC} \cdot K_{T_{amb}} \cdot K_{V_a} \cdot K_{RH} \cdot L^* = 763218.64 \text{ h} \quad (6.14)$$

6.3.2 EUL Analysis of Hitachi Al-Elec Capacitor Unit

6.3.2.1 EUL without Proposed CST

A. Ripple Current Stress Factor

Similarly, equivalent 120-Hz ripple current for Hitachi Al-Elec capacitor unit in this condition can be given as:

$$I_r = \sqrt{\sum_{i=1}^{n} \left(\frac{I_{ri}}{f_i \cdot \mu_t \cdot \mu_a} \right)^2} = 1.4733 \text{ A}_{\text{rms}} \quad (6.15)$$

Considering ambient temperature T_{amb} as 40 ℃ as well, all the necessary parameters are summarized in Table 6.11.

TABLE 6.11 RIPPLE CURRENT RATINGS FOR HITACHI AL-ELEC CAPACITOR

Manufacturer	**MPNs**	$\boldsymbol{I_r^*}$ **(Arms)**	$\boldsymbol{I_r}$ **(Arms)**	$\boldsymbol{T_{amb}}$ **(℃/K)**	$\boldsymbol{\Delta T_{core}^*}$ **(K)**
Hitachi	PL12W132QSBS17WPEC	5.41	1.4733	40/313.15	10

Ripple current stress factor for Hitachi Al-Elec capacitor $K_{RC,H,Elec}$ can be calculated by Eq. (4.8):

$$K_{RC,H,Elec} = \exp\left(10908.7 \left(\frac{I_r^{*2}}{{I_r}^2 \Delta T_{core}^* + {I_r^*}^2 T_{amb}} - \frac{1}{\Delta T_{core}^* + T_{amb}} \right) \right) = 2.7066 \quad (6.16)$$

B. Ambient Temperature Stress Factor

The necessary parameters for deriving ambient temperature stress factor are summarized in Table 6.12.

TABLE 6.12 AMBIENT TEMPERATURE RATINGS FOR HITACHI AL-ELEC CAPACITOR

Manufacturer	**MPNs**	$\boldsymbol{T_{amb}}$ **(℃/K)**	$\boldsymbol{T_{amb}^*}$ **(℃/K)**
Hitachi	PL12W132QSBS17WPEC	40/313.15	85/358.15

Ambient temperature stress factor for Hitachi Al-Elec capacitor $K_{T_{amb},H,Elec}$ can be calculated by Eq. (4.15):

$$K_{T_{amb},H,Elec} \cong 2^{\tau/10} = 2^{\frac{85-40}{10}} = 22.6274 \tag{6.17}$$

C. Applied Voltage Stress Factor

As shown in the conditions of Hitachi Al-Elec capacitor unit, an average applied voltage as 367 V is used here. The necessary parameters for deriving applied voltage stress factor are summarized in Table 6.13.

TABLE 6.13 APPLIED VOLTAGE RATINGS FOR HITACHI AL-ELEC CAPACITOR

Manufacturer	**MPNs**	$\boldsymbol{V^*}$ **(V)**	$\boldsymbol{V_a}$ **(V)**
Hitachi	PL12W132QSBS17WPEC	450	367

According to Eq. (4.21), Eq. (4.23), applied voltage stress factor for Hitachi Al-Elec capacitor $K_{V_a,H,Elec}$ can be calculated as:

$$K_{V_a,H,Elec} = \left(\frac{V_a}{V^*}\right)^{-2.5} = 1.6648 \tag{6.18}$$

D. Humidity Stress Factor

For the most common situation for general purpose MVMD's working environment, based on Eq. (4.27), humidity stress factor is given as:

$$K_{RH,H,Elec} = 1 \tag{6.19}$$

Combining Eq. (6.16) to (6.19), for this Hitachi Al-Elec capacitor with a 8000 h base lifetime L^*, EUL without the proposed CST can be expressed as:

$$EUL = K_{RC} \cdot K_{T_{amb}} \cdot K_{V_a} \cdot K_{RH} \cdot L^* = 815663.04 \text{ h} \tag{6.20}$$

6.3.2.2 EUL with the Proposed CST

A. Ripple Current Stress Factor

Similarly, equivalent 120-Hz ripple current for Hitachi Al-Elec capacitor unit in the condition with proposed CST can be given as:

$$I_r = \sqrt{\sum_{i=1}^{n} \left(\frac{I_{ri}}{f_i \cdot \mu_t \cdot \mu_a} \right)^2} = 1.1485 \text{ A}_{\text{rms}} \tag{6.21}$$

Considering ambient temperature T_{amb} as 40 ℃ as well, all the necessary parameters are summarized in Table 6.14.

TABLE 6.14 RIPPLE CURRENT RATINGS FOR HITACHI AL-ELEC CAPACITOR

Manufacturer	**MPNs**	I_r^* **(Arms)**	I_r **(Arms)**	T_{amb} **(℃/K)**	ΔT_{core}^* **(K)**
Hitachi	PL12W132QSBS17WPEC	5.41	1.1485	40/313.15	10

Ripple current stress factor for Hitachi Al-Elec capacitor $K_{RC,H,Elec}$ can be calculated by Eq. (4.8):

$$K_{RC,H,Elec} = \exp\left(10908.7 \left(\frac{I_r^{*2}}{I_r{}^2 \Delta T_{core}^* + I_r^{*2} T_{amb}} - \frac{1}{\Delta T_{core}^* + T_{amb}} \right) \right) = 2.7953 \tag{6.22}$$

For identical ambient temperature, applied voltage condition and selected relative humidity, EUL with the proposed CST can be expressed as:

$$EUL = K_{RC} \cdot K_{T_{amb}} \cdot K_{V_a} \cdot K_{RH} \cdot L^* = 842393.74 \text{ h} \quad (6.23)$$

6.3.3 EUL Analysis of Jianghai MPPF Capacitor Unit

6.3.3.1 EUL without Proposed CST

A. Ripple Current Stress Factor

For Jianghai MPPF capacitor unit, the equivalent 120-Hz ripple current without proposed CST can be given as:

$$I_r = \sqrt{\sum_{i=1}^{n} \left(\frac{I_{ri}}{f_i \cdot \mu_t \cdot \mu_a} \right)^2} = 3.0814 \text{ A}_{\text{rms}} \quad (6.24)$$

Considering ambient temperature T_{amb} as 40 ℃, so all the necessary parameters are summarized in Table 6.15.

TABLE 6.15 RIPPLE CURRENT RATINGS FOR JIANGHAI MPPF CAPACITOR

Manufacturer	**MPNs**	I_r^* **(Arms)**	I_r **(Arms)**	$\frac{E_a}{k_B}$	T_{amb} **(℃/K)**	R_{th} **(K/W)**	ESR **(mΩ)**
Jianghai	FCC03DL107*H09503*	92	3.0814	10800	40/313.15	2.7	1.5

Ripple current stress factor for Jianghai MPPF capacitor $K_{RC,J,MPPF}$ can be calculated by Eq. (4.10):

$$K_{RC,J,MPPF} = \exp\left(\frac{E_a}{k_B} \left(\frac{1}{{I_r}^2 ESR \cdot R_{th} + T_{amb}} - \frac{1}{{I_r^*}^2 ESR \cdot R_{th} + T_{amb}} \right) \right) = 29.9209 \quad (6.25)$$

B. Ambient Temperature Stress Factor

The necessary parameters for deriving ambient temperature stress factor are summarized in Table 6.16.

TABLE 6.16 AMBIENT TEMPERATURE RATINGS FOR JIANGHAI MPPF CAPACITOR

Manufacturer	**MPNs**	$\boldsymbol{\frac{E_a}{k_B}}$	$\boldsymbol{T_{amb}}$ **(℃/K)**	$\boldsymbol{T^*_{amb}}$ **(℃/K)**
Jianghai	FCC03DL107*H09503*	10800	40/313.15	85/358.15

Ambient temperature stress factor for Jianghai MPPF capacitor $K_{T_{amb},J,MPPF}$ can be calculated by Eq. (4.16):

$$K_{T_{amb},J,MPPF} = \exp\left(\frac{E_a}{k_B}\left(\frac{1}{T_{amb}} - \frac{1}{T^*_{amb}}\right)\right) = 76.1954 \tag{6.26}$$

C. Applied Voltage Stress Factor

As shown in the conditions of Jianghai MPPF capacitor unit, 1100 V is the average applied voltage. The necessary parameters for deriving applied voltage stress factor are summarized in Table 6.17.

TABLE 6.17 APPLIED VOLTAGE RATINGS FOR JIANGHAI MPPF CAPACITOR

Manufacturer	**MPNs**	$\boldsymbol{V^*}$ **(V)**	$\boldsymbol{V_a}$ **(V)**
Jianghai	FCC03DL107*H09503*	1300	1100

According to Eq. (4.25), applied voltage stress factor for Jianghai MPPF capacitor $K_{V_a,J,MPPF}$ can be calculated as:

$$K_{V_a,J,MPPF} = \left(\frac{V_a}{V^*}\right)^{-11.7} = 7.0606 \tag{6.27}$$

D. Humidity Stress Factor

For the most common situation for general purpose MVMD's working environment, based on Eq. (4.28), humidity stress factor is given as:

$$K_{RH,J,MPPF} = 1 \tag{6.28}$$

Combining Eq. (6.25) to (6.28), for this Jianghai MPPF capacitor with a 100000 h base lifetime L^*, EUL without the proposed CST can be expressed as:

$$EUL = K_{RC} \cdot K_{T_{amb}} \cdot K_{V_a} \cdot K_{RH} \cdot L^* = 1.6097 \times 10^9 \text{ h} \tag{6.29}$$

6.3.3.2 EUL with Proposed CST

A. Ripple Current Stress Factor

Similarly, equivalent 120-Hz ripple current with proposed CST can be given as:

$$I_r = \sqrt{\sum_{i=1}^{n} \left(\frac{I_{ri}}{f_i \cdot \mu_t \cdot \mu_a}\right)^2} = 2.3590 \text{ A}_{\text{rms}} \tag{6.30}$$

Considering T_{amb} as 40 °C, necessary parameters are summarized in Table 6.18.

TABLE 6.18 RIPPLE CURRENT RATINGS FOR JIANGHAI MPPF CAPACITOR

Manufacturer	**MPNs**	I_r^* **(Arms)**	I_r **(Arms)**	$\frac{E_a}{k_B}$	T_{amb} **(°C/K)**	R_{th} **(K/W)**	ESR **(mΩ)**
Jianghai	FCC03DL107*H09503*	92	2.3590	10800	40/313.15	2.7	1.5

Ripple current stress factor for Jianghai MPPF capacitor $K_{RC,J,MPPF}$ can be calculated by Eq. (4.10):

$$K_{RC,J,MPPF} = \exp\left(\frac{E_a}{k_B}\left(\frac{1}{{I_r}^2 ESR \cdot R_{th} + T_{amb}} - \frac{1}{{I_r^*}^2 ESR \cdot R_{th} + T_{amb}}\right)\right) = 29.9735 \quad (6.31)$$

For the same ambient temperature, applied voltage condition and selected relative humidity, EUL with the proposed CST can be expressed as:

$$EUL = K_{RC} \cdot K_{T_{amb}} \cdot K_{V_a} \cdot K_{RH} \cdot L^* = 1.6125 \times 10^9 \text{ h} \quad (6.32)$$

6.3.4 EUL Analysis of Hitachi MPPF Capacitor Unit

6.3.4.1 EUL without Proposed CST

A. Ripple Current Stress Factor

For Hitachi MPPF capacitor unit, the equivalent 120-Hz ripple current without proposed CST can be given as:

$$I_r = \sqrt{\sum_{i=1}^{n}\left(\frac{I_{ri}}{f_i \cdot \mu_t \cdot \mu_a}\right)^2} = 5.9265 \text{ A}_{\text{rms}} \quad (6.33)$$

Still considering ambient temperature T_{amb} as 40 ℃, necessary parameters are summarized in Table 6.19.

TABLE 6.19 RIPPLE CURRENT RATINGS FOR HITACHI MPPF CAPACITOR

Manufacturer	**MPNs**	$\boldsymbol{I_r^*}$ **(Arms)**	$\boldsymbol{I_r}$ **(Arms)**	$\boldsymbol{\frac{E_a}{k_B}}$	$\boldsymbol{T_{amb}}$ **(℃/K)**	$\boldsymbol{R_{th}}$ **(K/W)**	$\boldsymbol{ESR}$ **(mΩ)**
Hitachi	MLC1300V9 07KB116225	69	5.9265	12000	40/313.15	2.0	2.1

Ripple current stress factor for Hitachi MPPF capacitor $K_{RC,H,MPPF}$ can be calculated by Eq. (4.10):

$$K_{RC,H,MPPF} = \exp\left(\frac{E_a}{k_B}\left(\frac{1}{{I_r}^2 ESR \cdot R_{th} + T_{amb}} - \frac{1}{{I_r^*}^2 ESR \cdot R_{th} + T_{amb}}\right)\right) = 9.7925 \quad (6.34)$$

B. Ambient Temperature Stress Factor

The necessary parameters for deriving ambient temperature stress factor are summarized in Table 6.20.

TABLE 6.20 AMBIENT TEMPERATURE RATINGS FOR HITACHI MPPF CAPACITOR

Manufacturer	**MPNs**	$\boldsymbol{\frac{E_a}{k_B}}$	$\boldsymbol{T_{amb}}$ **(℃/K)**	$\boldsymbol{T^*_{amb}}$ **(℃/K)**
Hitachi	MLC1300V907KB116225	12000	40/313.15	80/353.15

Ambient temperature stress factor for Hitachi MPPF capacitor $K_{T_{amb},H,MPPF}$ can be calculated by Eq. (4.16):

$$K_{T_{amb},H,MPPF} = \exp\left(\frac{E_a}{k_B}\left(\frac{1}{T_{amb}} - \frac{1}{T^*_{amb}}\right)\right) = 76.7381 \quad (6.35)$$

C. Applied Voltage Stress Factor

As shown in the conditions of Hitachi MPPF capacitor unit, 1100 V is the average applied voltage. The necessary parameters for deriving applied voltage stress factor are summarized in Table 6.21.

TABLE 6.21 APPLIED VOLTAGE RATINGS FOR HITACHI MPPF CAPACITOR

Manufacturer	MPNs	V^* (V)	V_a (V)
Jianghai	MLC1300V907KB116225	1300	1100

According to Eq. (4.25), applied voltage stress factor for Hitachi MPPF capacitor $K_{V_a,H,MPPF}$ can be calculated as:

$$K_{V_a,H,MPPF} = \left(\frac{V_a}{V^*}\right)^{-11.6} = 6.9436 \tag{6.36}$$

D. Humidity Stress Factor

For the most common situation for general purpose MVMD's working environment, based on Eq. (4.28), humidity stress factor can also be given as:

$$K_{RH,H,MPPF} = 1 \tag{6.37}$$

Combining Eq. (6.34) to Eq. (6.37), for this Hitachi MPPF capacitor with a 130000 h base lifetime L^*, EUL without the proposed CST can be expressed as:

$$EUL = K_{RC} \cdot K_{T_{amb}} \cdot K_{V_a} \cdot K_{RH} \cdot L^* = 6.2831 \times 10^8 \text{ h} \tag{6.38}$$

6.3.4.2 EUL with Proposed CST

A. Ripple Current Stress Factor

The equivalent 120-Hz ripple current with proposed CST can be given as:

$$I_r = \sqrt{\sum_{i=1}^{n} \left(\frac{I_{ri}}{f_i \cdot \mu_t \cdot \mu_a}\right)^2} = 4.6760 \text{ A}_{\text{rms}} \tag{6.39}$$

Still considering ambient temperature T_{amb} as 40 ℃, necessary parameters are summarized in Table 6.22.

TABLE 6.22 RIPPLE CURRENT RATINGS FOR HITACHI MPPF CAPACITOR

Manufacturer	**MPNs**	$\boldsymbol{I_r^*}$ **(Arms)**	$\boldsymbol{I_r}$ **(Arms)**	$\boldsymbol{\frac{E_a}{k_B}}$	$\boldsymbol{T_{amb}}$ **(℃/K)**	$\boldsymbol{R_{th}}$ **(K/W)**	$\boldsymbol{ESR}$ **(mΩ)**
Hitachi	MLC1300V9 07KB116225	69	4.6760	12000	40/313.15	2.0	2.1

Ripple current stress factor for Hitachi MPPF capacitor $K_{RC,H,MPPF}$ can be calculated by Eq. (4.10):

$$K_{RC,H,MPPF} = \exp\left(\frac{E_a}{k_B}\left(\frac{1}{{I_r}^2 ESR \cdot R_{th} + T_{amb}} - \frac{1}{{I_r^*}^2 ESR \cdot R_{th} + T_{amb}}\right)\right) = 9.8635 \quad (6.40)$$

For the same ambient temperature, applied voltage condition and selected relative humidity, EUL with the proposed CST can be expressed as:

$$EUL = K_{RC} \cdot K_{T_{amb}} \cdot K_{V_a} \cdot K_{RH} \cdot L^* = 6.8324 \times 10^8 \text{ h} \quad (6.41)$$

6.3.5 Summary

Table 6.23 presents the EUL comparisons in these 4 dc-link power capacitor banks. What is worth noticing is that the lifetime extension capability of the proposed CST and EUL differences between Al-Elec capacitors and MPPF capacitors.

14692.68 h and 26730.7 h prolonged EULs could be expected for Jianghai Al-Elec capacitor banks and Hitachi Al-Elec capacitor banks respectively. For MPPF capacitors

from Jianghai and Hitachi, proposed CST could extend EULs for 2.8×10^6 h and 5.5×10^7 respectively.

TABLE 6.23 EUL COMPARISONS BETWEEN DC-LINK CAPACITOR BANKS

Manufacturer	**Capacitor Type**	**MPNs**	**EUL without CST (h)**	**EUL with CST (h)**	**EUL Extension (h)**	**EUL Extension (%)**
Jianghai	Al-Elec	ECS2GQL182 MVB350090V	748525.96	763218.64	14692.68	1.96
	MPPF	FCC03DL107* H09503*	1.6097×10^9	1.6125×10^9	2.8×10^6	0.17
Hitachi	Al-Elec	PL12W132QS BS17WPEC	815663.04	842393.74	26730.7	3.28
	MPPF	MLC1300V9 07KB116225	6.2831×10^8	6.8324×10^8	5.5×10^7	8.75

Huge differences in order of magnitude exist between MPPF capacitors' EULs and Al-Elec capacitors' EULs. Thanks to the magnificent ripple current ratings of MPPF capacitors, the actual lifetimes of them can easily each to their physical upper limits in practice.

By replacing Al-Elec power capacitors with MPPF power capacitors, regen CHB power cells' lifetime performance would be improved significantly, better reliability of regen CHB MVMD is expectable.

6.4 Power Loss Analysis of DC-link Capacitor Banks

By using the proposed CST, reductions on rms currents of dc-link power capacitor unit can also guarantee less power loss in regen CHB power cells. In this section, the advantage of CST in terms of power loss reduction will be given for the 4 different capacitor banks. Power loss differences between Al-Elec capacitors and MPPF capacitors will be mentioned as well.

General rms currents show the effectiveness as judgements. Equivalent 120-Hz rms currents will be used for power loss calculation, since ESRs in capacitor ratings are all defined on 120 Hz. The total power loss in all the banks will be calculated in order to reveal the effect in system level.

6.4.1 Power Loss Reduction of Jianghai Al-Elec Capacitor Unit

Fig. 6.9 makes a comparison between general rms currents of Jianghai Al-Elec capacitor unit with and without CST. By using the proposed CST, general rms current can be reduced by 21.95%, from 4.1 A to 3.2 A.

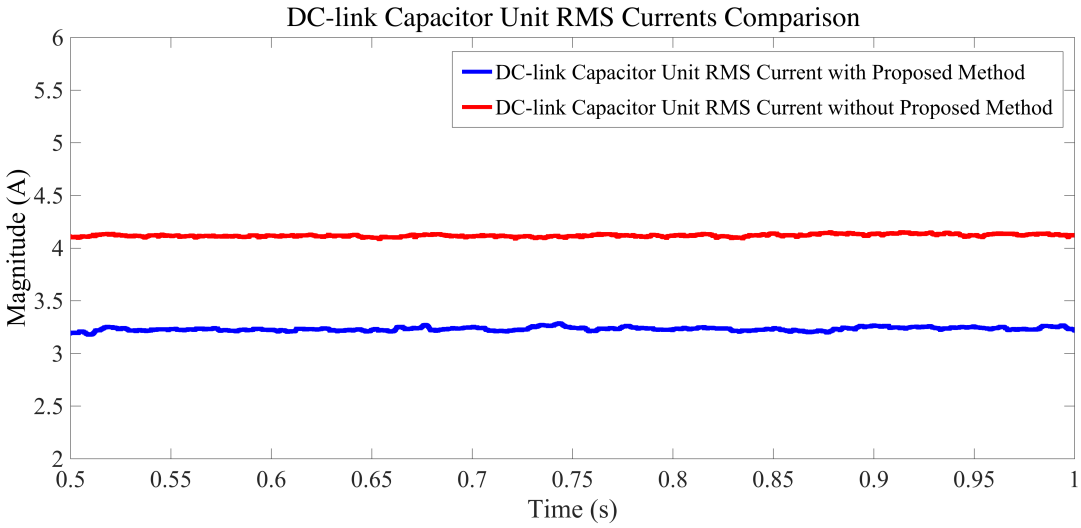


Fig. 6.9 Dc-link general rms currents comparison of Jianghai Al-Elec capacitor unit.

Parameters for power loss calculation is listed in Table 6.24, which is consisted of equivalent 120-Hz rms currents in both conditions, ESR in 120 Hz and total number of capacitor units in all the capacitor banks.

TABLE 6.24 POWER LOSS RATINGS FOR JIANGHAI AL-ELEC CAPACITOR

Manufacturer	**MPN**	**I_r without CST (Arms, 120 Hz)**	**I_r with CST (Arms, 120 Hz)**	**ESR (mΩ, 120 Hz)**	**Quantity of Caps (pcs)**
Jianghai	ECS2GQL182 MVB350090V	1.7764	1.3833	77	4×26×9

There are 9 power cells in the given regen CHB MVMD and each of them has 4 capacitors in series, 26 capacitors in parallel with Jianghai Al-Elec capacitors in every dc-link. The total rms-current-generated power loss W_r with/without CST can be given as:

$$W_{r,non-CST} = 936 \times {I_{r,non-CST}}^2 \cdot ESR = 227.43\ \text{W}$$

$$W_{r,CST} = 936 \times {I_{r,CST}}^2 \cdot ESR = 137.91\ \text{W}$$

A power loss reduction of 89.52 W, 39.36% can be anticipated by using the proposed CST in Jianghai Al-Elec capacitor banks.

6.4.2 Power Loss Reduction of Hitachi Al-Elec Capacitor Unit

Fig. 6.10 compares the dc-link general rms currents of Hitachi Al-Elec capacitor unit. By using the proposed CST, general rms current is reduced by 20.51%, from 3.9 A to 3.1 A. Parameters for power loss calculation is listed in Table 6.25.

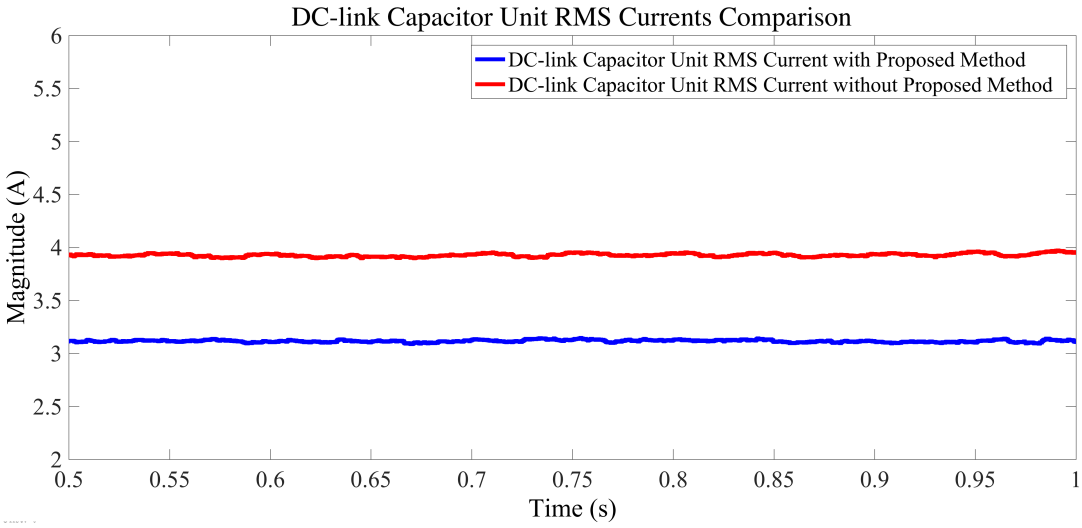


Fig. 6.10 Dc-link general rms currents comparison of Hitachi Al-Elec capacitor unit.

TABLE 6.25 POWER LOSS RATINGS FOR HITACHI AL-ELEC CAPACITOR

Manufacturer	**MPN**	**I_r without CST (Arms, 120 Hz)**	**I_r with CST (Arms, 120 Hz)**	**ESR (mΩ, 120 Hz)**	**Quantity of Caps (pcs)**
Hitachi	PL12W132Q SBS17WPEC	1.4733	1.1485	80	3×27×9

Each of the 9 power cells has 3 capacitors in series, 27 capacitors in parallel with Hitachi Al-Elec capacitors in each dc-link. The total rms-current-generated power loss W_r with/without CST can be given as:

$$W_{r,non-CST} = 729 \times {I_{r,non-CST}}^2 \cdot ESR = 126.59\ \text{W}$$

$$W_{r,CST} = 729 \times {I_{r,CST}}^2 \cdot ESR = 76.93\ \text{W}$$

A power loss reduction of 49.66 W, 39.23% can be expected by using the proposed CST in Hitachi Al-Elec capacitor banks.

6.4.3 Power Loss Reduction of Jianghai MPPF Capacitor Unit

Fig. 6.11 shows the dc-link general rms currents of Jianghai MPPF capacitor unit. By using the proposed CST, general rms current is reduced by 22.54%, from 7.1 A to 5.5 A. Parameters for power loss calculation is listed in Table 6.26.

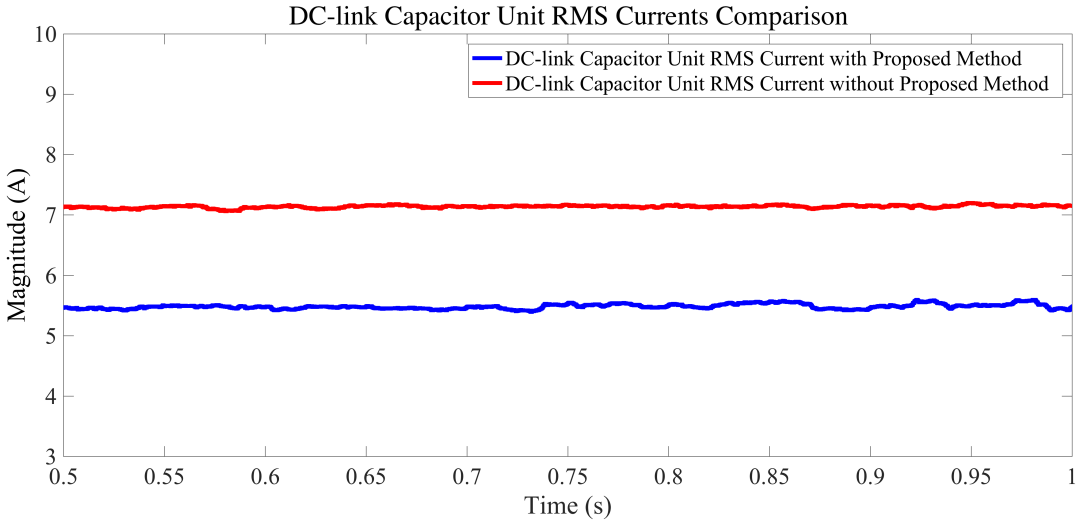


Fig. 6.11 Dc-link general rms currents comparison of Jianghai MPPF capacitor unit.

TABLE 6.26 POWER LOSS RATINGS FOR JIANGHAI MPPF CAPACITOR

Manufacturer	**MPN**	**I_r without CST (Arms, 120 Hz)**	**I_r with CST (Arms, 120 Hz)**	**ESR (mΩ, 120 Hz)**	**Quantity of Caps (pcs)**
Hitachi	FCC03DL107*H09503*	3.0814	2.3590	1.5	1×15×9

Each of the 9 regen CHB power cells has 1 capacitor in series, 15 capacitors in parallel with Jianghai MPPF capacitors in each dc-link. The total rms-current-generated power loss W_r with/without CST can be given as:

$$W_{r,non-CST} = 135 \times {I_{r,non-CST}}^2 \cdot ESR = 1.92\ \text{W}$$

$$W_{r,CST} = 135 \times {I_{r,CST}}^2 \cdot ESR = 1.13\ \text{W}$$

A power loss reduction of 0.79 W, 41.15% can be expected by using the proposed CST in Jianghai MPPF capacitor banks.

6.4.4 Power Loss Reduction of Hitachi MPPF Capacitor Unit

Fig. 6.12 compares the dc-link general rms currents of Hitachi MPPF capacitor unit. By using the proposed CST, general rms current is reduced by 21.95%, from 8.2 A to 6.4 A. Parameters for power loss calculation is listed in Table 6.27.

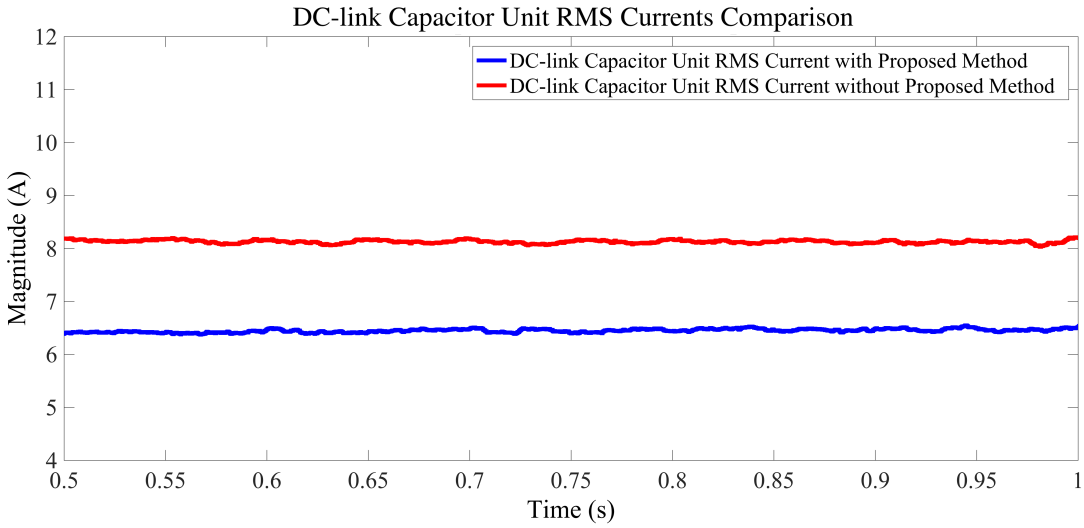


Fig. 6.12 Dc-link general rms currents comparison of Hitachi MPPF capacitor unit.

TABLE 6.27 POWER LOSS RATINGS FOR HITACHI MPPF CAPACITOR

Manufacturer	**MPN**	**I_r without CST (Arms, 120 Hz)**	**I_r with CST (Arms, 120 Hz)**	**ESR (mΩ, 120 Hz)**	**Quantity of Caps (pcs)**
Hitachi	MLC1300V9 07KB116225	5.9265	4.6760	2.1	1×13×9

Each of the 9 power cells in a regen CHB MVMD has 1 capacitor in series, 13 capacitors in parallel with Hitachi MPPF capacitors in every dc-link. The total rms-current-generated power loss W_r with/without CST can be given as:

$$W_{r,non-CST} = 117 \times {I_{r,non-CST}}^2 \cdot ESR = 8.63\ \text{W}$$

$$W_{r,CST} = 117 \times {I_{r,CST}}^2 \cdot ESR = 5.37\ \text{W}$$

A power loss reduction of 3.26 W, 37.78% can be expected by using the proposed CST in Hitachi MPPF capacitor banks.

6.4.5 Summary

Table 6.28 listed the total power losses of the 4 dc-link power capacitor banks. By using the proposed CST, thermal power dissipated in capacitors can be reduced for every capacitor bank.

Higher applied voltage ratings of MPPF capacitors cut down the number of capacitor units in power cells. Furthermore, taking advantages of extraordinarily small ESRs in MPPF capacitors, power losses in MPPF capacitor bank candidates are way less than those in Al-Elec candidates in this thesis.

TABLE 6.28 POWER LOSS COMPARISONS BETWEEN DC-LINK CAPACITOR BANKS

Manufacturer	Capacitor Type	MPNs	Power Loss without CST (W)	Power Loss with CST (W)	Power Loss Reduction (W)	Power Loss Reduction (%)
Jianghai	Al-Elec	ECS2GQL182 MVB350090V	227.43	137.91	89.52	39.36
	MPPF	FCC03DL107* H09503*	1.92	1.13	0.79	41.15
Hitachi	Al-Elec	PL12W132QS BS17WPEC	126.59	76.93	49.66	39.23
	MPPF	MLC1300V9 07KB116225	8.63	5.37	3.26	37.78

6.5 Summary

In this chapter, in order to design competent dc-link capacitor banks for regen CHB power cells, the demanded dc-link voltage level and required total capacitance are two essential criteria and are used in capacitor bank design.

By selecting Al-Elec capacitor candidate and MPPF capacitor candidate from Jianghai Capacitor Co., Ltd and Hitachi AIC Inc. respectively, 4 different dc-link capacitor banks in total were delivered for analysis.

For the sake of expressing the merits of proposed CST, in every capacitor bank, the simulation studies of one capacitor unit with respect to current harmonic contents and applied voltages were given.

With the help of the proposed EUL models in Chapter 4, further analysis of capacitor lifetimes in simulation condition were presented. CST can reduce the equivalent 120-Hz rms currents for capacitors, which means better ripple current performances and longer EUL can be anticipated. Generally, MPPF capacitors possess longer lifetime due to their better ripple current ratings.

Power losses of capacitor banks were also calculated in system level, less thermal power loss showed up when using CST in each bank. Al-Elec capacitor banks have more power losses than MPPF capacitor banks in the same conditions, because they have bigger ESRs, and more capacitors were involved in capacitor bank composing.

Chapter 7

Experimental Prototype and Experiment Studies

7.1 Introduction of Prototype

Experiment studies of the proposed CST for regen CHB MVMD are delivered with a 10 kW RL load, on a scaled-down prototype. Switching frequencies for both converter sides are chosen as 1200 Hz. The prototype is shown in Fig. 7.1, it is a 3-phase, 7-level regen CHB topology, 3 cells exist in each phase. Dc-link voltages are controlled as 160 V to fit load conditions, maximum output line-to-line rms voltage of regen CHB inverter is 600 V.

Fig. 7.1 Overview of experimental prototype.

7.1.1 7-level Regen CHB Inverter

Fig. 7.2 shows the layout of 7-level CHB inverter, there are three phases in this topology, each of them has 3 power cells cascaded in series, cells in phase A are pointed as references. Some main components in this topology will be introduced.

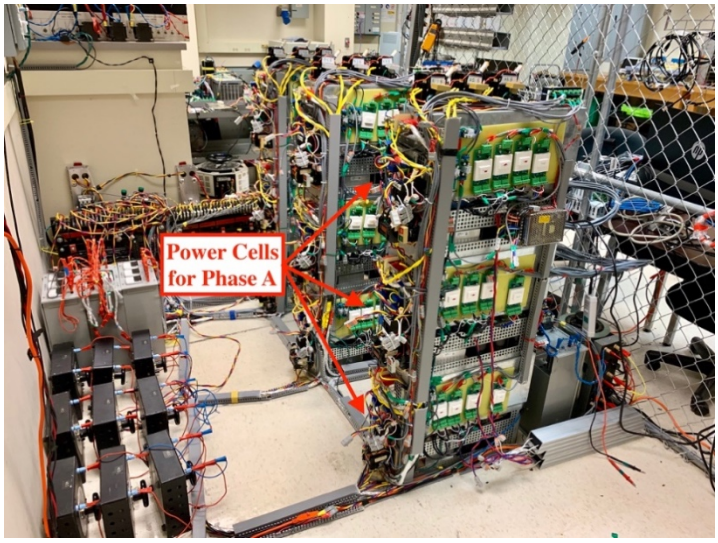
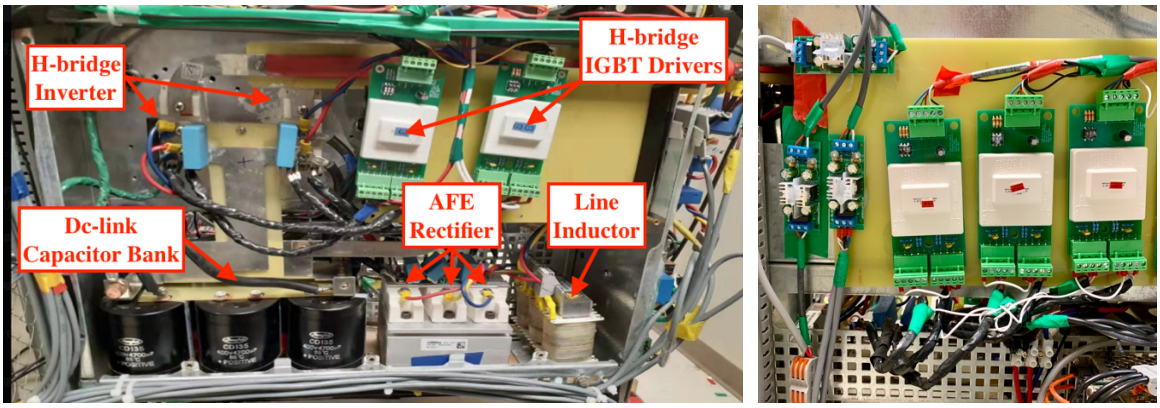


Fig. 7.2 Layout of 3-phase 7-level CHB inverter.



(a) Front side regen CHB power cell. (b) AFE IGBT gate drivers.

Fig. 7.3 Layout of regen CHB power cell.

Fig. 7.3 (a) presents the front side design of regen CHB power cell. A 3-phase line inductor performs as the filter, taking 3-phase voltage to AFE rectifier. Three AFE IGBT drivers are on the back side of cell case, as shown in Fig. 7.3 (b). Dc-link capacitor bank is consisted of 6 electrolytic capacitors, 2 in parallel and 3 in series, creating a 3200 μF total capacitance. H-bridge inverter has two IGBT modules, which are controlled by two IGBT drivers. Each IGBT module is parallel connected with a snubber capacitor in case of inrush currents. High power components in the power cells are connected via bus bars.

7.1.2 IGBT Module

Fig. 7.4 shows the IGBT module 1200V/50A, Semikron, SKM 50GB12T4, that used in regen CHB inverter. Two IGBTs are connected in series to create a half-bridge module. The collector-to-emitter voltage rating is 1200 V, representing the maximum voltage that

can be applied across IGBTs. Maximum affordable switching frequency of this module is 20 kHz.

Fig. 7.4 Half-bridge IGBT module.

7.1.3 Phase-shifting Transformer

Fig. 7.5 shows the autotransformer used for the prototype. The primary-side input line-to-line rms voltage is 240 V, the secondary-side output line-to-line rms voltage is set as 80 V.

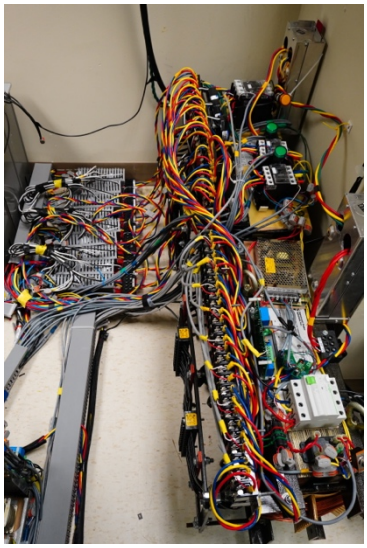


Fig. 7.5 Phase-shifting transformer.

7.1.4 Sensors and Contactors

Fig. 7.6 shows the arrangement of in-set up high-accuracy sensors and contactors for a regen CHB power cell. 2-channel current sensor monitors the input currents. Each channel has a sensor with one winding for measurement, and another with two windings for protection. 4-channel voltage sensor measures the 3-phase ac input voltages and dc-link voltage. These two sensors can transfer the actual V/I into -10~10 V voltage signals, with < 0.5% accuracies.

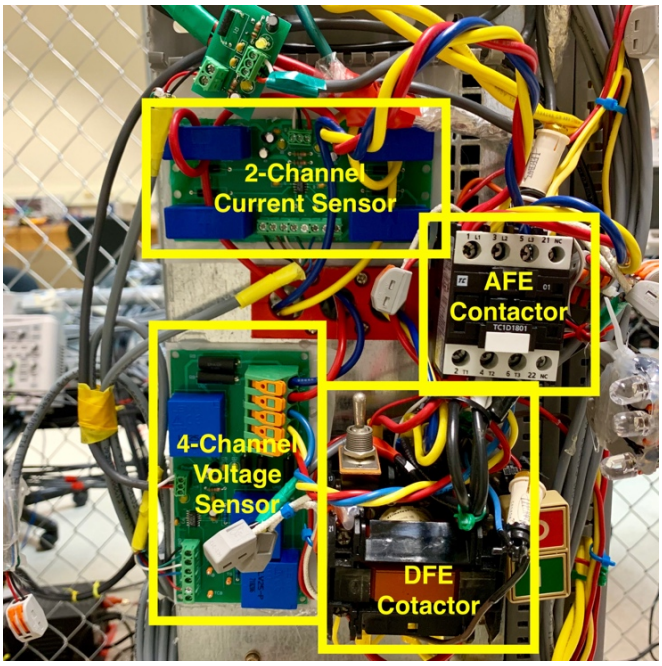
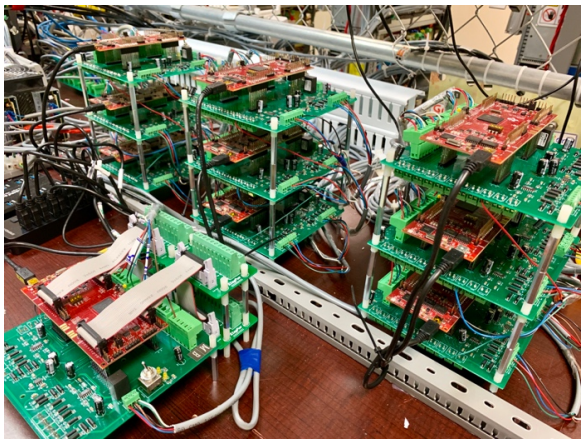


Fig. 7.6 Sensors and contactors.

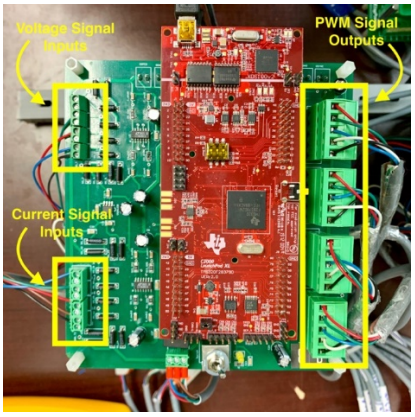
Considering the prototype flexibility, DFE rectifier and AFE rectifier are in parallel connection and their electric paths are controlled by contactors.

7.1.5 AFE Rectifier Control Platform

Fig. 7.7 (a) shows the design of AFE rectifier controllers. Each power cell is specified with a slave controller as shown in Fig. 7.7 (b). 9 slave controllers have internal communication between each other, such as the synchronization signal that used for generating synchronized PWM signals.



(a) Nine AFE slave controllers and one master controller.



(b) An slave controller.

Fig. 7.7 DSP-based AFE rectifier control platform.

Slave controllers receive the output signals of sensors and transform the voltage levels to 0~3.3 V CMOS voltages. A TI C2000 MCU F28379d launchpad is the embedded signal processor, utilizing the signals for system control and protection. 0~5 V TTL PWM signals can be sent to AFE/dc chopper drivers through the slave controller's output.

One master controller acts as the monitor for 9 slave controllers.

7.1.6 H-bridge Inverter Control Platform

Fig. 7.8 shows the H-bridge inverter controller based on dSpace MicroLabBox. H-bridge-side sensor signals are obtained as analog inputs of dSpace. The output control signals are delivered through dSpace's digital output channels. A PCB-based output signal regulator is used for voltage level transformation and distribute PWM signals to appointed H-bridge inverter IGBT drivers.

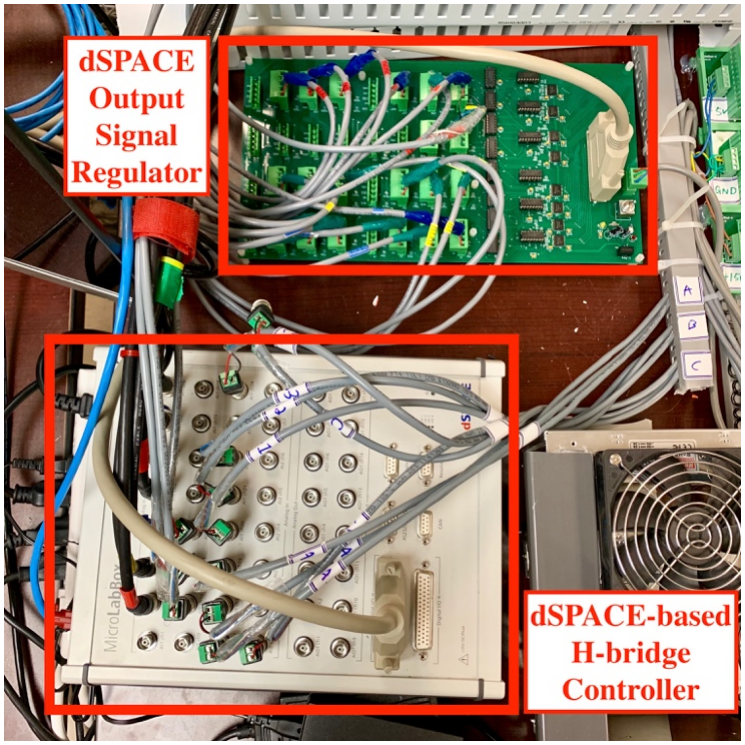


Fig. 7.8 dSpace-based H-bridge inverter control platform.

7.2 Experiment Studies

Fig. 7.9 shows the output voltage and current waveforms of a regen CHB power cell. Output voltage appears a 160 V peak value, same as dc-link voltage. Cell output current has a 10 A peak value.

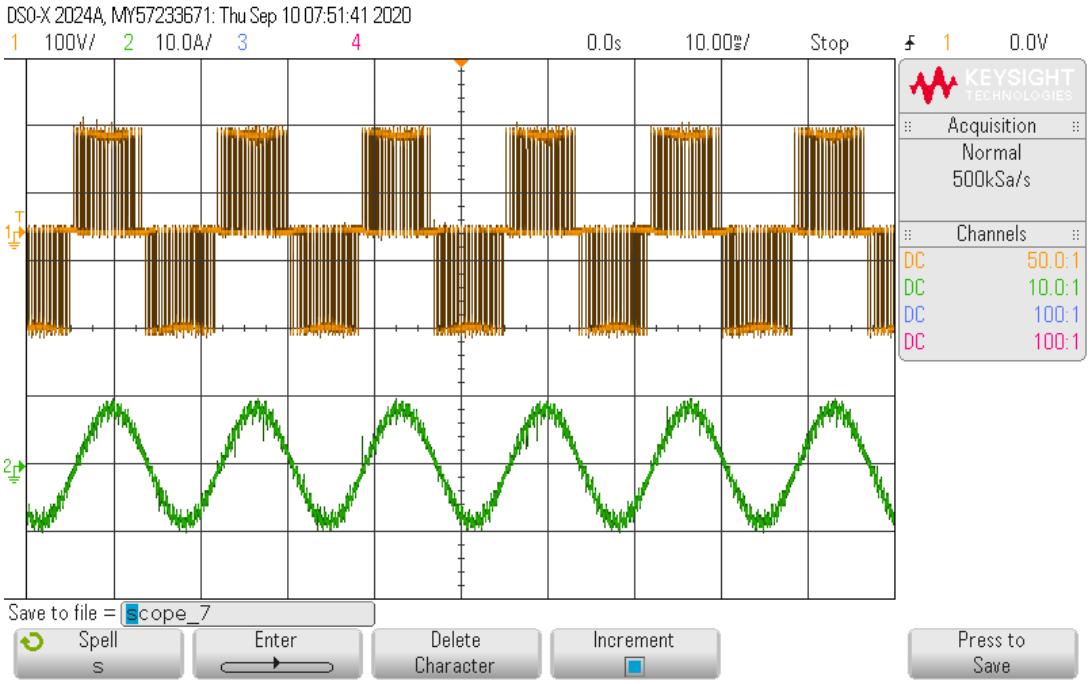


Fig. 7.9 Output voltage and current waveforms of a regen CHB power cell.

Fig. 7.10, Fig. 7.11 respectively show the dc-bus currents for 3-phase AFE rectifier and H-bridge inverter, as well as their spectrums, without the proposed CST. The colors of figure backgrounds are set to black for better presentation.

Pointers of spectrums locate on 2400 Hz, which is 2 times switching frequency. Significant current harmonics can be observed in this position on both converter dc-bus sides, as the central components on 2nd carrier band.

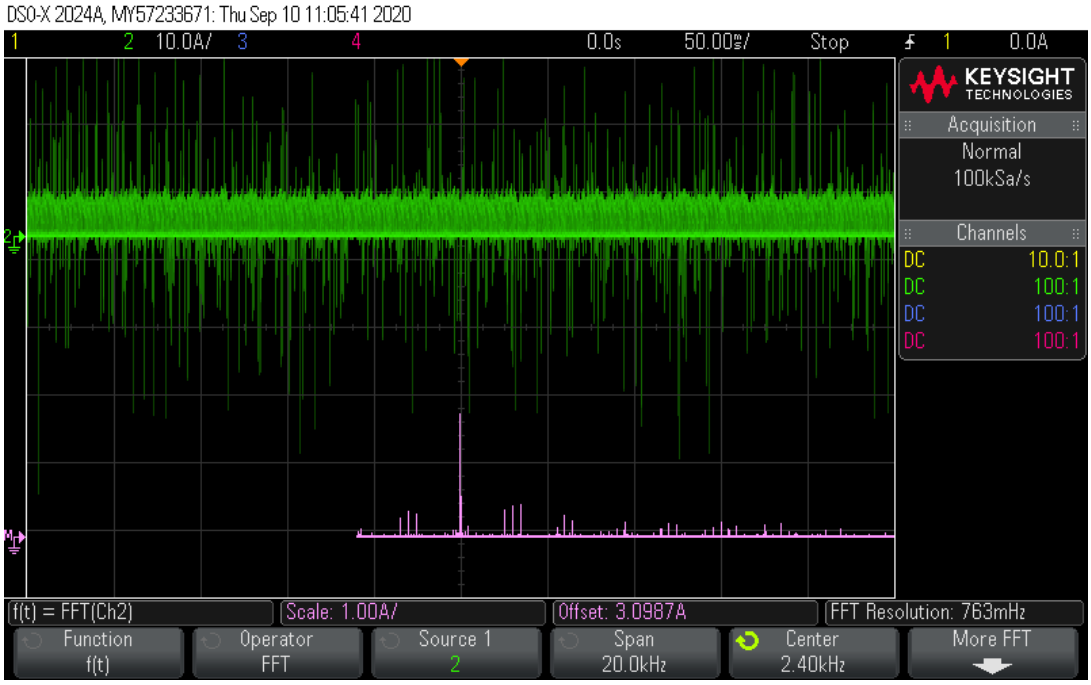


Fig. 7.10 3-phase AFE rectifier dc-bus current and spectrum without CST.

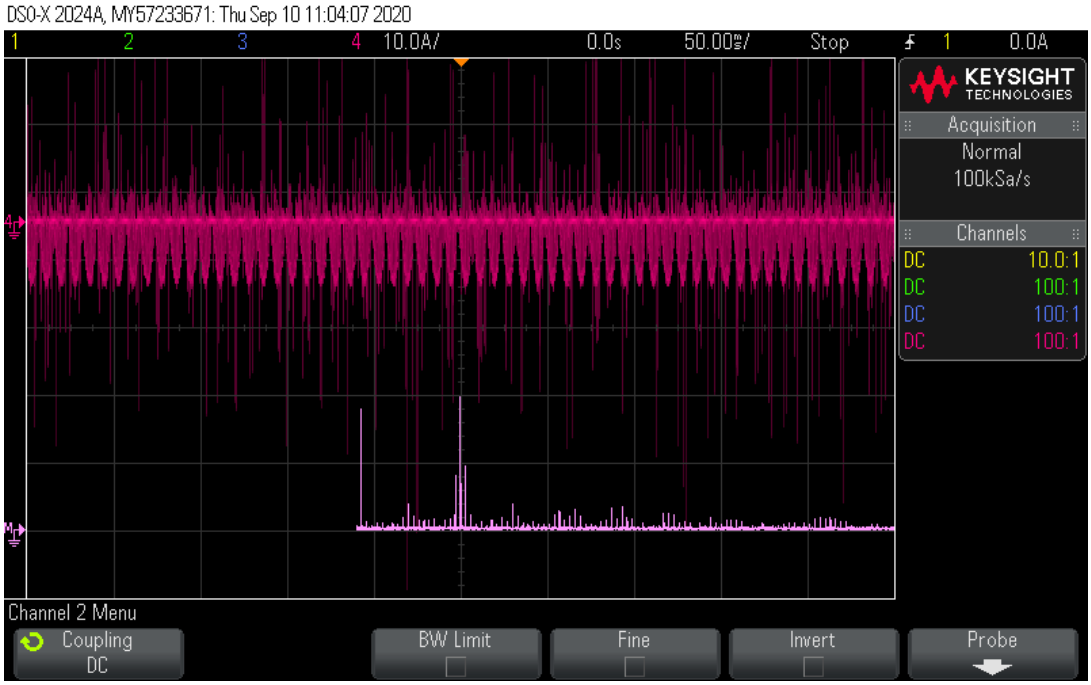


Fig. 7.11 H-bridge inverter dc-bus current and spectrum without CST.

Dc-link current of a capacitor unit is presented in Fig. 7.12. Without the utilization of proposed CST, a significant superposed 2400-Hz current harmonic is injected into dc-link capacitor.

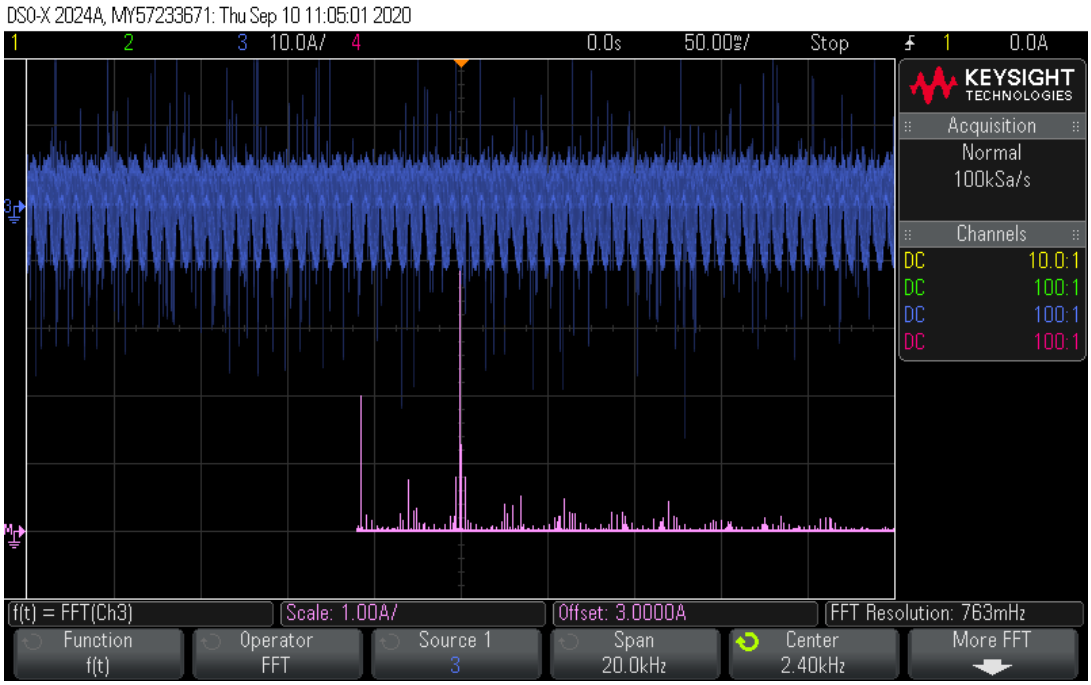


Fig. 7.12 Dc-link capacitor current and spectrum without CST.

Fig. 7.13, Fig. 7.14 respectively show the dc-bus currents for 3-phase AFE rectifier, H-bridge inverter and their spectrums, with the introduction of proposed CST. No difference can be noticed on two dc-bus currents, which means the two ac side current in a power cell will not be influenced by proposed CST.

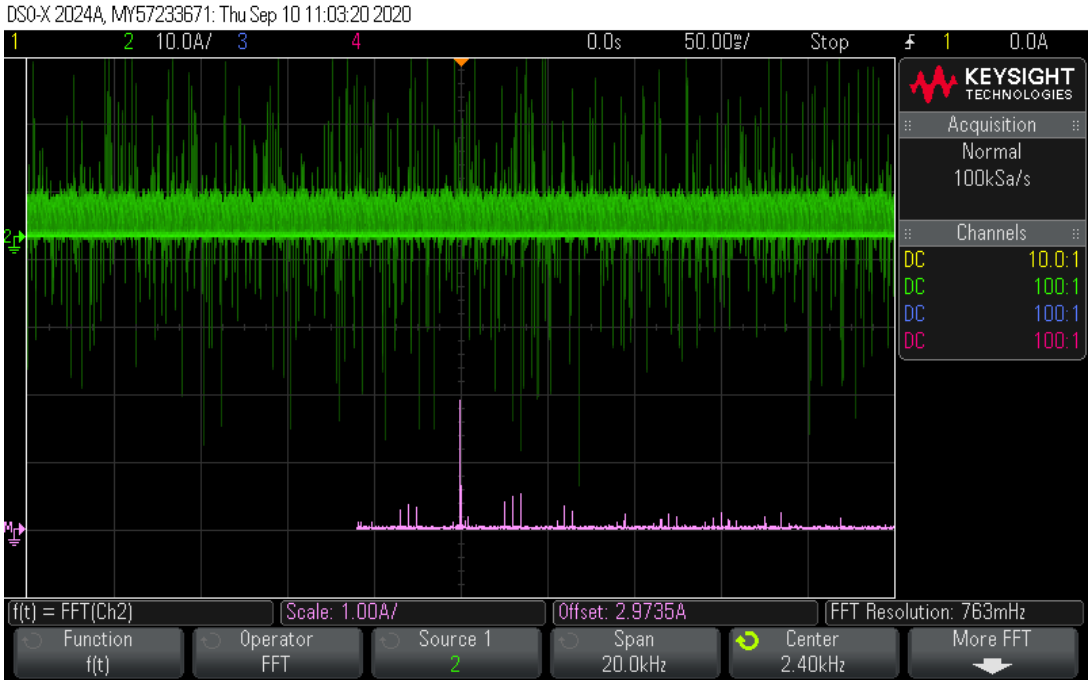


Fig. 7.13 3-phase AFE rectifier dc-bus current and spectrum with CST.

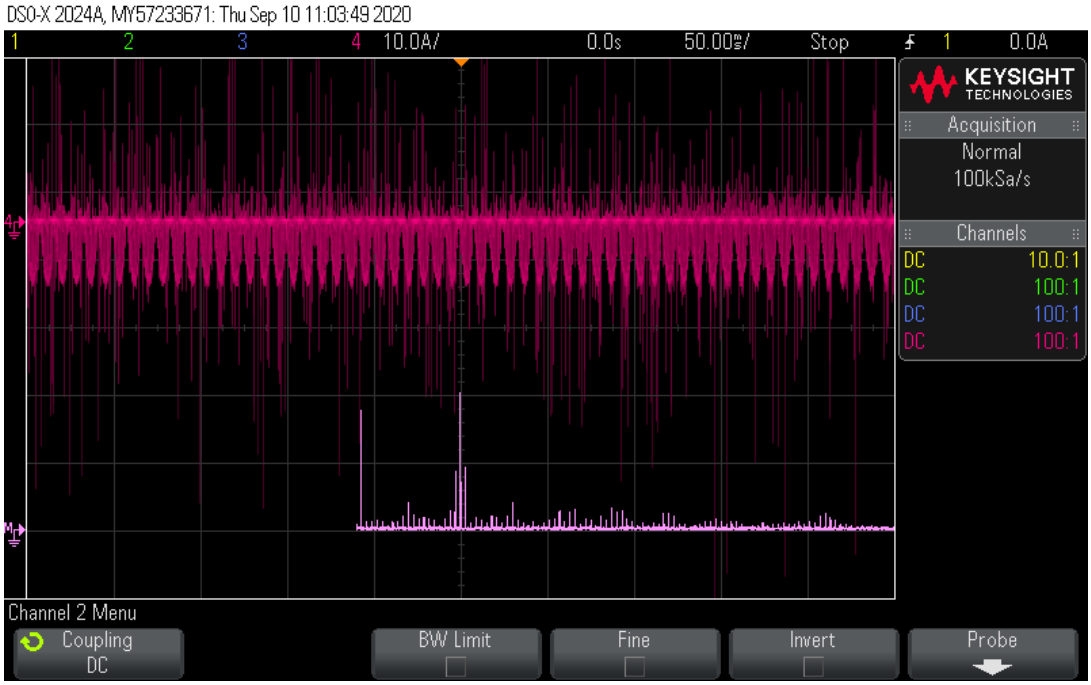


Fig. 7.14 H-bridge inverter dc-bus current and spectrum with CST.

Dc-link capacitor current with proposed CST is shown in Fig. 7.15. With the proposed method, the amplitude of 2400-Hz dc-link current harmonic can be drastically reduced. Feasibility of the proposed dc-link capacitor current harmonic reduction method can be proved.

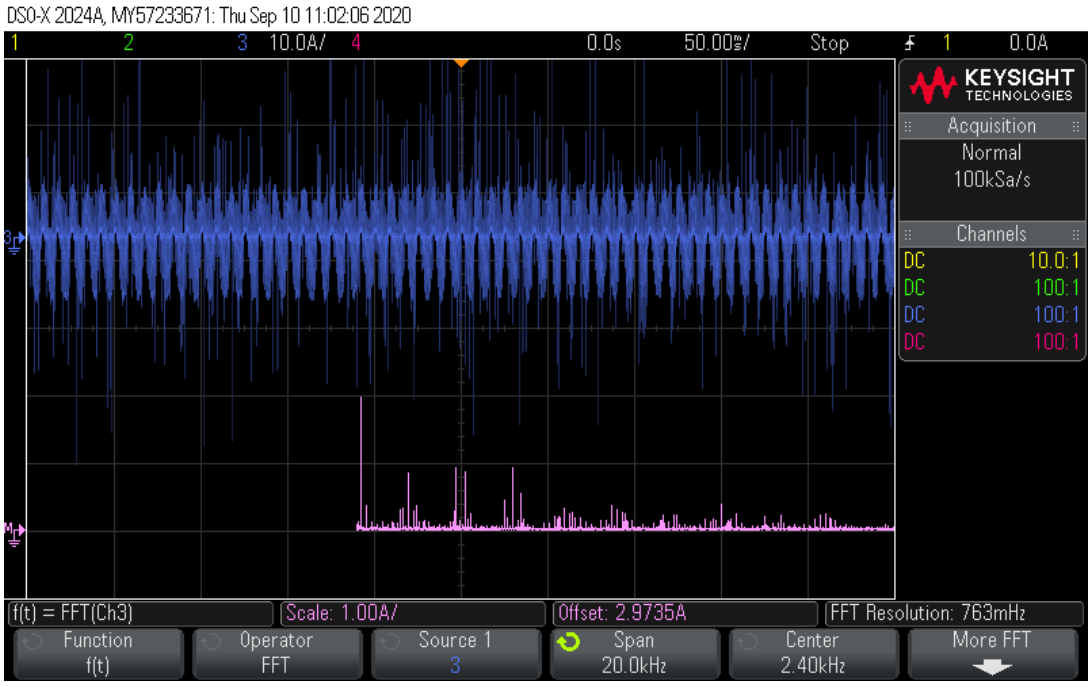


Fig. 7.15 Dc-link capacitor current and spectrum with CST.

7.3 Summary

Introduction of the experimental prototype was delivered in this chapter. An scaled-down regen CHB prototype was established. This prototype has a 600 Vrms line-to-line output voltage, and being tested by a RL load with 10 kW power. Layout of the CHB inverter, especially the power cell structure, was introduced. Some other components such as IGBT module, phase-shifting transformer etc. were also mentioned.

Precision V/I sensors, AFE rectifiers controllers based on DSPs and H-bridge inverters controller based on dSpace are presented in details, which are the kernels of topology control platform.

Detailed experimental results verify the feasibility of proposed CST, a significant reduction of the 2nd carrier band central harmonic can be seen.

Chapter 8

Conclusions and Future Work

8.1 Conclusions

This thesis discussed the modelling and improvement of dc-link capacitor lifetime in a regenerative cascaded H-bridge medium-voltage motor drive (regen CHB MVMD). A complete illustration of regenerative motor drive, capacitor types comparison and capacitor reliability stresses brought about proposed approaches on capacitor estimated useful lifetime (EUL) modelling. In order to mitigate the influence of ripple currents on capacitor lifetime and reduce the power loss of motor drive power cells, a PWM-based carrier shifting technique (CST) between active-front-end rectifier and inverter topologies are proposed.

Proposed EUL model is based on physics-based estimation (PE), it finds novelties on universal utility and accuracy. Both models for aluminum electrolytic (Al-Elec) capacitors and metallized polypropylene film (MPPF) capacitors shared similar form. Major lifetime stresses such as ripple current, ambient temperature, applied voltage and humidity are took

into consideration. Lifetime prediction given by the proposed models reasonably fitted the lifetime data provided by capacitor manufacturers. As revealed by the EUL models, ripple current has an obvious dominancy on determining capacitor lifetime. And generally, MPPF capacitor has a better lifetime performance compared with Al-Elec capacitor under same operating conditions.

Proposed CST focused on the intrinsic switching harmonics of SPWM modulation technique on dc-link current, by tuning the shifting angle between converters' PWM carriers, the main current harmonic component with two times carrier frequency can be significantly reduced. Feasibility of proposed CST is verified in a 3 kV, 140 A, 7-level regen CHB MVMD model in simulation. The EUL improvements, as well as power loss reduction for both capacitor types could be anticipated.

Four groups of dc-link capacitor banks with Al-Elec capacitors and MPPF capacitors from two leading manufacturers are designed for the 3 kV regen CHB MVMD. Reasonable number of capacitors in series and parallel are selected, in order to sustain dc-link voltage and reach demanded total capacitance. Based on the four capacitor banks and utilizing the proposed EUL models and the proposed CST, thorough analysis on capacitor banks lifetimes and thermal losses are given.

The proposed CST's effectiveness on lifetime extension and power losses reduction is proved on all four capacitor banks. Intercomparisons between Al-Elec capacitors and

MPPF capacitors revealed that MPPF capacitors are superior in terms of lifetime performance under identical given conditions. Furthermore, much less power losses can be expected in MPPF capacitors.

8.2 Contributions

This thesis concerns itself with the dc-link capacitor issues in regen CHB MVMDs. The main contributions of the presented work can be summarized as follows:

Structures and characteristics of Al-Elec capacitors and MPPF capacitors are studied. Reliability analysis of them is discussed.

EUL models for Al-Elec capacitors and MPPF capacitors are proposed to express impacts from ripple current, ambient temperature, applied voltage and humidity. Feasibility and accuracy of the models are verified by manufacturers' data.

A PWM-based CST is proposed to reduce a dominant current harmonic on dc-link capacitors. Simulation studies of the method verifies its effectiveness.

Based on selected Al-Elec capacitor and MPPF capacitor products, four capacitor banks are designed for a 3 kV regen CHB MVMD model. By integrating the proposed EUL models and CST, lifetime improvement and power loss reduction can be completed.

8.3 Future Work

Some research spots in this thesis worth further investigations in the future:

The first is experimental studies of the proposed EUL models. By using suitable lifetime testing platform, data-driven analysis of capacitors based on accelerated tests can be used for model verification and modification. Given testing conditions on several lifetime stresses can imitate practical situations in different capacitor applications. Artificial intelligence (AI) approaches can be applied for data analysis.

The second is EUL modeling of batteries and capacitors in powertrain applications, such as electric vehicles (EVs). Stresses such as mechanical vibration and electromagnetic interference (EMI) could be critical factors in EV battery lifetime. Some other reliability analysis models could be developed for this domain.

The next potential future work is utilization of the proposed CST in other regenerative power converter topologies. Two-level voltage source inverter (VSI) is widely used in low-voltage applications due to its simple topology, it is worth investigating the merits of CST in this topology with regeneration capability. For some other regenerative modular multilevel inverters, a similar research approach on regen CHB MVMD can be applied.

The last future plan in research work is capacitor upgrades by replacing electrolytic capacitors in existing prototype with film capacitors. By collecting actual lifetime-related parameters in the setup, dc-link capacitors databases for different capacitor products can be

established. An optimal capacitor selection in terms of EULs, power losses, size, weight and cost can be given for power cells optimal design.

Publication

[1] S. Yuan, and M. Narimani "*Current Harmonic Reduction in DC-link Capacitors of a Regenerative Cascaded H-bridge Converter"* Accepted for presentation in 2020 IEEE Energy Conversion Congress and Exposition (ECCE).

Future Publications

[2] S. Yuan, and M. Narimani "*Estimated Useful Lifetime Modeling for Aluminum Electrolytic Capacitors and Metallized Polypropylene Film Capacitors",* To be submitted to IEEE Transactions on Power Electronics.

[3] S. Yuan, and M. Narimani "*Lifetime Improvement and Power Loss Reduction of a Regenerative Cascaded H-bridge Converter",* To be submitted to IEEE Transactions on Industrial Electronics.

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