Six-Phase Voltage Source Inverter Efficiency Optimization Using Advanced Switching Techniques

SIX-PHASE VOLTAGE SOURCE INVERTER EFFICIENCY OPTIMIZATION USING ADVANCED SWITCHING TECHNIQUES

BY

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A THESIS

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

AND THE SCHOOL OF GRADUATE STUDIES

OF MCMASTER UNIVERSITY

IN PARTIAL FULFILMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

MASTER OF APPLIED SCIENCE

Master of Applied Science (2020) McMaster University

(Electrical & Computer Engineering) Hamilton, Ontario, Canada

TITLE:	Six-Phase Voltage Source Inverter Efficiency Optimization Using Advanced Switching Techniques
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NUMBER OF PAGES:	xv, 160

Abstract

Since the late 1990's, lots of attention has been given to the development of multi-phase motor drives due to the momentous interest in developing greener methods of transportation and the increased benefits when compared to their three-phase counter parts. These benefits include improved fault tolerant control, reduced torque ripple, improved motor power density, and reduced DC link capacitance which has resulted in an amplified interest in multi-phase machines for electric ship propulsion, electric aircrafts, and traction electric motors (electric and hybrid road vehicles). When looking specifically into multi-phase machines that are made up of six-phases, different topologies have been researched that include altering the phase shift between the different windings or winding sets as well as the number of neutral points within the machine. Out of all possible combinations, there are three common six-phase machine topologies studied in the literature. First is the six-phase machine with a 60° phase shift between each of the machine windings – referred to as a symmetrical six-phase machine. The second and third topologies are a six-phase machine with two sets of three phase windings where one winding set has a phase shift from the other winding set (typically 30°). When the two winding sets have a shared neutral point, the machine is referred to as an asymmetrical six-phase machine. Alternatively, when the two winding sets have isolated neutral points, the machine is referred to as a dual

three-phase machine.

From the recent surge in literature regarding the added benefits of the dual three-phase machine compared to other six phase topologies, this thesis will mainly focus on the control and switching techniques specifically for the dual three-phase machine. With an in-depth analysis, the effect of different switching techniques will be observed on the overall efficiency of the six-phase voltage source inverter (VSI). Furthermore, using the Matlab/Simulink and PLECS environment with a dual three-phase drive system vector space decomposition (VSD) based model, an accurate drive model that incorporates the machines dynamic behaviour and calculates the total losses of the VSI is also proposed. The VSI is connected to a 100 kW dual three-phase interior permanent magnet synchronous machine (IPMSM) and different switching techniques are applied to the inverter to properly control the six-phase drive system.

Similar to their three-phase counter parts, dual three-phase machines can be controlled using sinusoidal carrier-based pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM). This thesis explores the VSI efficiency when using different switching techniques proposed in the literature and proposes new techniques to improve the efficiency of the VSI. Additionally, a detailed plan for an experimental setup and testing procedure is provided for the switching techniques that are simulated throughout this thesis. This proposed testing procedure assumes a prototype six-phase VSI composed of six Infineon FF600R12IE4 IGBT modules that are connected to a dual three-phase 100 kW IPMSM. As the future work of this thesis includes experimental verification, the Matlab/Simulink drive model proposed in this thesis is designed with this particular setup in mind.

Acknowledgements

I would first like to express my deep appreciation to Dr. Mehdi Narimani and Dr. Ali Emadi for their guidance and support throughout my graduate studies. As my supervisor and co-supervisor, they both played an important role in getting me to where I am now as a researcher and I am very grateful for the opportunities that they have provided for me.

Additionally, my sincere appreciation also goes to Dr. Berker Bilgin who I could also always rely on for advice and assistance. His confidence in my work and willingness to always support me has helped me to achieve my goals both academically and professionally.

My gratitude also goes to my colleagues from the Department of Electrical and Computer Engineering, especially Dr. Babak Nahid-Mobarakeh, Diego F. Valencia, Sumedh Dhale, and Dr. Peter Azer who would never hesitate to stop what they are doing to assist me.

Last but not least, I would like to give a special thank you to my family. I would not be here without the love and support from my parents, Kevin and Gemma Taylor, as they have helped to shape the person I am today. A very special thank you to my wife, Courtney Taylor, who has shown me unconditional love and patience through my graduate studies and has always been by my side through this journey.

This research was undertaken thanks to funding from the Natural Sciences and Engineering Research Council of Canada (NSERC). I would also like to thank ANSYS for their support with ANSYS workbench, Mathworks for their support with Matlab and Simulink, and Plexim for their support with PLECS.

This work is dedicated to the memory of Iman Aghabali and Mehdi Eshaghian – two friends that truly made the workplace a more enjoyable place to be and are dearly missed.

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Chapter 1

Introduction

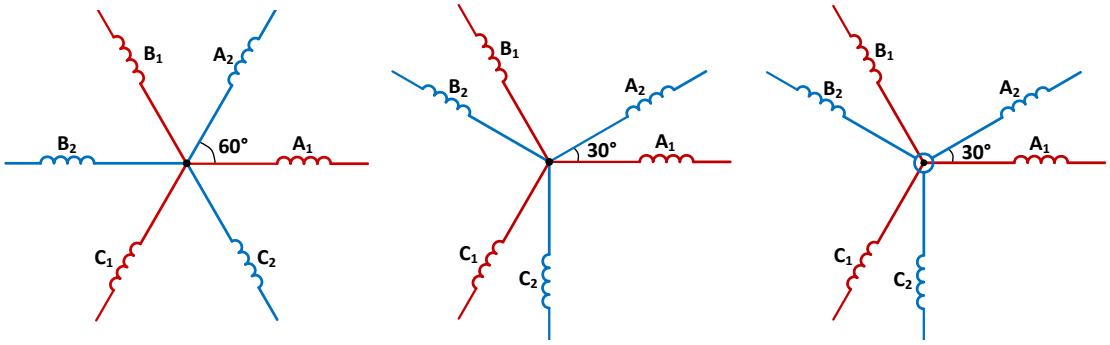
1.1 Motivation

Recent trends within a variety of applications are moving towards the use of electric machine drive systems with increased power ratings; however, these systems are being limited by the voltage and current ratings of the switching devices used within converter systems [1]. While three-phase systems are still preferred due to their availability and variety of both machines and power converters [2], multi-phase machine drives bring many added benefits compared to their three-phase counterparts and have been increasing in popularity since the 1990s. One of the main advantages of multiphase machines is that for a variable speed drive with the same power rating as its three-phase counterpart, lower power rated switching devices can be used due to the power distribution being split among a higher number of phases [1]. Therefore, for an increase in a multiphase machines' power rating, higher-rated switches are not required as they would be in the three-phase counterparts. Alternatively, for a multiphase machine with the same power rating as its three-phase counterpart, lower

rated switching devices can be utilized. Other significant advantages of multiphase drives include torque ripple reduction, improved fault-tolerant operation, improved motor power density, and increased control flexibility [1, 3]. Torque ripple reduction is typically achieved through the design of the machine as there is an increase in the frequency of the torque pulsations which lowers the amplitude of the oscillating torque waveform. This is because the frequency of the torque component is represented by the harmonic of the order $2n \pm 1$ for an n-phase machine [2]. When considering the improved fault-tolerant operation and increased control flexibility, the number of degrees of freedom of the system are what contributes to these benefits. The higher the number of phases in the system, the more degrees of freedom there are [4]. However, it is also important to note that with an increase in the degrees of freedom, there is a trade-off as control/design complexity increases. Therefore, several different aspects need to be considered when designing a multiphase drive system including the phase number, the number of neutral points in the system, and the phase shift between each of the phases.

Due to modularity and manufacturing simplicity, it has become very common for multiphase machines to be made up of a multiple of three phases. This also is preferred since many control and modelling techniques based around three-phase machines can be applied to machines of these phase numbers [4]. For example, commonly used control strategies for three-phase machines such as field-oriented control (FOC), which is first proposed in [5], and direct torque control (DTC), which is first proposed in [6], can be adapted to $3n$ (n = 2,3,4,...) phase machines. Nevertheless, due to the increase in complexity as the phase number increases, six-phase machines have proven to be a promising phase number for the implementation of multiphase drive

systems. Furthermore, there exist many different variations of six-phase machines where three topologies have become the most popular in the literature. First is the six-phase machine with a 60° phase shift between each of the machine windings – referred to as a symmetrical six-phase machine. The second and third topologies are both six-phase machines with two sets of three-phase windings where one winding set has a phase shift from the other winding set – this phase shift is typically 30°. When the two winding sets have a shared neutral point, the machine is referred to as an asymmetrical six-phase machine. Alternatively, when the two winding sets have isolated neutral points, the machine is referred to as a dual three-phase machine. The main benefit of using a 30° phase shift over any other angle between the two winding sets is to eliminate the 6^{th}, 18^{th}, and 30^{th} harmonic pulsations of the torque waveform as shown in [7]. The different topologies with their different neutral point configuration and phase shift between winding sets can be seen in Figure 1.1.



(a) Symmetrical Six-Phase (b) Asymmetrical Six-Phase (c) Dual Three-Phase

Figure 1.1: Common Six-Phase Machine Topologies

In a separate analysis completed in [4], it is proven that the dual three-phase machine provides the best performance compared to the other six-phase topologies for high power, variable speed applications. It can be further verified that the dual

three-phase machine is the only six-phase topology from Figure 1.1 with DC-link voltage utilization as high as its three-phase counterpart. This is one of the main reasons why the dual three-phase drive system is a preferred multiphase machine in the literature and the main focus of this thesis.

As the dual three-phase drive system has its proven advantages, the motivation of this work stems from the recent trends moving towards increasing the power rating of electric drive systems specifically in automotive applications. With first developing an accurate simulation model to emulate the dynamic behaviour of the physical motor, different aspects of the drive system can be adjusted to observe the overall performance. Moreover, the proposed model in this thesis which can be implemented for any multiphase machine allows for the efficiency of the two-level voltage source inverter (VSI) to be evaluated using different switching techniques while considering the motor's dynamic behaviour. With room for efficiency improvements due to the increased control flexibility of a dual three-phase drive system, this thesis focuses on implementing new switching techniques to further enhance the VSI efficiency. Though only small improvements for the overall drive system are expected, these improvements in efficiency for automotive applications help lead to an increased driving range as hybrid and electric vehicles continually gain interest in replacing the conventional internal combustion engine vehicles.

1.2 Contribution

As the motivation of this thesis is to work towards improved drive system efficiency for electric drives in automotive applications, the main contributions of this thesis are summarized as:

- An in-depth literature review of existing switching techniques developed for the constant torque region of dual three-phase drive systems. More specifically, the existing techniques from literature that are investigated require each switch, at maximum, to turn on and off one time and for the sampling frequency to remain equal to the switching frequency, $f_{samp} = f_{sw}$. These requirements are maintained for all techniques throughout this thesis to ensure that each switching technique can be implemented using a digital signal processor (DSP) without making any adjustments to the built in pulse width modulation (PWM) drivers of the control board.

- A dynamic modelling technique for multiphase motors is proposed and implemented using the Matlab/Simulink environment. This motor model is used with a detailed controller and inverter model to simulate an FOC based system that utilizes the dual three-phase VSD transformation. This Simulink drive model is simplified to only include the current control loop where a d and q axis reference current are obtained from an offline MTPA profile and used directly as inputs to the model. Additionally, the Simulink model is validated using FEA to show the accuracy of the proposed modelling technique.

- Implementation of multiple existing switching techniques using the aforementioned detailed Simulink model. These techniques are compared in terms of the overall inverter efficiency where a six-phase, two-level VSI is modelled using the PLECS by Plexim Simulink toolbox to accurately model temperature dependent power losses of each insulated-gate bipolar transistor (IGBT) module. Current literature on switching techniques of multiphase machines is focused on

reducing the phase current total harmonic distortion (THD), however, the literature does not contain a detailed analysis of reducing the switching frequency and the effect of different switching algorithms on the inverter efficiency.

- New switching techniques are proposed to help improve inverter efficiency where the numerous switching states of the six-phase VSI compared to its three-phase counterpart are taken advantage of while using the VSD transformation. The redundancy in the voltage vectors also play a key role in helping to reduce the average switching frequency over several sampling periods. This reduction in the switching frequency reduces the total switching power losses while conduction power losses of the IGBT module remain the same. For this reason, proposed switching techniques aim to lower the average switching frequency while still maintaining comparable THD results to existing techniques.

- A discussion of the planned DSP implementation and testing procedure to experimentally verify the findings of this work. The discussed testing bench will be intended for a 100 kW dual three-phase drive system where preliminary test results at very low power are used to experimentally validate the previously mentioned Simulink drive model.

1.3 Thesis Structure

This thesis is organized as follows:

Chapter 2 provides a comprehensive literature review of the existing six-phase drive system control and switching techniques. This chapter will focus on the difference between the VSD and Double dq transformations and how the switching techniques differ for each transformation. Switching techniques explored include carrier-based sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM). This chapter focuses on the proposed switching techniques from literature that reduce the switching frequency which will in theory lead to improved inverter efficiency.

Chapter 3 proposes a detailed modelling technique for multiphase motors while using the Matlab/Simulink environment to simulate an entire dual three-phase drive system. This motor modelling technique incorporates the dynamic behaviour of the machine as well as the high frequency current ripple that is created by the VSI switching instances. Additionally, with a focus on the inverter efficiency, PLECS by Plexim is used to calculate the switching and conduction losses of the IGBT modules, as well as the reverse recovery losses and conduction losses of the diodes within these modules.

Chapter 4 uses the Simulink drive model developed in Chapter 3 to provide simulation results for the existing switching techniques discussed in Chapter 2. Each of these techniques is compared in terms of overall inverter efficiency and phase current THD for the constant torque region of a dual three-phase drive system. This chapter also proposes new switching techniques that are specifically developed to improve the efficiency of the inverter with a comparison to the existing techniques found in the

literature. To further analyze and validate the proposed switching techniques, the harmonic performance will also be evaluated and compared to existing techniques.

Chapter 5 provides a discussion in to how the techniques discussed throughout this thesis can be implemented using a high-power experimental setup. Due to limited resources, the 100 kW dual three-phase drive system is only able to operate at very low load operating points to verify the DSP implementation techniques discussed throughout this chapter. This chapter also provides additional experimental validation of the Simulink drive model using the discussed methods of implementing switching techniques to the DSP.

Lastly, in Chapter 6, concluding remarks are made and a wrap up of the overall contributions of this thesis are reviewed. Proposed future work using the experimental setup and controller programming methods from Chapter 5 are also discussed in this chapter.

Chapter 2

Six-Phase Motor Control and Switching Techniques

2.1 Introduction

The surge in popularity and the added benefits of multiphase drive systems compared to their three-phase counterparts has led to an abundance of research that prove multiphase systems to be viable options for electric ship propulsion, more electric aircraft, and traction electric motors (electric and hybrid road vehicles). In recent years, the overflow of literature regarding multiphase machine drives and control has been summarized into several different surveys which categorize recent technical papers into various groups including multiphase machine modelling and design, control techniques, and PWM switching techniques [1, 2, 3, 8, 9, 10, 11, 12, 13, 14]. As this thesis will have a main focus on PWM switching techniques, it will be assumed throughout that a FOC scheme is being utilized. Therefore, it is important to draw attention to FOC based control techniques and switching techniques that have already

been proposed throughout the literature.

Looking back to the previously discussed benefit that six-phase drive systems, in general, have increased flexibility compared to three-phase drive systems, when designing the control of the drive, two different control/modelling methods are commonly used – the Vector Space Decomposition (VSD) and Double dq transformations. The VSD approach uses a generalized Clarke transformation proposed in [5] to create three orthogonal subspaces. First, the $\alpha\beta$ subspace contains the harmonics of the order $12n \pm 1$ (n = 1,2,3,...) which are the only harmonics that contribute to the electromechanical energy production of the machine [15]. Another subspace, referred to as the xy subspace, contains the harmonics of the order $6n \pm 1$ (n = 1,3,5,...) which do not generate any electromechanical energy due to zero magnetomotive force being generated in the air gap from these harmonics [5]. The third subspace that is created from the transformation contains the zero sequence, third order, harmonics which also have no contribution to the electromechanical energy conversion [5]. It is important to note that due to the dual three-phase machine having two winding sets with isolated neutral points, the zero sequence components cancel out and can be neglected to simplify the transformation which is another added benefit of the dual three-phase drive system compared to the other six-phase topologies discussed [15]. Alternatively, the Double dq approach for six-phase machines treats each three-phase winding set independently with their own separate dq subspaces – dq_1 and dq_2 [16]. This approach has the advantage of being able to utilize three-phase control techniques on each winding set separately. However, in [16] it is clear that the effect of mutual coupling between the two winding sets is significant, unlike the VSD approach where the three orthogonal subspaces are independent [3]. Both of these

control methods have their advantages and disadvantages and they will be analyzed further in the following section.

Continuing the discussion of control comparison between six-phase and three-phase drive systems, the flexibility of control within six-phase systems comes with the trade-off of increasing the control complexity; however, with the phase number increasing, so does the number of utilizable voltage vectors. Assuming a two-level inverter design seen in Figure 2.1 which is commonly used for multiphase drive systems, there exists 2^n possible inverter switching states, for an n-phase machine [8].

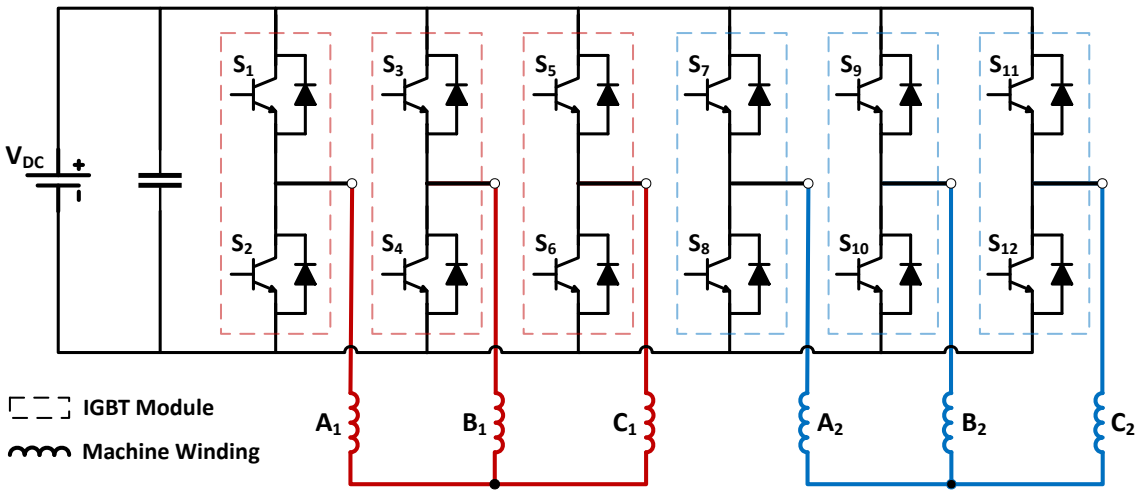
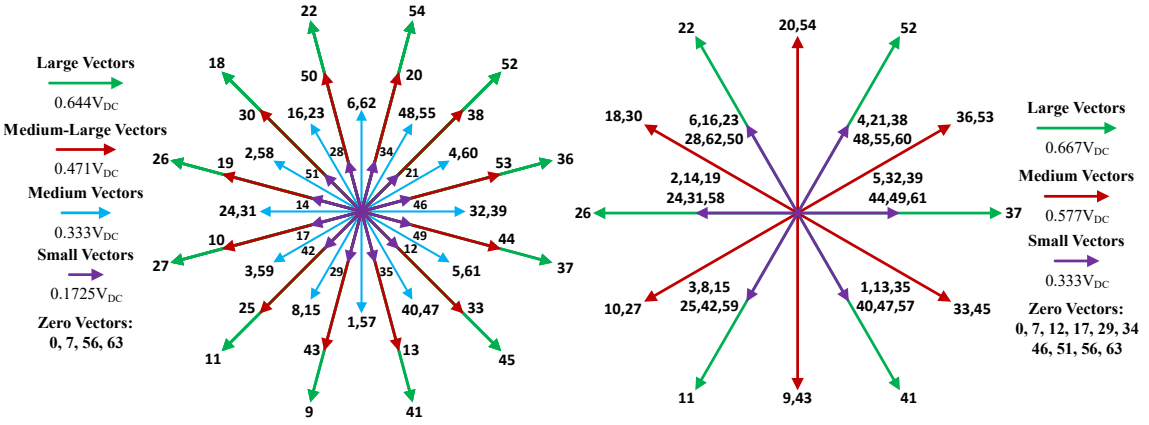


Figure 2.1: Two-Level Six-Phase VSI Connected to Dual Three-Phase Machine

In other words, any six-phase two-level inverter will have 64 possible switching states compared to a three-phase two-level inverter which only has 8 possible switching states. When considering the VSD transformation, each voltage vector from the 64 different switching states can be observed on one $\alpha\beta$ plane. It is important to note that these switching states include redundant zero voltage vectors and, for the sake of the six-phase inverter, redundancy in some of the other voltage vectors as

well. The redundant voltage vectors are related to the topology of the machine with direct relation to whether the phase shift between the windings is symmetrical or asymmetrical.



(a) Dual Three-Phase/Asymmetrical Six-Phase (b) Symmetrical Six-Phase

Figure 2.2: Utilizable Voltage Vectors of a Two-Level VSI for Different Machine Topologies

For the asymmetrical configurations (asymmetrical six-phase and dual three-phase machine), there are 49 possible voltage vectors that can be chosen from the 64 switching states with 4 redundant zero vectors and 12 redundant medium vectors which can be seen in Figure 2.2a. Alternatively, for the symmetrical six-phase configuration, there are only 19 possible voltage vectors to be chosen from the 64 switching states. This is because of the redundancy of each voltage vector except for the six large vectors which can be seen in Figure 2.2b. Therefore, the variety of voltage vectors with the asymmetrical configurations is another reason why the dual three-phase drive system is a preferred six-phase topology. Note that the decimal numbers used to label each voltage vector in Figure 2.2 represent six-digit binary numbers where each binary number represents the state of each phase leg of a two-level inverter. The

binary number "1" means that the top switch of the inverter phase leg is closed, and the bottom switch is open, and vice versa for the binary number "0". For example, assuming a phase order of $A_1B_1C_1A_2B_2C_2$, the voltage vector $36_{10} = 100100_2$ implies that the top switches of phase A_1 and A_2 are closed while all other phases have the bottom switch closed. Note that this phase order is assumed throughout this thesis.

Throughout this chapter, the two aforementioned coordinate transformations commonly used for multiphase machines will first be analyzed and the theory of each will be explained. It is important to note that these transformations can be further simplified for a dual three-phase machine. This chapter will then focus on the different FOC based control techniques that have been recently proposed based on these transformations. With these control techniques generating synchronous reference frame voltages, V_α and V_β, the inverter gate pulses can be generated which produce controlled voltages that are sent to the motor. These switching techniques that generate the inverter pulses are dependent on the coordinate transformation and control technique used but similar to three-phase systems, versions of SPWM and SVPWM are the commonly used methods for both transformations.

2.2 Six-Phase Coordinate Transformations

Continuing the discussion regarding the two different coordinate transformations commonly used for multiphase machines, the VSD and Double dq transformations each have advantages and disadvantages that impact the control and switching techniques.

2.2.1 Double *dq* Coordinate Transformation

First looking into the Double dq transformation, the idea of this method is to treat each three-phase winding set as separate three-phase machines that can each utilize independent three-phase Clarke transformations to transform phase values to two stationary reference frames [17]. Referring to Figure 2.1 and assuming a phase order of $A_1B_1C_1A_2B_2C_2$, the first three-phase winding set will be referred to as $A_1B_1C_1$ and the second three-phase winding set will be referred to as $A_2B_2C_2$. With this assumption, the Clarke transformation for each three-phase set can be defined in a similar way to the method used in [17]. Assuming f represents voltage, current, or flux linkage, the amplitude invariant Clarke transformation is given as:

$$\begin{bmatrix} f_{\alpha_1} \\ f_{\beta_1} \\ f_{\alpha_2} \\ f_{\beta_2} \end{bmatrix} = T_{Clarke_1} \begin{bmatrix} f_{A_1} \\ f_{B_1} \\ f_{C_1} \\ f_{A_2} \\ f_{B_2} \\ f_{C_2} \end{bmatrix} \qquad T_{Clarke_1} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 & 0 & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ 0 & 0 & 0 & \frac{1}{2} & \frac{1}{2} & -1 \end{bmatrix} \tag{2.1}$$

The transformation seen in (2.1) combines the two independent Clarke transformations for each three-phase winding set. However, it can be noted that the transformation for the second winding set, which is represented by the bottom right 2×3 matrix in T_{Clarke_1}, accounts for the 30° phase shift between the two three-phase winding sets which can be seen in Figure 1.1c. This transformation in (2.1) will transform the phase components of phase set one and phase set two to stationary reference frame components, $\alpha_1\beta_1$ and $\alpha_2\beta_2$, respectively. These stationary reference frame

components can then be transformed to the synchronous reference frame using the commonly used three-phase Park transformation for each winding set where θ represents the machine's rotor position:

$$\begin{bmatrix} f_{d_1} \\ f_{q_1} \\ f_{d_2} \\ f_{q_2} \end{bmatrix} = T_{Park_1} \begin{bmatrix} f_{\alpha_1} \\ f_{\beta_1} \\ f_{\alpha_2} \\ f_{\beta_2} \end{bmatrix} \qquad T_{Park_1} = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 0 & 0 \\ -\sin(\theta) & \cos(\theta) & 0 & 0 \\ 0 & 0 & \cos(\theta) & \sin(\theta) \\ 0 & 0 & -\sin(\theta) & \cos(\theta) \end{bmatrix} \tag{2.2}$$

With the same Park transformation being applied to both winding sets, the stationary components, $\alpha_1\beta_1$ and $\alpha_2\beta_2$, will be converted to synchronous reference frame components, d_1q_1 and d_2q_2. The control techniques that are commonly used for three-phase machines can then be applied to the two sets of synchronous components separately. In other words, the use of the Double dq transformation simply allows for each winding set of the drive system to be operated as independent three-phase machines [18]. This transformation is simple and easy to understand, however, with the two subspaces for each winding set, there exists significant mutual coupling and therefore compensation for how the subspaces interact with one another is difficult.

2.2.2 VSD Coordinate Transformation

Now moving the focus to the VSD transformation, the idea of this method is to consider the entire machine as a single system where only one subspace contributes to the torque production of the machine drive system. For six-phase machines, the generic transformation first proposed in [5], generates three orthogonal subspaces, $\alpha\beta$, xy, and 0^+0^-. Recall that the zero-sequence subspace components, 0^+0^-, cancel out

and can be omitted from the transformation for a dual three-phase drive system due to there being no physical path for the neutral currents [3]. Therefore, the Clarke and Park transformation from [5] can be defined neglecting the rows corresponding to the zero sequence components that are typically included in the matrices. Once again, assuming a phase order of $A_1B_1C_1A_2B_2C_2$ and that f represents voltage, current, or flux linkage, the amplitude invariant VSD-based Clarke transformation is given as:

$$\begin{bmatrix} f_\alpha \\ f_\beta \\ f_{x_s} \\ f_{y_s} \end{bmatrix} = T_{Clarke_2} \begin{bmatrix} f_{A_1} \\ f_{B_1} \\ f_{C_1} \\ f_{A_2} \\ f_{B_2} \\ f_{C_2} \end{bmatrix} \qquad T_{Clarke_2} = \frac{1}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{2} & \frac{1}{2} & -1 \\ 1 & -\frac{1}{2} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & 0 \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & \frac{1}{2} & \frac{1}{2} & -1 \end{bmatrix} \tag{2.3}$$

From this modified transformation for the dual three-phase machine, the six phase components are transformed into two independent subspaces in the stationary reference frame, $\alpha\beta$ and xy_s. With these two independent subspaces, torque production is isolated to a single subspace – the $\alpha\beta$ subspace which contains harmonics of the order $12n \pm 1$ ($n = 1,2,3,\ldots$). Alternatively, the xy_s subspace that contains harmonics of the order $6n \pm 1$ ($n = 1,3,5,\ldots$), is orthogonal to the dq subspace and therefore does not generate any torque and thus is considered to be a new type of zero sequence or circulating component [5]. Furthermore, the xy_s subspace will generate losses in a healthy operating condition [3]. Due to the $\alpha\beta$ components being the single subspace that produces torque, a dual three-phase Park transformation is seen in [19] that transforms only the $\alpha\beta$ components to the synchronous reference frame while

keeping the xy_s components in the stationary reference frame. Again, assuming that θ represents the machine's rotor position:

$$\begin{bmatrix} f_d \\ f_q \\ f_{x_r} \\ f_{y_r} \end{bmatrix} = T_{Park_2} \begin{bmatrix} f_\alpha \\ f_\beta \\ f_{x_s} \\ f_{y_s} \end{bmatrix} \qquad T_{Park_2} = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 0 & 0 \\ -\sin(\theta) & \cos(\theta) & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{2.4}$$

With the VSD method, it can be seen from the transformations above that the original six-dimensional vector space can be isolated to two independent subspaces when considering dual three-phase machines. One subspace that contributes to electromagnetic torque production similar to the VSD approach of three-phase drive systems and another subspace containing harmonics that only contribute to losses inside the machine. It will be seen in the next section, that this transformation can be slightly modified to improve the control simplicity of the overall system.

To provide a more direct comparison between the two transformations, when considering the Double dq transformation, the idea of controlling two three-phase winding sets separately allows for straightforward and simple implementation of commonly used three-phase control and switching techniques for each phase set. However, a major drawback of the Double dq method is that two parallel subspaces are generated for each three-phase machine which leads to significant mutual coupling between the subspaces which requires complicated compensation [18]. Alternatively, the VSD transformation considers the entire machine as one system with only a single torque

producing subspace where mutual coupling does not exist between the other subspaces. As the xy subspace has recently become physically interpreted as the circulating currents between the two winding sets [17], it becomes more complex to control this subspace compared to the two subspaces from the Double dq transformation [3], which will be discussed in the following section.

2.3 Control Techniques

With the knowledge of the different coordinate transformations that are used for dual three-phase machines, different control techniques are proposed in the literature that accommodate the significant disadvantages of each transformation.

2.3.1 Double *dq* Control

With the Double dq transformation having the benefit of being able to control each three-phase winding set with their own respective subspaces, d_1q_1 and d_2q_2, common three-phase control techniques used in automotive applications can be used for each subspace. This allows for the use of conventional three-phase control schemes that utilize proportional-integral (PI) controllers for each component individually [20]. This means that four separate PI controllers are required for each individual component of the two mutually coupled subspaces. However, due to the mutual coupling between the two subspaces, the tuning of each PI controller becomes very difficult as each controlled component is affected by any disturbance in the other three components [20]. For this reason, a decoupling matrix that is proposed in [20, 21, 22] can be implemented to the synchronous reference frame components to simplify the controller

development. Assuming f represents voltage, current, or flux linkage, the amplitude invariant decoupling matrix is given as:

$$\begin{bmatrix} f_{D_1} \\ f_{Q_1} \\ f_{D_2} \\ f_{Q_2} \end{bmatrix} = T_{Decouple} \begin{bmatrix} f_{d_1} \\ f_{q_1} \\ f_{d_2} \\ f_{q_2} \end{bmatrix} \qquad T_{Decouple} = \frac{1}{2} \begin{bmatrix} 1 & 0 & 0 & -1 \\ 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 \\ 0 & 1 & -1 & 0 \end{bmatrix} \tag{2.5}$$

In (2.5), $f_{dq_{12}}$ represent the output of the Double dq Park transformation from (2.2), and $f_{DQ_{12}}$ represent the two decoupled subspaces. This now allows for D_1 and Q_1 to represent the first winding set and be controlled independently from D_2 and Q_2 which represent the second winding set. Assuming SVPWM is used to generate the VSI gate pulses, the FOC based current control scheme adopting the Double dq coordinate transformation and making use of $T_{Decouple}$ can be seen in Figure 2.3.

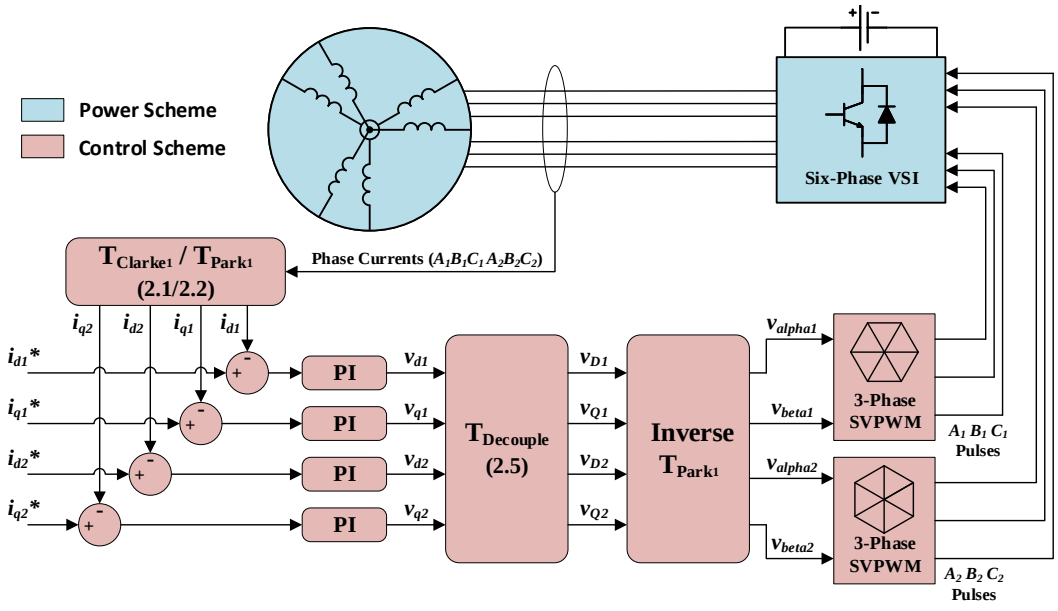


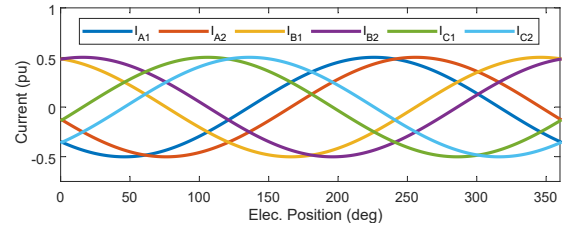
Figure 2.3: Current Control Scheme for FOC, Double dq Transformation Based Controller Utilizing SVPWM

Within this control scheme, the current sensors measure the phase currents of the six phases and convert them to the synchronous reference frame currents using equations (2.1) and (2.2). These synchronous reference frame currents, i_{dq_1} and i_{dq_2}, are then compared to each of their corresponding reference values, $i^*_{dq_1}$ and $i^*_{dq_2}$. The error between the actual synchronous and reference currents is then used as the input to the PI controllers to generate the voltages in the synchronous reference frame, v_{dq_1} and v_{dq_2}. The decoupling matrix in (2.5) is then utilized to obtain the decoupled voltages in the synchronous frame, v_{DQ_1} and v_{DQ_2}. At this stage, the inverse Park transformation can be used to generate stationary reference frame voltages which are then used in the switching algorithm to generate the gate pulses that are sent to the VSI.

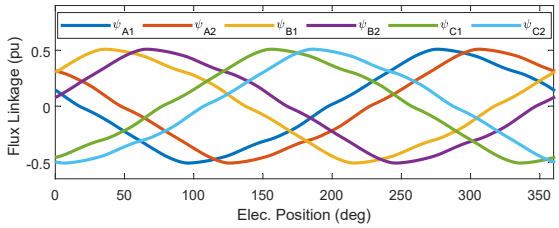
2.3.2 VSD Control

Shifting the focus to the VSD transformation, different current control techniques need to be adopted due to the orthogonal subspaces that are generated from the VSD Clarke and Park transformations seen in (2.3) and (2.4). Using the VSD transformation, it is important to understand how each component of the stationary and synchronous reference frames are interpreted so that controllers can be developed for the dq and xy_r subspaces. To see the physical interpretation of each subspace, it can be assumed that a perfectly sinusoidal input current at a fundamental frequency, seen in Figure 2.4a, is used for excitation of a 100 kW IPMSM. Since this current waveform will have no harmonic content, the xy components will be negligible and the physical interpretation of this subspace will not be realized. Therefore, the phase flux linkage waveforms that contain harmonic distortion and that are generated based

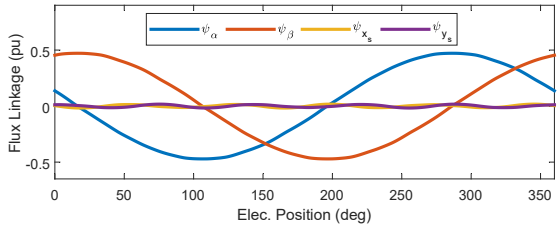
on the sinusoidal current excitation will be analyzed so that the xy subspace can be interpreted. The phase flux linkages seen in Figure 2.4b are calculated using Finite Element Analysis (FEA) for the given sinusoidal current excitation from Figure 2.4a where ψ represents flux linkage.



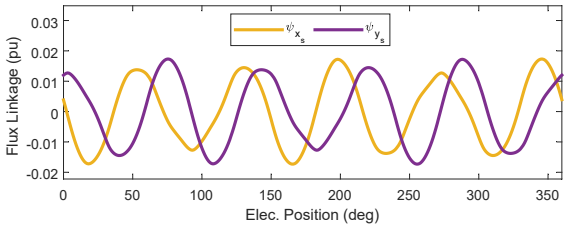
(a) Phase Current



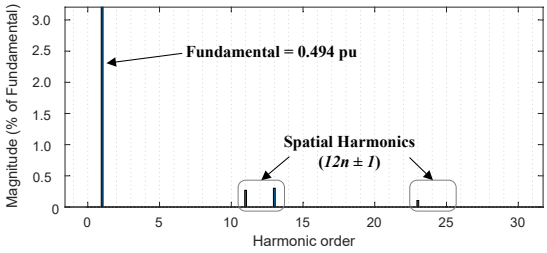
(b) Phase Flux Linkage



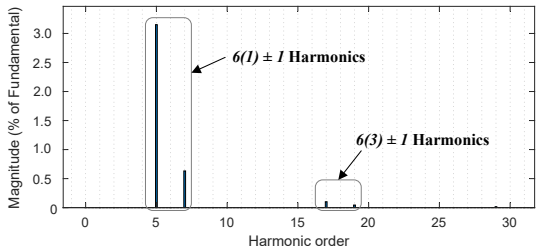
(c) Stationary Frame Flux Linkage



(d) Stationary Frame xy_s Flux Linkage



(e) FFT Analysis of ψ_α



(f) FFT Analysis of ψ_{x_s}

Figure 2.4: Phase and Stationary Reference Frame Components Used for Interpreting xy_s Subspace

It can be seen in Figure 2.4c that applying the VSD Clarke transformation from (2.3) to the phase flux linkage waveforms generates both $\alpha\beta$ and xy_s flux components in the stationary reference frame where an enlarged figure of the xy_s components can be seen in Figure 2.4d. It is clear from Figure 2.4e that the fundamental frequency

component of the $\alpha\beta$ components is dominant with very low harmonics of the order $12n \pm 1$ ($n = 1,2,3,\dots$) due to the spatial harmonics of the machine. However, when analyzing the FFT of the xy_s components in the stationary reference frame, it can be seen in Figure 2.4f that the x_s waveform is made up of harmonics of the order $6n \pm 1$ ($n = 1,3,5,\dots$) – this is also the case for the y_s component.

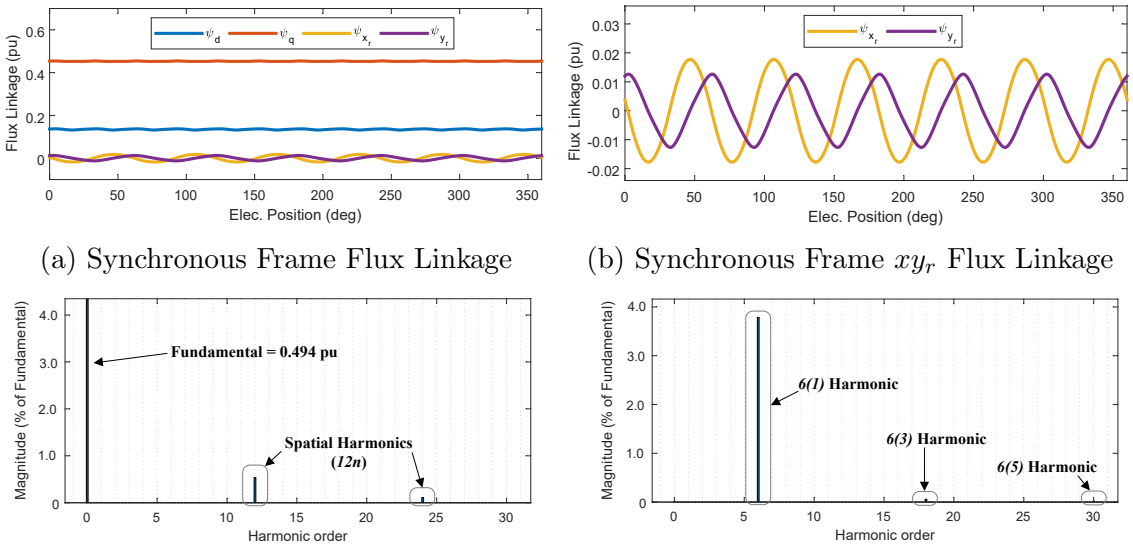
When looking into the VSD Park transformation in (2.4), in a similar way to three-phase systems, the generated dq components are represented by a DC offset which allows for simple PI controllers to be implemented for each component. Additionally, in the synchronous reference frame, the 12^{th} harmonic is present on the dq components due to spatial harmonics. However, (2.4) does not transform the xy components when going from the stationary reference frame to the synchronous reference frame, and therefore while the dq components are represented by a DC offset and being controlled with PI controllers, the xy components are still represented by the harmonics of the order $6n \pm 1$ ($n = 1,3,5,\dots$), which makes them difficult to control.

In recent literature, adaptations to the Park transformation have been proposed so that the xy_r components can be more easily controlled. It is important to note that the xy_r components are trying to be forced to zero since this subspace is where the harmonics of the system that do not contribute to torque production are being mapped [9]. Therefore, by effectively reducing the xy_r component to as close to zero as possible, the waveforms energizing the drive system will have less harmonic distortion. Due to control of the xy subspace being more easily completed in the synchronous reference frame, [19] proposes a Park transformation that rotates the

xy_s components in the opposite direction of the $\alpha\beta$ components:

$$\begin{bmatrix} f_d \\ f_q \\ f_{x_r} \\ f_{y_r} \end{bmatrix} = T_{Park_{Neg}} \begin{bmatrix} f_\alpha \\ f_\beta \\ f_{x_s} \\ f_{y_s} \end{bmatrix} \qquad T_{Park_{Neg}} = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 0 & 0 \\ -\sin(\theta) & \cos(\theta) & 0 & 0 \\ 0 & 0 & \cos(-\theta) & \sin(-\theta) \\ 0 & 0 & -\sin(-\theta) & \cos(-\theta) \end{bmatrix} \tag{2.6}$$

Applying this transformation to the stationary reference frame components seen in Figure 2.4c will generate dq and xy_r components in the synchronous reference frame which can be seen in Figure 2.5a. Examining the waveforms in the synchronous reference frame, the Park transformation applied to the dq components remains the same and therefore these components are once again represented by a dominant DC offset that can be controlled using PI controllers as seen in Figure 2.5c. However, with the xy_s components now being rotated in the opposite direction compared to the $\alpha\beta$ component, FFT analysis shows that the dominant harmonics of the resultant waveforms in the xy_r subspace are of the $6n$ (n = 1,3,5,...) order which can be seen in Figure 2.5d.



(a) Synchronous Frame Flux Linkage

(b) Synchronous Frame xy_r Flux Linkage

(c) FFT Analysis of ψ_d

(d) FFT Analysis of ψ_{x_r}

Figure 2.5: Synchronous Reference Frame Flux Linkages with FFT Results used for Interpreting the xy_r subspace

Adopting the transformation from [19], the control scheme from Figure 2.3 must be altered to accommodate the xy subspace component and improve the $\alpha\beta$ and xy_s voltage signals that are used for SVPWM. Since the xy_r subspace is represented by harmonics of the order $6n$ (n = 1,3,5,...), Proportional Resonant (PR) controllers can be used as proposed in [17]. These PR controllers which can be seen in Figure 2.6 are tuned at six times the fundamental frequency to control the xy_r components to be as close to zero as possible. This exact technique is seen again in [23], however, another method is seen in [24] that does not bother to rotate the xy subspace to the synchronous reference frame and instead uses two PR controllers tuned at five and seven times the fundamental frequency to help minimize the xy_s components to zero.

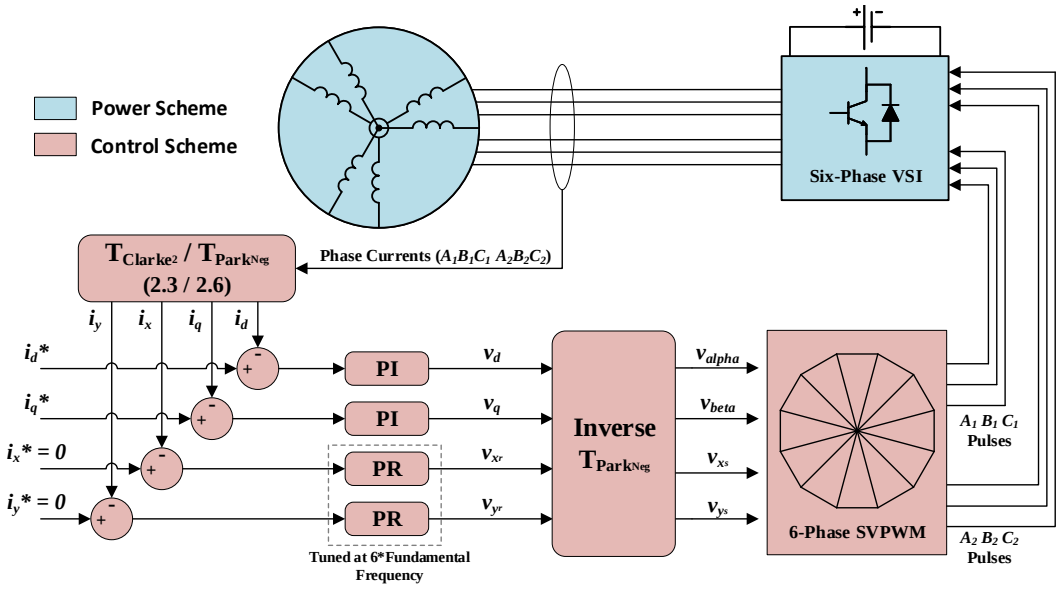


Figure 2.6: Current Control Scheme for FOC, VSD Transformation Based Controller Utilizing SVPWM

With the control techniques for both the coordinate transformations discussed, the control schemes in Figure 2.3 and Figure 2.6 both consider SVPWM. Using these control schemes, SVPWM switching techniques can be analyzed using different combinations of voltage vectors for calculated dwell times. Alternatively, SPWM can also be implemented to control dual three-phase machines and this will also be analyzed for the sake of comparison in which double zero sequence injection must be utilized so that the performance between SVPWM and SPWM is similar. With the focus of this thesis being on optimizing switching techniques to enhance the efficiency of six-phase inverters, the simulations completed throughout this thesis will assume the controllers in Figure 2.3 and Figure 2.6 are being implemented. Additionally, other aspects to be assumed include the phase order of the controlled drive system being $A_1B_1C_1A_2B_2C_2$, a VSD transformation-based drive model being used in the simulation environment, and the six-phase VSI being limited to only two voltage levels.

2.4 Switching Techniques

As the focus switches from the overall controller of a dual three-phase drive system to the switching techniques used to generate pulses for the two-level six-phase VSI, a detailed literature review of the existing techniques will be analyzed. The resultant pulses that are generated for the VSI can be produced using different switching techniques that take advantage of the 64 available switching states of the six-phase inverter. Alternatively, different three-phase switching techniques can be implemented for dual three-phase drive systems when assuming a Double dq based controller since each three-phase set is controlled as its own respective three-phase system. Furthermore, similar to their three-phase counterparts, carrier-based SPWM techniques can be implemented for multiphase drive systems. However, in the literature, it is discussed how zero sequence injection is required for both three-phase winding sets so that SPWM switching can obtain the same DC-link voltage utilization as other switching techniques. Another switching technique commonly discussed in the literature is the vector classification-based switching technique which is first proposed in [25]. The theory of this switching technique is further discussed in [26, 27] where the six-phase VSI is treated as two independent three-phase inverters and therefore, three-phase switching techniques can be applied independently to each inverter. Lastly, the most popular switching technique throughout the literature is SVPWM which is first proposed in [5]. SVPWM is the most discussed switching technique for multi-phase motor drives due to the increase in the number of utilizable voltage vectors compared to three-phase switching techniques and SPWM. In [3, 9, 13, 28, 29], in-depth surveys to review the advances in each of the aforementioned switching techniques from literature from the past two decades are provided.

2.4.1 Sinusoidal Pulse Width Modulation

When considering the SPWM technique for dual three-phase drives, it is important to note that the theory of SPWM is independent of the number of phases present in the drive system [30]. This means that, in terms of SPWM, the same techniques and theory commonly used for three-phase drive systems also applies to dual three-phase systems with the same major benefit of easy implementation [29, 31]. Like their three-phase counterparts, dual three-phase drive systems should consider the injection of zero sequence components to both three-phase winding sets to utilize similar DC-link voltage compared to other switching techniques [29]. This common technique for six-phase drives is referred to as double zero sequence injection (DZSI) SPWM due to the perception that the six-phase VSI is viewed as two separate three-phase inverters that are connected to the same DC-link supply [32]. This technique is further investigated in [33] where a generalized concept of n^{th} harmonic injection for n-phase inverters is discussed as well as the appropriate harmonics that should be injected to maximize DC-Link utilization. Furthermore, in [34], different carriers are compared using DZSI SPWM and how they affect power losses in IGBT Modules. Additionally, [35] analyzes the output current ripple of dual three-phase drives when DZSI SPWM is used to generate the pulses for the VSI switches. In more general comparisons, the concept of DZSI SPWM can also be compared to different SVPWM switching techniques in terms of harmonic performance [36, 37].

Although the focus of this thesis is mainly on the SVPWM switching techniques, the DZSI SPWM strategy used in [36] will also be analyzed for the sake of comparison. To establish a good comparison between the different switching techniques that have

been discussed, for DZSI SPWM, when looking at the six-phase VSI from a dual three-phase load point of view, two three-phase VSI's are separately controlled, forming two isolated polygons constructed of six voltage vectors similar to three-phase SVPWM [32]. This is also similar to the vector classification algorithm which will not be covered in the scope of this thesis. The difference between the two controlled three-phase VSI's is that there exists a 30° phase shift between the reference vector of each three-phase set and this is due to the 30° phase shift between the winding sets. Specifically for SPWM, this 30° phase shift also needs to be considered between the zero sequence components that are injected into the voltage set of each winding set. The overall current control scheme using a VSD based controller can be seen in Figure 2.7.

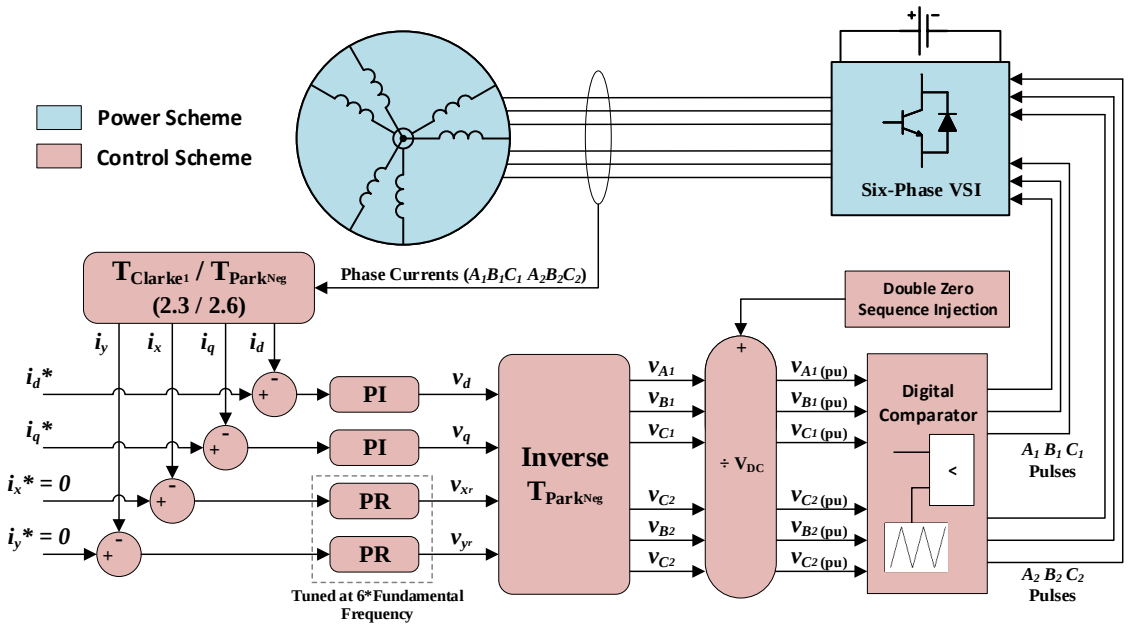


Figure 2.7: Current Control Scheme for FOC, VSD Transformation Based Controller Utilizing DZSI SPWM

As this thesis focuses on six-phase VSI efficiency, one of the most important factors to be examined is the average switching frequency. Throughout this thesis, the average switching frequency will be calculated for one full electrical cycle of the dual three-phase drive system which is not what is typically done throughout the literature. The idea of using one full electrical will be further discussed when analyzing SVPWM. It will also be assumed throughout this thesis that the switching frequency of the carrier waveform in the DSP is set to 20 kHz for each switching technique that is being examined. This is due to this switching frequency being near the maximum allowable frequency for the IGBT module being utilized. To ensure that the desired switching frequency of 20 kHz is maintained with balanced switching amongst all switches, each switch must turn on and off only once in the 50 μs sampling time which is calculated based on the specified switching frequency. Like, SPWM of three-phase drive systems, a major benefit of DZSI SPWM of six-phase VSIs is that the ideal scenario of each switch turning on and off only one time in each sampling period occurs. This is due to the simple implementation of this technique where the durations of the gate pulses for each switch of the VSI are determined by comparing the carrier waveform with the phase voltages which can be observed in Figure 2.7. For example, when the phase A_1 voltage is greater than the carrier waveform, the top switch of the corresponding phase leg of the VSI is on and the bottom switch is off. When the phase voltage is less than the carrier waveform, the top switch then turns off and the bottom switch turns on – more simply, the two switches of each phase leg are complimentary. Furthermore, it is important to recall that the switching state of each phase leg is represented using a binary system throughout this thesis where the binary number "0" means the bottom switch is on and the binary number "1" implies

that the top switch is on. The overall control scheme and an example of the resultant waveforms for one phase leg can be seen in Figure 2.7 and Figure 2.8 respectively.

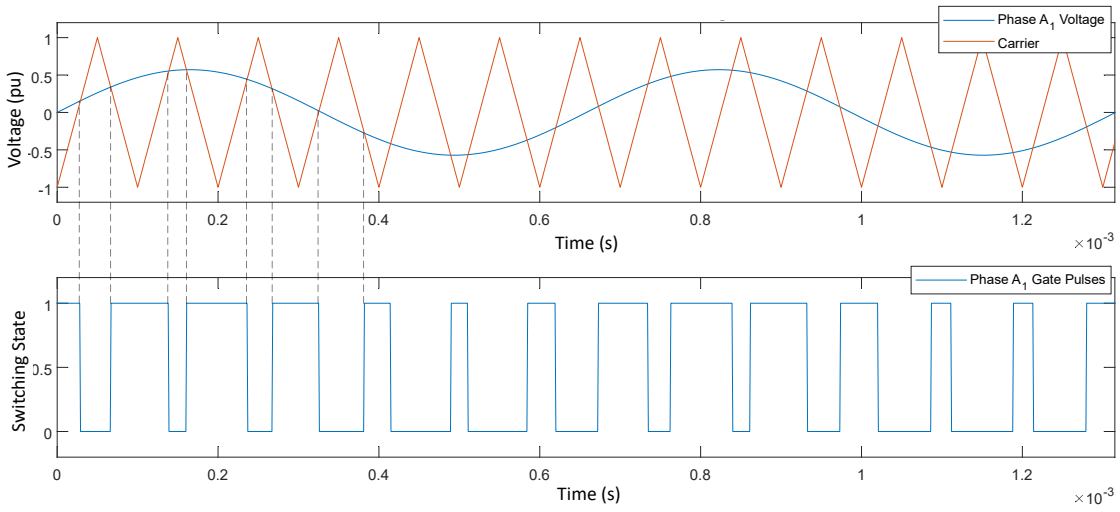


Figure 2.8: DZSI SPWM Waveforms for Generation of Phase Leg A_1 Gate Pulses

Throughout this thesis, all switching signals generated using DZSI SPWM use the same carrier waveform seen in Figure 2.8 and the same voltage comparison control method seen in Figure 2.7. The brief analysis of this technique can be used for comparison with many of the different SVPWM techniques especially since DZSI SPWM has a balanced switching pattern that provides the exact switching frequency of 20 kHz for each switch of the VSI.

2.4.2 Space Vector Pulse Width Modulation

In contrast, the most popular switching method of multiphase machines throughout the literature is SVPWM due to the exponential increase in voltage vectors as a result of the linear increase in the phase number of the drive system. As previously discussed, with the focus of this thesis being on the dual three-phase drive system with isolated

neutral points, the zero sequence components in the Clarke and Park transformations can be neglected. With this specific drive system, of the 64 possible switching states, there are 49 possible voltage vectors in the stationary reference frame, $\alpha\beta$, subspace that can be chosen. The per-unit magnitude and phase of these voltage vectors are produced using (2.7) where S_{A_1}, S_{B_1}, S_{C_1}, S_{A_2}, S_{B_2}, and S_{C_2} represent the switching state of each phase leg as previously discussed.

$$V_{\alpha\beta} = \frac{1}{3}(S_{A_1} + S_{B_1}e^{j(\frac{4\pi}{6})} + S_{C_1}e^{j(\frac{8\pi}{6})} + S_{A_2}e^{j(\frac{\pi}{6})} + S_{B_2}e^{j(\frac{5\pi}{6})} + S_{C_2}e^{j(\frac{9\pi}{6})}) \tag{2.7}$$

However, it is important to remember that for each voltage vector that is selected in the $\alpha\beta$ subspace, there is also a corresponding voltage vector in the stationary reference frame, xy_s, subspace which can be represented using the equation:

$$V_{xy_s} = \frac{1}{3}(S_{A_1} + S_{B_1}e^{j(\frac{8\pi}{6})} + S_{C_1}e^{j(\frac{4\pi}{6})} + S_{A_2}e^{j(\frac{5\pi}{6})} + S_{B_2}e^{j(\frac{\pi}{6})} + S_{C_2}e^{j(\frac{9\pi}{6})}) \tag{2.8}$$

The equations above will calculate the magnitude and phase of each vector for every switching state and these vectors can further be mapped to the $\alpha\beta$ and xy_s subspaces. This method is used to realize the corresponding xy_s voltage vector for every $\alpha\beta$ vector which can be observed in Figure 2.9 where almost all of the 49 possible vectors have different magnitudes and phase angles for the xy_s subspace due to the transposition of the angles seen in (2.8) compared to (2.7). With these equations calculating the per-unit magnitude of each vector, four different magnitudes are calculated, plus redundant zero voltage vectors. The different magnitudes of vectors are referenced based on their magnitude in the $\alpha\beta$ plane and will be referred to as large, medium-large, medium, and small vectors which are all summarized in Table 2.1.

Table 2.1: VSD Based Voltage Vector Classification and Magnitudes

Label	**Decimal Number Representation**	$\boldsymbol{\alpha\beta}$ **Magnitude**	$\boldsymbol{xy_s}$ **Magnitude**
Large	36, 52, 54, 22, 18, 26 27, 11, 09, 41, 45, 37	$\lvert V_L\rvert = 0.644V_{DC}$	$\lvert V_S\rvert = 0.1725V_{DC}$
Medium-Large	53, 38, 20, 50, 30, 19 10, 25, 43, 13, 33, 44	$\lvert V_{ML}\rvert = 0.471V_{DC}$	$\lvert V_{ML}\rvert = 0.471V_{DC}$
Medium	32, 39, 04, 60, 48, 55 06, 62, 16, 23, 02, 58 24, 31, 03, 59, 08, 15 01, 57, 40, 47, 05, 61	$\lvert V_M\rvert = 0.333V_{DC}$	$\lvert V_M\rvert = 0.333V_{DC}$
Small	46, 21, 34, 28, 51, 14 17, 42, 29, 35, 12, 49	$\lvert V_S\rvert = 0.1725V_{DC}$	$\lvert V_L\rvert = 0.644V_{DC}$
Zero	00, 07, 56, 63	$\lvert V_0\rvert = 0$	$\lvert V_0\rvert = 0$

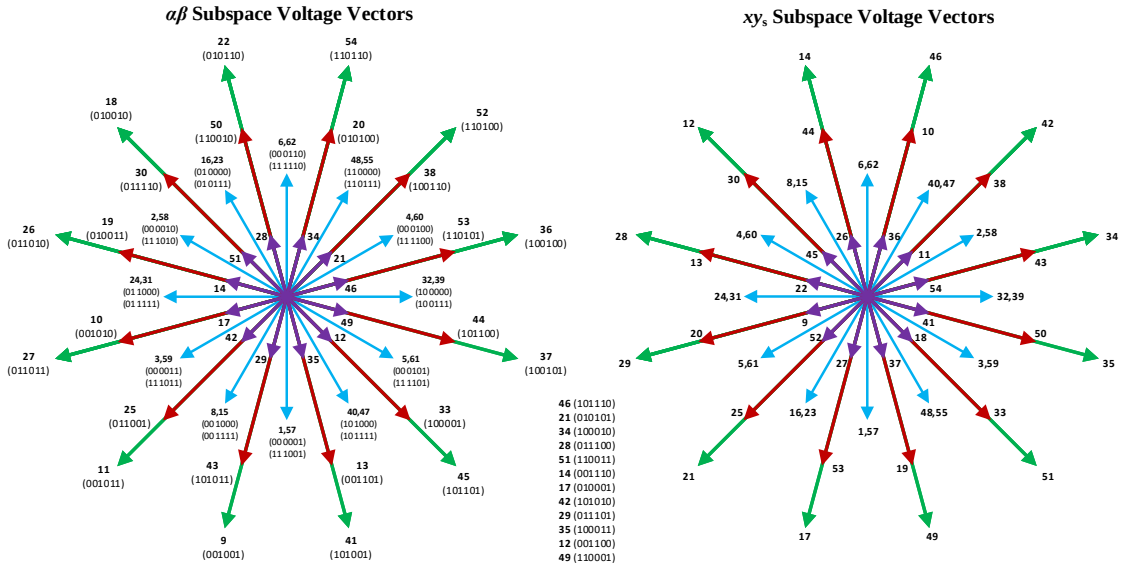


Figure 2.9: Dual Three-Phase Drive System Voltage Vectors in the Stationary Reference Frame

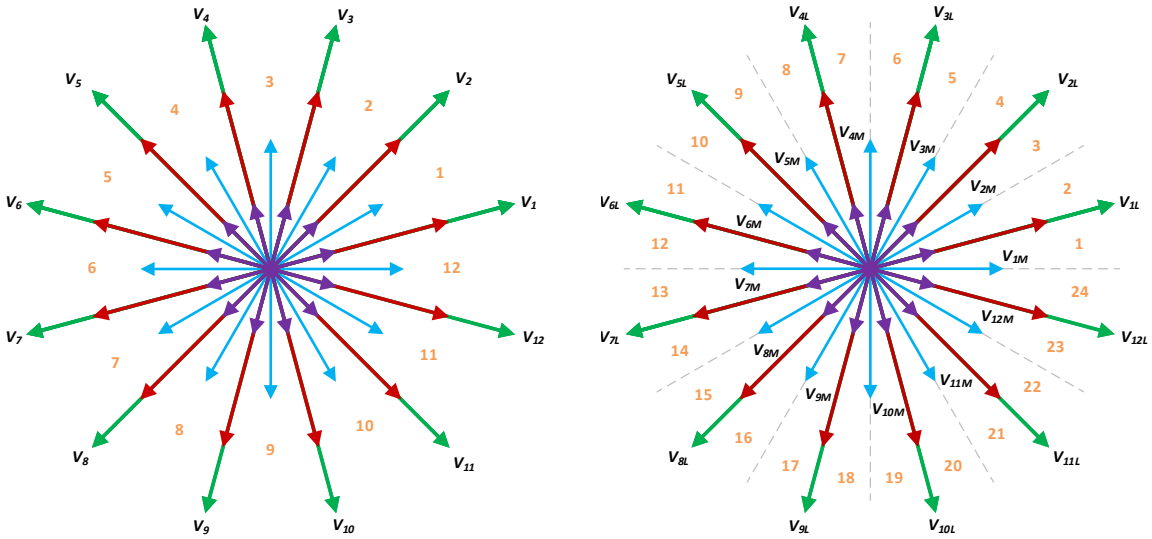
As previously discussed, in Figure 2.9, every voltage vector is referenced using a decimal number that corresponds to a six-digit binary number which represents the switching states of each phase leg assuming the phase order of $A_1B_1C_1A_2B_2C_2$. Recall that, a switching state of the binary number "1" means that the top switch of the phase leg is on and a switching state of the binary number "0" means that the bottom switch of the phase leg is on – where the two switches in each phase leg are complimentary. When SVPWM was first discussed in [5], it was discussed that the number of voltage vectors needed to control dual three-phase drive systems was the same as the number of dimensions in the system with an additional zero vector. Therefore, since the zero-sequence components can be ignored in this specific topology, four voltage vectors are required for the α, β, x, and y dimensions as well as a fifth zero vector. In general, for an n-phase machine, $n-1$ voltage vectors should be used [38]. Furthermore, since only the $\alpha\beta$ subspace contributes to electromagnetic torque production, the goal of this switching technique is to maintain the volt-seconds of the $\alpha\beta$ subspace to produce the desired amount of torque while at the same time maintain the volt-seconds of the xy_s subspace to remain as close to zero as possible [5]. This can be done using any combination of voltage vectors with [5] first proposing a 12-sector switching method using the four adjacent large vectors of the $\alpha\beta$ subspace. In this paper, only the large vectors of the $\alpha\beta$ plane are used due to the corresponding xy_s vectors having the smallest magnitude. This means that the desired concept of maintaining the volt-seconds of xy_s to be zero will be easier since only small magnitude voltage vectors are being applied to the xy_s subspace.

This proposed method using four large voltage vectors and one zero voltage vector has been the basis for modified and improved six-phase SVPWM techniques in the

last 20 years. This method was further observed when using different winding phase shifts between the two sets of three-phase windings within the drive system in [39] and carried over to a five-phase drive system in [38, 40]. In [41], the classic SVPWM scheme for six-phase machines is generalized for n-phase machines while [42] compares this n-phase generalized SVPWM technique to SPWM for a nine-phase drive system. Once again, the importance of including all dimensions in the SVPWM technique and not excluding the xy subspace is discussed in [43]. SVPWM techniques have also been improved for different coordinate transformations, specifically, the Double dq transformation and different multiphase drive system topologies as seen in [44] and [45, 46], respectively, with comparisons of SVPWM techniques for different coordinate transformations given in [47]. Furthermore, the use of SVPWM in the overmodulation region is discussed in [26, 27, 48, 49, 50], however, that is outside the scope of this thesis.

This thesis focuses on the machine's constant torque operating region for SVPWM switching schemes and, unlike other literature, focuses on the efficiency of the six-phase VSI specifically. Throughout this section, existing switching techniques will be examined and unique methods to reduce the average switching frequency will be observed in an effort to improve the overall six-phase VSI efficiency over a wide operating range. When looking at the existing literature for SVPWM techniques in the constant torque region, the main focus is typically to reduce the phase current THD with very few papers focusing on the average switching frequency across multiple sampling intervals. One of the common methods that is often associated with improving the harmonic performance of different switching techniques is the idea of increasing the sampling frequency. This typically corresponds to a decrease in the

number of different voltage vectors applied in one switching period where the duration of each voltage vector is referred to as a time-segment. Consequently, the more time-segments used within one switching period of a switching algorithm, the more switchings between the five selected voltage vectors occur. For example, the idea of using 9, 11, or even 13 time-segments by means of only the large vectors in the $\alpha\beta$ plane was first proposed in [51] along with a technique for easier DSP implementation of six-phase drive system SVPWM to reduce computation time. Similar switching algorithms are also discussed in [52] along with strategies for implementing different time segment methods to the DSP. Furthermore, aside from improving harmonic performance, some papers have even investigated solely reducing the switching frequency, but only looking into the conventional SVPWM method using four large and one zero voltage vector [53]. With the original SVPWM, assuming the $\alpha\beta$ subspace is divided into 12 sectors based on the 12 large voltage vectors, [54] was the first to propose a 24 sector switching algorithm using three large, one medium, and one zero voltage vector with a comparison to 12 sector continuous and discontinuous algorithms. Note that continuous switching refers to having every switch of the inverter turn on and off at least one time and discontinuous switching refers to having at least one inverter leg not switching during the sampling period. Figure 2.10 shows how the $\alpha\beta$ subspace is divided for both 12 and 24 sector switching methods.



(a) 12 Sector Method (b) 24 Sector Method

Figure 2.10: Sector Definition Based on the $\alpha\beta$ Subspace Voltage Vectors

The switching technique that uses three large, one medium, and one zero voltage vector was further investigated in [55] where different zero vectors are used in different locations of the switching pattern in an attempt to minimize the phase current THD. More recently, [56] proposes a new 24 sector switching pattern that uses three large, two medium, and one zero voltage vector where the medium vectors are dedicated to ease the transitions between the large and zero vectors. However, when using the widely adopted dwell time calculation that comes from [5] which can be seen in (2.9), this method would result in five dwell times for the six different voltage vectors so it must then be assumed that the two transition vectors are not independent of one another. In (2.9), v_j^k represents the voltage projection of the k^{th} vector on the j axis which includes the d, q, x_r, and y_r axes. Additionally, T_k represents the dwell time of the k^{th} vector during the sampling time, T_s. Lastly, v_j^* represents the j axis voltage

reference values where the reference voltage for the x_r and y_r axes are set to zero.

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_0 \end{bmatrix} = \begin{bmatrix} v_d^1 & v_d^2 & v_d^3 & v_d^4 & v_d^5 \\ v_q^1 & v_q^2 & v_q^3 & v_q^4 & v_q^5 \\ v_x^1 & v_x^2 & v_x^3 & v_x^4 & v_x^5 \\ v_y^1 & v_y^2 & v_y^3 & v_y^4 & v_y^5 \\ 1 & 1 & 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} v_d^* T_s \\ v_q^* T_s \\ 0 \\ 0 \\ T_s \end{bmatrix} \tag{2.9}$$

In addition, [56] analyzes different 12 sector and 24 sector techniques previously proposed in the literature with a comparison of phase current THD and an investigation into how these techniques transition to the overmodulation region. Furthermore, [57] and [58] have implemented 24 sector switching algorithms that use two large, two medium-large, and one zero voltage vector that is implemented in different locations of the switching cycle . Alternatively, instead of using zero vectors, [59] uses opposite large voltage vectors to obtain the desired magnitude of the reference voltage vector which has good performance at high modulation indexes. Lastly, [60] proposes different 24 sector technique variations of three large, one medium, and one zero voltage vector, as well as two large, one medium-large, one medium, and one zero voltage vector algorithms and compares them with other commonly used SVPWM techniques in terms of harmonic performance for a wide operating range.

Throughout all these pieces of literature, the average switching frequency is calculated based on the switching instances of one sector and any transitions in switching states between sectors are not included. Therefore, to calculate the average switching frequency, $f_{sw_{avg}}$, switching instances over one full electrical cycle will be considered with the frequency of the switching carrier waveform, $f_{sw_{carr}}$, set at 20 kHz where

(2.10) can be used to provide an accurate average switching frequency calculation for each of the more popular techniques to be discussed.

$$f_{sw_{avg}} = \left(\frac{\#\ of\ switchings\ over\ \textbf{\textit{one electrical cycle}}}{24 * 12} \right) (f_{sw_{carr}}) \tag{2.10}$$

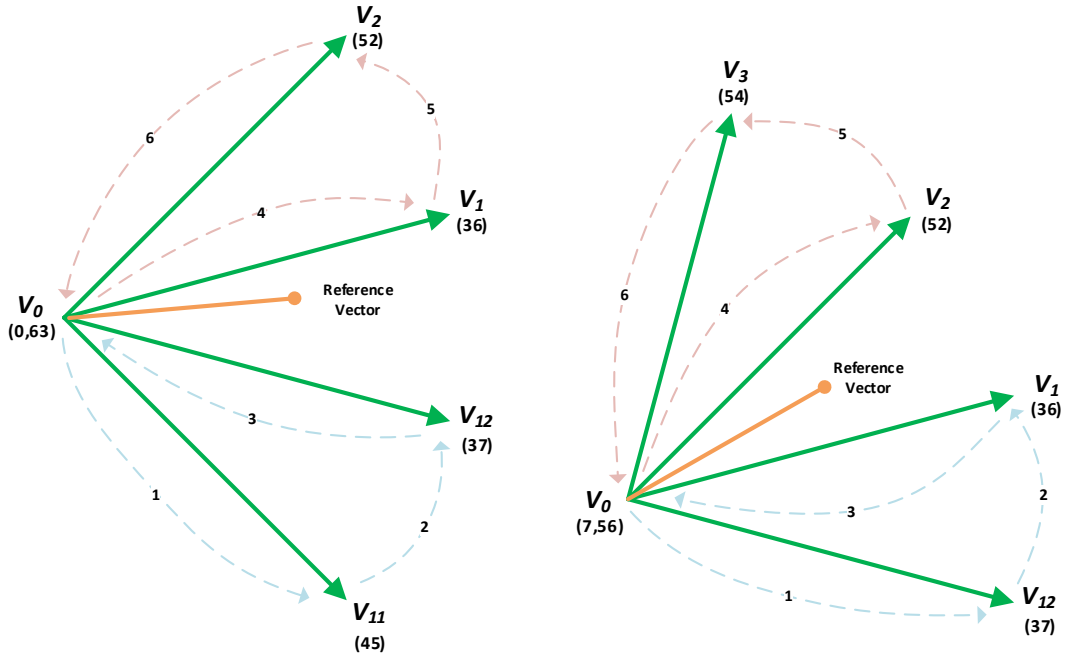
It is important to note that to allow for a proper comparison of the average switching frequency for each technique, one full electrical cycle is considered to be 24 sample periods. This allows for a 24 sector technique to change sectors every sampling period and make it through the entire electrical cycle. However, this also means that for 12 sector techniques, the sector changes every two sample periods so that one full electrical cycle is completed after 24 sample periods.

When it comes to minimizing the switching frequency of the existing techniques, the number of time segments utilized will need to be adjusted and the order in which the voltage vectors are applied can be altered. It is also important to know that there is typically a trade-off between minimizing the switching frequency and increasing the phase current THD. For this reason, the resultant phase current THD of each switching technique using different time segments will also be observed. With the focus of the drive systems discussed in this thesis being high power, variable speed systems, it is important that the switching frequency remains the same as the sampling frequency, $f_{samp} = f_{sw}$, to help reduce computation time and costs. Another important consideration for these switching techniques is being able to easily implement these techniques using a DSP where the PWM registers are designed to only turn on and off one time in each switching period. This means that the switching pattern within each sampling/switching period must have voltage vectors applied that will result in the phase voltage of each phase leg switching on and off only one time.

When looking into the four large and one zero voltage vector technique, [51] and [52] propose modifications to this switching technique that require the sampling frequency to be up to double the switching frequency but this should be avoided. Therefore, if this technique is to be implemented utilizing the existing PWM drivers of the DSP, it must be implemented as a 7 time-segment, continuous, 12 sector algorithm with the redundancy in the zero voltage vectors being taken advantage of. Recall that there exist four different zero vectors that can be used that are represented by the decimal numbers 00, 07, 56, and 63. Furthermore, the naming convention of the switching methods discussed in this thesis will be either a "C" or "D" to specify continuous or discontinuous switching, then a "12" or "24" to specify the $\alpha\beta$ subspace being divided into 12 or 24 sectors, followed by the combination of voltage vectors being used. With this convention, the four large and one zero voltage vector technique discussed will be referred to as C12-4L1Z and the switching characteristics can be seen in Table 2.2 and Figure 2.11.

Table 2.2: Switching Sequence for Each Sector Represented by Decimal Numbers for the C12-4L1Z Switching Technique Using 7 Time Segments

Sector	**Decimal Number Switching Sequence**	**Sector**	**Decimal Number Switching Sequence**
1	**07** – 37 – 36 – **56** – 52 – 54 – **07**	7	**56** – 26 – 27 – **07** – 11 – 09 – **56**
2	**00** – 36 – 52 – **63** – 54 – 22 – **07**	8	**63** – 27 – 11 – **00** – 09 – 41 – **63**
3	**56** – 52 – 54 – **07** – 22 – 18 – **56**	9	**07** – 11 – 09 – **56** – 41 – 45 – **07**
4	**63** – 54 – 22 – **00** – 18 – 26 – **63**	10	**00** – 09 – 41 – **63** – 45 – 37 – **00**
5	**07** – 22 – 18 – **56** – 26 – 27 – **07**	11	**56** – 41 – 45 – **07** – 37 – 36 – **56**
6	**00** – 18 – 26 – **63** – 27 – 11 – **00**	12	**63** – 45 – 37 – **00** – 36 – 52 – **63**



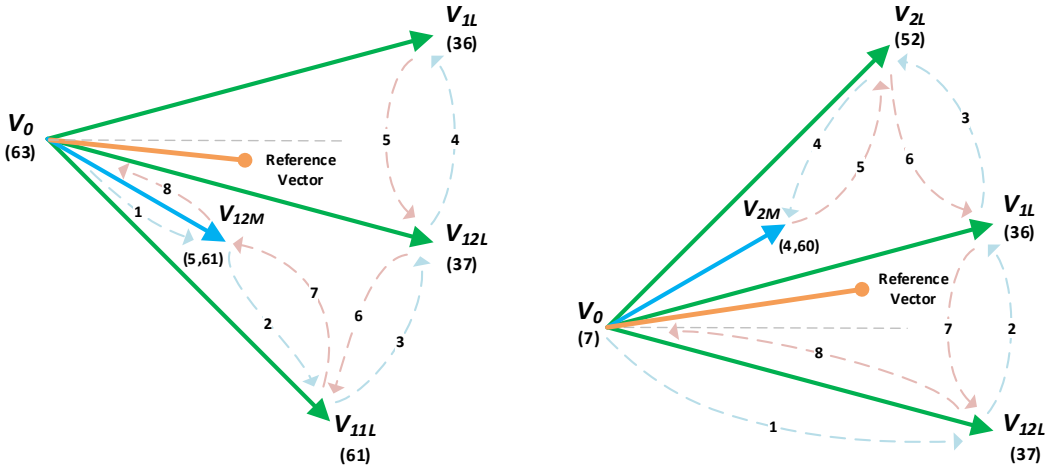
(a) Sector 12 (b) Sector 1

Figure 2.11: Visual Representation for the Sequence of the Voltage Vectors applied for the C12-4L1Z Technique Using 7 Time Segments

From Table 2.2, it can be seen that one of the benefits of this modified technique from the literature is that it can be implemented to the DSP with $f_{samp} = f_{sw}$ since each phase turns on and off only one time in each sampling/switching period. However, the actual average switching frequency needs to consider the switching changes that occur during the change in sectors as a result of the change in zero vectors being used. To calculate the average switching frequency, (2.10) can be used and for a defined carrier switching frequency, $f_{sw_{carr}}$, of 20 kHz, the average switching frequency, $f_{sw_{avg}}$, is calculated to be 22.5 kHz.

The aforementioned C12-4L1Z technique uses only the large vectors of the $\alpha\beta$ plane to limit the magnitude of the voltage vectors applied to the xy_s subspace, however, it was first proposed in [54] to take advantage of the redundancy in the

medium vectors to help reduce the phase current THD. This technique, therefore, uses three large, one medium, and one zero voltage vector and is implemented with a sampling frequency that is twice the switching frequency, $f_{samp} = 2f_{sw}$. With this technique also being discussed in [55], both 9 and 11 time-segments have been proposed. With the focus of this thesis being on reducing the switching frequency, the 9 time-segment, discontinuous switching technique will be reviewed which generates the lowest switching frequency of the different methods for this specific technique proposed in the literature. Due to the redundancy in the medium vectors when looking at Figure 2.9, this switching technique allows for a smoother transition between each voltage vector, especially when going from a large vector to zero vector. Additionally, with the angle in which the medium vectors sit, this switching technique has the best performance when the $\alpha\beta$ plane is split into 24 sectors rather than 12 as in Figure 2.10b. As a result, this technique is referred to as D24-3L1M1Z and the switching characteristics can be observed in Figure 2.12 and Table 2.3.



(a) Sector 24 (b) Sector 1

Figure 2.12: Visual Representation for the Sequence of the Voltage Vectors applied for the D24-3L1M1Z Technique Using 9 Time Segments

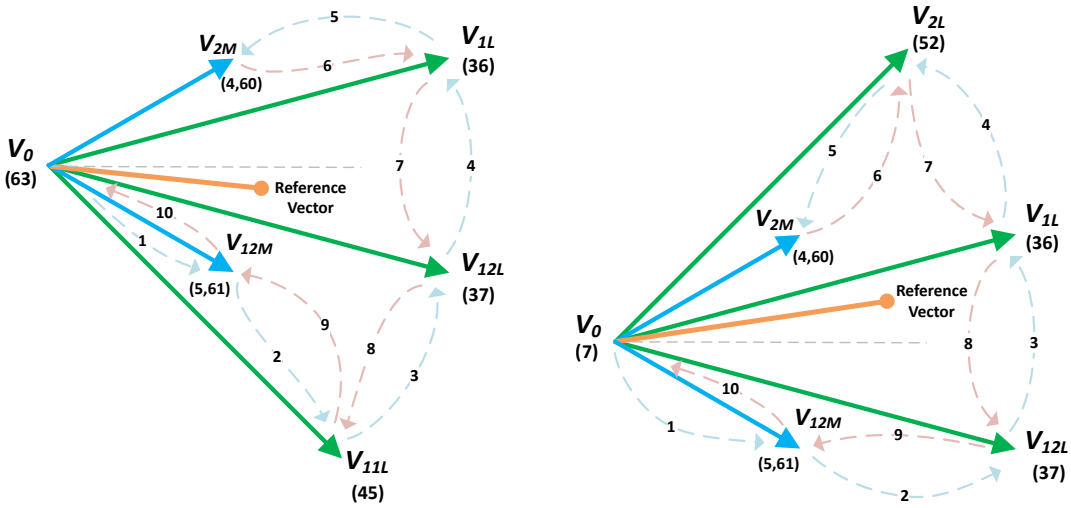
Table 2.3: Switching Sequence for Each Sector Represented by Decimal Numbers for the D24-3L1M1Z Switching Technique Using 9 Time Segments

Sector	**Decimal Number Switching Sequence**	**Sector**	**Decimal Number Switching Sequence**
1	**07** – 37 – 36 – 52 – 60 – 52 – 36 – 37 – **07**	13	**56** – 26 – 27 – 11 – 03 – 11 – 27 – 26 – **56**
2	**07** – 39 – 37 – 36 – 52 – 36 – 37 – 39 – **07**	14	**56** – 24 – 26 – 27 – 11 – 27 – 26 – 24 – **56**
3	**00** – 36 – 52 – 54 – 55 – 54 – 52 – 36 – **00**	15	**63** – 27 – 11 – 09 – 08 – 09 – 11 – 27 – **63**
4	**00** – 04 – 36 – 52 – 54 – 52 – 36 – 04 – **00**	16	**63** – 59 – 27 – 11 – 09 – 11 – 27 – 59 – **63**
5	**56** – 52 – 54 – 22 – 06 – 22 – 54 – 52 – **56**	17	**07** – 11 – 09 – 41 – 57 – 41 – 09 – 11 – **07**
6	**56** – 48 – 52 – 54 – 22 – 54 – 52 – 48 – **56**	18	**07** – 15 – 11 – 09 – 41 – 09 – 11 – 15 – **07**
7	**63** – 54 – 22 – 18 – 16 – 18 – 22 – 54 – **63**	19	**00** – 09 – 41 – 45 – 47 – 45 – 41 – 09 – **00**
8	**63** – 62 – 54 – 22 – 18 – 22 – 54 – 62 – **63**	20	**00** – 01 – 09 – 41 – 45 – 41 – 09 – 01 – **00**
9	**07** – 22 – 18 – 26 – 58 – 26 – 18 – 22 – **07**	21	**56** – 41 – 45 – 37 – 05 – 37 – 45 – 41 – **56**
10	**07** – 23 – 22 – 18 – 26 – 18 – 22 – 23 – **07**	22	**56** – 40 – 41 – 45 – 37 – 45 – 41 – 40 – **56**
11	**00** – 18 – 26 – 27 – 31 – 27 – 26 – 18 – **00**	23	**63** – 45 – 37 – 36 – 32 – 36 – 37 – 45 – **63**
12	**00** – 02 – 18 – 26 – 27 – 26 – 18 – 02 – **00**	24	**63** – 61 – 45 – 37 – 36 – 37 – 45 – 61 – **63**

Referring to Table 2.3, when implementing the D24-3L1M1Z switching technique, implementation to DSP can be accomplished with $f_{samp} = f_{sw}$ due to each switch, at maximum, only turning on and off one time. An added benefit of this balanced 9 time-segment switching technique is that there is discontinuous switching, where at least one switch in each sampling period does not turn on or off and this helps to reduce the average switching frequency. Modified versions of the switching techniques that use three large, one medium, and one zero voltage vector are shown in [54] that include the use of both discontinuous and continuous switching algorithms, but this 9 time-segment discontinuous technique proves to have the lowest average switching frequency. A detailed THD analysis of the resultant phase currents from these modified techniques is also provided in [54] and compared to modified versions of the four large and one zero vector technique. Similar to the C12-4L1Z technique

previously discussed, it can be seen that there are some instances where switches turn on or off when transitioning between sectors which must be considered when calculating the average switching frequency. Taking this into consideration and using (2.10) from above, for a defined carrier switching frequency, $f_{sw_{carr}}$, of 20 kHz, the average switching frequency is calculated to be 19.16 kHz.

With the three large, one medium, and one zero voltage vector technique being the first proposed technique that does not use only the large voltage vectors in the $\alpha\beta$ subspace, many recent papers have started to explore utilizing the wide variety of voltage vectors of different magnitudes that can be produced with a six-phase VSI. In [56], a switching method is adopted where three large vectors, two medium vectors, and one zero voltage vector are used. Based on the matrix to calculate the dwell times that was recently seen in (2.9), a problem arises when only calculating five dwell times for six voltage vectors. For this reason, the two medium voltage vectors are not independent of one another and the same dwell time is used as the duration for each of the medium vectors. The switching sequence of this technique uses a very similar concept to the D24-3L1M1Z technique previously discussed where the $\alpha\beta$ plane is divided into 24 sectors, however, an additional medium voltage vector is used in the middle of the switching sequence to simulate a lower voltage component, similar to how zero vectors are often used in the middle of switching algorithms for continuous methods. This technique is referred to as D24-3L2M1Z and the switching characteristics can be observed in Figure 2.13 and Table 2.4.



(a) Sector 24 (b) Sector 1

Figure 2.13: Visual Representation for the Sequence of the Voltage Vectors applied for the D24-3L2M1Z Technique Using 11 Time Segments

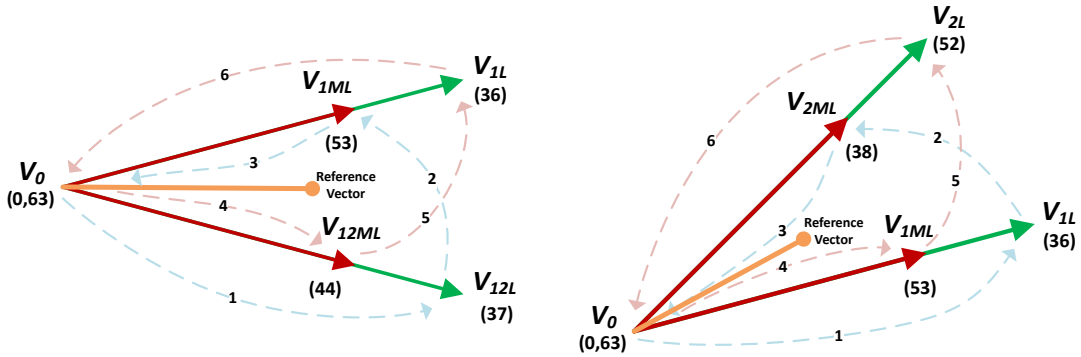
As seen in Table 2.4, with the D24-3L2M1Z technique being a discontinuous switching method, at least one switch does not turn on or off in each sample period and the requirement of $f_{samp} = f_{sw}$ is maintained allowing this technique to be implemented using a DSP. However, similar to all aforementioned techniques, there exist additional switchings every two sectors when the zero voltage vector being used is adjusted. Once again, considering these switching instances in the calculation of the average switching frequency, using (2.10) from above for a carrier switching frequency, $f_{sw_{carr}}$, of 20 kHz, the average switching frequency, $f_{sw_{avg}}$, is calculated to be 19.16 kHz.

Table 2.4: Switching Sequence for Each Sector Represented by Decimal Numbers for the D24-3L2M1Z Switching Technique Using 11 Time Segments

Sector	**Decimal Number Switching Sequence**	**Sector**	**Decimal Number Switching Sequence**
1	**07** – 05 – 37 – 36 – 52 – 60 – 52 – 36 – 37 – 05 – **07**	13	**56** – 58 – 26 – 27 – 11 – 03 – 11 – 27 – 26 – 58 – **56**
2	**07** – 39 – 37 – 36 – 52 – 48 – 52 – 36 – 37 – 39 – **07**	14	**56** – 24 – 26 – 27 – 11 – 15 – 11 – 27 – 26 – 24 – **56**
3	**00** – 32 – 36 – 52 – 54 – 55 – 54 – 52 – 36 – 32 – **00**	15	**63** – 31 – 27 – 11 – 09 – 08 – 09 – 11 – 27 – 31 – **63**
4	**00** – 04 – 36 – 52 – 54 – 62 – 54 – 52 – 36 – 04 – **00**	16	**63** – 59 – 27 – 11 – 09 – 01 – 09 – 11 – 27 – 59 – **63**
5	**56** – 60 – 52 – 54 – 22 – 06 – 22 – 54 – 52 – 60 – **56**	17	**07** – 03 – 11 – 09 – 41 – 57 – 41 – 09 – 11 – 03 – **07**
6	**56** – 48 – 52 – 54 – 22 – 23 – 22 – 54 – 52 – 48 – **56**	18	**07** – 15 – 11 – 09 – 41 – 40 – 41 – 09 – 11 – 15 – **07**
7	**63** – 55 – 54 – 22 – 18 – 16 – 18 – 22 – 54 – 55 – **63**	19	**00** – 08 – 09 – 41 – 45 – 47 – 45 – 41 – 09 – 08 – **00**
8	**63** – 62 – 54 – 22 – 18 – 02 – 18 – 22 – 54 – 62 – **63**	20	**00** – 01 – 09 – 41 – 45 – 61 – 45 – 41 – 09 – 01 – **00**
9	**07** – 06 – 22 – 18 – 26 – 58 – 26 – 18 – 22 – 06 – **07**	21	**56** – 57 – 41 – 45 – 37 – 05 – 37 – 45 – 41 – 57 – **56**
10	**07** – 23 – 22 – 18 – 26 – 24 – 26 – 18 – 22 – 23 – **07**	22	**56** – 40 – 41 – 45 – 37 – 39 – 37 – 45 – 41 – 40 – **56**
11	**00** – 16 – 18 – 26 – 27 – 31 – 27 – 26 – 18 – 16 – **00**	23	**63** – 47 – 45 – 37 – 36 – 32 – 36 – 37 – 45 – 47 – **63**
12	**00** – 02 – 18 – 26 – 27 – 59 – 27 – 26 – 18 – 02 – **00**	24	**63** – 61 – 45 – 37 – 36 – 04 – 36 – 37 – 45 – 61 – **63**

Another switching technique that has been proposed in [57] and [58] uses two large, two medium-large, and one zero voltage vector. The selection of these voltage vectors in the $\alpha\beta$ plane comes from the resultant vectors of the xy_s plane. In the xy_s plane, this technique results in pairs of medium-large and small vectors that are opposite in phase which help to maintain the volt-seconds of the xy_s subspace to be as close to zero as possible while maintaining the $\alpha\beta$ reference. This technique can

be implemented as a continuous 12 sector method which was seen in Figure 2.10a. Therefore, this switching sequence is referred to as C12-2L2ML1Z and its switching characteristics can be seen in Figure 2.14 and Table 2.5.



(a) Sector 12 (b) Sector 1

Figure 2.14: Visual Representation for the Sequence of the Voltage Vectors applied for the C12-2L2ML1Z Technique Using 7 Time Segments

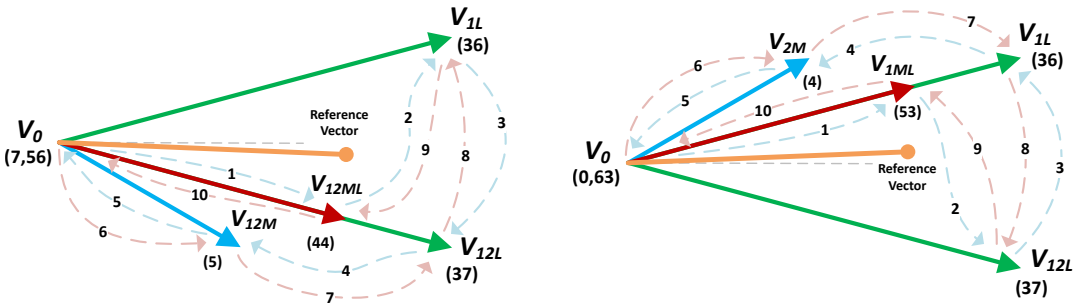
Table 2.5: Switching Sequence for Each Sector Represented by Decimal Numbers for the C12-2L2ML1Z Switching Technique Using 7 Time Segments

Sector	**Decimal Number Switching Sequence**	**Sector**	**Decimal Number Switching Sequence**
1	**00** – 36 – 38 – **63** – 53 – 52 – **00**	7	**00** – 10 – 11 – **63** – 27 – 25 – **00**
2	**00** – 38 – 54 – **63** – 52 – 20 – **00**	8	**00** – 11 – 43 – **63** – 25 – 09 – **00**
3	**00** – 20 – 22 – **63** – 54 – 50 – **00**	9	**00** – 09 – 13 – **63** – 43 – 41 – **00**
4	**00** – 22 – 30 – **63** – 50 – 18 – **00**	10	**00** – 13 – 45 – **63** – 41 – 33 – **00**
5	**00** – 18 – 19 – **63** – 30 – 26 – **00**	11	**00** – 33 – 37 – **63** – 45 – 44 – **00**
6	**00** – 19 – 27 – **63** – 26 – 10 – **00**	12	**00** – 37 – 53 – **63** – 44 – 36 – **00**

The C12-2L2ML1Z switching technique is proposed using both continuous and discontinuous algorithms in [57] and [58], however, the continuous method is analyzed in this thesis due to the poor performance of the discontinuous methods when evaluating the phase current THD. For this reason, the continuous switching method

discussed in this thesis uses only 7 time segments to help reduce the average switching frequency. Additionally, for this 12 sector switching method, the algorithm has removed the switching instances between each sector which helps to further reduce the average switching frequency. For a defined carrier switching frequency, $f_{sw_{carr}}$, of 20 kHz, the average switching frequency is calculated from (2.10) to be 20 kHz, which is similar to the DZSI SPWM technique first discussed.

Lastly, in [60] modifications of the three large, one medium, and one zero voltage vector switching technique are proposed where different medium vectors are used as well as a proposed technique that uses two large, one medium-large, one medium, and one zero voltage vector. The main contribution of this paper is the idea of alternating the medium voltage vector that is used for both switching techniques to improve the phase current THD at different operating points of a drive system. All techniques discussed in this paper divide the $\alpha\beta$ plane into 24 sectors and are compared to SPWM. Looking more in-depth at the proposed 24 sector technique in this paper using two large, one medium-large, one medium, and one zero voltage vector, this technique is developed by analyzing the resultant voltage vectors that would be generated by SPWM and making adjustments for a VSD based controller which helps to lower the phase current THD. This continuous switching technique will be referred to as C24-2L1ML1M1Z and from the two modified versions of this discussed in [60], the technique with the lowest THD is discussed with switching characteristics shown in Figure 2.15 and Table 2.6.



(a) Sector 24 (b) Sector 1

Figure 2.15: Visual Representation for the Sequence of the Voltage Vectors applied for the C24-2L1ML1M1Z Technique Using 11 Time Segments

This continuous switching algorithm from Table 2.6 once again requires a change in the zero vectors every two sectors which will be considered in the average switching frequency calculation. For a defined carrier switching frequency of 20 kHz, with each switch turning on and off at least one time in each switching period, and including the switchings between sectors, the average switching frequency can be calculated using (2.10) as 22.5 kHz. This is a similar average switching frequency to the proposed technique from [56] which shows that certain patterns and methods result in the same average switching frequency calculation.

From the techniques proposed in the literature that have been discussed above, different methods that help to reduce the switching frequency can be realized, but also some patterns that increase the average switching frequency can be observed. For example, the use of discontinuous switching helps to reduce the average switching frequency, however, changing the zero vectors every sector or every two sectors for 12 and 24 sector methods, respectively, increases the average switching frequency. In the upcoming chapters, these factors will be considered as the VSI efficiency is observed for these existing techniques from literature and new switching techniques

are proposed. However, to allow for accurate comparisons between the discussed techniques, it is important to develop an accurate model for dual three-phase drive systems.

Table 2.6: Switching Sequence for Each Sector Represented by Decimal Numbers for the C24-2L1ML1M1Z Switching Technique Using 11 Time Segments

Sector	**Decimal Number Switching Sequence**	**Sector**	**Decimal Number Switching Sequence**
1	**63** – 53 – 37 – 36 – 04 – **00** – 04 – 36 – 37 – 53 – **63**	13	**00** – 10 – 26 – 27 – 59 – **63** – 59 – 27 – 26 – 10 – **00**
2	**63** – 53 – 52 – 36 – 32 – **00** – 32 – 36 – 52 – 53 – **63**	14	**00** – 10 – 11 – 27 – 31 – **63** – 31 – 27 – 11 – 10 – **00**
3	**07** – 38 – 36 – 52 – 48 – **56** – 48 – 52 – 36 – 38 – **07**	15	**56** – 25 – 27 – 11 – 15 – **07** – 15 – 11 – 27 – 25 – **56**
4	**07** – 38 – 54 – 52 – 60 – **56** – 60 – 52 – 54 – 38 – **07**	16	**56** – 25 – 09 – 11 – 03 – **07** – 03 – 11 – 09 – 25 – **56**
5	**00** – 20 – 52 – 54 – 62 – **63** – 62 – 54 – 52 – 20 – **00**	17	**63** – 43 – 11 – 09 – 01 – **00** – 01 – 09 – 11 – 43 – **63**
6	**00** – 20 – 22 – 54 – 55 – **63** – 55 – 54 – 22 – 20 – **00**	18	**63** – 43 – 41 – 09 – 08 – **00** – 08 – 09 – 41 – 43 – **63**
7	**56** – 50 – 54 – 22 – 23 – **07** – 23 – 22 – 54 – 50 – **56**	19	**07** – 13 – 09 – 41 – 40 – **56** – 40 – 41 – 09 – 13 – **07**
8	**56** – 50 – 18 – 22 – 06 – **07** – 06 – 22 – 18 – 50 – **56**	20	**07** – 13 – 45 – 41 – 57 – **56** – 57 – 41 – 45 – 13 – **07**
9	**63** – 30 – 22 – 18 – 02 – **00** – 02 – 18 – 22 – 30 – **63**	21	**00** – 33 – 41 – 45 – 61 – **63** – 61 – 45 – 41 – 33 – **00**
10	**63** – 30 – 26 – 18 – 16 – **00** – 16 – 18 – 26 – 30 – **63**	22	**00** – 33 – 37 – 45 – 47 – **63** – 47 – 45 – 37 – 33 – **00**
11	**07** – 19 – 18 – 26 – 24 – **56** – 24 – 26 – 28 – 19 – **07**	23	**56** – 44 – 45 – 37 – 39 – **07** – 39 – 37 – 45 – 44 – **56**
12	**07** – 19 – 27 – 26 – 58 – **56** – 58 – 26 – 27 – 19 – **07**	24	**56** – 44 – 36 – 37 – 05 – **07** – 05 – 37 – 36 – 44 – **56**

Chapter 3

Proposed Dynamic Dual Three-Phase Drive System Modelling

3.1 Introduction

As research is conducted into developing higher performance, more reliable, and more efficient electric motors for traction applications, the design of an accurate simulation model is essential before carrying out any sort of experimental verification. For this thesis, due to the limited resources for operating a high-power multiphase setup, an accurate six-phase drive Matlab/Simulink Model has been proposed and verified at a very low operating point. This proposed drive model is a FOC based model that is divided into three separate subsystems – the motor, the controller, and the inverter. This chapter will investigate each subsystem of the drive model with a detailed explanation of every aspect of the system as well as the considerations that have been

made in the simulation model to match the experimental setup as closely as possible. In a similar way to the control techniques previously discussed, the motor subsystem can be modelled assuming either the VSD or Double dq coordinate transformation. Once again, due to the significant mutual coupling effect of the Double dq coordinate transformation, the motor subsystem utilizes the VSD transformation where the $\alpha\beta$ subspace contributes to torque production with other, loss contributing harmonics being mapped in the xy subspace. This proposed simulation model uses lookup tables that are generated in FEA software for each of the four synchronous reference frame dimensions of the dual three-phase drive system – d, q, x_r, and y_r. Similar to the physical motor, the six-phase voltages are the inputs to this motor model with the machine's phase currents being the output. Within the physical setup of the motor, phase voltages are generated by the inverter and sent to the motor and current sensors detect the phase currents and relay this information back to the controller.

With the proposed model structure being an IPMSM, FOC based model, the controller subsystem is simplified where an offline maximum torque per ampere (MTPA) profile is used to select reference i_d and i_q current inputs. It should be noted that to obtain the MTPA profile of the motor, the flux linkage and torque data should be obtained from FEA results at a given speed, usually the motor base speed. Then, by sweeping the phase current magnitudes and phase angles, the combination that produces the highest torque can be calculated at every operating point. Post processing can then invert the results to determine the phase current magnitude and phase angle that produces the maximum torque. Note that each combination of the current magnitude and angle corresponds to a pair of d and q axis current values. Determining the maximum torque for each combination of these d and q axis values produces

an optimized trajectory from zero to maximum torque for the specified quadrants of operation. Additionally, with the MTPA profile being generated offline at the motors base speed, this same trajectory can be used for the entire constant torque operating region where the d and q current inputs are selected to increase and decrease the load torque of the system to observe the operating characteristics of the machine. Therefore, the controller subsystem is required to take in the reference current values for each subspace, and additionally, the phase current and position feedback from the motor. Within the controller, different control and switching techniques are utilized to then generate gate signals for each of the switches of the six-phase VSI which is isolated in its own subsystem. Inside the inverter subsystem, the generated gate signals are used with a fixed DC link voltage where switching devices are utilized to generate phase voltages that are then fed to the motor subsystem. With a focus of this thesis being on the inverter efficiency, accurate power loss modelling of each IGBT module is completed in the inverter subsystem to provide accurate VSI efficiency calculations for the different control/switching techniques being used.

Figure 3.1 presents the closed-loop model where each of the subsystems seen will be discussed in more detail throughout this chapter. The contribution from this modelling method comes from the motor subsystem where lookup tables are generated in FEA that calculate the synchronous reference frame currents as functions of synchronous frame flux linkages and electrical position. Additionally, this proposed model provides the overall torque output of the system as a function of the synchronous frame currents and electrical position. Similar methods have been used for modelling three-phase IPMSMs [61], however, the motor model becomes much more complicated with the inclusion of the xy subspace. The details of this proposed

modelling strategy specifically for dual three-phase IPMSMs will be discussed in the following section.

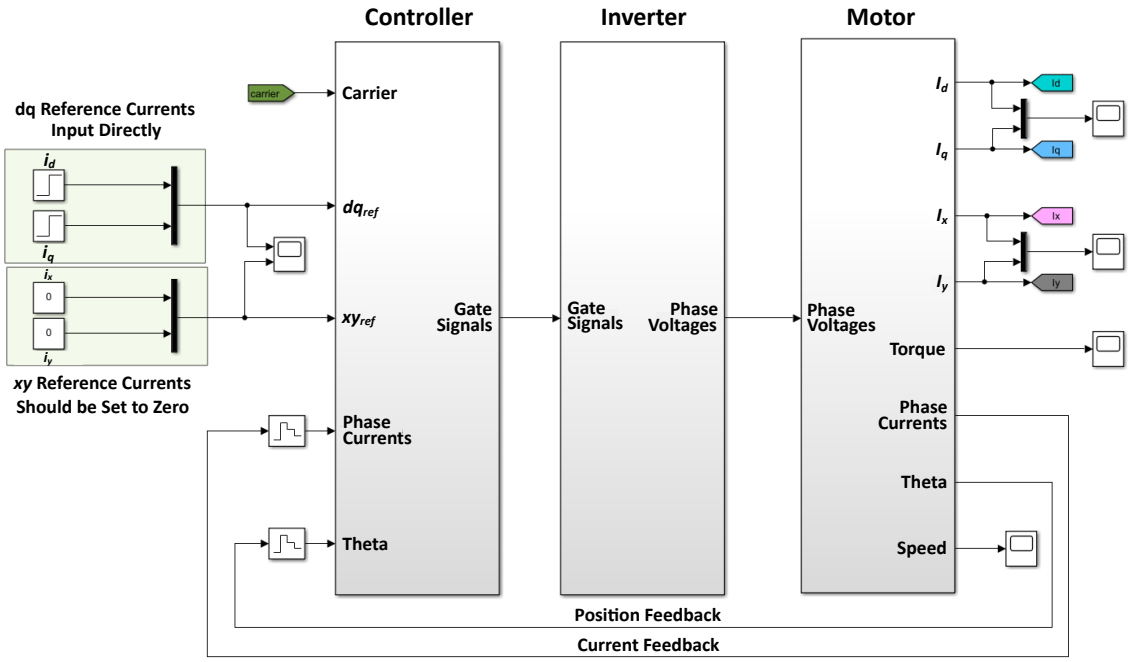


Figure 3.1: Overview of Dual Three-Phase Drive System in Simulink Environment

3.2 Motor Subsystem Modelling

Similar to the aforementioned control and switching techniques, multiphase machine modelling can be implemented using a Double dq or VSD transformation-based model. However, due to the significant mutual coupling between the two isolated phase sets that is associated with the Double dq transformation previously discussed, more complex voltage decoupling calculations are required. Therefore, the VSD based model is adopted to produce a mathematical representation of the different subspaces within the dual three-phase system. An added benefit of the VSD model is that it can be

applied to any multiphase motor and the motor does not have to have a multiple of three-phases as is required for the Double dq based model [62]. As mutual coupling still exists among phase windings, similar to three-phase machines, the VSD mathematical representation is given in the synchronous reference frame with spatial harmonics and saturation effects often ignored. The synchronous frame voltage equations are defined in [19] as:

$$v_d = R_s i_d + L_d \frac{di_d}{dt} - \omega_e L_q i_q \tag{3.1a}$$

$$v_q = R_s i_q + L_q \frac{di_q}{dt} - \omega_e (L_d i_d + \psi_{PM}) \tag{3.1b}$$

$$v_x = R_s i_{x_r} + L_z \frac{di_{x_r}}{dt} \tag{3.1c}$$

$$v_y = R_s i_{y_r} + L_z \frac{di_{y_r}}{dt} \tag{3.1d}$$

where v_k ($k = d,q,x_r,y_r$) represents the stator voltages, i_k ($k = d,q,x_r,y_r$) represents the stator currents, L_d and L_q represent the d and q axis stator inductances respectively, L_z represents stator leakage inductance, R_s is the stator resistance, ω_e is the electrical speed, and ψ_{PM} is the permanent magnet flux linkage. The stator flux linkages can then be defined in terms of the inductance parameters referenced in the above voltage equations:

$$\psi_d = L_d i_d + \psi_{PM} \tag{3.2a}$$

$$\psi_q = L_q i_q \tag{3.2b}$$

$$\psi_x = L_z i_{x_r} \tag{3.2c}$$

$$\psi_y = L_z i_{y_r} \tag{3.2d}$$

where ψ_k (k = d,q,x_r,y_r) represent stator flux linkages. All parameters from above can then be utilized to calculate the machine torque:

$$T_e = n_{pp}(\psi_{PM} i_q + (L_d - L_q) i_d i_q) \tag{3.3}$$

where n_{pp} is the number of pole pairs of the motor. In recent literature, many papers consider multiphase machine modelling utilizing this system of equations to develop a linear model with fixed inductance values ignoring the dynamic behaviour of the IPMSM. More recent modelling strategies have made attempts to include the dynamic behaviour of the IPMSM using complex mathematical representation such as in [63] and [64]. In addition, [65] proposes a simplified mathematical model which implements the Double dq transformation but this model does not consider any of the nonlinearities of the motor. A similar modelling strategy is then implemented for nine-phase machines in [66] which allowed for a generalized modelling technique for multiples of three phase machines to be discussed in [67] which is based on the relationship between phase voltage and current. Moreover, the torque of this modelling technique is calculated mathematically using an inductance matrix, however, some saturation effects have been ignored. Additionally, in [68], dual three-phase modelling utilizing the VSD based mathematical representation is seen but only assuming that the back-electromotive force is sinusoidal and also neglecting the high order nonlinear effects of the machine. Furthermore, in [69], the torque model is further improved through mathematical representation which includes the harmonics in the PM flux linkage, inductance, and currents using the Double dq transformation.

The multiphase machine model proposed in this thesis has been developed based on many recent advances in modelling strategies for three-phase IPMSMs. In [70, 71]

and [72], offline FEA is completed to generate LUTs for the nonlinear characteristics of a motor such as flux linkage, torque, or voltage. In [61], the concept of using these LUTs to model the dynamic behaviour of a three-phase IPMSM includes the high-frequency current ripple that results from the switching instances of the inverter which further increases the accuracy of the machine model. It is important to note that these three-phase modelling strategies only require FEA to calculate the nonlinear characteristics of the machine one time offline. The calculated machine characteristics that include the effects of spatial harmonics, cross-coupling, and magnetic saturation are then stored in LUTs for one full electrical cycle which can be utilized in Simulink with the conventional three-phase mathematical model that is represented in the synchronous reference frame as seen in [61]. This method of machine modelling removes the time-consuming FEA calculations and therefore, simulations in the Matlab/Simulink environment can run much faster while still providing the accuracy of FEA through the use of LUTs. Carrying these methods to multiphase machine modelling and adopting the VSD transformation, the inclusion of the xy subspace significantly increases the complexity of this modelling strategy. However, similar to the modelling of the three-phase counterpart, the simulation time is significantly improved through the use of LUTs for the d, q, and now x_r, and y_r components.

With the VSD transformation being utilized for dual three-phase machine modelling, there exist two independent subspaces to be considered – dq and xy_r. Since these subspaces are orthogonal and therefore independent of one another, this proposed machine model will consider each subspace individually. The independent subspaces can be observed in (3.1) where mutual coupling effects between the d and q axis as well as between the x and y axis can be observed, but there is no mutual

coupling between the dq and xy subspaces which is important to note for the proposed model. This system of equations will be used to model the dual three-phase machine, however as discussed in [61], to include the effects of mutual coupling in this system of equations, the d and q self-inductances and cross-coupling inductances need to be considered. Additionally, for the dual three-phase machine, the leakage self-inductance also needs to be considered for the xy subspace which increases the complexity of the calculations since these inductances are all functions of the stator currents and electrical position. Therefore to avoid these complex calculations, the flux linkage characteristics of the motor can be employed, but as pointed out in [61], derivative-based flux linkage equations could result in instability and error accumulation, so it is best to adopt integral based flux linkage equations as follows:

$$\psi_d = \int (v_d - R_s i_d + \omega_e \psi_q) dt \tag{3.4a}$$

$$\psi_q = \int (v_q - R_s i_q + \omega_e \psi_d) dt \tag{3.4b}$$

$$\psi_x = \int (v_x - R_s i_x) dt \tag{3.4c}$$

$$\psi_y = \int (v_y - R_s i_y) dt \tag{3.4d}$$

Due to the dependency of these flux linkage components on many of the machine parameters including synchronous reference frame currents, rotor position, and the physical structure of the machine, the most accurate results can be obtained using FEA. The use of FEA allows for all electrical characteristics of the machine to be calculated based on a given phase excitation current for a desired rotor position span. As this model requires flux linkage and torque data to be calculated in FEA, a range of

synchronous reference frame current values must be determined based on the desired operating quadrants to be modelled. Looking at the previously discussed three-phase FEA modelling strategies, a range of d and q axis current values are selected to be transformed to sinusoidal phase currents with a single magnitude and phase angle that cover the desired operating region of the model. However, in regards to dual three-phase machines, it needs to be considered that it is not possible to transform d, q, x_r, and y_r currents to generate perfectly sinusoidal phase currents for excitation in FEA. Therefore, the dq and xy_r subspaces will be analyzed separately using different simulations in FEA to generate LUTs for the respective flux linkages, which can be assumed due to the orthogonal definition of these subspaces from (2.3).

3.2.1 Modelling the *dq* Subspace

First considering the dq subspace and utilizing similar principles to the modelling technique developed in [61], a per-unit range can be specified for the d and q axis currents dependent on the operating quadrants being modelled while maintaining the xy_r currents to be zero. For this thesis, it will be assumed that $i_{d,pu}$ ranges from -1 to 0 at an interval of 0.02 and $i_{q,pu}$ ranges from -1 to 1 at an interval of 0.02 relative to the rated peak current of the machine which leads to a total of 51 current points for i_d and 101 current points for i_q. With every possible combination of these points being analyzed in FEA, the machine's dynamic behaviour will be calculated for 5151 (51×101) cases. It is required for each of these cases that the d and q axis currents are transformed into a phase value with a current magnitude and phase angle using:

$$I_{phase(k)} = i_d \cos(2\pi f_e t + \phi(k)) - i_q \sin(2\pi f_e t + \phi(k)) \tag{3.5}$$

where k represents the winding ($k = A_1$,B_1,C_1,A_2,B_2,C_2), f_e represents the machines electrical frequency in Hz, and ϕ is the phase shift for each winding relative to the A_1 winding. Note that the phase shift of each winding being relative to the A_1 winding is determined by the initial position in FEA being adjusted so that the d axis is in line with phase A_1. Using (3.5) for each case, a single d and q axis current value can produce six perfectly sinusoidal current waveforms that represent the entire operating range of d and q axis currents to be used for excitation of the machine in FEA. It is important to note that while generating LUTs for the dq subspace, the xy subspace is being ignored. Figure 3.2 shows an overview of the process for generating flux linkage and torque LUTs and the required inversion to produce current LUTs for the dq subspace.

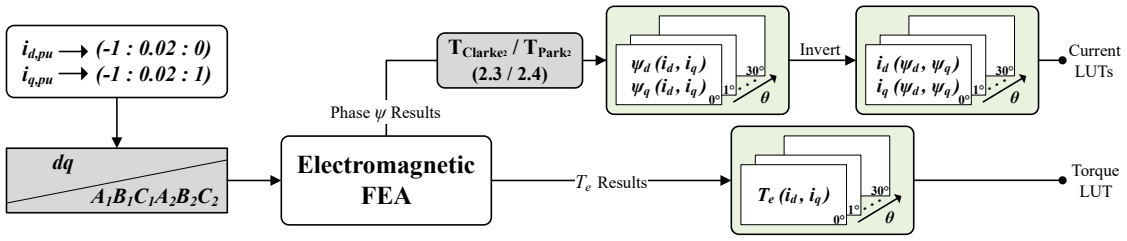


Figure 3.2: Block Diagram of Process to Generate LUTs for the d and q Axis Currents and Torque Production from the dq Subspace

During this process, it will also be assumed that in FEA each step to be calculated will correspond to 1° electrical. As a result of a dual three-phase machine windings being evenly distributed every 30°, which is verified by the spatial harmonic at $12n \pm 1$ (n = 1,2,3,...), the FEA calculations are only required for 30° electrical. This does require post-processing to reconstruct the calculated FEA data for a full electrical cycle, but by reducing the required electrical degrees to be calculated in FEA by a factor of 12, the time consuming FEA calculations can be completed much faster.

Therefore, for each of the 5151 cases calculated in FEA, flux linkage and torque results will be obtained for 30° electrical and stored as a 31 element vector. This means to run all cases for the desired rotor position span, the total number of FEA steps required is 189681 ($51 \times 101 \times 31$). Although this process is time-consuming, it only needs to be completed once to generate the desired LUTs. Additionally, the amount of FEA steps required can be lowered to reduce the computation time by increasing the current interval of i_d and i_q. Post-processing then requires the FEA data to be reconstructed for one full electrical cycle transforming this 31 element vector to a 361 element vector assuming that each step is equal to one electrical degree. Furthermore, since phase flux linkage data is calculated in FEA, (2.3) and (2.4) can be used to obtain the d and q axis flux linkage results that correspond to d and q axis input currents for the entire operating range of the machine. Once again, it is important to note that the xy components are being ignored during this simulation. This means that after executing all cases in FEA, d and q axis flux linkages LUTs are generated that are dependent on the d axis current, q axis current, and the electrical position. A similar LUT for the machine torque can also be provided from the FEA results that is also dependent on the d axis current, q axis current, and electrical position.

Now shifting the focus to the machine model in the Simulink environment, which employs the integral-based flux linkage equations in (3.4), the output of this model should be the machine phase currents. Therefore, an inversion process is required to develop lookup tables for i_d and i_q that are dependent on the d axis flux linkage, q axis flux linkage, and electrical position where this process is handled in post-processing of the calculated FEA data. The d and q axis flux linkages can then be calculated using

(3.4a) and (3.4b) respectively and fed into these LUTs with the electrical position to calculate synchronous reference frame currents. In [61] it was proven that a unique d and q axis current pair can be found based on the generated synchronous frame flux linkage LUTs. With this being the case, many methods have been proposed in the literature that utilize different Matlab commands such as using the *interpn* function or the *gridfit* function to invert lookup tables as seen in [61] and [73] respectively. Both of these functions provide similar synchronous reference frame current LUTs as they both consider the flux linkage results as 2D LUTs for different rotor positions that can be more easily inverted. As the modelling of the machine torque is another important aspect of the Simulink machine model, a torque LUT that is dependent on the d axis current, q axis current, and electrical position can also be created but no inversion process is required for this LUT.

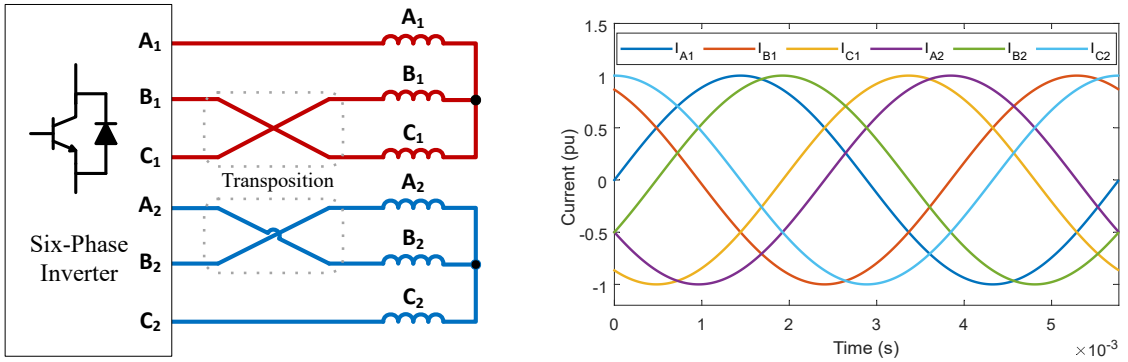
3.2.2 Modelling the *xy* Subspace

The increased complexity of the VSD-based dual three-phase IPMSM model comes from the concept of the additional xy subspace that is not present in the three-phase counterparts. As a summary, the presence of this subspace is seen in dual three-phase and not three-phase machines due to the spatial harmonics produced by the machine. In a three-phase machine, spatial harmonics and therefore the torque producing subspace is comprised of harmonics of the order $6n \pm 1$ ($n = 1,2,3,\dots$) with the even-order harmonics being eliminated, and the third-order harmonics nullifying one another. This covers all harmonics of the system and mathematically maps the torque producing harmonics to the $\alpha\beta$ subspace through the use of the three-phase

Clarke transformation. Alternatively, for a dual three-phase machine, spatial harmonics and the torque producing subspace are made up of harmonics of the order $12n \pm 1$ ($n = 1,2,3,\ldots$), where even order harmonics are once again eliminated, and third-order harmonics nullify one another similar to three-phase machines. However, this leaves harmonics of the order $6n \pm 1$ ($n = 1,3,5\ldots$) which are mathematically mapped to the xy subspace through (2.3). Therefore, with the xy subspace contributing to additional losses during healthy operating conditions, this subspace needs to be modelled accurately to observe the dynamic behaviour and efficiency of a drive system.

Similar to the aforementioned method used for modelling the dq subspace, when modelling the xy_r subspace, all dq components will be ignored due to these subspaces being independent of one another. In a similar fashion to selecting a range of d and q axis currents, a range of x_r and y_r axis currents need to be selected; however, since the xy_r currents will be represented in the synchronous frame as AC components, the selected range of these values cannot be limited to specific quadrants. Nevertheless, since x_r and y_r are dependent on the machine's leakage inductance, it can be assumed that these components will only be a fraction of the magnitude of the dq components. For this reason $i_{x_r,pu}$ and $i_{y_r,pu}$ will both range from -0.2 to 0.2 at an interval of 0.02 relative to the rated peak current of the machine. However, if the same method for generating a single current magnitude and phase angle is used as was for the dq subspace, the generated phase currents will only represent the dq subspace and not the xy_r subspace. With the focus being to generate LUTs for the xy_r subspace, a method is proposed in [74] which involves transposing certain phases of the machine so that one phase set acts as a motor and the other phase set acts as a generator which

can be seen in Figure 3.3a. This allows for the generation of sinusoidal excitation currents to only be represented fully by xy_r currents in the synchronous reference frame with the dq components being zero. The generated phase currents assuming the phase transposition can be seen in Figure 3.3b.



(a) (b)

Figure 3.3: Transposed Phase Currents in Regards to (a) Machine Winding Configuration and (b) Resultant Phase Currents

For the desired range of x_r and y_r current values, a separate FEA simulation can be executed with the transposed phases seen in Figure 3.3b. With the given current range, FEA will simulate 441 (21×21) cases, which, similar to the FEA for the dq subspace, will only be calculated for 30° electrical where each step in FEA is equivalent to 1° electrical. This will result in the FEA simulation having a total number of steps of 13671 ($21 \times 21 \times 31$) which is once again a time-consuming simulation that only needs to be completed one time. The significant modification that needs to be considered for the xy_r subspace compared to the dq subspace is that if the excitation current has a frequency equal to the fundamental frequency, the calculated phase flux linkages are not symmetrical. This is due to the xy subspace being represented by the fifth and seventh harmonics which rotate at $+5\omega_e$ and $-7\omega_e$ where it is only

at these frequencies that symmetrical phase flux linkage waveforms are produced. Therefore, this model will assume that the xy currents are excited at five times the fundamental frequency, which in FEA produces symmetrical phase flux linkages at the fundamental frequency. This allows for only 30° to be calculated in FEA which significantly reduces the computation time. This is compared to if the currents were excited at the fundamental frequency which does not produce symmetrical phase flux linkages, which requires FEA calculations for 360° to be completed since the waveforms can not be reconstructed due to the lack of symmetry.

To obtain the excitation currents at five times the fundamental frequency, each combination of current values must be converted to a phase value with a current magnitude and phase angle. It is important to note that the transposed phases, as well as excitation at five times the fundamental frequency, must be considered:

$$I_{phase(k)} = i_x \cos(5(2\pi f_e t + \phi(k))) - i_y \sin(5(2\pi f_e t + \phi(k))) \tag{3.6}$$

where k represents the winding ($k = A_1$,C_1,B_1,B_2,A_2,C_2), f_e represents the machines electrical frequency in Hz, and ϕ is the phase shift for each winding relative to the A_1 winding. Using (3.6) will generate six perfectly sinusoidal phase currents with transposed phase's at five times the fundamental frequency that are only represented by the xy_r subspace in the synchronous reference frame. Using these excitation currents in FEA for the given current range, phase flux linkage and torque LUTs can be generated using the same method that was used for the dq subspace. For the selected current range and interval, as well as each FEA step being equivalent to 1° electrical, torque data will be stored in a 441×31 matrix ($steps \times cases$), and phase flux linkage data will be stored in a 2646×31 matrix ($steps \times cases * 6$). Post-processing then

requires for these waveforms to be reconstructed to cover one full electrical cycle similar to the process used for modelling the dq subspace. However, with the assumption of the xy subspace rotating at five times the fundamental frequency, a modified Park transformation must be considered for the conversion and inversion process:

$$\begin{bmatrix} f_d \\ f_q \\ f_{x_r} \\ f_{y_r} \end{bmatrix} = T_{Park_{xy}} \begin{bmatrix} f_\alpha \\ f_\beta \\ f_{x_s} \\ f_{y_s} \end{bmatrix} \quad T_{Park_{xy}} = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 0 & 0 \\ -\sin(\theta) & \cos(\theta) & 0 & 0 \\ 0 & 0 & \cos(5\theta) & \sin(5\theta) \\ 0 & 0 & -\sin(5\theta) & \cos(5\theta) \end{bmatrix} \tag{3.7}$$

Note that this Park transformation for the xy_r subspace only needs to be considered within the motor subsystem and that the dq components of this transformation can be ignored. After using (3.7), synchronous reference frame flux linkage LUTs that are dependent on x_r and y_r axis currents, as well as electrical position, can be developed. These LUTs can then be inverted to produce x_r and y_r axis current LUTs that are dependent on x_r flux linkage, y_r flux linkage, and electrical position using the same process used for the inversion of the dq subspace LUTs. Although the xy subspace does not theoretically produce any electromagnetic torque, small oscillations due to the spatial harmonics are still generated in FEA from the xy subspace. This torque generated by the xy subspace is included in the drive model but does not contribute to the overall torque of the system because the average value of the xy torque is consistently zero. Figure 3.4 shows the process for generating flux linkage and torque LUTs and inverting them to produce current LUTs for the xy_r subspace. With current and torque LUTs generated for all subspaces considered in dual three-phase drive systems, these LUTs along with the flux linkage equations from (3.4) can be

considered in the Simulink environment.

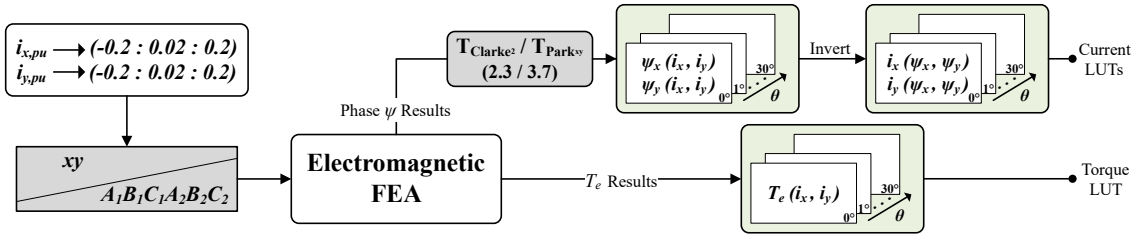


Figure 3.4: Block Diagram of Process to Generate LUTs for the x_r and y_r Axis Currents and Torque Production from the xy_r Subspace

However, to make the Simulink environment resemble a physical setup as closely as possible, it is necessary to discretize this subsystem. Additionally, since the xy subspace was rotated to obtain the LUTs which was not previously assumed, there is an additional component that needs to be added to both the x_r and y_r axis equations. Recall that the xy subspace was excited at five times the fundamental frequency which must be considered in the updated voltage equations. As the Simulink model is flux linkage based, with the above considerations, the integral based flux linkage equations from (3.4) can be modified for the proposed method of modelling the xy_r subspace. The addition of the rotating components to the x and y equations can be assumed to be in similar directions to the dq subspace since the x_s component also leads the y_s component by 90° in the stationary reference frame and the excitation remains in the same direction as it was for the dq subspace.

$$\psi_d = \int (v_d - R_s i_d + \omega_e \psi_q) dt \tag{3.8a}$$

$$\psi_q = \int (v_q - R_s i_q + \omega_e \psi_d) dt \tag{3.8b}$$

$$\psi_x = \int (v_x - R_s i_x + 5\omega_e \psi_y) dt \tag{3.8c}$$

$$\psi_y = \int (v_y - R_s i_y - 5\omega_e \psi_x) dt \tag{3.8d}$$

With LUTs developed that will calculate the currents for each subspace of a dual three-phase machine, the above equations can be seen in discrete form using the Backward Euler integration method as discussed in [61] which allows these equations to be discretely represented in the Simulink model:

$$\psi_d(n) = \psi_d + T_s\Big(v_d(n) - R_s i_d(n-1) + \omega_e(n-1)\psi_q(n-1)\Big) \tag{3.9a}$$

$$\psi_q(n) = \psi_q + T_s\Big(v_q(n) - R_s i_q(n-1) - \omega_e(n-1)\psi_d(n-1)\Big) \tag{3.9b}$$

$$\psi_{x_r}(n) = \psi_{x_r} + T_s\Big(v_{x_r}(n) - R_s i_{x_r}(n-1) + 5\omega_e(n-1)\psi_{y_r}(n-1)\Big) \tag{3.9c}$$

$$\psi_{y_r}(n) = \psi_{y_r} + T_s\Big(v_{y_r}(n) - R_s i_{y_r}(n-1) - 5\omega_e(n-1)\psi_{x_r}(n-1)\Big) \tag{3.9d}$$

where n is the time step, and T_s represents the sampling time of the system. From (3.9), the n^{th} flux linkage values are used as inputs to the LUTs to calculate the synchronous reference frame currents which are then fed back to this equation as the previous current values. The Simulink implementation of the above equations, as well as the current LUT operation, can be seen in Figures 3.5 and 3.6 respectively.

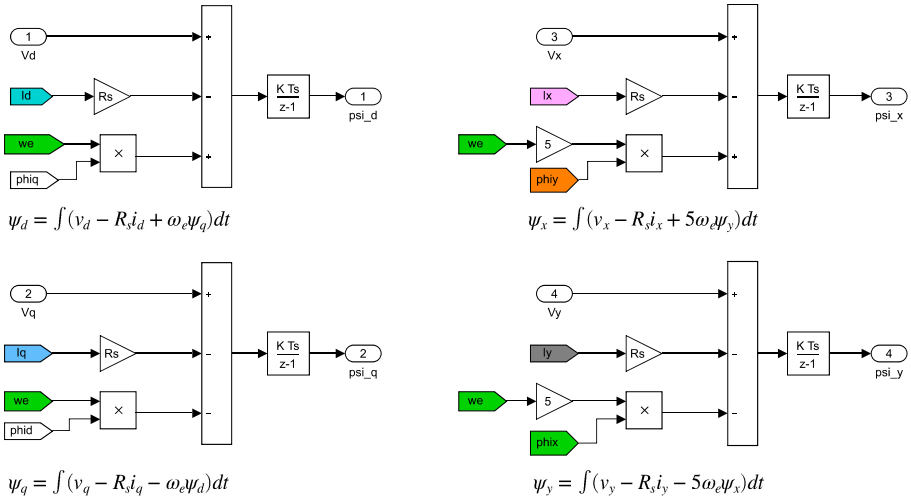
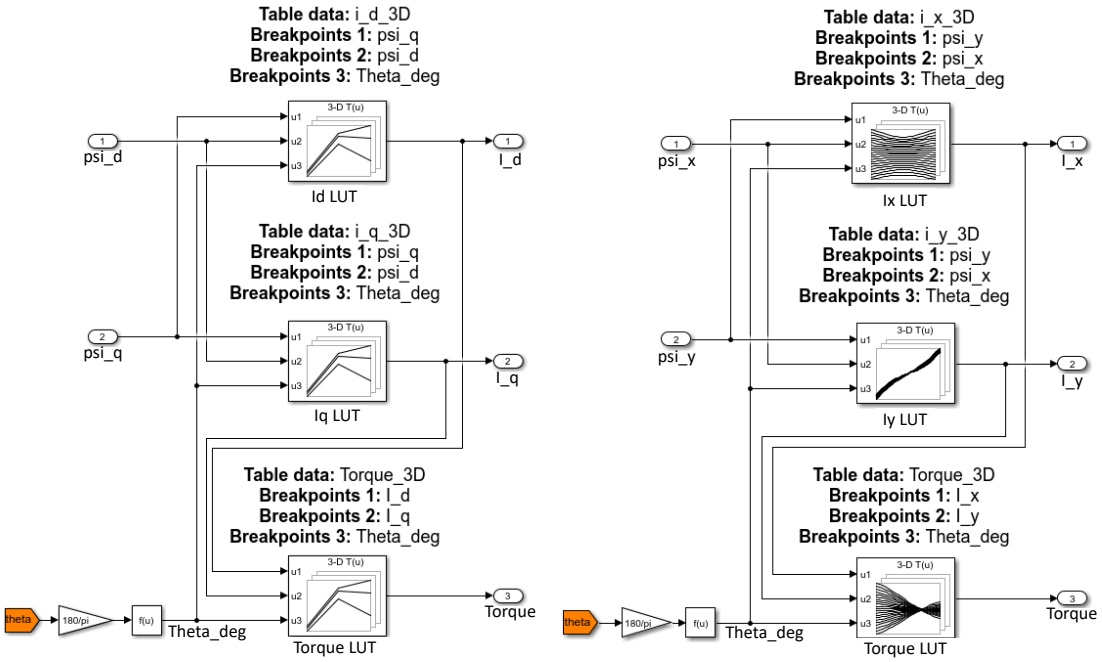


Figure 3.5: Implementation of Dual Three-Phase Voltage Equations in the Simulink Environment

Additionally, the synchronous frame voltage components come from the input phase voltages where (2.3) and (3.7) are used to obtain these values. Recall that the phase voltage waveforms are generated by the inverter subsystem which will be discussed in a later section. Lastly, with the current LUTs generating the synchronous reference frame values, the inverse of equation (2.3) and (3.7) can be implemented in Simulink to obtain the phase currents which are used as the input to the controller subsystem. This allows for the modified Park transformation in (3.7) to be contained only to the motor subsystem without the need to consider this unique matrix in other areas of the dual three-phase drive model.



(a) dq Current LUTs (b) xy_r Current LUTs

Figure 3.6: Implementation of Synchronous Reference Frame Current LUTs in the Simulink Environment

3.3 Controller Subsystem Modelling

The concept of having discrete phase current waveforms entering the controller subsystem is similar to the actual process that would take place for a physical setup where the current sensors transmit phase current feedback from the motor to the controller and these phase currents are sampled at a specified sampling frequency. This is done in simulations through the use of Simulink's *Zero Order Hold* block which holds the value of each phase current for the set duration of the sampling time. It is also important to note that a similar block is used for the position feedback from the motor. With sampled phase current and position inputs to the controller subsystem, the controller in Simulink can be accurately implemented similar to how it would physically

work when using a DSP. Within the controller subsystem of this model, the block diagram from Figure 2.6 is implemented, where different switching techniques can be utilized. As the control and switching techniques for dual three-phase motor drives have already been discussed in detail throughout Chapter 2, this section will focus on how these techniques are implemented in the Simulink environment.

As the input phase currents have already been discussed, the other important inputs to this subsystem are the synchronous frame reference currents. As previously mentioned, the reference d and q axis current values are typically determined by an MTPA profile and an outer speed loop and are then input to the inner closed-loop current controller. To simplify the Simulink model, the d and q axis reference current values are determined offline from the MTPA profile of the machine and input directly as constants to the controller subsystem. Alternatively, assuming only healthy operating points of the machine throughout this thesis, the x_r and y_r axis reference currents are set to zero due to this subspace contributing to losses at these operating conditions. Therefore, the controller will try to maintain the x and y current components at zero while the machine is rotating to minimize system losses. The entire Simulink block diagram for the controller subsystem is seen in Figure 3.7. It is important to note that if SPWM is selected as the switching technique to be implemented, an additional transformation is required to transform the stationary reference frame voltages to phase voltages.

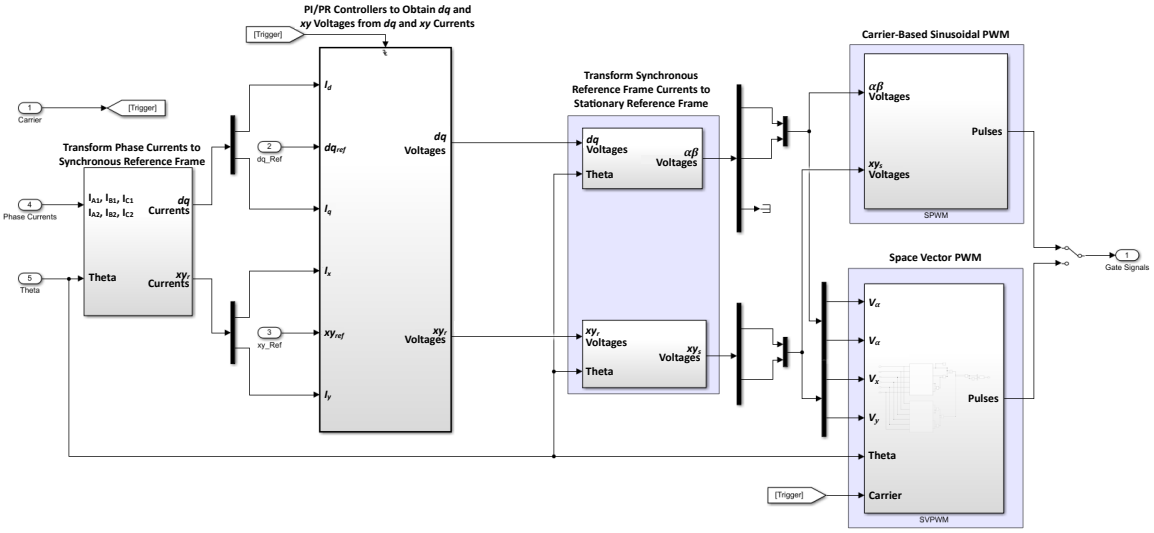


Figure 3.7: Controller Subsystem in the Simulink Environment

The dq and xy_r subspaces once again are considered individually when implementing current controllers. As the dq currents are both represented by DC components, PI controllers are implemented for each component to control the error between the reference and phase currents. These PI controllers can be tuned using similar methods to three-phase motor control techniques since the dq subspace is considered independently from the xy_r subspace. The method used to tune the PI parameters throughout this thesis requires the time constant of the d and q axis components and the phase resistance of the machine to be determined. The process of calculating these variables can be viewed as a commissioning step of the Simulink model or experimental model where, by fixing the angle of the machine so that there is no rotation, a step change to the d or q axis voltage is applied. Note that if a step change is applied to the d axis voltage, the q axis voltage should remain zero and vice versa which means that determining the PI parameters of each subspace requires two independent commissioning stages. Assuming the first stage is applying a voltage step to the d axis voltage,

the resultant increase in the d axis current is represented as a first-order exponential function which has a time constant, τ, that is calculated to be the time it takes for the d axis current to reach 0.632 $(1 - e^{-1})$ times the final value of the d axis current. Furthermore, the stator phase resistance, R_s, can also be calculated from this process using the change in voltage, Δv, and change in current, Δi, seen in (3.10a). With the d axis time constant and phase resistance calculated, the d axis inductance, L, can now be calculated using (3.10b). With these parameters determined and assuming the motor is represented by a first-order RL circuit as seen in [75], pole-zero cancellation can be used and the tuning parameters for the PI controller, K_p and K_i, can be seen in (3.10c) and (3.10d) respectively. Note that this same test needs to be repeated to obtain the gains for the q axis PI controller where the same phase resistance value should be obtained. Recall that when applying a q axis voltage step, the d axis voltage should remain zero and the machine position should be fixed.

$$R_s = \frac{\Delta v}{\Delta i} = \frac{v_f - v_i}{i_f - i_i} \tag{3.10a}$$

$$L_j = \tau_j R_s \tag{3.10b}$$

$$K_{p,j} = nR_s \tag{3.10c}$$

$$K_{i,j} = \frac{K_{p,j}}{\tau_j} \tag{3.10d}$$

It should be noted that v_f and v_i represent the final and initial voltage values respectively, i_f and i_i represent the final and initial current values respectively, j denotes the reference frame ($j = d, q$), and n is an additional tuning parameter than can be set to further optimize the PI controller parameters.

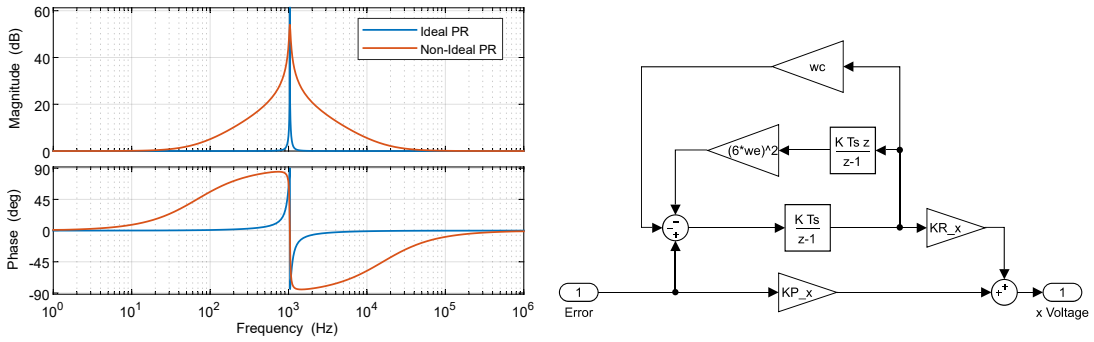
Alternatively, since the xy_r components are represented by AC components, PR controllers are implemented that are tuned at the frequency of the sinusoidal error between the reference and actual xy currents. As this model utilizes (2.6), the sinusoidal waveform of the AC component for both the x_r and y_r axis current are represented by the sixth harmonic so the PR controller must be tuned at six times the fundamental frequency. However, an ideal PR controller has limited bandwidth and can only accomplish error-free tracking for a small frequency range around the resonant frequency [62]. For this reason, throughout this thesis, a non-ideal resonant controller proposed in [62] is implemented with the continuous-time transfer function given as:

$$G_{PR}(s) = K_{P_j} + \frac{K_{R_j}\omega_c s}{s^2 + 2\omega_c s + 6\omega_e^2} \tag{3.11}$$

where j indicates the component of each subspace ($j = x_r$,y_r), K_{P_j} represents the proportional gain, K_{R_j} represents the integral gain, and ω_c is the cut-off frequency. In terms of tuning the non-ideal PR controller, the three terms to be considered are K_{P_j}, K_{R_j}, and ω_c, where K_{P_j} is simply tuned in the same way that the proportional gain is tuned for the PI controller previously discussed. Therefore, this leaves the integral gain and the cut-off frequency to be tuned where an increase in both of these parameters have a similar effect on the controller response. More specifically, an increase in the frequency bandwidth will be observed, but this results in a decrease in the controller gain. For this reason, throughout this thesis, the cut-off frequency, ω_c, is held constant and the integral gain of the PR controller, K_{P_j}, is increased until a suitable frequency bandwidth is achieved without sacrificing the overall gain. In terms of a suitable bandwidth, the larger the frequency band the better as this will allow for better transient response of the PR controller. However, as mentioned,

there is a trade-off between increasing the bandwidth and decreasing the gain, so the cut-off frequency and integral gain should be selected depending on the transient requirements of the system.

Implementing the transfer function from (3.11) in the Simulink environment with the appropriate parameters allows for the bandwidth of the controller to be increased which improves the gain of the controller over a broader range of frequencies centred around the resonant frequency. Therefore, this controller can achieve error-free tracking even with disturbances in the system as well as better control during transient operation. To show a comparison between the different PR controllers, a bode plot can be seen in Figure 3.8a to display the increased gain over a wider range of frequencies when using the non-ideal PR controller compared to the ideal counterpart. Additionally, based on the transfer function given in (3.11), the non-ideal PR controller can be implemented in Simulink in the discrete-time domain using the system seen in Figure 3.8b.



(a) PR Controller Bode Plot (b) Simulink Implementation

Figure 3.8: Proportional Resonant Controller for the xy Subspace in the Simulink Environment

Furthermore, to see the effect that the PR controller has on the xy_s subspace, simulation results can be seen in Figure 3.9 at the base speed of the simulated machine for a full load. These simulation results start with no current control of the xy_s subspace for the first half of the simulation with the PR controller then being implemented at 0.03 seconds. Note that all current and torque waveforms are displayed in per-unit values relative to the rated peak current and peak torque respectively.

From the results seen in Figure 3.9, when the PR controller is implemented at 0.03 seconds, the x_s and y_s components both converge to zero. With the xy_s currents being minimized closer to zero, it can be seen that the THD of the phase current is also reduced showing that the use of the PR controller can improve the performance of a dual three-phase drive system. These simulation results also show the lack of mutual coupling between the orthogonal dq and xy subspaces as the dq currents remain unchanged when the xy subspace current controller is engaged.

As the PI and PR controllers work to reduce the error between their respective reference and actual current values, the resultant synchronous frame voltages can then be transformed back to the stationary reference frame as seen in Figure 3.7. The stationary reference frame voltages are then used for any SVPWM techniques that wish to be implemented. As previously mentioned, if SPWM is the desired technique, then an additional transformation to obtain the phase voltages is required. The theory behind each of these switching techniques has been previously discussed in Chapter 2 where each technique utilizes the voltage waveforms generated by the current controllers to obtain gate signals for each of the switching devices of the inverter. Note that only 6 gate signals are required for the 12 switches of the two-level VSI due to the two switches in each phase leg being complimentary.

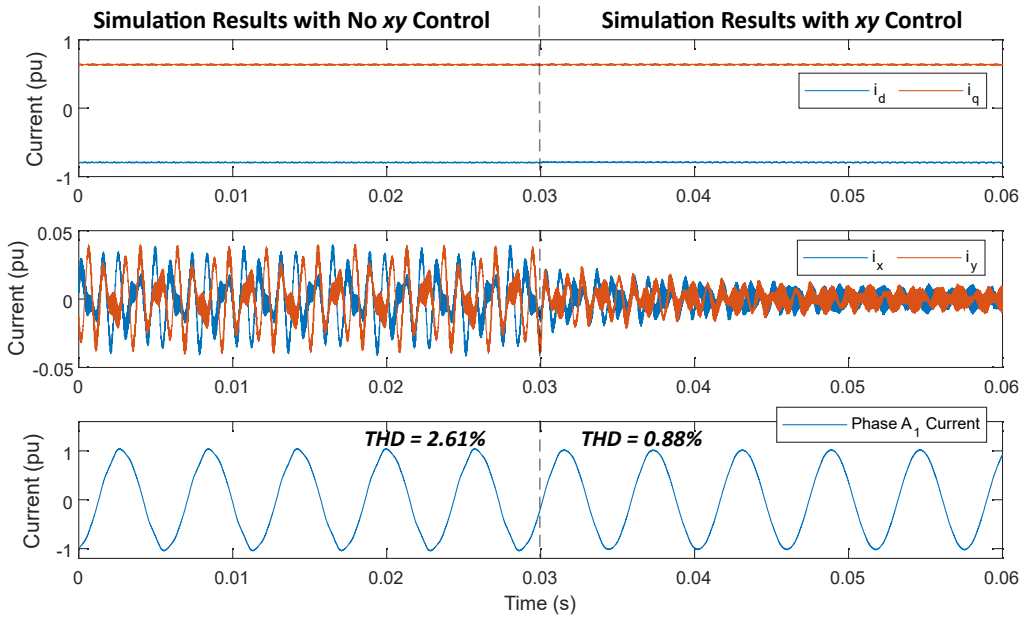


Figure 3.9: Simulation Results for a Fully Loaded Dual Three-Phase IPMSM at Base Speed Using DZSI SPWM

These gate signals generated by the controller subsystem are then used as the input to the inverter which emulates the physical system where the gate signal from the DSP is sent to the gate driver controlling the switch.

3.4 Inverter Subsystem Modelling

With a motor model that accurately displays the dynamic behaviour of a multiphase machine and a controller model that accurately resembles the DSP of a physical setup through the inclusion of realistic switching and sampling frequencies, the last major subsystem of the dual three-phase drive system to accurately model is the inverter. The inverter subsystem is responsible for converting the low voltage gate signals generated by the controller to phase voltages made up of square pulses through

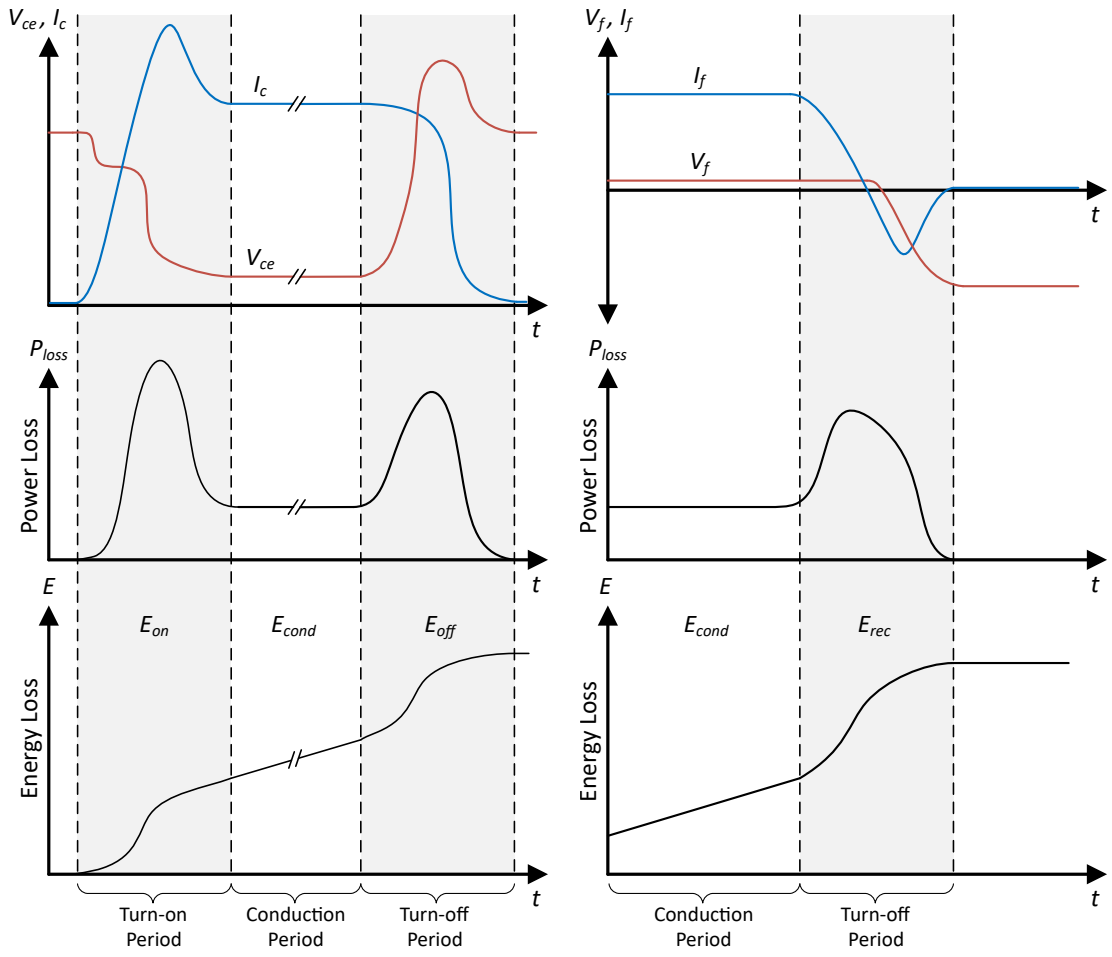
rapid, high voltage switching actions that are applied to each phase of the motor. As this thesis assumes a two-level VSI, six Infineon FF600R12IE4 IGBT modules [76] rated for 1200 $V/600$ A can be modelled within this subsystem for a DC link voltage of 350 V. As each of these modules contains two pairs of IGBTs and free-wheeling diodes, only six gate signals are required from the controller as the two switching devices of each module represent one phase leg as seen in Figure 2.1 with the gate signals for these two devices being complimentary. Note that the switch being used is overrated for this application, however, the selection of this switch is based on future work involving a motor with an operating voltage of 800 V. Additionally, this switch can be utilized for a three-phase machine as well, where for the same 100 kW power rating, the phase current would be doubled.

3.4.1 Loss Modelling

As a main focus of this thesis is on the effect that different switching techniques have on the inverter efficiency, it is important to accurately model the losses of the inverter through simulations. Accurate loss calculations require the operating principles of these switching devices to be divided into two separate parts – switching and conduction periods. As the conduction period of the components inside an IGBT module considers constant current and voltage values to calculate the power losses between switching instances, the calculation of conduction losses is much more straightforward than the calculation for switching losses. This can be observed in the conduction period for both the IGBT and diode in Figure 3.10 where the IGBT switching characteristics have been taken from [77] and the diode characteristics have been taken from [78]. In Figure 3.10, the voltage and current characteristics during the switching and

conduction periods are observed as well as the resultant power/energy losses. Note that the switching and conduction period energy losses are often what is provided in an IGBT module's datasheet. Furthermore, it can be seen from this figure that the changing voltage and current values throughout the switching periods of the IGBT and diode lead to more complicated loss calculations where a detailed analysis of the these losses is provided in [79].

First, considering the collector, emitter, and gate terminals of the IGBT, the process of current flowing from the collector to the emitter starts by applying a voltage signal to the gate terminal that must pass a certain threshold voltage before current can start to flow. The time it takes for the voltage across the gate signal to reach the threshold voltage of the switch is referred to as the turn-on delay time, $t_{d_{on}}$, and can be found in the device's datasheet. The current from the collector to the emitter, I_c, then requires a specified rise time, t_r, to reach the load current value. When I_c reaches the desired current level, the voltage from the collector to emitter terminal, V_{ce}, then starts to drop as seen in Figure 3.10. Once this voltage reduces to the on-state voltage of the device, the turn-on switching period is considered to be completed and the device is now in the conduction period. As there is an overlap of the increased current and high voltage across the device, the losses calculated during this process are referred to as the turn-on switching loss [80] where the corresponding power loss and energy loss can also be seen in Figure 3.10. As there remains a small on-state voltage with a high load current from the collector to emitter throughout the conduction period, the resultant losses during this period are known as the conduction losses of the IGBT [80].



(a) IGBT (b) Diode

Figure 3.10: Voltage and Current, Power Loss, and Energy Loss Characteristics of IGBT Module

Furthermore, the reverse process occurs when the device switches off where the voltage applied to the gate signal takes a defined turn-off delay time, $t_{d_{off}}$, before the voltage from the collector to emitter starts to rise to the blocking voltage of the device as seen in Figure 3.10. Once this voltage reaches the blocking voltage, I_c then starts to reduce back to zero which takes a defined time, t_f. Once I_c reaches zero, the turn off period is considered to be complete and once again the losses from the increase in the

voltage along with the current still across the device are referred to as the turn-off switching losses. This means that the total losses from the IGBT are a sum of the turn-on and turn-off switching losses and the conduction losses. Additionally, the losses of the free-wheeling diode must also be considered. Due to the short turn-on time of the free-wheeling diode, the turn-on losses are often neglected [80] leaving only the conduction losses and turn-off losses to be considered. With conduction losses of the diode calculated in a similar way to the IGBT, the main difference in loss calculation with the diode comes from the calculation of the turn-off switching losses being based on the reverse recovery time where the forward voltage, V_f, and current, I_f characteristics during the switching period can be seen in Figure 3.10.

From the description regarding the operation of an IGBT module, there are four sources of losses to be considered – IGBT conduction losses, IGBT switching losses, diode conduction losses, and diode switching losses [81]. As these are the main sources of losses in a traction inverter, the efficiency calculations throughout this thesis will only consider these losses. Additionally, the calculated losses will also depend on the junction temperature of each device which increases the complexity of the power loss calculations. For this reason, the PLECS by Plexim Simulink toolbox is utilized for increased accuracy and faster simulation of power electronic components [82]. Although PLECS only allows for thermal considerations to be made for ideal switches, the lookup tables provided for E_{on} and E_{off} from the device datasheet can be loaded directly into PLECS to provide accurate loss calculations for the four main sources of losses. To improve the accuracy of the efficiency calculations in this model, the turn-on and turn-off delay times are also considered to represent a dead-time between the on and off states of the two IGBT's in the same phase leg.

As previously mentioned, the IGBT module used for simulation purposes throughout this thesis is the Infineon FF600R12IE4 module rated for 1200 V/600 A. The datasheet for this module provides IGBT turn-on and turn-off switching losses, the IGBT conduction characteristics, the diode turn-off switching losses, and the diode forward characteristics all as functions of temperature [76]. All of this data from the datasheet can be converted to the PLECS library and implemented with ideal switching components in PLECS with the LUTs for the four main sources of losses seen in Figure 3.11.

As the overall goal from the inverter subsystem is to provide the total inverter efficiency, it is important to maintain a constant thermal environment for all simulations so that an accurate comparison can be made. For this reason, a heat sink is used that is held at a constant temperature of 25°C.

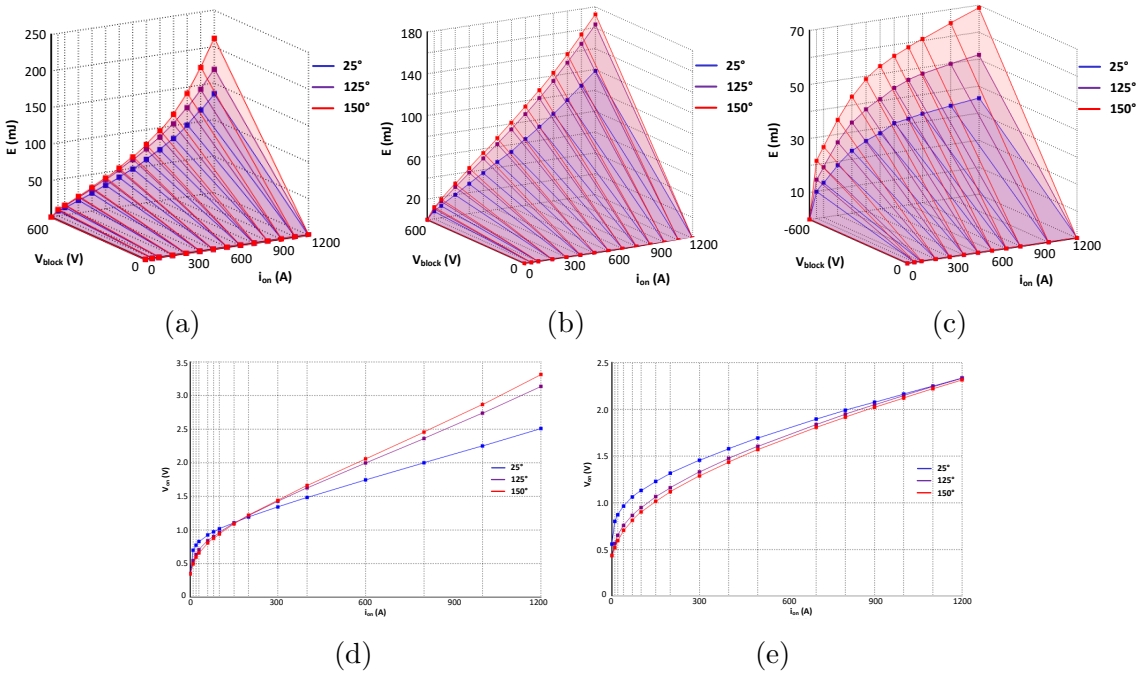


Figure 3.11: Lookup Tables Implemented in PLECS for IGBT Module Power Loss Calculations

With the temperature of the heat sink being fixed and the initial temperature of each module also being $25°C$, efficiency calculations are taken when the junction temperature of the IGBT's and diodes have increased to a steady-state value. Once the junction temperature of all the components within the inverter is steady, the efficiency of the inverter can be calculated by summing the switching and conduction losses of each component to obtain the overall power loss of the inverter, P_{loss}, and then using the equation:

$$\eta = 1 - \frac{P_{loss}}{P_{in}} \tag{3.12}$$

where η is the inverter efficiency, and P_{in} is the input power of the system. The overall PLECS system can be seen in Figure 3.12 where the inputs to the PLECS system include the gate signals from the controller subsystem as well as the phase currents.

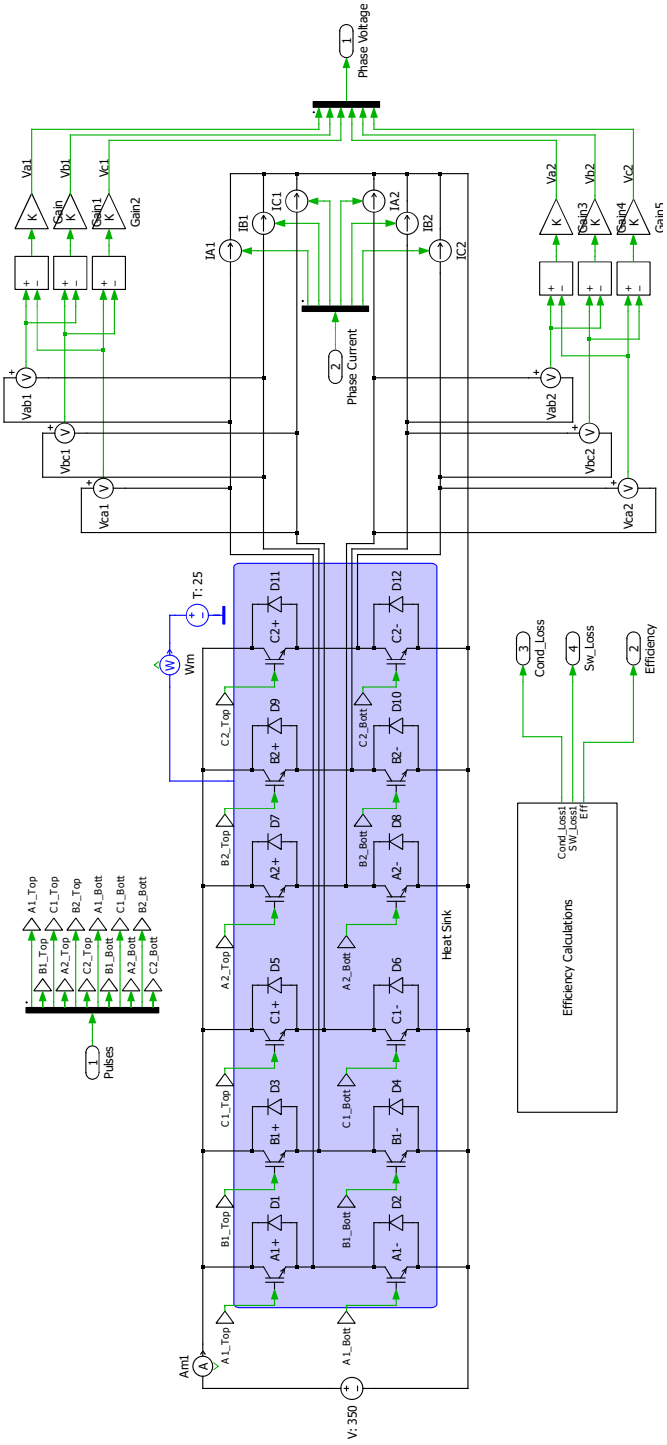


Figure 3.12: Six-Phase VSI Inverter Model Developed in PLECS Environment

Note that the phase currents are required in PLECS to simulate the attached load using current source blocks since no physical components are present in the simulation to act as a load. By including the current source blocks as the load, the correct phase voltage for each phase of the motor can be generated and fed to the motor subsystem.

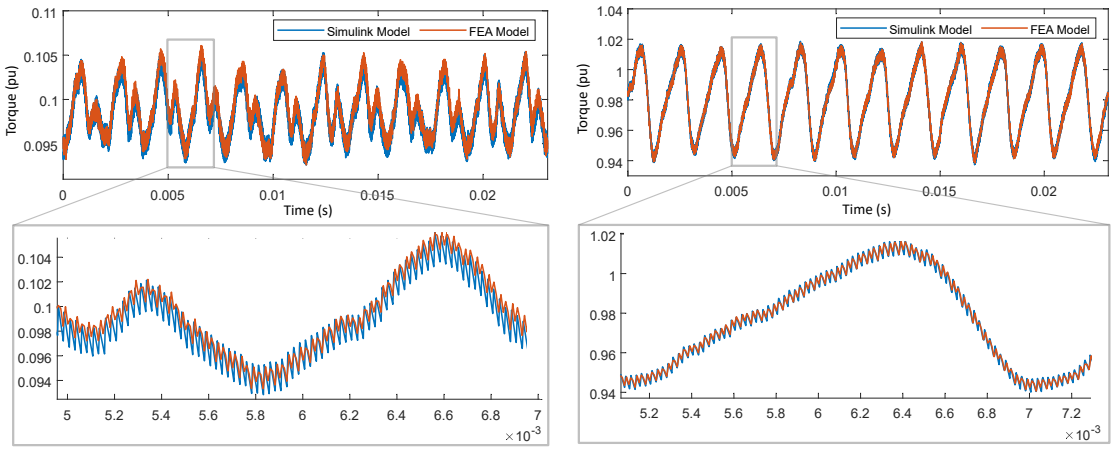
It should be acknowledged that while this thesis only focuses on the total switching and conduction losses of the inverter due to the fact that they lead to the majority of losses, there are other sources of losses that are not being considered. For example, DC-link capacitor losses are discussed in detail in [83] where harmonic analysis of the capacitor currents is required to determine these losses. Additionally, it is also important to properly design the bus bar of the inverter as the effects of stray inductance and capacitance can lead to additional losses as discussed in [84]. While the inverter model used throughout this thesis does not consider these other sources of losses, it should still be assumed that they are present in the system and would result in a slight reduction of the inverter efficiency calculations.

3.5 Dual Three-Phase Drive Simulink Model FEA Validation

As the proposed Simulink drive model can effectively track reference d and q axis current values to generate a desired torque reference, validation of the model can be completed by taking the torque generated in the Simulink model and comparing it to the torque that is generated in FEA. This can be done by using the phase currents generated by the motor subsystem of the Simulink model as the excitation current to FEA. It is important to note that the phase currents from Simulink are downsampled

before being used as inputs in FEA to reduce the computation time, which leads to a small error between the Simulink and FEA torque waveforms. To reduce this error, the factor at which the waveform is downsampled should be reduced or downsampling should not be used at all. An alternate method to improving the accuracy of the Simulink model is to make modifications when generating the lookup tables from the motor subsystem by lowering the interval of current values, but this also leads to longer computation times in FEA. Additionally, as the operating frequency of the machine plays a significant factor in the dynamic behaviour of the motor and the high-frequency current ripple, torque results from the Simulink drive model for different speeds will be displayed and compared to the FEA results. Note that throughout this thesis, only the constant torque operating region is considered and that is the region that the controller has been designed for. Therefore, the validation of the Simulink model only considers speeds up to the base speed of the motor throughout this section.

First, validating the Simulink drive model using a low speed that is $\frac{1}{4}$ the rated base speed of the motor, to observe the accuracy of the model, a torque comparison is completed for torque values of $0.1pu$ and $1.0pu$ relative to the rated torque of the machine. Recall that the reference torque values are obtained through offline selection of d and q axis currents based on the MTPA profile of the machine. The results at $\frac{1}{4}$ of the base speed for both load torque values can be seen in Figure 3.13 with a magnified section of each figure also displayed. The top waveform of each figure is the generated torque for one full electrical cycle and the magnified figure below is of a 30° section from this waveform.



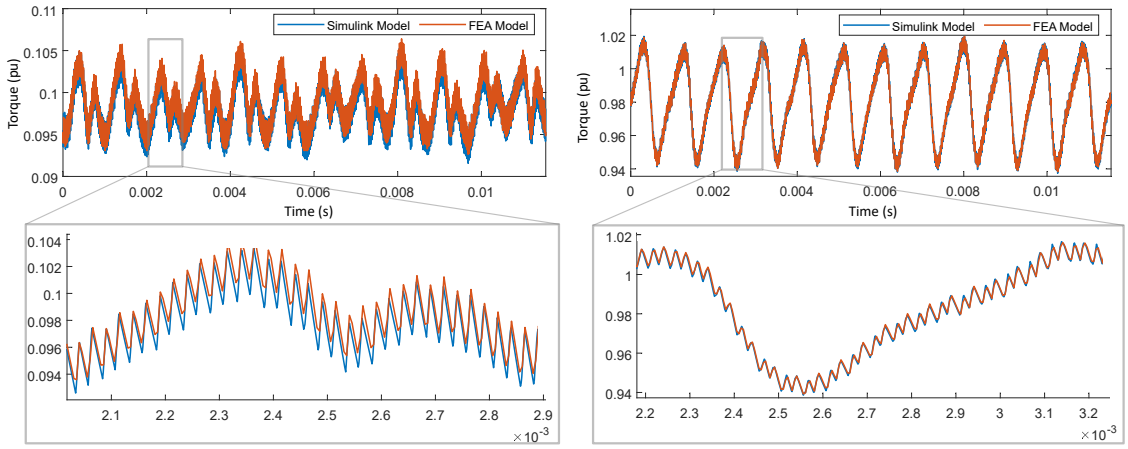
(a) Load Torque = $0.1pu$ (b) Load Torque = $1.0pu$

Figure 3.13: Simulink and FEA Torque Comparison for $\frac{1}{4}$ of the Motor Base Speed

From Figure 3.13, it can be seen that there is a small error between the Simulink and FEA torque waveforms as a result of the downsampled excitation current and the interval used for generating synchronous reference frame current LUTs. However, even with this error considered, it can be seen that the dynamic behaviour of the multiphase machine is accurately represented in the Simulink drive model with similar accuracy to FEA calculations even considering the effect of the inverter switching instances. With just this small error between the Simulink and FEA torque waveforms, it also must be considered that the Simulink model completes all computations in a fraction of the time compared to the FEA model. The Simulink model is able to make this calculation for 230769 points in just 45 seconds, whereas in FEA, the calculation of the downsampled 2308 points takes 4560 seconds.

Similar results can be observed when increasing the speed of the motor to $\frac{1}{2}$ the base speed. Once again using reference torque values of $0.1pu$ and $1.0pu$ relative to the rated torque of the machine, the torque waveforms from Simulink and FEA can be seen in Figure 3.14. Again, the currents used for excitation in FEA have been

downsampled where the phase current waveform for one electrical cycle in Simulink is constructed of 115384 sample points and the phase current used for excitation in FEA is reduced to 2308 sample points.



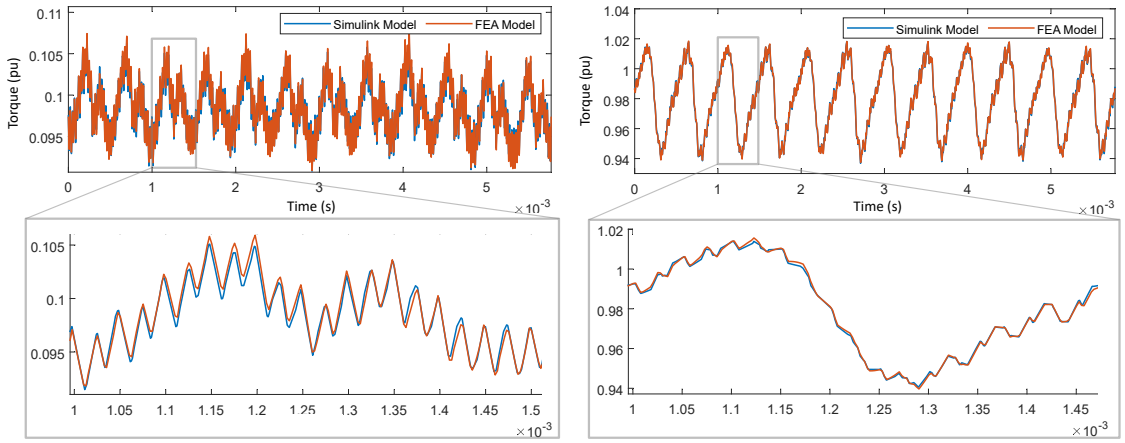
(a) Load Torque = 0.1pu (b) Load Torque = 1.0pu

Figure 3.14: Simulink and FEA Torque Comparison for $\frac{1}{2}$ of the Motor Base Speed

The results from Figure 3.14 once again show higher accuracy at a higher load torque due to the error between the Simulink and FEA waveforms being magnified at lower torque values. However, once again, the dynamic behaviour of the machine is accurately modelled using the Simulink drive model with the inclusion of the high-frequency current ripple as a result of the inverter switching instances.

Lastly, the speed can be increased to the base speed of the motor to prove the validation of the model for the entire constant torque operating region. With the same process being used for this speed point as was used for the previous speeds, the results for torque values of 0.1pu and 1.0pu relative to the rated torque of the machine can be seen in Figure 3.15. As the speed of the machine increases, the number of points calculated in Simulink is reduced as a result of the fixed Simulink step time. However, downsampling is still required for the verification at base speed,

but a smaller downsampling factor can be used which is why the accuracy of the verification process seems to improve as the speed of the machine increases.



(a) Load Torque = $0.1pu$ (b) Load Torque = $1.0pu$

Figure 3.15: Simulink and FEA Torque Comparison for the Motor Base Speed

In general, all speeds provide similar accuracy results for the low and high reference torque values. Although the error appears to be larger for the lower reference torque values, this is because of the smaller scale in each of these figures. Overall, the Simulink model can simulate the dynamic behaviour of the machine while also incorporating the high-frequency current ripple introduced by the inverter. This can be carried over to high-speed operation but that is not within the scope of this thesis.

3.6 Summary

As a proposed dynamic modelling strategy of dual three-phase drive systems has been developed and validated with FEA results through torque waveform comparisons for the same given phase current waveforms, investigations into the overall efficiency of these drive systems can now be completed. As this thesis has a main focus of improving the VSI efficiency through the use of different modulation techniques, implementing these techniques using this Simulink model will provide informative calculations on if the VSI efficiency is improved and whether or not this is at the expense of the motor performance. As validation with FEA results shows promising accuracy results of the proposed Simulink drive model, further validation will be provided in Chapter 5 using experimental results when the experimental implementation of different switching techniques is discussed in more detail.

Chapter 4

Proposed Modulation Schemes and Control Strategy to Improve Efficiency of Dual Three-Phase Motor Drives

4.1 Introduction

Through an in-depth literature review provided in Chapter 2, it was discovered that the main focus of the literature regarding switching techniques used in dual three-phase drive systems is the reduction of the phase current THD. As this is a very important aspect of the designed switching techniques, the improved quality of current waveforms is typically responsible for improving the drive system efficiency with regards to the motor and not the inverter. The improvement of the phase current

THD can be accomplished through both control and switching techniques but for both cases, the inverter efficiency remains almost unchanged. This can be seen in Figure 4.1 where an operating condition at the base speed for a full load is once again utilized as it was to show the results when implementing the PR controller in Figure 3.9. Note that in both of these figures, DZSI SPWM has been implemented.

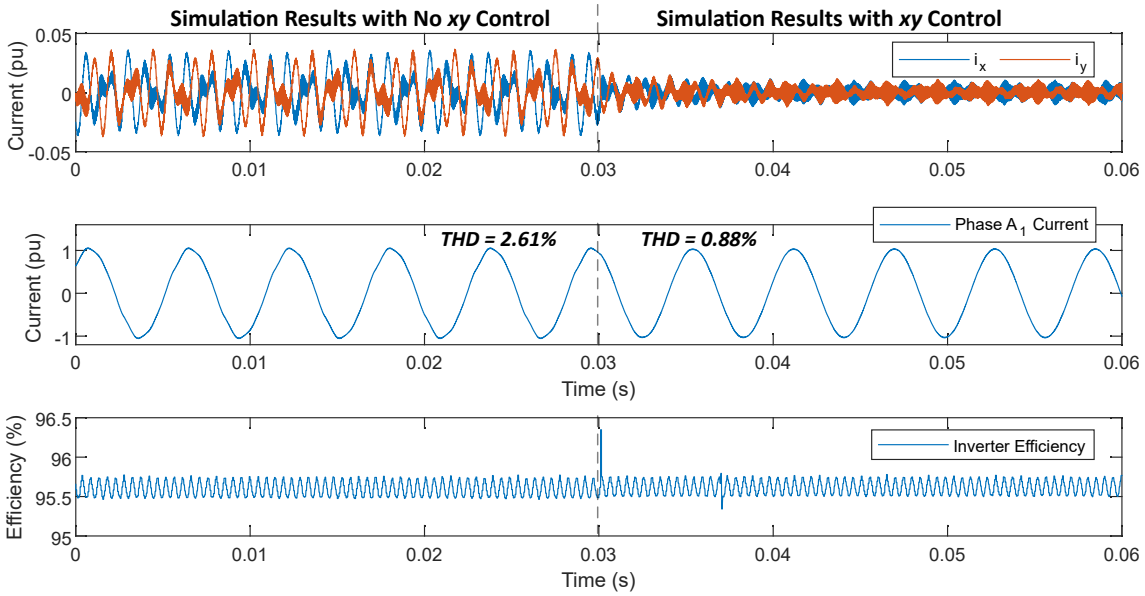


Figure 4.1: Effect of PR Controllers on the Inverter Efficiency for a Fully Loaded Dual Three-Phase IPMSM at Base Speed Using DZSI SPWM

In Figure 4.1, PR controllers are implemented on the x and y axis current components to force these values closer to zero causing the phase current THD to reduce from 2.61% to 0.88%. However, when these controllers are implemented at 0.03 seconds, it can be observed that the inverter efficiency remains constant at around 95.6% through this transition. This shows that there is no correlation between improving the phase current THD and improving the inverter efficiency and this concept can be considered for the development of switching techniques focused on improving the inverter efficiency.

As this thesis aims to optimize the efficiency of the VSI, it has been discovered in this research that reducing the average switching frequency is the best way to increase the drive system efficiency in regards to the VSI while still working to maintain a low phase current THD. For this reason, throughout this chapter, simulation results for the inverter efficiency using the different switching techniques discussed in Chapter 2 will be provided as well as phase current THD results throughout the constant torque region of the machine. Note that all simulation results in this chapter do not utilize PR controllers for the xy subspace as was discussed in Chapter 3 because the use of these controllers for each technique does not have the same performance which could create misleading comparison results. Therefore, to provide the best comparison of each switching technique in regards to inverter efficiency and phase current THD, the xy subspace is not controlled so that the altering performance of PR controllers on each technique is not included in the simulation results. It should be noted that PR controllers can still be implemented to each of these techniques to further improve the drive system performance, which is investigated at the end of this chapter.

Furthermore, to provide simulation results for the desired operating region, three different speeds will be simulated while sweeping the load torque from $0.1pu$ to $1.0pu$ relative to the rated torque of the machine. Recall that the existing techniques to be investigated include DZSI SPWM, C12-4L1Z SVPWM, C12-2L2ML1Z SVPWM, C24-2L1ML1M1Z SVPWM, D24-3L1M1Z SVPWM, and D24-3L2M1Z SVPWM. As previously discussed, a significant benefit of these specific techniques is that they can be easily implemented experimentally without any major modifications required to the PWM drivers of the DSP being used by maintaining the switching frequency equal to the sampling frequency. As the first section of this chapter investigates the

existing techniques, this chapter will also propose new switching techniques to reduce the average switching frequency in an attempt to improve the efficiency of the VSI. As these techniques have a main focus on improving the inverter efficiency, phase current THD results will also be considered as the quality of the current waveform plays a significant role in the overall drive system efficiency in regards to the motor.

4.2 Comparison of Simulation Results using Existing Switching Techniques

Using the Simulink drive model proposed in Chapter 3, the existing switching techniques discussed in detail throughout Chapter 2 can be accurately simulated in the Matlab/Simulink environment. Recall that the inverter subsystem of this model assumes four major sources of power losses in the inverter – IGBT switching losses, IGBT conduction losses, diode switching losses, and diode conduction losses. These power losses are calculated using the PLECS by Plexim Simulink toolbox where the device's power loss information from the datasheet can be loaded directly into the PLECS library. The sum of all the losses for each IGBT module is then used with the input power of the drive system to calculate the inverter efficiency using (3.12). Additionally, as it is still important to maintain a low phase current THD, the Simulink Powergui FFT Analysis tool is also used to calculate the THD of the resultant phase current waveform in the Simulink model.

4.2.1 Inverter Efficiency Analysis

To evaluate each of the existing techniques discussed throughout this thesis, for a given speed, the average inverter efficiency can be calculated as the motor load torque is swept from $0.1pu$ to $1.0pu$ relative to the rated torque of the motor. Recall from Chapter 2 that each technique was defined in terms of being continuous or discontinuous, the number of sectors that the $\alpha\beta$ subspace is divided into, the number of time segments, and the average switching frequency. The characteristics of each switching technique are provided in Table 4.1 as a summary of the discussion from Chapter 2.

Table 4.1: Summary of Existing Switching Techniques Analyzed Throughout this Thesis

Switching Technique	**Number of Sectors**	**Number of Time Segments**	**Average Switching Frequency**
DZSI SPWM	N/A	N/A	20 kHz
C12-4L1Z	12	7	22.5 kHz
C12-2L2ML1Z	12	7	20 kHz
C24-2L1ML1M1Z	24	11	22.5 kHz
D24-3L1M1Z	24	9	19.16 kHz
D24-3L2M1Z	24	11	19.16 kHz

Throughout the literature, each of the techniques from Table 4.1 are implemented in a variety of ways with the main focus being the reduction of the phase current THD. The selection of the specific techniques discussed in this thesis is based on the fact that these techniques allow for the switching frequency to be equal to the sampling frequency. However, with a set sampling frequency of 20 kHz, it can be observed that the average switching frequency for most of these techniques is not the same as the sampling frequency. There are two reasons why this occurs and that includes the utilization of different zero voltage vectors as the sector changes and

some switches not switching on or off during each sample period. This is the result of additional switching instances that must be considered in the average switching frequency calculation and the use of discontinuous switching techniques, respectively.

To allow for a proper comparison between each of the techniques throughout the constant torque operating region, the inverter efficiency for speeds of $\frac{1}{4}$ the base speed, $\frac{1}{2}$ the base speed, and the base speed will be plotted in separate figures. Simulation results of each technique for each respective speed point and a range of load torque values can be seen in Figures 4.2, 4.3, and 4.4. As previously discussed, the inverter subsystem in the Matlab/Simulink environment utilizes the PLECS by Plexim Simulink toolbox to calculate the power losses of each device within the inverter based on the device datasheet. The summation of all power losses from the inverter is used with the input power to the inverter to calculate the efficiency. For each point in Figures 4.2, 4.3, and 4.4, for the respective operating speed, d and q axis current values are determined offline from the dual three-phase machine's MTPA profile to obtain a certain load torque which is given a per-unit value based on the rated torque of the machine. Each simulation is evaluated independently for every operating point and efficiency calculations are taken as the average value of the waveform generated in PLECS using (3.12) once the junction temperature of all IGBT's and diodes have stabilized. Note that this is considering a constant heat sink temperature of 25° C and if this value was increased, the power losses of each device would also increase and lower the overall inverter efficiency.

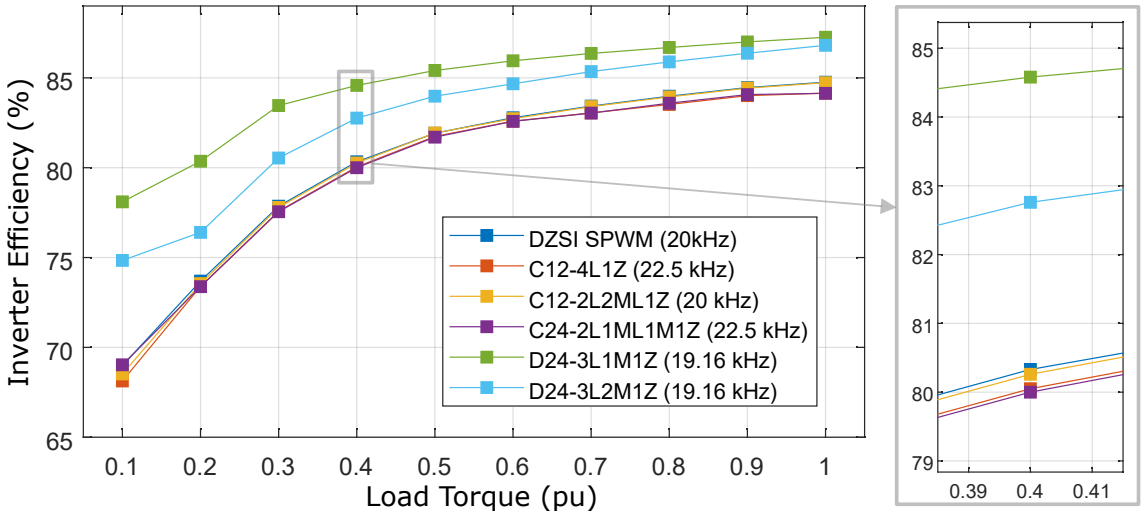


Figure 4.2: Inverter Efficiency as a Function of Load Torque for Operation at $\frac{1}{4}$ of the Motor Base Speed

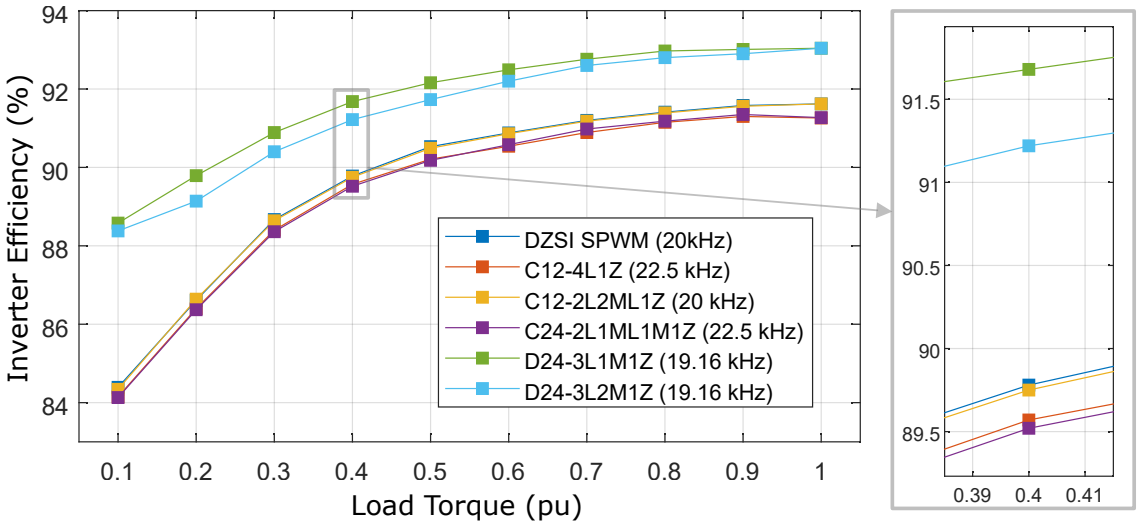


Figure 4.3: Inverter Efficiency as a Function of Load Torque for Operation at $\frac{1}{2}$ of the Motor Base Speed

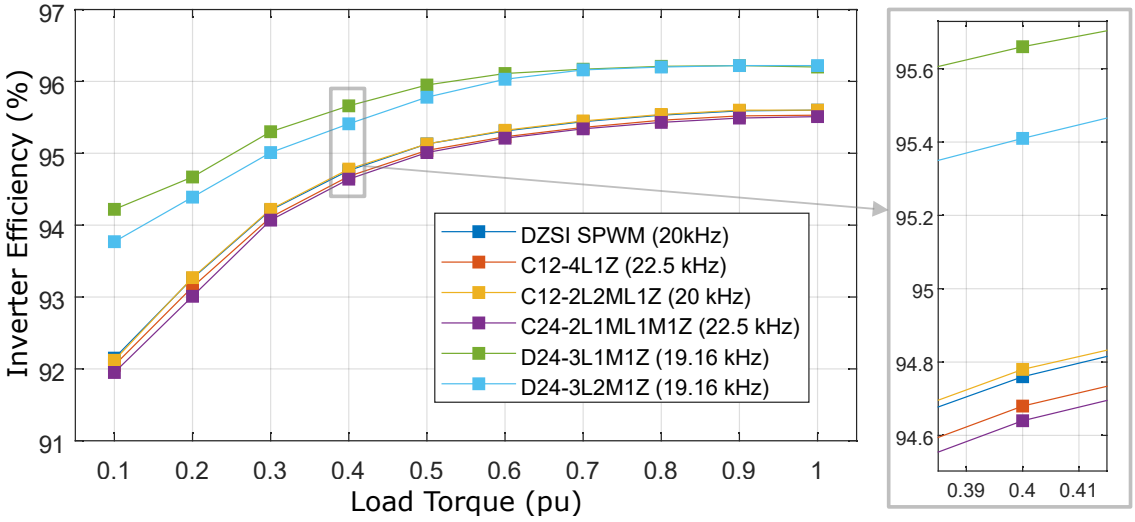


Figure 4.4: Inverter Efficiency as a Function of Load Torque for Operation at the Motor Base Speed

From these figures, certain patterns can be noticed when referring back to the summary of each technique in Table 4.1. As each operating speed provided similar patterns in regards to the different techniques examined, it can be seen that six techniques discussed in this thesis can be separated into three different clusters. The group with the lowest inverter efficiency results among all speed points within the constant torque operating region is composed of the C12-4L1Z and C24-2L1ML1M1Z SVPWM techniques where each switch turns on and off one time in each sampling period and additional switchings are used when changing sectors as the redundant zero voltage vectors change. Both of these techniques were observed to have the highest average switching frequency of 22.5 kHz. The next two techniques that make up the next cluster of waveforms are the DZSI SPWM and C12-2L2ML1Z SVPWM techniques. The benefit of these techniques is that they do not utilize the redundant zero vectors so no switching instances ever take place at the end of a sampling period. This benefit leads to a decrease in the average switching frequency to 20 kHz while

only a small increase in the inverter efficiency of at least 0.2% can be observed. While this is only a slight increase in the inverter efficiency, the removal of the switchings that occur between sectors does have the consistently added benefit of improving the overall VSI efficiency. The main increase in the inverter efficiency comes from the final cluster of waveforms which are generated using the discontinuous SVPWM techniques – D24-3L1M1Z and D24-3L2M1Z. The use of these discontinuous techniques leads to a more significant increase in the inverter efficiency due to at least one switch not turning on or off in a sampling period. This results in a reduction in the average switching frequency to 19.16 kHz for both techniques. It is important to note that both of these discontinuous techniques discussed implement all of the redundant zero vectors and, at times, there exists switching instances as the sector changes between sampling periods.

These patterns were observed at each speed point of the constant torque region further proving that the reduction of the average switching frequency leads to an improved VSI efficiency for a wide range of operating points. To get a better visual of how the average switching frequency affects the inverter efficiency, the breakdown of switching and conduction losses can also be observed. Recall that the observed switching losses are a summation of the turn-on and turn-off IGBT losses, as well as the turn-off losses of each diode in the VSI and that conduction losses are the combination of the IGBT and diode losses during the conduction period. The resultant losses for each technique for operation at the motor base speed and a full load can be seen in Figure 4.5.

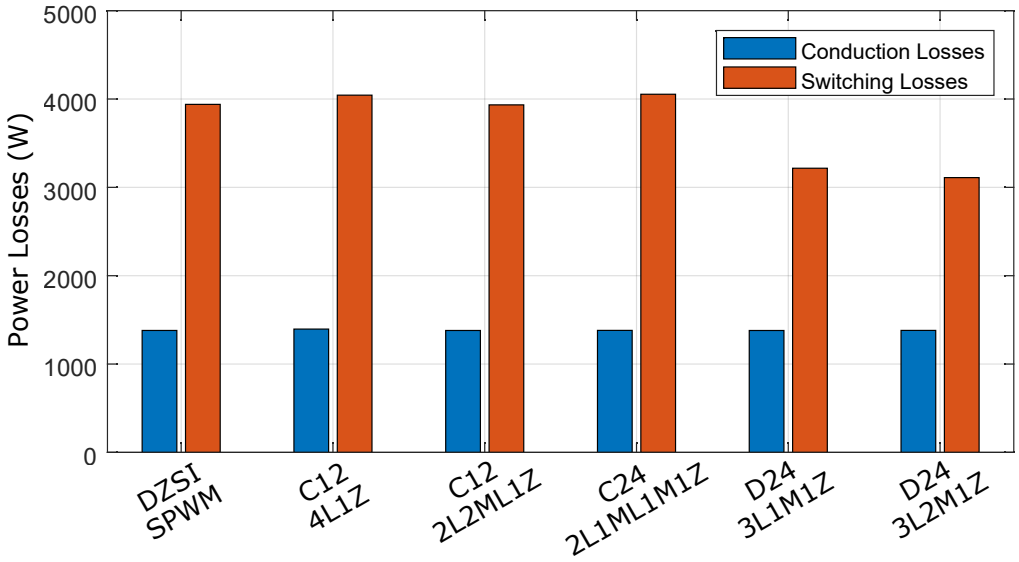


Figure 4.5: Power Loss Breakdown of Each Switching Technique for Operation at the Motor Base Speed with Full Load Torque

From Figure 4.5, it can be seen that while the conduction losses remain relatively constant for each technique, the main difference that affects the inverter efficiency is the switching losses which relate directly to the average switching frequency calculation of each technique in Table 4.1. In Figure 4.5, it can be seen that the discontinuous techniques implemented in this chapter have significantly lower switching losses compared to the other techniques, which shows that the main method of improving VSI efficiency is the implementation of discontinuous switching algorithms. Furthermore, as previously mentioned, there is a small decrease in the switching losses for techniques that do not include switching instances when the sector changes and this is what leads to only a slight increase in the efficiency when implementing the DZSI SPWM and C12-2L2ML1Z SVPWM techniques compared to the C12-4L1Z and C24-2L1ML1M1Z SVPWM techniques.

From the simulation results provided in this section, it is clear that the use of discontinuous techniques and reducing the number of switching instances in each sample period is what will lead to the most efficient operation of the voltage source inverter for dual three-phase drive systems. This includes both the removal of switching instances as the sector changes and having at least one switch not turning on or off during each sample period. While multiple speed points have been analyzed in this section, these conclusions can be made for the entire constant torque operating region. As the discontinuous techniques proved to have the best overall inverter efficiency compared to continuous SVPWM switching techniques and the DZSI SPWM technique, it is important to also maintain a low phase current THD which will be analyzed in the next section. That being said, with the idea of generating switching algorithms to improve the VSI efficiency, discontinuous algorithms with as few switching instances as possible should be implemented.

4.2.2 Phase Current THD Analysis

As the focus to this point has been on the inverter efficiency of dual three-phase drive systems, it is also important to maintain a low phase current THD. Although this was previously shown to have a negligible effect on the VSI efficiency, if a proposed switching technique to improve the VSI efficiency also leads to an increase in the phase current THD, then the efficiency of the motor will be impacted. Therefore, the benefit of increasing the inverter efficiency could result in a negative impact on the overall efficiency of the drive system if the switching technique used results in a higher phase current THD. For this reason, it is important to also analyze the phase current THD of each of these techniques for a wide range of operating points. Figure 4.6 provides

the THD results of all the discussed switching techniques at an operating speed equal to the base speed of the motor. These THD results are obtained by sweeping the load torque from $0.1pu$ to $1.0pu$ relative to the rated torque of the machine.

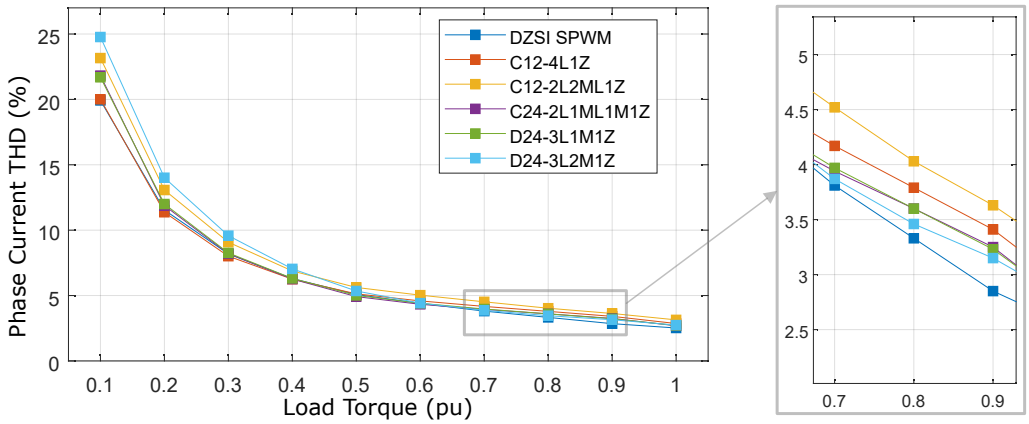


Figure 4.6: Phase Current THD Results for All Existing Switching Techniques at the Motor's Base Speed

From Figure 4.6, it can be seen that of the techniques discussed to this point in this thesis, the DZSI SPWM switching technique consistently results in the lowest phase current THD. Referring back to Table 4.1, the classification of each technique based on the number of time segments within one sample period is what most closely influences the phase current THD. It can be seen in the magnified portion of Figure 4.6 that the C12-4L1Z and C12-2L1ML1M1Z techniques which utilize the lowest number of time segments within a sampling period result in the highest phase current THD results. The remaining SVPWM techniques which utilize a higher number of time segments can then be seen with lower THD results that are more similar to the DZSI SPWM technique. However, it is important to note that the performance of different SVPWM techniques is dependent on the load torque. For example, the C12-4L1Z SVPWM technique has similar harmonic distortion on the phase current

as DZSI SPWM at a low load, but when increasing to a high load, while DZSI SPWM remains the technique with the lowest THD, the C12-4L1Z technique now has the second-highest THD. A similar phenomenon can be observed with the D24-3L2M1Z technique where, at a low load, this technique has the highest THD of all techniques. When a higher load is applied, this technique then improves to have the second-lowest THD results behind the DZSI SPWM. For this reason, adaptive switching techniques have been proposed in [56] where the SVPWM technique changes based on the load torque demanded by the drive system to help reduce the phase current THD as much as possible.

Additionally, the idea of using more time segments to help improve the phase current THD is part of the reason why existing literature looks into having a sampling frequency that is sometimes up to two times the switching frequency. This is seen in many pieces of literature where the proposed SVPWM techniques appear to have better performance than the general DZSI SVPWM [51, 52, 54, 55, 56, 59]. As this thesis solely focuses on switching techniques where the sampling frequency is equal to the switching frequency, a more accurate comparison between SPWM and SVPWM techniques can be provided for a fixed sampling frequency of 20 kHz. The effect of this limitation leads to DZSI SPWM having the best results in terms of reducing the phase current THD and therefore, for the remainder of this thesis, the DZSI SPWM technique will be used as the benchmark for the proposed techniques when analyzing the phase current THD at the base speed of the drive system.

Furthermore, from all of the results obtained throughout this section in regards to both the VSI efficiency and phase THD results, the proposed switching techniques

discussed in the next section aim to further improve the inverter efficiency while maintaining a good quality phase current waveform. Moving forward, the discontinuous techniques discussed throughout this thesis will be used as benchmark waveforms for comparison with proposed switching techniques when looking into the VSI efficiency. This is due to both the D24-3L1M1Z and D24-3L2M1Z techniques having consistently higher inverter efficiency calculations for all operating points within the constant torque region.

4.3 Proposed Switching Techniques to Improve Inverter Efficiency

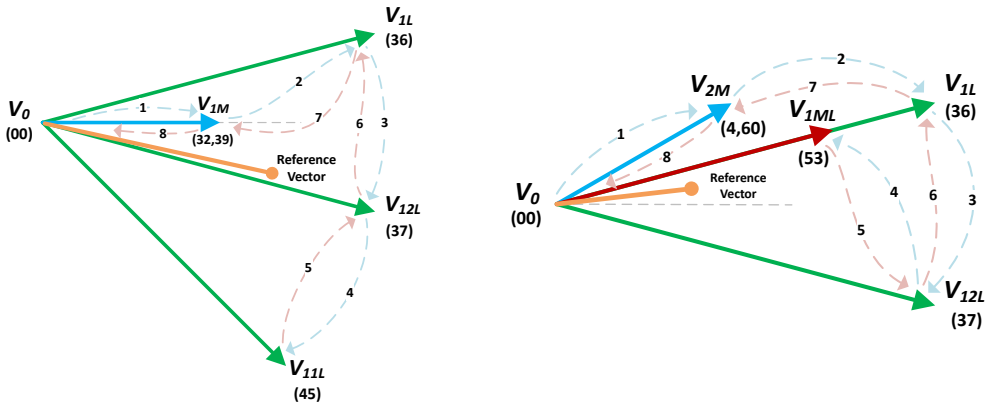
From the results in the previous section, it is clear that the use of discontinuous switching techniques and reducing the overall switching losses of the VSI as much as possible will result in maximum inverter efficiency throughout the constant torque operating region. In this section, after the investigation of several different methods and combinations of techniques, optimal switching algorithms are proposed that combine existing SVPWM strategies with some modifications to reduce the average switching frequency even further, which in turn reduces the overall switching losses of the inverter. The proposed techniques in this thesis implement modified versions of the aforementioned SVPWM algorithms where these techniques often change the pattern of voltage vectors applied every two sectors when considering one full electrical cycle over 24 total sample periods. These algorithms can be implemented in many different ways either using continuous or discontinuous switching, using 12 or

24 sectors, or altering the number of time segments in each sample period. Throughout this section, two different proposed switching techniques will be discussed and compared to the DZSI SPWM, D24-3L1M1Z, and D24-3L2M1Z methods in terms of both inverter efficiency and phase current THD. Recall that the contributions of this thesis are specifically for SVPWM techniques which consider the restriction that the sampling frequency should be equal to the switching frequency. This will be further explored when looking at DSP implementation in the following chapter.

4.3.1 Proposed SVPWM1

The first method of implementing a proposed technique, which will be referred to as SVPWM1, is using a 9-time segment, discontinuous switching algorithm that divides the $\alpha\beta$ subspace into 24 sectors which were seen in Figure 2.10b. This method utilizes the aforementioned D24-3L1M1Z and C24-2L1ML1M1Z techniques where the utilizable voltage vectors are adjusted every two sectors. This allows for the SVPWM1 method to reduce the average switching frequency as much as possible, where all switchings that occur when changing the sector are removed which was proven to result in a small increase in the inverter efficiency in the previous section. Additionally, the switching algorithm used for the SVPWM1 technique ensures that two switches do not turn on or off in each sampling period which is what theoretically leads to a larger increase in the VSI efficiency. For a better visual of how the two existing techniques are combined to make up the SVPWM1 technique, Figure 4.7 and Table 4.2 show a visual representation of the switching pattern as well as the switching patterns for each sector, respectively. In Figure 4.7, it can be observed that in sector 24,

modifications of the D24-3L1M1Z technique are implemented and in sector 1, modifications of the C24-2L1ML1M1Z technique have been implemented. Additionally, in Table 4.2 it can be seen that there are no switchings that occur when changing sectors.



(a) Sector 24 (b) Sector 1

Figure 4.7: Visual Representation for the Sequence of the Voltage Vectors applied for the SVPWM1 Technique Using 9 Time Segments

To get a better understanding of the switching patterns that are implemented using SVPWM1, detailed tables showing the voltage vectors as their binary numbers which represent the VSI phase leg switching state is also provided in Table 4.3. The detailed switching pattern is shown for sectors 11, 12, 13, and 14 where a transition between using three large, one medium, and one zero voltage vector to using two large, one medium-large, one medium, and one zero voltage vector occurs when going from sector 12 to sector 13. It should be noted from Table 4.3 that the phase order is assumed to be $A_1B_1C_1A_2B_2C_2$ and that the most significant bit (MSB) of the binary number corresponds to phase A_1 and the least significant bit (LSB) corresponds to phase C_2.

Table 4.2: Switching Sequence for Each Sector Represented by Decimal Numbers for the SVPWM1 Switching Technique Using 9 Time Segments

Sector	**Decimal Number Switching Sequence**	**Sector**	**Decimal Number Switching Sequence**
1	**00** – 04 – 36 – 37 – 53 – 37 – 36 – 04 – **00**	13	**00** – 02 – 10 – 26 – 27 – 26 – 10 – 02 – **00**
2	**00** – 32 – 36 – 52 – 53 – 52 – 36 – 32 – **00**	14	**00** – 08 – 10 – 11 – 27 – 11 – 10 – 08 – **00**
3	**00** – 04 – 36 – 52 – 54 – 52 – 36 – 04 – **00**	15	**00** – 08 – 09 – 11 – 27 – 11 – 09 – 08 – **00**
4	**00** – 04 – 36 – 52 – 54 – 52 – 36 – 04 – **00**	16	**63** – 08 – 09 – 11 – 27 – 11 – 09 – 08 – **63**
5	**00** – 04 – 20 – 52 – 54 – 52 – 20 – 04 – **00**	17	**00** – 01 – 09 – 11 – 43 – 11 – 09 – 01 – **00**
6	**00** – 16 – 20 – 22 – 54 – 22 – 20 – 16 – **00**	18	**00** – 08 – 09 – 41 – 43 – 41 – 09 – 08 – **00**
7	**00** – 16 – 18 – 22 – 54 – 22 – 18 – 16 – **00**	19	**00** – 01 – 09 – 41 – 45 – 41 – 09 – 01 – **00**
8	**63** – 16 – 18 – 22 – 54 – 22 – 18 – 16 – **63**	20	**00** – 01 – 09 – 41 – 45 – 41 – 09 – 01 – **00**
9	**00** – 02 – 18 – 22 – 30 – 22 – 18 – 02 – **00**	21	**00** – 01 – 33 – 41 – 45 – 41 – 33 – 01 – **00**
10	**00** – 16 – 18 – 26 – 30 – 26 – 18 – 16 – **00**	22	**00** – 32 – 33 – 37 – 45 – 37 – 33 – 32 – **00**
11	**00** – 02 – 18 – 26 – 27 – 26 – 18 – 02 – **00**	23	**00** – 32 – 36 – 37 – 45 – 37 – 36 – 32 – **00**
12	**00** – 02 – 18 – 26 – 27 – 26 – 18 – 02 – **00**	24	**00** – 32 – 36 – 37 – 45 – 37 – 36 – 32 – **00**

Table 4.3: Detailed Analysis of the Proposed SVPWM1 Switching Pattern for Sectors 11-14

	Sector 11									**Sector** 12								
MSB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Binary #	0	0	1	1	1	1	1	0	0	0	0	1	1	1	1	1	0	0
	0	0	0	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	0
LSB	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0
Decimal #	**00**	02	18	26	27	26	18	02	**00**	**00**	02	18	26	27	26	18	02	**00**

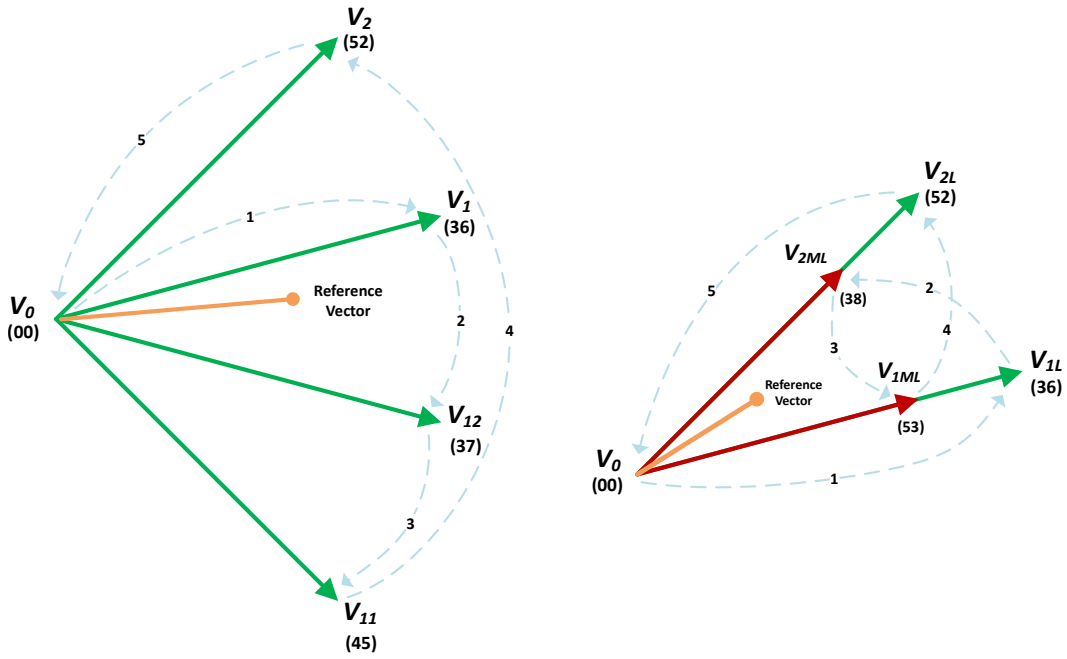
	Sector 13									**Sector** 14								
MSB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Binary #	0	0	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0
	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0
LSB	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	0	0
Decimal #	**00**	02	10	26	27	26	10	02	**00**	**00**	08	10	11	27	11	10	08	**00**

From Table 4.3, it can be observed from the transitions in switching states for each sector shown, that at least two switches do not turn on or off in each sampling period. Considering the lack of switching for at least two switches, and that there are no switchings that take place when changing sectors, the average switching frequency of this technique can be calculated using (2.10). This results in the average switching frequency of the discontinuous SVPWM1 technique being 13.33 kHz for a given carrier frequency of 20 kHz. Additionally, an added benefit of this proposed technique is the fact that only one switch turns on or off whenever there is a change in the voltage vector which can be seen in Table 4.3. However, it is important to acknowledge that this switching pattern has been designed with only reducing the average switching frequency in mind and not considering the phase current THD. As an ideal switching pattern would also result in a lower phase current THD, many of the concepts of the proposed SVPWM1 technique can be implemented using other methods.

4.3.2 Proposed SVPWM2

As the previous technique focused solely on increasing the inverter efficiency by reducing the switching frequency to 13.33 kHz, similar concepts can be used to still lower the average switching frequency while also considering the phase current THD. The next method to be discussed in this thesis combines the switching patterns of the C12-4L1Z and C12-2L2ML1Z SVPWM techniques where each of these algorithms is altered to allow for discontinuous switching. The proposed method, which will be referred to as SVPWM2, is a 12 sector switching method implemented using discontinuous switching and limited to 6-time segments to meet the requirement of maintaining the sampling frequency equal to the switching frequency. Similar to the previously

discussed SVPWM1 technique, the SVPWM2 technique also removes any switchings that occur when the sector changes. As the combination of the C12-4L1Z and C12-2L2ML1Z SVPWM techniques lead to more fluid transitions between each sector, a reduction in the phase current THD can be observed. However, it should be noted that for the SVPWM2 technique, half of the sectors have two switches that do not turn on or off in each sample period and half of the sectors have only one switch that does not turn on or off each sample period. For a better visual representation of the second switching technique that has been proposed, Figure 4.8 shows the transition between using four large and one zero voltage vector in sector 12 to using two large, two medium-large, and one zero voltage vector in sector 1. Additionally, Table 4.4 provides the switching pattern for each sector of the SVPWM2 switching method.



(a) Sector 12 (b) Sector 1

Figure 4.8: Visual Representation for the Sequence of the Voltage Vectors applied for the SVPWM2 Technique Using 6 Time Segments

Table 4.4: Switching Sequence for Each Sector Represented by Decimal Numbers for the SVPWM2 Switching Technique Using 6 Time Segments

Sector	**Decimal Number Switching Sequence**	**Sector**	**Decimal Number Switching Sequence**
1	**00** – 36 – 38 – 53 – 52 – **00**	7	**00** – 10 – 11 – 27 – 25 – **00**
2	**00** – 36 – 52 – 54 – 22 – **00**	8	**00** – 09 – 11 – 27 – 41 – **00**
3	**00** – 20 – 22 – 54 – 50 – **00**	9	**00** – 09 – 13 – 43 – 41 – **00**
4	**00** – 18 – 22 – 54 – 26 – **00**	10	**00** – 09 – 41 – 45 – 37 – **00**
5	**00** – 18 – 19 – 30 – 26 – **00**	11	**00** – 33 – 37 – 45 – 44 – **00**
6	**00** – 18 – 26 – 27 – 11 – **00**	12	**00** – 36 – 37 – 45 – 52 – **00**

From Table 4.4, the use of six time segments as well as the removal of the switchings that occur when the sector changes can be seen. The switchings can be further investigated by looking into the resultant binary numbers of each sector. In table 4.5, the binary numbers and their corresponding decimal numbers are displayed to show the transition between the on and off state of each phase leg for sectors 7, 8, 9, and 10. Recall that the phase order is assumed to be $A_1B_1C_1A_2B_2C_2$ and that the MSB of the binary number corresponds to phase A_1 and the LSB corresponds to phase C_2.

In Table 4.5, the detailed analysis of the SVPWM2 switching algorithm shows that in sectors 7 and 9, two large, two medium-large, and one zero voltage vector are utilized and in sectors 8 and 10, four large and one zero voltage vectors are utilized. Additionally, in sectors 8 and 9, there is only one switch that does not turn on or off in each sector whereas, in sectors 7 and 10, there are two switches that do not turn on or off. With the patterns of this switching technique observed in Figure 4.8 and Tables 4.4 and 4.5, the average switching frequency of the SVPWM2 technique can be calculated using (2.10). As the carrier frequency remains at 20 kHz, the calculated average switching frequency for the proposed technique is 15 kHz.

Table 4.5: Detailed Analysis of the Proposed SVPWM2 Switching Pattern for Sectors 7-10

	Sector 7						**Sector** 8					
MSB	0	0	0	0	0	0	0	0	0	0	1	0
Binary #	0	0	0	1	1	0	0	0	0	1	0	0
	0	1	1	1	1	0	0	1	1	1	1	0
	0	0	0	0	0	0	0	0	0	0	0	0
	0	1	1	1	0	0	0	0	1	1	0	0
LSB	0	0	1	1	1	0	0	1	1	1	1	0
Decimal #	**00**	10	11	27	25	**00**	**00**	09	11	27	41	**00**

	Sector 9						**Sector** 10					
MSB	0	0	0	1	1	0	0	0	1	1	1	0
Binary #	0	0	0	0	0	0	0	0	0	0	0	0
	0	1	1	1	1	0	0	1	1	1	1	0
	0	0	1	0	0	0	0	0	0	1	1	0
	0	0	0	1	0	0	0	0	0	0	0	0
LSB	0	1	1	1	1	0	0	1	1	1	1	0
Decimal #	**00**	09	13	43	41	**00**	**00**	09	41	45	37	**00**

Note that while the technique discussed in this section is considering both a reduction in the average switching frequency and a reduction in the phase current THD, while discontinuous switching is used, only 6-time segments are used to implement SVPWM2. It should be noted that from previous simulation results shown, it was proven that the more time segments that are used, the more the phase current THD can be reduced. However, this is the only allowable number of time segments for this technique for the sampling frequency to remain equal to the switching frequency. The idea of maintaining a low average switching frequency and low phase current THD while increasing the number of time-segments to be used in one sampling period is a concept that will be investigated in the future work of this thesis.

4.3.3 Inverter Efficiency Analysis

As these techniques are designed specifically to reduce the average switching frequency, a comparison to the existing switching techniques is provided to show that the SVPWM1 and SVPWM2 techniques lead to an increase in the VSI efficiency. Recall that of the existing switching techniques, the ones that utilized discontinuous switching had the best performance in regards to the VSI efficiency and for this reason, they are used for the comparison of the proposed techniques in this thesis. Additionally, the inverter efficiency results of the DZSI SPWM technique are also included in this section as this technique was proven to have a lower inverter efficiency due to the higher average switching frequency but also the lowest phase current THD of all existing techniques discussed throughout this thesis.

Once again, to provide a proper comparison between all the techniques throughout the constant torque operating region, the inverter efficiency for speeds of $\frac{1}{4}$ the base speed, $\frac{1}{2}$ the base speed, and the base speed will be plotted in separate figures. Similar to the previous discussion regarding the efficiency comparison of existing switching techniques, the proposed switching techniques have been simulated using the Simulink drive model from Chapter 3 at load torque points ranging from $0.1pu$ to $1.0pu$ relative to the rated torque of the dual three-phase drive system. Recall that the method of obtaining the desired load torque is through the offline selection of d and q axis currents based on the MTPA profile of the machine. Additionally, for the VSI efficiency results obtained in this section for the proposed switching techniques, the thermal environment of the inverter in the Simulink model has remained constant where the heat sink temperature is fixed at $25°C$.

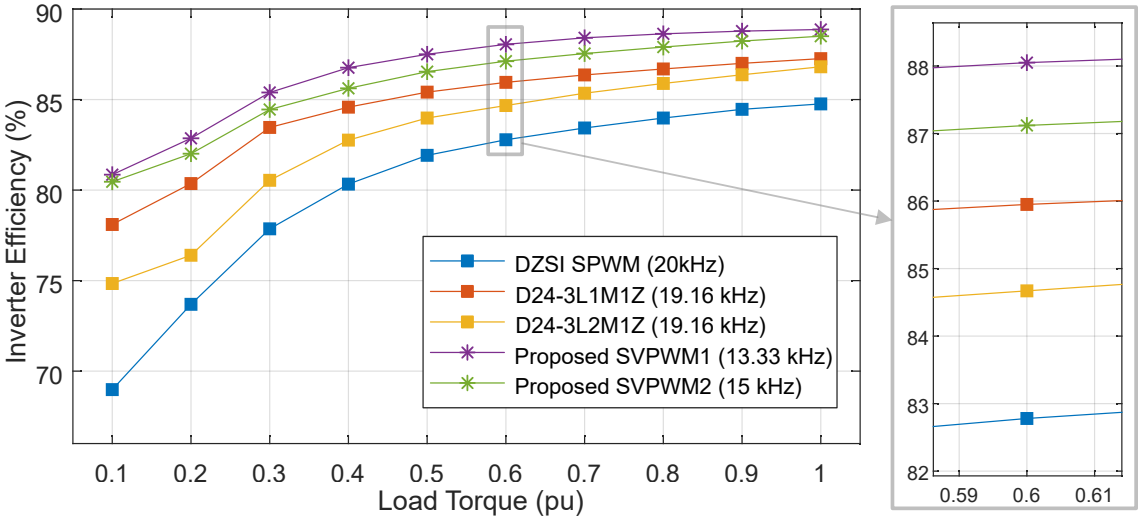


Figure 4.9: Inverter Efficiency of Proposed Switching Techniques as a Function of Load Torque for Operation at $\frac{1}{4}$ of the Motor Base Speed

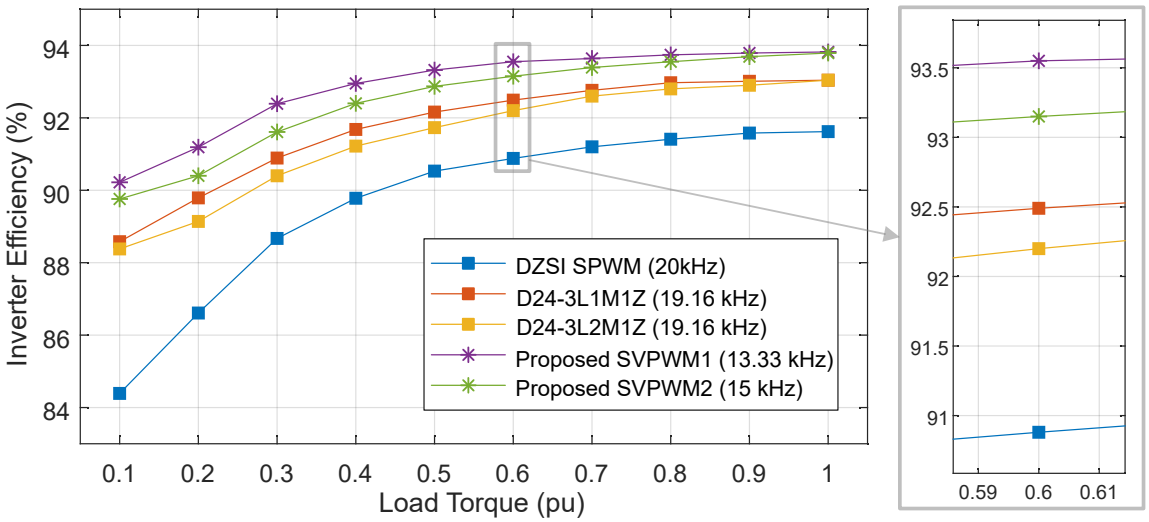


Figure 4.10: Inverter Efficiency of Proposed Switching Techniques as a Function of Load Torque for Operation at $\frac{1}{2}$ of the Motor Base Speed

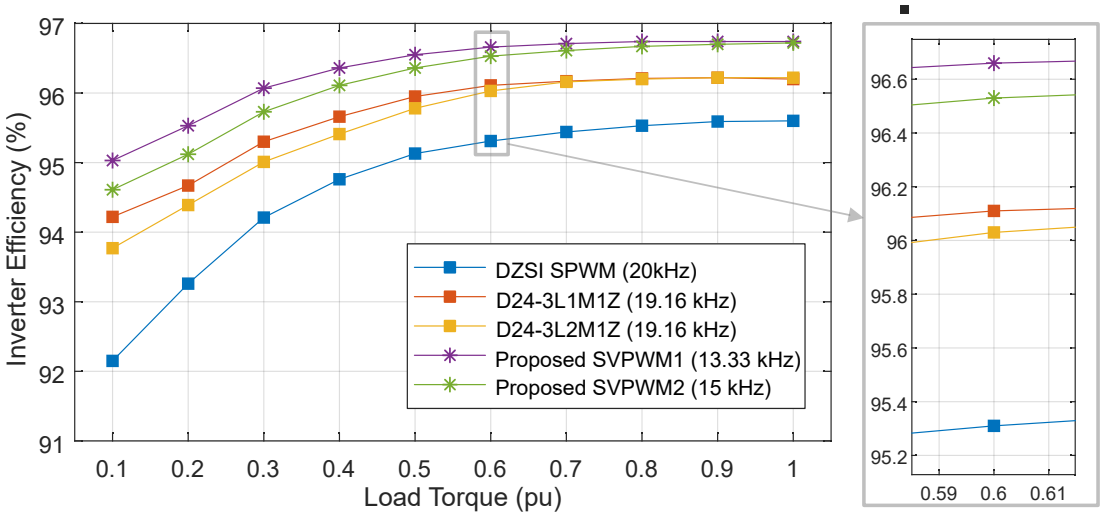


Figure 4.11: Inverter Efficiency of Proposed Switching Techniques as a Function of Load Torque for Operation at the Motor Base Speed

From Figures 4.9, 4.10, and 4.11, the inverter efficiency of the proposed techniques is displayed as the trajectories represented with the asterisks and the existing techniques are displayed as the trajectories represented by the squares. Similar to the VSI efficiency analysis of the existing techniques, the same patterns are seen for all speed points that have been simulated. It is worth noting that as the speed decreases, there is an increase in the difference between the inverter efficiency of each technique. It can be seen in Figures 4.9, 4.10, and 4.11 that the SVPWM1 technique has an increased inverter efficiency which is directly related to the reduction of the average switching frequency to 13.33 kHz. This has led to an increase in the VSI efficiency of at least 0.52% and up to almost 3% at low operating points when being compared to the aforementioned existing techniques. However, this SVPWM1 technique was designed solely considering reducing the average switching frequency and not considering maintaining a low phase current THD. For this reason, SVPWM2 was proposed to improve the phase current THD which will be analyzed in the next section.

While the SVPWM2 switching technique was designed keeping the phase current THD in mind, the main design benefit of this technique remains that a low average switching frequency of 15 kHz is maintained. Although there has been a trade-off of slightly increasing the average switching frequency to improve the phase current THD, it can still be seen from Figures 4.9, 4.10, and 4.11 that while the inverter efficiency results for the SVPWM2 technique are not as high as SVPWM1, SVPWM2 still has better performance than the aforementioned existing techniques. More specifically, when comparing SVPWM2 to the D24-3L1M1Z technique which previously had the best performance for VSI efficiency, the SVPWM2 technique leads to an increase in the inverter efficiency of at least 0.40% and up to 2.5%. As both the SVPWM1 and SVPWM2 techniques have been proven to result in improved VSI efficiency, it is also necessary to analyze the phase current THD of these techniques to ensure that with this improvement in the inverter efficiency, an improvement in the motor efficiency is not sacrificed so that the efficiency of the entire dual three-phase drive system will be increased.

Furthermore, as the inverter efficiency results over the constant torque region have been displayed, the loss breakdown of the proposed techniques can be compared to the existing techniques by observing the total losses broken down in terms of conduction losses and switching losses. In Figure 4.12, it can be seen that the conduction losses remain constant for all techniques being compared, but the switching losses for SVPWM1 and SVPWM2 are lower than the switching losses of the previously discussed techniques. Furthermore, the switching losses of SVPWM1 are slightly lower than those of SVPWM2 further proving that the lower the average switching frequency, the lower the losses of the VSI are, which results in higher inverter efficiency.

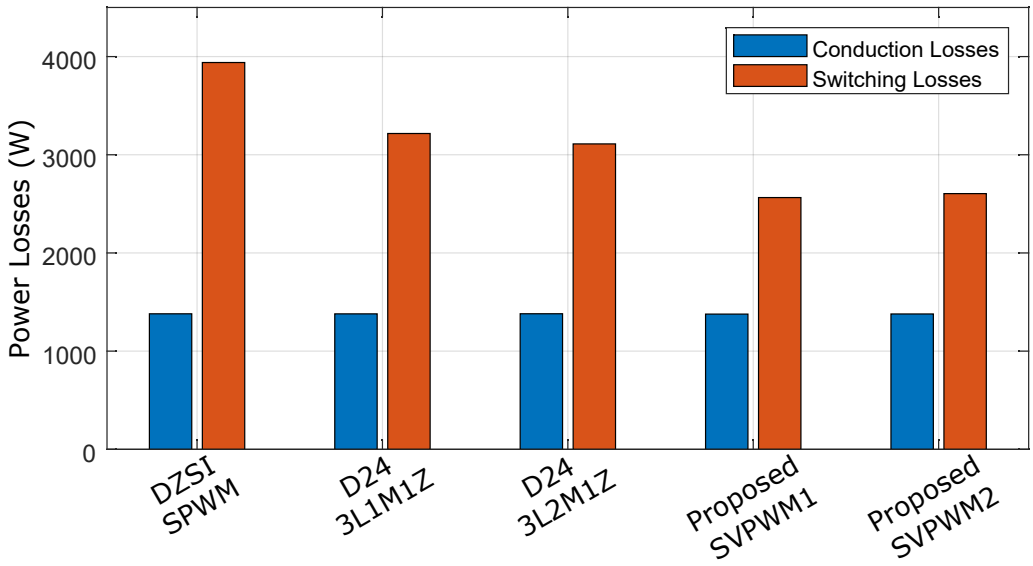


Figure 4.12: Power Loss Breakdown of the Proposed Switching Techniques for Operation at the Motor Base Speed with Full Load Torque

4.3.4 Phase Current THD Analysis

As the SVPWM1 and SVPWM2 techniques have been proven to result in a higher VSI efficiency than other existing techniques, the use of these proposed techniques is not practical if this results in a higher phase current THD. This is because although the efficiency of the inverter has increased, an increase in the phase current THD results in the efficiency of the motor being reduced. Moreover, while the overall goal is to improve the efficiency of the entire dual three-phase drive system, the efficiency of both the inverter and the motor must be considered and, therefore, increasing the average switching frequency should not come at the cost of increasing the phase current THD. In Figure 4.13, the phase current THD results of the proposed SVPWM1 and SVPWM2 switching techniques for a range of load torque values are provided at the base speed of the machine. The load torque values range from $0.1pu$ to $1.0pu$ relative to the rated torque of the machine, similar to the other simulation

results that have been provided throughout this thesis. Once again, the proposed techniques are displayed as the trajectories represented with the asterisks and the existing techniques are displayed as the trajectories represented by the squares.

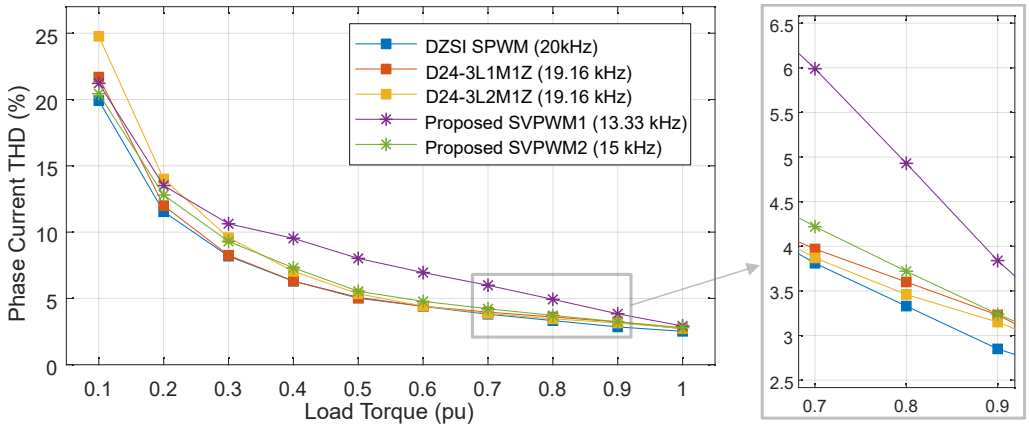


Figure 4.13: Phase Current THD Results for the Proposed Switching Techniques at the Motor's Base Speed

From Figure 4.13, the first thing to be noticed is that SVPWM1 does not follow similar trajectories to the existing techniques. The poor phase current THD results are an outcome of the transitions between using three large, one medium, and one zero voltage vector to using two large, one medium-large, one medium, and one zero voltage vector generating large spikes in the xy subspace current waveforms. This is due to the different characteristics that the D24-3L1M1Z and C24-2L1ML1M1Z techniques have in regards to calculating the dwell times of each switch of the VSI. Therefore, the resultant spikes in the xy subspace lead to additional distortion of the phase current waveform which has a negative effect on the motor performance. This means that while SVPWM1 is proven to have the best inverter performance, this technique would result in the worst motor performance which could even lead to a negative impact on the overall efficiency of the dual three-phase drive system.

The issue with the increased phase current THD that is associated with the SVPWM1 technique is the reason why the SVPWM2 technique was also proposed in this thesis. Although it was previously shown that SVPWM2 has slightly inferior inverter performance throughout the constant torque operating region compared to SVPWM1, in Figure 4.13, this switching technique sees a significant improvement to the phase current THD which more closely matches the trajectories of the existing techniques that have been discussed. The reason for the improvement in the phase current THD of the SVPWM2 technique is that the switching characteristics when using four large and one zero voltage vector are very similar to the characteristics when using two large, two medium-large, and one zero voltage vector. This allows for much smoother transitions between the sectors where the utilizable voltage vectors are changing. This helps to reduce the current spikes on the xy subspace that led to the poor THD performance of the SVPWM1 technique.

When considering all switching techniques discussed throughout this chapter, the results provided show evidence that a trade-off exists between reducing the average switching frequency and increasing the phase current THD. This is seen when referring to Figure 4.13 where the DZSI SPWM, which has the highest average switching frequency, also has the lowest current THD, and the SVPWM2 technique which had the lowest average switching frequency had the highest current THD. For this reason, while it cannot be expected for proposed switching techniques which have lower calculated average switching frequencies to have a lower THD than the DZSI SPWM technique, it can be expected that sacrificing a small percentage of the phase current THD can lead to more significant increases in the inverter efficiency. In turn, this could result in a larger net increase in the overall efficiency of a dual three-phase drive

system and that is why future work of this thesis intends to investigate each of these switching techniques and the effect that they have on the motor efficiency through the use of FEA loss calculations.

4.4 Proposed Control Scheme to Improve Motor Drive Efficiency

As previously mentioned, the simulation results shown throughout this chapter have not included the use of the PR controllers for the synchronous frame xy_r subspace as it was proven that the inclusion of these controllers does not have any effect on the inverter efficiency calculation. However, it was seen in Figure 4.1 that the use of these PR controllers contributes to improving the phase current THD. Therefore, as the proposed SVPWM techniques were designed to improve the inverter efficiency, the extension of using PR controllers with these switching techniques can lead to a reduction in the phase current THD resulting in improved motor performance. As the proposed modulation techniques from this chapter have been proven to increase the inverter efficiency, this section will explore the combination of utilizing these modulation schemes with PR controllers for the x and y axis current components, leading to reduced phase current THD and increased drive system efficiency.

Recall that the effect of the PR controller when using the DZSI SPWM was already displayed in Figure 3.9 for the motor base speed at a full load where the x and y components were not actively controlled for the first 0.03 seconds of the simulation. The PR controller for the xy_r subspace was then activated at 0.03 seconds and the x and y component both converged to zero where this made a noticeable improvement

in the phase current THD as it reduced from 2.61% to 0.88%. As the use of the PR controllers has already been shown to improve the phase current waveform when using the DZSI SPWM technique, simulation results for the same operating point can be obtained using the proposed SVPWM1 and SVPWM2 techniques and seen in Figures 4.14 and 4.15 respectively. For both of these figures, simulation results are collected for the base speed of the motor at a full load where the xy_r subspace is not controlled for the first half of the simulation and then the PR controllers for both the x and y components are activated at 0.03 seconds.

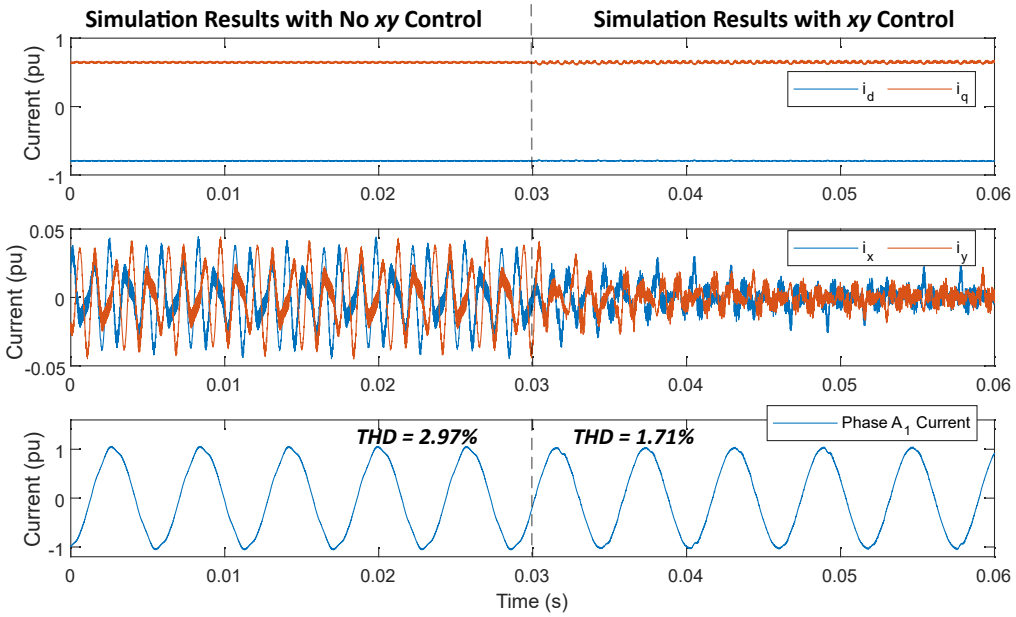


Figure 4.14: Simulation Results for a Fully Loaded Dual Three-Phase IPMSM at Base Speed Using SVPWM1 Switching

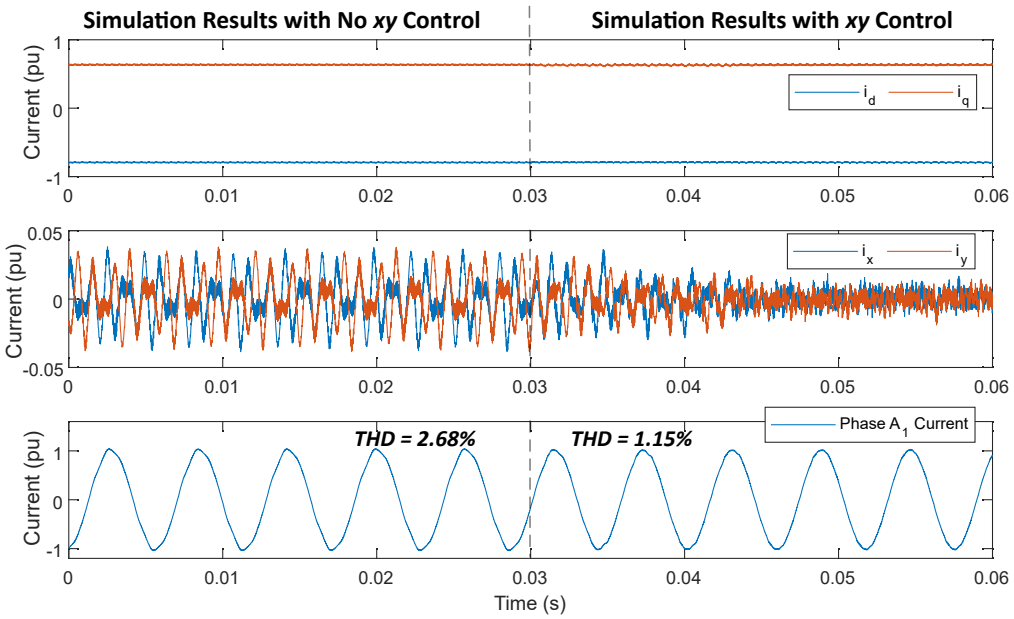


Figure 4.15: Simulation Results for a Fully Loaded Dual Three-Phase IPMSM at Base Speed Using SVPWM2 Switching

From Figure 4.14 and 4.15, it can be further validated that the use of PR controllers reduce the phase current THD as both the x and y components are suppressed to be closer to zero. Specifically looking into Figure 4.14, recall that while the SVPWM1 technique has been designed solely considering the reduction of the average switching frequency, the phase current waveform had the poorest quality of all switching techniques that have been discussed throughout this thesis. This same concept is also observed when looking at the THD results when the PR controller has been implemented at 0.03 seconds in Figure 4.14. The larger phase current THD compared to the DZSI SPWM and SVPWM2 techniques in Figures 3.9 and 4.15, respectively, is a result of the current spikes in the x and y current waveforms which are generated when the utilizable voltage vectors change between three large, one medium, and one zero voltage vector to two large, one medium-large, one medium,

and one zero voltage vector every two sectors. Although the x and y values are suppressed to be closer to zero when the SVPWM2 technique is used, these current spikes are still present on these waveforms leading to increased distortion on the phase current. This further validates the conclusion that while the SVPWM1 technique might result in improved inverter efficiency, the sacrifice in the quality of the phase current waveform could lower the overall dual three-phase drive efficiency.

Alternatively, looking into Figure 4.15, which implements the proposed SVPWM2 technique, it can first be observed that the phase current THD without any control of the x and y axis currents at 2.68% is close to the performance when using DZSI SPWM at the same condition where the THD was 2.61%. Furthermore, when the PR controllers are applied to the xy_r subspace in Figure 4.15, these components are reduced to be as close to zero as possible as intended. Recall, that the design of the switching algorithm of the SVPWM2 technique considers the phase current THD by ensuring that the transition between sectors that use four large, one zero voltage vector and sectors that use two large, two medium-large, and one zero voltage vector is more fluid than the aforementioned SVPWM1 technique. This helps to reduce spikes in the x and y axis currents which is further verified when implementing PR controllers where these spikes are hardly noticeable unlike the simulation results when using the SVPWM1 technique. In fact, the simulation results using SVPWM2 switching with PR controllers controlling the xy_r subspace result in a phase current THD of 1.15% which is closer to the resultant THD of 0.88% when using DZSI SPWM switching compared to when using SVPWM1 which resulted in a THD of 1.71%. This once again shows promising results in the proposed concept of the SVPWM2 technique, as this algorithm works to both improve the inverter efficiency as well as maintain a

low phase current THD leading to improvements in the overall efficiency of the dual three-phase drive system.

As the results of the proposed switching techniques have been validated using the proposed Simulink model verified by both FEA and experimental results, the future work of this thesis intends to implement these techniques using a high-power experimental setup. As this setup must be able to accommodate a 100 kW dual three-phase drive system, many design considerations such as an appropriate dynamometer, cooling system, and safety system are necessary. As the design and construction of this setup are outside the scope of this thesis, it is still possible to prepare a suitable control algorithm for the testing and validation of multiple different SVPWM techniques which will be briefly reviewed in the next chapter.

Chapter 5

Experimental Implementation and Validation of Dual Three-Phase Modulation Schemes

5.1 Introduction

With multiple different modulation schemes discussed throughout this thesis, although an experimental setup has not been constructed to carry out high-power testing, implementation to the DSP can still be considered using a temporary low power test setup. As this is only a temporary setup, the experimental test bench does not have a dynamometer or cooling system so only low load operating points have been considered. Moreover, the physical controller of this experimental setup is developed similar to the Simulink drive model where d and q axis current values are used as direct inputs. This means that the physical test setup does not operate with speed control and since no load or brake is attached, the input d and q axis

must slowly be increased to allow for the rotational speed of the machine's rotor to stabilize. Starting from zero and slowly increasing, the d and q axis currents cannot surpass $-0.05pu$ and $0.005pu$, respectively for safety reasons as this operating point settles at a rotational speed of 585 rpm.

With preliminary testing of the 100 kW dual three-phase drive system being conducted at these very low load operating points, an additional validation process of the proposed Simulink drive model can be completed by comparing the phase current waveforms generated by the simulation results and experimental results. Additionally, the initial programming of the controller and the considerations that have been made for the dual three-phase system will be discussed throughout this chapter. The experimental setup that was used for the validation of the Simulink drive model can be seen in Figure 5.1 where this setup utilizes a Texas Instruments TMS320F28377D dual-core microcontroller which is attached to a custom-built control board. This control board handles all signal conditioning between the DSP and the mechanical components so that the suitable signals at the correct voltages are input and output for the DSP. For example, some of the most important signals generated by the DSP are the PWM signals for each switch of the VSI which then require signal conditioning and voltage division circuits to be applied to the gate driver of the IGBT module directly. Note that the experimental setup also utilizes an interface printed circuit board (PCB) which can also be seen in Figure 5.1 where the PWM signals for each switch are distributed to their respective phase leg gate driver.

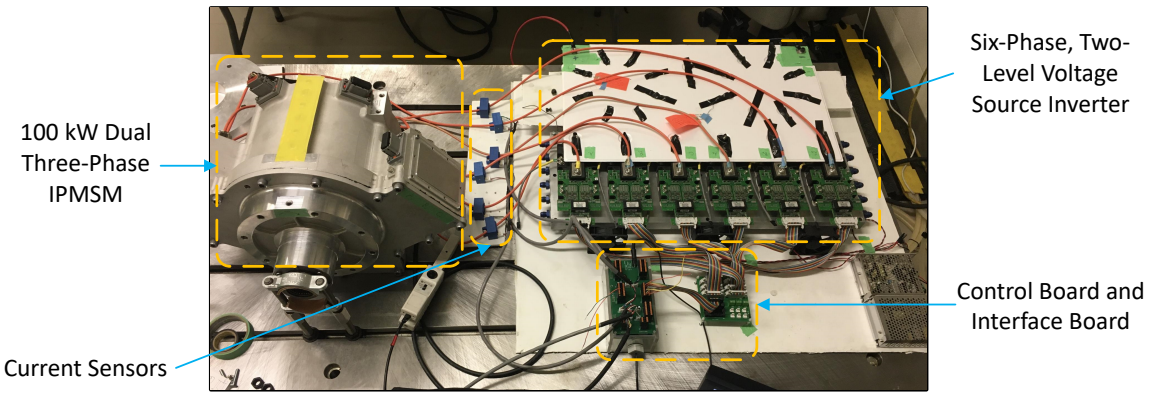


Figure 5.1: Preliminary Experimental Setup of 100 kW Dual Three-Phase Drive System for Low-Power Testing

The PWM signals that are applied to the VSI are first generated in the DSP and can be programmed in different ways to meet the needs of the different switching techniques that are applied. Although only experimental results using DZSI SPWM switching were obtained due to the limitations of the experimental setup, the programming of the DSP and the software changes made to the PWM drivers for the use of different switching techniques can also be further discussed. These necessary changes come from the concept that some of the switching techniques discussed and proposed in this thesis do not have symmetrical dwell times in each sample period. This will be more clearly explained in the following sections where the implementation of the DZSI SPWM switching technique to the DSP, which does have symmetrical switching, is first discussed. After providing details on how the DZSI SPWM technique can be implemented to the DSP, the validation of the Simulink drive model is further proven by utilizing this implementation strategy on the low-power preliminary experimental setup in Figure 5.1. This discussion is followed by an alternate method of implementing asymmetrical PWM signals to the experimental setup which is a task that is planned for the future work of this thesis.

5.2 Symmetrical PWM Signal DSP Implementation

The development of the controller for the dual three-phase drive system originated from an existing three-phase drive system set up where the initialization for all components such as the analog to digital converters (ADC), the resolver, and the current sensors had already been completed. Therefore, most of the significant modifications that need to be made when going from the three-phase to dual three-phase system in terms of the controller programming are mostly inside the current control function. Most importantly, the dual three-phase Clarke and Park transformations for the current signals must be properly defined using the feedback current from the calibrated current sensors as the input. The physical controller then works similarly to the block diagrams in Figures 2.6 and 2.7 with the exception that PR controllers have not yet been implemented to the physical controller. Therefore, the experimental results that have been gathered and shown in this thesis do not control the xy subspace which leads to increased THD on the phase current waveform. However, as proven throughout this thesis, the use of PR controllers can improve the quality of the phase current waveforms leading to better motor performance.

Shifting the focus to the generation of the PWM signals that are produced, it is important to acknowledge that the common method of generating the gate pulses for each switch of the VSI that is used for DZSI SPWM switching cannot be utilized in the same way for some of the SVPWM techniques discussed in this thesis. First, concentrating on techniques such as the DZSI SPWM, C24-2L1ML1M1Z, D24-3L1M1Z, D24-3L2M1Z, and SVPWM1, which can be classified as algorithms that calculate

symmetrical PWM signals, it should be noted that only the turn-on time of each switch needs to be calculated assuming that a triangular counter waveform is being used. Using DZSI SPWM switching as the primary example since this technique has been experimentally validated, at each sample point every 50 μs, a duty cycle is calculated between -1 and 1 based on the ratio of the per-unit phase voltage value and half of the normalized DC link voltage. Note that the controller is programmed so that a duty cycle of -1 represents the top switch being closed for an entire sample period and 1 represents the bottom switch being closed for an entire sample period. For example, if the value of the phase A_1 voltage at a specific sample point is $-0.25pu$ relative to the rated voltage of the machine, the ratio, which is equal to the duty cycle, is calculated to be -0.5. Based on the range of specified duty cycles in the controller, this value corresponds to a dwell time where the top switch is closed for 75% of the sample period and open for the remaining 25% for the phase A_1 inverter leg. This same calculation is completed for each phase leg of the inverter in each sample period.

With the defined concept of the duty cycle generated for the DZSI SPWM technique, the PWM driver for these symmetrical PWM signals is initialized as an up/down counter that resets every 20000 clock cycles which will be referred to as PRD. Note that one clock cycle is set to 2.5 MHz which is easily handled by the DSP as seen in the datasheet where each core of the DSP can provide up to 200 MHz of signal processing performance [85]. Furthermore, in the manual of the DSP, the concept of initializing the PWM driver as an up/down counter is discussed in detail which is what is used for the implementation of the symmetrical PWM signals [86]. The method used for generating the PWM signals requires a parameter that is half of PRD to be initialized which will be referred to as PRD_{Half} and is equal to 10000

clock cycles. The PRD_{Half} parameter is then used with the duty cycle that is calculated for the respective phase to determine a *Compare* value that resembles the turn-on or turn-off time of the top switch for the corresponding phase leg. It should be noted that since the PWM signal is symmetric within the sample period, the calculation for only one *Compare* value is required and this is referred to as $CMPA$ within the DSP. The $CMPA$ value for phase A_1 is determined using (5.1) and can be applied for each phase leg of the VSI.

$$CMPA_{A1} = \left(\frac{1}{2}PRD_{Half} * Duty\ Cycle_{A1}\right) + \frac{1}{2}PRD_{Half} \tag{5.1}$$

Recall the sample point where the phase A_1 voltage was calculated to be $-0.25pu$ which corresponds to a duty cycle of -0.5, using (5.1), the $CMPA$ variable for phase A_1 is calculated to be equal to 2500 clock cycles. Since this PWM method is symmetrical, as the clock cycle approaches the PRD_{Half} value, the up/down counter is increasing where it peaks at PRD_{Half} which is halfway through the sample period and the counter then decreases back down to zero which occurs at the end of the sample period. In the case where the duty cycle is -0.5, when the value of the up/down counter reaches 2500 while increasing, the EPWM1 register of the DSP, $EPWM1Regs$, flips from "0" to "1". This is the signal that is sent to the gate driver of the VSI phase leg where a "1" corresponds to the top switch being closed and the bottom switch being open and vice versa when the value is "0". The $EPWM1Regs$ value, which is assigned to phase A_1, then remains at the on-state while the up/down counter increases past PRD_{Half} and starts to decrease. As this value now decreases, when the counter reaches the $CMPA$ value on the descent, the $EPWM1Regs$ value flips to "0" which turns the top switch of the phase leg off and closes the bottom

switch. It is important to note that the EPWM1 register of the DSP can generate two PWM waveforms, A and B, but due to the two switches of each phase leg being complimentary, only one of these waveforms is needed which simplifies the initialization of the PWM driver. The process of applying a PWM signal to phase A_1 can be seen in Figure 5.2 for a duty cycle of -0.5 in the first sample period of the figure.

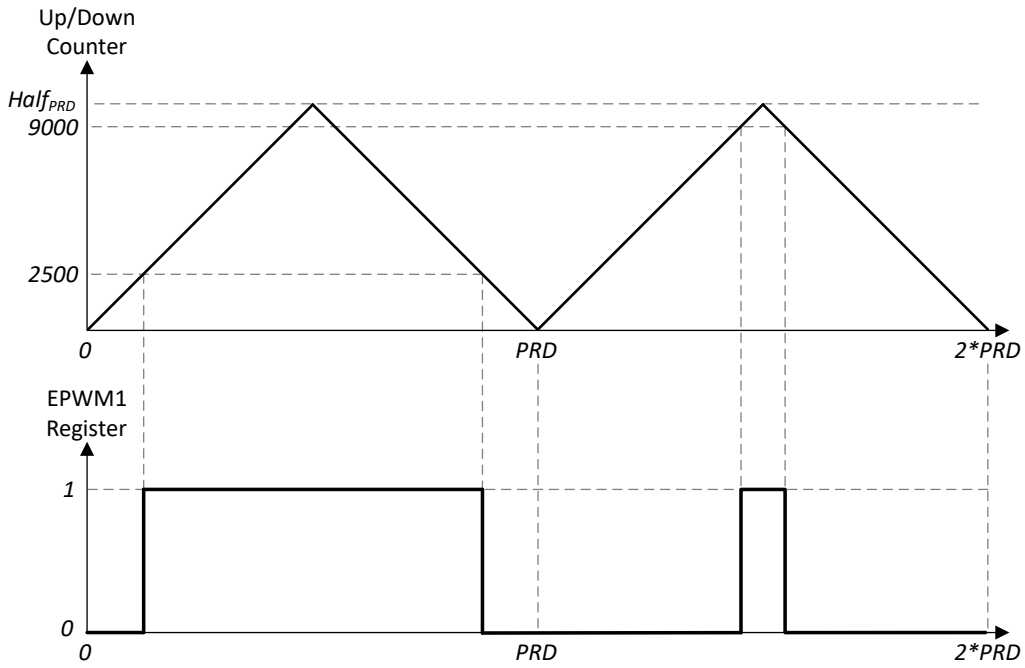


Figure 5.2: Symmetrical PWM Signal Implementation Using a DSP

In Figure 5.2, for a better understanding of the process of generating the PWM signal, it is also considered that after one sample period, the value of the phase A_1 voltage is now $0.4pu$ which corresponds to a duty cycle of 0.8. Then using (5.1) the $CMPA_{A1}$ value is calculated to be 9000 clock cycles. This sample point that is shown between sample times of PRD and $2 * PRD$ in Figure 5.2 verifies that a duty cycle of 1 would result in the bottom switch being closed and the top switch being open and a duty cycle of -1 would result in the opposite.

As the previous discussion focused on the implementation of DZSI SPWM, the same PWM initialization and generation of signals can be used for SVPWM techniques that have symmetrical dwell-time calculations. For example, the SVPWM1 technique which would implement the dwell time calculation in (2.9) using the DSP would only need the turn-on time of each switch to be calculated due to the symmetry of how each voltage vector from this technique is applied. This phenomenon can be seen in Table 5.1 where the application of each voltage vector and the corresponding dwell times using SVPWM1 for sector 11 can be observed for each time segment of the algorithm.

Table 5.1: Assigned Dwell Times for the Proposed SVPWM1 Switching Pattern for Sector 11

	Sector 11								
Binary # **MSB**	0	0	0	0	0	0	0	0	0
	0	0	1	1	1	1	1	0	0
	0	0	0	1	1	1	0	0	0
	0	0	0	0	0	0	0	0	0
	0	1	1	1	1	1	1	1	0
LSB	0	0	0	0	1	0	0	0	0
Decimal #	**00**	02	18	26	27	26	18	02	**00**
Dwell Times	$T_0/2$	$T_1/2$	$T_2/2$	$T_3/2$	T_4	$T_3/2$	$T_2/2$	$T_1/2$	$T_0/2$
	$T_s = T_1 + T_2 + T_3 + T_4 + T_0$								

From Table 5.1, it can be seen that for the switches that do turn on in the sample period, the summation of the dwell times at the beginning of the sample period before a change in the switching state is equal to the summation of the dwell times at the end of the sample period when returning to the original switching state. For example, from Table 5.1 in sector 11, the phase B_1 leg of the inverter is "0" for a total time of $\frac{T_0}{2} + \frac{T_1}{2}$ and then switches to "1" where the top switch of the inverter phase leg would be closed. The switching state then returns to "0" when there is a time of $\frac{T_0}{2} + \frac{T_1}{2}$ remaining in the sample period. Therefore, the $CMPA$ value that was previously

used for DZSI SPWM would now be calculated for phase B_1 in sector 11 using (5.2).

$$CMPA_{B1} = \left(\frac{T_0}{2} + \frac{T_1}{2}\right) PRD^2 \tag{5.2}$$

As all switches for each sector have this same symmetrical characteristic, the up/down counter can be used for all of these techniques. This allows for the same $CMPA$ value that is used to change the bit of the EPWM register inside the DSP when the counter is increasing to also be used when the counter is decreasing. It should be noted that there are not generalized equations for the dwell time calculations of each sector similar to three-phase SVPWM. Therefore, there is an increased computational burden when implementing SVPWM on the dual three-phase machine as each $CMPA$ value for each phase leg has to be calculated within each sector. This is due to the irregular pattern of the resultant voltage vectors of the xy subspace for the chosen voltage vectors of the $\alpha\beta$ subspace. For this reason, in the literature, offline dwell time calculations have been proposed to lower the computation time within the DSP where this was first proposed in [54]. Additionally, since the zero vector is sometimes changing when the sectors change, initialization of the EPWM registers can be coded in each sector to set the register as "active high" or "active low" depending on whether the switching algorithm starts with a "1" or a "0".

5.3 Dual Three-Phase Drive Simulink Model Experimental Validation

With a detailed understanding of how symmetrical PWM signals can be experimentally implemented, an additional verification process can be completed to further validate the accuracy of the Simulink drive model from Chapter 3. As the Simulink model discussed is physically constructed using the 100 kW dual three-phase motor and a six-phase, two-level voltage source inverter made up of six Infineon FF600R12IE4 modules seen in Figure 5.1, only preliminary experimental results can be obtained due to limitations on the experimental test bench. For this reason, as previously mentioned, experimental results have only been obtained for a very low load operating point as there is currently no dynamometer or cooling set up to increase the load of this system. It is important to note that these tasks are to be completed in the future work of this thesis. Therefore, with the limitations of the experimental setup, closed-loop current control can be implemented using a low load operating point of $I_d = -0.05pu$ and $I_q = 0.005pu$ relative to the rated current of the machine. The operating point is very low because the rotor of the machine is freely spinning since it is not connected to any load and speed control is not implemented. This results in an experimental set up that is very similar to the Simulink drive model that has been developed throughout this chapter where d and q axis current values are directly input as the reference values to the DSP. To properly validate the Simulink model, the DZSI SPWM implementation method discussed in the previous section is applied to the experimental setup and also used to obtain the simulation results.

When running the experimental setup at a low load operating point with no speed

control and no braking system, recall that the d and q axis currents must slowly be increased in small intervals starting from zero to allow the resultant rotational speed to stabilize at a safe operating condition. This is the reason why the d and q axis currents did not surpass $-0.05pu$ and $0.005pu$, respectively, where the rotational speed of the motor settles at an average speed of $585rpm$. Additionally, for safety reasons, a lower DC voltage of $0.14pu$ relative to the rated voltage of the motor is used for obtaining preliminary experimental results using the setup that was seen in Figure 5.1. As the controller in the setup works to maintain the d and q axis current values that have been set, the current sensors seen in Figure 5.1 provide current feedback for closed-loop current control to properly function for this dual three-phase drive system. As this process matches the Simulink drive model process that has been discussed in Chapter 3, the simulation environment can easily replicate the preliminary experimental setup in Figure 5.1.

With the limitations of the experimental setup that have been discussed, experimental results have only been obtained for a single operating point which can also be recreated in the simulation environment. As modifications are made to the Simulink drive model to accommodate for the lower DC voltage of $0.14pu$, other important characteristics of the experimental test bench to consider in the simulation environment include a switching and sampling frequency of 20 kHz, d and q axis reference currents of $-0.05pu$ and $0.005pu$ respectively, and a constant speed of $585rpm$. Although it is only a low operating point that can be used for experimental validation of the proposed Simulink drive model, Figures 5.3 and 5.4 show the comparison between experimental and simulation results for the resultant phase A_1 current and stationary frame x axis current, respectively.

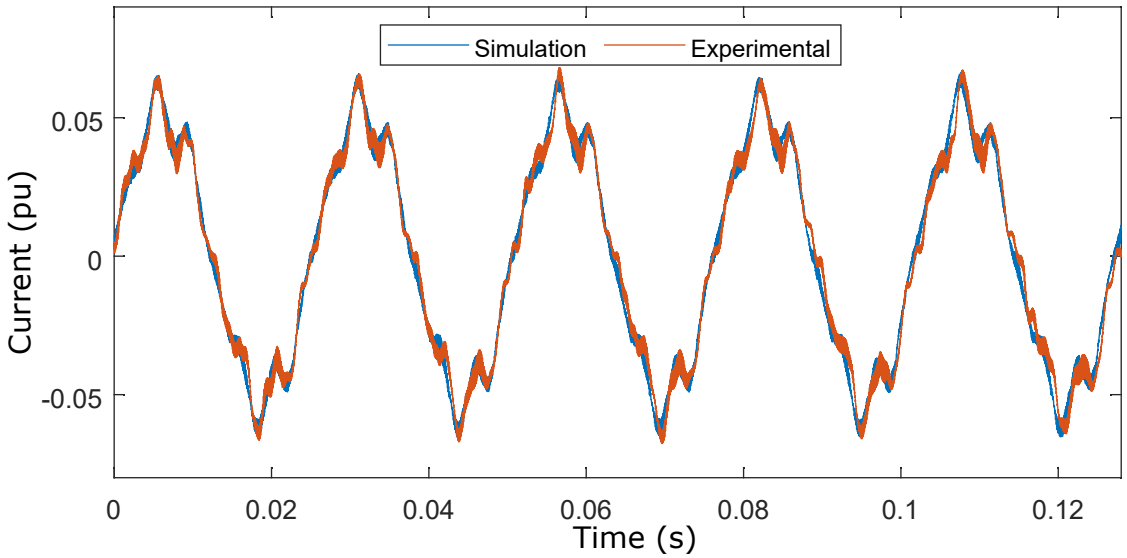


Figure 5.3: Comparison of Phase A_1 Current Waveforms for Experimental Validation of Proposed Modelling Strategy

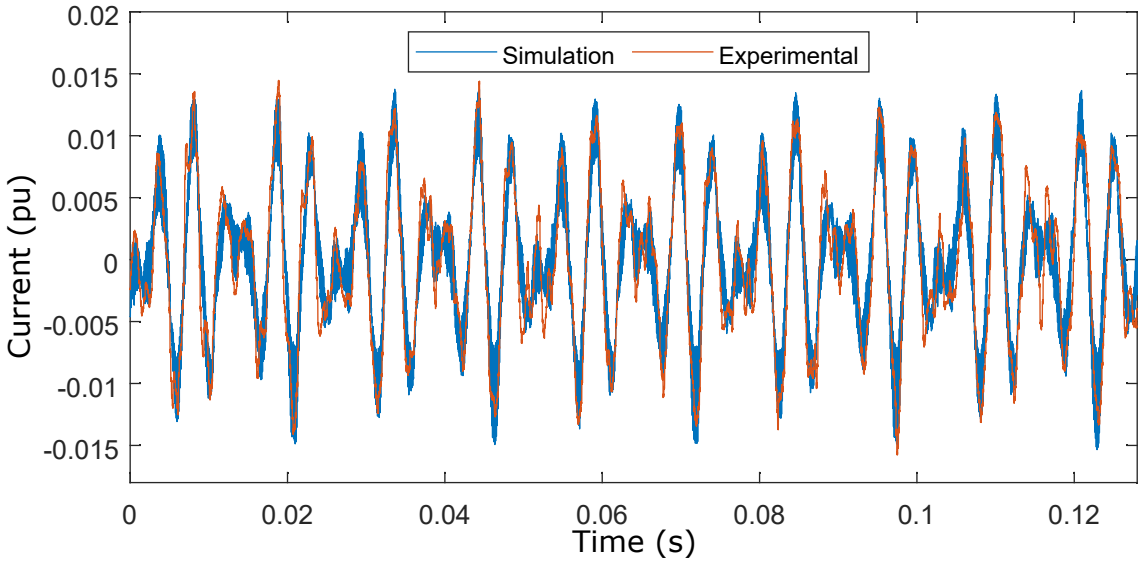


Figure 5.4: Comparison of Stationary Frame x-axis Current Waveforms for Experimental Validation of Proposed Modelling Strategy

From Figures 5.3 and 5.4, it can be seen that there is a small error present between the simulation and experimental waveforms. It is important to recognize that this error is due to the very low operating point being tested. With the d and q axis current values being a very small fraction of the rated current of the machine, and the current sensors being rated for two times the rated current of the machine, the tolerance of the current sensors is actually larger than the q axis reference current value being tested. Unfortunately, as this noise from the current sensor results in random fluctuations on the feedback phase current, this phenomenon is difficult to recreate in the simulation environment and is therefore ignored leading to a small error between the waveforms seen in Figures 5.3 and 5.4. However, it is important to acknowledge that given this source of error, the waveforms for both the phase A_1 current and stationary frame x axis current match very closely and the accuracy between the simulation and experimental results is only expected to improve as the load of the system increases. It is also important to note that the dominant harmonics that lead to the distortion of the phase currents in Figure 5.3 are the same in both waveforms which shows promising results supporting the accuracy of the Simulink drive model. This is further verified in Figure 5.4 where, again, a small error exists between the experimental and simulation results of the stationary frame x axis current, but the dominant harmonics of both waveforms are the same which validates that the proposed method of modelling the x and y subspace is accurate. Note that the stationary frame x axis current is shown where the dominant harmonics based on the aforementioned dual three-phase Clarke transformation are of the order $6n \pm 1$ ($n = 1,3,5,\dots$).

5.4 Asymmetrical PWM Signal DSP Implementation

Now shifting the focus to asymmetrical PWM signal implementation, these techniques, such as C12-4L1Z, C12-2L2ML1Z, and SVPWM2 have different turn-on and turn-off times, making the computation of the dwell times within the DSP more difficult. As the different turn-on and turn-off times result in asymmetrical PWM signals, an additional *Compare* value must be calculated for these switching techniques. Recall that the *Compare* value used for the symmetrical PWM signals was referred to as $CMPA$ within the DSP and now to properly implement asymmetrical PWM signals, a second Compare value referred to as $CMPB$ in the DSP is also required. Looking deeper into the initialization code of the PWM driver for the DSP, specifically for phase A_1, the EPWM1 register is initialized as being "clear" or in other words, the bottom switch is closed. The EPWM1 register bit is then "set" when the value of the increasing counter is equal to the $CMPA$ value. The EPWM1 register remains "set", or with the top switch closed, until the value of the counter is equal to the value of $CMPB$ where the EPWM1 register bit is then reset to be "clear".

From the manual of the DSP, it is shown that this technique can be used for any of the three main counter waveforms that this DSP can generate including the up/down, up, and down counters. As the up/down counter that was previously used for symmetrical PWM generation only allows for the $CMPB$ bit to be used on the back half of the sample period as the counter is decreasing, this thesis proposes using the up counter for asymmetrical PWM waveforms. This allows for the PWM signal to be set over a wider range of the given sample period. Therefore, the PWM driver

is initialized with an up counter that counts up to the value of PRD which remains as 20000 clock cycles. The up counter reaches the PRD value at the end of a sample period and then resets back to zero. This up counter is then compared to the $CMPA$ values and $CMPB$ values of each respective phase leg to determine when to "set" the EPWM registers and when to "clear" the registers.

To develop a better understanding of the implementation of asymmetrical PWM waveform generation using the up counter of the DSP, the proposed SVPWM2 technique which was shown to have improved inverter efficiency while maintaining low phase current THD can be analyzed. The asymmetrical characteristics of this switching pattern can be seen in Table 5.2 where the application of each voltage vector and the corresponding dwell times for sector 7 can be observed for each of the 6-time segments of the algorithm.

Table 5.2: Assigned Dwell Times for the Proposed SVPWM2 Switching Pattern for Sector 7

		Sector 7					
Binary #	**MSB**	0	0	0	0	0	0
		0	0	0	1	1	0
		0	1	1	1	1	0
		0	0	0	0	0	0
		0	1	1	1	0	0
	LSB	0	0	1	1	1	0
Decimal #		**00**	10	11	27	25	**00**
Dwell Times		$T_0/2$	T_1	T_2	T_3	T_4	$T_0/2$
		$T_s = T_1 + T_2 + T_3 + T_4 + T_0$					

From Table 5.1, when looking specifically into the B_1 phase leg, it can be observed that the summation of the dwell times before the switching state changes at the beginning of the sample period is not equal to the summation of the times at the end of the sample period after the switching state has returned to the original value. This can be seen in sector 7 of the SVPWM2 algorithm when the B_1 phase leg is "0" for

a total time of $\frac{T_0}{2} + T_1 + T_2$ before switching to "1". Then, at the end of the sample period, the phase leg returns to "0" only for a time of $\frac{T_0}{2}$. Therefore, these values can be used to set the $CMPA$ and $CMPB$ values of the B_1 phase leg using (5.3). Furthermore, modifications of (5.3) can be implemented for each phase leg of each sector to obtain the PWM waveforms for each switch of the VSI.

$$CMPA_{B1} = \left(\frac{T_0}{2} + T_1 + T_2\right) PRD^2 \tag{5.3a}$$

$$CMPB_{B1} = \left(T_s - \frac{T_0}{2}\right) PRD^2 \tag{5.3b}$$

Recall that PRD is the number of clock cycles in one sample period which is 20000, and T_s is the sample time of 50 μs. Again, it should be acknowledged that due to the irregular pattern of the resultant xy vectors, a set of generalized equations for the dwell time calculations can not be defined which increases the computational burden. Moreover, since the asymmetrical techniques require a $CMPA$ and $CMPB$ value to be calculated, the computational burden of asymmetrical PWM generation is even greater compared to the aforementioned generation of symmetrical PWM waveforms.

To obtain a visual representation of the asymmetric PWM signals, it will be assumed that the $CMPA_{B1}$ value from (5.3) is calculated to be 11000 clock cycles and $CMPB_{B1}$ is calculated to be 17000 clock cycles. With the method used for the initialization of the PWM driver, Figure 5.5 displays the resultant up counter and EPWM register bit that corresponds to phase B_1 as it changes between "0" and "1" for the defined values of $CMPA$ and $CMPB$ in the first sample period. For a better understanding of the process of generating the asymmetric PWM signal,

an additional example is provided where it is assumed that at the PRD sampling point in Figure 5.1, the $CMPA_{B1}$ value is calculated to be 5000 clock cycles and the $CMPB_{B1}$ value is calculated to be 12500 clock cycles and these values are applied to the second sampling period of the figure.

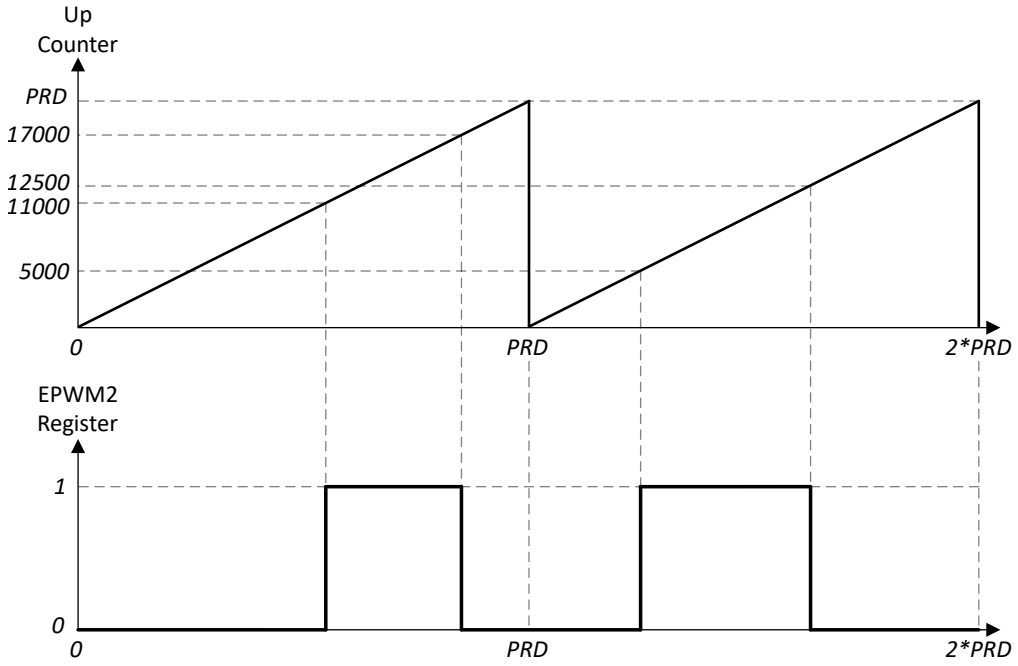


Figure 5.5: Asymmetrical PWM Signal Implementation Using a DSP

As Figure 5.5 shows the ability for this PWM driver to implement asymmetrical PWM signals for the switches of the VSI, it is also possible to reverse the initialization process if any switches require to start with the top switch being closed and bottom switch open, which is the case for techniques that utilize the redundant zero vectors. Additionally, as both the generation of symmetrical and asymmetrical PWM signals require increased computation time compared to three-phase control techniques or DZSI SPWM, future work intends to further explore how this can be minimized when implementing these methods to a high-power setup.

Chapter 6

Conclusion

As this thesis had the main focus of improving the overall efficiency of dual three-phase drive systems specifically through improving the efficiency of six-phase, two-level voltage source inverters, many of the different concepts of multiphase machines are reviewed. Throughout this research, the main emphasis is on dual three-phase machines which have been proven to have increased benefits compared to other multi-phase machines and even better performance than other six-phase machine topologies. The characteristics of the dual three-phase machines are discussed in detail to provide base knowledge for a conversation on the control of these machines and how the system efficiency can be improved through further developing modulation and control techniques. With this base knowledge provided, an in-depth literature review on the different modulation techniques including carrier-based sinusoidal PWM and space vector PWM techniques is provided and compared. As these techniques are intended to be implemented using a high-power experimental setup, only modulation techniques where the sampling frequency is equal to the switching frequency are discussed for the sake of easier implementation and reduced computation time.

With an in-depth literature review covering the existing switching techniques, a detailed drive system model has also been developed with a proposed method for specifically modelling multiphase machines using the Vector Space Decomposition transformation. The drive system model is developed in the Matlab/Simulink environment as a flux linkage, lookup table based model using FEA data collected by sweeping through every possible current magnitude and phase angle. This allows for all nonlinearities of the machine such as the effects of spatial harmonics, cross-coupling, and magnetic saturation to be modelled in the Simulink environment in a fraction of the time. The other significant contribution from the multiphase model discussed is the idea that the dynamic behaviour of the motor from FEA will also incorporate high-frequency current ripple that is generated from the switching instances of the inverter. With this accurate motor model, the drive system model is further developed with a properly sampled controller model and an accurate inverter model that calculates the power losses of the power electronic components using the PLECS by Plexim Simulink toolbox. Along with validating the Simulink drive model using FEA results, the model is also validated for a very low load operating point that has been experimentally obtained.

With an accurate Simulink model validated through FEA and experimental results, the inverter efficiency and phase current THD results can be calculated from the model for any specified modulation and control techniques. First, a comparison into the inverter efficiency of the existing switching techniques is provided throughout the constant torque region for multiple different speeds as the load torque is swept from $0.1pu$ to $1.0pu$ relative to the rated torque of the machine. As the inverter efficiency comparison provides results on improving the drive system efficiency in regards to the

inverter, the phase current THD of each technique is also analyzed to ensure that for any improvements in the inverter efficiency, the motor performance is not sacrificed and a net gain in the overall drive system efficiency is achievable. Through observing certain patterns and characteristics of the existing switching techniques, specifically using SVPWM, this thesis has proposed two new switching techniques which lead to increased inverter efficiency while maintaining a sampling frequency that is equal to the switching frequency. It is important to note that while the percentage increases in the inverter efficiency seem relatively low throughout this thesis, all simulation results are obtained assuming an environment that would lead to the minimum increase in the inverter efficiency. For example, at a higher junction temperature for each of the devices in the VSI, more losses would be generated which would increase the difference in the efficiency calculations for each technique. Additionally, as recent trends in variable speed drive systems investigate increasing the switching frequency of the system with the use of Silicon Carbide MOSFETs, larger switching losses would be generated and the difference between the switching losses calculated for each technique would increase, once again resulting in larger differences between the VSI efficiency results of all techniques.

The two techniques that have been proposed in this thesis which are referred to as SVPWM1 and SVPWM2 are designed specifically to improve the inverter efficiency by reducing the average switching frequency in one sample period. While the SVPWM1 technique is proven to provide the highest average switching frequency, this is at the expense of worsening the phase current waveform quality which would result in the motor performance being negatively impacted. As a result, the SVPWM2 technique is proposed where a small decrease in the inverter efficiency is seen compared

to SVPWM1, but the phase current THD remains comparable to the existing techniques that are also discussed in this thesis. This allows for the proposed SVPWM2 technique to have increased inverter efficiency without sacrificing the performance of the motor leading to an increase in the overall drive system efficiency. Furthermore, this thesis also explores the implementation of proportional resonant controllers in a Simulink VSD based controller model for the two proposed switching techniques as these PR controllers can lead to improved phase current waveform quality. Additionally, simulation results using the proposed dual three-phase drive system model are provided throughout this thesis using the proposed and existing switching techniques to allow for as accurate of a comparison as possible in terms of inverter efficiency and phase current THD.

Although a high-power experimental setup was not constructed for this research, the DSP implementation of how the different switching techniques can be applied to the experimental setup is also discussed as future work intends to experimentally validate the findings of this thesis. As the Simulink model has proven to be very accurate, it can be assumed that the experimental verification of this work will validate the improved efficiency of the proposed switching techniques, specifically SVPWM2, for dual three-phase drive systems, especially as they become a suitable alternative for their three-phase counterparts.

In conclusion, the multiple contributions that have been made throughout this thesis can be summarized as:

- A detailed dynamic dual three-phase machine model that incorporates high-frequency current ripple generated from the inverter validated using FEA and experimental results. As this model uses lookup tables in Simulink to model

the nonlinear characteristics of the machine obtained from FEA, this Simulink model has been proven to simulate dual three-phase machines as accurate as in FEA but in a fraction of the time.

- An in-depth comparison of existing switching techniques in regards to inverter efficiency and phase current THD. This comparison is made using the proposed Simulink drive system model where the inverter efficiency is calculated based on the switching losses of the power electronic devices inside the inverter, and the phase current THD is calculated for the resultant phase currents of the motor model in Simulink.

- Two proposed space vector PWM switching techniques referred to as SVPWM1 and SVPWM2, which both improve the VSI efficiency, are implemented using the Simulink drive model. The SVPWM1 technique is observed to have an increased risk of lowering the motor performance and therefore, SVPWM2 is proven to be the best all-around technique in terms of improving the inverter efficiency and maintaining a low phase current THD.

6.1 Future Work

When considering the future work that can be done to continue this research, it should be noted first and foremost that this thesis is based around the VSD transformation for both modelling and control techniques. While the modelling techniques proposed in this work have been proven to have better accuracy and easier implementation using the VSD transformation, the switching techniques using a Double dq transformation-based controller can be further investigated and compared to the

switching techniques that have been discussed in this thesis. While the Double dq transformation does not consider as many utilizable voltage vectors, the concepts of three-phase machine control techniques can be carried over to dual three-phase machines and potentially lead to drive system efficiency improvements. However, if the VSD transformation remains the preferred transformation for the controller subsystem, further work into developing a tuning method for the required PR controllers could also lead to improved drive system efficiency.

Sticking with the VSD based controller and SVPWM techniques, future work could also include further investigation into generating switching techniques that have as low of an average switching frequency as possible while using as many time-segments as possible inside one sample period. These characteristics and patterns were discovered to be what led to both improved inverter efficiency and low phase current THD when designing different switching algorithms. Additionally, through further investigation into more switching techniques to improve the inverter efficiency, future work can also include varying the switching frequency to observe the impact that this would have not only on the techniques discussed throughout this thesis but for any new techniques being investigated. Moreover, to provide further comparison into these switching techniques, the DC link capacitor current can also be observed to see if there is any further room for reducing the capacitor size.

As this thesis focuses on the inverter efficiency while also working to maintain good quality phase current waveforms, a detailed analysis of the impact of each switching technique on the motor efficiency can also be calculated. This can most easily be done by taking the generated phase current from the Simulink model and using this as the input to FEA to calculate the motor losses and overall motor efficiency. Then,

with the inverter efficiency and motor efficiency analysis, more concrete conclusions can be made on which techniques lead to improved drive system efficiency.

Lastly, an immediate next step in this research includes the design and construction of a high-power dual three-phase drive system experimental setup to allow for experimental validation of the findings of this research. This requires considerations to be made including an appropriate dynamometer, cooling system, safety system, and supply power system. Additionally, the development of a high-power dual three-phase experimental test bench can further be used to validate the benefits of these multiphase machines as they continue to gain interest in the electric motor market.

References and Bibliography

[1] Z. Liu, Y. Li, and Z. Zheng, "A Review of Drive Techniques for Multiphase Machines," *CES Transactions on Electrical Machines and Systems*, vol. 2, no. 2, pp. 243–251, June 2018.

[2] E. Levi, "Multiphase electric machines for variable-speed applications," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 5, pp. 1893–1909, May 2008.

[3] A. Salem and M. Narimani, "A Review on Multiphase Drives for Automotive Traction Applications," *IEEE Transactions on Transportation Electrification*, vol. 5, no. 4, pp. 1329–1348, Dec. 2019.

[4] D. F. Valencia, J. Taylor, M. Mohamadian, D. Luedtke, A. Emadi, and B. Bilgin, "A Comparative Analysis for Six-Phase Motor Configurations," in *Proc. WCX SAE World Congress Experience*, June 2020.

[5] Y. Zhao and T. A. Lipo, "Space Vector PWM Control of Dual Three-Phase Induction Machine Using Vector Space Decomposition," *IEEE Transactions on Industry Applications*, vol. 31, no. 5, pp. 1100–1109, Oct. 1995.

[6] H. A. Toliyat and H. Xu, "Novel direct torque control (DTC) method for five-phase induction machines," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, Aug. 2000, pp. 162–168.

[7] K. S. Khan, W. M. Arshad, and S. Kanerva, "On performance figures of multiphase machines," in *Proc. IEEE International Conference on Electrical Machines*, Vilamoura, Portugal, Mar. 2008.

[8] E. Levi, R. Bojoi, F. Profumo, H. A. Toliyat, and S. Williamson, "Multiphase induction motor drives - A technology status review," *IET Electric Power Applications*, vol. 1, no. 4, pp. 489–516, July 2007.

[9] R. Bojoi, F. Farina, F. Profumo, and A. Tenconi, "Dual-three phase induction machine drives control - A survey," *IEEJ Transactions on Industry Applications*, vol. 126, no. 4, pp. 420–429, 2006.

[10] E. Levi, N. Bodo, O. Dordevic, and M. Jones, "Recent advances in power electronic converter control for multiphase drive systems," in *Proc. IEEE Workshop on Electrical Machines Design, Control and Diagnosis (WEMDCD)*, Paris, France, June 2013, pp. 158–167.

[11] F. Barrero and M. J. Duran, "Recent advances in the design, modeling, and control of multiphase machines - Part I," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 1, pp. 449–458, Jan. 2016.

[12] M. J. Duran and F. Barrero, "Recent advances in the design, modeling, and control of multiphase machines - Part II," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 1, pp. 459–468, Jan. 2016.

[13] E. Levi, "Advances in converter control and innovative exploitation of additional degrees of freedom for multiphase machines," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 1, pp. 433–448, Jan. 2016.

[14] E. Levi, F. Barrero, and M. J. Duran, "Multiphase machines and drives - Revisited," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 1, pp. 429–432, Jan. 2016.

[15] A. Boglietti, R. Bojoi, A. Cavagnino, and A. Tenconi, "Efficiency Analysis of PWM Inverter Fed Three-Phase and Dual Three-Phase High Frequency Induction Machines for Low/Medium Power Applications," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 5, pp. 2015–2023, May 2008.

[16] M. L. Woldesemayat, H. Lee, S. Won, and K. Nam, "Modeling and Verification of a Six-Phase Interior Permanent Magnet Synchronous Motor," *IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 8661–8671, Oct. 2018.

[17] H. S. Che, E. Levi, M. Jones, W. P. Hew, and N. A. Rahim, "Current Control Methods for an Asymmetrical Six-Phase Induction Motor Drive," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 407–417, Jan. 2014.

[18] M. Zabaleta, E. Levi, and M. Jones, "Modelling approaches for an asymmetrical six-phase machine," in *Proc. IEEE International Symposium on Industrial Electronics (ISIE)*, Santa Clara, CA, Nov. 2016, pp. 173–178.

[19] L. Yuan, S. Chen, K.-y. Wei, and Y. Lin, "Current vector decoupling control for six-phase PM synchronous motor considering harmonic current," in *Proc. IEEE*

Conference on Industrial Electronics and Applications (ICIEA), Wuhan, China, June 2018, pp. 2565–2568.

[20] J. Karttunen, S. Kallio, P. Peltoniemi, P. Silventoinen, and O. Pyrhonen, "Decoupled Vector Control Scheme for Dual Three-Phase Permanent Magnet Synchronous Machines," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 5, pp. 2185–2196, May 2014.

[21] S. Kallio, M. Andriollo, A. Tortella, and J. Karttunen, "Decoupled d-q Model of Double-Star Interior-Permanent-Magnet Synchronous Machines," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 6, pp. 2486–2494, June 2013.

[22] M. Andriollo, G. Bettanini, G. Martinelli, A. Morini, and A. Tortella, "Analysis of Double-Star Permanent-Magnet Synchronous Generators by a General Decoupled d-q Model," *IEEE Transactions on Industry Applications*, vol. 45, no. 4, pp. 1416–1424, July 2009.

[23] Y. Hu, Z. Q. Zhu, and K. Liu, "Current Control for Dual Three-Phase Permanent Magnet Synchronous Motors Accounting for Current Unbalance and Harmonics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 2, pp. 272–284, June 2014.

[24] T. Zhao, Y. Zhang, H. Xu, X. Gui, and D. Xu, "DTP-PMSM Drive with Proportional Resonant Regulator and Dual Zero Injection PWM Control Method," in *Proc. IEEE International Conference on Electrical Machines and Systems (ICEMS)*, Jeju, South Korea, Nov. 2018, pp. 1628–1633.

[25] A. R. Bakhshai, G. Joos, and H. Jin, "Space Vector PWM Control of a Split-Phase Induction Machine Using The Vector Classification Technique," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, Feb. 1998, pp. 802–808.

[26] A. R. Bakhshai, G. Joós, P. K. Jain, and H. Jin, "Incorporating the overmodulation range in space vector pattern generators using a classification algorithm," *IEEE Transactions on Power Electronics*, vol. 15, no. 1, pp. 83–91, Jan. 2000.

[27] D. Yazdani, S. Ali Khajehoddin, A. Bakhshai, and G. Joós, "Full Utilization of the Inverter in Split-Phase Drives by Means of a Dual Three-Phase Space Vector Classification Algorithm," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 1, pp. 120–129, Jan. 2009.

[28] R. Bojoi, A. Tenconi, F. Profumo, and D. Martinello, "Complete Analysis and Comparative Study of Digital Modulation Techniques for Dual Three-phase AC Motor Drives," in *Proc. IEEE Power Electronics Specialists Conference*, Cairns, Australia, Nov. 2002, pp. 851–857.

[29] K. A. Chinmaya and G. K. Singh, "Experimental analysis of various space vector pulse width modulation (SVPWM) techniques for dual three-phase induction motor drive," *International Transactions on Electrical Energy Systems*, vol. 29, June 2018.

[30] O. Dordevic, M. Jones, and E. Levi, "A Comparison of Carrier-Based and Space Vector PWM Techniques for Three-Level Five-Phase Voltage Source Inverters," *IEEE Transactions on Industrial Informatics*, vol. 9, no. 2, pp. 609–618, May 2013.

[31] O. Ojo and G. Dong, "Generalized discontinuous carrier-based PWM modulation scheme for multi-phase converter-machine systems," in *Proc. IEEE Industry Applications Society (IAS) Annual Meeting*, Kowloon, Hong Kong, Oct. 2005, pp. 1374–1381.

[32] A. Boglietti, R. Bojoi, A. Cavagnino, and A. Tenconi, "Efficiency Analysis of PWM Inverter Fed Three-Phase and Dual Three-Phase Induction Machines," in *Proc. IEEE Industry Applications Society (IAS) Annual Meeting*, Tampa, FL, Dec. 2006, pp. 434–440.

[33] A. Iqbal, E. Levi, M. Jones, and S. N. Vukosavic, "Generalised sinusoidal PWM with harmonic injection for multi-phase VSIs," in *Proc. IEEE Power Electronics Specialists Conference (PESC)*, Jeju, South Korea, May 2006.

[34] L. Zarri, M. Mengoni, A. Tani, G. Serra, and D. Casadei, "Minimization of the Power Losses in IGBT Multiphase Inverters with Carrier-Based Pulsewidth Modulation," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 11, pp. 3695–3706, Nov. 2010.

[35] J. Prieto, E. Levi, F. Barrero, and S. Toral, "Output current ripple analysis for asymmetrical six-phase drives using double zero-sequence injection PWM," in *Proc. IEEE Industrial Electronics Society Annual Conference (IECON)*, Melbourne, Australia, Jan. 2011, pp. 3692–3697.

[36] P. R. Rakesh and G. Narayanan, "Analysis of sine-triangle and zero-sequence injection modulation schemes for split-phase induction motor drive," *IET Power Electronics*, vol. 9, no. 2, pp. 344–355, Feb. 2016.

[37] P. R. Rakesh and G. Narayanan, "Investigation on zero-sequence signal injection for improved harmonic performance in split-phase induction motor drives," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 2732–2741, April 2017.

[38] M. J. Duran and E. Levi, "Multi-Dimensional Approach to Multi-Phase Space Vector Pulse Width Modulation," in *Proc. IEEE Industrial Electronics Society Annual Conference (IECON)*, Paris, France, 2006, pp. 2103–2108.

[39] D. Hadiouche, H. Razik, and A. Rezzoug, "Study and simulation of space vector PWM control of Double-Star Induction Motors," in *Proc. IEEE International Power Electronics Congress*, Acapulco, Mexico, Oct. 2000, pp. 42–47.

[40] H. A. Toliyat, R. Shi, and H. Xu, "DSP-based vector control of five-phase synchronous reluctance motor," in *Proc. IEEE Industry Applications Society (IAS) Annual Meeting*, Rome, Italy, Oct. 2000, pp. 1759–1765.

[41] J. W. Kelly, E. G. Strangas, and J. M. Miller, "Multi-phase inverter analysis," in *Proc. IEEE International Electric Machines and Drives Conference (IEMDC)*, Cambridge, MA, June 2001, pp. 147–155.

[42] J. W. Kelly, E. G. Strangas, and J. M. Miller, "Multiphase space vector pulse width modulation," *IEEE Transactions on Energy Conversion*, vol. 18, no. 2, pp. 259–264, June 2003.

[43] M. J. Duran, F. Barrero, and S. Toral, "Multi-phase space vector pulse width modulation: Applications and strategies," *Renewable Energy and Power Quality Journal*, vol. 1, no. 5, pp. 580–586, March 2007.

[44] H. M. Ryu, J. H. Kim, and S. K. Sul, "Analysis of multiphase space vector pulse-width modulation based on multiple d-q spaces concept," *IEEE Transactions on Power Electronics*, vol. 20, no. 6, pp. 1364–1371, Nov. 2005.

[45] D. Dujic, A. Iqbal, and E. Levi, "A space vector PWM technique for symmetrical six-phase voltage source inverters," *European Power Electronics and Drives (EPE) Journal*, vol. 17, no. 1, pp. 24–32, 2007.

[46] E. A. R. B. E. Ariff and O. Dordevic, "Space vector PWM technique for a two-level asymmetrical six-phase drive," *The Journal of Engineering (IET)*, vol. 17, pp. 3878–3883, June 2019.

[47] Y. He, Y. Wang, J. Wu, Y. Feng, and J. Liu, "A comparative study of space vector PWM strategy for dual three-phase permanent-magnet synchronous motor drives," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Palm Springs, CA, Feb. 2010, pp. 915–919.

[48] J. Prieto, F. Barrero, M. J. Durán, S. Toral Marín, and M. A. Perales, "SVM Procedure for n-phase VSI with Low Harmonic Distortion in the Overmodulation Region," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 1, pp. 92–97, Jan. 2014.

[49] C. Zhou, G. Yang, and J. Su, "PWM Strategy with Minimum Harmonic Distortion for Dual Three-Phase Permanent-Magnet Synchronous Motor Drives Operating in the Overmodulation Region," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1367–1380, Feb. 2016.

[50] P. Wu, L. Yuan, Z. Zuo, and J. Wei, "Vector Weighting Approach and Vector Space Decoupling Transform in a Novel SVPWM Algorithm for Six-Phase Voltage Source Inverter," *Hindawi Mathematical Problems in Engineering*, vol. 5, Jun. 2019.

[51] D. Hadiouche, L. Baghli, and A. Rezzoug, "Space-vector PWM techniques for dual three-phase ac machine: Analysis, performance evaluation, and DSP implementation," *IEEE Transactions on Industry Applications*, vol. 42, no. 4, pp. 1112–1122, July 2006.

[52] K. Marouani, L. Baghli, D. Hadiouche, A. Kheloui, and A. Rezzoug, "Discontinuous SVPWM Techniques for Double Star Induction Motor Drive Control," in *Proc. IEEE Industrial Electronics Society Annual Conference (IECON)*, Paris, France, Nov. 2006, pp. 902–907.

[53] J. Prieto, F. Barrero, M. Jones, and E. Levi, "A modified continuous PWM technique for asymmetrical six-phase induction machines," in *Proc. IEEE International Conference on Industrial Technology*, Vina del Mar, Chile, March 2010, pp. 1489–1494.

[54] K. Marouani, L. Baghli, D. Hadiouche, A. Kheloui, and A. Rezzoug, "A New PWM Strategy Based on a 24-Sector Vector Space Decomposition for a Six-Phase VSI-Fed Dual Stator Induction Motor," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 5, pp. 1910–1920, May 2008.

[55] Y. Yu, L. Gao, Y. Liu, and F. Chai, "24-Sector space vector decomposition for a dual three-phase PMSM," in *Proc. IEEE International Conference on Electrical Machines and Systems (ICEMS)*, Hangzhou, China, Oct. 2014, pp. 1601–1606.

[56] C. Wang, K. Wang, and X. You, "Research on Synchronized SVPWM Strategies Under Low Switching Frequency for Six-Phase VSI-Fed Asymmetrical Dual Stator Induction Machines," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 3883–3891, Nov. 2016.

[57] J. Prieto, J. A. Riveros, and B. Bogado, "Continuous and Discontinuous SVPWM 2L+2M for Asymmetrical Dual Three-Phase Drives," in *Proc. IEEE International Electric Machines and Drives Conference (IEMDC)*, Miami, FL, May 2017.

[58] J. A. Riveros, J. Prieto, and H. Guzman, "Multifrequency Space Vector Pulse Width Modulation for Asymmetrical Six-Phase Drives," in *Proc. IEEE International Symposium on Industrial Electronics (ISIE)*, Edinburgh, UK, June 2017.

[59] J.-H. Baik, S.-W. Yun, and J.-Y. Yoo, "A New Active Zero State PWM for Six-Phase Inverter," in *Proc. IEEE International Conference on Power Electronics (ICPE)*, Busan, South Korea, May 2019.

[60] S. M. Suhel and R. Maurya, "Realization of 24-Sector SVPWM with New Switching Pattern for Six-Phase Induction Motor Drive," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5079–5092, June 2019.

[61] Y. Li, B. Howey, J. Liang, E. Sayed, A. A. Qazalbash, M. Kasprzak, D. Al-Ani, A. Emadi, and B. Bilgin, "Dynamic Modeling of an Interior Permanent Magnet Machine with Space-Vector-Modulation-Based Voltage Source Inverter," in *Proc. WCX SAE World Congress Experience*, June 2020.

[62] Z. Ruan, W. Song, and Y. Yan, "Current Harmonic Suppression for Dual Three-Phase Permanent Magnet Synchronous Motor Drives," *IEEE Access*, vol. 7, pp. 143 888–143 898, Sept. 2019.

[63] R. Zanasi, F. Grossi, and M. Fei, "Complex Dynamic Models of Multi-Phase Permanent Magnet Synchronous Motors," in *Proc. IFAC 18th World Congress*, vol. 44, no. 1. IFAC, 2011, pp. 12 183–12 188.

[64] P. Hollstegge, D. Keller, and R. W. De Doncker, "Dual three-phase machine modeling and control including saturation, rotor position dependency and reduction of low current harmonics," in *Proc. IEEE International Electric Drives Production Conference (EDPC)*, Wurzburg, Germany, April 2018.

[65] H. Kim, K. Shin, S. Englebretson, N. Frank, and W. Arshad, "Analytical model of multiphase permanent magnet synchronous machines for energy and transportation applications," in *Proc. IEEE International Electric Machines and Drives Conference (IEMDC)*, Chicago, IL, May 2013, pp. 172–179.

[66] M. Kozovsky, P. Blaha, and P. Vaclavek, "Verification of nine-phase PMSM model in d-q coordinates with mutual couplings," in *Proc. IEEE International Conference on Control System, Computing and Engineering (ICCSCE)*, April 2017, pp. 73–78.

[67] X. Wang, C. Gu, G. Buticchi, H. Zhang, and C. Gerada, "A Novel Modelling Approach of Modular Multi Three-phase Drive System for High Performance Applications," in *Proc. IEEE International Conference on Electrical Machines and Systems (ICEMS)*, Harbin, China, Aug. 2019.

[68] Y. Hu, Z. Q. Zhu, and M. Odavic, "Comparison of Two-Individual Current Control and Vector Space Decomposition Control for Dual Three-Phase PMSM," *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4483–4492, Sept. 2017.

[69] G. Feng, C. Lai, M. Kelly, and N. C. Kar, "Dual Three-Phase PMSM Torque Modeling and Maximum Torque per Peak Current Control Through Optimized Harmonic Current Injection," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 5, pp. 3356–3368, July 2019.

[70] X. Chen, J. Wang, B. Sen, P. Lazari, and T. Sun, "A High-Fidelity and Computationally Efficient Model for Interior Permanent-Magnet Machines Considering the Magnetic Saturation, Spatial Harmonics, and Iron Loss Effect," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4044–4055, July 2015.

[71] G. Luo, R. Zhang, Z. Chen, W. Tu, S. Zhang, and R. Kennel, "A Novel Nonlinear Modeling Method for Permanent-Magnet Synchronous Motors," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 10, pp. 6490–6498, Oct. 2016.

[72] S. Li, D. Han, and B. Sarlioglu, "Modeling of Interior Permanent Magnet Machine Considering Saturation, Cross Coupling, Spatial Harmonics, and Temperature Effects," *IEEE Transactions on Transportation Electrification*, vol. 3, no. 3, pp. 682–693, Sept. 2017.

[73] P. Azer, B. Bilgin, and A. Emadi, "Mutually Coupled Switched Reluctance Motor: Fundamentals, Control, Modeling, State of the Art Review and Future Trends," *IEEE Access*, vol. 7, pp. 100 099–100 112, July 2019.

[74] D. Hadiouche, H. Razik, and A. Rezzoug, "On the Modeling and Design of Dual-Stator Windings to Minimize Circulating Harmonic Currents for VSI Fed AC Machines," *IEEE Transactions on Industry Applications*, vol. 40, no. 2, pp. 506–515, March 2004.

[75] L. Harnefors and H. P. Nee, "Model-based current control of ac machines using the internal model control method," *IEEE Transactions on Industry Applications*, vol. 34, no. 1, pp. 133–141, Jan. 1998.

[76] *PrimePACK^{TM}2 module with Trench/Fieldstop IGBT 4 and Emitter Controlled 4 diode and NTC*, FF600R12IE4 Datasheet, Infineon Technologies, Nov. 2013, Rev 2.4.

[77] A. Blinov, D. Vinnikov, and T. Jalakas, "Loss calculation methods of half-bridge square-wave inverters," *Electronics and Electrical Engineering Research Journal*, vol. 113, no. 7, pp. 9–14, Sept. 2011.

[78] *HybridPACK ^{TM} Automotive Power Modules*, Infineon Technologies, Jan. 2010, Rev 2.1.

[79] K. Yang, "Transient Electro-Thermal Analysis of Traction Inverters Transient Electro-Thermal Analysis of Traction Inverters," Master's thesis, McMaster University, 2014.

[80] A. Bouzida, R. Abdelli, and M. Ouadah, "Calculation of IGBT power losses and junction temperature in inverter drive," in *Proc. IEEE International Conference on Modelling, Identification and Control (ICMIC)*, Algiers, Algeria, Jan. 2017, pp. 768–773.

[81] J. Pou, D. Osorno, J. Zaragoza, S. Ceballos, and C. Jaen, "Power losses calculation methodology to evaluate inverter efficiency in electrical vehicles," in *Proc. IEEE International Conference on Workshop Compatibility and Power Electronics (CPE)*, Tallinn, Estonia, June 2011, pp. 404–409.

[82] H. Huang, A. T. Bryant, and P. A. Mawby, "Electro-thermal modelling of three phase inverter," in *Proc. IEEE European Conference on Power Electronics and Applications (EPE)*, Birmingham, UK, Sept. 2011.

[83] G. I. Orfanoudakis, M. A. Yuratich, and S. M. Sharkh, "Analysis of dc-link capacitor current in three-level neutral point clamped and cascaded H-bridge inverters," *IET Power Electronics*, vol. 6, no. 7, pp. 1376–1389, Sept. 2013.

[84] A. D. Callegaro, J. Guo, M. Eull, B. Danen, J. Gibson, M. Preindl, B. Bilgin, and A. Emadi, "Bus Bar Design for High-Power Inverters," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2354–2367, March 2018.

[85] *TMS320F2837xD Dual-Core Microcontrollers*, TMS320F28377D Datasheet, Texas Instruments, Dec. 2013.

[86] *TMS320F2837xD Dual-Core Microcontrollers*, Technical Reference Manual, Texas Instruments, Dec. 2013.