LOW-VOLTAGE-TO-CELL BATTERY BALANCING CIRCUIT

MODELING AND IMPLEMENTATION OF A HARDWARE EFFICIENT LOW-VOLTAGE-TO-CELL BATTERY BALANCING CIRCUIT FOR ELECTRIC VEHICLE RANGE EXTENSION

BY

CHRISTINA RICZU, B.Eng. & Co-op

A THESIS

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AUTHOR:	Christina Riczu B.Eng. & Co-op (Electrical & Biomedical Engineering), McMaster University, Hamilton, Canada
SUPERVISOR:	Dr. Jennifer Bauman & Dr. Saeid Habibi
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Lay Abstract

One disadvantage of electric vehicles is their limited driving range when compared to internal combustion engine vehicles. Thus, there is a requirement to make the electric system as efficient as possible in order to increase its range. A large piece of the electric system includes the battery pack. Battery packs are typically constructed from around 100 battery cells in a series connection. During use of an electric vehicle, the battery cells become mismatched. This effect is also amplified as the electric vehicle ages. In order to use the whole capacity of the battery pack, and thus the entire range of the electric vehicle, the cells should be balanced. The thesis presents the design, modeling and implementation of a novel hardware efficient battery balancing circuit. The effect of the battery balancing circuit on driving range is examined.

Abstract

One disadvantage of electric vehicles is their limited driving range when compared to internal combustion engine vehicles. Battery packs are also a significant cost to electric vehicle manufacturers, and lithium-ion battery cells must remain within controlled voltage limits. Thus, the requirements for the electric system are to be cost effective, perform battery management, and make it as efficient as possible to increase its range.

Battery packs are typically constructed from around 100 battery cells in a series connection. During use of an electric vehicle, the battery cells become mismatched due to small differences in capacity. This effect is further amplified as the electric vehicle ages. Diverging cells cause issues during driving, since weak cells can limit the useable capacity of the vehicle. In order to use the whole capacity of the battery pack, and thus the entire range of the electric vehicle, the cells should be balanced. Strong cells should distribute their excess capacity to weaker cells during driving.

The thesis presents the design, modeling and implementation of a novel hardware-efficient battery balancing circuit. First, the theory behind battery balancing is presented. Next, existing battery balancing circuits are compared. Finally, the proposed battery balancing circuit is discussed. The design of the proposed topology is examined in detail. Simulations show that the circuit transfers energy between non-adjacent cells throughout the entire pack. Experimental work is performed on two custom printed circuit boards, a 12 cell lithium-ion module, and a 12V lead acid battery. The results confirm the function of the prototype.

The effect of the battery balancing circuit on driving range is examined with vehicle modeling simulations. A 2018 Chevrolet Bolt model is produced and capacity differences are given to each cell. The proposed topology balances the cells while driving, extending driving range on UDDS and HWFET drive cycles.

To my family,

your endless love is overflowing, I can only give it back to the world

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Notation, Definitions, and Abbreviations

Definitions

Greenhouse Gasses

Components of the atmosphere that contribute to the Greenhouse Effect of warming atmosphere. Greenhouse gasses include water vapour, carbon dioxide, methane, nitrous oxide and ozone.

Life Cycle The entire lifetime of a product, from the raw materials required to generate the product, to the supply of the product to the manufacturer, to the energy required to produce, sell and maintain the product.

Source-to-wheel

The assessment of the environmental impact of a product throughout its lifespan.

Abbreviations

AC2C	Adjacent cell to cell
ANL	Argonne National Laboratory
APM	Auxiliary power module
BB-APM	Battery-balancing APM
BCM	Boundary conduction mode
BEV	Battery electric vehicle
C2P	Cell to pack
CCM	Continuous conduction mode
DC2C	Direct cell to cell
DCM	Discontinuous conduction mode
EPA	Environmental Protection Agency
EV	Electric vehicle
FBC	Full-bridge converter
GUI	Graphical user interface
HBC	Half-bridge converter
HEV	Hybrid electric vehicle
HIL	Hardware-in-the-loop

HPPC	Hybrid pulse power characteristic
HV	High voltage
HWFET	Highway fuel economy driving schedule
ICE	Internal combustion engine
LCO	Lithium cobalt oxide
LFP	Lithium iron phosphate
LMO	Lithium manganese oxide
LTO	Lithium titanate oxide
LV	Low voltage
LVC	Low voltage connection
MC2MC	Multi-cell to multi-cell
MPG	Miles per gallon
MPGE	Miles per gallon equivalent
MY	Model year
NCA	Lithium nickel cobalt aluminum oxide
NMC	Lithium nickel manganese cobalt oxide
P2C	Pack to cell
PCB	Printed circuit board

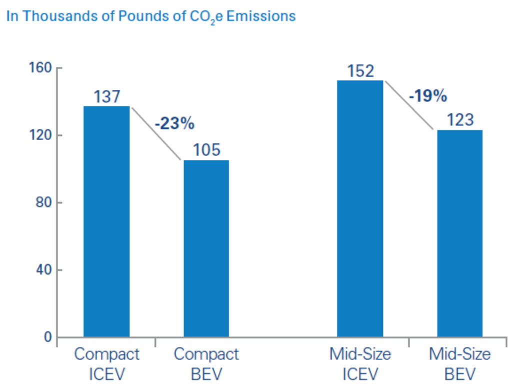
PHEV	Plug-in hybrid electric vehicle
SOC	State of charge
SPDT	Single-pole double-throw
OCV	Open circuit voltage
UDDS	Urban dynamometer driving schedule
ZVS	Zero-voltage switching
ZCS	Zero-current switching

Chapter 1

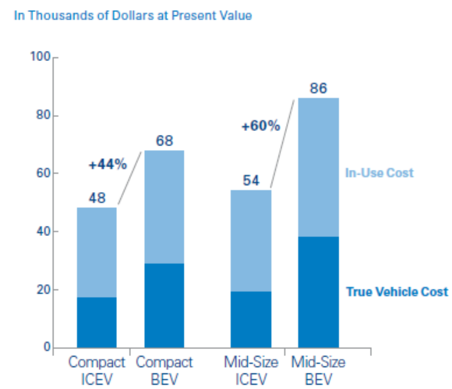
Introduction

1.1 Background and Motivation

Electric vehicles (EVs) have lower source-to-wheel energy consumption and can reduce greenhouse gas emissions by up to 23% when compared to traditional internal combustion engine (ICE) vehicles [1][2], as seen in Figure 1.1a. They experienced a rising trend in sales over the last five years which is fueled by environmental concerns and government policy [3]. The trend worldwide has been an increase in vehicle efficiency, seen in Figure 1.2, due to policies that mandate minimum fuel economy standards measured in miles per gallon (mpg)[4]. This trend is desirable for consumers, since increased efficiency of vehicles means lower costs at the pump or the electrical outlet. However, the total cost of owning a battery electric vehicle (BEV) over 20 years is up to 60% higher than ICE vehicles in Figure 1.1b, in part due to the high cost of manufacturing the battery pack [2]. Thus, the main concerns for automotive manufacturers today is to increase the efficiency of the vehicle, extend the available range, and lower the total cost to consumers.



(a) BEV vs. ICE Emissions



(b) BEV vs. ICE Cost

Figure 1.1: BEV vs. ICE Comparisons [2]

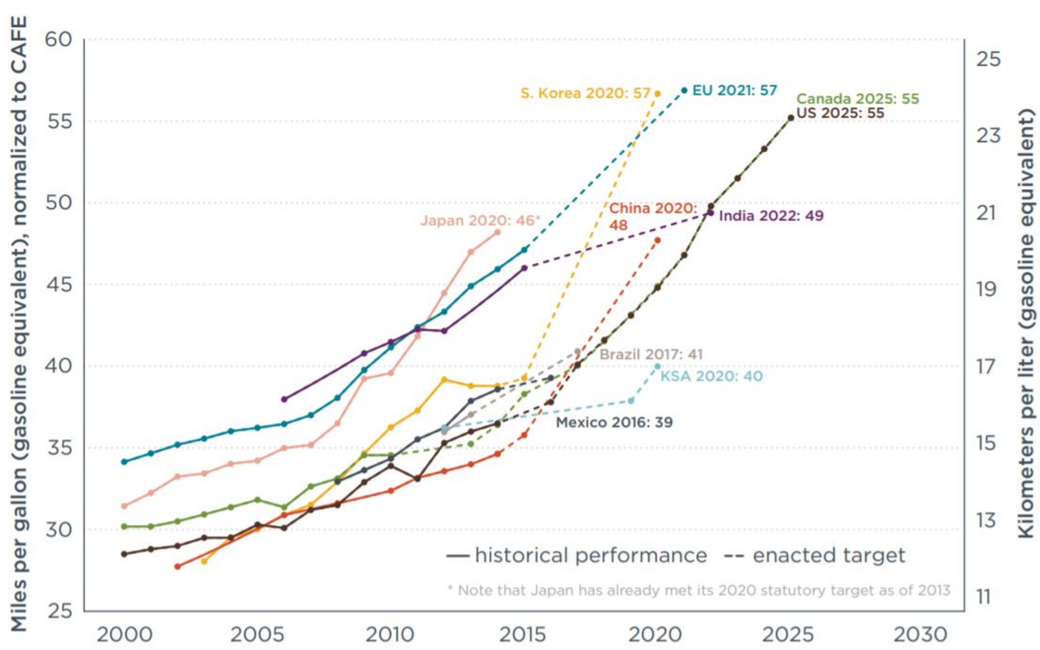


Figure 1.2: MPG by Country: 2000 - 2030 [4]

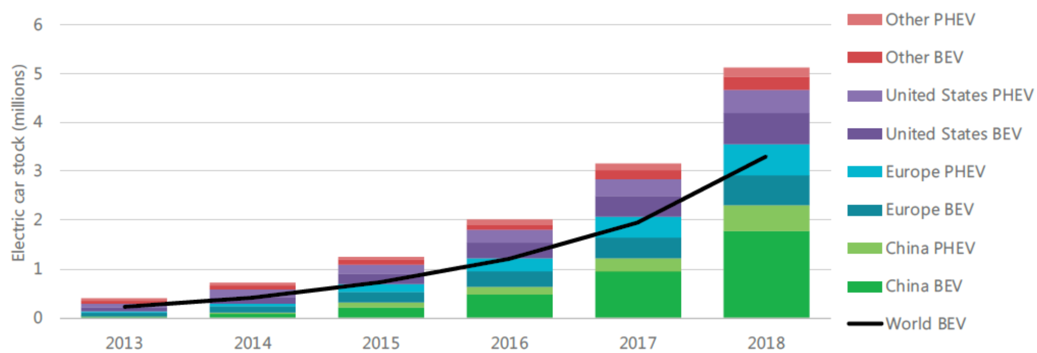


Figure 1.3: Global EV Stock: 2013 - 2018 [1]

Despite their high manufacturing cost, the EV market and unit sales are at a record high. EV car stock reached a record 5.1 million in 2018 [1], nearly doubling the previous year stock seen in Figure 1.3. This trend extends to commercial vehicle sales as well. New car sales in the US have dramatically surged in the last couple of years, seen in Figure 1.4 [5]. Thus, there is merit to investing in automotive research and commercialization. Since the main component to make up an EV is the battery pack, it is imperative to look at the history of battery technology and its effects on the automotive industry.

The electric battery was invented by professor Como Alessandro Volta as a means to artificially replicate the electric eel [6]. It became an opportunity to transition from stationary electronics to portable hardware. The initial battery cells were limited to a singular use, also named primary cells, driving research and interest into rechargeable versions [7]. After the commercialization of the lead-acid chemistry which allowed for the recharge of cells, the rise of nickel cadmium (NiCd) and nickel metal hydride (NiMH) batteries followed suit. Today, the lithium-ion

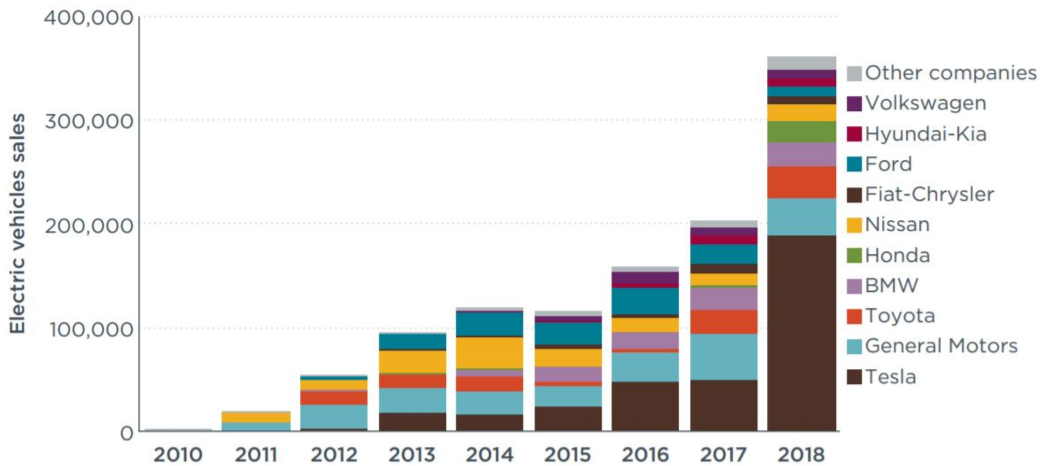


Figure 1.4: US Electric Vehicle Sales: 2010 - 2018 [5]

battery dominates the consumer electronics market [8]. Its main advantages of higher voltage and increased power density is undeniable, allowing battery packs to require less cells in series and with more capacity [7]. In addition, it has no memory and touts a low self-discharge rate. However, this chemistry has a high manufacturing price when compared to older cells that have reached maturity in design and manufacturing life cycles. Operating outside of the recommended voltage limits causes lithium-ion batteries to explode, or at the very least cause damage and accelerate aging. They require battery management systems consisting of both protection hardware and monitoring software to ensure that safety is not compromised.

For practical use, lithium-ion cells are typically stacked to increase the voltage from the small voltage range of one cell – typically 3 to 4 V – to the operating range of electronics and electric motors. In EVs, this can range from the low-voltage (LV) 12V electronics to an entire high-voltage (HV) battery pack consisting of 80 to 100 cells, from 240 to 400V. The monitoring of all cells in the pack would be trivial if lithium-ion batteries were manufactured identically, but there are several reasons for lithium-ion cells to differ in capacity; manufacturing impurities, temperature gradients, self-discharge, and mechanical constraints [9]. When placing lithium-ion cells in a series string to produce a larger voltage, these capacity differences manifest in stronger and weaker cells. These variations will amplify when the cells are cycled. Thus it is necessary that lithium-ion batteries be operated well within their limits at all times, and packs need to monitor and mitigate diverging cells in order to ensure safety

Early battery models were based on experimental data collected from testing, called behavioral models. Due to limited resources and knowledge, as well as the risk of detrimental explosion, the full capacity of the lithium-ion battery could not be utilized. With decades of research and testing, improved battery models and the use of intelligent battery management systems (BMS) and new algorithms have allowed lithium-ion battery users to extend the working range of the battery. The BMS is now a crucial part in every circuit that includes a lithium-ion battery. Its task is to monitor the lithium-ion cell conditions through voltage, current, and temperature sensors, and act if the cell is near the operating limits. While the sensors utilized in the BMS strategy are straightforward, the hardware that is used to keep cells within the correct limits varies greatly. A tradeoff between efficiency and cost has swayed automotive manufacturers towards simple, low cost, inefficient circuits that perform the basic duties of limiting cell voltage range. While there is a breadth of research on efficient practices for sharing energy between strong and weak cells, there is a hesitation by the industry to incorporate these complicated, bulky designs in EVs. Thus, there is a prevalent gap between industry practices and academic research in the topic of battery balancing circuits.

In brief, there is a need to mitigate the negative effects of lithium-ion characteristics, which is amplified when building battery packs with many cells in series. While state-of-the-art battery balancing techniques have incredibly high efficiency, they come with a high price tag typically due to the complexity or number of inductors required. There is also a notable disconnect between industry and research due to the high cost and difficulty in quantifying the benefits on a system-wide EV level.

1.2 Research Objectives and Contributions

The objective of the research is to develop a vehicle model of a 2018 Chevrolet Bolt with a simplified version of the proposed balancing circuit. The purposes of the simulation are to:

- Calculate the expected range of the vehicle
- Quantify the range extension of a vehicle using battery balancing

The main contribution of this research is a battery balancing strategy that strikes a balance between the current industry standard and overly complex solutions. In particular, this thesis presents the design, modeling, control, and experimental results of a battery balancing circuit with a low component count. The circuit achieves the following:

- Facilitate the flow of energy between non-adjacent cells in an EV battery pack
- Minimize the differences of state-of-charge (SOC) between cells in a pack

- Minimize the number of components, particularly switches and inductors

1.3 Thesis Organization

The dissertation is organized as follows. Chapter 1 has demonstrated the motivations for electrification; it allows both a reduction in environmental impact, as well as shows a thriving EV stock market and growing EV sales. It identifies the necessity for battery balancing in HV battery packs due to well-known limits on lithium-ion batteries. It introduces the research objectives and contributions.

Chapter 2 describes the literature review pertinent to the thesis, including battery chemistry, characteristics, and modeling, as well as control and operating limits. The construction and control of battery packs is introduced alongside the review of existing battery balancing circuits. State-of-the-art battery balancing is also examined.

Chapter 3 describes the proposed battery balancing circuit by discussing the design, modeling and control of the circuit. The system architecture is shown and described. The module-level circuit is proposed and printed circuit board (PCB) component selection for two PCBs are analyzed. The functions of the proposed design are divided into a switch matrix PCB, and a cell balancing DC/DC converter PCB. Principles of operation are discussed for both PCBs, while the overall proposed control algorithm is generated. The importance of dividing the algorithm into even and odd cell balancing is shown. Simulations of the proposed DC/DC converter are plotted and analyzed, as well as a system model.

Chapter 4 relays the experimental results from the proposed circuit. The test bench is shown, which includes a 12-cell lithium-ion module, 12V lead-acid battery, and the proposed circuit. Schematics and PCB footprints for both boards are shown and discussed. Control algorithms used to generate the switching sequences are given. Resulting waveforms and efficiency for the test cases are shown and analyzed.

Chapter 5 introduces the concepts of vehicle modeling, as well as an in-depth look at the vehicle model used for the research. A 2018 Chevrolet Bolt base model is described, as well as the changes to the model to reflect non-ideal cell capacities. Results show the effect of the proposed circuit on pack SOC convergence as well as increased driving range.

Chapter 6 summarizes the dissertation with the results and future work. SOC convergence and driving range are discussed as benefits of the proposed circuit. Future work is divided into both hardware and software endeavors.

Chapter 2

Energy Storage Systems

2.1 Battery Characteristics and Modeling

2.1.1 Battery Cells

2.1.1.1 Chemistry

Most modern electric vehicles (EVs) use a high-voltage (HV) lithium-ion battery pack for energy storage. Lithium-ion refers to the cluster of cell chemistries that pair a carbon or graphite anode with various cathode materials such as lithium titanate oxide (LTO), lithium manganese oxide (LMO), lithium iron phosphate (LFP), lithium cobalt oxide (LCO), lithium nickel cobalt aluminum (NCA), and lithium nickel manganese cobalt (NMC). The typical range for the specific energy and specific power of these lithium-ion cells are 90 − 230 Wh/kg and 160 − 2700 W/kg respectively [10][11][12]. In comparison to other energy storage chemistries such as lead-acid, nickel-cadmium, nickel-metal hydride, and ultra-capacitors, lithium-ion has the highest energy density. This characteristic of lithium-ion cells is advantageous in EVs since more energy can be stored in the same amount of weight as other chemistries, increasing the driving range of the vehicle. The lithium-ion cell owes its large energy density and stability to lithium, which has a lower density and smaller radii than other materials such as zinc and lead [13]. A cell provides energy by transferring lithium ions and electrons from the cathode to the electrode during discharge.

2.1.1.2 Form Factor

Batteries can be packaged in several forms, leading to specific characteristics. There are four different forms available today: button, cylindrical, pouch and prismatic [14]. These packages can be seen in Figure 2.1.

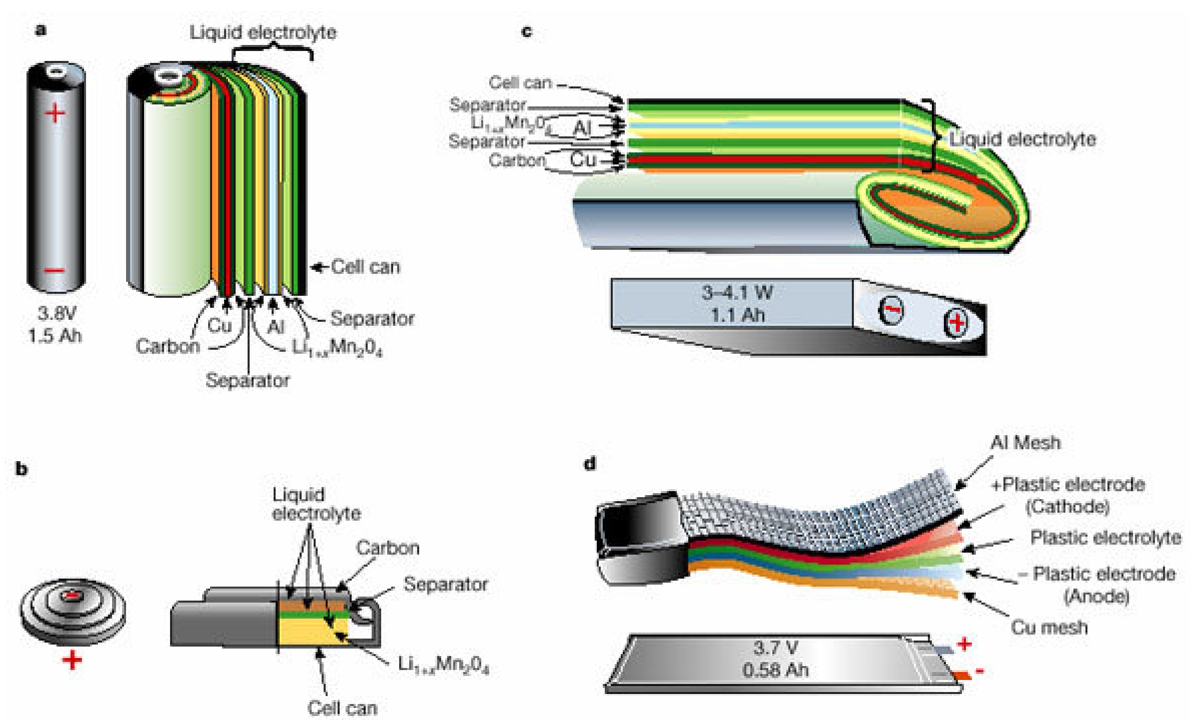


Figure 2.1: Battery Packages a) Cylindrical b) Button c) Prismatic d) Pouch [14]

Cylindrical cells are the most robust cell on the market, and easy to manufacture. The tubular shape is formed by rolling anode and cathode sheets into a cylindrical shape, providing a package resistant to pressure and deformation. The final form of a cylindrical cell is seen on the left of Figure 2.1a, while the unrolled package is on the right.

Button cells (also known as coin cells) are small, cylindrical cells that are typically no larger than a couple of centimeters in diameter, and less than a centimeter in height. Their small form requires little material, thus they are inexpensive to manufacture. The anode and cathode make the caps of the cell, shown in Figure 2.1b. Typical uses for button cells include watches, scales, medical implants and car keys. Their small energy capacity and low recharge rate limits their use beyond small, portable electronics.

Prismatic cells are created by placing a pouch cell inside an enclosure, typically made of aluminum in a rectangular shape. Although giving the cell more structure and resilience to puncture, prismatic cells can still swell during use and require mechanical pressure exerted to ensure safety. The wrapping of a pouch cell into a prismatic one is seen on the top of Figure 2.1c, while the final package is seen on the bottom.

Pouch cells have an increase in energy density due to less packaging when compared to cylindrical cells, but offer some mechanical disadvantages. Their high capacity is thanks to the complex folding of anode and cathode sheets into a flat, rectangular sheet. Two tabs are placed outside of the pouch exterior to allow for connections to the anode and cathode, respectively. However, the flat shape and flexible dimensions make an easily punctured cell. In addition, pouch cells must have a minimum pressure exerted on the largest faces or risk swelling during use.

The pouch cell can be seen in Figure 2.1d.

2.1.1.3 Safety and Operating Limits

To ensure proper lithium-ion battery function, a set of operating limits should be maintained. While each lithium-ion cell has its own characteristics described by the manufacturer, lithium-ion cells will have a voltage limit between 1.5 - 4.2V. Different cathodes provide several voltage ranges; LTO and LMO range from 1.5 - 2.7V, LFP ranges from 2.0 - 3.7V, and LCO, NCA, NMC and LMO all range from 2.5 - 4.2V [15]. Due to the higher voltage range, EV manufacturers typically favour the latter chemistries in order to have less cells in series to achieve the same desired HV pack.

Overcharging a lithium-ion cell results in a large current flow. Two issues arise from this over-voltage event; lithium plating and overheating [16]. When excessive current occurs, the lithium ions cannot be housed in the anode and begin to deposit on the surface of the anode as metallic dendrites. This process is called lithium plating and is irreversible, causing capacity loss and a potential for a short circuit if dendrites grow too large. In addition, a large current flow will cause a surplus of heating in the cell and can trigger thermal runaway if not handled properly. Thermal runaway is the accumulation of several unwanted effects. It begins with the breakdown of protective layers between the anode and electrolyte. Ultimately, it will lead to the breakdown of materials withing the cell, causing gasses to form and the pressure buildup will cause the cell to explode.

Undercharging a lithium-ion cell can also have adverse effects [16]. The anode copper will dissolve into the electrolyte and deposit as metallic copper when returned above 2V, which can cause a short circuit. From the cathode side, low voltages will cause the cathode to lose oxygen and cause permanent capacity loss of the cell. Undercharging a cell by only 1.2% can reduce the battery capacity by as much as 9% [17]. Thus, both overcharge and undercharge should be avoided to preserve the integrity of the lithium-ion cell.

2.1.2 Battery Modeling

Since the conception of batteries as an energy source, much research has gone into understanding and harnessing their characteristic behaviours. Modeling batteries can allow for accurate electrical system designs and increased overall performance. Below, several battery models are shown for their trade-off between accuracy and performance.

2.1.2.1 Ideal Model

The ideal model of a battery is simply that of an ideal voltage source, seen in Figure 2.2a. V_{BATT} represents the normal voltage from the battery. Infinite amounts of energy and power can be requested from the source without any change in voltage over time. Although highly unrealistic, this ideal model is useful for modeling electronics that are downstream, with the assumption that the voltage will be constant over a period of time.

2.1.2.2 Behavioural Model

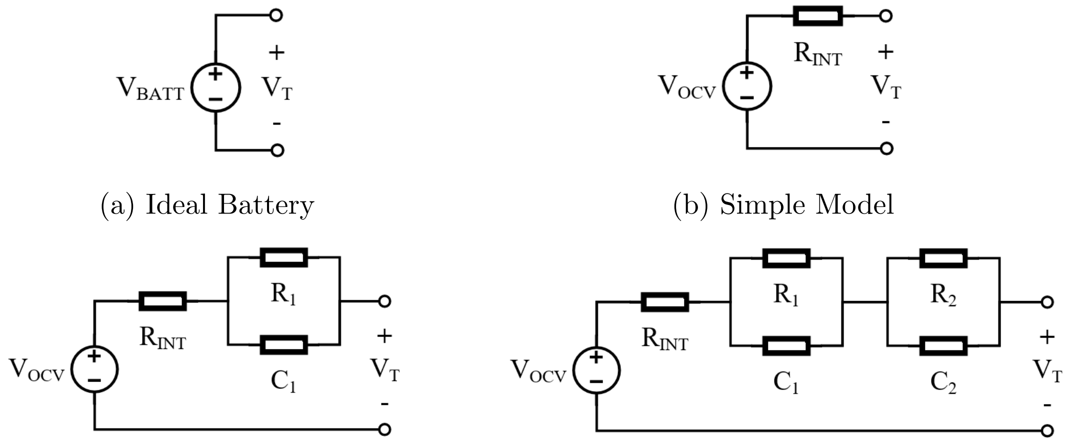
The behavioural model of a battery is based on data collected from experimental studies. The battery is typically charged and discharged completely at different rates, temperatures, or other factors that affect the rate of discharge. Curves can be fit to the data and used to establish look-up tables in models.

2.1.2.3 Equivalent Circuit Model

The equivalent circuit model is the most widely used battery model due to its initial simplicity, the ability to build complexity, and tangible physical realizations of its components.

The simplest version of the model is seen in Figure 2.2b, where an ideal voltage source V_{OCV} outputs the corresponding OCV based on the input SOC. From that, the internal resistance R_{INT} is added in series with V_{OCV} to model the basic inefficiency of the battery. R_{INT} can either be represented as a single resistance, a single lookup table, or two curves that represent the charge and discharge characteristics.

The model described above is called a zero-order model, since it does not consider the effects of time on the voltage waveform. To build on the complexity of the model, additional RC branches are placed in series. These RC branches add a time constant to the circuit and aid in modeling the non-instantaneous, exponential voltage changes that are seen in real batteries. Typically, a second-order model is used to model both the short-term and long-term voltage effects. Further RC branches model other time constants in between, adding accuracy but also increasing simulation run-time. The first-order model can be seen in Figure 2.2c and second-order model in Figure 2.2d.



(a) Ideal Battery (b) Simple Model

(c) First Order Model (d) Second Order Model

Figure 2.2: Equivalent Circuit Battery Models

2.1.3 Electric Vehicle Pack

2.1.3.1 Cell Selection

To create an EV battery pack, consideration must be given to the type of performance required from the pack. A minimum current requirement can be calculated from a powertrain if the parameters are known. From the speed and acceleration requirements, and other physical factors of the vehicle, the torque of the motor and thus the current supplied can be found. If a single cell cannot sustain the current requirement, cells can be placed in parallel at the expense of added pack complexity.

To sustain an EV for a typical range, most EVs on the market today use pouch or prismatic cells. Tesla is the only exception to the rule, using numerous cylindrical cells in parallel to achieve the same effect. The pouch and prismatic cells are useful due to their high output current, and their rectangular package lends itself well to a modular mechanical pack design. However, cooling them is no easy task. Cooling plates are typically used between cells to ensure that temperatures don't rise to dangerous levels.

2.2 Battery Balancing Circuits

2.2.1 Motivation

The HV pack consists of numerous cells connected in series. There is typically $n =$ 80 to 100 cells, where n refers to the number of cells in series. Therefore, most HV packs range in terminal voltage from 240 to 400V. The desired voltage for the pack is larger than 200V since the efficiency of the power electronics and electric motors will increase with a greater voltage. With the exception of Tesla's line of EVs, which place many lower capacity cylindrical cells in parallel, most recent EVs use a single or up to three parallel strings of pouch or prismatic cells. For example, the Tesla Model 3 uses 2170 cylindrical cells in a 96S46P configuration to achieve a pack capacity of 75kWh [18] while the 2018 Chevrolet Bolt uses a 96S3P setup of pouch cells to achieve around 60kWh of capacity [19].

In addition, the cells are typically organized into m modules of 8 to 12 cells [20]. A module will consist of the cells, a battery management system, cooling hardware, and the mechanical enclosure. Their primary use is to group cells into manageable clusters such that the battery management system can accurately measure voltage and current, and ensure that the cells do not exceed their operational limits. They also allow HV pack manufacturers to split the pack into parts that are easier to mass produce and assemble. Modules support a decentralized approach to battery management systems, allowing modules to house the low-level hardware required to calculate battery SOC and read cell temperatures. Building a singular HV pack with less modules, such as the Tesla Model 3, allows for increased overall HV pack energy density and reliability during assembly, but is more difficult to repair.

It is well-known that a HV battery pack will have weaker cells due to manufacturing impurities, temperature gradients across the pack, self-discharge rates, mechanical constraints and aging [9]. These differences will manifest as cell-to-cell differences in energy capacity, and will amplify over time from cycling the pack [21]. Thus, all HV battery packs require cell balancing circuits to protect the cells during charging and discharging.

Figure 2.3 shows the many different types of battery balancing methods that will be discussed in this chapter. Table 2.1 further specifies the components involved in each circuit and compares their size, control schemes, hardware implementation, balancing speed, and cost. Efficiency of each circuit is provided when reported in literature, as well as rated power and cell capacity for experimental work.

A weak cell is defined as any cell that has a reduced capacity when compared to other cells in the pack [22] as a result of this capacity fade. This cell will take less time to complete its charge because it requires less energy to do so. In order to continue charging the pack so that all cells reach their upper limit of charge, the weak cell will have to be slightly discharged so it can continue to charge with the other cells in the pack. Similarly, discharging will cause problems. The weakest cell will be discharged first and impose a lower limit on the pack. This is what is seen in practice with passive balancing. However, energy should be added to the cell during discharge if it is desired to use the full capacity of each cell. Battery balancing circuits seek to handle the issues that arise from weak cells for both of these cases.

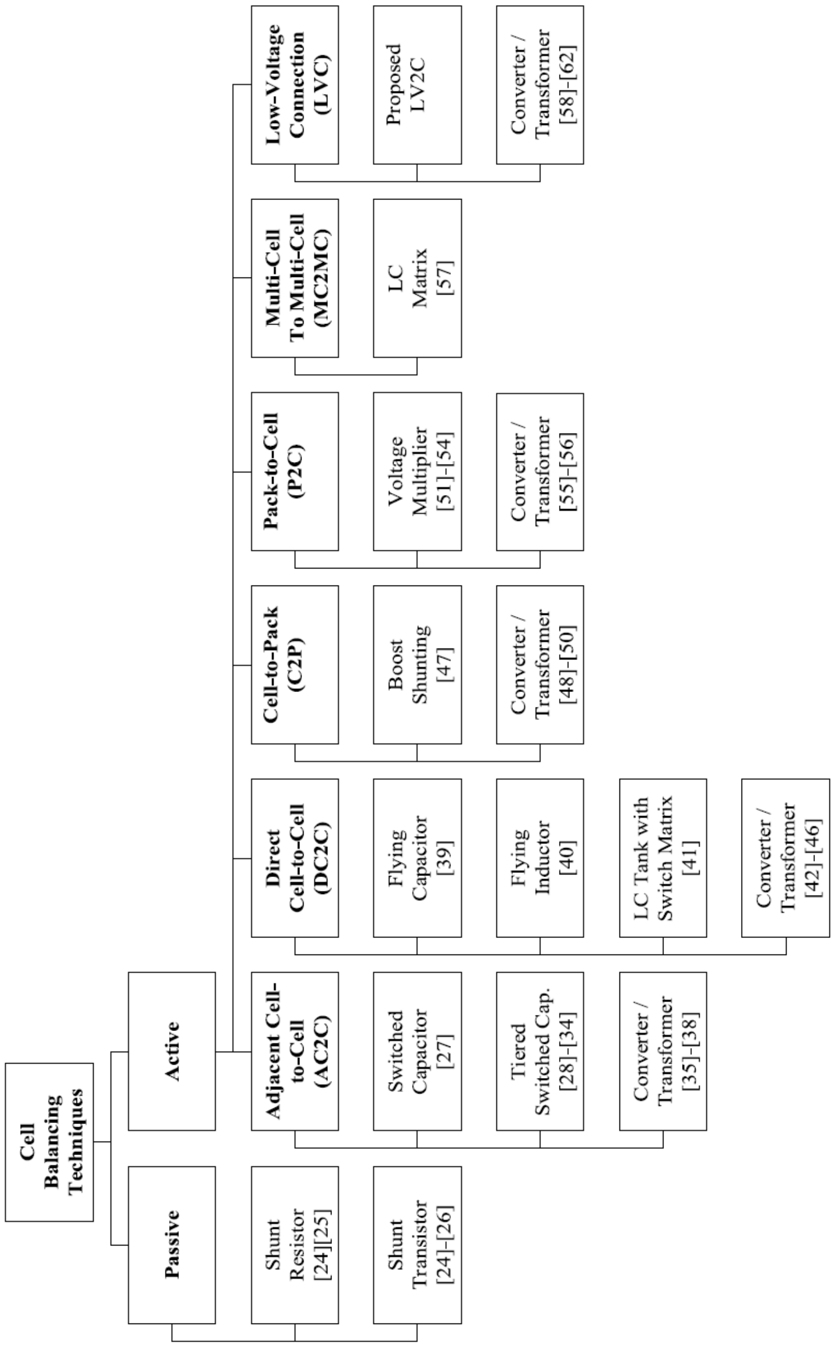


Figure 2.3: Battery Balancing Methods

2.2.2 Passive Balancing

Battery balancing methods fall into two major categories: passive and active. In commercial EVs, passive cell balancing is the prominent technology due to its low cost and simple control [23]. This method utilizes a dissipative element to drain excess energy from cells with higher voltage [24] [25] [26], which are the weakest cells with small capacities. This prevents them from overcharging while other cells in the pack continue to charge. Though the component count is low and control is simple, using only n switches and n resistors per n cells, there are two main drawbacks: all excess energy is lost, and weak cells cannot be charged while driving. Thus, only the charging issues of weak cells are handled by the battery balancing circuit and the HV pack will continue to deplete unevenly across cells. This means that the SOC of weak cells can never be aligned with stronger cells during driving, imposing a range reduction on the vehicle. In addition, the excess energy dissipated in the resistor or transistor components is converted to heat. This added heat increases the requirements of the cooling solution for the HV pack, which will increase the size of the cooling plate and add to the weight of the vehicle. If the cooling solution isn't made larger, then the additional heat will contribute to age of the cell or module and will negatively impact the overall lifetime of the HV pack.

A series stack of n cells in a battery pack is simplified and shown in Figure 2.4. The battery cells are represented by a filled in black circle, while equalizer elements E (resistors, transistors, capacitors, inductors, transformers, etc.) are shown as the outline of a circle. The power flow of the battery balancing methods can be simplified into charge and discharge operations with respect to the battery cells, shown in green and red respectively. The charge operation will have current flowing into the battery

Table 2.1: Battery Balancing Comparison Table

	Passive Balancing	Active Balancing							
		AC2C		DC2C		C2P	P2C	LVC	
Parameters	Shunt Resistor	Switched Capacitor	Buck-Boost Conv.	Flying Capacitor	LC Tank	Multi-Out Transf.	Switched Transf.	BB-APM	Proposed LV2C
Reference	[24][25]	[27]	[37]	[39]	[41]	[48]	[55][56]	[58][59]	
Switch	N	$2N$	$2(N-1)$	$4N$	$2(N+1)$ $+8$	$N+1$	$4N+1$	$2N$	$2(N+1)$ $+2M$
Inductor	0	0	$N-1$	1	1	0	0	0	0
Transformer [T]	0	0	0	0	0	$1[N]$	1[2]	$N[2]$	$M[1]$
Capacitor	0	$N-1$	0	1	1	0	0	N	$2M$
Diode	0	0	0	0	0	N	1	0	0
Size/Weight	E	E	P	G	G	P	S	P	G
Control Simplicity	E	E	G	S	P	G	S	P	S
Implementation	E	E	G	G	P	P	S	G	G
Balancing Speed	P	P	S	G	G	E	G	E	E
Cost	E	G	P	S	G	P	P	P	G
Efficiency	0%	–	$75-85.6\%$	$>83\%$	$93.2\%, 78.9\%$	–	81%	–	71%
Rated Power	–	–	$4W$	–	$0.56, 1.94W$	$5.2W$	$8W$	$30.95W$	$30W$
Cell Capacity	–	–	$10Ah$	–	$4.4Ah$	$2.6Ah$	$15.5Ah$	$25Ah$	$5.2Ah$
ΔSOC	–	–	–	–	15%	–	20%	16%	–

N: number of cells (typically 96), M: number of modules (typically 8), Transformer [T]: transformer with number of windings
E: excellent, G: good, S: satisfactory, P: poor

cell. Discharge will require current to flow out of the battery cell. If both charge and discharge can be completed, then the arrow shown will be represented in blue.

The green arrow at the top of the diagram in Figure 2.5a indicates that the charger can add energy to the whole pack. Assume that cells B_1 and B_2 are overcharged, B_3 is normal, and B_{n-1} and B_n are undercharged. For the shunt resistor, the charger will add energy to the pack when the EV is plugged in and charging. Since B_1, B_2 and B_3 have higher charges than B_{n-1} and B_n, they will have to deplete their excess energy during the charging operation. This extra energy will be dissipated into the equalizer elements E_1 to E_3. In this case, the equalizer elements represent the single switch and resistor combination that will drain excess energy into heat. The circuit topology for a resistor and switch can be seen in Figure 2.5b.

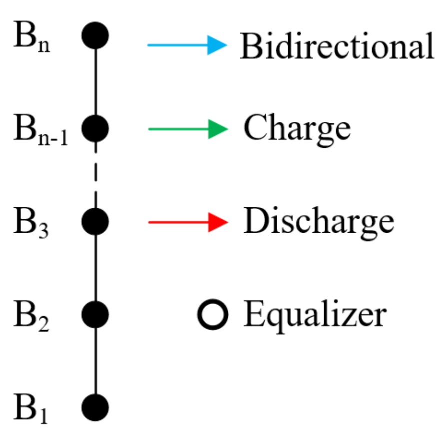
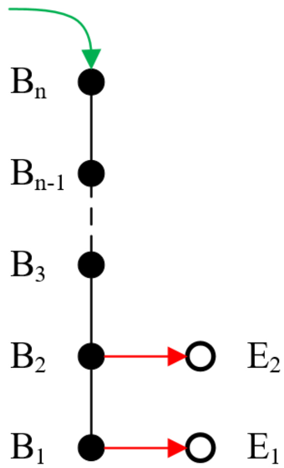
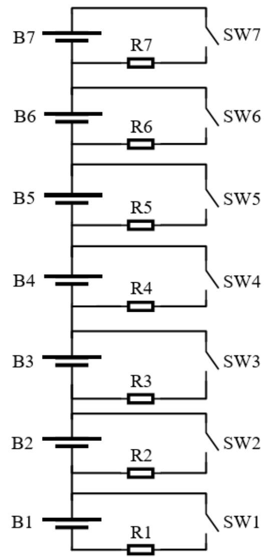


Figure 2.4: Balancing Path Definitions



(a) Passive Shunt Operation



(b) Dissipative Resistor Topology [24]

Figure 2.5: Passive Operation and Topology

2.2.3 Active Balancing

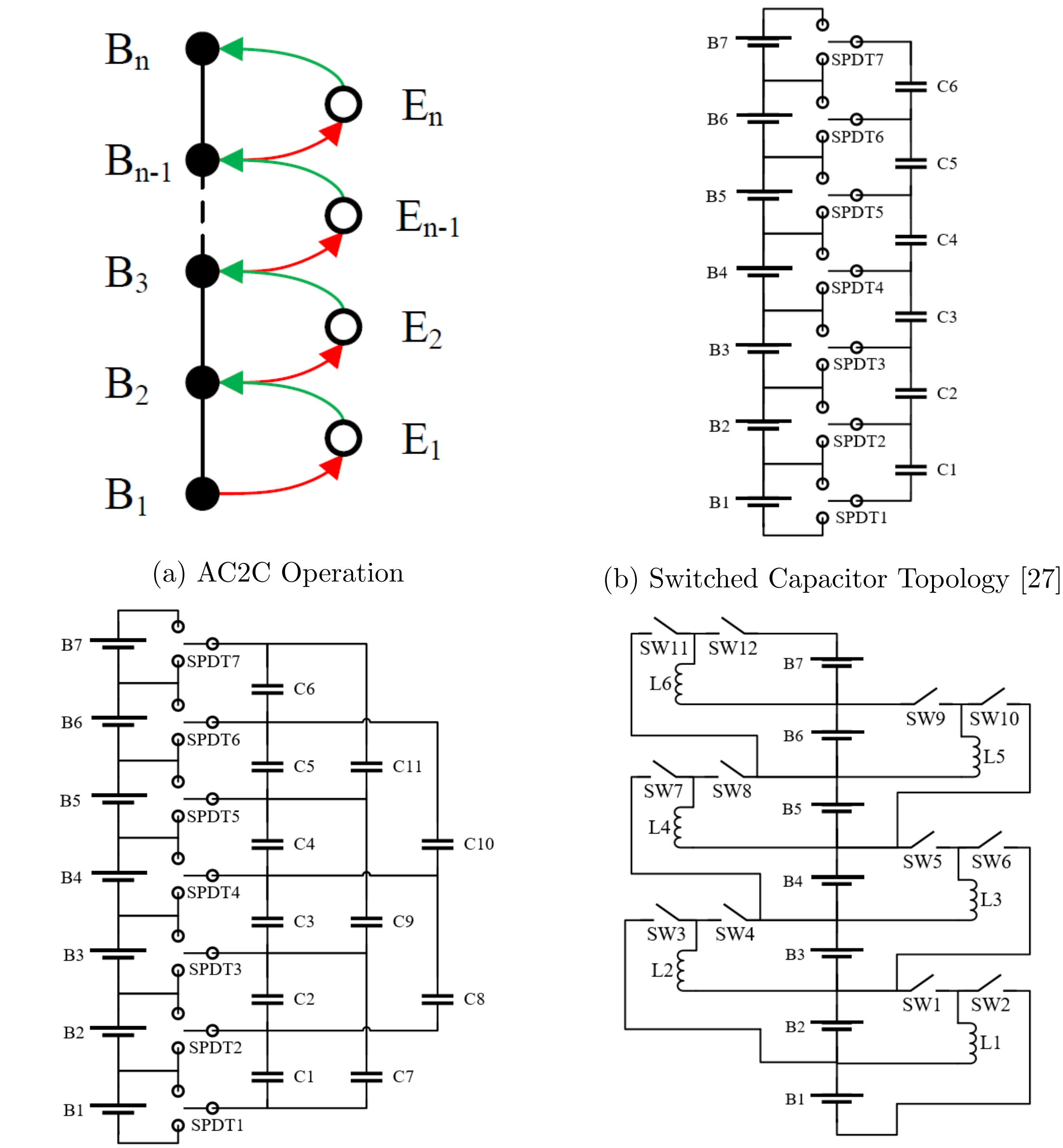
Active strategies have thus been a popular area of research as they have the potential to alleviate these drawbacks for both charging and discharging operation. In particular, if the weaker cells can be charged during driving, the vehicle range can be extended due to the use of the entire capacity of the HV pack. This is desirable for EV drivers [8]. Active methods can be further divided into six major classifications: adjacent cell-to-cell (AC2C), direct cell-to-cell (DC2C), cell-to-pack (C2P), pack-to-cell (P2C), multi-cell-to-multi-cell (MC2MC), and low-voltage connection (LVC) methods.

2.2.3.1 Adjacent Cell-to-Cell

AC2C encompasses the switched capacitor [27] and its tiered structures [28] [29] [30] [31] [32] [33] [34], Ćuk converters[35] [36], resonant converters [37], and multiple transformers [38]; this design shuttles charge from cell to cell. The highlight of AC2C is the low component count and simple control, as seen in Table 2.1. The basic switched capacitor structure uses only $2n$ semiconductor components (also referred to in literature as n single-pole-double-throw (SPDT) switches), as well as n capacitors. The basic topology can be seen in Figure 2.6b. The switches rely on a fixed frequency signal at 50% duty cycle for operation. The tiered structures add additional capacitors and switches to bridge across multiple cells, seen in Figure 2.6c. These tiered structures decrease the required balancing time in comparison to the basic structure, however it is at the expense of additional switches and cost. Another AC2C is the inductive equalizer topology seen in Figure 2.6d. This also uses $2n$ switches per cell and uses n inductors instead of n capacitors. A more complex control strategy is required for the inductive equalizer when compared to the basic and tiered capacitor structures. A fuzzy logic controller may be used to determine when and how to balance the cells.

AC2C has the slowest balancing time of all the active balancing strategies, evident from Table 2.1. Switched capacitors also experience inrush currents from hard switching, which can cause stress and failure over time. The inductive equalizer avoids the inrush currents by using inductors instead of capacitors, but n inductors adds a larger cost and weight to the vehicle. The balancing time of AC2C circuits can be reasonably cut down by increasing the operating frequency of the switches at the cost of additional switching losses. However, the fundamental problem of having a weak cell and strong cell at opposite ends of a pack will still require energy to pass across $n - 1$ capacitors and cells in the worst case. This scenario can be a likely situation due to temperature imbalance across an HV pack. In particular, slow equalization times can limit the usefulness of charging up the weak cells to extend EV range. Under some driving circumstances, such as the aggressive US06 driving cycle, the weak cells can discharge faster than the cell equalizations can take place. An additional drawback is the poor efficiency of the basic AC2C structure; the efficiency is not measured or reported for the switched capacitor or tiered structures, and only [27] mentions that the structure is to be used when efficiency is not important. The inductive equalizer reports efficiency ranging from 51 - 60% [36]. Converter based methods report efficiency up to 91.3%.

For the AC2C technique, charge is shuttled between a cell and its adjacent equalizer element, seen in Figure 2.6a. For the switched capacitor and tiered methods in Figures 2.6b and 2.6c, this equalizer represents the SPDT switch and capacitor chain structure. For the inductive equalizer in Figure 2.6d, the inductors are the equalizer. To transfer the excess charge from B_1 to B_n, the charge will have to pass from B_1 to E_1, E_1 to B_2, B_2 to E_2, and so on until E_n charges B_n. This balancing becomes tedious when there are many cells in the string, hence the long balancing times required for this type of method.



(a) AC2C Operation

(b) Switched Capacitor Topology [27]

(c) Tiered Switched Capacitor Topology [28]

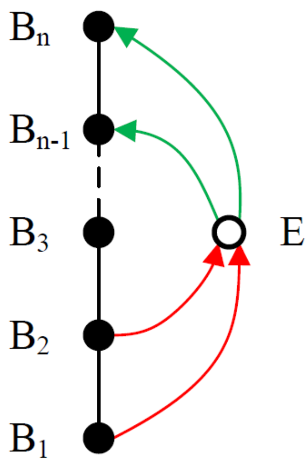
(d) Inductive Equalizer Topology [36]

Figure 2.6: AC2C Operation and Topologies

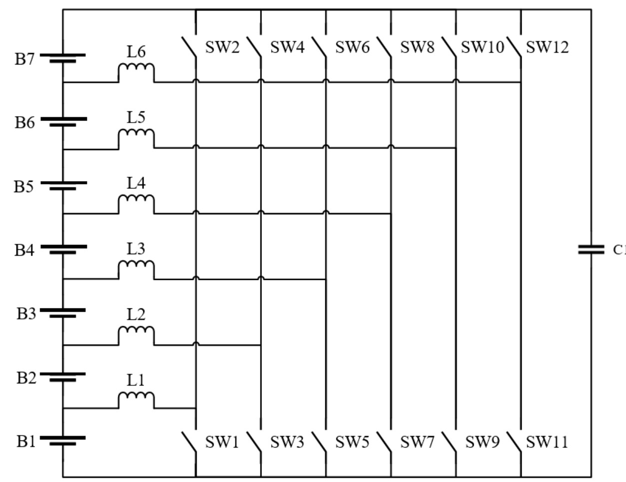
2.2.3.2 Direct Cell-to-Cell

DC2C has a faster balancing time by providing cell-specific charging, but suffers from a higher component count seen in the flying capacitor [39], flying inductor [40], LC tank [41], converter [42][43][44] and transformer [45][46] methods. These methods group the cells into stacks of up to 12 series cells and allow for direct transfer of energy from one cell to another despite the cells not being adjacent to one another. In the LC tank, $2n$ switches compose the switching matrix to choose a cell while 4 switches, one inductor and one capacitor form a tank for storing excess energy to transfer directly to weak cells. This method achieves a blend of reduced balancing time for non-adjacent cells, while keeping efficiency high. The reported efficiencies can reach 93.2%. However, at least $2n$ switches are required for any of these configurations, as well as additional capacitors and inductors.

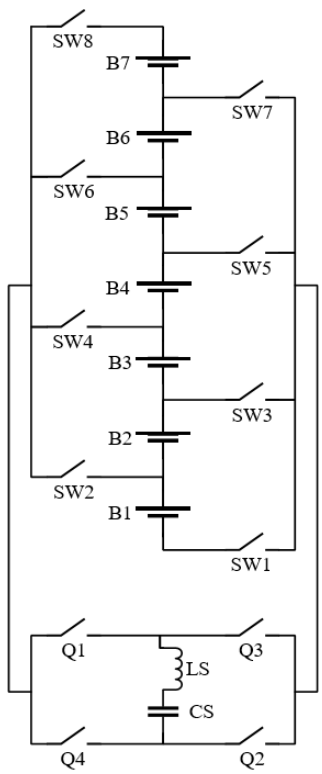
Figure 2.7a shows the balancing paths for the DC2C method. A common equalizer element E accepts charge from either B_1 or B_2, and can directly charge up B_{n-1} and B_n. This is achieved by having a matrix of switches that select the desired cell, and connect it to the common element. To reduce inrush current, the equalizer element could be a capacitor and inductor. Due to the flexibility of cell selection, the DC2C method is much faster than AC2C with only a few additional components.



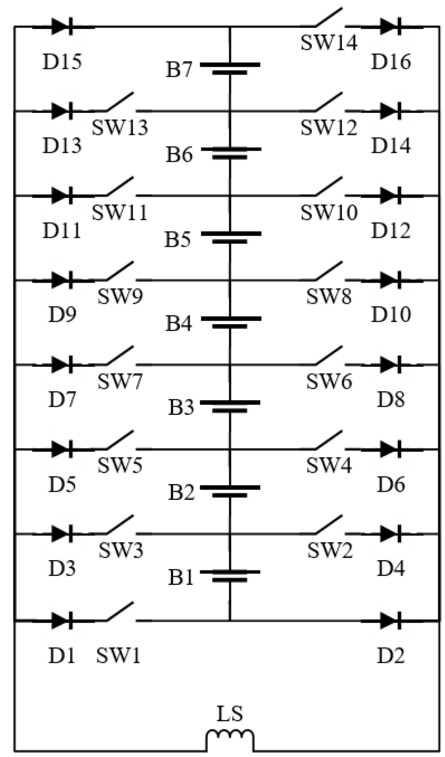
(a) DC2C Operation



(b) Interleaved Converter Topology [42]



(c) LC Tank Topology [41]



(d) Charge Equalizer Topology [40]

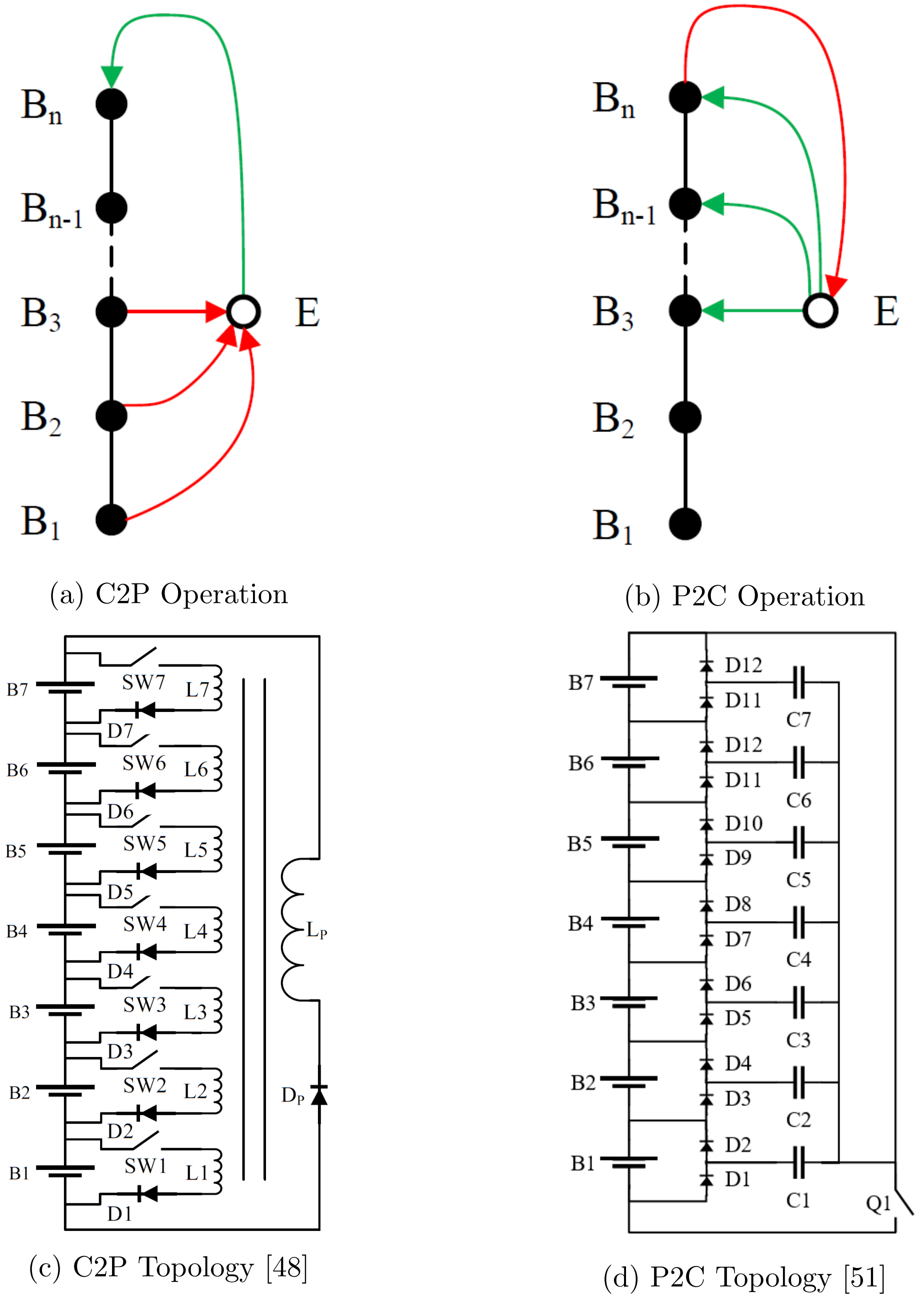
Figure 2.7: DC2C Operation and Topologies

2.2.3.3 Cell-to-Pack

C2P includes boost shunting [47] and multiple transformer configurations [48] [49]. The operation of these circuits can be seen in Figure 2.8a, where cells provide the equalizer energy which is redistributed to the whole pack. The attractiveness of these configurations is their exceptional efficiency and reduced balancing time. However, they are difficult to modularize for a commercial EV, making them less attractive as a commercial solution. Each output of the multi-winding transformer must be connected to a cell, seen in Figure 2.8c. In addition, changing the configuration of cells or reusing the balancing for multiple vehicle model years is not possible since the number of output windings will have to be changed, resulting in additional transformer design. Each circuit requires at minimum n inductors or a single, complicated transformer design which adds a large weight to the vehicle.

2.2.3.4 Pack-to-Cell

P2C uses the voltage multiplier [50][51][52][53], or transformers [54][55][56] to pull charge from the entire pack and redistribute directly to selected cells, which can be seen in Figure 2.8b. This topology suffers from the same complexities as C2P, either requiring many diodes or bulky and complex transformers. Since the P2C method is similar to the C2P and uses a similar overall circuit structure, the P2C and C2P functions can be combined by swapping diodes for additional bidirectional switches at the expense of added cost and complexity. To capitalize on a lower component count in the face of costly transformers, designers will often use unidirectional components and simplified control by taking advantage of careful switch placement and diodes where necessary.



(a) C2P Operation

(b) P2C Operation

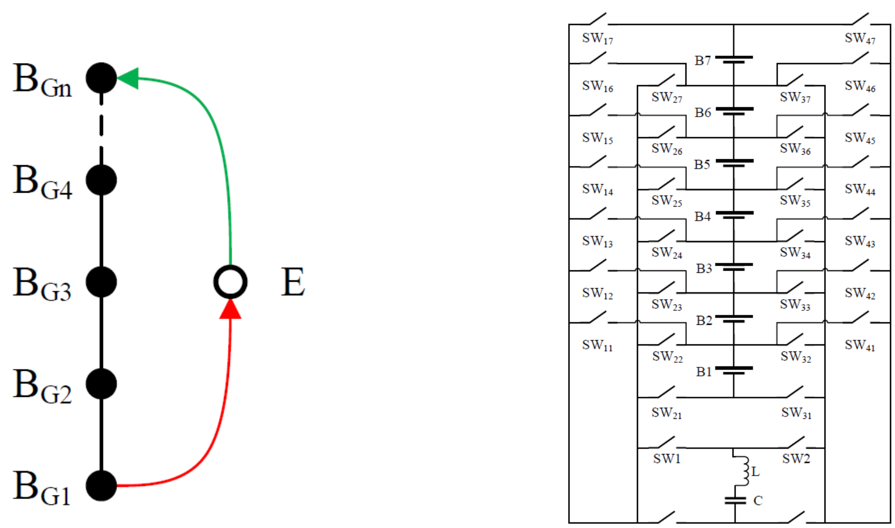
(c) C2P Topology [48]

(d) P2C Topology [51]

Figure 2.8: C2P and P2C Balancing Paths

2.2.3.5 Multi-Cell-to-Multi-Cell

The MC2MC LC matrix [57] links modules and cells, providing high efficiency and balancing time comparable to DC2C, but with an extremely high switch count. The reported experimental efficiencies were 99.2% at 0.17W and 75.9% at 0.45W. However, the switch count required is at the highest for any configuration at $4n + 4$, seen in Figure 2.9b. Figure 2.9a shows the simplicity of discharging from a group of cells B_{G1}, which could be B_1 and B_2, directly into the top group B_{Gn}, compromised of B_{n-1} and B_n.



(a) MC2MC Operation

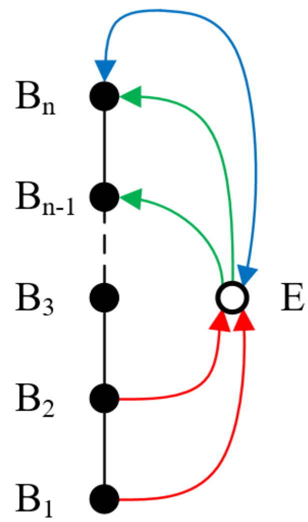
(b) MC2MC Topology [57]

Figure 2.9: MC2MC Operation and Topology

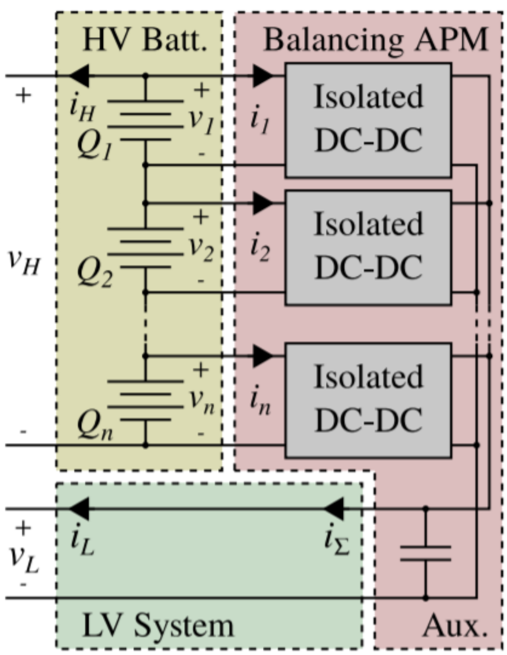
2.2.3.6 Low-Voltage Connection

Recent work has proposed utilizing the low-voltage (LV) bus as a convenient source or sink for cell balancing [58][59][60][61][62]. Reference [58] replaces the conventional isolated HV-to-LV DC/DC converter with many smaller isolated DC/DC converters, up to one converter per battery cell. The circuit is called the battery balancing APM (BB-APM), as seen in Table 2.1. In this architecture, the HV battery provides the LV accessory power through the smaller converters on a cell level, meaning the weakest cells can have less accessory power drawn from them than the healthier cells. Thus, the EV range and the battery lifetime can be extended by not deeply discharging the weakest cells [63]. The disadvantage of this architecture is the high component count: if one dual active bridge converter is used for each of the n cells in the pack, there will be $8n$ switches and n transformers required. Reference [62] proposes a circuit to perform a similar operation using only $2n$ switches and n transformers; however, the control complexity is increased.

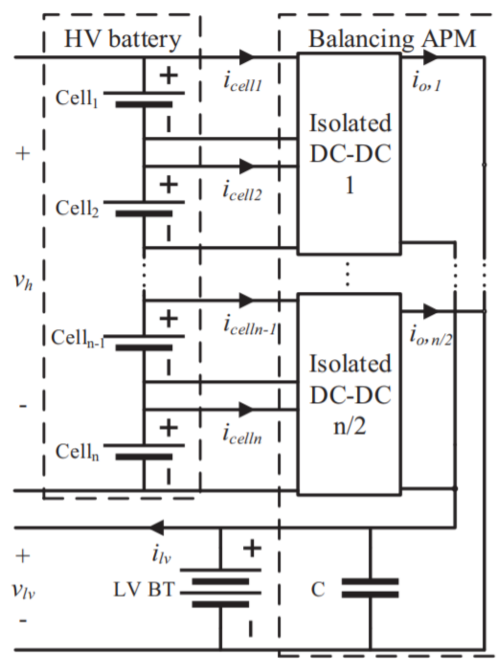
The low-voltage connection (LVC) balancing paths are shown below in Figure 2.10, and the equalizer in this case is the LV bus or the 12V lead-acid battery. Figure 2.10b shows that the circuit replaces the conventional LV battery entirely and the equalization element is the algorithm that precisely controls the LV bus load to and from the cells. The blue arrow is also used to indicate that the bidirectional APM found on most commercial vehicles can be used to add or take charge out of the 12V battery for Figure 2.10c. To equalize the charge, B_1 and B_2 can be discharged into E while B_{n-1} and B_n are being charged. If each cell has a converter attached, such as in [58], then this can all occur at the same time. This results in extremely fast balancing times. Although this balancing path looks similar to the DC2C or MC2MC, the unique ability to access all cells at the same time is what distinguishes the LVC circuits.



(a) LVC Operation



(b) LVC Single-Cell Link Topology [58]



(c) LVC Dual-Cell Link Topology [61]

Figure 2.10: LVC Operation and Topology

Chapter 3

Proposed Low-Voltage-to-Cell Balancing Circuit

3.1 System Architecture

The thesis proposes an active balancing architecture that uses the LV bus as a convenient source or sink for fast cell balancing, yet has a reduced component count compared to [58] and [59]. In contrast to [58] and [59], the proposed architecture uses a conventional isolated HV-to-LV DC/DC converter since this component is generally well-understood and has a relatively low cost due to mass production, and is already used in commercial EVs. The additional circuitry required for the proposed architecture is a single low-power DC/DC converter (e.g. 10W to 40W) per m modules, and $2(n+1)$ switches for n battery cells. However, these $2(n+1)$ switches are connected as $n+1$ bilateral switches, so only $n+1$ gate drive circuits and gate control signals are required.

The proposed low-voltage-to-cell (LV2C) system architecture is shown in Figure

3.1. Each module is represented by a group of cells from B_{M1} to B_{Mn}. Typically, a battery pack will have 8 modules with 12 cells each to reach a total of 96 cells. The bidirectional cell balancing DC/DC converters precisely control the current pulled or provided to each cell in a module, eliminating the inrush current issues seen in switched capacitor balancing. The LV battery is used as a buffer to allow quick sourcing or sinking of current needed by the cell balancing DC/DC converter (which can be rated for LV), without the need to charge or discharge the whole HV pack for each cell balancing operation. The control is flexible, allowing for direct charge and discharge of any odd cell and indirect balancing of even cells. Balancing time can be drastically reduced when compared to traditional C2C methods since the charge is not shuttled through each cell in the stack.

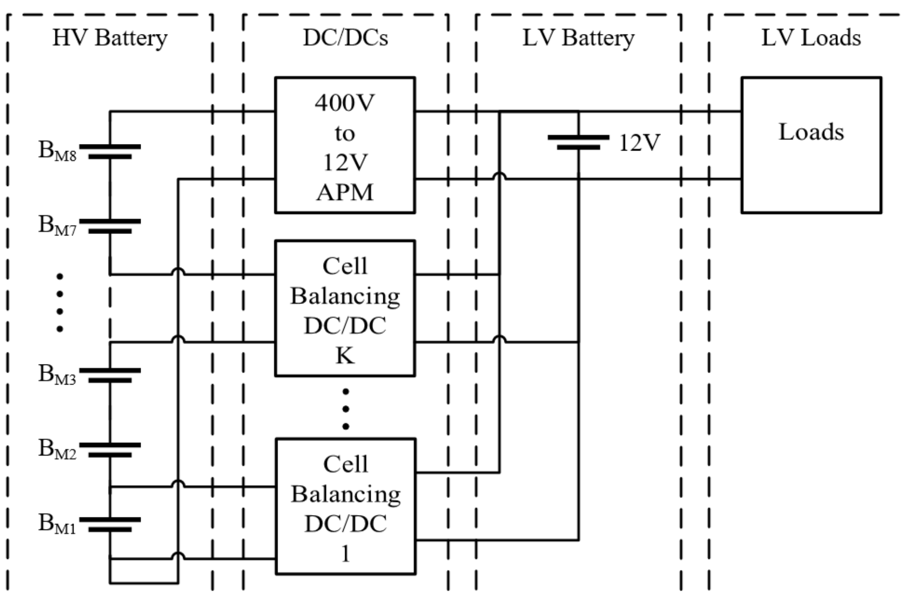


Figure 3.1: LV2C System Architecture

3.2 Proposed Topology

The proposed circuit is shown in Figure 3.2. A bidirectional cell balancing DC/DC converter must be used to source and sink current in both directions, allowing for precise control of each cell. Isolation is required to adhere to automotive standards, ensuring that the ground of the HV pack is isolated from the 12V battery. Figure 3.2 shows the DC/DC converter as a box, since any bidirectional isolated converter topology could feasibly be used. The high side of the DC/DC converter is connected through a bilateral switch to the top of each odd-numbered cell, while the low side is connected through a bilateral switch to the top of each even cell. Bilateral switches, composed of two back-to-back switches, are required to allow full control of the current for any cell, similar to the LC resonant circuit proposed in [43].

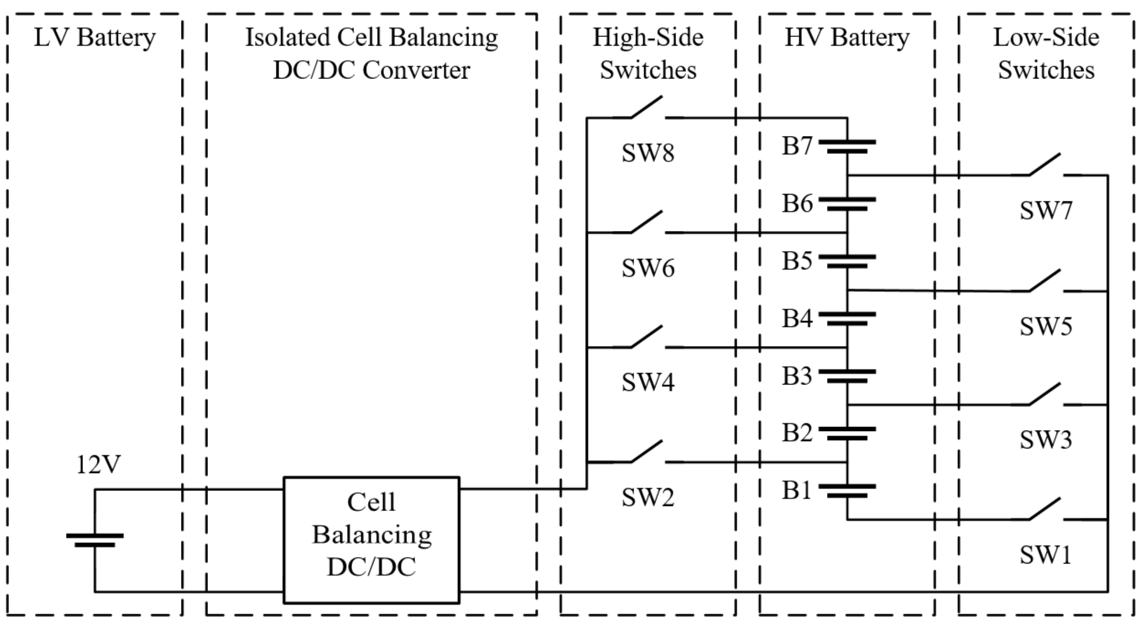


Figure 3.2: LV2C Circuit Architecture

Battery cell balancing circuits usually control equalization by voltage or state-of-charge (SOC) [21], where SOC control is generally preferred because it does not depend on the instantaneous terminal voltage of a cell, which can change during driving transients [64]. The proposed circuit controller can select the cell to be charged or discharged based on the estimated cell SOC. The control for the circuit is divided into odd and even cell control. Odd cells can be charged or discharged directly, one at a time, by closing the switches on the positive and negative sides of the cells to connect the cell to the output of the cell balancing DC/DC converter. Since the selected cell balancing DC/DC converter connection outputs a positive voltage only, the converter cannot directly charge or discharge even numbered cells because they are connected in opposite polarity. Instead, the even cells are charged or discharged in a 3-step process which is detailed in the Proposed Control section, where a stack of three cells is charged or discharged to the desired SOC of the middle (even) cell, and afterwards the cell balancing DC/DC converter controls the odd cells back to their desired setpoints.

When compared against existing cell balancing circuits, LV2C is advantageous. LV2C achieves a faster balancing time across the pack and better simulated efficiency when compared to AC2C and DC2C, which comes at the cost of additional switches. It greatly reduces the number or complexity of transformers when compared to C2P, P2C and LVC due to having a trade-off of lower efficiency. In general, LV2C strikes a balance between these two groups of cell balancing methods.

To select the desired cell from the module to connect to the DC/DC converter, a switch matrix is required. The design and component selection for the switch matrix is described below.

3.3 Switch Matrix Design

3.3.1 Switch Matrix Topology Selection

To reduce component count of the switch matrix PCB, only one connection per cell terminal is used. An additional 8 switches would be needed to reverse the polarity of the DC/DC converter output lines, which is undesirable. Thus, the intent of the lines are to serve as DC/DC converter rails; one being positive and one being negative.

This results in a wider required output voltage range for the DC/DC converter, but allows the reduction of switches. The cell balancing converter must be able to output 3 - 4 V for odd cell operations, and 9 - 12 V for even cells.

3.3.2 Principles of Operation

Odd cells in the stack have a direct connection from the top of the cell to the positive rail of the DC/DC converter, as well as the negative rail. However, even cells do not have such a connection. Therefore, even cells must be accessed through the charge and discharge of the odd cells above and below.

In order to block any voltage present on the DC/DC rails from the battery terminals, as well as maintain bi-directional current capability, two NPN mosfets are placed back-to-back. For this design, the sources and gates are tied together such that only one gate driver is required. Thus, by providing voltage above the threshold voltage of V_{THR}, the mosfets will be closed. The SI8271AB gate driver has a wide input voltage range of 2.8 - 5.5V, allowing for both 3.3V or 5V logic levels to be used. In the proposed circuit, 5V is used due to the lower limit of 4.75V on the Opal-RT OP4510 digital outputs. The gate driver also has a wide input range for the driver supply voltage of 9.5 - 30V, where 12V is used for the application.

3.3.3 Non-Ideal Transients

The purpose of the switch matrix is to connect the output of the cell balancing DC/DC converter with the cell. However, the output of the DC/DC converter contains output filtering capacitors which are susceptible to large current spikes. Thus, it is critical that the output voltage of the DC/DC converter match the cell voltage, or stack of cells. If V_{Cout} differs greatly from the cell voltage, closing the switch matrix bilateral switches will cause a large dV/dt and a large current entering into the filtering capacitors. This will cause irreversible damage to the capacitors, blowing the protection fuse and rendering the LV2C circuit unable to balance. Therefore, the control algorithm should implement a pre-charge step to avoid unwanted transients. It should read V_{Cout} from the DC/DC converter and compare it to the desired cell voltage before closing the switches.

3.3.4 Component Selection

Voltage present on the DC/DC converter rails must be blocked with bidirectional switches. This consists of two NPN mosfets back-to-back. Typically, the sources and drains of the mosfets are tied together to allow for unified control. This mosfet topology was selected for the switch matrix.

In order to reduce PCB size, a dual NPN mosfet package was selected. The BSO604NS2 mosfet from Infineon Technologies features two NPN mosfets in a single 8SOIC package [65], which aids in lowering part count and layout size. A suitable high-current gate driver from Silicon Labs, SI8271AB [66], was chosen to drive both mosfets.

The control of the switch matrix comes from the Opal-RT OP4510 hardware-in-the-loop (HIL) setup. Its inputs and outputs are DB-37 connectors, thus a DB-37 connector is needed to give digital outputs to the switches, as well as read cell voltages and send them as analog inputs.

3.4 DC/DC Converter Design

3.4.1 Converter Topology Selection

In principle, any DC/DC converter that is both isolated and bidirectional can be used for the connection between the LV 12V lead-acid battery and the switch matrix. Several types of converters meet these requirements: the flyback converter, half-bridge converter, and full-bridge converter. These topologies are presented below, and a DC/DC converter is selected.

The flyback converter can be seen in Figure 3.3. Featuring only 2 low-side switches and a wide operating range, the flyback can produce the required voltage output for both single-cell and three-cell connections. It can use asynchronous or synchronous switching schemes. The drawback is that the flyback is known to have a high voltage stress on the primary side switch [67]. However, it is suitable for the proposed circuit since low voltages are used and the voltage spike would be contained within the rated module voltage of 60V. It also requires larger filtering components due to the nature of the large ripples in switched current over the transformer. Despite these drawbacks, the flyback was chosen due to its low component count and simple control, which is advantageous for the design.

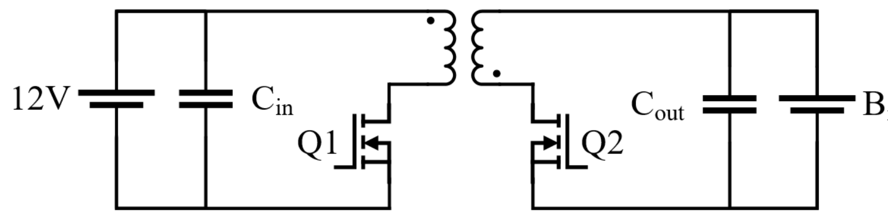


Figure 3.3: Flyback Converter Topology [67]

The half-bridge converter (HBC) can be seen in Figure 3.4. It requires 4 switches and 4 capacitors to operate. Synchronous switching must be used for the HBC design due to the increased risk of shoot-through. It also features high-side switches which have an increased design requirement for the gate driver. Due to the complex control scheme, typically using a phase-shifted technique, the filtering requirement at the input and output are far less than the flyback converter. When operated efficiently and not at light loads, zero-voltage switching (ZVS) can occur on the primary and secondary sides and thus provide increased efficiency [68]. One drawback is the inclusion of capacitors in series with the current path. These capacitors must be durable; they must be able to handle high current pulses and large voltage changes.

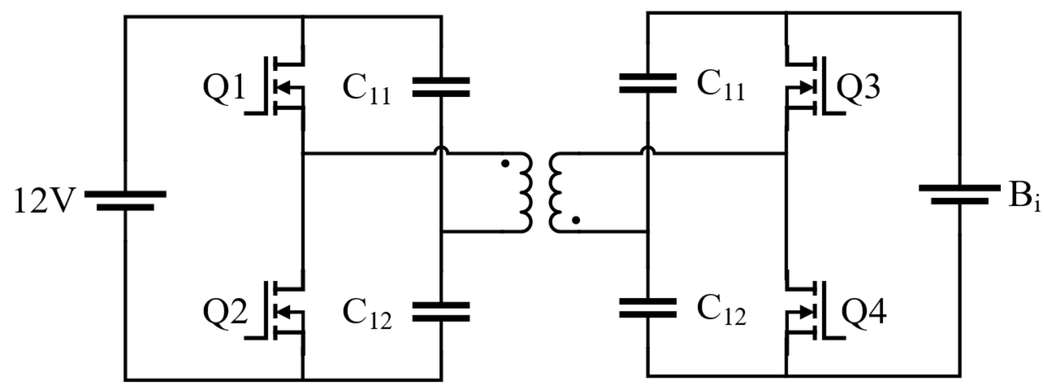


Figure 3.4: Half-Bridge Converter Topology [68]

The full-bridge converter (FBC) can be seen in Figure 3.5. The FBC uses 8 switches for operation. Similar to the HBC, the FBC can use phase-shifted technique. However, the additional switches grant increased control flexibility that can ultimately lower the filtering requirements below that of HBC, and the flyback. The FBC can leverage ZVS on all mosfets to achieve the highest efficiency of all presented converters [68]. However, its component count is costly and 4 high-side switches require a detailed gate driver design.

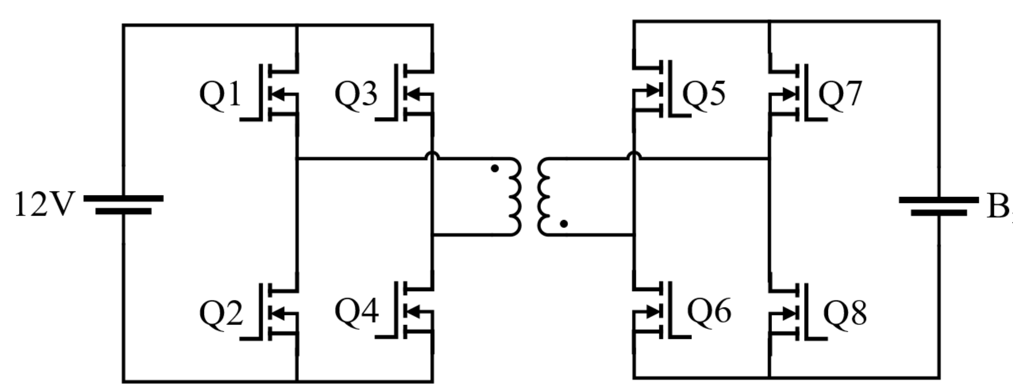


Figure 3.5: Full-Bridge Converter Topology [68]

To align with the desired low component count, the flyback converter was chosen. The flyback will be used to demonstrate that incredibly high-efficiency active balancing is not needed, since at a system level active balancing can provide significant benefits to driving range.

3.4.2 Principles of Operation

3.3.3.1 Derivations

An ideal converter will have a relationship between the input and output voltages described by Equation 3.4.1.

$$V_{OUT} = V_{IN} * D \tag{3.4.1}$$

Where V_{IN} is the 12V input voltage from the LV lead-acid battery, V_{OUT} is the desired voltage of the cells (single or three-cell), and D is the duty cycle, defined by Equation 3.4.2.

$$D = \frac{T_{ON}}{T_S} \tag{3.4.2}$$

Where T_{ON} is the time that the primary switch is on and T_S is the total period of the switching cycle. Equations 3.4.3 and 3.4.4 relate other parameters to these timing values.

$$T_S = T_{ON} + T_{OFF} \tag{3.4.3}$$

$$T_S = \frac{1}{f_s} \tag{3.4.4}$$

Where T_{OFF} is the period of time that the primary switch is off, and f_s is the switching frequency. For this application, the switching frequency was chosen to be 100kHz.

The non-ideal flyback duty equation will include the losses over the secondary side diode, as well as the turns ratio of the transformer. Equation 3.4.5 demonstrates this relationship.

$$D = \frac{(V_{OUT} + V_{FD}) * N_{PS}}{V_{IN} + (V_{OUT} + V_{FD}) * N_{PS}} \tag{3.4.5}$$

Where V_{FD} is the voltage drop over the diode and N_{PS} is the turns ratio of the transformer, defined by Equation 3.4.6.

$$N_{PS} = \frac{N_P}{N_S} = \frac{V_P}{V_S} \tag{3.4.6}$$

Where N_P is the turns of the primary side, and N_S is the number of turns on the secondary side. In an ideal transformer, the turns ratio also represents the ratio between the primary side input voltage V_P and the output voltage on the secondary side V_S. Due to the wide nature of the output voltage, two values must be explored: the minimum voltage for a single-cell operation, and the maximum voltage for a three-cell operation. These voltages correspond to 3V and 12V outputs from a 12V input voltage. Therefore, the turns ratios can be calculated using Equations 3.4.7

and 3.4.8.

$$N_{PS,O} = \frac{12V}{3V} = 4:1 \tag{3.4.7}$$

$$N_{PS,E} = \frac{12V}{12V} = 1:1 \tag{3.4.8}$$

The largest turn ratio must be used to ensure that the full voltage range is available for all operations. Thus, the 1:1 ratio is chosen for the turns ratio of the DC/DC converter.

3.3.3.2 Conduction Modes

There are three different operations of a flyback converter; discontinuous conduction mode (DCM), boundary conduction mode (BCM), and continuous conduction mode (CCM)[69][70]. DCM happens when the current of the primary inductor reaches zero before the next switching cycle. This can be seen in Figure 3.6. During DCM, t_{OFF} is a large enough time to allow for the transformer to fully demagnetize. The demagnetizing time t_{DEMAG} is the time it takes for the secondary current I_{SEC} to reach zero, while the additional time between t_{DEMAG} and the next switching cycle is called the dead time t_{DEAD}. DCM allows for the smallest transformer since continuous current does not need to be sustained by the core. However, the primary side switch is hard-switched and lowers the overall efficiency. In addition, the ripple current over the output capacitor is larger than continuous mode since peak current is also larger. This larger filter is required due to the large voltage ripples seen during the t_{DEAD} period, which reflect onto the output side.

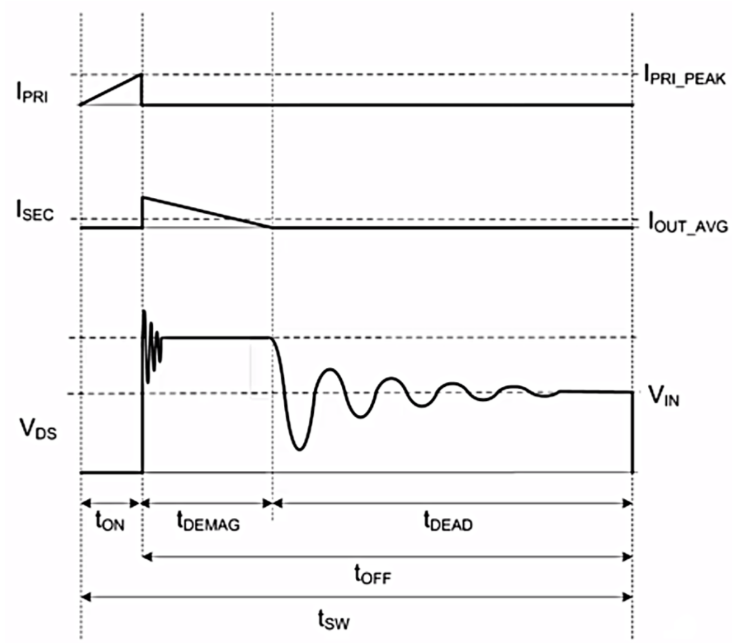


Figure 3.6: Flyback DCM [70]

BCM is on the boundary of DCM and CCM, where there is no dead-time after the current of the inductor reaches zero. This conduction mode can be seen in Figure 3.7. In BCM, t_{OFF} is exactly equal to t_{DEMAG} and the next switching cycle begins before the large oscillations on the switch. It harnesses the benefits of DCM while being efficient with timing. Controlling BCM is more complex than DCM since the frequency should be varied to accommodate for the exact moment the inductor current reaches zero. This requires a feedback loop, leading to a specialized gate driver design. BCM can increase the efficiency when compared to DCM if it employs specialized control, such as valley switching [70], to reduce switching losses.

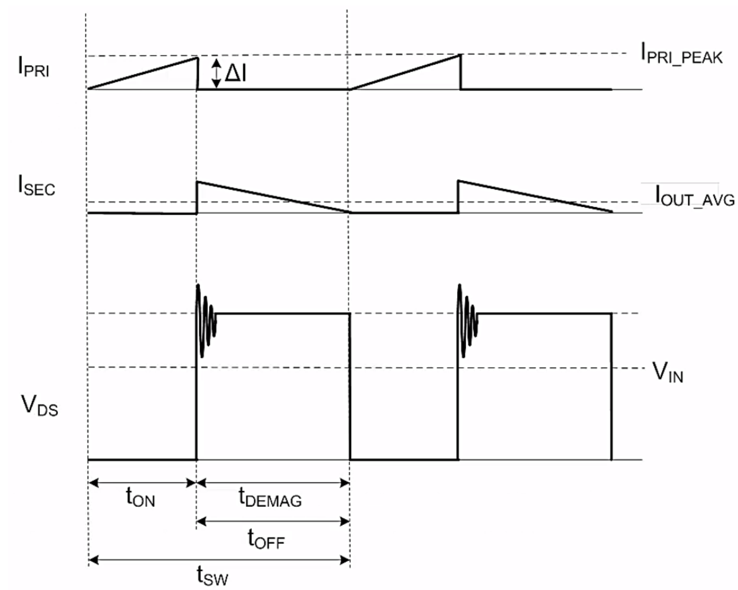


Figure 3.7: Flyback BCM [70]

CCM has a continuous current present across the transformer. This method can be seen in Figure 3.8. It is evident that the transformer currents I_{PRI} and I_{SEC} do not reach zero. I_{PRI} and I_{SEC} also typically have a reduced ripple current, since the required output current is the average of I_{OUT}. In DCM, larger peak currents are required to sustain the same average I_{OUT}. While output current ripple is smaller, CCM requires a larger transformer to sustain the output current. The control can also be difficult due to the inherent instability of the right half plane zero [70]. However, the advantage is that it requires much smaller filtering.

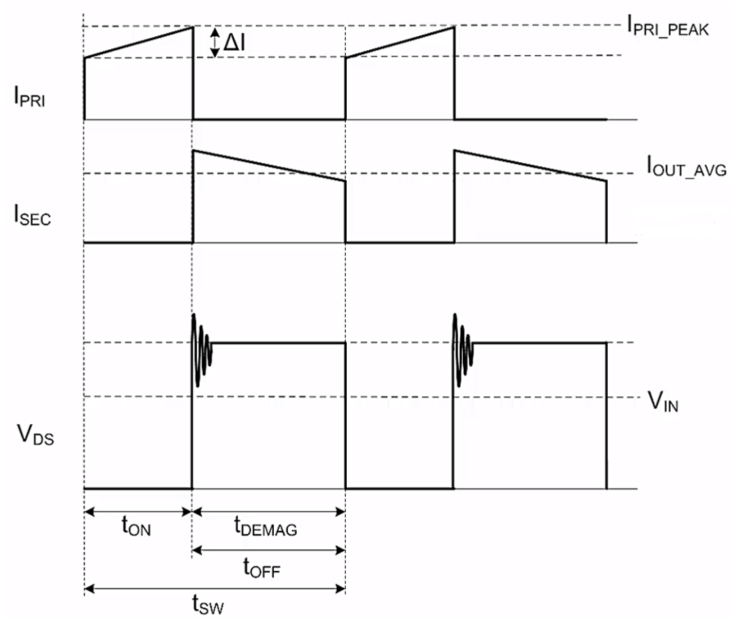


Figure 3.8: Flyback CCM [70]

DCM was chosen to minimize the transformer size and cost. A larger output ripple due to DCM operation will require a larger filtering capacitor. However, the lowered cost and rating of the transformer outweighs this trade-off.

3.3.2.3 Active Paths

The operating modes of the DCM flyback DC/DC converter can further be divided into four modes; no load, primary switch on, primary switch off and dead time. These modes can be seen in Figure 3.9 and demonstrate the active current paths during a charging operation. The modes show Q1 acting as the primary switch during charging. For brevity, the active paths for discharge are not shown since the only difference would be to have Q2 act as the primary switch.

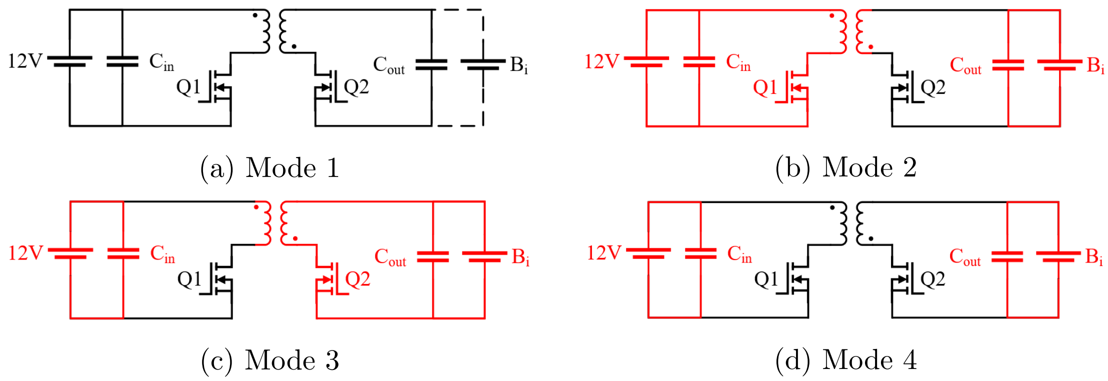


Figure 3.9: Active Paths of DCM Operation

During mode 1, the battery is disconnected from the battery balancing circuit by opening the switch matrix. The dashed line demonstrates this opening. No current paths are active during mode 1.

Once the switch matrix is closed and a charging operation is required, Q1 will act as the primary switch in mode 2. Q1 is turned on and allows current to pass in the time period t_{ON} in Figure 3.6. The voltage of the 12V lead-acid battery is applied over the primary side of the transformer, and thus the inductor current rises. The rising inductor current stores energy in the transformer.

During mode 3, Q1 is turned off and the stored energy of the transformer is passed to the secondary side. Mode 3 occurs during t_{DEMAG} in Figure 3.6 The primary side inductor current is abruptly stopped, and the current is passed to the secondary side with some losses. The active path on the secondary side is either through the closed Q2 switch (synchronous control) or the Q2 diode (asynchronous control). Since there is no voltage applied over the primary side of the transformer, and thus none on the secondary side, the inductor current on the secondary side decreases.

Mode 4 is characterized by the t_{DEAD} time period in Figure 3.6. Both switches are off and the transformer is not conducting. However, the filtering capacitors can provide an active current path to the input and output batteries.

During discharge, the same modes are employed with small changes. During modes 2 and 3, the active paths are mirrored through the center of the transformer. Mode 2 would have Q2 on during the t_{ON} period of Figure 3.6. Mode 3 would have Q2 off, allowing current to pass through Q1 during t_{DEMAG}. Currents shown in Figure 3.6 are swapped, thus the primary current rising during t_{ON} would be the secondary current rising to discharge the battery cell(s). Filtering still occurs during the t_{DEAD} time period, as shown in mode 4.

3.4.3 Non-Ideal Transients

Consideration should also be given to the voltage spike and ringing of the flyback. The voltage spike should not exceed 60V in experimental measurements and the ringing should be filtered at the output of the flyback DC/DC converter in order to not affect the cell. The ringing appearing in the switching waveforms can be characterized by two distinct sections; high frequency and low frequency [67]. The voltage spike is part of the initial high frequency ringing that is due to transformer leakage inductance and parasitic inductance of the PCB. Low leakage inductance is desired in the transformer.

3.4.4 Component Selection

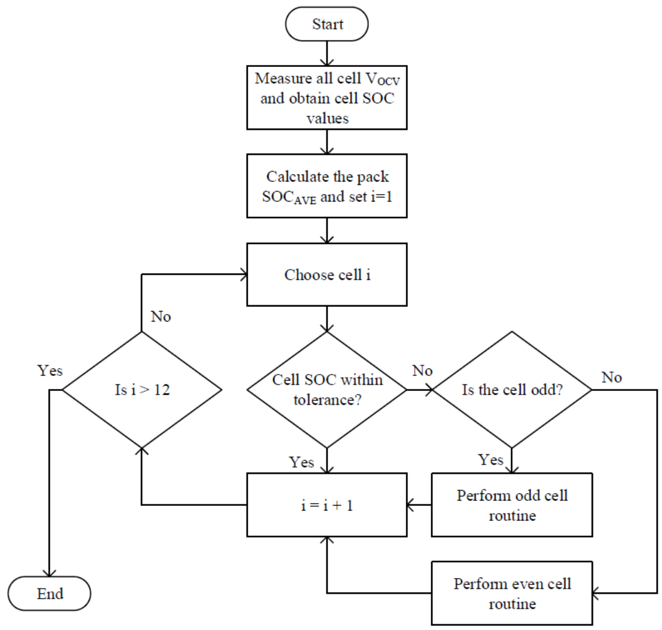
Due to the well-known voltage stress placed on the flyback primary switch during operation, mosfets chosen for the flyback must be able to handle more than the required output of 12V. To align with the module rated voltage as well as this potential spike, a voltage rating of 60V was chosen. The B80N06S2L switch from Infineon technologies was used with the SI8271AB gate driver on the DC/DC converter PCB

[71] [66]. Since the input is the 12V lead-acid battery, the flyback will be operating in buck mode. However, the high output voltage of 9 - 12V for a three-cell connection means that the transformer used in this case must have a 1:1 turns ratio. The power transformer 750312504 from Wurth Elektroinik was chosen for this application [72].

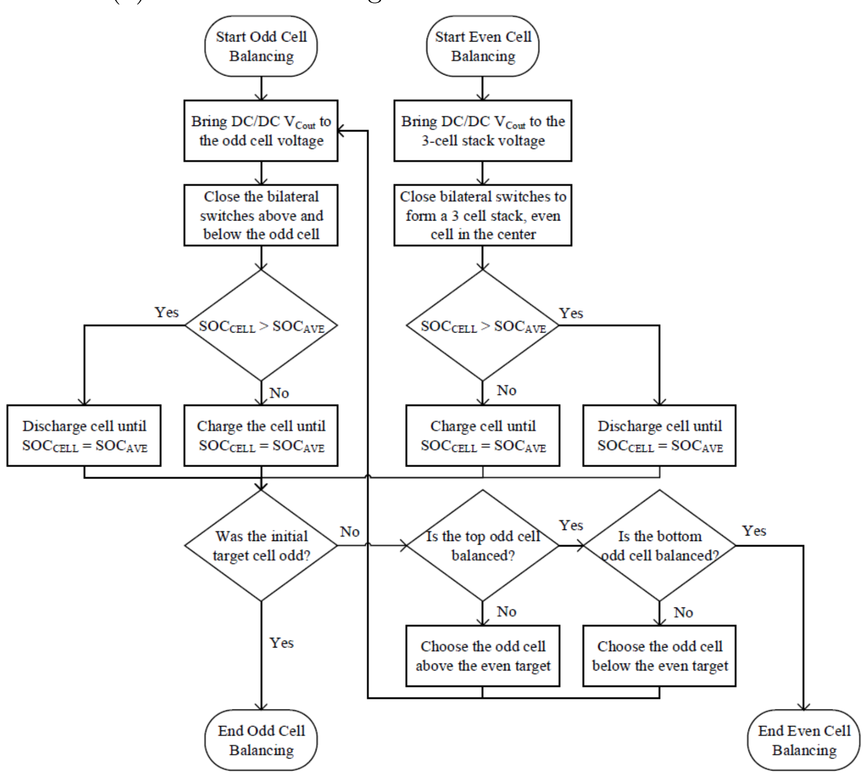
3.5 Proposed Control

The flowcharts seen in Figures 3.10a and 3.10b will be used to demonstrate the control algorithm for the LV2C circuit. Figure 3.10a shows the algorithm from a module level. The code routinely checks which cells need balancing by first measuring each cell voltage, estimating its SOC value, and comparing these with the average pack SOC. For each cell, if the cell isn't within the tolerance value of the average pack SOC, then balancing must be performed. If the cell is odd, the odd cell operation is performed. Likewise, with even cells. Afterwards, the next cell is chosen in the stack. This rule-based algorithm was performed on the vehicle model. However, in the experimental work, the algorithm found the cell with the SOC furthest away from the desired SOC and balanced this cell first. There are many ways the algorithm can choose to balance the cells.

On the cell level, Figure 3.10b shows the steps required to perform balancing on both even and odd cells. First, the output voltage V_{Cout} of the cell balancing DC/DC is controlled to the desired cell voltage(s). Next, the bilateral switches are closed. Charging or discharging operations are chosen and performed. If the target cell is odd, the balancing is finished. If the target cell is even, then additional odd cell balancing must be performed on the odd cells above and below the target cell. After these three balancing operations, the even cell algorithm is finished.



(a) Module Level Algorithm



(b) Cell Level Algorithm

Figure 3.10: Balancing Algorithms

3.5.1 Odd Cell Control

For example, to charge cell B3 in Figure 3.11, the output voltage of the cell balancing DC/DC converter is controlled to be approximately equal to the voltage of B3, then bilateral switches 3 and 4 are closed. Energy is transferred to or from the LV battery into B3 at a controlled rate to the desired SOC for B3. When the charging of B3 is complete, switches 3 and 4 are opened.

3.5.2 Even Cell Control

To charge cell B2 in Figure 3.12, switches 2 and 3 cannot be closed because this would attach the negative end of the cell to the positive output of the cell balancing DC/DC converter. Instead, switches 1 and 4 select a stack of three cells after the output voltage of the cell balancing DC/DC converter is matched to the sum of the three cell voltages. Energy is transferred to or from the LV battery into B1, B2 and B3 until the desired SOC of B2 is reached. Afterwards, additional steps are needed to bring the SOCs of B1 and B3 back to their desired setpoints. While this adds steps to the balancing algorithm, the reduced complexity of the switch matrix and reduced components were more desirable.

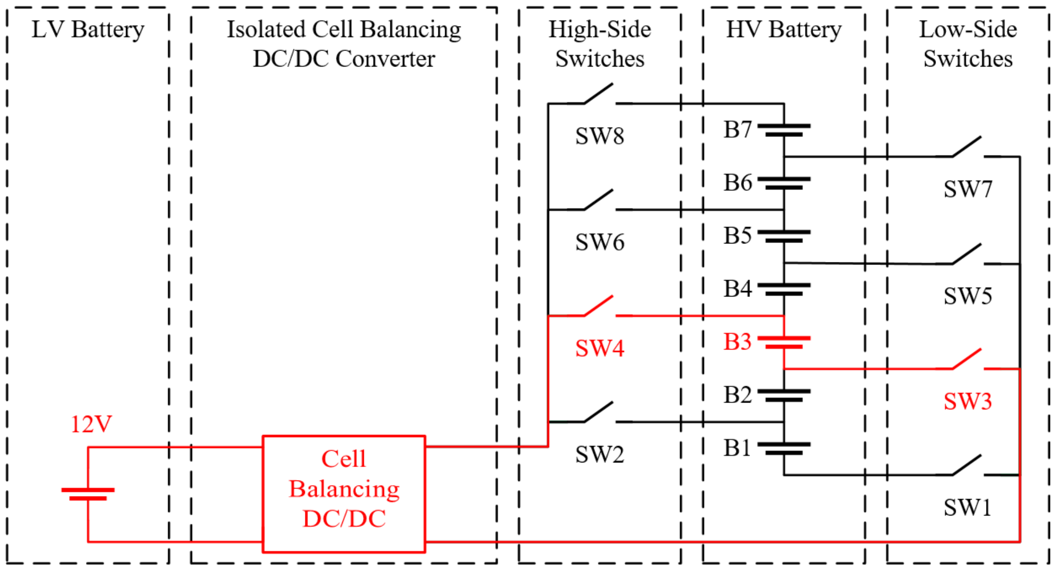


Figure 3.11: LV2C Odd Cell Selection

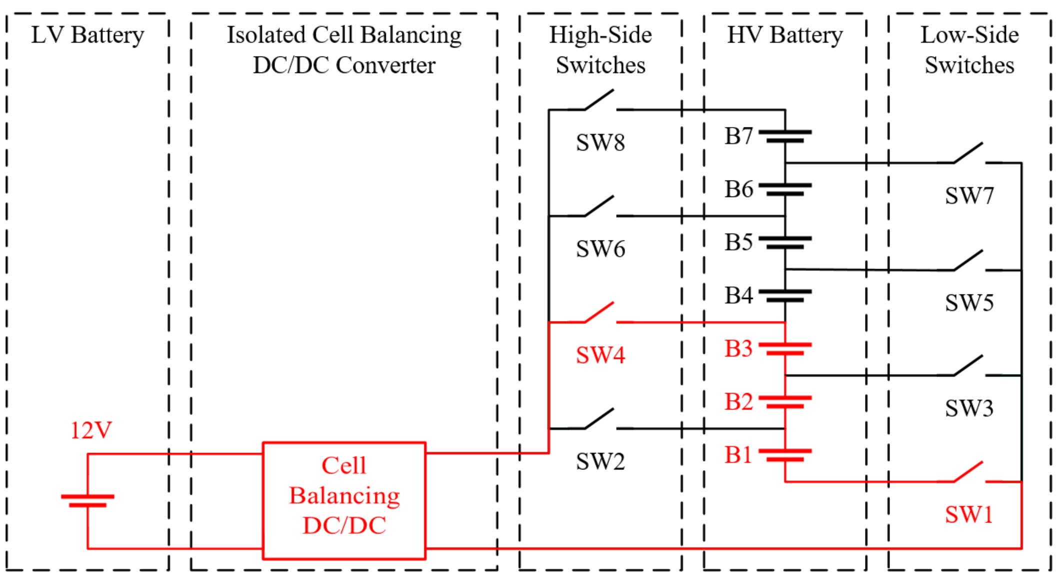


Figure 3.12: LV2C Even Cell Selection

3.6 LV2C Simulations

3.6.1 DC/DC Converter

The DC/DC converter was simulated in PSpice in order to approximate the ringing of the primary and secondary mosfet voltages, which is difficult to obtain in the PSIM or Matlab environments.

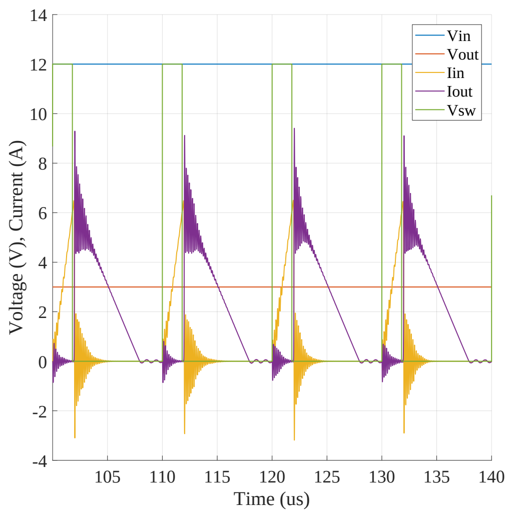
The values used in the PSpice environments are summarized in Table 3.1. The IPP80N06S2L model was downloaded from the Infineon website, and thus is an extremely accurate model of the switch. The output voltage sources are shown as 3, 4, 9, and 12V, which correspond to odd charging, odd discharging, even charging and even discharging operations. The properties of the 750312504 Wurth transformer were modeled with two coupled inductors with a leakage inductor and leakage resistor in series on either side of the transformer.

Table 3.1: PSpice DC/DC Properties

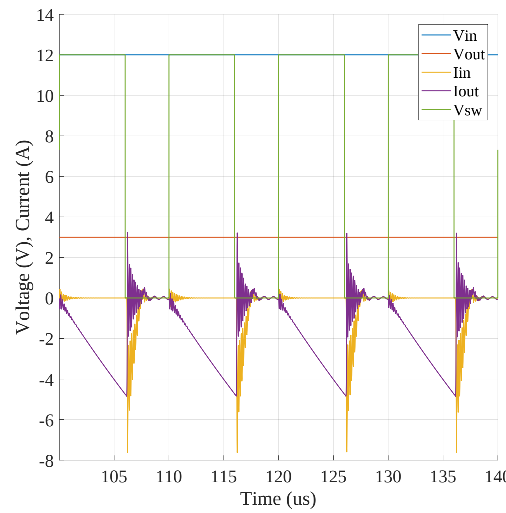
Annotation	Description	Value	Unit
V_{in}	Input Voltage Source	12	V
V_{out}	Output Voltage Source	3, 4, 9, 12	V
Q_i	Infineon MOSFET Model	IPP80N06S2L	N/A
N_{PS}	Turns Ratio	1:1	N/A
K_{PS}	Inductor Coupling	1	N/A
L_P	Primary Inductance	3.4	uH
L_{lk}	Leakage Inductance	120	nH
R_{DC}	Core Resistance	0.01	Ω
R_G	Gate Resistance	10	Ω

The simulations provided approximate waveforms seen in Figure 3.13. The input and output batteries are modeled as ideal voltage sources, and thus they appear as horizontal lines. The efficiency was calculated for each case, which is shown in Table 3.2. Figure 3.13c shows that the worst case maximum current limit will be just above 10A. Thus, the transformer was sized to have an upper limit of 10A, taking into consideration that the trace and wire losses will decrease the current, as well as core losses of the transformer.

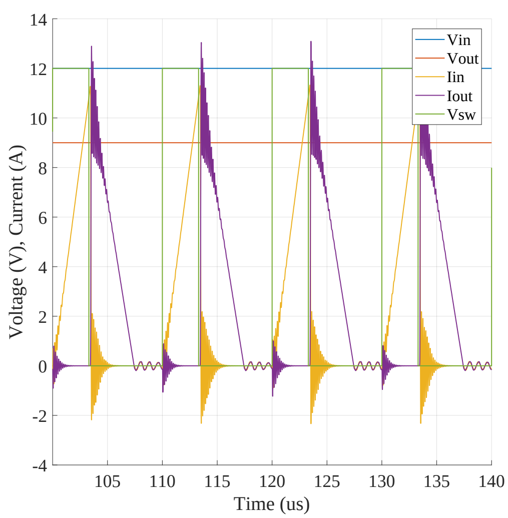
Note that the simulation efficiency reported in Table 3.2 shows that the DC/DC is more efficient during even cell operations than odd cell operations. This is due to the inherent inefficiency of the flyback buck operation; since approximately the same amount of current is transferred from primary to secondary side when the primary switch is turned off, the measured output power varies greatly based on the output voltage. The lower the voltage, such as 3V for the odd cell at low SOC, the lower the power on the output.



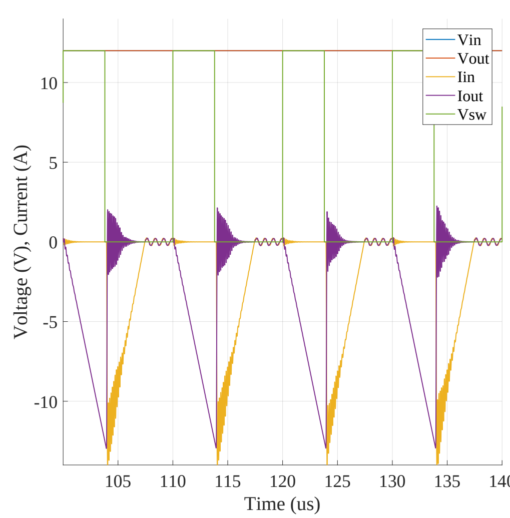
(a) 1 Cell Charge - Input and Output Waveforms



(b) 1 Cell Discharge - Input and Output Waveforms



(c) 3 Cell Charge - Input and Output Waveforms



(d) 3 Cell Discharge - Input and Output Waveforms

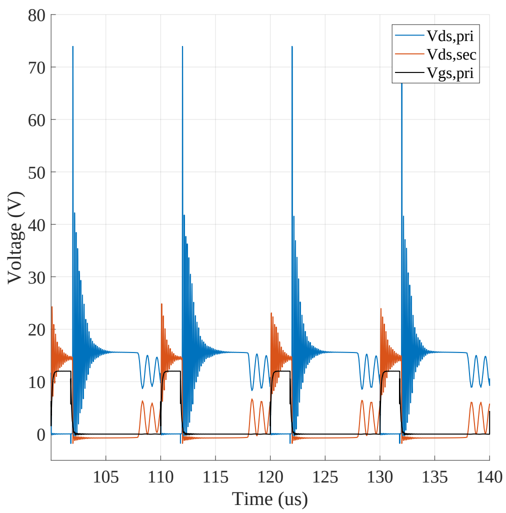
Figure 3.13: DC/DC Simulation - Input and Output Waveforms

Table 3.2: PSpice Efficiency

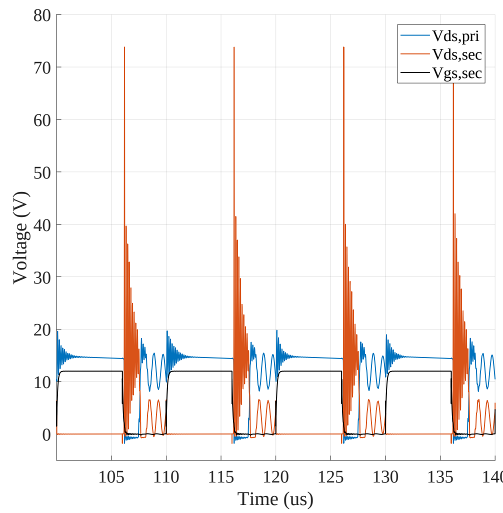
Cell Type	Test Case	Efficiency
Odd Cell	Charging	83.98%
	Discharging	80.56%
Even Cell	Charging	96.88%
	Discharging	94.63%

The primary and secondary switches will also be analyzed to determine whether a snubber circuit should be used. If the voltages in simulation return high voltage spikes, then a dissipative snubber should be used. However, if the voltage spikes are within the desired rated voltage of 60V, then the snubber does not have to be used. A snubber should be avoided when possible since it adds complexity and components to the design. Figure 3.14 shows the primary and secondary side switch voltages V_{DS} and V_{GS}, which correspond to the drain-source voltages and gate-source voltages. For charging, the primary switch is the first switch. During discharge, the secondary switch acts as the main switch and passes current back to the LV battery.

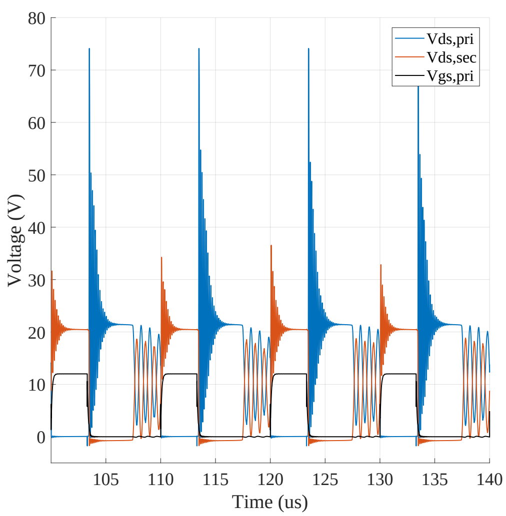
The simulated voltage spikes with ideal voltage sources show that the maximum voltage spike is less than 75V. Therefore, no snubber shall be used. The spikes in simulation exceed the rated module voltage of 60V. However, the expected voltage spike with lithium-ion cells as the load will be significantly smaller due to the capacitance of the cell reflected to the primary side. This will aid to lower the voltage spike, keeping the designed circuit within the desired rated voltage.



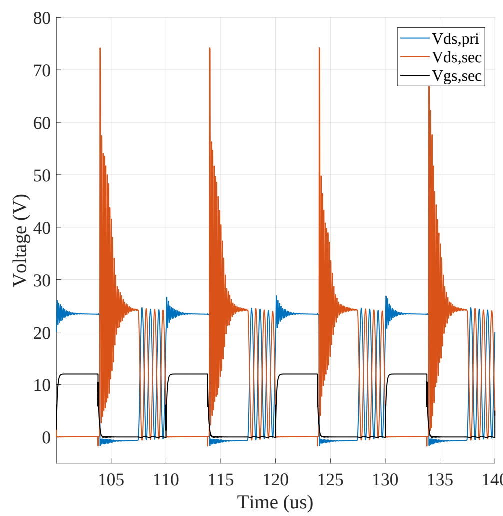
(a) 1 Cell Charge - Switching Waveforms



(b) 1 Cell Discharge - Switching Waveforms



(c) 3 Cell Charge - Switching Waveforms



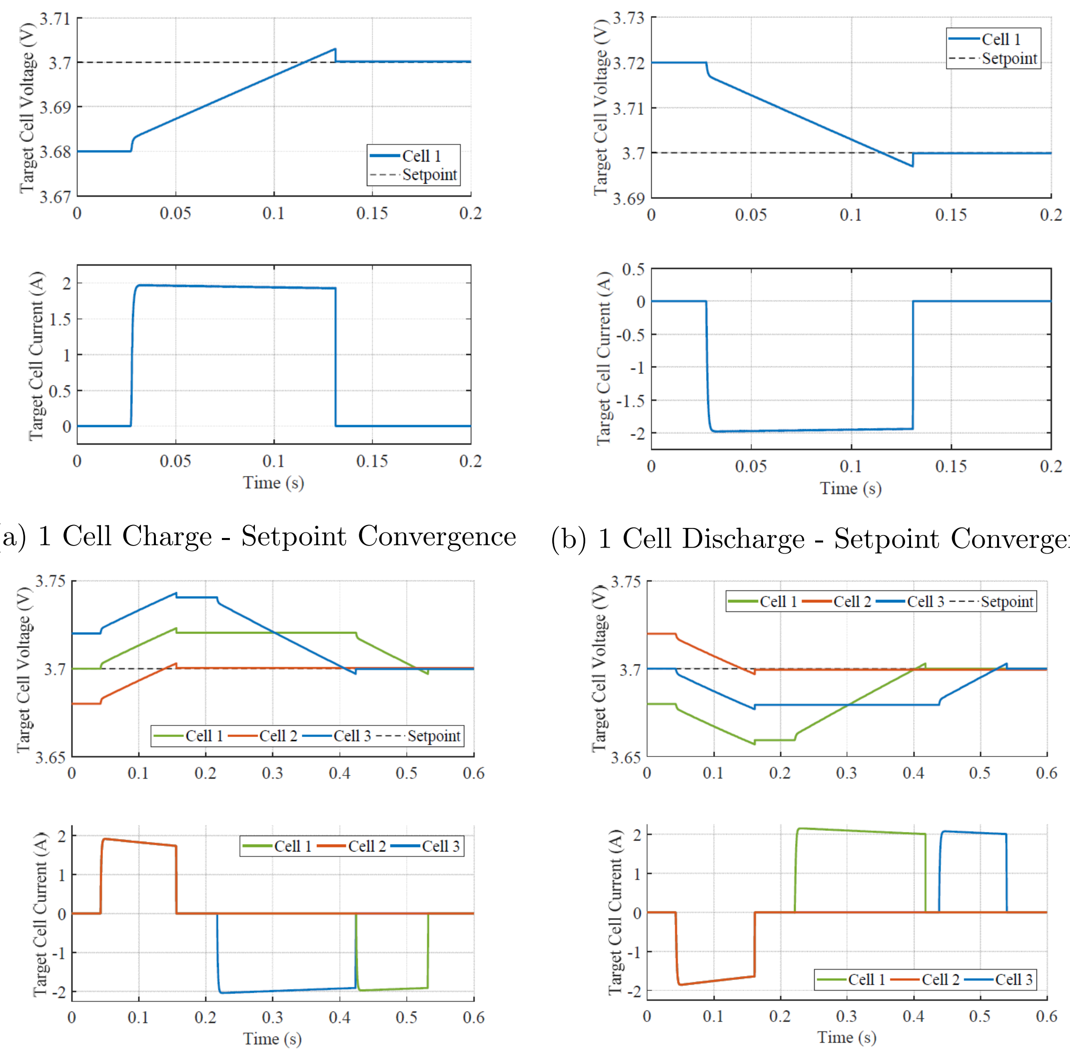
(d) 3 Cell Discharge - Switching Waveforms

Figure 3.14: DC/DC Simulation - Switching Waveforms

3.6.2 LV2C Operation

A simplified system model of the LV2C circuit was achieved in Matlab/Simulink. The odd and even cell charging and discharging waveforms can be seen in Figure

3.15. They demonstrate that the operations for selecting the cell and performing the algorithm can change the cell voltages, and thus SOC, to the desired setpoint. Figures 3.15c and 3.15d show that while charging or discharging an even cell, the odd cells above and below are effected. Thus, additional odd operations are needed as described by Figure 3.10b.

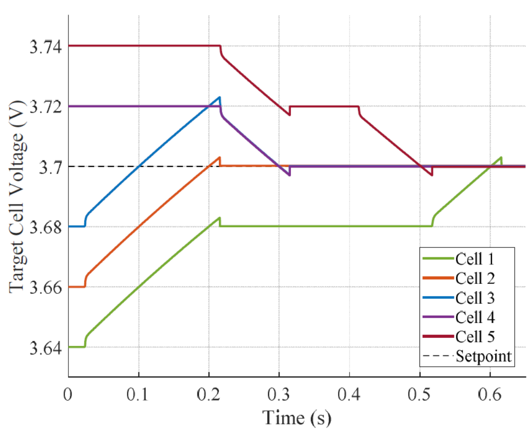


(a) 1 Cell Charge - Setpoint Convergence (b) 1 Cell Discharge - Setpoint Convergence

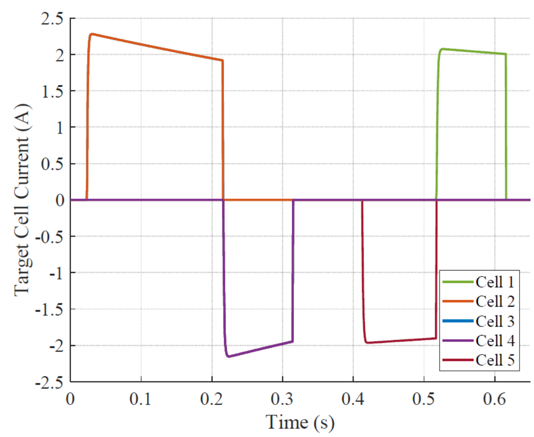
(c) 3 Cell Charge - Setpoint Convergence (d) 3 Cell Discharge - Setpoint Convergence

Figure 3.15: LV2C Simulations - Cell Cases

In addition, Figures 3.16a and 3.16b show that the cell convergence can be observed. Cells 2 and 4 are balanced first, then cells 1 and 5. Cell 3 is balanced through even cell operations. A brief gap in time is observed between the even and odd cell operations; between balancing cells 4 and 5. This small time step is to allow the voltage of the output filter capacitor, V_{Cout}, to discharge from a 3-cell voltage range to the voltage of a single cell, cell 5. Since the voltages between 3-cell and 1-cell operations are very similar, there is no need to change V_{Cout} between balancing cells 2 and 4, and cells 5 and 1. Thus, these operations can be performed immediately after each other.



(a) 5 Cell Convergence



(b) 5 Cell Balancing Current

Figure 3.16: LV2C Simulations - Cell Conversion

A potential reduction of operations by balancing all even cells first is evident in Figure 3.16a since cells 2 and 4 are addressed first before the odd cell operations are performed. From $t = 0$ to $t = 0.2$, cell 2 is charged. Cells 1 and 3 are also affected by this operation. While both of these cells need to be charged to reach the setpoint of 3.7V, cell 1 is brought below the setpoint and cell 3 overshoots the desired 3.7V. However, balancing cell 4 from $t = 0.2$ to $t = 0.3$ decreases the cell 3 voltage to the setpoint due to the discharge, as well as cell 5. In the end, cell 3 did not have an additional odd cell balancing operation performed on it, and thus some operations are reduced. Cells 1 and 5 are brought to the setpoint at the end. Balancing all similar voltage cells (or stacks of cells) allows for a reduction in transition timing due to little to no change in V_{Cout} required. Although the reduced-operation algorithm is not explored in the research, it is identified as an advantage for the LV2C topology.

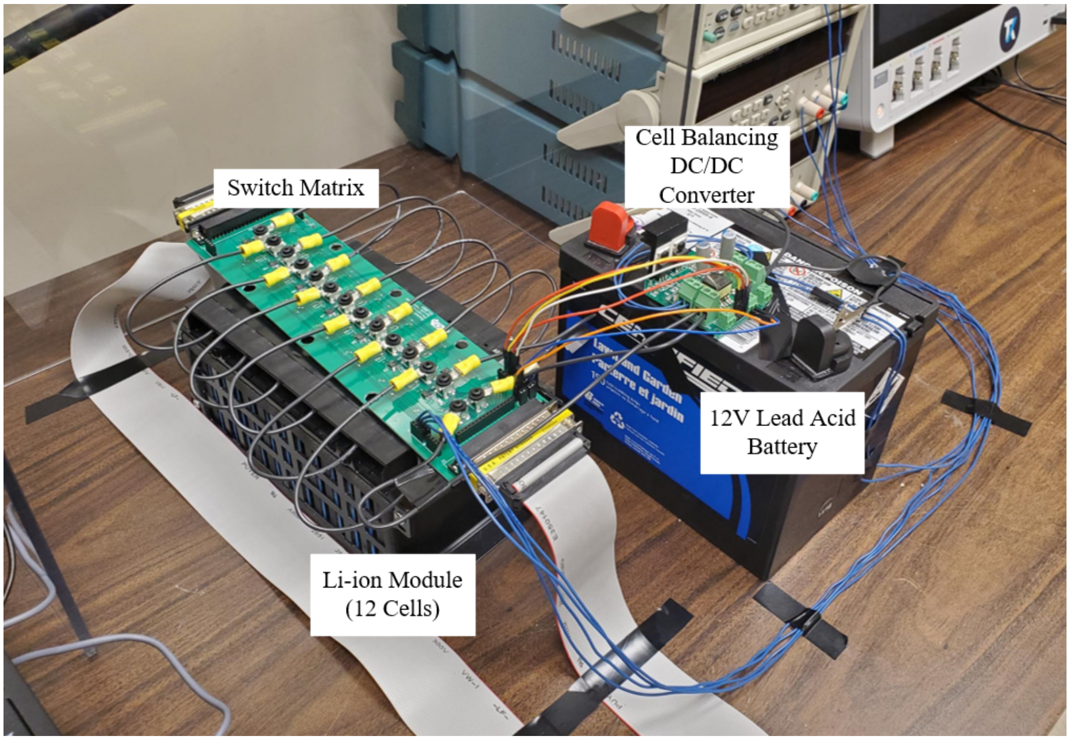
Chapter 4

Experimental Results

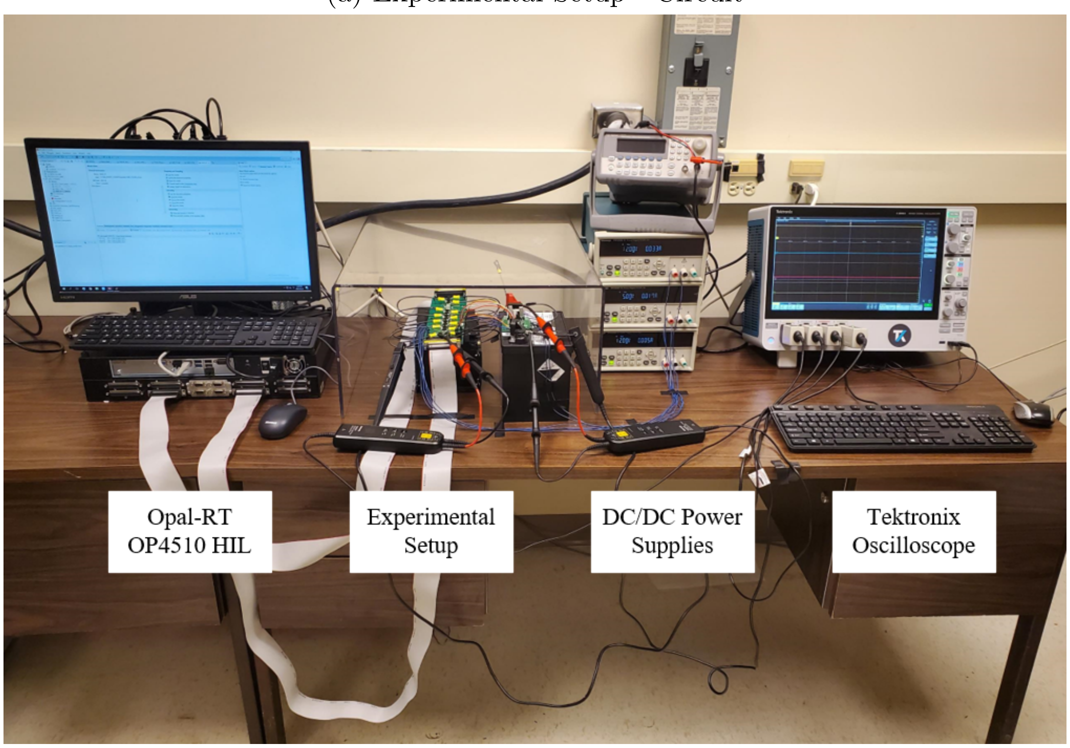
4.1 LV2C Prototype

4.1.1 Experimental Setup

In order to test the experimental setup, several cases were devised to test each portion of the proposed algorithm. Four test cases were needed; odd cell charging, odd cell discharging, even cell charging and even cell discharging. The experimental setup can be seen in Figure 4.1. It consists of two printed circuit boards (PCBs); one board is the switch matrix to select cells, and the other is the DC/DC converter. These can be viewed in Figure 4.1a. The controller used for the research is an Opal-RT OP4510 hardware-in-the-loop (HIL) system. The OP4510 acted as the BMS to read cell voltages, select cells as desired, and control the DC/DC converter using analog inputs and digital outputs. The data acquisition system was a Tektronix oscilloscope. The full experimental setup can be seen in Figure 4.1b.



(a) Experimental Setup - Circuit



(b) Experimental Setup - System

Figure 4.1: Experimental Setup

4.1.2 PCB Design

The DC/DC converter schematics can be seen in Figure 4.2 while the PCB can be seen in Figure 4.3. The dimensions of the DC/DC converter PCB were 54.9 mm by 66.4 mm, resulting in a total area of 3645.36 mm^2. The gate driver was placed physically close to the switch to try to eliminate trace inductance and ringing. The source net of the switch and gate driver was given a large area for heat dissipation.

The switch matrix schematics are separated into several pages; mosfet connections are shown in Figure 4.4, gate drivers and peripherals are seen in Figure 4.5, and all connectors for the board are shown in Figure 4.6. The switch matrix PCB is also divided into two figures due to its large size, seen in Figures 4.7 and 4.8. The PCB dimensions were large to accommodate the spacing of the battery pack connectors, and came out to 280.9 mm by 77.4 mm. The total area was 21,741.66 mm^2. There is a cutout in the middle of the board that represents the battery connections. This cutout was done to prevent voltage creep between adjacent traces by eliminating any planes near to the battery connections.

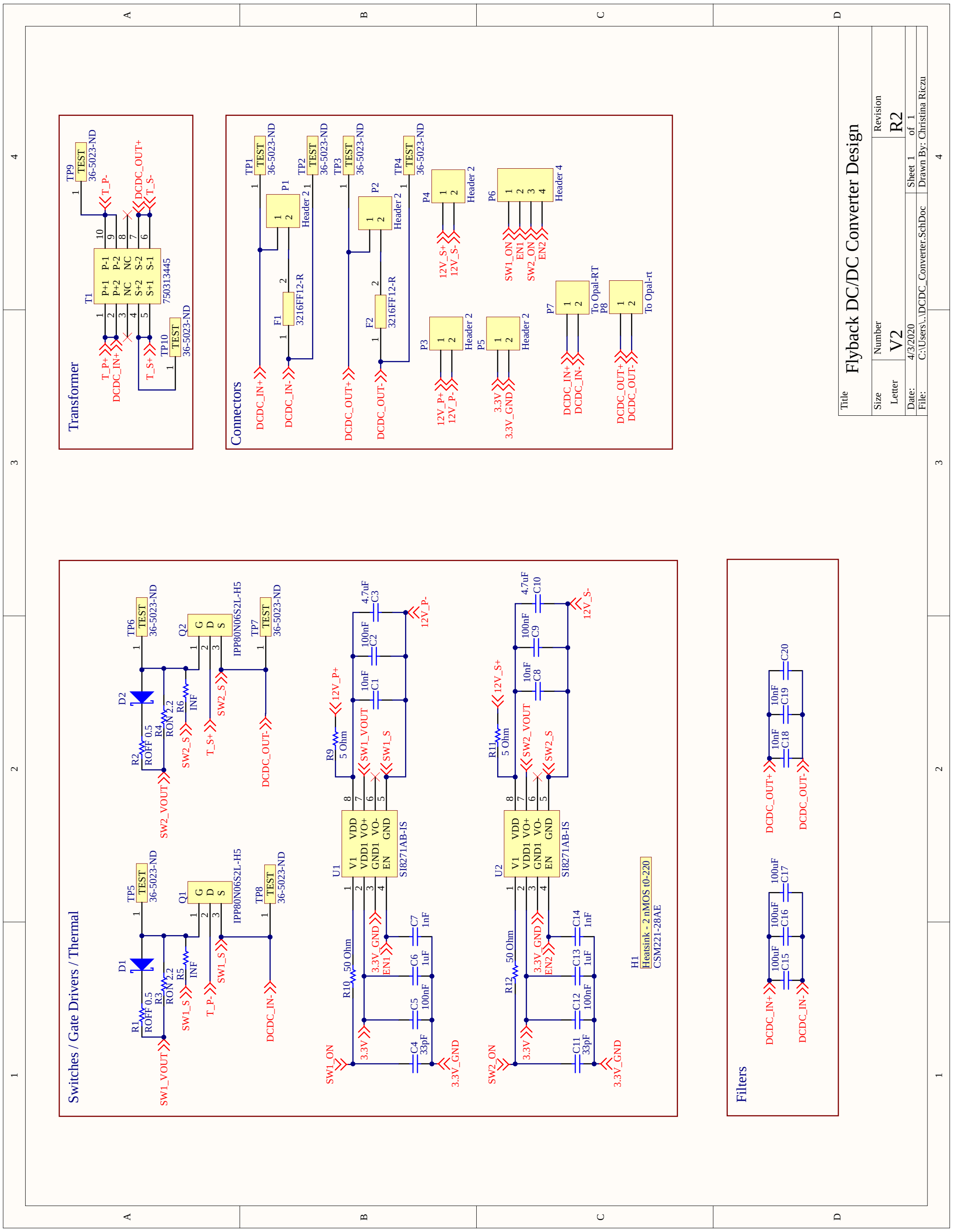
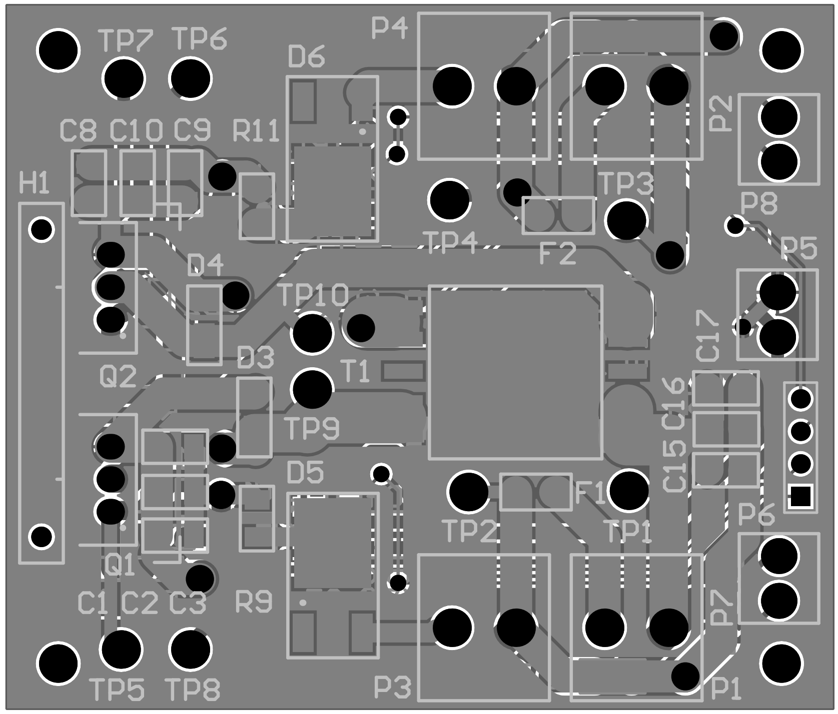
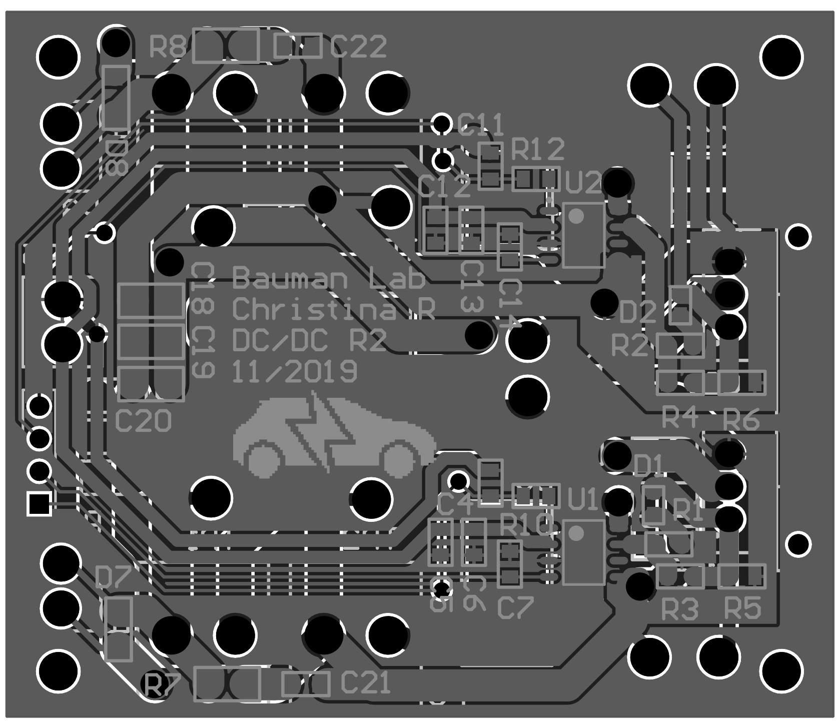


Figure 4.2: DC/DC Converter Schematic



(a) Top Layer



(b) Bottom Layer

Figure 4.3: DC/DC Converter PCB

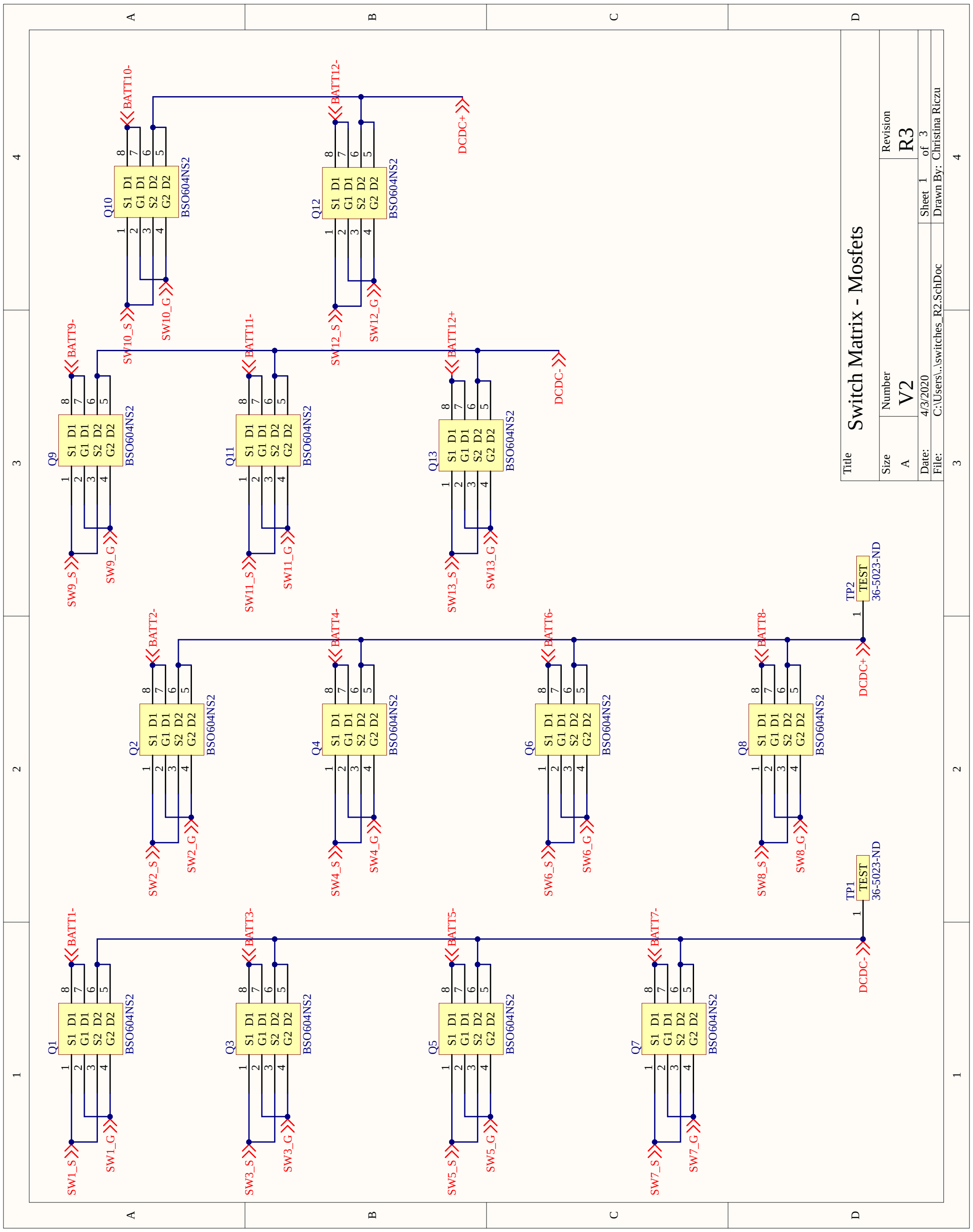


Figure 4.4: Switch Matrix Schematics - Mosfets

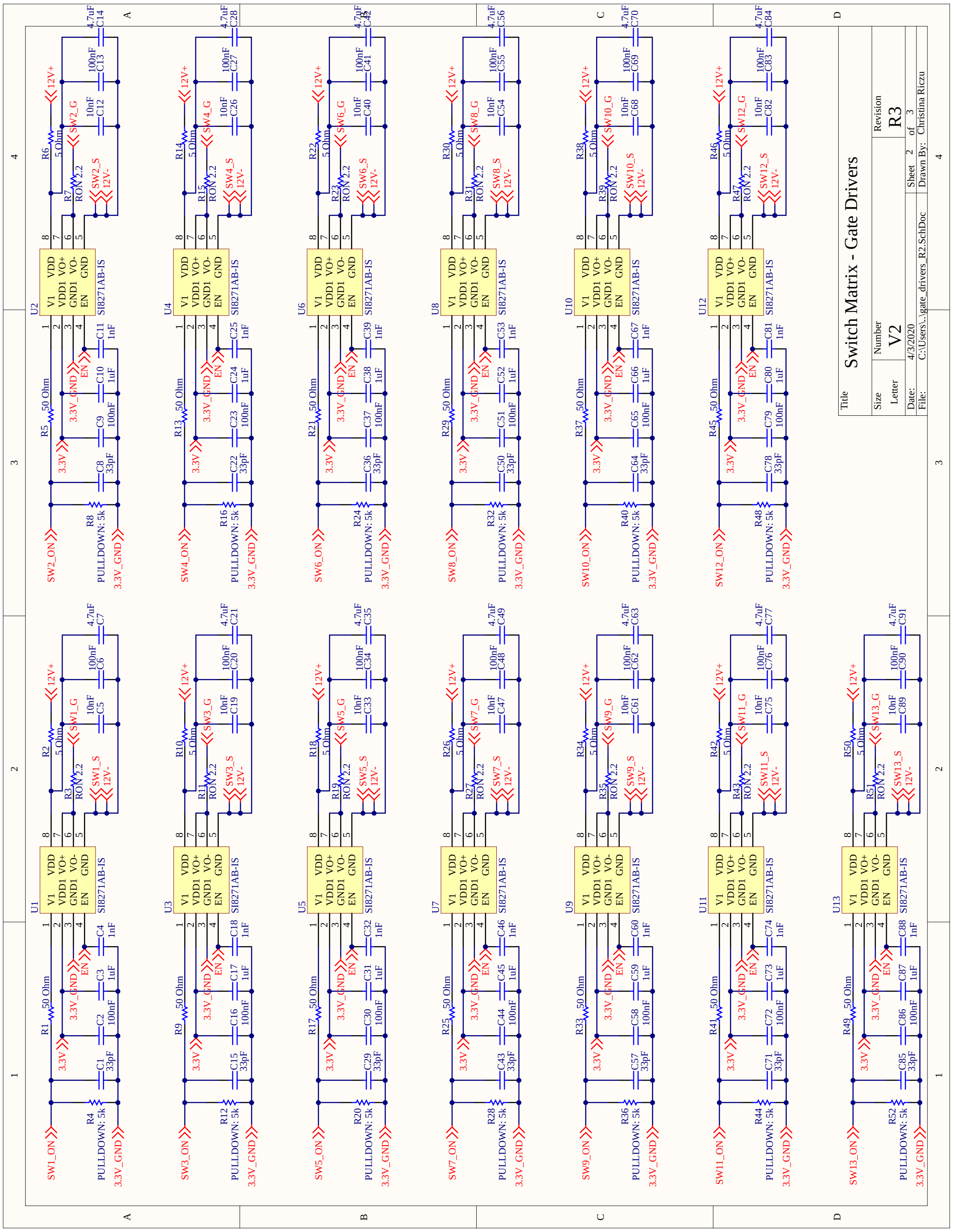


Figure 4.5: Switch Matrix Schematics - Gate Drivers

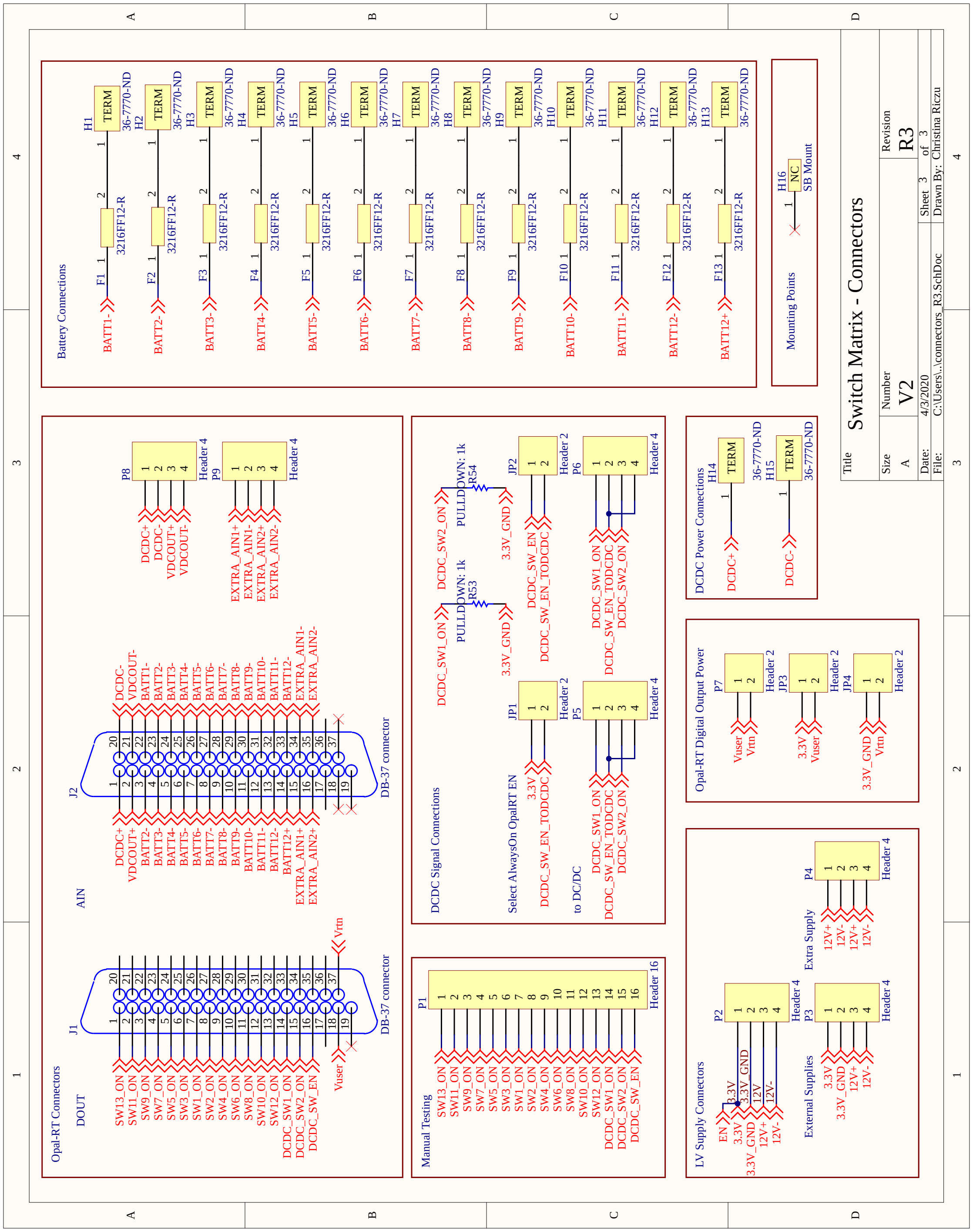


Figure 4.6: Switch Matrix Schematics - Connectors

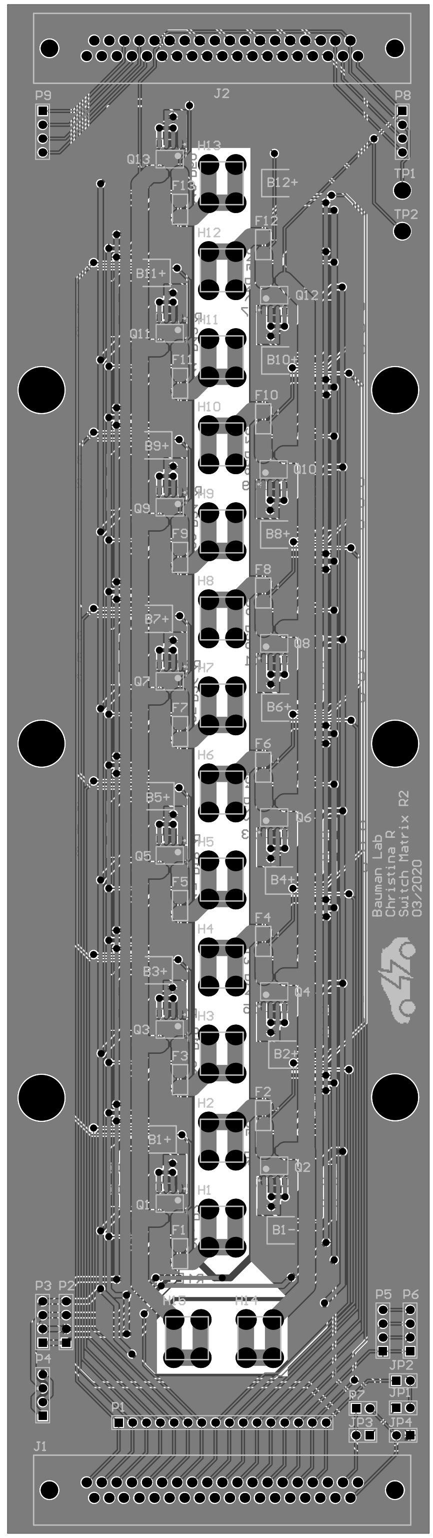


Figure 4.7: Switch Matrix PCB - Top Layer

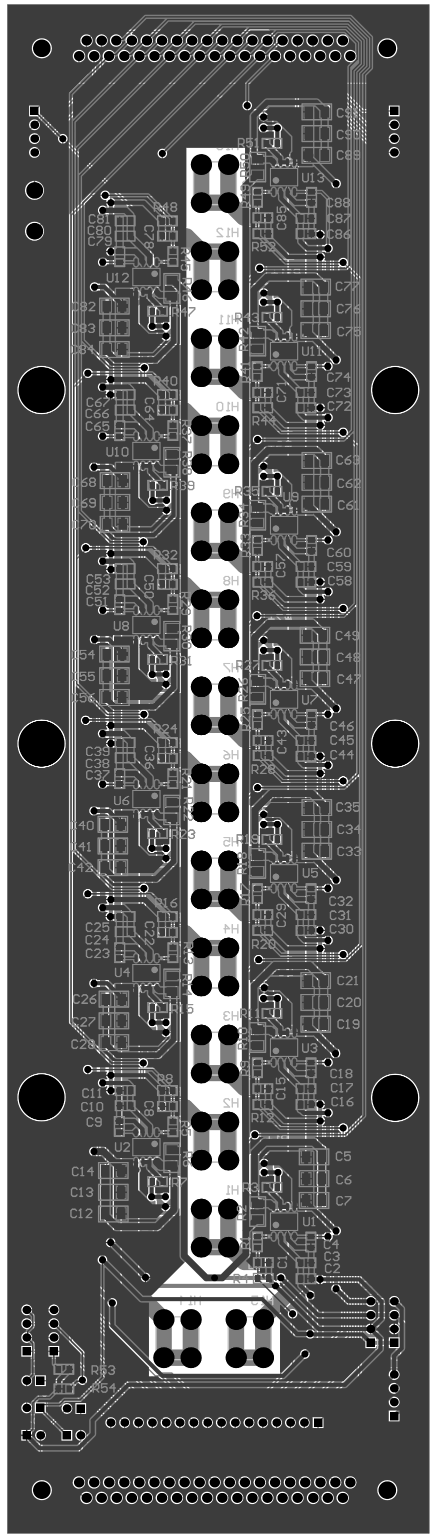


Figure 4.8: Switch Matrix PCB - Bottom Layer

4.1.3 HIL Code

The OP4510 HIL system is a real-time simulator that communicates to the host computer through a TCP/IP interface. The RT-LAB proprietary interface allows the programming of the HIL system, while Simulink is used to build the model. The Simulink model must be partitioned into computation and graphical user interface (GUI) elements so that multiple cores can be utilized. The computation elements are loaded onto the local FPGA chip such that the controller can sample up to 400kHz. The console gathers data asynchronously from the controller to ensure that controller runtime is optimal. The overall system model in Simulink can be seen in Figure 4.9.

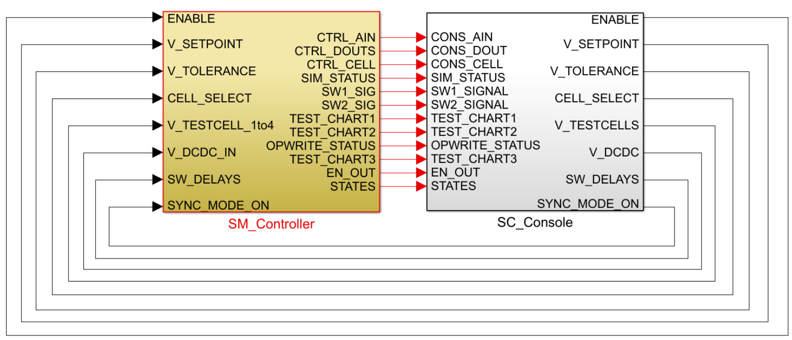
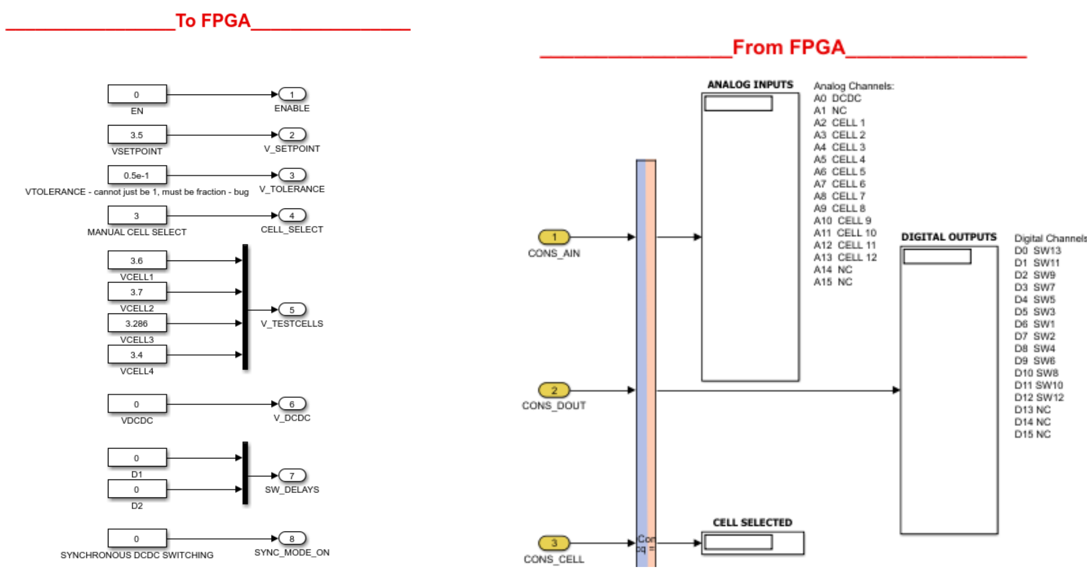


Figure 4.9: HIL System Model

In the console, inputs are defined and outputs from the controller can be viewed at a rate chosen by the user. The inputs to the controller can be seen in Figure 4.10a while a sample of the data given to the console can be seen in Figure 4.10b.

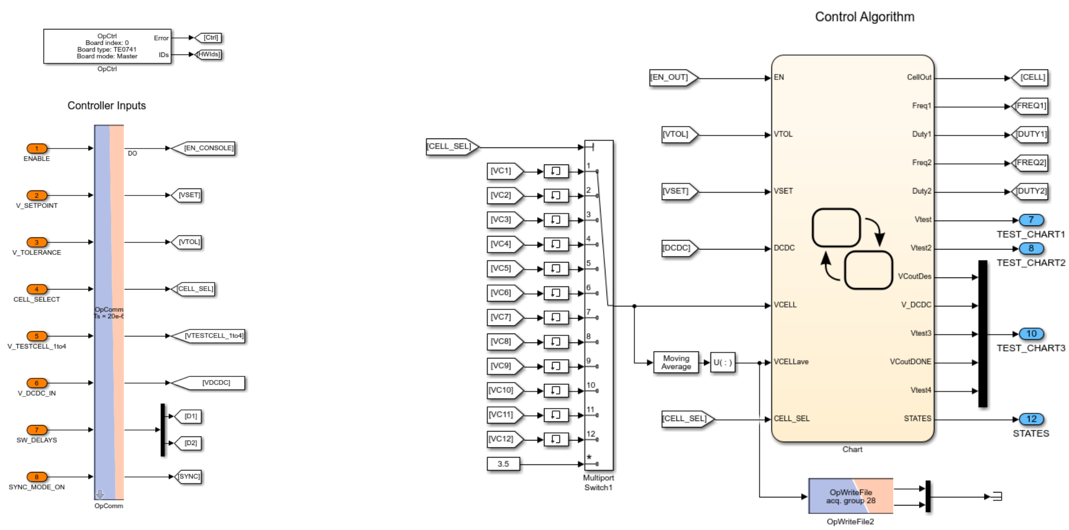


(a) To FPGA (b) From FPGA

Figure 4.10: HIL Console Model

The inputs that can be defined in the console include the enable signal, the voltage setpoint and the voltage tolerance. Other inputs are used for debugging or manual operation, or synchronous DC/DC operation. The outputs from the FPGA can be read into the console through a specialized Opal-RT OpComm block. The outputs shown include the analog inputs (DC/DC converter and cell voltages), digital outputs (the PCB switch control signals), and the current selected cell.

The controller model begins with the inputs to the controller from the console. These inputs are also passed through the specialized OpComm block, and can be seen in Figure 4.11a. The inputs are fed into the stateflow block that acts as the control algorithm, seen in Figure 4.11b.

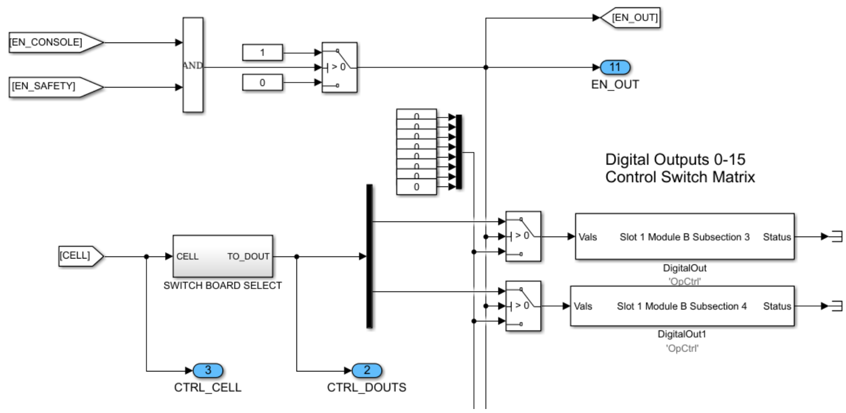


(a) Inputs

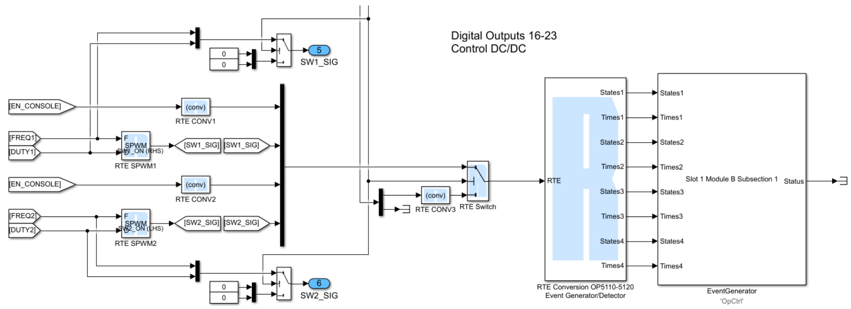
(b) Control Algorithm

Figure 4.11: HIL Controller Model - Inputs and Control Algorithm

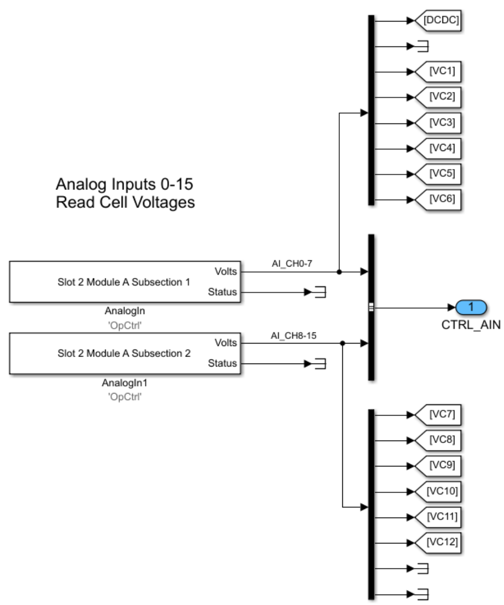
The switch matrix and DC/DC converter switches are controlled with digital outputs. The HIL system has DB-37 connectors for digital and analog inputs and outputs. The connector allows for 16 digital channels, while the rest of the pins are disconnected for isolation, or to provide external power and ground. There are also 16 differential analog input channels. The first set of digital outputs can be seen in Figure 4.12a and control the first 8 switches on the switch matrix. The rest of the 5 switch matrix signals are controlled by the next block, seen in Figure 4.12b. The last 3 signals are for DC/DC converter control; the enable signal for all the switches, and the primary and secondary switches. Since the DC/DC converter requires precise timing control, an EventGenerator block rather than the DigitalOut block from Figure 4.12a is used to ensure proper timing. Finally, the analog outputs are read in 8 channels at a time using the AnalogIn blocks, seen in Figure 4.12c. These analog signals include the DC/DC rail voltage and voltages from all 12 cells.



(a) Switch Matrix Control



(b) DC/DC Converter Control



(c) Analog Voltage Inputs

Figure 4.12: HIL Controller Model - Digital Outputs and Analog Inputs

4.2 Results

The test cases included odd cell charging, odd cell discharging, even cell charging and even cell discharging. The DC/DC converter was operated at a fixed frequency of 100kHz. The duty cycle was varied based on the operation performed. A summary of the results can be seen in Table 4.1.

Table 4.1: DC/DC Converter Experimental Results

Cell Type	Test Case	P_{IN}	P_{OUT}	Efficiency
Odd Cell	Charging	13.21 W	8.78 W	66.48%
	Discharging	6.27 W	4.47 W	71.29%
Even Cell	Charging	30.04 W	21.60 W	71.90%
	Discharging	19.86 W	14.11 W	71.05%

The odd cell charging waveforms can be seen in Figure 4.13. The efficiency for odd cell charging was found to be 66.48% for an average cell current of 2.63A and average power of 13.2W. In addition, a screen shot from the Tektonix oscilloscope can be seen in Figure 4.17a.The odd cell discharging waveforms can be seen in Figure 4.14. The efficiency for odd cell discharging was found to be 71.29% for an average cell current of 1.92A and average power of 6.23W. The even cell charging waveforms can be seen in Figure 4.15. The efficiency for even cell charging was found to be 71.90% for an average current of 2.16A and average power of 30.04W. The even cell discharging waveforms can be seen in Figure 4.16. The efficiency for even cell discharging was found to be 71.05% for an average current of 2.26A and input power of 19.85W.

Switching waveforms for each case can be viewed in Figure 4.18 for the odd cell cases and Figure 4.19 for even cell cases.

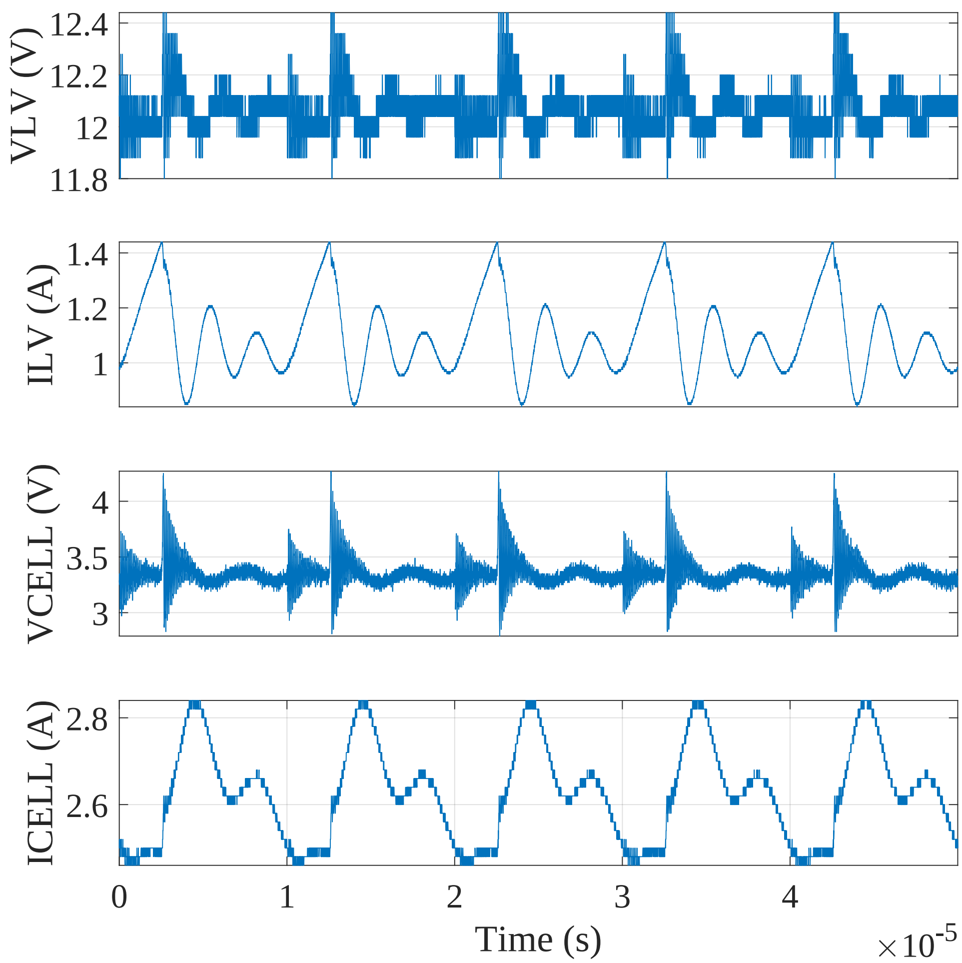


Figure 4.13: Odd Cell Charging Waveforms

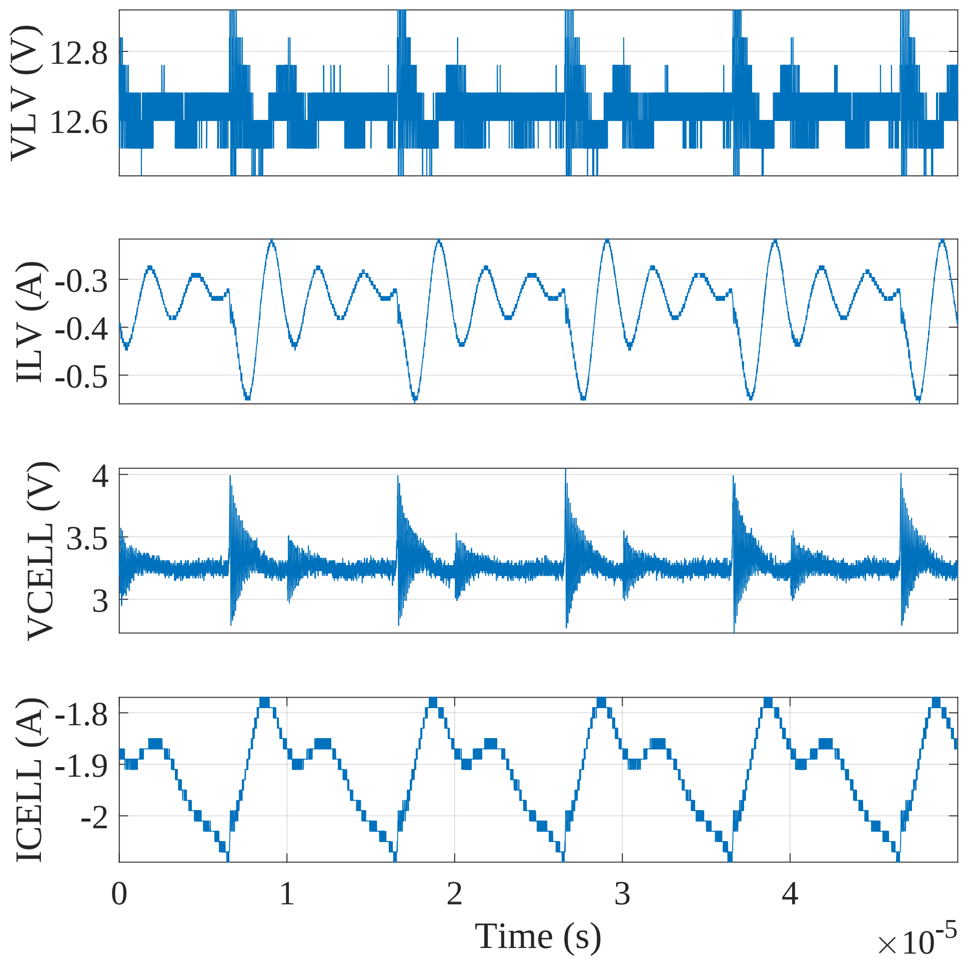


Figure 4.14: Odd Cell Discharging Waveforms

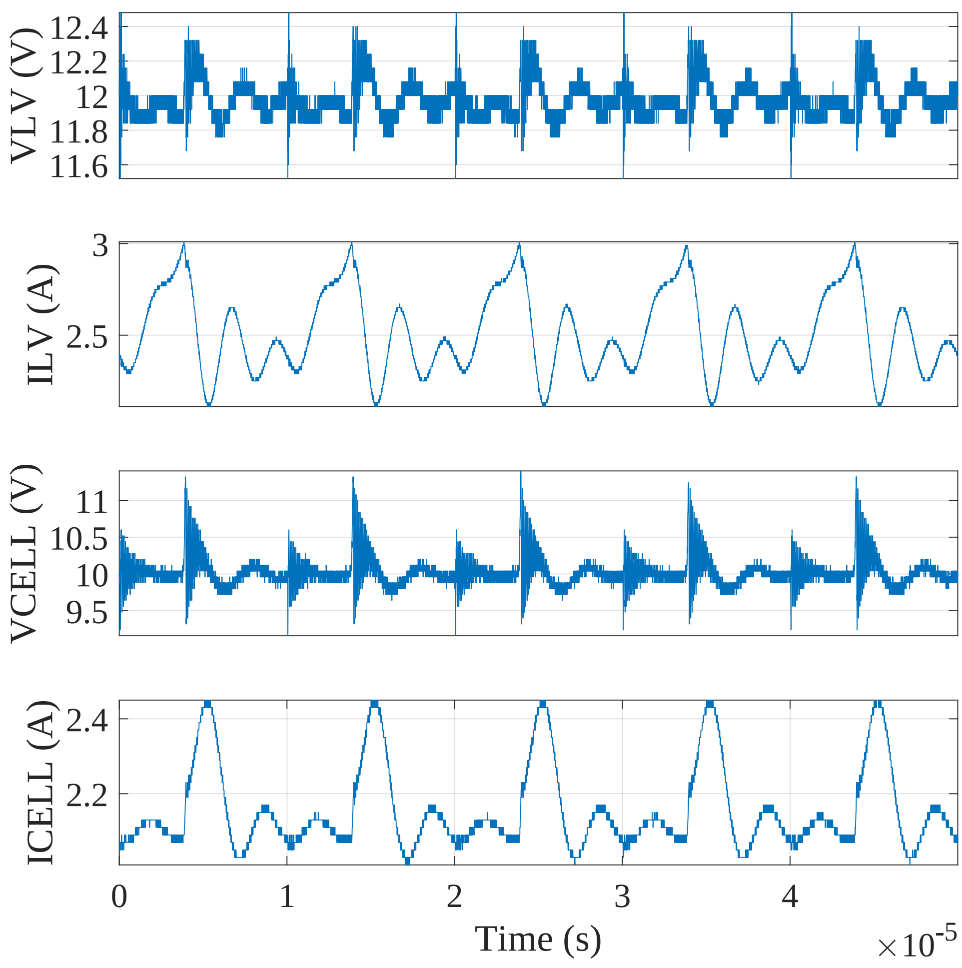


Figure 4.15: Even Cell Charging Waveforms

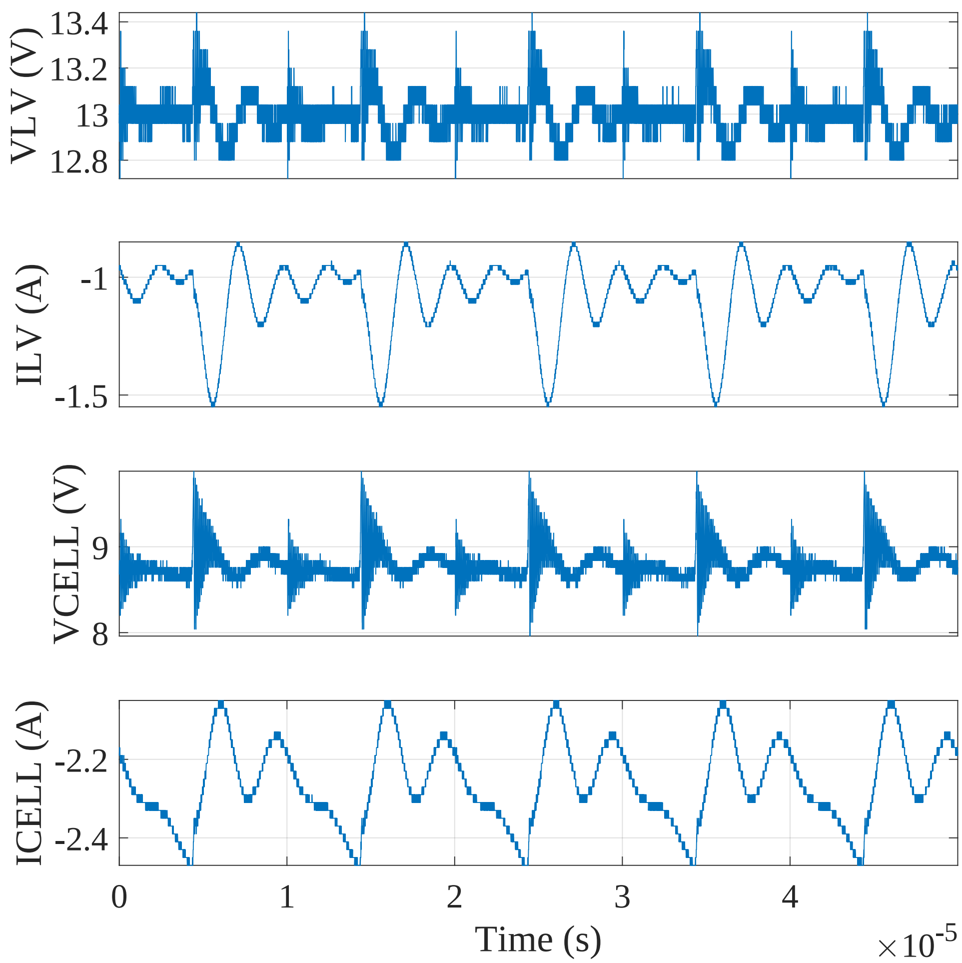
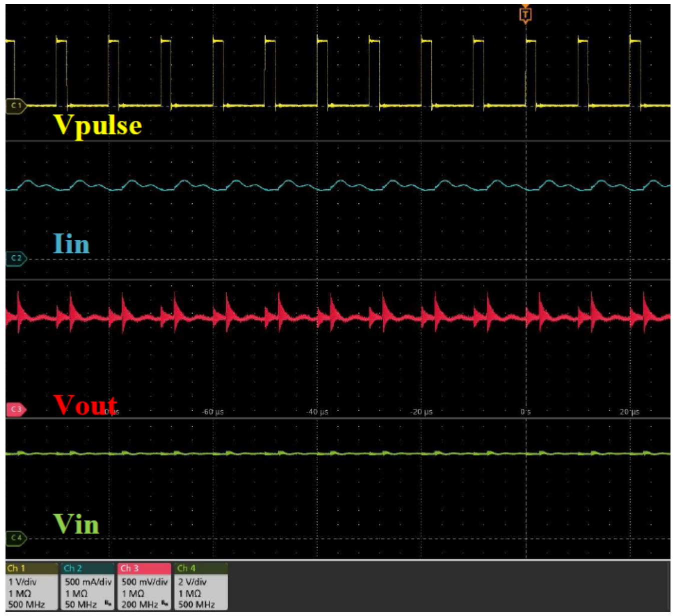
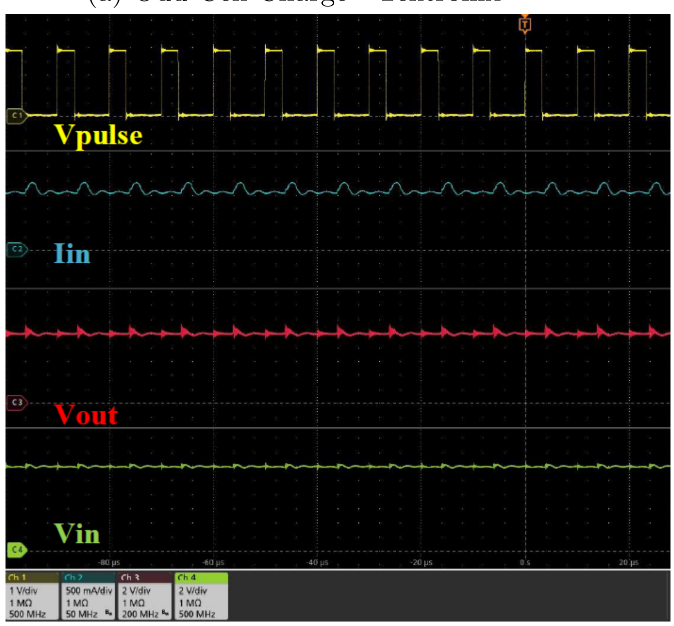


Figure 4.16: Even Cell Discharging Waveforms

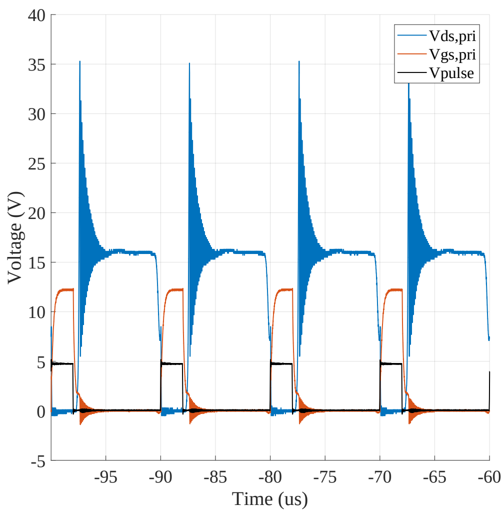


(a) Odd Cell Charge - Tektronix

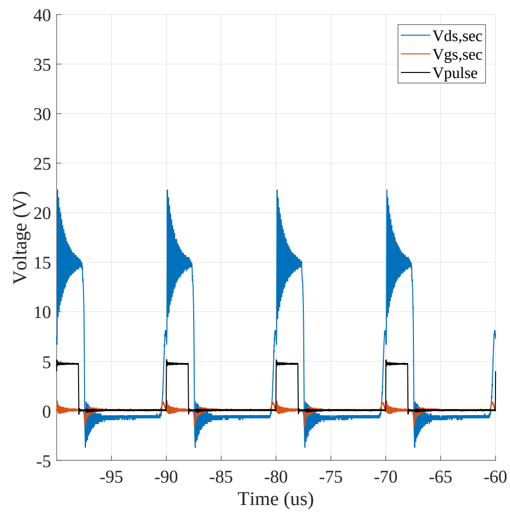


(b) Even Cell Charge - Tektronix

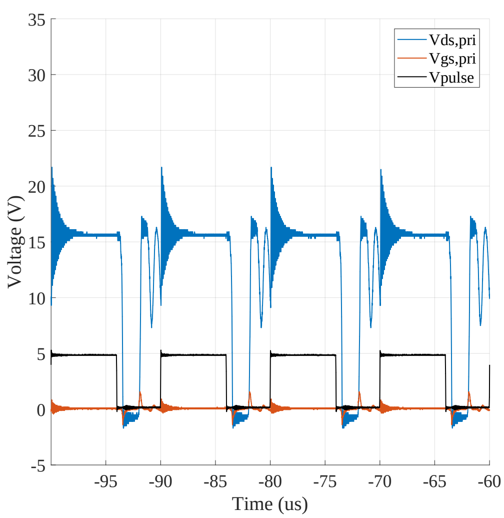
Figure 4.17: Oscilloscope Captures



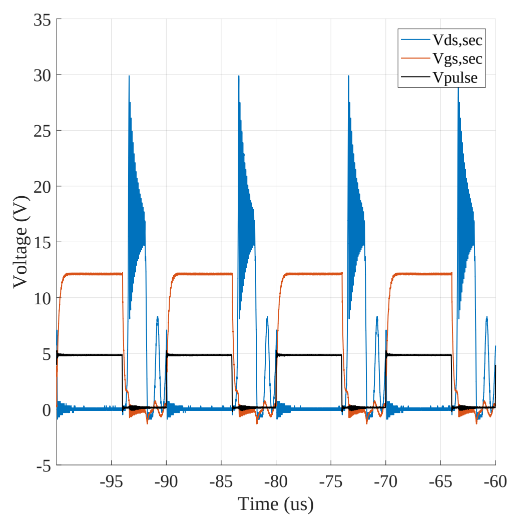
(a) 1 Cell Charge - Primary Switching Waveforms



(b) 1 Cell Charge - Secondary Switching Waveforms

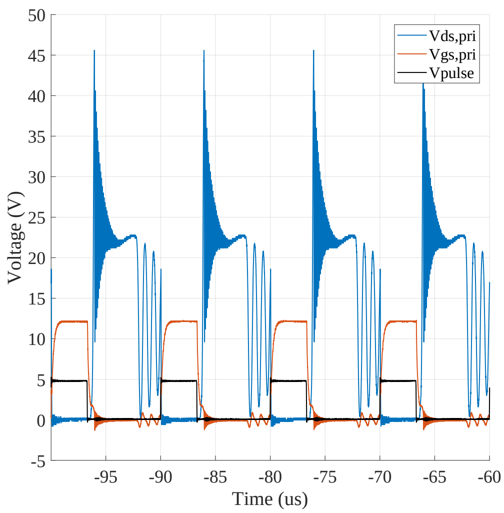


(c) 1 Cell Discharge - Primary Switching Waveforms

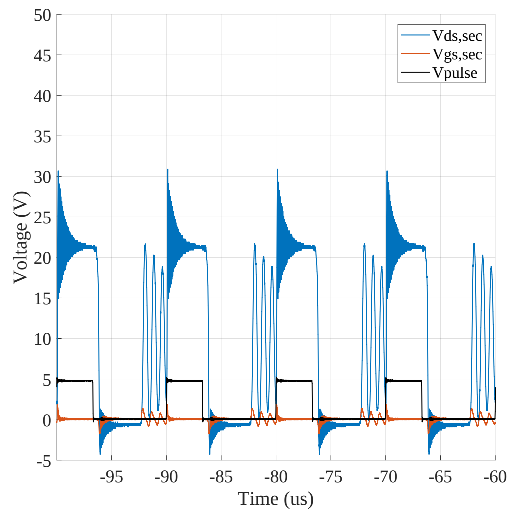


(d) 1 Cell Discharge - Secondary Switching Waveforms

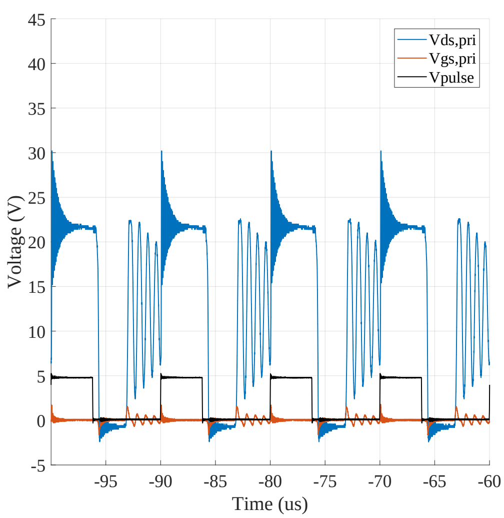
Figure 4.18: Odd Cell - Switching Waveforms



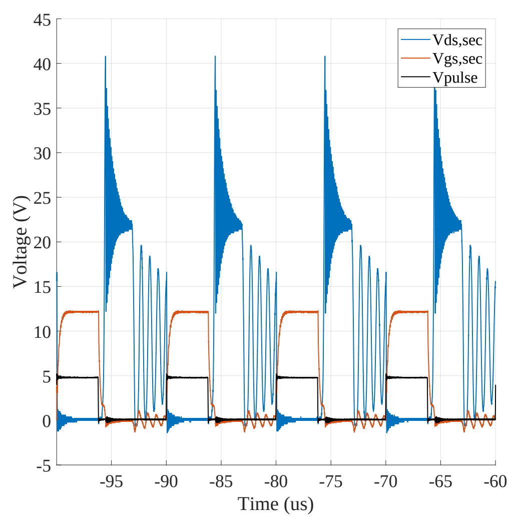
(a) 3 Cell Charge - Primary Switching Waveforms



(b) 3 Cell Charge - Secondary Switching Waveforms



(c) 3 Cell Discharge - Primary Switching Waveforms



(d) 3 Cell Discharge - Secondary Switching Waveforms

Figure 4.19: Even Cell - Switching Waveforms

4.2.1 Analysis

The overall efficiency of the LV2C circuit was approximately 71%. It did not match the simulations exactly due to the unique nature of the ringing, which is effected by the size of the wires, traces, and non-uniformity of components on the PCBs. Figures 4.13, 4.14, 4.15 and 4.16 show that the main function of the LV2C prototype, to charge and discharge the cells, is confirmed. The switch matrix did not exhibit unwanted transients during switch turn-on due to the transition control loop for V_{Cout}. The current ripple of the experimental testing was 0.3A. The voltage ripple on the cells reached 1V for odd cell testing, and up to 2V for even cell testing, or 0.66V per cell. Ringing issues presented a larger problem than anticipated. Undesirable voltage ringing can be seen on the V_{CELL} waveforms in each test case.

The switching waveforms behaved as expected, seen in Figures 4.18 and 4.19. During charging, the primary switch acted as the main switch and followed the V_{PULSE} turn-on waveform. This can be seen in Figures 4.18a and 4.19a. The secondary switch acted as the main switch during discharging. This can be viewed in Figures 4.18d and 4.19d. In each of these cases, V_{GS} of the main switch followed V_{PULSE} and the voltage over V_{DS} for the main switch approached zero. A significant portion of power loss was due to the small voltage present over the secondary switch diode from asynchronous switching. In all cases, the voltage spike was below the rated voltage of 60V. However, ringing caused significant voltage issues on the cells and an additional LC filter or snubber would aid in suppressing these undesirable effects.

Chapter 5

Vehicle Modeling for Range Extension

5.1 Vehicle Modeling

In order to save cost on the expensive materials and labor required to prototype new vehicles, automotive original equipment manufacturers (OEMs) moved to detailed simulations to validate their designs. The modern OEM can simulate the entire vehicle to determine the overall powertrain efficiency, as well as estimate the range of the vehicle. Advanced vehicle modeling serves as a valuable tool for these companies, allowing them to make quick decisions about the vehicle structure. The design process has thus become very iterative; designing and then checking with simulation before making improvements. However, computing times for running vehicle system models can be long. If the complexity of the system is increased, the time to run a simulation also increases drastically. There is a disconnect between component level circuit analysis and system level simulations in literature due to the issues that arise between modeling both levels of complexity. In order to run the entire vehicle model in a timely manner, efficiency maps are typically made into look-up tables which reference the inputs for an estimation. An example of this would be the electric motor; its efficiency would be derived from an array that picks a value based on the current torque, speed and voltage of the HV bus. Despite each individual piece of the vehicle being an estimation, the system model can mimic the results of a real-world vehicle with minimal error; enough to gain the interest of OEMs worldwide.

5.1.1 System Model

A forward-looking vehicle model was created to simulate the 2018 Chevrolet Bolt. A Matlab script was generated to run the Simulink model for several cases. The vehicle model is comprised of three main parts seen in Figure 5.1; the driver, the controller, and the plant. The driver model aims to mimic a person driving the desired path. The controller model takes the inputs from the driver and converts it into actions for the vehicle to take. Its primary purpose is to limit the torque request to the motor based on the speed of the chassis. Finally, the plant model describes the vehicle dynamics of each component along the powertrain and can be seen in Figure 5.2. The parameters used for the model are summarized in Table 5.1.

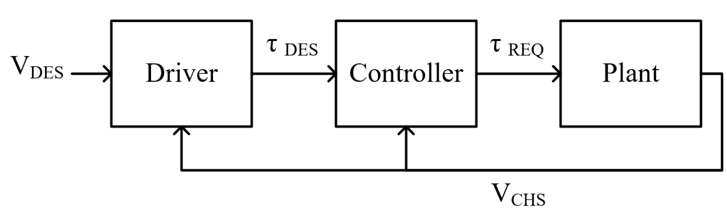


Figure 5.1: Simulation - System Model

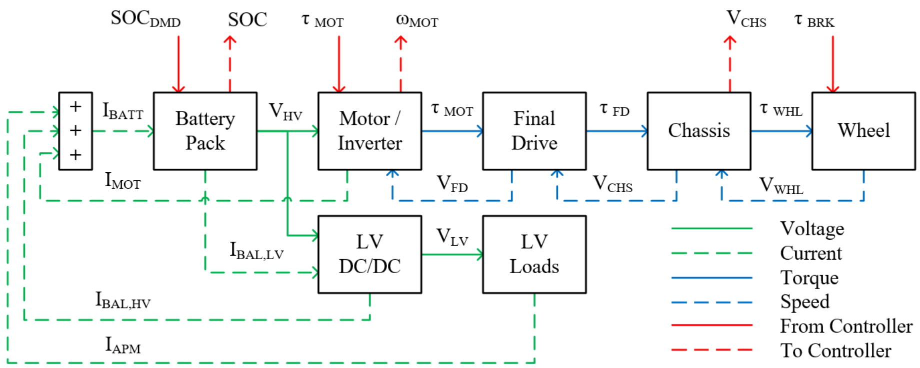


Figure 5.2: Simulation - Plant Model

Table 5.1: Vehicle Properties

Annotation	Description	Value	Unit
K_P	Driver PI Controller	1000	N/A
K_I	Driver PI Controller	0.5	N/A
τ	Driver Response	0.2	N/A
g	Gravity	9.81	$\frac{ksg}{ms^2}$
t	Ambient Temperature	25	^oC
I	Motor Inertia	0.0226	kgm^2
f	Final Drive Ratio	7.05	N/A
r	Wheel Radius	0.32385	m
u_1	Rolling Resistance	0.006	N/A
u_2	Rolling Resistance	0.0001	N/A
A	Frontal Area	2.532	m^2
m_{chs}	Chassis Mass	1625	kg
m_{drv}	Driver Mass	80	kg
cd	Coefficient of Drag	0.32	N/A
P_{ACC}	Accessory Power Draw	300	W

5.1.1.1 Driver

The driver is implemented as a PI controller. The error is defined as the difference between the desired speed of the vehicle model to follow the input drive cycle, and the actual speed of the chassis, seen in Equation 5.1.1 below. The PI controller output calculation is shown in Equation 5.1.2.

$$E(t) = V_{CHS}(t) - V_{DES}(t) \tag{5.1.1}$$

$$U(t) = K_P E(t) + K_I \sum E(t)dt \tag{5.1.2}$$

Where $E(t)$ is the error value, $V_{CHS}(t)$ is the speed of the vehicle chassis, and $V_{DES}(t)$ is the desired speed of the drive cycle. The value of $U(t)$ is the required torque to achieve the desired speed, while K_P and K_I are tunable parameters. For this model, the K_P is set to 1000 and the K_I value is 0.5, seen in Table 5.1.

In addition to the PI controller, a human reaction time is also incorporated into the model. A transfer function is used to add a small delay to the torque requests, which can be seen in Equation 5.1.3.

$$\frac{1}{\tau s + 1} \tag{5.1.3}$$

Where τ is the driver response time. In this case, the response time is set to 0.2 seconds. Finally, the torque requests are divided into positive and negative torque; this represents the driver applying their foot to the pedal to accelerate, or on the brake to decelerate. These commands are passed to the controller as τ_{ACC} and τ_{BRK} respectively.

5.1.1.2 Controller

The purpose of the controller is to limit the driver acceleration and braking demands to realistic values, such that the model remains accurate. The τ_{acc} and τ_{brk} commands are saturated so that they don't exceed the maximum force that can be applied on the wheel. Both are divided by the wheel ratio to convert to angular torque. Meanwhile, the motor speed is used as an input to two torque-speed lookup tables. The first is a positive table to determine the maximum torque limit during acceleration, and the second is a negative map to determine the maximum torque limit during braking. The torque-speed curve and motor efficiency map used for the model is seen in Figure 5.3. The outputs go to a set of maximum and minimum blocks. The first block takes the minimum torque acceleration demand between two inputs; the saturated acceleration torque command from the driver, and the positive maximum possible acceleration torque for the instantaneous motor speed. This will be the main portion of the torque demand to the motor. Another portion shall be the braking torque that the motor can accept. The vehicle speed is fed through a lookup table to determine how much braking torque will be accepted at the current speed. This is multiplied by the brake command to receive the allowed torque. The maximum block enforces the maximum torque limit during braking on this regeneration torque, and adds it to the motor torque. This is the final output motor torque demand τ_{mot}. The wheel braking command is the braking command minus the accepted motor regeneration.

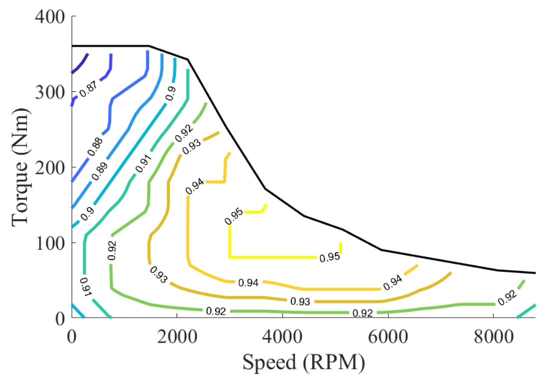


Figure 5.3: Torque-Speed Curve and Motor Efficiency Map

5.1.1.3 Chassis

The chassis block describes the dynamics of the vehicle. It assumes that the vehicle is a point in space with weight and aerodynamic losses. The following Equation 5.1.4 is used to determine the speed of the vehicle.

$$V_{CHS}(t+1) = V_{CHS}(t) + \frac{1}{m}\int_{t}^{t+1}(F_{WHL} - 0.5\rho_{air}AC_DV_{CHS}^2(t))dt \qquad (5.1.4)$$

Where $V_{CHS}(t)$ is the vehicle speed in m/s, F_{WHL} is the force from the wheels in N, m is the mass of the vehicle in kg, ρ_{AIR} is the density of air, A is the area of the front of the vehicle, and C_D is the coefficient of drag for the vehicle. The value of mass for the vehicle is both the chassis mass, 1625 kg, and the mass of the driver, 80 kg, which can be found in Table 5.1.

5.1.2.4 Wheels

The force that the wheels provide to the chassis is modeled using the wheel speed, size of the wheels, and coefficients to determine amount of slip that the wheels have with the road. Equation 5.1.5 shows this calculation.

$$F_{WHL} = \frac{\tau_{whl} + \tau_{brk}}{r_{whl}} - (\mu_1 + \mu_2 \omega_{whl}) mg \tag{5.1.5}$$

Where τ_{whl} is the torque supplied to the wheels in Nm, τ_{brk} is the torque applied by the friction of braking, r_{whl} is the radius of the wheel in m, μ_1 and μ_2 are coefficients of rolling resistance that determine the ability of the wheel to stick to the road, ω_{whl} is the speed of the wheel in m/s, and g is the coefficient of gravity in m/s^2.

5.1.2.5 Final Drive

Before the wheels, a final drive ratio is used to simulate the total ratio between the motor shaft and the wheels. For the 2018 Chevrolet Bolt, this ratio is 3.87. To determine τ_{whl}, the torque that is supplied to the wheel block, Equation 5.1.6 is used.

$$\tau_{whl} = \eta_{fd} r_{fd} \tau_{mot} \tag{5.1.6}$$

Where τ_{mot} is the torque provided by the electric motor, r_{fd} is the final drive ratio, and η_{fd} is the mechanical efficiency of the final drive gears. Typically, the final drive ratio is above 95% efficient.

5.1.2.6 Motor and Inverter

The motor and inverter characteristics can be represented on the same efficiency map, and thus are placed in one Simulink plant block to simplify the model. To determine the torque provided by the electric motor, τ_{mot}, the torque request from the controller is limited by the torque-speed curve in the block. The limited torque value is implemented with a dynamic saturation block, whose inputs are the positive and negative torque-speed curves. This can be seen in Equation 5.1.7.

$$\tau_{mot} = \begin{cases} \tau_{req} & \text{if } \tau_{neg,lim}(\omega_{mot}) < \tau_{req} < \tau_{pos,lim}(\omega_{mot}) \\ \tau_{lim} & \text{if } \tau_{neg,lim}(\omega_{mot}) \geq \tau_{req} \leq \tau_{pos,lim}(\omega_{mot}) \end{cases} \tag{5.1.7}$$

Where τ_{req} is the torque requested from the controller in Nm, $\tau_{pos,lim}(\omega_{mot})$ and $\tau_{neg,lim}(\omega_{mot})$ are the positive and negative torque limits, and ω_{mot} is the angular speed of the motor in rad/s. To calculate ω_{mot}, Equation 5.1.8 is used.

$$\omega_{mot} = \frac{r_{fd} V_{CHS}}{r_{whl}} \tag{5.1.8}$$

To provide the required mechanical angular speed and torque to the vehicle, the electrical motor must request current from the battery. Equation 5.1.9 is used to find the current requirement.

$$I_{MOT} = \frac{\eta_{mot} \omega_{mot} \tau_{mot}}{V_{BAT}} \tag{5.1.9}$$

Where I_{MOT} is the motor current requirement in A, η_{mot} is the efficiency of the motor based on speed and torque, and V_{BAT} is the voltage of the HV battery pack.

5.1.2.7 LV Loads

The electrical accessory block refers to the LV loads in the vehicle. This is any component that is powered by LV, including all the CPUs, PCBs, HVAC and fans, safety circuitry, and more. This load is named P_{APM} and was estimated to be 300W. To find the required battery current, the LV loads must first pass through the HV-to-LV DC/DC converter, otherwise known as the advanced power module or the APM.

5.1.2.8 APM

The APM steps down the 400V HV voltage to 12V for the lead-acid battery. It is the HV-to-LV DC/DC converter in every commercial vehicle. Due to the widespread use of the APM and its commercial maturity, the efficiency of the APM is high despite the large buck voltage difference. A constant value of 94% efficiency was used for this DC/DC converter. To calculate the current required from the battery pack to stabilize the LV battery, Equation 5.1.10 is used.

$$I_{APM} = \eta_{apm}(\frac{P_{APM}}{V_{LV}} + I_{BAL}) \tag{5.1.10}$$

Where I_{APM} is the required current from the HV battery pack to the APM DC/DC converter in A, η_{apm} is the constant efficiency of the APM at 94%, P_{APM} is the 300W LV load, V_{LV} is assumed to be a constant 12V from the lead-acid battery, and I_{BAL} is the current that is required from the balancing circuitry.

5.1.2.4 Battery Pack

The current that is required for the APM and the motor are summed together to find the battery pack current. Equation 5.1.11 shows this summation, while Equations

5.1.12 and 5.1.13 show the effect on pack SOC and cell SOC.

$$I_{BAT} = I_{APM} + I_{MOT} \tag{5.1.11}$$

$$SOC_{PCK}(t) = \sum SOC_i(t) \tag{5.1.12}$$

$$SOC_i(t+1) = SOC_i(t) + \frac{1}{C_i}\int_t^{t+1} I_{BATT}(t)dt \tag{5.1.13}$$

Coulomb counting is used to model the change in SOC over time. Although this method can have calibration error on real systems, the cell data for the 2018 Chevrolet Bolt model is not sufficient enough to support a more complex approach, such as a Kalman filter. This would be used when the cell data available included all types of cell tests, such as the static capacity test, SOC-OCV curve generation and hybrid pulse power characteristic (HPPC).

5.1.2 Balancing Model

Typical vehicle models assume that each cell in the pack has the same characteristics. If the SOC-OCV curve and capacity of one cell is known, a pack is created by multiplying the SOC-OCV curve to obtain the pack SOC-OCV curve, as well as multiplying the capacity by the number of parallel strings to obtain the full pack capacity. The cell SOC-OCV curve used for the research can be seen in Figure 5.4, showing that the battery cell voltage will vary between the expected 3 - 4V range for NMC cells. Usually, a vehicle model will assume that all cells will have the same capacity and thus the multiplication to estimate a pack SOC-OCV curve is accurate. However, some additions to the base vehicle model are required to quantify the range extension due to active balancing in the HV battery pack. The changes reflect a new requirement to model individual cells in order to observe the effect of differences in cell capacity.

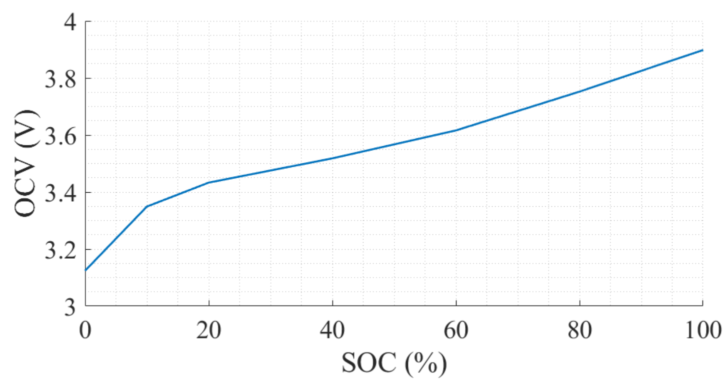


Figure 5.4: Cell SOC-OCV Curve

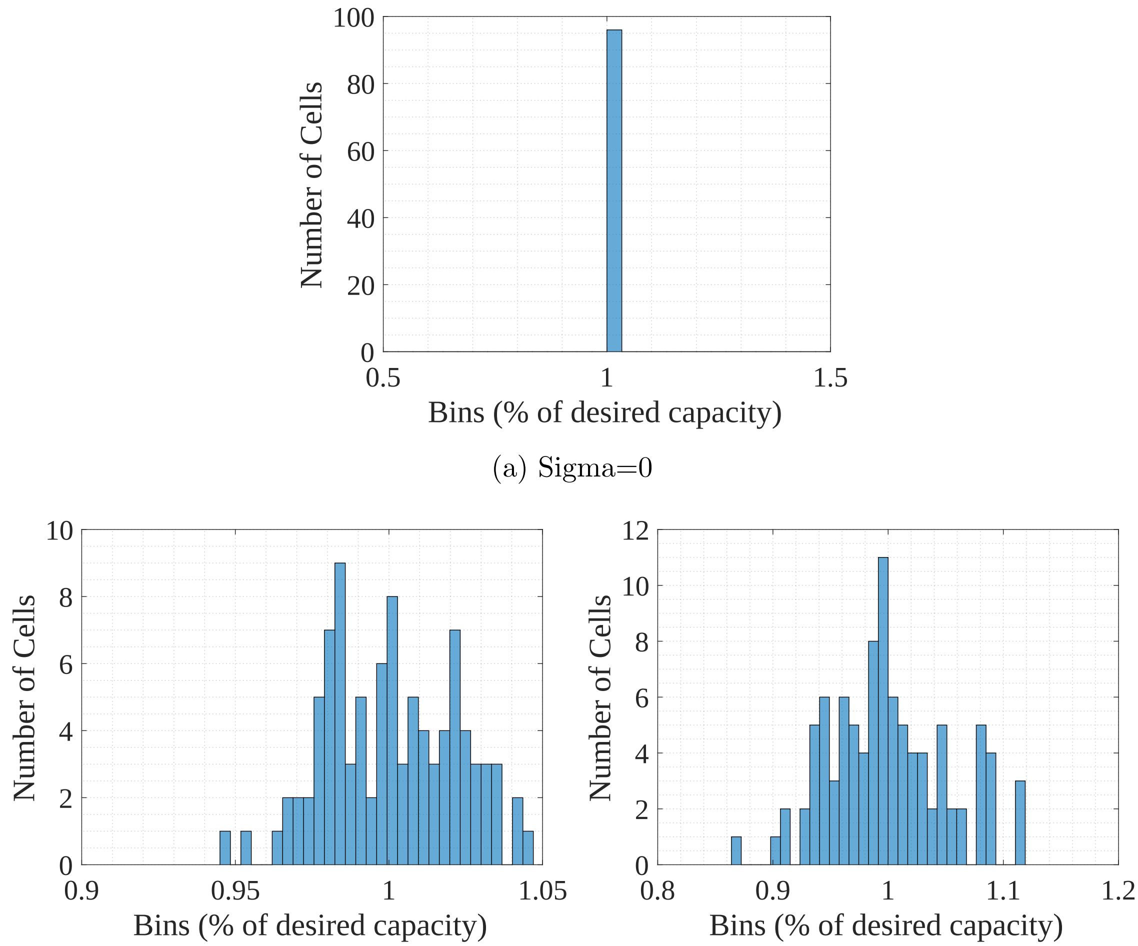
5.1.2.2 Cell Capacity

To accurately model the characteristics of the battery pack, cell capacity must differ. Since the 2018 Chevrolet Bolt has an overall configuration of 96S3P to form the battery pack [19], it is assumed that each parallel string will act similarly. Thus one parallel string will be modeled with different capacities at a third of the total required load current, and the current will be tripled to generate the total required current from the battery.

To generate the different cell capacities, a random number generator with bounds was programmed in Matlab script. All capacity values followed a normal distribution that was centered around 1, or 100% of the desired capacity. The output was limited to an array of 96 values which represented the capacity of each cell.

The value that was changed between sets of capacities was the σ to show different standard deviations of cell capacity. In the ideal case, battery cell capacities are matched perfectly and no active cell balancing is needed. This would mean that all cell capacities will center at a value of 1 and have a σ of zero with no variation. In fact, the added weight of the cell balancing circuit should decrease the range if it is not used. In the worst case, a battery pack aged many years would have major capacity fade issues which will take a large toll on the HV pack. It is assumed that the worst case would be a 5% cell capacity mismatch between all cells of the pack, giving just over a 10% cell SOC mismatch between the strongest and weakest cell. Thus, a range of cell capacities with σ 0%, 2% and 5% was generated.

Examples of three generated cell capacity variations can be seen in Figure 5.5. The histograms are divided into 30 bins to show the number of cells with similar capacity. The ideal vehicle model with all cells having the same capacity is shown in Figure 5.5a, as they all have a cell capacity of 1 with no variation. The worst variation of σ with value 5% is shown in Figure 5.5c, where the worst cell capacity approaches 85% capacity and could cause the HV pack to be retired from EV use. One other σ value is shown, 2%, to demonstrate a value in between the extremes.



(a) Sigma=0

(b) Sigma=0.02

(c) Sigma=0.05

Figure 5.5: Cell Capacity Variations

5.1.2.3 SOC Calculation

The goal of the vehicle model is for all cells to maintain the average pack SOC. If a cell strays too far from the average, the balancing algorithm will correct the cell by charging or discharging via the LV battery. The average pack SOC and pack voltage calculations are done at the module level using Equations 5.1.14 and 5.1.15.

$$SOC_{PCK,ave} = \frac{1}{n}\sum_{n=1}^{8} SOC_{MOD,n} \tag{5.1.14}$$

$$V_{PCK} = \sum_{n=1}^{8} V_{MOD} \tag{5.1.15}$$

A tolerance is used to determine whether a cell SOC needs to be corrected. The tolerance used in the model is V_{TOL}, which is set at 0.0001% SOC. This is a small value for simulation, and can be tuned to other values. On board a vehicle, this value would be larger to account for sensor error and SOC estimation error.

At the module level, the average pack SOC called $SOC_{PCK,AVE}$ is used to determine whether the balancing algorithm is required. Figure 5.6 shows the cell balancing model from a module level. The controller accepts the target SOC $SOC_{PACK,AVE}$, the SOC tolerance SOC_{TOL}, the SOC values of each cell, and the desired balancing current I_{BAL}. It will decide when to charge and discharge cells using the cell balancing DC/DC converter. The balancing current provided to each cell is called $I_{BAL,i}$, where i is the corresponding module cell from 1 to 12. A positive balancing current value assumes that the current will charge the cell. At the top, the pack current I_{BATT} is divided by 3 into the parallel string current called I_{STRING}. A positive string current assumes that the current is required from the cell, thus it is discharging current. Due to the opposite nature of these currents, $I_{BAL,i}$ is subtracted from I_{STRING} before it is passed to the cell model. The battery cell model calculates the cell's voltage and SOC based on the equation 5.1.13 and lookup tables for OCV and resistance. The module then sums all voltages and finds the average module SOC, both of which are passed to the full pack model.

The balancing current I_{BAL} is the value that is given to the cell. To calculate the balancing current required from the LV battery, I_{BAL} is multiplied by the inverse of the cell balancing DC/DC experimental efficiency to get the larger current $I_{BAL,LV}$ that is fed to the LV battery model seen in Figure 5.2. There are 8 modules in the pack, and thus up to 8 balancing operations happening simultaneously at any point in time. The balancing does not happen continuously. Rather, a balancing pulse every 1 minute is administered that triggers the start of balancing during the drive cycle.

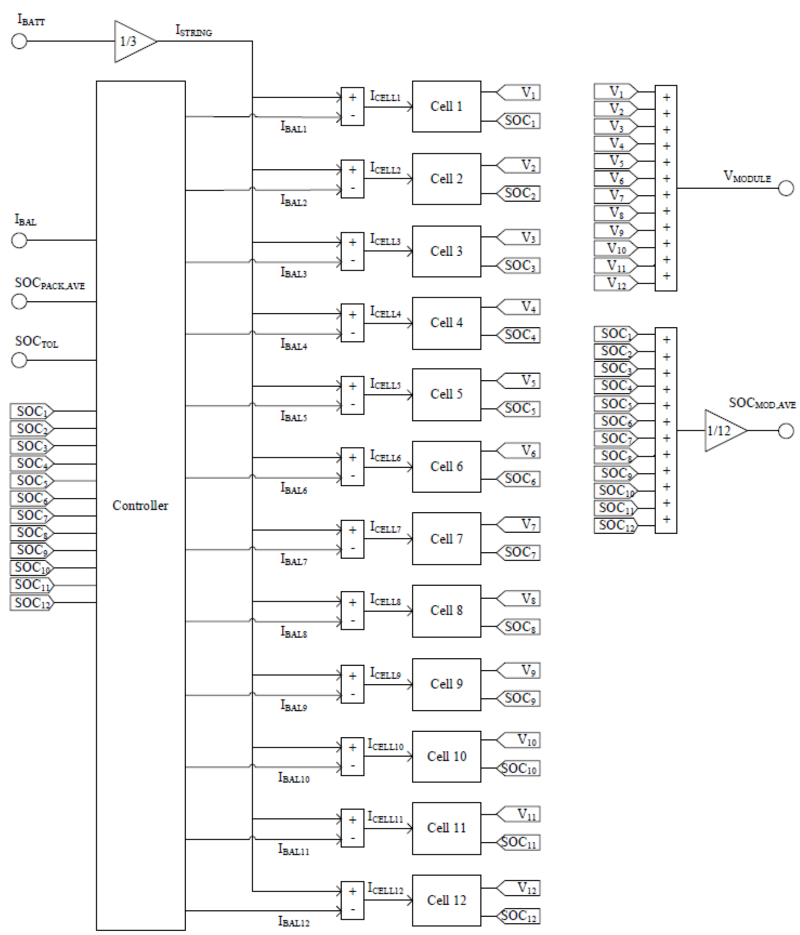
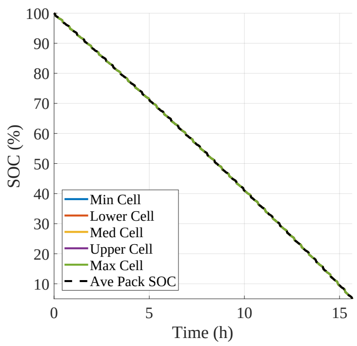


Figure 5.6: Simulation - Battery Module Model

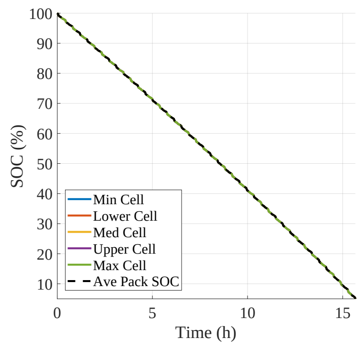
5.2 Results

The results of the cell balancing vehicle modeling for the 2018 Chevrolet Bolt show expected values. The LV2C circuit taps into more of the usable capacity in the vehicle, extending the range. The amount of range extension depends on the efficiency of the DC/DC, as well as the balancing current and time between balancing operations. For this study, the efficiency for each experimental case was used to determine the LV2C efficiency during simulation. In addition, the time between balancing operations was set to 1 minute. The balancing current was varied; 0A, 2A and 5A were used. A 12V lead-acid battery was simulated in the model, thus the system is a closed loop and the calculated range extension reflects the true results.

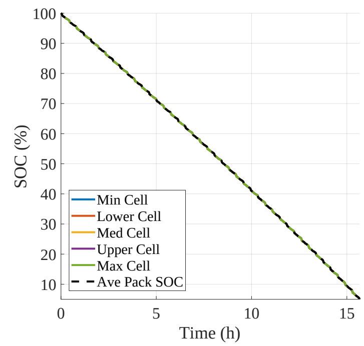
Figures 5.7 and 5.8 show SOC over time of varied capacity cells during repeats of the UDDS and HWFET drive cycles. The plots show cells with the lowest, low, average, upper, and maximum cell capacities out of the trial, as well as the average pack SOC. The range of the vehicle when the cells are ideal will be the largest out of any of the tests. This is true since no balancing would be needed to tap into the full capacity of the vehicle, and thus no energy lost to the balancing circuit. This is reflected in Figures 5.7a, 5.7b and 5.7c for the UDDS test and similarly for the top row of the HWFET repeats in Figure 5.8. Since the cells have the same capacity, the SOC does not diverge over time. The more variation in the cells, the less usable capacity is available, and the range is decreased with no active balancing. It is evident for the worst case of UDDS and HWFET in Figures 5.7g and 5.8g, where the minimum cell capacity reaches 5% SOC first even though the average pack SOC and maximum cell SOC is much greater.



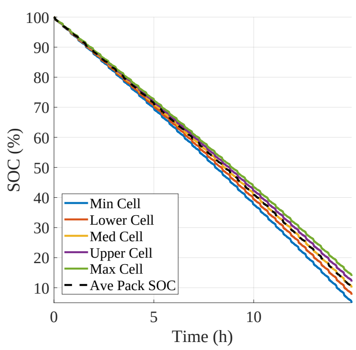
(a) Variation 0.00, with Balancing Current of 0A



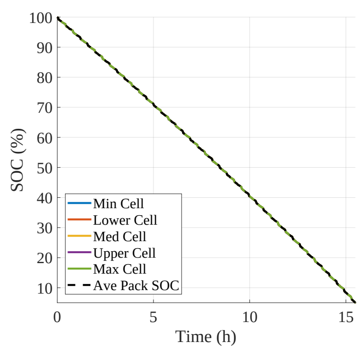
(b) Variation 0.00, with Balancing Current of 2A



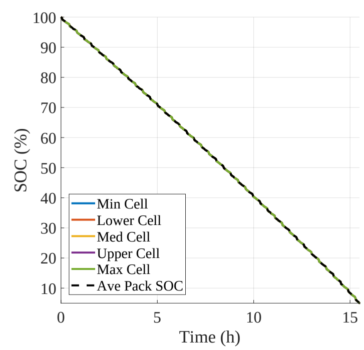
(c) Variation 0.00, with Balancing Current of 5A



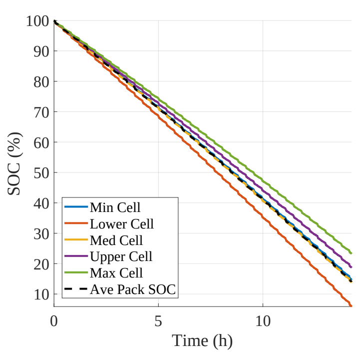
(d) Variation 0.02, with Balancing Current of 0A



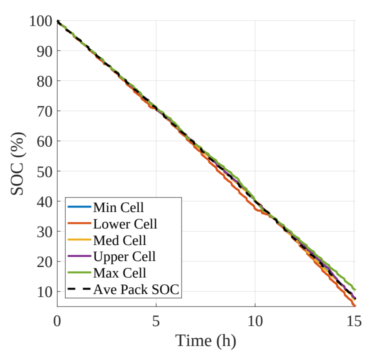
(e) Variation 0.02, with Balancing Current of 2A



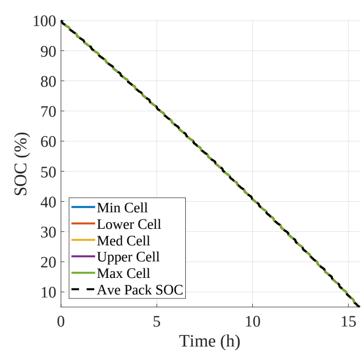
(f) Variation 0.02, with Balancing Current of 5A



(g) Variation 0.05, with Balancing Current of 0A

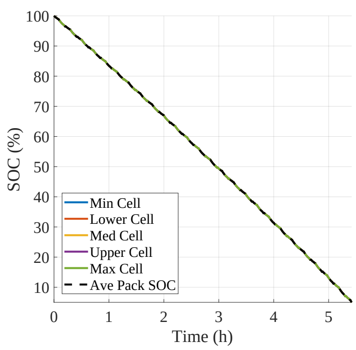


(h) Variation 0.05, with Balancing Current of 2A

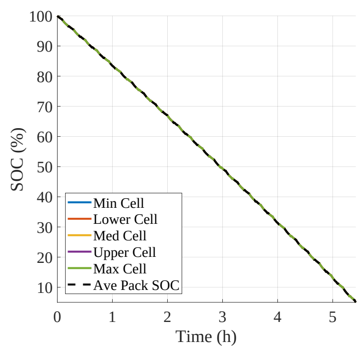


(i) Variation 0.05, with Balancing Current of 5A

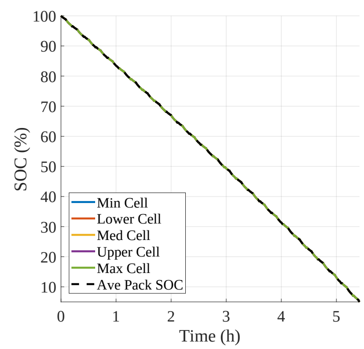
Figure 5.7: Cell SOC over Time - UDDS Repeats



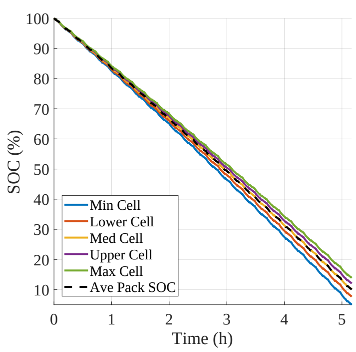
(a) Variation 0.00, with Balancing Current of 0A



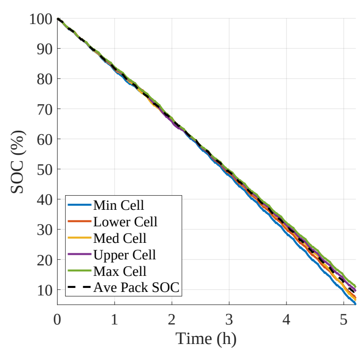
(b) Variation 0.00, with Balancing Current of 2A



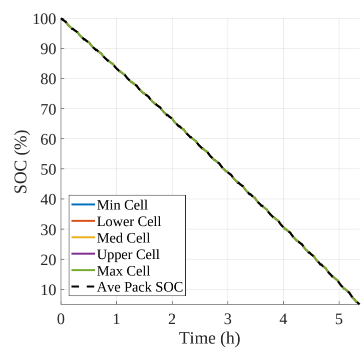
(c) Variation 0.00, with Balancing Current of 5A



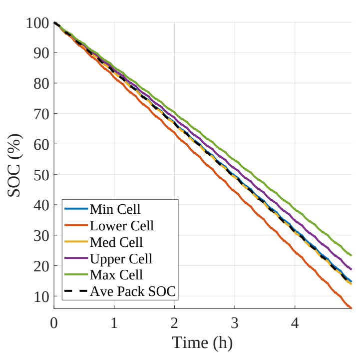
(d) Variation 0.02, with Balancing Current of 0A



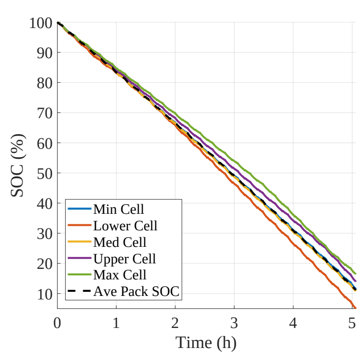
(e) Variation 0.02, with Balancing Current of 2A



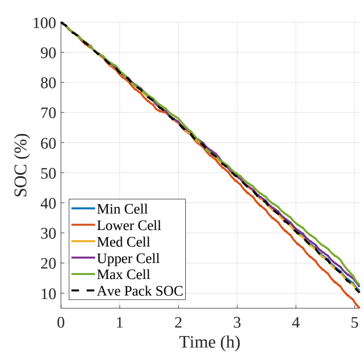
(f) Variation 0.02, with Balancing Current of 5A



(g) Variation 0.05, with Balancing Current of 0A



(h) Variation 0.05, with Balancing Current of 2A



(i) Variation 0.05, with Balancing Current of 5A

Figure 5.8: Cell SOC over Time - HWFET Repeats

The range results are summarized in Tables 5.2 and 5.3. The first row calculates the non-balanced range decrease of $\sigma = 2\%$ and $\sigma = 5\%$ based on the ideal case for $sigma = 0\%$. The next two rows for 2A and 5A balancing currents calculate the $\sigma = 2\%$ and $\sigma = 5\%$ range increases when compared to the 0A range in the same column. The largest range increase of 4.08% can be seen in Table 5.2 for both $\sigma = 2\%$ and $\sigma = 5\%$ with a balancing current of 5A. For $\sigma = 2\%$, both 2A and 5A keep the SOC values at the pack mean, seen in Figures 5.7e and 5.7f. They both fully utilize the pack capacity when considering LV2C losses, and thus arrive at the same range. On the highway, Table 5.3 shows that the range can be extended by up to 3.85% for the case of $\sigma = 2\%$ with a 5A balancing current. As expected, the 0A balancing for both UDDS and HWFET show that the range will remain the same. The small decrease is due to the energy consumed while running the balancing circuit algorithm. The smallest increase in range is seen for the HWFET case at $\sigma = 2\%$ and 2A balancing. The amount of balancing current can't keep up with the divergence in cell SOC, suggesting that there is a minimum balancing current needed for certain cases. This is also true for $\sigma = 5\%$ with 5A, which shows a lower value of 3.04% due to the difficulty of balancing larger SOC divergence. It is interesting to note that state-of-the-art balancing current typically does not exceed 2A, and thus the diverging SOC of aged packs cannot be accounted for in most active balancing solutions on the market today.

Table 5.2: Range Extension from LV2C Balancing - UDDS Repeats

Balancing Current	$\sigma = 0\%$	$\sigma = 2\%$	Range Increase	$\sigma = 5\%$	Range Increase
0A	493.48 km	469.92 km	-4.77%	469.92 km	-4.77%
2A	493.44 km	489.10 km	4.08%	475.43 km	1.17%
5A	493.39 km	489.11 km	4.08%	489.11 km	4.08%

Table 5.3: Range Extension from LV2C Balancing - HWFET Repeats

Balancing Current	$\sigma = 0\%$	$\sigma = 2\%$	Range Increase	$\sigma = 5\%$	Range Increase
0A	420.31 km	400.83 km	-4.64%	383.23 km	-8.82%
2A	420.29 km	404.12 km	0.82%	393.26 km	2.62%
5A	420.28 km	416.26 km	3.85%	394.87 km	3.04%

Chapter 6

Conclusions and Future Work

6.1 Summary of Research

In summary, the research objectives were achieved. A cell balancing circuit was proposed that allowed the transfer of energy easily from non-adjacent cells in an EV battery pack. This circuit could achieve a minimization in the SOC differences between all cells in the pack, demonstrated by the experimental work. Each case was proved experimentally - odd charging, odd discharging, even charging and even discharging - and efficiency was calculated. The proposed cell balancing DC/DC converter used minimal components, ultimately reducing the cost and weight of an active balancing circuit when compared to similar state-of-the-art hardware. The Matlab/Simulink code demonstrated that the active balancing circuit is beneficial for non-ideal battery cells in a pack. The range of the vehicle with and without the balancing aid was calculated and compared. A range extension of up to 4.08% during city driving can be found for multiple cases, while highway driving saw a range extension of up to 3.85%.

In Chapter 2, a review of battery characteristics and their safe operation is presented. The design choices made when constructing battery packs are discussed. Finally, battery balancing is thoroughly examined and state-of-the-art discussed.

Chapter 3 proposes a LV2C active battery balancing circuit that executes the design requirements. The concept, design, modeling and control of the circuit are discussed in detail.

In Chapter 4, the results of the experimental work with the LV2C circuit are shown. Each test case is proven and efficiencies are calculated.

Chapter 5 reviewed vehicle modeling concepts, as well as the vehicle model of a 2018 Chevrolet Bolt in Matlab/Simulink used for the research. The potential range extension with the LV2C circuit are presented.

In conclusion, active balancing shows promise for extending the range of a vehicle. Despite having a lower efficiency than other complex cell balancing circuits, the LV2C was able to extend vehicle range by 4.08%. The proposed circuit struck a balance between the current industrial standard, and the state-of-the-art complex circuits while maintaining a significant improvement over the no balancing case.

6.2 Recommendations and Future Work

The LV2C prototype testing should continue in order to gather additional experimental data. Several directions for future experimental work are summarized:

- Converge the SOCs of all lithium-ion cells in a module
- Test the LV2C prototype on a wide range of cell SOC
- Enable synchronous mode of the DC/DC converter

- Add a larger output filter to reduce ringing present on cells
- Generate a power versus efficiency curve for the DC/DC converter
- Redesign both PCBs for the switch matrix and DC/DC

Although the experiments show that energy can be transferred in and out of a single cell as well as the three-cell stack, the convergence of SOCs for a full 12-cell pack was not completed during the research. This would aid to further prove the LV2C concept in hardware.

The LV2C prototype was also tested at a fixed SOC and starting voltage. In order to fully test the product, the efficiency of the LV2C hardware should be recorded over the full range of SOC values.

Additionally, the flyback DC/DC converter was limited to asynchronous switching during the research. In order to increase the efficiency of the converter, synchronous switching should be tested on the LV2C prototype. Synchronous switching adds control complexity, but it would decrease the voltage over the secondary side switch during conduction and thus decrease losses in the flyback converter.

A larger output filter may help to reduce the unwanted voltage ringing that was present on the cells during experimental measurements. The output filter should be explored further, in addition to implementing a smaller voltage ripple requirement on the DC/DC converter.

The flyback DC/DC converter operations were limited to a static 100kHz switching frequency and respective duty cycles for each test case. In order to fully describe the DC/DC converter operation, other frequencies should be tested, as well as different duty cycles and thus several loads for the converter. A power versus efficiency curve for the DC/DC converter should be measured for multiple loads and for each test case; odd charge, odd discharge, even charge and even discharge.

Finally, a redesign of both PCBs should be performed. The PCBs were designed with the intent of flexible testing; the switch matrix could remain attached to the module while different DC/DC converters and redesigns could be swapped, and vice-versa. Preferably, these PCBs would be housed on a single PCB with embedded software programmed onto a CPU to eliminate the bulky DB-37 connectors for the Opal-RT HIL simulator. The PCBs were two layers in the research, while later revisions may want to add layers to reduce the footprint of traces. Additionally, this PCB should be housed within an enclosure that is rated for automotive applications, and have multiple connectors. It should have outputs for CAN communications, a CPU programming header, and a single input from the 12V lead-acid battery. From the 12V connection, 5V or 3.3V should be regulated to provide the CPU and IC input power, and 12V may be routed to the DC/DC converter input and gate drivers. This PCB could also be combined with other BMS functions, such as cell voltage monitoring, to further reduce PCB footprints in the vehicle. Finally, care should be taken to optimize the layout of the PCB to reduce parasitic resistance, capacitance and inductance by reducing the physical size and length of both the power-carrying traces, as well as the switch and gate driver connections. Reducing these can help to decrease switching node voltage ringing and improve the output waveforms.

With respect to the vehicle model, several improvements can be made:

- Compare LV2C vehicle simulations against other balancing circuits
- Test the LV2C algorithm with several classifications of vehicles (light-duty passenger, medium-duty passenger, light-duty trucks and heavy-duty trucks)

- Size the cooling system according to losses, add as weight
- Add an SOC dependency for the LV2C efficiency lookup table
- Add the power versus efficiency curve of the LV2C circuit
- Use a higher-order battery model

It would be incredibly valuable to compare other cell balancing circuits with LV2C on a system level. This would allow a direct comparison for automotive manufacturers to asses which cell balancing circuit would suit their needs. To complete this future work, one would need to program and test multiple cell balancing circuits in simulation or hardware to obtain their efficiency curves. These curves would appear as lookup tables in the vehicle model. The balancing algorithms for each type of cell balancing would be programmed and should replace the LV2C controller in simulation. It would be interesting to note which cell balancing algorithms could not keep up with the SOC divergence of cells, seen in the HWFET test with low balancing current and large SOC variance during this research. It would aid in deciding what the minimum cell balancing current truly should be based on SOC variance, and create a standard for cell balancing during the lifetime of the EV pack.

Testing different classifications of vehicles would expand the work and find a target vehicle where LV2C shows the greatest promise. Since LV2C is characterized by faster balancing, it may show much greater results for cells that are under large loads, such as for an electric bus. Additionally, cells with larger current load may require a larger balancing current to address their SOC divergence than typical cell balancing methods on the market today. LV2C is a flexible solution where the cell balancing DC/DC converter may be sized larger or smaller based on the required application, while providing similar fast balancing capabilities.

The thermal aspect of the vehicle model was not addressed, and is limited to electrical simulation only. However, the cooling system plays a large part in the final weight of the vehicle. In future work, the cooling system should be sized to address the heating requirements of the system, and weight added to the vehicle model.

The latter items - LV2C SOC dependency, LV2C power versus efficiency curves, and higher order battery models - are all used to increase the vehicle model's accuracy. Currently, the vehicle model is an accurate representation of a single operating point for the LV2C system. The vehicle model can be further expanded to include other operating points, thus allowing for complex control and searching for optimal operating points to reduce system losses.

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