GaN Based Cycloconverter-Type Dual-Active Bridge Converter: Control, Design, Analysis, and Experimental Verification

GAN BASED CYCLOCONVERTER-TYPE DUAL-ACTIVE BRIDGE CONVERTER: CONTROL, DESIGN, ANALYSIS, AND EXPERIMENTAL VERIFICATION

BY

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This work is dedicated to my parents Nancy, and Jeff, and to my girlfriend Katie

Abstract

In recent years, there has been a greater push to reduce green house gas emissions due to the looming threat of climate change. This has resulted in a shift towards more electrified transportation and as a result, reliance on renewable energy such as solar or wind and a decreased reliance on fossil fuels. Battery energy storage systems (BESS) have been one of the prevailing methods for storing electrical energy from intermittent energy sources due to their performance, cost and size. However, in order to interface BESS with the AC power grid, power electronics are a necessity. With this paradigm shift from fossil fuels to renewable energy, power electronics and their components have been a large focus of research in the scientific community. There has been a trend for continuous improvement of power electronic converter performance which has led to the desire for advances in semiconductor switches. Switches with lower power loss would allow power electronic systems to achieve higher efficiency and higher power density. Due to the continuous desire for improvement, researchers have begun to adopt Wide-bandgap (WBG) switching devices since silicon (Si) has been reaching its material limit and WBG devices offer improved performance. Silicon carbide (SiC) and gallium nitride (GaN) offer improved performance over Si, GaN in particular offers the fastest switching speeds and based on the device rating is well suited for medium power levels in BESS. Although the potential of GaN is known, it

is a fairly new technology and therefore a full analysis of its loss behaviour is required in order to model the device. In addition, GaN requires advanced measurement technologies to analyze them due to the high frequency operation and tiny device parasitics. Before GaN can reach widespread adoption in power electronic converters, the detailed analysis of the theoretical loss breakdown of a GaN-based power electronic system and measurement is required.

The incorporation of GaN into isolated DC/AC converters necessary for interfacing the AC grid with the DC battery has the potential to increase the power density and efficiency. However, incorporating GaN alone can not fix all the current problems in the conventional design approach of two-stage cascaded Dual-active bridge (DAB) and inverters. Typically, the DAB and inverter are connected through an intermediate DC bus which requires large and unreliable electrolytic capacitors to filter the ripple power, these capacitors reduce the life-time of the converter significantly.

This thesis proposes a GaN based single-stage DC/AC converter which does not require the large electrolytic capacitors or additional devices to filter the ripple power. In order to control the converter, a combined duty and phase shift control method is used. The operating condition for each discretized voltage output is derived based on the calculation for the lowest power loss conditions.

To further investigate the proposed control and use of GaN, a greater focus on gate driver and PCB design is needed to take advantage of the new WBG switching devices such as GaN HEMTs. As switching frequencies are continuously pushed higher and higher to improve the power density of converters, there is a need for extremely fast turn on and turn off times for FETs in order to minimize losses and maximize efficiency. However, large slew rates have a negative impact on the circuit

because the small parasitics present in the device packaging and PCB traces are no longer negligible and can result in severe oscillations and voltage spikes that can lead to increased losses or even device failure. Analysis of gate driver design and potential issues for designing with GaN are presented before the prototype is presented and analysed.

A single-stage isolated DC/AC converter using GaN is shown to provide superior performance compared with the traditional two-stage approach. Simulation comparisons of both converters reveal that the proposed topology greatly improves efficiency while also removing the intermediate DC bus which is known to cause reliability issues. The efficiency improvement is achieved through a proposed control scheme that determines the duty and phase shift for each discretized output voltage based on a weighting equation for minimum losses. The control scheme and converter behaviour are both validated through the use of a experimental prototype.

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Nomenclature

Symbols

C_{in} Input Capacitance, F

C_{iss} Transistor Input Capacitance, F

C_{oss} Transistor Output Capacitance, F

C_{out} Output Capacitance, F

C_{pcb} PCB Parasitic Capacitance, F

C_{pl} Inductor Parasitic Capacitance, F

C_{rss} Transistor Reverse Transfer Capacitance, F

D_1 Primary Side Duty Ratio

D_{1sw} Primary Side Minimum Switching Loss Duty Ratio

D_{2sw} Primary Side Minimum Switching Loss Duty Ratio

D_{cond} Minimum Conduction Loss Duty Ratio

D_{sw} Minimum Switching Loss Duty Ratio

E_{off} Switch Turn-off Energy Loss, J

E_{on} Switch Turn-on Energy Loss, J

E_{osshy} Capacitive Hysteresis Loss, J

E_{oss} Capacitance Loss, J

E_{qoss} Capacitance Loss, J

E_{qrr} Switch Diode Reverse Recovery Loss, J

f_s Switching Frequency, Hz

i_{Cin} Input Capacitor Current, A

i_{DC} Input DC current, A

i_{Lmax} Peak Leakage Inductor Current, A

i_L Leakage Inductor Current, A

$i_L(t)$ Inductor Current, A

K CHFL-DAB Parameter

k_{dR} Trapping Effect Ratio

k_{Tj} Heating Effect Ratio

L_{lk} Leakage Inductance, H

n Transformer Turns Ratio, n

P_{1cond} Primary Side Conduction Losses, W

P_{1sw} Primary Side Switching Losses, W

P_{2cond} Secondary Side Conduction Losses, W

P_{2sw} Secondary Side Switching Losses, W

P_{cond} Total Conduction Losses, W

P_{driver} Gate Driver Power Loss, W

P_{loss} Total Power Loss, W

P_o Output Power, W

$P_{transfer}$ Transformer Power Transfer, W

Q_g Gate Charge, C

Q_gd Gate-drain Charge, C

Q_gs Gate-source Charge, C

R Load Resistance, Ω

R_{dson} Transistor On-State Resistance, Ω

R_{gint} Internal Gate Resistance, Ω

R_{goff} External Off Path Gate Resistance, Ω

R_{gon} External On Path Gate Resistance, Ω

R_g External Gate Resistance, Ω

t Time, s

t_{fi} Current Fall Time, s

t_{fu} Voltage Fall Time, s

t_{ri} Current Rise Time, s

t_{ru} Voltage Rise Time, s

T_s Switching Period, s

V_{1ac} Transformer Primary Input Voltage, V

V_1 Primary Side Input Voltage, V

V_{2ac} Transformer Secondary Input Voltage, V

V_2 Secondary Side Outout Voltage, V

V_{dc} DC Bus Voltage, V

V_{ds} Drain-Source Voltage, V

V_{gon} Gate Off-state Drive Voltage, V

V_{gon} Gate On-state Drive Voltage, V

V_{gs} Gate-Source Voltage, V

V_L Leakage Inductor Voltage, V

V_{on} Transistor On-state Voltage, V

V_{plat} Gate Plateau Voltage, V

V_{th} Gate Threshold Voltage, V

w_1 Weight Factor 1

w_2 Weight Factor 2

w_3 Weight Factor 3

w_4 Weight Factor 4

Greek Symbols

α Duty Cycle, rad

Ω Electrical Resistance, ohm

ω Angular Frequency, rad/s

ϕ SPS Phase Shift, rad

σ DPSM Phase Shift, rad

Abbreviations

2DEG 2-dimensional electron gas

AGD Active Gate Driver

APM Auxiliary Power Modules

BESS Battery Energy Storage System

BEV Battery Electric Vehicle

CHFL-DAB Cycloconverter-type High Frequency Single-Stage Isolated DC/AC Converter

CM Common Mode

CMTI Common Mode Transient Immunity

DAB Dual-Active Bridge

DPSM Duty and Phase Shift Modulation

DPT Double Pulse Test

ESS Energy Storage System

FB Full-Bridge

FOM Figure of Merit

GaN Gallium Nitride

HEMT High Electron Mobility Transistors

IMS Insulated Metal Substrate

LiDAR Light Detection and Ranging

LUT Lookup Table

OOK On-Off Keying

PCB Printed Circuit Board

PV photovoltaic

PWM Pulse Width Modulation

RF Radio Frequency

SEI Solid Electroylte Film

SHC Second Harmonic Current

Si Silicon

SiC Silicon Carbide

SPS Single Phase Shift Modulation

WBG Wide Band Gap

ZCS Zero Current Switching

ZVS Zero Voltage switching

Chapter 1

Introduction

1.1 Motivation

Power electronics are crucial for energy storage systems. They dictate the efficiency of power transfer from one electrical source to another and are necessary when translating between AC and DC power. As society reduces its dependency on fossil fuels, renewable sources such as photovoltaic to wind power are becoming more important to fill the energy void left by oil and gas. However, renewable sources suffer from the inability to meet consistent demand, if it is not sunny or windy then there is no power to be supplied. Energy storage systems (ESS) are critical for solving this issue especially with society's increasing energy needs. ESS offer flexibility as energy can be stored during periods of low generation cost, low demand or from sources that do not produce a continuous or reliable stream of usable energy such as the aforementioned photovoltaic (PV) or wind power [1].

Of the possible ESS, battery energy storage systems (BESS) are well suited for electrical energy storage applications since they can be easily integrated into the grid,

provide a sink for power, and can quickly respond to changes in demand. Batteries are also very efficient and can maintain their stored energy for long periods of time [1]. Currently the climate crisis has increased the amount of focus on BESS as many industries and researchers are focusing on alternatives to oil and gas in order to reduce CO^2 emissions. Because of this, there has been an increased adoption of BESS for home and automotive applications [2].

The adoption of the BESS into the electrical grid is also needed in order to reduce the greenhouse gas emissions. Electrification of transportation is not enough if the increased demand of electrical power is sourced from fossil fuel burning plants. The adoption of BESS into the electrical grid has many advantages beyond being a necessity for climate control. Currently utility companies must have the ability to match real time peak demand, this often means that in a given year the generated power is a fraction of the total capacity, around 55% [3]. This disparity in capacity and actual electrical demand has a cost, new generating stations must be made much larger and they run at a lower efficiency. Increasing the amount of BESS has the additional benefit of allowing the decentralization of the power grid. Currently there are large power generation facilities responsible for the distribution of power to many consumers, by creating micro-grids the distributed power can be generated much closer to the end consumer thereby increasing transmission efficiency [4]. Thus, with the amount amount of BESS in service the demand for high power density and efficient power electronics to interface between the load and BESS is continually increasing. This demand has lead researchers to incorporate WBG devices like GaN because the improvement of Si is no longer satisfactory as it approaches the material limit. In addition to this, the conventional isolated two-stage approach that is

commonplace when interfacing a battery with an AC load needs to be challenged because this solution does not necessarily offer the highest reliability, efficiency or power density.

1.2 Power Electronics for BESS

Most electronics and the power grid are AC power, they cannot directly interface with the DC power of a BESS. Thus, high efficiency, high power density, long lifetime and high reliability are requirements for an isolated battery driven converter. Galvanic isolation is required to protect the consumer from shock in addition to breaking ground loops. A Transformer can be used for galvanic isolation but in order to interface with the 50-60Hz AC grid, the size requirement to achieve the volt second balance would not be practical. Thus, a switching frequency upwards of 10kHz can be used to achieve a more practical size. Continuously increasing the switching frequency yields a smaller converter design at the cost of power losses as the rate at which the device transitions from its on-state to off-state and vice versa is increased. In order to achieve higher switching frequencies and increased efficiency, the losses generated during these transition periods must be decreased, this can be achieved with WBG devices that offer superior switching transitions times.

1.2.1 Wide Band Gap Devices

Wide band gap devices (WBG) such as gallium nitride (GaN) and silicon carbide (SiC) are relatively new compared to traditional silicon devices which have been in use since the 1950s [5]. The need for continuous improvement of technology has researchers

focused on looking for ways to improve efficiency while making the devices more compact. Achieving the desired improvement to technologies with Si devices is becoming increasingly difficult as the technology approaches its limit [6] thus, researchers have been adopting WBG devices due to their promising characteristics. WBG devices are expected to outperform Si due to their better figures of merit (FOM) as well as a better theoretical limit for their on-state resistance [7]. There are 5 key qualities associated with WBG devices [8]:

- High dielectric strength
- Ability to operate at high temperatures
- High current density
- fast switching speeds
- low on-state resistance

Of these attributes on-state resistance and switching speed are very important to power density and efficiency, these characteristics are directly related to the physical characteristics of WBG devices summarized in 1.1.

Table 1.1: Physical Properties of Silicon and WBG devices [9]

Electrical property	Units	Si	SiC	GaN
Band gap energy	eV	1.12	3.26	3.39
Electron mobility	Cm^2/V-s	1300	950	800 / 1700
breakdown field	V/cm	$0.3x10^6$	$3x10^6$	$3.9x10^6$
saturation drift velocity	Cm/s	$1x10^7$	$2x10^7$	$1.4x10^7$
thermal conductivity	W/cm-K	1.5	3.8	2.46

Band gap energy is related to the blocking voltage of the device and allows them to be manufactured much smaller and thinner when compared to a silicon device of

similar voltage rating. Not only is the power density improved by reducing the size but the parasitic capacitance associated with the device also decreases. These two features make WBG devices much more attractive for many power electronic applications as they enable higher switching frequencies and efficiency. Table 1.1 might suggest that one WBG device should be a better option for use in high frequency applications and that there is a direct competition for GaN and SiC. However, these devices can coexist with each other as their different materials offer characteristics unique to each device which means the performance will depend on the application. Typically, SiC are preferred for high power due to their high thermal conductivity while GaN are used for higher frequency, medium power applications such as isolated converters for BESS [10]. The breakdown of each material and its preferred application is shown in Fig. 1.1.

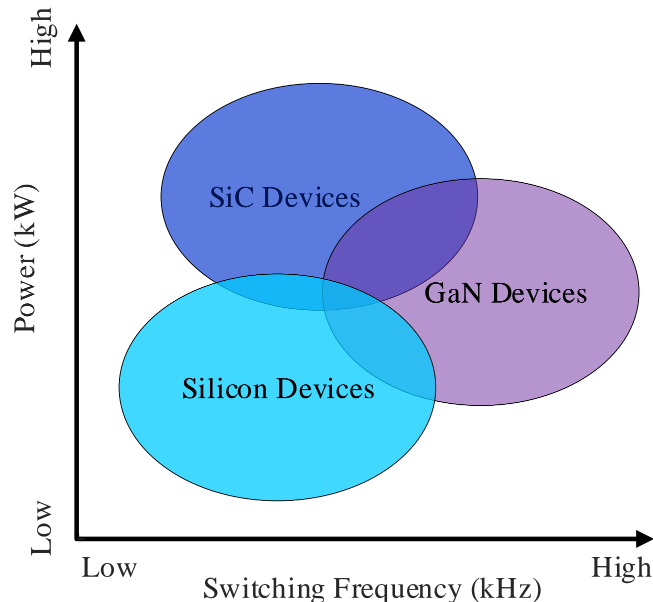


Figure 1.1: Application overlap of transistor technologies.

1.3 GaN Enhancement Mode Devices

GaN is a fairly new technology compared to silicon and thus there are a lot of GaN transistors entering the market with many companies currently offering 3rd, 4th and 5th generation devices. GaN technology is constantly improving and is poised to make a big impact on commercial products by offering high efficiency and compact sizes for things like laptop chargers, or isolated converters for BESS. A recent review [11] has compiled a table of commercially available GaN e-mode devices. However, Table 1.2 offers additional GaN devices that have come to the market since the review.

Table 1.2: Physical Properties of Silicon and WBG devices.

Manufacturer	Voltage Rating(V)	Current Rating(A)	R_{dson}(mΩ)	Q_g(nC)	Package
EPC [12]	100	16	5.6	5.2	BGA
	200	11	18	2.9	BGA
	200	32	7	8.2	BGA
GaN Systems [13]	100	120	5	18	Near-Chipscale
	650	120	12	25	bare-Die
Panasonic [14]	600	26	56	5	DFN
Infineon [15]	400	31	55	4.5	PG-DSO-20-87/PG-HSOF-8
	600	23	140	3.2	PG-HSOF-8
	600	60	55	5.8	PG-DSO-20-87/PG-HSOF-8

1.3.1 Advantages

Comparisons between transistor technologies never come to a definitive conclusion of which device is ultimately best, each has advantages and disadvantages making it suitable for some tasks and not others as illustrated in Fig. 1.1. Table 1.3 shows a list of key device parameters related to performance for Si, SiC and GaN. To highlight one such comparison, the parasitic capacitance of GaN are much lower than SiC and Si, large parasitic gate-drain and gate-source capacitances prevent the gate from quickly reaching the voltage necessary to fully saturate the switch, this means that the VI-overlap time will be longer resulting in higher switching losses. GaN have extremely

fast turn off and turn on speeds in the order of 10ns because the aforementioned capacitances are very low making GaN suitable for applications with frequencies above 1MHz [16, 17]. Fig. 1.2 shows a graph of available technologies with the year they were released vs Figure of merit (FOM) which is the product of on-state resistance and gate charge. GaN devices offer incredibly low on-state resistance in a package size that is smaller than SiC and as a result typically outperform both SiC and Si in regards to the FOM. FOM is a good tool for comparing transistors because it is desirable to have a small value for both the on-state resistance and gate charge. These parameters have an inverse relationship meaning devices with low on-state resistance are typically larger with relatively higher parasitic capacitances and larger gate charge.

Table 1.3: Physical Properties of Si and WBG devices.

Manufacturer	Material	V_{ds}(V)	$I_{ds}(A)$	R_{dson}(mΩ)	C_{iss}(pF)	C_{oss}(pF)	C_{irss}(pF)	Q_g(nC)
Infineon IPW60R105CFD7	Silicon	600	21	89	1752	33	10	42
Cree C3M0120090J	SiC	900	22	120	350	40	3	17.3
GaN Systems GS66506T	GaN	650	22.5	67	195	49	1.5	4.4

1.4 Research Objectives

Although the previous sections outlined all the advantages of GaN devices, currently there is a challenge in translating the benefits at the device level to the converter level. Therefore, comprehensive design guides for GaN converter are not in place. The main challenges are loss estimation, measurement, PCB design and gate driver design. This is why the loss breakdown, measurement techniques, PCB layout, and gate driver design guidelines for GaN are investigated.

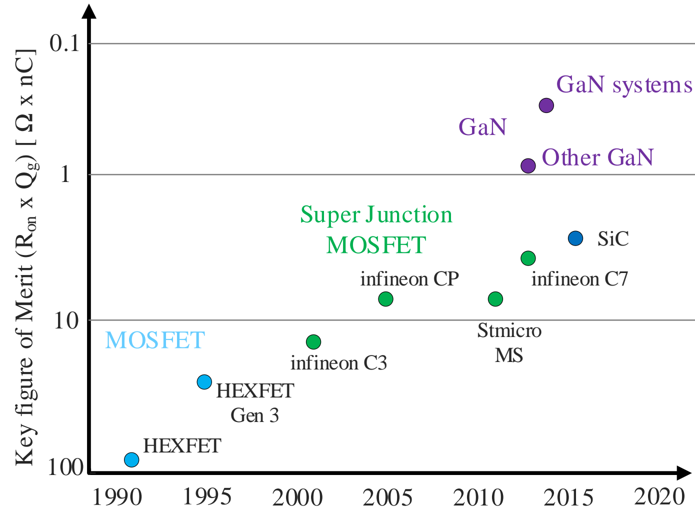


Figure 1.2: GaN figure of merit comparison to other available transistors.

Therefore, this thesis has taken a further look at designing power electronic converters with GaN. The effectiveness of GaN has lead to its incorporation in a cycloconverter-type high frequency single-stage isolated DC/AC converter (CHFL-DAB) and to that end an optimal control scheme is needed to operate the converter. In particular, the thesis attempts to tackle the following objectives:

1. Consolidate and analyse the loss mechanisms of GaN
2. Development of an optimal control scheme for a CHFL-DAB
3. Investigate the PCB and Gate driver requirements and considerations for GaN devices
4. Develop prototype to validate the proposed control scheme.

1.4.1 Publications

During the time spent working on the thesis, other research projects that dealt with power electronics were undertaken. Below is a list of all the published journal papers and conferences as a result of the work during this MaSc program:

[J1] J. Gareau, R. Hou and A. Emadi, ”Review of Loss Distribution, Analysis and Measurement Techniques for GaN HEMTs,” in *IEEE Transactions on Power Electronics* doi: 10.1109/TPEL.2019.2954819

[J2] P. Azer, R. Rodriguez, J. Guo, J. Gareau, J. Bauman, B. Bilgin, and A. Emadi, “Time Efficient Integrated Electro-Thermal Model for a 60 kW 3-Phase Bidirectional Synchronous DC-DC Converter” in *IEEE Transactions on Industry Applications* doi:10.1109/TIA.2019.2948804

[J3] J. Gareau, L. Dorn-Gomba and A. Emadi, ”Improved Control for Isolated Cycloconverter-type Dual Active Bridge DC/AC Converter,” 2020 *IEEE Transportation Electrification Conference and Expo (ITEC)*, Chicago, IL, 2020, pp. 1-7. *Accepted*

[J4] J. Gareau, B. Bilgin and A. Emadi, ”Power Inductor Optimization Using Nonlinear Magnetization Characteristics,” 2020 *IEEE Transportation Electrification Conference and Expo (ITEC)*, Chicago, IL, 2020, pp. 1-7. *Accepted*

1.5 Thesis Outline

The thesis consists of eight chapters including the introduction chapter. The introduction chapter provides the motivation for the adoption of GaN in high efficiency DC/AC converters by showing the merits of GaN over Si and SiC, namely the ability

to switch at high frequencies with low losses. The increased use of BESS has lead to a larger demand for compact, highly efficient isolated converters which makes GaN a highly attractive option for these systems. If the efficiency and power density can be improved for the DC/AC converters used to interface with BESS than these systems become even more attractive to consumers as their reduced energy consumption leads to lower energy bills and the size reduction makes them lighter weight and more aesthetically pleasing for the consumer to have in their home. Next, the loss mechanisms of GaN is presented in Chapter 2 and a review on modelling and measurement techniques for GaN is provided in Chapter 3.

The dual-active bridge converter is presented in Chapter 4 which is necessary for the analysis and development of the optimal control for the proposed converter in Chapter 5. Before a prototype is developed, the design considerations for the PCB and gate driver of a GaN based converter are discussed in Chapter 6. Finally, in Chapter 7 the prototype is designed and presented including simulation and experimental verification of the proposed control and the desired output behaviour.

Chapter 2

GaN Power Loss Mechanisms

2.1 Introduction

The Si based switches, like MOSFET and IGBT, are the legacy switch devices that have been used in various power converters designs. The methods to estimate the losses introduced from the MOSFET and IGBT have been well developed [18, 19]. Si switch devices have seen repeated technological improvements throughout their lifetime. However, it has now become apparent that this improvement cannot continue indefinitely as the device performance is limited by the material properties. The inclusion of WBG semiconductors in power converters is a necessary step to secure continued performance enhancement in power electronic systems [20–22]. GaN power switch devices recently have gained great popularity in both academia and industry, due to their better FOM versus conventional MOSFETs. So far, vertical GaN devices have not yet been produced on a commercial level. The commercially available GaN devices are most likely to be a lateral structure [22]. The device structure comparison between vertical Si MOSFET and lateral GaN enhancement-mode

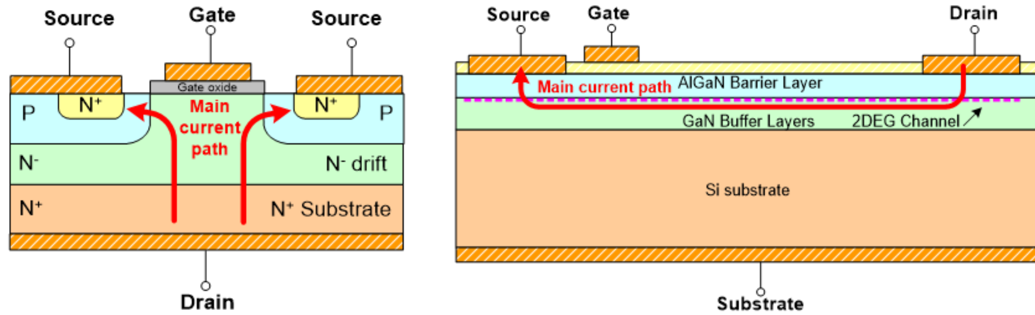


Figure 2.1: Transistor structure, (a) vertical Si MOSFET, (b) lateral GaN HEMT.

high electron mobility transistors (HEMTs) is shown in Fig. 2.1. GaN HEMTs have excellent performance and relatively high charge density and mobility. GaN differs from other transistors because of its 2-dimensional electron gas (2DEG). The 2DEG is a byproduct of the heterointerface between the GaN layer and AlGaN layer. The incorporation of GaN HEMTs into both soft-switching and hard-switching applications leads to many potential benefits due to the device performance. Using GaN HEMTs is beneficial when operating the switches with the zero-voltage switching (ZVS) technique, this is due to their much smaller parasitic capacitance compared to a conventional Si MOSFET. As the device capacitance is decreased, the required inductance needed to charge and discharge this capacitance is also reduced, resulting in a more compact converter. Small gate charge makes GaN devices suitable for hard switched converters as the duration of the VI overlap is much shorter than Si, in addition to the gate drive losses being reduced as well. GaN devices also do not contain a physical body diode which results in zero reverse-recovery losses. Therefore, GaN devices introduce lower switch on/switch off losses in hard switched converters [23–25]. In fact, GaN HEMTs are being incorporated into many power converter topologies and applications. These applications include AC adapters for consumer electronics, wireless chargers, light detection and ranging (LiDAR), onboard chargers, isolated

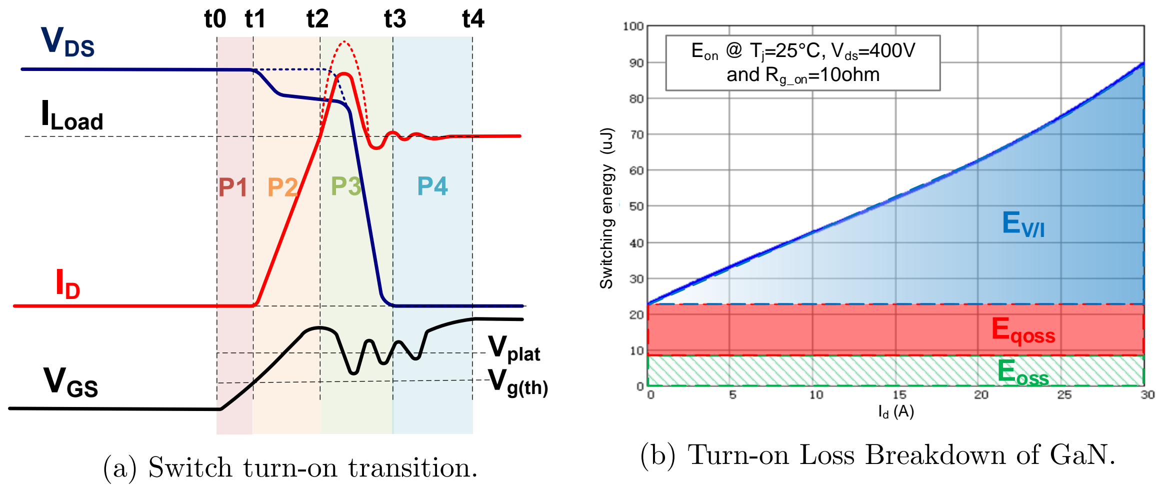
DC/DC auxiliary power modules (APM), and traction inverters [26–32]. With the increased usage of GaN devices, it becomes important for both researchers and engineers to understand how GaN devices differ from Si devices in terms of losses and how to appropriately measure these losses. However, there are not many papers that discuss and review the comprehensive loss distribution, loss analysis, and measurement techniques for GaN-based applications. In this chapter, the detailed E_{on}/E_{off} switching loss composition and percentage for GaN and the advantages of GaN compared to Si MOSFET in terms of loss are presented. Moreover, the dynamic on-state resistance (R_{dson}) is reviewed as this is becoming an emerging question about GaN devices.

2.2 GaN Power Loss Mechanisms

In general, similar to Si devices, the losses for GaN can be mainly divided into conduction losses and switching losses. While the detailed loss composition for GaN device differ from Si's. Therefore, care should be taken when analysing a converter developed with GaN such that the losses are accurately estimated. For GaN, the conduction loss includes the R_{dson} loss at 25°C, R_{dson} loss from heating effect, R_{dson} loss from trapping effect (also known as dynamic R_{dson} loss), and deadtime loss; the switching loss includes turn-on/turn-off VI overlap loss, E_{qoss} and E_{oss} losses. It is also noticed that under very high frequency, there is another type of loss called C_{oss} capacitance hysteresis loss which has drawn some attention for radio frequency (RF) applications.

2.2.1 VI Overlap Loss

Power loss is defined as the area of overlap between voltage and current waveforms. For semiconductor devices, the ideal operation is to have zero current through the switch in the off state and zero voltage across the switch in the on state. Both of these requirements are achieved instantaneously when a device transition is required. In practice, there is some V-I overlap as the devices transition from off to on and vice versa. For turn-on, each switching transition can be broken down into four segments. The stages for an on transition are detailed below and summarized by Fig. 2.2a and its loss breakdown is shown in Fig. 2.2b.



(a) Switch turn-on transition.

(b) Turn-on Loss Breakdown of GaN.

Figure 2.2: Switching characteristics.

- Period 1 turn-on delay (t_0 t_1): The device begins to transition into the on state when a positive gate voltage is applied. During this stage, the device remains off until the gate reaches the threshold voltage.
- Period 2 current rise (t_1 t_2): Once the gate voltage has reached the threshold, it continues to rise, with the channel current directly related to the gate voltage.

- Period 3 voltage fall time (t_2 t_3): Once the current has reached its full load value, the voltage begins to fall to its on-state value. The equivalent circuit is shown in Fig. 2.3.

- Period 4 oscillations (t_3 t_4): Once the voltage has reached its on-state value there may be some oscillations due to resonance. The gate voltage also rises from the plateau value to the steady-state value.

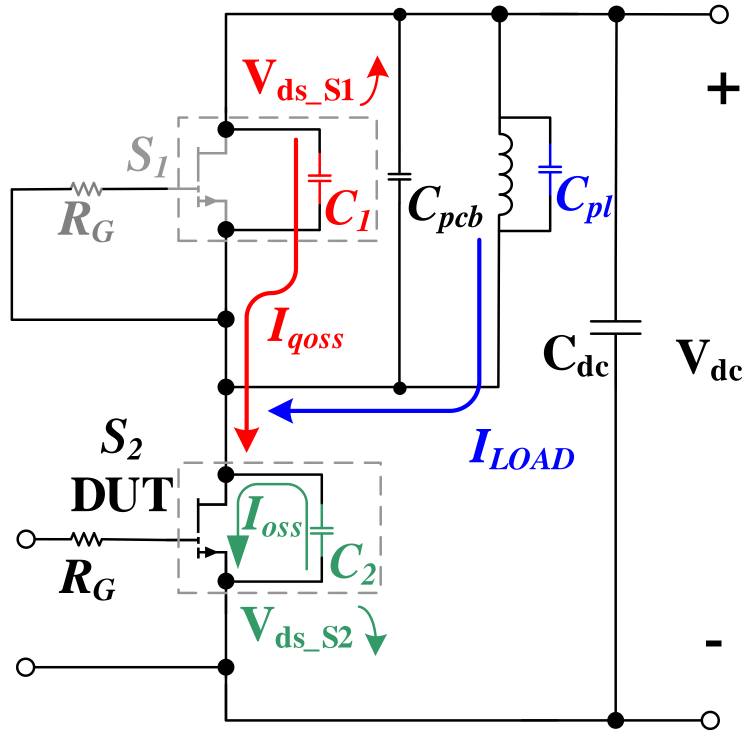


Figure 2.3: Equivalent circuit during the switching-on voltage commutation transition.

2.2.2 Capacitance Loss E_{oss}

E_{oss} loss is the energy lost in charging the parasitic capacitance of the switch. This energy is lost during turn-on as the capacitance is discharged through the channel of

the switch. The equation for E_{oss} is described in 2.1.

$$E_{oss} = \int_0^{V_{dc}} V_{ds} C_{oss}(V_{ds}) dV_{ds} \tag{2.1}$$

2.2.3 Capacitance Loss E_{qoss}

E_{qoss} is defined as the loss introduced from the capacitor charging current of the opposite switch in a half bridge configuration [25]. In a conventional Si MOSFET half bridge, during the turn-on transition, the current bump includes E_{qrr}, E_{oss}, and E_{qoss} losses, as shown in Fig. 2.4 (a) [19]. With the lack of reverse recovery loss, E_{qoss} becomes more obvious for GaN HEMT as shown in Fig. 2.4 (b). The equation for E_{qoss} is defined as:

$$E_{qoss} = \int_0^{V_{dc}} (V_{dc} - V_{ds}) C_{oss}(V_{ds}) dV_{ds} \tag{2.2}$$

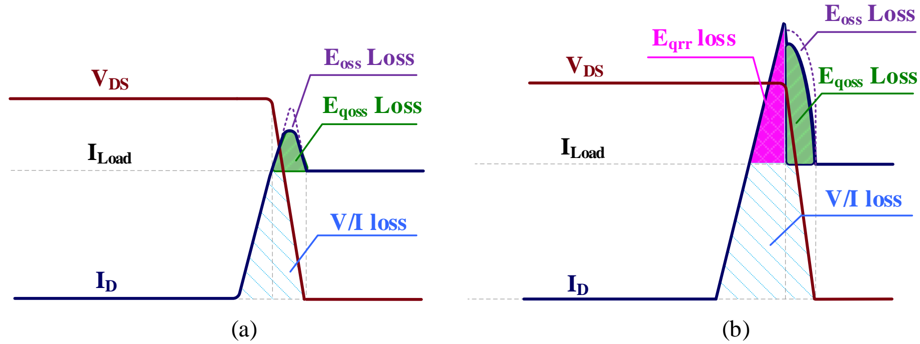


Figure 2.4: Hard-switch turn-on losses distribution (a) Si MOSFET, (b) GaN HEMT.

The mechanism for this E_{qoss} loss is that when the upper switch turns off, its output parasitic capacitance C_{oss} needs to be charged. This charging current has to travel through the low side switch which will generate additional losses. E_{qoss}

and E_{oss} both deal with the same capacitive component of the switch, thus the total charge of each is the same. However, they contribute different amounts of losses due to the different conditions surrounding them. For E_{oss} loss the initial drain-source voltage V_{ds} is equivalent to the DC-link voltage V_{dc} and is discharging to zero. For E_{qoss} the initial drain source voltage is close to zero and the switch is charging to the DC link. Thus, the total energy dissipated is different as described by (2.1) and (2.2). It is important to note that the parasitic capacitances from the printed circuit board (PCB) and power inductor will also contribute to this loss, which will be discussed later. In fact, The C_{oss} comparison among Si MOSFET C7 and CFD

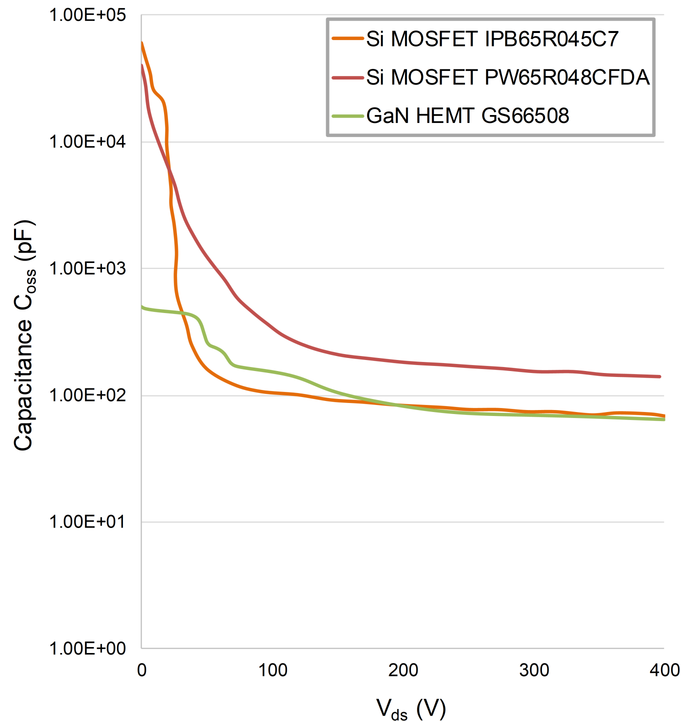
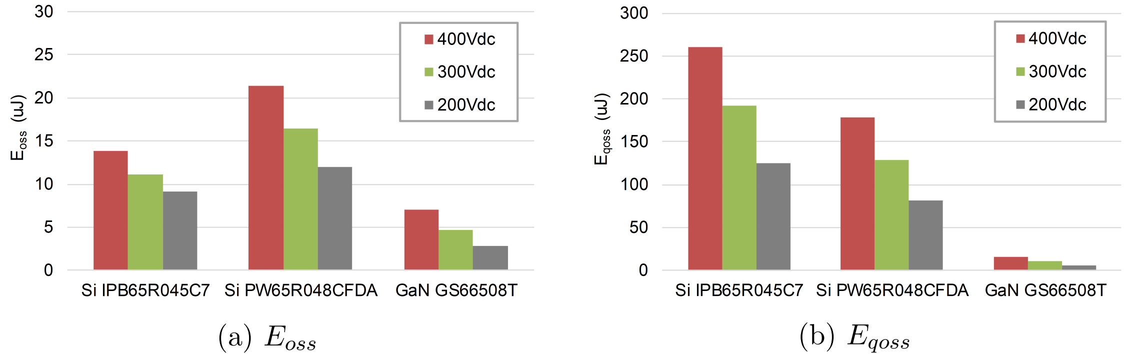


Figure 2.5: C_{oss} comparison between Si MOSFET and GaN HEMT.

and GaN HEMT are shown in Fig. 2.5. It is clear that the total C_{oss} of GaN is lower compared to Si MOSFET. This indicates a lower E_{oss} energy loss from GaN



(a) E_{oss} (b) E_{qoss}

Figure 2.6: Comparison between Si MOSFET and GaN HEMT under different voltages.

compared to Si MOSFET. Moreover, the Si MOSFET's are highly non-linear. This will make the E_{qoss} loss even larger. The comparisons for E_{oss} and E_{qoss} between Si MOSFET and GaN HEMT at different voltages are also shown in Fig. 2.6a and Fig. 2.6b, respectively.

2.2.4 Dynamic On-state Resistance Loss

Dynamic on-state resistance loss is a by-product of the so called dynamic R_{dson}. It is due to charge trapping effect of electrons and results in a decrease of the 2DEG density. This change in resistance will cause additional loss for the GaN based power electronic applications. Typical on-state resistance for most Si devices is affected by device channel current and temperature. However, recent research has shown that the increase in resistance for GaN devices exceeds what would be expected when accounting for temperature and current. This resistance increase is associated with charges becoming trapped due to material defects. The traps are a by-product of manufacturing lateral type GaN which has a buffer layer between the substrate and GaN, the buffer layer needs to have a large resistance to prevent leakage currents

[33]. Thus, manufacturers use iron and carbon inside the buffer to increase this resistance, but these impurities lead to the aforementioned traps that reduce the flow of current through the channel. Dynamic R_{dson} is not provided in manufacturers' datasheets but cannot be neglected as it represents additional losses and will cause a decrease in efficiency. These aspects are important as they can lead to extra junction temperature increase if not accounted for appropriately such as when considering the cooling system for a converter. Fig. 2.7 shows the layers of the GaN device and the space charges that can arise due to the traps. It also illustrates that there have been two types of traps reported: surface and buffer. Several impacting factors have been investigated by researchers to examine effects on the R_{dson}, a summary of these impacting factors is presented in Fig. 2.8. The low impact of temperature on dynamic R_{dson} is due to the fact that temperature only has a noticeable effect with a relatively long-time scale. In other words, under a real switching condition, the impact of temperature on the trapping effect is almost negligible [34, 35]. Hard/soft switching has been investigated as well and appears to be an outlier factor for Panasonic devices which contain a slightly different structure utilizing a second drain. An important distinction in the impacting factors is that while frequency and duty have been shown to affect dynamic on-state resistance [36], this effect is only note-worthy in cases where the resistance has been increased beyond its nominal value. In other words, duty cycle and frequency do not contribute to the trapping of charges that causes the resistance to increase. Fig. 2.9 gives an overview of dynamic on state resistance in a switching cycle. Its interval can be divided into a trapping phase in the off-state and a de-trapping phase in the on-state. When under a large voltage stress, charges flowing into the buffer become trapped during the off state. Once the device switches on

de-trapping occurs and the electrons are able to be freed. This effect can be observed as a change in the channel resistance.

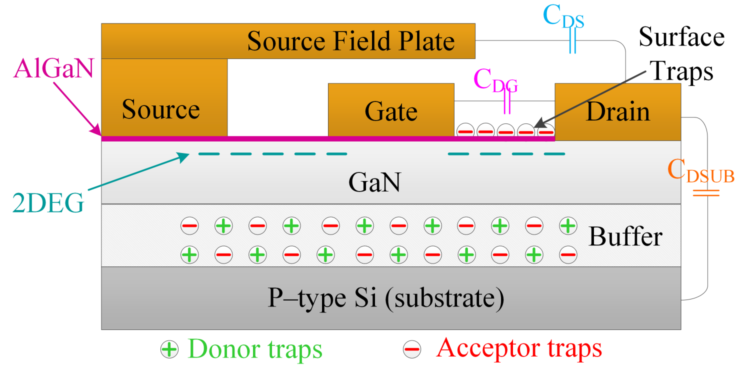


Figure 2.7: Lateral GaN device with traps.

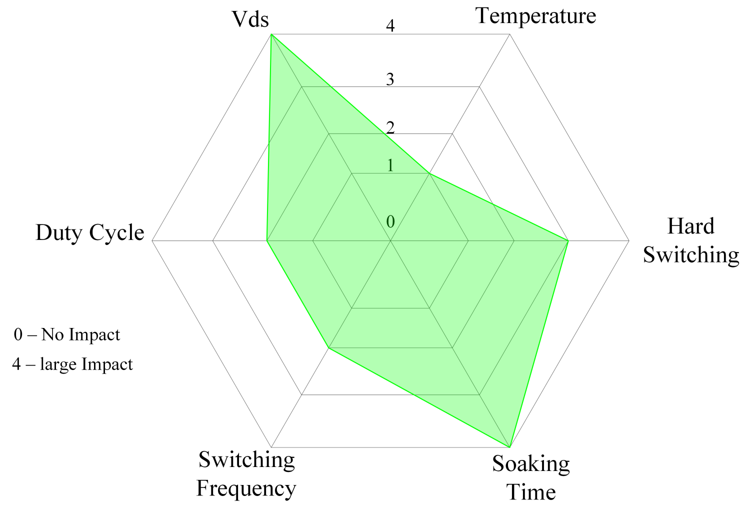


Figure 2.8: Impact factors of dynamic R_{dson}.

2.2.5 Dead Time Losses

Dead time is necessary for proper current commutation of switches and to avoid accidental shorting of phase legs. Dead time also has the additional function that

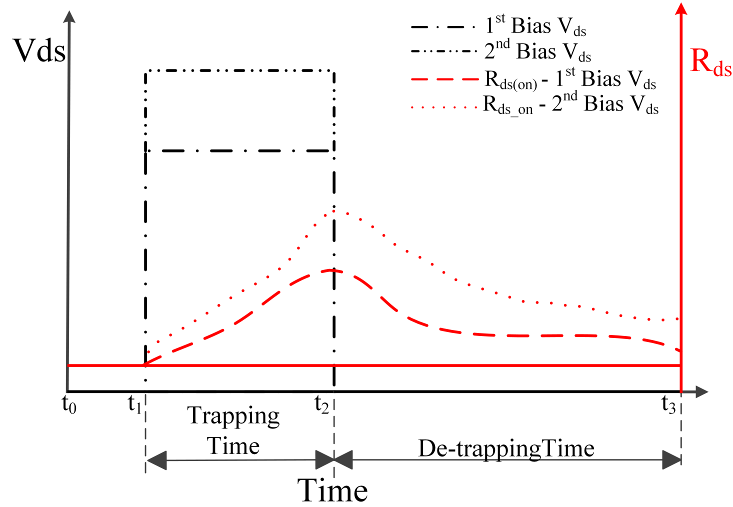


Figure 2.9: Effect of trapping and de-trapping process on dynamic on-state resistance.

allows some converters to operate in a zero voltage or zero current switching state by allowing the parasitic elements of the circuit to discharge. GaN devices do not have a parasitic body diode to conduct reverse current, thus they have no reverse recovery losses. However, they are still capable of conducting current reversely through the same channel when its gate is off and the behaviour for this is similar to a body diode. In order to prevent accidental turn-on, GaN devices are often recommended to use a negative gate voltage for the off-state. This negative gate voltage is added to the voltage drop across the channel resistance leading to more losses with a more negative V_{gs}. The device V_{ds} for various V_{gs} is shown in Fig. 2.10, V_{ds} is larger for the more negative turn off voltages. Compared to the parasitic body diodes found in Si, the voltage drop of a GaN device during reverse conduction is much higher which is the cause of the increased losses [37, 38]. Adding a Schottky diode in parallel can improve the dead time loss by fixing the forward voltage drop, but this introduces reverse recovery losses. Another solution to this problem is a method that requires the

overlap of the gate signals in a phase leg during switching transition, by ensuring they have a cross over point that is lower than the threshold voltage ZVS and minimized reverse conduction losses are achieved by virtue of using the minimum dead time [39]. It should be noted that the test set-up has an input voltage of 25 V to 50 V and power ranging from 50 W to 200 W. This method is not suitable for higher operating conditions with the 650 V GaN devices as dv/dt and di/dt may be much higher and overlapping gate signals may lead to shoot through.

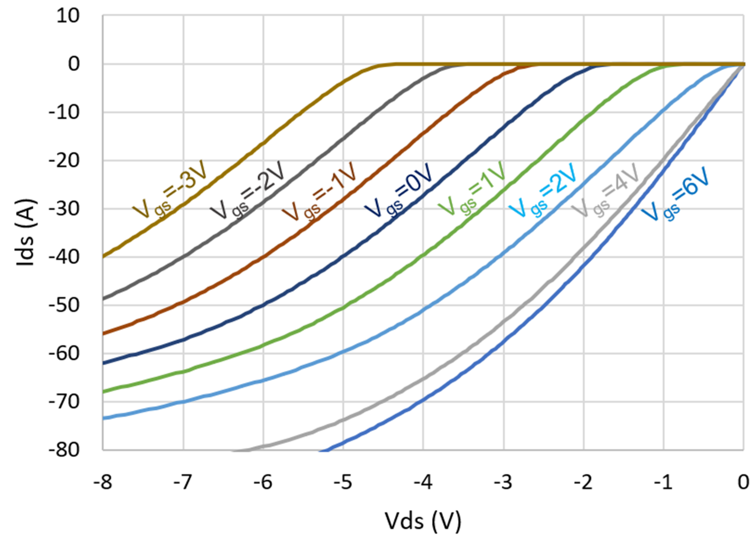


Figure 2.10: GaN reverse conduction characteristics.

2.2.6 Gate Driver Loss

The gate driver loss mechanism for GaN and Si are quite similar. However, due to the relatively small gate charge Q_g, the gate driver loss from GaN is smaller compared to Si's. Q_g comparison between Si MOSFET and GaN HEMT is shown in Fig. 2.11. GaN HEMT obtains 40 times smaller Q_g compared to a Si MOSFET with a similar

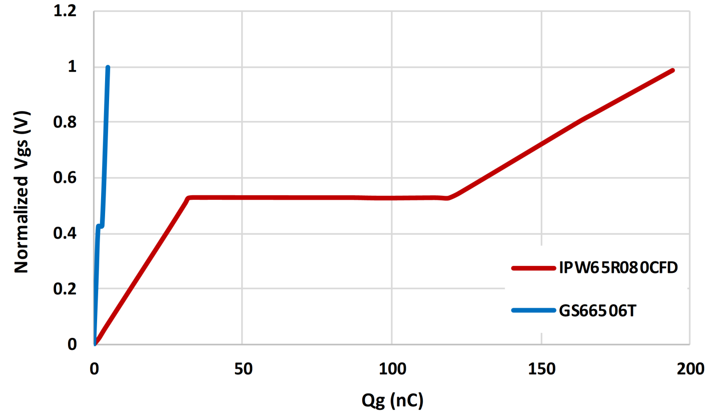


Figure 2.11: Q_g comparison between Si MOSFET and GaN HEMT.

R_{dson} value. The gate driver loss can be estimated with the equation:

$$P_{driver} = V_{gon} Q_g f_s \tag{2.3}$$

As a result, the gate driver loss comparison under different switching frequency can be obtained in Fig. 2.12. Under 1 MHz, the loss difference is about 2 W. This can be a large loss difference for low power applications, such as high frequency adaptors, etc.

2.2.7 Capacitance Hysteresis Loss at Higher Frequency

The losses associated with the output capacitance of the device also appear to show some sort of dynamics as researchers have reported in several works [40–44]. The importance of these findings is that a larger device die with smaller R_{dson} may not lead to a more efficient converter as the C_{oss} losses can begin to dominate at high frequency operation. The losses were first noticed when GaN switches were used in an RF rectifier circuit with their source and gate tied together such that it acted as a diode.

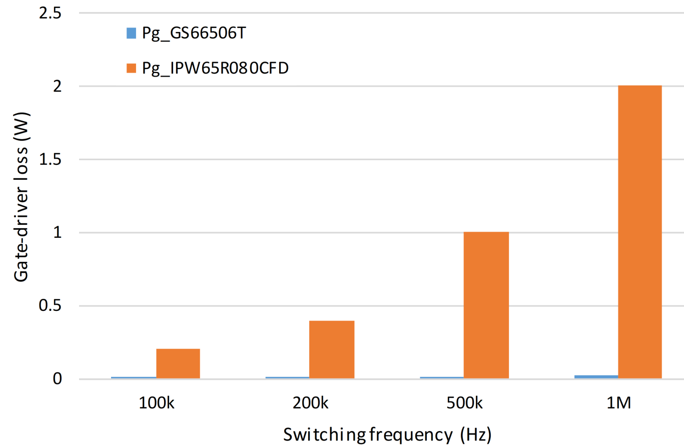


Figure 2.12: Gate driver loss comparison under different switching frequencies.

The measured performance was much lower than simulation results, this lead to the hypothesis that the increase in losses is a result of the output capacitance of the device or the dynamic R_{dson} [43]. In order to isolate the effects from dynamic R_{dson}, several experiments have been performed using the GaN device as a capacitor by tying the gate to source and connecting it in parallel with a switching device. These tests have noted significant heating on the off device even when considering the possibility of thermal cross coupling [40–42]. In order to quantify the losses, a sawyer tower circuit is used. The premise of this circuit is that a capacitor with linear characteristics is connected in series to the device held in the off position. Capacitors connected in series must have equal charges which means that a voltage measurement on the reference capacitor can be used to deduce the charge and therefore the losses of the switch. dv/dt is hypothesized to be responsible for the increase in losses, this is tested at a constant frequency with different wave shapes containing different frequency components(sine, square, Class-Φ2 waveform) [40]. The results show that the waves with larger dv/dt result in larger energy dissipated per cycle which agrees with the

previous notion of higher frequencies resulting in larger losses. In a continuation of these efforts to reduce the losses, the trapping effects in the buffer layer must be alleviated. In order to achieve this goal, a negative voltage bias is applied to the substrate. However, this mainly reduces the capacitance between the drain and substrate. The substrate capacitance is a part of the C_{oss} thus, any reduction in that value will reduce the total E_{oss}. The results show that despite decreasing the losses the dv/dt trend is not removed [42].

2.2.8 Effect of Device Parasitics on Losses

The parasitic inductances from the device package and system circuit layout don't directly affect losses. However, a relatively bad PCB layout design with large parasitic inductance can create some noise on the signals and impact the system efficiency indirectly. For example, the gate loop inductance might affect the V_{gs} signal and therefore a lower V_{gs} has to be applied. This leads to a higher R_{dson} value and a higher conduction loss; the power loop inductance might create a larger V_{ds} overshoot and therefore a lower operating voltage has to be applied to the system. In other words, by applying a relatively good layout with minimized parasitic inductance, the advantages of GaN in the power electronics system can be fully utilized.

The parasitic capacitances from the PCB and the load inductor can directly affect the losses of the converter. These parasitic capacitances can contribute additional E_{oss}/E_{qoss} losses, which is part of the switching loss. Because the capacitances are voltage-independent, the capacitive loss E_{oss}/E_{qoss} considering the other parasitics

from the circuit are given as,

$$E_{oss} = \int_0^{V_{dc}} V_{ds} C_{oss}(V_{ds}) dV_{ds} + \frac{1}{2}(C_{pl} + C_{pcb})(V_{dc})^2 \quad (2.4)$$

$$E_{qoss} = \int_0^{V_{dc}} (V_{dc} - V_{ds}) C_{oss}(V_{ds}) dV_{ds} + \frac{1}{2}(C_{pl} + C_{pcb})(V_{dc})^2 \quad (2.5)$$

where C_{pl} is the parasitic capacitance from the inductor and C_{pcb} is the parasitic capacitance from the PCB. The E_{qoss} measurement and calculation are also compared to verify the effect of parasitic capacitances on the loss, which is shown in Fig. 2.13.

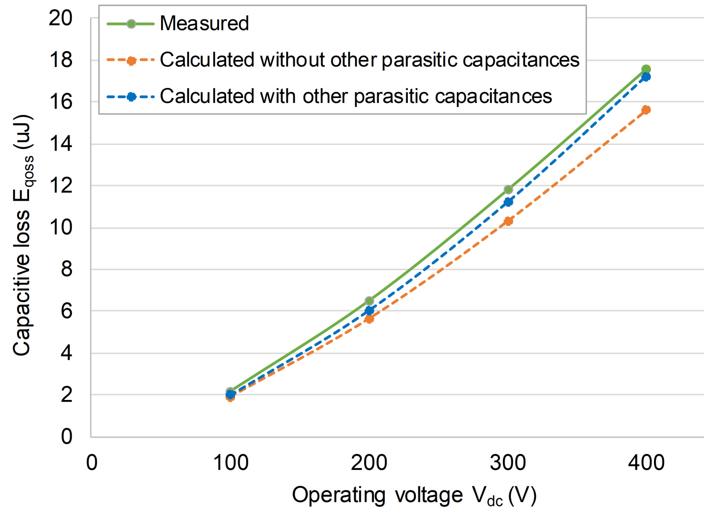


Figure 2.13: E_{qoss} loss with/without other parasitic capacitances from circuit [25].

2.3 Summary

Loss mechanisms for GaN power devices have been presented. GaN is a promising technology, with very low switching and conduction losses. However, there are some uncertainties existing on some factors contributing to small portion losses, such as

the dynamic R_{dson}, dead time losses, capacitance hysteresis loss, and the effect of device parasitics on losses. In general many of these additional loss components are quite small when compared to the total losses that they can be ignored for converter level loss simulation such as using a scaling approach which is covered in the the next chapter. The other additional loss components can be addressed with careful design considerations that will be addressed in later chapters.

Chapter 3

Analysis and Measurement Techniques for GaN HEMTs

3.1 Analytical Models

In Chapter 2, the mechanisms surrounding GaN were reviewed, depending on the converter operating conditions some of these losses may be ignored to simplify the estimation process as this chapter will show the difficulty in modelling the exact behaviour and loss mechanisms of GaN. First, the most basic models will be introduced followed by more complicated techniques that aim to capture a more accurate estimation. Next, alternative loss estimation techniques are considered that can provide accurate results without adding a large amount of complexity. A step-by-step case study on PLECS-based GaN loss modelling is also provided. Finally, this chapter also investigates measurement techniques and considerations for working with GaN including the experimental measurement technique for R_{dson}.

3.1.1 Piecewise Linear Model

The piecewise linear model is one of the most popular and traditional methods for analysing and estimating the losses of a transistor due to the simplicity of the model [20]. The model considers the circuit only in terms of the input capacitance and external gate resistor and thus the current and voltage overlap are determined through the charging time of these capacitors. The piecewise linear model does not provide accurate results due to its exclusion of parasitic parameters and temperature dependency. For example, The transconductance affects the plateau voltage of the device and the current through the channel. Because the transconductance in GaN devices depends on the junction temperature any change in temperature results in a non-negligible impact on the current rise time of the switch and contributes to larger turn on losses.

3.1.2 Improved Models

Several researchers have tried to account for the shortcomings of the piecewise linear model by increasing the complexity of the model by accounting for more dynamics. The more complicated analytical models are similar to the piecewise model in the analysis of the device transition, but they do not make the same simplifying assumptions. Thus, the end result is a more complicated model that accounts for more of the real dynamics that are present in the physical circuit. One example illustrating this concept has been shown in [45], in order to better model the switching losses, the piecewise linear model has been modified to include parasitic elements and the effects of the synchronous transistor. The transfer characteristics are linearized, and then

differential equations are developed to describe the switching process. The model performs quite well when predicting the voltage and current waveforms, however there is still a $10 - 20\%$ error between the measured and actual losses. Similar models for Cascode devices have been developed and report relatively high accuracy with <1% difference between the measured efficiency and predicted efficiency of a buck converter [46]. The discrepancy in accuracy between the Cascode and E-mode models reinforces the notion that additional losses are not accounted for in the E-mode GaN device. Comparisons of the dynamic R_{dson} of Cascode and E-mode devices have been performed and show that the increase in resistance for E-mode devices is higher [36]. One advantage of the previous models' simplification is that the developed equations are far simpler and relatively easy to solve. By using a more realistic approximation for the switching characteristic curves, the experimental dynamics can be approached. The model shown in [47] also considers the V_{gs} dependence of the C_{iss} which is not provided by the manufacturer and has to be derived. This model however still cannot match experimental losses despite mimicking the switching waveforms accurately, the authors cite the error to be within 20%. Transconductance of the GaN device is often neglected in the modelling process as it increases complexity. A good method for maintaining a simple model but allowing it to be useful at all operating points is to use a scaling method. The temperature coefficient for the transconductance of GaN devices is negative which is the opposite of Si and SiC, E_{on} can be scaled accurately using the transconductance value. Extraction of the transconductance values along with scaling methods are provided in [23, 24].

3.1.3 Circuit Simulation Models

Another approach to modelling GaN devices is to build a circuit model that tries to capture the behavior of the device during switching transitions. A GaN model has been developed in [48] that accounts for the reverse conduction characteristics of GaN, the results presented show that the simulated waveforms closely match those of the experimental ones. However, this model is resource intensive as circuit simulations are usually more computationally heavy and require more time to solve. This flaw is coupled with the fact that this model requires significant parameter extraction from the device datasheet. While the authors do present promising results, the lack of any loss estimates makes this method suspect. Other researchers, such as [45] have presented similarly accurate simulation waveforms but still had 10 - 20% error when estimating the losses.

3.2 PLECS Modelling

PLECS offers relatively quicker simulation than SPICE models as PLECS uses lookup tables (LUT) to approximate switching losses, this makes it suitable for system loss analysis of power electronic converters. In this chapter, PLECS modeling is discussed in detail as a case study to present the step-by-step loss modeling for GaN-based applications.

3.2.1 Loss Model

The PLECS device modeling mainly includes three parts. They are the switching loss E_{on}/E_{off}, conduction loss, and thermal impedance. Unlike the SPICE device

model, which determines the semiconductor losses from current and voltage transients, PLECS records the semiconductor's operating condition before and after each switch operation. The critical parameters used to determine the losses are drain current, blocking voltage, and junction temperature. PLECS then uses these parameters to read the resulting dissipated energy from a 3D look-up table.

By applying the aforementioned intrinsic E_{on}/E_{off} loss, the switching loss modelling in PLECS can be built as shown in Fig. 3.1. However, E_{on}/E_{off} is not only determined by the drain current, blocking voltage and junction temperature. The external gate resistance $R_{gon}/\ R_{goff}$ also affects the E_{on}/E_{off} values. In fact, the gate resistance affects the VI overlapping loss, while the capacitive loss E_{oss} and E_{qoss} are independent of the gate resistance. A scaling equation can be used to scale the E_{on}/E_{off} value from one gate resistance to another. This creates a relatively straightforward and accurate way to generate the R_g-dependent E_{on}/E_{off} value in the PLECS software.

The detailed loss modelling can be found in [24], the key equations are detailed here. The VI overlapping loss equation for both turn-on and turn-off can be written

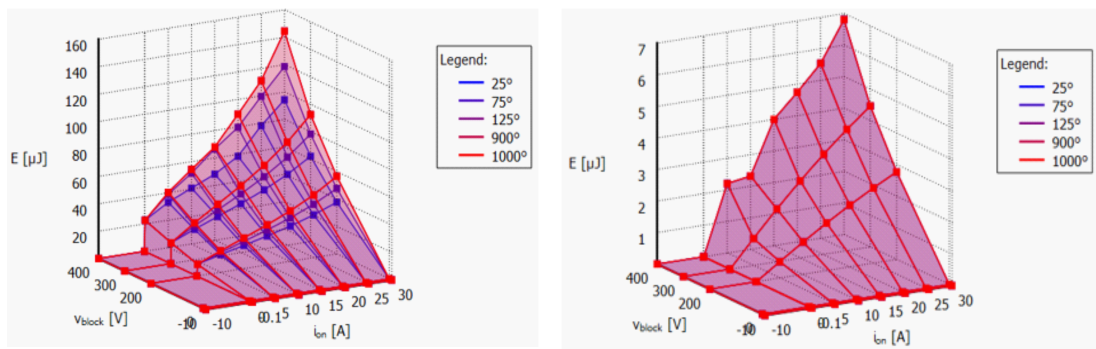


Figure 3.1: Switching loss 3D LUT table, (a) E_{on}, (b) E_{off}.

as,

$$E_{on} = \frac{\frac{V_{ds}I_{ds}}{2}[(Q_{gd}+Q_{gssw})(R_{gint}+R_{gon})]}{V_{gon}-V_{plat}} \tag{3.1}$$

$$E_{off} = \frac{\frac{V_{ds}I_{ds}}{2}[(Q_{gd}+Q_{gssw})(R_{gint}+R_{goff})]}{|V_{goff}|+V_{plat}} \tag{3.2}$$

where R_{gint} is the internal gate resistance of the GaN device, V_{gon}/V_{goff} is the turn-on/turn-off gate voltage, and Q_{gssw} can be obtained by (3.3),

$$Q_{gssw} = Q_{gs}\left(\frac{\frac{I_{ds}}{g_m}}{\frac{I_{ds}}{g_m}+V_{th}}\right) \tag{3.3}$$

Therefore, the E_{on}/E_{off} scaling equation on different R_g can be written as (3.4) and 3.5.

$$E_{on(x\omega)} = (R_{gon(x)} - R_{gon(a)})\frac{\frac{V_{ds}I_{ds}}{2}(Q_{gd}+Q_{gssw})}{V_{gon}-(V_{th}+\frac{I_{ds}}{g_m})} + E_{on(a\omega)} \tag{3.4}$$

$$E_{off(x\omega)} = (R_{goff(x)} - R_{goff(a)})\frac{\frac{V_{ds}I_{ds}}{2}(Q_{gd}+Q_{gssw})}{|V_{goff}|+(V_{th}+\frac{I_{ds}}{g_m})} + E_{off(a\omega)} \tag{3.5}$$

The conduction loss can be extracted by using the I-V curves of the device. The simulated I-V curves are shown in Fig. 3.2.

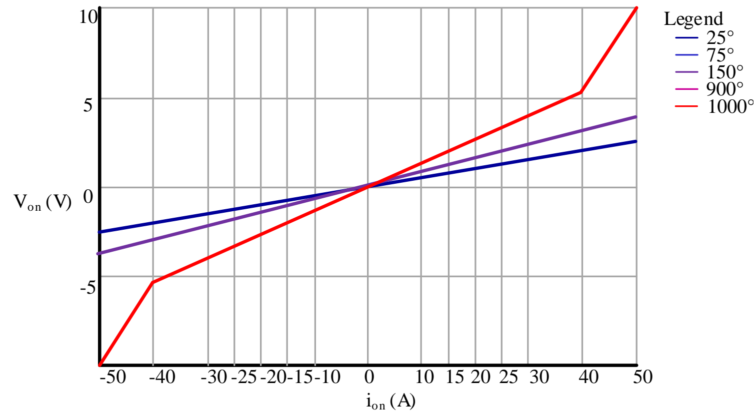


Figure 3.2: I-V curve modelling under different T_j.

The conduction loss can be separated as R_{dson} losses from heating effect and trapping effect. The heating effect can be modelled with different I-V curves under different junction temperatures. The extreme high temperature can be applied as a simulation boundary to avoid extreme thermal runaway and thus lead to the system breakdown. For trapping effect, as explained in Chapter 2, there are many different impact factors, but it is mainly affected by the operating voltage V_{ds} for continuous running applications. Therefore, an equation can be drawn to simulate this part of loss as,

$$V_{on}(V_{ds}) = V\left(1 + k_{Tj} + k_{dR}(V_{ds})\right) \tag{3.6}$$

where k_{Tj} is defined as the increased R_{dson} ratio due to the heating effect and k_{dR} is defined as the increased R_{dson} ratio due to the trapping effect [35]. The k_{dR} factor also varies with the vendors of GaN devices. In fact, this is still an ongoing research topic on the exact values of dynamic R_{dson} [33, 35, 36, 49, 50].

The dead time loss can be modelled by using the following equation in PLECS:

$$V_{on}(V_{ds}) = v - (i < 0)\,(1 - g)(V_{th} - V_{goff}) \tag{3.7}$$

This equation means that once the drain current is in reverse direction and the gate is turned off, there will be an additional on-state voltage drop which is equal to the term $(V_{th} - V_{goff})$ applied onto the total on-state voltage of the device to represent the diode behaviour of GaN HEMT.

Regarding the capacitive hysteresis loss, for most power electronic converters operating below 5 MHz, the impact from this capacitance loss is neglectable. While, for RF or wireless applications operating with a switching frequency above 5 MHz, the

loss will be gradually noticed with the switching frequency increasing. For GaN devices, the loss estimation can be approximated with a Steinmetz fit according to [40]:

$$E_{osshy} = K f_s^{\alpha} V_{ds}^{\beta} \tag{3.8}$$

where K, α, and β are Steinmetz parameters and will vary according to the device used. [40] provides a list of Steinmetz parameters for several commercially available GaN devices.

In fact, for the application scope with very high switching frequency, the PLECS simulation might no longer be a good way to simulate the overall system. Other simulation approaches should be considered.

3.2.2 Thermal Modelling

The last part of the PLECS device modeling is the thermal impedance. The detailed thermal model of GaN HEMT can be found in [51]. The model is based on Cauer RC thermal network and includes four stages. As shown in Fig. 3.3, each stage of the RC parameter is assigned to the corresponding package layers; copper base, attachment, Si substrate, and GaN layer. In addition, curve-fitting is applied to tune and improve the accuracy of the thermal model.

3.2.3 System Simulation based on PLECS

A GaN-based synchronous buck converter is built to verify the PLECS device model. The applied GaN device is GS66508T. The converter is operating under 200 kHz switching frequency, input voltage is 400 V, and output voltage is around 193 V. As a

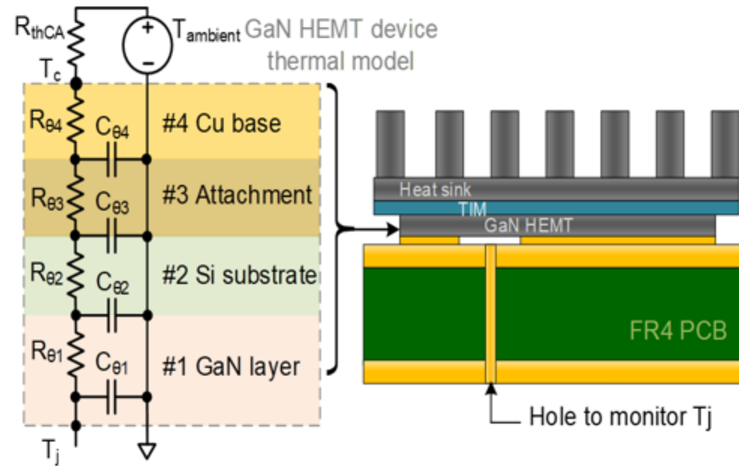


Figure 3.3: GaN HEMT device thermal model.

top-cooled GaN device is applied, the GaN layer of the device is relatively close to the PCB, as shown in Fig. 3.3. Therefore, the monitored temperature through the via can be considered as the junction temperature. In this test, the temperature on the active switch is monitored. The thermal resistance of the device has been measured on the PCB, the overall junction-to-ambient thermal resistance is 5 °C/W. By knowing the thermal resistance of the switch device, the overall loss can be calculated. At last, the junction temperature and the power loss on the active switch are compared, as shown in Fig. 3.4. It is clear that under heavy load, the simulation results are slightly larger than the measurement results. This can be explained by the fact that the measured temperature should be slightly lower than the real junction temperature, as it is measured outside the package.

As a short summary, the PLECS-based device model is relatively accurate which could help engineers and researchers on the converter-level simulation. It can be a helpful tool for users to select the most suitable switch device and also to determine the number of paralleled devices for their specific GaN-based power converter designs.

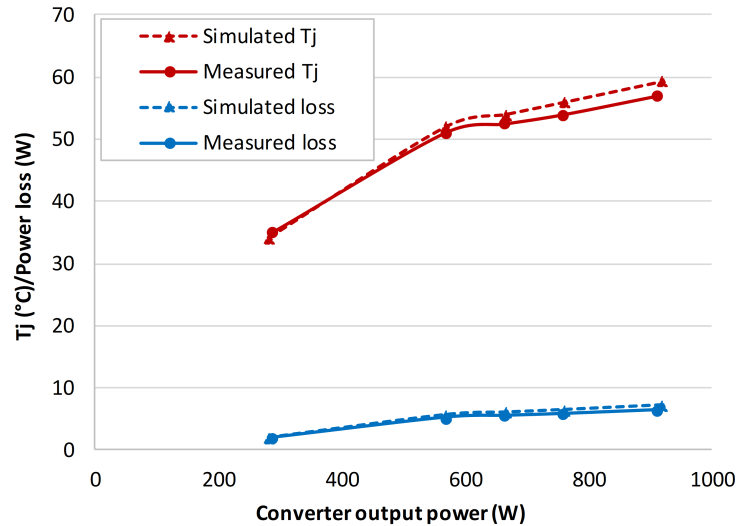


Figure 3.4: Comparison of simulation and measurement results on a GaN-based buck converter [52].

3.3 Loss Measurement Techniques

Experimental testing is usually paired with theoretic analysis of losses to validate the modelling or simulation. Special care needs to be taken when extracting data from an experimental test set-up, as devices like GaN have relatively high di/dt and dv/dt while the parasitic inductance and capacitance in the circuit are very small. Intrusive probes can greatly impact measurement results by introducing large amounts of stray inductance making high-fidelity equipment necessary to sample the data.

3.3.1 Double Pulse Test (DPT)

The DPT is a relatively straight forward and easy test to perform on switching devices to accurately determine losses. The DPT is also useful at determining the R_{dson} and

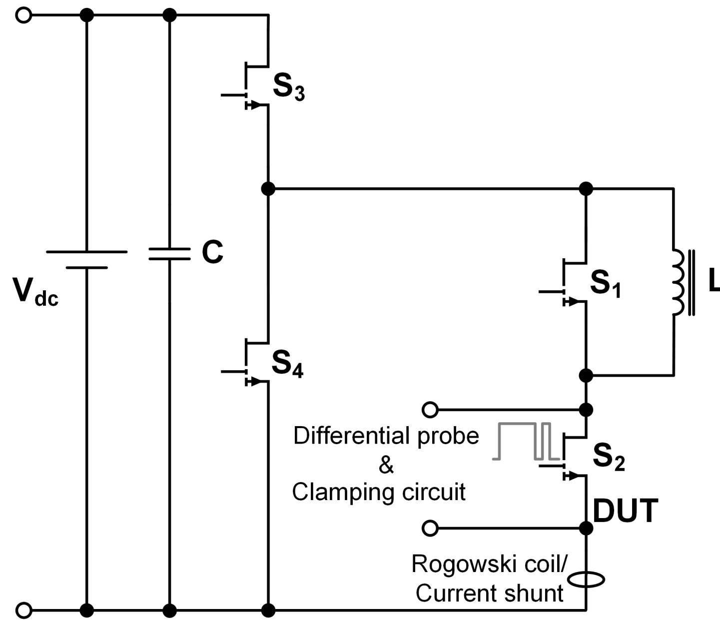


Figure 3.5: Double Pulse Test Circuit with soak time control.

can be modified with a clamping circuit for this purpose. Fig. 3.5 shows a traditional DPT circuit that has been modified to include S_3 S_4 which act as voltage soaking time control. Most literature extracts the dynamic on state resistance through a similar approach by measuring the on-state voltage and drain current of the device during test. For the on-state voltage measurement, it is possible to use equipment to take a direct measurement such as in [53]. This direct measurement technique requires relatively specific and sophisticated equipment, thus is not as popular.

When measuring R_{dson} with a DPT circuit, the on-state voltage typically requires a clamping circuit to block the off-state high voltage and therefore allows the oscilloscope to measure the on-state voltage with a large degree of accuracy. Typically, a GaN device may have voltage swings of 600 V to few millivolts when comparing the off-state voltage spike to the on-state. The V_{ds} voltage is only important during the on-state where the measurement range is relatively small. Thus, the voltage can be

clamped during the off state to allow a larger resolution during the on-state. Several clamping circuits have been proposed and developed in literature [49, 50, 54–62]. The clamping circuit topologies and their specification are summarized in Fig. 3.6 and Table 3.1.

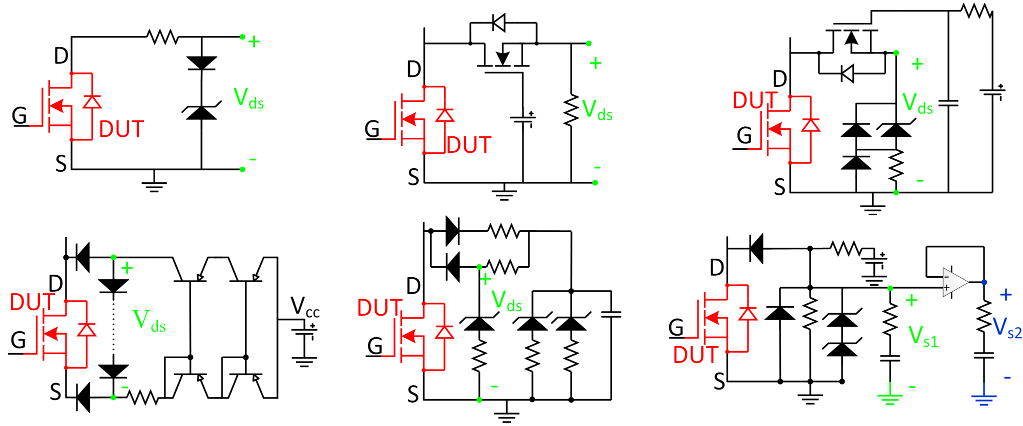


Figure 3.6: Clamping Circuits. (a) Circuit 1, (b) Circuit 2, (c) Circuit 3, (d) Circuit 4, (e) Circuit 5, (f) Circuit 6.

Table 3.1: Clamping circuits presented in literature.

	Circuit 1	Circuit 2 [61]	Circuit 3 [55, 62]	Circuit 4 [56–58]	Circuit 5 [49, 50, 54, 60]	Circuit 6
Based on	Zener Diode	MOSFET	MOSFET	Pn Diode	SiC SBD	Schottky diode
Propagation delay	>3000ns	<300ns	<100ns	<100ns	<100ns	<100ns
Clamped voltage	No limit	600V	600V	300V	600V	Limited to D_1 blocking value
External source Voltage	Passive	8V	8V	5V	Self-feeding	V_{cc} Op-Amp power
V_{dson} Measurement	Ground	Ground	Ground	Differential	Ground	Ground
Voltage offset	Subtracted	Subtracted	Subtracted	not introduced	Subtracted	Subtracted

Circuits 1 and 2 are very basic clamping circuits and not suitable for the application of measuring fast transients, they have only been included for completeness. Circuit 3 is a combination of Circuits 1 and 2 utilizing both a switching device and a diode. The diode is used to clamp the voltage to reduce spikes that result from

switching transients. More recently, another circuit similar to circuit 3 has been presented in [55]. This proposed circuit also requires a FET and clamping diodes but differs from circuit 3 due to the FET being a GaN and it is actively controlled. These small modifications result in much greater complexity but offer more control and performance improvement. The resistance measurement is stable with less than 50 ns settling time under various conditions.

Circuit 4 is the current mirror circuit. It is unique in that it does not require any adjustment to the measured voltage based on the diode forward voltage drop which is required in other clamping circuits. The design of the current mirror is presented in detail in [56]. It should be noted that due to the presence of common mode noise a differential probe is required. The current mirror is also used and compared with the SiC clamping circuit (circuit 5) in [57]. The results show that even with a differential probe, there remains some common mode noise in the measurement which skews the results. In [58] the current mirror is used as the clamping circuit, the tests are performed on Cascode devices which exhibit significantly less R_{dson}. However, the authors present the measured clamped drain-source voltage and it is shown to have significant noise and ringing. In [59], the authors propose a new circuit that is similar to circuit 5 except that an external source and filter are included for better performance. Overall the circuit in [59] looks to provide a good solution to clamping with a low settling time <100 ns. One uncertainty of this circuit is that the authors don't clearly define the benefits of the proposed circuit over the simpler circuit 5, which does not include any additional sources or filter circuits making the design and implementation much easier.

When characterizing dynamic R_{dson}, the most important time period is immediately after the device is switched on. Therefore, a faster settling time will enable an accurate measurement. The settling time is related to the capacitance of the diodes used in the clamping circuit which is the reason that low-voltage Schottky diodes and high-voltage SiC diodes are applied. As can be seen from Table 3.1, most experiments favour a circuit based on the SiC diode which is introduced in [54]. Circuit 5 and the updated Circuit 3 proposed in [55] are the most robust options.

When trying to determine the R_{dson} profile for a device, two different test setups can be performed. The first is the DPT and the second is a continuous test. The DPT is widely applied for switching loss analysis and is suitable to see the impact of switching state transitions on R_{dson}. However, some researchers have noticed an accumulation of charge trapping which further increases the R_{dson} in subsequent switching events. Thus, it becomes necessary to use a continuous test. Continuous tests best represent the device used in a power electronic system because they more accurately represent real applications and would provide the most accurate loss analysis. One issue with the continuous test is that the increased R_{dson} contains both the heating effect and trapping effect. This issue can be overcome using the DPT to first separate out the heating effect. The heating effect is not an issue for the DPT due to the time frame the test is run in. In [60], the authors separate the temperature effect by measuring the switching losses in the DPT and using these losses in a continuous DC test without switching. Thus, the change in resistance that would be caused by the same power loss can be quantified and then this can be contrasted with the continuous switching test to see how the resistance is affected.

Soft and hard switching have been investigated in several papers to see what effect

they play in the role of R_{dson}. [49] proposes a circuit that can be switched between soft and hard switching modulatio,. they also perform the DPT and multiple pulse test. The tests are performed on several devices from different GaN manufacturers, one of the devices is from Panasonic and has an additional p-n junction. The results show that soft switching reduces the R_{dson} except in the device with the additional p-n junction. A similar experiment is conducted in [62], where the tests show similar results. Soft switching reduces the level of R_{dson} with the conclusion that additional trapping is taking place during hard switching. One criticism of the tests performed is the lack of consideration for the heating effect which will be different for hard and soft switching because of the different loss levels. The heating effect was assumed to be negligible during multi-pulse test with the underlying assumption being that the duration is small enough that heating would not take place. Contrary to this, research in [60] shows that even a very small amount of heating can create a noticeable temperature rise in a double pulse test. The inclusion of a DC test similar to [60] that gives the baseline for temperature rise would provide more conclusive evidence to the comparison between soft-switching and hard-switching.

When considering the test setups for measuring R_{dson}, one important distinction is the blocking time. This is the time the switch is in the off-state while the operating high-voltage is applied on it. Typically, this is not accounted for and can drastically affect test results. Some tests have accommodated for the blocking time and created test set-ups that can vary this stress applied to the switch during the off-state through the use of additional power switches. [50] illustrates this phenomenon by showing that the longer the device is blocking, the higher the measured R_{dson}.

Modelling R_{dson} poses a challenge as can be seen from the various works presented.

The exact dynamics are heavily influenced by the manufacturing of the device and related to material defects. Thus, researchers who have attempted to model R_{dson} have first performed tests and measured the R_{dson}. In [61] researchers attempt to model the effects of R_{dson} through the use of 7 RC networks for a total of 28 parameters. However, the author reports the accuracy to be between 17% different from the actual value. Another paper is presented by the same author and presents similar data and claims the model results in an average difference of 6% and a maximal difference of 23% [63]. However, the model is taking into account very large de-trapping times which are not practical. Most converters using GaN will be operating at high frequencies so modelling the resistance after de-trapping time that is on the scale of 1ms is not useful in real applications.

3.3.2 VI Alignment

VI alignment is important when determining losses as the E_{on}/E_{off} is determined by the overlapping area between the current and voltage. By shifting these signals, the overlapping area and thus the measured loss will change. Properly aligning the probes can greatly impact the measurement as even a small delay can have a large negative impact on the measured losses [64]. Fig. 3.7 shows how the current and voltage can be aligned to acquire the loss measurement. Typically, during the switching-on transient, the di/dt and the stray inductance will cause a voltage drop on the V_{ds}. Therefore, the beginning and end of the di/dt shall be aligned with the V_{ds} voltage drop. There are three methods to de-skewing probes discussed in [64]:

- Use of calibration fixture
- Probe compensation output of scope

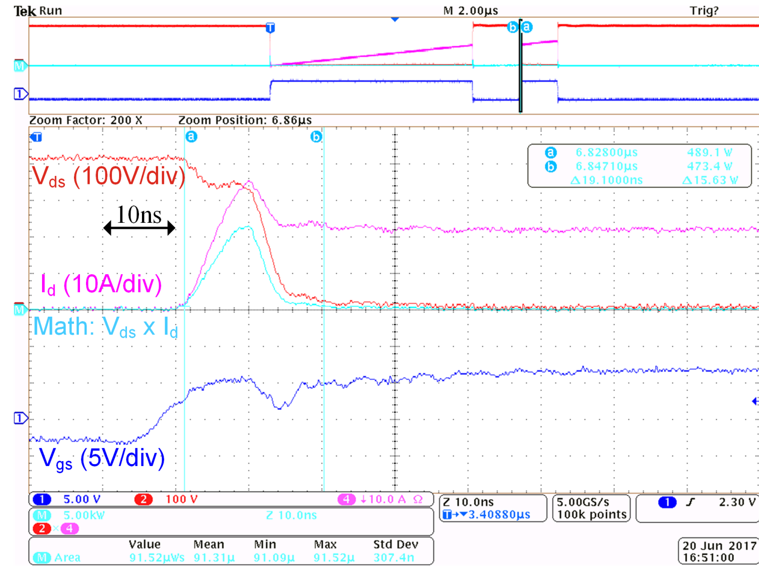


Figure 3.7: VI alignment - Eon (teal), Id (magenta), Vds (red), Vgs (blue).

- Using a resistive load

The steps for using the Tektronix calibration fixture can be found in [65]. The main drawback of this fixture is the requirement of the calibration fixture and the probe compatibility. This method is only compatible with Tektronix probes which are unsuitable for measuring high frequency transients of WBG devices due to their comparatively lower bandwidths (around 100 MHz) and unwanted added impedance.

Probe de-skewing can be done without the fixture used in the first method. Utilizing the square wave method, two probes can be connected to the probe compensation output of the scope. Each probe can be used to measure the same square wave, and then be adjusted using the de-skew option such that they are aligned. For this method one probe is selected as the baseline and all other probes will be aligned with the chosen probe. This method is much more desirable as it does not have probe requirements or additional hardware [66].

The third method is suggested by Cree for their SiC double pulse tester. This

method involves removing the freewheeling diode and replacing it with a low inductance 100-ohm resistor. The load inductor is also removed. This method will allow the current and voltage probes to be aligned because the load is entirely resistive, resulting in zero phase shift between the signals. In practice, there will exist a small delay due to tiny parasitics, but this delay should be negligible due to the total amount of impedance it contributes compared to the 100 Ω load [67].

3.3.3 Current/Voltage Probe Selection

When selecting voltage probes, designers have an option of passive or differential probes. Passive probes have much higher bandwidth and dynamic range when compared with differential probes, but they suffer from capacitive loading of the circuit at high frequencies which makes them undesirable when measuring the fast transitions of GaN [68]. The capacitive load of the probes reduces the rise time of other signal points in the system.

When selecting a current probe there are several popular options: coaxial shunt, split core probe current transformer, and Rogowski coil. Rogowski coil has the lowest bandwidth, making it unsuitable for DPT. It is reported in [69] that a Rogowski coil and amplifier is sufficient for measuring the current of GaN. However, this is not what is reported by [64]. Among the three methods, the coaxial shunt has the highest bandwidth and provides the best accuracy. As with small die GaN devices, the small stray inductance from the probe could be a large portion of the total stray inductance in the power loop, thus making any measurements non-indicative of the actual switch performance.

3.3.4 Probe Grounding

When utilizing measurement devices there are two more main concerns: probe lead inductance and common mode noise. Lead inductance results from using a long wire lead for the ground clip. This inductance is problematic, as it forms a resonant network with the input capacitance and can drastically alter measurements at high frequencies. The ideal solution is to use a spring clip for the probe tip, the total loop length for the spring clip is much smaller when compared to the traditional alligator clip. However, active probes are immune to the introduction of lead inductance.

Common mode chokes can be employed to reduce the common mode noise that is capacitively coupled through the earth ground due to the copper foil layer of the power supply transformer. This noise can make measurements difficult but can be reduced via a common mode choke, which is a transformer connected between the positive and negative of the power supply. The common mode choke works by cancelling flux of differential signals which are desired in this configuration and the flux is added for any common mode signals. When the flux adds, it creates impedance that reduces the common mode current.

3.3.5 Opposition Method

The opposition method is a technique for determining losses in a converter. An in-depth explanation of the method as well as examples are presented in [70]. The opposition method requires two identical converters that can operate in the reverse direction. The converters are connected in such a fashion that there is no resistive load, with the power circulating between the two converters as in Fig. 3.8. This setup is useful for testing the power losses at full load and offers more accuracy than

using a power analyser for the input and output. However, it may not be feasible as it requires two identical converters. An alternative is to use a different converter, provided it is compatible rating wise and its losses are already known.

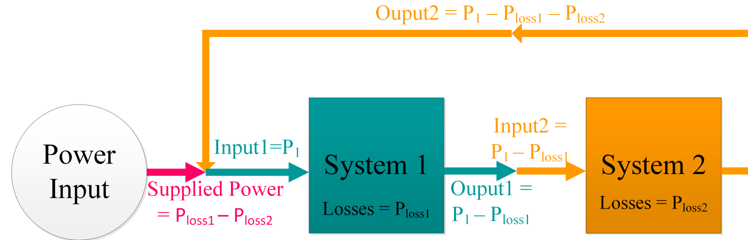


Figure 3.8: Opposition method

In [71], authors propose using the opposition method to non-intrusively measure the switching losses from GaN devices. This method makes use of two GaN half bridges with a load inductor connected between their switching nodes. The researchers apply the opposition method as it is described in [70] but vary the converter parameters to isolate various losses. Frequency-dependent losses can be identified by varying the switching frequency, while the turn on losses can be removed from the system with a purely AC current through the inductor. One important note is that the inductor losses are minimized during this test. To achieve this minimization, the researchers used two different inductors for the various tests such that they could minimize the conduction losses for one test and AC for another. This test looks promising for measuring GaN losses and provides significant advantages over the double pulse test in terms of being non-intrusive. Another advantage of this method is that state of the art probes are not required to measure fast transitions. The disadvantage of this test is the requirement of two inductors for minimizing losses in addition to temperature being an uncontrolled variable.

3.3.6 Calormetric

One method to determine losses is to use a calorimeter to measure the total change in heat of the system via the air temperature. Typically, traditional calorimeters require several hours to reach thermal balance, which is not practical. The proposed method in [72] utilizes the converter itself as the calorimetric chamber which can reach thermal equilibrium more quickly. This is because the converter has a lower thermal capacitance compared to a calorimetric chamber. One drawback of this method is the inability to separate out the individual losses. The authors also cite that the method cannot measure the losses in the passive components, but for the consideration of GaN losses this is irrelevant. However, similar to the opposition method presented in section 3.3.5, it may be possible to separate out losses with multiple tests by varying the switching frequency and load type.

3.3.7 Water Flow Exchanger

Similar to the calorimetric approach, this method is concerned with the change in temperature to determine the losses. The inlet temperature is compared against the outlet temperature to determine how much heat was injected into the coolant path. This method is applied in [73] in conjunction with the opposition method to determine the exact contributions of the loss. It should be noted that at low power the temperature difference may be extremely small, thus this method is largely suited to higher power testing.

3.4 Summary

Loss modelling for GaN power devices has been presented and loss measurement techniques were summarized. GaN is a promising technology, with very low switching and conduction losses. However, there are uncertainties existing on some factors contributing to a small portion of losses, such as the dynamic R_{dson}. Currently modelling this behaviour is difficult due to variation existing between different devices. Measurement equipment also needs some improvements as the bandwidth, stray capacitance and inductance introduce significant errors when performing a standard test, such as the DPT. However, because much of these uncertainties contribute to only a small amount of the total loss they can mostly be neglected for prototyping and simulations. The scaling approach method discussed in Section 3.1.2 is selected because of its ease of use and accuracy. The data from the manufacturers data sheets are from real DPT and can easily be scaled down to other operating conditions providing an accurate estimation for modelling GaN switching losses.

Chapter 4

Dual-Active Bridge (DAB) Converters

4.1 Converters for Isolated BESS

The rechargeable batteries used in the BESS require bi-directional power flow for charging and discharging the battery. In addition, galvanic isolation is needed for safety to protect the consumers from shock but also to provide voltage matching. Fig. 4.1 shows a typical system involving a BESS and accompanying power electronics. Typical converters used in these systems fall under two classifications; cascaded two-stage converters or single-stage converters. Both types make use of high frequency transformers as these allow for compact converter design compared with the line-frequency alternative. Two-stage cascaded converters are most commonly a modular design composed of a Dual-active bridge connected to a downstream inverter, the design is robust as it allows the designer to fine tune each stage of the converter based on the input battery and the required load. However, the control can be more

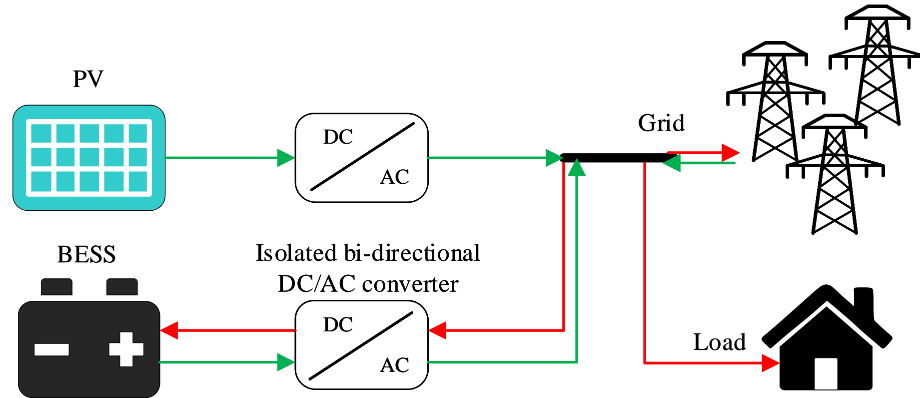


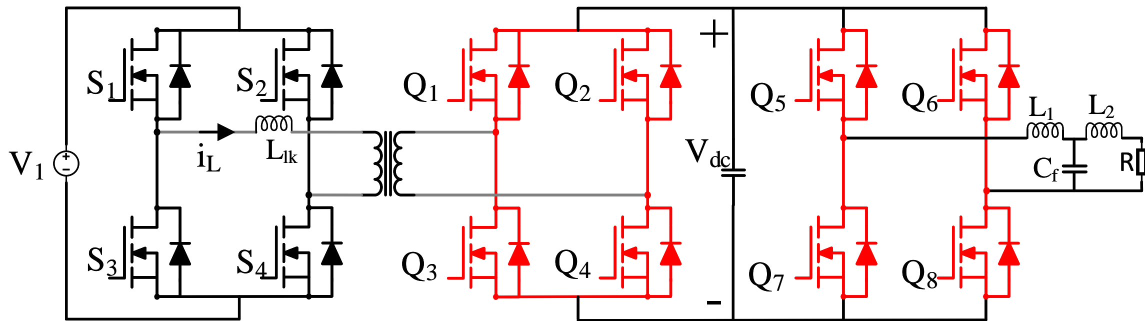
Figure 4.1: Isolated bi-directional DC/AC converters interfacing BESS with PV, grid and load.

complicated because there needs to be closed loop control for the intermediate DC bus and the output. In addition, the intermediate DC bus requires special attention due to the second harmonic current (SHC) which reduces efficiency [74, 75]. The single-stage approach is a hybrid design of the DAB and cycloconverter, it does not have the intermediate DC bus of the two-stage approach and the control system is for a single converter [76]. Fig. 4.2 shows the block diagram for both converter topologies.

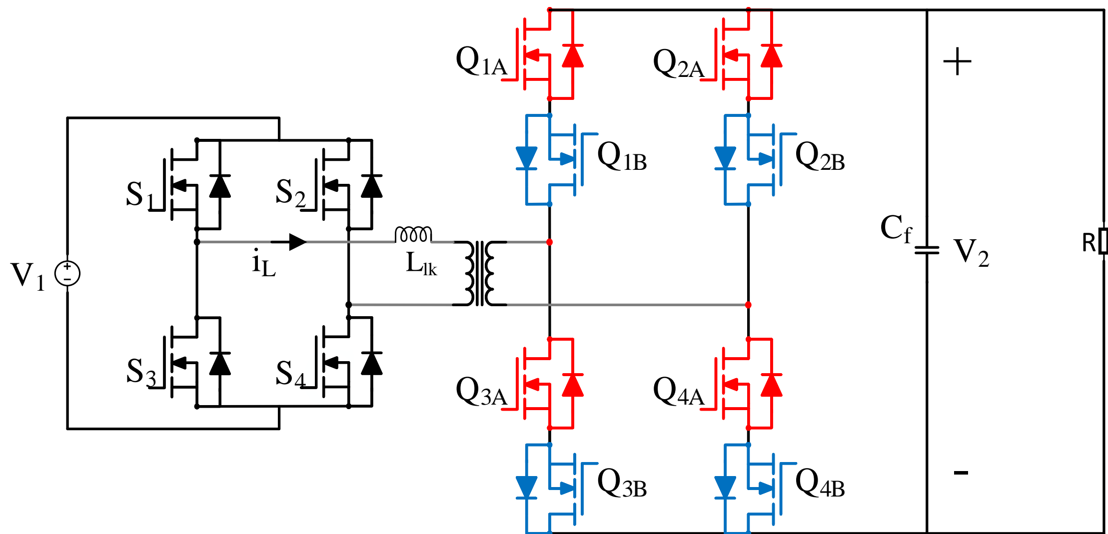
4.1.1 Two-Stage Cascaded Converters

As previously mentioned, the two stage approach offers a lot of flexibility to the designer. The two stage approach can be broken down into its key components of:

- Input source
- LV converter
- HV converter



(a)



(b)

Figure 4.2: Isolated DC/AC converters (a) Two stage cascaded DAB and Inverter with LCL filter (b) single stage cyclocomverter type DAB.

- High frequency transformer
- Intermediate DC link
- Inverter

Based off of Fig. 4.2 the input source is a DC battery or cell, the LV and HV converters

are most often full-bridges(FB), the high frequency transformer can be a traditional style or planar transformer, the intermediate DC link is usually a large electrolytic capacitor bank. Typical applications include: fuel cell power conditioning, BESS and EV chargers [77–81]. There are several areas of this converter that draw much research attention. Many researchers focus on the power decoupling in an attempt to reduce the size of the capacitors forming the intermediate DC bus which are often the Achilles heel of the converters lifetime. Another area of focus is the LCL filter and control relating to this as the output harmonics and performance of the inverter depend on this filter design.

4.1.1.1 Inverter LCL Filter

The design of the LCL filter is very straightforward and takes into account many parameters based on the application. Several of the design considerations are listed below [82]:

- The converter side inductor (L_1) is determined by the allowable current ripple, this value typically is 10% - 40% and is chosen based on the saturation value of the inductor
- The grid side inductor (L_2) has to attenuate the unwanted harmonics defined by *IEEE 519 – 2014* guidelines. Harmonics above the 35th should be attenuated to 0.3%
- The total inductance ($L_1 + L_2$) cannot cause a significant voltage drop on the system, ideally a voltage drop less than 10%.
- The capacitor value (C_f) is chosen to be less than 5% of the base value due to

the power factor variation of the grid [83].

- The resonant frequency of the filter (f_r) should be 10 times larger than the line frequency but smaller than half of the switching frequency.

4.1.2 Double Line Frequency Ripple

Battery driven isolated DC/AC converters experience a phenomenon known as the double line frequency ripple where the current pulsates at twice the output frequency. This phenomenon is caused by the changing instantaneous power demand which also pulsates at twice the line frequency and is shown in Fig. 4.3. Many researchers spend a lot of focus on this particular aspect of DC/AC converters in an attempt to decouple the ripple power. The main reasons for this are: battery health, efficiency

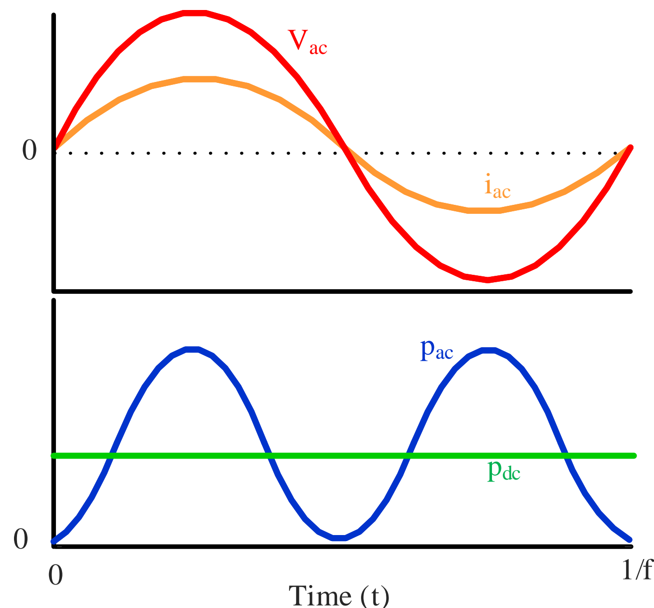


Figure 4.3: pulsating output power resulting in double line frequency ripple.

and reliability. Pulsating power can result in larger peak currents in the switching devices, leading to higher conduction and switching losses. In addition to this, many researchers believe that the battery supplying and absorbing the low frequency ripple current is damaging to its health. Currently in literature there are many approaches to address these concerns, such as adding a bi-directional buck/boost active ripple filter in parallel with the DC/DC converter. This type of solution adds a reactive network to provide the sinusoidal ripple current to prevent it from going into the battery. However, this adds switching and passive components which add to the overall size [84–86]. Another method involves trying to utilize switching devices already present in the circuit by adding a passive half-bridge phase-leg, this method attempts to steer ripple power into the passive devices [80]. One flaw of these methods is that the power decoupling is not independent of the power conversion stage and thus can negatively impact the performance [87]. Finally, in order to prevent increasing the size of the converter with additional switching or passive components, a control only method can be used. Control only methods usually focus on specific topologies and often are best suited for non-isolated applications where the DC/DC converter has more flexibility to control the ripple [88]. Overall, these strategies are focused on reducing the ripple current that must be filtered by the intermediate DC-link capacitor which enables a large reduction in size. Most research on this topic does not clearly establish the need for such added complexity and cost, unless the application is for a fuel cell which exhibits different properties than a battery due to its hysteresis behaviour which can cause thermal problems [89].

4.1.2.1 Battery Health

Battery performance degrades over time due to age and cycling the battery regardless of the C-rate [90]. Pulse charging has been the subject of much research as a way to provide a rest or 'relaxation' period for the battery so that the charging is more efficient. In general, there appears to be controversial opinions on whether or not the pulse charging is beneficial. In [91] lithium ion batteries are investigated using various pulsed charging techniques and it was concluded that the effect is overall negative, the evidence showed that a larger form factor defined as RMS/Mean current negatively impacted the battery capacity. In [92] the short term effect of low frequency ripple on the temperature of battery cells is investigated and it shows that 120 Hz current with the peak value being 200% of the DC component does not significantly alter the temperature compared with DC current. The additional losses are a result of the frequency dependant non-linear impedance but minimal increase to temperature should be tolerable in longer term tests. In [93] low frequency sinusoidal waveform pulse charging is used to charge a lithium iron phosphate battery, the long term effects this would have on the battery capacity are studied as it undergoes 2000 charge discharge cycles. Overall the degradation in capacity is similar to DC charging, the capacity degradation was reported to be 16.3% and 15.1% for pulse and DC, respectively. This difference is overall negligible and is expected due to the slightly higher temperature the battery should be operating at due to the ripple. Another paper looks at the long term impacts of battery health in an electric vehicle application and analyses several frequencies of interest from a real world application. Cells are chosen to be similar to each other and then each frequency is performed on 3 cells and the capacities are recorded every 300 cycles. The researchers conclude that the

AC ripples lead to increased capacity fade despite the surface temperature being maintained to 25°C, it is suggested that the internal temperature gradients could still vary from the DC case resulting in ageing mechanisms. The data presented for the low frequency cases does not drastically differ from the DC case especially around 254 Hz [94]. Similarly in [95], two lithium cells from a battery are cycled, one with DC and the other with 120 Hz (double line frequency) AC current. After 250 cycles the reduction in capacity is near identical with only a 0.55% difference between them. The mechanisms for why the super imposed AC waveforms lead to greater battery degradation are explained in detail in [96], in short the larger frequencies result in higher power throughput of the battery causing internal temperatures to increase which lead to accelerated growth of the solid electrolyte (SEI) film. In [96], multiple cells are cycled 1200 times with various frequencies, the frequencies selected are based on the braking event in a battery electric vehicle (BEV). The analysis shows that the capacity fade and power fade are largest for frequency components in the 14.8 kHz region, the capacity fade for 55 Hz and 254 Hz is much lower. This suggests that the double line frequency ripple of 100 − 120 Hz would increase any battery degradation by a negligible margin. In contrast to some of the previous research and results is the work of [97] which investigates both low and high frequency ripple on two different batteries, it is concluded that the low frequency ripple $<$ 10 Hz appears to have the largest impact on battery capacity fade relating to the time constants of the electrochemical processes. Some research even suggests control schemes for sinusoidal battery current in two stage approaches. By allowing the double frequency ripple current to flow into the battery, the ripple current present on the intermediate DC link is reduced which results in lower capacitance requirement [98].

4.1.2.2 Power Decoupling

The DC link capacitor is usually a large aluminium electrolytic capacitor to absorb the low frequency ripple of the output power. However, electrolytic capacitors are known for their poor lifetime and result in reduced reliability when compared with a film capacitor [99, 100]. Many strategies attempt to tackle the issue of the double line frequency power ripple, power decoupling is one such technique which tries to remove the ripple power from the DC link thus resulting in the ability to use a film capacitor which greatly improves the converter lifetime. Power decoupling is achieved through various techniques encompassing control algorithms and additional circuit components [87]. Power decoupling can be achieved with a ripple network that will consume and supply the reactive power. While this method is successful at eliminating the pulsating power on the DC link, it results in the addition of large passive devices elsewhere in the circuit. The required rating of the added passive devices quickly becomes unfeasible for operating as high power because they need to filter low frequencies while handling large amounts of current [80]. Control solutions offer much better performance as they do not add additional hardware components and instead rely only on control to reduce the ripple, one such example is in a two-stage cascaded buck converter-inverter design which uses a PR controller to control inductor currents which limits the double line frequency ripple [101].

4.1.3 Single-Stage Cascaded Converters

The two-stage combination of the DAB and inverter has proven to be a popular choice for the isolated DC/AC conversion. However, the need to include an intermediate DC bus increases the size, and the rectification stage decreases the efficiency. One

solution to this problem is to remove the DC bus and to modulate the transformer AC voltage to meet the desired standards. The idea of such a converter is built upon the cycloconverter, which is an AC/AC converter. In order to block AC voltages, two conventional switches such as MOSFETs are connected with their sources tied together to create an AC switch. The cycloconverter is designed to directly convert an AC input of a particular frequency and transform it into a different frequency without any intermediate DC bus [102, 103]. Currently, many of the single-stage converters in literature make use of very large passive components due to the need to filter out harmonics as a result of the control [104].

4.1.4 Cycloconverter

The analysis of cycloconverter-type high frequency link DAB (CHFL-DAB) often treats the cycloconverter stage as a positive converter and negative converter superimposed upon one another. For example, the converters presented in [105, 106] are a combination of a single-phase FB connected to a three-phase cycloconverter. The generation of the output is based on decoupling the high-frequency transformer output as two DC pulses with inverse polarity. In [107], a resonant tank replaces the leakage inductance to reduce the adverse effects of the voltage stress on the switches. Often, cycloconverters use an integrated control scheme which involves a single gate signal for both switches that make up the AC switch. In [108, 109], the two devices forming the AC switch receive their own unique (non-integrated control) pulse width modulation (PWM) signal. This enables the reduction of switching losses when compared with integrated control due to fewer active switches during each switching cycle [110, 111]. Another promising work presents an AC/DC converter for a battery

charger using a half-bridge composed of AC switches connected to a FB through an HFL transformer. The control strategy is based upon the DAB phase shift and frequency modulation. The optimal control variables are found by minimizing the peak current and are stored in a LUT such that the voltage, current, and mains angle can be used to determine which operating condition is most efficient [112, 113].

The fundamental idea behind the hardware topology is the use of interleaved DAB converters to create an AC output. Although the use of interleaved DAB converters was presented in [105], the control scheme proposed in this thesis will focus on duty modulation instead of frequency modulation with a simpler solution to generate the optimal control variables. The operational principle of the DAB converter in Fig. 4.2-a will be the same Fig. 4.2-b during one half cycle, while the operation during the next half-cycle is the same as the DAB with its polarity reversed. A positive output requires $Q_{1A} - Q_{4A}$ to operate as a DAB with $Q_{1B} - Q_{4B}$ turned on, the negative output can be produced with the operation of $Q_{1B} - Q_{4B}$ as a DAB with $Q_{1A} - Q_{4A}$ turned on.

4.2 DAB

As outlined in Section. 4.1.1 and Section. 4.1.3 the The DAB converter is integral for many isolated DC/DC converters due to its relatively simple analysis and its high efficiency with a low number of devices. Other options include: converters with fewer switching devices (flybuck, push pull network), or converters with resonant networks like the Resonant LLC converter. When considering the device stress, number of components and efficiency the DAB has good performance in all of these categories compared to the previously mentioned alternatives [114]. The LLC converter is very

similar to the DAB but it introduces additional passive components to form a resonant network in an attempt to reduce switching losses with ZVS and zero current switching (ZCS) [81].

The DAB has many options for control, this allows the designer a lot of flexibility for achieving high efficiency. Three parameters can be controlled to modulate the output voltage:

- Phase Shift
- Duty Cycle
- Switching Frequency

Typically one of these will be used or combined with others depending on the application. Single phase shift modulation (SPS) is very common and the most basic as it only requires the analysis and modification of a single parameter [115, 116]. The analysis of SPS is quite simple and it will lead into more advanced schemes. Using just phase shift control, the other two parameters are assumed to be fixed. The frequency can be set to whatever value is needed for the application and both bridges will be operating at the maximum duty cycle of 0.5. This gives four possible operating conditions for the voltage across the inductor: (V_1, $-V_2$), (V_1, V_2), ($-V_1$, V_2), ($-V_1$, $-V_2$). Because of the need for volt-second balance, the average inductor current will be zero during steady state operation. Due to this symmetry, only the half cycle needs to be considered for all future calculations. Since the analysis is based on the lossless DAB the transferred power $P_{transfer}$ will be equivalent to the output power defined by,

$$P_{transfer} = \frac{{V_2}^2}{R} \tag{4.1}$$

where V_2 is the output DC link voltage and R_{load} is the load resistance. Based on the assumption that the converter has zero power loss, the equivalent model for a lossless DAB is presented in Fig. 4.4. The input voltage is V_{1ac} and the input current is i_L, then the instantaneous power transferred $P_{transfer}(t)$ is define.

$$P_{transfer} = V_{1ac}(t) i_L(t) \tag{4.2}$$

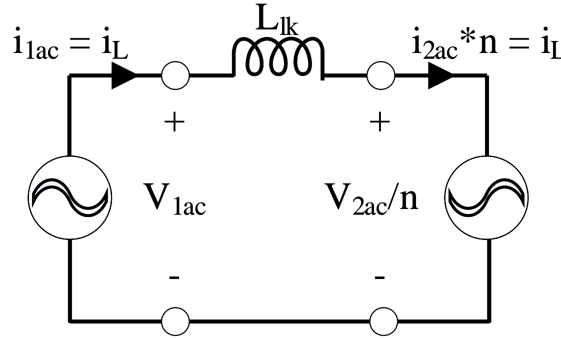


Figure 4.4: DAB lossless Model

The output voltage and power will be constant DC values. This power can be seen as equivocal to the average power of the transformer transmission power. In order to properly solve (4.1), the average value of (4.2) needs to be solved. Due to the volt-second balance, the average i_L during one switching cycle is zero. Thus, in order to calculate the average of (4.2) i_L must be integrated for a half-cycle. Because of the symmetry needed to achieve volt-second balance, the current at the start of the switching cycle will have the same magnitude as the current halfway through the cycle which is expressed in (4.3),

$$i_L(t) = -i_L(t - \frac{T_s}{2}) \tag{4.3}$$

where $i_L(t)$ is the inductor current at any given time interval 't' and T_s is the switching period. Thus, the integral of (4.2) over a half cycle can be represented as,

$$P_{transfer} = \frac{2}{T_s}\int_0^{\frac{T_s}{2}} V_{1ac}(t)i_L(t)dt \tag{4.4}$$

where V_{1ac} is the voltage appearing before the leakage inductor as seen in Fig. 4.4. V_{1ac} is directly related to the DC voltage and the applied gate signals, this fact is used to further simplify (4.4). Thus, V_{1ac} will be equal to V_1 (S_1 and S_4 on) or $-V_1$ (S_2 and S_3 on). This will allow the integral in (4.4) to be separated into two integrals with a constant V_{1ac}. The two different segments for $i_L(t)$ during a half cycle shown in Fig. 4.5 are defined by the constant voltages that appear across the inductor during these time periods. The equation for voltage across an inductor can be used to define $i_L(t)$.

$$V_L = V_{1ac} - V_{2ac} \tag{4.5a}$$

$$V_L = L_{lk}\frac{di}{dt} \tag{4.5b}$$

V_L is the voltage across the leakage inductance and V_{1ac} and V_{2ac} can be considered constants equal to their respective DC buses. Since each interval in Fig. 4.5 corresponds to a constant V_1 and V_2, the resulting i_L will be linear during this time period. di can be defined as the difference between the current at the start of the interval and any point located within that interval while dt is the difference between the starting time of the interval and the desired time t. Thus, assuming the start of the interval is at $t = 0$, and the phase shift between bridges is positive then the

equation for the current is determined.

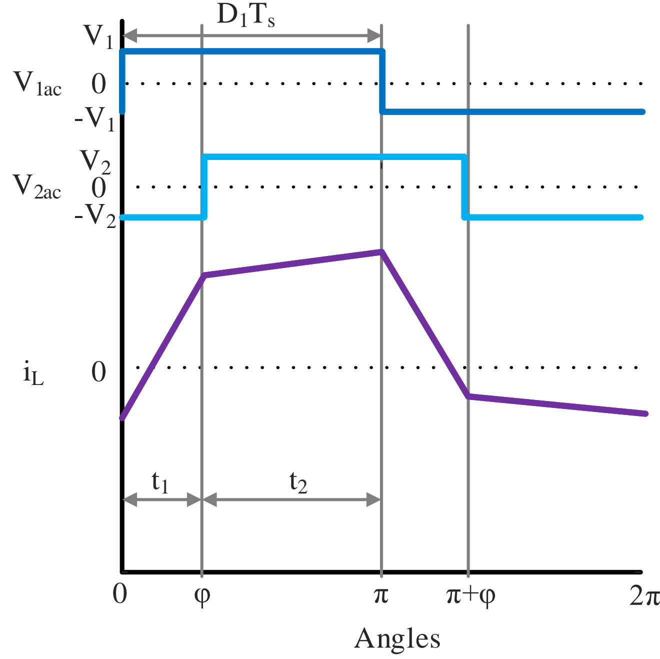


Figure 4.5: Ideal voltage and current waveforms using SPS.

$$i_L(t) = \begin{cases} \dfrac{V_1 + nV_2}{L} t + i_L(0) & 0 < t < t_1 \quad (4.6a) \\ \dfrac{V_1 - nV_2}{L} (t - t_1) + i_L(t_1) & t_1 < t < t_2 \quad (4.6b) \end{cases}$$

The time periods t_1 and t_2 are defined based on the duty cycle, the phase shift and the period respectively.

$$t_1 = \frac{\phi}{2\pi f_s} \tag{4.7a}$$

$$t_2 = \frac{T_s}{2} \tag{4.7b}$$

$i_L(0)$ is the initial current at the start of the interval and L_{lk} is the leakage inductance.

$i_L(0)$ can be solved by using (4.3) and (4.6),

$$i_L(0) = \frac{nV_2\pi - 2V_2\phi - nV_1\pi}{4n\pi L_{lk} f_s} \tag{4.8}$$

where ϕ is the phase shift between the two bridges as seen in Fig. 4.5. Each interval in (4.6) has a constant V_{1ac}, this allows the expression of the integral in (4.4) as the sum of the integrals over each interval defined in (4.11). V_{1ac} will equal to V_1 for (4.6a) and (4.6b), this allows the equation for output power P_o to be defined.

$$P_o = \frac{V_1 V_2(\pi\phi - \phi^2)}{2\pi^2 L_{lk} f_s} \tag{4.9}$$

From (4.9) it can be seen that the power depends entirely on the phase shift once all the other parameters are selected. The single control variable of SPS results in a low complexity system that is easy to implement. However, SPS is lacking in terms of flexibility when operating over a large voltage range as there are a limited number of states that can provide a desired output. Depending on the conditions it will be more difficult to maintain soft switching and low transformer RMS currents.

The analysis of the DAB operation assumed both duty cycles are 50% and constant. However, if both duty cycle and phase shift are varied (DPSM), then additional control over the transformer RMS currents can be achieved. The analysis is similar to the above phase shift control except that V_{1ac} has an additional state, if D_1 is less than 50% then V_{1ac} will be equal to 0 which results in two additional operating pairs (0, V2) and (0, -V2). Because of the additional operating pairs, $i_L(t)$ has an additional 2 intervals during one cycle when compared with SPS. Like the SPS there exists half cycle symmetry due to the need of balancing the transformer current so

only the 3 intervals in the first half period need to be analysed. $i_L(t)$ is broken in 3 segments based on the voltage pulses in the first half cycle as can be seen in 4.6.

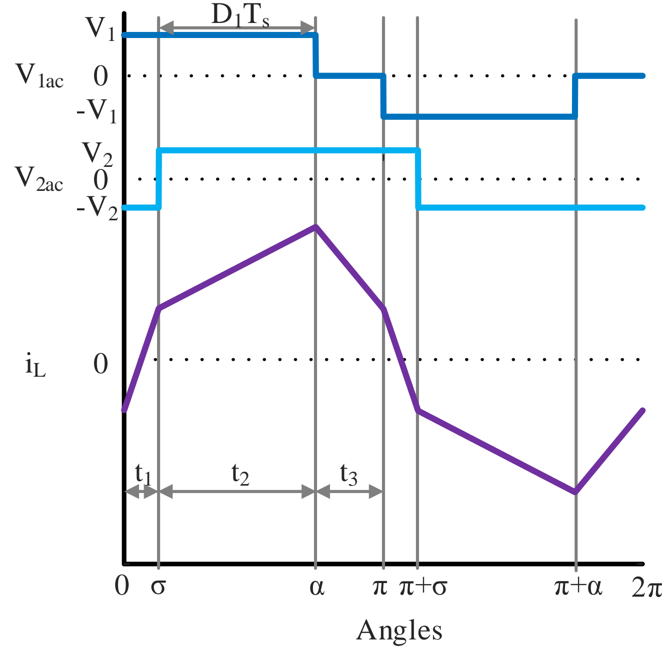


Figure 4.6: Ideal voltage and current waveforms using the DPSM.

$$i_L(t) = \begin{cases} \dfrac{V_1 + V_2}{L_{lk}} t + i_L(0) & 0 < t < t_1 \quad (4.10a) \\ \dfrac{V_1 - V_2}{L_{lk}} (t - t_1) + i_L(t_1) & t_1 < t < t_2 \quad (4.10b) \\ \dfrac{-V_2}{L_{lk}} (t - t_2) + i_L(t_2) & t_2 < t < t_3 \quad (4.10c) \end{cases}$$

The time periods t_1, t_2 and t_3 are defined based on the duty cycle, the phase shift

and the period, respectively.

$$t_1 = \frac{\sigma}{2\pi f_s} \tag{4.11a}$$

$$t_2 = \frac{\alpha}{2\pi f_s} \tag{4.11b}$$

$$t_3 = \frac{1}{2f_s} \tag{4.11c}$$

$i_L(0)$ can be solved by using (4.3) and (4.10),

$$i_L(0) = \frac{V_2\pi - 2V_2\sigma - nV_1\alpha}{4n\pi L_{lk} f_s} \tag{4.12}$$

where σ is the phase shift between the two bridges and α is the duty cycle of the primary side in radians as shown in Fig. 4.6. Each interval in (4.10) has a constant V_{1ac}, this allows the expression of the integral in (4.4) as the sum of the integrals over each interval defined in (4.11). V_{1ac} will equal to V_1 for (4.10a) and (4.10b) and it will equal zero for (4.10c). Thus, the power transferred will be equal to:

$$P_o = \frac{V_1V_2(D_1\pi^2 + 2D_1\pi\sigma - \sigma^2 - 2{D_1}^2\pi^2)}{2n\pi^2 L_{lk} f_s} \tag{4.13}$$

More importantly, (4.13) can be manipulated using (4.1) to give a relationship between the control parameters and V_2:

$$V_2 = \frac{V_1R(D_1\pi^2 + 2D_1\pi\sigma - \sigma^2 - 2{D_1}^2\pi^2}{2n\pi^2 L_{lk} f_s} \tag{4.14}$$

4.3 Summary

When designing power electronic converters for BESS, the DAB is an integral part for isolated designs. However, the two-stage approach which has long been the go to converter for isolated DC/AC applications has numerous issues which can not be solved by simply upgrading the switches. The two-stage approach requires multiple sensors and control loops in order to monitor and control the intermediate and output stages, this leads to higher cost and complexity. In addition, the intermediate bus contains poor reliability electrolytic capacitors to filter the unwanted ripple. The single-stage approach shows a lot of promise, the lack of the intermediate DC bus means the battery can directly supply and absorb the low frequency ripple without any additional components. The adverse affects on the battery due to these ripples will be minimal as the frequency is not large enough to induce any significant internal temperature increases. The next chapter will look at control for the single-stage approach and how this can offer even more advantages over the conventional two-stage approach.

Chapter 5

Cycloconverter-Type DAB Control Strategy

5.1 Control Strategy

In Chapter 4 the DAB converter was introduced as an integral part for both the single-stage and two-stage isolated DC/AC converters. Having already identified the areas of weakness for the two-stage approach and how the single-stage approach rectifies these areas, a method for determining the optimal control for the single-stage converter is presented which aims to provide even more benefits for an already promising converter topology. The equations presented will use the same notation as the previous Chapter 4 and will be describing the converter in Fig. 4.2

5.1.1 Parameter Selection

To simplify further analysis, parameter 'K' is introduced to represent the fixed parameters during operation.

$$K = \frac{V_1 R}{2n\pi^2 L_{lk} f_s} \tag{5.1}$$

Determining the minimum value for K will be imperative to the design of the converter. If K is too small, then the entire operating range cannot be realized. Thus, the maximum power conditions will be defined as the derivative of (4.13) with respect to D_1 and σ:

$$\frac{dP_o}{dD_1} = \pi^2 + 2\pi\sigma - 4D_1\pi^2 \tag{5.2a}$$

$$D_1 = \frac{\pi + 2\sigma}{4\pi} \tag{5.2b}$$

Likewise, the maximum with respect to σ is:

$$\frac{dP_o}{d\sigma} = 2D_1\pi - 2\sigma \tag{5.3a}$$

$$\sigma = D_1\pi \tag{5.3b}$$

Putting (5.2) and (5.3) together, the maximum power transfer is found to occur when D_1 is 0.5 and σ is $\pi/2$. Therefore, substituting 5.1, and the values for D_1 and σ into (4.14) the minimum value of K can be determined.

$$K_{min} = \frac{4V_2}{\pi^2} \tag{5.4}$$

5.2 Power Loss Modeling

In Section 4.2, the analysis of the converter neglected the losses. However, in order to develop a control scheme for the converter it is necessary to consider which operating conditions will give the lowest power loss. The sum of the switching and conduction loss is used to approximate the total losses, this is because the losses of the switching devices make up the majority of the losses. GaN devices have been selected for the switches $Q_{1A} - Q_{4B}$, while Si switches are used for $S_1 - S_4$ in Fig. 4.2.

$$P_{loss} = P_{1cond} + P_{2cond} + P_{1sw} + P_{2sw} \tag{5.5}$$

P_{loss} is the total loss of the converter, P_{1cond} and P_{2cond} are the conduction losses of bridges B_1 and B_2, respectively. While P_{1sw} and P_{2sw} are the switching losses of B_1 and B_2, respectively.

5.2.1 Conduction Losses

The device conduction losses can be calculated from the on-state resistance of the FET R_{dson} and the drain source current I_{ds}.

$$P_{cond} = I_{ds}^2 R_{dson} \tag{5.6}$$

For fully saturated Si devices, R_{dson} exhibits negligible change with respect to I_{ds}. R_{dson} is only impacted by the junction temperature T_j, the relationship between R_{dson} and T_j can be extracted from the manufactures datasheet and placed in a LUT. R_{dson} of a GaN FET is impacted by I_{ds} and T_j, the resulting LUT extracted from the

manufactures datasheet will contain an extra dimension compared to Si.

5.2.2 Switching Losses

Switching losses are a result of voltage and current overlap during the switching transition illustrated in Fig. 5.1.

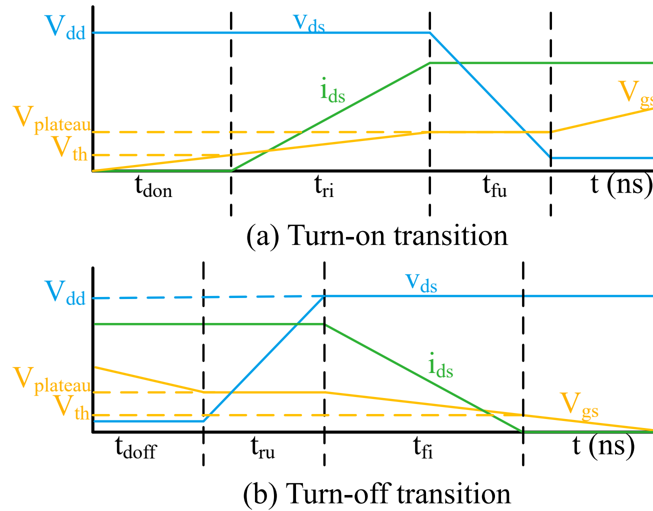


Figure 5.1: Si MOSFET voltage and current switching transition waveforms.

For Si devices, the losses can be approximated with the rise and fall times of the switching waveforms,

$$P_{sw} = \frac{I_{ds}V_{ds}}{2}(t_{ri} + t_{fu} + t_{ru} + t_{fi}) \tag{5.7}$$

where t_{ri} and t_{fi} are the current rise and fall times, respectively, t_{ru} and t_{fu} are the voltage rise and fall times respectively. The in-depth analysis and calculation of t_{ri}, t_{fu}, t_{ru} and t_{fi} are presented in [117], only the final expressions for each are

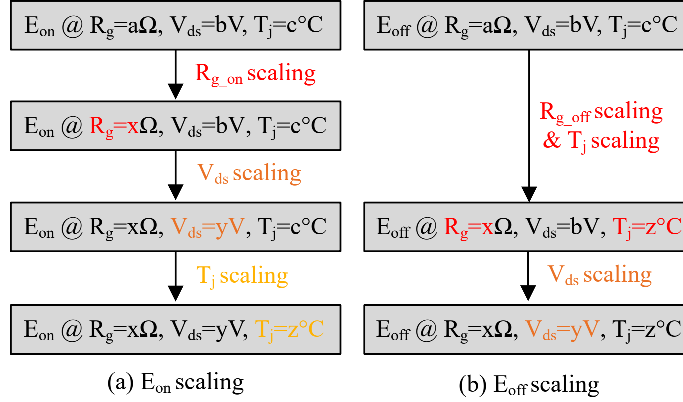


Figure 5.2: GaN HEMTs Eon/Eoff scaling procedures.

presented.

$$\begin{aligned} t_{ri} &= R_g C_{iss} ln\left(\frac{V_{gon}-V_{th}}{V_{gon}-V_{plat}}\right) \\ t_{fu} &= (V_{ds}-V_{on}) R_g C_{rss} \frac{1}{V_{gon}-V_{plat}} \\ t_{ru} &= (V_{ds}-V_{on}) R_g C_{rss} \frac{1}{V_{plat}-V_{goff}} \\ t_{fi} &= R_g C_{iss} ln\left(\frac{V_{goff}-V_{plat}}{V_{goff}-V_{th}}\right) \end{aligned} \tag{5.8}$$

R_g is the gate resistance, V_{gon} is the applied gate voltage during the on-time and V_{goff} is the applied gate voltage during the off-time. C_{iss} is the input capacitance and C_{rss} is the drain-gate capacitance, V_{th} is the gate threshold voltage and V_{plat} is the plateau voltage.

For GaN devices, the losses are calculated using a scaling approach [23, 24]. This method takes the measured E_{on} and E_{off} from a known operating condition such as those provided in the datasheet and uses a series of equations to scale that operating condition to the desired V_{ds}, T_j and R_g, Fig. 5.2 summarizes the scaling procedure found in [24].

5.3 Control

Control of the CHFL-DAB is based upon the DAB phase shift and duty cycle modulation defined in Section 4.2. Two FB converters on the output side of the transformer with inverse polarities are used in order to generate an AC waveform. Each FB is responsible for one half cycle, each half cycle is divided into discrete steps and each step is approximated as a DC voltage (Fig. 5.3). Multiple duty cycles and phase shift pairs are possible to create each DC step of Fig. 5.3.

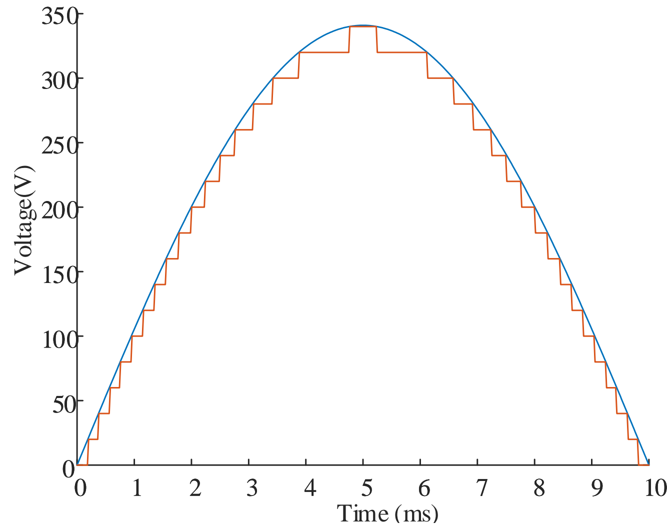
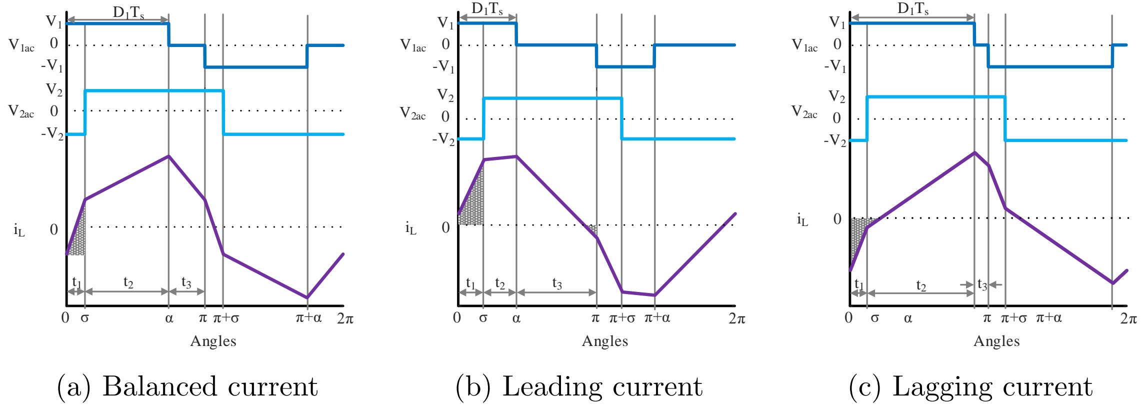


Figure 5.3: Quantized output voltage reference.

5.3.1 Minimum Back-Flow Power

Several methods exist to determine the duty and phase shift pairs for optimal control. One such method is based around minimizing the back-flow power. Back-flow power is defined as the area of overlap between i_L and either V_{1ac} or V_{2ac} when the polarities are opposite. The inductor current can have several different waveforms based on

the operating conditions, each condition produces slightly different time periods of back-flow power which is shown in Fig. 5.4.



(a) Balanced current (b) Leading current (c) Lagging current

Figure 5.4: Inductor current wave profiles showing the back-flow power.

Minimizing the back-flow power is a good way to determine suitable operating points. However, this method is computationally complex and does not result in the minimum power loss. Thus a new method for easily determining the minimum power loss is presented.

5.3.2 Minimum Power Loss For Quantized Output Voltage

The suggested control determines these two variables based on the operating conditions that lead to the minimum power loss. The use of two control variables allows greater flexibility while controlling the output power and transformer currents. On the other hand, the phase shift can be fixed to zero during low power operation to simplify the control. The direct approach of minimizing the total power loss with respect to the control variables can be computationally complex or even unfeasible as many researchers use LUTs to extract loss information from the manufacturer's datasheets. Thus, an indirect method for the optimal condition is derived based

on applying a weighted average to the individual optimum operating conditions for conduction and switching losses of both FBs.

After selecting a specific K value that is suitable for achieving the desired operating condition, it is necessary to determine the duty cycle and phase shift pairs required to achieve the voltage steps within a half-cycle. There are several possible approaches to try and achieve the optimal set of operating conditions. Directly trying to optimize the power loss or minimizing the back-flow power are two such approaches. The methods for optimizing the control are difficult, either they are computationally complex or in the case of minimum power loss a closed form expression may not exist. Loss estimation often makes use of datasheet values because it is much easier to scale real experimental data than to build an experimental set-up for the desired operating conditions. However, the use of LUTs means that a closed form expression for minimum power loss cannot be determined. [118] uses the snubber loss equations to represent the switching loss which is not applicable in circuits without snubbers. Another method is to minimize the inductor current at each step as this is relatively easy to do and computationally inexpensive. The peak inductor current is correlated with power loss, achieving the same output voltage with a smaller peak inductor current will result in lower power losses [112]. However, while the peak inductor current is correlated with losses, it only gives the minimum condition for conduction losses. For the minimum power losses, the operating conditions that achieve the minimum switching loss also need to be considered. As previously stated, the direct approach can be computationally complex or infeasible, thus an indirect method for the optimal condition will be derived. In order to determine the operating conditions for minimum power loss, each component of the total power loss can be determined individually

and then a weighted equation is used to average the three results.

5.3.2.1 Minimum Conduction Losses

The minimum conduction losses for both bridges intersect at the same point because the current of both bridges are in phase. P_{cond} was defined in (5.6) and represents the conduction losses, the minimum of this equation will result from the minimum of I_{ds} which in this case is equal to i_L. The minimum i_L RMS occurs approximately around the minimum peak inductor current i_{Lmax}, (4.5) from Chapter 4 can be used in order to determine the point where i_{Lmax} occurs. i_{Lmax} will occur the moment before i_L begins to decrease, while a positive voltage is induced across L_{lk} as seen in Fig. 4.6. Thus, the inductor current will be increasing while V_{1ac} is larger than V_{2ac}/n. Considering again the states previously discussed in section 4.2, V_{1ac} is equal to V_1 during the first two intervals and equal to zero during the third while V_{2ac}/n is equal to V_2 during those same intervals. Thus, V_{1ac} is always larger during the first two intervals and smaller during the third and the peak current will be reached once it hits the end of the charging period or when $t = t_2$.

$$i_{Lmax} = \frac{\alpha n V_1 + V_2(2\sigma + \pi - 2\alpha)}{4n\pi L_{lk} f_s} \tag{5.9}$$

Because (5.9) is linear with respect to both σ and α, taking the derivative will result in a constant and will not be solvable for a set of conditions. First, an equation that is a function of both duty and σ is derived by rearranging the equation for V_2 (4.14).

$$\sigma^2 + 2D_1\pi\sigma + \left(\frac{V_2}{K} - D_1\pi^2 + 2D_1^2\pi^2\right) = 0 \tag{5.10}$$

Treating D_1 as a constant, σ is derived as,

$$\sigma = \frac{-b+/-\sqrt{b^2-4ac}}{2a} \tag{5.11}$$

where:

$$\begin{aligned} a &= 1 \\ b &= -2D_1\pi \\ c &= \tfrac{V_2}{K} - D_1\pi^2 + 2D_1^2\pi^2 \end{aligned} \tag{5.12}$$

substituting (5.11) into (5.9) will give the duty cycle for minimum i_{Lmax}.

$$\frac{d\sigma}{dD_1} = \pi + \frac{2D_1\pi^2 - \pi^2}{2\sqrt{D_1\pi^2 - \frac{V_2}{K} - D_1^2\pi^2}} \tag{5.13}$$

$$\frac{dI_{Lmax}}{dD_1} = 1 + \frac{2D_1\pi - \pi}{2\sqrt{D_1\pi^2 - \frac{V_2}{K} - D_1^2\pi^2}} + \frac{nV_1 - 2V_2}{V_2} \tag{5.14}$$

5.3.2.2 Minimum B_1 Switching Losses

Switching losses are calculated as the overlap in current and voltage during the transition period (5.7). Similar to minimizing the conduction losses, I_{ds} will be minimized during the switching events in order to minimize (5.7). The switches in B_1 transition at i_{L0} and i_{Lmax}, this means that finding the minimum of their combined magnitude will yield the minimum loss.

$$i_{Lmax} + i_L(0) = \frac{\alpha n 2V_1 + V_2(4\sigma - 2\alpha)}{4n\pi L_{lk} f_s} \tag{5.15}$$

Substituting (5.11) in for σ, taking the derivative and setting it equal to zero results in the D_1 for the minimum P_{sw1}.

$$\frac{-nV_1}{V_2} = \frac{2D_1\pi - \pi}{2\sqrt{D_1\pi^2 - \frac{V_1}{K} - D_1^2\pi^2}} \tag{5.16}$$

5.3.2.3 Minimum B_2 Switching Losses

Taking the exact same approach as solving for P_{sw1}, the minimum for P_{sw2} can be determined to occur when $i_{L(t)}$ evaluated at 4.11b is as close to zero as possible.

$$i_L(\sigma) = \frac{\sigma n 2V_1 + \pi V_2 - \alpha V_2}{4n\pi L_{lk} f_s} \tag{5.17}$$

For some operating conditions it is possible to switch B_2 at zero current, otherwise (5.17) should be made as close to zero as possible.

5.3.2.4 Minimum Total Losses

As discussed at the beginning of this section, the minimum losses will be solved by taking a sum of the duty cycles corresponding to each optimal condition. Each duty cycle will be weighted and the weights will be determined by finding the approximate change in power across the D_1 range. First, the intersection of the switching losses will be calculated, this can be done with (5.7) and the change in I_{ds} can be found with (5.15) and (5.17) for B_1 and B_2 respectively.

$$w_1 = \frac{dP_{sw1}}{dP_{sw1} + dP_{sw2}} \tag{5.18}$$

w_1 is the weight for D_1 associated with P_{sw1}, dP_{sw1} and dP_{sw2} are the change in switching loss for B_1 and B_2, respectively. w_1 and w_2 must sum to 1, so $1 - w_1$ will be equal to w_2. Using (5.18) and the associated D_1, the crossover point between switching losses can be solved.

$$D_{sw} = w_1 D_{sw1} + w_2 D_{sw2} \tag{5.19}$$

D_{sw} is the duty cycle for the minimum switching loss, D_{sw1} and D_{sw2} are the D_1 resulting in the minimum switching loss for B_1 and B_2 respectively. After finding the minimum switching loss the same process will be repeated for the intersection between the minimum switching loss and minimum conduction loss using another set of weights. The weight calculation in this case will depend on the conduction losses (5.6) as well as the switching loss (5.7) as shown.

$$w_3 = \frac{dP_{cond}}{dP_{sw} + dP_{cond}} \tag{5.20}$$

For the change in P_{cond}, I_{ds} can be approximated with the change in squared inductor current.

$$dP_{cond} = \frac{i_{Lmax}^2}{2} \tag{5.21}$$

The change in P_{sw} can be equal to the sum of dP_{sw1} and dP_{sw2}. Again the weights w_3 and w_4 must sum to 1, this means to find w_4, $1-w_3$ will be used. Finally, (5.14), (5.19) and (5.20) can be combined to determine the duty cycle resulting in the minimum power loss.

$$D_{pmin} = w_3 D_{sw} + w_4 D_{cond} \tag{5.22}$$

D_{pmin} is the duty cycle resulting in the minimum power loss, D_{cond} is the D_1 resulting in minimum conduction losses given by (5.14).

5.3.2.5 Hybird Control Scheme

Depending on the desired output voltage it will be infeasible to use DPSM. This is true for small output power conditions, in this case the phase shift will be set to zero and only the duty cycle will be varied. To determine this crossover point between control schemes, DPSM will be implemented only when the entire set of σ values are real and positive. To determine this, σ will be solved to be greater than 0. Thus, the result of the square root will be a positive value that must be greater than $2\pi D_1$ in (5.11).

$$0 \geq -2D_1^2\pi^2 + D_1\pi^2 - \frac{V_2}{K} \tag{5.23}$$

Maximizing the right side of the equation with respect to D_1 will give the worst-case scenario. Thus, V_2 can be solved such that σ is always greater than zero.

$$0 = -4D_1\pi^2 + \pi^2 \tag{5.24}$$

(5.24) results in $D_1 = 0.25$, which can be subbed into (5.23) resulting in,

$$V_{2limit} = \frac{k\pi^2}{8} \tag{5.25}$$

where V_{2limit} is the reference voltage boundary condition, any reference above this value will use DPSM, while voltage references below this point will use just duty control.

5.4 Conclusion

The investigation of a the CHFL-DAB which is a single-stage isolated DC/AC converter was presented. The major advantage of the CHFL-DAB over the two stage approach is efficiency, which is realized through a significant reduction in switching losses due to fewer actively switching devices in the CHFL-DAB. This advantage makes the CHFL-DAB more suited to a high-frequency application where the switching losses dominate total losses. However, it should be noted that despite the same power rating, the peak current in the CHFL-DAB under these conditions is approximately twice larger due to the smaller leakage inductance. The larger peak current will cause higher device stress and may even result in higher rated devices or more devices in parallel. Before a prototype is developed to validate the proposed control, the PCB and gate driver design for GaN must first be addressed.

Chapter 6

Design of Cycloconverter-Type DAB for Isolated DC/AC Applications

6.1 Introduction

Power electronic converters utilising GaN have the potential for improvements to power density and efficiency. GaN enable higher switching frequencies which allows the passive component sizes to be reduced. In addition, GaN devices have low R_{dson} and gate charge making them highly efficient which allows heat sinks to be sized smaller due to the reduced losses, thus further increases power density. The benefits of GaN do not come without challenges, this chapter will explore some potential issues as well as how to overcome them and make the most out GaNs benefits.

6.1.1 GaN Design Challenges

There are four major issues for GaN devices, these issues are possible in other transistors but because of the characteristics of GaN they are more suceptible. The issues are the following:

- gate ringing
- common mode transient noises
- cross conduction
- over voltage

GaN devices are particularly sensitive to the above issues which can cause shoot through in a phase leg, leading to additional losses or outright device damage. This problem is due to the unintentional turn on of the synchronous device.

6.1.1.1 Gate Ringing

Gate ringing or oscillations refer to the resonance that occurs on the gate-source voltage and is caused by the parasitic source inductance being shared between the gate loop and power loop [119]. The resonant network is formed between the gate input capacitance (C_{iss}) and the parasitic inductance in the gate loop [120]. There are two forms of parasitic inductance: parasitic gate inductance that is a result of thin PCB traces as well as a long path between the gate drive and gate pin, and common source inductance which is shared between the power loop and the gate loop. Common source inductance is a major contributor to the oscillations as large changes in the drain current cause voltages to appear across this inductance which

negatively impacts the drive voltage [121]. During a turn on event, the drain-source current is increasing which causes a voltage dip at the gate, when the device turns off the large current change induces a negative voltage on the source which will create a spike at the gate. The voltage spikes and dips that occur due to the device transitions and the resulting oscillations of the drain-source voltage are shown in Fig. 6.1.

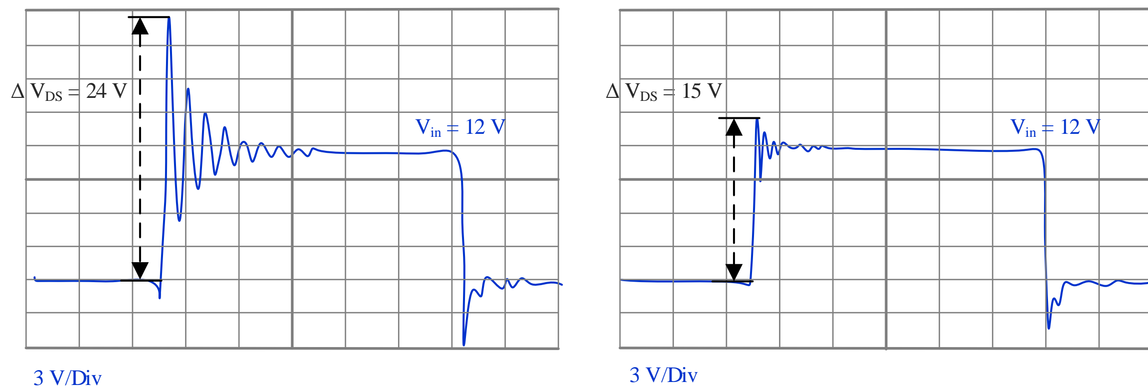


Figure 6.1: Reduction in loop inductance is shown to reduce oscillations that lead to voltage overshoot [122].

These spikes can resonate with the parasitic capacitances and result in an oscillatory behaviour that can damage the device by exceeding its maximum ratings. Stray inductances also contribute to other issues in the switch such as the negative feedback of the common source inductance which acts to slow down the current transition and increase switching losses, this makes minimizing these inductances is important for proper control operation [120]. This chapter will discuss the three most common methods in literature to improve problems resulting from the parasitics in the circuit: PCB layout, kelvin source connection, and ferrite beads.

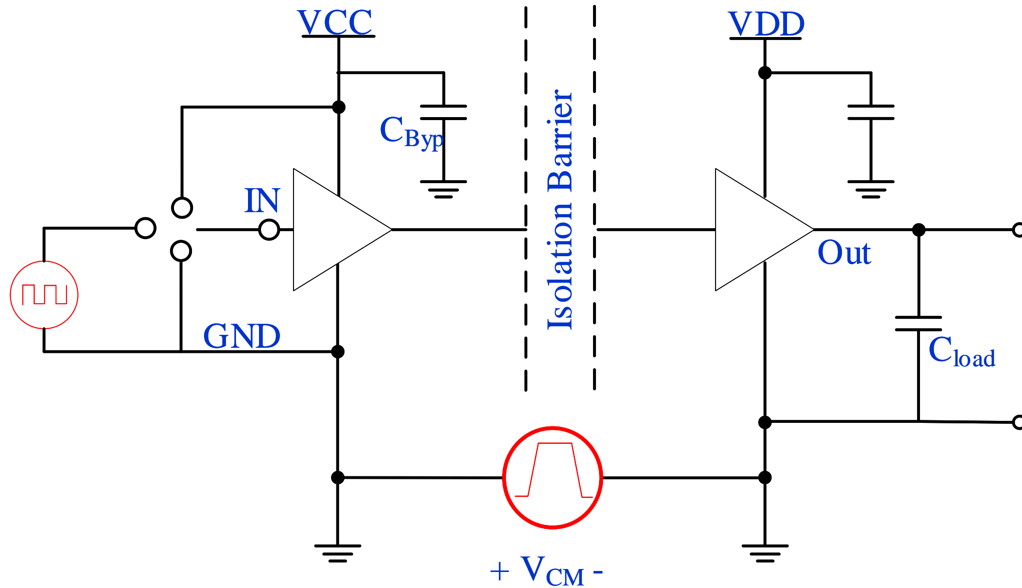


Figure 6.2: standard isolated gate drive circuit with common mode path.

6.1.1.2 Common Mode Transient Noise

Common-mode (CM) noise is the unwanted signal that appears between both the power ground and the signal ground as shown in Fig. 6.2. CM noise is caused by the fast transition periods of the GaN device and the resulting noise coupled through the ground planes via parasitic capacitance. The mid-point in a half-bridge phase leg is neither ground nor is it tied to the supply, this floating reference point which occurs in most switching applications is typically associated with CM noise. Common mode transient immunity (CMTI) is the rating that defines the protection against the voltage level that appears between the signal ground and power ground with respect to the voltage rise time. The CMTI rating is one of the most critical aspects of a gate driver. Many switching applications also require the use of isolation for the gate driving circuit due to the presence of high voltage. Isolation serves the purpose of separating the signals from the power circuit for safety which also has

the added benefit of improving performance as it severs the ground loop which is a path for harmful noise [123]. CM noise is problematic as it can trigger a host of problems in the driver such as false turn on. Therefore, having a high CMTI is a must with the manufacturer GaN Systems recommending at least 50 kV/μs [124]. Even with isolation separating the control ground and power ground, a small parasitic capacitance between the two planes exists which couples the transient noise. Certain steps can be taken to improve the CMTI rating of the gate drive which will prevent the noise from having any effect, but these efforts may go to waste if PCB design is not addressed as it can have a major impact on this problem by introducing many parasitics.

In [125], a modular GaN phase leg including the gate driver selection and the sensing circuitry is built. The authors discuss CMTI and the lack of availability of an isolator with >50 kV/μs immunity and thus they place an emphasis on improving the driver design and the rejection capability to CM noise. The researchers discuss the importance of using an isolator for both the top and bottom switches as this creates a large impedance path for the noise to travel through compared to isolating just the top side. Adding a second isolator is also beneficial to the timing of the switches because each PWM path now has the same delay. However, some additional safeguards are also discussed to prevent the noise from travelling through other unwanted low impedance paths and interfering with the DSP. Two capacitances are suggested to be added to create a low impedance path, they are connected between the phase-leg negative rail and chassis, and signal ground and chassis. In [125] only two isolators were found to withstand the tests: HCPL-0900 and SIB610EC-B-IS. Since this work, more options for isolators are available on the market. It is now possible to find off

the shelf isolators with greater than 100 kV/μs CMTI. Thus, adding a common mode choke and using isolation for the low side gate may no longer be required with the new isolator options, but they are available options if CM noise is a severe issue.

6.1.1.3 Accidental Turn on

Previously, the parasitic elements were discussed and how they can cause large oscillations to appear across the switch. Not only do these parasitic components contribute to oscillations, accidental turn on of the synchronous switch may occur due to the Miller current flow and cross conduction of the half-bridge.

The half-bridge is one of the most integral parts of many switching applications. The half bridge places two switches in series with the output taken at the joining point between the switches. Half-bridges are controlled in a complimentary fashion, meaning that when one switch is turned on, the other is turned off. During a switching event the switch that is undergoing a state transition is denoted as the 'active' switch, while the device that remains off may be denoted as the 'synchronous' switch. When the active switch is changing states the voltage across the synchronous switch is affected, this causes current to flow to and from the parasitic capacitances. The magnitude of the induced currents depends on the dv/dt of the active switch, high power applications are much more susceptible than lower power applications. One problem that can arise from these induced currents is the accidental turn on of the synchronous switch, this can short the DC bus and ground leading to increased losses or even device failure. GaN devices have a disadvantage over other WBG devices in that their driving voltages are much lower than comparable SiC devices. The typically recommended manufacturer levels range from -3 to 6 V, while SiC can be in the range

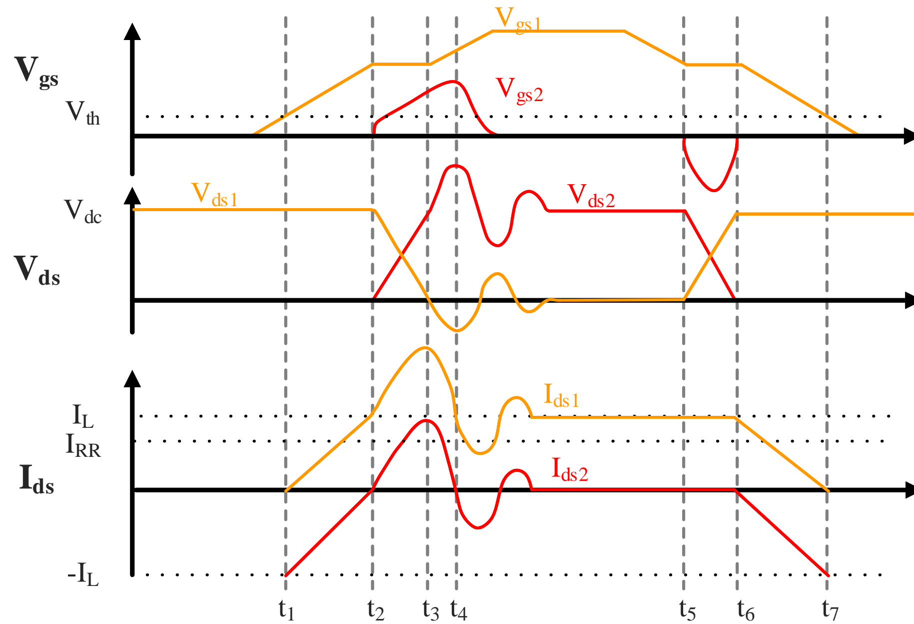


Figure 6.3: On-transition of active switch (orange) and the affected signals of the synchronous switch (red).

of -5 to 20 V. Therefore, spurious voltage spikes can easily meet the device ratings of GaN and trigger the turn on of the device. Not only are GaN devices more susceptible due to the low drive ratings, the device voltage and current slew rates are much faster than other currently available devices compounding the problem of accidental transitions. Fig. 6.3 details the timing diagram of a switching transition for the active device and how the complimentary waveforms are affected in the synchronous device. Using a small resistance during the off state is one method to reduce the voltage spike, another option is to provide a negative voltage to the gate. A negative gate voltage will prevent a small positive spike from exceeding the gate threshold and causing an accidental turn on event [126]. A negative voltage on the gate of a GaN device increases the reverse conduction current and lowers the efficiency by causing more dead time losses [127]. The use of a negative off voltage needs to be considered

carefully given that a negative voltage spike can easily exceed the lower voltage limit of a GaN device. In [127] several tests are conducted using a double pulse test and several gate drive configurations with different gate resistors in an attempt to characterize cross conduction losses of GaN in a phase leg topology. The researchers explore the losses and performance of a half bridge device with varying gate resistors namely a zero-resistance set up and an asymmetric set up and conclude that cross conduction can be reduced with asymmetrical gate resistance. However, it is noted that cross conduction is not completely removed and what little is gained from the prevention of cross conduction is lost to the reduction of gate transition speed. It is concluded that this trade-off of increased switching losses is not a good compromise but may be viable for low load operating, furthermore they recommend active gate driving as a potential solution. This research showcases the problem with WBG devices and does a good job of creating the narrative of how impactful cross conduction is on switching performance. However, it does little to offer any meaningful solution. Asymmetric resistance for gate drives is standard practice, most manufacturers will include this type of schematic in the datasheet. [128] proposes using a two-stage voltage during the off time, an additional power supply is added such that both voltage levels could be negative for robustness. During the turn on event of the active switch a small positive spike appears on the synchronous switch, it is during this time that the more negative voltage level biases the GaN device. Afterwards, the less negative voltage is applied in preparation for the negative voltage spike that appears during the turn off event of the active switch. Similar results are found in [129] where researchers propose using a 2-level voltage for both the on and off of the gate driver and find that mainly the off performance is affected with much lower oscillations without increasing

losses and off time too much.

One mechanism of accidental turn on that was briefly mentioned earlier is Miller current flow. Miller current results from high dv/dt across the drain to source terminals which induces current flow from the parasitic capacitances. The standard equation used to describe capacitor current can be used to define Miller current,

$$I_{miller} = C_{gd}\frac{dv}{dt} \tag{6.1}$$

where dv/dt represents the change in V_{ds}. When V_{ds} increases from low to high, current flows from C_{gd}, this causes a voltage spike on the gate that can exceed the threshold voltage and turn the device on. Having small gate loop inductance and a low impedance path helps to reduce this spike. Miller current flow when V_{ds} goes from high to low induces a current flow from source to drain causing a negative voltage spike. It is recommended in the literature and by the manufacturer GaN Systems to use asymmetric on/off resistance [124]. For single output drives this requires the use of a diode to provide a lower resistance return path. However, this current flow is more problematic for single output drivers as the R_{goff} is blocked by a diode resulting in a larger voltage spike. For this reason a diode clamp is suggested in [124], but this clamp makes use of a Zener diode which lacks the ability to clamp high frequency ringing [130]. Fig. 6.4 shows an example of the paths the Miller current can take during the off state of the synchronous switch. Unintended current flow caused by the active device turning on can induce a voltage on the gate of the synchronous switch because of the Miller current flowing through the gate resistance, a larger resistance will result in a larger voltage spike [126].

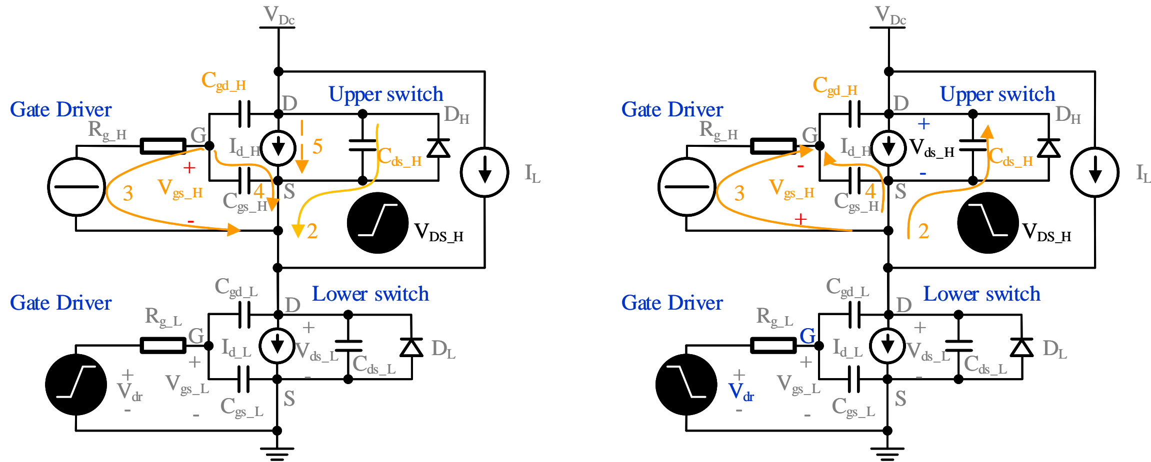


Figure 6.4: Miller current flow for half bridge.

6.1.1.4 Over Voltage Protection

Over voltage is an issue for GaN as the typical driving range for the GaN is about -3 V to 6 V. Thus, any spurious voltage spikes on the gate drive are a major concern as it can easily overcome the low threshold voltage which can trigger device turn on as previously mentioned, or it can outright damage the device by exceeding limits which for many devices are not much higher than the recommended driving voltage. For example, the GaN systems GS66506T has a maximum voltage rating of only +7 V [131]. Another issue related to over voltage is negative spurious triggers during turn off. GaN devices do not have an intrinsic body diode for freewheeling currents, instead they reverse conduct the current through the 2DEG. The voltage drop across the device in this case is related to the voltage on the gate, larger negative voltages cause greater reverse conduction which can increase dead-time losses. As stated, GaN devices have much tighter gate voltage requirements compared to Si and SiC, the maximum range is approximately -10 to +7 volts, this makes protecting against voltage spikes a priority as even a small spike could cause damage. One method is to

include a Zener diode between the gate and source such that if the voltage exceeds the diode rating it will start conducting. [132] discusses this technique and how it will affect the performance, the authors mention that Zener diodes have a capacitance that is on par with the (C_{gs}) value of a GaN device. Thus, by placing the Zenner across the gate and source it is effectively adding its capacitance to that of the GaN switch. Increased capacitance increases switching losses by slowing down the switching speed of the switch [132,133] in addition to causing other resonant issues [124]. The authors conclude that the Zener diode mainly contributes a noticeable effect for drives with high gate resistance, otherwise the effects can largely be ignored. One other point of interest is that the authors report increased efficiency with the Zener diode without any explanation, despite the expected increase in switching losses. Another option is to use a gate driver with multiple outputs, GaN Systems only recommends a clamping diode when using single output gate drives [124]. Some researchers still found it useful to include a Miller clamp as seen in [134] which includes a separate on and off path for the gate, but also an additional transistor that is only on when the switch is off to bypass the Miller current.

6.2 Converter Design Considerations

When designing a PCB, the placement of the devices is critical in relation to one another. The trace size and width can introduce common-source parasitic inductance which as previously stated can be a problem for fast current transitions. However, this is not the only issue that can be addressed with PCB design, additional stray capacitances can also be introduced to the system with the overlapping of planes like the control and signal grounds. One such example of this is explored in [121]

where researchers find accidental turn on occurring when the dv/dt was below the 50 kV/μs as provided by the digital isolator. The cause was found to be extra parasitic capacitance resulting from the overlapping of the V_{sw} plane and the primary ground plane, minimizing the area of overlap with a redesigned board alleviated the problem. Careful design consideration of the PCB can alleviate many potential issues, using wide PCB traces is recommended for the gate drive as this reduces the amount of parasitic inductance present [120]. The gate driver should be placed in close proximity to the switches, this reduces the gate loop length and the associated parasitic inductances [135].

6.2.1 PCB Design

When designing a converter with WBG devices there are two very important considerations which can greatly impact device performance: PCB layout and Gate drive design/selection. The performance of the gate driver can be severely impacted by dv/dt and di/dt transients if the PCB layout is sub-optimal. Careful design considerations can be taken to maintain clean control signals that allow the GaN switches to operate at high efficiency with greater reliability. Various techniques can be employed to improve the fidelity of the PWM signals as well as gate driver design. For example, one mistake that can easily be avoided is overlapping the ground planes of the gate driver. Parasitic capacitance exists between overlapped PCB layers and will provide a coupling path for CM noise [136].

The desire for high switching frequency is related to the passive components in the converter and how the size of such passive components is inversely related to the switching frequency. By increasing switching frequency, the passive inductive and

capacitive components will decrease in size while maintaining the same filter performance of a system with a lower frequency and larger passive components. There are several drawbacks with increasing switching frequency and using devices with slew rates >50 kV/μs, these drawbacks should be considered carefully when selecting the switching device and designing the accompanying gate driver and PCB layout. In practice PCB board layouts and device packages contain many parasitic elements. Parasitic inductance increases with large current loop paths while parasitic capacitance increases due to overlapping layers in close proximity. Typically, parasitic parameters are very small which means their impact is often negligible on circuit performance. However, as device switching performance increases such as with GaN which is capable of rise and fall times that exceed 100 kV/μs, the effects of these parasitic elements in non-optimized PCB layouts becomes readily apparent [137, 138]. Primarily there are three main areas of a circuit impacted by the parasitic inductance:

- common-source inductance (shared between power loop and gate loop)
- power loop inductance
- gate loop inductance

These three inductances are listed in order of their importance and how detrimental they can be to the circuit [139, 140]. Because the gate-loop inductance is not as critical, this section will primarily focus on techniques for reducing the common-source inductance and power loop inductance. The primary concern for the gate loop inductance is unbalancing the switching transitions of devices in parallel, in this case it should be ensured that the loop lengths are identical [141]. In general the

PCB layout should be designed such that components in a loop be placed as close as possible to minimize the inductance, but this cannot remove all the parasitics. Thus, several design standards can be employed to reduce the common-source inductance and the power loop inductance.

6.2.1.1 Kelvin Source Connection

Another method to improving the performance in the presence of stray inductance is to use an additional source connection called the 'Kelvin source connection'. The Kelvin source connection is a fourth pin on the package as shown in Fig. 6.5. This pin is a separate source connection for the gate drive. The main advantage of the Kelvin source connection is that it decouples the power loop and control loop. In a traditional MOSFET package, the control loop and power loop share the same source connection. By sharing the source connection the stray package inductance is also shared between both loops. Thus, the large power loop di/dt has a direct influence on the gate signal compared to the much smaller di/dt of the gate drive

Figure 6.5: Kelvin source connection footprint (left), Package parasitics associated with connection (right).

current [142]. Some researchers have cited some concerns with the Kelvin source connection such as increased gate inductance [127] which can cause gate ringing as the inductance resonates with the gate capacitance. Another concern is the lack of a standard package [143]. These concerns do not seem well founded because the gate inductance is of the least importance, this is why most researchers recommend the Kelvin source and many manufacturers provide this connection on their switches. The difficulty in switching GaN at high frequencies is largely tied to the parasitics of the package and PCB layout, GaN devices can transition between on and off extremly fast which results in large di/dt and dv/dt. The increased di/dt in particular can cause extremely large voltage spikes on the gate if the package inductance is shared between both the power loop and control loop making the decoupling almost necessary as large voltage spikes or dips can falsely trigger the switching device or exceed device ratings and cause damage. Therefore, the trade off of decoupling the source inductance at the cost of increasing gate inductance is worthwhile.

6.2.1.2 Flux Cancellation

Wires and traces that make up the power loop of a circuit contribute parasitic inductance to the circuit based on the size of this loop. Parasitic inductance in the power loop can increase V_{ds} overshoot leading to EMI issues, the magnetic flux generated could interfere with the gate driver operation or other components in the system [140]. A simple method for alleviating this issue is to use the flux cancelling by overlapping layers that carry high frequency current in opposing directions. This can be seen from

the equation for inductance and its dependence on magnetic flux density (6.2).

$$L = \frac{\Psi}{I} = \int \frac{B*dS}{I} \tag{6.2}$$

Fig 6.6 shows two layers with opposing currents and how the magnetic fields generated around them lead to opposing magnetic fields which can cancel each other out.

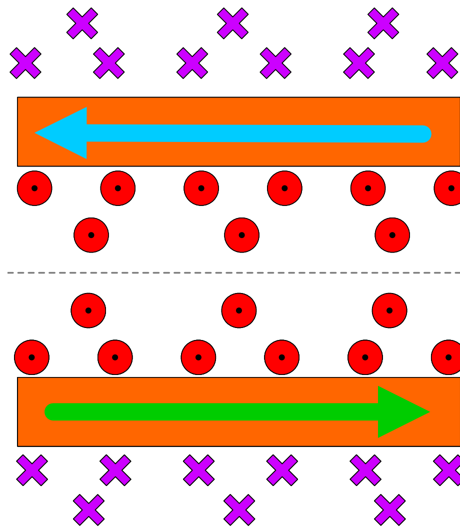


Figure 6.6: Generated magnetic fields from two traces carrying current in opposing directions.

6.2.2 Gate Driver Design

6.1.1.2 introduced CM noise, this section will disucss the several popular methods for isolating the gate driver and providing high CMTI. The most common options found in research and industry includes [144]:

- opto-couplers.
- transformative (pulse transformer or digital)

- capacitive isolation

Each method serves the purpose of galvanic isolation by providing some physical separation between the low power circuit and high power circuit, helping to ensure safety of the user and system. All the methods have some pros and cons and will be discussed in detail.

6.2.2.1 Opto-Couplers

Opto-couplers are an outdated option for gate drive and are inferior to digital isolators in many ways, they are mentioned here for completeness as most research does not make use of them. Opto-couplers are especially not suitable for GaN gate drive as they have relatively long propagation delay which hinders their ability to be used for high frequency operation [144]. Opto-couplers have several other undesirable features, their low CMTI rating and large parasitic capacitances couple transient noise through the shielding of the opto-coupler. This noise may result in a current dip during high logic state or a current spike during low logic state which will result in the LED transmitting the wrong value. CMTI is a very important parameter for GaN gate drivers as the extremely fast slew rates can easily generate common mode noise on the scale of 50 kV/μs. Opto-couplers also perform differently based on the temperature and the age of the opto-coupler. This performance affects the propagation delay which makes it very hard to synchronize the switches and can result in poor timing and larger than expected dead time losses [144]. Opto-couplers also lack robustness which is a result of mechanisms wearing out within the device which make the opto-couplers largely unattractive for GaN gate drivers.

There are ways recommended by opto-coupler manufacturers to improve the device

performance in environments with high CM noise but these methods require additional parts and compromise the device life time and efficiency. One such method is to overdrive the device during on time which will prevent a small negative transient or dip in current from turning the device off. During the off time a switch can be used to short the diode so that any transient currents will flow through the open switch and not accidentally turn the device on [145]. There are two issues with this method, the shorted diode increases the gate driver losses from the additional current and overdriving the device negatively impacts the longevity [145].

6.2.2.2 Pulse Transformers

Before digital ICs, pulse transformers were an attractive option for providing isolation, CMTI, and negligible transmission delay. However, they suffer from a few issues that make them inferior to the digital isolators. Transformers require a capacitor in series to prevent any DC value from saturating the transformer, in addition to this the transformer must be "reset" during the off time making it unsuitable for larger duty cycles above 50%. Another drawback to this method is the leakage inductance that is capable of forming a resonant circuit with the input capacitances of the gate [120]. Finally, the package size required for the gate drive of pulse transformers is quite a bit larger than digital.

6.2.2.3 Digital Isolation

Digital isolation appears to be the most common form of isolation due to its ability to provide good CMTI with a reasonable size package [145, 146]. The architecture of a digital isolator can varry from device to device. This is because it is possible to

use micro transformers or capacitive isolation barriers as well as different isolating materials or data transmission methods. Capacitive digital isolators are not differential by default and require additional circuitry to provide differential capability [147]. Differential signal input is the process of taking two input pins and outputting the difference between the pins [146], any CM noise or other interference present on both input terminals will cancel out. Using differential inputs improves the CMTI of the gate driver due to the cancellation of any noise present on the input pins [136, 145]. Transformers are naturally capable of differential data transmission so micro transformers may be highly alluring for higher CMTI environments. Another important aspect of digital isolation is the data transmission, on-off keying (OOK) for example. OOK is a method of transmitting data by using transmission as one state and no transmission as another state. The transmission of data requires a high frequency signal that can pass the isolation barrier [144], this isolation barrier is also uniform with minimal variance of 20% compared to the 300% difference in conventional opto-couplers [145]. The power efficiency of digital isolation is also much greater, an RF signal requires much less power than an LED does to transmit the light signal in an opto-coupler [145]. There exist several other data transmission techniques, another popular one is a pulse method which encodes rising edges as two pulses and falling edges as a single pulse. The pulse method has an advantage over the OOK in terms of power because it does not require a continuous transmission for the on state. Another key detail is timing delay of the device, this is an important factor in gate drives as the delay for the top and bottom switch should be matched so that the dead time is minimized [146, 148]. Other features of the digital isolator that make it a much more attractive option include its lower input-output parasitic capacitance which is

the CMTI coupling capacitance [149]. Also, the design of the digital receiver is made in such a way that it is very selective of the frequency.

Transformer-based digital isolators have the inherent advantage over capacitive digital isolators of being able to provide higher CMTI which cannot provide more than 50 kV/μs [150]. A transformative digital isolator utilizing polyimide insulation is used to achieve 200 kV/μs CMTI. They contrast the performance of this isolator with several other works, some of which are pulse transformers and others are capacitive digital isolators. The results show that the CMTI and surge protection are higher than all other works but the amount of current drawn by this gate driver is also higher. Table 6.1 presents a comparison between some of the available gate drives and the isolator presented in [150].

Table 6.1: Gate Drive Isolator Performance.

Part Number	Manufacturer	Isolation Type	Max Propagation delay (off)	Max Propagation delay (on)	CMTI (kV/μs)
Si2871 Si8274	Silicon Labs	Capacitive	75 ns 75 ns	75 ns 75 ns	200 200
ISO7763F ISOW7843	Texas Instruments	Capacitive	16 ns 19.7 ns	16 ns 19.7 ns	100 100
N/A	[150]	Transformative	11 ns	11 ns	200
ADuM4223 ADuM1100 ADuM4121	Analog devices	Transformative	65 ns 28 ns 53 ns	65 ns 28 ns 42 ns	25 35 150
6N139-HCPL-0701	HP	Opto-coupler	2000 ns	10000 ns	10
ACPL-P346	Broadcom	Opto-coupler	120 ns	120 ns	100

6.2.2.4 Ferrite Beads

Ferrite beads are often recommended by the manufacturers and researchers in cases of high gate ringing [124, 130]. Using a filter or an increased gate resistor to damp oscillations can present problems as the filters introduce additional capacitance and inductance, likewise the resistive option increases the turn on and off times and increases the losses of the system. Ferrite beads offer a flexible solution for high frequency

ringing as they impose a resistance on the system that is dependent on frequency. For low frequencies the ferrite bead is a small resistance, but for very high frequencies in gate oscillations the resistance is very high [151]. This makes the ferrite bead very good at damping unwanted oscillatory behaviour without compromising switching performance.

6.2.2.5 Inductive Gate Drive

A slightly different approach to handling the induced voltage spikes and oscillation is tackled in [143], a deep analysis of the common-source inductance is performed on a super junction (SJ) MOSFET. The mechanisms for the inductance having a large impact on the gate drive are due to the extreme non-linearity of the switch capacitance C_{ds}. The switch C_{ds} of a super junction MOSFET and GaN switch are compared in Fig. 6.7 to show that this analysis of SJ MOSFETS will hold true for any highly non-linear switch. The analysis shows the impact of the common source inductance, a voltage generated across the L_{sc} causes a change in the gate current polarity. Changing the impedance from resistive to primarily inductive will remove the direct impact of the L_{sc} because any change in voltage will cause the inductor of the gate to try and maintain the gate current. The drawback of this method includes an increase to the switching delay time as well as potential resonance between L_{gs} and C_{gs}. [143] cites that the resonant time is much longer than the switching time. Another crucial point is that they suggest an active component that utilizes the inductance at the beginning and that a resistive load could be used later.

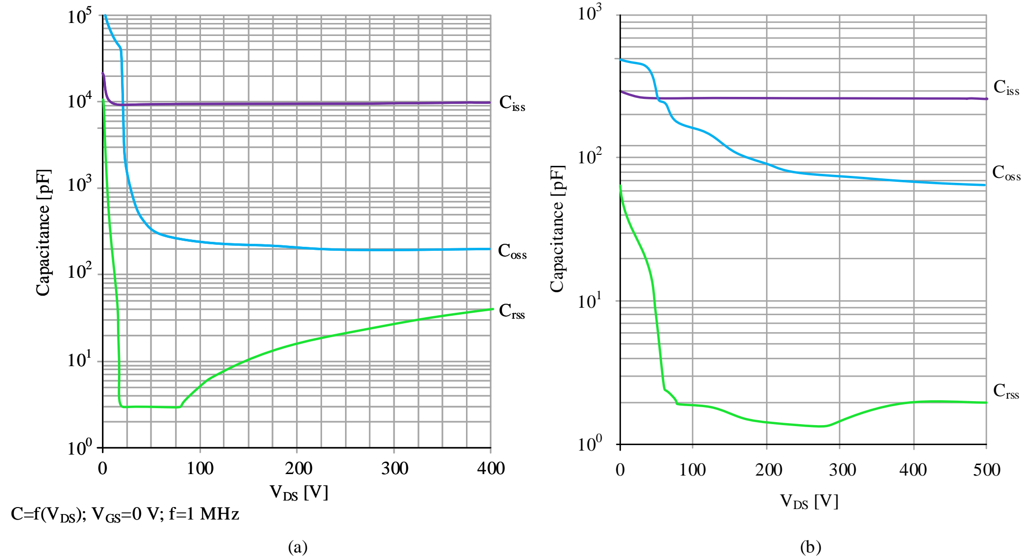


Figure 6.7: Comparison of non-linearity parasitic capacitances. (a) Super junction MOSFET [152]. (b) GaN HEMT [153].

6.2.2.6 Multi-Output Gate Driver

Multi-output gate drivers are one available option when more control over the turn on and off transition is desired. A multi-output gate driver contains a separate path that is usually used to sink current during turn off. This may be very useful for non-insulated GaN GITs which require a small continuous current to remain in conduction.

In terms of single output gate drives, the RC–type gate drives are a choice method for driving non-insulated gate drives which require a constant current to remain in conduction [122]. These gate drivers typically employ a capacitor to block some part of the current once the device is turned on. Researchers show one application of an RC-type drive in [154] along with a method to improve it. The main drawback of this method is that the discharge time of the capacitor is long during the off time, this capacitor creates a negative voltage which increases the reverse conduction of the GaN device. Therefore, improving the discharge speed will reduce reverse conduction

losses. The researchers propose adding a diode and another resistor to create a lower RC constant loop during turn off to significantly increase discharging speeds. Another drawback as noted by the authors is that the added diode will create a negative voltage at the gate based on its forward drop which will negatively impact the next turn on.

The work in [155] discusses the RC type gate drive and what the author denotes "GaN GIT driver". The GaN GIT gate drive uses a multi output driver to provide sources for the turn on currents. They have a high current output that is in series with a capacitor to block the current after the device is turned on. This path is in parallel with a second output that provides a small current to keep the device on. Finally, there is an output to sink current when the device needs to be turned off. The idea behind this is that having a single turn on path limits the speed at which the device turns on, so using two paths allows for a fast-high current path at the start to optimize the device performance. Another advantage of this driver is the ability to use the additional off path as a low impedance path for the Miller current. Using two outputs also allows the gate voltage to remain fixed in the off state as opposed to single output RC type drives which experience a voltage dip during turn off based on the charge of the speed up capacitor. The RC type circuit does offer the advantage of being able to recover to zero volts which is beneficial compared to always applying the negative rail during turn off. [129] presents a two-stage gate driver for reducing voltage overshoot and gate ringing. In comparison to standard approaches of increasing the external gate resistance and capacitance, the two-stage gate driver offers similar performance improvements without increasing the losses by as large a margin. By using multiple output voltage levels the di/dt on the gate can be managed, this would reduce any impact that the gate inductance may have.

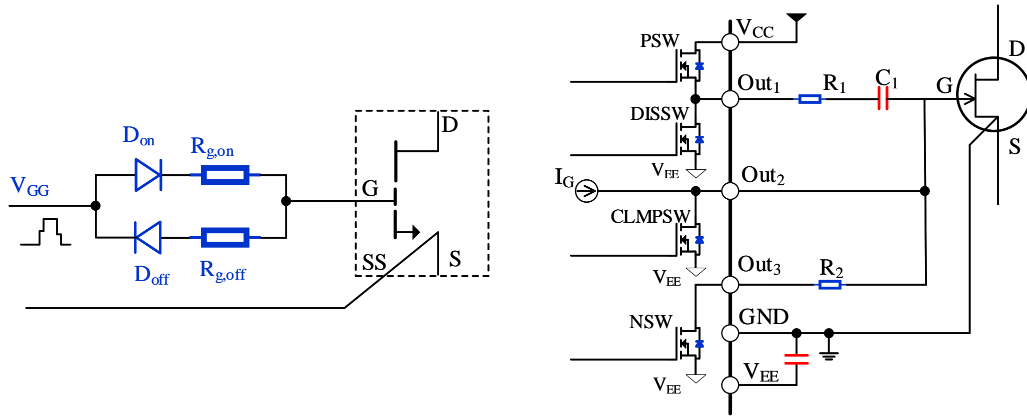


Figure 6.8: Single output Drive (left), multi-output drive (right).

6.2.2.7 Active Gate Drive

Many researchers have considered using multiple output stages for gate driving to alter the performance of the turn on/off. By using multiple outputs, it becomes possible to provide a larger current during the initial turn on to quickly charge the gate followed by a smaller output. In the case of a GaN device with a non-insulated Gate, this change can be used to keep the device in conduction. Researchers in [156] explore the multi output gate drive and how it affects the gate ringing experienced with high slew rates, extending the multi-output drive to include a third output used for turn on is proposed. With this addition it becomes possible to slowly ramp up the current used for turn on, this allows the gate current to achieve a smaller di/dt and become less affected by the parasitic inductance in the gate loop. Researchers in [157] attempt to reduce the amount of ringing in the gate voltage during by using a multi-stage driver to lower the di/dt. By using multiple gate driver outputs, several different output currents can be used to create a more gradual drop off. The simulation results show that the voltage oscillations are much less severe with the overall slew rate remaining relatively high. Multi-output gate driving leads into a more complex

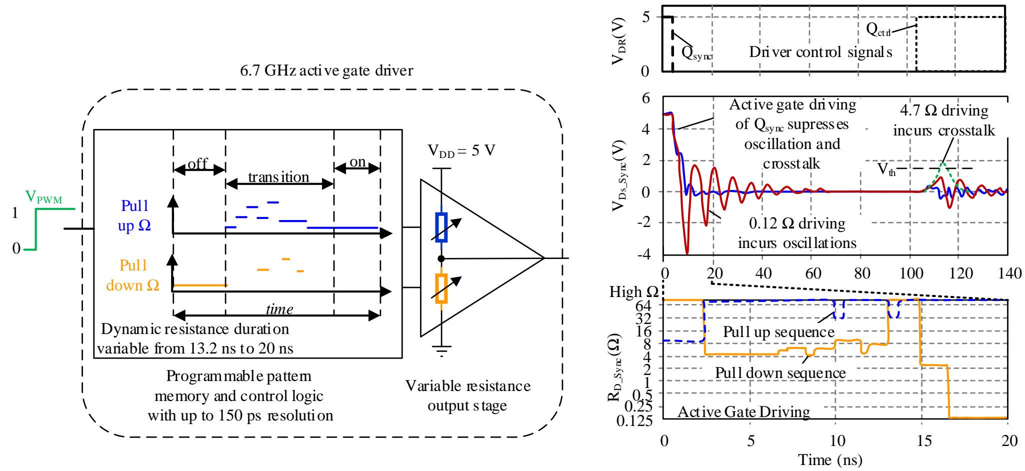


Figure 6.9: Active gate drive [158].

area of gate drivers, this area is known as active gate driving. The concept is like that of multi output gate driving and uses a control method to produce an optimal current, voltage, or resistance at each stage of the gate charging. Currently, this has not been discussed at length for GaN devices but it has been explored for both SiC and Si. Active gate driving is the process of trying to apply a more sophisticated waveform to the gate to better control the characteristics of the switch. A simple method of this process is feed forward control, which can be seen applied to SiC in [133], wherein the controller makes use of a delay to initially reduce the PWM signal at the start of turn on or increase the negative PWM at the beginning of turn off. The authors report fewer gate oscillations and reduced drain current overshoot but they do not discuss the drawbacks such as the increased turn on delay time and the susceptibility to cross talk during turn off. Active gate driving is not without its problems as developing this strategy for SiC devices was not trivial. Researchers in [159] discuss the active gate driver(AGD) control for a SiC device as well as the problems in doing so. SiC have very fast transients and are only getting faster, the

reported MOSFET in the paper had a transition time around 50 ns and the discussed closed loop AGD could have delays of approximately 10 ns due to comparators and propagation delay through logic gates. These delays are not easy to deal with as the state of the art SiC have very short rise and fall times, GaN have even greater switching speeds making any amount of delay very difficult to deal with. Table 6.2 summarizes some key switching characteristics of available GaN and SiC MOSFETs. Looking at the transition time for GaN, it should be readily apparent that any sort of feedback loop would be extremely difficult and complex to implement, in addition to this the analog measuring circuits would need very high bandwidth to detect the fast transitions. The proposed gate driver is an open loop design, the premise of which is that the switching transition is predicable and timing information can be used from the datasheet to apply a specified gate control technique. This approach is appealing as it does not require additional sensory circuitry and does not require adjustments for timing delays. However, it would require precise knowledge of the switch and any parasitics in the circuit could alter the timing enough to cause issue. Researchers in [160] take a similar approach to the open loop active gate by adding a gate assist circuit that is used to offer four output voltage levels and variable resistance. The control for the additional transistors is based on the logic for the primary transistors so no feedback is needed. The authors of [161] use an open loop control scheme for GaN with a control that has 150 ps timing resolution and a programmable gate sequence. [158, 162, 163] all detail works an on active gate driver that uses control schemes pre-loaded into a memory by an external controller.

Table 6.2: Switching Transition Times for WBG Devices

Part #	Manufacturer	Voltage Rating(V)	Current Ratting(A)	Rise time(ns)	Fall time(ns)
C2M0080120D	CREE	1200	36	20	19
SCH2080KE	Rohm	1200	40	33	28
C3M0075120K	CREE	1200	30	11	11
GS66508T	GaN Systems	650	30	3.7	5.2

6.3 Summary

In this chapter the positive attributes of GaN devices such as their low switching losses and on state resistance leading to high efficiency and the flexibility to use switching frequencies in the MHz enabling compact size devices was presented. However there are significant challenges when developing a system with GaN, many of these disadvantages can be overcome by smart design of the PCB and proper selection and design of the gate driver. A multi-output gate drive or active gate drive provide a robust solution to dealing with the Miller current that may cause accidental turn on/ off as well as over voltage, and the utilization of a Kelvin connection is sufficient to reducing the shared inductance between the power loop and gate loop. It is also recommended that a digital isolator is used for both low and high side gate as this improves timing performance as well as CMTI. The design guidelines presented here are used for the gate driver selection and PCB design for the experimental prototype that is presented in Chapter 7.

Chapter 7

Simulation, Analysis, and Experimental Verification

7.1 Hardware Design

Previously there has been much discussion about the power loss mechanisms in Chapter 2, control scheme in Chapter 5 and the design considerations in Chapter 6. This chapter will focus on the hardware prototype design and verification. The CHFL-DAB prototype will be built for a home BESS application, according to [164] the power requirement should be 2 to 5 kW. The output voltage will be set to match the line to line of the north American household which is 240 V and the input power will be 48 V which is a common battery voltage for home applications.

Table 7.1: Hardware Prototype Specifications

Input Voltage	42V-56V, 48V nominal
Output Voltage	240V RMS
Power Rating	3kW

A CHFL-DAB prototype is designed and built to achieve the specifications in Table 7.1. The design is split into two parts based on the converters architecture, the low voltage input side will be referred to as the primary and the high voltage output side will be the secondary. The transformer that interfaces the primary and secondary is a planar transformer with an 8:1 turns ratio. The turns ratio is selected such that the operating condition is always in buck mode ($V_1 > V_2$), full designs details for the planar transformer can be found in [165].

In order to use the selected half-bridge GaN module a more modular structure of 4.2 has been developed for the purpose of prototyping. The secondary side of the experimental topology differs slightly from Fig. 4.2, which could be thought of as two interleaved full bridge converters similar to a series connection. In order to make the prototype modular the cycloconverter was decomposed into a positive DAB and a negative DAB. Four additional Si switches ($Q_5 - Q_8$) were included, as shown in 7.1. These switches physically decouple the two FBs present on the output side and is similar to a parallel connection. Both the series type topology in Fig. 4.2-b and the parallel type topology in Fig. 7.1 can be reduced to a single DAB during any half cycle. Thus, the analysis remains the same for this topology as it functions exactly the same as described in Chapter 5. The parallel type topology contains additional switches that operate at line frequency, the additional switching losses are negligible but the device count is higher. However, the increased device count allows for a more modular design and better loss distribution. The modified topology and experimental setup built to verify the function and control are shown in Fig. 7.1 and Fig. 7.2, respectively.

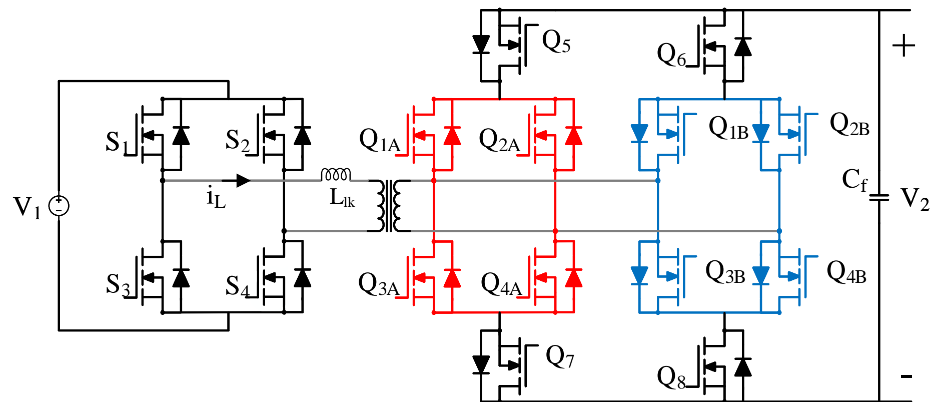


Figure 7.1: CHFL-DAB Experimental Topology.

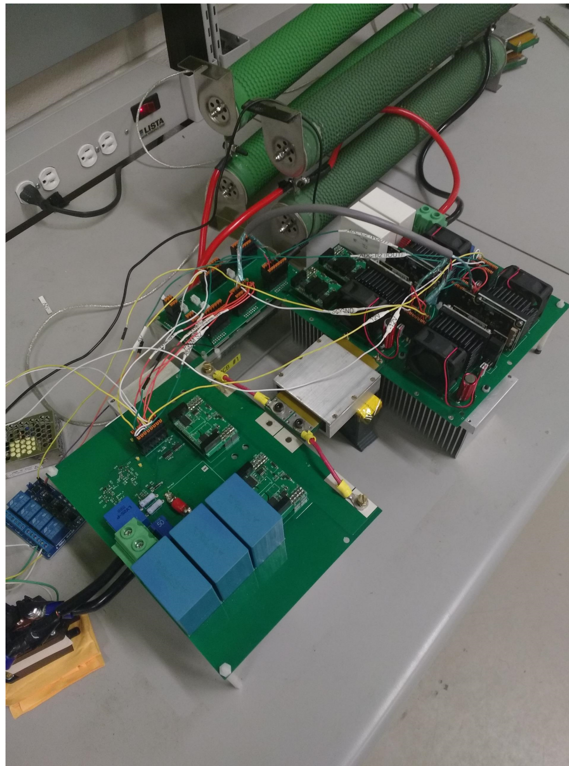


Figure 7.2: CHFL-DAB Experimental Set-up.

7.1.1 Primary Side

The primary side converter is composed of filter capacitors to absorb high frequency ripple and a full bridge converter to interface with the high frequency transformer.

The capacitance used can be determined based on the allowable voltage ripple, for this application ΔV was chosen to be approximately 1V which is 2% of V_1. In order to calculate the innput capacitance C_{in}, the equation relating total change in charge to the voltage ripple is used,

$$C_{in} = \frac{\Delta Q}{\Delta V} \tag{7.1}$$

where ΔQ is the total change in charge on the input capacitor during a charging or discharging cycle. The charge can be calculated by integrating the ripple current flowing into the capacitor, the leakage inductor current is made up of ripple supplied by the input capacitor and the average DC input current. The interval of charging or discharging can be determined from the backflow power discussed in Chapter 4.

$$I_{Cin} = i_L(t) - i_{DC}, \qquad \frac{\sigma}{2\pi f_s} < t < \frac{\alpha}{2\pi f_s} \tag{7.2a}$$

$$\Delta Q = \int_{\frac{\sigma}{2\pi f_s}}^{\frac{\alpha}{2\pi f_s}} I_{Cin} dt \tag{7.2b}$$

Utilising both (7.1) and (7.2) along with the given assumptions, the required input capacitance can be computed to be 250 μF. Based on device ratings and availability the three 100 μF capacitors were selected to be used in parallel.

The full bridge that interfaces with the transformer needs to be rated such that the switches can block the input voltage including any V_{ds} overshoot. Also, the switches should have low state on resistance because the primary side has much higher current. Based on the specifications, the switches need to block more than 60V and be able to handle peak currents around 200A with the RMS current being around 180A at peak operating conditions. Table 7.2 summarises the components and key parameters are

listed below:

Table 7.2: Primary Side Components.

Part name	Manufacturer	Part #
MOSFET	Infineon	IPP030N10N5
Input Capacitor	TDK	B32678G3107

The assembled primary side of the experimental set-up is show in Fig. 7.3:

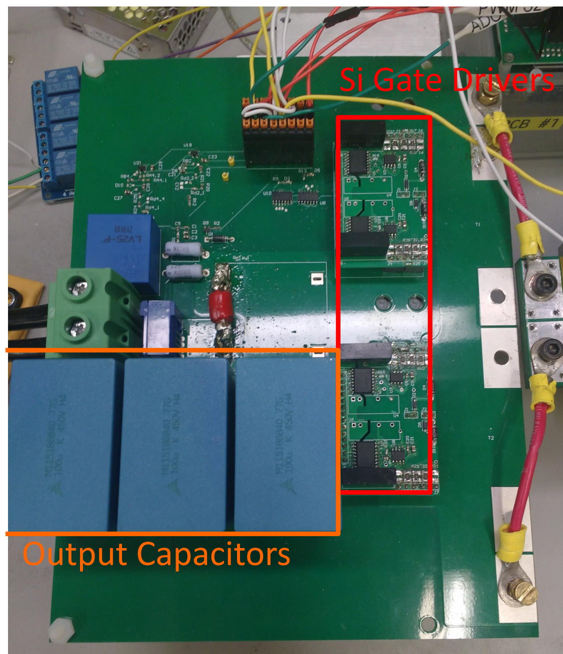


Figure 7.3: CHFL-DAB Experimental set-up Primary side

7.1.2 Secondary Side

The secondary side is composed of the external leakage inductor, cycloconverter and output filter capacitor, the assembled secondary side of the experimental set-up is show in Fig. 7.4. The external leakage inductor is used to trim up the leakage inductance of the transformer to the desired value, the equation for the maximum

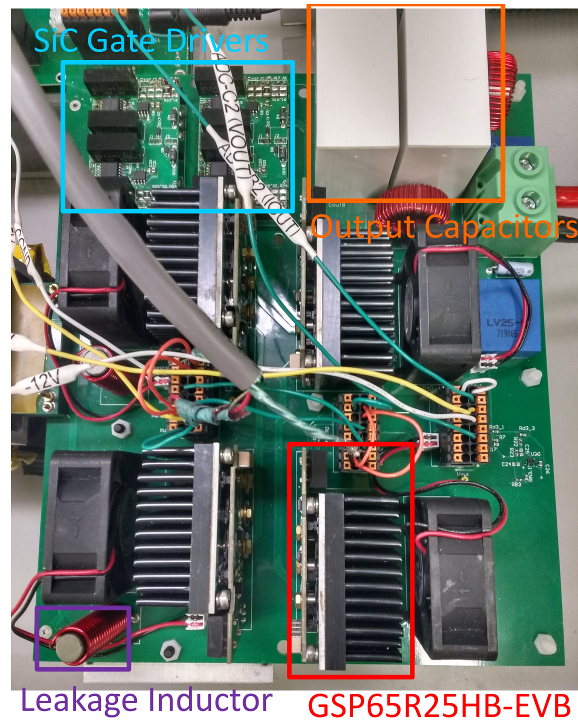


Figure 7.4: CHFL-DAB Experimental set-up secondary side.

value of L_{lk} was determined in Chapter 5. Using (5.1) and (5.4), the maximum total L_{lk} can be found to be 0.43 μH for the primary side, this value will be equal to 27.8 μH when referred to the secondary side. Thus, the external leakage inductance added in series with the transformer is 20 μH. The cycloconverter is a full bridge converter made up of AC switches. For the prototype the cycloconverter has been decoupled and decomposed into two seperate full bridges nested inside two half bridges. The half bridges are used to select which DAB will supply the output. The overall function of this converter is identical to the analysis presented in Chapter 4 and Chapter 5 with the main difference being the additional half bridges. In addition to the cycloconverter the output also needs a small capacitance to filter the high frequency ripple. In the lossless case the output capacitor C_{out} can be sized by referring C_{in} to the secondary

side as shown in (7.3).

$$\frac{n^2}{j\omega C_{in}} = \frac{1}{j\omega C_{out}} \tag{7.3a}$$

$$C_{out} = \frac{C_{in}}{n^2} \tag{7.3b}$$

It is important to note that if C_{in} was calculated with a very aggressive input voltage ripple than the value for C_{out} may result in worse performance during the half cycle transition point due to its longer discharging time.

Based on the design considerations discussed in Chapter 6, the GSP65R25HB-EVB module from GaN Systems as seen in Fig. 7.5 is selected to make up the decoupled DAB converters. C3M0065090D SiC MOSFET is selected for the additional switches $Q_5 to Q_8$ and are needed to determine which DAB converter is active. The GSP65R25HB-EVB module has been selected for several reasons:

- Chip-scale package with Kelvin source connection
- An Insulated Metal Substrate PCB (IMS PCB) is used to cool GaN Systems

Figure 7.5: GSP65R25HB-EVB

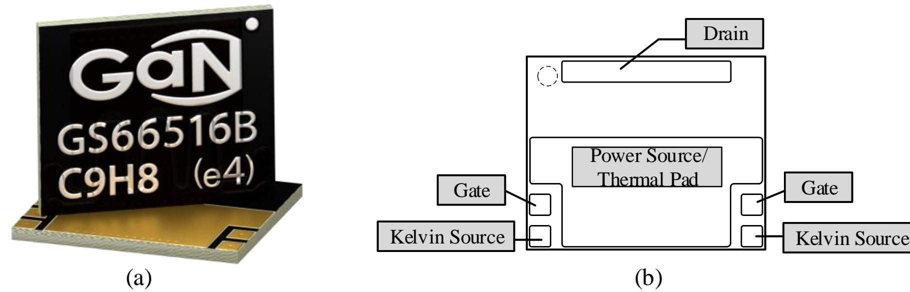


Figure 7.6: GS66516B GaNPX SMD Package, (a) GS66516B Package, (b) Footprint (view from top).

- Large power source/thermal pad for improved thermal dissipation
- Achieves high power density with its vertical design concept.

This module makes use of a low inductance surface mount package that is near chip-scale. In addition to this, the package also makes use of the Kelvin connection which is necessary to decouple the gate and power loops and is illustrated in Fig. 7.6. The typical through hole packaging such as TO-220 is not suitable for GaN because the long leads introduce large amounts of parasitics. These parasitics have large negative impacts on the switching behaviour through induced oscillations and voltage spikes as discussed in Chapter 6.

For the cooling requirements of GaN, an IMS PCB is used, the PCB contains a

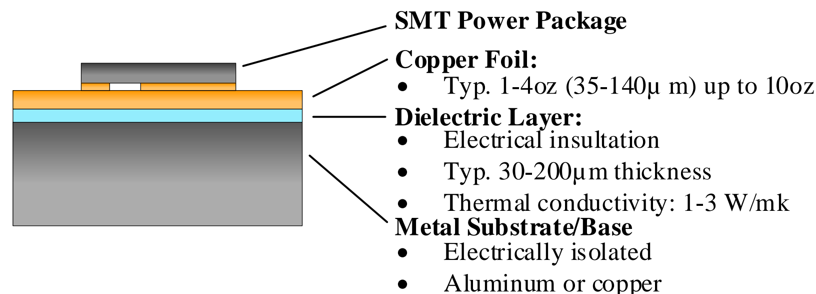


Figure 7.7: Cross-section view of a single layer IMS board

metal core such as aluminium to provide greater thermal conductivity when compared with the standard FR4 PCB (a cross section of a single layer IMS PCB is shown in Fig. 7.7).

The GSP65R25HB-EVB module includes the gate driving circuit which is mated to the IMS board via low pitch headers. The drive circuit is made up of a 12 V to 9 V power supply PS1, zener diode and a digital isolator. PS1 is combined with a zener diode to produce -3V and 6V references, the layout of this driver is shown in Fig. 7.8. The digital isolator Si8271 is from Silicon Labs, it has a separate on and off path allowing for customized gate resistance and combines low propagation delay with high CMTI immunity. The block diagram for Si8271 can be seen in Fig. 7.9 (Table. 6.1).

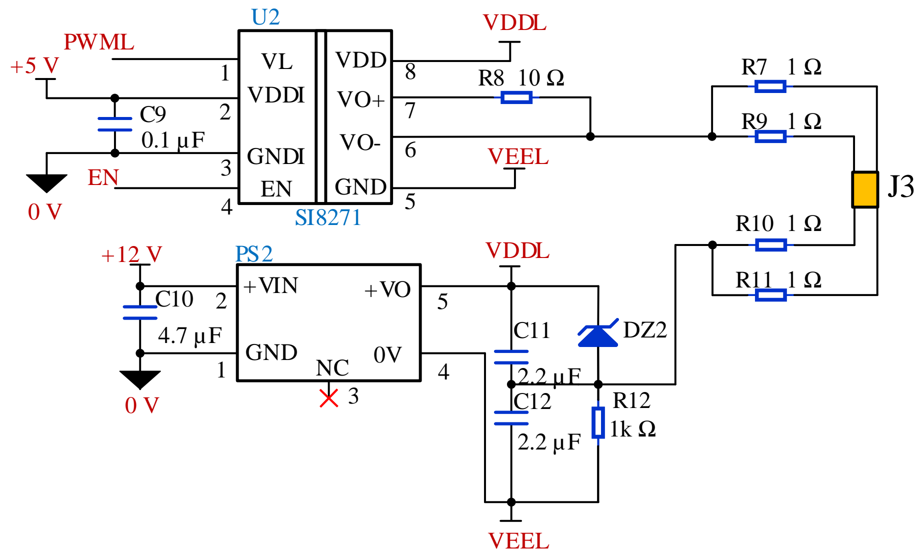


Figure 7.8: Gate driver circuit.

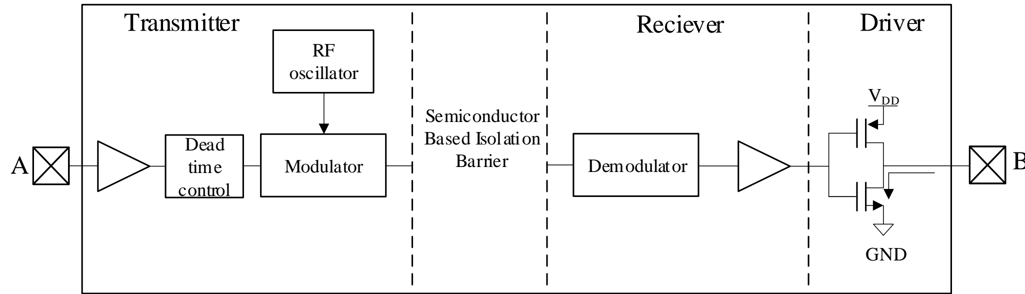
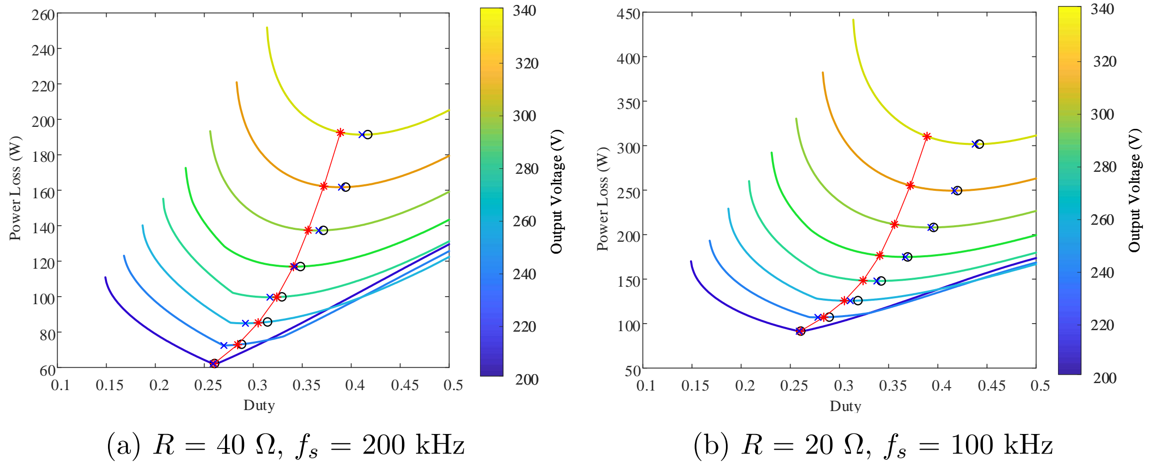


Figure 7.9: Digital isolator block diagram.

7.2 Simulation and Experimental Verification of Control

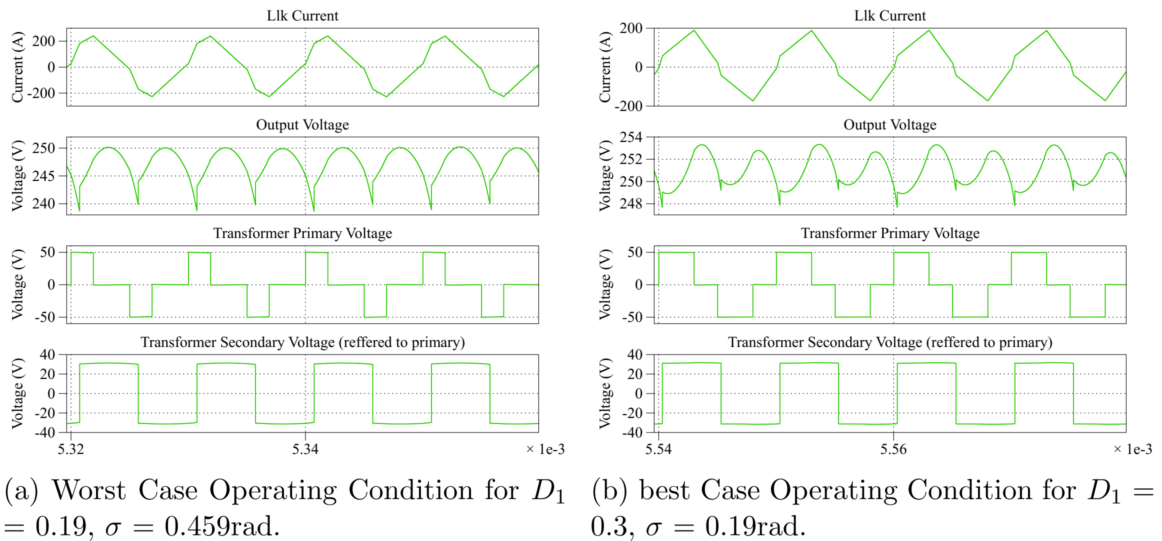
Chapter 5 discussed calculating the optimal operating condition for each quantized voltage step of the output AC voltage. To prove the effectiveness of the proposed calculation, all possible operating conditions are considered for each voltage step using the DPSM. Fig. 7.10 plots the simulated power loss against duty cycle with each curve representing a different output voltage, all curves use the same K value. The optimal condition for each voltage curve is denoted with an 'x' while the estimated point is an 'o', the accuracy depends on the weights calculated in (5.18) and (5.20). The overall difference between these two sets of operating conditions is about 1 watt. These operating points will be used to validate the simulation of a CHFL-DAB with a two-stage approach. To better illustrate the difference, the minimum loss condition is compared with the worst case condition at the nominal output voltage.

Fig. 7.11 shows the comparison between the best and worst cases for $V_1 = 48$ and $V_2 = 250$. In the worst case scenario (7.11a) the output voltage ripple is 11 V peak to peak, i_L RMS is 147.8A, i_L peak is 239.3A and the losses are 219 W. The best case scenario (7.11b) results in about 5 V peak to peak ripple of the output voltage, i_L



(a) $R = 40\ \Omega$, $f_s = 200$ kHz (b) $R = 20\ \Omega$, $f_s = 100$ kHz

Figure 7.10: Comparison of estimated minimal power loss 'o' with the minimum back-flow condition '*' and the absolute minimum 'x' for different output voltages.

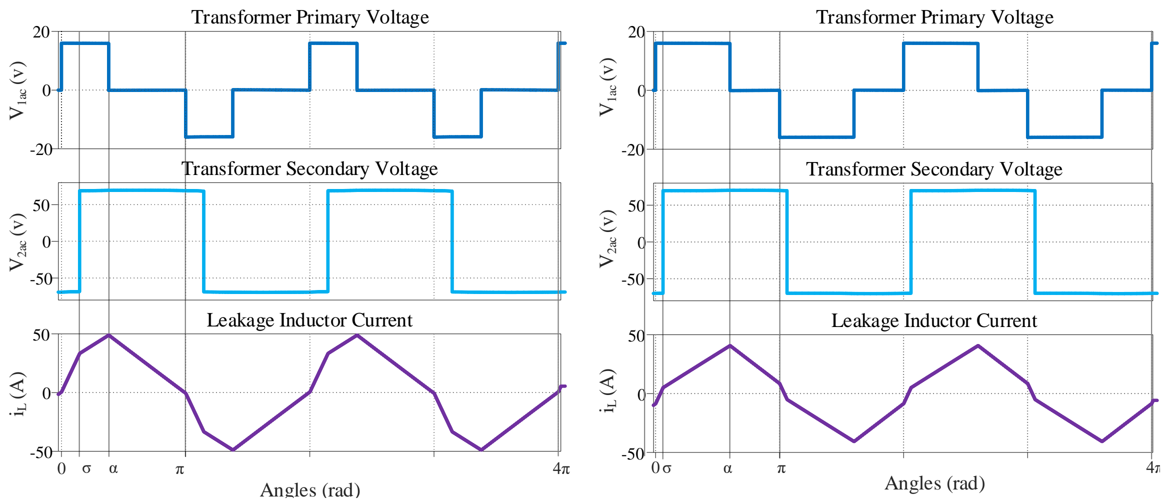


(a) Worst Case Operating Condition for $D_1 = 0.19$, $\sigma = 0.459$rad. (b) best Case Operating Condition for $D_1 = 0.3$, $\sigma = 0.19$rad.

Figure 7.11: Simulated worst and best case conditions for $V_2 = 250$.

RMS is 112.9A, i_L peak is 189.2A and the losses are 135.8 W. Thus, the comparison shows that the optimal operating condition has better performance metrics in every area compared with the worst case. If each quantized step is not carefully optimized then the converter performance could suffer.

The same optimal and worst case operating conditions are experimentally validated with a prototype converter, the experimental prototype is run with an input voltage of 16 V due to device limitations. The experimental conditions are also simulated to compare the waveforms and to illustrate the performance benefit of the optimal condition.



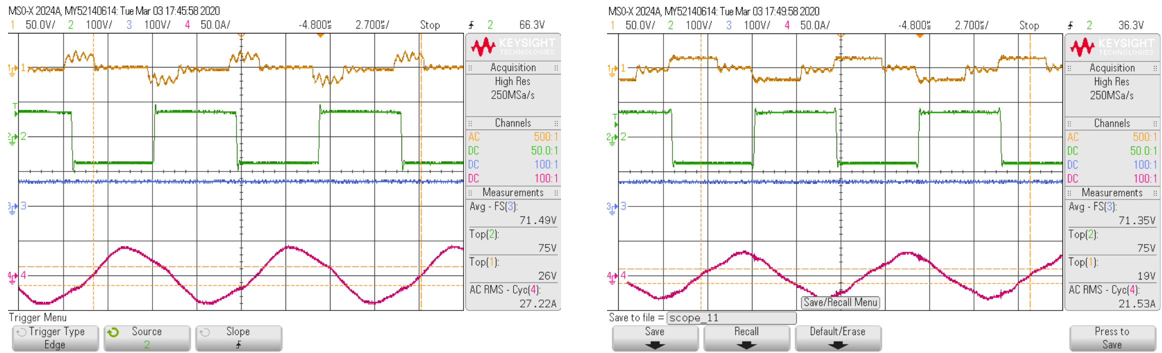
(a) Worst Case Operating Condition for D_1 = 0.19, σ = 0.459rad.

(b) best Case Operating Condition for D_1 = 0.3, σ = 0.19rad.

Figure 7.12: worst and best case conditions for $V_2 = 71$.

Fig. 7.12 repeats the simulation performed for Fig. 7.11 except the input voltage has been reduced to more closely represent the experimental validation. Fig 7.12b still shows significant improvement over 7.12a with significantly lower RMS and peak i_L. These trends are echoed in the experimental results depicted in Fig. 7.13 which closely match the simulated results. i_L is shown as the magenta curve and in the optimal case the peak and RMS values are significantly lower resulting in reduced power losses.

Table 7.3 summarizes the key characteristics of each simulation and experimental



(a) Worst Case Operating Condition for D_1 = 0.19, σ = 0.459rad.

(b) best Case Operating Condition for D_1 = 0.3, σ = 0.19rad.

Figure 7.13: Experimental Results for worst and best case operating conditions with V_2 = 75.

Table 7.3: Optimal Condition Comparison

Input Voltage (V)	Output Voltage (V)	Duty	σ (rad)	i_L RMS (A)	i_L peak (A)
Simulation Results(proposed method)					
48	245	0.19	0.459	147.8	239.3
48	250	0.3	0.19	112.9	189.2
17	70.5	0.19	0.459	29.9	46.5
17	71.5	0.3	0.19	24.8	38.6
Experimental Results					
20	71.5	0.19	0.459	27.2	38.5
18	71.35	0.3	0.19	21.53	30.5

test for a single operating point. Thus, by applying the optimal duty and phase shift for each desired output reference the total power loss and device stress are reduced. The experimental results show that for the same output power level the optimal conditions generate both a lower RMS leakage inductor current with a lower peak value, these contribute to overall lower switching and conducting losses.

7.3 Simulation and Experimental Verification of Converter Performance

The simulation and experimental results justify the proposed control scheme for the CHFL-DAB. However, the CHFL-DAB needs to be compared to the conventional two-stage approach to justify the converter topology. Two 3 kW DC/AC converters have been designed in PLECS, a single stage CHFL-DAB and a traditional two-stage DAB cascaded with an inverter. Both converters are designed with the same input and output ratings and are simulated using the parameters in Table. 7.4 with the loss information from the devices in Table. 7.5.

Table 7.4: Simulation Parameters.

Topology	$V_{in}(V)$	V_2 RMS (V)	L_{lk} (μH)	L_1 uH	C_f (μF)	L_2 (μH)
Inverter	400	240	-	50	2	10
DAB	48	400	0.9	-	4	-
CHFL-DAB	48	240	0.38	-	4	-

L_1 and L_2 represent the LCL filter at the inverter output, which is necessary to reduce the THD. This filter is not necessary for the DAB (DC output) or the CHFL-DAB. To simulate the losses, R_{dson} is used to calculate conduction losses and is scaled based on the junction temperature of the device provided by the datasheet. The R_{dson} for the GaN device also needs to be scaled with the I_{ds}. The t_r and t_f shown will give the reader an idea of how the switching losses compare to the conduction losses and can be used in (5.7) to calculate the weights $w_1 - w_4$.

The simulated output voltage, switching loss and conduction loss for the inverter and CHFL-DAB are shown in Fig. 7.14a and Fig. 7.14b, respectively. The average losses of the CHFL-DAB and the two-stage converter are summarized in Table. 7.6.

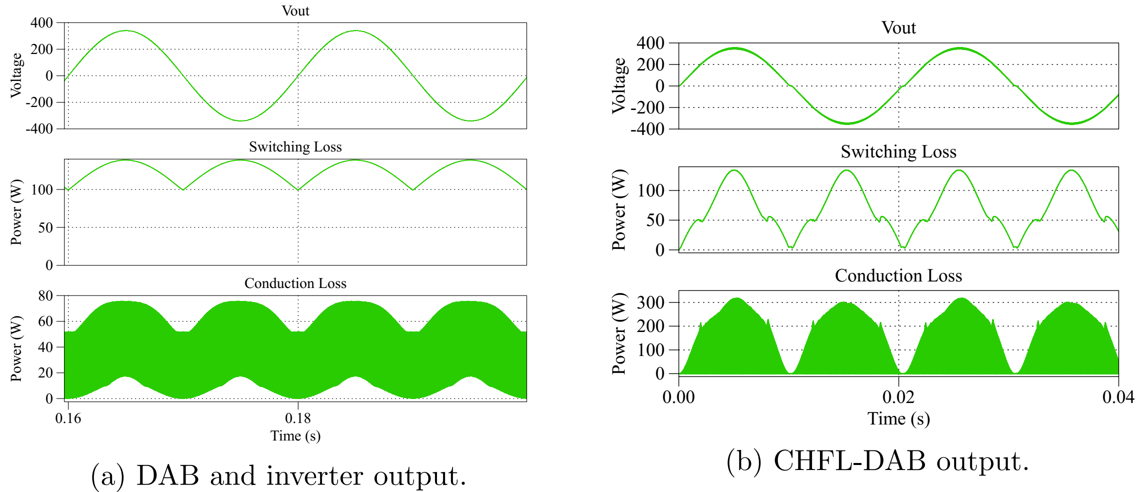
Table 7.5: Device Loss Information.

Device	Part Number	$R_{dson}(m\Omega)$	t_r (ns)	t_f (ns)
$S_1 - S_4$ (Si)	IPP030N10N5	3	15	17
$Q_5 - Q_8$ (Si)	IPW60R017C7	17	25	4
$Q_{1A} - Q_{4B}$ (GaN)	GS66516B	25	12.4	22

For a 3-kW load at 50 Hz with a switching frequency of 100 kHz, the total loss for the two-stage approach can be calculated by taking the sum of the inverter and DAB losses. The total losses of the two-stage approach is 173.4 W compared to the 144.2 W of the CHFL-DAB. The THD of the inverter output is about 0.3% while the CHFL-DAB is 5.4%. While the inverter does produce a cleaner signal but at the cost of including an LCL filter. The LCL filter requires two inductors which are not present to filter the CHFL-DAB output, these inductors contribute additional size and power loss. One particular thing to note about this implementation of the CHFL-DAB is that there is a small delay added when transitioning between the positive half-cycle and negative half-cycle. This delay is added to allow the output capacitor to discharge thus, preventing large current spikes but also results in slightly larger THD. It can be noted that the CHFL-DAB has a significant efficiency advantage resulting from the proposed control scheme achieving significantly lower switching loss which is outlined in Table 7.6.

Table 7.6: Simulated power losses.

<table>
<tr><th>Topology</th><th>Switching Device</th><th>Control</th><th>P_{sw} (W)</th><th>P_{cond} (W)</th><th>P_{total} (W)</th></tr>
<tr><td>DAB + Inverter</td><td>LV: Si
HV: GaN
Inverter: GaN</td><td>Power Loss
&
SPWM</td><td>124.2</td><td>49.3</td><td>173.5</td></tr>
<tr><td rowspan="2">CHFL-DAB</td><td rowspan="2">LV: Si
HV: GaN</td><td>Back-flow
Power</td><td>61.1</td><td>82.1</td><td>143.2</td></tr>
<tr><td>Proposed
method</td><td>62</td><td>77.5</td><td>139.5</td></tr>
</table>



(a) DAB and inverter output.

(b) CHFL-DAB output.

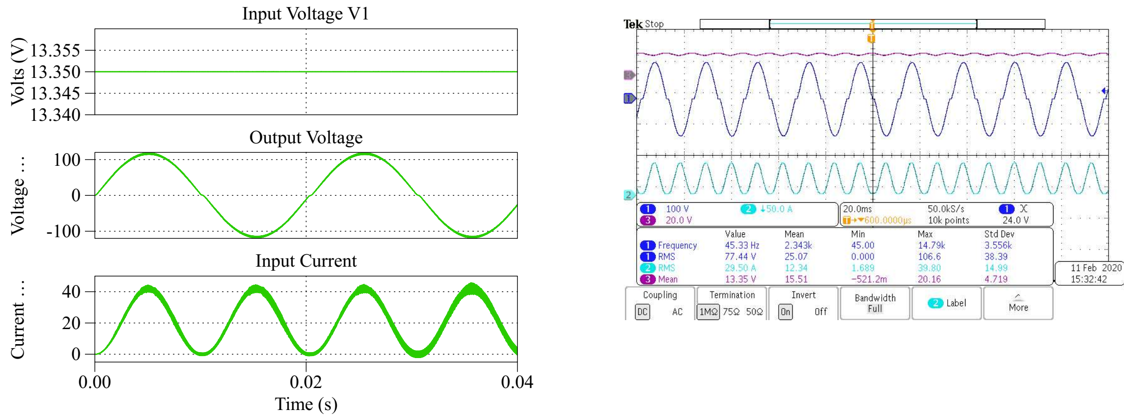
Figure 7.14: Simulation comparison of CHFL-DAB and two-stage approach.

In order to validate the comparison in Fig. 7.14, the proposed topology's behaviour and control scheme need to be proved. The built experimental prototype shown previously in 7.2 will be used to confirm the proposed control scheme and the behaviour. Table. 7.7 provides the specifications used for the comparison between the simulation result in Fig. 7.15a and the experimental results show in Fig. 7.15b.

Table 7.7: Experimental set-up specifications

Input Voltage	13.35 V
Output Load	25Ω
Switching Frequency	100 kHz

First, the simulation of the test conditions is performed to provide a reference point. Fig.7.15a shows the simulation result for an ideal CHFL-DAB converter, The Input current is 25.7 A RMS and V_{out} is 83 V RMS. Fig.7.15b is the test results from the experimental set-up under the same conditions as the simulation results. The input current is 29.5 A RMS and the output Voltage is 77.44 V RMS. The behaviour of the test setup closely matches the simulation results, however the small difference



(a) Simulation of CHFL-DAB for $V_1 = 13.35$ V.

(b) Experimental results of CHFL-DAB for $V_1 = 13.35$ V.

Figure 7.15: Comparison of experimental and simulation results for $V_1 = 13.35$ V.

in output voltage can be attributed to small differences in the experimental setup. Compared to the simulation model, the experimental setup differs in parameter values due to tolerances of components and unaccounted for parasitic components. The leakage inductor for example is made up of the external leakage inductance and the leakage inductance of the transformer. The transformer leakage inductance has been measured but some uncertainty remains in its value resulting in a small difference in output voltage. The input current is larger in practice due to the power loss in the form of conduction and switching losses and the transformer losses.

7.4 Summary

Overall The CHFL-DAB shows very promising results both in simulation and experimental results. The proposed control scheme has been validated and showed excellent improvement over the worst-case scenario. The performance of the CHFL-DAB was also acceptable as the total losses were decreased significantly while the behaviour of

the simulation and experiments was closely matching.

Chapter 8

Conclusion and Future Work

8.1 Conclusions

This thesis has presented an overview of the advantages to working with GaN tranistors and the accompanying design considerations for PCB and gate driver design. In addition to this the loss mechanisms are presented along with measurement techniques. The guidlines are used to develop a single-stage isolated DC/AC converter which shows promising improvements over the conventional two-stage approach and a control scheme for the optimal operating conditions is developed and validated.

Chapter 2 covers the loss mechanisms of GaN and illustrates how they differ slightly from other transistors such as silicon. The dynamic R_{dson} is studied and its impact on performance is presented.

Analysis and Measurement techniques for modelling and experimentally measuring GaN losses and the losses of converters are explored in Chapter 3. Several modelling methods include the analytical models, circuit simulation models and scaling

the manufacturers supplied data sheets to the desired operating conditions. Guidelines for probe selection and various pit-falls to avoid well taking measurements are also explored.

In Chapter 4 The dual active bridge converter is introduced as it is the building block for both the conventional two-stage approach and the presented CHFL-DAB topology. To set the stage for the CHFL-DAB first the analysis of controlling the DAB is required thus, the conventional SPS control is explored along with the more advanced duty and phase shift control. In addition to the DAB analysis the double-line frequency ripple problem is explored, this problem arises in the DAB from interfacing with an AC load.

Having introduced the DAB converter, Chapter 5 discusses the CHFL-DAB which is a single stage topology based around the DAB. The design of the CHFL-DAB utilizes the DAB control to produce quantized voltage levels approximating an AC waveform thus, each voltage level needs to be optimized. The technique and analysis for quickly and effectively calculating the optimal set of conditions is presented.

In order to design the converter to validate the control scheme, the design needs of GaN for both PCB and gate-drivers will be considered in Chapter 6. GaN operate extremly fast and this can allow any parasitics present in the circuit to cause issues. parasitics are present in all devices and circuits but usually slower voltage and current transitions such as those in silicon do not result in noticeable effects. In order to take full advantage of GaN the PCB layout and gate driver design need to be highly optimized.

Finally, Chapter 7 looks into the prototypes design including the devices selected

and the simulation results will be contrasted against the experimental results validating the proposed control and function of the CHFL-DAB.

8.2 Future Work

Further investigation of related research topics are provided:

- Explore the optimal input voltage rating for the rated output voltage and power. This may include investigation into using a larger input source or even a front-end boost converter type circuit. This may lead to overall lower device stress and increased efficiency

- Incorporate GaN into the low voltage side in order to reduce switching losses and move the system to a higher switching frequency which will allow for a smaller output filter capacitor and improve performance.

- Develop a hardware prototype for a two-stage approach so the efficiency comparisons can be experimentally validated.

- Develop control for the system to be grid-tied such as in the case with a BESS for PV applications.

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