Compact Low-Cost Ultra-Wideband Pulsed-Radar System

COMPACT LOW-COST ULTRA-WIDEBAND PULSED-RADAR SYSTEM

BY

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To my parents, sister and brother

Abstract

Recently, the advent of the integrated circuits (ICs), the monolithic microwave integrated circuits (MMICs) and the multiprocessing computer technology have provided numerous opportunities to make the radar technology compact and affordable. The ultra-wideband (UWB) technology gives many advantages over the traditional narrowband radar systems due to its high spatial resolution, low susceptibility to interference, superior penetration depths, and increased peak power. However, the ability to digitize and reconstruct the full UWB signal spectrum comes at a considerable cost and size. Ultimately, high-speed sampling rates above 10 giga-samples per second (GSPS) are beyond the abilities of conventional analog-to-digital converters (ADCs). The UWB technology is inaccessible to the end-user for various advanced applications in microwave imaging and detection. The purpose of this work is to provide a low-cost, dual-channel UWB pulsed-radar system that is readily available with a 1:10 system bandwidth. The advancements in low-cost alternatives for compact and portable designs empower many promising UWB applications. Here, the desired bandwidth is from 500 MHz to 5 GHz, which utilizes a fast pulse repetition frequency (PRF) in short-range applications. The preliminary results from the novel Equivalent-Time Sampling Receiver are promising with an equivalent-time sampling rate up to 20 GSPS. Nevertheless, the system design is versatile for bandwidth tuning in order to meet the needs of different applications. This versatility is enabled

by: i) selection of the effective sampling rate through the field-programmable gate array (FPGA) programming environment, ii) choice of the receivers' front-end track and hold (T & H) amplifier bandwidth, iii) a collection of different PRFs from the low kilohertz up to 20 MHz, iv) tuning of the pulse generator bandwidth, and v) simultaneous multi-channel capabilities enabling antenna beam-forming, polarization diversity and spatial diversity. The result is a fully functional prototype that costs a fraction of traditional bench-top solutions.

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List of Abbreviations

2D	Two dimensional
3D	Three dimensional
ADC	Analog-to-digital converter
ANSI	American National Standards Institute
ARM	Advanced RISC Machine
ASIC	Application-specific Integrated Circuit
AWG	Arbitrary waveform generator
AXI	Advanced Extensible Interface
BPF	Band-pass filter
BPSK	Binary phase shift keying
BVT	Bi-directional voltage translator
CC	Clock capable
CDC	Clock-Domain Crossing
CMOS	Complementary metal-oxide-semiconductor
CPU	Central processing unit
CW	Continuous wave
CWD	Concealed weapon detection
DAC	Digital-to-analog converter
dB	Decibel
DC	Direct current
DMAC	Direct Memory Access Controller
DDR	Double data rate
DSP	Digital signal processing
EM	Electromagnetic
ENOB	Effective number of bits
EIRP	Equivalent isotropically radiated power
ETR	Early-time response
FCC	Federal Communications Commission
FFT	Fast Fourier Transform
FIFO	First-In, First-Out
FM	Frequency modulated
FMC	FPGA magazine card

FPGA Field-Programmable Gate Array

GP General purpose

GPIO General purpose input output

GPR Ground penetrating radar

GSPS Giga-samples per second

HP High-performance

HDL Hardware descriptive language

I^2C Inter-integrated circuit

I/O Input/output

IC Integrated circuit

IF Intermediate frequency

IP Intellectual property

LDO Low-dropout

LO Local oscillator

LPC Low pin count

LPF Low-pass filter

LTR Late-time response

ITU International Telecommunication Union

LUTs Lookup tables

LVCMOS Low-voltage complementary metal-oxide semiconductor

LVDS Low voltage differential signaling

MIMO Multiple-input, multiple-output

MMIC Monolithic microwave integrated circuit

MSPS Mega-samples per second

NDT Non-destructive testing

OFDM Orthogonal frequency-division multiplexing

OOK On-off keying

OPM Orthogonal pulse modulation

PA Power amplifier

PAM Pulse amplitude modulation

PCB Printed circuit board

PDC Programmable delay chip

PDF Probability distribution function

PL Programmable Logic

PLL Phase-Locked Loop

PPM Pulse position modulation

PRF Pulse repetition frequency

PS Processing System

PSD Power spectrum density

PFN Pulse-forming network

RCS Radar cross-section

RF Radio frequency

RISC Reduced instruction set computing

RMS Root-Mean-Square

Rx Receiving

SAR	Synthetic Aperture Radar
SDR	Software defined radar
SERDES	Serializer/Deserializer
SFDR	Spurious free dynamic range
SINAD	Signal-to-noise-and-distortion ratio
SMA	Subminiature version A
SNR	Signal-to-noise ratio
SoC	System on a Chip
SPI	Serial peripheral interface
SPM	Signal processing module
SRD	Step recovery diode
TIE	Time-interval error
T & H	Track and hold
THD	Total harmonic distrotion
TTL	Transistor-transistor logic
Tx	Transmitting
UART	Universal asynchronous receiver/transmitter
USB	Universal Serial Bus
UWB	Ultra-wideband
VITA	VMEbus International Trade Association
VNA	Vector network analyzer

Chapter 1

Introduction

1.1 Background

The history of ultra-wideband (UWB) pulsed radar dates back to the first electromagnetic waves generated by Heinrich Hertz in 1887 [1–3]. The famous spark-gap experiments by the German physicist verified the propagation of electromagnetic waves, their polarization and reflection when interacting with metallic and dielectric objects [3,4]. However, the applications of Hertz's work would not introduce the radar system until the early twentieth century [5–8]. Radar is an acronym which stands for *RAdio Detection And Ranging*. By the mid-1930s, the first pulsed-radar system was demonstrated by Robert Watson-Watt in the United Kingdom and by the U.S. Army Signal Corps in the United States of America [9, 10]. The primary application of radars surged during the Second World War as the need for long-range marine and air military surveillance increased. Similarly, discoveries of radar systems began in Germany, the Soviet Union, France, Italy and Japan [9–11].

It was not until the 1960s, when UWB pulsed radar started to expand into civilian radar and communication applications [12,13]. Since then, the invention of integrated

circuits (ICs), monolithic microwave integrated circuits (MMICs), digital signal processing (DSP) and multiprocessing computer technology have opened numerous possibilities for new UWB radar applications. The Federal Communications Commission (FCC) in the United States has developed regulations for this growing technology in 2002 [14]. Similar regulations were introduced in Canada, Europe, Japan, and the International Telecommunication Union (ITU) [15–20]. Emerging technologies such as ground penetrating radar (GPR), non-destructive testing (NDT), through-the-wall imaging, surveillance, and medical imaging are now permitted to operate in the allocated UWB bands with some restrictions. These regulations set the frequency spectrum allocation, the emitted power spectrum density (PSD), and mitigation techniques for avoiding harmful interference [14, 17, 21].

The broad bandwidth of the UWB radar systems provides great frequency diversity leading to more information. This increase in information yields a better resolution, lower cross-ambiguities and increased recognition capabilities [13]. The use of frequency ranges within the low gigahertz domain offer reasonable penetration depths in opaque mediums in order to locate hidden objects. UWB signals are also less susceptible to interference and jamming due to their large operational bandwidths. However, a significant challenge faced by UWB radars is avoiding interference with the licensed communication frequency bands that overlap the UWB spectrum. Another challenge is the digitization of the broad range of spectral components within the UWB signals. The higher the frequency is, the faster the digitization must be to satisfy the Nyquist sampling criterion [22, 23]. The faster digitization requires a quicker and more expensive analog-to-digital converter (ADC). The UWB data acquisition now requires gigabit transceivers, strict timing considerations, and the careful design of gigahertz microwave interconnects. These complexities make these systems difficult to design and expensive to fabricate. To this day, UWB transmitters and

receivers are not available for purchase as off-the-shelf instruments. Their design and fabrication remain application-specific.

1.2 Motivation

Applications employing UWB systems have been emerging recently at an unprecedented rate [24–35]. The reason is due to the harmless non-ionizing radiation along with low-power emissions. These systems typically operate within the frequency ranges from the low megahertz to tens of gigahertz. However, the complexities behind the hardware implementation to generate and receive the broad spectrum pose challenges. Affordable and compact systems cannot be readily purchased and used with plug and play capabilities unlike much of the conventional wireless communication equipment. The goal here is to develop a system that has the flexibility and robustness to pave the way towards easy deployment of UWB radars. Specifically, the hardware developed is for a novel concealed weapon detection (CWD) surveillance system [36–38]. However, applications in GPR, NDT, through-the-wall imaging and medical diagnostics are also possible due to the shared bandwidth and performance requirements.

Current CWD systems such as walk-through detectors [39], X-ray and millimetre-wave full-body scanners [40], and portable scanners [41, 42] have very high purchase and operational costs, which means that they remain out of the public reach. Commercial systems have many drawbacks [43] resulting in high false positives due to sensitivity to innocuous objects such as belt buckles, keys and cell phones. They are obtrusive and require the presence of security personnel, thereby causing delays and inhibiting the flow of people in places of leisure and entertainment. In [38] presents a solution that enables unattended and unobtrusive surveillance. However, current

methods of implementation, such as the vector network analyzer (VNA) used in [36], do not meet the requirements for a compact covert surveillance system. Therefore, the motivation behind this research is the development of a novel compact, low-cost UWB radar system that meets the needs of the intended application. This development leads to a new generation of CWD technology, which defines the future of civilian CWD surveillance.

1.3 Contributions

The author has contributed to the development of a compact low-cost UWB pulsed-radar system in the following ways:

1. Conceived the high-level system requirements, component layout and design of the microwave interconnects [44–46].

2. Studied and analyzed the UWB pulse generator stability and performance in comparison to a laboratory-grade, multipurpose arbitrary waveform generator (AWG) [44, 45].

3. Designed and developed the hardware of the Equivalent-Time Sampling Receiver [46].

4. Designed and developed the field-programmable gate array (FPGA) firmware system for control of the UWB radar.

1.4 Outline of the Thesis

This thesis is intended to introduce the work achieved towards a novel compact low-cost UWB pulsed-radar system for short-range applications. It is based on the

initial work of McCombe *et al.* in [47–49].

Chapter 2 outlines the applications of UWB pulsed-radar systems in detection and imaging. The required system characteristics are discussed and the principles of the Equivalent-Time Sampling Theorem and the Nyquist Criterion are summarized. An overview discusses the current state-of-the-art UWB architectures and their challenges.

Chapter 3 introduces the proposed compact low-cost UWB pulsed-radar system. First, the design requirements for the system are defined. Presented is a system block diagram and a prototype system layout. An overview of the system operation is discussed along with the critical components that are required and their interconnects.

Chapter 4 takes a detailed look at the UWB transmitter module. The UWB pulse generator design principles and operation are presented. Reported is an analysis of the transmitter stability and performance in terms of signal jitter, noise and voltage.

Chapter 5 derives the receiver modules implementation. The Equivalent-Time Sampling Receiver hardware is presented and the principles used in the design are discussed. Shown are the challenges of the critical component choices and the interconnects between them. Outlined are the signal timing to trace length considerations and the fabricated printed circuit board (PCB) is presented.

Chapter 6 outlines the hardware descriptive language (HDL) and the software application running on the FPGA. The FPGA choice is justified and the programmable logic (PL) design that interfaces with the Equivalent-Time Sampling Receiver is explained. Next, the peripheral control using the bare-metal software application implemented on the built-in microprocessors are discussed. Finally, the preliminary results of a reconstructed UWB signal by the system are shown in comparison to a bench-top high-speed oscilloscope.

Chapter 7 provides a summary of the contributions of the work presented in this

thesis. Areas of improvement, not yet investigated, are suggested. Future work is discussed to continue the pursuit of an improved fast, portable and easily deployable system.

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Chapter 2

Background

This chapter discusses the theory and application of ultra-wideband (UWB) radars. It introduces the definitions used within the UWB community. The discrete-time and sampling theory is described, which is necessary to understand the work. Examples of various UWB radar system architectures and components are provided along with an overview of the emerging applications of the UWB radar.

2.1 Definitions for UWB Systems

This section lays out the terminology for an *ultra-wideband (UWB) Pulsed-Radar* system for *short-range* applications.

2.1.1 Definition of a UWB Device

The term *ultra-wideband (UWB)* device carries a special meaning within the engineering community [1–9]. A signal, radio or radar (i.e. a device) is classified as UWB if it meets all of the following criteria:

1. It has an absolute bandwidth, B_{abs}, which is larger than a defined minimum

bandwidth, B_{min},

$$B_{\text{abs}} \geq B_{\text{min}} \approx 500 \text{ MHz}. \tag{2.1}$$

The B_{min} value is set by the national regulating body and could range from 50 MHz to 500 MHz. However, most regulations state the B_{min} value as 500 MHz.

2. It has a fractional bandwidth, B_{f}, greater than 20%,

$$B_{\text{f}} \geq 0.20. \tag{2.2}$$

The fractional bandwidth is defined as

$$B_{\text{f}} = \frac{B}{f_{\text{c}}} = \frac{f_{\text{max}} - f_{\text{min}}}{f_{\text{c}}}, \tag{2.3}$$

where f_{min} and f_{max} are the minimum and maximum frequencies corresponding to a -10 dB threshold level from the maximum power spectrum density (PSD). The maximum PSD value does not necessarily correspond to the center frequency component. The center frequency is

$$f_{\text{c}} = \frac{f_{\text{max}} + f_{\text{min}}}{2}. \tag{2.4}$$

3. Its occupied bandwidth, B, is within the spectral range from 100 MHz to approximately 10 GHz

$$100 \text{ MHz} \leq B \leq 10.6 \text{ GHz}. \tag{2.5}$$

2.1.2 Definition of a Pulsed-Radar

Radar systems are used for detecting the presence of objects in a three dimensional (3D) space by emitting electromagnetic (EM) waves. The receiving antenna and the

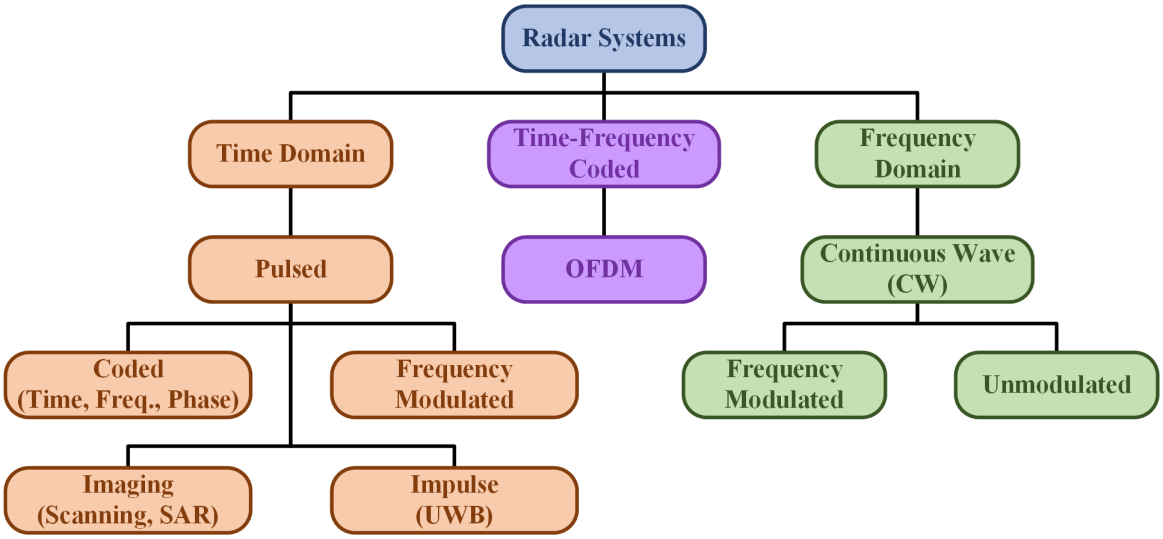
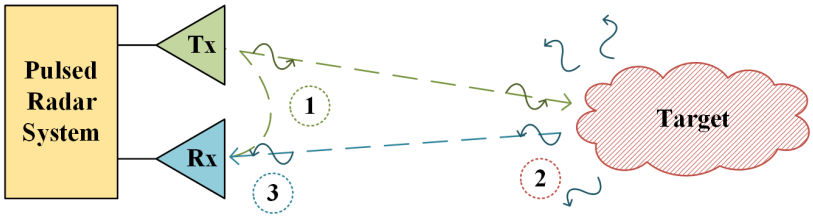


Figure 2.1: The types of radar classifications based on the emitted electromagnetic (EM) wave. The figure has been simplified from [10]. OFDM stands for orthogonal frequency-division multiplexing and SAR stands for Synthetic Aperture Radar.

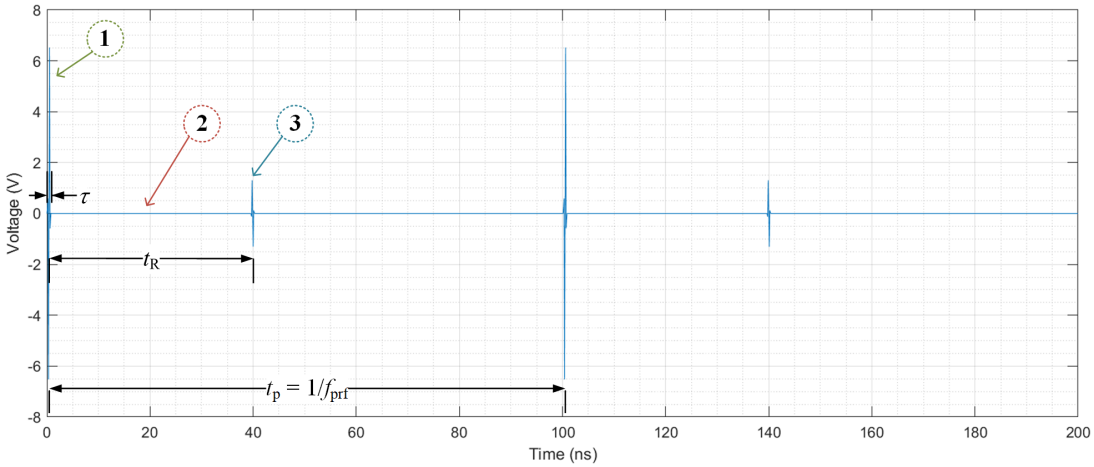
receiver collect the EM waves that are back-scattered from an object. Depending on the EM waveform, there are three types of radar systems: i) time-domain radars, ii) frequency-domain radars, and iii) time-frequency coded radars. Figure 2.1 presents a simplified radar-system classification tree from [10].

Time-domain systems are the traditional and most common radars based on the pulsed radar architectures. These systems work directly with time-domain signals where the emitted wave is a very short pulse. The radar then waits for a response from a target and during this time the transmitter is quiet. Many different pulsed radar systems exist and likely fall into one of the four categories: coded, frequency modulated (FM), imaging, and impulse radar. The category of particular interest is the impulse radar (Figure 2.2 shows an example). For this work, a pulsed radar refers specifically to the impulse radar category.

The other two types of radar systems do not relate to the work presented in this thesis. The frequency-domain systems use continuous wave (CW) radars. These



(a)



(b)

Figure 2.2: An ideal received signal from an impulse radar. (a) Signal interaction occurring in three stages: (1) the pulse radiated by the Tx antenna part of which is coupled to the Rx antenna; (2) scattering due to the presence of the target; (3) received back-scattered signal due to the target. (b) Received voltage versus time at the time of radiation, the time of interaction with the target, and the time of reception. τ is the transmitted pulse width. t_{R} is the time the signal takes to travel to and from the target. t_{p} is the pulse repetition period which is inversely proportional to the pulse repetition frequency (PRF), f_{prf}.

systems send continuously modulated or unmodulated tones (sinusoids) at specific frequencies. Time-frequency coded radars are new and emerging technologies pursued in the automotive sector [11]. It uses a signal that is coded in both time and frequency using communication-system coding methods. An example of such a coding scheme is the orthogonal frequency-division multiplexing (OFDM) [11].

2.1.3 Definition of Range and Limitations

The term *long-range* and *short-range* in radar applications are often found to be ambiguous. The terminology is typically specific to the application and can vary. *Long-range* applications involve a distance between the target and the radar, which is much greater than one of the following: i) the size of the target, ii) the size of the largest antenna dimension, or iii) the wavelength [12]. *Short-range* applications are at distances which are comparable or smaller than one of the three measures outlined above. For instance, within the emerging automotive radar sector, long-range radars operating at 76 GHz ($\lambda = 3.94$ mm) cover up to 200 meter; meanwhile, short-range radars are classified to have a range up to 30 meters [13].

Two factors limit the range of radar systems: i) the radar PRF in the unambiguous range equation, and ii) the signal-to-noise ratio (SNR) calculated from the radar range equation which defines the SNR as a function of the target radar cross-section (RCS), σ. These definitions and their respective equations are in [14–17].

The pulsed radar must avoid: i) ambiguities in resolving the distance to a target, and ii) interference between the target's echo and the signals coupled directly from the Tx antenna into the Rx antenna. The radar return from an object of interest must be received before the generation of a new pulse. There is a direct relationship between the period, t_{p}, between pulses and the expected maximum range of a target.

The frequency of the time period is defined as the pulse repetition frequency (PRF), f_{prf}. The unambiguous range, R_{un}, defines the maximum range to a target as

$$R_{\text{un}} = \frac{t_{\text{p}} c}{2} = \frac{c}{2 f_{\text{prf}}}, \tag{2.6}$$

where $t_{\text{p}} = 1/f_{\text{prf}}$ and c is the speed of light in a vacuum. The above formula holds for the case of monostatic radars, where the Tx and Rx antennas are co-located and the overall maximum unambiguous signal path is $2R_{\text{un}}$.

The second limitation on the range depends on the minimum SNR required by the radar receiver. The receiver must be able to detect the back-scattered signal, and therefore there exists a range limitation so that the received power is above a minimum SNR threshold. The standard far-zone radar range equation is

$$P_{\text{Rx}} = \frac{P_{\text{Tx}} G_{\text{Tx}} A_{\text{eff,Rx}} \sigma}{(4\pi)^2 R^4}, \tag{2.7}$$

with an effective area of the Rx antenna, $A_{\text{eff,Rx}}$, defined as

$$A_{\text{eff,Rx}} = \frac{\lambda^2 G_{\text{Rx}}}{4\pi}. \tag{2.8}$$

Substituting (2.8) into (2.7) yields the radar range equation in the form

$$P_{\text{Rx}} = \frac{P_{\text{Tx}} G_{\text{Tx}} G_{\text{Rx}} \lambda^2 \sigma}{(4\pi)^3 R^4}, \tag{2.9}$$

where

P_{Tx} = transmitted power, W P_{Rx} = received power, W

G_{Tx} = transmitting antenna gain G_{Rx} = receiving antenna gain

σ = mean RCS of the target, m^2 λ = the signal wavelength, m

R = the target range, m.

The minimum detectable signal power, $P_{\mathrm{Rx,min}}$, of a receiver is the weakest signal that can be detected. Rearranging (2.9) defines a maximum range, R_{max}, for a given minimum detectable signal power

$$R_{\mathrm{max}} = \sqrt[4]{\frac{P_{\mathrm{Tx}} G_{\mathrm{Tx}} G_{\mathrm{Rx}} \lambda^2 \sigma}{(4\pi)^3 P_{\mathrm{Rx,min}}}}. \tag{2.10}$$

The minimum SNR, $(SNR)_{\mathrm{min}}$, can then be defined by the minimum detectable signal power divided by the thermal noise power

$$(SNR)_{\mathrm{min}} = \frac{P_{\mathrm{Rx,min}}}{P_{\mathrm{n}}}. \tag{2.11}$$

The power of the thermal noise, P_{n}, is expressed as

$$P_{\mathrm{n}} = kT_{\mathrm{s}}B = kT_0F_{\mathrm{n}}B, \tag{2.12}$$

where

k = Boltzmann's constant (1.38×10^{-23})

T_{s} = system noise temperature ($T_{\mathrm{s}} = T_0F_{\mathrm{n}}$)

T_0 = standard (IEEE) temperature (290 K)

F_{n} = noise figure of the receiver (unitless)

B = instantaneous receiver bandwidth (Hz).

Substituting (2.12) into (2.11), rearranging for $P_{\mathrm{Rx,min}}$ and substituting into (2.10)

defines the maximum range with respects to the minimum SNR:

$$R_{\max} = \sqrt[4]{\frac{P_{\mathrm{Tx}} G_{\mathrm{Tx}} G_{\mathrm{Rx}} \lambda^2 \sigma}{(4\pi)^3 k T_0 F_{\mathrm{n}} B (SNR)_{\min}}}. \tag{2.13}$$

Within the work presented here, the range of the application is not intended to exceed 10 to 20 meters. The radar is classified as short-range according to the definitions and limitations above. The targets are of comparable size to the expected range but are typically larger than the wavelength and the antenna size. The physical limitations on the range of the system must also be kept in mind.

2.2 Discrete Time and the Sampling Theorem

The UWB radar signal is processed to determine if an object of interest is detected. Digital signal processing (DSP) applies numerous numerical methods and techniques for signal manipulation and feature extraction. However, to make use of DSP, the captured signal requires conversion into a discrete time signal. This process is called sampling. The challenge is to determine the sampling parameters accurately so that the sampled signal contains all the information carried by the original continuous-time signal. An explanation can be found in [16, 18] and is summarized here.

Sampling theory defines the relationship between a continuous-time signal, $x(t)$, and the discrete-time signal, $x[n]$. Here, the parentheses of the function x are used to denote a continuous-time signal whereas the square bracket notation is for a discrete-time signal. A discrete-time signal is said to be discrete if it takes only the discrete values $t = t_n$ of a continuous-time signal (such that $n = 0, \pm 1, \pm 2, ...$). It can be modelled by a multiplication between the continuous signal and an impulse train, $p(t)$, of Dirac delta, $\delta(t)$, functions, shifted in time by an interval (Δt_{s}). The impulse

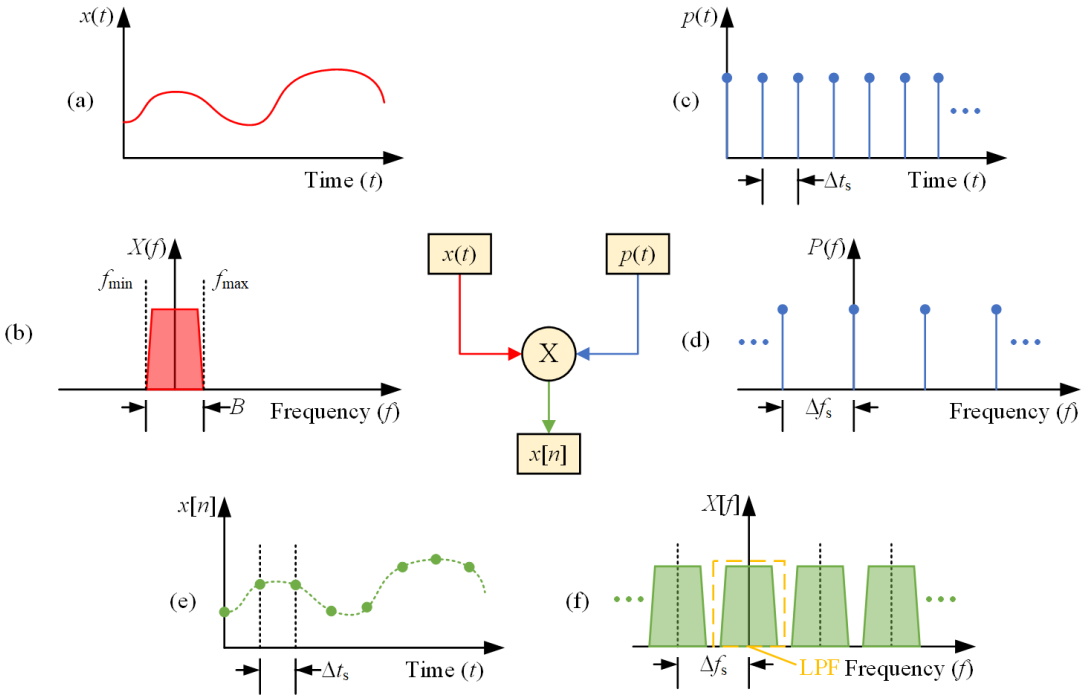


Figure 2.3: Sampling of a continuous time signal, $x(t)$. The temporal and spectral plots are shown respectively in (a) and (b) for the continuous signal, (c) and (d) for the impulse train $p(t)$, and (e) and (f) for the discrete time signal $x[n]$. LPF is the low-pass filter required for reconstruction of the continuous signal. The spectral plot of $X(f)$ does not accurately reflect the signal $x(t)$ and is used for explanation purposes only. Based on Figure 2.59 from [16].

train is

$$p(t) = \sum_{n=-\infty}^{\infty} \delta(t - n\Delta t_{\mathrm{s}}), \tag{2.14}$$

where the Dirac delta is defined by

$$\delta(t) = \begin{cases} 1, & t = 0 \\ 0, & t \neq 0. \end{cases} \tag{2.15}$$

The discrete signal, $x[n]$, for an idealized sampling process is then modelled as

$$\begin{aligned} x[n] &= x(t) \cdot p(t) \\ &= x(t) \sum_{n=-\infty}^{\infty} \delta(t - n\Delta t_{\mathrm{s}})|_{t=n\Delta t_{\mathrm{s}}} \\ &\approx \sum_{n=-\infty}^{\infty} x(n\Delta t_{\mathrm{s}}). \end{aligned} \tag{2.16}$$

The sequence $x[n]$ is now a discrete set of samples from the time-continuous signal, $x(t)$, when $t = n\Delta t_{\mathrm{s}}$. In other words, by definition

$$x[n] = x(t)|_{t=n\Delta t_{\mathrm{s}}} = x(n\Delta t_{\mathrm{s}}), \tag{2.17}$$

for any integer value of n [18].

The multiplication operation in the time domain presented in (2.16) results in a convolution operation in the spectral domain due to the Fourier transform property [18],

$$u(t) \cdot v(t) \longleftrightarrow \frac{1}{2\pi} U(\omega) * V(\omega) = U(f) * V(f). \tag{2.18}$$

The Fourier transform of the impulse train, $p(t)$, produces a frequency comb with spacing $f_{\mathrm{s}} = 1/(N_t t_{\mathrm{s}})$, where N_t is the number of time samples. As a result, the

Fourier transform of $x(t) \cdot p(t)$, yields a periodic spectrum of the original continuous-time spectrum at a sampling period of Δf_{s}. Figure 2.3 shows the sampling theory process based on a figure from [16].

To successfully reconstruct the continuous signal, $x(t)$, the periodic spectrum of the original signal should not overlap, which would cause aliasing. If the continuous signal has a spectral bandwidth B and a maximum frequency component $f_{\max}$ (refer to Figure 2.3), the sampling rate, f_{s} must then be greater than

$$f_{\mathrm{s}} \geq B \approx 2f_{\max}. \tag{2.19}$$

This allows for a low-pass filter with a cutoff frequency equal to $f_{\max} = f_{\mathrm{s}}/2$ to be used to convert the signal back to its analog form. According to the *sampling theorem* (often referred to as the Nyquist theorem, Shannon theorem, or Nyquist-Shannon theorem), the maximum spectral component of the time-continuous signal, $f_{\max}$, must have the following relationship with the sampling rate, f_{s}

$$f_{\mathrm{s}} \geq 2f_{\max}. \tag{2.20}$$

This is known as the *Nyquist Criterion* that must be met in order to maintain signal reconstruction. If $f_{\mathrm{s}} \leq 2f_{\max}$, overlapping in the spectral domain causes aliasing and the reconstruction of $x(t)$ from $x[n]$ is no longer accurate by using low-pass filtering.

2.3 Equivalent-Time Sampling Theory

Equivalent-time sampling is a technique that uses the repetitive nature of a signal to capture enough sample points at a slower rate in order to meet the Nyquist Criterion. It is also referred to as sub-sampling [16]. UWB pulsed radar bandwidths often

exceed the capabilities of standard data sampling equipment such as analog-to-digital converters (ADCs). These bandwidths operate well into the gigahertz frequency range and as presented in (2.20), the sampling rate of an ADC must be twice that of the highest frequency component. Current ADC technology is either widely available but cannot operate at the required sampling rates, or comes with extreme power efficiency issues and at a considerable cost. Finally, the data interfaces provide additional challenges in the implementation of gigabit speeds. These data interfaces are based on serializer/deserializer (SERDES) field-programmable gate array (FPGA) logic and more sophisticated interface protocols (i.e. JESD204B) [19].

Equivalent-time sampling is one approach to overcome these challenges. Data acquisition can spread over multiple pulses due to the repetitive nature of the pulsed radar. This reduces the sampling rate requirements but at the cost of an increase in acquisition time. The UWB community often uses this approach and it works as follows [16].

Step 1: The pulse is sub-sampled at an ADC sampling rate, $f_{\mathrm{s}} = 1/t_s$, for one pulse period. Here, t_{s}, is the period between individual ADC samples.

Step 2: The sampling point is shifted by a small time step, $\Delta t_{\mathrm{shift}}$.

Step 3: Steps 1 and 2 are repeated N times with a shift index $n = 0, 1, 2, ..., N-1$ until the sampled signal meets the Nyquist criterion. As a result, the equivalent time step is

$$t_{\mathrm{eq}} = t_{\mathrm{s}} - n\Delta t_{\mathrm{shift}}. \tag{2.21}$$

Here, $n\Delta t_{\mathrm{shift}}$ must be small enough to satisfy (2.20) that is re-written in

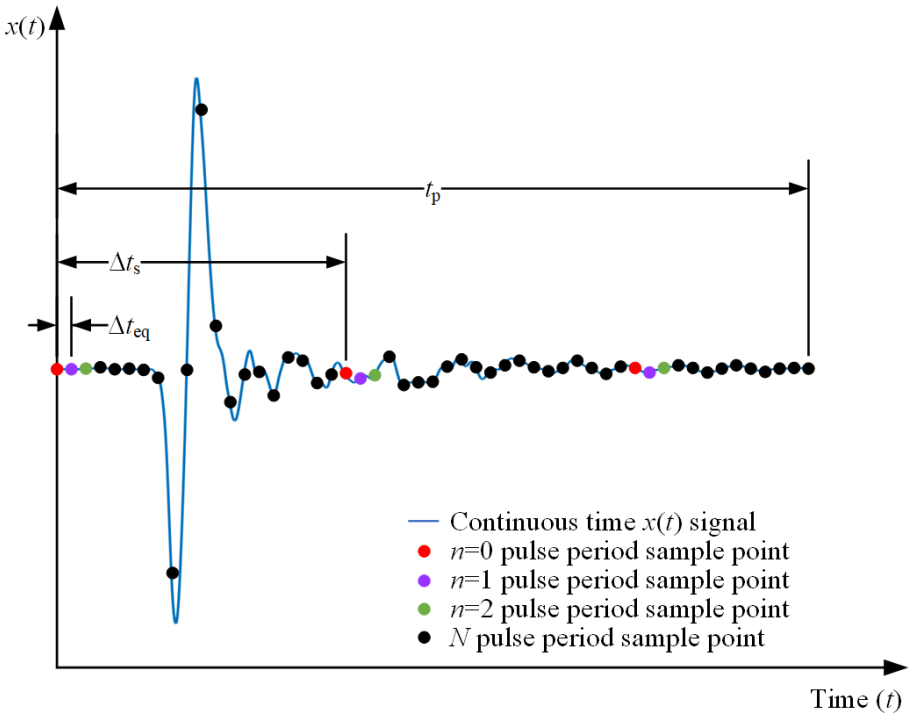


Figure 2.4: Equivalent-time sampling of a continuous signal, $x(t)$, with pulse repetition period of t_{p}, an ADC sampling rate of Δt_{s}, and an equivalent time sampling period of t_{eq} after N pulse periods.

terms of the equivalent-time sampling rate, f_{eq}:

$$f_{\mathrm{eq}} = \frac{1}{t_{\mathrm{eq}}} = \frac{1}{t_{\mathrm{s}} - n\Delta t_{\mathrm{shift}}} \geq 2f_{\mathrm{max}}, \tag{2.22}$$

where, f_{max} is the maximum UWB signal spectral component.

Figure 2.4 shows a continuous time signal, $x(t)$, being equivalently sampled in time.

2.4 UWB Architectures

The high-level block diagram behind a UWB radar system is shown in Figure 2.5. The transmitter and receiver modules are the main two hardware components of

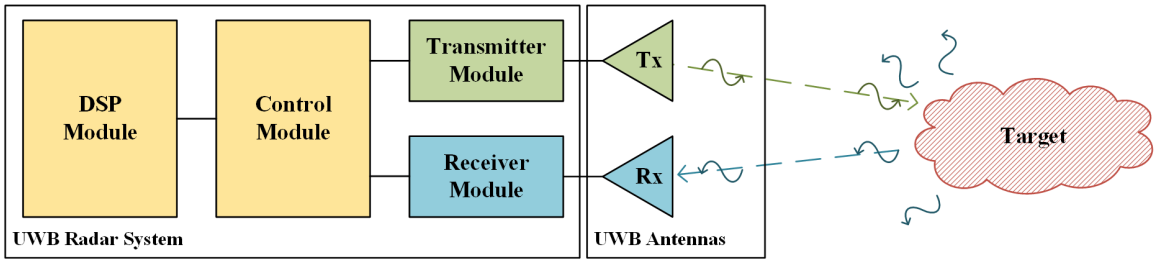


Figure 2.5: A high-level block diagram of a typical UWB radar system.

interest. The UWB antenna design is an interesting topic of its own and is not discussed here; for more information refer to [20–25].

2.4.1 UWB Transmitters and Pulse Shapes

The transmitter module generates a UWB signal which excites the spectral components of interest. Figure 2.6 shows the block diagrams of a narrowband (2.6a) and a UWB (2.6b) radar transmitters. UWB pulse generators are carrier-less, meaning they do not have a mixing stage like the traditional narrowband systems. This results in fewer radio frequency (RF) filters and components, simplifying the transmitter design and reducing the cost. On the other hand, the required RF components must also be able to support UWB signals. A trigger signal synchronizes the radar system to align pulse generation and reception. Special modulation schemes can be implemented such as pulse position modulation (PPM) and pulse amplitude modulation (PAM) with on-off keying (OOK), binary phase shift keying (BPSK) and orthogonal pulse modulation (OPM) [23]. Other ways of creating UWB signals include frequency chirp signals and frequency hopping [16].

There exist many different types of UWB pulses [6, 16, 23, 26]. The most common are the Gaussian pulse, one of its derivatives or a modulated Gaussian signal. The equations defined in [16] are presented below along with their temporal and spectral plots (see Figure 2.7). The numerical values presented in the Gaussian equations have

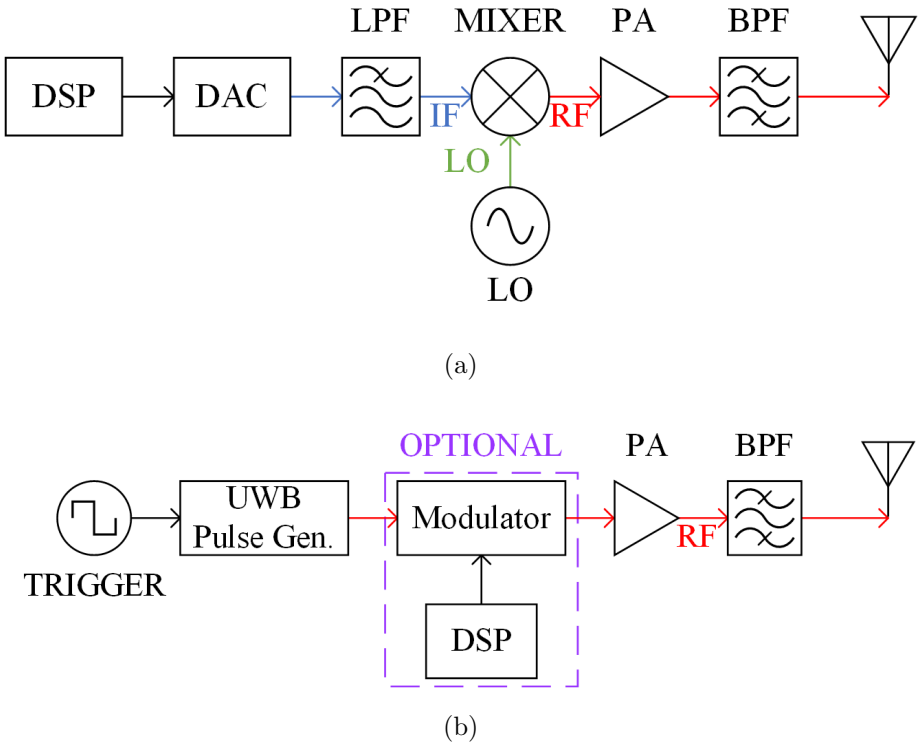


Figure 2.6: Block diagram of a typical (a) narrowband and (b) UWB radar transmitter. Abbreviations: BPF – band-pass filter, DAC – digital-to-analog converter, DSP – digital signal processing, IF – intermediate frequency, LO – local oscillator, LPF – low-pass filter, PA – power amplifier, RF – radio frequency.

truncation errors in practice caused by their truncation at a finite time.

Gaussian Pulse: The equation for a Gaussian pulse, $g(t)$, can be defined by

$$g(t) = Ve^{-\pi\left(\frac{t}{t_0}\right)^2}, \tag{2.23}$$

where V is an amplitude (scaling) quantity. The pulse width is characterized by

$$t_{\mathrm{w}} = 2t_0\sqrt{\frac{\ln 2}{\pi}} \approx 0.94t_0. \tag{2.24}$$

The bandwidth, B, corresponding to the -3 dB and -10 dB spectral strength is

defined by

$$B_{3\text{ dB}} = \frac{2\sqrt{\frac{\ln 2}{2\pi}}}{t_0} \approx \frac{0.664}{t_0}, \tag{2.25}$$

and

$$B_{10\text{ dB}} = \frac{2\sqrt{\frac{\ln 10}{2\pi}}}{t_0} \approx \frac{1.21}{t_0}. \tag{2.26}$$

As can be seen in Figure 2.7a that the Gaussian pulse consists of a large direct current (DC) component. This DC component cannot be radiated by the antennas resulting in significant efficiency issues. Thus, it is preferable to use one of the Gaussian derivatives as they do not have a DC component and therefore improve the pulse efficiency.

First Derivative: The first derivative of a Gaussian pulse is defined by

$$\dot{g}(t) = -\frac{2\pi V}{t_0}\frac{t}{t_0}e^{-\pi\left(\frac{t}{t_0}\right)^2}, \tag{2.27}$$

where the pulse width is defined by

$$t_{\text{w}} \approx 1.53 t_0. \tag{2.28}$$

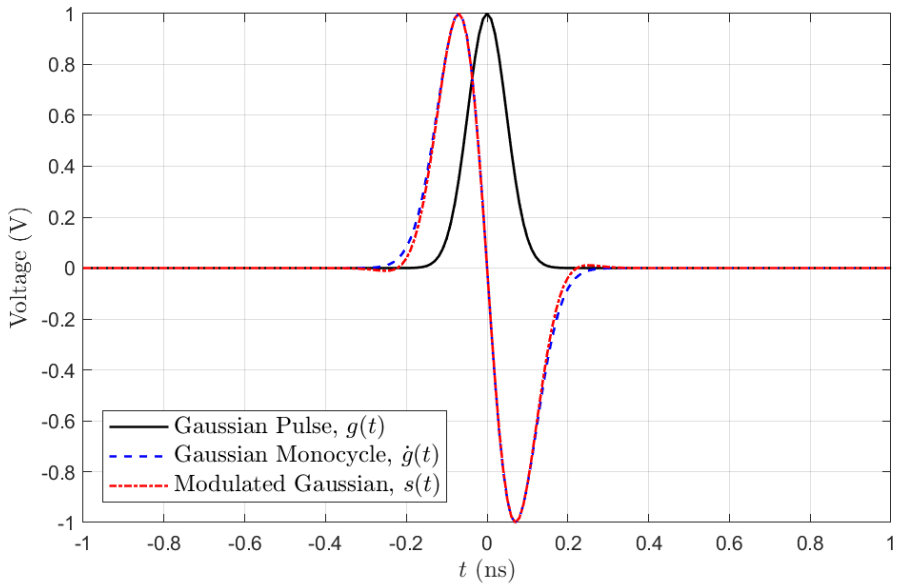
The first derivative of a Gaussian pulse is also referred to as a Gaussian monocycle or a differentiated Gaussian. The -3 dB and -10 dB bandwidths are defined as

$$B_{3\text{ dB}} \approx \frac{1.31}{t_0}, \tag{2.29}$$

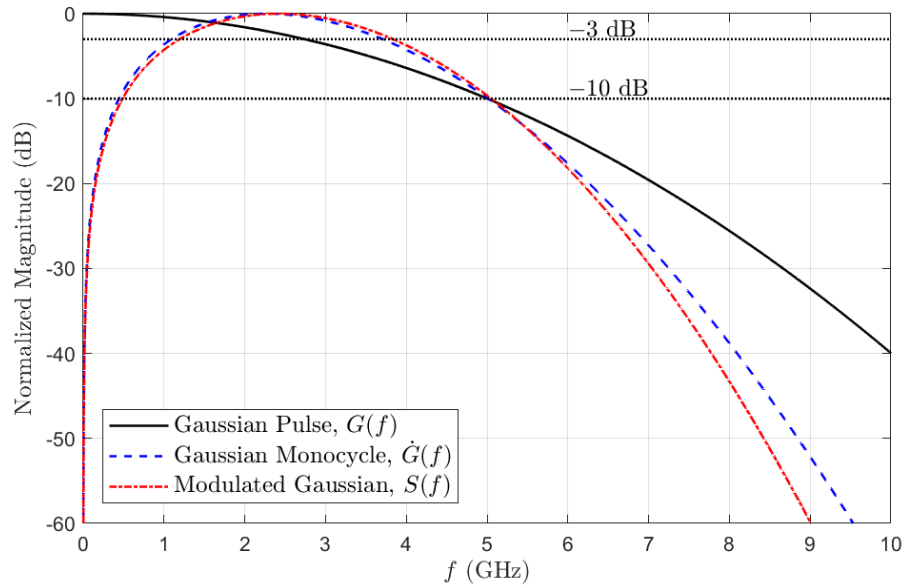
and

$$B_{10\text{ dB}} \approx \frac{1.76}{t_0}. \tag{2.30}$$

Higher-Order Derivatives: The 2nd order derivative of a Gaussian pulse is defined



(a)



(b)

Figure 2.7: A Gaussian pulse (black line), Gaussian monocycle (blue-dashed line) and modulated Gaussian (red-dashed-dot line) signals for a 500 MHz to 5 GHz bandwidth at -10 dB spectral strength when $V = 1$: (a) temporal domain and (b) spectral domain.

by

$$\ddot{g}(t) = -\frac{2\pi V}{t_0^2}\left[1 - 2\pi\left(\frac{t}{t_0}\right)^2\right] e^{-\pi\left(\frac{t}{t_0}\right)^2}. \tag{2.31}$$

This signal is sometimes referred to as a Gaussian droplet. The higher-order derivatives (3rd and 4th order) are available in [16]. These derivatives can improve the spectral efficiency of the pulse, which is critical for adhering to national regulations. However, this comes with added complexity in the RF design and at an increased cost.

Modulated Gaussian: As can be seen in (2.31), the complexity of the Gaussian signal increases as its derivative increases in order. An easy way of approximating the higher-order derivatives of a Gaussian pulse is through modulation with sine waves. An example of the equation for a modulated Gaussian is given by

$$s(t) = -g(t)\sin(2\pi f_c t). \tag{2.32}$$

In this case, a negative Gaussian pulse, $g(t)$, is multiplied by a sine wave with a carrier frequency of f_c so that the modulated signal approximates (2.27). This pulse can be seen in Figure 2.7 (red-dashed-dot line).

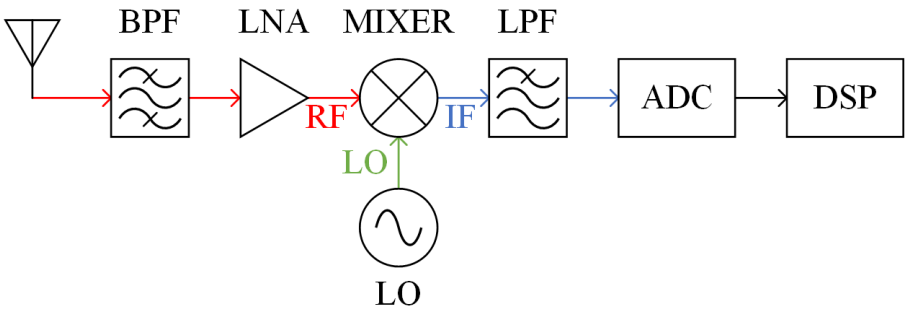
Many pulse generators have been proposed [27–37] which use analog circuitry with non-linear devices. These devices are tunnel diodes, avalanche diodes, step recovery diodes (SRDs) in conjunction with non-linear transmission lines. Tunnel diodes offer the fastest switching characteristics but at lower output voltages. Avalanche diodes provide a larger output voltage but offer slower switching characteristics. SRDs are a compromise between the two solutions. Non-linear transmission lines have their capacitance (or inductance) per unit length replaced by a voltage-dependent capacitance (or a current dependent inductance) to manipulate the propagation speed independent

from the signal amplitude [16]. This uses the pn-junction capacitance of a reverse-biased varactor diode. The alternative of mixing a UWB signal requires a wideband frequency mixer, similar to [38, 39], and a stable RF signal source. These increase the complexity and cost of the transmitter.

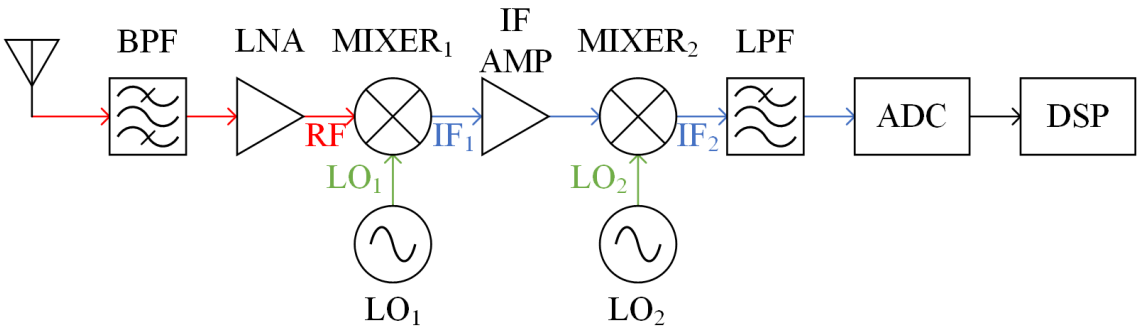
2.4.2 UWB Receivers

The receiver module is critical for capturing and digitizing a UWB signal of the back-scattered response of a target. Figure 2.8 shows the block diagram comparison of a narrowband heterodyne (2.8a), narrowband superheterodyne (2.8b) and a direct conversion UWB (2.8c) radar receiver. UWB receivers are a form of direct-conversion, sometimes referred to as homodyne or zero-intermediate frequency (IF) receivers, meaning they do not contain a mixing stage and the received signal is directly sampled. The design approach is to continuously sample at or above the Nyquist Criterion using a wideband ADC.

However, few ADCs exist on the market [40–47] that can directly sample in the giga-samples per second (GSPS) range. Table 2.1 is a summary of the commercially available ADCs from Texas Instruments, Analog Devices and a new emerging RF system on a chip (SoC) from Xilinx. These chips cost thousands of dollars and still cannot meet the sampling requirements for spectral bands beyond a couple of giga-hertz. Additionally, digital data offload requires very high-speed data communication buses and interconnects. The full-scale voltage is often limited to reduce the power consumption, which limits the dynamic range of an ADC. There are six common specifications for quantifying an ADC dynamic performance: signal-to-noise-and-distortion ratio (SINAD), effective number of bits (ENOB), signal-to-noise ratio (SNR), total harmonic distrotion (THD), THD plus noise (N), and spurious free



(a)



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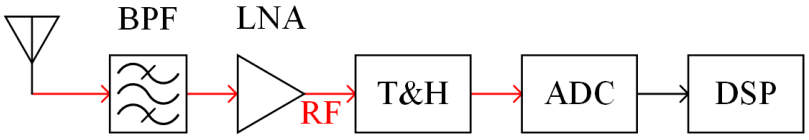

(c)

Figure 2.8: Block diagram of typical radar receiver architecture: (a) heterodyne, (b) superheterodyne, and (c) direct-conversion UWB radar receiver. Abbreviations: ADC – analog-to-digital converter, BPF – band-pass filter, DSP – digital signal processing, IF – intermediate frequency, LO – local oscillator, LPF – low-pass filter, RF – radio frequency, T & H – track and hold.

Table 2.1: Summary of select few commercially available giga-samples per second (GSPS) ADCs [40–47].

Manufacturer	Part Number	Sampling Rate	Bit Resolution	Full-Scale Input Voltage (Peak-to-Peak)	Availability
Texas Instruments	ADC12DL3200	6.4 GSPS (1x Channel) / 3.2 GSPS (2x Channel)	12-bit	0.8 V_{pp}	Active
Texas Instruments	ADC12J4000	4.0 GSPS (1x Channel)	12-bit	0.725 V_{pp}	Active
Texas Instruments	LM97600	5.0 GSPS (1x Channel) / 2.5 GSPS (2x Channel) / 1.25 GSPS (4x Channel)	7.6-bit	0.85 V_{pp}	Active
Analog Devices	AD9208	3.0 GSPS (2x Channel)	14-bit	1.7 V_{pp}	Active
Analog Devices	AD9689	2.6 GSPS (2x Channel)	14-bit	2.0 V_{pp}	Active
Analog Devices	HMCAD5831LP9BE	26 GSPS	3-bit	1.5 V_{pp}	Active
Analog Devices	AD9213	10.25 GSPS (1x Channel)	12-bit	1.4 V_{pp}	Pre-Release
Xilinx	UltraScale+ RFSoC (Gen 3.0)	5.0 GSPS (8x Channel)	14-bit	1.0 V_{pp}	Pre-Release

dynamic range (SFDR) [48]. The theoretical SNR of an ideal N-bit ADC is defined by

$$\text{SNR} = 6.02N + 1.76 \text{ dB}, \tag{2.33}$$

expressed in decibels (dB). In this work, the ADC must have a significant dynamic range to resolve the UWB signal. For example, to have an SNR of 98 dB, an ADC would require at least 16 bits. Keeping in mind that this is for an ideal ADC, the calculation for an actual ADC is closer to

$$\text{SINAD} = 6.02 \text{ ENOB} + 1.76 \text{ dB}, \tag{2.34}$$

where the ENOB is typically much lower than the actual bit resolution.

Many alternative sampling methods exist [16,23,26,49] that do not directly sample at the Nyquist rate. These methods include: i) random or sequential equivalent-time sampling [50, 51], ii) time-interleaved [52] or channelized ADCs [53], iii) alternative ADC topologies on the complementary metal-oxide-semiconductor (CMOS) and/or integrated circuit (IC) level [54], and iv) the synchronous time expansion method [26, 55, 56]. High-speed laboratory-grade oscilloscopes, such as [57–60], all implement a variety of these approaches. As a result, they are very costly, ranging into the tens, if not hundreds, of thousands of dollars. They are also bulky, making them impractical for the end-user.

2.5 UWB Detection and Imaging Applications

UWB systems have been growing at an unprecedented rate finding many applications in detection and imaging [16, 61–63]. Some of the well-known applications are listed below:

- **Ground penetrating radar (GPR)**: used in the detection of landmines, metals and objects close to the surface [49, 64, 65].
- **Non-destructive testing (NDT)**: civilian applications for inspection of building foundations, wires and pipes behind walls, roads and pavement, and tunnels [49].
- **Geology and archaeology**: Material and rock characterization as well as searching for buried structures, buildings and fossils.
- **Security and surveillance**: Detection of humans behind a wall using through-the-wall imaging [66], security checkpoints at the airports, convention centers and venues for concealed weapon detection [67, 68]
- **Microwave imaging**: Medical imaging and diagnostic test equipment [63, 69–73].
- **Automotive collision avoidance**: Adaptive cruise control [74], emergency brake assist, front cross traffic alert, pedestrian-detection, parking assist, rear cross traffic alert, blind spot detection, lane change assist, and pre-crash safety systems [13].
- **Search and rescue**: Detection of people under snow and debris following an avalanche or earthquake in a time of crisis.

2.6 Conclusions

This chapter has reviewed briefly the current state-of-the-art UWB radar technologies. The definition of a UWB pulsed-radar system for short-range applications

is provided. The required knowledge of the discrete-time signals and sampling theory is provided along with the introduction of the Nyquist criterion. An approach called equivalent-time sampling to overcome the high sampling rates required by the criterion is presented and discussed. The chapter also describes the state-of-the-art in UWB pulse shaping, transmitter components and receiver architectures. Moreover, the possible applications of such systems are summarized. It is important to note that the UWB technology and methods constitute a vast area of research with many unique architectures, techniques and applications. The major challenge of these techniques is the acquisition of the broad bandwidth at economical costs. Therefore, all advancements towards low-cost and compact UWB solutions benefit the engineering society. This is also the contribution of the work described in this thesis.

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Chapter 3

UWB Pulsed-Radar System Overview

3.1 Introduction

In this chapter, a novel ultra-wideband (UWB) pulsed-radar system is described. The system is built according to the design requirements for the intended concealed weapon detection (CWD) application [1–3]. However, possible customized features are also presented to open the hardware to other applications. The high-level system block diagram is developed and discussed, where each component role is defined. The goal is the development of a modular UWB radar system that can meet the needs of most UWB applications.

3.2 Design Requirements

The development of any UWB system is highly dependent on its application. The envisioned system here is intended for obtaining the late-time response (LTR) of a

target [4]. The LTR method is a non-imaging approach to target detection and therefore, does not generate images but responses in the form of signal waveforms. Highly complex digital signal processing (DSP) is required for detection and classification of a target [1,3]. However, other detection approaches used in different applications can be easily applied. It has an impact on the design requirements; however, with simple modifications, the proposed design can meet them. The design requirements have been first presented in [5] and they are updated, clarified and expanded upon here.

3.2.1 Frequency Bandwidth (500 MHz – 5 GHz)

The frequency band of interest is dependent on the target's size. A target's size affects the radar signal in two ways: i) it determines its intrinsic resonant frequencies, and ii) it changes its strength [2]. In the case of CWD, the objects of interest are weapons (e.g. handguns, rifles, knives, and grenades). Various handheld weapons have been found to hold their resonant signatures within the frequency range from 200 MHz to 5 GHz [2, 6, 7]. Therefore, the frequency bandwidth of the UWB radar system is chosen to be from 500 MHz to 5 GHz.

3.2.2 Pulse Width and Shape

Different types of pulse shapes exist, as previously discussed in Chapter 2. Each of these pulse shapes have advantages and disadvantages. The system should be able to change the pulse shape to meet the needs of different frequency content. This ensures that the transmitter module should be independent and interchangeable within the system design.

For the radar system developed here, a Gaussian monocycle pulse is chosen due to two key features: i) zero direct current (DC) component, and ii) easy spectrum

control. The frequency range of the system is from 500 MHz to 5 GHz resulting in a bandwidth of 4.5 GHz and the center frequency, f_c, based on (2.4), is 2.75 GHz. The bandwidth boundaries correspond to the standard UWB notation as the -10 dB level from the maximum power spectrum density (PSD).

The Gaussian monocycle pulse bandwidth can be defined by (2.30). However, it was found experimentally (using (2.30)) that to obtain the 500 MHz to 5 GHz bandwidth, $B_{10\text{ dB}}$ must be 10 GHz instead of 4.5 GHz. This is due to the fact that the bandwidths ($B_{3\text{ dB}}$ and $B_{10\text{ dB}}$) stated in [8] are relative to the standard Gaussian pulse bandwidth and not its derivatives. Re-arranging (2.30) for t_0,

$$t_0 = \frac{1.76}{B_{10\text{ dB}}} = \frac{1.76}{10 \times 10^9} = 176 \text{ ps}. \tag{3.1}$$

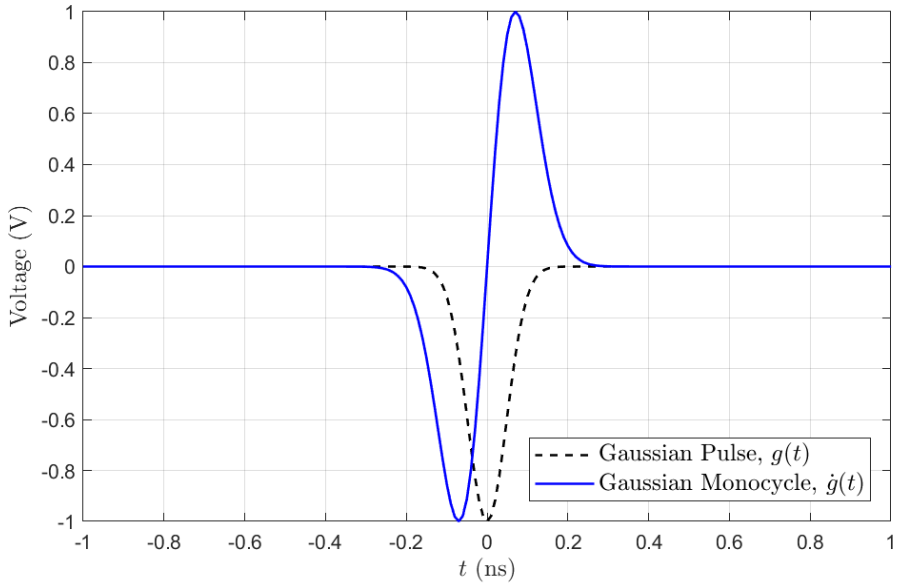
The desired Gaussian monocycle equation and pulse width can be defined, based on (2.27) and (2.28), respectively, as

$$\dot{g}(t) = -\frac{2\pi V t}{(176 \times 10^{-12})^2} e^{-\pi\left(\frac{t}{176\times10^{-12}}\right)^2}, \tag{3.2}$$

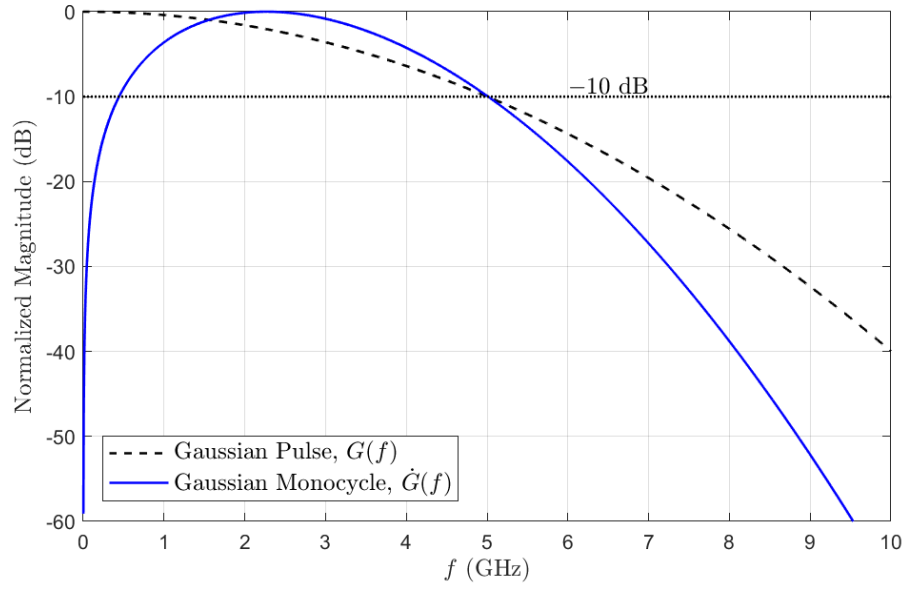
and

$$t_w = 1.53 t_0 = 1.53(176 \text{ ps}) = 269.28 \text{ ps}. \tag{3.3}$$

Here, V must be negative to account for the negative Gaussian pulse implemented in the hardware discussed in Chapter 4. The normalized temporal and spectral plots, based on the theoretical equation above can be seen in Figure 3.1.



(a)



(b)

Figure 3.1: Gaussian pulse (black-dashed line) and Gaussian monocycle (blue line) for a 500 MHz to 5 GHz bandwidth at −10 dB spectral strength such that $V = -1$: (a) temporal domain and (b) spectral domain.

3.2.3 Pulse Repetition Frequency (PRF)

The pulse repetition frequency (PRF) defines the interval at which a pulse is generated repetitively by the radar system. Short-range applications of UWB systems require a fast PRF (also referred to as a pulse repetition rate). The PRF is dependent on three key factors: i) the maximum unambiguous range based on (2.6), ii) the minimum time duration for the LTR responses to be captured, and iii) the regulations limiting the PSD emissions.

The maximum unambiguous range for the radar is expected to be 20 m. Using and re-arranging (2.6), the minimum period between pulses is

$$t_{\mathrm{p,min}} = \frac{2R_{\mathrm{un,max}}}{c} \approx \frac{2(20)}{3 \times 10^8} \approx 133.33 \text{ ns} \tag{3.4}$$

Therefore, the corresponding maximum PRF which removes target ambiguity is

$$f_{\mathrm{prf,max}} = \frac{1}{t_{\mathrm{p,min}}} = 7.5 \text{ MHz}. \tag{3.5}$$

The second condition is dependent on the LTR detection approach, and the PRF depends on the duration of the LTR region. Any back-scattered response of a target can be separated at time t_{L} into an early-time response (ETR) region and an LTR region as discussed in [4] and Chapter 3 of [9]. t_{L} is defined as twice the time required for the transmitted field to reach the object. In other words, it is the same as the unambiguous range such that

$$t_{\mathrm{L}} = \frac{2L}{c} \tag{3.6}$$

where L is the line of sight extent of the object and c is the speed of light in a vacuum [9]. The ETR region lasts until $t < t_{\mathrm{L}}$ and contains the impulse response of the incident wave due to the specular reflection and creeping waves. The LTR

occurs after $t > t_{\mathrm{L}}$ when standing waves are excited in the object. Therefore, the time required for the LTR region (t_{LTR}) must be added to the minimum period, $t_{\mathrm{p,min}}$ calculated in (3.4). This results in the minimum desired pulse period ($t_{\mathrm{p,desired}}$),

$$t_{\mathrm{p,desired}} = t_{\mathrm{p,min}} + t_{\mathrm{LTR}} \approx 133.33 \text{ ns} + t_{\mathrm{LTR}}. \tag{3.7}$$

The length of the LTR region can be system and deployment scenario dependent. At a minimum it is believed to be 12 ns ($6t_{\max}$, where $t_{\max} = 1/f_{\min} = 0.2$ ns). However, this has only been experimentally found and is not necessarily supported by the theory of Prony's Expansion along with the Fourier and Laplace transforms. A series of damped sinusoids/exponential signals can define the LTR region signal. Only one period is required to determine the frequency of a signal using the fast Fourier transforms but attenuating signals require additional periods to determine their attenuation rate. If the LTR region is too long, secondary reflections due to other objects in the field of view could mask the primary LTR with their ETR (i.e. the reflection of a wall behind the object of interest). Future research with the proposed system and the signal processing is required to determine a rigorous method for determining the LTR region length (t_{LTR}). At this time, an LTR length of 12 ns is used, therefore leading to a minimum desired period between pulses ($t_{\mathrm{p,desired}}$) to be 145.33 ns as per (3.7). The respective maximum PRF is 6.88 MHz.

The national regulating bodies, such as Industry Canada [10] and the Federal Communications Commission (FCC) [11] govern the UWB emission regulations. Limits are placed on the averaged and peak equivalent isotropically radiated power (EIRP) measured over a 1 MHz and 50 MHz resolution bandwidths. Spectrum analyzers are used to perform these measurements. The PRF of the pulse must take into account the dwell time for the measurement window. This is to ensure that the number of

pulses is limited in time relative to the resolution bandwidth (in the spectral domain) of a spectrum analyzer.

The averaged EIRP is the limiting factor as it is measured over a 1 MHz bandwidth with a dwell time of one millisecond or less [10]. This makes the averaged EIRP directly proportional to the PRF of the transmitter. A higher PRF leads to more captured pulses and as a result, a higher EIRP is obtained. Therefore, it is desirable to have a slower PRF guaranteeing a sufficiently low averaged power of the system. Preliminary results show that a PRF of 1 MHz is suitable.

The proposed system should have an easily tunable PRF from a few hundreds of kilohertz to 20 MHz to cover a wide variety of applications. The system is still in its prototyping stages and therefore, should have the ability to make easy adjustments. Having the choice of PRF allows the flexibility in meeting regulation while ensuring the desired unambiguous range and the LTR region duration. Further investigation into regulation testing of the system should be conducted to ensure the correct PRF for our application.

3.2.4 Receiver Sampling Rate

The sampling rate of the receiver is dependent on the Nyquist criterion as shown in (2.20). Since the maximum frequency component, $f_{\max}$, of interest is 5 GHz, the analog-to-digital converter (ADC) must be able to effectively sample at 10 giga-samples per second (GSPS)* or above. This sampling rate corresponds to a sampling period of 0.1 ns or smaller.

*A sampling rate of 10 GSPS is equivalent to sampling with a frequency of 10 GHz.

Table 3.1: Data acquisition window values for the worst case ($R = 0.5$ m) and the best case ($R = 20$ m) for a variety of walking and running velocities, v.

Human Velocity, v	Worst Case Time (ms)	Best Case Time (ms)
0.75 m/s	338.1	39,522.9
1.25 m/s	202.8	23,713.7
1.75 m/s	144.9	16,938.4
2.00 m/s	126.8	14,821.1
2.25 m/s	112.7	13,174.3
2.75 m/s	92.2	10,779.0
3.25 m/s	78.0	9,120.7

3.2.5 Data Acquisition Window

The data acquisition window is the time period in which the object of interest is located in the field of view of the radar. During this period, the object is illuminated by the incident wave and the back-scattered signal is received and processed. Two scenarios are of interest, namely, the worst and the best case for the ranges of $R = 0.5$ m and $R = 20$ m, respectively. Figure 3.2 shows in purple the acquisition region. An example of a moving target at a range distance of R is shown. This region is defined by the overlapping patterns of the transmitting (Tx) and receiving (Rx) antennas. The antenna radiation patterns are assumed to be triangular to simplify the calculation. Typically this is not the case in UWB antennas but can provide a reasonable estimate. The half-power beamwidth is denoted by θ and it determines the radar's field of view. This calculation uses the 74° E-plane half-power beamwidth of a UWB antipodal tapered slot antenna [12].

Assume that a target or an object travels perpendicular to the radar's boresight

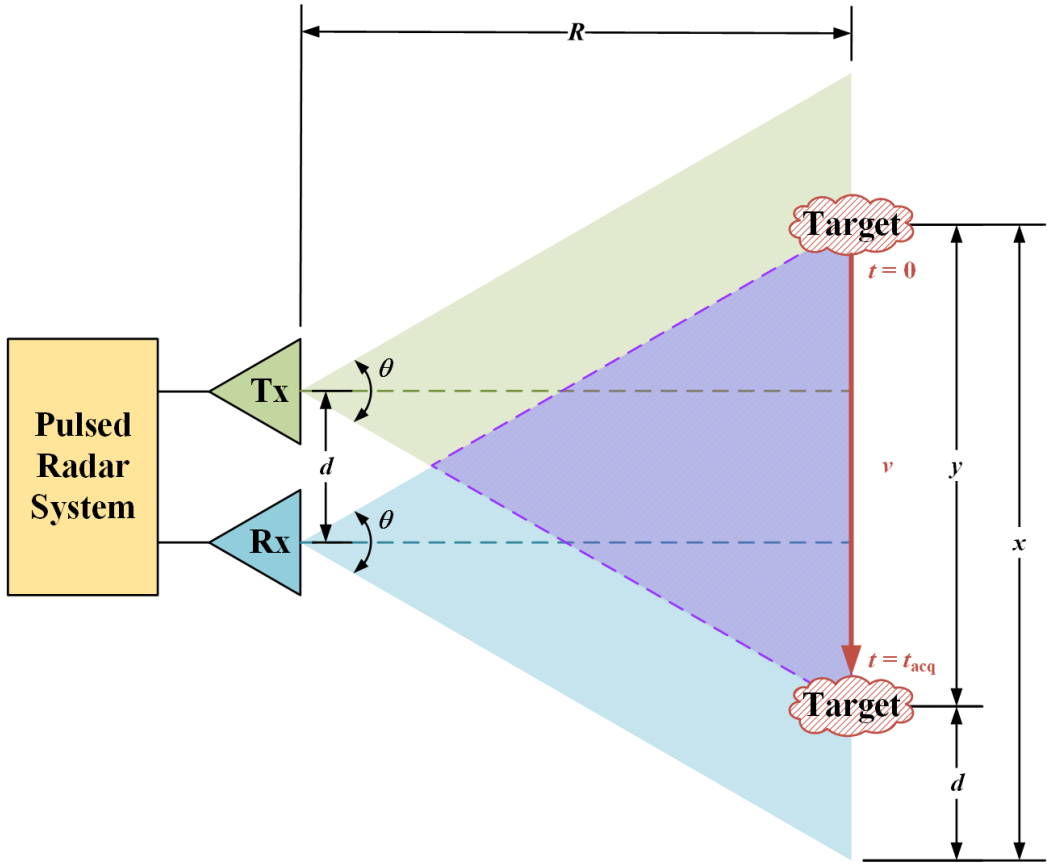


Figure 3.2: Data acquisition window diagram: The target acquisition window is shown in purple where the radiation pattern of the transmitting and receiving antenna overlap. The transmitting and receiving antennas of a pulsed-radar system are spaced d meters apart with an antenna half-power beamwidth of θ. A target is at a range of R meters and moves from $t = 0$ to $t = t_{\text{acq}}$ across a distance of y meters with a velocity of v in m/s.

with a velocity, v, from $t = 0$ to $t = t_{\text{acq}}$ across a distance of y while remaining at a constant range of R. The distance y can be determined by trigonometry to be

$$\begin{aligned} y &= x - d \\ y &= 2R\,\tan(\theta/2) - d. \end{aligned} \tag{3.8}$$

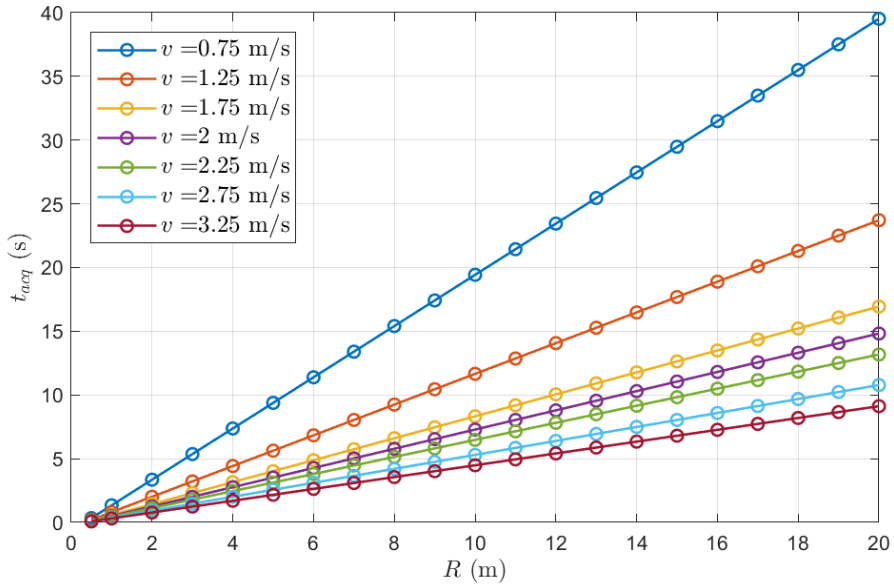


Figure 3.3: Data acquisition window values for ranges from 0.5 m to 20 m for a variety of walking and running velocities, v.

The available acquisition time of the system can now be defined by

$$t_{\text{acq}} = \frac{y}{v} = \frac{2R\tan(\theta/2) - d}{v}, \tag{3.9}$$

where y is in meters and v is in m/s.

Figure 3.3 shows the typical acquisition windows for human beings moving at multiple ranges, R. An average human is capable of walking at speeds in the range of 0.75 m/s to 2.0 m/s and running at speeds in the range of 2.0 m/s to 3.25 m/s [13]. The worst case is that of $R = 0.5$ m due to the short acquisition window, whereas the best case provides multiple seconds. Table 3.1 is a summary of the worst case and the best case acquisition times. It is shown that in the worst case, the radar would have anywhere from 78 ms to 338.1 ms to acquire a signature from the target. This sets a constraint on the speed of the data acquisition.

3.3 UWB Pulsed-Radar System

In essence, the UWB pulsed-radar system is an analog version of a software defined radar (SDR) with 1:10 bandwidth capabilities. Current SDR platforms are limited to narrow bandwidths up to 50 MHz. The importance of the UWB pulsed-radar system is the marrying of two state-of-the-art technologies: current field-programmable gate array (FPGA) technologies and advanced radar technologies. UWB radars are challenging to design and currently, no such commercial systems exist on the market. The proposed design aims at reducing the complexities and the design uncertainties associated with UWB development.

Figure 3.4 presents a high-level block diagram of the system developed here. It consists of two transmitting and two receiving ports. The hardware prototype is shown in Figure 3.5. These ports can be optionally connected to additional gain stages and then attached to their transmitting and receiving antennas. This two-channel system provides opportunities for polarization discrimination through co-polarization (V – V, H – H) and cross-polarization (V – H, H – V). Here, H denotes the horizontal polarization and V indicates the vertical polarization. The use of right-hand circular (RHC) and left-hand circular (LHC) antennas is also possible.

On the transmit side, a trigger generated within the FPGA travels through the receiver module to a single-ended, 50-Ω subminiature version A (SMA) connector. This SMA connector is then connected to the transmitter module. The trigger is a 5V-transistor-transistor logic (TTL) clock with a programmable PRF. The transmitter module is a UWB pulse generator based on step recovery diodes (SRDs) and non-linear transmission lines. The trigger is used to synchronize the UWB pulse between transmitting and receiving components. The transmitter module is further discussed in Chapter 4.

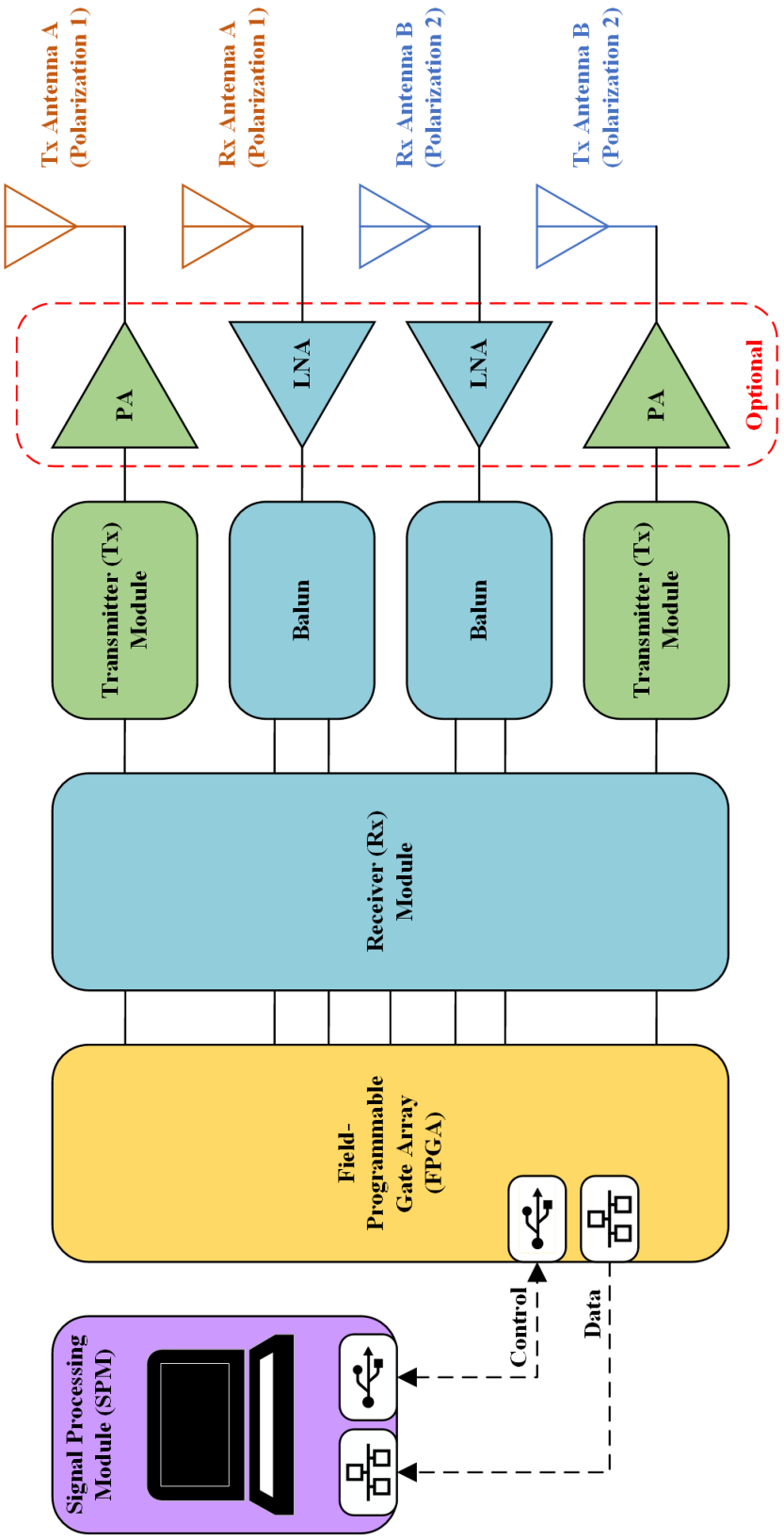


Figure 3.4: Block diagram of the proposed UWB pulsed-radar system.

On the receiver side (facing the receiving antenna), a single-ended 50-Ω impedance to a differential 100-Ω impedance balun is required to provide the correct input. The balun used is the BALH-0006 broadband balun from Marki-Microwave with a bandwidth from 200 kHz to 6 GHz [14]. The receiver module is an Equivalent-Time Sampling Receiver based on [15]. It consists of a single dual-channel 200 to 250 mega-samples per second (MSPS) ADC, two DC to 5 GHz bandwidth track and hold (T & H) amplifiers, a carefully timed clocking network and a programmable delay chip (PDC) with a programmable delay from 2.2 ns to 12.2 ns with 10 ps increments. The receiver module is further discussed in Chapter 5.

The FPGA controls the full radar system and the interfaces with the host personal computer which runs the signal processing module (SPM). The FPGA has three essential functions: i) triggering the transmitter module and synchronization of the transmitter with the receiver, ii) equivalent-time sampling control of the receiver module, and iii) configuring the control of the radar system, including data collection, saving and offloading. A Digilent Zedboard [16], which is an FPGA development board containing a Xilinx Zynq-7000 All Programmable System on a Chip (SoC) [17], is used. Universal asynchronous receiver/transmitter (UART) communication is used for system control. The waveform data packets are sent via Ethernet communication. More on the FPGA control is discussed in Chapter 6.

The SPM reconstructs the sampled waveforms and provides the detection algorithms. These algorithms could use the LTR approach for CWD detection or any other DSP for a UWB application. The SPM module is not the subject of this work.

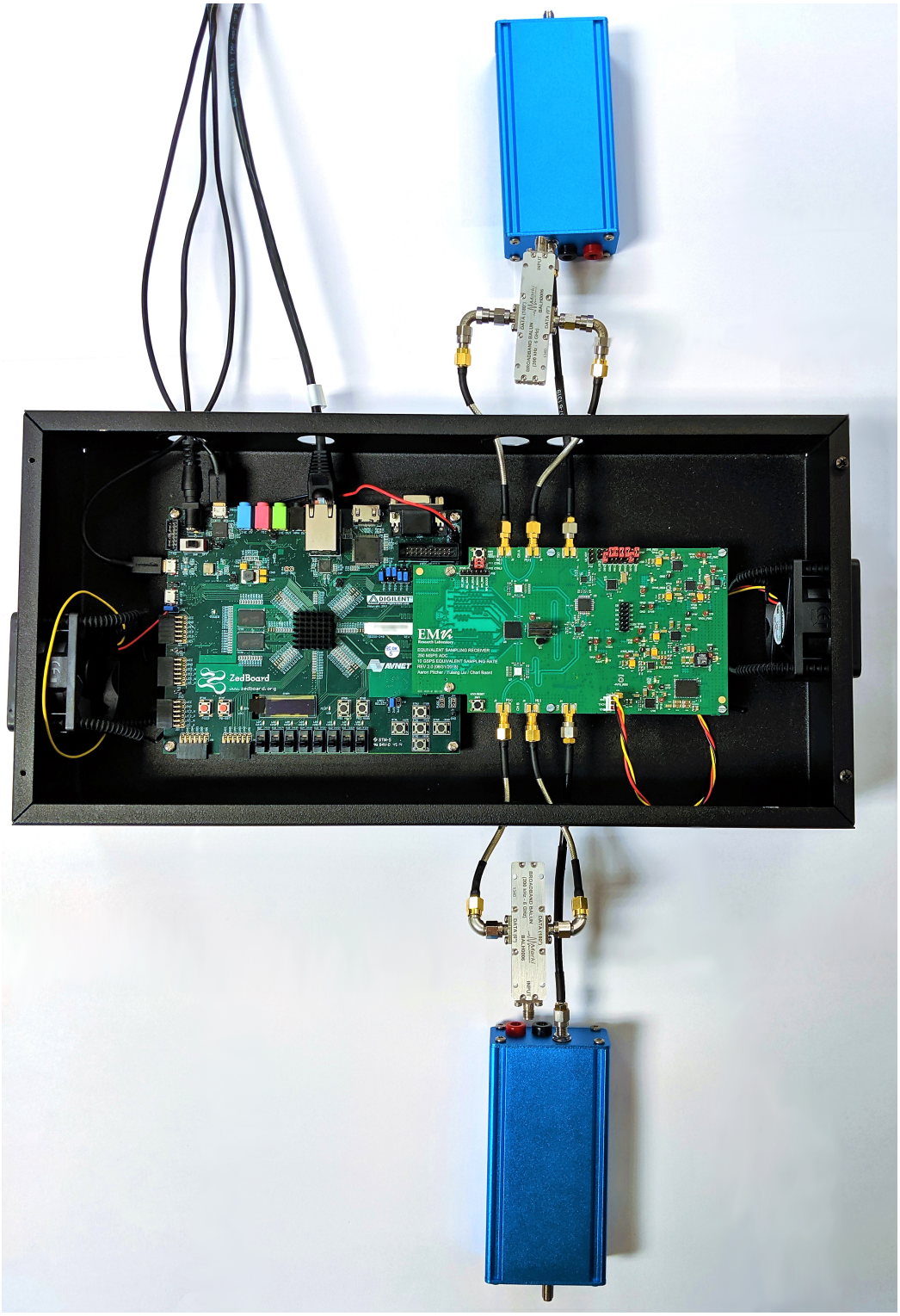


Figure 3.5: Physical hardware of the UWB pulsed-radar system prototype.

3.4 Conclusions

The proposed low-cost compact UWB pulsed-radar system has been presented at a high level. This 1:10 bandwidth UWB radar system is versatile and adaptive so that it can meet the needs of any UWB application. The design requirements have been stated and explained. The design is intended to use a Gaussian monocycle pulse to excite the 500 MHz to 5 GHz spectrum. However, other spectrums can be achieved by adequately replacing the transmitting module and re-tuning the receiver module. The roles of the system's four principal components (transmitter module, receiver module, FPGA and SPM) have been explained along with a high-level description of their architecture and main components.

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Chapter 4

UWB Pulse Generator Design and Analysis

4.1 Introduction

The transmitter is a critical component of the ultra-wideband (UWB) pulsed radar. This chapter describes the envisioned UWB pulse generator integrated into the transmitter module. Various generators have been proposed in the literature [1–10] that produce a pulse of UWB spectrum within the allocated frequency band from 3.1 GHz to 10.6 GHz. The generator developed here is based on the circuits first proposed in [4]. Similar designs have also been proposed in [5–7]. An overview of the design is first provided, followed by its measurements and analysis of the jitter and noise performance. These metrics are used to compare our UWB generator with a similar UWB pulse generation using a high-performance, laboratory-grade bench-top arbitrary waveform generator (AWG). Note that several portions of this chapter are taken *verbatim* from the author's work in [11] and [12].

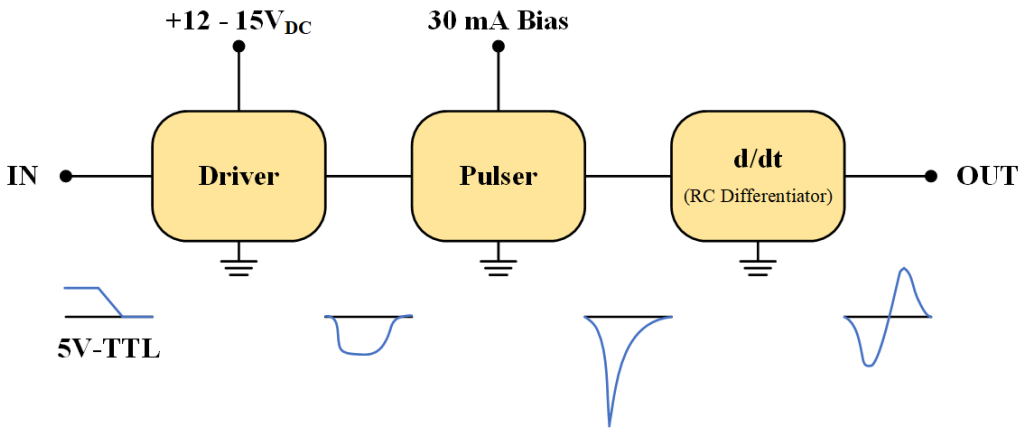


Figure 4.1: Block diagram of the UWB pulse generator.

4.2 UWB Pulse Generator Design

The pulse generator proposed in [4] is divided into three stages: i) the driver circuit which conditions the input transistor-transistor logic (TTL) signal, ii) the pulser circuit which sharpens the driver-circuit output using a non-linear transmission line producing an approximated Gaussian pulse, and iii) the monocycle pulse-forming network (PFN) which contains a resistor-capacitor (RC) differentiator producing the monocycle waveform. Figure 4.1 shows the three stages of the circuit.

The steps previously taken to tune, optimize and reconfigure the pulse generator for the 500 MHz to 5 GHz bandwidth is described in [13]. The generator is simulated using the Nexxim transient simulator from ANSYS Electronic Desktop [14]. Figure 4.2 shows the UWB pulse generator schematic. The component values are summarized in Table 4.1. The signal applied at P1 is an inverted 5V-TTL waveform with a 7 ns rise time. SD1 and SD2 are Infineon's BAT15 Schottky diodes [15] modelled using the provided Infineon's SPICE model. Note that R5 and R6 are used for simulation purposes only (as recommended by Infineon in the SPICE Model [16]) to improve the simulated reverse-bias performance. The step recovery diode (SRD) is an MMD830 from MACOM [17]. The model uses an ideal diode with parameters provided by

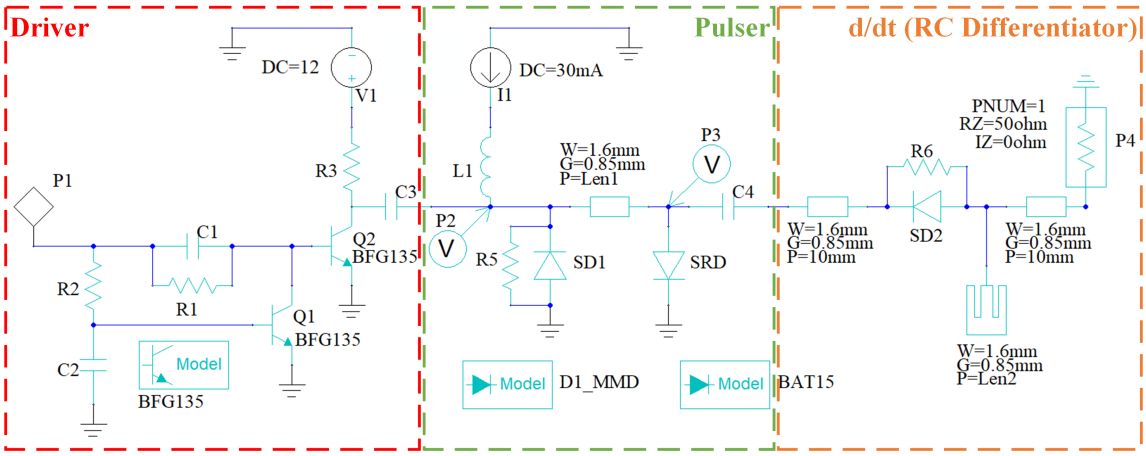


Figure 4.2: Schematic for the UWB pulse generator.

Table 4.1: List of transmitter component values.

Component	Value	Component	Value
R1	470 Ω	C1	47 pF
R2	1 kΩ	C2	10 pF
R3	150 Ω	C3	1 nF
L1	470 Ω	C4	3 pF
Len1	10 mm	Len2	14 mm

the SRD datasheet [17] because an actual model does not exist. Q1 and Q2 are NXP Semiconductor BFG135 transistors [18]. Coplanar waveguides are used as the transmission lines as they allow for easy shunt-element mounting and tuning of the shorted stub. The transmission lines have an impedance of 50 Ω on a 0.762 mm (30 mil) thick Rogers RO4003 substrate.

The fabricated printed circuit board (PCB) is shown in Figure 4.3. It fits in an enclosure with dimensions 124 mm by 63 mm by 30 mm (length (l) × width (w) × height (h)). A 12 V to 15 V and ∼ 147 mA source is required to power the on-board voltage regulators and the current source along with biasing the transistors. The input trigger for the pulse generator requires a 5V-TTL clock signal. A hex inverter [19] inverts the input trigger falling edge into a negative 5V-TTL rising edge with a known

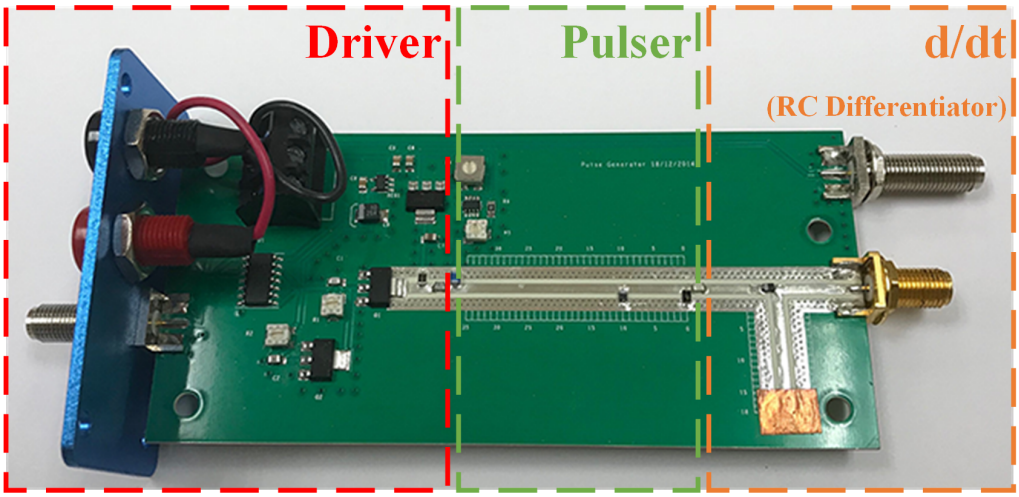


Figure 4.3: Fabricated UWB pulse generator board.

rise time. This allows for a standard TTL trigger source to be used. Variable resistors are used for R1 and R2, as well as for the feedback control resistors of the voltage regulator and the current source. The variability in the resistor values, the easy shunt-element placement and the tuning of the shorted stub allow for a tunable prototype of the pulse generator.

4.3 UWB Pulse Generator Measurements

The following measurements of the prototyped pulse generator [13] have been performed. The generator is tuned for its best performance according to two metrics: i) maximum peak-to-peak voltage and ii) maximum spectral coverage over the frequency band of interest (500 MHz to 5 GHz). A 10-dB high power UWB directional coupler [20] is used for the measurement of the output pulse. The directional coupler protects the input of the oscilloscope [21], which cannot handle the peak pulse power. The oscilloscope is connected to the coupled port, whereas a standard 50-Ω load terminates the output port. All measurements use a 15 V direct current (DC) power

supply to bias the pulse generator and a 5V-TTL square wave as the trigger unless otherwise noted. The square wave signal is generated from an AWG of a Keysight oscilloscope [22].

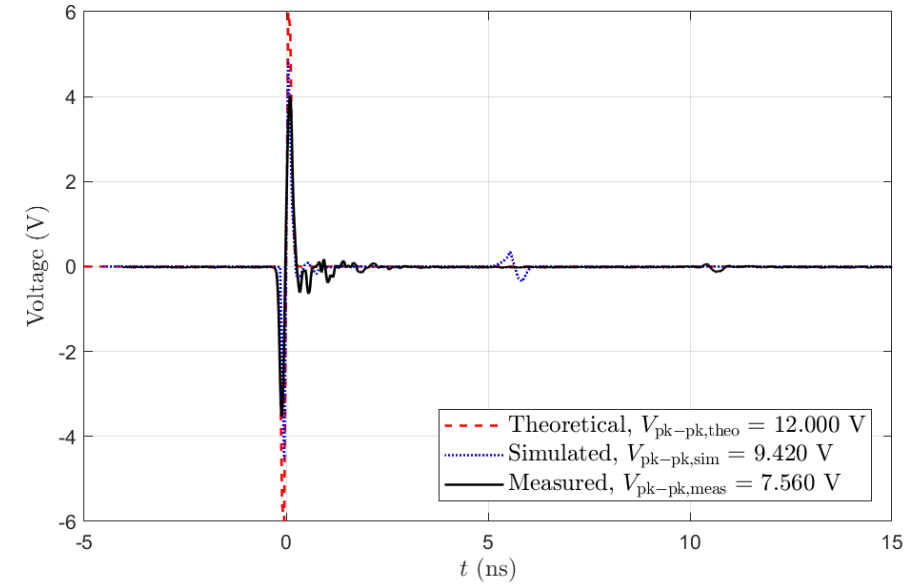
Figure 4.4 presents a comparison between the theoretical, simulated and measured temporal and spectral results for the UWB monocycle pulse. The theoretical model is based on the $\dot{g}(t)$ waveform from (3.2) where its amplitude is scaled using the following to fit within the 12 V peak-to-peak voltage,

$$V = \frac{-6\dot{g}(t)}{\max(\dot{g}(t))}. \tag{4.1}$$

A square wave trigger with a pulse repetition frequency (PRF) of 5.714 MHz and 15 V DC power supply are used for the measured results. The measured waveform is an average of 128 waveforms. Figure 4.5 shows only the measured waveform. The -10 dB bandwidth is indicated in figure 4.5b. The achieved maximum peak-to-peak voltage is 7.560 V. The -10 dB spectral bandwidth of the pulse is from 488.3 MHz to 3.7109 GHz.

There are discrepancies between the theoretical, simulated and measured results. The simulation results differ from the measured ones because of the ideal diode model and the simulation uncertainties of the SRD. A glitch can be observed in the simulated result after 5 ns, whereas in the measured results the glitch is smaller in amplitude and located closer to 10 ns. This late-time glitch is not desirable as it resides in the late-time response (LTR) region of the signal. Through the relatively strong antenna coupling, it may mask the LTR response of a target. Future work aims at the removal of this glitch and increasing the bandwidth of the transmitter to match our desired spectrum closely.

The UWB pulse generator has been claimed in [4] to operate at a PRF up to



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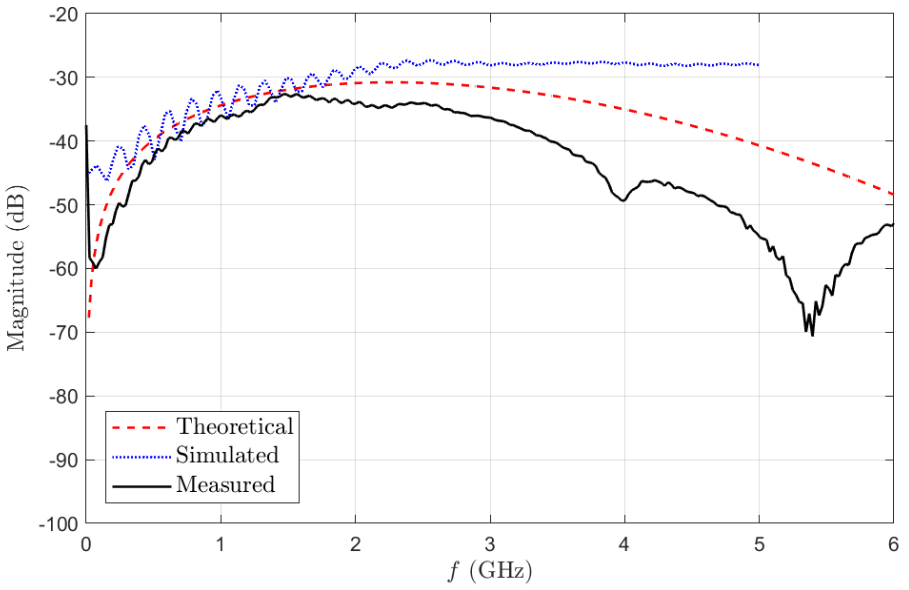
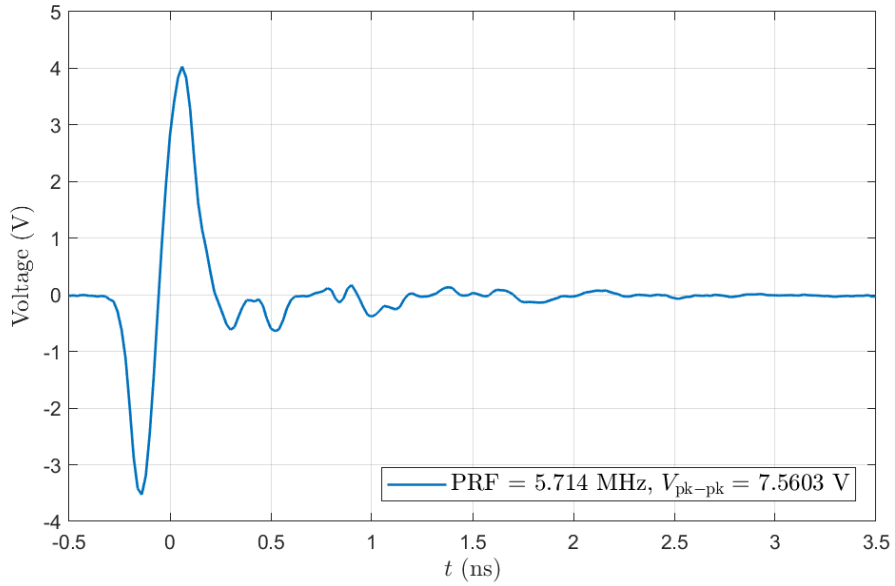


(b)

Figure 4.4: UWB pulse generated with a PRF of 5.714 MHz of a theoretical, simulated and measured Gaussian monocycle: (a) temporal plot and (b) spectral plot.



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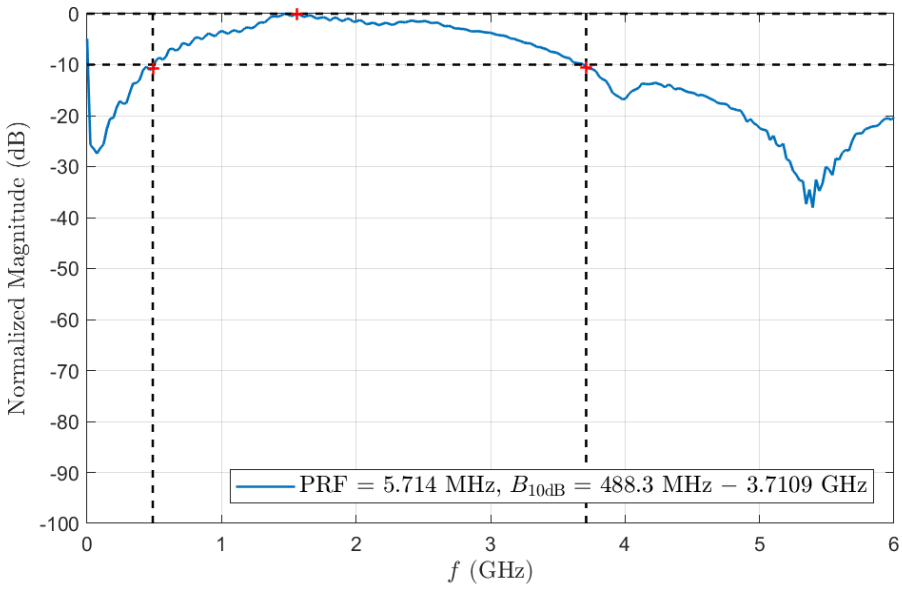


(b)

Figure 4.5: Measured UWB pulse generated with a PRF of 5.714 MHz: (a) temporal plot and (b) spectral plot.

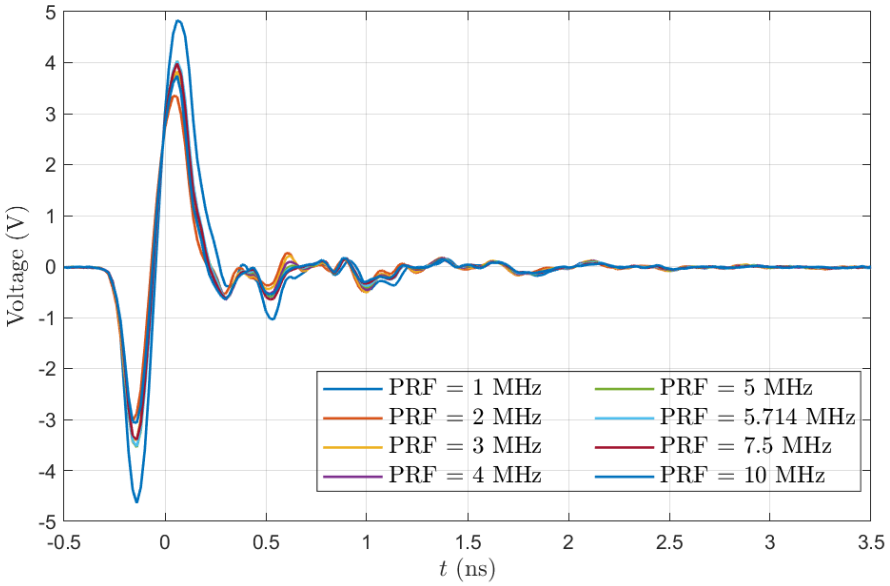
Table 4.2: UWB pulse peak-to-peak voltage generated at multiple PRFs.

PRF	$V_{\text{pk-pk}}$	PRF	$V_{\text{pk-pk}}$
1 MHz	9.477 V	7.5 MHz	7.385 V
2 MHz	6.379 V	10 MHz	6.815 V
3 MHz	7.231 V	10 MHz (Sinewave)	6.576 V
4 MHz	7.538 V	15 MHz (Sinewave)	5.533 V
5 MHz	7.584 V	20 MHz (Sinewave)	3.521 V
5.714 MHz	7.560 V	- - -	- - -

20 MHz. This design operates beyond the range of PRF values intended for our application (as previously discussed in earlier chapters). Thus, a validation of the acceptable range for the PRF has been conducted. Figure 4.6 and Figure 4.7 shows how the UWB pulse changes with different PRFs ranging from 1 MHz to 20 MHz. The waveforms in Figure 4.7 denoted in the legend as "(Sinewave)" have been triggered using a 5 V peak-to-peak voltage, 2.5 V DC offset sinewave. Sinewaves are used as equipment that supports a $5V$-TTL square wave at frequencies above 10 MHz can not be procured for the measurements. For reference, the UWB waveform generated by a 10 MHz square wave is also presented to show that there is minimal change between the output pulses due to the change in the trigger source. Table 4.2 summarizes the peak-to-peak voltages for different PRFs. Figure 4.8 shows the generated pulse with a 1 MHz PRF. The achieved maximum peak-to-peak voltage is 9.477 V. The -10 dB spectral bandwidth of the pulse is 439.5 MHz to 3.5889 GHz.

4.4 Signal Jitter and Noise

Signal stability is critical for the recovery of the weak resonant signature of a target. Jitter and noise can profoundly impact the signal recovery via equivalent-time sampling. A traditional way of evaluating the stability of repetitive signals in time



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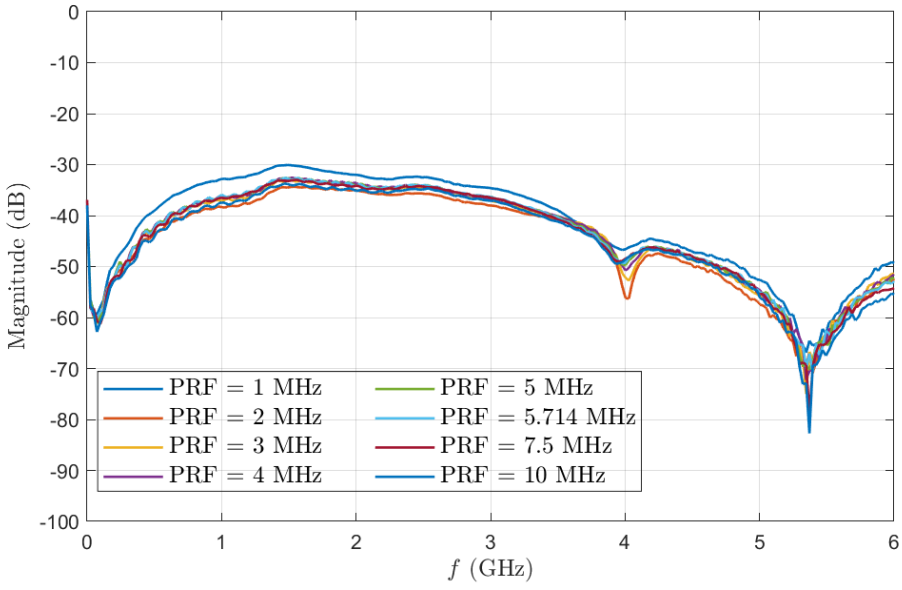
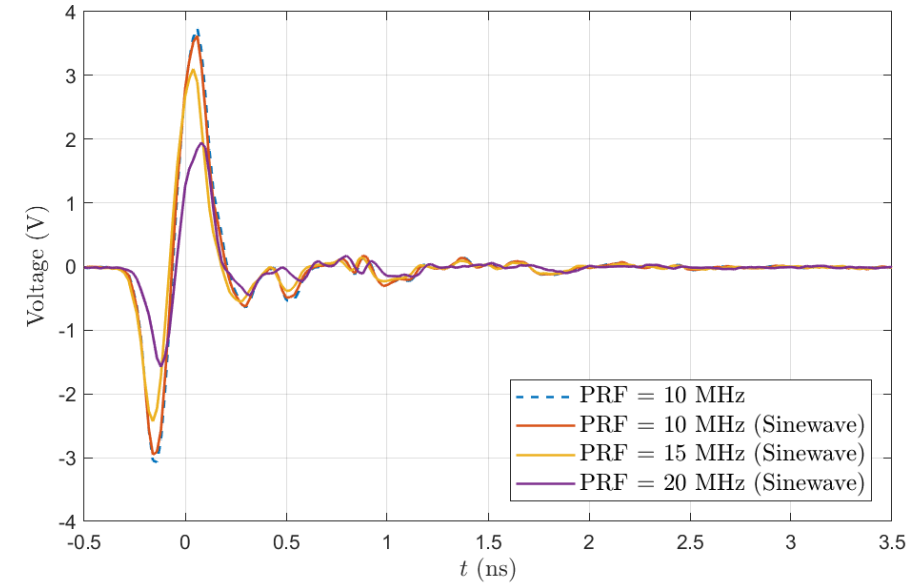


(b)

Figure 4.6: UWB pulse generated at multiple PRFs: (a) temporal plot and (b) spectral plot.



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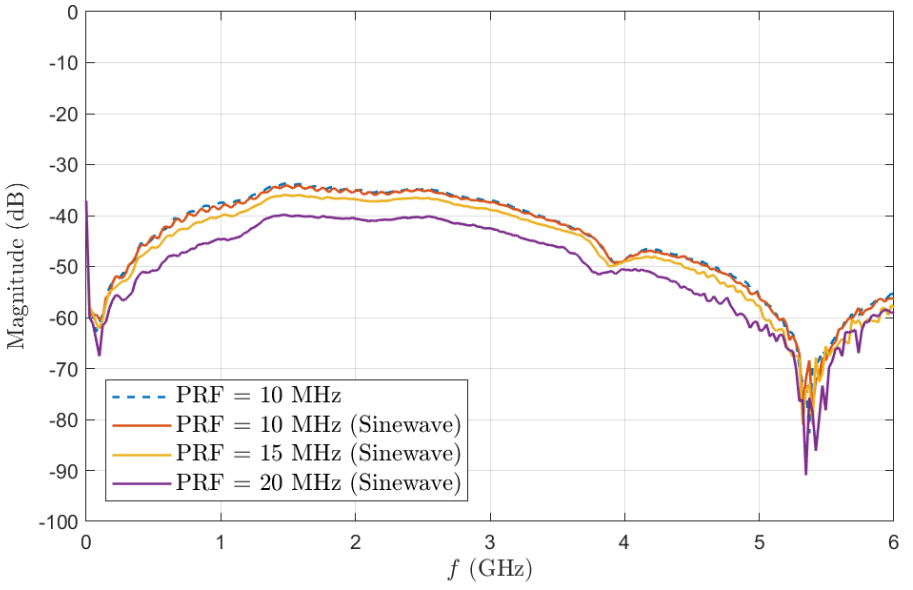
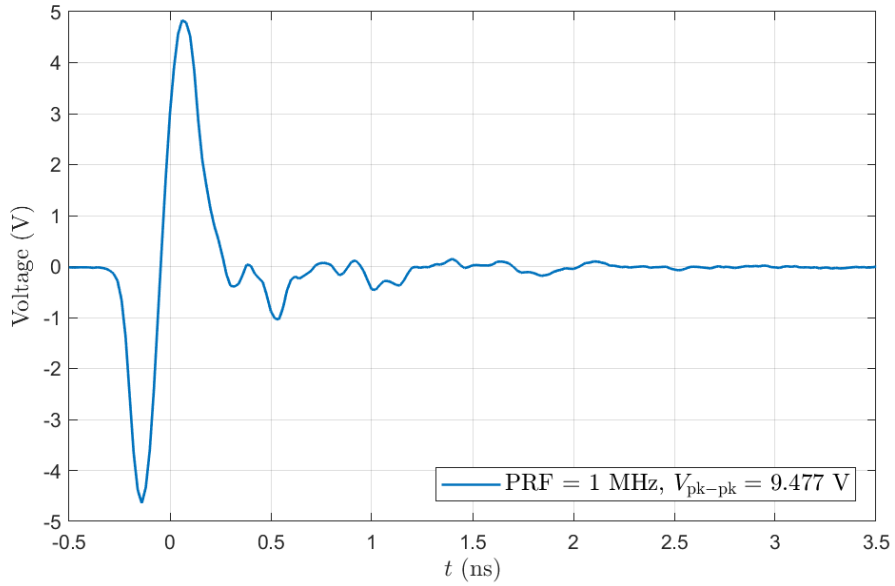


(b)

Figure 4.7: UWB pulse generated at multiple PRFs: (a) temporal plot and (b) spectral plot. Waveforms denoted as "(Sinewave)" in the legend are generated using a 5 V peak-to-peak sinewave with 2.5 V DC offset as a 5V-TTL signal can not be generated.



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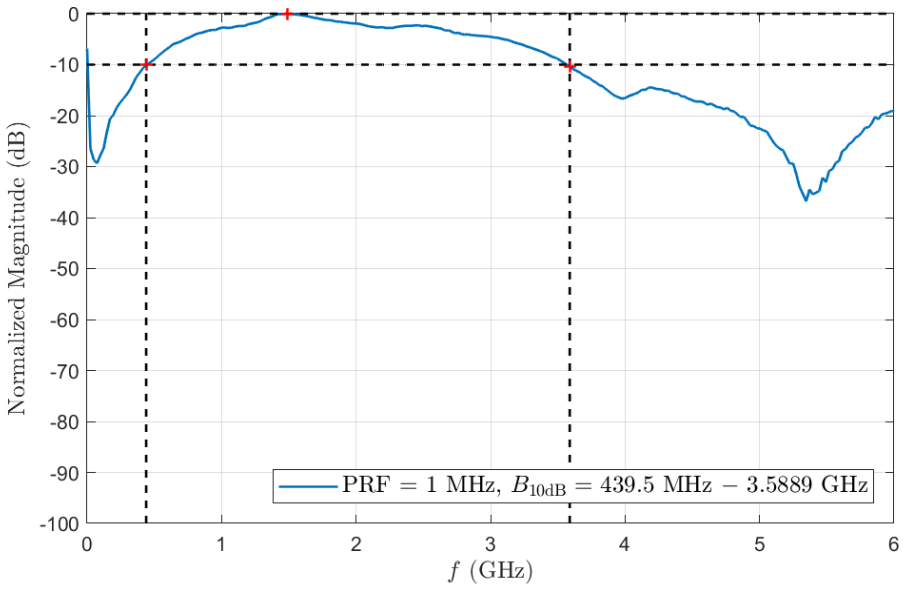

(b)

Figure 4.8: Measured UWB pulse generated with a PRF of 1 MHz: (a) temporal plot and (b) spectral plot.

is through jitter analysis. Another important metric is the voltage deviation due to noise. In this section, jitter and noise are defined and the measurements obtained using a pulse generator is presented.

4.4.1 Jitter Definitions

Jitter is the short-term variation of the significant instants of a timing signal from the ideal position in time [23, 24]. "Short-term" implies that these variations are of a frequency greater than or equal to 10 Hz. Jitter measurements are common in digital communication systems where it is crucial to have synchronization of the data bus between two points in a circuit. In radio frequency (RF) applications, jitter affects the timing signals used in the front-end conversion of an analog signal into the digital domain through digital signal processing (DSP) [25]. A perfect or ideal reference signal must have a fixed period and duty cycle which does not vary with time relative to a fixed starting point. Any jitter measurement can be performed on a repetitive signal as long as the ideal reference signal exists.

A UWB pulsed-radar system generates a periodic signal at a known fixed period relative to the starting time. Therefore, the reference signal can be found using the threshold trigger function of an oscilloscope. Then the time-interval error (TIE) is calculated based on multiple captures of the pulse.

Jitter is categorized into two groups depending on its physical nature: i) random jitter, and ii) deterministic jitter. Random jitter is stochastic and therefore there is no correlation between the source of jitter and an identifiable noise source. The probability distribution function (PDF) of random jitter often resembles a Gaussian distribution curve with a mean (μ) of zero and regions of standard deviation (σ). The nature of a Gaussian distribution is unbounded, i.e., it never reaches zero at its

extremities. Random jitter is therefore also unbounded and intrinsic to each system, making it difficult to diagnose and remedy [26]. A histogram can be used to show the number of hits against the time deviation of the recovered signal from the ideal signal. Deterministic jitter has an identifiable source which is often narrowband and periodic [26]. The PDF of a deterministic jitter does no resemble a Gaussian distribution. Most distributions are multimodal, typically consisting of a noisy sinusoidal signal that is the result of a periodic source of jitter.

Jitter can be examined by extracting the jitter component of a signal in the time domain [25]. The TIE measurement can be used to extract and examine the jitter component. The histogram of the error characterizes the jitter based on its physical nature. There are three different types of jitter TIE measurements considered here: i) peak-to-peak jitter, ii) absolute period jitter (6σ-Jitter), and iii) root-mean-square (RMS) jitter.

Peak-to-Peak Jitter

Peak-to-peak jitter is defined as the maximum observed amplitude in the TIE plot or the maximum time deviation captured by the TIE histogram over a specified time [25]. Peak-to-peak jitter is unbounded by nature; however, in measurements, it is limited by the oscilloscope capture time. Therefore, in practice, it is the maximum of the time deviation seen in the signal from its ideal time.

Absolute Period Jitter (6σ-Jitter)

Absolute period jitter, often referred to as 6σ-jitter, considers only the ± 3 standard deviation (σ) of the TIE histogram. It is sometimes better to bound the peak-to-peak jitter measurements statistically based on the histogram distribution. The 6σ-jitter is bounded by $\pm 3\sigma$, containing approximately 99.6 % of the distribution.

Table 4.3: Jitter comparison between custom UWB pulse generator and AWG.

Device	$T_{\text{jit(pk-pk)}}$	$T_{\text{jit}(6\sigma)}$	$T_{\text{jit(RMS)}}$
UWB Pulse Generator	9.000 ps	7.919 ps	1.320 ps
AWG	12.000 ps	7.858 ps	1.294 ps

Table 4.4: Noise comparison between custom UWB pulse generator and AWG.

Device	ΔV_{max}	$\Delta \bar{V}_{\text{max}}$	ΔV_{r}	$\Delta \bar{V}_{\text{r}}$
UWB Pulse Generator	324.0 mV	42.9 mV/pk	1079.0 mV	142.9 mV/pk
AWG	54.0 mV	68.9 mV/pk	68.4 mV	87.3 mV/pk

Root-Mean-Square (RMS) Jitter

The RMS jitter is the standard deviation (σ) of the TIE histogram [25]. The RMS jitter ($T_{\text{jit(RMS)}}$) and 6σ-jitter ($T_{\text{jit}(6\sigma)}$) have the following relationship

$$T_{\text{jit}(6\sigma)} = 6 \times T_{\text{jit(RMS)}}. \tag{4.2}$$

4.4.2 Jitter and Noise Measurements

Jitter measurements were performed using the built-in TIE measurement functions of the Tektronix Digital Signal Oscilloscope [21] in order to obtain the peak-to-peak jitter ($T_{\text{jit(pk-pk)}}$), 6σ-jitter ($T_{\text{jit}(6\sigma)}$) and RMS jitter ($T_{\text{jit(RMS)}}$). The results are summarized in Table 4.3 (see UWB pulse generator row). The 200 ps gating (capture) windows are defined around the zero crossing of the main monocycle pulse. The analysis is based on the TIE histogram of $1,000$ acquired pulses.

Two types of noise are evaluated using the difference between the upper and lower bounds of: i) the signal value at the positive peak of the main pulse (ΔV_{max}), and

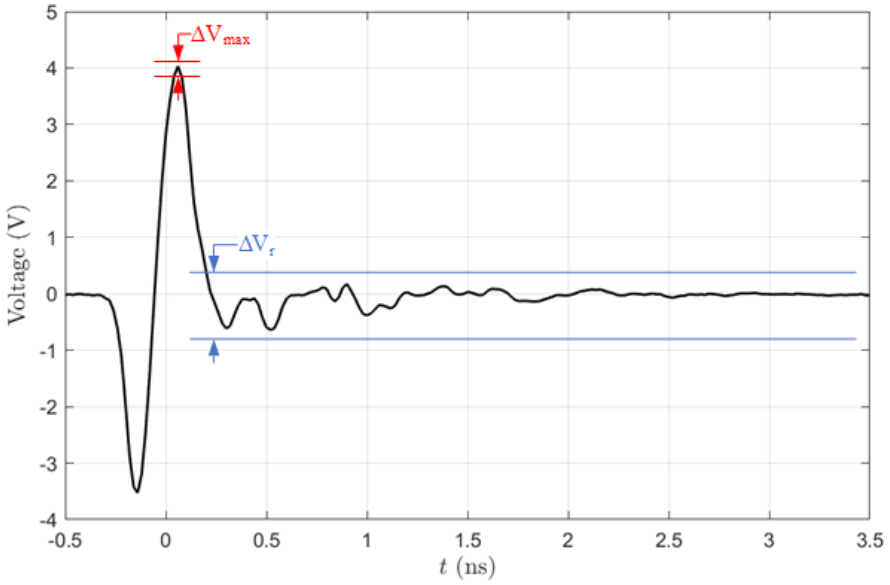

Figure 4.9: Voltage noise measurements: i) ΔV_{max} (red) ii) ΔV_{r} (blue).

ii) the peak-to-peak voltage (ΔV_{r}) after the first zero crossing following the main pulse. Refer to Figure 4.9 for these measurement locations. A histogram of $1,000$ waveforms are used. The results are summarized in Table 4.4 (UWB pulse generator row, columns 1 and 3).

For comparison, the same noise and jitter analysis are performed on a similar pulse generated by an AWG [27]. The jitter results are shown in Table 4.3 (see AWG row). The noise analysis results are shown in Table 4.4 (see AWG row, columns 1 and 3).

For a fair comparison of the noise levels between the two pulses, normalization with the signal strength is applied as

$$\Delta \bar{V}_{\text{max}} = \Delta V_{\text{max}} / V_{\text{pk-pk}}, \tag{4.3}$$

and

$$\Delta \bar{V}_{\text{r}} = \Delta V_{\text{r}} / V_{\text{pk-pk}}, \tag{4.4}$$

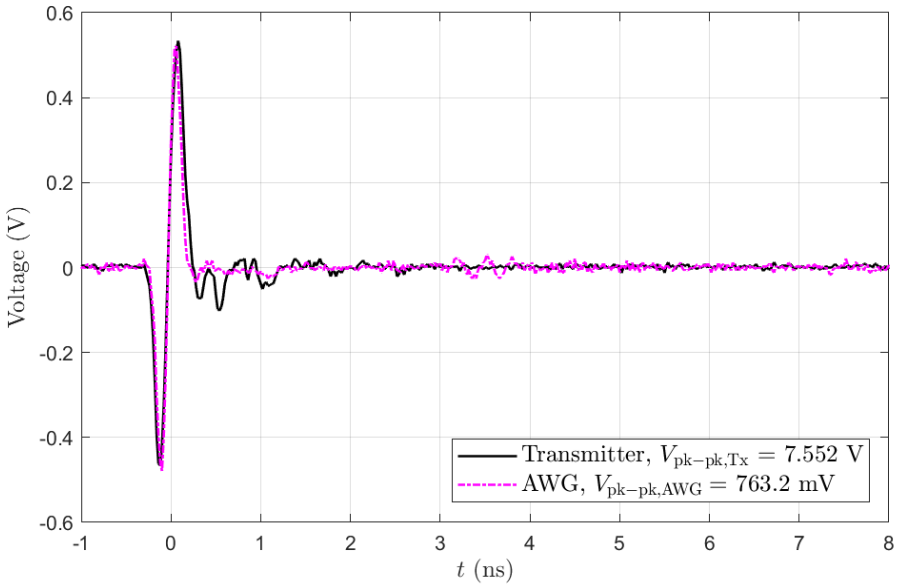

Figure 4.10: Pulsed generated by the UWB pulse generator and the AWG (normalized to their peak-to-peak value).

Refer to columns 3 and 4 in Table 4.4.

Figure 4.10 shows both the normalized UWB pulses of the generator and the AWG. It is evident that the pulse generated by the proposed UWB pulse generator has comparable noise and jitter performances to that of the AWG.

4.5 Conclusions

The design principles and the fabricated prototype of the UWB pulse generator are presented. The generator works at a variety of PRFs and can cover an approximate bandwidth from 450 MHz to 3.6 GHz. Future work aims at improving the bandwidth to cover the whole desired bandwidth from 500 MHz to 5 GHz and to remove the late-time glitch. The jitter and noise performance of the compact custom transmitter appear promising. The design closely matches that of the laboratory-grade bench-top AWG. However, quantifying jitter and noise performance metrics of a UWB pulse is

a relatively new topic discussed here with uncertainties in the measurements. Future work should expand upon and develop a rigorous methodology for quantifying jitter using high-quality, high-speed oscilloscopes.

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Chapter 5

UWB Equivalent-Time Sampling Receiver Design

5.1 Introduction

The ultra-wideband (UWB) Equivalent-Time Sampling Receiver hardware design is presented in the following chapter. UWB receivers are often unique in design and their architectures can vary as described in Chapter 2. Receivers employs various methods: i) direct sampling methods [1–8], ii) random or sequential equivalent-time sampling methods [9, 10], iii) time-interleaved [11] or channelized analog-to-digital converter (ADC) methods [12], iv) alternative ADC topologies on the complementary metal-oxide-semiconductor (CMOS) and/or integrated circuit (IC) level [13], and v) the synchronous time expansion method [14–16].

The design presented here is based initially on the concepts reported in [9] and [17] but implements a complete and customized solution to obtain the 1:10 bandwidth requirement of the system. The result is a low-cost receiver with the potential for a programmable effective sampling rate beyond 20 giga-samples per second (GSPS).

The architecture relies on four key off-the-shelf components: i) programmable delay chip (PDC), ii) track and hold (T & H) amplifier, iii) analog-to-digital converter (ADC), and iv) a field-programmable gate array (FPGA). Discussed next are the main design challenges with a focus on the microwave interconnects.

5.2 Theory of Operation

The main goal is to effectively increase the sampling rate of the receiver by implementing equivalent-time sampling. This allows for the use of a lower-end low-cost, high-speed ADC which samples at mega-samples per second (MSPS) rates to equivalently sample a signal that requires GSPS rates. This technique hinges on the receiver's ability to overcome four design challenges: i) the sampling rate of the ADC, ii) the ability to accurately shift the clock sampling signal, iii) the input bandwidth of the ADC, and iv) the dynamic range required for accurate data reconstruction.

The maximum spectral component ($f_{\max}$) of interest in the UWB pulsed radar system is 5 GHz. As discussed in Chapter 3 subsection 3.2.4, the receiver must have an equivalent-time sampling rate (f_{eq}) greater than or equal to 10 GSPS. This has a corresponding maximum equivalent-time sampling period t_{eq} of 0.1 ns. A 16-bit, dual channel ADC [18] with a sampling rate (f_{s}) up to 250 MSPS is used. The ADC is set to run at 200 MSPS corresponding to a 5 ns sampling period (t_{s}). Based on (2.21), the Equivalent-Time Sampling Receiver would require 50 pulses with a 0.1 ns time shift (Δt_{shift}) to meet the Nyquist Criterion. If the ADC were to operate at 250 MSPS, the design would see a reduction in acquisition time but at the cost of a more complex FPGA design. The sampling rate of 200 MSPS is chosen due to the FPGA constraints. The timing constraints within the FPGA become far more challenging with faster sampling rates.

The ability to shift the clock sampling position relative to the pulse trigger makes the equivalent-time sampling technique possible. The clock shift is accomplished by using a programmable delay chip (PDC) that is designed for clock de-skewing and timing adjustments in complex digital systems. It is of vital importance that all clocking devices have minimal impact on the clock jitter. The PDC must have a minimum delay step of 100 ps and be able to delay the full range of our sampling rates (i.e. 5 ns at 200 MSPS and 4 ns at 250 MSPS). A MC100EP195B PDC from ON Semiconductor [19] is chosen for its large programmable delay range (10 ns) and small incremental delay steps (10 ps). This device provides delay from 2.2 ns to 12.2 ns with a minimal 2 ps impact on clock jitter. Considering the 100 ps or 50 ps equivalent-time sampling periods, devices that introduce a comparable jitter component leads to instability in the ADC sampling and a reduction in the maximum reconstructed frequency.

The challenge with most ADCs which operate in the MSPS range is that they have limited input bandwidths. This limited bandwidth is problematic for the design of our UWB system, which has spectral components up to 5 GHz. A high input-bandwidth track and hold (T & H) or sample and hold device is used to overcome this issue. These devices pre-sample and hold the high bandwidth signal long enough to reduce the bandwidth to a level that is acceptable to the ADC. The ADC then samples during the hold stage ensuring a constant voltage amplitude. The design uses an HMC760LC4B T & H amplifier [20] from Analog Devices which has an input bandwidth of 5 GHz. This chip has a direct replacement with the HMC661LC4B T & H amplifier from Analog Devices [21] which has an input bandwidth up to 18 GHz for applications operating above 5 GHz.

Finally, the dynamic range of the receiver is essential because the back-scattered

late-time response (LTR) signals are weak by nature in comparison to their early-time response (ETR) counterparts. Chosen is the ADC [18] due to its high 16-bit resolution and excellent noise performance. Little-to-no performance benefits can be seen for operating the ADC at 200 MSPS over 250 MSPS [18].

The chosen ADC is dual-channel, allowing for fast reception on two channels. Achieving simultaneous multi-channel reception capabilities with a 1:10 bandwidth enables a real-time, two-channel UWB multiple-input, multiple-output (MIMO) system that can take advantage of antenna beam-forming, polarization diversity, and spatial diversity. Polarization diversity is possible through a full polarimetric measurement (H–H, H–V, V–H, and V–V) with two transmitting (Tx) and two receiving (Rx) antennas. The design comes at no loss in data acquisition speed and does not require radio frequency (RF) switching. The parallelization of processes available within the programmable logic (PL) of an FPGA to handle the data bus makes it possible.

5.3 Equivalent-Time Sampling Receiver Design

The Equivalent-Time Sampling Receiver is designed as an FPGA daughter board for the Digilent Zedboard [22]. It utilizes the FPGA standard low pin count (LPC) FPGA magazine card (FMC) (160-pin) interface. The interface pinout for the receiver and the Zedboard can be located in Appendix A and Appendix B, respectively. The FMC interface is an American National Standards Institute (ANSI) and VMEbus International Trade Association (VITA) standards developed by a consortium of FPGA vendors and end-users to accelerate their application development for baseboard and development kits [23]. Figure 5.1 shows the high-level block diagram of the Equivalent-Time Sampling Receiver. The on-board components are grouped into five categories described next.

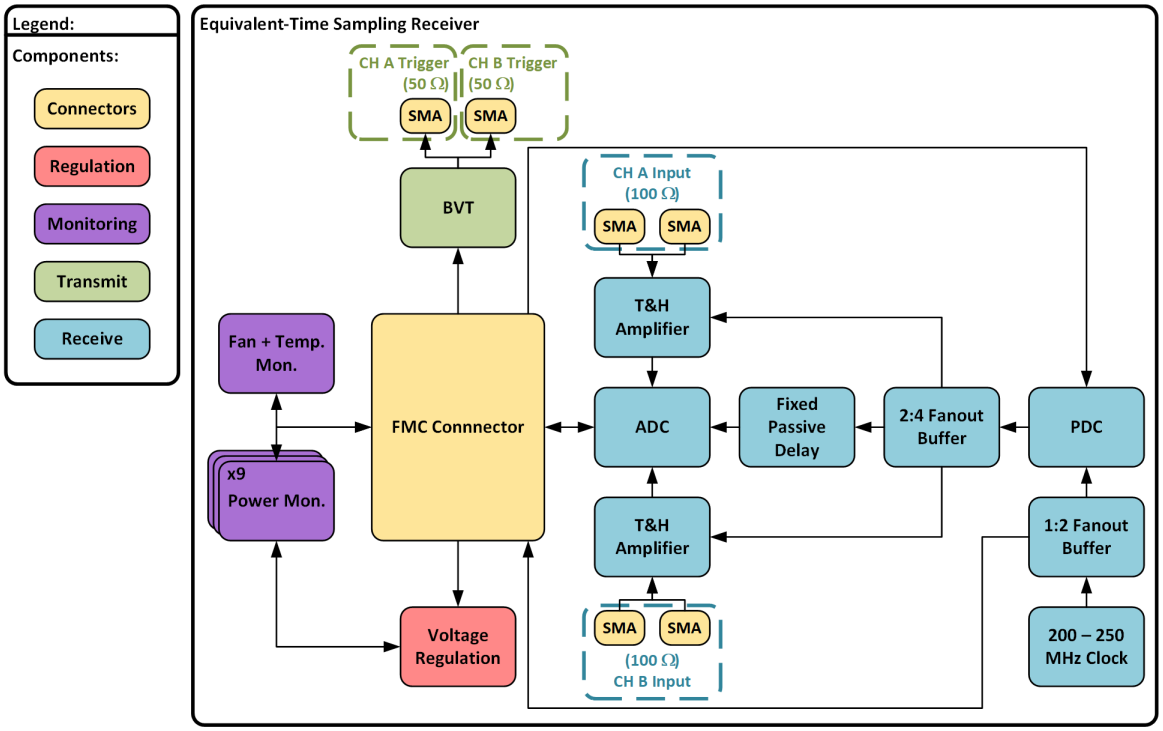


Figure 5.1: Block diagram of the Equivalent-Time Sampling Receiver.

Connectors: These blocks are the input/output (I/O) connectors of the Equivalent-Time Sampling Receiver board. They consist of the FMC connector that handles data offloading and control via the FPGA as well as all the RF Tx and Rx subminiature version A (SMA) connectors.

Regulation: Regulation blocks handle the on-board direct current (DC) voltage regulation required to provide the correct voltages to each IC. These are the Buck DC-DC converters and the low-dropout (LDO) regulators which regulate the 12.0 V, 3.3 V and VADJ (2.5 V) supplies provided by the FMC Connector.

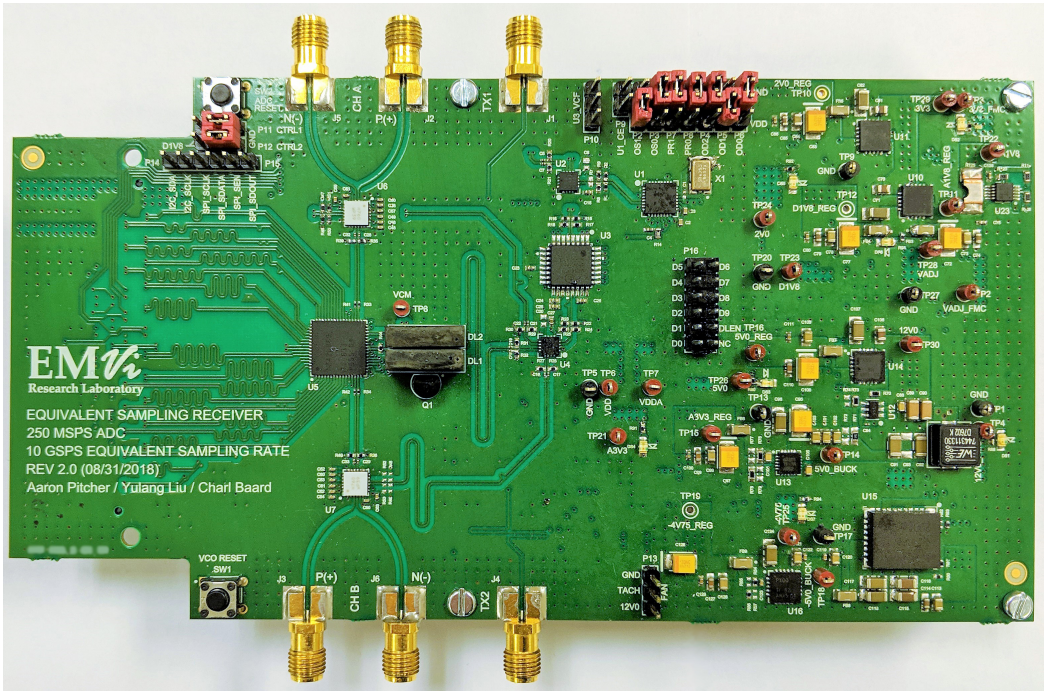
Monitoring: The board contains two types of monitoring components: i) a fan controller and temperature monitor which are used to read the board temperature and adjust the fan speed to control it, and ii) power monitors which measure all the voltage rails for voltage, current and power consumption, thus, ensuring the board is

operating nominally in different deployment scenarios.

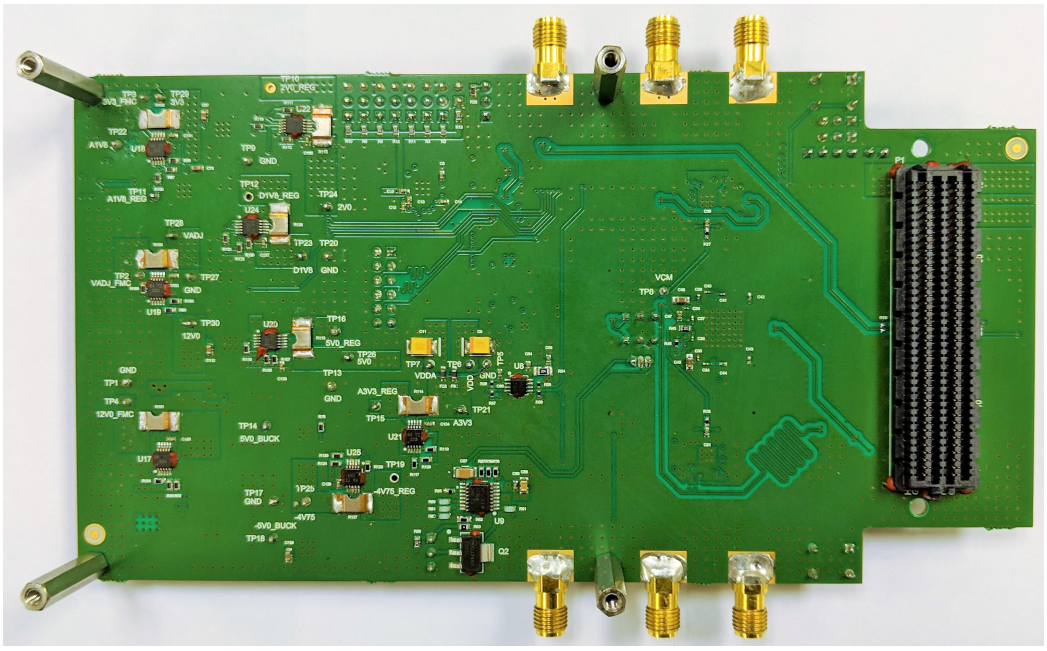
Transmit: The transmit block provides the trigger required by the transmitter. The bi-directional voltage translator (BVT) component is a logic level shifter designed to convert the 2.5 V low-voltage complementary metal-oxide semiconductor (LVCMOS) trigger signal (supplied from the FPGA) to a 5V-transistor-transistor logic (TTL) signal.

Receive: The received signals from channels A and B are sampled and digitized by receive blocks. These blocks contain all clocking networks including the PDC and the RF front end of the receiver. Here, the timing and the transmission line design of the microwave interconnects are critical.

Figure 5.2 shows the fabricated prototype of the Equivalent-Time Sampling Receiver. The printed circuit board (PCB) and the FPGA together fit an enclosure measuring 406 mm by 203 mm by 76 mm (length (l) $\times$ width (w) $\times$ height (h)). The receiver is an eight layer PCB consisting of two Rogers RO4003C substrate cores [24] and two standard FR-4 cores [25]. An FR-4 pre-impregnate [26] is used for laminating the substrate cores together. The PCB board stack-up is shown in Figure 5.3. An eight-layer board is required for separation and routing of various traces and planes: i) the voltage supplies, ii) the serial peripheral interface (SPI), inter-integrated circuit (I^2C), and PDC digital control bus, and iii) the RF signals which operate up to 5 GHz. Rogers RO4003C is chosen due to its low-loss ceramic substrate properties that are critical for the giga-hertz RF traces on the board. Therefore, only the top and bottom copper layers are used for the RF traces backed by a ground plane. The internal layers for the power planes and the control signals (i.e. SPI, I^2C, and the PDC digital control bus) use FR-4. The overall cost of the PCB reduces with the use of cheaper substrate (FR-4). The dielectric properties of the cores and the



(a)



(b)

Figure 5.2: Equivalent-Time Sampling Receiver board views: (a) top and (b) bottom.

Table 5.1: Substrate dielectric properties [24–26].

Substrate	**Material**	**Dielectric Constant** (ϵ_r)	**Loss Tangent** ($\tan(\delta)$)
Roger RO4003C	Core	3.38	0.0021
Isola Group 185HR (FR-4)	Core	4.13	0.0158
Technolam NP-175F (FR-4)	Pre-impregnate (Prepreg)	4.64	0.0110

pre-impregnates are summarized in Table 5.1.

All microwave transmission lines are designed for the Roger substrate of 0.2032 mm (8 mil*) height (h) backed by a ground plane. Figure 5.4 provides a cross-section and dimensions of the two types of microwave transmission lines. The 50-Ω single-ended microstrip line (shown in figure 5.4a) has a width (w) of 0.4064 mm (16 mil). The 100-Ω odd-mode coupled microstrip line (shown in figure 5.4b) has a width (w) of 0.2794 mm (11 mil) and a gap (g) of 0.1778 mm (7 mil). The odd-mode coupled microstrip lines are sometimes referred to as differential lines. For impedance calculations, a copper thickness (t) of 0.0533 mm (2.1 mil) is used. The impedance calculations are verified using the National Instruments TX-LINE [27], Mantaro Online Impedance Calculator [28] and the Saturn PCB Design Toolkit [29]. The ground planes located on the same layer as the microwave transmission lines have a minimum separation distance (s) of 0.8382 mm (33 mil). Blind vias† are used between the RF Signal 1 and GND 1 layers, as well as RF Signal 2 and GND 3 layers (refer to Figure 5.3) in order to shield the RF traces when possible. These blind vias are connected to ground planes and are placed approximately the same distance (s) ensuring that the via diameter is within the ground plane. The PCB is ground stitched with full height

*1 mil = 0.001 inch = 0.0254 mm.

†Blind vias are vias (copper-plated holes) which connect external layers to one or more inner layers. They do not fully penetrate the PCB board.

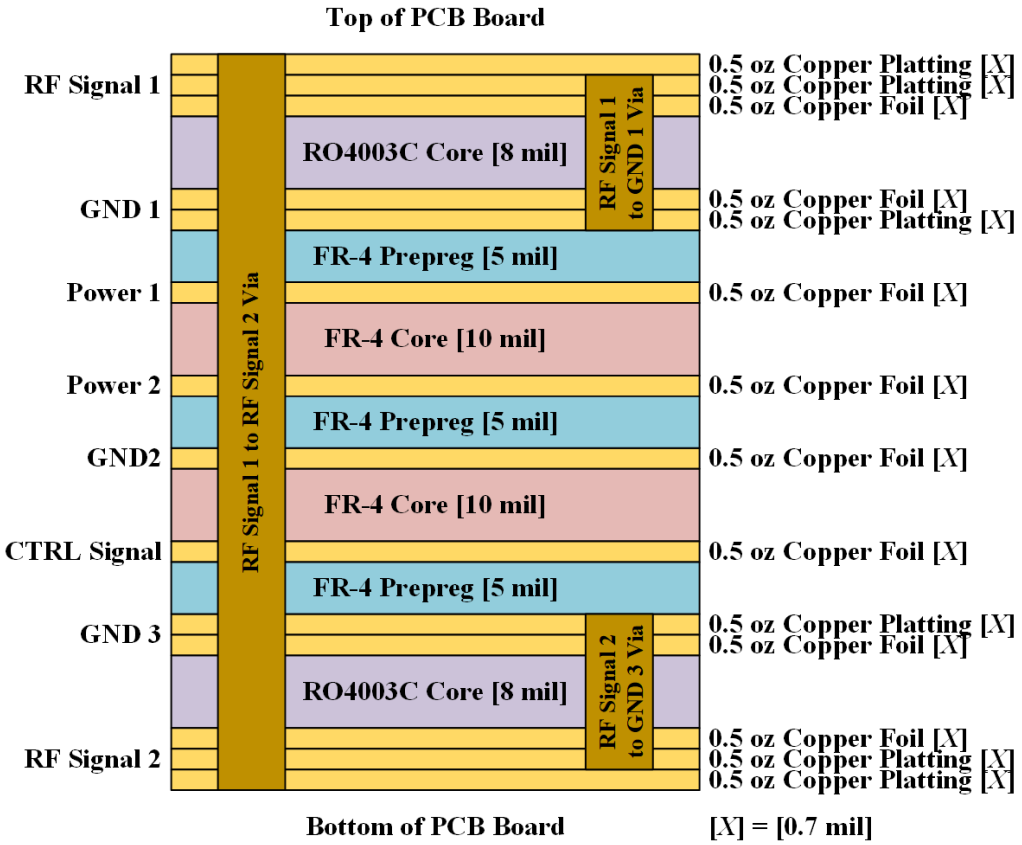


Figure 5.3: Equivalent-Time Sampling Receiver eight layer PCB stack-up. Shown is a cross-section of the board with the layers associated with the PCB design, where RF Signal 1 is at the top of the board and RF Signal 2 is at the bottom. The purple layers represent the Rogers RO4003C cores, the red layers represent the FR-4 cores, and the teal layers represent the FR-4 pre-impregnate. The copper foil and plating layers are shown in yellow, whereas the vias are in gold. This design contains both regular vias and blind vias. The signal layer names are indicated on the left and the copper foil and plating layers are shown on the right.

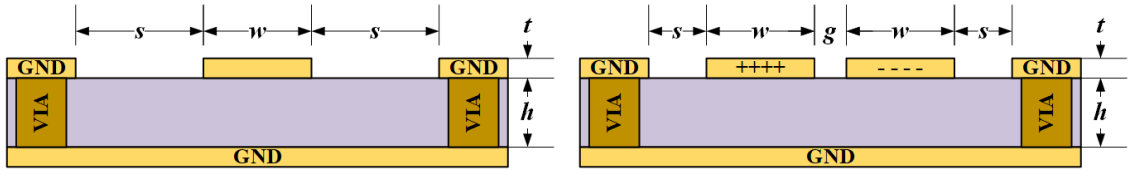


Figure 5.4: Microwave transmission line cross-sections with dimensions: (a) microstrip line, and (b) odd-mode coupled microstrip line (differential line).

copper plated vias minimizing the return path from ground.

An annotated layout of the PCB is shown in Appendix C. It provides a top and bottom view noting the layout of each IC, as well as each copper layer. The annotation boxes with a fill colour (not gray) and the ICs outlined in an unbroken line follow the same colour as the function notation in Figure 5.1. The annotation boxes with a gray fill colour outlined by colour and the correlated PCB traces outlined in the same colour with the dashed line are groups of signals linking the ICs together. The traces not annotated are the power planes, as well as the SPI and the I^2C lines, which follow standard PCB design practices.

5.4 Sample Clocking Network

5.4.1 Timing Calculations

The functionality of the receiver depends critically on the sample clocking network. Accurate timing of the clocks is achieved using the following timing diagram (shown in Figure 5.5) and timing calculations. The clocking network is implemented using the low voltage differential signaling (LVDS).

The T & H amplifier has two modes of operation. 1) In the "track mode" interval of the output signal (positive differential clock voltage) the device behaves as a unity

gain amplifier which replicates the input signal at the output subject to the input bandwidth and the output amplifier bandwidth limitations [20]. 2) The "hold mode" begins at the positive-to-negative clock transition where the device samples the input signal with a very narrow sampling time aperture and holds the output relatively constant during the negative clock interval at a value which is representative of the signal at the instant of sampling [20]. It is important that the T & H amplifier and the ADC are triggered at the correct time allowing the ADC to sample within the "hold mode". Shown in Figure 5.6 is the simplified model of the T & H amplifier and its operation. The switch triggered by the clock signal (CLK) controls the charge and the discharge of the output capacitor. When the switch is closed (track mode), the signal applied at the input is seen at the output. When the switch is open (hold mode), the last voltage over the ideal capacitor is held before the release of the switch.

The design uses three key timing constraints:

$$t_1 = t_3, \tag{5.1}$$

$$t_4 = t_5, \text{ and} \tag{5.2}$$

$$t_2 = t_1 + t_5 + t_{\text{delay}} = t_3 + t_4 + t_{\text{delay}}, \tag{5.3}$$

where t_{n} (n = 1, ..., 5) are the signal travel times between ICs (shown in Figure 5.5) and t_{delay} is the delay applied to the ADC clock (t_2) to compensate for the other sampling network delays. These sampling network delays consist of the following: i) the settling time (t_{ST}) in the T & H amplifier, ii) the internal clock buffer pipeline delay (t_{CD}) in the T & H amplifier, iii) the aperture delay (t_{A}) in the ADC, and iv) an offset (t_{Offset}) applied to shift the sample point away from the track-to-hold transition edge of the T & H amplifier. The settling time in the T & H amplifier

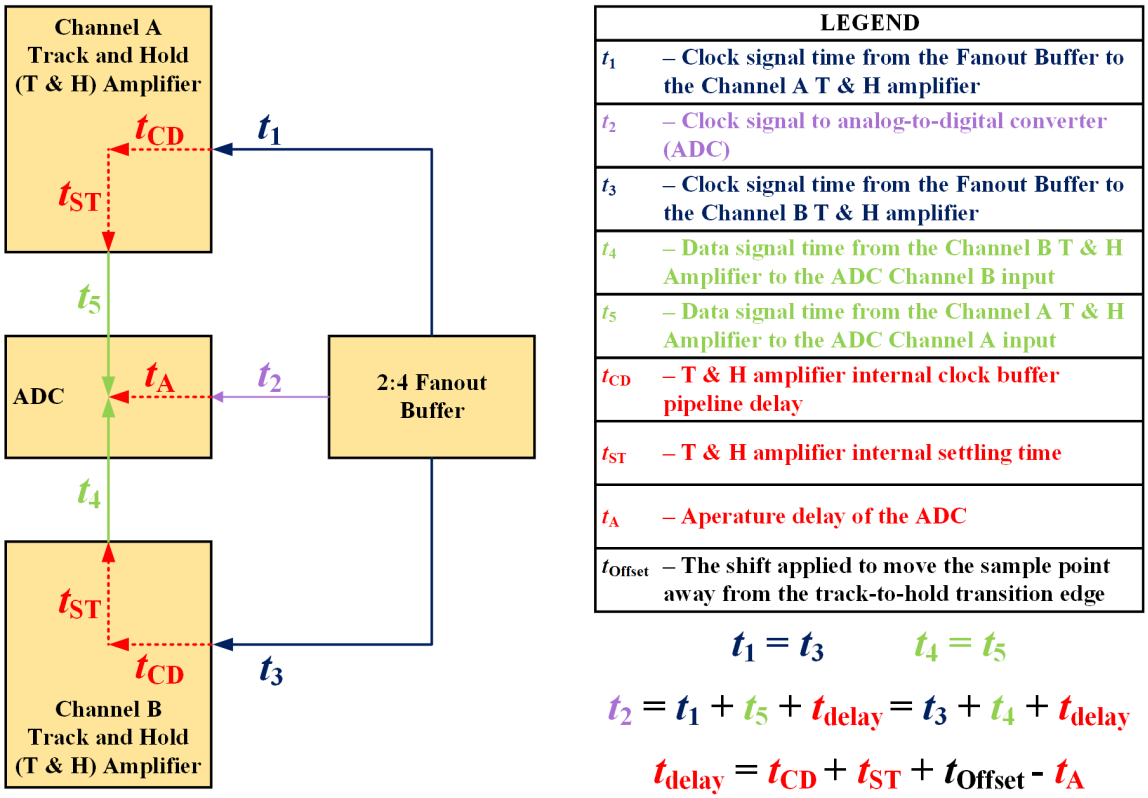


Figure 5.5: Diagram of the Equivalent-Time Sampling Receiver clocking network.

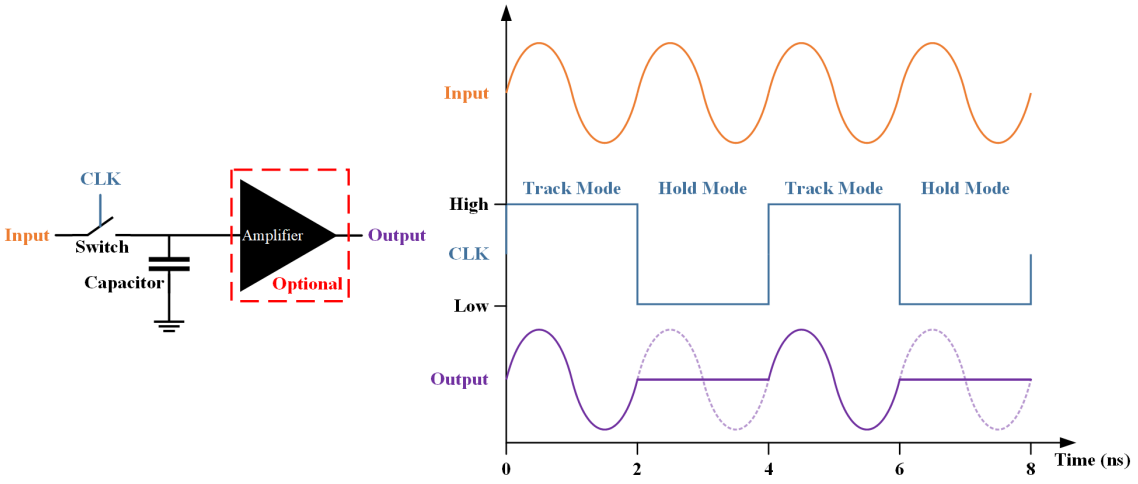


Figure 5.6: Simplified model of a T & H amplifier (shown on the left) and the waveforms of each signal (shown on the right) assuming ideal devices with no losses.

Table 5.2: The sampling network delays and their time values [18, 20].

Parameter	Time (ns)
t_{ST}	0.116
t_{CD}	0.035
t_{A}	0.7

is the time interval between the track-to-hold transition and the time at which the output signal is settled to within 1 mV [20]. According to [20], this includes the group delay of the output amplifier but does not include the pipeline delay of the clock. Thus, the internal clock buffer pipeline delay is added. The acquisition time and aperture delay of the T & H amplifier are not used because they are relative to the input signal before sampling. These metrics do not relate to these sample timing calculations. However, the aperture delay of the ADC does matter as it is within the sample clocking network. It is the delay of the exact sample time relative to the time that the input clock applies the sample command (i.e. when the clock triggers, a sample is taken X seconds later). Table 5.2 is a summary of the sampling network delays and their physical delay values according to the datasheets [18] and [20]. Thus, the delay time (t_{delay}) required for the ADC clocking signal (t_2) based on Figure 5.5 can be defined as

$$\begin{aligned} t_2 + t_{\mathrm{A}} &= t_1 + t_5 + t_{\mathrm{CD}} + t_{\mathrm{ST}} + t_{\mathrm{offset}} \\ t_2 &= t_1 + t_5 + t_{\mathrm{CD}} + t_{\mathrm{ST}} + t_{\mathrm{offset}} - t_{\mathrm{A}}. \end{aligned} \tag{5.4}$$

Knowing (5.3) and the parameter values from Table 5.2, t_{delay} can be solved as

$$\begin{aligned} t_{\text{delay}} &= t_{\text{CD}} + t_{\text{ST}} + t_{\text{offset}} - t_{\text{A}} \\ &= 0.035 \text{ ns} + 0.116 \text{ ns} + t_{\text{offset}} - 0.7 \text{ ns} \\ &= t_{\text{offset}} - 0.549 \text{ ns}. \end{aligned} \tag{5.5}$$

The offset time (t_{Offset}) ensures that the ADC samples away from the track-to-hold transition of the T & H amplifier (refer to Figure 5.7). If the maximum of the receiver sampling frequency is 250 MHz, corresponding to a 4 ns sampling period, the hold stage of the T & H amplifier is only half the period (i.e. 2 ns). The desired sampling region of the ADC is away from the transitions from track-to-hold and from hold-to-track. Thus, sampling in the center of the hold mode such that $t_{\text{Offset}} = 1$ ns ensures that a transition edge is 1 ns away and that the voltage on the capacitor has become stable.

Therefore, for $t_{\text{offset}} = 1$ ns, the calculated delay is $t_{\text{delay}} = 0.451$ ns. The fixed passive delay component in Figure 5.1 is used to achieve this delay. The design uses

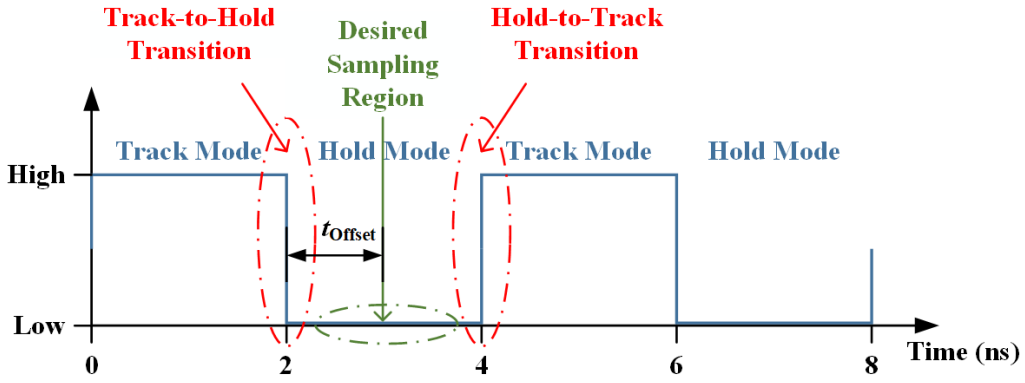
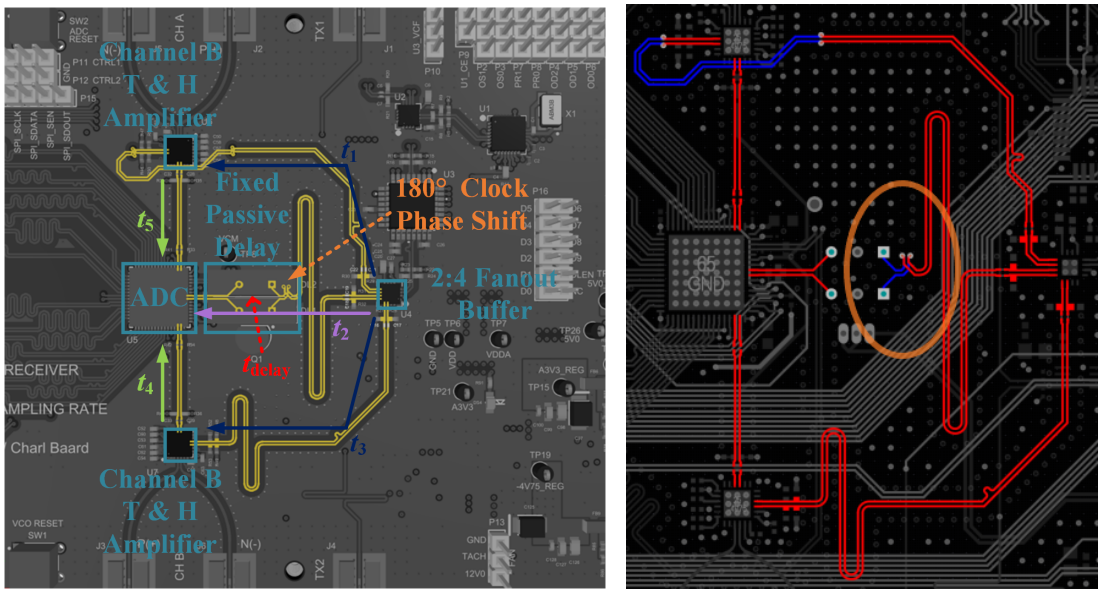


Figure 5.7: The desired sampling region of the ADC (shown in green) based on the track and hold (T & H) amplifier clock signal, its respective modes and transition edges. The T & H amplifier is in track mode when the clock is high and hold mode when the clock is low.



(a) (b)

Figure 5.8: The sample clocking network traces realized within the Equivalent-Time Sampling Receiver PCB. The 180° phase shift implemented in the traces is shown in orange. (a) A 3D view where: i) the differential traces are shown in yellow, ii) the ICs are outlined in teal, and iii) the signal times are annotated according to Figure 5.5. (b) A 2D view where the red traces are located on the top (RF Signal 1) layer and the blue traces are located on the bottom (RF Signal 2) layer.

a passive delay line [30] with a delay value of 0.5 ns.

Finally, the hold mode of the T & H amplifier occurs when its clock state is low, whereas the ADC samples on the rising edge of its clock signal. The calculation from (5.4) assumes that the "hold mode" of the T & H amplifier and the ADC sampling happen on the same clock state (positive). Therefore, the clock of the ADC must be 180° (out of phase) from the T & H amplifier clock.

5.4.2 Sample Clocking Network Design

The PCB implementation of the sample clocking network is shown in Figure 5.8. The location of each IC and the signal times according to Figure 5.5 are annotated.

The transmission lines in use here are the odd-mode coupled microstrip lines. These allows for the timing considerations (outlined in (5.1) to (5.3)) to use trace lengths (instead of time) between the ICs. This is because the phase velocity (v_p) of a transverse electromagnetic (TEM) line is constant over the given medium. Therefore, (5.1) to (5.3) can be re-written as:

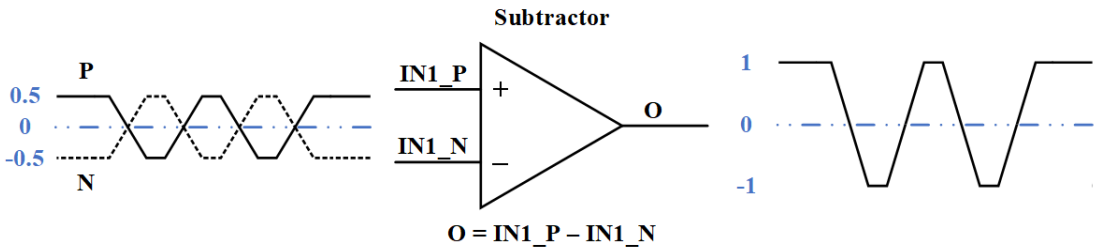
$$l_1 = l_3, \tag{5.6}$$

$$l_4 = l_5, \text{ and} \tag{5.7}$$

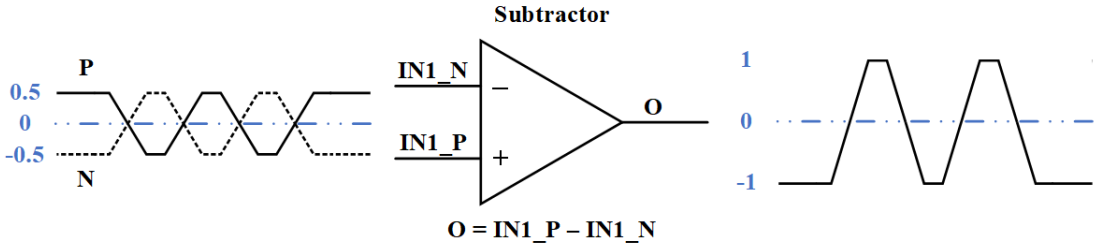
$$l_2 = l_1 + l_5 + (v_\mathrm{p} \cdot t_\mathrm{delay}) = l_1 + l_5 + (v_\mathrm{p} \cdot t_\mathrm{delay}), \tag{5.8}$$

where l_n ($n = 1, ..., 5$) are the trace lengths between ICs corresponding to t_n (i.e. $t_n = l_n/v_\mathrm{p}$). The passive fixed delay line is then used to implement the $(v_\mathrm{p} \cdot t_\mathrm{delay})$ delay. Ensuring the length of the traces based on (5.6) to (5.8) will maintain the timing constraints. The meandering lines are then used to enforce these trace length requirements.

Lastly, swapping the positive and negative signals of the low voltage differential signaling (LVDS) clock accomplishes the 180° phase shift to the ADC clock. Figure 5.9 shows how swapping the positive (P) and negative (N) pins of the subtractor impacts the output (O) of the receiver. The swap of the traces is shown in Figure 5.8b (circled in yellow). The clock signal to the right of the fixed passive delay device is taken to the bottom layer of the board so that the traces can swap before reaching the passive fixed delay device. With reference to Figure 5.8b, the red traces are located on the top (RF Signal 1) layer of the PCB whereas the blue traces are on the bottom (RF Signal 2) layer. Refer to Appendix C for a layer-by-layer layout of the PCB which shows a more detailed view of these traces.



(a)



(b)

Figure 5.9: A simplified LVDS subtractor circuit used for the conversion of the differential to a single-ended signal. The input differential signals are on the left and the output single-ended signal is on the right. (a) When the positive (P) and negative (N) signals are fed correctly to the IN1_P and IN1_N pins, respectively. (b) When the P and N signals are swapped and fed to IN1_N and IN1_P, respectively.

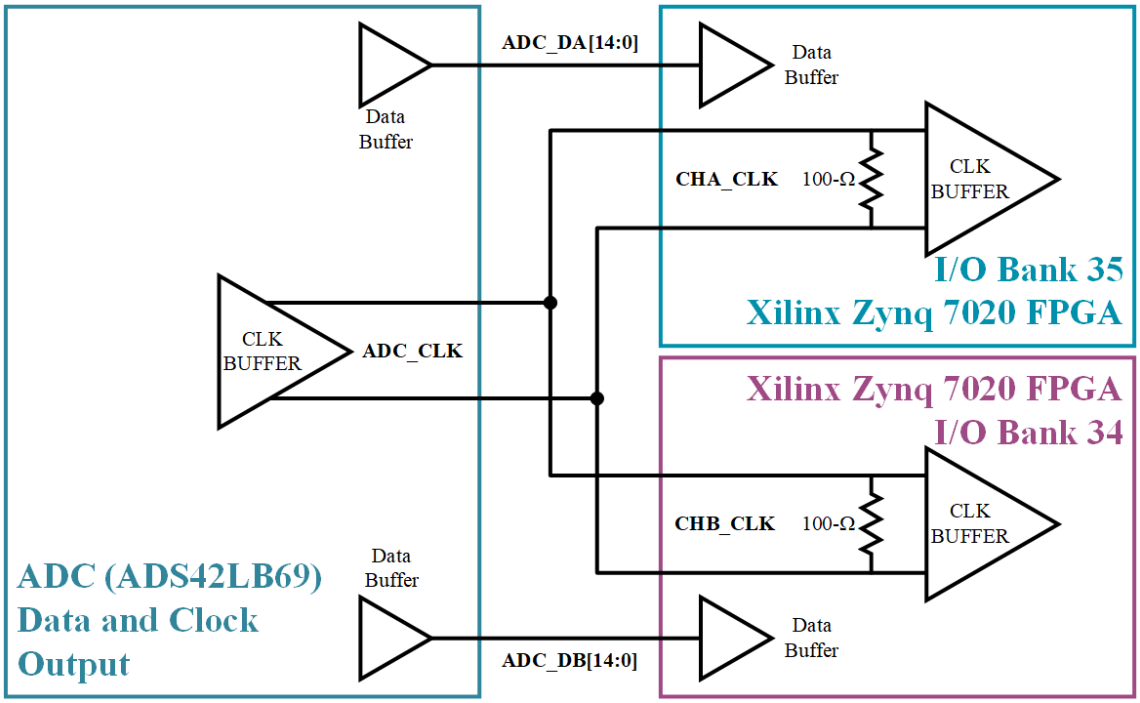


Figure 5.10: Block diagram of the ADC data bus clock output splitting. The single output clock divides between the two I/O banks (bank 34 and bank 35) of the Xilinx Zynq-7020 SoC. Here, the channel A data bus and split reference clock "CHA_CLK" is sent to bank 35 and the channel B data bus and split reference clock "CHB_CLK" is sent to bank 34. The separation of the channel data buses ensure proper deserialization within the FPGA (refer to Chapter 6).

5.5 ADC Data Bus Clock Output Splitting

The other critical design choice made in the Equivalent-Time Sampling Receiver is the ADC data bus clock splitting. The digital output from the ADC contains two LVDS 8 lane data buses tied to a single clock reference. This results in 34 (2 channels $\times$ 8 lanes $\times$ 2 traces per lane + 2 traces per clock) traces being routed to the FMC interface for the dual channel system. In order for the internal resources of the FPGA to receive the ADC data bus, the data bus and the reference clock must be split between two I/O banks. The concept is shown in Figure 5.10. The chip located on the Digilent Zedboard (the FPGA platform) is the Xilinx Zynq-7020 system on a

chip (SoC) [22, 31]. This chip contains multiple I/O banks which provide access to the processing system (PS) and PL sections. The I/O banks connected directly to the FMC interface are bank 34 and bank 35 [32]. The ADC data bus and reference clock split so that channel A data are sent to bank 35 and channel B data are sent to bank 34. Bank 35 is chosen for channel A due to logistics in the PCB routing of the Equivalent-Time Sampling Receiver. Channel A and Channel B split for two reasons: i) the number of I/O per bank cannot support the total number of traces for both channels, and ii) the internal FPGA resources utilize local clock buffer tied to their clock regions.

Figure 5.11 shows the internal floorplan of the FPGA provided from the Vivado Design Suite software [33]. The Advanced RISC Machine (ARM) central processing units (CPUs) section (PS section) is outlined in red, whereas the PL is shown in yellow separated by its clocking regions. The banks (bank 34 and bank 35) reside in their separate clock regions (shown in yellow in Figure 5.11). For more information on the FPGA clock resources, clock regions and floorplan, refer to [34].

Banks 34 and 35 have their separate FPGA resources which can use either an I/O clock buffer (BUFIO) or a regional clock buffer (BUFR) locked to their respective region. Horizontal clock buffers (BUFH) and global clock buffers (BUFG) are used to transfer those clocks to other regions. Additionally, the resources (shown in pink from Figure 5.11) are kept close to the I/O pins to minimize timing between components. Providing only one clock for both I/O banks causes a problem within the FPGA as it tries to meet the timing constraints based on the physical clock routing available. The clock must then be separated outside the chip (as shown in Figure 5.10) in order to receive the ADC channel data correctly. Finally, to access these clock buffers, the clock must drive a clock capable (CC) pin; otherwise, meeting signal timing is not be possible.

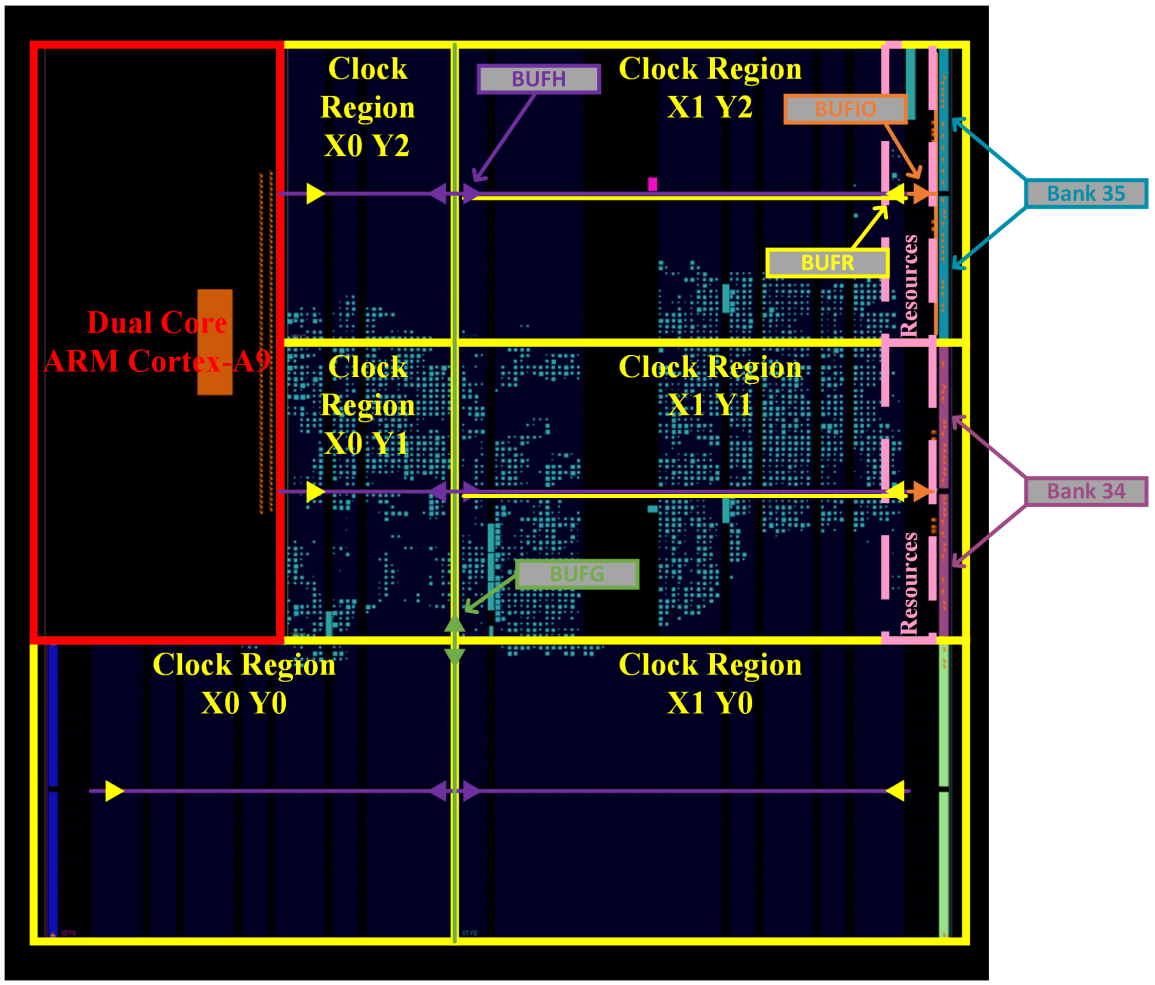
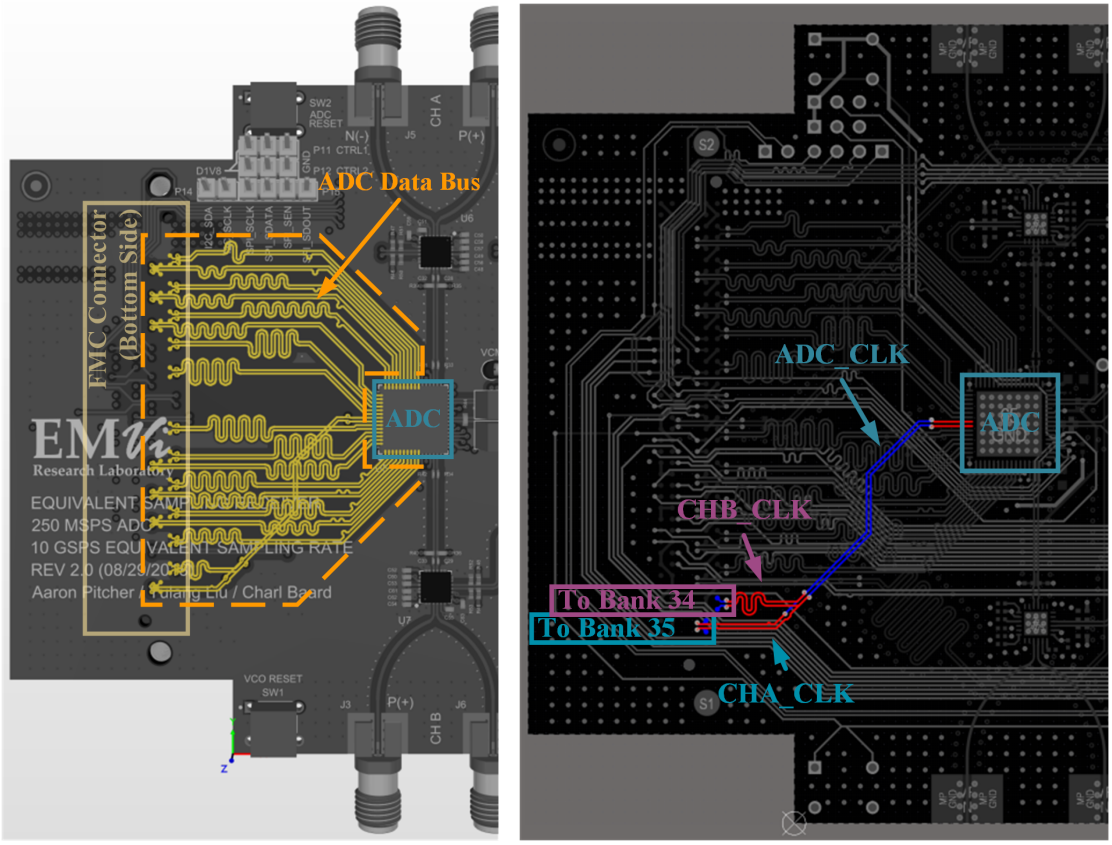


Figure 5.11: The internal clocking regions of the Xilinx Zynq 7020 Chip. The Vivado Design Suite software [33] provides the chip floorplan of the FPGA. The dual-core ARM Cortex-A9 section of the chip is annotated in red, whereas the PL is in yellow broken into clocking regions. For reference, the I/O banks 34 and 35 are shown along with the global (BUFG), the horizontal (BUFH), the regional (BUFR) and the I/O (BUFIO) clock buffers.



(a) (b)

Figure 5.12: The physical implementation of the separation of the ADC data bus clock. (a) A 3D view showing the LVDS ADC data bus outlined in a orange-dashed line. Outlined in teal is the ADC and outlined in beige is the FMC Connector. (b) A 2D view highlighting the "ADC_CLK" to "CHA_CLK' and "CHB_CLK" transition. The red traces are located on the top (RF Signal 1) layer and the blue traces are located on the bottom (RF Signal 2) layer.

The physical implementation of the ADC data bus is shown in Figure 5.12. Here, Figure 5.12a shows the layout of the full data bus. Figure 5.12b highlights the ADC reference clock traces being divided from "ADC_CLK" to "CHA_CLK" routed to bank 35 and "CHB_CLK" routed to bank 34. These traces are 100-Ω differential lines where the load impedance is formed by two 100-Ω impedance lines in parallel (i.e., the load impedance termination is now 50-Ω). The ADC comes with a mode which doubles the strength of the LVDS buffer to support 50-Ω differential termination [18]. By doing this, it ensures that the ±350 mV differential voltage required by the two LVDS receivers are maintained. The ADC mode doubles the current source to compensate for the decrease in load resistance. The ADC output buffer impedance behaves like a source-side series termination; therefore, absorbing reflections from the receiver end with a 100-Ω termination resistor helps improve signal integrity [18]. The meandering lines (the ADC Data Bus traces shown in Figure 5.12a) are used to maintain trace length tolerances of the LVDS data bus and clock as specified by the ADC datasheet [18].

5.6 Conclusions

In this chapter, the Equivalent-Time Sampling Receiver for the UWB pulsed radar system is presented. The receiver is designed to easily mate with most FPGA development boards through the VITA and ANSI standard FMC interface. The theory of its operation has been discussed along with an overview of the component choices. The critical development presented here is the design of the sample clocking network behind the dual-channel receiver. A working prototype and a fabricated PCB are shown. The design of the microwave interconnects is discussed. Future work to the receiver must focus on the evaluation of its dynamic range, jitter and noise performance.

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Chapter 6

Field-Programmable Gate Array (FPGA) Design and Control

6.1 Introduction

The field-programmable gate array (FPGA) control of the ultra-wideband (UWB) pulsed radar system is critical for the integration of all components. In this chapter, the design choices in using the Digilent Zedboard FPGA [1] are discussed. The design is broken down into two major sections: i) a high-level hardware descriptive language (HDL) design of the programmable logic (PL), and ii) the design of the processing system (PS) software embedded on the built-in microprocessor. The ability to utilize the built-in microprocessor functions and to perform real-time data acquisition with the PL make the control of the UWB Pulsed Radar system possible. The majority of the work presented here addresses the implementation of the programmable logic (PL). This effort involves: i) the data acquisition and storage of the analog-to-digital converter (ADC) data, ii) the synchronization and triggering of the transmitter, and iii) the implementation of the equivalent-time sampling process. Shown is the software application running on the processing system (PS) section of the Zynq-7020 system

on a chip (SoC). The software functions are discussed and proposed is the software stack-up with room for future expansion. Finally, presented are the first preliminary results from the UWB Pulsed Radar System.

6.2 Xilinx Zynq-7020 System on a Chip (SoC)

The FPGA chosen for the design is the Digilent Zedboard which contains a Zynq-7020 SoC. The Zedboard is chosen due to its ability to readily supply Gigabit Ethernet and USB connectivity along with access to a low pin count (LPC) (160-pin) FPGA magazine card (FMC) interface for daughter board development. These abilities make the board ideal for rapid prototyping and proof-of-concept development.

The Zynq-7020 chip provides a complete SoC package containing a programmable logic (PL) section and a processing system (PS) section. The chip has a maximum operating frequency up to 667 MHz (speed grade -1). The PL shares the same 7-series programmable logic as the Xilinx Artix-based devices [2]. The 7020 contains 85K logic cells, $52,300$ lookup tables (LUTs), and $106,400$ flip-flops which enables large and complex PL designs. The dual-core Advanced RISC Machine (ARM)* Cortex-A9 central processing units (CPUs) are the heart of the PS section. The ARM CPUs are embedded as a hard silicon core† which includes on-chip memory, external memory interfaces and a diverse set of peripheral interfaces (i.e. Gigabit Ethernet, USB, serial peripheral interface (SPI), inter-integrated circuit (I^2C), etc.) [2]. An overview of the functional block diagram for the Xilinx Zynq-7000 series SoC can be seen in Figure 1-1 from [3]. The diagram shows the interconnects within the PS section of the hard silicon core containing the ARM CPUs along with their built-in peripherals. The

*RISC stands for reduced instruction set computing.

†Implemented as a fixed hardware application-specific integrated circuit (ASIC) core within the silicon fabric of the chip. These are not a part of the PL and therefore cannot be re-defined at the hardware level.

interconnects with the PL section are shown at the bottom.

The Zynq-7020 chip has access to 512 MB[‡] (512 MiB) of DDR3[§] memory that is directly accessible though the ARM CPUs and the PL. Allowing the PL to handle and store the real-time data directly into memory. While at the same time, the PS can configure, control and transmit the data to the host computer.

A calculation of the expected data rate and amount of data is used to validate if the memory depth of the board is sufficient. For this calculation, it is assumed that the ADC is operating at a sampling frequency of 200 MHz ($f_\mathrm{s} = 1/t_\mathrm{s}$, where t_s is the sampling period) and that both channels operate simultaneously. Each channel of the ADC generates a 16-bit value per sample. As a result, the required data rate (r) for the two channels (concatenated together) is 32-bits per sample. Given the desired pulse repetition frequency (PRF) of 1 MHz, corresponding to a pulse period (t_p) of 1 μs, the number of samples per sub-sampled pulse (N) must be

$$N = \frac{t_\mathrm{p}}{t_\mathrm{s}} = t_\mathrm{p} f_\mathrm{s} = (1 \times 10^{-6})(200 \times 10^{6}) = 200 \text{ samples/pulse}. \tag{6.1}$$

The amount of data (D_pulse) generated in one sub-sampled pulse is

$$D_\mathrm{pulse} = rN = (32)(200) = 6400 \text{ bits/pulse} = 800 \text{ B/pulse}^{\P}. \tag{6.2}$$

[‡] *Mega*-bytes [MB] does not follow the standard SI prefix notation. Memory capacity is often defined as a multiple power of two due to the binary representation (i.e $2^{10} = 1,024$ bytes [B], where 1 B = 8 bits). However, confusion has resulted from the use of the SI prefixes (*kilo*- [k] and *mega*- [M]) being used interchangeably for their decimal multipliers (10^{3n}) or their binary multipliers (2^{10n}), where $n = 1, 2, 3, ..., 6$. Defined in [4] are the standard notations for binary multiplier prefixes. These notations are adopted here. The binary prefix notations are: *kibi*- [Ki] for $2^{(10)1} = 1,024$ and *mebi*- [Mi] for $2^{(10)2} = 1,024^2 = 1,048,576$.

[§] DDR3 stands for double data rate type 3. The DDR3 memory is a type of synchronous dynamic random access memory used for volatile system storage.

[¶] B stands for bytes, where 1 B = 8 bits

An equivalent-time sampling rate (f_{eq}) of 10 giga-samples per second (GSPS) or 20 GSPS has an equivalent-time sampling period (t_{eq}) of 0.1 ns or 0.05 ns, respectively. Therefore, the number of sub-sampled pulses (M) required per pulse reconstruction is

$$\begin{aligned} M_{10\text{ GSPS}} &= \frac{t_{\text{s}}}{t_{\text{eq}}} = \frac{1}{f_{\text{s}} t_{\text{eq}}} \\ &= \frac{1}{(200 \times 10^{6})(0.1 \times 10^{-9})} = 50 \text{ pulses/reconstruction}, \end{aligned} \tag{6.3}$$

or

$$\begin{aligned} M_{20\text{ GSPS}} &= \frac{t_{\text{s}}}{t_{\text{eq}}} = \frac{1}{f_{\text{s}} t_{\text{eq}}} \\ &= \frac{1}{(200 \times 10^{6})(0.05 \times 10^{-9})} = 100 \text{ pulses/reconstruction}. \end{aligned} \tag{6.4}$$

As a result, the amount of data per reconstruction (D_{reconst}) is

$$\begin{aligned} D_{\text{reconst}}^{10\text{ GSPS}} &= M_{10\text{ GSPS}} D_{\text{pulse}} \\ &= (50)(800) \\ &= 40000 \text{ B/reconst} = 39.0625 \text{ KiB/reconstruction}^{\|}, \end{aligned} \tag{6.5}$$

and

$$\begin{aligned} D_{\text{reconst}}^{20\text{ GSPS}} &= M_{20\text{ GSPS}} D_{\text{pulse}} \\ &= (100)(800) \\ &= 80000 \text{ B/reconst} = 78.125 \text{ KiB/reconstruction}^{\|}. \end{aligned} \tag{6.6}$$

$^{\|}$*kibi*-byte [KiB], where 1 KiB $= 2^{10} = 1,024$ bytes.

At the given pulse period (t_{p}) of 1 μs, the acquisition time for one pulse reconstruction based on 10 GSPS ($t_{10\ \mathrm{GSPS}}$) and 20 GSPS ($t_{20\ \mathrm{GSPS}}$) is

$$t_{10\ \mathrm{GSPS}} = M_{10\ \mathrm{GSPS}} t_{\mathrm{p}} = (50)(1 \times 10^{-6}) = 50\ \mu\mathrm{s/reconstruction}, \tag{6.7}$$

and

$$t_{20\ \mathrm{GSPS}} = M_{20\ \mathrm{GSPS}} t_{\mathrm{p}} = (100)(1 \times 10^{-6}) = 100\ \mu\mathrm{s/reconstruction}, \tag{6.8}$$

respectively. Then, the FPGA must be capable of handling a data rate (r_{reconst}) of

$$r_{\mathrm{reconst}} = \frac{D_{\mathrm{reconst}}^{10\ \mathrm{GSPS}}}{t_{10\ \mathrm{GSPS}}} = \frac{D_{\mathrm{reconst}}^{20\ \mathrm{GSPS}}}{t_{20\ \mathrm{GSPS}}} = 0.78125\ \mathrm{KiB}/\mu\mathrm{s} = 762.94\ \mathrm{MiB/s}. \tag{6.9}$$

In the proposed solution, the DDR3 memory acts as a data buffer. The PL section transfers the data to the memory, whereas the PS section receives and offloads the data. It is not possible to use the full amount of DDR3 memory for data storage because the PS section requires some memory for its operating system. However, based on the worst-case acquisition times provided in Table 3.1 in Chapter 3, the amount of DDR3 memory is sufficient. Given (6.9) and the worst case acquisition time (t_{acq}) of 78 ms the system would require a minimum of 59.50 MiB ($r_{\mathrm{reconst}} \cdot t_{\mathrm{acq}}$) of DDR3 memory.

The Xilinx FPGA has been chosen because the PS and PL designs had to be carried out without knowing the number of reconstructed pulses to be averaged. Within the worst case acquisition time (t_{acq}) of 78 ms, the acquired number of reconstructed pulses ($O_{10\ \mathrm{GSPS}}$ and $O_{20\ \mathrm{GSPS}}$) is

$$O_{10\ \mathrm{GSPS}} = \frac{r_{\mathrm{reconst}} t_{\mathrm{acq}}}{D_{\mathrm{reconst}}^{10\ \mathrm{GSPS}}} \approx 1597\ \text{reconstructed pulses}, \tag{6.10}$$

and

$$O_{20\text{ GSPS}} = \frac{r_{\text{reconst}} t_{\text{acq}}}{D_{\text{reconst}}^{20\text{ GSPS}}} \approx 798 \text{ reconstructed pulses}, \tag{6.11}$$

given an equivalent-time sampling rate of 10 GSPS and 20 GSPS, respectively. Achieving a minimum of 10 to 100 sequentially reconstructed pulses is possible.

6.3 Programmable Logic (PL) Design

The PL design is what makes the system integration come together. The development of the FPGA PL design has been a long and tedious process. The design flow within the software tools provided by the FPGA industry is not straightforward. Every tool is unique to the FPGA vendor with its challenges and limitations on the implementation processes although the low-level Verilog programming is the same. Documentation and examples are usually available; however, they are scattered through the thousand-page Technical Reference Manual [3] and the hundreds of subsequent User Guides [5–8], Application Notes [9–12], Product Guides [13–19] and Product Specification documents [1, 2, 20]. Countless hours have been spent on the Xilinx, Texas Instruments and Analog Devices support forums [21–23]. Here, direct interaction with FPGA designers and experts from the vendors, academics and the community is possible. In addition, attending undergraduate- and graduate-level courses on FPGA technology assisted in comprehending the task at hand and developing a strategy for its solution.

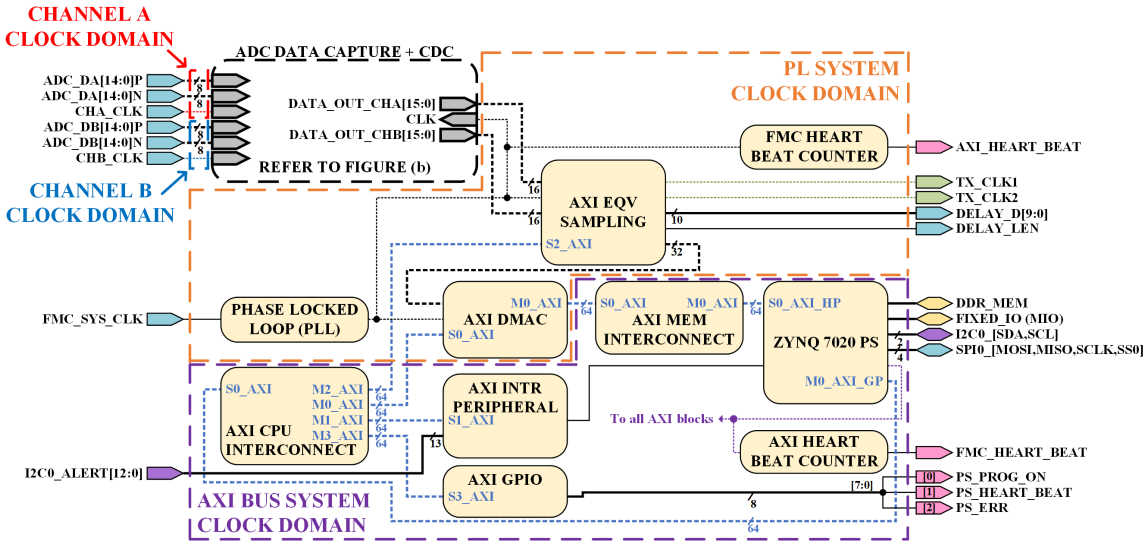
The PL design here is based on a Xilinx FPGA reference design for a similar ADC chip provided by Analog Devices [24]. The HDL and software examples are available in their GitHub repositories [25] and [26]. In addition, Xilinx application notes on low voltage differential signaling (LVDS) reception within the 7-series FPGAs were

used [9–11].

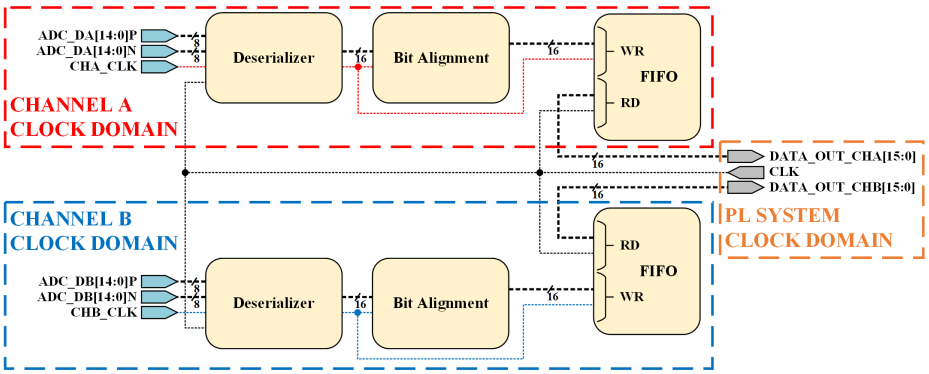
Figure 6.1 is a high-level HDL block diagram of the design implementation on the Zynq-7020 chip. This figure is referred to throughout this chapter to explain each step of the design process. The following convention is used for reading this figure. The data flow typically follows from left to right, i.e., input pins are to the left of the blocks and their outputs are to the right. The coloured signal ports (blue, green, purple, pink, yellow) at the far left and far right are the input/output (I/O) of the FPGA itself. These are connected directly to the pins and follow the same data flow convention unless their pointing direction indicates otherwise. Figure 6.1a illustrates the full PL design, whereas Figure 6.1b is only the ADC data capture and clock-domain crossing (CDC). Figure 6.1b can be found within the black dashed box of Figure 6.1a. A legend is provided in Figure 6.2 for reference.

In order to facilitate communication between the PS and PL, an Advanced Extensible Interface (AXI) bus is used [6]. Blocks in Figure 6.1 with "AXI" in their name use this bus (thick blue dashed line) to communicate with the ZYNQ 7020 PS block. It is a master/slave model of communication where ports designated with "M#_AXI" are the masters and pins with "S#_AXI" are the slaves. The AXI buses are synchronous to the 100 MHz clock (thin dashed purple line) provided from the ZYNQ 7020 PS block.

The design is comprised of a mixture of pre-made IP cores provided by Xilinx, Analog Devices or custom-built by the author. IP cores are pre-built HDL packages provided and validated by vendors in order to accelerate FPGA development. The main tasks discussed here are: the connection of these IP cores, the definition of their role, and the design of the custom IP cores. Here, the primary interest is the custom AXI Equivalent Sampling IP core (refer to "AXI Eqv Sampling" in Figure 6.1a). The challenge is working across multiple clock domains; which are a group of data signals



(a)



(b)

Figure 6.1: The HDL block diagram of the PL design used in the Zynq-7020 Chip. (a) The full system design that shows the interconnects of all IP cores. (b) The ADC data capture and clock-domain crossing (CDC) to the common PL system clock domain. The block diagram in (b) is a subsection within the block diagram of (a). This is noted in (a) by the "ADC DATA CAPTURE + CDC" block. Figure 6.2 contains the legend for reference. Refer to subsection 6.3.1 for all IP core definitions and functionality.

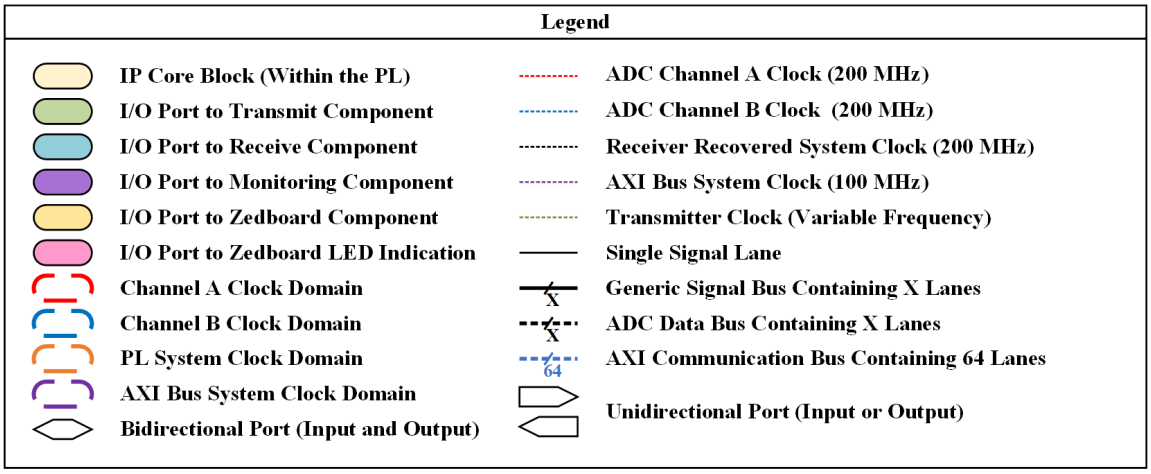


Figure 6.2: A reference legend of the symbols and notations used in Figure 6.1.

that are synchronous to a common clock. These common clocks are asynchronous between domains as their phase relationship is unknown and their frequencies may differ. Crossing between clock domains requires care to avoid metastability issues in the data and ensuring its integrity. In the design, there are four key clock domains: i) the channel A clock domain, ii) the channel B clock domain, iii) the PL system clock domain, and iv) the AXI bus system clock domain.

6.3.1 IP Core Definitions

The following section provides each IP core's definitions and functionality with respect to their use in Figure 6.1. They are broken down into their respective clock domains.

Channel A and Channel B Clock Domain

The IP cores contained in the channel A and B clock domains are the same. Each channel consists of three IP cores and is shown in Figure 6.1b. The channel A clock domain is outlined with a red-dashed line, whereas the channel B clock domain

is outlined with a blue-dashed line. The channel A and channel B clock domain primarily contain the data reception from each ADC channel. The following are the definitions and the functionality of each IP core for one channel reception.

Deserializer: The role of the deserializer is a parallelization process which transfers a serialized data bus into a parallelized data bus (refer to [5, 13] for the IP core specifications). Here, the deserializer is the first block which receives the serialized data stream from a single ADC channel. The ADC transfers 16 bits over a 100-Ω differential 8 lane bus tied to a reference clock (channel A's reference clock is CHA_CLK, whereas channel B's is CHB_CLK; refer to Figure 6.1b). Data bits are transferred on both the rising and falling edges of the reference clock, resulting in 2 bits on one lane per clock cycle (refer to ADC Data Input from Figure 6.3). This type of serialization is called double data rate (DDR). The block recovers the individual data bits and distributes them across the new 16 lane data bus (i.e. one bit per lane). The even bits are acquired on the rising edge of the clock (assigning them to lanes 1 to 8), whereas the odd bits are captured on the falling edge (assigning them to lanes 9 to 16). A new recovered reference clock is provided from the ADC's reference clock and the serialization process (the recovered clock frequency is 200 MHz). An example of the single-channel data stream before and after the deserializer is shown in Figure 6.3 (refer to ADC Data Input and Deserializer Output).

Bit Alignment: The bit alignment IP core is the first of the custom designed IP cores. Its role is to re-arrange the 16 data lanes generated at the output of the deserializer. The core re-distributes the lanes so that they are in bit sequential order (i.e., the least significant bit is in lane 1 and the most significant bit is in lane 16). As shown in Figure 6.3, the deserializer output lumps together the even bits in lanes 1 to 8 and the odd bits in lanes 9 to 16. A re-distribution process is required so that

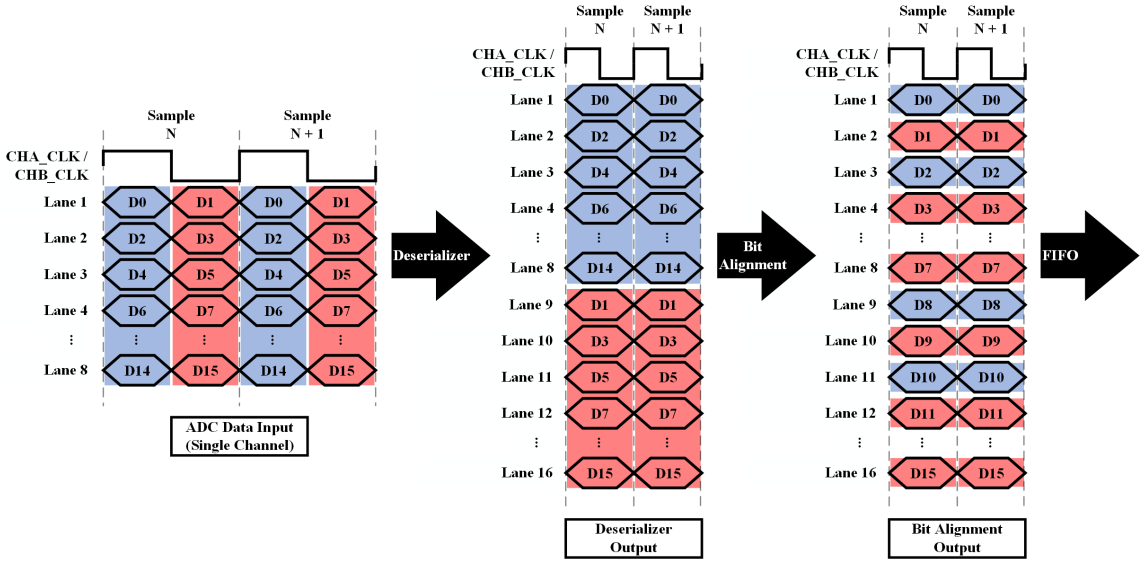


Figure 6.3: The single channel data processing within the channel A and B clock domains.

the data is structured correctly across the data bus. This is illustrated in Figure 6.3 (refer to Deserializer Output and Bit Alignment Output).

FIFO: The first-in, first-out (FIFO) blocks are used as a small-depth (16 writes and reads deep) asynchronous CDC FIFO [14]. One FIFO is used per ADC channel's clock domain (refer to Figure 6.1b). Their purpose is to transfer the data stream from one clock domain to another. Therefore, bringing the two asynchronous ADC channel clock domains to a common synchronous clock domain (PL system). The asynchronous FIFO implements independent read and write clocks. The CDC is accomplished using a clock synchronizer with three stages. Each channel's data stream writes to their respective domain's FIFO (using their CHA_CLK or CHB_CLK clocks). The FIFOs read then occurs using the PL system clock domain's clock, which is the Equivalent-Time Sampling Receiver's clock recovered using a phase-locked loop (PLL). The depth of the FIFO is kept short to minimize the data delay to the equivalent-time sampling IP core.

PL System Clock Domain

The PL system clock domain is where the signals within the equivalent-time sampling procedure synchronizes to the transmitting and receiving functionalities. Without this synchronized domain, the signal reconstruction based on equivalent-time sampling is not possible. This domain contains the following IP cores and their roles.

Phase-Locked Loop (PLL): The PLL [15] recovers the Equivalent-Time Sampling Receiver system clock and distributes it to the FPGA PL fabric. Its location is shown in Figure 6.1b. The recovered clock has the same frequency (f_s = 200 MHz) and phase as the receiver's clock before any group delay from the programmable delay chip (PDC). As a result, the equivalent-time sampling process (contained within the "AXI Eqv Sampling" block) is synchronous with the transmitter clock signal, which triggers each new pulse. The deserializer requires this recovered clock (refer to CLK from Figure 6.1b) for the alignment of the data window (or data "eye").

AXI Eqv Sampling: The "AXI Eqv Sampling" IP core implements the equivalent-time sampling procedure. This block is instrumental in the capabilities of the system to achieve sampling rates of 10 GSPS and 20 GSPS. It is further discussed in subsection 6.3.2.

AXI DMAC: The AXI direct memory access controller (DMAC) is a high-speed high-throughput controller intended for data transfer between the PL of the chip and the system DDR3 memory [27]. The AXI DMAC is provided by Analog Devices [25–27]. This IP core crosses from the PL system clock domain over to the AXI bus system clock domain by implementing a small FIFO (similar to the FIFOs from the channel A and B CDC). The DMAC output uses the high-performance AXI bus at 100 MHz to directly access the DDR3 memory. The memory write addresses are allocated by the ARM CPUs and an acquisition (a write process to memory) is triggered once

per iteration through the software program. Memory allocation is required as the locations share between the IP core and the ARM CPUs. Due to the fact they are asynchronous, a scenario can occur where the DMAC has partially written an acquisition while the CPU pulls and transmits the allocated memory segment. This asynchronous behaviour leads to a corrupt measurement where the data splits over two acquisitions. Therefore, the simplest solution is to suspend the ARM CPU operations until the "transfer complete" flag is raised by the DMAC.

FMC Heart Beat Counter: The FMC heart beat counter is used for debugging purposes only. It indicates to the user the status of the Equivalent-Time Sampling Receiver's clock. The custom-designed IP core is for clock division using a 32-bit counter. The result is a division in the 200 MHz PL system clock which blinks a light every half second (i.e. the counter counts to 100 million at a clock period of 5 ns).

AXI Bus System Clock Domain

The AXI bus system clock domain facilitates the AXI bus communication between the PL and PS sections of the chip. This enables PS control of the IP cores on the AXI bus. The IP cores in this domain are listed below along with their role.

ZYNQ 7020 PS: The ZYNQ 7020 PS IP core [16] contains all the interconnects available from the built-in ARM CPUs (PS section) to the PL (all capabilities are shown in Figure 1-1 from [3]). The built-in peripheral controllers are located here for I^2C, SPI, Gigabit Ethernet and memory interconnects along with all other available controllers. As shown in Figure 6.1a, this IP core is used for the I^2C and SPI buses routed to chips on the Equivalent-Time Sampling Receiver. It utilizes the general purpose (GP) AXI master controller (M0_AXI_GP) to control the AXI IP cores in the PL. The high-performance (HP) AXI slave controller (S0_AXI_HP) is for direct

memory access through the "DDR_MEM' data bus, which is utilized by the AXI DMAC IP core. Finally, the Gigabit Ethernet is accessible through the "Fixed_IO (MIO)" data bus.

AXI CPU Interconnect: The AXI CPU interconnect connects one or more memory-mapped slave AXI buses to one or more memory-mapped master AXI buses [3, 17]. In this case (refer to Figure 6.1a), the interconnect connects the GP AXI bus master (M0_AXI_GP) to the remaining slave AXI IP cores (i.e., the AXI Eqv Sampling, the AXI DMAC, the AXI intr peripheral and the AXI general purpose input output (GPIO)). Each slave IP core is assigned a memory-mapped address allowing each to be accessed independently.

AXI Mem Interconnect: The AXI Mem Interconnect is the exact same IP core as the AXI CPU interconnect [3,17]. The only exception is that it now uses the HP AXI bus slave controller (S0_AXI_HP) for direct memory access. This connects the AXI DMAC IP core to the ZYNQ 7020 PS core. The direct memory access is provided through the ZYNQ 7020 PS using the programmable logic to memory interconnect [3].

AXI Intr Peripheral: The AXI intr peripheral is an interrupt controller used to expand the number of interrupt ports available to the ARM CPUs. Its purpose is to receive multiple interrupt inputs from peripheral devices and merge them into a single interrupt output to the system processor [18]. Here, "intr" is used as a short-form for interrupt. This block monitors the I^2C interrupts from the Equivalent-Time Sampling Receiver for power and temperature monitoring along with fan control. The interrupt controller simplifies the logic required for routine interrupt handling as there are 13 interrupts provided by the receiver printed circuit board (PCB).

AXI GPIO: The AXI GPIO IP core [19] is a general purpose input output (GPIO) used to toggle indicators as per the status of the PS program. These indicators are for debugging purposes to ensure that the program on the ARM CPUs is: i) on

and programmed (both the PL and PS), ii) iterating through its processes, and iii) error-free.

AXI Heart Beat Counter: The AXI heart beat counter is used for debugging purposes only. It indicates to the user the status of the AXI bus communication clock. The IP core is identical to the FMC heart beat counter except for the light indicator blinking once a second. A one-second cycle is due to the block counting to 100 million with a clock period of 10 ns (the 100 MHz AXI bus clock).

6.3.2 Equivalent-Time Sampling Procedure

The equivalent-time sampling procedure is accomplished in the AXI Eqv Sampling IP Core. Figure 6.4 shows how the data is passed through the IP core and is manipulated. Following the ADCs data capture and CDC (refer to Figure 6.1b), the data is passed into the equivalent-time sampling block (refer to AXI Eqv Sampling in Figure 6.1b). This data stream is shown in Figure 6.4a as the AXI Eqv Sampling IP core data input. Here, each 16-bit sample from channel A and channel B is represented by $A_{m,n}$ and $B_{m,n}$, respectively, where m is the pulse index ranging from 1 to M and n is the sample index ranging from 0 to N. M represents the number of sub-sampled pulses and N represents the number of samples per sub-sampled pulse.

At the beginning of each pulse, the equivalent-time sampling block replaces the first data sample (i.e., $A_{m,0}$ and $B_{m,0}$) with a header ($H_{m,0}$). This header is inserted to indicate a new sub-sampled pulse. A counter (internal to the IP core) counts the n sample indices on the positive edge of the input clock until N samples are acquired; this is the sample counter. Another internal counter, the pulse counter, tracks the current pulse index (m) and increments at the same clock edge where the header is inserted. The process repeats such that the sample counter counts to its threshold N

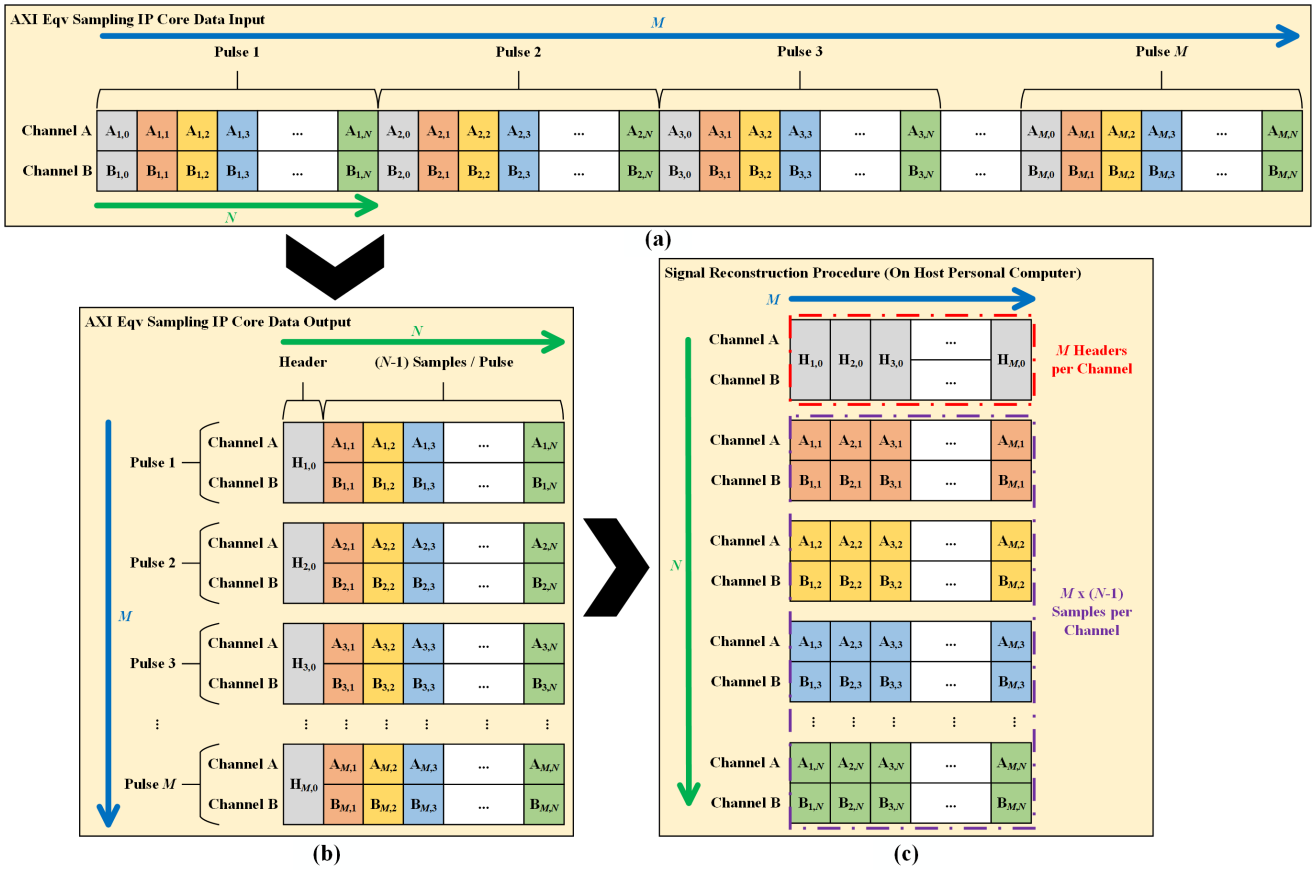


Figure 6.4: The equivalent-time sampling procedure: (a) the AXI Eqv Sampling IP core data input, (b) the AXI Eqv Sampling IP core data output, and (c) is the signal reconstruction procedure (completed on the host personal computer). Here, each 16-bit sample from channel A and channel B is represented by $A_{m,n}$ and $B_{m,n}$, respectively, where m is the pulse index ranging from 1 to M and n is the sample index ranging from 0 to N. M represents the number of sub-sampled pulses and N represents the number of samples per sub-sampled pulse. The ADC data samples $A_{m,0}$ and $B_{m,0}$ are replaced with a unique identifying header $H_{m,0}$. The data arrays are read from left to right (one row) and then from top to bottom.

and then triggers a new header insertion until all M sub-sampled pulses are acquired. The data output from the AXI Eqv Sampling IP core is shown in Figure 6.4b. This output passes along to the next IP core (refer to Figure 6.1a).

The beginning of a sub-sampled pulse is known based on the internal pulse and sample counters. The challenge is identifying the first and the last sub-sampled pulse required for a complete pulse reconstruction. A unique header is used to indicate the sub-sampled pulse index (m) so that signal reconstruction can occur. When channel A and channel B samples ($A_{m,n}$ and $B_{m,n}$) are concatenated together, a 32-bit wide bus is created ($A_{m.n}$ uses bits 0 to 15 and $B_{m,n}$ uses bits 16 to 31). Therefore, 32-bits can be used to create a header ($H_{m,0}$) which replaces both samples $A_{m,0}$ and $B_{m,0}$. The header ($H_{m,0}$) format is broken into two 16-bit variables: i) the current pulse number (PULSE_ID) which uses bits 0 to 15, and ii) a unique identifier (UNIQUE_ID) which uses bits 16 to 31. Here, the PULSE_ID is automatically set to the current (mth) pulse index, whereas the UNIQUE_ID can be user-defined. In this case, a 16-bit hexadecimal value of AAAA is chosen as its binary representation is an alternating sequence of zeros and ones ($16'\text{hAAAA} = 16'\text{b1010\_1010\_1010\_1010}$)** and its decimal representation using signed two's complement is -21846. This makes it a known value to look for in conjunction with the PULSE_ID.

Two other parallel processes occur at the same clock edge where the header is inserted. First, the transmitter clocks (signals tx_clk1 and tx_clk2 from Figure 6.1a) are toggled to trigger new pulses by the two pulse generators. The two output transmitter clocks allow for independent control of the trigger and clock period of the two pulse

**Representation of numeric literals in verilog (a type of FPGA HDL) typically follow these conventions: <*size*>′<*radix*> *value* (where "<>" are optional). <*size*> is the number of binary bits the number contains. <*radix*> is the radix or base of the number (i.e., binary – ′b, hex – ′h and decimal – ′d. *value* is any number supported by the radix (i.e., binary legal characters are '0', '1'; hex legal characters are '0-9', 'a-f', 'A-F'; and decimal legal characters are '0-9'). The underscore "_" is a separator used to improve the readability (i.e., $8'\text{d160} = 8'\text{hA0} = 8'\text{b1010\_0000}$).

generators. As discussed in Chapter 3, the system is dual-channel that contains two transmitters. Therefore, separate control of the transmitting clock enables control over each channel. The input clock of 200 MHz is used to obtain a 1 MHz clock signal for each transmitter. The 200 MHz input clock is divided by 200 using a separate internal counter, which toggles between a low logic level state upon reset and a high logic level on the count of 100 out of 200. Using the recovered receiver reference clock (refer to Figure 6.1a) the PL system clock domain synchronizes the two transmitter clocks.

The second parallel process, which occurs at the same clock edge where the header is inserted, controls the PDC. This second process controls the group delay applied by the PDC to the ADC clock in order to shift the sampling position in time. When the header is inserted at the clock's rising edge the latch-enable pin to the PDC (refer to DELAY_LEN signal from Figure 6.1a) goes low enabling the new delay value to be written. The latch enable returns to its nominal high state on the next rising clock edge. The delay value is written to the PDC chip using the 10-bit wide DELAY_D[0:9] digital bus (refer to Figure 6.1a). To maintain the delay value, a separate 10-bit counter that increments after N samples. The starting value and incremental step delay value used by this counter are configurable via the PS software, which writes to registers available in the IP core using the AXI bus. These configurable registers enable dynamic control over the equivalent-time sampling rate. The default starting value is 0 ps, which results in no group delay applied. An incremental step delay of either 100 ps or 50 ps is applied while the latch is low to achieve an equivalent-time sampling rate of 10 GSPS or 20 GSPS, respectively. Here, the incremental delay is repeated M times until the PDC is reset to its starting value. The insertion of the header is the ideal location for this to occur as changing the delay in the clock can result in instability in the ADC sample.

Signal reconstruction occurs after data offload to the host personal computer. Here, the header is used to identify the start of a new signal reconstruction (i.e., pulse index $m = 1$) and to identify the subsequent sub-sampled pulses. Shown in Figure 6.4c under the Signal Reconstruction Procedure is this process. Arranging the equivalent-time sampled data into a channel A and channel B matrices of size M-by-N, the signal reconstruction is the transpose of the respective matrix. For example, let the matrix $\mathbf{A}$ contain the channel A header and samples presented in Figure 6.4b,

$$\mathbf{A} = \begin{bmatrix} H_{1,0} & A_{1,1} & A_{1,2} & \cdots & A_{1,N} \\ H_{2,0} & A_{2,1} & A_{2,2} & \cdots & A_{2,N} \\ H_{3,0} & A_{3,1} & A_{3,2} & \cdots & A_{3,N} \\ \vdots & \vdots & \ddots & & \vdots \\ H_{M,0} & A_{M,1} & \cdots & \cdots & A_{M,N} \end{bmatrix}. \tag{6.12}$$

Taking the transpose of $\mathbf{A}$ results in the reconstructed pulse matrix ($\mathbf{A}_{\text{reconst}}$, presented in Figure 6.4c) of size N-by-M,

$$\mathbf{A}_{\text{reconst}} = \mathbf{A}^{\text{T}} = \begin{bmatrix} H_{1,0} & H_{2,0} & H_{3,0} & \cdots & H_{M,0} \\ A_{1,1} & A_{2,1} & A_{3,1} & \cdots & A_{M,1} \\ A_{1,2} & A_{2,2} & A_{3,2} & \cdots & A_{M,2} \\ \vdots & \vdots & \ddots & & \vdots \\ A_{1,N} & A_{2,N} & \cdots & \cdots & A_{M,N} \end{bmatrix}, \tag{6.13}$$

which when unwrapped row by row results in the reconstructed signal. Applying the same process to the matrix $\mathbf{B}$ which contains the channel B header and samples (presented in Figure 6.4b) reconstructs channel B.

The IP core works under the assumption that all external propagation delays are

the same. However, this is not the case because each IP before the AXI Eqv Sampling suffers logic delays along with different trace lengths, which may not be delay matched. The result is a delay in the location of the samples of the sub-sampled pulse relative to the transmitter clocks (signals tx_clk1 and tx_clk2 from Figure 6.1a) trigger edge. It was found experimentally that a direct feed from the trigger port to the ADC input has a measured delay of approximately 33 samples. Nonetheless, pulse reconstruction is still possible due to the repetitive and synchronous behaviour of the system. At the completion of the Mth pulse, the 1st pulse is repeated allowing for continuity in the data stream.

The process is not without its challenges as the clock tied to the ADC data output shifts with respects to the system clock. As a result, after the Mth pulse, the group delay of approximately 5 ns (due to the PDC) is reset to 0 ns. This reset causes instability in the clock due to a nearly 360° phase shift where part of a clock cycle is missed. The data stream then becomes unstable and is not ready to be read by the time it reaches the CDC FIFOs (see Figure 6.1b). The FIFO then runs empty. Currently, the FIFO read/write controls are used to prevent a read while the FIFO is empty. However, the instability in the data waveform measurements still exist. The current solution is to shift the pulse to begin after the position in time where the instability occurs. This shift allows for the removal of this logic glitch in the measured waveform by time gating but does not resolve the root cause.

Future work should look at alternative methods of implementing the incremental counter for the PDC delay so that a sudden loss in group delay does not happen. Calibration methods for de-embedding the propagation delays in the internal logic must be developed. Finally, the current PDC [28] has a large delay variance which is temperature sensitive. Alternative PDC chips should be explored that guarantee delay values over a given temperature range.

Table 6.1: Zynq-7020 FPGA resource utilization report.

Resource	Utilization (units)	Available (units)	Utilization (%)
LUT	5,267	53,200	9.9 %
LUTRAM	609	17,400	3.50 %
FF	8,294	106,400	7.80 %
BRAM	6.5	140	4.64 %
IO	79	200	39.5 %
BUFG	6	32	18.5 %
PLL	1	4	25 %

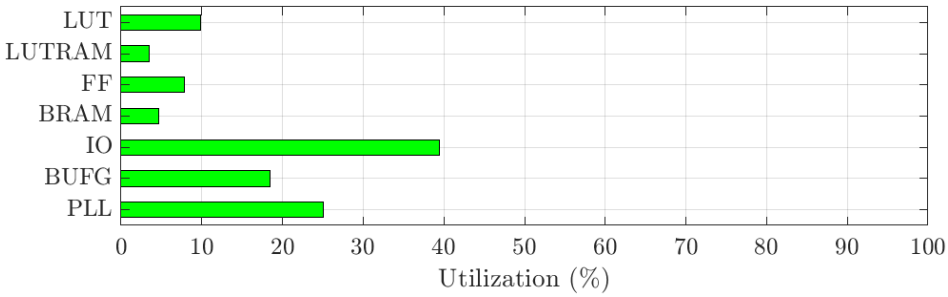


Figure 6.5: Zynq-7020 FPGA resource utilization percentage.

6.3.3 FPGA Resource Usage

The resource distribution of the designed FPGA PL control is shown in Table 6.1. The respective percentages are plotted in Figure 6.5. As shown, the design is not resource heavy. It is I/O constrained by the number of I/O routed to the FMC connector. This can also be seen in the FMC pinouts for the receiver and zedboard shown in Appendix A and Appendix B, respectively. Since the design is not resource heavy, future work can expand the PL fabric capabilities to include averaging of measurements, real-time fast Fourier transform (FFT) along with signal-processing techniques for detection and classification.

6.4 Processing System (PS) Design

The PS design has four main tasks to manage: i) receiver state management, ii) FPGA PL configuration and control, iii) peripheral control through I^2C and SPI, and iv) data offload. The PS system contains the software which runs on the ARM CPUs in order to perform the radar tasks.

The current software implementation is on a standalone bare-metal operating system provided by Xilinx for the Zynq SoC chips [7]. This operating system comes with all required board support packages and drivers to interface the ARM cores with their internal peripherals and the developed Xilinx IP cores. Figure 6.6 shows the stack of the current software implementation (Figure 6.6a) and the intended software implementation (Figure 6.6b). Currently, the design only utilizes one of the two ARM core processors. Additionally, the standalone bare-metal operating system provides limited capabilities in the types of operations that can be easily performed by the ARM cores. Thus, the intended (i.e. goal) design is shown in Figure 6.6b, which uses both cores. At the current stage of development, one core is more than sufficient to show a working proof-of-concept system. However, for improved performance in system control and faster data acquisition; one ARM core could implement a real-time operating system which provides strict timing to operation such as data collection and storage. At the same time, a general-purpose operating system (such as Linux or similar builds provided by Xilinx) can be used for data offloading, network communication and signal pre-processing purposes. Multi-operating system support is well supported on the Xilinx platform and deserves further investigation [12]. In order to obtain a working prototype, the software stack is shown in Figure 6.6a is used, thus reducing the development time.

The bare-metal software implements all the initialization and control required by

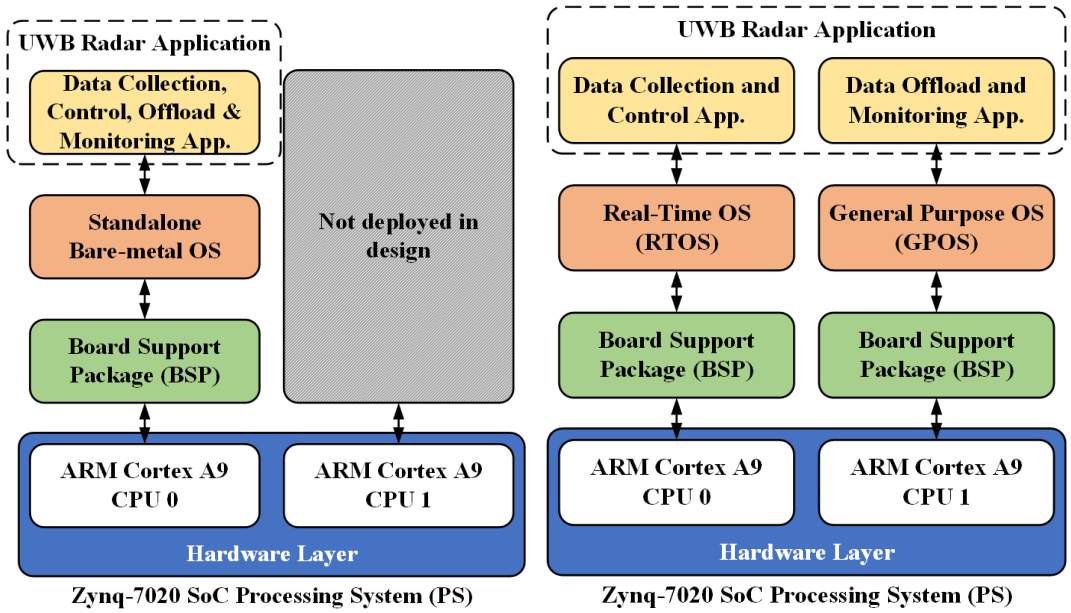


Figure 6.6: The software stack-up implemented on the Zynq 7020 PS system: (a) the current software stack, and (b) the intended software stack.

the system. It uses the built-in I^2C and SPI peripheral controllers to initialize the ADC and to configure the power monitor along with the fan controller and temperature monitor on the Equivalent-Time Sampling Receiver. The built-in Gigabit Ethernet and universal asynchronous receiver/transmitter (UART) peripherals are used to control and acquire data from the system. The UART provides only the program information that requires a low data throughput, whereas the Ethernet connection supplies the raw signal data acquired by the receiver. The bare-metal software also controls all the AXI bus registers for the IP cores. It configures the equivalent-time sampling rate and transmitter clock period for the AXI Eqv Sampling core by writing to the register within the PL. In addition, it also controls the allocated memory addresses and controls for the AXI DMAC IP core.

The use of the PS control of the Gigabit Ethernet for data offloading is a critical

design choice for the proposed system. Ethernet allows the information to be obtained fast and securely without the loss of data. However, this strategy is still not sufficient to meet the needs of the data generated by the receiver. The proposed system requires a data rate of 762.94 MiB/s (as outlined in section 6.2). Gigabit Ethernet, on the other hand, has a theoretical limit capable of transmitting 1 gigabit per second (Gbps) which is equivalent to 125 MiB/s. This limit is rarely reached in practice due to the overhead in communication protocols. The lower data transfer rate of the Ethernet results in the dropping of data packets and the loss of received signals. Future work should investigate the following methods of reducing the loss of data. i) Finding alternative solutions for data offloading that can obtain these high data rates. These could include alternative physical communication strategies such as 10 Gigabit Ethernet, universal serial bus (USB) 3.0 or USB 3.1. ii) Performing additional digital signal processing (DSP) on the data within the PL and PS sections of the FPGA. iii) Ensuring data transmission and reception is optimized and tuned on both the FPGA and signal processing module (SPM) module. This would include optimizing the management of tasks running within the FPGA in order to handle the events of lost data, as well as, the capability of the SPM module of receiving and detecting lost information.

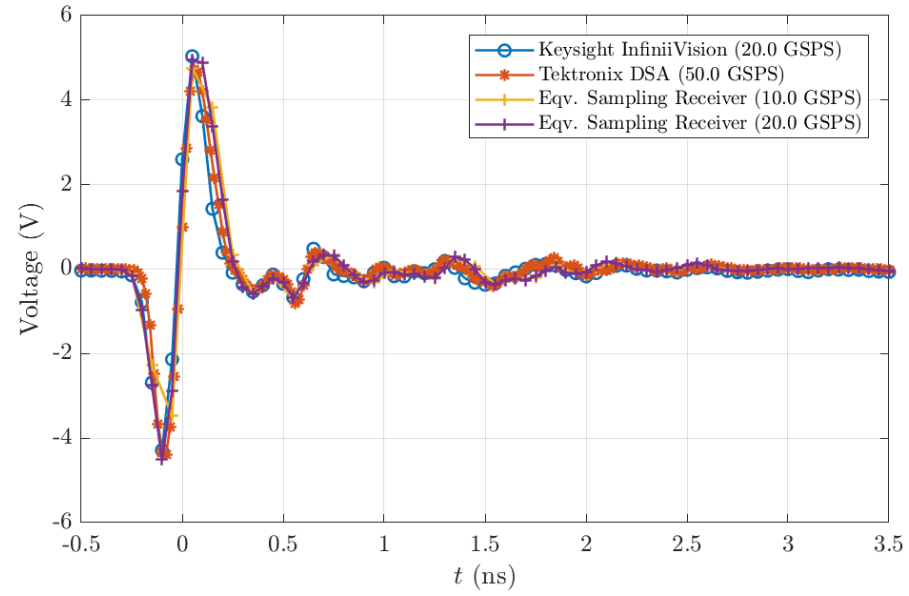
6.5 Preliminary Results of the UWB Pulsed-Radar System

The first preliminary results of an equivalently sampled signal using the proposed system are presented. A comparison made between two bench-top laboratory-grade

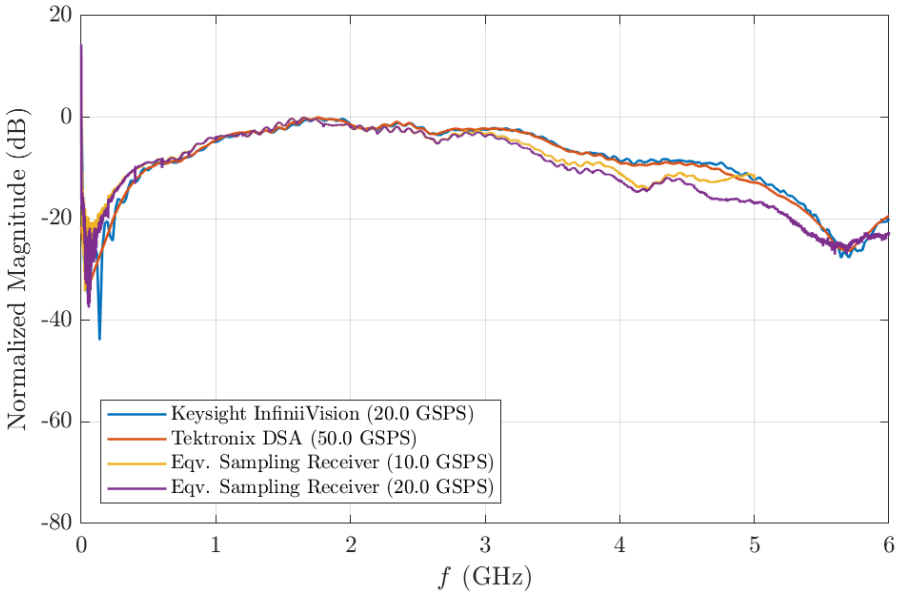
oscilloscope [29, 30] and the Equivalent-Time Sampling Receiver shows promising results. The same UWB pulse generator setup with a 20 dB directional coupler [31] is used for all four measurements. As explained in Chapter 4, a directional coupler is required to protect the input of an oscilloscope or the receiver. A 50-Ω termination loads the through-port of the directional coupler and the coupled port connects to the oscilloscope or the receiver. The pulse generator for these measurements differ from the one measured in Chapter 4 as an improvement has been made to the peak-to-peak voltage and bandwidth [32]. Presented for each instrument is an average (mean) of 128 waveforms. In all measurements, a calibration is performed for the directional coupler losses and alignment of the pulses in time. The spectral plots are normalized to their maximum spectral component (beyond the direct current (DC) component). Thus, a comparison can be made of their spectral-domain shapes. At present, a minor DC offset is seen in the measurements with our receiver due to calibration steps required for the ADC.

Figure 6.7 shows an overlay comparison in the temporal and spectral domains of all four measurements. Figure 6.8 only shows the equivalently reconstructed signal from the Equivalent-Time Sampling Receiver. Finally, Figure 6.9 and Figure 6.10 show the comparison of the spectral domain results for all four measurements. The -10 dB spectral bandwidth is calculated and shown.

There is a good agreement between the peak-to-peak voltages measured by all systems. The pulse shapes are in good agreement as well. In Figure 6.8, it is observed that the slower sampling rate misrepresents the negative main-pulse peak by nearly 1 V. However, in the spectral domain, there is a good agreement from 0.5 GHz to 3 GHz. Above 3 GHz, the frequency-domain results of the Equivalent-Time Sampling Receiver appear to attenuate faster, especially at 20 GSPS rate. There are three potential causes for this high-frequency loss: i) the balun used at the input to the



(a)



(b)

Figure 6.7: A UWB pulse shown in: (a) the time domain and (b) the frequency domain. Reconstruction is done using: i) a Keysight InfiniiVision Oscilloscope [29] (blue), ii) a Tektronix Digital Signal Analyzer (DSA) [30] (orange), and iii) the Equivalent-Time Sampling Receiver (10 GSPS - yellow, 20 GSPS - purple).

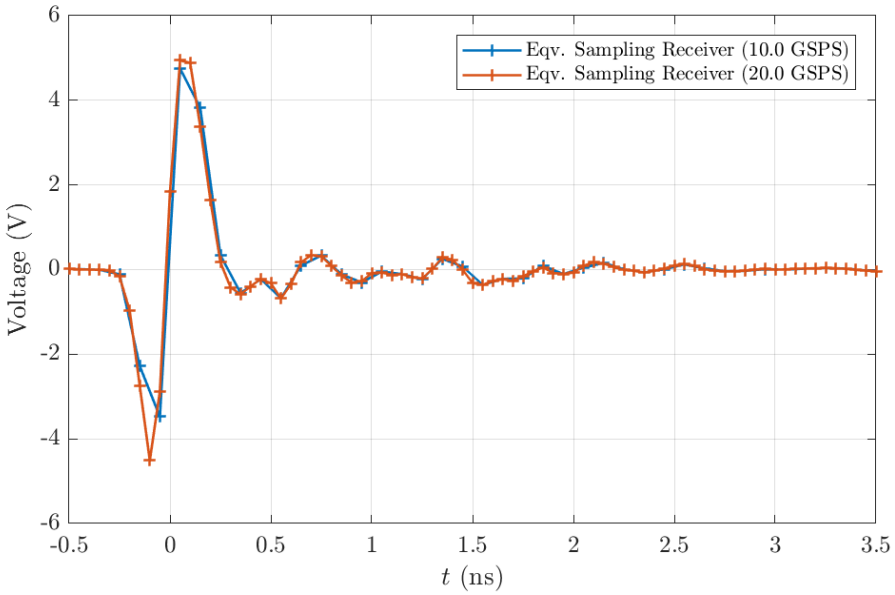
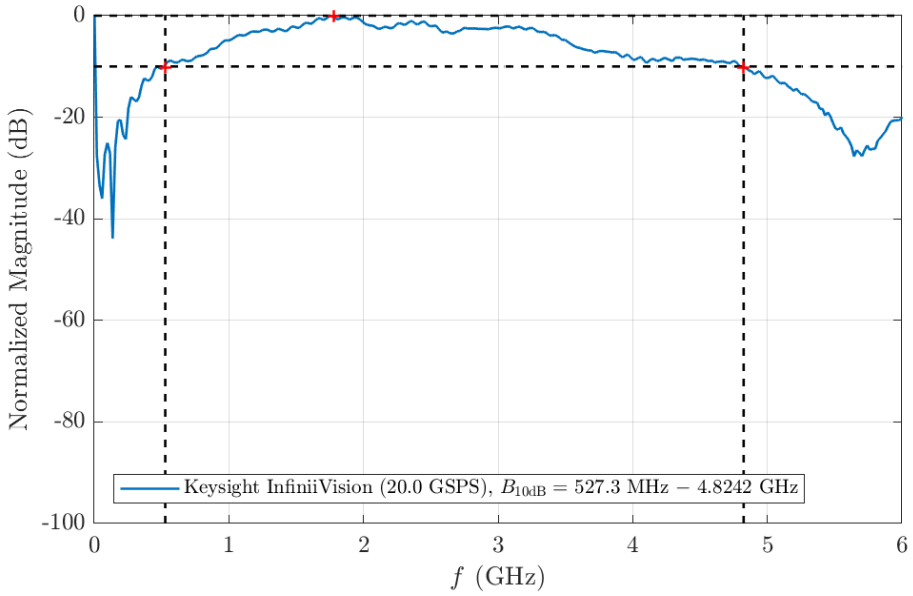


Figure 6.8: Only the UWB pulse waveform reconstructed using the Equivalent-Time Sampling Receiver at an equivalent sampling rate of: i) 10 GSPS (blue), and ii) 20 GSPS (orange).

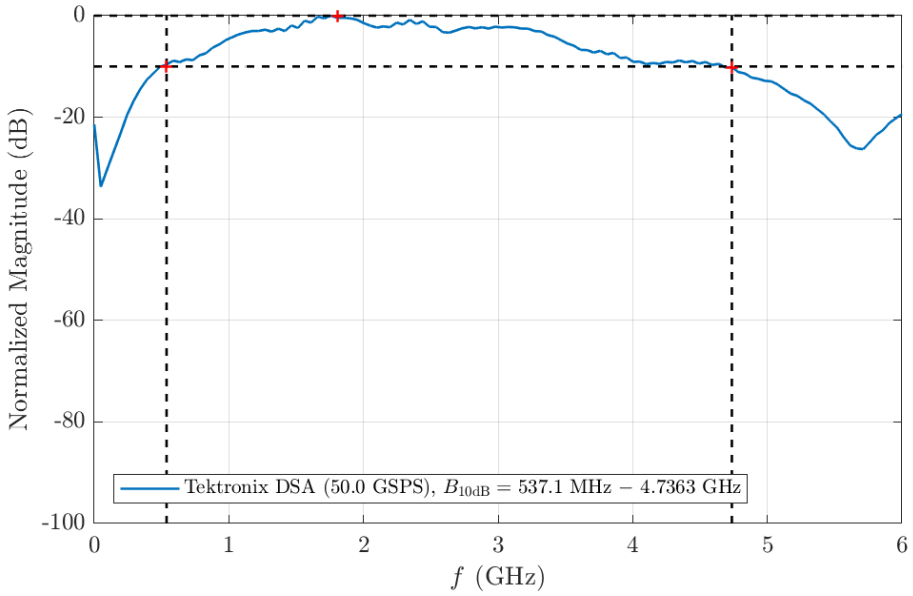
receiver (providing the differential signal) has an insertion loss of approximately 2 dB at 5 GHz [33], ii) the transfer function of the track and hold (T & H) amplifier at 5 GHz has approximately 3 dB loss [34], and iii) the temperature dependence of the PDC impacts the actual delay applied to the ADC clock [28]. Future work should investigate the characterization of these losses and the development of calibration techniques to remove the effects.

6.6 Conclusions

The software running the UWB pulsed radars, specifically the Equivalent-Time Sampling Receiver, is developed. The choice of the FPGA used for the design is justified. The SoC provided in the Zedboard meets the specification for the design and provides the capabilities to allow the PL section to manage the real-time aspect of the

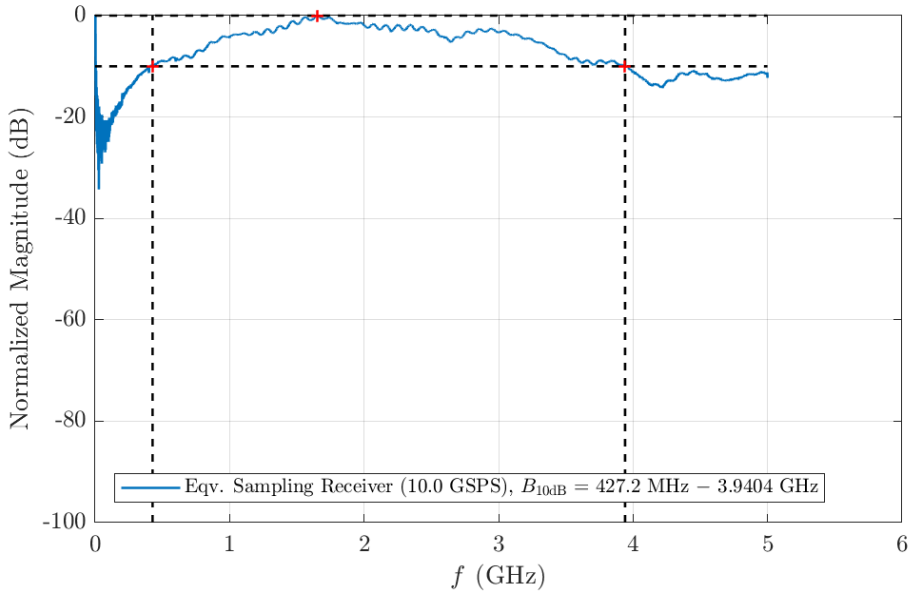


(a)

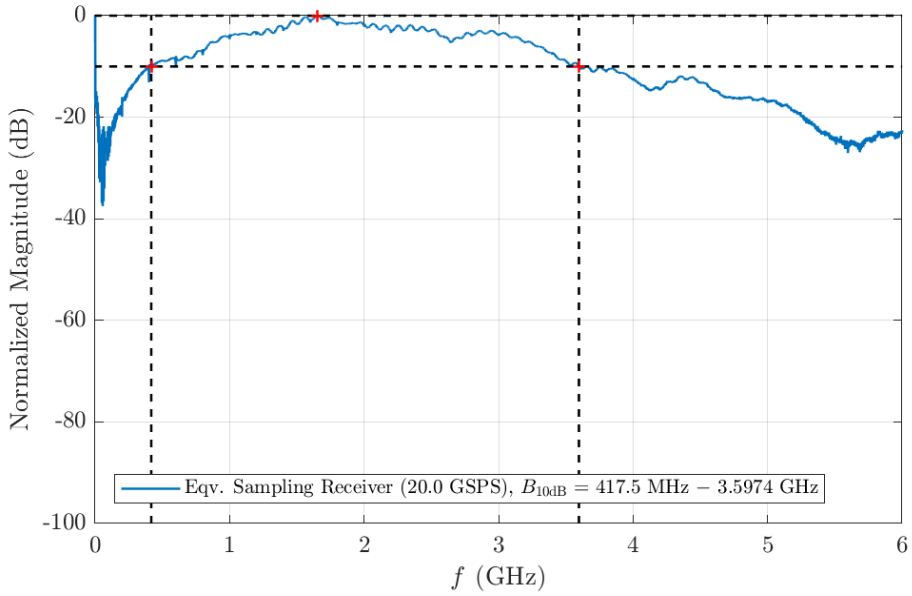


(b)

Figure 6.9: Spectral domain results with their −10 dB bandwidths: (a) the Keysight InfiniiVision Oscilloscope, and (b) the Tektronix Digital Signal Analyzer (DSA).



(a)



(b)

Figure 6.10: Spectral domain results with their −10 dB bandwidths: (a) the Equivalent-Time Sampling Receiver set at an equivalent sampling rate of 10 GSPS, and (b) the Equivalent-Time Sampling Receiver set at an equivalent sampling rate of 20 GSPS.

data collection. At the same time, the PS section handles the communication and data management with the host personal computer. The SoC also opens future capabilities not yet explored or even considered here. Outlined is the HDL design within the PL fabric of the FPGA, along with a discussion behind the ADC data processing. Presented is a high-level view of the software implemented on the PS core of the SoC, along with the findings of the first equivalently sampled pulse. The comparison results of the equivalently sampled pulse to two bench-top laboratory-grade oscilloscopes are promising. Future work should aim at the calibration of known losses in the Equivalent-Time Sampling Receiver input and improving the signal reconstruction time (i.e. running at 250 MHz instead of 200 MHz). The result of this effort is that a prototype of a UWB radar system is fully operational.

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Chapter 7

Conclusions and Future Work

7.1 Conclusions

In this work, a compact low-cost ultra-wideband (UWB) pulsed-radar system is developed. It combines the state-of-the-art in field-programmable gate array (FPGA) technologies and UWB radio frequency (RF) architectures to develop a novel analog version of a software defined radar (SDR) with 1:10 bandwidth capabilities. The design targets the emerging short-range UWB applications in concealed weapon detection (CWD) surveillance along with ground penetrating radar (GPR), non-destructive testing (NDT), through-the-wall imaging, and medical diagnostic imaging. Here, the desired bandwidth of the dual-channel system is from 500 MHz to 5 GHz. Presented is the novel system at the system level with further discussion on the individual modules which make up the system integration. The design requirements are based on the intended application in CWD; however, simple modifications (noted throughout the thesis) to select modules, chips and FPGA programming can broaden the system capabilities.

The system modules described here are: i) the transmitter module (a UWB pulse

generator), ii) the receiver module (the Equivalent-Time Sampling Receiver), and iii) the FPGA module with its hardware descriptive language (HDL) design and software implementation. The UWB pulse generator has been presented to show a promising bandwidth from approximately 450 MHz to 3.6 GHz at a pulse repetition frequency (PRF) of 1 MHz. Measurements of the generators jitter stability and voltage noise are comparable to that of a bench-top laboratory-grade arbitrary waveform generator (AWG). Presented as a daughter development board for FPGAs is the hardware development of the Equivalent-Time Sampling Receiver. The key component choices for the analog-to-digital converter (ADC), track and hold (T & H) amplifier and programmable delay chip (PDC) are discussed. Here, the emphasis is on the component layout, the sample clocking network and the ADC data bus clock. The first FPGA HDL and software control of the UWB pulsed-radar system are presented. The main challenge addressed in the FPGA development is working across multiple clock domains for the synchronization of the transmitter and the receiver modules. Reconstruction of the desired bandwidth is not possible without the work on the equivalent-time sampling process presented in this work. Finally, the first results of a UWB pulse signal reconstruction using the designed system are shown to be comparable to those of bench-top laboratory-grade oscilloscopes.

The full cost of the system is under $5,000 Canadian dollars. This includes two UWB pulse generators (approximately $300 per boxed-up board), one Equivalent-Time Sampling Receiver (approximately $3,000 per board, including the box), and one FPGA (approximately $800 per Zedboard). The result is a fully functional prototype that costs a fraction of traditional bench-top solutions. The solution comes in a much smaller form factor when compared to the sizes of the bench-top instruments. The final system design is sophisticated but modular to allow for customization in performance to meet the needs of any short-range UWB radar applications.

7.2 Future Work

The main purpose in this development of a compact low-cost system is for its use in a surveillance system detecting concealed or contraband items [1]. Throughout this work, many suggestions for future work have been provided. All of these can improve the radar performance. For instance, finding an alternative to the PDC group delay instability is discussed in Chapter 6. Methods for increasing the peak-to-peak voltage and the bandwidth of the UWB pulse generator are discussed in Chapter 4.

Those working in the hardware development of similar radar systems should remain aware of advancements in RF system on a chip (SoC) technologies (sometimes referred to as FPGAs with RF sockets), much like the Xilinx UltraScale+ RFSoC [2]. These RF SoCs marry the latest state-of-the-art RF and FPGA technologies into one integrated circuit (IC). This emerging technology is very promising; however, they are currently at a primitive state and do not meet the current needs of the proposed system. As these technologies advance, their costs will decrease making them affordable and their sampling rates will increase to meet the needs of the design shown here.

In addition to improving the hardware, the following steps are necessary for this line of work.

1. **Performance evaluation of the radar modules.** This evaluation includes returning to the jitter and noise measurements discussed in Chapter 4 to define a rigorous measurement methodology for the characterization of the UWB pulse jitter. Shown in this work is only a preliminary evaluation of the Equivalent-Time Sampling Receiver performance. A detailed evaluation of the RF front-end noise figure, signal-to-noise ratio (SNR), noise floor and suppression of wireless interference must be completed along with jitter and noise performance of the

receiver.

2. **Integrating the transmitter module, receiver module, and FPGA on a common printed circuit board (PCB)** reducing the RF interconnect complexity, power consumption and the radar form factor. This work can also include an investigation into applying an RF front-end gain stage and filtering to the Equivalent-Time Sampling Receiver. The goal leads to the pursuit of a portable and easily deployable UWB radar system.

3. **Improving the data offload rate and reducing the dropped data packet occurrences.** The current data offload is insufficient for obtaining all received signals from the FPGA and as a result data is lost. Further investigation is required to overcome this design challenge and possible avenues include:

   (a) Finding alternative physical communication strategies and solutions for data offloading that can obtain higher data rates such as 10 Gigabit Ethernet, universal serial bus (USB) 3.0 or USB 3.1.

   (b) Performing additional digital signal processing (DSP) on the data within the programmable logic (PL) and processing system (PS) sections of the FPGA.

   (c) Ensuring data transmission and reception is optimized and tuned on both the FPGA and signal processing module (SPM) module. This would include optimizing the management of tasks running within the FPGA in order to handle the events of lost data, as well as, the capability of the SPM module of receiving and detecting lost information.

4. **Implementation of on-chip FPGA signal averaging.** Begin the implementation of an average and a rolling average for an X number of signals within

the PL of the FPGA.

5. **Expand the Ethernet capabilities in order to remotely control the radar system via an Ethernet connection.** Thereby removing and replacing the universal asynchronous receiver/transmitter (UART) control and enable the opportunities for a network of radar systems to work in unison.

6. **Implementation of a real-time and/or a general-purpose operating systems on the dual central processing unit (CPU) FPGA PS.** Investigate whether or not the proposed ideal software stack-up for a dual operating system would improve the management of task the FPGA performs. This will also enable the possibility of implementing the pre-processing and DSP for target detection and classification within the FPGA (PL and PS sections).

7. Finally, **testing the UWB radar system performance in a deployment scenario.** Calibration techniques must be developed for de-embedding the target signatures from the radar systems transfer function. In other words, building target signatures which are independent of the antenna and radar system so that the same signatures can train different systems.

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Appendix A

Equivalent-Time Sampling Receiver FMC Pinout

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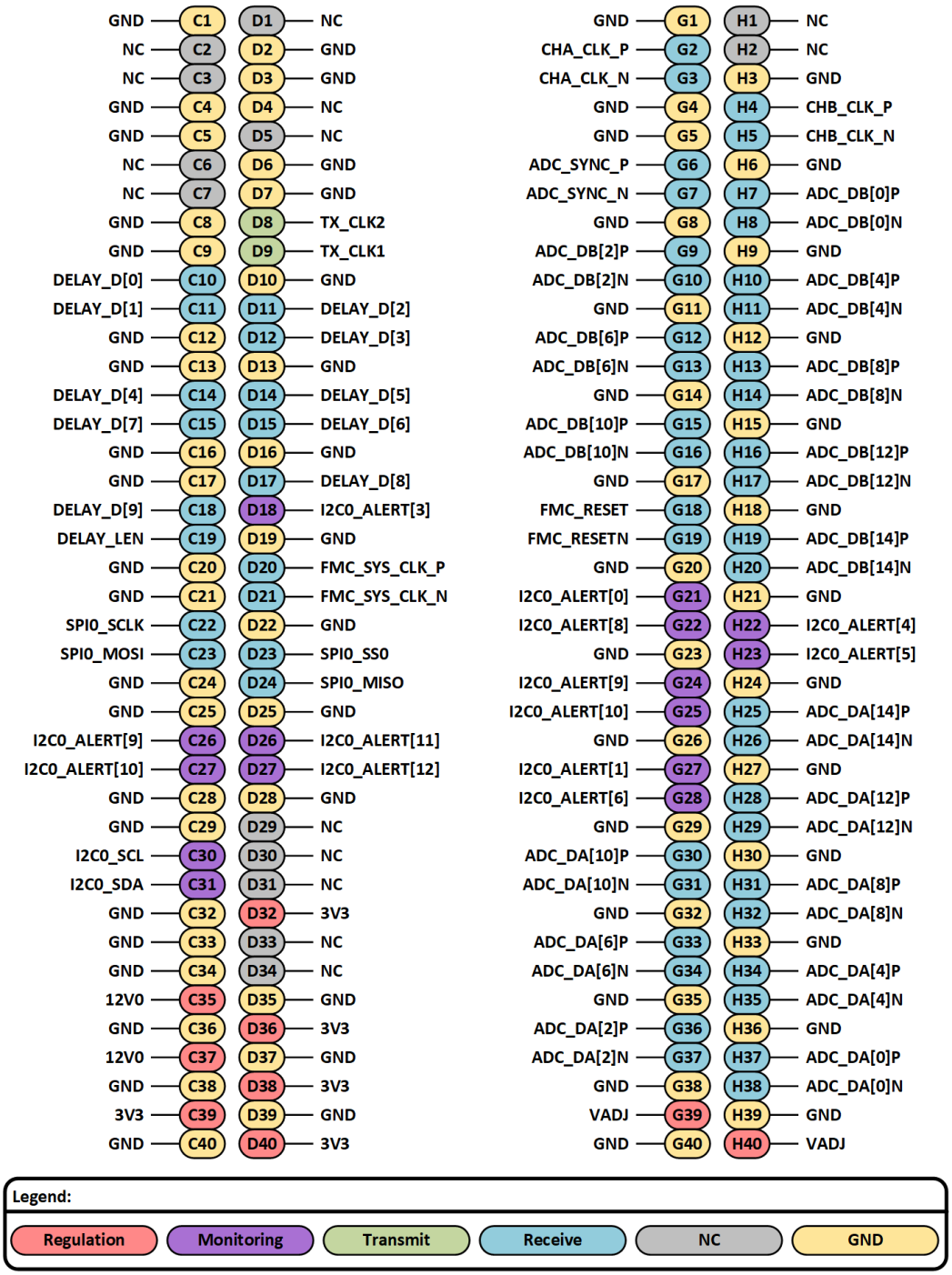

Figure A.1: Equivalent-Time Sampling Receiver FMC connector pinout.

Appendix B

Zedboard FMC Pinout

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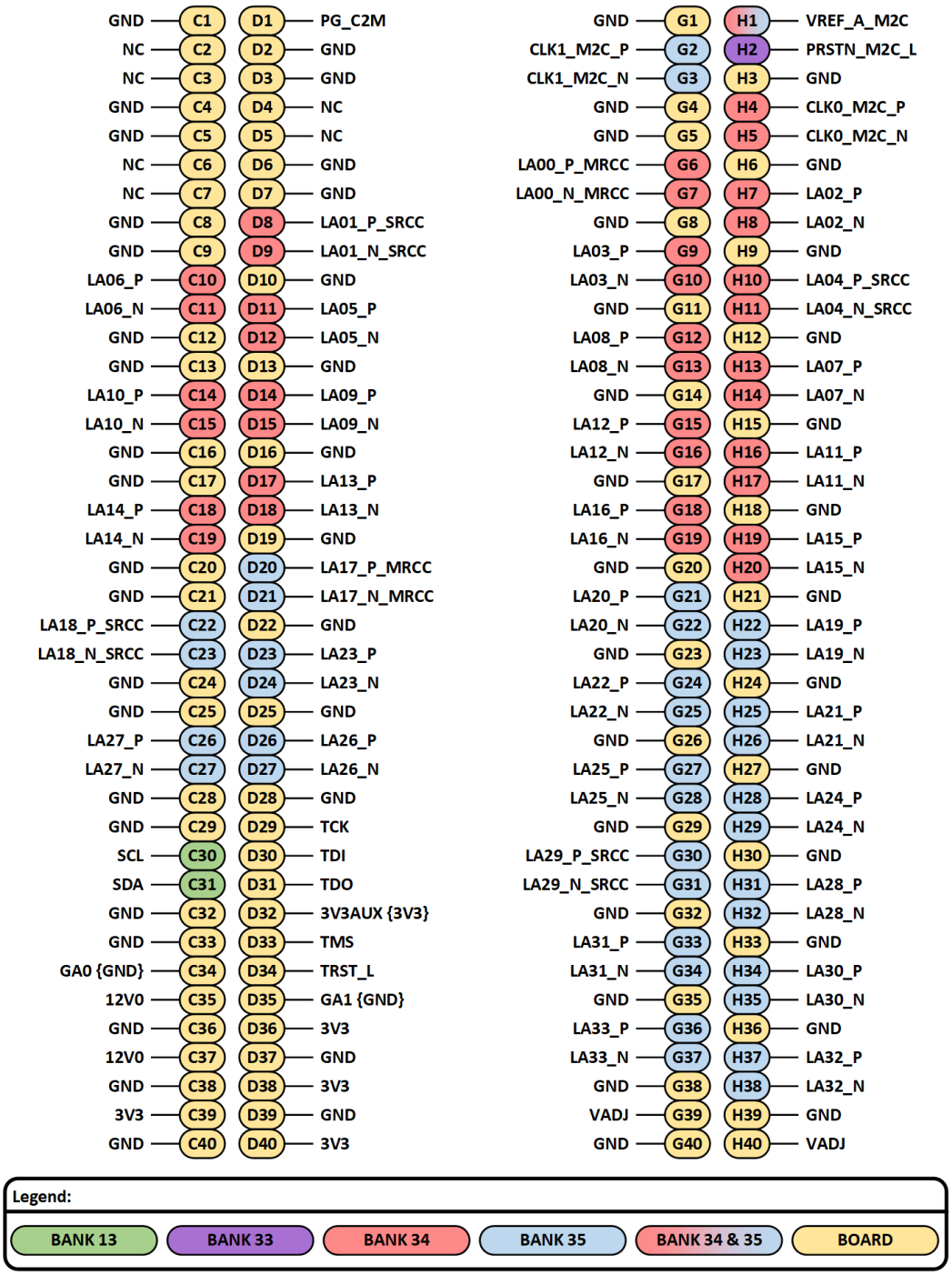

Figure B.1: Digilent Zedboard FMC connector pinout [1].

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Appendix C

Equivalent-Time Sampling Receiver PCB Layout

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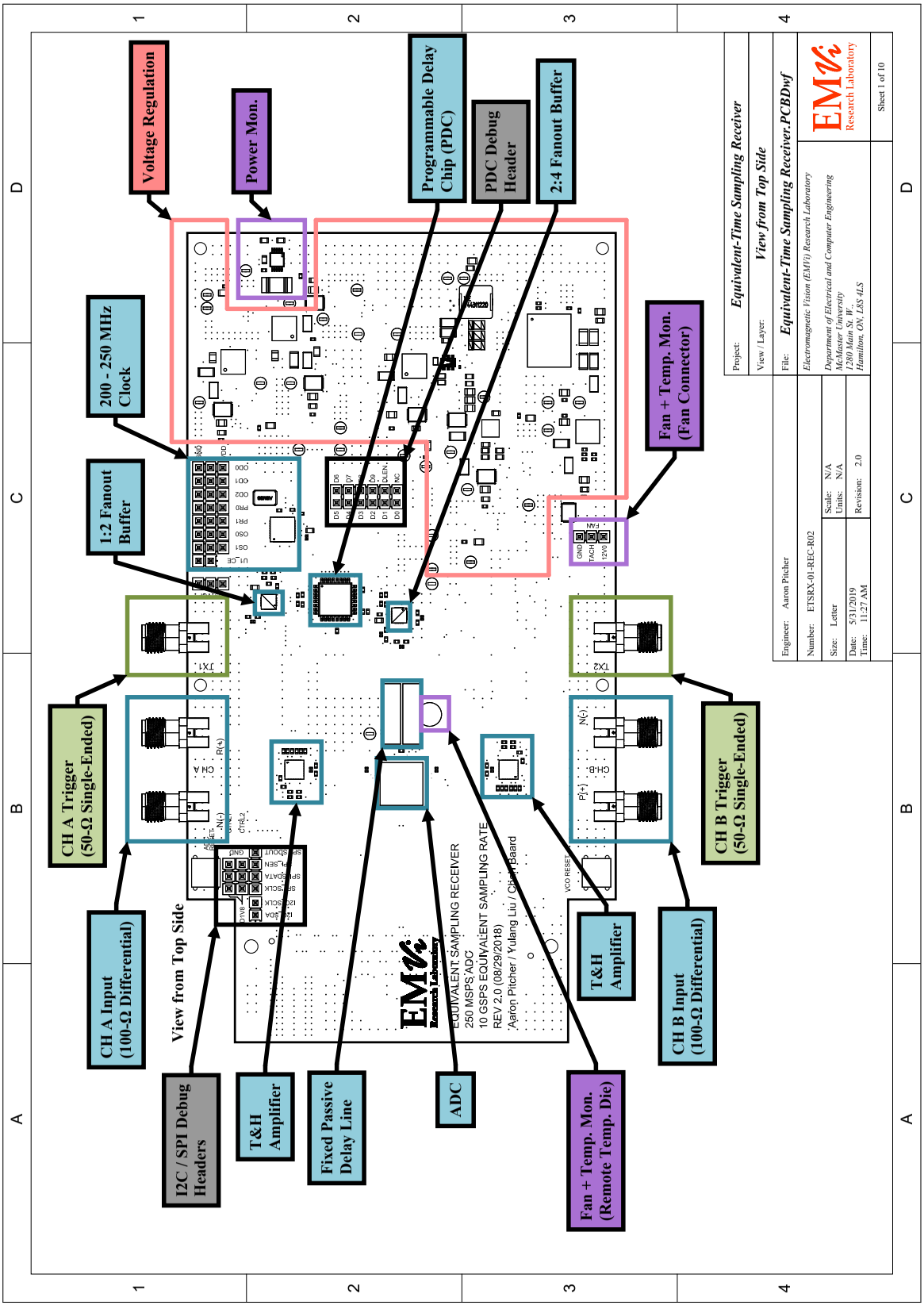
Voltage Regulation
Power Mon.
Programmable Delay Chip (PDC)
PDC Debug Header
2:4 Fanout Buffer
200 - 250 MHz Clock
1:2 Fanout Buffer
Fan + Temp. Mon. (Fan Connector)
CH A Trigger (50-Ω Single-Ended)
CH B Trigger (50-Ω Single-Ended)
CH A Input (100-Ω Differential)
CH B Input (100-Ω Differential)
T&H Amplifier
T&H Amplifier
I2C / SPI Debug Headers
Fixed Passive Delay Line
ADC
Fan + Temp. Mon. (Remote Temp. Die)
View from Top Side
EQUIVALENT SAMPLING RECEIVER
250 MSPS ADC
10 GSPS EQUIVALENT SAMPLING RATE
REV 2.0 (08/29/2018)
Aaron Pitcher / Yulang Liu / Chuan Baard
Project: Equivalent-Time Sampling Receiver
View / Layer: View from Top Side
File: Equivalent-Time Sampling Receiver.PCBDwf
Engineer: Aaron Pitcher
Number: ETSRX-01-REC-R02
Size: Letter
Date: 5/31/2019
Time: 11:27 AM
Scale: N/A
Units: N/A
Revision: 2.0
Electromagnetic Vision (EMVi) Research Laboratory
Department of Electrical and Computer Engineering
McMaster University
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Hamilton, ON, L8S 4L8
Research Laboratory
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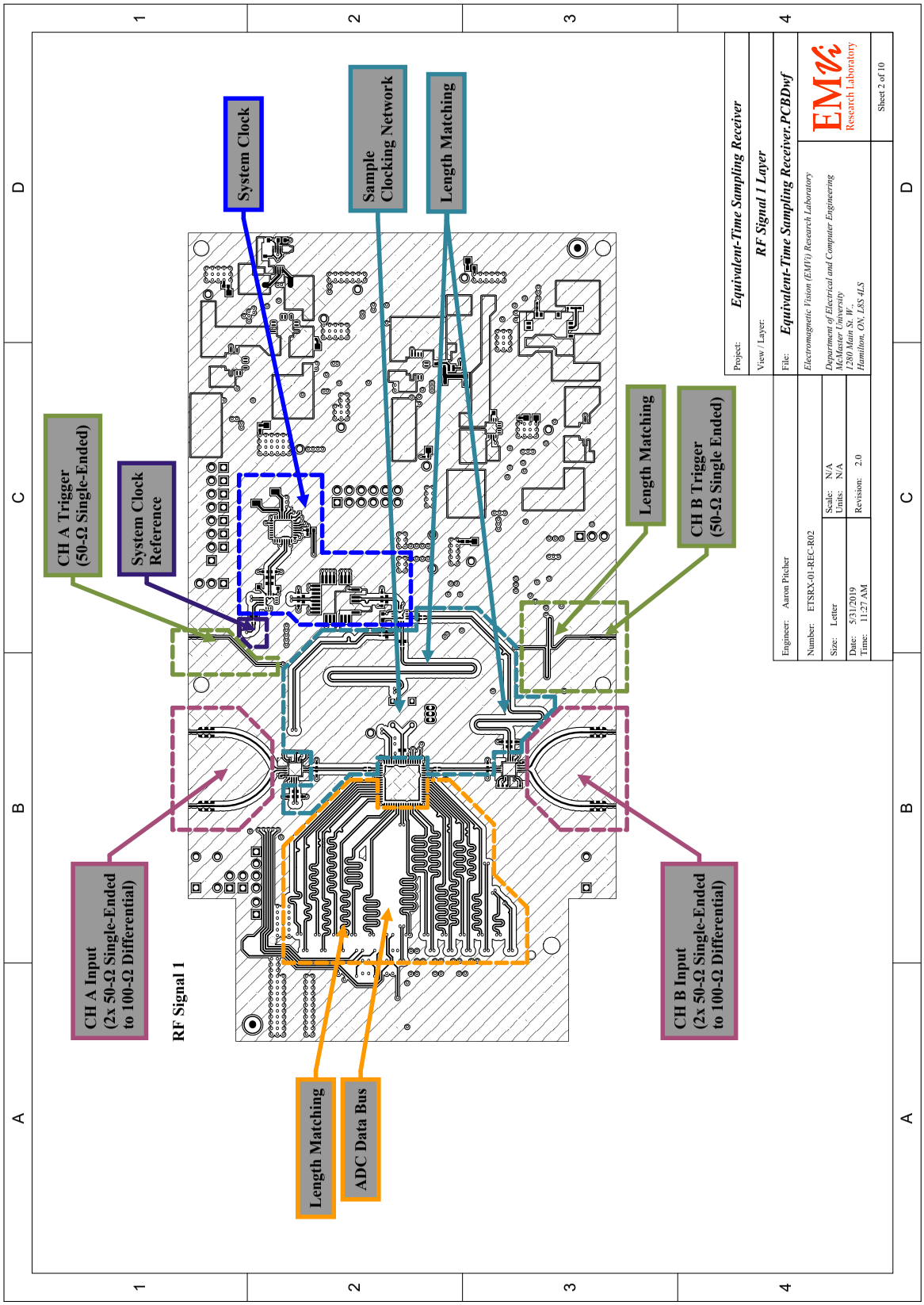
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Sample Clocking Network
Length Matching
CH A Trigger (50-Ω Single-Ended)
System Clock Reference
Length Matching
CH B Trigger (50-Ω Single Ended)
CH A Input (2x 50-Ω Single-Ended to 100-Ω Differential)
RF Signal 1
CH B Input (2x 50-Ω Single-Ended to 100-Ω Differential)
Length Matching
ADC Data Bus
Project: Equivalent-Time Sampling Receiver
View / Layer: RF Signal 1 Layer
File: Equivalent-Time Sampling Receiver.PCBDwf
Electromagnetic Vision (EMVi) Research Laboratory
Department of Electrical and Computer Engineering
McMaster University
280 Main St. W.
Hamilton, ON, L8S 4L8
EMVi
Research Laboratory
Engineer: Aaron Pitcher
Number: ETSRX-01-REC-R02
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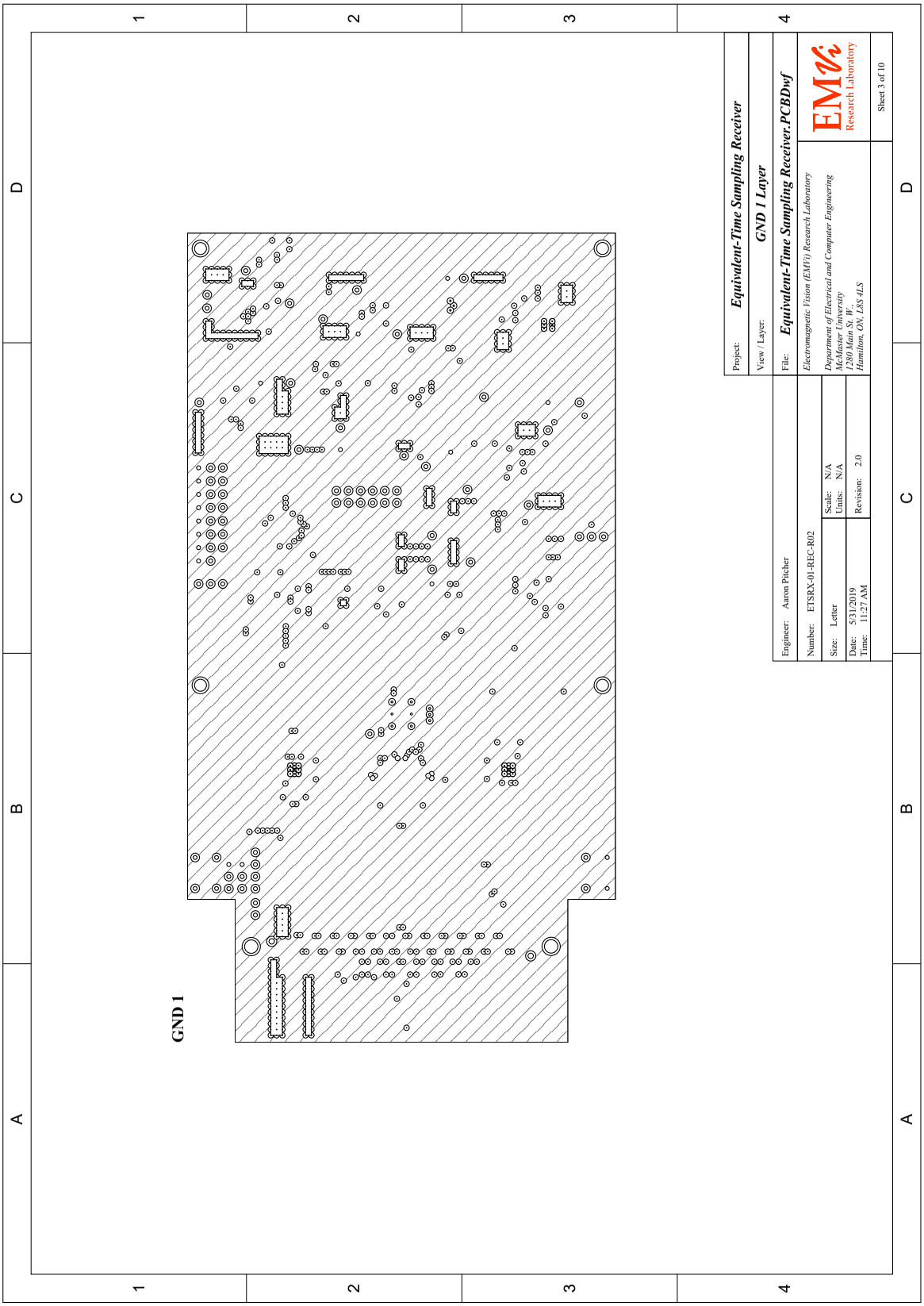
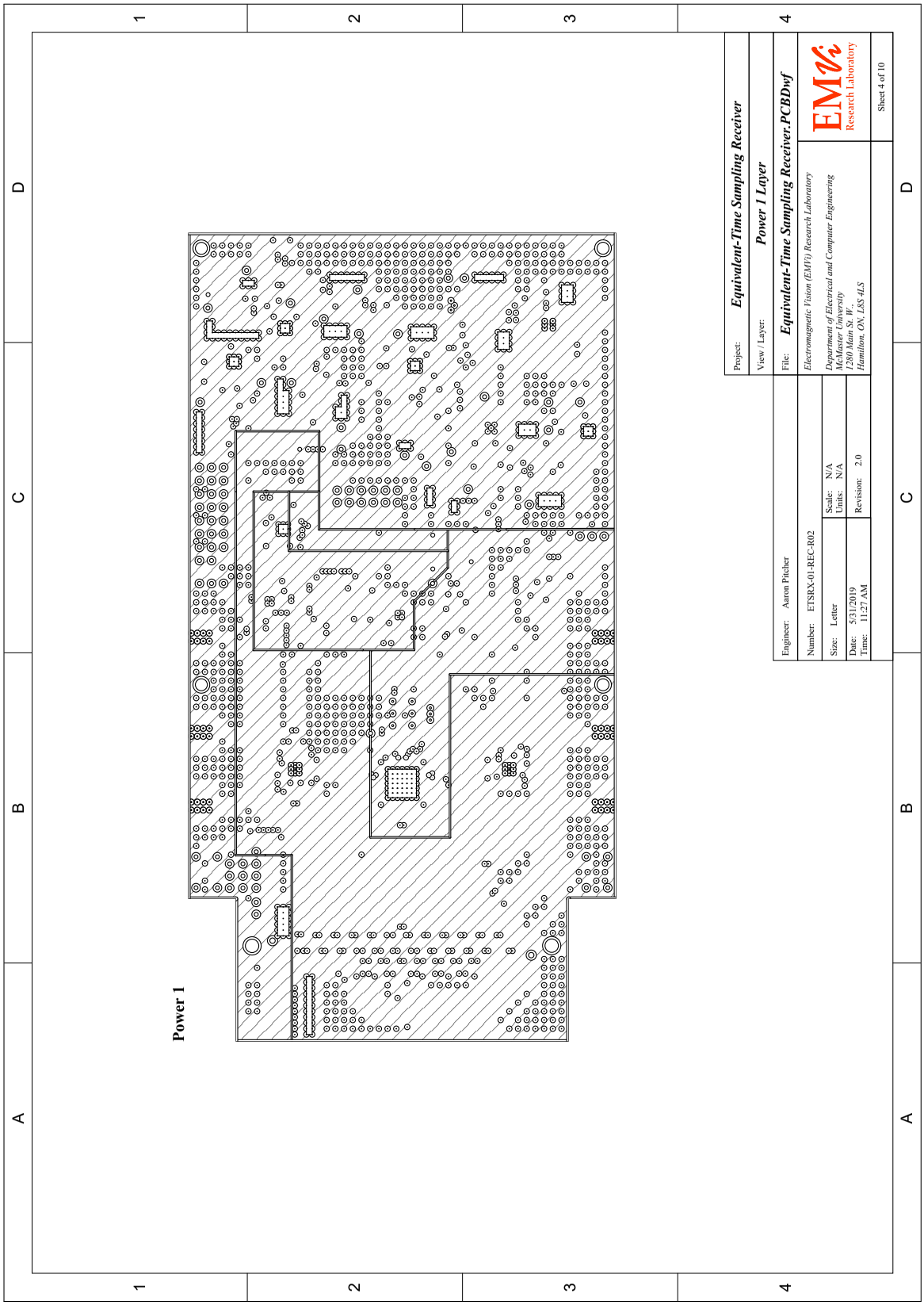
Time: 11:27 AM
Revision: 2.0
Sheet 2 of 10


GND 1
Project: Equivalent-Time Sampling Receiver
View / Layer: GND 1 Layer
File: Equivalent-Time Sampling Receiver.PCBDwf
Engineer: Aaron Pitcher
Number: ETSRX-01-REC-R02
Size: Letter
Date: 5/31/2019
Time: 11:27 AM
Scale: N/A
Units: N/A
Revision: 2.0
Electromagnetic Vision (EMVi) Research Laboratory
Department of Electrical and Computer Engineering
McMaster University
1280 Main St. W.,
Hamilton, ON, L8S 4L8
EMVi
Research Laboratory
Sheet 3 of 10


Power 1
Project: Equivalent-Time Sampling Receiver
View / Layer: Power 1 Layer
File: Equivalent-Time Sampling Receiver.PCBDwf
Engineer: Aaron Pitcher
Number: ETSRX-01-REC-R02
Size: Letter
Date: 5/31/2019
Time: 11:27 AM
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Units: N/A
Revision: 2.0
Electromagnetic Vision (EMVi) Research Laboratory
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Hamilton, ON, L8S 4L8
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Research Laboratory
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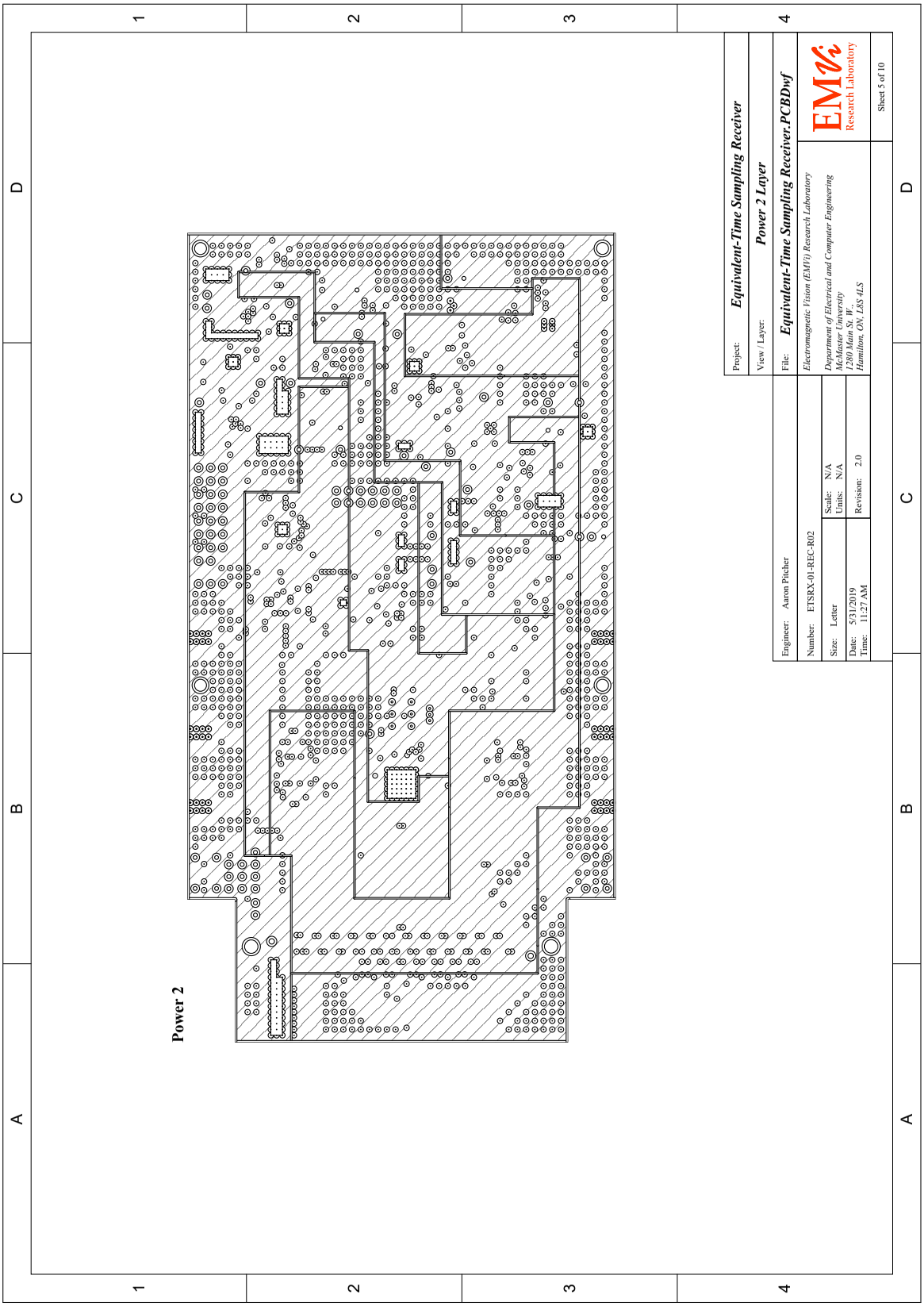
Power 2
Project: Equivalent-Time Sampling Receiver
View / Layer: Power 2 Layer
File: Equivalent-Time Sampling Receiver.PCBDwf
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Department of Electrical and Computer Engineering
McMaster University
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Hamilton, ON, L8S 4L8
EMVi
Research Laboratory
Engineer: Aaron Pitcher
Number: ETSRX-01-REC-R02
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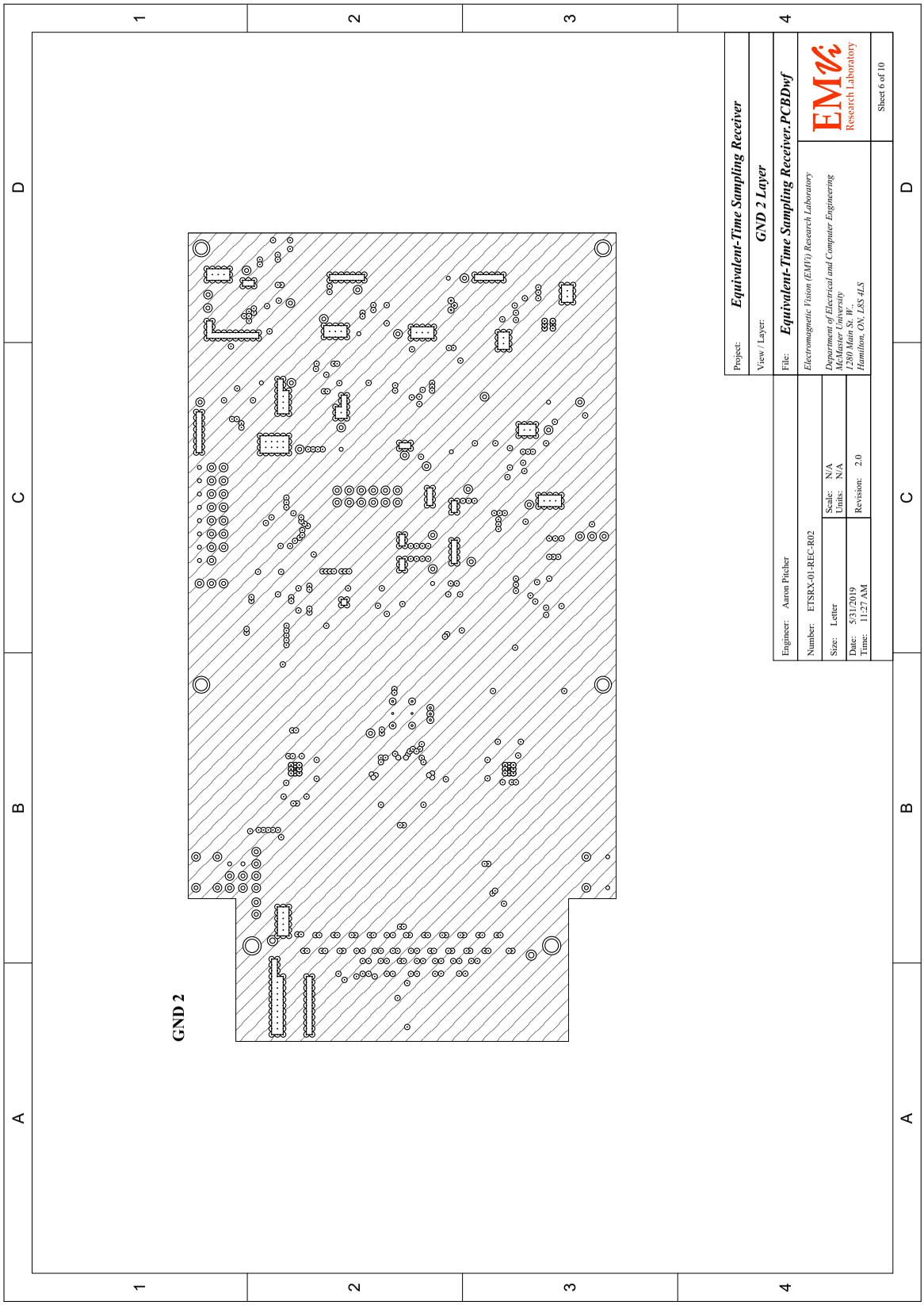
Revision: 2.0
Sheet 5 of 10


GND 2
Project: Equivalent-Time Sampling Receiver
View / Layer: GND 2 Layer
File: Equivalent-Time Sampling Receiver.PCBDwf
Engineer: Aaron Pitcher
Number: ETSRX-01-REC-R02
Size: Letter
Date: 5/31/2019
Time: 11:27 AM
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Units: N/A
Revision: 2.0
Electromagnetic Vision (EMVi) Research Laboratory
Department of Electrical and Computer Engineering
McMaster University
280 Main St. W.
Hamilton, ON, L8S 4L8
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Research Laboratory
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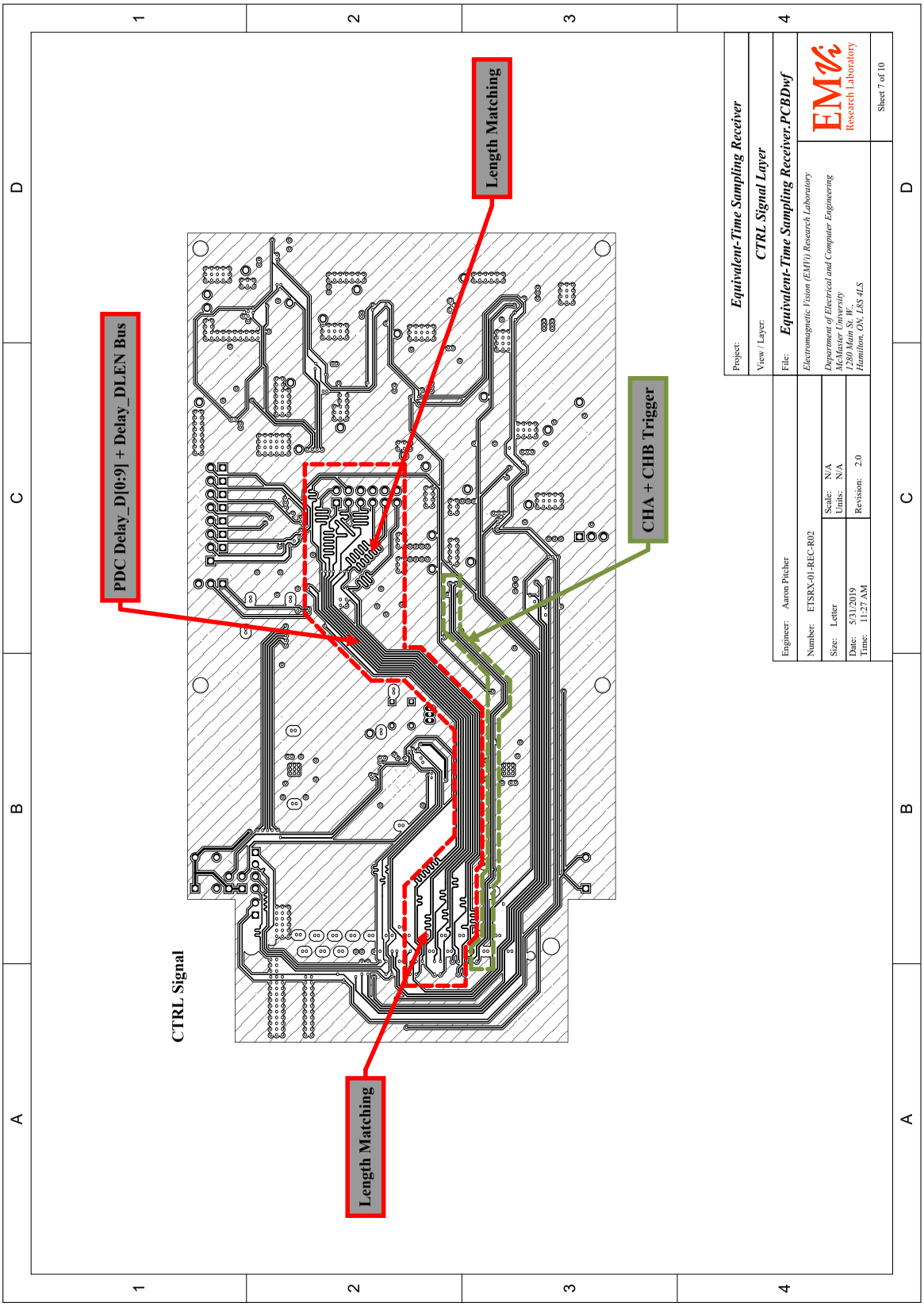
Length Matching
PDC Delay_D[0:9] + Delay_DLEN Bus
CHA + CHB Trigger
CTRL Signal
Length Matching
Project: Equivalent-Time Sampling Receiver
View / Layer: CTRL Signal Layer
File: Equivalent-Time Sampling Receiver.PCBDwf
Electromagnetic Vision (EMVi) Research Laboratory
Department of Electrical and Computer Engineering
McMaster University
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Hamilton, ON, L8S 4L8
EMVi
Research Laboratory
Engineer: Aaron Pitcher
Number: ETSRX-01-REC-R02
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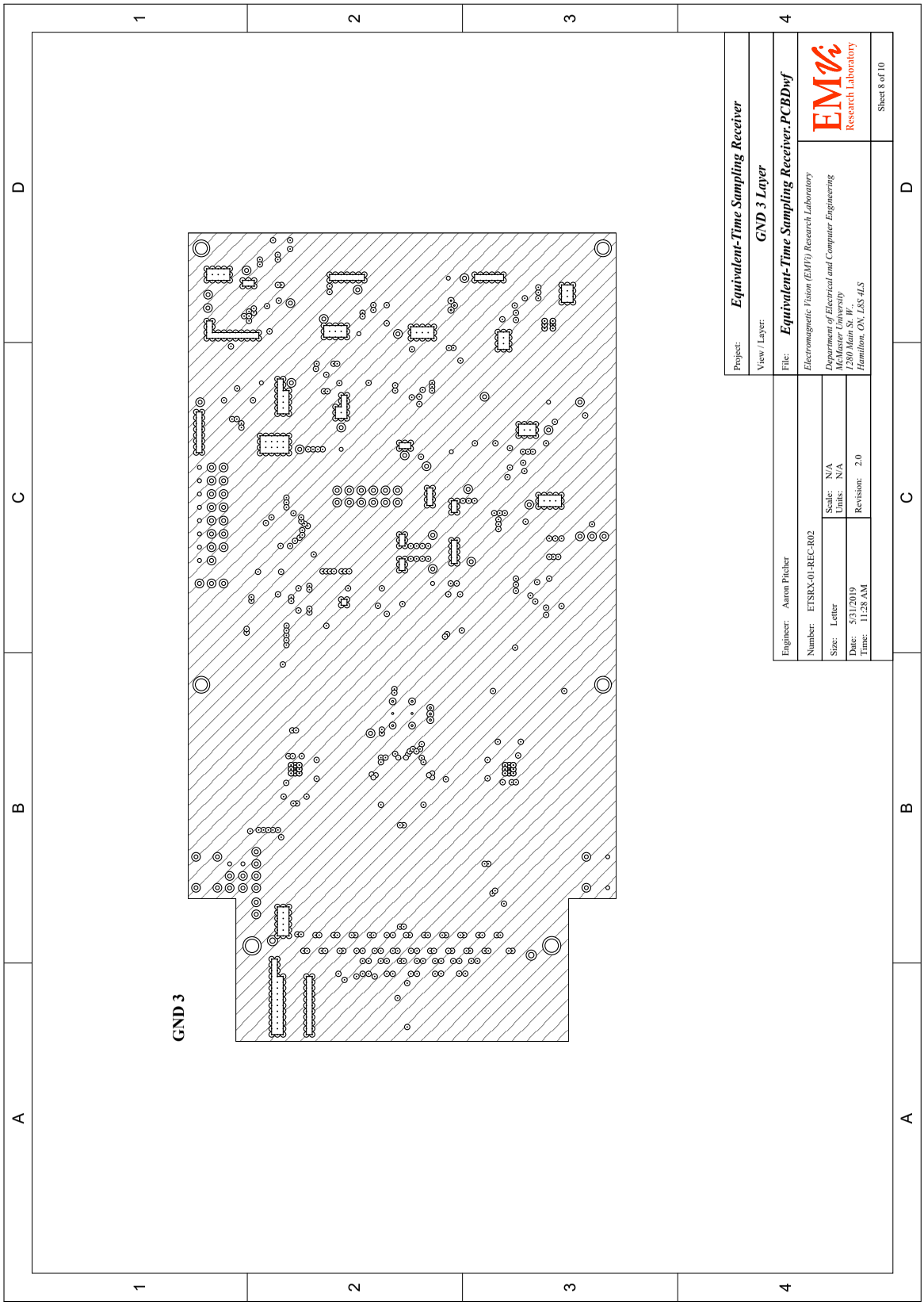
Revision: 2.0
Sheet 7 of 10


GND 3
Project: Equivalent-Time Sampling Receiver
View / Layer: GND 3 Layer
File: Equivalent-Time Sampling Receiver.PCBDwf
Engineer: Aaron Pitcher
Number: ETSRX-01-REC-R02
Size: Letter
Date: 5/31/2019
Time: 11:28 AM
Scale: N/A
Units: N/A
Revision: 2.0
Electromagnetic Vision (EMVi) Research Laboratory
Department of Electrical and Computer Engineering
McMaster University
280 Main St. W.
Hamilton, ON, L8S 4L8
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Research Laboratory
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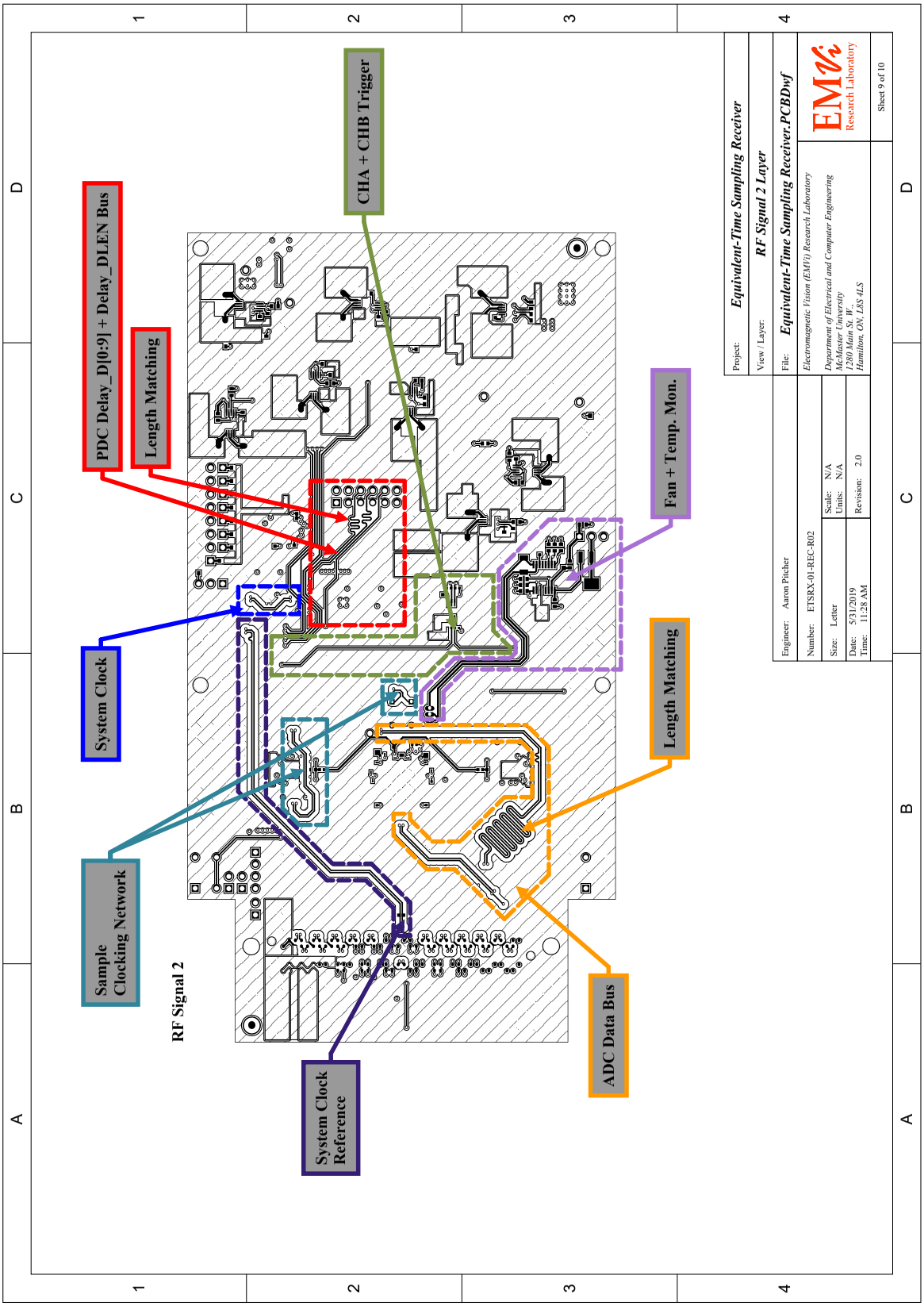
CHA + CHB Trigger
PDC Delay_D[0:9] + Delay_DLEN Bus
Length Matching
System Clock
Sample Clocking Network
RF Signal 2
System Clock Reference
Fan + Temp. Mon.
Length Matching
ADC Data Bus
Project: Equivalent-Time Sampling Receiver
View / Layer: RF Signal 2 Layer
File: Equivalent-Time Sampling Receiver.PCBDwf
Electromagnetic Vision (EMVi) Research Laboratory
Department of Electrical and Computer Engineering
McMaster University
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Hamilton, ON, L8S 4L8
EMVi Research Laboratory
Engineer: Aaron Pitcher
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Scale: N/A
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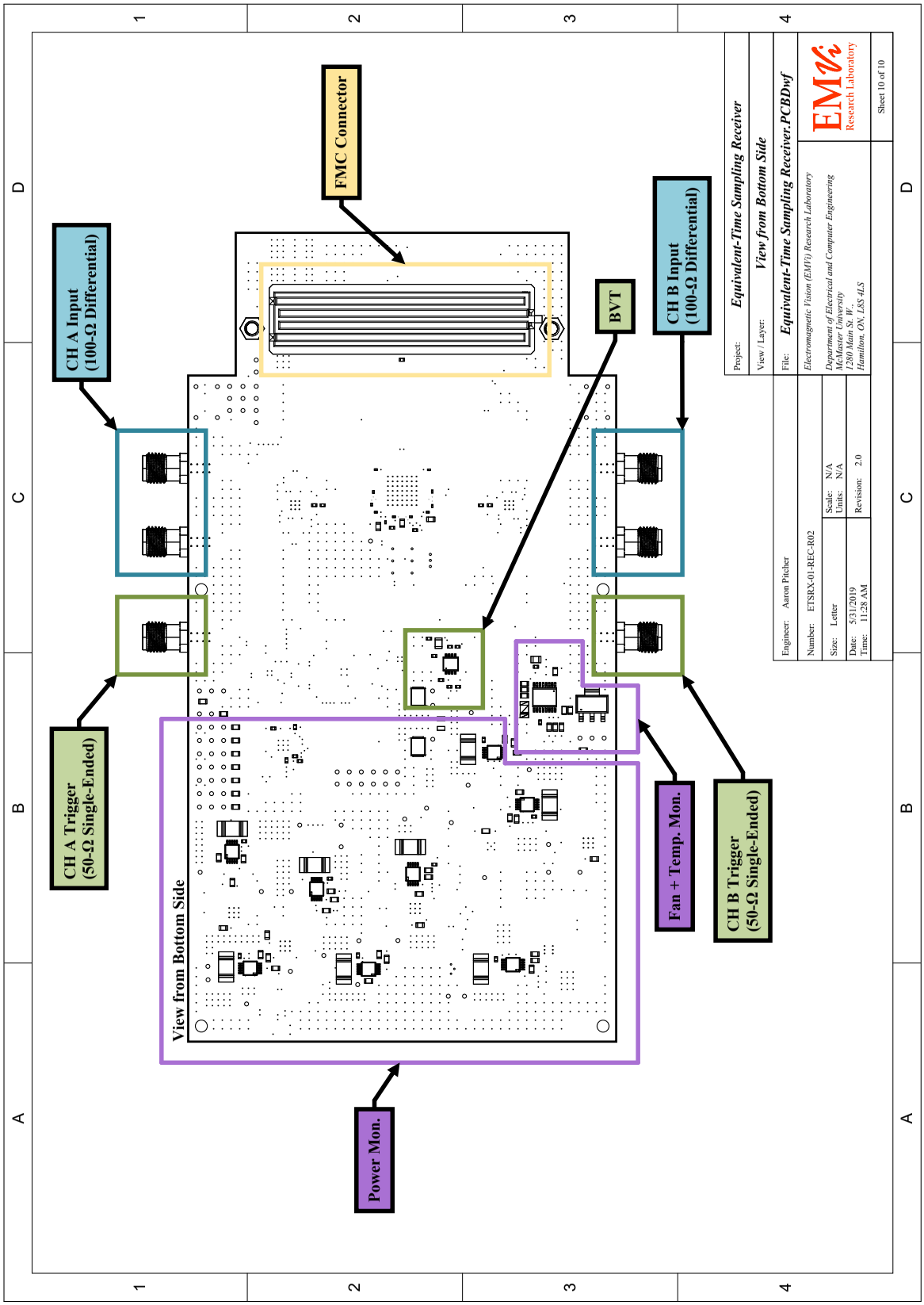
Time: 11:28 AM
Revision: 2.0
Sheet 9 of 10


FMC Connector
CH A Input (100-Ω Differential)
CH B Input (100-Ω Differential)
BVT
CH A Trigger (50-Ω Single-Ended)
CH B Trigger (50-Ω Single-Ended)
Fan + Temp. Mon.
Power Mon.
View from Bottom Side
Project: Equivalent-Time Sampling Receiver
View / Layer: View from Bottom Side
File: Equivalent-Time Sampling Receiver.PCBDwf
Engineer: Aaron Pitcher
Number: ETSRX-01-REC-R02
Size: Letter
Scale: N/A
Units: N/A
Date: 5/31/2019
Time: 11:28 AM
Revision: 2.0
Sheet 10 of 10
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