On the Use of Light-Emitting Freewheeling/Blocking Diodes for Optical Wireless Communications

ON THE USE OF LIGHT-EMITTING FREEWHEELING/BLOCKING DIODES FOR OPTICAL WIRELESS COMMUNICATIONS

BY

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I would like to dedicate this thesis in memory of my Nonno who inspired my passion for electrical engineering, my mother for her unwavering support and strength, and both my father and brother for always believing in me.

Abstract

Although visible light communication(VLC) systems can provide high density links for use with IoT devices, an energy efficient, high rate method of designing a VLC transmitter is still unclear. Present designs for transmitters such as the bias-T, designs with switch manipulation, and interleaved converters are not commercially viable due to costly and complex designs that sacrifice energy efficiency for data rate. A design allowing for efficient, high rate communications, while maintaining a low cost would allow for widespread adoption of this technology.

In this thesis, a novel approach of integrating power converters and VLC systems is explored by replacing commutating diodes with LEDs. By leveraging switched-mode power supply(SMPS) structures, the power dissipated within the converter may be harnessed and used for communications. The result is a simple and energy efficient solution capable of high rate links.

Simulation and experimental results demonstrate buck and boost SMPS topologies that simultaneously increase energy efficiency and provide communications at SMPS switching rate without increasing component count.

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Without the help of my supervisors, Dr. Steve Hranilovic, and Dr. Mehdi Narimani, this work would not be possible. Their technical expertise and guidance through my academic career were invaluable. I feel privileged to have worked with both of you.

I would also like to acknowledge all of my friends and family that helped me through this incredible journey. Words cannot express how much I appreciate the support from each and every one of you!

Notation

D - Duty cycle (%)

V_s - Source Voltage (V)

V_o - Output Voltage (V)

I_s - Source Current (A)

I_o - Source Current (A)

I_L - Inductor Current (A)

I_D - Diode Current (A)

V_{bias} - Diode Bias Voltage (V)

V_+ - Voltage at diode anode (V)

V_- - Voltage at diode cathode (V)

V_f - Diode Forward Voltage (V)

V_f^{LEFD} - LEFD Forward Voltage (V)

V_f^{LEBD} - LEBD Forward Voltage (V)

f_{sw} - Switching Frequency (Hz)

$P_e(\lambda)$ - Spectral power distribution (W/nm) P_{error} - Probability of error

$P_D^c onduction$ - Diode conduction loss (W)

$P_{SW}^c onduction$ - Switch conduction loss (W)

P_{Dsw} - Diode switching loss (W)

P_{FETsw} - FET switching loss (W)

P_{IN} - Input electrical power (W)

P_{OUT} - Output electrical power (W)

P_{cond} - Conduction power loss (W)

P_{switch} - Switching power loss (W)

R_{Deq} - Equivalent diode resistance (Ω)

t_{ON} - Control switch conducting time (s)

t_{OFF} - Control switch non-conducting time (s)

T - Period (s)

η_E - Electrical Efficiency $(\%)$

η_O - Efficacy (lm/W)

η_O^{SMPS} - Efficacy of switched-mode power supply (lm/W)

$\eta_O^L ED$ - Efficacy of light-emitting diode (lm/W)

η'_O - Normalized Optical Efficiency $(\%)$

Φ_E - Radiant Flux (W)

Φ_V - Luminous Flux (lm)

d_{min} - Minimum Euclidian distance

$\bar{d}_{min}$ - Normalized minimum Euclidian distance

Abbreviations

AC - Alternating Current

BER - Bit Error Rate

CCM - Continuous Conduction Mode

CCT - Correlated Colour Temperature

CIE - International Commission on Illumination

CRI - Colour Rendering Index

CSK - Color-Shift Keying

D - Duty Cycle of Main Control Switch

DC - Direct Current

DCM - Discontinuous Conduction Mode

EMI - Electromagnetic Interference

EN - European Standards

FET - Field-Effect Transistor

IEC - International Electrotechnical Commission

IEEE - Institute of Electrical and Electronics Engineers

IoT - Internet of Things

LEBD - Light-Emitting Blocking Diode

LED - Light-Emitting Diode

LEFD - Light-Emitting Freewheeling Diode

MAC - Media Access Control Layer

MRI - Magnetic Resonance Imaging

OCC - Optical Camera Communications

OPPM - Overlapping Pulse Position Modulation

OWC - Optical Wireless Communications

PCB - Printed Circuit Board

PHYS - Physical Layer

PoE - Power Over Ethernet

PPM - Pulse-Position Modulation

PWL - LTspice Piecewise Linear File

PWM - Pulse Width Modulation

RF - Radio Frequency

SWMPS - Switching Mode Power Supply

VLC - Visible Light Communications

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Chapter 1

Introduction

Wireless communications has seen a tremendous amount of innovation in recent decades, connecting an increasing number of devices. According to studies of mobile data traffic growth completed by Cisco Systems and Ericsson, the number of Short-range Internet-of-Things (IoT) connected devices was in the range of 6.1 to 6.2 billion devices in 2017. Both companies forecast the increasing demand for these devices to reach 14.6 billion in 2022 [1] and 15.7 billion in 2023 [2]. IoT devices use a wide variety of bands within the electromagnetic spectrum to facilitate communication links. As new technologies are released, an already congested spectrum is becoming increasingly cluttered. Much of this spectrum is licensed and heavily regulated as outlined by the *Canadian Table of Frequency Allocations* [3] and depicted by the related visual representation in [4]. Ranges of radio frequencies (RF) are being re-allocated in order to shift the types of devices using those bands. In Europe, it has been proposed to exclude TV broadcasting from the 700MHz band (694-790MHz) band and re-purpose it to support widespread, high speed Internet communications [5]. This would force broadcasters to focus on adopting new technologies to use spectrum-efficient methods

of transmission [6]. A number of different methods are being proposed to solve the issue of the cluttered RF spectrum [7].

- Re-allocation of existing bands by international bodies [5] [6].
- Adopting spectrum-efficient technologies (e.g. new methods of compression & transmission)
- Avoiding interference (e.g. Smart-Cells & Smart-Antennas) [7]
- Using under-utilized & unlicensed spectrum (millimeter-wave RF band(27-300GHz) & optical band)

In addition to issues of overcrowded spectrum, privacy and security are important issues when discussing IoT devices. There is enormous monetary value in data and companies are trusted to maintain strict security. As the number of connected devices increases, so does the amount of threat vectors. This is of growing concern evidenced by the 864 breaches that released 34.2 million records in September 2018 [1].

Throughout daily life, the use of luminaires are generally overlooked. Efficient lighting technologies have become necessity and are present virtually everywhere. It is estimated that approximately 20% of energy generated worldwide is for illumination. [8] [9] Modern lighting is dominated by light-emitting diode (LED) sources due to their inherent advantages in efficiency and lifespan in addition to their compact size. LEDs can provide up to four times the energy efficiency compared to incandescent lamps with lifetimes approaching 100,000 hours compared to the 750-1500 hour lifespan of incandescent bulbs [9]. Previously, compact fluorescent and linear fluorescent bulbs were a commonly used lighting technology as their energy efficiency matches that of

LEDs closely. However, LEDs have become more cost efficient as fluorescent lamp lifespans range from 6,000-10,000 hours in the case of compact fluorescents and 20,000 hours in the case of linear fluorescents [9]. Another prevailing lighting technology has been halogen lights with a lifespan of 2000-4000 hours [9]. LEDs may achieve energy efficiency values of three times that of halogen lamps. The combination of energy efficiency and greatly prolonged lifetimes over previous lighting technologies is a compelling reason to adopt LEDs.

The use of visible wavelengths (380nm - 780nm) to accomplish communications is termed visible-light communications (VLC) and is a subset of a larger group termed, optical-wireless communications (OWC) that encompasses the entire optical spectrum(100nm - 1mm) [10]. VLC is accomplished by modulating the intensity of light from an optical source, specifically LEDs in this thesis. LEDs with modulation rates of as high as 463 MHz have been demonstrated as in [11]. Conventional LEDs used for illumination achieve modulation bandwidths ranging from 2MHz to 10MHz [12]. As the usage of LEDs expands, using VLC has become a viable method of integrating communications in luminaires and providing a large number of devices information. In addition to a large number of links, these systems are immune to RF interference. The creation of a large amount of interference free links allows for a dense framework of communications to provide data to IoT devices. VLC also has inherent security benefits associated with the inability of light to penetrate objects, allowing it to be confined to specified areas. Use of this new and exciting technology will allow for relief of RF spectrum congestion and create a new method to transfer sensitive information with confidence.

1.1 VLC Standards and Influencers

Multiple standards exist governing VLC systems both directly and indirectly. Standards directly governing VLC are published by the Institute of Electrical and Electronic Engineers (IEEE) such as 802.15.7 and 802.11bb. Examples of standards that indirectly affect VLC systems are lighting and energy standards. The standards governing VLC systems demonstrate that there are challenges that must be overcome to allow for adoption of this technology. The commercialization of VLC devices shows that a market and role for VLC exists within the current technological framework. As better solutions are discovered to implement VLC transmitters, standards will be met and surpassed, resulting in VLC becoming a common wireless networking solution.

1.1.1 VLC Standards

In 2012, the IEEE 802.15.7 standard was created and defines both Physical (PHY) and Media Acess Control (MAC) layers to facilitate optical wireless communications using visible light. These links are designed to be short range and achieve rates ranging from tens of kbps to tens of Mbps used to allow for audio and video multimedia services. This standard discusses colour shift keying (CSK), On Off Keying, and variable pulse-position modulation (VPPM) as modulation techniques. Dimming for each modulation is explored in addition to their impacts on VLC. [13] An extension of IEEE 802.15.7 is IEEE 802.15.7m which develops the standard further to include optical camera communications (OCC) and low rate photodiode communications. This standard expands the wavelengths used to include infrared (700-1000nm) and ultraviolet (100-400nm) in addition to visible light. It also includes more methods of modulation such as pulse-width modulation (PWM), pulse-position modulation

(PPM), and orthogonal frequency-division multiplexing (OFDM) to achieve higher rate links [14].

1.1.2 Lighting and Energy Standards

The work to integrate VLC with the current set of 802.11 standards is being developed under the 802.11bb Task Group on Light Communications. This standard considers wavelengths ranging from 380nm to 5000nm which includes visible and infrared light. The standard specifies a minimum link rate of 10Mbps and a possible link of up to 5Gbps [15].

Standards for lighting are defined by governments and organizations for minimum lighting levels in a specified area as well as quality of light produced. For example, ranges for the amount of illuminance (Lux - discussed in Chapter 2) are designated for specific tasks [16]. Lighting quality can be controlled by setting minimum values of the colour rendering index(CRI) and correlated colour tempeprature(CCT). These are measures of the ability of a light to reproduce colours accurately and what the colour of the light is with reference to sunlight [8, p. 16] [17]. Another important measure of light quality for VLC is light flicker. Light flicker is defined as rapid changes in brightness over a given time frame. Depending upon the amplitude and rate of change, flicker can be a health and safety concern [18] [19].

Energy standards place limitations on energy efficiency and electromagnetic interference (EMI). These are of concern for many VLC systems due to possible decreases in energy efficiency to allow for communications in conjunction with EMI resulting from required switching for modulation. Many products sold are labeled with *Energy Star* compliance. This is a voluntary program for manufacturers, however it is a great

marketing tool. In order to be Energy Star compliant, a LED luminaire of less than 5W must have a power factor of greater than or equal to 0.5. For LED luminaires above 5W, a minimum power factor of 0.7 must be achieved [17]. Furthermore, an LED light meeting Energy Star standards must have a minimum luminous efficacy which can vary depending upon the intended purpose of the luminaire [17]. The *International Electrotechnical Commission* (IEC) and *European Standards* (EN) have created guidelines for minimum harmonic distortion of luminaires connected to the grid. This is is outlined in IEC/EN 61000-3-2, with lighting specifically detailed as being class C devices [20].

1.1.3 Influencers

In addition to the standards discussed, multiple companies are focusing on implementing VLC. A non-exhaustive list of companies include, pureLiFi [21], Philips and their company Signify [22], and Lucibel [23]. Bi-directional VLC links are being provided by pureLiFi for a variety of applications including hospitals, where Wi-Fi networks can interfere with medical equipment such as magnetic resonance imaging(MRI) [24]. Philips under the name Signify, has integrated VLC luminaires to transform shopping by locating and specializing promotional offers to shoppers in Carrefour stores [25]. Lucibel is partnered with pureLiFi and offers lighting solutions for bi-directional VLC links.

1.2 Implementation of VLC

Although VLC holds great promise for RF interference free, ubiquitous connectivity, implementation of energy efficient VLC modulators is an open problem. It is important to realize that while high rate VLC is possible, it will not be commercially relevant if it is not both cost effective and energy efficient. In order to drive LEDs and maintain energy efficiency, switched-mode power supplies (SMPS) are used. There are many different topologies that may be used that will be discussed in greater detail in Chapter 2. Cost of a product is generally scaled with component count. More complex designs with a greater number of components will cost more. Therefore, it is important to keep total components used to a minimum.

To implement a VLC transmitter, the application it is used in must be understood. Indoor lighting is among the most common use case for VLC. Traditionally, AC lines are used to power indoor lighting solutions, however power-over-Ethernet (PoE) is quickly being adopted as a power source [26]. PoE is an ideal technology to deliver both power and data to VLC luminaires. The use of PoE supplies 44-57 VDC at powers from 15-100 W along with up to Gbps data connectivity [27]. The DC power supplied over PoE is input to a step-down DC-DC converter to ensure the proper current output to the illumination LEDs. In addition to indoor lighting, LED technology has become ubiquitous for car headlights and tail lamps [28] [29]. This, combined with the trend of developing autonomous vehicles by researchers [30] and companies such as, Tesla [31], Waymo [32], comma.ai [33], and various car manufacturers creates a possible application of VLC between cars. Car batteries are typically 12V, while LED headlights often use a large amount of LEDs in series making higher supply voltages necessary. This scenario requires step up DC-DC conversion.

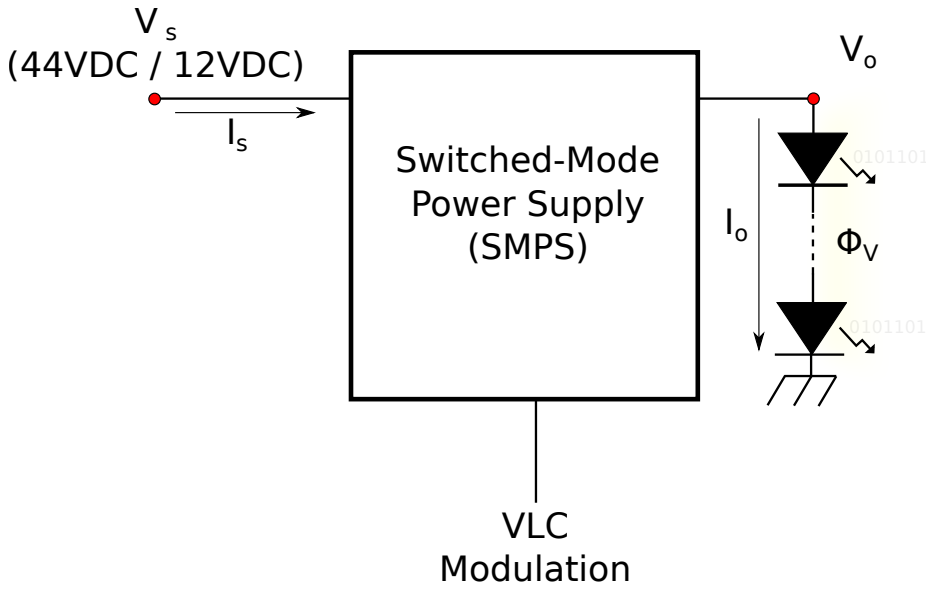

Figure 1.1: Block diagram of a VLC modulator with applicable design characteristics labeled.

Figure 1.1 gives a block diagram of a VLC modulator. Design parameters such as source voltage (V_s), input current (I_s), output voltage (V_o), and output current (I_o) are determined by the application VLC will be used in and the required number of illumination LEDs. The number of LEDs required will be a function of the LEDs used and desired amount of illumination.

When comparing lighting technologies, important specifications are electrical efficiency (η_E), and luminous efficiency (η_O), referred to as *efficacy*. A Mathematical definition of electrical efficiency is,

$$\eta_E = \frac{P_{OUT}}{P_{IN}}. \tag{1.1}$$

where P_{OUT} and P_{IN} are defined by,

$$P_{OUT} = V_o I_o, \quad \text{and} \quad P_{IN} = V_s I_s. \tag{1.2}$$

Efficacy is the measure of light output versus the input electrical power. The units used to express it is most commonly lumens per Watt($\frac{lm}{W}$). Efficacy is defined to be,

$$\eta_O[\frac{lm}{W}] = \frac{\Phi_V}{P_{IN}}. \tag{1.3}$$

Measures of light output such as radiant flux, luminous flux, and illuminance are discussed in greater detail in Chapter 2.

Distinguishing between LED efficacy and overall converter efficacy is important. Many datasheets provide an LED's efficacy, η_O^{LED}. When LEDs are used within a SMPS, LED efficacy is scaled by the converter's electrical efficiency, n_E^{SMPS}. Overall efficacy, η_O, is

$$\eta_O = \eta_E^{SMPS} \eta_O^{LED} \tag{1.4}$$

This provides overall SMPS efficacy and is the metric used to compare luminaires in this thesis.

In conclusion, an ideal VLC modulator would combine high efficacy and high data rate capability with low cost. This solution may be different depending upon the given application of VLC due to changes in operating parameters. It is accepted that SMPS topologies provide high efficacy solutions for LED lighting. What topology to use and how to integrate VLC modulation is a difficult and open engineering problem.

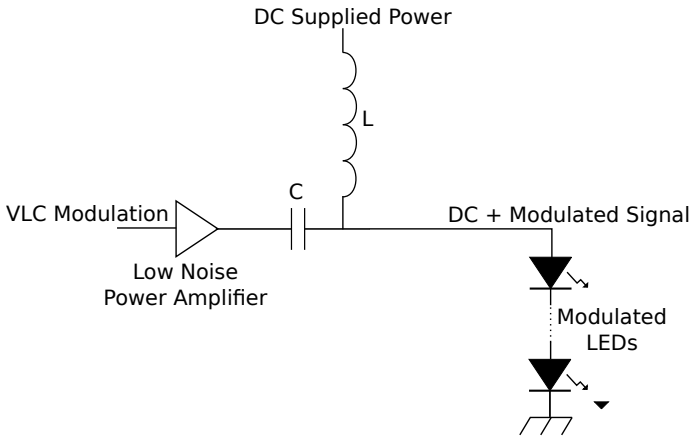

Figure 1.2: Simplified diagram of bias-T modulator for VLC.

1.3 Previous Approaches to VLC Transmitters

There have been many proposed solutions to the problem of creating efficient, high rate communications links with SMPS integration. Despite the length of time VLC has been researched, a single solution to integration within power converters has not been agreed upon. Many of the previous approaches to VLC transmitters have been demonstrated with a simple SMPS termed a buck converter. This topology and others will be explained in greater detail in Chapter 2. The approaches to realizing VLC transmitters presented are compared and contrasted to understand the advantages and disadvantages of each.

Bias-T

A simple diagram depicting a bias-T solution to a VLC transmitter is shown in Figure 1.2. A DC power supply is combined with a high speed low noise amplifier through a capacitor. The use of a bias-T is an example of an external modulation approach to VLC modulation which permits high data rates and a supports a wide

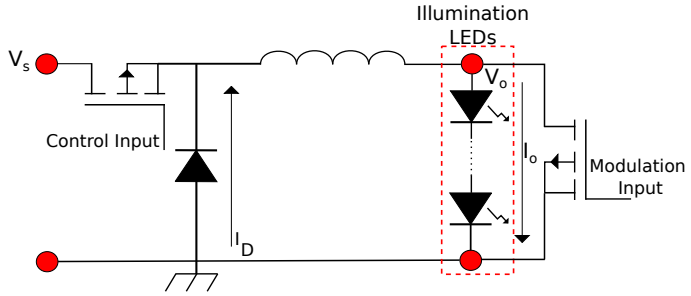

Figure 1.3: Example of shunting based approach to buck converter VLC integration as shown in [12], [36], and [37].

variety of modulation schemes [34] [35]. To use a bias-T, LEDs must be biased below their maximum operating current. This results in lower average brightness compared to non-modulated luminaires. A bias-T decreases achievable brightness, efficiency, and increases cost of a VLC modulator. Despite its ability to offer high rate VLC, inefficient and costly implementation makes this approach not commercially viable.

Shunting of Output LEDs

A more recent approach is to integrate the modulator into the DC-DC converter in order to preserve efficiency. One approach is to shunt illumination LEDs using an additional switch as shown in Figure 1.3.

The switch is connected in parallel with illumination LEDs in order to provide an alternate output current path and turn off illumination LEDs [12] [36] [37]. Although this design retains efficiency and provides high data rate, the output brightness of the luminaire is scaled by the duty cycle of the shunting switch. The use of a high speed switch capable of the same current as the illumination string increases cost of this transmitter approach significantly. Additionally, the reduction in output brightness requires the use of more LEDs or LEDs capable of higher brightness. It should be

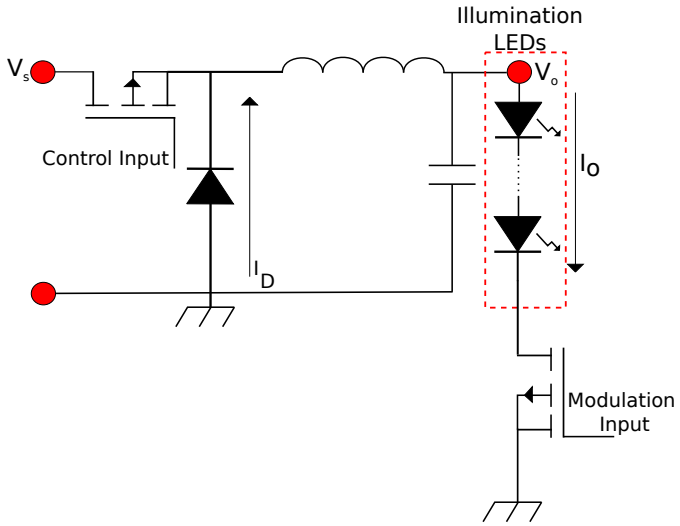

Figure 1.4: Example of series switch based approach to buck converter VLC integration as used in [12], [35], and [39].

noted that this design does not include an output capacitor as the shunting switch would short the capacitor. This results in a larger inductor being required. A VLC transmitter that shunts output LEDs has multiple sources of increased cost over a conventional luminaire.

1.3.1 Series Switch for LED Modulation

Alternatively, it has been suggested to use a switch in series as opposed to in parallel with illumination LEDs as shown in Figure 1.4 [12] [35] [39]. This would allow for a variation of output current by controlling a field-effect transistor (FET) in the linear region. This approach enables a large variety of modulation techniques and high achievable data rates. The disadvantage to this approach is the amount of power dissipated by the series switch and difficulty manufacturing a switch capable of handling large current values at high bandwidth. As with all previous approaches

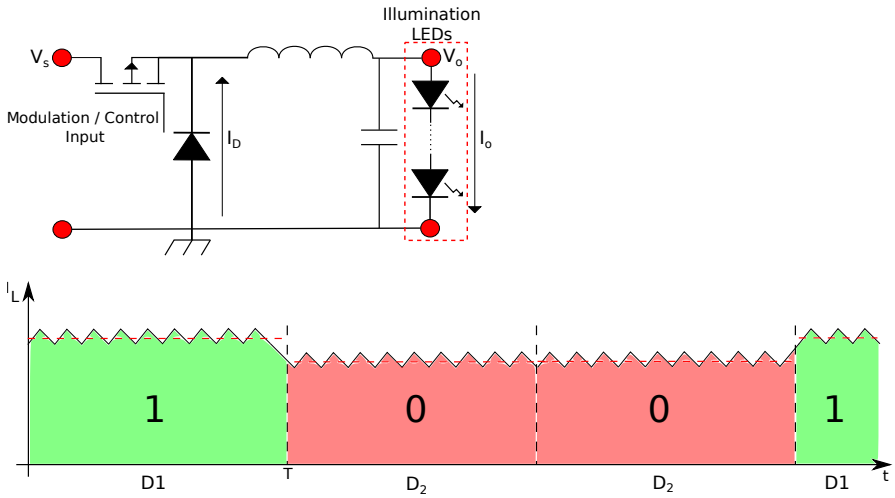

Figure 1.5: Slow variation of PWM to encode data. Example duty cycle D_1, greater than D_2.

discussed, average output brightness is decreased resulting in increased luminaire cost. This technique does not seem commercially viable as efficiency is reduced and cost is increased to enable high rate VLC.

1.3.2 Slow Varying Light Output via Pulse Width Modulation(PWM)

Figure 1.5 demonstrates an approach to integrating VLC into an LED driver by use of pulse width modulation (PWM). PWM will be described in greater detail in Section 2.3.1 of Chapter 2. Brightness varies slowly as high frequencies are filtered by the inductor and output capacitor. While this approach maintains a desired brightness, is efficient, and inexpensive, it has very low achievable data rates of approximately one tenth of the converter switching frequency [12] [36] [37]. The simplicity of this approach makes it a compelling solution to a VLC transmitter, however there are

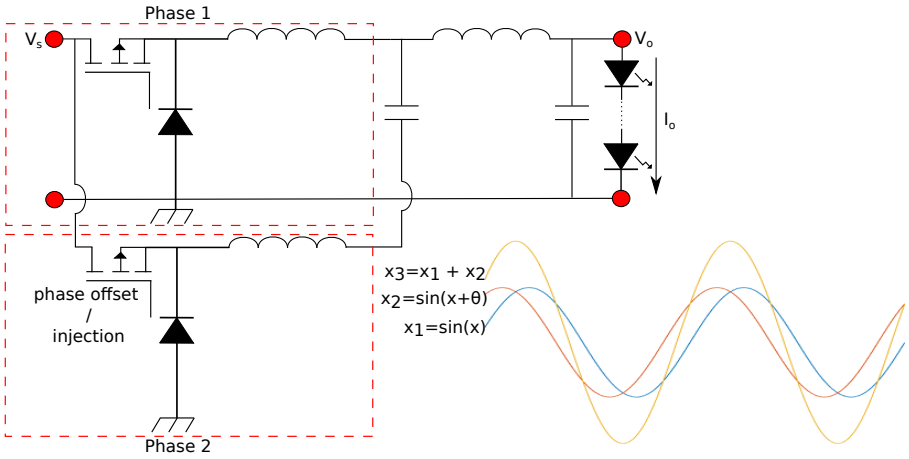

Figure 1.6: A Multi Phase Interleaved buck converter approach to VLC integration as shown in [38].

inherent limits to the communications bandwidth of this approach.

1.3.3 Multi-Phase(Interleaved) Converters

A new approach discussed in [38] demonstrates the use of a two phase buck converter to send data with changes in output ripple. This is achieved by controlling the phases of switches within each phase of the multi-phase buck converter. Constructive and destructive addition of two sinusoids is leveraged to produce an output signal. Figure 1.6 demonstrates this idea using a two-phase buck converter. Efficiency is maintained for this topology and high data rates may be achieved at the expense of using more components and greater design complexity. A multi-phased design was also demonstrated as a method of injecting a desired signal on top of a DC bias supplied by the main converter phase similar to that of a bias-T [39]. The number of components scales linearly with the number of phases added to the converter and results in greatly increased VLC transmitter cost.

1.4 Thesis Contributions

This thesis describes and demonstrates a new method of integrating VLC modulation into LED drivers with constant output brightness, high modulation frequencies, and increased efficacy as published in [40]. The use of light emitting freewheeling diodes(LEFD) and light emitting blocking diodes (LEBD) replaces existing components to integrate VLC in power conversion. Consequentially, the proposed solution is cost-effective as the total number of components required for a VLC transmitter is not increased.

All previous approaches to VLC transmitters modulate illumination LEDs to perform communications. This thesis presents a method of separating illumination LEDs from modulated LEDs. This allows for the use of an output capacitor in SMPS without a reduction of modulation bandwidth, making designs simpler. Additionally, VLC modulators using this approach have increased illumination quality and lifespan.

Many VLC transmitter designs focus solely on integration within step-down SMPS. This is remedied by the work in this thesis and a step-up converter is also considered. By demonstrating the use of freewheeling and blocking diodes as a source of VLC in buck and boost converters, other SMPS topologies with galvanic isolation are simple extensions of the proposed designs.

All proposed designs were simulated and prototypes have been built for verification. The contributions presented for VLC modulators bring them one step closer to being a widespread solution to wireless networking.

1.5 Thesis Outline

Chapter 2 provides background information concerning the concepts of lighting, operation of diodes and LEDs, power conversion, and modulation schemes for use in VLC transmitters. Chapter 3 proposes the use of LEFDs within buck converters to allow for VLC. The concept, simulations, and experimental results are presented and discussed. Similarly, in chapter 4, LEBDs are proposed and their uses within boost converters are analyzed. Chapter 5 concludes the results of simulation and experiments within this thesis. Possible extensions of this work will also be discussed.

Chapter 2

Switching Power Converters and Illumination

This chapter presents the relevant concepts required to integrate VLC within power converters. The principles of illumination, characteristics of diodes, and principles of switching power conversion are reviewed to give appropriate context to the work described in this thesis.

2.1 Illumination and Diode Characteristics

2.1.1 Measurement of Light

Light output is quantified by two possible measures: radiometric, and photometric. Radiometric measurements, referred to as radiant flux (Φ_e), are given by total optical output power at each given wavelength (λ) and are measured in Watts (W). A

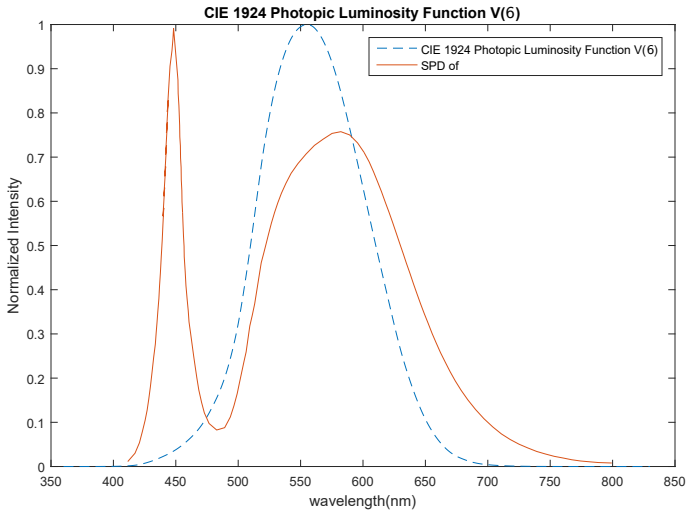

Figure 2.1: CIE Photopic response function of the human eye as plotted from equation found in [43] and spectral power distribution(SPD) of a Philips 3535L LED [44] plotted using data extracted from the datasheet.

mathematical definition of radiant flux is given by

$$\Phi_e = \int P_e(\lambda) d\lambda, \tag{2.1}$$

where P_e is the spectral power distribution(SPD) of a light source measured in $\frac{W}{nm}$. This distribution gives the amount of energy present for a given wavelength [41]. An example SPD curve for the white LEDs used in this thesis is given in Figure 2.1.

Photometric measurements account for the sensitivity of the human eye to particular wavelengths. This is done by scaling radiometric quantities by sensitivity curves. Depending upon lighting conditions, eye sensitivity can be described by the photopic sensitivity curve or the scotopic sensitivity curve. Lighting levels are typically expressed using the photopic sensitivity curve [8, p. 28-32]. The scaled measure of radiant flux is referred to as luminous flux, measured in lumens (lm) [42] [43].

Luminous flux is defined by

$$\Phi_V = K \int_{\lambda=380nm}^{\lambda=780nm} P_e(\lambda) V(\lambda) d\lambda, \tag{2.2}$$

where K is a constant scalar($683\frac{lm}{W}$) used due to a change in units [44, p. 232] and $V(\lambda)$ is the photopic response function of the human eye. The photopic response is depicted in Figure 2.1. The equation used to define the photopic sensitivity curve,

$$V(\lambda) = 1.019e^{-285.4(\lambda-0.5559)^2}, \tag{2.3}$$

was established by the *International Commission on Illumination* (CIE) in 1924 and has been used to present day [43].

Radiant Flux is measured in Watts (W) and is the measure of total optical power produced by a source. This is not typically a measure for lighting as the photopic response accounts for the sensitivity of the human eye.

In order to quantify luminous flux, measured in lumens (lm), a device termed an integrating sphere is required. This tool should be larger than the source attempting to be measured by a factor of four or five [8, p. 189-191]. Additionally, when the light shines into the sphere, the device converting the light into an electrical signal (typically a photodiode) must not have a direct line of sight to the source. This is to avoid saturation of the device measuring the light. Integrating spheres are usually calibrated with a known light source to ensure accurate readings [8, p. 189-191].

Illuminance is a measure of luminous flux for a given area and is measured in lumens per square meter ($\frac{lm}{m^2}$). Measuring illuminance is much easier and less costly than measuring luminous flux because an integrating sphere is not required. To

measure illuminance, a lux meter is used. These devices are sensitive to changes in distance as measurements are proportional to the square of distance from a light source. To obtain precise measurements with a lux meter, measured distance should be fixed. Additionally, measurements should be taken in line with the axis of the luminaire attempting to be measured. This is because luminaires typically do not produce uniform distributions of light. If one measurement is taken and compared to another at the same distance but slightly off center, the lux is different [8, p. 187-189].

The photometric quantities of luminous flux (lm) and illuminance ($\frac{lm}{m^2}$) and their corresponding measurement devices are used in Chapters 3 and 4.

2.1.2 Diode Characteristics

Diodes are typically created by the interfacing of p and n-type semiconductors [45, p. 110]. This structure creates a device that allows current flow in a single direction while impeding flow in the opposite. [46] Figure 2.2 gives an overview of different diode parameters and models discussed within this Section. When referring to diode operation, a diode is referred to as either forward biased or reverse biased. The bias voltage (V_{bias}) is defined as the the voltage drop from anode (V_+) to cathode (V_-).

If bias voltage is above the diode's forward voltage (V_f), the diode is forward biased. Conversely, a lower voltage than V_f results in a reversed biased diode. An ideal diode acts as an ideal switch and would have a V_f of zero as shown in Figure 2.2a.

Diodes, and by extension LEDs, in practice have I-V characteristics that are modeled as an exponential curve as shown in Figure 2.2c. As bias voltage increases,

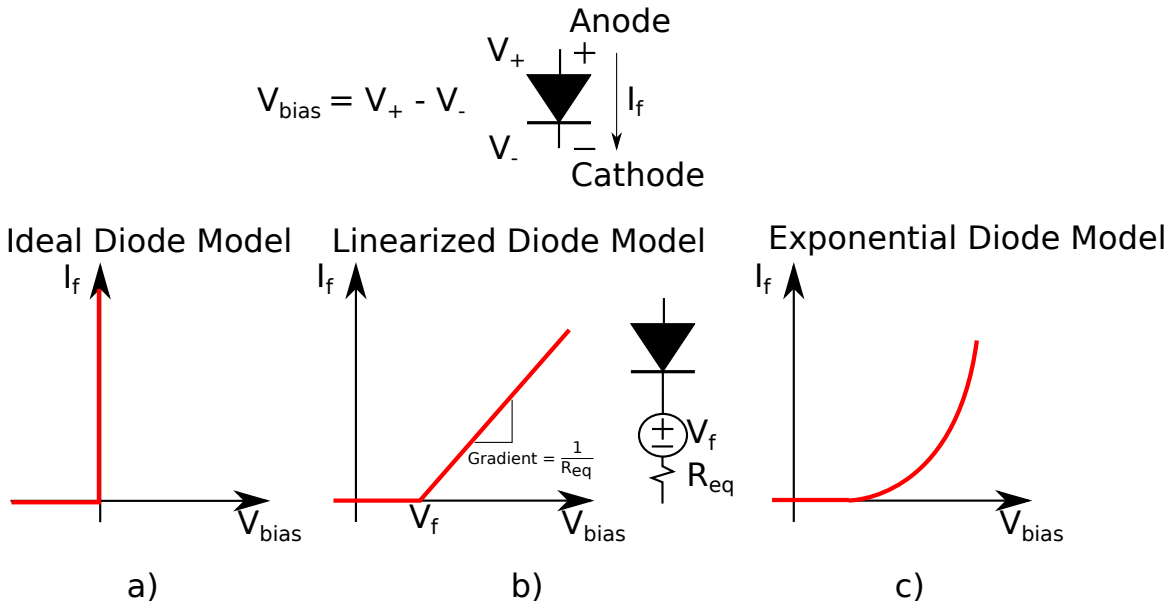

Figure 2.2: A diagram of a standard diode is presented with example I-V characteristics for the ideal case, linearized case, and exponential case.

forward current increases exponentially as described by

$$I(V_{bias}) = I_0 e^{k * V_{bias}} \tag{2.4}$$

and is relevant for all bias voltages. Th paramaeter I_0, is termed the saturation current and is used as a scalar of current [8, p. 47]. Voltage is scaled by k which is temperature dependant[p. 47] [8]. These constants are approximations of diode parameters, typically at room temperature.

The I-V characteristics of a diode may be idealized to have a constant forward drop and a forward current dependent upon biasing voltage [47]. This linearized model is depicted in Figure 2.2b and is often used to simplify the analysis. This relationship

is described mathematically by

$$I_f = \frac{V_{bias} - V_f}{R_{Deq}}. \tag{2.5}$$

The linear diode model is only valid when the diode is forward biased. This model will be used for the work presented in Chapters 3 and 4.

A capacitance termed the *junction capacitance*, is responsible for the amount of time it takes to turn on a diode as charge must be accumulated [45, p. 115]. Before the diode can turn off and block current, it must dissipate all stored charge. This takes a longer time than turn on and is referred to as reverse recovery, t_{rr} [45, p. 115]. These turn-on and turn-off times are responsible for the bandwidth of a diode. In Section 2.2.3, t_{rr} will be identified as an important factor for switching losses of diodes.

Reverse breakdown voltage of a diode is the result of a large of enough reverse bias voltage and causes current to flow in the opposite direction it typically would [45, p. 113]. LEDs as with any diode realized in practice have a reverse breakdown voltage that can be measured. At a specific reverse bias voltage, the diode will undergo reverse breakdown [45, p. 113]. The voltage level that this occurs at is a property of a diode dependent upon geometry and material combinations [48]. A study of the effects of reverse biasing LEDs and the effects of electrostatic discharge (ESD) are described in [49].

2.1.3 Light Emitting Diodes and Illumination

By definition, LEDs are diodes specifically designed for their light producing properties. They follow the same operating principles conventional diodes do although parametric values may change. In addition to their electrical characteristics, each

LED has their own characteristic equation for lumen output given a forward current. A linear model is popular, however, in general the relationship is non-linear. Characterization of this relationship is typically done through measurement and curve fitting [8, p. 221-223]. The work in Chapters 3 and 4 is presented with non-linear fits of the LEDs used.

White light is preferred for illumination and cannot be generated via a single LED without additional elements as it is created by the mixture of multiple wavelengths across the visible spectrum. To produce white light, one of two methods are used; a blue LED with a phosphor coating, or a combination of red, green, and blue LEDs with light combined and summed spatially. Blue LEDs combined with a phosphor are more common due to their simplicity and being more economical to produce [8, p. 3-4].

2.2 Switched-Mode Power Supplies(SMPS)

Many SMPS topologies exist, their purpose ranging from AC/DC conversion, DC/AC conversion, and DC/DC conversion. DC/DC converter topologies are typically used for LED driver designs, an overview of LED driver topologies and control schemes is provided in [50]. Despite losses from the switch and other components, it is still possible to achieve efficiencies of greater than 90% from SMPS LED drivers [51].

Each of these types of converters may or may not be galvanically isolated. Galvanic isolation separates the input power source from that of the output of an electrical circuit both physically and electrically. This is typically accomplished by use of a transformer. Galvanic isolation can help to reduce noise on the secondary side of the transformer and provide protection for both powered devices and people [52]. The focus of this thesis will be non-galvanically isolated DC/DC conversion as these

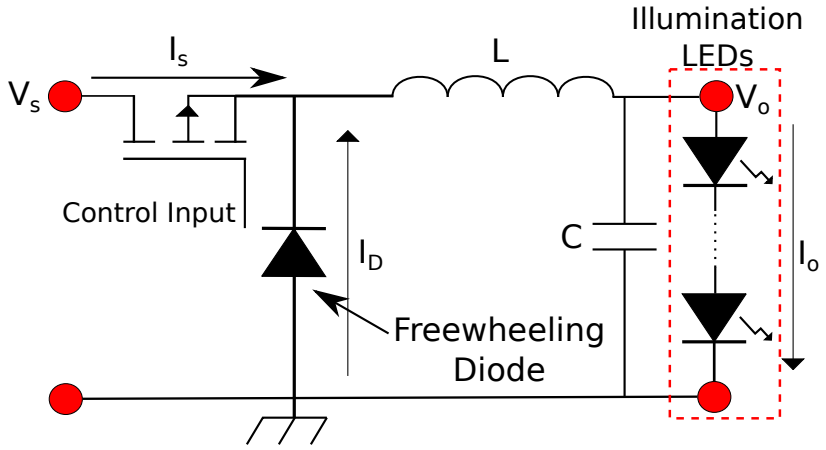

Figure 2.3: Diagram of base case buck converter using a standard freewheeling diode.

circuit topologies are less complex making them easier to analyze and prototype. The specific topologies that will be considered and checked for feasibility and performance are the buck and boost converters which step-down and step-up voltage respectively.

2.2.1 Buck Converter Theory of Operation

A buck converter is an example of a "step down" switching power supply and therefore is useful for applications that require a lower voltage than supplied such as indoor lighting. This topology is commonly used for LED drivers due to its high efficiency and ability to act as a constant current source [12].

Define the *base case* buck topology to be a buck converter with a standard freewheeling diode as shown in Figure 2.3. This base case buck topology will be used as a reference when evaluating designs used in Chapter 3.

The following described operation assumes a constant and positive current through the inductor. This is termed continuous conduction mode (CCM) as opposed to discontinuous current mode(DCM) where inductor current may reach zero [53]. CCM is

preferred as it is more efficient to operate in this regime. Both switching and conduction losses, discussed in more detail in Section 2.2.3, are lower for converters operating in CCM compared to those operating in DCM [54]. In addition to efficiency of SMPS operating in CCM being greater than those operating in DCM, CCM is preferred due to lower peak currents present. Higher peak currents from SMPS operating in DCM result in greater strain on components. Due to this, converters operating in DCM require components that are more robust which can increase converter cost.

A buck converter varies the ratio of time that a control switch is conducting (t_{ON}) and non-conducting(t_{OFF}) over a given period [46, p. 198]

$$T = t_{ON} + t_{OFF}. \tag{2.6}$$

The switching frequency, f_{sw}, of a converter is defined to be [46, p. 198]

$$f_{sw} = \frac{1}{T}. \tag{2.7}$$

Duty cycle, D, can be described by the previous values as shown in, [46, p. 198]

$$D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{t_{ON}}{T} = t_{ON} f_{sw}. \tag{2.8}$$

This thesis assumes that all uses of the term *duty cycle* refers to the ratio defined for SMPSs.

The operation of a buck converter can be described by the two phases of the control switch. The conduction phase allows for power from the source to charge an inductor. During this phase, the freewheeling diode is reverse biased by V_s. Therefore,

reverse breakdown voltage must be greater than V_s. While the switch is not conducting, the power stored within the inductor can be discharged. During this phase, a freewheeling diode will conduct allowing for current to flow and preventing inductive voltage spiking. The time the freewheeling diode is conducting can be defined as the compliment of the switch,

$$t_{OFF} = (1 - D)T. \tag{2.9}$$

The time a freewheeling diode conducts is a useful result used in Chapter 3.

By varying duty cycle, the output voltage and current can be limited. Output voltage of a buck converter is directly proportional to duty cycle as described by, [46, p. 202]

$$V_o = V_s D. \tag{2.10}$$

In Chapter 3, a new relationship for buck converter output voltage will be presented that does not assume negligible forward drop of the freewheeling diode.

Through the use of basic converter parameters, various buck converter component values may be computed. Many of these values are computed to be minimum values and the use of larger component values will result in more stable operation.

Given knowledge of the load, duty cycle, and switching frequency, the minimum inductor size can be computed to maintain CCM given by [46, p. 203]

$$L_{min} = \frac{(1 - D)R}{2f_{sw}}. \tag{2.11}$$

This assumes a large output capacitor capable of maintaining constant V_o [46, p. 203].

The change in current over a single period is defined as the ripple current, Δi_L. For a given inductor, current ripple is calculated to verify CCM and follow design

specifications. This is defined by, [46, p. 203]

$$\Delta i_L = \left(\frac{V_s - V_o}{L}\right) DT = \left(\frac{V_s - V_o}{L f_{sw}}\right) D = \frac{V_o(1-D)}{L f_{sw}}. \tag{2.12}$$

Equation (2.12) may be used to appropriately choose how much to oversize an inductor to meet criteria of standards or design goals.

The final component that must be sized is the output capacitor. Minimum capacitor size can be calculated from

$$C = \frac{1-D}{8L(\frac{\Delta V_o}{V_o})f_{sw}^2} \tag{2.13}$$

for a desired output voltage ripple (ΔV_o) [46, p. 205].

The buck converter is a simple topology that when designed correctly allows for high efficiencies to be realized. It also is an ideal topology for LED drivers as it can be used as a constant current source.

2.2.2 Boost Converter Theory of Operation

The boost converter is used in applications where supplied voltage is lower than required such as in a car headlamp. This topology is also commonly used for LED luminaries due to its high efficiency and ability to act as a constant current source [55].

Define the *base case* boost topology to be a boost converter with a standard blocking diode as shown in Figure 2.4. This base case boost topology will be used as a reference in Chapter 4.

Just as in the buck converter example, CCM is assumed for the boost converter and definitions for T, f_{sw}, and D remain the same for the boost converter. During

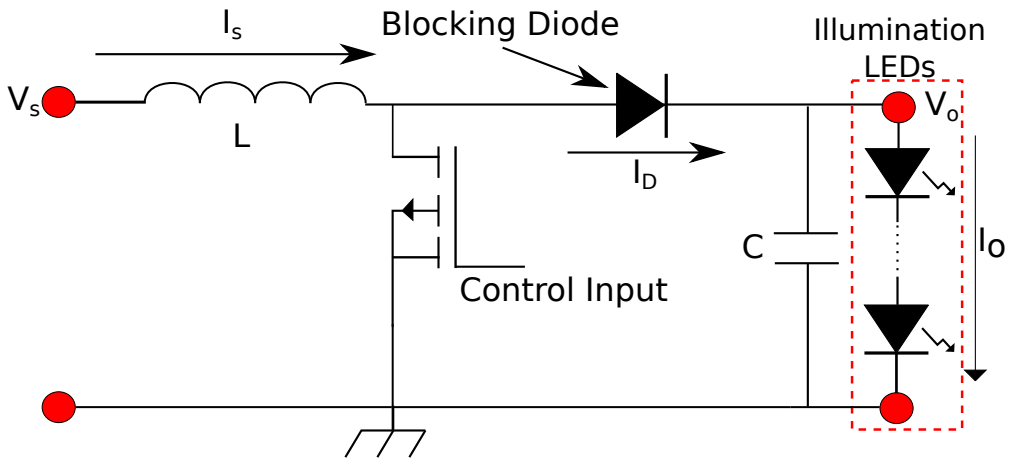

Figure 2.4: Diagram of base case boost converter using a standard blocking diode.

the conducting phase of the switch, the inductor is charged and the blocking diode prevents the output string from being short circuited to ground. The blocking diode is reverse biased by V_o. Therefore, reverse breakdown voltage must be higher than the desired V_o. The non-conducting phase of the switch discharges the inductor as the output voltage is higher than supplied voltage. The relationship for output voltage is described by, [46, p. 214]

$$V_o = \frac{V_s}{(1-D)}. \tag{2.14}$$

Similar to the buck converter, this assumes an ideal diode with zero forward drop. A new output voltage relationship will be defined in Chapter 4 which includes the effects of blocking diode forward voltage.

Minimum inductor size to maintain CCM is, [46, p. 215]

$$L_{min} = \frac{D(1-D)^2 R}{2f_{sw}}. \tag{2.15}$$

A useful version of this is defined by ripple current. Given a desired ripple current

the inductor size may be calculated as given by, [46, p. 213]

$$L = \frac{V_s DT}{\Delta i_L} = \frac{V_s D}{\Delta i_L f_{sw}}. \tag{2.16}$$

Finally, [46, p. 216]

$$C = \frac{D}{R(\frac{\Delta V_o}{V_o}) f_{sw}} \tag{2.17}$$

gives capacitor sizing in order to maintain a given voltage ripple. A capacitor of large value allows for a steady output voltage, however this will also lead to long start-up transients.

2.2.3 Power Losses

The law of conservation of energy states that total input power must be equal to total output power for any circuit as stated in

$$P_{IN} = V_s I_s = P_{OUT} = V_o I_o. \tag{2.18}$$

Output power can be split into useful power and losses as described by

$$P_{OUT} = P_{useful} + P_{loss}. \tag{2.19}$$

While there are likely numerous alternative sources of losses that are not accounted for, power losses can be split into conduction and switching losses as described by,

$$P_{loss} = P_{cond} + P_{switch}. \tag{2.20}$$

The two main components considered when discussing conduction and switching losses are the control switch and the freewheeling or blocking diode.

Conduction losses are proportional to the current through the converter and parasitic resistances of devices used. This includes passive components such as capacitors and inductors. One example of conduction loss is from freewheeling and blocking diodes. By assuming the linearized diode model shown in Figure 2.2 the power lost to a diode during conduction, $P_D^{conduction}$, is described by, [56] [57]

$$P_D^{conduction} = V_f I_{Davg} + R_{Deq} I_{Drms}^2. \tag{2.21}$$

This loss is scaled linearly with V_f and is an important consideration used in Chapters 3 and 4. It is also increased by R_{Deq} and the square of root mean square (RMS) current [46, p. 34]. Conduction losses of the control switch in a SMPS occur during the conducting phase of a switch. These losses are scaled by an equivalent resistance of the FET, R_{DSon} and are described by, [57]

$$P_{SW}^{conduction} = R_{DSon} I_s^2. \tag{2.22}$$

Conduction loss in a switch is also proportional to the square of I_s, however, FET conduction losses are typically much lower compared to conduction losses of diodes [57].

Switches such as FETs have switching losses caused by parasitics such as resistances, capacitances, and inductances. These slow the switching transition process and dissipate energy as heat [58]. Switching losses of both diodes and the control switch are proportional to f_{sw} [57] [59]. This means that while a higher switching

frequency will allow for smaller component values in both buck and boost SMPSs, losses will be increased. Relationships for switching loss of diodes and control switches are derived in [59]. The diode switching loss, P_{Dsw}, is defined in terms of switching energies, E_{ONd}, and E_{OFFd}, as given by,

$$P_{Dsw} = (E_{ONd} + E_{OFFd}) f_{sw} \approx E_{ONd} f_{sw}. \tag{2.23}$$

The switching losses from a FET, P_{FETsw}, are also given in terms of energies, E_{ONsw}, and E_{FETsw}, as well as f_{sw} given by,

$$P_{FETsw} = (E_{ONsw} + E_{OFFd}) f_{sw}. \tag{2.24}$$

Reverse recovery of a diode is the main contributor to diode switching losses and accounts for a significant portion of losses in SMPS [59]. Longer values of t_{rr} will increase power dissipated and higher frequencies will force a diode to undergo reverse recovery more often. Therefore, t_{rr} and switch parasitics should be kept low to allow for high switching frequencies and low power dissipation.

The dominant source of loss in a converter can change as I_o changes as demonstrated by the prior discussion of conduction and switching losses. For lower currents, switching losses are more significant compared to conduction losses. Conversely, as load current increases, conduction losses increase significantly since they are proportional to the square of current.

2.3 Low-Complexity Optical Intensity Modulation Techniques for use in VLC Power Converters

There are many methods to accomplish modulation for VLC. Depending on the transmitter, some modulation schemes are more easily used than others. Schemes discussed in this thesis are all binary level and vary pulse width or position as this encompasses simple forms of modulation that can be applied to the control switch of SMPS. To demodulate sent data in Chapters 3 and 4, this thesis assumes maximum likelihood (ML) detection and uses match filtering to accomplish this.

Minimum distance, d_{min}, is a measure of the minimum Euclidean distance between any two sent symbols, x_i and x_j [60]. This is used to contrast the ease of demodulation for proposed modulation techniques and is described by

$$d_{min}^2 = \min_{i \neq j} \int (x_i(t) - x_j(t))^2 dt. \tag{2.25}$$

A larger minimum distance between signals implies a set that can be demodulated with a lower probability of error. Conversely, smaller minimum distances result in greater probability of error [61, p. 185]. From d_{min}, the equation for the probability of an error, P_{error} is upper bounded by [62, p. 140],

$$P_{error} \leq (M-1)Q\left(\frac{d_{min}}{\sqrt{2N_0}}\right). \tag{2.26}$$

Given the probability of error of a given symbol, bit error rate(BER) can be defined as, [62, p. 141]

$$BER = \frac{P_{error}}{log_2 M} \tag{2.27}$$

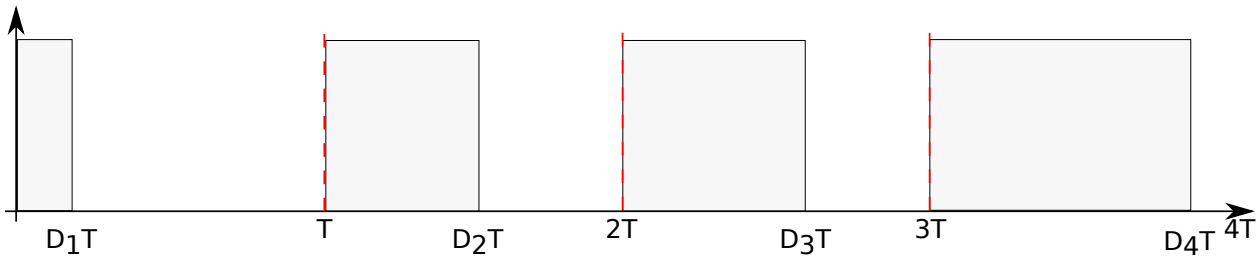

Figure 2.5: Illustration of Pulse Width Modulation for four increasing duty cylces, D_1,D_2,D_3, and D_4.

These equations assume that the signals sent have high signal to noise ratio(SNR) and that the most likely errors to occur are given by adjacent signals with the smallest d_{min}.

2.3.1 Pulse Width Modulation

PWM is achieved by varying the duration of a pulse, referred to in power electronics as the duty cycle, D. PWM is commonly used to alter average output power when passed through a system that low passes the signal. Figure 2.5 demonstrates a set of pulses with four different duty cycles.

2.3.2 Pulse Position Modulation

PPM assumes a fixed duty cycle or pulse width and data are transmitted by varying the position of the leading or trailing edge of a pulse. It is defined by splitting a period, T, into a set number of M sub-intervals as shown by Figure 2.6. M is referred to as the modulation order of PPM. The order of PPM defines naming conventions, for example, an M of two is referred to as BPPM (Binary-PPM), and an M of four is referred to as 4-PPM. This naming convention continues for increasing orders. To

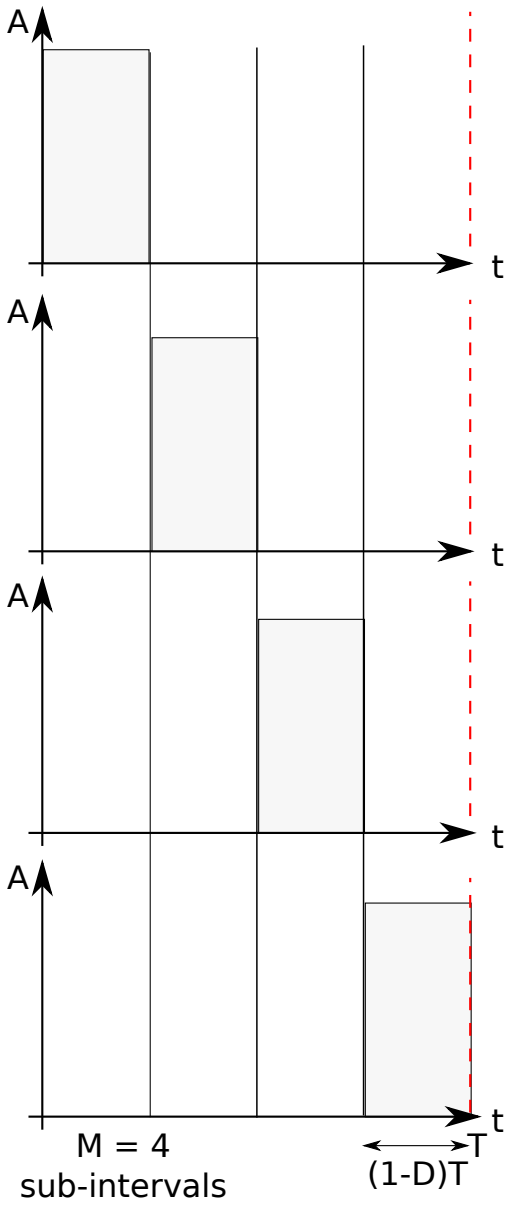

Figure 2.6: Four-ary Pulse Position Modulation (4PPM) with duty cycle D

define a mathematical expression for a sample PPM signal, first a rectangular pulse, $rect(t)$, is defined as,

$$rect(t) = \begin{cases} 1 & 0 \leq t \leq 1 \\ 0 & else \end{cases} \tag{2.28}$$

From this, a definition of a sample PPM signal is given by,

$$x_k(t) = Arect\left(\frac{t - \frac{kT}{M}}{(1-D)T}\right), \qquad \begin{matrix} k = \{0, .., M-1\} \\ \frac{M-1}{M} \geq D > 0 \end{matrix} . \tag{2.29}$$

where A scales the amplitude of the pulse and the width is $(1-D)T$. A shift by $\frac{kT}{M}$ defines symbols, where k selects what symbol to send out of M possible signals.

The symbols of PPM are all equidistant and d_{min} can be derived by substituting any two unique $x(t)_k$ for x_i and x_j in equation (2.25). This will yield an expression for d_{min} defined by

$$d_{min} = \sqrt{2A^2DT}, \quad \text{and} \quad \frac{M-1}{M} \geq D > 0 \tag{2.30}$$

that is not dependent upon the order of modulation. These definitions are only valid for duty cycles in the range $\frac{M-1}{M} \geq D \geq 0$ since duty cycles outside of that range will result in overlapping pulses and a separate type of modulation, overlapping-pulse position modulation(OPPM).

Overlapping Pulse Position Modulation

In order to enable dimming in a SMPS and send data with an order M modulation scheme, it is necessary to have duty cycles that do not support PPM. For these cases,

OPPM is defined. OPPM symbols shift the leading or falling edge position in equally spaced intervals of the period according to duty cycle as shown by Figure 2.7. Using equation (2.28), a sample OPPM signal will follow the following relationship,

$$x_k(t) = Arect\left(\frac{t - \frac{kDT}{M-1}}{(1-D)T}\right), \qquad \begin{matrix} k = \{0, .., M-1\} \\ 1 \geq D > \frac{M-1}{M} \end{matrix}. \tag{2.31}$$

Similar to the case of PPM, equation (2.25) can be used to defined d_{min} for OPPM. By substituting two unique sample symbols from equation(2.31) into equation (2.25), the minimum distance can be defined. This results in the following,

$$d_{min} = \sqrt{\frac{2A^2DT}{M-1}}, \quad \text{and} \quad 1 > D > \frac{M-1}{M}. \tag{2.32}$$

Overlapping of pulses causes the minimum distance of this modulatiom technique to depend upon modulation order. As modulation order increases, minimum distance decreases proportionally. This may limit the order of modulation that can be used as the probability of error increases with reduced d_{min}.

VPPM as a modulation technique is specifically defined in the the IEEE standard for VLC, IEEE 802.15.7 [13]. This concept is simply defined by the binary case of the more general modulation technique of OPPM.

2.4 Conclusion

This Chapter has presented the principles of illumination and typical methods of collecting these metrics. The principles of electrical operation of diodes and LEDs was presented as well as typical methods of producing illumination LEDs. The specific

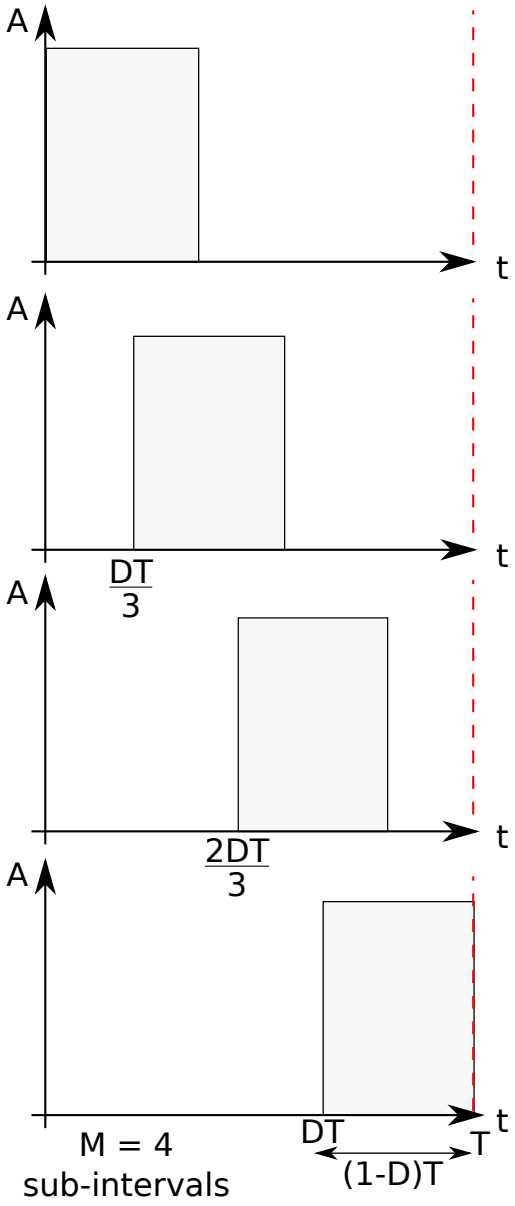

Figure 2.7: Four-ary Overlapping Pulse Position Modulation (4OPPM) with duty cycle D

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topologies of buck and boost converters were explained with details of component value selection based upon operating principles. Additionally, sources of loss within these SMPS were outlined for later discussion in Chapters 3 and 4. Finally, an overview of modulation techniques used within this thesis was presented. Definitions of sample signals were given with control of SMPS in Chapters 3 and 4 in mind. The metric of d_{min} was presented for the modulation schemes used in order to quantify effectiveness of communications.

Chapter 3

Light Emitting Freewheeling Diodes and Buck Converter Integration

In this chapter, a new method of integrating VLC modulation into a buck converter is presented. The concept is explored, including design considerations, and advantages over modulation techniques discussed in Chapter 2. By simulating and prototyping the proposed circuit with LEDs versus those of conventional diodes, characteristics were verified and potential design challenges were identified. The effects on efficiency, efficacy, and potential data rates are presented and discussed.

3.1 Concept

Freewheeling diodes are necessary for buck converter operation and are also a source of power loss within the circuit. Many buck converter designs attempt to minimize this

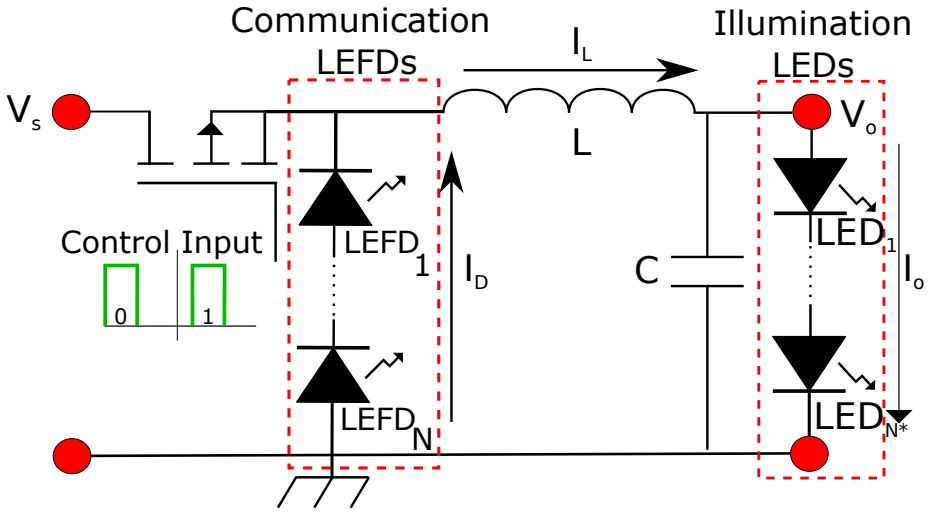

Figure 3.1: A buck converter with proposed light-emitting freewheeling diode (LEFD).

loss through the use of diodes with low forward bias (Eg. Schottky diodes) or replacing the freewheeling diode with a switch (synchronous converter) [63]. This thesis replaces the idea of minimizing loss with harnessing the lost power, that is, making it useful. To accomplish this, the freewheeling diode present in a standard buck converter is replaced with an LED, termed a *light-emitting freewheeling diode* (LEFD) as presented in Figure 3.1. Energy typically dissipated within the freewheeling diode is used to provide modulated illumination for VLC. Wavelengths outside of the visible range can also be used, for example, LEFD(s) that produce infrared light allow for invisible OWC. The use of LEDs outside of the visible spectrum will not contribute to overall luminous flux of the proposed design.

This design is able to modulate VLC signals at the full switching rate of the SMPS while remaining energy efficient. In addition to energy efficient modulation, the design supports a simple method of dimming through the use of PWM. By altering the duty cycle, the output power is scaled and the luminaire is dimmed. Choosing

a sufficiently large inductor to maintain CCM will accommodate a wide range of duty cycles and by extension a wide range of dimming levels. Another advantage to this approach is that, unlike earlier designs, LEDs modulated for VLC are separated from illumination LEDs. This is a property of the buck converter structure as the inductor (L) supplies constant current to illumination LEDs while communicating LEDs alternate between conducting and non-conducting states. A major concern for illumination is the degradation of LEDs which leads to colour shift and lumen depreciation [64]. Previously proposed VLC modulators discussed in Chapter 1 use illumination LEDs to support modulation. Reductions in lifespan, quality of colour, and lumen output are potential disadvantages of these approaches. The separation of communication LEDs and illumination LEDs provides a solution to minimize the effects of supporting VLC on the quality of illumination provided by the luminaire. This is accomplished by the proposed LEFD converter design.

3.1.1 Electrical Operation and Design Considerations

Replacement of freewheeling diodes with LEFDs cannot be done without careful assessment of the consequences replacing a conventional diode with an LED entails. Various elements of converter operation are affected and must be understood to produce a luminaire supporting VLC through use of LEFDs.

LEFDs are reverse biased by V_s as shown in 3.1. This reverse biasing may be problematic for LEFDs as as they are typically not designed to be driven in this manner (e.g., [65]). In cases where reverse breakdown of the LEFD is low in comparison to desired V_s, multiple LEFDs may be used in series. Additional LEFDs will alter circuit performance by increasing the forward drop present.

An additional significant difference between conventional diodes and LEFDs is that forward drop voltage is typically larger. A conventional diode may have a forward voltage of approximately 0.7V, while a conventional high power white LED will be in the range of 3V [65]. To denote this difference, when referring to V_f of LEFDs, V_f^{LEFD} is used. As with all diodes, material difference of LEDs can greatly impact forward drop [66]. Increasing forward voltage yields two major design considerations; impact of forward voltage on converter efficiency, and maximum achievable output voltage.

As discussed in Section 2.2.3 and described by equation (2.21), power consumption of a diode scales linearly with V_f and R_{Deq}. Additionally, $N \geq 1$ LEFDs can be used in series due to limitations of reverse breakdown voltage, as in Figure 3.1. The aforementioned losses will further be increased by a factor of N defined by,

$$P_{LEFD} = NV_f^{LEFD} I_{Davg} + NR_{Deq}. \tag{3.1}$$

The use of N LEFDs also will affect output voltage control. Increasing the number of LEFDs used in series will affect output voltage as a function of duty cycle as

$$V_o = (V_s + NV_f^{LEFD})D - NV_f^{LEFD}. \tag{3.2}$$

This equation demonstrates that V_f^{LEFD} will reduce V_o. A full derivation of this equation is supplied in Appendix A and has been derived with the assumptions of CCM and a large output capacitor for constant V_o. A duty cycle resulting in a negative output voltage means that the converter will not function in CCM and is not valid as it violates the assumption made to derive the equation. Additionally, when using

this relationship to design for a luminaire, multiple illumination LEDs may be used in series. This further places a restriction on permissible output voltage as it must be high enough to forward bias all illumination LEDs. This changes how duty cycle must be chosen to yield a desired output. To achieve the same V_o and I_o as the base case buck converter in Chapter 2, higher duty cycles must be used in converters using LEFD(s). However, this is not an issue since LEFD(s) provide illumination in addition to communications. This results in a converter that uses lower values of V_o and I_o to achieve the same illumination as the base case.

Use of multiple LEFDs will result in higher losses and lower output range. Therefore, unless required, for the greatest efficacy and output range the number of LEFD(s) used should be minimized. If dimming is not required and lower efficacy is acceptable, a greater number of LEFDs may be used to improve communications performance by transmitting greater power.

3.1.2 Communicating with LEFDs

Prior designs demonstrated in Chapter 1 introduce modulation where light would otherwise be constant (DC). As previously mentioned, VLC modulators using LEFD(s) separate LEDs used for communications and illumination. This means that illumination LEDs are driven by constant current (DC) while LEFD(s) are modulated. The modulation schemes considered are specifically PPM and OPPM.

The current waveforms I_D and I_L are shown in Figure 3.2. The periodic nature of I_D can be viewed as being modulated by circuit structure. As stated in Chapter 2, the freewheeling diode conducts during the non-conducting phase of the switch. Manipulating the control switch conduction interval can be used to alter the position

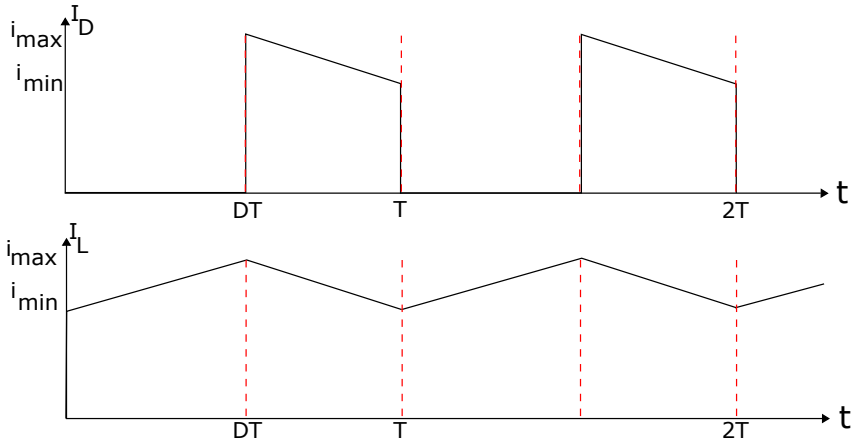

Figure 3.2: Current waveform of freewheeling diode in buck converter.

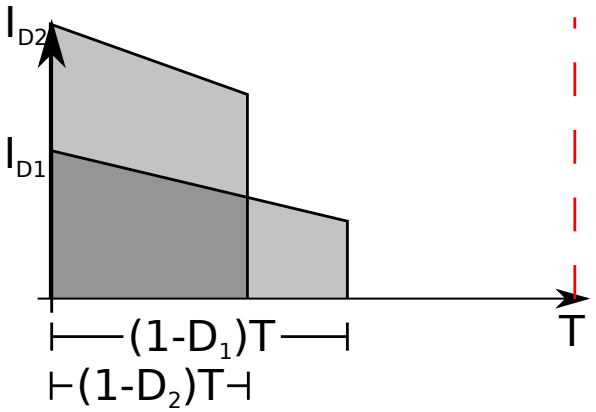

Figure 3.3: Diagram illustrating relationship of duty cycle and amplitude.

of I_D in T.

To enable dimming for LEFD converters, duty cycle, D, can be set to a lower value. This will yield lower V_o and I_o. Figure 3.3 demonstrates how dimming changes LEFD pulse width and amplitude. Duty cycle, D_1, is smaller compared to D_2 resulting in a greater LEFD pulse width. This duty cycle also dictates the amplitude of I_D as shown by comparing I_{D1} to I_{D2} in Figure 3.3. The change in amplitude is due to I_D being the same as the current through the inductor, I_L. Once a desired dimming level is set,

duty cycle should be kept constant to maintain a desired brightness. This will also maintain a constant state for receiving the signals from LEFD(s). PPM and OPPM as discussed in Section 2.3.2 work well to modulate LEFDs because information can be sent for any combination of duty cycle and amplitude.

3.2 Simulation

3.2.1 Simulation Setup

The parameters used for simulation of the buck converter are found in Table 3.2.1. These parameters were chosen considering the IEEE 802.3at standard for PoE [67] and components used for prototypes. The required value for the inductor was calculated based upon equation (2.11) and equivalent resistance of the output string of illumination LEDs. This was determined through estimation of LED turn on voltage and slope that matched operating currents closely as shown in Appendix B. The minimum inductor size is not used as it simply maintains CCM for a given duty cycle and switching frequency. The inductor was over-sized to accommodate a large range of testing duty cycles and load conditions. The switching frequency of 400 kHz was based upon the bandwidth of the inexpensive switch selected for this work. It should be noted that higher bandwidth switches capable of current requirements will allow for higher communication rates.

A combination of MATLAB [71] and LTSpice [72] were used to model and simulate the base case and LEFD converters to determine electrical efficiency and efficacy. Modulation of the LEFD converter was accomplished by generating a piecewise linear (PWL) file for use in LTspice. A PWL file allows for a waveform to be constructed

Table 3.1: Buck Simulation Parameters

V_s	48 V
f_{sw}	400 kHz
Max. Load Current, I_L	300 mA
Switch	IRF7343P [68]
Inductor	2 mH
Illumination LEDs	Lumileds 3535L [69]
Freewheeling Diode	RB558VYM150 [70] (base case) Lumileds 3535L [69] (LEFD)

from a series of line segments defined by endpoints [73]. These files of various duty cycle and OPPM order consisted of random data converted into switch control signals by MATLAB following rules defined in Section 2.3.2.

The I-V characteristic parameters for the Lumileds 3535L were extracted from datasheet plots and input as custom components to LTSpice (See Appendix B). The definition of electrical efficiency defined in (1.1) was used to compare LEFD converter efficiency to the base case buck converter. LTspice values of V_s, I_s, V_o, and I_o were used to determine output and input power defined by,

$$P_{OUT} = \frac{1}{k^*T}\int_0^{k^*T} V_o(t)I_o(t)dt, \quad P_{IN} = \frac{1}{k^*T}\int_0^{k^*T} V_sI_s(t)dt \tag{3.3}$$

where k^* is the number of cycles the simulation was run for.

The definition of efficacy as defined in equation (1.3) is used to compare the LEFD converter to the base case buck converter. The equation for luminous flux for a given drive current,

$$\Phi_V(I)[lm] = -0.0002I^2 + 0.531I + 0.4035 \tag{3.4}$$

was found by digitizing the plot given in the datasheet for the Lumileds 3535L [69] and

using Microsoft Excel [74] to perform regression as shown in Appendix B. The best fit was found to be quadratic with an R^2 value of 1. After simulating circuit operation in LTspice, I_D and I_o were substituted into (3.4) to determine output luminous flux.

3.2.2 Simulation Results

Limitations of Simulation

Simulations do not fully represent the underlying physics of the systems being modeled. The losses that are not accounted for in the following simulations are: losses in inductors and capacitors due to parasitic resistances, inductor core and copper losses [75], and losses caused by parasitic elements from printed circuit board (PCB) layout. An example of the PCB layout for the experimental work in Section 3.3 is given in Appendix E and was generated using KiCAD [76]. As length of traces increase, parasitic resistances, and inductances become greater sources of loss. Multilayer PCBs have parasitic capacitances that also impact circuit operation. Modeling such parasitics is difficult and is only approximated in advanced software tools [77]. In addition to parasitics of components, simulation software does not model the transient characteristics of devices. This is potentially a large source of loss as communication LEDs used within simulation do not operate in steady state. Even with the use of advanced modeling software, it is difficult to estimate losses within a SMPS. Therefore, simulation results can be used to provide a general insight into the trends involved in the design of SMPSs, while experimental results are required in order to fully characterize how design choices affect the performance of a SMPS.

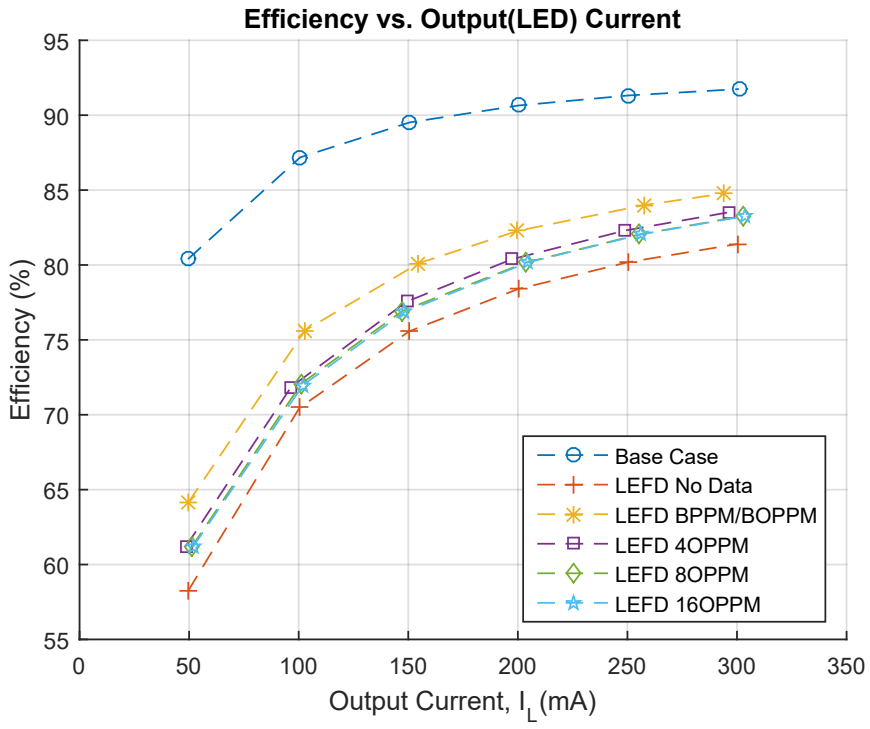

Figure 3.4: Simulated electrical efficiency of base case and LEFD topologies versus load current, I_L.

Electrical and Optical Efficiency

Figure 3.4 plots electrical efficiency, as defined by equation (1.1), of the base case topology and the LEFD converter when it is un-modulated and when it is carrying BPPM/BOPPM, 4-OPPM, 8-OPPM, and 16-OPPM. The LEFD topology has a slightly lower efficiency than the base case due to increased conduction loss in the LEFD and increased switching losses due to the larger forward drop in comparison to a conventional diode. This efficiency measure of the LEFD converter does not take into account the additional light output from the LEFD device itself. If the power used by the LEFD is considered to be useful output power, the efficiency curves of

the LEFD and base case topology will be significantly closer.

When modulated, the converter using an LEFD yields higher efficiency due to the use of PPM. In the cases where PPM or OPPM symbols are at either extreme of the period, two switching cycles are removed. On average, for BPPM/OPPM the amount of switching transitions is reduced by a half. Switching losses discussed in Section 2.2.3 are therefore reduced resulting in higher efficiency. As higher order PPM is used, the likelihood of removing switching transitions is reduced resulting in lower efficiency.

Figure 3.5 plots the simulated efficacy as defined by equation (1.3) for base case and LEFD topologies. At low I_o the efficacy of the base case is not accurately simulated due to the difficulty in modeling converter losses adequately. While the efficacy of an LED alone will increase for lower Luminous Flux values, converter losses are expected to dominate in this regime.

It can also be seen in Figure 3.5 that the efficacy of the base case and LEFD design are approximately the same for high values of luminous flux. As the luminaire is dimmed, the efficacy suffers. This is due to the duty cycle being increased in order achieve great I_o. By increasing I_o, I_D is increased as well, resulting in greater conduction loss from LEFDs. It is clear that the amount of luminous flux provided by LEFDs may not be suffucient to overcome conduction losses.

As the LEFD design is modulated, efficacy is increased as shown in 3.5. The efficacy increases for the same reasoning as the improvement in efficiency. For high duty cycles where the converter is most efficient, efficacy for converters using a LEFD will be higher than that of the base case. This is attributed to the light contribution of the LEFD. Furthermore, the overall achievable brightness is higher for a converter

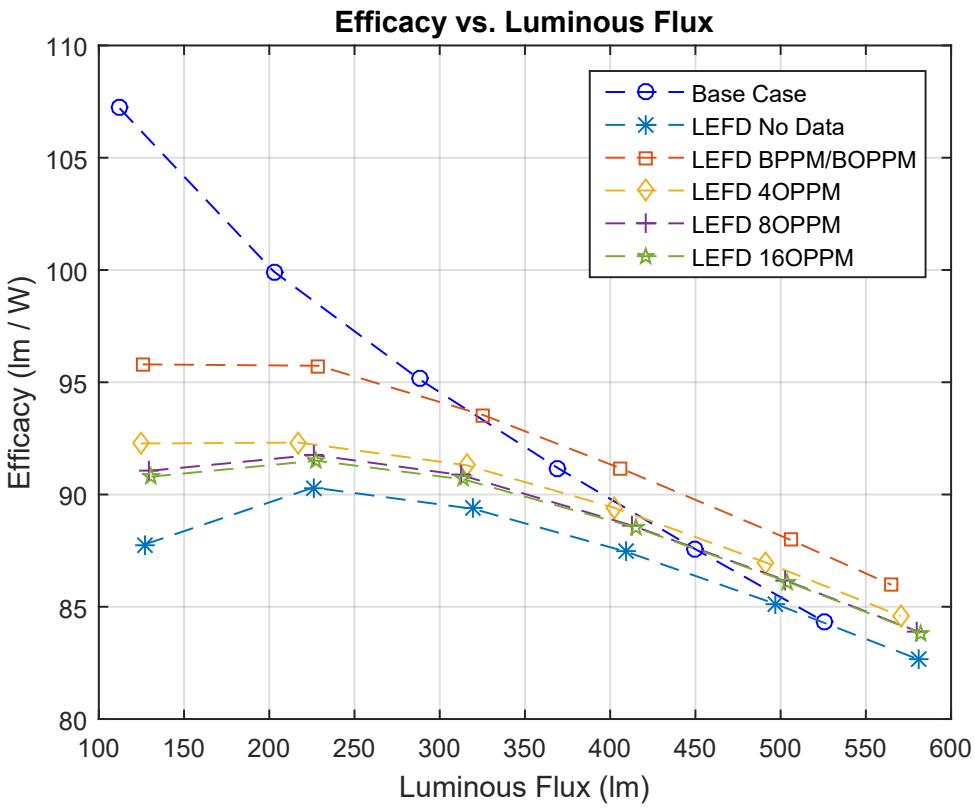

Figure 3.5: Simulated efficiency versus luminous flux of base case and LEFD designs: unmodulated, BPPM, 4-PPM, 8-PPM, and 16-PPM.

using an LEFD. If a given maximum brightness is targeted, a converter using a LEFD can achieve the same brightness as the base case using less drive current. From this observation, a lower power converter can be designed with the light contribution of the LEFD in mind.

The use of PPM increases both efficiency and efficacy from the non-modulated case of the LEFD design. While efficiency is increased, output current ripple is also increased for sets of periods that ignore switching transitions. If ripple current must be reduced, a higher switching frequency, larger value inductor, or a larger output capacitor may be used.

Simulations demonstrate that despite reduced efficiency caused by higher forward voltage of LEFD(s), efficacy may be increased as LEFD(s) contribute to luminous flux of the light. These results are verified by the prototype in the following Section.

3.3 Experiment

3.3.1 Experimental Setup and Parameters

The parameters and components used for the experimental setup are tabulated in Table 3.3.1. Component values were based on similar commercial designs used in practice for indoor lighting [80] and match those of simulation. The LEDs used were white Philips Lumiled 3535L [69]. Although these devices are not intended to be operated in reverse bias, our testing of 20 LEDs illustrated a reverse breakdown of approximately 40V to 45V (well above the given value on the data sheet and noted in [49]). Due to reverse breakdown voltage, source voltage used for experimental measurements was limited to 40V.

Table 3.2: Buck Experimental Parameters

V_s	40 V
f_{sw}	400 kHz
Max. Load Current, I_L	300 mA
Switch	IRLML0060TRPBF [78]
Inductor	2 mH
Illumination LEDs	Lumiled 3535L [69]
Freewheeling Diode	1N4148 [79] (base case) Lumiled 3535L [69] (LEFD)

Figure 3.6 displays a photograph of the prototype used to characterize and contrast performance of the proposed design with simulation. Communicating and illumination LEDs are identified within the LED array. The modulated signal is summed spatially with the illumination LEDs causing an easily removed DC shift via high pass filter when received. Experimental buck converter results were completed using a single LEFD and initially no capacitor was used across the load. Future tests used an output capacitor to reduce output ripple current and improve transmitted waveforms.

The experimental luminaire was modulated to test communications in addition to its effects on efficiency and efficacy. Random sets of data were created comprising of a single bit (BPPM/BOPPM), two bits (4OPPM), and three bits (8PPM). BPPM was used for the case of dimmed communications tests that resulted in duty cycles of less than 50% in the binary case and BOPPM was used for duty cycles of greater than 50%. For further tests of higher order, OPPM was used as duty cycle necessitated it. The data was saved into ROM of the DE0-Nano FPGA [81] and converted into an appropriate control signal following the rules outlined in Section 2.3.2 and described in Appendix C. This signal was applied to the switch of the buck converter

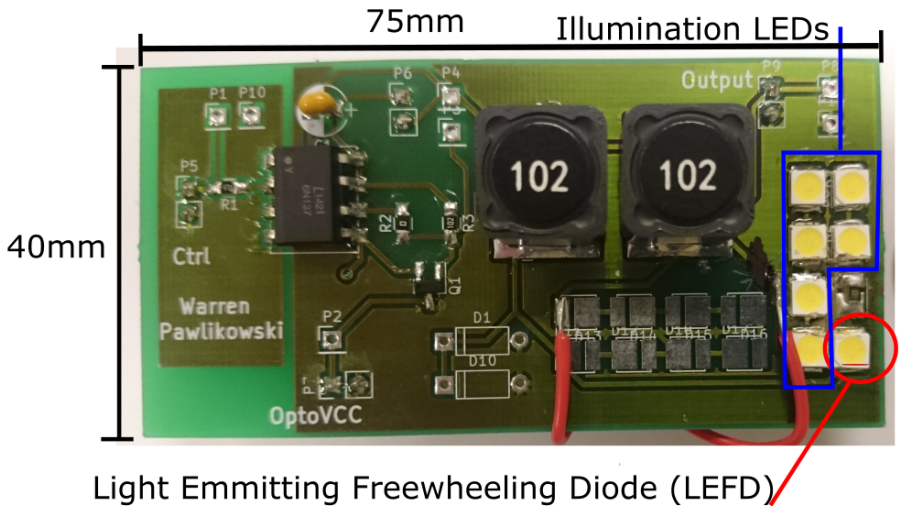

Figure 3.6: Experimental LEFD buck converter design

through a 6N137 opto-isolator [82] to separate and protect digital control circuitry from comparatively high voltages and currents in the SMPS. The signal output from the opto-isolator was probed via an Agilent Infinium 54853A oscilloscope [83] to capture the sent sequence prior to being affected by the transmitter, channel, or receiver.

To test communications, light from the LEFD was combined with illumination LEDs via the THORLABS DG20-1500 diffuser [84] and captured by the THORLABS PDA36A photodiode [85] with adjustable gain initially set to 10dB as shown in Figure 3.7. The luminaire was 110 cm from the photodiode along the optical axis. After waveforms were collected from the oscilloscope, they were saved and analyzed with MATLAB. Additionally, the signal persistance function within the oscilloscope was utilized to create eye diagrams for each modulation order.

The minimum distance, of increasing orders of OPPM was test using the LEFD

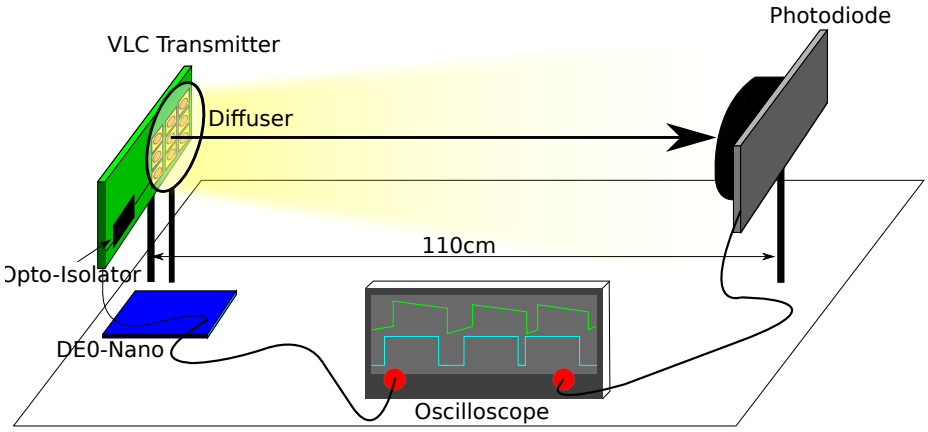

Figure 3.7: Diagram demonstrating the experimental setup to collect experimental communication results

converter. The nominal d_{min0} of BPPM at a I_o of 300 mA was used as the normalization factor to define $\bar{d}_{min}$ given by

$$\bar{d}_{min} = \frac{d_{min}}{d_{min0}}. \tag{3.5}$$

This was done in order to eliminate the dependence of d_{min} on common factors affecting the amplitude, A, of the received signal since d_{min} should be measured at the receiver. By setting duty cycle and making illuminance measurements at 110cm from the Extech Instruments Model HD400 lux meter [86], experimental values of $\bar{d}_{min}$ were found. The amplitude of pulses, A, determined by the illuminance value and duty cycle were substituted into equations (2.30) and (2.32) for PPM and OPPM respectively.

To monitor P_{IN}, voltage and current from the DC supply was monitored and verified with a multimeter. Using a multimeter, P_{OUT} was monitored between illumination LEDs and ground for current and by monitoring overall voltage drop of

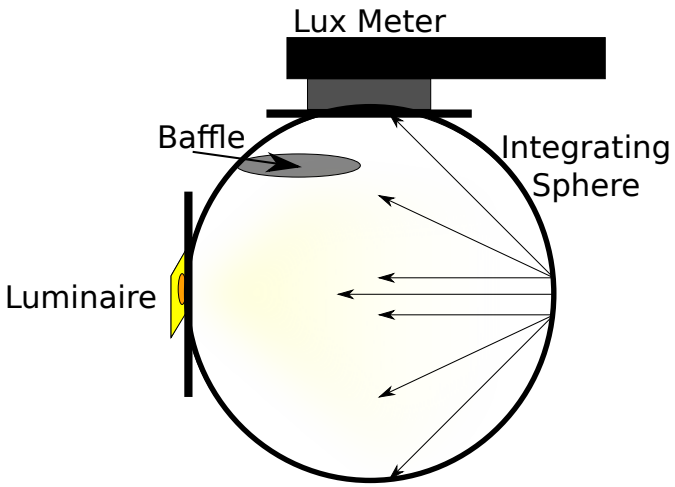

Figure 3.8: Diagram demonstrating the integrating sphere and lux meter setup used to measure light output of designed luminaires.

all illumination diodes. Converter efficiency was determined via P_{IN} and P_{OUT} and equation (1.1).

Experimental measurement of efficacy was accomplished by using an integrating sphere as shown in Figure 3.8. Size limitations did not allow for the luminaire to be placed inside and the prototype was instead coupled with an opening of the sphere. This is a possible source of error as some light may not be collected by the integrating sphere. In order to quantify the optical output, the illuminance was measured using the Extech Instruments Model HD400 lux meter [86] and normalized. Through the combination of the integrating sphere and the fixed area of the lux meter detector, a normalized measure of optical efficacy can be made. This is because when normalizing, the area of the detector is eliminated. The normalized optical efficacy used to contrast with simulated efficacy curves is defined as

$$\eta'_O = \frac{E_V/P_{in}}{E_V/P_{in}|_{\text{BCmax}}}. \tag{3.6}$$

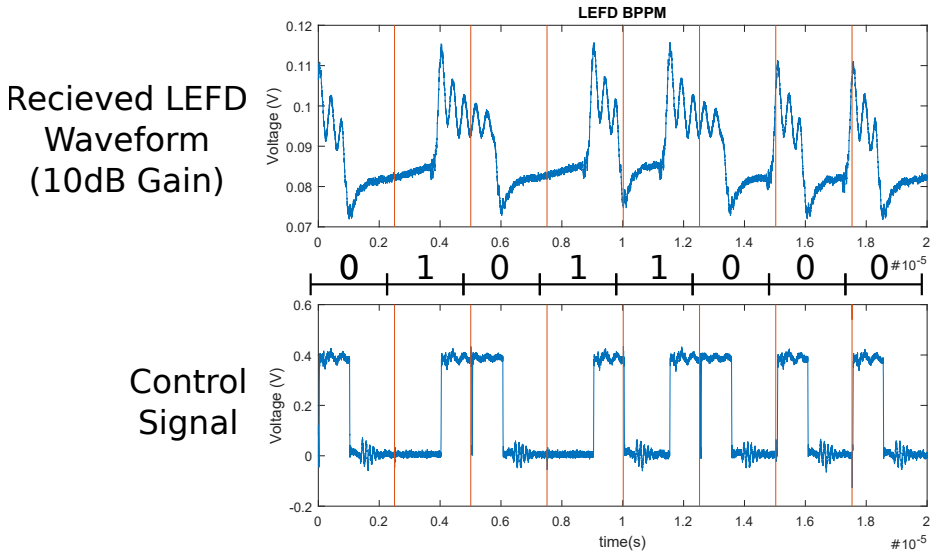

Figure 3.9: Sample Received and sent BPPM LEFD waveforms

$E_V/P_{in}|_{\text{BCmax}}$ is the maximum value of illuminance measured for the base case and the quantity used to normalize optical efficacy.

3.3.2 Experimental Results

Experimental Communications Results

Initially, transmitted waveforms were visually inspected to verify that the control circuit generated appropriate waveforms that were sent and received. The received signals for the buck converter were heavily distorted by a resonant frequency above that of f_{sw} as shown by sample waveforms in Figure 3.9. This was determined to be caused by parasitic capacitance present in the PCB layout shown in Appendix E. To more clearly identify waveforms, photodiode gain was increased to 20dB, and the waveforms were low-pass filtered. Figure 3.9 contrasts received and sent signals

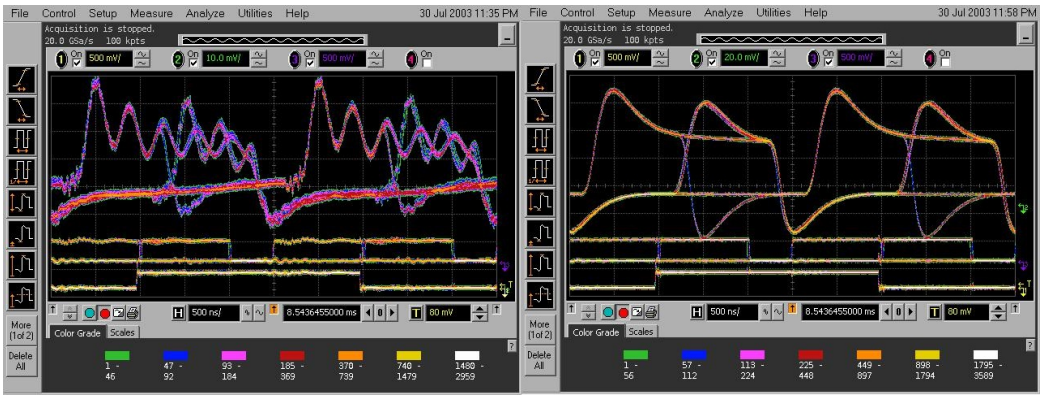

Figure 3.10: LEFD BPPM Eye Diagram for low gain, high bandwidth and higher gain, low-pass filtered

for BPPM. Sample received and sent signals for 4OPPM and 8OPPM may be found in Appendix D. These sample received signals demonstrate experimentally that data may be discerned through visual inspection. Received waveforms may lag in time due to the presence of the inductor in the buck converter. The amount of lag is based upon the size of the inductor used.

Eye diagrams are presented with both a lower gain (10dB) with higher bandwidth and a higher gain (20dB) with lower bandwidth. Figure 3.10 presents an eye diagram for BPPM. Eye diagrams for 4OPPM and 8OPPM may be found within Appendix D. The lower gain and resonant frequency present distorts the eye diagram and obstructs the ability to evaluate the quality. The filtered, higher gain eye diagrams however very clearly depicts an open eye diagram with clear transitions between symbols. As the order of PPM is increased and lighting is dimmed through a reduction in current, eye diagrams deteriorate and symbol transitions become more difficult to differentiate. This is due to increased overlap of OPPM symbols. It is expected that more errors would be present when demodulating for dimmed luminaires as overlap would increase and amplitude would decrease, resulting in an eye diagram that is

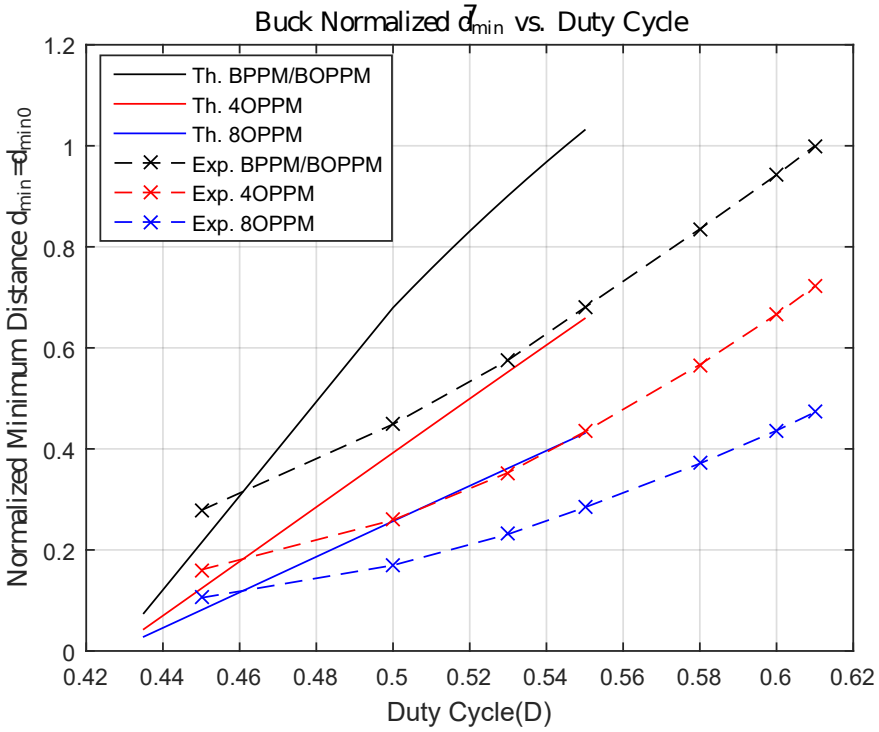

Figure 3.11: Normalized d_{min} for increasing orders of modulation.

closing and overlapping with other signals more.

Figure 3.11 plots $\bar{d}_{min}$, the normalized minimum distance for both theoretical and measured results. Increasing orders of OPPM were plotted to demonstrate the difference that increases of modulation order have on d_{min} both theoretically and in practice. Lower values of the measured $\bar{d}_{min}$ are attributed to under-estimating drive current for a give D. The LEFD converter required larger D than in theory to reach nominal operating conditions. Limitations of diode modeling and simplifications of converter operation are responsible for $\bar{d}_{min}$ being lower than expected. Additionally, the amount of resonant frequency distortion in the experiment also affected the curvature of the $\bar{d}_{min}$ trend. In the theoretical calculations, pulses are assumed to be

Table 3.3: BER for Increasing Modulation Order

Duty Cycle	60	55	50	45	40
BPPM/BOPPM	No Errors	No Errors	No Errors	No Errors	No Errors
4-OPPM	No Errors	No Errors	No Errors	0.0588	0.1459

square waves while the measured values have significant ringing. The ringing within the LEFD converter prototype is likely the result of parasitic capacitance due to the ground plane in the PCB layout shown in Appendix E.

Figure 3.11 demonstrates that duty cycle changes result in significant differences in d_{min}, and by extension, the ability to demodulate signals reliably is also affected. As duty cycle is increased, LEFDs are driven with higher current and overlap less with adjacent signals. Conversely, lowering duty cycle results in a decrease of drive current and an increase of pulse overlap.

Data sets of 10^5 symbols were created and sent to experimentally determine BER for BPPM/BOPPM, and 4OPPM as tabulated by table 3.3.2. BER tests of greater than 10^5 symbols were not able to be recorded due to oscilloscope capture limitations. Due to the age of the oscilloscope and the amount of time taken to write waveforms to memory, the amount of data that could be saved and analyzed within a reasonable amount of time was limited.

For BPPM, throughout dimming as duty cycles were changed no errors were detected. As 4OPPM was tested with larger duty cycles to allow for dimming, data could no longer be recovered with high reliability. This was demonstrated for a heavily dimmed luminaire and for most operating conditions, no errors were detected. This results in a possible data rate of 800 kbps when using the 400 kHz f_{sw} and 4OPPM.

The failure to demodulate 4OPPM without errors at higher duty cycles and inability to demodulate 8OPPM is attributed to the low resolution of shifts available from the FPGA as well as the reduction of d_{min} as demonstrated previously. As shown in Appendix C, the FPGA had 100 intervals in order to define duty cycle and shift. This meant that for 8PPM and a duty cycle of 60%, adjacent signals were only five intervals apart. This combined with timing jitter, where the the clock is not constant over time results in a difficult set of signals to recover reliably. Future tests with higher resolution of shifts from the FPGA and a more stable clock should allow for higher orders of PPM to be demodulated reliably.

Electrical Efficiency and Normalized Efficacy

Figure 3.12 plots the measured efficiency of the base case and the LEFD converter topology with and without PPM modulation. Experimental results mirror simulations with a decrease in efficiency over about 10% when using a LEFD. The resulting efficiencies of experimental work are likely lower due to the limitations of simulation as described in Section 3.2.2. Although 10% is a significant difference in efficiency between simulation and experiment, this amounts to a difference of only 1.3 W. The LEFD designs simulated and tested had a peak input power of 13 W which is relatively low power. Combinations of small sources of power loss account for a large percentage of total power, resulting in the discrepancy between simulation and experiment. The impact of modulation on efficiency is not as strong in our measurements as in simulations, however, noticeable changes are still apparent.

Figure 3.13 presents a plot of the normalized optical efficiency, given by equation (3.6), versus the measured illuminance. The output luminous flux of a luminaire is

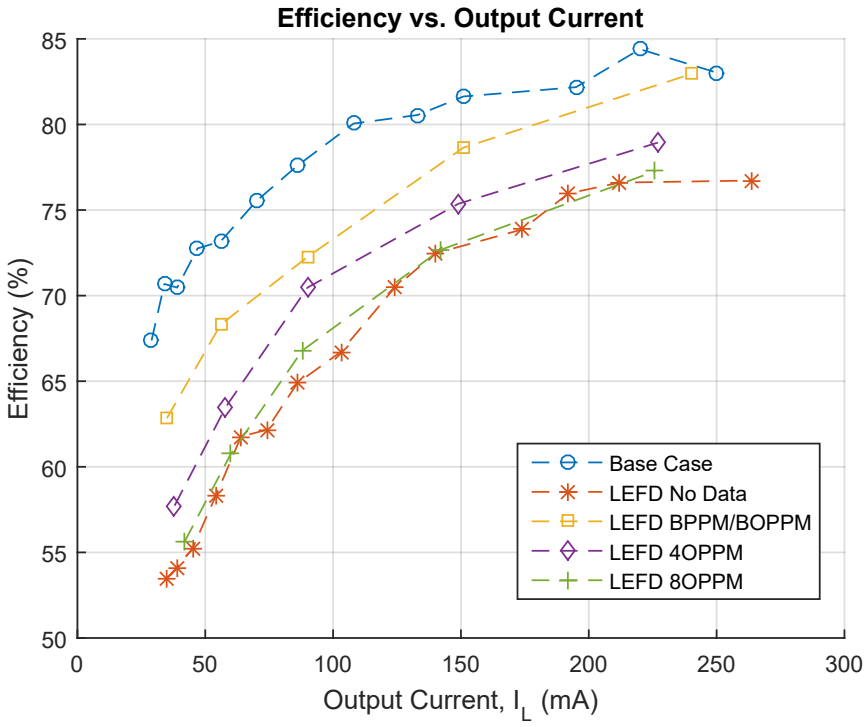

Figure 3.12: Experimentally measured efficiency of the Base Case, LEFD design non-modulated, LEFD design modulated by BPPM, and LEFD design modulated by 4-PPM

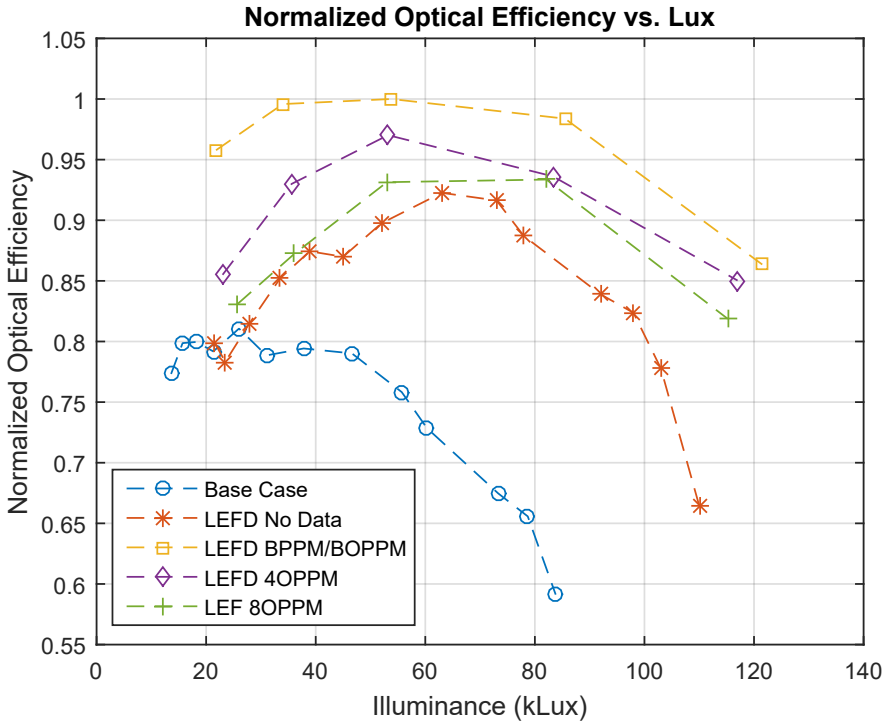

Figure 3.13: Experimentally measured normalized optical power of the Base Case, LEFD design non-modulated, LEFD design modulated by BPPM, and LEFD design modulated by 4-PPM

proportional to the drive current from a power converter. As lighting varies from low lighting levels to higher levels, the power converter losses that are dominant change. Power converters operating at low output current are dominated by switching losses as described in Section 2.2.3. While operating in a high output current regime, conduction losses are increased and become significant than switching losses. Under a specific load current, switching and conduction losses are balanced resulting in a peak efficacy.

The optical efficiency for BPPM-modulated LEFD converter is nearly the same as the base case for low illuminance while at high illuminance the LEFD topologies exceeds the base case. For higher illuminance values, using an LEFD with other modulation schemes also increases optical efficiency as compared to the base case. This is a major improvement over previous modulation techniques which result in the same or decreased optical efficiency. The additional light output of the LEFD yields higher optical efficiency because the power used in the freewheeling portion of the converter is useful power and is not lost. As is the case for the simulated efficacy, the measured optical efficiency decays at high duty cycle due to the LEFD conducting for a shorter time, thereby contributing less light compared to power used. As shown in simulations, a greater amount of light is output when using a LEFD in the converter. As previously mentioned, this can be considered when designing a luminary as LEDs may be driven with less current to achieve the same level of brightness. The affect of modulation on the measured optical efficiency is similar to that of electrical efficiency. As the order of PPM is increased, optical efficiency decreases with BPPM yielding the highest optical efficiency.

3.4 Conclusions

In this chapter, a buck converter using a LEFD was proposed. Design considerations and advantages of LEFD(s) were presented as well as a method of supporting modulation at the rate of the converter switching frequency. The outlined concept was extended to both simulation and an experimental prototype.

The experimental prototype was used to verify quality of transmitted waveforms and communication performance of a LEFD SMPS. The highest order modulation scheme reliably recovered was 4OPPM at a switching frequency of 400kHz. This setup yielded a data rate of 800 kbps. Through increases in switching frequency by using a better switch and increased modulation order through use of a better signal generator, data rates of tens of Mbps can be achieved.

Finally, electrical efficiency and efficacy of a standard buck converter used as a luminaire was contrasted with the proposed LEFD buck converter design. Both simulation and experimental results demonstrated an increase in efficacy despite larger losses from LEFD(s) over a conventional freewheeling diode. Differences between simulation and experimental results were due to losses that could not easily be modeled. Due to the low power SMPS implemented, losses not accounted for comprised of a significant amount of total input power and resulted in an approximate 10% difference of efficiency between simulation and experiment. Higher luminous flux of the LEFD converter was verified and can be leveraged in future work to design luminaires of lower input power that produce the same lumen output.

Chapter 4

Light Emitting Blocking Diodes and Boost Converter Integration

In this chapter, boost converters using LEBDs to facilitate communications are discussed. As in the previous chapter, the concept, simulation, and experimental results are discussed and analyzed. The boost converter topology, similar to the buck was chosen for its simplicity as a non-isolated SMPS capable of constant current. The application of this topology differs from the buck converter, however many design philosophies and results are shared. The effects on efficiency, efficacy, and potential data rates are presented and discussed. The purpose of this chapter is to demonstrate a second SMPS topology that uses similar design practice to LEFD converters. Through verification of the concepts presented in this Chapter and Chapter 3 it is demonstrated that this technology may be used in a wide variety of circuit topologies.

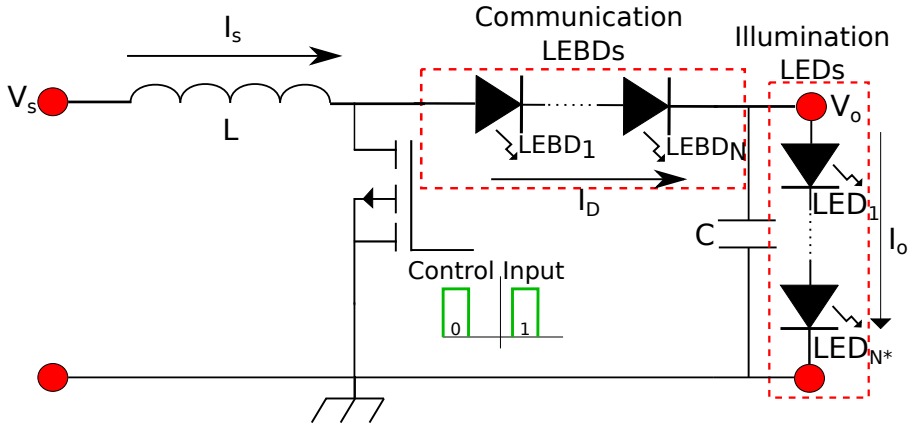

Figure 4.1: A boost converter with proposed light-emitting blocking diode (LEBD).

4.1 Concept

A simple diagram of a proposed boost converter with a LEBD is provided in Figure 4.1. Blocking diodes are a fundamental component in boost converters that are a source of power loss within conventional designs. The use of diodes with low forward bias is a standard practice to avoid large power dissipation by this component. [87] As in Chapter 3 where the freewheeling diode of a buck converter was replaced with an LEFD, the blocking diode in a boost converter may be replaced with a LED termed a *light-emitting blocking diode* (LEBD). Blocking diodes are very similar in operation to freewheeling diodes. The difference lies within their importance to circuit operation. They prevent a flow of current such as the discharging of a capacitor, while freewheeling diodes are present in order to facilitate current flow. As noted with LEFD(s) in Chapter 3, LEBD(s) are not limited to the visible spectrum. The use of LEBD(s) outside of the visible spectrum allow for invisible OWC links.

Chapter 3 separated communicating LEDs from illumination LEDs by exploiting buck converter structure. Boost converter structure also enables this, however,

instead of an inductor separating communication and illumination LEDs, the boost converter uses an output capicitor. The output capacitor present in a boost separates communications and illumination, allowing for illumination LEDs to maintain conduction without limiting the bandwidth of LEBDs. Without the presence of this capacitor, all LEDs would alternate between conducting and non-conducting states. This is due to the inductor being disconnected from all LEDs while it is charging. An advantage of a boost converter that uses LEBDs and a load which is also LEDs is that the number of communicating LEBDs and illumination LEDs can be divided simply by changing the placement of the output capacitor. The number of illumination LEDs determines the required output voltage. This also determines the reverse biasing of the LEBDs. By dividing the ratio of illumination LEDs to LEBDs appropriately, it is possible to overcome the problem of low reverse bias voltage of a LED. The resulting changes in efficiency and efficacy caused by differing numbers of LEBDs will be demonstrated later in this chapter.

Similar to LEFDs presented in Chapter 3, LEBDs can be modulated at full rate of the SMPS and increase overall efficacy. This is due to the power used by the blocking diode providing illumination in addition to the LEDs used within the output string. Dimming is supported in the same manner that it was previously through the use of PWM. It is assumed that CCM is maintained for boost converter designs using LEBD(s) and therefore, using equation (2.15), a minimum value for the inductor may be found. Using larger inductor values will produce lower ripple current and a greater range of duty cycles used for dimming that maintain CCM.

4.2 Electrical Operation and Design Considerations

As discussed in the Chapter 3, it is necessary to understand the effects of replacing a conventional diode with a LED. The consequences of different forward voltage, reverse voltage, and operating currents compared to conventional diodes should be assessed along with their impact on overall circuit operation.

Reverse biasing of LEFDs was a necessary property of LEFD converter operation discussed in Chapter 3. Similarly, boost converter operation relies on LEBD(s) being reverse biased, however, they are reverse biased by V_o instead of V_s. In the case of buck converters, V_s is the largest voltage present. V_o in boost converters is also the largest voltage present in the circuit. This means that both LEFDs and LEBDs must handle the largest potentials found in each topology in reverse bias.

The current waveform of LEBDs used within boost converters does not change significantly compared to LEFDs used within buck converters. Blocking diode current waveforms are still periodic and in the case of a boost converter are the compliment of a control switch. Duty cycle is fixed to control output current, and LEBD current is dependent upon duty cycle. Therefore, the method of sending information through LEBDs remains the same as used within buck converters. Duty cycle is kept constant and the position of the waveform is varied to implement PPM or OPPM.

The use of N LEBDs will affect output voltage control. The increased forward drop of LEBDs, referred to as V_f^{LEBD}, results in LEBDs designs having a different relationship of input voltage to output voltage as described by,

$$V_o = \frac{V_s - (1-D)NV_f^{LEBD}}{(1-D)}. \tag{4.1}$$

This equation is found by including the forward voltage of the LEBD and not assuming it to be negligible as done in Chapter 2. A derivation assuming a large output capacitor and CCM can be found in Appendix A.

A key difference between LEBDs and LEFDs is that I_D is not the same as I_o. The current through LEBD(s), I_D, is the same as inductor current, I_L. This is due to the output voltage being fixed by output capacitor, C, to maintain constant current for illumination LEDs. While the inductor is charging, LEBD(s) are not conducting and the output capacitor supplies current to illumination LEDs. During the discharge phase of the inductor, current is shared between illumination LEDs and the output capacitor in order for it to charge.

4.3 Simulation

4.3.1 Simulation Parameters

The parameters and components used in the simulation are tabulated in Table 4.3.1. Component values are comparable to commercial designs used for car headlamps [88] [89]. Through the use of LTspice and MATLAB, LEBD converters were simulated to verify electrical efficiency and optical efficacy. Methodologies for simulation were maintained from Chapter 3 when simulating LEFDs in buck converters. The LEBD converter used different LEDs for LEBDs due to increased current requirements. The LEDs used were the CREE XLamp XP-E2 [90]. A fit for the luminous flux from datasheet graphs was also completed with Microsoft Excel [74] as shown in Appendix

Table 4.1: Boost Simulation Parameters

V_s	12 V
f_{sw}	400 kHz
Max. Load Current, I_o	300 mA
Max. Inductor Current, I_L	600 mA
Switch	IRLML0060TRPBF [78]
Inductor	2 mH
Illumination LEDs	Lumiled 3535L [69]
Blocking Diode	1N4148 [79] (base case) CREE XLamp XP-E2 [90] (LEBD)

B. The resulting equation for the XLamp XP-E2 LEDs was,

$$\Phi_V(I)[lm] = -0.0001I^2 + 0.3451I + 5.1269 \tag{4.2}$$

with an R^2 value of 0.9998. This was used to find luminous flux resulting from I_D in simulation. Illumination LEDs still used equation (3.4) and I_o for their contribution to overall luminous flux.

4.3.2 Simulation Results

As discussed in Section 3.2.2, limitations of loss estimation make simulation of SMPS difficult. To understand performance fully, simulations should be combined with experimental measurements.

Electrical and Optical Efficiency

LEBD converters using output capacitors have higher peak current through I_D when compared with I_o shown in Figure 4.1. As discussed in Section 4.1, this is caused

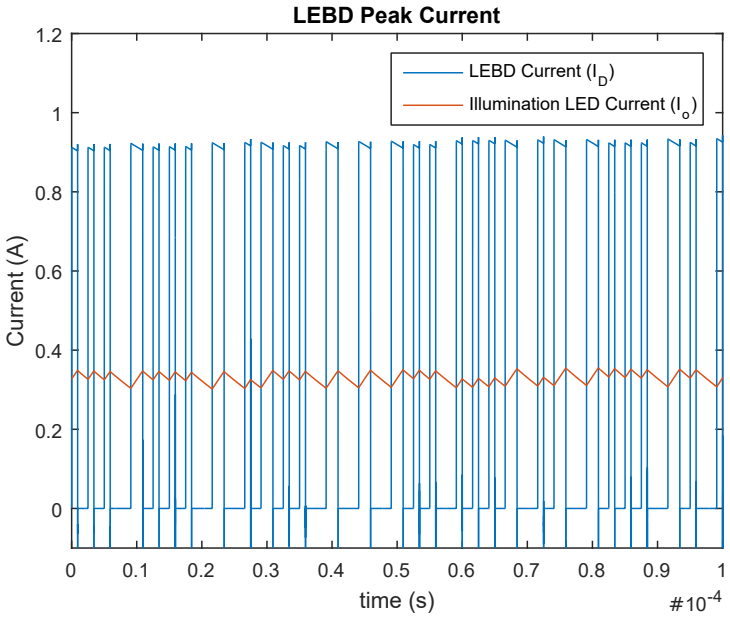

Figure 4.2: Simulated peak current of LEBD versus illumination LEDs.

by the output capacitor, C, maintaining constant current for illumination LEDs. The current through LEBDs is the same as the inductor current when the control switch is off. The current during this phase of converter operation is split between illumination LEDs and charging of the output capacitor. Therefore, the current through illumination LEDs is a fraction of the LEBD current. Initially, placing LEBDs in parallel was considered. However, as LEBDs heat up due to conduction, a positive feedback loop will occur [8, p. 67-69]. Since I_D is temperature dependent as noted in equation (2.4), each diode would contribute to the temperature of the other diode and increase their currents. Impurities within LEDs cause slight differences in I-V characteristics even for LEDs of the same model and manufacturer. The positive feedback loop would continue until an equilibrium was met, resulting in un-equal current splitting of LEBDs [8, p. 67-69]. This would lead to shorter device lifetimes

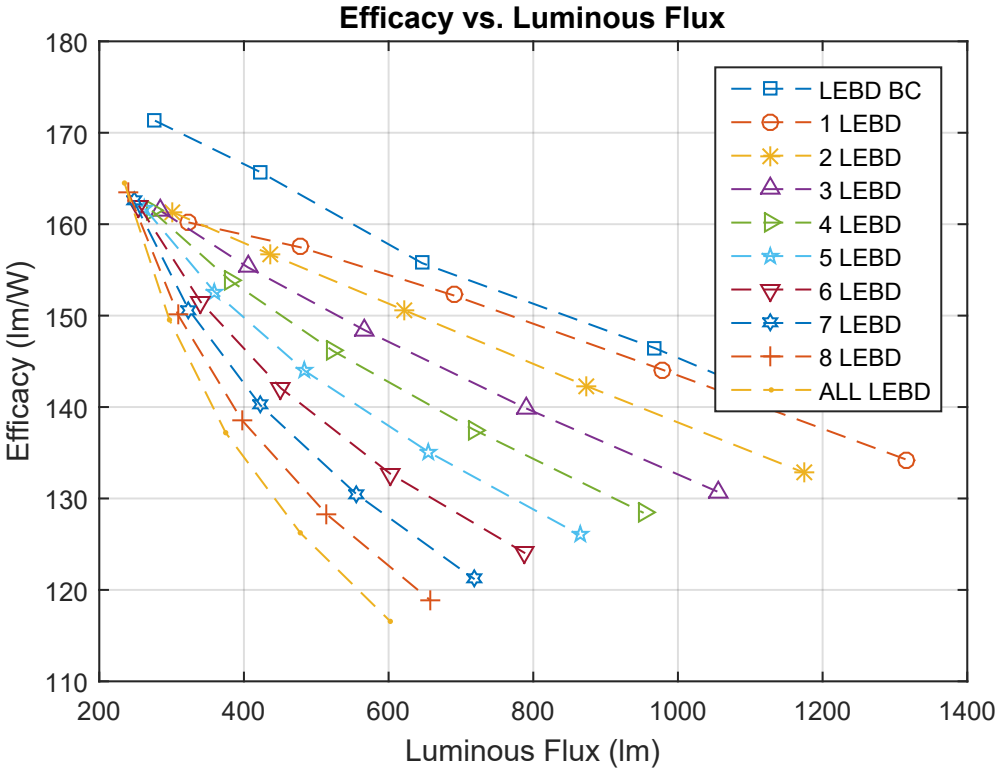

Figure 4.3: Simulated efficay versus luminous flux of base case and LEBD designs: base case, 1 LEBD, 2 LEBDs, 3 LEBDs, 4 LEBDs, 5 LEBDs, 6 LEBDs, 7 LEBDs, 8 LEBDs, 9 LEBDs.

and inconsistent operation of transmitters.

Figure 4.3 plots the efficacy of the base case topology versus the LEBD converter using increasing amounts of LEBDs. A total of nine diodes are used in each converter. The base case uses eight LEDs and a single conventional diode. The boost converter using LEBDs is simulated from a single LEBD to the case of completely removing the output capacitor. The last case results in a converter where all diodes are modulated and used to facilitate VLC. As the number of LEBDs increases, efficacy of the

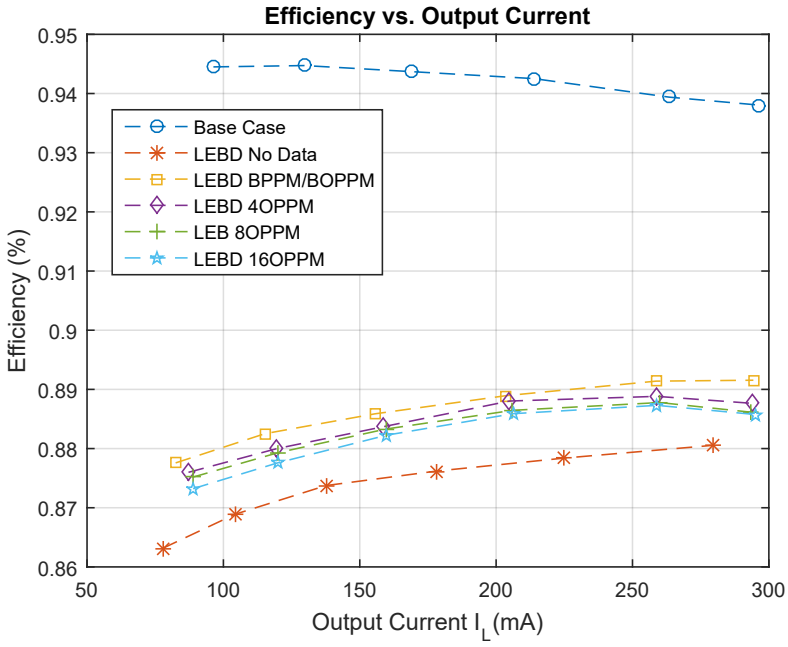

Figure 4.4: Simulated efficiency versus luminous flux of base case and LEBD designs: unmodulated, BPPM/BOPPM, 4OPPM, 8OPPM, and 16OPPM.

converter is decreased. There are two reasons for this decrease in efficacy. The primary reason is an increase in power lost to reverse recovery of the LEDs as described in Section 2.12 of Chapter 2. The second is due to LEDs with lower efficacy being used as LEBDs in order to handle the large peak current depicted by 4.2. For the remainder of this Chapter, LEBD converters will be evaluated using a single LEBD.

Simulated efficiency of the LEBD converter compared to the base case can be found in Figure 4.4. As found in the case of the buck converter simulations, efficiency was reduced by approximately 7% when compared to the base case converter. This is expected due to the large forward drop of the LEBD.

Figure 4.5 demonstrates simulated efficacy of the LEBD converter compared to that of the base case boost converter. Efficacy for the LEBD converter is increased

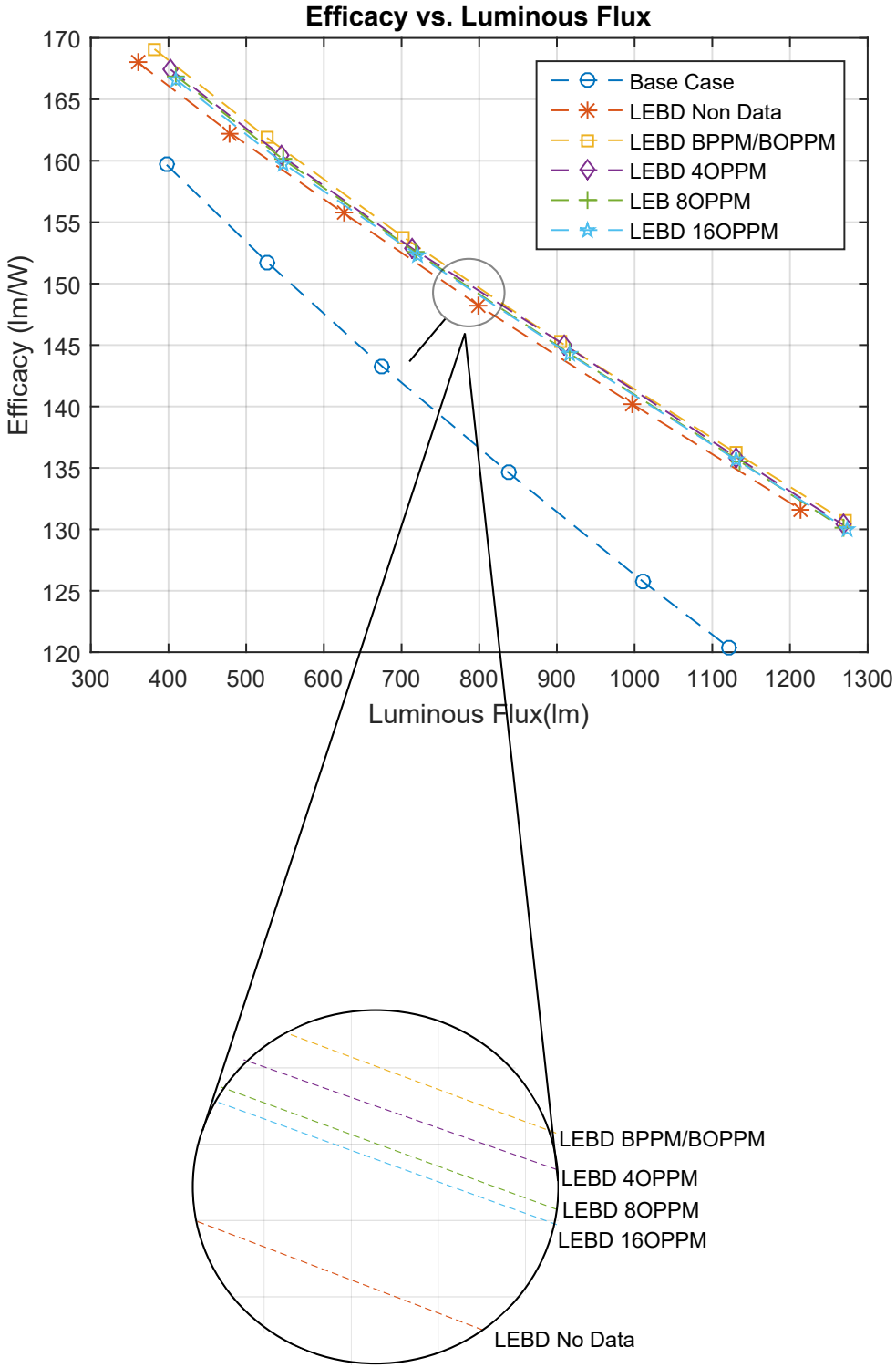

Figure 4.5: Simulated efficacy versus luminous flux of base case and LEBD designs: unmodulated, BPPM, 4-PPM, 8-PPM, and 16-PPM.

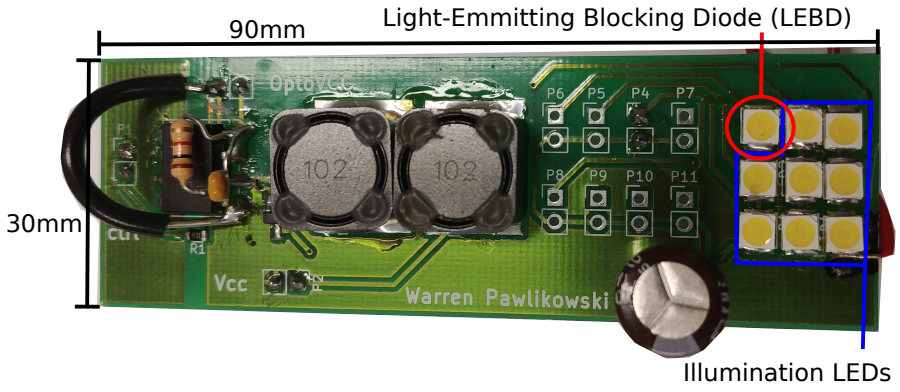

Figure 4.6: Experimental LEBD boost converter design.

over the base case, as expected from results with LEFDs. As moduation order increased from BOPPM to 8OPPM, efficiency and efficacy decreased as expected. Similar to Chapter 3 and LEFD converters, the elimination of a switching transition for some symbol transitions results in less switching power losses. This effect is much less pronounced in LEBD converters and is due to higher the higher currents present that result in the dominant source of loss being attributed to conduction losses.

4.4 Experiment

4.4.1 Experimental Setup and Parameters

Experimental parameters match the simulation setup as found in Table 4.3.1. The number of LEBDs was fixed to one as simulations indicated this to yield the highest efficacy. An image of the prototype boost VLC converter is given in Figure 4.6.

The LEDs used were white Philips Lumiled 3535L [69] and the CREE XLamp XP-E2 [90]. The CREE LEDs were tested for maximum reverse breakdown and were

verified to handle up to approximately 40V, similar to that of the Philips LEDs. The CREE LEDs were used as they are rated for a larger forward current of 1 A.

Testing methods for communications performance were not changed from Section 3.3.1 for the evaluation of LEBD converters. The testing setup matched the setup depicted by Figure 3.7 and the FPGA code was used with different duty cycles being set. Sample waveforms, eye diagrams, minimum distance, and some BER results are presented.

Experimental measurements of efficiency and efficacy were obtained via the same methodology as used for the buck converter defined in Section 3.3.1. The use of an integrating sphere as shown in Figure 3.8 was used to measure normalized optical efficacy as defined in equation (3.6). Efficiency and efficacy were both analyzed for the non-modulated case and the use of BOPPM, 4OPPM, and 8OPPM.

4.4.2 Experimental Results

Experimental Communications Results

As in Chapter 3, initial testing of communications was completed via a visual inspection of sent and received waveforms as shown by Figure 4.7. Design of the boost converter was completed after tests of the buck converter and LEFDs. The resonant frequency from the PCB was removed and waveforms are much more clear. Additionally, due to higher drive current, waveforms are received at greater amplitudes.

Figure 4.8 presents BPPM eye diagrams for a boost converter using an LEBD and a duty cycle of 50%. It can be seen that the amount of noise present is small relative to the amplitude of the signal. The eye diagram testing BPPM is not impacted by jitter and timing issues. Additional eye diagrams are displayed in Appendix D,

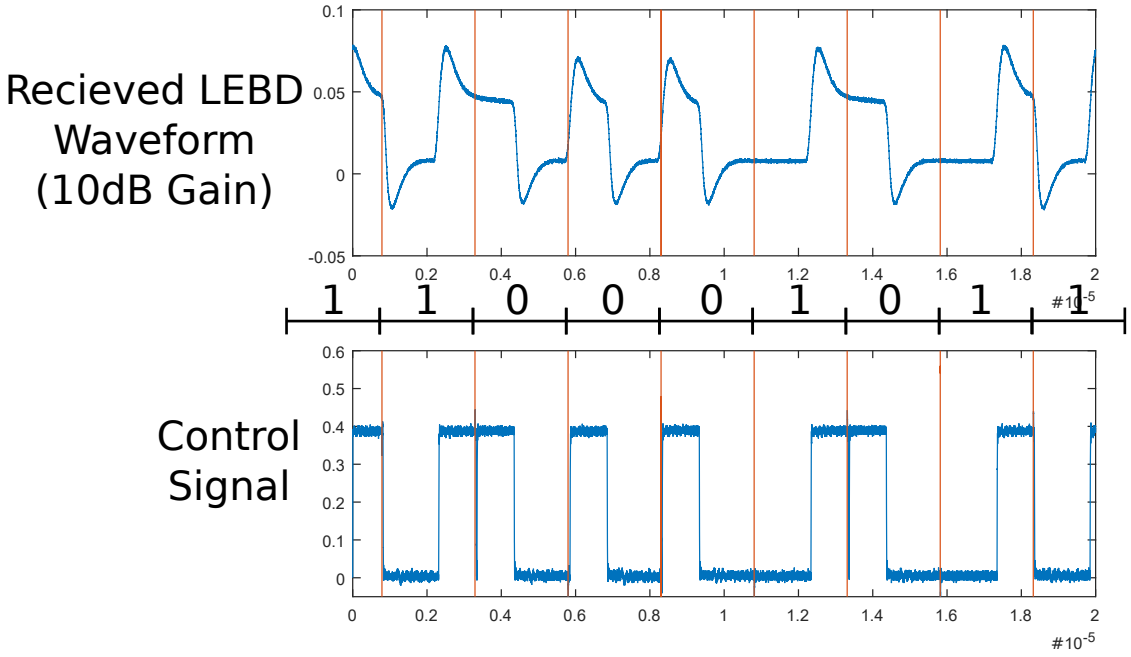

Figure 4.7: Sample Received and sent BPPM LEBD waveforms

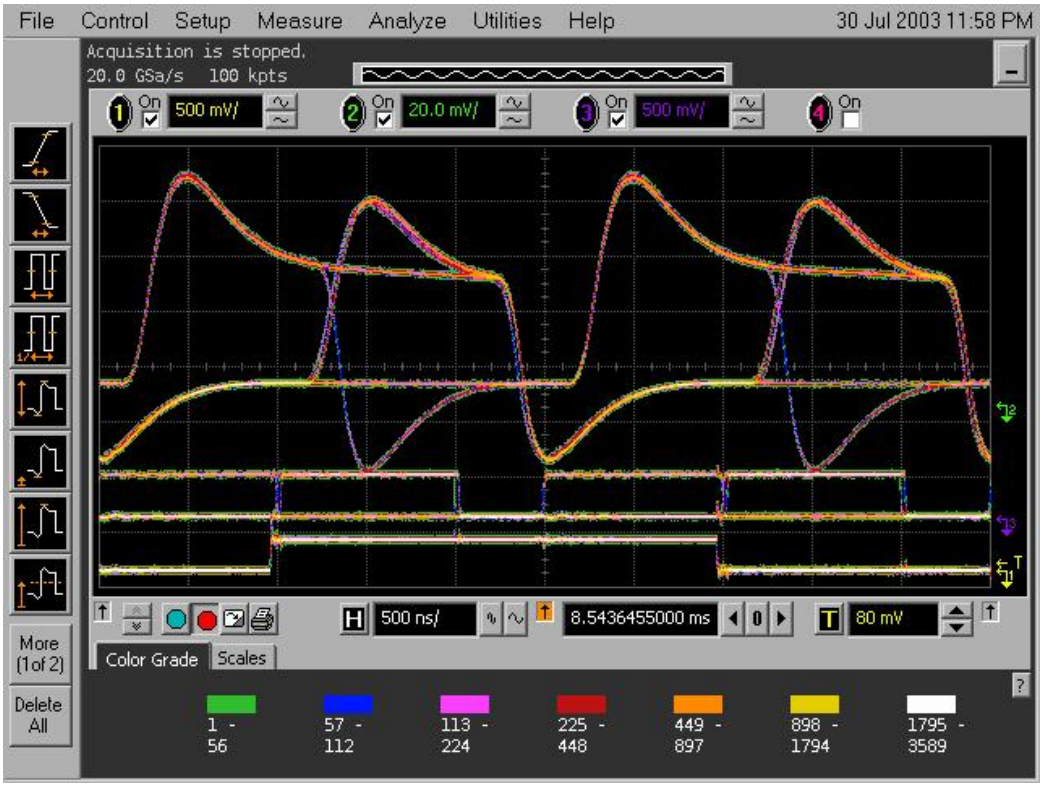

Figure 4.8: LEBD BPPM Eye Diagram

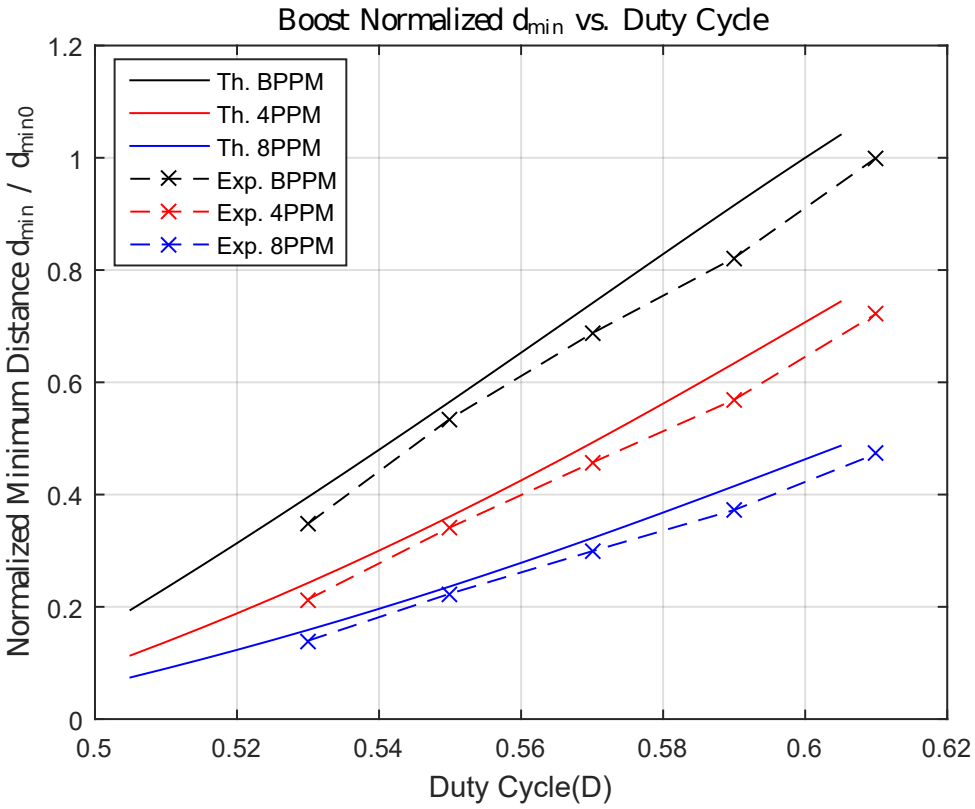

Figure 4.9: Normalized $\bar{d}_{min}$ for increasing orders of modulation.

demonstrating 4OPPM and 8OPPM. The eye diagrams were collected with a duty cycle of 50% as well and the effects of overlapping of pulses and timing jitter make discerning between symbols more difficult. For lower D, eye diagrams will close as the amplitude is reduced and overlap of signals is increased.

Figure 4.9 shows the normalized minimum distance, $\bar{d}_{min}$, for both theoretical and measured results of the boost converter and LEBD converter. Similar to the results in Chapter 3, as duty cycle is increased, $\bar{d}_{min}$ increases as well. This is due to higher amplitude pulses with less overlap being sent by LEBDs. It is also apparent

Table 4.2: BER for Increasing Modulation Order

Duty Cycle	65	60	55	50	45
BPPM/BOPPM	No Errors	No Errors	No Errors	No Errors	No Errors
4OPPM	No Errors	No Errors	No Errors	No Errors	No Errors

that measured values are below that of theoretical, however, values collected from the LEBD converter match theoretical values much more closely. This is likely due to the higher quality of sent waveforms in comparison to the LEFD converter with the resonant frequency distortion. By improving the PCB layout shown in Appendix E, sent signal quality was enhanced. Received waveforms more closely match the assumed square waves used to calculate theoretical values of $\bar{d}_{min}$ and the curvature of the trend matches theoretical results much better than the LEFD experimental setup.

As discussed in Chapter 3, the graph of $\bar{d}_{min}$ demonstrates the effects of dimming on communications clearly. Shorter duty cycles required for dimming not only severely diminish the amount of transmitted power, but also increase overlap of pulses. Despite this, it is still possible to achieve communications at the rate of the converter while enabling dimming control of the luminaire.

As done in chapter 3 with the buck converter, data sets of 10^5 symbols were created and sent through the experimental setup. For both BPPM/BOPPM and 4OPPM, throughout dimming as duty cycles were changed, BER measurements were all at or below 10^-5. The increaed quality of BER tests for the boost converter is attributed to the increase in duty cycle required to achieve nominal operating conditions. This resulted in shorter, higher amplitude pulses from LEBDs. Additionally, higher currents through the communicating LEBD based on circuit structure compared to that

of the LEFDs in Chapter 3 is another reason for improved communications performance. 8OPPM was tested and data could still not be recovered reliably. For the case of 8OPPM, failure to demodulate reliably at higher duty cycles was caused by the same problems present for the buck converter tests. Insufficient resolution of shifts from the FPGA and difficulty determining shift from the sent signal caused errors in demodulation.

Electrical Efficiency and Optical Efficacy

Figure 4.10 compares results of experimental efficiency for the base case boost converter and the LEBD converter for increasing modulation orders. As expected, the use of a single LEBD results in a loss of efficiency. This is caused by the increased V_f^{LEBD} and the correlated conduction losses. A difference in efficiency of up to 20% can be seen between simulation and those determined experimentally. This is greater than in Chapter 3 for LEFD converters, however, current values through components of the boost converter are higher. The losses discussed in Section 3.2.2 which are not accounted for in simulations are increased for higher currents and are likely the cause of these differences. Similar to LEFD converters in Chapter 3, LEBD converter designs were relatively low power and are greatly impacted by multiple sources of small losses. A difference of only 2 W accounts for 20% of the power consumed by the 10 W luminaire.

It is also apparent that modulation minimizes the amount of efficiency lost when using an LEBD. This is expected as the amount of switching transitions is reduced. The case of BPPM and BOPPM result in the greatest increases of efficiency with diminishing advantages as modulation order increases due to elimination of switching

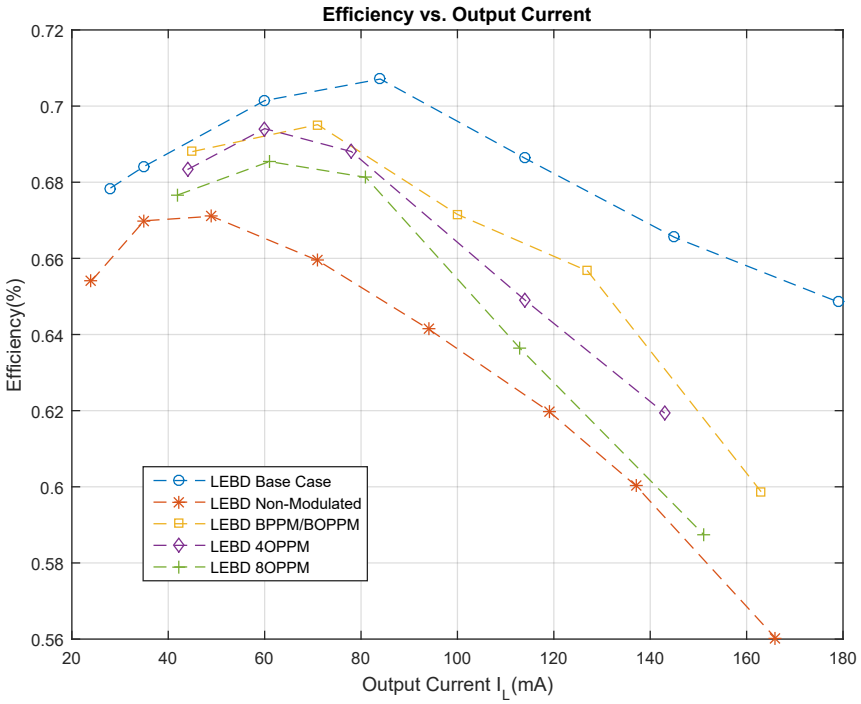

Figure 4.10: Experimentally measured efficiency of the Base Case, LEBD design non-modulated, LEBD design modulated by BPPM, and LEBD design modulated by 4-PPM

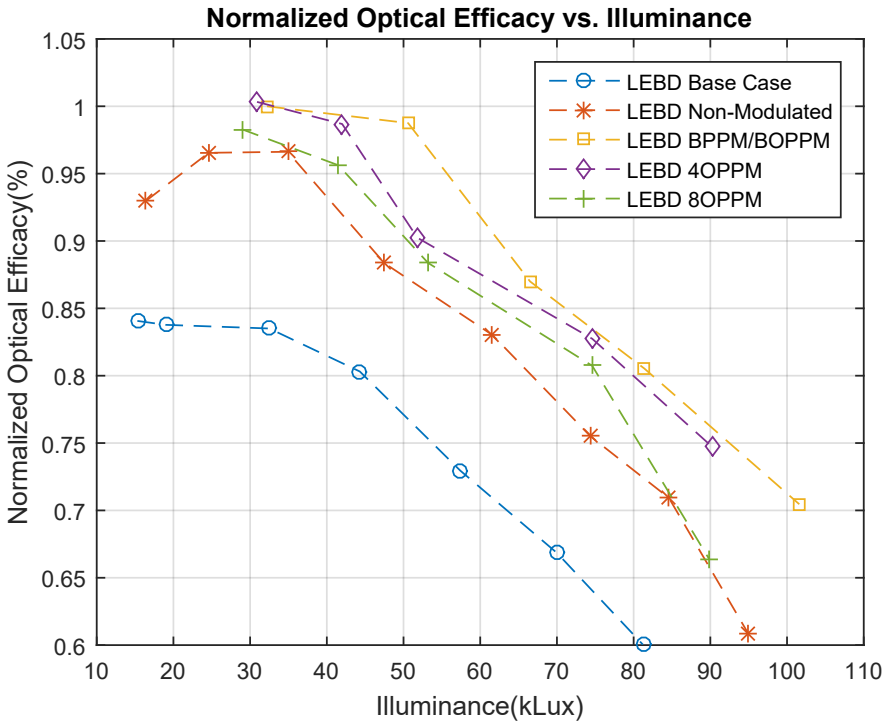

Figure 4.11: Experimental normalized optical efficacy of the Base Case, LEBD design non-modulated, LEBD design modulated by BPPM, 4OPPM, and 8OPPM.

cycles becoming a less likely occurence.

Efficacy using LEBDs is shown to be improved over the base case as demonstrated by 4.11. The amount of useful power emitted by the LEBD is not included when looking at electrical efficiency and gives a skewed expectation for performance of converters using LEBDs. When viewing efficacy, it is apparent that the LEBD contributes a significant amount of illumination compared to power consumed.

4.5 Conclusions

In this chapter, a boost converter using LEBD(s) was proposed. Changes in topology operation and resulting design considerations were discussed. The concepts outlined were used to simulate and experimentally test communications, efficiency, and efficacy.

In both simulations and experiments, efficiency and efficacy were compared for the LEBD converter versus a base case LEBD luminaire. Discrepancies between values of efficiency and efficacy are considered to be caused by incomplete modeling of losses within simulations. These tests resulted in higher luminous flux output of the LEBD converter in addition to increased efficacy. It is re-iterated that future designs may use lower power to achieve the same brightness, achieving even greater gains of efficacy. Additionally, LEBDs were modulated at the rate of SMPS and communications viability was checked through experimentation. These properties of the LEBD converter allow for lower power designs of luminaires that facilitate VLC.

Chapter 5

Conclusions

Through simulation and experiment, it has been demonstrated that the use of LEFDs and LEBDs within buck and boost converters can increase device efficacy and facilitate communications with rates proportional to converter switching frequency and modulation order. The experimental setups using a switching frequency of 400kHz and 4OPPM demonstrated a rate of 800 kbps for high duty cycles.

By demonstrating the proposed changes with a buck and boost converter topology, the use of LEFD(s) and LEBD(s) has been demonstrated as a viable solution to VLC in SMPS. Other converter topologies that include Galvanic isolation such as forward or flyback converters may take advantage of LEFDs, LEBDs, or both.

The technology presented by this thesis has demonstrated support for dimming and has the advantage of separating LEDs used for communications and illumination. The designs proposed and tested within this thesis offer a compelling combination of cost effectiveness, improved efficacy, and high rate communications for future VLC transmitters.

5.1 Future Directions

Possible future directions for the work described in this thesis are described in this section. The work presented creates an opportunity to develop LEDs with parameters better suited for the style of use proposed in this thesis. Alternatively, different choices of LEFDs and LEBDs are a future topic for this work to extend it beyond VLC and into the OWC domain. Finally, the use of better switch technologies and more complex modulation schemes would allow for higher data rates from the proposed converter topologies.

5.1.1 Higher Data Rates

While OWC can enable high rate communications (Gbps) [91] [92], these solutions are not used to provide illumination. The integration of communications within a power converter limits the achievable data rate due to limitations placed on control switches by the voltage and currents present. By using new and costly switching technologies such as GaN switches as demonstrated in [93], data rates of the proposed design can be increased.

The use of higher order and more sophisticated modulation techniques is also a source of possible data rate improvements. Fast variations of duty cycle between symbol periods can be used to encode information in pulse width while maintaining an average output brightness. Combination of changing duty cycle and pulse position may lead to modulation techniques capable of sending many more bits per symbol period. Through the combination of advanced switching technologies and higher order modulation, rates of tens of Mbps are possible.

5.1.2 LEDs designed for Reverse Biasing

LEDs are not typically used in applications where they are reverse biased. Research regarding lifetime and potential performance degradation was outside of the scope of this work. If designs using LEFDs and LEBDs become more prevalent, LEDs may be manufactured with higher reverse biasing voltages.

5.1.3 Wavelengths

This thesis focused specifically on the use of the visible range of the electromagnetic spectrum that spans for 380nm to 780nm to facilitate communications. Diodes designed for other output wavelengths may be used for LEFDs and LEBDs. luminaries using wavelengths outside of the visible range will not benefit from increased efficacy, however efficiency may not be affected as severely if diode forward voltage is reduced. The use of LEFD(s) and LEBD(s) outside of the visible spectrum, such as infrared, allow for invisible OWC links. LEDs outside of the visible spectrum can have greater modulation bandwidths, thereby increasing possible communication rates.

Appendix A

Derivation of Output Voltage Equations

Derivations of output voltage for the LEFD and LEBD converters are presented in this section. The equations follow the same procedure to deriving output voltage as outlined in [46]. The inclusion of V_f^{LEFD} and V_f^{LEBD} changes these equations as shown.

A.1 LEFD Converter

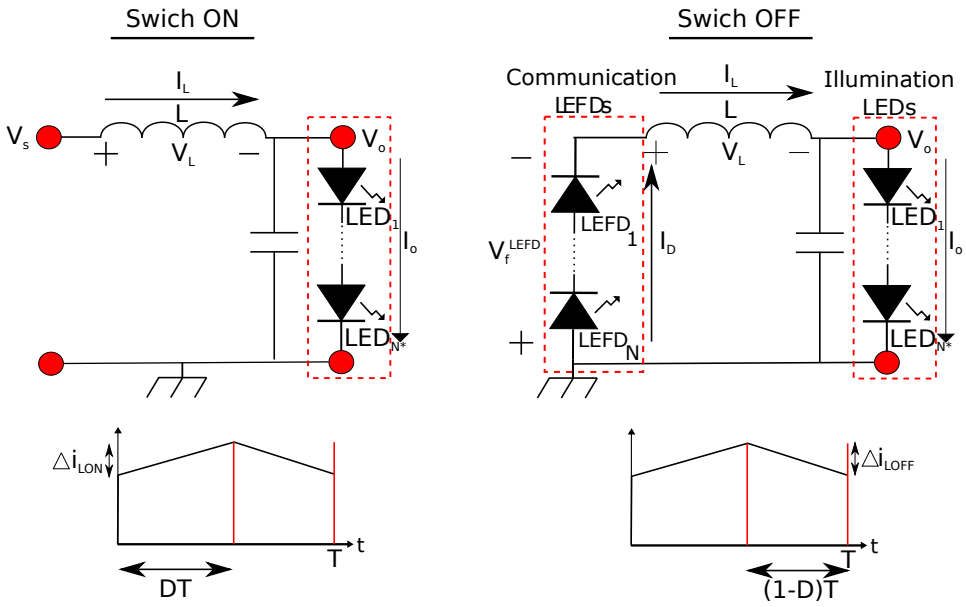

Figure A.1: Conducting and Non-Conducting States of LEFD buck converter.

The voltage across the inductor can be defined as,

$$V_L = L\frac{di_L}{dt}. \tag{A.1}$$

where change in inductor current, Δi_L, and change in time, Δt, can be assumed to be linear for ease of calculation.

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t} \tag{A.2}$$

Referencing Figure A.1, change in current during on time, Δi_{LON}, and change in current during off time, Δi_{LOFF} can be defined by the following,

$$\Delta i_{LON} = \frac{V_s - V_o}{L}DT \quad \Delta i_{LOFF} = \frac{-V_f^{LEFD} - V_o}{L}(1-D)T. \tag{A.3}$$

The change in inductor current over one period must be zero, therefore,

$$\Delta i_{LON} + \Delta i_{LOFF} = 0. \tag{A.4}$$

Through substitution, the expression,

$$\frac{(V_s - V_o)}{L} DT + \frac{(-V_f^{LEFD} - V_o)}{L}(1 - D)T = 0 \tag{A.5}$$

is found and is simplified in,

$$V_s D + V_f^{LEFD} D - V_f^{LEFD} - V_o = 0. \tag{A.6}$$

Finally, the equation is re-arranged to give V_o as shown in,

$$V_o = (V_s + V_f^{LEFD})D - V_f^{LEFD}. \tag{A.7}$$

A.2 LEBD Converter

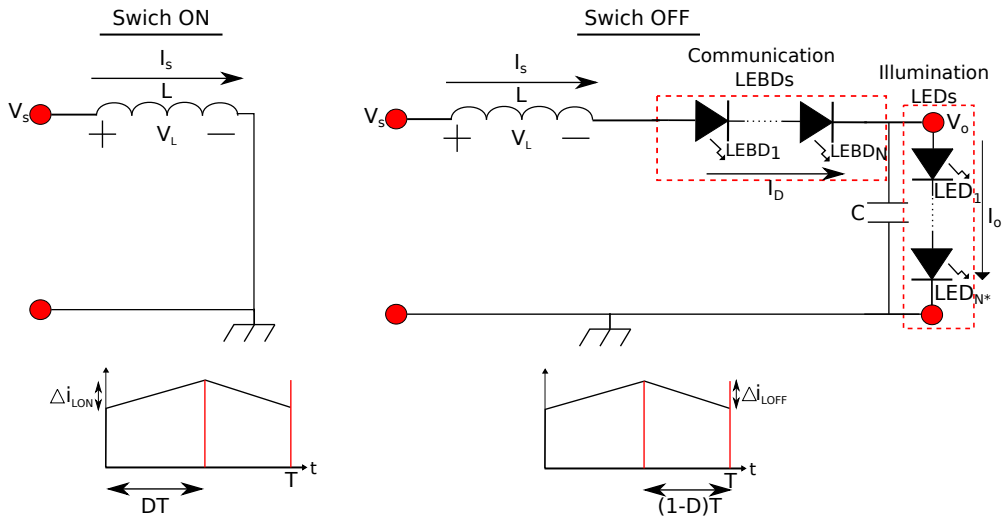

Figure A.2: Conducting and Non-Conducting States of LEBD boost converter.

Similar to the previous example, the voltage across the inductor can be defined as,

$$V_L = L\frac{di_L}{dt}. \tag{A.8}$$

The change in inductor current, Δi_L, and change in time, Δt, can be assumed to be linear for ease of calculation.

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t} \tag{A.9}$$

Referencing Figure A.2, change in current during on time, Δi_{LON}, and change in current during off time, Δi_{LOFF} can be defined by the following,

$$\Delta i_{LON} = \frac{V_s}{L}DT \quad \Delta i_{LOFF} = \frac{V_s - V_f^{LEBD} - V_o}{L}(1-D)T \tag{A.10}$$

Just as in the previous case, net inductor current for a given period must be zero to maintain steady state operation as given by,

$$\Delta i_{LON} + \Delta i_{LOFF} = 0. \tag{A.11}$$

Through substitution,

$$\frac{V_s}{L}DT + \frac{V_s - V_f^{LEBD} - V_o}{L}(1-D)T = 0 \tag{A.12}$$

is found and can be simplified to,

$$V_s - V_f^{LEBD}(1-D) - V_o(1-D) = 0. \tag{A.13}$$

Finally, by re-arranging, V_o can be solved for by,

$$V_o = \frac{V_s - V_f^{LEBD}(1-D)}{1-D}. \tag{A.14}$$

Appendix B

Modelling of LEDs for use in LTspice and Microsoft Excel

This thesis required modeling of two LED I-V characteristics in addition to luminous flux characteristics as a function of current.

An iterative method using the exponential model (2.4) with a series resistor and data from I-V graphs in datasheets of the 3535L [69] and XLamp XP-E2 [90] was used to approximate diode parameters. These values for parameters found were used in LTspice for all simulations to estimate efficiency and efficacy as accurately as possible. The parameters and subsequent I-V characteristics are shown in B.3 and B.4.

B.1 I-V Characteristics

The plot in Figure B.3 displays the I-V characteristics as simulated by a voltage sweep in LTspice. This was done to verify the estimated parameters resulted in matching simulated I-V characteristics when compared to the datasheet [69].

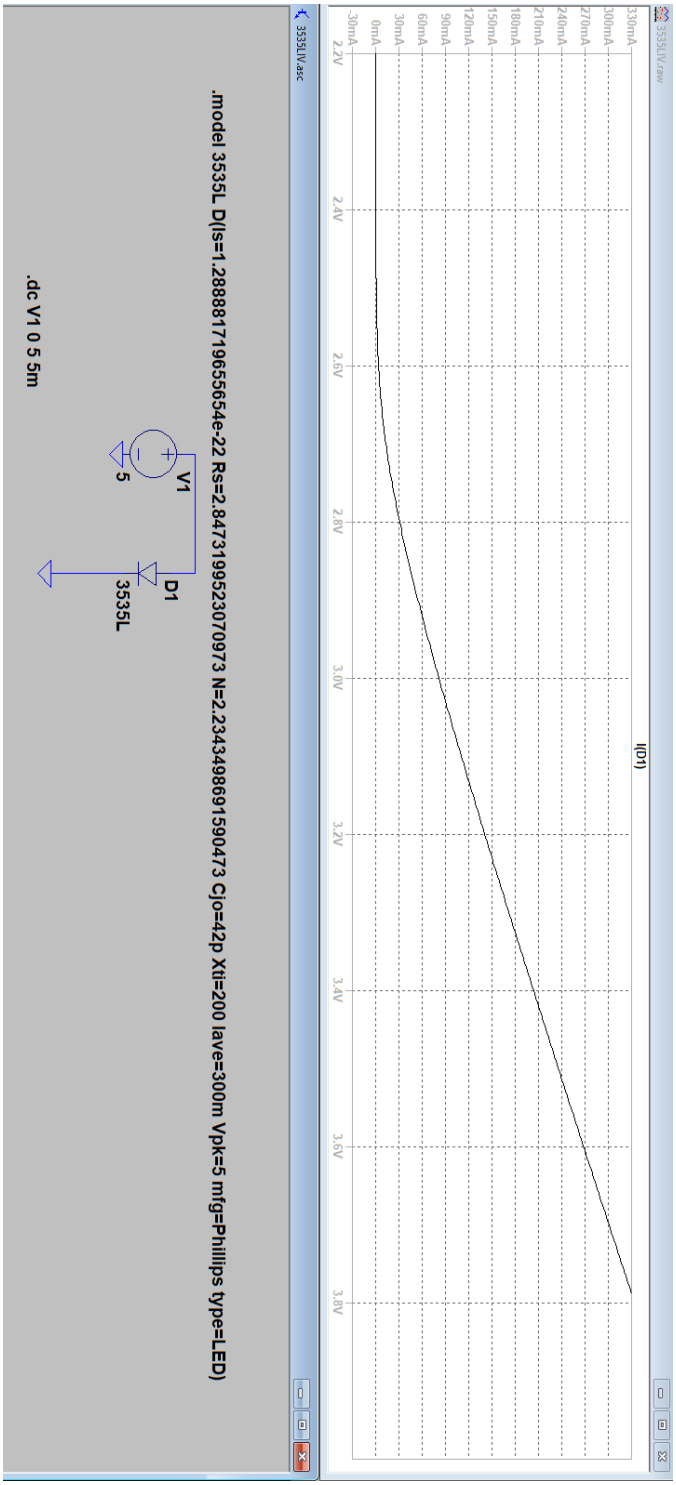

Figure B.3: Plot of Philips 3535L I-V characteristics in LTspice using estimated parameters.

The process was repeated and a set of I-V characteristics for the CREE Xlamp XP-E2 [90] was simulated in LTspice. This was compared to the datasheet to verify that the I-V characteristics used matched.

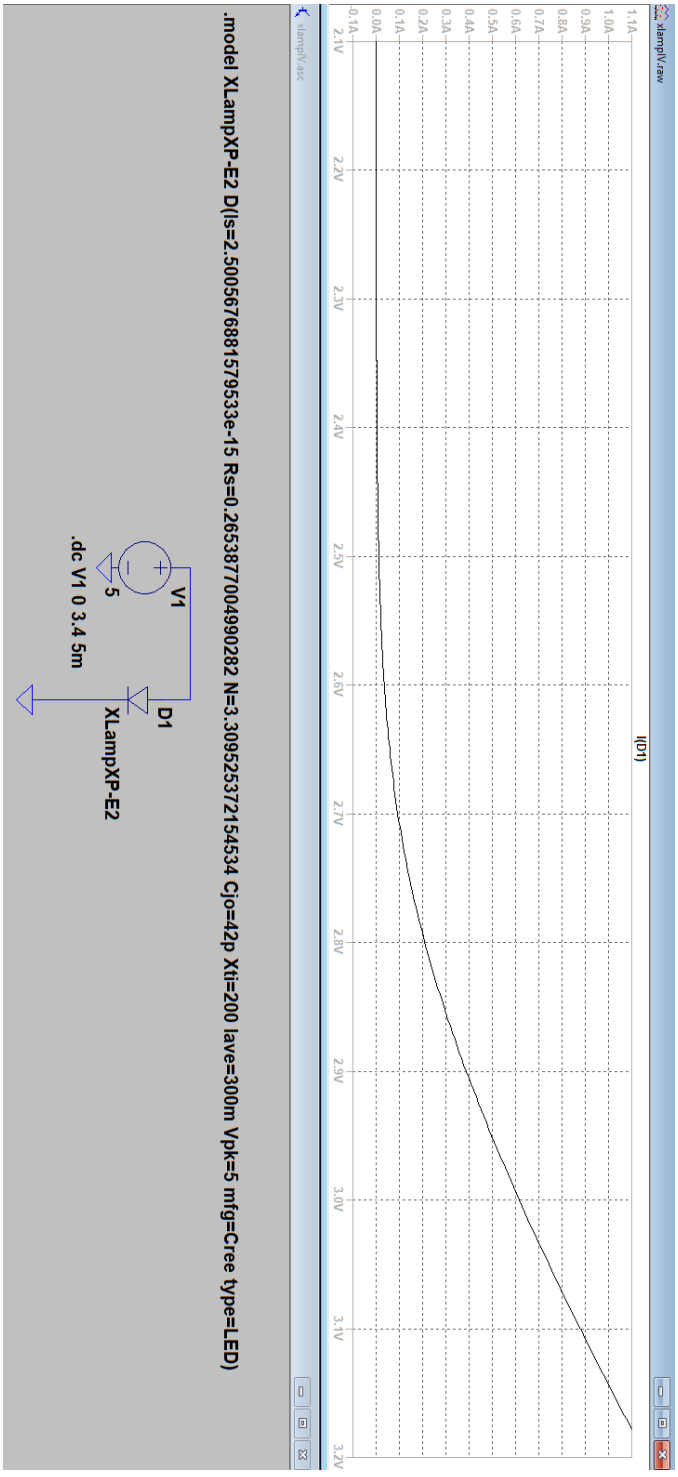

Figure B.4: Plot of CREE XLamp XP-E2 I-V characteristics in LTspice using estimated parameters.

B.2 Luminous Flux Fitting

Luminous flux for the Philips 3535L LEDs [69] was taken from the datasheet and plotted in Microsoft Excel [74]. Using the trendline tool, a quadratic fit with R^2 of 1 was found as described by equation (3.4).

$$\Phi_V(I)[lm] = -0.0002I^2 + 0.531I + 0.4035 \qquad R^2 = 1 \tag{B.15}$$

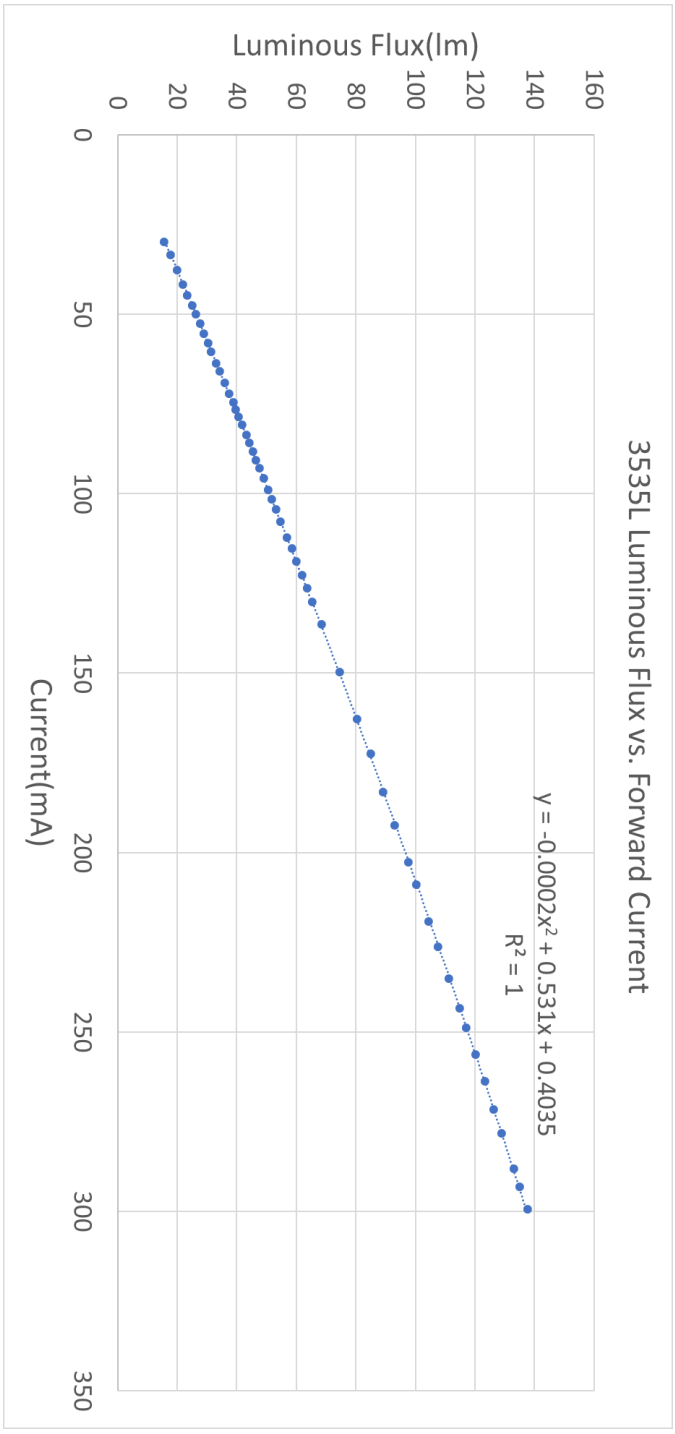

Figure B.5: Fit found using Microsoft Excel for luminous flux of 3535L LED given forward current.

Similarly, luminous flux for the CREE XLamp XP-E2 LEDs [90] was taken from the datasheet and plotted in Microsoft Excel [74]. Using the trendline tool, a quadratic fit with R^2 of 0.9998 was found as described by equation (4.2).

$$\Phi_V(I)[lm] = -0.0001I^2 + 0.3451I + 5.1269 \qquad R^2 = 0.9998 \tag{B.16}$$

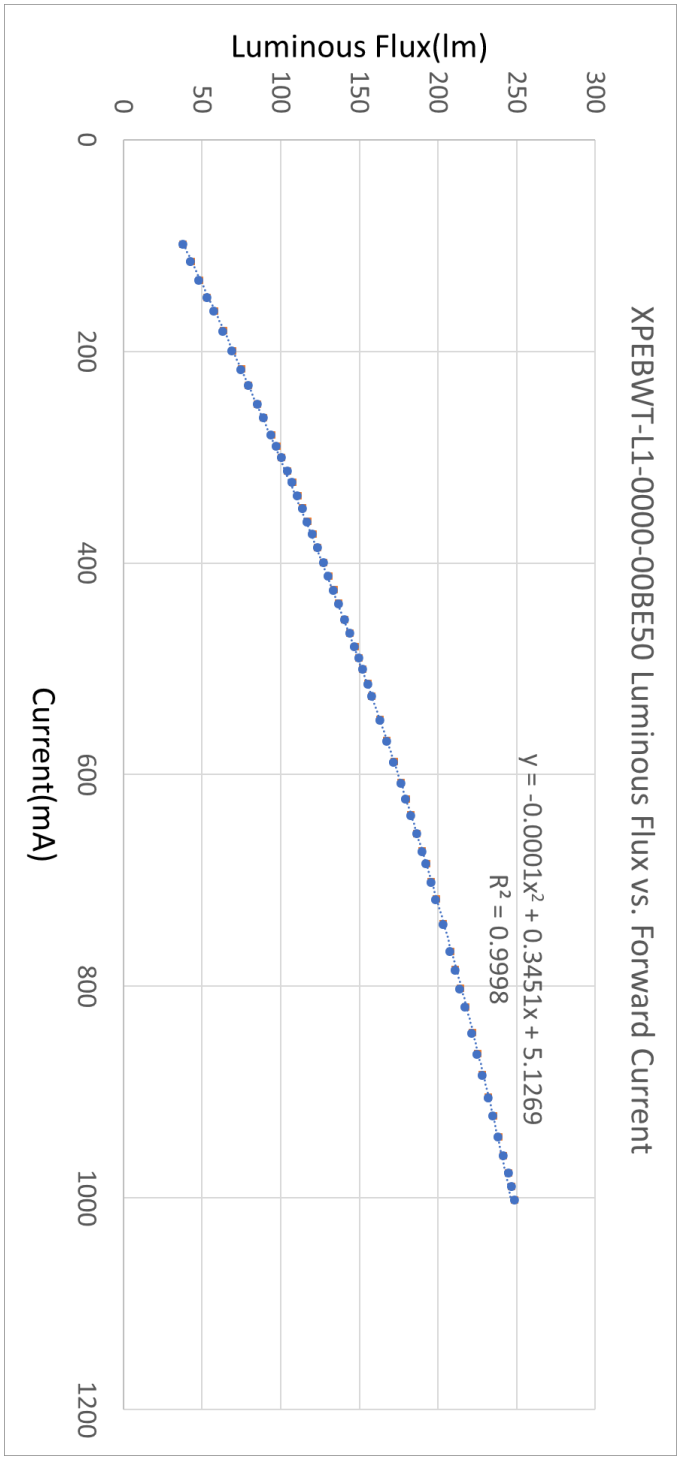

Figure B.6: Fit found using Microsoft Excel for luminous flux of CREE XLamp XP-E2 LED given forward current.

Appendix C

Modulation Via FPGA

The DE0-Nano FPGA [81] was used to implement modulation signals for use in experimental prototypes discussed in Chapters 3 and 4. Control waveforms were created based upon PPM and OPPM (depending on duty cycle) sample waveforms as described in Section in equations (2.29) and (2.31). Waveforms were generated as the LEFD or LEBD would output them due to the inverting logic provided by the opto-isolator before the SMPS control switch.

Figure C.7 gives an example waveform stored in ROM.

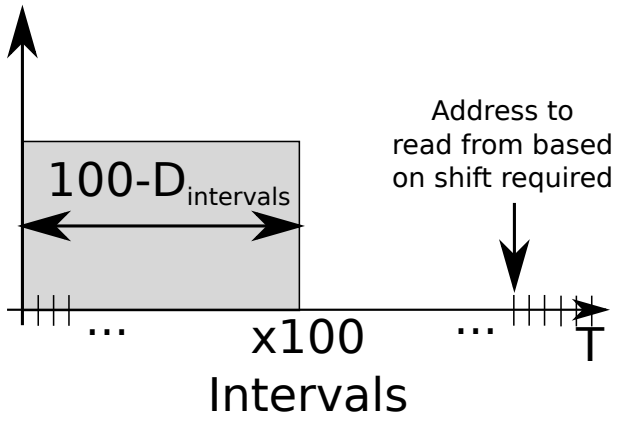

Figure C.7: Diagram depicting algorithm to produce FPGA control waveform.

Periods were split into 100 intervals. Duty cycle was adjusted by controlling the number of intervals, $D_{intervals}$, the waveform produced by the DE0 was low for,

$$D_{intervals} = 100D. \tag{C.17}$$

Pulses of increasing duty cycles were prepared and saved into wav files for use in the FPGA. These files all had pulses starting at time zero and were logic high for $100 - D_{intervals}$. The FPGA used these waveforms in order to create PPM or OPPM symbols based on a data value, k, read from a randomly generated data set, saved in a separate ROM. In order to mimic the symbols defined by equations (2.29) and (2.31), the FPGA read from an address coded for each shift given a specific duty cycle. When the FPGA reaches the end of the wav file, the address to read from is set to zero and it will start to read from the start of the wav file on the next increment of the counter. By doing this, shift can easily be encoded in addresses without the need to save multiple symbols in ROM.

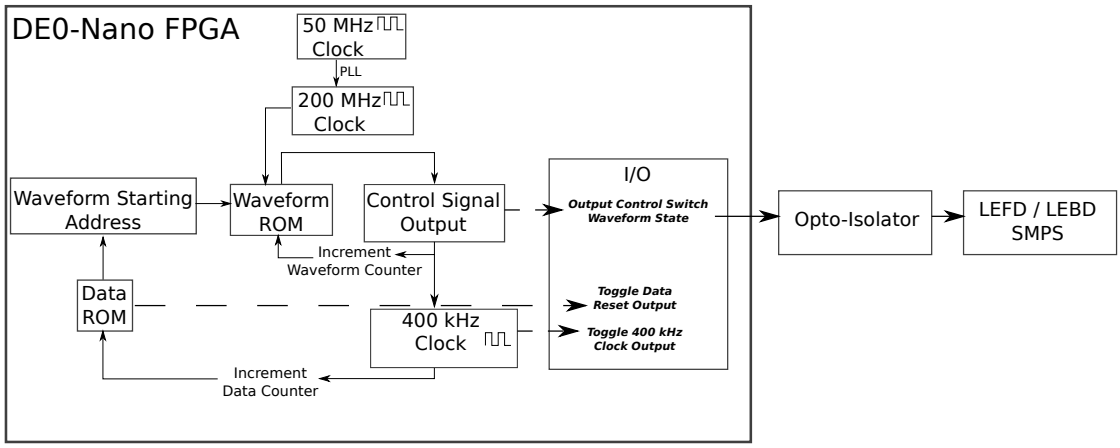

Figure C.8: Diagram depicting algorithm to produce FPGA control waveform.

The method to determine the shift address is as follows,

$$Shiftaddress = 100 - k \left\lfloor \frac{100D}{M-1} \right\rfloor . \tag{C.18}$$

The floor is taken to account for fractional shifts and any leftover clock cycles present due to rounding are placed at the end of a period. This results in a "guard" interval to differentiate between symbol periods. For higher clock frequencies, this would not be present as the fractional shift could be accounted for.

Figure C.8 gives a top level block diagram for of the FPGA. The diagram displays the clocks responsible for updating each ROM. The 50 Mhz clock of the DE0-Nano is used to generate a 200 MHz clock via a PLL. This is then used to create the 100 intervals needed for a 400 kHz period signal. This is done as the 50 MHz clock does not divide evenly for this setup. By using a 200 MHz clock and using it to every 4 clock cycles, a 40 MHz update cycle is created. This allows for the 400 kHZ period waveform to be updated 100 times per period.

C.1 FPGA VHDL Code

```
`timescale 1ns/100ps
`default_nettype none

module N_PPM(
  input logic CLOCK_50,
  output logic GPIO_0[33:0],
  input [2:0] SW
);

logic resetn;
logic CLOCK_200;
logic lock;
integer data;
logic [5:0] binarydata;
integer datacount = 0;

-- define and set all counters data and outputs
integer counter = 0;
integer PPM_counter = 0;
integer address_counter = 0;
-- Used to generate 400kHz clock
integer count_to = 400;
-- Step Size of 5 clock cycles (200MHz clock)
```

```
--100 Steps per period
integer PPM_count_to = 4;
integer flag = 0;
-- Define Output
logic wav_out;
integer binData;
logic dataLoop;
logic DataWav;
logic dataClck;

assign resetn = ~SW[0];

-- Define PLL for 200MHz clock
PLL pll_inst0(
   .areset(resetn),
   .inclk0(CLOCK_50),
   .c0(CLOCK_200),
   .locked(lock)
);

-- Define set duty cycle waveform to be shifted
wav wav_inst0(
   .address(address_counter),
   .clock(CLOCK_200),
```

```
  .q(wav_out)
);

-- define dataset
binData binData_inst0(
  .address(datacount),
  .clock(CLOCK_200),
  .q(binData)
);

always_ff@(posedge CLOCK_200 or posedge resetn)begin

  if(resetn == 1) begin
    counter <= 0;
    -- Reset Frequency Dividing Counter
    PPM_counter <= 0;
    -- Count to duty cycle - 1
    -- Duty cycle hard coded, must be changed manually
    -- Library of output files with various duty cycles was made
    address_counter <= 59;
  end

  else begin
```

```
if(PPM_counter == PPM_count_to) begin
  if(counter == count_to) begin
    counter <= 0;
    address_counter <= 59;
    -- Loop based on length of data
    -- example size of 10^5
    if(datacount == 100000) begin
      datacount <= 0;
      data <= binData;
    dataLoop <= !dataLoop;
    dataClck <= !dataClck;
    end
    else begin
      data <= binData;
      flag <= 0;
      -- Increment data index counter
      datacount <= datacount + 1;
      dataClck <= !dataClck;
    end
  end
  else begin
    PPM_counter <= 0;
    if(address_counter == 99) begin
      address_counter <= 0;
```

```
end
else begin
  address_counter <= address_counter + 1;
end
-- BOPPM
-- Two symbols, set address shifts for BOPPM
if((data == 0) && (flag == 0)) begin
  address_counter <= address_counter-0;
  flag <= 1;
end
else if((data == 1) && (flag == 0)) begin
  address_counter <= address_counter-59;
  flag <= 1;

end
/*
-- 4OPPM
-- Four symbols, set address shifts for 4OPPM
if((data == 0) && (flag == 0)) begin
  address_counter <= address_counter-0;
  flag <= 1;
end
else if((data == 1) && (flag == 0)) begin
  address_counter <= address_counter-20;
```

```
    flag <= 1;

end
else if((data == 2) && (flag == 0)) begin
    address_counter <= address_counter-40;
    flag <= 1;

end
else if((data == 3) && (flag == 0)) begin
    address_counter <= address_counter-59;
    flag <= 1;
end
-- 8OPPM
-- Eight symbols, set address shifts for 8OPPM
if((data == 0) && (flag == 0)) begin
    address_counter <= address_counter-0;
    flag <= 1;
end
else if((data == 1) && (flag == 0)) begin
    address_counter <= address_counter-8;
    flag <= 1;

end
else if((data == 2) && (flag == 0)) begin
```

```
    address_counter <= address_counter-16;
    flag <= 1;

  end
  else if((data == 3) && (flag == 0)) begin
    address_counter <= address_counter-24;
    flag <= 1;

  end
  else if((data == 4) && (flag == 0)) begin
    address_counter <= address_counter-32;
    flag <= 1;

  end
  else if((data == 5) && (flag == 0)) begin
    address_counter <= address_counter-40;
    flag <= 1;

  end
  else if((data == 6) && (flag == 0)) begin
    address_counter <= address_counter-48;
    flag <= 1;

  end
```

```
        else if((data == 7) && (flag == 0)) begin
          address_counter <= address_counter-56;
          flag <= 1;

        end
        */
        -- Output shifted value of Waveform
        -- Loops x100 times(whole period)
        DataWav <= wav_out;
      end
    end
    -- Increment counters
    else begin
      counter <= counter + 1;
      PPM_counter <= PPM_counter + 1;
    end
  end
end
-- Assign outputs to IO
  assign GPIO_0[3] = dataLoop;
  assign GPIO_0[2] = DataWav;
  assign GPIO_0[4] = dataClck;
endmodule
```

Appendix D

Additional Experimental Communication Results

The diagrams presented in this appendix demonstrate 4OPPM and 8OPPM sample waveforms and eye diagrams for duty cycles of 50%. Design parameters and collection methods match those found in Chapters 3 and 4, described in Sections 3.3.1 and 4.4.1. Waveforms were collected with a gain of 10dB on the THORLABS PDA36A photodiode [85]. For the LEFD converter, eye diagrams were also collected with a gain of 20dB with a lower bandwidth to filter high frequency resonance frequencies that distort the signals.

D.1 LEFD Sample Signals and Eye Diagrams

D.1.1 4OPPM

Similar to Section 3.3.2 with BPPM, LEFD received waveforms were distorted by a resonant frequency for 4OPPM. Further collected data adjusted the photodiode gain to 20 dB to low pass filter higher frequencies.

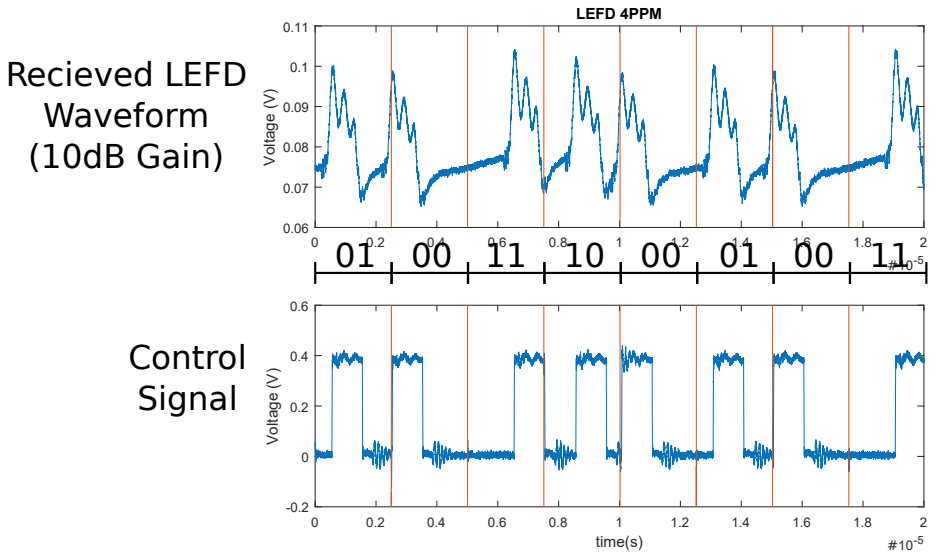

Figure D.9: Sample Received and sent 4OPPM LEFD waveforms.

Eye diagrams for the LEFD converter modulated with 4OPPM are displayed in Figure D.10. The eye diagram is open and transitions are clear.

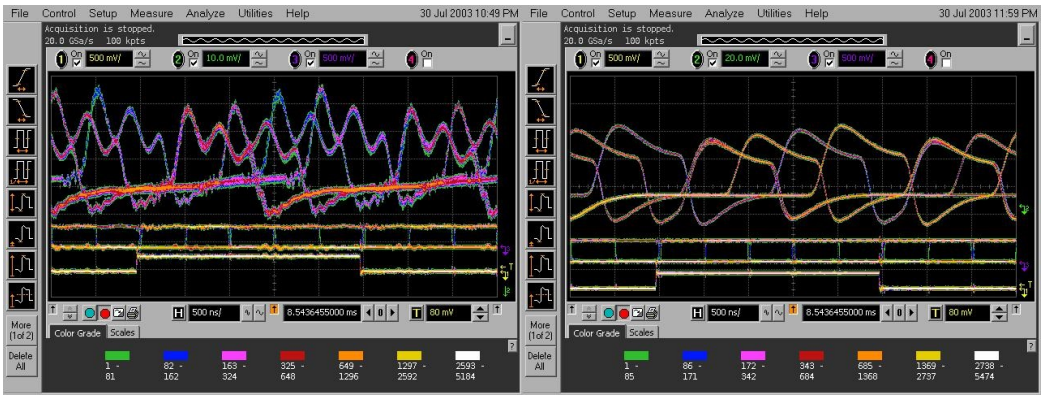

Figure D.10: LEFD 4OPPM Eye Diagram for 10 dB gain, high bandwidth and 20 dB gain, low-pass filtered.

D.1.2 8OPPM

Sample waveforms of 8OPPM present the same results as shown by BPPM and 4OPPM.

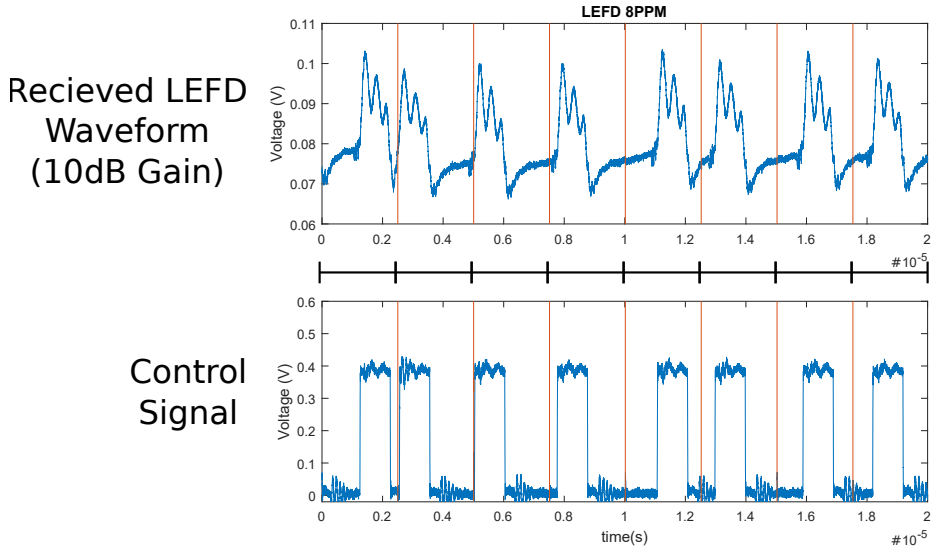

Figure D.11: Sample Received and sent 8-PPM LEFD waveforms

The eye diagram presented for the LEFD converter modulated by 8OPPM as shown in Figure D.12 is open, however the amount of overlap between symbols can be seen to significantly increase from 4OPPM. Transitions for this duty cycle are still clear, however the rise and fall times overlap with adjacent symbols making differentiation difficult. Dimming of the luminaire for 8OPPM will yield results with a closing eye due to reduced amplitude and greater overlap, making symbols even more difficult to differentiate.

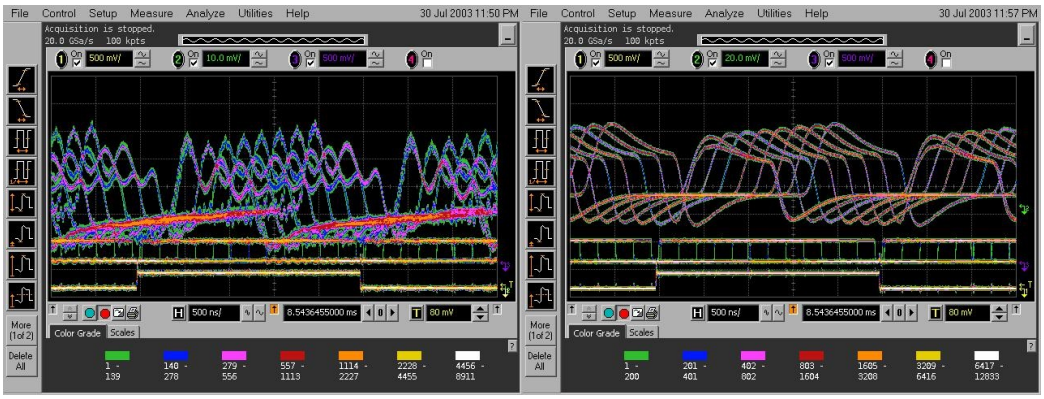

Figure D.12: LEFD 8OPPM Eye Diagram for 10 dB gain, high bandwidth and 20 dB, low-pass filtered.

D.2 LEFD Sample Signals and Eye Diagrams

D.2.1 4OPPM

A set of 4OPPM sable sent and received waveforms are depicted by Figure D.13. The waveforms are not distorted by a resonant frequency as LEFD sets were and symbols are clearly able to be distinguished.

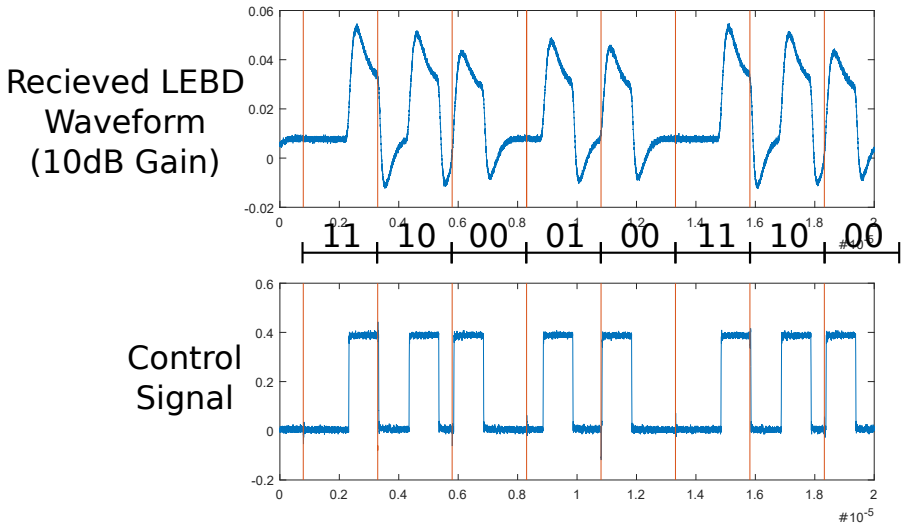

Figure D.13: Sample Received and sent 4OPPM LEBD waveforms.

An eye diagram for the LEBD converter modulated by 4OPPM is shown in Figure D.14. The amplitude of the signals is large compared to noise, resulting in an open eye. Transitions are clear, however a significant amount of symbol overlap is present.

Figure D.14: LEBD 4OPPM Eye Diagram.

D.2.2 8OPPM

Resulting 8OPPM waveforms for the LEBD converter are demonstrated by Figure D.15. Though these waveforms appear to be easily distinguishable, errors of the nearest adjacent symbols were common.

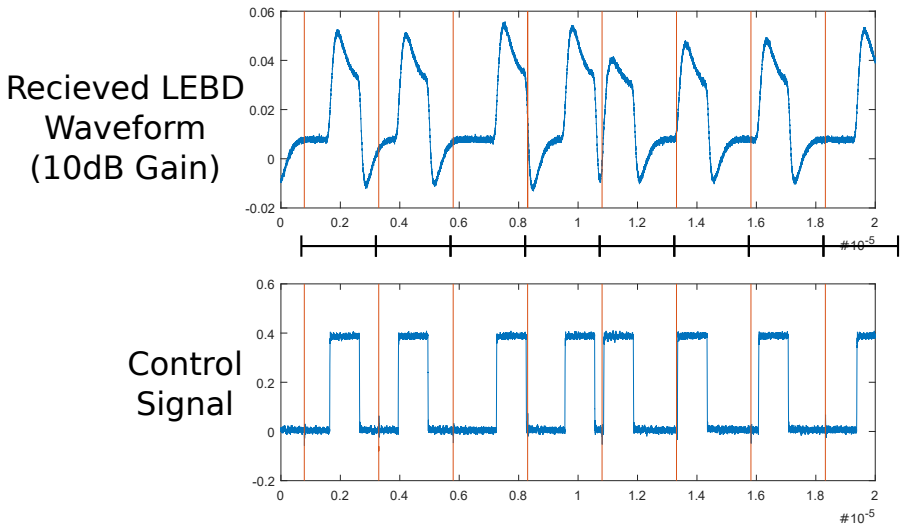

Figure D.15: Sample Received and sent 8OPPM LEBD waveforms.

Finally, an eye diagram of 8OPPM for the LEBD converter is presented by Figure D.16. As discussed with the LEFD converter, amplitude of signals is large compared to noise levels resulting in an open eye. A large amount of overlap is present for symbols making it difficult to discern the symbol sent. Additionally, rise times of adjacent symbols overlap, further reducing ability to distinguish signals.

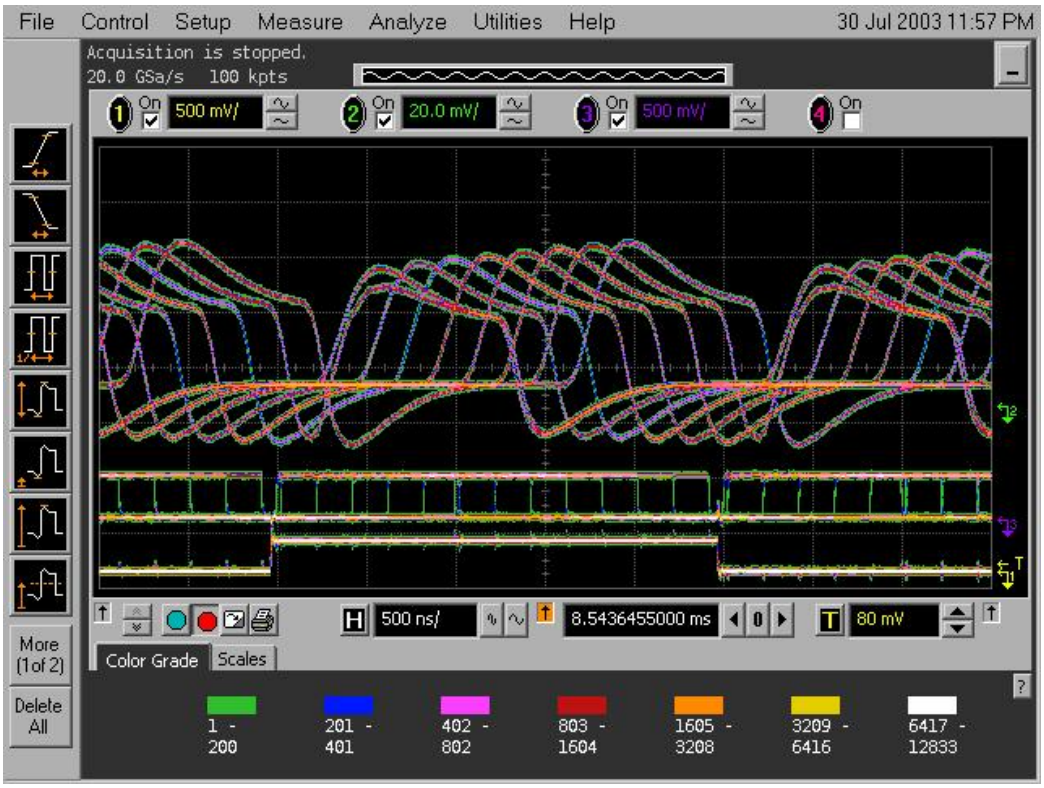

Figure D.16: LEBD 8OPPM Eye Diagram.

Appendix E

Printed Circuit Board (PCB) Layout

The images found within this appendix show the PCB layout of the LEFD and LEBD converters tested. The PCB was designed to be modular and allow for testing of various designs such as the case of a typical freewheeling or blocking diode. The number of illumination LEDs, LEFD(s) or LEBD(s) could be changed through some modification. By using the same PCB for the base case and modulated designs, losses caused by the PCB were common between the two designs.

E.1 LEFD Converter PCB Layout

Figure E.17 displays the LEFD converter PCB design. This PCB used a ground plane on the opposite side of many of the components. This was done to simplify the layout process, however, this also introduced parasitic capacitance responsible for the ringing seen in the experimental results of Chapter 3.

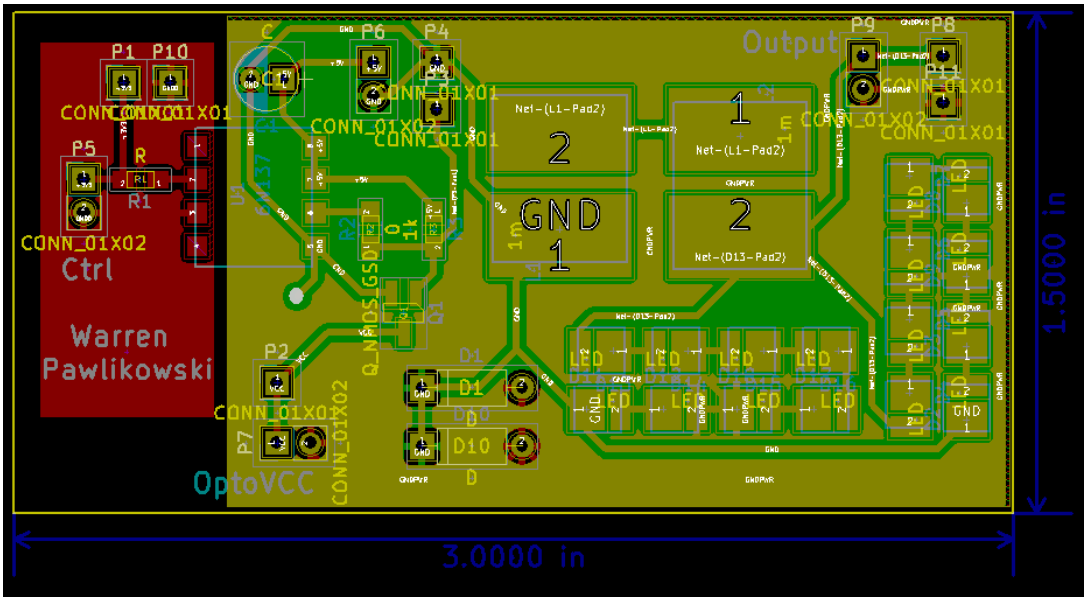

Figure E.17: Printed Circuit Board (PCB) Layout of LEFD converter prototype.

E.2 LEBD Converter PCB Layout

The LEBD converter PCB layout is shown in Figure E.18. The design of this PCB minimized the amount of vias and usage of the second layer of the PCB. The elimination of a ground plane on the second layer reduced parasitic capacitance present. The improved PCB layout is responsible for the higher quality waveforms recorded in Chapter 4.

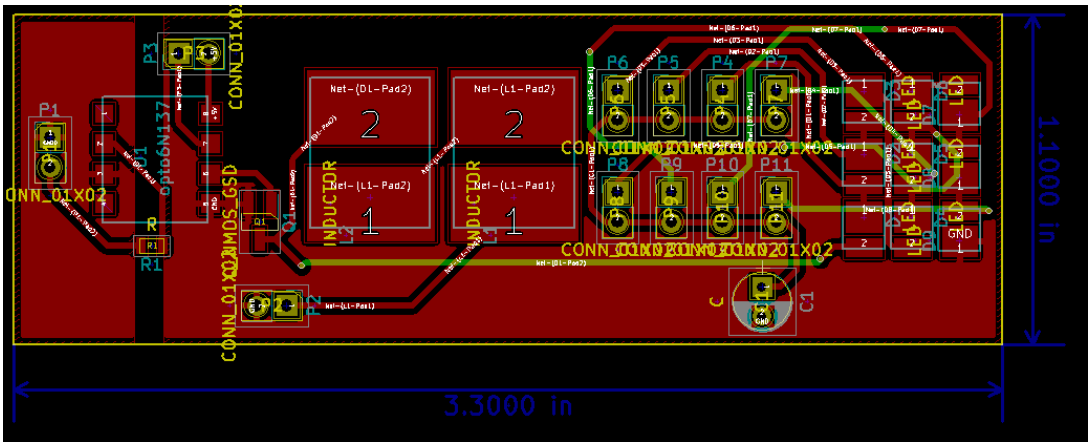

Figure E.18: Printed Circuit Board (PCB) Layout of LEBD converter prototype.

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