Hybrid FPGA/MCU Supervisory Controller for Multi-Source Inverter Integrated with Hybrid Energy Storage System in Electrified Vehicles

HYBRID FPGA/MCU SUPERVISORY CONTROLLER FOR MULTI-SOURCE INVERTER INTEGRATED WITH HYBRID ENERGY STORAGE SYSTEM IN ELECTRIFIED VEHICLES

BY

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To my parents France Pageot and Djaafar Ramoul along with my brother Bryan Ramoul. Thank you for always being there and to never have given up on me. We all had our own battles and I am glad we have come out of them!

Abstract

This thesis discusses how to apply parts of the aerospace safety standard processes and guidelines such as the DO-254 and DO-160 to the firmware and hardware design of a supervisory control board for the E/E powertrain systems of an electric vehicle. A supervisory control board is developed as an ECU that is a computer-based electronic module intended to be used for automotive and aerospace applications. The functions of the developed ECU acquires/monitors system parameters, isolates and detects system faults, and communicates with the vehicle. The ECU includes two main sub-modules including a safety critical digital core based on NXP's MPC5777m MCU and a FDAC system based on Xilinx's Artix-7 FPGA. ECU micro-processing module and digitized analog I/O processed in an FPGA for aerospace application will enable this technology for the automotive application for fast and reliable supervisory controls capable of handling complex multi-physics control strategies.

A Neural Network Energy Management Controller (NN-EMC) is also designed and applied to a HESS using the Multi-Source Inverter (MSI). Its aim is to manage the current sharing between a Li-ion battery and an Ultracapacitor by actively controlling the operating modes of the MSI. A discharge duty cycle that biases the use of one source over another is used as the control variable. To limit the battery wear and the input source power loss, an optimized solution is obtained with Dynamic

Programming (DP). The NN-EMC is designed with an artificial neural network and trained with the optimized duty cycle obtained by DP. The DP/NN-EMC solution was compared to the battery-only Energy Storage System (ESS) and the HESS-MSI with 50% discharge duty cycle. Both the battery RMS current and peak battery current have been found to be reduced by 50% using the NN-EMC compared to the battery-only ESS for the New York City drive cycle.

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Notation and abbreviations

ABS - Automatic Braking System

ADC - Analog to Digital Converter

ANN - Artificial Neural Network

ARINC - Aeronautical Radio Incorporated

ARM - Advanced RISC Machine

ASIC - Application Specific Integrated Circuit

BIST - Built-In Self Test

BITE - Built-In Test Equipment

CAN - Controler Area Network

CDS - Cockpit Display System

CIDS - Cabin Intercommunication Data System

CISC - Complex-Instruction-Set Computing

CPU - Computing Processing Unit

DAC - Digital to Analog Converter

DP - Dynamic Programming

EASA - European Aviation Safety Agency

ECU - Electronic Control Unit

EMI - Electromagnetic Interference

eSCI - Enhanced Serial Communication Interface

ESD - ElectroStatic Discharge

FAA - Federal Aviation Authorities

FDAC - Fast-Data Acquisition and Control

FIT - Failure In Time

FPGA - Field Programmable Gate Array

FWS - Flight-Warning System

HW - Hardware

ISA - Instruction Set Architecture

ISC - Short Circuit Current

LISN - Line Impedance Stabilization Network

MCU - Micro Controller Unit

MMU - Memory Management Unit

MTBF - Mean Time Between Failure

NVM - Non-Volatile Memory

OS - Operating-System

PLD - Programmable Logic Device

PowerPC - Performance Optimization With Enhanced RISC – Performance Computing

Req - Requirement

RF - Radio-Frequency

RTCA - Radio Technological Committee Authorities

RTL - Register-Transfer Level

SW - Software

UC - Ultracapacitor

UUT - Unit Under Test

TI - Texas Instrument

TVS - Transient Voltage Suppressor

Vds - Drain-to-Source Voltage

VOC - Voltage Open Circuit

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Chapter 1

Introduction

1.1 Motivation

The trend towards hybridization of vehicle propulsion systems has made the task of managing system energy flow increasingly complex and varied. For example, hybrid electric vehicle energy management systems aim to minimize fuel consumption while aerospace propulsion systems ensure fail safe operation and multi-source grid tied electric systems may minimize peak power draw, maximize backup power availability, or both [4]. New research has started to focus on a range of hybrid and electric aerospace propulsion systems for hydrocarbon and solar powered planes and airships [5–11]. Fuel cell emergency power units for aerospace have also been investigated, and a range of meta-heuristic energy management algorithms have been investigated [12]. Various energy management strategies have also been developed for vehicle charging, renewable energy, maritime, and other grid tied systems as well [4, 13–18].

The E/E architecture associated with these complex and varied propulsion systems

have been exposed to their own challenges due to the increased communication bandwidth, self-diagnostic features, flexibility and rigorous safety requirements [19,20]. For example, in the aerospace industry, federal regulations have pushed federated avionics architectures as a compromise between centralized and distributed architectures as a push towards a more centralized E/E architecture [21]. This has pushed the simple and safe analogue techniques for controlling avionics systems to much more complex embedded controllers comprising of control and monitor Field Programmable Gate Arrays (FPGAs), reliable Micro-Controller Units (MCUs), Digital-to-Analog Controllers (DACs) and Analogue-to-Digital Controllers (ADCs) [22]. Communication protocol standards by Aeronautical Radio Incorporated (ARINC) such as ARINC 429, ARINC 664 pt7 and MIL-1553 have been implemented in the E/E Architecture to ensure deterministic and reliable communication links between distributed avionics [23]. More rigorous verification processes are now in place to ensure safe design of software and firmware in aircrafts that have driven verification and validation costs upwards.

Another example is that of the automotive industry where domain and zonal architectures have been widely investigated due to the increased number of Electronic Control Units (ECU) [24]. In the domain architecture, functionalities of many ECUs are combined to form powerful supervisory ECU providing commands to less powerful ECUs called smart actuators/sensors [22]. Communication protocols such as Ethernet and Time Deterministic Ethernet have been introduced for the powerful supervisory ECUs while a slower communication medium (CAN, FlexRay, LIN, etc.) is used for the smart actuators/sensors [25, 26].

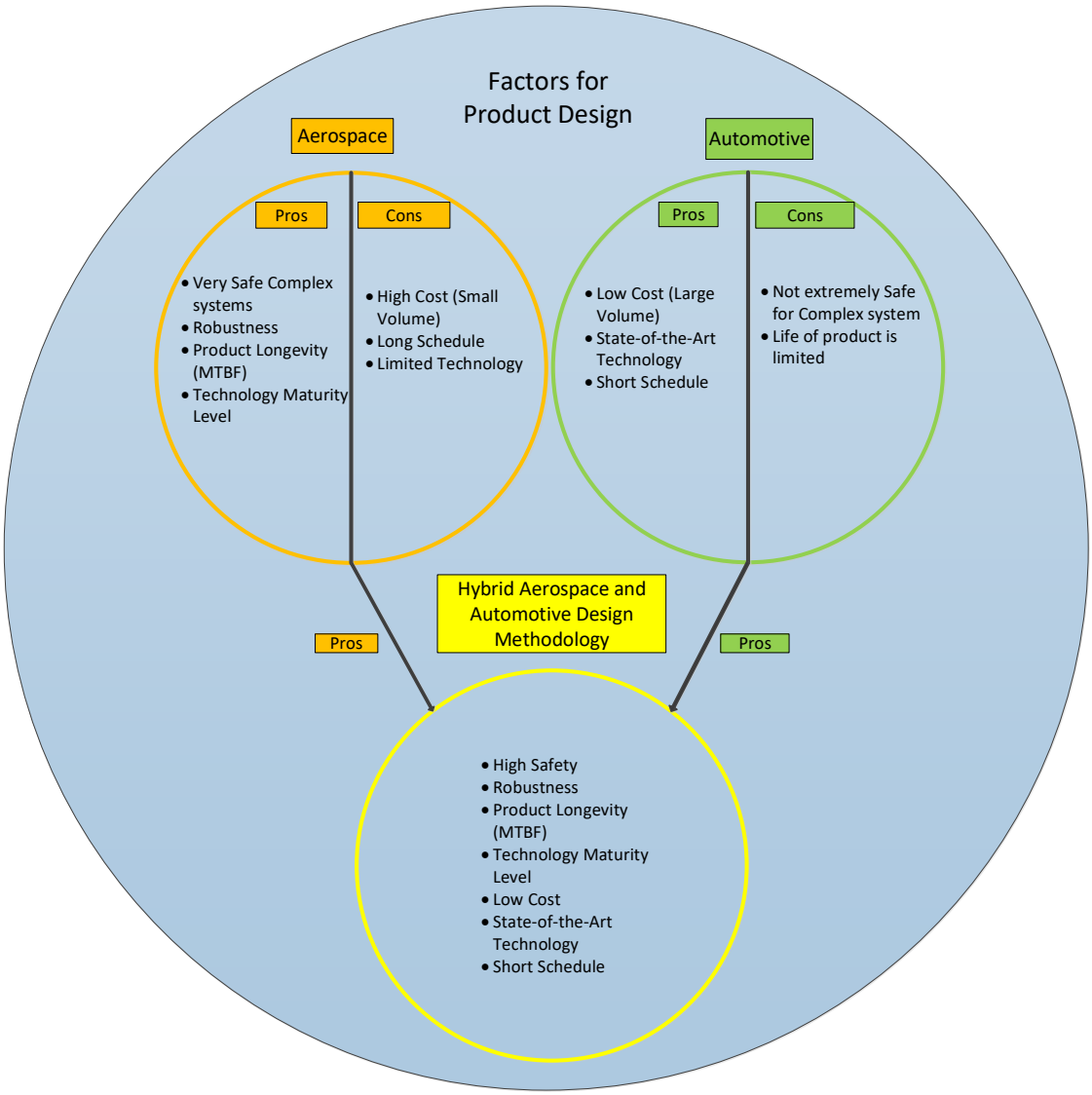


Figure 1.1: Aerospace process applied to the automotive technologies

The challenge of designing commercial vehicles is mounting as the electrical systems grow in size and sophistication. Several interconnected networks of Electronic Control Units (ECUs), sensors, and actuators monitor and control the critical mission

systems in modern vehicles. This system of ECUs is constantly measuring system parameters such as temperature, pressure, and position of various components. The combination of ECU's also control the activation of electrical and hydraulic actuators, engine and drivetrain components, and much more. The increasing systems complexity of commercial and off-highway vehicles is similarly evident in the cabin. Agricultural tractors, for example, now feature electronic and digital controls as well as cabin amenities like heated seats and climate control systems [27].

As electronics are being designed into automobiles, both driven and driverless, that brings functional safety down into the hustle and bustle of cars built for consumers. So, the goal shifts from making sure nothing can ever go wrong (practically speaking) to arranging for any system experiencing a fault to naturally move into a safe state. There's no question that providing for functional safety takes additional work. But it's much less work than a re-design after recall of a component or vehicle and a lot less expensive. There are all the electronics being designed into automobiles, both driven and driverless. That brings functional safety down from the rarified world of military/aerospace and directly into the cars built for consumers. The DO-160 and DO-254 are standards for aerospace hardware design. The adoption of these standards has helped improve the safety of the aircraft electrical and electronic (E/E) systems in avionics of aircrafts.

1.2 Development Process for Safety Critical Avionics

This part discusses guidelines for planning, developing and testing a new design for safety critical avionics. The design starts with the system specifications and ends up in a produced piece of hardware. These guidelines will be applied on a real design project for the aerosapce industry.

Component obsolescence and lower cost requirements raise various challenges when new technologies are introduced. The fail-safe and redundant implementations are the most important requirements to be met in order to prevent any system error from causing incidents that might endanger people's lives. The aerospace industry is constrained to build safety critical systems. These systems include complex programmable logic device (fush as Field Programmable Gate Arrays) as a complement of a CPU (SoftWare). In a safety critical system, the reliability on the implementation in civil aircrafts is really strict such that a catastrophic error must not appear more than once in 10^9 flight hours on average [3, 28]. The RTCA DO-254 [29], released in April 2000, is a guideline for design of airborne complex electronic HW. The DO-254 has been introduced in order to help the aviation industry verify that these new technologies still meet the fail-safe requirements set up by the Federal Aviation Administration (FAA), Transport Canada (TCA) and European Aviation Safety Agency (EASA). The ability to test and independently verify the functionality of both the analog and the digital electronics is crucial to whether or not it can be used in safety critical airborne systems. The analogous of the DO-254 is the DO-178 which is the development process for software design in safety critical avionics systems [30].

1.2.1 Development Process

Fig.1.2 demonstrates the development process in safety critical avionics. The process starts with the ARP4754 that states the design guidelines to obtain a fail-safe or fail-operational product [28]. The elements that are used for safety assessment are shown in Fig.1.3 and deal from the identification of the hazards, requirement generation due to the hazards and then a complete analysis of the hazards due to the implementation of the system.

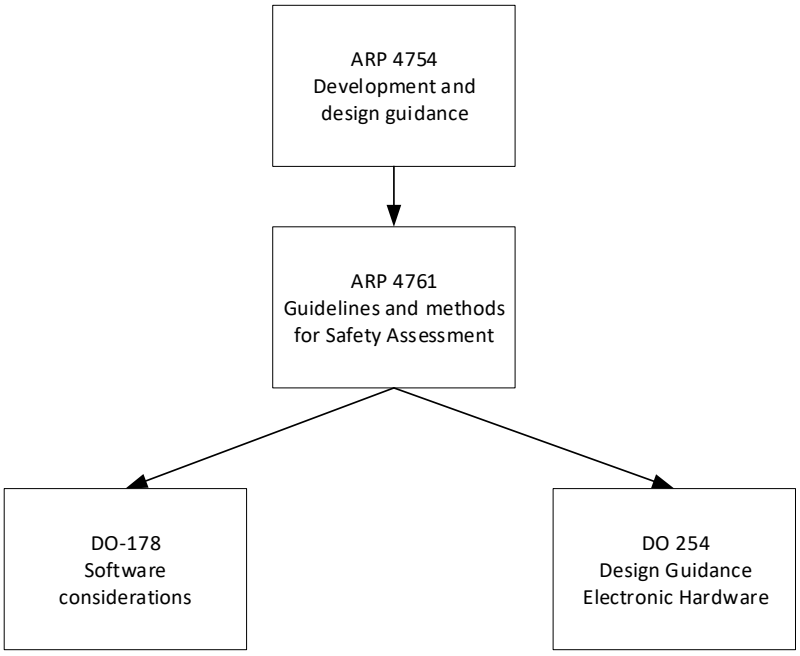


Figure 1.2: Development process

In Aerospace, the design will have to meet a certain Delopment Assurance Level (DAL) due to the criticality of the functions. For example, a landing gear in aerospace

would have a DAL of level A which means that the probability of failure must be below 1e-9 per flight hour [28]. This means that failures must be extremely improbable and such a failure could be catastrophic to human lives. Table 1.1 demonstrates the DAL level from [28].

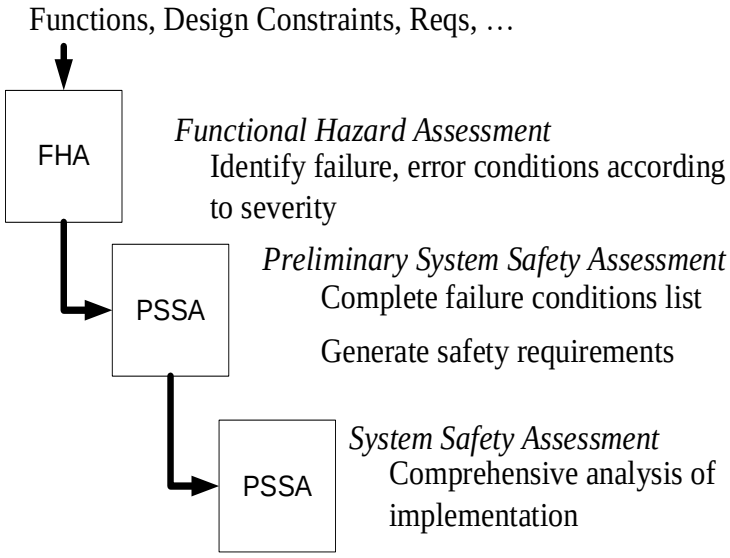


Figure 1.3: Safety Assessment Elements

Table 1.1: Development Assurance Level (DAL)

	Per flight hour				
Probability (quantitative)	1.0	1.0E-3	1.0E-5	1.0E-7	1.0E-9
Probability (Descriptive)	Frequent	Reasonably Probable	Remote	Extremely Remote	Extremely Improbable
Failure Condition	Minor		Major	Severe Major	Catastrophic
Severity Classification	Minor		Major	Hazardous	Catastrophic
Failure Cond. Effect	1. slight reduction in safety margins 2. slight increase in crew workload 3. some inconvenience to the occupants		significant reduction in safety margins or functional capabilities	large reduction in safety margins or functional capabilities	all failure conditions which prevent continued safe flight
Development Assurance Level	Level D		Level C	Level B	Level A

1.2.2 Safety Analysis

To ensure that the system is safe, a safety analysis is formalized at each level of the product development process by the following activities:

1. FHA: Identification of the complete list of Minor, Major, Hazardous or Catastrophic failure conditions which are in relation with the functional behavior of the system under study.

2. PSSA: Verification that the preliminary system architecture is able to meet the objectives associated with failure conditions. The PSA should determine the safety requirements (including development assurance level) to be imposed on each equipment

3. FTA: Deductive failure analysis which focuses on one particular undesired event. Quantitative evaluation of uniquely undesirable event and their combination

4. FMEA: Method of identifying the failure modes of an equipment to determine the effects on the next higher level of the design.

   (a) Functional FMEA: of the failure modes induced by the failure of an elemental group.

   (b) Component FMEA: evaluation, for each component, of the failure mode produced by the defect of a component. A probability is assigned to each failure mode.

5. SSA: To show that safety requirements are met. Assessment of each elementary failure

6. CCA: Evaluation of the generic faults and the hardware "upsets" that could cause malfunctions in multiple items.

A flow chart of this safety analysis is shown in Fig.1.4.

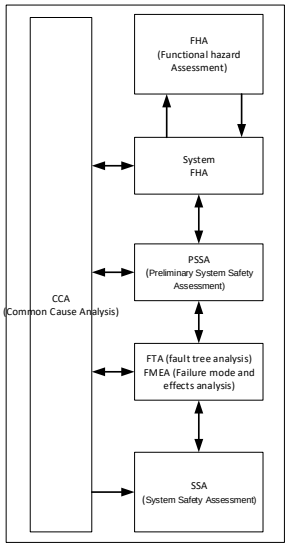


Figure 1.4: Safety analysis

1.2.3 System Design Process

The purpose of the system development is to identify the structure and the configuration of the entire system. ARP-4754 is the main guideline to carry on this activity in line with the certification objectives. The SW and HW components are identified including operational needs, environment and safety. The system development will interact in a bidirectional way with the HW and SW development.

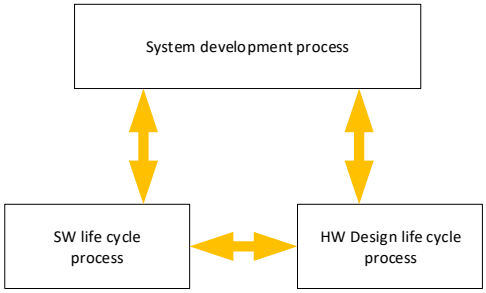


Figure 1.5: System design process

1.2.4 Design Process

The main rule to follow during design processes is that a structured design approach to the system, will likely lead to a safe development and safe design. This is because in a structured approach, the phases of the design are clearly defined before the design starts. Requirements are captured for the needs of the design and the na verification and validation process against the requirements are performed. Fig.1.6 demonstrates a flow chart of such design.

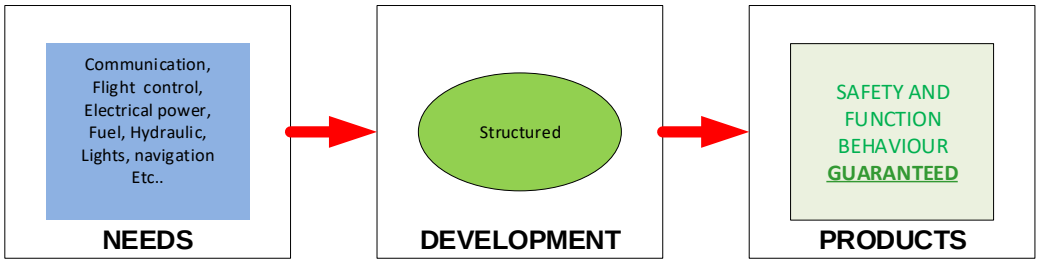


Figure 1.6: Design process basic rules

Both the design and safety analysis are performed in parallel. This is to ensure that although safety is met, the design does not take millions of years to do. An iterative process is performed to capture the additional requiremetns during the development process. This is shown in Fig.1.7.

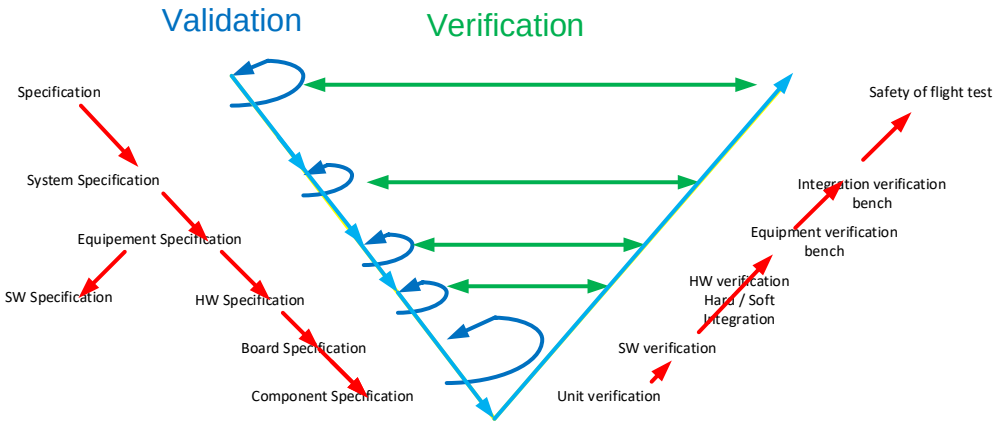


Figure 1.7: Requirement based engineering

The basic rules to requirement based engineering are as follows:

1. Capture the requirement which define the need of the product

2. Verification of the product against the requirement

1.2.5 Hardware Design Life Cycle

The hardware design life cycle offers guidelines to different important processes in the design process of the system throughout production. These processes are needed for hardware certification according to RTCA DO-254. The guideline objectives are to assist in developing fail-safe reliable hardware. The hardware design life cycle is

divided into different key processes, each with its own objectives. Changes made in one process must be iterated into all other processes to assure that a modification in one does not affect objectives in the other and vice versa.

DO-254 breaks the hardware design life cycle down into five separate steps. Fig.1.8 shows how the different processes in the hardware design lifecycle interact.

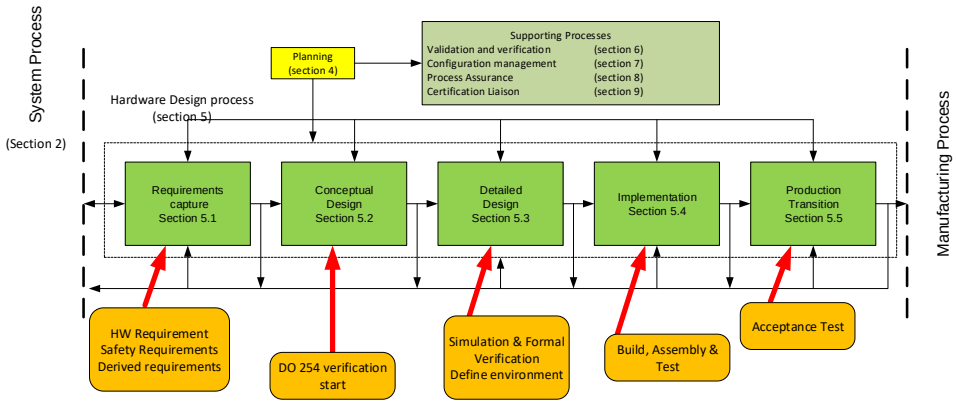


Figure 1.8: HW design cycle

The "design assurance" activities applied at different parts of the flow fall into the following three categories:

1. Review: a manual process of reading code or examining documentation (block diagrams, schematics, etc.) to determine correctness.

2. Analysis: a partially/fully-automated process in which software tools are applied to examine the functionality, performance and/or safety implications of a hardware item and its relationship to other functions to provide evidence that a requirement is correctly implemented.

3. Test: a manual or automated process to confirm that the hardware item correctly responds to stimuli in its intended operational environment.

This is a very rigorous process to ensure taht safety requirements are met based on the system's interaction with the world. Large teams of many companies collaborate on a single system to ensure not only safety is met but this process does not take an infinite amount of time or infinite amount of money [22].

1.2.6 DO 254 Overview

The FPGA technology is extremely flexible in terms of programmability. An Automotive or Aerospace application, where product requirements change quite vastly and quickly, would receive a lot of benefits from using this technology. This flexibility without rules may lead to complex designs, hard to design or verify, which lack robustness, are not deterministic, or designers may attempt building structures which are not supporting PLD technologies. Moreover, the different tools used during the design of a PLD (synthesis, place-and-route, Static-Timing-Analysis (STA) and Simulations) needs that good practice rules are respected in order to ensure an optimum use of the design tools and the FPGA technology. An example of such tools are Modelsim for simulation [31], Synplify for synthesis [32] and VIVADO for the whole process [33].

Due to the current size of FPGAs, the complexity of implemented algorithms and the time length of a project, it is required to use a system of consistent rules, such as in software, to ensure the code readability and maintainability, but also to anticipate on the behavior of simulation and synthesis tools, and also to allow the porting to other technologies. This is why the HW design process is needed to set

number of rules and methodologies to ensure a safe implementation of the design. The HW design process produce a Hardware Requirement (HWQ) item that fulfills the requirements allocated to HW from system requirements. The DO-254 standard can be separated into the following activities:

1. Planning - DO-254 Section 4
2. Requirements Capture - DO-254 Section 5.1
3. Conceptual Design - DO-254 Section 5.2
4. Detailed Design - DO-254 Section 5.3
5. Implementation - DO-254 Section 5.4
6. Production Transition - DO-254 Section 5.5

There are three main objectives for the Planning process described in the DO-254 Section 4 [29]. The three main objectives are:

- To define the means to produce the HW items
- To satisfy system requirements
- To satisfy certification requirements

The planning process objective is to control the conversion of the documented functionality specifications and security specifications for the airborne system into a developed hardware with appropriate design assurance so that the hardware performs its intended functions without any anomalous behavior. The planning process

includes choices and definitions of standards as well as choosing the design environment for system development and testing.

The objective of the requirements capture process described in the DO-254 Section 5.1 is as follows:

- Hardware requirements are identified, defined and documented in accordance with the requirements from the system.
- HW specification contains.
  - High level requirements are allocated to the HW.
- Derived requirements which are produced during the design activities.

The specifications include the requirements derived from the Preliminary System Safety Assessments (PSSA) which means that in the proposed system architecture, consideration is taken according to the System Development Assurance Level of the design. A testability strategy is also defined so that the design can be tested at each step to verify consistency between the system design and the system specification.

After the requirements have been captured, the conceptual design on a high system level is produced so that an assessment of the possibility of verifying that the developed systems design corresponds with the derived system requirements can be performed. A conceptual design can be made using functional block diagrams or architecture descriptions.

Once a functional block diagram or an architecture is conceived, the detailed design step would start. This step is to assure that the objectives derived from the system requirements and hardware specifications can be met in the system design

on a low level of the design. For example, if the system is based on an FPGA the detailed design can be written in VHDL code. The constructions of test benches for system and safety verification are also made in the detailed design.

The detailed design will then be subject to a process of implementation onto the desired Unit Under Test (UUT). The implementation process objectives are to develop manufacturing processes so that production of the hardware from the detailed design is possible. During this stage all data needed for implementation, assembly and installation are produced and the product can finally transition to a production process. The objectives for the product transition are to establish baselines containing complete design and assembly data to be able to start consistent hardware manufacturing. Production control focuses on safety requirements which should be established and documented during this process.

Once the design process of the UUT has been appropriately planned with a detailed design, the verification and validation process start (Section 6 of the DO-254) [29]. The verification process objective is to ensure that the implemented hardware is compliant with the hardware requirements of the detailed design. A traceability control is performed to make sure it is chronologically possible to follow the development process and the modifications made to the system. Furthermore, a control is done to verify that it is possible to implement the test criteria and that the test criteria are thorough enough depending on the system development assurance level. The objectives of the validation process is to ensure that the final requirements in the derived hardware specification are met by the original system requirements according to functionality and safety. The validation process is performed using analysis, tests and reviews.

Once the system has been verified and validated against the detailed design, the artifacts of data need to be configured in a matter such that if any of the above processes or design changes, traceability of the changes can be re-produced. Thus, a configuration process would follow a validation and verification process with a configuration management tool. This tool is to maintain control of different versions of designs, hardware, test benches and documentation developed during the hardware design life cycle. The objective with the configuration management is to identify and document each version of the different parts of the hardware design life cycle so that the traceability never risks being compromised. Such configuration management tools are IBMs DOORs [34] or even a simple github [35].

The process assurance manages the documentation of all progress and modifications made during the system development. Its objective is to make sure that traceability between the interactions of the different steps during the development process is documented and that the derived hardware complies with the approved plans. All deviations from the original hardware plans must be detected, evaluated and approved.

1.2.7 Safety-Critical Verification according to the DO-254

The product requirements are really the heart of the whole process. The validation of requirements is still essentially a manual review process. The goal is to correlate the verification activities against those requirements. Most verification is done in the detailed design step, mostly on the Register-Transfer-Level (RTL) design but also including the gate-level simulation and lab testing. The way to improve safety-critical verification is to apply this methodology with automation as much as possible while

having a clear traceability of every piece of the design to a set of tests and back to the initial requirements so that we can continuously monitor our progress throughout the process.

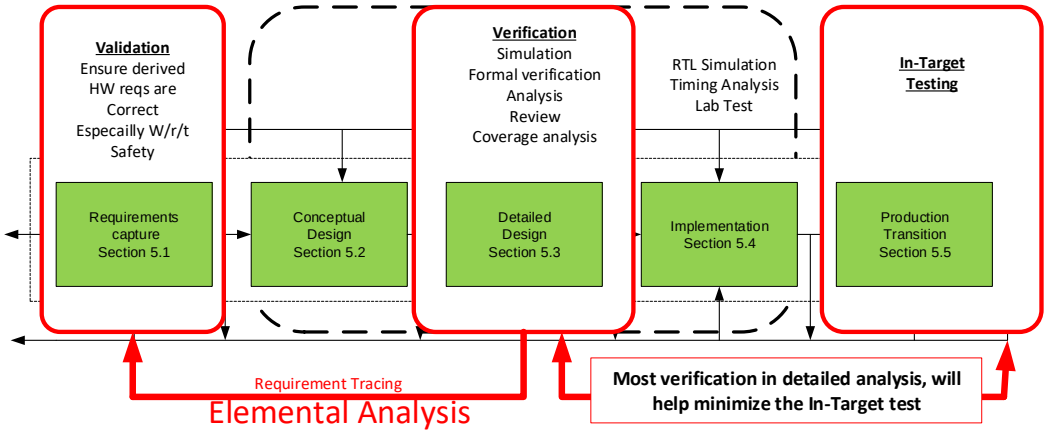


Figure 1.9: Safety critical verification in DO 254

In this project, a fully automated test bench is designed, with a built-in self-test capability that will be used for testing CEH developed in an aeronautic environment. The automated test bench is developed in order to achieve the functional verification of a complex electronic hardware (CEH), such as an FPGA, that was designed for an aerospace application. This test also needs to be integrated in the verification process in line with the objectives of DO-254 DAL A as shown in Fig.1.9.

The newly developed system allows for the optimization of the required time to execute and analyze the tests and it minimizes the risks of mistakes when reporting the verification results. This approach provides better integrity of results and analysis and ensures, at a lower cost, the non regression of the FPGA after the various specification

modifications that are typical in such projects.

1.3 Research Objective and Scope

The aim of this project is to design and prototype an ECU to be used as a universal data acquisition and controller for power control in the automotive/aerospace application. This ECU will be applied to the MSI-HESS system as an energy management controller. The ECU is a computer-based electronic module intended to be used for automotive and aerospace controllers. The ECU acquires and monitors system parameters, executes system fault detection and isolation, and communicates with the vehicle (aircraft/automotive). The ECU includes two main sub-modules; (i) a digital core based on MPC5777 microprocessor and, (ii) a fast data acquisition and control (FDAC) system based on field programmable gate array (FPGA). ECU micro-processing module, Ethernet network switch, and digitized analog I/O processed in an FPGA for aerospace application will make this technology usable by automotive application for fast and efficient superviory controls capable of handling multiple tasks and complex multi physics control strategies. The contributions made as a result of this research include:

- The selection of the Embedded Controllers to support the supervisory functions of the ECU based on automotive performance and cost and aerospace safety standards.
- The development of a universal supervisory power electronics control board that adheres to parts of the following avionic development standards:
  - DO-254: Design assurance guidance for airborne electronice hardware.

  - DO-160: Environmental conditions and test procedures for airborne equipment.

- The development of an optimized supervisory energy management system for the HESS-MSI system in MATLAB/Simulink as outlined in [36].
- An automated verification process for FPGA development with a Design Assurance Level-A.
- An automated verification test bench for FPGA development.

Chapter 2

Hybrid Energy Storage Systems (HESS) in Electrified Vehicles

Present-day Electric Vehicles (EV) use Li-ion Batteries as the main source of energy to supply electrical loads within the vehicle due to its high energy density [37]. Electrical loads, such as the electric motor, experiences highly dynamic power demand profiles due to the unpredictable driving trends of the vehicle drivers. During high acceleration and braking, the battery experiences large current magnitudes and fluctuations which has been found to cause an increase in the internal resistance of the Li-ion battery thus increasing the battery wear over its lifespan [37, 38]. Due to the highly dynamic power demands of the electric motor, batteries are over-sized accordingly to meet all power demands while minimizing the internal resistance increase during the vehicles dynamic power demands [37,38]. Another source of energy that is used in commercial vehicles, such as Mazda's 6 series sedan and in-city transit busses are the UltraCapacitors (UC) due to their high power density [39]. They are mainly

used for start-stop systems and regenerative braking to store the quick burst of energy [40]. The main disadvantage of UCs is that they cannot store a large amount of energy like Li-ion Batteries thus are not used as a main energy source.

By introducing a Hybrid Energy Storage System (HESS), the benefits of two energy sources can be exploited [37, 38, 41]. By combining a Li-ion Battery with a UC, the UC's high power density along with the high energy density of the Li-ion Battery can be used simultaneously. This enables the UC to handle high dynamic demands while the battery would handle the constant and low power demands.

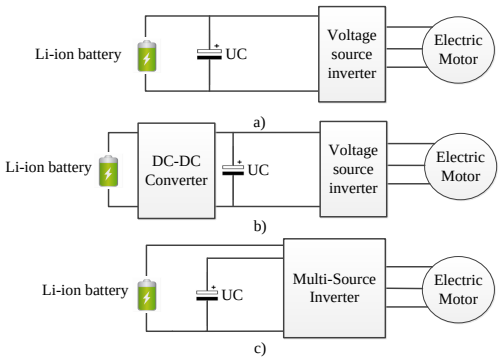


Figure 2.1: Different HESS Li-ion battery and UC topologies. a) Passive parallel HESS b) Battery-UC active HESS c) HESS using MSI.

HESS topologies range from being passive systems or more dynamic active systems where power converters and controllers are used to improve performance. Passive parallel topologies, as in Fig.2.1-a, offer battery current peak reduction compared to battery only energy storage systems due to the use of an UC acting like a low pass filter to the battery [38]. The disadvantage of this topology is that the UC's voltage is locked at the battery voltage and therefore the UC's full capabilities are not used as well as having the battery directly connected to the inverter causing

battery wear [42–44]. Conventional active HESS topologies offer better performance by enabling the control of the charge and discharge rate of the battery and UC through a power converter [38]. A common active HESS topology used is the Battery-UC active topology shown in Fig.2.1-b. Although active HESS topologies offer the control over the current distribution of both DC sources, they tend to be much larger, costly and more expensive than the passive HESS topology due to the added DC/DC power electronics converter thus limiting their use in industrial applications [41].

Chapter 3

Embedded Controllers in Electrified Vehicles and Aircrafts

3.1 Requirements

The Supervisory Universal Power Electronics Control Board is divided into two main components such as the Digital Core and the Fast Data Acquisition and Control System (FDAC). The digital core will handle the safety critical tasks such as monitoring and fualt logging while the FDAC will handle the tasks to acquire data of the system and its surroundings along with controlling the system behavior.

The Digital Core of the Universal Power Electronics Control Board **shall** have the following features:

1. A reliable and robust microprocessor
2. Multi-Core architecture
3. Non volatile memories (NAND and NOR Flash)

4. Serial line interface

5. SPI buses

6. External user I/O

The fast data acquisition and control system based on a low-cost, high performance FPGA **shall** have the following features:

1. Analog to digital converter

2. Embedded Digital Signal Processing math blocks

3. 1Gb/s Ethernet capabilities

4. Multiple I/Os

3.2 MicroProcessor Units

3.2.1 ARM-Based Processors

The Advanced RISC Machine (ARM) processor (originally known as Acron RISC Machine) was the outcome of a project within Acorn's Advanced Research and Development section with first samples delivered in 1985 [45]. ARM is a Reduced Instruction Set Computing (RISC) processor architecture that is currently developed by the ARM Holdings plc and licenced to other companies [46, 47]. ARM Holdings plc by licensing the architecture instead of manufacturing the actual chip opened up new business model for the industry [48]. Basics of ARM processors are RISC technology and concept. Unlike Complex Instruction Set Computing (CISC) the RISC

is based on simplified instruction sets providing higher performance when combined with microprocessor architecture capable of executing instructions in fewer microprocessor cycles per instruction [49]. ARM-based processors are simple in structure and compared to general-purpose microprocessors have relatively small number of transistors hence allowing other modules to be included on the chip. Therefore, due to its modular design an ARM processor may consist of mandatory pipelines, cashes, Memory Management Unit (MMU), floating point and co-processors. This gives flexibility in developing application-specific ARM processors. The ARM processors and their pipeline are designed for minimized energy consumption suitable for embedded systems, small in size, low power while providing high performance [47]. The ARM processors usually use variable execution time, subword parallelism, digital signal processor-like operations, thread-level parallelism and exception handling, and multiprocessing which these make ARM-based processors efficient with high performance capability [48]. ARM has load-store architecture i.e. the ARM processor first loads the data to one of the general-purpose registers before processing it. Therefore, instructions in the ARM Instruction Set Architecture (ISA) load and store multiple registers with variable cycles to execute compared to loading and storing each register individually in RISC systems. This therefore improves code density, reduces instruction fetches, and reduces overall power consumption [48].

ARM Holdings plc currently develops three different profiles for the ARM architecture namely ARM Cortex-A (Application Profile), ARM Cortex-R (Real-time Profile) and ARM Cortex-M (Microcontroller Profile) [46], [50]. Fig.3.1 shows some application examples for ARM-x Cortex profiles.

Figure 3.1: ARM Cortex application examples.

ARM Cortex-A processors are capable of undertaking complex computing tasks such as hosting a rich platform for Operating System (OS) and supporting multiple software applications [51]. ARM Cortex-A processors provide highest performance at low power; they have MMU support and they are used in ranges of applications such as smartphones, digital TVs, mobile computing platforms, Internet of Things (IoT) devices, networking, server solutions etc.

Popular Cortex-A processors deliver an optimal efficient performance and are designed to tackle complex functions like the ones required by smartphones. Their fast response with low-power architecture has attracted many applications. Cortex-A processors provide support for extensions including [51, 52]:

- Full OS's including Linux.
- Systems requiring MMU such as Android, Chrome, MontaVista etc.
- Single Instruction Multiple Data (SIMD) technology.
- Advanced SIMD (NEON) technology: NEON is ARM general-purpose SIMD engine that efficiently processes current and future multimedia formats, enhancing the user experience.
- Thumb ISA, Thumb-2: Thumb is a 16-bit instruction set which is a condensed version of ARM ISA that allows higher code density at a slight performance cost [48], [53]. Thumb-2 technology is a further extension to code density which mixes the 32- and 16-bit instructions in the same instruction stream to increases the code density.
- Enhanced Digital Signal Processing (DSP) instructions: This supports flexible and fast 16 $\times$ 16 multiply and arithmetic saturation on top of standard ISA.
- Advanced single and double-precision Floating Point support (VFP): VFP Applications include [54]:
  - Automotive control applications: Powertrain, ABS, Traction control & active suspension.
  - 3D Graphics: Digital consumer products, Set-top boxes, games consoles.
  - Imaging: Laser printers, still digital cameras, digital video cameras.
  - Industrial control systems: Motion controls.

- Virtualization: Enable the efficient implementation of virtual machine hypervisors.
- Large Physical Address Extension (LPAE) addressing up to 1TB of physical memory.
- big.LITTLE processing.
- Jazelle: An ARM technology for acceleration of execution environments such as Java, Python and Microsoft .NET Compact Framework.
- TrustZone: An ARM technology that is a System-on-Chip (SoC) and CPU system-wide approach to security.
- Coprocessors: Each Cortex-A series processor contains 16 internal coprocessors. These coprocessors handle a variety of tasks such as system control, debugging, and VFP operations.
- Multicore Technology: All the ARMv7-A and ARMv8-A processors support ARM's multicore technologies. The multicore technology includes:
  - Single to quad-core implementation for performance orientated applications.
  - It supports symmetric and asymmetric OS implementations.
  - Coherency throughout the processor exported to system via Accelerator Coherency Port (ACP).

Table A.1 lists different AMR Cortex-A architectures. Cortex-A5, Cortex-A7, Cortex-A8 have the same clock speed of 1 GHz while the clock of Cortex-A9 is 2

GHz. The clock speed for other architectures varies as seen from Table A.1 with Cortex-A73 having highest value i.e. 2.8 GHz. However, when comparing microprocessors the number of operations that the processor can do in each clock cycle is an important parameter. One such method of benchmarking processors is Dhrystone and is representative of system (integer) programming [55]. The Dhrystone benchmark counts how many times the Dhrystone code can be run a second and then divides that result by 1757 [55]. Dhrystone benchmarking usually gives the metric as either Dhrystone million instructions per second (DMIPS) or Dhrystone million instructions per second per megahertz (DMIPS/MHz) [55]. As seen from Table A.1 the DMIPS/MHz for Cortex-A5, Cortex-A7, Cortex-A8 and Cortex-A9 are 1.6, 1.9, 2 and 2.5 respectively. The DMIPS/MHz varies for different architectures with a trend of increase for newer versions.

As seen from Table A.1 the execution order for Cortex-A processors is either in-order or out-of-order. If a processor has out-of-order execution then they can continue with other instructions while waiting for a stalled instruction to complete [52]. The Cortex-A8 and Cortex-A9 architectures have vector floating point VFPv3 while other Cortex-A architectures offer VFPv4. As listed in table A.1 the interconnect varies for different Cortex-A architectures. Cortex-A processors use advanced microcontroller bus architecture (AMBA) as interconnect. These AMBA's have multiple different versions [56] as follows:

- Coherent Hub Interface (CHI) – Highest performance
- Advanced eXtensible Interface (AXI) – Widespread AMBA used for connectivity of 100's of masters and slaves
- AXI Coherency Extensions (ACE) – Used in ARM's big.LITTLE system

- Advanced High-performance Bus (AHB) – Main system bus in microcontroller usage
- Advanced Peripheral Bus (APB) – Minimal gate count for peripherals
- Advanced Trace Bus (ATB) For moving trace data

All Cortex-A architectures offer L1 data and instruction cash while L2 cash is not available for Cortex-A5 and Cortex-A9.

For ARMv7 family of Cortex-A processors when looking at pure performance the Cortex-A17 is the winner; this is to be expected as it is the newest ARMv7 high performance processor. However, if cost and power-efficiency are of interest the Cortex-A5, Cortex-A7, Cortex-A8 and Cortex-A9 are the processors to be examined more closely. The Cortex-A9 has the highest performance but the Cortex-A7 is 80% more power efficient. In fact, if two Cortex-A7 processors are used in multicore operation they have more performance and still have better power efficiency. Between the Cortex-A5 and Cortex-A7, the Cortex-A7 has more performance at an increase of power but it also supports more options in its ISA.

ARM Cortex-R processors offer high-performance computing and deliver fast deterministic processing for systems where reliability, high availability, fault tolerance and maintainability and real-time responses are needed [57]. Through proven technology ARM Cortex-R processors provide fast time-to-market. Cortex-R processors offer performance, power and area optimized package for systems needing high error-resistance. Cortex-R processors are popular in embedded and real-time applications where high-performance and cost-effective real-time processing is demanded such as automotive safety, storage and wireless baseband. Cortex-R processors feature [57]:

- High performance: Fast execution of complex code and DSP functionality.
  - High performance, high clock-frequency.
  - Dual-core multi-processing configurations - Asymmetric Multi-Processing (AMP) and Symmetric Multi-Processing (SMP).
  - Hardware SIMD instructions for very high performance DSP and media functions.
- Real-time: Deterministic operation to ensure responsiveness and high throughput.
  - Fast, bounded and deterministic interrupt response.
  - Tightly Coupled Memories (TCM) local to the processor for fast-responding code/data.
  - Low-Latency Interrupt Mode (LLIM) to accelerate interrupt entry.
- Reliable: Detects errors and maintains system operation.
  - User and privileged software operating modes with Memory Protection Unit (MPU).
  - ECC and parity error detection/correction for Level-1 memory system and buses.
  - Dual-Core Lock-Step (DCLS) redundant core configurations.
- Cost effective: Fast time-to-market and customizable features.
  - Best-in-class energy and die area/cost efficiency.

  - Configuration to include/exclude features to optimize power, performance and area.
  - Fast development and testing with configurable debug breakpoints and watchpoints through CoreSight^{TM} debug access port with embedded trace module options.

Table A.2 shows a comparison of all of the ARM Cortex-R series processors. As previously mentioned the Cortex-R4 and Cortex-R5 are focused more on efficiency and thus do not have all of the features that Cortex-R7 and Cortex-R8 such as a branch target address cache (BTAC). The purpose of BTAC is to help speed up dynamic branch prediction by storing information about previous branch executions. The major difference between the Cortex-R4 and Cortex-R5 is that the Cortex-R5 can be two cores as long as it is in AMP mode [58]. Clock speed of Cortex-R4 and Cortex-R5 is 600 MHz lower than 1 GHz for Cortex-R7. However, all of the Cortex-R architectures have same DMIPS/MHz of around 2.5, use VFPv3 vector floating point and have 64-bit AMBA interface.

The Cortex-M family offers a low cost and energy efficient solution processor suitable for applications such as IoT, connectivity, motor control, smart metering, human interface devices, automotive and industrial control systems, domestic household appliances, consumer products and medical instrumentation [59]. Cortex-M processors are most popular in embedded system applications and feature [59]:

- Energy efficiency achieved via:
  - Power efficient 32-bit processors.
  - Support for sleep modes.

  - Low power design with further optimization packs available.
  - Low power consumption enables longer battery life.

- High performance through:
  - Leading Microcontroller Unit (MCU) performance.
  - Instructions for bit manipulation.
  - Low interrupt latency.
  - Powerful DSP extensions and optional hardware Floating Point Unit.

- Ease of use including:
  - Program in C/C++.
  - Standardize software framework (Cortex-M Software Interface Standard).
  - Free DSP library.

- Reduced system size achieved by:
  - Low gate count.
  - High code density reduces memory size.
  - Small area (which reduces die cost and package size).

- Other features including:
  - Interrupt control via Nested Vectored Interrupt Controller (NVIC).
  - OS support features.
  - MPU.

– Comprehensive debug and reliability features.

Table A.3 shows comparison of Cortex-M series processors. Note that the Cortex-M0 and Cortex-M0+ both only support a subset of the Thumb/Thumb 2 architecture which means that they do not support every instruction that the other Cortex-M processors do. In addition, the Cortex-M0 does not have a memory protection unit. The memory protection unit supports access permission and 8 or 16 protection regions [60].

3.3 Field-Programmable-Gate-Arrays

The Field-Programmable Gate Array (FPGA) concept was first introduced by Ross Freeman, in 1984 [61]. FPGAs are digital Integrated Circuits (ICs) that consist of logic blocks and interconnections that can be programmed to do a wide array of functions. Each FPGA usually contains a large number of elements called Configurable Logic Blocks (CLBs) or Logic Array Blocks (LABs). Each logic block can be further broken into smaller blocks such as an Adaptive Logic Module (ALM), Logic Element (LE) or Logic Cell (LC) [62]. The smaller logic blocks are different in composition but all share basic components such as Look-Up Tables (LUTs), Multiplexers (MUXs), Flip-Flops (FFs), and carry logic or full adders [62]. Carry-logic and full-adders are logic that allow for addition and subtraction of bits [63]. Fig.3.2 shows a simplified architecture for ALM, LE and LC.

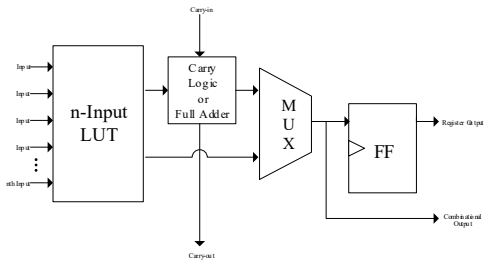


Figure 3.2: Typical simplified architecture for ALM, LE and LC

The hierarchical approach to logic blocks allows each small module (i.e. LE, ALM or LC) to share a local LAB / CLB interconnect and access to the larger FPGA interconnect []. In addition, FPGAs usually contain components such as I/O blocks, PLLs, ADCs, DACs, dedicated DSP blocks, embedded memory, and soft or hard microprocessors [64]. A soft processor is a processor implemented within the device's logic while a hard processor is an embedded processor within the device. The combination of these components, the flexible nature of the FPGA architecture, and the consistently increasing library of Intellectual Property (IP) modules ensures that FPGAs can handle a wide variety of tasks. Due to the reprogrammable nature of FPGAs are advantageous over their fixed counterpart i.e. the Application-Specific Integrated Circuit (ASIC). An ASIC is an integrated circuit that is designed either from the ground-up or using specific logic libraries for a specific task [65]. These benefits include significantly less Non-Recurring Expense (NRE), a simpler design cycle, faster time-to-market and the ability to modify the device at any stage of its life-cycle, including when it is being used by an end-user [66,67]. The ability to modify the device in the field is particularly attractive as it offers a way of at least partially

avoiding obsolescence as the FPGA can be updated to include new functionality and remove obsolete modules [68].

3.3.1 SRAM and Flash Based Architecture

Most modern FPGAs are usually based on Static Random-Access Memory (SRAM), however some use flash memory [63,69]. These memory cells are programed whenever the device is configured. An n-input LUT can implement any logic function that requires up to n-inputs. Fig.3.3 shows a 2-input FPGA LUT consisting of memory cells and MUX's.

SRAM based FPGAs are volatile and thus every time they lose power they need to reconfigure these cells using information from an external non-volatile memory. Flash based FPGAs on the other hand are non-volatile thus keep their configuration when powered down. Flash memory has an advantage over SRAM memory is that flash memory is more resistant to single event upsets (SEUs). However, as flash memory has a limited number of writes that can be used to reprogram it.

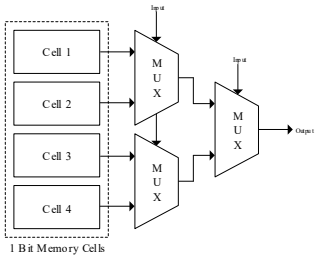


Figure 3.3: A 2-input LUT

3.3.2 Single Event Upsets

In logic systems, events called Single Event Effects (SEE) can occur as a result of cosmic rays or high energy particles. These SEEs can take many different forms, such as SEUs and Single Event Latch-ups (SELs) [70]. SEUs can either flip bits in memory or registers as well as create transient pulses that propagate through the system while SELs cause higher than safe operating currents [70]. SEUs become a major concern for safety-critical systems such as avionics and for this reason they are heavily considered when selecting a device [69]. There are techniques to detect and mitigate SEUs but they come at an additional cost [69]. One such technique is Triple-Module Redundancy (TMR) which is when the component is triplicated and whichever output occurs at least two of the three is used as the final output [71]. This is obviously resource intensive as everything critical needs to be made three times instead of once and majority-detecting logic also needs to be added. SEU problems become more and more prevalent as capacitance on the switch decreases and the voltage and cell size decrease [72]. SEUs are a safety concern when they occur in the logic but can be especially dangerous when they cause changes in the configuration memory of the FPGA [72].

From the requirements of the FPGA, only Xilinx and Microsemi were considered due to microsemi's flash based, SEU immune technology and due to Xilinx's DSP functions and SEU immunity through ECCs. Other FPGA vendors such as Altera Corporation (now part of Intel), Lattice Semiconductor Corporation, Atmel Corporation, QuickLogic Corporation and Achronix Semiconductor Corporation are not considered. Although a comparison of Cyclone V FPGA from Alera has been studied to ensure completeness of the FPGA choice.

3.3.3 Xilinx FPGAs

Xilinx offers a wide range of FPGA families that address varying needs ranging from high capacity performance intensive networking to small footprint FPGAs [1]. The Xilinx FPGA families and their general purposes are listed in Fig.3.4.

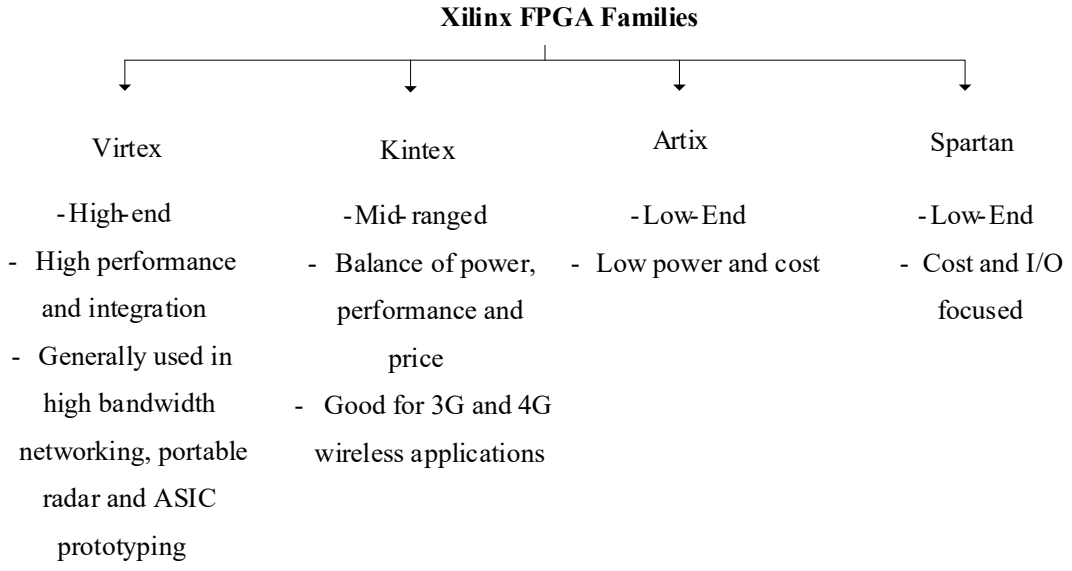


Figure 3.4: Xilinx FPGA Families

The Xilinx four families are offered at different technology nodes as listed in Fig.3.5. Of these four families the Spartan-6 and Artix-7 families are the best choice for the project as the Virtex and Kintex families are focused more on higher performance than power and cost efficiency.

Figure 3.5: Xilinx Multinode Product Profile [1]

Xilinx SEU Mitigation

Xilinx devices are designed to have low susceptibility to SEUs as well as allow a full recovery one occurring [73]. Xilinx's SEU Failures in Time (FIT) rate decreases from node to node [73]. Xilinx devices also use Ultra-Low Alpha (ULA) materials and offer free IP such as the Soft Error Mitigation (SEM) core to help manage SEUs [73].

The SEM core is available on all UltraScale, UltraScale+, series 7 and Spartan-6 FPGAs [74]. The SEM detects errors in configuration memory and allows for their correction [74]. The SEM module also allows for the emulation of SEUs to provide a way of testing a device's resistance without having to send it to a radiations effects facility [74].

Another feature that is offered by Xilinx is the Isolation Design Flow. Isolation Design Flow provides fault containment and logic segregation [73]. The EDA tools can be configured to not optimize away redundant modules that are used for safety such as a TMR component [73].

Xilinx releases a semi-annual "Device Reliability Report" that includes FIT rates and other safety test results for each device and offers a SEU FIT rate estimator on

their website (for approved registered members) [75, 76].

Spartan-6

The Spartan family is Xilinx's FPGA with the lowest total cost, for high-volume applications. For any comparison of FPGA devices it would be impractical to list every separate device that could possibly be ordered. The reason for this is the sheer number of different devices that could potentially be ordered from each manufacturer. The ordering information can be found in [77].

Since there are 13 different Spartan-6 device types, there are ∼208 (13 x 4 x 1 x 2 x 1 x 2) devices assuming there is only one package type and one number of pins (this is not the case for either of these options). Hence, each device type is broken down into each of its operating temperature ranges as in []. From there each section lists the minimum and maximum pin count as well as the minimum and maximum unit price. It should also be mentioned that all of the unit prices are taken from Digikey.com as it is a common distributer for all of the manufacturers.

All of the Spartan-6 devices have a maximum internal clock tree of 400 MHz. Most of them also have three operating temperature ranges (0°C ∼ 85°C (TJ), 0°C ∼ 100°C (TJ) and -40°C ∼ 125°C (TJ)) while a couple only have two (0°C ∼ 85°C (TJ) and 0°C ∼ 100°C (TJ)).

For the Spartan-6 devices as the amount of Logic Cells increases so does the number of embedded math blocks. Each math block in the Spartan-6 devices contain an 18 x 18 multiplier, an adder and an accumulator [77]. The devices without high-speed interfaces can be eliminated since it is an important parameter for this project. The remaining FPGAs all end with T. From this the 6SLX45T is a suitable option

Device	LCs/LEs/ALMs (k)	Max Internal Clock	Math blocks	Memory (Max Block RAM (Kb))	Memory Controller Blocks	Clock Resources	Min Pins	Max Pins	Operating Temperatures	Min Approx. Price (US$)	Max Approx. Price (US$)
6SLX4	3.384	400 MHz	8	216	0	2 PLLs 4 DCMs	102	132	0°C ~ 85°C (TJ)	11.48	15.19
									0°C ~ 100°C (TJ)	13.23	26.11
							132		-40°C ~ 125°C (TJ)	26.53	29.19
6SLX9	9.152	400 MHz	16	576	2 x DDR,DDR2,DDR3,LPDDR	2 PLLs 4 DCMs	102	200	0°C ~ 85°C (TJ)	16.52	25.13
									0°C ~ 100°C (TJ)	18.97	33.39
							160		-40°C ~ 125°C (TJ)	29.54	37.38
6SLX16	14.579	400 MHz	32	576	2 x DDR,DDR2,DDR3,LPDDR	2 PLLs 4 DCMs	106	232	0°C ~ 85°C (TJ)	23.45	33.81
									0°C ~ 100°C (TJ)	26.95	39.27
							160		-40°C ~ 125°C (TJ)	34.79	44.03
6SLX25	24.051	400 MHz	38	936	2 x DDR,DDR2,DDR3,LPDDR	2 PLLs 4 DCMs	186	266	0°C ~ 85°C (TJ)	34.02	54.81
									0°C ~ 100°C (TJ)	39.13	67.55
									-40°C ~ 125°C (TJ)	52.01	75.67
6SLX45	43.661	400 MHz	58	2088	2 x DDR,DDR2,DDR3,LPDDR	4 PLLs 8 DCMs	218	358	0°C ~ 85°C (TJ)	54.74	83.23
									0°C ~ 100°C (TJ)	62.93	95.76
								320	-40°C ~ 125°C (TJ)	76.16	98.28
6SLX75	74.637	400 MHz	132	3096	4 x DDR,DDR2,DDR3,LPDDR	6 PLLs 12 DCMs	280	408	0°C ~ 85°C (TJ)	99.54	131.67
									0°C ~ 100°C (TJ)	114.52	135
								328	-40°C ~ 125°C (TJ)	127.5	132.51
6SLX100	101.261	400 MHz	180	4824	4 x DDR,DDR2,DDR3,LPDDR	6 PLLs 12 DCMs	326	480	0°C ~ 85°C (TJ)	124.04	146.25
									0°C ~ 100°C (TJ)	127.5	168.75
								326	-40°C ~ 125°C (TJ)	146.25	146.25
6SLX150	147.443	400 MHz	180	4824	4 x DDR,DDR2,DDR3,LPDDR	6 PLLs 12 DCMs	338	576	0°C ~ 85°C (TJ)	158.75	242.5
									0°C ~ 100°C (TJ)	182.5	278.75
6SLX25T	24.051	400 MHz	38	936	2 x DDR,DDR2,DDR3,LPDDR	2 PLLs 4 DCMs	190	250	0°C ~ 85°C (TJ)	50.89	64.33
									0°C ~ 100°C (TJ)	58.52	74.97
									-40°C ~ 125°C (TJ)	66.36	84
6SLX45T	43.661	400 MHz	58	2088	2 x DDR,DDR2,DDR3,LPDDR	4 PLLs 8 DCMs	190	296	0°C ~ 85°C (TJ)	70.21	88.83
									0°C ~ 100°C (TJ)	80.78	102.9
									-40°C ~ 125°C (TJ)	100.24	115.22
6SLX75T	74.637	400 MHz	132	3096	4 x DDR,DDR2,DDR3,LPDDR	6 PLLs 12 DCMs	268	348	0°C ~ 85°C (TJ)	119.21	147.5
									0°C ~ 100°C (TJ)	135	168.75
								268	-40°C ~ 125°C (TJ)	138.75	153.75
6SLX100T	101.261	400 MHz	180	4824	4 x DDR,DDR2,DDR3,LPDDR	6 PLLs 12 DCMs	296	498	0°C ~ 85°C (TJ)	128.75	148.75
									0°C ~ 100°C (TJ)	202.5	232.5
6SLX150T	147.443	400 MHz	180	4824	4 x DDR,DDR2,DDR3,LPDDR	6 PLLs 12 DCMs	296	540	0°C ~ 85°C (TJ)	180	276.25
									0°C ~ 100°C (TJ)	207.5	317.5

Table 3.1: Spartan 6 FPGA comparison

that has a good balance of math blocks versus cost. The next FPGA in the series is on average 50 dollars extra. In addition, 6SLX45T has the military grade option (-40°C $\sim$ 125°C (TJ)) which costs $\sim$20 more per unit. All of the available Spartan-6 can be viewed in Table 3.1.

Artix-7

The Artix-7 is designed to give the most performance per watt while still having the lowest power and cost at 28nm [78]. A comparison of all Artix-7 FPGAs can be seen in Table 3.2. For operating temperature ranges, there is consumer (0 to 85), extended (0 to 100), industrial (-40 to 100), automotive (-40 to 125) and defense (-55 to 125) [78–80].

All of the Artix-7 devices have a maximum clock frequency up to 628 MHz. In

Device	LCs/ LEs/ ALMs (k)	Max Internal Clock	Math blocks	Memory (Max Block RAM (Kb))	Memory Controller	Clock Resources	Min Pins	Max Pins	Operating Temperatures	Min Approx. Price (US$)	Max Approx. Price (US$)
7A15T	16.64	628 MHz	45 DSP Slices	900	DDR3	5x MMCM and PLLs	106	250	0°C ~ 85°C (TJ)	25.69	45.5
									0°C ~ 100°C (TJ)	33.95	60.2
									-40°C ~ 100°C (TJ)	29.54	52.36
7A35T	33.28	628 MHz	90 DSP Slices	1800	DDR3	5x MMCM and PLLs	106	250	0°C ~ 85°C (TJ)	34.37	60.97
									0°C ~ 100°C (TJ)	45.43	80.57
									-40°C ~ 100°C (TJ)	39.55	70.07
7A50T	52.16	628 MHz	120 DSP Slices	2700	DDR3	5x MMCM and PLLs	106	250	0°C ~ 85°C (TJ)	53.2	117.32
									0°C ~ 100°C (TJ)	70.35	106.26
									-40°C ~ 100°C (TJ)	61.18	101.99
7A75T	75.52	628 MHz	180 DSP Slices	3780	DDR3	6x MMCM and PLLs	170	300	0°C ~ 85°C (TJ)	92.61	137.5
									0°C ~ 100°C (TJ)	122.5	182.5
									-40°C ~ 100°C (TJ)	106.47	158.75
7A100T	101.44	628 MHz	240 DSP Slices	4860	DDR3	6x MMCM and PLLs	170	300	0°C ~ 85°C (TJ)	109.2	173.75
									0°C ~ 100°C (TJ)	128.75	128.75
									-40°C ~ 100°C (TJ)	125.58	200
							210	285	-40°C ~ 125°C (TJ)	147.5	161.25
7A200T	215.36	628 MHz	740 DSP Slices	13140	DDR3	10x MMCM and PLLs	285	500	0°C ~ 85°C (TJ)	186.25	282.5
									0°C ~ 100°C (TJ)	246.25	373.75
									-40°C ~ 100°C (TJ)	213.75	325

Table 3.2: Artix 7 FPGA Comparison

addition, each device has a number of PLLs and Mixed-Mode Clock Managers (MMCMs). These MMCMs are modules similar to PLLs but include fractional counters in the feedback and output path as well as more phase shift options [81]. As the number of Logic Cells increases so does the number of math blocks. Each DSP slice contains a 25 x 18 multiplier, pre-adder, adder and 48-bit accumulator [79].

After comparing the Artix-7 FPGAs the best choice is the 7A35T as it has a good balance of the needed Logic cells and DSP slices without having too many and thus increasing the cost and power consumption.

3.3.4 Microsemi FPGAs

Fig.3.6 shows Microsemi FPGA families and their main features. Of the four Microsemi families only the IGLOO2 series have built in DSP hardware or embedded math blocks and thus they are considered here. Having embedded math blocks is a key feature for the design as multiple multiplications are required to process the input

signals from the transducers; these multiplications need to be with numbers that are stored on a large number of bits for high accuracy. If a device does not have embedded math blocks then these multipliers need to be created either with digital logic, memory elements or a combination of both. These methods of creating multipliers are resource intensive and can limit performance. For example a multiplication of two 4-bit numbers requires a memory that is 8-bits wide and 256 (2^8 different possible results) words deep [82]. This has serious scalability issues, as a single 8-bit by 8-bit multiplication would need 131.072 kB of memory to implement. The amount of bytes needed to implement a multiplier can be reduced but it comes at the cost of having to use digital logic resources that could be used for other functionality.

IGLOO2's configuration bits are immune to SEU and IGLOO2 has a CoreEDAC core which supports TMR, error detection and correction hence IGLOO2 FPGAs have a good SEU mitigation.

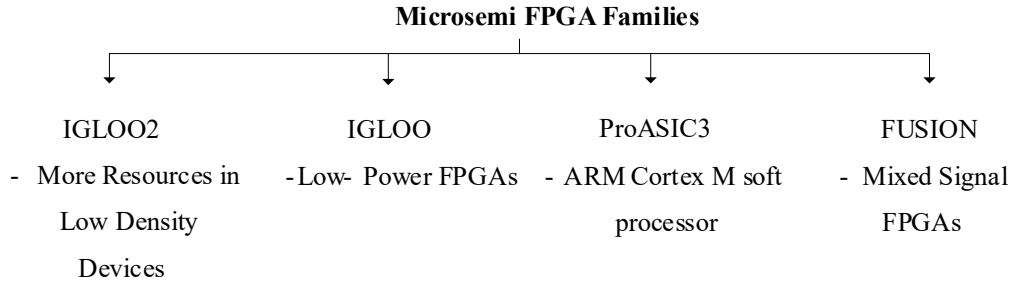


Figure 3.6: Microsemi FPGA Families

IGLOO2

The IGLOO2's are flash-based FPGAs with high-performance communication interfaces and embedded math blocks for DSP functions. IGLOO2's have multiple reliability features such as buffers with SEU resistant latches on DDR bridges and SPI FIFO. Due to the node size and manufacturing process of the embedded Flash memory, the configuration memory of the IGLOO2 is immune to SEU. Fig.3.7 shows structure of IGLOO2 FPGA. Microsemi devices list multiple clocking resources such as a high-precision 32 kHz to 20 MHz Main Crystal Oscillator, a 1 MHz Embedded RC Oscillator, a 50 MHz RC oscillator, multiple PLLs and multiple clock conditioning circuits. The clock conditioning circuits take an input of 1 MHz to 200 MHz and outputs 20 MHz to 400 MHz. Each math block supports 18 x 18 signed multiplications, 17 x 17 unsigned multiplications and has a 44-bit accumulator [83]. Among different products the IGLOO2 M2GL150 and M2GL050 have better memory interfaces as well as more clock resources. The M2GL150 has a high performance but it come at a significantly more expensive price than the M2GL050.

Devices	LCs/LEs/ALMs (k)	Max Internal Clock	Math blocks	Memory Block Total RAM (k bits)	Memory Controller (LPDDR/DDR2/DDR3)	Clock Resources (PLLs and CCCs)	Min Pins	Max Pins	Operating Temperatures	Min Approx. Price (US$)	Max Approx. Price (US$)
M2GL005	6.06	400 Mhz[1]	11	703	1x18 DDR	2	83	209	0°C ~ 85°C (TJ)	13.357	23.392
									-40°C ~ 100°C (TJ)	15.355	26.078
M2GL010	12.084	400 Mhz	22	912	1x18 DDR	6	75	233	0°C ~ 85°C (TJ)	25.364	47.685
									-40°C ~ 100°C (TJ)	29.155	56.49
							233		-55°C ~ 125°C (TJ)	88.17375	100.6578
M2GL025	27.696	400 Mhz	34	1104	1x18 DDR	6	148	267	0°C ~ 85°C (TJ)	42.75	69.76725
									-40°C ~ 100°C (TJ)	46.86108	115.9338
							267		-55°C ~ 125°C (TJ)	130.1065	140.448
M2GL050	56.34	400 Mhz	72	1826	2x36 DDR	6	200	377	0°C ~ 85°C (TJ)	61.72602	117.23
									-40°C ~ 100°C (TJ)	68.45852	208.5841
							267	267	-55°C ~ 125°C (TJ)	182.5558	204.461
M2GL060	56.52	400 Mhz	72	1826	1x18 DDR	6	200	387	0°C ~ 85°C (TJ)	61.72602	104.4523
									-40°C ~ 100°C (TJ)	68.45852	116.9965
M2GL090	86.316	400 Mhz	84	2586	1x18 DDR	6	200	425	0°C ~ 85°C (TJ)	92.25898	178.9515
									-40°C ~ 100°C (TJ)	104.5247	246.1298
							267	267	-55°C ~ 125°C (TJ)	324.4933	349.7728
M2GL150	146.124	400 Mhz	240	5000	2x36 DDR	8	248	574	0°C ~ 85°C (TJ)	207.0544	291.5663
									-40°C ~ 100°C (TJ)	238.1099	707.8529
							574		-55°C ~ 125°C (TJ)	549.315	615.2379

Table 3.3: IGLOO2 FPGAs comparison

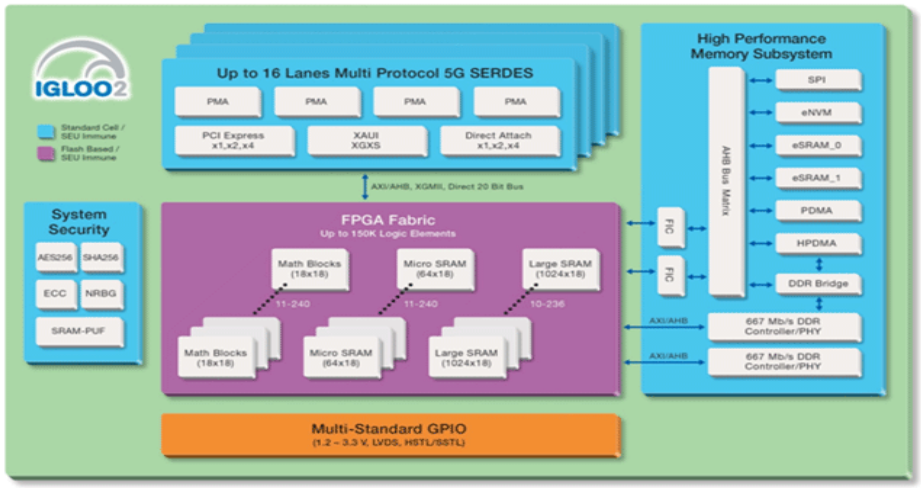


Figure 3.7: IGLOO2 FPGA [2].

3.4 Summary of chosen embedded controller chips

Due to the legacy and the high technology maturity level of the PowerPC Architecture based processors, NXP's MPC5777m has been investigated as a potential Microprocessor. The PowerPC is formerly known as Performance Optimization With Enhanced RISC – Performance Computing. Further literature can be found in the following references to why the choice was performed [84, 85]. The MPC5777m consists of a reliable and safe multi-core MCU and adheres to all the requirements of the Digital Core. It also adheres to the Technology Readiness Level (TRL) that is wanted by Aerosapce industries. Based on the requirements set forth in the first section, Fig.3.8 and Fig.3.9 respectively illustrates the two competing microprocessors and the competing FPGAs chosen for the hybrid FPGA/MCU control board.

Key Features	NXP MPC5777m	TI TMS570LC4357-ZWT
Architecture(s)	Power Architecture	ARM Architecture
Cores Used	3xe200z7 1xe200z4	2xCortex-R5F in Lockstep
Maximum Clock Frequency	300MHz 200MHz	300MHz
Efficiency (DMIPS/MHz)	Low Power and Stop Mode available (DMIPS/MHz not available.)	1.66
Functional Safety Level (ISO 26262)	ASIL-D	ASIL-D
Temperature Range (°C)	-40 to 125	-40 to 125
Communications	Flexray, LINFlex, CAN, CAN-FD, 100Base-T Ethernet, DSPI, I²C	Flexray, LIN, CAN, 10/100 Ethernet, SPI, I²C
Price (USD)	48.9377 per 100 unit	38.45 per 1000 Unit
Memory	8MB Flash 596KB SRAM with Memory Protection Unit	4MB Flash 512KB SRAM With Memory Protection Unit

Figure 3.8: Summary of Chosen MicroProcessors

Key Features	IGLOO2 M2GL050	XA7A35T ARTIX-7	Cyclone V 5CEA4
Gate Technology	Flash	SRAM	SRAM
Manufacturer	Microsemi	Xilinx	Intel FPGA (Formerly known as Altera)
Maximum Clock Frequency	400MHz	628MHz	550MHz
Clock Management Modules	6	5	4
DSP Blocks	72	90	66
Temperature Range	-55 to 125	-40 to 125	-40 to 125
Logic Elements/Cells	56 340	33 280	49 000
Price (USD)	85.239 per 100 Units	46.97 per 10 Units	86.45 per 70 units
Memory	1826 Kb RAM	1800Kb RAM	3080Kb RAM

Figure 3.9: Summary of Chosen FPGA

Chapter 4

Multi-Source Inverter integrated with Hyrbid Energy Storage System

The MSI has been studied for a new type of system architecture in electric propulsion for EVs [86]. This topology converts multiple independent DC sources through a single stage of conversion to obtain a desired output voltage.

4.1 Control and operation of the MSI

A MSI with two input DC sources, shown in Fig.4.1, can have three different output voltages depending on the switching states. Three modes of operations can be defined with two inputs as:

- Mode 1: Switches S_a, S_b, S_c and T_a, T_b, T_c act together to form a two level inverter with V2 as the input DC voltage source. R_a, R_b, R_c are always open.

- Mode 2: Switches R_a, R_b, R_c and S_a, S_b, S_c act together to form a two level inverter with V1-V2 as the equivalent input DC voltage source. T_a, T_b, T_c are always open.

- Mode 3: Switches R_a, R_b, R_c and T_a, T_b, T_c act together to form a two level inverter with V1 as the input DC voltage source. S_a, S_b, S_c are always open.

As shown from Fig.4.1, every operational mode of the MSI consists of a two-level inverter with a different input DC voltage. To control the speed and the torque of the motor connected to the MSI, an adapted Space Vector Pulse Width Modulation (SVPWM) control scheme is developed that is similar to the three-level SVPWM control strategy [87].

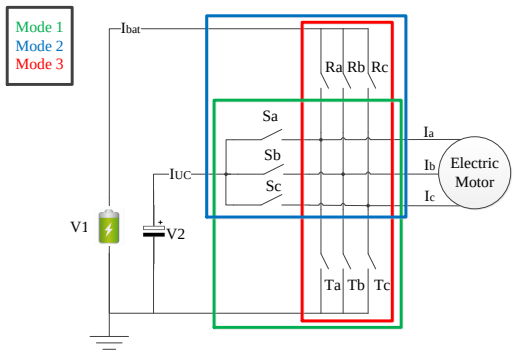


Figure 4.1: Multi-Source Inverter Schematic. Different modes of the MSI are shown.

4.2 HESS using the MSI topology

Using the MSI in a HESS topology can be done by connecting a Li-ion battery to V_1 and connecting a UC to V_2 shown in Fig.2.1-c. As in all active HESS topologies, the HESS-MSI system aims to control the current distribution of both sources such that

the power density of the UC and the energy density of the battery are used efficiently while minimizing the degradation of the battery throughout its lifetime [87–89].

The HESS-MSI's control strategy consists of a closed loop speed-torque control comprising of Proportional Integral (PI) controllers generating the voltage reference to the aforementioned adapted SVPWM algorithm which then chooses the mode of the MSI for the desired speed and torque reference. Since each mode of the MSI consists of one DC source, the current distribution of the battery and UC cannot be controlled as in a conventional HESS. An active mode control scheme has been developed for the HESS-MSI system in reference [87] where the current distribution of both sources can be managed effectively for the load demands. This is done by periodically switching from mode 3 to mode 1 with a control frequency, f_c and discharge duty cycle, D_c. The discharge duty cycle sets how long the battery will supply the load during one control period, $1/f_c$. With an appropriate choice of the control frequency, f_c, the input capacitor banks will keep the input current to the MSI from being discontinuous. Therefore with the added mode control, the average battery current, I_{bat}, and the average UC current, I_{UC}, for one control period can be distributed appropriately with equations (4.1) and (4.2) respectively.

$$I_{bat} = D_c I_{in} \tag{4.1}$$

$$I_{UC} = (1 - D_c) I_{in} \tag{4.2}$$

I_{in} is the average input current that would supply a load during one control period. Dynamically choosing D_c gives the HESS-MSI topology all the advantages of an active HESS topology without the disadvantages of an additional DC/DC converter [88]. The control strategy is shown in Fig.4.2. An energy management controller (EMC)

is introduced to actively chose the current distribution for the demanded load based on the SOC for both sources.

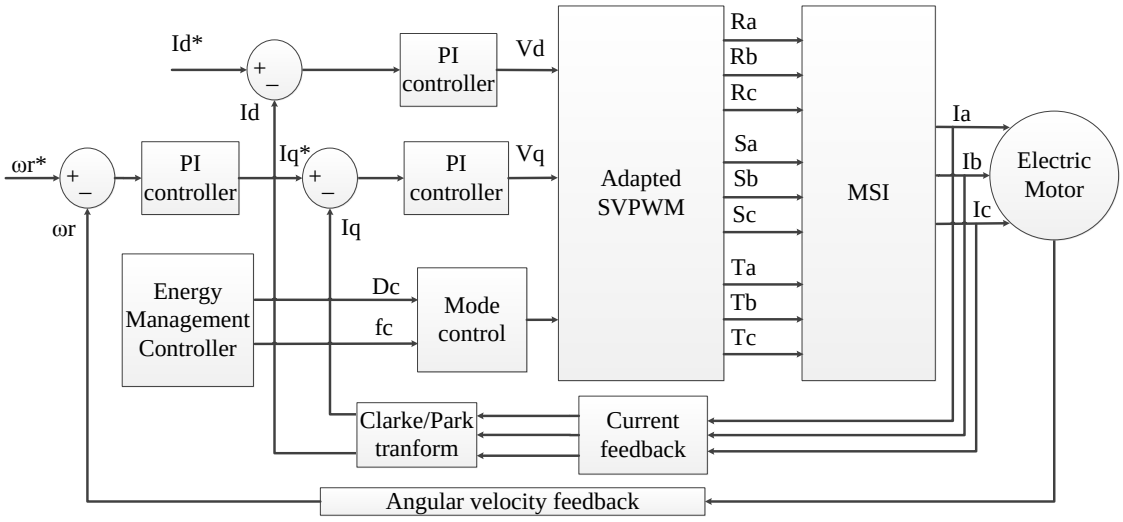


Figure 4.2: Control Strategy for the HESS-MSI system.

Chapter 5

Hybrid FPGA/MCU Supervisory Control Board

5.1 Failure detection, confirmation and description in avionics

5.1.1 Monitoring

There are two means of detecting failures which are:

1. **Monitoring technique**: Monitoring is a non intrusive technique which is mainly based on the comparison between the operational signal and a model (a physical hardware redundancy or theoretical software model). Refresh rate, range, or validity status expected on an input signal are theoretical models. Monitoring is considered as an operational application.

2. **Testing technique**: The testing is considered as an intrusive technique where

stimuli are generated to detect the faults. The tests can be activated automatically or manually.

The monitoring functions are considered as an operational capability of the system. Following failure detection and confirmation by monitoring functions or tests, the system first performs failure adaptation, which consists of a system reconfiguration (i.e. redundancy management) and/or the display of information to the cockpit, cabin, or maintenance crew. After confirmation, failure information (description and context) are also transmitted to the System Built-In Test Equipment (BITE). The System BITE is in charge of failure isolation at the system level (identification of the failure root cause, mainly when multiple failures are detected within a given time frame) and of elaborating a resulting maintenance message if needed. Maintenance messages will only be transmitted if a real failure has been detected. For example, EV, FTI, FAL information have to be managed outside maintenance perimeter: they will not result in maintenance message emission.

5.1.2 System BITE perimeter

Each System BITE has a corresponding "monitoring perimeter" defined in the BITE specification. Every monitoring function within this perimeter sends its result to the same System BITE. A System BITE perimeter is made up of a list of aircraft elements. These elements may be subject to two types of failures which are detected by the system BITE as:

1. **Internal failure** : Failure for which the root cause is located with certainty within the System BITE perimeter. Even in case of ambiguity (multiple possible

root causes), the failure is considered internal only if all the possible root causes are located inside elements which all belong to the System BITE perimeter.

2. **External failure** : Failure for which the root cause is possibly located outside of the System BITE perimeter. In case of ambiguity (multiple possible root causes), if any one of the possible root causes is located in an element which does not belong to the System BITE perimeter, then the failure is deemed external.

5.1.3 Failure Effects

Failures have operational effects which are noticeable from the different crews operating on the aircraft. The different crews of the aircraft are listed below:

1. **Flight Deck Effect**: any effect which may be noticed by the Cockpit Crew when in the flight deck.

2. **Cabin Effect**: any effect which may be noticed by the Cabin Crew, but not by the cockpit crew.

3. **Maintenance Effect**: any effect which may be noticed by the maintenance crew only.

A common term for the failure effects consists of a Flight Deck or Cabin Effecet (FDCE). As these effects will be the first information logged to describe an aircraft malfunction, the list of potential effects corresponding to a given failure has to be provided with each failure description. For a given internal or external failure detected by a system, a resulting effect has to be considered as belonging to the same system at least in the following cases:

1. When the Effect is triggered by another system (i.e. Flight-Warning Systems, Cockpit Display System, CIDS, etc.):
   (a) following a request from the system.
   (b) due to invalid data emitted by system.
2. when the Effect is directly triggered by the system's equipment(s) as a result of the system's own operations or logic.

5.2 Environmental and EMC Qualification

Engineers need to design vehicles that will operate in very severe environment. This comes from the heat of the sahara desert, to the artic cold of Siberia and to the heavy humidity of Costa Rica [fordeurope.blogspot.com]. RTCA/DO-160 (or its precursor, RTCA/DO-138) has been used as a standard for environmental testing since 1958 [3]. It defines standard environmental test conditions (categories) and applicable test procedures for airborne equipment. The categories that have been developed over time reflect a reasonably mature understanding as to the severity of the environmental stresses, the degrees of mitigation achievable in the design of an installation, and the robustness that must be designed into equipment in order to perform in the operating environment.

5.2.1 EMI Test

ESD, EFT, surge, and conducted RF. These test signals are specified in a basic standard, like the DO-160 or the IEC 61000-4-2 at a certain voltage and a certain performance acceptance criterion. The performance acceptance criterion A means

that the controller module shall continue to operate as intended with no loss of function or performance even during the test. This would be an example requirement for a conducted RF where the module has to pass without any performance degradation.

Criterion C would means that there is a temporary degradation of performance during the test accepted. However, after the test, the module shall continue to operate as intended without any manual intervention. This would be the minimum requirement for the ESD, the EFT, and the surge. Further criterions can be found within [3].

5.3 Electronic Control Unit Design

In the Supervisory Control Board (SCB) design, only sections 19, 20,21 and 22 of the DO-160G are taken into account. Due to the time of a masters thesis, environmental conditions are not tested in this design. Simulations are performed to validate the EMC requirements of the SCB. As of this point, the SCB will be named as an Electronic Control Unit (ECU) to facilitate the reader's point of view.

5.3.1 Architecture Block Diagram

Flexible, agile and reconfigurable manufacturing systems based on a modular product and process. Through model based design, the project includes the following steps:

1. Analysis for different module in the ECU
2. Characterization and Evaluation of individual modules within ECU
3. ECU integration and prototyping.

The top level architecture is captured with the ORCAD Schematic Capture (Insert Reference of Orcad) software and is shown in 5.1. The design of the modules are organized (Hardware and Firmware) as a set of distinct components that can be developed independently and then plugged together. This design is scalable and can adapt to a variety of power level, and power control. The design methodology is applied for some functional blocks of the ECU. The following modules are developed through this methodology:

- EMI Filter and Power supplies module
- RS232 Interface
- CAN Interface
- Discrete Inputs Interface
- Discrete Outputs Interface
- Analog Inputs Interface
- Analog Outputs Interface
- Microprocessor Interface
- FPGA Interface

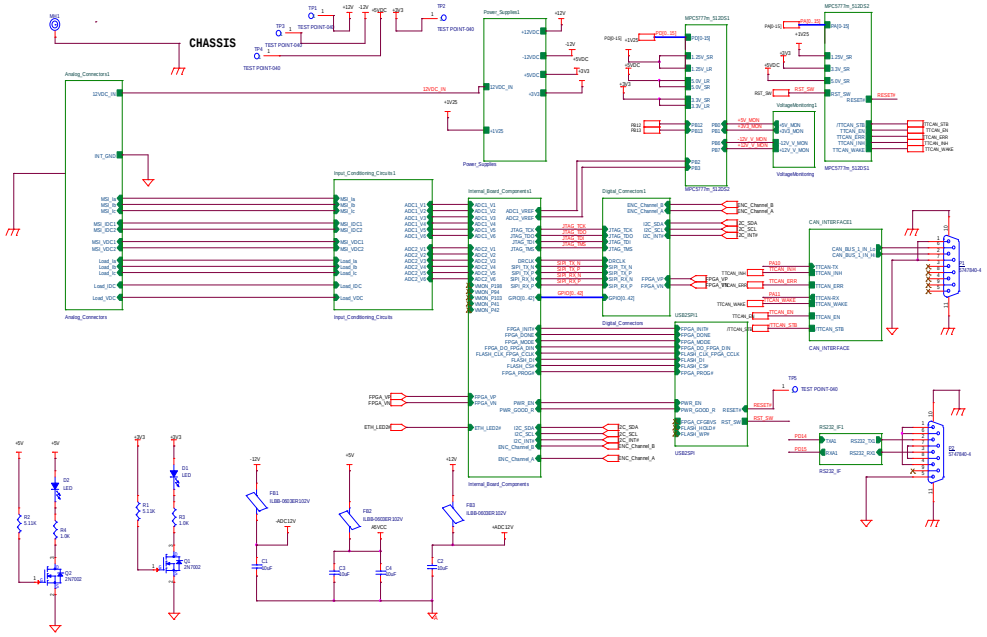


Figure 5.1: ECU hardware Orcad Schematic Top Level.

5.3.2 EMI Filter and Power supplies

The ECU receives input power from the 12V Battery. The controller EMI Filter and Power Supplies module perform the following functions:

- EMI Filtering and Protection
- Internal Power Distribution
- Internal Power Regulation to 16V by a DC/DC boost converter

- Overvoltage Fault Protection

The board generates all the power supplies needed for the different modules.

5.3.3 ECU Requirements

The ECU design will have the following requirements:

- MASc_HRD1: The controller **shall** be compatible with steady state voltages of +12V DC provided by the battery.
- MASc_HRD2: The controller **shall** be protected against Reverse Polarity conditions on the Power Input bus.
- MASc_HRD3: The maximum power demand of the controller (not including external loads) **shall** be <40W.
- MASc_HRD4: The ECU **shall** provide EMI / Transient filtering on the power input path used for critical load management and internal DC/DC Conversion.
- MASc_HRD5: The voltage measurement **shall** have an accuracy of <= ±0.5V with respect to the voltage at the ECU Power Input pins.
- MASc_HRD6: The ECU **shall** provide any necessary internal voltage rails to support ECU functions and core processing.
- MASc_HRD7: Any internally generated voltages **shall** be made available to the digital core via an ADC for monitoring and reporting to support failure detection and design for test.

- MASc_HRD8: The Power-Built-In Test (PBIT) **shall** be completed without failure or nuisance-faults when the ECU power is applied within the steady state value of 12VDC.

The ECU filtering and protection blocks may incorporate voltage and/or current limiting protections to ensure downstream components are not damaged during abnormal conditions such as power or signal transients.

5.3.4 Conceptual design

Analog connectors and EMI filter blocks

The analog connector block contains the analog interface and the connector that interfaces with the external systems. This is shown in Fig.5.2.

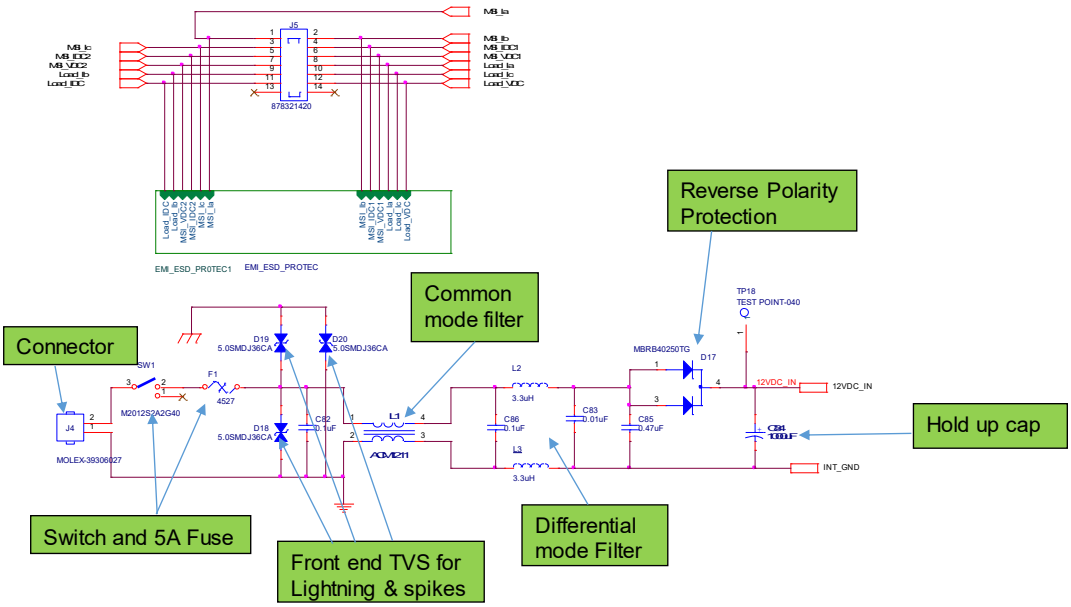


Figure 5.2: Analog connectors block and EMI filter.

This block contains the EMI protection, the power supply front end EMI filter and transient protection. The main components are listed below:

- Power supply connector
- Power switch
- Fuse
- Transient Voltage Suppression (TVS) diodes for power inputs
- Common mode filter
- Differential mode filter
- Reverse polarity protection
- Hold up capacitor
- EMI protection for the input signals

Power supplies Blocks

The ECU generates all of the power supplies needed for the different components on the ECU controller board. The power supplies are shown in Fig.5.3. The five auxiliary power supplies that are needed for the control board operations are:

- +12V
- -12V
- +5V

- +3.3V
- +1.25V

For the analog signal acquisition, the following power supply outputs are filtered for extra noise immunity through a ferrite bead:

- +12V
- -12V
- +5V

The front end block allows the ECU to be powered from 48V down to 12V in case of any power supply transients.

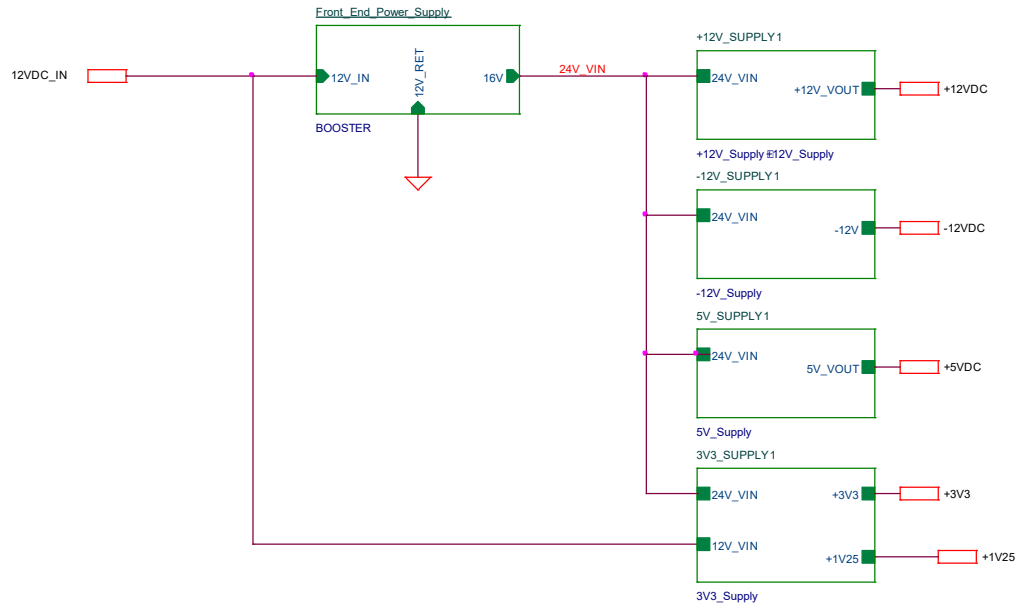


Figure 5.3: Power supplies block.

5.3.5 Detailed design

EMI filter description

The front end design contains an EMI filter. The EMI filter consists of passive components, including common mode choke filter, capacitors and inductors. This EMI filter allows to keep the inside noise of the equipment inside and the outside noise outside. Its function is to reduce high frequency electronic noise that may cause interference with other devices. Regulatory standards limit the amount of noise that can be emitted. EMI is generated from the Turn-on/off of the electrical current and comes from a variety of sources residing on the ECU. High frequencies range from several kHz to more than 20 MHz as described in [3]. The following two types of filters are used:

- Common mode filter
- Differential mode filter

The common mode filter is based on inductor choke filter and capacitors. The capacitors provide a low impedance path to divert the high frequency noise away from the input of the filter, either back into the power supply, or into the chassis ground connection. The differential mode filter is based on inductor and capacitors. The inductors allow DC or low frequency currents to pass through, while blocking the harmful and unwanted high frequency currents. The capacitors provide a low impedance path to divert the high frequency noise away from the input of the filter, either back into the power supply or into the chassis ground connection.

EMI filter Implementation

The EMI Filter characteristics are comprised of the following:

- TVS protection against lightning
- Common mode filter
- Differential filter
- Reverse polarity protection by serial schottky diode
- Hold up capacitor

The input filter implementation is shown in Fig.5.4. Due to the different parasitics inductors and capacitors there is risk of oscillations. The analysis will be performed by spice simulation. The circuit will be loaded by the different input passive circuit (rectifier, resistor inductor and capacitor). The power input is protected against lightning through the TVS diodes, taking into consideration the operational and environmental conditions for the automotive or the aerospace environments, specifically power quality requirements. The lightning protection are connected to the common chassis ground to meet differential mode injection requirements.

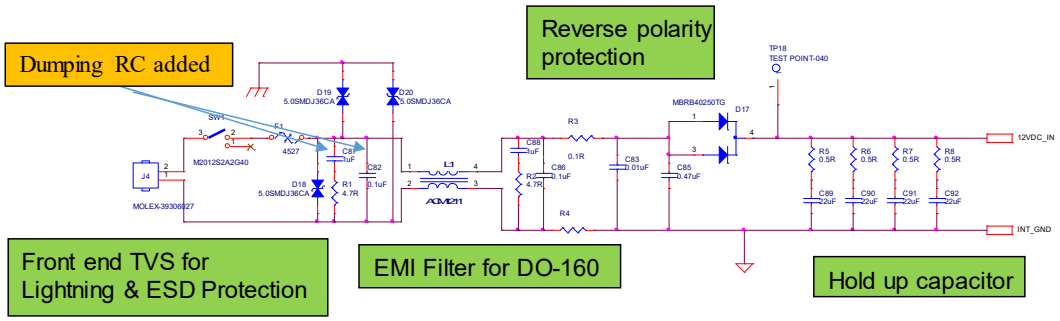


Figure 5.4: Front end EMI Filter.

EMI Filter Validation by Simulation

The EMI filter shown in Fig.5.4 includes an overshoot due to the parasitic inductance from the harness and large current fluctuations (di/dt). Thus, a dumping Resistor-Capacitor (RC) filter is added. It includes two ceramic capacitors placed very close to the pin connectors as shown in the simulation model from Fig.5.5.

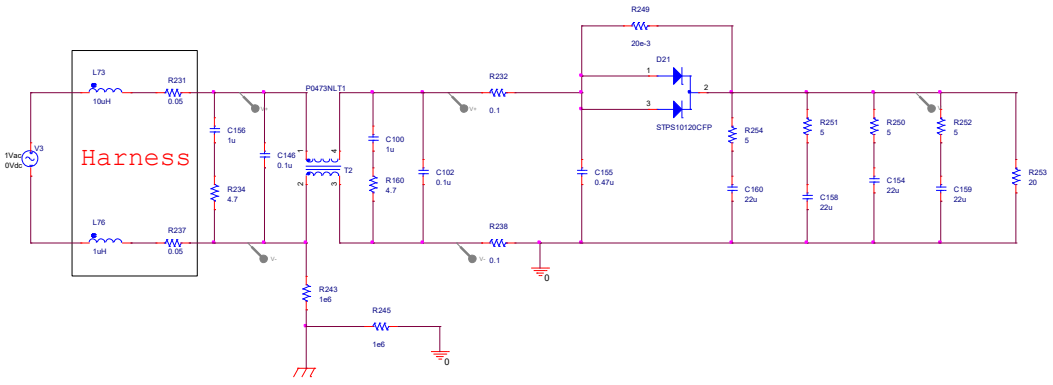


Figure 5.5: Front end filter simulation model.

For the simulation model, the diode is replaced by the equivalent small signal model. The TVS diodes are open circuit, the capacitance is negligible (500pF). The harness is simulated by its inductor equivalent of 10uH. The improved response with the added dumping RC filter added is shown in Fig.5.6.

Figure 5.6: Improved Front end filter simulation results.

The next step of the analysis if to perform the an AC response of the filter from the power supply input. The purpose of this analysis is to verify the ability of the filter to attenuate the conducted emission level. The AC response test bench for the simulation is shown in Fig.5.7 along with the Bode plot results of the AC response in Fig.5.8.

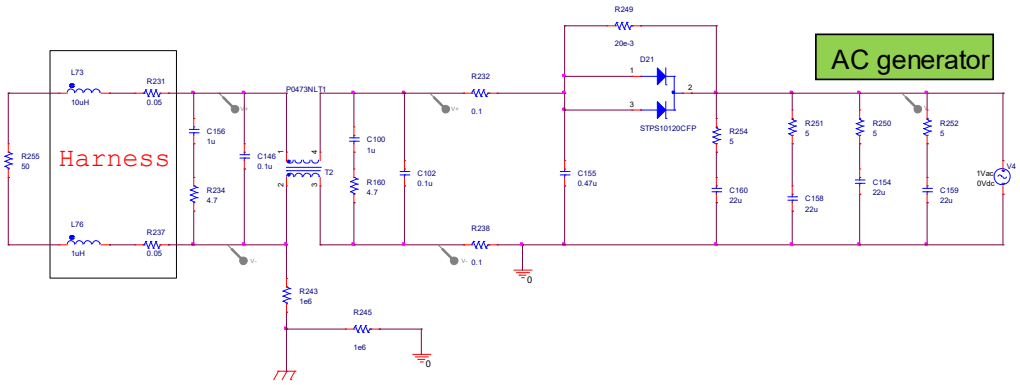


Figure 5.7: Simulation test bench AC response from the output.

Figure 5.8: Bode plot of the AC response from the output.

Radio Frequency Conducted Emissions

The purpose of the conducted emissions test determines that the ECU does not emit undesired RF noise in excess of the levels specified in Section 5.7.2 of the DO-160F. The resquirements for the RF conducted emissions test **shall** be conducted according

Table 5.1: Emission Frequency Bandwidth and Dwell Time per DO-160G

Frequency Range	**6dB Bandwidth**	**Dwell Time**
0.150 – 30MHz	1kHz	0.015 seconds
30 – 152MHz	10kHz	0.015 seconds

to RTCA, Inc. DO-160F, Section 21, category M [3]. The maximum conducted RF interference level is illustrated in Fig.5.9. The measurement receiver bandwidths and minimum dwell times are listed in Table 5.1. Fig.5.10 is a figure from [3] section 21 that depicts the testbench for the conducted emissions test.

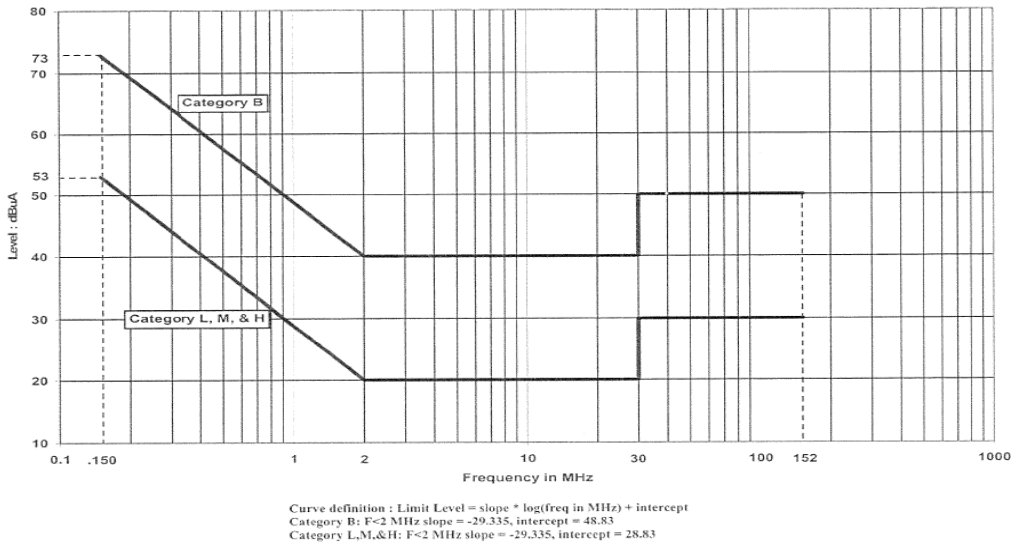


Figure 5.9: Maximum Level of Conducted RF Interference – Power Lines (Category M) [3].

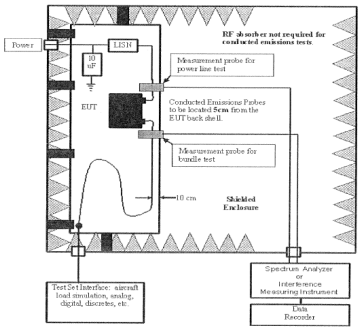


Figure 5.10: RF Conducted emission test [3].

The simulations performed for the conducted emissions test are shown in Fig.5.12. The test bench that the simulation was performed is according to Fig.5.10 and is shown in Fig.5.11.

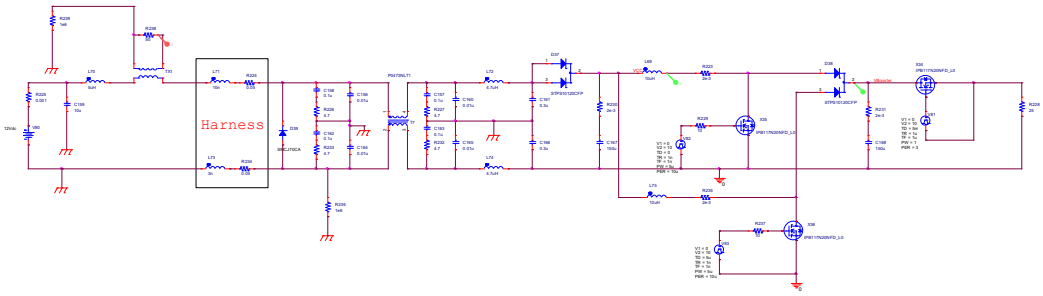


Figure 5.11: CE simulation test bench.

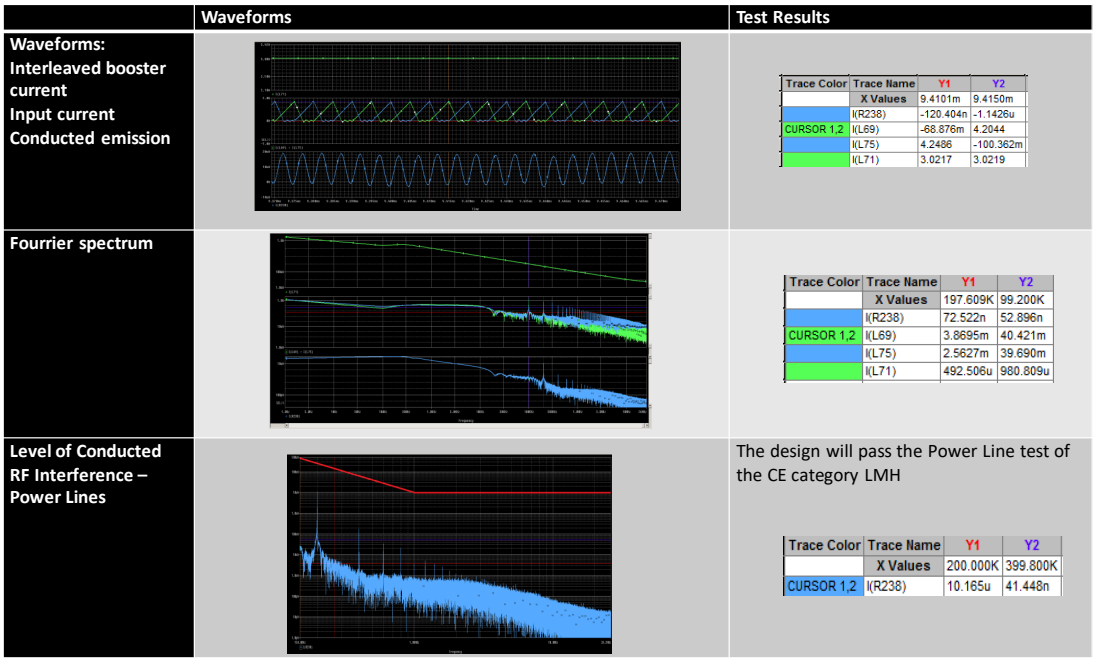


Figure 5.12: CE simulation test results.

Radio Frequency Conducted Susceptibility

The purpose of the RF conducted susceptibility test is to determine whether the ECU will operate within performance specifications when the ECU and interconnecting wiring are exposed to an unwanted level of RF modulated power by probe injection onto the power lines and interface circuit wiring. The requirements for the RF conducted susceptibility **shall** be conducted according to RTCA, Inc. DO-160F, Section 20, Tables 3 and 8 [3]. The required RF test levels are illustrated in Table 5.2. The blocking device used for the power input is a diode.

Table 5.2: RF Conducted Susceptibility Test Level HIRF Environment I & II [3].

Frequency Band	**Environment I Test Level (mA)**	**Environment II Test Level (mA)**
10 KHz to 500 KHz	3-150 (Note 1)	0.6-30 (Note 1)
500 KHz to 2 MHzzIissue 2 Tables 16&17esponse timeuts the critical function is not adversely affectedncy and with 4	150	45
2 MHz to 30 MHz	150	150
30 MHz to 100 MHz	150	30
100 MHz to 200 MHz	150	45
200 MHz to 400 MHz	150	30

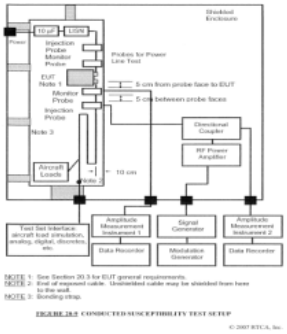


Figure 5.13: RF Conducted Susceptibility Test Set Up [3].

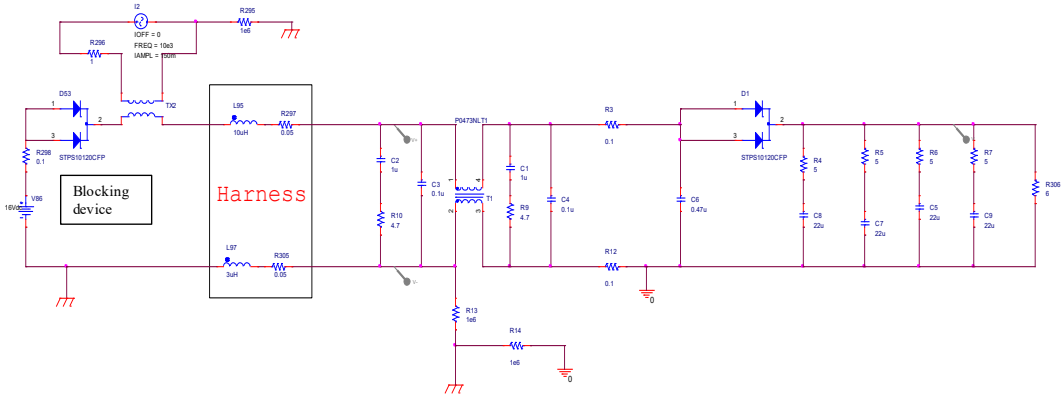


Figure 5.14: RF Conducted Susceptibility simulation test bench.

Figure 5.15: DC/DC Boost converter Input current conducted susceptibility simulation results for 150mA injection at 10kHz.

Table 5.3: DO-160G guidelines.

Waveform 3 (Voc/Isc)		**Waveform 4 (Voc/Isc)**	
Shielded	**Unshielded**	**Shielded**	**Unshielded**
600V/24A	600V/24A	300V/60A	300V/60A

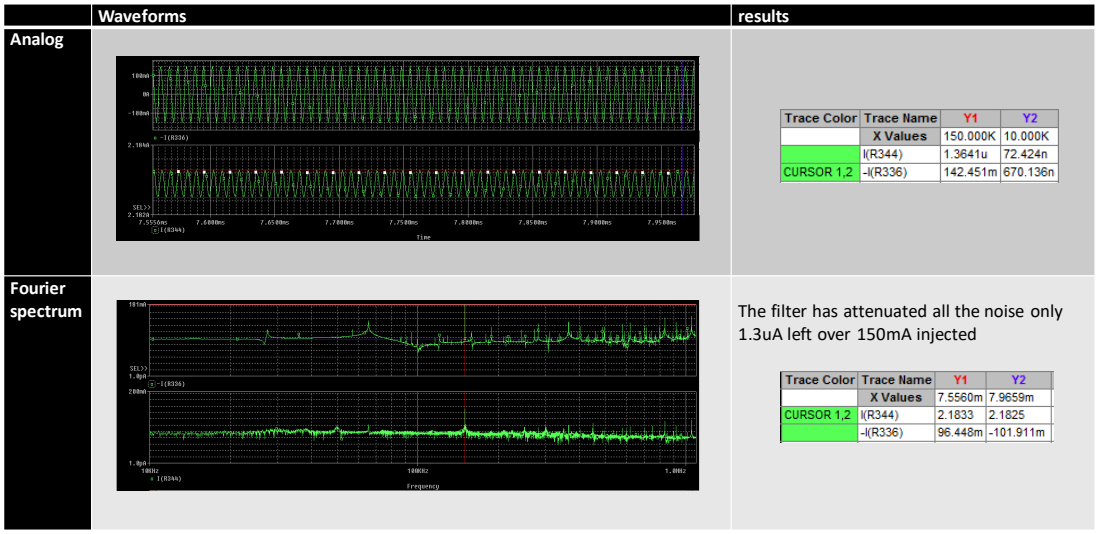
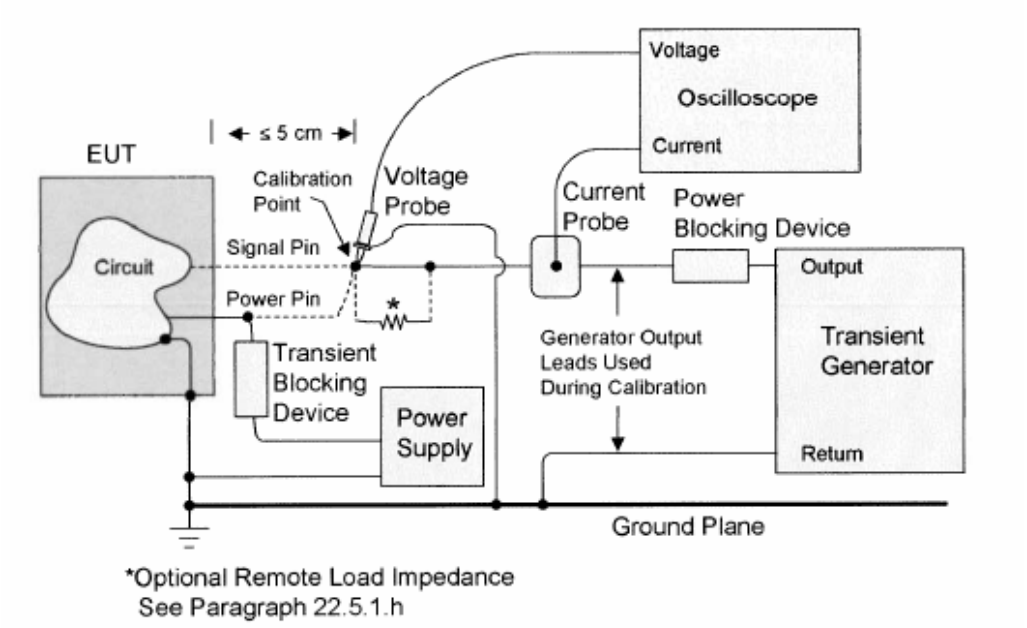


Figure 5.16: DC/DC Boost converter Input current conducted susceptibility simulation results for 150mA injection at 150kHz.

Pin Injection Test on Power Pin

The purpose of the pin injection test is to verify the capability of the equipment to withstand a selection of test transients defined in section 22 of the DO-160G which are intended to represent the induced effects of lightning. The waveforms and levels, and the pass/fail criteria for equipment performance during the test shall be listed in the applicable equipment specification.



NOTES:

1. *The notes from the calibration setup of Figure 22-10 apply.*
2. *Test setup and procedures are to be such that the required lightning transients appear differentially between the aircraft power and return/neutral lines. If power and return/neutral originate from a remote load, in the same cable bundle with signals, then the test setup should use an isolated power return to ensure the proper common-mode evaluation.*
3. *The power supply is not necessary for tests on un-powered equipment.*
4. *Test procedures assume lightning transients appear common-mode between all pins and case. If the expected installation utilizes local power and/or signal returns tied either internally or externally to case or aircraft structure, tests shall be performed with the return(s) tied to the case.*
5. *Return wire lengths shall be kept as short as possible.*

Figure 5.17: Waveform 4 pin injection – power line [3].

The requirement for the pin Injection test **shall** be conducted with a test procedure according to RTCA, Inc. DO-160G, Section 22. The pin injection test levels are applicable to the power line pins. Waveform 4 is illustrated in Fig.5.17 and referenced from Figures 22-4, 22-5 & 22-6 of DO-160G, pages 22-26 and 22-27 [3]. The guidelines

for the pin injection test are outlined in Table 5.3. The simulation test bench for the pin injection waveform 4 level 1 test, is shown in Fig.5.18. The results for the validation in simulation are shown in 5.19.

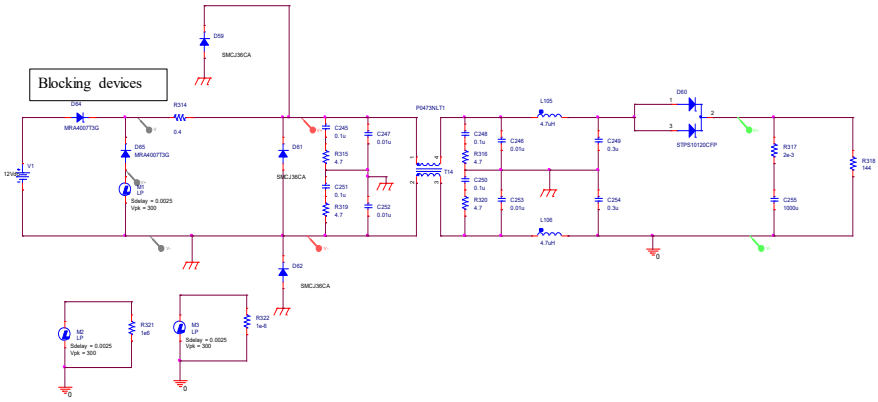


Figure 5.18: Power line Pin injection test bench.

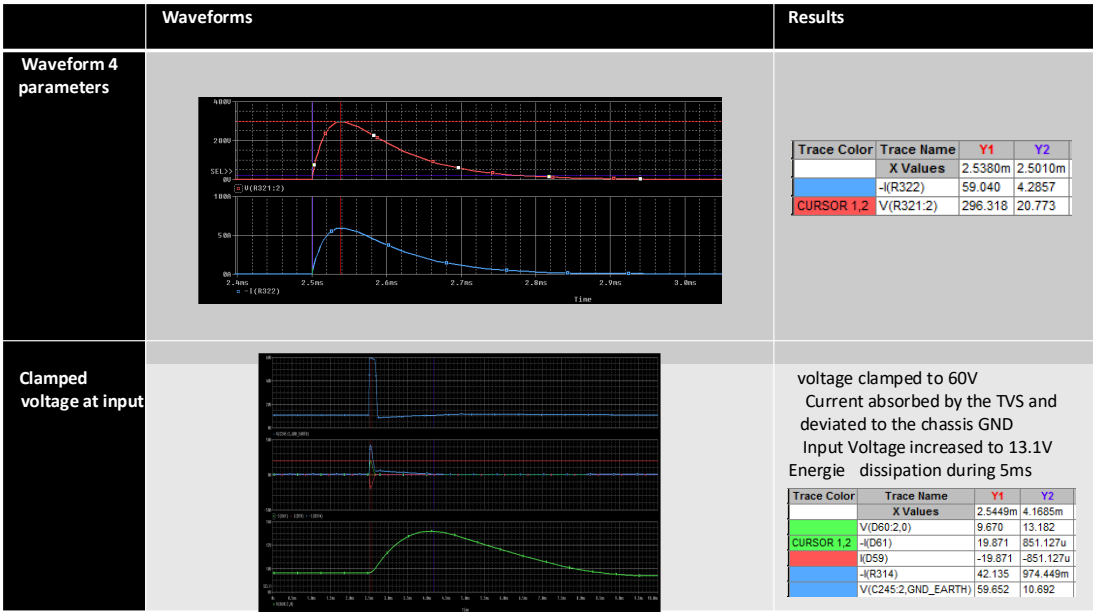


Figure 5.19: Power line Pin injection simulation results.

Electro-Static Discharge

The Electro-Static Dsicharge (ESD) test is intended to prove the ability of the equipment to perform its intended function, or not suffering permanent damage, when exposed to electrostatic discharges. It relates to equipment which may be involved in static electricity discharges from human contact. The test is applicable for all electronic equipment which are accessible to any person during operation or maintenance of the aircraft.

According to IEC 61000-4-2 [90], the immunity to electrostatic discharge shall be determined by the ability of the equipment under test (EUT) to withstand a series of electrostatic contact discharges of 8kV, directed at specific human contact locations on the Electronic Under Test (EUT). The quantity of pulses shall be ten (**??**) of both

positive and negative voltage polarities at each of the selected locations. Similarly for the DO160G, the equipment shall have the ability to withstand a series of electrostatic discharge pulse of 15,000V. The test diagram from the DO160G is shown in 5.20.

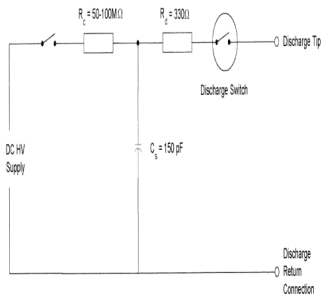


Figure 5.20: Simplified diagram of the ESD Generator – DO 160F section 25 [3].

Analog Connector Block

From the input voltage, auxiliary power supplies output the following voltages to supply the board functions:

- 16V
- 12V
- -12V
- 5V
- 3.3V
- 1.25V

Front end power supply

The front end power supply is designed to provide the necessary input voltage for the different auxiliary internal power supplies. In the case of 12 V battery a step up converter is needed to ensure reliable functionality of the duty cycle of the DC/DC Buck converter generating 12V from the 12V supply. Input operating voltage range is 12 V to 48V. The auxiliary supplies need a voltage higher than 12V to operate correctly. The DC/DC Boost converter topology is a 2 stage Inter-leaved Boost Converter. Each phase can supply half of the input current. The opearting current is 5ADC maximum from the 12VDC power input. The switching frequency is set to 100kHz per phase, thus giving an equivalent of 200kHz output frequency of the DC/DC Boost Converter. The output voltage is regulated at 16V with a precision of 3%. The maximum efficiency is greater than 97% due to the LM5032 chip utilised.

Using LM5032, interleaved booster ECU using average current mode control from TI. Due to this controller change a daughter board was used. The front end is built around the LM5032. The main components Include the LM5032 current mode controller, the power MOSFETs as well as the rectifying diode.

The LM5032 implements two parallel interleaved control channels using the forward converter topology.Its features include:

- Input ripple current reduced by two channels operating in interleaved mode.
- Each regulator channel contains a complete PWM controller, current sense input, soft-start circuit, and gate driver output.
- Common to both channels are the startup and VCC regulator, line undervoltage

- Switching frequency up to 2 MHz
- Maximum duty cycle control, and hiccup mode fault protection circuit.
- Input under-voltage lockout circuit (UVLO) designed to enable the VCC regulator and output drivers when the system voltage (VPWR) exceeds the desired level.

The power MOSFETs are chosen with a VDS rating capability of widthstanding the maximum High Voltage (HV) port and transient spikes (ringing). In this design, the maximum HV-rail voltage is 16 V. Selecting the 60 V rated MOSFETs will allow 40-V transient spikes. The Rds(ON) is equivalent to 0.04ω and has a total gate charge, Q_g, to balance the conduction and switching losses. The thermal stress and the conduction losses in each MOSFET is determined by the following equations:

$$P_{cond} = R_{DS\_125} \times I^2_{Q\_RMS}$$

$$R_{DS\_125} = 1.8 \times R_{DS\_25}$$

$$I_{Q\_RMS} = \sqrt{D_{max}} \times I_{max}$$

Pcond = 0.324W

where 1.8 is the approximate temperature coefficient of the Rds(ON) at 125°C, Dmax is the maximum duty cycle. The switching voltage transient rise and fall times are approximately determined by:

$$t_{rise} = \frac{Q_G}{I_{source}} = \frac{13}{1.5} = 8.7ns$$

$$t_{fall} = \frac{Q_G}{I_{sink}} = \frac{13}{2.5} = 5.2ns$$

And the switching losses of each of the paralleled MOSFETs are approximated by:

$$P_{Q\_SW} = 0.5 \times C_{OSS} \times V_{HV}^2 \times F_{SW} + 0.5 \times I_{peak} \times V_{HV} \times (t_{rise} + t_{fall}) \times F_{SW}$$

The resulting power dissipation is of 40mW per MOSFET where $Coss = 170pF$ is the MOSFET's output capacitance and a Gate charge of $Q_g = 12nC$. A gate-to-source resistor of $10k\Omega$ is used to mitigate the effects of a failed gate drive.

The rectifying diode used is MBRB40250TG. It is a Switch-mode Schottky Power Rectifier with a blocking voltage of 250 V and maximum current of 40 A. Its forward voltage is equivalent to 0.86V with a soft recovery characteristic of $T_{RR} < 35ns$. The equivalent junction temperature is $T_J = 65 - 150°Celsius$

An RC Snubber is added to suppress high-frequency oscillations associated with the reverse recovery effects in power converters. The L-C tank oscillates at a frequency and amplitude that is generally unknown until the circuit is tested. In many instances the oscillation amplitude and duration is significant and must be reduced. One solution is to damp or "snub" the oscillation with a series R-C circuit, typically placed across the rectifier or the FET device.

This ringing or oscillation can generate radiated and conducted noise, cause circuit jitter, over-stress components, and create excessive dissipation. This is often a major concern in applications such as audio, processor power, and any design that requires electromagnetic interference (EMI) qualification.

Here a simple resistor-capacitor (R-C) snubber to damp out the ringing is added

across the rectifier. The choice of the capacitor value is based on the dynamic capacitor of the rectifier. Empirically, the snubber capacitance is chosen to be 10 times the rectifier capacitor. The effects of the snubber circuit is a comprimise between osccilation and efficiency as shown in Fig.5.21. Larger values for Csnub reduce the voltage spike amplitude further, but also increase power loss in Rsnub. A tradeoff between acceptable voltage ring amplitude and Rsnub loss. The values for the RC snubber circuit are listed below:

- $Csnub = 10nF$
- $Rsnub = 10\Omega$

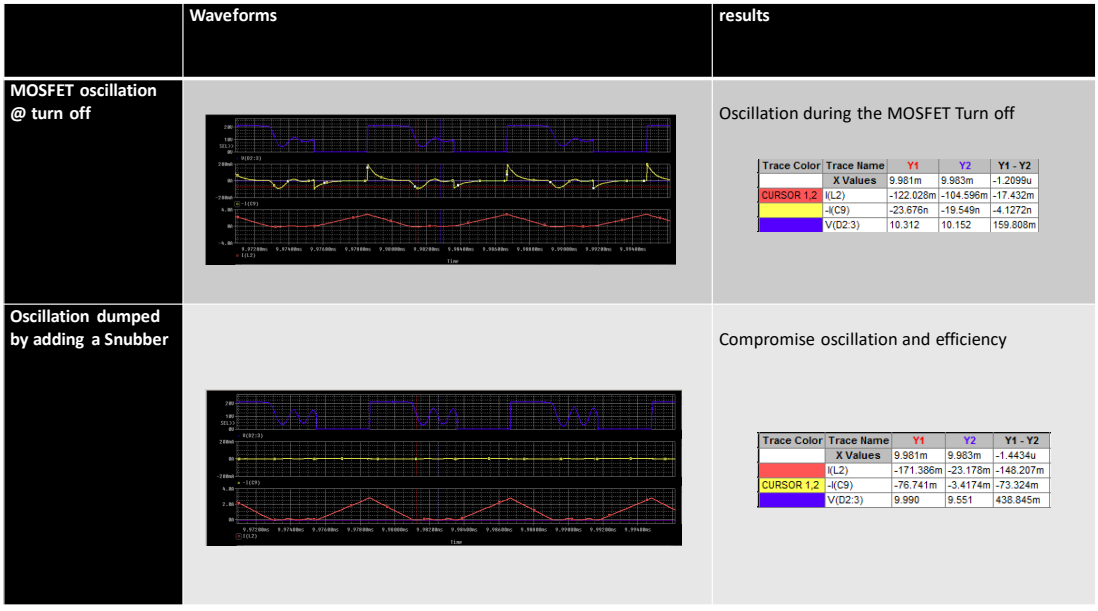


Figure 5.21: Dumping the MOSFET oscillation at turn OFF.

From the vendor Texas Instruments, the LM5032 pspice model is not available. In this simulation the interleaved features advantages are shown through the simulation

testbench in Fig.5.22. The simulation results are shown for Discontinuous Conduction Mode (DCM) and Continuous Conduction mode (CCM) respectively in Fig.5.23 and Fig.5.25. The Fast Fourier Transform (FFT) of the controller in both states DCM and CCM are respectively shown in Fig.5.24 and Fig.5.26.

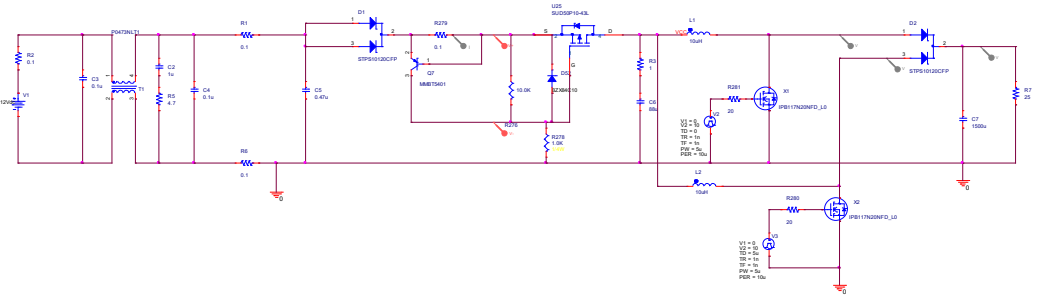


Figure 5.22: Interleaved Booster simulation model.

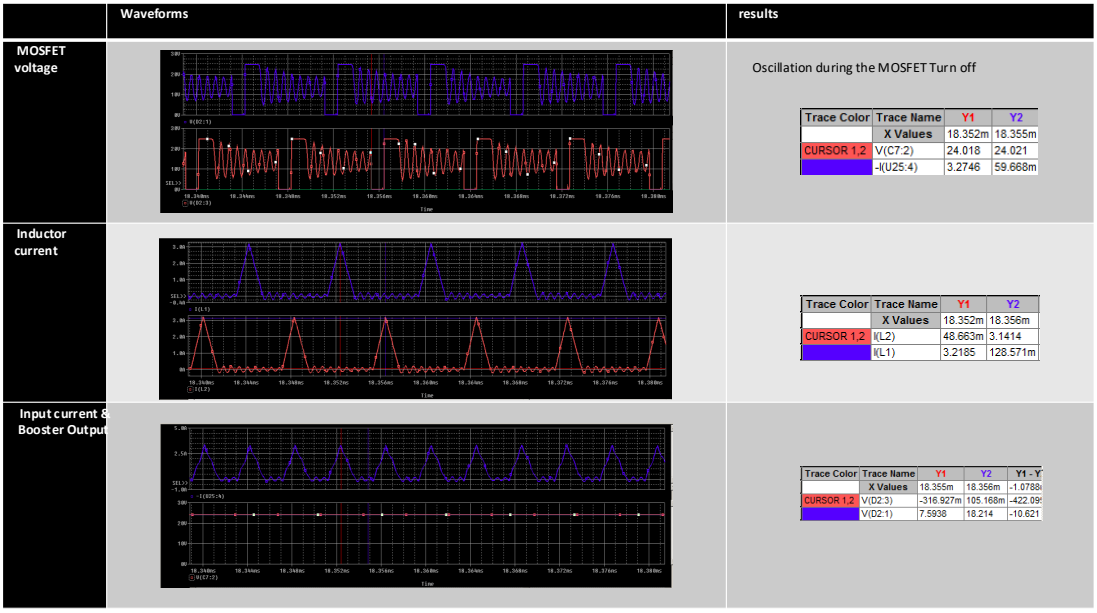


Figure 5.23: Booster Simulation results non continuous conduction.

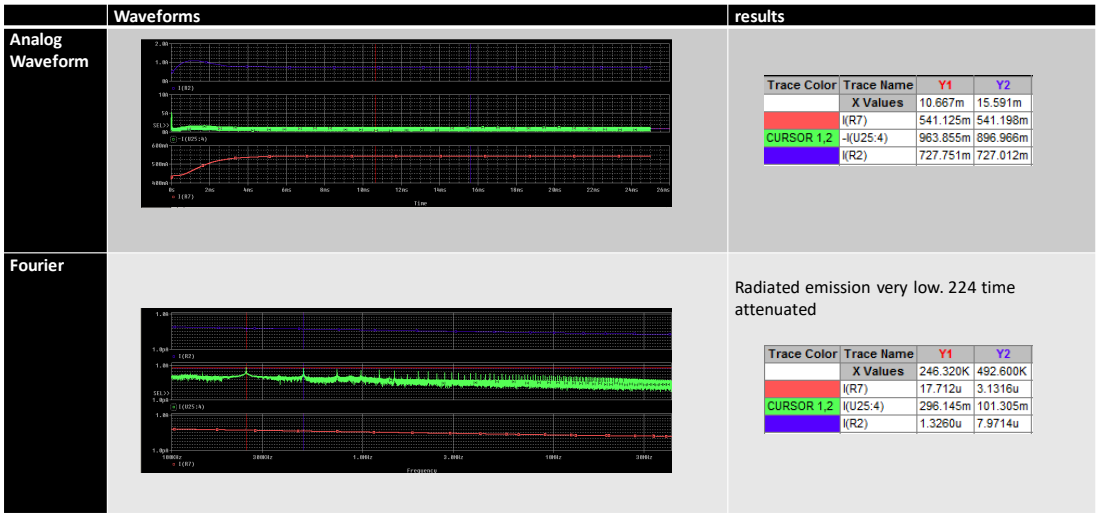


Figure 5.24: Non continuous conduction mode current.

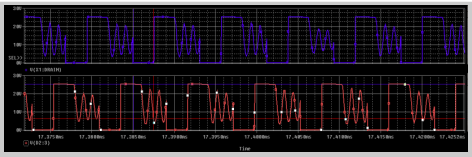
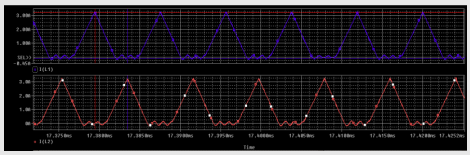
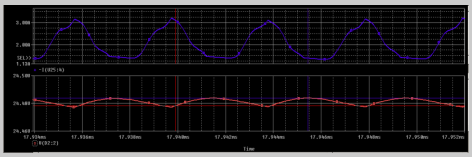
	Waveforms	results
MOSFET voltage		Trace Color | Trace Name | Y1 | Y2 X Values | 17.388m | 17.385m CURSOR 1,2 | V(D2:3) | 6.2112 | 25.128 V(X1:DRAIN) | 42.215m | 3.3814m
Inductor current		Trace Color | Trace Name | Y1 | Y2 X Values | 17.380m | 17.384m I(L2) | -46.016m | 3.1945 CURSOR 1,2 | I(L1) | 3.1925 | -82.423m
Input current & Booster Output		Trace Color | Trace Name | Y1 | Y2 X Values | 17.940m | 17.945m CURSOR 1,2 | V(D2:2) | 24.478 | 24.484 -I(U25:4) | 3.1060 | 1.3785

Figure 5.25: Continuous conduction.

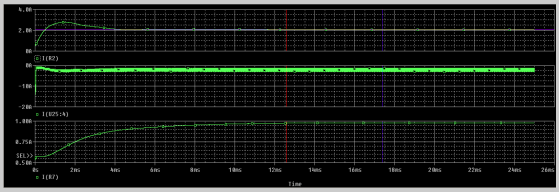
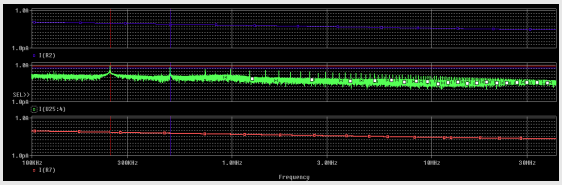
	Waveforms	results
Analog Waveform		Trace Color | Trace Name | Y1 | Y2 X Values | 12.596m | 17.376m I(R7) | 974.551m | 979.006m I(U25:4) | -1.9665 | -2.7273 CURSOR 1,2 | I(R2) | 2.0656 | 2.0565
Fourier		Radiated emission very low. 7000 times attenuated Trace Color | Trace Name | Y1 | Y2 X Values | 246.320K | 492.600K I(R7) | 20.197u | 11.836u CURSOR 1,2 | I(U25:4) | 628.568m | 124.321m I(R2) | 78.697u | 39.118u

Figure 5.26: Continuous conduction mode Current.

Auxiliary power supplies

This example details the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known in order to start the design process. The simulation test bench is shown in Fig.5.27.

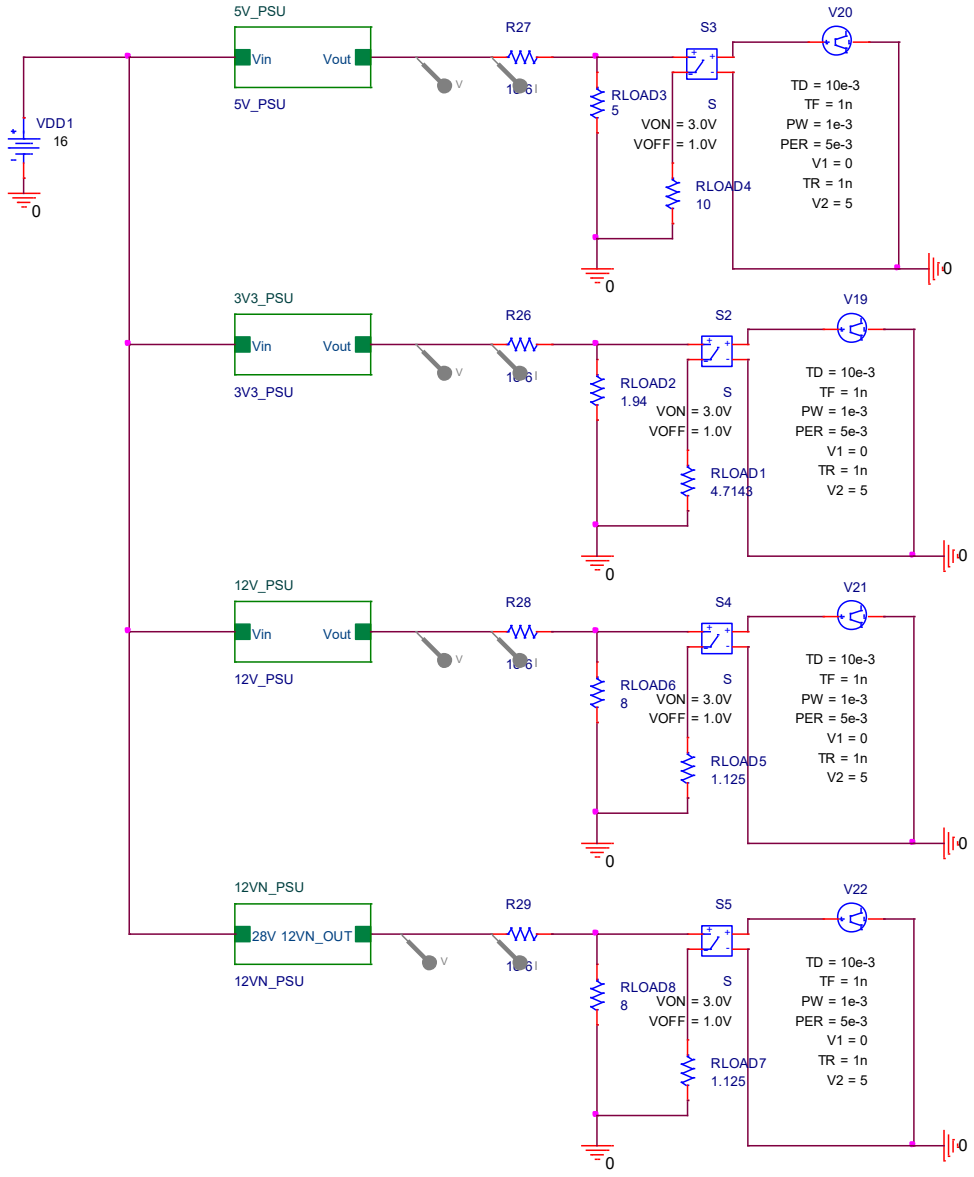


Figure 5.27: Power Supply simulation test bench.

The design procedure is outlined below regarding both the Buck Converter Design

and the Compensator network for controlling the power supply. The Step-Down Buck converter design is based on the above requirements from table 1. The final schematic is shown in figure 1.

The TPS40200 is used as the voltage regulator. For the switching MOSFET, the SUD50P10-43L is used. The components that will be redesigned are as follows:

1. Output Inductor
2. Output Capacitor
3. Network Compensator: Type III Analog OP-Amp Compensator

It must be noted that the Ferrite Beads are not included in the simulation since they do not affect the circuit at the analysed frequencies.

5.3.6 Auxiliary buck converter design procedure

Using design requirements of the various auxilirary power supplies, the necessary steady state duty cycle is found in equation [1]:

$$(V_{out} + I_{OUT} * R_L + V_d) = (V_{in} + V_d - V_{ds})D, [1]$$

Equation [1] takes into account the voltage drop, V_d, on the Shottky Diode along with the voltage drop, V_{ds}, of the MOSFET. The voltage drop across the inductor is taken into account as well through its DC Resistance (DCR).

The next step is to find the minimum inductance for the inductor such that a continuous current is found at the load at all times. Equation [2] states the necessary

condition for the minimum inductance:

$$L_{MIN} = D_{MIN} * \frac{V_{IN,MAX} - V_{out}}{f_s I_{Peak}}, [2]$$

Where D_{MIN} is the minimum duty cycle for a high line (Maximum V_{IN}) and a low load (Minimum I_{OUT}) and I_{Peak} is the maximum, minimum load current on the inductor (2*MIN(IOUT)). The inductance of the inductor is chosen such that it is 1.25 times the minimum value to ensure Continuous Conduction Mode (CCM). This will limit the amount of EMI in the system.

To ensure the output voltage remains constant, the capacitance of an output capacitor is chosen based on two criteria shown in equations [3] and [4]:

$$C_{OUT} = \frac{L_{OUT} * I_{OUT}^2}{\left(\Delta V_{OUT} + V_{OUT}\right)^2 - V_{OUT}^2}, [3]$$

$$C_{OUT} = \frac{\left(MAX\left(I_{OUT}\right) - MIN\left(I_{OUT}\right)\right) * \left(1 - D_{MIN}\right)}{\left(f_s * \Delta V_{OUT} * V_{OUT}\right)}, [4]$$

Equation [3] demonstrates the stored energy in the inductor that the capacitor needs to absorb during a sudden load change while equation [4] comes from having a full load step with a certain specified voltage overshoot of ΔV_{OUT}. The larger capacitance of equations [3] and [4] would be used such that the energy requirements are met in both cases.

5.3.7 Compensator network design procedure

The compensator chosen was a Type III Op-Amp Compensator due to the nature of the designed RLC Filter at the output of the buck converter. The LC filter frequency

response is shown below for the minimum load, nominal load and maximum load using the 12V design as an example. As shown in Fig.5.28, the phase margin at a desired cut off frequency of 40kHz for the LC filter is -180° so a type 3 compensator is used to boost the phase up to theoretical 180°.

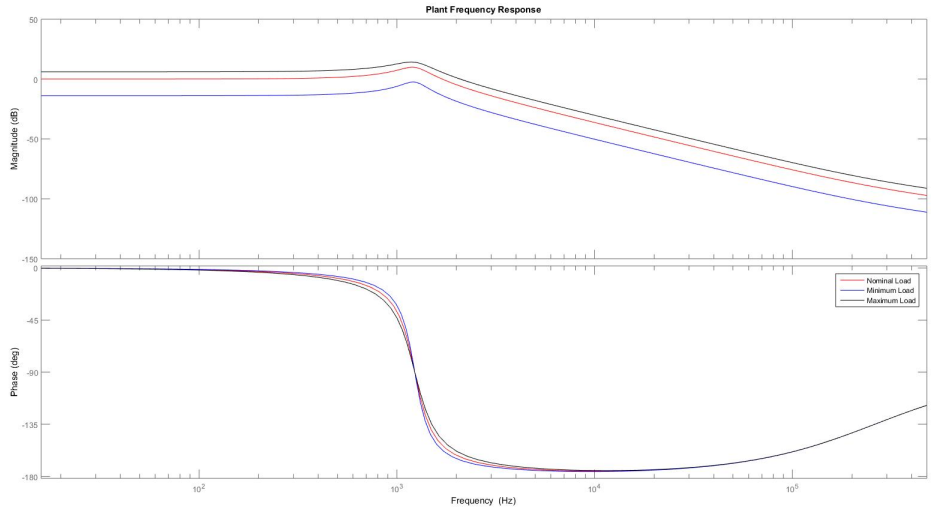


Figure 5.28: 12V RLC output filter bode plot.

The compensator circuit used is shown in Fig.5.29 along with the added poles and zeros of the compensated design. The goal is to achieve a -20dB roll off at the cut off frequency along with a 45° Phase Margin.

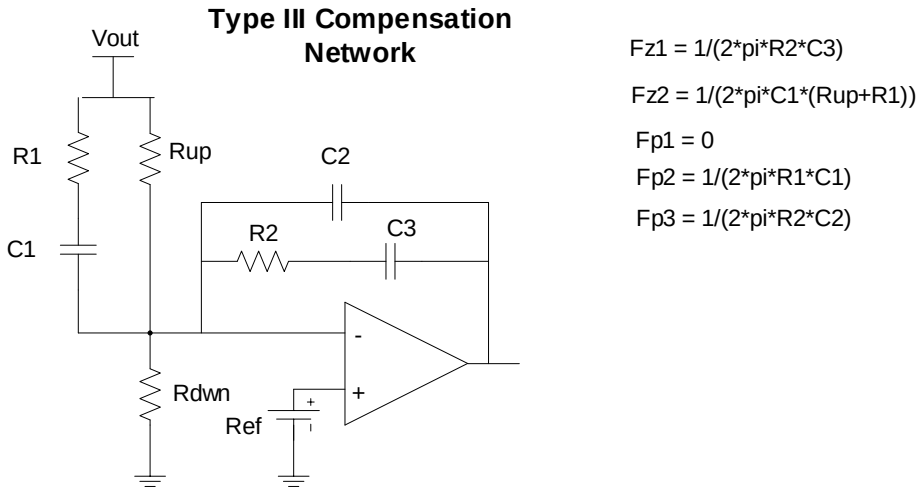


Figure 5.29: Schematic of the type-III compensation network.

+12V auxiliary power supply

The implementation of the 12V auxiliary power supply is shown in Fig.5.30. The simulation of the 12V auxiliary power supply is shown Fig.**??**. The design parameters for the 12V auxiliary power supplies are as follows:

- $VIN_{NOM} = 16V$
- $VIN_{MIN} = 12V$
- $VIN_{MAX} = 24V$
- $VOUT = -12V$
- $IOUT_{MIN} = 100mA$

- $IOUT_{NOM} = 300mA$
- $IOUT_{MAX} = 500mA$

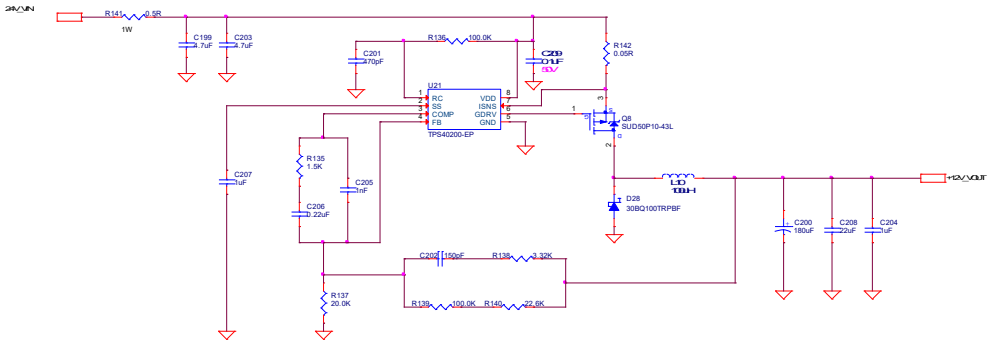


Figure 5.30: +12V Power supply schematic.

-12V auxiliary power supply

The implementation of the -12V auxiliary power supply is shown in Fig.5.31. The simulation of the -12V auxiliary power supply is shown Fig.5.32. The design parameters for the -12V auxiliary power supplies are as follows:

- $VIN_{NOM} = 16V$
- $VIN_{MIN} = 12V$
- $VIN_{MAX} = 24V$
- $VOUT = -12V$
- $IOUT_{MIN} = 100mA$

- $IOUT_{NOM} = 300mA$
- $IOUT_{MAX} = 500mA$

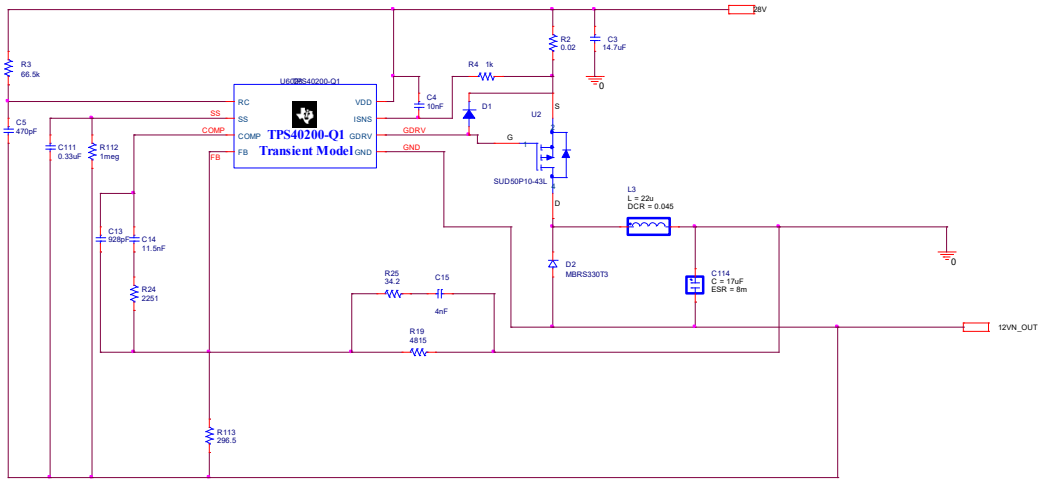
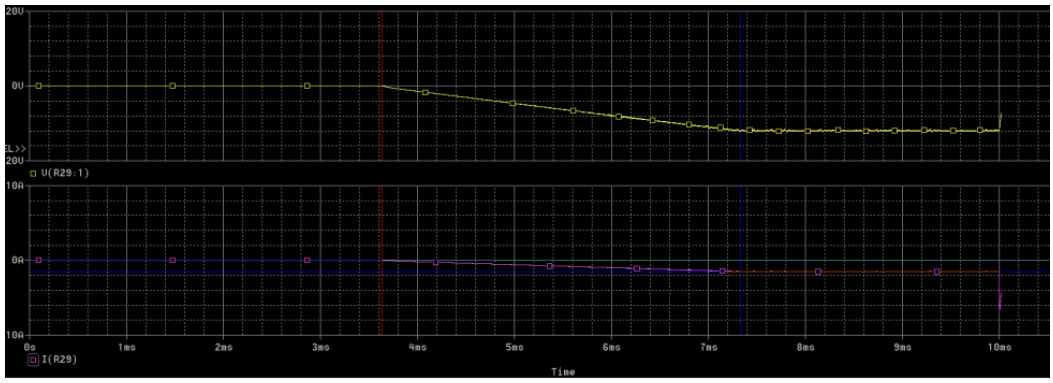


Figure 5.31: -12V Power supply Simulation Test Bench.



Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	3.6313m	7.3313m	-3.7000m
CURSOR 1,2	I(R29)	514.056u	-1.5088	1.5093
	V(R29:1)	4.1124m	-12.070	12.074

Figure 5.32: -12V Power supply simulation results.

5V auxiliary power supply

The implementation of the 5V auxiliary power supply is shown in Fig.5.33. The simulation of the 5V auxiliary power supply is shown Fig.5.34. The design parameters for the 5V auxiliary power supplies are as follows:

- $VIN_{NOM} = 16V$
- $VIN_{MIN} = 12V$
- $VIN_{MAX} = 24V$
- $VOUT = 5V$
- $IOUT_{MIN} = 500mA$

- $IOUT_{NOM} = 1A$
- $IOUT_{MAX} = 1.5A$

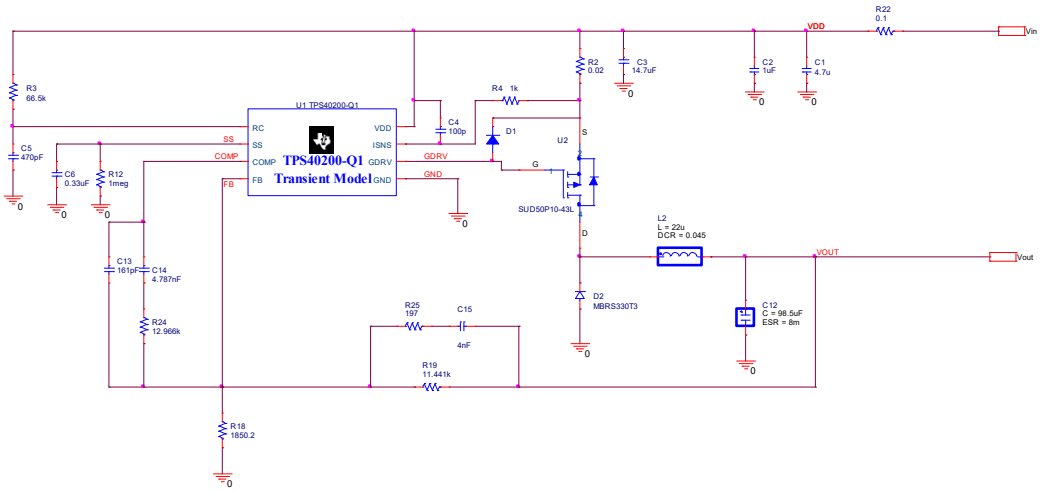
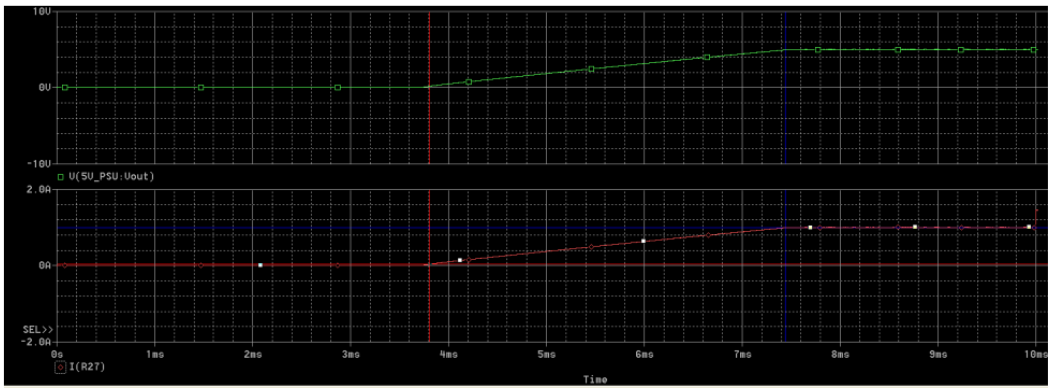


Figure 5.33: 5V Power supply Simulation Test Bench.



Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	3.8050m	7.4403m	-3.6353m
CURSOR 1,2	I(R27)	38.332m	993.273m	-954.941m
	V(5V_PSU:Vout)	191.660m	4.9663	-4.7746

Figure 5.34: 5V Power supply simulation results.

3.3V auxiliary power supply

The implementation of the 3.3V auxiliary power supply is shown in Fig.5.35. The simulation of the 3.3V auxiliary power supply is shown Fig.5.36. The design parameters for the 3.3V auxiliary power supplies are as follows:

- $VIN_{NOM} = 16V$
- $VIN_{MIN} = 12V$
- $VIN_{MAX} = 24V$
- $VOUT = 3.3V$
- $IOUT_{MIN} = 700mA$
- $IOUT_{NOM} = 1.2A$

- $IOUT_{MAX} = 1.7A$

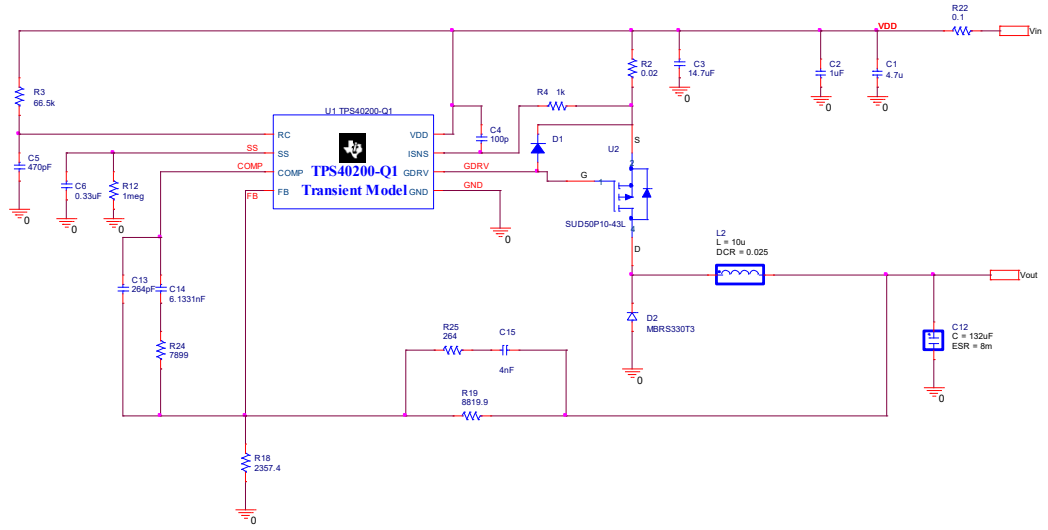
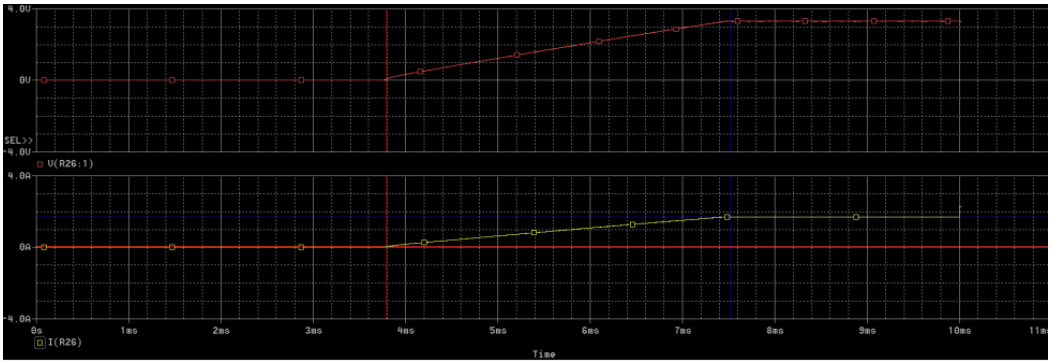


Figure 5.35: 3.3V Power supply simulation Test bench.



Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	3.7925m	7.5220m	-3.7295m
CURSOR 1,2	I(R26)	41.166m	1.7052	-1.6640
	V(R26:1)	79.896m	3.3080	-3.2281

Figure 5.36: 3.3V Power supply simulation results.

1.25V auxiliary power supply

Due to the model of the controller not being available, the verification of the power supply was performed with the Motherboard of the MPC5777m evaluation module [put reference of MPC5777m EVM]. The same design was implemented to ensure validation of the pwoer supply.

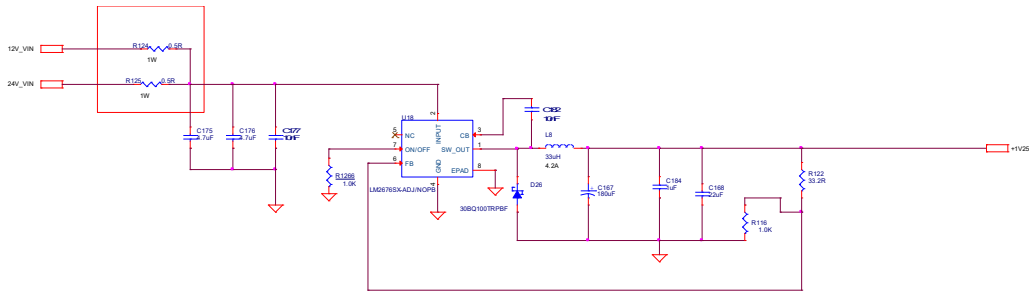


Figure 5.37: 1.25V Power Supply schematic.

5.4 Control and Data acquisition

The acquisition of analog input sensors is a function that is implemented in most of Electronic Control Unit. To be utilized by the Application Software (AS), the analog value must be converted to a digital value and processed. This task is performed by a combination of ADC, FPGA and component drivers (MOSFET, or IGBT). The sensor types encountered in these applications are often very similar. We can distinguish the following main families:

1. Current sensor

2. Voltage sensor

3. Position sensors

4. Temperature sensors: ThermoCouple (TC),

5. Strain Gauges (SG),

The acquisition of the control board is based on digital sampling and digital signal processing. The channels for processing such sensors have a similar structure, which can be defined as shown in Fig.5.38. The ECU is a flexible design capable of managing various applications and platforms. The ECU can accommodate various type of interfaces.

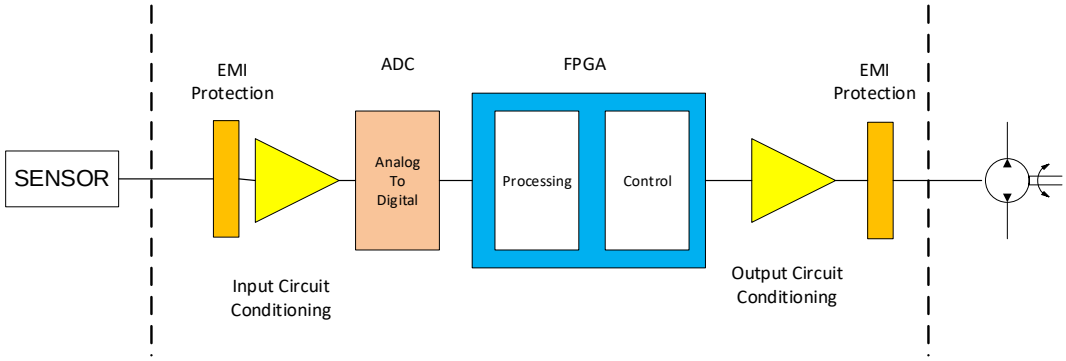


Figure 5.38: Analog data acquisition.

5.4.1 Functional Requirements

Analog inputs

The ECU **shall** have 12 analog inputs (ADC_IN[1:12]).

The ECU **shall** be able to acquire analog inputs with a range of ±10V.

The ECU HW **shall** convert the conditioned analog input to a SW-readable (digitized) value via an external ADC and FPGA.

The ECU **shall** measure the current of each motor phase (Phase A, Phase B, Phase C) with the following characteristics:

- Range: -5A to 5A
- Accuracy: 3%
- Resolution: 0.1A
- Bandwidth: ¿66KHz (at -3dB)

The current measurements **shall** be provided to the FPGA as a digital representation (eg. through an analog to digital converter).

Control Output

The ECU **shall** drive a PMSM motor.

Each Permanent Magnet Synchronous Motor (PMSM) **shall** be driven by one three phase inverter (i.e. DC-to-AC converter). The PMSM has the following characteristics:

- Resistance ph-n at 20 °C : 1.43 Ohm +/-10%
- Inductance ph-n : 0.1 mH +/-30%
- Back EMF Constant : 0.09 V peak ph-n/(rad/s mechanical equivalent rotational speed)

The three phase inverter **shall** use a power MOSFET that has the following requirements:

- The ECU **shall** provide control to 6 Power MOSFET integrated in a 2 level, 3-phase inverter to drive a PMSM motor.
- The MOSFET **shall** be able to handle a peak current of 10A at any temperature between -40 and +70C.
- The MOSFET switching time **shall** be lower than 200ns.

Each power MOSFET needs A suitable driver circuit with the following requirements:

- The MOSFET Driver **shall** be provided for the proper switching at frequency as high as 50 KHz.
- The MOSFET Driver **shall** combine both isolation and buffer-drive function.
- The MOSFET Driver **shall** integrate a programmable dead time and a disable control.
- The MOSFET driver operating voltage **shall** be higher or equal than 15V.
- The MOSFET driver input **shall** be TTL compatible.
- The MOSFET driver output voltage **shall** be in the range of 8 to 12V.
- The switching time of the MOSFET Driver **shall** be lower than 10ns.
- The maximum gate drive current **shall** be higher or equal than 4A.

- The MOSFET gate driver **shall** integrate suitable protection against reverse currents.
- An anti-parallel diode **shall** be provided in order to lower the turn off delay.
- The MOSFET **shall** be protected against high dv/dt terms.

ADC Interface

The ECU's Data acquisition system **shall** provide an interface according to the functional requirements and constraints of the ADS8556 data sheet.

The ADC **shall** operate in parallel mode.

The ADC **shall** be configured using the external pins as shown in Table 7.1.

Based on the requirements listed above, the ADC chip from TI ADS8556 is selected to perform the analog to digital conversion. Its features include the following:

- 16 bit ADC Resolution.
- Input: Bipolar signal range ±10 V.
- Sampling Rate: Up to 800 kSPS
- Supply +12V, -12V, 5V and 3.3V
- ADC resolution = $\frac{10}{2^{15}}$ 0.305mV nominal
- ADC accuracy at 400ks/s = $\frac{10V}{2^{14}}$ 0.610mV (represent 10 ENOB (effective number of bits))
- 2 ADC are used which allows 12 analog input converted simultaneously.

The Analog to digital (ADC) conversion is performed by two ADS8556 ADC from Texas Instrument [101]. This will provides accurate and fast conversions for a wide range of applications. Each ADC has 6-channel input, simultaneous sampling, integrated data acquisition system based on a 16-bit Successive Approximation Register (SAR) Analog-to-Digital converter (ADC). Each input channel on the device supports true bipolar input ranges of ±10 V. The sampling rate is set to 386kS/s. The voltage reference is external and is using the IC REF5025AIDR. The implementation of the schematic is shown in Fig.5.39.

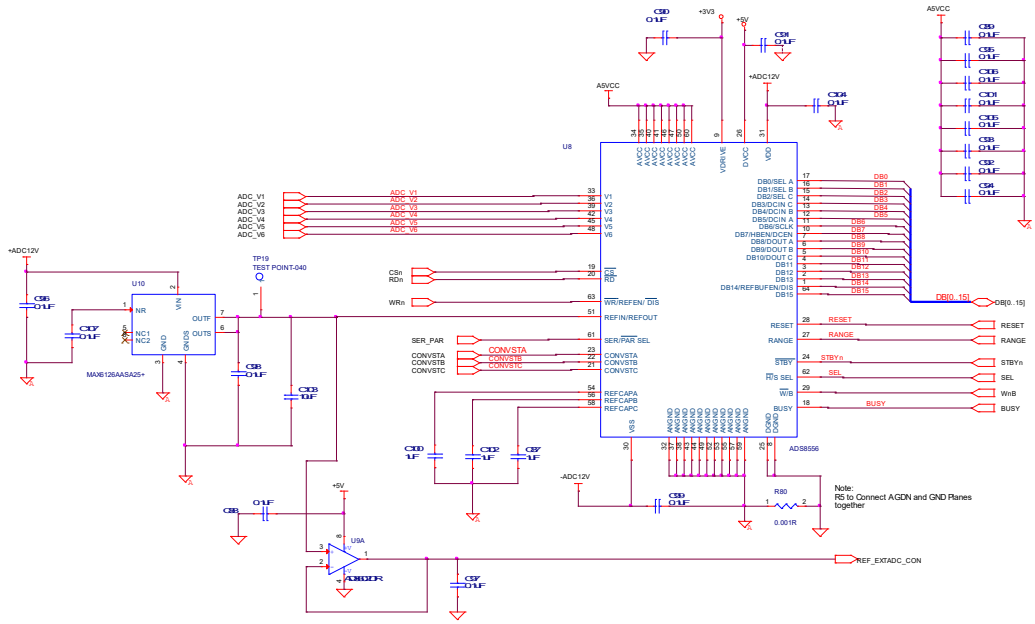


Figure 5.39: Simultaneous Acquisition of 6 analog signals with one ADC.

A low pass filter is added before the ADC preventing the aliasing components to be captured. The cut off frequency is 56KHz, of this filter which is below the Nyquist

frequency. With the two independent ADCs, the ECU can acquire enough data to treat twelve sensors of any type. The ADS8556 uses a high speed parallel interface that allows sampling rates of up to 800 kSPS.

The ADC should have a perfect linear realtionship from converting analog signals to digital signals but that is never the case inthe real world. The ADC transfer function is not perfectly linear, so a linear curve fit based on the end point is applied to the function. This is shown in Fig.5.40. The corrected code is given by the following equation:

$$Y = S \times X + offset$$

Where

$$S = \frac{V_{ou2} - V_{out1}}{V_{in2} - V_{in1}}$$

X is the measured code

$$offset = Conversion\ Code\ axis\ intercept$$

Consequently, the gain error is:

$$GE = \frac{S - S_0}{S_0} \times 100\%$$

S_0 is the ideal transfer function.

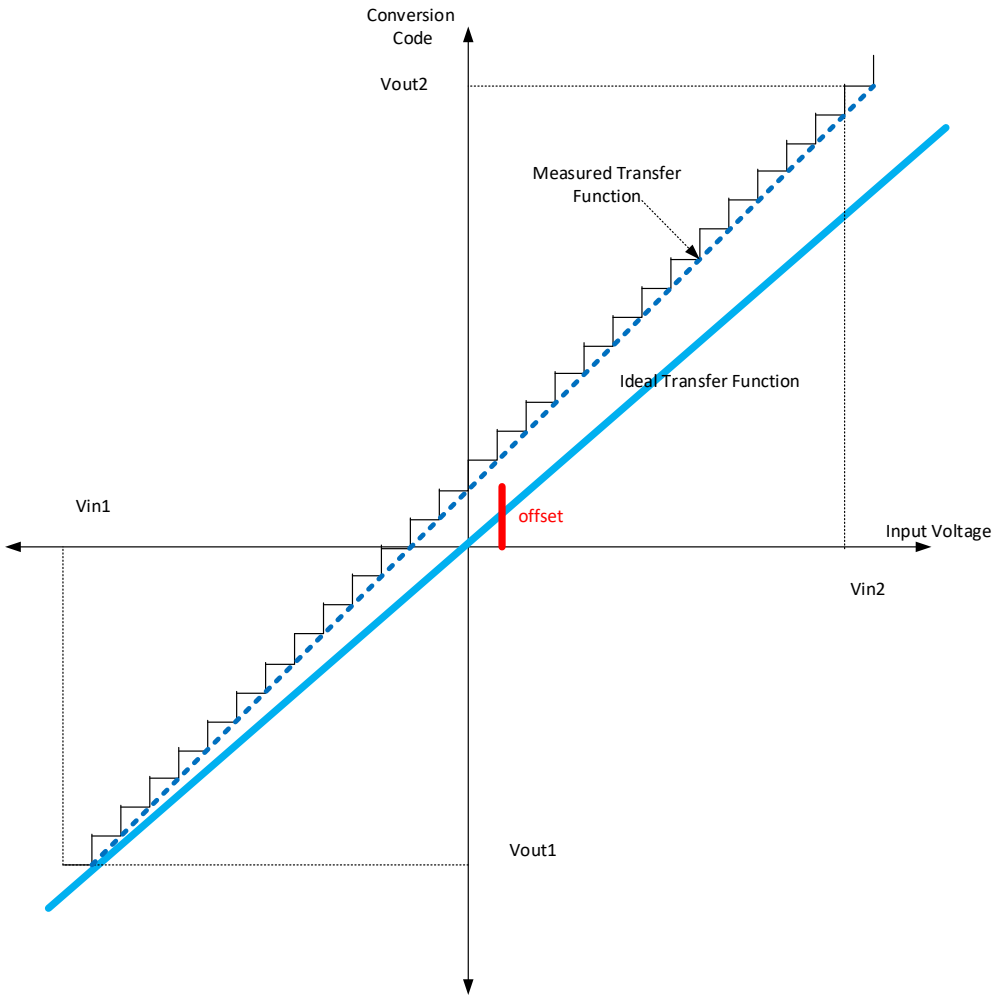


Figure 5.40: ADC Offset and gain error correction.

Digital interface

The device is configured to operate with 16 bit parallel hardware mode. The maximum achievable data throughput is 630KSPS. The data output format of the ADS8556 is binary twos complement. The access control of the ADC is performed by the FPGA. By offering simultaneous conversion of the 6 channels, the device is well suited to be

used in the 3-phase power system. The implementation is shown in Fig.5.41. This indicates that 12 analog to digital conversion can be performed simultaneously.

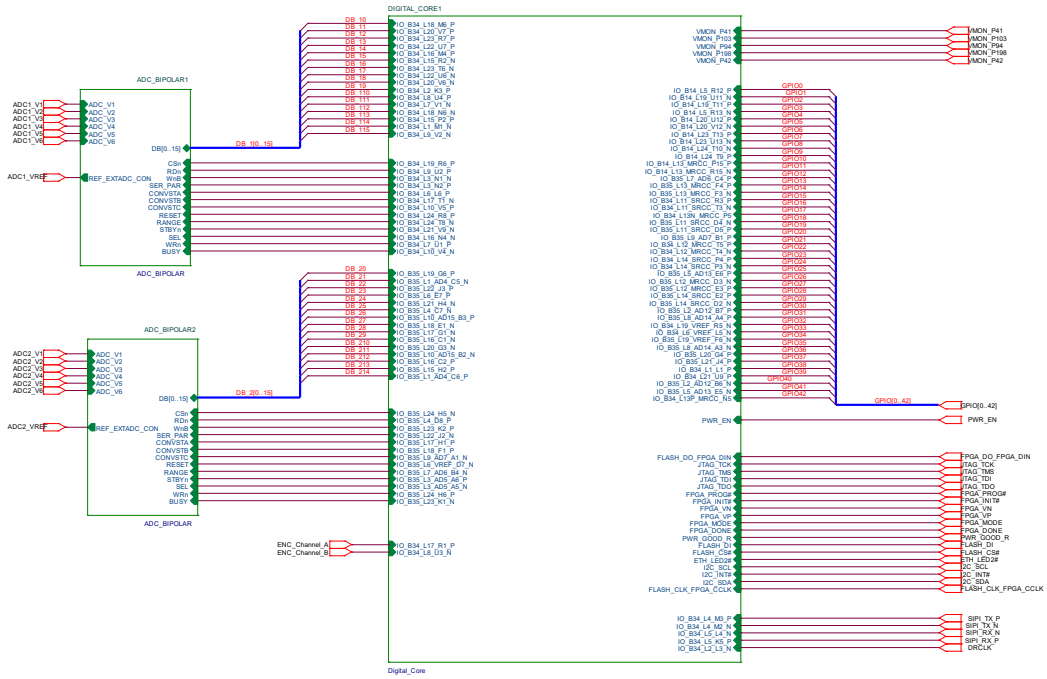


Figure 5.41: Connection of the ADC to the FPGA.

Anti aliasing filter implementation

The bandwidth and settling time requirements demanded of an in-amp buffering an ADC, and for the sample-and-hold function preceding it, can be quite severe. The input buffer must pass the signal along fast enough so that the signal is fully settled before the ADC takes its next sample. At least two samples per cycle are required for an ADC to unambiguously process an input signal (FS/2). This is referred to as the Nyquist criteria. Therefore, the 386Ks/s sampling of the ADS8556 requires that

the input buffer/sample-and-hold sections preceding it provide 15-bit accuracy at a 179KHz bandwidth. Settling time is equally important since the sampling rate of an ADC is the inverse of its sampling frequency for the 386KHz.

ADC, the sampling rate is 2.6 μs. This means that for a total throughput rate, these same input buffer/sample-and-hold sections must have a total settling time of less than 2.6 μs.

The primary benefit of an in-amp circuit is that it provides common-mode rejection. The AD8221 is well suited for this application because its high CMRR over frequency ensures that the signal of interest, which appears as a small difference voltage riding on a large sinusoidal common-mode voltage, is gained and the common-mode signal is rejected. In typical instrumentation amplifiers, CMRR falls off at about 200 Hz. In contrast, the AD8221 continues to reject common-mode signals beyond 10 kHz.

One very effective way to raise system resolution is to amplify the signal first, to allow full use of the dynamic range of the ADC. However, this added gain ahead of the converter will also increase noise. Therefore, it is often useful to add a low-pass filtering between the output of an in-amp (or other gain stage) and the input of the converter. Also, in most cases, the system bandwidth should not be set higher than that required to accurately measure the signal of interest. A good rule of thumb is to set the -3 dB cutoff frequency of the low-pass filter at 10 to 20 times the highest frequency that will be measured in the system. This low pass filter is shown in Fig.5.42 and is known as the anti-aliasing filter.

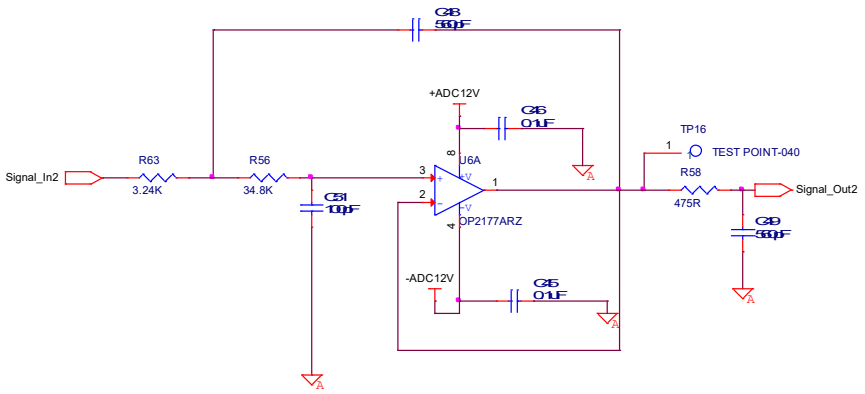


Figure 5.42: Anti-Aliasing filter schematic.

Analog front end

The front end circuit uses an instrumentation amplifier with a high common-mode rejection ratio. It features an extended frequency range over which the instrumentation amplifier has good common-mode rejection. The circuit consists one instrumentation amplifier and an antialiasing filter. The overall gain of the system can be determined by an external resistor.

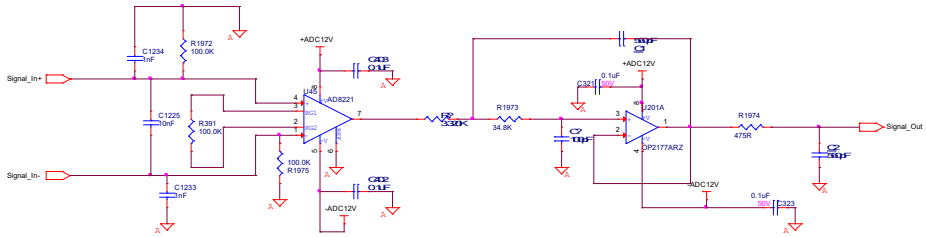


Figure 5.43: DC Offset removing OP-Amp.

EMI/ESD Protection

This EMI filter has TVS for protection against overvoltage by clamping the overvoltage to ±14V which is acceptable by the front end differential amplifier AD8221.

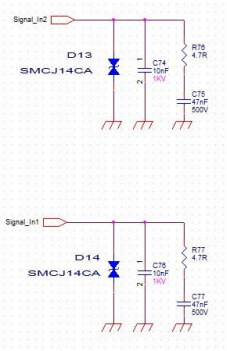


Figure 5.44: EMI and ESD protection schematic.

5.4.2 FPGA Functional modes

Several different modes are identified corresponding to different behaviors of the controller module. The transition from one mode to another is done upon software request. For this project, an "auto acquisition" mode is used to facilitate FPGA synchronization. The "auto acquisition" mode **shall** consist in the succession of operating sequences. The FPGA module shall launch its first operating sequence at the latest $28\mu s$ after the first rising edge.

5.4.3 Digital Connectors Block

The Digital_Connectors1 block is shown in Fig.5.45 and contains the following functions:

- JTAG connectors used for FPGA configuration.
- SPI connectors needed MCU and FPGA Inter-communications.
- Optional 43 discrete digital signals that can be configured as input or output for any control or status reporting to the FPGA or out of the FPGA.

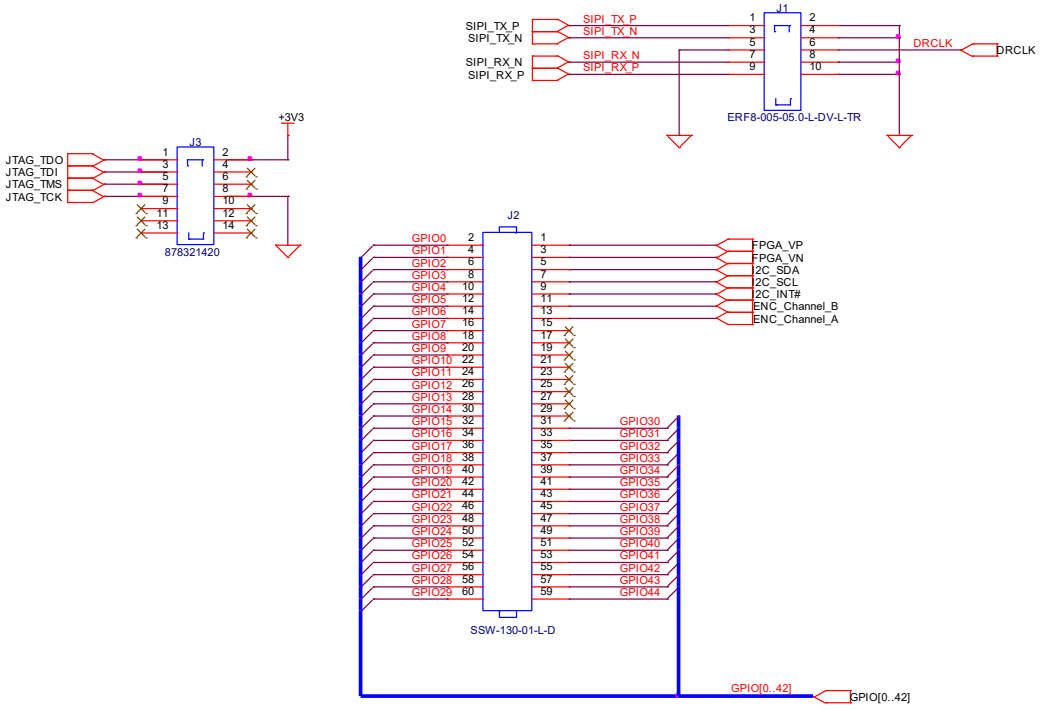


Figure 5.45: Digital connector block.

5.4.4 USB2SPI1: Voltage Monitoring Block

This block contains the 3.3V voltage supervisor and the status of the FPGA configuration. The implementation of the block is shown in Fig.5.46.

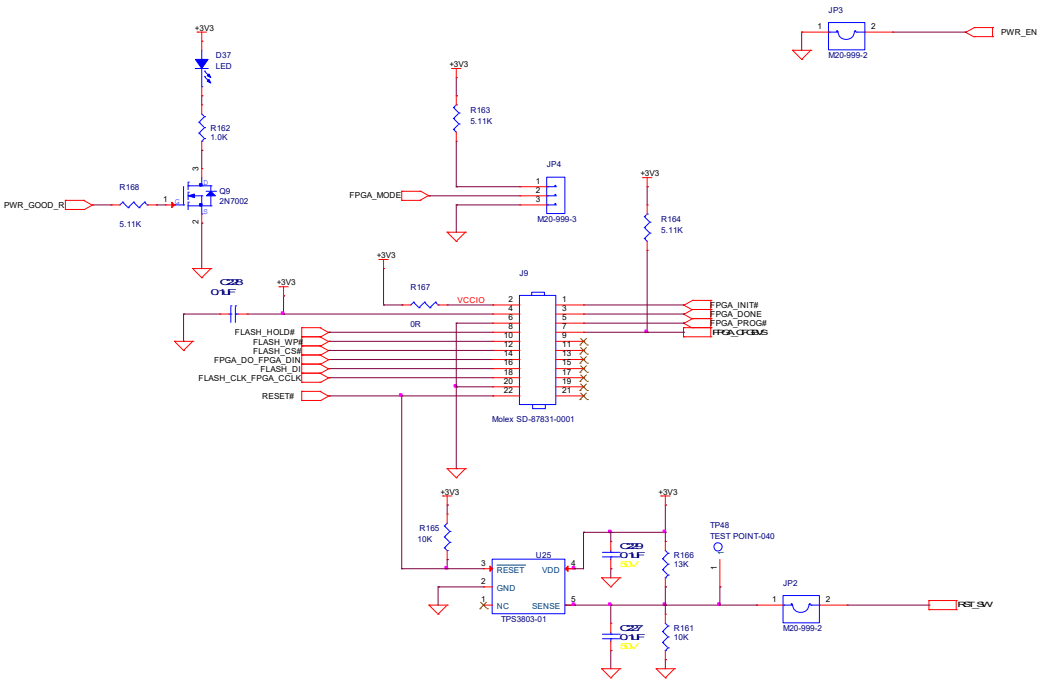


Figure 5.46: USB2SPI1: Voltage Monitoring Block.

5.4.5 CAN Interface

The CAN interface is shown in Fig.5.47. It is driven by the MPC5777m 512DS Daughter card.

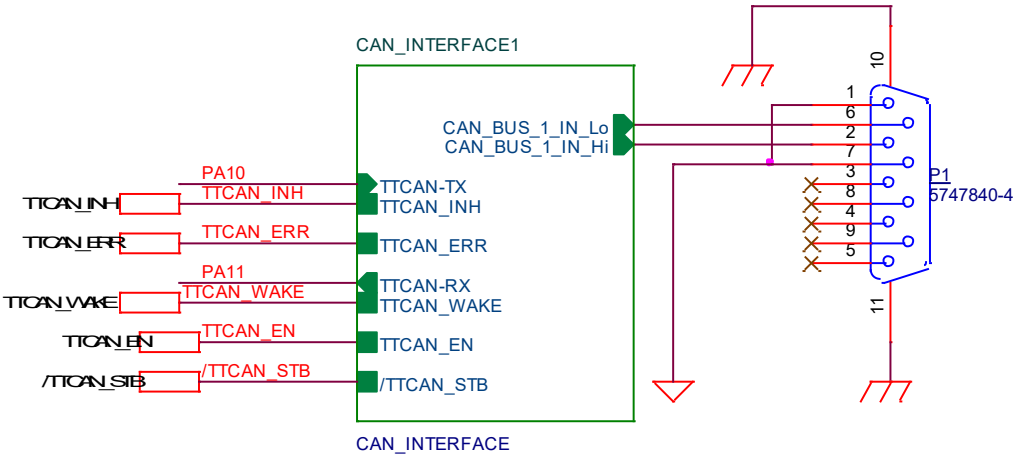


Figure 5.47: Controller Area Network Interface.

5.4.6 UART Interface

The UART interface is shown in Fig.5.48. This UART is an RS232 and is controlled by the MPC5777m 512DS Daughter card.

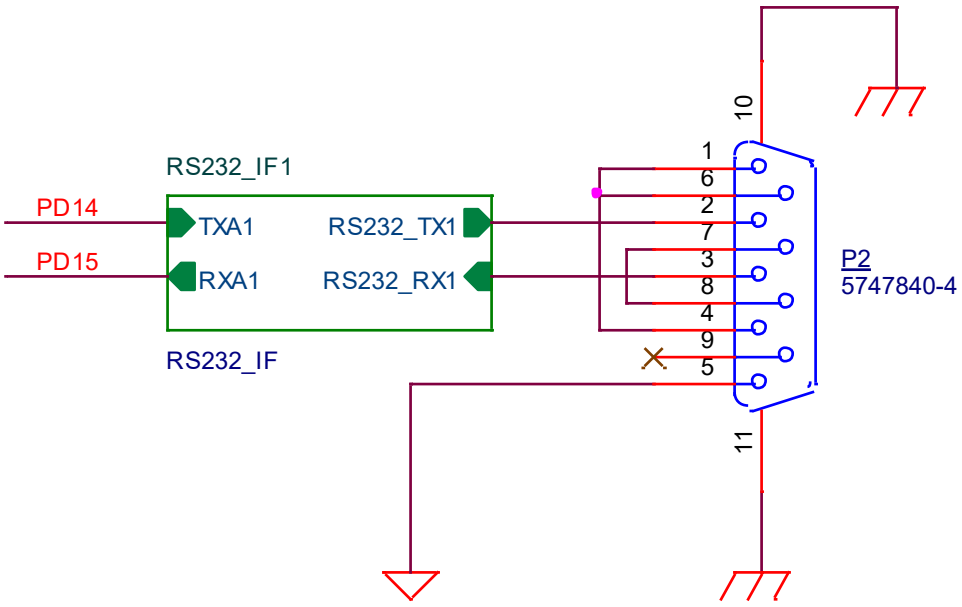


Figure 5.48: Universal Asynchronous Receiver/Transceiver Interface.

5.4.7 MPC5777m 512DS Daughter Card Interface

This block contains the MPC5777m 512DS Daughter card interface and is shown in Fig.5.49. The main functions are monitoring and communication.

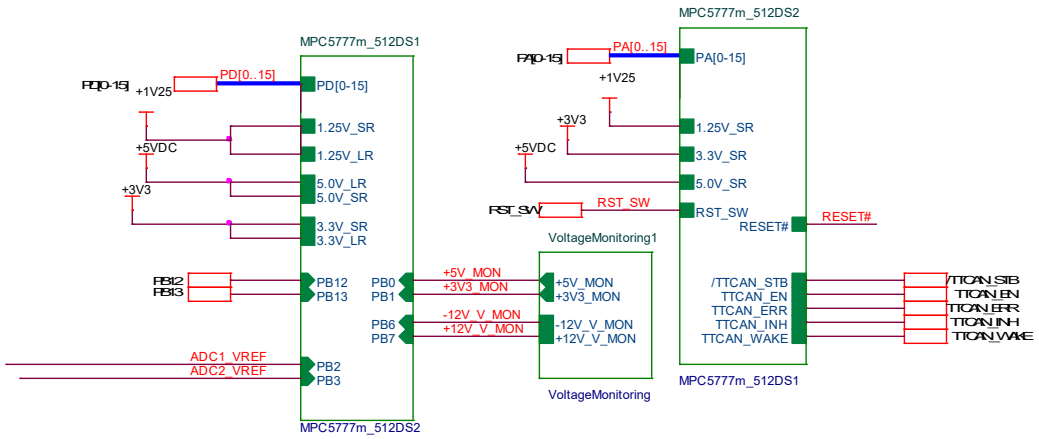


Figure 5.49: Power PC interface.

5.4.8 Detailed Description

CAN Bus interface

TJA1041 is a CAN transceiver that meets the specifications of the ISO11898-2 standard.

As a CAN transceiver, the device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps). The device is designed for operation in especially harsh environments, and it features cross-wire, overvoltage and loss of ground protection from –27 V to 40 V and over-temperature shutdown, as well as –12-V to 12-V common-mode range.

The TJA1041 is characterized for operation over the junction temperature range of –40°C to 150°C

The SMCJ Transil series has been designed to protect sensitive equipment against electrostatic discharges according to IEC 61000-4-2, and MIL STD 883, method 3015, and electrical over stress according to IEC 61000-4-4 and 5. These devices are more generally used against surges below 1500 W (10/1000 μups).

This CAN Interface between power PC (MPC5777m) microcontroller and J1 (X4J1KIT) connector is a connection between controller for off-the box communication using CAN bus interface from U6. The microcontroller contains three controller area network (FlexCAN) modules. Only one is used. FlexCAN module is a communication controller implementing the CAN protocol according to CAN Specification version 2.0B and ISO Standard 11898. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth.

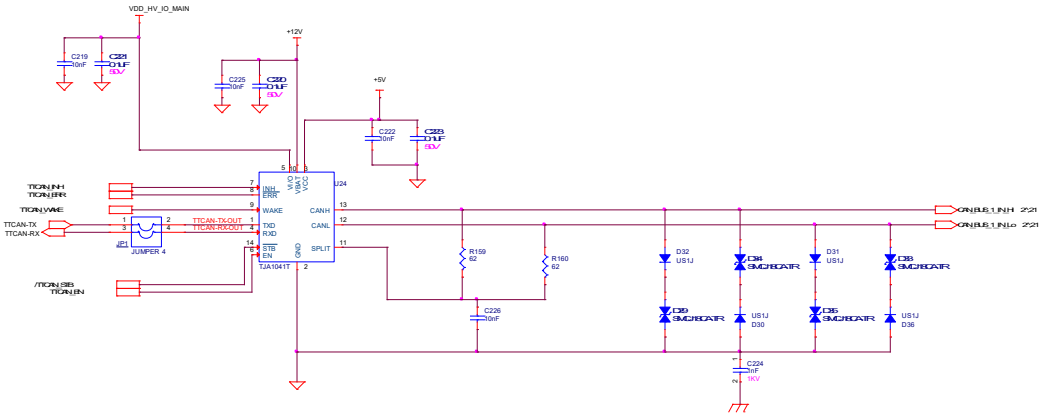


Figure 5.50: Controller Area Network (CAN) Bus Interface.

RS232 IF

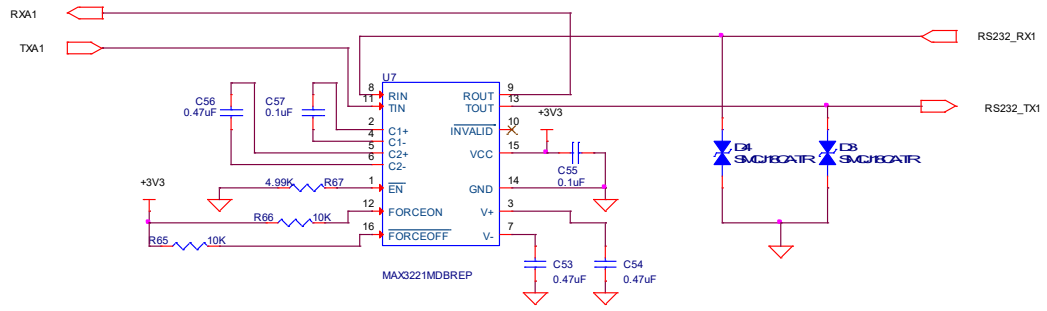


Figure 5.51: RS232 IF Schematic.

The MAX3221 consists of one line driver, one line receiver, and a dual charge-pump circuit with 15-kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. These devices operate at data signaling rates up to 250 kbit/s and a maximum of $30 - V/\mu s$ driver output slew rate.

The eSCI includes these distinctive features:

1. Full-duplex operation
2. Standard mark/space non-return-to-zero (NRZ) format
3. Configurable baud rate
4. Programmable 8-bit or 9-bit data format

5. LIN master node support

6. Configurable CRC detection for LIN

7. Separately enabled transmitter and receiver

8. Programmable transmitter output parity

9. Two receiver wake-up methods:

- Idle line wake-up
- Address mark wake-up

1. Interrupt-driven operation

2. Receiver framing error detection

3. Hardware parity checking

4. 1/16 bit-time noise detection

5. Two-channel DMA interface

The SMCJ Transil series has been designed to protect sensitive equipment against electrostatic discharges according to IEC 61000-4-2, and MIL STD 883, method 3015, and electrical over stress according to IEC 61000-4-4 and 5. These devices are more generally used against surges below 1500 W.

Chapter 6

An Optimized Supervisory Energy Management Controller

6.1 Optimization problem

The optimization problem is formulated to effectively split the source currents between the Li-ion battery and UC such that the load demand is met while minimizing the battery degradation. This is done by actively choosing the mode of operation of the MSI such that peak load currents are handled by the UC and constant current loads are handled by the battery. For a drive cycle's desired speed, $\{\omega_r(k), k = 1, ..., N\}$, and torque, $\{\tau_r(k), k = 1, ..., N\}$, the formulation of a multi-objective optimization problem is presented in this section through an offline implementation with DP to obtain the optimized MSI discharge duty cycle, D_c, at time-step k. The control frequency, f_c, is kept constant at 1kHz.

6.1.1 Problem formulation

The objective functions that are subjected to the optimization problem are shown in equations (6.1), (6.2) and (6.3).

$$f_1(k) = (i_{bat}^2(k)R_{bat} + i_{UC}^2(k)R_{UC})/P_{max} \tag{6.1}$$

$$f_2(k) = i_{bat}^2(k)/i_{bat,max}^2 \tag{6.2}$$

$$f_3(k) = (i_{bat}(k) - i_{bat}(k-1))^2/(\triangle i_{bat,max}^2) \tag{6.3}$$

Here, $P_{max} = 10kW$ is the maximum power loss, $i_{bat,max} = 100A$ is the maximum battery current and $\triangle i_{bat,max} = 10A$ is the maximum battery current fluctuation. R_{UC} is the internal resistance of the UC while R_{bat} is the internal resistance of the battery. The variable k is the current time step in the drive cycle. Equation (6.1) comprises of the system power losses. The power loss in each source is given by the changing internal resistance of the sources through ohms law. The power loss in the MSI is not considered since both paths of the DC sources in modes 1 and 3 are practically identical. Equation (6.2) represents the battery current magnitude and equation (6.3) represents the battery current fluctuations between time step k and $k-1$. A weighted sum of equations (6.1) - (6.3) can be formed and applied to the optimization problem for the necessary speed and torque references for one drive cycle as in equation (6.4).

$$\sum_{k=1}^{N} Af_1(k) + Bf_2(k) + Cf_3(k) \tag{6.4}$$

The constants A, B and C are chosen such that the biggest influence would be

the battery current magnitude and fluctuations. Regenerative braking is used with the mode selection of the MSI to recharge the UC whenever it dips below a certain SOC [91]. This is done since the UC will discharge much quicker than the Li-ion battery especially if it is used for all high-power demands [92]. This becomes a constraint in the optimization problem along with the maximum currents of each source. The UC is limited to a dip of 3% SOC from an 70% initial SOC to ensure sufficient energy is available during the whole drive cycle.

$$A + B + C = 1 \tag{6.5}$$

$$SOC_{UC}(k) > 67\% \tag{6.6}$$

$$|I_{bat}(k)| < 80A \tag{6.7}$$

$$|I_{UC}(k)| < 120A \tag{6.8}$$

From equations (6.5) to (6.8), a multi-objective optimization problem is formulated where D_c becomes the control variable. The optimization problem becomes the following for one drive cycle:

$$\begin{aligned} &\underset{D_c \in [0,1]}{\text{Minimize}} \quad (6.4) \\ &\text{subject to} \quad (6.5) - (6.8) \end{aligned} \tag{6.9}$$

6.1.2 Problem implementation

The multi-objective optimization problem has now been formulated to effectively split the current distribution between the UC and the battery while minimizing the battery wear from the load demanded. Dynamic Programming (DP) has been chosen as the

optimization algorithm. With DP, the data of the system must be known apriori to starting the algorithm. Fig.6.1 includes the flow chart used for the DP algorithm.

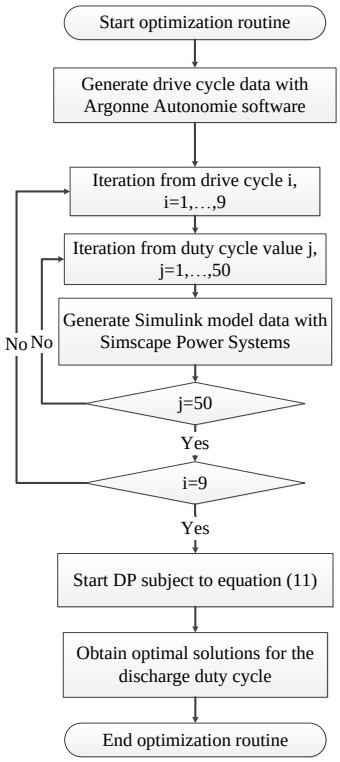


Figure 6.1: DP flow chart used to solve the multi-objective problem in equation (6.9).

The speed and torque from a single Toyota Prius PMSM reference data for nine drive cycles are generated with Argonne Autonomie Software [93]. The HESS-MSI model was then run in MATLAB Simulink with the nine reference drive cycles to generate a look up table of i_{UC}, i_{bat}, SOC_{UC}, R_{UC} and R_{bat} for discharge duty cycle values, D_c, spanning from 1% to 99% in steps of 2% inclusive. The DP algorithm is subjected to the optimization problem (6.9) to obtain the optimized D_c for the mode control of the HESS-MSI topology. A backward search to obtain an optimized solution for the optimization problem in equation (6.9) is then performed with the

look up tables generated through the MSI MATLAB Simulink model.

6.2 Neural Network Energy Management Controller

Due to the nature of DP having to know the whole drive cycle data apriori to obtain the optimized solutions, it cannot be used in real-time [41, 94–96]. By utilizing the learning nature of an Artificial Neural Network (ANN), it can learn the behaviour of the DP optimized solutions and be implemented for real-time control in the HESS-MSI system.

6.2.1 Neural Network controller

The NN-EMC is an ANN trained with the optimal duty cycles obtained through the DP algorithm as the target data. This ensures that the solutions obtained by the ANN will be within the testing error of the optimized solution [41]. The ANN is trained with the Scaled Gradient Method (SCG) method and the performance of the ANN is measured by the Mean Squared Error (MSE). The flow chart for the training of the Neural Network is shown in Fig.6.2. The architecture used for this Neural Network includes seven inputs, two hidden layers with ten neurons for the first hidden layer and five neurons for the second hidden layer and one output layer. The activation functions for each hidden layer is a Rectified Linear Unit (ReLU) function while the output layer has a linear activation function. The input data and the target data is sampled at 5kHz since the control frequency, f_c, is set to a constant 5kHz.

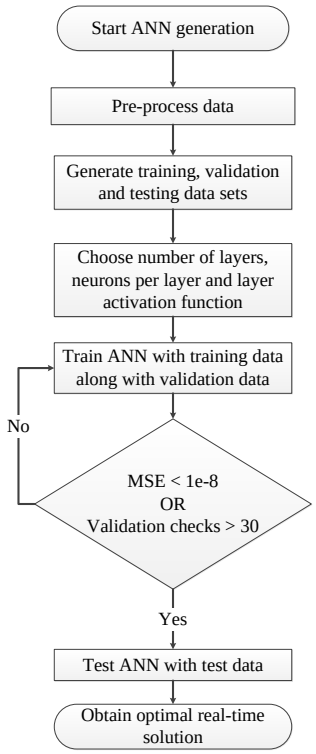


Figure 6.2: ANN training flow chart for real-time implementation of equation (6.9).

The ANN was trained with the MATLAB Neural Network Toolkit [97] until a Mean Squared Error (MSE) of 1e-8 was achieved or if more than 30 validation checks were done. The training was halted due to the 30 validation checks from the validation data set. From the Neural Network training, the Mean Absolute Error (MAE) and validating MAE were found to be 7.2% and 7.6% respectively from the optimized solution obtained with DP.

6.2.2 Simulation results

The NN-EMC's performance on the HESS-MSI system is now compared with the Battery-Only ESS, HESS-MSI system with a constant 50% discharge duty cycle and

with the optimized solution obtained with DP. The speed and torque control is done through the adapted SVPWM algorithm for the MSI mentioned in [36].

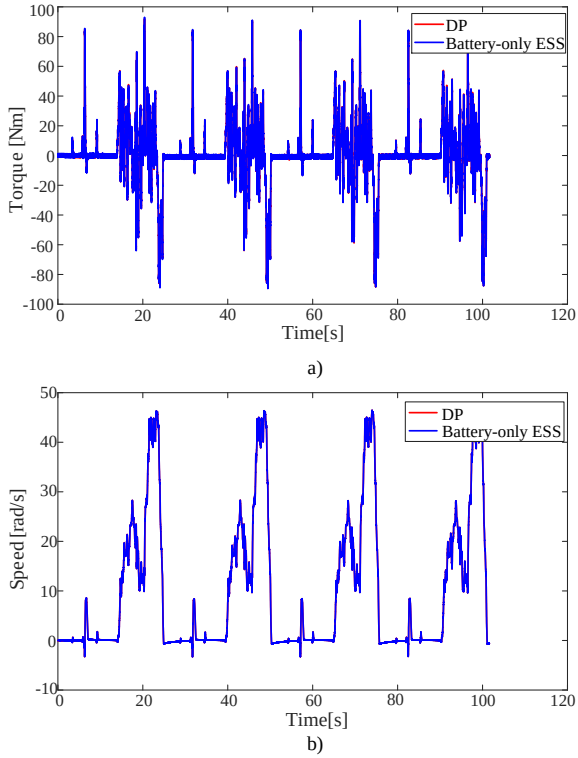


Figure 6.3: Speed-torque control of the motor for New York City drive cycle. a) Speed control and b) Torque control.

The resultant speed and torque control results are shown in Fig.6.3 for the DP optimized solutions. It can be seen that the control system closely follows the speed control of the Battery-Only ESS without having the DP solutions affecting the speed and torque control.

The trained ANN controller was used over the New York City testing drive cycle. The peak current magnitudes and mean absolute currents of both sources are shown in table 6.1 for the Battery-Only ESS, constant 50% HESS-MSI, DP optimized solutions

Table 6.1: Battery an UC currents results for New York City drive cycle.

Quantities	Battery-Only ESS	HESS-MSI ($D_c = 50\%$)	DP	NN-EMC
Battery Current Mean Magnitude (A)	3.09	1.59	2.05	1.72
Battery Current Max Magnitude (A)	66.77	39.75	56.44	37.91
UC Current Mean Magnitude (A)	N/A	1.67	1.20	1.53
UC Current Max Magnitude (A)	N/A	43.88	76.24	81.09

and the NN-EMC real-time control. The NN-EMC achieves a mean absolute battery current of 1.72A while the DP algorithm achieves a mean absolute battery current of 2.05A. The peak current in the battery was found to be 37.91A which is lower than the DP optimized solutions. This is due to the fact that the ANN does not consider the UC SOC as strongly as the DP optimized solutions. This can be seen in table 6.2 where the SOC of both sources are shown for the same test drive cycle. It can be seen that the UC is used more often than the battery whenever its SOC is not below 67%. The resultant battery and UC currents for the NN-EMC are shown in Fig.6.5.

It can be seen that the mean absolute battery current is roughly 65% of the mean absolute UC current, making the SOC of UC decrease much quicker than that of the

Table 6.2: Battery and UC SOC results for New York City test drive cycle.

Quantities	Battery-Only ESS	HESS-MSI ($D_c = 50\%$)	DP	NN-EMC
Battery SOC (%)	89.72	89.85	89.81	89.84
Battery SOC Change (%)	0.27	0.14	0.18	0.15
UC SOC (%)	N/A	66.85	67.74	67.20
UC SOC Change (%)	N/A	3.14	2.25	2.79

battery. Although the SOC of the UC decreases quicker, the NN-EMC includes regenerative braking for UC recharging such that an acceptable SOC of 67% is achieved.

It can be noted that the Neural Network UC SOC diverges further than expected from the DP optimized solutions. This is due to the cumulative errors when approximating the SOC because it is estimated as an integral of the current [38,92,98]. Since 100000 sample data are taken, the error between the ANN and DP will accumulate within the sample data as shown in Fig.6.6-b.

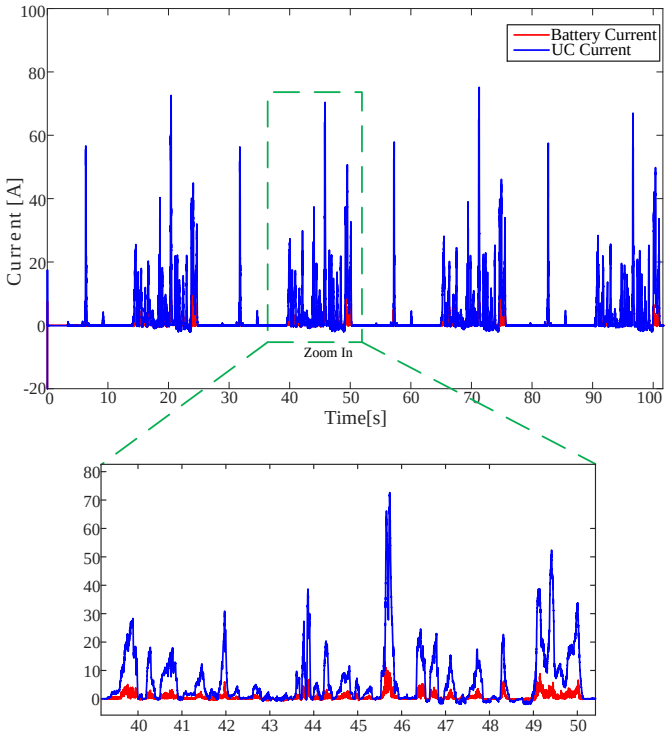


Figure 6.4: DP optimized results for output current of battery and UC for New York City drive cycle.

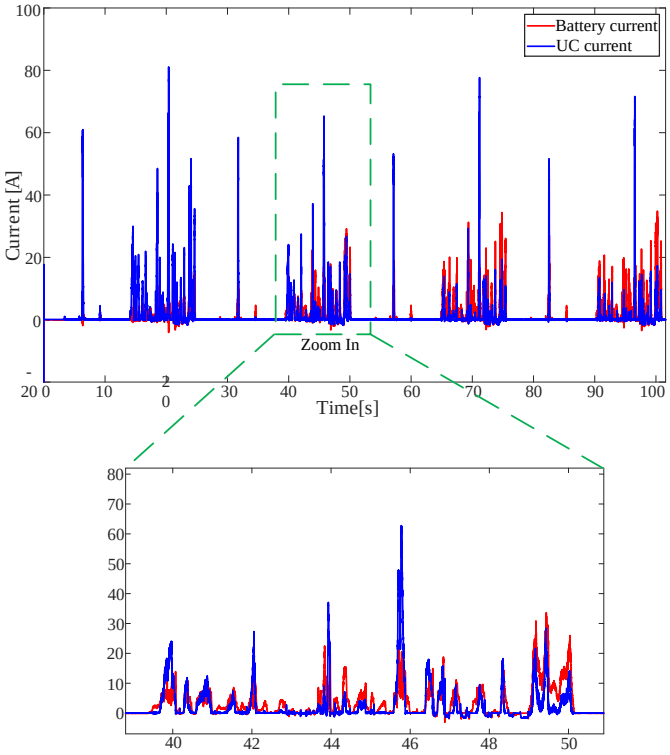


Figure 6.5: NN-EMC results for output current of battery and UC for New York City drive cycle.

Both the Battery SOC and UC SOC for each scenario are shown in Fig.6.6-a and Fig.6.6-b with respective initial values of 90% and 70%. The final SOC of each run is shown in table 6.2. The final SOC of both sources can give an idea on which source is being used the most and to see if the UC stays within the constraint such that sufficient power is available at all times.

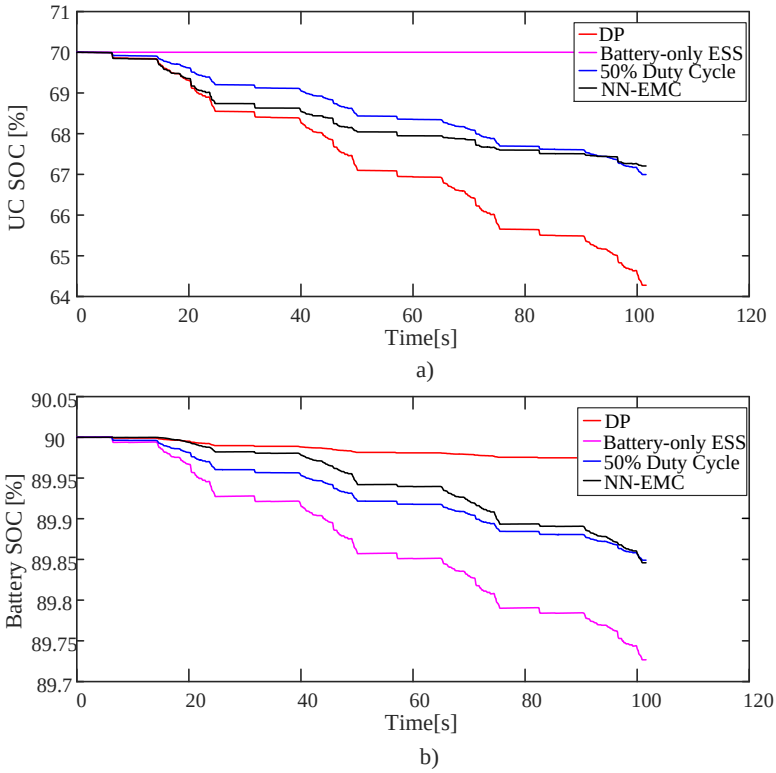


Figure 6.6: Sources SOC for New York City drive cycle: a) Battery SOC b) UC SOC

Chapter 7

Experimental Verification

7.1 Board bring up

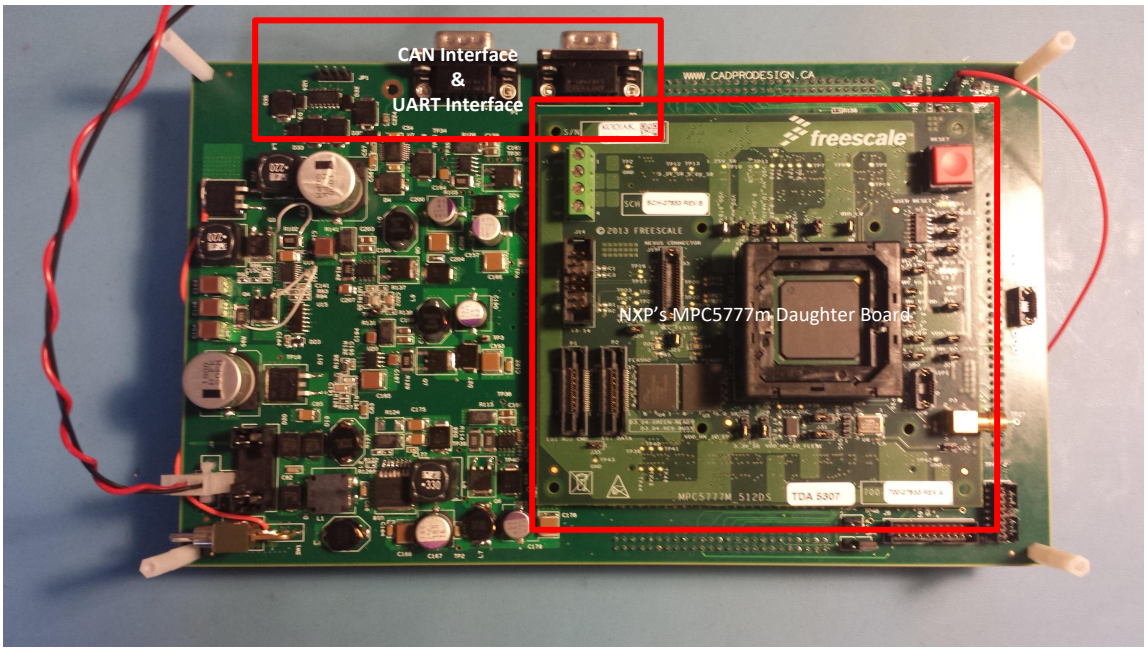


Figure 7.1: Finished Controller board

The board was designed with the help of CADProDesign [99]. A collboration was done to bring up the board to functionality and to ensure a smooth manufacturing process of the PCB board and component placement. A Modular design approach was used to ensure re-usability of implemented traces and footprints and re-usability of design.

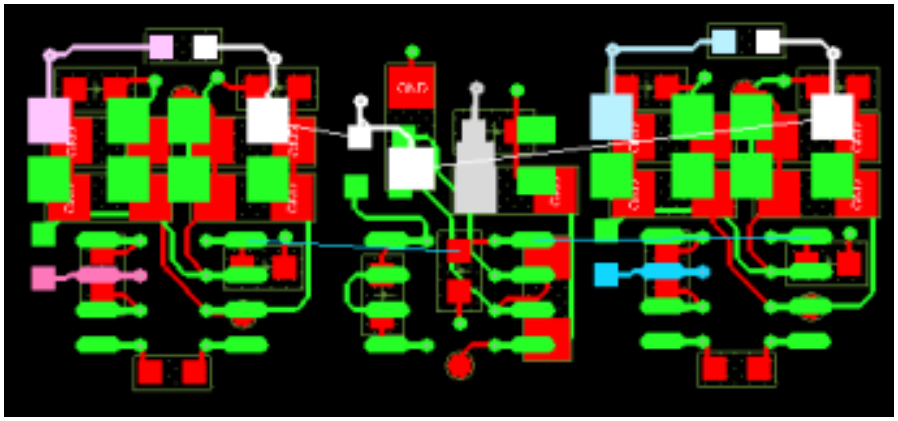


Figure 7.2: Modular PCB Layout

The board designed is a 10 layer board. Multiple layers were used to ensure the integrity of signals on the board. Local and global ground planes are set on the board. Fig.7.3 shows the layout of the power planes of the board. The software used to design the PCB layout was OrCad Allegro [100].

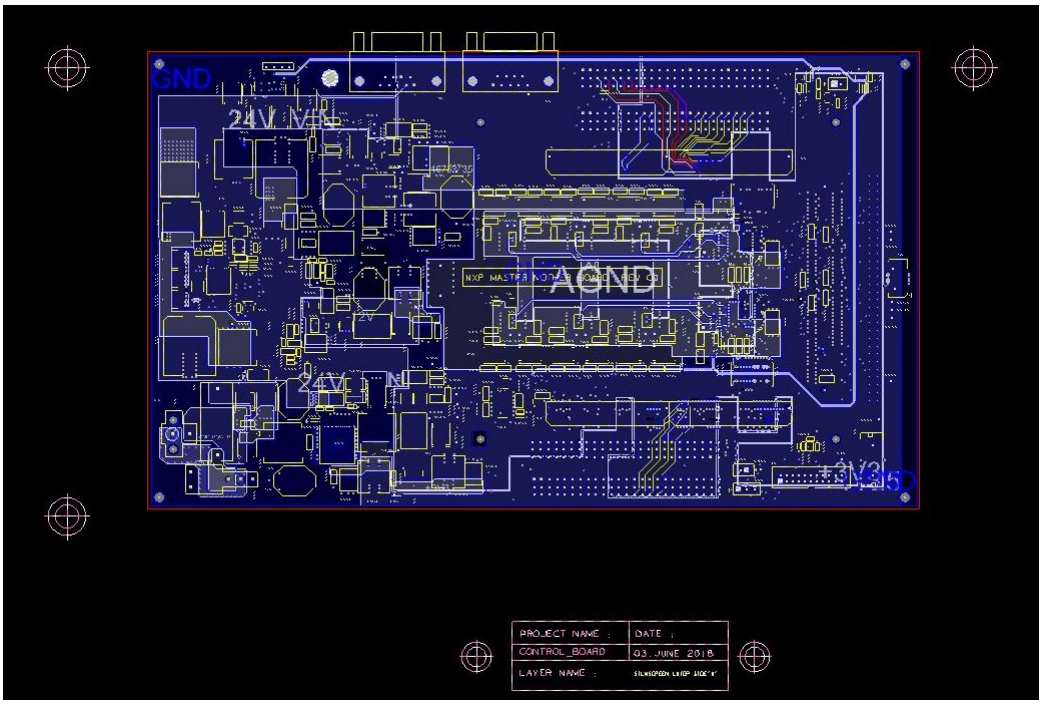


Figure 7.3: PCB Layout of Power, Power Ground, Analog Ground and Digital Ground planes.

Each component block listed in Fig.5.1 has been highlighted in Fig.7.4 for the top and for the bottom view in Fig.7.5.

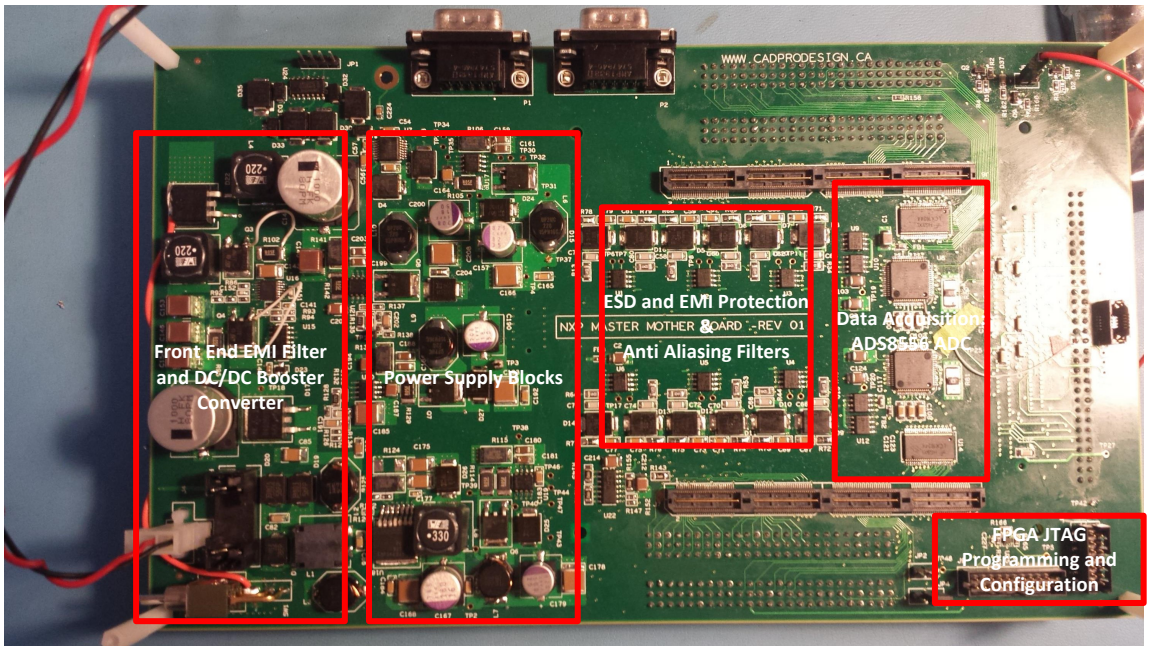


Figure 7.4: Top of the Control Board without MPC5777m

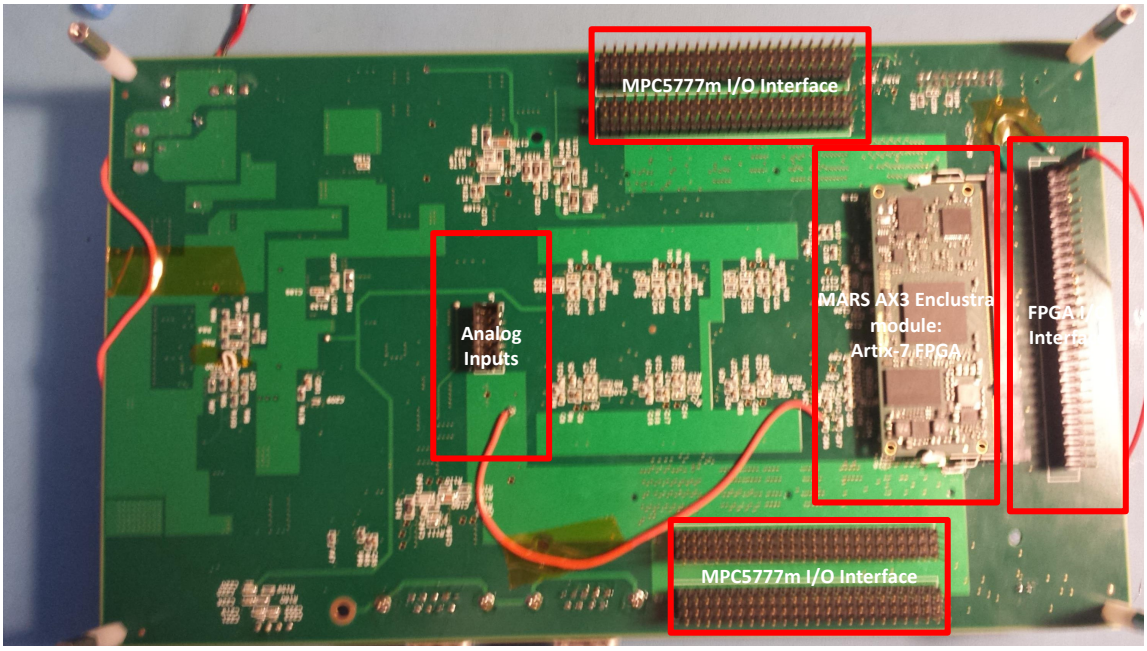


Figure 7.5: Top of the Control Board without MPC5777m

7.2 Power Supplies Verification

7.2.1 Front End Power Supply Verification

This section shows the experimental results of the front end DC/DC Boost converter power supply. The transients of the external power on supply is shown in Fig.7.6. The results show a smooth transition from a 12V supply to a 16Vdc internal supply to the auxiliary power supplies. The current, input voltage and output voltages are shown. As can be seen, the output voltage has a soft-start to ensure limited current at start-up of the board.

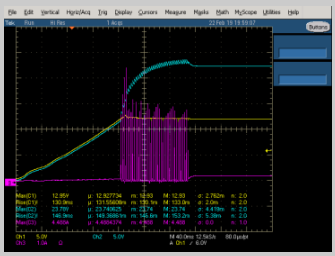
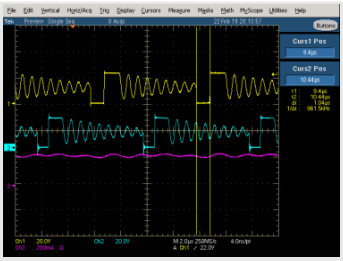
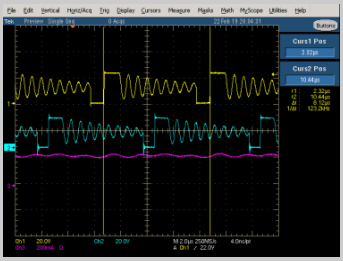
	Switching Waveforms	Results
Booster at power on		Current limit Output voltage Power ON
		Reverse recovery-induced oscillation in Rectifier
		

Figure 7.6: DC/DC Boost converter during power on experimental results. The purple waveform shows the input current, the blue waveform shows the output voltage and the yellow waveform shows the input voltage.

As mentioned in the simulation validations of the front end DC/DC boost converter, the switching oscillations can be avoided by reducing the efficiency but ensuring a good EMI performance by adding an RC network in parallel with the boost

converter. The oscillations are minimized with the added components but the efficiency of the system will be affected negatively. This is verified and shown in Fig.7.7.

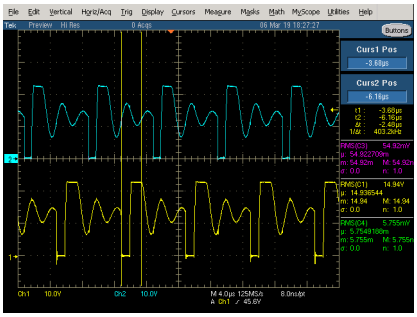
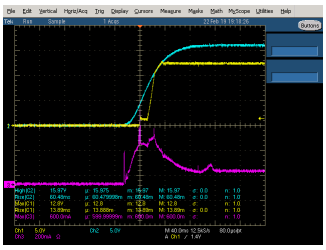
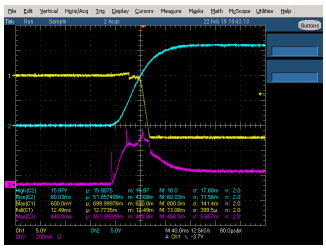


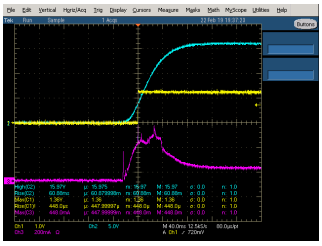
Figure 7.7: RC Snubber added in parallel with the rectifier experimental results.

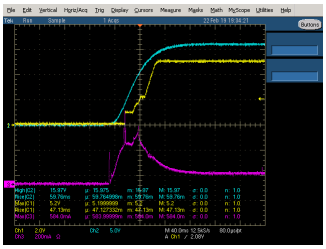
7.2.2 Auxiliary Power Supply Verification

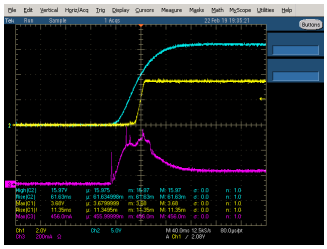
This section demonstrates the verification of the auxilirary power supplies needed to pwoer the components on the board. All the auxiliary power supplies are verified against the requirements. Each have a soft start feature except for the 1.25V power supply. Experimental results are shown for the +12VDC, -12VDC, 5VDC, 3.3VDC and 1.25VDC in Fig.7.8 with the results obtained from a multimeter. The waveform in purple is the input current of the total control board, the blue waveform shows their respective input voltage of 16V and the yellow waveforms demonstrates the output voltage of the respective power supply.


a)


b)


c)


d)


e)

Power Supply Units	Mean	Max
+12V	12.1V	12.8V
-12V	-12.1V	-12.8V
5V	5.05V	5.19V
3.3V	3.34V	3.68V
1.25V	1.28V	1.36V

f)

Figure 7.8: Experimental Results for: a) +12VDC Power supply b) -12VDC Power Supply c) 1.25V Power Supply d) 5V Power Supply e) 3.3V Power Supply and e) The mean voltage during steady state and maximum transient voltage

7.3 Automated FPGA verification for DAL-A design

As mentioned in the introduction, an fully automated test bench for FPGA verification will decrease both the schedule time and development costs of designing a system with FPGA. The automated test bench created for this project is shown in Fig.7.9. It comprises of a logic analyzer, the control board, current sensors, inverter and an RL load to measure some type of physical parameters which is in this case a sinusoidal phase current.

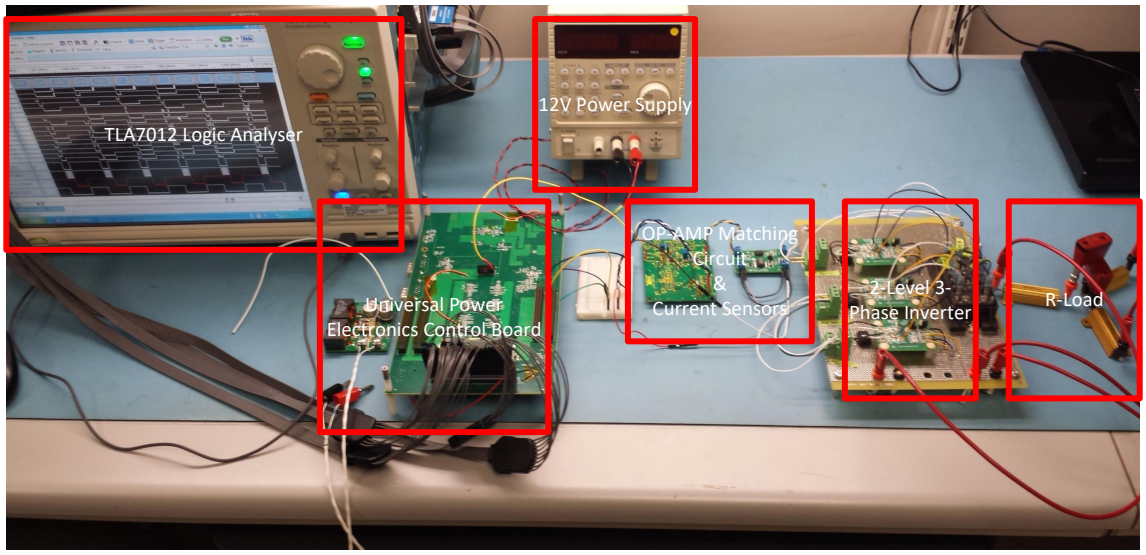


Figure 7.9: Test Bench for Automated FPGA design verification

7.3.1 Requirements

The requirements are listed below to ensure completeness of the design process:

- **MASc_Req_ADC1**: The ECU **shall** provide an interface according to the functional requirements and constraints of the ADS8556 data sheet [101]. The expected results for timing are shown in table 7.3. A timing diagram is as well shown in Fig.7.10.
- **MASc_Req_ADC2**: The ADC **shall** operate in parallel mode.
- **MASc_Req_ADC3**: The ADC **shall** be configured using the external pins as shown in Table 7.1 using the FPGA Interface.
- **MASc_Req_ADC4**: The ECU **shall** operate in "Auto Acquisition" mode consisting in the succession of multiple acquisitions. Table **??** shows the expected

Table 7.1: ADS8556 Input/Output register states during reset.

Output Name	**Expected Outcome**
PRE_ADC_RANGE	0
PRE_WORD_N_BYTE	0
PRE_SER_PAR_N	0
PRE_STBY_N	1
PRE_HW_N_SW	0
PRE_WRITE_N	0
PRE_RESET	1
PRE_CONVERST_A	0
PRE_CONVERST_B	0
PRE_CONVERST_C	0
PRE_READ_N	1
PRE_CS_N	1

results of the auto acquisition timing of certain signals.

- **MASc_Req_ADC5**: The periodicity of the auto acquisition signal "Sample_Strobe" **shall** be 2.6±12.5μs

Now with these requirements, a test procedure must be followed to ensure that the requirements are tested and verified appropriately. The automated test bench is used in concurrence with MATLAB to ensure a fully automatic verification testbench.

7.3.2 Test procedure

This verification is organized as follows:

Step 1: Setup the test environment to start Auto Acquisition sequence and check external component configuration registers during Reset:

Expected Results (**MASc_Req_ADC1**, **MASc_Req_ADC2**, **MASc_Req_ADC3**):

Step 2: Check Start of Auto Acquisition Timing Sequence.

Table 7.2: Auto Acquisition timing Requirements.

Output Name	**Expected Outcome**
PRE_CONVST_A	2.6±0.0125 μs
PRE_CONVST_B	2.6±0.0125 μs
PRE_CONVST_C	2.6±0.0125 μs
CLKOUT	25±1 ns
sample_strobe	2.6±0.0125 μs

Step 2.1: Check the time between the falling edge of sample_strobe and rising edge of PRE_CONVST_A, PRE_CONVST_B and PRE_CONVST_C is 1 Clock Cycle (40MHz Clock Frequency).

Step 2.2: Check the time that PRE_CONVST_A, PRE_CONVST_B and PRE_CONVST_C is logic high.

Step 2.3: Check that sample_strobe pulse is generated to logic high every 104 Clock cycles (40MHz Clock Frequency)

Step 2.4: Check the Clock Management Interface Timing

Expected results (MASc_Req_ADC4, MASc_Req_ADC5):

Step 3: Check Functionality of ADS8556 ADC.

Table 7.3: ADS8556 Timing Requirements.

Timing Name	**Expected Outcome**
t_{acq}	280 ns Minimum
t_1	20 ns Minimum
t_2	0 ns Minimum
t_4	0 ns Minimum
t_6	30 ns Minimum
t_7	10 ns Minimum

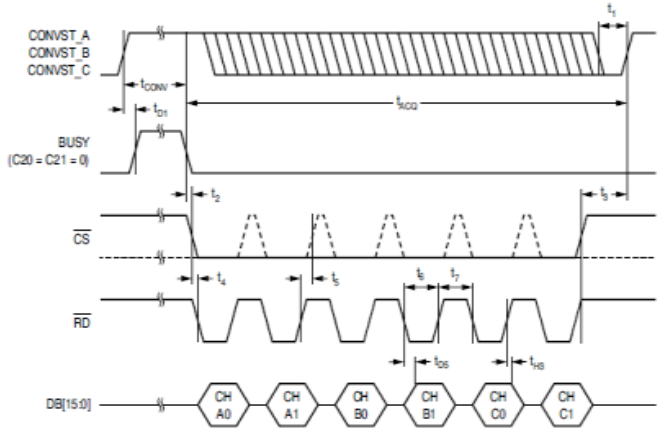


Figure 7.10: Timing requirements for functionality of the ADS8556 ADC

Step 3.1: Check the necessary timing and functionality of the ADC shown in Fig.7.10.

Expected result (MASc_Req_ADC1):

Physical Verification procedure steps

Step 1: Setup the test environment to start Auto Acquisition sequence and check external component configuration registers during Reset.

- Step 1.1: Turn on main power on the test unit;
- Step 1.2: Trigger on PRE_RESET Falling edge;
- Step 1.3: Press Run on the TLA7012 Logic Analyser;
- Step 1.4: Press the List tab to create a list in a tabular format;
- Step 1.5: Save the list as "MASc_Control_Board_Physical_Timing_Verification.txt" from the dropdown menu file;
- Step 1.6: Export the file onto a memory stick ;
- Step 1.7: Load file into the following MATLAB Directory:
- Step 1.8: Open the MATLAB Script "MASc_Control_Board_Physical_Timing_Verification_Script.m" and press RUN;
- Step 1.9: Check the first values of each signal listed in table 7.1 while the ECU is in reset.

Expected Results(See table 7.1):

Step 2: Check Start of Auto Acquisition Timing Sequence.

- Step 2.1: Check the time between the falling edge of sample_strobe and rising edge of PRE_CONVST_A, PRE_CONVST_B and PRE_CONVST_C is 1 Clock Cycle (40MHz Clock Frequency).
  - Step 2.1.1: Measure the time of the falling edge of sample_strobe.
  - Step 2.1.2: Measure the time of the successive rising edge of PRE_CONVST_A, PRE_CONVST_B and PRE_CONVST_C.

  - Step 2.1.3: Check the difference in time between both measurements.

- Step 2.2: Check the time that PRE_CONVST_A, PRE_CONVST_B and PRE_CONVST_C is logic high.
  - Step 2.2.1: Measure the time of the rising edge of PRE_CONVST_A, PRE_CONVST_B and PRE_CONVST_C.
  - Step 2.2.2: Measure the time of the successive falling edge of PRE_CONVST_A, PRE_CONVST_B and PRE_CONVST_C.
  - Step 2.2.3: Check the difference in time between both measurements.
- Step 2.3: Check that sample_strobe pulse is generated to logic high every 104 Clock cycles (40MHz Clock Frequency).
  - Step 2.3.1: Measure the time of the rising edge of sample_strobe.
  - Step 2.3.2: Measure the time of the next rising edge of sample_strobe.
  - Step 2.3.3: Check the difference in time between both measurements.
- Step 2.4: Check the Clock Management Interface Timing
  - Step 2.4.1: Measure the time of the rising edge of CLKOUT.
  - Step 2.4.2: Measure the time of the next rising edge of CLKOUT.
  - Step 2.4.3: Check the difference in time between both measurements.
  - Step 2.4.4: Measure the time of the rising edge of sample_strobe.
  - Step 2.4.5: Measure the time of the next rising edge of sample_strobe.
  - Step 2.4.6: Check the different in time between both measurements.

- Step 2.4.7: Measure the time of the rising edge of PRE_CONVST_A, PRE_CONVST_B and PRE_CONVST_C.
- Step 2.4.8: Measure the time of the next rising edge of PRE_CONVST_A, PRE_CONVST_B and PRE_CONVST_C.
- Step 2.4.9: Check the difference in time between both measurements.

Expected result(See table 7.2):

Step 3: Check Functionality of ADS8556 ADC.

- _Step 3.1: Check the necessary timing and functionality of the ADC shown in figure 1.
  - Step 3.1.1: Measure the time of the falling edge of PRE_BUSY.
  - Step 3.1.2: Measure the time of the successive rising edge of PRE_CONVST_A, PRE_CONVST_B and PRE_CONVST_C.
  - Step 3.1.3: Check the difference in time between both measurements. The difference should correspond to t_{acq} expected result.
  - Step 3.1.4: Measure the time of the falling edge of PRE_CONVST_A, PRE_CONVST_B and PRE_CONVST_C.
  - Step 3.1.5: Measure the time of the successive rising edge of PRE_CONVST_A, PRE_CONVST_B and PRE_CONVST_C.
  - Step 3.1.6: Check the difference in time between both measurements. The difference should correspond to t_1 expected result.
  - Step 3.1.7: Repeat step 3.1.1.
  - Step 3.1.8: Measure the time of the falling edge of PRE_CSn.

- Step 3.1.9: Check the difference in time between both measurements. The difference should correspond to t_2 expected result.
- Step 3.1.10: Repeat step 3.1.8.
- Step 3.1.11: Measure the time of the successive falling edge of PRE_READ_N.
- Step 3.1.12: Check the difference in time between both measurements. The difference should correspond to t_4 expected result.
- Step 3.1.13: Measure the time of the falling edge of PRE_READ_N.
- Step 3.1.14: Measure the time of the successive rising edge or PRE_READ_N.
- Step 3.1.15: Check the difference in time between both measurements. The difference should correspond to t_6 expected result.
- Step 3.1.16: Measure the time of the rising edge of PRE_READ_N.
- Step 3.1.17: Measure the time of the successive falling edge of PRE_READ_N.
- Step 3.1.18: Check the difference in time between both measurements. The difference should correspond to t_7 expected result.

Expected result(See table 7.3)

Results: The test report is generated by a Matlab script tha emulates the behavior of the system. The waveforms from TLA are examined by the tester. A failure is reported if the waveform is not correct. The waveforms obtained from the logic analyzer are shown for one ADC conversion cycle in Fig.7.11. A full auto acquisition cycle is shown in Fig.7.12.

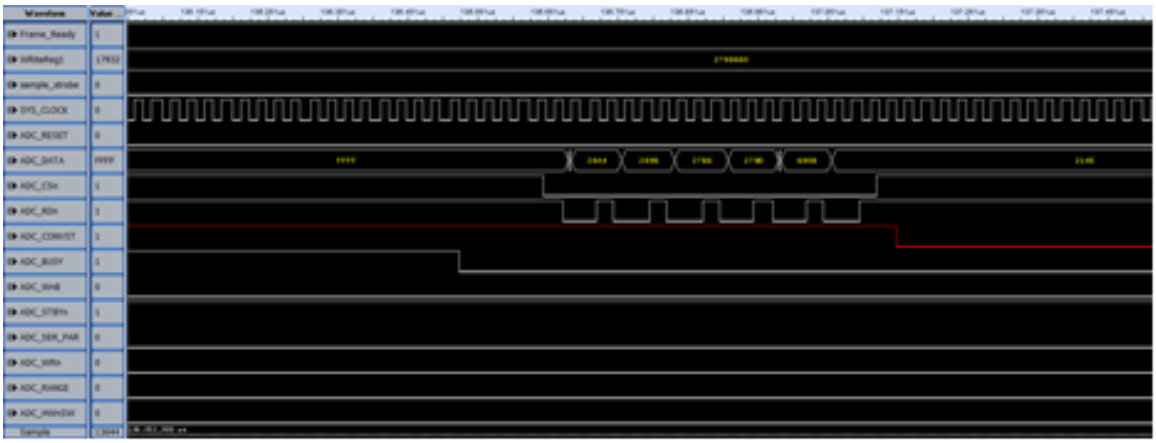


Figure 7.11: Logic Analyzer zoomed waveform for ADS8556 requirement verification.

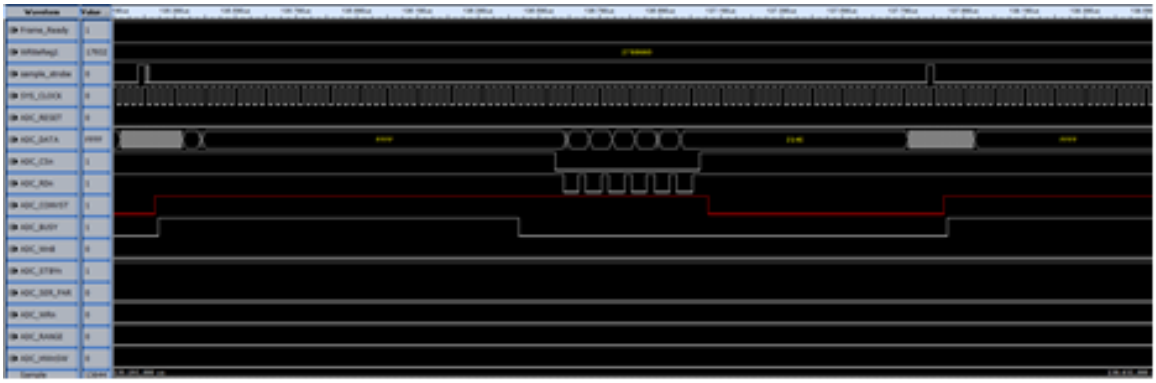


Figure 7.12: Logic Analyser Waveform for auto acuisition mode verification.

The test results show that the FPGA tests have all passed within the specified requirements. The verification matrix results are shown in the Appendix as Fig.A.1 which show all requirements were passed. This is the artifact needed to be able to certify your hardware design efficiently, safely and by keeping a low cost to development.

Chapter 8

Conclusions and Future Work

8.1 Conclusion

The time and resources limit for a Master of Science thesis has contributed to the fact that a complete verification process could not be done at a system level. Instead methods of verification for FPGA and recommendations for verifying a real project on a hardware and FPGA level is presented. The DO-254 guidelines are followed to ensure the safety and functional requirements of the hybrid FPGA/MCU control board are met. Verification artifacts have been produced with a pass or fail criteria to ensure traceability is found within the design process. As well, the DO-160 has been followed to produce hardware requirements during the control board design process to have a pass or fail criteria before testing in a credited DO-160 laboratory.

Furthermore, a NN-EMC was designed for a HESS using the MSI topology. A power split multi-objective optimization problem was formulated to limit the battery wear and to limit the power losses in the UC and Li-ion Battery input sources. DP was used to solve the multi-objective optimization problem and it obtained optimized

solutions to minimize the battery wear by limiting the peak current through the battery and to minimize the fluctuations of the battery current. For real-time application of the DP optimized solutions, an ANN has been designed. The ANN was taught the optimized solutions obtained by DP and received a testing error of 8.7% for NYC drive cycle. It was found that the NN-EMC results had a 50% current peak shaving ability and 50% RMS battery current reduction from the battery-only ESS.

8.2 Future Work

Further work can be performed by generating a second output of the NN-EMC to chose at which control frequency, f_c, the system is more efficient. This will help to improve the efficiency of the HESS-MSI by actively changing the control frequency to obtain minimal power losses while minimizing battery wear.

Future work consisting of the control board includes the following:

- Implementing the optimized energy management controller onto the control board.
- Developing the BIST in software on the MPC5777m with the DO-178 process.
- Verify experimentally the following DO-160 tests performed in simulation:
  - Power line pin injection experimental tests
  - RF Conducted Susceptibility experimental tests
  - RF Conducted Emissions experimental tests
- Development of Automated Test Procedure for the final product requirement verification and validation.

- Development of Revision 2 of the Control Board with the review artifacts created from revision 1

Appendix A

Appendix

```
        MatLabScript                =    MASc_TestProcedure_ADC.m
        Board SN#                   =    1
        Firmware                    =    1
        Logic Analyzer File Name    =    MASc_TEST_PROC.txt
        Tester name                 =    John Ramoul
        Verifier name               =    Verifier1
        DATE                        =    12-February-2019 19:36:40
```

Name: MASc Requirements Testing	Type:Physical Verification	Identifier: CCRD_Mcmaster_PHY_Timing

Step 1: Setup the test environment to start Auto Acquisition sequence

Traceability	Name	Test Procedure Step	Criteria Result	Expected (s)	± TOL	Received (s)
Setup the test environment	Start Auto Acquisition sequence	Step 1	N/A	N/A	N/A	N/A
Setup the test environment	Turn main power on test unit	Step 1.1	N/A	N/A	N/A	N/A
TLA7012 Logic Analyser	Trig. on PRE_RESET Falling edge	Step 1.2	N/A	N/A	N/A	N/A
TLA7012 Logic Analyser	Press Run ON the TLA7012	Step 1.3	N/A	N/A	N/A	N/A
TLA7012 Logic Analyser	Press list in a tab. format	Step 1.4	N/A	N/A	N/A	N/A
TLA7012 Logic Analyser	Save File "MASc_TEST_PROC.txt"	Step 1.5	N/A	N/A	N/A	N/A
MatLab PC	Transfer file to Matlab PC	Step 1.6	N/A	N/A	N/A	N/A
File	Load file In MATLAB Directory	Step 1.7	Work 1	File in Work 1	N/A	N/A
matlab Script	Run "MASc_TestProcedure_ADC.m"	Step 1.8	Work 1	Test Result GUI	N/A	N/A
MASc_Req_ADC3	PRE_SER_PAR_N	Step 1.9	Pass!!!	0	N/A	0
MASc_Req_ADC3	PRE_ADC_RANGE	Step 1.9	Pass!!!	0	N/A	0
MASc_Req_ADC3	PRE_WORD_N_BYTE	Step 1.9	Pass!!!	0	N/A	0
MASc_Req_ADC3	PRE_SER_PAR_N	Step 1.9	Pass!!!	0	N/A	0
MASc_Req_ADC3	PRE_STBY_N	Step 1.9	Pass!!!	1	N/A	1
MASc_Req_ADC3	PRE_HW_N_SW	Step 1.9	Pass!!!	0	N/A	0
MASc_Req_ADC3	PRE_WRITE_N	Step 1.9	Pass!!!	0	N/A	0
MASc_Req_ADC3	PRE_RESET	Step 1.9	Pass!!!	1	N/A	1
MASc_Req_ADC3	PRE_CONVERST_C	Step 1.9	Pass!!!	0	N/A	0
MASc_Req_ADC3	PRE_READ_N	Step 1.9	Pass!!!	1	N/A	1
MASc_Req_ADC3	PRE_CS_N	Step 1.9	Pass!!!	1	N/A	1
MASc_Req_ADC5	SampleStrobe2AdcConvSt (s)	Step 2.1	Pass!!!	2.500000e-08	1.250000e-08	2.000000e-08
MASc_Req_ADC4	ADC_ConvTimeHigh (s)	Step 2.2	Pass!!!	1.260000e-06	1.190000e-06	1.830000e-06
MASc_Req_ADC4	Sample strobe Rate	Step 2.3	Pass!!!	104	N/A	1.040000e+02
MASc_Req_ADC4	SYS_CLOCK (s)	Step 2.4	N/A	2.500000e-08	N/A	2.000000e-08
MASc_Req_ADC4	Acquis. Periodicity	Step 2.4	Pass!!!	2.600000e-06	1.250000e-08	2.600000e-06
MASc_Req_ADC4	PRE_CONVST (A,B,C)	Step 2.4	Pass!!!	2.600000e-06	1.190000e-06	2.600000e-06
MASc_Req_ADC1	ADC Tacq	Step 3.1	Pass!!!	2.800000e-07	Min	1.390000e-06
MASc_Req_ADC1	ADC T1	Step 3.1	Pass!!!	2.000000e-08	Min	1.418320e-03
MASc_Req_ADC1	ADC T2	Step 3.1	Pass!!!	0	Min	1.200000e-07
MASc_Req_ADC1	ADC T4	Step 3.1	Pass!!!	0	Min	2.000000e-08
MASc_Req_ADC1	ADC T6	Step 3.1	Pass!!!	3.000000e-08	Min	5.000000e-08
MASc_Req_ADC1	ADC T7	Step 3.1	Pass!!!	1.000000e-08	Min	3.000000e-08

Comment: MASc_Req_ADC2: see MASc_Req_ADC3 signal PRE_SER_PAR_N

Figure A.1: Automated FPGA verification of the ADS8556 interface results.

Table A.1: Cortex-A processor chips comparison.

Features	Cortex-A5	Cortex-A7	Cortex-A8	Cortex-A9	Cortex-A15	Cortex-A17	Cortex-A32	Cortex-A35	Cortex-A53	Cortex-A57	Cortex-A72	Cortex-A73
Release date	Dec. 2009	Oct. 2011	Jul. 2006	Mar. 2008	Apr. 2011	Announced Feb. 2014	Announced Feb. 2016	Announced Nov. 2015	Jul. 2014	Jan. 2015	Announced Apr. 2015	Announced May 29 2016
Architecture	ARMv7-A	ARMv7-A	ARMv7-A	ARMv7-A	ARMv7-A	ARMv7-A	ARMv8-A	ARMv8-A	ARMv8-A	ARMv8-A	ARMv8-A	ARMv8-A
Typical clock speed	~1 GHz	~1 GHz on 28nm	~1 GHz on 65nm	~2GHz on 40nm	~2.5GHz on 28nm	Beyond 2.5GHz on 28nm	-	-	2GHz on 28nm	1.5 to 2.5GHz on 20nm	Up to 2.5GHz on 16 nm	2.8GHz on 10nm
Execution order	In-order	In-order	In-order	Partial Out of order	Out of order	Out of Order	In-order	In-order	In-order	Out of order	Out of order	Out of order
Cores	1 to 4	1 to 4	1	1 to 4	1 to 4	1 to 4	1 to 4	1 to 4	1 to 4	1 to 4	1 to 4	1 to 4
Peak integer throughput	1.6 DMIPS / MHz	1.9 DMIPS / MHz	2 DMIPS / MHz	2.5 DMIPS / MHz	3.5 DMIPS / MHz	-	-	-	2.3 MIPS / MHz	4.1 to 4.76 MIPS / MHz	-	-
Vector Floating Point (VFP) Architecture	VFPv4	VFPv4	VFPv3	VFPv3	VFPv4	VFPv4	VFPv4	VFPv4	VFPv4	VFPv4	VFPv4	VFPv4
NEON Architecture	NEON	NEON v2	NEON	NEON	NEON v2	-	-	-	-	-	-	-
Half precision extension	Yes	Yes	No	Yes	Yes	-	-	-	-	-	-	-
Hardware Divide	No	Yes	No	No	Yes	Yes	-	-	-	-	-	-
Fused Multiply Accumulate	Yes	Yes	No	No	Yes	Yes	-	-	-	-	-	-
Pipeline stages	8	8	13+	8 to 11[1]	15+	11+	8	8	8	-	-	-
Instructions decoded per cycle	1	Partial dual issue	2 (super-scalar)	2 (super-scalar)	3 (super-scalar)	-	-	-	2	3	3	-
LPAE	No	Yes	No	No	Yes	Yes	-	-	-	-	-	-
Floating Point Unit	Optional	Yes	Yes	Optional	Optional	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Advanced Microcontroller Bus Architecture (AMBA) Interface	64-bit AMBA 3	128-bit AMBA 4	64 or 128 bit AMBA 3	2 x 64-bit AMBA 3	128-bit AMBA 4 ACE	128-bit AMBA 4 ACE	128-bit AMBA 4 ACE or AMBA5 CHI or AXI 4	128-bit AMBA4 ACE or AMBA AXI4 or AMBA5 CHI	64-bit 1/F AMBA 4 (supports AMBA 4 and AMBA 5)	128-bit 1/F AMBA 4 (supports AMBA 4 or AMBA 5)	128-bit AMBA 4 ACE or AMBA5 CHI	128-bit AMBA 4 AXI4 or ACE
L1 Cache size (Instruction)	4 Kilobytes (KB) to 64KB	8KB to 64KB	16KB to 32KB	16KB to 64 KB	32 KB	32KB to 64KB	8KB to 64KB	8KB to 64KB	8KB to 64KB	48KB	48KB	64KB
L1 Cache size (Data)	4KB to 64KB	8KB to 64KB	16KB to 32KB	16KB to 64 KB	32KB	32KB	8KB to 64KB	8KB to 64KB	8 KB to 64 KB	32 KB	32KB	32KB to 64KB
L2 Cache	None	0 to 1024 KB	0 to 1MB	None	256KB to 4MB	256KB to 8MB	Shared 128KB to 1MB	Shared 128KB to 1MB	128KB to 2MB	512KB to 2MB	512 KB to 2MB	Shared 256KB to 8MB
ISA Support	-ARMv7 -Thumb-2 / Thumb -DSP & SIMD extensions	-ARMv7-A -Thumb-2 -Trust Zone security technology -DSP & SIMD extensions -Hardware virtualization support	-ARM -Thumb-2 / Thumb -Trust Zone technology	-ARMv7-A -Thumb-2 / Thumb -Trust Zone technology -Jazelle -DSP extension	-ARMv7-A -Thumb-2 -TrustZone technology -DSP & SIMD extensions -Hardware virtualization support -Hypervisor debug instructions	-ARM and Thumb-2 -TrustZone technology -DSP & SIMD extensions -Hardware virtualization support -Hypervisor debug instructions	-AArch32 -TrustZone technology -DSP & SIMD extensions -Hardware virtualization support	-AArch32 -AArch64 -TrustZone technology -DSP & SIMD extensions -Hardware virtualization support	-AArch32 -AArch64 -TrustZone technology -DSP & SIMD extensions -Hardware virtualization support	-AArch32 -AArch64 -TrustZone technology -DSP & SIMD extensions -Hardware virtualization support	-AArch32 -AArch64 -TrustZone technology -DSP & SIMD extensions -Hardware virtualization support	-AArch32 -AArch64 -Trust Zone technology -DSP & SIMD extensions -Hardware virtualization support

[1] Arm Site says 8 to 11, Arm Developer Site says 10+ and ARM programmer's guide says 9 to 12

Table A.2: Cortex-R Series Comparison

Features	Cortex-R4	Cortex-R5	Cortex-R7	Cortex-R8
Release Date	May 2006	August 2010	March 2012	Announced Feb 2016
Typical Clock Speed	600 MHz on 40nm	600MHz on 40nm	1Ghz on 28nm	-
Execution order	In order	In order	Out of order	Out of order
Cores	1	1 to 2 (AMP mode only)	1 to 2	1 to 4
Peak integer throughput	2.45 DMIPS/MHz	2.45 DMIPS/MHz	2.5 DMIPS/MHz	2.5 DMIPS/MHz
VFP architecture	VFPv3	VFPv3	VFPv3	VFPv3
Half precision extension	No	No	Yes	-
Hardware integer divide	Yes	Yes	Yes	-
Fused Multiply Accumulate	No	No	No	-
Pipeline stages	8	8	11	11
Instruction decode per cycle	Partial dual issue	Partial dual issue	2 (superscalar)	-
Floating Point Unit (FPU)	Optional	Optional	Optional	Optional
AMBA interface	64-bit AXI3	64-bit AXI3	64-bit AXI3	64-bit AXI
Generic Interrupt Controller (GIC)	Not included	Not included	Included	Included
Branch predictor entries	256	256	Configurable	-
Indirect predictor	No BTAC	No BTAC	256 to 4096 BTAC entries	-

Table A.3: Cortex-M Series Comparison

Features	Cortex-M0	Cortex-M0+	Cortex-M3	Cortex-M4	Cortex-M7
Year Announced	2009	2012	2004	2010	2014
Architecture	ARMv6-M	ARMv6-M	ARMv7-M	ARMv7E-M	ARMv7E-M
ISA support	Thumb / Thumb-2 subset	Thumb / Thumb-2 subset	Thumb / Thumb-2	Thumb / Thumb-2	ARMv7-M
Memory Protection	no	yes	yes	yes	yes
Non-Maskable Interrupt	yes	yes	yes	yes	yes
Physical Interrupts	1 to 32	1 to 32	1 to 240	1 to 240	1 to 240
Pipeline stages	3	2	3	3 + branch speculation	6 (superscalar) + branch prediction
FPU	None	None	None	Single precision	Single and double precision
Performance Efficiency	0.87 DMIPS/MHz	0.95 DMIPS/MHz	1.25 DMIPS/MHz	1.25 DMIPS/MHz no FPU, 1.27 DMIPS/MHz with FPU	2.14 DMIPS/MHz
Enhanced Instructions / DSP Extensions	Hardware single cycle (32 x 32) multiply	Hardware single cycle (32 x 32) multiply	Saturated math support, Single-cycle (32x32) multiply, Hardware divide (2-12 cycles)	Single cycle 16/32-bit MAC Single cycle dual 16-bit MAC 8/16-bit SIMD arithmetic hardware divide (2-12 Cycles)	Single cycle 16/32-bit MAC Single cycle dual 16-bit MAC 8/16-bit SIMD arithmetic hardware divide (2-12 Cycles)

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