DESIGN AND CONTROL OF AN ISOLATED BATTERY-DRIVEN GRID INTERFACE WITH THREE-PHASE DUAL-ACTIVE-BRIDGE CONVERTER

DESIGN AND CONTROL OF AN ISOLATED BATTERY-DRIVEN GRID INTERFACE WITH THREE-PHASE DUAL-ACTIVE-BRIDGE CONVERTER

BY

DEQIANG WANG, M. Eng.

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AUTHOR:	Deqiang Wang M. Eng., (Aeronautical Engineering) Beihang University, Beijing, China
SUPERVISOR:	Dr. Ali Emadi
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谨以此献给我的父母，王军 孙立晶

和我的未婚妻 赵晶

To my Parents, Jun Wang and Lijing Sun

and my Fiancee, Jing Zhao

Abstract

Battery energy storage system (BESS) is promising to be implemented in residential applications for supporting PV integration, load shifting, and backup power purposes. For this application, 48V second-life battery draws more and more attentions for their cost-effectiveness, safe voltage level, reliability, and potential large market. This thesis proposes the comprehensive control and design of an isolated battery-driven grid interface (IBDGI) with the dual-active-bridge (DAB) converter for residential applications with 48V battery pack.

The three-phase DAB converter is a promising candidate as the front-end DC/DC converter in the two-stage IBDGI due to its high efficiency, high power density, and low capacitance requirement. An effective design strategy for the three-phase DAB converter is proposed based on the zero-voltage-switching (ZVS) zone and back-flow power to achieve high efficiency for a wide operating voltage range and different load conditions. Based on the power loss model, an easily-implemented variable switching frequency operating method is proposed to further increase the efficiency at light load conditions.

The dead-time effect is observed in the three-phase DAB converter. To avoid the dead-time effect and better understand the phenomena, a comprehensive analysis is proposed. All the cases of the dead-time effect in the three-phase DAB converter

are analysed in terms of the buck, boost, and matching states. The expressions of the transmission power, constraint conditions, and key time of the dead-time effect are derived for each state. The operation waveforms of the dead-time effect are also presented.

The hybrid capacitor bank composed by the LC resonant filter with electrolytic capacitor and film capacitor is utilized for the DC bus of the IBGDI. The electrolytic capacitors work as passive decoupling purpose while the film capacitor is responsible for high switching harmonic filtering. Moreover, a current sharing method between the hybrid capacitor bank is proposed to extend the electrolytic capacitor's life.

The LCL single-phase inverter is applied for the downstream of the IBDGI. A step-by-step design procedure of the LCL filter with passive damping is proposed for the 120V/240V dual grid-tied and standalone modes. The PR controllers are also designed for the LCL inverter for standalone and grid-tied modes.

At the system level, a novel second harmonic current (SHC) reduction strategy is proposed for the IBDGI with the three-phase DAB converter by adding a load current feedforward (LCFF) path to the DAB voltage closed-loop controller. This method will suppress the SHC without modifications of the original controller's bandwidth, which make it easy to be implemented. The small-signal model of the three-phase DAB converter is provided and verified by the step response. The parameter sensitivity analysis for the LCFF method is proposed to show that the SHC is well suppressed within $\pm 20\%$ parameter error.

The proposed converter and control methods are verified by simulation and experimental results.

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Notation and abbreviations

Symbol	Description	Unit
ϕ	Phase shift	rad
d	Equivalent conversion ratio	-
D	Dead-time	rad
K	DAB design factor	H·Hz
r	Back-flow power ratio	-
n	Turn ratio of transformer	-
L_k	Leakage inductance of transformer	-
f_s	Switching frequency	Hz
C_{gs}	Gate-source capacitance	nF
C_{iss}, C_{oss}, C_{rss}	Input, output, and reverse transfer capacitance	nF
E_{on}, E_{off}	Switch turn-on and -off energy loss	mJ
$E_{on,M}$, $E_{off,M}$	MOSFET turn-on and -off energy loss	mJ
P_{loss}	Switch power loss	W
t_{ri}, t_{fi}	Current rise- and fall-time	ns
t_{ru}, t_{fu}	Voltage rise- and fall-time	ns

V_{th}, $V_{plateau}$	Threshold and plateau voltage	V
R_{ac},R_{dc}	AC and DC resistance of the windings of transformer	Ω
v_{ds}, v_{gs}	MOSFET drain-source and gate-source voltage	V
C_E, C_F	Eletrolytic capacitance and film capacitance	F
L_E	Add-on inductance to electrolytic capacitor	H
Z_c	Totle impedance of open-loop front-end converter	Ω
Z_{capa}	Impedance of DC bus capacitor	Ω
Z_{DAB}	Impedance of the DAB converter	Ω
Z_{c_close}	Totle impedance of closed-loop front-end converter	Ω
C_1	Input capacitor of the DAB converter	F
C_f	Capacitor in LCL filter	F
L_1	Inverter-side inductor in LCL filter	H
L_2	Grid-side inductor in LCL filter	H
R_d	passive damping resistor	Ω
ω_{o}	Angular frequency of the output inverter	rad
f_{o}	Frequency of the output inverter	Hz
φ	Phase angle of the grid	s
AC	Alternating current	-
BESS	Battery energy storage system	-
PV	Photovoltaic	-
DC	Direct current	-
EMI	Electromagnetic interference	-

IBDGI	Isolated battery-driven grid interface	-
DAB	Dual active bridge	-
MOSFET	Metal-oxide-semiconductor field-effect transistor	-
PCB	Printed circuit board	-
PWM	Pulse width modulation	-
SPWM	Sinusoidal pulse width modulation	-
SHC	Second harmonic current	-
ZVS	Zero voltage switching	-
LCFF	Load current feedforward	-
PR	Proportional resonant	-
PLL	Phase locked loop	-
SPS	Single phase shift	-
EPS	Dual phase shift	-
DPS	Load current feedforward	-
ZCS	Zero current switching	-
SiC	Silicon Carbide	-
GaN	Gallium Nitride	-
THD	Total harmonic distortion	-
RMS	Root mean square	-
HC	Harmonics compensator	-
BPF	Bandpass filter	-

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Chapter 1

Introduction

1.1 Background

1.1.1 Utilizing Battery Energy Storage System in Residential Applications

Energy storage system (ESS) draws increasing attention to improve the grid's power quality, flexibility and reliability by providing grid support functions, such as peak shaving, energy arbitrage, integration of renewable energy, voltage and frequency regulation and so on (Chang *et al.*, 2017).

As a typical mechanical ESS, pumped hydroelectric systems (PHS) account for 95% of a worldwide energy storage capacity ofdischarge power in 2017 (Chang *et al.*, 2017). However, battery energy storage system (BESS) can offer a number of high-value opportunities supposing lower cost can obtained due to their fast-response and relatively high power density and energy density (Chang *et al.*, 2017; Dunn *et al.*, 2011). Among them, the BESSs applied in residential application is promising to

use energy more efficiently, economically and reliably. The provided grid services can be categorized into (IEC, 2011): (1) Integration of renewable energy to increase dispersed generation-based self-consumption; (2) Load shifting and peak shaving; (3) Emergency backup power for critical loads and so on.

Firstly, BESS are one of the most promising solutions for the integration of renewable resources, especially for residential PV units (Alam *et al.*, 2013; Barcellona *et al.*, 2018). To achieve low greenhouse gas emission, the electric vehicles (EVs), especially battery electric vehicles (BEVs) and plug-in electric vehicles (PHEVs), grows extremely rapidly these years all around the world (International Energy Agency, 2017). However, the increasing EVs won't be more environmental-friendly than the internal combustion engine (ICE) vehicles if most of its electricity is supplied from the conventional power generation systems using fossil fuels. Thus, the proliferation of renewable energy source (RESs), such as wind and photovoltaic (PV), is essential to achieve a cleaner and sustainable future considering the rising energy demand. RESs is preferred as the form of distributed generators (DGs) to produce electricity because it will avoid transmission and distribution losses and increasing the efficiency of the electricity grid, as well as higher power reliability (Rodriguez-Diaz *et al.*, 2016). However, the intermittent renewable energy sources enlarge the mismatch between the electricity generation and consumption which leads to severe problems such as fluctuations in frequency and voltage, stability issues and/or violations of power lines capability margin (Molina, 2017). Distributed BESSs can solve these issues of the distributed RESs as form of residential microgrids (MGs) (Garrity, 2010).

A basic example is illustrated as Figure 1.1 where BESS supporting PV integration for load balancing in residential application. In case to achieve more self-consumption,

the power profile of the grid is not provided. The BESSs are charged in the daytime, when PVs generate power, and are discharged at night when PV power is unavailable. The self-consumption of PV energy is increased because the system power is balanced. The grid will supple the deficient amount of energy or even will be sold by extra energy to make some profit for the household.

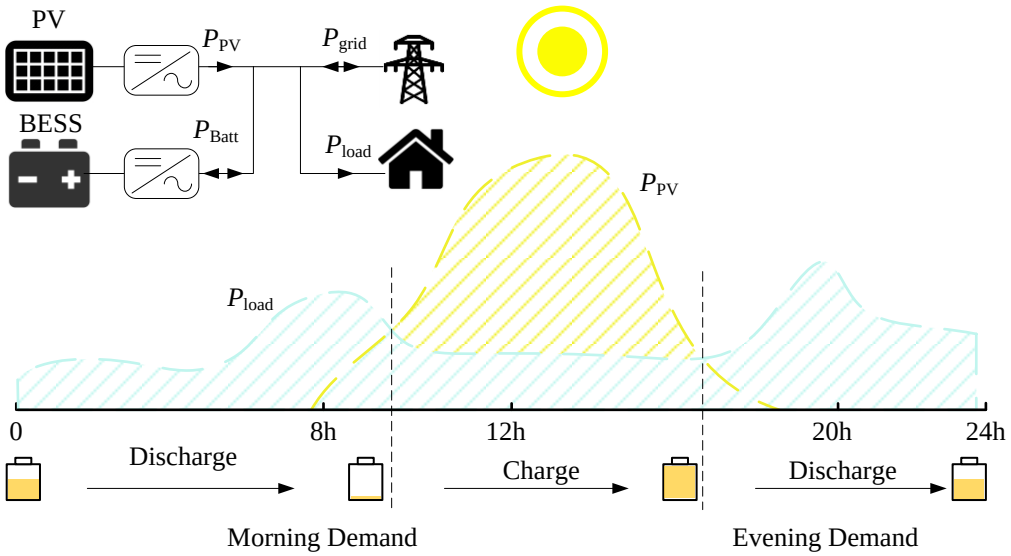


Figure 1.1: Illustration for battery energy storage system in residential microgrid.

Secondly, load shifting and peak shifting by battery-only residential system can potentially save electricity cost for the household. By deploying BESSs behind-the-meter, they can store the purchased energy when time-of-use (TOU) prices are low then release it when the TOU prices are high thus the customers' bills are reduced. The same happens with demand charge reduction, by managing the load profile to reduce the customer peak demand charge (Molina, 2017; Zhu *et al.*, 2016).

The last but not the least, the BESS can active as residential backup power (Fitzgerald *et al.*, 2015). Battery storage can operate off-grid as a continuous voltage power supply to sensitive loads and critical loads until a generator can be turned on

or the utility power is restored.

1.1.2 Second Life Battery from Electrified Vehicles

The capital cost of the battery is the primary barrier to further expand the market in residential application (IEC, 2011). With purchased EV, its battery can be used for grid applications like load-shifting, peak-shaving and energy backup which is generally called vehicle-to-grid (V2G). However, V2G applications accelerate battery aging due to the increased charge-discharge cycles then the range and performance of EVs are degraded. Second-life batteries from electric and hybrid vehicles are promising to be reused in grid system as cost-effective alternative to the existing off-the-shelf BESSs (Strickland *et al.*, 2014). For EV application, batteries for traction purpose are considering end-of-life (EoF) when it's degraded to nominally 70%-80% of its original capacity. Assuming a typical battery capacity of around 5—24 kWh [mild hybrid electric vehicle (MHEV) 5 kWh-–BEV 18-–24 kWh battery, and a 10year lifespan, this equates to a projection of batteries available for storage in second-life applications of >1 GWh by 2025. Although EoF batteries are not considered fitful for EV traction, they can be estimated to work as network deferral purpose for another 15 years, which fulfills the requirements for home energy management and home backup purpose (Akhil *et al.*, 2015). The financial sense of reused EV batteries in European electricity grid is investigated for integration of renewable energy purpose (Gur *et al.*, 2018). The economic analysis provided in (Heymans *et al.*, 2014) supports the use of second life batteries in residential applications of Ontario, Canada.

Among the second life batteries, 48V batteries are promising for this residential application because (1) they will be a large market as typical second-life batteries

from mild hybrid vehicles; (2) 48V is considered as safety applied in home since the voltage level no need for protection system against indirect contacts is 120V according to (Rodriguez-Diaz *et al.*, 2016) (3) 48V battery pack has less cells connected in series which ensure reliability compared with high voltage battery pack.

Above all, BESSs with second life 48V battery are quite attractive in residential applications with or without distributed renewable energy system, such as PV panels.

1.1.3 Specifications

Based on the background, it's essential to develop a high efficient, power density, reliability and long lifetime isolated battery-driven grid interface (IBDGI) for BESS with 48V battery pack. According to (Akhil *et al.*, 2015), the BESS for home energy management and home backup should be sized from 2 to 5kW power rating. Thus, a 3kW laboratory prototype is focused in the thesis. HE-52104 high energy battery pack from ALLCELL is selected to be applied in this system. On the other hand, the three-wire single phase system is common in North America for residential and light commercial applications (Wikipedia, 2018). In this case, the voltages are 120V line to neutral (grounded center tap of transformer) and 240 V line to line. This system also allows 120V to be supplied for lighting and convenience outlets while 240V for higher-demand appliances such as space heating, air conditioning, electric vehicle charging, kitchen stoves or water heaters. So our system should have two output options (120V AC/240V AC) but share the same hardware. The output for 120V AC should has limited power rating considering the fuse of the outlets.

Galvanic isolation is essential for battery-driven grid interface in residential application for the following reasons: (1) Isolation is required for distributed generation

for safety concerns (Karshenas and Daneshpajooh, 2011), preventing accidental current from reaching ground through a person's body. (2) High voltage conversion ratio can be provided by isolated DC/DC converter through its high-frequency transformer for voltage matching between 48V battery source and 120V/240V utility grid. The specifications of the system is summarized as Table 1.1.

Table 1.1: Specifications of IBDGI for residentail applications.

Input voltage	48V DC norminal (42V-58V)
Output voltage	120V AC/240V AC
Output frequency	60Hz
Power rating	1kW(120V AC)/3kW(240V AC)
Other	Galvanic isolation

1.2 Motivation and Challenges

Although there are several single-stage DC/AC topologies available for this application, the conventional two-stage inverter with high-frequency-link isolated DC/DC converter is still proved to be effective for IBDGI in case of complexity, power density and efficiency.

Dual-active-bridge (DAB) converter is a promising candidate for the front-end isolated DC/DC converters of the IBDGI due to its galvanic isolation, bidirectional operation, high power density, and high efficiency. But the widely-researched single-phase DAB converter suffers from its large capacitor banks on both input side and output side. Moreover, the BESSs driven by 48V battery has more input capacitance requirement than them by high voltage battery under same power rating. Thus the

three-phase DAB converter is a promising alternative since the capacitance on both sides of the three-phase DAB converter is around one third of that in the single-phase DAB converter. However, there are not materials available discussing an effective design strategy for the three-phase DAB converter for wide input voltage range and wide load conditions.

The dead-time effect phenomena were observed by analyzing the experimental waveforms of the designed three-phase DAB converter. The so-called "dead-time" in the DAB converter is designed to ensure ZVS which depends on the oscillation time caused by the leakage inductance and the switch's stray capacitance and avoid cross-conduction. However, the dead-time effect may have significant impact on the converter performance when high switching frequency, wide input and output voltage range or wide operation power range are required. It's essential to propose the comprehensive theoretical analysis of the dead-time effect in three-phase DAB converter to provide an insight to the dead-time compensation.

Single-phase LCL inverter is widely utilized for residential grid-tied applications. For the two-stage IBDGI, the standalone operation mode is also necessary for backup power usage. However, it's lack of the detailed design strategy of the LCL-based inverter with both grid-tied and standalone operations. Passive power decoupling method with electrolytic capacitors is widely used to buffer the second harmonic caused from single-phase inverter in the commercial products because of simple structure and reliability. However, the electrolytic capacitor is usually oversized considering additional high frequency switching harmonics. A reasonable DC bus capacitor bank needs to be designed for the system to interface the front-end converter and the downstream inverter.

To the system controller level, second harmonic current (SHC) reduction method should be proposed for the two-stage IBDGI with the three-phase DAB converter. Without well mitigation, SHC will pass through the front-end converter to increase Ah-throughput of the battery which makes it age faster than expected. However, the availble SHC reduction strategy for the system with the DAB topology as its front-end converter is complicated besides it needs to modify the original compensator's bandwidth. A new SHC reduction strategy should be investigated.

1.3 Contributions

The author has contributed to a number of original developments on the design and control of an isolated battery-driven grid interface with three-phase DAB converter. These contributions are briefly described below:

1. A comprehensive design strategy of the front-end three-phase DAB converter in IBDGI is proposed based on the ZVS zone and back-flow power to achieve high efficiency for wide operating voltage range and load conditions.

2. An easily-applied variable switching frequency operation method is proposed to further increase the efficiency of the three-phase DAB converter at light load conditions.

3. The comprehensive analysis of the dead-time effect in the three-phase DAB converter are analysed in terms of the buck, boost, and matching states.

4. A hybrid capacitor bank with electrolytic and film capacitors is proposed for the DC bus of the IBDGI system. A current sharing method is proposed where

an inductor with reasonable size can be utilized in the LC resonant filter to extend the electrolytic capacitors' lifetime.

5. A step-by-step design procedure is proposed for the downstream single-phase LCL inverter in IBDGI with passive damping and the corresponding PR controllers are designed for standalone and grid-tied operation.

6. A SHC reduction method is proposed for the two-stage IBDGI with the three-phase DAB converter using a load current feedforward (LCFF) control which intends to incorporate virtual impedance to the output impedance of the front-end converter.

1.4 Outline of the Thesis

This thesis presents a comprehensive design and control of an isolated battery-driven grid-interface inverter with three-phase DAB converter and its outlines is illustrated as follows.

In chapter 2, the conventional and proposed IBDGI are introduced in case of topology and SHC reduction strategy. After analyzing the specifications, two-stage isolated topology is still promising applied in residential applications considering power density, efficiency and safety. Isolated bidirectional DC/DC converters for high power applications are reviewed as the battery-interface front-end converter. The advantages of the three-phase DAB converter the single-phase DAB converter make it promising for this application. The output filter is reviewed for the downstream single-phase grid-tied inverter. The design and control of the single-phase LCL inverter are also introduced. Then different power decoupling methods are discussed for the single-phase

inverter system. Moreover, the drawbacks of the second harmonic current existing in two-stage single-phase inverter is presented then the strategies of SHC reduction are reviewed in two approaches: virtual impedance and modified reference. Finally, the configuration for IBDGI with three-phase DAB converter is proposed and analyzed based on all the analysis above.

Chapter 3 proposed a comprehensive design strategy of the front-end three-phase DAB converter in IBDGI based on the ZVS zone and back-flow power to achieve high efficiency for wide operating voltage range and load conditions. The design strategy is verified by the efficiency analysis and its power loss model. An easily-applied variable switching frequency operation method is proposed to increase the efficiency at light load conditions. It will minimize the power loss by increasing switching frequency for the three-phase DAB converter. The simulation and experimental results are utilized to verify the design strategy and variable switching frequency method.

In chapter 4, the dead-time effect of the three-phase DAB converter is analyzed. The dead-time effect existing in the single-phase DAB converter is also observed in the three-phase DAB DC/DC converter. The occurrence of the dead-time effect depends on the relationship of the switching frequency, the phase shift value, the dead-time value and the equivalent conversion ratio. The dead-time effect may have significant impact on the converter performance when high switching frequency, wide input and output voltage range or wide operation power range are required. Therefore, comprehensive research of the dead-time effect is essential to improve the design of the three-phase DAB converter over a wide operation range. In this chapter, all the cases of the dead-time effect in the three-phase DAB converter are analyzed in terms of the buck, boost, and matching states. The expressions of the transmission power,

constraint conditions, and key time of the dead-time effect are derived for each state. The operation waveforms of the dead-time effect are also presented to better understand the dead-time effect. Finally, the analysis is verified by both simulation and experimental results.

Chapter 5 presents a hybrid capacitor bank for the DC bus in the two-stage IBDGI system and a current sharing method is discussed for the capacitor bank. The electrolytic capacitors are usually used in the DC-bus as typical passive decoupling components while the film capacitors can be added in parallel with the electrolytic capacitor to help filtering out the high frequency harmonics to extend the electrolytic capacitors' lifetime. In addition, the LC resonant filter can be utilized for the decoupling purpose to achieve better performance. However due to the relatively low resonant frequency, it results in large inductance which will significantly increase the size and cost of the system. A current sharing method is proposed in this chapter. With this method, an inductor with reasonable size can be utilized in the LC resonant filter to further extend the electrolytic capacitors' lifetime. In this chapter, the design procedure of the hybrid capacitor bank for the single-phase inverter with unipolar modulation will be discussed. The simulation and experimental results will be provided to verify the design of the hybrid capacitor bank.

Chapter 6 proposes a downstream single-phase LCL inverter in IBDGI to fulfill the requirement for both 120V and 240V operation in standalone and grid-tied modes. The step-by-step design procedure is presented for the LCL inverter with passive damping. Then the Proportional Resonant (PR) controllers are designed for the standalone and grid-tied modes. The phase-locked-loop (PLL) is used to detect the phase of the grid voltage for grid-tied operation mode. The simulation and

experimental results are provided to verify the filter and PR controller performance.

In chapter 7, a new SHC reduction strategy is proposed for the twp-stage IB-DGI system with three-phase DAB converter. The SHC existing in the front-end DC/DC converter is caused by the pulsating power of the single-phase inverter. The SHC will increase the battery's degradation and the component stress of the front-end converter. A SHC reduction method is proposed for the three-phase DAB converter based two-stage single-phase inverter using a LCFF control. The proposed idea is to incorporate virtual impedance to the output impedance of the front-end converter. The easy-to-be-implemented method doesn't need to modify the original voltage closed-loop controller but suppress SHC while keep good dynamic performance. As part of analysis, the small-signal model of the three-phase DAB converter is provided and verified by its step response. The parameter sensitive analysis of the proposed method is proposed to demonstrate that the SHC can be well suppressed within $\pm 20\%$ parameter error of the feedforward control. Finally, the experiment setup is built to verify the performance of the proposed SHC reduction method.

Chapter 8 concludes the thesis and proposes potential future works.

Chapter 2

Isolated Battery-Driven Grid-Interface Systems

2.1 Topology Evaluation of Isolated Battery-Driven Grid-Interface Systems

Generally, bidirectional power flow is required for the isolated battery-driven grid interface (IBDGI) to charge and discharge the battery pack. As mentioned in Section 1.1, galvanic isolation is needed for safety concerns and voltage matching. High-frequency-link isolation will provide a compact and flexible design than it with line-frequency transformer. Two-stage converter is effective solution to achieve it by introducing a front-end high-frequency isolated DC/DC converter which couples battery source with intermediate DC bus whereas a downstream inverter will interconnect the DC bus with the utility grid. The two-stage isolated DC/DC converter can mainly be categorized into stable DC bus voltage and variable DC bus voltage as Figure 2.1.

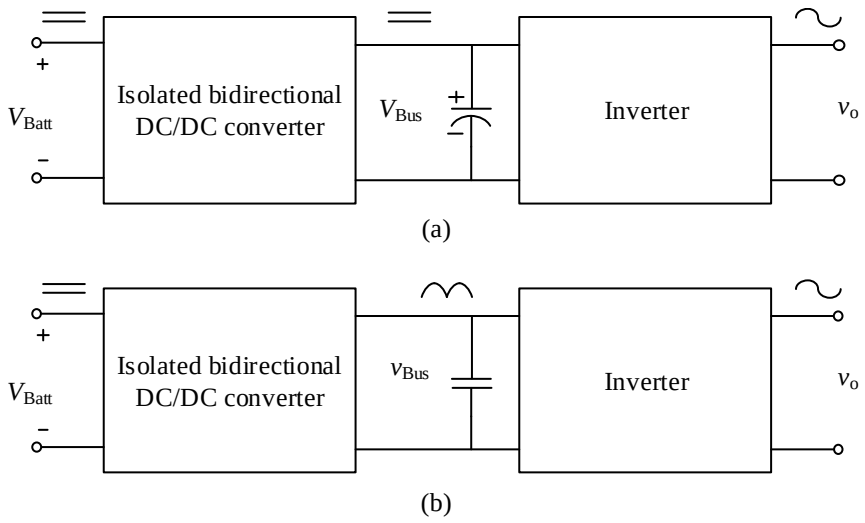


Figure 2.1: Topology evaluation of two-stage isolation bidirectional DC/AC inverter: (a) Stable DC bus voltage. (b) Variable DC bus voltage.

The conventional two-stage DC/AC converter shown as Figure 2.1(a) is widely researched and applied for energy storage system (Inoue and Akagi, 2007; Zhao *et al.*, 2014a; Tan *et al.*, 2012). Moreover, the stable DC bus can provide a high voltage DC link for additional distributed energy source such as PV panels (Wang and Ruan, 2016). The stable DC bus voltage can be utilized for the coordinative control in the bidirectional power application (Tian *et al.*, 2016, 2015).

Another category is the two-stage DC/AC converter with a variable DC bus voltage as Figure 2.1(b). Usually, the DC bus voltage is controlled incorporating a second order harmonic which leads to lower DC bus capacitance requirement. Thus, smaller DC bus size will be achieved by replacing bulk electrolytic capacitors with film capacitor (Liu and Li, 2015). However, the wide DC bus voltage range causes narrow soft-switching zone so the efficiency of the converter is lower than the conventional topology with stable DC bus voltage. To deal with this issue, variable switching frequency is applied to make sure the converter operating within the ZVS zone for the

variable DC bus voltage (Bai *et al.*, 2017; Cho *et al.*, 2016). Since the core selection of the transformer depends on the volt-sec theory (Cui Ying, 2017), the applied variable switching frequency leads to a larger transformer size. At the same time, the voltage stress of the DC bus capacitor and switches is increased. Thus the topology with variable DC bus voltage may not be more compact than conventional design. Also, the complexity of the controller is another obstacle to apply this topology. Thus conventional the two-stage topology as Figure 2.1(a) is applied in this thesis.

2.2 High-Frequency Isolated Bidirectional DC/DC converters

Dual-Active-Bridge (DAB) topology is a promising candidate for the battery-interface bidirectional isolated DC/DC converters in the IBDGI due to its galvanic isolation, bidirectional operation, high power density, and high efficiency (Zhao *et al.*, 2014c). The biggest advantage is that Zero voltage switching (ZVS) can be naturally achieved to achieve high operation efficiency. DAB topology can be mainly divided into single-phase DAB converter and three-phase DAB converter.

2.2.1 Single-Phase DAB Converter

Topology of the single-phase DAB converter is illustrated as Figure 2.2 where S_1-S_4 and Q_1-Q_4 are controllable switches, so-called "active bridge", on primary and secondary side of the converter. Leakage inductance of the transformer is utilized to analyze the operation of this topology. In this work, we define the battery connected

side is the primary side while the DC-bus connected side is the secondary side. Single-phase-shift (SPS) modulation is usually applied in DAB topology and the operation waveforms of single-phase DAB converter are shown as Figure 2.3.

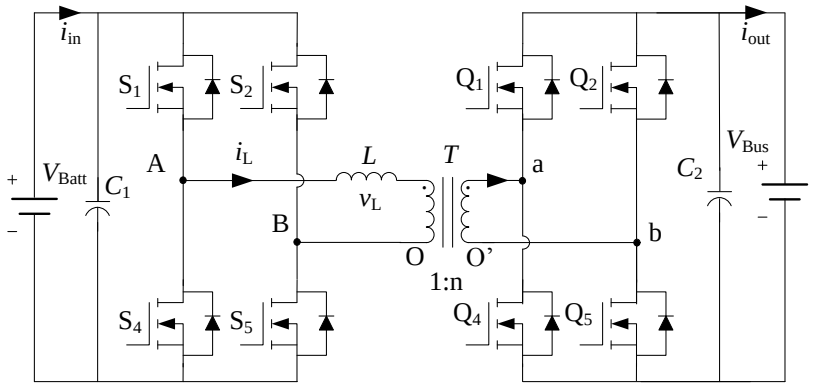


Figure 2.2: Illustration of single-phase DAB converter.

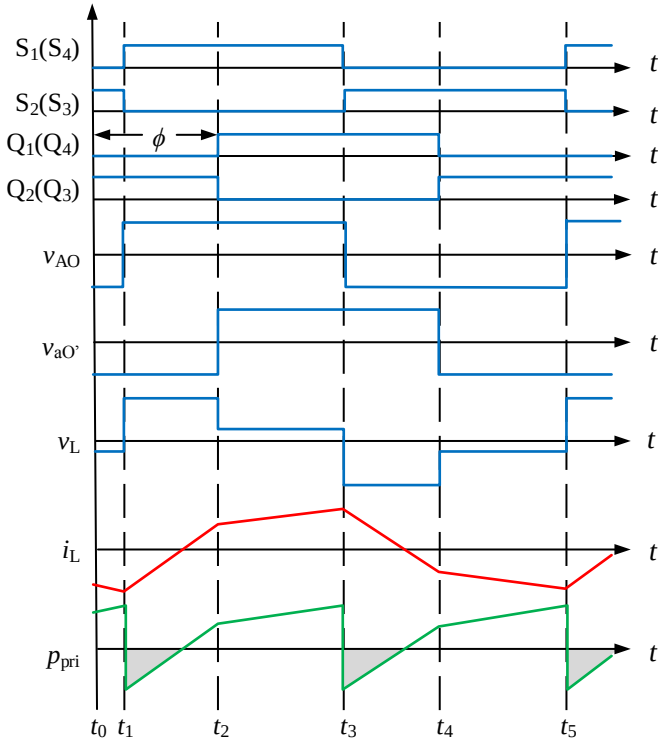


Figure 2.3: Operation waveforms of single-phase DAB converter.

By applying a phase shift ϕ between the primary side and the secondary side switches, the voltage difference, v_{L}, across the leakage inductance of the transformer will be produced. It will induce the current i_{L} go through the transformer thus the power p_{pri} can be transmitted from the primary side to the secondary side or the other side around. The grey area in Figure 2.3 represents the backflow power caused by negative leakage inductance current.

A modular high-frequency-link DC transformer based on single-phase DAB converter for flexible MVDC distribution is discussed on full-process operation, control and experiments (Zhao *et al.*, 2017). The biggest advantage of the DAB topology is that it can naturally achieve ZVS for both primary and secondary sides by allowing certain dead-time. An overall study of the single-phase DAB converter is proposed and the design strategy based on the ZVS zone and reactive power is discussed in (Alonso *et al.*, 2010). A synthetic discrete design methodology of high-frequency isolated bidirectional DC/DC converter is proposed for grid-connected battery energy storage system (Zhao *et al.*, 2014a). Different purpose design strategies: increasing ZVS operation range and improving efficiency at full load are proposed for the single-phase DAB converter in (Rodríguez *et al.*, 2015).

2.2.2 Three-Phase DAB Converter

The single-phase DAB converter suffers from its large capacitor banks needed on both input side and output side (Krismer, 2010). In comparison, the three-phase DAB converter is a promising alternative to the single phase DAB in high power applications, which can reduce the required capacitance significantly and has higher power density (De Doncker *et al.*, 1991). According to (De Doncker *et al.*, 1991), the capacitance on both sides of the three-phase DAB converter is around one third of that in the single phase converter. Indeed, interleaved topology of single-phase DAB converte may be the solution to solve this issue however much more switches have to be added-on thus the cost and size of the system increase significantly. Multi-phase DAB converter, like 4-phase and 5-phase DAB, is still possible but the added-on components, especially transformers, is not worthwhile to reduce more capacitors size and cost so three-phase DAB converter is good enough in case to decrease the bulk capacitance requirement of the single-phase DAB converter. Topology of the three-phase DAB converter is shown as Figure 2.4.

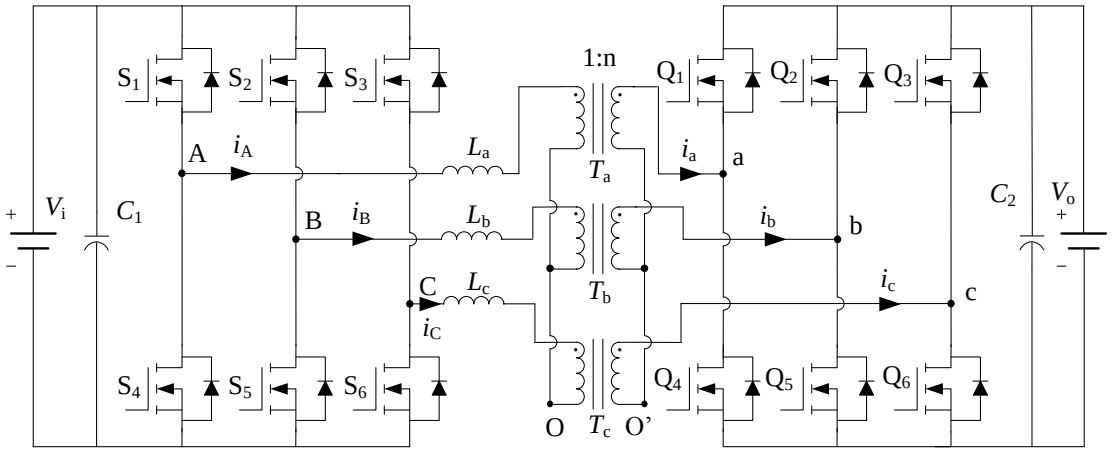


Figure 2.4: Illustration of three-phase DAB converter.

The operation waveforms of the three-phase DAB converter are illustrated in Figure 2.5. There are two available operation modes where the phase shift range are 0-$\pi/3$ and $\pi/3$-$2\pi/3$. By applying a phase shift ϕ between the primary side and the secondary side , the voltage difference across the leakage inductance of the transformer will be produced. It will induce the current go through the transformer thus the power can be transmitted from the primary side to the secondary side or the other side around.

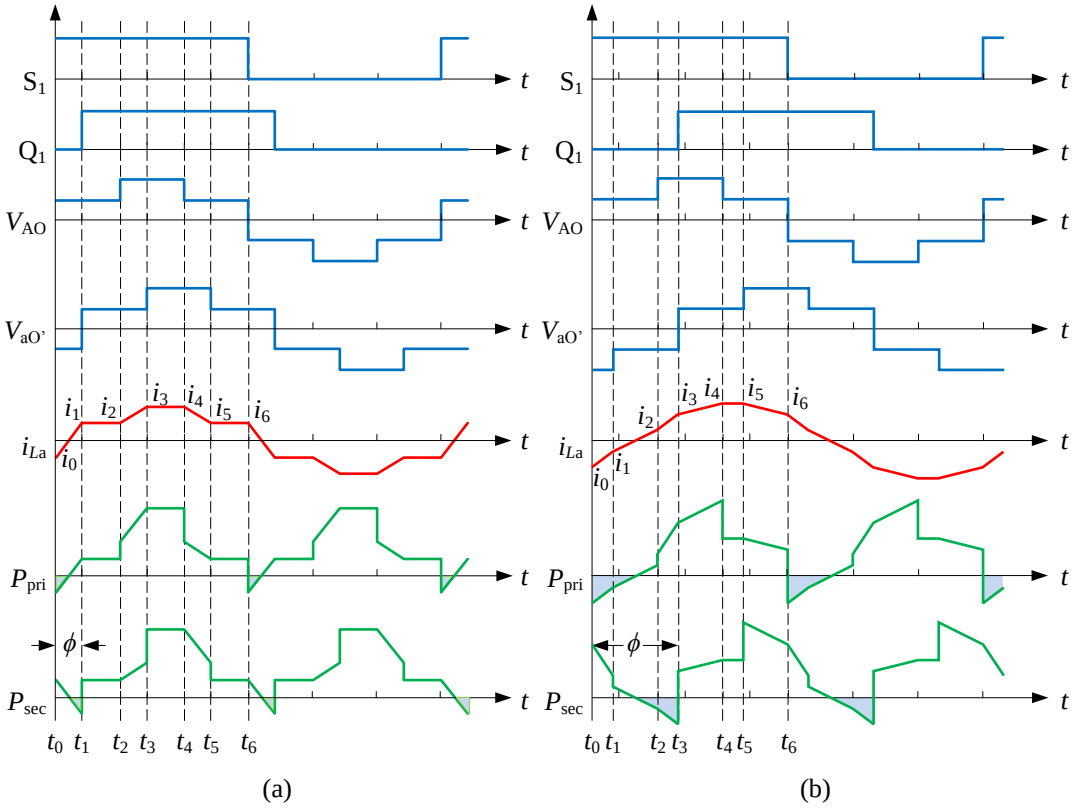


Figure 2.5: Operation waveforms of three-phase DAB converter: (a)0-$\pi/3$ (b)$\pi/3$-$2\pi/3$.

The operation principle of the three-phase DAB converter can also be found in (De Doncker *et al.*, 1991; Xue, 2010; Waltrich *et al.*, 2016). Based on the discussion

above, the single phase shift (SPS) is utilized because of its simplicity and naturally achieved ZVS for all switches. Three individual transformers connected as Y-Y are utilized because more flexibility can be achieved. The turn ratio of the transformers n, leakage inductance L of the transformer and the switching frequency f are the main parameters that should be designed for the three-phase DAB converter.

The three-phase DAB converter with six inverter legs are analyzed and the analytical expressions are provided in (Waltrich *et al.*, 2016). A medium-voltage high-frequency isolated DC/DC converter is designed based on three-phase DAB converter in (Tripathi *et al.*, 2015). Moreover, a three-phase current-fed DAB converter is proposed in (Wang and Li, 2012). However, there is not a reference providing an overall design strategy for the three-phase DAB converter for wide input voltage range.

At the same time, the DAB topology including the three-phase DAB converter suffers from the low efficiency at light load conditions because the soft-switching will be lost. However, the Constant voltage (CV) charging phase as a typical light load condition will occur for long duration if Constant Current (CC) – Constant Voltage (CV) charge is applied (About *et al.*, 2015). Thus, how to improve the efficiency on the light load conditions is crucial for this application. In case to improve the efficiency, the methods can be classified into new modulation strategy and burst mode control For single-phase DAB topology, PWM plus phase-shift modulation is proposed, such as extended-phase-shift (EPS) (Zhao *et al.*, 2012b) and dual-phase-shift (DPS) (Zhao *et al.*, 2012a) are proposed to reduce the circulating current and the power loss of the single-phase DAB converter. However, these symmetric modulation methods are hard to apply to the three-phase DAB converter. Another modulation

schemes with the triangular and trapezoidal current modes have been adopted to realize the Zero-Current-Switching (ZCS) for the single-phase DAB converter in (Krismer and Kolar, 2012). A method to operate the triangular and trapezoidal modulations for the three-phase DAB converter is proposed by paralleling two phases with 180o phase shift angle to the third phase but the larger capacitors are needed (Van Hoek *et al.*, 2013). A simultaneous PWM control is proposed to operate the three-phase DAB converter under soft-switching in the whole load range (Huang *et al.*, 2015). Asymmetrical duty-cycle control is proposed for the soft-switching range extension in (Hu *et al.*, 2016). However, it's very complicated to apply in practice because there are too many operation modes. On the other hand, the burst model control is used to overcome the low efficiency at low power level where the switching losses dominate (Evzelman and Zane, 2016). A burst mode is proposed to improve the efficiency at light load conditions for the single-phase DAB converter (Rodríguez *et al.*, 2015). A switching sequence with burst mode is proposed to achieve higher efficiency than the conventional operation (Oggier and Ordonez, 2016). The operation range of the burst mode is limited by the needed capacitors which support energy during the converter turning off. An effective operation strategy should be proposed to improve the efficiency at the light load conditions.

2.3 Dead-time Effect in Dual-Active-Bridge Converter

Since the power switches have turn on and turn off delay time, a DC path exists between the supply lines if the "on" states of the two switching devices overlap in

half bridge or full bridge applications. This is called "cross conduction" and cause immediate failure. A dead-time will be introduced as the period at which both devices are off to prevent the cross conduction (Billings and Morey, 2010). So the dead-time is usually designed by the turn-on and turn-off delay time. On the other hand, the dead-time in DAB is also designed to ensure ZVS which depends on the oscillation time caused by the leakage inductance and the switch's stray capacitance (Van Hoek, 2017). However, when the dead-time is introduced, the deadband effect and phase shift error in the single phase DAB converter, was analysed for the short-time-scale transient processes in (Bai *et al.*, 2008). The operation and design of the single-phase DAB converter is studied in (Chris and Bai, 2008) and the dead-time effect of the primary H-bridge is analysed. Based on the experimental tests, the internal power transfer, phase drift, and low system efficiency are observed for the single-phase DAB converter in (Xie *et al.*, 2010). A new power flow model over a short time scale is proposed that incorporates additional parameters, including the power semiconductor voltage loss and dead time in (Xie *et al.*, 2010). Other dead-time effect phenomena, such as voltage polarity reversal and voltage sag, are observed (Zhao *et al.*, 2014b) as Figure 2.6 and a comprehensive theoretical analysis and experimental verification is studied for single-phase DAB converter.

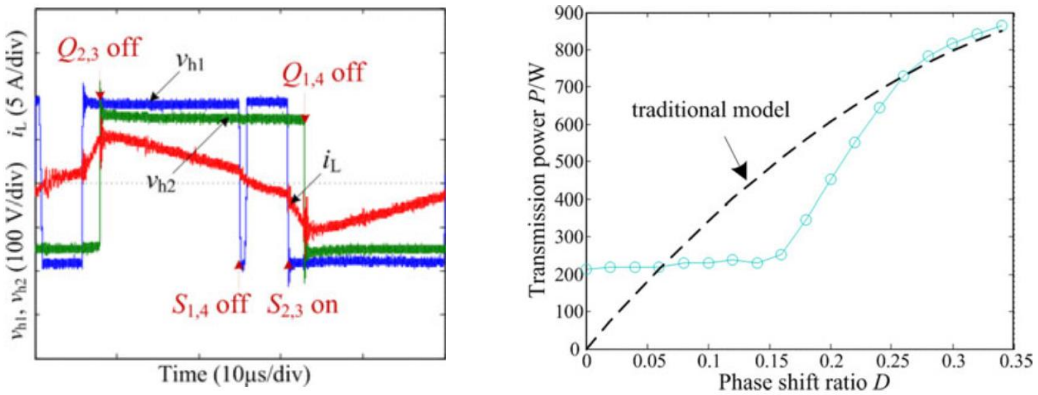


Figure 2.6: Dead-time effect phenomena observed in experimental waveforms of single-phase DAB converter: (a)Voltage Polarity Reversal Phenomenon. (b)Phase Drift Phenomenon.(Zhao *et al.*, 2014b).

Moreover, High switching frequency is desired for modern power converters because it can help shrink the size of the bulk passive components in the system (Zhang *et al.*, 2015a). Wide bandgap devices, like Silicon Carbide (SiC) and Gallium Nitride (GaN), enables the high switching frequency in the power electronics because of their low switching loss (Morsy and Enjeti, 2016). The dead-time effect is essential to design DAB converter with very high switching frequency (Costinett *et al.*, 2013). On the other hand, wide operation condition, input/output voltage and power, is required by power converters, like battery-interface DC/DC converters. However, the impact of the dead-time effect is more obvious when high switching frequency and wide operation range are required. Only one case of the dead-time effect in three-phase DAB converter is also observed in (Van Hoek, 2017). This thesis provides the comprehensive theoretical analysis for all the possible cases of the dead-time effect in three-phase DAB converter. In an effort to minimize the influence of the dead-time effect, dead-time compensation can be applied in the controller loop (Segaran *et al.*,

2013), most of which rely on the analytic closed-form expressions of the dead-time effect. Thus the comprehensive research of the dead-time effect should be proposed for the implementation of the three-phase DAB. Besides the dead time analysis presented in this thesis will provide an insight to the dead-time compensation of the three-phase DAB converter.

2.4 DC Bus Design for Two-Stage Single-Phase Inverter

The downstream single-phase inverter with DC bus capacitors are shown as Figure 2.7.

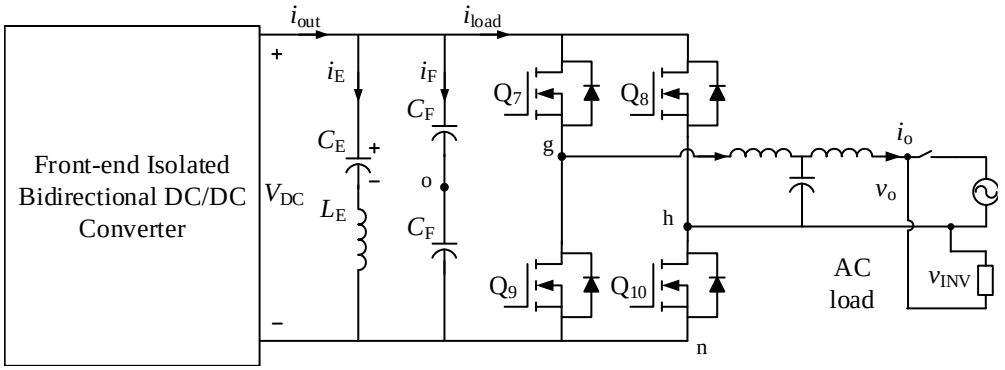


Figure 2.7: Downstream single-phase inverter with hybrid capacitor bank.

Since the single-phase inverter suffers from the double grid frequency harmonic on the DC-bus, power decoupling techniques are studied to deal with this problem (Tang and Blaabjerg, 2015; Hu *et al.*, 2013). A buck-type active filter is proposed to absorb the second-order current ripple as an active power decoupling method in (Ruxi *et al.*, 2011). An integrated dual-active-bridge converter based active filter is

proposed to filter the second order harmonic from on board battery charger (Hou and Emadi, 2017). However, the active components will increase the complexity of the whole system. Considering additional switches and their gate drivers, current sensors and inductors, the active power decoupling methods may not significantly reduce the space and size compared to the passive method. Thus, the passive power decoupling method is widely used in the commercial products because of simple structure and reliability. Capacitors are usually applied as the energy buffer with passive power decoupling method. In (Krein *et al.*, 2012), the minimum energy and capacitance requirements for the DC-bus capacitor are discussed. Besides, the double frequency harmonic, the high frequency harmonics still exist in the DC-bus. The high frequency harmonics caused by the PWM of the single-phase inverter needs to be considered when designing the DC-bus.

The capacitors used in DC-bus are discussed in (Wang and Blaabjerg, 2014) as Figure 2.8. Generally, Aluminum Electrolytic Capacitors is superior in the energy density and capacitance, which makes it suitable for the energy buffer purpose. The Metallized Polypropylene Film Capacitors is superior in terms of ripple current and frequency, which makes it suitable for the high frequency harmonics filtering purpose. The electrolytic capacitors are usually used as the energy buffer for the power decoupling purpose.

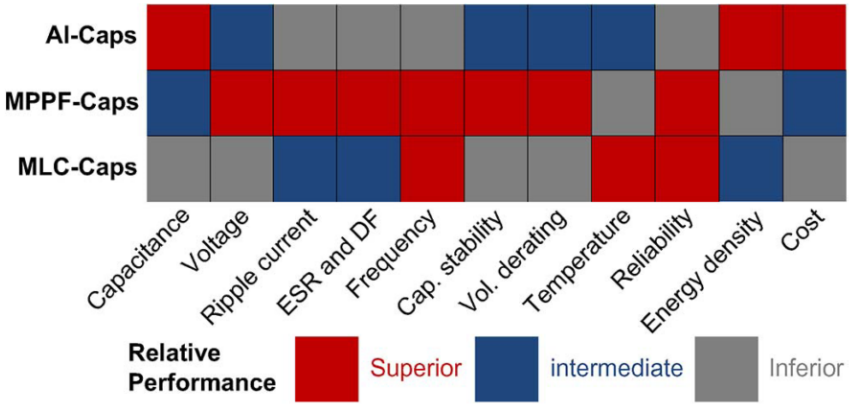


Figure 2.8: Performance comparisons of the capacitors for dc-link applications (Wang and Blaabjerg, 2014).

However, the life time of the electrolytic capacitor is limited by the RMS value of the ripple current. Thus, the electrolytic capacitor is usually oversized considering additional high frequency harmonics caused by PWM. Thus, it is feasible to design a DC-bus capacitor bank to combine the advantages of both electrolytic capacitor and film capacitor. Based on this idea, the electrolytic capacitor will be designed for the double frequency harmonic while the film capacitor will be designed to filtering out the high frequency harmonics. In addition, the resonant LC filter in DC-bus is employed in single-phase active rectifiers (Van Hoek, 2017) to avoid oversizing of the DC-bus capacitor and to obtain less voltage variation on the DC-bus. However, since the resonant frequency for LC filter is low, the weight and size of the additional inductor are considerable. Besides, the voltage across the capacitor of the LC branch may be higher than the maximum DC-bus voltage. In this thesis, a current sharing method is proposed that a reasonably small inductor is added in series with the electrolytic capacitor to form an LC resonant filter to further extend the life time of the electrolytic capacitor. At the same time, the size and cost of the system won't be

sacrificed too much. The hybrid capacitor bank, including film capacitors and the LC resonant filter with small inductor should be proposed for the single-phase inverter.

2.5 Single-Phase Inverter with Grid-Tied and Standalone Operation Modes

The full-bridge dual-buck inverter will convert DC bus voltage into AC output which will feed to utility grid or critical home load as backup power. Since the pulsating power exists in the output of the inverter, the input current of the inverter i_{INV}, contains averaged DC current, second harmonic current (SHC) and high-frequency switching harmonics if a stable voltage can be achieved on the DC bus. Decoupling method needs to be implemented to buffer the SHC so that only the averaged DC current can penetrate through the front-end converter while film capacitors will be utilized to filter the high-frequency switching harmonics. The assuming is made that the output impedance of the DC/DC converter is much greater than it of the passive decoupling capacitor bank which will be discussed next section. The single-phase inverter with dual grid-tied and standalone modes and passive decoupling method will be introduced in this section

As mentioned as the specifications in Section 1.1.3, the grid interface is a 120V split-phase system (180 degree out of phase) and therefore, the line to line voltage is 240V in North America. At the same time, another low power single-phase 120V AC output is always required in household application. The inverter operating with grid-tied mode will work as current source which synchronized with the grid voltage while the inverter with standalone mode can be seen as a voltage source to the AC

load as Figure 2.7.

For grid-tied mode, Total Harmonic Distortion (THD) and the maximum harmonic current distortion in percent of current are required in the IEEE 1547 (IEEE standards Coordinating Committee 21, 2009) standard as Table 2.1 which the inverter and controller design should follow.

Table 2.1: Maximum harmonic current distortion in percent of the fundamental current.

Individual harmonic order (odd harmonics)	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$
Percent(%)	4.0	2.0	1.5	0.6
Individual harmonic order (odd harmonics)	$35 \leq h$		Total demand distortion (THD)	
Percent(%)	0.3		Percent(%)	5.0

The standard for standalone operation of the inverter can be set as the same as the utility standard as in IEEE 519. More detail requirement of voltage distortion can be found in EN 50160 (CENELEC, 2005) as Table 2.2. Moreover, the THD of the supply voltage shall be less than or equal to 8%.

Table 2.2: Values of individual harmonic voltages at the supply terminals for orders up to 25 given in percent of fundamental voltage amplitude.

Odd harmonics				Even harmonics	
Not multiples of 3		Multiples of 3			
Order h	Relative voltage	Order h	Relative voltage	Order h	Relative voltage
5	6%	3	5%	2	2%
7	5%	9	1.5%	4	1%
11	3.5%	15	0.5%	6...24	0.5%
13	3%	21	0.5%		
17	2%				
19	1.5%				
23	1.5%				
25					

Unipolar SPWM of the single-phase inverter is widely utilized in grid-tied application because the dominating switching harmonic frequency with unipolar modulation is twice of the switching frequency. Thus the size of the output filter and DC-bus capacitors will be reduced a lot compared to those with bipolar SPWM. The comparison of the output voltage harmonics of the unipolar and bipolar SPWM for single-phase inverter is shown as Figure 2.9.

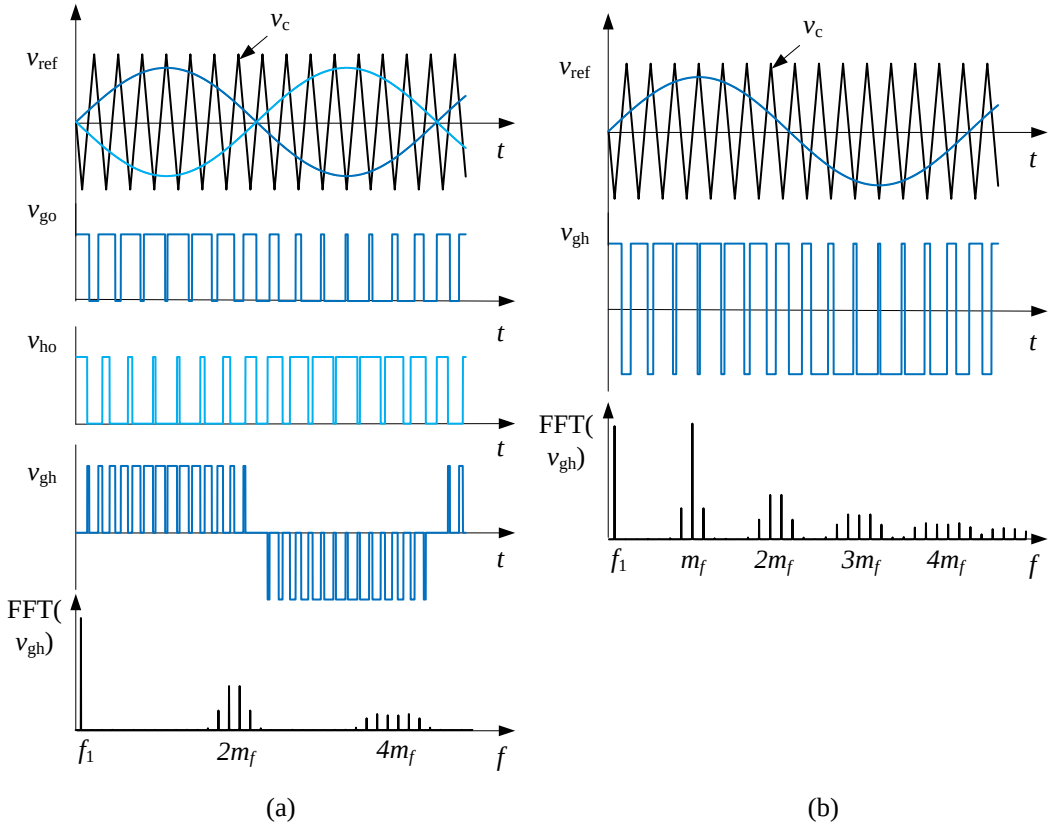


Figure 2.9: Harmonics comparison between the unipolar and bipolar SPWM for single-phase inverter: (a) Unipolar SPWM. (b) Bipolar SPWM.

The output filter of the single-phase inverter needs to be designed to fulfil the specifications and the standards. The LCL filter is widely utilized for grid-tied applications. Compared with L filter, the LCL filter composes a third order filter and can achieve higher attenuation in high frequency range. Thus, it helps to reduce the size and cost of passive component in the filter then increase the power density in the whole system. The LCL filter with active damping is proposed for low-voltage active-front-end PWM voltage source converters in (Jalili and Bernet, 2009). A step-by-step design of a LCL filter with passive damping is proposed for three-phase active rectifier in (Liserre *et al.*, 2005). In (Reznik *et al.*, 2014), a design methodology of LCL filter

for grid-interconnected inverter is proposed. Recently, a LLCL power filter is proposed (Wu *et al.*, 2012). The LLCL filter will obtain more attenuation at a certain high frequency but the slope of the filter is reduced from -60dB/decade to -20dB/decade in the other high frequency range which is not desired to filter other high frequency harmonic. A design of the LCL-based inverter with both grid-tied and standalone operations are discussed in (Chen *et al.*, 2008) but detailed design procedure based on IEEE requirements are not provided. A LCL filter step-by-step design procedure should be proposed to meet the standard constrains for both grid-tied operation and the standalone operation with same hardware.

The corresponding controller is essential for the single-phase inverter to achieve grid-tied and standalone operations. The PR controller based voltage-source converter is proposed in (Vazquez and Salmeron, 2006) and the advantages of PR controller than PI controller is disused. The admittance compensation in the current loop control is proposed for the LCL inverter in (Park *et al.*, 2008). A step-by-step controller design for LCL grid-tied inverter with active damping is proposed in (Bao *et al.*, 2014). A new feedback method for PR controller is discussed in (Shen *et al.*, 2010) however one more current sensor is needed. The drawback of the LCL filter is that it need certain damping method to suppress the magnitude at its resonant frequency. Compared with active damping, passive damping is cheaper, more robust and has no need of computation requirement of microcontroller. Hence, PR controllers are designed for standalone and grid-tied operations with passive damping in this thesis. To extend the capabilities of the PR controller, cascading several generalized integrators tuned to resonate at the desired frequency can be added in (Blaabjerg *et al.*, 2006). The phase locked loop (PLL) is utilized to synchronize with the grid

(Bhardwaj, 2013). The PR controllers should also be designed to achieve standalone and grid-tied mode.

2.6 Second Harmonic Current Reduction Strategy in Two-Stage Single-Phase Converter

The so-called "Second harmonic current" (SHC) will appear at the input of the downstream single-phase inverter because of its pulsating output power. With a constant voltage closed-loop control of the front-end DAB converter, the SHC will pass through the front-end converter to the input current of the battery (Zhu *et al.*, 2015). From the aging model of the Lithium-ion battery in (Ecker *et al.*, 2012), the extra Ah-throughput caused by SHC ages the battery faster than expected. The root-mean-square (RMS) value of the current flowing through the DAB converter is increased with the SHC so the switch and transformer current stress is increased and the system efficiency reduces. Moreover, the soft-switching can't be guaranteed with the extra SHC.

The mechanism of SHC is introduced in the system as Figure 2.7. Supposed the output voltage v_{o}, and the output current i_{o}, of the single-phase inverter is ideal sinusoid. They can be expressed as (2.1) and (2.2).

$$v_o = V_o \sin(\omega_0 t) \tag{2.1}$$

$$i_o = I_o \sin(\omega_0 t - \varphi) \tag{2.2}$$

where V_{o} and I_{o} are the amplitude of the output voltage and output current. ω_{o}

is the angular frequency of the output inverter, $\omega_o = 2\pi f_o$, and f_o is the fundamental frequency of the inverter. φ is the phase angle of the output. Then the instantaneous power can be expressed as (2.3).

$$p_o = v_o i_o = \frac{1}{2} V_o I_o \cos(\varphi) - \frac{1}{2} V_o I_o \cos(2\omega_o t - \varphi) \tag{2.3}$$

Assuming the power loss of the system and the switching harmonics of the inverter are neglected, the power on the input of the downstream inverter is (2.4).

$$p_i = p_o = V_{Bus} i_{load} = \frac{1}{2} V_o I_o \cos(\varphi) - \frac{1}{2} V_o I_o \cos(2\omega_o t - \varphi) \tag{2.4}$$

If the crossover frequency of the voltage close-loop controller is high enough, the voltage on the DC bus is assumed to be constant. Then the output current of the front-end converter is (2.5).

$$i_{load} = \frac{1}{2} \frac{V_o I_o \cos(\varphi)}{V_{Bus}} - \frac{1}{2} \frac{V_o I_o}{V_{Bus}} \cos(2\omega_o t - \varphi) \tag{2.5}$$

From (2.5), there is a sinusoid current with twice the fundamental frequency $2f_o$, and as high amplitude as the DC component. To the front-end DC/DC converter, the downstream inverter is simplified as a resistor in parallel with a sinusoid current source based on (2.5). The so-called "second-harmonic-current" (SHC) is supposed to be absorbed by the DC bus capacitor bank. The extreme example is that there is no variation in DC bus voltage with a high bandwidth voltage controller then no energy will be storage in DC bus capacitor bank based on $E = 1/2 \cdot C\Delta V^2$. The SHC will flow through the switches and transformer of the DAB converter finally to the input

battery source. It will increase the hardware current stress. Moreover, the input current of the front-end DC/DC converter including second order harmonics which also accelerate battery aging supposing the capacitors on the battery side capacitor is not increased. Thus the SHC should be suppressed for the system.

To mitigate the SHC issue, more DC bus capacitors can be added however the power density of the system reduces with the bulk capacitor bank (Krein *et al.*, 2012). On the other hand, an inductor can be used in series at the output of the three-phase DAB converter thus a current closed-loop control with high crossover frequency can be applied however the stability of the system should be carefully considered since the closed-loop single-phase inverter can be seen as a constant power load to the front-end converter (Emadi *et al.*, 2006). Instead of the bulk capacitor bank, the active decoupling method can be utilized to solve the SHC issue (Ruxi *et al.*, 2011; Vitorino *et al.*, 2017) but extra circuit will lead to more power loss and complexity to the system.

Another category to suppress SHC is to apply a new control scheme of the front-end converter. The most straightforward way is to lower the crossover frequency of the voltage closed-loop converter than $2f_{\mathrm{o}}$ however the corresponding poor dynamic performance during load transient will be expected, especially the large overshoot which will increase the switches and DC bus capacitor stress and the large. A notch filter with characteristic frequency tuned at 2fo can be inserted to achieve a small voltage loop gain at $2f_{\mathrm{o}}$ (Jung *et al.*, 2011; Ksiazek and Ordonez, 2014) however a large negative phase-shift at the frequencies lower than 2fo which will jeopardize the stability of the system. Furthermore, a feedback path (Zhang *et al.*, 2014) of the inner inductor current with a bandpass filter (BPF) or a feedforward path of the load

current with a notch filter can be added from the perspective of the output impedance (Zhu *et al.*, 2015). Virtual impedance is introduced to be in series with the original output impedance while the other one is in parallel with the intermediate DC bus capacitor which makes the output impedance relative high at $2f_o$ but relative low at the frequencies other than $2f_o$ (Zhang *et al.*, 2015b). The strategy is claimed to reduce SHC and improve dynamic performance at the same time. The idea also can be applied for the boost-derived converters in (Zhang *et al.*, 2017). However, the dual feedback path and feedforward path make the stability analysis more complicated and some strategies insert a notch filter or a BPF in the close loop which maybe make the system instable. The virtual impedance idea can also be appllied to improve the stability of the system (Karbalaye Zadeh *et al.*, 2016; Cai *et al.*, 2015). Also the virtual impedance can be added to improve injected grid current quality (Chen *et al.*, 2018). On the other hand, by controller the DC bus voltage waveform can ensure all SHC is absorbed by the DC bus capacitors (Kwon *et al.*, 2009). This SHC reduction strategy only with load current feedforward (LCFF) path won't influence the stability analysis of the close-loop controller so that it makes the controller design much easier. The DC bus voltage reference modification method with LCFF is made to suppress SHC for the buck-derived converter in (Shi *et al.*, 2016). A modified reference of DC bus voltage with LCFF for SHC reduction method is researched for the DAB topology based standalone photovoltaic power system in (Wang and Ruan, 2016). However, the crossover frequency of the controller should be much higher than $2f_o$ or a PIR controller has to be designed if a better SHC reduction performance wants to be achieved. Also the parameter sensitivity analysis is not provided for the feedforward control. A new SHC reduction strategy is essential for the system.

2.7 Proposed Configuration of Isolated Battery-Driven Grid Interface

The proposed configuration for IBDGI with three-phase DAB converter is shown as Figure 2.10. The three-phase DAB converter is utilized to achieve high power density and efficiency as its front-end converter. LCL inverter is applied for grid-tied and standalone operation purpose. Hybrid capacitor bank will serve as passive decoupling for the whole system.

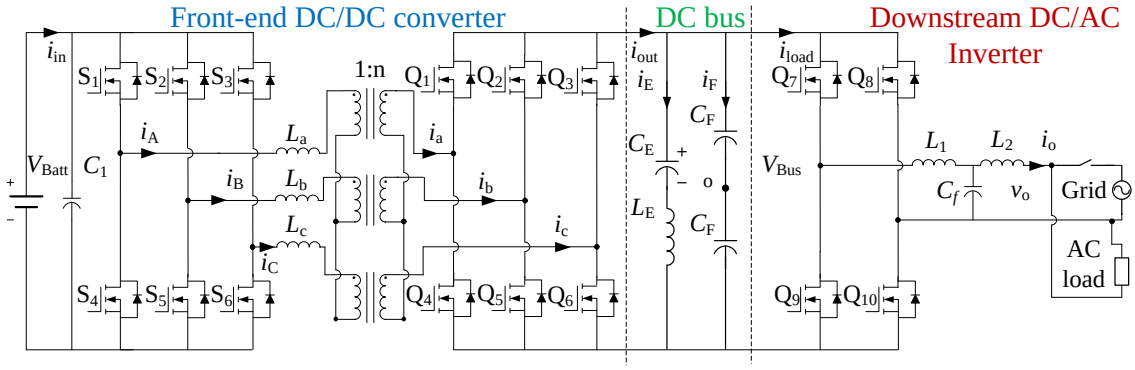


Figure 2.10: Proposed topology for the isolated battery-driven grid interface with the three-phase DAB converter.

2.8 Conclusion

The topologies of IBDGI in this chapter. Two-stage topology is the most promising because high-frequency isolation method can be effectively provided at the front-end DC/DC converter. Among the isolated bidirectional DC/DC converter, DAB topology is widely researched since high efficiency can be achieve due to the naturally ZVS for all the switches while the three-phase DAB converter is an excellent candidate

because of the low capacitance requirement. However, a comprehensive design strategy of the three-phase DAB converter needs to be proposed. At the same time, the dead-time effect of the three-phase DAB converter is also essential to be researched. LCL inverter can be applied to link the DC bus and AC output due to its smaller filter size. The passive decoupling method with hybrid capacitor bank should be utilized because of its reliable and simple structure. Moreover, the SHC reduction strategy is crucial for two-stage DC/AC inverter with stable DC bus. Then based on the analysis in the chapter, the configuration of the IBDGI system is proposed with the three-phase DAB converter.

Chapter 3

Three-Phase Dual-Active-Bridge Converter Design Strategy

3.1 Introduction

The three-phase dual-active-bridge (DAB) converter as Figure 3.1 is a promising candidate applied as the front-end converter of IBDGI because of its high efficiency, power density and low capacitance requirement. The design strategy of the three-phase DAB converter based on the zero-voltage-switching (ZVS) zone and back-flow power is proposed to achieve high efficiency for wide operation voltage range and load conditions. The power loss model of the converter is analyzed and the design strategy is verified by the efficiency analysis. However, low efficiency at light load conditions of the battery-interface three-phase DAB converter needs to draw enough attention considering the constant voltage (CV) charging phase of the CC-CV charging scheme of Li-ion battery. An easily-applied variable switching frequency method is proposed to improve the efficiency at light load conditions, such as CV charging phase, for the

three-phase DAB converter by minimizing the switching loss. The simulation and experimental results are utilized to verify the design strategy and variable switching frequency method.

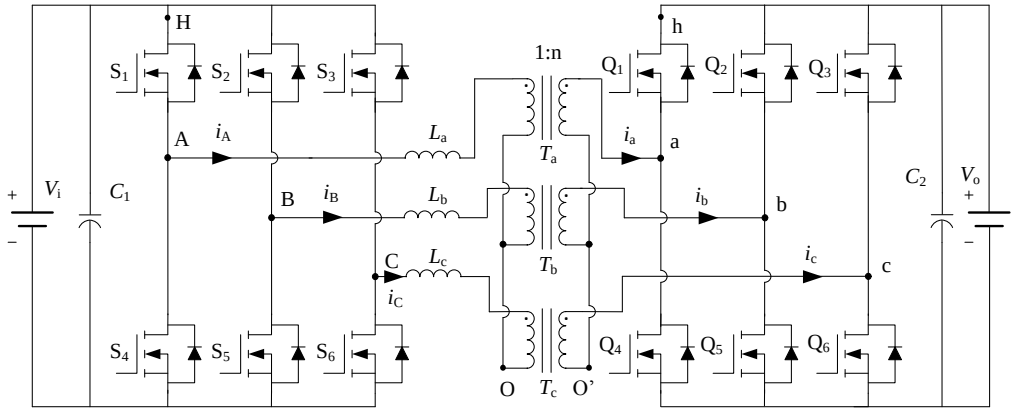


Figure 3.1: Topology of the three-phase DAB converter.

The organization of this chapter is as follows: Section 3.2 will describe the design strategy in the three-phase DAB topology. Section 3.3 presents the verification of the design strategy considering the efficiency map. Section 3.4 will present a variable switching frequency method to improve the efficiency at light load conditions. In Section 3.5, the experiment results will be presented to validate the simulation results. Finally, Section 3.6 concludes the finding and contributions of this chapter.

3.2 Design Strategy of the Three-Phase DAB Converter

The step-by-step design strategy of the three-phase DAB converter with single-phase-shift (SPS) modulation is proposed in this section. Based on the discussion above, the

SPS is utilized because of its simplicity and naturally achieved ZVS for all switches. The topology of the three-phase DAB converter is shown as Figure 2.4. The specifications are shown as Table 3.1. A typical 48V battery pack is used whose input voltage range is 42V-58V while 400V is selected as the DC bus voltage in case to cover the peak voltage of single-phase inverter which is $240\sqrt{2}V$. Three individual transformers connected as Y-Y are utilized because more flexibility can be achieved. The turn ratio of the transformers n, leakage inductance L of the transformer and the switching frequency f are the main parameters which should be designed for the three-phase DAB converter. The design requirements are to achieve high efficiency for the half load to full load operation in whole input voltage range. High switching frequency is required to achieve high power density. Planar transformer is utilized to further improve the power density by achieving a flat design (Cui Ying, 2017).

Table 3.1: Specifications of the three-phase DAB converter.

Input voltage	48V norminal (42V-58V)
Outputvoltage	400V
Power rating	3kW
Other	Flat design

3.2.1 Operation Expression

In Section 2.2.2, the operation waveforms of the three-phase DAB converter is illustrated as Figure 2.5. There are two available operation modes where the phase shift range are $0 - \pi/3$ and $\pi/3 - 2\pi/3$. After analyzing the current relationship of the leakage inductance, the current on the primary side of the transformer can be

expressed as (3.1) where the equivalent conversion ratio $d = V_{\rm o}/nV_{\rm i}$ is introduced.

$$\begin{cases} i_0 = \dfrac{dV_o(2\pi d - 2\pi - 3d\phi)}{18\pi nfL} \\ i_1 = \dfrac{dV_o(3\phi - 2\pi + 2\pi d)}{18\pi nfL} \\ i_2 = \dfrac{dV_o(3d\phi - \pi + \pi d)}{18\pi nfL} \\ i_3 = \dfrac{dV_o(6\phi - \pi + \pi d)}{18\pi nfL} \\ i_4 = \dfrac{dV_o(\pi + 6d\phi - \pi d)}{18\pi nfL} \\ i_5 = \dfrac{dV_o(3\phi + \pi - \pi d)}{18\pi nfL} \end{cases} \qquad 0 \le \phi \le \frac{\pi}{3} \tag{3.1a}$$

$$\begin{cases} i_0 = \dfrac{dV_o(3\pi d - 2\pi - 6d\phi)}{18\pi nfL} \\ i_1 = \dfrac{dV_o(3\phi - 3\pi + \pi d)}{18\pi nfL} \\ i_2 = \dfrac{dV_o(3\pi d - 3d\phi - \pi)}{18\pi nfL} \\ i_3 = \dfrac{dV_o(6\phi - 3\pi + 2\pi d)}{18\pi nfL} \\ i_4 = \dfrac{dV_o(\pi + 6d\phi)}{18\pi nfL} \\ i_5 = \dfrac{dV_o(3\phi + \pi d)}{18\pi nfL} \end{cases} \qquad \frac{\pi}{3} < \phi \le \frac{2\pi}{3} \tag{3.1b}$$

As Figure 2.4, $V_{\rm i}$ is the input voltage on the primary side while $V_{\rm o}$ is the output voltage on the secondary side, ϕ is the applied phase shift, n is the turn ratio of the transformer form the primary side to the secondary side, f is the switching frequency and L is the leakage inductance converted in the primary side. The instantaneous transmission power of the converter can be derived by three times the product of

the phase current and voltage of the transformer. Assuming there is no power loss, the transmission power can be expressed as (3.2) by averaging the instantaneous transmission power.

$$P = \begin{cases} \frac{V_o^2}{2\pi n^2 f L} d^3 \phi (\frac{2}{3} - \frac{\phi}{2\pi}) & 0 \leq \phi \leq \frac{\pi}{3} \\ \frac{V_o^2}{2\pi n^2 f L} d^3 (\phi - \frac{\phi^2}{\pi} - \frac{\pi}{18}) & \frac{\pi}{3} < \phi \leq \frac{2\pi}{3} \end{cases} \tag{3.2}$$

Then the conversion ratio d can be reshaped as 3.3.

$$d = \frac{V_o}{nV_i} = \begin{cases} K \frac{\phi}{2\pi} (\frac{2}{3} - \frac{\phi}{2\pi}) & 0 < \phi < \frac{\pi}{3} \\ K[\frac{\phi}{2\pi} - \frac{1}{36} - 2(\frac{\phi}{2\pi})^2] & \frac{\pi}{3} < \phi < \frac{2\pi}{3} \end{cases} \tag{3.3}$$

Where $K = V_o^2/(n^2 L f P)$. K value is an important parameter when designing the converter because it related with the output voltage, the transmission power and the three-phase DAB design parameters (n, L and f). To better design and analyze the converter, the operation of three-phase DAB converter can be represented as Figure 3.2 where all the operation points are described by conversion ratio d and phase shift value ϕ. In Figure 3.2, K can also be expressed as the blue lines. With a designed converter (n, L and f are selected), K value will represent the power condition of the converter. Larger K value means smaller transmission power P.

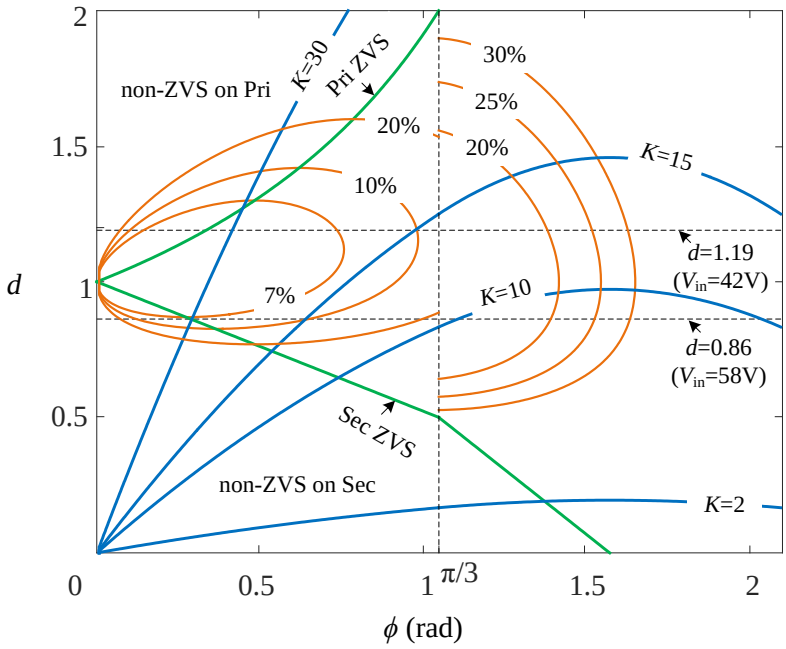


Figure 3.2: Operation illustration of the three-phase DAB converter: blue lines represent K value; green lines represent the ZVS conditions; orange lines represent the back-flow power ratio.

3.2.2 ZVS Conditions

The turn-on soft-switching, ZVS, can be achieved for all switches of the three-phase DAB converter. Negative current goes through the switch before it's turned on thus the body diode will be conducted if enough dead-time is guaranteed. In this way, the voltage of the switch will keep zero during turn on so the turn-on switching loss is zero and soft-switching is achieved. A rough ZVS condition for the converter is the negative current of the switch before turn on. Based on the analysis of the circuit and the operation mode $0 < \phi < \pi/3$, i_0 and $-i_1/n$ is the instantaneous current that S_1 and Q_1 turn on. So $i_0 < 0$ and $i_1 > 0$ are the ZVS conditions of switches on the primary side and secondary side. Following the same analysis, $i_0 < 0$ and $i_2 > 0$ are

the ZVS conditions of switches on the primary side and secondary side for operation mode $\pi/3 < \phi < 2\pi/3$. Put equation (3.3) into the ZVS conditions, the (3.4) can be derived.

$$\begin{cases} 1 - \dfrac{3\phi}{2\pi} < d < \dfrac{1}{1 - \dfrac{3\phi}{2\pi}} & 0 < \phi < \dfrac{\pi}{3} \\ \dfrac{3}{2} - \dfrac{3\phi}{\pi} < d < \dfrac{1}{\dfrac{3}{2} - \dfrac{3\phi}{\pi}} & \dfrac{\pi}{3} < \phi < \dfrac{2\pi}{3} \end{cases} \tag{3.4}$$

The ZVS conditions can be expressed as green curves in Figure 3.2 where the operation points in the center area can achieve soft-switching on both primary and secondary side. To improve the efficiency of the converter, we want to operate it during the center area as much as possible so nominal input voltage operate can selected as $d = 1$ (Alonso *et al.*, 2010). So the turn ratio of the transformers n can be chosen as 8. The input voltage range 42V-58V can be shown as the dash lines in Figure 3.2 in the middle range between $d = 1.19$ and $d = 0.86$. Higher K value means lower transmission power. Observed from Figure 3.2, narrower ZVS zone will be obtained with higher K which can also explain the soft-switching will be hard to achieve at light load conditions.

3.2.3 Back-flow Power Ratio

The single-phase DAB topology with SPS modulation suffers from the so-called back-flow power which can be seen as (Alonso *et al.*, 2010; Zhao *et al.*, 2014c). EPS and DPS modulations are solutions for the single-phase DAB (Zhao *et al.*, 2012b) however it's hard to be applied in the three-phase DAB topology. The back-flow power of the three-phase DAB converter is still observed in Figure 2.5. This negative power won't contribute to the transmission power but flow back to primary side $Q_{\mathrm{b,pri}}$ and

secondary side $Q_{\mathrm{b,sec}}$ which increase the device stress and power loss of the system. Thus, to better design of the converter, the back-flow power should be kept as small as possible for the whole operation. The back-flow power can be represented by the back-flow power ratio r which is the ratio between back-flow power and its corresponding transmission power as equation (3.5).

$$\begin{cases} r = \dfrac{Q_{\mathrm{b,pri}}}{P_{\mathrm{o}}} + \dfrac{Q_{\mathrm{b,sec}}}{P_{\mathrm{o}}} = \dfrac{(2\pi + 3\phi d - 2\pi d)^2}{9(d+1)d\phi(4\pi - 3\phi)} + \dfrac{(3\phi - 2\pi + 2\pi d)^2}{9(d+1)\phi(4\pi - 3\phi)} & 0 < \phi < \dfrac{\pi}{3} \\ r = \dfrac{Q_{\mathrm{b,pri}}}{P_{\mathrm{o}}} + \dfrac{Q_{\mathrm{b,sec}}}{P_{\mathrm{o}}} = \dfrac{(3\phi - 3\pi + \pi d)^2 - (3\phi - \pi)(3\phi - 5\pi - 6d\phi + 4\pi d)(d+1)}{3(18\pi\phi - \pi^2 - 18\phi^2)d(d+1)} & \\ + \dfrac{(\pi + 3d\phi - 3\pi d)^2 + (3\phi - \pi)(6\phi - 4\pi - 3d\phi + 5\pi d)(d+1)}{3(18\pi\phi - \pi^2 - 18\phi^2)(d+1)} & \dfrac{\pi}{3} < \phi < \dfrac{2\pi}{3} \end{cases} \tag{3.5}$$

From the equation, we can notice that the back-flow power ratio is only based on the conversion ratio d and the phase shift value ϕ. Thus the value can be referred as a universal design of the three-phase DAB converter. In Figure 2.5(b), higher back-flow power ratio will occur when $\pi/3 < \phi < 2\pi/3$ which can also be observed as the orange curves in Figure 3.2. In case to achieve higher efficiency and lower device stress, the three-phase DAB converter should be designed with operation mode $0 < \phi < \pi/3$.

3.2.4 Design Strategy

Based on the analysis above, the design requirements of the three-phase DAB converter are 1) wider ZVS zone should be achieved to obtain high efficiency for the wide input voltage range which is chosen as $d = 1$ when $V_{\mathrm{i}} = 48V$; 2) operation mode $0 < \phi < \pi/3$ should be utilized to keep low back-flow power ratio; 3) high efficiency should be guaranteed from half load to full load condition.

Based on the analysis, the 58V input voltage at half load condition is the worst

case which is point A in Figure 3.3 in case to achieve ZVS for whole voltage range $0.86 < d < 1.19$ at half load condition. Based on the $d = 0.86(V_{\text{i}} = 58V)$ and equation, the phase shift value ϕ is 0.289. Then $d = 0.86$ and $\phi = 0.289$, K can be calculated as 30.2 from the (3.3). Thus the $K = 15$ represents the full load condition of the converter in Figure 3.3.

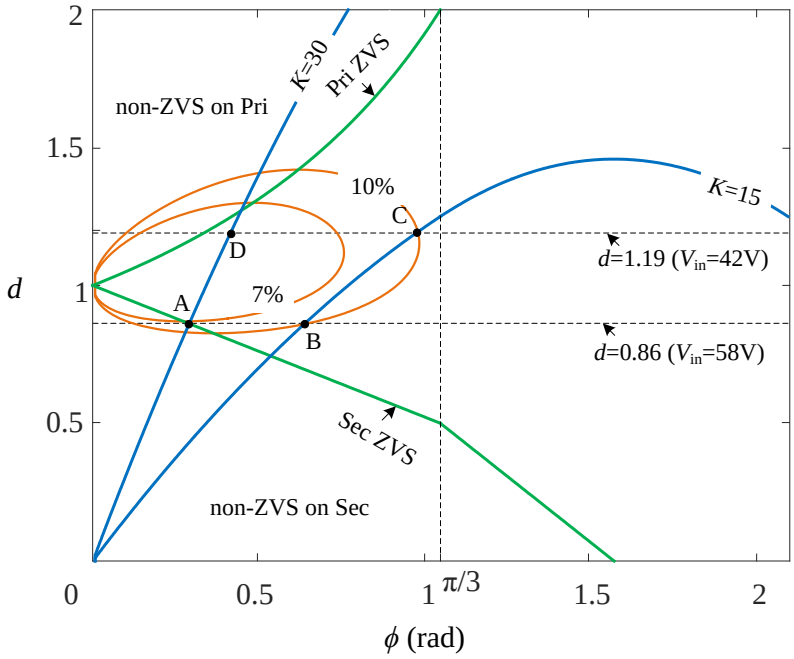


Figure 3.3: Design diagram of the three-phase DAB converter.

The area ABCD in Figure 3.3 is the operation range to achieve ZVS for 42V-58V input voltage range and from half load to full load conditions. All the operation area is within operation mode $0 < \phi < \pi/3$ and the area is within the ZVS condition zone. At the same time, the back-flow power ratio for the area is less than 10%. All the design requirements are fulfilled. From $K = V_{\text{o}}^2/(n^2LfP)$, the product of L and f can be calculated as $Lf = V_{\text{o}}^2/(n^2KP) = 0.056\text{H} \cdot \text{Hz}$. 100kHz switching frequency is selected as the tradeoff between the size of the converter and its power loss. Then

the leakage inductance of the transformer is $0.56\mu H$ converted on the primary side. Until now, the three-phase DAB converter is designed. The required capacitance on the primary side and secondary side can be calculated as (3.6) and (3.7) respectively.

$$C_1 = \frac{25(9d\phi^2 - 6\pi d\phi + 2\pi^2 d - 2\pi^2)^2}{216f^2L\pi^4(2-d)} \tag{3.6}$$

$$C_2 = \frac{25(9\phi^2 - 2\pi^2 d + 2\pi^2 - 12\pi\phi + 12\pi d\phi)^2}{432f^2Ld\pi^4(d-1)} \tag{3.7}$$

The sizing of the applied switches can base on (3.8) and (3.9).

$$i_{\text{Pri,RMS}} = \frac{dV_o\sqrt{-27\phi^3d^2 - 27\phi^3d + 27\pi\phi^2d^2 + 27\pi\phi^2d + 2\pi^3d^2 - 4\pi^3d + 2\pi^3}}{36\sqrt{2}\pi\sqrt{\pi}nfL} \tag{3.8}$$

$$i_{\text{Sec,RMS}} = \frac{dV_o\sqrt{-27\phi^3d - 27\phi^3 + 27\pi\phi^2d + 27\pi\phi^2 + 2\pi^3d^2 - 4\pi^3d + 2\pi^3}}{36\sqrt{2}\pi\sqrt{\pi}n^2fL} \tag{3.9}$$

3.3 Verification of the Three-Phase DAB Design Strategy

The three-phase DAB converter is roughly designed by last section however this design strategy still needs to be verified by the efficiency map. The power loss model will be used and a ZVS condition from the energy aspect will be discussed.

3.3.1 Power Loss Model

An accurate power loss model of the single phase DAB converter can be seen in (Krismer and Kolar, 2010). The power loss is analyzed for the three-phase DAB

converter in (Van Hoek, 2017). The power loss model includes the switches' loss, the transformers loss and the add-on inductor power loss. The power loss of the MOSFET includes conduction loss and switching loss and the transformer loss has winding loss and core loss.

$$P_{\text{loss}} = P_{\text{tran,winding}} + P_{\text{tran,core}} + P_{\text{sw,conduction}} + P_{\text{sw,switching}} + P_{\text{ind}} \tag{3.10}$$

Power Loss Model of MOSFET Switches

The analytical loss model of the MOSFET switches can mainly be divided by conduction loss and switching loss (Lee, 2006). The conduction loss of the switches can be calculated by (3.11), where $R_{\text{DS(on)}}$ is the on-resistance of the MOSFET switch and $I_{\text{sw,RMS}}$ is the RMS value of the current going through the MOSFET which can be found by (3.8) and (3.9).

$$P_{\text{sw,conduction}} = \frac{1}{T}\int_0^T \left(R_{\text{DS(on)}} \cdot i_{\text{D}}^2(t)\right) dt = R_{\text{DS(on)}} \cdot I_{\text{sw,RMS}}^2 \tag{3.11}$$

The switching loss of the MOSFET can be calculated by (3.12).

$$P_{\text{sw,switching}} = (E_{\text{onM}} + E_{\text{offM}}) \cdot f \tag{3.12}$$

The turn-on and turn-off energy of MOSFET can be calculated as (3.13).

$$E_{\text{onM}} = \begin{cases} U_{\text{DS}} I_{\text{DSon}} \cdot \dfrac{t_{on}}{2} & \text{non} - \text{ZVS} \\ 0 & \text{ZVS} \end{cases} \tag{3.13}$$
$$E_{\text{offM}} = U_{\text{DS}} I_{\text{DSoff}} \cdot \frac{t_{off}}{2}$$

Where $t_{on} = t_{ri} + t_{fu}$ and $t_{off} = t_{ru} + t_{fi}$. The voltage across the switches equals to the voltage level V_i and V_o. The turn-on and turn-off instantaneous current of the switches on the primary side can be expressed as i_0 and $-i_0$ from (3.1). Also the turn-on and turn-off instantaneous current of the switches on the secondary side can be expressed as $-i_1/n$ and i_1/n from (3.1). From (Guo, 2017), the falling time and rising time of the voltage and current can be estimated from the information of the datasheet and the gate driver design as (3.14).

$$\begin{cases} t_{fu} = (U_{dc} - R_{DS(on)} \cdot i_{ds}) \cdot R_g \cdot C_{rss} \cdot \dfrac{1}{V_{drive} - V_{plateau}} \\ t_{ru} = (U_{dc} - R_{DS(on)} \cdot i_{ds}) \cdot R_g \cdot C_{rss} \cdot \dfrac{1}{V_{plateau} - V_{drive,n}} \\ t_{fi} = R_g \cdot C_{iss} \cdot \ln \dfrac{V_{plateau} - V_{drive,n}}{V_{th} - V_{drive,n}} \\ t_{ri} = R_g \cdot C_{iss} \cdot \ln \dfrac{V_{drive} - V_{th}}{V_{drive} - V_{plateau}} \end{cases} \tag{3.14}$$

Where R_g, V_{drive} and $V_{drive,n}$ are the gate resistance, positive gate driver voltage and negative gate driver voltage. C_{rss}, C_{iss}, V_{th} and $V_{plateau}$ are the stray capacitance, threshold voltage and plateau voltage which can be found from datasheet. IPP045N10N3 MOSFET and C3M0065090D SiC MOSFET are selected as the switches on the primary side and secondary side.

Transformer Power Loss Model

The planar core E64 with Ferrite N87 material is utilized to design the planar transformer. From (Cui Ying, 2017), the core loss of three transformers can be calculated

by Steinmetz equation as (3.15).

$$P_{\text{tran,core}} = K_{\text{tran}} \cdot f^{\alpha} \cdot (\Delta B/2)^{\beta} \tag{3.15}$$

Where K_{tran}, α and β are constants provided by the manufacturer and ΔB is the peak-to-peak flux density that can be obtained from Faraday's law. The transformer copper loss can be calculated by (3.16).

$$P_{\text{tran,winding}} = 3 \cdot I^2_{\text{rms\_tf}} \cdot (R_{ac} + R_{dc}) \tag{3.16}$$

Where the R_{ac} is the AC resistance of the windings by taking eddy current effect into consideration and R_{dc} is the resistance of the transformer converted to the primary side. The RMS value of the current going through the transformer on the secondary side is as (3.17).

$$i_{\text{TSec,RMS}} = \frac{dV_o\sqrt{3}\sqrt{-27\phi^3 d + 54\pi\phi^2 d + 5\pi^3 d^2 - 10\pi^3 d + 5\pi^3}}{54\pi n^2 f L\sqrt{\pi}} \tag{3.17}$$

The ratio between AC resistance R_{ac} and DC resistance R_{dc} can be described by (3.18).

$$\frac{R_{ac}}{R_{dc}} = \frac{\xi}{2}\left[\frac{\sinh\xi + \sin\xi}{\cosh\xi - \cos\xi} + (2m-1)^2 \cdot \frac{\sinh\xi - \sin\xi}{\cosh\xi + \cos\xi}\right] \tag{3.18}$$

where $\xi = h/\delta$, h is the conductor thickness, δ is the skin depth at a certain frequency. Ratio m comes from planar transformer design.

3.3.2 Design Verification

Based on the power loss model, the efficiency map can incorporate into design diagram Figure 3.2 then a new diagram with efficiency is illustrated as Figure 3.4. Although the ZVS condition of the DAB converter can be roughly obtained by (3.4). Actually, the absolute value current should be large enough to ensure the energy storage in the inductor larger than it in the stray capacitance of the switching device (Rodríguez *et al.*, 2015). It can be seen as 3.19. Then a more strict ZVS condition regarding the energy is shown as the light green curves as Figure 3.4.

$$E_{L_k} > 2E_{C_{oss}} \rightarrow \frac{1}{2}Li^2 > 2 \cdot \frac{1}{2}V^2 \int_0^V C_{oss}(v)dv \tag{3.19}$$

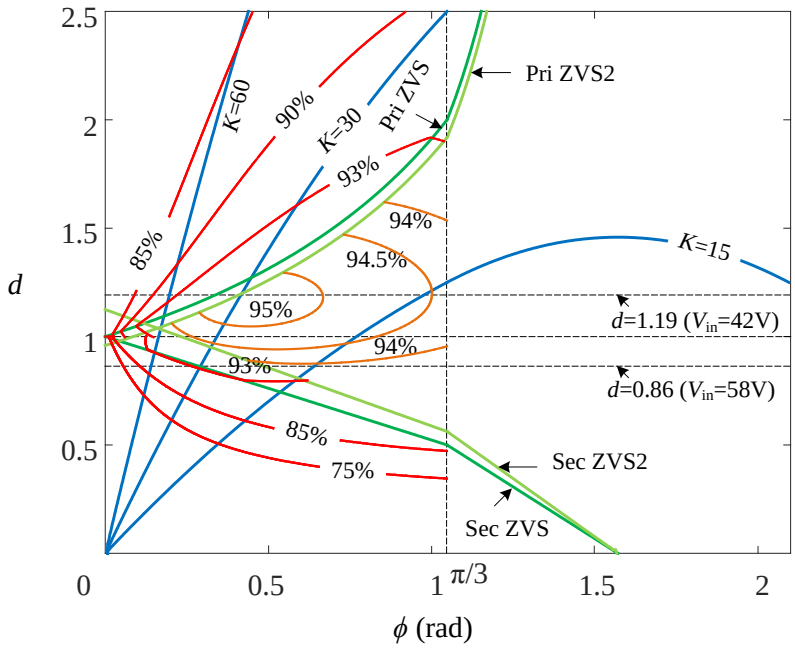


Figure 3.4: Design verification diagram of the converter: blue lines represent K value; dark green lines represent the rough ZVS conditions; light green lines represent the strict ZVS conditions; orange lines represent the efficiency within ZVS zone; red lines are the efficiency curves losing ZVS.

Three blue lines, $K = 15$, $K = 30$ and $K = 60$ represents the full load, half load and quarter load conditions respectively. Observed from Figure 3.4, the efficiency from half load to full load conditions for whole voltage range is above 93% although the ZVS is lost for high input range ($d < 1$) because of the strict ZVS condition.

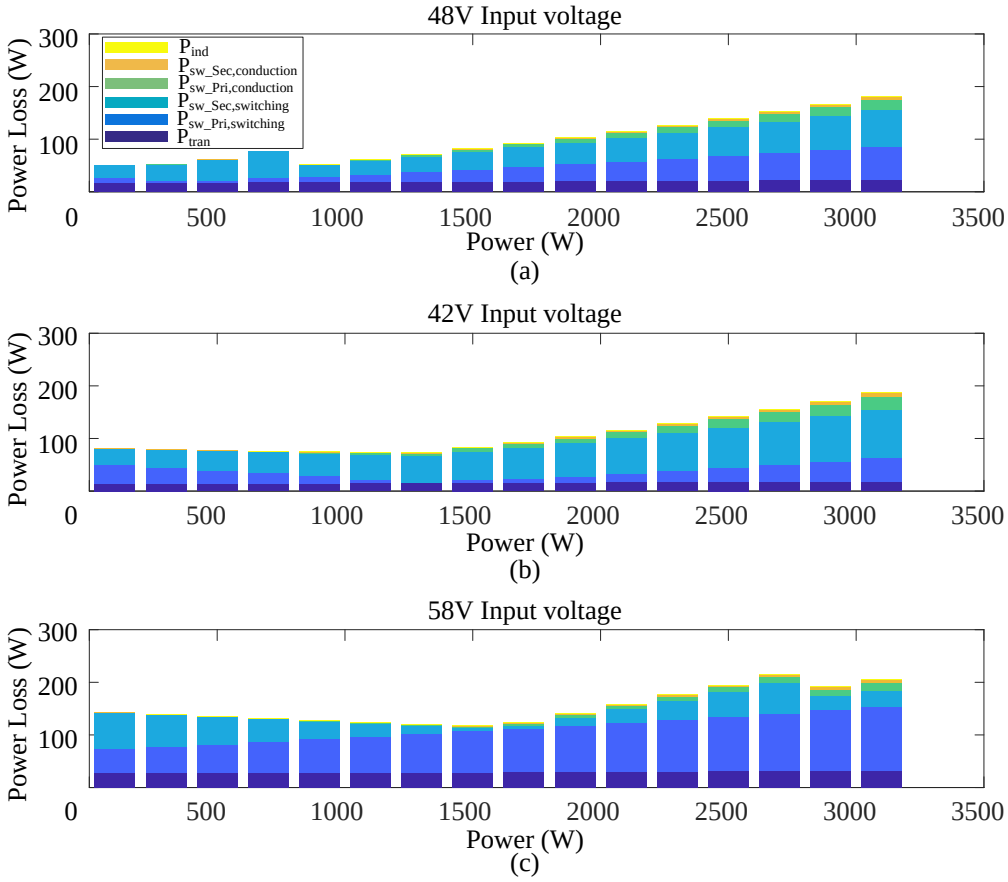


Figure 3.5: Power loss breakdown with constant switching frequency operation in different input voltage level: (a) 48V input voltage. (b) 42V input voltage. (c) 58V input voltage.

However, lower efficiency at the power rating lower than the half load is achieved by this design, especially the d is not equals to 1. Dramatically efficiency drop is observed across the dark green curves in Figure 3.4 when the power rating decreases.

Among them, the efficiency at $d < 1$ is lower at light load conditions. The power loss breakdown can be shown as Figure 3.5. The Lowest power loss will be achieved at 48V input voltage. More power loss will occur for 58V input voltage at light load conditions.

3.4 Variable Switching Frequency Operation for Efficiency Improvement at Light Load Conditions

Based on the analysis above, the three-phase DAB converter is designed with a high efficiency from half power rating to full power rating for whole voltage range. However, the efficiency is still low when the power is lower than half power rating especially the equivalent conversion ratio d is not 1. To improve the efficiency of the converter during the CV charging phase which can be considered as light load conditions, an easily-applied increasing switching frequency strategy is proposed by minimizing the power loss. The lowest switching frequency mainly depends on the saturation of the selected core for the transformer. Lower switching frequency will lead to saturation of the transformer or a bigger core size so only increasing switching frequency is acceptable. On the other hand, the maximum switching frequency is limited by the application of the planar transformer. Since the stray capacitance of the planar transformer is usually high, the high switching frequency will cause distortion of the operation waveforms of the DAB converter (Pahlevaninezhad *et al.*, 2014).

3.4.1 Analytical Discussion

From the observation of the power loss breakdown in Figure 3.5, the switching loss of the MOSFET switches dominate the power loss model with low power. Since the RMS value of the current going through switches (3.8) and (3.9) and transformer (3.17) is low on light load conditions, the power loss related with RMS current can be neglect. At the same time, the core loss of the transformer doesn't change with power rating as (3.15). Then how to reduce the power loss at light load conditions is changed to how to minimize the switching loss of the switches during operation.

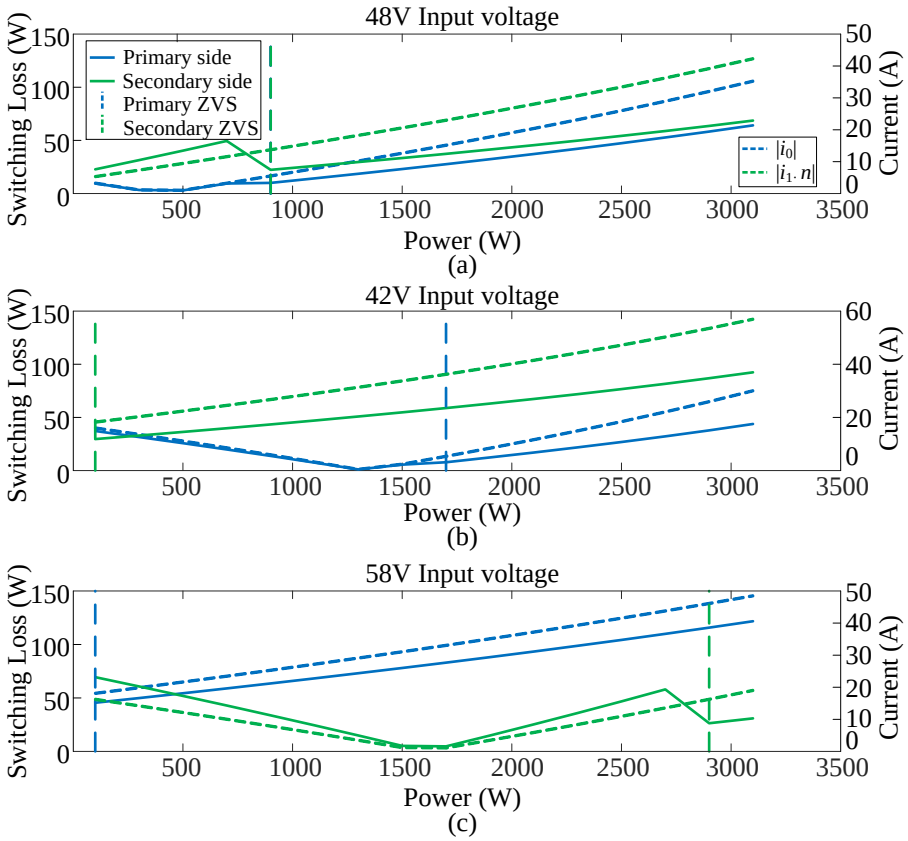


Figure 3.6: Switching loss and the instantaneous current analysis with different input voltage level: (a) 48V input voltage. (b) 42V input voltage. (c) 58V input voltage.

To better understand the problem, the switching loss and its corresponding instantons current is illustrated as Figure 3.6. From the observation, the switching loss of the switches on the secondary side dominate the variation of the power loss with 58V input voltage and the switching loss of the switches on the primary side dominate the variation of the power loss with 42V input voltage. Since the on-resistance of the switches is usually low, the rising time and falling time calculated from (3.14) are assumed to be constant with different power rating. Thus, the switching loss model from (3.12) and (3.13) are only related with the instantaneous current when switches turning on and off. Since ZVS is lost for light load conditions, the power loss model is as (3.20).

$$P_{\text{sw\_loss}} = P_{\text{sw\_Pri,switching}} + P_{\text{sw\_Sec,switching}} = (E_{\text{onM\_pri}} + E_{\text{offM\_pri}} + E_{\text{onM\_Sec}} + E_{\text{offM\_Sec}}) \cdot f \tag{3.20}$$

Based on the analysis of the instantaneous current, the turn-on and turn-off energy can be (3.21) and (3.22).

$$E_{\text{onM\_Pri}} = \begin{cases} V_{\text{in}} \cdot |i_{\text{DS,on\_Pri}}| \cdot \dfrac{t_{\text{on\_Pri}}}{2} = V_{\text{in}} \cdot |i_0| \cdot \dfrac{t_{\text{on\_Pri}}}{2} & \text{non - ZVS} \\ 0 & \text{ZVS} \end{cases} \tag{3.21}$$

$$E_{\text{offM\_Pri}} = V_{\text{in}} \cdot |i_{\text{DS,off\_pri}}| \cdot \frac{t_{\text{off\_Pri}}}{2} = V_{\text{in}} \cdot |i_0| \cdot \frac{t_{\text{off\_Pri}}}{2}$$

$$E_{\text{onM\_Sec}} = \begin{cases} V_{\text{o}} \cdot |i_{\text{DS,on\_Sec}}| \cdot \dfrac{t_{\text{on\_Sec}}}{2} = V_{\text{o}} \cdot \left|\dfrac{i_1}{n}\right| \cdot \dfrac{t_{\text{on\_Sec}}}{2} & \text{non - ZVS} \\ 0 & \text{ZVS} \end{cases} \tag{3.22}$$

$$E_{\text{offM\_Sec}} = V_{\text{o}} \cdot |i_{\text{DS,off\_Sec}}| \cdot \frac{t_{\text{off\_Sec}}}{2} = V_{\text{o}} \cdot \left|\frac{i_1}{n}\right| \cdot \frac{t_{\text{off\_Sec}}}{2}$$

The operation point O in Area 2 can be analyzed as an example in Figure 3.8.

The Area 1 (N-E'-A') and the Area 2 (N-E-A) are interested to improve the efficiency. During CV charging phase, the input voltage is 58V. As the power decreasing from half power, the operation point moves left from A' to E' along the dash line $d = 0.86$. Based on the K value is 60, the transmission power is quarter of the full power at operation point O. From the Figure 3.4, the efficiency is around 86% because the ZVS is lost for primary side. During the Area 2, the ZVS of switches on the secondary side is lost. In Area 2 of Figure 3.7, $i_0 < 0$ and $i_1 < 0$ while $i_0 > 0$ and $i_1 > 0$ in Area 1. Substituting the expression of the current i_0 and i_1 from (3.1), the switching loss of (3.20) can be expressed as (3.23).

$$\begin{aligned} P_{\text{sw\_loss\_Area2}} &= -(V_{\text{in}} \cdot i_0 \cdot \frac{t_{\text{off\_Pri}}}{2} + V_{\text{o}} \cdot \frac{i_1}{n} \cdot \frac{t_{\text{on\_Sec}} + t_{\text{off\_Sec}}}{2}) \cdot f \\ &= \frac{(1-d)V_o^2}{18n^2L}[t_{\text{off\_Pri}} + (t_{\text{on\_Sec}} + t_{\text{off\_Sec}})d] + \frac{dV_o^2}{12\pi n^2 L}[t_{\text{off\_Pri}} - (t_{\text{on\_Sec}} + t_{\text{off\_Sec}})] \cdot \phi \end{aligned} \tag{3.23}$$

Ideally, the turn-off and turn-on time of the switches on the primary side and the secondary side should be designed to be similar from equation (3.14). And usually the turn-off time of the switch is much lower than the turn-on time of the MOSFET switch. Thus the second term of (3.23) is negative. Thus, to minimize the switching loss with certain d value in Area 2, the phase shift ϕ should be chosen as the maximum possible value. So the operation point with 58V input voltage should be at point A' to achieve high efficiency. The efficiency improvement performance depends on the relationship of the turn-on and turn-off time of the switches on the primary side and secondary side. Based on the $K = V_{\text{o}}^2/(n^2LfP)$, the operation point O' ($K = 60$) can be moved to A' ($K = 30$) by increasing the switching frequency from 100kHz to 200kHz with the same quarter of the transmission power. In the switching power equations of the DAB converter, the switching frequency cancels itself with it in the

instantaneous current equations. That's why the efficiency at light load conditions has just relationship with the operation point in the design diagram.

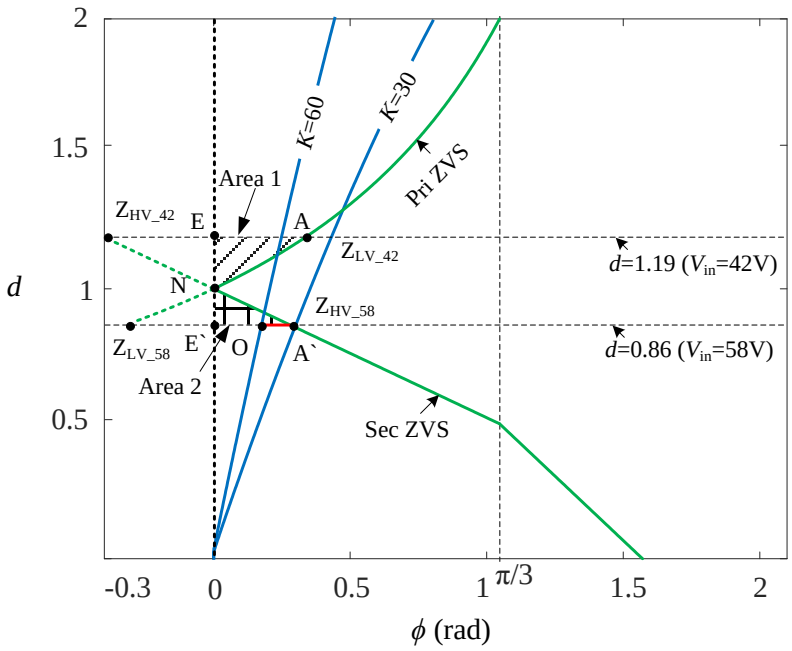


Figure 3.7: Variable switching frequency method analytical analysis.

Similar analysis can be done for the operation point with 42V input voltage, the switching loss can be expressed as (3.24).

$$\begin{aligned} P_{\text{sw\_loss\_Area1}} &= (V_{\text{in}} \cdot i_0 \cdot \frac{t_{\text{on\_Pri}} + t_{\text{off\_Pri}}}{2} + V_{\text{o}} \cdot \frac{i_1}{n} \cdot \frac{t_{\text{off\_Sec}}}{2}) \cdot f \\ &= \frac{(d-1)V_o^2}{18n^2L}[(t_{\text{on\_Pri}} + t_{\text{off\_Pri}}) + t_{\text{off\_Sec}}d] + \frac{dV_o^2}{12\pi n^2 L}[t_{\text{off\_Sec}} - (t_{\text{on\_Pri}} + t_{\text{off\_Pri}})] \cdot \phi \end{aligned} \tag{3.24}$$

Thus the operation point should be at point A in Figure 3.7 to achieve higher efficiency during the light load conditions at 42V input voltage.

3.4.2 Operation Strategy

To improve the efficiency at the light load conditions in Area 2, the variable switching frequency method is summary as following:

1. the equivalent conversion ratio d' can be calculated by $d' = V_{\mathrm{o}}/n/V'_{\mathrm{in}}$ with a input voltage V'_{in};

2. the corresponding phase shift value can be calculated by (3.4) which is $\phi' = 2\pi/3(1-d')$;

3. the K value going through the operation point can be calculated by (3.3) which is $K' = 12\pi 2d'/\phi/(4\pi - 3\phi)$;

4. the switching frequency $f' = V_{\mathrm{o}}^2/(n^2 LK'P')$ can be calculated with a transmission power P'.

The variable switching frequency method can also be analyzed following same analysis in Area 1. The K value 35.05 and 30 are calculated with the input voltage 42V and 58V following the steps as Figure 3.8.

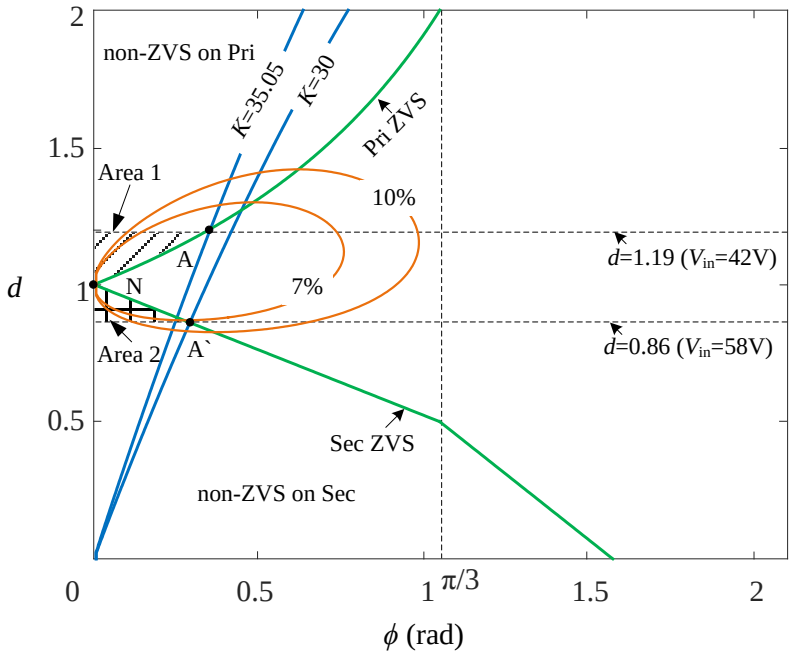


Figure 3.8: Variable switching frequency strategy operation principle.

The maximum switching frequency depends on the planar transformer application. 200kHz is chosen as the maximum switching frequency for our design. The power loss breakdown and applied switching frequency are shown as Figure 3.9. The power loss, especially the switching loss, is reduced by increasing the switching frequency. At the same time the core loss is reduced with increasing switching frequency from (3.15).

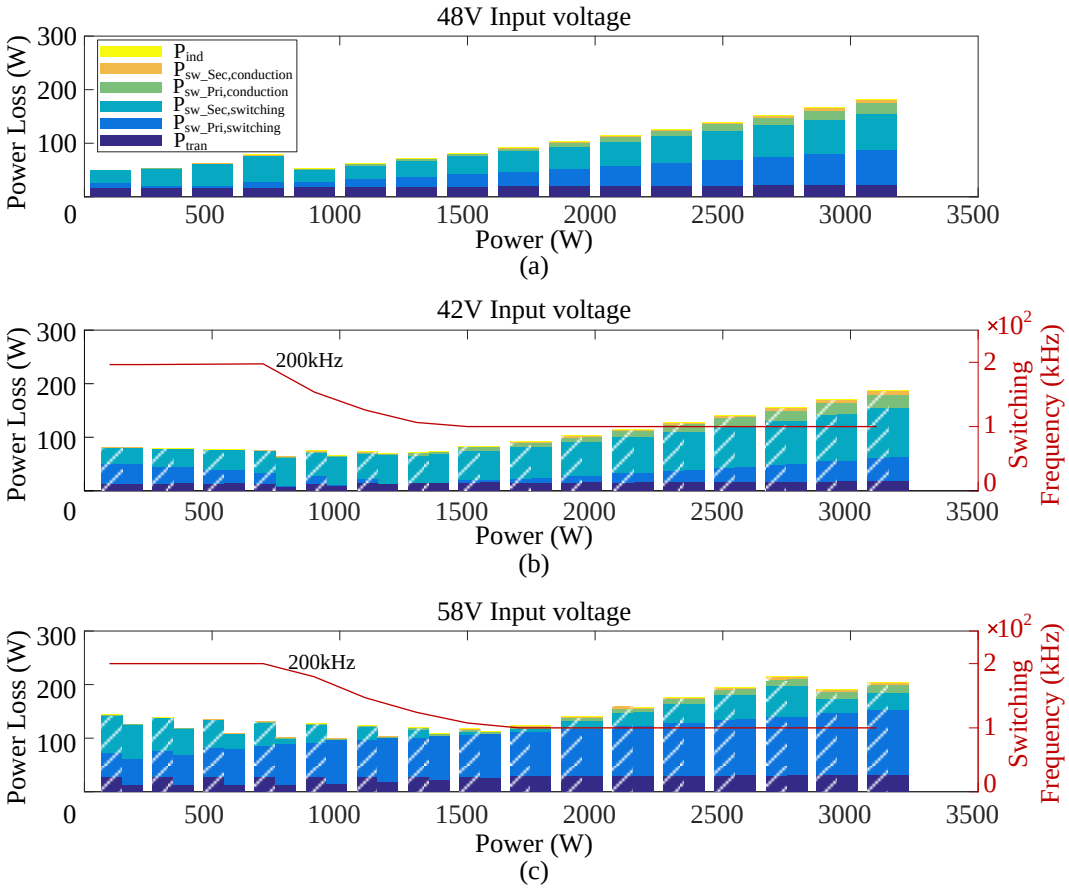


Figure 3.9: Power loss breakdown of the variable switching frequency strategy with different input voltage level. Shadowed area represents the power loss breakdown of the 100kHz original operation.

3.5 Experimental Results

To verify the design of the three-phase converter and variable switching frequency strategy, the experiment setup is built as Figure 3.10. Three planar transformers are built with E64 core. The component list is shown as Table 3.2. The input voltage range is from 42 58V and the output voltage is 400V. The switching frequency is 100kHz. The controller is TI TMS28377D.

The experimental waveforms of the three-phase DAB converter are shown with 3kW power rating as Figure 3.11. The converter efficiency is obtained by measuring the input and output power of the primary and secondary sides of the converter. YOKOGAWA WT 1800 high performance power analyzer and LEM ULTRASTAB 867-200I precision current transducer are used. The efficiency is shown as Figure 3.12 where blue lines and red lines represent conventional and proposed efficiency curves from theoretical analysis; blue circles and red crosses represent conventional and proposed m efficiency measurement from experiment.

Table 3.2: Component list of the three-phase DAB converter experiment setup.

Component	Description
MOSFETs on the primary side S1∼S6	IPP045N10N3
MOSFETs on the secondary side Q1∼Q6	C3M0065090D
Transformer	N87 Epcos EE 64 core. N1=1, N2=8; 5oz PCB
Add-on leakage inductor	33uH VER2923-333KL
Input capacitor Cin	80uF
Output capacitor Co	10uF

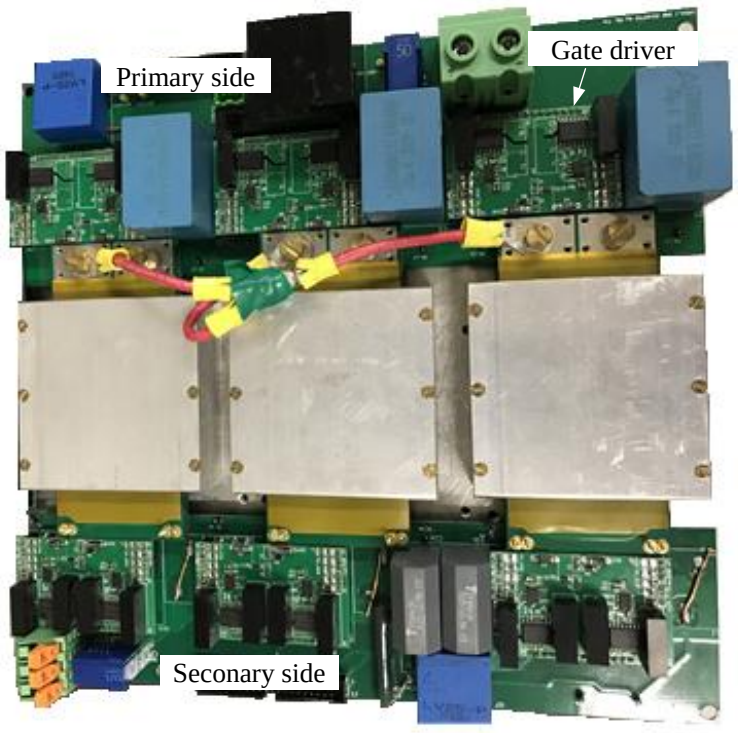


Figure 3.10: Experiment setup of the three-phase DAB converter.

From Figure 3.12, the measured efficiency matches with the theoretical efficiency model. Variable switching frequency method is applied with low power experiment for 42V and 58V input voltage. The measured efficiency as the red crosses in Figure 3.12 matches the theoretical analysis in Section 3.4. The method can be applied with whole input voltage range at light load conditions. The variable switching frequency method has better performance with 58V input voltage than 42V. It can be explained by the relationship between the turn-on and turn-off time of the switches on the primary and secondary sides from (3.22) and (3.23). The variable switching frequency can help to improve the efficiency, maximum 4%, during the CV charging phase with 58V input voltage.

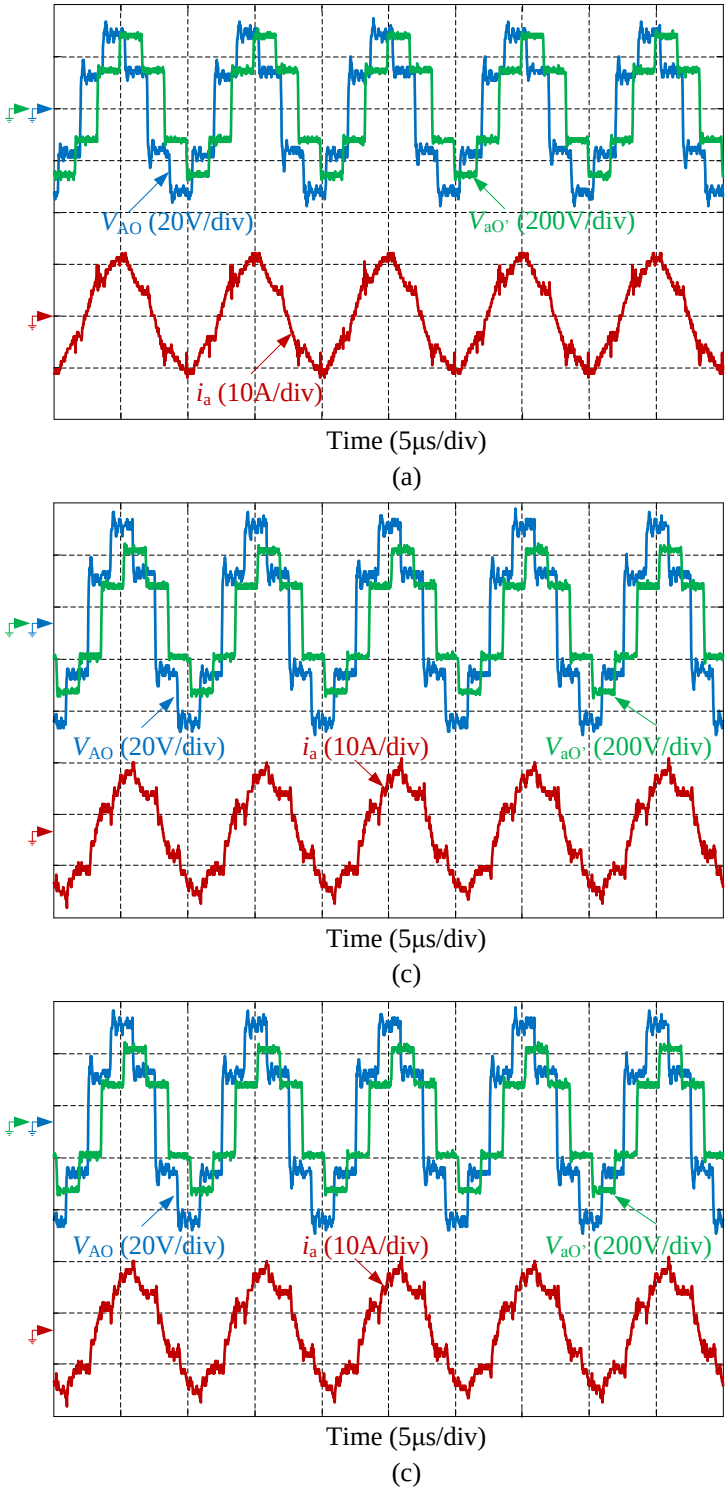


Figure 3.11: 3kW Experiment waveform: (a) 48V to 400V; (b) 42V to 400V; (c) 58V to 400V.

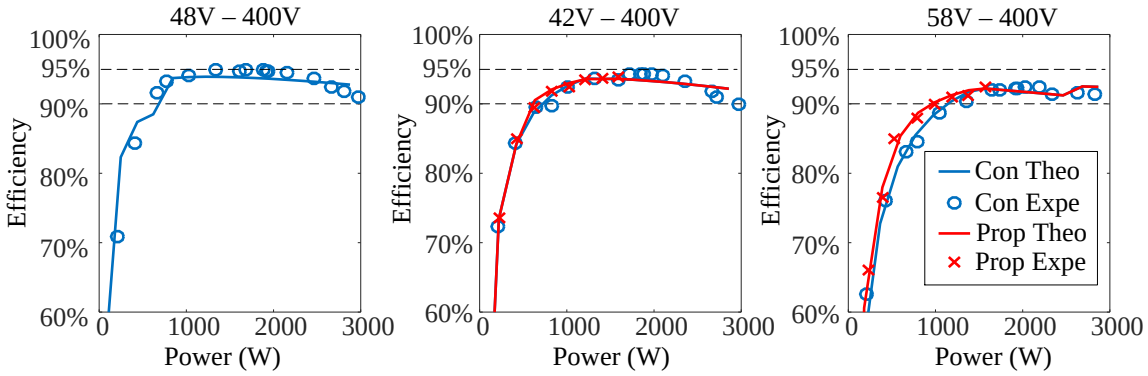


Figure 3.12: Theoretical and experimental efficiency comparison between constant switching frequency operation and variable switching frequency operation.

3.6 Conclusion

The design strategy of the three-phase DAB converter is proposed to achieve high efficiency in wide operation voltage range and load conditions. The design strategy is verified by the efficiency map and the power loss model is analyzed. Then a variable switching frequency method is proposed to improve the efficiency at the light load conditions by minimizing the switching frequency. It's very easy to be applied by following one equation. A 3kW experimental setup is built and its results are used to verify the design strategy and the variable switching frequency method.

Chapter 4

Dead-Time Effect of the Three-Phase Dual-Active-Bridge DC/DC Converter

4.1 Introduction

The dead-time effect is observed in the three-phase dual active bridge (DAB) DC/DC converter. The occurrence of the dead-time effect depends on the relationship of the switching frequency, the phase shift value, the dead-time value and the equivalent conversion ratio. The dead-time effect may have significant impact on the converter performance when high switching frequency, wide input and output voltage range or wide operation power range are required. Therefore, comprehensive research of the dead-time effect is essential to improve the design of the three-phase DAB converter over a wide operation range. In this chapter, all the cases of the dead-time effect in the three-phase DAB converter are analyzed in terms of the buck, boost, and matching

states. The expressions of the transmission power, constraint conditions, and key time of the dead-time effect are derived for each state. The operation waveforms of the dead-time effect are also presented to better understand the dead-time effect. Finally, the analysis is verified by both simulation and experimental results.

This chapter aims to improve the design of the dead-time of the three-phase DAB at different operating conditions by comprehensively analyzing the dead-time effect in terms of the conversion ratio and phase shift value. The organization of this chapter is as follows: Section 4.2 describes the dead-time effect in the three-phase DAB topology. Section 4.3 presents the detailed analysis of the dead-time effect in different operation mode especially the operation waveforms and expression equations. In Section 4.4, experimental results are presented to validate the simulation results. To better reveal all the cases of the dead-time effect, different specifications are utilized than the other of the thesis. Finally, Section 4.5 concludes the findings and summarizes contributions of this chapter.

4.2 Dead-Time Effect Phenomena in Three-Phase DAB Converter

4.2.1 Conventional Operation of the Three-Phase DAB DC/DC Converter

A typical three-phase DAB DC/DC converter is illustrated in Figure 3.1. With the single-phase-shift (SPS) control method, the operation principle of the three-phase DAB converter is similar to that of the single phase converter. Each phase conducts

120^o in turn while the phase shift is controlled between two sides of the converter to produce voltage difference across the leakage inductance of the transformers. The basic idea is to utilize the voltage difference across the inductor to induce the current flow and, thus, the power can be delivered from one side to the other side. Three individual transformers with the same parameters which are connected in Y type are more promising, as shown in Figure 3.1, because it adds more flexibility to the converter. For example, the performance evaluation for three-phase DAB converter with different transformer configuration is proposed in (Baars *et al.*, 2016).

The biggest advantage of the DAB topology is that all the switches can operate in turn-on ZVS which makes it high efficient. However, in order to achieve soft-switching, sufficient dead-time should be given so that the switch voltage drop to zero before the switch is turned on (Van Hoek, 2017). The traditional operation waveforms of the three-phase DAB converter with SPS control with $\phi \in [0, \pi/3]$ can be found in Figure 4.1(a), where v_{HA} and v_{ha} represent the voltage across the switch S_1 and Q_1 respectively, v_{AO} and $v_{\mathrm{aO'}}$ represent the phase voltage of the transformer A and i_{A} represent the current going through transformer A. In this chapter, I define the current going through the MOSFET switch from source to drain as negative and otherwise as positive. The upper graph in Figure 4.1(a) shows the voltage across the switch. The lower graph in Figure 4.1(a) shows the voltage of the phase A and the current of the phase A transformer. When the current going through the switch is negative during the dead-time interval, the body diode of the switch is conducting then the voltage across the switch will drop to zero before the switch is turned on. Thus, the turn on ZVS can be achieved. A lower limit of the dead-time has to be designed to ensure ZVS. If the dead-time is a relatively large value, the dead-time

effect will happen.

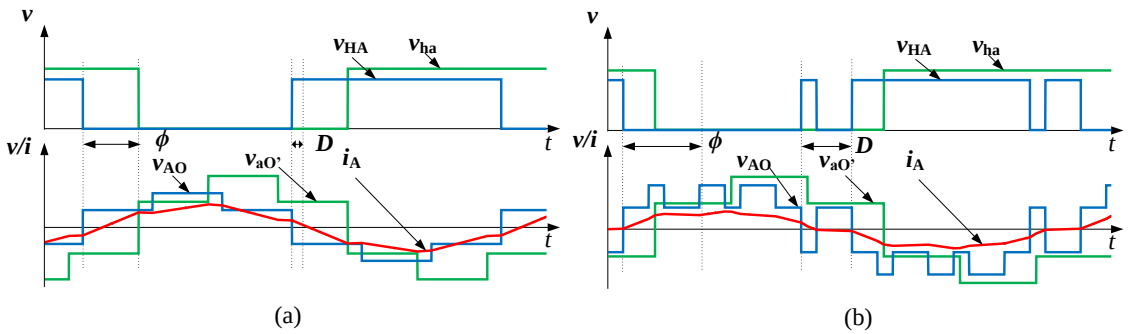


Figure 4.1: Operation waveforms of three-phase DAB converter: (a) Conventional, (b) Dead-time effect (simulation condition: dead-time in rad is 0.70; phase shift in rad is 0.48.)

4.2.2 Dead-time Effect Phenomena in Three-Phase DAB Converter

In (Zhao *et al.*, 2014b), the voltage polarity reversal, voltage sage and phase shift are found in single-phase DAB converter. They all exist in three-phase DAB converter.

The voltage polarity reversal as a typical dead-time effect of the three-phase DAB converter is still observed as Figure 4.1(b). In the upper waveforms of the Figure 4.1(b), a voltage pulse during the switch turning on and voltage sag during the switch turning off can be observed. This phenomenon is so-called voltage polarity reversal which can be also seen in the single phase DAB converter (Zhao *et al.*, 2014b). When the current going through the switch is positive during the dead-time interval, the body diode of the other switch of the same leg will be conducting and the voltage across the switch will be the DC-bus voltage. Thus the so-called voltage polarity reversal happens. When the current going through the switch is zero during the dead-time, the voltage sag will happen where the voltage value should be depended

on the voltage of other legs. The dead-time effect of the single phase DAB converter is straight forward it's a full bridge topology. However the analysis of the three-phase DAB will be more complicated because its three half-bridge topology will cause the voltage difference across the inductor depending on all the voltage shape of the three legs.

The transmission power of the conventional case ($\phi \in [0, \pi/3]$) and dead-time effect case are illustrated as Figure 4.2 and can be calculated as (4.1).

$$P = \frac{dV_i^2\phi}{\omega L}(\frac{2}{3} - \frac{\phi}{2\pi}) \tag{4.1}$$

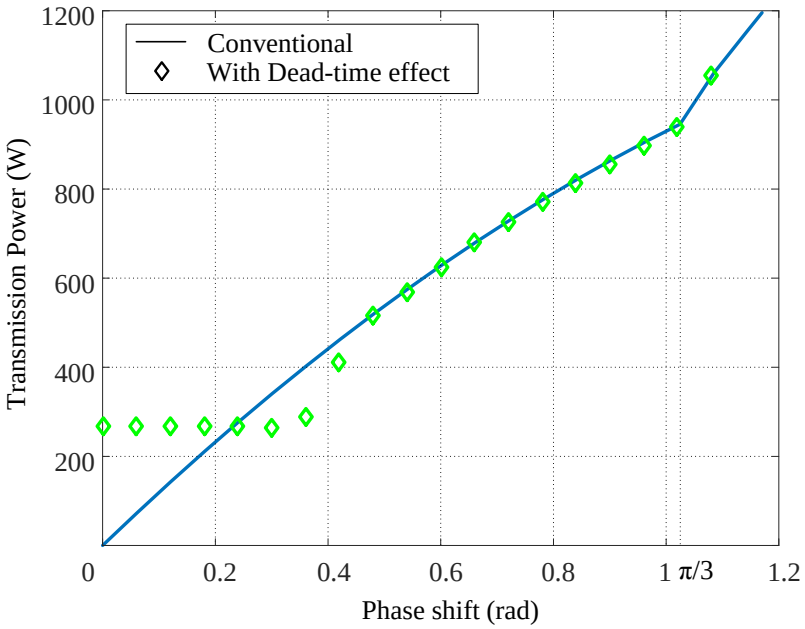


Figure 4.2: Transmission power comparison (Blue solid line: conventional simulated curve with relatively small dead-time; green dots: simulation result with dead-time 0.35 in rad).

The main purpose in this chapter is to propose the comprehensive expression of

the dead-time effect in three-phase DAB converter. Thus the applied parameters and specifications in this chapter are not necessary to be the same as the rest of this thesis. For experiment setup convenience, the input and output voltage of interest are 34V and 180V, respectively. The turn ratio of the applied transformers is 1:6. The different trend of the power curve before and after $\pi/3$ is caused by the different operation modes of the three-phase DAB converter ($\phi \in [0, \pi/3]$ and $\phi \in [\pi/3, 2\pi/3]$) (De Doncker *et al.*, 1991). The green dot curve represents the simulation power results with dead-time as 0.35 in rad. Based on the observation of Figure 4.2, the transmission power is the same as conventional case for larger phase shift value. However, at lower phase shift value, the transmission power is quite nonlinear with the phase shift value. This is because of the voltage distortion due to voltage sag and voltage reversal. At first, the transmission power is lower than conventional operation. Then the power at lower phase shift value is kind of "saturated" where lower transmission power will not be achieved. This may cause malfunction of the converter. Thus, the dead-time effect should draw enough attention when designing the converter with wide operation range. And the comprehensive analysis of the dead-time effect is needed.

4.3 Dead-time Effect Analysis Details of The Three-Phase DAB Converter

The comprehensive analysis of the dead-time effect will be shown in this section. Since the phase voltage of the transformer is highly depended on the equivalent conversion ratio d, all of the dead-time effect can be categorized into three operational states: boost ($d > 1$), buck ($d < 1$) and matching ($d = 1$). The detailed analysis of the operation waveforms can be found. The constrain equations, the transmission power and key characterizing timing can also be found. Due to the symmetry of the three-phase DAB topology, only 60^o of the waveform in Phase A is analysed as an example and the other analysis can refer to it. The range of the interested dead-time is $0-\pi/3$ because larger dead-time results in too small conduction time. The phase shift value range is $0-2\pi/3$ in this thesis because larger phase shift produces too much back-flow power (De Doncker *et al.*, 1991).

4.3.1 Boost State ($d > 1$)

Mode A1

When $0 \leq \phi < D$ and $0 \leq \phi < t_{i0}$, the operation waveforms are illustrated in Figure 4.3(a) where t_{i0} represent the time when the current going through the transformer, i_{A}, equals to zero in the half period.

At t_0, the switch S_1 is turned ON. The equivalent circuit is as shown in Figure 4.5(a). During the interval between t_0 and t_1, Q_1 and Q_4 are turned OFF due to the dead-time. Besides there is no current going through T_{A}, their body diode is not conducting. On the other hand, S_1, S_3 and S_5 are turned ON so the voltage v_{AO} can

be easily derived as $V_i/3$ using the basic circuit theory.

Based on the basic circuit theory, the expression equations describing the relationship between the voltages are summarized as (4.2).

$$\begin{cases} v_{\mathrm{aO'}} = nV_{\mathrm{i}}/3 \\ v_{\mathrm{aO'}} + v_{\mathrm{ah}} = v_{\mathrm{cO'}} \\ v_{\mathrm{cO'}} - v_{\mathrm{bO'}} = V_{\mathrm{o}} \\ v_{\mathrm{aO'}} + v_{\mathrm{bO'}} + v_{\mathrm{cO'}} = 0 \end{cases} \tag{4.2}$$

The voltage can be derived as (4.3) by solving the equations (4.2).

$$\begin{cases} v_{\mathrm{aO'}} = nV_{\mathrm{i}}/3 \\ v_{\mathrm{bO'}} = (3V_{\mathrm{o}} - nV_{\mathrm{i}})/6 \\ v_{\mathrm{cO'}} = (3V_{\mathrm{o}} + nV_{\mathrm{i}})/6 \\ v_{\mathrm{ha}} = (V_{\mathrm{o}} - nV_{\mathrm{i}})/2 \end{cases} \tag{4.3}$$

From t_1 to t_2, Q_1 begins to conduct. On the primary side, although S_3 is turned OFF, its body diode is still conducting because i_C is negative as shown in Figure 4.5(b). Based on the operation of the converter, the voltage v_{AO} and $v_{\mathrm{aO'}}$ can be derived as $V_{\mathrm{i}}/3$ and $V_{\mathrm{o}}/3$. Thus, the voltage across L_{A} is $(nV_{\mathrm{i}} - V_{\mathrm{o}})/3n$. The voltage is negative because of the boost state ($d > 1$). This voltage will cause i_{A} to increase linearly in the negative direction.

During the interval between t_2 and t_3, the primary side of the converter remains the same. At t_2, Q_3 is turned OFF. Due to the leakage inductance in the transformer, the current i_C cannot change instantaneously at that moment. Thus the negative direction of i_C forces the body diode of Q_6 to conduct as shown in Figure 4.5(c).

The voltage across L_{C} is $(nV_{\mathrm{i}} + V_{\mathrm{o}})/3n$ resulting in the current going through it to decrease in the negative direction. i_C ends up to zero at t_3.

Since i_C is zero at t_3, the body diodes of S_3 and Q_6 are not conducted anymore as shown in Figure 4.5(d). Since there is no current in the leakage inductor, v_{CO} and $v_{\mathrm{cO'}}$ are zero. The voltage v_{HC} and v_{hc} equal to $V_{\mathrm{i}}/2$ and $V_{\mathrm{o}}/2$, respectively. Based on KVL, v_{AO} and $v_{\mathrm{aO'}}$ are $V_{\mathrm{i}}/2$ and $V_{\mathrm{o}}/2$, respectively. The rest of the waveform can be analysed based on the similar analyse procedure for the phase B and phase C. For example, the interval $t_4 - t_5$ in Phase A can be analyzed following the same steps analyzing interval $t_0 - t_1$ for Phase C. Then the voltage is derived as $v_{\mathrm{aO'}} = (nV_{\mathrm{i}} + 3V_{\mathrm{o}})/6$ according to (4.3).

After observing the operation waveform, ZCS can be achieved for the primary side switches during turning on and off while ZVS can be achieved for the secondary side switches during turning on. This mode can be utilized to increase efficiency when ZVS is lost in light load condition of the regular modulation. Although the transmission power here is negative, we can see this mode as a Buck state with positive transmission power.

Table A.1 and Table A.2 summarizes the constraint conditions and the corresponding transmission power expressions. Considering the length of the chapter, the derivations are not showed here. The time of the zero current in Figure 4.3(a) is derived in (4.4).

$$t_{i0} = \frac{2(2\pi + 3Dd - 2\pi d)}{3(d+1)} \tag{4.4}$$

Mode A2

If $0 \leq \phi < D$ and $0 \leq t_{i0} < \phi$, the operation waveforms are illustrated in Figure 4.3(b).

Since $0 \leq t_{i0} < \phi$, the Mode A2 does not have the zero v_{AO} situation. At t_0, S_1 is turned ON. During the time interval t_0 to t_1, the current i_{A} is positive as shown in Figure 4.5(e). Although Q_1 is turned OFF, the body diode is conducting because of the positive current i_{a}. Based on the operation condition, the voltage across L_{A} is $(nV_{\mathrm{i}} - V_{\mathrm{o}})/3n$ which is negative due to $d > 1$. Hence, the current i_{a} decreases linearly in the positive direction then it end up to zero at t_1. The analysis of the interval $t_1 - t_4$ in Mode A2 is the same as the interval $t_0 - t_3$ in Mode A1. The equivalent circuits are as shown in Figure 4.5(a), Figure 4.5(b) and Figure 4.5(c) sequentially.

After analysing the operation waveform, ZVS can be achieved in the secondary side when turning on but the soft-switching is lost in the primary side. The time of the zero current is derived in (4.5).

$$t_{i0} = -\frac{6\phi - 4\pi - 6Dd + 4\pi d}{3(d-1)} \tag{4.5}$$

Mode A3

If $0 \leq \phi < D$ and $t_{i0} = 0$, the operation waveforms are shown in Figure 4.3(c). Since $\phi < D$, the effective value of the phase shift is negative in Mode A1-3. That is why phase shift drift happens.

During the time interval t_0 to t_1, the analysis is almost the same as the interval $t_0 - t_1$ in Mode A2 except that the current i_{A} ends up to a positive value instead of 0. Another difference is that when Q_1 is turned ON during the interval t_0 to t_1, the

current will go through the MOSFET other than its body diode.

At t_1, Q_3 is turned OFF as shown in Figure 4.5(f). However, the current i_C forces the body diode of Q_6 to conduct. The voltage across L_A will be $(nV_i - 2V_o)/3n$ which cause i_A to decrease to negative value at t_2.

Mode A4

As shown in the Figure 4.3(d), the Mode A4 conditions are $\phi > D$, $i(S_{1off}) < 0$ and $i(S_{4on}) < 0$.

At t_0, S_1 is turned ON. Therefore, S_1, S_3 and S_5 are conducting on the primary side and Q_3, Q_4 and Q_5 are turned ON as shown in Figure 4.5(k). The voltage across L_A is $(nV_i + V_o)/3n$ which will induce i_A to increase.

At t_1, Q_4 is turned OFF. i_C will keep the positive direction thus the body diode of Q_1 is conducting. The equivalent circuit for the interval $t_1 - t_2$ is shown in Figure 4.5(j). Just before t_1, the switch S_3 is turned OFF while its body diode will be conducting.

Mode A5

The constraint conditions are $\phi > D$, $i(S_{1off}) > 0$ and $i(S_{4on}) < 0$. But this mode can be further divided into three different cases as shown in the Figure 4.3(e), Figure 4.3(f) and Figure 4.3(g) where t_{iN} represents the time interval when negative current conducting from the time S_1 turned OFF to the time S_4 turned OFF.

Case a: When $\phi \geq \pi/3$ and $t_{iN} \leq D - \phi + \pi/3$, the operation waveforms are shown in Figure 4.3(e). At t_0, S_1 is turned ON. S_1, S_3 and S_5 are conducting on the primary side as shown in Figure 4.5(m). On the secondary side, Q_3 and Q_4 are turned

ON and the body diode of Q_5 is conducting. The voltage across L_A is $(nV_i + V_o)/3n$ which will cause i_A to increase in the positive direction.

For the time interval between t_1 and t_2, two actions happening. First, S_3 is turned OFF when the body diode of S_6 is conducting resulted from the direction of the current i_C as shown in Figure 4.5(h). Then, since Q_5 is turned ON, the MOSFET is conducting instead of its body diode. The voltage across L_A is $(2V_i + V_o)/3n$ which will cause i_A to increase in the positive direction.

For the interval t_2 to t_3, the equivalent circuit is shown in Figure 4.5(i). The body diode of Q_1 is conducting after Q_4 is turned OFF at the time t_2 due to the positive direction of i_a.

At t_3, the polarity of the current i_C changes from positive to negative. Hence, the body diode of S_3 is conducting as shown in Figure 4.5(j).

The time of the negative current in the waveform in Figure 4.3(e) is derived as (4.6).

$$t_{iN} = \frac{3D - 2\pi + 3Dd + 2\pi d - 3d\phi}{3d} \tag{4.6}$$

Case b: When $\phi \geq \pi/3$ and $t_{iN} > D - \phi + \pi/3$, the operation waveforms are shown in Figure 4.3(f).

During the interval t_0 to t_1, this interval can be analyzed with the same procedure like interval $t_0 - t_1$ in Case 1 of Mode A5. The equivalent circuit is illustrated in Figure 4.5(m).

At t_1, S_3 is turned OFF as shown in Figure 4.5(n). But the body diode of S_6 is forced to conduct due to the positive i_C. The voltage across L_A is $(2V_i + V_o)/3n$ which will cause i_A to increase in the positive direction.

At t_2, the polarity of the current i_C changes from negative to positive. Although

S_3 is not turned ON, its body diode is conducting as shown in Figure 4.5(o).

At t_3, Q_4 is turned OFF while the body diode of Q_1 is conducting due to the positive i_a as shown in Figure 4.5(j).

The time of the negative current in the waveform as shown in Figure 4.3(f) is derived in (4.7).

$$t_{i\mathrm{N}} = \frac{3D - 2\pi + 6Dd + 3\pi d - 6d\phi}{6d} \tag{4.7}$$

Case c: When $0 \leq \phi < \pi/3$, the operation waveforms are shown in Figure 4.3(g).

At t_0, S_1 is turned ON. S_1, S_3 and S_5 are conducting on the primary side as shown in Figure 4.5(g). On the secondary side, Q_3, Q_4 and Q_5 are turned ON. The voltage across L_A is $(nV_i + V_o)/3n$ which will cause i_A to increase in the positive direction.

At t_1, Q_4 is turned OFF while the body diode of Q_1 is conducting due to the positive i_a as shown in Figure 4.5(p).

From the time interval t_2 to t_3, the equivalent circuit is shown in Figure 4.5(i). At t_2, S_3 is turned OFF then the body diode of S_6 is conducting as shown in Figure 4.5(i).

At t_3, the direction of the current i_C changes so the body diode of S_3 conducts. Then, Q_1 is turned ON as shown in Figure 4.5(q).

The time of the negative current in the waveform as shown as Figure 4.3(g) is derived as (4.8).

$$t_{i\mathrm{N}} = \frac{3D - 2\pi + 3Dd + 2\pi d - 3d\phi}{3d} \tag{4.8}$$

To summarize the soft-switching condition in Mode A5, ZVS can be achieved in the secondary side when turning on but the soft-switching is lost in the primary side.

Mode A6

The operational waveforms of Mode A6 are shown in Figure 4.3(h) and Figure 4.3(i).

The constraint conditions of Mode A6 are $\phi > D$, $i(S_{1off}) > 0$ and $i(S_{4on}) > 0$. In this mode, the dead-time does not affect the waveforms and this mode is similar to the normal operation mode of the three-phase DAB converter. This mode can be further divided into 2 cases.

Case a: The constraint conditions of the case is $0 \leq \phi < \pi/3$ and its waveforms are shown in Figure 4.3(h). At t_0, S_4 is turned OFF. Since the current i_A is negative, the body diode of S_1 is conducting. Besides, S_3 and S_5 are conducting on the primary side as shown in Figure 4.5(r). On the other side, Q_3, Q_4 and Q_5 are turned ON. The voltage across L_A is $(nV_i + V_o)/3n$ which will cause i_A to increase in the positive direction. The zero crossing of the current is later than the moment when S_1 is turned ON. Therefore, ZVS is achieved. At t_1, Q_4 is turned OFF. Due to the positive i_a, the body diode of Q_1 is conducting as shown in Figure 4.5(p).

Case b: The constraint condition of this case is $\pi/3 < \phi \leq 2\pi/3$ and its waveforms are shown in Figure 4.3(i). At t_0, S_4 is turned OFF. Since the current i_A is negative, the body diode of S_1 is conducting as shown in Figure 4.5(l). During the interval t_0 to t_1, S_1 is turned ON and ZVS is achieved.

At t_1, Q_2 is turned OFF. Since the current i_b is negative, the body diode of Q_5 is conducting as shown in Figure 4.5(m).

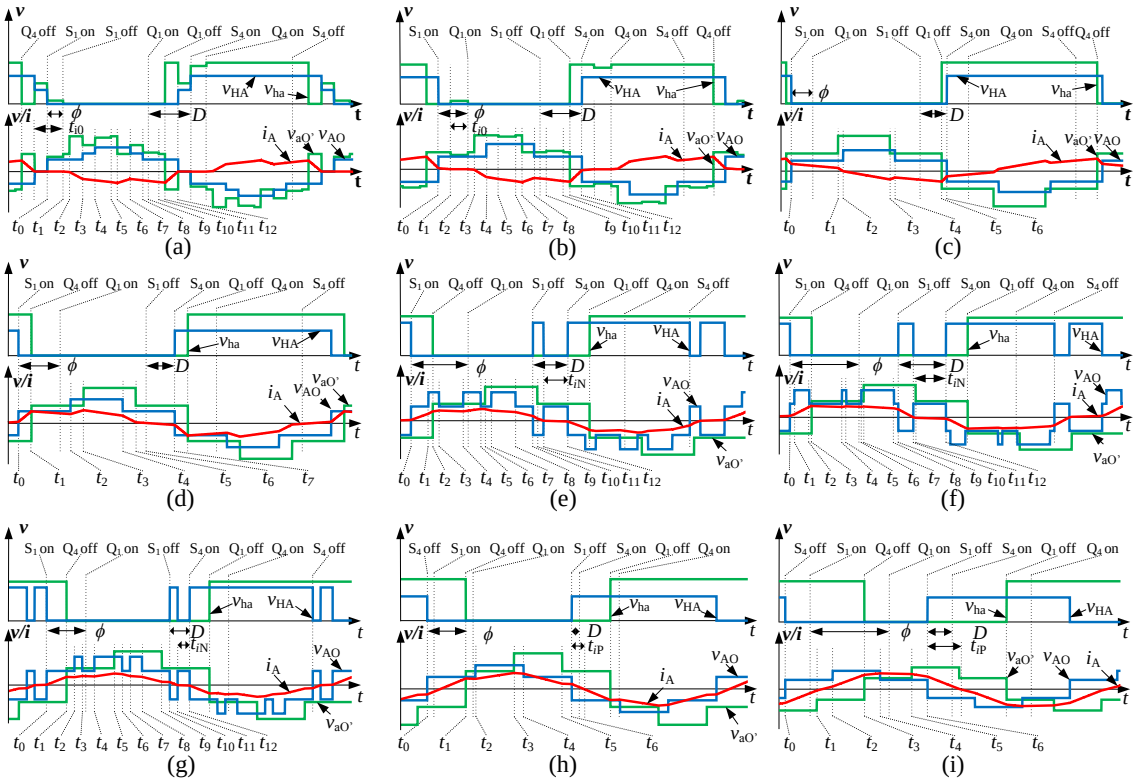


Figure 4.3: Operation waveforms for Boost state.

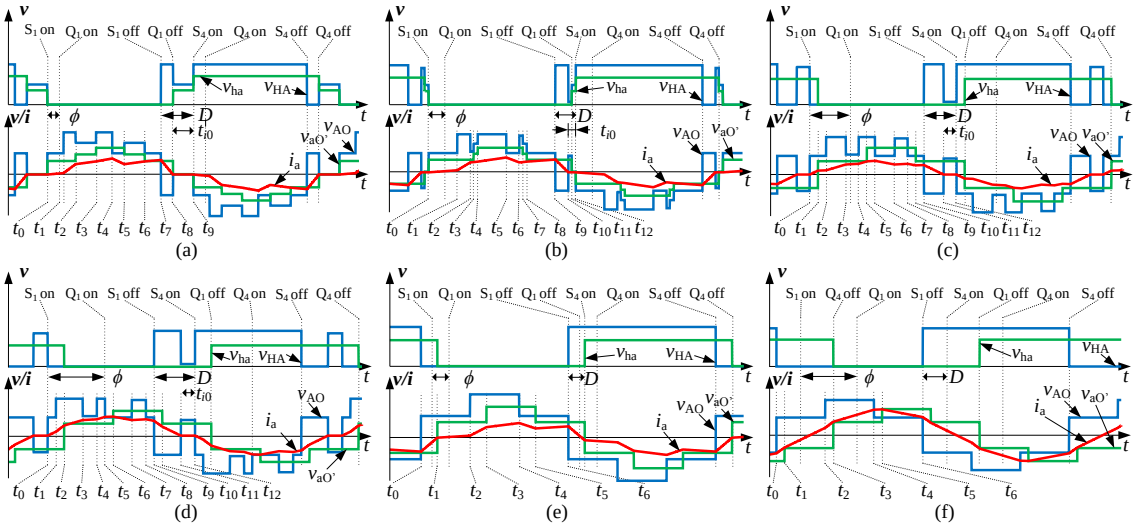


Figure 4.4: Operation waveforms for Buck state.

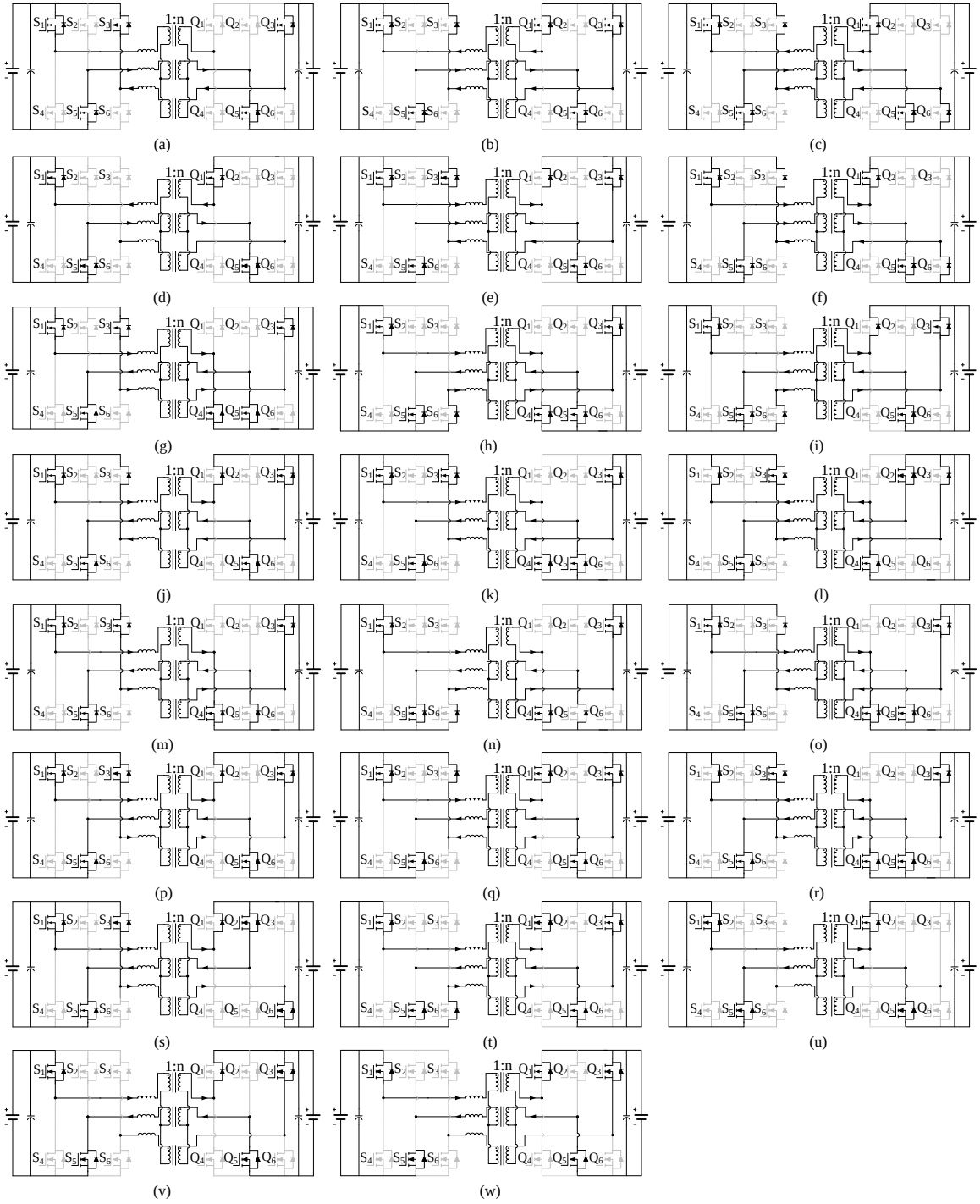


Figure 4.5: Equivalent circuits of the three-phase DAB converter for the dead-time effect analysis.

4.3.2 Buck State ($d < 1$)

Mode B1

When $0 < \phi \leq D$, $t_{i0} > 0$ and $t_{i0} = D - \phi$, the operation waveforms of the Mode B1 is shown in Figure 4.4(a).

At t_0, S_1 is turned ON. Although Q_1 is not turned ON, its body diode is conducting due to the positive i_a as shown in FFigure 4.5(p). The voltage across L_A is $(nV_i - V_o)/3n$. Since $d < 1$ in Buck state, it will cause i_A to increase in the positive direction.

At t_1, S_3 is turned OFF as shown in Figure 4.5(t). However, the body diode of S_6 is conducting depending on the polarity of the current i_C. If we focus on Phase C, the voltage across L_C is $(-nV_i - V_o)/3n$ which will cause i_C to decrease in the positive direction. At t_2, i_C ends up to zero.

For the time interval t_2 to t_3, the equivalent circuit is shown in Figure 4.5(u). The analysis for the time interval $t_2 - t_3$ is very similar to the analysis for the time interval $t_3 - t_4$ as shown in Figure 4.5(d). The difference is that the polarity of i_A and i_B is opposite. The time duration of the zero current is calculated in (4.9).

$$t_{i0} = \frac{2(3D - 2\pi + 2\pi d)}{3(d+1)} \tag{4.9}$$

The constraint conditions and transmission power expression are shown in Table A.3. After analysing the operation waveform, the ZVS can be achieved in the switches of the primary side during turning on at the same time the ZCS can be achieved in the switches of the secondary side during turning on and off. This mode may be utilized to increase the efficiency when the ZVS is lost in the light load condition of the regular modulation.

Mode B2

When $0 < \phi \leq D$, $t_{i0} > 0$ and $t_{i0} > D - \phi$, the waveforms are shown in Figure 4.4(b). The analysis for the time interval $t_0 - t_2$ is the same as the time interval $t_0 - t_2$ in Mode B1.

Although the current i_{C} is zero same as in the previous analysis at t_2, Q_3 is turned ON as shown in Figure 4.5(w). The voltage relationship can be derived based on the analysis for the time interval $t_0 - t_1$ in Mode A1. The voltages are derived as the equations in (4.10).

$$\begin{cases} v_{\mathrm{AO}} = (3V_{\mathrm{i}} - nV_{\mathrm{o}})/6 \\ v_{\mathrm{BO}} = nV_{\mathrm{o}}/3 \\ v_{\mathrm{CO}} = (3V_{\mathrm{i}} + nV_{\mathrm{o}})/6 \\ v_{\mathrm{HA}} = 0 \end{cases} \tag{4.10}$$

At t_3, the current i_{c} is zero and Q_3 is still turned OFF as shown in Figure 4.5(u). The analysis is very similar to the analysis of the time interval $t_3 - t_4$ as shown in Figure 4.5(d). The difference is that the polarity of i_{A} and i_{B} is opposite. The time duration of zero current is derived in (4.11). Same as Mode B1, the ZVS can be achieved in the primary side when turning on while ZCS can be achieved in the secondary side when turning on and off. This mode can be utilized to increase the efficiency when the ZVS is lost in the light load condition of the regular modulation.

$$t_{i0} = \frac{2(3D - 2\pi + 2\pi d)}{3(d+1)} \tag{4.11}$$

Mode B3

When $\phi > D$ and $t_{i0} > 0$, the operation waveforms are shown in Figure 4.4(c) and Figure 4.4(d). But this mode can be divided further into two cases and will be discussed below.

Case a: The constraint condition of this case in Mode B3 is $D \leq \phi < \pi/3$ and its operation waveforms are shown in Figure 4.4(c).

The analysis for the time interval $t_0 - t_3$ can be done referred to the time interval $t_0 - t_3$ in Case 3 of Mode A5. The equivalent circuits are shown in Figure 4.5(g), Figure 4.5(p) and Figure 4.5(i) respectively.

At t_3, i_C is zero according to aforementioned analysis. Q_3 is still open as shown in Figure 4.5(v). This case is very similar to the time interval $t_0 - t_1$ in Mode A1. The voltage equations are found in equation (4.10). The time duration of zero current is calculated in (4.12).

$$t_{i0} = \frac{2(3D - 2\pi + 3Dd + 2\pi d - 3d\phi)}{3(d+1)} \tag{4.12}$$

Case b: The constraint condition of this case in Mode B3 is $\phi \geq \pi/3$ and its operation waveforms are shown in Figure 4.4(d).

The analysis for the time interval $t_0 - t_3$ can be done referred to the time interval $t_0 - t_3$ in Case 1 of Mode A5. The equivalent circuits are Figure 4.5(m), Figure 4.5(h) and Figure 4.5(i) respectively.

The analysis for the time interval $t_3 - t_4$ is similar to the time interval $t_3 - t_4$ in Case 1 of Mode B3. The time duration of zero current is derived as (4.13). To summarize the soft-switching condition, the ZVS can be achieved in both primary

side and secondary side.

$$t_{i0} = \frac{2(3D - 2\pi + 3Dd + 2\pi d - 3d\phi)}{3(d+1)} \tag{4.13}$$

Mode B4

When the time t_{i0} is zero as shown in the Figure 4.4(e) and Figure 4.4(f), it can be observed that this mode is the normal operation mode for three-phase DAB converter in Buck state. It can be divided into 2 cases by $0 \leq \phi < \pi/3$ and $\pi/3 \leq \phi < 2\pi/3$. The analysis of this Mode is the same as Mode A6 for the Boost state.

4.3.3 Matching State ($d = 1$)

Mode C1

When $0 \leq t_{i0} < D$, the operation waveforms are shown in Figure 4.6(a) and Figure 4.6(b). But this mode can be divided further into two cases and will be discussed below.

Case a: When $D \leq \phi < \pi/3$, the waveforms of this case are shown in Figure 4.6(a). The analysis for the time interval $t_0 - t_1$ is the same as the time interval $t_0 - t_1$ in Mode A4 in the Boost state as shown in Figure 4.5(k). The analysis for the time interval $t_1 - t_3$ is similar to the time interval $t_0 - t_2$ in Mode B1 in the Buck state as shown in Figure 4.5(p) and Figure 4.5(t). However, for the interval t_1 to t_2, the voltage across L_{A} is $(nV_{\mathrm{i}} - V_{\mathrm{o}})/3n$, which is zero considering the Matching state ($d = 1$). Therefore, the current i_{A} remain the same instead of increasing linearly in Mode B1.

The analysis for the time interval $t_3 - t_4$ is the same as the time interval $t_3 - t_4$ in

Case 3 of Mode A5 in the Boost state as shown in Figure 4.5(q). The time duration of zero current is derived as (4.14). The constraint conditions and transmission power are shown in Table A.6.

$$t_{i0} = \frac{D - 2\phi + Dd + d\phi}{2d - 1} \tag{4.14}$$

Case b: When $\phi \geq \pi/3$, the waveforms of this case can be found in Figure 4.6(b). The analysis for the time interval $t_0 - t_3$ is the same as the time interval $t_0 - t_3$ in Case 2 in Mode B3 of the Buck state as shown in Figure 4.5(m), Figure 4.5(h) and Figure 4.5(i).

During the time interval $t_3 - t_4$, the equivalent circuit is shown in Figure 4.5(j). The voltage across L_{A} is zero so the current i_{A} stay as the same. The time duration of zero current is derived as (4.15). The ZVS can be achieved in both the primary side and secondary side.

$$t_{i0} = \frac{6D + 3\phi - 5\pi + 6Dd + 5\pi d - 9d\phi}{12d - 6} \tag{4.15}$$

Mode C2

The waveforms of this mode are shown in Figure 4.6(c). Roughly speaking, the constraint conditions is $t_{i0} = T$ which means the current is zero all the time. However, the current is not always zero but very close to zero. After the switching, the current not increases or decreases like the other modes but stay the same value due to the matching of the voltage. At t_0, S_1 is turned ON and its equivalent circuit is shown in Figure 4.5(q). Since the voltage across the leakage inductance is zero, the current is a very small value. The current is small but need to force the body diode to conduct like S_3 as shown in Figure 4.5(q).

For the time interval $t_1 - t_2$, the equivalent circuit is shown in Figure 4.5(u). Since there is almost no current in the leakage inductor and all switches for Phase C are closed, v_{CO} and $v_{\mathrm{cO'}}$ are zero. The voltage v_{HC} and v_{hc} are derived to be $V_{\mathrm{i}}/2$ and $V_{\mathrm{o}}/2$. Based on KVL, v_{AO} and $v_{\mathrm{aO'}}$ are $V_{\mathrm{i}}/2$ and $V_{\mathrm{o}}/2$, respectively. The current is still a very small value.

The current is almost zero because the matching of the voltage across the leakage inductance. However, very small current still exists in the circuit. For the time interval t_0 to t_1, the circuit is shown in Figure 4.5(q). From time interval t_1 to t_2, the circuit is shown in Figure 4.5(u). Based on the analysis, the constraint condition is $0 \leq \phi < D$. The power is close to zero, $P = 0$.

Mode C3

When the time t_{i0} is zero as shown in Figure 4.6(d) and Figure 4.6(e), it can be observed that this mode is the normal operation mode for three-phase DAB converter. It can be divided into 2 cases by $D \leq \phi < \pi/3$ and $\pi/3 \leq \phi < 2\pi/3$.

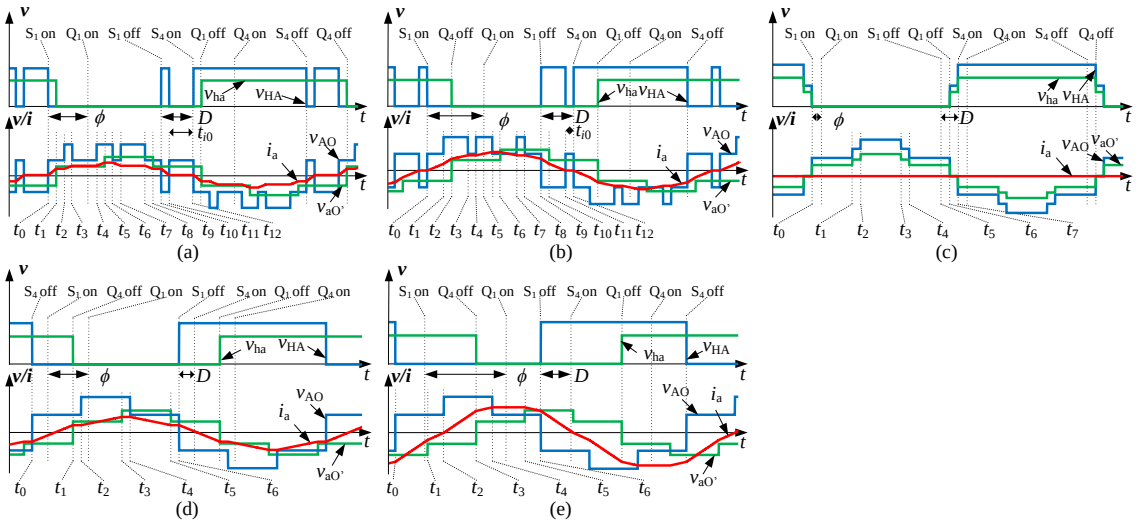


Figure 4.6: Operation waveforms for Matching state.

4.4 Experiment Verification

To verify the dead-time effect analysis, a three-phase DAB converter experiment setup is built. Three individual transformers with 1:6 turn ratio are utilized. For this boost stage, the input voltage is 26V, and the output voltage is 180V. As for the buck state, the input and output voltage are set as 34V and 180V, respectively. For the matching state, the input is 30V and the output voltage is 180V. The detailed specifications of the experiment are shown in Table 4.1. To better illustrate the dead-time effect phenomena, 50kHz switching frequency is applied. Although the specifications are not the same as it in other chapters, the dead-time effect analysis is general to be used for the prototype in this thesis. The experimental results for the boost state, the buck state and the matching state are shown in Figure 4.7.

Table 4.1: Specifications of the dead-time effect experiment setup.

Parameters	Value
Input DC voltage V_{i} (Boost/Buck/Matching)	26V/34V/30V
Output DC voltage V_{o}	180V
Switching frequency f	50kHz
Leakage inductance L	$1.76\mu H$
Transformer ratio n	1:6
Input capacitor C_1	$100\mu F$
Output capacitor C_2	$40\mu F$

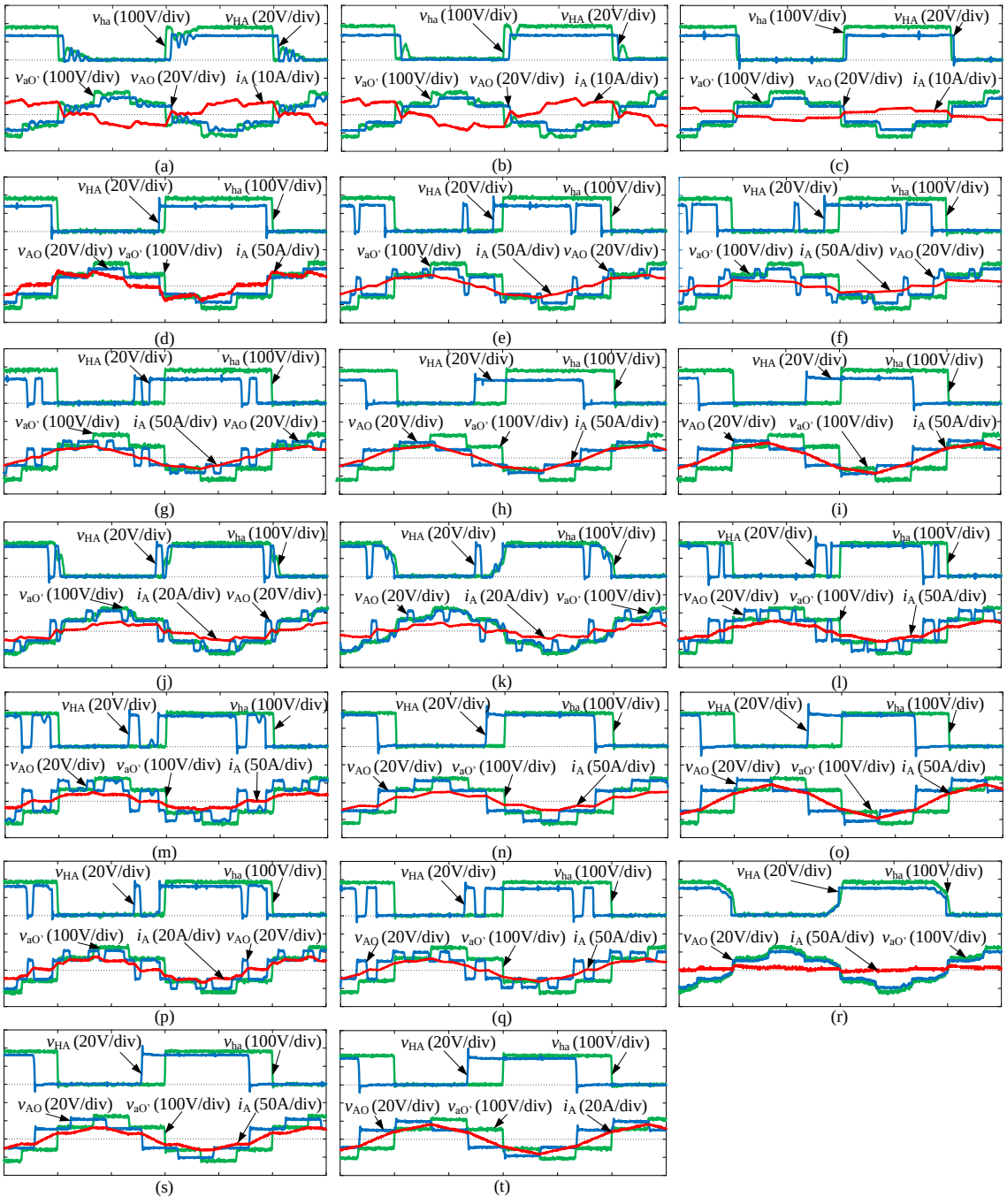


Figure 4.7: Experimental results of the dead-time effect analysis (Time scale: $15\mu s/div$).

The experiment conditions are summarized as following. Boost state: (a) $D = 0.96, \phi = 0$; (b) $D = 0.70, \phi = 0.48$; (c) $D = 0.52, \phi = 0.48$; (d) $D = 0.35, \phi = 0.52$; (e) $D = 0.55, \phi = 1.07$; (f) $D = 0.96\phi = 1.29$; (g) Mode A1: $D = 0.52, \phi = 0.87$; (h) $D = 0.35, \phi = 0.99$; (i) $D = 0.38, \phi = 1.11$. Buck State: (j) $D = 0.44, \phi = 0.14$; (k) $D = 0.40, \phi = 0.52$; (l) $D = 0.58, \phi = 0.82$; (m) $D = 0.96, \phi = 1.17$; (n) $D = 0.38, \phi = 0.62$; (o) $D = 0.57, \phi = 1.08$. Matching state: (p) $D = 0.85, \phi = 0.98$; (q) $D = 0.70, \phi = 1.12$; (r) $D = 0.91, \phi = 0.47$; (s) $D = 0.38, \phi = 0.77$; (t) $D = 0.38, \phi = 1.11$. It can be found that the experiment results match the simulation results in Figure 4.3, Figure 4.4 and Figure 4.6. The experiments are also conducted to verify the analytical transmission power equations. The transmission power comparison is shown in Figure 4.8.

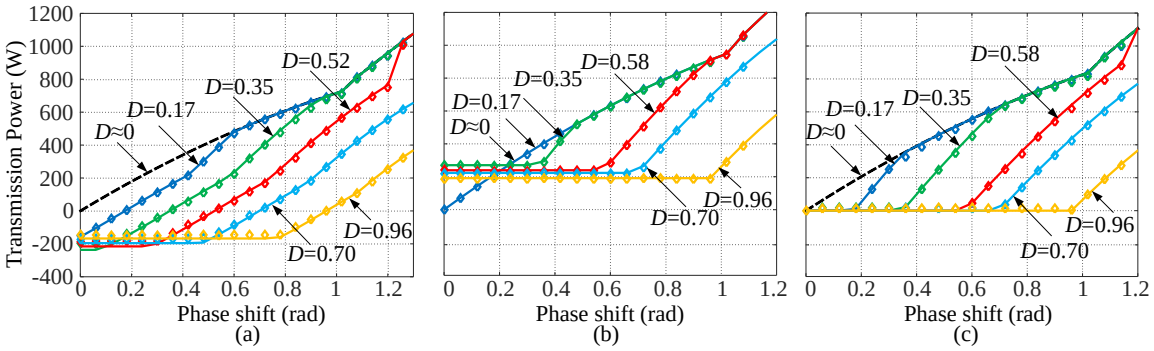


Figure 4.8: Transmission power of the three-phase DAB converter with different dead-time: (a) Boost state; (b) Buck state; (c) Matching state.(Solid line: Theoretical results with dead-time effect; Dash line: Conventional results; Diamond mark: Experimental results).

The benchmark is the simulated transmission power of the conventional operation which is the dash line in Figure 4.8. The dead-time of the dash line is a relatively small value ($D \approx 0$) than the dead-time effect analysis to ensure the conventional operation. The so-called phase shift drift exists in all the three states. General speaking, the

dead-time decreases the transmission power of the three-phase DAB converter. It can be found there is a sudden rise at $\pi/3$ in the conventional operation due to the operation modes change of the three-phase DAB converter from the operation with the phase shift in $0 \leq \phi < \pi/3$ and the operation with the phase shift in $\pi/3 \leq \phi < 2\pi/3$.

4.5 Conclusion

In this chapter, the dead-time effect of the three-phase DAB converter is comprehensively analysed. The detailed operation states, transmission power, constrain equations and switching characterization are provided. The dead-time phenomena in single-phase DAB converter, such as voltage polarity reversal, voltage sag and phase shift, is also existing in the three-phase topology. The experiment results and simulation results verified the theoretical analysis. This study can help to better design of the three-phase DAB converter to avoid the dead-time effect and better understanding of the operation with dead-time effect. The future work can also focus on how to utilize the dead-time effect to reduce the power loss at light load condition.

Chapter 5

DC-Bus Design with Hybrid Capacitor Bank for Single-Phase Inverters

5.1 Introduction

The active or passive decoupling method has to be utilized to deal with the second-order harmonic existing in the DC-bus of the grid-tied single-phase inverters as Figure 5.1. Compared with the active decoupling method, the passive decoupling method is simpler, cheaper and more reliable. The electrolytic capacitors are usually used in the DC-bus as typical passive decoupling components. The film capacitors can be added in parallel with the electrolytic capacitor to help filtering out the high frequency harmonics to extend the electrolytic capacitors' life. In addition, the LC resonant filter can be utilized for the decoupling purpose to achieve better performance. However due to the relatively low resonant frequency, it results in large inductance which will

significantly increase the size and cost of the system. A current sharing method is proposed in this chapter. With this method, an inductor with reasonable size can be utilized in the LC resonant filter to further extend the electrolytic capacitors' life. In this chapter, the design procedure of the hybrid capacitor bank for the single-phase inverter with unipolar modulation will be discussed. In this chapter, the specifications in this chapter is utilized as an illustration of the design procedure and current sharing strategy. Although it's not the same as it in other chapters, the theory can be applied to the case in this thesis. The simulation and experimental results will be provided to verify the design of the hybrid capacitor bank for a 3kW single-phase grid-tied inverter.

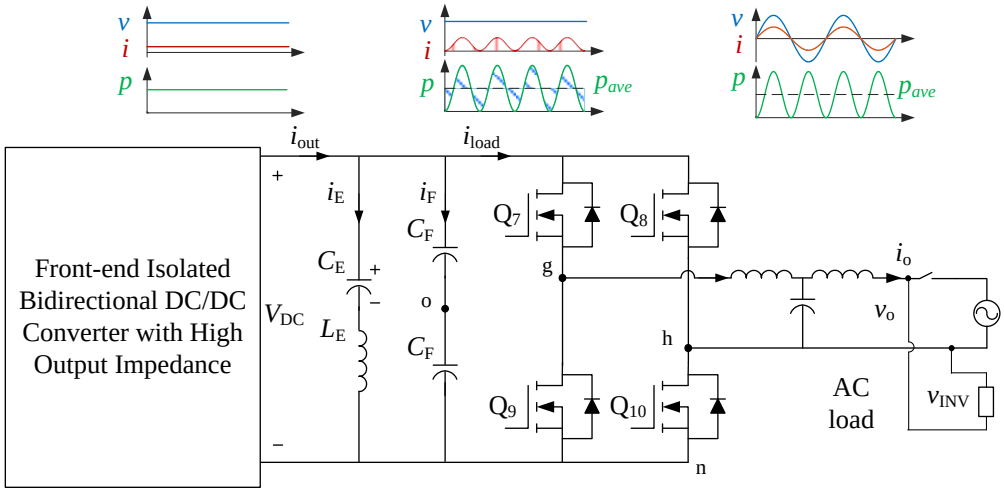


Figure 5.1: Downstream single-phase inverter with hybrid capacitor bank.

In this chapter, a hybrid capacitor bank, including film capacitors and the LC resonant filter with small inductor is proposed for the single-phase grid-tied inverter as shown in Figure 5.1. C_E is the electrolytic capacitor bank and, L_E is the inductor with reduced size, thus L_E C_E represents the LC resonant filter. C_F represents the film capacitor. The detailed design procedure of the electrolytic and film capacitors

is discussed in Section 5.2. The LC resonant filter design for this application is discussed in Section 5.3. Simulation and experimental results are provided to verify the proposed hybrid capacitor bank in Section 5.4.

5.2 Design of the Hybrid Capacitor Bank

5.2.1 Design of the Electrolytic Capacitor

The interested system is discussed in Section 2.7 and shown as Figure 5.1. The hybrid capacitor bank is expected to filtering out the harmonics caused by the single-phase inverter to achieve a stable DC-bus voltage. The electrolytic capacitor is used to buffer the double frequency harmonic while the film capacitor is responsible for the high frequency harmonics. It is assumed that the grid voltage is $v_{\mathrm{g}}(t) = V_{\mathrm{g}}\cos(\omega t)$ and the output current is $i_{\mathrm{g}}(t) = I_{\mathrm{g}}\cos(\omega t - \phi)$, where φ is the phase angle with respect to the grid voltage. For simplicity, harmonics in the output current of the inverter i_{o} are not considered at this time, which won't cause much error (Kolar and Round, 2006). Therefore, it is assumed that $i_{\mathrm{o}}(t) \approx i_{\mathrm{g}}(t) = I_{\mathrm{g}}\cos(\omega t - \phi)$. With the unit power factor, the capacitance is designed by small signal analysis in (Krein *et al.*, 2012) as (5.1).

$$C_{\mathrm{E}} = \frac{P_{\mathrm{o}}}{2\pi f V_{\mathrm{DC}} \Delta V} = \frac{V_{\mathrm{g}} I_{\mathrm{g}}}{2\pi f V_{\mathrm{DC}} \Delta V} \tag{5.1}$$

where f represents the grid frequency which is 60Hz in North America.P_{o} is chosen as 3kW and V_{DC} is the 400V for our case. ΔV is the maximum allowed voltage variation in DC-bus and is chosen as 5%. The RMS current going through the electrolytic

capacitor is obtained as (5.2).

$$i_{C_{\mathrm{E}},\mathrm{RMS}} = \frac{P_{\mathrm{o}}}{\sqrt{2}V_{\mathrm{DC}}} \tag{5.2}$$

5.2.2 Design of the Film Capacitor

The unipolar SPWM modulation is applied for the single-phase inverter because the switching harmonic frequency of the inverter output is twice of its switching frequency. Therefore, the size of passive component in the system will be reduced. The RMS current of the three-phase inverter and bipolar SPWM single-phase inverter are calculated in (Kolar and Round, 2006). However, the RMS current analysis of the unipolar SPWM single-phase inverter is not discussed. The unipolar SPWM modulation process is illustrated in Figure 5.2. It is assumed that the inverter's voltage is in the same phase as the grid voltage.

In Figure 5.2, the two red lines represent the two reference signals for unipolar modulation. The voltage across Q_9 and Q_{10} are shown as blue curves and the green curve represents the inverter's output voltage. ω represents the radial speed of the grid, m is the modulation index and T_c represents the period of the carrier signal.

Based on the basic geometric principles,

$$\frac{m\cos(\omega t_0)}{1} = \frac{t_2 - t_1}{t_2 - t_0} = \frac{t_2 - t_1}{T_c/4} \quad 0 \le \omega t_0 \le \pi/2 \tag{5.3}$$

$$t_1 - t_0 = \frac{T_c}{4} - \frac{T_c}{4} m\cos(\omega t)\} \tag{5.4}$$

So the duty cycle for Q_9 is

$$d_{\text{gn}}(t) = \frac{T_c - 2 \times (t_1 - t_0)}{T_c} = \frac{1}{2}(1 + m\cos(\omega t)) \tag{5.5}$$

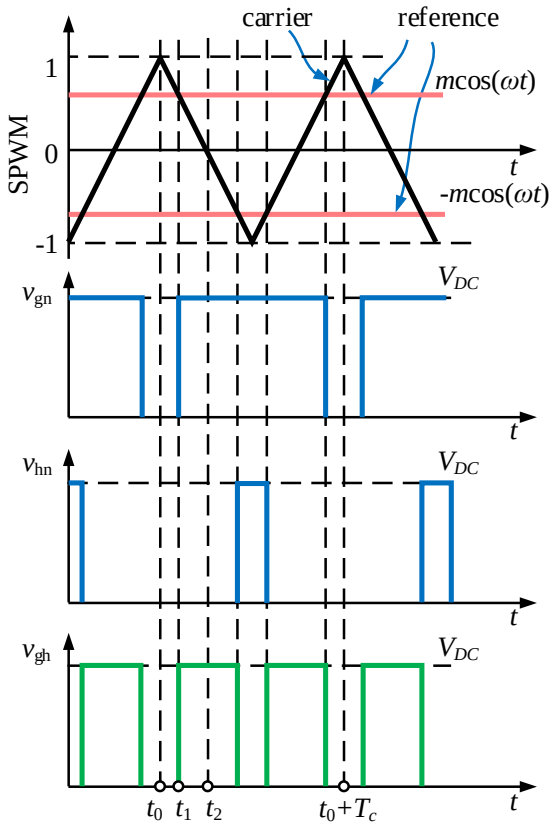


Figure 5.2: Unipolar SPWM modulation illustration.

Based on the same procedure, the duty cycle for Q_{10} is

$$d_{\text{hn}}(t) = \frac{1}{2}(1 + m\cos(\omega t + \pi)) \tag{5.6}$$

Thus the duty cycle for unipolar SPWM modulation can be expressed as (5.7).

$$d_{\mathrm{gh}}(t) = d_{\mathrm{gn}}(t) - d_{\mathrm{hn}}(t) = |m\cos(\omega t)| \tag{5.7}$$

The squared input current of the single-phase inverter can be expressed by the product of its squared output current and the duty cycle of the unipolar SPWM modulation. The square of the input current can be calculated by (5.8).

$$i_{\mathrm{INV}}^2(t) = d_{\mathrm{ab}}(t) \cdot i_{\mathrm{o}}^2(t) = |m\cos(\omega t)| \cdot I_{\mathrm{g}}^2 \cos^2(\omega t + \phi) \tag{5.8}$$

The RMS value of the input current can be calculated by (5.9), assuming $\theta = \omega t$.

$$\begin{aligned} I_{\mathrm{INV,RMS}}^2 &= \frac{1}{\pi}\int_0^{\pi} i_{\mathrm{INV}}^2(\theta)d\theta \\ &= \frac{1}{\pi}\int_0^{\pi} |m\cos\theta| \cdot I_{\mathrm{g}}^2\cos^2(\theta+\phi)d\theta = \frac{4mI_{\mathrm{g}}^2}{3\pi}\cdot\cos^2\phi + \frac{2mI_{\mathrm{g}}^2}{3\pi}\cdot\sin^2\phi \end{aligned} \tag{5.9}$$

The RMS value of the input current includes three components, DC current, the double frequency harmonic current and the high frequency harmonic current. Based on the concept of the RMS value, the RMS value of i_{INV} can also be expressed by the sum of the RMS value of its components as (5.10).

$$I_{\mathrm{INV,RMS}}^2 = I_{C_{\mathrm{F}},\mathrm{RMS}}^2 + I_{\mathrm{DC}}^2 + I_{C_{\mathrm{E}},\mathrm{RMS}}^2 \tag{5.10}$$

Ideally, all the high frequency harmonics should be filtered out by the film capacitors. Thus, the RMS value of the high frequency current is

$$\begin{aligned} I_{C_{\mathrm{F}},\mathrm{RMS}} &= \sqrt{\frac{4mI_{\mathrm{o}}^2}{3\pi}\cdot\cos^2\phi + \frac{2mI_{\mathrm{o}}^2}{3\pi}\cdot\sin^2\phi - I_{\mathrm{DC}}^2 - I_{C_{\mathrm{E}},\mathrm{RMS}}^2} \\ &= \sqrt{\frac{4mI_{\mathrm{o}}^2}{3\pi}\cdot\cos^2\phi + \frac{2mI_{\mathrm{o}}^2}{3\pi}\cdot\sin^2\phi - \frac{m^2I_{\mathrm{o}}^2}{4}\cos^2\phi - \frac{m^2I_{\mathrm{o}}^2}{8}} \end{aligned} \tag{5.11}$$

The capacitance of the film capacitor can be calculated by $C = \Delta Q/\Delta V$. The voltage variation for the film capacitors should be chosen as the system requirement, which is 1% for our application. When selecting the voltage variation of the film capacitor, it should be lower than the voltage variation of the electrolytic capacitor. Because compared with double frequency, the other harmonic currents have much larger frequency. So the capacitance should be calculated by the maximum value of the coulomb go through the film capacitor. The coulomb can be calculated by

$$\begin{aligned} Q(t) &= \int i_{C_{\mathrm{F}}}(t)dt = T_{\mathrm{on}}\cdot(i_{\mathrm{INV}}(t) - i_{\mathrm{INV,AVE}}(t)) \\ &= \frac{d_{\mathrm{ab}}(t)}{2}\times T_s \times [i_{\mathrm{INV}}(t) - \int_{t_0}^{t_0+T_c} i_{\mathrm{INV}}(t)dt] \\ &= \frac{1-d_{\mathrm{ab}}(t)}{2}\times T_s \times [\frac{mI_{\mathrm{o}}}{2}\cos\phi - \frac{mI_{\mathrm{o}}}{2}\cos(2\omega t+\phi)] \qquad \omega t\in[0,\pi] \end{aligned} \tag{5.12}$$

Obviously, the coulomb varies with time. The equation is function of modulation index, phase angle and the power rating. The modulation index is constant if the output inverter voltage and DC-link voltage are chosen. The analytic equation of the maximum coulomb from (5.12) can be obtained however it's too complicated. Therefore, it's more convenient to use simulation to help calculate the maximum coulomb value by software. The relationship for 3kW maximum power and 150kHz

switching frequency is plotted by MATLAB as Figure 5.3 where we can read the maximum coulomb value.

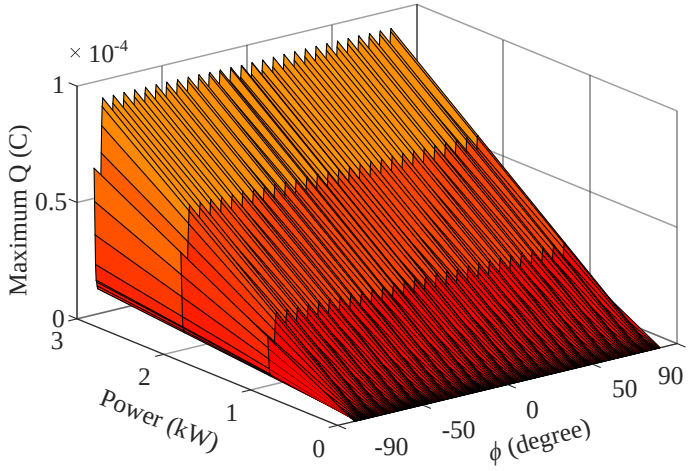


Figure 5.3: Maximum Q for calculating the film capacitor.

In our case, the capacitance of the film capacitor is calculated as (5.13).

$$C_{\mathrm{F}} = \frac{Q_{\mathrm{Max}}}{\Delta V} \tag{5.13}$$

5.3 Current Sharing Method for the Hybrid Capacitor Bank

Until now, the design of the electrolytic and film capacitors is completed based on the ideal case. However, the electrolytic capacitors should be oversized since some of the high frequency switching harmonic will be filtered out by them. The LC resonance filter whose resonant frequency is tuned at 120Hz can be applied for the current share in the hybrid capacitor bank. However, the drawback is that the additional inductor will increase the size of DC-bus and the voltage stress of the electrolytic capacitors.

Thus, reasonable value of the inductor should be chosen.

To understand the problem, the spectra analysis of the input current i_{INV} should be deduced. The voltage harmonic for the single-phase inverters are illustrated in (Holmes and Lipo, 2003). The input current of the three-phase inverter and bipolar SPWM single-phase inverter are calculated in (McGrath and Holmes, 2009). The input current of the inverter equals to the product of the SPWM signal and the inverter's output current which is assumed to be ideally sinusoid. Besides the double frequency harmonic, there are high frequency harmonics whose dominant frequency will be around doubled switching frequency for unipolar SPWM modulation. Unlike the rough calculation of i_{INV} as (5.8), the analytical expression for input current of the single-phase inverter with unipolar SPWM modulation is shown as (5.14), where ω is the angular speed of the grid and ω_s represents the angular speed of switching frequency. In our case, the grid frequency is 60Hz so the double frequency harmonic is 120Hz. The switching frequency of the single-phase inverter is chosen as 150kHz. Thus, the main high frequency switching harmonics is around 300kHz.

$$\begin{aligned} i_{\mathrm{INV}}(t) &= \frac{m}{2} I_{\mathrm{o}} \cos(\phi) + \frac{m}{2} I_{\mathrm{o}} \cos(2\omega t + \phi) \\ &+ \sum_{j=1}^{\infty} \sum_{k=-\infty}^{\infty} \left\{ \begin{array}{l} \frac{I_{\mathrm{o}}}{j\pi} \cos([j+k]\pi) \cos(\phi) \times [J_{2k+1}(j\pi m) - J_{2k-1}(j\pi m)] \cos(2j\omega_{\mathrm{s}} t + 2k\omega t) + \\ \frac{I_{\mathrm{o}}}{j\pi} \cos([j+k]\pi) \sin(\phi) \times [J_{2k+1}(j\pi m) + J_{2k-1}(j\pi m)] \sin(2j\omega_{\mathrm{s}} t + 2k\omega t) \end{array} \right\} \end{aligned} \tag{5.14}$$

The equivalent circuit of the hybrid capacitor bank is shown as Figure 5.1. The stray resistance and inductance of the film capacitor are neglected. The stray parameters of the electrolytic are also not considered since they are negligible compared with impedance of L_{E}. For the convenience of the analysis, it assumes that the closed-loop controller of the DC/DC converter is ideal i_{DC} has no harmonics. In the best

scenario, the double frequency current harmonic will be buffered by the electrolytic capacitor while the high frequency switching harmonics is filtered through the film capacitors. However, in reality the share of the current harmonic between the electrolytic capacitor leg and film capacitor leg depends on the ratio of their impedance. The impedance of the resonant filter and film capacitor can be expressed by (5.15) and (5.16).

$$Z_{\mathrm{R}}(j\omega) = j(\omega L_{\mathrm{E}} - \frac{1}{\omega C_{\mathrm{E}}}) \tag{5.15}$$

$$Z_{\mathrm{F}}(j\omega) = -\frac{j}{\omega C_{\mathrm{F}}} \tag{5.16}$$

The current share in the resonant filter can be represented as the coefficient as (5.17).

$$Zc(\omega) = \frac{|Z_{\mathrm{F}}(j\omega)|}{|Z_{\mathrm{R}}(j\omega)| + |Z_{\mathrm{F}}(j\omega)|} = \frac{C_{\mathrm{E}}}{|\omega^2 C_{\mathrm{F}} C_{\mathrm{E}} L_{\mathrm{E}} - C_{\mathrm{F}}| + C_{\mathrm{E}}} \tag{5.17}$$

The current went through the resonant filter can be expressed as (5.18). The RMS current in the resonant filter leg can be calculated by the sum of each component's RMS value as (5.19).

$$\begin{aligned} i_{\mathrm{E}}(t) &= Zc(2\omega)\frac{m}{2} I_{\mathrm{o}} \cos(2\omega t + \phi) \\ &+ \sum_{j=1}^{\infty}\sum_{k=-\infty}^{\infty} \left\{ \begin{array}{l} \frac{I_{\mathrm{o}}}{j\pi} \cos([j+k]\pi)\cos(\phi) \times Zc(2j\omega_{\mathrm{s}} + 2k\omega)[J_{2k+1}(j\pi m) - J_{2k-1}(j\pi m)]\cos(2j\omega_{\mathrm{s}} t + 2k\omega t) + \\ \frac{I_{\mathrm{o}}}{j\pi} \cos([j+k]\pi)\sin(\phi) \times Zc(2j\omega_{\mathrm{s}} + 2k\omega)[J_{2k+1}(j\pi m) + J_{2k-1}(j\pi m)]\sin(2j\omega_{\mathrm{s}} t + 2k\omega t) \end{array} \right\} \end{aligned} \tag{5.18}$$

$$\begin{aligned} I_{\mathrm{E,RMS}}^2 &= \left[Zc(2\omega)\frac{m}{2} I_{\mathrm{o}} \right]^2 \\ &+ \sum_{j=1}^{\infty}\sum_{k=-\infty}^{\infty} \left\langle \begin{array}{l} \cos([j+k]\pi) \times \left\{ \frac{I_{\mathrm{o}}}{j\pi} \cos(\phi) Zc(2j\omega_{\mathrm{s}} + 2k\omega)[J_{2k+1}(j\pi m) - J_{2k-1}(j\pi m)] \right\}^2 + \\ \cos([j+k]\pi) \times \left\{ \frac{I_{\mathrm{o}}}{j\pi} \sin(\phi) Zc(2j\omega_{\mathrm{s}} + 2k\omega)[J_{2k+1}(j\pi m) + J_{2k-1}(j\pi m)] \right\}^2 \end{array} \right\rangle \end{aligned} \tag{5.19}$$

Based on the design of the electrolyte capacitor in previous section, LLS2V471MELB Nichicon (voltage rating: 350V; Capacitance: 470uF; Ripple current: 2.53A@120Hz)

is chosen considering size and price. Two capacitors will be connected in series to match the voltage level and three strings will be connected in parallel for redundancy. The lifetime of the LLS series electrolytic capacitor can be estimated by the online tool from Nichicon. The lifetime estimation as (5.20) is not a guaranteed life specification but it's accurate enough for our research purpose.

$$L_{\mathrm{n}} = L_0 \times 2^{\frac{T_0 - T_{\mathrm{n}}}{10}} \times 2^{1-\frac{\Delta t_{\mathrm{n}}}{K}} \qquad \Delta t_{\mathrm{n}} = \Delta t_0 \times (\frac{I_{\mathrm{n}}}{I_{\mathrm{m}}})^2 \tag{5.20}$$

Where L_0 is the specified life time (3000 hours), T_0 is the max operating temperature (85^oC), Tn is the ambient temperature (chosen as 25^oC), K is the Boltzmann's constant, In is the applied current and I_m is the rating current of capacitor. The frequency dependency ESR of the electrolytic capacitor results in a frequency coefficient of the ripple current RMS value. It is considered when rating the capacitor and calculating its life time. For this type of electrolytic capacitor, the frequency coefficient of 50kHz or more is 1.43. In addition, the ESL of the medium size electrolytic capacitor is from10nH to 30nH (Nichicon, 2009).

Conventionally, the inductance of the resonant filter is tuned with the 120Hz resonant frequency as (5.21). However, the inductor with this rating is usually quite large and costly.

$$L_{\mathrm{E,C}} = \frac{1}{\omega^2 C_{\mathrm{E}}} \tag{5.21}$$

The impedance is plotted as The RMS ripple current and its corresponding estimated life time is plotted with different inductance selection from 10nH to 1.25mH as Figure 5.4.

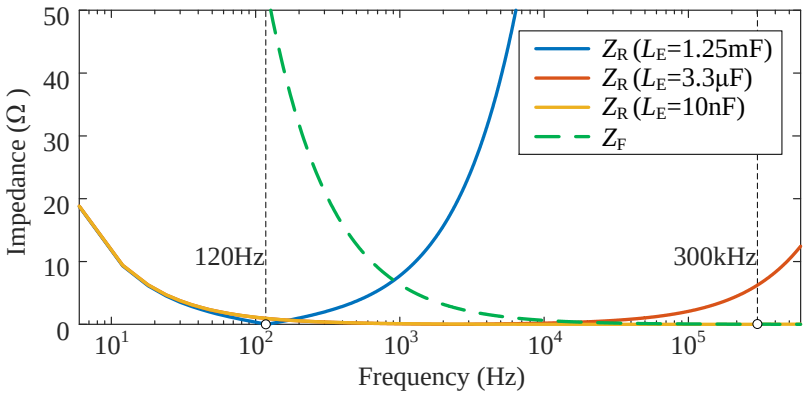


Figure 5.4: Impedance of the resonant filter and film capacitor.

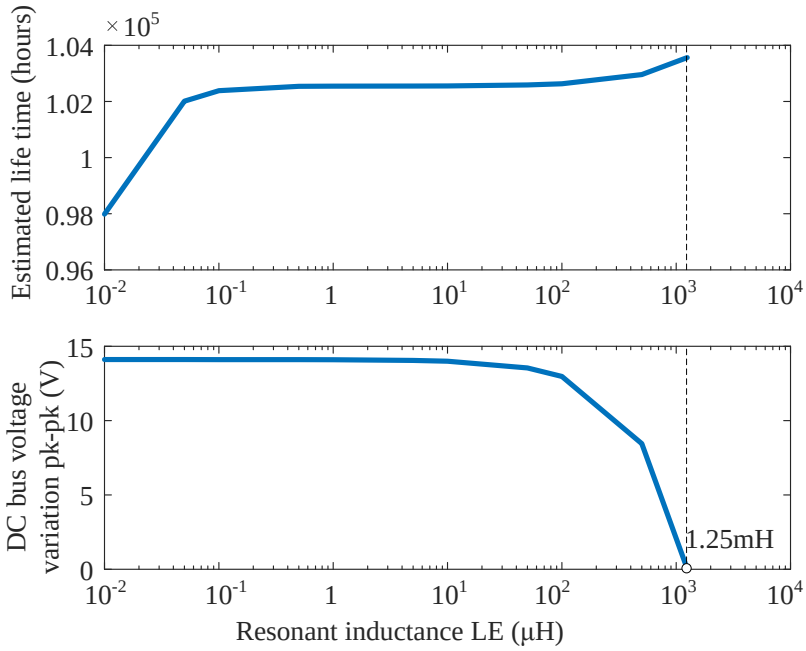


Figure 5.5: Estimated lifetime of the electrolytic capacitor and DC-bus voltage variation with different resonant inductance L_E.

From Figure 5.4, we can observe that the add-on inductor will increase the impedance at high frequency as 300kHz for this case. The high frequency harmonic currents tend to go through the film capacitor. So the higher L_E will result in lower RMS value of the ripple current in the electrolytic capacitors. Finally, longer life time will be

achieved. From Figure 5.5, we can directly observe that the electrolytic capacitor will achieve life time saving by adding the resonant inductor. But larger L_{E} will result in significant reduction in the DC-bus voltage variation. However, the DC-bus is already designed by the maximum allowable voltage variation. Thus the benefit of using a large L_{E} will not make up the disadvantage in practice. Thus, L_{E} is chosen as a reasonable value, like 3.3μH, resulted from the tradeoff between the lifetime saving and the size and cost of the system.

5.4 Simulation and Experimental Results

The design of the hybrid capacitor bank and the current sharing method is verified by the simulation and experiment results in this section. The hybrid capacitor bank is designed for 3kW grid-tied single-phase inverter with 150kHz switching frequency. Based on the design in previous analysis, the passive components are selected by the off-the-shelf items from Digikey and Coilcraft. The design value and the selected value are listed as Table 5.1. The manufacturer part number is also shown.

Table 5.1: Passive component of the applied DC bus.

	Designed value	Selected value	Manufacturer Part number
C_E(mF)	0.994	1.41	LLS2V471MELB
L_E(μH)	3.3	3.3	VER2923-332KL
C_F(μF)	23.1	25	B32796E2256

The simulation is used to verify the current sharing with different resonant inductance value as Figure 5.7. The simulation model is built by MATLAB/Simulink. From the simulation results, we can see that the RMS value of the current going

through the electrolytic capacitors reduces significantly by adding an inductor in series with the capacitor to form a resonant filter.

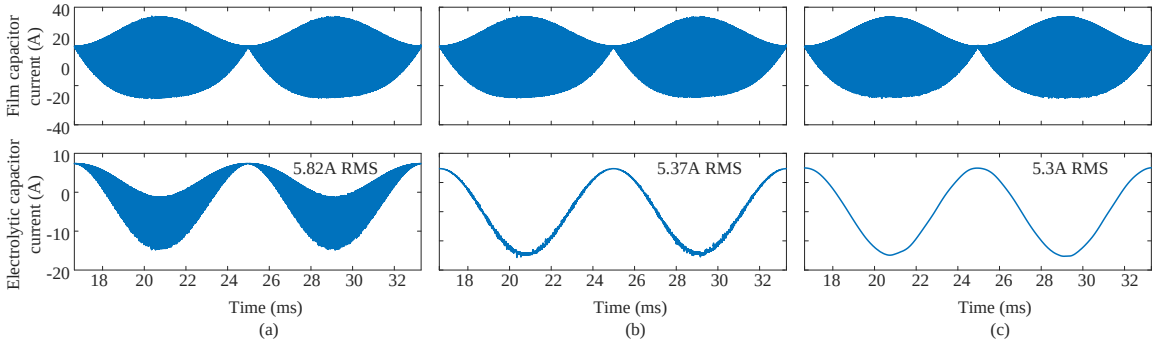


Figure 5.6: Current sharing performance: (a) $L_E = 10$nH; (b) $L_E = 3.3\mu$H; (c) $L_E = 1.25$mH.

In this way, the life time of the electrolytic capacitor can be saved. Moreover, the most current reduction can be achieved by designing the inductor at the resonant frequency, 1.25mH while the RMS value can be reduced significantly by adding a reasonably small inductance, like 3.3μH which is 0.2% of the conventional inductance design with the same current rating. We make the following conclusions that in terms of life time saving for the electrolytic capacitor: (1) It's practical to design the capacitor bank as a hybrid capacitor bank which combines electrolytic capacitors and film capacitors; (2) Adding an small value of inductor in series with the electrolytic capacitor to form a resonant filter will further extend the life time of the electrolytic capacitor. Additionally, since the ESR value of the electrolytic capacitor is relatively large, the reduction of the RMS value of the current will result in the power loss reduction of the system.

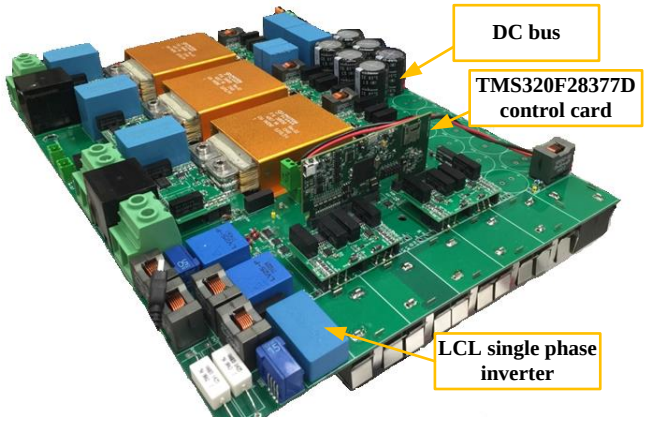


Figure 5.7: Experiment setup for hybrid capacitor bank.

The experiment setup is shown as Figure 5.7 where the LCL single-phase inverter passive-damping is built. The full bridge inverter is controlled by the TI DSP28377D microcontroller. The experimental results showed as Figure 5.8 also verify the current sharing method. The RMS value i_E is reduced from 5.53A to 5.39A by adding a 3.3μH inductor in series with the electrolytic capacitor. It should be noted that the benchmark experiment as Figure 5.8(a) is done by replace the 3.3μH with a wire. This wire will also add some stray inductance to the electrolytic capacitor thus its RMS value is lower than the simulation results as Figure 5.6(a) which is ideal condition.

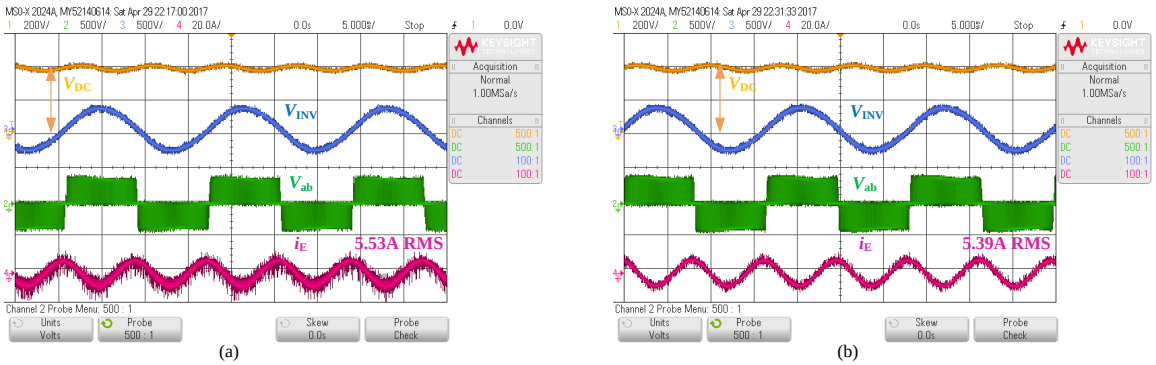


Figure 5.8: Experimental verification of the current sharing method: (a) no add-on L_E; (b) $L_E = 3.3\mu$H.

5.5 Conclusion

A hybrid capacitor bank is designed and utilized in the DC-bus of the single-phase inverter system. The hybrid capacitor bank is composed by the LC resonant filter with electrolytic capacitor and film capacitor. The design procedure of the hybrid capacitor bank for the single-phase inverter with unipolar modulation is discussed. The performance of the proposed capacitor bank is verified by both simulation and experimental results.

Chapter 6

Design and Control of Single-Phase Dual Mode LCL Inverter

6.1 Introduction

The LCL inverter as Figure 5.1 is widely applied in the renewable energy application. In North America, the grid-tied inverter usually provides single-phase (120V) and split-phase (240V) output options. The proposed design strategy is to use the same hardware to fulfil the requirement for both 120V and 240V operation in standalone and grid-tied modes. The step-by-step design procedure is provided for the LCL inverter with passive damping. Then the Proportional Resonant (PR) controllers are designed for the standalone and grid-tied modes. The phase-locked-loop (PLL) is used to synchronize the grid voltage in grid-tied operation mode. The simulation and experimental results are provided to verify the filter performance and PR controller performance.

The contributions of this chapter are 1) a step-by-step design procedure of the

LCL inverter with passive damping is proposed for dual mode operation. 2) The PR controllers are design to achieve standalone and grid-tied mode. The organization of this chapter is as follows: Section 6.2 the small-signal models of the single-phase inverter are derived for standalone and grid-tied mode. Section 6.3 will describe the design strategy of the 120V/240V dual mode LCL inverter. Section 6.4 presents PR controller design strategy for standalone and grid-tied modes. Section 6.5 provides simulation and experimental results to verify the LCL filter performance and the PR controller. Finally, Section 6.6 concludes the finding and contributions of this chapter.

6.2 Small-Signal Model of the LCL Inverter

As the first step of the LCL inverter design, the small-signal model of the LCL inverter should be derived. The grid-tied mode and standalone mode of the single-phase inverter are illustrated as Figure 6.1. When the inverter is in grid-tied mode, the inverter will work as current source which synchronized with the grid voltage. On the hand the inverter with standalone mode can be seen as a voltage source to the AC load.

There are lots of methods of modeling the LCL inverter as (Dong, 2009). The classic two-port network is utilized in the work to obtain the transfer function of a LCL filter. This universal method can also be easy to be implemented to other filter types. The two-port network of the single-phase inverter with passive damping can be found in Figure 6.2. On the primary side, the full-bridge inverter is taken as voltage source with PWM waveforms while on the secondary side it's an ideal voltage source with 60Hz as Figure 6.2(a) or a load with impedance as Z_{load} for standalone operation mode.

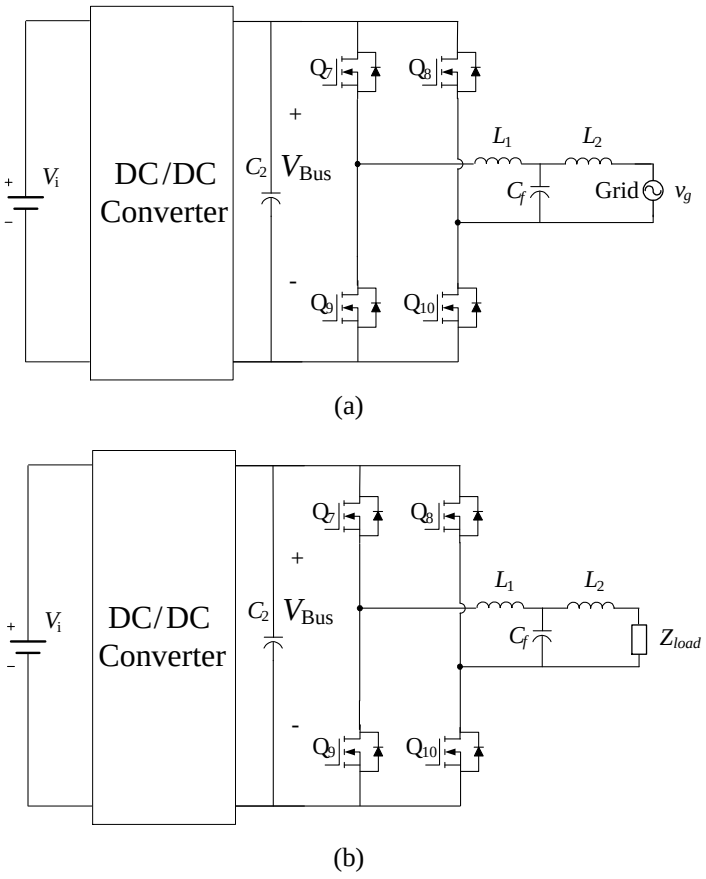


Figure 6.1: The downstream single-phase inverter: (a) Grid-tied mode. (b)Standalone Mode.

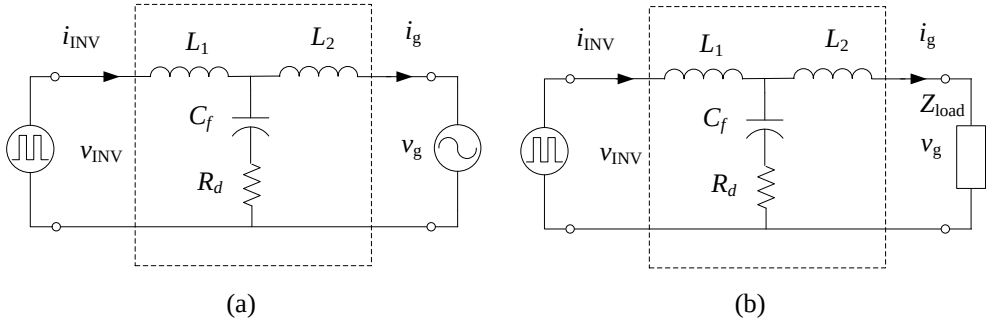


Figure 6.2: Two port network of the single-phase inverter: (a) Grid-tied mode. (b) Standalone mode.

Based on the two-port network as Figure 6.2, the LCL filter can be expressed as (6.1),(6.2),(6.3),(6.4) and (6.5).

$$\begin{bmatrix} i_{\mathrm{INV}} \\ i_g \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} v_{\mathrm{INV}} \\ v_g \end{bmatrix} \tag{6.1}$$

$$Y_{11} = \frac{i_{INV}(s)}{v_{INV}(s)}\Big|_{V_g=0} = \frac{L_2C_fs^2 + C_fR_ds + 1}{L_1L_2C_fs^3 + (L_1+L_2)C_fR_ds^2 + (L_1+L_2)s} \tag{6.2}$$

$$Y_{12} = \frac{i_g(s)}{v_{INV}(s)}\,|_{V_g=0} = -\frac{C_fR_ds + 1}{L_1L_2C_fs^3 + (L_1+L_2)C_fR_ds^2 + (L_1+L_2)s} \tag{6.3}$$

$$Y_{21} = \frac{i_{INV}(s)}{v_g(s)}\,|_{V_{INV}=0} = -\frac{C_fR_ds + 1}{L_1L_2C_fs^3 + (L_1+L_2)C_fR_ds^2 + (L_1+L_2)s} \tag{6.4}$$

$$Y_{22} = \frac{i_g(s)}{v_g(s)}\Big|_{V_{INV}=0} = \frac{L_1C_fs^2 + C_fR_ds + 1}{L_1L_2C_fs^3 + (L_1+L_2)C_fR_ds^2 + (L_1+L_2)s} \tag{6.5}$$

Considering the direction of the grid current i_{g} is opposite with the current of the secondary port in two-port network analysis, the grid current can be expressed as (6.6) using (6.1),(6.4) and (6.5).

$$\begin{aligned} i_g(s) &= -Y_{21}v_{INV}(s) - Y_{22}v_g(s) \\ &= \frac{C_fR_ds + 1}{L_1L_2C_fs^3 + (L_1+L_2)C_fR_ds^2 + (L_1+L_2)s}v_{inv}(s) \\ &-\frac{L_1C_fs^2 + C_fR_ds + 1}{L_1L_2C_fs^3 + (L_1+L_2)C_fR_ds^2 + (L_1+L_2)s}v_g(s) \end{aligned} \tag{6.6}$$

Thus the transfer function of the single-phase inverter with grid-tied mode can be found as (6.7) and (6.8).

$$G_{i_gV_{inv}} = \frac{i_g(s)}{v_{INV}(s)} = \frac{C_fR_ds + 1}{L_1L_2C_fs^3 + (L_1+L_2)C_fR_ds^2 + (L_1+L_2)s} \tag{6.7}$$

$$G_{i_g v_g} = \frac{i_g(s)}{v_g(s)} = \frac{L_1 C_f s^2 + C_f R_d s + 1}{L_1 L_2 C_f s^3 + (L_1 + L_2) C_f R_d s^2 + (L_1 + L_2) s} \tag{6.8}$$

To derive the transfer function of the standalone mode, the grid voltage is (6.9).

$$v_g(s) = -\frac{1}{Y_{22}} i_g(s) - \frac{Y_{21}}{Y_{22}} v_{INV}(s) \tag{6.9}$$

Considering that $v_g(s) = i_g(s) \cdot Z_{load}$, the transfer function of standalone mode, (6.10), can be expressed from (6.9).

$$\begin{aligned} G_{v_g v_{inv}} &= \frac{v_g(s)}{v_{INV}(s)} = -\frac{Y_{21} Z_{load}}{Y_{22} Z_{load} + 1} \\ &= \frac{C_f R_d Z_{load} s + Z_{load}}{L_1 L_2 C_f s^3 + +(L_1 + L_2) C_f R_d s^2 + L_1 C_f Z_{load} s^2 + C_f R_d Z_{load} s + (L_1 + L_2) s + Z_{load}} \end{aligned} \tag{6.10}$$

6.3 Design of the 120V/240V Dual-Mode LCL Inverter

The specification of the LCL inverter can found as Table 6.1. The design requirements of the LCL inverter are as followings.

1. The reactive power won't exceed 5%;
2. Voltage drop of the LCL filter shouldn't over 10%;
3. The current ripple go through the inductor should be 15% 40%;
4. The performance of the filter should fulfil the standard IEEE 1547, IEEE 519 and EN 50160. The current harmonic limit is 0.3% and the voltage limit is less than 0.25%.

The unipolar SPWM is utilized for the single-phase inverter because of its "doubled" switching frequency as discussed in Section 2.5. In this way, the filter size can be designed smaller than that with bipolar SPWM . The step-by-step design procedure is shown as following.

Table 6.1: Specifications of the single-phase inverter.

Parameters	Value
Input DC bus voltage	400V
Output frequency	60Hz
Power rating	1kW for 120V, 3kW for 240V
Switching frequency	100kHz
Others	Flat design, dual mode (grid-tied and standalone)

6.3.1 Design of Inverter Side Inductor L_1

The inverter side inductor is usually sized by the current ripple flowing through it (Reznik *et al.*, 2014). The equation can be found as (6.11).

$$15\% \leq \frac{\Delta I_1}{I_{ref}} = \frac{V_{\text{Bus}}}{8 L_1 f_s I_{ref}} \leq 40\% \tag{6.11}$$

where I_{ref} is the peak value of the output current of the inverter, V_{Bus} is the value of the DC-link voltage and f_s represents the switching frequency. Thus the induction L_1 can be designed by selecting an acceptable current ripple. When selecting inductor, the saturation current should be carefully considered. For example, larger current ripple leads to a smaller inductance but the peak operation current may excess its saturation current.

6.3.2 Design of the Capacitor C_f

From (Reznik *et al.*, 2014), the upper limit of the capacitance can be calculated by its allowed reactive power, $C_{upper} = 0.05C_b$ where $C_b = P_o/(\omega_o V_o^2) \cdot F$. P_o is the active power of the inverter, ω_o is the grid frequency and V_o is the RMS value of the fundamental voltage of the inverter output.

Another perspective to design the capacitance is to use the $L_1 - C_f$ as a second-order filter to attenuate the voltage harmonics for the standalone mode according to (Chen *et al.*, 2008). Assuming the impedance of the grid side inductor L_2 is designed much less than the equivalent AC load, the transfer function (6.10) can be simplified with $L_2 = 0$. Since the damping resistor will decrease of the slope of the filter from -40 dB/decade to -20 dB/decade, it's reasonable to neglect the passive damping resistor R_f to simplify the design of C_f. Then its simplified standalone transfer function is as (6.12).

$$G_{v_g v_{inv}} = \frac{Z_{load}}{L_1 C_f Z_{load} s^2 + L_1 s + Z_{load}} \tag{6.12}$$

The grid voltage can be expressed as $v_g(t) = V_{\text{Bus}} M \cos(\omega_0 t)$ where M is the modulation index. Thus the voltage harmonics of the full bridge single-phase inverter with unipolar SPWM can be expressed as (6.13) from (Holmes and Lipo, 2003).

$$\begin{aligned} &v_{\text{INV}}(t) = V_{\text{Bus}} M \cos(\omega_o t) + \\ &\frac{4V_{\text{Bus}}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2m} J_{2n-1}(m\pi M) \cos([m+n-1]\pi) \cos(2m\omega_{sw} t + [2n-1]\omega_0 t) \end{aligned} \tag{6.13}$$

where ω_{sw} is the switching frequency of the inverter and J represents Bessel function. The voltage harmonic with the highest amplitude is interested when designing the capacitance for standalone mode operation. From (6.13), the amplitude of the

voltage harmonics are (6.14).

$$|v_{\mathrm{INV}}(\omega_h)| = \left|\tfrac{2V_{\mathrm{Bus}}}{\pi m} J_{2n-1}(m\pi M)\right| \quad \omega_h = 2m\omega_{sw} + (2n-1)\omega_0, m = 1, 2, \cdots, \infty \quad (6.14)$$

From (6.13) and (6.14), the largest amplitude occurs at $(2\omega_{sw} \pm \omega_0)$ and the worst case is $(2\omega_{sw} - \omega_0)$. The attenuation requirement of the voltage harmonics can be found from EN 50160. From (6.12) and (6.14), the (6.15) should be fulfilled.

$$|v_g(2\omega_{sw} - \omega_0)| = |v_{\mathrm{INV}}(2\omega_{sw} - \omega_0)| \cdot \left|\frac{1}{4\pi^2(2f_{sw} - f_0)^2 L_1 C_f - 1}\right| \leq 0.25\% V_0 \quad (6.15)$$

Then the capacitance can be calculated as (6.15) from (6.16).

$$C_f \geq \frac{1}{4\pi^2(2f_{sw} - f_0)^2 L_1}\left(\frac{|v_{inv}(2\omega_{sw} - \omega_0)|}{0.25\% V_0} + 1\right) \quad (6.16)$$

6.3.3 Design of the Grid-Side Induction L_2

The principle of designing L_2 is to fulfil the attenuation requirement of grid-tied operation from IEEE 1547. From (6.6), the harmonics of the grid-tied current i_{g} is functions of the inverter output voltage v_{INV} and the grid voltage v_{g}. It can assume that v_{g} doesn't has significant harmonics so the design L_2 just considers the harmonics of v_{INV}. Although v_{g} has some low frequency harmonics as EN 50160, the closed-loop controller can take care of them which will be researched later. Until now, the damping resistor is not designed. The design without damping is discussed here. Following the analysis above, the voltage harmonics in v_{INV} with the highest

amplitude should be focused. Thus the attenuation can be achieved as (6.17).

$$\left|G_{i_g v_{\text{INV\_wd}}}(2\omega_{sw}-\omega_0)\right| = \frac{|i_g(2\omega_{sw}-\omega_0)|}{|v_{\text{INV}}(2\omega_{sw}-\omega_0)|} \tag{6.17}$$

Where $G_{i_g v_{\text{INV\_wd}}}(s)$ represents the transfer function without damping. From IEEE 1547, the requirement should be fulfilled.

$$\begin{aligned} &|i_g(2\omega_{sw}-\omega_0)| \\ &= |v_{INV}(2\omega_{sw}-\omega_0)| \cdot \left| \frac{1}{(L_1+L_2)(2\omega_{sw}-\omega_0) - L_1L_2C_f(2\omega_{sw}-\omega_0)^3} \right| \leq 0.3\%I_0 \end{aligned} \tag{6.18}$$

Thus the induction L_2 is calculated without damping as (6.19).

$$L_{2,wd} = \frac{1}{2\omega_{sw}-\omega_0 - L_1C_f(2\omega_{sw}-\omega_0)^3}\left[\frac{|v_{INV}(2\omega_{sw}-\omega_0)|}{0.3\%I_0} - L_1(2\omega_{sw}-\omega_0)\right] \tag{6.19}$$

Figure 6.3 is used to illustrate how to design L_2 with passive damping (red line) from the design without damping (blue line). The slope without damping after resonant frequency is -60 dB/decade while the slope is -40 dB/decade with damping. However, no matter which case, the lines should go through the attenuation point $D(2\omega_c-\omega_0, 20\log_{10}\left|G_{i_g v_{inv}}\right|)$.

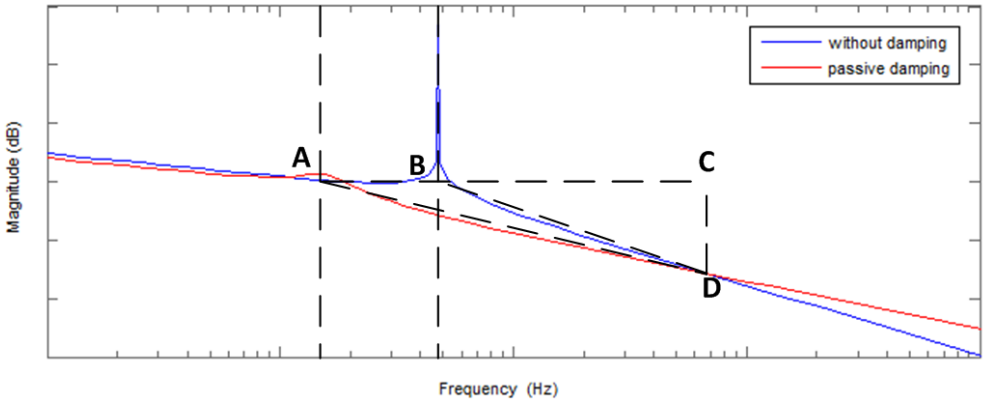


Figure 6.3: Comparison of grid-tied transfer function of LCL between with damping and without damping.

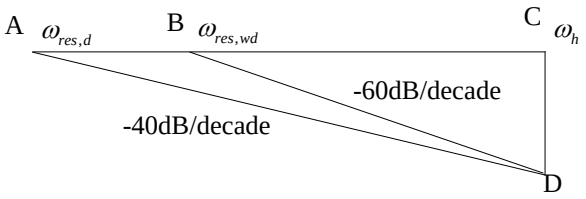


Figure 6.4: Detailed analysis of the passive damping influence.

Based on the geometric analysis of Figure 6.4,

$$\frac{\omega_h}{\omega_{res\_wd}} \times 60 = \frac{\omega_h}{\omega_{res\_d}} \times 40 \tag{6.20}$$

Where ω_h is the frequency at which we should attenuate, ω_{res_d} is the resonant frequency of the LCL filter with passive damping and ω_{res_wd} is the resonant frequency of the LCL filter without damping. The damping frequency can be expressed the same as (6.21) with or without damping.

$$\omega_{res\_d} = \omega_{res\_wd} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \tag{6.21}$$

Thus, the inductor L_2 with damping can be derived from (6.20) and (6.21).

$$L_{2\_d} = \frac{9L_1 L_{2\_wd}}{4L_1 - 5L_{2\_wd}} \tag{6.22}$$

Combining (6.22) and (6.19), the inductor L_2 can be designed.

The passive resistor can be calculated as (6.23) from (Reznik *et al.*, 2014). The resonant frequency can be found as (6.21).

$$R_d = \frac{1}{3\omega_{res} C_f} \tag{6.23}$$

6.3.4 Design Verification of the LCL Inverter.

Since the switching frequency of the unipolar SPWM inverter is 100kHz, the "doubled" switching frequency 200kHz is the worst case to design. The attenuation requirements of the inverter at 200kHz can be summarized as Table 6.2. From the specifications, the filter should be designed based on 1kW 120Vrms AC as the worst case.

Table 6.2: Attenuation requirements at 200kHz for the sing-phase inverter.

System	Grid-tied	Standalone
1kW 120Vrms AC	-70.25 dB	-48.67 dB
3kW 240Vrms AC	-66.73 dB	-42.65 dB

Based on the specification and requirements, the LCL inverter is designed as following. (1) Choosing 40% allowed ripple $L_1 = 50uH$. (2) The capacitance $C_f = 8uF$ for the attenuation of the standalone mode. (3) By selecting the value of $L_2 =$

$15uH$ the condition (6.18) is fulfilled. (4) The damping resistance is 0.6Ω and the resonant frequency is 23kHz.

The design of the LCL inverter can be verified by the bodeplot of the grid-tied and standalone transfer function can be found in Figure 6.5 and Figure 6.6. Since the transfer function of the standalone mode is influence by its equivalent load as (6.8), the transfer function with full load, half load and 10% load are shown as Figure 6.6. Finally, the designed LCL filter can fulfil the requirement of 120V/240V dual mode operation.

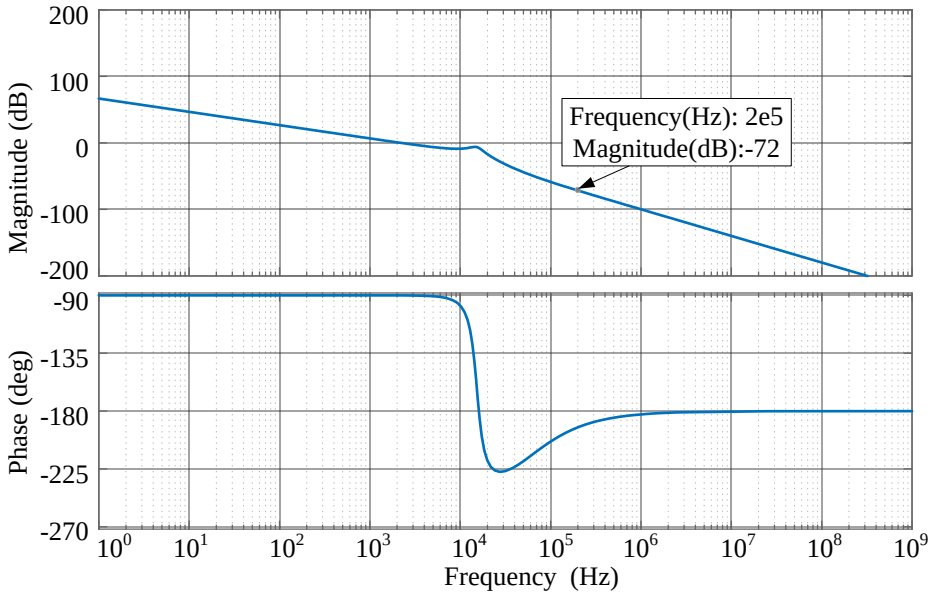


Figure 6.5: Bodeplot of grid-tied transfer function.

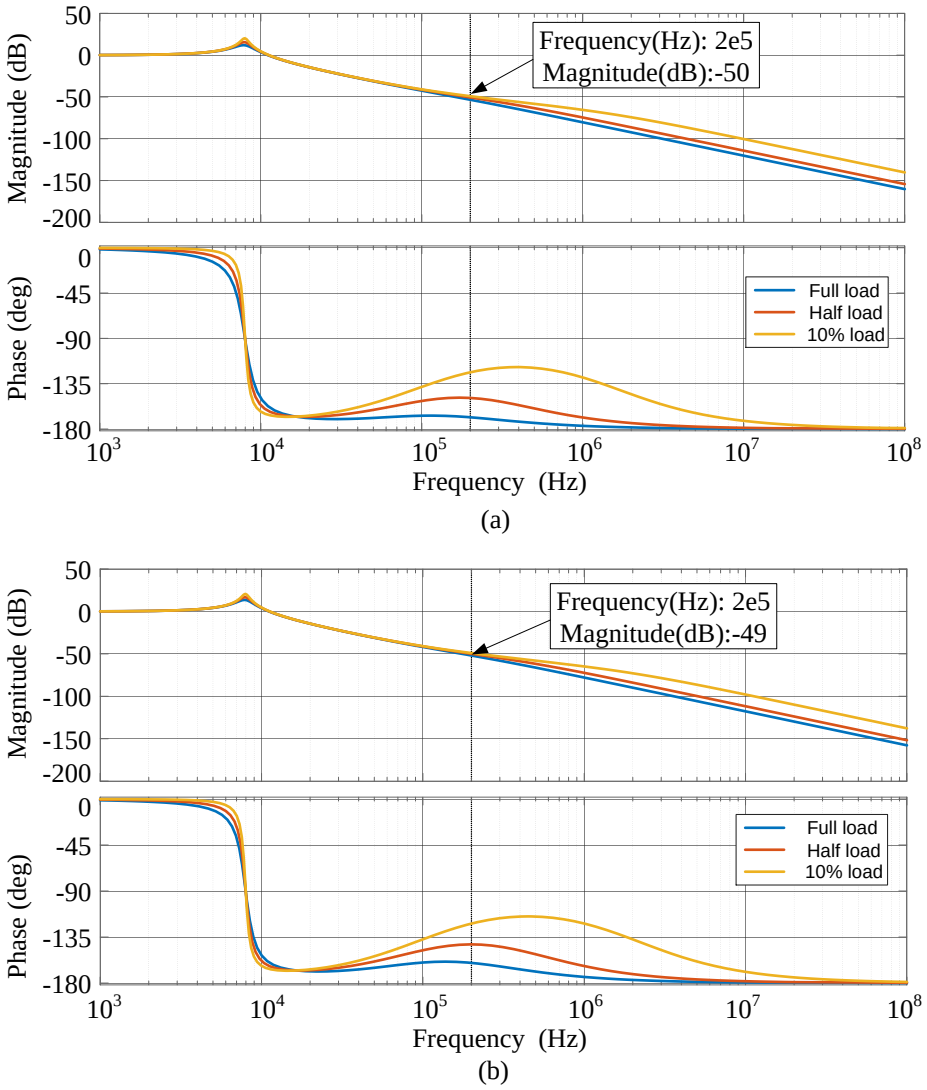


Figure 6.6: Bodeplot of standalone transfer function: (a) 120V case. (b) 240 case.

6.4 PR Controller Design for the LCL Inverter

The PR controller is utilized for the standalone and grid-tied operation to achieve high gain at the fundamental frequency.

6.4.1 Controller Design for the Grid-tied Mode

PR Controller for Grid-tied Mode

The design of the grid-tied PR controller is mainly followed by (Bao *et al.*, 2014). The schematic of the LCL inverter and controller diagram are shown as Figure 6.7.

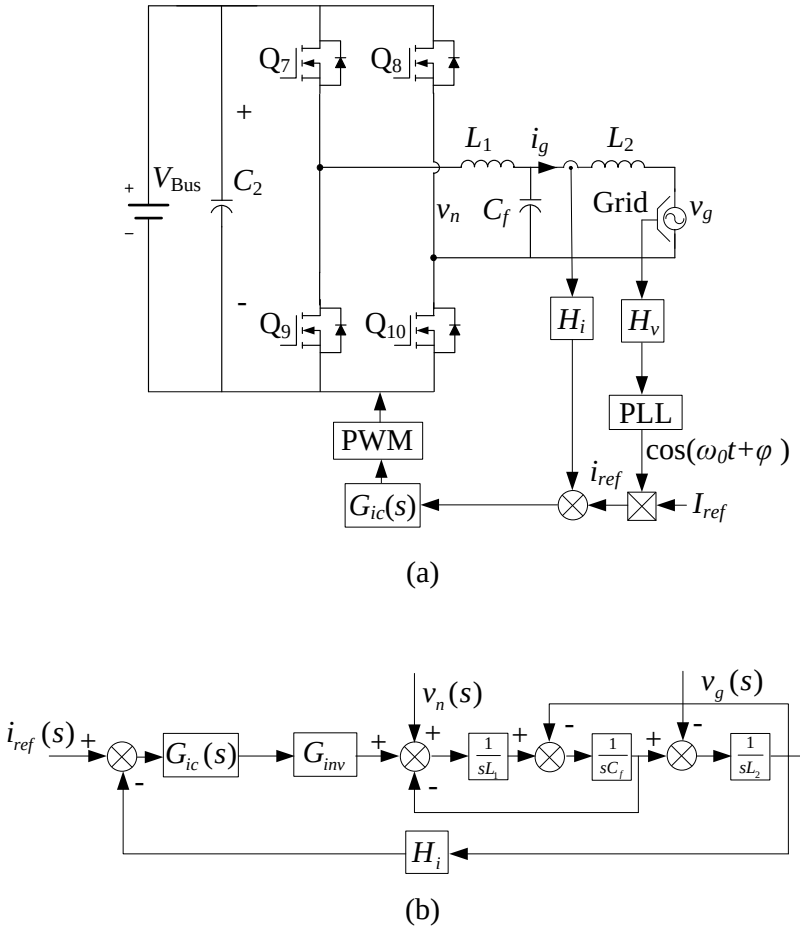


Figure 6.7: Grid-tied LCL inverter with controller: (a) Configuration of the LCL inverter with controller. (b) Control block diagram of the grid-tied LCL inverter.

The output current of the closed-loop LCL inverter is (6.24).

$$i_g(s) = \frac{1}{H_i}\frac{T_i(s)}{1+T_i(s)}i_{ref}(s) + \frac{G_{i_g v_{inv}}}{1+T_i(s)}v_n(s) - \frac{G_{i_g v_g}}{1+T_i(s)}v_g(s) \tag{6.24}$$

The $G_{ic}(s)$ represents the current PR controller for grid-tied mode. The transfer function of the LCL filter $G_{i_g v_{\mathrm{INV}}}(s)$ can be found as (6.7) and $G_{i_g v_g}(s)$ can be found as (6.8). The inverter gain G_{inv} can be expressed as the DC bus voltage value. The sensor gain H_v and H_i can be set as 1 for the following analysis, The open loop of the system can be expressed as $T_i(s) = G_{i_g v_{inv}}(s) G_{ic}(s) H_i G_{inv}$.The voltage harmonics of the H-bridge and the grid can be seen as disturbance $v_n(s)$ and $v_g(s)$.

From (6.24), the gain of the open loop transfer function at the fundamental frequency should be large enough so that the grid current can follow the current reference without steady-state error. Hence the resonant frequency is ω_0 of the PR controller to achieve large gain in the $T_i(s)$. The PR controller can be expressed as (6.25).

$$G_{ic}(s) = K_p + \frac{2K_r \omega_i s}{s^2 + 2\omega_i s + \omega_0^2} \tag{6.25}$$

From the analysis of the second term on the left side of (6.24), the high frequency switching harmonics in $v_n(s)$ can be suppressed by the open loop LCL filter $G_{i_g v_{\mathrm{INV}}}(s)$ however the closed-loop controller $G_{\mathrm{ic}}(s)$ should be designed to attenuate the low frequency harmonics in grid voltage $v_g(s)$ from the analysis of the third term on the left side of (6.24). In this section, the PLL and the grid voltage are assumed to be ideal. The PLL design and the harmonics of the grid voltage will be considered later on.

The PR controller can start with the crossover frequency of $T_i(s)$. The f_c should be larger than 25 times of the fundamental frequency f_0 to ensure enough gain at f_0 and suppress the harmonics caused by the non-ideal v_g while f_c should be less than one tenth of the switching frequency so that the switching harmonics can be

suppressed enough as (6.26).

$$25f_o < f_c < 0.1f_{sw} \tag{6.26}$$

To simplify the design procedure, some assumptions should be made based on the analysis of Figure 6.8. From Figure 6.8(a), the bodeplot of the LCL filter can be approximated as it of the inductor with the sum inductance of L_1 and L_2 from 0Hz to the resonant frequency of the LCL filter. From Figure 6.8(b), the bodeplot of the PR controller far away from its resonant frequency ω_0 can be assumed to be just a proportional controller K_p. The crossover frequency f_c is chosen as 2000Hz from (6.26). Since f_c is much larger than the resonant frequency of PR controller and smaller than the resonant frequency of LCL filter, the magnitude of the open loop at the crossover frequency is (6.27).

$$|T_i(j\omega_c)| = |G_{LCL} \cdot G_{PR} \cdot H \cdot G_{inv}| = \frac{1}{\omega_c \cdot (L_1 + L_2)} \cdot K_p \cdot H \cdot G_{inv} = 1 \tag{6.27}$$

Thus, K_p of the PR controller can be calculated from (6.28),

$$K_p = \frac{2\pi f_c(L_1 + L_2)}{H \cdot G_{inv}} \tag{6.28}$$

To achieve good compensation performance, the magnitude of open loop gain is selected larger than 80.

$$20\log_{10}|T_{f_0}| > 80 \tag{6.29}$$

Since the fundamental frequency, 60Hz, is much less than the designed resonant frequency of LCL filter, the LCL filter is assumed as the inductor filter for this

analysis.

$$K_r > \frac{10^4 \cdot 2\pi f_0 \cdot (L_1 + L_2)}{H \cdot G_{inv}} - K_p \tag{6.30}$$

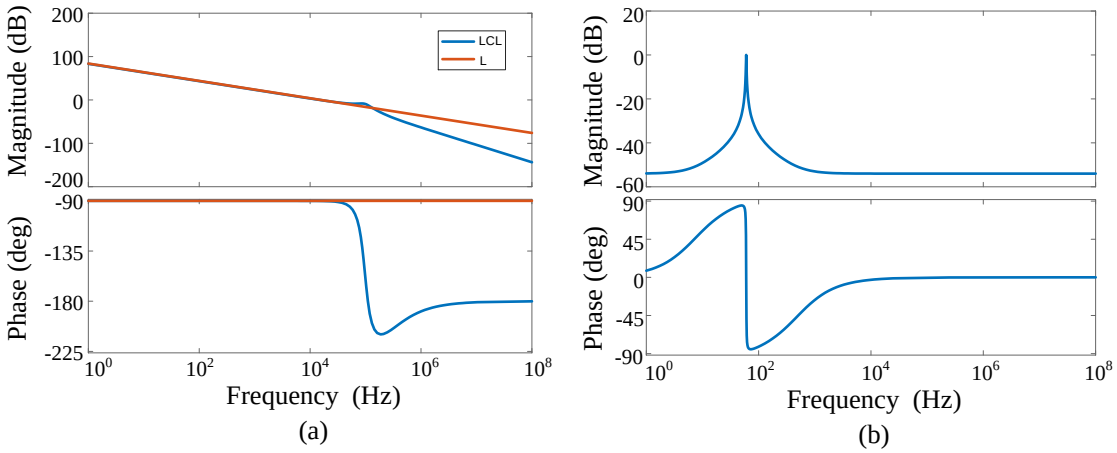


Figure 6.8: Examples for controller design: (a) Comparison between LCL and L filter. (b) Bodeplot of a PR controller.

To achieve a good dynamic performance, enough phase margin should be given.

$$PM = 180^o + \angle T_i \,|_{s=j2\pi f_c} \geq 45^o \tag{6.31}$$

The phase requirement of the current PR controller is

$$\angle G_{ic} \,|_{s=j2\pi f_c} = \arctan\left(\frac{2K_r\omega_i\omega_c \cdot (\omega_o^2 - \omega_c^2)}{K_p * [(\omega_o^2 - \omega_c^2)^2 + 4\omega_i^2\omega_c^2] + 4K_r\omega_i^2\omega_c^2}\right) \geq -45^o \tag{6.32}$$

Thus K_r can be selected by the conditions (6.30) and (6.32). Finally, the PR controller is designed by the parameters of the LCL filter: $K_p = 2e-3$; $K_r = 4$; $\omega_0 = 2\pi * 60$. The ω_i is chosen as $2\pi * 0.5$ allow frequency variable. The performance of the compensator can be found in Figure 6.9.

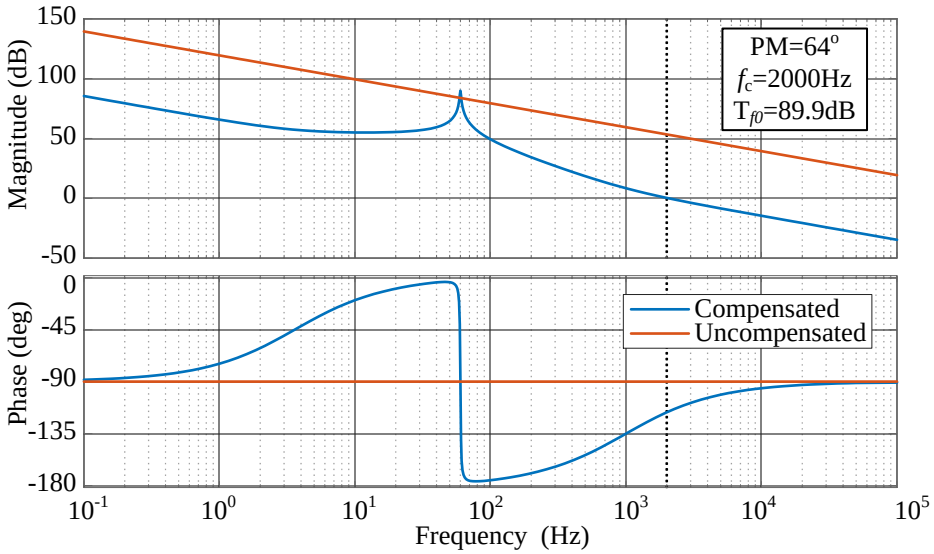


Figure 6.9: Bodeplot of the closed-loop grid-tied inverter.

PLL Design for the Grid-Tied Mode

A typical phase locked loop (PLL) is shown as Figure 6.10 which includes phase detect (PD), PI controller and voltage controller oscillator (V_{CO}). The measured grid voltage and the output of V_{CO} are as (6.33) and (6.34).

$$v = v_{grid}\sin(\theta_{in}) = v_{grid}\sin(\omega_{grid}t + \theta_{grid}) \tag{6.33}$$

$$v' = \cos(\omega_{\mathrm{PLL}}t + \theta_{\mathrm{PLL}}) \tag{6.34}$$

Thus the error is (6.35)

$$\varepsilon = \tfrac{v_{grid}}{2}[\sin((\omega_{grid} - \omega_{PLL})t + (\theta_{grid} - \theta_{PLL})) + \sin((\omega_{grid} + \omega_{PLL})t + (\theta_{grid} + \theta_{PLL}))] \tag{6.35}$$

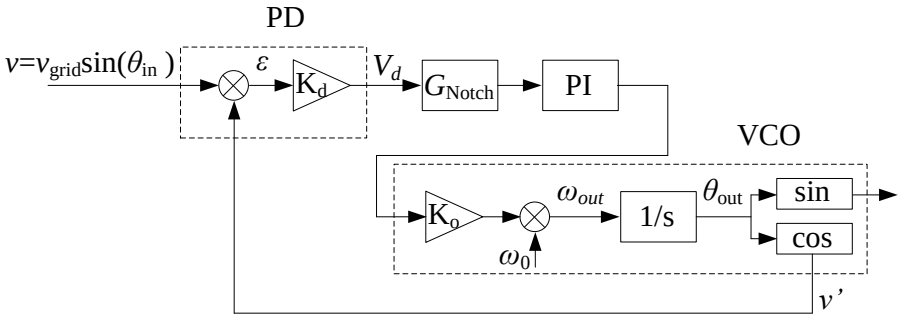


Figure 6.10: Phase locked loop basic structure.

The PI controller should be designed to filter out the twice frequency component of the error as well as to form a feedback control loop to reduce the locking steady-state error. Furthermore, a notch filter can be added to attenuate the twice frequency component as Figure 6.10. The PLL parameters can be designed by selecting the natural frequency and the damping ration of the closed loop transfer function $K_p = 166.6$ and $K_i = 27755.55$.

Multi-PR Controller for Non-Ideal Grid Voltage

From the analysis of (6.24), the PR controller should be designed to suppress the low frequency harmonics in grid voltage. In (Blaabjerg *et al.*, 2006), the harmonics compensator (HC) should be designed to compensate the third, fifth, seventh and nineth harmonics in the grid voltage as (6.36).

$$G_h(s) = \sum_{h=3,5,7,9} K_{ih} \frac{s}{s^2 + (\omega_0 \cdot h)^2} \tag{6.36}$$

The capabilities to attenuate the grid voltage harmonics can be extended by adding more harmonic compensation but it's limited by the computation burden

of the microcontroller as Figure 6.11. The HC design should not affect the dynamics of the main PR controller.

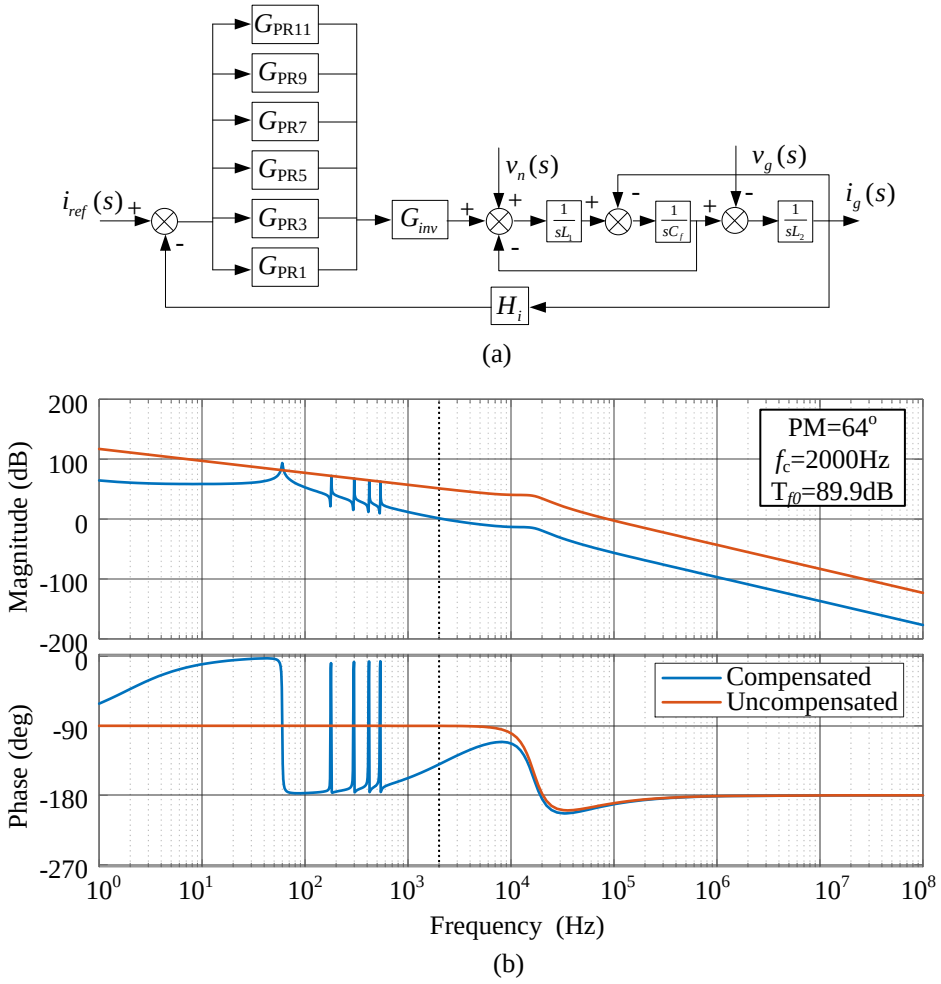


Figure 6.11: A PR controller with multiple HC: (a) Control block with multi-HC. (b) Bodeplot.

6.4.2 Controller Design for the Standalone Mode

v_n represents the voltage harmonics on the H-bridge of the inverter which is disturbance of the closed-loop controller. The control block of the standalone mode single-phase inverter can be found in Figure 6.12 where $G_{vc}(s)$ is the PR controller

for standalone mode, G_{INV} is the model of the inverter, $G_{v_g v_{inv}}(s)$ is the LCL filter transfer function as (6.10), H_v represents the feedback gain of the voltage sensor.

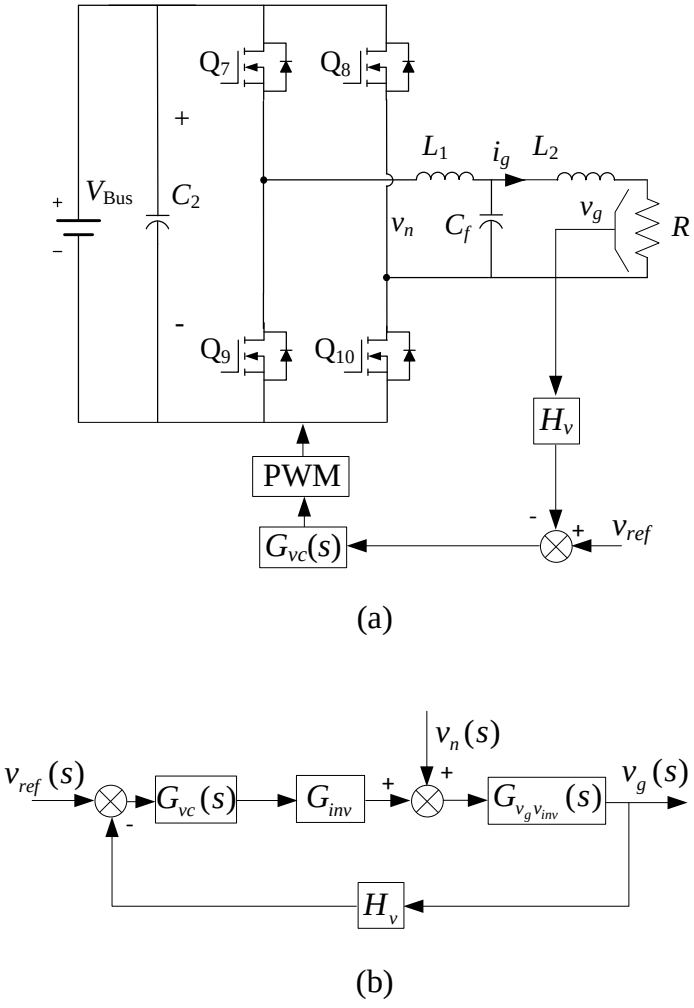


Figure 6.12: Standalone LCL inverter with controller. (a) Configuration of the LCL inverter with controller. (b) Control block diagram of the grid-tied LCL inverter.

Thus the open loop transfer function of the controller is (6.37).

$$T_v(s) = G_{vc}(s)G_{inv}G_{v_g v_{inv}}(s)H_v \tag{6.37}$$

Thus the output voltage of the standalone mode LCL inverter can be expressed as (6.38).

$$v_g(s) = \frac{1}{H_v}\frac{T_v(s)}{1+T_v(s)}v_{ref}(s) + \frac{G_{v_g v_{inv}}}{1+T_v(s)}v_n(s) \tag{6.38}$$

The PR controller can be expressed as (6.39).

$$G_{vc}(s) = K_p + \frac{2K_r\omega_i s}{s^2 + 2\omega_i s + \omega_0^2} \tag{6.39}$$

From Figure 6.13, for the frequency below the resonant frequency of the standalone mode LCL filter, the LCL filter can be approximate as LC filter with $L_2 = 0$ to simplify the design procedure. The crossover frequency of the open loop $T_v(s)$ should be designed less than the resonant frequency. The crossover frequency is chosen as 1000Hz for the standalone mode. The magnitude of the $T_v(j\omega_c)$ can be expressed by (6.40).

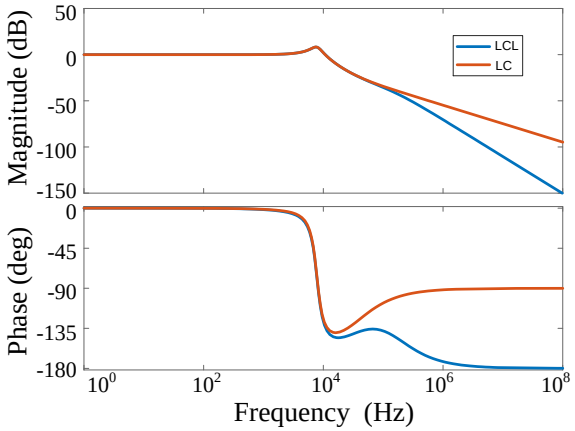


Figure 6.13: Comparison between LCL and L filter for standalone mode.

$$|T_v(j\omega_c)| = \left|G_{v_g v_{inv}}(j\omega_c)\cdot G_{PR}(j\omega_c)\cdot H\cdot G_{inv}\right| = 1 \tag{6.40}$$

The magnitude of the open loop gain at the fundamental frequency should be larger enough as (6.41).

$$20\log_{10}|T_v(j\omega_0)| > 50 \tag{6.41}$$

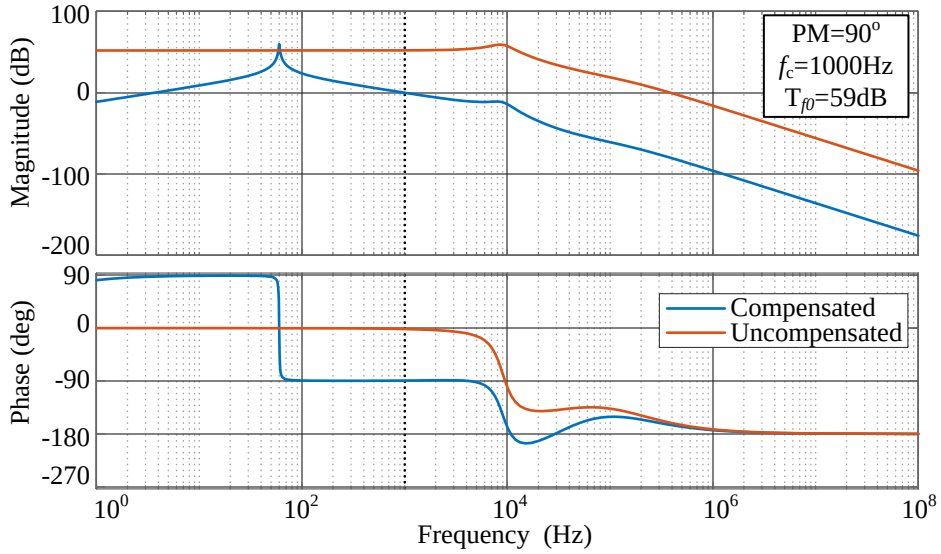


Figure 6.14: Bodeplot of the closed loop standalone inverter.

The large phase margin of the closed-loop controller should be obtained to achieve good dynamic performance as (6.42).

$$PM = 180^o + \angle T_v|_{s=j2\pi f_c} \geq 45^o \tag{6.42}$$

Based on the phase margin condition, the K_r is chosen at first then based on the (6.41), the K_p can be calculated. Based on (6.42), the Kp and Kr value can be verified. After the trial, the controller is designed as $K_p = 1e-4$, $K_r = 2.4$, $\omega_0 = 2\pi * 60$ and $\omega_i = 2\pi * 0.5$. The bodeplot is utilized to verify the compensator design as Figure 6.14.

6.5 Simulation and Experimental Results

The simulation and experimental results are utilized to verify the design of the LCL filter and PR controller. The summary of the parameters of the LCL single-phase inverter and PR controller are shown as Table 6.3 and Table 6.4.

Table 6.3: Parameters of the LCL filter.

Parameters	Value
Inverter-side inductor L_1	$50\mu H$
Grid-side inductor L_2	$18\mu H$
Capacitor C_f	$8\mu F$
Passive damping R_d	0.6Ω
Fundamental frequency f_0	$60Hz$
Switching frequency f_sw	$100kHz$

Table 6.4: Parameters of the PR controller.

Parameters	Standalone Value	Grid-tied Value
K_p	1e-4	2e-3
K_r	2.4	4
ω_0	$2\pi \times 60$	$2\pi \times 60$
ω_i	$2\pi \times 0.5$	$2\pi \times 0.5$
PLL	Value	
K_p	166.6	
K_i	27755.55	

6.5.1 Simulation Results

Standalone Mode

The simulation models are built as the parameters in Table 6.3 and Table 6.4 by MATLAB/Simulink. The simulation results can be found in Figure 6.15 and Figure 6.16.

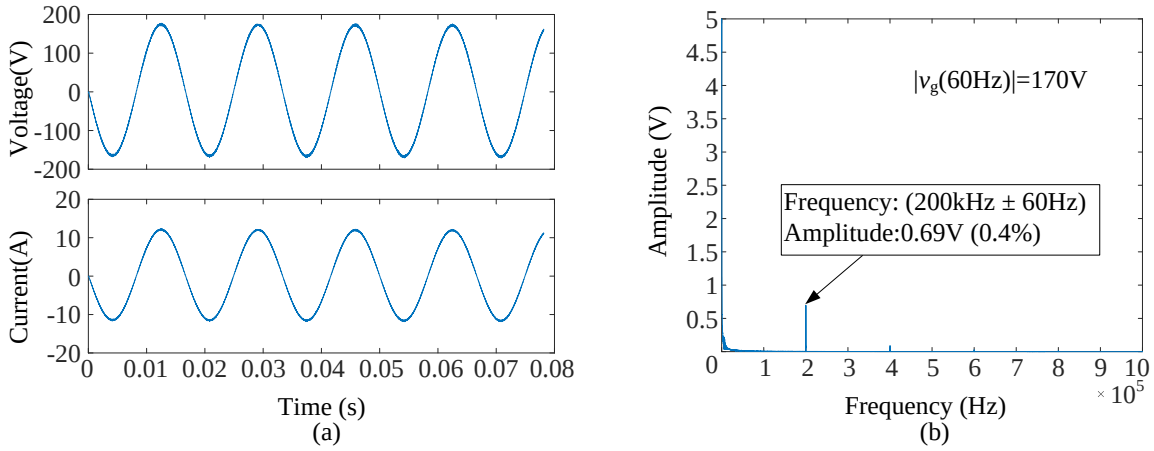


Figure 6.15: 1kW 120V standalone mode simulation results: (a) Waveforms. (b) FFT analysis of the output voltage.

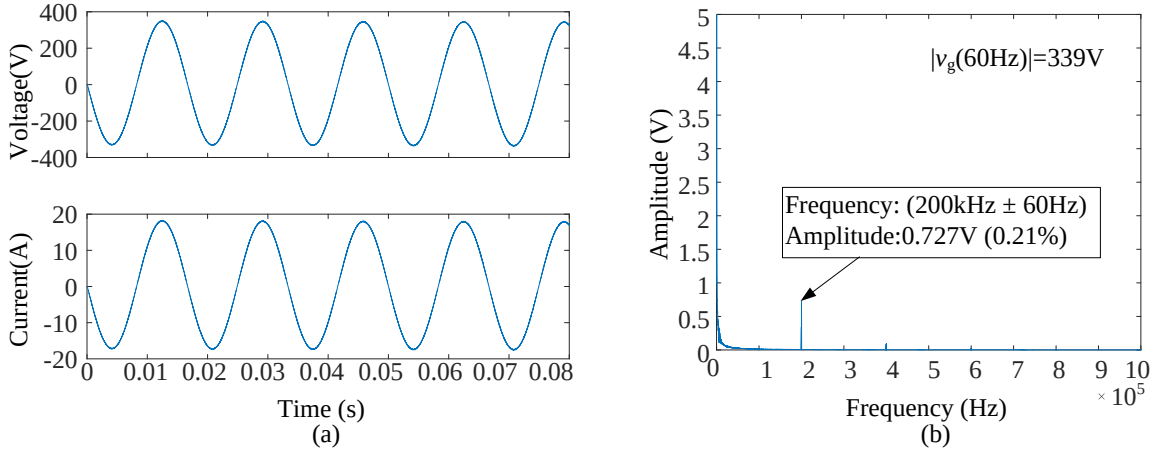


Figure 6.16: 3kW 240V standalone mode simulation results: (a) Waveforms. (b) FFT analysis of the output voltage.

Since the equivalent switching frequency, 200kHz, is far away from the fundamental frequency 60Hz, the most challenging attenuation performance is around 200kHz as analysis above. The harmonic distortion in Figure 6.15(b) and Figure 6.16(b) is less than 0.5% which fulfilled the EN 50160 requirements.

Grid-tied Mode

he grid-tied single-phase inverter simulation model is built assuming the grid voltage has no harmonics. The harmonic current of the 1kW 120V and 3kW 240V cases are less than 0.3%. THD of the 120V case and 240V as Figure 6.17(b) and Figure 6.18(b) are less than 5% and the current harmonics are less than the requirements of IEEE 1547. The simulation results verified the design of the LCL filter.

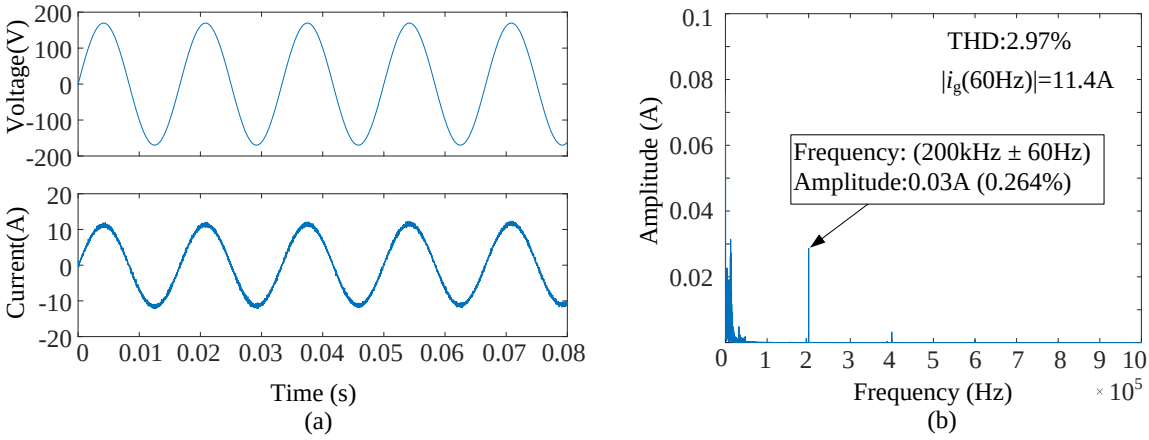


Figure 6.17: 1kW 120V grid-tied mode simulation results: (a) Waveforms. (b) FFT analysis of the grid current.

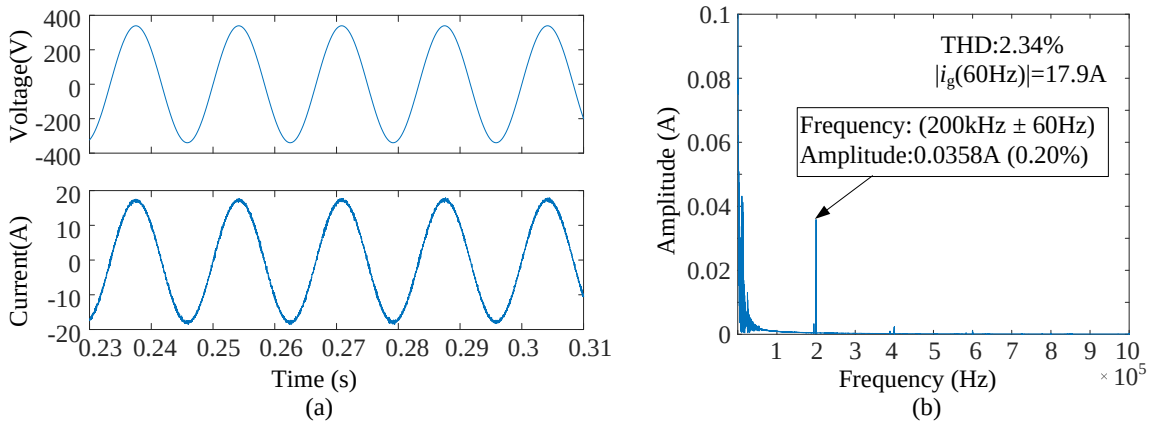
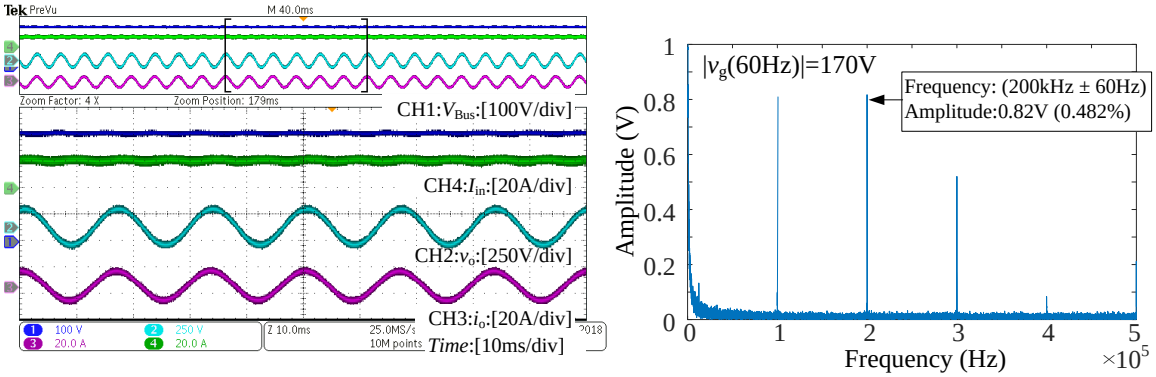


Figure 6.18: 3kW 240V grid-tied simulation results: (a) Waveforms. (b) FFT analysis of the grid current.

6.5.2 Experimental Results

Standalone Mode

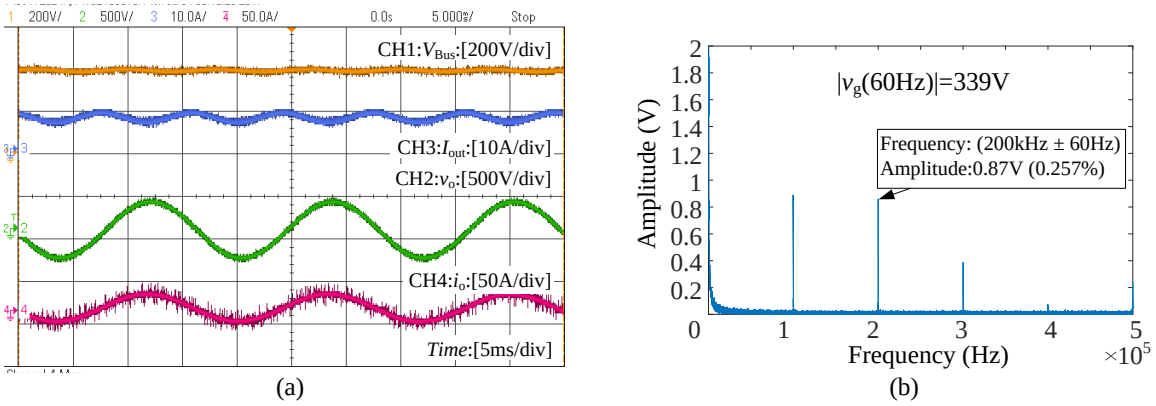
The experiment setup is made to verify the performance of the LCL filter and its PR controllers. Since the standalone mode inverter works as the voltage source to the resistor load, the quality of the voltage is interested. Analytically, the main harmonic of the single-phase inverter should be around 200kHz which is shown as Figure 6.19(b) and the harmonic percentage is 0.482% below the EN 50160's requirement. There is a high harmonic happening at 100kHz which is the switching frequency of the unipolar SPWM inverter because of the overshoot of the switches' turn on due to the stray inductance existing in the legs of the MOSFET.



(a) (b)

Figure 6.19: 1kW 120V standalone mode experimental results: (a) Waveforms. (b) FFT analysis of the output voltage.

The experimental results of the 3kW 240V case is shown as Figure 6.20. The output current waveform has distortion as Figure 6.20(a) because of the noise in the current probe. The voltage harmonics fulfilled the requirements. Also, the harmonics percentage is much less than it of the 120V case.



(a) (b)

Figure 6.20: 3kW 240V standalone mode experimental results: (a) Waveforms. (b) FFT analysis of the output voltage.

Since the efficiency of the inverter has no matter with the operation mode, the efficiency of the standalone mode is illustrated here as Figure 6.21. The efficiency of

the 120V case is around 92% at 1kW while the efficiency of the 240V case is around 96.5% at 3kW.

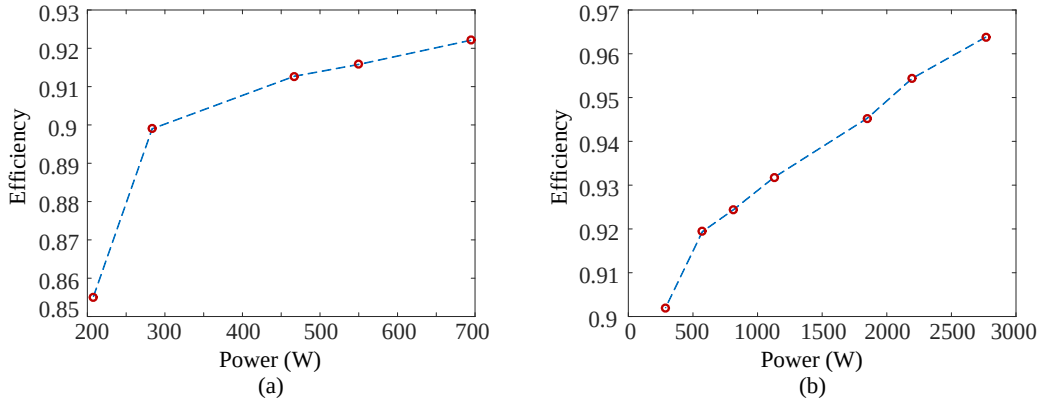


Figure 6.21: Efficiency map of the single-phase inverter: (a) 1kW 120V. (b) 3kW 240V

The system efficiency is also measured as Figure 6.22. For the system with 240V AC output, the maximum efficiency is around 90%. For the system with 120V AC output, the peak efficiency is around 86%. To further improve the overall system efficiency, lower switching frequency of the inverter can be utilized however a larger filter size will be resulted.

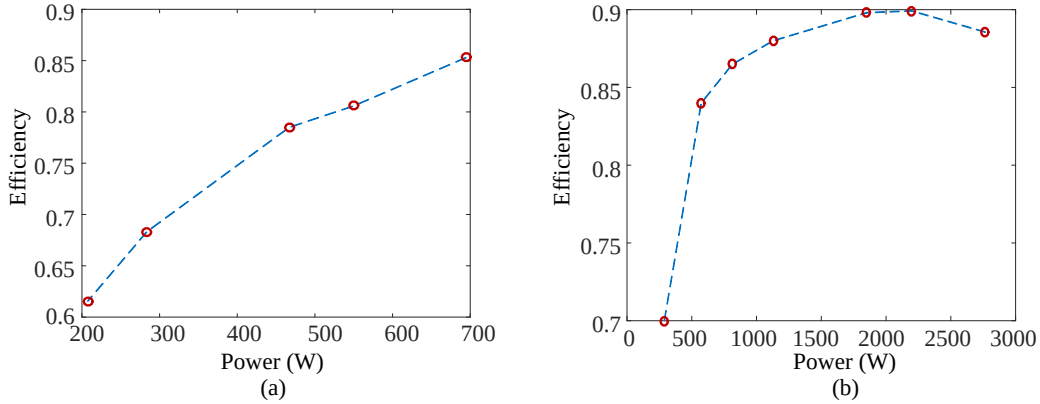


Figure 6.22: Efficiency map of the system: (a) 1kW 120V. (b) 3kW 240V

The dynamic performance is verified by full load to half load step and half load to full load step. Since the transfer function (22) and the controller (28) has no relationship with the output voltage level, Figure 6.23 can represent both 120V and 240V cases. An experiment with load steps is conduct by the 120V case as Figure 6.23. During the load transient, the output voltage vo has fast response and almost no overshoot as the CH2 in Figure 6.23.

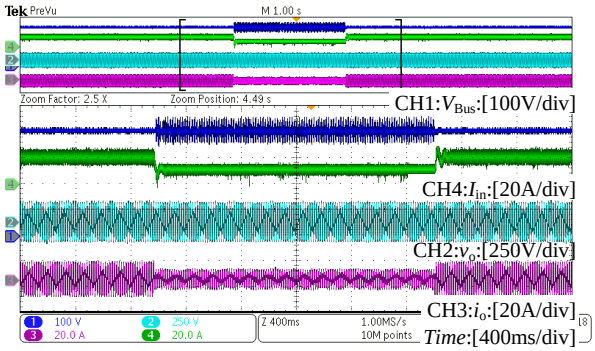


Figure 6.23: Dynamic performance of the PR controller.

Grid-Tied Mode

As analysis in Section 6.4 and the simulation results, the attenuation requirement for the 1kW 120V case is harsher than the 3kW 240V case. Thus the experimental results of the 1kW 120V case are illustrated to verify the performance of the LCL filter and the PR controller for the grid-tied operation. The low frequency of the grid voltage hamonics are shown as Figure 6.24. These relatively high low frequency harmonics will propagate into the output grid current as (). Multiple harmonic compensators (HCs) have to be added to solve this issue. The performance to suppress the harmonics caused by the low frequency grid voltage distortion is shown as Figure 6.25.

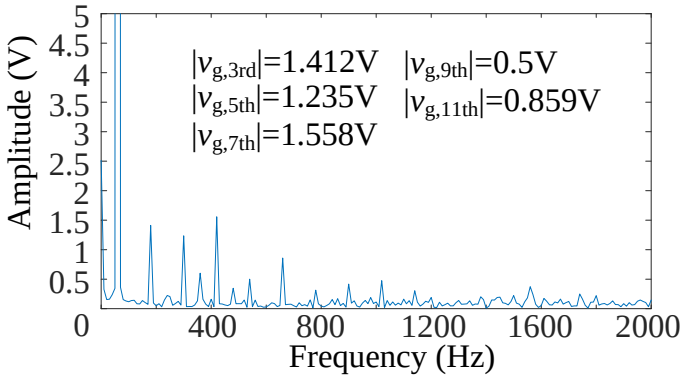


Figure 6.24: FFT analysis of a grid voltage in Marc

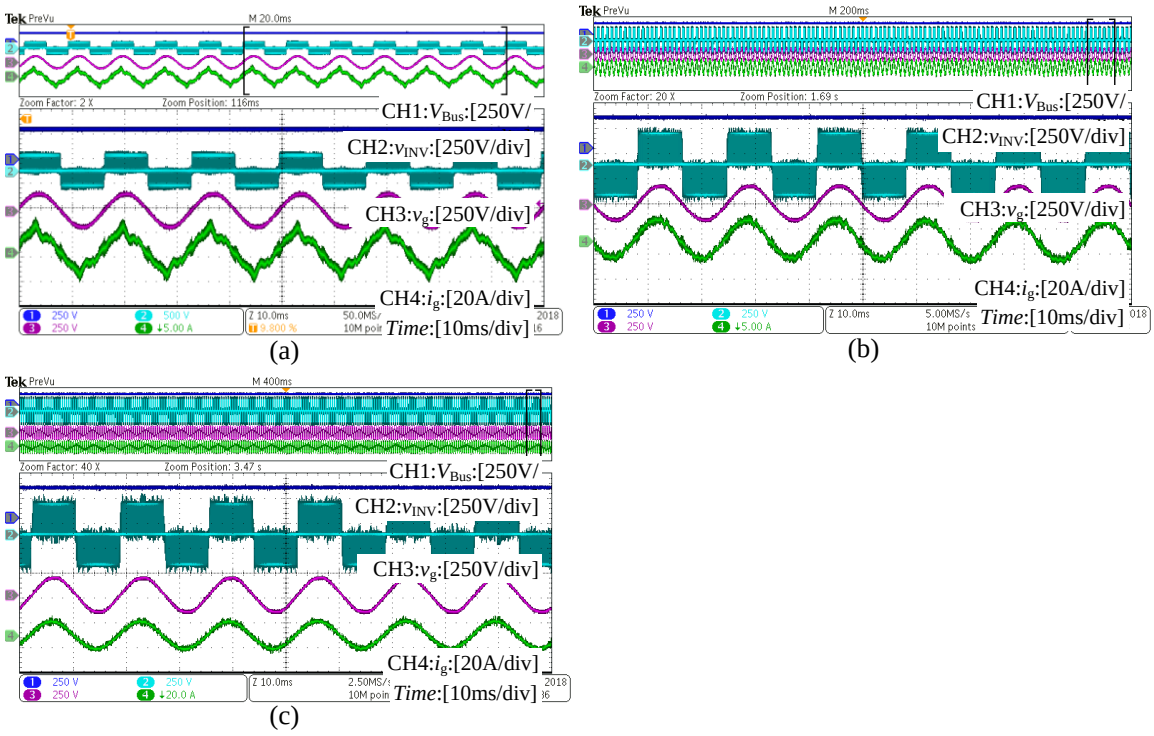


Figure 6.25: 1kW 120V grid-tied mode experimental waveforms: (a) Only PR controller. (b) PR controller with 3rd, 5th HCs. (c) PR controller with 3rd, 5th , 7th, 11th HCs.

The FFT analysis of the output grid current in Figure 6.25(c) is shown as Figure 6.26. THD of the grid-tied inverter is 4.6% for 1kW 120V case. No matter the

low frequency current harmonics caused by grid voltage distortion or high frequency current harmonics caused by inverter swathing characteristic are well suppressed by the LCL filter and PR controllers which fulfills the IEEE 1547 requirements.

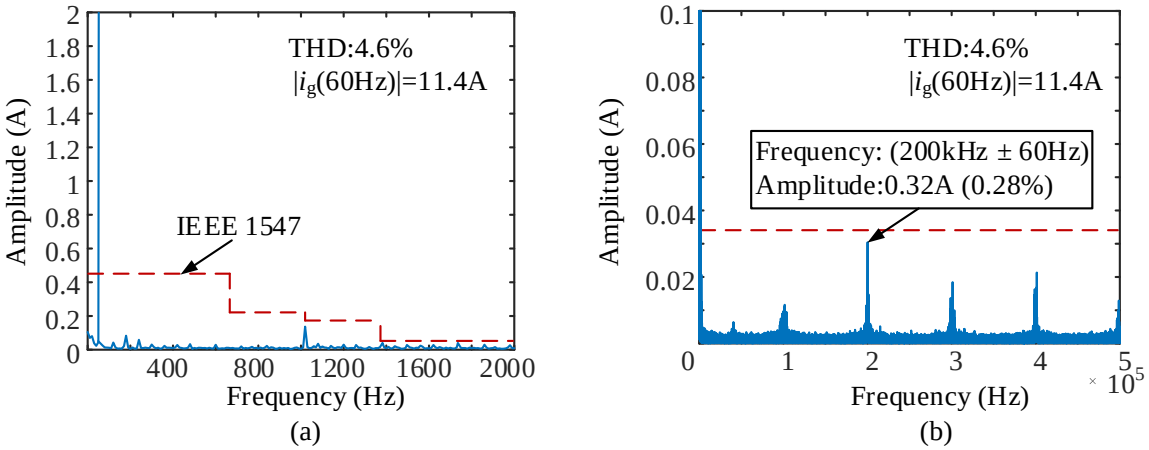


Figure 6.26: FFT analysis of the grid current for 1kW 120V grid-tied mode experimental results: (a) Low frequency. (b) High frequency.

The dynamic performance of the load step is shown as Figure 6.27. During the load transient, short setting time and low overshoot or undershoot are observed.

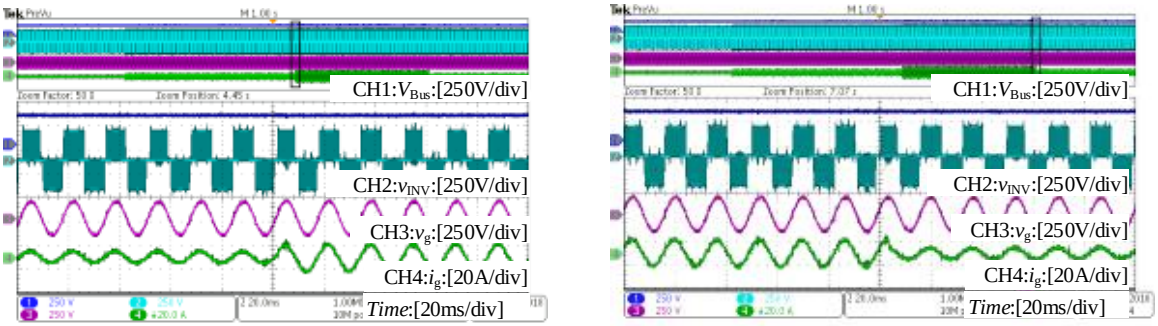


Figure 6.27: Dynamic perfornance of the grid-tied controller: (a) Half load to full load. (b) Full load to half load.

6.6 Conclusion

The dual standalone and grid-tied mode LCL single-phase inverter is designed for 1kW 120V and 3kW 240V with same hardware setup. A step-by-step design procedure of the LCL filter with passive damping is proposed for the 120V/240V dual mode inverter. The PR controllers are designed for the LCL inverter for standalone and grid-tied modes. The simulation and experimental results are provided to verify the performance of the LCL filter and PR controllers.

Chapter 7

Second Harmonic Current Reduction Strategy by Virtual Impedance in Two-Stage IBDGI with Three-Phase DAB Converter

7.1 Introducation

Isolated two-stage single-phase inverter is widely applied for the battery-to-grid application. The second harmonic current (SHC) existing in the front-end DC/DC converter is caused by the pulsating power of the single-phase inverter. The SHC will increase the battery's degradation and the component stress of the front-end converter. A SHC reduction method is proposed for the three-phase dual-active-bridge

(DAB) converter based two-stage single-phase inverter using a load current feedforward (LCFF) control. The proposed idea is to incorporate virtual impedance to the output impedance of the front-end converter. The easy-to-be-implemented method doesn't need to modify the original voltage closed-loop controller and suppress SHC while keep good dynamic performance. As the first step of analysis, the small-signal model of the three-phase DAB converter is provided and verified by its step response. The parameter sensitivity analysis is proposed to demonstrate that the SHC can be well suppressed within ±20% parameter error of the feedforward control. Finally, a 1kW experiment setup is built to verify the performance of the proposed SHC reduction method.

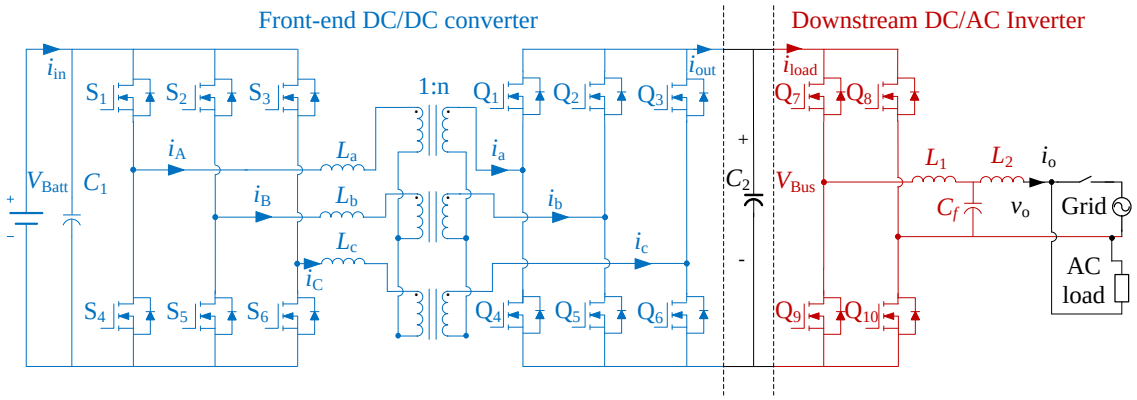


Figure 7.1: A three-phase DAB based IBDGI with downstream single-phase inverter.

This chapter proposed a SHC suppressing method by LCFF control to add virtual impedance to the output impedance of the front-end three-phase DAB converter. Also this method can also be applied for the system with front-end single-phase DAB converter. The proposed method is to increase the original output impedance at 2fo to the desired output impedance for SHC reduction purpose. Since the output of LCFF path is phase-shift not voltage reference, no requirement of the controller's

bandwidth is needed which is different from (Wang and Ruan, 2016) thus this method is quite easy to be implemented. The contributions of this chapter are: (1) a SHC reduction method based on virtual impedance perspective is proposed for the front-end three-phase DAB converter by adding a LCFF path; (2) the small-signal model of the three-phase DAB converter is provided and verified; (3) the parameter sensitivity analysis of the SHC reduction method is provided. The organization of this chapter is as follows. In Section 7.2, the small-signal model of the three-phase DAB converter is provided. Two PI controllers are designed as benchmarks of further research. Then the small-signal model is verified by the simulation and experimental results. In Section 7.3, a virtual-impedance-based approach by adding a LCFF path is proposed for the front-end DAB converter based system. The parameter sensitivity analysis of the proposed method is provided. In Section 7.4, the simulation and experimental results are provided to verify the proposed method. Finally, Section 7.5 concludes the findings and contributions of the chapter.

7.2 Small-Signal Modeling and PI Controller Design for Three-Phase DAB Converter

7.2.1 Mechanism of SHC in the System.

From (2.5), there is a sinusoidal current with twice the fundamental frequency $2f_{\mathrm{o}}$, and as high amplitude as the DC component. To the front-end DC/DC converter, the downstream inverter is simplified as a resistor in parallel with a sinusoidal current source based on (2.5) in Figure 7.2. The so-called "second-harmonic-current" (SHC) is supposed to be absorbed by the DC bus capacitor bank. The extreme example is

that there is no variation in DC bus voltage with a high bandwidth voltage controller then no energy will be storage in DC bus capacitor bank based on $E = 1/2 \cdot C\Delta V^2$. The SHC will flow through the switches and transformer of the DAB converter finally to the input battery source. It will increase the hardware current stress. Moreover, the input current i_{in} including second order harmonics which also accelerate battery aging supposing the capacitors on the battery side C_1 is not increased. Thus the SHC should be suppressed.

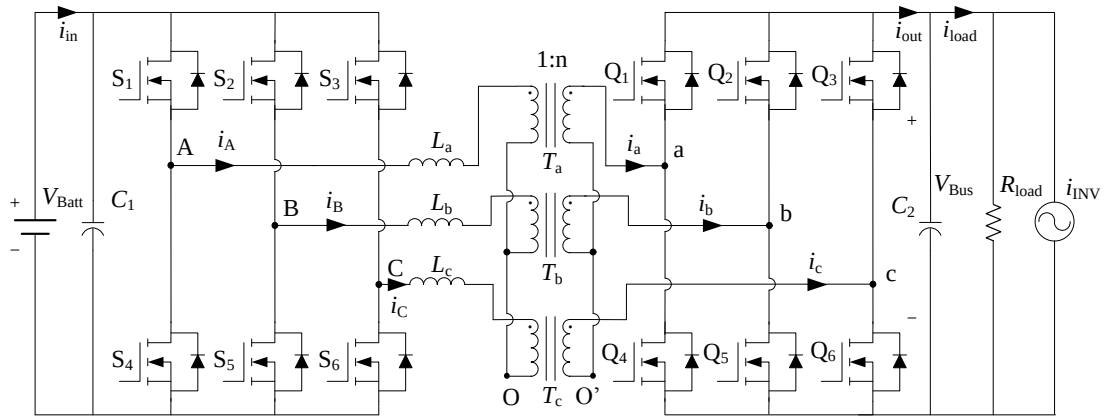


Figure 7.2: Simplified topology of the system.

7.2.2 The Small-Signal Model of the Three-Phase DAB Converter.

The performance of the SHC reduction method highly depends on the accuracy of the model of the system. Thus the small-signal model should be derived at the first step of the analysis. The fundamental waveforms of the three-phase DAB converter with simple-phase-shift (SPS) modulation can be found in Figure 2.5. There are two available operation modes where the phase shift range are $0-\pi/3$ and $\pi/3-2\pi/3$. In this work, we define the battery connected side is the primary side while the DC-bus

connected side is the secondary side. Based on the symmetric operation, the operation of Phase A is analyzed. By applying a phase shift ϕ between the primary side and the secondary side switches, the voltage difference across the leakage inductance of the transformer will be produced. It will induce the current go through the transformer thus the power can be transmitted from the primary side to the secondary side or the other side around. Since the back-flow power ratio highlighted by grey area in p_{pri} of Figure 2.5 in the operation mode $\pi/3 < \phi < 2\pi/3$ is more than $0 < \phi < \pi/3$ (De Doncker *et al.*, 1991). Thus the three-phase DAB converter operated in the $0 < \phi < \pi/3$ range is focused in this chapter and its transmission power can be expressed during $0 < \phi < \pi/3$ as (7.1).

$$P = -\frac{V_{\text{Batt}} V_{\text{Bus}} \phi}{n L_{\text{k}} \omega} (\frac{2}{3} - \frac{\phi}{2\pi}) \tag{7.1}$$

An average model of the DAB converter can be derived as Figure 7.3 by analysis of the operation waveforms. To simplify the analysis, first order model can be achieved by only considering DC bus capacitors C_2. The input current i_{in} and output current i_{out} is averaged during one switching period as (7.2) and (7.3).

$$\langle i_{\text{in}} \rangle = \frac{6}{T_s} \int_0^{\frac{T_s}{6}} i_{\text{in}}(t) dt = -\frac{\phi V_{\text{Bus}} (3\phi - 4\pi)}{6 n L_{\text{k}} \pi \omega} \tag{7.2}$$

$$\langle i_{\text{out}} \rangle = \frac{6}{T_s} \int_0^{\frac{T_s}{6}} i_{out}(t) dt = -\frac{\phi V_{\text{Batt}} (3\phi - 4\pi)}{6 n L_{\text{k}} \pi \omega} \tag{7.3}$$

where the turn ratio of the transformers n, leakage inductance L_k of the transformer and the switching angular frequency $\omega = 2\pi f$.

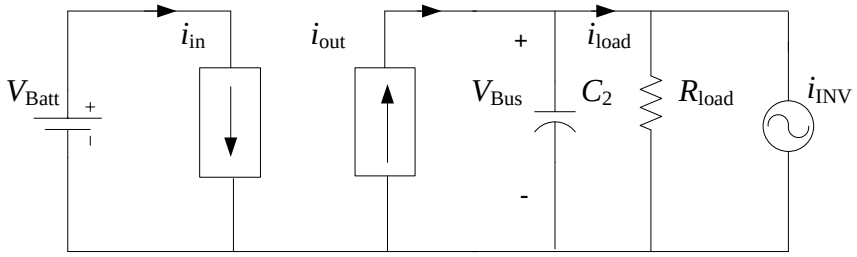


Figure 7.3: Averaged model of the three-phase DAB converter.

Based on the current relationship,

$$\langle i_{\text{out}} \rangle = C_2 \frac{dV_{\text{Bus}}}{dt} + \frac{V_{\text{Bus}}}{R_{\text{load}}} + i_{\text{INV}} \tag{7.4}$$

Rearrange the (7.2),

$$\frac{d\langle V_{\text{Bus}} \rangle}{dt} = -\frac{1}{C_2 R_{\text{load}}} \langle V_{\text{Bus}} \rangle + \frac{1}{C_2} \langle i_{\text{out}} \rangle - \frac{i_{\text{INV}}}{C_2} \tag{7.5}$$

Based on the perturbation and linearizion concept in (Erickson and Maksimovic, 2001), small ac variations are superimposed into the quiescent value $\langle V_{\text{Bus}} \rangle = V_{\text{Bus0}} + \hat{V}_{\text{Bus}}$, $\langle \phi \rangle = \phi_0 + \hat{\phi}$ and $\langle i_{\text{INV}} \rangle = i_{\text{INV0}} + \hat{i}_{\text{INV}}$. Then the small-signal model can be derived as following.

$$\frac{d\hat{V}_{\text{Bus}}}{dt} = -\frac{1}{R_{\text{load}} C_2} \cdot \hat{V}_{\text{Bus}} + \begin{bmatrix} -\frac{1}{C_2} & -\frac{6\phi_0 - 4\pi}{6 C_2 n L_{\text{k}} \pi \omega} V_{\text{Batt}} \end{bmatrix} \begin{bmatrix} \hat{i}_{\text{INV}} \\ \hat{\phi} \end{bmatrix} \tag{7.6}$$

The output impedance and phase-shift to output voltage transfer function can be found as following.

$$G_{vi}(s) \Big|_{\hat{\phi}(s)=0} = Z_{\text{o\_o}} = \frac{v_{\text{Bus}}(s)}{i_{\text{INV}}(s)} = -\frac{R_{\text{load}}}{R_{\text{load}} C_2 s + 1} \tag{7.7}$$

$$G_{v\phi}(s)\Big|_{\hat{i}_{\mathrm{INV}}(s)=0} = \frac{v_{\mathrm{Bus}}(s)}{\phi(s)} = -\frac{R_{\mathrm{load}}V_{\mathrm{Batt}}(3\phi_0 - 2\pi)}{3L_{\mathrm{k}}n\omega\pi(R_{\mathrm{load}}C_2 s + 1)} \tag{7.8}$$

The static phase shift ϕ_0 can be calculated from (6). The basic control block of the three-phase DAB converter with a voltage close-loop controller is illustrated as Figure 7.4, where the compensator is represented by $G_c(s)$ and $H(s)$ is the voltage sensor gain.

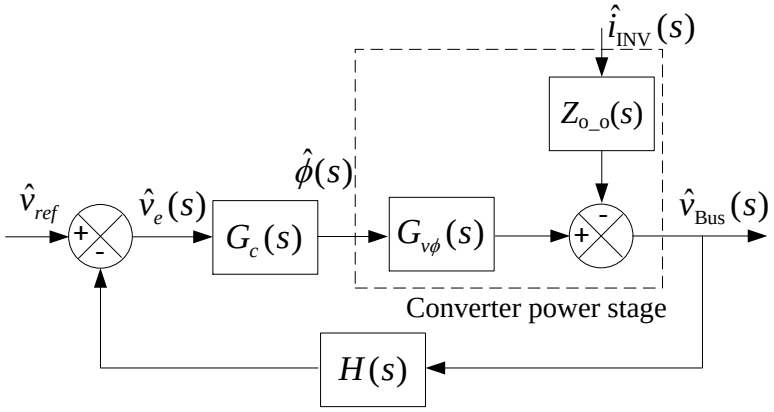


Figure 7.4: Basic control block of three-phase DAB converter.

7.2.3 PI Controllers and Small-Signal Model Verification

The three-phase DAB converter is designed based on Section 3. The parameters of the three-phase DAB converter are summarized as Table 7.1. The switching frequency is 100kHz as tradeoff between efficiency and power density of the system. To achieve 0.5% of DC voltage variation, the DC bus capacitance is chosen as 2mF. The DC bus capacitor bank design can be found in Section 5.2.

Table 7.1: Specifications of the proposed IBDGI.

Parameters	Value
Input battery voltage V_{in}	48V
Output voltage on DC bus V_{out}	400V
Transformer turn ratio n	1:8
Transformer leakage inductance on the secondary,side L_k	$33\mu H$
Input capacitor C_1	$80\mu F$
Output capacitor C_2	2mF
Switching frequency f	100kHz
Equivalent resistor laod R_{load}	160Ω

Based on the (7.7) and (7.8), the bode plot of the transfer functions can be plotted in Figure 7.5.

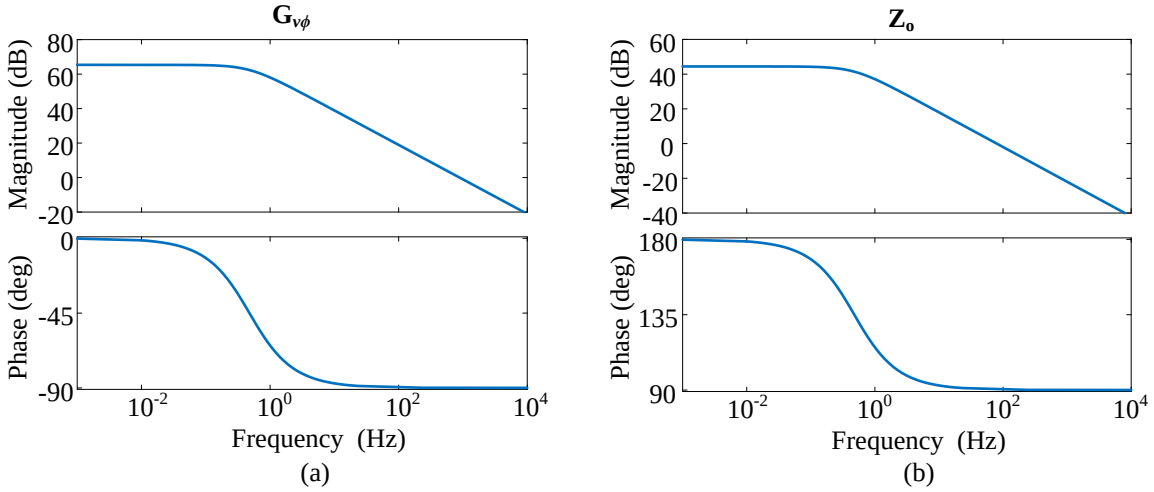


Figure 7.5: Bodeplot of transfer function: (a) phase-shift to voltage transfer function. (b) Output impedance of the front-end converter.

To compare with the method in (Wang and Ruan, 2016), a PI controller is designed

with the cross-frequency between 0Hz and 120Hz however it's not small enough to reject the SHC so the case with this PI set is called as "Fast PI". On the other hand, another PI controller is design as benchmark with much lower cross-frequency than 120Hz to achieve SHC reduction which is called as "Slow PI" in the rest of the chapter. These two sets of PI controller are designed and their bodeplots are shown as Figure 7.6 where the "Slow PI" controller with $K_p = 6.6e-3$, $K_i = 0.3$ has as small crossover frequency as 8Hz while the "Fast PI" controller with $K_p = 3e-2$, $K_i = 3$ has a higher crossover frequency as 30.25Hz.

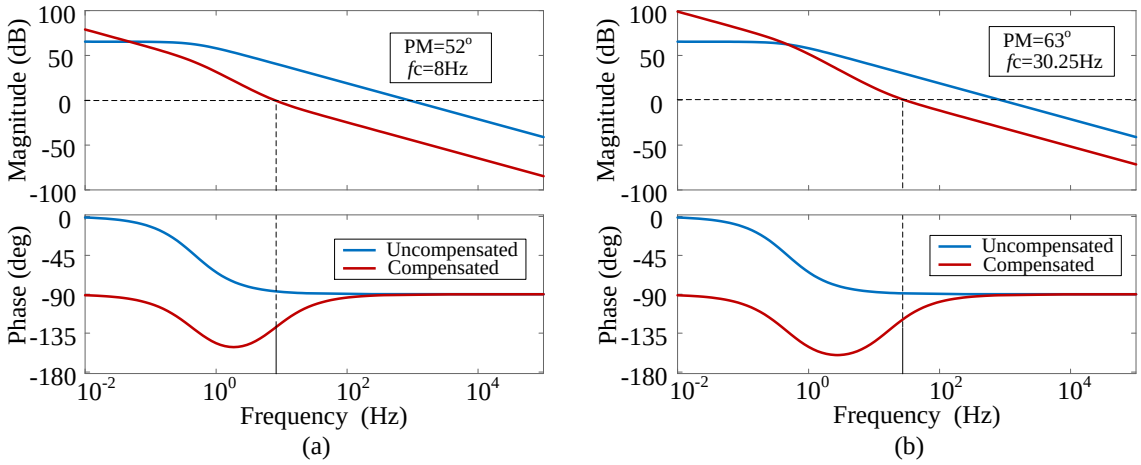


Figure 7.6: Bodeplot of the open-loop and close-loop system: (a) Slow PI case with $K_p = 6.6e-3$, $K_i = 0.3$. (b) Fast PI case with $K_p = 3e-2$, $K_i = 3$.

The step response is utilized to verify the small-signal model. The simulation results are shown as Figure 7.7. At 0 time, a step response from 400V to 410V is given to the voltage reference.

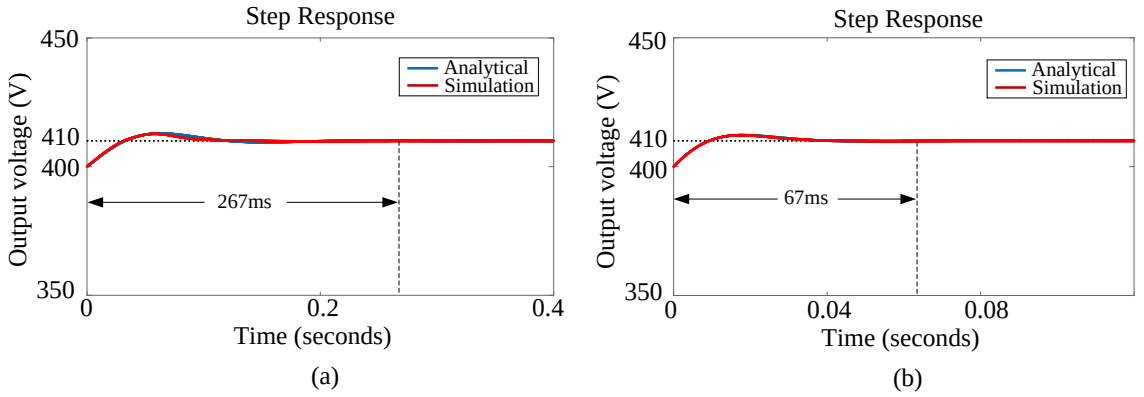


Figure 7.7: Step response of the controller comparison between analytical and simulation results: (a) Slow PI case. (b) Fast PI case.

The experimental results of the step response are also utilized to verify the small-signal model shown as following.

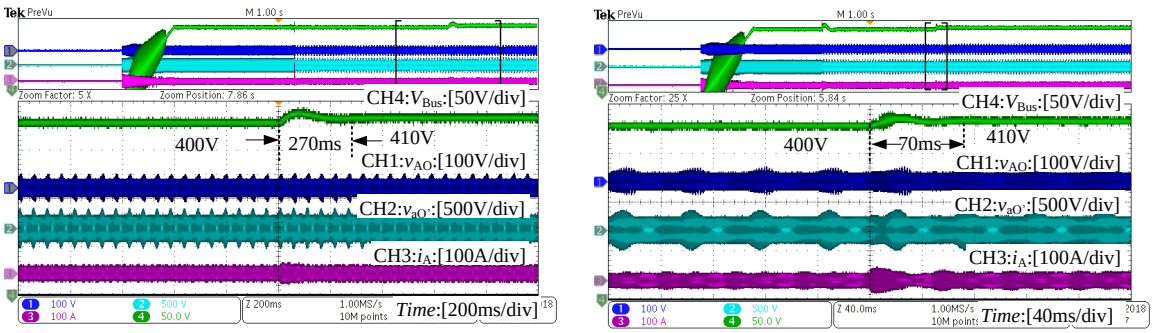


Figure 7.8: Experimental results of step response from 400V to 410V: (a) Slow PI case. (b) Fast PI case.

The step response with slow PI and fast PI controllers of the simulation and experimental results match the analytical results very well. Thus, the small-signal model is accurate enough for the following analysis.

7.3 SHC Reduction Strategy Based on Virtual Impedance Concept

7.3.1 SHC Problem from the Perspective of Output Impedance

The existing SHC problem can be viewed from the perspective of output impedance in Figure 7.9 (a). Z_c is the output impedance of the front-end converter at the static operation point with equivalent resistor R_{load}. Z_c is formed by the impedance of the DC bus capacitor Z_{capa} and the output impedance of the rest of the converter Z_{DAB}. With open loop, the output impedance Z_c equal to Z_{o_o} as (7.7).

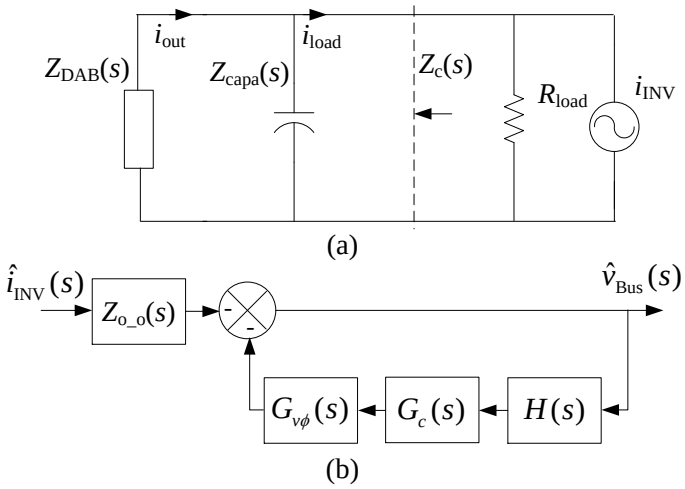


Figure 7.9: Equivalent circuit from output impedance view: (a) Equivalent circuit. (b) Control block with virtual impedance.

Ideally, no SHC passing through the DAB converter means all the sinusoidal current is buffered by the DC bus capacitor in Figure 7.9 (a). It requires the output impedance $Z_{\text{DAB}}(j2\omega_0)$ at $2f_0$ is much higher than the impedance $Z_{\text{CAPA}}(j2\omega_0)$ at $2f_0$.

At the same time Z_{DAB} at 0Hz is much smaller than the impedance Z_{CAPA} at 0Hz which means better load current disturbance rejection at steady-state. Since we can't change the impedance of capacitor Z_{CAPA}, the SHC reduction problem is transformed to how to increase the impedance of Z_{DAB} at $2f_0$. And the higher $Z_{\mathrm{DAB}}(j2\omega_0)$, the better SHC reduction performance.

The output impedance of the closed-loop three-phase DAB converter can be derived from Figure 7.4 as Figure 7.9 (b) supposing the voltage reference equals to 0.

Thus the close-loop output impedance of the converter can be expressed as

$$Z_{\mathrm{c}}(s) = -Z_{o\_o}(s)\frac{1}{1 + H(s)G_c(s)G_{v\phi}(s)} \tag{7.9}$$

Since the DAB converter is connect in parallel with the capacitor, $Z_{\mathrm{c}}(s) = Z_{\mathrm{DAB}}(s) \,\|Z_{\mathrm{Capa}}\,(s)$, as Figure 7.9 (b), then the close-loop output impedance of the DAB converter is

$$Z_{\mathrm{DAB}}(s) = \frac{Z_{\mathrm{c}}(s)Z_{\mathrm{Capa}}(s)}{Z_{\mathrm{Capa}}(s) - Z_{\mathrm{c}}(s)} = -\frac{Z_{\mathrm{o\_o}}(s)Z_{\mathrm{Capa}}(s)}{Z_{\mathrm{Capa}}(s) + Z_{\mathrm{Capa}}(s)H(s)G_c(s)G_{v\phi}(s) + Z_{\mathrm{o\_o}}(s)} \tag{7.10}$$

The output impedance of the converter is plotted as Figure 7.10.

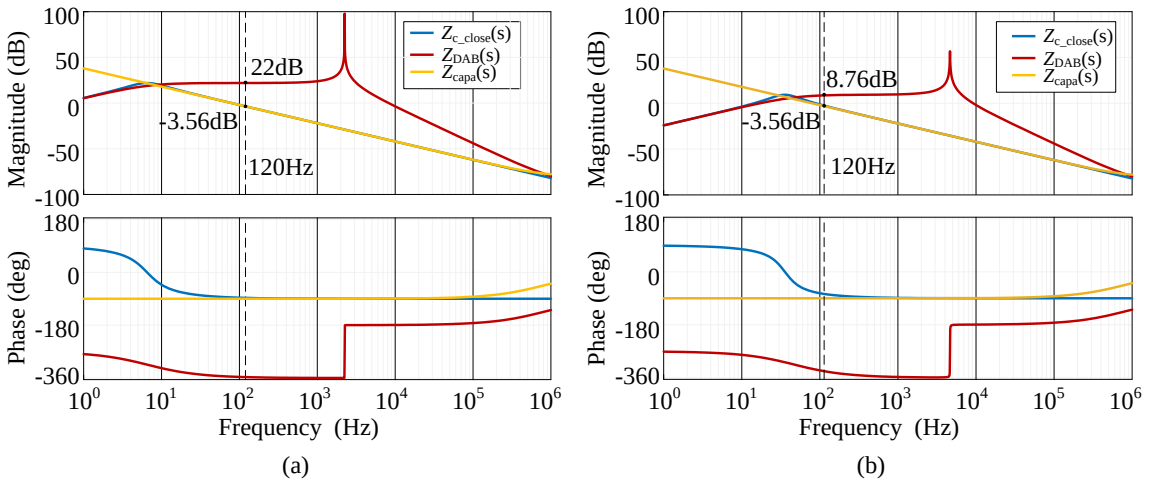


Figure 7.10: Closed-loop output impedance comparison: (a) Slow PI case. (b) Fast PI case.

From the Figure 7.10, the impedance $Z_{\mathrm{DAB}}(j2\omega_0)$ of the slow PI case is higher than the fast PI case and they are all higher than the $Z_{\mathrm{CAPA}}(j2\omega_0)$ which means the SHC reduction performance is better with the low crossover frequency than it with high crossover frequency. It matches analysis in the (Shi *et al.*, 2016). Also the output impedance of the converter $Z_{\mathrm{c}}(0\mathrm{Hz})$ of slow PI case is higher than it with fast PI case then a poor dynamic performance during load change transient will be expected with slow PI.

7.3.2 SHC Reduction Method based on Virtual impedance

To suppress the SHC as well as not sacrifice the dynamic performance of the system, the output impedance $Z_{\mathrm{DAB}}(j2\omega_0)$ should be increased but the impedance at other frequency should keep unchanged. From Figure 7.9 (b), virtual impedance including a load current feedforward path with a bandpass filter (BPF) with $2f_0$ characteristic frequency can be added in series with the open-loop output impedance Z_{o_o} as Figure

7.11.

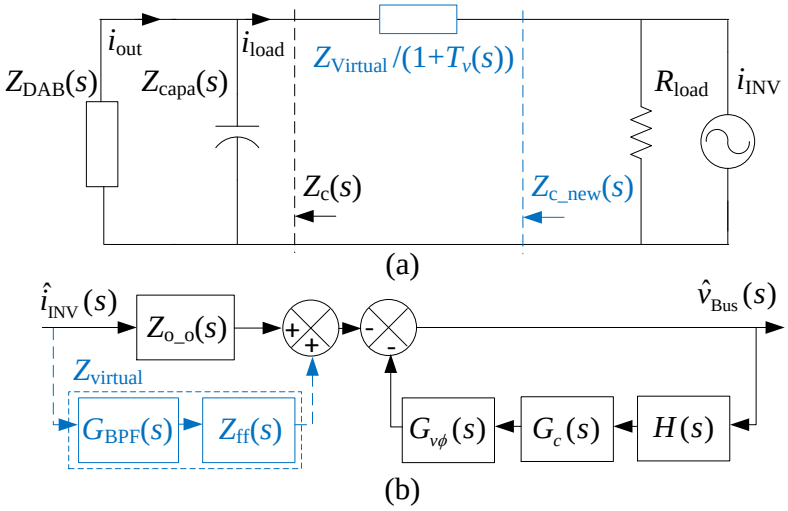


Figure 7.11: Illustration of the virtual impedance idea: (a) Equivalent circuit. (b) Control block with virtual impedance.

Thus the new output impedance of the closed-loop converter can be derived as

$$Z_{\text{c\_new}}(s) = -[Z_{o\_o}(s) + Z_{ff}(s) \cdot G_{\text{BPF}}(s)] \frac{1}{1 + H(s)G_c(s)G_{v\phi}(s)} \tag{7.11}$$

From (7.10), the output impedance of the DAB converter with LCFF is

$$\begin{aligned} Z_{\text{DAB\_new}}(s) &= \frac{Z_{\text{c\_new}}(s)Z_{\text{Capa}}(s)}{Z_{\text{Capa}}(s) - Z_{\text{c\_new}}(s)} \\ &= -\frac{(Z_{ff}(s) \cdot G_{\text{BPF}}(s) + Z_{o\_o}(s))Z_{\text{Capa}}(s)}{Z_{\text{Capa}}(s)(1 + H(s)G_c(s)G_{v\phi}(s)) + Z_{ff}(s) \cdot G_{\text{BPF}}(s) + Z_{o\_o}(s)} \\ &= -\frac{1}{\dfrac{1 + H(s)G_c(s)G_{v\phi}(s)}{Z_{ff}(s) \cdot G_{\text{BPF}}(s) + Z_{o\_o}(s)} + \dfrac{1}{Z_{\text{Capa}}(s)}} \end{aligned} \tag{7.12}$$

Thus if we want to maximum the amplitude of $Z_{\text{DAB\_new}}(j2\omega_0)$, the equation should

be fulfilled.

$$\frac{1 + H(j2\omega_0)G_c(j2\omega_0)G_{v\phi}(j2\omega_0)}{Z_{ff}(j2\omega_0) \cdot G_{\text{BPF}}(j2\omega_0) + Z_{o\_o}(j2\omega_0)} + \frac{1}{Z_{\text{Capa}}(j2\omega_0)} \approx 0 \tag{7.13}$$

Since $G_{\text{BPF}}(j2\omega_0)$ equals to 1, the impedance of the feedforward part should be

$$Z_{ff}(j2\omega_0) = -Z_{\text{Capa}}(j2\omega_0) - Z_{\text{Capa}}(j2\omega_0)H(j2\omega_0)G_c(j2\omega_0)G_{v\phi}(j2\omega_0) - Z_{o\_o}(j2\omega_0) \tag{7.14}$$

In general the transfer function of the feedforward path should be

$$Z_{ff}(s) = -Z_{\text{Capa}}(s) - Z_{\text{Capa}}(s)H(s)G_c(s)G_{v\phi}(s) - Z_{o\_o}(s) \tag{7.15}$$

From (Shi *et al.*, 2016), the bandwidth of the BPF should be at least 2.8Hz. Given margin, the f_b is chosen as 20Hz while Q equals to 6.

$$G_{\text{BPF}}(s) = \frac{1/Q/\omega_{2\text{nd}}s}{1/\omega_{2\text{nd}}^2 s^2 + 1/Q/\omega_{2\text{nd}}s + 1} \tag{7.16}$$

The proposed SHC reduction method is applied to the controller with the fast PI case. The output impedance is shown as Figure 7.12. The modified output impedance of the DAB converter is shown as the green curve in Figure 7.12. The amplitude is increased from 8.76dB to 72.9dB. The $Z_{\text{DAB\_new}}(0\text{Hz})$ rises a little because of the wide bandwidth BPF but it's quite acceptable.

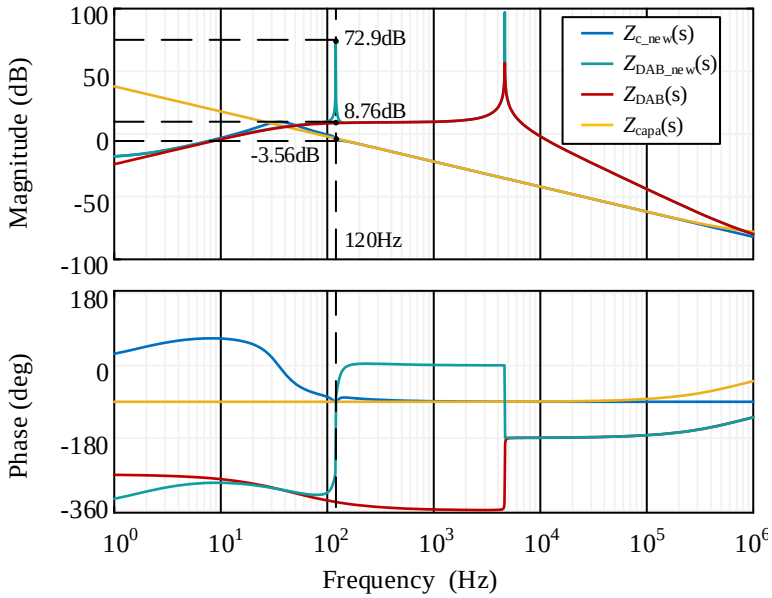


Figure 7.12: Output impedance of the fast PI case with proposed SHC reduction method.

7.3.3 Implement of the LCFF Control

The control block with the LCFF control is shown as Figure 7.13.

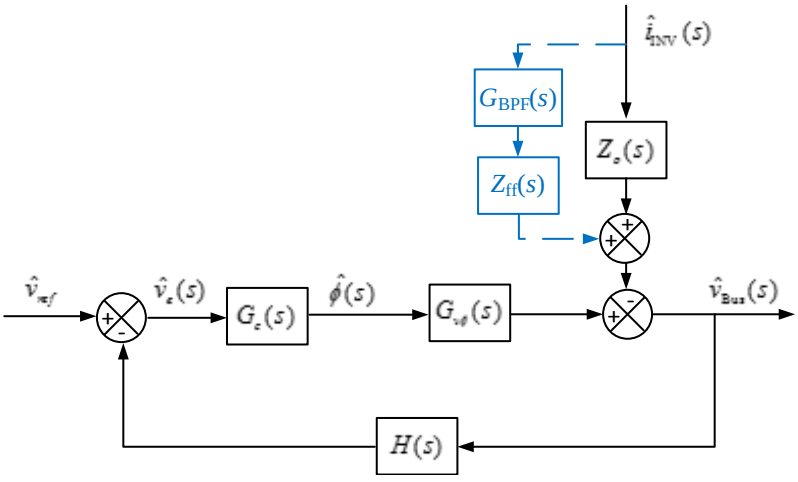


Figure 7.13: Control block with the proposed LCFF path.

In order to implement the feedforward method, the "feedforward" phase-shift value can be added for the three-phase DAB converter by moving the node in Figure 7.13 forward as Figure 7.14.

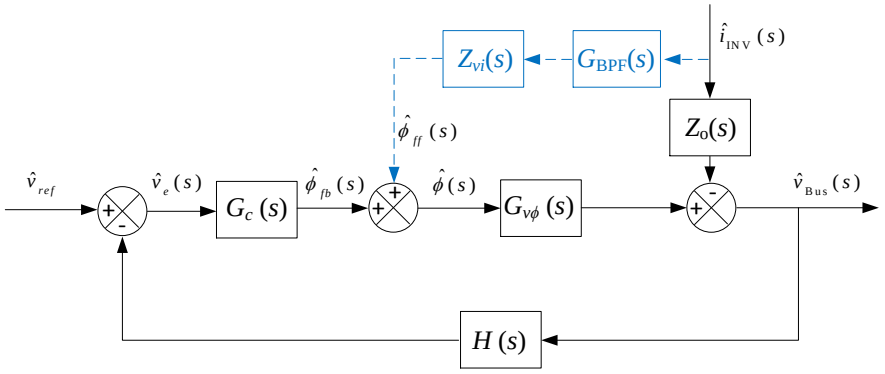


Figure 7.14: Control block with the proposed LCFF path.

If I neglect the stray inductance an ESR of the capacitors, Z_{capa} is $1/sC_2$. Thus the LCFF term $Z_{vi}(s)$ can be expressed as

$$Z_{vi}(s) = Z_{\text{Capa}}\left(\frac{3L_k n\omega\pi}{R_{\text{load}}V_{\text{Batt}}(3\phi_0-2\pi)} - G_c(s)\right) = \frac{1}{sC_2}\left(\frac{3L_k n\omega\pi}{R_{\text{load}}V_{\text{Batt}}(3\phi_0-2\pi)} - K_p - \frac{K_i}{s}\right) \quad (7.17)$$

Since an integration part existing in the $Z_{vi}(s)$, the add-on phase-shift value $\hat{\phi}_{ff}(s)$ will keep increasing with time. It will cause problem if a digital controller with saturation is applied in experiment. To solve this problem, another BPF can be added after $Z_{vi}(s)$ in the LCFF path. This method won't increase the order of the whole LCFF control path thus this BPF is not discussed in the chapter.

7.3.4 Parameter Sensitivity Analysis

The accuracy of the parameter L_k and C_2 affects the SHC reduction performance by the load current feedforward control. When implementing the LCFF method, the

equivalent resistor load R_{load} should be calculated online by the sensed bus voltage and load current so R_{load} can be seen as a parameter in the LCFF method at steady-state operation. Considering the sensor's error, R_{load} may not be exactly accurate. Hence, the parameter sensitivity analysis of L_k, C_2 and R_{load} should be provided. The parameter error within $\pm 20\%$ is considered in this chapter. The amplitude of $Z_{\text{DAB\_new}}(j2\omega_0)$ under $\pm 20\%$ parameter errors is used to analysis the SHC reduction performance as Figure 7.15 and Figure 7.16.

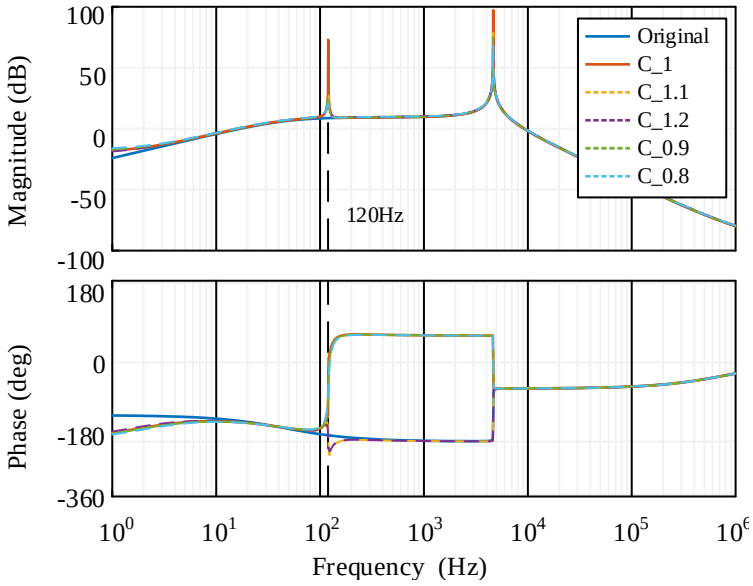


Figure 7.15: Parameter sensitivity analysis of the LCFF method under capacitance error.

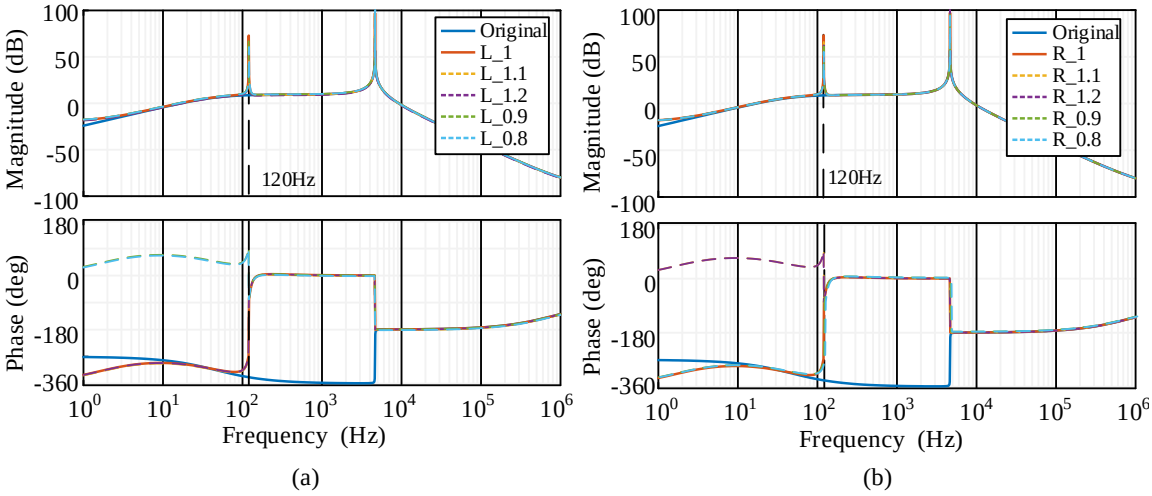


Figure 7.16: Parameter sensitivity analysis of the LCFF method: (a) under L_k error. (b) under R_{load} error.

The amplitude of $Z_{\text{DAB\_new}}(j2\omega_0)$ is summarized in Table 7.2.

Table 7.2: Parameters sensitive analysis by amplitude of $Z_{\text{DAB\_new}}(j2\omega_0)$ (dB).

Parameters	100%	110%	120%	90%	80%
C_2	72.9	29.1	23.9	27.2	20.2
L_k	72.9	61.7	57	68.7	60.3
R_{load}	72.9	70	62.3	61	55.3

From the Figure 7.15, Figure 7.16 and Table 7.2, the amplitude of $Z_{\text{DAB\_new}}(j2\omega_0))$ under L_k and R_{load} parameter errors are close to it without error which means the LCFF method is not sensitive with their error. For C_2 parameter error, the amplitude of the output impedance drops. However, the LFCC method with capacitance error still works quite better than it without LFCC method. And the SHC reduction performance closes to it with slow PI. The analysis will be continued in the Section IV.

7.4 Simulation and Experimental Results

7.4.1 Simulation Results

A simulation model of the system as Figure 7.1 is built to verify the performance of the SHC reduction method.

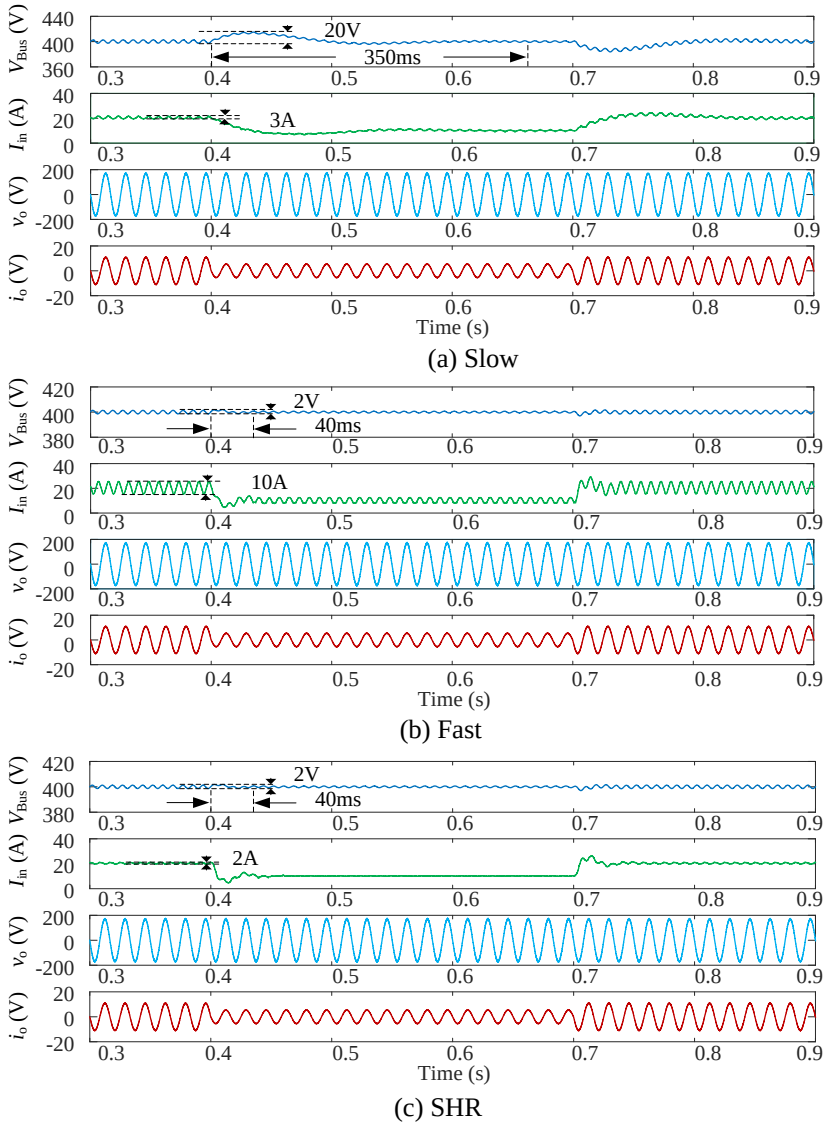


Figure 7.17: Simulation results: (a) the slow PI case. (b) the fast PI without LCFF case. (c) the fast PI with LCFF case.

The output of the inverter is 60Hz 120Vrms. 1kW simulation waveforms are illustrated as Figure 7.17. The converter operates at 1kW. At 0.4s, the load transient is form 1kW to 500W then at time 0.7s the load transient is from 500W to 1kW. For the dynamic response performance, the fast PI case and the fast PI with LCFF case share the similar voltage overshoot, undershoot and transient time. However, the slow PI case has a much longer transient time and larger overshoot.

For the steady-state analysis, the battery current is utilized to compare the performance of SHC reduction as green lines in Figure 7.17. Although the fast PI case without LCFF control has good dynamic response, the SHC is as high as peak-to-peak 7.86A which will age the battery by adding extra Ah-throughput. For the fast PI cast with LCFF control, the SHC is almost as low as the slow PI cast but still remain a good dynamic response. The simulation results proves the SHC reduction method.

7.4.2 Experimental Results

To verify the proposed SHC reduction method, a two-stage single-phase inverter is setup as Figure 7.18. The specifications of the battery energy storage system are listed in Table 7.3.

Table 7.3: Parameters of the isolated battery-driven grid interface.

Specifications		value
Input battery voltage V_{Batt}		48V
DC bus voltage V_{Bus}		400V
Output inverter voltage v_{o}		120Vrms
Output inverter frequency f_0		60Hz
	Parameters	value
Front-end three-phase DAB converter	Transformer turn ratio n	1:8
	Transformer leakage inductance L_k	$33\mu H$
	Input capacitor C_1	$80\mu F$
	Output capacitor C_2	2mF
	Switching frequency f	100kHz
Downstream inverter	Inverter side inductor L_1	45uH
	Inverter capacitor C_f	$8\mu F$
	Grid side inductor L_2	$15\mu H$
	Switching frequency f	100kHz

The front-end three-phase DAB converter is responsible to interface between the battery and the DC bus. The downstream single-phase inverter has dual grid-tied and standalone modes. The inverter operates as standalone mode using a resistor as

the load. The DSP TI28337D is utilized to control the system. The sample period is selected as 10us. The DC bus is designed by a hybrid capacitor bank as Chapter 5.

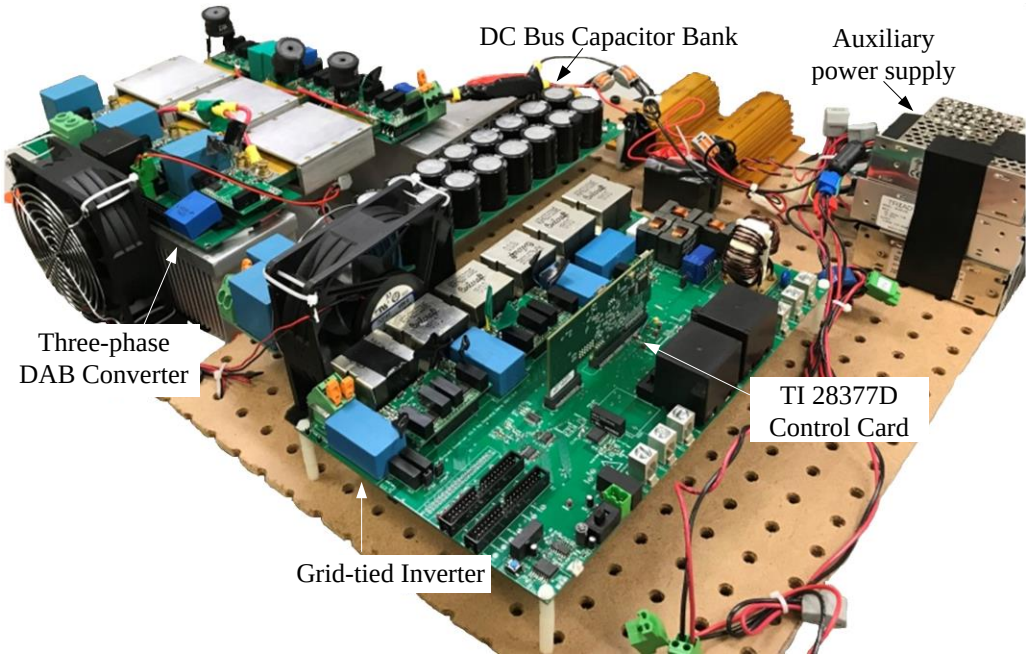
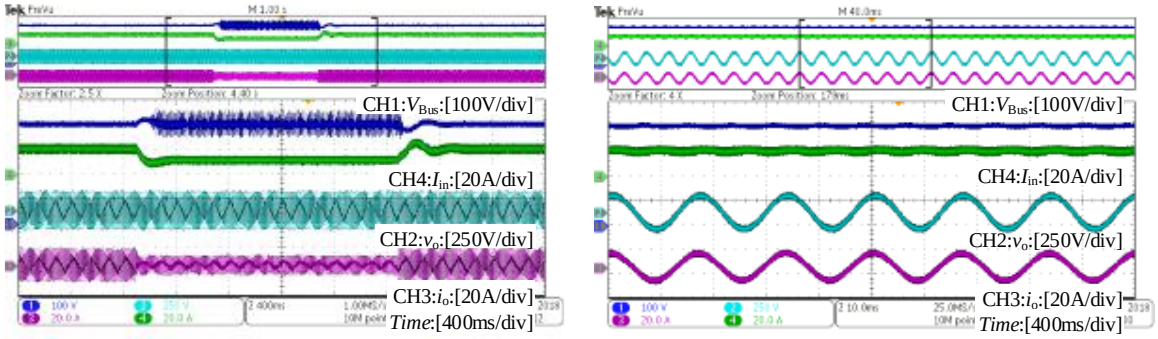


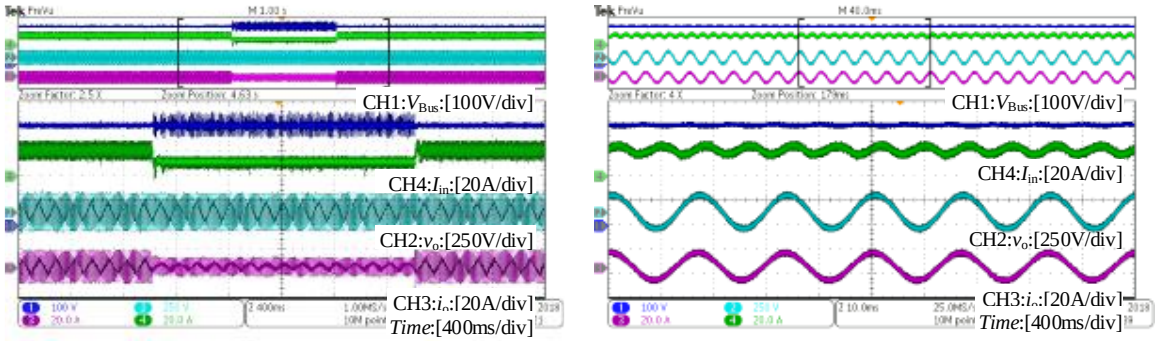
Figure 7.18: Experiment setup.

A 1kW experiment is conduct to verify the performance of SHC reduction. The waveforms of the slow PI case, the fast PI case without LCFF control and the fast PI case with LCFF control are shown as Figure 7.19, Figure 7.20 and Figure 7.21 respectively. The oscillation of the V_{Bus}, blues lines in Figure 7.19, Figure 7.20 and Figure 7.21, during 500W load condition is caused by losing ZVS of the DAB converter however it won't affect our SHC reduction performance.



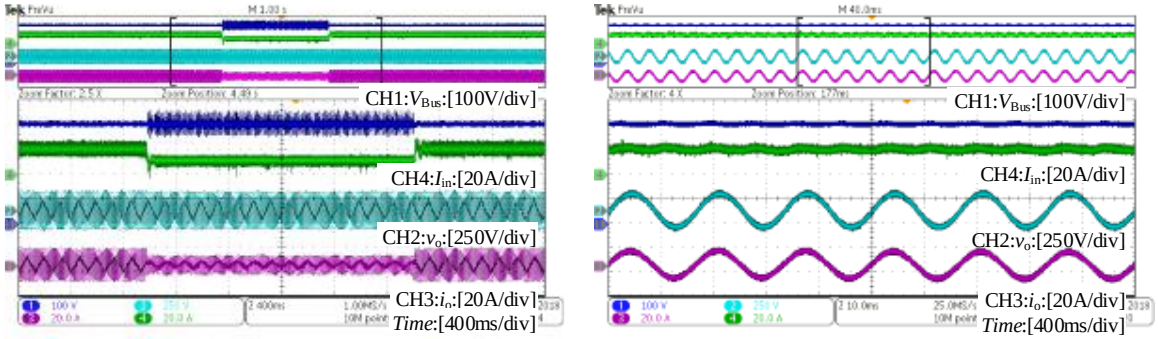
(a) Dynamic Performanc (b) Steady-State Performance

Figure 7.19: Experimental waveforms with the slow PI cast: (a) Load transient response between 1kW and 500W. (b) Steady-state performance.



(a) Load change (b) SHC Performance

Figure 7.20: Experimental waveforms with the fast PI cast without LCFF control: (a) Load transient response between 1kW and 500W. (b) Steady-state performance.



(a) Dynamic Performanc (b) Steady-State Performance

Figure 7.21: Experimental waveforms with the fast PI cast with LCFF control: (a) Load transient response between 1kW and 500W. (b) Steady-state performance.

The dynamic response performance and steady-state SHC of the three cases are summarized as Table 7.4. The voltage V_{Bus} overshoot, undershoot and setting time are shown to assess the dynamic response performance during load transient while the DC component and second harmonic of the battery current i_{in} are utilized to compare the SHC reduction performance.

Table 7.4: Dynamic response and steady-state performance comparison.

Cases	Dynamic performance			Steady-state performance		
	Overshoot	Undershoot	Setting time	DC component of iin	Second harmonic of i_{in}	
					Amplitude	$i_{\text{sec}}/I_{\text{DC}}$
Slow PI	21V	20.2V	353ms	20.7A	0.79A	3.82%
Fast PI without LCFF	1.2V	1.4V	45ms	20.7A	3.12A	15.1%
Fast PI with LCFF	1.3V	1.5V	50ms	20.7A	0.69A	3.35%

From Table 7.4, the case of fast PI with LCFF has less SHC component than it with slow PI case but has similar dynamic response with fast PI case. This verifies that the SHC reduction method by adding a LCFF path for the three-phase DAB converter based two-stage single-phase system. The second harmonic current of the experiment is less than the simulation results because the decoupling capacitor and the film capacitor for filtering high switching frequency harmonics will absorb part of SHC in the experiment.

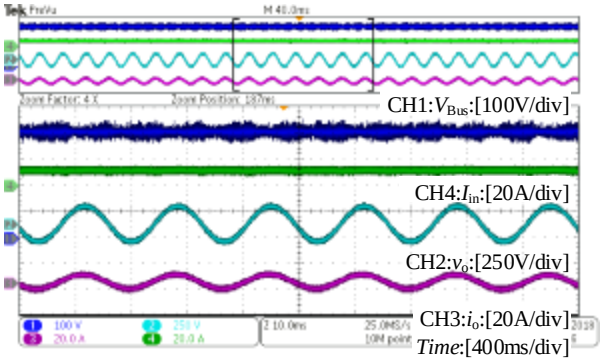


Figure 7.22: Steady-state performance for the fast PI with LCFF case at 500W.

The steady-state performance for the fast PI with LCFF control case at half load is still shown as Figure 7.22. The SHC proportion $i_{\text{in}}(120Hz)/i_{\text{in}}(0Hz)$ is 5.2% which shows the SHC reduction method still works in this case. It means that the LCFF method still works very well even with 50% Rload error.

7.4.3 Experimental Results for Parameter Sensitivity Analysis.

As the following research of parameter sensitivity, the experimental results are provided to verify the SHC reduction performance with parameters' errors. The steady-state performance waveforms are illustrated as Figure 7.23. The SHC proportion of the battery current for the fast PI with LCFF control at 1kW experiment is summarized as Table 7.5. All the SHC is within 10% of the DC component which is quite acceptable with ±20% parameter error.

Table 7.5: SHC proportion comparison with parameter errors.

Intereste parameters	Parameters ratio				
	100%	110%	120%	90%	80%
DCbus capacitance C_2	3.32%	4.08%	4.29%	4.15%	5.29%
Leakageinductance L_k	3.32%	3.47%	3.53%	3.5%	3.53%
Equivalent load resistor R_{load}	3.32%	3.32%	3.55%	3.53%	3.59%

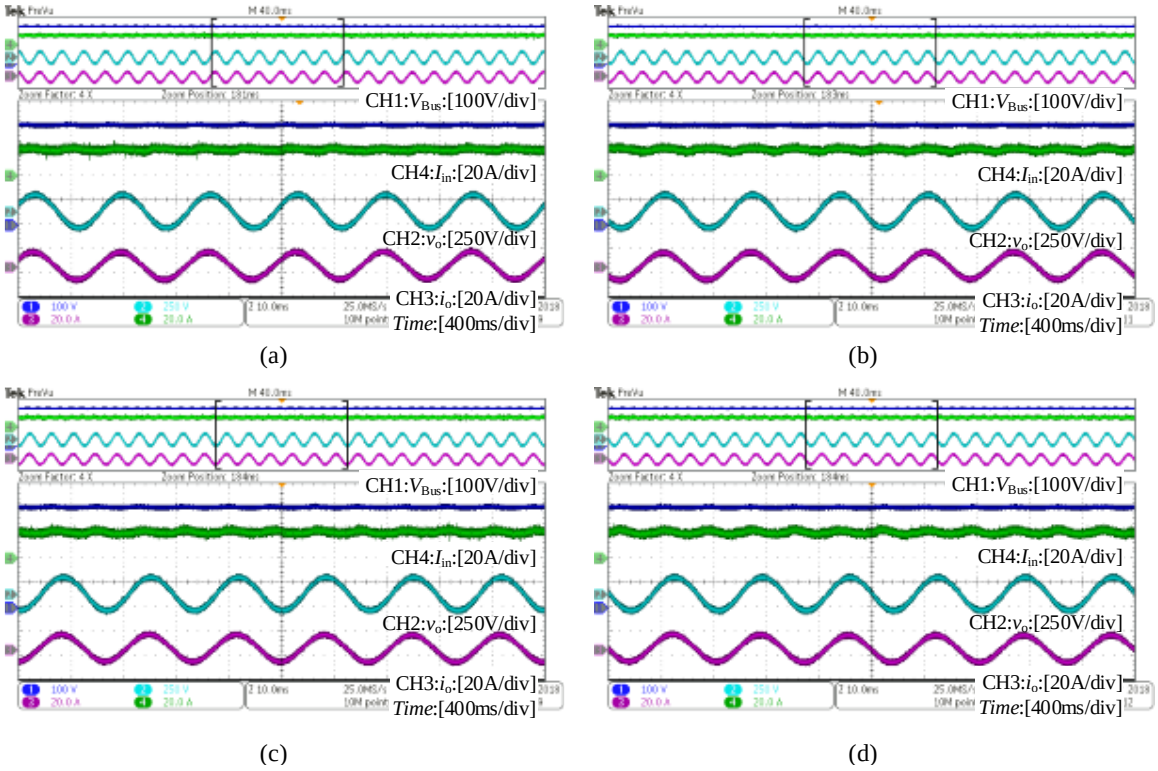


Figure 7.23: Steady-state performance with capacitance error: (a) 110% C_2. (b) 120% C_2. (c) 90% C_2. (d) 80% C_2.

7.5 Conclusion

A SHC reduction method is proposed for the three-phase DAB convert based two-stage single-phase inverter with just adding a LCFF path. This method is analyzed from the perspective of the output impedance to add virtual impedance to the output impedance of the front-end three-phase DAB converter so that the output impedance at the double frequency is much higher than it of the DC bus capacitor. This method will suppress the SHC as well as keeping good dynamic performance. The method doesn't need to modify the voltage closed-loop controller of the front-end converter so that it's easy to be implemented. The small-signal model of the three-phase DAB converter is provided and verified by its step response. The parameter sensitivity analysis for the LCFF method is proposed to show that the SHC is well suppressed within $\pm 20\%$ parameter error. Finally, a 1kW simulation and experimental results are provided to verify the SHC reduction method.

Chapter 8

Conclusions and Future Work

8.1 Conclusions

A two-stage isolated battery-driven grid interface (IBDGI) with front-end three-phase DAB converter is proposed for battery energy storage system (BESS) in residential applications.

An effective design strategy of the front-end three-phase DAB converter is proposed to achieve high efficiency in wide operation voltage range and load conditions considering the ZVS zone and back-flow ratio. The design strategy is verified by the efficiency analysis based on the power loss model. Then a variable switching frequency strategy is proposed to improve the efficiency at the light load conditions by minimizing the switching frequency. By tracking the power rating, the method is quite easy to be applied by following one equation. A 3kW experimental setup is built to verify the design strategy and the variable switching frequency method.

In this thesis, the comprehensive analysis of the dead-time effect is proposed for the three-phase DAB converter. The dead-time phenomena, such as voltage polarity

reversal, voltage sag and phase shift, is also existing in the three-phase topology. The detailed operation states, transmission power, constrain equations and switching characterization are provided. The experiment results and simulation results verified the theoretical analysis. This study can help to better design of the three-phase DAB converter to avoid the dead-time effect and better understanding of the operation phenomena with dead-time effect in the three-phase DAB converter.

The design procedure of the hybrid capacitor bank is presented for the DC bus of the IBDGI system. The hybrid capacitor bank is composed by the LC resonant filter with electrolytic capacitor and film capacitor where the electrolytic capacitors are utilized for passive decoupling purpose while the film capacitor is responsible for high switching harmonic filtering. Then a current sharing method between the hybrid capacitor bank is analyzed. The performance of the proposed capacitor bank is verified by both simulation and experimental results.

The LCL single-phase inverter is used as the downstream converter of the IBDGI system for both grid-tied and standalone operation modes. A step-by-step design procedure of the LCL filter with passive damping is proposed for the 120V/240V dual mode inverter. PLL is utilized to detect the grid voltage phase. The PR controllers are designed for the LCL inverter for standalone and grid-tied modes. The simulation and experimental results are provided to verify the performance of the LCL filter and PR controllers.

A novel SHC reduction strategy is proposed for the IBDGI system with the front-end three-phase DAB convert by adding a LCFF path to the DAB voltage closed-loop controller. This method is analyzed from the perspective of the output impedance to add virtual impedance to the output impedance of the front-end converter so that

the output impedance at the double frequency is much higher than it of the DC bus capacitor. This method will suppress the SHC but doesn't need to modify the voltage closed-loop controller which make it easy to be implemented. The small-signal model of the three-phase DAB converter is provided and verified by the step response. The parameter sensitivity analysis for the LCFF method is proposed to show that the SHC is well suppressed within ±20% parameter error. Finally, a 1kW simulation and experimental results are provided to verify the SHC reduction method.

8.2 Future Work

Related research topics which can be further investigated in future developments are listed as follows:

1. Advanced modulation strategy of the three-phase DAB converter can be investigated to further reduce the back-flow power and increase the overall efficiency. Like extended-phase-shift (EPS) and dual-phase-shift (DPS) in single-phase DAB converter, similar modulation is promising in three-phase DAB topology. However, certain strategy should be proposed to overcome the drawback of the three half-bridge structure in three-phase DAB converters.

2. To further increase the efficiency, three-phase LLC converter can be proposed for this application. Wider soft-switching zone can be achieved by the LLC resonant tank however wide switching frequency range will make the efficiency comparison complicated. Moreover, larger passive component may be resulted depending on its lowest switching frequency.

3. The dead-time effect of the three-phase DAB converter is proposed in this thesis.

However, an online Dead-time compensator can be the following work to avoid the dead-time effect with wide operation conditions. On the other hand, some of the dead-time effect is promising to be implemented during normal operation for their ZCS features.

4. Simple and reliable active decoupling method can be proposed to replace the passive decoupling method. The stability analysis is still crucial for the system with active decoupling since low DC bus capacitance will contribute to the constant power load issues.

5. The two-stage topology discussed in this thesis also suffers from low efficiency especially for low voltage high power application. Some strategy should be proposed to improve the efficiency of the full-bridge single-phase inverter. One solution is that the switching frequency can be reduced to decrease the switching loss but keeping the same power density by using coupled inductor. Multi-level single-phase inverter can also be investigated to reduce the switching frequency but keep the same inverter performance with smaller filter. On the other hand, new topology can be proposed for the single-phase inverter to achieve soft-swiching.

6. Islanding detection is always a hot spot for grid-tied inverter. And the system control strategy should be proposed to smooth switch between standalone mode and grid-tied mode.

7. The SHC reduction strategy is still needed for charge phase of the IBDGI system. How to mitigate the SHC with single-phase PFC rectifier can be an interesting future work especially for the CV charge phase.

8. Advanced switching devices like Gallium Nitride (GaN) HFETs are perfect for this application where 600V and 100V V_{ds} are preferred. However, careful gate driver design should be proposed to avoid self turn-on of the switches and cooling system design is also challenging for their small top or bottom cooling package.

8.3 Publications

Accepted papers

- **D. Wang**, F. Peng, J. Ye, Y. Yang and A. Emadi, "Dead-Time effect analysis of a three phase dual active bridge DC/DC converter," *IET Power Electronics*, 2017.

- **D. Wang**, P. Malysz, Y. Hong and A. Emadi, "Battery state and parameter estimation using a mixed sigma-point kalman filtering and recursive least squares technique," *US patent* , Application No. 15298314, 2018.

- **D. Wang**, M. Preindl, F. Peng, J. Ye and A. Emadi, "DC-Bus Design with Hybrid Capacitor Bank in Single-Phase PV Inverters," *Industrial Electronics Society , IECON 2017 - 43rd Annual Conference of the IEEE*, 2017.

- Y. Cui, **D. Wang**, and A. Emadi, "Three-Phase Dual Active Bridge Converter Design Considerations," *Industrial Electronics Society , IECON 2017 - 43rd Annual Conference of the IEEE*, 2017.

Submitted papers

- **D. Wang**, B. Nahidmobarakeh, Y. Jin, and A. Emadi, "Design strategy of a three phase Dual active bridge DC/DC converter for renewable energy application," *IEEE Transactions on Power Electronics*.

- **D. Wang**, B. Nahidmobarakeh, and A. Emadi, "Second harmonic current reduction with load current feedforward control for the three-phase dual active bridge DC/DC converter based two-stage single-phase inverter," *IEEE Transactions on Industrial Electronics*.

- **D. Wang**, Y. Jin, and A. Emadi, "Design of LCL inverter and PR controllers for dual grid-tied and standalone mode operation in residential applications," *IEEE Transactions on Industrial Electronics*.

Appendix A

Transmission Power and Constrain Conditions of Dead-time Effect in Three-Phase DAB Converter

A.1 Boost State

Table A.1: Constrain conditions for boost state.

	Constraint conditions
Mode A1	$\frac{2\pi(d-1)}{3d} \leq D < \frac{\pi}{3}$ and $0 \leq \phi < \frac{4\pi + 6Dd - 4\pi d}{3(d+1)}$
Mode A2	$\frac{2\pi(d-1)}{3d} \leq D < \frac{\pi}{3}$ and $\frac{4\pi + 6Dd - 4\pi d}{3(d+1)} \leq \phi < \frac{3Dd - 2\pi d + 2\pi}{3}$
Mode A3	$\begin{cases} 0 \leq D < \frac{2\pi(d-1)}{3d} & 0 \leq \phi < \frac{3Dd - 2\pi d + 2\pi}{3} \\ 0 \leq D < \frac{\pi}{3} & \frac{3Dd - 2\pi d + 2\pi}{3} \leq \phi < D \end{cases}$
Mode A4	$\begin{cases} 0 \leq D < \frac{\pi}{3} & D \leq \phi < \frac{3D - 2\pi + 2\pi d}{3d} \\ \frac{\pi(2-d)}{3} \leq D < \frac{\pi}{3} & \frac{3D - 2\pi + 2\pi d}{3d} \leq \phi < \frac{3D - 2\pi + 3\pi d}{6d} \end{cases}$
Mode A5a	$\frac{\pi(2-d)}{3(d+1)} \leq D < \frac{\pi(2-d)}{3}$ and $\frac{\pi}{3} \leq \phi < \frac{3D + 3Dd - 2\pi + 2\pi d}{3d}$
Mode A5b	$\frac{\pi(2-d)}{3} \leq D < \frac{\pi}{3}$ and $\frac{3D - 2\pi + 3\pi d}{6d} \leq \phi < \frac{3D + 6Dd - 2\pi + 3\pi d}{6d}$
Mode A5c	$\begin{cases} 0 \leq D < \frac{\pi(2-d)}{3} & \frac{3D - 2\pi + 2\pi d}{3d} \leq \phi < \frac{3D + 3Dd - 2\pi + 2\pi d}{3d} \\ \frac{\pi(2-d)}{3(d+1)} \leq D < \frac{\pi(2-d)}{3} & \frac{3D + 3Dd - 2\pi + 2\pi d}{3d} \leq \phi < \frac{\pi}{3} \end{cases}$
Mode A6a	$0 \leq D < \frac{\pi(2-d)}{3(d+1)}$ and $\frac{3D + 3Dd - 2\pi + 2\pi d}{3d} \leq \phi < \frac{\pi}{3}$
Mode A6b	$\begin{cases} 0 \leq D < \frac{\pi(2-d)}{3(d+1)} & \frac{\pi}{3} \leq \phi < \frac{2\pi}{3} \\ \frac{\pi(2-d)}{3(d+1)} \leq D < \frac{\pi(2-d)}{3} & \frac{3D + 3Dd - 2\pi + 2\pi d}{3d} \leq \phi < \frac{2\pi}{3} \\ \frac{\pi(2-d)}{3} \leq D < \frac{\pi}{3} & \frac{3D - 2\pi + 3\pi d}{6d} \leq \phi < \frac{2\pi}{3} \end{cases}$

Table A.2: Transmission power for boost state.

	Transmission power
Mode A1	$-\frac{dV_i^2(d-1)(3D-4\pi)^2}{18L\omega\pi(d+1)}$
Mode A2	$-\frac{dV_i^2(D-\phi)(3D+3\phi-8\pi-9Dd+8\pi d+3d\phi)}{6L\omega\pi(d-1)}$
Mode A3	$-\frac{dV_i^2(D-\phi)(3\phi-3D+4\pi)}{6L\omega\pi}$
Mode A4	$-\frac{dV_i^2(D-\phi)(3D-3\phi+4\pi)}{6L\omega\pi}$
Mode A5a	$-\frac{V_i^2(9D^2d^2-9D^2-18Dd^2\phi+12\pi Dd^2+12\pi D+27d^2\phi^2-30\pi d^2\phi+5\pi^2d^2-4\pi^2)}{18Ld\omega\pi}$
Mode A5b	$-\frac{V_i^2(18D^2d^2-9D^2-36Dd^2\phi+24\pi Dd^2+12\pi D+54d^2\phi^2-60\pi d^2\phi+9\pi^2d^2-4\pi^2)}{36Ld\omega\pi}$
Mode A5c	$-\frac{V_i^2(9D^2d^2-9D^2-18Dd^2\phi+12\pi Dd^2+12\pi D+18d^2\phi^2-24\pi d^2\phi+4\pi^2d^2-4\pi^2)}{18Ld\omega\pi}$
Mode A6a	$\frac{dV_i^2\phi}{\omega L}(\frac{2}{3}-\frac{\phi}{2\pi})$
Mode A6b	$\frac{dV_i^2\phi}{\omega L}(\phi-\frac{\pi}{18}-\frac{\phi^2}{\pi})$

A.2 Buck State

Table A.3: Constrain conditions for buck state.

	Constraint conditions
Mode B1	$\frac{2\pi(1-d)}{3} \leq D < \frac{\pi}{3}$ and $0 \leq \phi < \frac{(d-1)(3D-4\pi)}{3(d+1)}$
Mode B2	$\frac{2\pi(1-d)}{3} \leq D < \frac{\pi}{3}$ and $\frac{(d-1)(3D-4\pi)}{3(d+1)} \leq \phi < D$
Mode B3a	$\frac{2\pi(1-d)}{3} \leq D < \frac{\pi}{3}$ $D \leq \phi < \frac{3D+3Dd-2\pi+2\pi d}{3d}$ $\frac{\pi(2-d)}{3(d+1)} \leq D < \frac{\pi}{3}$ $\frac{3D+3Dd-2\pi+2\pi d}{3d} \leq \phi < \frac{\pi}{3}$
Mode B3b	$\frac{\pi(2-d)}{3(d+1)} \leq D < \frac{\pi}{3}$ and $\frac{\pi}{3} \leq \phi < \frac{3D+3Dd-2\pi+2\pi d}{3d}$
Mode B4a	$0 \leq D < \frac{2\pi(1-d)}{3}$ $0 \leq \phi < \frac{3D+3Dd-2\pi+2\pi d}{3d}$ $0 \leq D < \frac{\pi(2-d)}{3(d+1)}$ $\frac{3D+3Dd-2\pi+2\pi d}{3d} \leq \phi < \frac{\pi}{3}$
Mode B4b	$0 \leq D < \frac{\pi(2-d)}{3(d+1)}$ $\frac{\pi}{3} \leq \phi < \frac{3D+3Dd-2\pi+2\pi d}{3d}$ $0 \leq D < \frac{\pi}{3}$ $\frac{3D+3Dd-2\pi+2\pi d}{3d} \leq \phi < \frac{2\pi}{3}$

Table A.4: Transmission power for buck state.

	Transmission power
Mode B1	$-\frac{dV_i^2(d-1)(3D-4\pi)^2}{18L\omega\pi(d+1)}$
Mode B2	$-\frac{dV_i^2(d-1)(3D-4\pi)^2}{18L\omega\pi(d+1)}$
Mode B3a	$\frac{dV_i^2(3\phi-4\pi)(6D-3\phi-4\pi+6Dd+4\pi d-9d\phi)}{18L\omega\pi(d+1)}$
Mode B3b	$\frac{dV_i^2(6\pi\phi-17d\pi^2-36d\phi^2+15\pi^2-18\phi^2-24\pi D+18D\phi-24\pi Dd+18Dd\phi+54\pi d\phi)}{18L\omega\pi(d+1)}$
Mode B4a	$\frac{dV_i^2\phi}{\omega L}(\frac{2}{3}-\frac{\phi}{2\pi})$
Mode B4b	$\frac{dV_i^2\phi}{\omega L}(\phi-\frac{\pi}{18}-\frac{\phi^2}{\pi})$

A.3 Matching State

Table A.5: Transmission power and constrain conditions for matching state.

	Constraint conditions
Mode C1a	$\begin{cases} 0 \le D < \frac{\pi}{6} & D \le \phi < 2D \\ \frac{\pi}{6} \le D < \frac{\pi}{3} & D \le \phi < \frac{\pi}{3} \end{cases}$
Mode C1b	$\frac{\pi}{6} \le D < \frac{\pi}{3}$ and $\frac{\pi}{3} \le \phi < 2D$
Mode C2	$0 \le \phi < D$
Mode C3a	$0 \le D < \frac{\pi}{6}$ and $2D \le \phi < \frac{\pi}{3}$
Mode C3b	$\begin{cases} 0 \le D < \frac{\pi}{6} & \frac{\pi}{3} \le \phi < 2D \\ 2D \le \phi < \frac{2\pi}{3} \end{cases}$

Table A.6: Transmission power and constrain conditions for matching state.

	Transmission power
Mode C1a	$-\frac{dV_i^2(D-\phi)(21\phi - 9D + 2\pi + 9Dd^2 + 2\pi d^2 + 3d^2\phi + 4\pi d - 30d\phi)}{6L\omega\pi(2d-1)}$
Mode C1b	$-\frac{dV_i^2(108D^2d^2 - 108D^2 - 252Dd^2\phi + 84\pi Dd^2 + 180Dd\phi - 132\pi Dd + 144\pi D)}{72L\omega\pi(2M-1)}$ $-\frac{dV_i^2(135d^2\phi^2 - 90\pi d^2\phi + 3\pi^2d^2 + 18d\phi^2 - 72\pi d\phi + 46\pi^2 d - 45\phi^2 + 42\pi\phi - 45\pi^2)}{72L\omega\pi(2d-1)}$
Mode C2	0
Mode C3a	$\frac{dV_i^2\phi}{\omega L}(\frac{2}{3} - \frac{\phi}{2\pi})$
Mode C3b	$\frac{dV_i^2\phi}{\omega L}(\phi - \frac{\pi}{18} - \frac{\phi^2}{\pi})$

Appendix B

Experiment Setup

B.1 Prototype

B.1.1 Prototype 1

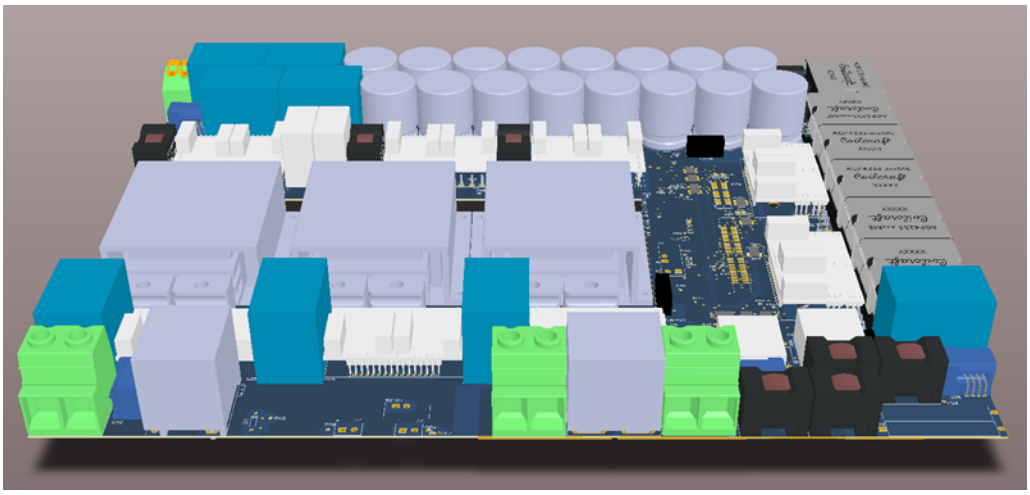


Figure B.1: 3D PCB model of the Prototype 1.

Table B.1: Hardware component list for the proposed system.

Description		Index	Part Number
Three-phase DAB Converter	Input side capacitor	C_1	B32676G3206K
	Input side switch	$S_1 - S_6$	IPP045N10N3G
	Add-on leakage inductor	L_a, L_b, L_c	VER2923-682
	Output side Capacitor	C_2	B32794D2106
	Output side Switch	$Q_1 - Q_6$	c3m0065090d
DC Bus	Film capacitor	C_F	B32796E2256
	Electrolyte capacitor	C_E	647-LLS2V471MELB
	Electrolyte capacitor inductor	L_E	VER2923-682
Single-phase LCL Inverter	Switches	$Q_7 - Q_{10}$	C2M0025120D
	Inverter-side inductor	L_1	AGP4233-682ME
	Capacitor	C_f	B32796E2256
	Passive damping resistor	R_f	RS010R2000FE73
	Grid-side inductor	L_2	VER2923-332

The first prototype of the isolated battery-driven grid interface is built as Figure B.1 and its component list can be found in Table B.1. The board size Length*Width*Hight is 391.41mm*294.51*49.44mm as Figure B.2. The utilized transformers with 1:8 turn ratio is custormer designed by Payton but they suffer from lwo magnetizing inductance which will result in high circulating current.

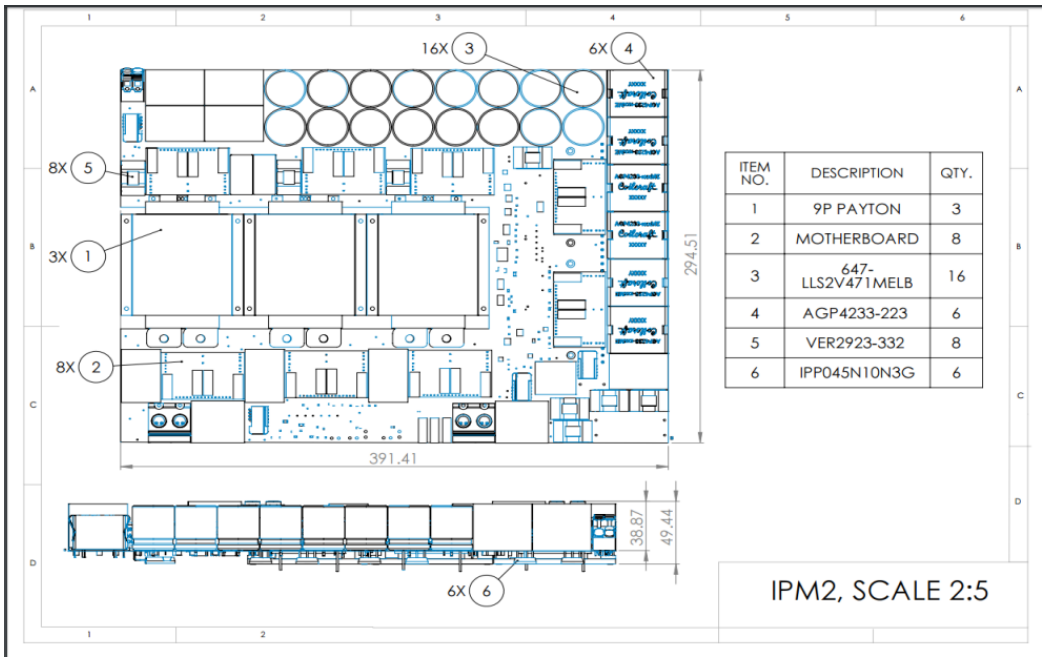


Figure B.2: Size of the Prototype 1 3D model.

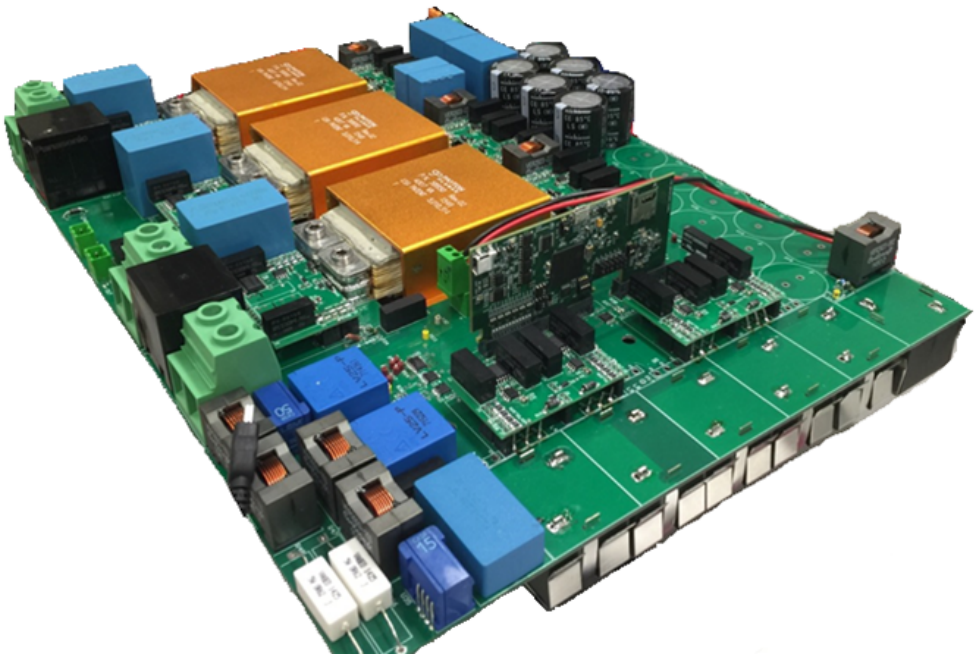


Figure B.3: Experiment setup of the Prototype 1.

The first prototype setup can be found in Figure B.3. The gate driver design as Figure B.4 refers to Cree's two-stage gate driver reference design which includs a multi-function IGBT driver chip (1ED020I12-B2) and a high-current MOSFET driver chip(IXDN609SI)

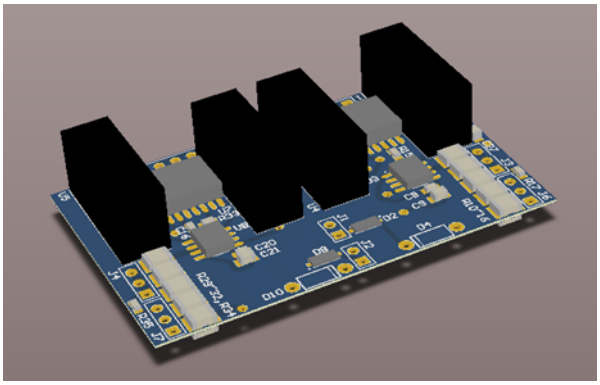


Figure B.4: Applied gate driver.

A lot of work is done to solve the parasitics issues for the experiment setup when a flat product-shape prototype wants to be achieved. For example, the netrual point of the three transformers of the three-phase DAB converter should be carefully layouted. Since the waveform of the netrual point will be pulsed varied instead of keeping constnat as other applications, the stray capacitance between the netrual point and positive/negative DC bus will cause distortion of the voltage waveform. Besides the feedback signals, current and voltage sensing signal, should be filtered since the power-stage board is so close to the controller board.

B.1.2 Prototype 2

To obtain more flexibility and redundance, the three-phase DAB converter, DC bus and single-phase inverter is designed seperately as Figure B.5 and Figure B.8. All

used components are the same with the Prototype 1 as Table B.1. The DSP 28377D controller board and the controller interface are also built in Figure B.8.

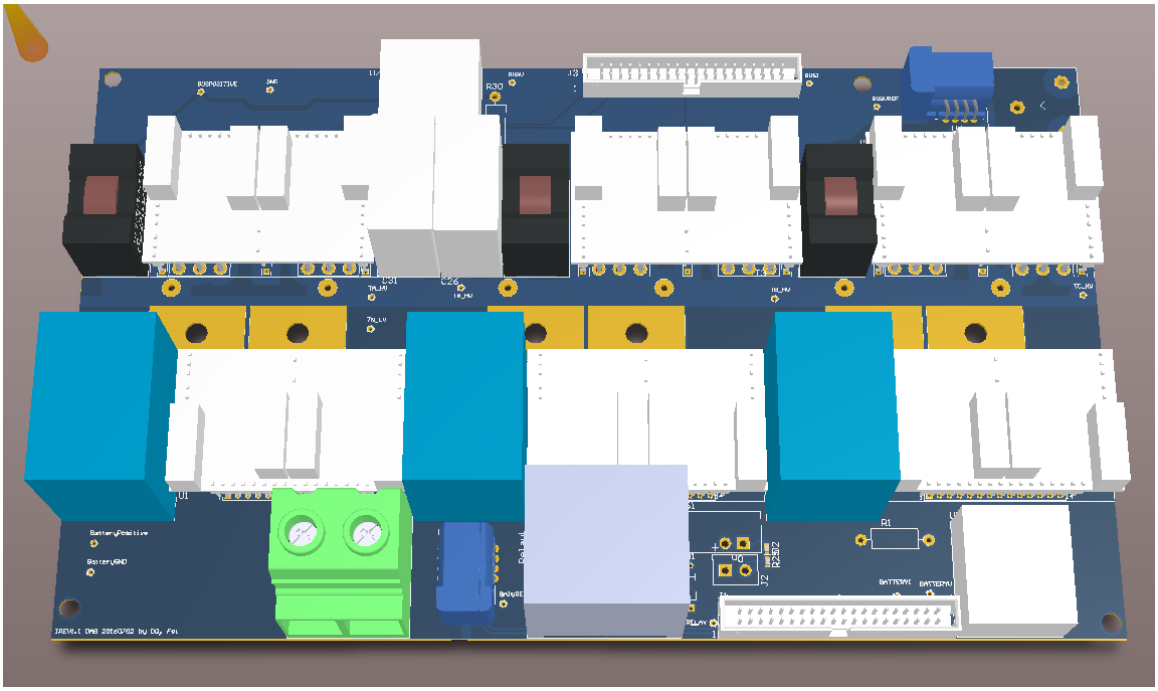


Figure B.5: 3D PCB model of the DAB part in Prototype 2.

The high-frequency transformers are designed by Cui Ying and more detailed can be found in (Cui Ying, 2017). The core of the transformer select N87 Ferrite material from Epcos. To achieve a planar application, EE 64/10/50 core dimension is selected. The copper thickness of the primary and secondary PCB winding is 0.175mm and PCB substrate (FR4) thickness is 0.3mm. Insulation thickness between PCBs is 0.2008mm. Primary trace width is 18.5mm for potential high current which secondary trace width is 3mm. The terminology and winding stack arrangement can be found in Figure B.6. The assembled transformer can be found in Figure B.7.

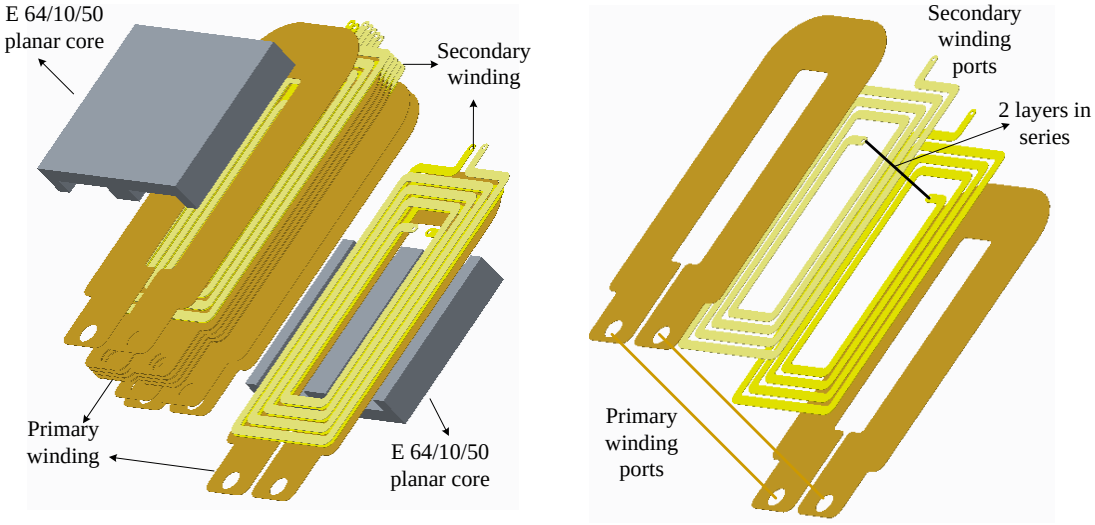


Figure B.6: Terminology and winding stack arrangement of the applied transformer in (Cui Ying, 2017).

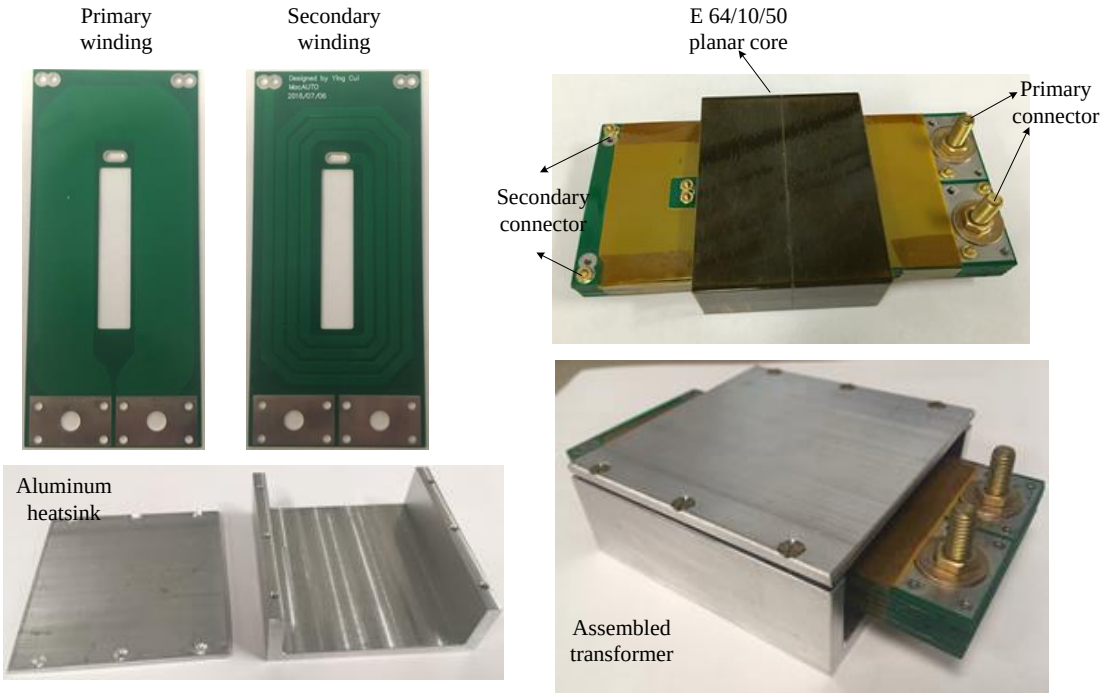


Figure B.7: PCB winding and assembled planar transformer in (Cui Ying, 2017).

The magnetizing inductance of the designed transformer is 803.6μH and the stray resistance converted to the secondary side is 12$m\Omega$. The stray capacitance between primary and seconary side is 3.11nF while the stray capacitance of the secondary is 3.16nF.

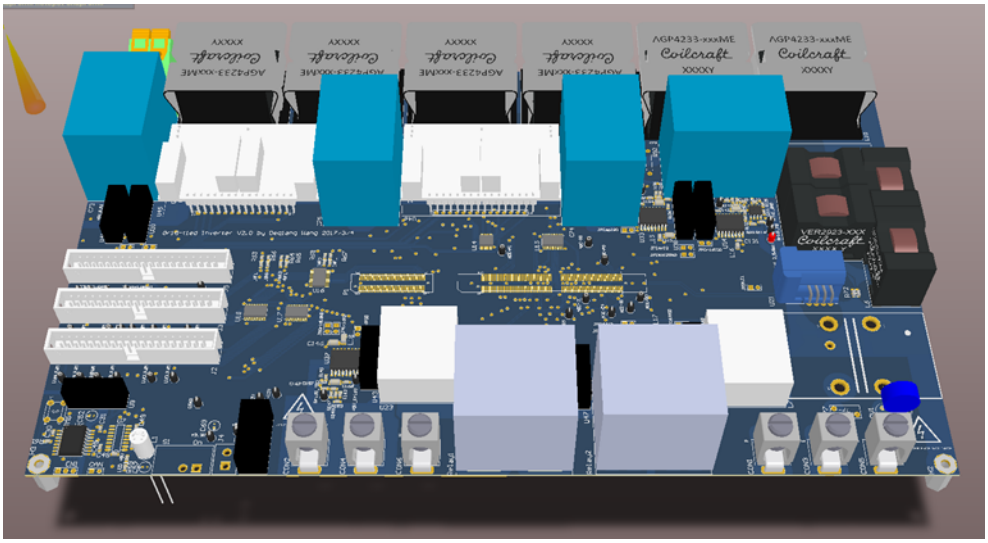


Figure B.8: 3D PCB model of single-phase inverter with controller interface.

The single-phase LCL inverter is built as Figure B.8. Moreover the controller interface is incorporated in the inverter board. To reduce the EMI coupling noise, Sigma Delta Filter Module (SDFM), AMC1204DW, is utilized in stead of regular ADC chip for the grid voltage and current sensing. Software protection is also considered and designed by CMPSS module for ADC signals and comparator unit for SDFM signals. Also the software protection scripts are in the main 100kHz interrupt to ensure quick action.

The experiment setup of the prototype is shown as Figure B.9. One of the future work is to design the final prototype merging the separated PCBs of the Prototype 2 into one PCB as Prototype 1.

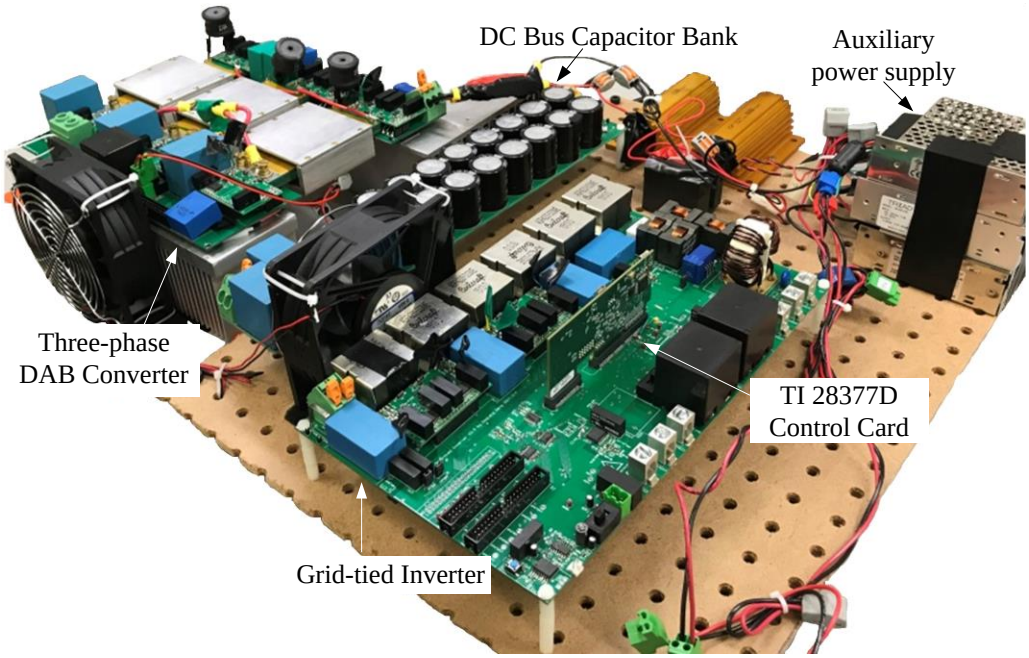


Figure B.9: Experiment setup of the Prototype 2.

B.2 Upper-Level GUI Software

A upper level GUI software is designed as Figure B.10 by $C^{\#}$. The CAN communication is used to exchange information between the upper level controller and downstream controller. Basic hardware information such as battery voltage and current, grid voltage and current, board status and fault codes is updated through CAN message with 100Hz. State machines are designed with ON, OFF, Soft-start and Fault status. Anti-islanding is considered by detect grid voltage frequency and grid voltage distortion by the firmware not the details are beyond the scope of the thesis.

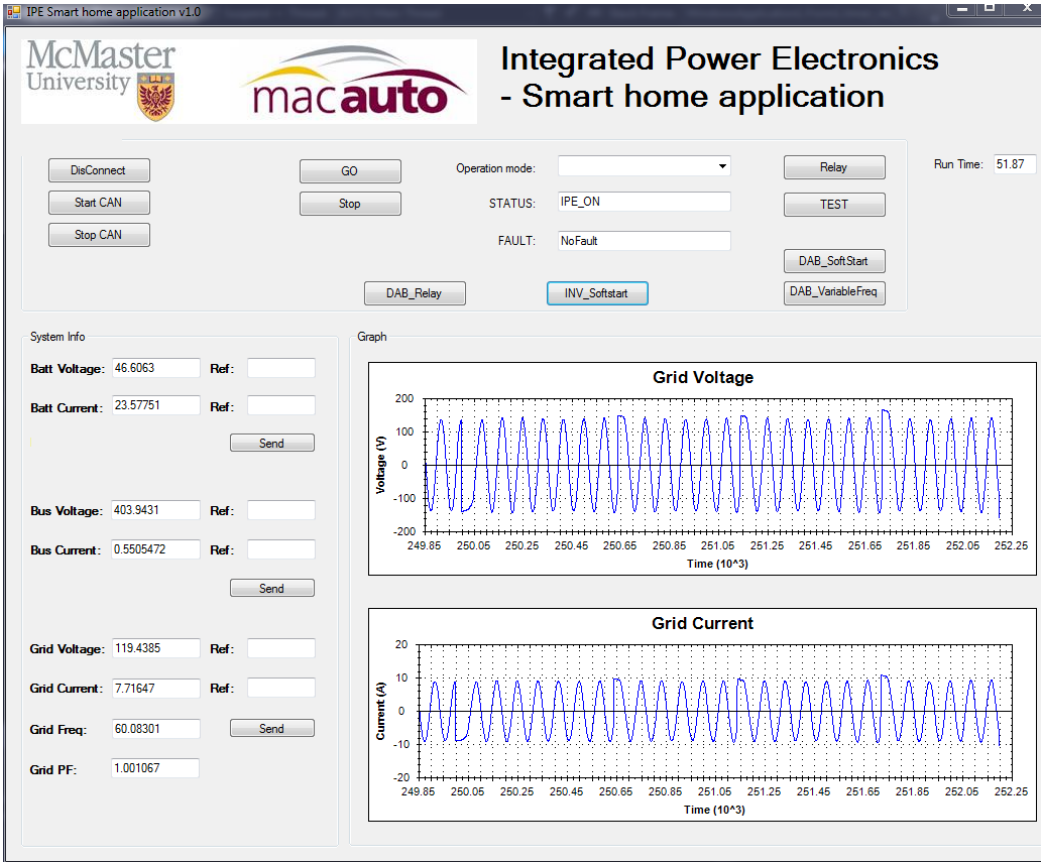


Figure B.10: Upper-level GUI software.

B.3 Soft-Start of the System

In case of soft-start in the system, ramp up and increasing switching frequency are utilized. To control the in-rush current, 1s ramp up is applied to control the output voltage reference of the three-phase DAB converter as Figure B.11. On the other hand, the huge transient transformer current will be resulted from large voltage difference across the leakage inductance of transformer during start state when the HV side voltage is much lower than nV_{Batt}. One solution is to increase the switching frequency during start state to mitigate the transient transformer current as Figure B.11. When the DC bus voltage is around 400V in our case, the switching frequency is back to operation frequency as 100kHz. The illustration of this idea is shown as Figure B.12. For safety concerns, a down-scale experiment is done which the input voltage 10V while the output voltage is 80V. The transient transformer current i_A with 200kHz soft-start is much slower than it with 150kHz soft-start as Figure B.12.

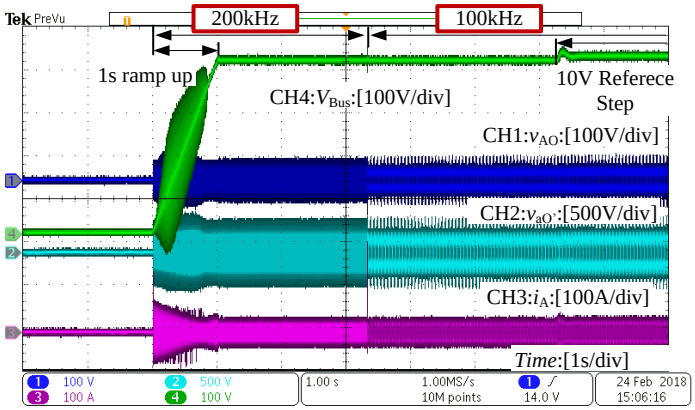


Figure B.11: Soft-start applied in the system.

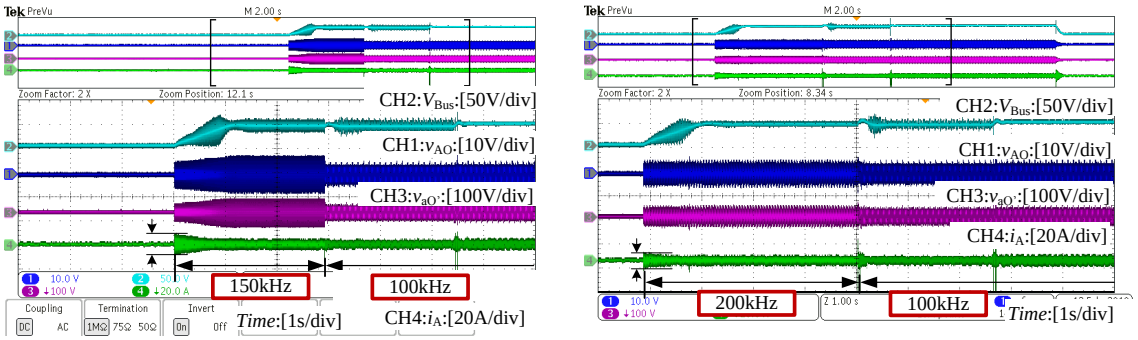


Figure B.12: Transformer current impact comparison during soft-start with difference switching frequency: (a) 150kHz soft-start. (b) 200kHz soft-start.

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