A MCU-CONTROLLED PHOTOVOLTAIC SYSTEM WITH MAXIMUM POWER POINT TRACKER

A MCU-CONTROLLED PHOTOVOLTAIC SYSTEM WITH MAXIMUM POWER POINT TRACKER

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ABSTRACT

Given the growing concern over climate change, air pollution, rising energy prices, and the uncertain reliability of conventional fuel sources, solar power has become more popular in a variety of applications. Solar power is free, safe, abundant, renewable, and has few negative impacts on the environment.

The photovoltaic array is substantially influenced with unpredictable environmental conditions (sun illumination and array temperature), which in turn, results in nonlinear Voltage-Current (or Power-Voltage, Power-Current) characteristics. These characteristics make it difficult to estimate the maximum power operating point. To extract the maximum power available from photovoltaic (PV) arrays on a continuous basis, a device called the Maximum Power Point Tracker (MPPT) is needed to continuously deliver the highest possible power to the load given unpredictable variations in environmental conditions.

The PV system used in our experiment has a maximum 300W capability. Two sets of PV arrays are used in parallel to demonstrate the scalability of the system; each branch consists of three series-connected PV modules that are individually rated at 50W. Two DC-DC buck-type converters are implemented. A 24V battery bank is used as a power storage unit and is also connected to the load. An MC-based 56F8013 and its demonstration board from Freescale are employed to implement different MPPT control schemes, with multiple-PWM channels. The design can therefore adequately handle two main independent switches for each power converter.

Several MPPT control algorithms are validated and comparatively analyzed in both indoor and outdoor experiments in real time. A new control strategy (called Adaptive Hill-Climbing) is proposed as a modified version of the conventional Hill-Climbing method using an optimally adaptive power window. Other methods including dp/dv method and IncCond method are also implemented in the PV system. The experimental investigation is conducted using these control topologies to seek continuously varying Maximum Power Point (MPP) from solar arrays. The experimental results show that the new proposed control method strongly outperforms the other methods.

This thesis shows that the proposed MPPT can increase the power generated by PV arrays by up to at least 30% more than a PV system without an MPPT. The proposed MPPT system is adaptive to environmental disturbances; it is flexible and can be expanded to an N-parallel PV system.

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NOMENCLATURE

A	Ampere
AC	Alternative current
A/D	Analog to digital
ADC	Analog to digital converter
Ah	Ampere hour
ASM	Assembly language
A_c	Area of a conductor
A_l	Current loop area
B	Magnetic field density
C	Capacitor
CCM	Continuous current mode
CPU	Central processing unit
CV	Constant voltage
C_{bypass}	Bypassing capacitor
C_{ds}	Drain-to-source capacitance
C_g	Total gate capacitance in a MOSFET
C_{gs}	Gate-to-source capacitor of a MOSFET
C_p	Parasitic/Sum of junction capacitor of a MOSFET and the capacitor due to trace

C_{in}	Input filtering capacitor/capacitance (μF)
C_{in1}	Input filtering capacitor/capacitance 1 (μF)
C_{in2}	Input filtering capacitor/capacitance 2 (μF)
C_{iss}	MOSFET input capacitance (pF)
C_{oss}	MOSFET output capacitance (pF)
C_{out}	Output filtering capacitor/capacitance (μF)
C_{out1}	Output filtering capacitor/capacitance 1 (μF)
C_{out2}	Output filtering capacitor/capacitance 2 (μF)
D	Freewheeling diode
DAC	Digital to analogy converter
DCM	Discontinuous current mode
DC	Direct current
DSC	Digital signal controller
DSP	Digital signal processing
D1	Freewheeling diode 1
D2	Freewheeling diode 2
Db	Blocking diode
d	Distance between the two adjacent conductors
d_1	Duty cycle 1 when the switch (MOSFET) is on
d_{1_max}	Maximum duty cycle when the switch is on

d_{1_mim}	Minimum duty cycle when the switch is on
d_2	Duty cycle 2 when the switch is (MOSFET) off
d_{2_max}	Maximum duty cycle 2 when the switch is on
d_{2_mim}	Minimum duty cycle 2 when the switch in on
E	Electric field
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
ESL	Equivalent series inductance (mH)
ESR	Equivalent series resistance (Ω)
ESR_{MAX}	Maximum equivalent series resistance (Ω)
E_{t_off}	Switching energy loss during turn-off time
E_{t_on}	Switching energy loss during turn-on time
f_c	Cut-off frequency (Hz)
f_{SW}	Switch frequency or operational frequency (Hz)
G	Sun illumination
GaAsP	Gallium arsenide phosphide, is a semiconductor material
g	Conductance
Δg	Incremental conductance
I	Current (A)
IC	Integrated circuit

IDE	International development enviornment
IGBT	Insulated gate bipolar transistor
IncCond	Incremental conductance
I_a	Array current
I_c	Solar cell terminal current
I_C	Current going though the output filtering capacitor
I_{C1}	Current going though the output filtering capacitor 1
I_{C2}	Current going though the output filtering capacitor 2
I_D	Drain current
I_d	Current going throughput a freewheeling diode
I_{MOSFET}	Current at the maximum power point
I_{mpp}	Average maximum output current in one buck converter
$I_{O(MAX)}$	The maximum inductor current
I_{op}	The current going through the operational amplifiers
I_{ph}	Photon generated current or light induced current
I_{reg}	Voltage regulator current
I_{SC}	Short circuit current solar cell
$I_{SC(T1)}$	Short circuit current solar cell art T1
$I_{SC(T2)}$	Short circuit current solar cell at T2

I_{s1}	Saturation current due to diffusion mechanisms (diode saturation current)
I_{s2}, I_0	Saturation current due recombination in space – charge layer
I_{in}	Input current
$I_{in(RMS)}$	Input capacitor RMS current rating
I_{in1}	Input current 1
I_{in2}	Input current 2
I_{L_max}	Maximum output current going through the inductor
I_{L1_max}	Maximum output current going through the inductor 1
I_{L2_max}	Maximum output current going through the inductor 2
I_{L_min}	Minimum output current going through the inductor
I_{L1_min}	Minimum output current going through the inductor 1
I_{L2_min}	Minimum output current going through the inductor 2
I_{out}	Total output current
I_{out1}	Output current 1
I_{out2}	Output current 2
I_{L1}	Output current going through the inductor 1
I_{L2}	Output current going through the inductor 2
I_{RMS}	Root mean square current
i_L	Output current going through the inductor

ΔI	Current difference
$\Delta I_L, \partial I_L$	Inductor current ripple
$\Delta I_{L\_\max}$	Maximum inductance ripple
$\Delta I_{L\_\min}$	Minimum inductance ripple
K_0	Temperature coefficient
k	Boltzmann constant $1.38\times10^{-23}(J/K)$
L	Inductor (mH)
LED	Light emitting diode
$L_{Leakage}$	Circuit's intrinsic leakage inductance
$L_{\max}$	Maximum inductance (mH)
$L_{\min}$	Minimum inductance (mH)
l_m	Effective magnetic path length
MOSFET	Metal-oxide-semiconductor field-effect transistor
MOSFET1	Metal-oxide-semiconductor field-effect transistor 1
MOSFET2	Metal-oxide-semiconductor field-effect transistor 2
MPP	Maximum power point
MPPT	Maximum power point tracker
N	Sampling number
N_s	The number of PV cell connected in series
N_{sh}	The number of PV cell connected in parallel

n	Diode quality factor or ideality factor, variable with cell types, general between 1 and 2
P	Power
PCB	Printed circuit board
PID	Proportional integral derivative control
PWM	Pulse width module
P&O	Perturbation and observation
PV	Photovoltaic
$P_{C_{OSS}}$	Power loss due to MOSFET output capacitance
P_D	Maximum power consumption in a MOSFET
P_{diode}	Total power loss of a diode
P_{drive}	MOSFET power consumption in its driving circuit
P_{d_cond}	Diode power loss due to conduction
P_{d_rev}	Diode power loss due to reverse recovery
P_{in}	Input power
P_{MOSFET}	Total MOSFET power loss
P_{max_ref}	Maximum power point reference
$P(n)$, $P(n)'$	The next power sampling point
P_{out}	Output power
P_{reg}	Total power loss in a regulator

$P_{R_{DS}}$	Heat power loss due to drain-to-source resistance
$P_{R_{sn}}$	Power loss in a snubber resistor
P_{SW}	Total switching power loss of a MOSFET
P_{window}	The adaptive power window
Q	Amount of heat or total power loss of the device, such as MOSFET (W)
Q_g	Total gate charge (C)
Q_{rr}	Reverse recovery charge (nC)
q	Electron charge $1.6\times10^{-19}(C)$
R	Resistor or load
RC	Multiplication of R and C is time constant
RMS	Root mean square
$R_{DS(ON)}$	Drain-to-source resistance
R_f	Feedback resistor
R_g	Gate resistance of a MOSFET
R_{gs}	Gate-to-source resistance of a MOSFET
R_{limit}	Resistor used for limiting current
R_s	Internal series resistance per cell (Ω)
R_{sh}	Internal shunt resistance per cell (Ω)
$R_{\theta CS}$	Thermal resistance of interface material (usually, silicon grease) (°C/W)

$R_{\theta JC}$	Thermal resistance of device (°C/W)
$R_{\theta JA}$	Thermal resistance of Junction-to-Ambient (°C/W)
$R_{\theta sa}$	Thermal resistance of the heat-sink (°C/W)
R_1	Resistor 1
R_2	Resistor 2
r	Ratio
S	Effective area
SW	Switch
T_a	Ambient fluid temperature or absolute cell temperature (K)
T_c	Cut-off period
$T_{j\max}$	Maximum allowable junction temperature
T_{SW}	Switch (MOSFET) period
T1	Reference temperature (°C)
T2	Temperature 2 (°C)
$t_{d(on)}$	MOSFET turn-on delay time
$t_{d(off)}$	MOSFET turn-off delay time
t_{on}	MOSFET turn-on time
t_{off}	MOSFET turn-off time
t_{rise}	Rise time of a MOSFET

t_{fall}	Fall time of a MOSFET
V	Voltage
V_a	Array voltage
V_C	Solar cell terminal voltage
V_{CS}	Output voltage of a Hall-effect current sensor
V_{cc}, V_{ss}	Voltage supply for digital circuits
V_{CC_min}	The minimum voltage supply
V_D	Allowable voltage across a diode
V_{DS}	Drain-to-source voltage of a MOSFET
V_{drive}	MOSFET's driving voltage
$V_{forward}$	Forward voltage of a diode
V_g	Band gap for silicon 1.11 (eV)
V_{gs}	Gate-to-source voltage of a MOSFET
$V_{GS(th)}$	MOSFET's threshold voltage
V_L	Inductor voltage
V_{mpp}	Voltage at the maximum power point
V_{MOSFET}	Allowable voltage across a MOSEFET
V_{in}	Input voltage
V_{in1}	Input voltage 1

V_{in2}	Input voltage 2
V_{OC}	Open circuit voltage of solar cell
V_{out}	Output voltage
$V_{out\_\max}$	Maximum output voltage
$V_{out\_\min}$	Minimum output voltage
V_{o1}	Output voltage1
V_{reg}	Voltage regulator voltage
V_{RMS}	Root mean square voltage
ΔV	Voltage difference, or voltage ripple
ΔV_{in}	Input voltage ripple in the input filtering capacitor
$\Delta V_{in\_\min}$	Minimum Input voltage ripple in the input filtering capacitor
$\Delta V_{in\_\max}$	Maximum Input voltage ripple in the input filtering capacitor
ΔV_{out}	Output voltage ripple in the output filtering capacitor
Xv	Term symbol
Xv_p	Term symbol
x_i	The i^{th} sampled data
$\bar{x}$	The averaged sampled data

Greek symbols

ε_0	Vacuum permittivity

ε_r	Relative permittivity
εmf	Electromotive force
μ_0	Permeability of Vacuum
ω_o	Cut-off angular frequency (rad/s)
φ_m	Magnetic flux

Chapter 1
Introduction

1.1 Background

Shifts from glacial to interglacial periods have generally occurred over thousands of years. Carbon dioxide levels have doubled in roughly several decades according to [1], and that, theoretically, could be just the beginning. Carbon dioxide emissions have increased dramatically in recent decades. With the rapid growth of new technologies, carbon dioxide and other pollutants have many source (electricity, fossil fuels, chemicals etc.), and some of these pollutants are the main source of a buildup in the atmosphere of greenhouse gases. With the fear of sudden climate shift, it is an incentive for people to invest in alternative energy sources.

Besides pollution problems with conventional energy sources (like fossil fuels) that we use daily, these resources are finite. Solar energy on the other hand, is constantly replenished by the sun for free. Solar is a promising energy source for meeting currently ever-increasing demand.

There are two basic methods of conversion between solar radiation and electricity for terrestrial applications: thermal and photovoltaic. Thermal (or passive solar) conversion uses the energy of photons received from the sun to produce heat, and then uses conventional technology to convert the heat to electricity [2]. In contrast photovoltaic conversion attempts to transform all the energy of the photons into electricity directly (it bypasses thermodynamic cycles and mechanical generators

altogether) by taking advantage of the intrinsic photovoltaic (PV) effect, which can be best realized in layers of modern semiconductor materials [2].

Even though the sun has no detrimental impact on our environment, and the PV cells themselves produce no air pollution or hazardous waste, there are potential pollution hazards caused by the semiconductor materials used in the PV cells and in the process of producing PV cells. Manufacturing PV cells in turn require input of energy, and this energy is provided by conventional energy (fuels) [3]. However, as the development of new thin film PV technologies comes into use, and the scale of production increases, the energy input to manufacture PV systems will decrease considerably, with consequent reduction in carbon dioxide emissions, to levels below that of conventional electricity generating technologies [3]. Due to the low utilization efficiency of a PV cell (generally around 12%), it is important to use maximum power point trackers (MPPTs) in PV systems in order to boost or enhance overall system efficiency.

1.2 Research Motivation and Objectives

The motivation of this research is to build up knowledge about photovoltaic (PV) systems. In particular, this study deals with the process of digitally controlled Maximum Power Point Tracker (MPPT) design and comparisons among different MPPT control schemes in a stand-alone PV system with relatively high system efficiency and stability. The recommendations made are directly related with real world issues, and different hardware designs are experimented with and analyzed. A final hardware design solution is then proposed, several MPPT control algorithms are employed and compared, and

eventually a typical PV system is setup and tested to confirm the whole system design validity.

1.3 Contributions

The contribution of this research concerns power electronic issues, such as the selection of power component, driving circuit, isolation, and PCB layout. An experimental MPPT prototype with the control chip 56F8013 and its demonstration board from Freescale in a stand-alone PV system has been developed and tested in real time under different weather conditions. The experimental results with different control strategies and final conclusion are shown and discussed at the end. Some of the ideas published in the literatures have not been found to be necessarily correct. The basic concept has a wide variety of electric power application.

1.4 Overview

Chapter 2

Several mathematical photovoltaic (PV) or solar cell models are analyzed, discussed and compared. The various impacts on solar cell and the maximum power point (MPP) of solar array are described in detail along with matlab-generated diagrams. Finally some issues in the PV array connection and their solutions are commented upon.

Chapter 3

The aim of this chapter is to understand the main control algorithm and structure of the entire PV system. The reasons why we need maximum power point tracker (MPPT) are briefly explained. An overview of several different concepts behind MPPT

control algorithm is presented and compared. In addition the proposed basic configuration of MPPT is selected, discussed and mathematically developed with practical considerations. PV system classifications are finally reviewed.

Chapter 4

The detailed component selections and calculations in the proposed power stage circuit are presented. Similarly components in the control circuits and conditioning circuits are also discussed. Experiments to further investigate the functionality of designed circuits are performed as they are developed, then all the circuit designs are finalized. A printed circuit board (PCB) is presented along with the discussion of layout design issues. The MC-based 56F8013 chip and its demonstration board from Freescale Company are briefly described.

Chapter 5

A main system software flowchart is shown and explained; the code is written and compiled in the CodeWarrior™ development environment. Several MPPT control methods and the proposed control algorithms are actually developed and implemented in the proposed MPPT system.

Chapter 6

The designed close-loop system by using PV emulator is initially developed and investigated. The experimental results are first presented and analyzed based on the indoor system performances. Ultimately a stand-alone PV system with the designed MPPT controller is constructed and validated in a natural environment. The experimental

results are collected, presented and compared based on the overall system performances under various climate conditions. A conclusion is finally drawn proposed.

Chapter 7

Final comparison between theory and actual experimental results are summarized and possible investigations and MPPT system improvements in the future are suggested.

Chapter 2

Photovoltaic Modeling and its Characteristics

2.1 Introduction

A solar cell or photovoltaic cell consists of semiconductor material, which converts sunlight into DC current using the photovoltaic effect. Photovoltaic energy conversion in solar cells generally consists of two steps. First, absorption of light generates an electron-hole pair. The electron and hole are then separated by the structure of the device-electrons to the negative terminal and holes to the positive terminal thereby generating electrical power [4].

A solar cell consists of a p-n junction fabricated in a thin wafer or layer of semiconductor. In the dark (no illumination), the I-V curve output characteristic of a solar cell has an exponential characteristic similar to the performance of a diode. When exposed to sunlight, photons with energy greater than the band gap energy of the solar cell material are absorbed and electron-hole pairs are formed. These mobile carriers are swept apart under the influence of the internal electric field of the p-n junction depletion layer and thus create a current proportional to the incident radiation [4]. There are two basic circuit conditioning scenarios for the actual PV cell and for its equivalent circuit. Firstly when the cell is connected to a load, the current flows in the external circuit; secondly when the cell is open circuited, then the current becomes shunted internally by the intrinsic p-n junction diode.

2.2 The Ideal Photovoltaic Cell

An ideal solar cell can be represented by a light induced current source, which is due to the separation and drift of the photon-generated electron–hole pairs under the influence of the built-in field, connected in parallel with a rectifying diode, as shown in the equivalent circuit of Fig. 2.1.

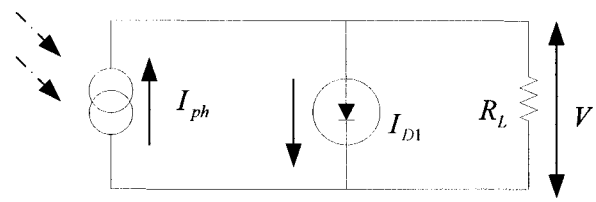


Fig. 2.1 Ideal Equivalent Circuit Model of a Solar Cell

The corresponding I-V characteristic is described by equation (2.1) [4]:

$$I_C = I_{ph} - I_{D1} = I_{ph} - I_{s1}\left[e^{\frac{qV_C}{kT_a}} - 1\right] \qquad (2.1)$$

Here, I_{ph} represents photon generated current or light induced current (linear with illumination), I_{D1} represents the diode current that flows through the p-n junction diode, I_{s1} represents reverse saturation current due to the diffusion mechanism. This is also called diode saturation current, since a solar cell in the dark is simply a semiconductor current rectifier, or just a diode [4]. The symbol q represents electron charge $1.6\times10^{-19}C$, k is Boltzmann's constant $1.38\times10^{-23}J/K$, T_a represents ambient temperature (K), V_C is the solar cell terminal voltage, and I_C is the solar cell terminal current.

In the ideal case, the short circuit current I_{SC} is equal to the photo-generated current I_{ph}, and the open circuit voltage V_{OC} can be solved from equation (2.1) and expressed in equation (2.2):

$$V_{OC} = \frac{kT_a}{q} \ln(1 + \frac{I_{ph}}{I_{s1}}) \qquad (2.2)$$

2.3 The Practical Photovoltaic Cell

A double-exponential mathematical model shown in equation (2.3) represents an I-V characteristic of a practical solar cell, and its equivalent circuit diagram is illustrated in Fig. 2.2. The equation is derived based on the physics of the p-n junction and is generally accepted as reflecting the behavior of the cells that especially are constructed from polycrystalline silicon [5]. Equation (2.4) provides a better fit to the crystalline or amorphous type cells simply setting I_{S1} to zero from equation (2.3) [5]. Given the problems of existing parasitic components, the solar cell generally contains series and parallel resistances (also shown in Fig. 2.2 [6]). Including all the above elements, equation (2.1) needs to be further developed to mathematical models of equation (2.3) or (2.4) according to their physical properties.

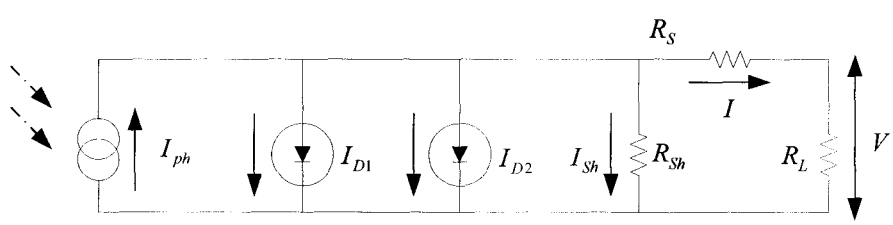


Fig. 2.2 Practical Equivalent Circuit Model of a Solar Cell

$$I_C = I_{ph} - I_{s1}\left[e^{\frac{q(V_C+IR_S)}{kT_a}} - 1\right] - I_{s2}\left[e^{\frac{q(V_C+IR_S)}{nkT_a}} - 1\right] - \frac{V_C + I_C R_S}{R_{sh}} \quad (2.3)$$

$$I_C = I_{ph} - I_{s2}\left[e^{\frac{q(V_C+IR_S)}{nkT_a}} - 1\right] - \frac{V_C + I_C R_S}{R_{sh}} \quad (2.4)$$

Where I_{s2} represents saturation current due to recombination in space-charger layer, n represents diode quality factor usually between 1 and 2. Instead of equation (2.3), this factor can be introduced in the single-diode equation [4]. The symbol R_s represents the intrinsic series resistance per cell, and R_{sh} represents the intrinsic shunt resistance per cell.

2.4 The Simplified Mathematical Model for a Photovoltaic Cell

The simplified equivalent circuit model of a solar cell is a current source in parallel with only one diode. As illustrated in Fig. 2.3, the I_{ph} represents a temperature dependent photon generated current.

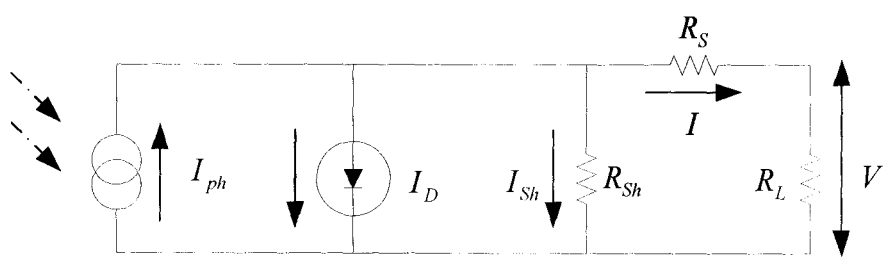


Fig. 2.3 Simplified Equivalent Circuit Model of a Solar Cell

The series resistance R_s has a significant contribution to both of the slope of an I-V curve and the position of the maximum power point. In contrast, the shunt resistance R_{sh} has less effect on the position of the maximum power point [7] (The above effects are all proven in the latter of this chapter). The previous equation (2.4) now can be written as equation (2.5), where I_0 represents I_{s2} the saturation current due to recombination in space-charger layer.

$$I_C = I_{ph} - I_0\left[e^{\frac{q(V_C+IR_S)}{nkT_a}} - 1\right] - \frac{V_C + I_C R_S}{R_{sh}} \qquad (2.5)$$

2.5 From Cell to Module to Array

Since one cell voltage is very small, it must be connected to several cells in series in order to build up the terminal voltage. A certain number of cells in series are called a module. Generally, one module includes 36 to 72 cells in series. For large power systems, multiple modules, in turn, can be connected in series to further increase output voltage, and in parallel to increase output current. A combination connection of series and parallel modules is referred to as an array [8].

We can generalize the PV array equivalent circuit as described above, and then an overall multidimensional array simplified model is shown in equation (2.6):

$$I_a = N_{sh}\left\{I_{ph} - I_0\left[e^{\frac{q(V_C+I_C R_S)}{nkT_a}} - 1\right] - \frac{V_C + I_C R_S}{R_{sh}}\right\} \qquad (2.6)$$

Where N_{sh} is the number of PV cells connected in parallel, N_s is the number of PV cells connected in series, V_a represents array voltage ($V_C = V_a / N_s$), and I_a represents array current ($I_C = I_a / N_{sh}$).

2.6 The Impacts of Internal Series and Shunt Resistances of PV Array

By using the simplified general PV mathematical model (equation 2.6) as shown in the previous section, and parameter information provided from US-64 module datasheet [9], the following plots are generated by MATLAB 7.1 in order to investigate the impacts of the internal series and parallel resistances on PV cells or PV modules.

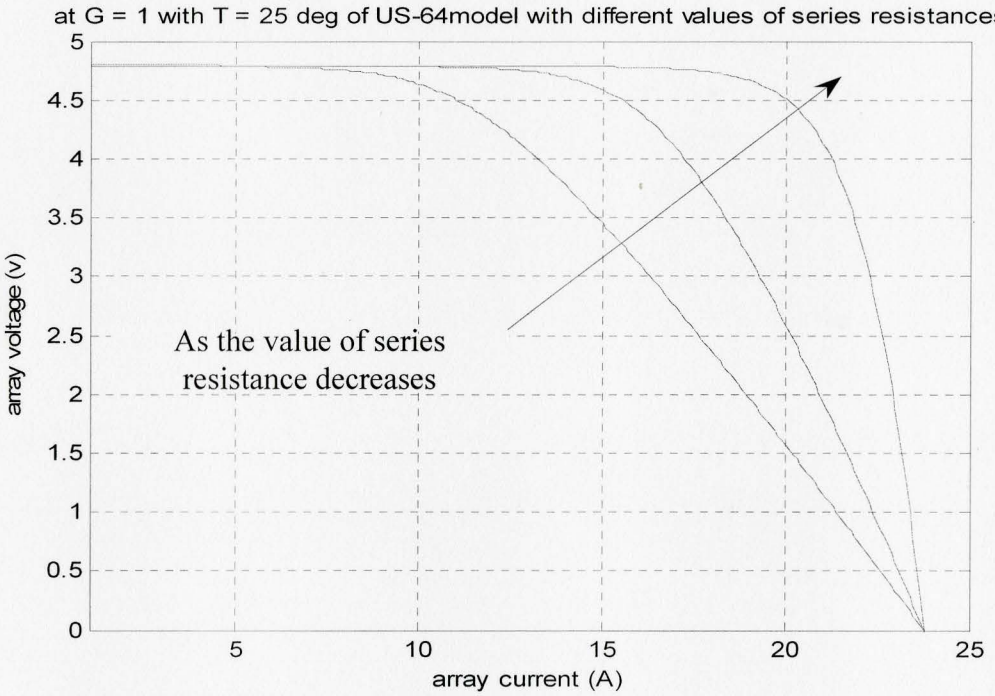


Fig. 2.4 I-V Curve of US-64 with Different Values of Series Resistances

As shown in the Fig. 2.4, given the condition of very large shunt resistance, the series resistance R_s has a huge impact on the slope of the I-V curve at V $= V_{OC}$. We can

observe that as the series resistance becomes smaller, the slope of the IV curve at open circuit voltage becomes steeper. Under the same assumption, Fig. 2.5 shows that the series resistance R_s has a significant impact on the position of the maximum power point as well. Therefore, we can conclude that as the internal series resistance decreases the maximum power point increases and vice versa.

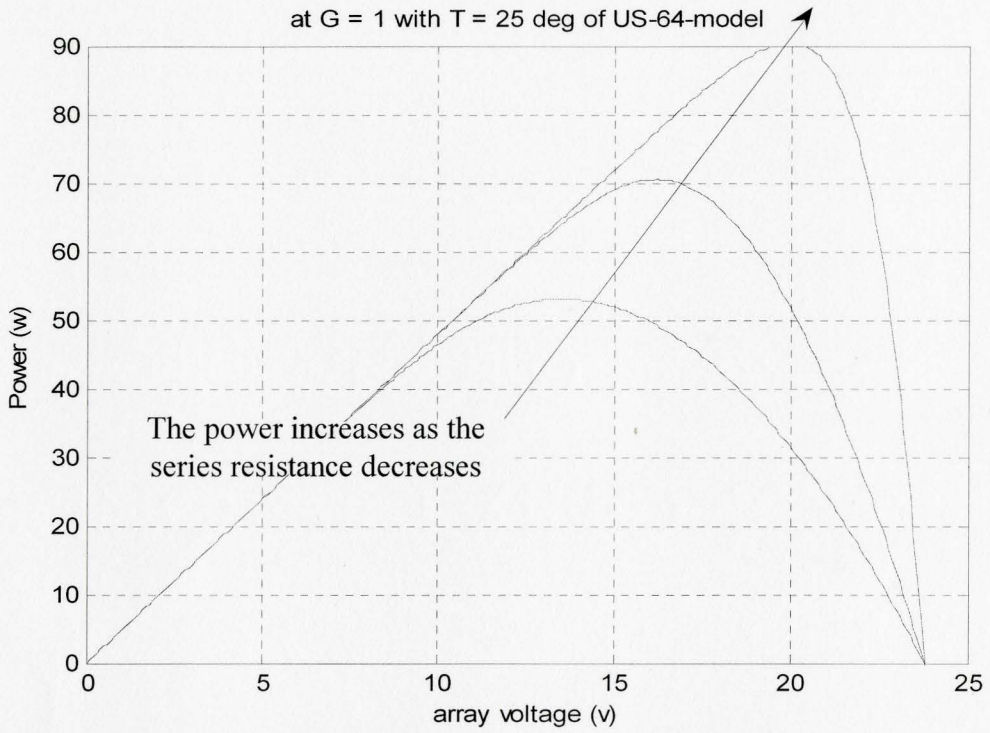


Fig. 2.5 P-V Curve of US-64 with Different Values of Series Resistances

In contrast the shunt resistance has less effect on the slope of the I-V curve at I $= I_{SC}$, as is shown in Fig. 2.6. Compared with the effect of the series resistance, the shunt resistance has an insignificant effect on the position of the maximum power, as seen in Fig. 2.7.

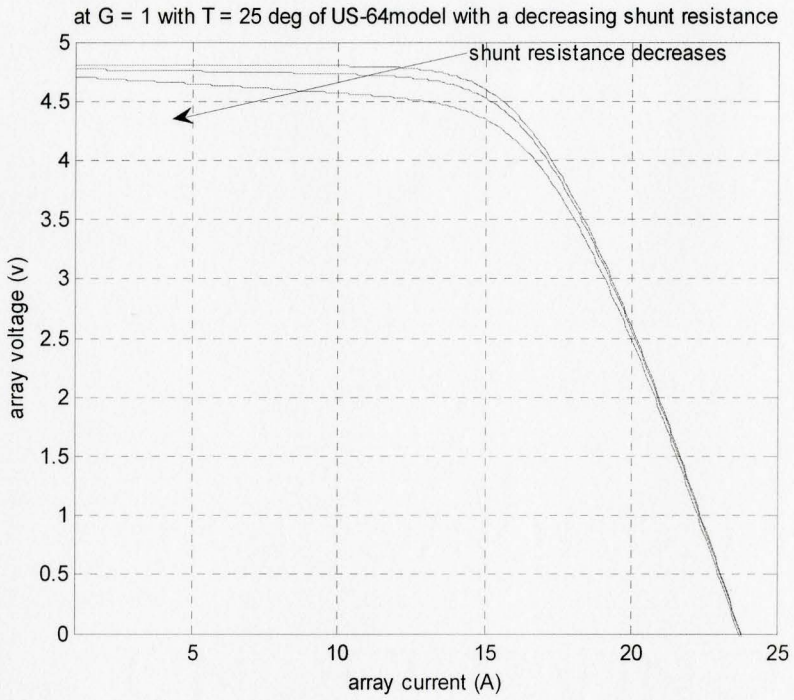


Fig. 2.6 I-V Curve of US-64 with Different Values of Shunt Resistances

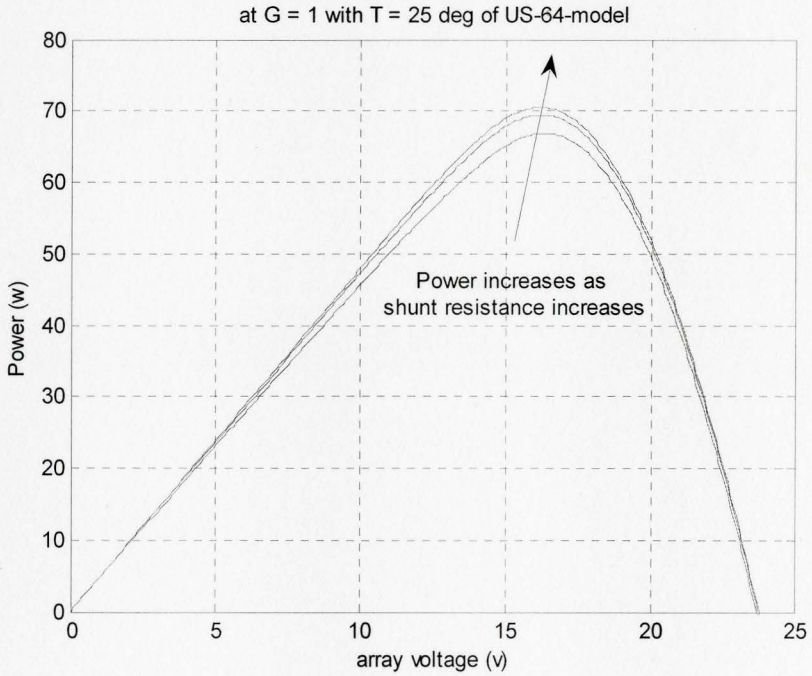


Fig. 2.7 P-V Curve of US-64 with Different Values of Shunt Resistances

In summary since the series resistance reduces the voltage produced by one cell, which ultimately reduces the voltage of one PV module, we can not ignore it. The shunt resistance makes a path and leads currents away from the intended load, and the effect is detrimental to the performance especially at low intensity levels [10]. In other words, the larger the shunt resistance the better the performance of solar cells. Consequently, even though the series resistance is the dominant factor in the PV model, both of the series and shunt resistance has a significant contribution on the position of the maximum power. Imperfections on PV cells have to be taken into account.

2.7 The Impacts of Cell Temperature and Sun Illumination Changes on MPP of PV Array

The following diagrams are based on the same simplified PV mathematical model but the parameters are taken from GEPV050 module datasheet. Since six "GEPV050" modules are adopted in the final proposed PV system experiment, the following matlab-generated diagrams are all based on this GEPV050 module.

From the datasheet, we know that $I_{mpp} = 2.9A$, $V_{mpp} = 17.3V$, $V_{OC} = 22V$, and $I_{SC} = 3.3A$ at the temperature of 25°C [11]. The simulation of I-V curve result of the GEPV050 module at different temperature and illumination is shown in Fig. 2.8. I-V and P-V comparison curves are also shown in Fig. 2.9.

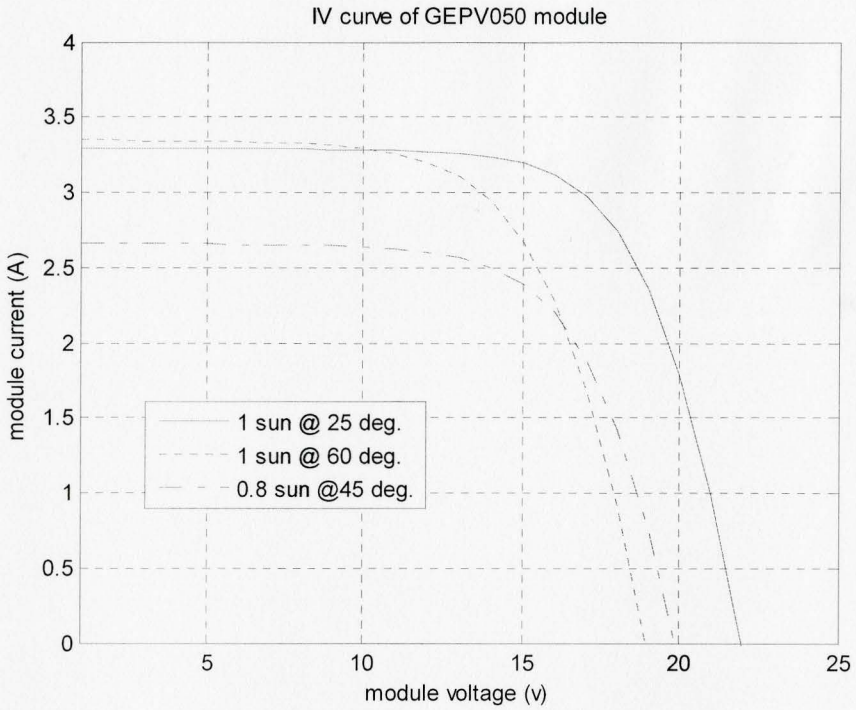


Fig. 2.8 I-V Curve of GEPV050 Module

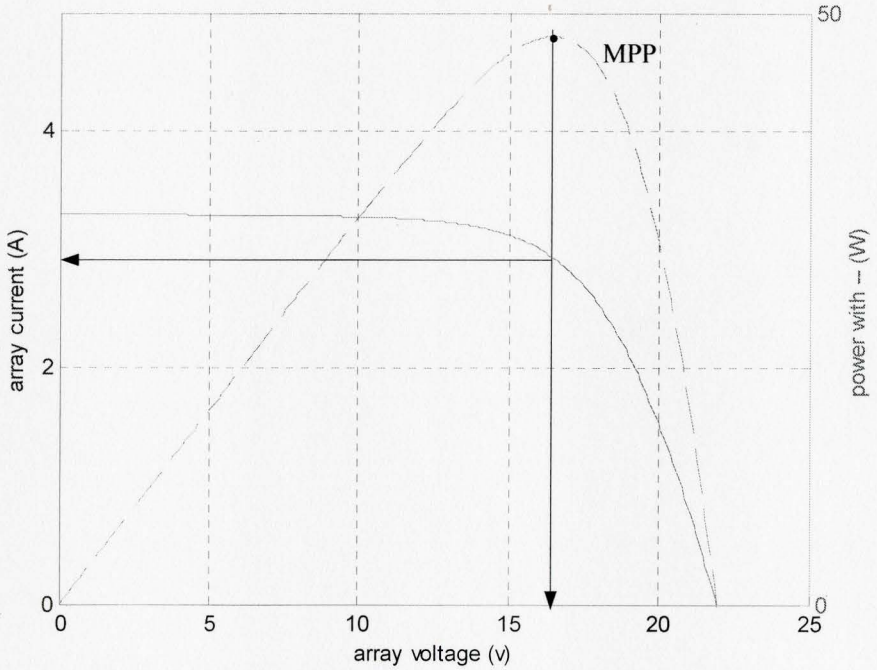


Fig. 2.9 V-I and P-V Characteristic Curves of GEPV050 Module

A maximum power point (MPP) is a point giving the maximum power from a PV array. To visualize this (as illustrated in Fig. 2.9), the MPP is the point on the I–V curve of a PV module that defines the largest possible area of a rectangle under the I-V curve.

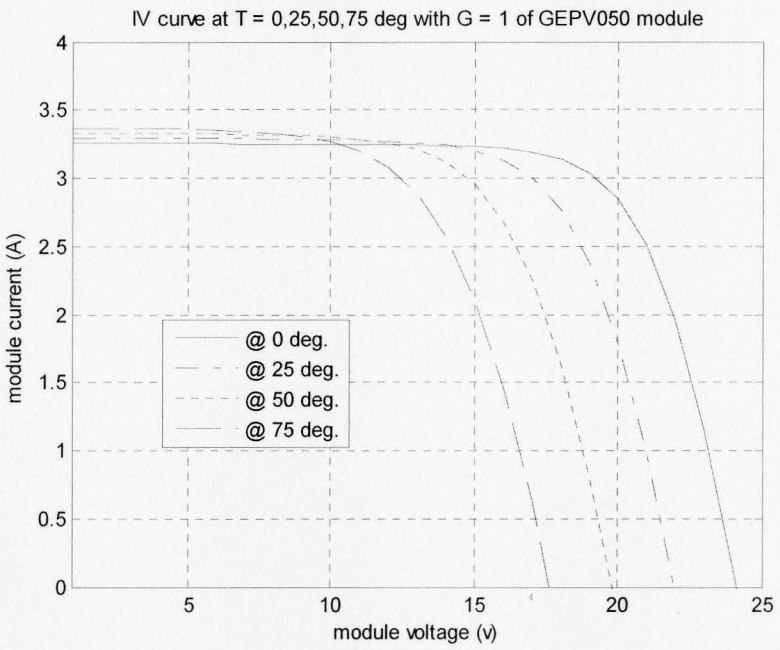


Fig. 2.10 V-I Characteristic Curves with Different Array Temperatures

Furthermore from Fig. 2.10, Fig. 2.11, and Fig. 2.12, they show that when the temperature of the PV module increases from 0°C to 75°C, the voltage V_{mpp} at the MPP decreases drastically. This is because the most pronounced effect of the temperature increase is a decrease in the open circuit voltage Voc, which is due to the reverse saturation current I_0 increasing exponentially with temperature. Overall, with the module temperature increase, the output power of the module at a constant illumination level (G = 1) shifts to lower array voltage [7]. In other words when a PV module gets hot its

maximum output voltage decreases. The hotter the module, the more voltage it loses, in turn the more power it loses.

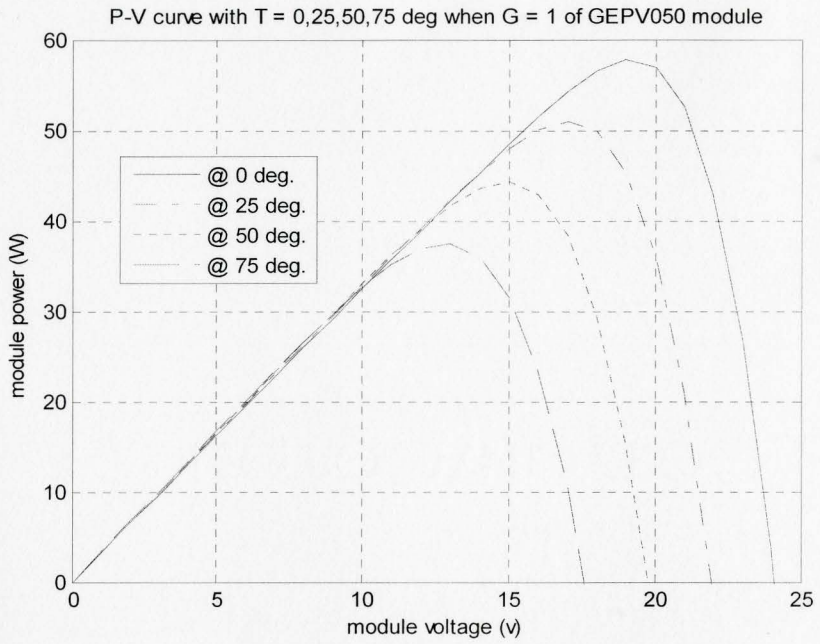


Fig. 2.11 P-V Characteristic Curves with Different Array Temperatures

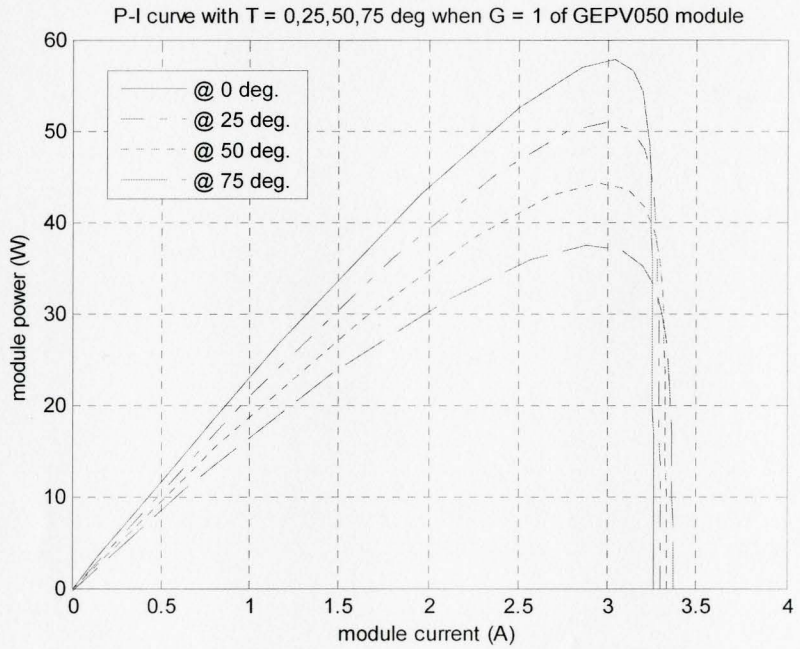


Fig. 2.12 P-I Characteristic Curves with Different Array Temperatures

By changing the sun illumination level G form 1 to 0 with a step of 0.25, the effect of sun intensity on I-V, P-V and P-I curves is shown in Fig. 2.13, Fig. 2.14 and Fig. 2.15 respectively. As the illumination level G decreases, the maximum power point voltage V_{mpp} decreases slightly, whereas the current I_{mpp} available at the maximum power point varies greatly since the short circuit current is proportional to the irradiance [7] as shown in Fig. 2.13. As a result, the position of the maximum power point decreases severely as the illumination is reduced. Overall the voltage at the maximum power voltage V_{mpp} changes are very small with varying irradiance but are largely influenced by changing temperature. The current I_{mpp} varies widely with changing irradiance but considerably less with varying temperature.

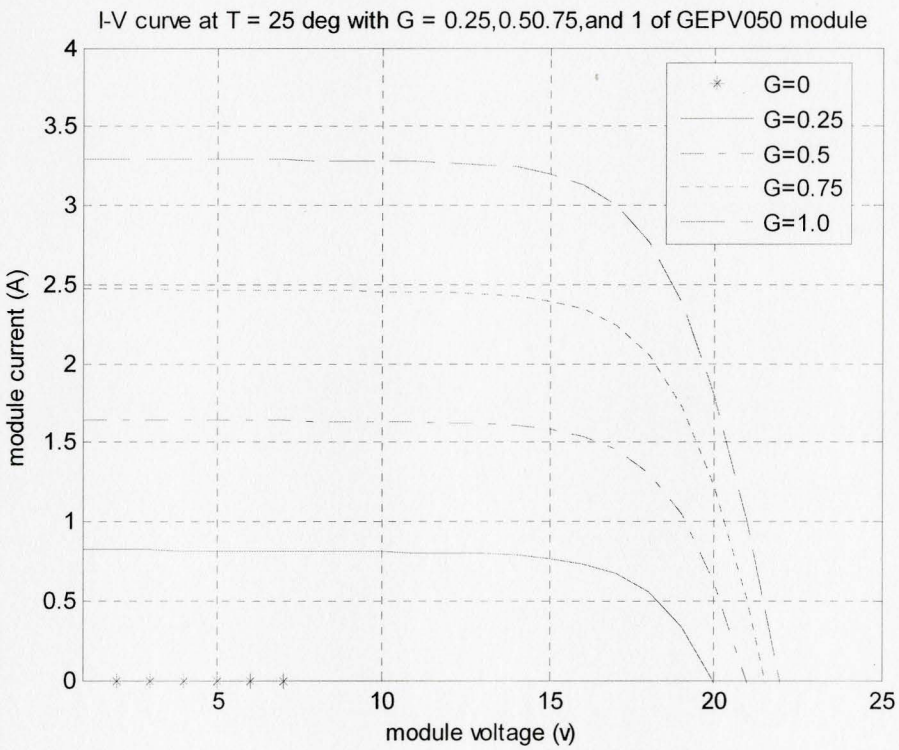


Fig. 2.13 V-I Characteristic Curves with Different Sun Illuminations

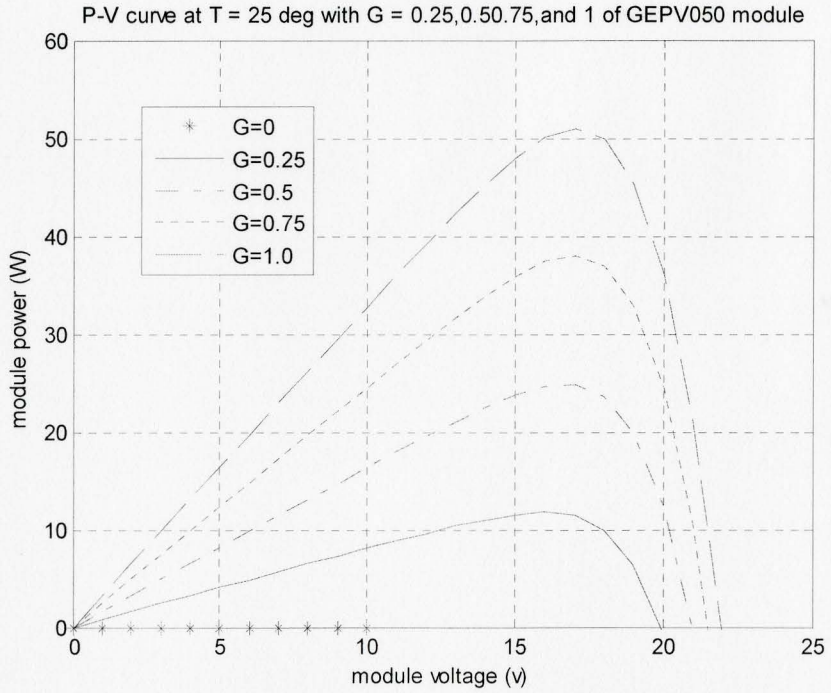


Fig. 2.14 P-V Characteristic Curves with Different Sun Illuminations

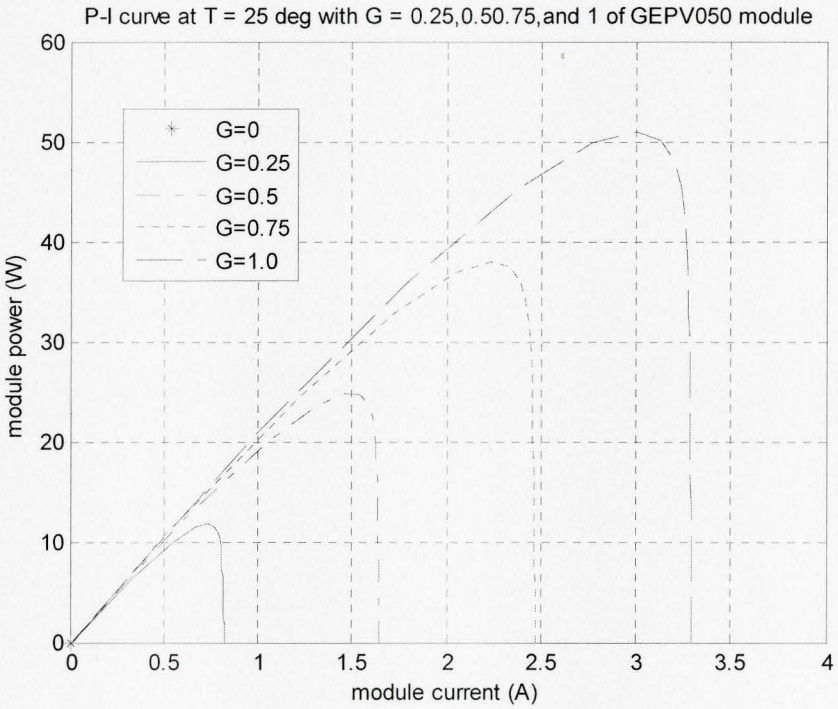


Fig. 2.15 P-I Characteristic Curves with Different Sun Illuminations

In conclusion, the maximum power point (or the corresponding voltage V_{mpp}) is not constant; it depends primarily on PV module temperature and sun illumination. At lower illumination level G, the short circuit current decreases approximately linearly with irradiation. The open circuit voltage does not decrease as much until irradiation is very low. The effect of PV module temperature on the open circuit voltage of the PV module is more profound than that of the sun irradiance. The higher the module temperature, the lower the open circuit voltage is, and therefore the less maximum power is available from the PV modules.

2.8 Issues in the PV Cell or Module Connection and Solutions

During day time, the solar array charges a battery when excess power can be generated. Given unpredictable weather conditions, it is difficult to prevent a portion of a PV array from being shaded occasionally. This will result in a considerable voltage drop on the output voltage, and at the same time causes the shaded cells to dissipate power as heat (hot spot). This problem can be solved by adding by-pass diodes across each PV cell, as seen from the Fig. 2.16. Each by-pass diode provides an alternative current path, because the resistance of a shaded cell is bigger than the internal resistance of a diode. Instead of a large voltage drop, the voltage drop can be limited to the relatively small forward diode drop of 0.3~0.7V [8].

Another situation may arise when several series-connected PV modules are connected in parallel. If one of the series-connected modules is partially shaded, it acts as a load, and results in keeping current from other PV modules. During night time, each

solar cell behaves as a diode under forward bias. When they are directly connected to the battery, they provide a discharge path for the battery, which causes leaking current and damage to the solar cells. These problems are traditionally avoided by the use of blocking or string diodes (are also shown in Fig. 2.16) on top of each paralleled-connected PV string. Overall the by-pass and blocking diodes reduce the output of the system slightly but prevent the PV cells from damage.

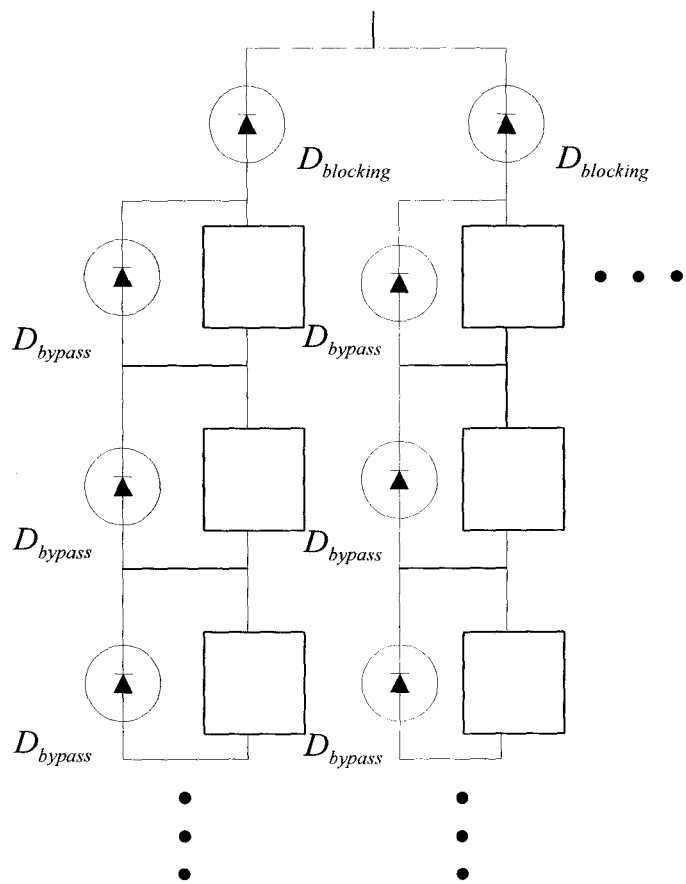


Fig. 2.16 Structure of a PV Array

Chapter 3

Photovoltaic Systems

3.1 PV Systems Classification

Photovoltaic systems can be designed to provide DC or AC power, can be interconnected with or independent of the utility grid, and can be integrated with other energy sources and energy storage systems.

According to functionality, operational requirements and component configurations, the photovoltaic systems can be classified into two categories; they are stand-alone (or off-grid) PV systems that operates independently of the grid; or grid-connected (or utility-interactive) PV systems that are tied into the grid network. Both types use PV modules connected in series and parallel to form PV arrays that produce DC energy at various voltage levels and eventually feed an AC converter.

Energy storage batteries are found in stand-alone systems, but sometimes they are also found in the utility-interactive systems. Variations of each system are possible with some utility-interactive systems having battery banks to provide energy when the utility power is not available. The larger residential stand-alone systems will usually have a back-up generator, and these systems are known as hybrid stand-alone systems.

3.1.1 Stand-alone PV Systems

Stand-alone PV systems are typically installed in remote areas where the utility grid is not available or where the connection fees to the grid are higher than the costs of an alternative energy system. Stand-alone PV systems are designed to operate completely

independently of any other power supplies, and are generally designed and sized to supply certain DC or AC electrical loads [12].

The simplest type of stand-alone PV system is a direct-coupled PV system, where a PV array is directly connected to a DC load, as depicted in Fig. 3.1. Since there is no battery storage, this system can only be used during the day time.

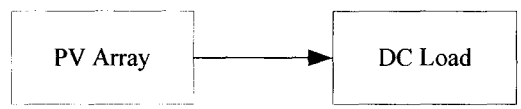


Fig. 3.1 Direct-coupled PV System [12]

A well-designed stand-alone PV system can satisfy any load requirements, and by adding a Maximum Power Point Tracker (MPPT) between the PV array and the loads, it helps by constantly extracting the maximum power produced from the PV array. Usually batteries are incorporated in this system; they store the energy from the PV array during day time, and provide the energy during night or cloudy day time (see Fig. 3.2).

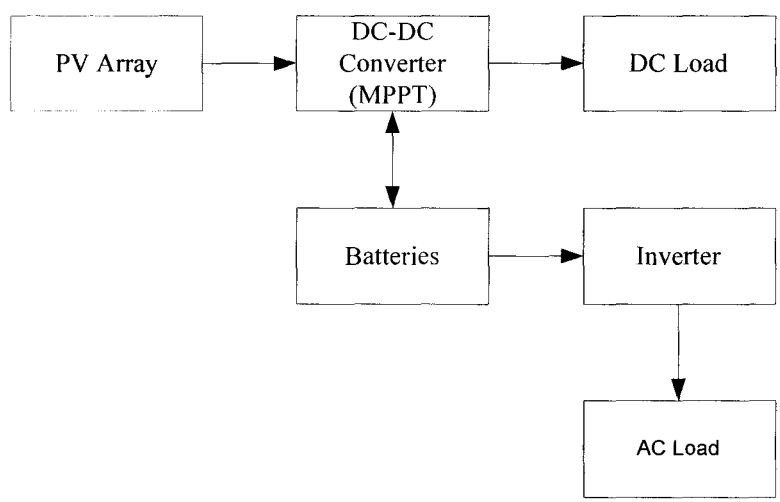


Fig. 3.2 Mixed DC/AC with MPPT PV System [12]

A system that is not only powered by the PV array but also wind turbine or diesel generator as an auxiliary power source, is known as a hybrid PV system as seen in Fig. 3.3.

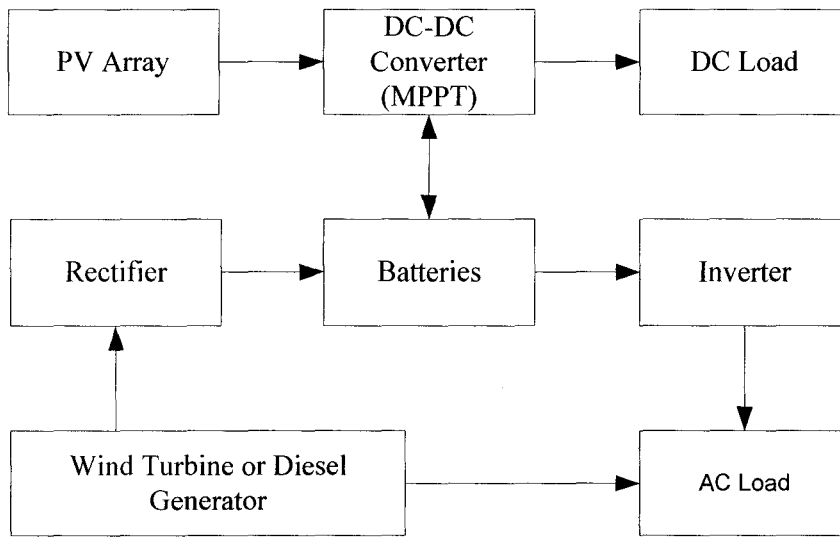


Fig. 3.3 Hybrid PV System [12]

3.1.2 Grid-connected PV system

Grid-connected systems are designed to operate synchronously in parallel with the local utility networks. The grid stores excess power produced form the PV array, and provides power when the electrical loads are greater than the PV array output (as seen in Fig. 3.4 and Fig. 3.5) [12]. Grid-connected systems with batteries take advantage of available utility grid, but give additional protection (by using backup batteries) from outages [13], as shown in Fig. 3.6.

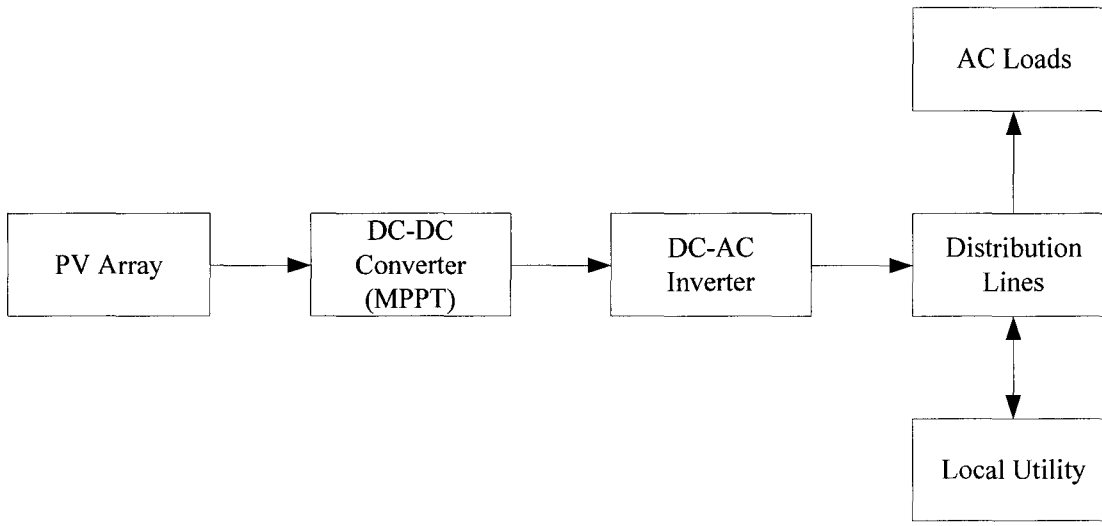


Fig. 3.4 Grid-connected PV System [12]

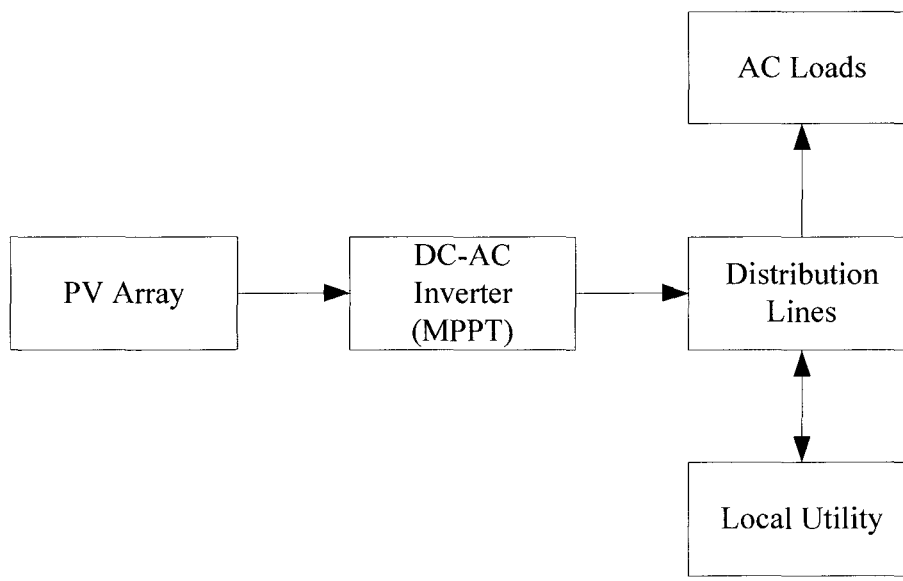


Fig. 3.5 Grid-connected PV System with Inverter Only [12]

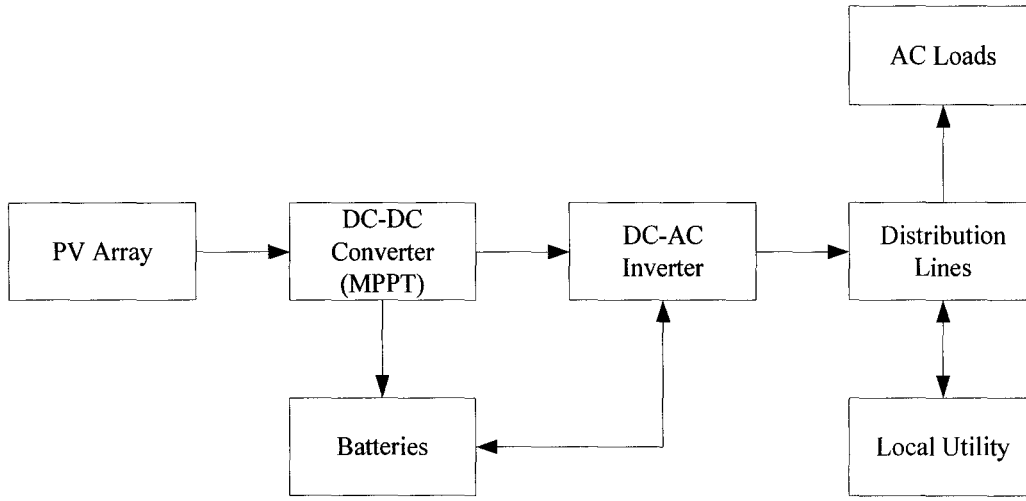


Fig. 3.6 Grid-connected PV System with Backup Batteries [12]

In grid-connected power systems, the grid acts like a battery with an unlimited storage capacity. In a stand-alone system, when the batteries are fully charged the rest of the direct current generated from the PV array is unused.

3.2 Why MPPT

The solar cell I-V relationship continuously varies under different atmospheric conditions and is strongly dependent on PV cell temperature and sun illumination. Thus every I-V curve has its own optimal point or Maximum Power Point (MPP). The nonlinear solar I-V curves characteristics will determine component selection, circuit design, and software control schemes.

In a PV stand-alone system without a Maximum Power Point Tracker (MPPT), a PV array is usually forced to operate at the load (batteries) voltage. This is usually below the voltage of PV array at the maximum power point V_{mpp}. In this situation, some of the power generated from a PV array will be lost resulting in low power conversion

efficiency. Rather than directly connecting the PV array to the load, a MPPT is introduced as an interface between the PV source and the load. This ensures that the PV system will operate at its maximum power point or voltage (V_{mpp}) under a variety of environmental conditions. If there is excess voltage available from the PV array the MPPT will convert this to additional current and store the extra energy in the output batteries.

3.3 Different Maximum Power Point Tracker Algorithms

A control algorithm is the heart of a maximum power point tracker in a PV system. Many different mechanisms for MPPT have been proposed and accomplished over the years. There are several MPPT methods described in the literature, which are described in the following sections.

3.3.1 Hill-Climbing Method (HC)

The most common MPPT algorithm is the conventional Hill-Climbing method. The method directly searches for the MPP by measuring the solar array terminal power. If there is an increase in power, then the change of power in the PV array should remain the same to find the MPP, otherwise the search direction should be reversed. Particularly if we assume that the initial operating point is at P_0, and the next point is at P_1, this increase in the power will keep the searching direction same. But if the next operating point is at P_2, which is still higher than the previous power point P_1, the controller will keep going in the wrong direction and bring the operating point further away from the

MPP to the point P_3, this will result in a large oscillation as illustrated in Fig. 3.7. Its control flow diagram is also shown in Fig. 3.8.

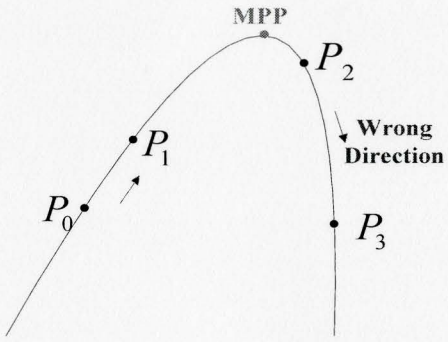


Fig. 3.7 Hill-Climbing Algorithm

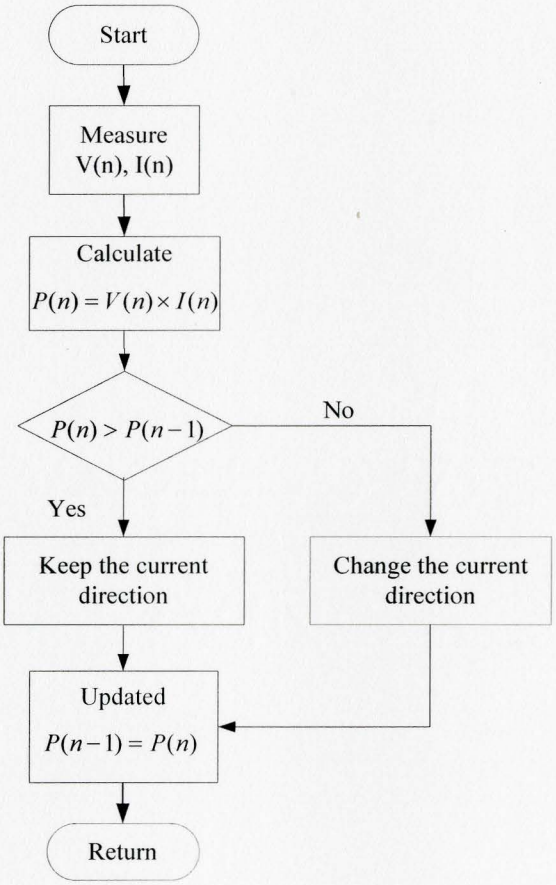


Fig. 3.8 Flowchart of Hill-Climbing Method

The method fails under rapidly changing atmospheric conditions. The solar power fluctuations are highly dependent on the increment (changing step size) of the duty cycle. This incremental duty cycle affects the searching time and the suppression of power fluctuations (reduction of power fluctuation) [14][15][16]. Fast searching time will suffer from larger power fluctuations. There is thus a tradeoff between the searching time to find the MPP and the power oscillations which need to be investigated experimentally. The Hill-Climbing method is not a standard PID control. The standard PID algorithm attempts to correct the error between the measured data and the desired value. In our application, we do not know the target due to the unpredictable weather conditions, thus the error between the measured data and the target cannot be defined.

3.3.2 Perturbation and Observation Method (P&O)

The perturbation and observation method is widely used because of its ease of implementation and its simple feedback structure with a few measured parameters. The MPPT operates by periodically incrementing or decrementing the PV array operating voltage (referred to as the perturbation) by comparing the current PV array output power to the previous one.

If a given perturbation leads to an increase in the PV array power, the subsequent perturbation will continue in the same direction in the next cycle so that the operating point moves toward the MPP and vice versa [17][18]. In this manner, the MPPT continuously seeks the peak power point and its flowchart is represented in Fig. 3.9.

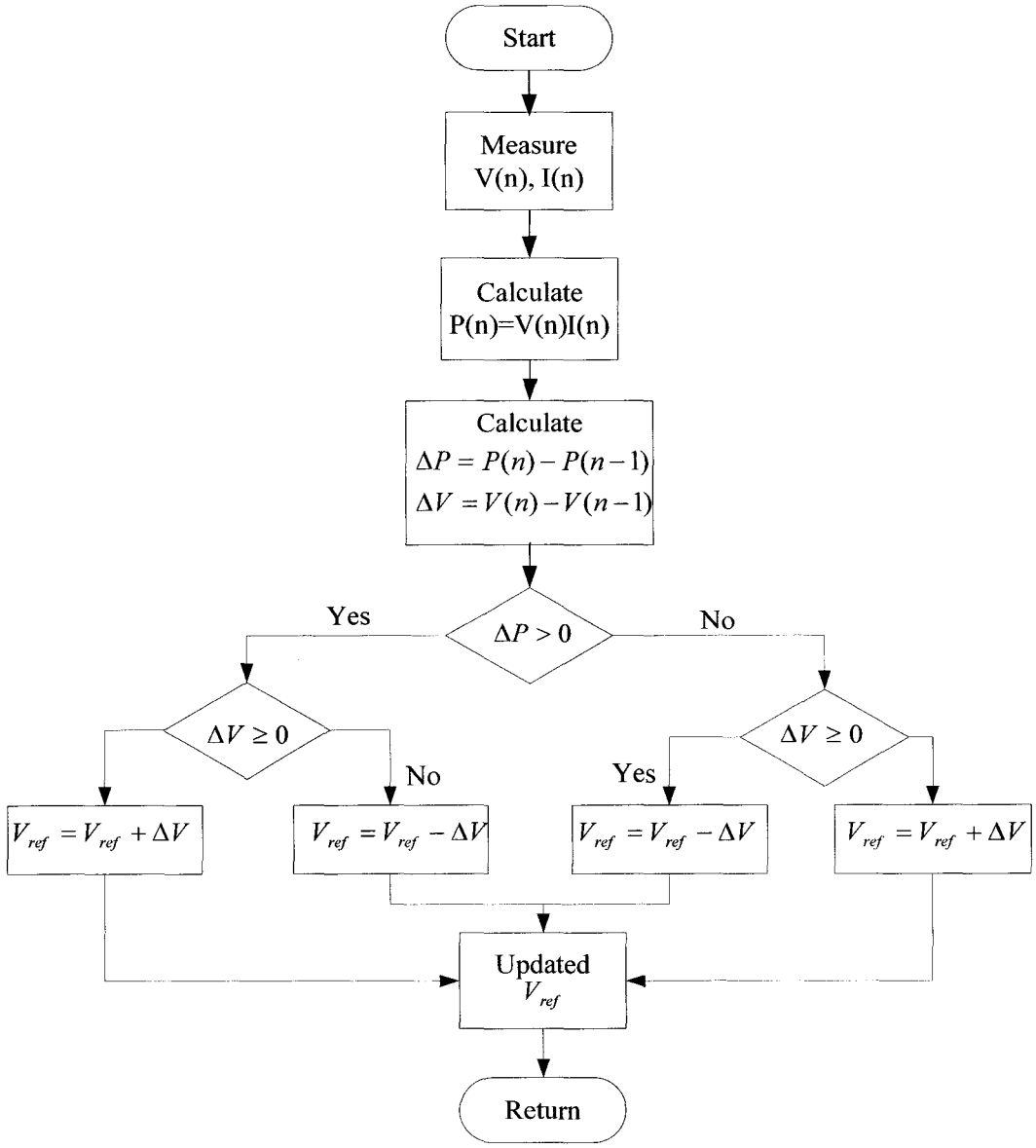


Fig. 3.9 Flowchart of P&O Method [17]

The drawback of both P&O and hill-climbing methods is the operating point oscillates around the real MPP in the steady state, which causes power losses. Moreover all the literature ([14][18][19][20]) claims that under a rapidly or unstable atmospheric change condition, they both fail to capture the real MPP quickly, which leads to more

power losses. Hill-climbing and P&O methods are different ways to envision the same fundamental method. The HC method utilizes a perturbation in the PWM duty ratio (which in turns perturbs the PV array voltage), and the P&O method uses a perturbation in the operating voltage of the PV array. The trade-off between fast transient responses and steady state performance must be considered carefully.

3.3.3 Incremental Conductance (IncCond) Method

To overcome the disadvantage of the previous control approaches the Incremental Conductance (IncCond) algorithm was developed. This algorithm uses the derivative of the PV array output power with respect to the PV array voltage (the slope of the P-V curve). This derivative is equal to zero at the maximum power point [19][20]. If the slope of the P-V curve is positive, this means that the operating point is on the left side of the real MPP. While if the slope pf the P-V curve is negative, then the operating point is on the right side of the real MPP, as illustrated in Fig. 3.10.

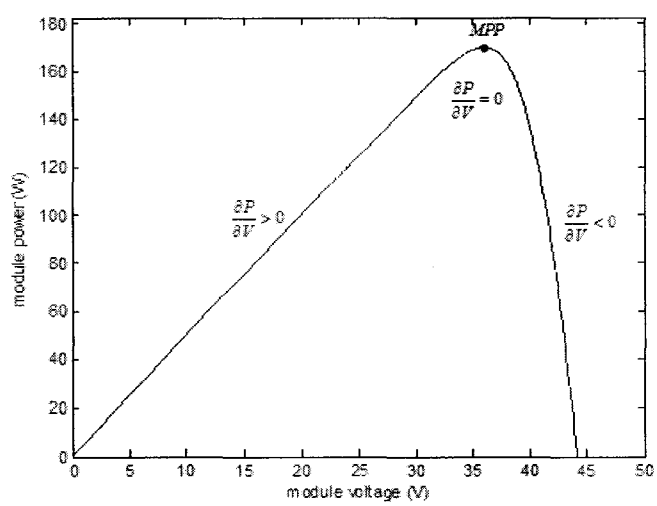


Fig. 3.10 P-V Curve of PV Array

We know that $P = V \cdot I$. Given this expression divide by V, and take a derivative on both sides, and then the expression can be written as:

$$\frac{\partial P}{\partial V} = \frac{\partial (V \cdot I)}{\partial V} = I + V\frac{\partial I}{\partial V} \Rightarrow \frac{1}{V} \cdot \frac{\partial P}{\partial V} = \frac{I}{V} + \frac{\partial I}{\partial V} \qquad (3.1)$$

Equation (3.1) can be further simplified as:

$$\frac{1}{V} \cdot \frac{\partial P}{\partial V} = g + \Delta g \qquad (3.2)$$

Where $g = \frac{I}{V}$ denotes conductance and $\Delta g = \frac{\partial I}{\partial V} = \frac{\Delta I}{\Delta V}$ denotes incremental conductance

From equation (3.2), we can conclude as the following:

$$\begin{cases} \frac{\partial P}{\partial V} = 0, \text{ at the MPPT} \\ \frac{\partial P}{\partial V} > 0, \text{ left side of the MPPT} \\ \frac{\partial P}{\partial V} < 0, \text{ right side of the MPPT} \end{cases} \Rightarrow \begin{cases} g = |\Delta g|, \text{ at the MPPT} \\ g > |\Delta g|, \text{ left side of the MPPT} \\ g < |\Delta g|, \text{ right side of the MPPT} \end{cases}$$

Using the above relationships, the MPPT can keep searching for the real MPP of PV array until the array's instantaneous conductance g is equal to its incremental conductance Δg. The algorithm flow chart is depicted in Fig. 3.11. We can see that the left branch is responsible for cell temperature variation, while the right branch is responsible for the sun illumination variation.

The IncCond method solves the limitations of hill-climbing and P&O methods, because once the real MPP is reached, it stops searching and ideally it does not oscillate

around the real MPP as discussed in [19]. The IncCond method can trace the real MPP under rapid weather condition quickly. The method yields high system accuracy and efficiency, but with increased complexity, computational time, and thus expense [20].

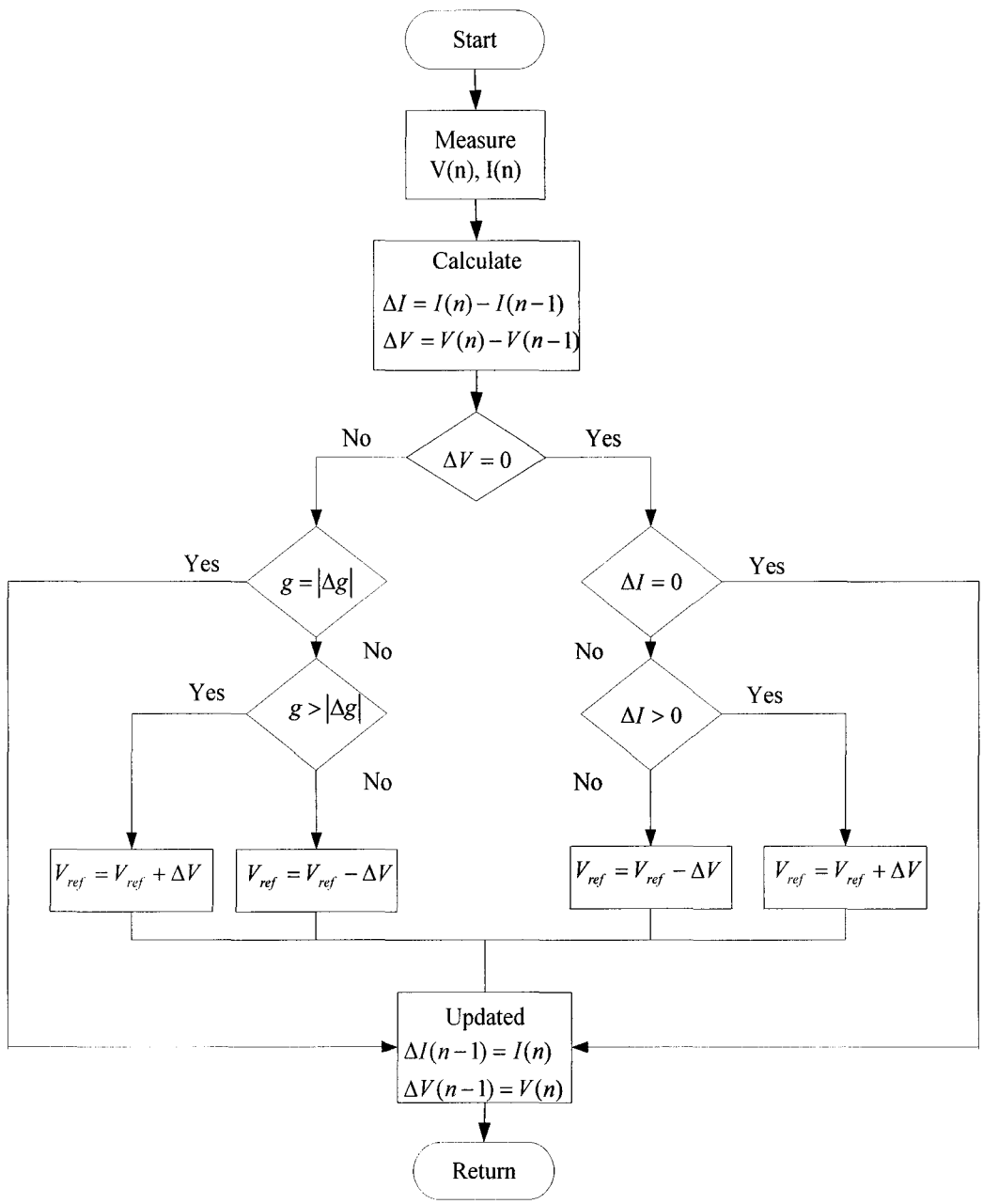


Fig. 3.11 Flowchart of IncCond Method

3.3.4 dp/dv Method

The dp/dv algorithm is similar to the IncCond method, but simpler, because it is directly based on the sign of the derivative of the output power with respect to the output voltage of PV array (dp/dv). So if dp/dv is positive, the operating point is on the left side of the MPP of P-V curve. If dp/dv is negative, then the operating point is on the right side of the MPP. If dp/dv is zero, then the operating point is at the MPP (refer back to Fig. 3.10). In other words, the duty cycle is continually adjusted until dp/dv=0. This approach offers a simple and stable solution compared to the other MPPT control methods. Overall the dp/dv method can give a fast transient response and low oscillations at steady-state.

3.3.5 Constant Voltage (CV) Method

The constant voltage algorithm requires prior study of PV model and its characteristics (as presented in chapter 2) unlike the previous tracking methods. The CV method uses these characteristics to estimate the MPP with ambient condition and solar cell temperature measurements. If the sun intensity varies slightly, then the open circuit voltage of the PV array V_{OC} and the maximum power point voltage V_{mpp} will change in very small increments [17]. Despite the fact that the ratio between V_{mpp} and V_{OC} depends on the parameters of a PV array, usually V_{mpp} is set to 76% of V_{OC} for simplicity regardless of the effects of sun irradiance and cell temperature [18] [20]. This control method tracks the MPP faster than the other methods. There are several problems with this method. Firstly V_{mpp} is not always 76% of V_{OC}, this is just an approximation. The tracked MPP is not the real MPP generated from the PV array. Secondly the input energy

is wasted when the load is disconnected from the PV array in order to sample the PV array open voltage. Thirdly this method needs more sensors than other methods, which means that it is expensive, and some parameters of the PV array are not known adequately from manufacturers [18]. Despite these issues, this algorithm is suitable for a satellite system due to conditions of constant sun illumination and stable PV cell temperature. A Table of comparison among various MPPT control algorithms presented in the previous sections is summarily shown in Table 3.1.

MPPT Method	True MPPT	Advantage	Disadvantage
HC and P&O	Yes	The simplest MPPT	Oscillates around the real MPP, which causes system power loss
IncCond	Yes	None or less oscillations around the real MPP	Error due to low accuracy of sensors, and more computational time
dp/dv	Yes	None or less oscillations around the real MPP	Error due to low accuracy of sensors, and more computational time
CV	No	High efficiency	Not a true MPPT, and expensive

Table 3.1 Comparison of MPPT Algorithms

3.4 Suitable Construction of MPPT and Selection of PV Systems

A Maximum Power Point Tracker (MPPT) normally utilizes standard switch mode DC-to-DC converters. These converters can converter a source of DC from one voltage level to another by storing the source energy temporarily and then releasing that energy to the output. The most common topologies are buck, boost, buck-boost, and Cuk converters. In the following sections, the following assumptions have been made:

1) The switch (MOSFET Q) is turned on and off (in each converter) at a frequency of f_{SW}, which is called the operating frequency or the switching frequency. The inverse of this frequency is defined as the switching period $T_{SW} = 1/f_{SW}$.
2) When the switch (MOSFET Q) is turned on at $T_{ON} = d_1 T_{SW}$, it is called on-stage. Where T_{ON} represents the time when the switch is on, the term d_1 represents the duty cycle when the switch is on.
3) When the switch (MOSFET Q) is turned off at $T_{OFF} = d_2 T_{SW}$, it is called off-stage. Where T_{OFF} represents the time when the switch is off, the term d_2 represents the duty cycle when the switch is off.
4) The relationship between the duty cycle d_1 and the duty cycle d_2 is: $d_1 + d_2 = 1$

3.4.1 Buck Converter

A buck converter is known as the step-down converter. It alternates between connecting the inductor with the source voltage to store energy in the inductor, and transferring the energy to the load. The basic circuit diagram is depicted in Fig. 3.12.

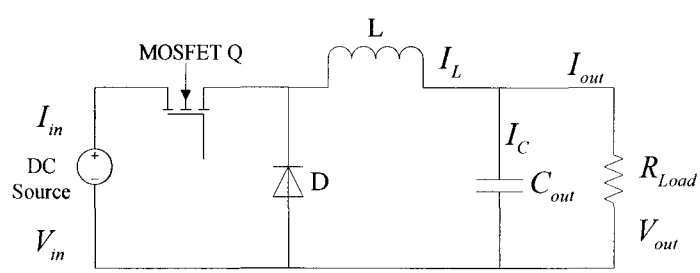


Fig. 3.12 Basic Circuit of a Buck Converter

Depending on the choices of the switching frequency and circuit components, the inductor current can be driven in Continuous Current Mode (CCM) [21], which means "constant average current". In this mode, the current going through the inductor L never falls to zero. The equivalent waveforms for the inductor current I_L, the output capacitor current I_C, and the output voltage V_{out} are also illustrated in Fig. 3.13.

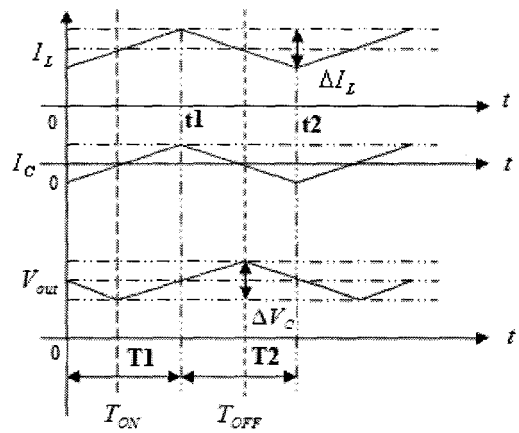


Fig. 3.13 Waveforms of Buck Circuit

Given the continuous mode, the basic buck circuit operation can be divided into two stages: In the on-stage, the MOSFET Q is switched on at $T_{ON} = d_1 T_{SW}$. The input current I_{in} rises and flows through the filtering inductor L, the output filtering capacitor C_{out}, and the load R_{Load}. Note here that the current waveform is an exponential rise and fall, but at higher frequencies and with very low resistances involved, this can be approximated by a linear variation. In the off-stage, the MOSEFT Q is turned off at $T_{OFF} = d_2 T_{SW}$. The inductor current I_L is prevented from stopping because of the magnetic flux in the inductor L hence is forced through the freewheeling diode D, so that

the inductor current I_L continues to flow through L, C_{out}, R_{Load}, and the diode D. The inductor current I_L decreases until the MOSFET Q is turned on again in the next cycle. As a result, the buck converter is able to step down the input DC voltage V_{in} from its fixed high level to a desired low level by controlling the duty cycle d_1. The output voltage V_{out} across the load in the steady state can be expressed as:

$$V_{out} = V_{in} \cdot d_1 \qquad (3.3)$$

If assume that all the components in the circuit are ideal, then the average output current I_{out} can be written as:

$$I_{out} = I_{in} / d_1 \qquad (3.4)$$

3.4.2 Boost Converter

A boost converter is a step-up converter. It has the same components as the buck converter, but provides a higher output voltage than its input voltage due to its different arrangement of components in the circuit as shown in Fig. 3.14.

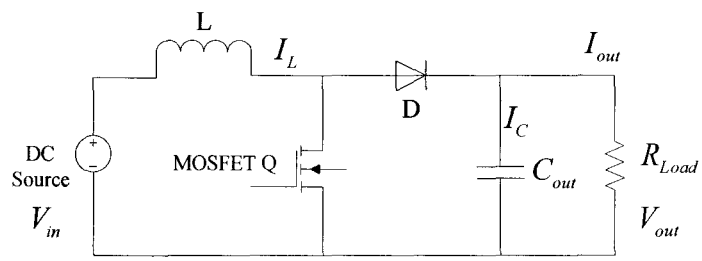


Fig. 3.14 Basic Circuit of a Boost Converter

In the on-stage with a time duration of $T_{ON} = d_1 T_{SW}$, the MOSFET Q is closed causing an increase in the inductor current I_L and the magnetic energy stored in the inductor L is built up. In the off-stage with a time duration of $T_{OFF} = d_2 T_{SW}$, the inductor current I_L can not stop instantly thus going through the freewheeling diode D, the output capacitor C_{out}, and the load R_{Load}. The energy stored in the inductor during the on-stage is transferred into the output capacitor C_{out} and the load R_{Load} during the off-stage. The inductor current I_L decreases until the MOSFET Q is closed again, the diode is reverse-biased, and the output capacitor C_{out} sustains the load R_{Load}. If the boost converter is operated in CCM, the current in the inductor will not decay to zero. Besides the fact of the inductor L being the storage element, the inductor L also helps controlling the magnitude of current ripple; the larger the inductance the smaller the current ripple. Since the voltage across the inductor L reverses and adds to the source voltage during the off-stage, the average output voltage V_{out} as shown in equation (3.5) is thereby higher than the input voltage V_{in}, and it is adjustable according to the duty cycle d_1, which represents the duty cycle when the switch is on.

$$V_{out} = \frac{V_{in}}{1 - d_1} \qquad (3.5)$$

If the boost converter is 100% efficient, then the average output current I_{out} can be expressed as:

$$I_{out} = I_{in} \cdot (1 - d_1) \qquad (3.6)$$

3.4.3 Buck-Boost Converter

A buck-boost converter provides both buck and boost functionalities. In other words, its output voltage can be either higher or lower than its input voltage. Additionally the polarity of the output voltage is opposite the input voltage. The basic buck-boost circuit is illustrated in Fig. 3.15.

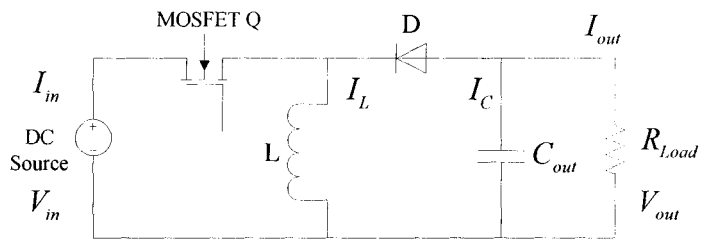


Fig. 3.15 Basic Circuit of a Buck-Boost Converter

In the on-stage with a time duration of $T_{ON} = d_1 T_{SW}$, the inductor is directly connected across the source voltage V_{in}, the input current is built up to provide stored magnetic energy in the inductor L, the diode D becomes reverse-biased, and the capacitor C_{out} supplies the output load R_{Load}. In the off-stage with a time duration of $T_{OFF} = d_2 T_{SW}$, the inductor reverses its polarity and causes the diode D forward-biased, so that the inductor current I_L charges on the bottom side of the output capacitor C_{out} [21]. The average output voltage V_{out} can be written in equation (3.7). If we ignore losses in the circuit, then the average output current I_{out} is expressed in equation (3.8).

$$V_{out} = -\frac{d_1}{1-d_1} \cdot V_{in} \qquad (3.7)$$

$$I_{out} = \frac{1-d_1}{d_1} \cdot I_{in} \qquad (3.8)$$

3.4.4 Cuk Converter

The Cuk converter has additional components compared to the other three types of converters. The circuit configuration is shown in Fig. 3.16, which looks like a combination of the buck and boost converters.

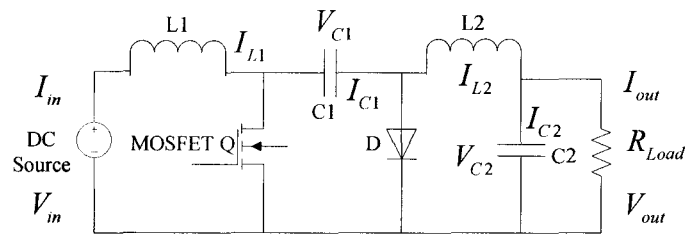


Fig. 3.16 Basic circuit of a Cuk Converter

The MOSFET Q is initially turned on, the current in the inductor L is established. When the MOSFET is turned off, the inductor current I_L continues to charge the capacitor C1 via the freewheeling diode D, and back to the source. In the on-stage, the current flowing through the inductor L1 rises again, meanwhile the voltage of the capacitor C1 makes the diode D reverse-biased. The current discharges from the capacitor C1 and flows through the capacitor C2, the inductor L2, and the load R_{Load}. In the off-stage, the capacitor C1 is charged from the source, and the energy stored in the inductor L2 is released to the capacitor C2 and the load R_{Load}. Equivalently the current

I_{L2} charges the bottom side of the capacitor C2, and supplies the load R_{Load}. Hence we can find the average output voltage V_{out} as:

$$V_{out} = -\frac{d_1}{1-d_1} \cdot V_{in} \qquad (3.9)$$

From equation (3.9), we know that the Cuk converter can increase or reduce the output voltage just like the buck-boost converter. Likewise the average output can thus be expressed as equation (3.8).

If the Cuk converter is operated in CCM, due to the inductors (L1 and L2) at both input and output sides, the input and the output currents are both continuous. Unlike the other types of converters that use an inductor to transfer the energy from the source to the load, in the Cuk converter, the energy is transferred through an intermediate capacitor (C1). Note that importantly all of the output current has to flow through the capacitor C1, thus the capacitor C1 needs to be able to handle a high ripple current rating and give a low equivalent series resistance to reduce the power loss [21].

3.4.5 Converter Comparisons and Their Advantages and Disadvantages

A buck converter can be used to reduce the source voltage. A boost converter can be used to enlarge the source voltage. Both buck-boost and Cuk converters can be used to either reduce or increase the input voltage, and always have the output voltage reversed in polarity with respect to the source voltage. Based on the energy transference, the buck, boost, and buck-boost converters all use an inductor to transfer energy between input and

output. The Cuk converter however uses capacitive energy transfer. Table 3.2 presents a summary of the advantages and disadvantages of the converters described in previously.

Converter Type	Functionalities	Advantages	Disadvantages
Buck	Step down, inductive energy transfer	Simple, continuous output current, the source is not directly connected to the load	Discontinuous input current, requires floating gate drive
Boost	Step up, inductive energy transfer	Simple, continuous input current, ground-referenced gate drive	Discontinuous output current, the source is directly connected to the load
Buck-Boost	Step up or down, inverting, inductive energy transfer	Can increase or decrease the output voltage, the source is not directly connected to the load	Discontinuous input and output currents current, requires floating gate drive, complex
Cuk	Step up or down, inverting, capacitive energy transfer	Continuous input and output currents, low current ripple, ground-referenced gate drive	Requires more components than other converters, the capacitor needs to handle a high current ripple, complex, and expensive

Table 3.2 Advantages and Disadvantages of each Converter

The input current of a buck converter is discontinuous. The current discontinuity must be compensated by adding an input voltage filtering capacitor. A boost converter has an inductor on its input which makes the input current quasi continuous. However it requires larger inductance and output capacitance than needed in a buck converter of the same design specification [21]. For a buck-boost converter, its input and output currents

are pulsating and it has high peak current flowing through the switch. Due to high ripple currents, this converter normally has lower efficiency than the previous two converters. The polarity of the output voltage is opposite to its input voltage. The Cuk converter has more components than the other converters, and the capacitor C1 has to handle much higher current ripple than the capacitors in the other converters. Consequently these elements make the design more complicated and expensive. In our application, the buck converter is chosen for convenience of implementation, and also mainly because it allows a direct connection, which the boost converter does not allow.

3.5 Calculations for the Basic Buck Circuit Components

Inductor

The difference between the input voltage and the output voltage is the voltage across the inductor as shown in the circuit diagram of Fig. 3.12. Assume that the resistance is negligible, the current ripple ΔI_L in the inductor L can be calculated as:

$$(V_{in} - \mathrm{V_{out}}) = L\frac{\partial I_L}{\partial T_{ON}} \rightarrow \Delta I_L = \frac{(V_{in} - \mathrm{V_{out}})}{L} d_1 T_{SW} \qquad (3.10)$$

Given ∂I_L is approximately equal to ΔI_L. Where V_{in} denotes the input voltage of the buck converter, the term V_{out} represents the output voltage of the buck converter. The term d_1 represents the duty cycle 1 when the switch is on and its value is computed as the output batteries voltage divided by the operating voltage at the maximum power point.

In steady state, the inductor current ripple at t1 should be approximately equal to the inductor current at t2, as illustrated in Fig. 3.13. The derivation is expressed in equation (3.11). The switch-on time T_{ON} is equal to $d_1 \cdot T_{SW}$, where $d_1 = V_{out} / V_{in}$, and the relationship between d_1 and d_2 is $d_1 + d_2 = 1$.

$$|\Delta I_L|@t_1 = |\Delta I_L|@t_2 \rightarrow \frac{(V_{in1} - V_{out})}{L} d_1 T_{SW} = \frac{V_{out}}{L}(1-d_1)\cdot T_{SW} = \frac{V_{out}}{L} d_2 \cdot T_{SW} \qquad (3.11)$$

We choose ΔI_L 10%-20% of the current in the inductor I_L. The input voltage V_{in} is equal to the voltage V_{mpp} at the maximum power point when the buck converter is working at its optimal point. The inductor L can be deduced from equation (3.11) and shown as follows:

$$L \geq \frac{(V_{mpp} - V_{out})\cdot d_1 \cdot T_{SW}}{\Delta I_L} = \frac{V_{out}\cdot(1-d_1)\cdot T_{SW}}{\Delta I_L} = \frac{V_{out}\cdot d_2 \cdot T_{SW}}{\Delta I_L} \qquad (3.12)$$

Capacitors

In a buck converter, the input current is pulsating. To make this input current relatively stable and continuous, an input capacitive filter (or smoothing) must be placed in parallel with the DC supply (solar source), in order to act as a reservoir. The source voltage will be filtered so that the input voltage is quasi constant if the input capacitor is large enough. Input capacitor is determined by the factors including the input current drawn from the source and the ESR existing in the input capacitor.

The input filtering capacitor C_{in}, during T_{ON} switch on time, discharges an average current of $(I_{out} - I_{in})$ as shown in Fig. 3.12 [22]. This discharge causes a linear input voltage ripple ΔV_{in}, and can be expressed in equation (3.13):

$$\Delta V_{in} = \frac{(I_{out} - I_{in}) \cdot T_{ON}}{C_{in}} \quad (3.13)$$

The input capacitor C_{in} is then derived as shown in equation (3.14). Where I_{out} can be found from the assumption of $V_{in} \cdot I_{in} = V_{out} \cdot I_{out}$.

$$C_{in} \geq \frac{(I_{out} - I_{in}) \cdot T_{ON}}{\Delta V_{in}} = \frac{(I_{out} - I_{in}) \cdot d_1 \cdot T_{SW}}{\Delta V_{in}} \quad (3.14)$$

Similarly, but with opposite polarity, during switch off time T_{OFF}, the input voltage ripple ΔV_{in} and the input filtering capacitor C_{in} can also be derived from equation (3.15) and equation (3.16).

$$\Delta V_{out} = \frac{I_{in} \cdot T_{OFF}}{C_{in}} \quad (3.15)$$

$$C_{in} \geq \frac{I_{in} \cdot T_{OFF}}{\Delta V_{out}} = \frac{I_{in} \cdot d_2 \cdot T_{SW}}{\Delta V_{out}} \quad (3.16)$$

Another parameter that needs to be determined is the RMS current going through the input capacitor as shown in equation (3.17):

$$I_{in(RMS)} = \sqrt{\left((I_{out} - I_{in})\sqrt{d_1}\right)^2 + \left((I_{in})\sqrt{d_2}\right)^2} \quad (3.17)$$

By substituting $d_1 = V_{out}/V_{in}$, $d_2 = 1 - d_1$, and $I_{in} = d_1 \cdot I_{out}$ into equation (3.17), the equation can be further simplified to equation (3.18) [22]:

$$I_{in(RMS)} = \frac{i_{out}}{V_{in}}\sqrt{V_{out}(V_{in} - V_{out})} \quad (3.18)$$

A higher ripple current rating is required at high frequencies to contain the switching spikes. It is important that the selected input capacitor has a high frequency rating and its RMS current rating should be well above the maximum operating RMS current [22].

The output capacitance usually is determined from the output ripple voltage specification, and this output ripple voltage is primarily influenced by the output inductor ripple current. Refer back to Fig. 3.12. Since $I_C = I_L - I_{out}$ and using the same idea of the voltage ripple ΔV_{out} in the output capacitor C_{out}, then the relationship between C_{out} and ΔV_{out} can be derived in equation (3.19). With the assumption that ΔV_{out} is 0.5%-1% of V_{out}, the output capacitor C_{out} can be finally evaluated as shown in equation (3.20).

$$\Delta V_{out} = \frac{1}{C_{out}}\int_{T_{ON}}^{T_{OFF}} i_C dt = \frac{1}{C_{out}}\left(\frac{1}{2}\cdot\frac{\Delta I_L}{2}\cdot\frac{T_{SW}}{2}\right) = \frac{\Delta I_L T_{SW}}{8C_{out}} = \frac{V_{out}(1-d_1)T_{SW}^{\ 2}}{8LC_{out}} \quad (3.19)$$

$$C_{out} \geq \frac{V_{out}(1-d_1)\cdot T_{SW}^{\ 2}}{8L\Delta V_{out}} \quad (3.20)$$

By examining equation (3.20), we can clearly see that the magnitude of the output voltage ripple ΔV_{out} can be influenced by the output capacitor C_{out} , the switch frequency f_{SW}, the inductor L, and the duty cycle d_1.

Alternatively, we can use the center frequency f_c to compute the value of the output capacitor C_{out} as expressed in equation (3.21):

$$f_c = \frac{1}{2\pi\sqrt{LC_{out}}} = (1 \sim 2)KHz \qquad (3.21)$$

This center frequency f_c is given by the LC low pass filter in the buck circuit, it should be less than the switching frequency in order to filter out the switching harmonics and give only a DC output voltage. Due to the rule of thumb, generally it should be at least 10 times smaller than f_{SW} [23].

Chapter 4

Hardware Design and Implementation

4.1 Introduction

The Maximum Power Point Tracker (MPPT) is constructed from two buck converters. The MPPT is powered by six PV modules, and the absorbed solar energy can be stored in a 24V battery bank. An MC-based 56F8013 control chip is responsible for finding the Maximum Power Point (MPP) of the PV array by tuning the PWMs' duty cycle on a continuous basis. The main circuit is divided into two basic parts: the power stage as shown in Fig. 4.1 (including two buck converters), and the control stage (including sampling or conditioning circuits and 56F8013 demonstration board from Freescale).

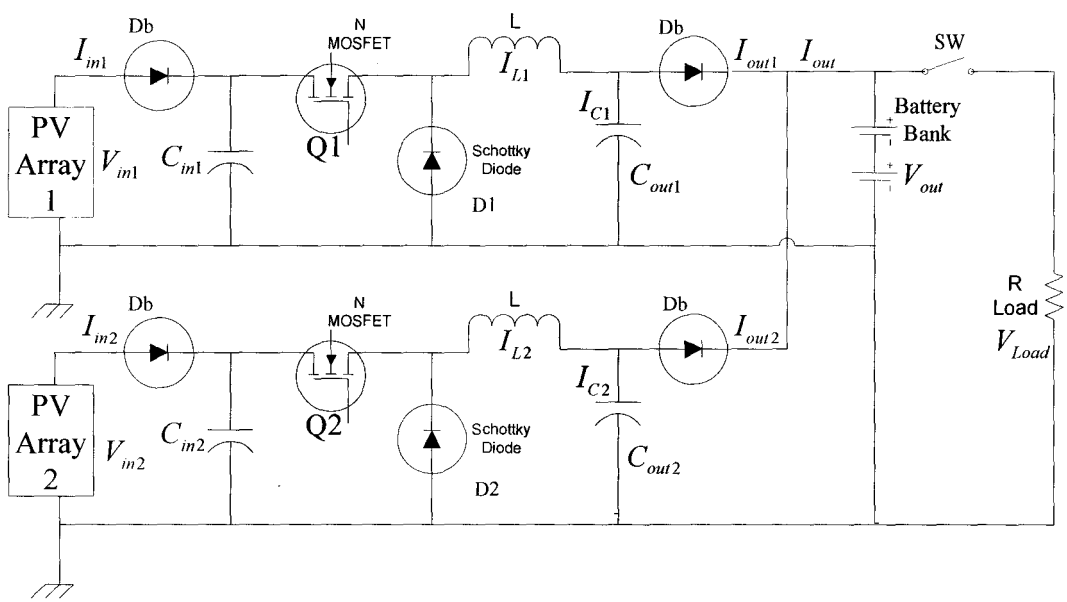


Fig. 4.1 MPPT Power-Stage Circuit

In order to generate the total input power, two PV arrays are constructed. Each array is connected by three "GEPV-050" modules in series to achieve a higher PV terminal voltage. Each buck converter is supplied by one array, the outputs of the two buck converters are connected in parallel. However, since each converter is an independent current source isolated by a diode feed, the converters are in essence isolated from each other and have only one control loop.

4.2 Components Selection of the Buck Converter in the Power Stage

The choice of the components in each buck circuit is vital because the converter must carry the entire source current. Each converter has to offer a high efficiency over a wide range of operating points. Any resistances or other losses, no matter how small they are, will contribute to the total power loss of the system.

4.2.1 Inductor

Initially we can assume that the converter output voltage is approximately constant at 24V and the converter is running at 100% efficiency, such as $P_{in} = P_{out}$. Each converter is assumed to operate in Continuous Conduction Mode (CCM). To find the value of the inductor and the rest of components for each buck converter, an extreme case has to be studied. Given the extreme case when the PV array operates at its maximum power under the standard conditions, including full sunlight (G=1) and 25°C for the PV array temperature. From the datasheet of the "GEPV-050" module, one module gives $I_{in} = I_{mpp} = 2.9$ A, $V_{in} = V_{mpp} = 17.3$ V, $V_{OC} = 22$ V and $I_{SC} = 3.3$ A. For three "GEPV-050" modules which are connected in series to form one array we will get

$V_{in} = V_{mpp} = 17.3 \times 3 = 51.9$ V and $V_{OC} = 22 \times 3 = 66$ V. Hence each PV array is able to deliver 150 W to each buck converter, and the total input power for the two buck converters is 300W. Based on the assumption that the two buck circuits are identical, then the currents going through each inductor and capacitor in each buck converter are also identical. According to Fig. 4.1, the average current going though each inductor (I_{L1} and I_{L2}) and the average current going through the load (I_{out1} and I_{out2}) are computed using equation (4.1), and the total output current I_{tot_out} is computed with equation (4.2)

$$I_{L1} = I_{L2} = I_L = \frac{P_{total}}{2 \cdot V_{battery}} = \frac{301.02W}{2 \cdot 24V} = \frac{150.51}{24} = I_{out1} = I_{out2} = I_{out} = 6.27A \quad (4.1)$$

$$I_{tot\_out} = I_{L1} + I_{L2} = 2 \cdot I_L = 12.54A \quad (4.2)$$

In a well designed converter circuit, the magnitude of the switching ripple should be much smaller than the DC components. If we assume that the amplitude of the inductor's current ripple ΔI_L is typically varies between 10% and 20% of its DC value I_L, and refer back to equation (3.12) in chapter 3, then the value of the inductor L can be calculated using equation (4.3), here that the current ripple ΔI_L is chosen to be 20% of I_{L1} and equal to 1.254A.

$$L \geq \frac{(V_{in} - V_{out}) \cdot d_1 \cdot T_{SW}}{\Delta I_L} = \frac{(51.9 - 24)V \cdot 0.462 \cdot 20\mu s}{1.254A} = 0.2056mH \quad (4.3)$$

or alternatively using equation (4.4):

$$L \geq \frac{(\mathrm{V_{out}}) \cdot d_2 \cdot T_{SW}}{\Delta I_L} = \frac{(24)V \cdot 0.538 \cdot 20\mu s}{1.254A} = 0.206mH \qquad (4.4)$$

The switching period T_{SW} is 20μs if the desired switching frequency is 50 KHz. The duty cycle d_1 is calculated using V_{out}/V_{mpp} and equal to 0.462 when the switch is on. The duty cycle d_2 can be computed as $d_2 = 1 - d_1 = 0.538$ when the switch is off.

In practice, the output voltage of any battery is not constant, it varies with the charging and discharging processes. The 24V-battery bank includes 12 individual cells, the minimum output V_{out_min} voltage of two 12V lead-acid batteries in series is the product of the individual cell voltage and the cell number: $V_{out\_min} = 1.65 \times 12 = 19.8$ V. The maximum output voltage V_{out_max} of the two batteries is $V_{out\_max} = 2.4 \times 12 = 28.8$ V. The inductor L can be re-evaluated from equation (4.3) or equation (4.4), note here that we use equation (4.4) to calculate the inductance, and the maximum value will be chosen to be the lower value boundary for the inductor L.

$$L \geq \frac{V_{out\_min} \cdot d_{2\_max} \cdot T_{SW}}{\Delta I_{L\_max}} = \frac{(19.8)V \cdot 0.6185 \cdot 20\mu s}{1.52A} = 0.161mH \qquad (4.5)$$

$$L \geq \frac{V_{out\_max} \cdot d_{2\_min} \cdot T_{SW}}{\Delta I_{L\_min}} = \frac{(28.8)V \cdot 0.445 \cdot 20\mu s}{1.046A} = 0.245mH \qquad (4.6)$$

The term I_{L_max} (150.51/19.8=7.6A) represents the maximum current going through each inductor, and its corresponding maximum current ripple ΔI_{L_max} is 20% of 7.6A. The

term $I_{L\_\min}$ (150.51/28.8=5.23A) represents the minimum current going through each inductor, and its corresponding minimum current ripple $\Delta I_{L\_\min}$ is 20% of 5.23A. The term $d_{1\_\min}$ denotes the minimum duty cycle when the switch is on. It can be calculated by using the minimum output voltage $V_{out\_\min}$ divided by the input voltage V_{in}, and it is equal to 0.3815. The term $d_{2\_\max}$ denotes the maximum duty cycle when the switch is off, it is equal to 0.6185 $(1-d_{1\_\min})$. Similarly $d_{1\_\max}$ is the maximum duty cycle when the switch is on, and it is equal to 0.555. The symbol $d_{2\_\min}$ represents the minimum duty cycle when the switch is off, it is equal to 0.455 $(1-d_{1\_\max})$.

The value computed for the inductor L is important since it determines the ripple current flowing through the output capacitor [24]. Using a small inductance will reduce the size of the choke but will increase the current ripple. A large inductance reduces the output voltage ripple and increases efficiency, but it has a large physical size that will consume a large space in a PCB layout.

Based on the previous calculations, and the inductor must at least be able to handle current of 6.27 A. Two inductors of 1mH from HAMMOND Manufacturing with part number 157D were chosen. These inductors are sufficiently large to ensure the two buck converters are working in CCM. Given a current rating of 10A and an internal resistance of 38mΩ, the maximum and minimum current ripple given the chosen inductance of 1mH can be recalculated from equations of (4.5) and (4.6) using equations of (4.7) and (4.8).

$$\Delta I_{L\_\min} = \frac{V_{out\_min} \cdot d_{2\_max} \cdot T_{SW}}{L} = \frac{19.8V \cdot 0.6185 \cdot 20\mu s}{1mH} = 0.245A \quad (4.7)$$

$$\Delta I_{L\_\max} = \frac{V_{out\_max} \cdot d_{2\_min} \cdot T_{SW}}{L} = \frac{28.8V \cdot 0.445 \cdot 20\mu s}{1mH} = 0.256A \quad (4.8)$$

4.2.2 Output and Input Capacitors

Since the input current of a buck converter is pulsating, the selected input capacitors need to have a high frequency rating, and provide a high RMS current rating [24]. They must be able to operate normally at least for the worst case of the RMS current, and the worse case of the input spike voltage. Otherwise, they will be susceptible to overheating and in that case permanently damaged. The power dissipation generated by capacitor's internal Equivalent Series Resistance (ESR) should also be considered. A small ESR will improve the system efficiency and reliability.

There are several different types of capacitors which can be considered. Electrolytic capacitors are most often used since they are not expensive and available with a wide range of RMS current ratings. The drawback to using electrolytic capacitors is that they are physically larger than other types of capacitors. Ceramic capacitors are better at high frequency and usually have a higher RMS current rating for a given package size with a lower ESR than other capacitor types, however they cost more [24]. No matter what type of capacitors we use, in some situations, it is possible to connect several capacitors in parallel in order to reduce the overall ESR and effectively in turn reduce the output voltage ripples.

If the desired operational frequency f_{SW} is 50 KHz, and the input voltage ripple is around or less than 0.5%-1% of the input voltage (we are using 1%), then the input capacitor can be found using equation (4.9).

$$C_{in} \geq \frac{(I_{out} - I_{in}) \cdot d_1 \cdot T_{SW}}{\Delta V_{in}} = \frac{(6.27 - 2.9) \cdot 0.462 \cdot 20\mu s}{0.01 \cdot 51.9} = 59.99\mu F \quad (4.9)$$

The maximum ESR of the input capacitor is also computed in equation (4.10) [25]. Here ΔI_{in} is the input current ripple, which is 20% of I_{mpp}.

$$ESR_{MAX} < \frac{1\% V_{in}}{\Delta I_{in}} = \frac{0.01 \cdot 51.9}{0.58} = 0.895\Omega \quad (4.10)$$

The current ripple going through the input capacitor C_{in} can be found out as $I_C = I_{out} - I_{in} = I_L - I_{in}$. Given the practical consideration of ESR, the total input voltage ripple is the summation of the voltage across ESR and the ripple voltage of the input capacitor as illustrated in Fig. 4.2.

As shown in Fig. 4.1, when the switch is off, the input current I_{in} charges the input capacitor C_{in}. When the switch is on, the input current I_{in} supplies the load, as the input capacitor discharges. Given the presence of ESR in the capacitor, voltage degradations include $I_{in} \cdot ESR$ due to charging and $(I_L - I_{in}) \cdot ESR$ due to discharging. The total input voltage ripple ΔV_{in} of the input capacitor can be derived using equation (4.11).

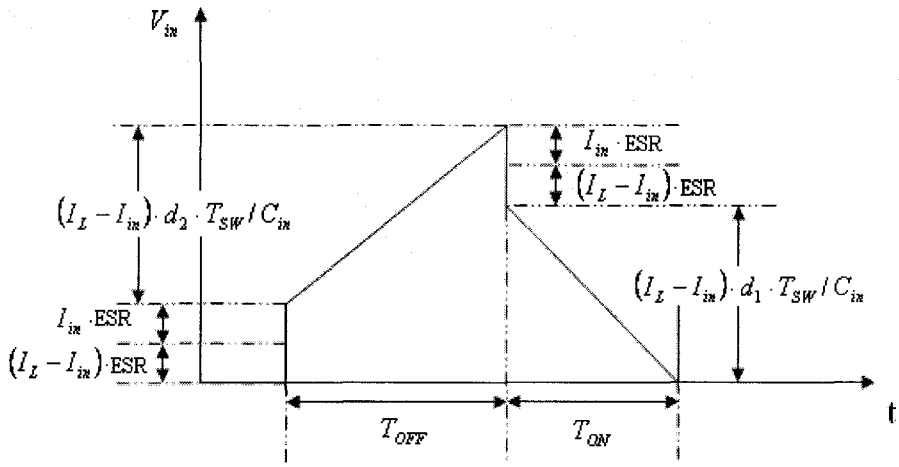


Fig. 4.2 Input Capacitor Voltage Ripple with Consideration of ESR

$$\Delta V_{in} = I_{in}\cdot ESR + (I_L - I_{in})\cdot ESR + \frac{(I_L - I_{in})\cdot d_2 \cdot T_{SW}}{C_{in}} \quad (4.11)$$
$$= I_{in}\cdot ESR + (I_L - I_{in})\cdot ESR + \frac{(I_L - I_{in})\cdot d_1 \cdot T_{SW}}{C_{in}}$$

According to equation (4.11), we can observe that a small ESR causes less voltage ripple. Based on the calculated value of 59.99μF, four 100μF polyester film capacitors are chosen (from AVX Corporation) for the two buck converters. They have 100V voltage rating, 10% tolerance, 24A of RMS maximum current, 0.55mΩ ESR, and can operate at temperatures of 105°C.

The two capacitors are connected in parallel, resulting in the equivalent of 200μF capacitance with a 100V rating and 0.275mΩ ESR, to be the input filtering capacitors. The minimum ripple voltage and maximum ripple voltage of the input filtering capacitors can be found out using equation (4.12) and (4.13) respectively.

$$\Delta V_{in\_\min} = I_{in} \cdot ESR + \left(I_{L\_\min} - I_{in}\right) \cdot ESR + \frac{\left(I_{L\_\min} - I_{in}\right) \cdot d_{1\_\max} \cdot T_{SW}}{C_{in}} \quad (4.12)$$

$$= 2.9 \cdot 0.275m\Omega + (5.23 - 2.9) \cdot 0.275m\Omega + \frac{(5.23 - 2.9) \cdot 0.555 \cdot 20\mu s}{200\mu F}$$

$$= 0.1308V$$

$$\Delta V_{in\_\max} = I_{in} \cdot ESR + \left(I_{L\_\max} - I_{in}\right) \cdot ESR + \frac{\left(I_{L\_\max} - I_{in}\right) \cdot d_{1\_\min} \cdot T_{SW}}{C_{in}} \quad (4.13)$$

$$= 2.9 \cdot 0.275m\Omega + (7.6 - 2.9) \cdot 0.275m\Omega + \frac{(7.6 - 2.9) \cdot 0.3815 \cdot 20\mu s}{200\mu F}$$

$$= 0.1814V$$

The maximum ripple voltage of the input capacitors is 0.1814V. This is merely 0.35% of the input voltage. This maximum ripple voltage satisfies the initial assumption made that the input ripple voltage is at least between 0.5% and 1% of the input voltage.

For the output capacitors it is important to satisfy the output voltage ripple requirement. To achieve a low output voltage ripple, the capacitor must have a low ESR under the normal operation of the circuit. If we assume that the output voltage ripple is 1% of its DC value (24V), then the output capacitor can be evaluated as:

$$C_{out} \geq \frac{V_{out}(1 - d_1) \cdot T_{SW}^{\ 2}}{8L\Delta V_{out}} = \frac{24 \cdot 0.538 \cdot (20\mu s)^2}{8 \cdot 0.245mH \cdot 0.24} \cong 11\mu F \quad (4.14)$$

We can double check for the value for the output capacitor by using the equation $f_c = \frac{1}{2\pi\sqrt{LC_{out}}} = (1 \sim 2)$ KHz (using 2KHz in the calculation).

This center frequency f_c should be far away from the switch frequency (50 KHz), so that the low-pass filter can essentially pass only the DC component of the voltage across the free-wheeling diode, and remove the switching harmonics. The output capacitor can be alternatively expressed in equation (4.15), and its maximum ESR is calculated in equation (4.16).

$$C_{out} = \left(\frac{1}{2\pi \cdot 2kHz}\right)^2 / L = 25.87\mu F \tag{4.15}$$

$$ESR_{MAX} < \frac{1\%V_{out}}{\Delta I_{out}} = \frac{0.01 \cdot 24}{2.536} = 0.095\Omega \tag{4.16}$$

The minimum capacitance value needed for the circuit is 25.87 μF. Four 20μF polyester film capacitors, with 100V voltage rating (10% tolerance), 2.6A of RMS maximum current, and 3mΩ ESR, were selected. By connecting two of them (for each buck) in parallel, this results in a total capacitance of 40μF with a 100V rating and the equivalent of 1.5mΩ ESR. The minimum and maximum ripple voltages of the output capacitors are shown in equation (4.17) and (4.18) respectively.

$$\Delta V_{out\_\min} = \frac{V_{out\_\min} \cdot (1 - d_{1\_\min}) \cdot T_{SW}^2}{8LC_{out}} = \frac{19.8 \cdot (1 - 0.3815) \cdot (20\mu s)^2}{8 \cdot 1mH \cdot 40\mu F} = 0.01531 \tag{4.17}$$

$$\Delta V_{out\_\max} = \frac{V_{out\_\max} \cdot (1 - d_{1\_\max}) \cdot T_{SW}^2}{8LC_{out}} = \frac{28.8 \cdot (1 - 0.555) \cdot (20\mu s)^2}{8 \cdot 1mH \cdot 40\mu F} = 0.01602 \tag{4.18}$$

The equivalent 40μF output capacitor gives a maximum 0.01602V ripple voltage. This ripple voltage is 0.067% of the output voltage and meets the requirement that the output ripple voltage is between 0.5% and 1% of the input voltage. Ultimately the filtering capacitors provide a means of smoothing the input and output current drawn from the PV array, maintaining the input and output current close to its DC value.

4.2.3 Diodes

Freewheeling Diode

Diode choice results in a trade-off of breakdown voltage, reverse leakage current, and forward voltage drop. The low forward voltage drop of a diode results in low power dissipations, better efficiency and smaller heat-sinks. In our case, a fast diode is needed to act as a switch for the energy stored in the inductor L. If the diode is slow to react, the efficiency of the buck converter will be low. The diode must have the ability to handle high breakdown voltages in case of high voltage transients and possible large output voltages if the load is suddenly disconnected. The minimum diode voltage V_D and current $I_{D(ON)}$ ratings are calculated using equation (4.19) and (4.20) respectively. Here, V_{OC} stands for the open voltage of the PV array, $I_{O(MAX)}$ represents the maximum current going through the inductor L, ΔI_L represents the inductor current ripple.

$$V_D = V_{OC} \cdot 1.5 = 66 \cdot 1.5 = 99V \quad (4.19)$$

$$I_{D(ON)} = I_{O(MAX)} + 0.5(\Delta I_L) = 6.27 + 0.5 \cdot 1.254 = 6.897A \quad (4.20)$$

The best combination of these features that could be found for the freewheeling diodes is High Voltage Schottky Rectifiers (part number is MBRF10H100 from Vishay Semiconductor). The selected diodes have a relatively lower forward voltage drop, and a good current capability that gives a faster reverse recovery than regular p-n junction diodes. They have a 100 V maximum repetitive peak reverse voltage, and 0.77 V maximum instantaneous forward voltage drop when the room temperature is 25°C and the maximum average forward rectified current is 10A.

Blocking Diodes

The rest of diodes were chosen to prevent currents flowing backwards from the batteries to the PV array. For simplicity, these blocking diodes are selected to be High Voltage Schottky Rectifiers (MBRF10H100) as well. But in general for Schottky diodes have a much higher reverse leakage current than non-Schottky ones. When reverse current leaks from the output batteries, the voltages across the drain-to-source of the MOSFET and the freewheeling diode in the buck converter build up and cause a voltage across the input capacitors. This voltage will influence the input voltage measurement, the voltage sensors for each buck converter should be arranged before the input blocking diodes and the input capacitors in the PCB layout.

4.2.4 MOSFET

Since the desired switch frequency 50 KHz is within a medium range and low voltage application such as less than 250V [26], using MOSFET as the switch over IGBT is a suitable choice in our case. The drain-to-source voltage V_{DS} rating should be at least

equal to 2 times the open voltage from the PV array if it is to be able to tolerate voltage spikes in a normal operating mode. The continuous drain current I_D rating has to be larger or equal to 1.5-2.0 times the short circuit current from the PV array. Thus the ratings of the MOSFET voltage and current can be evaluated in equation (4.21) and (4.22), where I_{SC} represents the short circuit current of the PV array and it is equal to 3.3A.

$$V_{DS} = 2 \times 66V = 132V \quad (4.21)$$

$$I_D \geq (1.5 \sim 2.0) I_{SC} = 6.6A \quad (4.22)$$

The choice of MOSFET will result in a tradeoff between conduction loss and gate drive power dissipation [27]. Given a maximum 200V drain-to-source voltage, a maximum 20 A drain current, 300W power dissipation, and an n-channel enhancement mode power MOSFET (IRFP24PbF) was selected from International Rectifier as the high speed-switching devices for MOSFET1 and MOSFET2.

The MOSFET has a maximum leakage current of 100 nA, maximum 4 V gate threshold voltage, and a relatively low on-state resistance of 0.18Ω @ Vgs = 10 V. It has a relatively low gate charge Q_g, the maximum value is 70 nC. If the voltage rating of the MOSFET is derated to 80% [26] of its maximum value of 200V, then the calculated 132V drain-to-source voltage rating is still within the range of 160V margin.

4.2.4.1 MOSFET Switching Characteristics

A typical MOSFET switching waveform with a resistive load is shown in Fig. 4.3. The turn-on delay time $t_{d(on)}$ is the time that is required to charge the input capacitance C_{iss} to the MOSFET's threshold voltage $V_{GS(th)}$. The rise time t_{rise} is the time after the gate-to-source voltage V_{GS} reaches to the $V_{GS(th)}$ to finish the transient. The drain current I_D of the MOSFET starts from zero and rises linearly to the output current I_{out}. The drain-to-source voltage V_{DS} of the MOSFET begins from the input voltage V_{in} and falling to the on-stage voltage. After the rise time t_{rise}, the V_{GS} rises to the overdrive voltage and the MOSFET is fully enhanced [28].

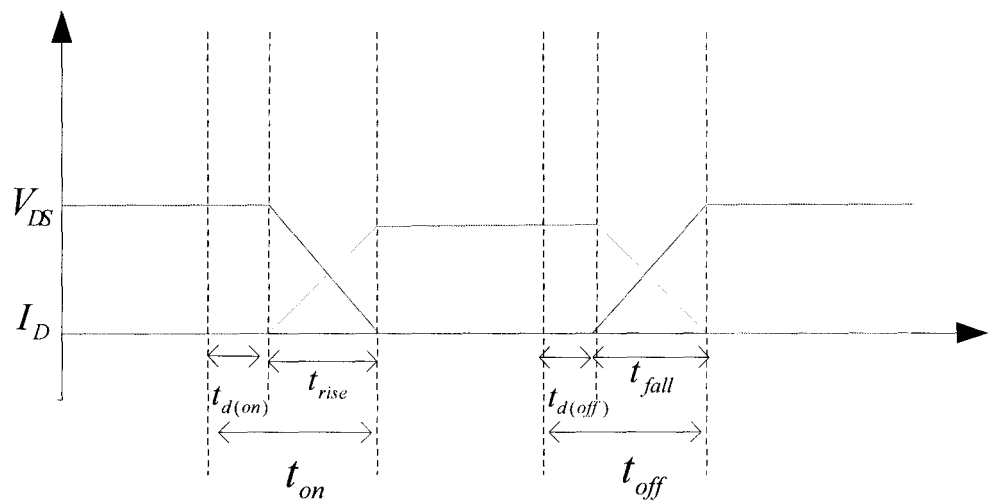


Fig. 4.3 Switching Waveforms of the Input Voltage V_{DS} and the Output Current I_{out}

The turn-off delay time $t_{d(off)}$ is the time required for the input capacitance C_{iss} to discharge from the overdrive voltage to the saturation region where the drain current I_D

remains saturated at the value of I_{out}. The fall time t_{fall} is the time that is required for the input capacitance to discharge from the saturation region to the $V_{GS(th)}$ [21]. The V_{DS} increases from the on-stage voltage to V_{in}, and the drain current I_D decreases from the output current I_{out} to zero. After the fall time t_{fall}, the V_{GS} decreases to zero, the MOSFET is fully turned off.

We define that the sum of $t_{d(on)}$ and t_{rise} as the turn-on time t_{on} and the sum of $t_{d(off)}$ and t_{fall} as the turn-off time t_{off}. During the times of $t_{d(on)}$ and $t_{d(off)}$, there are no changes to I_D and V_{DS}, the power dissipations do not occur. Thus the total power loss due to switching is taken into account only during the transitions of t_{rise} and t_{fall}. For simplicity, we assume that t_{rise}, t_{fall}, t_{on}, and t_{off} are approximately the same and are between 100ns and 200ns for the later calculations.

4.2.4.2 Gate Resistor and Gate-to-Source Resistor

Accordingly with the switching time dependency on charging time of the gate capacitor in a MOSFET, we can calculate the value of series gate resistance R_g as shown in equation (4.23) by using the total gate capacitor C_g and the rise time t_{rise} where $C_g = \frac{Q_g}{V_{gs}} = \frac{70nC}{10v} = 7\,nF$ and the time t_{rise} is assumed to be 150ns.

$$R_g = \frac{t_{rise}}{3 \cdot C_g} = \frac{150ns}{3 \cdot 7\,nF} \cong 7.1\Omega \qquad (4.23)$$

The value of R_g is chosen to be between 10Ω and 20Ω. Adding this externally passive gate resistor R_g results in slowing down the gate charging (or discharging) time, and in turn slowing down turn-on (or turn-off) time. In contrast, the resistor R_g is able to reduce EMI noise. The tradeoff among gate resistance loss, reduction of EMI noise, and switching speed needs to be made. A smaller gate resistor gives a faster transition and lower switching losses, but at the same time, means more ringing and induced additional EMI noise in the circuit generated by the fast slew rates of a MOSFET drain-to-source voltage [26][27][28]. Another resistance R_{gs} ($R_{gs} >> R_g$) can be added between the gate and the source of a MOSFET. Since the gate charge can be very large on a MOSFET, it causes the MOSFET to remain on even if the gate drive has been removed. Thus the purpose of adding this resistor R_{gs} is to release any excess charge of C_g safely from the gate in the event of this occurrence. The overall MOSFET protection circuit diagram is depicted in Fig. 4.4

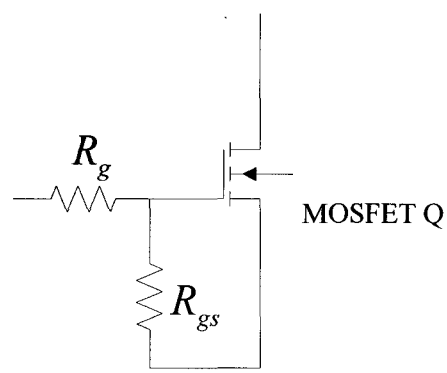


Fig. 4.4 MOSFET Protection Circuit

4.2.5 Heat-Sink

In power circuits, any losses in MOSFETs or Schottky diodes can heat up the silicon of the device above its maximum junction temperature $T_{j\max}$, which will lead to device performance failure [29]. Heat-sinks are used to dissipate heats, and their types are primarily dependant upon component power consumption, device package type, ambient temperature, and air flow.

The sources of a MOSFET loss can be grouped into four main categories: conduction loss, switching loss, charging MOSFET output capacitance loss, and gate drive loss. A detailed calculation is presented in equations (4.25) through (4.30).

Firstly a MOSFET is a resistive channel from drain-to-source, so the conduction loss $P_{R_{DS}}$ due to the resistance $R_{DS(ON)}$ between the source and the drain in the on-stage is shown in equation (4.25) [26]. The worse case occurs at the maximum duty cycle in the buck converter. This means that the operating voltage is at the maximum power point. Here I_{RMS} denotes average current going through $R_{DS(ON)}$, the symbol I_{out} denotes output current of a buck converter, and $d_1 = \frac{V_{out}}{V_{mpp}} = \frac{24}{51.9} = 0.462$ is the duty cycle when the switch is on and the operating voltage is at the maximum power point.

$$\begin{aligned} P_{R_{DS}} &= R_{DS(ON)} \cdot I_{RMS}^2 = I_{out}^2 \cdot R_{DS(ON)} \cdot d_1 \\ &= 6.34^2 \cdot 0.18 \cdot 0.462 = 3.34\,W \end{aligned} \qquad (4.25)$$

The conduction power $P_{R_{DS}}$ is not the only cause of power dissipation in a MOSFET. Dynamic power loss due to the switching behaviour of the MOSFET also

needs to be concerned. Given the fact that a high drain current I_D of the MOSFET (which is presumed to be the output current I_{out}) and a high drain-to-source voltage V_{DS} of the MOSFET are present in the device simultaneously for a short period of rise t_{rise} and fall t_{off} times as illustrated previously in Fig. 4.3. The energy stored E_{t_rise} in the MOSFET during the rise time t_{rise} can be approximated in equation (4.26), which is integration under the triangle area [21][27].

$$\begin{aligned} E_{t\_rise} &= \int_0^{t_{rise}} \left(V_{DS} - V_{DS} \cdot \frac{t}{t_{rise}} \right) \cdot I_{out} \cdot \frac{t}{t_{rise}} \cdot dt \\ &= \frac{1}{2} \cdot V_{DS} \cdot I_{out} \cdot t_{rise} - \frac{1}{3} \cdot V_{DS} \cdot I_{out} \cdot t_{rise} \\ &= \frac{V_{DS} \cdot I_{out}}{6} t_{rise} \end{aligned} \quad (4.26)$$

Likewise, the energy loss E_{t_fall} during fall time t_{off} can be estimated in a similar way, thus the average power loss P_{SW} due to the switching actions with the desired switching frequency f_{SW} of 50 KHz is shown in equation (4.27) if the times of t_{on} , t_{off} , t_{rise}, t_{fall} are assumed to be same and equal to 200ns.

$$\begin{aligned} P_{SW} &= \left(E_{t\_on} + E_{t\_off} \right) \cdot f_{SW} \\ &= \left(\frac{V_{DS} \cdot I_{out}}{6} t_{rise} + \frac{V_{DS} \cdot I_{out}}{6} t_{fall} \right) \cdot f_{SW} \\ &= \frac{1}{6} \cdot V_{in} \cdot I_{out} \cdot f_{SW} \cdot \left(t_{rise} + t_{fall} \right) \\ &= \frac{1}{6} \cdot 51.9V \cdot 6.34A \cdot 50KHz \cdot \left(200ns + 200ns \right) = 1.1\,W \end{aligned} \quad (4.27)$$

The power loss $P_{C_{OSS}}$ associated with charging and discharging the MOSFET's output capacitance C_{oss} can be evaluated as:

$$P_{C_{OSS}} = \frac{1}{2} C_{oss} \cdot V_{in}^2 \cdot f_{SW} = \frac{1}{2} \cdot 400pF \cdot 51.9^2 \cdot 50kHz = 0.027W \quad (4.28)$$

For the power loss in the gate driving circuit, we can view this power dissipation as a result of charging and discharging the total gate capacitor C_g in order to turn the MOSFET on and off. The power loss in the gate driver circuitry can be expressed in equation (4.29), where V_{drive} is the MOSFET driving voltage in the experiment. The total power loss of the MOSFET is then represented by equation (4.30) [28].

$$P_{drive} = C_g \cdot V_{drive}^2 \cdot f_{SW} = 7nF \cdot (14V)^2 \cdot 50kHz = 0.069W \quad (4.29)$$

$$P_{MOSFET} = P_{R_{DS}} + P_{SW} + P_{C_{OSS}} + P_{drive} = 4.536W \quad (4.30)$$

To estimate the thermal resistance of heat-sink $R_{\theta sa}$, according to the MOSFET's datasheet, the thermal resistance from Junction-to-Ambient $R_{\theta JA}$ is 40°C/W, the thermal resistance of device is 0.83°C/W, the thermal resistance of interface material is 0.24°C/W, and the maximum allowable junction temperature T_{jmax} is 150°C. If we assume that the maximum allowable junction temperature is derated to 80% of its value (150°C), and the ambient temperature is 50°C, then thermal resistance of heat-sink $R_{\theta sa}$ can be calculated in equation (4.31):

$$R_{\theta sa} = \frac{(80\% \cdot T_{jMAX} - T_a)}{P_{MOSFET}} - (R_{\theta IC} + R_{\theta CS}) \quad (4.31)$$
$$= \frac{(0.8 \cdot 150 - 50)}{4.536} - (0.83 + 0.24)$$
$$= 14.36°C/W$$

Therefore, a heat-sink will be required with a thermal resistance less than or equal to 14.36°C/W.

For freewheeling diodes, the power dissipation due to conduction P_{d_cond} is presented in equation (4.32). It depends on the forward conduction current I_D (here is I_{out}), the forward voltage drop $V_{forward}$, and the duty cycle d_1. Here I_{RMS} represents the average current going through the diode.

$$P_{d\_cond} = V_{forward} \cdot I_{RMS} = V_{forward} \cdot I_{out}\sqrt{(1-d_1)} \quad (4.32)$$
$$= 0.77 \cdot 6.34 \cdot \sqrt{0.367} = 2.96W$$

The power dissipation due to diode reverse recovery P_{d_rev} is determined in equation (4.33). By substituting these two calculated values in equation (4.34), we can find out the total power loss P_{diode} in one diode. Where Q_{rr} denotes the total reverse recovered charge.

$$P_{d\_rev} = Q_{rr} \cdot V_{ds} \cdot f_{SW} = 8.823nC \cdot 51.9V \cdot 50KHz = 0.023W \quad (4.33)$$

$$P_{diode} = P_{d\_cond} + P_{d\_rev} = 2.96 + 0.023 = 2.983W \quad (4.34)$$

The thermal resistance of heat-sink $R_{\theta sa}$ for the Schottky diode can be evaluated using equation (4.35). Therefore, a heat-sink will be required with a thermal resistance less than or equal to 20.53°C/W.

$$R_{\theta sa} = \frac{(80\% \cdot T_{jMAX} - T_a)}{P_{diode}} - (R_{\theta JC} + R_{\theta CS}) \qquad (4.35)$$
$$= \frac{(0.8 \cdot 150 - 50)}{2.983} - (2.7 + 0.24) = 20.53°C/W$$

4.2.6 Battery Bank

A stand-alone PV system needs a device to store energy delivered from the PV modules. The input power produced from the source varies at any time accordingly with continuously changing climate conditions. We need batteries to provide power when the PV modules produce nothing at night or less than the electrical load requires during day time. Among numerous possible technologies today, the conventional lead-acid battery is the most used in the PV system based on its cost versus efficiency. Two 12V seal-lead-acid batteries (Exide 51R-60) were chosen, which can tolerate long periods of inactivity, and each has 530 CA, 450 CCA, and 70 RCminutes at 25A. Connecting the two in series can achieve desired 24V at the output of two parallel-coupled buck converters.

4.3 Control Units

4.3.1 Voltage Sensor and its Conditioning Circuit

A voltage sensor can be constructed by a simple potential divider (resistor-network) to generate an analogue voltage signal that is proportional to the PV panel

voltage. The resistor-network is followed by a voltage follower providing a high impedance input to an RC low pass filter, and two clamping diodes to protect the control chip (56F8013) from voltage spikes. The circuit diagram is illustrated in Fig. 4.5. Since the control chip can only process digital information, A/D conversions are required.

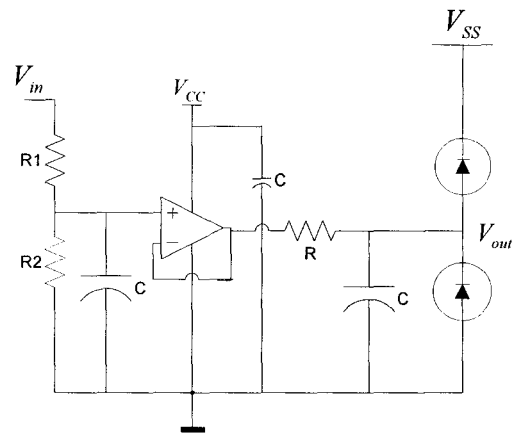


Fig. 4.5 Voltage Divider with its Conditioning Circuit

The sampled voltage from the voltage divider network is encoded as an analog signal and must be converted to binary numbers that are understood by the control chip.

The internal A/D reference voltage is V_{SS} (3.3V), is the voltage supplied to the control chip. To sample the voltages from the input PV arrays and the batteries, the resistor-networks has to scale the voltages down to within a safe margin. We use 3.1V as the reference voltage to calculate resistors in the circuit design. As seen from Fig. 4.5, the resistor ratio used for the input voltage divider network can be computed as:

$$\frac{R_1}{R_2} = \frac{1 - V_{SS}/V_{in}}{V_{SS}/V_{in}} = \frac{1 - 3.1/66}{3.1/66} = 20.29 \qquad (4.36)$$

The values of R_1 and R_2 can be chosen as long as they have a ratio close to that given in equation (4.36). Using R_1= 200 kΩ, and R_2 = 10 kΩ, the input resistor-network results in 3.143V if the input voltage generated from the PV array is at its maximum 66V.

More importantly, these resistor networks should be inserted before the blocking diodes and the input filtering capacitors so that the measured values are the actual voltages from the PV array. Otherwise, the voltage measurements will be affected by the reverse current leaking from the output blocking diodes.

Similarly for the batteries voltage, the ratio between the output voltage (24V) and the supply voltage of the control chip V_{SS} (3.1V) can be calculated using the same relationship of equation (4.36), the resulted ratio is 8.25. Using R_1= 820 kΩ, R_2 = 100 kΩ, the output resistor-network gives 3.13V when the output batteries are fully charged to 28.8V.

4.3.1.1 RC filter

RC filters can filter out the circuit noise and make the sampled signals smooth. The center frequency f_c given by the desired RC filter must be far less than the switching frequency f_{SW} (50 KHz). The relationship between the center frequency of the RC filter and the circuit switching frequency is given in equation (4.37), the circuit is also shown in Fig. 4.5.

$$f_c = \frac{1}{T_c} = \frac{1}{2\pi RC} << f_{SW} \qquad (4.37)$$

4.3.1.2 Over-voltage Protection

The voltage follower is constructed from an operational amplifier (MC34074A). The voltage supply range of the MC34074A is between 3.0V and 44V. Due to stability, choosing 5.0V as its voltage supply V_{CC} is fairly good. In contrast, the 56F8013 chip's recommended maximum operating voltage V_{SS} is 3.3V, thus we need two diodes connected as shown in Fig. 4.5 to protect the control chip from over-voltage.

4.3.1.3 Voltage Sensing Test Result

The input voltage sensing circuit was tested. The voltage difference between the calculated data and experimental data are shown in Table A.1 of Appendix A. The percentage between the error and the calculated value is plotted in Fig. 4.6.

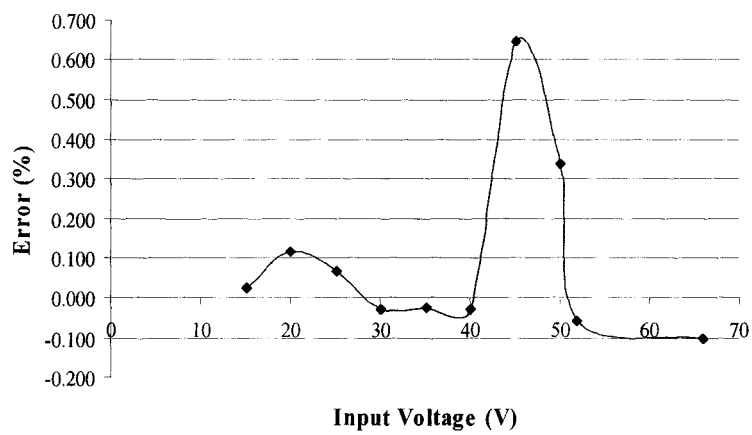


Fig. 4.6 Voltage Error between Calculated and Measured Data

It shows that the maximum error in percentage is 0.9%, and the average error in percentage is 0.096%. Given ±1% accuracy of the resistors in the voltage sampling circuit, the accuracy of the voltage sensing circuit is acceptable.

4.3.2 Current Sensor

Current transducers LTS 6-NP and LTS 25-NP were chosen to be the input current sensor and output current sensor respectively. They are devices that contain both hall-effect sensors and a high gain integrated circuit amplifier in a single package. Their features include a closed loop current transducer using the Hall-effect, unipolar voltage supply, insulated plastic case, and extended measuring range.

Compared to the conventional current sensors which use shunt resistors and operational amplifiers, the LTS current transducers do not require additional shunt resistors and thus have no insertion losses. They offer excellent accuracy (±0.2%), very good linearity, optimized response time, galvanic isolation between primary and secondary circuits, and very high immunity to external interference.

Since the maximum input current (the short circuit current generated from the PV array) is 3.3A, we selected the LTS 6-NP with a maximum 6A current range for the input current sensor. Its output voltage formula was taken from its datasheet, and is shown in equation (4.38):

$$V_{CS} = 2.5 + 0.625 \times \frac{I_{in}}{\text{Current Range}} \qquad (4.38)$$

The equivalent output voltage V_{CS} range of LTS 6-NP is calculated between 2.5V and 2.9167V if the input current range is between 0A and 4.0A where I_{in} denotes the current from solar array, and V_{CS} represents the output voltage from the current sensor.

Since the maximum output current is 17A, we choose the current sensor (LTS 25-NP) with a 25A maximum current range as the total output current sensor. The equivalent output voltage calculation is shown in equation (4.38) and expressed in equation (4.39). The equivalent output voltage V_{CS} range of LTS 25-NP was calculated as falling between 2.5V and 2.925V if the output current range is between 0A and 17A.

$$V_{CS} = 2.5 + 0.625 \times \frac{I_{out}}{25} \qquad (4.39)$$

With such a small voltage range (0.425V) between 2.925V and 2.5V, a conditioning circuit is desperately needed to magnify the sampling range and increase the precision so that the usable range of the A/D bits is increased. The proposed current sensing conditioning circuit is schematically shown in Fig. 4.7.

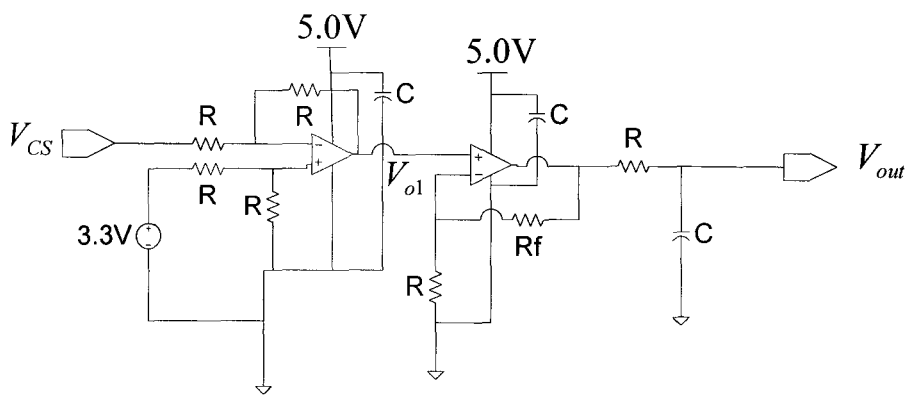


Fig. 4.7 Current Sensing Conditioning Circuit

The circuit is constructed using a differential amplifier (offset circuit) and non-inverting (magnifying circuit) amplifier. Based on the above circuit diagram, the offset circuit can

be expressed in equation (4.40) and the magnifying circuit can be mathematically written in equation (4.41).

$$V_{o1} = 3.3 - V_{CS} \tag{4.40}$$

$$V_{out} = \frac{R + R_f}{R} V_{o1} \tag{4.41}$$

Substituting equation (4.38) and (4.40) into equation (4.41), the relationship between the input current I_{in} from solar source and the output voltage V_{out} fed to the ports can be expressed as:

$$V_{out} = 3.2 - 2.5 \cdot \frac{I_{in}}{\text{Current Range}} \tag{4.42}$$

The input current sensing circuit with 6A current range, and using R = 100 kΩ and R_f = 300 kΩ, the equation (4.42) becomes equation (4.43):

$$V_{out} = 3.2 - 2.5 \cdot \frac{I_{in}}{6} = 3.2 - 0.4167 \cdot I_{in} \tag{4.43}$$

When the input current is 0A, the output voltage is 3.2V. If the input current is 4.0A, the output voltage is 1.53V. The output voltage sensing range is now between 1.53V and 3.2V, the difference is 1.67V. The original range 0.4167V is enlarged to 1.67V, which is magnified 4 times.

Similarly for the output current sensing circuit with the same equation but different current range (25A) then equation (4.42) becomes equation (4.44):

$$V_{out} = 3.2 - 2.5 \cdot \frac{I_{out}}{25} = 3.2 - 0.1 \cdot I_{out} \quad (4.44)$$

When the output current is 0A, the output voltage is 3.2V. If the output current is 17.0A, the output voltage is 1.5V. The output voltage sensing range is between 1.3V and 3.2V, and their difference is 1.7V. Thus the original sensing range 0.425V is enlarged to 1.7V, which represents a magnification of 4 times.

4.3.2.1 Current Sensing Test Result

The proposed input and output current sensing circuits were tested. For simplicity, only accuracy estimation of the input current sensing circuit is derived in equation (4.45). Here ΔI_{in} represents the current difference between the calculated input current and the measured input current, and ΔV_{out} represents the voltage difference between the calculated voltage after the conditioning circuit and the measured voltage after the conditioning circuit.

$$\Delta I_{in} = \frac{\Delta V_{out}}{0.4167} \quad (4.45)$$

The experimental data is shown in Table A.2 of Appendix A and the corresponding data is plotted as seen in Fig. 4.8 and Fig. 4.9 respectively.

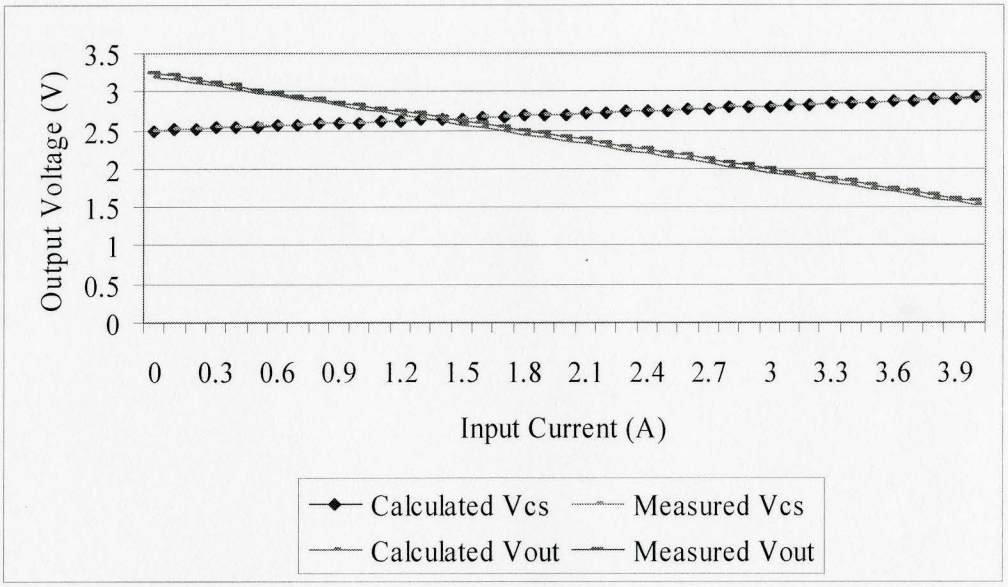


Fig. 4.8 Comparison between Calculated and Measured Data of Input Current Senor LTS 6-NP

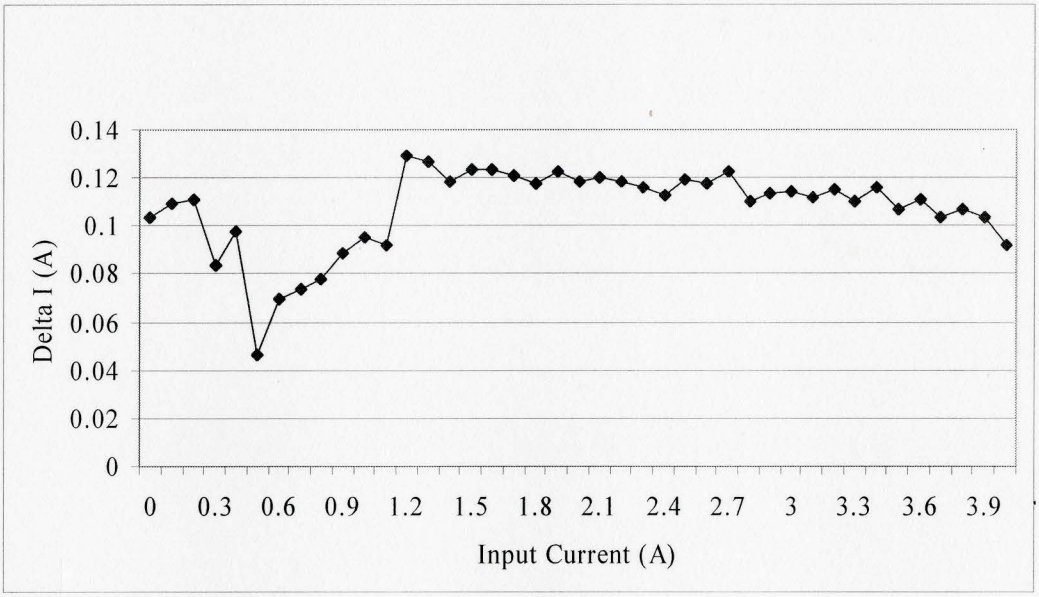


Fig. 4.9 Measured Error of the Input Current Sensing Circuit

As shown in Fig. 4.8, there are small deviations between the measured output voltage and the calculated output voltage. These deviations are caused by both the ±0.2% accuracy

variation of the current transducer, and by the ±1% accuracy of the resistors, or the temperature drift in the operational amplifiers. Fig. 4.9 shows that the maximum error is 0.1293V, the average error in the input current sensing circuit is 0.10718V, and the maximum error in percentage is 2.77%. Further precision can be achieved by properly adjusting the software which measures the input and output sensing circuits, such as the averaging filtering algorithm.

4.3.3 Gate Drive Method 1: MOSFET Driver

The PWM current signals generated by the control chip can only deliver a maximum current of 8mA. A MOSFET driver (MIC4427) is chosen to boost the current. The MIC4427 family provides highly-reliable dual non-inverting low-side MOSFET drivers with low power consumption and a high efficiency. This MOSFET driver operates at current as low as 1.5mA and is capable of supplying two independent peak output currents up to 1.5A, and its rise and fall times are matched.

To guarantee low supply parasitic inductance over a wide frequency range [30], paralleled bypass capacitors are needed for the power supply. Normally one 1μF ceramic capacitor connected in paralleled with a small 1000pF-4700p ceramic capacitor will adequately reduce voltage spikes [30]. Bypass capacitors are required for all operational amplifiers and optocouplers voltage supplies for the same reason.

In our case, the minimum supply voltage V_{CC_min} of MIC4427 is 4.5V. A 1μF ceramic capacitor was chosen to be the supply bypass capacitor C_{bypass}. The existing voltage ripple ΔV in the supply voltage can be computed as:

$$C_{bypass} \cdot \Delta V = C_g \cdot V_{drive} \rightarrow \Delta V = \frac{C_g \cdot V_{drive}}{C_{bypass}} \quad (4.46)$$

Substituting C_g =7nF, V_{drive} =14V, and C_{bypass} =1μF in equation (4.46), the calculated voltage ripple ΔV is 0.098V. The voltage difference (4.902V) between the voltage supply (5.0V) and the calculated voltage ripple (0.098V) is higher than the minimum supply voltage V_{CC_min} (4.5V) requirement.

4.3.3.1 Gate Driver Transformer

The need for a floating gate drive makes the MOSFET driving circuit more complicated. There are several approaches. One could use a high-side MOSFET driver, although it is expensive. An optical coupler is also a good option, but it requires isolated power supplies for each MOSFET as well as switching characteristics above 50KHz. A gate drive transformer called pulse transformer is a traditional choice, it is reliable and most importantly galvanic isolation can be easily achieved [31][32].

The MIC4427 MOSFET driver is for the low-side MOSFET, a gate drive transformer is thus needed to interface the high-side MOSFET with the ground-connected PWM control circuit. Unfortunately the transformer itself has several limitations. The transformer generates only AC signals, and its operating duty cycle is limited due to the reset time of the transformer's core. The transformer needs some extra components to improve the overall circuit performance. There are different design options for the high-side gate drive application; one example is illustrated in Fig. 4.10.

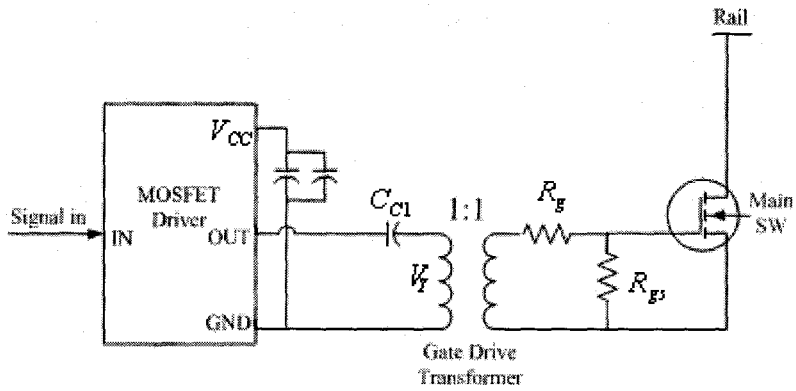


Fig. 4.10 Gate Drive Transformer

The coupling capacitor C_{C1} offers the reset voltage for the magnetizing inductance in the transformer. It is charged during the switch-on time, and provides negative bias voltage to the transformer during the switch-off time [33]. However, at large duty cycles, there may not be enough voltage to turn the MOSFET on. Additional elements including another coupling capacitor C_{C2}, a clamping diode, and a low power floating PNP transistor are necessary to add to the secondary side of the transformer in order to restore the DC value of the gate drive and improve the gate turn-off speed at the same time [33][34] as shown in Fig. 4.11.

During the switch-on time, the MOSFET is turned on by the summation of the voltage across the secondary winding of the transformer V_T and the voltage across the second coupling capacitor $V_{C_{C2}}$. During the switch-off time, the primary coupling capacitor C_{C1} is connected in paralleled with the primary winding of the transformer, the clamping diode is forward-biased, and the secondary coupling capacitor C_{C2} is thereby charged on its right side.

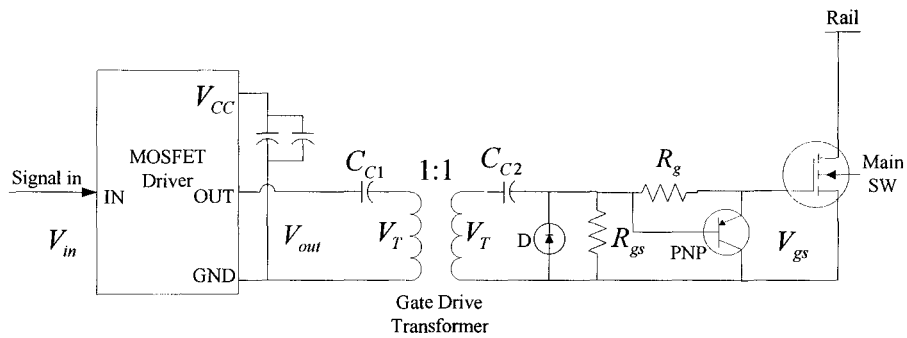


Fig. 4.11 The Proposed Gate Drive Transformer

Meanwhile the PNP transistor is turned on and this causes the gate-to-source voltage V_{gs} of the MOSFET to clamp to zero, so that the MOSFET is turned off. In addition, the gate resistor is here to limit the turn-on speed. The gate-to-source resistor provides a current path. Consequently, with the proposed gate drive transformer circuit, a low-side MOSFET driver is allowed in this application.

4.3.3.2 Experimental Results of Gate Drive Transformer

The proposed gate drive transformer circuit was tested. The purchased pulse transformer (610AA) has a relatively large leakage inductance, and this inductance lead to time delays and oscillations in the gate drive circuit [35] so that the resulted rise time or fall time was around 640ns as illustrated in Fig. A.1 and Fig. A.2 in Appendix A. The turn-on and turn-off times were much longer than our assumption that is between 100ns and 200ns. Even though we let R_g be equal to zero, the time delay did not meet our goal. Furthermore in the MPPT application, at wide duty cycles, such as in the buck converter, the duty cycle could be between 0% and 100% result in the extreme case. Using a gate

drive transformer is difficult to support in this case. As a result, the gate drive circuit design is opted for the method 2 described in the following section.

4.3.4 Gate Drive Method 2: Gate Drive Optocoupler

The gate drive optocoupler (HCPL-3120 from AVAGO Technologies) integrates an LED light source and optical receiver for safety isolation. It has transistors to provide the minimum 2.0A peak output current, which is possible to directly drive a MOSFET. The gate drive optocoupler with a high-side MOSFET is shown in Fig. 4.12. Here R_{limit} is a resistor between the PWM port and the input side of the optocoupler and used to limit the input current going through the photodiode. HCPL-3120 has a broad supply voltage V_{CC} range between 15V and 30V, and 2500 V_{RMS} for 1 minute [36]. An isolation of 630V is high compared to the open circuit voltage 66V generated from the PV array. In contrast with the circuit which used the gate drive transformer, the new circuit becomes much simpler, although it will need extra isolated power supplies.

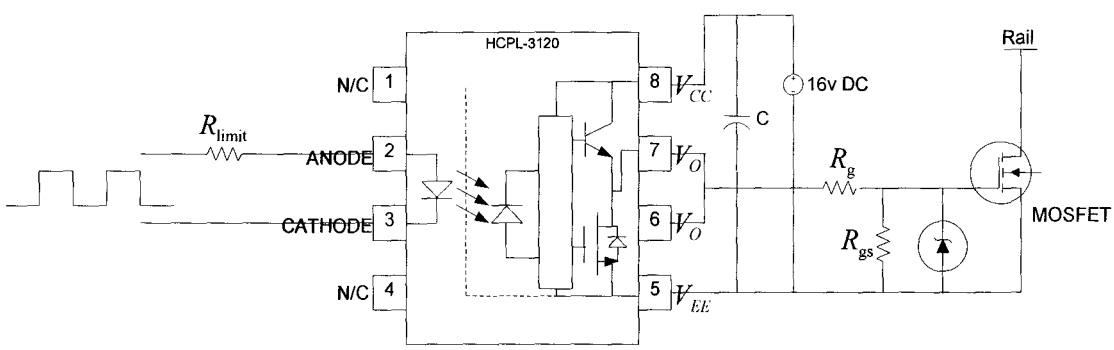


Fig. 4.12 Gate Drive Optocoupler with a High-Side MOSFET

4.3.4.1 Final Solution for High-Side MOSFET Driving

The ADC ports (in 56F8013 control chip) are capable of tolerating 5.0V [37]. The diodes used in the voltage sampling circuits for the over-voltage protection can be eliminated to simplify the circuit design and save space in the PCB layout. The final solution for the high-side MOSFET driving circuit is illustrated in Fig. 4.13.

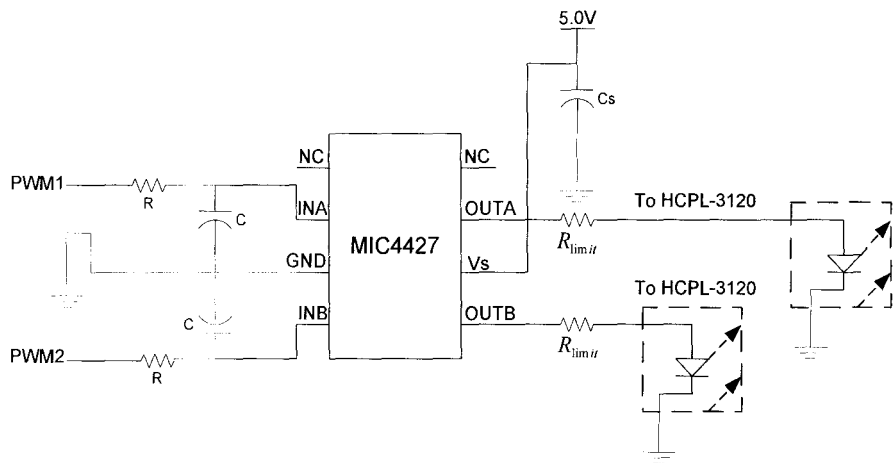


Fig. 4.13 Final Solution for High-Side MOSFET Driving

Only one MIC4427 driver is used to increase the input currents from the control chip to each photodiodes. Given a maximum 25mA forward current $I_{f\max}$ and a maximum 1.8V forward voltage $V_{f\max}$ of the photodiode in the HCPL-3120 optocoupler, we can calculate the components R_{limit} in equation (4.48) with a power consumption P_R of 0.08W as shown in equation (4.49).

$$R_{limit} = \frac{V_s - V_{f\max}}{I_{f\max}} = \frac{5.0 - 1.8}{25m} = 128\Omega \qquad (4.48)$$

$$P_R = \frac{V^2}{R_{limit}} = \frac{(5.0-1.8)^2}{128} = 0.08W \quad (4.49)$$

Resistors between 100Ω and 180Ω with 0.25W rated power can be selected.

4.3.4.2 Isolated DC-DC Converter

It is meaningless to use a regular voltage supply in a gate drive optocoupler to isolate digital signals from analog signals for surge protection. The voltage supply of the gate drive optocoupler itself obviously should be isolated as well. Four isolated dc-dc converters (AV10-24S08) are chosen to supply the gate drive optocouplers. The converter converts 24V input voltage to 8V output voltage with a high efficiency, an optoisolator is used inside to maintain complete isolation between primary and secondary. Since the recommended supply voltage of the gate drive optocoupler is between 15V and 30V, the inputs of two converters can be connected in parallel (and this 24V voltage can be actually supplied by the 24V batteries) and their outputs are connected in series, in order to provide 16V output voltage.

4.3.4.3 The Proposed High-Side MOSFET Driving Experiment

A close-loop circuit for the proposed high-side MOSFET driving was at last constructed and tested in a buck converter. A GEN600-2.6 was used as the input voltage source, two 12V batteries were connected in series as the load. The voltage waveform across the gate and source of the MOSFET was measured by an oscilloscope. When the duty cycle was set to be 50%, the waveform of V_{gs} is shown in Fig. A.3 in Appendix A.

The magnitude of the gate-to-source voltage V_{gs} of the MOSFET is around 14V, this voltage is smaller than the optocoupler's supply voltage (16V) because of the voltage degradation caused by resistances in the driving circuit. The waveform of V_{gs} has drooping edges, which are caused by the resistor R_{gs} and the parasitic components in the circuit. The rise and fall times are both within 200ns as shown in Fig. A.4 and Fig. A.5 in Appendix A. The waveform of the drain-to-source voltage V_{ds} of the MOSFET was also examined and shown in Fig. A.6 and Fig. A.7 in Appendix A. There are no spikes involved in the waveform thus snubber circuits are so far not needed.

4.3.5 Linear Voltage Regulator

The voltage supplies of some selected components (like operational amplifiers, MIC4227, etc.) are all 5.0V. This 5.0V voltage supply can be achieved by using one isolated dc-dc converter (AV10-24S08) and a linear voltage regulator (L78M05CV), the circuit diagram is shown in Fig. 4.14.

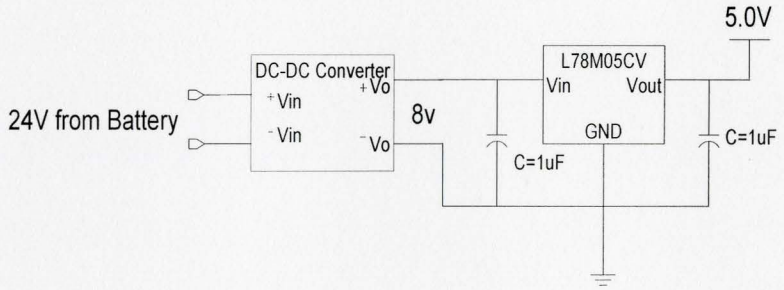


Fig. 4.14 Construction of 5.0V Voltage Supply

This 5.0V voltage source supplies all the current sensors, Op-amps, and one MIC4427. The output voltage 8.0V from the isolated converter supplies the 56F8013 demonstration

board. The current I_{reg} draw from this voltage regulator is approximately the summation of the currents into the CPU (I_{CPU}), the Op-amps (I_{op}), and the MIC4427s (I_{4427}). The power loss due to this voltage regulator can be evaluated as:

$$\begin{aligned} P_{reg} &= V_{reg} \cdot I_{reg} = V_{reg} \cdot (I_{CPU} + I_{op} + I_{4427}) \\ &= 8V \cdot (200mA + 2mA + 10\mu A) \\ &\cong 8V \cdot 202mA = 1.616W \end{aligned} \quad (4.50)$$

The lower input voltage, the less power dissipation. Similarly a 3.3V voltage supply can be obtained using a linear voltage regulator LM1117 instead of L78M05CV.

4. 4 Final MPPT Hardware Design Solution

4.4.1 Final MPPT Schematic Diagram

Both power-stage circuits and control-stage circuits were constructed, evaluated, and tested. Some necessary modifications were done, and the final proposed maximum power point tracker (MPPT) schematic diagram is presented in Fig. A.8 of Appendix A. The proposed circuit consists of two buck converters each with independent driving and conditioning circuits. Two high-side MOSFETs are isolated using gate drive optocouplers. The measured voltages (using resistor-networks) and currents (using current transducers) are fed into the voltage-conditioning block, which offsets and scales the measured voltages down to the desired levels (between 0V and 3.3V), ready for the analog-to-digital converters of the 56F8013 control chip to sample. Three auxiliary voltage supplies, including 3.3V, 5.0V and 24V, are used in the circuit.

4.4.2 Printed Circuit Board Layout Issues

High noise due to the switching buck converters is produced in the circuit. The noise propagates through conduction and radiation. A bad layout of components in a PCB board can negatively affect system performance, lead component failures or cause the system to operate in an abnormal mode. For instance, a bad placement of a MOSFET and its gate resistor could lead to a huge voltage spike across the drain and source of the MOSFET, the high voltage would make the MOSFET fail. A poor placement of supply bypass capacitors could cause a large parasitic inductance and make the supply voltage unstable. As a result, proper component selection, good placement of components in a PCB can effectively reduce a certain amount of parasitic circuit components, and in turn reduce conducted and radiated EMI, and cause less component failures and keep the converter's performance stable [38].

4.4.2.1 Parasitic Components in PCB Layout

When two or more conductors are placed in a close space, they are capacitively coupled as seen in Fig. 4.15.

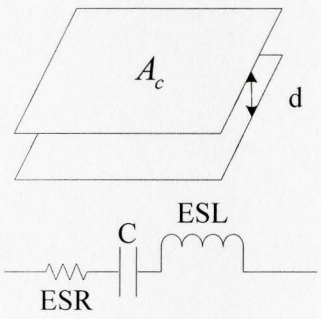


Fig. 4.15 Capacitor Structure and its Parasitic Components

These undesired parasitic capacitors will couple signals from one circuit to another. We know that capacitance is inversely proportional to the distance d between the two adjacent conductors and proportional to the surface area A_c of the conductors as expressed in equation (4.51). Here ε_0 is the permittivity of a vacuum and ε_r is the relative permittivity. In order to reduce the conducted noise caused by the parasitic capacitors, we need to minimize the surface area A_c of the conductors or keep the separation distance d large [38].

$$C = \varepsilon_r \varepsilon_0 \frac{A_c}{d} \tag{4.51}$$

For an inductor, normally each turn of a coil is covered with wire insulation, which forms a small capacitor between each pair of turns. This results in adding these capacitors in series and forming an equivalent capacitor C_p in parallel with the inductor L as illustrated in Fig. 4.16.

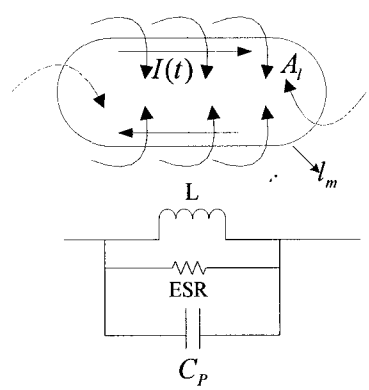


Fig. 4.16 Single-turn Air-core Inductor Structure and its Parasitic Components

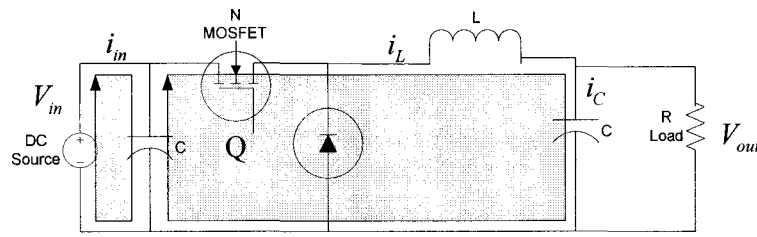
In a buck converter, this parallel capacitor C_p provides a path for the inductor (or output) current to the output capacitor and the load, which usually results in spikes on the output voltage. From Fig. 4.16 and equation (4.52), we learn that the parasitic inductance is proportional to the loop area A_l and inversely proportional to the effective magnetic path length l_m [39]. Where μ_0 is the permeability of vacuum. In order to reduce parasitic inductance, we need to reduce the loop area A_l or increase the effective magnetic path length l_m.

$$L = \mu_0 \frac{A_l}{l_m} \qquad (4.52)$$

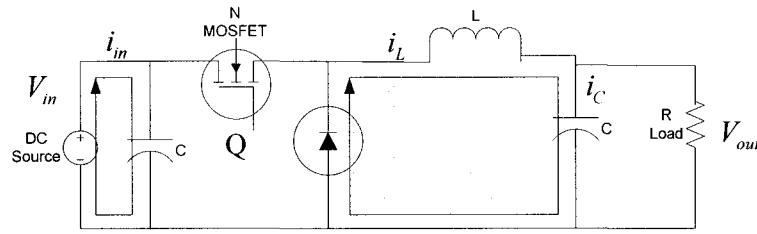
4.4.2.2 Minimize Current Loop in PCB Layout

Despite the undesired parasitic elements in a non-ideal circuit, current loops not only increase the inductance of conductors, but also radiate magnetic fields, especially in the high-current paths. Hence, the input current loop and output current loop are the primary source of radiated noise in a converter circuit. The placement of MOSFETs, Schottky diodes, inductors, input capacitors and output capacitors in the final PCB layout is critical to the overall circuit's proper operation and interaction.

To understand the radiated magnetic field generated by the large current loop, refer to Fig. 4.17 (a) and (b), consider only one buck converter as an example. When the MOSFET changes from ON to OFF, the current loop area as seen from (a) to (b) is changed quickly.



(a) MOSFET ON



(b) MOSFET OFF

Fig. 4.17 Different Current Loops when the MOSFET is ON and OFF

From equation (4.53), we know that magnetic flux φ_m is proportional to its magnetic field density B and its loop area dS [40] [41].

$$\varphi_m = B \cdot dS \tag{4.53}$$

$$\varepsilon mf = \oint E \cdot dS = -\frac{\varphi_m}{\partial t} \tag{4.54}$$

Faraday's law (as shown in equation (4.54), where E is electric field) states that the induced voltage εmf in a closed loop equals the negative of the time rate of change of magnetic flux through the loop, this means that the induced εmf is generated by a changing magnetic environment. As a result, when the MOSFET is turned ON to OFF, or

OFF to ON, the magnetic flux is changed, and from the above relationship, we know that a change of the magnetic flux through a loop of conductive trace induces an unwanted voltage along another trace. Therefore, to reduce the radiated magnetic field problem the current change loop area must be made as small as possible [40].

Refer back to Fig. 4.17, during a normal operation of a buck converter, the input current is discontinuous. Adding an input filtering capacitor can supply the excess current when Q1 is on, and store the charges from the input current when Q1 is off, and thus the input capacitor sees discontinuous current. In reality, a finite capacitance given a certain amount of ESR and ESL, the actual voltage across the input capacitor fluctuates over partial charging and discharging cycles. By connecting an additional low impedance bypass (ceramic) capacitor in parallel with the input capacitor, effectively not only does this reduce ESR and improve high frequency characteristic of the equivalent capacitor, but it also reduces the high frequency loop area, thereby reducing the overall parasitic inductance in the PCB layout.

Generally long lead traces or large loop areas will cause a large amount of ringing due to the inductance of the traces combined with the gate capacitance of a MOSFET. This ring causes EMI to radiate through the circuit board at a high switching frequency, and they are very difficult to suppress [42] [43]. To summarize, all of the power traces should be made as short and wide as possible, and importantly all of the power components should be placed as close to each other as possible. Thus the harmful effects, including radiated EMI, parasitic inductance, lead resistance, noise spikes, ringing, and induced voltages, can be mitigated.

4.4.2.3 Ground Plane

Ground is defined as a reference potential for linear circuit elements such as amplifiers, voltage references, and A/D converters etc. It is used as the return for power systems elements such as switching regulators, power amplifiers, and digital circuit blocks. It is also used as a shield to prevent the propagation of electromagnetic noise in the circuit. Because of these diverse uses, proper care must be taken in laying out the PCB ground system to avoid interference between different areas of the board [44].

A practical way to reduce crosstalk (parasitic impedance of return path) is to add a ground plane. Doing so will not only lower the overall parasitic impedance ground connections, but also will also provide more nearly equipotential ground references (since the larger continuous areas of ground plane, the shorter return current paths). However a poor layout of the ground plane can cause more problems, generally ground planes of sensitive circuits and noisy circuits should be separated. Ground loops typically have very small impedances; large currents can be very easily coupled into ground loops. They cause problems like ground bounce, signal distortion, and so on [44]. Thus ground loops should be avoided in the layout.

4.4.3 Design PCB Layout Using ORCAD 9.2

Using ORCAD version 9.2, PCB layout is designed using a 2-layer board and through-hole plating, the final PCB layout schematic diagram is given in Fig. A.9 in Appendix A, and the PCB layout design procedure is shown as following:

- Choose 2-layer PCB, named top and bottom, and design the PCB layout manually instead of autoroute

- If possible, the circuit main components should be located on the top layer, and the analog and digital areas should be separated
- Layout the critical parts first (for example, input capacitors, output capacitors, MOSFETs, freewheeling diodes, and inductors), and then layout the driving circuits, sampling circuits etc.
- Have all the high current (or power) paths on the top layer, and the return paths should be located on the bottom layer. In particular, overlap the power paths with the return paths in the power circuits. The overlap can effectively minimize high current loop area, resulting in a reduced EMI emissions and susceptibility. Keep all high current traces as short and as wide as possible
- Keep layout symmetrical if possible. In our case, the two buck converters are identical, and their outputs are parallel connected. Therefore they can be placed vertically mirror-imaged to each other
- The supply bypass capacitors should be placed as close as possible to the IC
- Add a big ground plane area under the driving, sampling, and voltage supplying circuits, but separated from the power return paths even though they both have the same netlist
- Avoid discontinuities in the ground plane
- Avoid the use of right angles, and sharp corners
- After the layout done, use "Design Rule Check" to check for errors on the board. If there are no errors, then we can generate the Gerber files and send to the factory to produce the designed PCB

In general no matter how heavy the current going through the power circuit or the driving circuit, or even sampling circuits, the overall loop track length, should be always kept as short as possible to minimize the inductance of the traces in the circuit board. By doing so, it will reduce most of the noise spikes, ringing, and resistive losses of wires or traces in the PC board.

4.5 Control Stage Hardware Purchased from Freescale

4.5.1 56F8013 Control Chip

The 56F8013 is a member of the 56800E core-based family of Digital Signal Controllers (DSCs). It combines, on a single chip, DSP performance and MCU functionality with a flexible set of peripherals to create a cost-effective solution for a broad range of power applications, such as motor control application, which require a greater number of PWM modules, but it also has been successful as a general purpose controller [45].

This project uses the Freescale 56F8013 chip to sense the continuously varying input voltages and input currents, and then calculate the corresponding power. An iterative algorithm can be employed to control the PWM duty cycles of the two DC-to-DC buck converters until the maximum power is found. Since 56F8013 is constantly searching for MPP generated on each PV array, both PV arrays will be operated at maximum efficiency under unpredictable varying weather conditions.

The 56F8013 block diagram is illustrated in Fig. A.10 of Appendix A. This control chip is well suited to this application, because it features:

- 12-bit ADCs, 9-bit accuracy
- 5 MHz ADC clock
- High-speed 6-output Pulse Width Modulator that can be clocked at up to 96MHz
- Serial communication interface (SCI) with LIN slave functionality
- 16KB of program flash

The MC-based controller was chosen since it is affordable, it provides excellent performance and a high level of peripheral and memory integration with unique features [46][47] and it has at least two PWM outputs and six A/D inputs ports.

4.5.2 56F8013 Demonstration Board

The 56F8013 demonstration board, shown in Fig. 4.18, is an evaluation module board. It contains a 56F8013 chip, RS-232 interface, 6 user LEDs, 2 user pushbutton switches, 9V at 450 mA DC power supply (gives 3.3 V by connecting a voltage regulator U3), a JTAG connector (J1) and a daughter card connector (P2), which allows signal monitoring and expandability of user features [48].

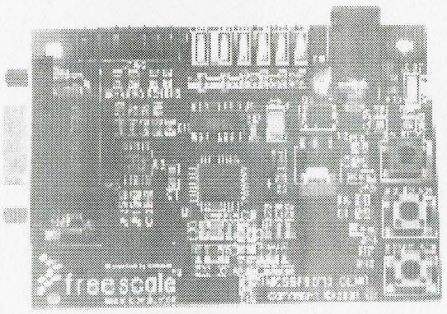


Fig. 4.18 56F8013DEMO Board [48]

The 56F8013 demonstration board can be adapted to develop real-time software and hardware products. The software platform allows users to write and simulate

algorithms, download the software to on-chip memory, run it, and debug it using a debugger via the JTAG/Enhanced OnCE (EOnCE) port. The hardware platform allows the user to connect external hardware peripherals. The on-board peripherals can be disabled, providing the user with the ability to reassign any and all of the processor's peripherals. The EOnCE port's unobtrusive design means that all memory on the board and on the processor is available to the user [48].

The power of the 16-bit 56F8013 processor, combined with the on-board RS-232 interface and daughter card connector, makes the 56F8013 demonstration board flexible enough to allow users to fully exploit the 56F8013's features to optimize the performance of products, and hence it is suitable for developing and implementing various MPPT control techniques [48].

4.5.2.1 ADC Accuracy Test

Applying different voltage signals to the six ADC ports, and comparing the calculated values to the actual reading data from a computer, we can find out the accuracy of the ADCs. By analyzing the data given in Table A.3 of Appendix A, we can see that the absolute maximum error of six ADC ports reading is 10 and the ADC accuracy can be estimated in equation (4.55):

$$\frac{10}{4095} \times 100\% = 0.244\% \qquad (4.55)$$

Chapter 5

Software Design and Implementation

5.1 Introduction

A low-cost effective microcontroller controls two buck type converters and performs all control functions required by several different MPPT control strategies implementing batteries charging method as necessary. The single MC-based MPPT controller reduces the overall system complexity and cost (multiple PV arrays share a single chip). The proposed MPPT system is able to adapt to changeable environmental conditions, such as sun intensity and solar cell temperature.

5.2 Software Development Environment

The CodeWarrior™ Development Studio for Freescale™ 56800/E Digital Signal Controllers enables engineers to build and use 56800 or 56800E systems effectively and easily. The CodeWarrior Development Studio contains a menu item called Processor Expert (PE); the main job of this PE is to organize CPU and other hardware resources and to allow virtual prototyping and design across the entire 56800/E family. Embedded beans are components that are used in PE, they encapsulate functionality of basic elements of embedded systems. For instance, ADC bean implements encapsulation of CPU internal A/D converter peripheral functionality, it defines all settings for the ADC operation mode. The beans support several languages such as ASM, C, and ANSI. The Processor Expert plug-in generates code from the embedded beans. The CodeWarrior is responsible for managing the project files, the compilation, and debugging processes

[49][50]. The CodeWarrior environment supports everything we need to exploit the capabilities of the 56800 and 56800E architectures, so that we can develop embedded applications rapidly for a broad range of microcontrollers and microprocessor systems.

5.3 The Proposed MPPT Software Description and System Setup

The MPPT system flowchart is shown in Fig. 5.1. It initializes the MC56F8013 chip and all the data in the system, then waits for a while to make sure that ADC is stable enough to sample accurate input voltages and input currents from the PV array.

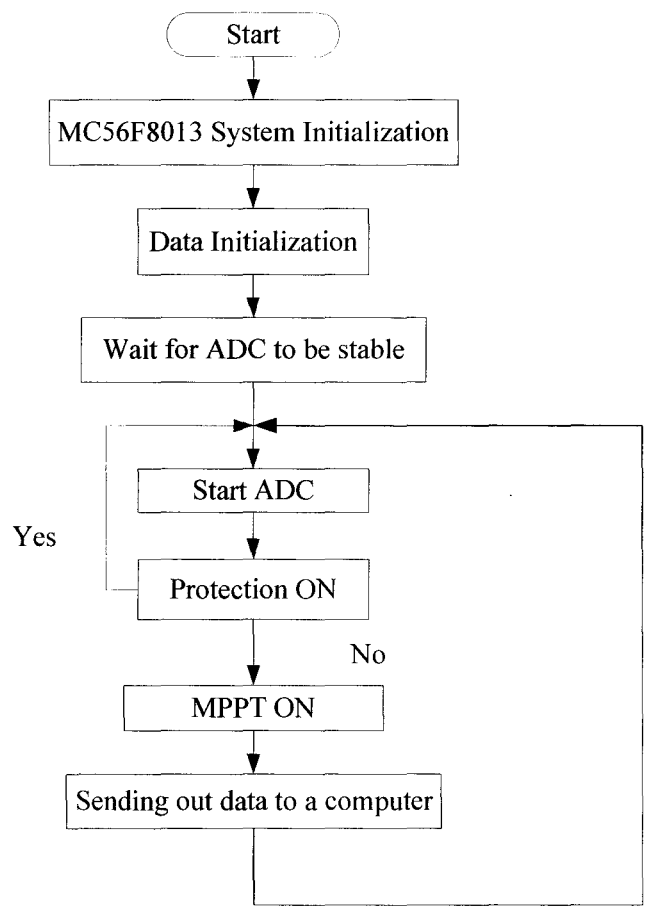


Fig. 5.1 The Overall MPPT System Flowchart

The system begins the ADC sampling, followed by a system protection check. If all the sampled data fall within the required margins, the proposed MPPT control is enabled. Otherwise, the MPPT will never start until the initial margins are satisfied. Finally the sampled data are sent to a computer and loops forever.

The project code was created with the processor expert stationary. The target board and processor were selected as MC56F8013VFAE. The main code was written in C, and mixed with ASM, and all of the code was compiled by the IDE.

5.3.1 The Basic Bean Setup in Metrowerks CodeWarrior

The basic setup for each bean in Metrowerks CodeWarrior is described in this section. There are four beans, which are PWM1, ADC1, TI1, and AM1, the detailed setup for each bean is presented in the following sections.

5.3.1.1 PWM1 Bean

Sets PWM prescaler as one. The counter module is initialized to 1920 using the PWM_3x_system_clock as the PWM clock rate. This results in the required 50 KHz PWM frequency. The clock runs in edge-aligned mode, and the dead time value is zero for this application. Since there are two MOSFETs in the MPPT circuit, two PWM channels are enabled as GPIOA0_PWM0 and GPIOA0_PWM1 respectively. Disable all the PWM interrupts, and enable all the initializations.

5.3.1.2 ADC1 Bean

The ADC initialization uses clock divisor of 32, which consequently gives a 0.5 MHz A/D frequency. Stop mode 1 is enabled, and the ADC mode is chosen to be "once

parallel". Parallel mode is set as "simultaneous". The channels configurations are all selected to be single-ended mode, and all the channel samples are enabled except sample3. Conversion complete (0) interrupt is enabled, its priority is medium, and its interrupt name is "ISR_ADC". Both "Call Init method" and "Enable peripheral clock" are selected, and the rest of ADC functionalities remain default. As a result, the converter A captures samples from 0 to 2, the converter B captures samples from 4 to 6, these samples are taken synchronously and scanning stops when either converter encounters a disabled sample or both converters complete all three samples.

5.3.1.3 TI1 (Timer) Bean

TMR0_Compare is set as timer, its interrupt priority is medium, and the interrupt prescaler is selected to be auto, and finally its interrupt period is set as 1ms, and the rest of setting is default. In the Events.c, the ADCs is enabled by the timer every 1ms.

5.3.1.4 AM1 (AsynchroMaster) Bean

This bean supports an asynchronous serial master-slave communication. The communication format contains 8 information bits and 1 control wake-up bit. Thus the number of information bit is default 9-bit. Stop bit is set to 2, and all the interrupts are disabled, SCI output mode is set as normal, and the baud rate is 57600 baud, which is chosen experimentally. All other settings remain default.

5.3.2 The Proposed MPPT Control Software Description

In the proposed MPPT system protection, all the input current overflow protections and battery charging status are checked. The controller has to continuously

detect the output voltage to prevent batteries from overcharging and discharging deeply. If the batteries are over-charged, the MPPT mode is stopped and changed to floating–charge mode.

For the maximum power point tracking (MPPT) control mechanism, the conventional Hill-Climbing approach and other algorithms as well as the proposed method are all separately implemented and compared in the indoor and outdoor experiments. As previously mentioned in chapter 3, the conventional Hill-Climbing technique always assumes that the previous power point is the maximum power point (MPP). The method compares the previous MPP with the current power point, and if the current power is larger than the previous one, updates the previous one with this larger one. Otherwise changes its current climbing direction. This control method results in oscillating around the real MPP, which causes a large system power loss.

In practice, due to unavoidable system noises and insufficiently accurate sensors and conditioning circuits or ADCs, the current and voltage measurements will not be precise. These inaccurate measurements will negatively affect the decisions made by the some control schemes.

The proposed MPPT control mechanism, adds an additional power window P_{window} to reduce the above problems. A power window sets a margin around the real MPP. This margin makes the controller track to a point, which is slightly smaller than the real MPP. We initially assume that the operating point is the maximum power point, and we use it as a reference called $P_{\max\_ref}$. If the next sampling point P(n) is smaller than $P_{\max\_ref} - P_{window}$, the searching direction will be reversed. If the next sampling point P(n)

is smaller than P_{max_ref}, the searching direction will be kept same. The reference P_{max_ref} will be updated only when the next sampling point P(n) is larger than P_{max_ref}. Particularly this is illustrated in Fig. 5.2, if the next sampling point is at P(n), the searching direction is changed, so that the operating point is brought back within the power window P_{window}. The searching direction is kept unchanged until the operating point is larger than the reference P_{max_ref}, such as the point at P(n)', then the reference P_{max_ref} is updated to the point P(n)'. The searching direction will remain the same in order to approach the MPP. With this power window P_{window}, the operating point is remaining closed to the MPP and has a tendency to settle on the right side of the hill. The additional benefit of a working point on the right side of the hill is that the slope on the right side is steeper than the slope on the left side. Thus the controller is less prone to noise on the data because the relatively larger increments in power output resulting from an increment in the current.

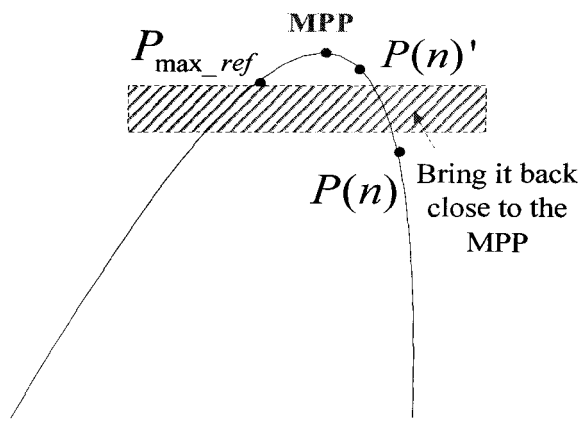


Fig. 5.2 Adaptive Hill-Climbing Algorithm

Consequently this power window can effectively reduce the power oscillations by sacrificing a very small portion of the source power. Note here that this conclusion will be proven in the later experiment in chapter 6. Without this margin, the MPPT controller will trace the MPP incorrectly (even though it ideally can operate correctly), and causes extra system power loss. The size of the power margin has to be decided based on the precision of the input power calculation, power oscillation, system noises and overall system power loss. If the value is chosen to be small, the duty cycle eventually results in considerably small oscillations when the input power is small, and it results in relative large oscillations when the input power is large. If the value is set to be big, the duty cycle gives relatively large oscillations if the input power is small, and it gives relative small oscillations if the input power is large.

In order to choose the value of the power margin and overcome the disadvantage of the conventional Hill-Climbing method, a simple modification (based on the conventional Hill-Climbing method) is introduced to the proposed MPPT control strategy. The modification is to make the power margin adaptive, namely *Adaptive Hill-Climbing*. This control flow diagram is shown in Fig. 5.3. If the input power is small, the power margin is not worth being adaptive; the power margin is chosen to be 0.2W constant which was found experimentally. If the input power is larger than a certain value, for instance above a level of 30W, then the power margin is chosen according to a small fraction of the calculated input power, for example $0.012 * P_{\max\_ref}$. The reason of choosing 30W as the power threshold is that this 30W is approximately 10% of the maximum power of 301.02W generated by the PV array. Below this power threshold, the

input power is very small, it is not necessary to make the power window adaptive. A constant small number of 0.2W will be fairly enough. The α = 0.012 is tuned experimentally.

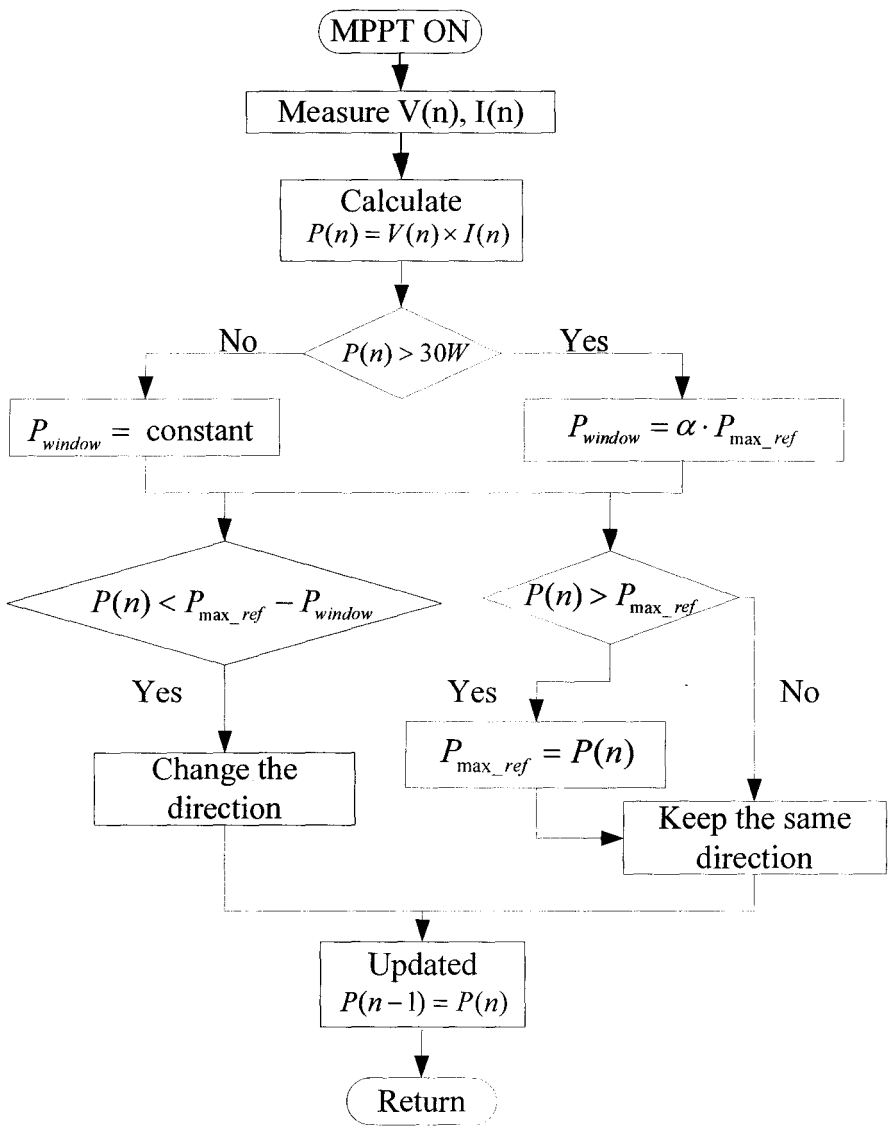


Fig. 5.3 Flowchart of Adaptive Hill-Climbing Method

The 0.001 was used as a starting value, and increased to 0.012 in small increments. The oscillations are observed to decrease as one increases α, and eventually remain stable.

The power window P_{window} is then large enough to deal with the system noise and the generated power oscillations are considerably reduced. By doing so, the automatically tuned power window can overcome the noise so that the correct direction can be decided upon by the controller and the duty cycle can be increased or decreased by a step of 0.05% based on the decision.

The input filtering capacitors have a notable influence on the system response time and the measurements of the PV array voltages and currents. The larger the capacitance we choose, the slower the response time we receive. If the input capacitors are too small, then the input voltage and inherent current ripples or noises generated by the switching operation of the power converter are high. The balance between the response time and the data accuracy can be addressed by adding a digital averaging filter in the control chip in order to clean the sensed PV array terminal voltage or current and give more precise data. The mathematical model of a digital averaging filter is shown in equation (5.1). Where $\bar{x}$ represents the averaged value, the term x_i represents the ith sampled value, and N is the sampling number.

$$\bar{x} = \frac{1}{N}\sum_{i=1}^{N} x_i \qquad (5.1)$$

In our case, the sampling number N was selected to be 16 in order to provide a better estimate of its true value. Because the timer was set to enable the ADCs every 1ms, thus the resulted ADC sampling rate was 16ms.

5.4 Serial Communication and Hyper-terminal Setup

In "AsynchroMaster" bean setting, the stop bit is set to 2 and baud rate is chosen to be 57600 baud. Other settings are default. The hyper terminal setting in a computer should be same as the setting of the "AsynchroMaster" bean, use COM1 or COM2 as the connection, and its port setting is shown in Table 5.1. Since the conflict between the default setting of 9 data bits in "AsynchroMaster" bean and 8 data bits in the computer, we have to manually force the 9-bit to be 8-bit in the serial communication interface SCI.

Bits per Second	57600 baud
Data bits	8
Parity	None
Stop bits	1
Flow control	None

Table 5.1 Port Setting

Hence, the sampled data can be received and saved in a computer for the later experimental investigations.

Chapter 6

System Setup and Experiment Results

6.1 PV Emulation System Introduction

An experimental prototype MPPT is constructed. Before testing this MPPT in a real weather environment, a sequence of emulations is under taken.

We can use a DC power supply with a variable resistor connected in series, as the solar array emulator [51]. Fig. 6.1 illustrates the construction of closed-loop experiment without real PV modules. This indoor experiment has the advantage of allowing the comparison of system performance for various MPPT control methods under the same or very similar operating conditions. Unfortunately it can not verify the control algorithms that use the non-linear I-V relationship, like the real solar array does. The control mechanism, such as the incremental conductance control method introduced in section 3.3.3 of chapter 3, can not be tested using such a PV emulation system.

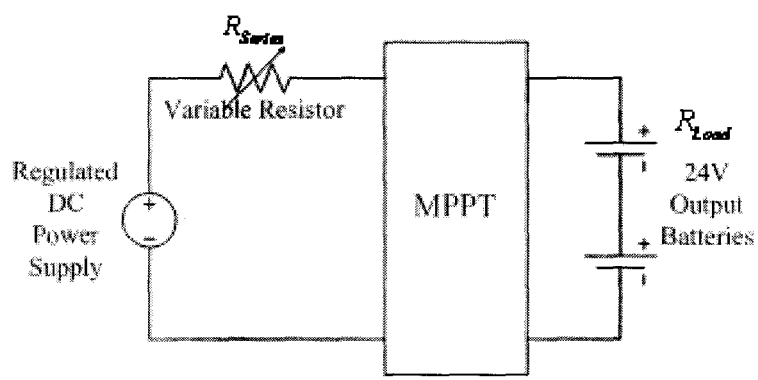


Fig. 6.1 Closed-loop Experiment Construction without Real PV Modules

The two buck converters are positioned between the DC source and the load as seen in Fig. 6.2. According to the maximum power theorem, in order to obtain the maximum power from a source with a fixed internal resistance R_{Series}, if the system is designed to operate at or near the MPP, then the impedance seen from the input side of the buck converters (includes the batteries) needs to match the internal impedance of the source by automatically adjusting converter's duty cycle [51]. In this case, the power dissipated approaches the maximum is when the voltage drop across the R_{series} is half of the applied input DC source voltage.

6.2 Indoor Experiment by Using PV Emulation System

A laboratory setup of the PV emulator power system with the proposed MPPT controller is implemented and tested. The outcomes of the tests are discussed; the benefits and disadvantages of the proposed MPPT control method and other MPPT control approaches are addressed.

In the actual experiment, a GEN600-2.6 is used as the DC regulated voltage supply. A maximum 42Ω variable resistor is used as the series resistor R_{Series} with a 3.5A maximum rated current, and the load is two 12V batteries connected in series. The indoor experimental setup is illustrated in Fig. 6.2.

Two experimental cases are studied. One emulates a sudden increase (or decrease) in the sun intensity. The other one is to emulate a rapid increase (or decrease) in PV module temperature. These tests allow us to investigate whether the MPPT with different control methods can respond quickly to the different emulated weather conditions.

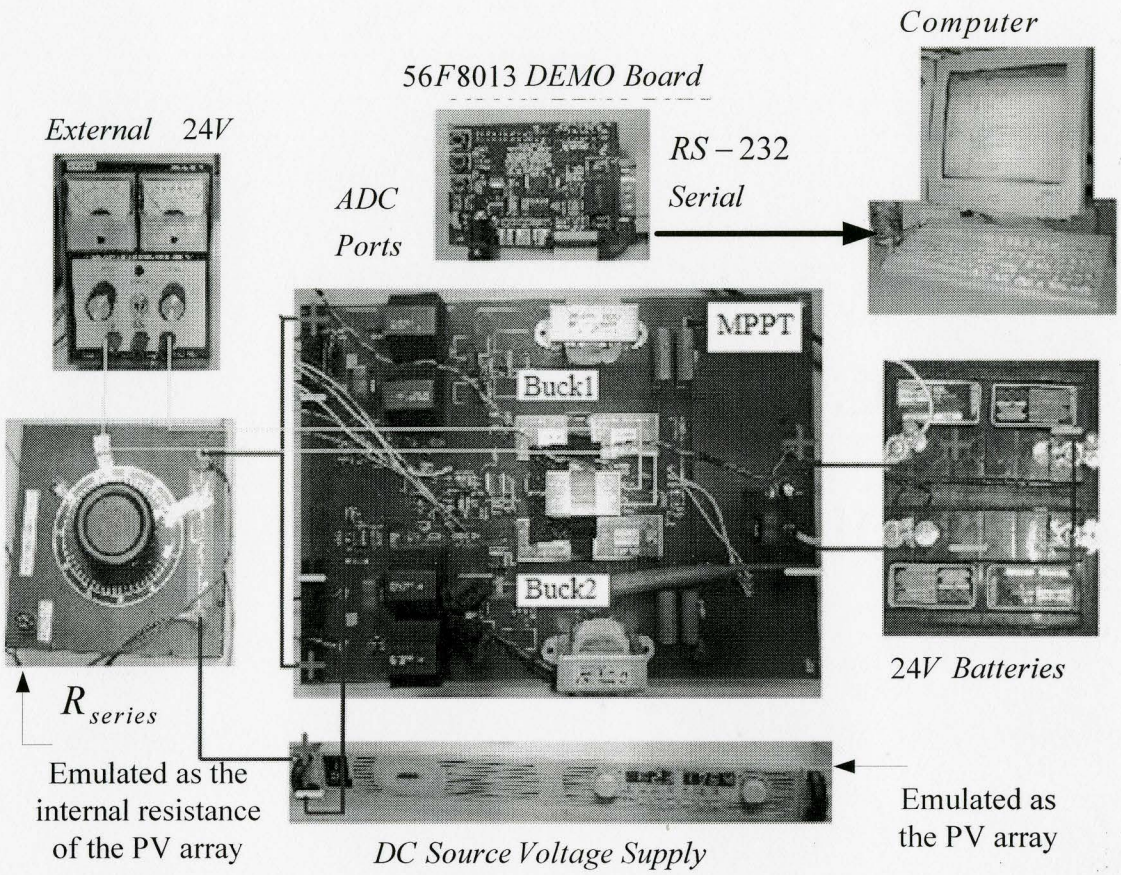


Fig. 6.2 Indoor Experiment Setup

6.2.1. Case One: Indoor Experiment Emulated as Solar Cell Temperature Varies

In a PV system, as cell or module temperature varies the open circuit voltage, V_{OC} of PV array alters abruptly. This situation can be represented by using a varying DC voltage supply and a fixed series resistance R_{Series}. The procedure of the experiment is to increase the DC voltage source from 60V to 104V at several different voltage levels (60V, 74V, 84V, 94V, and 104V).

The conventional Hill-Climbing control method is used to seek the varying maximum power point as the input DC voltage source increases from 60V to 104V. The corresponding input power for each converter, total input power and its duty cycle versus time are shown in Fig. 6.3. One input power (P1) expanded time scale from the power range of 9.5W-10.3W is displayed in Fig. 6.4.

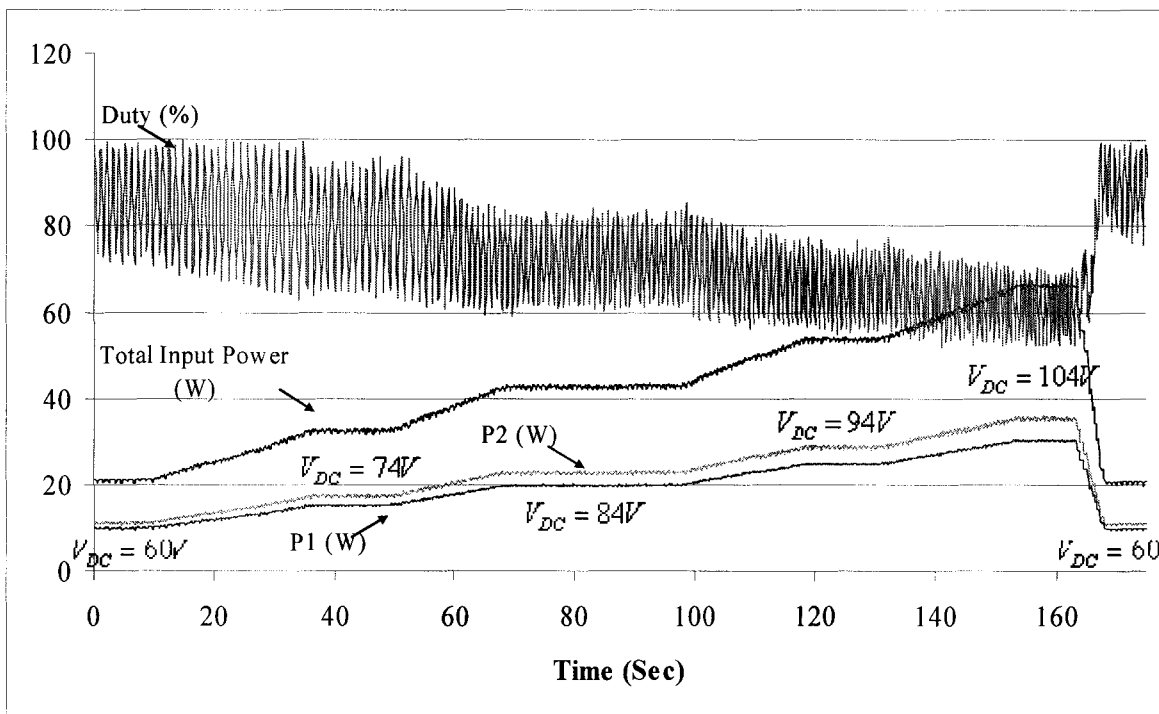


Fig. 6.3 Power1, Power2, Total Input Power and Duty by Hill-Climbing

The figure reveals that the conventional Hill-Climbing control method gives relatively big oscillations within the entire 35W power range for each converter. This is because the power margin is set to be relatively large compared to 35W. The oscillations become relatively smaller as the input power gradually increases. This considerably large power margin results in smaller oscillation as the input power becomes noticeably high.

However, as the input power becomes very large, this power margin compared to the continuously increasing input power is then relatively small. This will again lead to an undesired big power oscillation.

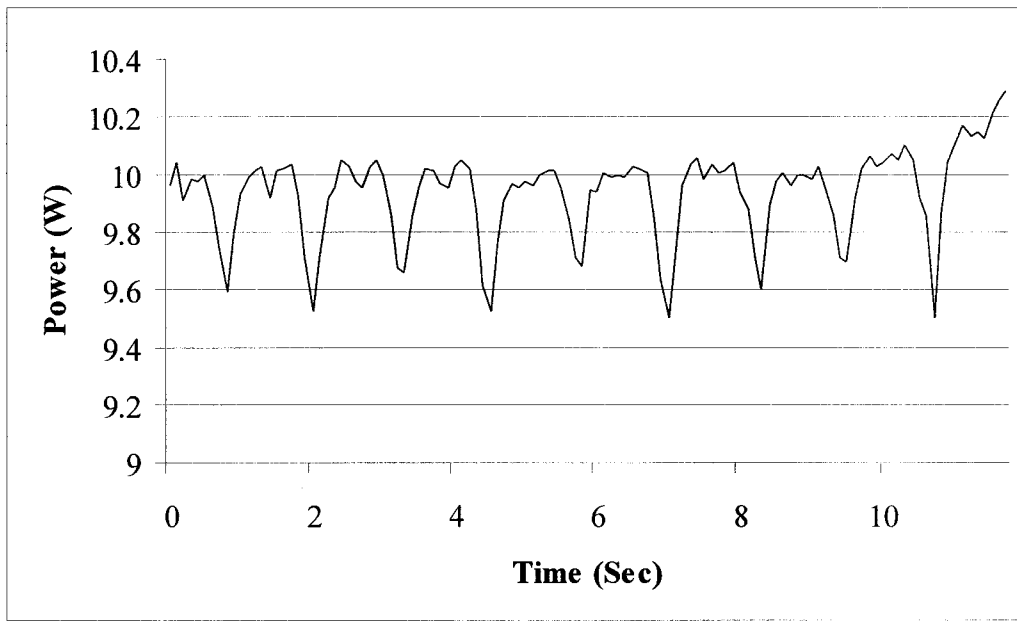


Fig. 6.4 Power1 Expanded Time Scale from Power Range of 9.5W-10.3W

The proposed algorithm *Adaptive Hill-Climbing* is tested using the same equipment, the experimental results are illustrated in Fig. 6.5 and Fig. 6.6 respectively. These figures show that the power fluctuation produced by using the proposed control technique are substantially reduced throughout the test run compared to the conventional Hill-Climbing results shown in Fig. 6.3 and Fig. 6.4.

Plots for total input power, output power and power conversion efficiency using the conventional Hill-Climbing and the proposed Adaptive Hill-Climbing are also illustrated in Fig. 6.7 and Fig. 6.8 respectively.

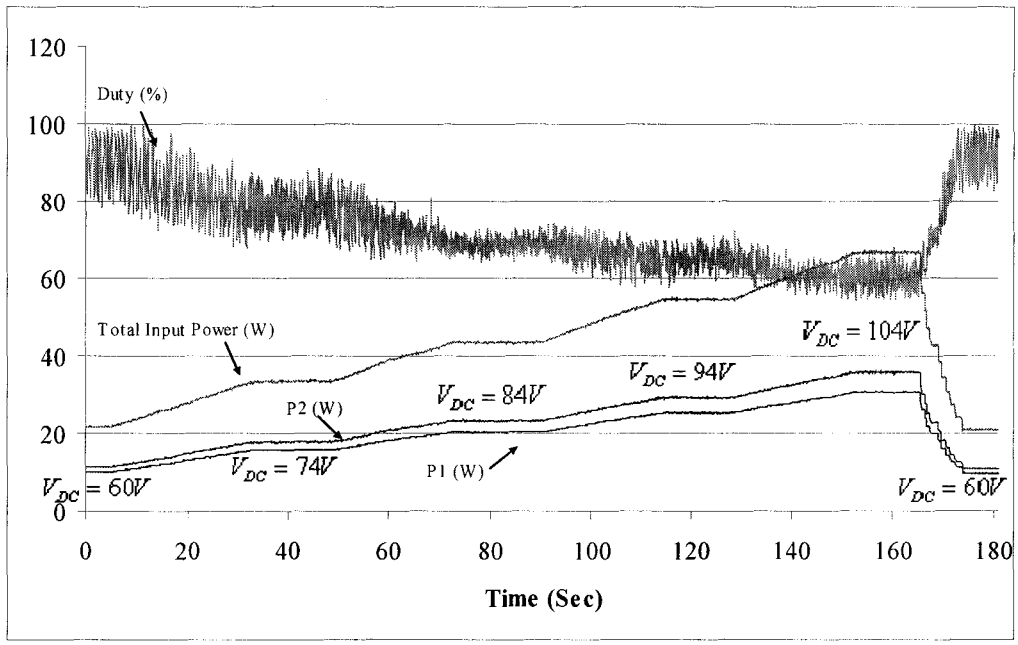


Fig. 6.5 Power and Duty by Adaptive Hill-Climbing

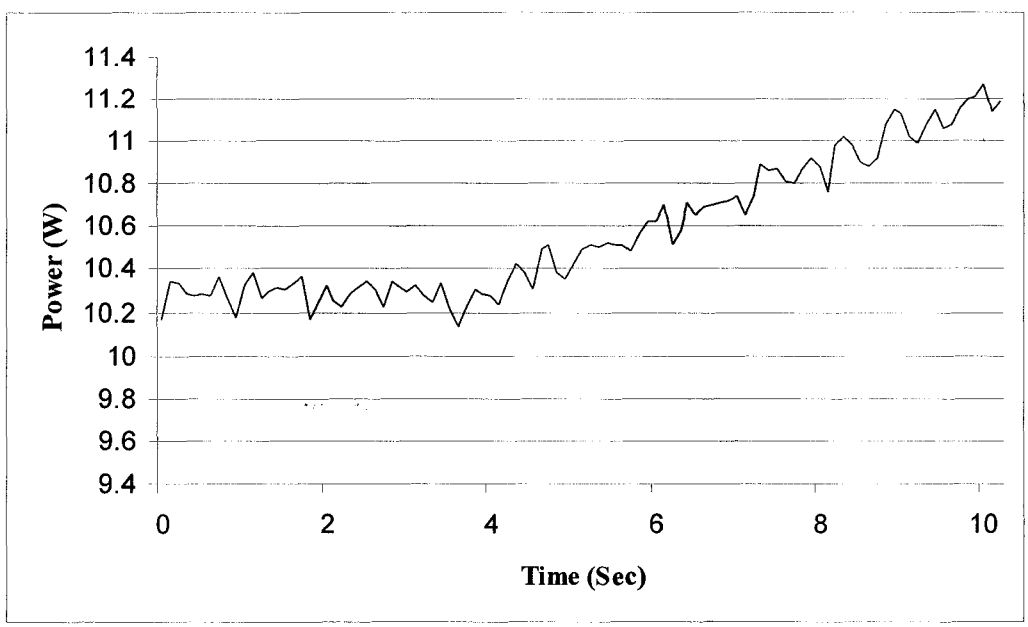


Fig. 6.6 Power1 Expanded Time Scale from Power Range of 10.19W-11.3W

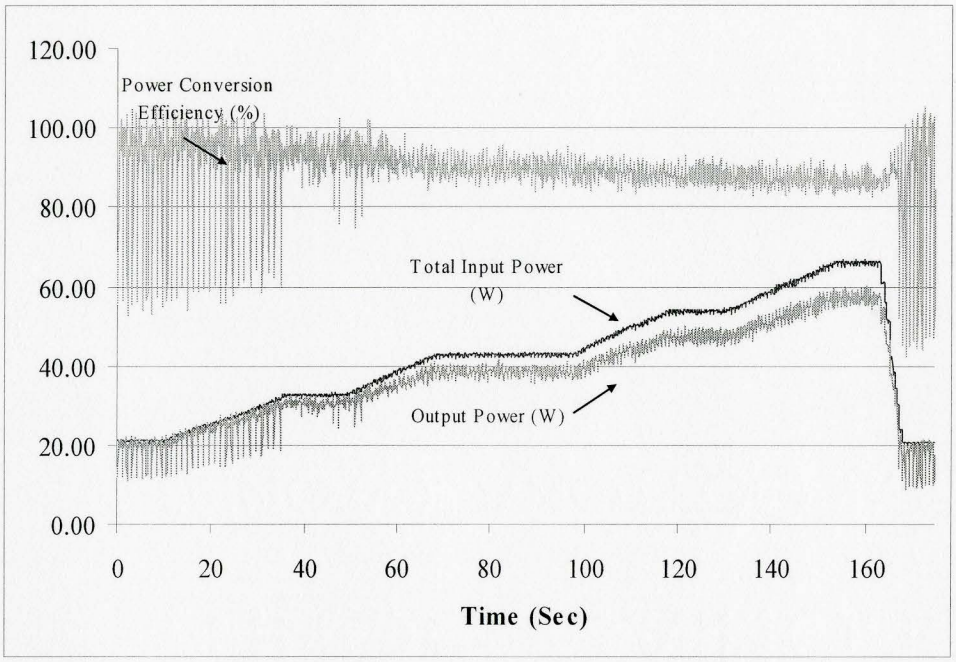


Fig. 6.7 The Total Input Power versus The Output Power, and its corresponding Power Conversion Efficiency by Conventional Hill-Climbing as the Input DC Source Voltage Varies

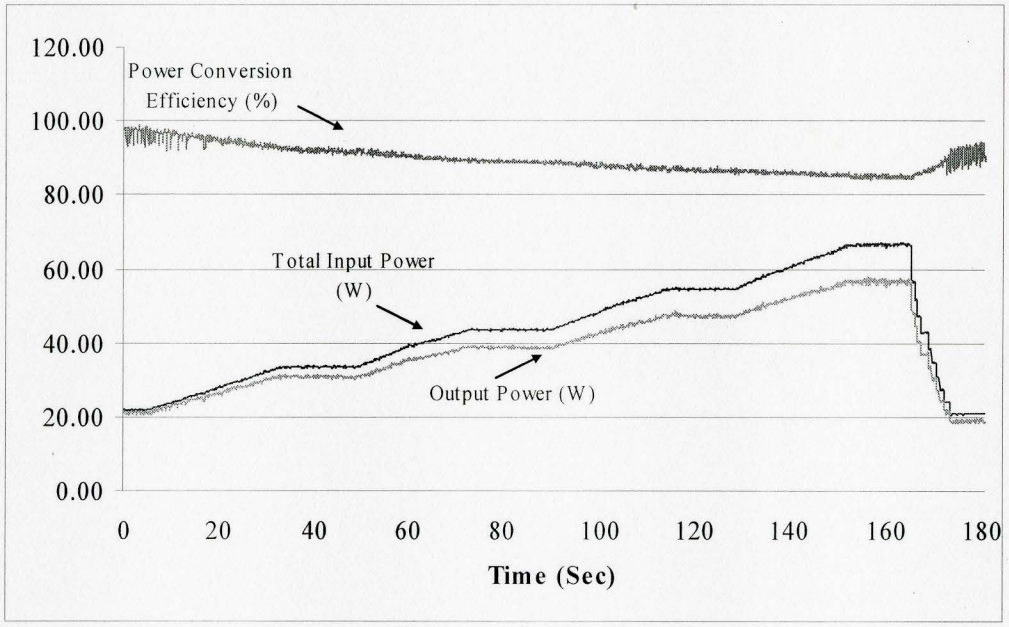


Fig. 6.8 The Total Input Power versus The Output Power, and its corresponding Power Conversion Efficiency by Adaptive Hill-Climbing as the Input DC Source Voltage Varies

The power efficiency of the Adaptive Hill-Climbing (89.58%) is slightly higher than the efficiency of the conventional Hill-Climbing method (89.18%). From a power oscillation point of view, the MPPT by using Adaptive Hill-Climbing control technique performs better than the conventional method.

In particular, for the Adaptive Hill-Climbing control method, its dynamic performance is shown in Fig. 6.9 and Fig. 6.10.

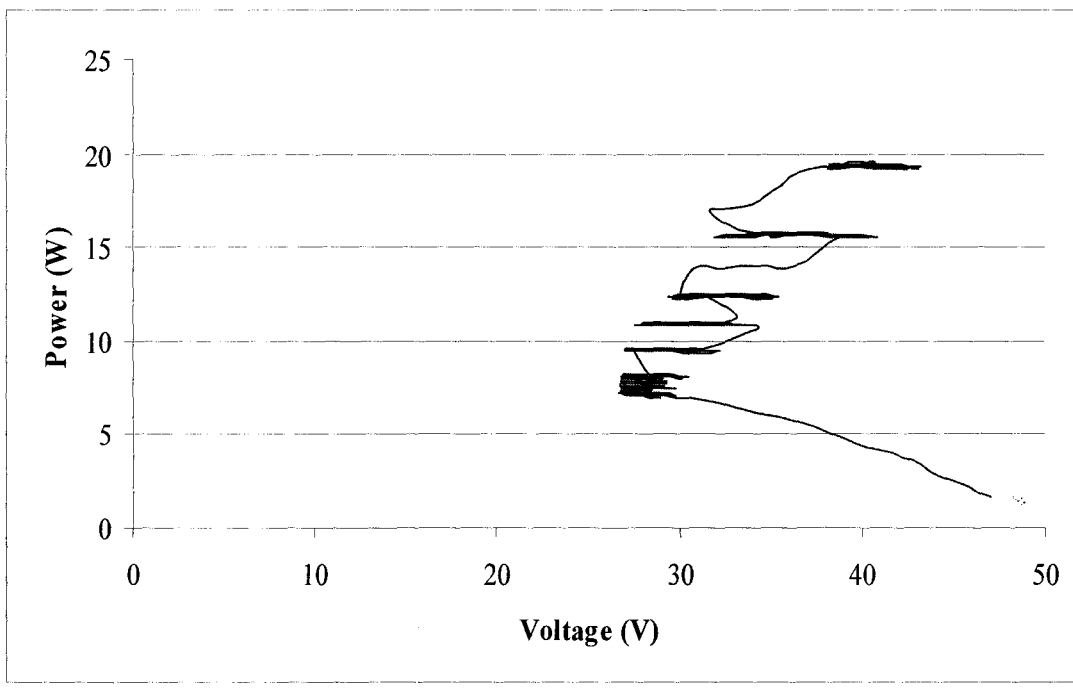


Fig. 6.9 Trajectory of Input Power versus Input voltage by Adaptive Hill-Climbing at the beginning of tracking

From these two figures, they both show that The MPPT starts tracking at the open circuit voltage (this indicates that the MPPT begins on the low impedance side of P-V curve of the PV array if real PV modules were used in the later outdoor experiment).

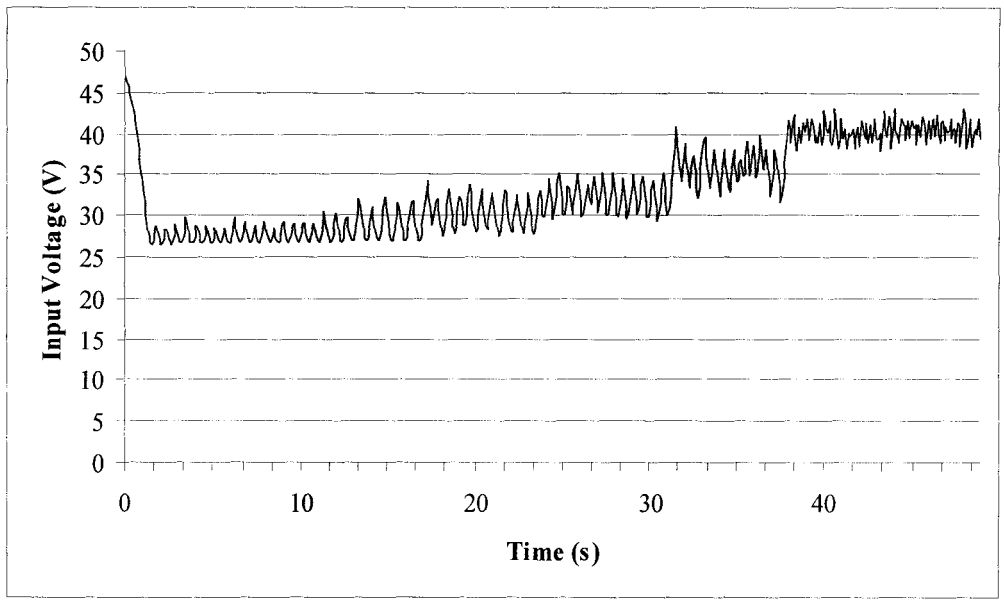


Fig. 6.10 Dynamic Response of the Input Voltage by Adaptive Hill-Climbing at the beginning of tracking

The MPPT controller keeps capturing to the corresponding MPP. Once the operating point reaches to the MPP then it oscillates around them or keeps searching the new MPP as the input power increases or decrease (as displayed in Fig. 6.9 and Fig. 6.10).

Using the dp/dv method and repeating the same experiment, the individual input power and duty cycle versus time, total input output powers and its power conversion efficiency are depicted in Fig. 6.11 and Fig. 6.12 respectively.

Ideally the dp/dv method should not result in oscillations around the MPP, it should make the operation stable at the steady-state. In contrast the experimental results, illustrated in Fig. 6.11, the method still causes oscillations as the source voltage changes at different voltage level. The reasons behind the oscillations are the system noise and the accuracy of sensors and ADCs.

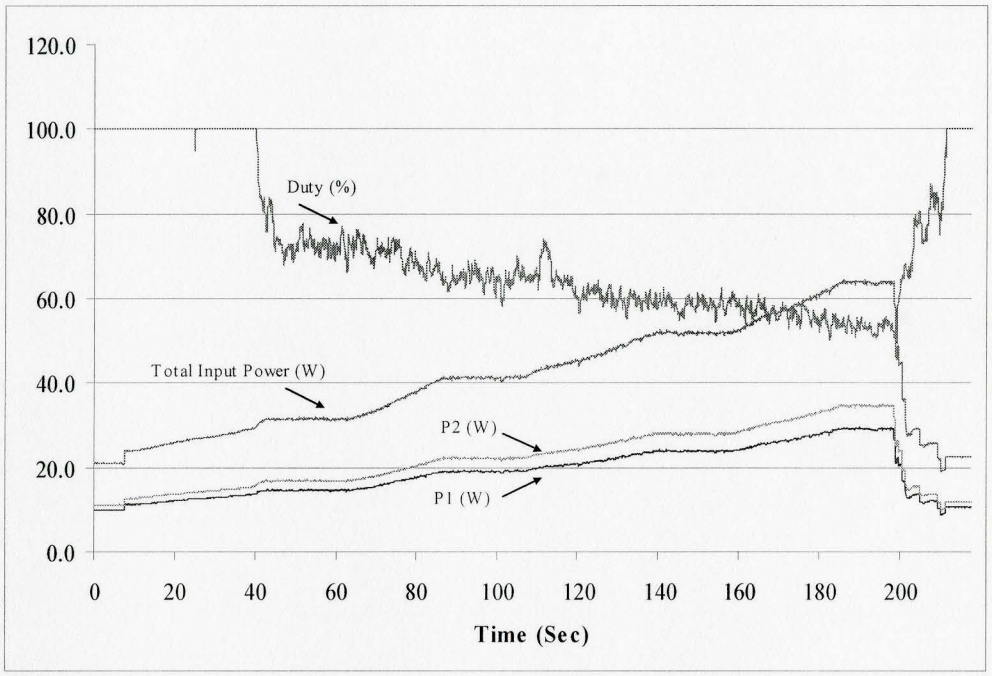


Fig. 6.11 Individual Input Power and Duty by dp/dv Method

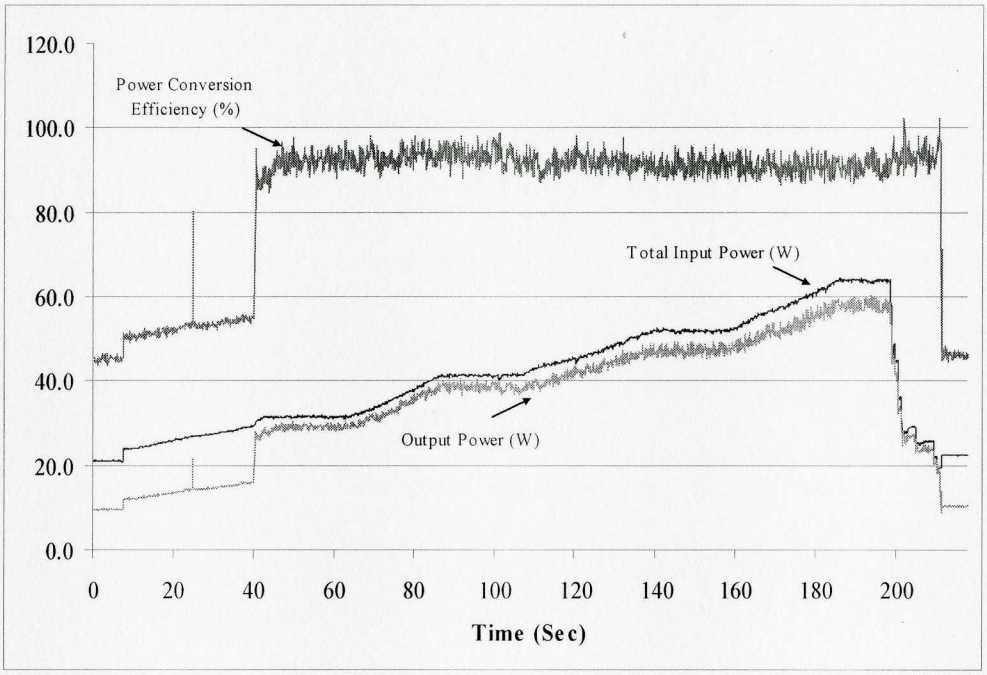


Fig. 6.12 The Total Input Power versus The Output Power and its corresponding Power Conversion Efficiency by dp/dv Method as the Input DC Source Voltage Varies

Despite these unavoidable factors, the dp/dv control method does give fewer power fluctuations at the steady-state than the conventional Hill-Climbing and the proposed methods. By observing Fig. 6.11 and Fig. 6.12, we can see that when the DC voltage source is below 70V, the input power is very small. This means that the slope of the P-V curve is not steep. So when the derivative signal is not large enough compared to the existing noise, the signal to noise ratio drops drastically, hence erroneous samples fool the MPPT controller and consequently the controller makes wrong decisions. This makes the duty cycle unity, which causes the input to connect to the output directly.

In summary, the adaptive power window in the proposed method can reduce the power oscillations comparing to the conventional Hill-Climbing method. When the input power is small, the dp/dv method has difficulty in correctly detecting the sign of the dp/dv slope due to system noise. Thereby the dp/dv method gives much lower power efficiency than the proposed method as the input power becomes relatively low. The proposed method is more effective at low illumination (low input solar power) than the dp/dv method, for the dp/dv method comparatively requires a high degree of accuracy to calculate the slope (dp/dv).

6.2.2 Case Two: Indoor Experiment Emulated as Sun Illumination Varies

While the sun illumination varies, the short circuit current I_{SC} of the PV array can change suddenly. We can use a fixed DC voltage supply and varying series resistance R_{Series} to represent the situation. The test procedure is that R_{series} is changed from 41Ω to 33Ω, and back to 41Ω, then decreased to 30Ω, and back to 41Ω again. Using the Hill-

Climbing method, the testing result is shown in Fig. 6.13. We can observe that the input power increases as the input current increases, and vice versa. The oscillation of the duty cycle is between 69% and 98%, which is large.

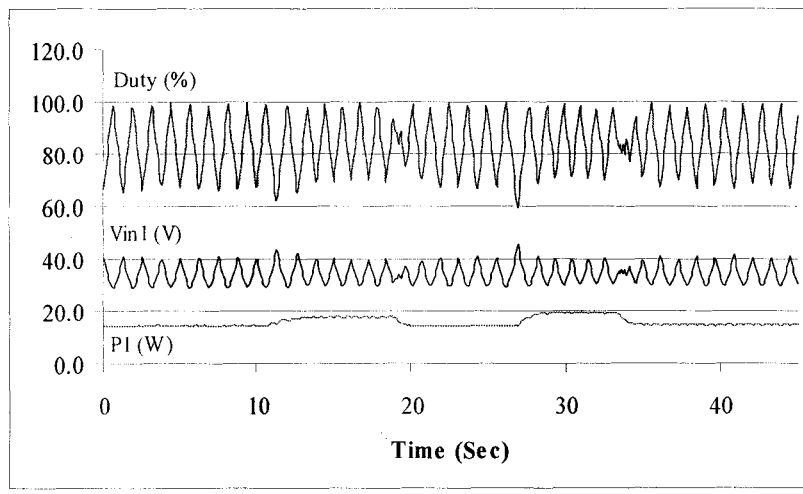


Fig. 6.13 Input Power, Voltage, and the Duty Cycle by Hill-Climbing method as the series resistor varies

The same experimental procedure is carried out with the proposed method, particularly changed R_{series} from 41Ω to 32.5Ω, and back to 41Ω instantly, then decreased to 29.2Ω, and then again back to 41Ω. The corresponding test result is shown in Fig. 6.14 through Fig. 6.17. From Fig. 6.14, as the R_{series} decreases from 41Ω to 29.2Ω and then increases back to 41Ω, we can see that the duty cycle of the converter increases slightly, but the input voltage still remains the same as before. From Fig. 6.15, we know that as the R_{series} decreases the input current to the converter increases correspondingly. From both diagrams we can conclude that as input current increases, the duty cycle of the converter increases as well. Overall the results reveal that the MPPT still can seek

continuously varying MPP as the input current varies instantly as illustrated in Fig. 6.14 and Fig. 6.16, the efficiency in this case is around 90.15% as depicted in Fig. 6.17.

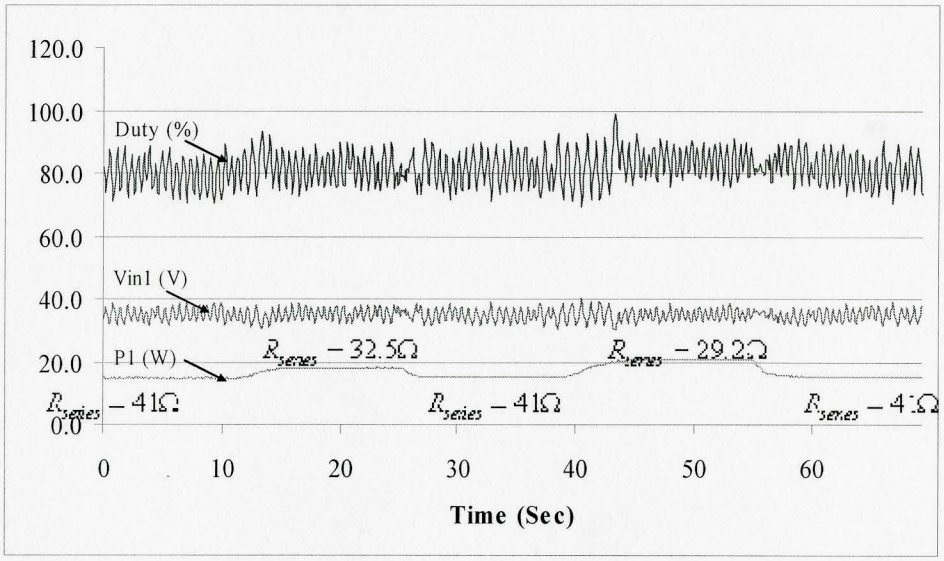


Fig. 6.14 Power1, Voltage1, and Duty Cycle by Adaptive Hill-Climbing as the series resistor varies gradually

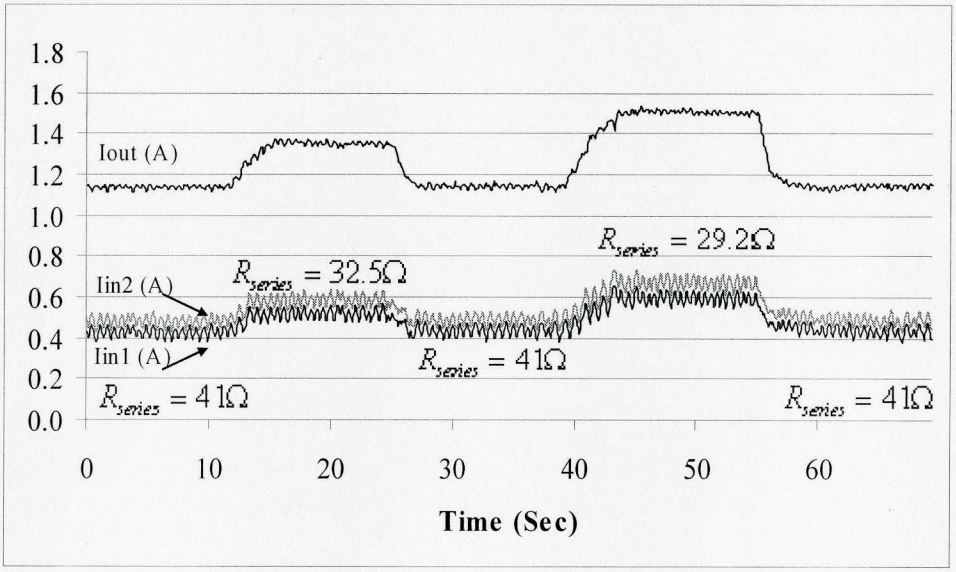


Fig. 6.15 The Input Current1, Input Current2, and its Total Current by Adaptive Hill-Climbing as the series resistor varies gradually

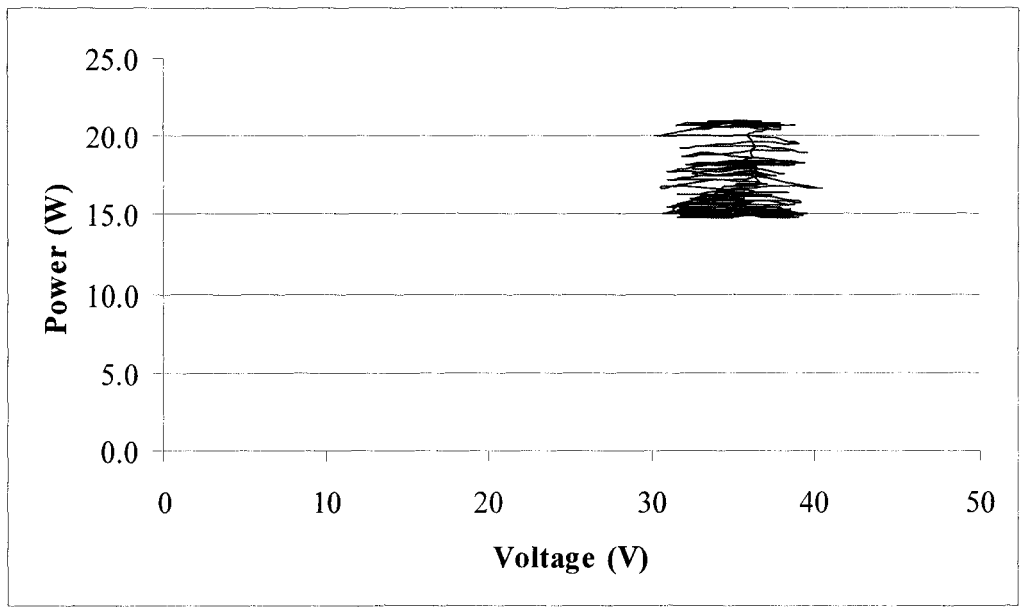


Fig. 6.16 Input Power versus Input Voltage by Adaptive Hill-Climbing as the series resistor varies gradually

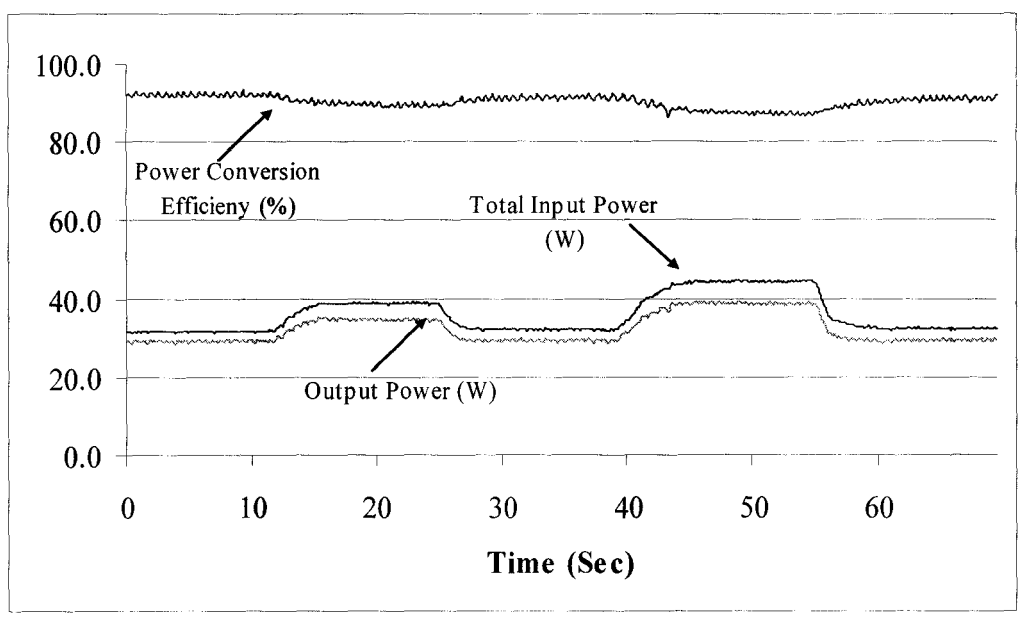


Fig. 6.17 The Total Input Power versus The Output Power, and its corresponding Power Conversion Efficiency by Adaptive Hill-Climbing as the series resistor varies gradually

A similar experiment is performed, using only one buck converter this time, and varying R_{series} rapidly by a large amount. The purpose of this test is to emulate an extreme case when the sun illumination level alters drastically. The DC input voltage source is still at 72V, and the test procedure is that R_{series} is varied from 40Ω to 28Ω, and back to 40Ω instantly, then decreased to 26.5Ω, and then again back to 40Ω immediately. Fig. 6.18 displays the input power and input voltage verve time.

The input current started around 0.9A, increased to 1.29A (ΔI = 0.39A), and reduced back to 0.9A (ΔI = -0.39A), then increased to 1.36A (ΔI = 0.46A), finally back to 0.9A (ΔI = -0.46A). This test represents a severe climate condition that the PV array is partially shaded by clouds or the partial shaded PV array exposed to the sun suddenly, which leads the input current from the PV array to increase or decrease dramatically.

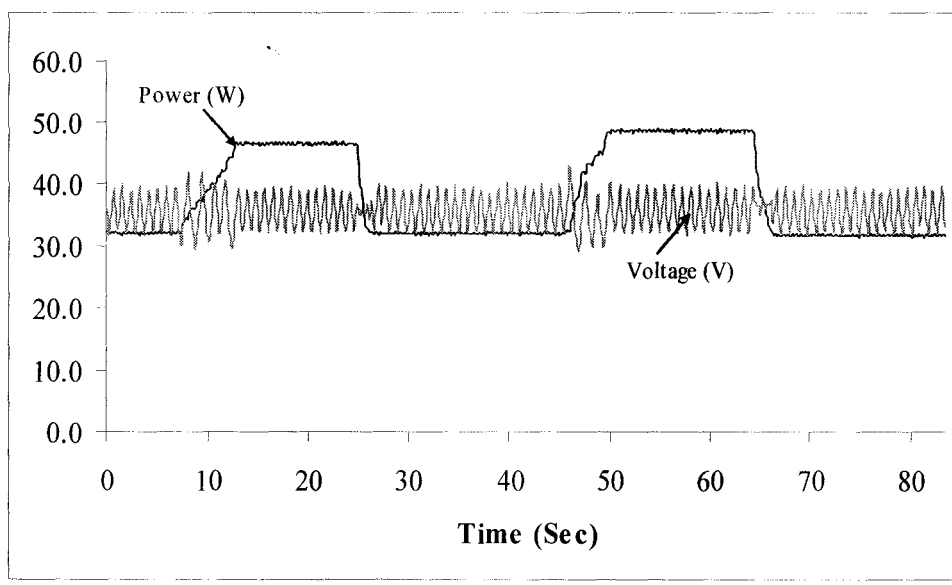


Fig. 6.18 Input Power and Voltage by Adaptive Hill-Climbing as the series resistor varies dramatically

Using the dp/dv method, the test results are shown in Fig. 6.19 and Fig. 6.20 as R_{series} is changed from 41Ω to 30Ω, and back to 41Ω, then decreased to 28Ω, and back to 41Ω again.

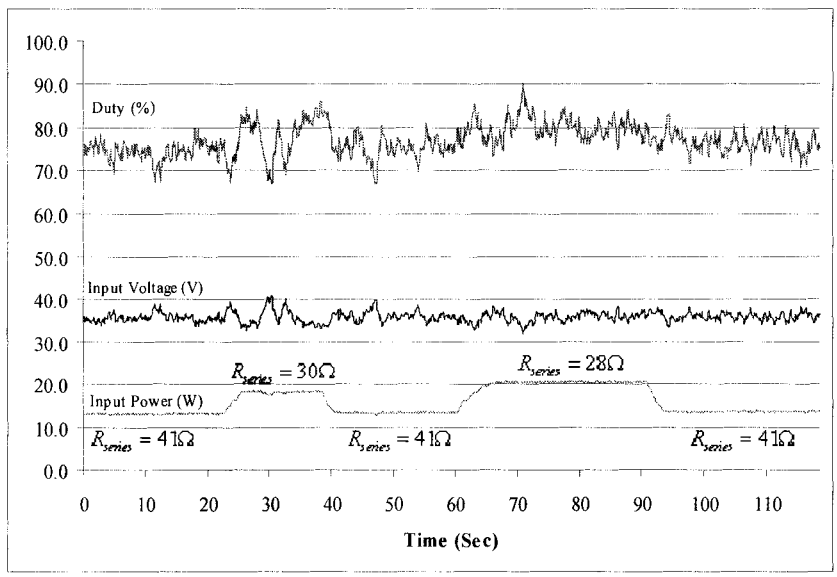


Fig. 6.19 Input Power and Voltage by dp/dv method as the series resistor varies

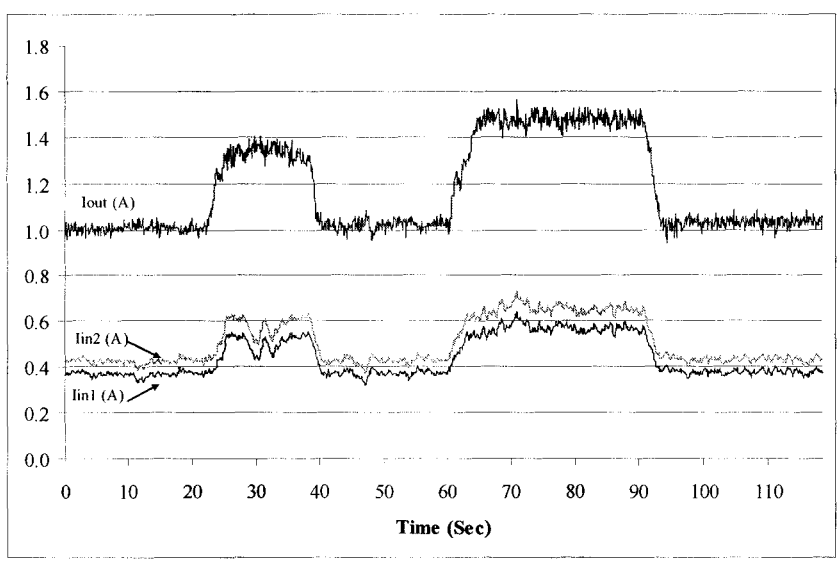


Fig. 6.20 Total Input Power versus The Output Power, and its corresponding Power Conversion Efficiency by dp/dv method as the series resistor varies

As expected, the dp/dv method can quickly lock on to the MPP as the input current changes.

6.2.3 How Much the Input Power can be increased By Using the designed MPPT Controller

The purpose of this chapter is to show and confirm that using the MPPT extracts higher power than the conventional direct coupled method. For instance, when the input DC power is constant at 80V, the corresponding total input powers, and its power conversion efficiencies without and with the MPPT, are graphically shown in Fig. 6.21 respectively.

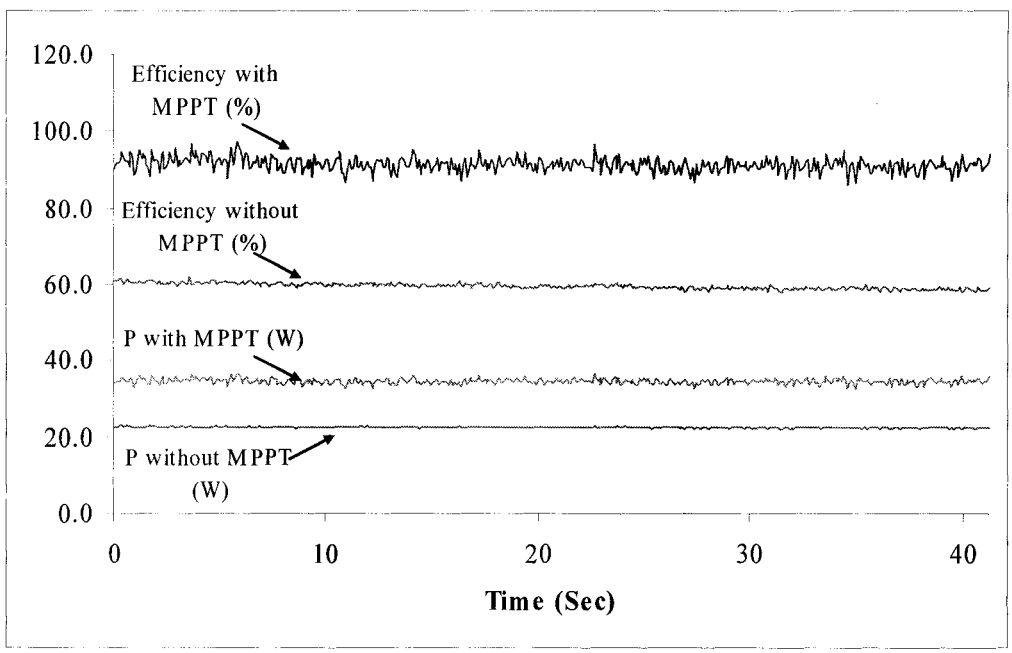


Fig. 6.21 Output Power and Power Efficiency without and with MPPT

By directly connecting the input source to the output batteries, the average power efficiency is 59.58% based on the direct-coupled experiment. Whereas by adding the

connection of the proposed MPPT as the interface between the input source and the output batteries, using the MPPT can boost up the average efficiency up to 91.5%.

As a result, using the proposed MPPT definitely can give benefits in terms of power, especially at a larger power range. For the outdoor experiments, the parameters may need to be tuned further in order to make MPPT perform better in a real environment.

6.2.4 Indoor Experiment Conclusion

In the PV emulated system, two parallel-coupled buck converters are interfaced between a DC voltage source and 24V batteries. A microcontroller-based unit has been chosen as the control unit, and the principle of energy conservation has been employed into the entire system. The basic purpose of the PV emulated system is to simplify investigations of various MPPT control methods. In contrast to the conventional Hill-Climbing method, the proposed control algorithm introduces an adaptive power window, which uses the input power as the key control variable. And with further consideration between tuning parameters and sampling time, experimental results reveal that a mitigation of power fluctuation in steady-state can be acquired by the proposed control method. On the other hand, the dp/dv method is capable to offer relatively small power fluctuation than the proposed method, but its efficiency is very poor when the input power is small.

Ultimately with the proposed method employed in the MPPT, high efficiency can be achieved up to 90%. Without the MPPT, efficiency is only around 56%. A better performance for the proposed MPPT system under rapid variations conditions can be

obtained by higher execution speed. The proposed control strategy outperforms the conventional Hill-Climbing approach, and offers better efficiency than the dp/dv method when the input power is small. The indoor experimental results have been proven and ensured that the proposed MPPT can be utilized at later experiments under realistic weather conditions. There is enough evidence to show that the proposed MPPT method is better than the conventional Hill-Climbing method in the indoor experiment. Hence only MPPT control methods, including the Adaptive Hill-Climbing, dp/dv, and IncCond will be tested in the outdoor experiment.

6.3 Outdoor Experiment

The outdoor experiment is essential to be performed and studied in order to understand the practical validity of the whole PV system. In accordance with the previous system configuration, as shown in Fig. 6.2, the complete solar power system with a different implementation of MPPT control solutions was developed and built. The final experimental constructions are as illustrated in Fig. 6.22 and Fig. 6.23.

The solar source consists of six identical PV modules, with their specification is presented in Table 6.1. Each module has built-in by-pass diodes to reduce any voltage or power drop caused by shadows. Given the standard condition of 100% sun illumination and 25°C temperature, three individual PV modules are connected in series to give a total 66V open circuit voltage and to form one PV array. In our case (generally) choosing considerably high voltage as the PV terminal voltage can effectively minimize the power loss caused by the cable or wirings, since the less current goes through the cable the lower power losses caused by the resistance in the wires.

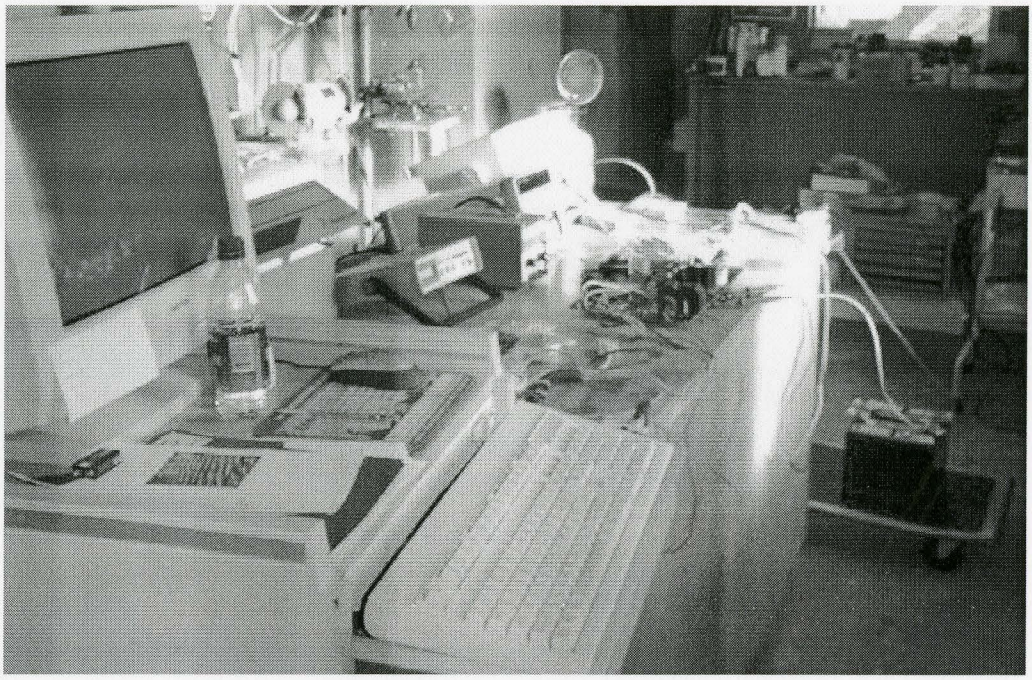


Fig. 6.22 Actual Experiment Setup

Fig. 6.23 Actual PV Array Setup

Finally each PV array is coupled by one DC-DC buck converter, and the outputs of the two converters are connected in parallel to feed the output 24V batteries.

GEPV-050 module	
I_{SC}	3.3A
V_{OC}	22V
I_{mpp}	2.9A
V_{mpp}	17.3V

Table 6.1 Specification of PV Module

6.3.1 PV System

In the experimental setup, two PV arrays are completely exposed to a real environment. The system demonstrates a variety of behaviors under different weather conditions. The designed MPPT controller system is tested under three different types of weather conditions: sunny days, cloudy days, and cloudy with sunny breaks days. The experimental data such as input (or output) voltage and current are continuously monitored, average power is calculated. These data are gathered through a RS-232 serial for communications with a PC's serial port, and saved on a personal computer in order to verify and validate the proposed method and other MPPT control schemes in a natural environment.

6.3.2 Outdoor Experiment Results

Case one: Nov. 25th 2007, a sunny day. The testing period was from 10:00am to 2:00pm. The sunlight illumination was varying slowly, and the ambient temperature range was from 3°C to 5.1 °C. The measured open circuit voltage of one PV array was 66V, and the other one was 66.1V. The open circuit voltage of a PV array or corresponding operating voltage at the MPP (V_{mpp}) is mainly dependent on the array temperature. Otherwise it is barely changing if the temperature is not varying dramatically. The short circuit current of one PV array was 1.5A, and the other one was also 1.5A at 10:30am. Both of these will eventually increase as the sun radiation increases because the short circuit current of the PV array is proportional to the irradiance. The actual experimental outcomes were separately recorded with several implementations of different MPPT control strategies, and the corresponding data are plotted, and discussed.

The proposed MPPT method is examined. The testing period was from 11:30am to 12:00am, since the two input powers generated by each PV array were approximately same, thus only one the input power and the total input power are shown in Fig. 6.24. The calculated average total power from the actual data is 173.6W. From Fig. 6.24, we can observe that the input power generated from PV array increases gradually as the sun illumination increases. The input power to one converter increases from 83W to 89W over time. Its expanded time scale used in Fig. 6.25 shows the magnitude of the input power fluctuation is around 1.3W, comparing to 86.8W, it is only 0.15% of the total power.

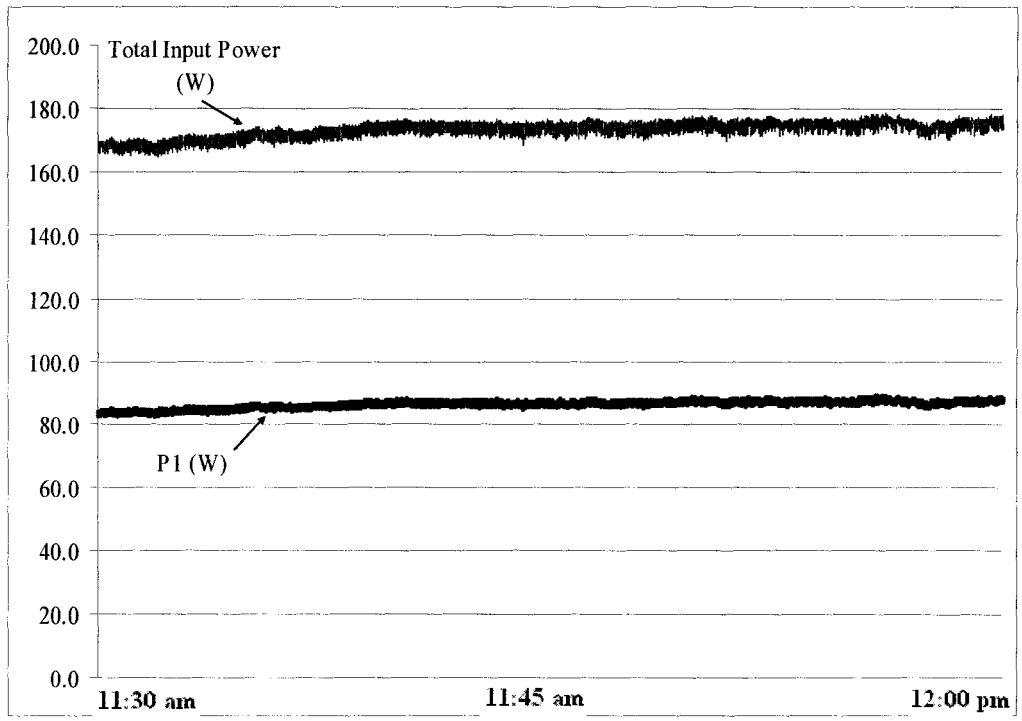


Fig. 6.24 Input Power1 and Total Input Power by the Proposed Method

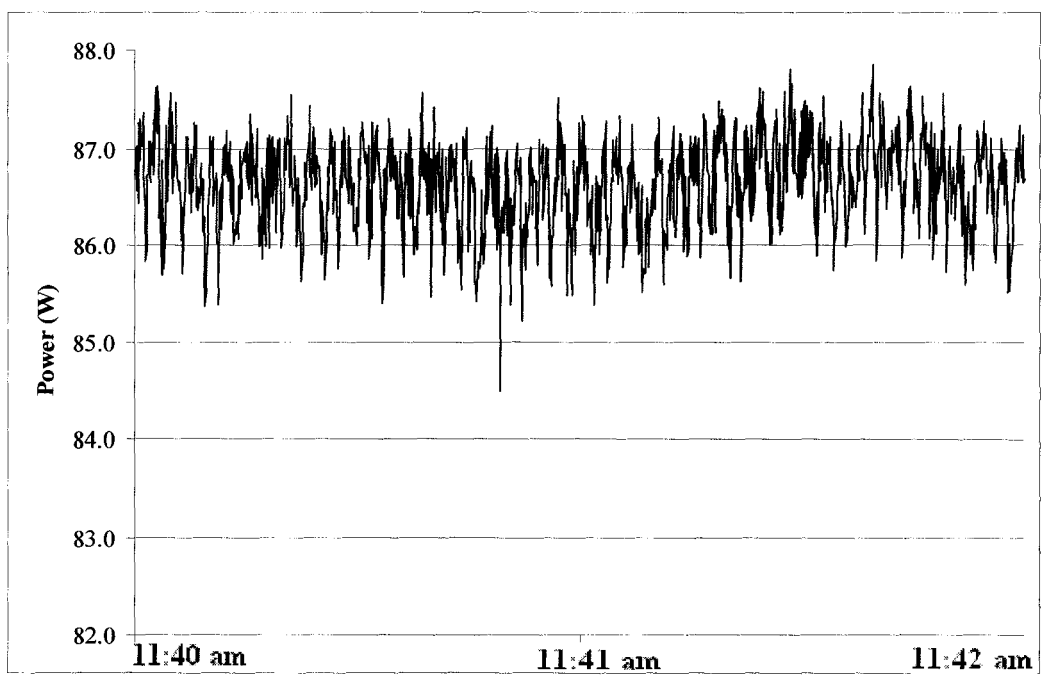


Fig. 6.25 Expanded Time Scale of Input Power1

From 12:30pm to 1:00pm, the dp/dv method is used by the MPPT system, and the experimental result is presented in Fig. 6.26 and Fig. 6.27.

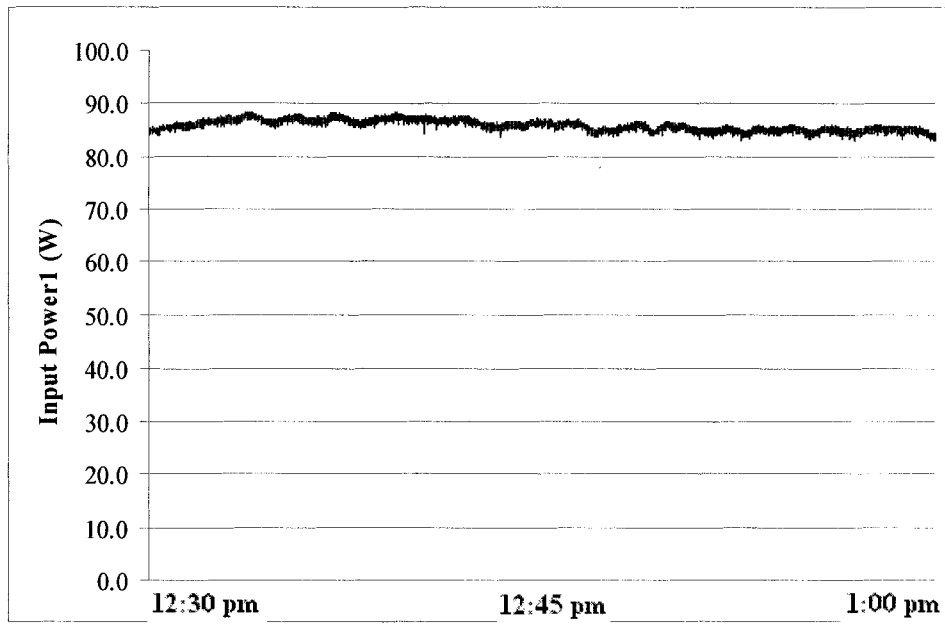


Fig. 6.26 The Input Power1 to One Converter by the dp/dv Method

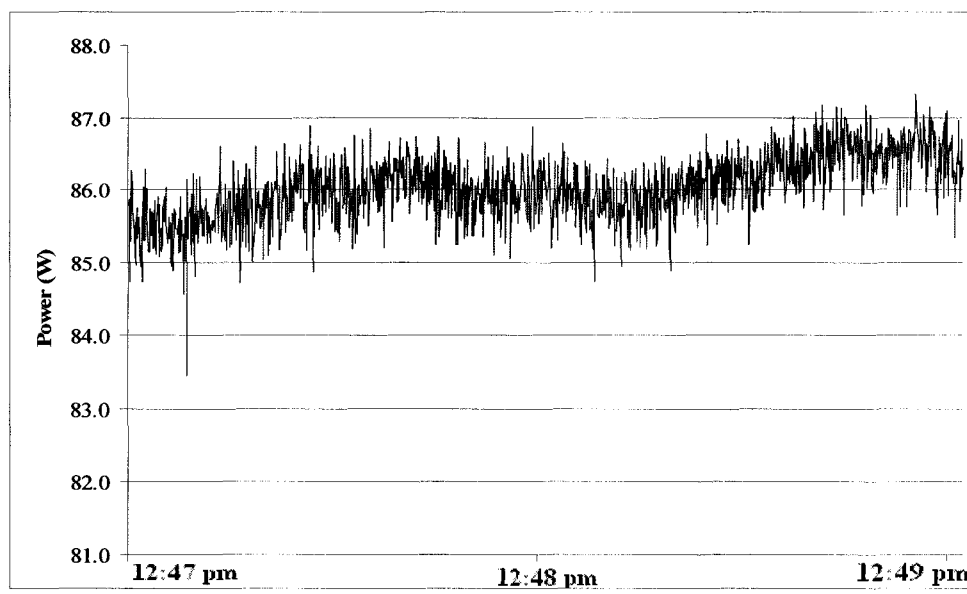


Fig. 6.27 Expanded Time Scale of Input power1

The magnitude of the input power1 fluctuation is around 1.1W, which is smaller than the proposed method 1.3W. This is because using the slope of P-V curve as the control variable causes relatively lower power oscillation. The reason for this was already explained and experimentally shown in the indoor experiment (in the section of 6.2.1).

Finally from time period of 1:30pm to 2:00pm, the IncCond method is employed to the system, and the experimental results are depicted in Fig. 6.28 and Fig. 6.29 respectively.

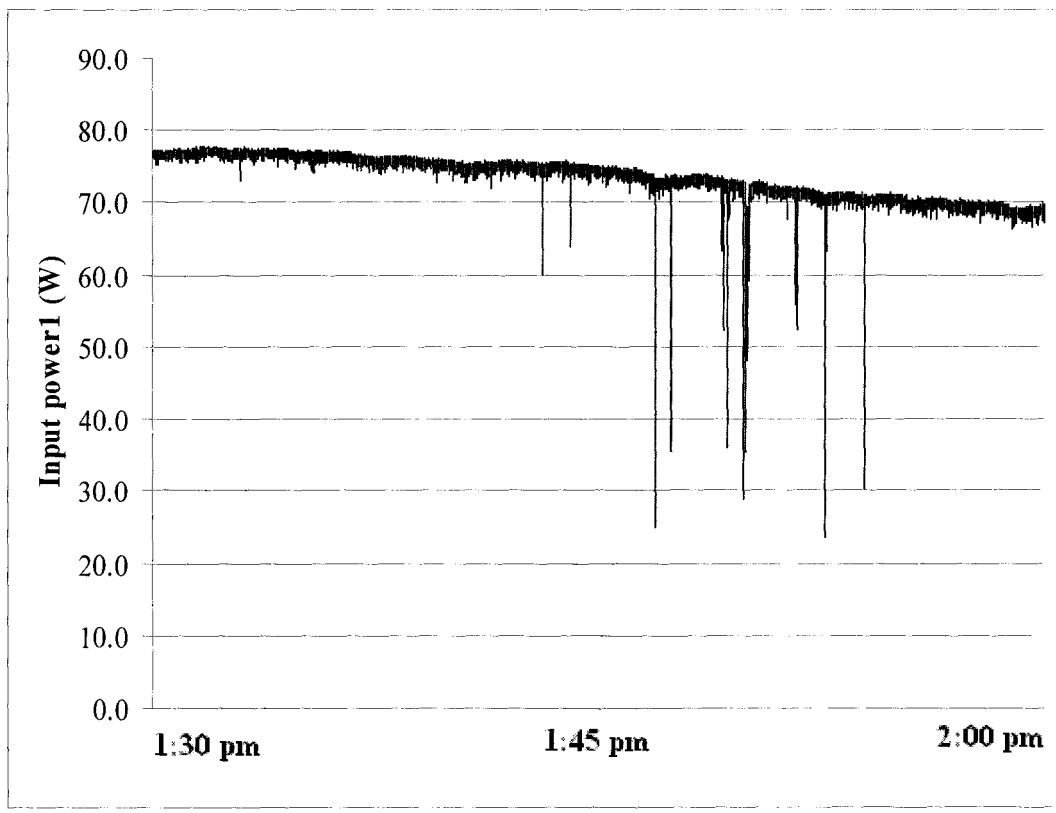


Fig. 6.28 The Input Power1 to One Converter by IncCond Method

Theoretically the IncCond method should give relatively smoother power curve than the proposed method, because the proposed MPPT strategy is based on the input

power only, and the operating point oscillates around the MPP since this method does not assume that the MPP is known. Contrast this with the IncCond method, once the operating point is controlled to reach the MPP, then it should be stabilized. Fig. 6.29 shows that the magnitude of the input power fluctuation is around 1.4W, which is larger than the proposed method and dp/dv method. One reason for this relatively larger power oscillation might be the unstable climate conditions, another one might be insufficient accuracy of sensors or ADCs. Since this control method is based on the slope of P-V curve calculation, it requires a high degree accuracy of sampling data in order to give precise divisional calculations.

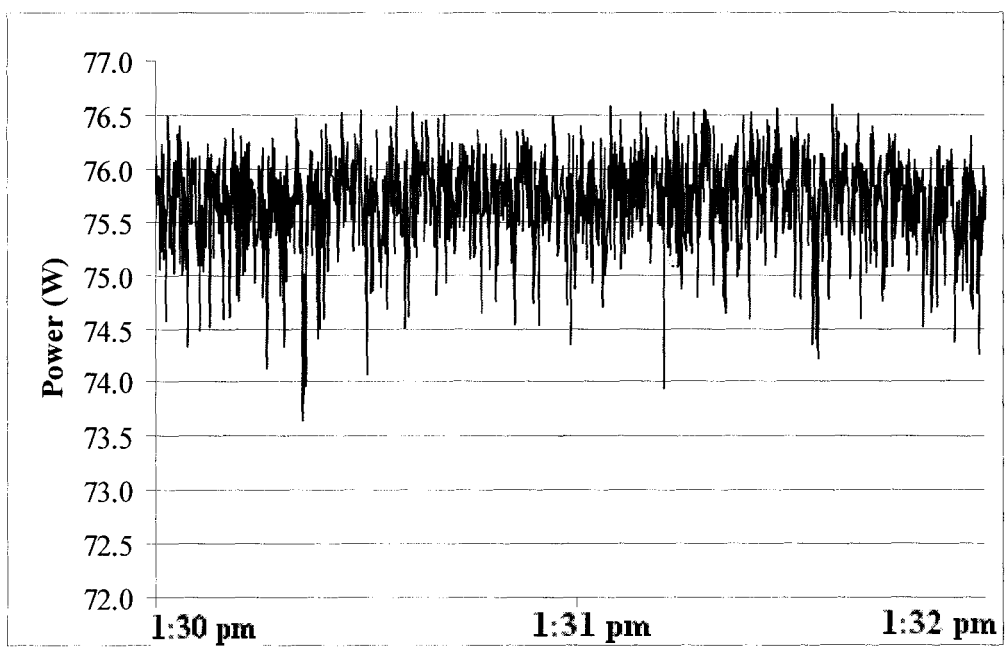


Fig. 6.29 Expanded Time Scale of Input Power1

From Fig. 6.28 we can visibly notice that there are some large power degradations as low as 25W, which are probably caused by the rapid weather conditions,

such as fast-moving clouds over the PV array area. Once clouds pass the PV array, we can clearly see that the IncCond method can quickly relock to the new MPP as shown in Fig. 6.28. Overall the input power extracted to one converter begins at 77W, and it gradually decreases to 70W due to the decrease of the sun intensity (from time 1:30pm to 2:00pm). On the same day, the V_{gs} waveforms of two MOSFETs were measured. The duty cycle of the MOSFET fluctuates around 65%, it is due to the fact that V_{mpp} is approximately constant when the PV array temperature is not changing severely. In our case, the ambient temperature is within the range of 3°C to 5.1 °C.

Case two: On Nov. 26th2007, the sky was overcast, and the humidity was around 90% during the testing period. The ambient temperature was between 5 °C and 6 °C. We know that humidity is a measurement of amount of water vapor in the air, and the water vapor reflects the partial sunlight back to the sky. The PV array also uses the diffuse radiation from the clouds. The brighter it is outside, the more power can be generated from the PV array, regardless of whether the sun is directly visible or not. Thus as cloud cover thickens, the sunlight is reduced, which in turn reduces the power drawn from the PV. During that day, the overall distribution of light over the sky was very low. The actual experiment was performed from 10:30am to 11:00am, and then it started raining. The data is plotted and shown in Fig. 6.30, which shows that the total power drawn from the PV array is very low, roughly between 7W and 12W. And as it began raining the power dropped greatly (less than 6W), and hence caused the MPPT to be turned off, because there is not enough power to charge the batteries. The duty cycle was also measured. Comparing this duty cycle with the previous one when the sky was sunny (on

Nov. 25th), the duty cycle is smaller. This is because the open circuit of PV array drops by a considerable amount when the sun intensity is extremely low and the temperature is approximately same as the day on Nov. 25th. Thus in turn the corresponding V_{mpp} is reduced, which results a relatively smaller duty cycle, in this case it is around 53%. We can conclude that partial shadows can cause power degradation, but mainly cloudy and foggy or raining days can cause major discrepancies, which the MPPT is useless under these environment conditions.

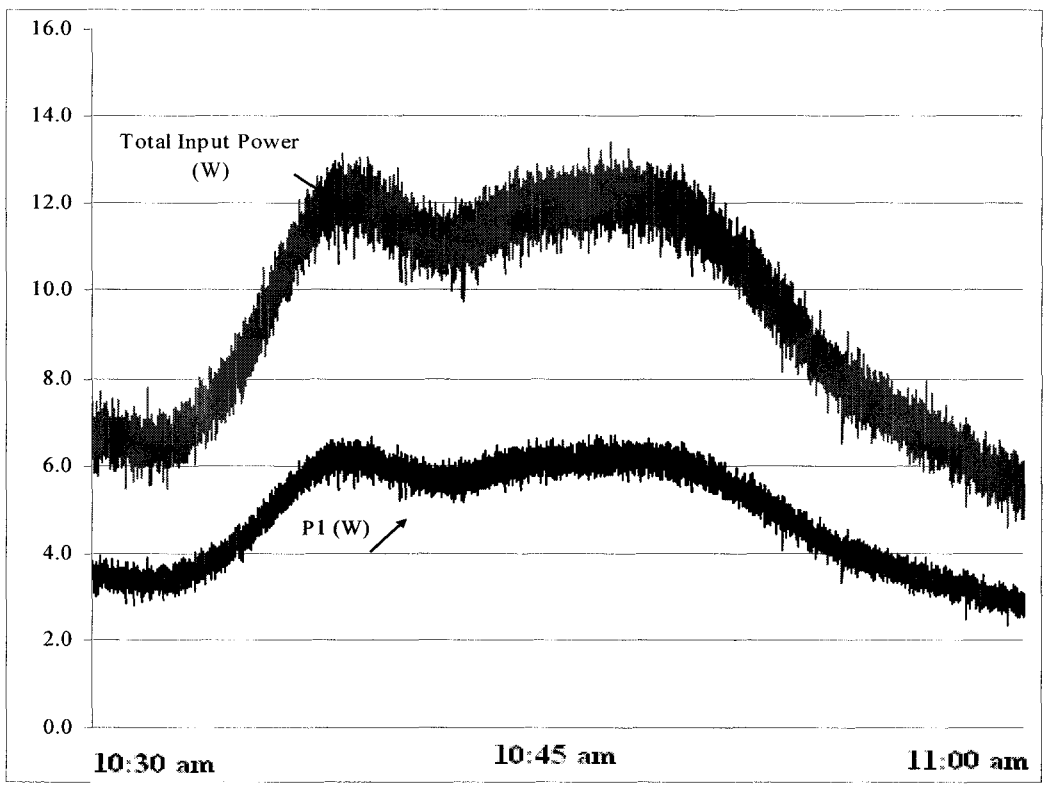


Fig. 6.30 Input Power1 and Total Power by the Propose Method

Case three: On Nov. 28th2007, the ambient temperature was between -4°C and 1°C. It was a cloudy day but with randomly sunny breaks during the time period of

10:30am to 12:30pm. Nov. 28th was brighter than the day on Nov. 26th, but after 12:30pm it became mainly cloudy, which caused the sun intensity to decrease abruptly.

From 10:40am to 11:10am, without using the MPPT as the interface between the solar source and the batteries, the direct-coupled method was tested first. The experimental data are graphed in Fig. 6.31 and Fig. 6.32 respectively. Fig. 6.31 shows that this conventional connection method forces the input voltage to operate a little bit higher than the battery charging voltage, in order to do the charging job.

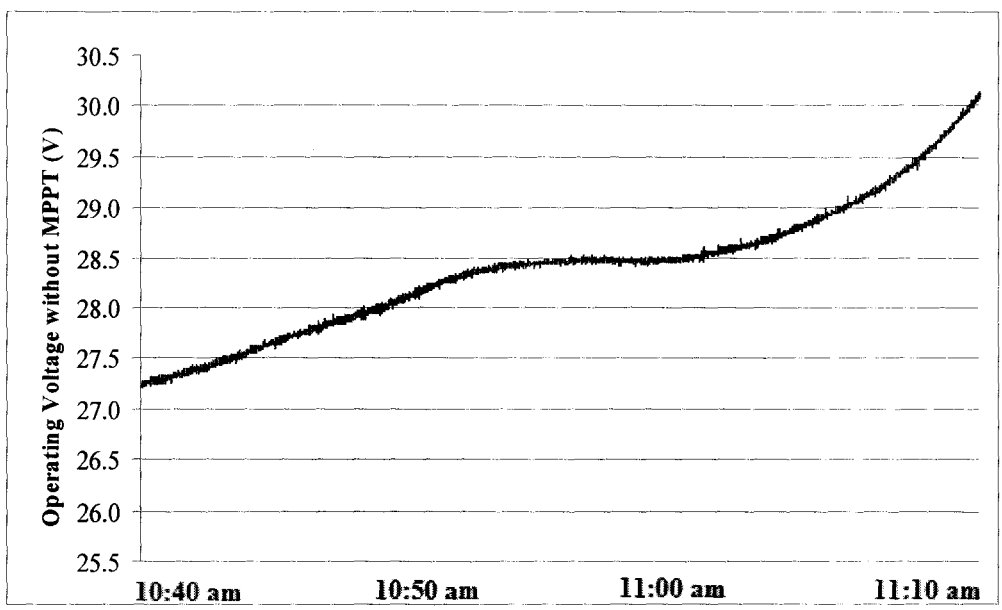


Fig. 6.31 Operating Voltage to One Converter by the Direct-Coupled Method

Typically this input voltage is not the optimal operating voltage generated from the PV array, and more importantly this voltage is totally dependent on the load. In our case, when the PV array is charging the 24V battery bank, and as the input current increases the operating voltage gradually increases as well. The total power generated

from the PV array is increased from 11W to 29W as the sky becomes slightly brighter, and the diagram is depicted in Fig. 6.32.

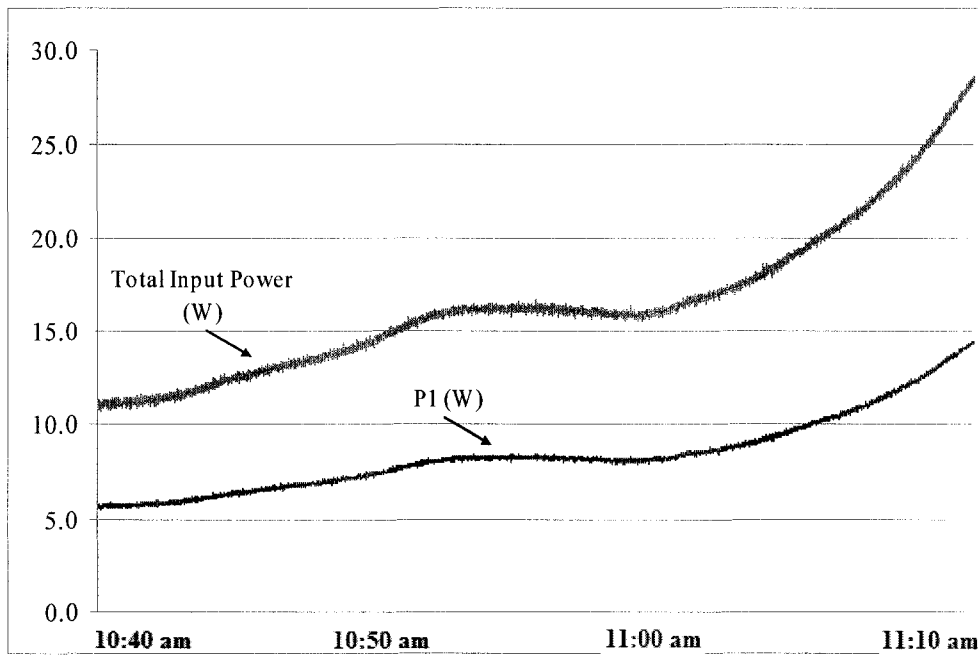


Fig. 6.32 Input Power1 and Total Power by the Direct-Coupled Method

From 11:10am to 11:40am, the sky became much brighter, and started having several sunny breaks. Rather than simply directly connecting the solar source to the batteries, the proposed MPPT was connected in between the source and the load, and the dp/dv control technique was employed in the system. The experimental results are illustrated in Fig. 6.33 and Fig. 6.34 respectively.

Fig. 6.33 clearly shows that the operating voltage with the implemented MPPT controller is around 55V to 56V. Despite the rising sunlight intensity, comparing with the previous classic direct-coupled method, the operating voltage is imposed from the battery

charging voltage 28V to an optimal voltage 55V. This added 27V potential produces additional wattage (as shown in Fig. 6.34) and increases the output charging current.

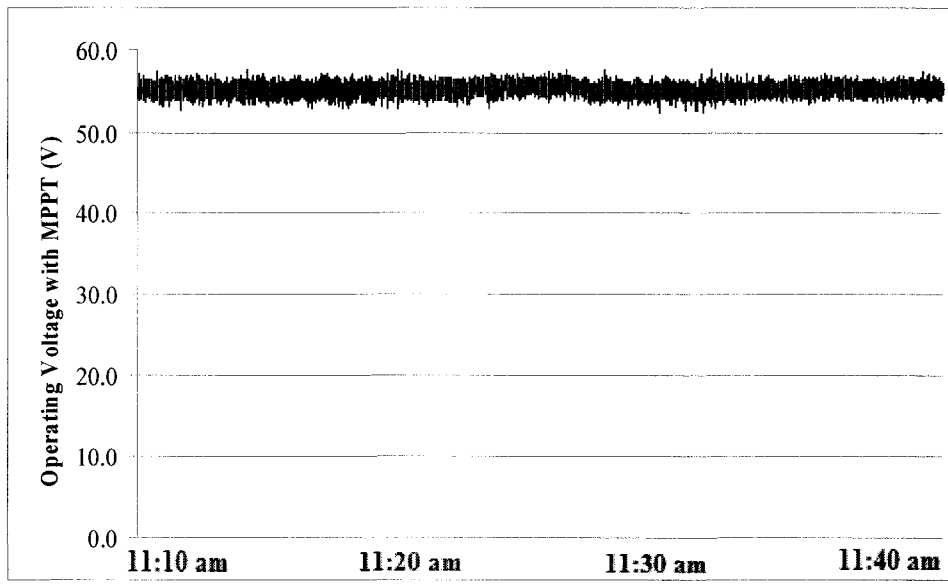


Fig. 6.33 Operating Voltage to One Converter by the dp/dv Method

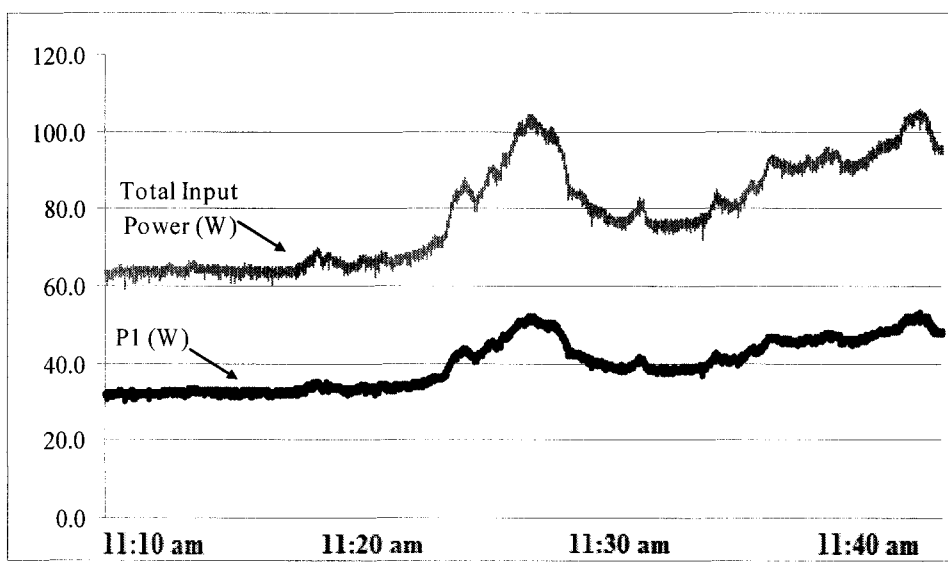


Fig. 6.34 Input Power1 and Total Power by the dp/dv Method

From 11:40am to 12:10pm, the clouds became thick so that the sun illumination is falling fast over time. The proposed control method is executed to the MPPT system, and the experimental results are shown in Fig. 6.35 and Fig. 6.36.

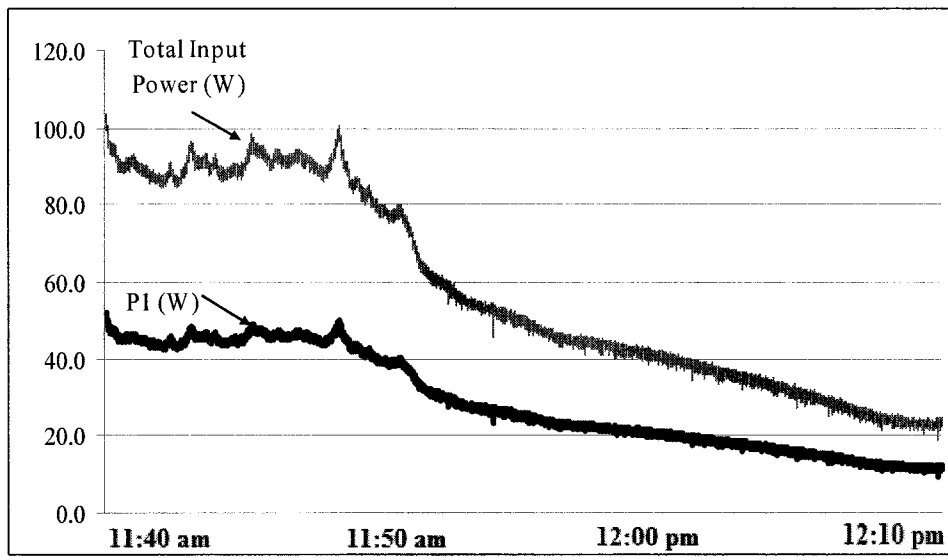


Fig. 6.35 Input Power1 and Total Power by the Proposed Method

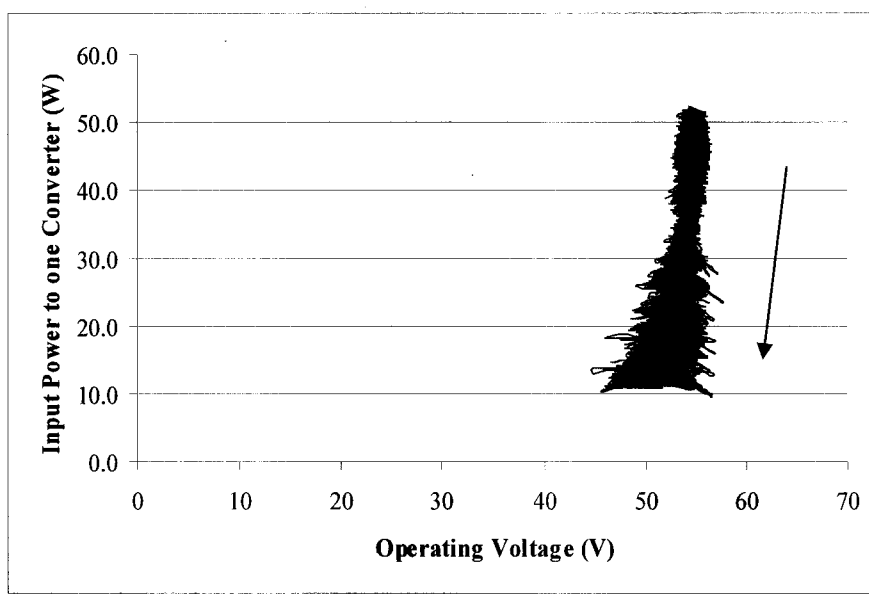


Fig. 6.36 Trajectory of Input Power versus Input voltage by the Proposed Method

We can see that the input power is dropping drastically from 57W to 11W. This shows that the proposed method is able to respond fast enough without error under the rapid weather change conditions as seen in Fig. 6.35. Fig. 6.36 shows that as the sunlight diminishes the controller still kept seeking the new MPPT.

From 12:10pm, the IncCond method is applied to the MPPT system. The resulting diagrams imply that this method is not capable of tracking the MPP due to extremely low sun illumination, and the duty cycle is forced to work in unity. This leads directly connecting the input to the load as seen in Fig. 6.37 and Fig. 6.38 respectively.

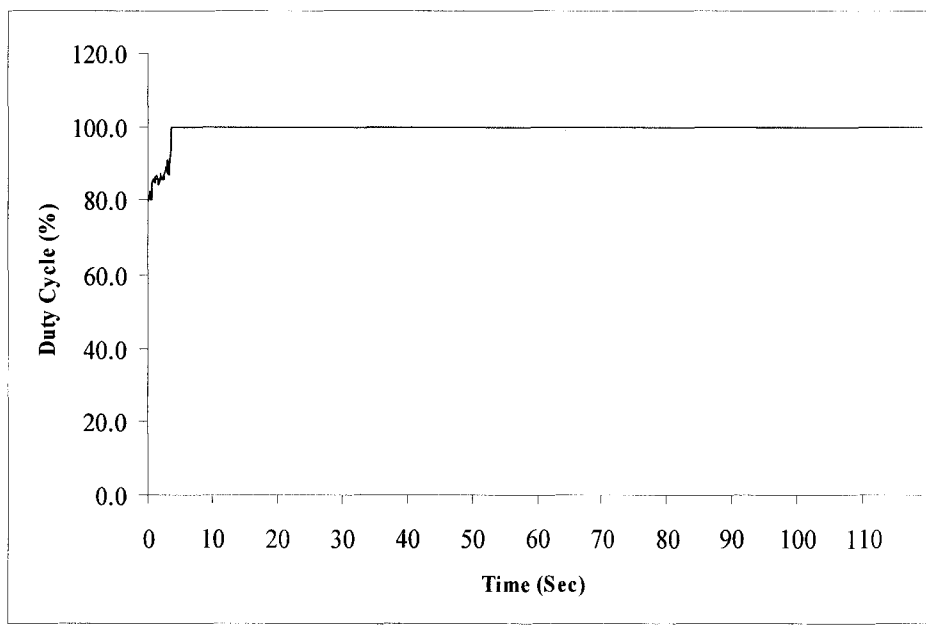


Fig. 6.37 Duty Cycle by the IncCond Method

Comparing with the day which used the proposed method (Adaptive Hill-Climbing method) on Nov. 26th, the proposed algorithm is still able to capture the MPP even though the sun intensity is even lower than the day on Nov. 28th. This makes us

conclude that the proposed method can effectively track the MPP under the low sun intensity without confusion.

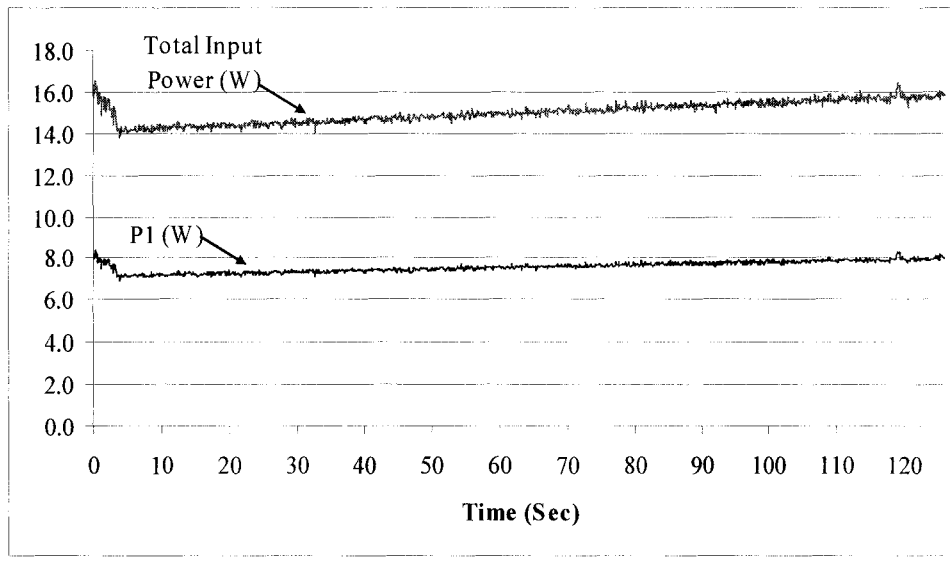


Fig. 6.38 Input Powers and Total Powers by the IncCond Method

The IncCond and dp/dv methods are not able to seek the MPP and are not stable or reliable given the condition of low sun intensity. Since they are both based on the same tracking concept, which uses the principle of dp/dv = 0. They both make the decision on the sign of dp/dv, to determine the MPP by constantly sampling the input power and voltage drawn from the PV array.

6.3.3 Outdoor Experiment Conclusion

The practical tradeoff among tracking response time, suppression of power fluctuation in steady-state, and relevance of system noises must be carefully considered in the determination of tuning parameters. Different MPPT control algorithms were

thoroughly investigated via the actual outdoor experiments during different types of atmospheric conditions, such as uniform or unstable solar illumination, or severely low sun intensity.

The proposed method, Adaptive Hill-Climbing algorithm, can seek the MPP effectively under any weather condition, especially low sun illumination. Even though the power fluctuation which occurs in the proposed method is eventually slightly larger than the other methods, it is still acceptable. For the dp/dv method, the experimental evidence has shown the fact that the dp/dv method is capable of causing less power oscillation. The IncCond method can successfully follow continuously varying MPP under rapid atmospheric conditions. However both of dp/dv and IncCond methods fail to track the MPP under low sunlight illumination. Overall, the proposed method is very simple, reliable and easy to implement. In contrast, the methods of dp/dv and IncCond both need adequate accuracy of sensed signals in order to determine a proper control direction towards the actual MPP. The experimental results show that the proposed algorithm exhibits a better overall performance. According to the data on Nov.25th only, the designed MPPT controller can significantly increase the total input power generated from the PV array by up to 59.85% comparing to the direct-coupled method.

The experimental results confirmed the predicted performances measured in the indoor PV emulation system. The entire MPPT system is simple. It is comprised of only one power stage and one DCU controller which implements two functionalities: one is the proposed MPPT control strategy. The other is a basic charging method for the battery bank. Overall the designed MPPT system is able to provide robust and reliable

conversion under various weather conditions, and this 2-parallel PV system can be expanded to N-parallel PV system by adding control chips and upgrading or modifying the control algorithm.

Chapter 7

Conclusion and Future Work

7.1 Summary and Conclusion

This thesis has presented a detailed design process and a development system for an integrated PV system, including the comparison of various implementations of Maximum Power Point Tracking (MPPT) control methods. The development system provides a tool for comparison and analysis of different MPPT control algorithms. Experimental results were shown in order to demonstrate the advantages and the disadvantages of each control methodology.

Due to the nonlinear nature of PV array, the maximum power and its correspondingly optimal operating voltage V_{mpp} fluctuate in response to array's temperature and the sun intensity. The proposed new MPPT implemented is able to continuously extract the maximum power delivered by the PV array between the solar source and the load under different climate conditions, and performs better than the conventional methods described in the literature.

One major challenge dealt with in the outdoor experiment was the inability to control the testing conditions. The power drawn from the PV array is dependant on how direct the sunlight is at that time of day. Factors which affect the solar power include the angle at which the PV array is aimed at the sun, the temperature of the solar panel, and the visibility level of the sky. As a result, it is very difficult to accurately compare different MPPT control algorithms under different weather conditions. The indoor

experiment allowed the control of various parameters which made comparison of the different control methods possible under identical conditions.

The proposed MPPT control strategy (Adaptive Hill-Climbing) is a modified version of the conventional Hill-Climbing method. Only one control variable and an adaptive power window are used in this new method. The adaptive power window intentionally attenuates the effect of system noise on the decision-making process of the MPPT control algorithm. We have experimentally proven that the adaptive power window can decrease the power fluctuation in the system.

Based on the results discussed in chapter 6, the indoor emulation experiment showed that the Adaptive Hill-Climbing method caused less power oscillations than the conventional Hill-Climbing method and it gave much higher efficiency than the dp/dv method when the input power was low. Accordingly with the outdoor experimental results, even though a slightly larger magnitude of 1.3W (0.15% of input power) power fluctuation was produced by the Adaptive Hill-Climbing method than 1.1W (0.13% of input power) by the dp/dv method, the Adaptive Hill-Climbing method was able to respond faster under rapid atmospheric conditions. The incremental conductance method produced the magnitude of 1.4W power oscillation, which ideally should not be larger than the magnitude generated by the Adaptive Hill-Climbing method. The IncCond method was not able to capture the maximum power point (MPP) when the sun intensity was as low as 9W input power generated by the PV arrays. In contrast the Adaptive Hill-Climbing method still performed properly when only 7W of input power was drawn from the PV arrays. The proposed MPPT control method increased the power generated by PV

arrays by up to at least 30% more than a PV system without an MPPT according to the outdoor experimental data on Nov.25th 2007 only.

Even though both the dp/dv and IncCond methods offer lower power oscillation than the proposed method, dp/dv and IncCond are unable to perform properly when the sun intensity is low, and they require much higher accuracy sensors and ADCs than the proposed MPPT method. Table 7.1 gives a summary of the advantages and disadvantages of each control methodology.

MPPT Method	True MPPT	Number of control variable	Pros	Cons
Hill-Climbing	Yes	1	The simplest MPPT	Oscillations around the real MPP, which causes more system power loss
(New) Adaptive Hill-Climbing	Yes	1	Simple, causes less power fluctuations than the Hill-Climbing, offers much higher efficiency than dp/dv and IncCond methods when the sun intensity is low, is able to capture MPP under rapid weather conditions	Results slightly larger power oscillations than dp/dv
dp/dv	Yes	2	Causes less power oscillations than the Adaptive Hill-Climbing, response fast under various weather conditions	Not able to perform efficiently when the sun intensity is low, require high accuracy of ADCs and sensors, and complex
IncCond	Yes	2	Quickly relock to the MPP under abrupt environment, produces less oscillations only if the precise of the ADCs and sensors is high enough	Not able to track the MPP when the sun intensity is low, requires much higher precise than Adaptive Hill-climbing, and complex

Table 7.1 Different MPPT Control Method Summary Based on Experiment

The flexibility of the proposed control method and the designed MPPT system can be exploited by adjusting it in a way that is applicable to different power systems with various requirements and tolerances. The designed MPPT was built with buck converters. The MPPT can be also constructed with other types of power converter (such as a boost converter) to meet other design constraints.

7.2 Project Refinements

The component choice in the current design needs additional review in order to further reduce some of the losses in the system. The driving voltage of the MOSFET is 16V, which is relatively high and causes a relatively large power loss in the gate driving circuit. If a lower gate driving voltage (such as 10V or even 6V) were chosen in the circuit, the power loss in the driving circuit would be lower and the spike voltage between the gate and the source of the MOSFET would be in turn lower as well. The designed power converter can also adopt synchronous rectification with soft switching technology to improve the efficiency of the controller. So far the proposed MPPT controller can only do fast-charging and float-charging. A more sophisticated charge-monitoring system may need to be considered. Current sensors and their conditioning circuits could be improved to provide more accuracy in order to make current measurements more reliable.

7.3 Future Research

As a further research of the present work, a number of new approaches or more appropriate alternatives, and recommendations for a strong emphasis on enhancing practical designs in terms of utilization efficiency and reliability are worthy of attention.

There are a number of ways to improve the efficiency and stability of the current design. There are several sources of power losses in the system. For example, actual charge currents could be decreased with wiring, circuit breakers, and the controller itself. Other power losses, such as mismatching losses, partial shadows, variations in current–voltage (I–V) characteristics of PV modules, differences in the orientations and inclinations of solar surfaces, and temperature effects could be investigated further.

PV modules manufactured by different technologies respond differently to the changes in solar illumination and cell temperature. Designing a MPPT control system which can handle any kind of disturbances is very important. The MPPT should be especially insensitive to variations in external disturbances, such as the degradation of solar cells over long period of time.

The proposed MPPT system is the simplest 2-parallel converter system. If the power demand is higher, the system will need to expand to a multiple-parallel converter system to meet the requirement. Multiple-parallel converters do not share the power evenly. This will make each converter's thermal stress different (such as component failure). Additional control features need to be considered in such system in order to force these multiple-parallel converters to distribute the power or current uniformly [52]. The concept and implementation of uniform current distribution need to be studied carefully in the current design (or larger modular architecture system) so that less component stress, higher reliability, good stability, and easier maintenance will be achieved. New experimental implementation and verification need to be performed using the uniform current distribution technique combined with the MPPT control method, and

further research may consider the use of the MPPT control approach in the other types of PV system (like a grid-connected PV system).

APPENDIX A

Hardware Experimental Data and Schematics

A.1 Voltage Sensing Circuit: Accuracy Test Result

V_{in} (V)	V_{out} (calculated) By using the ratio	V_{out} (measured) after the resistor-network	V_{out} (measured) after the voltage follower and RC filter (V)	The voltage difference between the calculated and measured data
5	0.239	0.23917	0.23939	0.0043
10	0.478	0.4821	0.4823	0.0002
15	0.717	0.7170	0.7172	0.0011
20	0.956	0.9569	0.9571	0.0008
25	1.195	1.1957	1.1958	-0.0004
30	1.434	1.4334	1.4336	-0.0004
35	1.673	1.6725	1.6726	-0.0005
40	1.912	1.9114	1.9115	0.0139
45	2.151	2.1648	2.1649	0.0081
50	2.39	2.3980	2.3981	-0.0014
51.9 @ MPP	2.481	2.4795	2.4796	-0.0032
66 @ open cct	3.1548	3.1511	3.1516	0.0043

Table A.1 Voltage Sensing Test Result

A.2 Input Current Sensing Circuit: Accuracy Test Result

Iin (A)	Calculated V_{CS} (V)	Measured V_{CS} from the output sensor (V) by using a multi-meter	Calculated V_{out} after magnifying circuits by using multi-meter (V)	Measured V_{out} by using a multi-meter (V)	$\Delta I_{in} = \frac{\Delta V_{out}}{0.4167}$ (error)
0	2.5	2.4975	3.2	3.2433	0.10391
0.1	2.5104	2.512	3.1583	3.204	0.10967
0.2	2.52083	2.523	3.1167	3.163	0.1111
0.3	2.53125	2.533	3.075	3.110	0.08399
0.4	2.54167	2.544	3.0333	3.074	0.09767
0.5	2.55283	2.555	2.99165	3.011	0.0464
0.6	2.5625	2.562	2.94998	2.979	0.06964
0.7	2.5729	2.573	2.9083	2.939	0.07367
0.8	2.5833	2.583	2.86664	2.899	0.07766
0.9	2.59375	2.593	2.82497	2.862	0.0886
1.0	2.604167	2.604	2.7833	2.823	0.09527
1.1	2.61458	2.615	2.7416	2.780	0.09215
1.2	2.625	2.6216	2.6999	2.7538	0.1293
1.3	2.63542	2.6322	2.6583	2.7111	0.1267
1.4	2.64583	2.6431	2.6166	2.666	0.11855
1.5	2.65625	2.6531	2.57495	2.6264	0.12347
1.6	2.6667	2.6636	2.5333	2.5847	0.12335
1.7	2.6771	2.6739	2.4916	2.5420	0.12095
1.8	2.6875	2.6848	2.4499	2.4990	0.11783
1.9	2.6979	2.6946	2.4083	2.4593	0.12239
2.0	2.7083	2.7054	2.3666	2.4158	0.11807
2.1	2.71875	2.7156	2.3249	2.3750	0.12023
2.2	2.72916	2.7262	2.2833	2.3326	0.1183
2.3	2.73958	2.7368	2.2416	2.2901	0.11639
2.4	2.750	2.7475	2.1999	2.2470	0.113
2.5	2.76042	2.7571	2.15825	2.2080	0.11939
2.6	2.7708	2.7677	2.1166	2.1657	0.11783
2.7	2.78125	2.7787	2.0749	2.1219	0.12279
2.8	2.79167	2.7892	2.0332	2.0792	0.11039
2.9	2.8021	2.7992	1.9916	2.0388	0.11327
3.0	2.8125	2.8097	1.9499	1.9975	0.11423

3.1	2.8229	2.8202	1.9082	1.9548	0.11183
3.2	2.8333	2.8302	1.8666	1.9147	0.11543
3.3	2.84375	2.8411	1.8249	1.8708	0.1102
3.4	2.8542	2.8510	1.7832	1.8315	0.1159
3.5	2.8646	2.8622	1.7416	1.7861	0.10679
3.6	2.875	2.8720	1.6999	1.7463	0.11135
3.7	2.88542	2.8832	1.6582	1.7014	0.10367
3.8	2.8958	2.8932	1.6165	1.6612	0.10727
3.9	2.90625	2.9039	1.5749	1.6182	0.1039
4.0	2.9167	2.9154	1.5332	1.5716	0.09215

Table A.2 Input Current Sensing Test Result

A.3 Experimental Results of Gate Drive Transformer Circuit

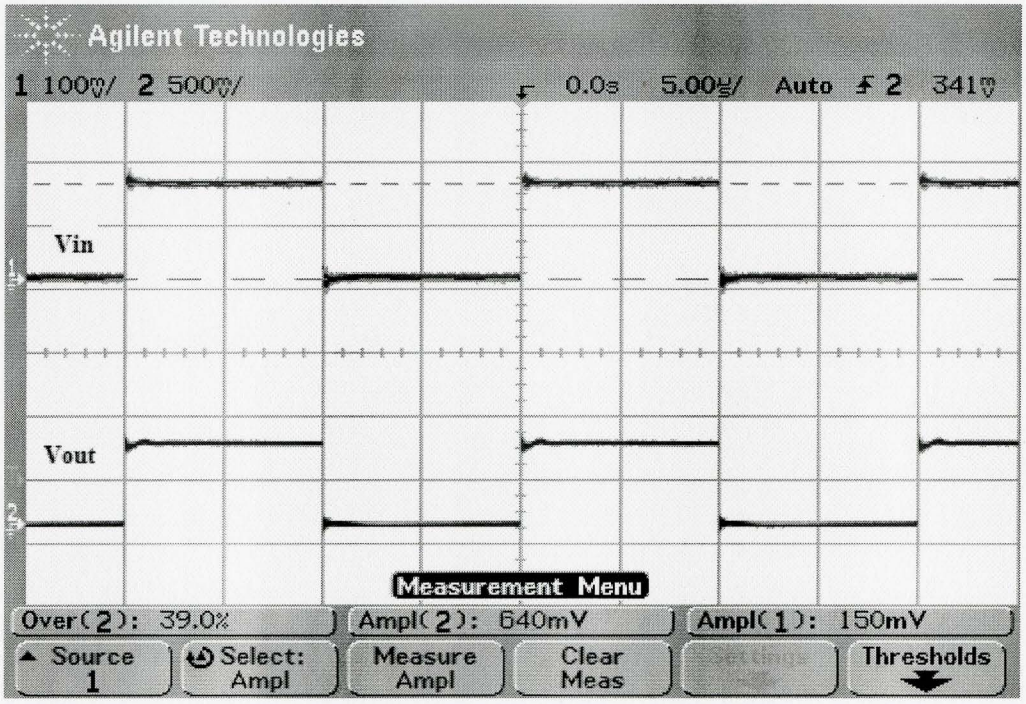


Fig. A.1 Waveforms of Vin VS. Vout by using 610AA

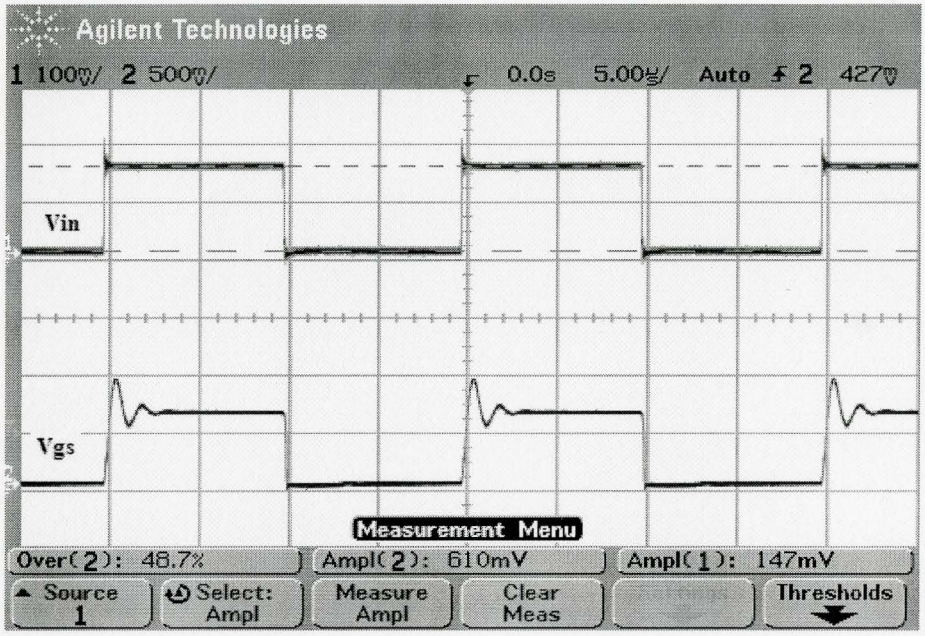


Fig. A.2 Waveforms of Vin VS. Vgs by using 610AA

A.4 MOSFET Driving Circuit Experimental Result

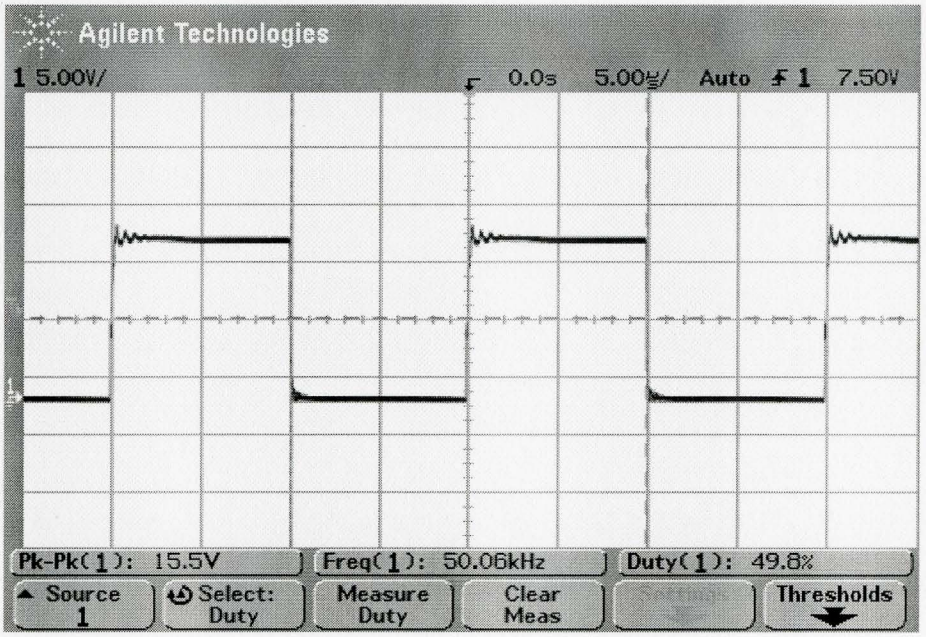


Fig. A.3 Waveform of V_{gs}

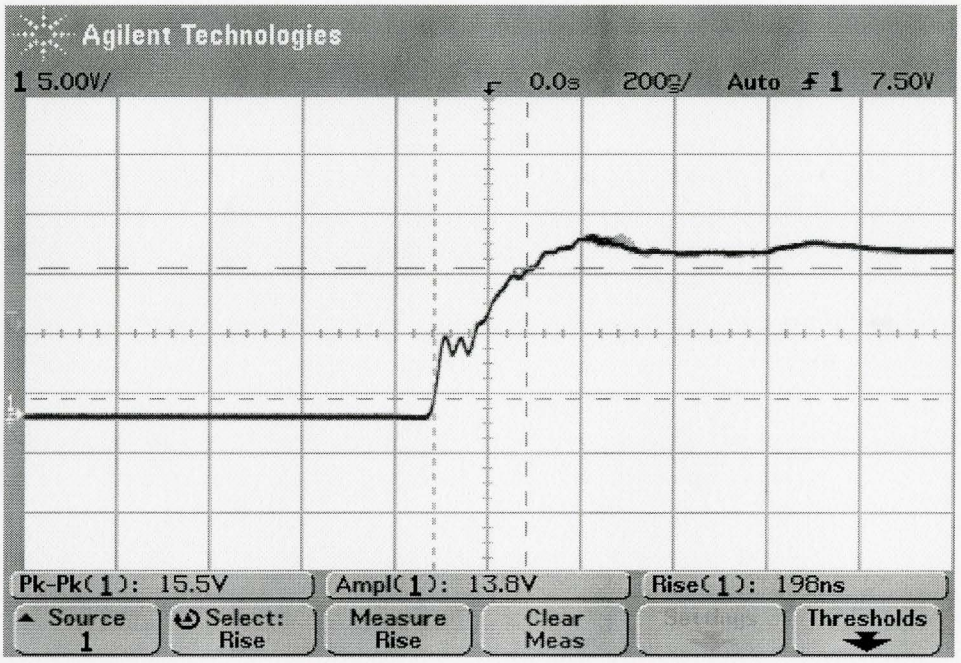


Fig. A.4 Rising time of V_{gs}

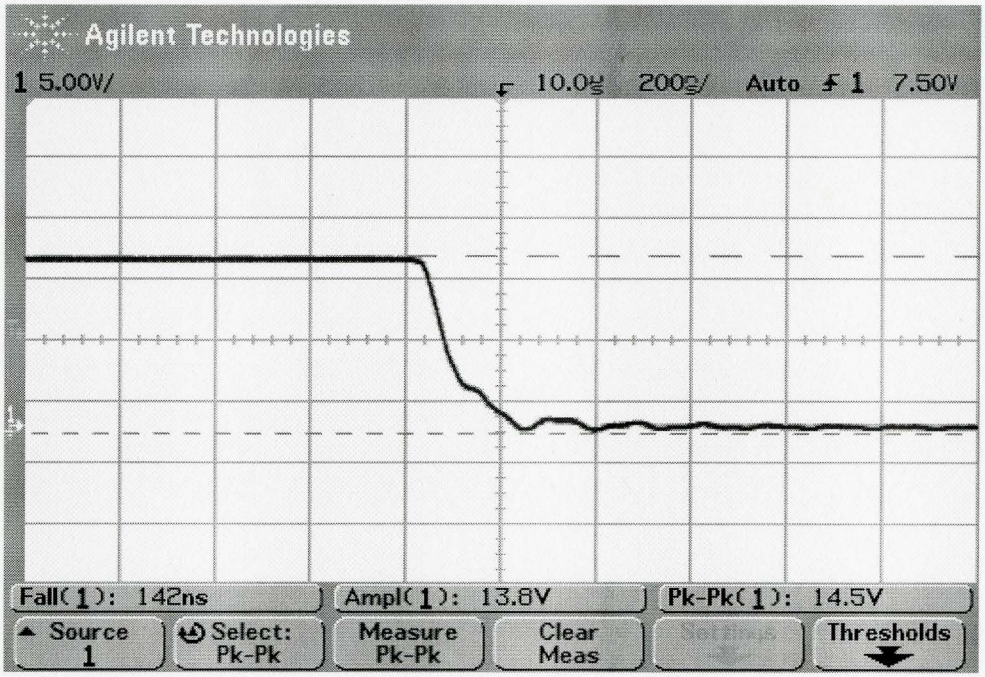


Fig. A.5 Falling time of V_{gs}

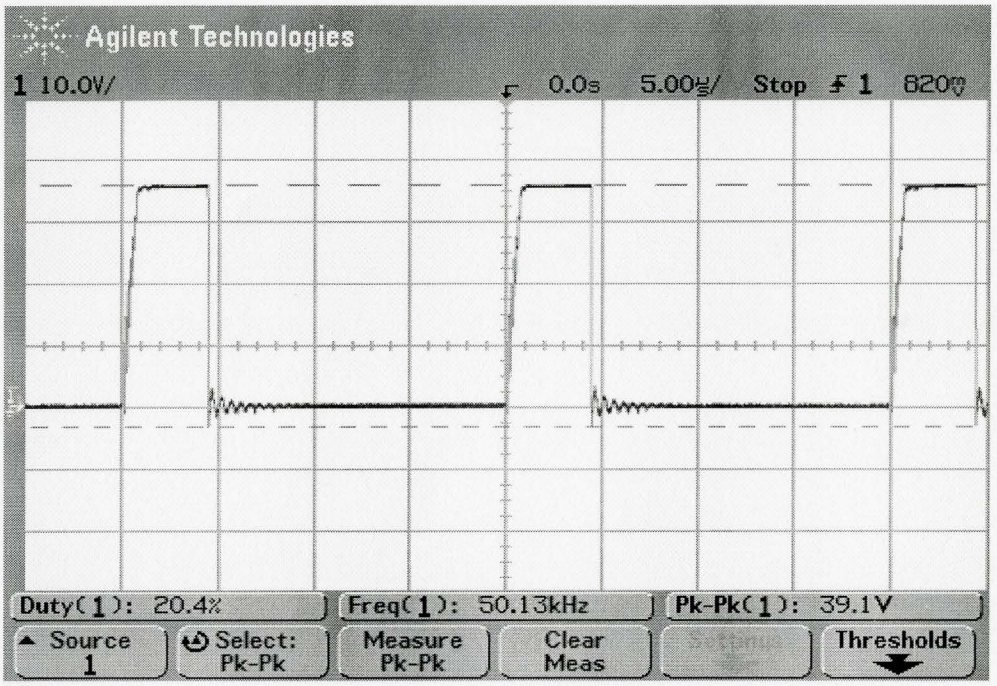


Fig. A.6 Waveform of V_{ds}

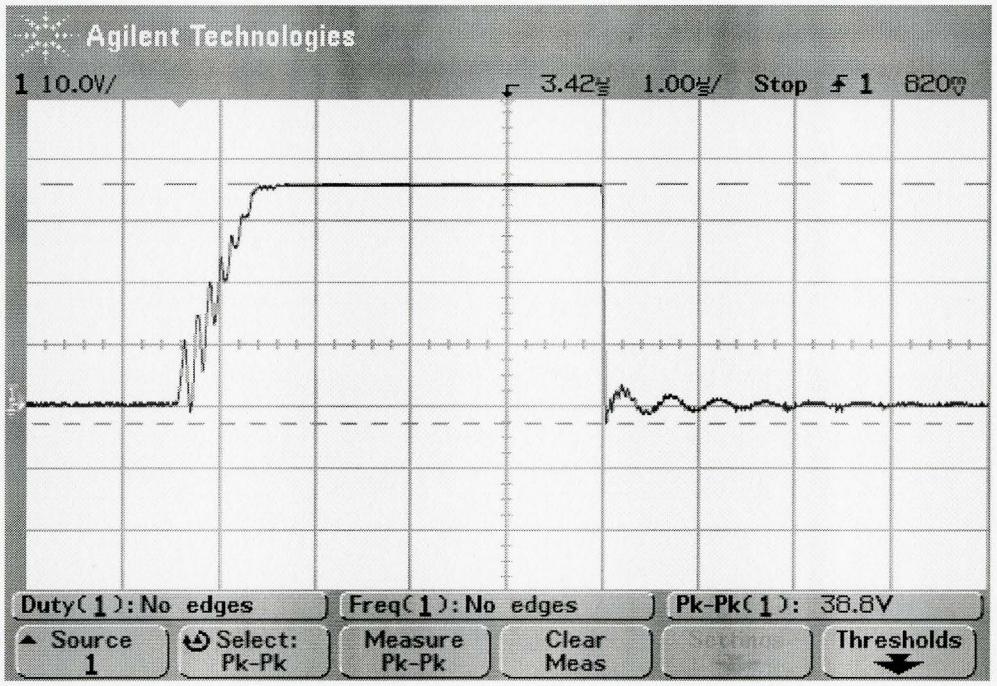


Fig. A.7 Zoom-In diagram of V_{ds}

A.5 Final Schematic Diagram of MPPT

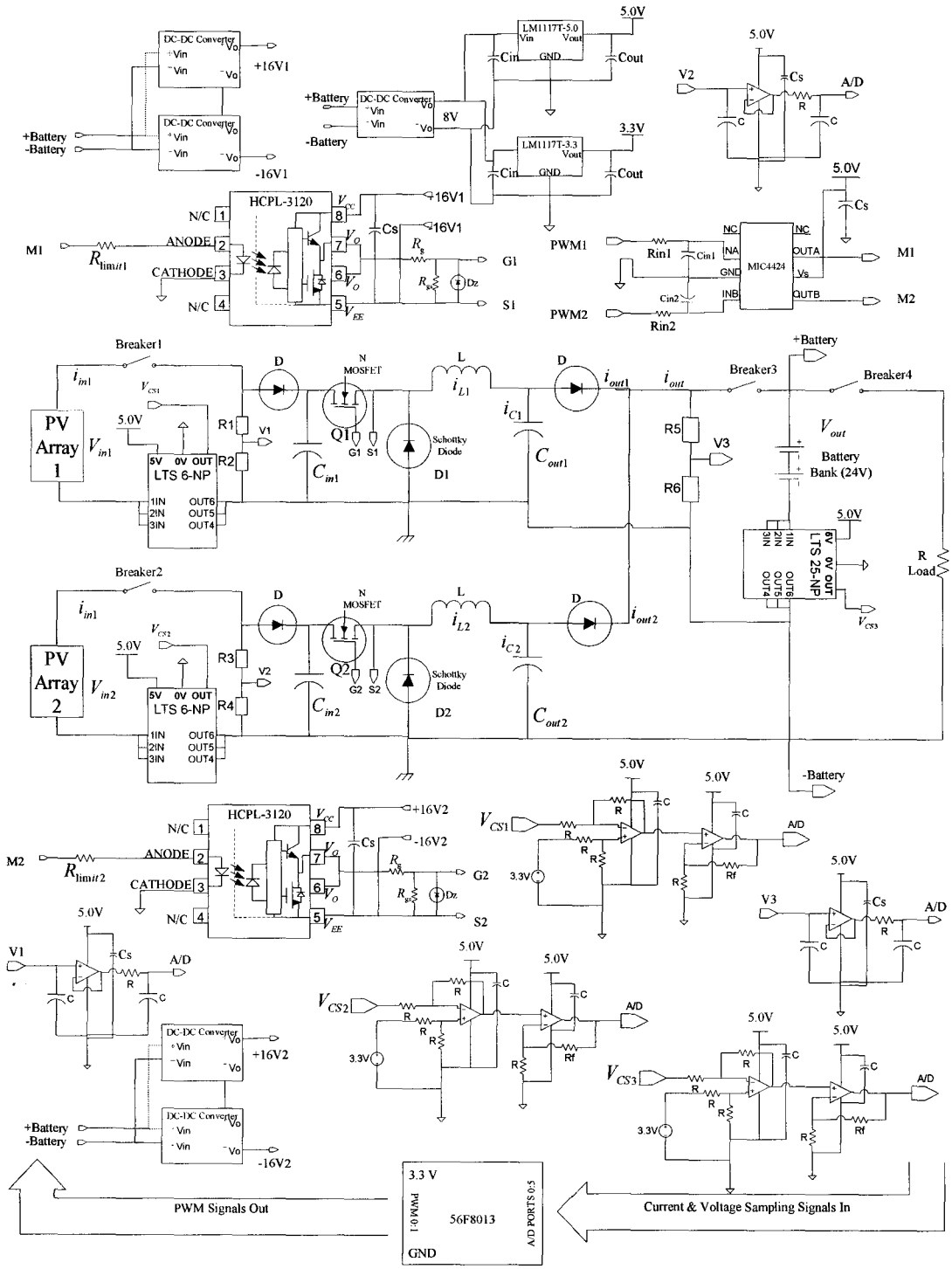


Fig. A.8 Final Schematic Diagram of MPPT

A.6 ADC Accuracy Test Data for 56F8013DEOMBOARD

ADC Ports	Input voltage Signal (V)	Calculated	ADC reading	Difference
ANA0 (I_in1)	0.185	230	237	-7
	3.225	4002	3996	+6
ANA1 (V_in1)	0.185	230	235	-5
	3.225	4002	3992	+10
ANA2 (V_out)	0.185	230	235	-5
	3.228	4002	3993	+9
ANB0 (I_in2)	0.186	231	227	+4
	3.225	4002	3995	+7
ANB1 (V_in2)	0.1868	232	226	+6
	3.227	4004	3996	+8
ANB2 (I_out)	0.186	231	225	+6
	3.225	4002	3997	+5

Table A.3 ADC Accuracy Test

The calculated formula is incoming voltage signal multiplying by 1240.91.

A.7 MPPT Final PCB Layout

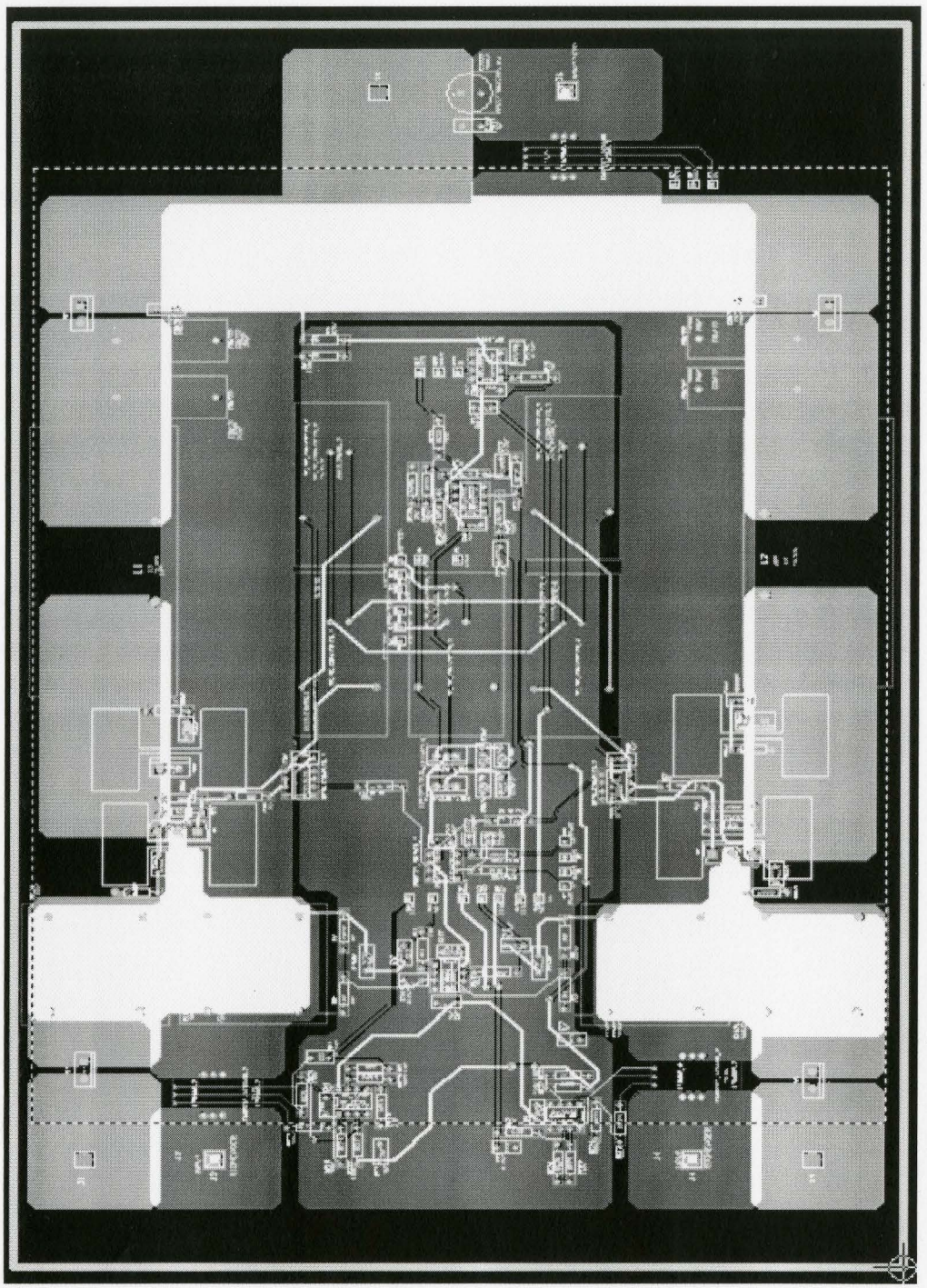


Fig. A.9 MPPT Final PCB Layout

A.8 56F8013 Chip Information

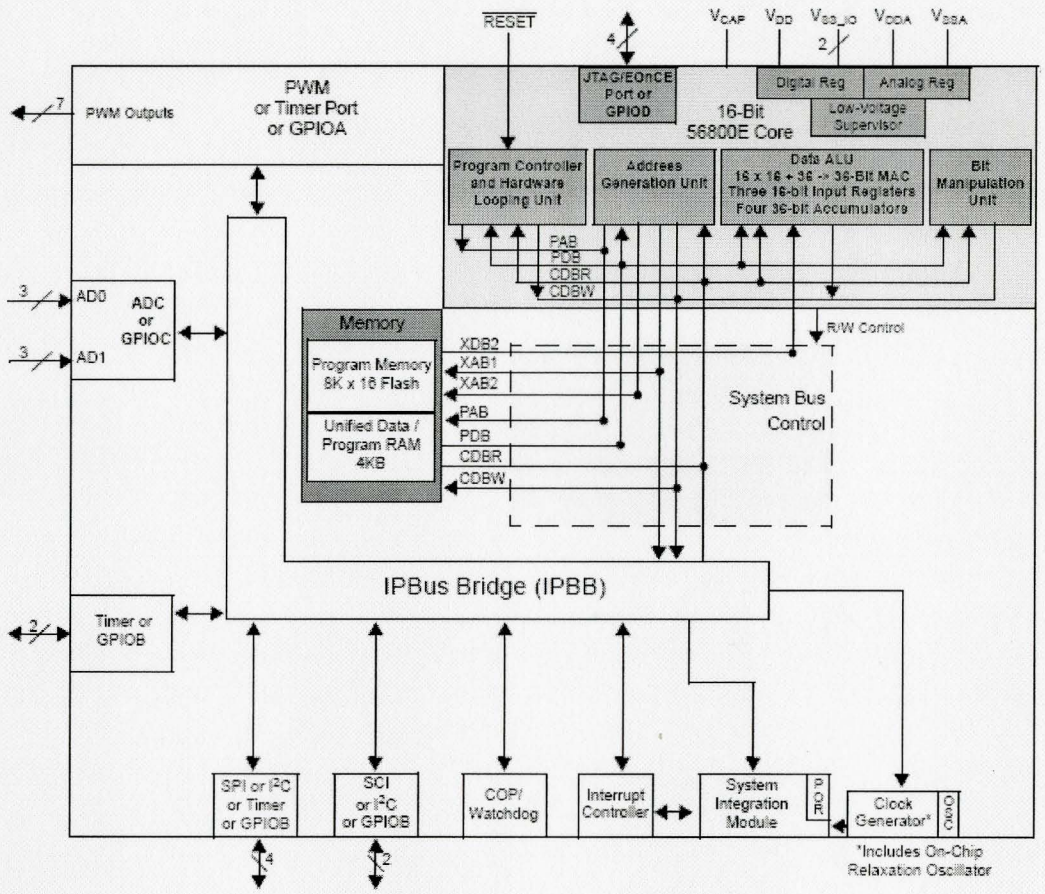


Fig. A.10 56F8013 Block Diagram

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