# SUBSTRATE BIASING TECHNIQUES ON GILBERT MIXER

# ANALYSIS AND DESIGN OF A LOW POWER 1.2 V CMOS DOWNCONVERSION MIXER UTILISING SUBSTRATE BIASING

By
HORACE MAN-HO GON. B.ENG.
McMaster University, April 2001

A Thesis
Submitted to the School of Graduate Studies
in Partial Fulfillment of the Requirements
For the Degree
Master of Applied Science

McMaster University

Copyright by Horace Gon, Oct 2005

MASTER OF APPLIED SCIENCE (2005) McMaster University
Electrical and Computer Engineering Hamilton, Ontario

TITLE: Analysis and Design of a Low Power 1.2 V CMOS Downconversion Mixer Utilizing Substrate Biasing

AUTHOR: Horace Man-Ho Gon, B.Eng. (McMaster University)

SUPERVISOR: Professor James C.H. Chen

NUMBER OF PAGES: ix, 121

# ABSTRACT

This thesis presents detail theoretical analysis of downconversion Gilbert cell mixer with the improvements on major performance parameters by utilizing different substrate biasing techniques. By modifying the threshold voltage of the switching core, the LO transistors perform more ideally as a perfect switch. It improves the active mixer performances in conversion gain, noise and linearity performances. The techniques are implemented on a 1.2 V low power CMOS downconversion mixer for performance comparisons between simulation and measurements result. They are realized in TSMC 0.18 um CMOS technology. It shows that body-biasing techniques help to increase the switching efficiency of the Gilbert mixer. And a mixer with a better switching provides better performance. With no additional power consumption, the no body effect technique in Design B has shown a 1.5 dB higher in conversion gain, 2 dBm higher in IIP3, and a 0.5 dB lower in NF performance. With the varying biasing technique implemented in Design C, it shows an improvement of 22 dB in conversion gain. Both Design B and C have less than 2 mW power consumption and are suitable for Bluetooth applications. This thesis also introduces a stage-by-stage procedure for designing a Gilbert mixer; design tradeoffs at each stage are also discussed.

# ACKNOWLEDGEMENT

I would like to take this opportunity to thank my supervisor, Dr. James C.H. Chen, for his guidance and continuous supports during my research work. The research work would not have completed without his advices. I would also like to thank Dr. M. Jamal Deen and Dr. Nicola Nicolici for being the committee members of my thesis defence.

I would like to express my gratitude to Sasan Naseh and Wai Leung Ngan for their technical assistance. I would also like to thank Cheryl Gies for her prompt and friendly services.

I would like to acknowledge the CMC for arranging the fabrication of the test chip.

I would like to thank my parents, Cheung Wai Gon and Fung Kuen Wong, and my brother Elvin Gon for their understandings and supports in this academic pursuit. I would like to extend my appreciation to Nadia Lau for her help in revising my thesis and her continuous supports on my research work.

# TABLE OF CONTENTS

# LIST OF FIGURES

# LIST OF TABLES

# CHAPTER 1
# INTRODUCTION

## 1.1 Motivation

The rapid growth in wireless communication systems for past decades has given tremendous energy in the development of radio frequency (RF) integrated circuits (ICs). Mixer is one of the main components in receiver architectures to accomplish frequency conversion. It is important to ensure the baseband signal is slow enough to save the computation power for data processing. There are many challenges for designing a good mixer. The performances of a mixer limit the overall sensitivity of a receiver. Mixers are nonlinear in nature to perform a frequency conversion. However, it is important to design a mixer as linear as possible to restraint the generation of unwanted intermodulation distortions between signals. It is necessary to design a mixer with competitive performance to meet with the ongoing demands. This thesis provides detail analysis of the substrate biasing techniques in Gilbert cell mixer for improving mixer performances. Design tradeoffs at each stage of a Gilbert mixer are also presented to ease the difficulties in the design process of a double-balanced mixer.

The complementary metal-oxide-semiconductor (CMOS) transistors are used in this thesis design because of the inexpensive cost and ease of integration with digital circuits to meet the increasing demand of wireless communication products. In addition, the need to integrate every components of a transceiver on a single chip is also a driving force for the continuous development in the metal-oxide-semiconductor field-effect

transistors (MOSFETs). With the downscaling of CMOS technologies, there is an ongoing reduction in the supply voltage, which drives the new RFIC design to the low power applications. It is necessary for the realization of the system-on-chip technology because of the limitation of battery lifetime. As a result, the demand of highly integrated CMOS RFIC building blocks in the low power consumption initiatives the design of a CMOS Gilbert mixer for the applications of popular Bluetooth technology.

## 1.2 Research Goal

This thesis is aimed to provide detail anaylsis in the study of substrate biasing techniques and their effects on the improvements of major performance parameters of mixers. A downconversion Gilbert cell mixer is designed for low power low voltage applications using different bulk terminal biasing techniques to improve the switching characteristics at the LO switches.

Through Canadian Microelectronics Corporation (CMC), 0.18 um CMOS technology is utilized in the mixer circuit. A typical Gilbert mixer, operating at 2.4 GHz with a supply voltage of 1.2 V, is designed with three different bulk terminal biasing techniques. The effects with different biasing techniques are examined and the simulation results are compared with the measurement results to evaluate the validity of the techniques. Even though the main focus is on the study of body biasing techniques, designs are compared with the most recent 0.18 um CMOS mixers to examine the usability of the designs for Bluetooth applications.

## 1.3 Thesis Outline

This thesis is composed of six chapters.

Chapter 1 presents the motivation and research goal with a summary of the thesis outline. An overview of Bluetooth technology is also discussed.

Chapter 2 is an introduction of some typical CMOS mixer topologies.

Chapter 3 provides the fundamental knowledge on mixer circuitry. The major performance parameters of mixers are discussed briefly in order to ease the explanations and comparisons of the most popular mixer topologies that are presented in chapter 2. Theoretical improvements in major parameters are also shown with the improvement on switching efficiency at the switching core.

Chapter 4 discusses design tradeoffs in a Gilbert mixer. It presents design procedures for a Gilbert mixer on the circuit level followed by an example using automation tools to design the Gilbert mixer. The studies of body-biasing techniques are presented with the simulation and measurement results.

Chapter 5 examines the discrepancies between the simulation and measurement results. Experimental setups are shown. And this chapter also provides different techniques to optimize the thesis design and it ends with suggestions on possible future work.

Chapter 6 concludes this thesis report.

## 1.4 What is Bluetooth

Bluetooth is the codename for a technology specification for small size, low cost, and short-range radio links between mobile phones, mobile PCs and other portable devices. Cost and space considerations are among the primary motivators for the drive toward a single-chip system solution. Since Bluetooth chips are intended for portable battery-driven equipments, provisions for saving power consumption are mandatory. The Bluetooth Special Interest Group (SIG) is an industry group consisting of nine leading computing and telecommunication companies. It originates at Ericsson in 1994; it is likely the first connection between headsets and mobile phones. Bluetooth enables users to connect a wide range of telecommunication and computing devices conveniently without connection cables. It also supports both point-to-point and point-to-multipoint connections. The modulation scheme is Gaussian binary frequency shift keying (GFSK). Bluetooth radio operates in the unlicensed ISM band at 2.4 GHz. Frequency band is in the range of 2400 to 2483.5 MHz. There are 78 RF channels with bandwidth of 1 MHz. In order to comply with out-of-band regulations in each country, a lower and upper band edge are used with bandwidth of 2 and 3.5 MHz respectively.

## 1.5 Bluetooth Receiver Architectures

For direct conversion receiver architecture, it is best suitable for FSK receivers [1]. However, GFSK has considerable amount of energy at the zero intermediate

frequency (IF). The dc offset and flicker noise will degrade the receiver performance significantly. Particularly, the flicker noise caused by the LO switches from the mixer may be of a magnitude that limits the overall noise figure of the receivers. On the other hand, a superheterodyne receiver maintains the signal at a higher IF. Hence, it does not suffer from the dc offset and flicker noise contributions are much smaller. But superheterodyne receivers require off-chip filters and image rejection. This opposes the goal of the single-chip integration. Moreover, extra current consumption is needed to drive the off-chip low impedance filters. As a result, the most attractive architecture for a Bluetooth receiver is a low IF topology. It allows the receiver having a good sensitivity performance with very low power consumption.

Since Bluetooth technology requires low cost, low power and moderate performance receivers to allow a wide diversity in connecting portable electronic devices, a fully integrated CMOS mixer is desirable to deliver the solution.

# CHAPTER 2

# TYPICAL CMOS MIXER TOPOLOGIES

Other than CMOS transistors, bipolar technologies and Schottky diodes can also be used to construct a mixer. However, CMOS technologies allow high level of integration to gain chip compactness with cost reduction. Hence, it becomes very attractive in many transceiver applications. This section will focus on mixer topologies using CMOS technologies. There are a variety of CMOS mixer topologies proposed. With the brief discussions of different performance metrics in chapter 3, competing architectures can be evaluated more thoroughly. CMOS mixer topologies can be categorized into two main groups: active and passive mixers. The most popular topologies will be introduced in this section. Topologies with their operations will be discussed briefly along with their typical circuit characteristics. Published designs will also be presented along with their possible applications. At the end, a comparison between different mixers will be discussed to conclude this section.

## 2.1 Active Mixers

Active CMOS mixers have the incoming RF voltage signal converted to current domain before mixing occurs. The voltage to current conversion is accomplished with CMOS transistors. Gain is provided because of these active devices. Moreover, active mixers require a lower LO power than their passive counterparts. A reduction in the LO drive is significant in low power integrated circuit design because large LO is difficult to

generate in low supply voltage and a larger LO drive means more power consumption. Different active mixer topologies will still have different performances due to their specific circuit characteristics. Several architectures will be discussed along with their applications.

### 2.1.1 Single-Balanced Mixer

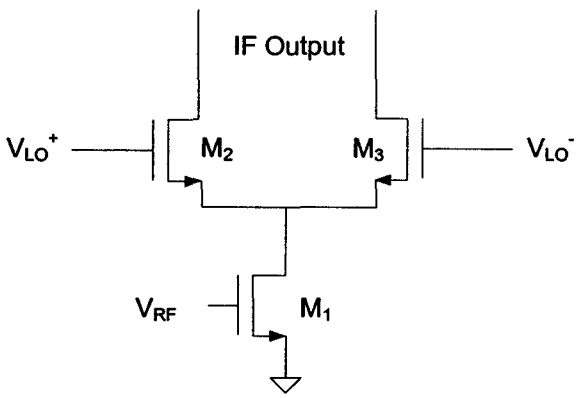


Figure 2.1: A single-balanced mixer (the loads are not shown).

A single-balanced (SB) mixer is shown in figure 2.1. It can be separated into three main stages: transconductance stage, switching core, and load. The transconductance stage consists of only one CMOS transistor in a SB active mixer. Transistor $M_1$ is biased at the saturation region for better conversion gain. Incoming RF voltage signal at the gate is converted to current with gain provided by transistor $M_1$. In typical topologies, the conversion gain of an active mixer is determined heavily by the transconductance of $M_1$ if the LO driven transistors act as good switches. The converted current at $M_1$ will flow through the switching core to the load of SB mixers. In SB mixer,

there is a differential pair of transistors controlled by the differential LO signal. The LO magnitude is normally chosen large enough to increase efficiency of the switches. The switches should operate with a 50% duty cycle for maximum conversion gain. With the LO dc biased at threshold voltage, $M_2$ and $M_3$ should ideally be turned on and off simultaneously, resulting in a perfect square wave function at the switching core. In reality, it is not possible to be realized due to the nonlinear current and parasitic capacitance of $M_2$ and $M_3$. Without the perfect switching, NF, linearity and conversion gain of the active mixer will be degraded. The simplest active mixer will be an unbalanced mixer with only one switch. However this simple topology is not commonly used because of very poor signal isolation. (2.1) shows a simplified voltage output of an unbalanced mixer, assuming the amplifier coverts voltage to current linearly without higher order terms. Moreover $R_L$ represents the resistance of the load, $A_{RF}$ is the input signal strength, and $g_m$ is the transconductance of $M_1$. The LO function can be represented by (2.2), when it behaves as a perfect square wave.

$$V_{IF}(t) = [I_{DC} + g_m A_{RF} \cos\omega_{RF} t] \cdot LO^+(t) \cdot R_L \tag{2.1}$$

where

$$LO^+(t) = \frac{1}{2} + \sum_{n=1}^{\infty} \frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}} \cos(n\omega_{LO} t) \tag{2.2}$$

From (2.1) and (2.2), it can be seen that both undesired RF feedthrough and LO feedthrough will appear at the output because of the dc terms from RF current and LO function. The conversion gain of an ideal unbalanced mixer is shown in (2.3), which is

equal to the multiplication of $\cos(\omega_{RF}t)$ and $\cos(\omega_{LO}t)$ when $n=1$. The extra one half factor at the front in (2.3) is due to the trigonometric principle of multiplying two sinusoidal inputs.

$$G_{uB} = (\frac{1}{2})\frac{R_L(\frac{2g_m A_{RF}}{\pi})}{A_{RF}} = \frac{g_m R_L}{\pi} \tag{2.3}$$

In the SB mixer shown in figure 2.1, RF feedthrough from both $M_2$ and $M_3$ cancel each other. Recalls from (2.1) that the RF feedthrough is due to the multiplication of the LO dc term and RF fundamental term. Also assuming perfect switching, the LO function for the SB mixer can be modeled as (2.4).

$$LO(t) = LO^+ - LO^- = \frac{1}{2} + \sum_{n=1}^{\infty} \frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\cos(n\omega_{LO}t) - \left[\frac{1}{2} - \sum_{n=1}^{\infty} \frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\cos(n\omega_{LO}t)\right] \tag{2.4}$$

$$= 2\cdot\sum_{n=1}^{\infty} \frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\cos(n\omega_{LO}t)$$

The dc term of LO function will be cancelled out at the differential output, while the LO feedthrough is found at the output due to the mixing of LO fundamental with the dc component of RF signal. With this topology, SB mixer has double conversion gain than (2.3) due to the LO function. An alternative design can have the RF and the LO input swapped, it will suppress the LO feedthrough but let the RF signal feed to the output. Active mixers can be loaded with polysilicon resistors or MOS transistors depending on the design specifications. Low voltage low power applications can choose MOS

transistors, while polysilicon load are free of flicker noise. However, the resistive loads limit the mixer current because of voltage drop across them. This will limit the improvement in IIP3 with the fixed supply voltage.

The main drawback of SB mixers are the RF or the LO feedthrough depending on the topology. Good signal isolation is important because it can reduce a significant amount of output filtering. SB mixers are recently found in constructing a distributed mixer for broadband system [2-4]. Several SB mixers are used as a unit cell for building a distributed mixer. It provides wideband conversion gain even at high frequencies (20 GHz - 40 GHz). Artificial transmission lines are incorporated in the distributed mixer to absorb the parasitic capacitances. Different signals through different paths are added in phase at tap points of the circuit to extend the bandwidth. Circuits are designed with 0.18 um CMOS technology. Conversion gain in the range of 1-4 dB at RF signal of 20 GHz is obtained from simulations [2],[3].

### 2.1.2 Double-Balanced Mixer

Double-balanced (DB) mixers have higher signal isolation than SB mixers. Two SB mixers are used to construct a DB mixer with an addition of a current sink as shown in figure 2.2. It is also called a quad or Gilbert mixer. The basic structure of a DB mixer is similar to an SB mixer. However, it converts a differential input voltage to a differential current by transistors $M_2$ and $M_3$. The two SB mixers are connected in antiparallel with respect to the LO signal, but they are in parallel to the RF signal. To make it more clear and self-explanatory about the operation of active DB mixers, current

at each branch are shown as below. Assumptions of perfect square wave switching function and linear voltage to current amplification are still valid.

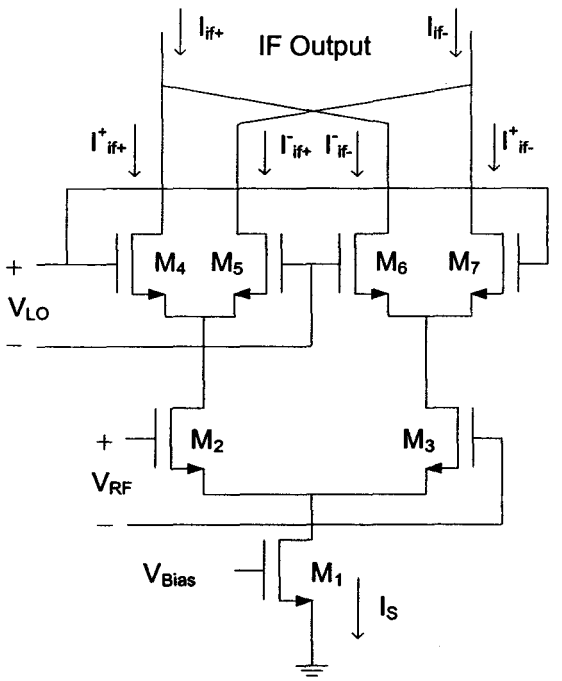


Figure 2.2: A double-balanced mixer (Gilbert mixer).

$$I^{+}_{if^{+}}(t) = \left(\frac{I_{DC}}{2} + \frac{g_m A_{RF}\cos\omega_{RF}t}{2}\right) + \left(I_{DC} + g_m A_{RF}\cos\omega_{RF}t\right)\left[\sum_{n=1}^{\infty}\frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\cos(n\omega_{LO}t)\right] \quad (2.5)$$

$$I^{-}_{if^{-}}(t) = \left(\frac{I_{DC}}{2} - \frac{g_m A_{RF}\cos\omega_{RF}t}{2}\right) - \left(I_{DC} - g_m A_{RF}\cos\omega_{RF}t\right)\left[\sum_{n=1}^{\infty}\frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\cos(n\omega_{LO}t)\right] \quad (2.6)$$

$$I^{-}_{if^{+}}(t) = \left(\frac{I_{DC}}{2} + \frac{g_m A_{RF}\cos\omega_{RF}t}{2}\right) - \left(I_{DC} + g_m A_{RF}\cos\omega_{RF}t\right)\left[\sum_{n=1}^{\infty}\frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\cos(n\omega_{LO}t)\right] \quad (2.7)$$

$$I^{+}_{if^{-}}(t) = \left(\frac{I_{DC}}{2} - \frac{g_m A_{RF}\cos\omega_{RF}t}{2}\right) + \left(I_{DC} - g_m A_{RF}\cos\omega_{RF}t\right)\left[\sum_{n=1}^{\infty}\frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\cos(n\omega_{LO}t)\right] \quad (2.8)$$

$$I^{+}_{if}(t) = I^{+}_{if^{+}} + I^{-}_{if^{-}} = I_{DC} + 2g_m A_{RF}\cos\omega_{RF}t\left[\sum_{n=1}^{\infty}\frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\cos(n\omega_{LO}t)\right] \quad (2.9)$$

$$I^{-}_{if}(t) = I^{-}_{if^{+}} + I^{+}_{if^{-}} = I_{DC} - 2g_m A_{RF}\cos\omega_{RF}t\left[\sum_{n=1}^{\infty}\frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\cos(n\omega_{LO}t)\right] \quad (2.10)$$

Therefore the differential output voltage can be calculated by

$$V_{IF}(t) = R_L \cdot [I^{-}_{if} + I^{+}_{if}] = 4R_L g_m A_{RF}\cos\omega_{RF}t\left[\sum_{n=1}^{\infty}\frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\cos(n\omega_{LO}t)\right] \quad (2.11)$$

This is clear that the LO and the RF feedthrough are cancelled out in active DB mixers. However, due to device mismatch from fabrication, there is always a finite signal feedthrough. In addition, the differential pair of RF transistors also provides a better linearity than their single-ended counterpart. NF, on the other hand, will be degraded since there are more noise sources in the circuit. Even though the output signal is four times the gain of (2.3), it is noted that the gain is double than that of an ideal SB mixer at the expense of doubling the current consumption at the current sink. Moreover, the ideal conversion gain can never be realized because of impossible prefect switching. The

current sink is normally implemented by a large transistor to ensure an almost constant current even with the small fluctuation in drain voltage. For low voltage applications, using no power dissipation LC tanks can eliminate the voltage headroom in the tail current.

The majority of the popular CMOS DB mixer topology is based on the traditional bipolar DB differential modulator introduced by Gilbert [5]. The inherent port-to-port isolation of Gilbert mixer is well suited to integrated circuit design. Moreover, the performance of CMOS technologies could allow a considerable increase in transceiver integration and a reduction in cost. Because of the good RF-IF and LO-IF signal isolation in DB mixer, more output filtering can be eliminated to reduce the front-end size. All of the above characteristics are in favor of the pursuing of single-chip integrated transceiver in today's RF ICs development. Since it is suitable for integrated circuit design, Gilbert cell mixers are widely adopted in mobile PCs, mobile radio, cellular phones, and VHF transceivers for GPS, Bluetooth, CDMA, GSM and DECT wireless communication standards. Typical active CMOS Gilbert mixers [6-10] provide conversion gain in the range of 1-20 dB, SSB NF between 10-16 dB, and IIP3 from –14 to +5 dBm within 4-12 mW power consumption and below 0 dBm LO power supply.

### 2.1.3 Folded Mixer

In the last few years, several new folded designs have been published. It is still based on the Gilbert mixer but with the elimination of one stack of transistors. In a typical Gilbert mixer, there is a load in series with other three transistors that limits the

usable voltage headroom. It makes DB mixer difficult for further development in low voltage application with the downscaling of CMOS technologies. Although [11] published a solution by using LC tank circuits to replace the active loads and current sink transistors for 1.9 GHz application, the on-chip LC tank circuit is very size-consuming and LC tank circuit resonant at high RF frequency is very difficult to fabricate because of the low Q-value of the spiral inductor. Hence, [12-15] show alternate solutions for derived versions of the Gilbert mixer in pursing to maintain the inherent signal isolation characteristics.

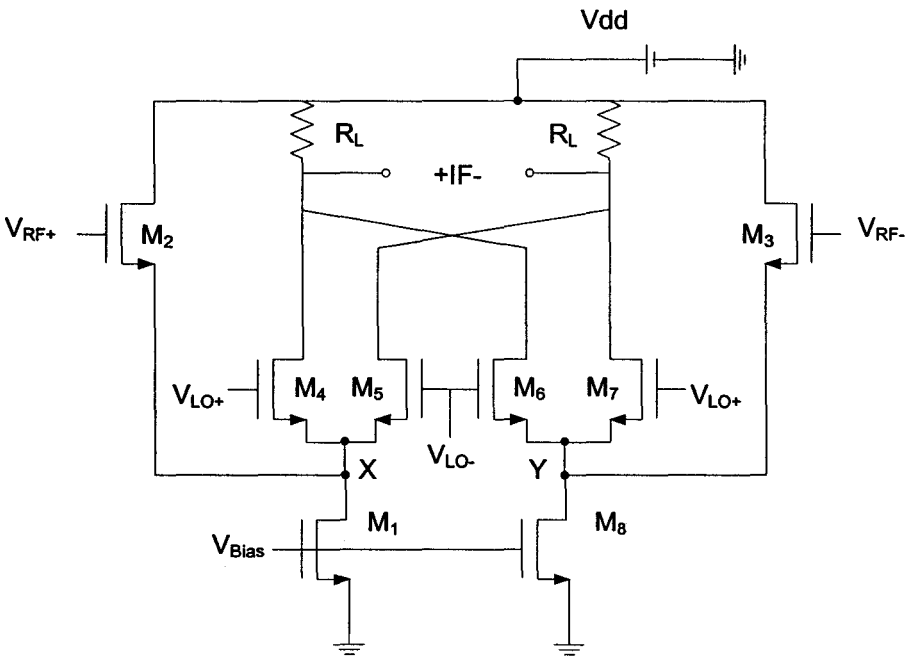


Figure 2.3: A folded Gilbert mixer.

Figure 2.3 shows a typical folded Gilbert mixer. Rather than the common-source input RF stage in a typical DB mixer, two source followers $M_2$ and $M_3$ are used to share the current from the biasing transistors $M_1$ and $M_8$ with the cross-coupling cells $M_4$-$M_7$.

Input signals are injected through the followers into nodes X and Y, and the switching core modulates the input signal according to the LO drive to produce the IF at the output. For this architecture, linearity will be improved significantly because the usable voltage headroom permits the design with a smaller aspect ratio in transconductance transistors. It leads to higher overdrive voltage and helps to increase IIP3. However, both the switching core and RF transistors now share the bias current. A reduction in current through transistors and a reduction in transconductance will degrade both NF and conversion gain under the same current consumption condition as in the case of original Gilbert mixer. It can be seen from [12],[13] that IIP3 is increased to a range of 1-26 dBm with power dissipation within 3-8 mW, whereas NF is increased to above 20 dB with a conversion loss instead of a gain. With the specific performance in NF and conversion loss in the folded design, it does not seem to be a better topology than a typical Gilbert mixer. However, it is a sound architecture for low voltage application in saving one stack of voltage headroom. In order to improve the NF and conversion gain of a folded mixer, [14],[15] have integrated the technique developed in [16] to achieve a folded mixer with 14 dB in NF, 12 dB in conversion voltage, and IIP3 at –3 dBm with a 3.2 mW power dissipation. The mixer is designed and implemented in 0.18 um CMOS technology operating at 2.4 GHz. The technique in [16] is possible in the new folded mixer because of the sufficient voltage headroom in the RF branch by adding a PMOS transistor in series with the NMOS transistor to increase the overall transconductance.

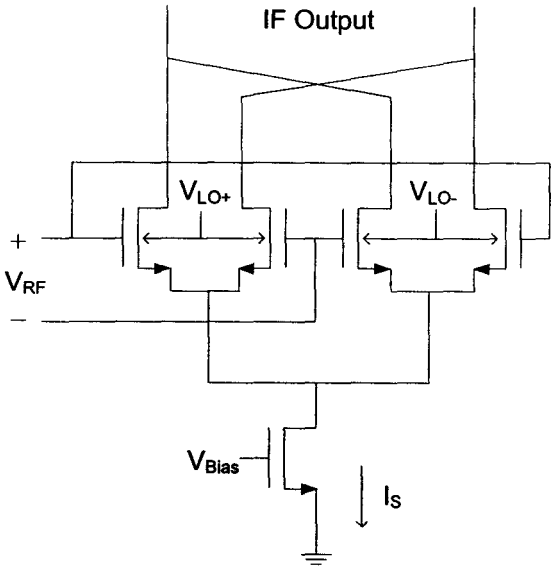


Figure 2.4: A body-injection mixer.

Rather than using a folded topology, [17] fully utilizes the fourth terminal of transistors as the LO input. The RF signal inputs at the gate while the LO drive inputs at the body terminal. This also saves a stack of transistors for low-voltage application. Figure 2.4 shows the proposed topology. In addition, [18] has a similar idea but with the RF and the LO signal swapped. [17] demonstrates a higher gain as the gate-source transconductance is lower than the body-source tranconductance. Both designs have supply voltage at around 1.2 V and power consumption under 2 mW. However, both designs provide DSB NF higher than 17 dB because of the low current consumption. Moreover, the input signal to the body terminal makes the substrate noisier. The preceding LNA with high gain is needed to compensate the high NF.

## 2.2 Passive Mixers

The most fundamental choice in CMOS mixer design is whether to adopt a passive or an active topology. The primary advantage of passive mixers is the increased dynamic range at the expense of a larger LO drive. Passive mixers typically provide conversion loss with transistors operating in the linear region. They demonstrate excellent intermodulation performance with large LO power [19],[20]. However, higher NF, lower conversion gain, and higher LO power consumption are the tradeoffs for excellent IIP3 performance.

### 2.2.1 Subsampling Mixer

Subsampling mixers perform frequency conversion by under-sampling RF signals at a rate that satisfies the Nyquist rate. The sampling rate is at least twice of the IF signal, then the IF signal can be extracted from the RF signal without aliasing [21]. Thus LO frequency (the clock signal for sample and hold mode) is at a sampling rate significantly less than the RF signal. Figure 2.5 shows the circuit implementation of a subsampling mixer.

Subsampling mixers demonstrate excellent linearity when compared to active mixers. They are suitable for direct conversion receivers since the LO signal can be operated at a much lower frequency. Direct conversion receiver can reduce power consumption because IF is moved to dc which saves computation power for signal processing at higher IF. However, NF is very high in subsampling mixer because all noise power within the RF input bandwidth would be aliased to the baseband [21].

Moreover, it also inherits with huge power consumption spent on clock generation. A subsampling mixer in [22] has a performance with 47dB in NF and –16 dB in conversion gain.

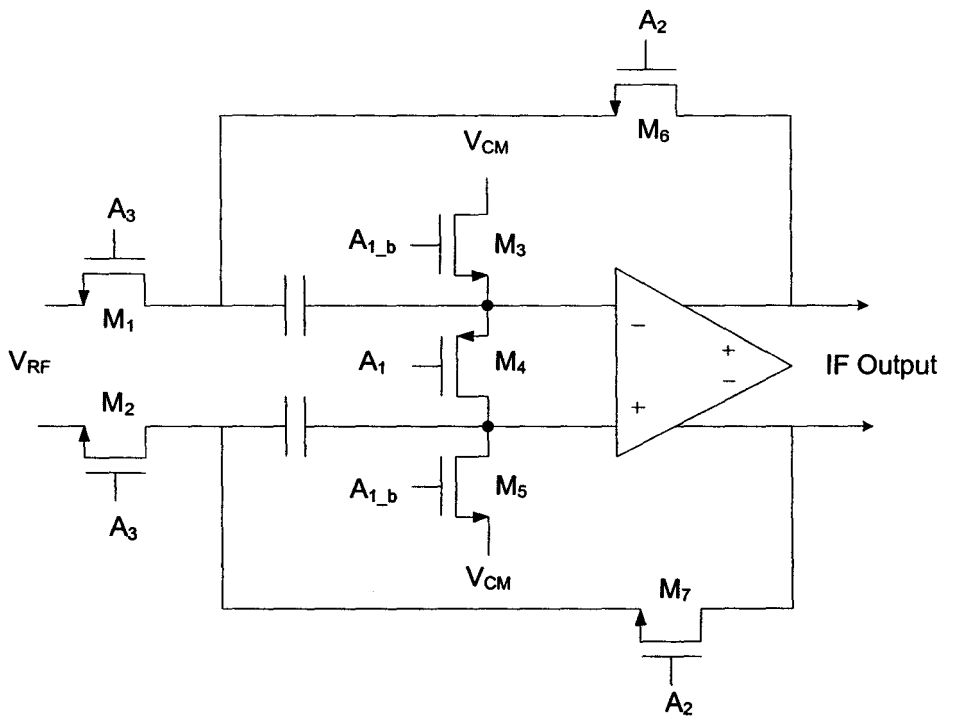


Figure 2.5: A subsampling mixer.

## 2.2.2 Passive Double-Balanced Mixer

A circuit implementation of a passive DB mixer is shown in figure 2.6. The switches $M_1$-$M_4$ are driven by LO signals in antiphase. At any time, only one diagonal pair of transistors is conducting current. Hence, it can be seen that the switches connect either the input or the inverse of the input to the output port. It performs more linearly because the frequency translation is accomplished in the voltage domain. It avoids the distortion during V-I conversion as in active mixers. A fully equivalent description is

that this design multiplies the RF signal in voltage domain by a unity amplitude square wave driven by a large LO signal to ensure fully switching. As a result, the output consists of many mixing products between the odd-harmonics of LO frequency from square wave function of switches with the RF fundamental. The ideal conversion gain is then equal to $(2/\pi)$. A 0.5 factor due to the splitting of IF energy between the difference and the sum components after mixing and a $(4/\pi)$ factor due to the fundamental Fourier coefficient of a unity square wave. It equals to a loss of 3.92 dB even with a perfect square switching function with a large LO drive.

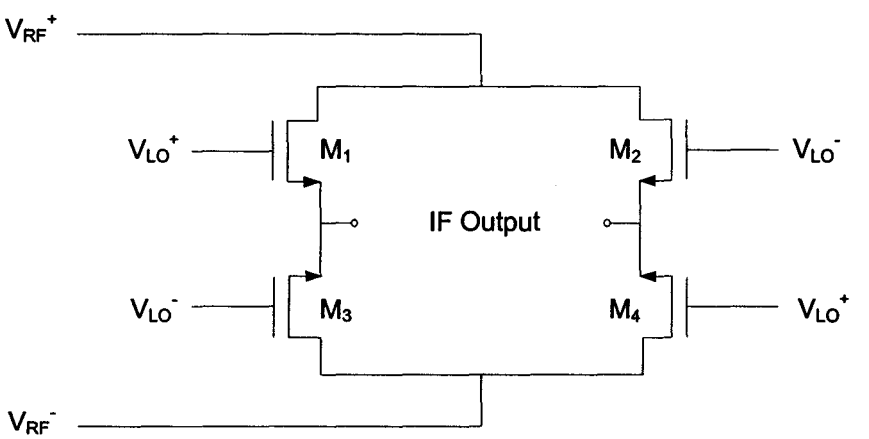


Fig 2.6: Passive double-balanced mixer.

CMOS technology is well suited for passive mixers because of the excellent performance in switching. High performance multipliers based on switching are realized in CMOS transistors almost exclusively. Moreover, it is suitable for extremely low-power application due to the absence of bias current. However, LO needs to provide a

high voltage swing to prevent further penalty in conversion gain. The design in [23] demonstrates a loss of 7 dB and DSB NF of 6.8 dB with IIP3 at 20 dBm.

## 2.3 Comparison of Different Mixer Architectures

Most popular mixer topologies suitable for RF communications have already been discussed. Since each architecture has its own advantages with the specific circuit implementation, there is no particular design regarded as the topology with best performances. First of all, there are many techniques available for each topology to optimize certain performance parameters. In the case of active Gilbert mixers, source inductive degeneration [24] can be used by adding an inductor below the current sink to improve linearity by attenuating high frequency harmonics and intermodulation components at the transconductor. However, downside is the significant increase in chip area consumption. Secondly, there can be modifications for each architecture in order to target for design requirements. Folded mixer is an example to aim for low-voltage application due to the downscaling of CMOS technologies. It also improves linearity by providing sufficient headroom at the RF transistors with the penalty in conversion gain and NF. Nevertheless, active Gilbert mixer is still chosen as the basic structure for this thesis design due to the inherent good RF-IF and LO-IF isolation with higher conversion gain and moderate NF performance.

Among the active and passive mixers that are discussed in previous sections, an active Gilbert mixer is able to provide the highest conversion gain and best signal isolation with moderate NF and low IIP3. However, the typical four stacks of stages on

top of each other have set a limitation on the minimum supply voltage. Active SB mixers also have a similar limitation. An SB mixer has less conversion gain and poor signal isolation with better NF performance than a DB mixer. Moreover, less power is needed to spend on extra transformers to generate differential input signals. In order to pursuit for low voltage applications due to the downscaling of CMOS technologies, a folded design based on the Gilbert mixer has been developed with an additional improvement in linearity. However, lower gain and higher NF is reported when compared with a typical Gilbert mixer. Additional techniques are needed to improve the performances of a mixer. Yet, this design serves as an example for possible improvement in a mixer topology to parallel with the downscaling in CMOS technologies. For an application when extremely high linearity is required, passive DB mixer should be chosen as the basic topology. However, it does not provide gain and NF is normally higher than a Gilbert mixer. In addition, designer has to make sure the LO power is larger enough to drive the switches in passive DB mixer. Typically, an LO power of above 8 mW is needed for almost ideal switching.

In conclusion, designers have to be certain of the design requirements and specifications of the mixer component. There are some basic restrictions that are set by the specific topology. Even with available techniques to improve mixer performances, it is not possible for a Gilbert mixer to have IIP3 at +20 dBm under low voltage application. Even it is possible to provide sufficient LO power, typical passive DB mixer is unavailable to provide a conversion gain. As a result, it is important for mixer designers to be aware of the above issues before choosing a specific architecture.

# CHAPTER 3

# DISCUSSIONS OF CMOS DOWN-COVERSION MIXER

## 3.1 Overview

Mixer is one of the main components in telecommunication devices. It has a nonlinear time varying characteristic that leads to frequency conversion of an input signal in a transceiver. Mixer, frequency converter, performs frequency translation by multiplying two signals and possibly their harmonics. Downconversion mixer, which is the core of this thesis that employed in the front end of a receiver, has two different inputs for frequency conversion. The RF ports are the main input that contains RF signals. Signal is received from an antenna and processed after a Low Noise Amplifier (LNA) stage in receiver architectures. In general, a local oscillator (LO) port provides a periodic sinusoidal wave as the second input signal to the mixer. Due to the circuitry of downconversion mixers, the output signal has an IF equal to the subtraction and addition of RF and LO frequency. The reason why it works as above is generally being overlooked. Since this is the fundamental in mixer theory, the following section will briefly derive the mathematical proof with an aid of a simple circuit. Moreover, section 3.3 will discuss the performance parameters of mixers.

## 3.2 Mixer Fundamentals

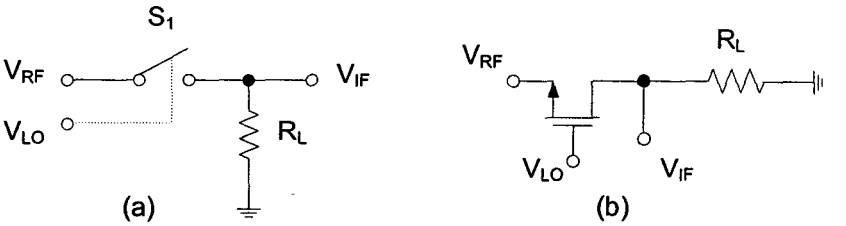


Figure 3.1: (a) Simple circuit to illustrate a mixer, (b) Implementation of the switch using NMOS transistor.

Mixer is a Nonlinear Time Variant (NLTV) circuit when viewed as a whole. However, it can be broken into stages to simplify various kinds of analysis, such as noise analysis using Volterra series in [25]. Mixer is complicated in nature because of the combination of a small signal and a periodic large signal characteristic within the circuitry. In general active mixer topologies, there is a small signal transconductance stage, which converts RF signal from voltage to current, followed by a large signal swing switch controlled by an LO input signal. Mixing is done in the current domain in this design. Figure 3.1(a) is a simplified circuit to illustrate a mixer. The RF port contains a signal that is needed to be downconverted and the LO port is a switch that is controlled by the periodic sinusoidal signal from local oscillator. Hence, the output is zero when it is switched off and the output is equal to RF input when the switch is on. Note that the system is nonlinear because the output is very sensitive to the switch that is only controlled by $V_{LO}$. A NMOS transistor is used to implement the switch in figure 3.1(b). The on-resistance of the transistor contributes noise and as RF input signal varies, the changes in voltage division between the transistor and the resistor introduce nonlinearity

in this system. Moreover, the system is a variant because its output also depends on $V_{RF}$. According to the definition of a variant system, by launching impulses in the same system with different launch times and same observation time, the impulse response observed will be different. In the circuit of figure 3.1, impulse response depends on $V_{RF}$ and it can be zero depending on the launch time of the impulse. As a result of these characteristics, it can be concluded as an NLTV system.

After explaining the basic operation of a mixer in a simplified circuit, it is necessary to understand how a mixer works. Why does the output signal have a frequency subtraction characteristic between RF and LO signal? Why mixer operates by performing the trigonometric principle of multiplying two sinusoidal inputs to give 2(cosA)(cosB) = cos(A+B) + cos(A-B)? Is it the non-linear nature due to the multiplication of the signal that leads to mixing or is it due to other properties inherited from the circuitry? All of these questions cannot be answered before going through a basic mixer circuit with mathematical derivation. Figure 3.1(a) should be the most simplest mixer circuit to serve the purpose. Output $v_{IF}(t)$ can be considered as the product of $v_{RF}(t)$ and a square wave toggling between 1 and 0 controlled by $v_{LO}(t)$. According to Fourier Transform, one rectangular pulse of amplitude 1 with duration $T_{LO}/2$ and period $T_{LO}$ as shown in figure 3.2 can be obtained by evaluating the complex Fourier coefficient $c_n$ with signal described analytically over one period as in (3.1).

$$g_{TLO}(t) = \begin{cases} 1, & -\frac{T_{LO}}{4} \le t \le \frac{T_{LO}}{4} \\ 0, & \textit{for the remainder of the period} \end{cases} \tag{3.1}$$

The complex Fourier coefficient $c_n$ becomes

$$c_n = \frac{2}{T_{LO}} \int_{-\frac{T}{4}}^{\frac{T}{4}} 1 \cdot \exp(-j2\pi n f_{LO} t) dt = \frac{2}{n\pi} \sin\frac{n\pi}{2}$$

To represent the whole periodic rectangular pulses, a summation of all the impulses at different frequencies is needed. This can be accomplished by using the Dirac delta function, as follows:

$$G_{LO}(f) = \sum_{-\infty}^{\infty} \frac{\sin(\frac{n\pi}{2})}{\frac{n\pi}{2}} \delta\left(f - \frac{n}{T_{LO}}\right) \tag{3.2}$$

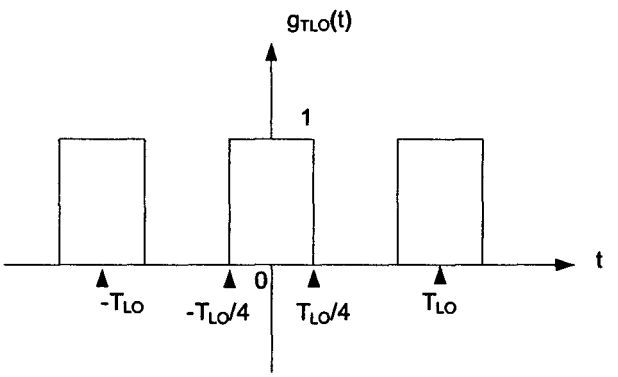


Figure 3.2: Periodic train of rectangular pulses of period $T_{LO}$ and duration $T_{LO}/2$.

The signal $v_{RF}(t)$ in frequency representation is $V_{RF}(f)$. The multiplication in time domain is transformed to convolution in frequency domain according to the multiplication theorem. Thus, output $V_{IF}(f)$ is equal to the convolution of $V_{RF}(f)$ and $G_{LO}(f)$.

$$V_{IF}(f) = V_{RF}(f) * \sum_{-\infty}^{\infty} \frac{\sin(\frac{n\pi}{2})}{\frac{n\pi}{2}} \delta\left(f - \frac{n}{T_{LO}}\right)$$

$$= \sum_{-\infty}^{\infty} \frac{\sin(\frac{n\pi}{2})}{\frac{n\pi}{2}} V_{RF}\left(f - \frac{n}{T_{LO}}\right) \tag{3.3}$$

Hence, (3.3) is the resultant of mixing the described square wave with $v_{RF}(t)$ from the circuit in figure 3.1(a). Note that it is not the $v_{LO}(t)$ that is multiplied with $v_{RF}(t)$. When observing (3.3) closely, it can be seen that many different frequency components are generated due to the $n/T_{LO}$. The output in frequency spectrum will then consist of vertically scaled components of $V_{RF}(f)$ shifted by this $n/T_{LO}$ with respect to the input frequency component, which can also be multiples of RF frequency. Note that there is a dc term of 0.5 when $n$ equals 0, and magnitude of $V_{RF}(f)$ decreases as n increases. And the square wave only consists of odd harmonics as the sin function goes to zero for even $n$. Rather than the multiplication of signals that leads to mixing, it is actually the periodic time varying nature that generates many different frequency components other than the desired IF signal. This is the fundamental of mixer operation.

## 3.3 Performance Parameters

Before discussing different mixer topologies, it is necessary to understand some essential performance parameters for mixer performance evaluation. There are tradeoffs between those parameters when designing mixers. Conversion gain is important to

ensure the overall gain in the receiver system meets the design requirements. Gain is distributed over different frequency bands (RF, IF, baseband) at different stages of receiver architectures. Without desirable gain, signal becomes too weak at the output stage. Moreover, with the downscaling of CMOS technologies, there is also a need for reducing power consumption of the circuitry. It becomes crucial to redesign RF analog circuitries to target for low voltage and low power topologies. Noise is undesired because it corrupts the desired signal; hence there are specifications for noise figure (NF) at each stage of the receiver. In addition, downconversion mixer at the receiver end has a comparably lower IF output signal. Flicker noise is much more severe in analog mixers, other than the noise transferred from multiple frequency bands to the output. On the other hand, linearity is a very important parameter to mixer designers for performance considerations. Due to the complexity of mixer circuitry, not too many publications have been able to illustrate thorough principles or to develop meaningful mathematical methods for intermodulation distortions of mixers. A perfect square wave function is usually assumed when considering the switching core operation in mixers. Distortion contribution in the switching core is usually overlooked.

### 3.3.1 Conversion Gain

Conversion gain of a mixer is defined as the ratio of the desired IF output to the RF input. Passive mixers usually give a gain less than 1, thus a conversion loss rather than a gain. As for active mixers, they normally have conversion gain in excess of unity. Different mixers will be covered more briefly in section 3.4. Conversion gain is usually

evaluated using power ratio (3.4) over voltage ratio (3.5) due to convenience and engineers' preference. The unit would be decibel (dB) for the resultant ratio.

$$Voltage\ gain = 20 \cdot \log\left(\frac{V_{IF}}{V_{RF}}\right) \tag{3.4}$$

$$Power\ gain = 10 \cdot \log\left(\frac{P_{IF}}{P_{RF}}\right) \tag{3.5}$$

A conversion gain greater than unity is often convenient because mixers provide amplification along with the frequency conversion. However, a mixer with a very high conversion gain does not necessary mean a superior design. As a component within the receiver design, it has to be compatible with other stages to integrate as a system that meets design specifications for typical applications. Moreover, providing a very high gain usually sacrificing margins in other performance parameters such as linearity in the design, which can be very undesirable. As a rule of thumb in circuit design, there are always tradeoffs between all performance parameters. Higher conversion gain can usually be achieved by increasing bias current at the transconductance stage or by providing a large LO amplitude for hard-switching; however, both cases lead to higher power consumption. The conversion gain of a mixer is important to ensure the signal will be amplified to the levels well above the noise of the mixer for signal processing at a later stage. The gains for typical active CMOS mixers are around 1 to 20 dB. The LNA preceding mixer is mainly adopted in a receiver to serve this purpose. Hence, if a mixer has superior performances in conversion gain with acceptable NF and linearity performances, the role of LNAs in the receivers will be diminished.

When designing mixer, it is convenient to calculate the conversion gain from (3.4) and (3.5) using circuit simulators or data collected from measurements. However, during the design phase, it would be an unknown before the completion of the circuit. It is extremely difficult to develop a mathematical method for the switching core of mixers. Approximation of conversion gain could be very inaccurate if a perfect square wave is assumed.

### 3.3.2 Power Consumption

Power Consumption in a mixer is the total power dissipated in the circuitry, which is equal to the multiplication of voltage supply and current. For 0.18 um CMOS technologies, normal supply voltage for the chip is 1.8 V. In semiconductor industry, MOSFET dimensions are reduced into the deep submicrometer range because of the increasing demands on speed and circuit complexity per unit of chip area. The lower power consumption is one of the challenging requirements due to the battery lifetime. With downscaling of CMOS technologies, the most severe consequence is a reduction in voltage supply. While CMOS technology scaling is very beneficial to digital circuits, the redesign of RF analog circuits becomes very challenging. Insufficient voltage room can cause many circuit topologies non-functional. And a reduction in this constraint would affect the performance of new circuitries. As a result, research in low-voltage low-power circuit topologies is essential. Moreover, the reduction in supply voltage moves the bias points of MOSFETs from strong inversion to moderate and weak inversion. These become a major concern for low-power and low-voltage mixer designs. On the other

hand, current minimization is another consideration for power reduction. Power consumption is usually assumed as the product of voltage supply and dc current, for convenience again. However, in mixer circuitry, the average current is not necessary equal to dc current. There are always fluctuations in the current around dc bias level. Designers have to approximate the accuracy before using the dc current for calculating power consumptions. Typical power consumptions for newly designed low power CMOS mixers are under 10 milli-watt, moving into the micro-watt region.

### 3.3.3 Noise Figure

Noise Figure is commonly known as the signal to noise ratio (SNR) at the input port divided by the SNR at the output port with unit in dB. However, because of the presence of a large LO signal, linear noise analysis of mixers based on a fixed operating point is not feasible. LO signal is usually large to provide a better switching in the mixer circuitry. It helps providing better conversion gain and less noise contribution [26] in mixer performances. The large LO signal causes substantial change in the operating points of switching transistors over LO cycles. A relatively small numerical error to LO amplitude will then be quite large to other signals in the mixer. Hence, due to the nonlinear time varying operation of mixer circuits, noise behavior cannot be analyzed with conventional circuit techniques. As a result, mixer designers depend on nonlinear noise simulators to obtain NF almost exclusively. In order to develop techniques for noise cancellation [27] and noise reduction, the existence of mathematical models for noise contributions in mixers are very essential for providing design insights. Because of

the periodic time-varying nature of mixers, the output noise varies periodically, even though it is not constant. Due to this nature of cyclostationary [28], a number of techniques developed in [26],[29],[30] are feasible to approximate the NF of mixers. These techniques provide systemic approaches for NF estimation in typical mixer topologies. However, detail discussion of noise analysis in mixers is out of the scope of this thesis.

#### 3.3.3.1 Noise Fundamentals

There are two representations for NF in mixers; they are single-sideband (SSB) and double-sideband (DSB) NF. Other than the desired RF signal, an image signal of above or below LO frequency by an equal amount to the IF will produce an output at the same frequency, the two frequencies are referred as sidebands. In the case when the desired signal appears at only one frequency, SSB NF should be used. If both sidebands contain useful information, DSB should be reported. Since SSB has two sidebands with noise power but only one sideband with signal power, it has half of the SNR comparing to DSB; in other words, SSB NF will normally be 3 dB higher than DSB NF.

Mixers are very noisy comparing to other components within a receiver system. CMOS balanced mixers usually have SSB NF around 10 to 15 dB. It is usually the limiting factor for sensitivity within a communication system. LNA is designed to amplify signal without adding much noise for the ease of the subsequent stage, mixer. LNA has to amplify signal to levels well above the noise of the mixer and the subsequent stages, then the overall NF in the receiver system will be dominated by LNA instead of

the mixer. The role of LNAs in receivers will then be diminished if mixers can be designed with much lower NF. It seems very promising to design less noisy mixers with the possibility of reducing LNAs, considering LNAs are larger in size than mixers because of the inductors within the circuits. It becomes necessary to pinpoint the sources of noise in mixers, from circuit elements, in order to seek for better methods in reducing noise contributions in mixers.

Generally speaking, noise is unwanted fluctuations in electronic circuits. It is known that noise originates from the random motion of carriers in solid-state devices. The collisions among those carriers themselves or between the carrier and the atom of the device leads to continuous changing in speed and direction of the carriers; hence causing the fluctuations in current. On the system level, both inherent noise and interference noise contributions to overall system NF. However, since interference noise is a result of unwanted interactions between different parts of the circuitry, or between the circuit and the outside world, this thesis will only describe fluctuations that are generated by the devices within the mixer circuitry, inherent noise. It should be noticed that in most physical systems, noise signal appears to have an average value of zero in time domain. And it is always analyzed in frequency domain due to its random characteristic with time. Shot, thermal, generation and re-combination, and flicker noise are the most fundamental inherent noise mechanisms. Within a typical CMOS mixer circuitry, which consists of MOS transistors and resistors, the most important noise sources are thermal and flicker noise. Thermal noise, also known as white noise, is often referred to the thermal excitation of charge carriers in conductors. It has a white spectral density, which noise

power is independent of frequency, and is proportional to absolute temperature. Hence, noise power is constant within any given bandwidth at a specific temperature. Thermal noise can be found in all resistors (including MOSFETs) above absolute zero. Ideal inductors and capacitors do not generate thermal noise; however there are always parasitic resistance within inductors and capacitors that lead to thermal noise generation. On the other hand, flicker noise can be found in all active devices when a dc current is flowing. It is due to traps of carriers, which constitute dc current flow, in semiconductors. Since flicker noise is well modelled as having a $1/f^{\partial}$ spectral density, where $\partial$ is around unity, it is often referred as $1/f$ noise. Figure 3.3 shows a typical plot of root spectral density of the drain current noise of a MOS device that has both $1/f$ and white noise. Flicker noise curve intersects with white noise curve at the $1/f$ noise corner. Corner frequency, $f_c$, of the noise corner has values range from several hertz to several megahertz, depending heavily on the size of the MOSFETs. Thermal noise is dominant at high frequency while flicker noise is dominant at low frequency.

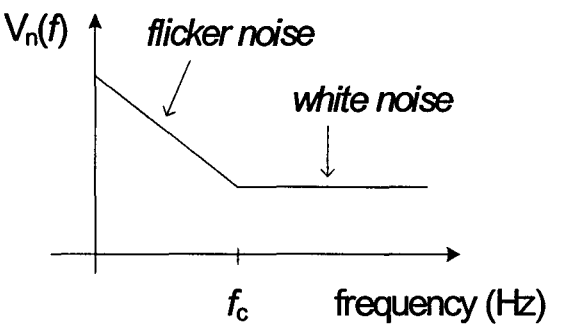


Figure 3.3: Root spectral density plot with both $1/f$ and white noise.

### 3.3.3.2 Noise Generated in Mixers

In typical CMOS active downconversion mixer topologies, there are flicker noise generated from all MOSFETs and thermal noise contributed from resistors and MOSFETs. Analysis of noise contributions in mixers can be confusing since it is very design specific. In addition, recall from the (3.3), derived from a simple mixer circuit in section 3.2, mixer performs frequency conversion due to the mixing of many different input frequencies. Noise at a number of different input frequencies may contribute to output noise after frequency translation to IF.

If the receiver is for direct conversion or low IF applications, flicker noise from mixers may strongly affect the sensitivity. The gate-input referred flicker noise power spectral density of MOS transistors is inversely proportionally to the transistor active gate area as shown in (3.6) [31],

$$S_{1/f}(f) = \frac{KF}{W_{eff} \cdot L_{eff} \cdot C_{OX} \cdot f^{AF}} \tag{3.6}$$

where $AF$ is around 1 and $KF$ are technological parameters (fabrication process dependent), which can be considered as bias independent. Thus as can be seen in (3.6), with continuous downscaling of CMOS technologies, the chip area is getting smaller and flicker noise become dominant in nonlinear noise analysis of mixers with low IF. With modern technologies, the minimum transistor gate-length requirement on RF circuits is decreasing continuously. As a result, the flicker noise component might exceed the white noise up to several megahertz [31]. When using small transistors, the flicker noise corner frequency moves up to several 100 kHz and therefore becomes the dominant noise

component. On the other hand, the power consumption of the LNA is strongly related to the load it drives, which is established by the input impedance of the downconverting mixer. As a result, the mixing transistors have to be kept small to drive less current so as to minimize the power consumption of the front-end design. Because of these factors, the flicker noise generated by these devices becomes more significant and it continues to degrade overall system NF.

Hard-switching mixer that needs a larger LO amplitude will give less flicker noise and thermal noise [31],[32]. The large LO amplitude gives a better switching characteristic, thus it is faster for the transition between ON and OFF stage. Consider a single balanced mixer with LO amplitudes as shown in Fig. 3.4. The output current plot of the mixer is shown beneath the corresponding LO+ drive. $V_x$ is the voltage to turn on the switches while $-V_x$ is the voltage for turning on the other switches in the differential pairs. A larger LO amplitude gives a smaller $T_{ON}$, when the LO voltage is between $V_x$ and $-V_x$. Since switches contribute noise to the output over the time when both switches are ON [32], a mixer with a larger LO amplitude will generate less noise. It is found that lower frequency noise at the gate of the switching transistors appears at the output without frequency translation [32], and flicker noise contributed at the mixer output is mostly originated from switches. On the contrary, in the case of thermal noise contribution, white noise at double harmonics of LO frequency will be downconverted to the IF [32]. In order to reduce noise contributions from the switching core of mixers, a reduction in bias current at the switch may help to reduce white noise generation to the output. In addition, transistor size will have effects on noise contribution. Recall from

(3.6) that smaller transistor size will generate more flicker noise; however transistor size does not have an effect on thermal noise contribution as presented in [32]. Furthermore, p-channel devices are less noisy than their n-channel counterparts since holes are less likely to be trapped. Thus, the mixer designed and fabricated in this thesis has adopted PMOSFETs as the switches to reduce flicker noise contribution. In [33], a passive mixer is designed with no dc current flowing through the switches, thus eliminating $1/f$ noise contribution. For LO signals of moderate amplitude, as required by low power and low voltage application, more flicker noise contribution is expected and a detailed analysis of flicker noise had been presented in [31]. More accurate nonlinear noise (including both thermal and flicker noise) analysis of general mixer has been presented in [29].

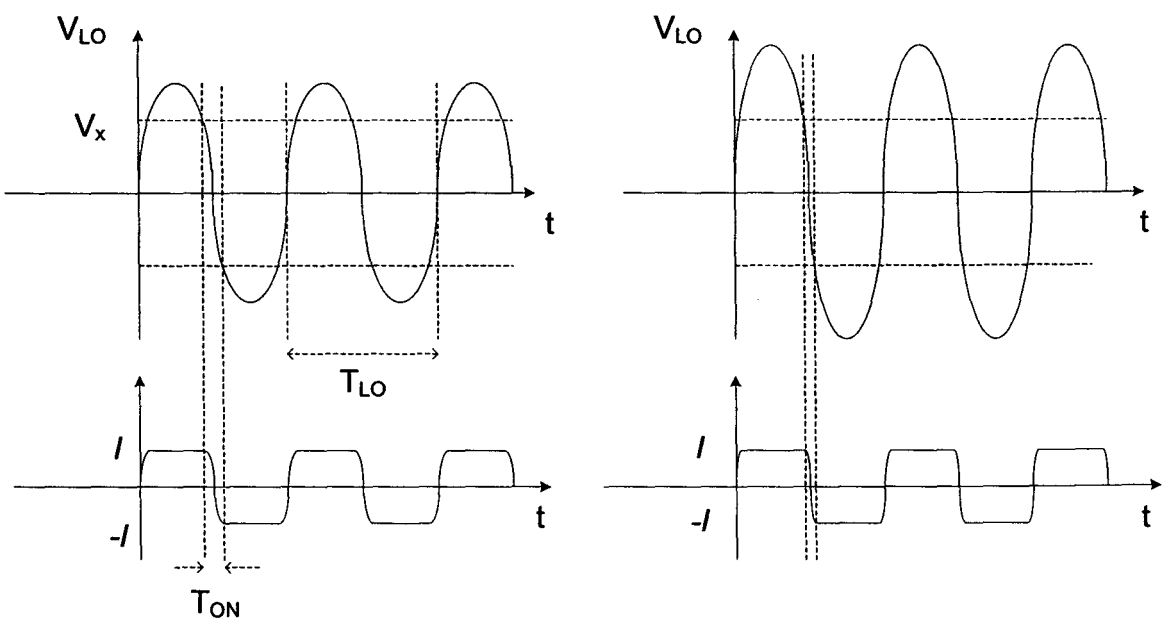


Figure 3.4: Output current characteristics of single-balanced mixer with different LO amplitudes.

Load is another stage that will contribute noise at the output. Using NMOS loads will generate both white and flicker noise with a reduction in voltage headroom in mixer design. PMOS loads maybe a better choice because of less flicker noise contribution. For zero-IF receiver, flicker noise will be a dominant source of noise to the output. Hence, a mixer can be loaded with polysilicon resistors at the expense of some voltage headroom but eliminating flicker noise contribution from the loads.

In CMOS mixer, noise in the transconductance MOSFETs accompanies RF input signals. Flicker noise in these transistors are upconverted to around LO frequency (and to its odd harmonics), while thermal noise at around LO frequency (and its odd harmonics) is downconverted to around IF [32]. If output lies at zero-IF, then the transconductance transistors only contribute thermal noise after frequency conversion, since IF output is much lower than LO frequency. However, due to mismatches in switching transistors during fabrication, some amount of flicker noise in the transconductance transistors may appear at the output. In [26], it shows that 81% of thermal noise contributions from the transconductance transistors are originated from white noise downconverted from $f_{LO} \pm f_{IF}$, while 9% is from white noise at $3f_{LO} \pm f_{IF}$.

In conclusion, thermal noise contribution is usually dominant at transconductance stage and mainly from white noise around LO frequency, while flicker noise could be significant at the switch if LO amplitude is not large enough to provide a fast perfect switching. A smaller LO drive also generates more thermal noise at the switch, where white noise at around even multiples of LO frequency will be translated to the output IF. Moreover, choosing polysilicon resistors as loads can further reduce flicker noise in

mixers. Total noise contributions to the output can then be calculated with all the individual noise sources identified. However, since it is very time-consuming and challenging to be applied in a straightforward manner to evaluate NF of mixers analytically or numerically, designers are most likely dependent on simulation tools to obtain NF of mixers before product fabrication, if focus of the design is not for NF minimization.

### 3.3.4 Linearity

Most of the active double-balanced mixers utilized in wireless receivers are based on the Gilbert mixer topology. In general, mixers nonlinearities are contributed from the transconductor and the switching core. Good downconversion mixers are required to provide high linearity, low NF, and good conversion gain. This simultaneous achievement on all of the performance parameters is very difficult for mixer designers. High linearity in mixers becomes even more challenging for the low power dissipation and low supply voltage applications. In order to reduce considerable amount of power consumption in typical Gilbert mixers, both the supply voltage of the circuitry and the bias current at the transconductance stage have to be reduced significantly. With the reduction in voltage headroom at the transconductance transistors, linearity is worsened. As a result, a good linearity performance in the active mixers is difficult to achieve with the limited power consumption constraint.

Mixers linearity limits the dynamic range of the corresponding communication system. The floor of dynamic range is set by the NF, which conveys to how weak a

signal can be processed. On the other hand, the ceiling is established by the onset of severe nonlinearites that accompany the input signals [34]. In RF communication systems, linearity is commonly characterized by the 1-dB compression point and the third-order intermodulation intercept point (IIP3). As the interference level due to nonlinearity tends to intensify for RF applications, circuit linearity is of great importance. Nonlinearity is usually caused by intermodulation among undesired signals from the system. In other words, interferences outside channel frequency can be translated onto the frequency of interest under frequency translation. Since these interferences behave like noise, nonlinearities will degrade the SNR at the output. IIP3 is commonly used to indicate the linearity of a circuit with respect to its third-order intermodulation distortion (IMD3). A higher IIP3 mixer means it generates smaller IMD3 and thus more linear. Alternatively, the compression point is also a measure of dynamic range ceiling. It is the point when the output power of mixer begins to depart from the linear dependence on the RF input power. A higher compression point means the mixer perform more linearly at stronger received signals.

### 3.3.4.1 Gain Compression

In reality, mixer has limits beyond which the output power has a linear dependence on the RF input power. As RF signals strength increases at the gate of the transconductance transistor, the output power of mixer begins to saturate and the curve shown in figure 3.5 starts to depart from the ideal linear curve represented in dotted line.

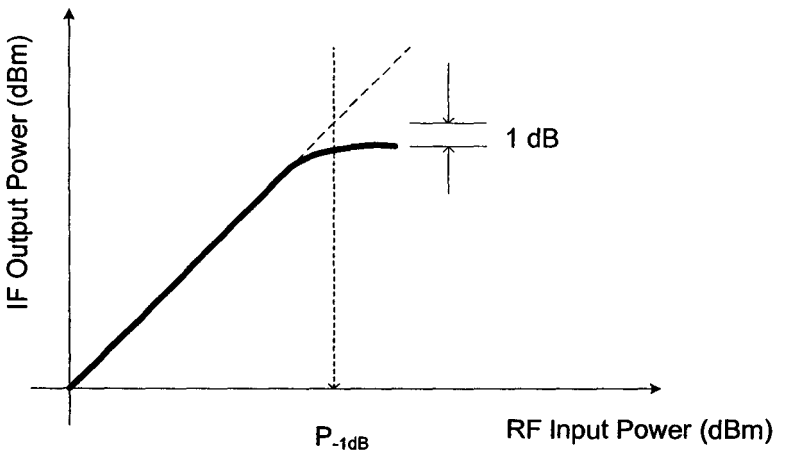


Figure 3.5: Definition of mixer 1-dB compression point.

Since subtraction of input power from output power gives conversion gain at corresponding RF power, gain is compressed and starting to reduced with increasing input power after compression point, as output power is saturated. The 1 dB compression point of mixers is a measurement of the input power level, in dBm, when the output power deviates the ideal linear curve by 1 dB. In other words, the linear small signal gain is dropped by 1 dB at this input level. With further reduction in voltage headroom and bias current due to design specifications, mixers will behave even more nonlinear. Although gain compression point gives an upper limit of the strength of received signals at corresponding RF frequency, it gives no insights of the contribution of nonlinearities from different intermodulation distortion components. Simulation tools such as Cadence SpectreRF® can give a relatively fast result for 1-dB compression point. Normally, simulation for IIP3 takes much longer time than 1-dB compression point simulation.

Hence, it gives a rough idea about the mixer linearity for designers if IIP3 simulation is too time consuming and computationally expensive.

### 3.3.4.2 Harmonics and Intermodulation Distortions

The primary effect of nonlinearities in mixers is that they will corrupt the desired signal by frequency translating interferences at various frequency components onto the frequency bandwidth of interest. Due to these nonlinearities, distortions are generated. There are commonly two types of distortion dues to nonlinearities, i.e. harmonic and intermodulation distortions. Harmonic distortion is generally not a main concern. Since interferences occur at frequencies further away from frequency of interest, they can be easily filtered out along the receiver chain. However, due to intermodulation distortions, some interferers will be translated to the vicinity of output frequency and the output signal will be corrupted.

In linearity analysis the process can quickly become very complex and intractable with higher order nonlinearities. And in radio communication, nonlinearities up to the third order are of most significant. Hence, a system with nonlinearities up to the third order will be discussed and a memoryless system is assumed for simplicity. (3.7) describes the input-output characteristics of a system with an output signal y(t), an input signal s(t), and memoryless nonlinearities up to the third order.

$$y(t) = a_1 s(t) + a_2 s^2(t) + a_3 s^3(t) \tag{3.7}$$

When a single tone signal is input into the system, where $s(t) = A\cos(\omega_1 t)$. Using (3.7), the output of this nonlinear system becomes,

$$y(t) = \frac{a_2 A^2}{2} + \left( a_1 A + \frac{3a_3 A^3}{4} \right) \cos\omega_1 t + \frac{a_2 A^2}{2} \cos 2\omega_1 t + \frac{a_3 A^3}{4} \cos 3\omega_1 t \qquad (3.8)$$

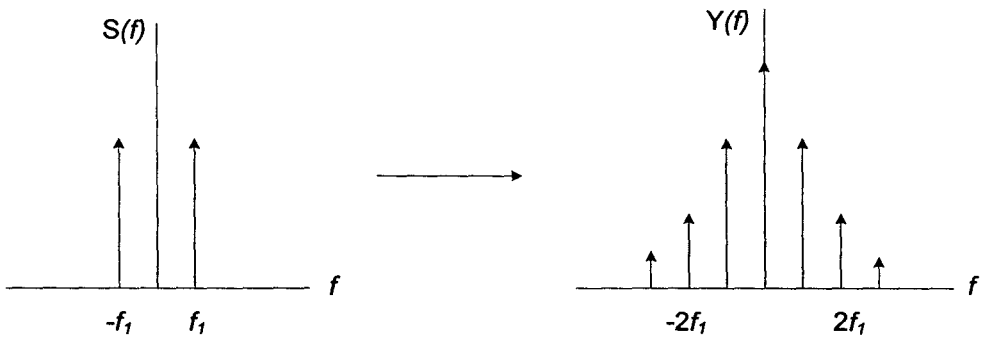


Figure 3.6: Frequency spectra of one tone input and output signal of a nonlinear system

It can be easily seen that after Fourier transform, the output consists of vertically scaled frequency components at dc, fundamental, and harmonics of input frequency. Harmonic distortion is defined as the ratio of the amplitude of a particular harmonic to the amplitude of the fundamental. Figure 3.6 shows the frequency spectra of the one-tone input signal and the corresponding output for the described nonlinear system to (3.7). Harmonic distortions in mixer are generally not a main concern. They can be filtered out easily, since the IF output is very distant from the difference between LO frequency and harmonics of input RF frequency. However, for zero-IF architecture, the dc component may post a threat to corrupt the output signal. One useful ratio would be the third-order harmonic distortion ($HD_3$), which will establish a relationship with IMD3 later. Refer back to (3.8), since $(a_1 A >> 3a_3 A^3 / 4)$, the ratio of coefficient of the third harmonic to the fundamental becomes,

$$HD_3 = \frac{a_3 A^2}{4a_1} \tag{3.8}$$

Intermodulation distortions, on the other hand, occur when more than one-tone are applied to the input. It is defined as the ratio of the amplitude of a particular intermodulation product to the amplitude of the fundamental. Two-tone input signals are commonly used to demonstrate and analyze this distortion. Assume two strong signals, $s(t) = A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t)$, is presented at the input of a mixer circuitry. Substitute $s(t)$ into (3.7), we will get the coefficients at dc, fundamentals, different harmonics, and intermodulation products. Using a Bluetooth downconversion mixer as an example, input signals with LO frequency at 2.3 GHz, and $f_1$ and $f_2$ at 100 and 101 MHz respectively are applied to the mixer. Hence the two signals feeding into the input of the mixer are $\omega_1 = 2\pi(f_1+f_{LO})$ and $\omega_2 = 2\pi(f_2+f_{LO})$. In other words, this mixer has a desired received signal at 2.4 GHz for Bluetooth wireless application and an interferer at 2.401 GHz. An adjacent bandwidth of 1 MHz is chosen since RF channel band for Bluetooth is 1 MHz in width. After mixing with the LO signal, all harmonics and most intermodulation products are located much farther away from desired frequency and can be filtered out. However, the frequency that are causing threats are $2f_1-f_2$ = 99 MHz and $2f_2-f_1$ = 102 MHz in particular. Since output signal at $f_1$ = 100 MHz is very close to these two third-order intermodulation (IM3) products, filtering after mixer stage is not possible to attenuate the interference. As a result, the output signal is corrupted. Both SNR and IIP3 degrade due to these IMD3. A graphical representation of this process is shown in figure 3.7. It should be noted that after RF signals passing through an active mixer, the

output at $f_1$ is amplified because of conversion gain. In the two-tone test in mixer, the interferer signal is applied with the same amplitude as the RF input. IMD3 will be amplified along with RF input signals. Designers have to make sure that linearity requirement is met when trying to boost the conversion gain of the mixers. Referring back to (3.7) with two-tone input *s(t)*. The amplitude for both $2f_1$-$f_2$ and $f_2$-$f_1$ are equal to $(3a_3A^3/4)$, while the amplitude for their fundamentals are equal to $a_1A$. As a result, IMD3 for both IM3 components for this nonlinear system as defined in (3.7) will be equal to

$$IMD_3 = \frac{3a_3A^2}{4a_1} \tag{3.9}$$

And by comparing (3.8) and (3.9), the following relationship can been found from this memoryless nonlinear system.

$$IMD3 = 3HD_3 \tag{3.10}$$

However, equation (3.10) is valid only if it is a memoryless nonlinear system or if it is within a block of the system that is memoryless. For a memory circuit such as low pass filter, more attenuation will be on higher frequency components. Because of the non-constant frequency response, (3.10) is not valid anymore because $HD_3$ is located at much higher frequency. Since mixers at the front-end generally receive RF signal at high frequency, nonlinear capacitance in transistors will introduce memory effects on mixers. Hence, Volterra series, which includes memory effect, is commonly used to analyze the nonlinearity effect on mixers.

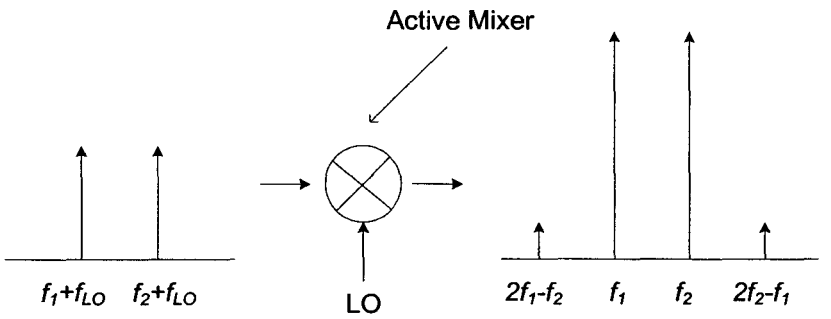


Figure 3.7: Demonstration of intermodulation distortions in active downconversion mixers.

### 3.3.4.2.1 Third-Order Intermodulation Intercept Point

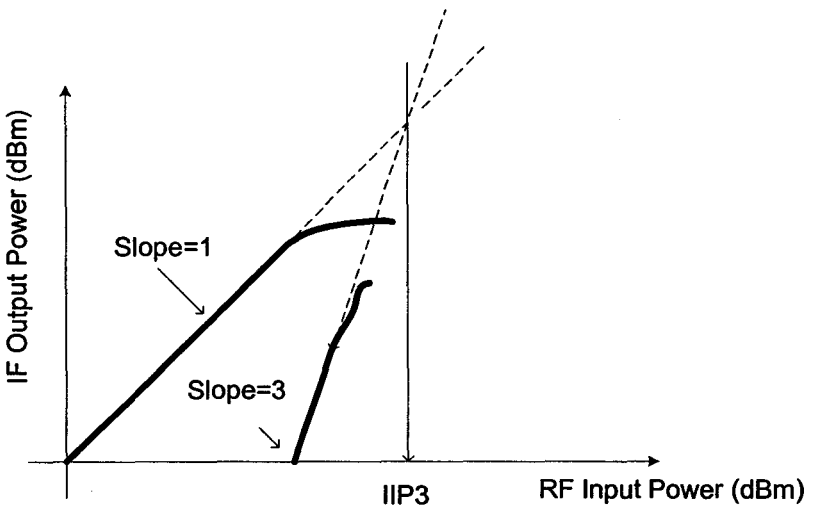


Figure 3.8: Definition of mixer third-order intermodulation intercept point (IIP3).

IIP3 is used as one of the main indicator for mixer linearity. From figure 3.8, there are two output curves represented in logarithmic scale in power level, corresponding to RF input power. Referring back to the simple nonlinear memoryless system in (3.7), as input amplitude $A$ increases, the desired output (the fundamental) also

increases proportional to A with the multiplication of gain $a_1$. As a result, this curve has a slope of unity before gain compression due to nonlinearities and saturation of active device. On the other hand, IMD3 components increase with a third order, $(3a_3A^3/4)$, proportion to the input signal. Thus it has a general slope of 3 in this graph. IIP3 is defined as the input level when the two lines intersect with each other. The higher the IIP3, the more linear the mixer is.

#### 3.3.4.2.2 Active Mixer Third-Order Intermodulation Distortions

The intermodulation analysis in diode mixers has been available since the late 1980s. But only few works have been published on the IMD3 analysis of active CMOS mixers, except for the case of resistive mixers, which are passive mixers with analysis method almost identical to diode mixers. Active mixers are complex for analysis due to the unpredictable switching function for current characteristic from the switching core, which is difficult to model in an accurate and a straightforward manner. Moreover, there are large LO and small RF signals within mixers. In [35], intermodulation distortions from small signal RF input is predicted by the Volterra series. Harmonic balance technique is used to analyze distortions from LO signal, since Volterra series is limited to small excitations and not suitable for the large signal input from the LO in mixers [35]. Comparisons between harmonic balance technique and Volterra series can be found in [36]. Due to less computation cost from the elimination of Fourier transforms and because of the efficiency in analyzing multiple inputs, Volterra series is more preferable

for IMD3 analysis in active mixers. However, for the IMD3 analysis in the switching core, approximations are required [37] and mixer is modeled as periodically time-varying weakly nonlinear (PTVWN) system.

After the discussion of the nonlinear memoryless system in the previous section, the generation of intermodulation distortions should be comprehensible. However, memoryless system is not practical in analyzing nonlineariy in mixer circuitry. Due to the parasitic capacitance in MOS transistors at the transconductance stage, memoryless system is not adequate to describe mixer circuitry and it is not correct for the calculation of IMD3 in high frequency mixers utilized in the front-end receiver. One alternative is to use a complete Volterra series analysis, which includes memory effect, to predict IMD3 at the transconductance stage in mixers. [25] shows that high frequency effect in circuits can easily degrade the distortion performance by around 100% more than estimation using low-frequency analysis with simplified memoryless system. Volterra series analysis is done from [25] with figure 3.9 redrawn from [25]. A source-coupled pair (SCP) as shown in figure 3.9 is commonly implemented as the transconductance stage of active mixers. Parasitic capacitance is included in the analysis, since downconversion mixer operates at high frequency, which enhances the nonlinearity effect. The MOS transistor that is used to implement current sink is usually much larger in size, hence its drain to bulk capacitance is dominant. In parallel with source to bulk capacitance from $M_1$ and $M_2$, $C_d$ denotes the total capacitance. Nonlinearity distortions, arise from the V-I converter at the transconductance stage of active mixers, are because of the square law

drain current characteristic of MOS transistors at saturation. Detailed hand calculation is carried out in [25] with IMD3 predicted as shown in (3.11).

$$IMD3 = \frac{3A^2}{32\left(V_{GS} - V_{TH}\right)^2}\left[\left|1 - \frac{1}{3}\frac{j(\omega_1)C_d}{K_n(V_{GS} - V_{TH})}\right|\right] \tag{3.11}$$

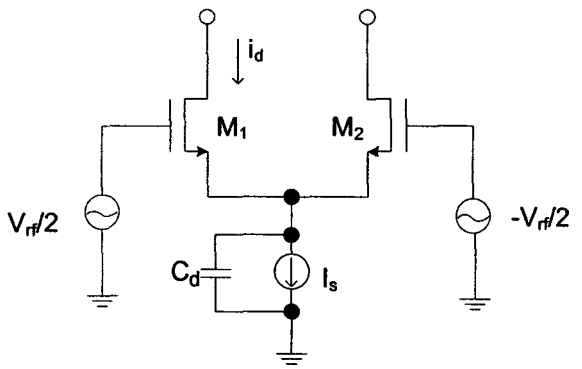


Figure 3.9: The transconductance stage (SCP) of Gilbert mixer with parasitic capacitance [25].

It shows from (3.11) that IMD3 increases with increasing operating frequency $\omega_1$. And increasing the gate overdrive voltage ($V_{GS}$-$V_{TH}$) will help reducing IMD3 generated at the transconductance transistors. Both agree with [37]. Moreover, IMD3 decreases with increasing $K_n$ from (3.11), which agrees with [38] by increasing transistors aspect ratio for better linearity performance. Increasing in capacitance $C_d$ will also increase IMD3. Knowing that it is complex and time consuming to develop mathematical methods for IMD3 in mixers, most designers depend heavily on simulation tools to obtain distortion levels at the output. Although most simulation tools provide good accuracy that is limited by the detailed models they employ, only telling the IIP3 or IMD3 does not provide any insights regarding the relationships between design parameters and circuit

linearity. Thus it is insufficient to provide detailed information of how the mixer linearity can be improved.

Although [25] has a complete hand calculation on IMD3 analysis using Volterra series at the transconductance stage, there is no work published regarding the close form solution for the switching core of active mixer, except some models developed for higher accuracy and more efficient algorithms in computer simulations for IMD3 estimation in mixer switching core in [37],[39]. A prefect switch with prefect square wave function is always assumed for IMD3 analysis [24]. However, due to the characteristics of MOS transistors, the switching function of current characteristic in time domain will be controlled by the gate and the source voltage. Moreover, the switching transistors operate in weak, moderate and strong inversion with difficult corresponding current characteristics. This nonlinear drain current will introduce intermodulation distortions and the phenomena will be accentuated by the *Cgs* at high frequency operation. As a result, a perfect square function with only ON or OFF state is not possible to be realized at the switching core. Furthermore, it was shown from [37],[39] that IMD3 from the switching core could be a dominant contributor. Simply assuming a perfect switch without detailed linearity analysis at the switching core will underestimate the IMD3 in active mixers. Since a square wave consists of only odd harmonics of the fundamental in frequency domain, no new IMD3 will be generated near the output IF with this assumption at the switching core. Other than the expected $\omega_1 = 2\pi(2f_1-f_2-f_{LO})$ or $\omega_1 = 2\pi(2f_2-f_1-f_{LO})$ which interacts with the fundamental of LO frequency, other distortions with the interaction of higher harmonics will not be introduced around IF. Hence, a filter

after mixer stage at the front-end can easily filter them out. With the nonlinear I-V characteristics and the parasitic capacitance inherited at the switching transistors, the switching function will have unknown frequency components to generate new distortions around IF. From [39], IMD3 is predicted for individual transistor within a double-balanced active mixer. It shows that IMD3 from switching transistors are more significant than that from the transconductance transistors. And [37] further demonstrates that IMD3 from switching transistors of a single-balanced active mixer, operating at high frequency, depends on the magnitude of the LO swing and the drain current through them. Results show that IMD3 from a switching pair in the tested single-balanced mixer dominant IMD3 from the transconductor within the chosen ranges of LO swing and bias current. And there is an optimal point for comparatively high current or high LO voltage swing. However, it is not feasible to have a mixer operating at high bias current due to the power consumption constraint. Moreover, a large voltage swing from the LO is also limited by the system specifications due to higher power consumption at the LO. It is noted that as the LO voltage swing increases at fixed current bias, IMD3 improves up to an optimal value after which the IMD3 is worsen. A higher LO voltage means higher gate voltage at the switching transistors. In all NMOS typologies, since the source voltage is also determined by the drain node of the transconductance transistor, the relatively small fluctuation in source voltage is almost neglectable. Because it exceeds the threshold voltage earlier in the beginning of switching cycle, a larger gate voltage swing will ensure the switches to be turned ON or OFF in a shorter time. It is also illustrated in figure 3.4 that a higher LO swing gives a steeper curve characteristic within

the same LO period. The LO dc bias is not shown in figure 3.4. As a result, the increase in gate overdrive voltage will ensure the switches to turn ON or OFF more efficiently. However, since the drain to source voltage ($V_{DS}$) across the transistors are set by the voltage headroom under the supply voltage, a relatively large increment in the LO drive will force the transistor to operate in linear region or strong inversion mode for a longer time within the ON period of the switches. Even though the switch performs more efficiently with a larger LO swing, further increase in magnitude after an optimal point will degrade the mixer linearity. With a higher voltage swing at the common-source node, a higher current is injected by the Cgs that accentuates the high frequency characteristics and further increases IMD3 [37].

Although only models are developed for more accurate prediction of IMD3 from the switching core, it has dominant effect on IMD3 contribution [37],[39]. (3.11) can be considered analogous due to the same source of linearity distortion from the nonlinear current characteristics. An increase in overdrive voltage up to an optimal point will improve IMD3 and a smaller parasitic capacitance will reduce IMD3 as well. In addition, the switching function should also have a great impact on the mixer linearity. The main design idea for this thesis is to bias the fourth terminal of a single gate MOS transistor at the switching core. While this body terminal is normally grounded for active mixers, different ways are tried to bias the body terminal to modify the body effect. The first obvious improvement will be the changing in threshold values, which helps switching the transistors ON and OFF more efficiently. With typical active mixers, the simple method in achieving better switching is to supply a larger LO drive. However, it may not be

feasible since the magnitude is always limited by the power consumption of the LO. As discussed previously, it will increase IMD3 to the mixer output with sufficient high LO swing. On the other hand, the attempt in changing threshold voltages can also ensure the fast switching of the mixer. This is feasible to achieve the same switching characteristic with a reduction in the LO drive by modifying the body effect. Thus, it provides a mean to maintain a feasible design method of active mixers for lower power consumption at the front-end while achieving better linearity, noise and gain performance, which are products of better switching. As a result, it should be very desirable for low voltage low power application. A detailed analysis with simulation results will be presented in chapter 4.

### 3.3.4.2.3 Mixer Second-Order Intermodulation Distortions

Other than IMD3, second-order intermodulation distortion (IMD2) analysis is also important for direct conversion or low-IF receiver architectures. If two strong interferers are located at $f_1$ and $f_2$ close to the channel of interest, they will generate a low frequency IMD2 component at frequency $f_1 - f_2$, because of even order distortions along the communication channel. Due to the LO suppression at the output, downconversion mixers usually utilize double-balanced topologies, which generate a small amount of even order distortions. In reality, finite second-order intermodulation intercept point (IIP2) is resulted from the finite feedthrough from RF input to IF output [40]. The mixer IIP2 is determined by the mixer mismatches, offsets, and second-order non-linearity [41]. As a result, the most possible way to maximize the achievable mixer IIP2 is to minimize

the generation of mixer IMD2, since offsets and device matching cannot be improved beyond certain limits. In general, it is the downconversion mixer that determines the achievable IIP2 of the entire receiver [42].

## 3.4 Improvements on major parameters with better switching efficiency

The focus of this thesis is to study the effects on mixer performances by improving the switching efficiency of the LO switches. By modifying the threshold voltage, a more perfect square wave switching function can be obtained at the switching core of an active mixer. This section will present the theoretical improvements on major performance parameters with modified threshold voltages at the LO transistors.

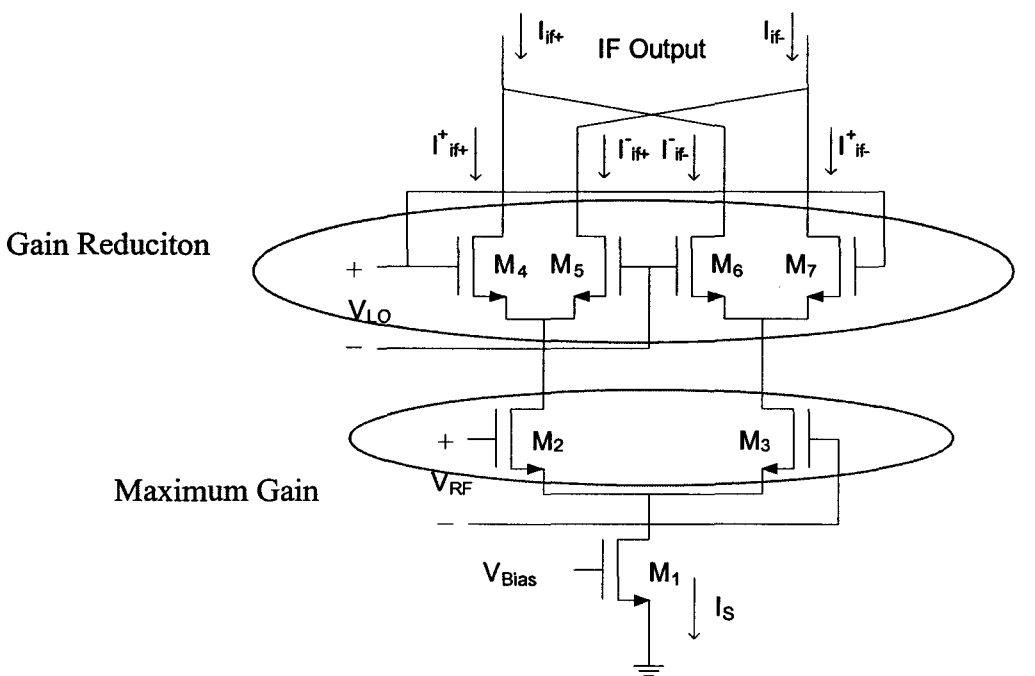


Figure 3.10: A Gilbert mixer showing different effects on conversion gain.

From an active Gilbert cell mixer, the maximum gain is set by the transconductance of $M_2$ and $M_3$. Recalls from (2.1) and (2.4), the ideal gain for a SB active mixer is equal to (3.12) when the LO transistors are working as perfect switches.

$$Voltage\ Gain = (\frac{1}{2})\frac{2R_L(\frac{2g_m A_{RF}}{\pi})}{A_{RF}} = \frac{2g_m R_L}{\pi} \tag{3.12}$$

However, switches $M_4$ to $M_7$ have finite rise time and fall time when conducting current. It contributes to the $T_{ON}$ as shown in figure 3.4 and it introduces gain reduction to (3.12). The $2/\pi$ term is the gain penalty from a perfect square switching function. In order to predict a more realistic gain reduction due to the finite rise time and fall time of the switches, and in order to study the effects of different switching functions on the gain penalty in mixer conversion gain, Fourier transform analysis is performed on a trapezium waveform as shown in figure 3.11.

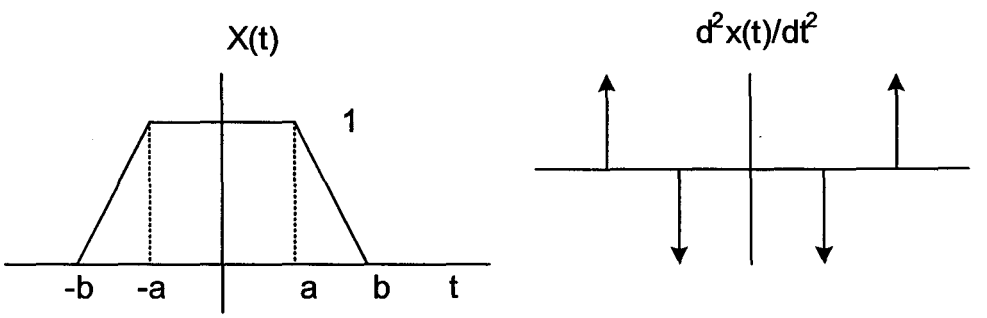


Figure 3.11: A trapezium switching function with its second derivatives.

To ease the calculation of the Fourier transform of the trapezium waveform, its second derivatives are used. The impulses can then be represented as in (3.13). The Fourier

transform of the trapezium switching function can then be obtained by dividing the Fourier transform of (3.13) by $(\pi nf)^2$. (3.14) is the frequency representation of a trapezium switching function with $K$ equals to $1/b\text{-}a$.

$$\frac{d^2x(t)}{dt^2} = K[\delta(t+b) - \delta(t+a) + \delta(t-b) - \delta(t-a)] \tag{3.13}$$

$$X(f) = K\left[b^2 \frac{\sin^2 \pi nfb}{(\pi nfb)^2} - a^2 \frac{\sin^2 \pi nfa}{(\pi nfa)^2}\right] \tag{3.14}$$

In ideal switching function with $a=b$, a square wave is obtained. And for ineffective switching, the function will have $a$ close to zero. When plotting (3.14) with Matlab, it can be seen that when $a=0$, most energy concentrates at dc. And when $a$ is increasing from zero to $b$, more energy is distributed to the side-lobes. From mathematical point of view, it means that when $a=0$, the LO switching function can be expressed as (3.15) with $f=f_{LO}$ and $b=T_{LO}/4$. While with the ideal square wave, switching function of an SB mixer is represented by (3,16). The conversion gain can be evaluated by finding the coefficient of $\cos(\omega_{LO}t)$ when $n=1$, since this is the signal that mixes with $\cos(\omega_{RF}t)$ to perform the frequency conversion.

$$LO(t) = 2 \cdot \sum_{n=1}^{\infty} \left[\frac{1}{2} \frac{\sin\frac{n\pi}{4}}{\frac{n\pi}{4}}\right]^2 \cos(n\omega_{LO}t) \tag{3.15}$$

$$LO(t) = 2 \cdot \sum_{n=1}^{\infty} \left[\frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}}\right] \cos(n\omega_{LO}t) \tag{3.16}$$

As a result, it shows that there is more gain reduction in (3.15) than in (3.16). Hence, conversion gain can be improved with a more effective switching at the LO transistors, when the switching function is closer to a perfect square wave with shorter rise time and fall time. Gain penalty decreases with a smaller $T_{ON}$, which can be achieved by the substrate biasing techniques.

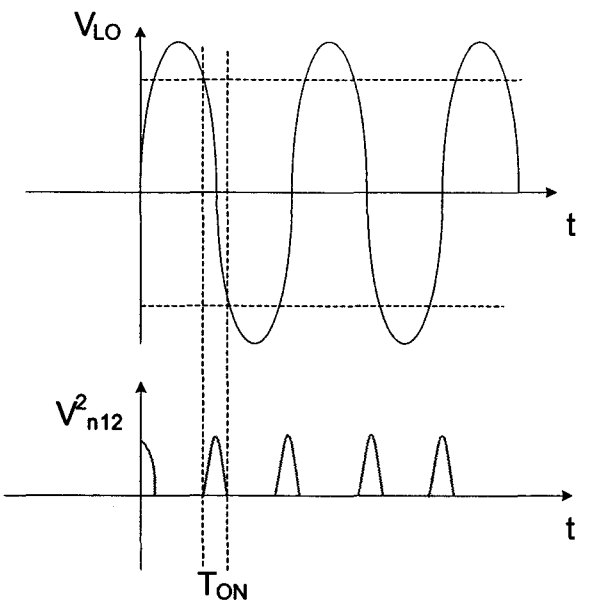


Figure 3.12: White noise contributions of the switching core of an active mixer.

On the other hand, noise performance can also be improved by increasing the switching efficiency. With a smaller $T_{ON}$ (resulted from the modified threshold voltage) at the LO transistors, it means that the time duration when both switches are conducting current is reduced. From [26],[32], it shows that LO switches only generate white noise to the output during $T_{ON}$ as shown in figure 3.12. Thus, the substrate biasing techniques, which reduce the $T_{ON}$, help to increase noise performance of an active mixer.

For linearity performance, the improvement can be estimated by using the analysis done in (3.11) with figure 3.9, since a differential pair of LO transistors with a RF transistor is analogous to the one in figure 3.9. By reducing the threshold voltage when the transistor is turning on, the overdrive voltage $\left(V_{GS} - V_{TH}\right)$ will increase. Hence, IMD3 decreases as shown in (3.11) and linearity is improved.

# CHAPTER 4

# THE DESIGN OF CMOS DOUBLE-BALANCED DOWNCONVERSION MIXER

## 4.1 Introduction

Among all the mixer topologies, active DB mixer is chosen for this thesis design. The core of the thesis is to investigate the advantages of body biasing in terms of the improvement in performance parameters. The fourth terminal of MOS transistors at the switching core of a Gilbert mixer is fed with signal to improve efficiency in switching. The input signal at the body terminal will help the switches to turn on and turn off faster. As a result, switches will be more ideal and it helps to improve performance without additional power consumption.

Even though this technique can actually apply to any mixer topology that has the body terminal of switching transistors unbiased, a Gilbert mixer topology is chosen because of its popularity. Moreover, it has good overall performances compared to other architectures. It has a lower NF and a higher conversion gain with the best signal isolation compared to other active mixers. Passive mixer is not considered because the mixer is target for Bluetooth application where RF signal operates at 2.4 GHz ISM band. The Bluetooth technology requires a low cost low power transceiver with moderate performance for a wide diffusion in short-range radio connectivity with portable electronic devices such as mobile phone and PCs. Passive mixers are not qualified since

it has very poor conversion gain and linearity is well above the requirements for Bluetooth technology. Moreover, it is not feasible for LO to provide a very high output swing. Even it is possible to generate such high LO drive, it will increase the power consumption for the overall system. Since Bluetooth chips are designed for portable equipments driven by battery cells, low power consumption is of prime importance for the mixer. According to the specification for Bluetooth receiver, it requires a sensitivity of at least –70 dBm. This means it can tolerate with a receiver inherits NF as high as 23 dB with IIP3 as low as –16 dBm [43],[1]. As long as the preceding LNA is designed with moderate gain and excellent linearity, performances from a Gilbert mixer make it very compatible to integrate with LNA for Bluetooth application. Again, CMOS is chosen as the design technologies because of the ongoing development for low voltage low power applications with low cost and high integration characteristics, which are well suited for Bluetooth applications.

To design an active CMOS DB mixer with good performances could be a very challenging task. Even with a solid understanding of the circuit operation and a clear knowledge of MOS transistor models, there are many relationships and tradeoffs between the design parameters and performance parameters. Chapter 3 should have explained the operation of Gilbert mixer circuitries clearly with the basic understanding of various performance parameters in mixer design. [44] provides very detailed descriptions of MOS transistor modeling and operations. It is impossible to obtain an optimized mixer at the first trial. Fine-tuning is often needed to optimize for certain performance parameter. This chapter is aimed to introduce a design procedure for Gilbert mixer, which is also

applicable to most mixer topologies. Then, the thesis mixer design is presented with the study of body biasing effects. Simulation and measurement results will be compared and discussed to conclude this chapter.

## 4.2 Design Procedures for Gilbert Mixer

For proper design of Gilbert mixer, an initial working design is needed before any optimization or fine-tuning of the mixer. First of all, it is necessary to know the power consumption and voltage supply that can be allocated for the mixer according to the target application. It gives the maximum allowable bias current condition for the design. With this information, designers can choose the size of the transistors and the voltage headroom dedicated for each stage. The dc bias for the LO and RF can then be chosen to ensure the transconductance transistor will be working on saturation region at all time and the LO is biased at the threshold level of the switches. LO ac magnitude is often limited by the voltage swing supplied from LO, but it is often set as a design parameter to tune the mixer for better performances. In general, it has to be large enough to switch the transistors on and off efficiently.

### 4.2.1 Circuit Design of Gilbert Mixer

By following the above procedure, it will give an initial active mixer design. However, the process requires many calculations and it relates many constraints within each circuit element. To design a Gilbert mixer, it is always easier to break it down into different stages. Since a Gilbert mixer is equivalent to the addition of two SB mixers and

a current sink, it is simpler to start with an SB mixer as the first design product. Figure 4.1 shows the dissection of a Gilbert mixer. The design considerations will be discussed along with relationships between design parameters and mixer performances at each block of the mixer element.

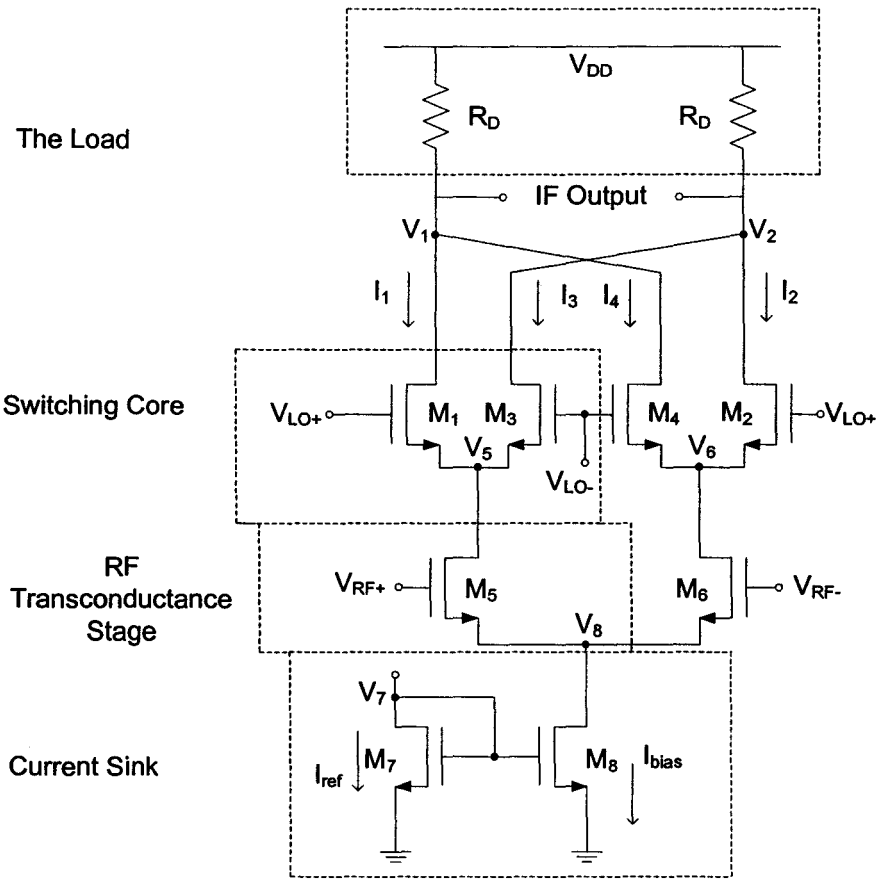


Figure 4.1: Dissection of a Gilbert Mixer.

#### 4.2.1.1 RF Transconductance Stage

In this stage of a Gilbert mixer, RF input signal is received from the LNA. The voltage signal should be converted to a current with half of the total dc bias current $I_{bias}$. In other words, an SB mixer should be designed with only half of the design bias current. In a typical Gilbert mixer, the maximum gain that can be achieved is dependent on the transconductance of the RF transistor. The maximum gain is shown in (4.1),

$$G_{DB} = (\frac{1}{2})\frac{R_L(\frac{8g_m A_{RF}}{\pi})}{A_{RF}} = \frac{4g_m R_L}{\pi} \tag{4.1}$$

which can be derived from (3.22). In order to achieve a better conversion gain, the RF transistor is always biased to operate in the saturation region at a higher $g_m$. With a target current chosen already, there are two design variables at the RF transconductor. Recall from the circuit equation for NMOS transistor operating at saturation region as shown in (4.2).

$$I_{DS} = \mu_n C_{OX} \frac{W}{L}(V_{GS} - V_{TN})^2 \tag{4.2}$$

Since voltage headroom is normally small in a typical Gilbert mixer and the transistor channel length is short, modulation length modulation is not taken into consideration in (4.2) for simplification. Hence, either adjusting the transistor aspect ratio or the voltage applied at gate of RF transistor can obtain the dc current for an SB mixer. However, the designated voltage headroom across the transistor sets the maximum gate voltage at the transconductor to ensure it operates at the saturation region. Moreover, it is noted that voltage headroom is reserved for the current sink if it will be implemented by MOS

transistors. Hence, the source node is not equal to zero and it will increase the threshold voltage at the transconductor because of a positive $V_{SB}$ from (4.3), when the body terminal is grounded.

$$V_{TN} = V_{TO} + \gamma(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}) \tag{4.3}$$

The voltage headroom is needed to input at node $V_8$ of figure 4.1 for an accurate circuit simulations. Since the magnitude of RF ac input signal $A_{RF}$ is always small in magnitude, the transistor can be linearized as a voltage controlled current source, where ac current is equal to $g_m A_{RF}$. Since the mixer gain is directly proportional to $g_m$ of the RF transconductor, which can also be seen from (4.1), it is logical to bias the transistor at a $V_{GS}$ value that gives the highest $g_m$. However, it normally results in a mixer with poor IIP3 and higher power consumption. Figure 4.2 shows a plot of the drain current and the derivatives of drain current with respect to $V_{GS}$ for an enhancement mode NMOS transistor.

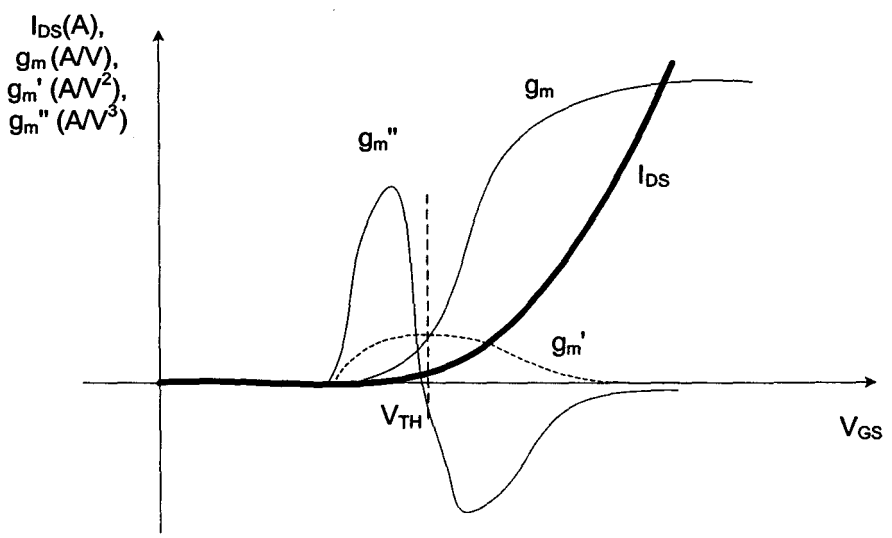


Figure 4.2: Drain current and its higher derivatives w.r.t. the gate to source voltage.

Although all curves are plotted with respect to the same $V_{GS}$, the y-axis for each curve is of different scale to each other. Moreover, sufficient $V_{DS}$ is assumed for the transistor to operate in the saturation region. When the transconductor is designed for better conversion gain and NF performance, the transistor should be biased at the $V_{GS}$ that gives a large $g_m$. From the plot, the $g_{m''}$ is around the minimum negative peak for large positive $g_m$. The $g_{m''}$ plays an important role in the IMD3 at the RF amplifier. Analogous to (3.7), the drain current of a common source MOS transistor up to the third order is expressed using Taylor series as (4.4), $v_{gs}$ is the small signal gate to source voltage.

$$i_{DS} = I_{DC} + g_m v_{gs} + \frac{g_m'}{2!} v_{gs}^2 + \frac{g_m''}{3!} v_{gs}^3 \tag{4.4}$$

With a more negative $g_{m''}$, more IMD3 is generated at the RF amplifier due to the nonlinear drain current in reality, violating the ideal $i_{DS} = g_m v_{gs}$ linear model. In theory, it is possible to obtain a high $g_m$ and a nearly zero $g_{m''}$ at higher $V_{GS}$. The curves from figure 4.2 agree with (3.11). However, with the limited voltage headroom designated for the RF transconductor in a typical four stacks Gilbert mixer, RF transistor will not be operating in saturation region when biased at such $V_{GS}$. Alternatively, a gate to source voltage near the threshold voltage can be chosen, where IMD3 will decrease with a significant reduction in conversion gain because of the small $g_m$ at the given $V_{GS}$. In addition, such a mixer consumes less power and generates more noise because of the smaller dc current through the RF transistor. Noise in the transconductance transistor accompanies the RF input signal. With the same mechanism, noise is translated in

frequency after mixing with LO signal. White noise is dominant at the transconductor [8] and it is formulated by H. Darabi in [8] as (4.5).

$$V_O^2 \propto kTR_L^2 g_m \tag{4.5}$$

The white noise power at the mixer output generated from the RF transconductance stage is proportional to the square of mixer load resistance and the $g_m$ at RF transistor. From figure 4.2, when the transistor is biased close to the threshold voltage, the reduction in $g_m$ is greater than the reduction in drain current because of the steeper $g_m$ slope. However, the load resistance will be adjusted in order to dissipate the same voltage headroom designated in the load stage. Moreover, the increase in $R_L$ also helps to increase the conversion gain as can be seen in (4.1) to compensate for the loss in $g_m$. For instance, the low tranconductance transistor is designed for a better linearity performance. It is then biased close to the threshold voltage. The current is reduced by 40% with a reduction of 50% in $g_m$ when compared to the biasing at the maximum $g_m$. Because of the square root for the load resistance (4.6), it will result in 39% increase of white noise to the mixer output with the reduction in current at the RF transistor.

$$V_{O,new}^2 \propto kT(\frac{1}{0.6})^2 R_L^2 (0.5) g_m = (1.39) \cdot kTR_L^2 g_m \tag{4.6}$$

As a result, by simply choosing the dc biasing point for the RF input signal at the gate of the transistor, there are design tradeoffs between conversion gain and NF against linearity and power consumption at the RF transconductor. And it can be chosen flexibly and should be chosen carefully to suit the application requirements.

### 4.2.1.2 The Switching Core

The switching core of a CMOS Gilbert mixer consists of two differential pairs of transistors. CMOS transistor is suitable as switches because of the good switching property. A simplified equivalent circuit of a Gilbert mixer can be seen in figure 4.3.

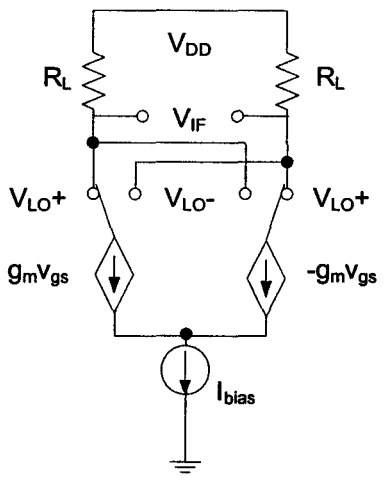


Figure 4.3: An equivalent circuit of a typical Gilbert mixer.

Voltage is amplified and converted to the current domain at the RF transistors. Ideally, the current passes through the switches at either the LO+ or the LO- path. However, because of the finite rise time and fall time of the transistor, there is a time period when both transistors conducting current from the RF stage. In other words, all switches in Gilbert mixer are conducting current during a period of time. It is undesirable since it degrades performances of the mixer.

Voltage headroom, aspect ratio of transistors, LO dc bias voltage, LO ac magnitude, and LO frequency are the design parameters for the switching core of an SB

mixer. The LO frequency determines the mixer IF since it is equal to the difference of LO and RF frequency in a downconversion mixer. Designers have to ensure the switching transistors can handle the maximum current through them, which is equal to the dc bias current at the RF transistor with the addition of ac current converted by the RF amplifier. It is related to the voltage headroom and the transistor size at the switching core. LO dc bias should be chosen around the threshold voltage of the transistors. By having $V_{GS}$ around $V_{TH}$, a small ac LO power is enough to turn the transistor on or off. It increases the efficiency in switching for a lower LO power. However, it is difficult to have the dc bias exactly at the threshold voltage because of the fluctuation at the source node. But the near threshold voltage biasing relaxes the drain to source voltage headroom for the transistor to work in the saturation region. In addition, it ensures a close to 50% duty cycle performance from the switches. In other words, the switches in a differential pair will be turned on or off with the same duration within an LO period. This implies with the properties of the same magnitude in ac current passing through the differential switches and the same switching function characteristics between them. Recall from (3.16) to (3.22), LO and RF feedthroughs are suppressed efficient assuming with the 50% duty cycle because it takes the full advantage of the differential pairs. Furthermore, conversion gain will be optimized when the switch operates at 50% duty cycle. A simple derivation using Fourier transforms on the waveform will be able to prove this statement. (3.12) is rewritten as (4.7) to show the voltage output of an SB mixer.

$$V_{IF}(t) = [I_{DC} + g_m A_{RF} \cos\omega_{RF} t] \cdot LO(t) \cdot R_L \tag{4.7}$$

$$V_{IF}(t) = [I_{DC} + g_m A_{RF} \cos\omega_{RF}]\left[2\sum_{n=1}^{\infty} \frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}} \cos(n\omega_{LO}t)\right] R_L$$

The LO function from a 50% duty cycle perfect square wave will contribute a coefficient of $(4/\pi)$ in the SB mixer. However, for an SB mixer with a LO drive giving the switching function as shown in figure 4.4, it will have a smaller coefficient when $n$=1 to give the IF output for mixing.

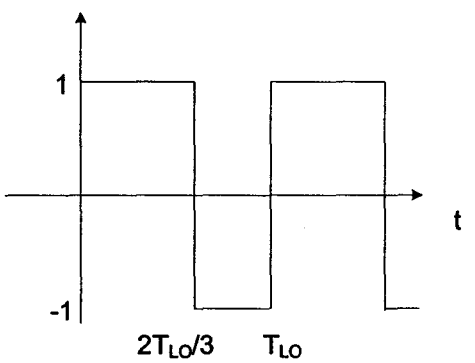


Figure 4.4: The switching function for a SB mixer.

The switching function is assumed with a 66.7% and 33.3% duty cycle for the differential pair. It is still assumed a perfect switch with zero fall time and rise time. Using Fourier transform to get the coefficient when frequency is at $\cos\omega_{LO}t$, we get (4.8).

$$\frac{3}{2n\pi}\sin(\frac{2n\pi}{3}) + \frac{3}{n\pi}\sin(\frac{n\pi}{3}) = \frac{9\sqrt{3}}{4\pi} \tag{4.8}$$

It has 3% loss in the conversion gain in this ideal case. However, when LO transistors are not biased near their threshold voltage, the ac current through them at the positive and negative LO drives are generally different. It causes more penalty in the gain performance as can be seen from (4.7). As for the LO power, it can be easily chosen by

running the NF and the conversion gain simulation within a range of LO power to get the optimal point. As shown in figure 4.5, the general trend of having the minimum NF and the maximum conversion gain occurring within the same range of LO power held for all supply voltages [26].

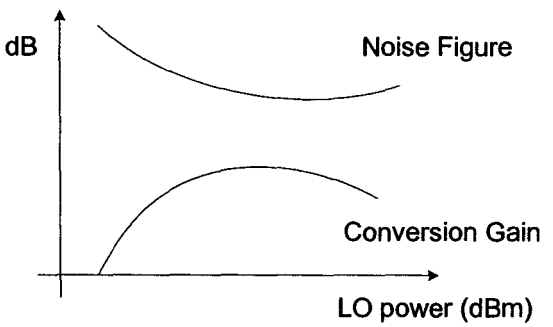


Figure 4.5: Conversion gain and noise figure as a function of LO power.

Since it is difficult to analyze the switching core of mixer by hand calculation, designers depend on circuit simulators almost exclusively to find the optimal LO power for the switching transistors. Moreover, it is understood that when the LO power gives the optimal NF and gain, the LO power is sufficient for efficient switching. A further increase in LO power will degrade NF, gain and linearity of the mixer. Question maybe asked regarding the case for a small LO power. Since a cosine function decomposes to two real even delta functions in frequency domain, only half of the power is wasted. However, when the switching core is behaving as a cosine wave function, it means that the LO transistors is functioning as another amplifier in response to $A_{LO}\cos\omega_{LO}t$ and the voltage output of an SB mixer becomes (4.9) with the conversion gain in (4.10).

$$V_{IF}(t) = [I_{DC} + g_{mRF} A_{RF} \cos\omega_{RF} t] \cdot 2[g_{mLO} A_{LO} \cos\omega_{LO} t] \cdot R_L \quad (4.9)$$

$$C.G = g_{mRF} g_{mLO} A_{LO} R_L \quad (4.10)$$

The factor of one half for splitting in power for the two frequency components is cancelled off with the factor of two in a differential pair of the switching transistors in an SB mixer. The gain is much lower than the case with large LO drive since the gain is now dependent on the magnitude of LO drive and the transconductance of the LO transistors, which are much smaller than unity. In addition, the $A_{LO}$ is supplied by the LO drive whose amplitude is hard to control exactly. As a result, the gain of a mixer will also be difficult to control with it being dependent on the LO power directly.

### 4.2.1.3 The Loads

The load conserves the voltage headroom for the mixer output. It is generally implemented in polysilicon resistors. The resistance value simply depends on the voltage headroom at the load stage and the current consumption of the mixer. More voltage headroom can be allocated for the load by increasing the resistance. It increases the conversion gain but generates more white noise at the same time. However, a typical Gilbert mixer has four stacking stages in the architecture. There is limited voltage headroom that can be allocated to the load stage. Hence, PMOS active loads can be used to save some of the voltage dissipation for low voltage applications. However, the fabrication mismatches between two loads can introduce a big discrepancy from designed mixer operation condition, which degrades performances of the design. Addition circuit attention is also needed to ensure the PMOS active loads are working in the active region.

In addition, PMOS active loads introduce flicker noise that is absent in polysilicon loads, even though PMOS transistors are less noisy than their n-channel counterparts.

#### 4.2.1.4 A Complete Gilbert Mixer

After the completion of a single SB mixer, a complete Gilbert mixer can be composed as shown in figure 4.1 by adding the two SB mixers with a current sink to stabilize the total dc current consumed by the Gilbert mixer. The current sink has to be stable enough to stand the small ac current fluctuation at the node $V_8$ of figure 4.1, which is the common source node of the differential RF transistors.

### 4.2.2 Geometric Programming

In section 4.2.1, it is clear that to obtain an initial mixer prototype requires many circuit designs and considerations. In order to automate the processes and to save considerable amount of time in designing mixers, convex optimization is an alternative to achieve this goal. In this section, sets of constraint for Gilbert mixer design are formulated as posynomial functions of the design variables. The size of CMOS transistors used in the proposed circuit in figure 4.1 are optimized by means of standard Geometric Programming (GP). Two algorithms, generalized linear programming (GLP) and interior-point method, are adopted for the purpose of result comparisons. Even though convex optimization has not been widely used in analog circuits design, the power tool might reduce the design time devoted to the analog circuitry significantly. It is

noticed that a number of circuit constraints and specifications of a Gilbert mixer can be formulated as a special form in convex optimization problem. It will be shown how they can be formulated as a set of posynomial GP in 4.2.2.2. After a set of monomial and posynomial equations are obtained, the formula with the size of transistors is chosen as the objective function for optimization. Certainly, many optimizations, other than the size of transistors, can be achieved if the objective function can be related to formulate a set of constraints from the circuit requirements and the design specifications. GPGLP [45] and MOSEK [46] are used to solve the GP problem respectively, and discussion of the result will be presented in 4.2.2.3. GPGLP is a software written in FORTRAN using the algorithm by Rajgopal [47], while MOSEK is recommended by Dr. Stephen Boyd using the interior-point algorithm to optimize a CMOS operating amplifier design [48].

### 4.2.2.1 Posynomial Geometric Programming

Let $x_1,...,x_n$ be $n$ real and positive variables. A function is called a posynomial function of $x$ if it has the form of (4.11)

$$f(x_1,...,x_n)=\sum_{k=1}^{t} c_k x_1^{\alpha_{1k}} x_2^{\alpha_{2k}} \cdots x_n^{\alpha_{nk}} \tag{4.11}$$

where $c_j \geq 0$ and $\alpha_{ij} \in \Re$ . Note that the coefficients must be nonnegative but the exponents can be any real numbers, including negative and fractional. When $t = 1$, the function is a monomial function, whereas it is called posynomial when $t$ is greater than one. In the Gilbert mixer as shown in figure 4.1, all constraints can be formulated as the GP form (4.12) as a standard optimization problem,

$$\begin{aligned} &\min\ f_o(x) \\ &subject\ to\ \ f_i(x) \le 1,\ \ i = 1,\ldots,m, \\ &\qquad g_i(x) = 1,\ \ i = 1,\ldots,p, \\ &\qquad x_i > 0,\ \ i = 1,\ldots,n, \end{aligned} \tag{4.12}$$

where $f_i$ are posynomial and $g_i$ are monomial functions.

#### 4.2.2.2 Problem Formulation

As discussed in section 4.2.1, the design of a Gilbert mixer will be simpler if it is dissected into sub-building blocks. The proposed design as shown in figure 4.1 is broken into three parts including the current sink, the switching core, and the RF transconductance stage. This section serves as an example to show how the circuit requirements and design specifications can be formulated to optimize the size of transistors.

##### 4.2.2.2.1 Current Sink Stage

The current sink consists of NMOS transistors $M_7$ and $M_8$. With the design, a same voltage drop between gate and source of $M_7$ and $M_8$ is forced with current $I_{ref}$ passing through $M_7$. $I_{bias}$ can then be calculated neglecting the channel length modulation effect of the device.

$$I_{ref} = 0.5K_n'(\frac{W_7}{L_7})(V_{GS7} - V_{TH})^2 \tag{4.13}$$

$$I_{bias} = 0.5K_n'(\frac{W_8}{L_8})(V_{GS8} - V_{TH})^2$$

Since $V_{GS7} = V_{GS8}$, after reformulating the equations, constraint (4.14) is obtained with design variables $W_7$, $W_8$, $L_7$ , and $L_8$.

$$\frac{W_8 L_7 I_{ref}}{W_7 L_8 I_{bias}} = 1 \tag{4.14}$$

$M_7$ is operating in saturation region by the condition of the design. And for $M_8$ to work in saturation region, an additional constraint (4.15) has to be considered.

$$V_{DS} \geq V_{GS} - V_{TH} \tag{4.15}$$

By observation from the circuit, $V_{DS} = V_8$ and $V_{GS} = V_7$. Hence, (4.15) becomes

$$V_8 \geq V_7 - V_{TH}$$

and from (4.13),

$$V_7 = \sqrt{\frac{2I_{ref} L_7}{K_n' W_7}} + V_{TH}$$

then, it simplified to (4.16).

$$V_8 \geq \sqrt{\frac{2I_{ref} L_7}{K_n' W_7}} \tag{4.16}$$

## 4.2.2.2.2 Switching Core Stage

PMOS transistors are used for M1 - M4 instead of the NMOS transistors as shown in figure 4.1. For the operations of the two differential pair transistors, assuming either

$M_1$, $M_2$ or $M_3$, $M_4$ will be turned on respectively. When a negative $V_{LO}$ is applied to the circuit, $M_1$ and $M_2$ are on. The current $I_1$ and $I_2$ flow through the transistor to the RF block. While with a negative $V_{LO}$, $M_3$ and $M_4$ will conduct current. As a result, the following constraints can be observed. Assuming $M_1$, $M_2$, $M_3$, and $M_4$ are operating in the saturation region when they are turned on. Since for PMOS transistors,

$$I_{SD} = 0.5K_p'\frac{W}{L}(V_{SG} + V_{TP})^2$$

when $V_{SD} \geq V_{SG} + V_{TP}$, assuming M1 and M2 on, then

$$I_1 = 0.5K_p'(\frac{W_1}{L_1})(V_{SG1} + V_{TP})^2$$

hence,
$$V_{SG1} = \sqrt{\frac{2I_1L_1}{K_p'W_1}} - V_{TP}$$

in order to satisfy the condition for saturation region,

$$V_1 \geq \sqrt{\frac{2I_1L_1}{K_p'W_1}} + V_5 \tag{4.17}$$

$$V_2 \geq \sqrt{\frac{2I_2L_2}{K_p'W_2}} + V_6 \tag{4.18}$$

In addition, the differential switching pair should be symmetrical, so the size of transistors should be matched as well. Hence, additional constraints on the size of transistors are needed (4.19) - (4.22).

$$W_1W_3^{-1} = 1 \tag{4.19}$$

$$W_2W_4^{-1} = 1 \tag{4.20}$$

$$L_1 L_3^{-1} = 1 \tag{4.21}$$

$$L_2 L_4^{-1} = 1 \tag{4.22}$$

#### 4.2.2.2.3 RF Transconductance Stage

$M_5$ and $M_6$ are NMOS transistors that biased to work in saturation region. A max small signal variation, $V_{in}$, is set such that it is within the limitation as a small signal to the RF amplifier. A matching between the size of $M_5$ and $M_6$ is also needed as a constraint (4.23), (4.24) at this stage.

$$W_5 W_6^{-1} = 1 \tag{4.23}$$

$$L_5 L_6^{-1} = 1 \tag{4.24}$$

And constraints on $V_5$ and $V_6$ can be formulated as below.

$$V_5 \geq \sqrt{\frac{2I_1 L_5}{K_n' W_5}} + V_8$$

$$V_6 \geq \sqrt{\frac{2I_2 L_6}{K_n' W_6}} + V_8$$

And from constraints (4.16), (4.17), and (4.18), two new constraints can be formulated as (4.25), (4.26).

$$\frac{1}{V_1}\left(\sqrt{\frac{2I_1 L_1}{K_p' W_1}} + \sqrt{\frac{2I_1 L_5}{K_n' W_5}} + \sqrt{\frac{2I_{ref} L_7}{K_n' W_7}}\right) \leq 1 \tag{4.25}$$

$$\frac{1}{V_2}\left(\sqrt{\frac{2I_2 L_2}{K_p' W_2}} + \sqrt{\frac{2I_2 L_6}{K_n' W_6}} + \sqrt{\frac{2I_{ref} L_7}{K_n' W_7}}\right) \leq 1 \tag{4.26}$$

For the maximum $V_{in}$ from RF signal, two more constraints are formed.

$$10 \cdot \sqrt{\frac{2I_1 L_5}{K_n' W_5}} \leq 1 \tag{4.27}$$

$$10 \cdot \sqrt{\frac{2I_2 L_6}{K_n' W_6}} \leq 1 \tag{4.28}$$

## 4.2.2.2.4 Standard Form of the GP Problem

With all the constraints formulated, the objective function for the size of transistors in the proposed circuitry can be formulated as:

$$W_1 L_1 + W_2 L_2 + W_3 L_3 + W_4 L_4 + W_5 L_5 + W_6 L_6 + 0.5 W_7 L_7 + 0.5 W_8 L_8 \tag{4.29}$$

A weighting coefficient of 0.5 is given to the current image block for less significance in the circuit design of mixer. The object function is minimized subject to the constraints (4.14), (4.19), (4.20), (4.21), (4.22), (4.23), (4.24), (4.25), (4.26), (4.27), and (4.28) with a lower bound of 2.0 um in weight (W) and 0.2 um in length (L). Table 4.1 shows the design parameters used in the circuit design. This GP convex optimization problem has 16 design variables with seven equality constraints and six inequality constraints (including the two lower bounds posynomial constraints), while all design variables are greater than 0. It is important to mention that there are many other different objectives (conversion gain, intermodulation point, noise factor) that can be optimized using geometric programming. This example is only served to show the effectiveness in the automation of the mixer design. Many constraints is simplified or neglected, such as the

LO power and the constraints in order to meet the minimum requirements for those performance parameters are not included in this design.

| Parameter | Value |
|---|---|
| Minimum Weight, $W_{min}$ | 2.0 um |
| Minimum Length, $L_{min}$ | 0.2 um |
| Biased Current, $I_{bias}$ ( $I_1 + I_2$ ) | 1.0 mA |
| Current 1, $I_1$ | 0.7 mA |
| Current 2, $I_2$ | 0.3 mA |
| Kp' (PMOS) | 30 uA/$V^2$ |
| Kn' (NMOS) | 92 uA/$V^2$ |
| Supply Voltage, $V_{DD}$ | 2.0 V |
| Node Voltage at $V_1$ | 1.3 V |
| Node Voltage at $V_2$ | 1.7 V |
| Node Voltage at $V_8$ | 1.0 V |
| Reference Current, $I_{ref}$ | 2.0 mA |
| Resistor Value, $R_D$ | 1.0 kΩ |

Table 4.1: Design parameters used in the circuit.

### 4.2.2.3 Problem Simulations and Discussions

Two different algorithms are adopted to simulate the GP problem given in section 4.2.2.2.3. Since the multiple of W and L would drive the solution of the objective function to the $10^{-12}$ $m^2$ range, the minimum weight and length of transistors are modified to 2.0 m and 0.2 m due to limitations on the software. Since W and L are also a ratio to each other, the modification would not affect the algorithm in optimizing values for design variables. The simulation results of the design variables are summarized in table 4.2.

There are a few testing elements used as a quick indicator to verify the correctness of the GP in this mixer design. Two currents with significant difference are input as $I_1$ and $I_2$. Moreover, very small voltage headroom is reserved for transistors $M_1$ and $M_5$. From the result, it shows that there is an enormous value for $W_5$ and $W_6$ because with the limited voltage headroom, a very large transistor is needed to support the specific current in the saturation region. In addition, ratio between $W_1$ and $W_2$ is more than the doubled current because of the limited voltage headroom allocated for $M_1$. Ratio of the output $W_7$ and $W_8$ is according to their current ratio and all transistors are optimized with their minimum length in this problem. As a result, the simulation results from table 4.2 are very reasonable.

| Design Variables (W and L in um) | GPGLP | MOSEK |
|---|---|---|
| $W_1$ | 74.274931 | 74.33833 |
| $W_2$ | 11.67866 | 11.68469 |
| $W_3$ | 74.274931 | 74.33833 |
| $W_4$ | 11.67866 | 11.68469 |
| $W_5$ | 1722.0342 | 1722.034 |
| $W_6$ | 1722.0342 | 1722.034 |
| $W_7$ | 173.5318 | 173.3463 |
| $W_8$ | 86.76588 | 86.67316 |
| $L_1$ | 0.199999 | 0.2 |
| $L_2$ | 0.199999 | 0.2 |
| $L_3$ | 0.199999 | 0.2 |
| $L_4$ | 0.199999 | 0.2 |
| $L_5$ | 0.199999 | 0.2 |
| $L_6$ | 0.199999 | 0.2 |
| $L_7$ | 0.199999 | 0.2 |
| $L_8$ | 0.199999 | 0.2 |
| Objective Function | 749.225 $um^2$ | 749.19 $um^2$ |

Table 4.2: Simulation results from the two software.

The objective values that obtained from both algorithms are very close. But with some comparisons done on the two software, MOSEK always guarantee to give a better globally optimal solution. Moreover, the length of transistors used by GPGLP is a little

bit below the lower bound. This software does not work very well with high significant figures. The solutions obtained are very consistent after a number of simulations. MOSEK is proved to be a more powerful tool because of a better optimal value with less processing time (8-10 iterations in MOSEK, 18-22 iterations in GPGLP). Due to the size of the problem, only 0.01 second is needed for both algorithms to locate the optimal solution on a P4 2.0GHz PC with a 512MB RAM. However, MOSEK should work better in GP problem with more system variables. MOSEK uses interior-point method for posynomial GP problem. Interior-point algorithm is recently developed to solve GP globally with great efficiency and no initial point is needed. A primal barrier is used for solving the convex form of a GP. The dual of the problem is also solved simultaneously for ensuring the convergency and accuracy of the solutions. However, in GPGLP, the primal-dual pair in GP are linearized so that the primal is stated as a semi-infinite linear program and the dual as a GLP. The procedure begins with an initial approximation of the GLP as a linear program with some initial set of columns, which is then solved using the simplex method [45]. At each iteration, the dual prices at the current iteration (simplex multipliers) are used to price out columns and attractive columns are added to the GLP to obtain a better approximation. The LP is then re-optimized and the procedure continues until no columns price out favorably. In this design, MOSEK implemented with interior-point algorithm gives a better global solution with a better performance.

The GP shows a promising automation method for mixer design. Although it takes considerable amount of time to develop and to formulate the set of constraints, it can be reused for redesigning a mixer with the same topology. Simply changing the

design parameters or conditions, it is guaranteed to give the global optimal solution for the objective function. For instance, it is suitable to redesign Gilbert mixers to pursue the low voltage applications with the continuous reduction of supply voltage. Even if the Gilbert mixer is chosen to have the same architecture, a new design has to be started in conventional circuit design because the reduction in voltage headroom across each stage may push the transistors out of the desired working region. With all the new changes, each block of the Gilbert mixer has to be redesigned to ensure the proper working of the circuit. The only design time that can possibly be saved in the design process is probably due to the experiences and the skills of designers. On the other hand, a GP optimization can easily be applied again with some numerical modifications in the design parameters from table 4.1. The set of constraints from previous designs can also be reused again with very few modifications, if the architecture stays the same. The optimal design can be obtained again without much effort in going through all the design procedures. However, the GP optimization only gives an optimal mixer design on condition that all the circuit requirements, performance parameters and design specifications have been integrated into the constraints. A better solution will be obtained with more detailed specification on the constraints, which is the same case as the conventional circuit design. It is noted that the figure of merit, which is sometimes utilized to evaluate mixer designs, can be formulated as the objective function in order to optimize the design variables in mixer design. It certainly takes time to formulate the GP problem for mixer optimizations. However, it will reduce the design time significantly for the future developments on the same mixer architecture. As a result, GP convex optimization has

given a very efficient automation method for a Gilbert mixer design as shown in our example.

## 4.3 Circuit Implementations of a Gilbert Mixer

The thesis mixer design is applied with a signal to the bulk terminal at the LO switches. However, a basic Gilbert cell is needed to serve as a fundamental to compare the performances of the improved Gilbert designs with the bulk biased. Therefore, a mixer with three different configurations at the bulk of the LO switches are designed and simulated using Cadence SpectreRF® based on the BSIM3V3 models. The mixer design is integrated in a TSMC 0.18 um CMOS process. This section presents the three different configurations along with their simulation and measurement results. The performance improvements by using different bulk biasing are discussed, and the figure of merit used to evaluate and to compare mixer designs is introduced.

### 4.3.1 The Fundamental Gilbert Mixer (Design A)

Figure 4.6 shows the circuit implementation of the fundamental Gilbert mixer of this thesis. Since the mixer is designed for Bluetooth applications, the main focuses are on a lower manufacturing cost, a lower power dissipation, and a smaller chip area consumption. Basically, the circuit design in figure 4.6 is very similar to the one in figure 4.1, except with the usage of PMOS transistors for the LO switches. The design parameters and the operating conditions of the fundamental Gilbert mixer are listed in table 4.3.

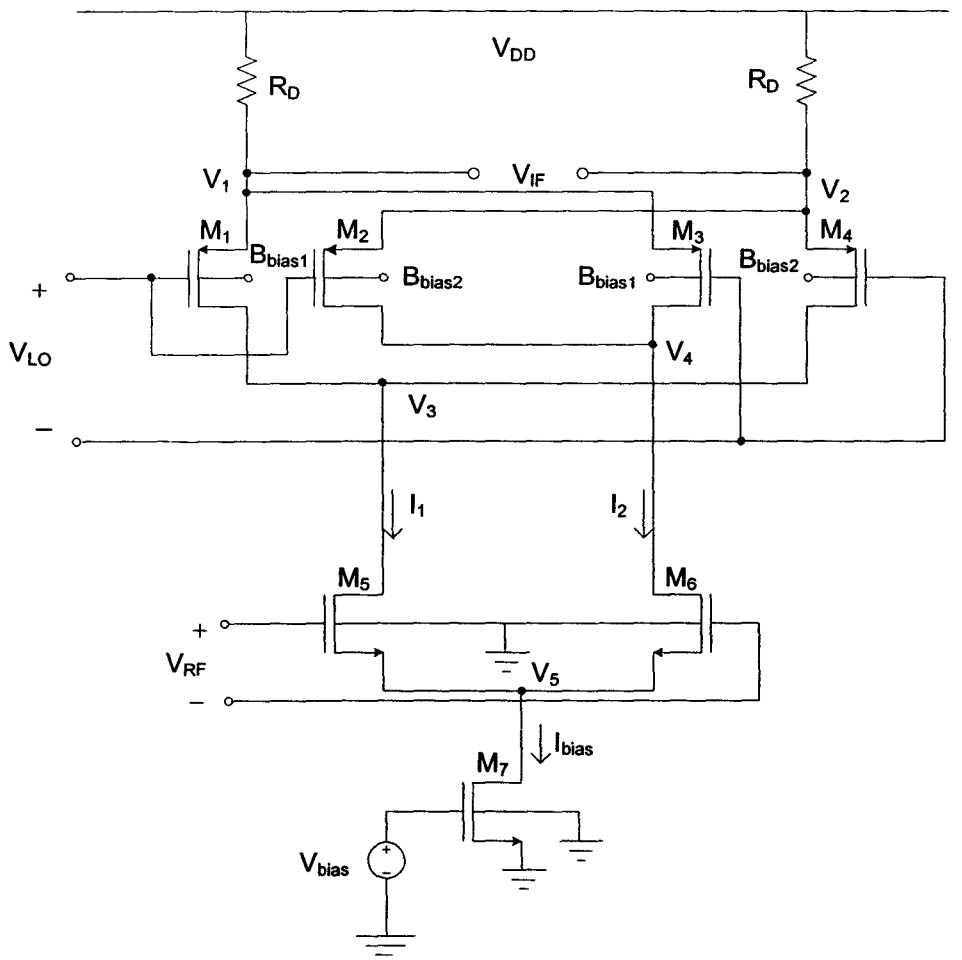


Figure 4.6: Circuit implementation of the Gilbert mixer.

All high frequency transistors $M_1$ to $M_6$ are designed with the minimum length of 0.18 um, since the I-V characteristic is more linear at shorter channel length [49] of CMOS transistors. Moreover, it takes the advantage of downscaling of CMOS technologies to minimize the utilization of chip area. The width of those transistors is designed with 2.5 um in order to simplify the process when laying out the transistors. Different sizes of transistors can then be designed with different finger numbers (nr).

The current sink is chosen with much larger aspect ratio in order to minimize the VDS across it. In other words, the source voltage $V_5$ of the transconductors $M_5$ and $M_6$ in figure 4.6 is kept as small as possible. A voltage supply of 1.2 V is chosen to minimize the power consumption of the design with bias current $I_{bias}$ less than 300 uA. For such a small bias current in a Gilbert mixer, the design having a poor performance in conversion gain, and NF is compromised. In order to utilize the fourth terminal, n-channel transistors can be used as the switches but a twin-well process is needed. To maintain a low manufacturing cost, p-channel switches are used. Even though the hole has a lower mobility, which may have adverse effects on the switching, it has several advantages when integrated in the design. P-channel transistors are known to generate less noise. Moreover, it is possible to have no dc biased for the switches as shown in table 4.3. Nevertheless, there are strong indications that such a mixer will work without great penalties and it should be adequate for the study of body biasing at the switching core. For the design with the body terminal $B_{bias1}$ and $B_{bias2}$ connected to the $V_{DD}$, it is referred as Design A, which is just an original mixer designed to study for the improvement on performance parameters at the switching core when body biasing techniques are applied.

The LO dc bias is chosen close enough to the threshold voltage of the switch in order to minimize the LO power, while the dc level at RF stage is biased near the highest $g_m$ to optimize for the conversion gain. The magnitude of LO drive is chosen from running an LO sweep on the NF and the conversion gain simulations on the mixer design. It is shown in figure 4.7 that the optimal point is located at +0 dBm. A higher LO power is expected because of the usage of p-channel switches. The RF transconductance

transistors are designed with the nmos_rf model in Cadence SpectreRF®, which includes parasitic effects at high frequency. However, pch model is chosen for the LO switches because of the limitation of the minimum nr on the pmos_rf model.

| Design parameters and operating conditions | Value |
|---|---|
| Supply Voltage (V) | 1.2 |
| RF frequency (GHz) | 2.4 |
| LO frequency (GHz) | 2.3 |
| RF dc bias (V) | 0.804 |
| LO dc bias (V) | 0.0 |
| RF transistor aspect ratio (um) (W/L) | 2.5/0.18 |
| LO transistor aspect ratio (um) | 2.5/0.18 |
| Current sink dc bias (V) | 0.589 |
| Current sink transistor aspect ratio (um) | 50/1.0 |
| RF fingers number | 6 |
| LO fingers number | 2 |
| Current sink fingers number | 2 |
| Load resistor $R_D$ ( $k\Omega$ ) | 2.0 |

Table 4.3: Operating conditions and design parameters for the fundamental mixer.

The buffer is not shown in figure 4.6, it will be presented in detail with Design C. In order to compare the differences in the performance of the mixer core only with different body biasing techniques, simulations with the buffer is not included here. They will be presented with measurement results in section 4.3.3.3.

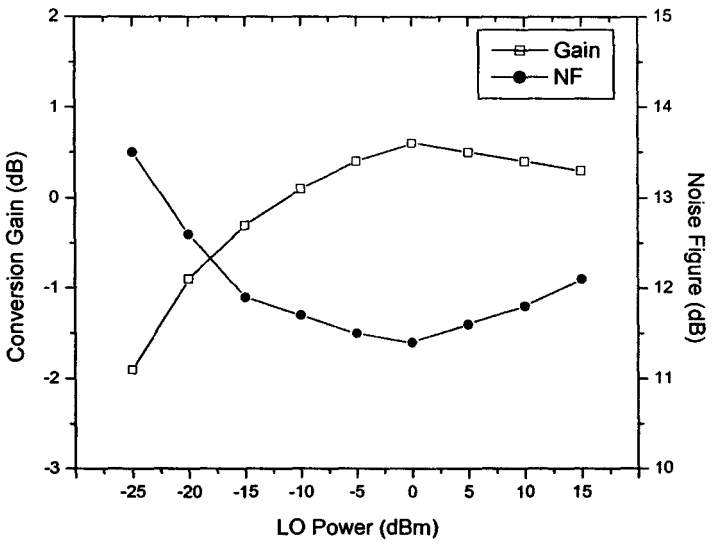


Figure 4.7: Simulation results of NF and conversion gain against LO power (Design A).

## 4.3.2 No Body Effect Gilbert Mixer (Design B)

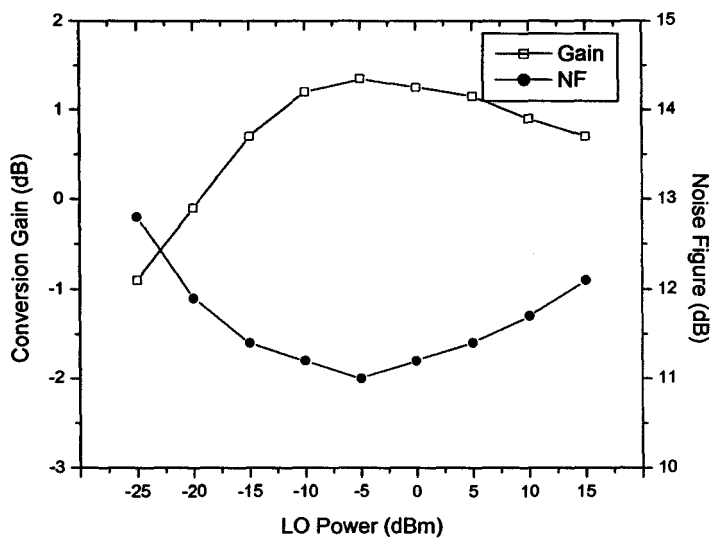


Figure 4.8: Simulation results of NF and conversion gain against LO power (Design B).

It is observed from simulations that there is more than 0.5 V difference between the body and the source terminal at the LO transistor when the switch is in the ON stage. It contributes a huge body effect at the switches, which is not desirable. From the circuit shown in figure 4.6, instead of having the bulk terminal tied to $V_{DD}$, the simplest method to get rid of this body effect is to connect the $B_{bias1}$ of $M_1$ and $M_3$ to node $V_1$ and the $B_{bias2}$ of $M_2$ and $M_4$ to node $V_2$. The mixer with such a configuration is referred as Design B. By doing so, the voltage difference between the source and the body terminal will be zero at all times. Before the discussions of the advantages with body biasing techniques, figure 4.8 is shown with the simulation results with the same circuit operating conditions and design parameters as in table 4.3. There are several interesting results from the elimination of the body effect in a typical Gilbert mixer.

First of all, the optimal NF and conversion gain occurs at a lower LO power. It means a better performance at low power consumption, which is very desirable. Explanation for this phenomenon is simple. The LO transistors act as switches to direct the current through the mixer. A threshold voltage with no body effect results in a less negative $V_{TP}$, as can be seen from (4.30).

$$V_{TP} = V_{TO} - \gamma(\sqrt{V_{BS} + 2\phi_F} - \sqrt{2\phi_F}) \tag{4.30}$$

Whether the PMOS is operating in the linear or the saturation region, a less negative $V_{TP}$ requires a smaller $V_{SG}$ to support the same current through the transistor. Although the fluctuation in the source node $V_1$ and $V_2$ follows the LO drive, it is in a much smaller amplitude. Hence, a reduction in the body effect means that a similar switching function can be supported with a smaller LO drive. However, why it does not give the same

performance but behaves even better? For this no body effect design, $V_{TP}$ is a constant and is always less negative than or equal to the threshold voltage in the LO switches of Design A. Figure 4.9 shows the output current characteristic of a differential LO switches with different instantaneous LO powers and threshold voltages, when parasitic capacitive effects are ignored.

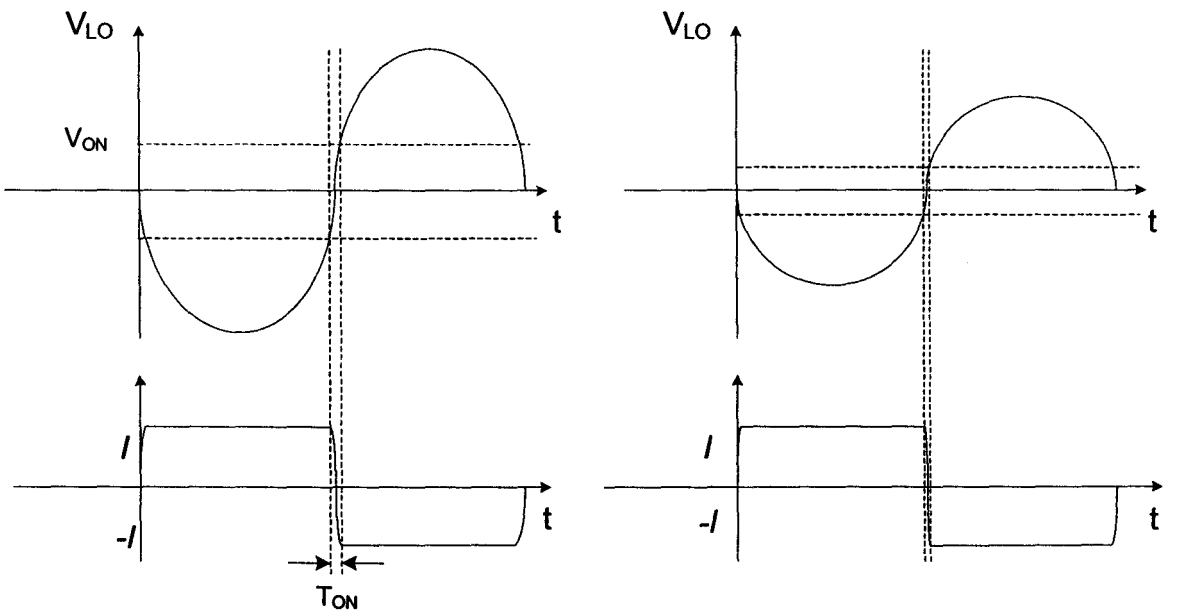


Figure 4.9: $T_{ON}$ resulted from different LO drives and threshold voltages in an SB mixer.

The source voltage is integrated with the threshold voltage to form $V_{ON}$, which is the turn on voltage. Since the source node is varying, the $V_{ON}$ is just an average value to illustrate the effects of a smaller turn on voltage. The plots show that a smaller LO power with a smaller turn on voltage can achieve a smaller $T_{ON}$ period. $T_{ON}$ is the period when both transistors of a differential pair are conducting current. Both transistors have to conduct the current that is fixed by that RF transconductor when the other transistor is not completely turned off. A smaller $T_{ON}$ in the output current plot means a better switching

at the LO transistors because of the shorter rise time and fall time performances from the transistors. It agrees with simulation results that a smaller $T_{ON}$ is resultant from Design B. The reduction in $T_{ON}$ means less noise generation from the switch, and a steeper rise time and fall time slope means a better conversion gain and a fewer IMD3 generation, more details will be covered in the next section. As a result, better performances in a Gilbert mixer can be achieved with a lower LO drive in a no body effect design as presented.

Secondly, it can be seen from simulation results that the slopes for both the NF and the gain of Design A and B are similar until they hit the optimal LO power. Slopes for Design B degrade in a faster manner than Design A with the no body effect implementation. Before the mixer operates at the optimal LO power, the improvement in the gain and the NF for Design B should be proportional in theory. This can be seen easily by plotting a similar graph as in figure 4.9. The percentage in the reduction of $T_{ON}$ is the same for a smaller or a larger LO power. However, when the switches is overdriven by the LO drive after the optimal point, the reduction in threshold voltage exaggerates the adverse effects and further degrades the performance of Design B. Even though IIP3 simulation is not shown yet, but in theory it should be improved by increasing the overall gain in Design B. As shown in figure 4.10, an upshifted output power slope with the same 3-dB slope will increase the IIP3 point. [13],[15] show that IMD3 decrease with the increasing of LO power until a considerably large LO drive is provided. Hence, the IIP3 will further increase if the 3-dB slope is downshifted. The performance comparisons between Design A and B is summarized in table 4.4. Note that

the performance of Design B is not optimized at 0 dBm LO power. With the same power consumption, Design B has a better conversion gain and NF performance. IIP3 and 1-dB compression point is also expected to be improved with 0 dBm LO power.

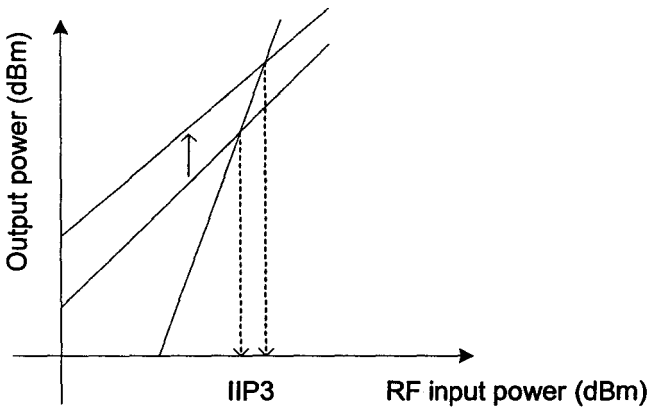


Figure 4.10: IIP3 with an upshifted 1-dB output power slope.

| RF power at –25 dBm | LO power (dBm) | IF (MHz) | NF (dB) | Gain (dB) | Current (uA) | Power Consumption (mW) |
|---|---|---|---|---|---|---|
| Design A | 0.0 | 100 | 11.4 | 0.6 | 300 | 0.36 |
| Design B | 0.0 | 100 | 11.2 | 1.25 | 300 | 0.36 |

Table 4.4: Performance comparisons of mixer Design A and B.

### 4.3.3 Body Biased Gilbert Mixer (Design C)

Basically, the previous design with no body effect helps to turn the LO switches on more efficiently. With a lower constant threshold voltage, a switch is turned on more easily. On the other hand, since the transistor conducts current more easily, it is more difficult to turn the transistor off. With the performance improvements from the Design

B at no extra expense in power consumption, a varying biasing technique seems very promising in achieving even better results. A lower threshold voltage only helps the transistor to conduct current more easily, but the $T_{ON}$ is the transition interval when the transistor goes from completely on to completely off state. Lowering the threshold voltage can reduce the rise time of the transistor, but the fall time could only be reduced by making the switch more easily turned off. In order to achieve this goal, the obvious method is to bias the bulk terminal correspondingly such that the body effect helps the switches to turn on and off more efficiently. Figure 4.11 shows the technique when biasing the bulk terminal of LO switches in this thesis.

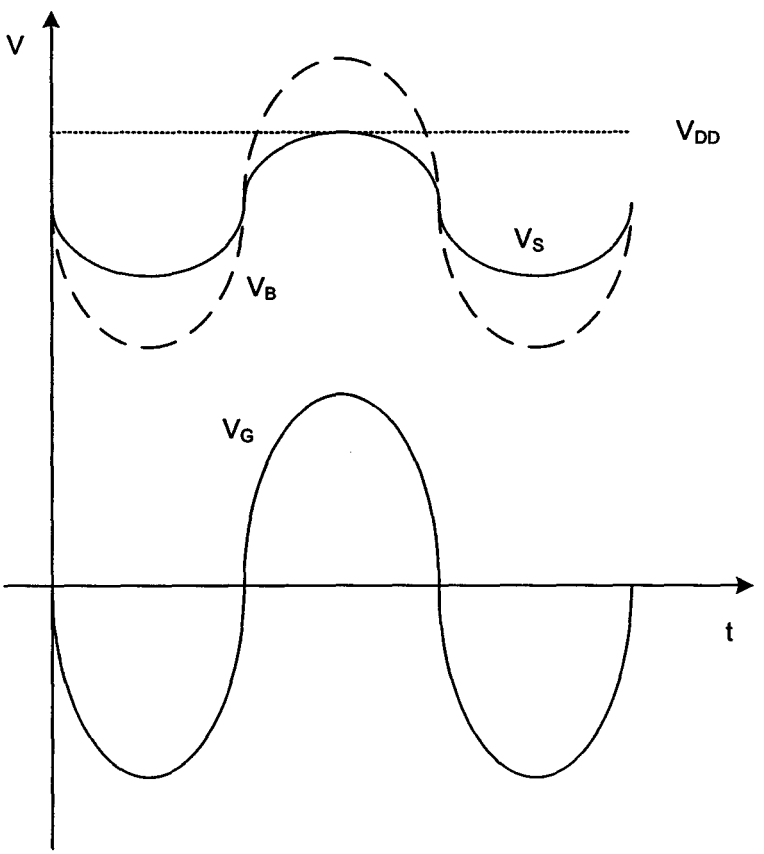


Figure 4.11: The output waveforms at various nodes of a LO switch.

Design A has the bulk terminal connected to $V_{DD}$. It means that when the switch is turning on at the negative LO phase, the $V_{BS}$ is increasing to the maximum positive value. From (4.30), a positive $V_{BS}$ increases $V_{TP}$ more negatively. On the other hand, when the switch is about to turn off in the positive LO phase, the $V_{TP}$ is reaching the minimum value. As a result, in a typical Gilbert mixer, the switch finds it harder to turn on and off completely. It decreases the efficiency in the LO switch. Design B has the bulk terminal connected to the source terminal. As discussed in the previous section, it helps the switch to turn on more easily. However, a bulk biased with varying signals is needed to keep the switch efficiently turning on and off for a more ideal switching. The idea proposed in this thesis is to reuse the source node voltage in a way that it would improve switching efficiency. In order to help the switch to turn on more easily, a negative $V_{BS}$ is desired to reduce the $V_{TP}$ to a minimum. On the other hand, the body effect is desired to introduce a large positive $V_{BS}$ to increase the $V_{TP}$ to a maximum in order to turn the transistor on more easily. The proposed idea is to enhance the source node signal so that it will have the dotted waveform as shown in figure 4.11. This idea can easily be applied by designing an amplifier to take $V_s$ as the input and to feed $V_B$ back to the bulk terminal as the output of the amplifier, this is referred as Design C. However, it is necessary to monitor the biasing condition of the *pn* junctions to ensure the proper working of the transistor. Since there are many components in the proposed mixer circuit, separate components will be discussed and drawn as a box in the final mixer circuit diagram for a more clear presentation. As specified in previous sections, one fundamental Gilbert mixer is tested with different bulk connections in the design. And

different bulk terminal connections in Design A, B, and C are selected and controlled by simple PMOS and NMOS switches, they will not be drawn for simplicity.

#### 4.3.3.1 The Amplifiers

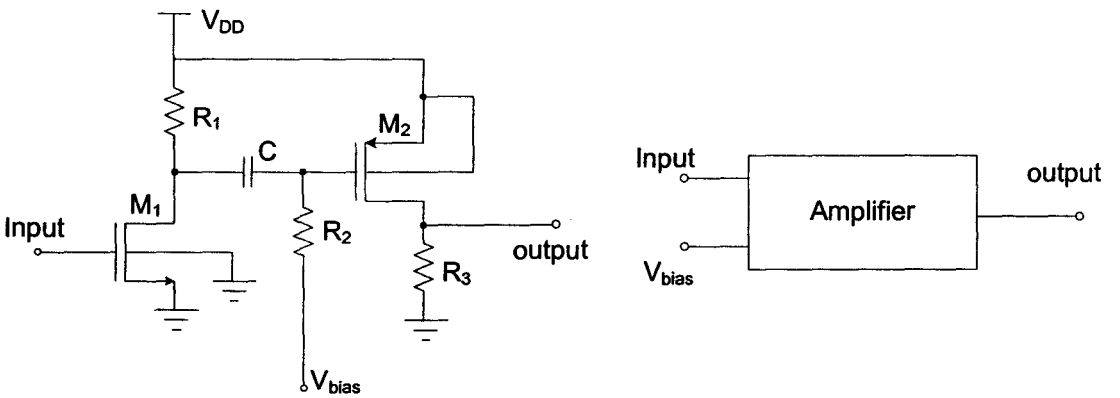


Figure 4.12: The circuit implementation of an amplifier with its simplified block diagram.

An amplifier is designed to enhance the source signal from the LO switches. The dc level of the signal must be remained to ensure the proper working of the mixer core. It can be very time-consuming to design an amplifier with a high gain, a low noise, and a high linearity characteristic. Due to the time constraints in the design process, an amplifier is designed to fulfill the purpose in generating the desired waveform as shown in figure 4.11. With the addition of the amplifier, it is expected to have a poor noise and linearity performance because of more noise sources and more nonlinear currents generated by the I-V converters. However, by improving the switching efficiency, it should be able to serve the purpose for the study of body biasing techniques. The circuit implementation of the designed amplifier is shown in figure 4.12 with the simplified

block diagram. The design parameters are shown in table 4.5. The designed amplifier is able to amplify the source node ac amplitude by four times. The input and output signal are in phase to each other. There are two same amplifiers in the Design C Gilbert mixer.

| Design parameters | Value |
|---|---|
| $R_1$ ($k\Omega$) | 1.0 |
| $R_2$ ($k\Omega$) | 2.0 |
| $R_3$ ($k\Omega$) | 4.5 |
| C (pF) | 1.0 |
| Aspect ratio of $M_1$ (W/L in um) | 2.5/0.18 |
| Aspect ratio of $M_2$ (W/L in um) | 2.5/0.18 |
| Number of fingers of $M_1$ (nr) | 2 |
| Number of fingers of $M_2$ (nr) | 16 |
| $V_{DD}$ (V) | 1.2 |
| $V_{bias}$ (V) | 0.589 |

Table 4.5: Design parameters for the amplifiers.

The amplifier from figure 4.12 is integrated into the fundamental Gilbert mixer in figure 4.6. The $B_{bias1}$ terminal is connected to the input port of the amplifier while $B_{bias2}$ is connected as an input to another amplifier. The $V_{bias}$ port is from the same node as in figure 4.6, while the output from the amplifiers feed back to the bulk terminals of the Gilbert mixer correspondingly. The same simulations are run at RF power of –25 dBm, the results are plotted in figure 4.13. In Design A and B, the output nodes are taken at the source terminal of LO transistors as in a typical Gilbert mixer. However, it is noted that the output from the amplifier is actually the amplified version of the source signals. It shows from simulations that it gives a much better performance than the results that are taken at the source terminal. NF is similar but with an increase in the conversion gain for

more than 10 dB. The conversion gain at 0 dBm LO power is recorded as 8.6 dB when the output is taken from the source terminal. Compare to Design A and B, a more efficient switching function is obtained when the rise time and fall time are reduced, the mixer shows better performance. The conversion gain from Design C has increased by 7.35 dB and 8 dB when compared to Design A and B respectively. However, the amplifiers in Design C consume more power. Even though NF performance should be improved in Design C because of the same trend as the conversion gain, the additional noise generators from the amplifiers have increased the NF by 3 dB at LO power of 0 dBm. It is necessary to emphasize that all the improvements is from the switching core of the mixer. The RF transconductor are kept constant among all three designs.

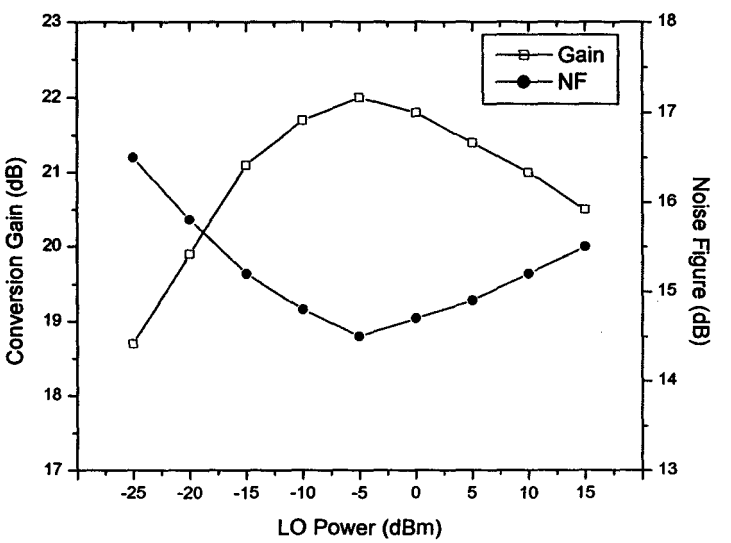


Figure 4.13: Simulation results of NF and conversion gain against LO power (Design C).

### 4.3.3.2 The Buffers

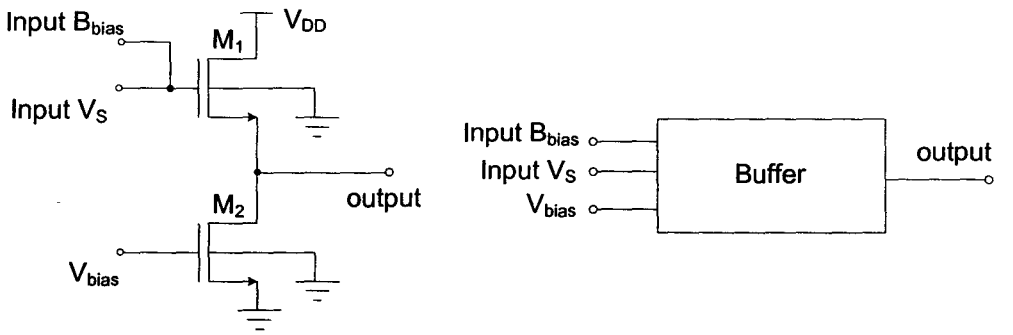


Figure 4.14: Circuit implementation of the buffer with its block diagram.

A buffer is needed for the complete mixer circuit. It is designed to delivered around 50% of the signal power to a 50 Ω load at the output port. The circuit implementation of the buffer is shown in figure 4.14 with its block diagram. The buffer $M_2$ is biased by $V_{bias}$ while input is taken at the gate of $M_1$. The input at M1 is again controlled by a switch, which is not shown in the diagram. The switch provides a choice to allow input signal to enter from the output of the amplifier or from the source terminal of the LO transistors. The complete circuit diagram of the Gilbert mixer Design C is shown in figure 4.15 as a blocked diagram, the Gilbert mixer core is the same as figure 4.6 and also shown as a block diagram. The RF and LO signal input are simplified to one input port to the main block of the Gilbert mixer core. For the block diagram of Design A, it can be regenerated from figure 4.15 with the elimination of block Amplifier+ and Amplifier-. Moreover, $B_{bias1}$ and $B_{bias2}$ are connected to the $V_{DD}$ with the buffer blocks modified to two input ports only. A block diagram for Design B can be generated with similar modifications. The layout diagram with all three configurations integrated in the

Gilbert mixer is shown in figure 4.16. The silicon space is granted with an area of 1000 by 1000 microns. It is packaged and bonded to a CMC text fixture CFP80TF for measurements.

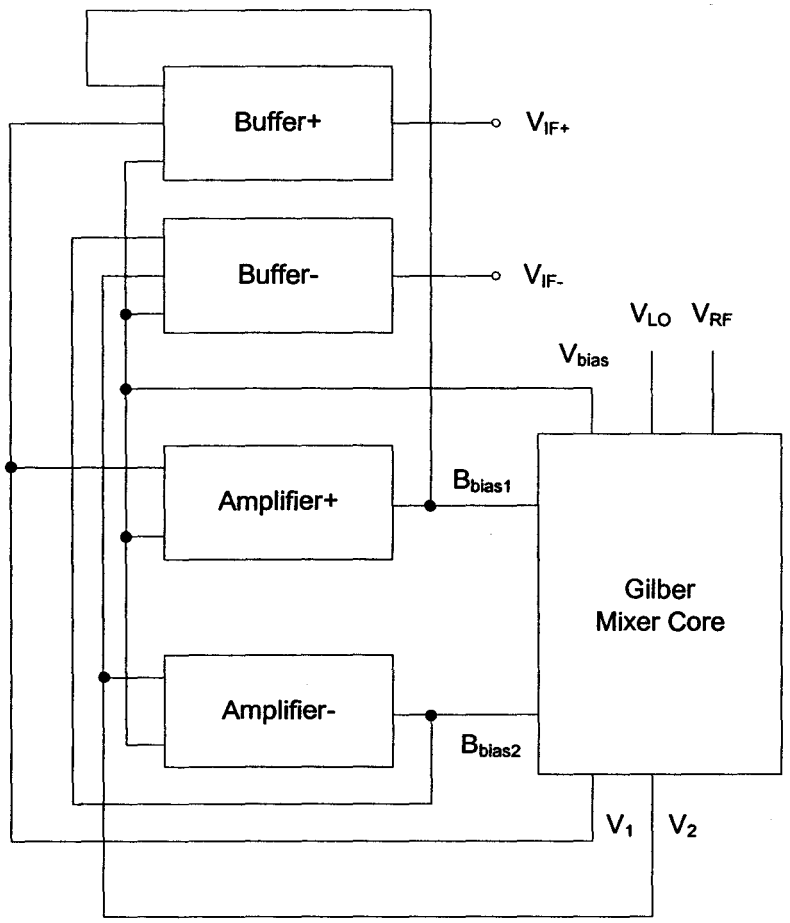


Figure 4.15: A block diagram showing the complete Gilbert mixer of Design C.

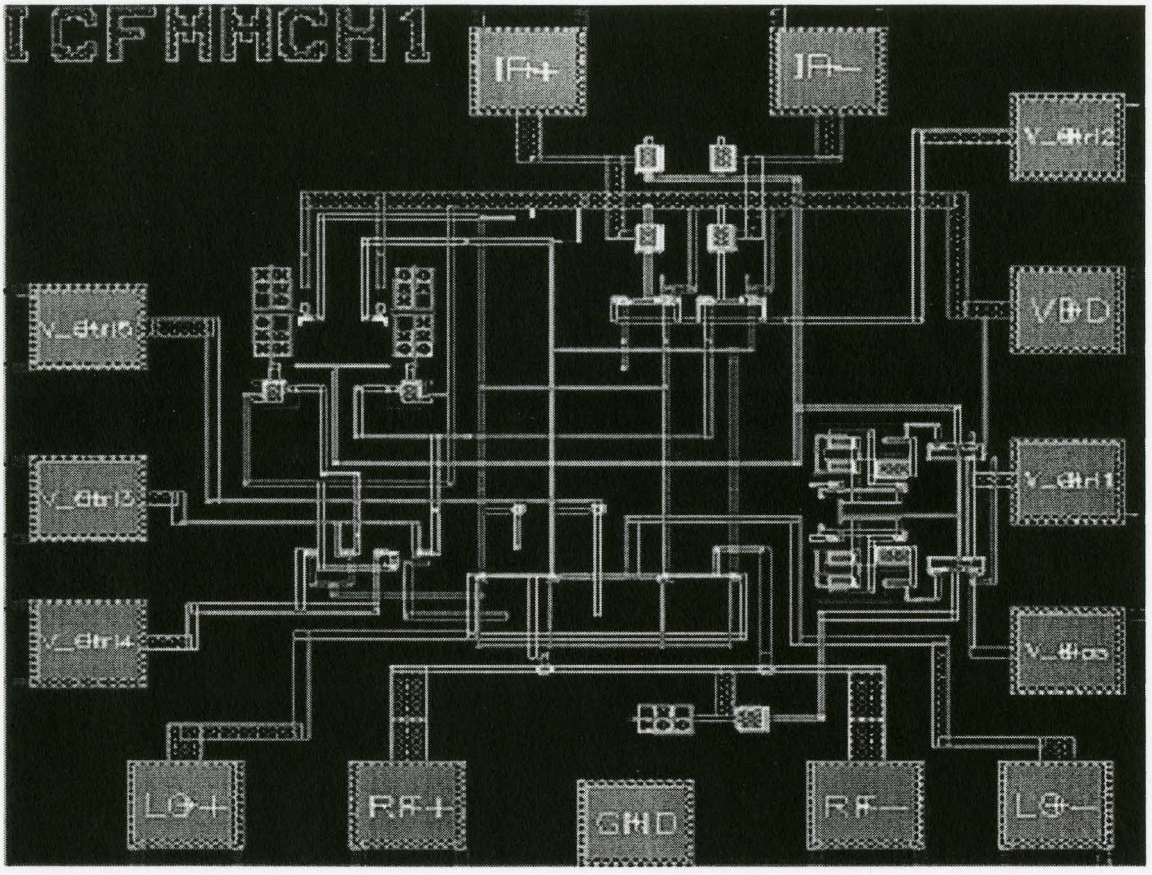


Figure 4.16: Layout diagram of the Gilbert mixer with three different configurations.

### 4.3.3.3 Simulation and Measurement Results

A complete Gilbert mixer is shown in figure 4.15. Simulations and measurement results are compared in this section. Performances are expected to degrade with the addition of buffers. Simulations are run in previous sections without the buffer in order to show the performance difference from only the mixer core. It is shown that better switching behaviors from LO transistors increase the conversion gain and NF performances. And IIP3 is also expected to increase.

Before starting any measurements, the signal loss in all cables and equipments are measured. The signal loss from the connection between the LO port and the signal generator is measured as 6.2 dB. It includes two RF cables, a splitter, and a BiasT. Due to different quality of RF cables, the signal loss in the RF signal path is measured as 4.6 dB. The elements in the RF path is the same as those in LO path. Each RF cable has a loss of 0.2 dB at IF frequency. Moreover, all RF cables are measured with the same signal loss within allowable range of input power. A cable conduct signal at higher frequency is measured with higher signal loss. Since the RF cables have different quality for signal losses, the RF cables used to connect LO port are always kept as the LO port connectors. To adjust for the loss, LO power is set as 6.2 dB higher than the simulation in order to have an accurate comparison. Output power recorded is shifted by 4.6 dB with respect to RF input power. The measured IF power is added by 0.4 dB to compensate for the signal loss from cables. As a result, the IF output power is measured with a LO power of 6.2 dBm instead of the 0 dBm from the measurement. RF is input from the range of –30.6 dBm to 9.6 dBm in the measurement instead of the range of –35 dBm to 5 dBm in the simulation.

Figure 4.17 shows the simulation and measurement results for Design A and table 4.6 summarizes the mixer performance at 0 dBm LO power and –25 dBm RF input power. The IIP3 from simulation is around –9 dBm and it is –8 dBm from measurement.

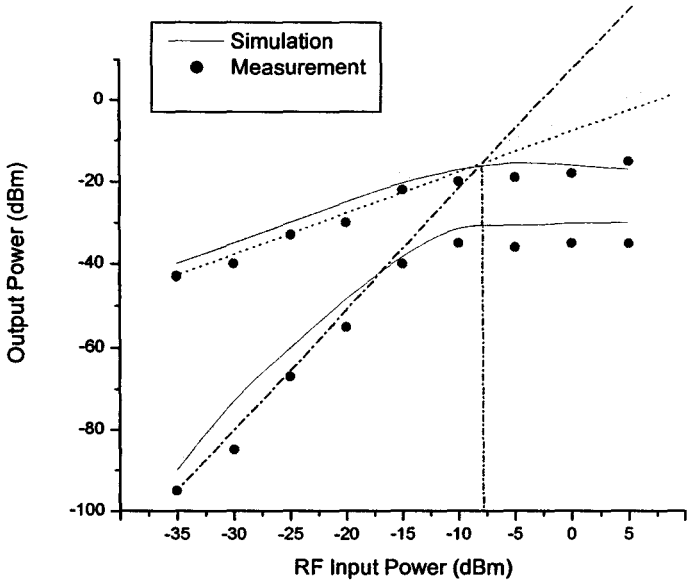


Figure 4.17: Comparison between measurement and simulation results in a two-tone IIP3 test of Mixer Design A.

| Key Parameters | Simulation Result | Measurement Result |
|---|---|---|
| Supply Voltage ($V_{DD}$) | 1.2 V | 1.2 V |
| Current Consumption | 300 uA | 295 uA |
| Conversion Gain | -4.5 dB | -7.5 dB |
| SSB Noise Figure | 12.9 dB | 13.5 dB |
| IIP3 | -9 dBm | -8 dBm |
| Power Consumption | 0.36 mW | 0.354 mW |

Table 4.6: Performance summary of mixer Design A.

Figure 4.18 shows the comparison between simulation and measurement results for Design B. Table 4.7 shows a summary on the performance of Design B.

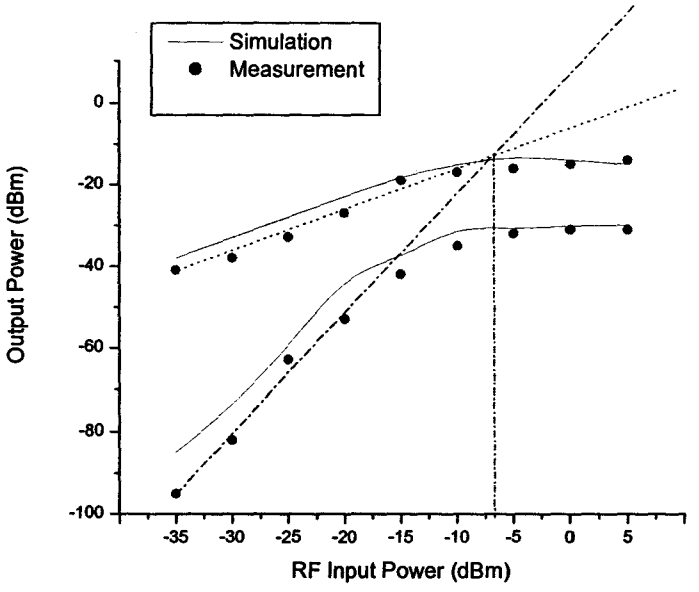


Figure 4.18: Comparison between measurement and simulation results in a two-tone IIP3 test of Mixer Design B.

| Key Parameters | Simulation Result | Measurement Result |
|---|---|---|
| Supply Voltage ($V_{DD}$) | 1.2 V | 1.2 V |
| Current Consumption | 300 uA | 296 uA |
| Conversion Gain | -4.0 dB | -6.5 dB |
| SSB Noise Figure | 12.5 dB | 13 dB |
| IIP3 | -7.5 dBm | -6 dBm |
| Power Consumption | 0.36 mW | 0.355 mW |

Table 4.7: Performance summary of mixer Design B.

Figure 4.19 shows the comparison between simulation and measurement results for Design C, while table 4.8 shows a summary on the performance of Design C.

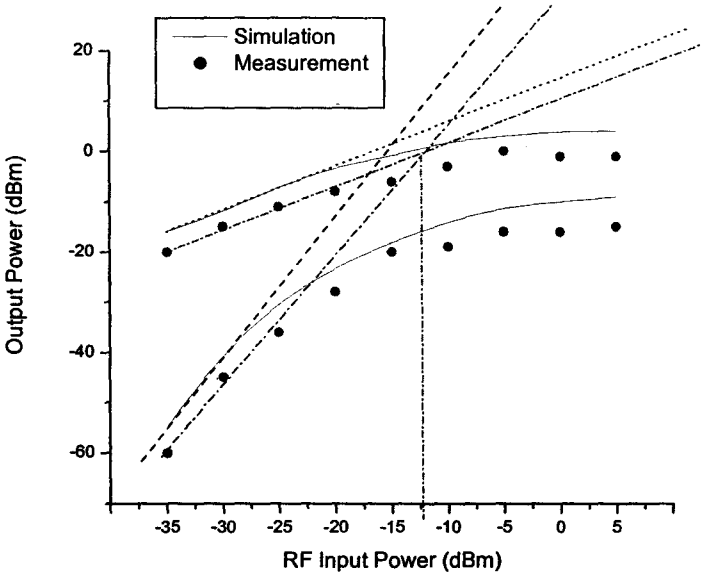


Figure 4.19: Comparison between measurement and simulation results in a two-tone IIP3 test of Mixer Design C.

| Key Parameters | Simulation Result | Measurement Result |
|---|---|---|
| Supply Voltage ($V_{DD}$) | 1.2 V | 1.2 V |
| Current Consumption | 1.7 mA | 1.65 mA |
| Conversion Gain | 18 dB | 14.5 dB |
| SSB Noise Figure | 16.5 dB | 17 dB |
| IIP3 | -15 dBm | -12.5 dBm |
| Power Consumption | 2.04 mW | 1.98 mW |

Table 4.8: Performance summary of mixer Design C.

Figure 4.20 to figure 4.22 show the simulation and measurement results of NF performance in Design A, B, and C respectively.

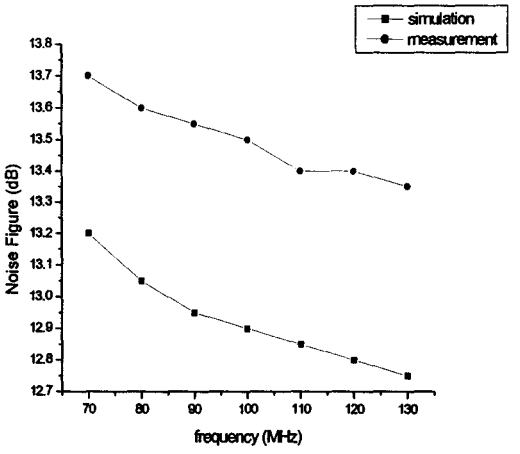


Figure 4.20: NF from Design A.

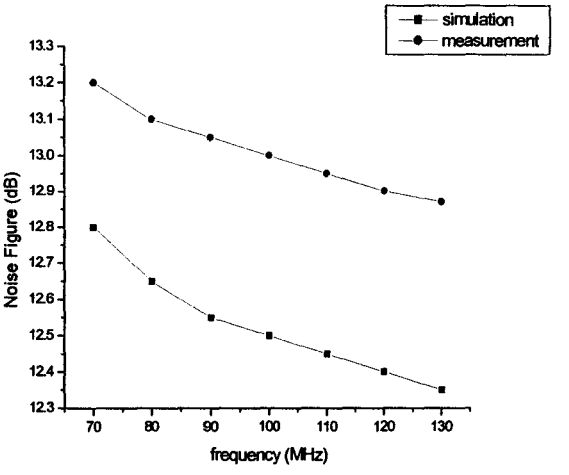


Figure 4.21: NF from Design B.

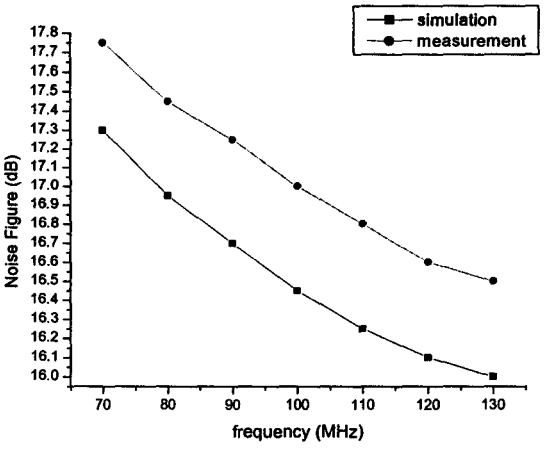


Figure 4.22: NF from Design C.

### 4.3.3.4 The Figure of Merits

The performances of Design A, B and C are compared with the most recent published designs integrated with 0.18 um CMOS process. A fair comparison can only be made if the CMOS mixers are designed with the same effective channel length and at a close input frequency. Table 4.9 summarizes the performances of those selected CMOS mixer with the measured performance of Design A, B and C.

| Row | Ref. | RF (GHz) | $V_{DD}$ (V) | Power Consumption (mW) | SSB NF (dB) | Gain (dB) | IIP3 (dBm) |
|---|---|---|---|---|---|---|---|
| 1 | [28] | 5.8 | 1.5 | 11.78 | 13.6 | 10.4 | -10.66 |
| 2 | [50] | 2.4 | 1.8 | 28.8 | 18.5 | 3.5 | 1.5 |
| 3 | [51] | 2.4 | 1.4 | 6.6 | 14 | 11 | 4.1 |
| 4 | Design A | 2.4 | 1.2 | 0.354 | 13.5 | -7.5 | -8 |
| 5 | Design B | 2.4 | 1.2 | 0.355 | 13 | -6.0 | -6 |
| 6 | Design C | 2.4 | 1.2 | 1.98 | 17 | 14.5 | -12.5 |

Table 4.9: Comparison of the performances of different 0.18 um CMOS mixers.

It can be very confusing when trying to choose a better mixer. As a result, a figure of merits (FOM) is sometimes used to rate the performances of a mixer. However, the weightings on different performance parameters have to be carefully assigned; otherwise the calculated FOM could be even more misleading. [52] recommends (4.31) in calculating FOM,

$$FOM = \sum_{i=1}^{n} w_i \frac{|p_i - p_{i\min}|}{|p_{i\max} - p_{i\min}|} \tag{4.31}$$

where $n$ is the total number of performance parameters taken into consideration. The weightings are set by $w_i$ correspondingly for each parameter $p_i$. The maximum and minimum values of the performance parameters are also considered in this equation, which are input as $p_{imax}$ and $p_{imin}$ respectively. For normal comparison, same weightings of 1 are assigned to different parameters for $V_{DD}$, power consumption, NF, gain and IIP3. The result for each entity is shown in table 4.10 with the figure of merit of corresponding design. Result shows that mixer from row 2 give the best overall performance. But for Bluetooth application, higher weightings should be placed on power consumption and supply voltage. With a heavier weightings on those two parameter, it is obvious that Design A, B and C outperform other designs. Hence, it can be seen the importance of choosing a better representative weightings.

| Row | Ref. | $V_{DD}$ (V) | Power Consumption (mW) | SSB NF (dB) | Gain (dB) | IIP3 (dBm) | Figure of Merit |
|---|---|---|---|---|---|---|---|
| 2 | [50] | 0 | 0 | 0 | 0.5 | 0.84 | 1.34 |
| 3 | [51] | 0.5 | 0.78 | 0.82 | 0.84 | 1 | 3.94 |
| 4 | Design A | 1 | 1 | 0.91 | 0 | 0.27 | 3.18 |
| 5 | Design B | 1 | 1 | 1 | 0.07 | 0.39 | 3.46 |
| 6 | Design C | 1 | 0.94 | 0.27 | 1 | 0 | 3.21 |

Table 4.10: Figure of merits for different mixers using same weightings of 1.

### 4.3.3.5 Discussions

In this thesis design, the RF transconductors are biased at the best $g_m$ for best conversion gain and NF performance. The RF stage is kept the same, while the efficiency in switching is studied by applying different signals to the bulk terminal of the LO transistors. From simulation results, the $T_{ON}$ is reduced when comparing Design C to Design B, or when comparing Design B to Design A. The reduction in the rise time and fall time of the LO transistor in Design C has resulted in a more ideal switching, which is closer to a perfect square wave switching function. The results agree with theoretical predications. The improvements from Design B to Design A has shown a better performance in the bulk biased technique.

By using the Fourier transform, similar to figure 4.4, with an overlapping $T_{ON}$ period, it shows that there is a reduction in the conversion gain with increasing $T_{ON}$, because the coefficient of the transformed function is reduced when $n$=1. Moreover, [2] and [8] have detailed analyses showing that a reduction in $T_{ON}$ reduces the noise generation from the switches. Since switches in a differential pair only contribute white noise when they are both on, a reduction of $T_{ON}$ will reduce the total noise generated at the mixer output. Hence, the simulation and measurement results from the designs agree with the theory. In addition, IIP3 increased in Design B after eliminating the body effect. A more perfect switching means the switching function from LO transistors are getting closer to a square wave. Since square wave is composed by the fundamental and the odd order harmonics, it creates less IMD3. When the switching function is more shaped like a square wave, more energy is disturbed to the odd harmonics. The odd harmonics do not

generate intermodulation distortion within the frequency of interest, so less IMD3 is generated. Design C shows an improved conversion gain when the IF is taken from the source terminal of the LO transistors. It proves continuous improvements resulted from the more efficient switching due to the varying biasing technique. However, the MOS transistors from the amplifiers introduce more noise generators and nonlinear V-I converters in the Design C. The NF and linearity performances are expected to degrade. Because of the time constraint in the design stage, there are many margins for improvement from the current amplifiers. With a more careful design in the amplifiers, a Gilbert mixer with a lower IF and a higher IIP3 can be obtained.

In conclusion, the bulk terminal biasing technique improves the switching efficient of a Gilbert mixer. It helps to reduce the $T_{ON}$ at the LO switches. The simulation and measurement results agree with theories. A Gilbert mixer with a better NF, conversion gain, and linearity is obtained.

# CHAPTER 5
# DISCUSSION AND FUTURE WORK

## 5.1 Discrepancies of Experimental Result

Comparing the results between simulation and measurement, there are some discrepancies for all three mixer designs. Some possible reasons for the differences are due to transistor mismatches from fabrication, and parasitic losses that are not accounted for in the BSIM3V3 models.

Because of the fabrication process, there are always transistor mismatches in a differential pair. The non-fully differential pair leads to performance discrepancies between the simulation and measurement results. Since simulators assume perfect match transistors during simulations, the results obtained are for ideal cases. A mismatch in a differential pair leads to more signal feedthrough, and a non-symmetric switching function from the LO drive. Hence, the NF, linearity and conversion gain performances will be worsen in the measurement results.

The parasitic loss due to the intrinsic capacitance and resistance from transistors have always been a difficult issue for RF IC design. When transistors are operating at higher frequency, the parasitic capacitance degrades the performance of mixers even more severe. In order to obtain more realistic simulation results to match the measurement results, all the parasitic loss from the circuit elements have to be taken into consideration if they are not included in the simulator models.

There is a range of 2.5-3.5 dB differences in conversion gain between simulation and measurement results. The NF performance has a discrepancy of around 0.4–0.6 dB, while the IIP3 has a difference of 1-2.5 dBm. It is noticed that the current consumption is measured with a smaller quantity than from simulation. It makes sense because a smaller current consumption in the design means the RF transistors are not biased at the best $g_m$ which leads to lower conversion gain and higher NF. When the RF transistors are biased closer to the threshold voltage, IIP3 is expected to increase because of a lower $g_m''$. The measured current consumption is around 2-3% less than the simulation. A smaller current consumption is possibly due to a higher resistance in the resistor resulted from the fabrication process. Resistance of 3% higher than the designs are used to re-simulations, which is within the error percentage that is stated in the TSMC specification handbook. Results obtained match more to the measurement results. Hence, the resistors are not fabricated as the designed values and lead to performance discrepancies.

Even though there are some discrepancies between the measurement and simulation results, it is close enough for a valid comparison. Moreover, the trends of the results are the same, which shows the sources of error are persistence. As a result, the measurement results serve the purpose to prove and match with the simulation results. Experimental setups for measuring IF output power using one-tone test is shown in figure 5.1 for obtaining the conversion gain of the mixer. While the two-tone test are shown in figure 5.2 for measuring the IIP3 of the mixer under test. On the other, noise figure measurement are shown in figure 5.3 and figure 5.4 respectively.

## 5.2 Optimizations of the Designs

Design A is just a typical Gilbert mixer serving as the fundamental for performances comparison with Design B and C. Design B has improved the performances without any extra power consumption. It has extremely low power consumption with a moderate SSB NF and IIP3, which maybe suitable for low power applications. Design C has low power consumption with a high conversion gain and acceptable linearity and NF performances. However, there are ways to improve the design to obtain a higher IIP3 and lower NF. With the varying biasing technique applied to Design C, the performance from switching core is almost optimized. However, one possible area to improve the NF is to eliminate the dc current through the LO switches, since flicker noise is generated due to the dc current. White noise generation is minimized with the bulk-biased technique because the $T_{ON}$ is minimized. Even though the switching core is optimized, there are rooms for improvement at the RF transconductance stage. One tradeoff is to bias the transistor at a lower $V_{GS}$ in order to obtain better linearity. However, the NF and conversion gain performances are expected to degrade. A better approach to increase IIP3 in Design C without suffering performance loss is to apply the technique [53] by using multiple gated transistors (MGTR) combined with cascode configuration at the RF transconductors. The MGTR effectively reduces $g_m''$ almost to zero, and with the cascode configuration, the measured IIP3 increases by 10 dBm without sacrificing the conversion gain and NF performance.

## 5.3 Future Work

In order to compare the performance improvements between Design B and Design C, a low noise and highly linear amplifier is needed. It is believed that Design C can have a better performance if a better amplifier is designed.

For a better result matching between the simulations and measurements, the exact value of circuit elements after the fabrication process is needed. In the case of this mixer, the small difference in resistance of the resistors result in performance differences between the simulations and experiments. For low voltage low power designs, a small fluctuation from the designed operating condition can lead to circuit nonfunctioning.

Even though the bulk biasing techniques are applied to a Gilbert mixer, it is feasible to be applied to other mixers. It is interesting to compare the performance improvements when applying the techniques to folded mixer. It is also possible to have another more effective way to bias the bulk terminal.

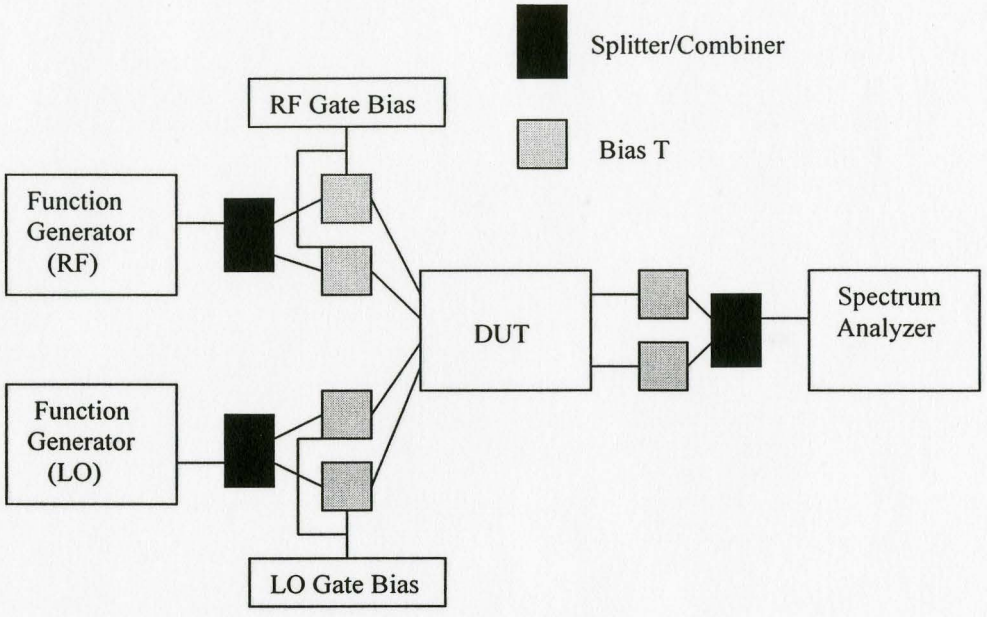


Figure 5.1: Test setup for the conversion gain measurement.

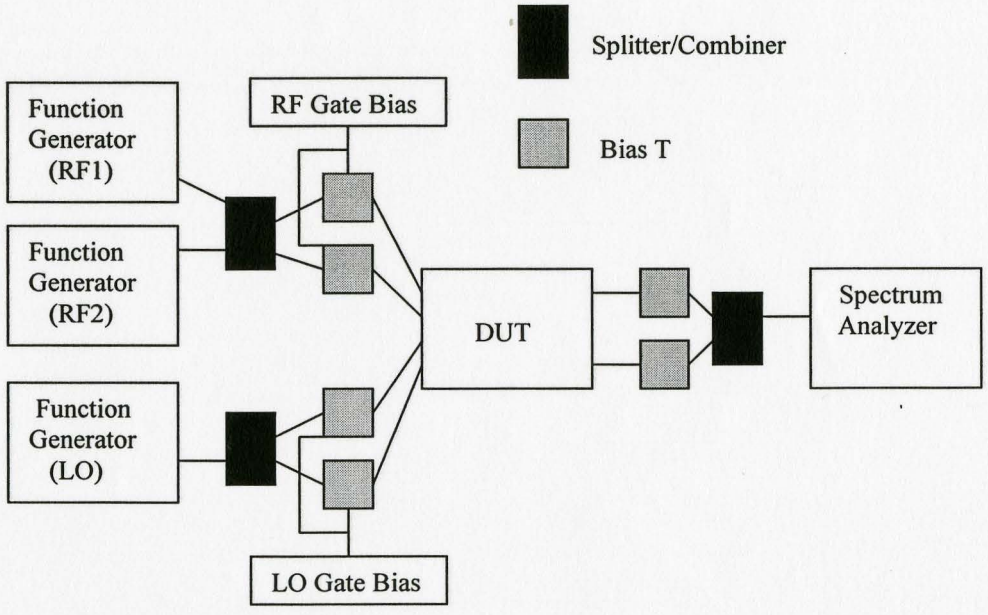


Figure 5.2: Test setup for the IIP3 measurement.

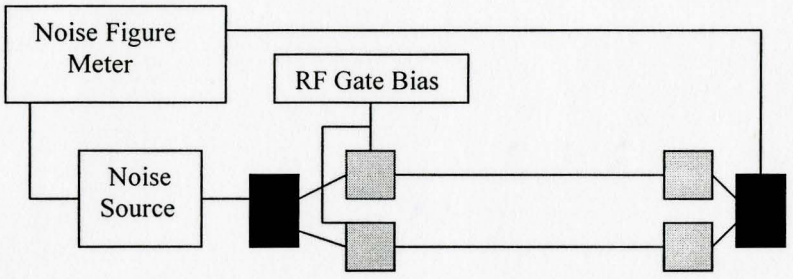


Figure 5.3: Test setup for system calibration before noise figure measurement.

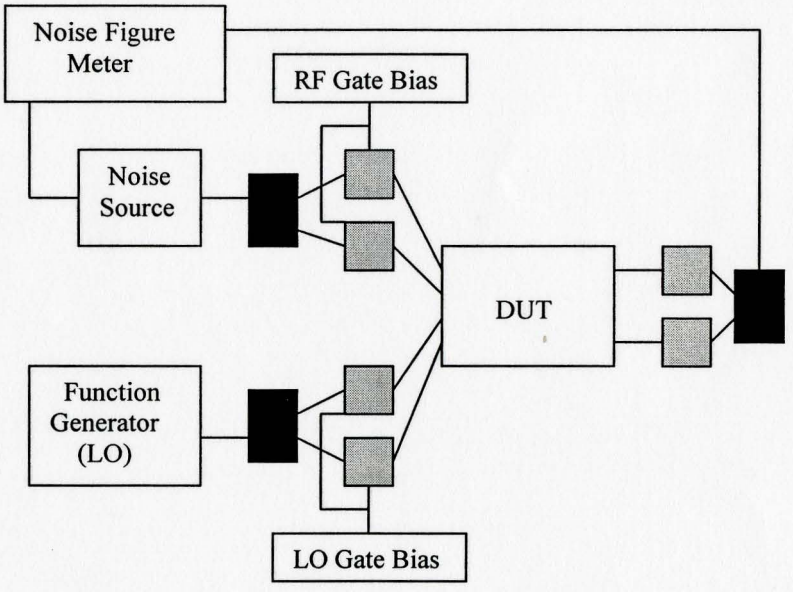


Figure 5.4 Test setup for noise figure measurement.

# CHAPTER 6
# CONCLUSION

A Gilbert mixer with three different bulk terminal connections are designed to operate at 1.2 V voltage supply for low power Bluetooth applications. Three designs are used to examine the benefits with different body biasing techniques applied on a typical CMOS Gilbert mixer. PMOS transistors are used to realize the LO switches because of a lower noise generation and lower manufacturing cost.

Design A serves as the fundamental for performances comparison with Design B and C. The RF transconductor is biased for the best conversion gain and NF with the designated $V_{DS}$ across the transistors. The LO switches are biased close to the threshold voltage at dc. However, in the transient operation with the ac LO drive, the body effect is introduced to cause a fluctuation in the threshold voltage as a function of $V_{SB}$. Design B is measured and simulated to have better performances than Design A at no extra cost of power consumption. Design B is applied with a no body effect technique to help switches turning on more easily. The elimination of the body effect also helps the LO biasing to be closer to the threshold voltage over the LO period. It shows to reduce the rise time when the LO transistor of a differential pair is turning on completely to support the total current at one branch at the RF port. Attempting to reduce both the rise time and the fall time in the output current characteristics, a varying biasing technique is implemented in Design C. However, the minimum $T_{ON}$ is set by the slew rate at the

common source node of the differential pair at the switching core. The parasitic capacitances from MOS transistors introduce a nonzero rise time and fall time in the switching behavior. And it is more severe at a higher operating frequency. PMOS transistors, with a lower mobility, are used as the LO switches to observe the worst-case performance from improving the switching performance of a Gilbert mixer. Design C shows a prominent improvement in the conversion gain because of a more efficient switching characteristics from the LO switches. However, a better amplifier is needed to estimate the improvements in performance from the no body effect technique to the varying biasing technique.

Design B and Design C are implemented with bulk-biased techniques and are proved to provide better performances compared with their original Design A. The results from simulations and measurements agreed with theoretical predictions. The bulk biasing techniques provide a method to optimize the switching characteristics of the mixers. Design B and Design C are both suitable for low power Bluetooth applications. While Design B is very attractive for extremely low power application with a moderate linearity and NF performance, the high conversion gain inherited from Design C made it suitable for a different receiver needs.

# REFERENCES


1. H. Darabi, S. Khorram, H.M. Chien, M.A. Pan, S. Wu, S. Moloudi, J.C. Leete, J.J Rael, M. Syed, R. Lee, B. Ibrahim, M. Rofougaran, and A. Rofougaran, "A 2.4-GHz CMOS transceiver for Bluetooth," *IEEE Solid-State Circuits*, vol. 36, pp. 2016-2024, Dec. 2001.

2. X. Fan and E. Sanchez-Sinencio, "3-22GHz CMOS distributed single-balanced mixer," *IEEE SOC Conference*, pp. 93-96, Sept. 2004.

3. A.Q. Safarian, A. Yazdi, and P. Heydari, "Design and analysis of an ultrawide-band distributed CMOS mixer," *IEEE Trans. VLSI System*, vol. 13, pp. 618-629, May 2005.

4. A.Q. Safarian and P. Heydari, "Design and analysis of a distributed regenerative frequency divider using distributed mixer," *IEEE Trans. Circuits and Systems*, vol. 1, pp. 23-26, May 2004.

5. B. Gilbert. "A new wideband amplifier technique," *IEEE J. of Solid State Circuits*, vol. SC-3, pp. 335-365, Dec. 1968.

6. T. Chouchane and M. Sawan, "A 5 GHz CMOS RF mixer in 0.18 um CMOS technology," *IEEE CCECE*, vol. 3, pp. 1905-1908, May 2003.

7. C.C. Tang, W.S. Lu, L.D. Van, and W.S. Feng, "A 2.4-GHz CMOS down-conversion doubly balanced mixer with low supply voltage," *IEEE Circuits and Systems*, vol. 4, pp. 794-797, May 2001.

8. P.J. Sulivan, B.A. Xavier, and W.H. Ku, "Low Voltage Performance of a Microwave CMOS Gilbert Cell Mixer," *IEEE Solid-State Circuits*, vol. 32, pp. 1151-1155, July 1997.

9. S. Li, J. Zohios, J.H. Choi, and M. Ismail, "RF CMOS mixer design and optimization for wideband CDMA application," *IEEE Mixed-Signal Design*, pp. 45-50, Feb. 2000.

10. X. Wang, R. Weber, and D. Chen, "A novel 1.5 V CMFB CMOS down-conversion mixer design for IEEE 802.11 A WLAN systems," *IEEE Circuits and Systems*, vol. 4, pp. 373-376, May 2004.

11. T. Manku, G. Beck, and E.J. Shin, "A low-voltage design technique for RF integrated circuits," *IEEE Circuits and Systems II*, vol. 45, pp. 1408-1413, Oct. 1998.

12. K.K Kan, K.C. Mak, D. Ma, and H.C. Luong, "A 2-V 900-MHz CMOS mixer for GSM receivers," *IEEE Circuits and Systems*, vol. 1, pp. 327-330, May 2000.

13. W.C. Cheng, C.F Chan, C.S. Choy, and K.P Pun, "A 1.5V 900 MHz CMOS current folded-mirror mixer," *IEEE ASIC*, vol. 2, pp. 1050-1053, Oct. 2003.

14. V. Vidojkovic, V.D. Tang, A. Leeuwenburgh, and V. Roermund, "Mixer topology selection for a 1.8 - 2.5 GHz multi-standard front-end in 0.18 um CMOS," *IEEE Circuits and Systems*, vol. 2, pp. 300-303, May 2003.

15. V. Vidojkovic, V.D. Tang, A. Leeuwenburgh, and V. Roermund, "A low-voltage folded-switching mixer in 0.18 um CMOS," *IEEE Solid-State Circuits*, vol. 40, pp. 1259-1264, June 2005.

16. A.N Karanicolas, "A 2.7-V 900-MHz CMOS LNA and mixer," *IEEE Solid-State Circuits*, vol. 31, pp. 1939-1944, Dec. 1996.

17. C. Kienmayer, M. Tiebout, W. Simburger, A.L. Scholtz, "A low-power low-voltage NMOS bulk-mixer with 20 GHz bandwidth in 90 nm CMOS," *IEEE Circuits and Systems*, vol. 4, pp. 385-388, May 2004.

18. G. Kathiresan, and C. Toumazou, "A low voltage bulk driven downconversion mixer core, " *IEEE Circuits and Systems*, vol. 2, pp. 598-601, June 1999.

19. P. Y.Chan, A.Rofougaran, K.Ahmed, and A. A.Abidi, "A highly linear 1 GHz downconversion mixer," *Proc. Eur. Solid-State Circuits Conf.*, pp. 210-213, 1993.

20. A.Pärssinen, R.Magoon, S. I.Long, and V.Porra, "A 2 GHz subharmonic sampler for signal downconversion," *IEEE Trans. Microwave Theory and Tech.*, vol. 45, pp. 2344-2351, Dec. 1997.

21. W.H. Toole, E.I. Masry, T. Manku, "A novel highly linear 1 GHz switched-current sub-sampling mixer," *IEEE Circuits and Systems*, vol. 1, pp. 203-206, May 1996.

22. E. Cijvat, P. Eriksson, T. Nianxiong Tan, and H. Tenhunen, "A 1.8 GHz subsampling CMOS downconversion circuit for integrated radio circuits," *IEEE Circuits and Systems*, vol. 2, pp. 65-68, June 1998.

23. J. Pihl, K.T. Christensen, and E. Bruun, "Direct downconversion with switching CMOS mixer," *IEEE Circuits and Systems*, vol. 1, pp. 117-120, May 2001.

24. T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits* Cambridge, U.K.: Cambridge Univ. Press, 1998.

25. Bosco Leung, *VLSI for Wireless Communication*, 2nd ed., Prentice Hall, 2002.

26. Manolis T. Terrovitis, "Noise in Current-Commutating CMOS Mixer," *IEEE J. Solid State Circuits*, vol.34, pp. 772-783, June 1999.

27. M. Derevlean and G. Arsinte, "CMOS RF Mixer Design - A Noise Cancellation Approach," *IEEE*, pp. 245-248, 2003.

28. Joel Phillips and Ken Kundert, "Noise in Mixers, Oscillators, Samplers, and Logic. An Introdution to Cyclostationary Noise," *IEEE Custom Integrated Circuits Conference*, pp. 431-438, 2000.

29. Chris. D. Hull and Robert G. Meyer, "A Systematic Approach to the Analysis of Noise in Mixers," *IEEE Trans. Circuits and Systems*, vol. 40, pp. 909-919, Dec. 1993.

30. Wei Yu and Bosco Leung, "Noise Analysis for Sampling Mixers Using Stochastic Differential Equations," *IEEE Trans. Circuits and Systems*, vol. 46. pp. 699-704, June 1999.

31. A.S. Porret, T. Melly, D. Python, C. C. Enz, and E. Vittoz, "An analysis of Flicker Noise Rejection in Low-Power and Low-voltage CMOS Mixer," *IEEE J. Solid State Circuits*, vol. 36, pp. 546-563, Jan 2001.

32. H. Darabi and A. Abidi, "Noise in RF CMOS mixers: A simple physical model," *IEEE J. Solid-State Circuits*, vol. 35, pp. 772-783, Jan. 2000.

33. E. Sacchi, I. Bietti, S. Erba, T. Tee, P. Vilmercati, R. Castello, "A 15 mW, 70 kHz 1/f corner direct conversion CMOS receiver," *IEEE Custom Integrated Circuits Conference*, pp. 459-462, Sept. 2003.

34. T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits* Cambridge, U.K.: Cambridge Univ. Press, 1998.

35. P. Li and L.T. Pileggi, "Nonlinear distortion analysis via linear-centric models," *Design Automation Conference*, pp. 897-903, Jan. 2003.

36. S. A. Maas, "How to model intermodulation distortion," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 1, pp. 149-151, 1991.

37. M.T. Terrovitis, and R.G. Meyer," Intermodulation distortion in current-commutating CMOS mixers," *IEEE Journal of Solid-State Circuits*, vol. 35, pp 245-263, Oct. 2000.

38. M.S. Yang, H.R. Kim, and S.G. Lee, "A 900MHz low voltage low power highly linear mixer for direct-conversion receivers," Circuits and Systems, vol. 3, pp. 974-997, Dec. 2003.

39. Peng, P. J. McCleer, and G. I.Haddad, "Nonlinear models for the intermodulation analysis of FET mixers," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 1037-1045, May 1995.

40. B. Razavi, *RF Microelectronics*, Prentice Hall, NJ: 1998.

41. P. Sivonen, A. Vilander, and A. Parssinen, "Cancellation of Second-Order Intermodulation Distortion and Enhancement of IIP2 in Common-Source and Common-Emitter RF Tranconductors," *IEEE Trans. Circuits and Systems*, vol. 52, no. 2, pp. 345-352, Feb. 2005.

42. D. Manstretta, M. Brandolini, and F. Svelto, "Second-order distortion mechanisms in CMOS downconverters," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 394-406. Mar. 2003.

43. M. Brandolini, P. Rossi, D. Manstretta, and F. Svelto, "Toward multistandard mobile terminals - fully integrated receivers requirements and architectures," *IEEE Trans. Microwave Theory and Techniques,* vol. 53, pp. 1026-1038, March 2005.

44. Y.Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed. New York: McGraw Hill, 1999.

45. C. Tunasar and J. Rajgopal, "User's Manual for GPGLP - A Posynomial Geometric Programming Solver," *Technical Report No.* TR95-11, Department of Industrial Engineering, University of Pittsburgh, Pittsburgh, PA.

46. The MOSEK optimization toolbox for MATLAB, User's Guide and Reference Manual, rev. 51.

47. J. Rajgopal, "An Algorithm for Solving the Posynomial GP Problem, Based on Generalized Linear Programming," *Technical Report No.* TR95-10, Department of Industrial Engineering, University of Pittsburgh, Pittsburgh, PA.

48. M. Hershenson, S.P. Boyd, and T.H. Lee, "Optimal design of a CMOS op-amp via geometric programming," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 20, pp. 1-21, Jan. 2001.

49. Q. Huang, F. Piazza, P. Orsatti, and T. Ohguro, "The impact of scaling down to deep submicron on CMOS RF circuits," *IEEE Solid-State Circuits*, vol. 33, pp. 1023-1036, July 1998.

50. W. Hioe, K. Maio, T. Oshima, Y. Shibahara, T. Doi, K. Ozaki, and S. Arayashiki, "0.18-um CMOS Bluetooth analog receiver with -88-dBm sensitivity." *IEEE Solid-State Circuits*, vol. 39, pp. 374-377, Feb. 2004.

51. E. Klumperink, S.M. Louwsma, G. Wienk, and B. Nauta, "A CMOS switched transconductor mixer," *IEEE Solid-State Circuits*, vol. 39, pp. 1231-1240, Aug. 2004.

52. C. Yu and J.S. Yuan, "Linearity and power optimization of a microwave CMOS Gilbert cell mixer," *The 11th IEEE International Symposium on Electron Devices for Microwave and Optoelectronic Applications*, pp. 234-239, Nov. 2003.

53. T.W. Kim, B. Kim, and K. Lee, "Highly linear RF CMOS amplifier and mixer adopting MOSFET transconductance linearization by multiple gated transistors," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 107-110, June 2003.