MULTIPHASE POWER ELECTRONIC CONVERTERS FOR ELECTRIC VEHICLE MACHINE DRIVE SYSTEMS

MULTIPHASE POWER ELECTRONIC CONVERTERS FOR ELECTRIC VEHICLE MACHINE DRIVE SYSTEMS

BY

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Abstract

The past few decades have seen a rapid sales increase and technological development of electric vehicles (EVs). As the key part of the electrical power train systems, the traction machine drive systems in modern EVs are composed of voltage source inverters (VSI) and electric machines. In this thesis, multiphase VSIs are studied and designed to achieve volume reductions when compared with existing 3-phase benchmark VSIs.

Different existing switching strategies for arbitrary phase number multiphase VSIs are investigated resulting in an understanding of best practice and a newly proposed switching strategy. Thus, the first contribution of this thesis are switching strategies that support subsequent investigations and experimental validation.

DC-link capacitor and heat sink are two bulkiest components in VSIs and hence it is more efficient to decrease their volumes to achieve the compactness improvement. The investigation methodology and procedure for arbitrary phase number VSI DC-link capacitor requirements, i.e. capacitance and RMS current ratings, are firstly developed. Increased phase number decreases the DC-link capacitor requirements and hence the VSI volume significantly. Throughout this analysis, the connected multiphase machine is considered appropriately, though no electric machine design is described in the thesis. While other authors have studied DC-link current ripple, this thesis qualifies and quantifies the system benefits. This is the second contribution.

Multiphase VSIs thermal models are built and their respective thermal performances studied and evaluated against a reference 3-phase benchmark VSI. The power loss deviation among different semiconductor dies is lower or even eliminated in the multiphase VSIs. Furthermore, the multiphase integrated design VSIs have a significant heat sink volume reduction when compared to the 3-phase benchmark VSI. This study and concluding benefits are the third contribution. Finally, comparative test validations are made on an experimental set-up designed to illustrate the benefits of a 9-phase against a reference 3-phase system. Here, the test hardware and implementation are carefully designed to representatively illustrate performance benefits.

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Acknowledgments

I would like to express my deeply appreciation to Dr. Nigel Schofield. Thanks to his supervision, patience and kindness.

I would also like to thank the other members from the Department of Electrical and Computer Engineering who give me supports to finish this thesis.

I would also like to express my deeply love to my parents and hometown.

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Declaration of Academic Achievement

No portion of the work referred to in this thesis has been submitted in support of an application for another degree or qualification of this or any other place of learning.

Chapter 1

Introduction

1.1 Electric Vehicle and Associated Power-train Development

Public concerns of increasing global environmental problems, the depletion of fossil fuel reserves and global warming problems, partially introduced by conventional internal combustion engine (ICE) vehicles, has motivated research and development into electric vehicles (EVs) containing battery electric vehicles (BEVs) and hybrid electric vehicles (HEVs) etc. as proposed solutions [1]–[4]. In 2016, global EV sales reached 2.0 million, as depicted in Figure 1.1 [5] showing the total EV sales distribution by country, the total BEVs and BEVs plus plug-in hybrid EVs (PHEV). China accounts for the highest share, almost one third of the global stock, followed by the United States. The data is primarily based on the cumulative sales of BEVs and PHEVs since 2005 [5]. This rapid and increasing demand for EVs motivates continuing research and development into EVs and EV power-trains.

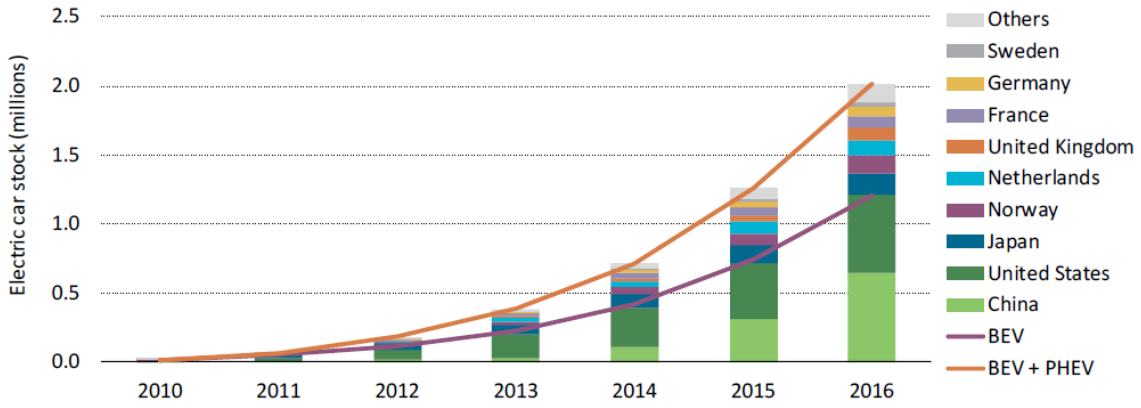
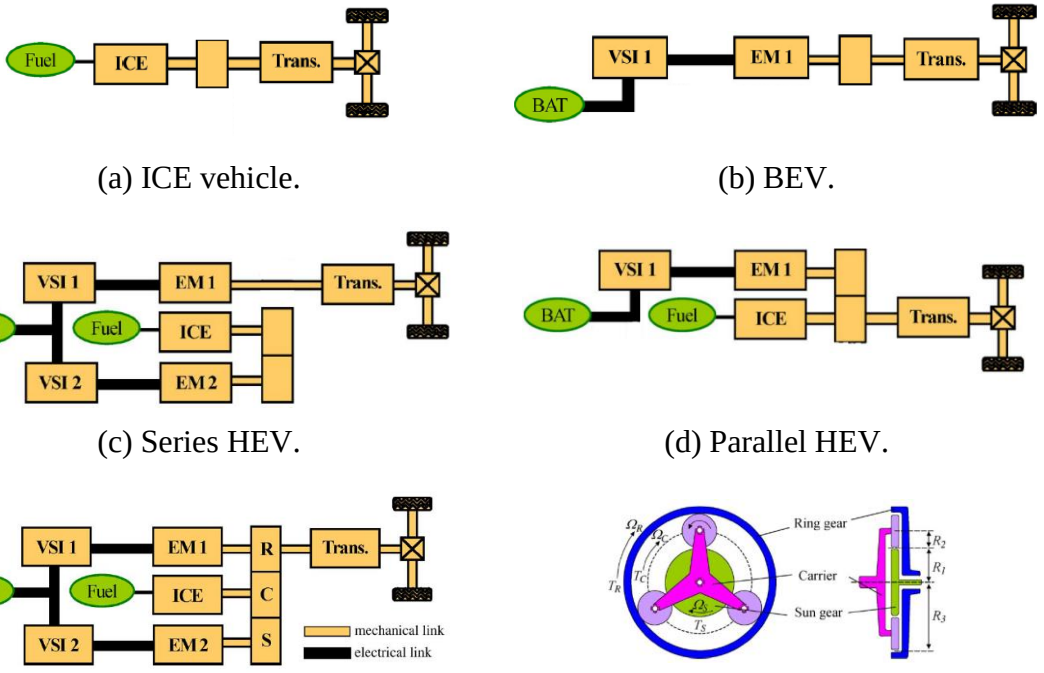


Figure 1.1 Global EV sales [5].

To generate the mechanical power to the road surface from fossil fuels like gasoline or diesel (in ICE vehicles) or electric power sources (in BEV or HEVs), power-train systems are critical to vehicles. Different power-train architectures have been proposed for EVs and HEVs, some of which are shown in Figure 1.2. As a means of comparison, the ICE vehicle power-train is shown in Figure 1.2 (a), the BEV in Figure 1.2 (b), the series and parallel HEVs in Figure 1.2 (c) and Figure 1.2 (d) respectively, an example of a series-parallel HEV power-train in Figure 1.2 (e) that implements the planetary gear set shown in Figure 1.2 (f) [6].

As well as the mechanical aspects of the power-train, there is potential to implement a diverse range of electrical energy sources, i.e. batteries, flywheels, fuel cells, and super/ultra-capacitors, to increase the design flexibility and enhance vehicle performances and capacities under different driving conditions [1]–[3]. Simplified schematics of a number of possible power-train architectures are shown in Figure 1.3.



(a) ICE vehicle.

(b) BEV.

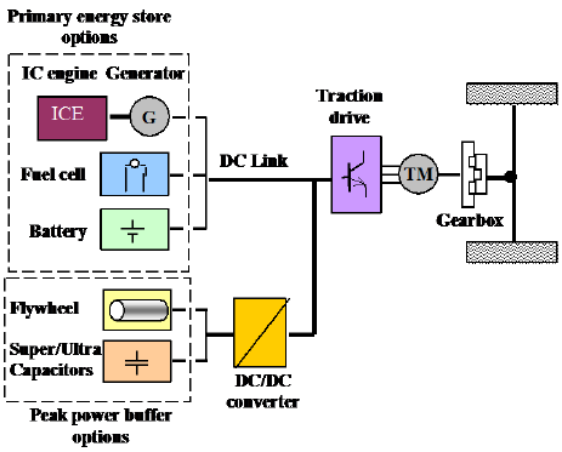
(c) Series HEV.

(d) Parallel HEV.

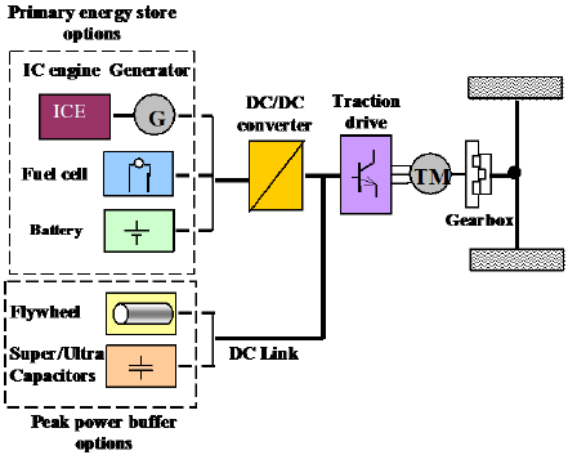
(e) Series-parallel HEV with planetary gear.

(f) Planetary gear set.

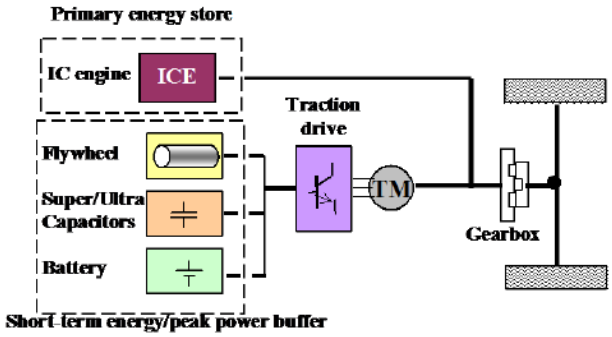
Figure 1.2 Different power-train architectures [6].



(a) Series; DC-DC converter interfaces peak power buffer to DC-link.



(b) Series; DC-DC converter interfaces energy source to DC-link.



(c) Parallel; electrical system provides peak power buffer to mechanical drive-train.

Figure 1.3 The power-trains with diverse power sources [1].

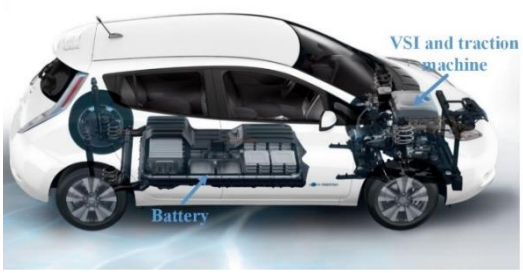
No matter what format or structure these power-train topologies take, power electronics converters are a critical element, as shown in Figure 1.3, where DC-DC converters and voltage source inverters (VSIs shown as a traction drive in the figure) interface between the various power-train elements.

With this in mind, this thesis focuses on the study, evaluation and comparison of EV VSIs, in particular multiphase VSIs. To benchmark the research the Nissan Leaf, a full EV, comprising of a 3-phase interior permanent magnet (IPM) and associated 3-phase VSI is chosen since there has already been many studies of the power-train and a wealth of public-

domain test data for validation of theoretical studies. The Nissan Leaf EV and its installed power-train are illustrated in Figure 1.4 (a) and Figure 1.4 (b), and the traction machine drive system composed of the 80 kW peak VSI and traction machine is shown in Figure 1.4 (c). The VSI is assembled on top of the traction machine. Alternatively, Figure 1.4 (d), Figure 1.4 (e) and Figure 1.4 (f) illustrate a 50 kW integrated electric machine and VSI offered by Zytek company Ltd, UK.

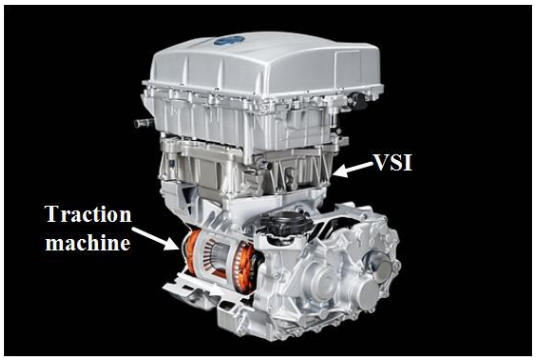
As with other vehicle power-train components, performance targets for EV VSIs have been proposed by the Advanced Power Electronics and Electric Motors R&D (APEEM), US Department of Energy (DOE). These targets, along with data quoted from various automotive manufactures are detailed in Table 1.1, specifically the VSI peak power density and peak specific power. Data for the benchmark vehicle is also given for comparisons. Clearly, the DOE targets for 2020 are some way in advance of current state-of-art VSI's (as detailed in Table 1.1).

Hence, part of the motivation of this thesis is to address the US DOE targets, thus this thesis studies two of the heaviest and bulkiest components in VSIs, the DC-link capacitor and liquid cooling heatsink [7], [8], via multiphase solutions. Moreover, system mass and volume reduction is also studied similar to the 3-phase product illustrated in Figure 1.4 (f) via an integrated multiphase VSI and traction machine design concept. Finally, the multiphase VSI is studied as an enabling component to future multiphase traction machine, the assessment of which is out of the scope of this thesis.

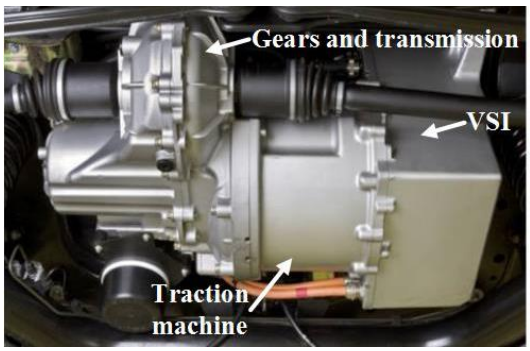


(a) Nissan Leaf power-train view 1 [9].

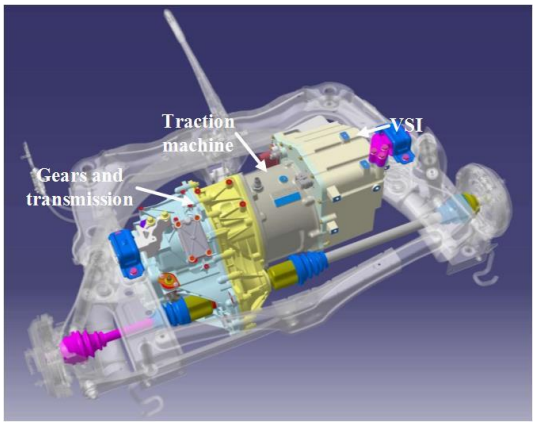
(b) Nissan Leaf power-train view 2 [9].



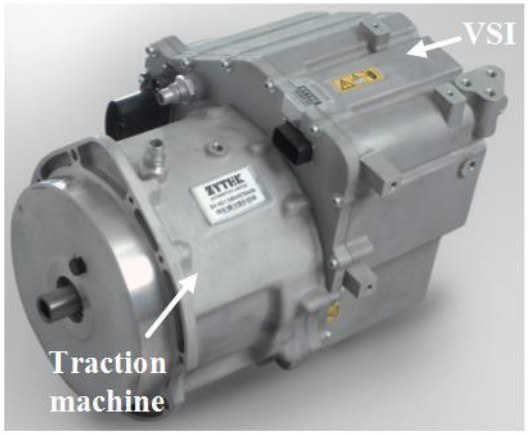
(c) Nissan Leaf machine drive system [10].



(d) Zytek power-train view 1.



(e) Zytek power-train view 2.



(f) Zytek machine drive system.

Figure 1.4 Nissan Leaf and Zytek power-trains and traction machine drives (The Zytek figures are courtesy of Dr. Tim O'Sullivan of Continental Engineering Services UK).

Table 1.1 DOE 2020 targets for EV VSIs and example systems [8], [11], [12].

	Manufacturer	Peak power density (kW/l)	Peak specific power (kW/kg)	Vehicle type
Traction machine VSI				
2010 DOE targets	-	8.7	10.8	-
2012 DOE targets	-	10	11.2	-
2015 DOE targets	-	12	12	-
2020 DOE targets	-	13.4	14.1	-
2006 Accord (12 kW)	Honda	2.9	2.4	HEV
2007 Camry (70kW)	Toyota	7.4*	5*	HEV
2008 LS600h Lexus (110kW)	Toyota	10.6*	7.7*	HEV
2010 Prius (60kW)	Toyota	5.9*	6.9*	HEV
2011 Sonata (30 kW)	Hyundai	7.3	6.9	HEV
2012 Leaf (80kW)	Nissan	5.14	4.9	EV
*Boost converter volume and mass are considered for Toyota ones.				
Traction machine				
2010 DOE targets	-	3.7	1.2	-
2012 DOE targets	-	4	1.24	-
2015 DOE targets	-	5	1.3	-
2020 DOE targets	-	5.7	1.6	-
2006 Accord (12 kW)	Honda	1.5	0.5	HEV
2007 Camry (70kW)	Toyota	5.9	1.7	HEV
2008 LS600h Lexus (110kW)	Toyota	6.6	2.5	HEV
2010 Prius (60kW)	Toyota	4.8	1.6	HEV
2011 Sonata (30 kW)	Hyundai	3	1.1	HEV
2012 Leaf (80kW)	Nissan	4.2	1.4	EV
Traction drive system				
2010 DOE targets	-	2.60	1.08	-
2012 DOE targets	-	2.86	1.12	-
2015 DOE targets	-	3.53	1.17	-
2020 DOE targets	-	4.00	1.44	-
2006 Accord (12 kW)	Honda	0.99	0.41	HEV
2007 Camry (70kW)	Toyota	3.28	1.27	HEV
2008 LS600h Lexus (110kW)	Toyota	4.07	1.89	HEV
2010 Prius (60kW)	Toyota	2.65	1.30	HEV
2011 Sonata (30 kW)	Hyundai	2.13	0.95	HEV
2012 Leaf (80kW)	Nissan	2.31	1.09	EV

1.2 VSIs for EV Traction Systems

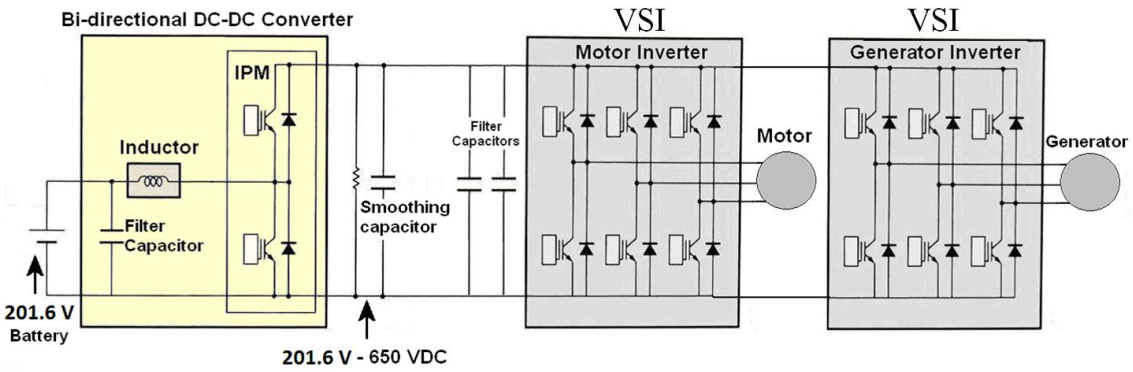
Different silicon device packaging technologies may be selected for VSIs in EV traction applications. However, the two main power electronic switching technologies used to-date are the insulated gate bipolar transistor (IGBT) and the metal-oxide semi-conductor field effect transistor (MOSFET). These technologies will be explored further in Chapter 2, but will be discussed here as part of a VSI overview.

The 2010 Toyota Prius power conversion unit (PCU) circuit schematic is shown in Figure 1.5 (a) in which there is one DC-DC converter and two VSIs, one for the traction motor and the other for the generator. The power electronic components shown in the VSI of Figure 1.5 are the commonly accepted structure for a 3-phase voltage source inverters. This system is implemented via one single integrated IGBT power module. Figure 1.5 (b) shows the system overview, Figure 1.5 (c) shows the different sub modules after teardown containing AC and DC buses, IGBTs and their drivers and controller, Figure 1.5 (d) shows the AC and DC buses and Figure 1.5 (e) illustrates the different parts of the integrated IGBT module for the traction machine VSIs and the DC-DC converter.

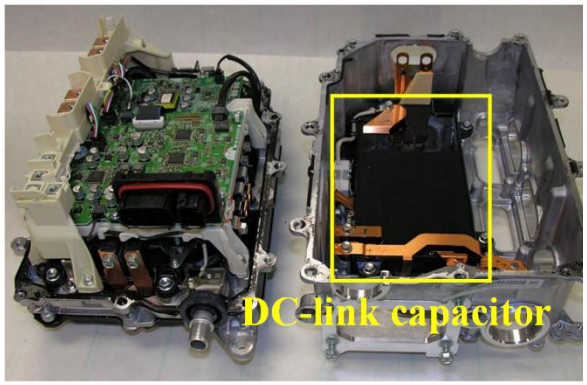
These two designs mentioned above are typical representatives for the implementations of IGBTs with two different packages, modules and discrete devices. Although the reasons that they choose different solutions for the inverter design are not declared, the design considerations must comprehensively include cost, volume (relating to torque and power density), reliabilities, etc. As to the power densities, the IGBT module integration design achieves the advances over the IGBT discrete device technology. It is the compromise among different factors whether to choose IGBT modules with higher current capability or split the current into several portions with lower rated current discrete IGBTs. In addition, the inverter structure and thermal design are application specific.

Multiple discrete IGBTs (TO-247 packages) are used in the Tesla Model S traction VSI [13]–[16] and full-bridge IGBT power modules are used in the Nissan Leaf, Honda Accord hybrid, Toyota Prius and Toyota Camry hybrid traction VSIs. Power module packaging technologies for IGBTs and MOSFETs are mature, developed and capable to hold higher power throughput than their discrete counterparts, discrete IGBT switches (as a

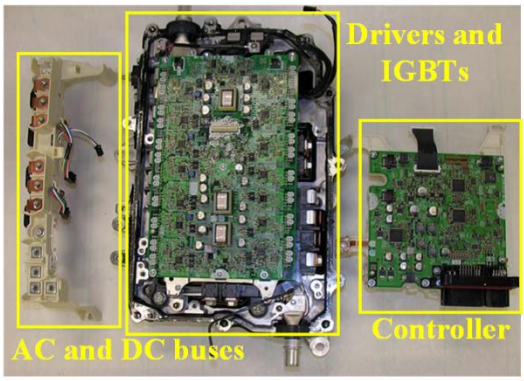
comparatively old technology) are applied in the Tesla Model S traction VSI, from a cost perspective. Although the TO-247 package discrete IGBTs are used in Tesla Model S, 14 discrete IGBTs are connected in parallel to compose one IGBT switch [13]–[16]. Hence the 320 kW 350 V DC-link voltage VSI comprises of 84 discrete IGBTs whose RMS current rating is estimated as 22 A. Figure 1.6 (a) shows the Tesla Model S 3-phase traction VSI [13]–[16] which has a prism shape, and is thus symmetrically arranged around the three surfaces of the internal cooling heatsinks. Each heatsink and power converter forms one VSI phase leg containing the discrete IGBTs, drivers and DC-link capacitors, Figure 1.6 (b). The PCB design for each phase leg is shown in Figure 1.6 (c) where 14 IGBTs are connected in parallel and 28 discrete IGBTs arranged in one phase leg. The VSI controller generating all the 3-phase control signals is mounted on the outer of the prism as shown in Figure 1.6 (b).



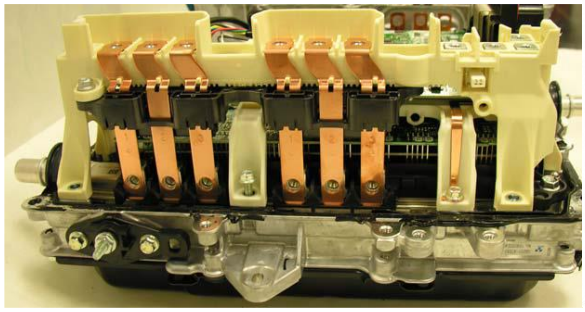
(a) 2010 Toyota Prius PCU circuit diagram [17].



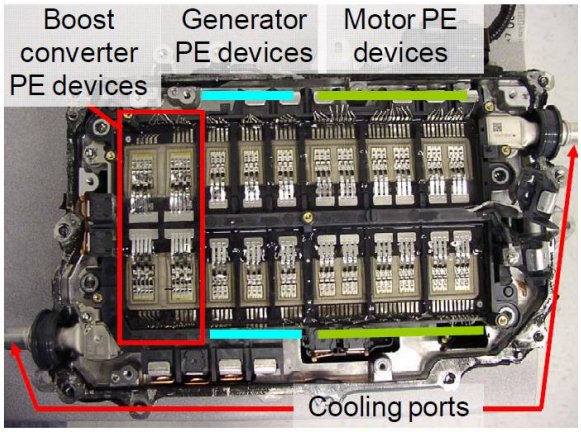
(b) System overall view.



(c) Power converter teardown.

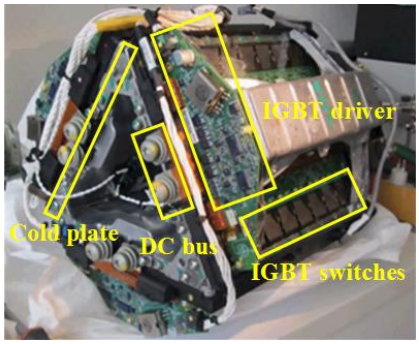


(d) AC- and DC-bus leads.

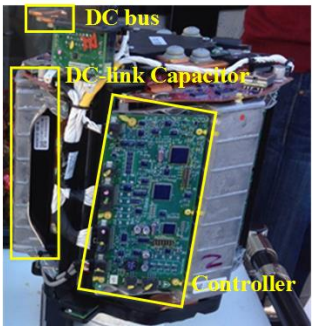


(e) Integrated power module.

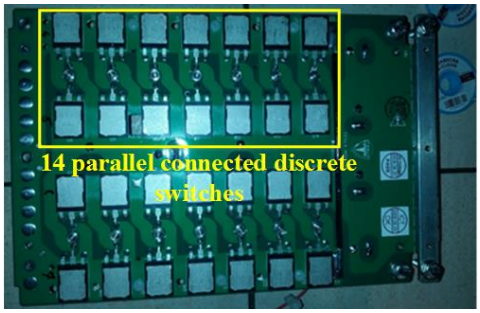
Figure 1.5 2010 Toyota Prius PCU [17].



(a) View 1.



(b) View 2.



(c) PCB board of 1 phase leg.

Figure 1.6 Tesla Model S traction VSI [13]–[16].

1.3 Multiphase Machine Drive Systems

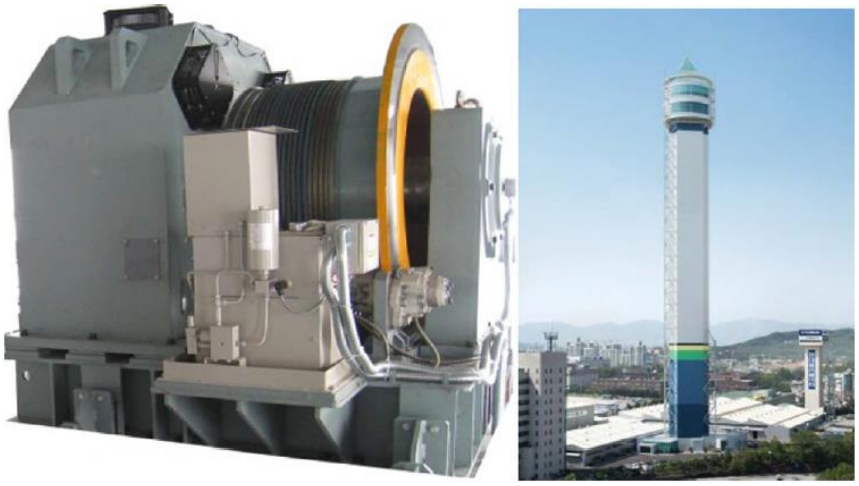
As discussed previously, most traction electric machine drive systems for production EVs and HEVs utilise 3-phase, interior permanent magnet (IPM) variable speed, electric machines [8], [11], [12], except for Tesla who uses an induction machine (IM) [18]. A number of research organisations and companies are studying switched reluctance machines, flux-switching machines, synchronous reluctance machines, though these are numerous and not referenced here. These systems are 3-phase primarily due to established industrial fixed frequency custom and practice. However, power electronic converters need not be constrained by frequency output or phase number as has been explored by a number of applications specifically at much higher powers, i.e. MW levels. Variable phase number is a main consideration of this thesis, specifically considering output flexibility and drive system hardware implementation.

Comparisons between conventional 3-phase and multiphase machine drive systems indicate that the application of higher phase numbers can reduce the per phase power handling and hence the current ratings [19]–[22], have potential for fault tolerant capabilities [20], [21], [30]–[38], [22]–[29], increase torque output and improve torque quality [20]–[22], [39], [40] etc.

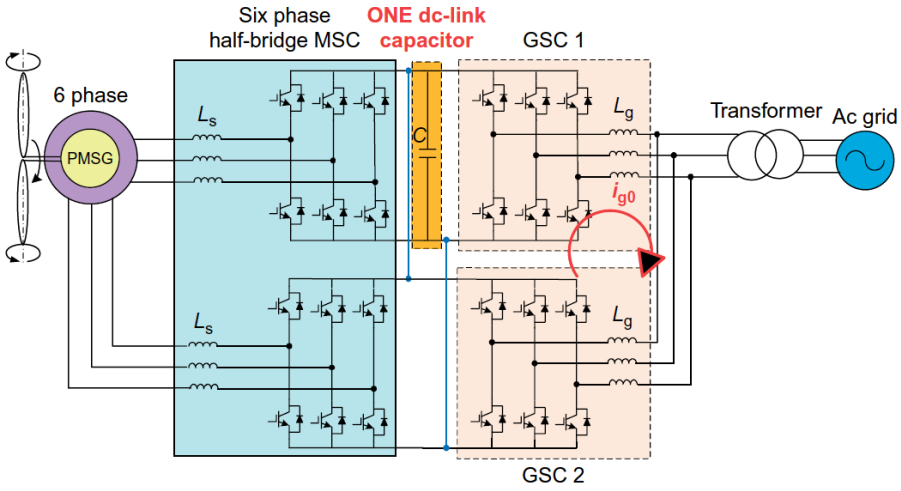
There are a number of published examples that show the different applications of multiphase machine drive systems, in [24] a 9-phase permanent magnet machine drive in ultra-high-speed elevators is discussed as illustrated in Figure 1.7 (a). In [7] a 5-phase permanent magnet motor drives for ship propulsion applications is discussed, while a 15-phase induction machine drive for ship propulsion is proposed in [41]. A multiphase permanent magnet generator for a wind energy turbines application is discussed in [42], [43], the drive system of which is as illustrated in Figure 1.7 (b).

Along with more ‘conventional’ multiphase topologies, an example of which is shown in Figure 1.8 (a), some new circuit configurations and topologies are proposed, for example, a multiphase topology with multiple single-phase units, as shown in Figure 1.8 (b), and a multiphase topology with multiple 3-phase units, as shown in Figure 1.8 (c) [44].

Figure 1.9 illustrates a 9-phase, dual inverter topology that is claimed to increase the DC-link voltage utilization and decreases the machine phase low order harmonics [45]. Multilevel, multiphase VSIs increase the choices for the multiphase systems, i.e. 3-level, 5-phase VSI [46], 3-level, 6-phase VSI [47], multiphase cascade H-bridge [21] etc. The reduction of electric machine time harmonics due to the implementation of the multilevel topology further improves the torque output quality [48].

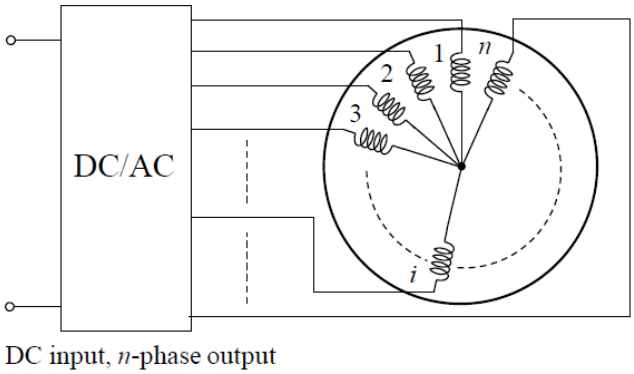


(a) 9-phase PMSM lift drive machine and the elevator test tower [24].

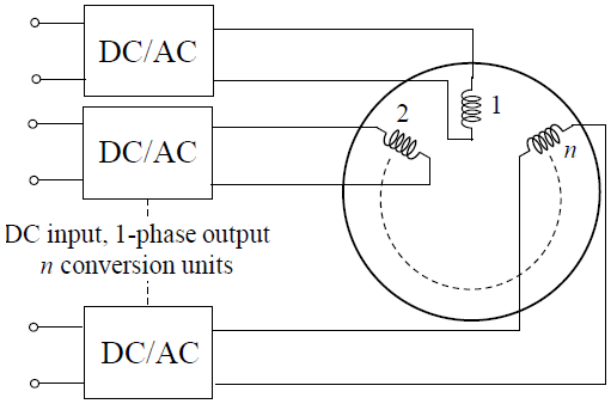


(b) 6-phase permanent magnet synchrnous generator drive for wind turbine [43].

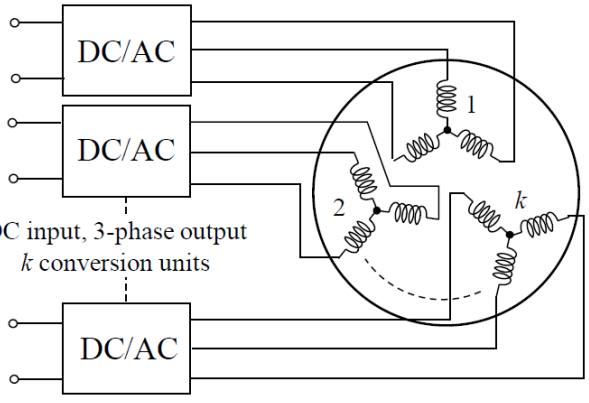
Figure 1.7 Example multiphase machine drive systems as reported in the literature.



(a) Conventional star-connected multiphase winding topology with single star point.



(b) Multiphase topology with multiple single-phase winding units.



(c) Multiphase topology with multiple 3-phase winding units.

Figure 1.8 Different multiphase machine drive system topologies as reported in the literature [44].

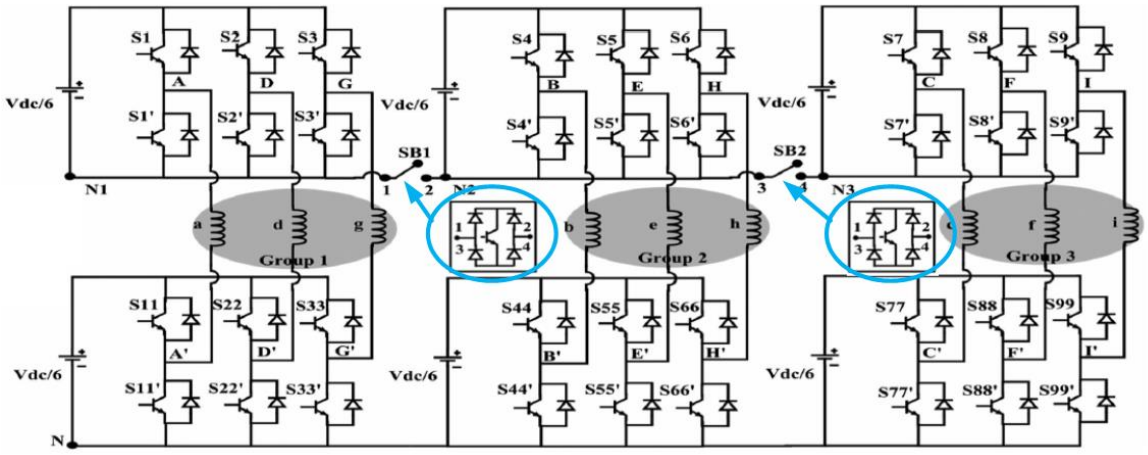


Figure 1.9 9-phase dual inverter as reported in the literature [45].

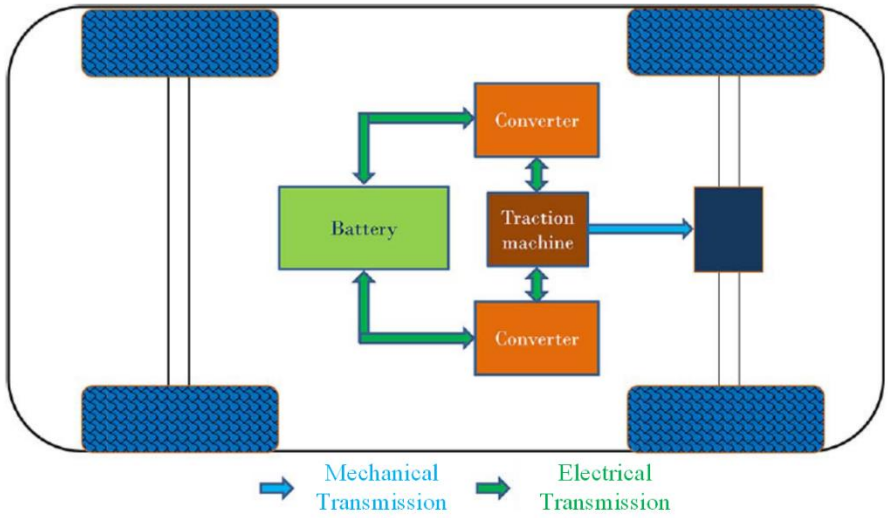
One of the key features, advantages and hence numerous studies into multiphase machine drive system topologies has been where the system requires some aspect of fault tolerance capability and faulted operation. The fault severity and classification are evaluated for inter turn faults, rotor eccentricity and magnet damage for a 5-phase permanent magnet machine via both finite element analysis and experimental validation [30]. Different stator winding faults, including open circuit, short circuit and inter-turn short circuit are introduced to a 3x 3-phase permanent magnet assisted synchronous reluctance machine, and the corresponding torque, current and thermal performances are investigated under faulty operating modes [29]. The thermal performance of a 5-phase permanent magnet machine under faulted operating conditions is investigated via both finite element analysis and experimental validation in [49]. Other papers also focus on open-circuit fault studies, i.e. [31]–[36], and short-circuit fault studies, [37], [38], for multiphase machine drives. Different measures are also proposed to enhance multiphase machine drive system fault tolerant capabilities from both the machine design side [50], [51] and the power electronic inverter side [52], [53].

In terms of EV applications, multiphase machine drive systems have been studied as part of power-train studies. A detailed comparison between 3-phase and 9-phase Brushless

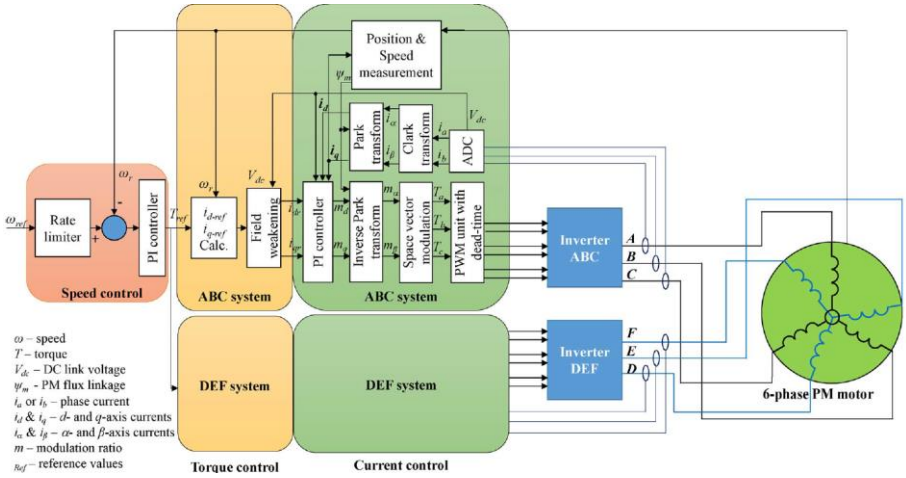
Permanent Magnet (BLPM) machine drive systems was reported in [39], while [54] gives a general view and quantitative analysis and evaluation between them. Under conditions of comparable machine stator current density and machine geometry, the adoption of a 9-phase BLPM machine drive system improves torque capability and torque quality under similar iron losses [39]. Additionally, the VSI DC-link voltage and current ripple are reduced and hence a smaller (in terms of capacitance and RMS current) VSI smoothing capacitance is required [54], [55]. Instead of the 3-phase machine drive systems, the application of the 5-phase machine drive system increases the torque output capability, decreases the torque output ripple and vibration levels etc. [56]. In [40], a 9-phase concentrated winding IPM machine design was studied and shown to decrease the stator back-EMF space harmonics, hence reduce the torque ripple and iron losses when compared to the 3-phase optimized designed counterpart with the same specifications for EV traction application. Another highly integrated 9-phase machine drive system is proposed in [57] to increase the system compactness and investigate the feasibility to replace the rare earth permanent magnet material with the ferrite magnet material. A proposed machine drive system for EVs and HEVs implemented a VSI with single chip per switch, new SiC switch technology and multiphase topology, which is claimed to decrease the DC-link capacitor size (by increasing switching frequency), system cost and power losses and introduce fault tolerance capability [58]. In another application, the EV power-train is enhanced via the application of the 2x 3-phase traction machine drive system [28] for which the undesirable stator back-EMF space harmonics are reduced, power/torque density increased and fault tolerant capability introduced. The concept vehicle power-train architecture is schematically shown in Figure 1.10 (a), while Figure 1.10 (b) shows the 6-phase machine and drive system schematic.

The adoption of multiphase machine drive system topologies may offer some new features and advances. For example, it is possible to integrate the vehicle on-board battery charger with the multiphase machine drive system as reported for 5, 6 and 9-phase system in [59]–[63] and shown schematically in Figure 1.11, an example 9-phase system. During charging

operation, the machine windings provide the series line inductance that interface to the electrical power grid.



(a) Power-train architecture.

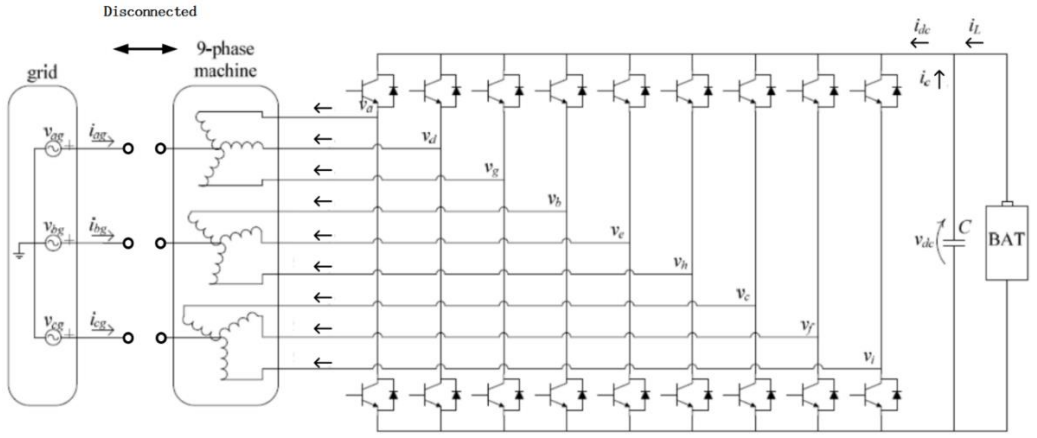


(b) Machine drive system schematic with 2x 3-phase machine, inverter and controller architecture.

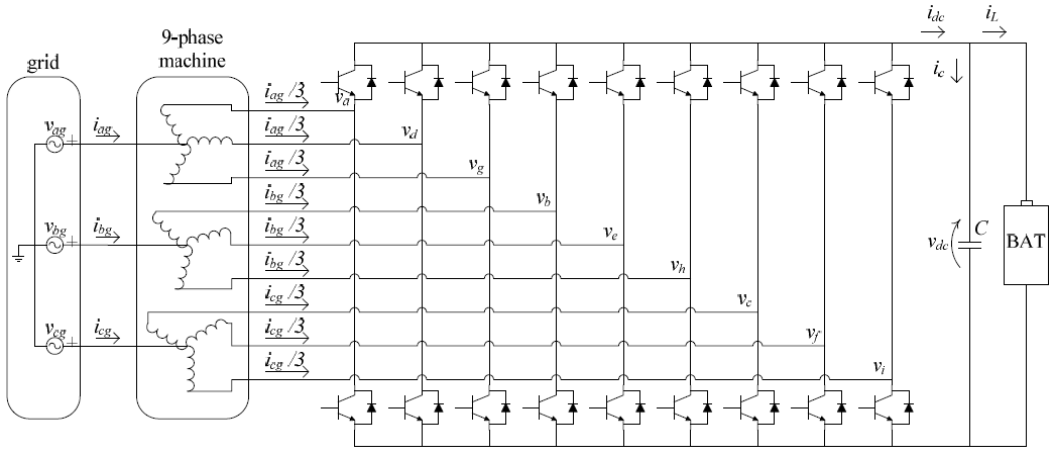
Figure 1.10 Example multiphase drive system – a 2x 3-phase traction machine drive system for an EV application [28].

Furthermore as well as conventional AC machine drive systems, switched reluctance machine (SRM) drive systems have received much interest in recent years due to the uncertainty in permanent magnet cost [64], or more specifically, the rare-earth materials. Compared with conventional AC machine drive systems, the SRM machine drive technology has some application specific advantages including the potential for low total drive system cost, machine structure robustness and simplicity, control reliability and simplicity, high efficiency, high operation speed and permanent magnet material free designs [65]–[69] etc. Thus, SRMs could be accepted as an emerging machine drive technology for EV traction application. Due to the different torque generation mechanisms, the requirements of machine inverters for SRMs are different to other AC machine technologies. Different VSIs driving SRMs are studied containing the 6-switch and 12-switch conventional SRM VSIs and the 6-switch and 12-switch toroidal SRM VSIs, of which the 12-switch SRM VSIs require twice the semiconductor devices and can be compared to the multiphase version SRM VSIs of the 6-switch ones. Hence for the sake of more comprehensive consideration, the SRM VSIs and the corresponding multiphase versions should be investigated. Also the IGBT power loss study conducted in the SRM VSIs is the same with the multiphase machine drives. For this discussion, an SRM with a conventional winding configuration as shown in Figure 1.12 (a) is referred to as the conventional switched reluctance machine (CSRM). The Toroidal Switched Reluctance Machine (TSRM) has a different winding configuration to that of the CSRM [70]–[72], having the stator coils toroidally wound on the stator back-iron, as shown in Figure 1.12 (b). Compared with CSRMs, the TSRM potentially yields better cooling and improved winding packing factor [73]. However, the different winding configuration of the TSRM leads to it having different current paths than the CSRM, requiring different commutations and power electronic converter topology [71], [72], [74]. Different power converter topologies and control strategies have been proposed for CSRM and TSRM [75]–[78]. However, the inverter performances, characteristics and the silicon device specifications of different CSRM or TSRM drive systems have not been analysed and characterised before. At the beginning of the Ph.D. study, CSRM and TSRM drive systems utilising VSIs of

different topologies, containing 6-switch CSRM VSI, 12-switch CSRM VSI, 6-swtich TSRM VSI and 12-switch TSRM VSI are studied, characterized and implemented to investigate the different multiphase VSIs for the CSRM and TSRM application. Note, the 12-swtich VSIs can be regarded as the multiphase VSIs compared with their 6-switch counterparts. Since the SR technology digresses somewhat from the main considerations of this thesis, the results of the research are presented in Appendix A1.

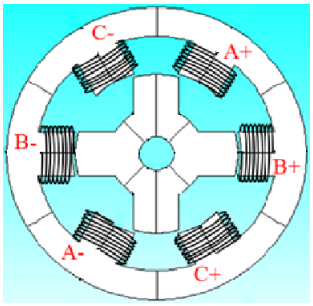


(a) Circuit schematic for traction motor operation.

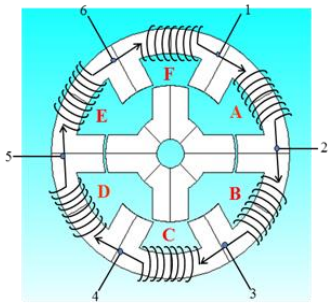


(b) Circuit schematic for 3-phase battery charging.

Figure 1.11 Power-circuit topology of the integrated 9-phase machine drive and 3-phase battery charger discussed in [60].



(a) CSRM configuration.



(b) TSRM configuration.

Figure 1.12 CSRM and TSRM configurations.

1.4 Motivations and Research Contributions

Except the multiphase machine drive system researches reviewed above, there are some other uninvestigated characteristics, advantages and design flexibilities, which could reinforce the multiphase machine drive system research and improve the EV traction machine drive system design.

These include but not restricted to:

1) The general space vector modulation (SVM) switching strategies and their feasibilities to arbitrary multiphase VSIs, the possible new switching strategies, concepts, and the best choice among different strategies
2) The VSI DC-link capacitor requirements investigation method for arbitrary phase number VSIs, the DC-link capacitor requirements comparison among different phase number VSIs and the potential advantages of higher phase number VSIs, the DC-link capacitor requirements of other new and conceptual multiphase VSIs with novel topologies and the multiphase VSI DC-link capacitor design procedure
3) The thermal performance, integrational design and other potential advantages of the higher phase number multiphase machine drives systems compared with the 3-phase counterparts.

Those are the motivations of this Ph.D. study and this thesis research contributes to:

1) The signal injection based symmetrical and discontinues SVMs feasibility is generalized to an arbitrary phase number multiphase machine drive system whose 3-phase counterpart can be implemented with these SVMs. Some new SVMs and concepts are proposed and evaluated. The best performance SVM is selected via the evaluation and comparison among different investigated SVMs considering the phase current distortion, harmonic content, and the DC-link voltage utilization.
2) The DC-link capacitor requirement investigation method is proposed for arbitrary phase number VSIs, based on which the analytical studies are conducted under different phase number VSIs to assess their DC-link capacitor requirements. The increase of the phase number decreases the DC-link capacitor requirement. Moreover, for the higher phase number systems their increased flexibilities and degrees of freedom make it possible to decrease the DC-link capacitor requirements further by the implementation of different switching schemes and carrier waveform interleaving techniques. That is based on the investigation on 2x 3-phase (one special 6-phase system), 4x 3-phase (12-phase), 2x 5-phase (10-phase), 5x 3-phase (15-phase), 3x 5-phase (15-phase), 6x 3-phase (18-phase), 4x 5-phase (20-phase), and 9x 3-phase (27-phase) VSIs. Furthermore, the new conceptual *G*x paralleled *n*-phase inner-phase pseudo-multiphase VSI (IPPM-VSI), is proposed and its DC-link capacitor investigation is studied on 2x paralleled 9-phase and 4x paralleled 9-phase IPPM-VSIs which are compared with the 9-phase VSIs. The investigation method and studies are validated by a configurable 3- and 9-phase BLPM machine drive system. Finally, the DC-link capacitor design procedure is proposed for arbitrary multiphase VSIs.
3) The mechanisms, consequences and solutions are investigated for the current and hence power loss imbalances in parallel-connected semiconductor power devices. The thermal performance is investigated for the benchmark system (the 3-phase 2012 Nissan Leaf traction system VSI) under different IGBT die power loss deviations, which is compared with the newly proposed 9-phase conventional design VSI. The thermal performance is improved in the proposed 9-phase

conventional design VSI. Moreover, the 9-phase integrated design VSI is also proposed with even better thermal performance, system power density, integration and compactness. To generalize the multiphase VSI thermal performance study, 18-phase, 27-phase and 36-phase integrated design VSIs are proposed and investigated. The implementation of multiphase VSIs improve the VSI thermal performance by eliminating IGBT die power loss imbalances and spreading the heat sources.

1.5 Thesis Structure

Chapter 1: EV developments and power-trains are briefly discussed, followed by the introduction of different commercial EV traction machine drive system VSIs. The features, advantages, design flexibilities etc. of the multiphase machine drive systems are reviewed. While some other characteristics, potential advantages and design flexibilities are not studied or proposed yet, which are the motivations for this Ph.D. thesis and the research results, outputs and conclusions in this thesis are the author's Ph.D. contributions. The thesis structure is also outlined in this chapter.

Chapter 2: Different modern power electronics devices are reviewed and investigated, which supports and links the rest of the thesis, and contributes the thesis consistency with these fundamental and general knowledge and principles.

Chapter 3: Generalized and computationally efficient multiphase space vector modulation (SVM) techniques are investigated, and some other new SVMs and concepts are proposed. The sinusoidal pulse width modulation (SPWM) is implemented as the benchmark reference. Specifically, the SVM techniques are firstly studied and implemented on a configurable surface mounted concentrated winding brushless permanent magnet (BLPM) machine in 9-phase and 3x 3-phase configurations, from which each phase is equivalent to a resistive-inductive load with rotor position dependent inductance and back-EMF with harmonic contents. The compatibility between different SVM techniques and the 9-phase BLPM machine drive system generalizes the feasibilities of SVMs to any multiphase machine drive system whose 3-phase counterpart can be implemented with SVMs. Moreover, the best choice among different SVM techniques is firstly proposed for 9-phase systems, the balanced group based 3x 3-phase SVM considering VSI phase output current harmonic contents and DC-link voltage utilization.

Chapter 4: The capacitor volume dependency on both its RMS current and capacitance ratings is studied for the DC power application, herein the VSI DC-link capacitor. The investigation method on DC-link capacitor requirements, RMS current ratings and capacitances are initially proposed and the investigation is conducted under different phase number VSIs considering different switching strategies, carrier waveforms, and

interleaving techniques. The increase of VSI phase number decrease the DC-link capacitor requirements. The more phase number systems have higher design flexibilities further decreasing the DC-link capacitor requirements via the group based interleaved carrier waveforms. Moreover, the new conceptual *G*x paralleled *n*-phase inner-phase pseudo-multiphase VSI (IPPM-VSI) is initially proposed and its DC-link capacitor requirements are studied under the 2x and 4x paralleled 9-phase IPPM-VSIs, which is compared with the 9-phase VSIs.

Chapter 5: The experimental test facility design is discussed in detail in this chapter. The configurable 3-phase and 9-phase BLPM machine are discussed and characterized. Having the same rotor, stator iron circuit and stator winding while the different winding connection configuration results in the equitable operating conditions for both the 3-phase and 9-phase BLPM machines, e.g., same copper losses and almost the same Back-EMFs. This experimental test facility is used for the validation in Chapter 3. The experimental validation method and design is introduced and the analytical study results on DC-link capacitor requirements in Chapter 4 are validated experimentally with diverse results presented in the chapter and the corresponding Appendix part. Moreover, some tests are conducted under faulted conditions in 9-phase machine drive system, followed by the fault tolerance capability discussion and analysis, supporting the fault tolerance capability statements in the previous chapters and initialize the potential future research interests.

Chapter 6: The mechanism of the current imbalance in parallel-connected power semiconductor devices, the consequences and the solutions are investigated in VSIs applications. The thermal performance is firstly studied and compared under different degrees of parallel-connected IGBT dies power loss imbalances in the benchmark 3-phase VSI. That is compared with the newly proposed 9-phase conventional design VSI nearly without the power loss imbalance due to the non-parallel connection of IGBT dies and individual current control for each phase hence each die. The 9-phase integrated design VSI is also proposed for the further improvements on the thermal performance, VSI and traction machine integration, power density and compactness. To generalize the multiphase VSI thermal study, 18-phase, 27-phase and 36-phase integrated design VSIs are proposed and

their thermal performances are studied. The multiphase VSIs can achieve better thermal performance than their 3-phase or lower phase number VSI counterparts can. This is due to the higher current controllability on each power devices and the spreading heat sources in multiphase VSI applications. Inheriting the DC-link capacitor investigation in Chapter 4 and Chapter 5, the DC-link capacitor size is decreased for higher phase number VSIs and hence VSIs power density is increased.

Chapter 7: The research outputs of the whole thesis are concluded and the future research plan is proposed in this chapter.

Chapter 2

Power Electronic Devices

2.1 Introduction

Modern power electronic converters contain semiconductor devices, passive components, cooling systems, control and protection systems etc., of which active and passive power semiconductor devices are fundamental components. In this chapter, an overview of power electronics components is made. The technical considerations for designing multi-phase VSIs are the same with those in the 3-phase VSIs. These include the rating and selection of semiconductor devices and DC-link capacitor, power losses and thermal design, DC bus mechanical design and packaging, EMI and EMC consideration etc. However each VSI design is specific in terms of the geometry and layouts.

2.2 Power Electronics Semiconductor Devices

Apart from the use of new materials, the fundamental physics and operational mechanisms of semiconductor devices have remained essentially the same since their first release, although the past few decades has witnessed improving electrical characteristics. These include higher voltage and current ratings, decreased turn-on and turn-off periods permitting higher switching frequencies, lower on-state voltage drop and conducting resistances, higher reliabilities, etc. The development of new semiconductor materials, new microelectronic designs, improved packaging design, thermal and system integration has led to continuing increases in electronic power densities, as illustrated by the data trend in Table 1.1.

Despite these improvements in silicon performances, power electronic circuit packaging is constrained by passive elements and heatsink cooling requirements that impact on total converter volume and mass.

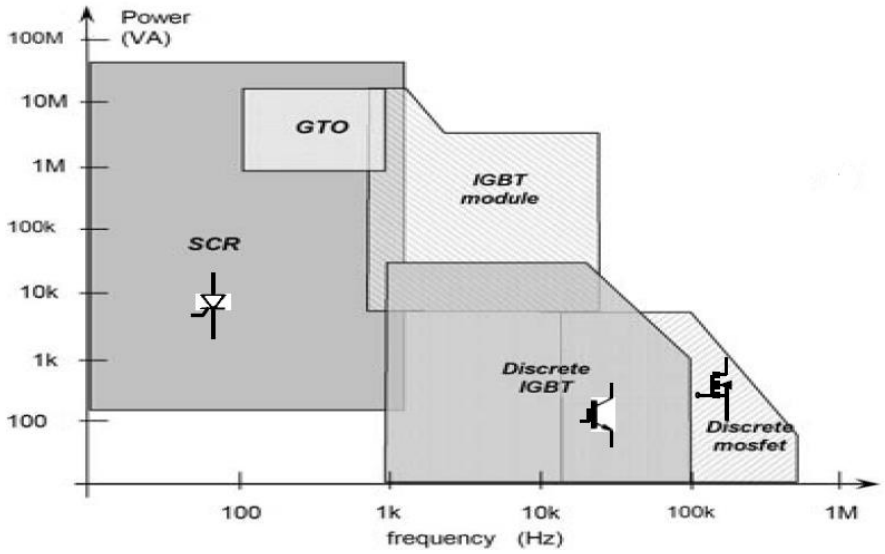
Pure semiconductor materials defined as intrinsic, with a specific electrical conductivity somewhere between ideal conductors and insulators, are doped by donor and acceptor dopants to get two different extrinsic materials, n-type and p-type, which have more electrons than holes and more holes than electrons respectively. Semiconductor devices are built by these two extrinsic materials, where control of electron mobility controls in a switching action.

Semiconductor material characteristics including energy bandgap, avalanche breakdown electric field, thermal conductivity, saturation electron drift velocity, electron mobility, etc. determine the switch static/transient electrical characteristics, thermal performances, packaging and integration design and so forth. So far, the most employed semiconductor material is silicon whose manufacture and application technologies are mature and hence most cost efficient. Wide energy bandgap materials like silicon carbide (SiC) and gallium nitride (GaN) improve on basic silicon structures facilitating larger voltage and current ratings, minimizing loss due to lower resistance and shaper switching profiles. Table 2.1 shows the characteristics of main power semiconductor materials.

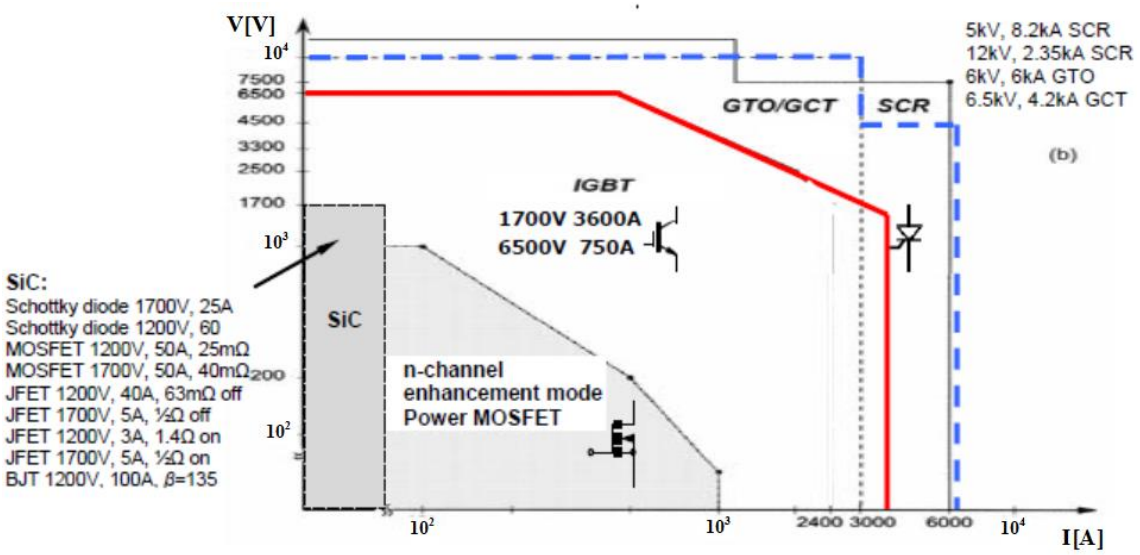
The power, current, voltage and switching capabilities of power semiconductor devices is shown in Figure 2.1. Thyristor type devices or IGBT modules dominate the low-frequency, high-power applications while the high-frequency, low-power applications are dominated by IGBTs and MOSFETs, as shown in Figure 2.1 (a). The current and voltage limits for different power device technologies are shown in Figure 2.1 (b).

Table 2.1 Main applied semiconductor materials in fabrication [79].

Material	Bandgap energy	Dielectric constant	Electron / Hole mobility	Breakdown electric field	Saturated electron drift velocity	Thermal conductivity	Figure of merit w.r.t Si	Coefficient of linear thermal
	E_g	ε_r	μ_n/μ_p	ξ_b	V_{sat}	λ_T	FoM	α
	eV	p.u.	cm^2/Vs	MV/cm	10^7 cm/s	W/mK	$\lambda_T(\xi_b V_{sat})^2$	$\times 10^{-6}$/K
Si	1.12	11.9	1400/450	0.3	1	150	1	2.6
GaAs	1.43	13.1	8500/400	0.46	1	46		6.86
GaN	3.45	9	1000/350	2	2.5	110	407	5.6
3C-SiC	2.36	9.72	800/320	1.3	2.7	360	2381	2.8
4H-SiC	3.26	10.1	900/120	2.2	2	370	3241	5.2
6H-SiC	3.03	9.66	400/90	2.5	2	490	1307	5.2
β-Ga_2O_3	4.6	10	130/-	2.1		13	-	-
diamond	5.45	5.5	2200/1800	10	2.7	2200	54000	0.8



(a) Device power capability limited by the frequency related losses.



(b) Voltage and current limits respectively due to silicon materials, and packaging and die sizes.

Figure 2.1 Semiconductor devices electrical rating bounds [79].

2.3 Device Losses

2.3.1 Introduction

Semiconductor device losses are composed of conduction losses, switching losses, diode reverse recovery losses, gate driver losses and blocking losses. Among these losses, blocking losses are normally negligible and are hence not usually calculated. Here only IGBT, MOSFET, and antiparallel free-wheeling diode losses are investigated since these are the devices of interest in this thesis. Loss analysis of other switch technologies can be similarly determined.

2.3.2 Conduction Losses

During the conduction mode, an IGBT can be modelled by an equivalent electrical circuit comprising of a series DC voltage source and an on-state resistance, as illustrated in Figure 2.2 (a) [80]–[82], from which the device collector-to-emitter voltage can be modelled from:

$$u_{CE} = u_{CE0} + r_{CE} \cdot i_C \tag{2.1}$$

where u_{CE} - the collector-to-emitter voltage, u_{CE0} - the on-state zero current collector-to-emitter voltage drop, r_{CE} - the on-state resistance and i_C - the collector current.

from which the IGBT instantaneous conduction loss can be calculated from [82]:

$$p_{IGBTcond}(t) = u_{CE}(t) \cdot i_C(t) = u_{CE0} \cdot i_C(t) + r_{CE} \cdot i_C^2(t) \tag{2.2}$$

and the IGBT average conduction loss can be calculated from [80], [82]:

$$P_{IGBTcondave} = \frac{1}{T_{cycle}} \int_0^{T_{cycle}} p_{IGBTcond}(t)\,dt = u_{CE0} \cdot I_{Cave} + r_{CE} \cdot I_{Crms}^2 \tag{2.3}$$

where T_{cycle} - the one cycle period, I_{Cave} - the average current during the one cycle period and I_{Crms} - the RMS current during the one cycle period.

As shown in Figure 2.2 (b) the MOSFET drain-to-source voltage can be similarly modelled as:

$$u_{DS} = r_{DS} \cdot i_D \tag{2.4}$$

where r_{DS} - the on-state drain-to-source resistance and i_D - the drain current.

from which the MOSFET instantaneous condition loss can be calculated from [82]:

$$p_{MOSFETcond}(t) = u_{DS}(t) \cdot i_{DS}(t) = r_{DS} \cdot i_{DS}^2(t) \tag{2.5}$$

and the MOSFET average conduction loss can be calculated from [80], [82]:

$$P_{MOSFETcondave} = \frac{1}{T_{cycle}} \int_0^{T_{cycle}} p_{MOSFETcond}(t)\,dt = r_{DS} \cdot I_{Drms}^2 \tag{2.6}$$

where I_{Drms} - the RMS current during the one cycle period.

The diode has the same electrical equivalent circuit as the IGBT as shown in Figure 2.2 (c). Hence, the diode conduction losses can be calculated in the same way [80], [82]:

$$P_{DIODEcondave} = \frac{1}{T_{cycle}} \int_0^{T_{cycle}} p_{DIODEcond}(t)\,dt = u_{D0} \cdot I_{Fave} + R_D \cdot I_{Frms}^2 \tag{2.7}$$

where u_{D0} - the diode conduction mode voltage drop, I_{Fave} - the average diode current during one cycle period, R_D - the diode resistance and I_{Frms} - the diode RMS current during one cycle period.

2.3.3 Switching Losses

The investigation on device characteristics and performances during switching transients is the prerequisite for the devices switching losses calculation. The gate-to-emitter voltage, collector-to-emitter voltage, collector current and the power loss of an IGBT switch have to be studied to illustrate the device switching transient performances. MOSFETs have equivalent performances. Figure 2.2 (d) shows the idealized waveforms during a turn-on and turn-off transient, the linear approximation of the real transient waveform as shown in Figure 2.2 (e). As to the turn-on instant, firstly the gate driver – a voltage source, charges the gate-to-emitter capacitance C_{GE} and the collector current keeps zero. This procedure lasts until the gate-to-emitter voltage reaches the threshold voltage and this period is called the turn-on delay time t_{don}, after which it is the rise time – t_{ri}, the gate-to-emitter voltage keeps increasing whilst the collector current starts building up in line with the gate-to-emitter voltage. Between the end of rise time and the beginning of the voltage fall time –

t_{fu}, the reverse recovery current of diode is absorbed by IGBT switch introducing some extra energy loss (E_{onTrr}). The turn-on time t_{con} is the sum of the rise time and voltage fall time. The collector current increases to load current – I_{Con} and keeps stable while the collector-to-emitter voltage decrease to on-state voltage at the end of the voltage fall time. Similarly, the turn off procedure is reverse to the turn on, the turn-off delay time – t_{doff}, the rise time – t_{ru}, the voltage fall time – t_{fi} and the load current at turn-off – I_{Coff}.

Switching losses are characterized for IGBT and the calculation in MOSFET is the same [81], [82]. The turn on energy loss is the sum of switch-on energy without free-wheeling diode effect to the switch (E_{onTi}) and the energy caused by diode reverse-recovery (E_{onTrr}) [81], [82]. Turn on energy can be calculated by [81], [82]:

$$\begin{aligned} E_{on} &= \int_0^{t_{ri}+t_{fu}} \left(u_{CE}(t)\cdot i_C(t)\right)dt = E_{onTi} + E_{onTrr} \\ &= U_{DD}\cdot I_{Con}\cdot\frac{t_{ri}+t_{fu}}{2} + Q_{rr}\cdot U_{DD} \end{aligned} \tag{2.8}$$

where U_{DD} - The converter supply voltage, I_{Con} - the on-state collector current, and t_{ri} - the current rise time, t_{fu} - the voltage fall time and Q_{rr} - the reverse recovery charge.

Turn off switching energy[81], [82]:

$$E_{off} = \int_0^{t_{ru}+t_{fi}} \left(u_{CE}(t)\cdot i_C(t)\right)dt = U_{DD}\cdot I_{Coff}\cdot\frac{t_{ru}+t_{fi}}{2} \tag{2.9}$$

I_{Coff} - the off-state collector current, t_{ru} - the voltage rise time and t_{fi} - Current fall time

2.3.4 Diode Reverse Recovery Loss

The diode turn-on loss is negligible while the turn-off loss, commonly referred as reverse recovery loss, is calculated [81], [82]:

$$E_{rec} = \int_0^{tri+tfu} u_D(t)\cdot i_F(t)\,dt = \frac{1}{4}\cdot Q_{rr}\cdot U_{Drr} \tag{2.10}$$

where u_D - the diode voltage, i_F - the diode current, Q_{rr} - the diode reverse recovery charge and U_{Drr} - the diode voltage during the reverse recovery.

2.3.5 Gate Drive Loss

In MOSFETs and IGBTs the semiconductor layers among gate, drain (collector), and source (emitter) terminals introduce gate-to-drain (collector) capacitance, gate-to-source (emitter) capacitance and drain(collector)-to-source (emitter) capacitance, which contribute to the switching transients and also to the gate charge. Hence, there are gate losses during the turn-on and turn-off switching transients. Although compared with conduction and switching losses gate drive loss is negligible according to the previous study, the investigation on it is necessary to a comprehensive loss study.

As discussed before IGBTs can be equivalent to the combination of MOSFET and BJT so that in terms of gate driving phenomena and requirements those of IGBTs have the same characteristics with MOSFETs. Gate driver losses can be calculated by:

$$P_{gate} = V_{CC} \cdot Q_g \cdot f_{sw} \tag{2.11}$$

where V_{CC} – the driver supply voltage, Q_g – the total gate charge to drive the switching and f_{sw} - switching frequency. In addition, the driver supply voltage and total gate charge are normally given by the manufacturer.

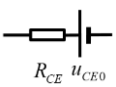
2.3.6 Summary

Take IGBTs for example here that combining semiconductor device power losses, i.e. conduction, switching, diode reverse recovery and gate drive losses (neglecting the blocking losses), yields the total power loss equation:

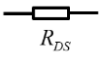
$$\begin{aligned} P_{total} &= P_{IGBTcondave} + P_{DIODEcondave} + P_{sw} + P_{gate} \\ &= P_{IGBTcondave} + P_{DIODEcondave} + \left(E_{on} + E_{off} + E_{rec} + V_{CC} \cdot Q_g\right) \cdot f_{sw} \end{aligned} \tag{2.12}$$

where P_{sw} – the switching losses.

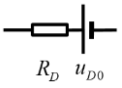
The device power losses are calculated for the VSI in the thermal study in Chapter 6 and the device gate drive power requirements are related to device current and are hence unchanged with phase number.



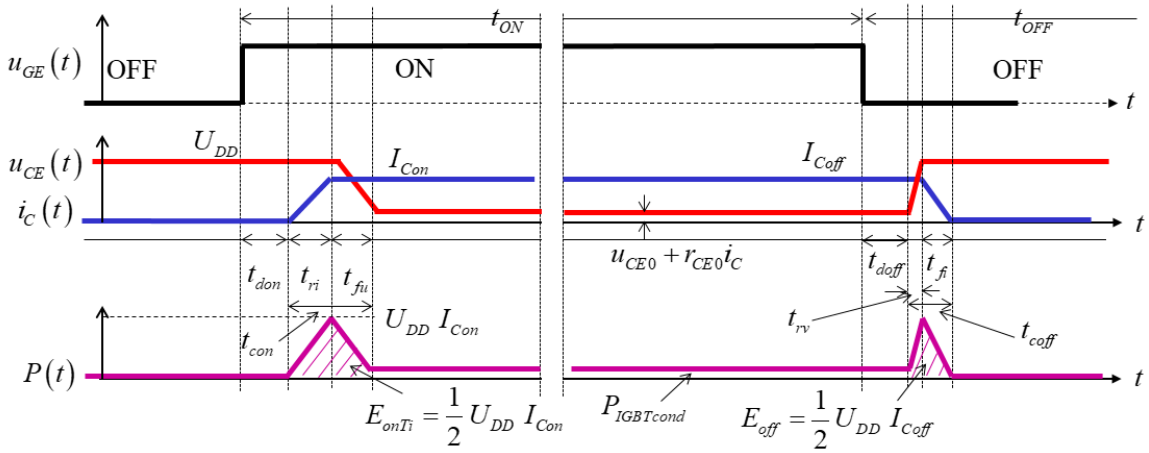
(a) IGBT.



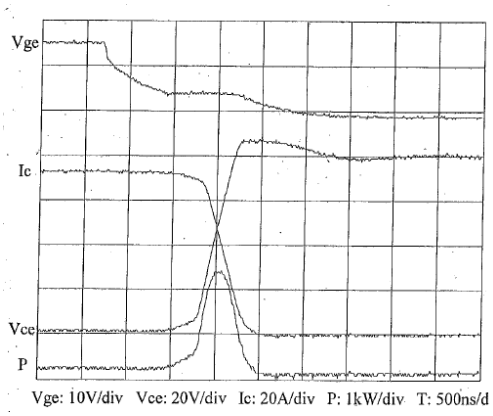
(b) MOSFET.



(c) Diode.



(d) IGBT switch turn-on and turn-off transients.



(e) The turn-off transient waveforms of Trench IGBT; CM600HA-5F, single chip.

Figure 2.2 Power device on-state modelling and IGBT switch turn-on and turn-off transients [80].

2.4 Device Die Ratings and Dimensions

2.4.1 Introduction

Taking IGBTs as an example technology, then if it is assumed that the same semiconductor fabrication technology and material are applied in semiconductor switch die design and manufacture, the IGBT die ratings and characteristics are determined by the die size and geometry. By reviewing manufacturers die designs and their associated ratings, it can be concluded that the die thickness relates to the device rated voltage and the die cross-sectional area (perpendicular to the current flow direction) generally determine the die RMS current rating. Thus, these parameters can be investigated analytically and results compared with different Infineon IGBT3 bare dies and their other products to develop a general design guide for die sizing.

The pn-junction breakdown voltage and the depletion region width have a relationship as shown in Equation (2.13), a function, in which the depletion region width determines the IGBT device directional thickness for current flow and hence the die thickness, for a two pn junction structure [83].

$$V_{BD} = \frac{1}{2} \cdot \left(\frac{n+1}{B} \cdot w^{n-1} \right)^{\frac{1}{n}} \tag{2.13}$$

where w is the depletion region width, and B and n are the constants which are temperature and semiconductor material dependent.

For the silicon material at 300K, the two constant values are $n=7$ and $B = 2.107 \times 10^{-35} cm^6 / V^7$. For non-punch-through (NPT) designs, the base width $W_B = W$ and hence, from Equation (2.13), the base width is given [83]:

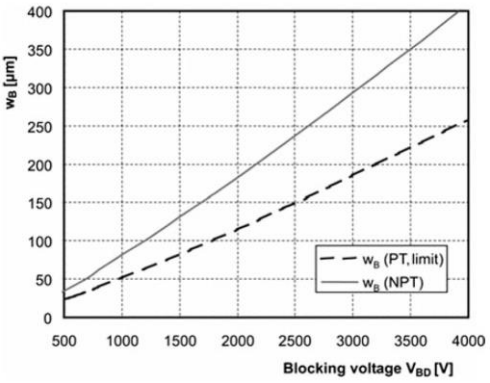
$$w_B = 2^{\frac{2}{3}} \cdot B^{\frac{1}{6}} \cdot V_{BD}^{\frac{7}{6}} \tag{2.14}$$

For the punch-through (PT) designs, the base width is given as:

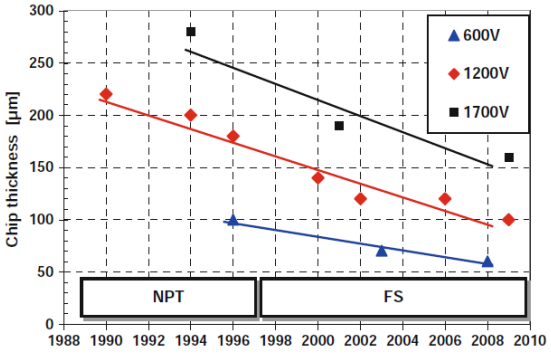
$$w_B = B^{\frac{1}{6}} \cdot V_{BD}^{\frac{7}{6}} \tag{2.15}$$

Figure 2.3 (a) shows the relationship between the base widths and the corresponding blocking voltages for both NPT and PT designs. Figure 2.3 (b) and Figure 2.3 (c) show the IGBT die technology evaluation with the changes on the die thickness and area respectively.

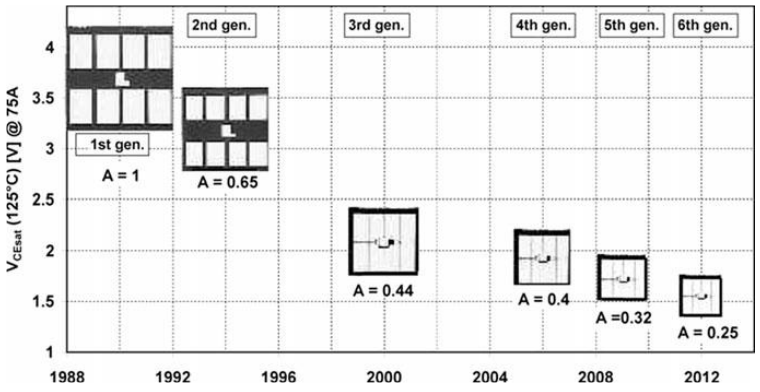
The comparison of rated collector-to-emitter voltage versus their corresponding die thicknesses for different Infineon IGBT 3 bare dies is shown in Figure 2.4, where the IGBT bare die thickness is contributed by different layers, with the base width accounting for the thickest part. The comparison for the IGBT nominal currents versus their corresponding die areas is shown in Figure 2.5 for Infineon IGBT 3 650V bare dies from the SIGCxxT65xxx series [84]–[88] showing the approximate proportional relationship between them.



(a) Die minimal base widths versus blocking voltages.



(b) Device thickness for different generations from Infineon (Note: FS – field stop).



(c) Die area for different IGBT generations, from Infineon.

Figure 2.3 IGBT die thicknesses and areas [83].

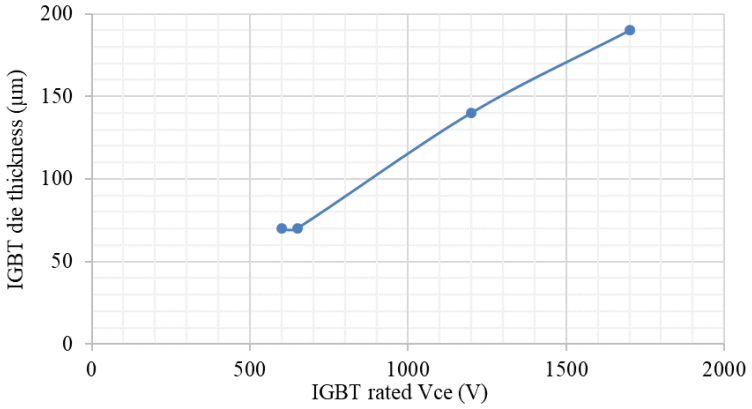


Figure 2.4 Dies collector-to-emitter voltage ratings versus the thicknesses.

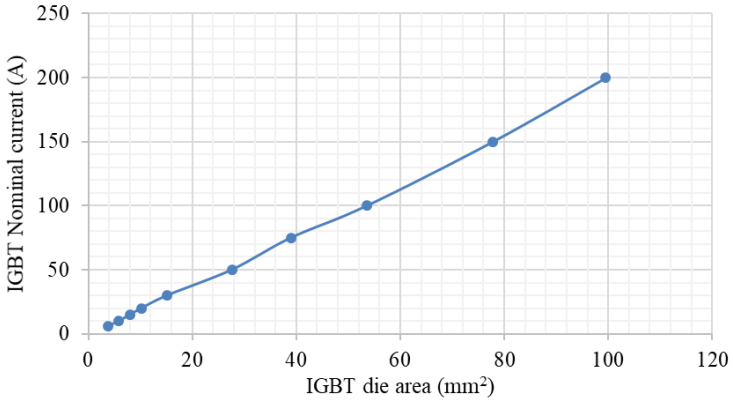
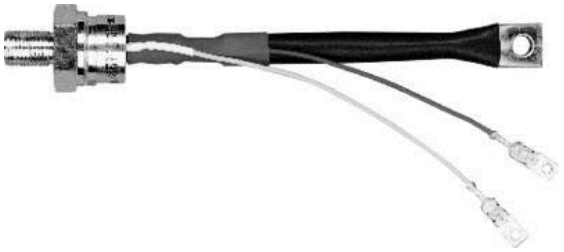


Figure 2.5 IGBT nominal currents versus the respective die areas.

2.4.2 Review of the Commercial Device Packaging

It is semiconductor die chips that execute the electrical functions switching on and off the circuit current and blocking voltage. However, electrical connections between the semiconductor die and external circuits via terminals, heat generation and transfer from semiconductor die to the outside ambient, isolation and protection from outside hazardous environments, etc. are critically important to ensure the proper function, operation and life time of semiconductor devices. Depending on the application, different mechanical and electrical connection and assembly technologies can be applied for the die packaging to

achieve the corresponding electrical, mechanical and thermal criteria. Inside semiconductor devices the technologies for electrical and mechanical joints between semiconductor dies and terminals contain soldering, diffusion sintering, wire bonding, pressure contact, etc., and the differentiations among them focus on thermal and mechanical properties, capabilities and reliabilities, cost efficiencies, etc. [89]. As to packaging and integration technologies, semiconductor switches are categorized into discrete power semiconductors, insulated modules with common base plates, insulated modules without base plates, and intelligent power modules (IPM) etc., example of which are shown in Figure 2.6.



(a) Stud mount for thyristor [90].

(b) Stud mount for diode [91].

(c) Capsule/disc cell mount for diodes [92].

(d) Though hole and surface mount [93].

(e) Insulated module with base plate 1 [94].

(f) Insulated module with base plate 1 [95].

(g) Insulated module without base plate [96].

(h) Intelligent power module (IPM) [97].

Figure 2.6 Different semiconductor die packaging technologies.

2.5 Device Thermal Network

Heat generated on semiconductor die chips needs transferring to keep the temperature of the semiconductor die and their surrounding connections within safe limits at the rated currents. That requires good heat transfer from the die to a suitable heatsink and from heatsink to ambient. Different packaging technologies lead to different switch thermal network, however, the theories and methods to their thermal analysis are the same and general. The VSI thermal design is covered in depth in Chapter 6.

2.6 Other Considerations

Take the IGBT module as an example, the connections between the semiconductor die and module terminals are made via bond wires, internal connection wires, lugs and angle connectors. These lead to internal parasitic inductance which can induce overvoltage during the turn-off instant and damp current build-up at the turn-on instant [89]. Moreover, for multi-parallel semiconductor die designs, the existence of internal parasitic inductances between connecting die results in current share imbalance and even electrical oscillation between dies. Furthermore, parasitic inductance due to terminal connections and cables could also affect the external power circuitry and switching transients.

Due to the existence of the parasitic inductances and capacitances in VSIs circuitry, the switching operation excites electromagnetic interference (EMI) leading to the electromagnetic compatibility (EMC) problem for VSIs. The EMI can be suppressed by using the filter and optimization design of the propagation paths. EMI and EMC are not studied further in this thesis.

Electromagnetic forces between conductors, particularly during switch operation cause movement of connecting wires/bonds that leads to material fatigues and hence aging effects during their lifetime, and hence some parameter and performance variations and ultimate failure. Furthermore, if the cooling system of the semiconductor device cannot transfer the generated heat from die and the temperature on the die exceeds certain levels, thermal

breakdown occurs resulting in the semiconductor die failure. The excessive heat generation can be introduced by the avalanche breakdown, surge current, high current leakage under switch blocking mode, short circuit, over current, etc. Figure 2.7 shows an IGBT failure at the die emitter side due to excess temperature. Besides the above, cosmic rays containing high energy particles can also introduce die failure by forming a pinhole-size molten channel throughout the die layers [89]. This is a particular important consideration for aerospace applications, but less so for automotive.

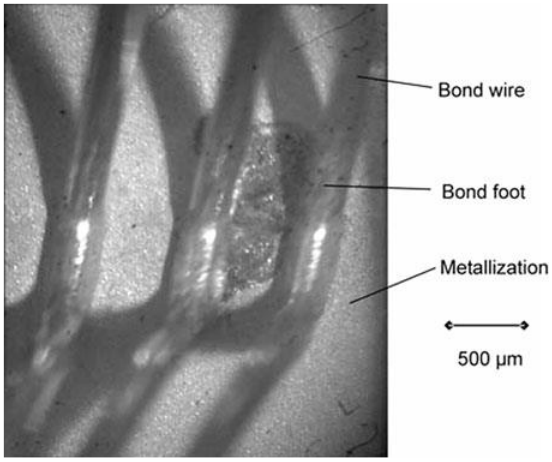


Figure 2.7 An IGBT failure at the chip emitter side due to excess temperature [89].

2.7 Other Power Electronics Components

Besides the power electronics semiconductor devices, other components could be used in power electronic circuitries depending on the application and design considerations, such as contactors and relays (to change the connection of the circuitry), transducers and sensors (to measure the operating conditions for monitoring, control and protection etc.), and passive devices (i.e. resistors, inductors, transformers and capacitors) etc. The functions and applications are briefly discussed here for passive devices.

Resistors whose main types contain carbon/metal film, solid and wire wound are used to either dissipate power or limit the charging/discharging currents, for example [79]:

- Snubber applications for different devices
- Static voltage sharing in series connected circuits
- Static current sharing in parallel connected circuits
- Current and voltage sensing etc.

Inductors and transformers can be used in [79]:

- Snubbers
- Filters
- Transient current sharing
- Current source inductors
- L-C resonator circuit etc.

The functions of capacitors in the electrical circuitry can be summarized [79]:

- Snubbers
- Filters
- Transient current sharing
- AC power factor correction and compensation
- L-C resonator circuit
- DC-bus capacitors etc.

The electrolytic or film capacitor that maintains the DC-link voltage in VSIs is a bulky component in the VSI design, upwards of 20 – 30% of the VSI volume. Further, the capacitor has limitations in terms of environmental pressure and temperature and is one of the major sources of failure in VSIs accounting for around 30% of VSI failure modes [98]. Hence, the study of electrolytic and film capacitors in VSIs is reported in depth in Chapter 4.

2.8 Summary

In this chapter an overview of power electronic semiconductor devices is presented to clarify definitions and terminologies used throughout the remaining chapters. Semiconductor device losses, die ratings and dimensions, device packaging and other device considerations are also presented while the DC-link capacitor and device thermal issues are discussed in greater depth in Chapter 4 and Chapter 6 respectively.

Chapter 3

Switching Strategies for Multiphase Machine Drive Systems

3.1 Introduction

With the increase of the machine drive system phase number, the power electronic device switching strategies become more complex. Generally, a vector space decomposition (VSD) method is taken [27] wherein the most widely used switching strategies are carrier-based pulse width modulation (CBPWM) [27], [99]–[103] and space vector modulation (SVM) [19], [27], [101], [103]–[108].

The basic space vector based SVM strategies have been discussed for 9-phase voltage source inverters (VSIs) driving simple 9-phase resistive-inductive loads [106], 9-phase induction machines [107] and 5-phase VSIs driving a 5-phase brushless permanent magnet (BLPM) machine [109]. So far, there is no comparison among different SVM strategies and no general conclusion for the feasibility of SVM techniques based on the signal injection into the sinusoidal pulse width modulation (SPWM) duty ratio (referred to as "signal injection based SVM" in the following content) to an arbitrary phase number machine drive system whose 3-phase counterpart can be implemented with signal injection based SVM. With increasing phase number the signal injection based SVM is more computational efficient and generalized than the basic space vector based SVM because the algorithm does not change regardless of the phase number. Furthermore, there has been no phase current harmonic content comparison and DC-link voltage utilization study, hence the best SVM is not yet proposed for multiphase machine drive systems.

Different from the other SVM researches in which the experimental validation is conducted with 9-phase resistive and inductive loads or induction machine, this chapter studies

different SVM strategies on a 9-phase, 8-pole, surface mounted, concentrated winding BLPM machine with some effects introduced by the machine fundamental back-EMF and harmonics, winding saliency (inductance variation with rotor position). Besides the previous basic space vector based SVM strategies implementation on the 5-phase BLPM machine drive system, and the 9-phase induction machine drive system in [107], [109], this chapter generalizes the feasibility of different signal injection based SVM strategies containing:

- symmetrical SVM,
- discontinuous SVM,
- balanced group based SVM

for arbitrary n-phase machine drive systems whose 3-phase counterparts can be implemented with these SVM techniques. The chapter then proposes a new selected active basic space vector SVM (only the outermost basic space vectors employed). These SVM strategies are firstly evaluated and compared in terms of phase current harmonic content and DC-link voltage utilization. The arbitrary n-phase system vector control structure is also proposed and implemented on 9-phase and 3x 3-phase drive systems. Furthermore, the 9-phase BLPM base speed under linear modulation region is firstly studied and compared between 9-phase and balanced 3x 3-phase configurations under SPWM and symmetrical SVM, from which the conclusion can be generalized to any multiphase machine drive system being capable to implement group based SVM.

Additionally, different balanced group based SVM techniques are studied in terms of certain harmonic cancellation, phase relation, and machine winding connection configuration. Based on these studies, the best SVM option for 9-phase BLPM is proposed, the balanced group based 3x 3-phase SVM. Moreover the unbalanced group based SVM concept is firstly proposed.

3.2 Multiphase System VSD and Vector Control Structure

For a multiphase machine, the phase displacement between consecutive phases is given by:

$$\alpha = \frac{2\pi}{n} \tag{3.1}$$

where *n* is the number of phases.

The VSD approach has been introduced to model and analyse multiphase systems [27]. An n-phase system can be decomposed into a set of zero-sequence planes and *k* mutually orthogonal planes, where *k* is given by:

$$k = \left\lfloor \frac{(n-1)}{2} \right\rfloor \tag{3.2}$$

Clarke's decoupling transformation matrices [27] for a multiphase system with an arbitrary phase number, *n*, is given in Equation (3.3) under power-invariant conditions and Equation (3.4) under amplitude-invariant conditions, both of which have the same dimension of *n* columns multiplied by *2(k+1)* rows. The first two rows correspond to the *1st* plane (alpha-beta plane) of this multiphase system and define the fundamental component and some certain orders of harmonics. The last third and fourth rows correspond to the *kth* plane and the last two rows define the zero-sequence components. Note, the last row does not exist in an odd phase number system. A system with an odd phase number and floating star point connection does not contain any of the zero-sequence components [27]. Different planes define different order harmonics, i.e.:

x1-y1 plane: $nh \pm 1$ harmonics (where *h* is even)

x2-y2 plane: $nh \pm 2$ harmonics (where *h* is odd)

…

xk-yk plane: $nh \pm k$ harmonics (where *h* is odd when *k* is even, *h* is even when *k* is odd).

$$C_p = m_p \cdot \begin{bmatrix} 1 & \cos\alpha & \cos 2\alpha & \cos 3\alpha & \cdots & \cos 3\alpha & \cos 2\alpha & \cos\alpha \\ 0 & \sin\alpha & \sin 2\alpha & \sin 3\alpha & \cdots & -\sin 3\alpha & -\sin 2\alpha & -\sin\alpha \\ 1 & \cos 2\alpha & \cos 4\alpha & \cos 6\alpha & \cdots & \cos 6\alpha & \cos 4\alpha & \cos 2\alpha \\ 0 & \sin 2\alpha & \sin 4\alpha & \sin 6\alpha & \cdots & -\sin 6\alpha & -\sin 4\alpha & -\sin 2\alpha \\ \vdots & \vdots & \vdots & \vdots & \cdots & \vdots & \vdots & \vdots \\ 1 & \cos k\alpha & \cos 2k\alpha & \cos 3k\alpha & \cdots & \cos 3k\alpha & \cos 2k\alpha & \cos k\alpha \\ 0 & \sin k\alpha & \sin 2k\alpha & \sin 3k\alpha & \cdots & -\sin 3k\alpha & -\sin 2k\alpha & -\sin k\alpha \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} & \cdots & 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1/\sqrt{2} & -1/\sqrt{2} & 1/\sqrt{2} & -1/\sqrt{2} & \cdots & -1/\sqrt{2} & 1/\sqrt{2} & -1/\sqrt{2} \end{bmatrix} \begin{matrix} x_1 \\ y_1 \\ x_2 \\ y_2 \\ \vdots \\ x_k \\ y_k \\ 0_+ \\ 0_- \end{matrix} \tag{3.3}$$

$$C_a = m_a \cdot \begin{bmatrix} 1 & \cos\alpha & \cos 2\alpha & \cos 3\alpha & \cdots & \cos 3\alpha & \cos 2\alpha & \cos\alpha \\ 0 & \sin\alpha & \sin 2\alpha & \sin 3\alpha & \cdots & -\sin 3\alpha & -\sin 2\alpha & -\sin\alpha \\ 1 & \cos 2\alpha & \cos 4\alpha & \cos 6\alpha & \cdots & \cos 6\alpha & \cos 4\alpha & \cos 2\alpha \\ 0 & \sin 2\alpha & \sin 4\alpha & \sin 6\alpha & \cdots & -\sin 6\alpha & -\sin 4\alpha & -\sin 2\alpha \\ \vdots & \vdots & \vdots & \vdots & \cdots & \vdots & \vdots & \vdots \\ 1 & \cos k\alpha & \cos 2k\alpha & \cos 3k\alpha & \cdots & \cos 3k\alpha & \cos 2k\alpha & \cos k\alpha \\ 0 & \sin k\alpha & \sin 2k\alpha & \sin 3k\alpha & \cdots & -\sin 3k\alpha & -\sin 2k\alpha & -\sin k\alpha \\ 1/2 & 1/2 & 1/2 & 1/2 & \cdots & 1/2 & 1/2 & 1/2 \\ 1/2 & -1/2 & 1/2 & -1/2 & \cdots & -1/2 & 1/2 & -1/2 \end{bmatrix} \begin{matrix} x_1 \\ y_1 \\ x_2 \\ y_2 \\ \vdots \\ x_k \\ y_k \\ 0_+ \\ 0_- \end{matrix} \tag{3.4}$$

In an *n*-phase system the total instantaneous power is given by:

$$P_{abcd\cdots} = \left[V_{abcd\cdots}\right]^T \left[I_{abcd\cdots}\right] \tag{3.5}$$

In *k* planes the total power is:

$$\begin{aligned} P_{x1y1x2y2\cdots} &= \left[V_{x1y1x2y2\cdots}\right]^T \left[I_{x1y1x2y2\cdots}\right] \\ &= \left[V_{abcd\cdots}\right]^T C_p^T C_p \left[I_{abcd\cdots}\right] \end{aligned} \tag{3.6}$$

Under power-invariant conditions, the factor m_p of Equation (3.3) can be derived as:

$$m_p = \sqrt{\frac{2}{n}} \tag{3.7}$$

while under the amplitude-invariant conditions, the factor m_a of Equation (3.4) can be derived as:

$$m_a = \frac{2}{n} \tag{3.8}$$

The discussion in this chapter focuses on the voltage and current waveforms, and hence the amplitude-invariant Clarke transformation matrix is used.

In most BLPM drive systems the fundamental component of phase current contributes the major steady output torque [110] and thus the analysis in the first plane is proper for the fundamental output, while the harmonics from the other planes can result in stator flux distortion in the machine air gap and also result in higher phase RMS current, and hence copper losses. Some exceptions exist, for example, 3rd harmonic current injection can contribute to torque generation and decrease torque ripple [110]. In this chapter, the analysis will be based on the sinusoidal back-EMF BLPM machine and its first plane fundamental component.

The vector control strategy is applied here as it is easy to be implemented and, compared to the other control strategies it has the same inner current loop structure and function, i.e. achieving certain magnitude sinusoidal fundamental output phase current in phase with the machine back-EMF (not considering field weakening operation). Moreover, the investigation of this thesis dose not focus on the control but the switching strategy, DC-link capacitor reduction in Chapter 4 and thermal performances in Chapter 6. Consequently, the implementation of vector control is eligible for the experimental validation purposes reported in these subsequent chapters.

The n-phase machine drive system vector control structure is shown in Figure 3.1 where the current harmonics in each plane are controlled individually, i.e. *Iq1* and *Id1* being the direct and quadrature currents in the first plane (*x1y1* plane), *Iq2* and *Id2* in the second plane (*x2y2* plane) and *Iqk* and *Idk* in the kth plane (*xkyk* plane) etc. Under the operating condition discussed above only the fundamental current in the first plane is excited in the stator winding for the torque production while the current harmonics in the other planes are controlled to zero. The current *Id1* is also controlled to zero when not considering field weakening operation.

The VSD n-phase amplitude invariance Clark transformation matrix has been given in Equation (3.4) whose inverse matrix can be calculated as well. The inverse Clark matrix is to convert the components in each stationary planes into the modulation indices of each phases, which are input into the subsequent duty ratio generation module that converts the phase modulation indices into the phase duty ratios for different switching strategies, i.e. SPWM or SVM. This phase duty ratio generation method can be VSD based SPWM or signal injection based SVM. The VSD inverse Clark and the *n*-phase duty ratio generation modules could be substituted by the other duty ratio generation module if the switch-on and switch-off time of each VSI power switch is calculated individually, i.e. basic space vector based SVM, as discussed later. The Park and inverse Park transformation matrices that converts the components between the stationary coordinate and the rotating coordinate systems are defined in [111], [112]. The outer loop is the speed control loop.

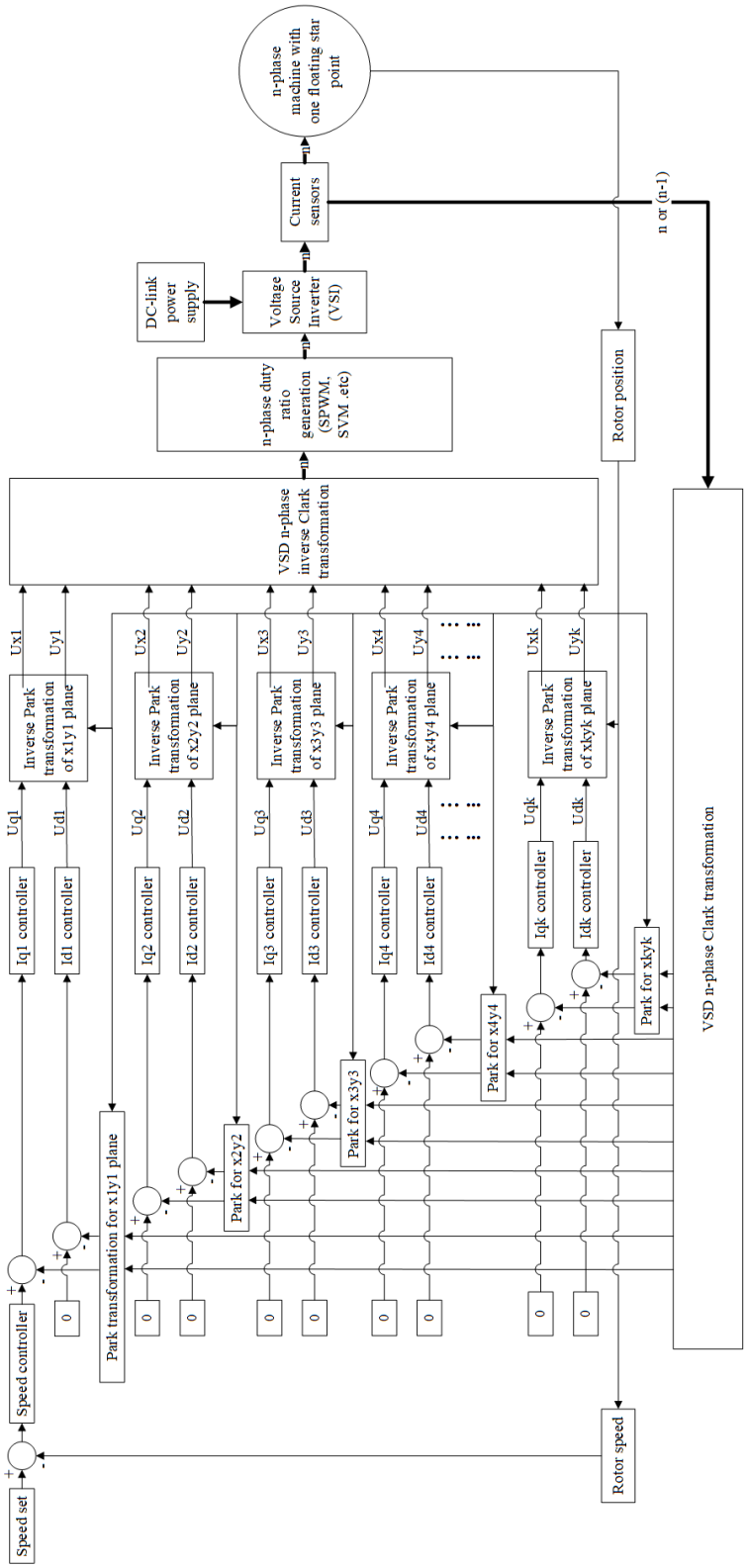


Figure 3.1 Drive system vector control for a n-phase machine structure.

3.3 Multiphase BLPM Machine Model and Experimental Test Facility

The multiphase VSI SVM strategies discussed in this chapter can be applied to different brushless machine technologies, i.e. induction, permanent magnet and synchronous reluctance. The modelling of an arbitrary phase number, star connected BLPM machine is investigated here while other machine technologies can be modelled using a similar methodology. The machine model is similar for both distributed and concentrated wound machine stators, surface or imbedded rotor magnet topologies.

For a balanced, well-constructed machine, the per phase electrical model can be simplified to a phase winding resistance, synchronous inductance and back-EMF [113]. For interior permanent magnet machines (IPM) the phase inductances can be highly non-linear, particularly at high loads [114]. These variations affect, but do not dominate, the functionalities of the inverter. Therefore, to simplify the analysis these effects can be neglected and the machine winding inductances can be regarded as constant. The machine phase voltage can thus be modelled as:

$$\left[v_s^{ph}\right] = \left[R_s\right]\left[i_s^{ph}\right] + \left[L_s\right]\frac{d}{dt}\left[i_s^{ph}\right] + \left[e_s^{ph}\right] \tag{3.9}$$

where $[v_s^{ph}]$, $[R_s]$, $[L_s]$, $[i_s^{ph}]$ and $[e_s^{ph}]$ are the phase voltage, resistance, inductance, current and back-EMF matrices respectively. The machine winding resistance matrix can be expanded as:

$$\left[R_s^{ph}\right] = \begin{bmatrix} R_1 & 0 & \cdots & 0 & \cdots & 0 \\ 0 & R_2 & \ldots & 0 & \cdots & 0 \\ \vdots & \cdots & \ddots & \vdots & \cdots & \vdots \\ 0 & 0 & \cdots & R_x & \cdots & 0 \\ \vdots & \cdots & \cdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 0 & \cdots & R_n \end{bmatrix} \tag{3.10}$$

where R_n is the resistance of phase n and $R_1 = R_2 = \ldots = R_n$ for balanced machine windings. The machine inductance matrix can be expanded as:

$$\left[L_s^{ph}\right]=\begin{bmatrix} L_1 & M_{12} & \cdots & M_{1x} & \cdots & M_{1n} \\ M_{21} & L_2 & \cdots & M_{2x} & \cdots & M_{2n} \\ \vdots & \cdots & \ddots & \cdots & \cdots & \vdots \\ M_{x1} & M_{x2} & \cdots & L_x & \cdots & M_{xn} \\ \vdots & \cdots & \cdots & \vdots & \ddots & \vdots \\ M_{n1} & M_{n2} & \cdots & M_{nx} & \cdots & L_n \end{bmatrix} \tag{3.11}$$

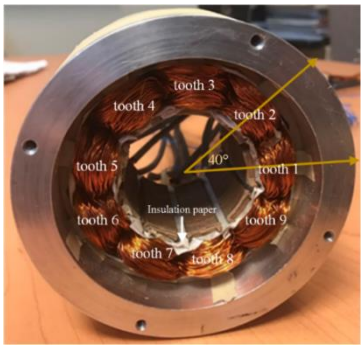
where L_n is the self-inductance of phase n, and M_{xy} is the mutual inductance between phase x and y. For the test machine and this analysis, the machine back-EMFs are sinusoidal. Hence, the phase back-EMF matrix is:

$$\left[e_s^{ph}\right]=\begin{bmatrix} E_p\cos(\omega t+\varepsilon) \\ E_p\cos(\omega t+\alpha+\varepsilon) \\ \vdots \\ E_p\cos\left[\omega t+(n-2)\alpha+\varepsilon\right] \\ E_p\cos\left[\omega t+(n-1)\alpha+\varepsilon\right] \end{bmatrix} \tag{3.12}$$

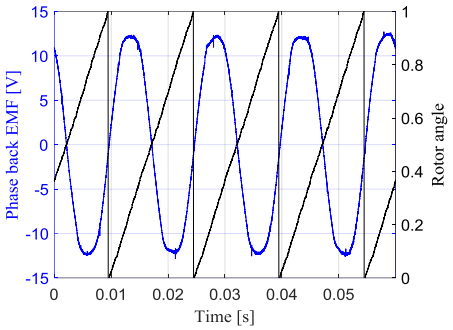
where E_p is the peak value of phase back-EMF, peak value which is proportional to electrical rotational speed, ω, and ε is an arbitrary angle.

Figure 3.2 (a) shows the test machine stator used for experimental validation. The machine has a 9-phase concentrated coil stator winding, and 8-pole rotor. Open circuit back-EMF test results are presented in Figure 3.2 (b), showing the back-EMF waveforms for phase 1 and rotor alignment with the phase 1 back-EMF. Hence, ε is zero for this test facility.

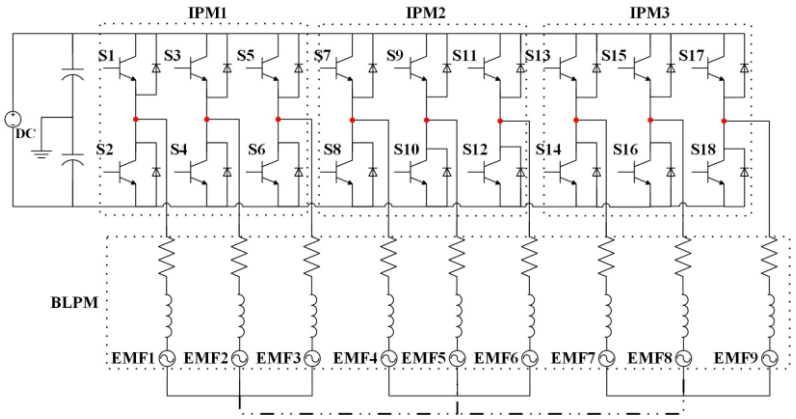
In an arbitrary phase number two level multiphase VSI there are n legs, $2n$ switches, and 2^n different switching states, i.e. basic space vectors. For the test facility here, the 9-phase VSI is implemented via 3 integrated power modules (IPM 1 to 3), as shown schematically in Figure 3.2 (c). Note that the 9-phase star connection could be split to form a 3x 3-phase configuration, as indicated by the dashed connecting line in Figure 3.2 (c). The overview of the experimental test facility is shown in Figure 3.2 (d) and a detailed discussion of the test facility given in Chapter 5.



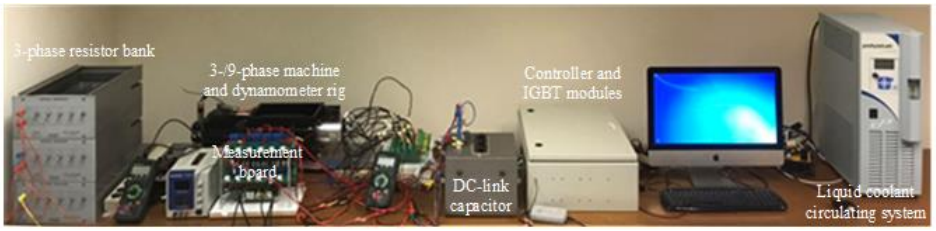
(a) Stator of surface mounted, concentrated winding, 9-phase, 8-pole, BLPM machine.



(b) Phase 1 back-EMF waveforms and rotor position measurement.



(c) 9-phase VSI and BLPM schematic diagram.



(d) Overview of full experimental setup

Figure 3.2 Test facility for experimental validations of control strategies.

3.4 Multiphase SVM Strategies

Different SVM strategies are discussed here for an arbitrary phase number, multiphase system. While a 9-phase system is implemented here as an example for illustration chosen primarily since the electric machine and power electronic converter can be configured, by design, into either a 9-phase or 3x 3-phase structure. The signal injection based symmetrical and discontinues SVM strategies are studied in Chapter 3.4.1, a new selected active basic space vector SVM strategy is proposed in Chapter 3.4.2 and the new concept – balanced and unbalanced group based SVMs are proposed in Chapter 3.4.3. The DC-link voltage utilization is finally assessed in Chapter 3.4.4 under different switching strategies.

3.4.1 Multiphase Signal Injection Based Symmetrical and Discontinuous SVMs

The VSD approach can be applied to generate phase current with desired harmonic content by controlling corresponding harmonic distributions in different planes i.e. *x1y1*, *x2y2*, *x3y3, ... xkyk*. The machine back-EMF could contain different orders of harmonics and their corresponding orders of stator current harmonics could generate synchronous torque [110]. Here, the simplest condition is assumed that the back-EMF is sinusoidal and only contains the fundamental element. Then only the fundamental stator current should be excited by only enabling first plane current output and setting the current output in other planes *x2y2, x3y3* etc. to zero.

The similar scheme has been discussed and implemented in [107], [115]–[117] and here it is generalized to an n-phase system SVM solution. Two different SVM strategies are introduced here, symmetric SVM and discontinuous SVM whose phase duty ratios are generated from the signal injection into the SPWM duty ratios.

In SPWM, n-phase duty ratios are $d_{SPWM}(1)$ to $d_{SPWM}(n)$, and the maximum and minimum values are:

$$d_{\max} = \max\left[d_{SPWM}(1) \quad d_{SPWM}(2) \quad \cdots \quad d_{SPWM}(n) \right] \tag{3.13}$$

$$d_{\min} = \min\left[d_{SPWM}(1) \quad d_{SPWM}(2) \quad \cdots \quad d_{SPWM}(n) \right] \tag{3.14}$$

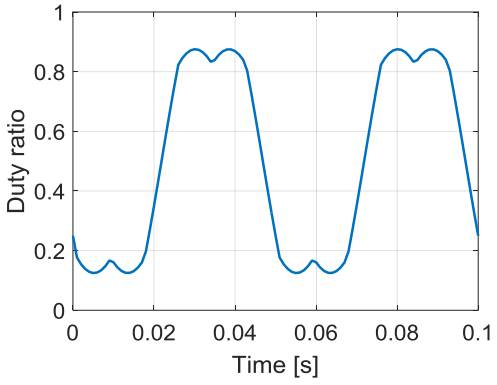
For n-phase symmetric SVM the phase *n* duty ratio is:

$$d_{SVM}(n) = d_{SPWM}(n) + 0.5(1 - d_{\max} - d_{\min}) \tag{3.15}$$

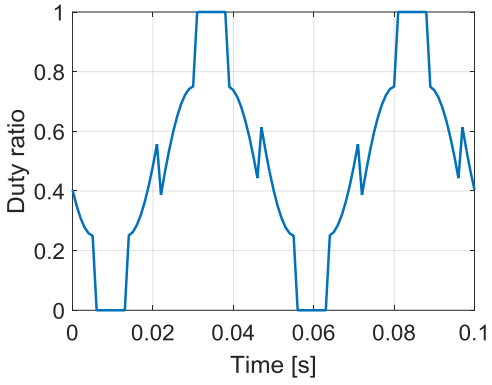
For n-phase discontinuous SVM the phase *n* duty ratio is:

$$d_{DSVM}(n) = \begin{cases} d_{SPWM}(n) - d_{\min} & d_{\max} + d_{\min} < 1 \\ d_{SPWM}(n) + (1 - d_{\max}) & d_{\max} + d_{\min} \geq 1 \end{cases} \tag{3.16}$$

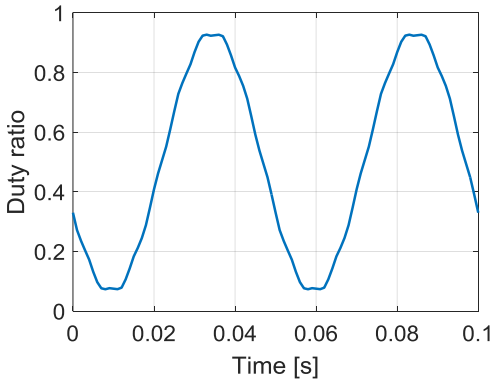
The phase voltage duty ratios under symmetrical and discontinues SVMs for 3-phase and 9-phase systems are presented in Figure 3.3. The duty ratio waveforms under different switching strategies result in the subsequent phase voltage and the different DC-link voltage utilization.



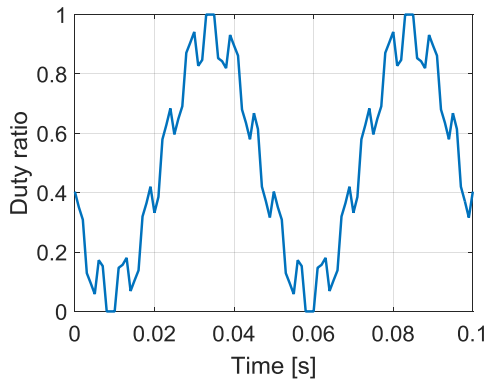
(a) 3-phase symmetrical SVM.



(b) 3-phase discontinuous SVM.



(c) 9-phase symmetrical SVM.



(d) 9-phase discontinuous SVM.

Figure 3.3 Duty ratios for 3-phase and 9-phase signal injection based SVM strategies.

3.4.2 Multiphase Selected Basic Space Vector SVM

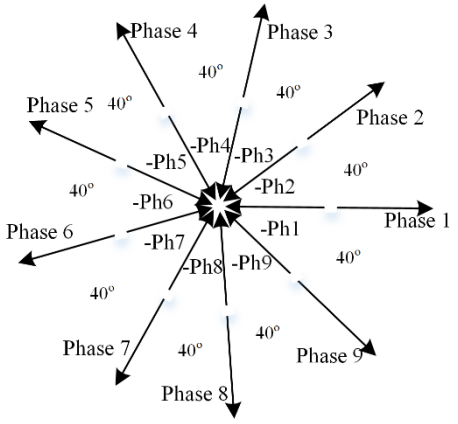
Before further discussion, three items are defined here, the switching number combination, the phase voltage vector and the basic space vector.

The switching number combination is the on-state number pair of the upper and lower switches. Taking the 9-phase system as an example, 1 upper switch on and 8 lower switches on, and 8 upper switches on and 1 lower switch on are defined as one switching number combination. Hence, for a 9-phase system there are 4 different switching number combinations (1, 8), (2, 7), (3, 6) and (4, 5). The numbers of possible switching number combinations of an n-phase multiphase system can be generalized by:

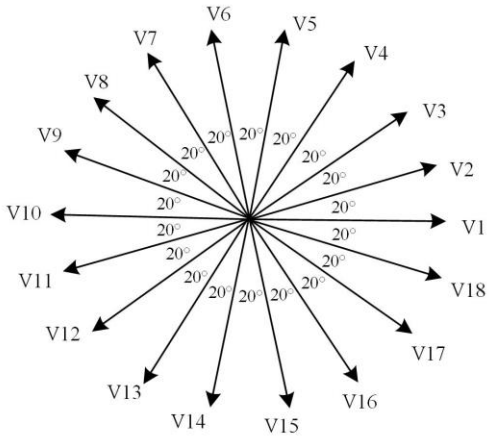
$$com = \begin{cases} (n-1)/2 & n \text{ is odd} \\ n/2 & n \text{ is even} \end{cases} \tag{3.17}$$

The phase voltage vector determines the inverter phase leg voltage magnitude and phasor angle while the basic space vector is the voltage vector synthesising all the phase voltage vectors in the machine stationary coordinate. Again, taking a 9-phase system as an example, Figure 3.4 shows 18 different phase voltage vectors, i.e. two opposing direction vectors from each 9 phase leg (a) and 18 different basic space vectors (b) (under one switching number combination) of which each are synthesised by 9 of the 18 phase voltage vectors. There is 40° electrical displacement between consecutive phase vectors and 20° electrical displacement between consecutive basic space vectors.

For an *n*-phase system there are finite switching states corresponding to 2^n different basic space vectors in which there are two zero magnitude basic space vectors, the switching conditions with all upper switches on or all lower switches on. Increasing phase number increases the possibilities of basic space vectors with different magnitudes and phasor angles, and hence the modulation complexity.



(a) Phase voltage vectors of 9-phase system.



(b) Basic space vectors under one switching number combination for 9-phase system.

Figure 3.4 Phase voltage and basic space vector definition.

The switching states of the 9-phase system are defined as:

$$[S]=[S_1 \quad S_2 \quad S_3 \quad S_4 \quad S_5 \quad S_6 \quad S_7 \quad S_8 \quad S_9] \tag{3.18}$$

where *S* indicates the switching state of one leg and having a value of 1 or -1, 1 means the upper switch is turned on and lower switch off, and -1 means the upper switch is turned off and lower switch on.

From observation, even for the switching states of the same switching number combination, their basic space vector magnitudes vary due to the different on-state switch distributions in different phase legs. Further, under the same switching number combination, the highest magnitude basic space vectors are synthesized when the same switching states appear in the neighbourhood phase legs, eliminating the phase voltage vector cancellation and utilizing the DC-link voltage more effectively. Here, those corresponding basic space vectors are defined as the outmost basic space vectors for one switching number combination. For example switching states A generates higher basic space vector than switching states B, where switching states A are defined as:

$$[S_A]=[1 \quad 1 \quad 1 \quad 1 \quad -1 \quad -1 \quad -1 \quad -1 \quad -1] \tag{3.19}$$

and switching states B are defined as:

$$[S_B] = [1 \quad 1 \quad -1 \quad -1 \quad 1 \quad 1 \quad -1 \quad -1 \quad -1] \tag{3.20}$$

Consequently, switching states A correspond to one of the outmost basic space vectors for the (4, 5) switching number combination. To optimize the DC-link voltage utilization, only the outmost basic space vectors are selected and applied. Furthermore, even the outmost basic space vectors under different switching number combinations have different magnitudes. These outermost basic space vectors are categorized into different groups and, at one switching period, basic space vectors from one or multiple groups can be applied to synthesize and track the reference voltage vector in the machine stationary coordinate system.

With one group of basic space vectors employing SVM strategies, the machine stationary coordinate (first plane) is divided into *2n* sections, in which the reference voltage vector is synthesized by the neighborhood two basic space vectors, their operating time and zero time in each switching period are given by Equations (3.21), (3.22) and (3.23), as illustrated in Figure 3.5 (a), under linear modulation operation region. The functioning time of the basic space vectors in one switching period can be calculated as:

$$T_N = \frac{T_c U_{x1} \sin\left[N\left(180^\circ / n\right)\right] - T_c U_{y1} \cos\left[N\left(180^\circ / n\right)\right]}{\left|\vec{V}_N\right| \sin\left(180^\circ / n\right)} \tag{3.21}$$

$$T_{N+1} = \frac{T_c U_{x1} \sin\left[(N-1)\cdot\left(180^\circ / n\right)\right] - T_c U_{y1} \cos\left[(N-1)\cdot\left(180^\circ / n\right)\right]}{-\left|\vec{V}_{N+1}\right| \sin\left(180^\circ / n\right)} \tag{3.22}$$

$$T_0 = T_c - T_N - T_{N+1} \tag{3.23}$$

where N is the sector number (from 1 to 2n), T_c is the switching period, U_{x1} and U_{y1} are the reference voltage vector variables in the machine two axis stationary coordinates, $\vec{V}_N$ and $\vec{V}_{N+1}$ are two neighbourhood active basic space vectors and T_N T_{N+1} and T_0 are the respective application times for the two active basic space vectors and zero vectors.

Taking the 9-phase system as an example; at any instance, *M* upper switches and corresponding (9-*M*) lower switches are on, which leads to basic space vectors with different DC bus utilization. The highest DC bus utilization basic space vectors (the outmost ones), are selected in each switching number combinations with different *M* and categorized into four groups:

- Group A: 1 or 8 upper switches ON
- Group B: 2 or 7 upper switches ON
- Group C: 3 or 6 upper switches ON
- Group D: 4 or 5 upper switches ON

The comparison has been made for different groups of outmost basic space vectors in terms of the ratio between the basic space vector magnitude and the DC bus voltage, as shown in Figure 3.5 (b). In each switching period, up to 4 groups of the basic space vectors and two zero vectors can be employed to generate the reference voltage vector. In some situations, all the outmost basic space vectors from different groups are applied [105], [106] while in other situations, only one group of the basic space vectors with the biggest magnitudes are introduced [105].

The application of different groups of active basic space vectors results in performance differences especially for the modulation index. Here only group D basic space vectors are selected to achieve the highest DC-link voltage utilization. However, this approach does not apply a given or even known voltage in the *x2y2, x3y3,* etc. planes, in which these "parasitic" voltages will drive unintended current harmonics. This scenario is validated under one operating point via simulation (U_{x1} *= 25.49 V,* U_{y1} *= 30.82 V,* DC-link voltage *80 V,* and switching frequency *5 kHz*), *N = 3,* and T_3 T_4 and T_0 are *82 µs 77 µs* and *41 µs* respectively, as shown in Figure 3.5 (c).

3.4.3 Multiphase Balanced and Unbalanced Group Based SVMs

Another scenario to achieve *n*-phase SVM is to apply balanced group based SVM. For an *n*-phase system, if *n* is a multiple of 3, this system can be composed of (*n*/3)x 3-phase systems. The same approach is also eligible if *n* is a multiple of 5, 7 etc. Then the system

can be composed of multiple 5-phase, 7-phase systems etc. Furthermore, theoretically one multiphase system can also be composed of different isolated multiphase systems with different phase numbers, for example, a 6-phase system and a 3-phase system can synthesize a 9-phase system, which is defined as the unbalanced group based SVM here. However, this will increase the control complexity and introduce more system imbalance problems than a 9-phase system composed of 3x 3-phase systems. As previously discussed, the phase shift between two consecutive voltage phases for a symmetrical 9-phase system is 40º electrical, while in a 3-phase system it is 120º electrical. Consequently, a 9-phase system can be composed of 3x 3-phase systems where each individual 3-phase set is shifted by 40º electrical, denoted ABC1, ABC2 and ABC3, as shown in Figure 3.5 (d). Here, each 3-phase set is controlled by 3-phase SVM. Under this condition, the machine has three separate floating star points. From a phase current and voltage point-of-view (i.e. the electrical side), this switching modulation scheme is inherently a 3-phase SVM.

As discussed before regarding the balanced group based SVM scenario, taking the 9-phase system composed of 3x 3-phase system as an example, in terms of the machine star point side configuration, the isolation among these 3-phase subsystems are necessary, thus 3 floating star points. The reason for the necessity is that each subsystem has other voltage harmonics injection additional to the fundamental under SVM strategies. If the star points are connected together, the injected voltage harmonics among different subsystems (each 3-phase system) will affect each other due to their common connection, resulting in circulating currents, which do not contribute to torque production while dissipating extra copper losses. However inside each isolated subsystem this current circulation does not occur as the injected voltage harmonics are in phase in the different phase legs.

3.4.4 DC-link Voltage Utilization Comparisons under Different Multiphase SVMs

The modulation index is defined here as the ratio of the phase fundamental peak voltage to the DC-link voltage. For SPWM the maximum linear region modulation index is 0.5 while for SVM this value is no less than 0.5, hence leading to potentially better DC-bus voltage

utilization. The modulation index for different SVM strategies are derived and generalized here.

All the basic space vectors in different planes and switching states are given from:

$$\begin{bmatrix} V_{x1} \\ V_{y1} \\ V_{x2} \\ V_{y2} \\ \vdots \\ V_{x_k} \\ V_{y_k} \\ V_{0+} \\ V_{0-} \end{bmatrix} = C_a \cdot \frac{V_{DC}}{2} \begin{bmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \\ \vdots \\ S_{n-3} \\ S_{n-2} \\ S_{n-1} \\ S_n \end{bmatrix} = \frac{V_{DC}}{n} \begin{bmatrix} \sum_{i=0}^{n-1} \cos(i \cdot \alpha) \cdot S_{i+1} \\ \sum_{i=0}^{n-1} \sin(i \cdot \alpha) \cdot S_{i+1} \\ \sum_{i=0}^{n-1} \cos(2 \cdot i \cdot \alpha) \cdot S_{i+1} \\ \sum_{i=0}^{n-1} \sin(2 \cdot i \cdot \alpha) \cdot S_{i+1} \\ \vdots \\ \sum_{i=0}^{n-1} \cos(k \cdot i \cdot \alpha) \cdot S_{i+1} \\ \sum_{i=0}^{n-1} \sin(k \cdot i \cdot \alpha) \cdot S_{i+1} \\ \sum_{i=0}^{n-1} 1/2 \cdot S_{i+1} \\ \sum_{i=0}^{n-1} (-1)^n \cdot 1/2 \cdot S_{i+1} \end{bmatrix} \tag{3.24}$$

If only the first plane element (*x1y1*) is considered, the fundamental, the corresponding maximum fundamental phase voltage is given by:

$$\max\left\{\left|V_{x1} + jV_{y1}\right|\right\} = \begin{cases} \cos\left(\frac{\alpha}{4}\right)\frac{V_{DC}}{n}\sqrt{\left(\sum_{i=0}^{n-1}\cos(i\cdot\alpha)S_{i+1}\right)^2 + \left(\sum_{i=0}^{n-1}\sin(i\cdot\alpha)S_{i+1}\right)^2} & \text{if n is odd} \\ \cos\left(\frac{\alpha}{2}\right)\frac{V_{DC}}{n}\sqrt{\left(\sum_{i=0}^{n-1}\cos(i\cdot\alpha)S_{i+1}\right)^2 + \left(\sum_{i=0}^{n-1}\sin(i\cdot\alpha)S_{i+1}\right)^2} & \text{if n is even} \end{cases} \tag{3.25}$$

Hence, the maximum linear region modulation index can be given by:

$$\max Index = \begin{cases} \frac{\cos\left(\frac{\alpha}{4}\right)}{n}\sqrt{\left(\sum_{i=0}^{n-1}\cos(i\cdot\alpha)S_{i+1}\right)^2 + \left(\sum_{i=0}^{n-1}\sin(i\cdot\alpha)S_{i+1}\right)^2} & \text{if n is odd} \\ \frac{\cos\left(\frac{\alpha}{2}\right)}{n}\sqrt{\left(\sum_{i=0}^{n-1}\cos(i\cdot\alpha)S_{i+1}\right)^2 + \left(\sum_{i=0}^{n-1}\sin(i\cdot\alpha)S_{i+1}\right)^2} & \text{if n is even} \end{cases} \tag{3.26}$$

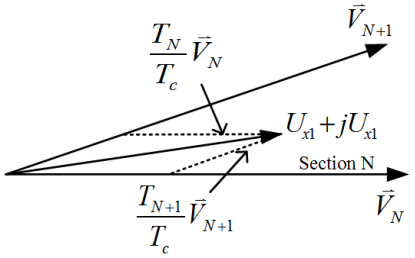
Considering the selective active outermost basic space vector SVM, from the geometry observation, the maximum modulation index occurs when there are *k* successive upper switches on or *k+1* successive upper switches on, with the corresponding lower switches off. This result in the highest outermost basic space vector e.g. Group D in a 9-phase system. Therefore, to calculate the maximum modulation index the switch states are given by:

$$S_n = \begin{cases} 1 & n = 1, 2, ...k \\ -1 & n = k, ...n \end{cases} \tag{3.27}$$

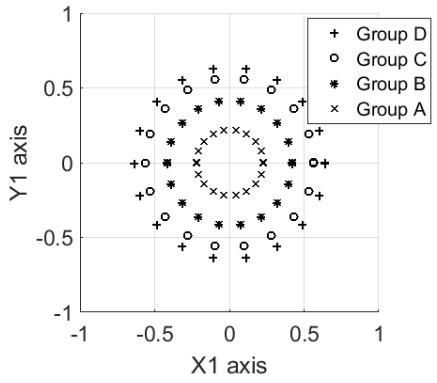
The maximum linear region modulation indexes for n-phase symmetric or discontinuous SVMs are given by [117]:

$$\max Index = \begin{cases} \dfrac{1}{2\cos\left(\dfrac{\pi}{2n}\right)} & \text{if n is odd} \\ 0.5 & \text{if n is even} \end{cases} \tag{3.28}$$

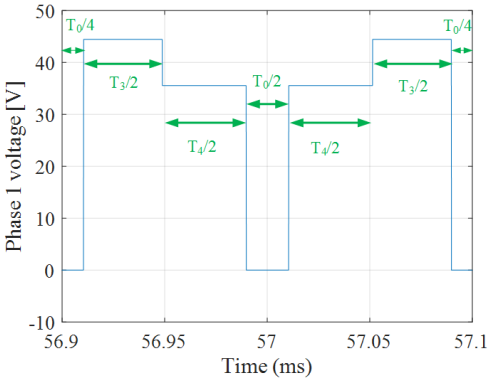
Based on Equations (3.26) and (3.28), Table 3.1 shows the maximum linear region modulation indices that can be achieved by different modulation strategies. It is noted that selected active basic space SVM can achieve the highest modulation index, however it introduces voltage harmonics in the *x2y2*, *x3y3* and *x4y4* etc. planes that drive undesired load currents, in this case, in the electric machine.



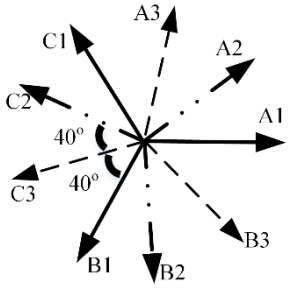
(a) SVM voltage vectors synthesis.



(b) Different groups of basic space vectors.



(c) Validation for the selective active basic space vector SVM.



(d) 9-phase system balanced group-based SVM.

Figure 3.5 Illustrations for selected basic space vector SVM and balanced group based SVM.

Table 3.1 Comparisons of maximum modulation index, for sinusoidal PWM the maximum modulation index is 0.5.

Number of phases n	Symmetric/ discontinuous SVM	SVM with selected basic space vectors
3	0.5775	0.5775
4	0.5000	0.5000
5	0.5255	0.6155
6	0.5000	0.5775
7	0.5130	0.6260
8	0.5000	0.6035
9	0.5075	0.6300
10	0.5000	0.6155
∞	0.5000	0.6365

3.5 Vector Control Structures for 3x 3-phase and 9-phase

According to VSD Clark matrices, the 3-phase system has only 1 plane structure while the 9-phase system has 4 plane structures. The different planes, their corresponding phase sequences and harmonic contents in each planes for a 9-phase system are given in Table 3.2. The harmonic orders in both 3-phase and 9-phase systems are given in Table 3.3.

The 9-phase system can be a 9-phase system with 4 planes or decomposed into 3 sets of 3-phase systems with 1 plane for each set, as shown schematically in Figure 3.6. As a result, under machine field oriented vector control there are two controller structures proposed:

- 9-phase controller, and
- 3x 3-phase controller.

The 3x 3-phase controller is inherently composed of 3-phase controllers for three isolated 3-phase machine winding sets. The 9-phase machine drive system vector control structure is shown in Figure 3.7 and the balanced group based 3x 3-phase one is shown in Figure 3.8. The 3-phase VSD Clarke matrix is given in Equation (3.29) and the 9-phase one is given in Equation (3.30), both of which are under the amplitude invariant condition.

$$C_{3-phase} = \frac{2}{3} \cdot \begin{bmatrix} 1 & \cos\frac{2\pi}{3} & \cos\frac{4\pi}{3} \\ 0 & \sin\frac{2\pi}{3} & \sin\frac{4\pi}{3} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{3.29}$$

$$C_{9-phase} = \frac{2}{9} \cdot \begin{bmatrix} 1 & \cos\frac{2\pi}{9} & \cos\frac{4\pi}{9} & \cos\frac{2\pi}{3} & \cos\frac{8\pi}{9} & \cos\frac{8\pi}{9} & \cos\frac{2\pi}{3} & \cos\frac{4\pi}{9} & \cos\frac{2\pi}{9} \\ 0 & \sin\frac{2\pi}{9} & \sin\frac{4\pi}{9} & \sin\frac{2\pi}{3} & \sin\frac{8\pi}{9} & -\sin\frac{8\pi}{9} & -\sin\frac{2\pi}{3} & -\sin\frac{4\pi}{9} & -\sin\frac{2\pi}{9} \\ 1 & \cos\frac{4\pi}{9} & \cos\frac{8\pi}{9} & \cos\frac{4\pi}{3} & \cos\frac{2\pi}{9} & \cos\frac{2\pi}{9} & \cos\frac{4\pi}{3} & \cos\frac{8\pi}{9} & \cos\frac{4\pi}{9} \\ 0 & \sin\frac{4\pi}{9} & \sin\frac{8\pi}{9} & \sin\frac{4\pi}{3} & \sin\frac{2\pi}{9} & -\sin\frac{2\pi}{9} & -\sin\frac{4\pi}{3} & -\sin\frac{8\pi}{9} & -\sin\frac{4\pi}{9} \\ 1 & \cos\frac{2\pi}{3} & \cos\frac{4\pi}{3} & 1 & \cos\frac{2\pi}{3} & \cos\frac{2\pi}{3} & 1 & \cos\frac{4\pi}{3} & \cos\frac{2\pi}{3} \\ 0 & \sin\frac{2\pi}{3} & \sin\frac{4\pi}{3} & 0 & \sin\frac{2\pi}{3} & -\sin\frac{2\pi}{3} & 0 & -\sin\frac{4\pi}{3} & -\sin\frac{2\pi}{3} \\ 1 & \cos\frac{8\pi}{9} & \cos\frac{2\pi}{9} & \cos\frac{8\pi}{3} & \cos\frac{2\pi}{3} & \cos\frac{2\pi}{3} & \cos\frac{8\pi}{3} & \cos\frac{2\pi}{9} & \cos\frac{8\pi}{9} \\ 0 & \sin\frac{8\pi}{9} & \sin\frac{2\pi}{9} & \sin\frac{8\pi}{3} & \sin\frac{2\pi}{3} & -\sin\frac{2\pi}{3} & -\sin\frac{8\pi}{3} & -\sin\frac{2\pi}{9} & -\sin\frac{8\pi}{9} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{3.30}$$

Table 3.2 Plane number, corresponding phase sequence and harmonic content for 9-phase system.

Plane number	Phase sequence									Harmonic content
1	1	2	3	4	5	6	7	8	9	1, 17, 19 …
2	1	3	5	7	9	2	4	6	8	7, 11, 25, 29 …
3	1	4	7	1	4	7	1	4	7	3, 15, 21 …
4	1	5	9	4	8	3	7	2	6	5, 13, 23, 31 …

Table 3.3 Harmonic content within 20 harmonic orders for 3-phase and 9-phase drive systems

Phase number	Harmonics orders
3	1, 5, 7, 11, 13, 17, 19… …
9	1, 3, 5, 7, 11, 13, 15, 17, 19… …

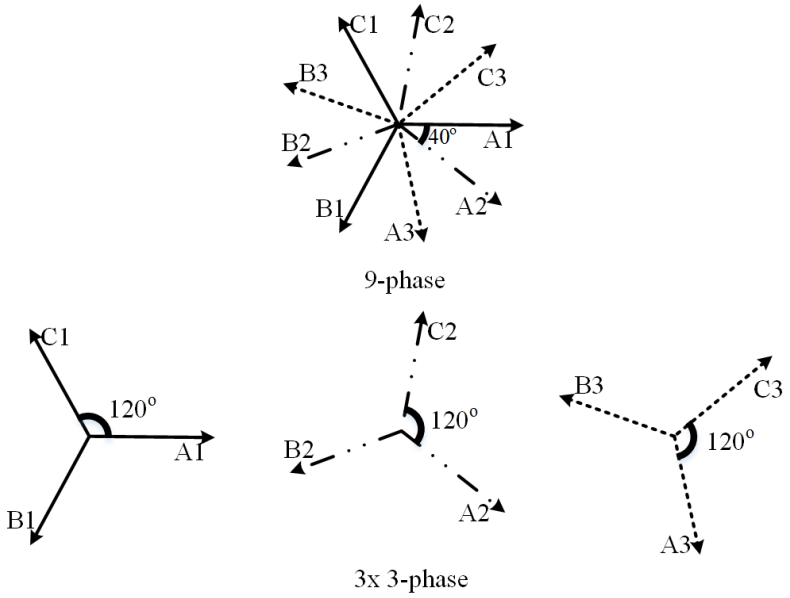


Figure 3.6 9-phase and 3x 3-phase configurations.

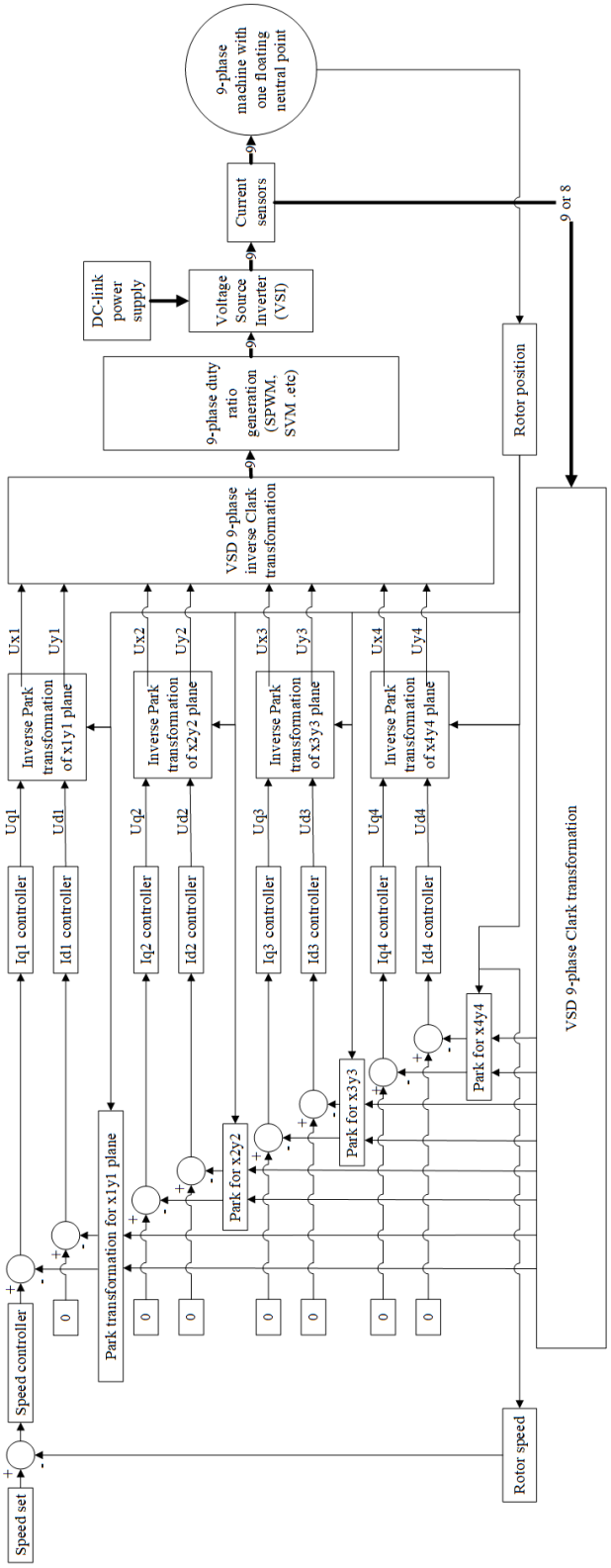


Figure 3.7 Vector control structure for 9-phase machine drive system.

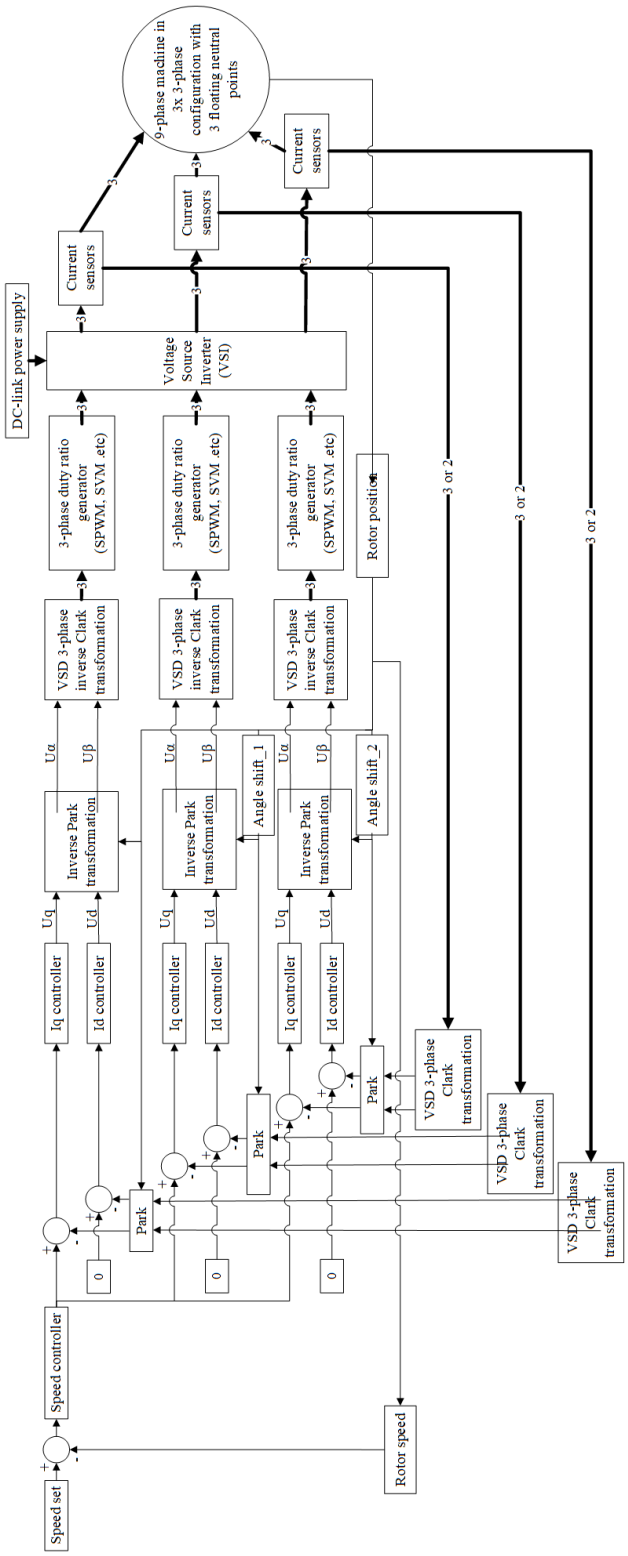


Figure 3.8 Vector control structure for 3x 3-phase machine drive system.

3.6 Experimental Validation and Analysis

The 9-phase BLPM machine in Figure 3.2 has a surface mounted permanent magnet rotor and a concentrated winding of which each phase has a resistance of 0.8 Ω, synchronous inductance 2.4 mH and phase back-EMF coefficient of 9.3 Vphrms/kRPM. Three SVM strategies containing 9-phase symmetrical SVM, discontinuous SVM, and balanced group based 3x 3-phase SVM, with SPWM as the benchmark are implemented experimentally to analyse, compare and evaluate different SVM strategies with the consideration of their phase current harmonics. The experiments are conducted with the following conditions: (i) DC-bus voltage = 110 V, (ii) switching frequency = 10 kHz, (iii) fundamental output frequency = 100 Hz electrical (1500 RPM mechanical) and (iv) the output torque 3.4 Nm.

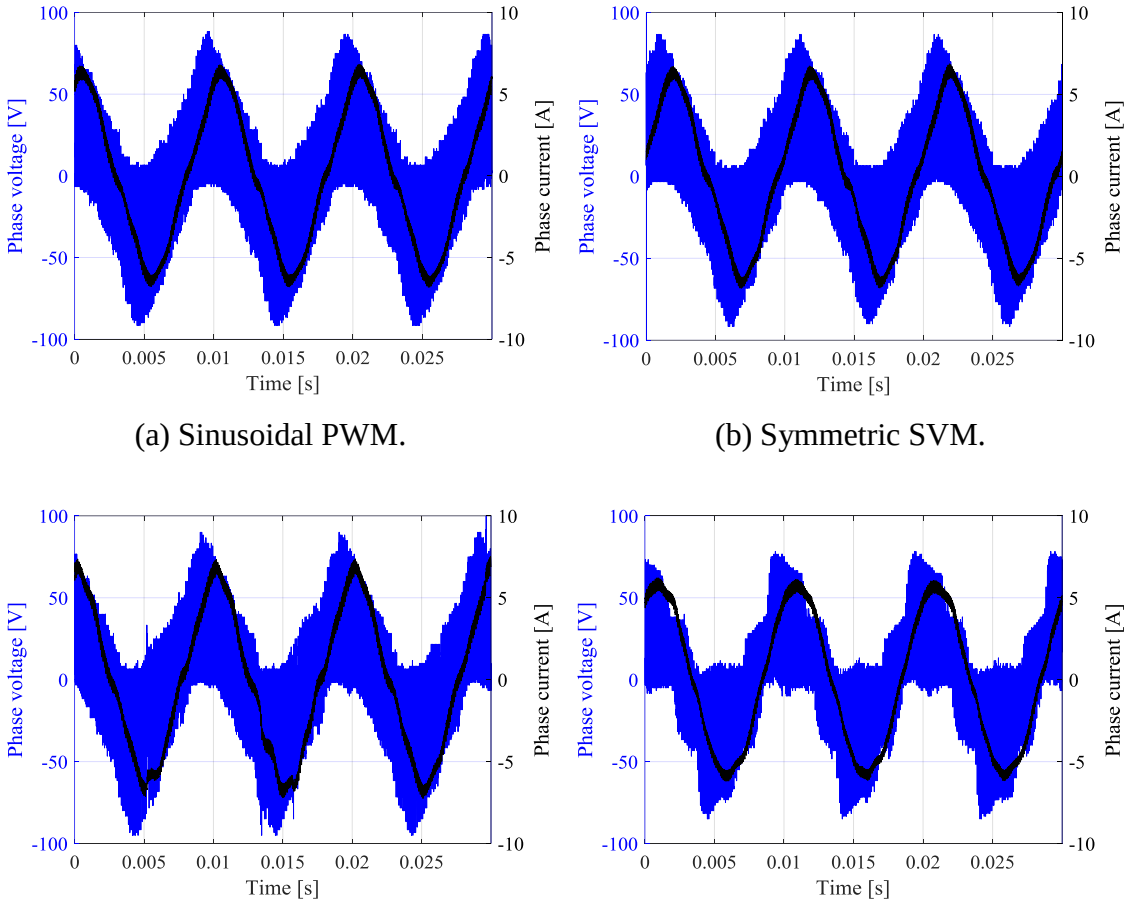
The selective active basic space vector SVM strategy, group D, has the highest phase current harmonic content because this strategy drives currents in the *x2y2, x3y3,* and *x4y4* planes, as previously discussed before. As a result, no further experimental validation is conducted for this strategy because of the inherent high phase current distortion.

Figure 3.9 shows phase 1 current and voltage waveforms in which the phase current distortion can be compared for the different strategies and Figure 3.10 shows phase 1 voltage and modulation index waveforms. To analyze the phase 1 harmonic content in detail, a Fast Fourier Transform (FFT) between 0 Hz to 1500 Hz is applied and the current spectra results are shown in Figure 3.11.

The balanced group based 3x 3-phase SVM has the least phase current distortion compared with other 9-phase switching strategies, as shown in Figure 3.9, and Figure 3.11. The third harmonic current is cancelled and this advantage over the other strategies is shown on the third harmonic content in Figure 3.11. This can also be observed in Figure 3.9, since it has the most sinusoidal shape phase current than the other examples. The 9-phase symmetrical SVM has a similar phase current distortion with the 9-phase SPWM. While the 9-phase discontinuous SVM controlled machine drive has the highest degree of phase current distortion, as can be observed on both the phase current of Figure 3.9 (c) and harmonic content shown Figure 3.11 (c). This is due to the modulation index distortion, and hence the phase voltage distortion, as shown in Figure 3.10 (c). Therefore, the balanced group

based 3x 3-phase SVM is the best choice among all the switching strategies in terms of the current harmonic content analysis.

Additionally, the machine drive system torque versus speed characteristics under the linear modulation operation region and different switching strategies are compared in Figure 3.12. The base speed under 3x 3-phase symmetrical SVM is the highest among the 9-phase SPWM, 9-phase symmetrical SVM and 3x 3-phase symmetrical SVM, indicating the best DC-link voltage utilization, thus confirming the analytical study presented before.



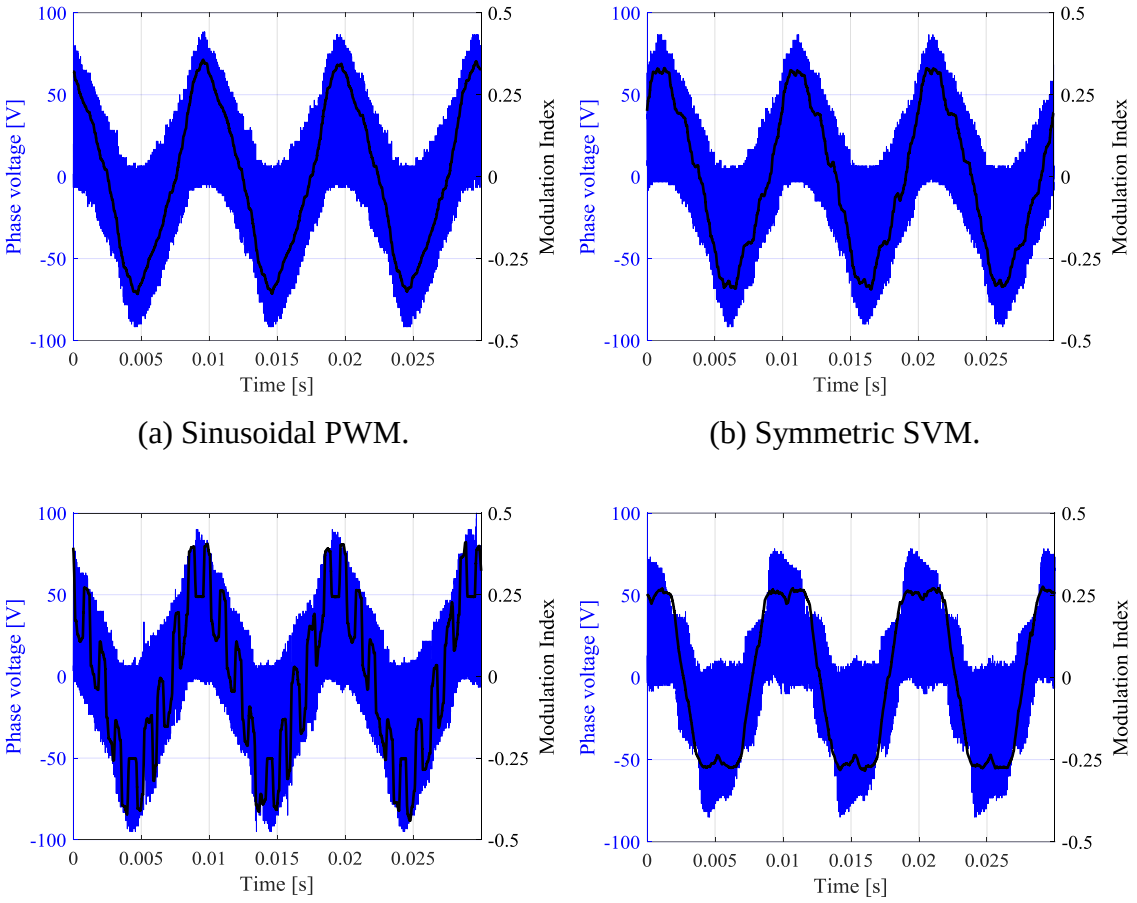
(a) Sinusoidal PWM.

(b) Symmetric SVM.

(c) Discontinuous SVM.

(d) Balanced group based 3x 3-phase SVM.

Figure 3.9 Phase 1 voltage and current waveforms for the different switching strategies investigated.



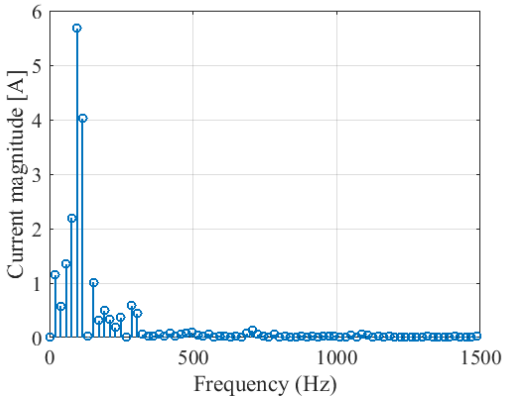
(a) Sinusoidal PWM.

(b) Symmetric SVM.

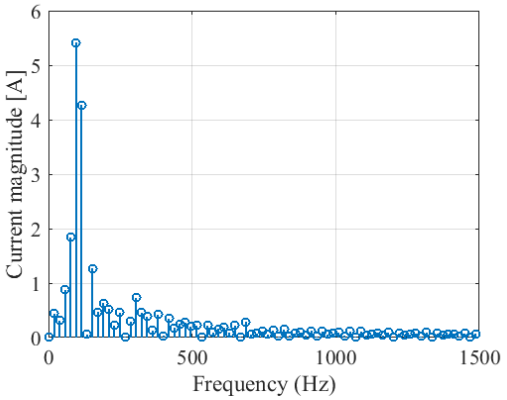
(c) Discontinuous SVM.

(d) Balanced group based 3x 3-phase SVM.

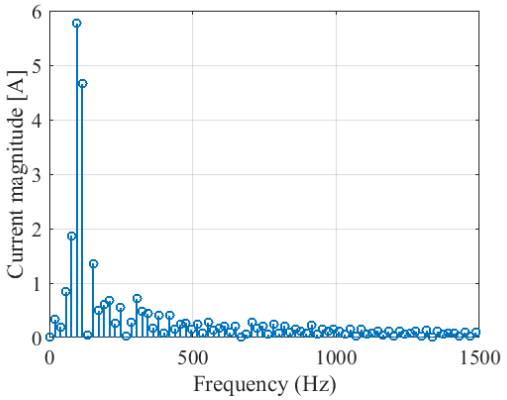
Figure 3.10 Phase 1 voltage and modulation index waveforms for the different switching strategies investigated.



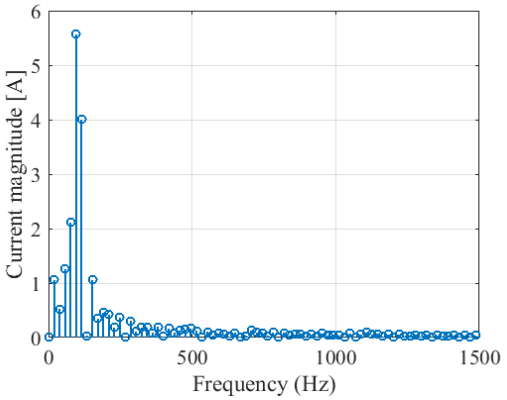
(a) Sinusoidal PWM.



(b) Symmetric SVM.



(c) Discontinuous SVM.



(d) Balanced group based 3x 3-phase SVM.

Figure 3.11 Experimental results of phase 1 current spectra.

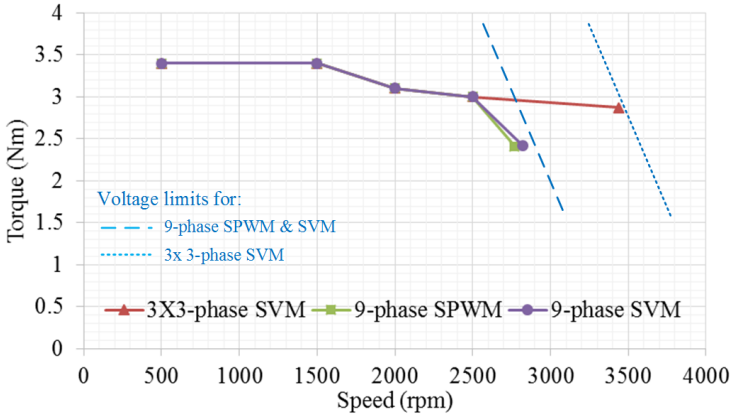


Figure 3.12 Machine drive torque-speed characteristics under different switching strategies, in the linear modulation region.

3.7 Summary

In this chapter the signal injection based symmetrical and discontinues SVMs have been generalized to an arbitrary phase number, multiphase machine drive system whose 3-phase counterpart can be implemented with these SVMs. Different SVM strategies have different performances including phase current distortion, harmonic content, DC-link voltage utilization and torque versus speed characteristics under the linear modulation operation region.

For multiphase systems with phase numbers greater than 3, SVMs implementing only the outermost basic space vectors have the best DC-link voltage utilization, hence the machine drive system speed capability can be extended. The detrimental effect of the proposed scheme is the increased phase current harmonic content which will impact on machine losses, although these are considered acceptable if the additional speed capability is transitory in nature, for example, during acceleration or deceleration.

Low phase number (odd number) systems have low order current harmonic cancellation characteristics, i.e. cancellation of the 3rd harmonic in 3-phase systems, the cancellation of the 5th harmonic in 5-phase systems etc. The multiphase systems with balanced group based SVMs and machine configuration can cancel specific orders of current harmonics caused by whichever switching schemes or machines. The unbalanced group based SVM concept is also proposed as a new option for the SVM family.

Experimental results validate the analytic study and show the cancellation of the 3rd current harmonic in 3x 3-phase SVM and the existence of the 3rd current harmonic in 9-phase SVMs. Due to the 3rd current harmonic cancellation, among these strategies, 3x 3-phase SVM has the least distorted phase current and hence the least machine ohmic losses. Additionally, the BLPM machine drive under 3x 3-phase SVM has the highest DC-link voltage utilization, hence the highest base speed or the best torque versus speed characteristics of the options studied. Consequently, 3x 3-phase SVM and its corresponding machine configuration is the best choice of the 9-phase VSI options and this conclusion could be extended and generalized to any multiphase machine drive systems capable of implementing balanced group based SVM.

Chapter 4

Multiphase VSI DC-link Capacitor Considerations

4.1 Introduction

A number of authors have reported on schemes to reduce the higher frequency ripple component at the DC input to VSIs [118]–[120]. However, they do not then carry this analysis or investigation forward to quantify the potential reduction in VSI DC-link capacitance. Further, the expansion of these studies as a function of phase number has not been reported to-date.

Consider an arbitrary n-phase, two level, voltage source inverter (VSI), as shown schematically in Figure 4.1 (a), where there are n-phase legs composed of either IGBTs, MOSFETs or other actively controlled semiconductor devices, a power supply from either rectified mains, or a DC energy storage device, for example, a battery and an n-phase load. Here the load is an AC machine having a per phase equivalent circuit comprising of an inductive-resistive impedance in series with a back-EMF.

The current and voltage ripples introduced by the inverter switch side are determined by inverter topology, switching schemes, control strategies, phase output current profile etc. The current and voltage ripples from the DC power source vary due to the types of the DC power sources, for example, utility grid connecting one-phase or three-phase rectifiers widely used in industrial drives, batteries or supercapacitors normally in electrical traction machine drive systems, i.e., electric vehicles (EVs) and more electric ship, DC-DC converters or AC-DC converters and so forth. Rectifiers normally have rectification output effects, the periodic voltage ripples with twice or six times the utility grid main frequency. The DC power sources of the electrochemical energy storage devices, i.e. batteries, have a

decreasing trend in output voltage due with decreasing state-of-charge (SOC) and instantaneous voltage ripples according to the varying voltage drop on the battery inner equivalent resistive-capacitive networks, resulting from the fluctuating current profile [121]–[123]. Just a few applications are mentioned here.

Continuing the former discussion, the functions of DC-link capacitors can be categorized [124]–[128]:

- Compensate power gap between the DC power source and the inverter switch side
- Supply the required pulsating current to the inverter switch side
- Reduce the pulsating current transmission from the inverter switch side to the power source side
- Absorb the drive side demagnetization and regeneration energy
- Protect against transient peak voltage from the power source side

The implementation of different DC power supplies can result in different voltage and current ripples on the DC-link capacitor, while the ripples introduced by the inverter switch side can be generally studied. As a result, the DC power supplies that introduce the least ripples, the battery or other electrochemical energy storage device in EVs, HEV applications as shown in Figure 4.1 (b), is considered in this chapter and the focus is on the DC-link voltage and current ripples introduced by the inverter switch side which is called the DC power supply idealization condition discussed in Chapter 4.3. The inductance L_i and resistance R_i are due to the current filter and the parasitic components between the DC power source and the DC-link capacitor, and the parasitic inductance and resistance between the DC-link capacitor and the inverter switch side, i.e. nano Henry level of inductance [129] and nearly zero resistance, are generally negligible due to their much smaller values compared with L_i and R_i.

Thus, DC-link capacitors function as transient energy stores stabilizing the DC-link environment and their specification requirements are dependent on both the DC power source and the inverter switch functions. The DC-link capacitance is chosen to limit the DC-link voltage ripple, a typical requirement being to control within 5% of the rated DC-link voltage [NS discussions]. Whereas the DC-link capacitor RMS current stress relates

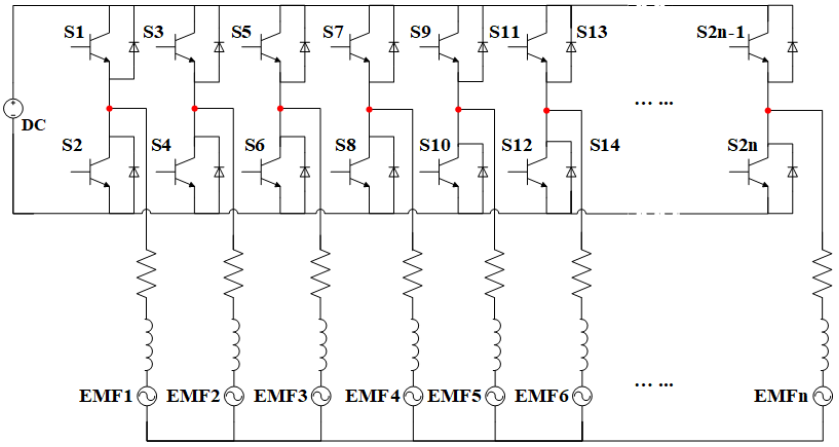
directly to component thermal performance; this usually being the parameter that determines the VSI DC-link capacitor requirements, i.e. the thermal performance of the capacitor as opposed to the Faradic necessity.

In terms of the inverter switch side, different switching schemes, for example the sinusoidal pulse width modulation (SPWM), space vector modulation (SVM) etc. discussed in the preceding chapters; different circuit topologies, for example, two-level, multilevel, one phase, three phase and multiphase, etc., and different inverter AC output currents, i.e. sinusoidal, rectangular etc., determine the inverter switch side input current ripple content and hence the DC-link capacitor current capacitance requirement. Considering the most applicable techniques in EVs, two level multiphase VSIs controlling sinusoidal phase currents are investigated under the linear modulation region SPWM and SVM.

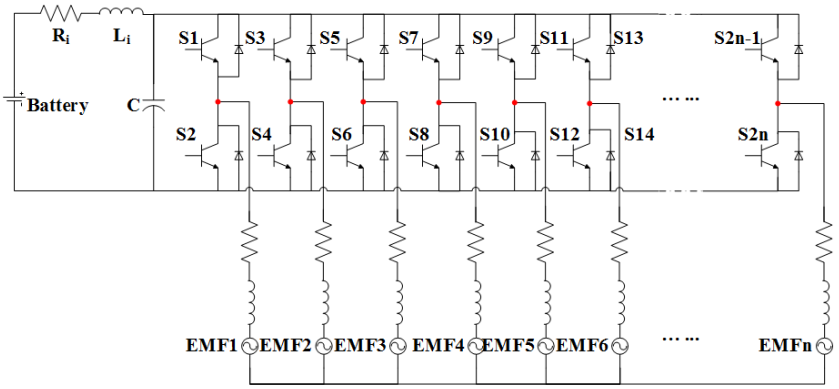
Additionally, among different components in a power electronics converter, DC-link capacitors are the most susceptible to environmental conditions and hence the most likely to fail, accounting the highest failure potential among different converter components, as shown in Figure 4.2. Moreover, the DC-link capacitor volume is a significant percentage of the whole converter volume, typically about two-thirds [130], hence converter power density is linked to capacitor volume. Thus, both converters reliability and volume considerations relate to the DC-link capacitor electrical performance in terms of DC-link capacitor current rating and Faradic capacitance. Although some investigations have been done on DC-link capacitor reduction by increasing the machine drive system phase number from 3-phase to 9-phase [55], interleaving two sets of 3-phase VSIs [131], [132] and phase shifting in a 4-phase DC-DC converter [133], a comprehensive DC-link capacitance and RMS current rating investigation; generalized investigation method and DC-link capacitor design procedure for arbitrary phase number VSIs has not been published to-date.

In this chapter, the relation between the DC-link capacitor volume, and the RMS current and capacitance ratings is studied and concluded specifically for higher current, medium voltage, EV traction machine drive systems. The investigation method of DC-link capacitor requirements is developed firstly. Based on the method, the DC-link capacitor RMS current and capacitance ratings are investigated analytically, then generalized and compared for

different phase number VSIs with the consideration of different switching strategies, carrier waveforms and interleaving technologies. Moreover, for the higher phase number systems their increased flexibilities and degrees of freedom make it possible to decrease the DC-link capacitor requirements further by the implementation of different switching schemes and carrier waveform interleaving techniques. That is based on the investigation on 2x 3-phase (one special 6-phase system), 4x 3-phase (12-phase), 2x 5-phase (10-phase), 5x 3-phase (15-phase), 3x 5-phase (15-phase), 6x 3-phase (18-phase), 4x 5-phase (20-phase), and 9x 3-phase (27-phase) VSIs. Furthermore, the new conceptual Gx paralleled n-phase inner-phase pseudo-multiphase VSI (IPPM-VSI), is proposed and its DC-link capacitor investigation is studied on 2x paralleled 9-phase and 4x paralleled 9-phase IPPM-VSIs which are compared with the 9-phase VSIs. The study of this chapter is validated experimentally via a 3-phase brushless permanent magnet (BLPM) machine drive system and a 9-phase BLPM machine drive system with equivalent load performance demands. The experimental facility and subsequent test validation are discussed in detail in Chapter 5.



(a) n-phase VSI and an n-phase AC machine load.



(b) n-phase VSI with an n-phase machine load powered by battery on the DC-link.

Figure 4.1 n-phase VSI.

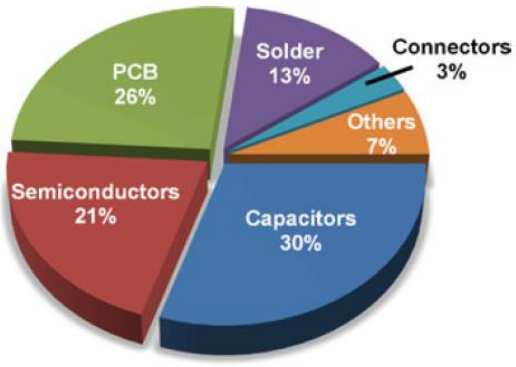


Figure 4.2 Power electronics converter failure possibilities introduced by different components [98].

4.2 Electrolytic and Film Capacitors for VSI DC-link

4.2.1 Power Capacitor Types and Comparison

Capacitors can be categorized into electrolytic capacitors, film capacitors and ceramic capacitors [125], [134], of which aluminum electrolytic capacitors, metallized polypropylene film capacitors, and high capacitance multi-layer ceramic capacitors can be used as the VSI DC-link capacitors due to their high current ratings, high capacitance per unit volume, etc. [124], [125], [127], [135]–[140]. While compared with aluminum electrolytic capacitors ("electrolytic capacitors" in the following content) and metallized polypropylene film capacitors ("film capacitors" in the following content), multi-layer ceramic capacitors are less commonly applied as VSI DC-link capacitors due to their cost and capacitance sensitivity to temperature and terminal voltages [125], [141]. Therefore, this thesis investigation will focus on electrolytic and film capacitors.

Compared with film capacitors, electrolytic capacitors have larger capacitance per unit volume with smaller RMS current ratings, though they are less reliable, cannot withstand reverse voltage, and have shorter load life, leading to their being the most (lifetime) vulnerable component of VSIs [127], [139], [142]. Taking aluminum electrolytic capacitors as an example, the life at the maximum permitted core temperature is 10,000 hours; while film capacitors have about ten times the life time at 100,000 hours [128], [137]. Electrolytic capacitor life time depends on the degree of electrolyte evaporation and deterioration. In VSIs employing electrolytic capacitors, most of the VSI failures are due to electrolyte failures [128]. In terms of the equivalent series resistance (ESR), a comparison between film capacitors and electrolytic capacitors illustrates that electrolytic capacitors have higher ESR, a parameter that is also sensitive to temperature and increases with their deterioration [135], [138], [143]–[146]. In terms of the frequency response, electrolytic capacitor ESR values decrease with increasing frequency, while this trend reverses for film capacitors [126].

4.2.2 Capacitor Modelling

The equivalent circuit of electrolytic capacitors can be modelled as illustrated in Figure 4.3 (a), where R_0 represents the sum of foil, tabs, and terminals resistances, R_1 accounts for the resistance introduced by electrolyte, C_1 indicates the terminal capacitance and R_2 and C_2 stand for dielectric dynamics [126], [143], [147], [148]. From this circuit, the ESR can be expressed as a frequency dependent formula [126], [143], [147], [148]:

$$ESR = R_1 + R_0 + \frac{R_2}{1+\left(2\pi f R_2 C_2\right)^2} \tag{4.1}$$

where f represents the frequency at the capacitor terminals.

The periodic current through the capacitor can be decomposed via Fourier transformation into infinite numbers of harmonic components, each of which has its own harmonic frequency, f_n, and ESR_n given by:

$$ESR_n = R_1 + R_0 + \frac{R_2}{1+\left(2\pi f_n R_2 C_2\right)^2} \tag{4.2}$$

From Equation (4.1), the ESR is inversely proportional to the square of frequency. ESR frequency dependence for a commercial device is shown in Figure 4.3 (b), where f_1 and f_2 denote low frequencies, f_3 is 2 kHz and f_n represents high frequencies, from which R_2 variation should be considered over the low frequency range, while negligible are the high frequency range. Consequently, the ESR at high frequency is nearly constant and much lower than that at low frequencies, resulting in less power losses and hence the higher RMS current rating under high frequencies [128].

ESR is also temperature dependent due to the thermal dependency of the electrolyte conductivity. The main contribution is given by R_1, whose resistance can be represented by a function of temperature:

$$R_1 = R_{1base} e^{\frac{T_{base}-T}{F}} \tag{4.3}$$

where R_{1base} is the resistance value at T_{base}, T is the capacitor electrolyte temperature and F is a temperature sensitivity coefficient [126], [147], [148]. The temperature dependency of ESR is also shown in Figure 4.3 (c). Note, a typical base temperature is 27 °C.

The equivalent circuit of film capacitors is shown in Figure 4.4 (a), in which the ESR is the ohmic part of three elements, R_{pol} representing Joule losses of dielectric material, R_S indicating the resistance of leads, terminals and electrode, and R_{is} accounts for the insulation resistance [149]. The parasitic inductance, L, is dependent on the geometric design of the capacitor elements, the length and thickness of leads [149].

The ESR can be modelled by a function of frequency[126], [150]:

$$ESR(f) = R_s + (K-1)a \tag{4.4}$$

where R_S is the base resistance at nominal temperature and frequency, α is a constant relating to the capacitor geometry, and K is a frequency dependent factor, as shown in Figure 4.4 (b).

4.2.3 Capacitor Dimensions

The dimensions of electrolytic and film capacitors are investigated here on the basis of the capacitor principle that the capacitor physical model can be simplified to the structure with two electrically conductive material layers separated by a dielectric layer. The aluminum electrolytic capacitor physical model is shown in Figure 4.5 (a) where the aluminum anode and cathode foils are separated by the dielectric, and the electrolyte and paper layers [151]. The film capacitor geometry, e.g., the electrode foils and dielectric layers distribution and layout, are similar with the aluminum electrolytic capacitor, however the layer materials are different, for example, plastic foil is applied in some film capacitor [152].

The capacitance can be calculated via [151]:

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d} \tag{4.5}$$

where ε_0 – is absolute permittivity, ε_r – the dielectric material relative permittivity, A - capacitor electrode surface area and d – the distance between the two electrodes.

The dielectric layer material relative permittivity, ε_r, is required if an electrolyte material is selected. For air cared capacitors $\varepsilon_r = 1$ and, since ε_0 is constant, the capacitance is only dependent on A and d. To simplify the analysis and comparison, it is assumed here that d is also fixed for a given operating DC-link rated voltage relating to the dielectric material thickness and hence the insulation grade. Consequently, the capacitance is proportional to A, hence the volume of the capacitor (d is fixed), if the volumes of the terminals, insulation and sealing accessories are considered negligible when compared with the capacitance-related volumes, as shown in Figure 4.5 (b).

From these simplifying assumptions, a comparison of different commercial electrolytic capacitors, the KEMET's ALS60/61 series, for a rated DC voltage of 550 V, is illustrated in Figure 4.6 (a). Here, capacitance versus the corresponding volume is made and indicates that the capacitance is approximately proportional to the capacitor volume as intuitively expected from the above discussion.

Despite the rated voltage and required capacitance that are determined by the VSI DC-link voltage and voltage ripple constraints respectively, the capacitor RMS current affects the capacitor dimensioning. Assume that the capacitor internal Joule heat is generated uniformly and the temperature distribution is even in the 3-dimensional space of the capacitor so that the required capacitor volume is proportional to the capacitor Joule heat/power loss, e.g., the power loss per volume for different current rating capacitors remains the same. However, this is not a very accurate estimation because the thermal network and power dissipation inside a capacitor are complicated and not uniformly distributed. Further, under steady-state conditions the peak temperature normally occurs in the center of the capacitor. Here, it is assumed that these facts are negligible to simplify and approximate the study.

The capacitor power dissipation can be calculated as [124], [142], [151], [153]:

$$P_C = R_{ESR\ @\ typical\ Hz} I_{C,equ}^2 \tag{4.6}$$

where $R_{ESR\ @\ typical\ Hz}$ is the capacitor ESR at typical frequency and $I_{C,equ}$ is the equivalent RMS current value at typical frequency.

The capacitor current contains different current harmonic components having corresponding capacitor ESRs. To simplify the power loss calculation the ESR is assumed to be a constant at the typical frequency, $R_{ESR\ @\ typical\ Hz}$ given by the manufacturer, i.e., ESRs quoted at 100 Hz or 120 Hz, and the other current harmonic components, are thermally equivalently converted and superimposed to current harmonic components at the typical frequency – $I_{C,equ}$. The equivalent RMS current at typical frequency can thus be calculated as [124], [142], [151], [153]:

$$I_{C,equ}^2 = \sum_{fi} K_{fi} I_{C,(fi),equ}^2 \tag{4.7}$$

K_{fi} can be denoted as:

$$K_{fi} = \frac{R_{ESR@\,fi}}{R_{ESR@typicalHz}} \tag{4.8}$$

where $R_{ESR@fi}$ is the capacitor resistance at the frequency of f_i.

For the PWM controlled IGBT based VSIs in EV traction machine drive systems, the switching frequencies typically range between 5 kHz to 10 kHz resulting in high frequency current harmonics on the DC-link capacitor. From the previous discussion, capacitors have nearly constant ESRs in the high frequency range (above 2.5 kHz), hence the same K_{fi} can be assumed for all the current harmonic components in the high frequency range. So the equivalent RMS current at typical PWM frequencies is:

$$I_{C,equ} = \sqrt{K_{fi}} I_{C,rms} \tag{4.9}$$

where $K_{fi} = 0.794$ for the ALS3(1)(2)471DA200 capacitor in [154].

The power loss per volume can be calculated as:

$$\frac{P_C}{Volume\_C} = \frac{R_{ESR@typicalHz} I_{C,equ}^2}{Volume\_C} \tag{4.10}$$

where *Volume_C* - the capacitor volume.

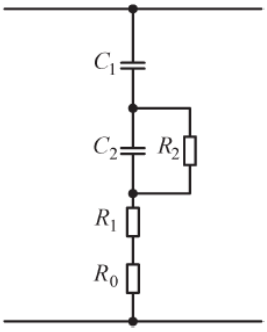
According to Equation (4.10), the capacitor RMS current rating is proportional to the capacitor volume. Figure 4.6 (b) shows the current ripple RMS ratings versus capacitor volume for different KEMET's ALS60/61 series electrolytic capacitors at 85°C and for both 100 Hz and 10 kHz. The capacitor ESR is inversely proportional to the conductor cross sectional area and electrode surface area. Hence, this relationship can be verified by the capacitor ESR versus capacitor volume for different KEMET's ALS60/61 series electrolytic capacitors, as illustrated in Figure 4.6 (c), which shows the general inversely proportional trend between ESRs and capacitor volume. These general trends correspond to the analytical study that concludes the proportionality between capacitor current ripple RMS rating and volume.

Similarly, Figure 4.7 illustrates the capacitances (a), RMS current ripple ratings (b) and ESRs (c) versus capacitor volume for C44A MKP series film capacitors, with a rated DC voltage of 600V. The results of Figure 4.7 show similar trends to the electrolytic capacitors results of Figure 4.6, except the ESR versus capacitor volume. For film capacitors, the ESR is not closely dependent on the capacitor volume and its value is much lower than that of an electrolytic counterpart.

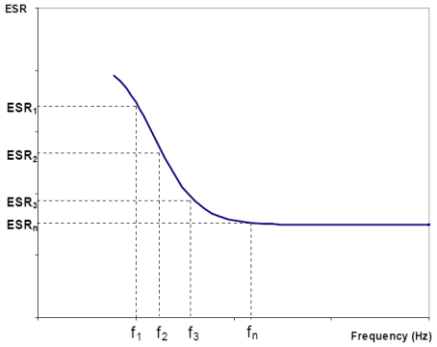
The results for the KEMET's ALS60/61 series, 550V, electrolytic capacitors shown in Figure 4.6 and the KEMET's C44A MKP series, 600V, film capacitors shown in Figure 4.7 are combined in Figure 4.8 for ease of comparison.

From the previous study and comparisons, at a representative voltage level, capacitor capacitance, RMS ripple current and ESR are related to capacitor volume. Additionally, for the high current and medium power application, i.e. EV traction machine drive systems, the film capacitor technology is a better choice and the capacitor volume is dependent of the rated RMS current, the thermal performance consideration [155]. Consequently, the

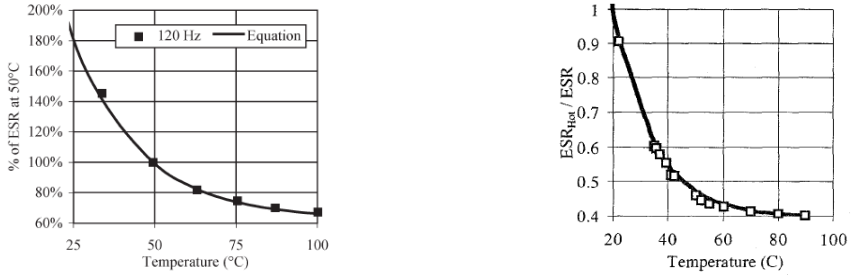
capacitor volume is proportional to the capacitor RMS current rating in the investigation in this chapter.



(a) Equivalent circuit of an electrolytic capacitor [6].

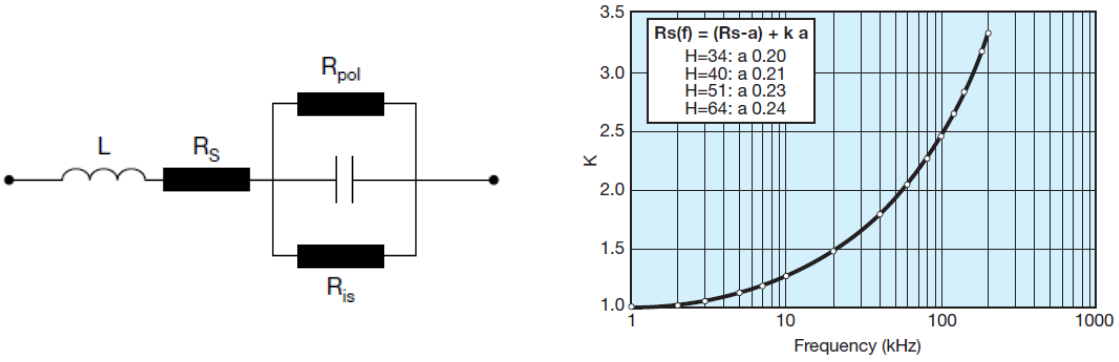


(b) Electrolytic capacitor ESR_n versus fundamental (1) and harmonic frequencies [128].



(c) Temperature dependency of electrolytic capacitor ESR [143], [147].

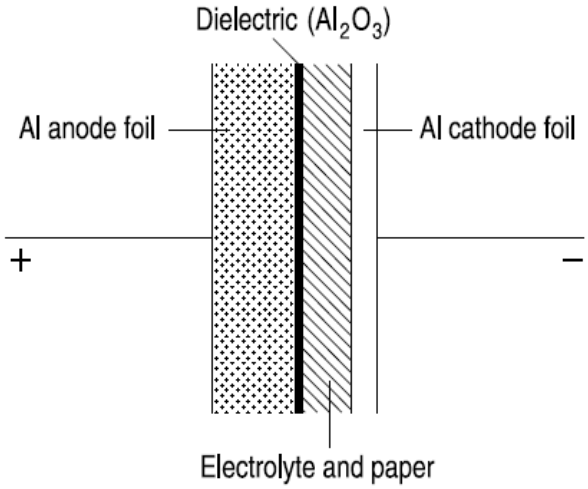
Figure 4.3 ESR of a typical electrolytic capacitor.



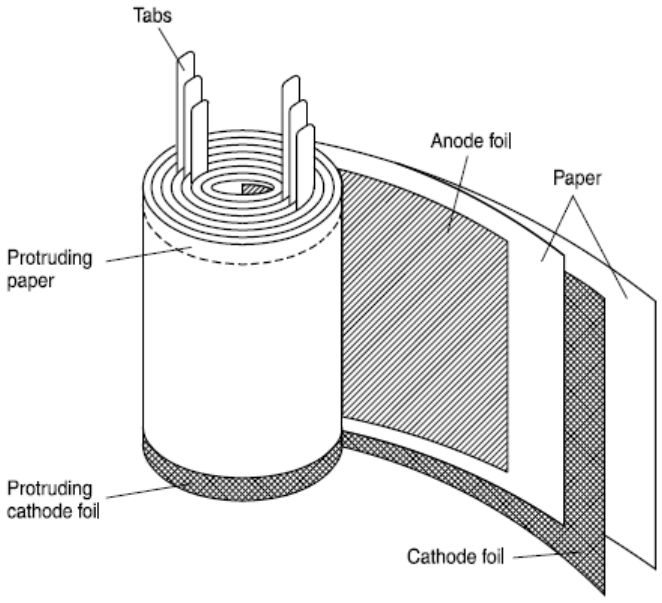
(a) Equivalent circuit of film capacitors [149]

(b) Frequency dependent factor – *K* for frequencies higher than 1 kHz [150].

Figure 4.4 ESR of a typical film capacitor.

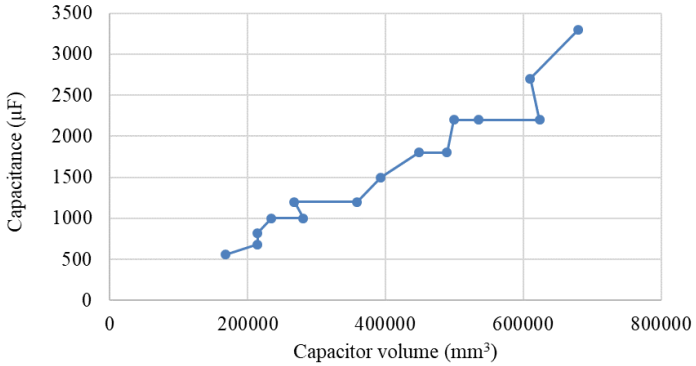


(a) Simple physical model of an aluminum electrolytic capacitor [151].

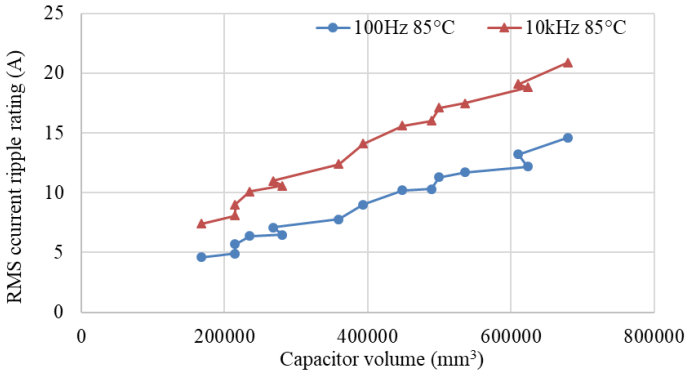


(b) Construction of an aluminum electrolytic capacitor [151].

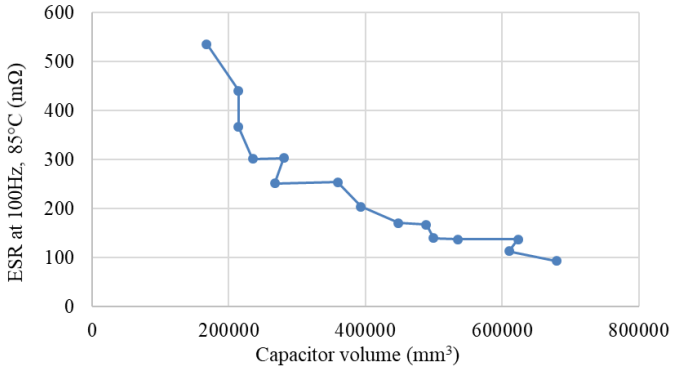
Figure 4.5 Electrolytic capacitor model and structure.



(a) Capacitances versus capacitor volumes.

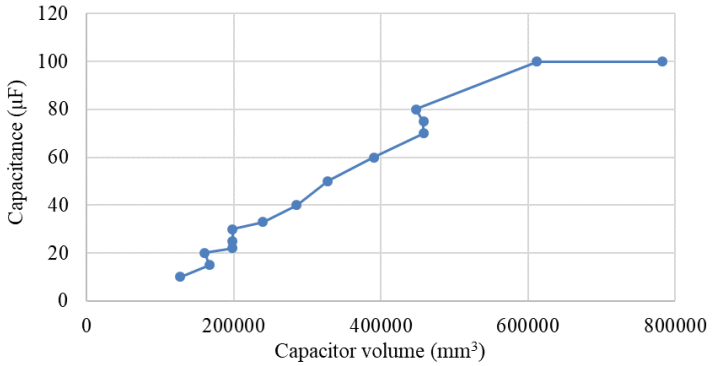


(b) Capacitor RMS current ripple ratings versus capacitor volumes.

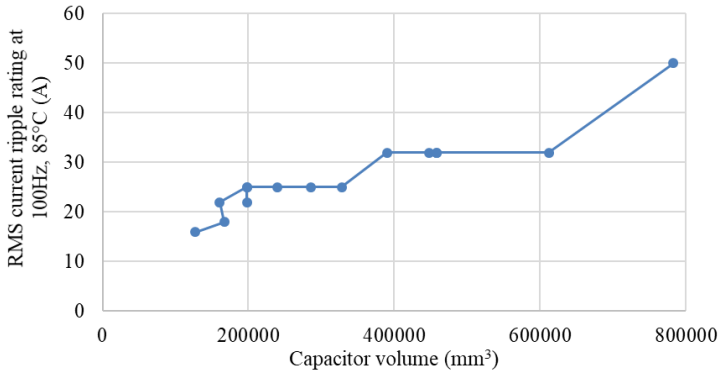


(c) Capacitor ESRs versus capacitor volumes.

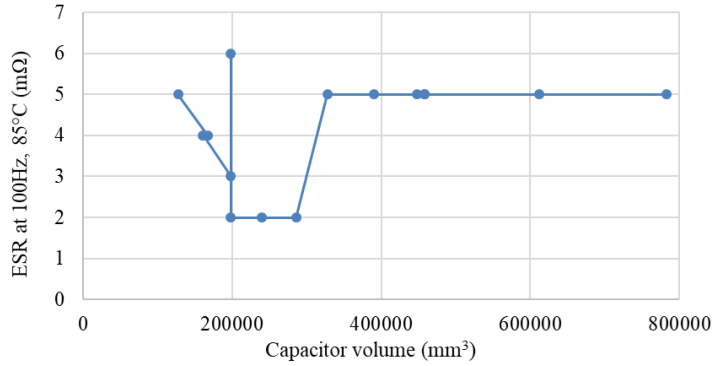
Figure 4.6 KEMET's ALS60/61, 550V, series electrolytic capacitors specification [156].



(a) Capacitances versus capacitor volumes.

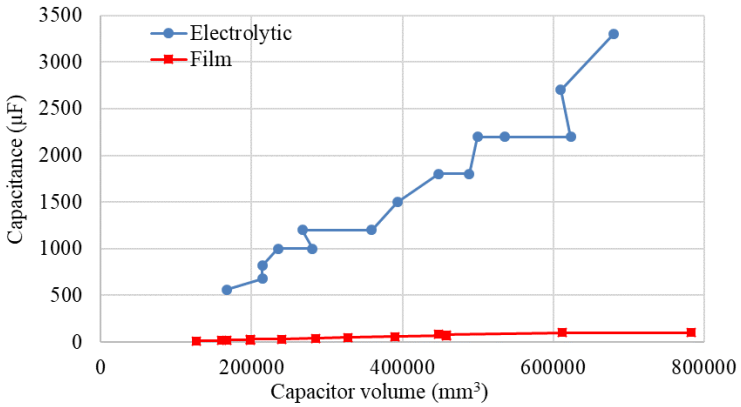


(b) Capacitor RMS current ripple RMS ratings versus capacitor volumes.

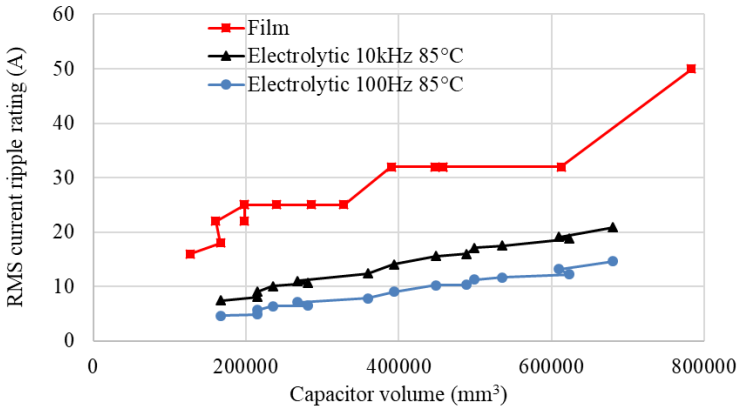


(c) Capacitor typical ESRs versus capacitor volumes.

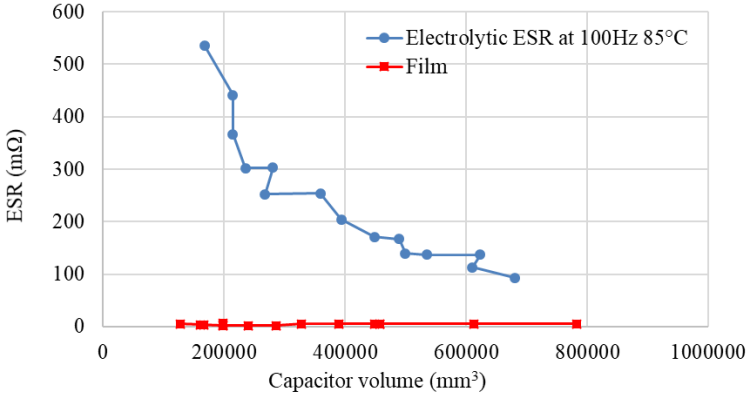
Figure 4.7 KEMET's C44A MKP, 600V, series film capacitors specification [157].



(a) Capacitances versus capacitor volumes.



(b) Capacitor RMS current ripple ratings versus capacitor volumes.



(c) Capacitor ESRs versus capacitor volumes.

Figure 4.8 Specification comparison between the KEMET ALS 60/61, 550V, electrolytic and C44A MKP, 600V, film capacitors [156], [157].

4.3 VSI DC-link Capacitor Requirements Investigation

In this section, an investigation is conducted within the linear modulation region SPWM with non-interleaved, triangular carrier and controlled sinusoidal phase current – the most representative strategy applied to VSIs driving PM and IMs. That is followed by a into DC-link capacitor current due to:

- VSI switching schemes – SPWM or SVM
- Carrier waveform shapes – triangular or saw tooth, and
- Carrier waveform – interleaving or non-interleaving.

4.3.1 Investigation Methodology

SPWM gate switching signals are generated by the comparison between the carrier waveform (here the triangular carrier waveform) and the sinusoidal voltage control waveforms generated from the drive system controller as shown in Figure 4.9 (a) for 3-phase and (b) for 9-phase. The triangular carrier waveform is given by:

$$Tri(t)=\begin{cases}\dfrac{2}{T}t & 0\le t<\dfrac{T}{2}\\ -\dfrac{2}{T}t+2 & \dfrac{T}{2}\le t<T\end{cases} \quad and \quad Tri(t)=Tri(t+kT) \tag{4.11}$$

where T is the period of the triangular carrier waveform, k is non-negative integer, and t is time.

The voltage control waveforms, duty ratios, for each phases in an n-phase VSI are:

$$\left.\begin{aligned} d_{ph}(1,t) &= M\cos\left(\omega t+\varepsilon\right)+0.5\\ d_{ph}(2,t) &= M\cos\left(\omega t-\alpha+\varepsilon\right)+0.5\\ d_{ph}(3,t) &= M\cos\left(\omega t-2\times\alpha+\varepsilon\right)+0.5\\ &\vdots\\ d_{ph}(n,t) &= M\cos\left(\omega t-\left(n-1\right)\times\alpha+\varepsilon\right)+0.5\end{aligned}\right\} \tag{4.12}$$

where M is the modulation index, ω is the electrical frequency, α is defined in Chapter 3, and ε is the arbitrary angle.

Here the assumption is made that the phase current is sinusoidal and the phase currents in n-phase VSI are:

$$\left.\begin{aligned} I_{ph}(1,t) &= \hat{I}_{ph}\cos\left(\omega t-\phi+\varepsilon\right) \\ I_{ph}(2,t) &= \hat{I}_{ph}\cos\left(\omega t-\alpha-\phi+\varepsilon\right) \\ I_{ph}(3,t) &= \hat{I}_{ph}\cos\left(\omega t-2\alpha-\phi+\varepsilon\right) \\ &\vdots \\ I_{ph}(n,t) &= \hat{I}_{ph}\cos\left(\omega t-(n-1)\alpha-\phi+\varepsilon\right) \end{aligned}\right\} \tag{4.13}$$

where $\hat{I}_{ph}$ is the peak phase current, and ϕ is the current lagging angle with respect to the fundamental phase voltage (relating to power factor).

In each phase leg, four semiconductor devices containing upper switches and diodes, and lower switches and diodes take turns to conduct within one switching period – one switch or diode on simultaneously. A conduction function is introduced here to represent the state of these semiconductor devices, e.g., in phase i:

$$\left.\begin{aligned} &I_{ph}(i,t)\geq 0,\ d_{ph}(i,t)\geq Tri(t) \quad S_{upperSW}(i,t)=1 \quad others\ are\ 0 \\ &I_{ph}(i,t)\geq 0,\ d_{ph}(i,t)\leq Tri(t) \quad S_{lowerDI}(i,t)=1 \quad others\ are\ 0 \\ &I_{ph}(i,t)< 0,\ d_{ph}(i,t)< Tri(t) \quad S_{lowerSW}(i,t)=1 \quad others\ are\ 0 \\ &I_{ph}(i,t)< 0,\ d_{ph}(i,t)> Tri(t) \quad S_{upperDI}(i,t)=1 \quad others\ are\ 0 \end{aligned}\right\} \tag{4.14}$$

where "0" means the off-state of the corresponding device, "1" represents the on-state, subscript "upperSW" means the upper switch in one phase leg, "upperDI" means the upper diode in one phase leg, and similar for "lowerSW" and "lowerDI".

As shown in Figure 4.9 (c) and (d) the instantaneous input current in one phase leg equals to the summary of the upper switch current and upper diode current:

$$I_{phaseleg}(i,t)=\left[S_{upperSW}(i,t)+S_{upperDI}(i,t)\right]\cdot I_{ph}(i,t) \tag{4.15}$$

The inverter switch side instantaneous input current equals to the sum of the n-phase legs currents:

$$I_{inv}(t) = \sum_{i=0}^{n} I_{phaseleg}(i,t) \tag{4.16}$$

It is assumed that under VSI steady state operation all the current pulses introduced by the inverter switch side are absorbed by the DC-link capacitor while the DC power source provides constant current, consequently, only the inverter switch side pulsed current introduces the DC-link capacitor current. This is called power source idealization. So the DC-link capacitor current can be derived as the inverter switch side input current subtracted by the average of the inverter switch side input current in one electrical cycle:

$$I_{DCcap}(t) = I_{inv}(i,t) - \frac{1}{t_1}\int_0^{t_1} I_{inv}(i,t) \tag{4.17}$$

where t_1 is one electrical cycle.

The DC-link capacitor current and the phase current are shown in Figure 4.9 (e) and (f) for 3-phase and 9-phase systems. The DC-link capacitance is determined by the DC-link voltage ripple constraint specified as 5% of the rated DC-link voltage, from common industry practice.

The capacitor stored charge is given by:

$$Q = CV_{cap} \tag{4.18}$$

where Q is the stored charge in the DC-link capacitor, V_{cap} is the DC-link capacitor voltage and C is the capacitance assuming to be constant under different DC-link voltages, temperatures etc.

Equation (4.18) can be rewritten as:

$$Q = CV_{cap} = \int_0^t I_{DCcap}(t)\,dt \tag{4.19}$$

where I_{DCcap} is the capacitor current.

From Equations (4.18) and (4.19), the steady state stored charge in the capacitor within one electrical cycle can be calculated via Coulomb counting of the DC-link capacitor current, which results in the voltage ripple:

$$Voltage\ ripple = \frac{\Delta V_{cap}}{V_{DC}} = \frac{\Delta Q_{cap}}{CV_{DC}} = \frac{1}{CV_{DC}}\left(Q_{\max} - Q_{\min}\right) \tag{4.20}$$

where ΔV_{cap} is the voltage ripple magnitude on the DC-link capacitor, V_{DC} is the rated DC-link voltage, ΔQ_{cap} is the DC-link capacitor stored charge variation, Q_{max} is the maximum stored charge within one electrical cycle and Q_{min} is the minimum stored charge within one electrical cycle.

Q_{max} and Q_{min} are difficult to be estimated because they are DC-link capacitance dependent, and the initial DC-link capacitor stored charge is also unknown. While under steady state, the DC-link capacitor stored charge variation, ΔQ_{cap}, can be calculated by Coulomb counting of the DC-link capacitor current.

Figure 4.10 shows examples of DC-link capacitor current and the respective Coulomb counting results related to the DC-link capacitor stored charge variation for 3- and 9-phase VSIs, when the phase current magnitude is 1 A. When the switching frequency reduces from 10 kHz to 5 kHz as shown in Figure 4.10 (a) and Figure 4.10 (c), and Figure 4.10 (b) and Figure 4.10 (d), the DC-link capacitor current pulses are divided into two, while they still have the same peak values and the same RMS value. In other words, within the normal switching frequency range for IGBT driven VSIs, e.g. about 5 kHz to 20 kHz, the RMS of the DC-link capacitor RMS current ripple is essentially independent of the switching frequency. Additionally, if all the other parameters are the same except the fundamental frequency, a change of fundamental frequency will not change the RMS of the DC-link capacitor current ripple. In terms of the DC-link capacitor charge variation, increased switching frequency narrows the width of each DC-link capacitor current pulse while the peaks have the same magnitudes, resulting in reduced Coulomb counting and hence decreased stored charge variation. In more detail, the capacitor charge variation is

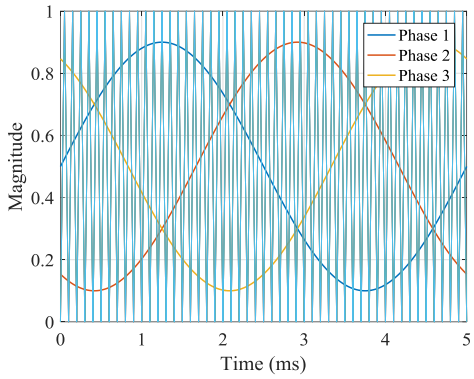
proportional to the pulsed current width and hence inversely proportional to the PWM switching frequency. Moreover, the change of the fundamental frequency does not change the peak of the DC-link capacitor current pulse. Therefore, the DC-link stored charge variation is independent of the fundamental frequency.

The DC-link capacitor current profile is determined by the VSI output phase current, PWM modulation index, controlled load power factor, PWM switching frequency and VSI output fundamental frequency. To simplify and generalize the analysis, and for comparison of results, the capacitors RMS current can be normalised to the VSI output phase RMS current. The independence of fundamental freqeuncy and switching frequency will be illustrated over the full range of modulation index and phase current angle (lagging only). The results shown in this chapter are under leading power factors (phase current lagging phase voltage) while the normalized values for both leading and lagging power factors are symmetrical. Hence the normalized values under leading power factors are representative and can be used to calculate the capacitor ratings.

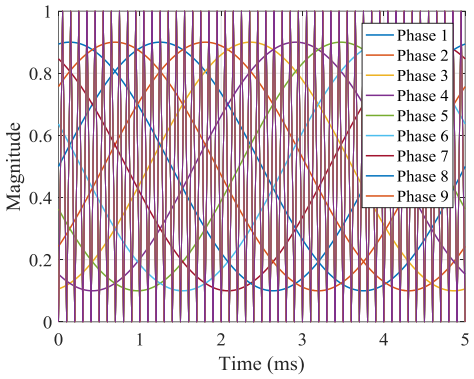
The normalized DC-link capacitor RMS current is calculated at different discrete points generating a continuous surface of results. Figure 4.11 (a) shows the normalized DC-link capacitor RMS current surface generation procedure. Each discrete point on the suface is calculated individually in discrete steps with 100 MHz simpling (10,000 times the switching freqeuncy of 10 kHz) in Matlab according to Equations (4.17) for which the continuous domain integration is converted to the discrete domain integration. The results for the normalized DC-link capacitor RMS current independence of fundamental and switching frequencies for the full range of whole modulation index and phase current angle range (lagging) is illustrated in Figure 4.12 (a) and Figure 4.12 (b).

For simplification and generalization purpose of the analytical study, the normalized DC-link capacitor charge variation is introduced, which is defined here as the DC-link charge variation divided by the phase current magnitude, leading to the unit of Coulombs per Ampere (using $\mu C/A$ for convenience). As discussed before, the normalized DC-link capacitor charge variation does not vary with the output fundamental frequency of the VSI, hence it is neglected. Therefore, the normalized DC-link capacitor charge variation is a

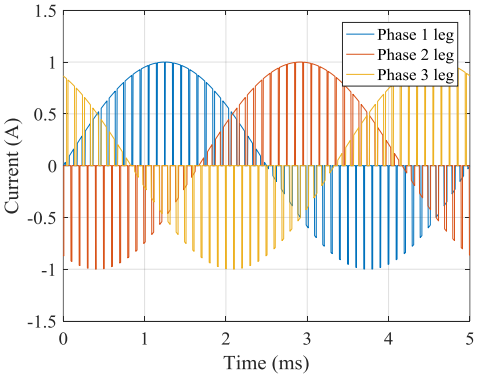
function of PWM modulation index, output power factor and PWM switching frequency, for which the switching frequency for the VSI design studied is fixed at 10 kHz. Hence, the only considered variables are the modulation index and power factor. The normalized DC-link capacitor charge variation for fundamental frequencies of 100 Hz, 200 Hz and 400 Hz converge to the same surface, as shown in Figure 4.12 (c), which confirms independence of the fundamental frequency. Moreover, the normalized DC-link capacitance variation dependency on the switching frequency, the inverse proportionality by the results shown in Figure 4.12 (d) at 5 kHz, 10 kHz and 20 kHz. Finally, the normalized DC-link capacitor stored charge variation calculation and surface generation procedure is shown in Figure 4.11 (b).



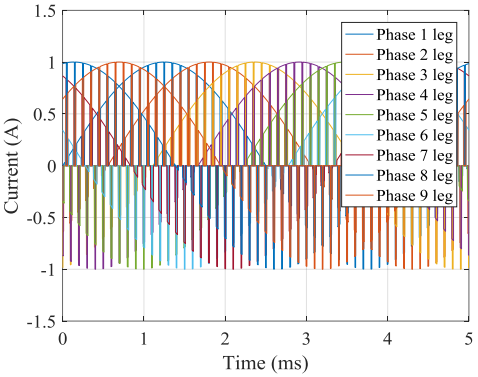
(a) 3-phase control signal and carrier waveform.



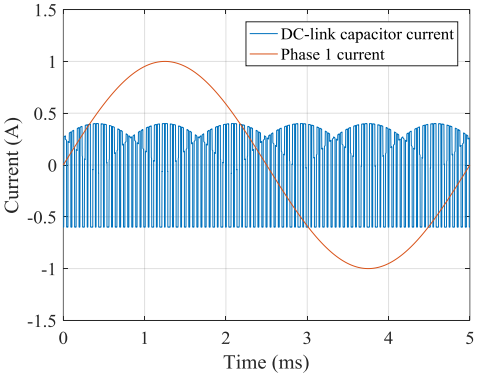
(b) 9-phase control signal and carrier waveform.



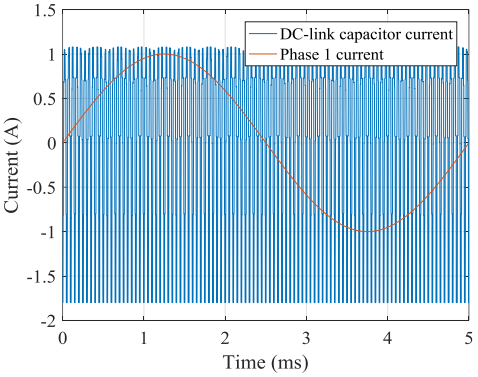
(c) 3-phase phase leg currents.



(d) 9-phase phase leg currents.

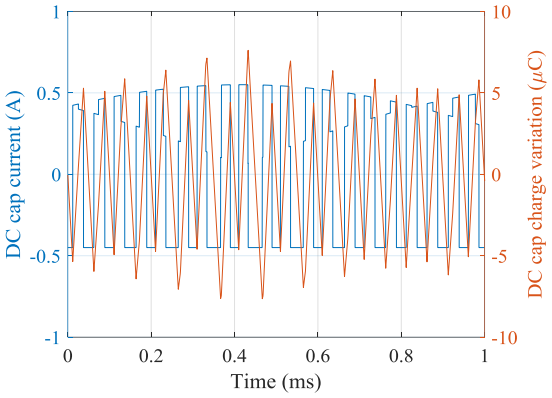


(e) 3-phase DC-link capacitor current.

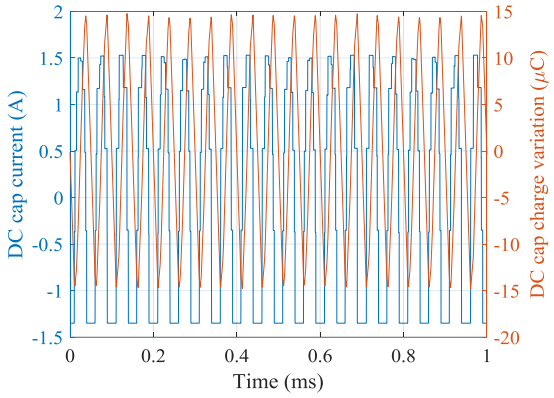


(f) 9-phase DC-link capacitor current.

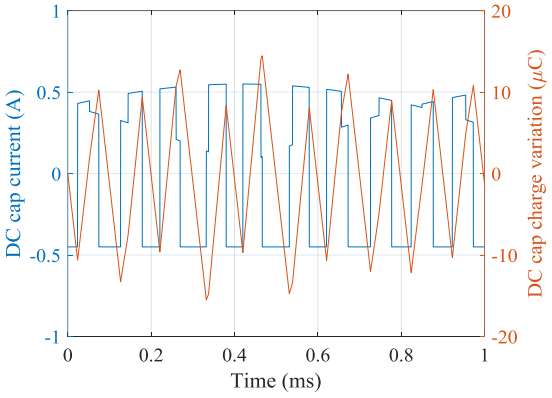
Figure 4.9 3-phase and 9-phase VSIs waveforms under modulation index 0.8, unity power factor and 10 kHz carrier waveform.



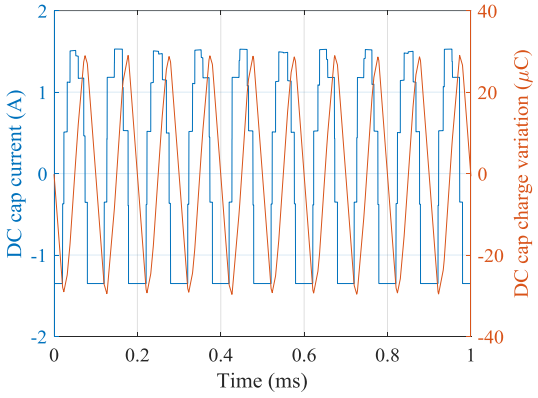
(a) 3-phase SPWM 10 kHz.



(b) 9-phase SPWM 10 kHz.

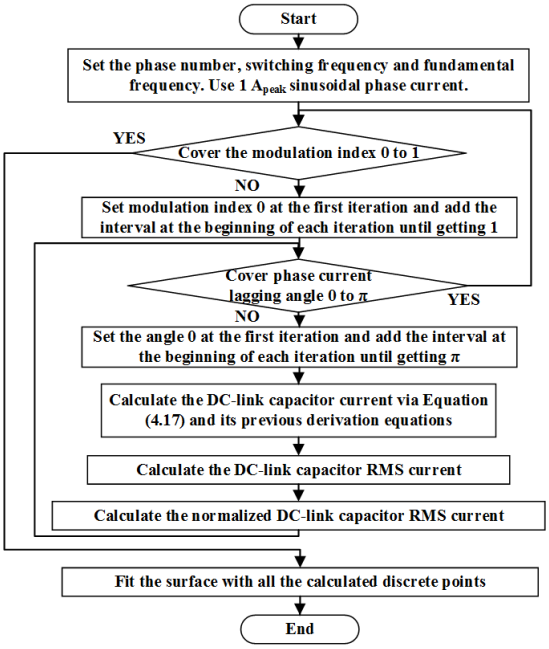


(c) 3-phase SPWM 5 kHz.

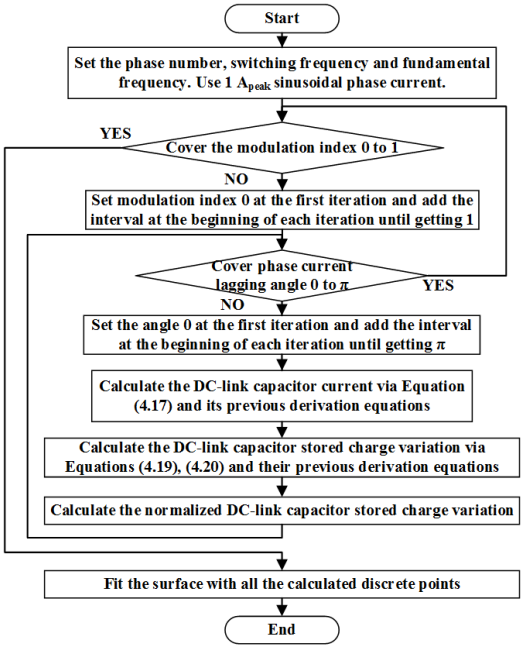


(d) 9-phase SPWM 5 kHz.

Figure 4.10 DC-link capacitor charge variation under 3 and 9-phase SPWM fundamental 200 Hz (unity power factor and modulation index 0.6).

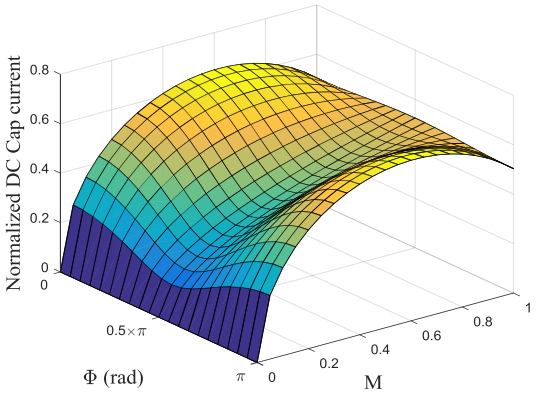


(a) Normalized DC-link capacitor RMS current calculation procedure.

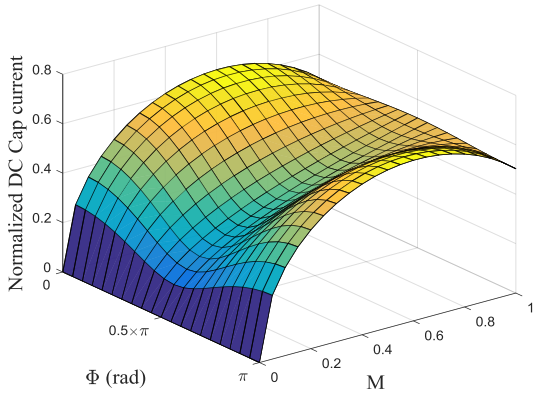


(b) Normalized DC-link capacitance calculation procedure.

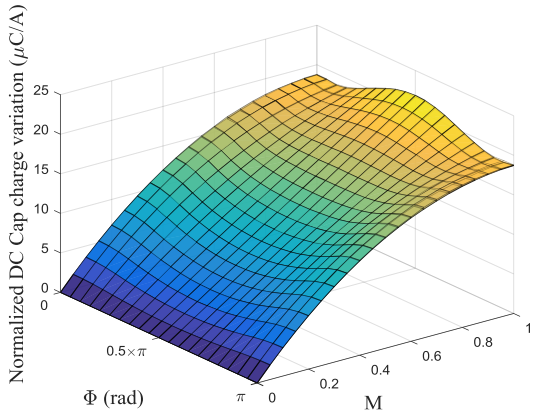
Figure 4.11 Normalized values calculation procedure.



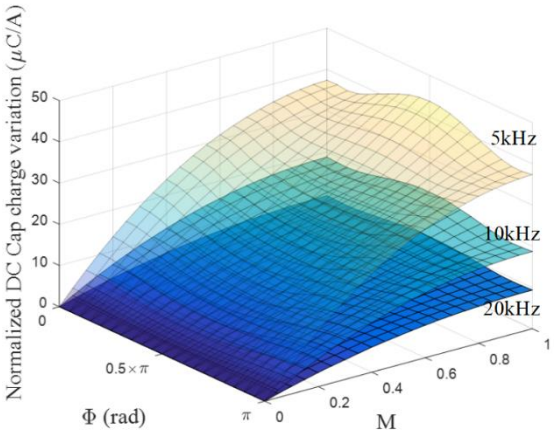
(a) Consistency under different fundamentals (100, 200, and 400 Hz coinciding) at 10 kHz switching.



(b) Consistency under different switching (5, 10, and 20 kHz coinciding) at 200 Hz fundamental.



(c) Consistency under different fundamentals (100, 200, and 400 Hz coinciding together) at 10 kHz switching.



(d) Relations among different switchings at 200 Hz fundamental.

Figure 4.12 The fundamental and switching frequency considerations for the normalized values.

4.3.2 Capacitor RMS Current Rating for Different Phase Number VSIs

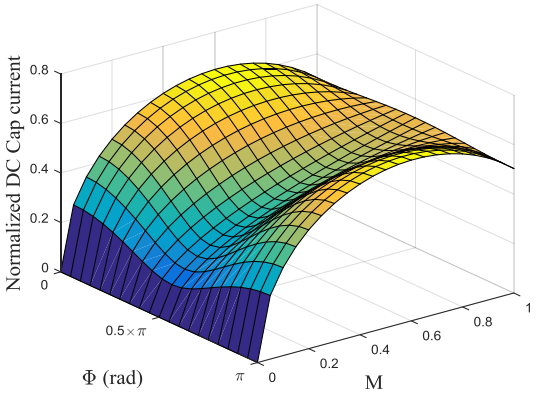
Results for the normalized DC-link capacitor RMS current from 3-phase to 20-phase VSIs are shown in Figure 4.13, Figure 4.14 and Figure 4.15. Note that due to the number os results presented, the results are splited between the three figures, i.e. Figure 4.13 for phase numbers 3 to 8, Figure 4.14 for phase numbers 9 to 14 and Figure 4.15 for phase numbers 15 to 20. The results show that there are two symetrical global peaks on the normalized DC-link capacitor RMS current surfaces, both occuring at unity power factor, motoring and generating, and for a modulation index 0.6. From Figure 4.13, Figure 4.14 and Figure 4.15, the maximum normalized DC-link RMS current for different phase number VSIs is detailed in Table 4.1. For equal power output, the phase current magnitude is inversely proportional to the inverter phase number, reflected by the normalized values in Table 4.1. The DC-link capacitor RMS current rating is the multiplication of the maximum normalized DC-link RMS current and the phase RMS current. The DC-link capacitor RMS current ratings for different phase number VSIs are compared in normalized values in Table 4.1 and Figure 4.16.

Figure 4.16 summarizes the results and show that the DC-link capacitor RMS current rating decreases slightly (about 10 %) with the increased phase number in VSIs.

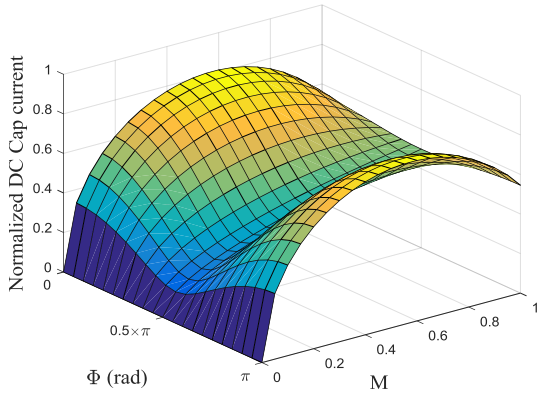
4.3.3 Capacitance Requirements for Different Phase Number VSIs

Results for the normalized DC-link capacitor charge variation from 3-phase to 20-phase VSIs (at 10 kHz) are shown in Figure 4.17 for phase numbers 3 to 8, Figure 4.18 for phase numbers 9 to 14 and Figure 4.19 for phase numbers 15 to 20. Here, the global peak values appear at unity power factor except for the 3-phase system whose maximum value is at the zero power factor operating point, as shown in Figure 4.17 (a). Under steady state operation most AC brushless machines have high power factors, usually above 0.7. Operationally, low power factor can occur under some transient states or for machines outside the scope of this study, i.e. synchronous reluctance or transverse flux machines. As a result, VSI operation over the full power factor range should be considered to calculate the DC-link capacitance to satisfy the DC-link voltage ripple within the aforementioned 5%

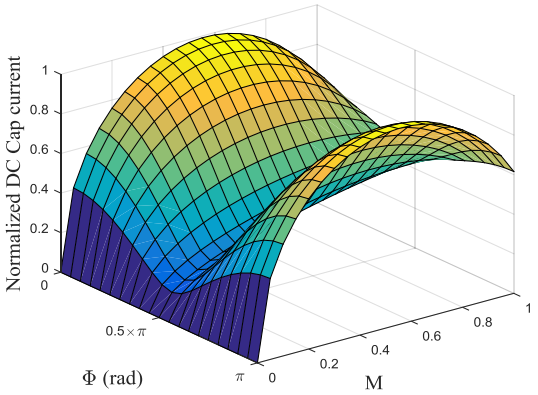
specification requirement. The maximum normalized DC-link charge variation under different phase number VSIs are given in Table 4.2. Similarly, for equal power output the phase current magnitude is inversely proportional to the VSI phase number. The required DC-link capacitance is proportional to the multiplication of the maximum normalized DC-link charge variation and the phase current, as shown in both Table 4.2 and Figure 4.20. Figure 4.20 summarizes the results and shows that the DC-link capacitance decreases with the increased phase number. Note that for the 9-phase VSI the reduction in capacitance is 54%, which is further explored in Chapter 5.



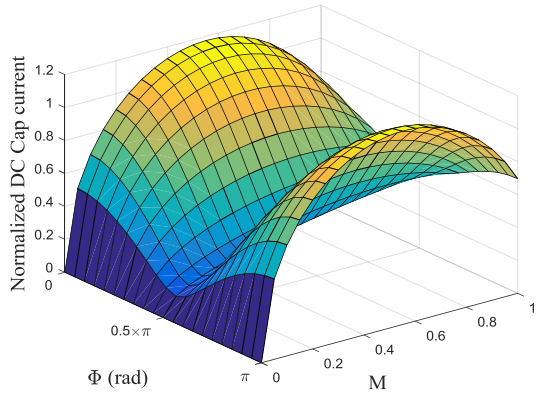
(a) 3-phase.



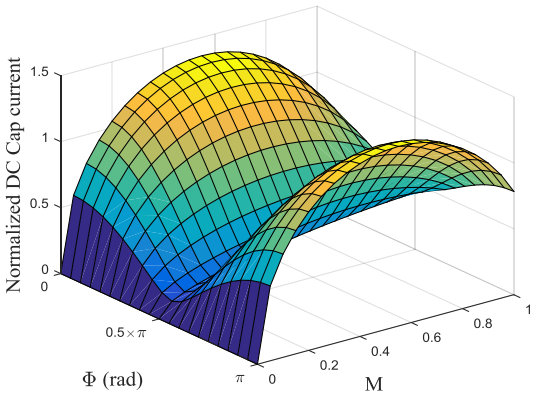
(b) 4-phase.



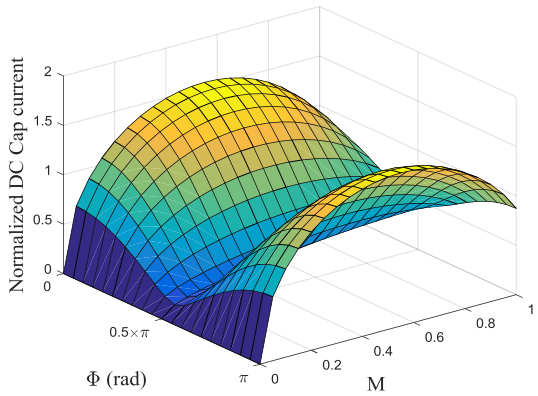
(c) 5-phase.



(d) 6-phase.

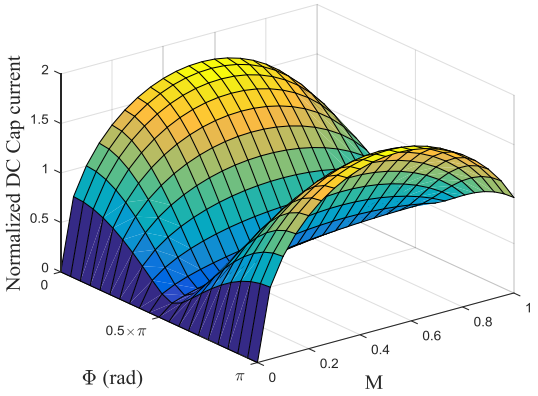


(e) 7-phase.

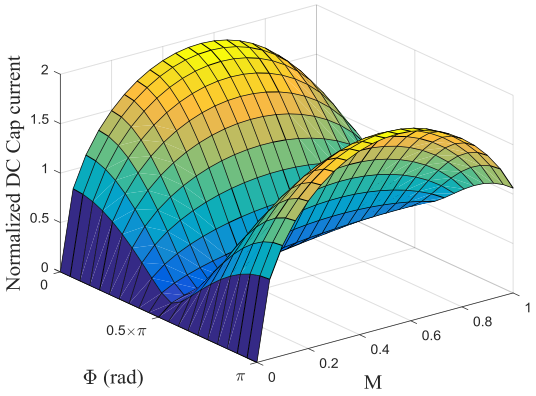


(f) 8-phase.

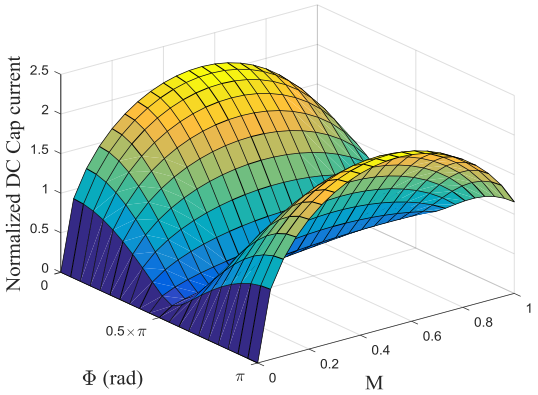
Figure 4.13 Normalized DC-link capacitor RMS current under SPWM and 10kHz triangular carrier for different phase number VSIs.



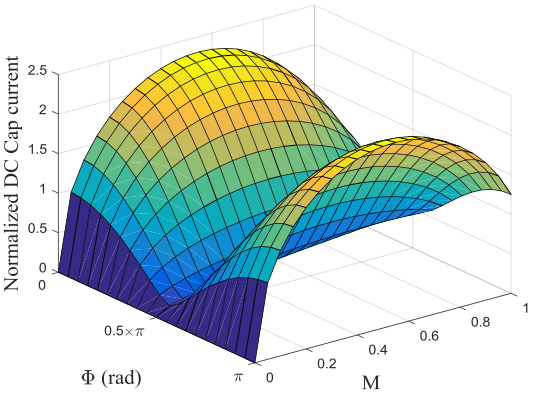
(a) 9-phase.



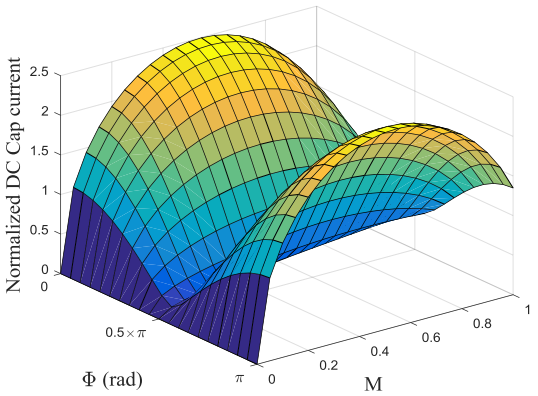
(b) 10-phase.



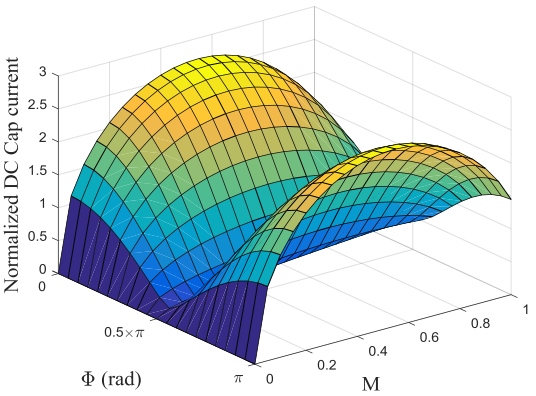
(c) 11-phase.



(d) 12-phase.

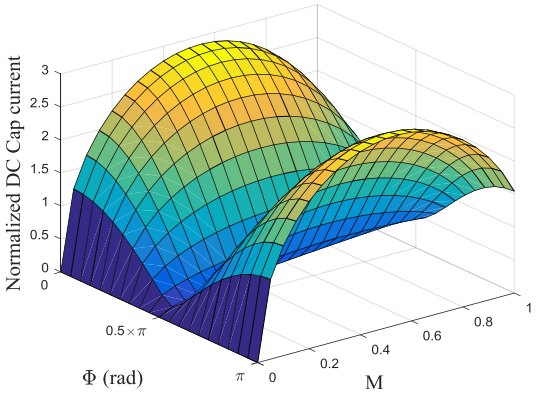


(e) 13-phase.

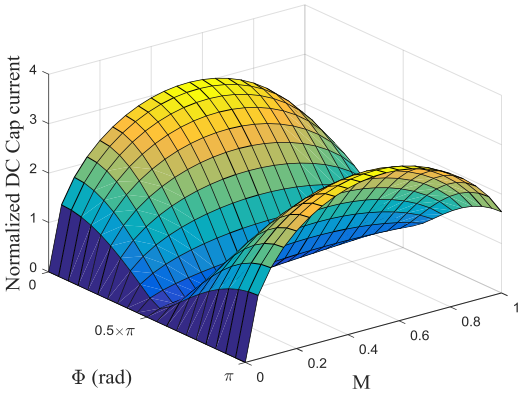


(f) 14-phase.

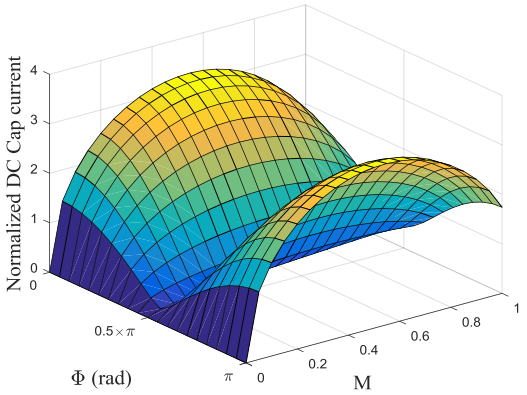
Figure 4.14 Normalized DC-link capacitor RMS current under SPWM and 10kHz triangular carrier for different phase number VSIs.



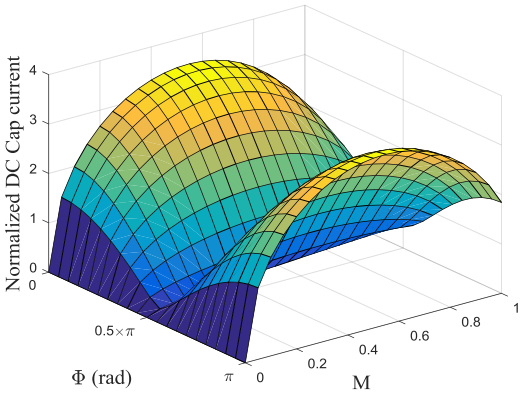
(a) 15-phase.



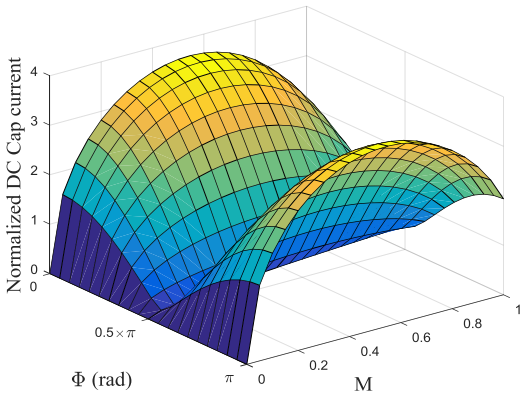
(b) 16-phase.



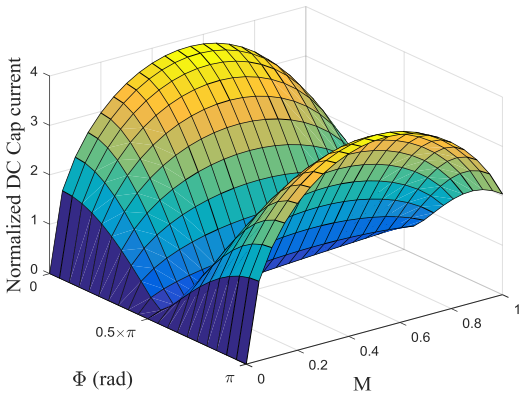
(c) 17-phase.



(d) 18-phase.



(e) 19-phase.



(f) 20-phase.

Figure 4.15 Normalized DC-link capacitor RMS current under SPWM and 10kHz triangular carrier for different phase number VSIs.

Table 4.1 DC-link capacitor RMS ratings comparison for different phase number VSIs.

Machine phase number	The maximum normalized DC-link RMS current	Phase current	Per unit DC-link RMS rating
3	0.65	1.00	1.00
4	0.81	0.75	0.94
5	0.99	0.60	0.91
6	1.17	0.50	0.90
7	1.36	0.43	0.90
8	1.55	0.38	0.89
9	1.74	0.33	0.89
10	1.93	0.30	0.89
11	2.12	0.27	0.89
12	2.31	0.25	0.89
13	2.50	0.23	0.89
14	2.69	0.21	0.89
15	2.88	0.20	0.88
16	3.07	0.19	0.88
17	3.26	0.18	0.88
18	3.45	0.17	0.88
19	3.64	0.16	0.88
20	3.83	0.15	0.88

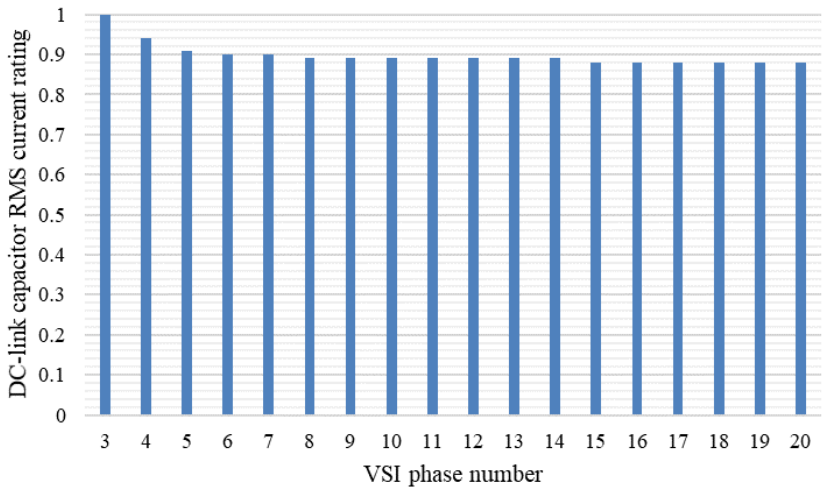
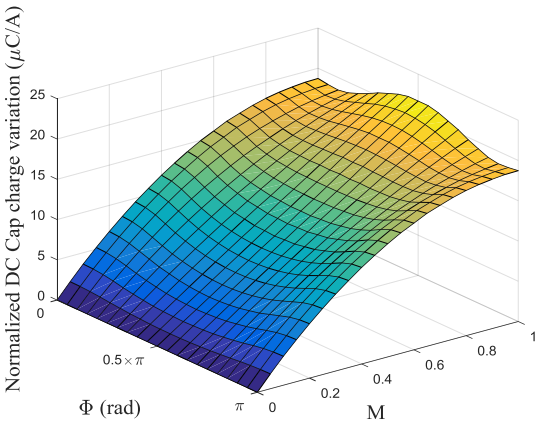
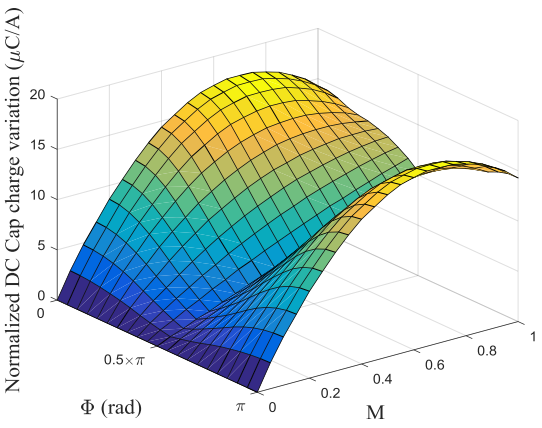


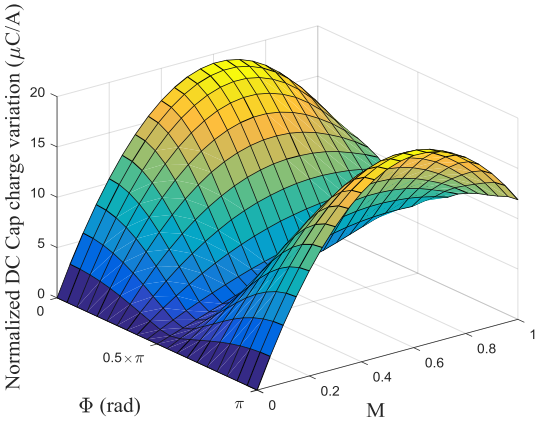
Figure 4.16 DC-link capacitor RMS ratings comparison for different phase number VSIs.



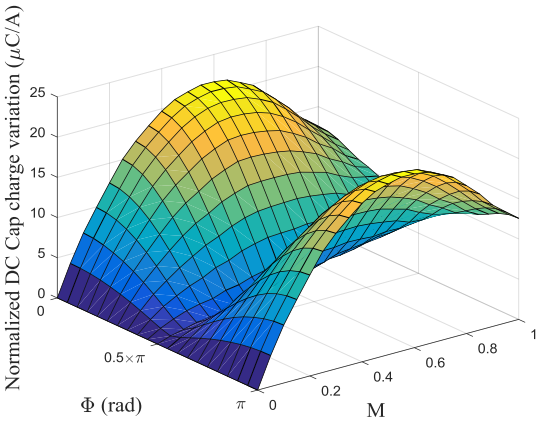
(a) 3-phase.



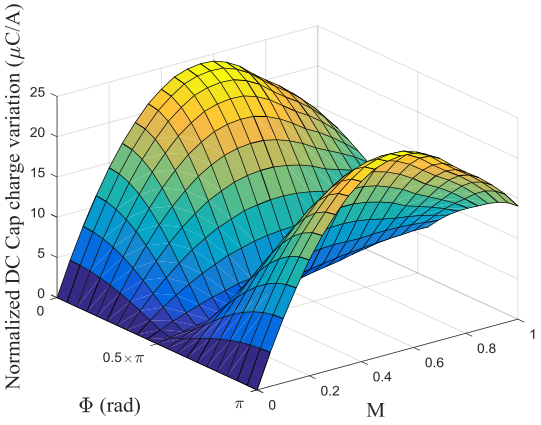
(b) 4-phase.



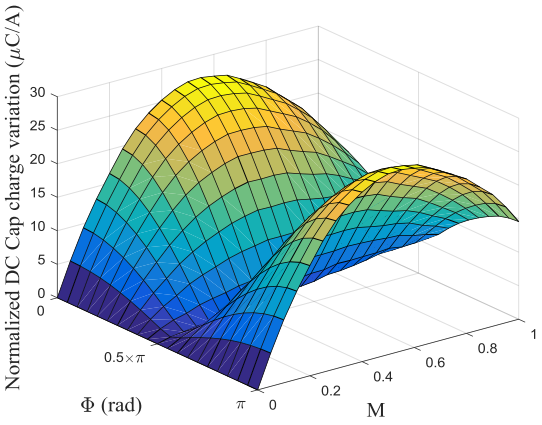
(c) 5-phase.



(d) 6-phase.

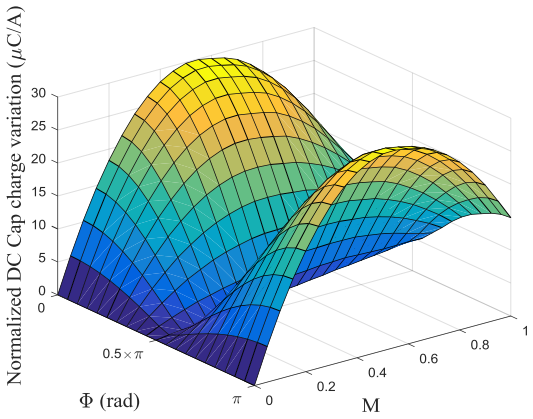


(e) 7-phase.

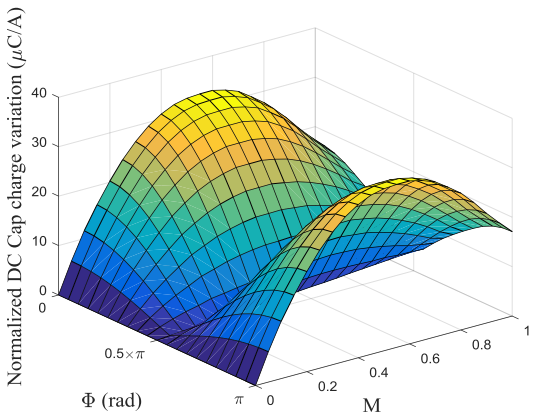


(f) 8-phase.

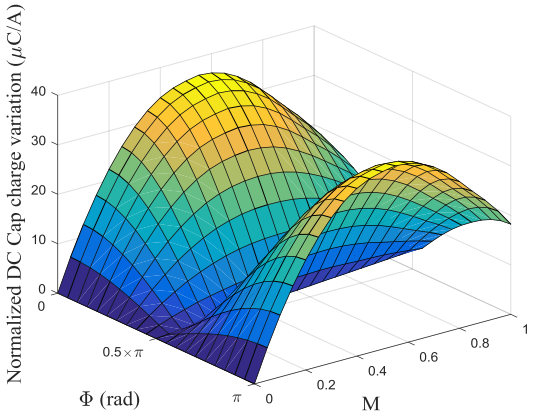
Figure 4.17 Normalized DC-link capacitor charge variation under SPWM and 10kHz triangular carrier for different phase number VSIs.



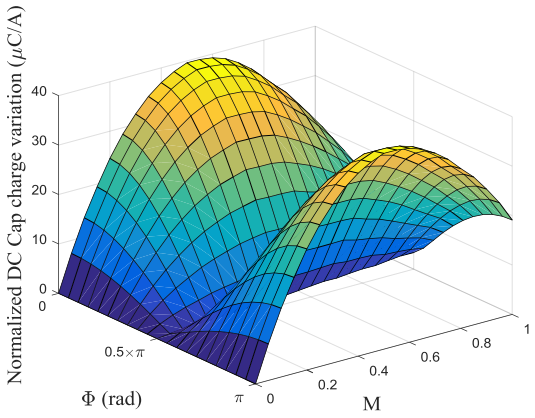
(a) 9-phase.



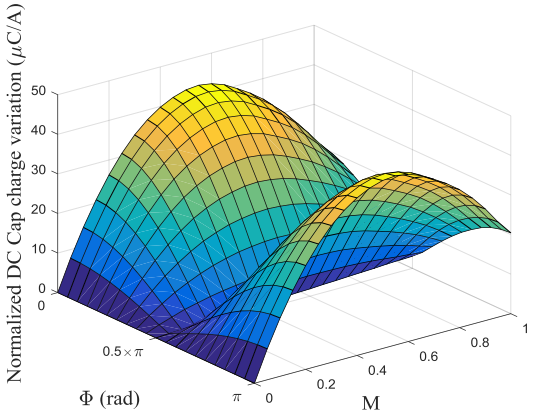
(b) 10-phase.



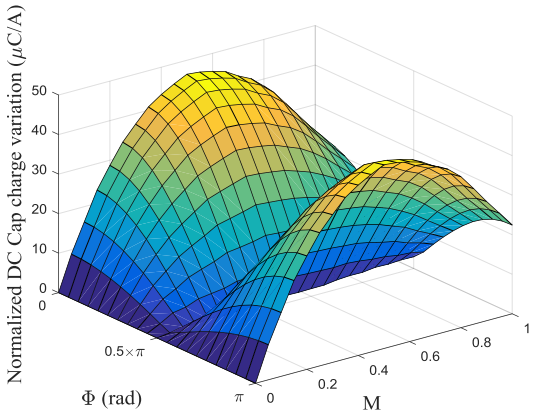
(c) 11-phase.



(d) 12-phase.

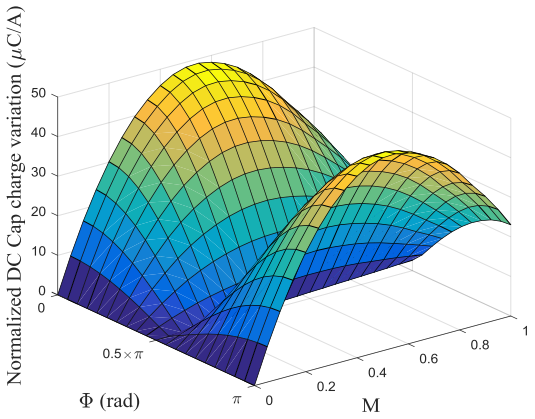


(e) 13-phase.

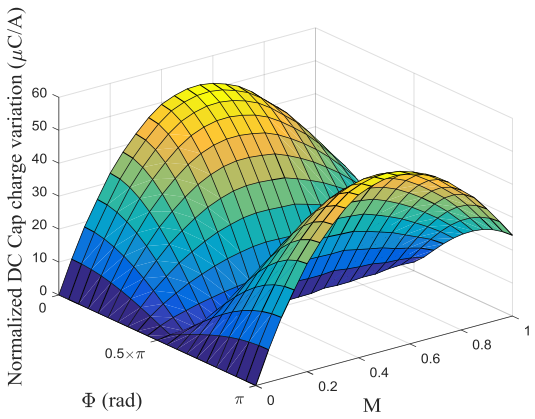


(f) 14-phase.

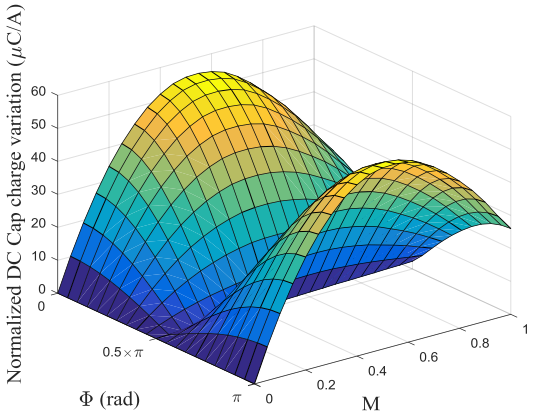
Figure 4.18 Normalized DC-link capacitor charge variation under SPWM and 10kHz triangular carrier for different phase number VSIs.



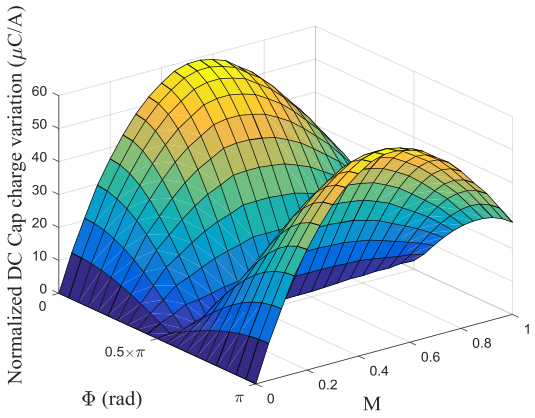
(a) 15-phase.



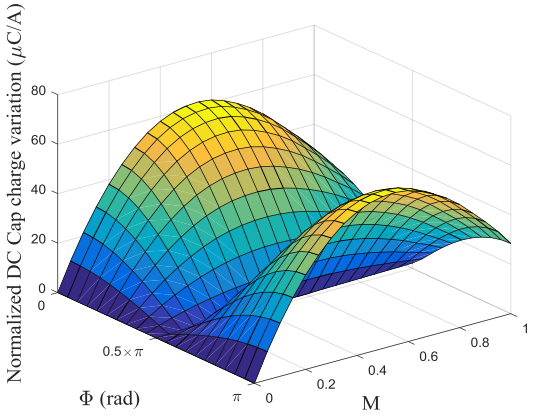
(b) 16-phase.



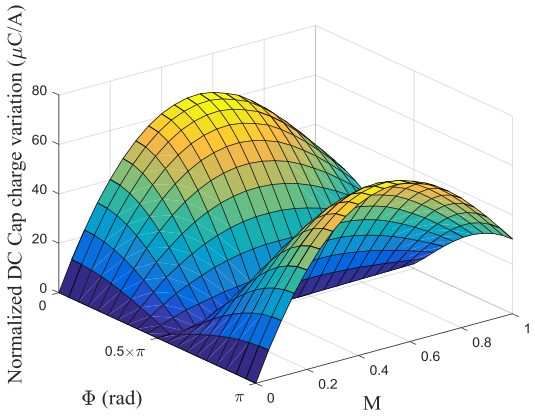
(c) 17-phase.



(d) 18-phase.



(e) 19-phase.



(f) 20-phase.

Figure 4.19 Normalized DC-link capacitor charge variation under SPWM and 10kHz triangular carrier for different phase number VSIs.

Table 4.2 Required DC-link capacitance comparison for different phase number VSIs.

Machine phase number	The maximum normalized DC-link charge variation (μC/A)	Phase current	Per unit DC-link capacitance
3	21.70	1.00	1.00
4	17.44	0.75	0.60
5	19.10	0.60	0.53
6	21.65	0.50	0.50
7	24.20	0.43	0.48
8	27.06	0.38	0.47
9	29.90	0.33	0.46
10	32.97	0.30	0.46
11	36.40	0.27	0.46
12	39.62	0.25	0.46
13	42.70	0.23	0.45
14	46.47	0.21	0.46
15	48.90	0.20	0.45
16	52.20	0.19	0.45
17	55.10	0.18	0.45
18	59.20	0.17	0.45
19	61.70	0.16	0.45
20	65.03	0.15	0.45

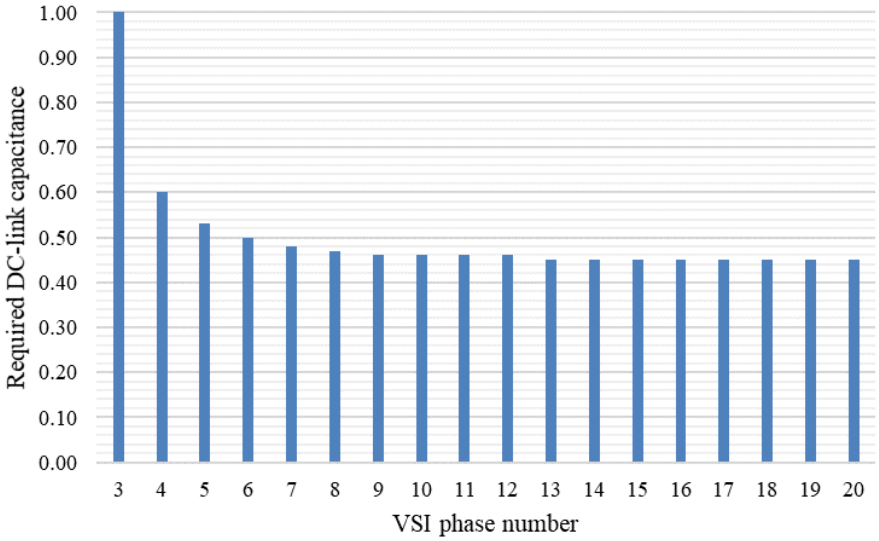


Figure 4.20 DC-link capacitance comparison for different phase number VSIs.

4.4 Switching Strategy, Carrier Waveform and Interleaving Technology Considerations

4.4.1 Investigation Method for 3- and 9-phase VSIs Study

The previous section highlighted a number of interesting results. However, given that it would not be feasible to validate all of the phase number options within the scope of this thesis, it was described to focus on the 3- and 9-phase options.

The DC-link capacitor RMS current ratings and required capacitance are investigated for SPWM and triangular waveform in the previous sections. While there are some other factors that can determine the DC-link capacitor requirements, for example, carrier waveform shapes, interleaving techniques, switching strategies (SPWM SVM or others) that are studied here.

In spite of the triangular waveform in Equation (4.11), a saw tooth waveform is another option for the carrier waveform:

$$\begin{aligned} &Saw(t) = \frac{1}{T}t \quad 0 \le t < T \\ &and \;\; Saw(t) = Saw(t + kT) \end{aligned} \tag{4.21}$$

Two different interleaving techniques are proposed here the symmetrical interleaving and group based interleaving techniques for both triangular and saw tooth carrier waveforms. For these interleaving techniques, every phase has its individual carrier waveform, where the carrier waveforms are in phase in the non-interleaved technique. Some phase shift among different phase carrier waveforms is also an option. For symmetrical interleaving, technology different phase carrier waveforms are distributed symmetrically, leading or lagging the same angle between consecutive phases. In group based interleaving, the phases within the same group have the in-phase carrier waveforms while the carrier waveforms in different groups are distributed symmetrically.

Thus for the symmetrical interleave technology:

$$\begin{aligned} &Saw_1(t) = \frac{1}{T}t \quad 0 \le t < T \ \ and \ \ Saw_1(t) = Saw_1(t + kT) \\ &Saw_{kp}(t) = Saw_1\left[t + (kp-1)\frac{T}{n}\right] \ or \ Saw_{kp}(t) = Saw_1\left[t - (kp-1)\frac{T}{n}\right] \end{aligned} \tag{4.22}$$

where *kp* is the phase index.

For the group based interleave technology:

$$\begin{aligned} &Saw_1(t) = \frac{1}{T}t \quad 0 \le t < T \ \ and \ \ Saw_1(t) = Saw_1(t + kT) \\ &Saw_{kg}(t) = Saw_1\left[t + gg \cdot (kg-1) \cdot \frac{T}{n}\right] \ or \ Saw_{kg}(t) = Saw_1\left[t - gg \cdot (kg-1) \cdot \frac{T}{n}\right] \end{aligned} \tag{4.23}$$

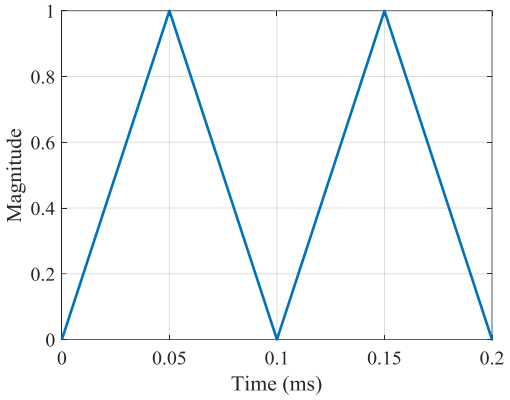
where *kg* is the group carrier waveform index and *gg* is the group number that the machine phases are divided into.

The triangular and saw tooth carrier waveforms, symmetrical interleaving and group based interleaving techniques are illustrated in Figure 4.21, taking the 9-phase and 3x 3-phase systems as examples.

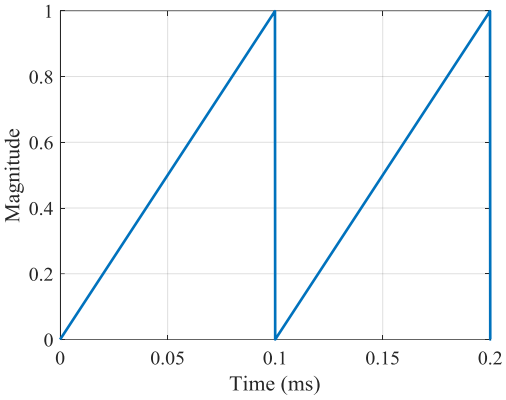
Successive to the SPWM scheme in Equation (4.12), the SVM phase duty ratio, $d_{ph\_SVM}(n,t)$, in an *n*-phase VSI is:

$$\left.\begin{aligned} d_{ph\_\max}(t) &= \max\left[d_{ph}(1,t) \quad d_{ph}(2,t) \quad \cdots \quad d_{ph}(n,t)\right] \\ d_{ph\_\min}(t) &= \min\left[d_{ph}(1,t) \quad d_{ph}(2,t) \quad \cdots \quad d_{ph}(n,t)\right] \\ d_{ph\_SVM}(1,t) &= d_{ph}(1,t) + 0.5\left[1 - d_{ph\_\max}(t) - d_{ph\_\min}(t)\right] \\ d_{ph\_SVM}(2,t) &= d_{ph}(2,t) + 0.5\left[1 - d_{ph\_\max}(t) - d_{ph\_\min}(t)\right] \\ d_{ph\_SVM}(3,t) &= d_{ph}(3,t) + 0.5\left[1 - d_{ph\_\max}(t) - d_{ph\_\min}(t)\right] \\ &\vdots \\ d_{ph\_SVM}(n,t) &= d_{ph}(n,t) + 0.5\left[1 - d_{ph\_\max}(t) - d_{ph\_\min}(t)\right] \end{aligned}\right\} \tag{4.24}$$

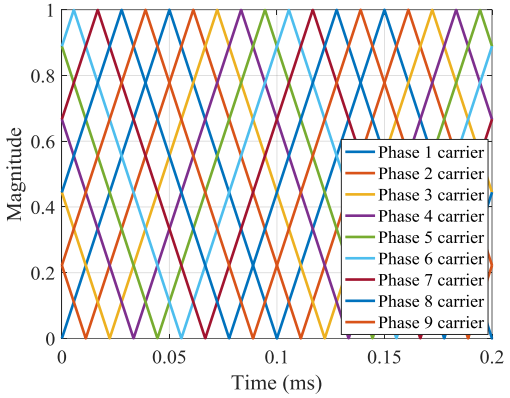
from which the group based SVM can also be derived. The 9-phase SVM control waveforms and the 3x 3-phase group based SVM control waveforms (discussed in Chapter 3) are illustrated in Figure 4.22.



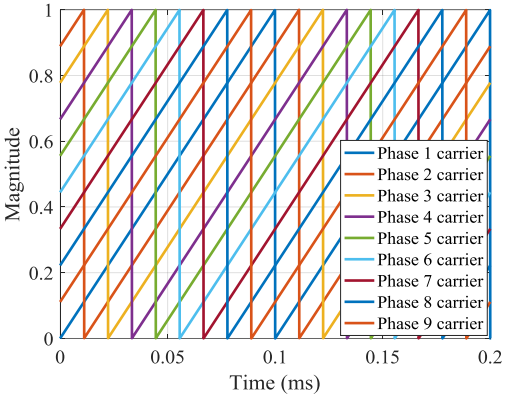
(a) Non-interleaved triangular carrier.



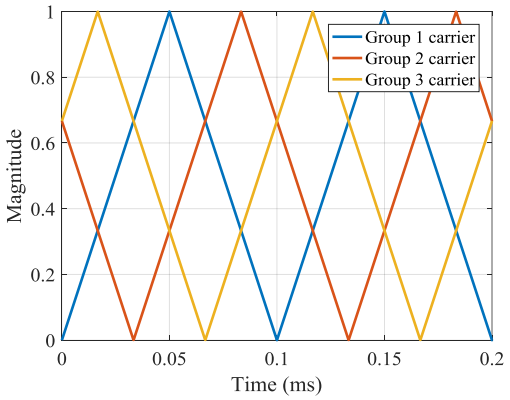
(d) Non-interleaved saw tooth carrier.



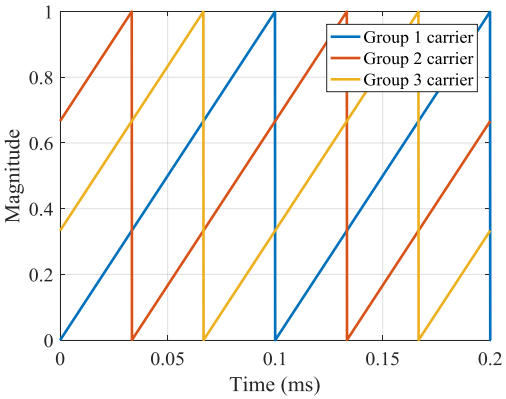
(b) Symmetrical interleaved triangular carrier.



(e) Symmetrical interleaved saw tooth carrier.

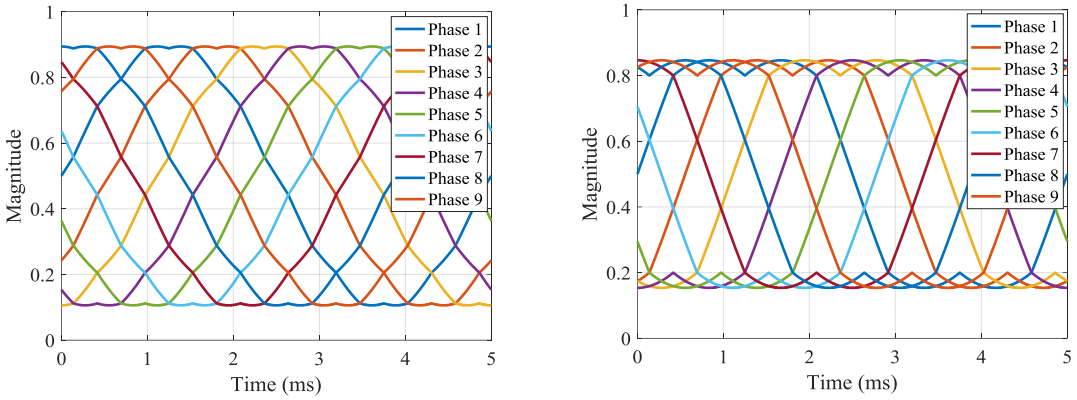


(c) Group based interleaved triangular carrier.



(f) Saw tooth carrier Group based interleaved saw tooth carrier.

Figure 4.21 Non-interleaved and interleaved carrier waveforms (10 kHz) for 9-phase or 3x 3-phase VSIs.

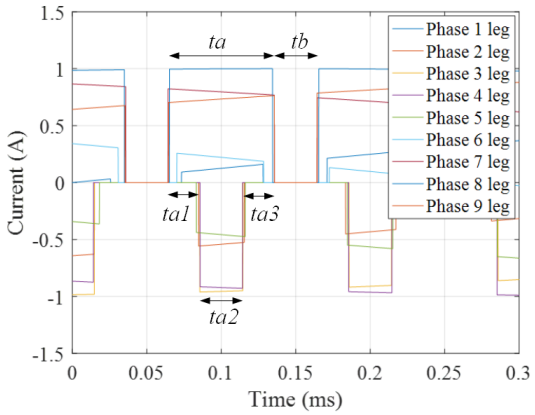


(a) 9-phase SVM control waveform. (b) 3x 3-phase SVM control waveform.

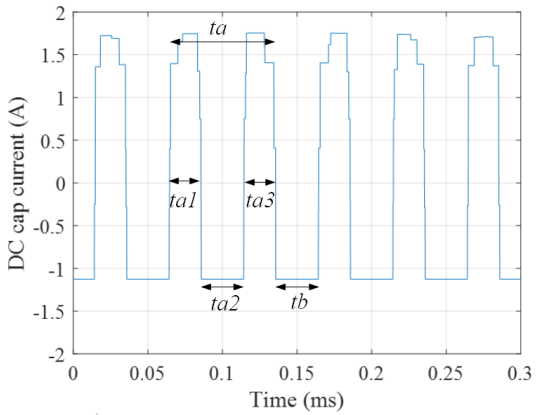
Figure 4.22 SVM and group based SVM control waveforms (0.8 modulation index) for 9-phase and 3x 3-phase systems.

The application of the interleaving techniques change the DC-link capacitor current ripple pulses as shown in Figure 4.23, which, for example, focuses on the 3x 3-phase VSIs. One switching cycle is divided into two time slots, *ta* and *tb*, *ta* is further divided into *ta1*, *ta2* and *ta3*. In the non-interleaved condition, as shown in Figure 4.23 (a), all the negative phase leg current pulses are in the middle of the positive ones cancelling with each other, the *ta2* and *tb* time slots result in the bottom DC-link capacitor current pulses, and the *ta1* and *ta3* time slots result in the peak ones. In the symmetrical interleaved condition shown in Figure 4.23 (b), the positive and negative phase leg current pulses cancellation is weakened that in *ta1* and *ta3* there are 4 positive pulses with higher magnitudes, only 2 negative pulses with lower magnitudes and in *ta2* all 5 pulses are positive. Within the *tb* slot, the negative pulses have higher magnitude than the positive ones. This enlarges the DC capacitor current pulse peak-to-peak magnitude and the pulse lengths as shown in Figure 4.23 (d) when compared with that shown in Figure 4.23 (b).

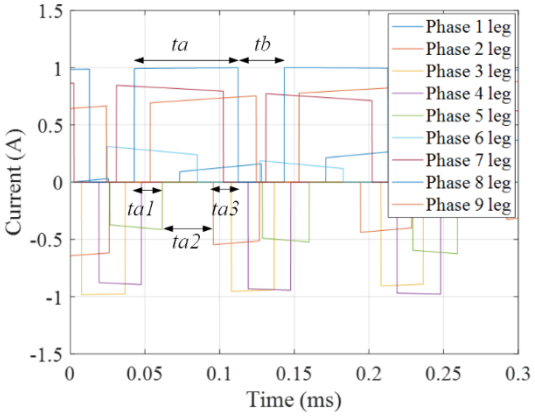
In the group based interleaved condition, the phase leg current pulses in Figure 4.23 (e) do not accumulate together as in the non-interleaved case, nor distribute as in the symmetrical interleaved. Some negative pulses in *ta1* and *ta3* cancel with the positive ones, and both positive and negative pulses occur in *tb*, but have cancellation effects. This decreases both the DC current pulse peak-to-peak magnitude and time duration, as shown in Figure 4.23 (f).



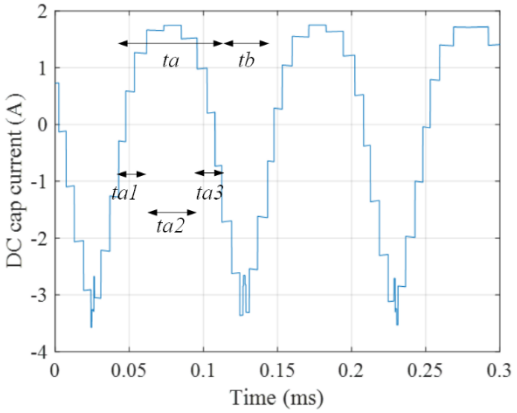
(a) Phase leg currents 3x 3-phase SVM non-interleaving.



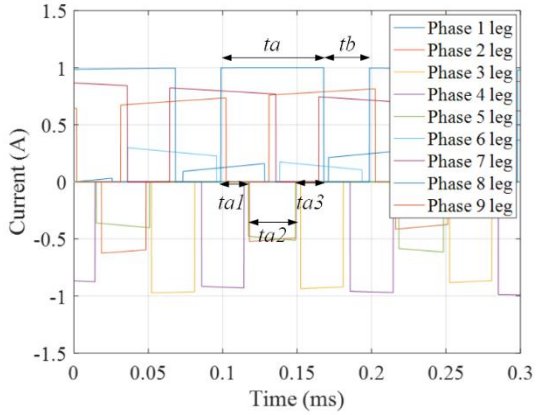
(b) DC Cap current 3x 3-phase SVM non-interleaving.



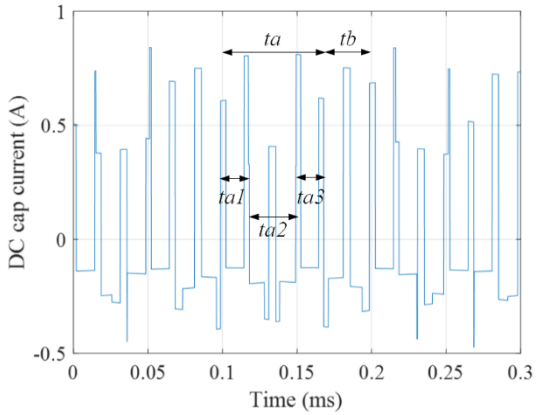
(c) Phase leg currents 3x 3-phase SVM symmetrical interleaving.



(d) DC Cap current 3x 3-phase SVM symmetrical interleaving.



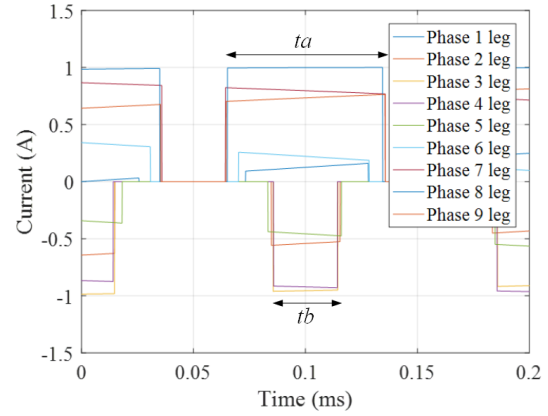
(e) Phase leg currents 3x 3-phase SVM group based interleaving.



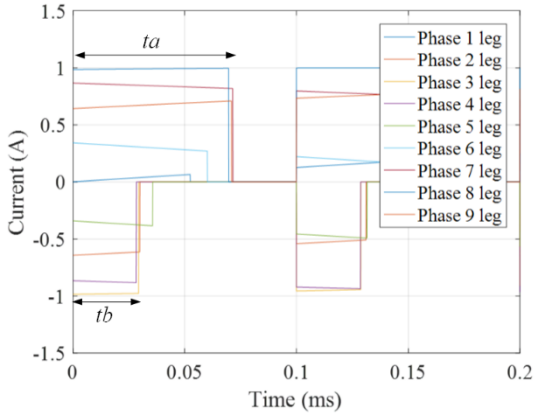
(f) DC Cap current 3x 3-phase SVM group based interleaving.

Figure 4.23 Comparison between interleaved and non-interleaved triangular carrier at unity power factor and 0.5 modulation index.

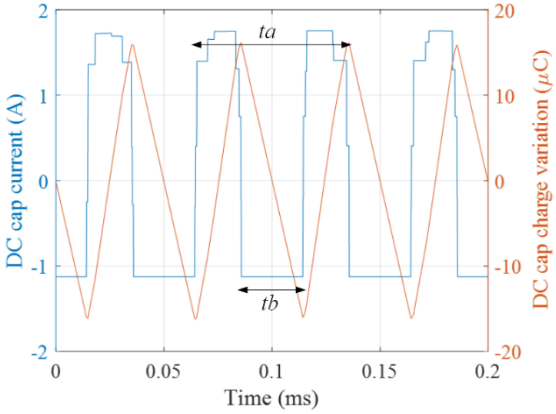
The phase leg current shape and superposition are shown in Figure 4.24 for VSIs with non-interleaved triangular and saw tooth carrier waveforms. The negative phase leg current pulses (over *tb* time slot) accumulate in the middle of the positive pulses (over *ta* time slot) in the triangular carrier, as shown in Figure 4.24 (a), while they accumulate in the side of the positive pulses in the saw tooth, waveforms as shown in Figure 4.24 (b). This results in the same DC-link capacitor current pulses magnitudes, while of different pulse widths, as shown in Figure 4.24 (c) and Figure 4.24 (d), leading to the doubled DC-link capacitor stored charge variation, but with the same DC-link capacitor RMS current.



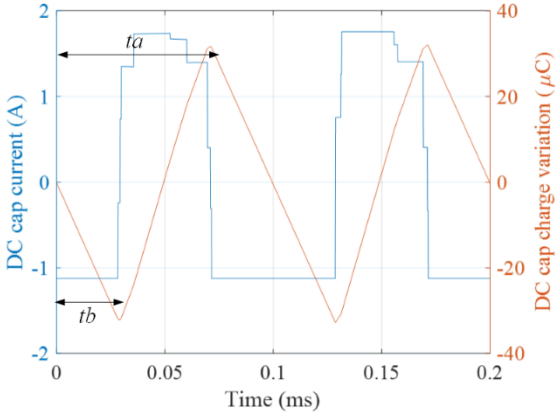
(a) 3x 3-phase SVM non-interleaved triangular phase leg current.



(b) 3x 3-phase SVM non-interleaved saw tooth phase leg current.



(c) 3x 3-phase SVM non-interleaved triangular DC-link cap current.



(d) 3x 3-phase SVM non-interleaved saw tooth DC-link cap current.

Figure 4.24 Comparison between triangular and saw tooth carrier waveforms (10 kHz switching frequency, power factor 1 and modulation index 0.6)

In terms of the normalized DC-link capacitor RMS current, neither the saw tooth carrier waveform nor the SVM switching strategy results in any sound difference compared with the SPWM and triangular carrier waveform. The results are shown in Figure 4.25 (a) Figure 4.25 (b) and Figure 4.25 (c) for 3-phase VSIs, Figure 4.26 (a) and Figure 4.26 (b) for 9-phase, Figure 4.27 (b) and Figure 4.27 (c) for 3x 3-phase non-interleaved carrier waveform, and Figure 4.27 (e) and Figure 4.27 (f) for 3x 3-phase interleaved carrier waveform.

The symmetrical interleaving technology increases the normalized DC-link capacitor RMS current for all 3-phase, 9-phase and 3x 3-phase systems as shown in Figure 4.25 (d), and Figure 4.26 (c) and Figure 4.27 (d). While the group based interleaved technology significantly decreases the normalized DC-link capacitor RMS current over the high power factor operating region, as shown in Figure 4.26 (d), Figure 4.27 (e) and Figure 4.27 (f).

By comparing among Figure 4.25, Figure 4.26, and Figure 4.27, the best strategy with the lowest DC-link capacitor RMS current (in the most common machine operating range, i.e. above 0.7 power factor) is the 3x 3-phase SVM with group based interleaved triangular carrier waveform, as shown in Figure 4.27 (f). The reason for not choosing saw tooth carrier waveform is the increase in required DC-link capacitance. The reason for choosing only power factors above 0.7 regardless of the peaks at zero power factor in Figure 4.27 (f), is that the transient operating points in the vicinity of zero power factor are very rare to occur and negligible. Hence, they would not bring considerable thermal problems due to the transient increase in RMS current. Moreover, although the steady state DC-link capacitor RMS current is investigated here, that can also represent the RMS current limit under transient states due to the saturation in the phase current controller. In other words, at any moment the DC-link capacitor current is less than the steady state DC-link capacitor RMS current rating (corresponding the rated phase current and the peak point on the normalized DC-link capacitor RMS current surface above 0.7 power factor).

No sound difference is found between the 3-phase VSIs with SPWM and SVM, which the 3-phase VSI with SPWM non-interleaving represents the minimum DC-link capacitor RMS rating 3-phase VSI. Even though the SVM group-based interleaved technique is applied in the 3x 3-phase (one 9-phase system) VSI, no interleaving occurs within each 3-

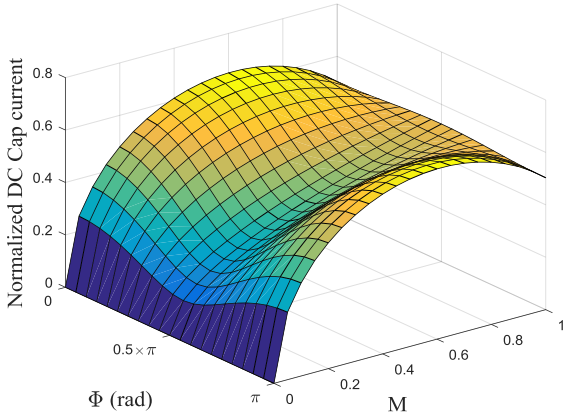
phase sub systems and it requires the minimum DC-link capacitor RMS current ratings among the 9-phase VSIs of different switching strategies and interleaving techniques. This results in the equivalent comparison condition. The DC-link capacitor RMS current comparison between 3- and 9-phase systems is given in Table 4.3 and illustrated in Figure 4.28 where the 3x 3-phase system with SVM group based interleaved triangular carrier waveform requires only 1/3 DC-link capacitor RMS current rating than its 3-phase counterpart.

Regarding the normalized DC-link capacitor stored charge variation in the 3-phase VSI, by applying SVM the high power factor region, the normalized DC-link capacitor charge variation is much lower than that under SPWM, while the peak value and its location do not change drastically, as shown in Figure 4.29 (a) and Figure 4.29 (c). For 9- and 3x 3-phase VSIs, the SVM introduces slight differences to the normalized DC-link capacitor stored charge variation and increases the peak values, as shown in Figure 4.30 (a), Figure 4.30 (b) and Figure 4.30 (c). The application of saw tooth carrier waveform, as opposed to triangular carrier wave, increases the normalized DC-link capacitor charge variation, as shown in Figure 4.29 (a) and Figure 4.29 (b) and Figure 4.30 (e) and Figure 4.30 (f). The symmetrical interleaving introduces the significant increase to the normalized DC-link capacitor stored charge variation, as shown in Figure 4.29 (d) and Figure 4.30 (d). The group based interleaving technique decreases the normalized DC-link capacitor stored charge variation significantly within the normal machine drive high power factor operating range, and reduces the peak value slightly as can be seen by comparing Figure 4.30 (c) and Figure 4.30 (e).

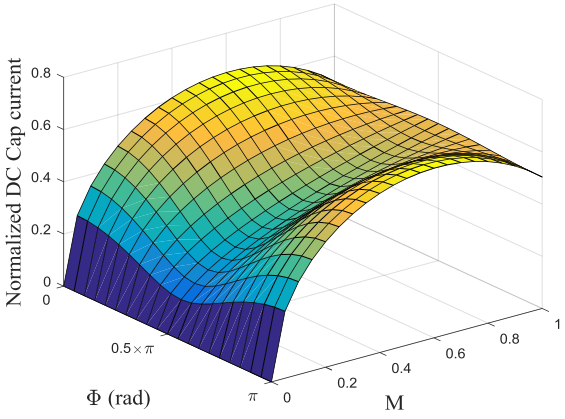
The required DC-link capacitance comparison among 3- and 9-phase VSIs is given in Table 4.4 and illustrated in Figure 4.31, where the results do not change significantly with those presented in Table 4.2 and Figure 4.20.

Consequently, after the comprehensive study on switching strategies, carrier waveforms and interleaving techniques, the 3x 3-phase SVM group base interleaved triangle waveform strategy is proposed as the best strategy in terms of the lowest DC-link capacitor RMS current and the second lowest DC-link capacitance requirement to that of the 9-phase SVM

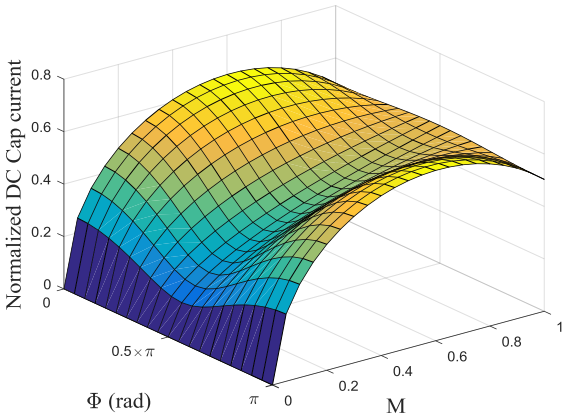
group based interleaved triangle waveform strategy. Additionally, although the 9-phase SVM group based interleaved triangle waveform strategy has slightly higher DC-link capacitor RMS current than the 3x 3-phase strategy, it has lower DC-link voltage utilization as discussed in Chapter 3, and its phase to star voltage peak occurs among the whole operating range (refer to the discussion in the experimental validation part in Chapter 5). When group based interleaving is applied in the 3x 3-phase system, each set of 3-phase systems are electrically isolated with each other. Naturally, there is no carrier waveform interleaving in each isolated 3-phase system.



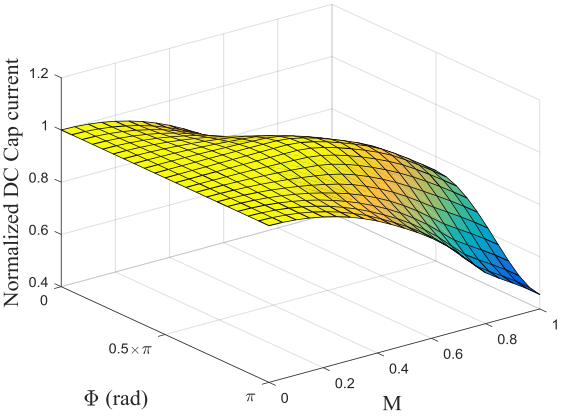
(a) SPWM non-interleaved triangular 10 kHz.



(b) SPWM non-interleaved saw tooth 10 kHz.

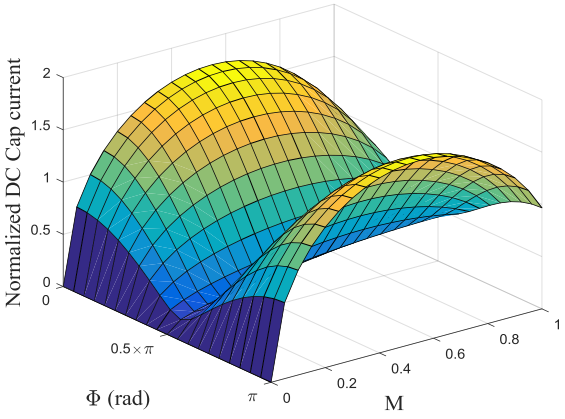


(c) SVM non-interleaved triangular 10 kHz.

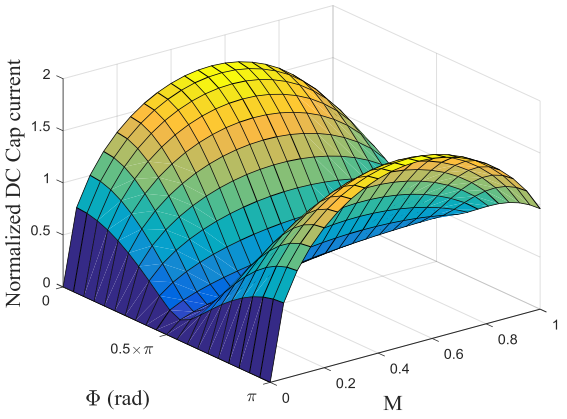


(d) SVM symmetrical interleaved triangular 10 kHz.

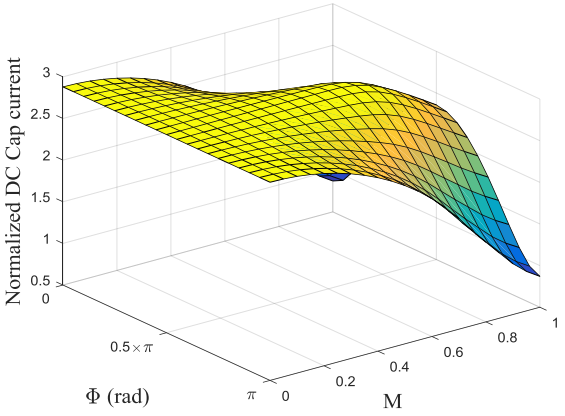
Figure 4.25 DC-link capacitor normalized RMS current comparison under different strategies for 3-phase VSIs.



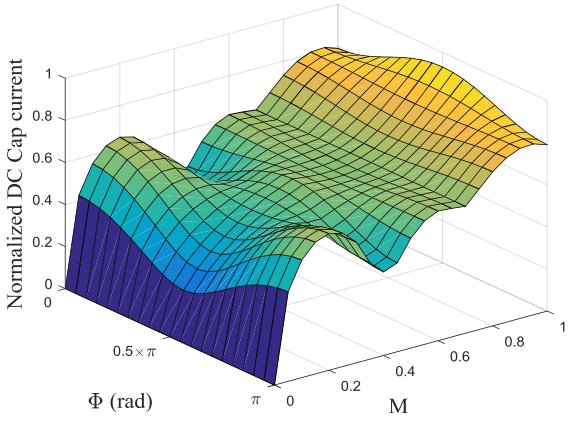
(a) SPWM non-interleaved triangular 10 kHz.



(b) SVM non-interleaved triangular 10 kHz.

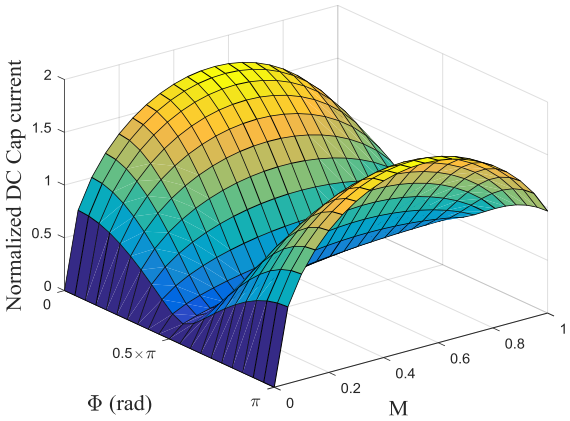


(c) SVM symmetrical interleaved triangular 10 kHz.

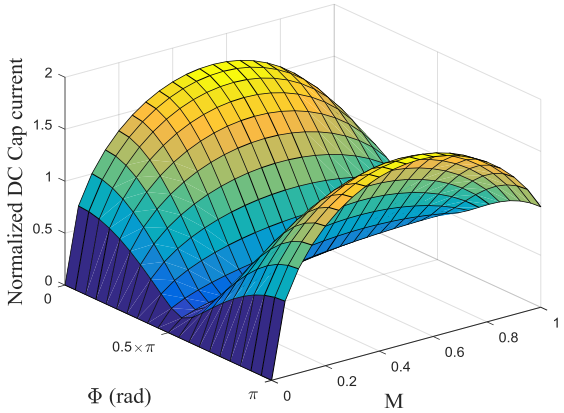


(d) SVM group based interleaved triangular 10 kHz.

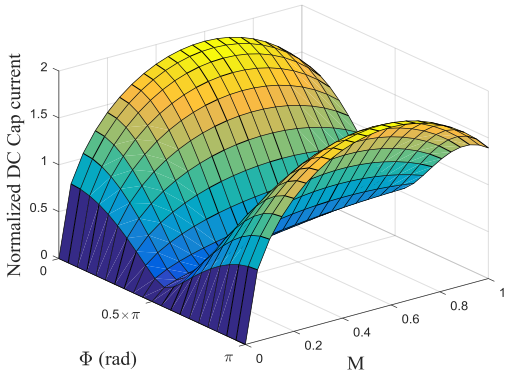
Figure 4.26 DC-link capacitor normalized RMS current comparison under different strategies for 9-phase VSIs.



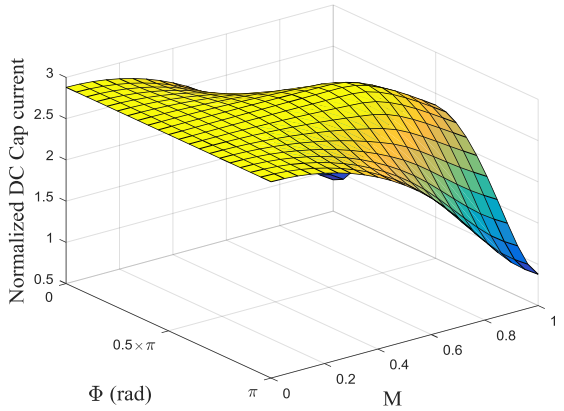
(a) SPWM non-interleaved triangular 5 kHz.



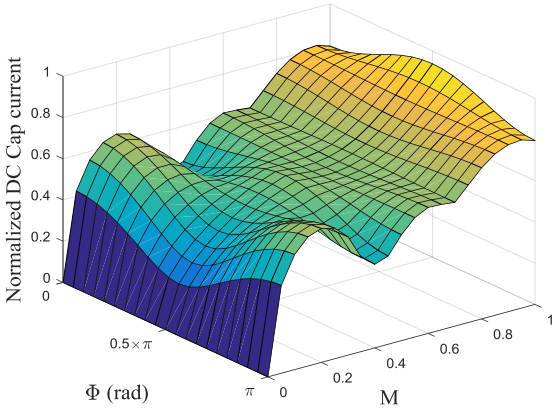
(b) SPWM non-interleaved triangular 10 kHz.



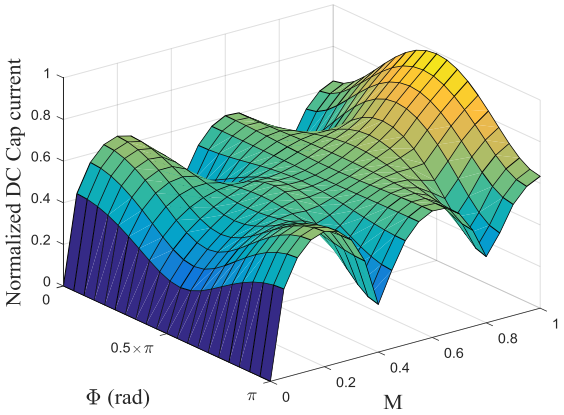
(c) SVM non-interleaved triangular 10 kHz.



(d) SPWM symmetrical interleaved triangular 10 kHz.



(e) SPWM group based interleaved triangular 10 kHz.



(f) SVM group based interleaved triangular 10 kHz.

Figure 4.27 DC-link capacitor normalized RMS current comparison under different strategies for 3x 3-phase VSIs.

Table 4.3 DC-link capacitor RMS rating comparison between 3- and 9-phase VSIs.

Machine phase number	The maximum normalized DC-link RMS current	Phase current	DC-link Cap RMS rating	Note
3	0.65	1.00	1.00	SPWM non-interleaved
9	0.65	0.33	0.33	3x 3-phase SVM group based interleaved

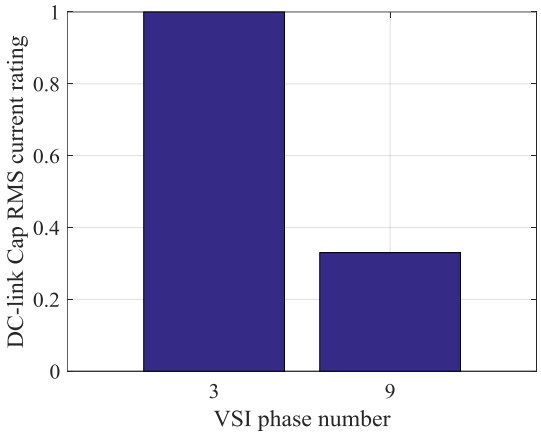
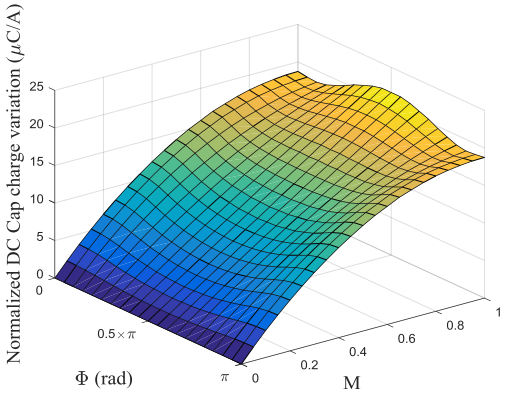
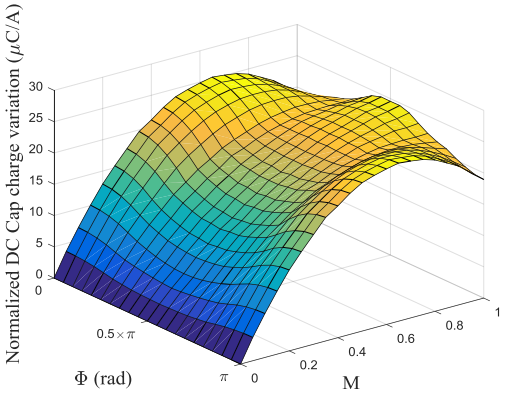


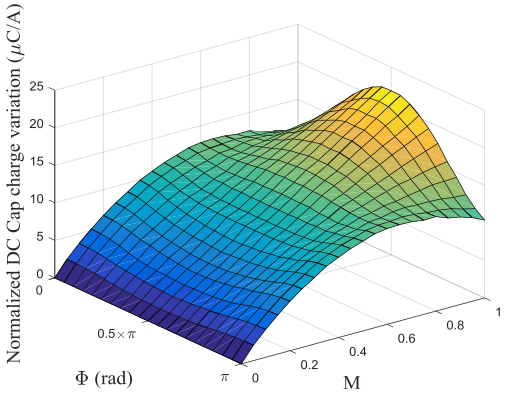
Figure 4.28 DC-link capacitor RMS ratings comparison between 3- and 9-phase VSIs.



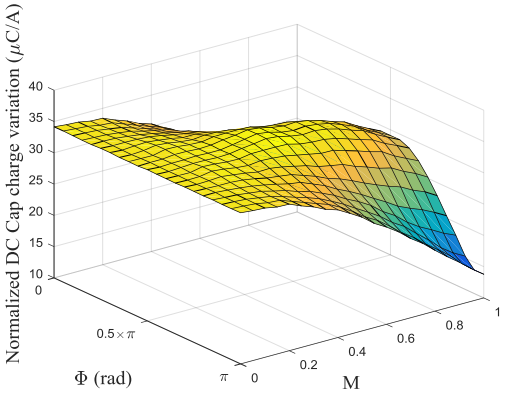
(a) SPWM non-interleaved triangular 10 kHz.



(b) SPWM non-interleaved saw tooth 10 kHz.

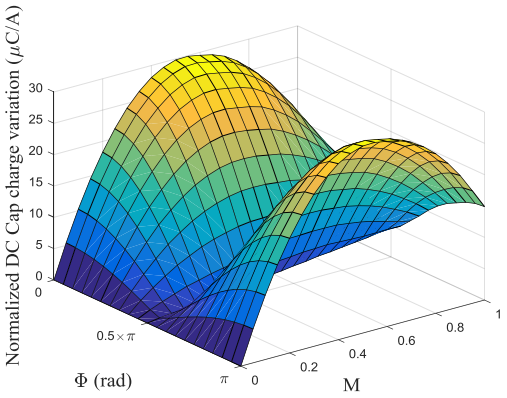


(c) SVM non-interleaved triangular 10 kHz.

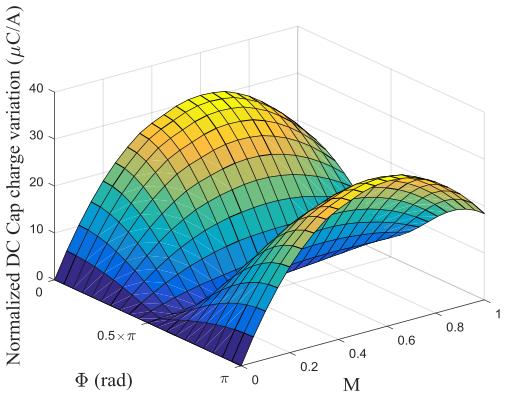


(d) SVM symmetrical interleaved triangular 10 kHz.

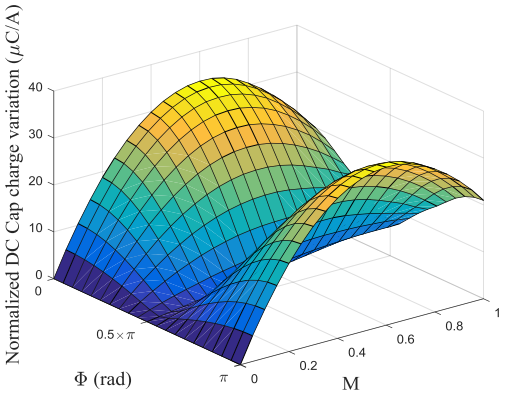
Figure 4.29 DC-link capacitor normalized stored charge variation comparison under different strategies for 3-phase VSIs.



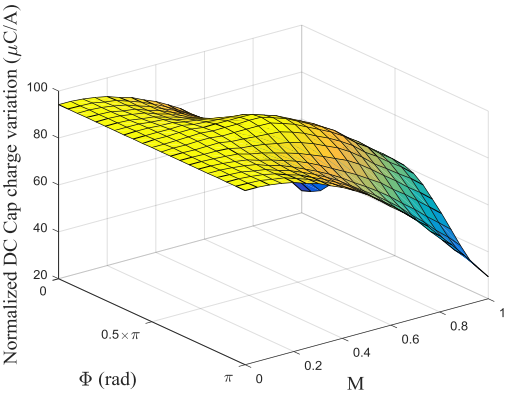
(a) 9-phase or 3x 3-phase SPWM non-interleaved triangular 10 kHz.



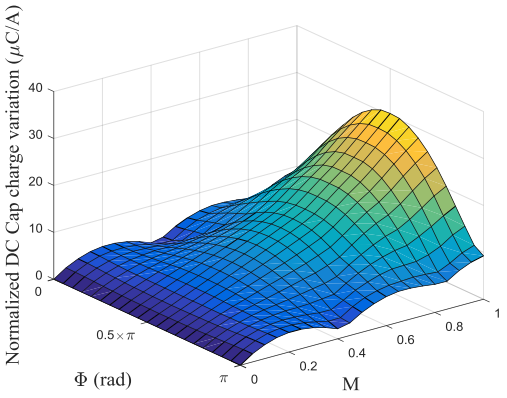
(b) 9-phase SVM non-interleaved triangular 10 kHz.



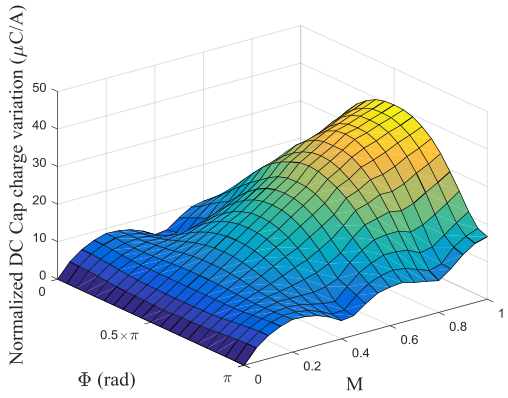
(c) 3x 3-phase SVM non-interleaved triangular 10 kHz.



(d) 3x 3-phase SVM symmetrical interleaved triangular 10 kHz.



(e) 3x 3-phase SVM group based interleaved triangular 10 kHz.



(f) 3x 3-phase SVM group based interleaved saw tooth 10 kHz.

Figure 4.30 DC-link capacitor normalized stored charge variation comparison under different strategies for 9-phase and 3x 3-phase VSIs.

Table 4.4 Required DC-link capacitance comparison among 3-phase and 9-phase VSIs.

Machine phase number	The maximum normalized DC-link charge variation (μC/A)	Phase current	Required DC-link capacitance	Note
3	21.70	1.00	1.00	SPWM non-interleaving
9	29.90	0.33	0.45	SPWM non-interleaving
9	30.43	0.33	0.46	3X 3-phase SVM group based interleaving

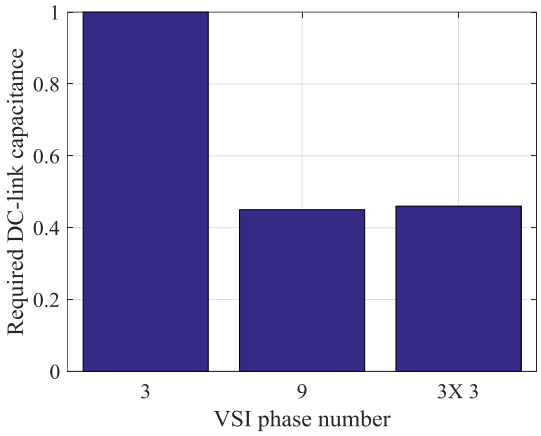


Figure 4.31 Required DC-link capacitance comparison among 3- and 9-phase VSIs.

4.4.2 Study on Other Phase Number VSIs

Based on the investigation method and results in the previous section, different phase number VSIs with SVM group based interleaved triangular carrier are studied against benchmark 3-phase and 5-phase VSIs. The group based systems with multiple 3- and 5-phases are investigated here due to their higher DC-link voltage utilization (studied in Chapter 3), simpler control and higher feasibilities compared with the group based systems with higher phase numbers, i.e. 7-phase, 9-phase etc. The considered phase numbers are the:

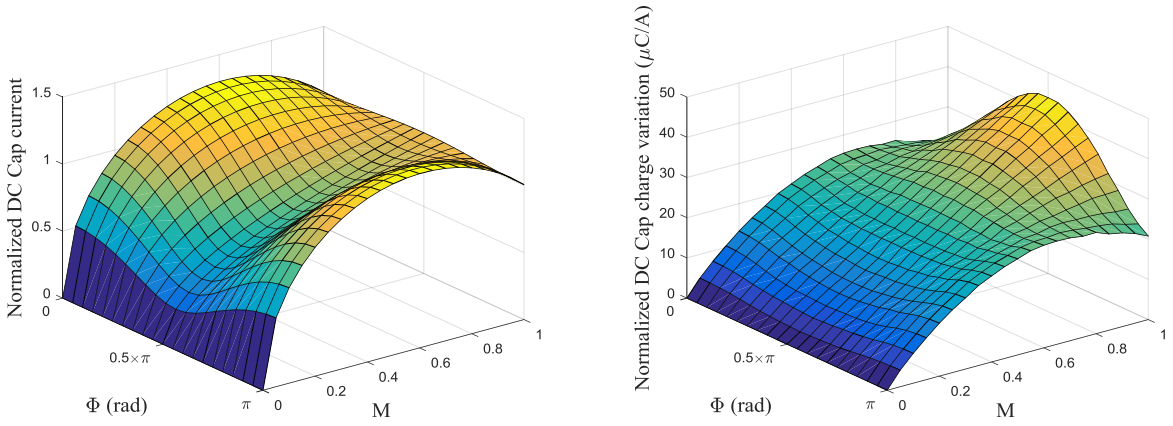
- 2x 3-phase (one special 6-phase system),
- 4x 3-phase (12-phase),
- 2x 5-phase (10-phase),
- 5x 3-phase (15-phase),
- 3x 5-phase (15-phase),
- 6x 3-phase (18-phase),
- 4x 5-phase (20-phase), and
- 9x 3-phase (27-phase).

Due to the number of results the normalized DC-link capacitor RMS current and normalized DC-link capacitor charge variation results are split over Figure 4.32, Figure 4.33 and Figure 4.34. The DC-link capacitor requirements for different phase number systems are summarized in Figure 4.35, Figure 4.36, Table 4.5 and Table 4.6.

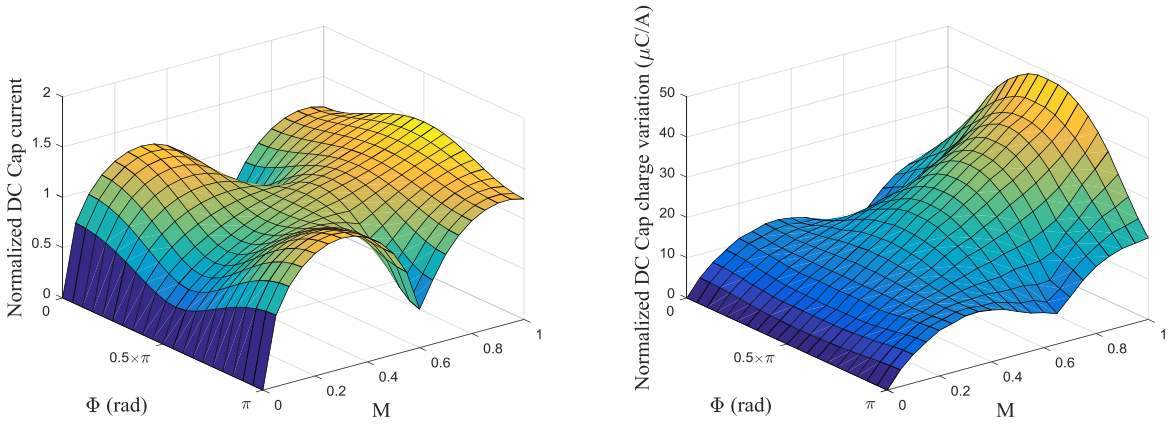
In terms of the DC-link capacitor RMS current compared with a benchmarking 3-phase VSI, the odd number multiplier 3-phase systems containing 3x 3-, 5x 3- and 9x 3-phase systems have a decreasing trend. Although there is also a reducing trend in the even number multiplier 3-phase VSIs among 2x 3-, 4x 3- and 6x 3-phase VSIs. The 2x 3-phase VSI has the same rating with the 3-phase one.

For the 5-phase and the multiplier 5-phase VSIs, 3x 5-phase VSI requires lower rating than the 5-phase, while the 2x 5-phase has the same rating followed by a decrease for the 4x 5-phase VSI. Thus having the same trend as that of the 3-phase and multiplier 3-phase VSIs. As to the required DC-link capacitance, these results have the same trend with those of the DC-link RMS current rating.

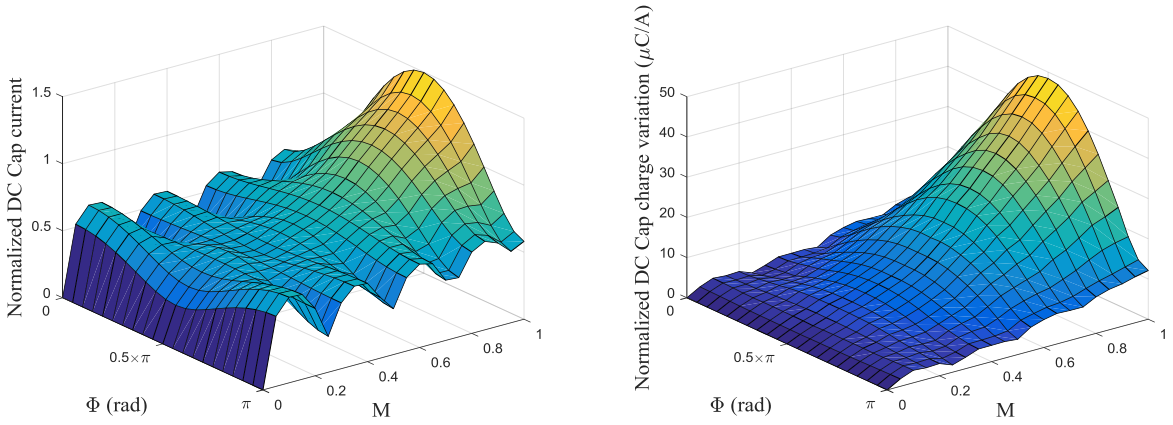
It should be noted here that the group based systems studied in this thesis are all symmetrical and that electrical vectors of different phases are distributed symmetrically.



(a) 2x 3-phase.

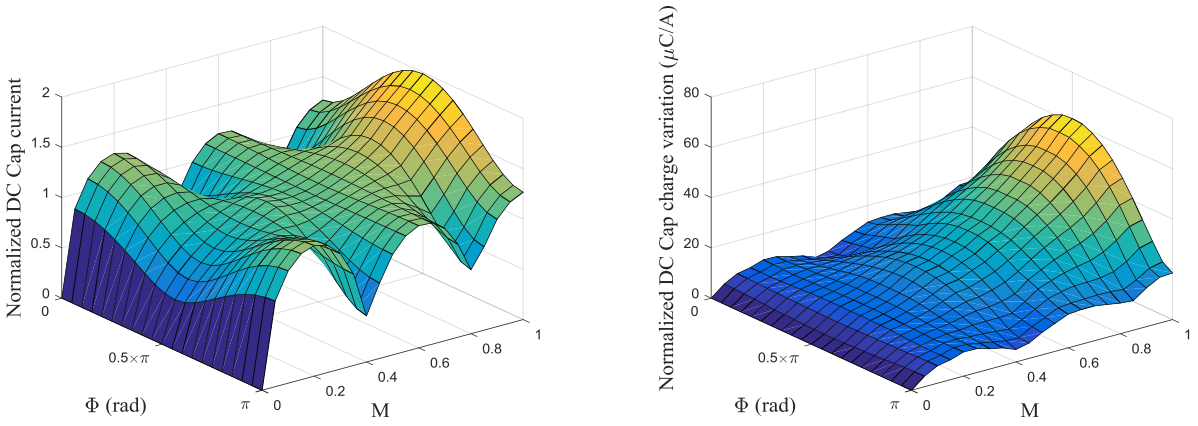


(b) 4x 3-phase.

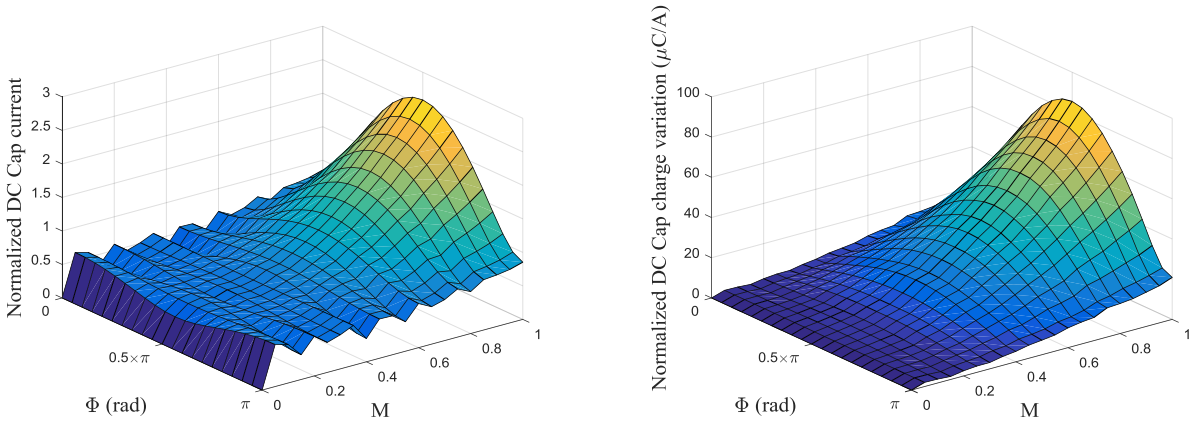


(c) 5x 3-phase.

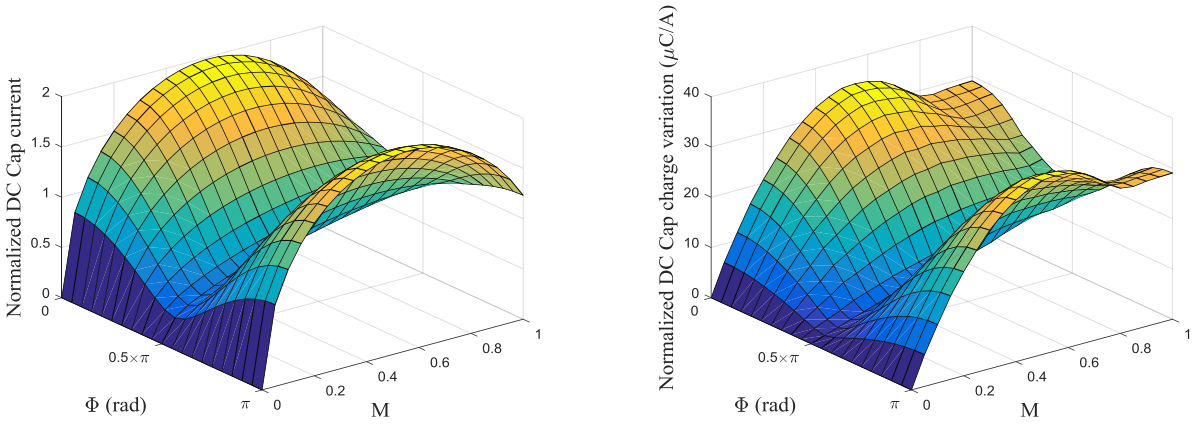
Figure 4.32 Normalized DC-link RMS current and charge variation for different phase number VSIs under SVM group based interleaved triangular carrier.



(a) 6x 3-phase.

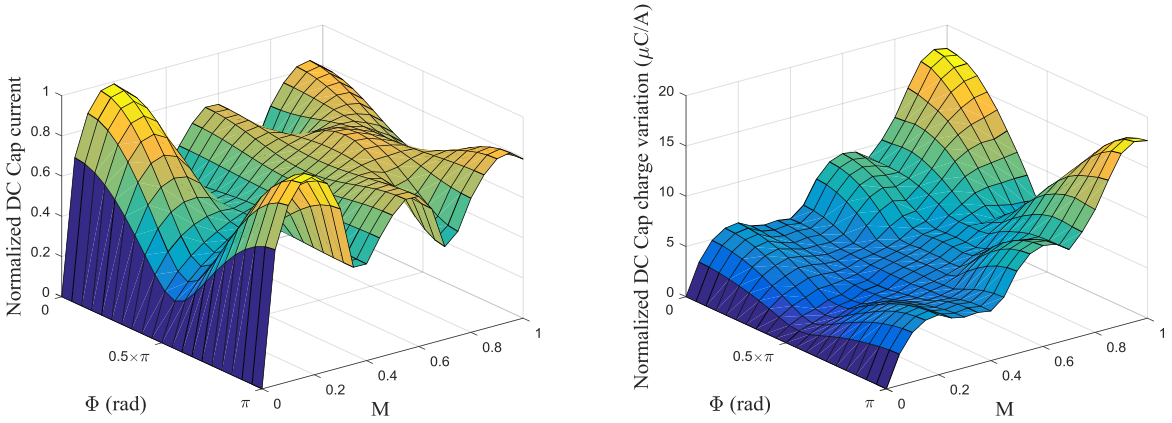


(b) 9x 3-phase.

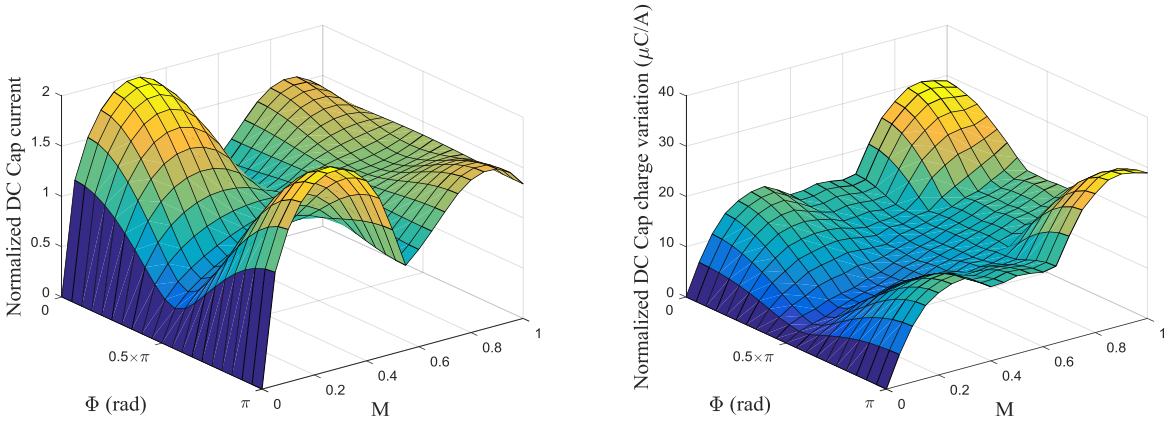


(c) 2x 5-phase.

Figure 4.33 Normalized DC-link RMS current and charge variation for different phase number VSIs under SVM group based interleaved triangular carrier.



(a) 3x 5-phase.



(b) 4x 5-phase.

Figure 4.34 Normalized DC-link RMS current and charge variation for different phase number VSIs under SVM group based interleaved triangular carrier.

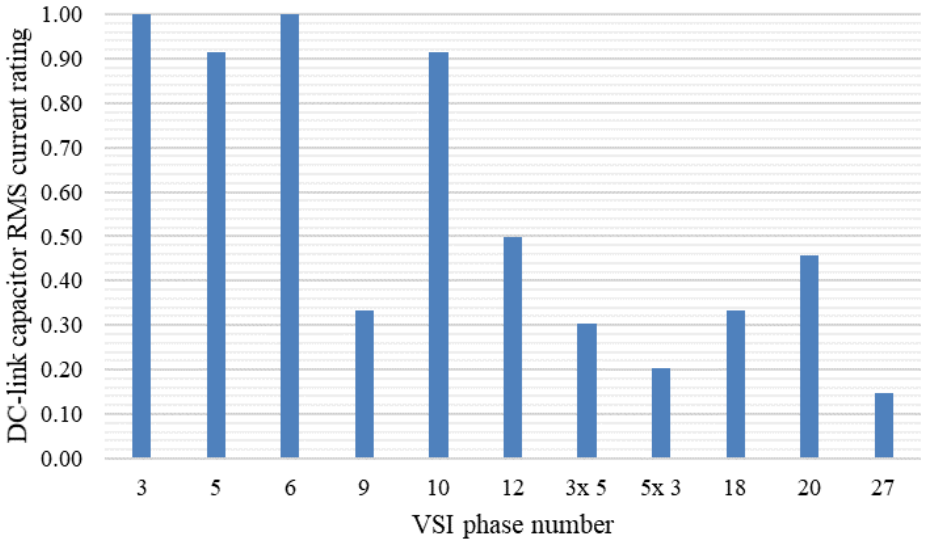


Figure 4.35 DC-link capacitor RMS ratings comparison among different phase number VSIs under SVM group based interleaved triangular carrier.

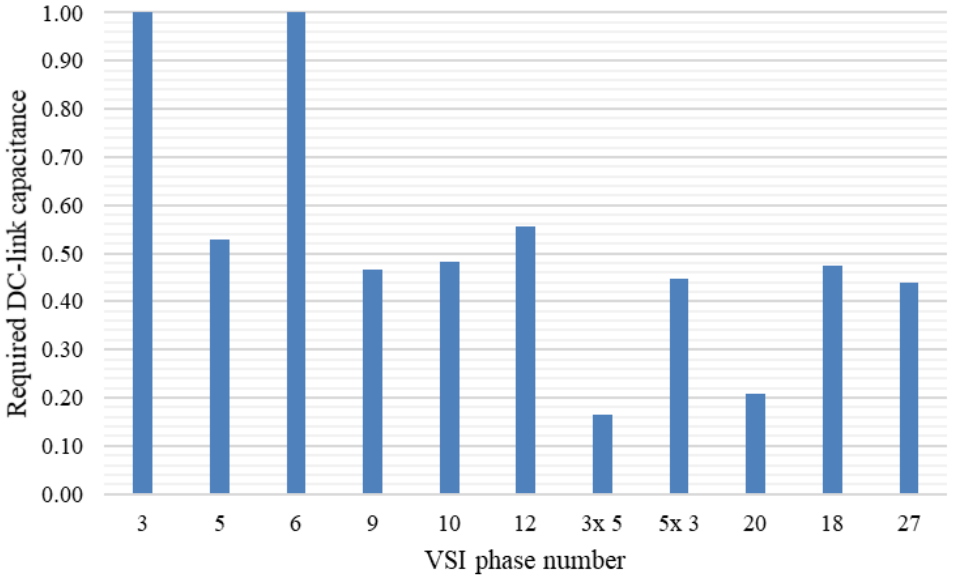


Figure 4.36 Required DC-link capacitance comparison among different phase number VSIs under SVM group based interleaved triangular carrier.

Table 4.5 DC-link capacitor RMS ratings comparison among different phase number VSIs under SVM group based interleaved triangular carrier.

Machine phase number	The maximum normalized DC-link RMS current	Phase current	Per unit DC-link RMS rating	Note
3	0.65	1.00	1.00	
5	0.99	0.60	0.91	
6	1.30	0.50	1.00	2x 3
9	0.65	0.33	0.33	3x 3
10	1.98	0.30	0.91	2x 5
12	1.30	0.25	0.50	4x 3
15	0.99	0.20	0.30	3x 5
15	0.66	0.20	0.20	5x 3
18	1.30	0.17	0.33	4x 5
20	1.98	0.15	0.46	6x 3
27	0.85	0.11	0.15	9x 3

Table 4.6 Required DC-link capacitance comparison among different phase number VSIs under SVM group based interleaved triangular carrier.

Machine phase number	The maximum normalized DC-link charge variation (μC/A)	Phase current	Per unit DC-link capacitance	Note
3	21.70	1.00	1.00	
5	19.10	0.60	0.53	
6	43.74	0.50	1.01	2x 3
9	30.43	0.33	0.47	3x 3
10	34.84	0.30	0.48	2x 5
12	48.19	0.25	0.56	4x 3
15	17.91	0.20	0.17	3x 5
15	48.42	0.20	0.45	5x 3
20	30.14	0.15	0.21	4x 5
18	61.65	0.17	0.47	6x 3
27	85.51	0.11	0.44	9x 3

4.4.3 Study on *G*x Paralleled *N*-phase Inner-Phase Pseudo-Multiphase VSI

In some machine designs, the phase winding is composed of parallel-connected coils having the same electrical angle. This kind of machine can be controlled via the strategies studied in previous sections or via another newly proposed strategy: Inner-Phase Pseudo-Multiphase VSI (IPPM-VSI).

In IPPM-VSIs, the currents in the machine coils within one phase are individually or semi-individually controlled, thus the 'multiphase' reference, while their electrical angles are the same, thus the 'pseudo' reference. This strategy is applied for each phase thus the 'inner-phase' reference.

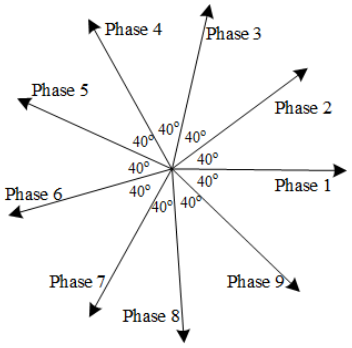
The implementation of IPPM-VSIs requires reconfiguration of the machine phase winding coils resulting in a *G*x paralleled *n*-phase machine. Such a configured machine is discussed here based on a 9-phase machine design presented by Yang in [158].

In the 9-phase machine design, the phases are distributed symmetrically as shown in Figure 4.37 (a) where each phase is composed of 4 parallel-connected coils having the same electrical angle, as shown in Figure 4.37 (b). This machine can be connected as the 9-phase machine as shown in Figure 4.37 (c) and one of the 9-phase related strategies mentioned previously can be applied to the VSI. Moreover, the flexibilities of coils connection results in different machine drive system configuration and VSI strategies. The 2x parallel, 9-phase machine with 2 star points configurations in each phase is shown in Figure 4.37 (d), where two coils in each phase are connected in parallel and the summed current through them controlled, *I1_A* and *I1_B*, referring to here as 'semi-individually controlled'. The 4x paralleled 9-phase machine with a 4 star point configuration in each phase is shown in Figure 4.37 (e), in which the current through each coil is individually controlled, *I1_A*, *I1_B*, *I1_C* and *I1_D*, refer to as 'individually controlled'. The higher current controllability and flexibility enables the application of interleaved carrier waveforms in the individual coil current control, which has the potential to decrease the DC-link capacitor requirements via the group based interleaving technique.

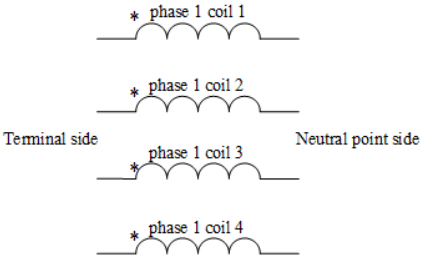
The DC-link capacitor requirements for such connections are studied and compared against the 9-phase as a benchmark system. The normalized DC-link capacitor RMS current and

capacitor charge variation are shown in Figure 4.38. The DC-link capacitor RMS rating comparisons are given in Table 4.7 and illustrated in Figure 4.39. The DC-link capacitance comparisons are given in Table 4.8 and illustrated in Figure 4.40.

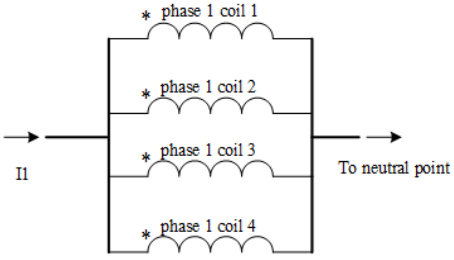
The 3x 3-phase VSI with SVM group based interleaving has the lowest DC-link capacitor RMS rating while the 4x parallel, 9-phase IPPM-VSI SVM group based interleaving has the lowest required DC-link capacitance.



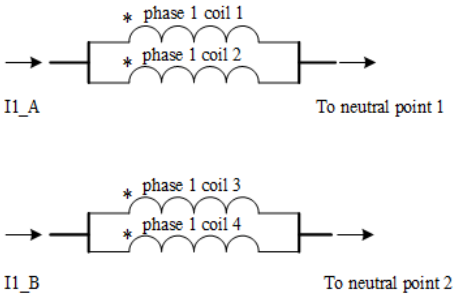
(a) 9-phase machine phase electrical vectors.



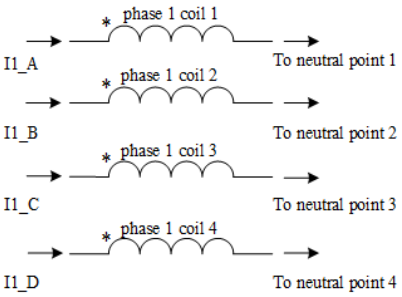
(b) Coil connection in one phase.



(c) Connection configuration 1.

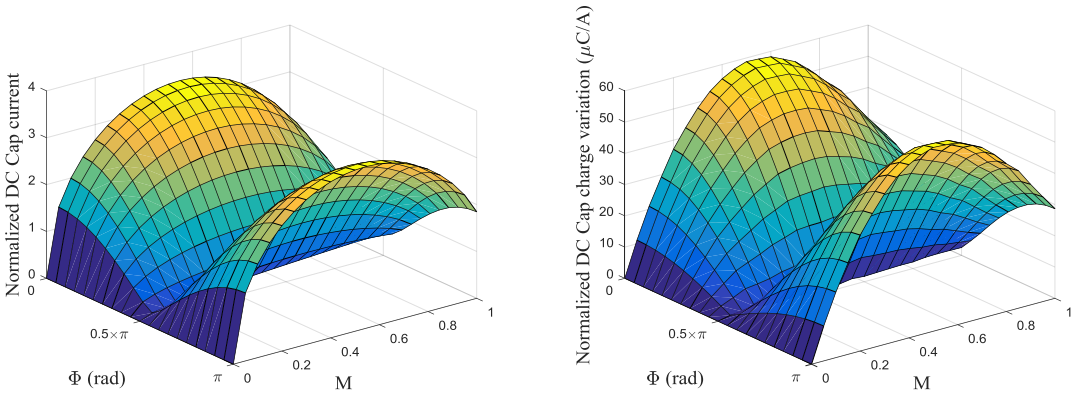


(d) Connection configuration 2.

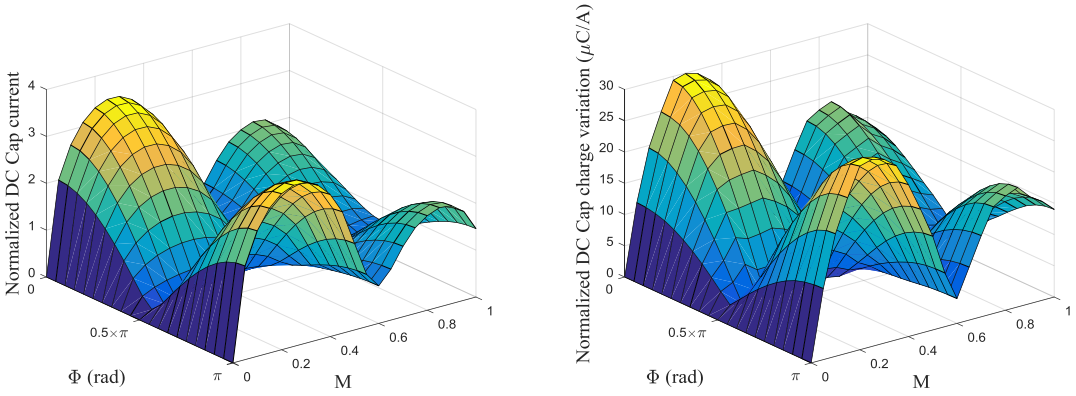


(e) Connection configuration 3.

Figure 4.37 Phase electrical vectors and coil connection in a 9-phase VSI.



(a) 2x paralleled 9-phase VSIs.



(b) 4x paralleled 9-phase VSIs.

Figure 4.38 Normalization values for the 2 and 4 parallel 9-phase IPPM-VSIs with group based interleaved triangular carrier waveform.

Table 4.7 DC-link capacitor RMS ratings comparison among different 9-phase VSIs.

Machine phase number	The maximum normalized DC-link RMS current	Phase current	DC-link RMS rating
9-phase SPWM non-interleaving	1.74	1.00	1.00
3x 3-phase SVM group based interleaving	0.65	1.00	0.37
2x parallel 9-phase IPPM-VSI SVM group based interleaving	3.45	0.50	0.99
4x parallel 9-phase IPPM-VSI SVM group based interleaving	3.44	0.25	0.49

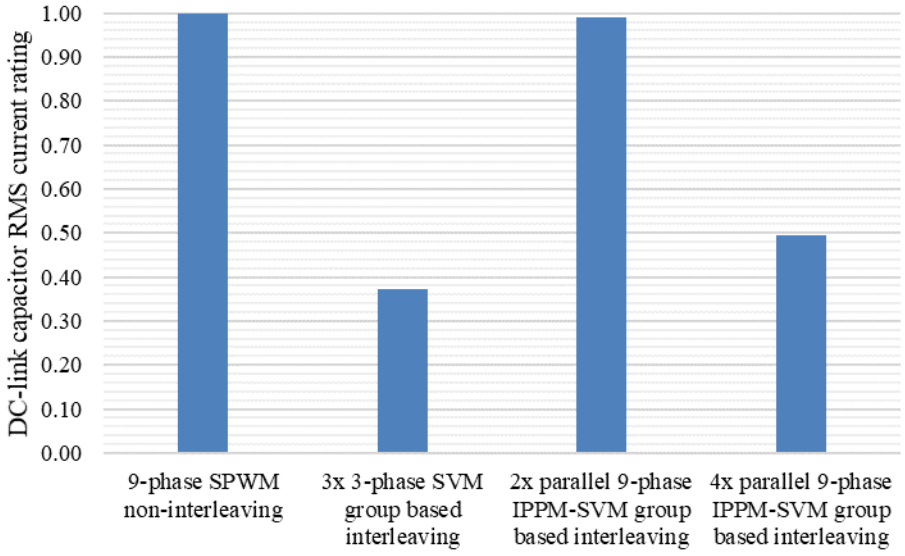


Figure 4.39 DC-link capacitor RMS ratings comparison among different 9-phase VSIs.

Table 4.8 Required DC-link capacitance comparison among different 9-phase VSIs.

Machine phase number	The maximum normalized DC-link charge variation (μC/A)	Phase current	Required DC-link capacitance
9-phase SPWM non-interleaving	29.90	1.00	0.98
3x 3-phase SVM group based interleaving	30.43	1.00	1.00
2x parallel 9-phase IPPM-SVM group based interleaving	58.83	0.50	0.97
4x parallel 9-phase IPPM-SVM group based interleaving	29.92	0.25	0.25

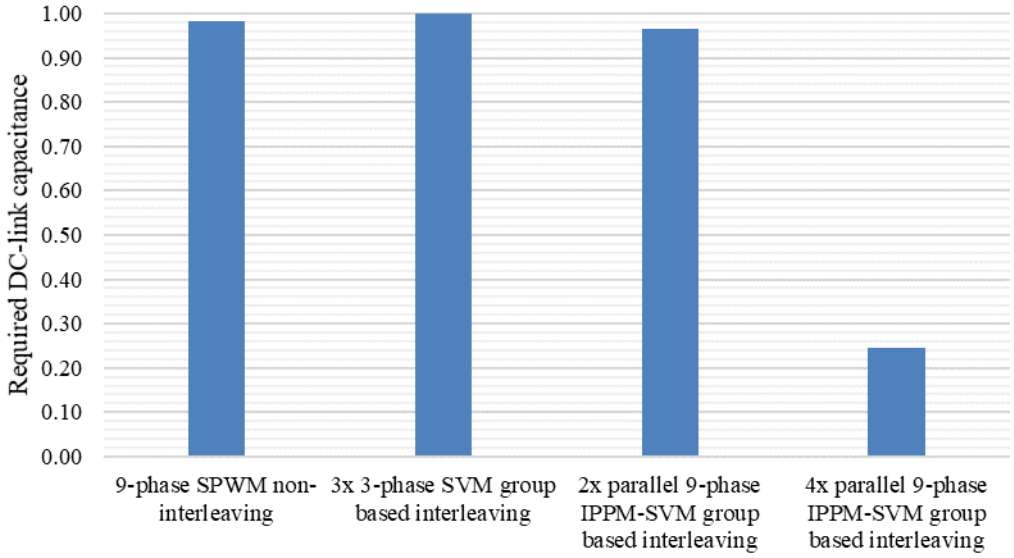


Figure 4.40 Required DC-link capacitance comparison among different 9-phase VSIs.

4.5 Summary

The investigation method for the DC-link requirements, e.g. RMS current ratings and capacitance, are proposed for arbitrary phase number two-level VSIs, based on which the DC-link capacitor requirements are assessed and compared quantitatively among different phase number VSIs. The normalized DC-link capacitor RMS current and one newly proposed concept – normalized DC-link capacitor charge variation are applied to generalize the analysis quantitatively. The research results show that under the equal power output, the implementation of multiphase VSIs can decrease the DC-link capacitor requirements. The DC-link capacitor RMS current rating decreases slightly (about 10%) with the increased phase number in VSIs. The DC-link capacitance decreases with the increased phase number, for example, 54% reduction in the 9-phase than that in the 3-phase.

Moreover, for the VSIs of higher phase numbers, their increased flexibilities and degrees of freedom make it possible to further decrease the DC-link requirements via the implementation of the group based interleaved carrier waveform. Additionally, different switching strategies, switching frequencies and carrier waveforms can also influence the DC-link capacitor requirements. Furthermore, the new conceptual *G*x paralleled *n*-phase IPPM-VSI is proposed and the characteristics of 2x paralleled 9-phase and 4x paralleled 9-phase IPPM-VSIs are studied and compared with the other 9-phase systems. The 4x paralleled 9-phase IPPM-VSI has the lowest required DC-link capacitance and the second lowest DC-link capacitor RMS current.

The analytical study is validated in the following chapter.

Chapter 5

Experimental Test Facility and Validation Results

5.1 Introduction

The full test validation of the multiphase VSI options studied in the preceding chapters is clearly out of the scope of this thesis research. However, a number of measurement points can be made to validate the analytical study previously reported by way of a brushless permanent magnet (BLPM) machine VSI facility that can be configured for either 3-phase or 9-phase operation. In this chapter the design and utilization of an experimental test facility is described in detail for both the 3- and 9-phase voltage source inverters (VSIs) and the configurable 3- and 9-phase BLPM machine. The experiment validation method is also introduced to support the equitable operational conditions between the 3- and 9-phase machine drive systems for the DC-link capacitor investigation reported in Chapter 4 and hence underpins the thermal discussion reported in Chapter 6. Finally, the test facility is utilized to briefly explore VSI faulted operation for the 9-phase machine drive system with the existing topology and control techniques to support fault tolerance statements proposed in previous chapters. These tests are brief, but form the potential for future research topics.

5.2 Overview of Experimental Test Facility

The experimental test facility contains the 3- and 9-phase VSIs, the configurable 3- and 9-phase BLPM test machine, a BLPM machine acting as the dynamometer load machine, a liquid cooling system for the power electronics heatsink including coolant temperature management and circulating pump, a DC power supply and measurement board. A full the equipment overview is shown in Figure 5.1 (a).

Three full 3-phase IGBT bridge modules, PM50RLA060, with their associated Powerex BP7B driver boards are used for the 3- or 9-phase VSIs. One 3-phase IGBT module is used for the 3-phase VSI while three, 3-phase, IGBT modules are used for the 9-phase VSI, as shown in Figure 5.1 (b). All the IGBT modules are mounted on the liquid cooled heatsink with the distilled water coolant driven by the coolant machine controlling the coolant temperature below 25°, as shown in Figure 5.1 (c). The VSI controller board with a Texas Instrument DSP TMS320F28377D control card and the DC-link capacitor (a variable capacitor bank), are shown in Figure 5.1 (d) and Figure 5.1 (e) respectively.

The 3- and 9-phase VSIs topologies are illustrated in Figure 5.2 (a) and Figure 5.2 (b) respectively, where the 9-phase machine drive system can be either a true 9-phase system with one star point, or a 3x 3-phase system with three unconnected star points. Current (LEM LA-55P) and voltage (LEM LV-25P) transducers, as shown in Figure 5.3 (a), are used to measure the phase 1 current (I_{PH_1}), IGBT module DC input current (I_{DC_IGBT}), DC-link capacitor current (I_{DC_Cap}), DC power supply unit current (I_{PSU}), and phase 1 phase-to-star voltage (V_{PH_1}), as labelled in Figure 5.2 (a) and Figure 5.2 (b) for clarity. A voltage differential probe (20 MHz) is used to measure the DC-link voltage (V_{DC}), as shown in Figure 5.3 (b).

Depending on the variety of the VSI applications there can be different kinds of DC power sources on the VSI DC-link, which has been discussed before in Chapter 4. Despite their differences, mainly the voltage and current ripples and harmonic contents, the similarity among them is that, for example, during the inverter steady state operation (constant power output) their voltage and current outputs are both supposed to be as constant as possible due to correct design of the DC-link capacitor, that is, the expected full absorption of the

inverter current pulses due to the switching or commutation events and hence the stabilized instantaneous DC-link voltage. Even under the VSI transient operation, for example corresponding the acceleration or deceleration modes of a machine drive system, the DC power source is expected to output steady voltage and smooth current which approximates to the average inverter current input during one switching or commutation event. The DC-link capacitor functions under both steady and transient operations are the same. Hence, the DC-link investigation in Chapter 4 is conducted under steady-state and representative for the DC-link capacitor requirements. Stabilizing the DC-link voltage and smoothing the pulsed current from the switch side, the DC-link capacitor functions to approximate the inverter to a constant resistive load, while under the transient state to be equivalent to a resistive load with varying resistances, with the DC power source side converging to an ideal DC voltage source with constant current output. To emulate the DC power source and isolate the DC-link capacitor from the possible applied DC power source side capacitive interferences, an inductive load of 100 μF, 0.1 Ω is used as shown in Figure 5.3 (c) and Figure 5.3 (d). The applied DC power supply (Ametek SGI 500/20) is shown in Figure 5.3 (e). Consequently, an authentic DC-link environment is built such that the current from the emulated DC power source is nearly constant, with the study target DC-link capacitor absorbing almost all of the current pulses from the VSI switch side and stabilizing the DC-link voltage ripple to within 5% of the rated average DC-link voltage - the criteria discussed in Chapter 4.

5.3 Configurable 3- and 9-phase BLPM machine

The 3- and 9-phase BLPM machine is implemented via the same machine stator and rotor. The stator winding is designed to be configurable for either 3- or 9-phase by connecting the stator coils in either of two configurations.

The BLPM test machine has a 4 pole-pair rotor, as shown in Figure 5.4. The test machine rotor originally had a hollow shaft and geared output. This rotor has been modified to allow testing for this thesis by adding 2 end pieces and a central connecting threaded rod. Figure 5.4 (a) shows the three parts of the rotor, Figure 5.4 (b) shows the whole rotor assembly, while Figure 5.4 (c) and Figure 5.4 (d) show detailed views of the rotor magnets and containment sleeve for two different views. Part of the rotor sleeve has been removed to allow the rotor magnet dimensions to be measured for input to a finite element analysis (FEA) study of the machine that is reported elsewhere.

The stator laminations are stacked and fixed into the machine case as shown in Figure 5.5 (a). Slot liner insulation paper pieces are cut as shown in Figure 5.5 (b) and fitted into the machine slots as shown in Figure 5.5 (c) and Figure 5.5 (d). Cardboard end plates with the same shape as the laminations are attached at the each end of the stator lamination stack to prevent the damage of winding insulation as well as provide the insulation between the stator end-windings and the laminations.

There are 9 teeth on the machine stator and 3 coils on each tooth. Every coil is wound with 30 turns of a bundle of copper wires. Each bundle contains 1 wire of 0.56 mm outer diameter (OD) and 4 wires of 0.28 mm OD to realize the desired total cross-sectional area per turn.

In the 3-phase machine, the 3 coils on one tooth are connected in parallel (then still a 30 turns coil) and 3 consecutive teeth are connected in series with a winding sense as shown in Figure 5.6 (a), resulting in a 90 turns per phase. For the 9-phase winding implementation, the 3 coils on each tooth are connected in series and in the sense as shown in Figure 5.6 (b), again resulting in a 90 turns per phase.

The machine stator and winding details are shown in Figure 5.7 (a), in which the 40° mechanical angle displacement between two consecutive teeth is identified. The coils

electrical angles on each tooth is given in Table 5.1. The tooth number and insulation layer are also labelled in Figure 5.7 (a).

Tooth 1, 2 and 3 coil geometry vectors are shown in Figure 5.7 (b), where the mechanical angle between the coils on the consecutive teeth is 40°. For the 4 pole-pair machine, the back-EMF vectors of coils on tooth 1 2 and 3 are shown in Figure 5.7 (c).

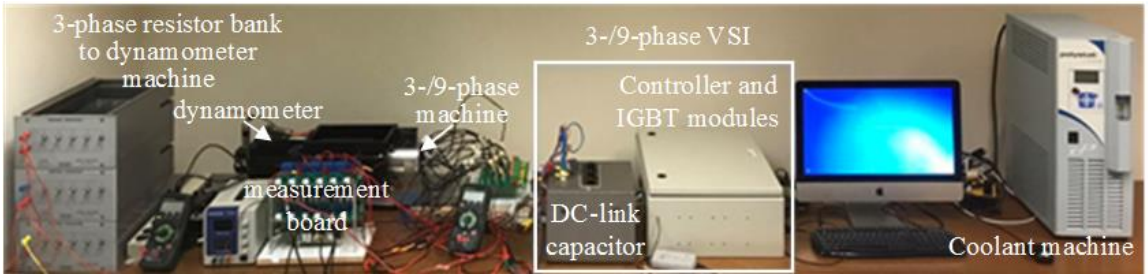
To characterize the BLPM machine tests are conducted for the phase back-EMF, phase resistance and inductance, and parameter consistency of the different phases to confirm balance. The machine back-EMF tests are conducted for both 3- and 9-phase configurations at 1000 RPM, as shown in Figure 5.8 (a) and Figure 5.8 (b) respectively. The back-EMF coefficients or phase-to-star RMS voltage versus the rotational speed, are 9.38 Vphrms/kRPM for the 3-phase machine and 9.30 Vphrms/kRPM for the 9-phase machine. The machine phase inductances (phase-to-star) are measured at different rotor positions for the 3-phase and 9-phase configurations via an inductance bridge test excited at 120 Hz. The winding self-inductances are shown in Figure 5.8 (c) and Figure 5.8 (d) respectively, where the periodical variation is due to the rotor saliency, and the maximum and minimum values are the upper and lower boundaries from the LCR meter measurements. A Leader LCR-745 meter was used for the test, as shown in Figure 5.8 (e). From the measured data, the synchronous inductances for the 3-phase and 9-phase machine are 1.2 mH and 2.4 mH respectively.

The machine phase DC resistance is measured by applying a steady DC voltage to the phase winding and dividing this voltage by the current, from which the DC resistances of 3- and 9-phase machine are 0.26 Ω and 0.8 Ω respectively. The current ratings of the 3-phase and 9-phase machine are set to 15 Arms and 5 Arms according to test experience of the thermal performance of the machine, while higher currents are allowable for short time duration. The DC-link voltage is set to 110 V according to the machine back-EMF coefficient and its power level (1 kW). The 3- and 9-phase BLPM machine specifications are summarized in Table 5.2.

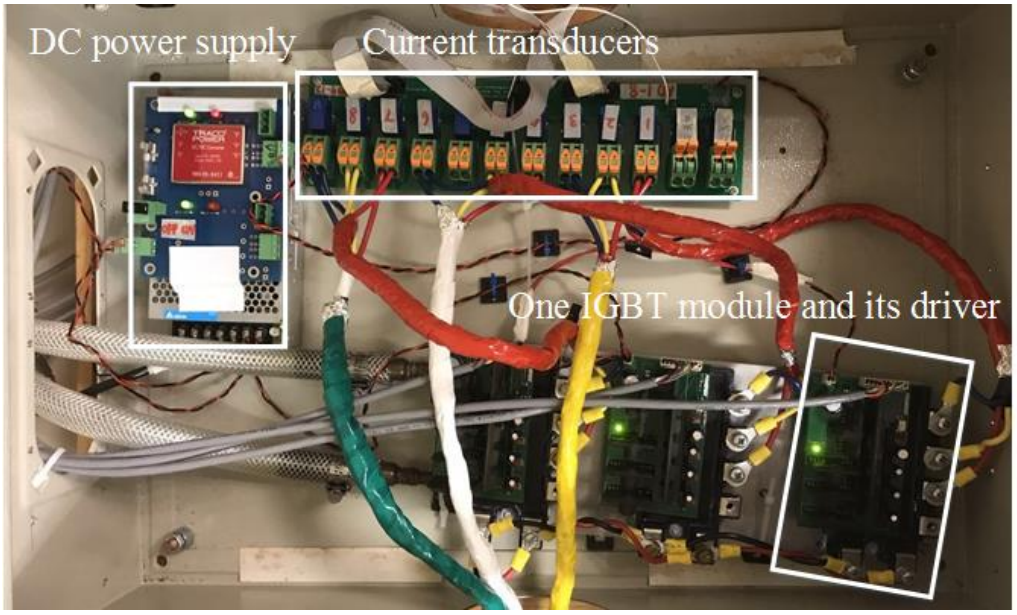
The dynamometer shown in Figure 5.9 (a) is a 3-phase permanent magnet synchronous machine from Control Techniques with the model number UNIMOTOR UM

142UMB300CACAB and specifications are detailed in Table 5.3. It is mechanically coupled to the test machine via the in-line torque transducer. The machine electrical output is connected to a 3-phase resistor bank, as shown in Figure 5.9 (b) to realize the different load torques.

A SAW based in-line torque transducer is coupled between the test machine and the dynamometer machine to measure torque output of the test machine, as illustrated in Figure 5.9 (c) and Figure 5.9 (d), showing the Sensor Technology E300 RWT toque transducer and its associated data acquisition unit, the Sensor Technology Display E302.



(a) Equipment overview.



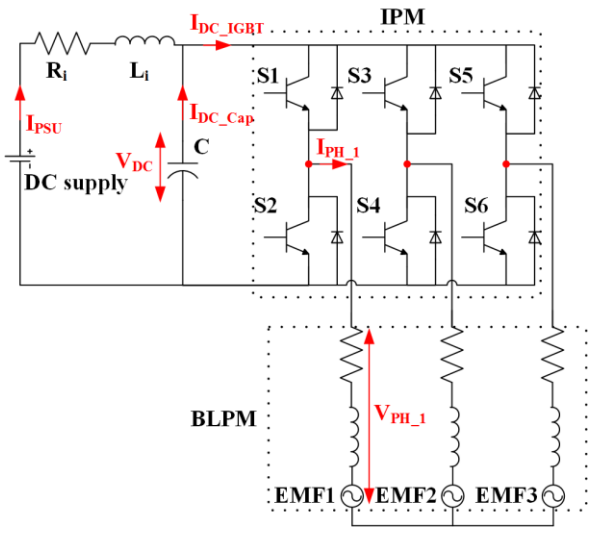
(b) IGBT modules on liquid heatsink, current sensors and its DC power supply.

(c) Coolant system.

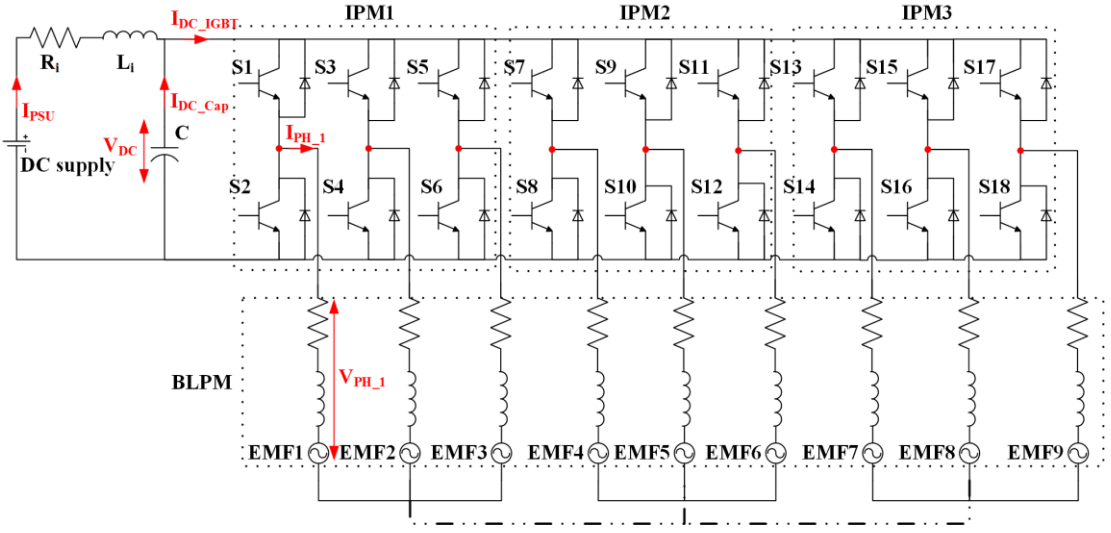
(d) DSP controller board and interface board.

(e) DC-link capacitor.

Figure 5.1 Multiphase VSI experiment test facility.

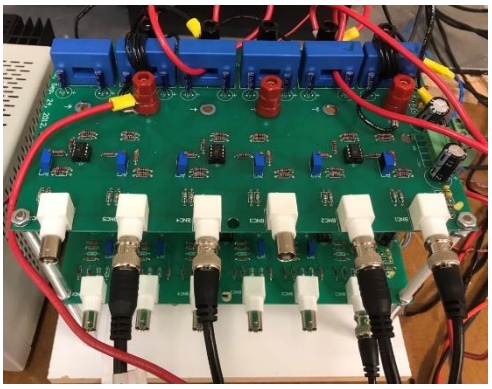


(a) 3-phase.



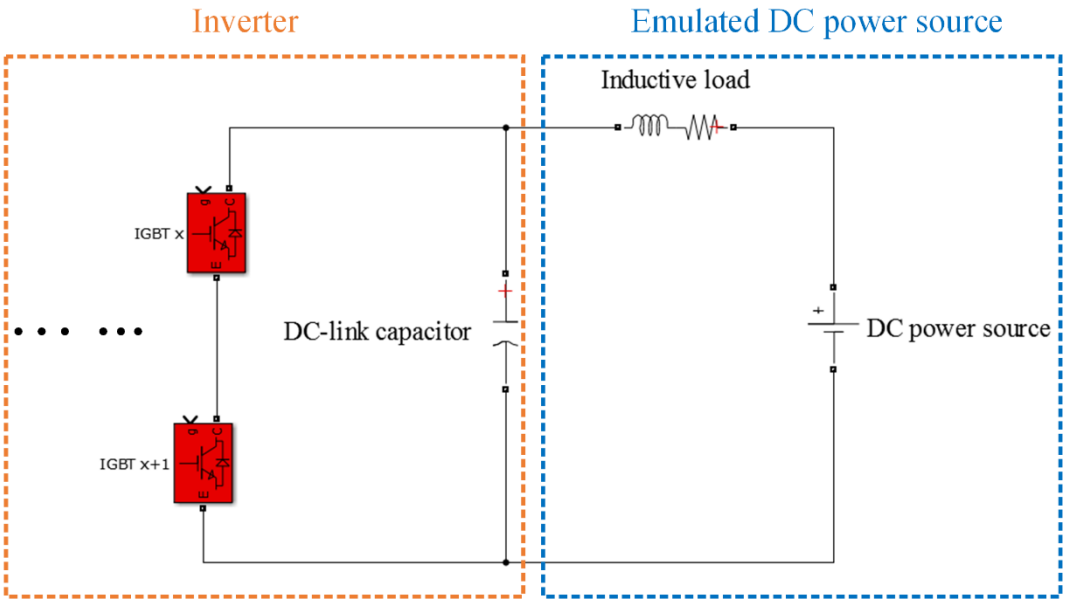
(b) 9-phase.

Figure 5.2 3- and 9-phase machine drive topologies and measurement points.



(a) Current and voltage measurement board.

(b) Differential voltage probe.



(c) DC-link power supply and VSI diagram.

(d) Filter inductor.

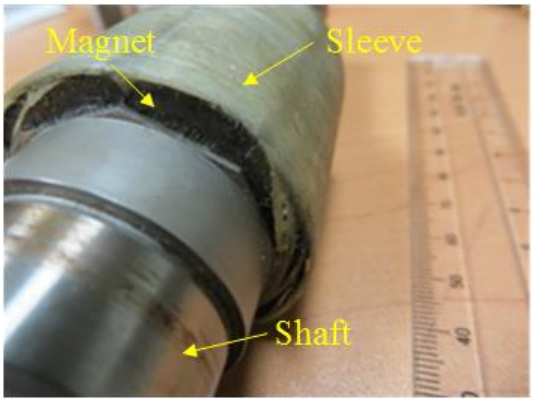
(e) DC power supply.

Figure 5.3 The measurement equipment and DC power supply.

(a) Rotor and shaft disassembly.

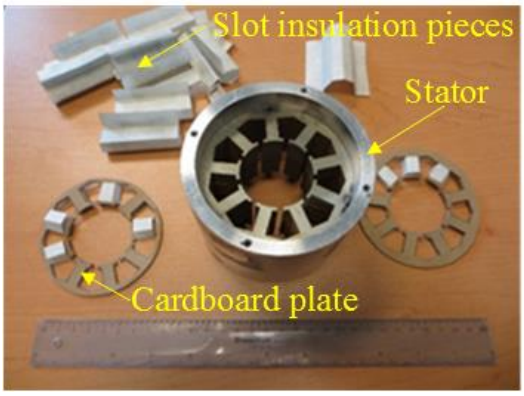
(b) The whole rotor.

(c) Rotor view 1.



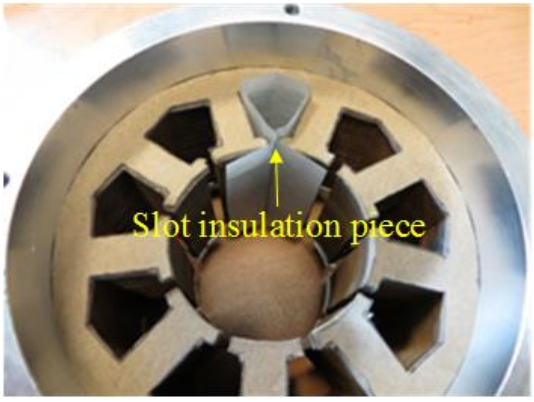
(d) Rotor view 2.

Figure 5.4 Rotor views.



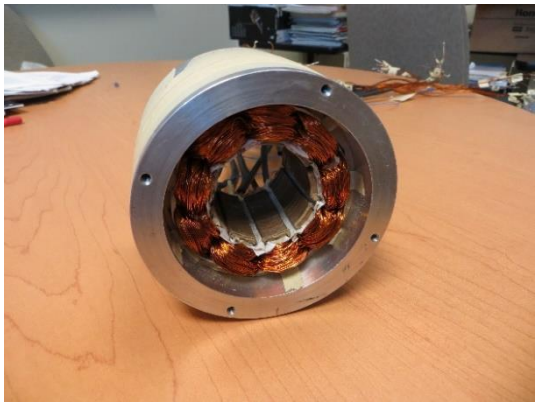
(a) Stator core and insulation pieces.

(b) Slot insulation paper piece.

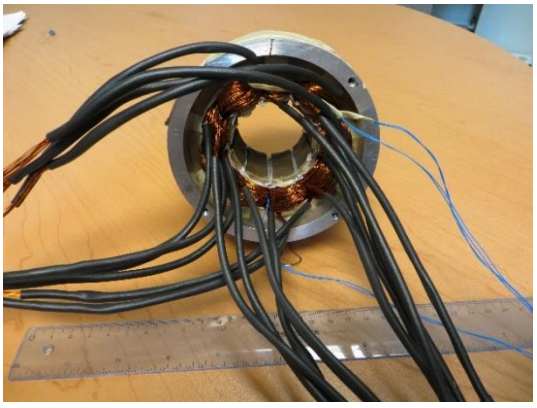


(c) Slot insulation paper installment 1.

(d) Slot insulation paper installment 2.

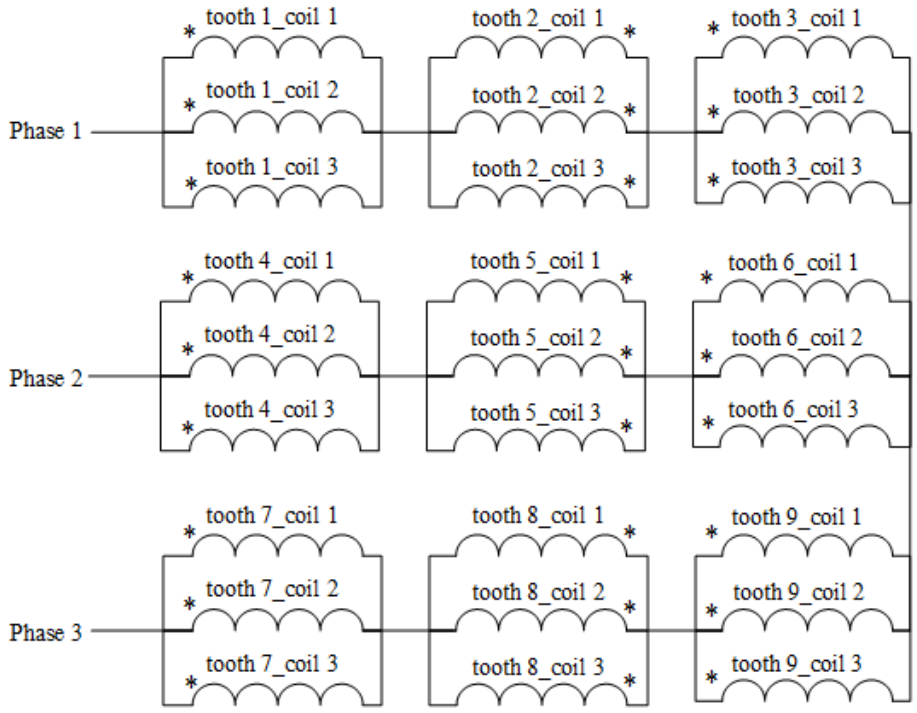


(e) Stator winding opposite the end winding side.

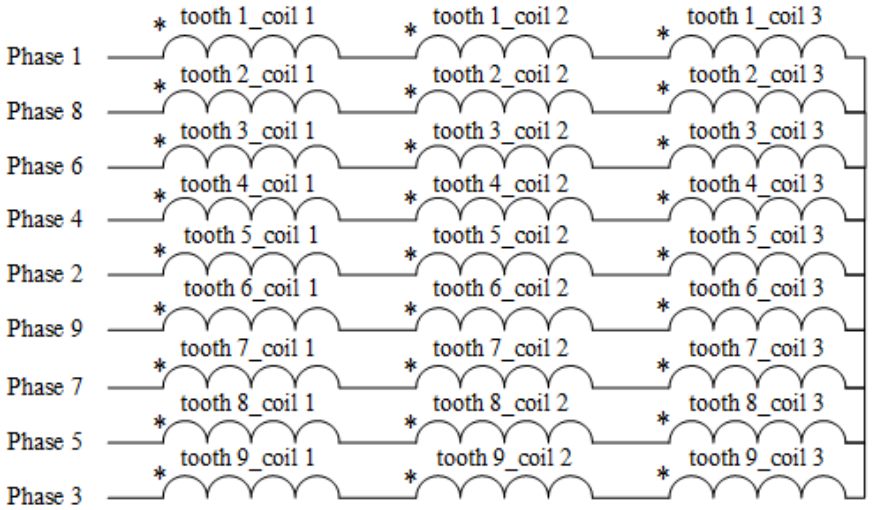


(f) Stator winding view at the end winding side.

Figure 5.5 Stator views.

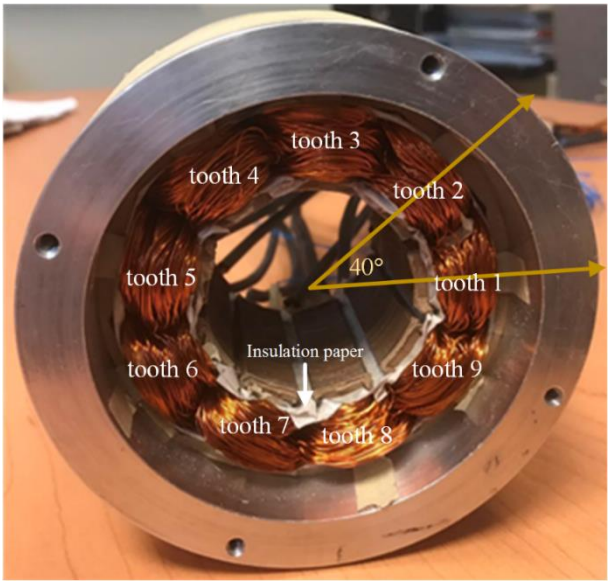


(a) 3-phase.

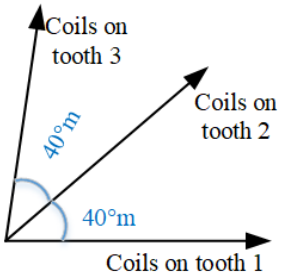


(b) 9-phase.

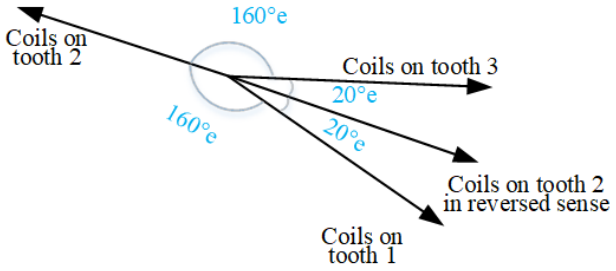
Figure 5.6 3- and 9-phase machine stator winding configuration.



(a) Machine stator showing wound teeth.



(b) Back-EMF in mechanical angle.

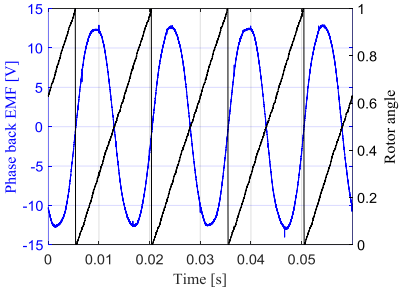


(c) Back-EMF in electrical angle (4 pole-pair).

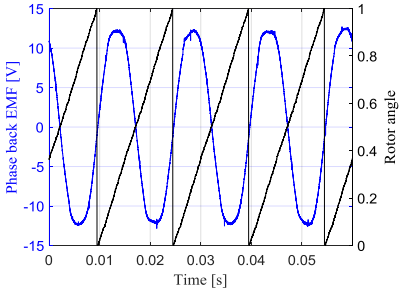
Figure 5.7 Machine stator winding and back-EMF vectors.

Table 5.1 Stator coils mechanical angle and back-EMF electrical angle.

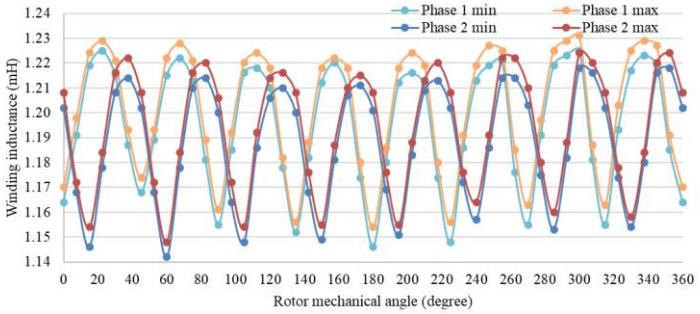
Tooth number	1	2	3	4	5	6	7	8	9
Mechanical angle (degree)	0	40	80	120	160	200	240	280	320
Back-EMF Electrical angle (degree)	0	160	320	120	280	80	240	40	200



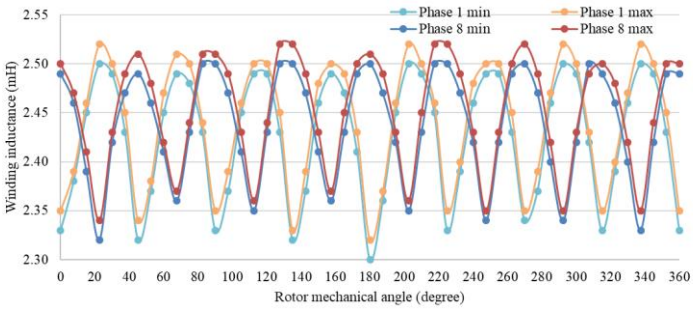
(a) 3-phase back-EMF test and corresponding rotor electric angle.



(b) 9-phase back-EMF test and corresponding rotor electric angle.



(c) 3-phase winding inductance with respect to rotor mechanical angle.

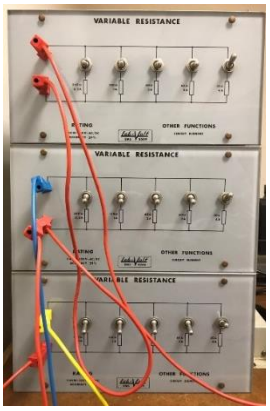


(d) 9-phase winding inductance with respect to rotor mechanical angle.

(e) LCR meter for machine phase inductance measurement.

Figure 5.8 Machine specification measurement.

(a) Dynamometer PMSM machine.



(b) 3-phase resistor banks.

(c) Torque transducer.

(d) Data acquisation box.

Figure 5.9 Dynamometer and torque transducer system.

Table 5.2 Test BLPM machine specifications.

Phase number	3	9
Phase to star synchronous inductance (mH)	1.2	2.4
Phase to star DC resistance (Ω)	0.26	0.8
Phase current rating (Arms)	15	5
Back-EMF coefficient (Vph(rms)/krpm)	9.38	9.30
DC-link voltage (V)	110	
Rated speed (rpm)	3000	
Rated power (kW)	1	

Table 5.3 Dynamometer machine specifications.

Torque constant Kt (Nm./Aph(rms))	1.6
Back-EMF constant Ke (Vph(rms)/krpm)	56.6
Phase to phase resistance (Ω)	1.72
Phase to phase inductance (mH)	13.3
Rated speed (rpm)	3000

5.4 Experimental Validation

The 3- and 9-phase BLPM machine has the same rotor, stator iron circuit and configurable stator winding, which results in the same material volume and equitable 3- and 9-phase machine drive systems under the same torque speed operation points, i.e. same copper losses, similar iron losses (maybe slightly different due to the different electromagnetic flux distribution) and almost the same back-EMF.

The experimental facility is applied to validate the analytical study in Chapter 4, DC-link capacitor investigation. Although the 3- and 9-phase BLPM machines are 1 kW, it is the analytical study and design method that the experimental facility and its test results validate no matter the size and power rating of the machine. Moreover, because the 9-phase machine drive system is a specific example of the multiphase machine drive systems, the experiments partially validate the multiphase analytical study and design method for arbitrary phase number multiphase machine drive systems DC-link capacitor investigation. Furthermore, the research conclusion in Chapter 4 supports the study in Chapter 6 reducing the size of DC-link capacitor by 2/3 in a typical EV application by the implementation of 9-phase traction machine as opposed to a more traditional 3-phase system.

This experimental facility is also used for the experimental validation of the studies on different switching strategies for multiphase VSIs reported in Chapter 3.

The experiment tests are conducted under different operating points, as shown in Table 5.4 with a DC-link capacitor of 90 μF Ω. The machine torque output is both measured from the torque transducer and estimated via the power on the resistor bank connected to the dynamometer machine. From the results in Table 5.4, the measured torque values have the same trend with the estimated ones, while at each operating point the measured torque is slightly higher than the estimated due to small losses in the dynamometer fractional, iron and copper losses that are not considered in the torque estimation.

As the DC-link voltage ripple is within 5% of the DC-link voltage under all the validation tests with the DC-link capacitance 90 μF, the consistency of DC-link RMS current with different DC-link capacitances is verified for DC-link capacitance 120 μF and 150 μF, as

detailed in Table 5.5. Although slight differences occur, this can be negligible and will not influence the DC-link capacitor RMS current and the experimental validation.

The analytical study results are compared with the experimental ones and presented in the form of waveforms and tables. The results show good correlation with some acceptable errors (within 15% for normalized DC-link RMS current). In this section some selected representative validation results are shown containing the DC-link capacitor RMS current independence of switching frequency, the DC-link capacitor current profiles, the normalization results, and the original experimental waveforms. All the processed data is tabulated in Appendix A2.

The DC-link capacitor RMS current does not change with the variation of the switching frequency which is discussed in the analytical study and validated here as detailed in Table 5.6 and Table 5.7. Hence, the DC-link RMS current consistency is validated for different switching frequencies (5 kHz and 10 kHz) and strategies.

Figure 5.10 shows the DC-link capacitor current profile comparisons between the analytical digital simulation and experimental results for two different strategies, from which the experimental results are shown to match the simulation results, although there are some local differences between them due to the simulation and experiment conditional differences.

The normalized DC-link capacitor RMS currents of the 3-phase SPWM non-interleaved system and 3x 3-phase SVM group based interleaved system are validated experimentally, as shown in Figure 5.11. The phase current lagging angle axis is reversed for the observation purpose in Figure 5.11 (b). The experimental result points are located on or in the very close vicinity of the normalized DC-link capacitor RMS current surfaces with some errors (no more than 13.03% as detailed in Appendix A2 Table A 2.1 and Table A 2.14).

Figure 5.12 to Figure 5.15 show some original experimental waveforms of 3-phase, 3x 3-phase and 9-phase systems containing the DC-link capacitor current, the current after DC-link capacitor (VSI switch side input current), phase current, DC-link voltage, phase voltage, and modulation index. The modulation index is not sinusoidal but with some

distortion since the machine is not an ideal resistive-inductive and back-EMF load, but has some rotor position dependent inductance variation characteristics and small back-EMF harmonic content. The group based interleaving technique does not influence the phase voltage waveform for 3x 3-phase VSIs as the 3 sets of 3-phase windings are electrically isolated, and there is no interleaving within each set. However, in the 9-phase VSI, the group based interleaving technique changes the phase voltage shape, as shown in Figure 5.15, where the peak voltage occurs at the whole operating range.

Experimental test results for the DC-link voltage ripples are compared for 3-phase SPWM non-interleaved triangular carrier waveform, 3-phase SPWM non-interleaved saw tooth carrier waveform and 3x 3-phase SVM group based interleaved triangular carrier waveform systems. Although the fundamental frequency related voltage ripple is superimposed, the main contribution to the DC-link capacitor peak to peak voltage ripple is due to the switching event related current pulses through the DC-link capacitor under this steady state test condition. Hence the DC-link capacitor current pulses width and magnitude determine the DC-link capacitor voltage ripple and the maximum value occurs at the high speed and high toque operating point. Because the dynamometer is connected to a passive resistive load and only limited resistance values can be set, the investigated target machine cannot operate under low speed and high torque condition. While the high speed and high torque operation results are representative for the maximum voltage ripples. Hence there is no need to test under very low-frequency operation. The results are shown in Figure 5.16, where 3x 3-phase SVM group based interleaved triangular carrier waveform VSI has the lowest DC-link voltage ripple and the 3-phase SPWM non-interleaved saw tooth carrier waveform VSI has higher DC-link voltage ripple than the 3-phase SPWM non-interleaved triangular carrier waveform VSI. These results match the trends of the analytical study. The 3x 3-phase SVM group based interleaved triangular carrier waveform VSI has the lowest DC-link voltage ripple under the same DC-link capacitance, in other words, to keep the DC-link voltage ripple within the 5% of the DC-link voltage this system requires the lowest DC-link capacitance.

The reasons for the difference between the analytical study and experiment validation results are that in the real experiment environment:

- the phase currents are not pure sinusoidal (some distortion due to the control and switching)
- there are influences from the power supply side (current ripples and voltage ripples) introduced other than the power supply idealization conditions in the analytical study
- there are parasitic components in the circuit implementation
- the harmonic content in machine back-EMF and nonlinear inductance characteristics result in some distortion in the control/modulation waveform (not pure sinusoidal control waveform)
- switching dead time introduces some non-linearity

5.5 Proposed DC-link Capacitor Design Procedure for Multiphase VSI

The DC-link capacitor design procedure is proposed here, as illustrated in Figure 5.17 based on the analytical study and experimental validation.

Following the flow chart of Figure 5.17, the VSI basic specifications containing VSI phase number and configuration, current and voltage ratings, switching strategy and frequency, carrier waveform, and interleaving techniques should be determined. In terms of the DC-link capacitor RMS current rating design, the nominalized DC-link capacitor current surface is calculated, the function of modulation index and power factor, via the procedure in Figure 4.11 (a). The DC-link capacitor RMS current rating can be calculated by the rated phase current and the normalized DC-link capacitor RMS current, which is followed by the experimental validation and the redundancy consideration due to the different conditions between the analytical study and experiment validation. As to the design of the DC-link capacitance, the procedure is similar, as shown in the flow chart.

Table 5.4 Experiment validation tests operating points.

Rotation speed (rpm)	Dyno resistance per phase (Ω)	Estimated torque (Nm)	Measured torque (Nm)
500	12.6	2.9	3.4
1000	30.0	2.6	3.1
1500	40.0	3.0	3.4
2000	60.0	2.7	3.1
2500	80.0	2.5	3.0

Table 5.5 The consistency of DC-link capacitor RMS current with different DC-link capacitances under 3x 3-phase SVM 10 kHz group based interleaved triangular carrier.

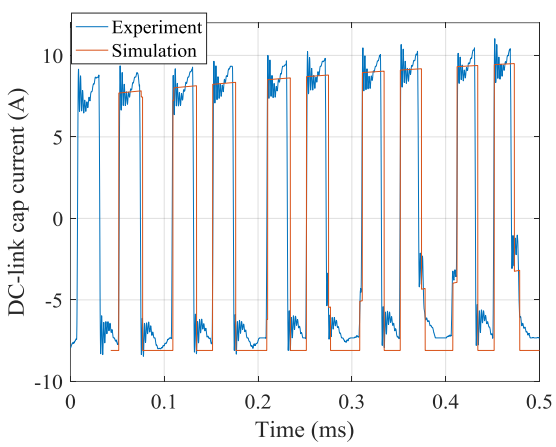
DC-link capacitor (μF)	Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization
90	1000	30.00	0.26	0.43	3.50	1.07	0.30
120			0.26	0.43	3.54	1.06	0.30
150			0.26	0.43	3.54	1.05	0.31

Table 5.6 The consistency of DC-link capacitor RMS current with 5 kHz and 10 kHz switching frequencies under 3x 3-phase SPWM non-interleaved triangular carrier.

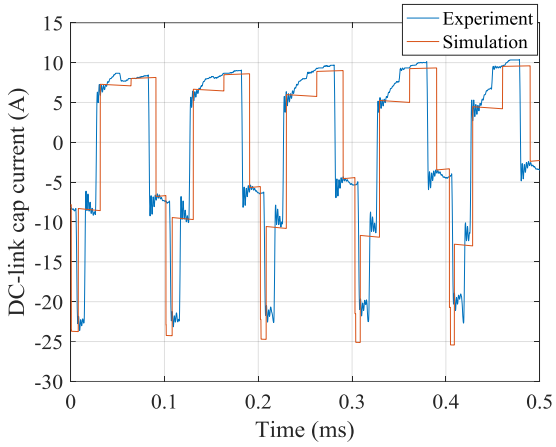
Switching frequency (kHz)	Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization
5	1000	30.00	0.35	0.41	3.58	5.36	1.50
10			0.26	0.45	3.68	5.27	1.43

Table 5.7 The consistency of DC-link capacitor RMS current with 5 kHz and 10 kHz switching frequencies under 3x 3-phase SVM group based interleaved triangular carrier.

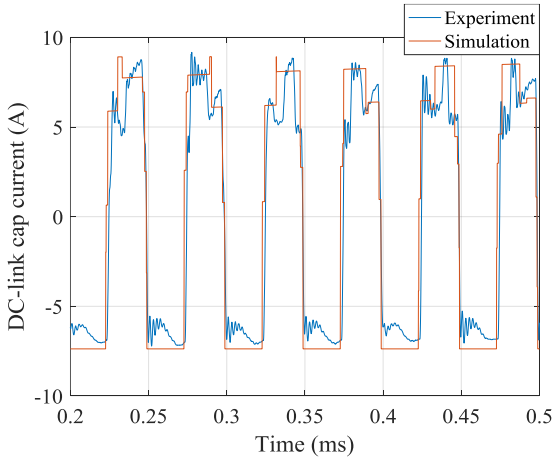
Switching frequency (kHz)	Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization
5	1000	30.00	0.35	0.41	3.53	1.04	0.29
10			0.26	0.43	3.50	1.07	0.31



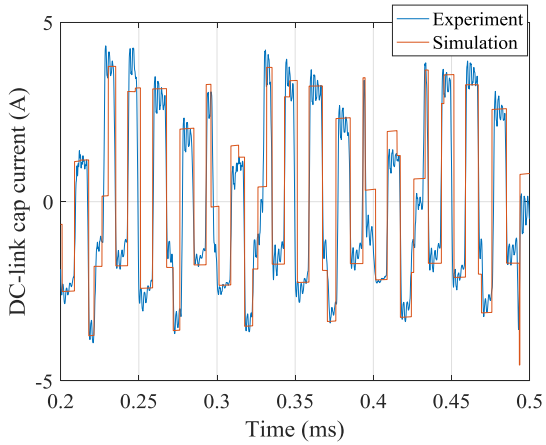
(a) 3-phase SPWM non-interleaving.



(b) 3-phase SPWM symmetrical interleaving.

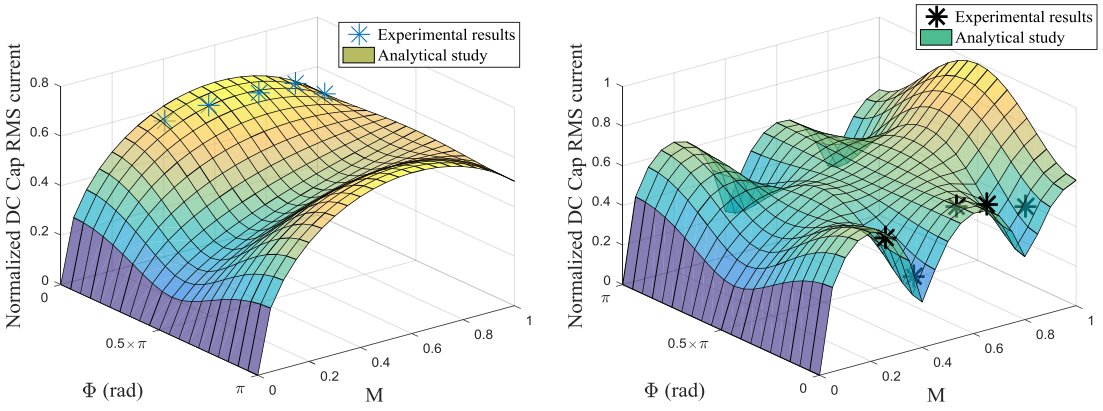


(c) 3x 3-phase SPWM non-interleaving.



(d) 3x 3-phase SPWM group based interleaving.

Figure 5.10 DC-link capacitor current experiment and analytical study simulation comparison at 1500rpm 3.4 Nm (10kHz triangular carrier).



(a) 3-phase SPWM non-interleave.

(b) 3x 3-phase SVM group based interleave.

Figure 5.11 Comparison between the analytical study and experimental results (10kHz triangular carrier).

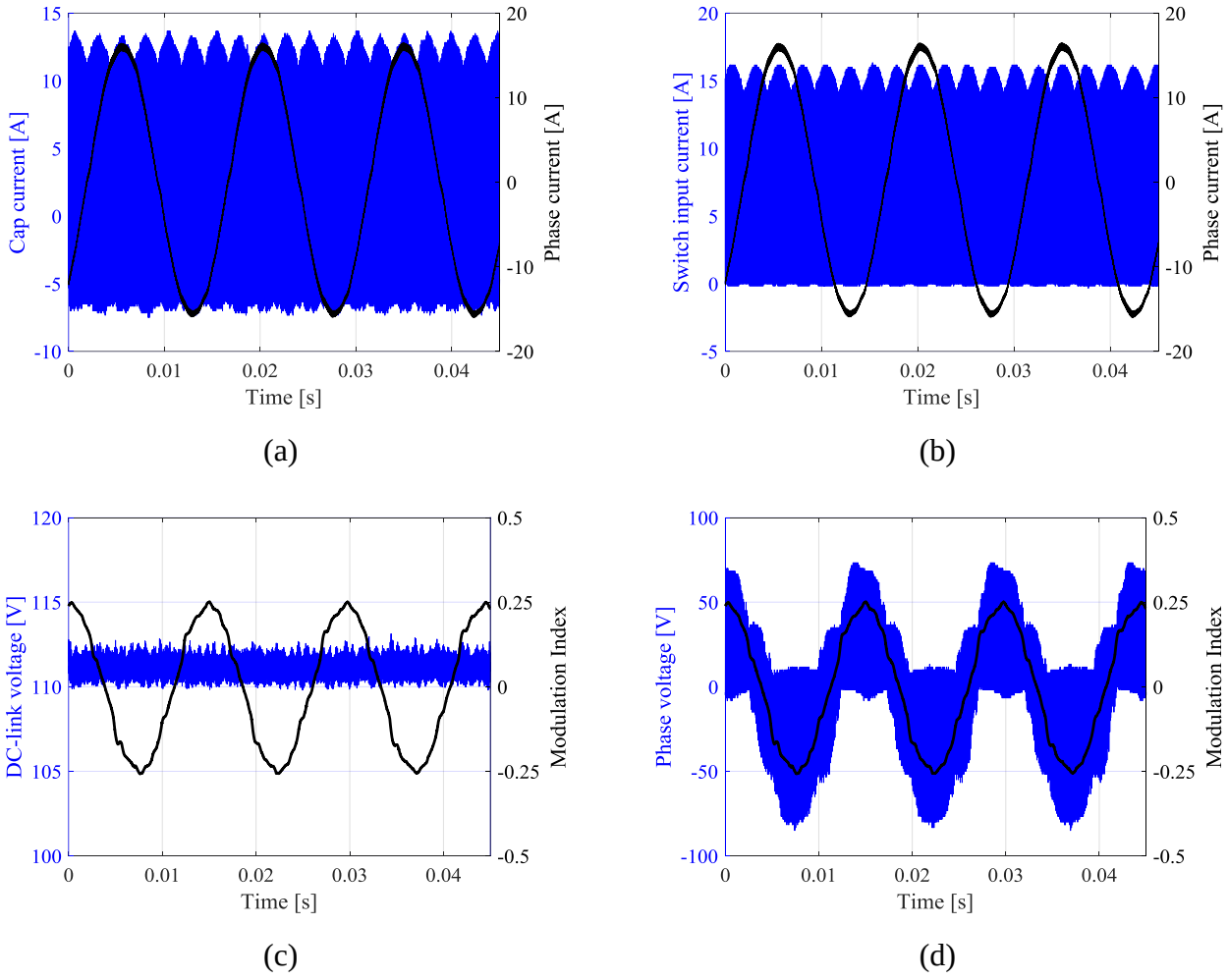


Figure 5.12 3-phase SPWM non-interleaved triangular 10 kHz at 1000 rpm 3.1 Nm.

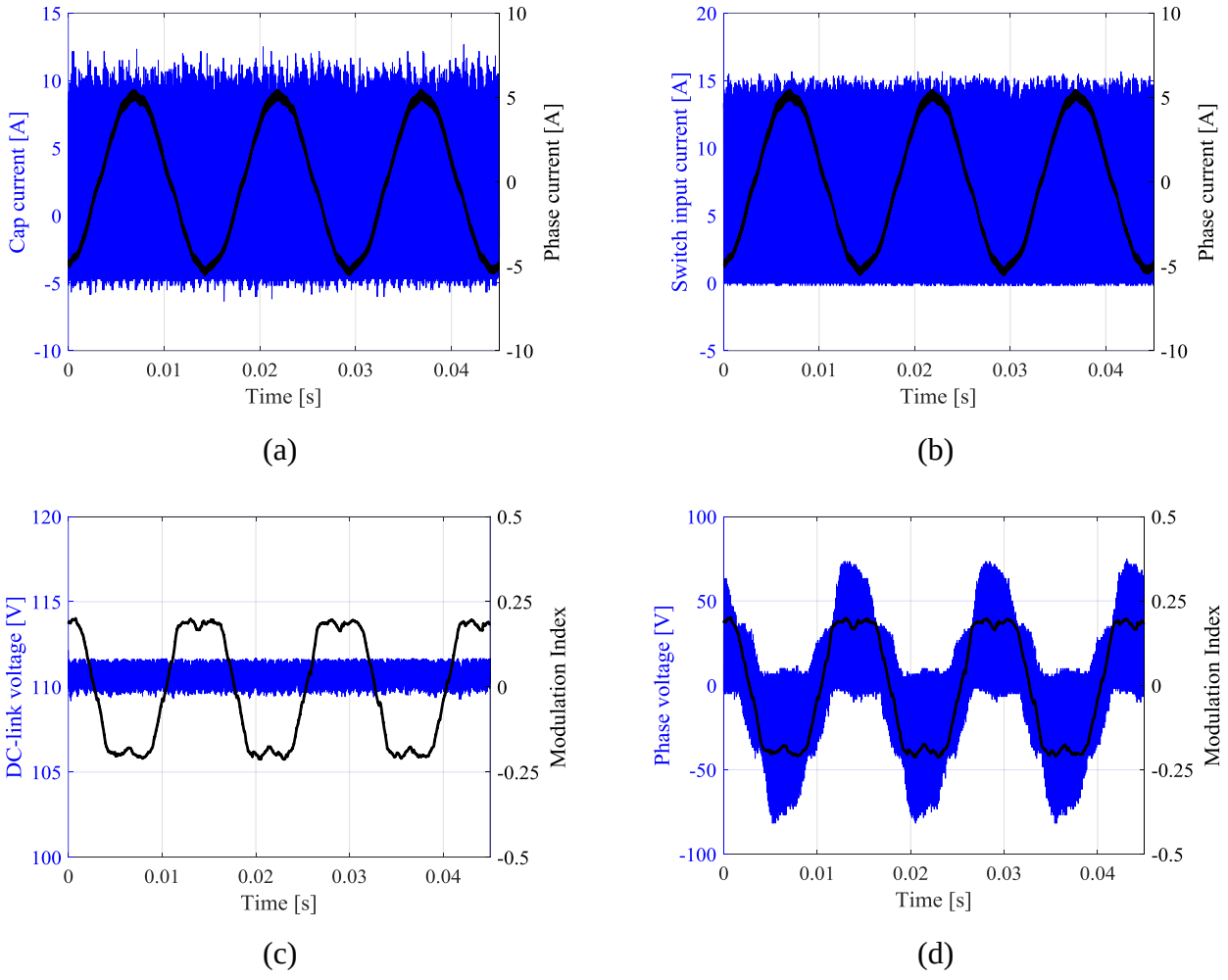


Figure 5.13 3x 3-phase SVM non-interleaved triangular 10 kHz at 1000 rpm 3.1 Nm.

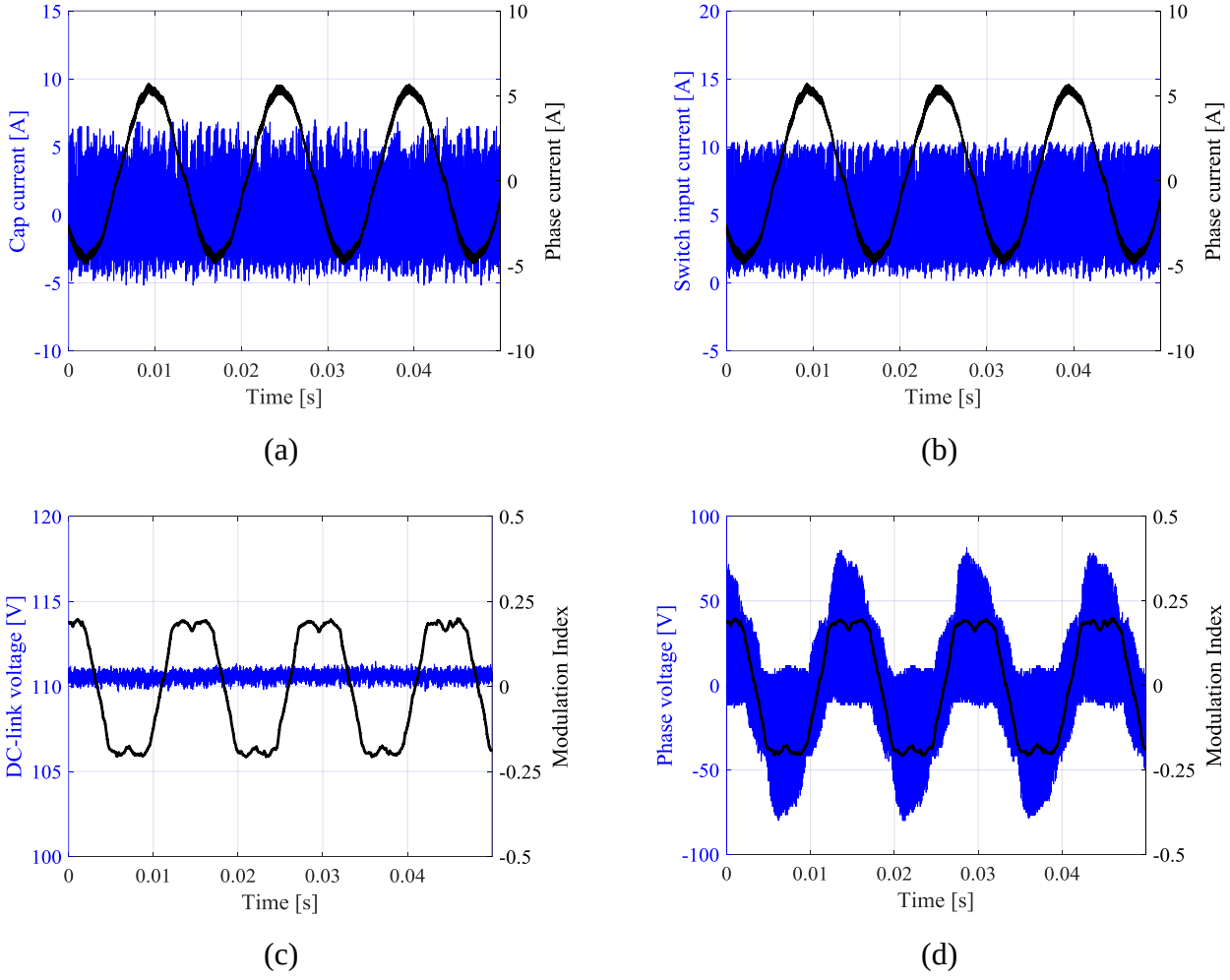


Figure 5.14 3x 3-phase SVM group based interleaved triangular 10 kHz at 1000 rpm 3.1 Nm.

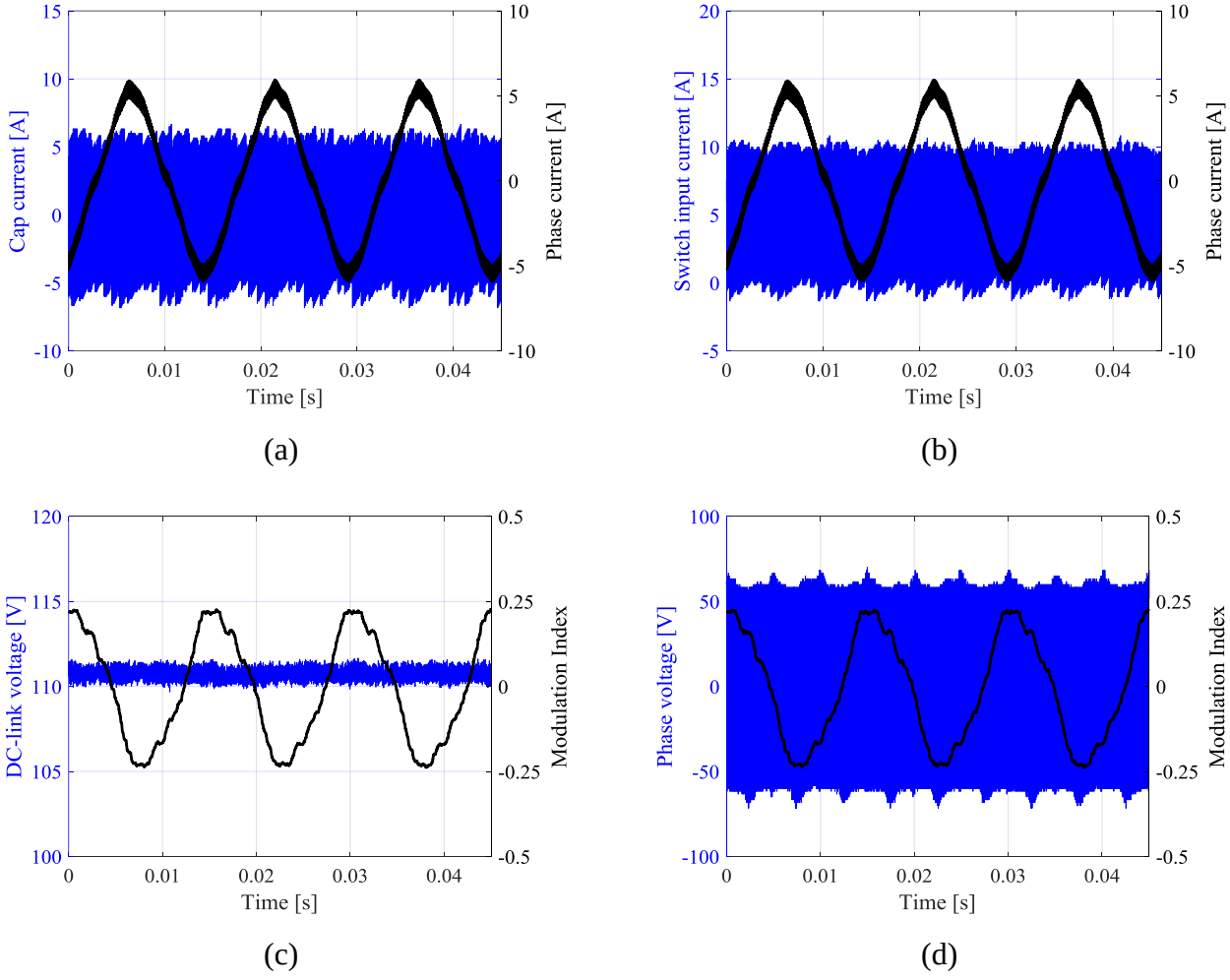


Figure 5.15 9-phase SVM group based interleaved triangular 10 kHz at 1000 rpm 3.1 Nm.

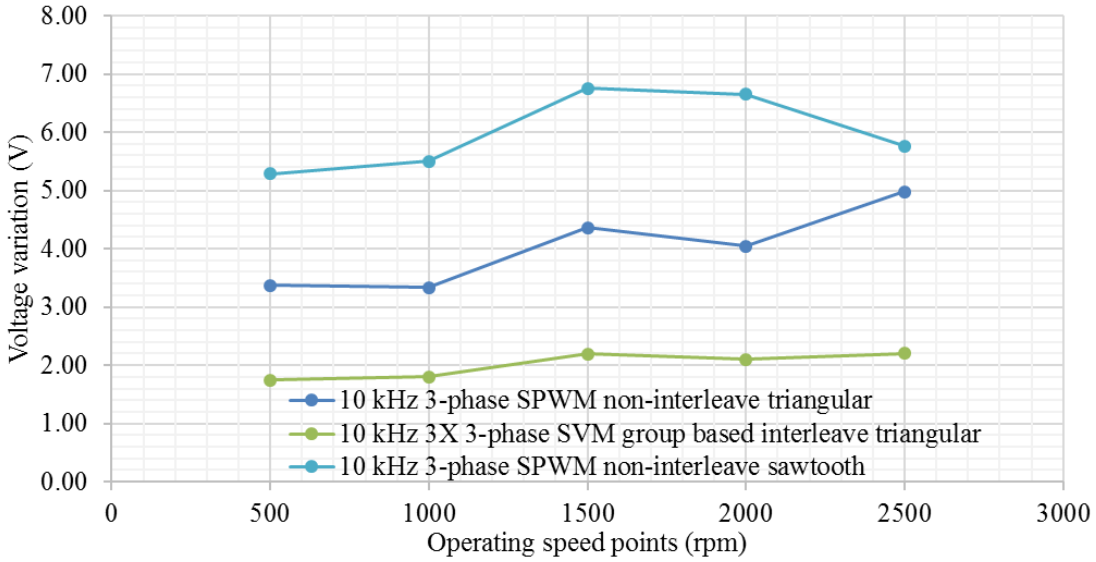


Figure 5.16 DC-link voltage ripple under different operating points and VSIs.

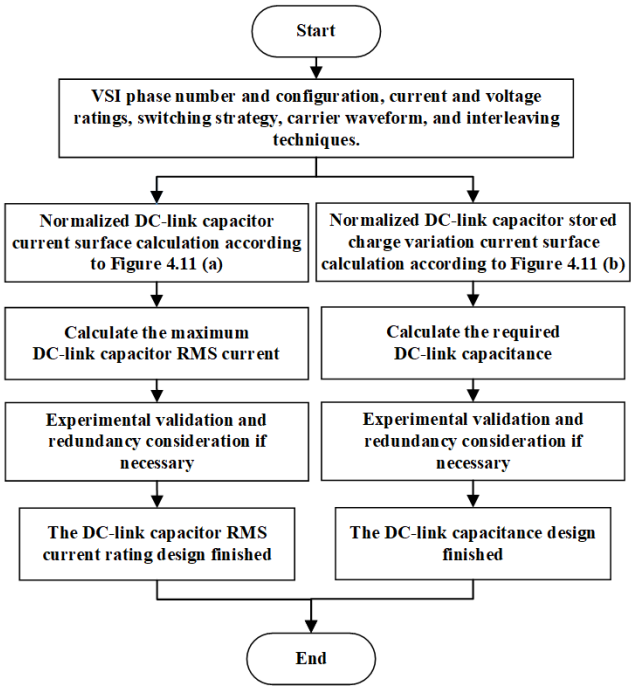


Figure 5.17 Multiphase VSI DC-link capacitor design procedure.

5.6 Nine Phase Machine Drive System Faulted Operation

5.6.1 Overview

Although faulted operation of the multiphase system was not originally part of this thesis content, a number of tests were performed to illustrate the potential for faulted operation while the test facility was still operational. Thus, for the 9-phase machine, the 3 isolated star point configuration, i.e. 3x 3-phase, (A1B1C1, A2B2C2, and A3B3C3), as shown in Figure 5.18 (a), allows the fault isolation within one faulty set of 3-phase winding that are not affecting the other two healthy sets of 3-phase windings if the winding fault only occurs in one set of 3-phase winding.

The experimental test facility is tested under healthy conditions (1000 RPM, 3.1 Nm) as a typical benchmark condition followed by faulty conditions containing one phase open circuit (phase C1), as shown in Figure 5.18 (b); one set of 3-phase winding open circuit (A1B1C1), as shown in Figure 5.18 (c) and 2 sets of 3-phase phase windings open circuit (A1B1C1 and A3B3C3), as shown in Figure 5.18 (d), for which the last two conditions emulate triggered protection mechanisms, and the operation of 2/3 and 1/3 of the full winding. The phase currents under faulted condition operation are constrained to be within the healthy condition phase current corresponding to the power device current rating in the practical design.

5.6.2 Healthy Condition

The phase currents are balanced under the healthy conditions, as shown in Figure 5.18 (e), where the phase currents electrical angle relation matches with that in Figure 5.18 (a). Figure 5.18 (f) shows the DC-link capacitor current and instantaneous torque highlighting some vibration due to the machine rotor shaft eccentricity and experimental facility mechanical coupling.

5.6.3 One Phase Open-Circuit

When one phase is open-circuit in the 9-phase VSI the machine can still operate while the other two phases in the faulty 3-winding set have 180° phase shift and higher phase currents than the healthy phases, as shown in Figure 5.19 (a) and Figure 5.19 (b). Due to the constrains that the phase currents should be lower than those under healthy condition the machine can operate at 1000 RPM and 1.8 Nm. DC-link capacitor current distortion and torque vibration are shown in Figure 5.19 (c).

5.6.4 One Set of Three Phase Winding Open-Circuit

The faulty 3-phase winding set can be disconnected from the system when there is a phase fault in this winding set, which can be a protection mechanism of sorts. The two healthy sets can still work and the machine can operate at 1000 RPM, 2.1 Nm, i.e. 2/3 of the healthy condition torque corresponding to the same phase current magnitude in the healthy winding sets with the healthy operating condition as shown in Figure 5.20 (a). No extra torque vibration is added compared with the healthy condition, as shown in Figure 5.20 (b). The machine is actually 2x 3-phase, or 6-phase machine.

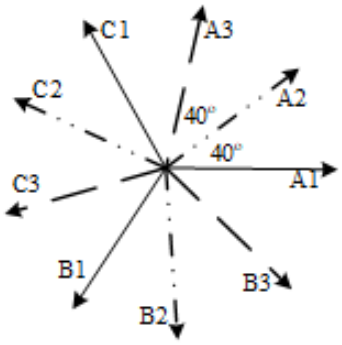
5.6.5 Two Sets of Three Phase Winding Open-Circuit

Similar with the previous condition, this operation is designed for severer fault conditions. The machine can operate at 1000 RPM and 1 Nm with the remaining working phases current, DC-link capacitor current and torque as shown in Figure 5.20 (c) and Figure 5.20 (d) respectively. This operating condition is the same with a 3-phase machine drive system.

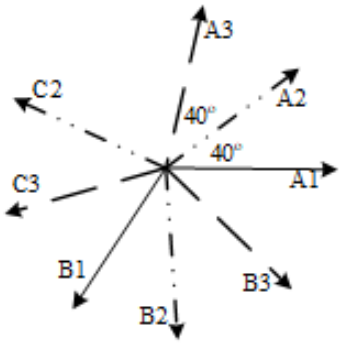
5.6.6 Evaluation and Comparison

The performances of different operating conditions are summarized in Table 5.8. These tests verify the fault tolerance capability and propose the protection mechanism (one or two sets of 3-phase windings open), for which the 9-phase machine with a 3x 3-phase winding configuration can still operate albeit with the torque output of a lower quality (one phase open) or lower torque output capabilities. This is to support the fault tolerance capability

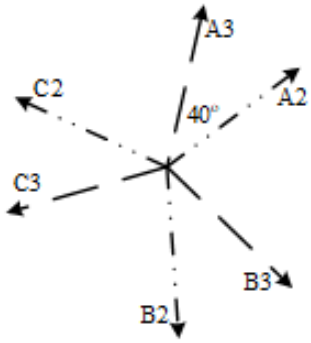
statement in the previous chapters. Another novelty to the thesis and another benefit of the multiphase traction system in EV application, which although not fully explored due to time constraints, form part of the author's future research interests.



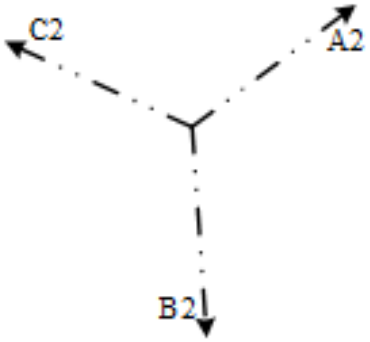
(a) Healthy condition.



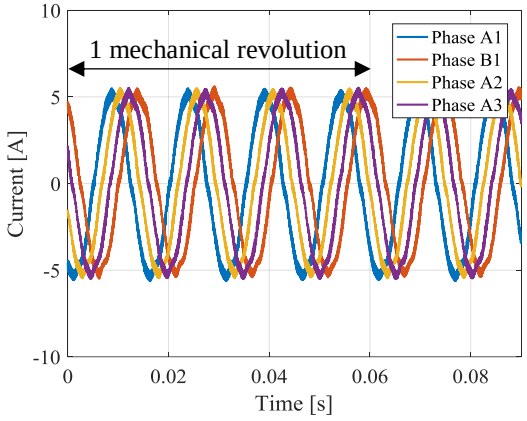
(b) One phase open condition.



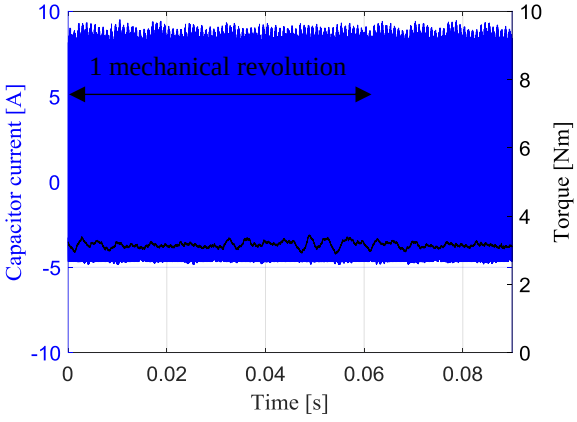
(c) One set of 3-phase winding open.



(d) Two sets of 3-phase windings open.

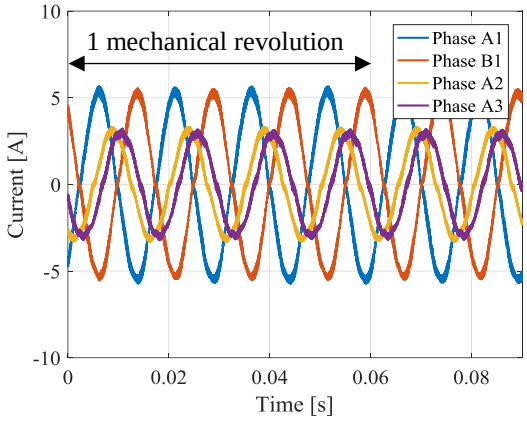


(e) Healthy condition phase currents.

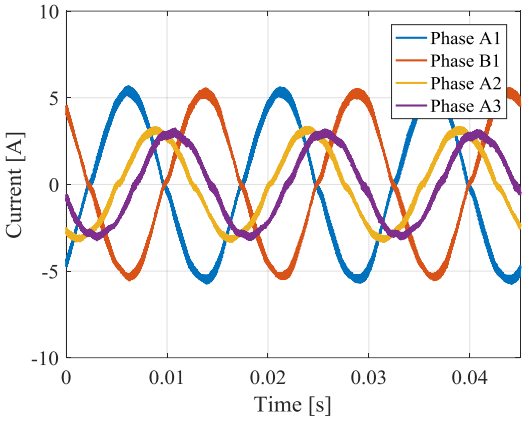


(f) Healthy condition DC cap current and torque.

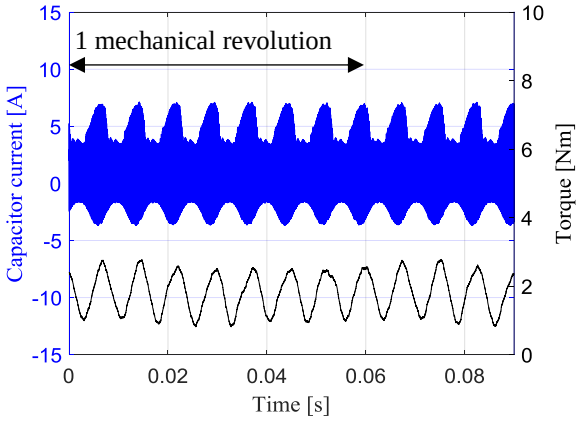
Figure 5.18 Operating conditions and healthy condition test results.



(a) Phase currents over one mechanical cycle.

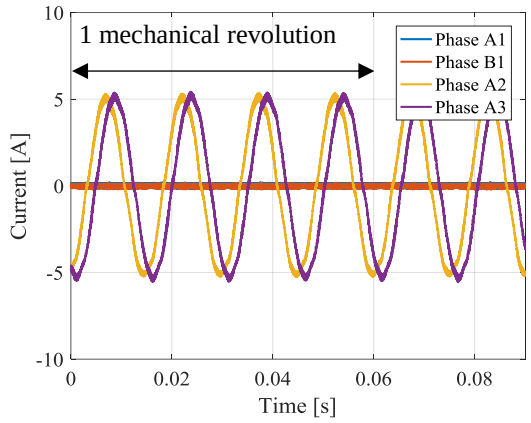


(b) Phase current detail.

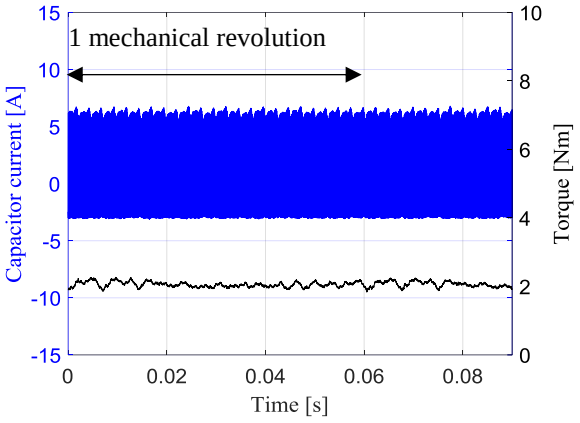


(c) DC-link cap current and torque.

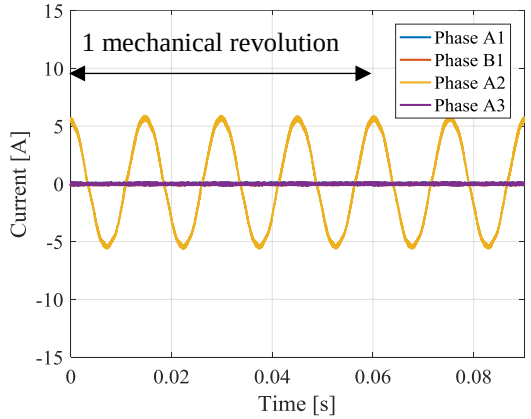
Figure 5.19 One phase open condition test results.



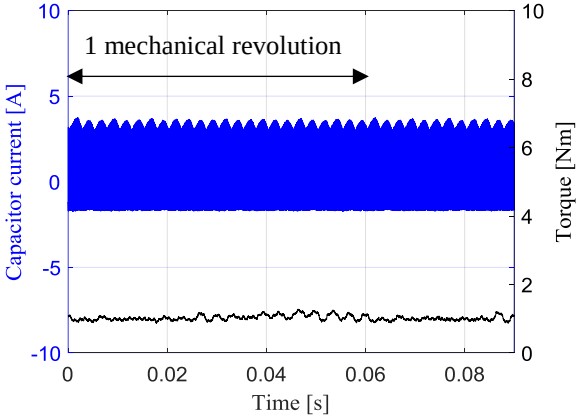
(a) Phase currents over one mechanical cycle (one set open).



(b) DC-link cap current and torque (one set open).



(c) Phase currents over one mechanical cycle (one set open).



(d) DC-link cap current and torque (one set open).

Figure 5.20 One and two sets of 3-phase windings open condition test results.

Table 5.8 Comparison of results for healthy and chosen fault conditions at 1000 rpm.

Conditions	Current (Arms)					Torque (Nm)
	Phase A1	Phase B1	Phase A2	Phase A3	DC-link Cap RMS current	
Healthy	3.7	3.7	3.7	3.7	5.2	3.1
One phase open	3.7	3.7	2.2	2.2	2.8	1.8
One set open	0	0	3.7	3.7	3.4	2.1
Two sets open	0	0	3.7	0	1.9	1

5.7 Summary

In this chapter, an experiment test facility is reported that is designed containing the 3- and 9-phase VSIs and configurable 3- and 9-phase BLPM machine. The experimental facility is used for validation of Chapter 3, the switching strategy study for multiphase machine drive systems.

The method is explained to validate the DC-link capacitor investigation in Chapter 4 and support the VSI DC-link capacitor redesign section in Chapter 6.

The investigation method of DC-link capacitor requirements in Chapter 4 is validated via the equitable power output 3- and 9-phase VSIs. The analytical study in Chapter 4 proposed the solution with the best performance among all the 3- and 9-phase VSIs, the 3x 3-phase SVM group based interleaved triangular carrier waveform VSI having 1/3 DC-link capacitor RMS current rating and approximate 1/2 DC-link capacitance of its 3-phase counterpart. These are validated in this chapter. In the EV traction machine drive VSIs, the capacitor volume is proportional to the RMS current rating. Therefore, the 3x 3-phase VSI has a DC-link capacitor 1/3 volume of its 3-phase counterpart. Consequently, the implementation of multiphase system significantly reduces the DC-link capacitor sizes and hence increases the system power density. Based on the analytical study and experimental validation the generalized DC-link capacitor design procedure is proposed for arbitrary phase number and flexible configuration VSIs.

As in the previous chapters, the fault tolerance capability of the multiphase machine is briefly studied via faulty tests conducted on one type of 9-phase machine drive system, a 3x 3-phase machine drive system. Although some publications discuss fault tolerance, the phenomenon of the faulty condition and the corresponding operating performances are not studied yet for a 3x 3-phase topology, not to mention the protection mechanisms – one or two sets of healthy 3-phase windings sill functioned.

Chapter 6

Thermal Design of Multiphase VSIs

6.1 Introduction

The power electronics converter (PEC) thermal performance is critically important because it determines the heat generation and transfer from the power switch and diode dies (the electrical function part of semiconductor devices such as IGBTs, MOSFETs, diodes, etc.) hence their temperature. The die operating temperature and its variation determine the device life time [159], [160].

In some high power and high current voltage source inverters (VSIs) applications, each of the power devices, i.e. IGBTs, MOSFETs and diodes, is composed of parallel-connected multiple dies to achieve high current capacity, which can result in the unequal current share and hence unequal heat generation and temperature among these dies. In this chapter, the investigation focuses on the thermal performance improvement and design flexibility with the implementation of multiphase VSIs. Assuming that the VSI controls sinusoidal phase current driving brushless permanent magnet (BLPM) machine with sinusoidal phase back-EMFs, the inverter Volt-Ampere rating and hence total required silicon volume is theoretically independent of the system phase number [39].

The mechanism of the current imbalance, its consequences, and solutions are studied and proposed, which is followed by the multiphase VSI solution investigation. The finite element analysis (FEA) thermal model is built for the 3-phase Nissan Leaf 2012 traction machine drive system VSI – the benchmark and its simulation results are compared with the published data to validate its consistency with the real experiment condition. Based on the model, the thermal performance is firstly studied and compared under different dies power loss imbalances conditions. That is compared with the newly proposed 9-phase

conventional design VSI, which nearly does not have the power loss imbalance problem due to the non-parallel connection of IGBT dies and individual current control for each phase, each die. The 9-, 18-, 27- and 36-phase integrated design VSIs are also proposed. Better thermal performance can be achieved via the implementation of multiphase VSIs. The decreased DC-link capacitor volume (from the Chapter 4 and 5) and multiphase integrated design both increased the VSI compactness.

Other methodologies based on lumped parameter modelling are also used for converters thermal design. The lumped modelling simplifies the thermal network into the combination of basic elements – thermal resistance and capacitance to model the heat transfer. Only the FEA modelling based methodology is applied here and implemented via the software Ansys Icepak.

6.2 Current Sharing in Parallel-Connected Dies

The power switches (both discrete devices and dies), i.e. IGBT, MOSFET, and diode etc., are connected in series or parallel to achieve the high voltage or high current capability, which meanwhile brings unequal voltage distribution or imbalanced current sharing on different switches. This is due to the power semiconductor devices tolerance, driver variations, asymmetric parasitic in power and driver circuits, etc. [161] Under those unequal or imbalanced conditions some individual switch could exceed its ratings, hence cause the failure and even the cascaded failure of the other switches and the whole system [161]. Two level VSIs, in terms of the voltage level, are eligible and normally applied for the traction system VSI in most EV applications (not very high voltage and high current), as a result, power device paralleling problems (other than series connection problems) and solutions are reviewed and studied here.

6.2.1 Current Imbalances and Consequences

The main contributions for the steady state current imbalance include [89], [161]–[164]:

- Output characteristics variation
- Different junction temperatures
- Commutation loop resistance discrepancy etc.

The main causes for the dynamic current mismatch include [89], [161]–[164]:

- Different transfer characteristics (Not for diodes)
- Gate resistance and gate driver variations (Not for diodes)
- Asymmetrical parasitic and electromagnetic coupling in power and driver circuits (due to the geometry design) etc.

The steady state and dynamic current imbalances are studied here with the parallel-connected discrete IGBT switches or dies as examples, with which the parallel-connected MOSFETs and diodes current imbalance has the same mechanism and are not discussed here.

Different IGBT output characteristics with different saturated collector-to-emitter voltages result in the different IGBT currents under the same IGBT voltage among the paralleled IGBTs, the steady state current imbalance [165].

According to [166] the temperature variation causes the different IGBT output characteristics as well and most manufactured IGBTs of the latest technologies have the positive temperature coefficient characterization as in [166], which can alleviate the current and power loss imbalances hence the temperature discrepancy among different paralleled IGBTs (dies, discrete devices or power modules), reversely benefit the current sharing balance [163], [167].

The IGBT transfer characteristics, the relation between gate-to-emitter voltage and the IGBT current, affects the switching transient and hence their differences result in the current imbalance [162]. Furthermore, the transfer characteristics are temperature dependent [166].

In the application of the discrete packaged IGBTs the loop asymmetry is dependent on the power circuitry layout and geometry, e.g. printed circuit board (PCB) design, bus bar design etc., and in the IGBT modules it relates to the packaging design, the layout of direct bonded copper (DBC), bondings, dies, etc. These lead to the not even distributed parasitic hence the current imbalances. The parasitic impedances equivalent circuitry of each die emitters and their coupling with the corresponding gate circuits for a lower switch with 3 parallel dies in the IGBT power module EUPEC 1200 V/450 A are illustrated and discussed in [168]. The pulse test simulation shows the resulting deviation in the individual gate signals, voltage and current during switching transients. The higher current frequency results in the severer current imbalance, which is both analyzed and validated by 3D FEA model and experimental tests [169].

The simulation based research (the electrical analytical model with parameters from Q3D parasitic extraction and the FEA thermal model) on two different packaging types of 600 V/300 A IGBT modules (three dies in parallel for one IGBT switch) in paper [170] shows the current sharing, power loss distribution and die chip temperature distribution imbalances. The imbalance is due to the module internal electromagnetic and thermal

characteristics. Under the operation condition of 300 V DC-link voltage, 300 A load current, 10 kHz switching frequency and 55% duty cycle, the maximum temperature rise gap between two dies is 11.6 °C in type A package, accounting for approximate 50% of the average temperature rise, and 7 °C in type B package [170].

High voltage and high current IGBT modules (1.7 kV/2400 A or 3.3 kV/1200 A) with 6 parallel-connected IGBT dies per switch is investigated via simulations and experiments showing the maximum individual die peak current 190 A and minimum value 120 A during the switching on transient [171].

More detailed Q3D parasitic extraction is presented in [172], [173] considering the skin effect, proximity effect and eddy current in the module DCB layer. Another megawatt scale level IGBT module (1.7 kV/1 kA) with 6 IGBT dies in parallel connection per switch is also investigated using the same method with [170] under both simulation and experimental test in paper [174]. The total power losses containing switching and conduction losses of different IGBT dies are compared under the test condition of 10 kHz switching frequency, 50% duty cycle, 700 V collector emitter voltage and 650 A conduction current. The results demonstrate that the IGBT die with the maximum power loss has 230 W more than the least power loss IGBT die, accounting for 50% of its power dissipation [174] and the higher switching frequency results in higher power loss differences, also concluded in [169]. As the test current 650 A is below the device current rating, the power loss deviation will be enlarged under the rated current, 1 kA.

Moreover, the switch-on current sharing mismatch in parallel connected dies in IGBT module is studied under the discrepancies of gate resistance, gate-emitter capacitor and propagation gate driver signal delay time [175]. Besides the parallel connection of IGBT die chips in IGBT modules, designs of parallel-connected IGBT modules are implemented for the increased current rating requirement in power converters and the analysis principles are similar with those of parallel-connected dies. The thermal imbalance of parallel-connected IGBT modules also result in current imbalance under both on-state and switching transient, and the current imbalance will lead to the thermal imbalance vice versa [176].

The basic consequence of the current imbalance in parallel-connected semiconductor power devices is that some devices could work under their current ratings while the others over the current ratings. Besides that, according to the relation among operating temperatures, aging effects, fatigue degrees, the resulting parameter variations, and the lifetime [159], [160], [177], [178], different die power losses result in different die operating temperatures and die temperature variations. This leads to different thermal mechanical stresses hence the different aging effects and fatigue conditions (resulting in different junction to case thermal resistance and on-state resistance) reversely enlarging the die temperature imbalance, the circle with detrimental influences. As a result, the parallel-connected semiconductor power devices will have different lifetime, not fully using of all their lifetime.

6.2.2 Solutions

The existing solutions for the current imbalance and its consequences include the parallel devices de-rating, the active gate drive control, the geometry and cooling design optimization, etc., [161] besides which the implementation of multiphase systems can also alleviate and even eliminate the current imbalance problems [179].

The de-rating technique is based on the principle that the current mismatch is acceptable provided that none of the paralleled IGBTs exceeds its ratings [161]. So the de-rating consideration contains safe operating area (SOA) and the parallel-connected IGBTs thermal de-rating [167].

Under steady state the de-rating factor indicating the effective current capability reduction is defined as [165]:

$$\delta_d = 1 - \frac{I_{total}}{n_{para} I_{rated}} \tag{6.1}$$

where δ_d - derating factor under steady state, I_{total} - total current acceptable for the parallel combination of IGBTs, I_{rated} - single IGBT rating and n_{para} - number of IGBTs in parallel.

Under steady state the mismatch factor is defined as the maximum current compared to the minimum current [165]:

$$m_{mis} = \frac{I_{rated} - I_{\min}}{I_{rated}} \tag{6.2}$$

where m_{mis} - mismatch factor under steady state and I_{min} - minimum current of a single IGBT in parallel operation.

Under dynamic state the current mis-sharing factor is defined [165]:

$$m_{mis\_d} = \frac{I_{peak\_\max} - I_{peak\_\min}}{I_{Peak\_\max}} \tag{6.3}$$

where m_{mis_d} - mis-sharing factor under dynamic state, I_{peak_max} - maximum peak current for a single IGBT and I_{peak_min} - minimum peak current through a single IGBT in parallel operation.

Under dynamic state the de-rating factor is defined [165]:

$$\delta_{d\_d} = 1 - \frac{\left(n_{para} - 1\right)\left(1 - m_{mis\_d}\right) + 1}{n_{para}} \tag{6.4}$$

where δ_{d_d} - dynamic de-rating factor.

The relation between the number of parallel-connected devices and the corresponding de-rating factor dependent of static, dynamic current sharing, thermal stability and external circuit is discussed in [161] suggesting the derating factors of parallel-connected IGBT modules under the certain operating condition. Mitsubishi Electric's policy constrains the variation of collector-to-emitter saturated voltage, the key parameter for steady-state current imbalance, within 0.3V under the same production rank and guarantees the up to 15% current imbalance for two parallel-connected IGBT modules [180]. ABB also publishes a 6500 V/600 A IGBT module parameter spread based on statistical analysis of one year production [167].

In terms of IGBT and diode dies parameter variation the statistical result is provided by Vinotech on the collector-to-emitter voltage spread from 40 thousand module samples with Infineon IGBT3 low loss IGBTs and Emcon HE fast recovery epitaxial diodes (FREDs) dies. The result shows that the saturated collector-to-emitter voltage of 99.99 % IGBTs do not vary above 310 mV at 25 °C and 450 mV at 125 °C, and for freewheeling diodes these values are 400 mV and 490 mV respectively, both causing conduction losses deviation. The distributions of the IGBT and diode voltage spread under 25 °C typical operating point are illustrated in [181], based on which 99.99 % IGBTs require 13 % current rating reduction and 99.99 % diodes require 25 % current rating reduction. Besides that, the switching loss deviation among different devices is within 10 to 15 % when the gate driver is properly designed [181].

The de-rating factor is dependent on both the number of paralleled IGBTs and the operating conditions, e.g. switching frequency, load current and junction or ambient temperature. Although it is very hard to find the suggested de-rating factors from the academic research or industrial practice except the report [181], the current and power loss imbalances discussed before do suggest the necessity for the de-rating consideration.

An active gate signal control scenario via gate signal delay-time compensation for parallel-connected IGBTs is proposed in paper [182] and the current imbalance can be constrained effectively under different operating points. The gate resistance dynamic control, having the equivalent effects with changing the gate timing, is presented and validated experimentally, which can improve the switching-on and switching-off current balances by 71% and 77% for the maximum current imbalance and 74% and 65% for the averaged current imbalance [183]. Two other current balance strategies are proposed in [184]. Although the switching-on and switching-off current imbalances cannot be alleviated specifically, the overall current balance improvements can be achieved via the control of the gate voltage with the feedback of average current through different IGBTs in parallel or the corresponding IGBT current and the other IGBT current – current cross reference strategy [184].

The paper [185] discusses the causes of transient current imbalances in high power IGBT module (EUPEC 1200V/450A FS450R12KE3) via the partial element equivalent circuit model considering skin and proximity effects and presents the switching transient current balance improvement via the optimization of the gate circuit geometry. The dies layout, DBC geometry optimization, and the newly employed pin fin cooling system in IGBT power module are conducted and simulated via Q3D, thermal FEA and analytical models giving the improved current and temperature balance on IGBT junctions, which is also validated via experimental tests [186].

Although various solutions can be considered, the de-rating design decreases the use of the semiconductor materials, and cannot fully use the parallel-connected devices lifetime, the active gate drive control results in more complex circuitry and control, and the geometry and cooling design optimization can only alleviate the imbalances to some extent and is application specific. While the implementation of the multiphase system can highly alleviate the current and power loss imbalance by dividing the total power to more individually controlled phases. As a result, less parallel or even non-parallel power device connections can be achieved with only limited modification based on the existing 3-phase VSIs, and hence the degradation and fatigue degrees of power devices are more even resulting in the improved use of their lifetime. The implementation of multiphase VSI and the resulting performance improvement are studied in the following sections comparing with the 3-phase benchmark.

6.3 Benchmark VSI Study and Modelling

6.3.1 System Overview and Specifications

The Nissan Leaf 2012 traction machine drive system is selected as the benchmark, one typical 3-phase system with a VSI (with the specification shown in Table 6.1) and a 3-phase 8 pole interior permanent magnet machine (IPM) with the peak output torque 280 Nm and the rated speed 10,390 rpm [11]. All the machine drive system specifications, test conditions and results are from the publications of Oak Ridge National Laboratory (ORNL) and National Renewable Energy Laboratory (NREL) [7], [11], [187]–[192]. The machine drive system diagram is shown in Figure 6.1 (a) that the on-board battery pack is connected to the VSI via relays and pre-charge resistor, and the 3-phase machine is connected to the VSI. The size and weight of the power converter unit, the VSI, are labeled in Figure 6.1 (b).

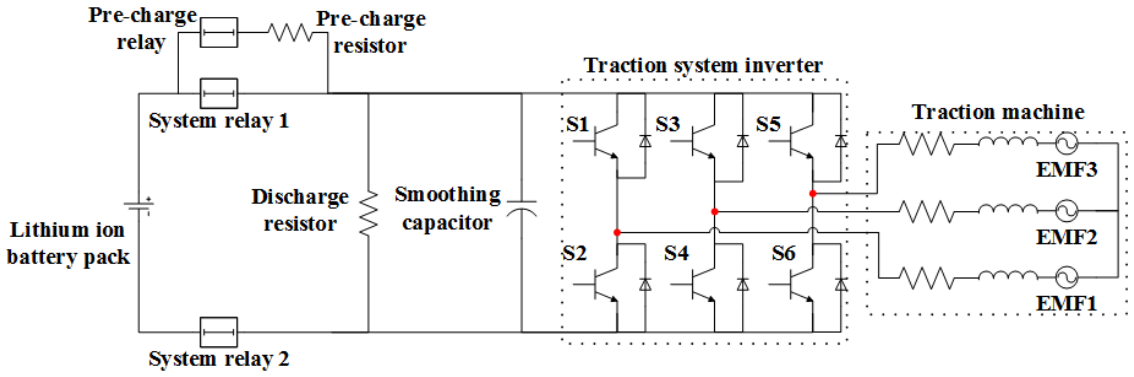
The VSI assemblies are shown in Figure 6.2, among which Figure 6.2 (a) shows the overview of the inverter, Figure 6.2 (b) shows the IGBT and IGBT driver board sizes, Figure 6.2 (c) shows the DC-link capacitor size, Figure 6.2 (d) shows the X-ray inside view of the DC-link capacitor containing capacitor, small capacitor, thermistor and connector, Figure 6.2 (e) shows the mounting of the IGBT on the heatsink, and Figure 6.2 (f) shows the VSI liquid cooling heatsink composed of couples of paralleled serpentine-finned channels.

Each IGBT module composes one VSI phase leg as shown in Figure 6.3 (a), where there are upper and lower switches, and their corresponding freewheeling diodes as illustrated in Figure 6.3 (b). Each switch is composed of three parallel connecting switch dies, and three parallel connecting diode dies compose one freewheeling diode. The switch and diode die chip sizes are shown in Table 6.1 and Figure 6.4 shows the vertical view of the IGBT module [187].

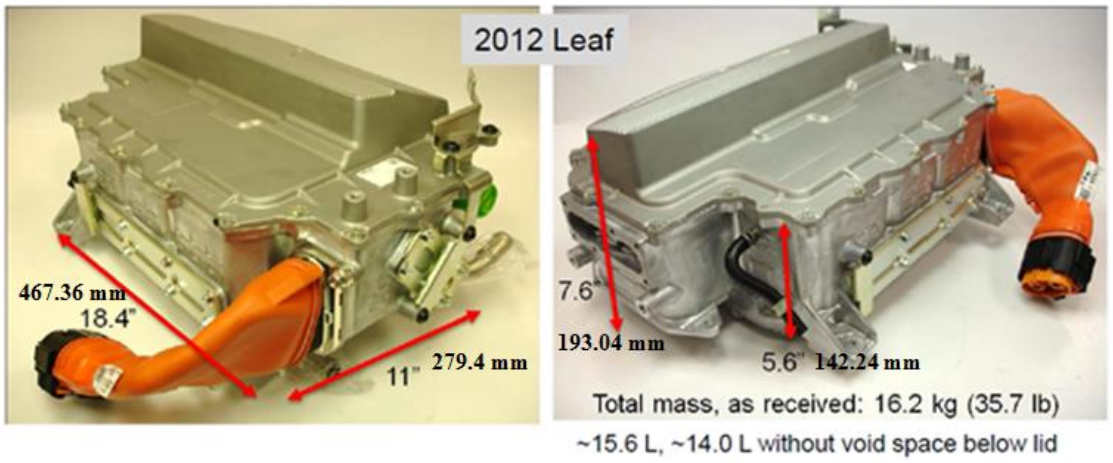
The layout and thickness of each layers of IGBT and diode dies are shown in Figure 6.5 and their thermal conductivities are shown in Table 6.2 in which the temperature dependency is negligible under the IGBT operating temperature here.

Table 6.1 VSI specifications and test conditions [11].

Inverter overview	Rated power (kW)	80
	Peak power density (kW/L)	5.7
	Peak specific power(kW/kg)	4.9
	DC-link voltage (V) - test condition	375
	Switching frequency (kHz)	5
	Efficiency under high speed (%)	99
DC-link	Capacitance (μF) - big capacitor	1186.5
	Rated voltage (V) - big capacitor	600
	Capacitance (μF) - small capacitor	1.13
	Rated voltage (V) - small capacitor	600
	DC-link bleed resistor 61 kΩ, 15 Watt	
Conductors	Input side DC cables	1/0 AWG
	Output side AC cables	3/0 AWG
IGBT	Breakdown voltage (V)	1000
	Rated current per die chip (A)	300
	Parallel connected die chip number per switch	3
	Die chip size (mm)	15 X 15
	Die chip thickness (mm)	0.361
Diode	Breakdown voltage (V)	1000
	Rated current per die chip (A)	300
	Parallel connected die chip number per diode	3
	Die chip size (mm)	14 X 14
	Die chip thickness (mm)	0.25
Cooling system	Coolant type	water ethylene glycol
	Coolant input temperature (°C) - test condition	65
	Coolant flow rate (litre per minute - lpm)	10

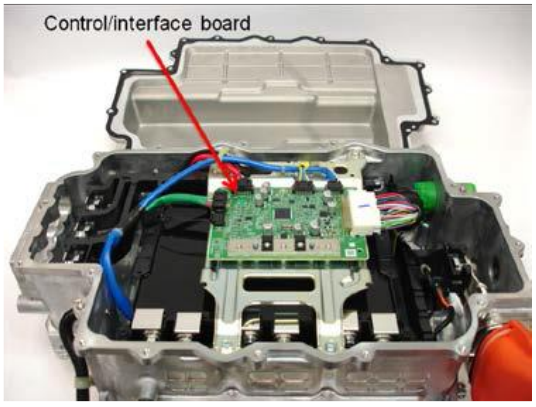


(a) Benchmark traction system diagram [193].

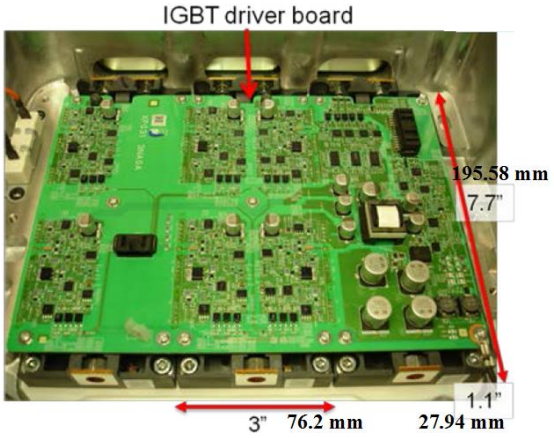


(b) VSI [11]. Note, the author thanks Dr. T. Burress for permission to use this material.

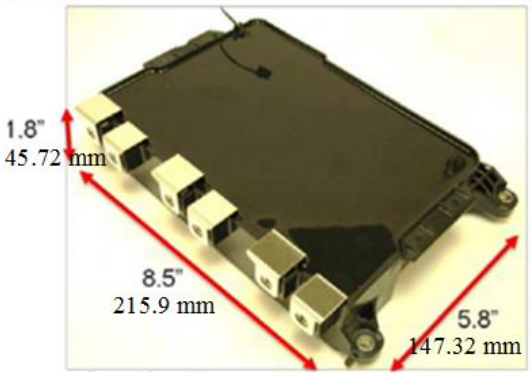
Figure 6.1 2012 Nissan Leaf traction machine drive system.



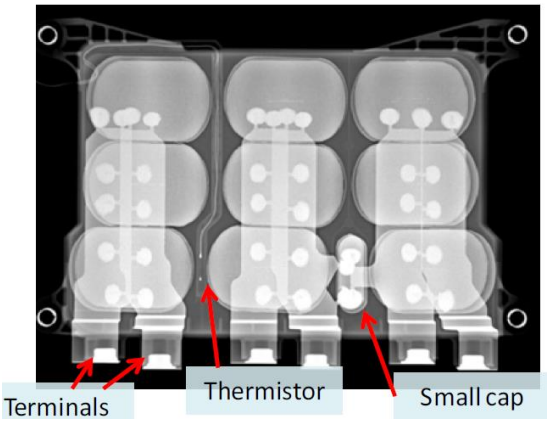
(a) Inverter overview.



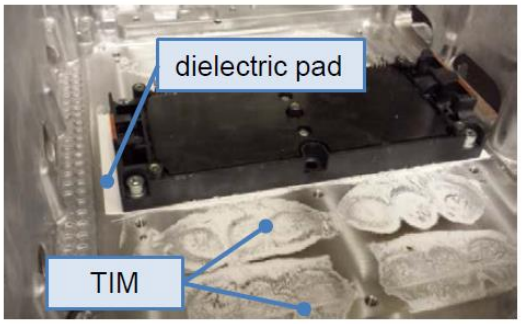
(b) IGBT module and driver.



(c) DC-link capacitor.



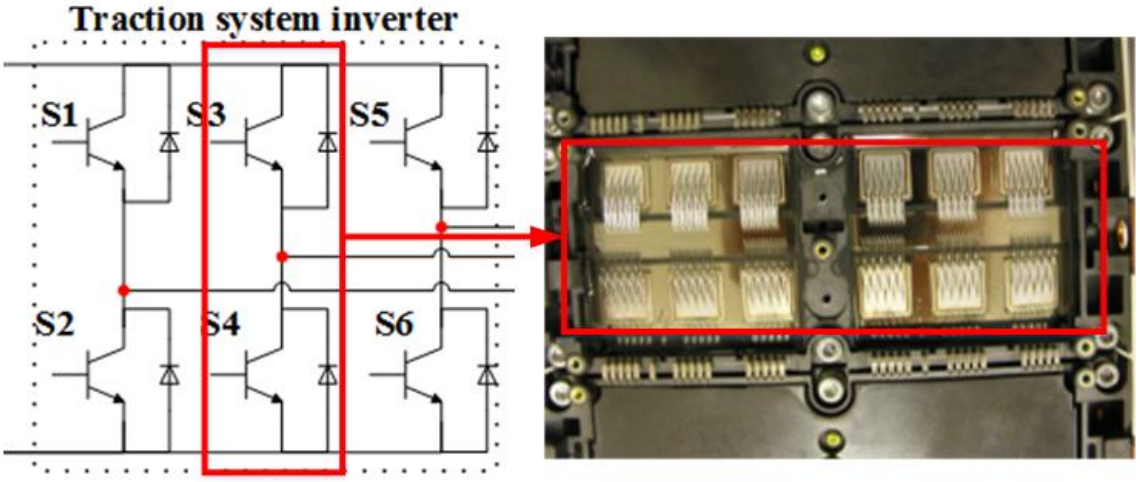
(d) X-ray view of DC-link capacitor.



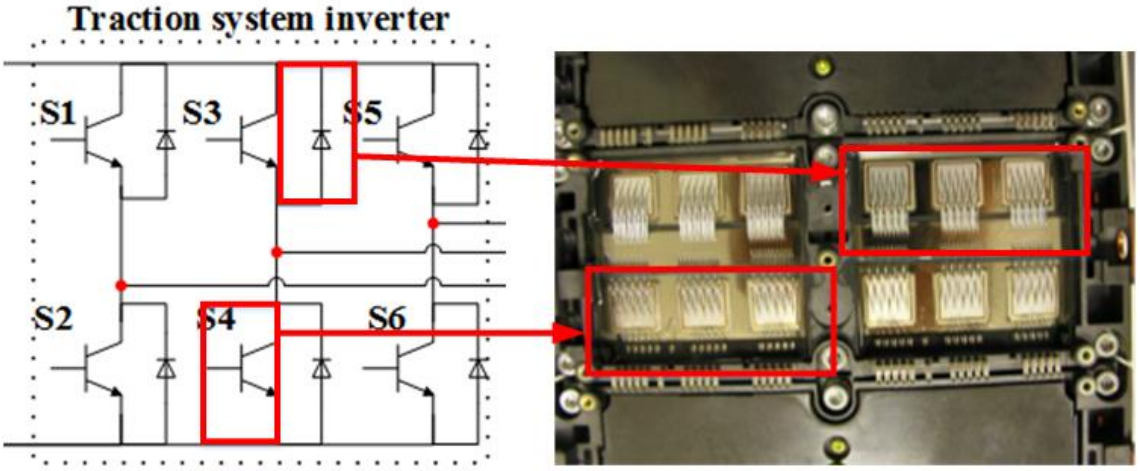
(e) IGBT module mounting.

(f) VSI liquid cooling system.

Figure 6.2 2012 Nissan Leaf VSI assemblies and components [11]. Note, the author thanks Dr. T. Burress for permission to use this material.



(a) VSI phase leg and the corresponding IGBT module.



(b) Inverter switch and diode demonstration.

Figure 6.3 2012 Nissan Leaf VSI IGBT module [11]. Note, the author thanks Dr. T. Burress for permission to use this material.

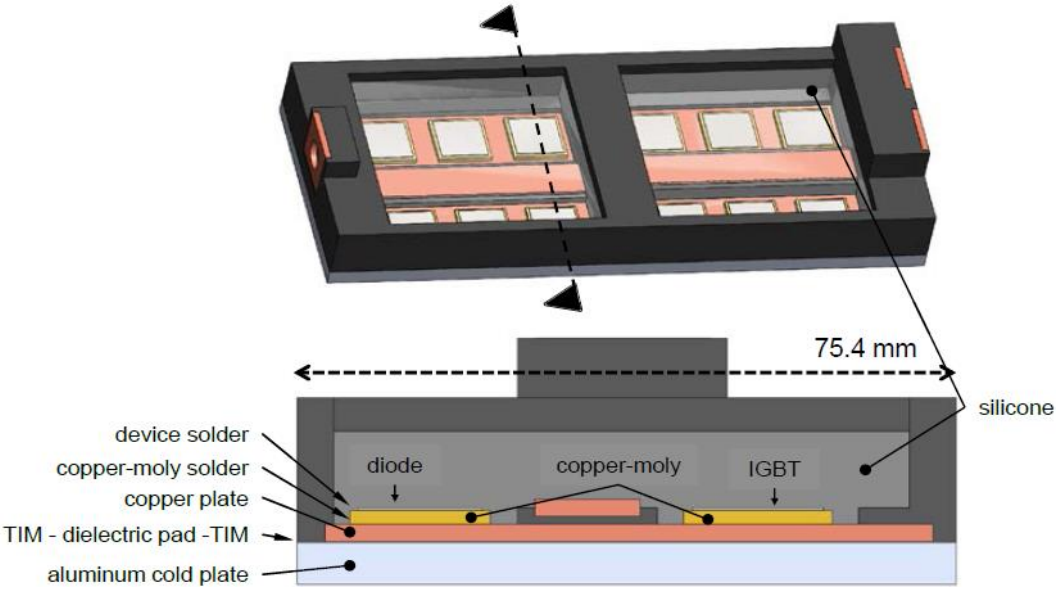
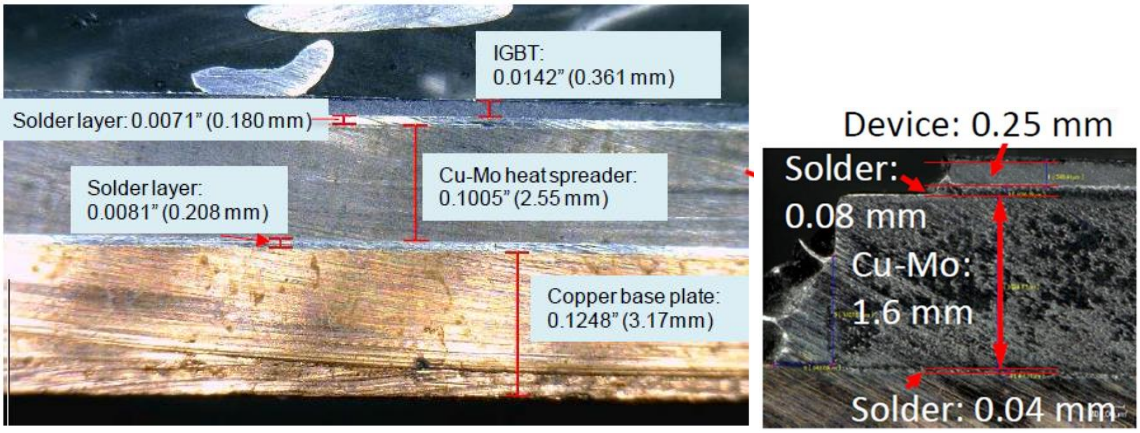


Figure 6.4 Cross-sectional view of IGBT used in Nissan Leaf EV VSI [189]. Note, the author thanks Dr. T. Burress for permission to use this material.



(a) IGBT die. (b) diode die.

Figure 6.5 Thickness of different IGBT and diode die layers [11], [188]. Note, the author thanks Dr. T. Burress for permission to use this material.

IGBT switch junction-to-coolant specific thermal resistances versus different coolant flow rates are given in Figure 6.6 containing both the experimental results and simulation results. These results will be compared with the results from the built FEA model in the following content for the modelling consistency (with the published experiment data) validation (test condition: 50 A current through and approximate 55 W power loss). Figure 6.7 demonstrates the temperature drop through the thermal path composed of different IGBT layers under one operating condition, in which the thermal interface material (TIM) and the dielectric pad have the highest thermal resistance withholding the highest temperature drop among all the layers while the temperature drops of both solder layers are much smaller compared with the others.

The inverter efficiency contour under different operation conditions is shown in Figure 6.8 and the machine drive system (both the VSI and the machine) efficiency contour is shown in Figure 6.9. Extracted from the contours, the machine drive system power outputs, machine drive system and VSI efficiencies and VSI power losses under some representative discrete operating points are shown in Figure 6.10 and Figure 6.11. Some operating points will be compared with the simulation results in Chapter 5.3.2.1 for power loss modelling consistency (with the published experiment data) validation purpose.

Table 6.2 Thermal conductivities of different IGBT and diode die layer materials [191].

Material	Thermal conductivity (W/m-K)
Silicon	180
Copper-moly (20-80)	164
Copper	195
Dielectric pad	2.6
Aluminum	167
TIM	1
Solder	35

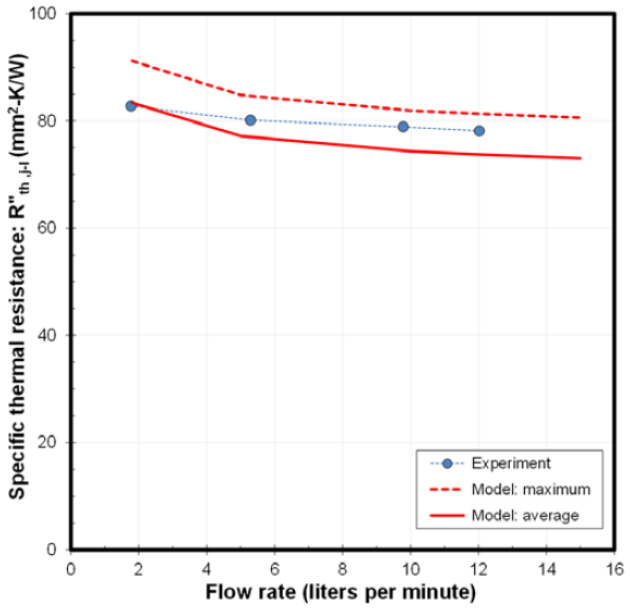


Figure 6.6 The IGBT junction-to-coolant specific thermal resistance versus coolant flow rate [187]. Note, the author thanks Dr. T. Burress for permission to use this material.

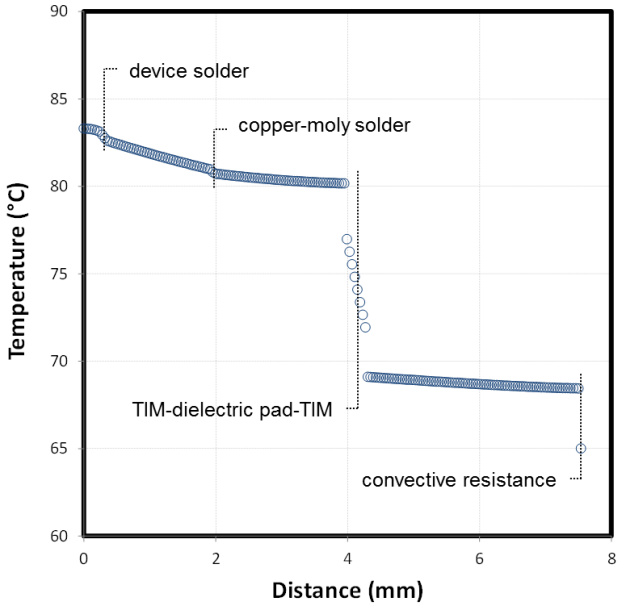


Figure 6.7 The demonstrated temperature drop of the thermal path of different IGBT layers [7]. Note, the author thanks Dr. T. Burress for permission to use this material.

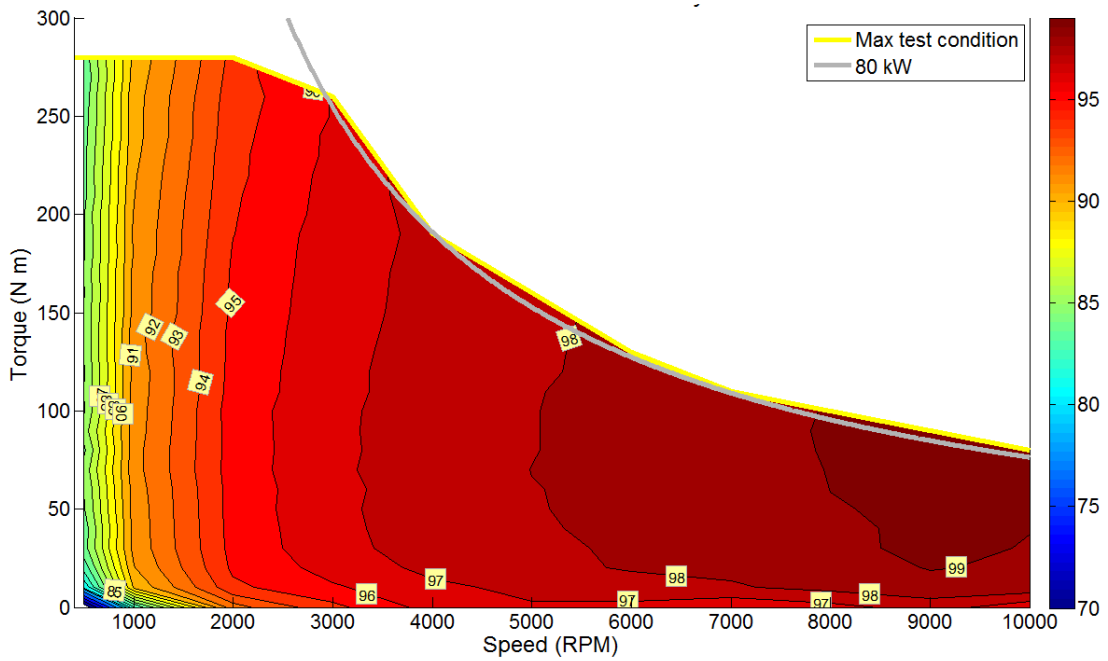


Figure 6.8 Nissan Leaf VSI efficiency contour [11]. Note, the author thanks Dr. T. Burress for permission to use this material.

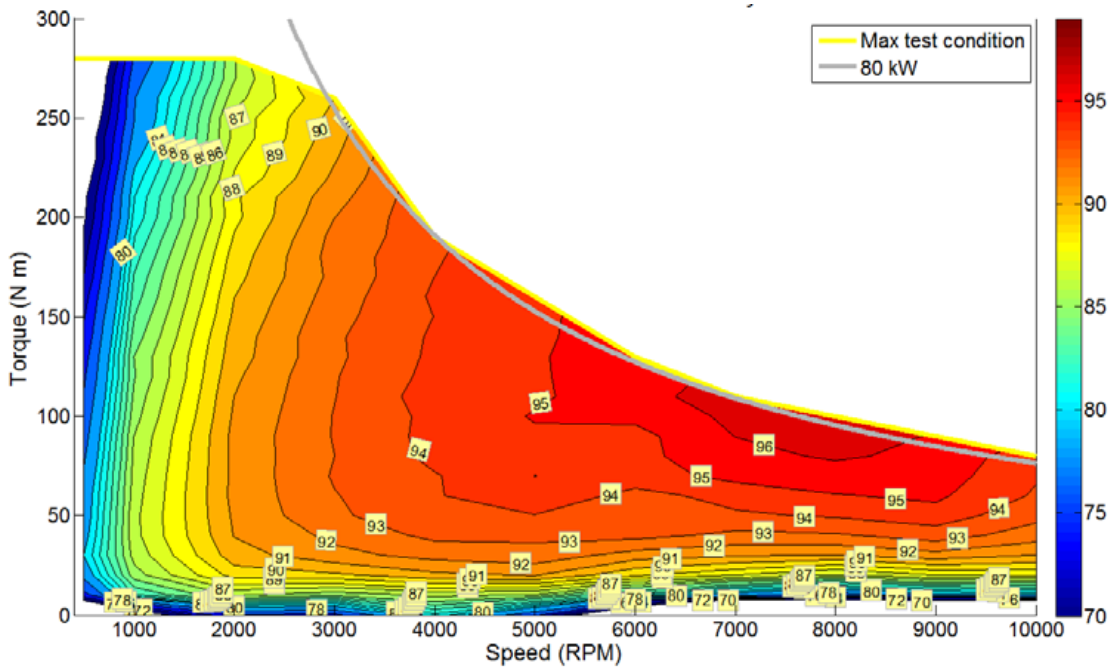


Figure 6.9 Nissan Leaf machine drive system efficiency contour [11]. Note, the author thanks Dr. T. Burress for permission to use this material.

Torque (N.m)																						
280	NA	29322	43982	58643	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
275	NA	28798	43197	57596	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
250	NA	26180	39270	52360	65450	78540	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
225	NA	23562	35343	47124	58905	70686	82467	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
200	10472	20944	31416	41888	52360	62832	73304	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
175	9163	18326	27489	36652	45815	54978	64141	73304	82467	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
150	7854	15708	23562	31416	39270	47124	54978	62832	70686	78540	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
125	6545	13090	19635	26180	32725	39270	45815	52360	58905	65450	71995	78540	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
100	5236	10472	15708	20944	26180	31416	36652	41888	47124	52360	57596	62832	68068	73304	78540	83776	NA	NA	NA	NA	NA	NA
75	3927	7854	11781	15708	19635	23562	27489	31416	35343	39270	43197	47124	51051	54978	58905	62832	66759	70686	74613	78540		
50	2618	5236	7854	10472	13090	15708	18326	20944	23562	26180	28798	31416	34034	36652	39270	41888	44506	47124	49742	52360		
25	1309	2618	3927	5236	6545	7854	9163	10472	11781	13090	14399	15708	17017	18326	19635	20944	22253	23562	24871	26180		
Speed (rpm)	0	500	1000	1500	2000	2500	3000	3500	4000	4500	5000	5500	6000	6500	7000	7500	8000	8500	9000	9500	10000	

(a) Machine drive power output under different torque versus speed operating points.

Torque (N.m)																						
280	NA	78%	80%	85%	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
275	NA	78%	82%	85%	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
250	NA	78%	83%	87%	88%	90%	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
225	NA	79%	83%	87%	89%	91%	92%	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
200	74%	81%	85%	88%	90%	91%	92%	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
175	75%	82%	86%	89%	90%	92%	93%	93%	94%	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
150	76%	83%	87%	90%	91%	92%	93%	94%	94%	94%	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
125	77%	84%	87%	90%	91%	92%	93%	94%	94%	94%	95%	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
100	78%	85%	88%	91%	92%	93%	93%	94%	94%	95%	95%	95%	96%	96%	96%	NA	NA	NA	NA	NA	NA	NA
75	79%	86%	88%	91%	92%	93%	93%	94%	94%	94%	94%	95%	95%	95%	95%	95%	95%	95%	94%	94%		
50	79%	86%	88%	91%	92%	92%	93%	93%	93%	93%	93%	93%	93%	93%	94%	94%	94%	94%	94%	93%		
25	79%	86%	88%	90%	90%	91%	91%	91%	91%	91%	91%	90%	90%	90%	90%	90%	90%	89%	90%	90%		
Speed (rpm)	0	500	1000	1500	2000	2500	3000	3500	4000	4500	5000	5500	6000	6500	7000	7500	8000	8500	9000	9500	10000	

(b) Machine drive efficiency under different torque versus speed operating points.

Figure 6.10 Machine drive outputs and efficiency.

Torque (N.m)																					
280	NA	90%	92%	94%	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
275	85%	90%	92%	94%	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
250	85%	90%	92%	94%	95%	96%	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
225	85%	90%	92%	94%	95%	96%	96%	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
200	85%	90%	92%	94%	95%	96%	96%	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
175	86%	91%	93%	95%	95%	96%	96%	97%	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
150	86%	91%	93%	95%	95%	96%	96%	97%	97%	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
125	86%	91%	93%	95%	96%	96%	97%	97%	97%	98%	98%	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
100	86%	91%	93%	95%	96%	96%	97%	97%	97%	98%	98%	98%	98%	98%	99%	NA	NA	NA	NA	NA	NA
75	86%	91%	93%	95%	96%	96%	97%	97%	97%	98%	98%	98%	98%	98%	99%	99%	99%	99%	99%	99%	99%
50	85%	91%	93%	95%	96%	96%	97%	97%	97%	98%	98%	98%	98%	98%	99%	99%	99%	99%	99%	99%	99%
25	84%	91%	93%	95%	95%	96%	96%	97%	97%	97%	98%	98%	98%	98%	98%	98%	99%	99%	99%	99%	98%
0	500	1000	1500	2000	2500	3000	3500	4000	4500	5000	5500	6000	6500	7000	7500	8000	8500	9000	9500	9500	10000
Speed (rpm)																					

(a) VSI efficiency under different torque versus speed operating points.

Torque (N.m)																					
280	NA	3759	4398	4140	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
275	NA	3692	4214	4066	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
250	NA	3356	3785	3611	3719	3491	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
225	NA	2983	3407	3250	3309	3107	3586	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
200	2123	2586	2957	2856	2909	2762	3187	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
175	1710	2011	2237	2059	2545	2390	2759	2365	2632	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
150	1447	1703	1896	1745	2158	2049	2365	2005	2256	2507	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
125	1190	1402	1580	1454	1438	1707	1478	1671	1880	2089	1516	1653	NA	NA	NA	NA	NA	NA	NA	NA	NA
100	940	1109	1249	1151	1138	1351	1182	1337	1504	1653	1213	1323	1433	1527	1636	873	NA	NA	NA	NA	NA
75	696	822	937	863	854	1013	887	1003	1128	1253	919	1003	1075	1157	1240	661	703	744	794	836	
50	497	548	625	575	569	683	591	676	760	845	619	676	732	788	836	891	473	501	535	563	
25	265	274	312	291	364	345	403	345	388	432	475	349	378	407	436	465	500	262	276	582	
0	500	1000	1500	2000	2500	3000	3500	4000	4500	5000	5500	6000	6500	7000	7500	8000	8500	9000	9500	10000	
Speed (rpm)																					

(b) VSI power losses under different torque versus speed operating points.

Figure 6.11 VSI efficiency and power losses.

6.3.2 System Modelling and Validation: IGBT Power Loss

The system thermal modelling can be categorized into two parts – the IGBT power losses modelling (based on the IGBT data sheet) and VSI FEA thermal modelling (using Ansys Ice Pak), both of which are validated by comparing with the results from ORNL and NREL. The accuracy and correctness of the modelling are the basis of the following investigations. To model the power losses, the detailed specification of the IGBT used in Nissan Leaf EV VSI is not accessible, and the Fuji Electric IGBT module 2MBI650VXA-170E-50 is selected (call Fuji IGBT in the following content) as shown in Figure 6.12. This is due to its similar match with the IGBT used in Nissan Leaf EV VSI on the geometry size, voltage and current ratings (as shown in Figure 6.13), IGBT switch power loss under 50 A constant current – 55 W [191], IGBT collector current vs. collector-emitter voltage, diode forward current vs. forward voltage, and the switching loss vs. collector current characteristics under typical conditions. Based on these, the IGBT switch and diode power losses under different Nissan Leaf representative operating points are calculated and compared with the results from the ORNL as shown in Table 6.3, for 4 different machine operating points are from [194], and both the VSI and machine drive system efficiencies are according to Figure 6.10 and Figure 6.11 .The power factors and modulation indexes are calculated on the basis of the assumption that both the phase voltage and current are sinusoidal. Hence, the phase 1 current, upper IGBT switch and diode currents, IGBT switching on/off losses, and diode reverse recovery losses can be simulated based on Fuji IGBT module specification at 150 °C as shown in Figure 6.14, Figure 6.15, Figure 6.16 and Figure 6.17. To simplify the power loss modelling, the total VSI power loss is the multiplication of the per IGBT switch and per diode losses, and the total IGBT and diode numbers, assuming that the power losses are balanced in IGBTs as well as diodes. The total power loss based on the Fuji IGBT specification and the results from ORNL are compared in Table 6.3, matching with each other in spite of some acceptable and negligible errors, within 10 %.

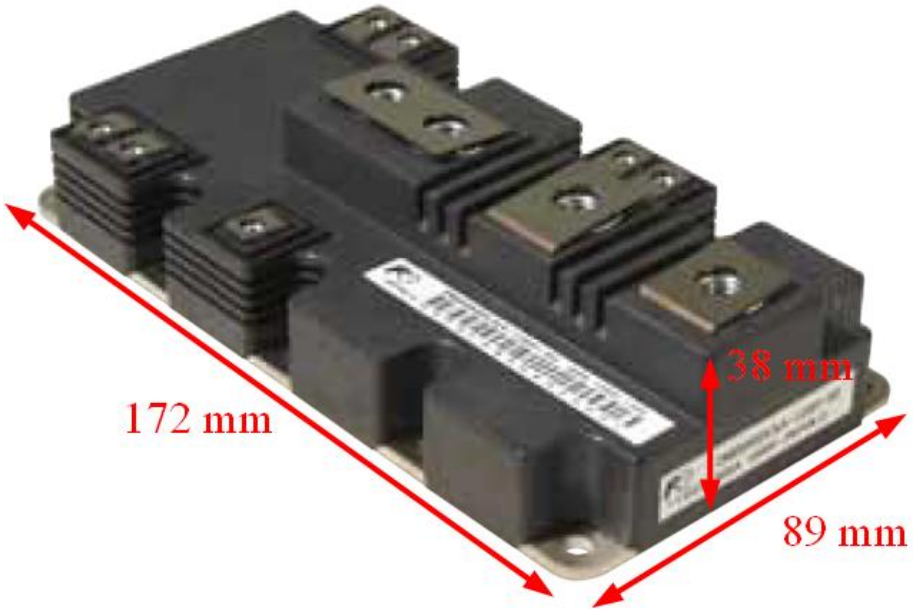


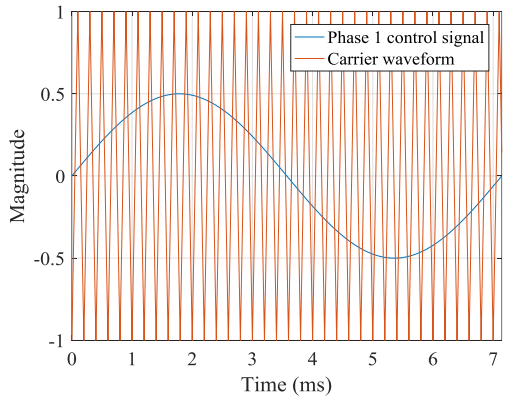
Figure 6.12 Fuji Electric IGBT module 2MBI650VXA-170E-50 [195].

Items		Symbols	Conditions		Maximum ratings	Units
Inverter	Collector-Emitter voltage	V_{CES}			1700	V
	Gate-Emitter voltage	V_{GES}			±20	V
	Collector current	Ic	Continuous	Tc=25°C	900	A
				Tc=100°C	650	
		Ic pulse	1ms		1300	
		-Ic			650	
		-Ic pulse	1ms		1300	
	Collector power dissipation	Pc	1 device		4150	W
Junction temperature		Tj			175	°C
Operating junction temperature (under switching conditions)		T_{jop}			150	
Case temperature		T_c			150	
Storage temperature		Tstg			-40 ~ +150	
Isolation voltage	between terminal and copper base (*1)	V_{iso}	AC : 1min.		4000	VAC
	between thermistor and others (*2)					
Screw torque (*3)	Mounting	-	M5		6.0	N m
	Main Terminals		M8		10.0	
	Sense Terminals		M4		2.1	

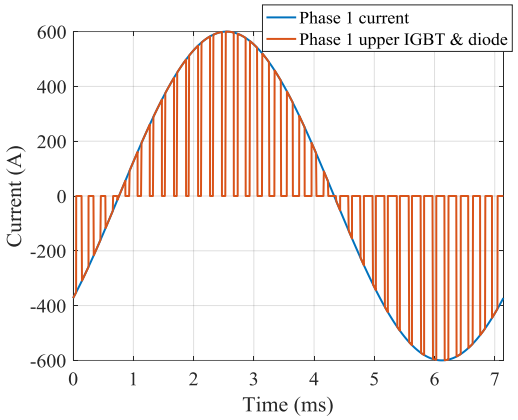
Figure 6.13 Fuji IGBT specifications [195].

Table 6.3 Nissan Leaf machine drive operating points and the power losses [11], [194].

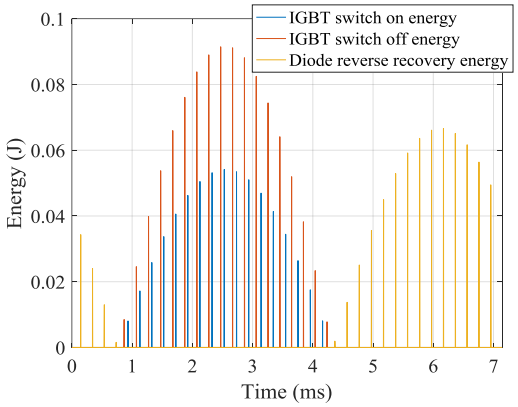
Speed (rpm)	2100	3000	4000	5000
Torque (Nm)	282.55	254.55	190.89	151.85
Vphase_RMS (V)	66.90	91.72	110.86	122.85
Iphase_peak (A)	600.00	535.00	403.00	345.00
Switching frequency	5 kHz			
Machine efficiency	92.91%	95.19%	96.69%	97.01%
Drive system efficiency	86.00%	90.00%	93.00%	94.00%
Inverter efficiency	94.00%	96.00%	97.00%	97.00%
Power factor	0.79	0.81	0.87	0.91
Modulation index	0.50	0.69	0.84	0.93
Current lagging angle (rad)	0.67	0.63	0.51	0.42
Total switches losses based on Fuji IGBT (W)	2996	2763	2044	1773
Total diodes losses based on Fuji IGBT (W)	1338	1051	676	521
Per IGBT die loss (W)	166.4	153.5	113.6	98.5
Per diode die loss (W)	74.3	58.4	37.6	28.9
VSI loss based on Fuji IGBT (W)	4334	3814	2720	2294
Nissan Leaf EV VSI loss from ORNL (W)	4335	3554	2579	2538



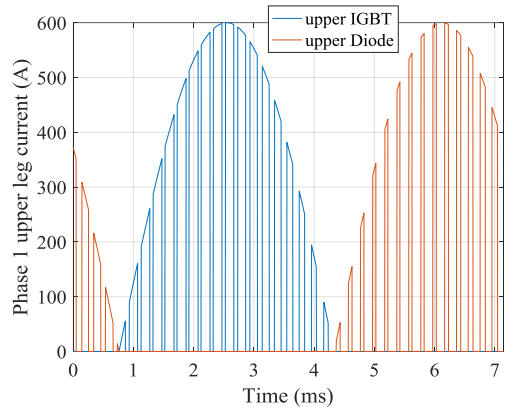
(a) Phase 1 control signal and carrier wave.



(b) Phase 1 and upper leg currents.

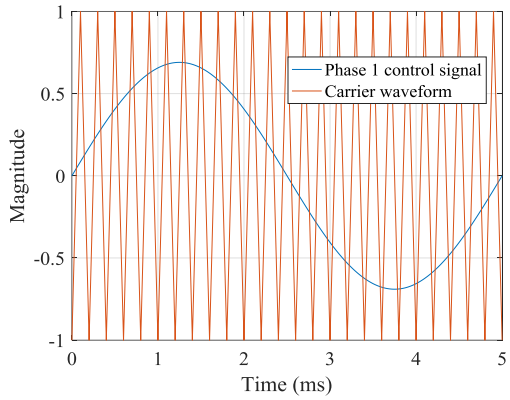


(c) Phase 1 upper leg switching losses.

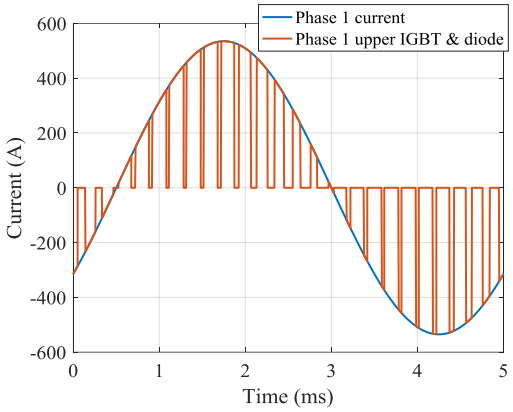


(d) Phase 1 upper leg current.

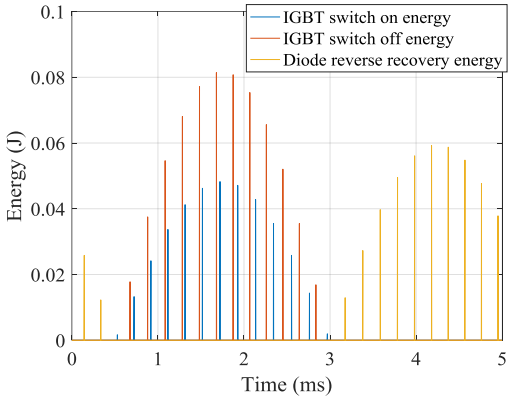
Figure 6.14 Phase 1 waveforms for power loss modelling under 2100 rpm operating condition.



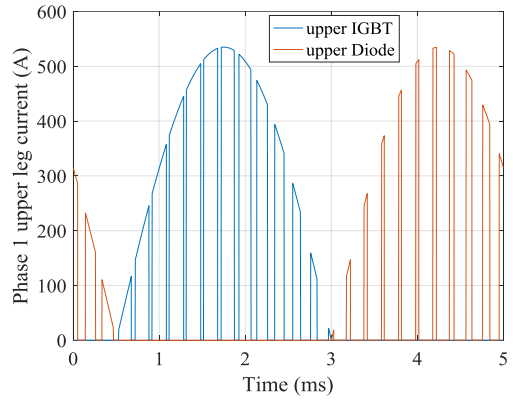
(a) Phase 1 control signal and carrier wave.



(b) Phase 1 and upper leg currents.

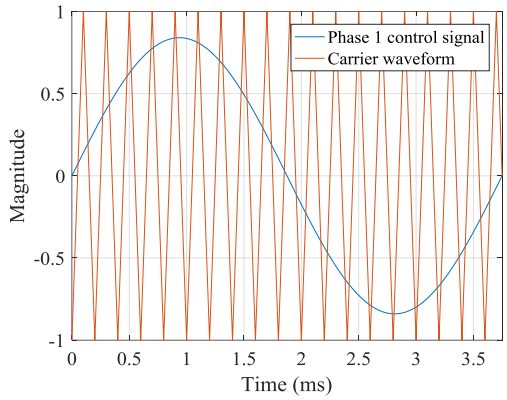


(c) Phase 1 upper leg switching losses.

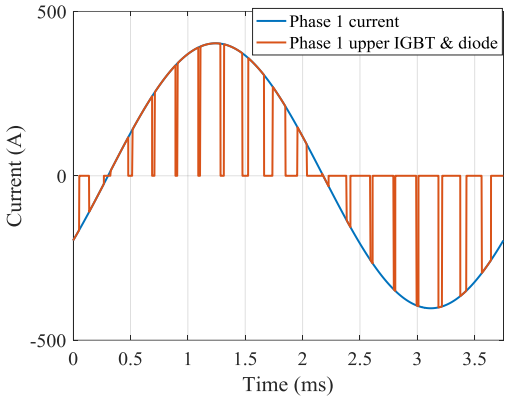


(d) Phase 1 upper leg current.

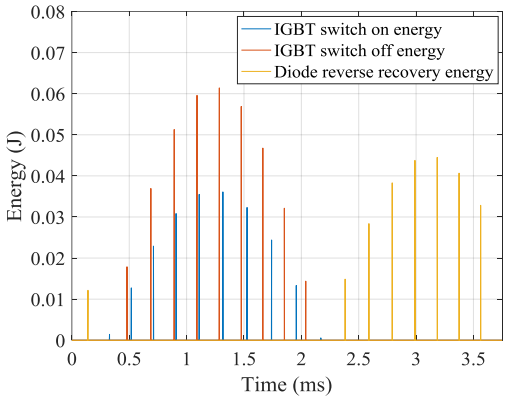
Figure 6.15 Phase 1 waveforms for power loss modelling under 3000 rpm operating condition.



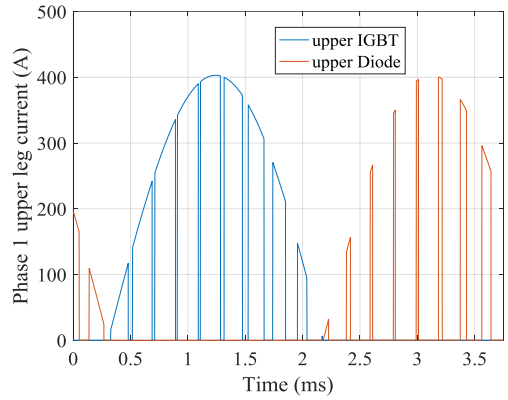
(a) Phase 1 control signal and carrier wave.



(b) Phase 1 and upper leg currents.

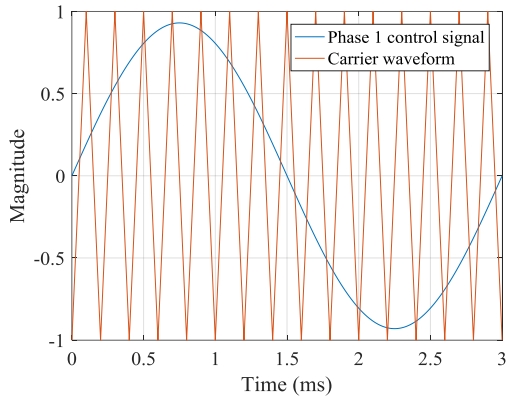


(c) Phase 1 upper leg switching losses.

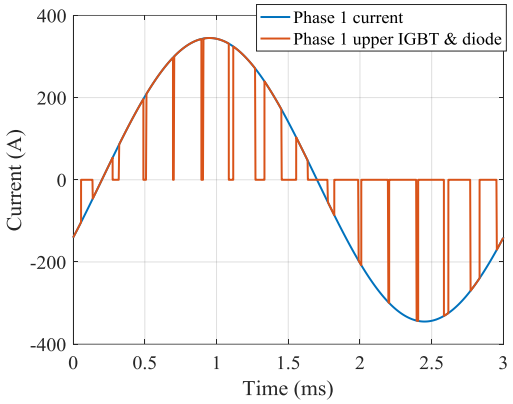


(d) Phase 1 upper leg current.

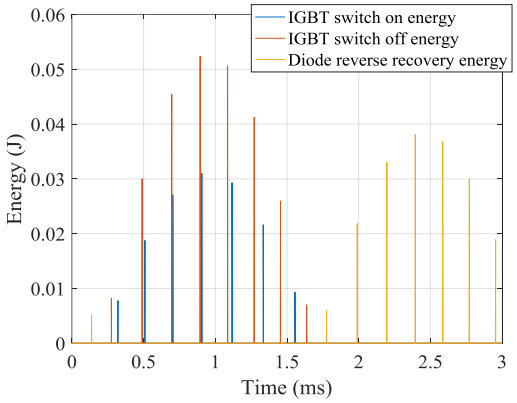
Figure 6.16 Phase 1 waveforms for power loss modelling under 4000 rpm operating condition.



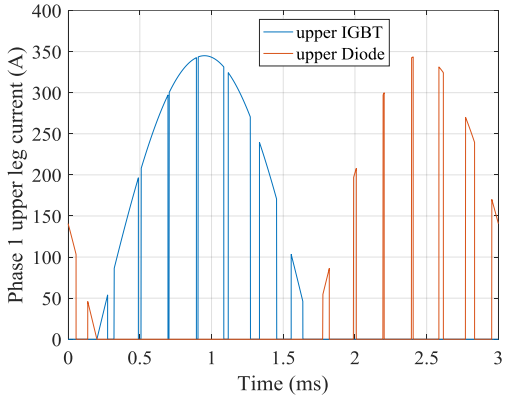
(a) Phase 1 control signal and carrier wave.



(b) Phase 1 and upper leg currents.



(c) Phase 1 upper leg switching losses.



(d) Phase 1 upper leg current.

Figure 6.17 Phase 1 waveforms for power loss modelling under 5000 rpm operating condition.

6.3.3 System Modelling and Validation: Thermal FEA of VSI

The basic structure of a power semiconductor module with base plate and its multi-layer equivalent circuit physical model is illustrated on page 83 in [89]. A semiconductor die is

the source of heat resulting a gradient temperature distribution from itself to the ambient illustrated on page 85 in [89].

The temperature difference between die and ambient is:

$$\Delta T_{d-a} = T_d - T_a \tag{6.5}$$

where T_d - die temperature and T_s - heatsink temperature.

Determined by the heat generated from the die chip and the thermal impedance between junction and the ambient, the temperature difference is supposed to be as low as possible. The relation between junction to heatsink temperature difference and the power loss, the thermal impedance (thermal resistance under steady state), is:

$$R_{th(j-s)} = \frac{T_j - T_s}{P_j} \tag{6.6}$$

where P_j - junction power loss.

Also the thermal resistance can be modelled by the heat conductivity (material characteristics) and the geometry of the layer:

$$R_{th} = \frac{d}{\lambda \cdot A} \tag{6.7}$$

where d - the thickness of the layer, λ - heat conductivity, and A - the layer area.

Besides the heat conductivity relating to thermal resistance, the heat storage characteristic introduces thermal capacitance in the thermal network and hence dominates the dynamics in heat transfer. The thermal capacitance can be modelled:

$$C_{th} = s \cdot V \tag{6.8}$$

where s - heat storage characteristic, and V - material volume of the target layer.

The heat generation on die chip has the priority to be considered as it is the major heat generation within the device. Compared with that the heat generated on internal connections, and external terminals and joints is negligible under low current situation, e.g. below 100A. However if the current increases to couples of hundreds amperes even for a low terminal resistance, 0.5 mΩ for example, the heat generation needs considering for the sake of terminal and hence the device reliability.

The Nissan Leaf VSI FEA model is built in the software of Ansys Icepak according to the benchmark system geometry and material properties. The different operation conditions are simulated on the FEA model to compare with the experimental results in [7], their specific thermal resistances under 55W power dissipation on one IGBT switch, 3 IGBT dies in parallel, and the coolant flow rates from 2 to 10 lpm with 2 lpm difference between consecutive flow rates. The FEA simulation results, the temperature distribution of IGBT switch and diode dies, are shown from Figure 6.18 to Figure 6.24 and the simulation summary is shown in Table 6.4. With the simulation results, the specific thermal resistance ($mm^2 - K/W$) can be calculated by:

$$R_{th\_specific} = \frac{\Delta T}{P_{jIGBT}} \cdot A_{jIGBT} \tag{6.9}$$

where ΔT is the temperature difference between the IGBT die and the coolant, P_{jIGBT} is the power loss on the IGBT switch, and A_{jIGBT} is the IGBT switch area.

The coolant temperature is defined as the average of the inlet coolant and outlet coolant temperature, and both the IGBT dies maximum temperature and average temperature are considered in the specific thermal resistance calculation. The specific thermal resistances calculated from the built model is compared with those in the experiments in [7] and the results in Figure 6.25 show the match between each other indicating that the FEA model is consistent with the experimental conditions and results.

6.3.4 Thermal Study under Unbalanced IGBT Die Power Losses

The current hence power loss imbalance of the parallel-connected IGBT switch and diode dies are discussed before. The simulations are conducted on the validated Nissan Leaf 2012 VSI FEA thermal model under 2100 rpm operating point (almost the highest VSI power loss among the whole operating range) and balanced power losses for all the IGBT switches and their corresponding freewheeling diodes as shown in Figure 6.26. The diode dies temperatures are much lower than those of the switch dies indicating less thermal

consideration. As a result, here the investigation only focuses on the parallel-connected unbalanced IGBT switch dies power losses and the resulting temperature deviation.

To simplify the analysis and simulation all the other IGBT switch and diode dies power losses are kept balanced while the unbalanced power losses are assumed to only occur in the three parallel-connected switch dies in the red circle as shown in Figure 6.26. The reason to choose this IGBT switch is that even under the balanced power losses these three IGBT switch dies have the highest temperature deviation degree (due to the coolant fluid and heatsink geometry), hence the temperature deviation degree and peak temperature spot could be severer under the unbalanced power losses conditions. As the power losses on IGBT dies are temperature dependent, the power losses on the 3 parallel-connected IGBT dies are recalculated considering their respective die temperatures. This procedure continues for 1 iteration and the power losses converge with the die temperatures as shown in Figure 6.27. Here for the iteration it is assumed that:

- Only the temperature variation affects the current hence power imbalance.
- The die power loss is proportional to the die current.
- The current variation between 125 °C and 150 °C die temperature is linear.

In the paralleled switch dies the power loss deviations of different degrees 2.5%, 5%, 10%, and 30%, under 2100 rpm operating point are investigated emulating the current imbalances introduced by the circuitry, thermal, and fatigue degree imbalances among the parallel-connected IGBT dies. The FEA simulation results are summarized in Table 6.5 containing power loss, maximum temperature, minimum temperature, and average temperature on each IGBT dies as well as the inlet and outlet coolant temperatures. The VSI temperature distributions under these conditions from the FEA simulations are shown from Figure 6.26 to Figure 6.32.

The maximum and minimum temperatures of the three IGBT dies versus different power loss deviation degrees are shown in Figure 6.33 and the IGBT dies temperature differences (between the maximum and minimum temperatures) are shown in Figure 6.34. The summarized results show the linearity between the IGBT dies maximum and minimum temperatures and their differences, and the power loss deviation degrees – higher power

loss deviation corresponding higher die maximum temperature and temperature differences among the 3 parallel-connected IGBT dies. Higher IGBT die temperature results in faster aging procedure and the higher IGBT die temperature difference leads to higher different degrees of fatigue development. As a result, the higher power loss deviation indicates less use of the lifetime of all the parallel-connected IGBT switch dies.

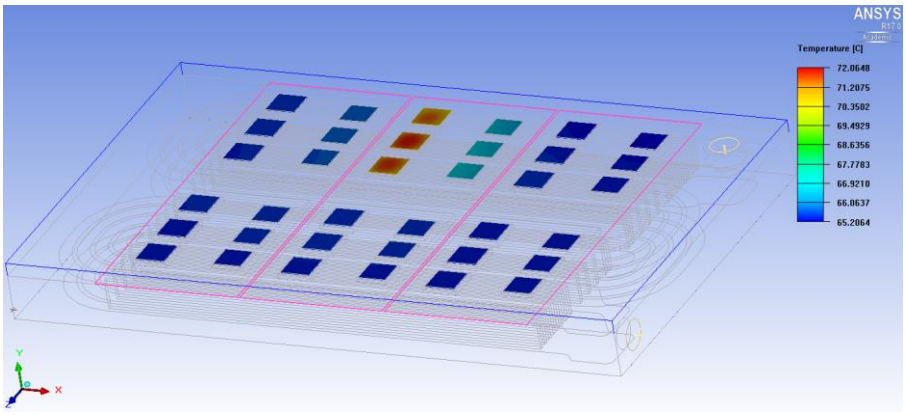


Figure 6.18 FEA simulation under the flow rate of 2 lpm.

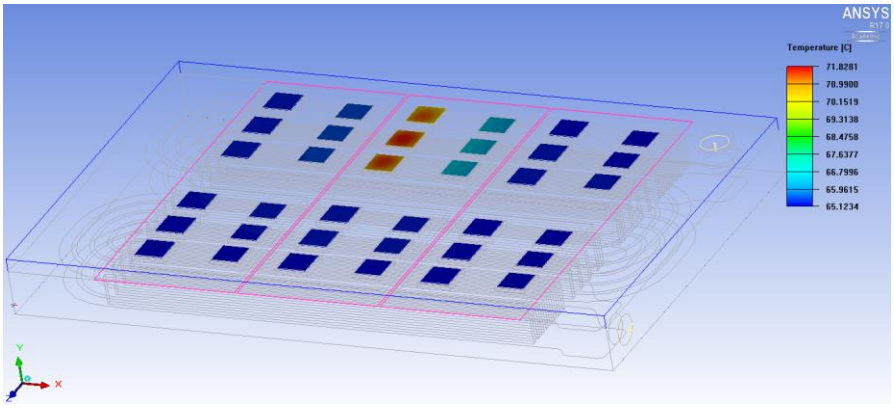


Figure 6.19 FEA simulation under the flow rate of 4 lpm.

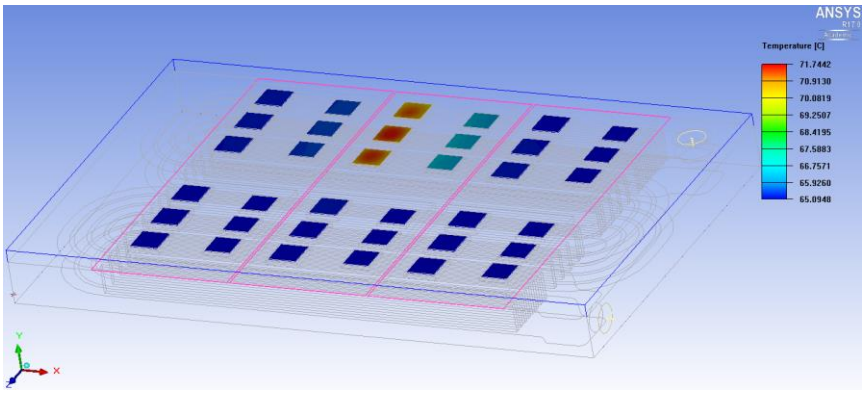


Figure 6.20 FEA simulation under the flow rate of 6 lpm.

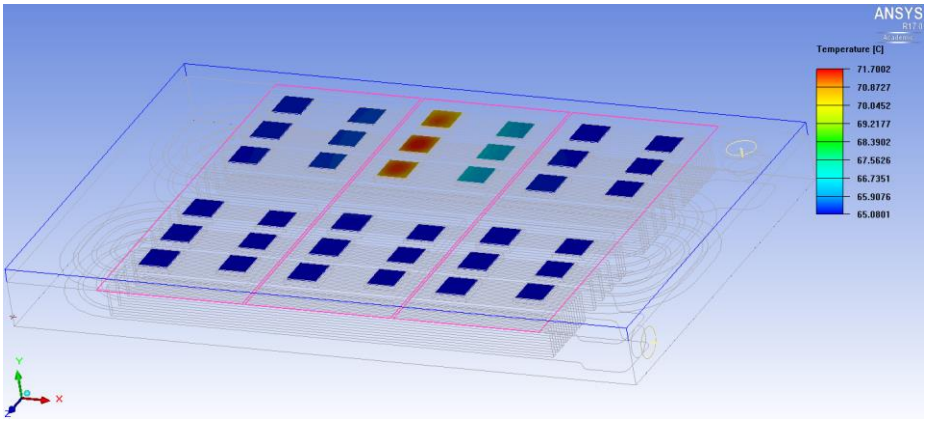


Figure 6.21 FEA simulation under the flow rate of 8 lpm.

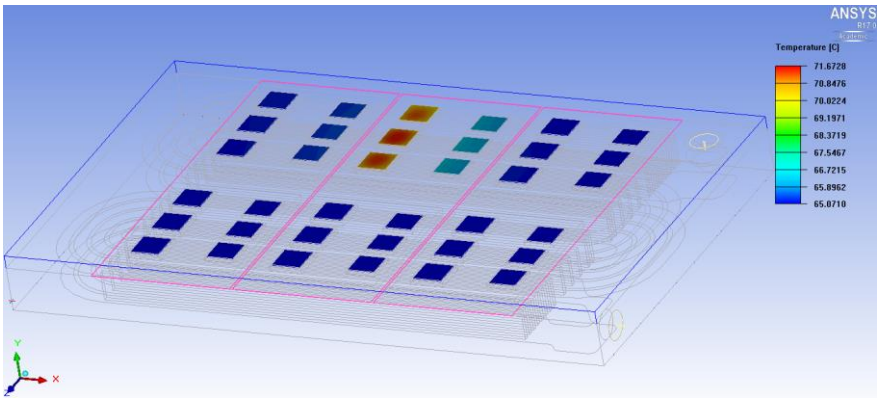


Figure 6.22 FEA simulation under the flow rate of 10 lpm.

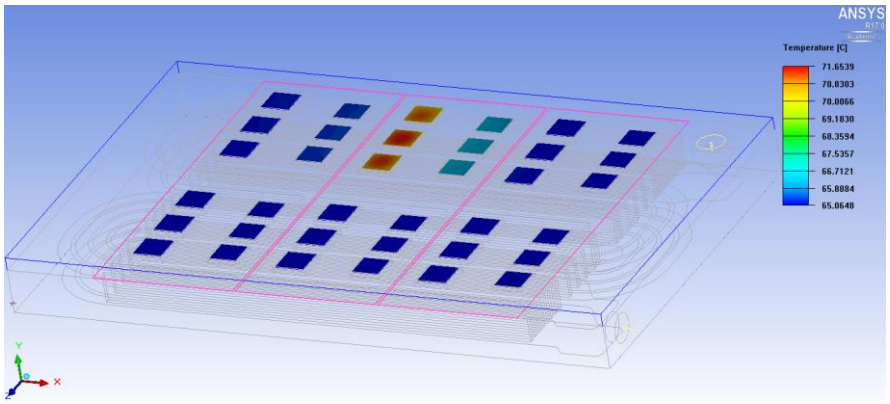


Figure 6.23 FEA simulation under the flow rate of 12 lpm.

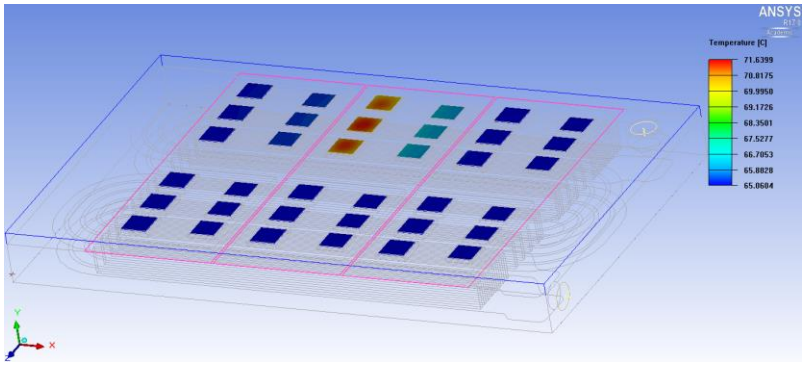


Figure 6.24 FEA simulation under the flow rate of 14 lpm.

Table 6.4 FEA simulation results on different coolant flow rates.

	Inlet coolant (°C)	Outlet coolant (°C)	3 IGBT dies (°C)		
Flow rate (lpm)			Min	Max	Mean
2	65.0	65.5	69.9	72.1	71.4
4	65.0	65.2	69.7	71.8	71.2
6	65.0	65.2	69.7	71.7	71.1
8	65.0	65.1	69.6	71.7	71.0
10	65.0	65.1	69.6	71.7	71.0
12	65.0	65.1	69.6	71.7	71.0
14	65.0	65.1	69.6	71.6	71.0

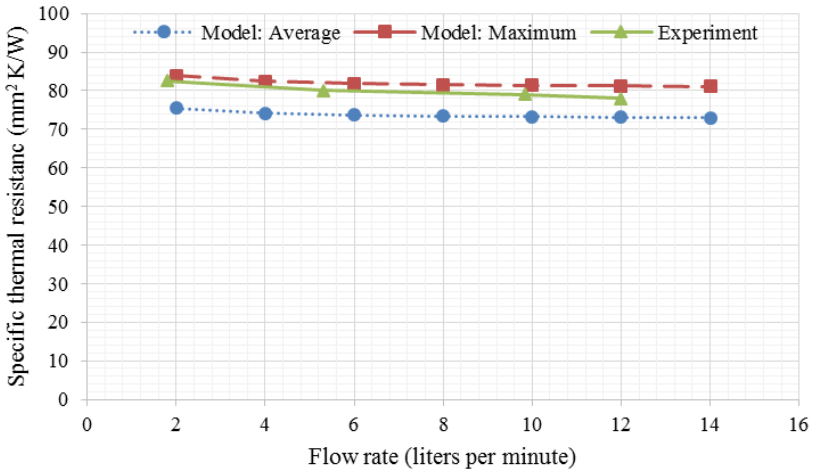


Figure 6.25 Specific thermal resistance comparison between the experimental results and the simulation results from the FEA model.

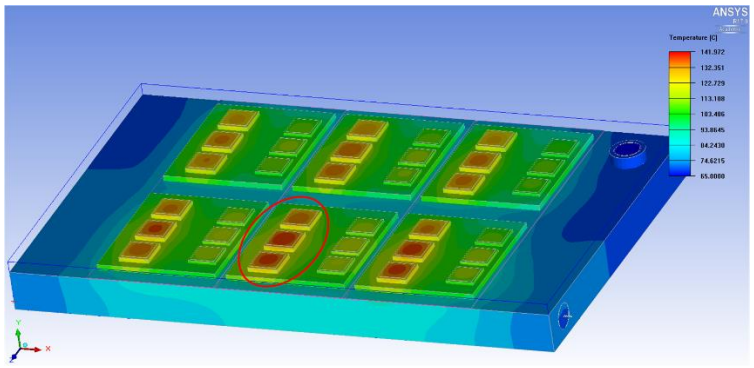


Figure 6.26 FEA simulation and dies temperature distribution under balanced power loss in 3 paralleled IGBT dies.

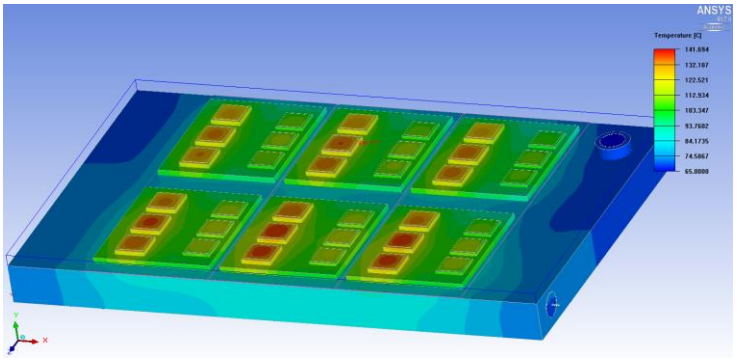


Figure 6.27 FEA simulation and dies temperature distribution under balanced power loss in 3 paralleled IGBT dies with 1 iteration considering the temperature dependency.

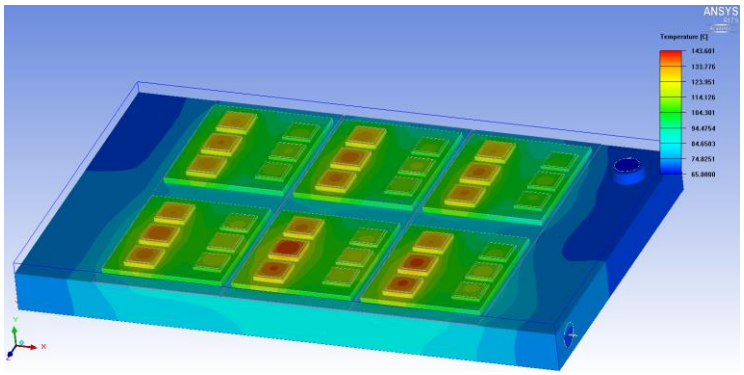


Figure 6.28 FEA simulation and dies temperature distribution under 2.5% power loss deviation in 3 paralleled IGBT dies.

Table 6.5 FEA simulation results under different power loss deviation conditions.

		Upper Die	Middle Die	Lower Die	Inlet coolant	Outlet coolant
Balanced power loss	Power loss (W)	166.4	166.4	166.4	N/A	N/A
	Max temperature (°C)	137.2	142.0	140.7	N/A	N/A
	Min temperature (°C)	121.9	128.9	127.0	N/A	N/A
	Ave temperature (°C)	132.6	137.8	136.4	65.2	72.4
1 iteration consideration	Power loss (W)	168.3	165.0	165.9	N/A	N/A
	Max temperature (°C)	137.6	141.7	140.5	N/A	N/A
	Min temperature (°C)	122.2	128.8	126.9	N/A	N/A
	Ave temperature (°C)	133.0	137.6	136.3	65.2	72.4
2.5% power loss deviation	Power loss (W)	162.2	174.7	162.2	N/A	N/A
	Max temperature (°C)	136.5	143.6	139.9	N/A	N/A
	Min temperature (°C)	121.4	129.8	126.5	N/A	N/A
	Ave temperature (°C)	132.0	139.2	135.8	65.2	72.4
5% power loss deviation	Power loss (W)	158.1	183.0	158.1	N/A	N/A
	Max temperature (°C)	135.9	145.2	139.2	N/A	N/A
	Min temperature (°C)	120.8	130.8	125.9	N/A	N/A
	Ave temperature (°C)	131.4	140.6	135.1	65.2	72.4
10% power loss deviation	Power loss (W)	149.8	199.7	149.8	N/A	N/A
	Max temperature (°C)	134.6	148.5	137.8	N/A	N/A
	Min temperature (°C)	119.8	132.7	124.8	N/A	N/A
	Ave temperature (°C)	130.2	143.4	133.9	65.2	72.4
20% power loss deviation	Power loss (W)	133.1	233.0	133.1	N/A	N/A
	Max temperature (°C)	132.0	155.0	135.0	N/A	N/A
	Min temperature (°C)	117.8	136.6	122.6	N/A	N/A
	Ave temperature (°C)	127.7	149.0	131.2	65.2	72.4
30% power loss deviation	Power loss (W)	116.5	266.2	116.5	N/A	N/A
	Max temperature (°C)	129.6	161.5	132.3	N/A	N/A
	Min temperature (°C)	115.7	140.4	120.4	N/A	N/A
	Ave temperature (°C)	125.2	154.6	128.7	65.2	72.4

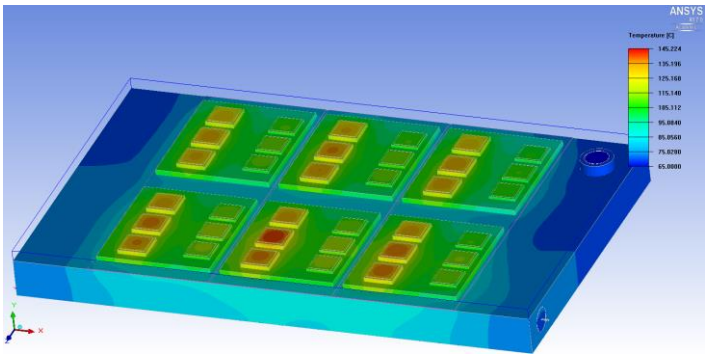


Figure 6.29 FEA simulation and dies temperature distribution under 5% power loss deviation in 3 paralleled IGBT dies.

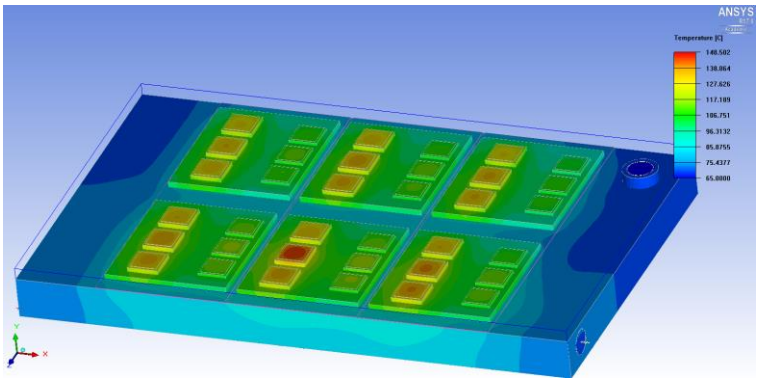


Figure 6.30 FEA simulation and dies temperature distribution under 10% power loss deviation in 3 paralleled IGBT dies.

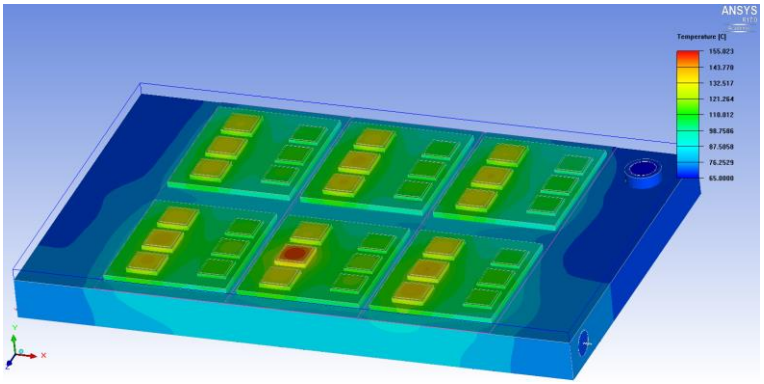


Figure 6.31 FEA simulation and dies temperature distribution under 20% power loss deviation in 3 paralleled IGBT dies.

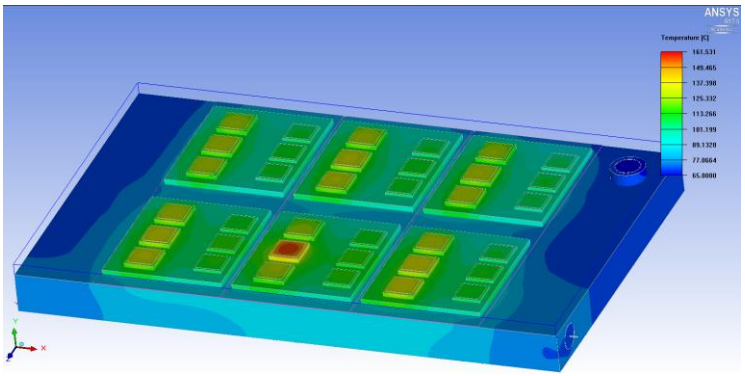


Figure 6.32 FEA simulation and dies temperature distribution under 30% power loss deviation in 3 paralleled IGBT dies.

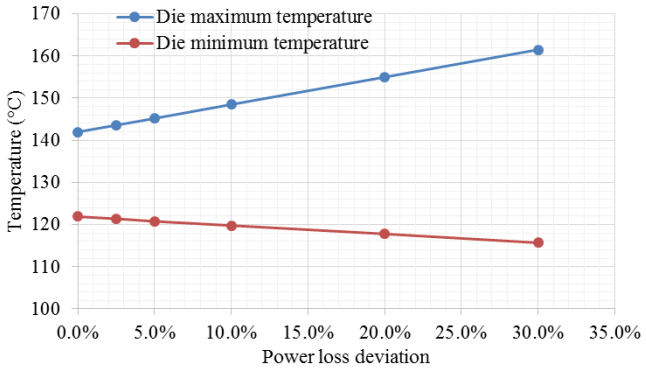


Figure 6.33 Maximum and minimum die temperatures under different degree power loss deviation in the 3 parallel IGBT dies.

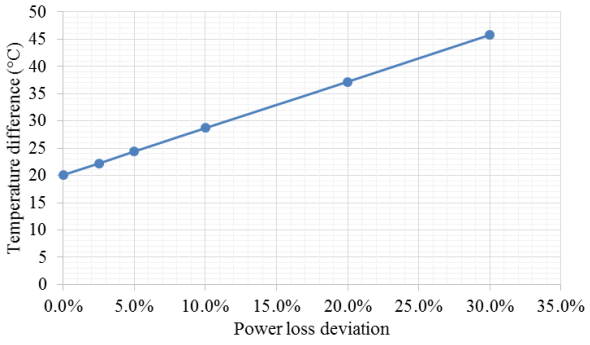


Figure 6.34 Maximum and minimum die temperature difference under different degree power loss deviation in the 3 parallel IGBT dies.

6.4 New Multiphase VSI Designs

6.4.1 A New 9-phase Conventional Design VSI

Instead of the 3-phase benchmark VSI, a 9-phase conventional design VSI is proposed to alleviate the parallel IGBT dies current and power loss imbalance, decrease the DC-link capacitor volume (based on and successive to Chapter 4), and decrease the VSI and machine connecting cable conductor volume.

There are 3 IGBT modules in the benchmark VSI and each IGBT module is for each phase leg containing upper and lower IGBT switches and diodes, each of them with 3 dies in parallel connection as shown in Figure 6.35 (a). While in the proposed 9-phase conventional design VSI, each IGBT module is newly designed and modified to have 3 phase legs and there is not any die parallel connection – 1 IGBT die for 1 IGBT switch and 1 diode die for 1 diode. This design requires 3 individual AC output connectors and 6 gate pins on per IGBT module controlling each phases respectively as shown in Figure 6.35 (b). 3 newly designed and modified IGBT modules compose 9 phase legs as shown in Figure 6.36. The die layout and size do not change while the AC output connectors, the connection between AC output connector and the IGBT dies, and the gate pins are modified. The mounting and layout of the IGBT modules on the heatsink keep the same as well.

Inside the 3-phase VSI the phase current is controlled by driving the upper and lower IGBT gate signals while each IGBT switch is composed of 3 IGBT dies in parallel connection so that the current through each die cannot be controlled directly and there is inevitable unbalanced currents and hence unbalanced power losses. However, in the 9-phase VSI as each IGBT die corresponds each IGBT switch, the phase current control is actually the control of the current through each IGBT dies. As a result, the power losses of IGBT dies will converge to the same value while there is still some power loss differences due to the IGBT dies temperature deviation (because of the heatsink geometry) – the die power loss dependency to the temperature. The FEA thermal model is shown in Figure 6.37 (semi-transparent grey – heatsink entity, semi-transparent cyan – liquid coolant, semi-transparent white – dielectric layer, semi-transparent brown – copper layer, yellow – copper moly layer,

and white – dies), geometrically the same with the 3-phase benchmark system. Here it is assumed that the die power loss discrepancy due to the temperature deviation is negligible, the temperature distribution from the FEA simulation under the balanced power loss on the dies is shown in Figure 6.38. It has the better performance than any unbalanced power losses conditions in 3-phase VSI. Figure 6.39 shows the coolant temperature distribution, which corresponds the IGBT dies temperature distribution in Figure 6.38.

The DC-link capacitor in the 9-phase VSI design is 1/3 the volume of that in the 3-phase design which has been concluded in Chapter 4. As a result, the proposed 9-phase VSI just requires 1/3 size DC-link capacitor of its 3-phase counterpart (as shown in Figure 6.40 (a) and (b)) resulting the new capacitor design as shown in Figure 6.40 (c).

The standard cables (in AWG or Kcmil) are supposed to be applied to connect between the VSI and the traction machine, which is fit for the volume manufacture and cost control. The standard cables comparison is shown in Table 6.6 and the current densities versus cable conductor cross sectional areas are shown in Figure 6.41 (a) where for the current density under each cable temperature rating there is an exponential decrease with respect to the increase of the cable conductor cross sectional area. These characteristics result in the possibility of the decreased total cable conductor material, and hence increase the machine drive system power density by the implementation of multiphase machine drive systems. Although the better utilization of the cable conductor is briefed in [179] while not described in detail and not even investigated and compared quantitatively for different phase number systems.

Under the same VSI power rating the requirement of the DC input cable between the battery pack and the VSI does not change, that the 3-phase benchmark and the proposed 9-phase inverter both use 1/0 AWG cable. In the benchmark system three 3/0 AWG cables are used in the AC output side with the current ratings 165 A (in 60 °C rating cable) 200 A (in 75 °C rating cable), and 225 A (in 90 °C rating cable). While in the proposed 9-phase system under the equivalent power rating nine 6 AWG cables are eligible with the current ratings 55 A (in 60 °C rating cable), 65 A (in 75 °C rating cable), and 75 A (in 90 °C rating cable). The total AC output cables conductor cross sectional area ratio between the 3-phase

benchmark VSI and the proposed 9-phase inverter is 1:0.47. The cable length between the VSI and the machine varies for different machine drive system designs while under the same length the total conductor volume is proportional to the total cable conductor cross sectional area of all the phases. As a result, the total AC cable conductor material volume ratio is 1:0.47 between the 3-phase benchmark and the proposed 9-phase conventional design VSI saving 53% conductor material. The lower current rating cable is also more flexible to bend and hence easier to be managed in the assembling.

To generalize the conclusion, another case is studied with a different VSI phase current rating (300 A phase current in a 3-phase VSI) to compare the conductor material volume used in different phase number systems under the equivalent VSI power rating.

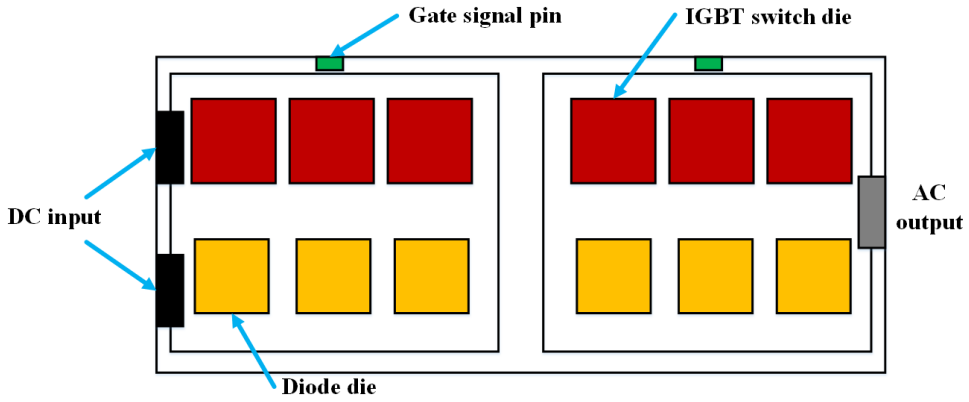
The phase current ratings and corresponding selected standard cables for different phase number systems are shown in Table 6.7, Table 6.8, and Table 6.9 under 3 different cable temperature ratings. Figure 6.41 (b) shows the normalized total conductor material volume with different even number (1 to 19) multiphase inverters under three different temperature ratings, of which compared with the 3-phase system the 9-phase system saves about half the conductor material volume, and the increased phase number system decreases the conductor material use.

6.4.2 A New 9-phase Integrated Design VSI

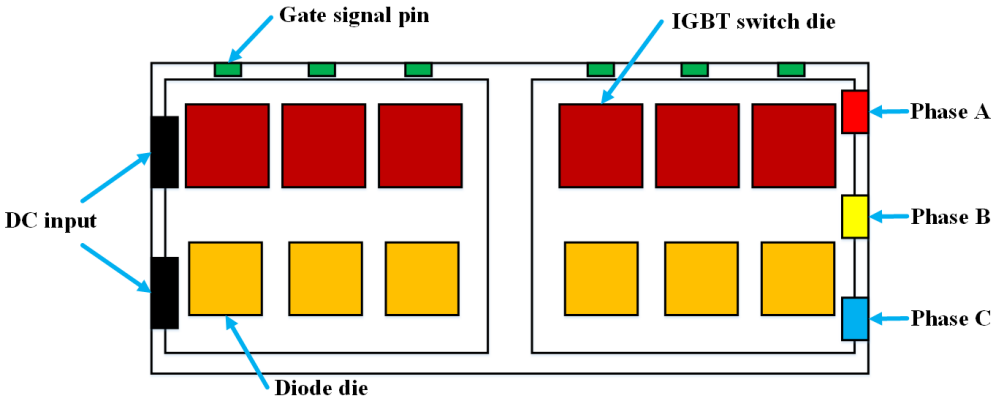
A new circular disk shape VSI is proposed here. According to the heat transfer isometric characteristics (in most cases and assumed to be here) the circular disk shape has the advantage over the rectangular shape (in the benchmark VSI) that the temperature gradient is from the center to the outer perimeter while the rectangular shape possibly has the lowest temperature spots on the angle. This suggests more efficient use of the heat transfer hence the volume. Moreover, the circular coolant channel in the circular heatsink eliminates the coolant direction turning parts (in the benchmark VSI), which are not directly underneath the heat sources, the dies, hence not highly efficiently contribute to the heat transfer from the dies to the coolant. With the circular coolant channel design, all the coolant channels

are underneath the power dissipating dies reinforcing the heat transfer efficiency and reducing the heatsink volume. Additionally, the circular disk shape design makes it possible for the VSI integration to the traction machine eliminating the power cables between the VSI and the machine, which decreases the connection complexity, and manufacture and maintenance difficulties of the 9-phase machine drive system due to its increased power terminals (can be generalized to other phase number VSIs). Consequently, better thermal performance, lower mechanical structure complexity, and higher integration are assumed to be achievable via the new 9-phase integrated design VSI that will be designed, studied, and compared with the previous designs in this section. Although some machine drive system integration designs are studied, for example, in papers [196]–[198] no publication is found for the multiphase VSI integration design with liquid cooling system, which enhances the novolty of this chapter.

The new 9-phase integrated design VSI is proposed to have the same cross section area and is fixed on one side of the traction machine. The benchmark 3-phase traction machine is redesigned to a 9-phase one (assuming that the 9-phase traction machine has the same dimensions with the benchmark one – 250 mm outer perimeter diameter as shown in Figure 6.42). The other properties, i.e. IGBT dies material and dimensions, different layers' materials and thicknesses, coolant flow rate, power losses on each IGBT and diode dies etc., are kept the same with the 9-phase conventional design VSI to have an equilibrium comparison condition. The diode dies and the accessary layers underneath them are modified to have the same cross-sectional dimensions with the IGBT dies, i.e. changing diode dies dimension from 14x14 mm to 15x15mm, while keeping the previous design layers thicknesses unchanged, which will not result in sound changes to the dies thermal performance while could lead to volume manufacturing conveniences.



(a) IGBT used in Nissan Leaf EV VSI.



(b) Proposed modified IGBT module.

Figure 6.35 IGBT used in Nissan Leaf EV VSI and the proposed modified IGBT module.

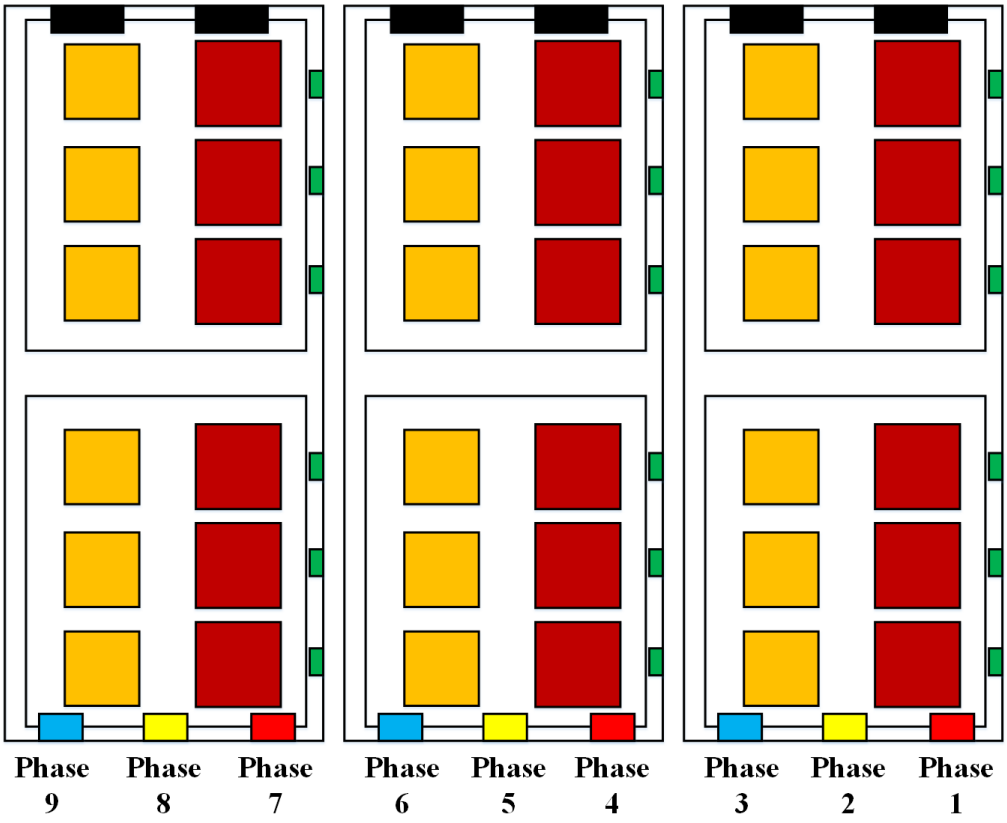


Figure 6.36 Proposed 9-phase VSI with the newly designed IGBT modules.

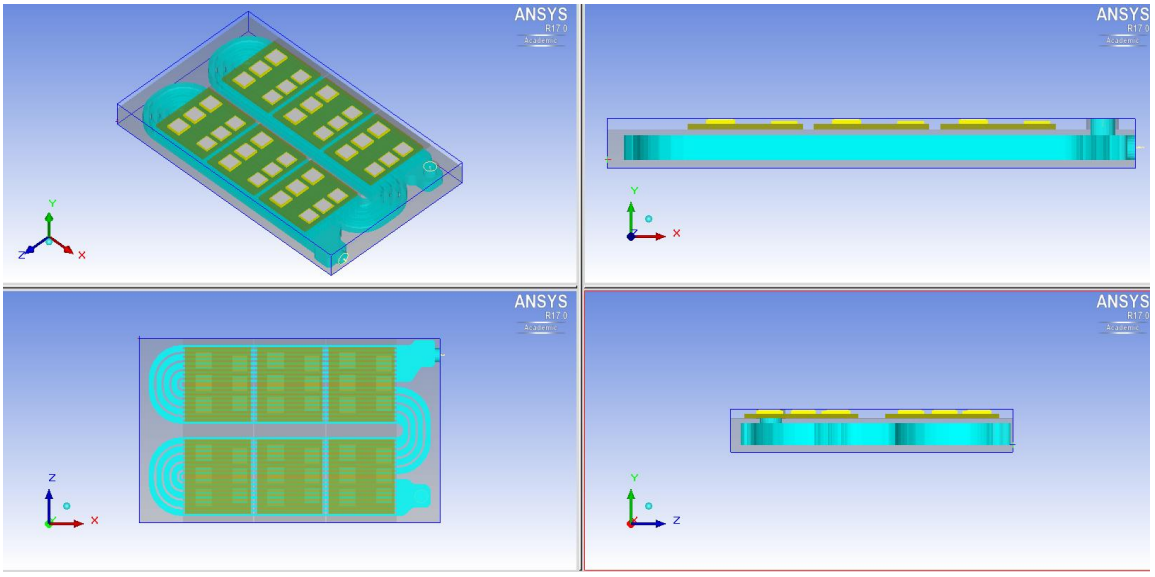


Figure 6.37 Different views of 9-phase conventional design VSI.

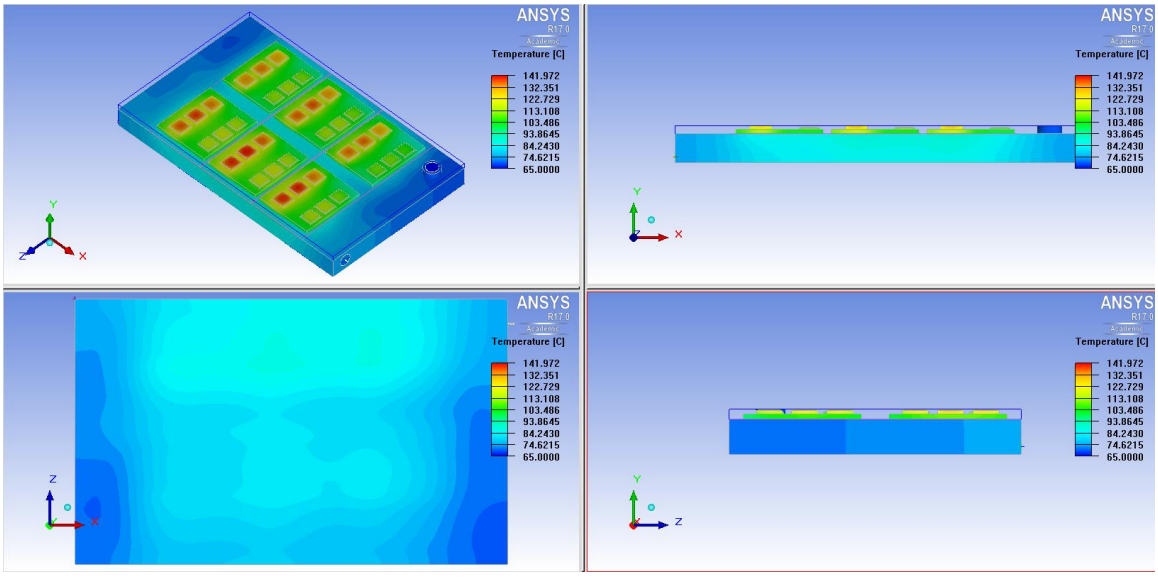


Figure 6.38 Temperature distribution of 9-phase conventional design VSI.

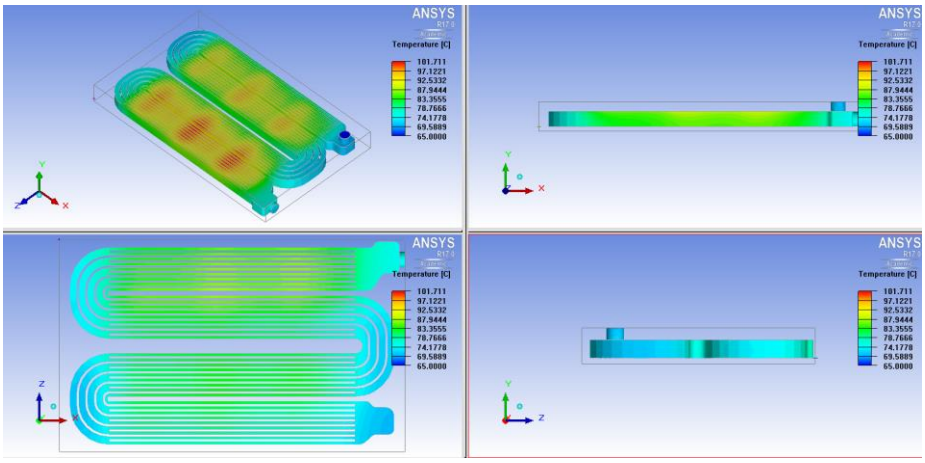
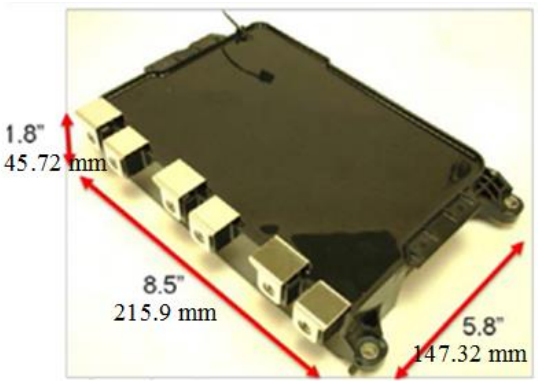
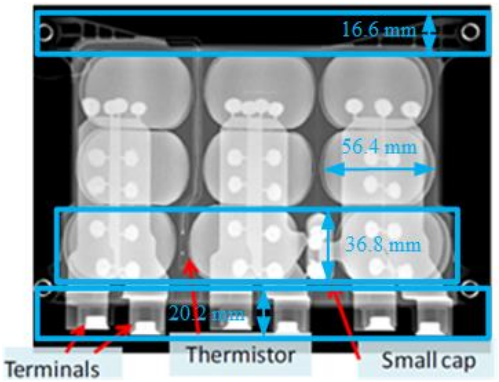


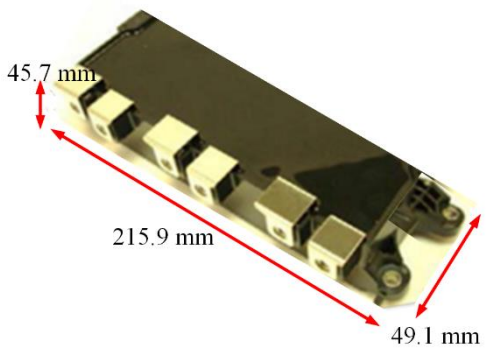
Figure 6.39 Coolant temperature distribution of 9-phase conventional design VSI.



(a) Nissan Leaf Cap size.



(b) Nissan Leaf Cap size in X-ray view.

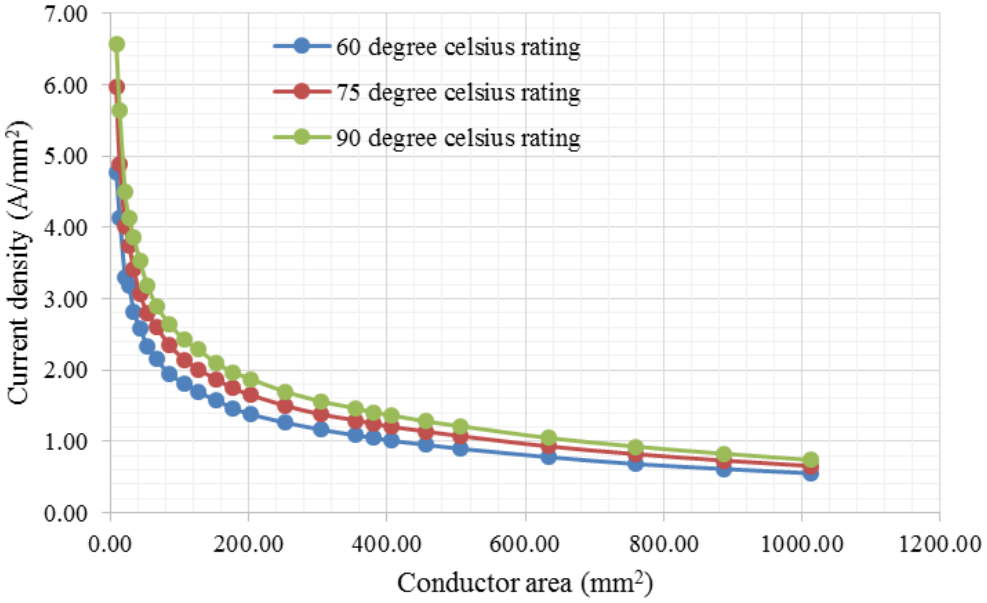


(c) Proposed 9-phase VSI Cap size.

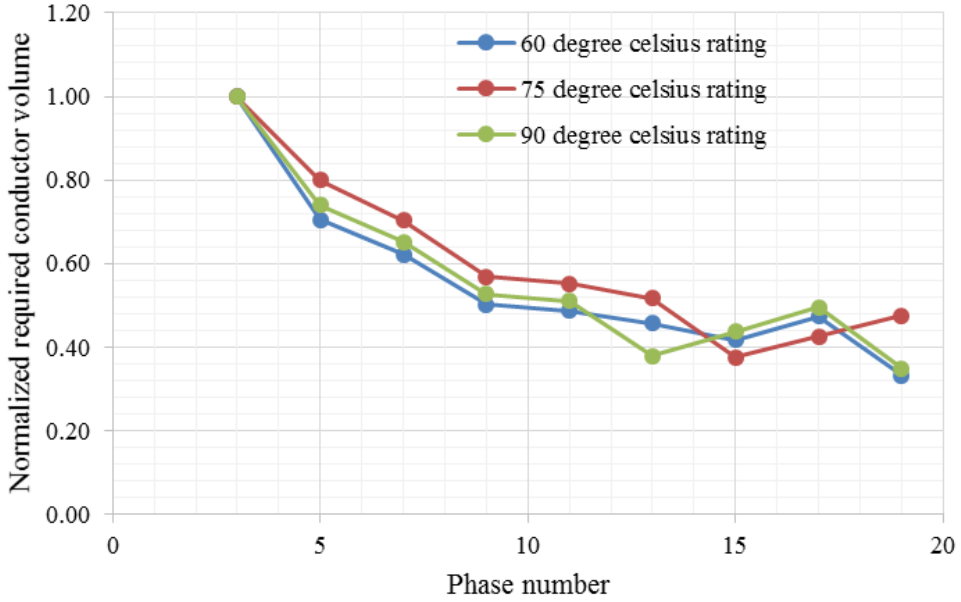
Figure 6.40 Nissan Leaf capacitor size, proposed 9-phase VSI capacitor size. Note, the author thanks Dr. T. Burress for permission to use this material.

Table 6.6 The standard cables comparison [199].

AWG/Kcmil	Conductor area (mm^2)	Ampacity with 60°C rating (A)	Ampacity with 75°C rating (A)	Ampacity with 90°C rating (A)	Current density with 60°C rating (A/mm^2)	Current density with 75°C rating	Current density with 90°C rating (A/mm^2)
8	8.37	40	50	55	4.78	5.98	6.57
6	13.30	55	65	75	4.13	4.89	5.64
4	21.15	70	85	95	3.31	4.02	4.49
3	26.67	85	100	110	3.19	3.75	4.12
2	33.63	95	115	130	2.82	3.42	3.87
1	42.41	110	130	150	2.59	3.07	3.54
1/0	53.48	125	150	170	2.34	2.80	3.18
2/0	67.43	145	175	195	2.15	2.60	2.89
3/0	85.03	165	200	225	1.94	2.35	2.65
4/0	107.22	195	230	260	1.82	2.15	2.42
250	126.68	215	255	290	1.70	2.01	2.29
300	152.01	240	285	320	1.58	1.87	2.11
350	177.35	260	310	350	1.47	1.75	1.97
400	202.68	280	335	380	1.38	1.65	1.87
500	253.35	320	380	430	1.26	1.50	1.70
600	304.02	355	420	475	1.17	1.38	1.56
700	354.69	385	460	520	1.09	1.30	1.47
750	380.03	400	475	535	1.05	1.25	1.41
800	405.36	410	490	555	1.01	1.21	1.37
900	456.03	435	520	585	0.95	1.14	1.28
1000	506.70	455	545	615	0.90	1.08	1.21



(a) Standard cable conductor current density versus the conductor cross sectional area.



(b) Standard cable conductor material volume comparison normalization for different phase number inverters.

Figure 6.41 Standard cable conductor comparison under different phase number VSIs.

Table 6.7 Cable (60°C rated) requirements of equivalent power multiphase inverters.

	3-phase	5-phase	7-phase	9-phase	11-phase	13-phase	15-phase	17-phase	19-phase
AWG/Kcmil	500 Kcmil	4/0 AWG	2/0 AWG	1 AWG	2 AWG	3 AWG	4 AWG	4 AWG	6 AWG
Ampacity with rated 60°C (A)	320	195	145	110	95	85	70	70	55
Conductor cross section area (mm^2)	253.35	107.22	67.43	42.41	33.63	26.67	21.15	21.15	13.30
Required conductor material normalization	1.00	0.71	0.62	0.50	0.49	0.46	0.42	0.47	0.33

Table 6.8 Cable (75°C rated) requirements of equivalent power multiphase inverters.

	3-phase	5-phase	7-phase	9-phase	11-phase	13-phase	15-phase	17-phase	19-phase
AWG/Kcmil	350 Kcmil	3/0 AWG	1/0 AWG	2 AWG	3 AWG	4 AWG	6 AWG	6 AWG	6 AWG
Ampacity with rated 75°C (A)	310	200	150	115	100	85	65	65	65
Conductor cross section area (mm^2)	177.35	85.03	53.48	33.63	26.67	21.15	13.30	13.30	13.30
Required conductor material normalization	1.00	0.80	0.70	0.57	0.55	0.52	0.37	0.42	0.47

Table 6.9 Cable (90°C rated) requirements of equivalent power multiphase inverters.

	3-phase	5-phase	7-phase	9-phase	11-phase	13-phase	15-phase	17-phase	19-phase
AWG/Kcmil	300 Kcmil	2/0 AWG	1 AWG	3 AWG	4 AWG	6 AWG	6 AWG	6 AWG	8 AWG
Ampacity with rated 90°C (A)	320	195	150	110	95	75	75	75	55
Conductor cross section area (mm^2)	152.01	67.43	42.41	26.67	21.15	13.30	13.30	13.30	8.37
Required conductor material normalization	1.00	0.74	0.65	0.53	0.51	0.38	0.44	0.50	0.35

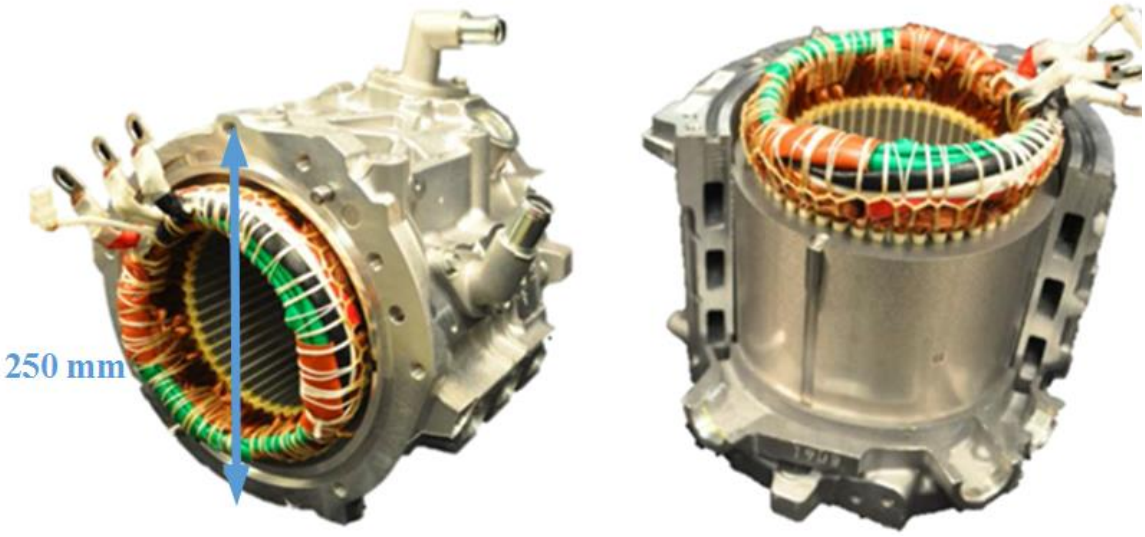


Figure 6.42 Nissan Leaf traction machine [191]. Note, the author thanks Dr. T. Burress for permission to use this material.

6.4.3 A New 9-phase Integrated Design VSI: Initial Design and Evolution Procedure

The initial design VSI, a disk shape with the diameter 250 mm, is shown in Figure 6.43 (semi-transparent grey – heatsink entity, semi-transparent cyan – liquid coolant, semi-transparent white – dielectric layer, semi-transparent brown – copper layer, yellow – copper moly layer, and white – dies) where the 9-phase IGBT module is designed to be a circular shape, and the IGBT and diode dies are radially and symmetrically placed on the circular copper base plate (with one phase leg dies labelled). The circular and counter-flow coolant is applied, which the inlet and outlet positions and coolant directions are labelled in Figure 6.43. Figure 6.44 and Figure 6.45 show the VSI surface temperature distribution and coolant channel temperature distribution respectively. In each phase leg, the two hotter dies are IGBT dies among the four, two IGBTs and two diodes. Because the diode dies temperature distribution is almost balanced and their peak temperature is much lower than that of the IGBT dies, the discussion and focus are on the IGBT dies peak temperature and their temperature distribution in the following content.

The initial design has higher peak IGBT die temperature compared with the 9-phase conventional design VSI. Some IGBT dies temperature deviation can be observed on Figure 6.44 because of 3 reasons:

- The coolant channel layouts underneath different IGBT dies are different, i.e. some IGBT dies crossing 3 different channels while some just on two as shown in Figure 6.43.
- Some asymmetrical characteristics in the coolant channel lead to the unbalanced coolant channel temperature distribution as shown in Figure 6.45.
- The shape and dimension of the copper base plate layer are not properly designed resulting in the corresponding inner and outer IGBT dies temperature differences as shown in Figure 6.44.

The temperature distribution can be improved by heatsink and IGBT module geometry modification. Additionally, from Figure 6.44 the non-gradient temperature distribution on both the central parts of the copper layer and the heatsink suggests the possible hollowing

to an annulus shape without sound temperature change on the IGBT dies while reducing the volume hence increasing the power density.

The evolutional design is conducted in the following content and its procedure is proposed in Figure 6.46 to improve the thermal performance and reduce the unnecessary material use. The first evolution designs focus on the modification on the copper layer dimensions (the same with the dielectric layer) and the coolant inlet and outlet positions. In the second evolution designs the coolant channels are changed to be thinner and their layouts are changed with the consideration of the coolant inlet and outlet positons. The third evolution design is to furtherly consider the coolant pressure drop between the inlet and outlet suggesting the comparable coolant channel flow resistance and resulting coolant circulation driving power with the benchmark system heatsink. After all the evolution designs the candidates are selected, evaluated and compared comprehensively with the 9-phase conventional design VSI, after which the best choice is proposed.

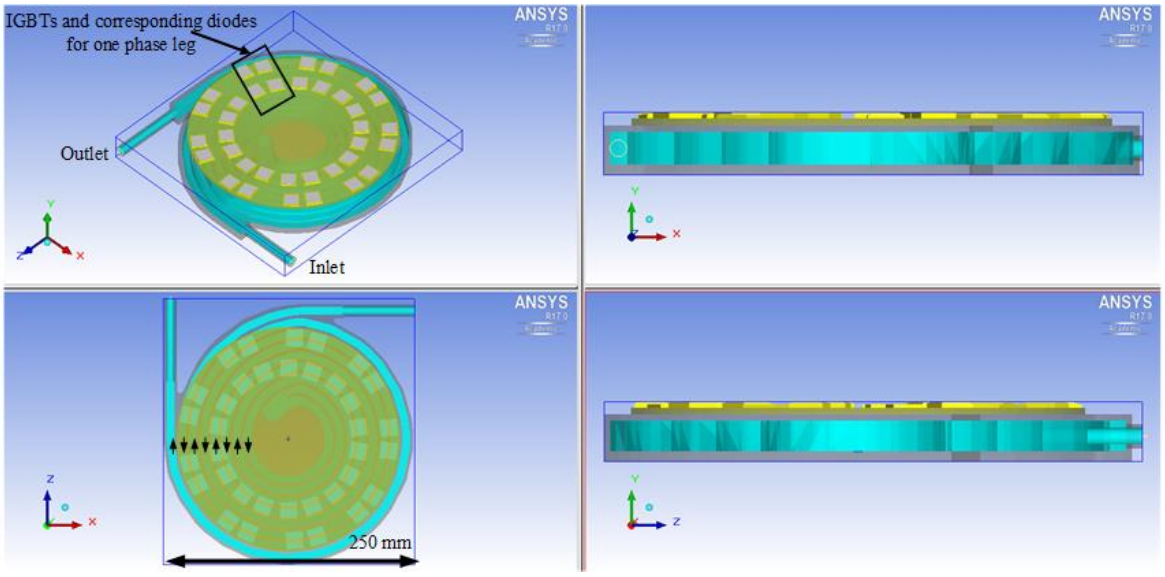


Figure 6.43 Different views of the initial 9-phase integrated design VSI.

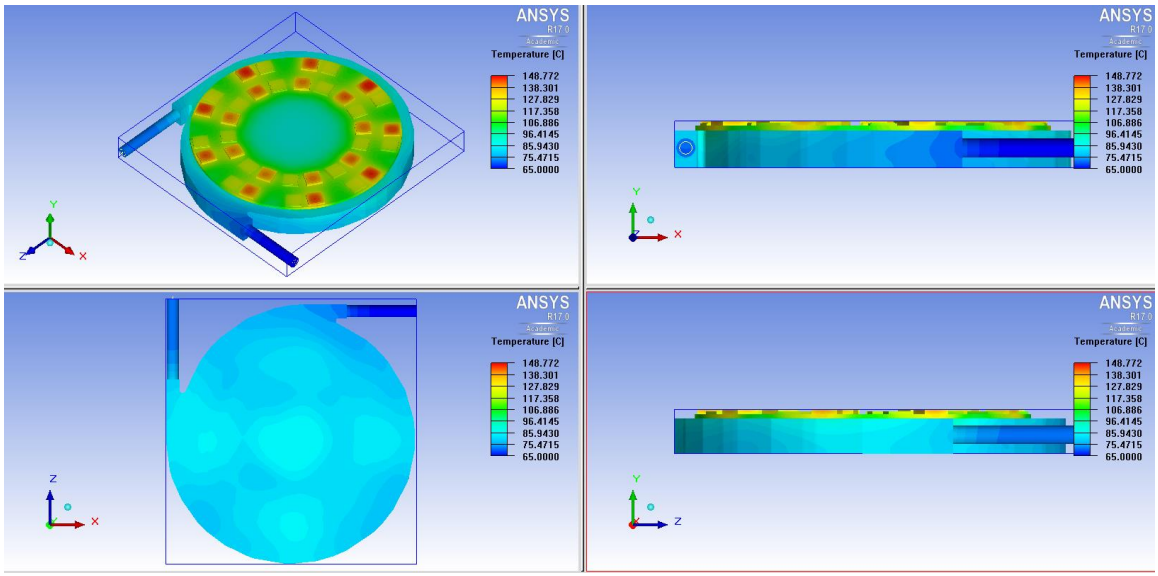


Figure 6.44 Temperature distribution of the initial 9-phase integrated design VSI.

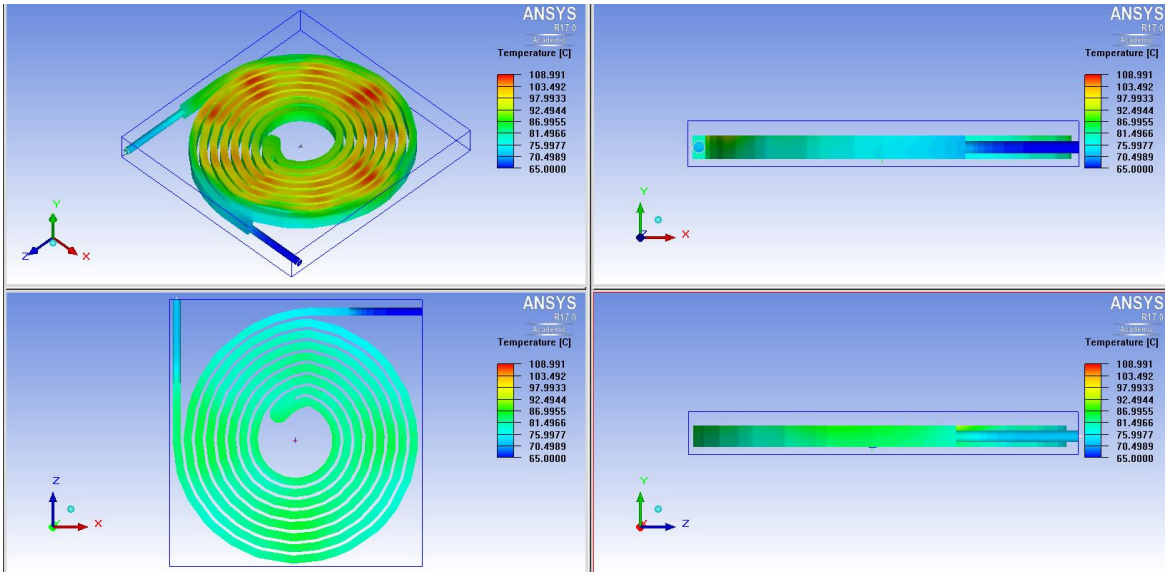


Figure 6.45 Coolant temperature distribution of the initial 9-phase integrated design VSI.

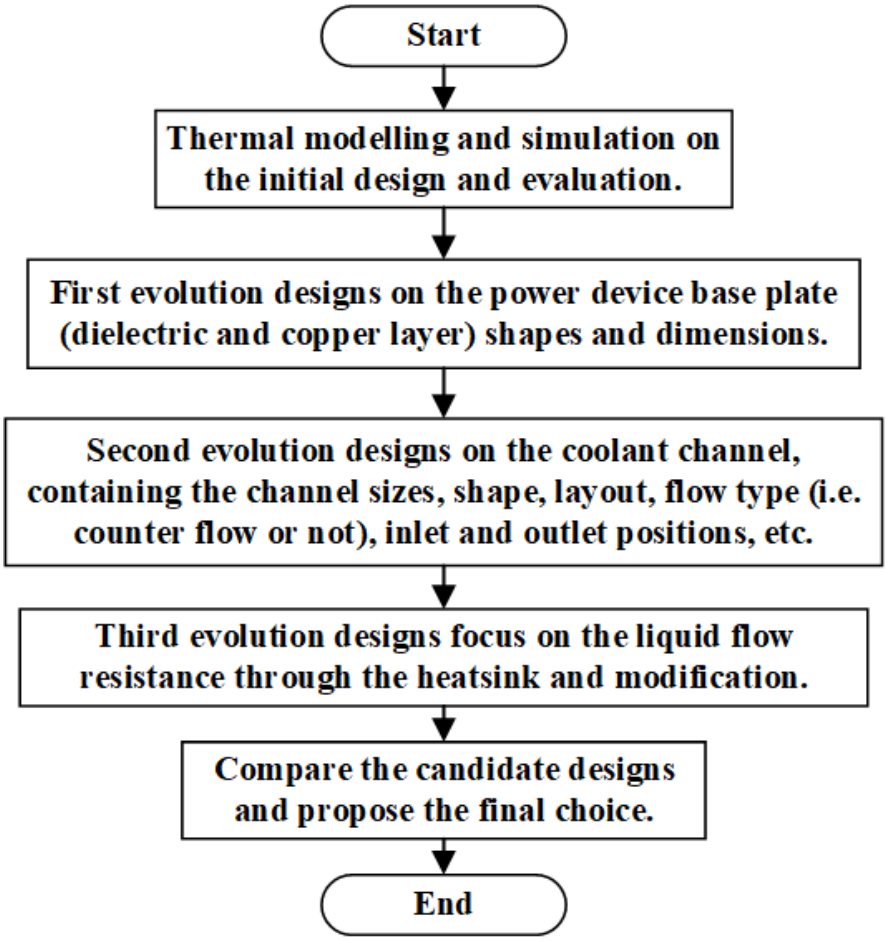


Figure 6.46 Evolution design procedure.

6.4.4 A New 9-phase Integrated Design VSI: First Generation Design 1

In the first generation evolution design 1 (with the abbreviation G1D1, similar for the following design naming) the central parts of the copper layer is hollowed resulting the annulus IGBT module shape. The outer perimeter is extended to the heatsink perimeter and the inner perimeter (due to the hollowing) is set to have the same distance to the inner IGBT die edges with those between the outer perimeter and the outer IGBT die edges as shown in Figure 6.47. The coolant inlet and outlet positions are also set together to enable the full coverage to the IGBT module outer perimeter.

As shown in Figure 6.48 the peak IGBT die temperature is decreased compared with the initial design but still higher than the 9-phase conventional design VSI. The IGBT die temperature distribution balance is not improved soundly while different with the initial design the inner IGBT dies temperatures are higher than those of the outer IGBT dies suggesting the shrinking of the annulus inner perimeter in the next design. The modification of the coolant inlet and outlet positions also leads to the changes to the coolant channel hence its temperature distribution as shown in Figure 6.49.

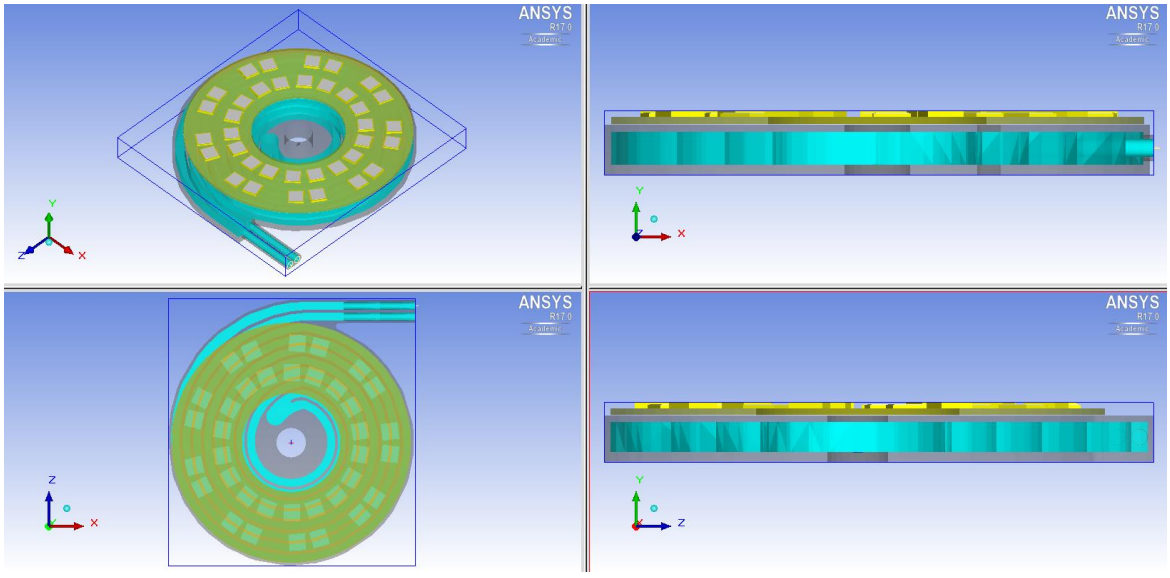


Figure 6.47 Different views of the G1D1.

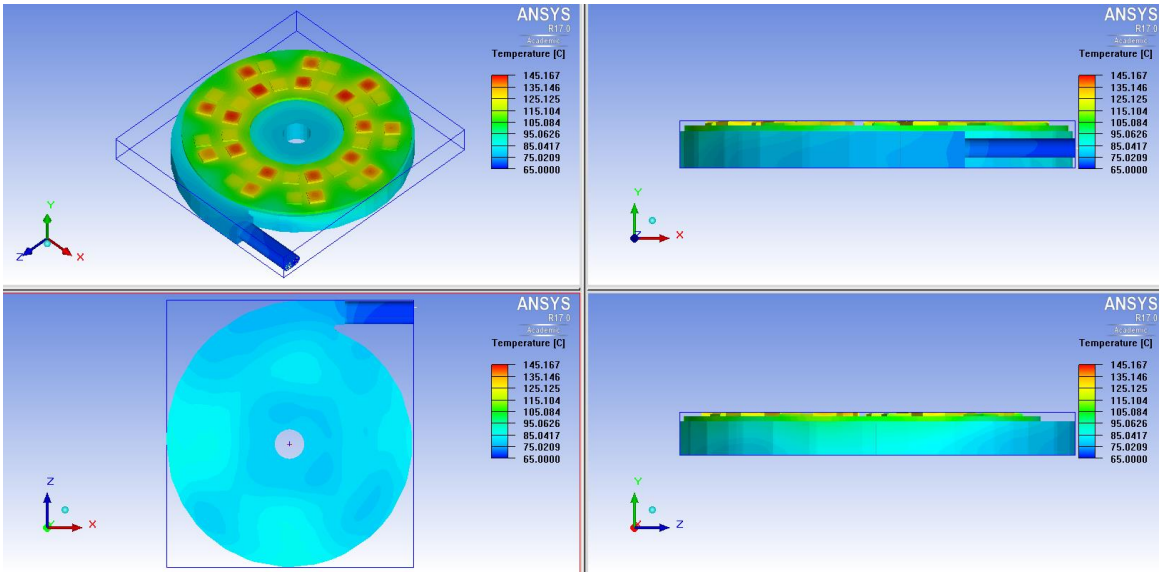


Figure 6.48 Temperature distribution of the G1D1.

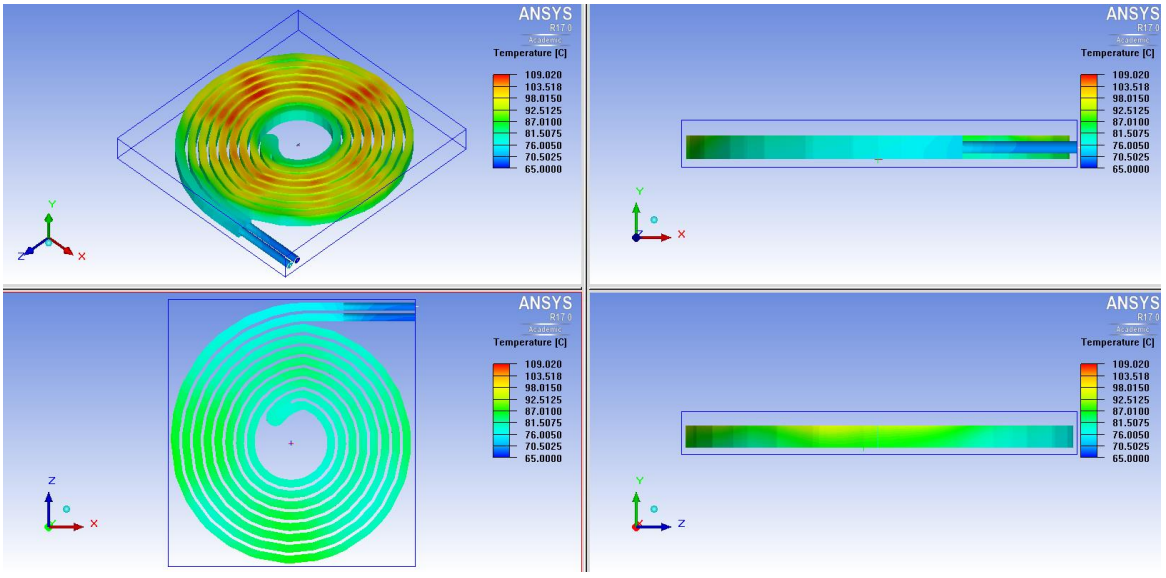


Figure 6.49 Coolant temperature distribution of the G1D1.

6.4.5 A New 9-phase Integrated Design VSI: First Generation Design 2

According to the design suggestion from the previous design the inner perimeter of the copper layers is shrunk to possibly evenly cover all the inner coolant channels as shown in Figure 6.50. This results in the IGBT die peak temperature decrease and more even temperature distribution on the corresponding inner and outer IGBT dies as shown in Figure 6.51. More even and symmetrical temperature distribution can be also observed on the coolant as shown in Figure 6.52.

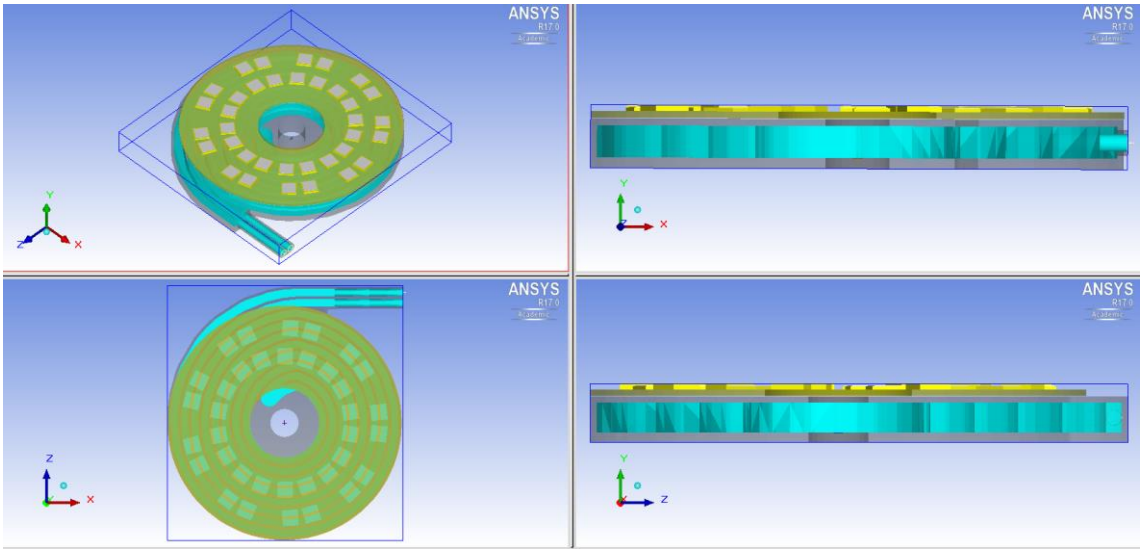


Figure 6.50 Different views of the G1D2.

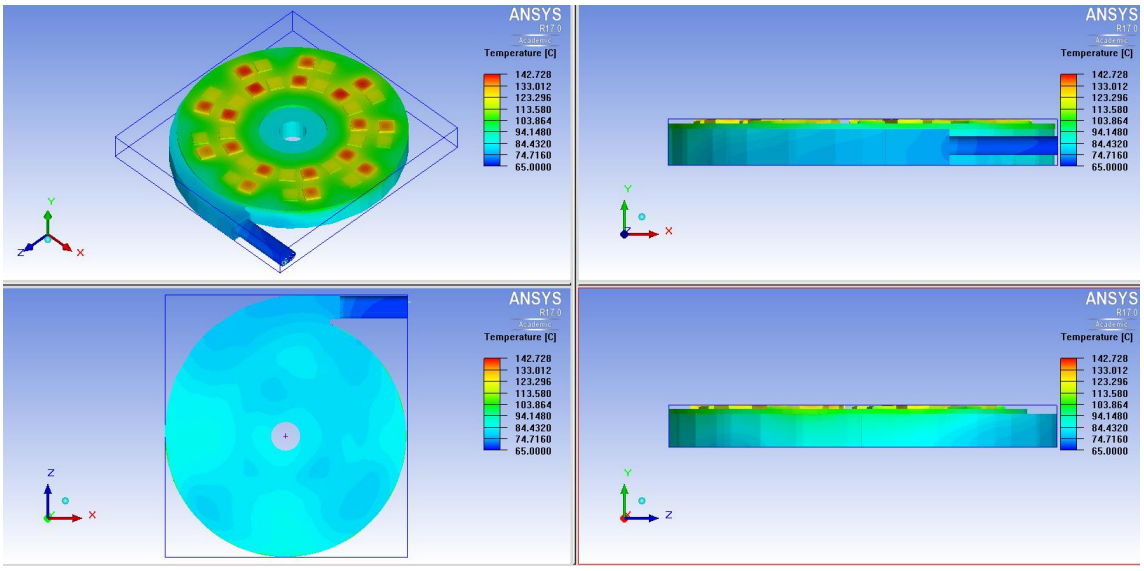


Figure 6.51 Temperature distribution of the G1D2

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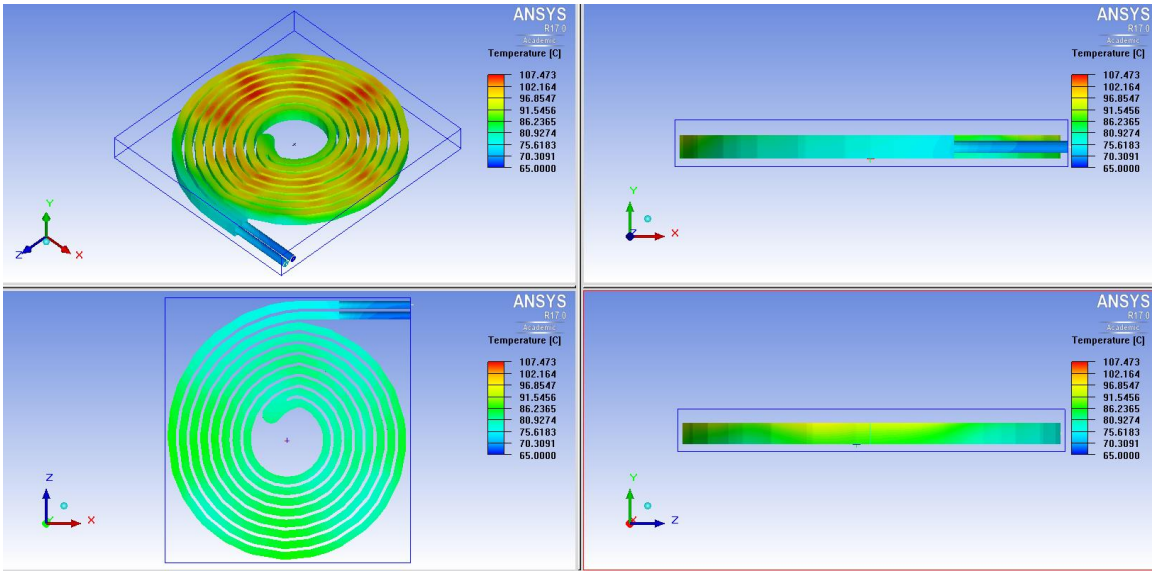

Figure 6.52 Coolant temperature distribution of the G1D2.

6.4.6 A New 9-phase Integrated Design VSI: First Generation Design 3

The coolant inlet and outlet positions are changed in this design to the center of the channels and they are closed on the outer side of the heatsink as shown in Figure 6.53. According to Figure 6.54 and Figure 6.55 it has the similar performance with the previous design.

So far the first evolution designs are finished and the copper layer shape and dimensions are determined achieving the same temperature between the corresponding inner and outer IGBT dies regardless the inlet and outlet positions of the counter-flow coolant channels which verifies the copper layer geometry design. The next evolution designs will focus on the coolant channel modification to achieve more uniform global IGBT dies temperature distribution and lower peak IGBT die temperature.

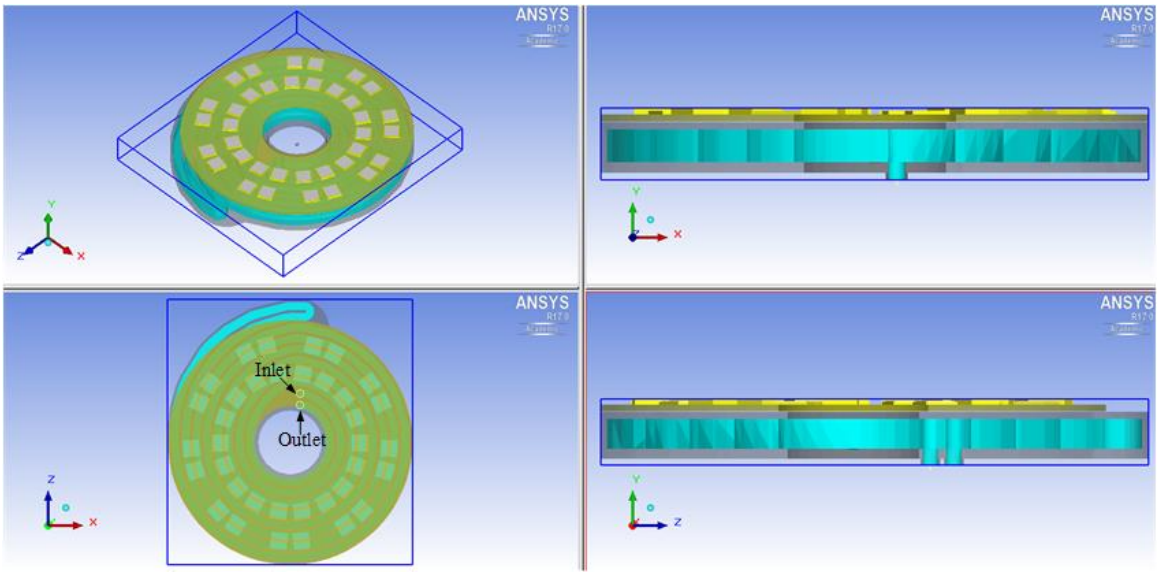

Figure 6.53 Different views of the G1D3.

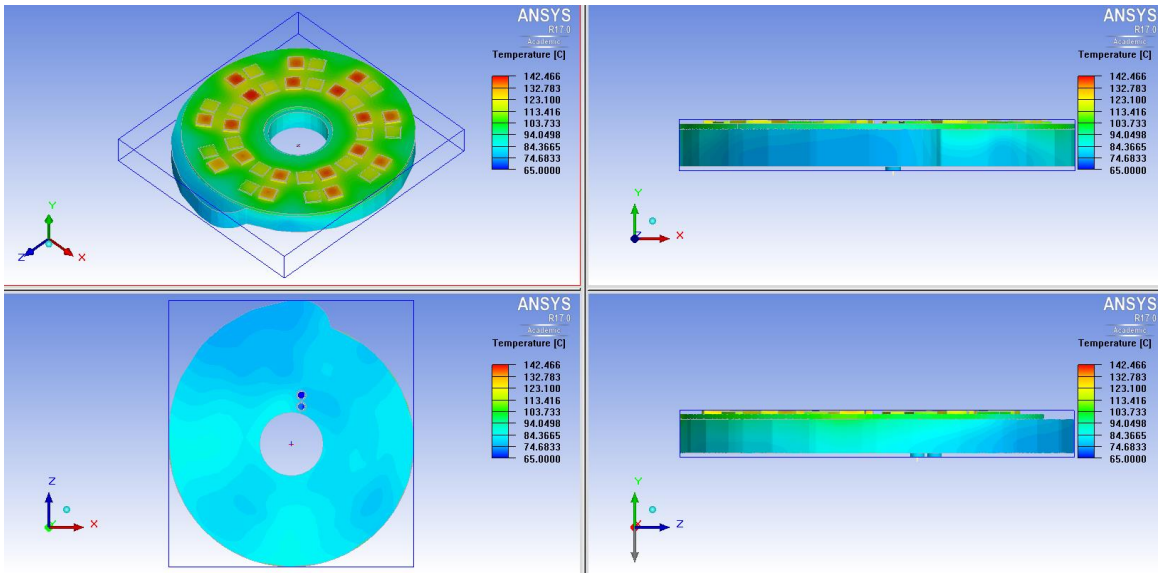

Figure 6.54 Temperature distribution of the G1D3.

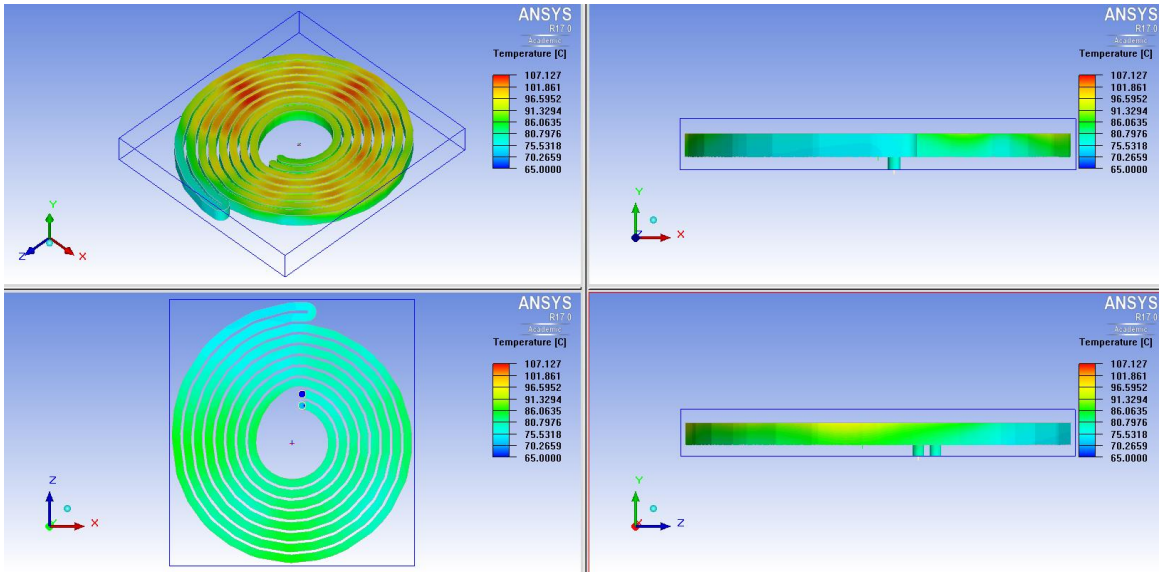

Figure 6.55 Coolant temperature distribution of the G1D3.

6.4.7 A New 9-phase Integrated Design VSI: Second Generation Design 1

In the second generation evolution designs the coolant channels are modified to be thinner (with the channel width half of the previous designs) resulting longer coolant path and larger surface attachment between the coolant and the heatsink hence the better heat transfer characteristics and thermal performance are supposed to be achieved. In this design the coolant inlet and outlet are still located in the center of the heatsink and counter flow is applied as shown in Figure 6.56. Lower IGBT die peak temperature and more uniform IGBT dies temperature distribution than the 9-phase conventional design VSI are achieved as shown in Figure 6.57 which is because of a more evenly and symmetrically distributed coolant channel temperature hence the more efficient heat transfer as shown in Figure 6.58.

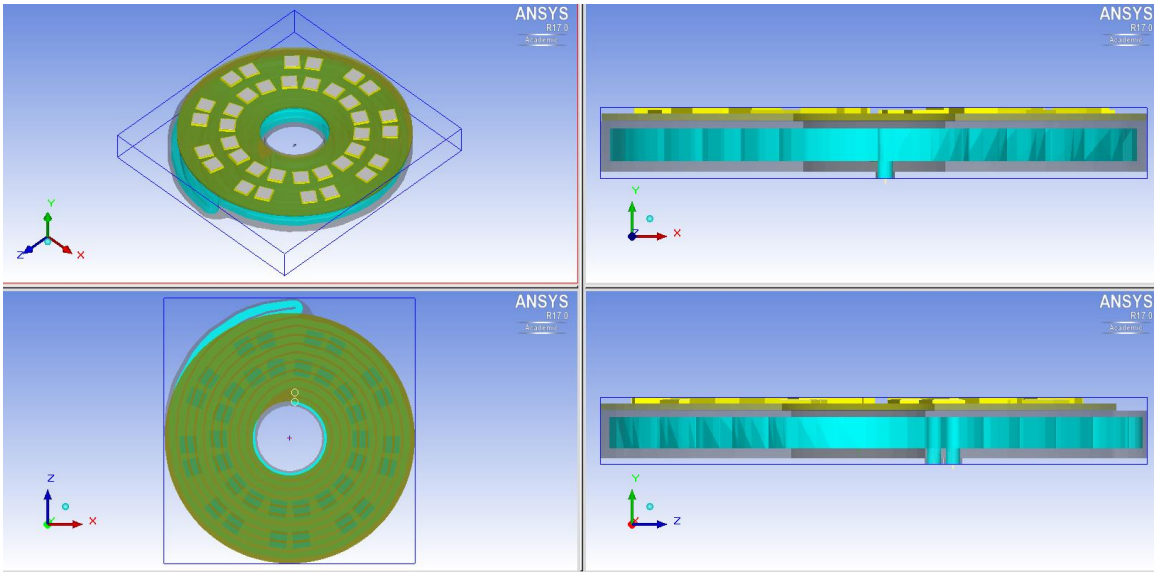

Figure 6.56 Different views of the G2D1.

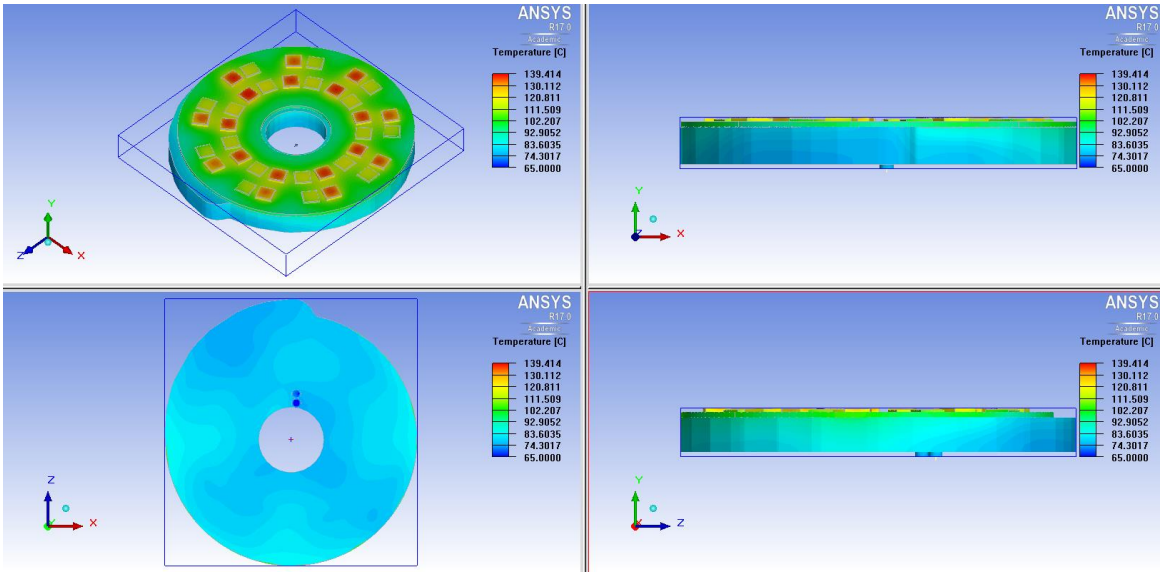

Figure 6.57 Temperature distribution of the G2D1.

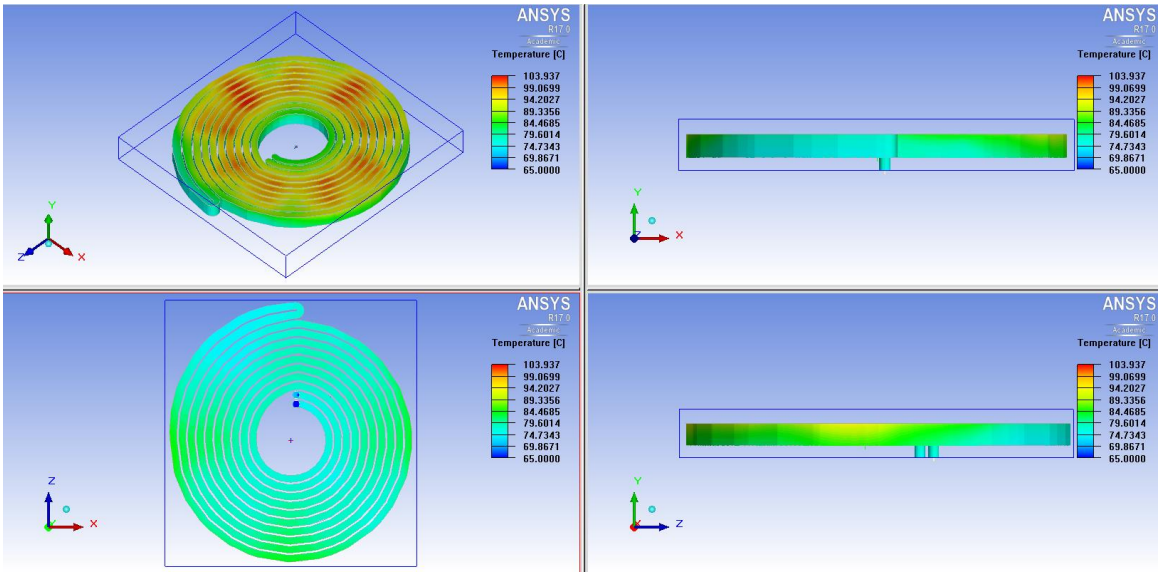

Figure 6.58 Coolant temperature distribution of the G2D1.

6.4.8 A New 9-phase Integrated Design VSI: Second Generation Design 2

In this design the coolant inlet and outlet are positioned in the outer perimeter of the heatsink as shown in Figure 6.59 while the thermal performance does not change soundly compared with the previous design as shown in Figure 6.60 and Figure 6.61.

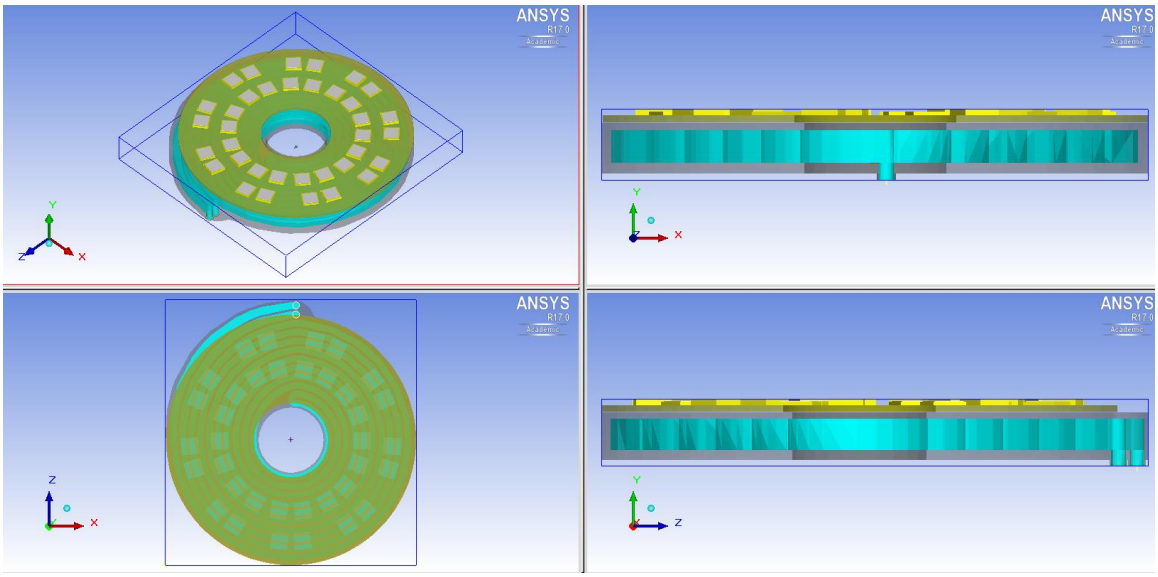

Figure 6.59 Different views of the G2D2.

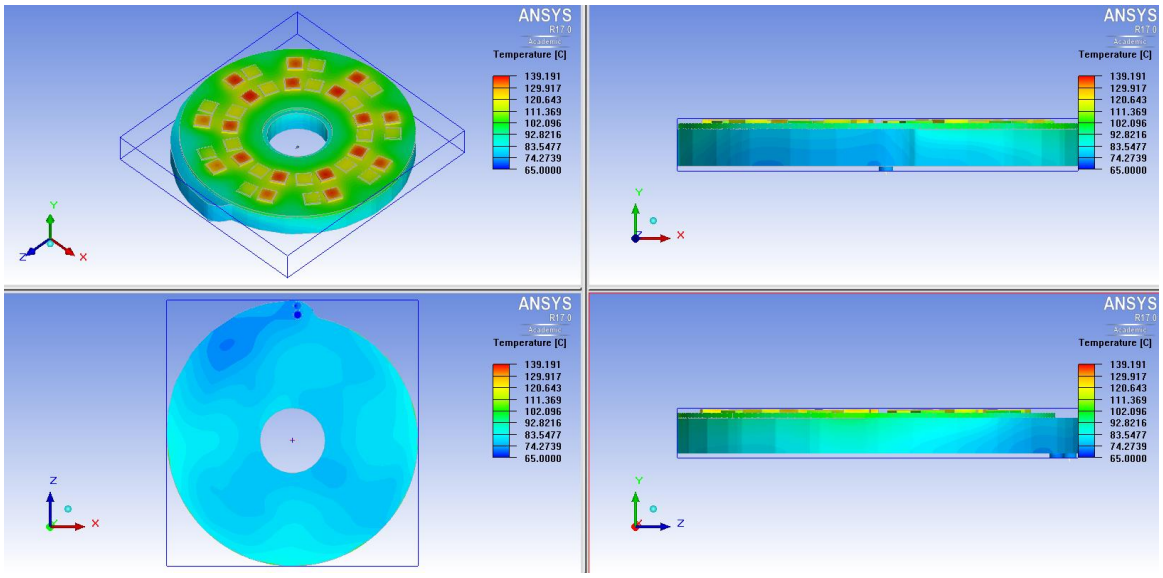

Figure 6.60 Temperature distribution of the G2D2.

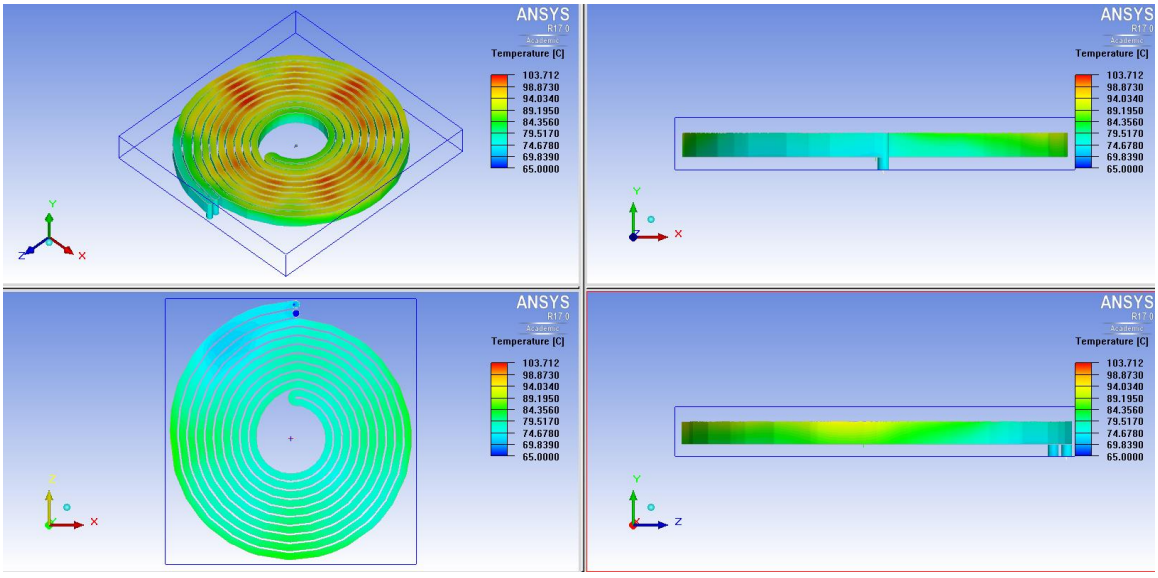

Figure 6.61 Coolant temperature distribution of the G2D2.

6.4.9 A New 9-phase Integrated Design VSI: Second Generation Design 3

From the observation of the previous designs the application of the coolant counter flow results in the thermal coupling between the inlet coolant and the outlet coolant which decreases the cooling efficiency by heating the inlet coolant temperature before the coolant begins the journey underneath the dies. However this discussion is only restricted to this design and whether the counter flow brings the benefits in terms of thermal performance is application specific and could not be general. In this design the counter-flow coolant is not applied with the substitution of the circulating coolant channel with the inlet in the central part of the heatsink and outlet in the outer side as shown in Figure 6.62. The coolant temperature at the inlet is lower than that at the outlet resulting in a temperature gradient from the center to the outer perimeter. Hence the outer dies have higher temperature coolant underneath them than the inner ones while the outer dies larger area attachment for the heat transfer, to some extent, benefits the die temperatures balance. Moreover, the coolant channel layout in this design is more symmetrical resulting nearly the same coolant channel distribution under each IGBT dies. As shown in Figure 6.63 the more balanced IGBT dies temperature distribution and slightly lower peak IGBT die temperature are achieved compared with the previous design. More evenly temperature distribution can also be observed on the coolant channel as shown in Figure 6.64 where the supposed temperature gradient is observable although it is higher affected by the die placement.

As from this design, the thermal performance has good improvement compared with the 9-phase conventional design VSI, another heatsink specification – the inlet and outlet coolant pressure drop is considered from this design (73197 Pa for this design) and compared with that of the 9-phase conventional design VSI heatsink (5720 Pa). Under the same flow volume higher coolant pressure drop means the higher power requirement to drive the coolant thought the heatsink and the higher requirement to the coolant pump.

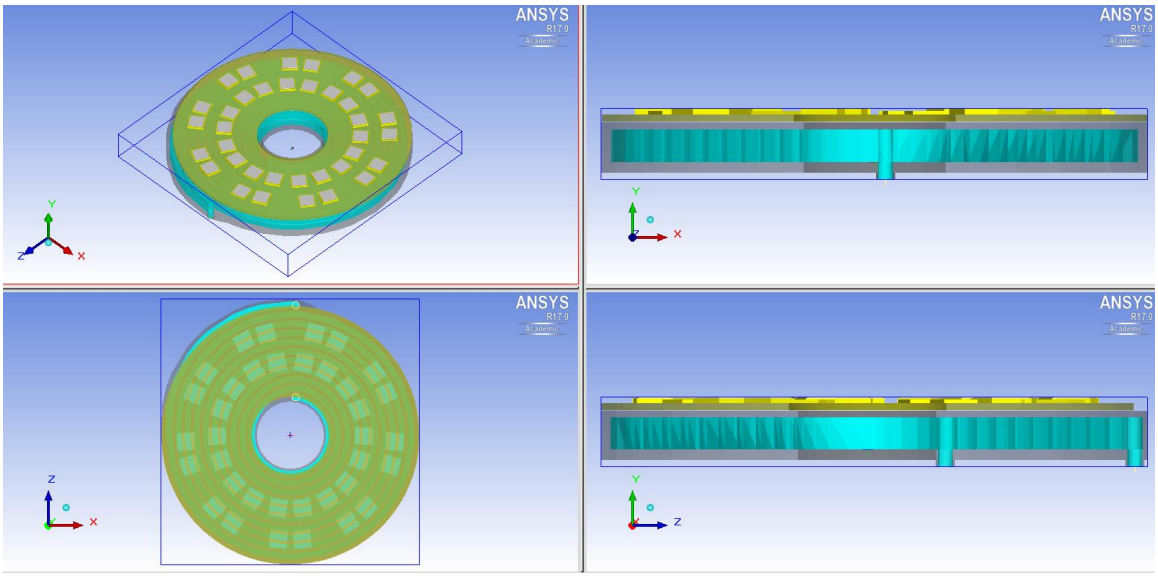

Figure 6.62 Different views of the G2D3.

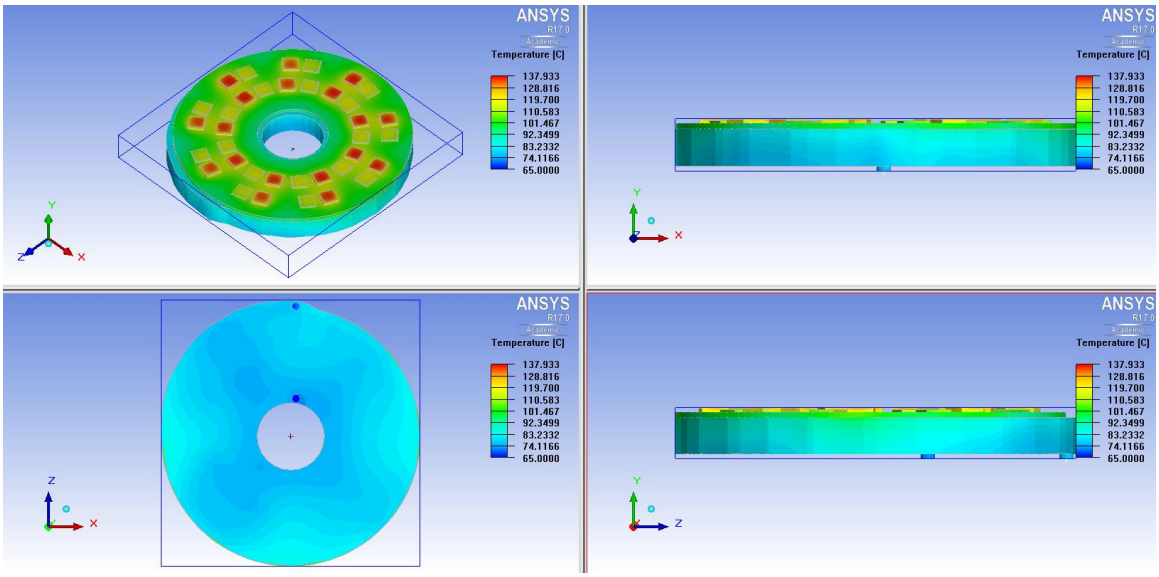

Figure 6.63 Temperature distribution of the G2D3.

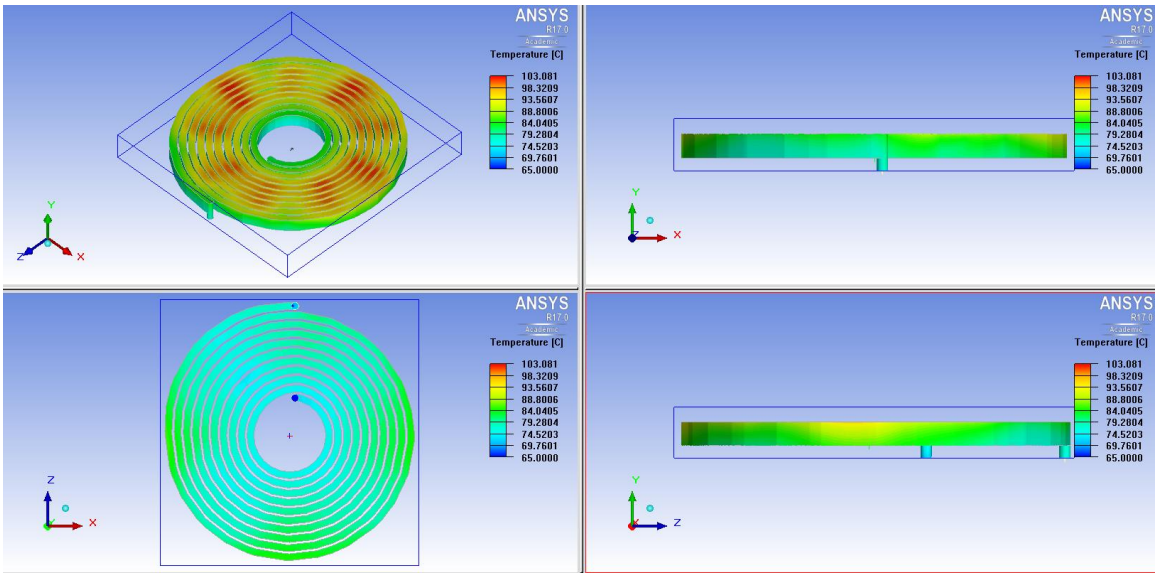

Figure 6.64 Coolant temperature distribution of the G2D3.

6.4.10 A New 9-phase Integrated Design VSI: Second Generation Design 4

Among the precious second evolution designs the one with the best thermal performance (second generation evolution design 3) is chosen, which is followed by the further evolution design by adding another fin in the middle of the coolant channel from the inlet to the outlet. This design will enlarge the total surface attachment between the coolant and the heatsink entity, enhance the thermal coupling among different dies, and refine the coolant channels as shown in Figure 6.65, which results in a sound peak IGBT die temperature reduction and more balanced IGBT die temperature distribution as shown in Figure 6.66. The improved temperature distribution and its gradient can also be observed in Figure 6.67 to support this phenomenon.

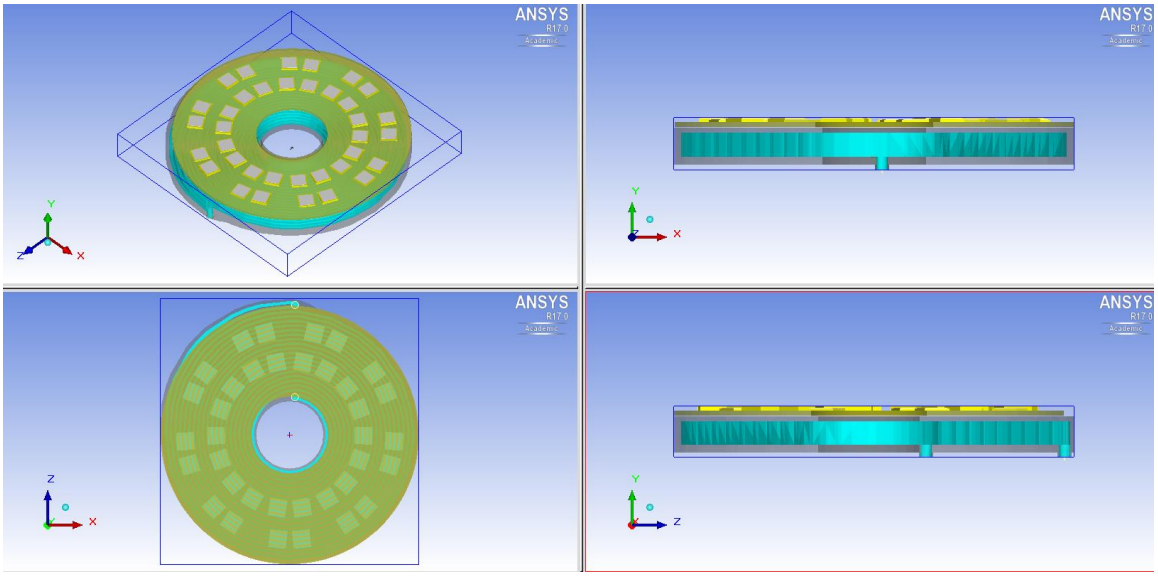

Figure 6.65 Different views of the G2D4.

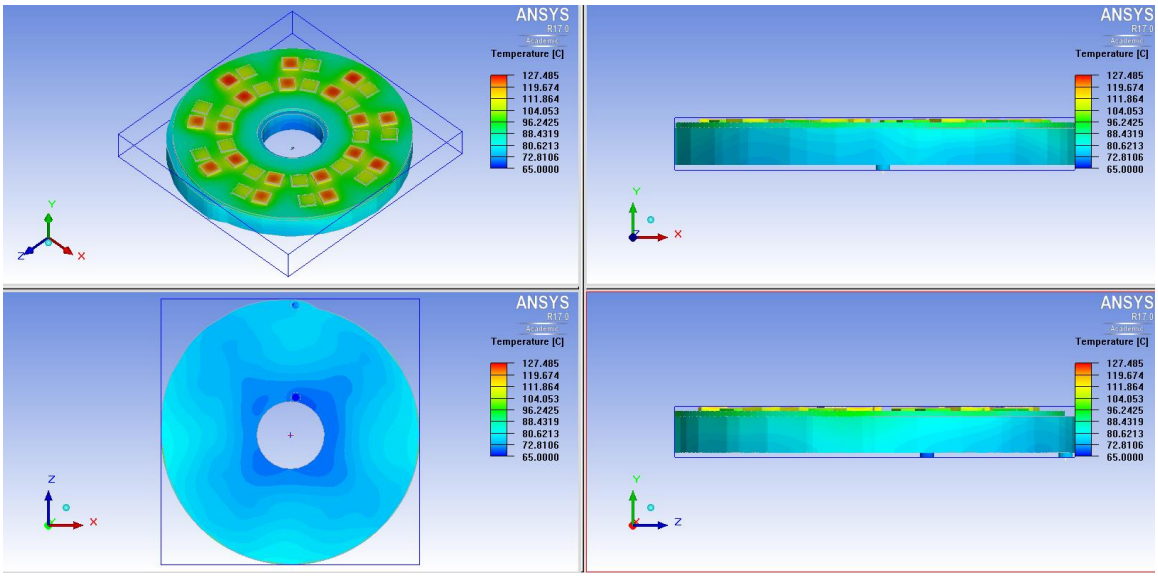

Figure 6.66 Temperature distribution of the G2D4.

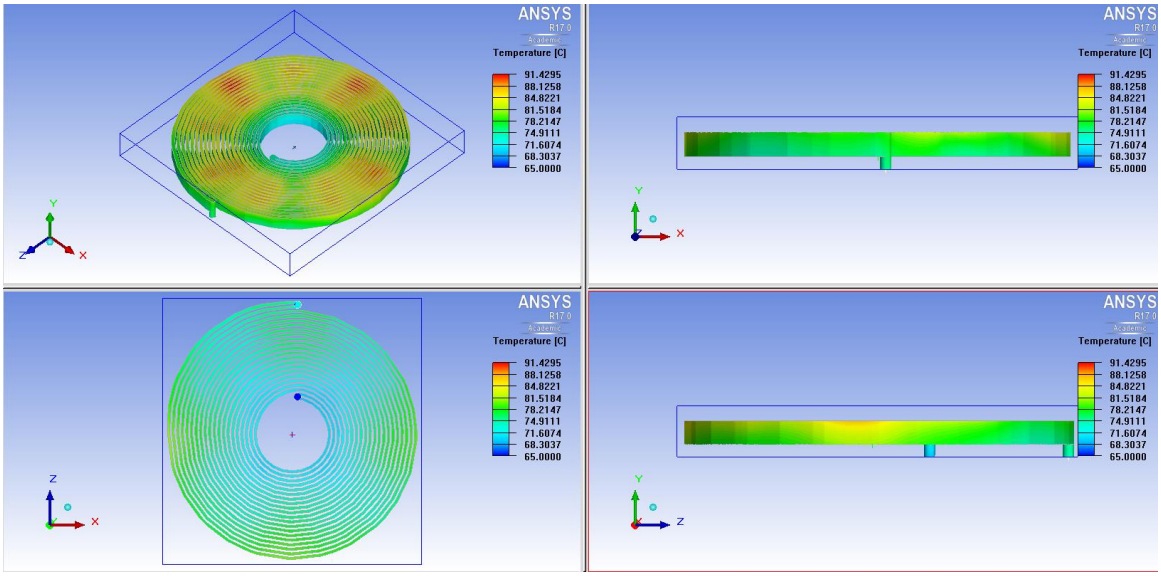

Figure 6.67 Coolant temperature distribution of the G2D4.

6.4.11 A New 9-phase Integrated Design VSI: Third Generation Design 1

The previous designs achieve better thermal performance while the thinner channel design and even the fins in the middle of the channel increase the fluid flow resistance. This results in the rise in the coolant pressure drop and the power requirement to drive the coolant through the heatsink compared with the 9-phase conventional design VSI from the judgement of the coolant channel geometry. Measures are taken in the third generation evaluation designs to decrease the fluid flow resistance as much as possible without changing a lot on the volume and thermal performance with respect to the previous designs (at least should not be worse than the 9-phase conventional design VSI). The design procedures contain shortening the coolant channel length and increasing the coolant channel cross sectional area via the enlargement of its height (twice that of the previous designs) and width (the same width with the dies). Both the IGBT and diode dies are placed, as much as possibly, right on the coolant channel as shown in Figure 6.68. Although the pressure drop between the inlet and outlet is decrease to 4110 Pa, even lower than the benchmark cooling system (5720 Pa), the thermal performance is not promising as shown in Figure 6.69 and Figure 6.70 compared with the 9-phase conventional design. This suggests the further thermal performance improvement design based on this design via the enlargement of the attached surface between the heatsink and the coolant.

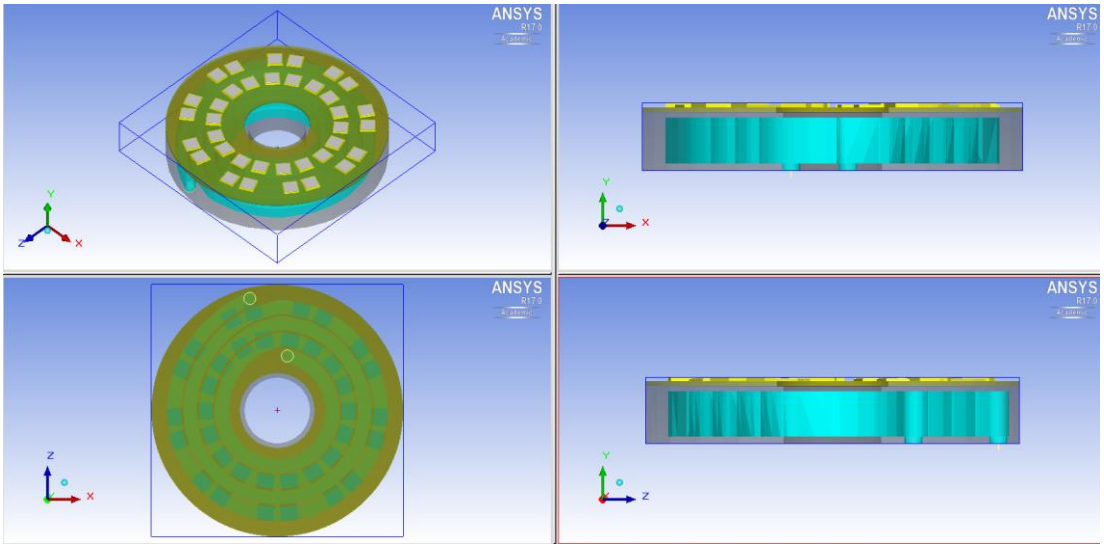

Figure 6.68 Different views of the G3D1.

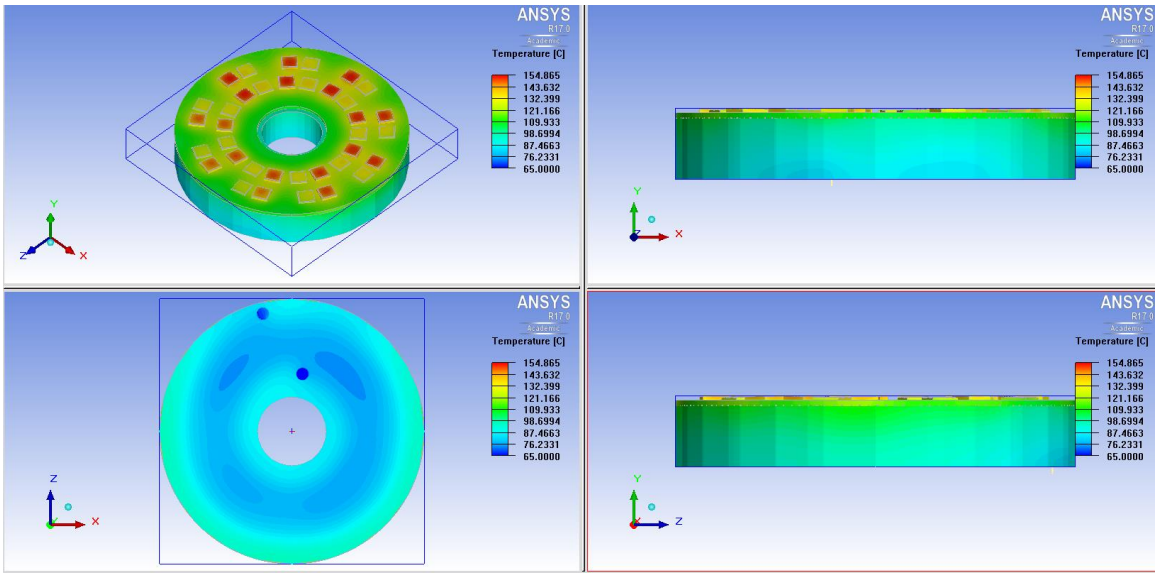

Figure 6.69 Temperature distribution of the G3D1.

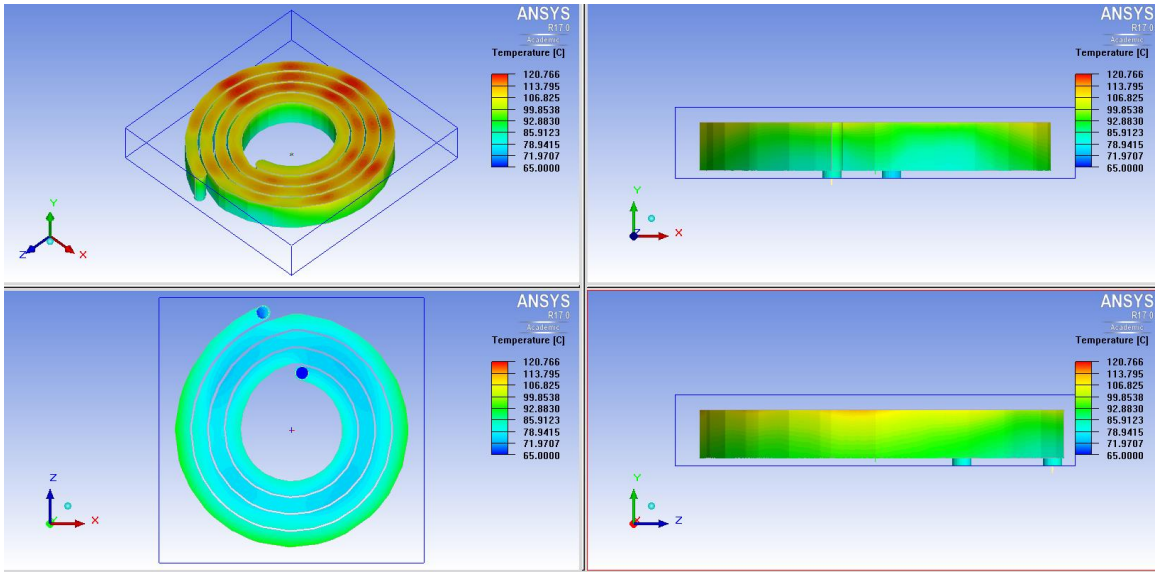

Figure 6.70 Coolant temperature distribution of the G3D1.

6.4.12 A New 9-phase Integrated Design VSI: Third Generation Design 2

According to the suggestion from the previous design, the fin are designed to be in the middle of the coolant channel as shown in Figure 6.71 increasing the attachment surface between the heatsink entity and the coolant, enhancing the heat transfer from the dies to the coolant, and reinforcing the thermal coupling among different dies. Better thermal performance than the G3D1 as well as the 9-phase conventional design VSI can be observed as shown in Figure 6.72 and Figure 6.73. While a slight increase occurs on the coolant inlet and outlet pressure drop 7523Pa, a little higher than the 9-phase conventional design 5720 Pa.

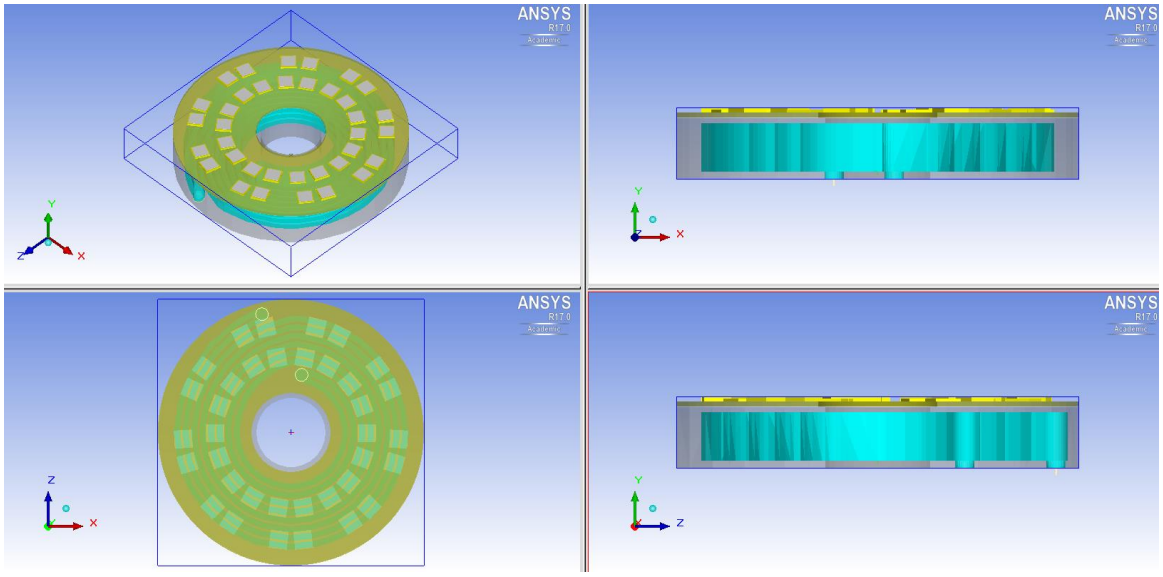

Figure 6.71 Different views of the G3D2.

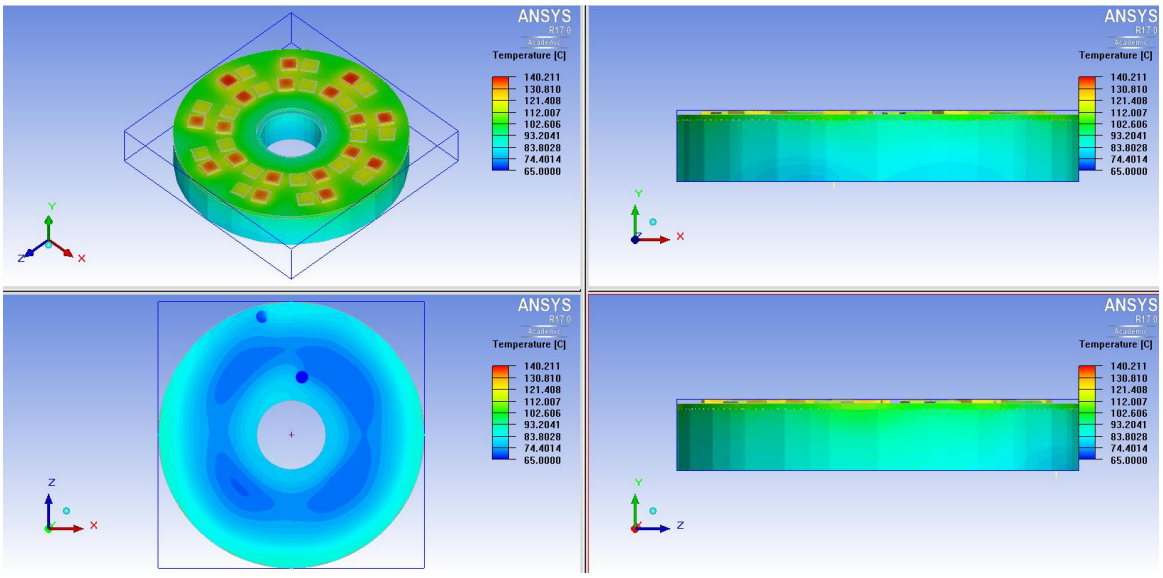

Figure 6.72 Temperature distribution of the G3D2.

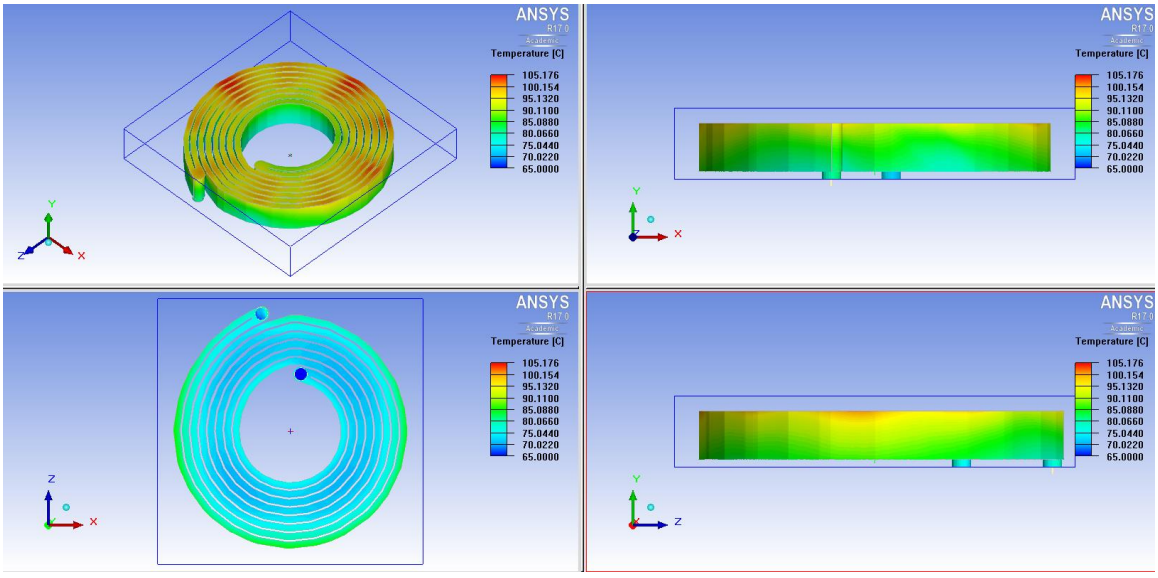

Figure 6.73 Coolant temperature distribution of the G3D2.

6.4.13 9-phase Design Comparisons and Final Decision

Three candidates of the 9-phase integrated evolution designs are selected, G2D3, G2D4 and G3D2 whose specifications and thermal performances are compared with the 9-phase conventional design VSI (with the abbreviation 9PC) and the 3-phase benchmark VSI (with the abbreviation 3PB). The best choice of the 9-phase integrated design VSIs is proposed after the comparison. As the thermal performance between the 3PB and 9PC is compared in Chapter 6.4.1 showing the advantages of 9PC because of the alleviation and almost elimination of parallel dies current imbalances hence the power loss differences, the comparison between the proposed 9-phase integrated design VSI and 3PB only focuses on the VSI volumes. The VSI volume comparison considers the sum of heat sink, DC-link capacitor and IGBT module volumes as these three parts dominate the VSI total volume in traction machine VSIs due to [130]. While in the real application, the case and mechanical part of VSIs account much volume that could be solved in a mechanical and material view. The VSI specifications of 3PB, 9PC and three candidates of the 9-phase integrated design VSIs are shown in Table 6.10.

Figure 6.74 shows 18 IGBT dies temperatures (the average for each IGBT dies) of different 9-phase designs, and the die temperature standard deviation is shown in Figure 6.75. All the 9-phase integrated design candidates have both the lower peak IGBT die temperature and more uniform IGBT dies temperature distribution compared with the 9-phase conventional design VSI, better thermal performances. Moreover, the heatsink, IGBT module, DC-link capacitor volumes and their sum are shown in Figure 6.76 for different 9-phase designs. Similarly, the heatsink weights among these designs are also compared with the results shown in Figure 6.77. Finally, the heatsink coolant driving power is the multiplication of the pressure drop and the coolant flow rate, and the different coolant inlet outlet coolant pressure drop results in the different power requirements for the 9-phase designs as shown in Figure 6.78. G2D4 requires the highest power (37.8 W) 37 times of the 9PC (1 W). The G2D3 and G3D2 are in the middle 12.2 W and 1.3 W respectively.

The consideration focuses on the designs with lower volumes compared with the 9PC – G2D4 and G2D3 among which G2D4 has the best thermal performance while requires

highest heatsink coolant driving power. Although the G2D4 thermal performance, 15 °C lower peak IGBT die peak temperature and the lowest dies temperatures standard deviation, benefits the IGBT life time and reliability, the over cooling compared to 9PC is the not necessary. Comparatively, G2D3 improves the thermal performance in a proper degree and requires more reasonably coolant driving power increase (11.2 W more than 9PC. still negligible compared to the inverter power loss). Consequently, G2D3 is the compromised choice as the 9-phase integrated design VSI. The sums of heat sink, DC-link capacitor and IGBT module volumes are compared under G2D3 and 3PB as shown in Figure 6.79. There are 1.2 litres volume decrease in G2D3 than 3PB and hence the improved power density. Compared with 3PB, the G2D3 design also decreases the heatsink mass significantly by 43% as shown in Figure 6.80.

The assembling of the VSI and traction machine is shown in Figure 6.81 where the black cylinder in the central hollow part (diameter 65 mm) of the heat sink indicates the DC-link capacitor (diameter 60 mm, thickness 17 mm and volume 0.48 litre) and the green cylinder the traction machine. The power terminal connection between the VSI and traction machine are the special shape designed copper bars with the insulation through the space between the DC-link capacitor and heatsink hollow hole. 10 mm gap is between the VSI and the traction machine for the assembling purpose.

Table 6.10 Different VSI designs specifications.

Design index	3PB	9PC	G2D3	G2D4	G3D2
Heatsink length (mm)	196	196	NA	NA	NA
Heatsink width (mm)	320	320	NA	NA	NA
Heatsink thickness (mm)	23.3	23.25	23.25	23.25	38.25
Heatsink inner diameter (mm)	NA	NA	65	65	65
Heatsink outer diameter (mm)	NA	NA	250	250	250
Heatsink volume (litre)	1.46	1.46	1.09	1.09	1.75
Heatsink aluminum volume (litre)	1.04	1.04	0.59	0.74	1.04
Heatsink aluminum weight (kg)	2.82	2.82	1.59	1.99	2.81
Coolant volume (litre)	0.42	0.42	0.5	0.35	0.71
Coolant weight (kg)	0.45	0.45	0.54	0.38	0.77
Heatsink weight with coolant (kg)	3.27	3.27	2.14	2.38	3.58
Coolant pressure drop (Pa)	5720	5720	73197	226577	7523
Coolant driving power (W)	1	1	12.2	37.8	1.3
IGBT module volume (litre)	0.88	0.88	1.07	1.07	1.07
DC Cap volume (litre)	1.45	0.48	0.48	0.48	0.48
Inlet coolant temperature (°C)	65	65	65	65	65
Outlet coolant temperature (°C)	72	72	72	72	72
Peak IGBT die temperature (°C)	NA	142	138	127	140
Lowest IGBT die temperature (°C)	NA	116	120	110	122
IGBT die temperature standard deviation	NA	3.1	1.3	0.9	1.4

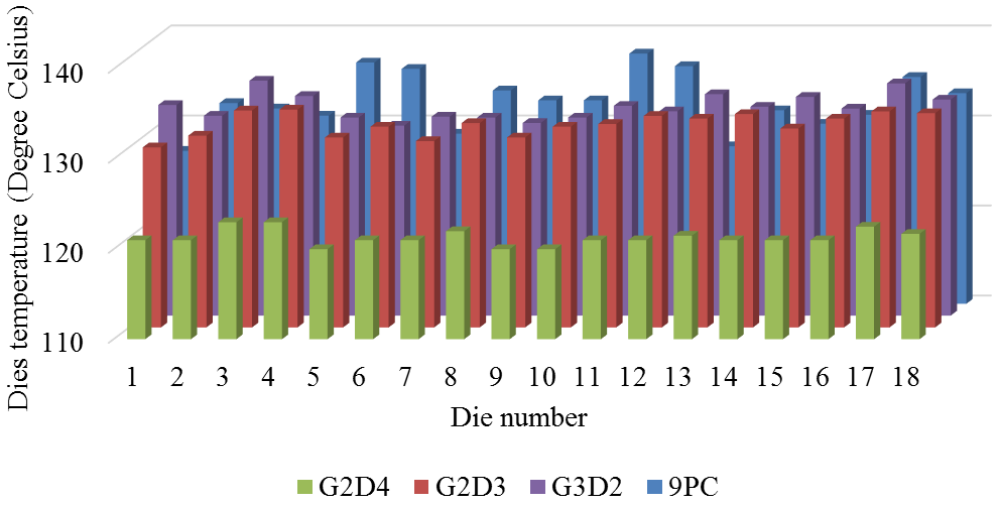

Figure 6.74 IGBT dies temperatures for different 9-phase VSI designs.

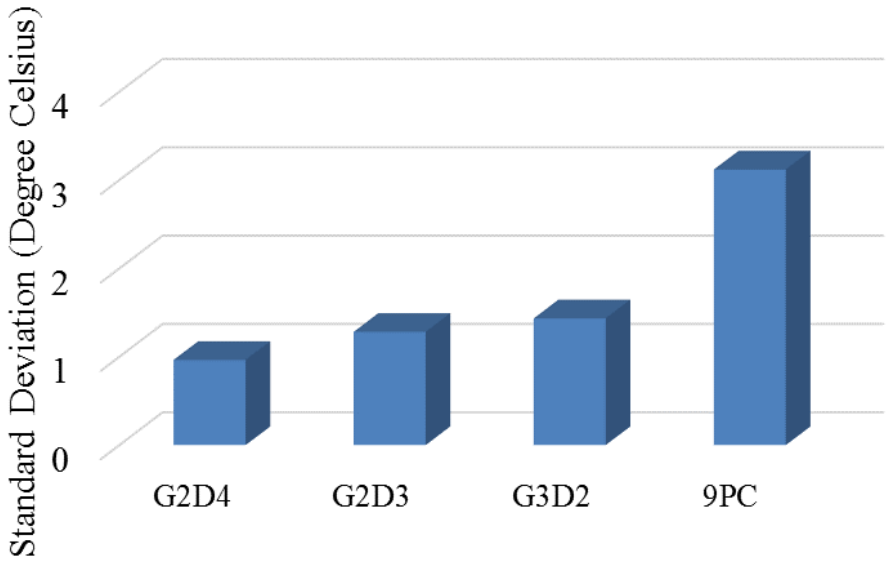

Figure 6.75 IGBT dies temperature standard deviations for different 9-phase VSI designs.

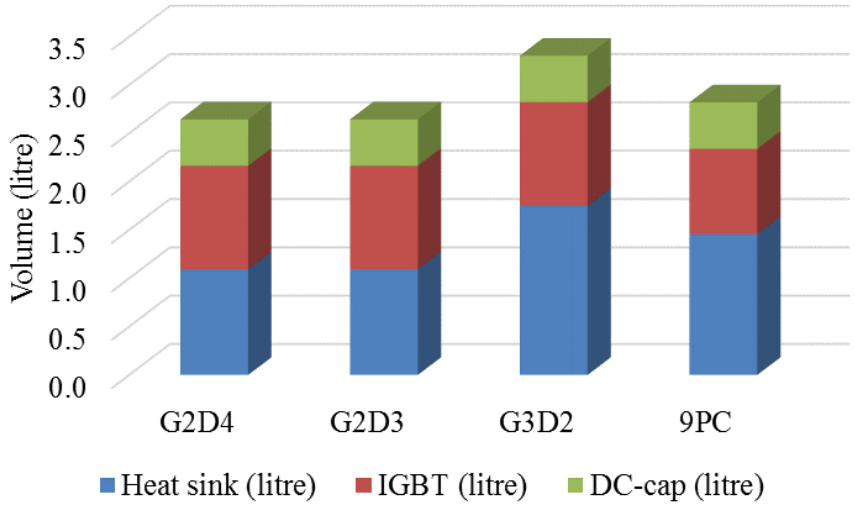

Figure 6.76 Components volumes comparison for different 9-phase VSI designs.

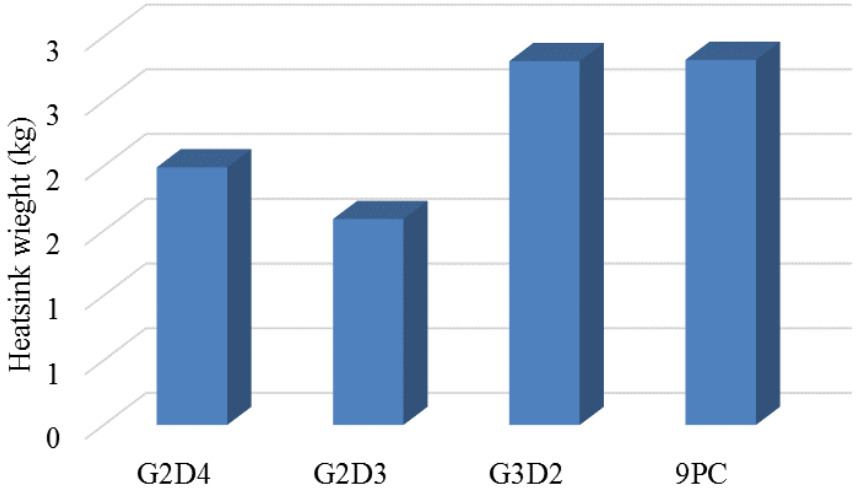

Figure 6.77 Heatsink weight comparison for different 9-phase VSI designs.

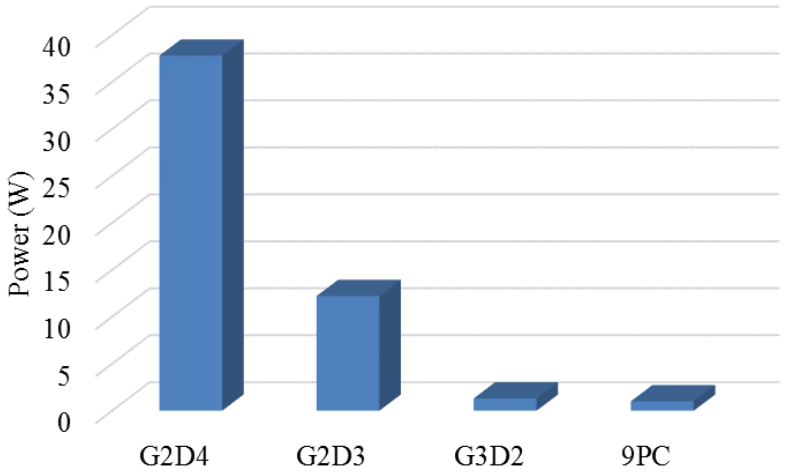

Figure 6.78 Heatsink coolant driving power for different 9-phase VSI designs.

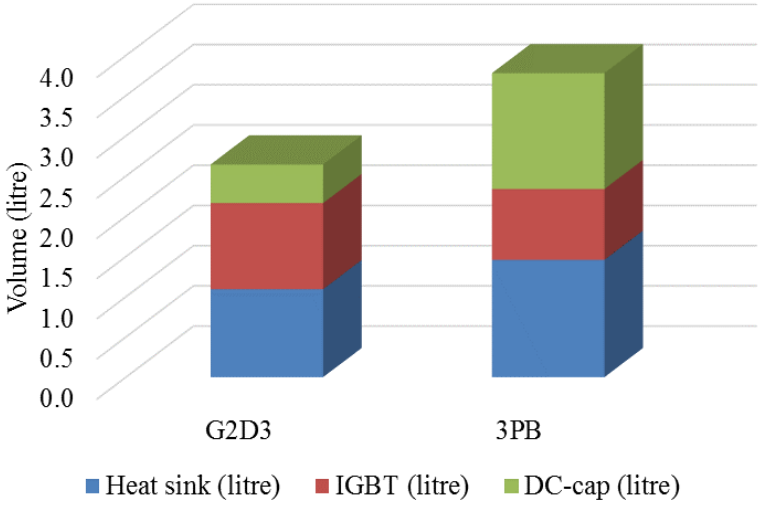

Figure 6.79 Components volumes comparison between the final chosen 9-phase integrated design VSI (G2D3) and the 3-phase benchmark VSI.

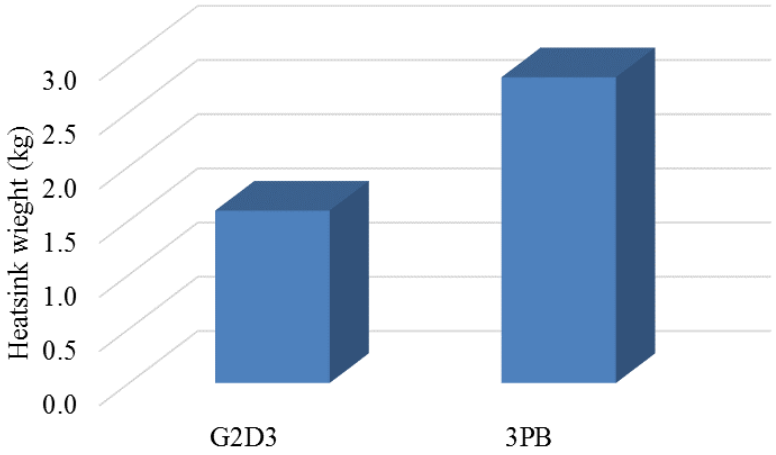

Figure 6.80 Heatsink weight comparison between the final chosen 9-phase integrated design VSI (G2D3) and the 3-phase benchmark (3PB) VSI.

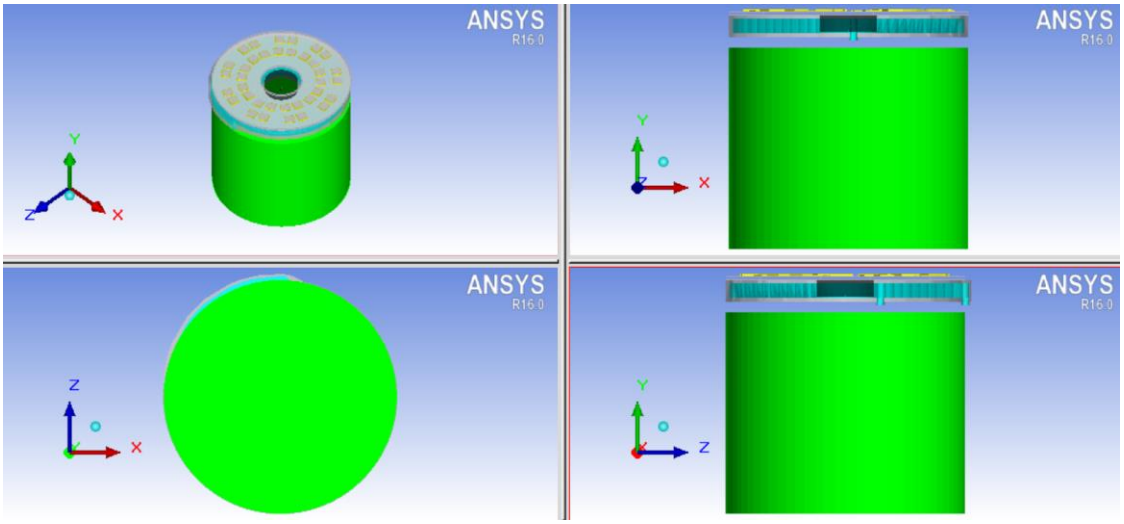

Figure 6.81 Integrated VSI and traction machine assembling.

6.4.14 Comparison of 18-phase, 27-phase and 36-phase Integrated Design VSIs

Compared with the benchmark, the 9-phase conventional design VSI improves the VSI thermal performance via the non-paralleled connection of IGBT dies avoiding the IGBT dies current imbalance and hence the power loss deviation. The 9-phase integrated design VSI further improves the thermal performance and the machine drive compactness. Moreover, according to the figures and discussion on page 297 in [89], under the same heat source power loss and dissipating area the divided power source areas (peak temperature 96.2 °C) have 5.2 °C lower peak temperature than the single area (peak temperature 101.4 °C). Splitting the single die into several ones and controlling the current individually can be achieved by higher phase number multiphase phase VSIs. Based on that the single IGBT and diode dies can be divided into 2, 3 and 4 individuals, and compose 18-, 27- and 36-phase VSIs, which will result in better thermal performance. That will be modelled and analyzed.

The 18-phase, 27-phase and 36-phase integrated design VSIs are proposed and they have the same heat sink and base plate (the copper layer) with the 9-phase integrated design VSI. The IGBT and diode dies are placed on the same area with that in the 9-phase integrated design VSI, and the total IGBT and diode die semiconductor die areas are the same resulting the smaller die sizes and more die numbers as shown in Table 6.11. Under the equilibrium power output, the sums of phase RMS current are same in 9-phase, 18-phase, 27-phase and 36-phase systems resulting the same total IGBT and total diode dies power losses under the assumption that both the conduction and switching losses are proportional to the current magnitude. The IGBT and diode dies and their power loss specification is shown in Table 6.11 and all the IGBT dies have the same power loss due to the non-paralleled connection, the same for the diode dies.

The temperature distribution for 18-, 27-, and 36-phase integrated design VSIs are shown in Figure 6.82, Figure 6.83 and Figure 6.84. The 18-phase integrated design VSI has 2.3% lower IGBT die peak temperature (134.8 °C) than the 9-phase one (137.9 °C), and the 27-phase and 36-phase one has the lowest value (133.8 °C, 3.0% lower than the 9-phase one). The temperature distribution results indicate the smaller heat sink volumes for the same

IGBT dies peak temperature, 2.25% lower in 18-phase one and 3.0% lower in 27- and 36-phase ones, compared with the 9-phase integrated VSI.

Furthermore, inheriting the research conclusion in Chapter 4, the volume sum of heat sink, DC-link capacitor and IGBT modules are compared among the integrated design 9-, 18-, 27- and 36-phase VSIs (named as 'G2D3' '18PH' '27PH' and '36PH' respectively) and the benchmark (named as '3PB') as shown in Table 6.12 and Figure 6.85. Notes should be made here that the DC-link capacitors sizes in the 9-, 18-, 27- and 36-phase integrated design VSIs are correspondingly based on 3x 3-, 6x 3- and 9x 3-phase SVM group based interleaved triangular carrier and 4x paralleled 9-phase IPPM-VSI. By increasing the phase number, the VSI volume is decreased significantly compared with the benchmark and the 9-phase, 27-phase and 36-phase VSIs volumes account the benchmark by 70%, 63%, 61% and 60%. Therefore, the VSI power density can be significantly increased by the implementation of multiphase VSIs.

Table 6.11 IGBT and diode dies in 9-, 18-, 27- and 36-phase VSIs.

VSI phase number	IGBT die size (mm x mm)	IGBT die number	IGBT die loss (W)	Diode die size (mm x mm)	Diode die number	Diode die loss (W)	Total loss (w)
9	15x 15	18	166.4	15x 15	18	74.3	4334
18	10.6x 10.6	36	83.2	10.6x 10.6	36	37.2	4334
27	8.7x 8.7	54	55.5	8.7x 8.7	54	24.8	4334
36	7.5x7.5	72	41.6	7.5x 7.5	72	18.6	4334

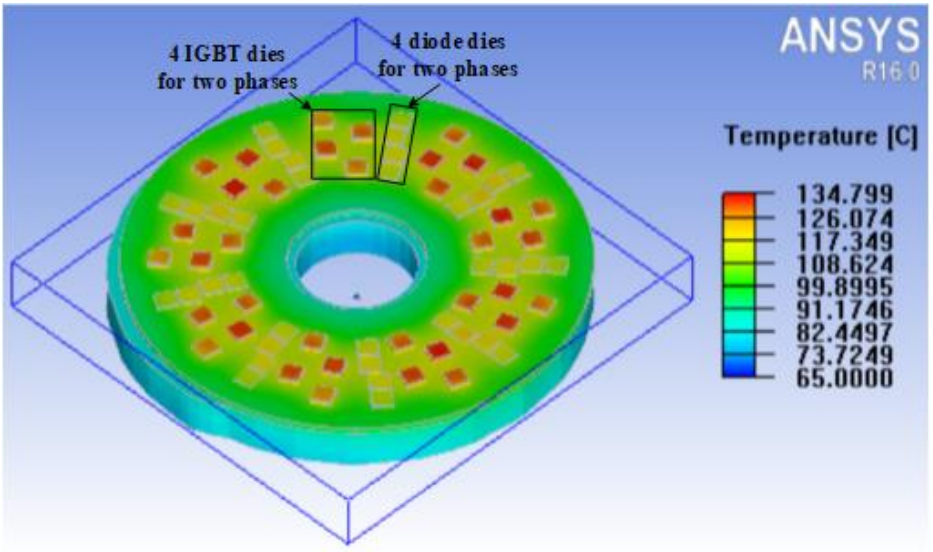

Figure 6.82 Temperature distribution of the 18-phase integrated design VSI.

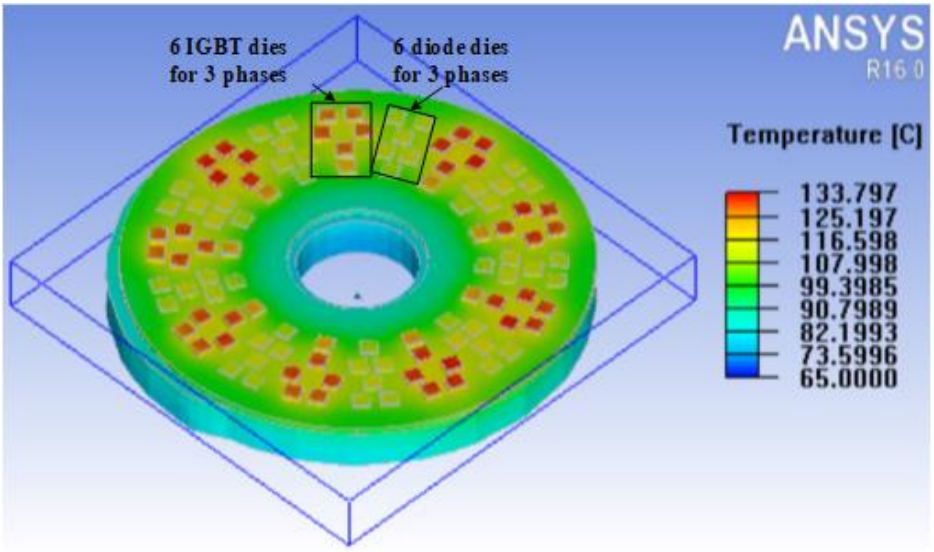

Figure 6.83 Temperature distribution of the 27-phase integrated design VSI.

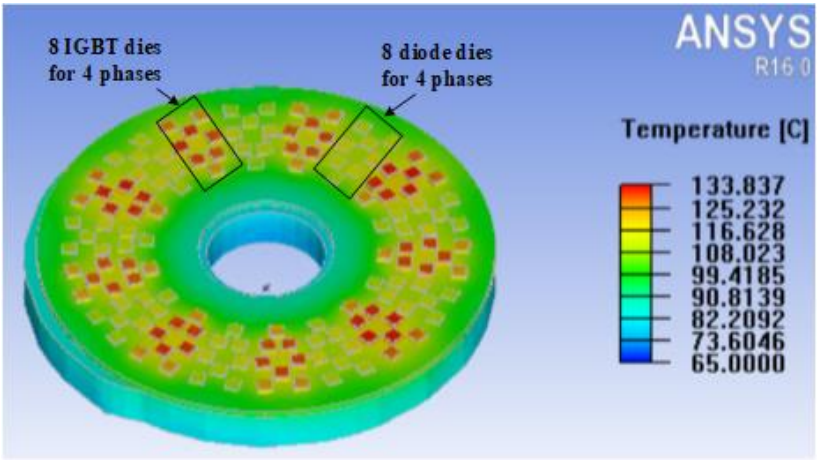

Figure 6.84 Temperature distribution of the 36-phase integrated design VSI.

Table 6.12 Heat sink, IGBT module and DC capacitor volumes sum among different VSIs.

	3PB	9PI	18PI	27PI	36PI
IGBT	0.88	1.07	1.07	1.07	1.07
Heat sink	1.46	1.09	1.06	1.06	1.06
DC Cap	1.44	0.48	0.26	0.17	0.12
Total (litre)	3.78	2.64	2.39	2.30	2.25

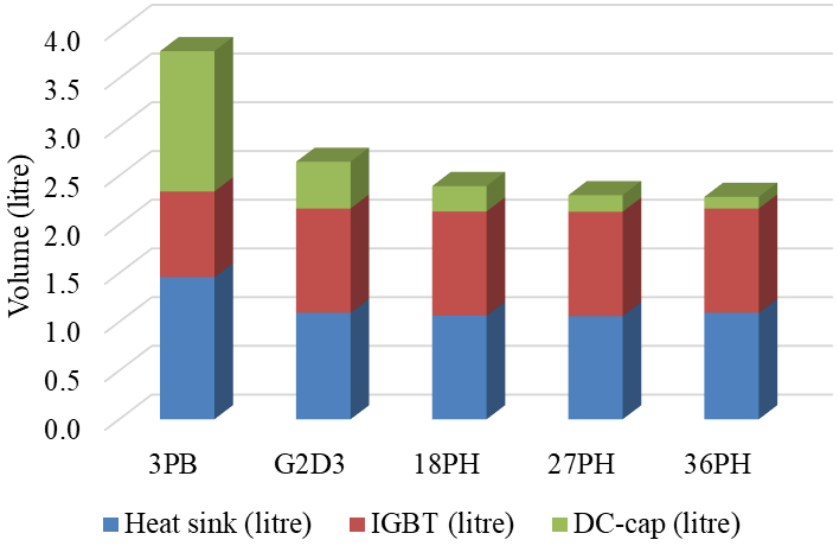

Figure 6.85 Heat sink, IGBT module and DC capacitor volumes sum among different VSIs.

6.5 Summary

In this chapter, the mechanisms of the current and hence power loss imbalances in parallel-connected power semiconductor devices, and the consequences are investigated, followed by the solutions. After comparing different solutions, the multiphase topology is selected as the best one and proposed in the EV traction system VSIs. The thermal performance is studied and compared under different degree power loss imbalances among the parallel-connected IGBT dies in the benchmark 3-phase VSI. A 9-phase conventional design VSI is introduced eliminating the IGBT die parallel connection and hence the power loss imbalance, which improves the thermal performance. The 9-phase integrated design VSI is proposed and has the significant improvements on the thermal performance, power density and compactness compared with the benchmark. Finally, the 18-phase, 27-phase and 36-phase VSIs are designed and modelled, and their thermal performances are evaluated generalizing the conclusion that the implementation of multiphase VSI improve the thermal performance by the higher feasibility to control the IGBT dies current individually and split the single die into several ones to spread the heat source. Furthermore, continuing the DC-link investigation in Chapter 4 the volume sums of heat sink, DC capacitor and IGBT module are compared that the implementation of multiphase VSI significantly decreases the VSI volume.

No previous research has introduced the thermal modelling procedure and thermal performance investigation method on multiphase VSIs, the multiphase VSI integrated evolution design procedure and the performances and characteristics evolution with the increasing phase number VSIs ,which are the novelties and contributions of this chapter.

Chapter 7

Conclusions, Future Research Work and Publications

7.1 Conclusions

Different space vector modulations (SVMs) for multiphase voltage source inverters (VSIs) are studied. The multiphase VSIs with balanced group based SVMs have low output phase current harmonic contents and high DC-link voltage utilization. This is validated experimentally via the 3x 3-phase and 9-phase SVM machine drive systems. The best choice for the 9-phase machine drive systems is the 3x 3-phase SVM. Unbalanced group based SVM concept is proposed as a new option for the group based SVM family. SVMs implementing only the outermost basic space vectors increase the DC-link voltage utilization while introduce some detrimental effects of phase output current harmonics. The study method and procedure can be generalized to other phase number multiphase VSIs.

The investigation method for the DC-link requirements, e.g. RMS current ratings and capacitance, are proposed for arbitrary phase number VSIs, based on which the DC-link capacitor requirements are assessed and compared quantitatively among different phase number VSIs. The normalized DC-link capacitor RMS current and one newly proposed concept – normalized DC-link capacitor charge variation are applied to generalize the analysis quantitatively. The research results show that under the equivalent power output, the implementation of higher phase number VSIs can decrease the DC-link capacitor requirements. Moreover, for the VSIs of higher phase numbers, their increased control flexibilities make it possible to further decrease the DC-link requirements via the implementation of the group based interleaved carrier waveform. Additionally, different

switching strategies, switching frequencies and carrier waveforms can also influence the DC-link capacitor requirements. Furthermore, the new conceptual *G*x paralleled *n*-phase inner-phase pseudo-multiphase VSI (IPPM-VSI) is proposed and the characteristics of 2x paralleled 9-phase and 4x paralleled 9-phase IPPM-VSIs are studied and compared with the other 9-phase systems. The analytical study is validated via the equivalent power output 3- and 9-phase VSIs that the 3x 3-phase VSI with SVM group based interleaved triangular carrier requires 1/3 DC-link capacitor RMS current rating and approximate 1/2 DC-link capacitance compared with its 3-phase counterpart. In the EV traction machine drive VSIs, the capacitor volume is proportional to the RMS current rating. Therefore, the 3x 3-phase VSI has a DC-link capacitor 1/3 volume of its 3-phase counterpart. Finally, based on the analytical study and experimental validation a generalized DC-link capacitor design procedure is proposed for arbitrary phase number two level VSIs.

The current and power imbalances among parallel-connected power devices and the consequences are investigated, and the solutions are compared to get the best choice, the implementation of multiphase topology, the multiphase VSI. The benchmark system (the 3-phase 2012 Nissan Leaf traction system VSI) thermal model is built and validated via the comparison with the experiment test results from the existing publications. The 9-phase conventional design VSI is proposed and compared with the benchmark system. Increasing phase number enables the higher controllability to the current through each IGBT dies and hence alleviate or even eliminate the power loss difference, resulting in the better thermal performance. The multiphase integrated design VSI evolutionary design procedure is proposed, based on which the 9-phase integrated design VSI is proposed and it have better thermal performance compared with the 9-phase conventional VSI. To generalize the multiphase VSI thermal investigation, the 18-phase, 27-phase, and 36-phase integrated design VSIs are also proposed, and they have better performances than the 9-phase integrated VSIs. Inheriting and combining the conclusions in Chapter 4 and 5 that the increased phase number VSI decreases the DC-link capacitor requirements and hence its

volume, the implementation of multiphase VSI can achieve the volume reduction and better thermal performance.

Therefore, contributions of this thesis can be summarized as:

- The most appropriate choice of multiphase VSI switching strategies is studied and defined
- Quantitative analysis on the DC-link capacitor requirements reduction in multiphase VSIs is presented and illustrated via a comparative design study
- Multiphase integrated design VSIs and heatsink volume reduction is studied and quantified by a representative design study
- An experimental setup is designed to provide some validation of the research studies.

7.2 Future Research Work

1) In Chapter 3, the new concept – unbalanced group based SVM is proposed and the future research could focus on this, i.e. the SVM for the 8-phase VSI composed of 3-phase and 5-phase ones. Their feasibility, performances and other characteristics could be investigated.
2) In Chapter 4, the new conceptual Gx paralleled n-phase IPPM-VSI is proposed and the DC-link capacitor requirements are studied for 2x paralleled 9-phase IPPM-VSI and 4x paralleled 9-phase IMMP-VSI. Further research could study the IPPM-VSIs and their DC-link capacitor requirement.
3) In Chapter 5, the 3x 3-phase machine drive system has been tested under one phase open condition, 2 sets of 3-phase operating condition and 1 set of 3-phase operating condition, which has not been investigated before. Some further research could continue the faulty operation investigation and the control strategies design.
4) In Chapter 6, the thermal performances, and VSI components volumes are studied under different newly proposed multiphase VSIs and the benchmark. Future research could focus on the multiphase VSI design with wide-bandgap semiconductor power devices.

7.3 Publications

The following publications have resulted from this Ph.D. study:

Published journal paper:

Z. Nie and N. Schofield, "Analysis and Comparison of Power Electronic Converters for conventional and Toroidal Switched Reluctance Machines," Energy and Power Engineering, 9, 241-259, 2017. https://doi.org/10.4236/epe.2017.94017.

Prepared Journal Papers:

[1] **Z. Nie** and N. Schofield, "Multiphase Voltage Source Inverter DC-link Capacitors,".

[2] **Z. Nie** and N. Schofield, "Thermal Design of Multiphase Voltage Source Inverters,".

International refereed conference papers:

[1] **Z. Nie**, M. Preindl and N. Schofield, "SVM strategies for multiphase voltage source inverters," 8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016), Glasgow, 2016, pp. 1-6.

[2] **Z. Nie** and N. Schofield, "Condition monitoring of a permanent magnet synchronous generator for a wind turbine application," 8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016), Glasgow, 2016, pp. 1-6.

[3] **Z. Nie** and N. Schofield, "Analysis and comparison of power electronic converters for Conventional and Toroidal Switched Reluctance Machines," 8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016), Glasgow, 2016, pp. 1-6.

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Appendices

A1 Analysis and Comparison of VSIs for CSRM and TSRM

A1.1 Introduction

During the early part of this thesis, the power electronic converter (herein the VSI) requirements for a non-conventional switched reluctance machines (SRMs) was investigated. The toroidally wound machine studied has an iron circuit similar to that of a conventional 6-4 SRM (CSRM), i.e. 6 wound stator teeth and 4 rotor poles. The toroidally wound SRM, or TSRM, also has 6 coils but these are wound on the stator back-iron portions between the stator teeth. To appropriately control the current of the machine stator windings a 12-switch VSI is required. Since the new TSRM is a topology rival to the CSRM, an assessment of both the CSRM and TSRM, VSIs was made. Hence, different VSI topologies are introduced for both CSRM and TSRM drive systems. Their commutation, switch and diode currents, power losses, and efficiencies under over modulation operation are analyzed and compared for the VSI characteristics study, performance evaluation and topology selection for CSRM and TSRM drive systems. The switch and diode silicon volumes required for both CSRM and TSRM VSIs are also compared according to their corresponding currents at the equivalent machine torque versus speed operating points.

A1.2 Overviews of the CSRM and TSRM VSIs

Although different VSIs for CSRMs have been proposed [200], the most widely used one is the asymmetric VSI as shown in Figure A 1.1 (a) in which unidirectional phase current is switched through the phase winding. Different power electronic VSI topologies are introduced for both CSRM and TSRM drive systems [75]–[77], [201] as shown in Figure A 1.1 and Figure A 1.2. Their commutation, switch and diode currents, power losses, and efficiencies are investigated, compared and evaluated, based on which the total switch and diode silicon volumes for each CSRM and TSRM VSIs are investigated at the equivalent machine torque versus speed operating points. The better VSI choice is also proposed for either CSRM or TSRM VSIs. This can help to make references when determining the ratings of power electronic switches, diodes, thermal design and VSI topology selection.

Two different VSIs are introduced for either the CSRM or TSRM. The CSRM VSI in Figure A 1.1 (a) is a typical asymmetric converter, i.e. 6 switch mode (6-switch), and the one in Figure A 1.2 (a) is a VSI composed of 2x 3-phase full bridge VSIs, 12 switch mode (12-switch). Two different VSIs for TSRM are also illustrated in Figure A 1.1 (b), 6-switch VSI and in Figure A 1.2 (b), 12-switch VSI. The experiment facility is shown in Figure A 1.2 (e).

A1.3 Operation Mechanism Investigation

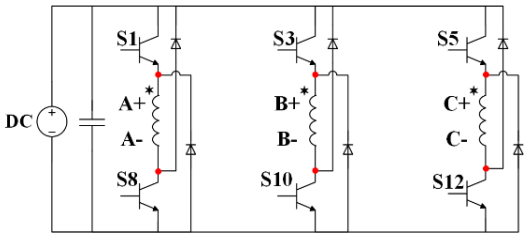
The switching sequences for CSRM 6-switch and CSRM 12-switch VSIs under over modulation are given in Figure A 1.1 (c) and Figure A 1.2 (c), and Figure A 1.1 (d) and Figure A 1.2 (d) show TSRM 6SW and TSRM 12SW VSIs switching sequences. Taking the CSRM 6SW VSI switching sequence for example, in this 4-pole SRM there are 4 electrical periods in one mechanical revolution i.e. 1 electrical revolution corresponding 1/4 mechanical revolution, 1/4 REV in Figure A 1.1 (c). "Event" means the commutation state and the "Coil sequence" indicates the on-state switches. "Coil current" shows the polarity of the coil current in the respective commutation states. While in CSRM 12-switch VSI 1 electrical revolution corresponds 1/2 mechanical revolution and unlike CSRM 6-switch VSI the coil current is bipolar. Having the same mechanical and electrical revolution relation with CSRM, both the TSRM 6-switch VSI and TSRM 12-switch VSI have bipolar current in their coils, while the TSRM 6-switch VSI has unbalanced current in coils, different to the other systems.

The coil A current waveforms for two different CSRM VSIs (6-switch and 12-switch) are shown in Figure A 1.3 (a) and Figure A 1.3 (b), where the 6-switch VSI has unipolar current, but in the 12-switch VSI the coil current polarity reverses in every period. During the coil current increasing segment of each pulse, the current is driven by the DC-link through switches, and during the coil current decreasing segment, the coils are discharged releasing the storage magnetic energy via the diodes. Theoretically, both the VSIs have the same coil current in spite of their polarity, which means the same overall power dissipation under the same operating conditions. While in the 12-switch VSI the current goes through 12 switches and diodes, and in 6-switch VSI the current goes through 6 switches and diodes – same overall power losses on different numbers of switches and diodes. This indicates more even and uniform power dissipation on the heat sink of the 12-switch VSI than the 6-switch VSI. Another characteristics of the CSRM VSIs is that their coils are independently connected to the DC bus, which means from the converter side, there is no mutual effects between different phases and the current waveform of each coil can be studied and analysed separately. That is also called the decoupled characteristics in CSRM VSIs while in TSRM

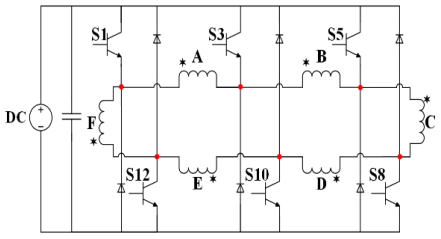
VSIs the mutual effects among different phases counts. Figure A 1.3 (c) and Figure A 1.3 (d) show the operation waveforms for TSRM 6-switch and TSRM 12-switch VSIs respectively. The TSRM 6-switch VSI current waveforms for different coils and phases are by nature not all the same resulting in the switches and diodes currents imbalance, which means the ratings and power losses among different switches and diodes are not all balanced. Moreover, the current imbalance hence the power loss deviation result in different switch and diode thermal-mechanical stresses and fatigue degrees that some of them reach their end of life while the others do not, not fully use of all devices lifetime. Moreover, the mutual effects or coupling among neighbouring coils, and the diode voltage clamping effects introduce transient voltage states during the switch commutations, which does not exist in CSRM VSIs. However, the switches transient voltages are lower than the DC-link voltage implying the same voltage rating of switches and diodes compared with CSRM VSIs. In the TSRM 12-switch VSI both the coil currents and phase currents are balanced, which means the same RMS currents. Similar with the 6-switch one, the coupling among phases and hence the switch transient voltage states exist.

The semiconductor device ratings are constrained and determined by their electrical, material, mechanical, and thermal properties, design, and manufacture processes etc., among which the thermal properties are comparatively dominant on the rating determinations. The devices thermal properties are determined by power losses and heat transfer characteristics. Power losses in a semiconductor device include conduction losses, switching losses, diode recovery and gate losses discussed in Chapter 2. Heat transfer characteristics are dependent on the material and the switch geometry design investigated in Chapter 6. According to the EV traction machine drive system application, IGBTs and MOSFETs are widely used nowadays, and hence the CSRM and TSRM VSIs composed of IGBT modules are investigated, analysed and implemented here. During the switch-on state, currents go through switches junctions and generate joule heat so that the temperature growth occurs at the junction (accounting for the majority), the internal leads and contacts, and the external connectors. During the off-state, at least one junction is reverse-biased to hold the voltage which has an upper limitation equal to the breakdown voltage of the device

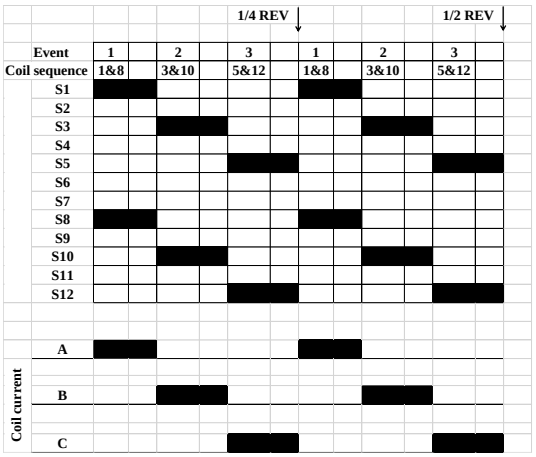
junction [202]. Usually, maximum rated collector-emitter voltages are constrained under different temperatures [81]. Two current restrictions are the maximum continuous collector current and a maximum peak current pulse whose magnitude, width and some other conditions are pre-defined by manufactures [81]. Given that the peak silicon current rating is usually transitory, and this peak current is not exceeded, the silicon volume used in power switch/diode die is dependent on the power loss hence the RMS and average currents conducted, material properties, and the power switches geometry (dies and packaging). Herein, the IGBT and diode currents are investigated on different VSIs.



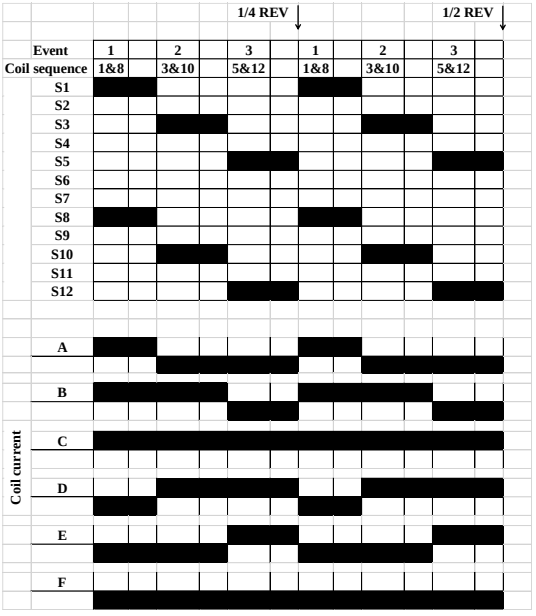
(a) CSRM VSI topology.



(b) TSRM VSI topology.

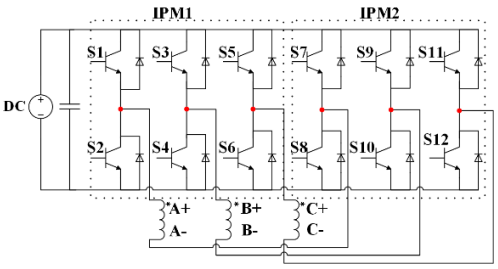


(c) CSRM switching sequences.

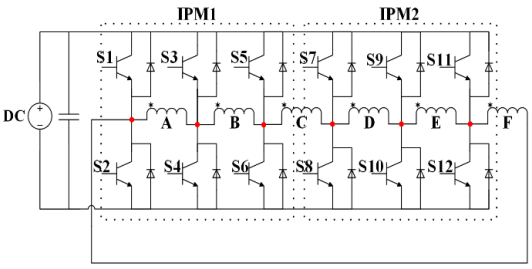


(d) TSRM switching sequences.

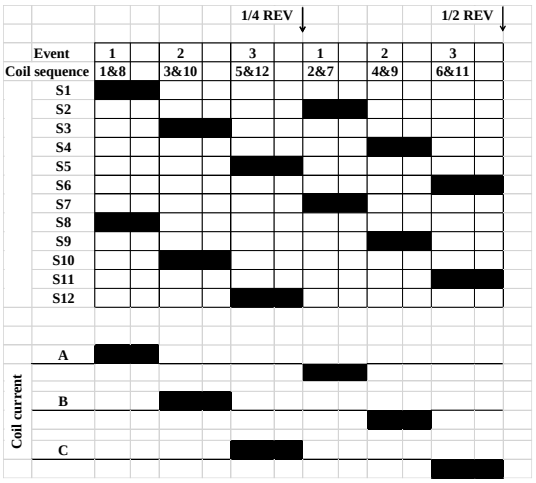
Figure A 1.1 CSRM and TSRM 6-switch VSI topologies, switching sequences and corresponding coil current polarity.



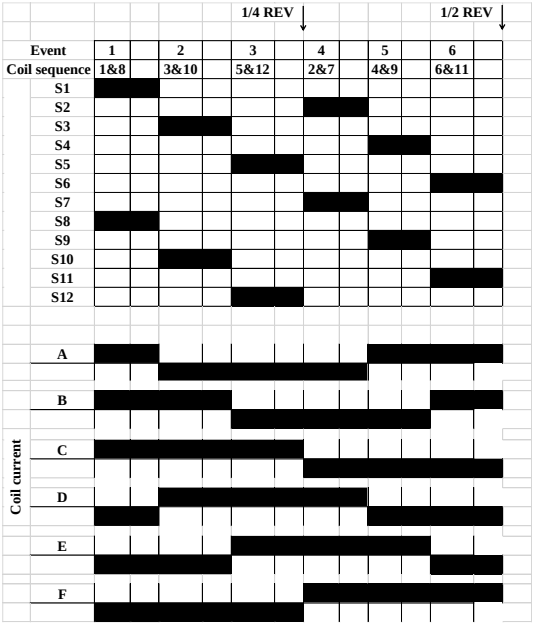
(a) CSRM VSI topology.



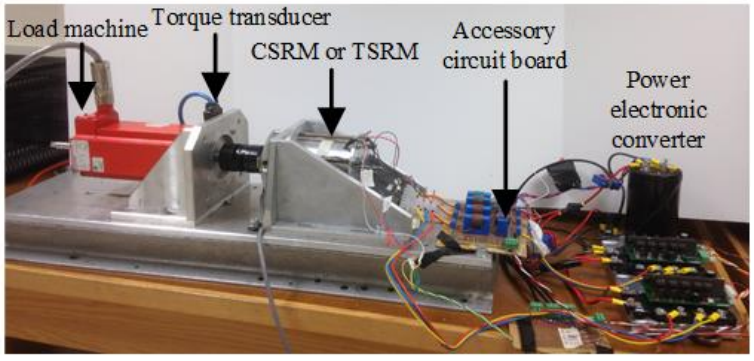
(b) TSRM VSI topology.



(c) CSRM switching sequences.

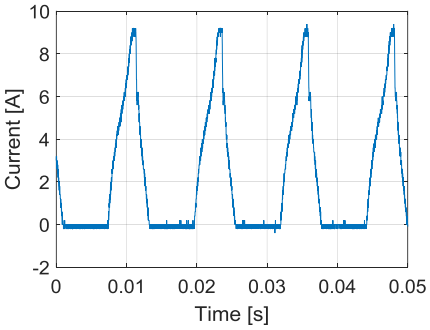


(d) TSRM switching sequences.

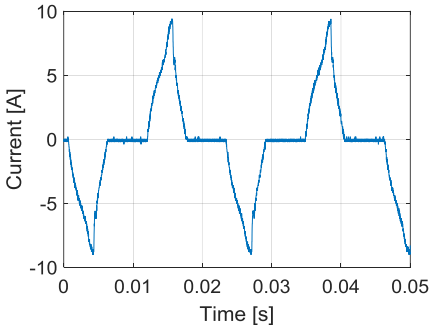


(e) Test facility.

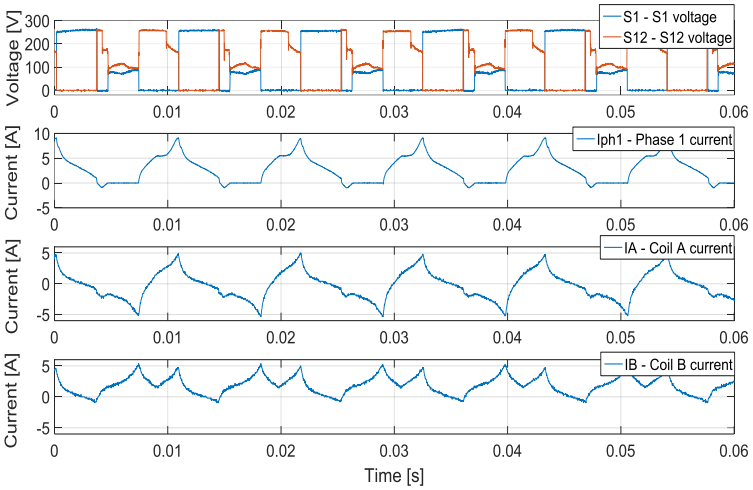
Figure A 1.2 CSRM and TSRM 12-switch VSI topologies, switching sequences, corresponding coil current polarity and test facility.



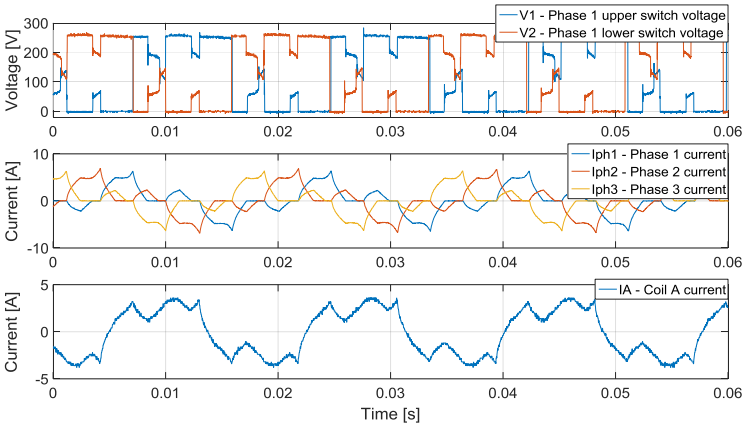
(a) CSRM 6-switch coil A current.



(b) CSRM 12-switch coil A current.



(c) TSRM 6-switch operation waveforms.



(d) TSRM 12-switch operation waveforms.

Figure A 1.3 CSRM and TSRM VSIs operating waveforms.

A1.4 Test Results Analysis and Evaluations

The CSRM and TSRM VSIs are implemented and evaluated. The experiment facility contains an Arduino DUE R3 as the controller, 2 PM50RLA060 integrated power modules (3-phase full bridge IGBT module) from Powerex and their corresponding driver boards, Powerex BP7B, load dynamometer machine, CSRM and TSRM machines, power supplies, torque transducer and accessary circuit boards for logic signal conversion and isolation. In terms of measurements, a Tektronix oscilloscope MDO3024, Metrix differential probe MX 9003, and LEM LA 55-P current transducers are used to capture voltage, current and torque waveforms. The experiment facility is shown in Figure A 1.2 (e).

A1.4.1 The Evaluation and Comparison between CSRM 6-switch and 12-switch VSIs

IGBT switch and diode currents, power losses and VSI efficiencies are evaluated and compared between CSRM 12-switch and CSRM 6-switch VSIs for different load operation points. For the over modulation operation, switching loss and reverse recovery loss can be neglected and only conduction loss is taken into consideration. The power losses of switches and diodes are dependent on their corresponding RMS currents and average currents, as discussed in Chapter 2. A water based thermally managed cold plate is used in the experiment facility to keep the IGBT module case temperature at 20ºC. As the current rating of the IGBT modules used here is far more than operating currents for all of the CSRM and TSRM VSIs. Thus, it is assumed that the IGBT and diode parameters applied here are at 25ºC junction temperature, and the analysed power losses relation among different VSIs is representative under the other junction temperatures or IGBT specifications.

Figure A 1.4 (a) and Figure A 1.4 (b) show the torque versus speed characteristics, and the switch and diode RMS currents versus speed for different operating points of the CSRM 6-switch and CSRM 12-switch VSIs at DC-link voltages of 150 and 300V. To normalize the experimental results in Figure A 1.4 (a) and Figure A 1.4 (b), the torque to switch and torque to diode RMS current ratios are calculated and compared quantitatively. Figure A

1.4 (c) and Figure A 1.4 (d) show these ratios versus the machine rotational speed at DC-link voltages of 150 and 300V.

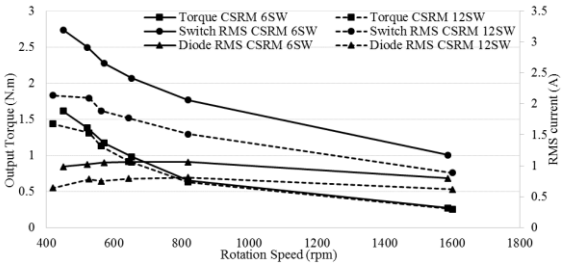
Figure A 1.4 (c) and Figure A 1.4 (d) denote higher torque to switch and torque to diode RMS current ratios for the CSRM 12-switch VSI than the CSRM 6-switch one. This indicates lower RMS currents per switch or diode under the same torque in CSRM 12-switch VSI than those in CSRM 6-switch one. Also in either CSRM 12-switch or CSRM 6-switch VSI under the same operation point the torque versus diode RMS current ratios are more than the torque versus switch RMS current ratios, which is understandable because the excitation currents via switches are more than the freewheeling currents through diodes as shown in Figure A 1.3 (a) and (b). In semiconductor devices the switches are normally designed to have the same current and voltage ratings with their respective freewheeling diodes so only the torque versus switch RMS current ratios are investigated and compared for simplification. On the contrary, if the same current ratings in switch and its freewheeling diode are not constrained, for this specific and some other certain applications the freewheeling diodes can be designed with lower current ratings than the corresponding switches to save the silicon materials and hence the costs.

Under the DC-link voltage of 150V the difference between the torque versus switch RMS current ratios of both CSRM 12-switchand CSRM 6-switch VSIs is not sound, 0.65 Nm/Amp and 0.5 Nm/Amp at the highest torque points on Figure A 1.3 (c). While this difference is enlarged when the DC-link voltage becomes 300V that the ratios are 0.83 Nm/Amp and 0.5 Nm/Amp at the highest torque points on Figure A 1.3 (d). For the torque to diode RMS current ratios of both CSRM 12-switch and CSRM 6-switch under 300V DC-link voltage, the values are 1.67 Nm/Amp and 1.17 Nm/Amp respectively. It is assumed that the switch or diode silicon volume is proportional to the RMS current (for the same break down voltage) as discussed in Chapter 2. under the same machine operating point and between CSRM 6-switch and CSRM 12-swtich, the former requires 1.7 times silicon volume for each switch and 1.4 times silicon volume for each diode to the latter. However, the total switch and diode numbers of CSRM 6-switch is half the CSRM 12-

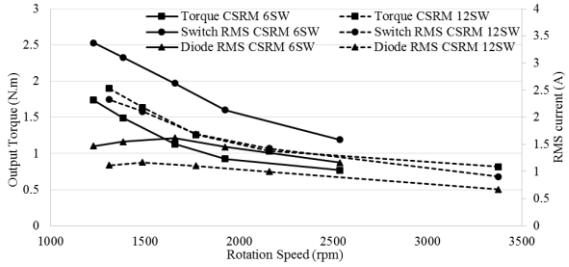
switch so that the total switch and diode silicon volume for CSRM 6-switch is 0.8 times and 0.7 times of those for CSRM 12-switch.

From the current waveforms in Figure A 1.3 (a) and Figure A 1.3 (b), the switch conduction segments account for about 1/3 of the total period in CSRM 6-switch VSI and about 1/6 of the total period in CSRM 12-switch VSI. The switch RMS currents are the switch RMS currents during the total electrical period, while under the steady state operation the junction temperature hits the peak at the every ends of the switch conduction segments. Although the switch RMS current over the whole electrical period provides a reference for the VSI switch RMS current rating, the switch RMS current within every conduction segments should also be considered. However, this situation only occurs under low speed high torque that the switching period is compared to the silicon junction thermal time constant. Under this condition, the switches and diodes in CSRM 6-switch and CSRM 12-switch VSIs require the same current ratings if the switch and diode RMS currents over the conduction segments are considered although the switches and diodes number in CSRM 12-switch VSI doubles that of CSRM 6-switch VSI. However, the RMS current of the whole electrical period is considered here assuming that the machine rotational speed is not low enough to compare with the silicon junction thermal time constant.

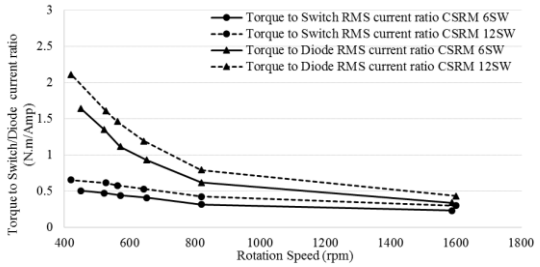
Under similar machine torque versus speed operating points, the CSRM 12-switch VSI has lower switch and diode average current than CSRM 6-switch VSI, approximate the half, which is easy to be understood because the CSRM 12-switch VSI switch current electrical period doubles that of CSRM 6-swtich VSI while their conduction segment currents are the same. Table A 1.1 shows the total power losses and their respective efficiencies under different operation points, showing no significant difference occurs between CSRM 6-switch and CSRM 12-switch VSIs.



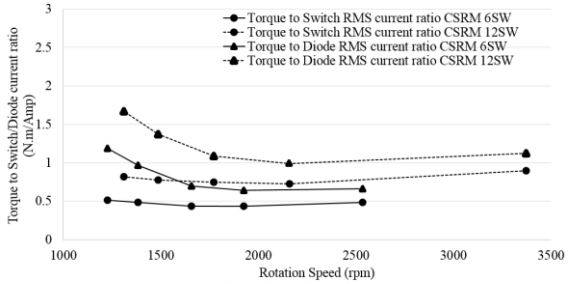
(a) Torque, diode and switch RMS current versus rotational speed at a DC bus voltage = 150V.



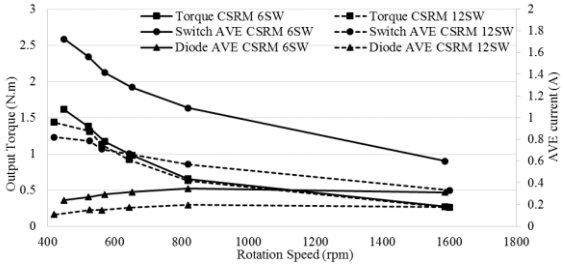
(b) Torque, diode and switch RMS current versus rotational speed at a DC bus voltage = 300V.



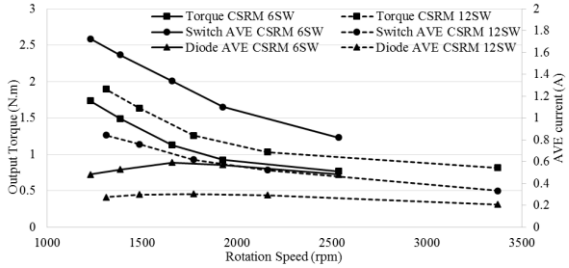
(c) Torque to switch and torque to diode RMS current ratio versus rotational speed at a DC bus voltage = 150V.



(d) Torque to switch and torque to diode RMS current ratio versus rotational speed at a DC bus voltage = 300V.



(e) Torque, diode and switch average (AVE) current versus rotational speed at 150 V DC bus.



(f) Torque, diode and switch average (AVE) current versus rotational speed at 300 V DC bus.

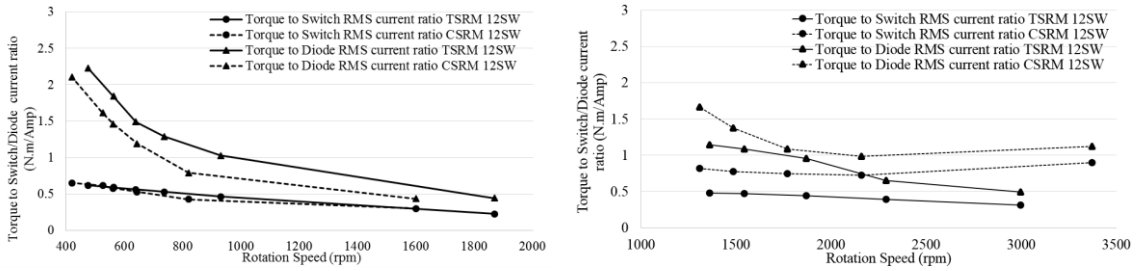
Figure A 1.4 Test results for the CSRM (Note: 6SW for 6-swtich and 12SW for 12-switch).

A1.4.2 The Evaluation and Comparison between 12-switch TSRM and CSRM VSIs

The symmetric characteristics is an advantage of TSRM 12-switch VSI over TSRM 6-switch VSI and it results in a symmetric design of the VSIs (in terms of switch and diode specifications, layout etc.). Consequently, the TSRM 12-switch VSI is selected as the candidate from the two TSRM VSIs, and its switch and diode current, power losses and converter efficiencies are compared with CSRM 12-switch VSI under different operation points. Similarly, only the conduction loss is taken into consideration.

Figure A 1.5 shows the normalized switch and diode RMS current experimental results, i.e. the torque to switch and the torque to diode RMS current ratios for CSRM 12-switch and TSRM 12-switch VSIs. When the DC-link voltage is 150V there is no significant difference in terms of the torque to switch RMS current, while more diode RMS current is required in CSRM 12-swith VSI. However, when the DC-link voltage is 300V, the CSRM 12-switch VSI system requires less RMS switch and diode currents than TSRM 12-switch VSI for equivalent torque output. A higher DC-link voltage is usually selected to have a better power output capability under the same current limitation. When 300V DC is selected, as shown in Figure A 1.5 (b), the highest torque points (around 1300rpm) 1.46 times switch RMS current and 1.8 times diode RMS current are required for the TSRM 12-switch VSI than those in CSRM 12-switch VSI which indicates that more silicon volume is required. Comparison between CSRM 12-switch and TSRM 12-switch VSIs identifies that to drive the same torque output, TSRM 12-switch VSI requires respectively 2.13 times and 3.24 times switch and diode silicon volume compared with CSRM 12-switch VSI.

Table A 1.1 shows the total power losses and their respective efficiencies under different operating conditions and DC-link voltages for TSRM 12-switch VSI. The comparison between CSRM 12-switch and TSRM 12-switch VSIs shows that there is no sound difference in terms of power losses and efficiencies at similar operating conditions.



(a) DC bus voltage = 150V. (b) DC bus voltage = 300V.

Figure A 1.5 Test results for torque, diode and switch RMS current ratio versus rotational speed for both the CSRM and TSRM. (Note: 12SW for 12-switch).

Table A 1.1 Power losses and efficiencies at different operating points for the 6-and 12-switch CSRM and 12-switch TSRM VSIs.

	Rotational speed (rpm)	DC-link input power (W)	Power loss (W)	Efficiency (%)
CSRM 6-switch 150V	1587.3	195.9	5.8	97
	819.7	363	9.3	97
	652.2	399	10.4	97
	571.4	351	11.1	96
	521.7	459	12	97
	449.8	444	12.9	97
CSRM 6-switch 300V	2533.8	267	8.4	96
	1924.3	246.3	10.9	95
	1657.9	408	12.7	96
	1382.8	429	13.9	96
	1227.2	543	14.6	97
CSRM 12-switch 150V	1600	162.3	6.5	96
	819.7	247.5	9.9	96
	643.8	354	10.9	96
	561.8	321	11.2	96
	526.3	276.9	12.3	95
	420.2	516	12.1	97
CSRM 12-switch 300V	3372.7	192.3	6.9	96
	2159.1	223.8	10.6	95
	1770.4	272.4	12	95
	1485.5	318	14	95
	1310.3	345	14.7	95
TSRM 12-switch 150V	1869.2	137.1	6.7	95
	930.2	303	10.9	96
	736.2	408	12.6	96
	639	483	13.9	97
	562.9	537	14.1	97
	475.4	636	15.6	97
TSRM 12-switch 300V	2997	163.5	9.1	94
	2288.3	224.4	12.4	94
	1869.2	363	14.5	96
	1544.4	507	16.9	96
	1362.1	540	19.4	96

A1.5 Summary

The operation and commutation mechanisms are investigated for the CSRM and TSRM 6- and 12-switch VSIs, followed by the comparison of their IGBT switch and diode currents. The TSRM 6-switch VSI is not considered as a proper solution due to the current imbalances in different IGBT switches and diodes. The IGBT switch and diode silicon material volumes requirement is compared among CSRM 6- and 12-switch and TSRM 12-switch VSIs. While, due to the fact that the switch number in CSRM 12-swtich VSI doubles that in CSRM 6-switch VSI, the power loss in CSRM 12-switch VSI is more uniformly distributed on the heat sink than that in the CSRM 6-switch one. As a consequence, this potentially leads to a better thermal performance and potentially increases the drive capability.

A2 DC-link Capacitor Investigation Test Validation Results

Table A 2.1 Analytical and experimental normalized DC cap current comparison under 3-phase SPWM 10 kHz non-interleaved triangle carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.18	0.36	12.37	6.24	0.50	0.58	-13.03%
1000	30.00	0.31	0.50	11.16	6.17	0.55	0.62	-10.83%
1500	40.00	0.45	0.66	12.86	7.40	0.58	0.61	-5.67%
2000	60.00	0.46	0.80	11.77	6.66	0.57	0.59	-4.09%
2500	80.00	0.52	0.90	11.33	6.00	0.53	0.56	-5.43%

Table A 2.2 Analytical and experimental normalized DC cap current comparison under 3-phase SPWM 10 kHz symmetrical interleaved triangle carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.18	0.36	12.26	11.24	0.92	0.93	-1.42%
1000	30.00	0.31	0.50	11.18	9.63	0.86	0.86	0.16%
1500	40.00	0.45	0.66	12.73	9.70	0.76	0.78	-2.31%
2000	60.00	0.46	0.80	11.69	7.75	0.66	0.67	-1.05%
2500	80.00	0.52	0.90	11.16	6.25	0.56	0.61	-8.19%

Table A 2.3 Analytical and experimental normalized DC cap current comparison under 3-phase SPWM 10 kHz non-interleaved saw tooth carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.18	0.36	12.51	7.30	0.58	0.59	-1.10%
1000	30.00	0.31	0.50	11.31	6.99	0.62	0.62	-0.32%
1500	40.00	0.45	0.66	12.93	8.28	0.64	0.61	4.98%
2000	60.00	0.46	0.80	11.81	7.42	0.64	0.60	6.67%
2500	80.00	0.52	0.90	11.52	6.72	0.58	0.56	4.17%

Table A 2.4 Analytical and experimental normalized DC cap current comparison under 3-phase SPWM 10 kHz symmetrical interleaved saw tooth carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.18	0.36	12.73	11.50	0.90	0.92	-1.81%
1000	30.00	0.31	0.50	11.25	9.28	0.82	0.84	-1.80%
1500	40.00	0.45	0.66	12.93	9.34	0.72	0.75	-3.69%
2000	60.00	0.46	0.80	11.54	7.20	0.62	0.64	-2.51%
2500	80.00	0.52	0.90	11.25	6.10	0.54	0.60	-9.63%

Table A 2.5 Analytical and experimental normalized DC cap current comparison under 3-phase SVM 10 kHz non-interleaved triangle carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.18	0.36	12.49	6.43	0.51	0.58	-11.24%
1000	30.00	0.31	0.50	11.36	6.32	0.56	0.62	-10.27%
1500	40.00	0.45	0.66	12.86	7.51	0.58	0.61	-4.27%
2000	60.00	0.46	0.80	11.77	6.73	0.57	0.59	-3.09%
2500	80.00	0.52	0.90	11.28	6.03	0.53	0.56	-4.54%

Table A 2.6 Analytical and experimental normalized DC cap current comparison under 3-phase SVM 10 kHz symmetrical interleaved triangle carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.18	0.36	12.24	11.35	0.93	0.93	-0.29%
1000	30.00	0.31	0.50	11.18	9.74	0.87	0.86	1.30%
1500	40.00	0.45	0.66	12.84	10.00	0.78	0.78	-0.15%
2000	60.00	0.46	0.80	11.72	7.96	0.68	0.66	2.91%
2500	80.00	0.52	0.90	11.20	6.55	0.58	0.61	-4.13%

Table A 2.7 Analytical and experimental normalized DC cap current comparison under 3-phase SVM 10 kHz non-interleaved saw tooth carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.18	0.36	12.27	7.18	0.59	0.58	0.89%
1000	30.00	0.31	0.50	11.13	7.00	0.63	0.62	1.44%
1500	40.00	0.45	0.66	12.72	8.26	0.65	0.61	6.45%
2000	60.00	0.46	0.80	11.69	7.44	0.64	0.59	7.87%
2500	80.00	0.52	0.90	11.05	6.54	0.59	0.56	5.69%

Table A 2.8 Analytical and experimental normalized DC cap current comparison under 3-phase SVM 10 kHz symmetrical interleaved saw tooth carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.18	0.36	12.17	11.25	0.92	0.93	-0.60%
1000	30.00	0.31	0.50	11.20	9.47	0.85	0.86	-1.68%
1500	40.00	0.45	0.66	12.66	9.42	0.74	0.77	-3.37%
2000	60.00	0.46	0.80	11.57	7.44	0.64	0.65	-1.07%
2500	80.00	0.52	0.90	11.22	6.20	0.55	0.60	-7.90%

Table A 2.9 Analytical and experimental normalized DC cap current comparison under 3x 3-phase SPWM 10 kHz non-interleaved triangle carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.14	0.28	3.94	5.04	1.28	1.50	-14.72%
1000	30.00	0.26	0.45	3.68	5.27	1.43	1.65	-13.21%
1500	40.00	0.32	0.61	4.08	5.94	1.46	1.64	-11.23%
2000	60.00	0.40	0.76	3.75	5.18	1.38	1.48	-6.67%
2500	80.00	0.35	0.87	3.58	4.28	1.20	1.32	-9.43%

Table A 2.10 Analytical and experimental normalized DC cap current comparison under 3x 3-phase SPWM 10 kHz group based interleaved triangle carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.14	0.28	3.90	2.22	0.57	0.60	-5.13%
1000	30.00	0.26	0.45	3.60	1.57	0.44	0.44	-0.88%
1500	40.00	0.32	0.61	4.05	2.39	0.59	0.61	-3.26%
2000	60.00	0.40	0.76	3.72	2.22	0.60	0.68	-12.24%
2500	80.00	0.35	0.87	3.54	2.64	0.75	0.80	-6.78%

Table A 2.11 Analytical and experimental normalized DC cap current comparison under 3x 3-phase SPWM 10 kHz non-interleaved saw tooth carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.14	0.28	3.94	6.05	1.54	1.50	2.37%
1000	30.00	0.26	0.45	3.58	5.96	1.66	1.66	0.29%
1500	40.00	0.32	0.61	4.08	6.91	1.69	1.64	3.27%
2000	60.00	0.40	0.76	3.75	5.99	1.60	1.48	7.93%
2500	80.00	0.35	0.87	3.60	4.96	1.38	1.32	4.38%

Table A 2.12 Analytical and experimental normalized DC cap current comparison under 3x 3-phase SPWM 10 kHz group based interleaved saw tooth carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.14	0.28	3.84	2.59	0.67	0.60	12.41%
1000	30.00	0.26	0.45	3.47	2.05	0.59	0.58	1.86%
1500	40.00	0.32	0.61	3.90	2.78	0.71	0.67	6.39%
2000	60.00	0.40	0.76	3.56	2.66	0.75	0.73	2.35%
2500	80.00	0.35	0.87	3.40	2.92	0.86	0.82	4.73%

Table A 2.13 Analytical and experimental normalized DC cap current comparison under 3x 3-phase SVM 10 kHz non-interleaved triangle carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.14	0.29	3.95	5.50	1.39	1.52	-8.39%
1000	30.00	0.26	0.43	3.64	5.52	1.52	1.68	-9.73%
1500	40.00	0.32	0.61	4.06	6.47	1.59	1.8	-11.47%
2000	60.00	0.40	0.75	3.70	5.76	1.56	1.70	-8.43%
2500	80.00	0.35	0.89	3.57	5.04	1.41	1.56	-9.50%

Table A 2.14 Analytical and experimental normalized DC cap current comparison under 3x 3-phase SVM 10 kHz group based interleaved triangle carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.14	0.29	3.83	2.19	0.57	0.59	-3.08%
1000	30.00	0.26	0.43	3.50	1.07	0.31	0.33	-7.36%
1500	40.00	0.32	0.61	4.00	2.35	0.59	0.61	-3.69%
2000	60.00	0.40	0.75	3.66	1.96	0.54	0.50	7.10%
2500	80.00	0.35	0.89	3.52	1.73	0.49	0.56	-12.24%

Table A 2.15 Analytical and experimental normalized DC cap current comparison under 3x 3-phase SVM 10 kHz non-interleaved saw tooth carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.14	0.29	3.93	6.30	1.60	1.61	-0.43%
1000	30.00	0.26	0.43	3.61	6.30	1.75	1.76	-0.84%
1500	40.00	0.32	0.61	4.09	7.44	1.82	1.8	1.06%
2000	60.00	0.40	0.75	3.78	6.72	1.78	1.70	4.58%
2500	80.00	0.35	0.89	3.57	5.82	1.63	1.56	4.50%

Table A 2.16 Analytical and experimental normalized DC cap current comparison under 3x 3-phase SVM 10 kHz group based interleaved saw tooth carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.14	0.29	3.80	2.52	0.66	0.58	14.34%
1000	30.00	0.26	0.43	3.35	1.29	0.39	0.34	13.26%
1500	40.00	0.32	0.61	3.84	2.43	0.63	0.63	0.45%
2000	60.00	0.40	0.75	3.53	2.19	0.62	0.55	12.80%
2500	80.00	0.35	0.89	3.43	2.28	0.66	0.59	12.66%

Table A 2.17 Analytical and experimental normalized DC cap current comparison under 9-phase SPWM 10 kHz non-interleaved triangle carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.18	0.28	3.90	5.13	1.32	1.50	-12.31%
1000	30.00	0.25	0.48	3.64	5.09	1.40	1.67	-16.27%
1500	40.00	0.28	0.70	4.14	5.77	1.39	1.61	-13.43%
2000	60.00	0.41	0.83	3.79	4.84	1.28	1.37	-6.79%

Table A 2.18 Analytical and experimental normalized DC cap current comparison under 9-phase SPWM 10 kHz group based interleaved triangle carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.18	0.28	3.87	2.24	0.58	0.60	-3.53%
1000	30.00	0.25	0.48	3.68	1.71	0.46	0.49	-5.17%
1500	40.00	0.28	0.70	4.07	2.54	0.62	0.6	4.01%
2000	60.00	0.41	0.83	3.67	2.78	0.76	0.76	-0.33%

Table A 2.19 Analytical and experimental normalized DC cap current comparison under 9-phase SPWM 10 kHz non-interleaved saw tooth carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.18	0.28	3.92	6.09	1.55	1.50	3.57%
1000	30.00	0.25	0.48	3.57	5.88	1.65	1.67	-1.37%
1500	40.00	0.28	0.70	4.16	6.77	1.63	1.61	1.08%
2000	60.00	0.41	0.83	3.84	5.76	1.50	1.37	9.49%

Table A 2.20 Analytical and experimental normalized DC cap current comparison under 9-phase SPWM 10 kHz group based interleaved saw tooth carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.18	0.28	3.86	2.62	0.68	0.60	13.13%
1000	30.00	0.25	0.48	3.49	2.20	0.63	0.61	3.34%
1500	40.00	0.28	0.70	4.02	2.98	0.74	0.65	14.05%
2000	60.00	0.41	0.83	3.66	3.21	0.88	0.80	9.63%

Table A 2.21 Analytical and experimental normalized DC cap current comparison under 9-phase SVM 10 kHz non-interleaved triangle carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.18	0.29	3.90	5.07	1.30	1.51	-13.91%
1000	30.00	0.25	0.49	3.56	4.99	1.40	1.67	-16.07%
1500	40.00	0.28	0.72	4.07	5.62	1.38	1.59	-13.16%
2000	60.00	0.41	0.85	3.78	4.73	1.25	1.34	-6.62%

Table A 2.22 Analytical and experimental normalized DC cap current comparison under 9-phase SVM 10 kHz group based interleaved triangle carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.18	0.29	3.88	2.23	0.57	0.59	-2.59%
1000	30.00	0.25	0.49	3.54	1.63	0.46	0.51	-9.72%
1500	40.00	0.28	0.72	4.07	2.55	0.63	0.63	-0.55%
2000	60.00	0.41	0.85	3.75	2.86	0.76	0.77	-0.95%

Table A 2.23 Analytical and experimental normalized DC cap current comparison under 9-phase SVM 10 kHz non-interleaved saw tooth carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.18	0.29	3.97	6.12	1.54	1.60	-3.65%
1000	30.00	0.25	0.49	3.66	5.98	1.63	1.68	-2.75%
1500	40.00	0.28	0.72	4.15	6.73	1.62	1.59	1.99%
2000	60.00	0.41	0.85	3.86	5.69	1.47	1.34	10.01%

Table A 2.24 Analytical and experimental normalized DC cap current comparison under 9-phase SVM 10 kHz group based interleaved saw tooth carrier waveform.

Rotation speed (rpm)	Dyno resistance (Ω)	Current lagging angle (rad)	Modulation index	Phase RMS current (A)	DC cap RMS current (A)	DC cap RMS current normalization	Analytical DC cap RMS current normalization	Error between experiment and analytical study
500	12.60	0.18	0.29	3.84	2.60	0.68	0.59	14.76%
1000	30.00	0.25	0.49	3.51	2.19	0.62	0.62	0.63%
1500	40.00	0.28	0.72	4.02	2.98	0.74	0.67	10.64%
2000	60.00	0.41	0.85	3.68	3.26	0.89	0.82	8.03%