Polymer-embedded AC-driven Light-emitting Diode (LED) Assembly

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Light-emitting Diode (LED) Assembly

By

WEIWEI(ERIC) ZHAO, B.ENG.

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AUTHOR: Weiwei(Eric) Zhao, B.Eng. (Central South University)

SUPERVISOR: Professor Adrian H. Kitai

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Abstract

The traditional framework of LED assembly can only work with direct current(DC) source, and requires soldering/wire bonding, limiting the flexibility and further improvement of display resolution. In this thesis, an innovative small-size AC-driven LED assembly has been successfully developed, in which LEDs get their power through insulating dielectric layers without wire bonding when using high-frequency AC source. This novel package method of an AC powered flexible dual-LED unit is built up with two reverse-parallel-connected LED chip, namely dual-LEDs. The dual-LEDs preparation process is involved with the surface and interface modification, dielectric composites and combined transparent electrode layer processing. The key parameters of preparing the polymer-embedded LED platelet are obtained and the properties of combined transparent electrodes of Indium Tin Oxide(ITO)/silver nanowires(AgNWs) have been investigated. The luminous properties of the AC-driven assembly are explicitly evaluated based on the Sawyer-Tower method and the luminous intensity and luminous efficiency in variation of input AC voltage are presented. The package shows a good flexibility and is much smaller in size compared with traditional LED package, as well as eliminates the need of wirebonding to be powered on. The method of assembly is very promising in the future low cost printed assembly of large numbers of dual LED platelets in a sheet or strip.

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Chapter 1 Introduction

1.1 Current Flat Panel Display Technology

Light emitting diode(LED) as a semiconductor display device was first invented (Holonyak and Bevacqua, 1962) and soon has lasting and profound influences on current information display industry. Since the 1970s, the performance and properties of LED has been largely improved regarding brightness, lifetime and light efficiency and quickly applied into industrial manufacturing with the development of semiconductor materials synthesis technology. Into the 1990s, the LED experienced great breakthroughs particularly with the invention of nitride blue LED by Nakamura from Nichia Corporation of Japan (Nakamura S., 1994). Ever since then, the average LED usage in each household has grown more than tenfold. LED application areas include LCD backlights, displays, transportation equipment lighting, and general lighting.

LED displays have advantages over the other competitors for their unique advantages, such as: high reliability, long life, high brightness, low power consumption, rich colors LED displays have been widely used in industrial, transportation, commercial advertising, information dissemination, sports competitions and other fields. Due to their high efficiency, high reliability and saturated colors, LED display will be more widely used. LEDs are used as a light source for LCD backlights in products such as mobile phones, cameras, portable media players, notebooks, monitors, and TVs. Display applications include LED electronic scoreboards, outdoor billboards, and signage lighting, such as LED strips and lighting bars. Examples of transportation equipment lighting areas are passenger vehicle and train lighting (e.g., meter backlights, tail and brake lights) and ship and airplane lighting (e.g., flight

error lighting and searchlights). General lighting applications are divided into indoor lighting (e.g., LED lamps, desk lighting, and surface lighting), outdoor lighting (e.g., decorative lighting, street/bridge lighting, and stadium lighting), and special lighting (e.g., elevator lighting and appliance lighting). The use of LEDs in general lighting has increased, beginning with street lighting in public areas and moving onto commercial/ business lighting and consumer applications, as seen in table 1 (Karlicek, et al., 2005; Krames et al., 2016; Nicolics et al., 2010).

Table 1 General application are of LEDs

Application area	Application examples
LCD backlight	Mobile phones Cameras Portable media player Monitors Televisions
Displays	Electronic socreboads Outdoor billboard Signage lighting
Transportation equipment lighting	Vechicl/train lighting Ship/airplane lighting
General lighting	Decoration llighting Indoor lihting Outdoor lighitng

LED display technology/module is operated by a number of light-emitting diodes, which constitute the dot matrix form. Through electronic control, LED displays can be used to display text, graphics, images, animation, video, and other information. With the rapid development of computer technology and semiconductor technology, it has become a

comprehensive multi-function large-scale display device that can play dynamic video information from a computer or play still images from a storage device.

1.2 The package and assembly of LED

A LED package and the associated display systems, like other electronic systems, are involved with a lot of manufacturing processes from epitaxial growth to chip manufacturing to packaging and to final fixture assembly before LED based applications enter the consumer market (Liu S. and Luo X., 2011).

Manufacturing processes of the LED chips and package directly influence the reliability and maintenance in applications of LED devices and determines the opto-electronic performance of the application. The manufacturing process of LEDs is somewhat similar to microelectronics, but there are functional requirements, materials, and interfaces in LEDs that make their failure modes and mechanisms unique.

Along the chain of the LED manufacturing industry, the midstream part of package/assembly plays the essential role in bridging from the upstream processes of semiconductor die making and the downstream aspects of multiple types of applications. The typical manufacturing flow, from chips to application, includes bonding process, die attach process and epoxy curing process and critical package, which are shown in details in figure 1.1 (Chang et al., 2012; Liu et al. 2014).

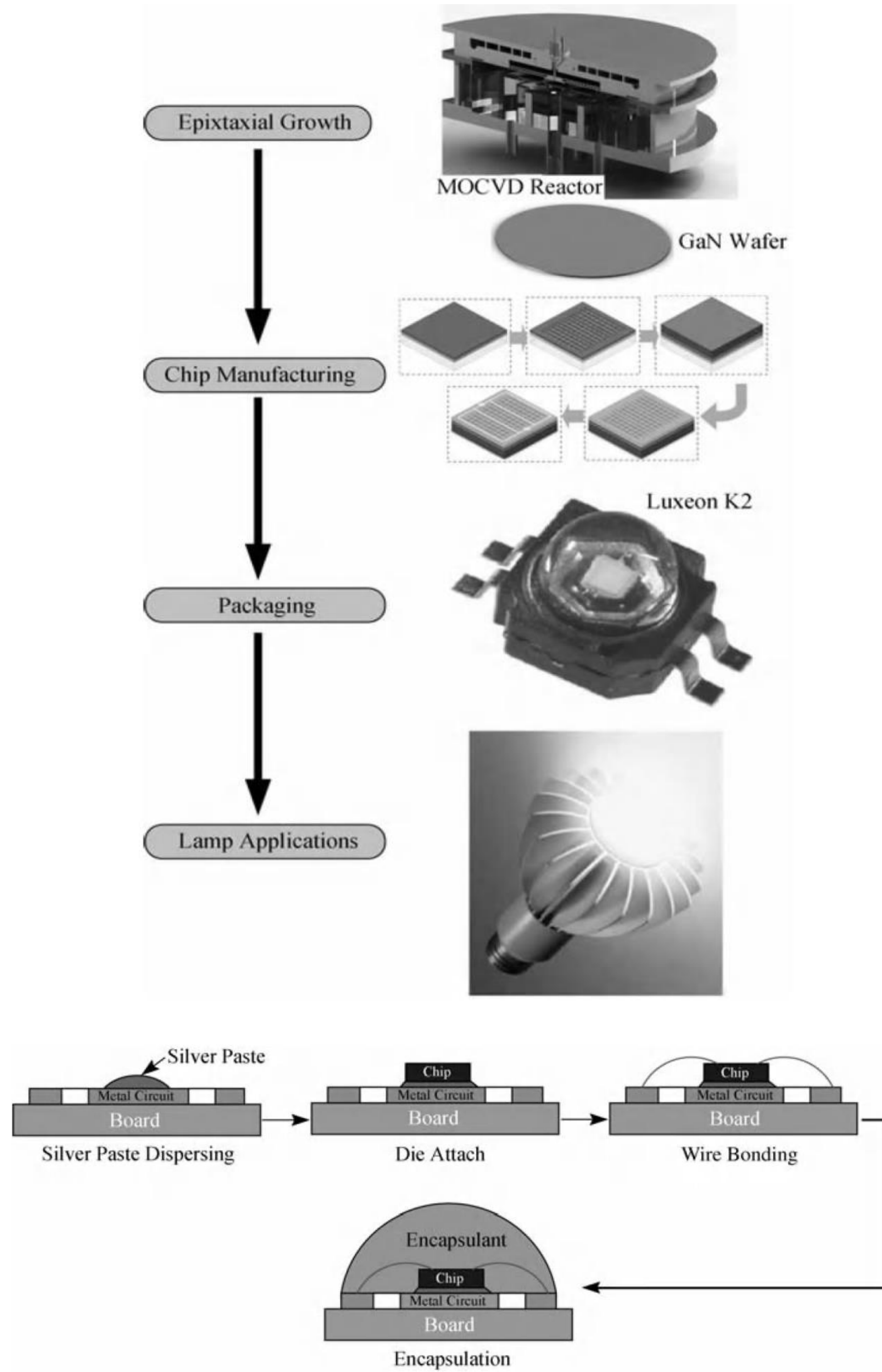

Figure 1.1 Schematic of the sequence in terms of major business classification and a typical packaging process with wirebonding (Liu et al. 2014)

The critical package processes include bonding process, die attach process and epoxy curing process, and each process will directly affect LED reliability. However, even though the current packaging technology is mature, package problems or failure that will cause poor reliability might result from three main aspects: failure in die attachment, cracks at wire-bonding area and Voids/Bubbles formation in the epoxy resin (Lu et al., 2009). The details of the failure and package problems will be discussed in detail in Chapter 2.

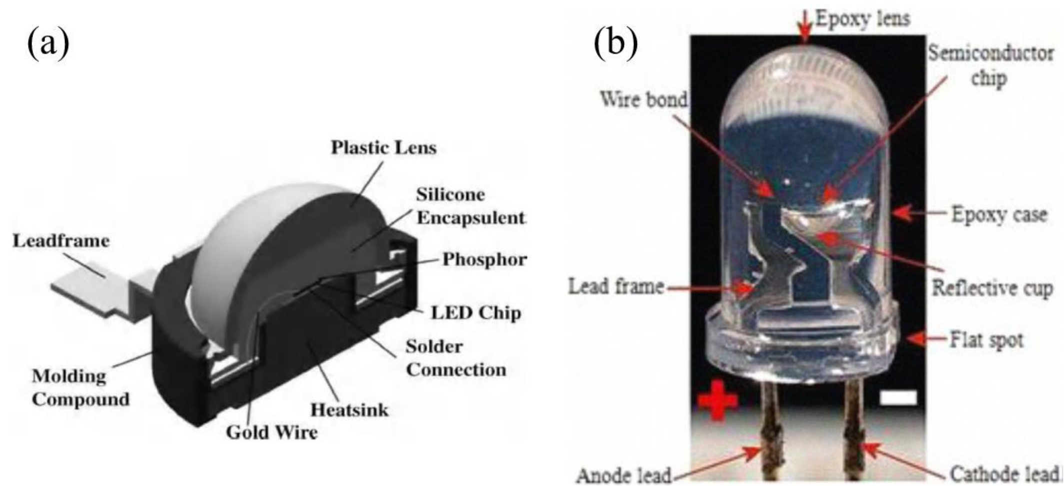

Figure 1.2 One of the most commonly used LED packaging structure: (a) schematic of cross section (Lin et al., 2009); (b) real photo of the cross section of a LED packaged device (Lu et al., 2009)

One main objective of the LED package is to guarantee electrical performance between the die and the outer electric circuit. Packaging of LED die protects it from mechanical stress, thermal stress, moisture and other exterior impacts (Lin et al., 2009). At the same time, the LED must realize its optical characteristics, and corresponding consideration should be given to optics during the packaging process.

Here, the focus of manufacturing is of LEDs at the die and package levels, which comprises the steps of integrating LED chips into an assembly. The most simple and complete LED lamp includes the semiconductor chip, reflective cup, lead frame, epoxy lens, epoxy case and other components (Lu et al., 2009), as shown in figure1.2.

1.3 Alternating-Current(AC)-Driven LED Assembly

The LED is one of the semiconductor P-N junction diodes. LED gives emits light when being applied with forward-bias current, because the electrons and holes as majority carriers that are injected across the junction and undergo radiative recombination in or near junction zone (Kitai A. et al., 2011). Whereas the recombination of electrons and holes could not occur in a reverse direction.

When forward-bias voltage applied, the energy barrier height at the transition region will be decreased, which is beneficial for the majorities of electrons and holes flow into the junction area. When one electron and one hole undergo the radiative recombination near or at the junction, one photon of light will be probably produced, thus emitting light out. On the other hand, when a reverse-bias is applied, the negative bias will result in a higher energy barrier height and eliminate the recombination process of electrons and holes. Besides, once a reversed bias exceeds the breakdown voltage, the p-n junction diode might be damaged if the applied voltage reaches the breakdown value.

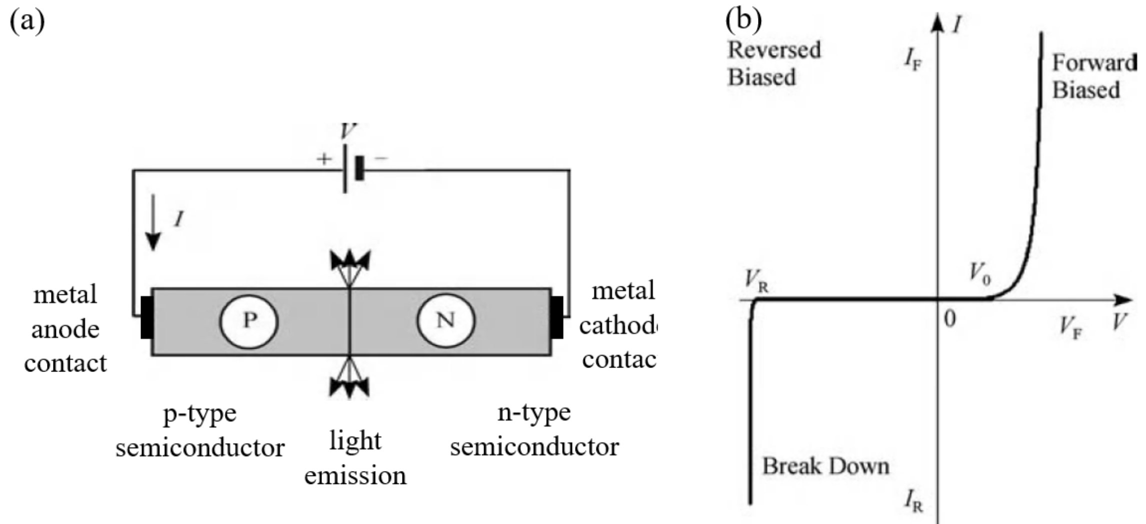

Figure 1.3 (a) a p-n junction lighting emitting diode with external voltage applied; (b) I-V characteristic curve of LED

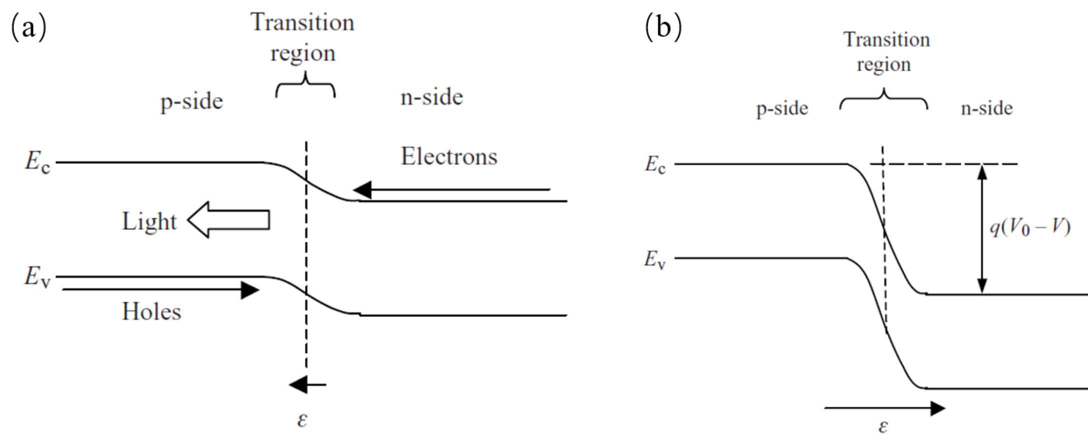

Figure 1.4 Diode band model with application of a forward bias(a) and a revers bias(b). The energy barrier height is narrower in (a) and becomes wider in (b) because of the influence of the positive and negative applied voltage respectively (Kiati A. et al., 2011).

Though LED die may be made of different the semiconductor materials and the structure of LED device varies, however, the LED can only be operated by directly current under forward-bias voltage and cannot be lightened up by a reverse-bias voltage. In general, if

the voltage to drive the LED comes from an AC source, an AC-DC converter is required and generally an inductor and capacitor in the AC-DC converter needs to be incorporated in the circuit, thereby causing the size and weight of the corresponding LED system to be increased (Zong et al., 2009). Therefore, such an LED chip embedded with a proper connection topology and driven directly by an AC source without any converters, could reduce the size and weight of an LED system while enhancing reliability.

For providing functionality to LED die to operate under AC mode operation, a few approaches have been reported on LED chips and LED mounted packages (Dayal et al., 2012; Kuo et al., 2010). The AC mode operated LEDs are generally composed of anti-parallel LED arrays, so that each LED would be operated for half of an operation cycle—that is, during a single AC cycle, one of the dies turns on at the positive half cycle while the other is off during the negative half. The alternating illumination enables the appearance of continuous light when using a normal AC source.

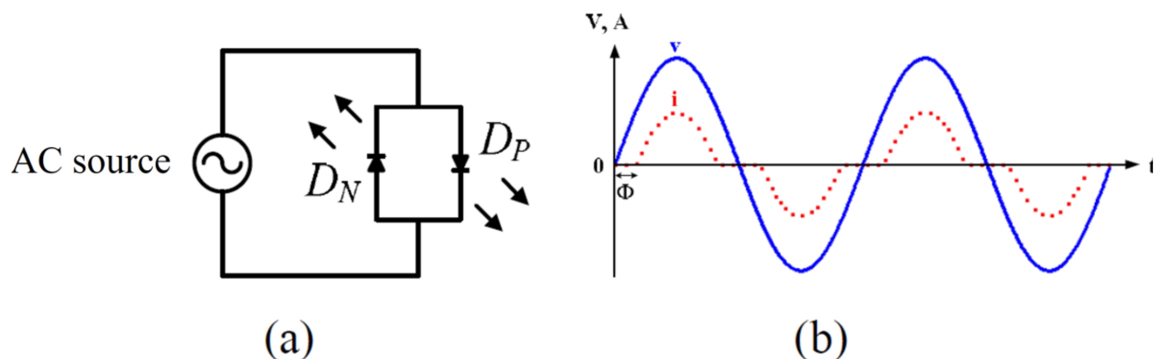

Figure 1.5 Concept of equivalent circuit of AC-driven LED and correlated waveforms of voltage and current in a AC periodicity (Kuo et al., 2010)

However, even though the prototype to operate the LED device by the AC source is presented, the current package-mounted AC-LED assemblies are still based on the traditional

framework package, in which each single LED die is connected by a bond wire to form the anode/cathode lead that reaches to the outer power source (Hwu et al., 2013). Conductive adhesive and/or soldering are also key connection process for an LED package to receive power. The typical configuration and the real device of the assembly is shown in figure 1.6, in which the bridgeless LED dies connection contains a resistor as a current regulator.

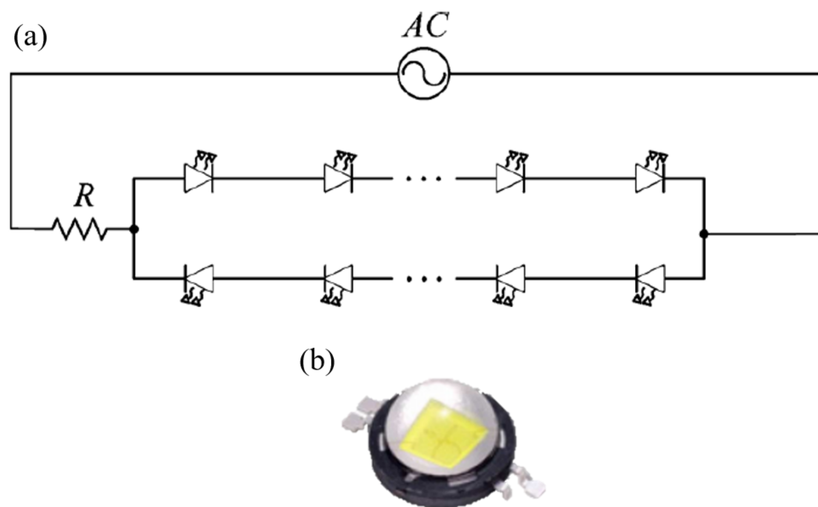

Figure 1.6 A typical design and product of AC driven LED bulb with the current regulator of resistor (Hwu et al., 2013)

Efforts have been made to minimize the size of the construction of the assembly by integrating multiple dies on the same substrate, nevertheless, the basic configuration is still be the mode of die-wirebonding-substratebonding/soldering, which limits the potential application where miniaturization and mechanical flexibility are desired. Thirdly, packaging technology requires a high accuracy with low tolerance in manufacturing because of the complexity of the assembly, and because the mounted units of die, connection leads, adhesive/solder layers and the substrates of conductive layers s are attached with each other

mechanically. The multiple packaging steps also lower the yield because the chance of processing failure increases during the independent fabrication of each component.

To overcome shortcomings mentioned above, we hence developed a new design of the configuration and structure of an AC-Driven LED. Still, the basic idea is connecting the LED die in antiparallel. But instead of integrating the mounted wire bonded LED bulb, the LED die are embedded in a polymer with the both anodes and cathodes contacted with a conductive layer. Then dielectric layers, which comprise capacitive elements, are coated on both sides of inner conductive layers. With the fabricated dielectrics, AC operation is achieved. After the final contact layers are deposited a layer-by-layer assembly is built up in a sandwich structure, shown in figure 1.7, the polymer embedded dual-LED portion acts as the light emitting core layer and the two layers of dielectrics coated on both sides form the capacitive coupling, enabling the LED chip to directly receiving power from an AC source.

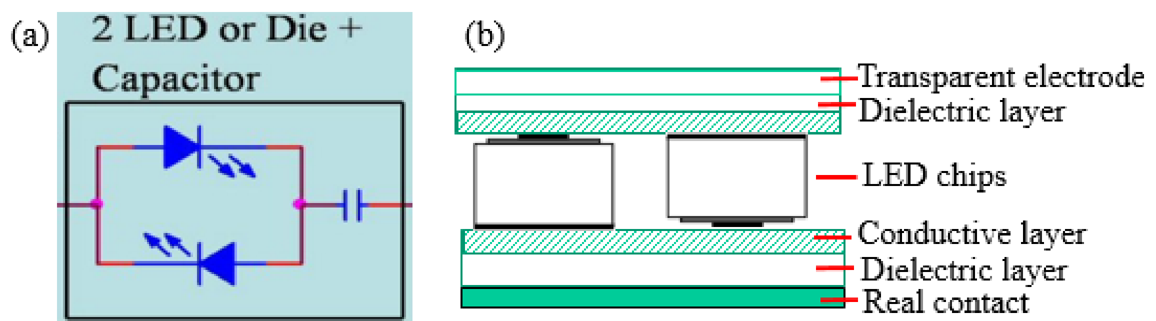

Figure 1.7 Schematic of basic device:(a) principle circuit; (b) layer-by-layer structure

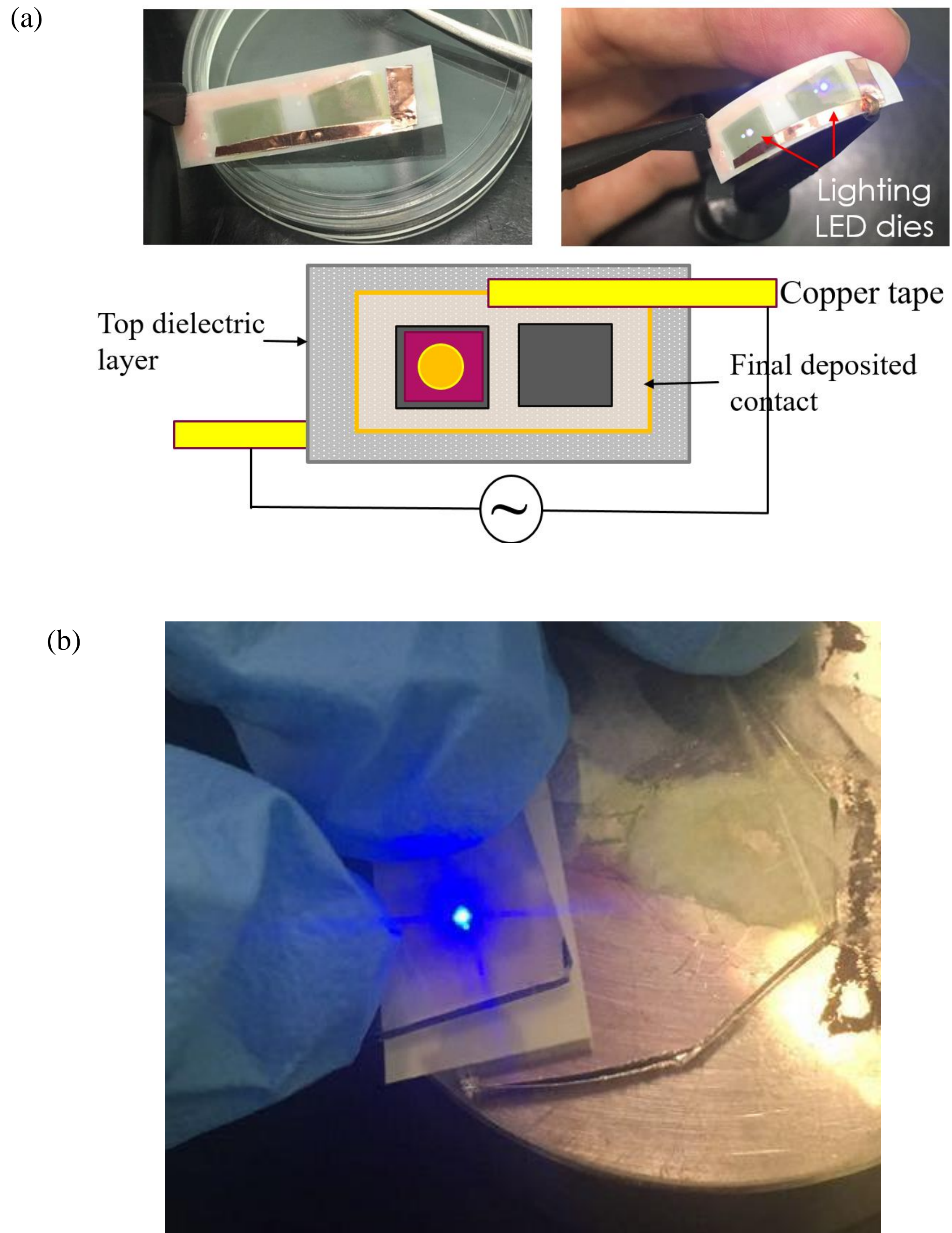

Figure 1.8 Wirebonding-free working dual-LEDs assembly with dielectric layers: (a) in the schematic of electronic test, the centric orangish area representing the final deposited contact area and the grey area representing the dielectric composite as the capacitor; (b) the dual-LEDs assembly is powered by an AC source with the contact of two layers of ITO glass

Shown in figure 1.6 and 1.7, the polymer matrix is formed by epoxy resin, which covers the edges but not the anode and cathode contacts of LED dies, and each unit contains two dies, one facing up and one facing down, with their electrodes accessible and slightly elevated relative to the epoxy matrix. Between the core layer and the dielectric layers electrodes are symmetrically formed by transparent conductive layers, which can be either Silver Nanowires(AgNWs) networks or a combination of Ag Nanowires and Indium Tin Oxide(ITO). Then Barium Titanite, $BaTiO_3$, functionalized epoxy composite is attached on the sides of the transparent conductive layers. Lastly, after another two transparent conductive layers are applied, the final assembly of polymer embedding AC-driven Dual LED is accomplished.

Overall, the package method of LED dies described in this thesis allows for the smallest possible packages measuring under 0.6 mm in length. It also eliminates the requirement for external components and can enable flexible sheets or strips of LEDs in which the LED packages are virtually invisible. Compared with current liquid crystal displays and OLED displays, we can enable a display unit that is not only flexible, but that also offers a large improvement in the energy efficiency, while maintaining an attractive cost. Embedded in polymer film, the whole unit is able to tolerate bending with a bend radius as low as 6mm. The transparent conductive layers are composed by the combination of Indium Tin Oxide (ITO) and Ag Nanowires, to act as the electrodes of capacitors as well as attachment on the core light emitting layer, removing the need for soldering metal contacts. Also, the polymer-based LED chip assembly is cost effective in terms of raw materials price and

processing. Our unique packaging does not cause significant light loss because no additional resistance applied theoretically, thus greatly optimizing luminous efficiency.

In conclusion, the light emitting diode (LED), is the most important solid-state lighting source, and is widely used. However, the traditional framework of LED assembly requires both wire bonding and soldering/bonding, which limits the flexibility and further improvement of flexible LED lighting and display products. Thus, the fabrication and characterization of a novel prototype of an AC powered flexible dual-LED unit is investigated involving of two reverse-parallel-connected LED chips. The rapid alternating illumination of the two LED dies enables the appearance of continuous light when using AC sources, which is promising for large-scale flexible displays and lighting.

Chapter 2 Details of Materials Process and Assembly

In this chapter, the details of overall assembly are explicitly discussed and the steps of preparation are shown in figure 2.1. Panel (a-d) illustrate the fabrication steps of the Au-coated transparent LED/epoxy platelet with the combined Ag NWs and ITO as the back and top contact; (e) and (d) shows the processed of the semitransparent intact assembly with two layers of dielectric layer made of $BaTiO_3$/epoxy as capacitive coupling and the network of dispersed Ag NWs functions as the final contact. The steps of layer-by-layer structure and the key parameters are involved, as well as the quality issues and their related methods of improvement.

2.1 Structure of the Assembly in Details

The whole assembly is fabricated symmetrically, consisting of multiple functional layers of central lighting layer, $BaTiO_3$/epoxy composite layers, combined electrode of ITO/AgNWs as well as deposited Au layer. The light emitting layer is the central core layer, where two of LED dies are embedded in the epoxy resin in reversely parallel order, is comprised by the commercial LED chips, EZ290-n LED provide by Cree Inc., and commercial epoxy resin, EPO-TEK 301-2 provided by Epoxy Technology, forming the LED/Epoxy platelet. The thickness of platelet is around 145 μm, corresponding to the height of LED chips, including the 5 μm Au cathode bondpad and Au-terminated anode contact protruding out. On the both sides of core layer, dielectric layers are symmetrically fabricated as capacitive couplings to powder on the LEDs. The capacitive couplings are composed by $BaTiO_3$ functional epoxy composite.

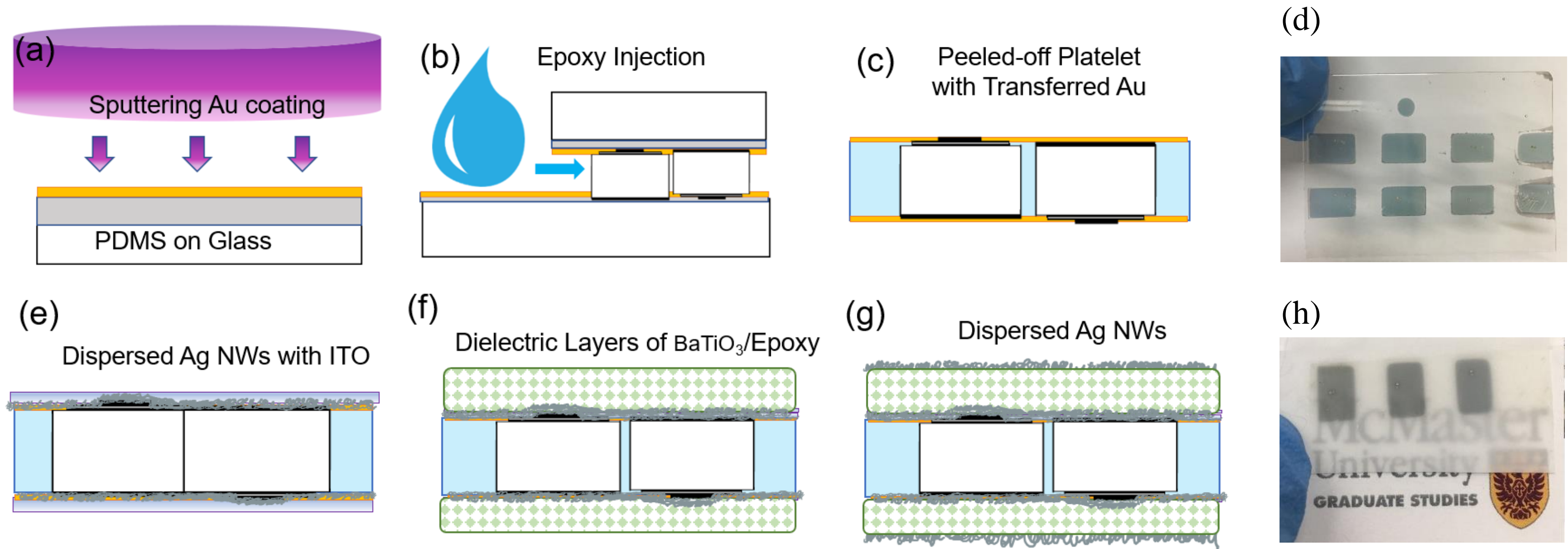

Figure 2.1 Schematic of the packaging process flow of the flexible AC-driven Dual-LED unit. (a-c) and (e-g) show the steps of the packaging method; (d) shows peel-off platelet containing eight darker area, each of which the pair of two LED die are reversely set with transferred Au film; (f) show the final intact assembly with the capacitive coupling, appearing semitransparent

2.2 The Fabrication Processes of the Assembly

2.2.1 Preparation of spin-on PDMS-coated substrate

Based on the spin speed-time-thickness relationship, we obtain a PDMS substrate able to hold the chip and protect electrodes well.

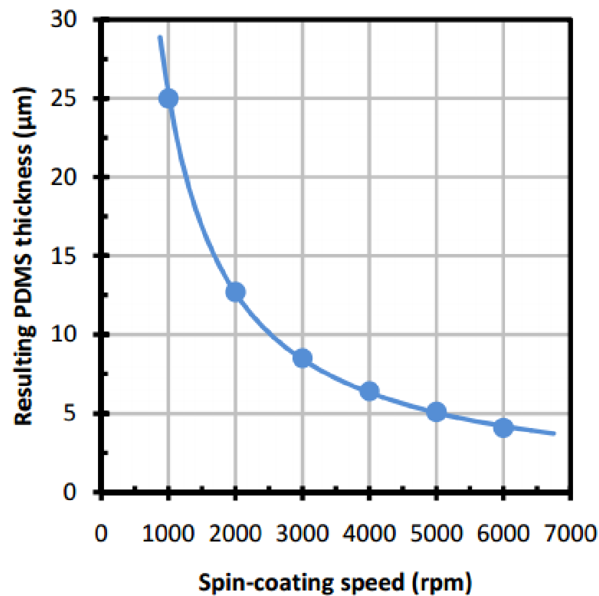

Figure 2.2 Thickness of PDMS Silgard 170 v.s. spin-coaring speed for 30 seconds on glass substrate

To utilize capillary insertion of epoxy, two parallel PDMS substrate plates need to be pre-pared in advance. There are some special and key requirements for the substrate materials: 1. providing proper range of retention to hold the micro-size LED chips; 2. physically re-pellant to liquid epoxy; if not, the epoxy might easily flow in between the holding layer and the contact area of LED chips, then sealing the electrodes and turning the cured epoxy to the insulating layer on electrodes; 2. elastomeric, properly elastic to cover the LED chip; 4. chemically stable and compatible to the curing reaction of epoxy: the candidates of

substrate are supposed to stay chemically inertia to curing process of epoxy and not participate in the solidification reaction, as well as to stay resistant to the terminated functional group of epoxy to make the epoxy film peelable from the substrate after curing.

The spin-coated PDMS film is used as the substrate to both hold the LED chips and protect the electrode (bondpad) of the chips. The ability of materials to hold micro-size chips can be achieved by various methods, such as attaching chips by viscous surface, wetting behavior and etc. However, in this work, if the attachment is too strong, it might destroy the topography of the contact area of chips and cause the negative influence on peeling off the core layer, namely the epoxy/ LED platelet. In this case, a substrate that is capable of providing proper retention by surface tension seems to be a good candidate to immobilize the LED chips on surface. in regard of the fact that the contact area, the bondpad of cathode and the Au-terminated anode, is required to be epoxy free and connected to the outer power, thus, a soft layer, that physically can be suitable to protect both electrodes via producing a strain to cap the contact areas of chips according. The degree of the holding force and strain is intrinsic to the thickness of the soft film, which is supposed to match the size of the tomographic size of the EZ290 LED chips. Finally, after the curing reaction of epoxy finishes, this material must be chemically stable and must allow the platelet to be peeled off from the silicone molding layers

Considering all the requirements of the substrate materials, Polydimethyl-siloxane (PDMS), namely silicone, is used as the buffering substrate to physically hold LED chips. PDMS is one of the most commonly used polymeric organosilicon materials, is our

choice because of its elastomeric, properties and chemically inertness after cross-link reaction is completed.

The Spin-on coating technology is applied to prepare a uniform film of PDMS on a clean glass sheet. According to the basic principle of Spin-On technology, the most important parameters to improve the film quality and obtain an ideal film of PDMS is the spin time and spin speed.

The spin-on time and speed are set at 30s and 3000 rpm to smoothen PDMS-coated substrates via spin-coating technique with a moderate elastomeric property and thickness, closed to the height of the bondpad of LED chips.

2.2.2 Epoxy Resin Injection by Axial Capillary Action

To fabricate the layer-by-layer structure assembly, the first step is to find a way to accommodate the LED chips in reverse directions while leaving the Au Bondpad and Au-terminated pad accessible to the outside circuit. In this work, we have developed a strategy of injecting the epoxy to anchor chips at their edges only and to form the epoxy matrix embedded with dual-LED chips by axial capillary force.

The basic strategy is to build up a “Substrate-Dual LED Chip-Substrate” Sandwich Structure, and then drop the proper amount of epoxy at room temperature so that the liquid epoxy will be driven by axial capillary forces in-between the space of the two plates of substrate.

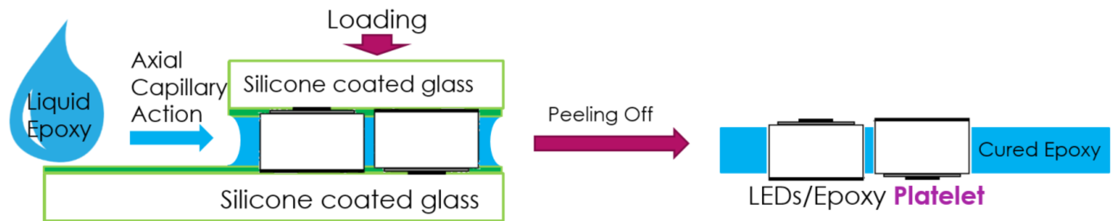

Figure 2.3 Details of the epoxy injection by axial capillary action and the platelet able to be peeled off after the epoxy curing reaction

In order to form a flexible support layer, a strategy of injecting the epoxy around the LED chips, as the core light emitter, is developed and void-free and intact LED/epoxy platelets are obtained. The thickness of the platelet corresponds to the size of the commercial LED chips used, approximately 5-8 μm thinner than the original chips, because the anode and cathode need to be free from the epoxy. In this work, the LED chips applied are the EZ290 Blue chips, provide by Cree Optoelectronics Inc., and the epoxy is Epo-Tek 301-2, whose mixing ratio is Base:Curing Agent of 100:35 by weight ratio. The curing process of the optical epoxy is performed at room temperature for 24 hours.

Driven by capillary force, the liquid epoxy will spontaneously fill inside space within the sandwich structure and after totally cured, forms a stable, flexible supporting matrix around LED chips. The LED chips are accommodated within the Epoxy matrix firmly, with both electrode free from by epoxy contamination and protruding out so that can be achievable bending radius of the platelet is as low as 5 mm.

The basic idea of this step is that, by applying a proper loading on the Silicone coated rigid substrate according to the Young's modulus of the PDMS, PMDS film will produce a compressive strain and is able to cover the protruding parts of electrode and repel the flow of liquid epoxy to produce a uniform pressure. Measured by topographic results measured by

the step profilometer (KLA Tencor D-100), the height of cathode Bondpad is approximately 5 to 6 μm and the diameter is approximately 90 μm, which are corresponded to data sheet of the EZ290. The spin-coating parameter of PDMS buffer layer is based on the results of Step Profilometer.

A selected number of Dual-LED chip pairs, one facing up and one facing down, are first placed carefully on the prepared PDMS coated glass substrate, and then covered with another PDMS coated substrate symmetrically on the top. Next, a proper amount of the mixed deformed epoxy liquid is dropped at the edge of the two sheets of the PDMS-coated substrate. Driven by the axial capillary action, the liquid epoxy will spontaneously flow into and fill in the space between solid phases, and then slowly surround the edge of chips inside while the top and bottom surfaces of chips are left uncontaminated. After cureing at room temperature, an intact sheet of solid phase epoxy with Dual-LED pairs embedded, can be peeled off from the PDMS-coated substrate, namely the Epoxy/LEDs platelet.

To test the reliability and evaluate the spin-coated the PMDS substrate, a profilometry test is taken to test the topography of the platelet. The protruding peak and area show the alignment of the two LED dies and indicate that they are free from the covering of epoxy resin and available to be contacted up the subsequent conductive layers.

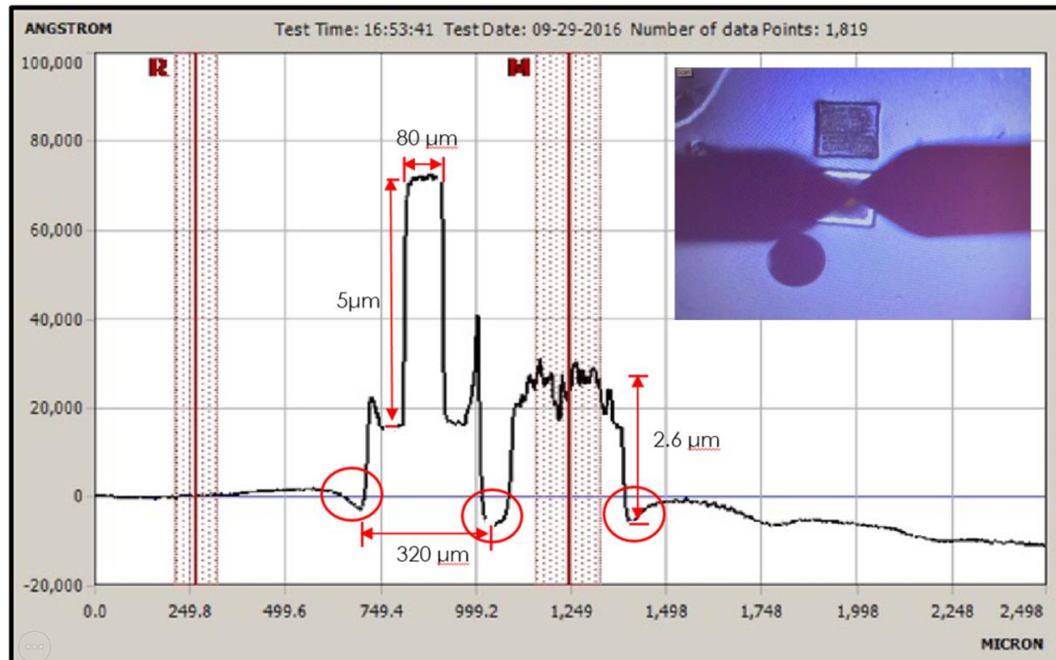

Figure 2.4 Profilometric graph show the real size of the bondpad and the cross part of the LED die, indicating both the cathode and anode part are free from epoxy resin

The basic strategy of epoxy embedding the dual-LED chip pair has been developed, however, the quality of the Epoxy/LEDs platelet must be improved: there are unexpected voids and bubbles in the structure of the epoxy matrix which will lower the binding strength between chips and epoxy and reduce the overall bending strength, and negatively affect the later assembly steps.

In the process of embedding liquid epoxy, the voids/bubbles will nucleate and grow spontaneously and randomly within the epoxy during the solidification process.

Thus, the issue of void/bubbles control needs to be investigated. The nucleation and growth process of voids during the epoxy solidification is shown in figure 2.5.

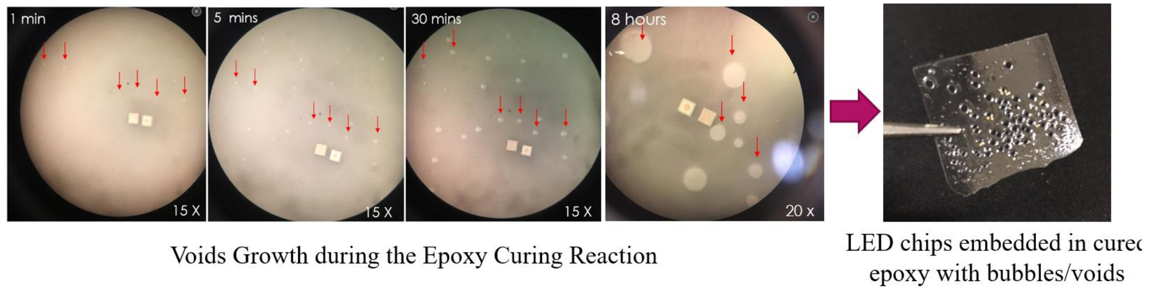

Figure 2.5 Void growth between the parallel plates coated with pure silicone during epoxy solidification

The liquid epoxy embedding process is concerned with the surface energy and wettability, which is involved with the phases of vapor, liquid and solid. Details of the mechanism and influence factors of the surface energy and wettability will be discussed in Chapter 4.

Table 2 Table of surface energy of common materials

Material	Surface Energy (mJ/m^2)
Glass	310 (Parikh et al, 1958)
Copper	1564 (Adamson, 1967)
Silicone	24 (Owen, 1989)
Teflon	18 (Ellison et al., 1954)
Au	1138 (Rhee et al., 1977)
Epoxy	46 (Abobott et al., 1988)

From the table 2 of surface energy of common materials, most of the metal and ceramic materials belong to the category of materials holding high surface energy, while most of the polymeric materials belong to the category of low surface energy materials, including the silicone and epoxy applied in this work. Thus, to modify the surface energy becomes the key to solving the problem. Surface modification of the silicone used as the thin film mold of high energy material becomes a possible solution. A thin film of Au prepared by

Physical Vapor Deposition (PVD, processed by S150B Edwards Sputter Coater, is used to treat the surface of silicone. The thickness of PVD Au layer should correspond to the surface roughness of PMDS and reported by Tang et al., 2015, the typical surface roughness is around 20 nm, after 120 seconds deposition**.**

In this way, the original low energy surface of silicone is substituted by the thin film of Au layer and hence the surface wettability of the spin-on coated silicone has been substantially improved. The modified hydrophilic silicone surface becomes suitable for the epoxy resin to wet readily thus forming an intact, void-free platelet within the Au-coated area.

Another benefit that comes with the Au coating is that the Au particles make the surface of the epoxy layer more suitable for the transparent electrode materials to be deposited in subsequent steps. During the curing process of the epoxy resin, the Au particle are almost entirely transferred from the coated silicone layer to the surface of the peel-off cure epoxy.

2.2.3 Transparent Conductive Layer Deposition

The transparent conductive layers play an essential role in the assembly because they are not only the partial components to build the capacitive coupling, removing the need for soldering metal contacts, but also function as final electrode to connect to the AC source. The transparent conductive layers are directly deposited in-between the core layer and the dielectric layers as a connection, and are also coated at the outer sides of the dielectric layers.

The efficiency of light extraction is considered to be one of most important. All the conductive layers used as the electrodes in the layer-by-layer structure, need to be optically

transparent. Thus, the network of dispersed Ag NWs can be ideal to constitute the electric bridge between the anode and cathode of the dual-LED chips and connects the core light emissive layer to the dielectric layer of $BaTiO_3$/epoxy. Also, the element of silver is an earth-abundant material.

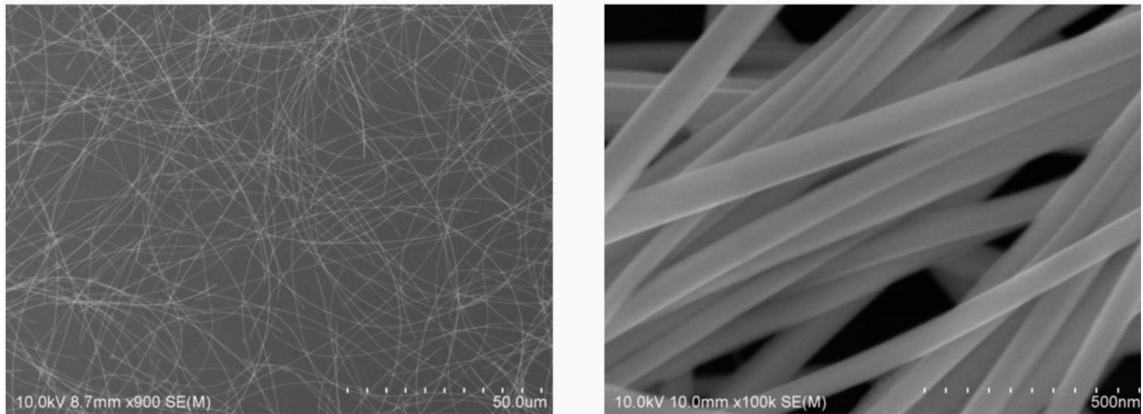

Figure 2.5 SEM images of the commercial Ag Nanowires (propertied by ACS Materials)

The commercial Ag Nanowires(AgNWs) is provided by ACS Materials and the typical data is listed in Table 3:

Table 3 Typical parameters of the commercial Ag NWs-L70

Products	Average Diameter	Length	Silver Purity	Concentration
Agnw-L70	70 nm	100-200 μm	~99.5 %	20 mg/ml

The combined Ag Nanowires (Ag NWs) are utilized and prepared to be the transparent contact for being conductive and highly bendable with proper transmittance. AgNWs, with diameter of 70 nm and length ranging between 100 and 200 μm in ethanol solution, are coated on by Meyer Rod Coating method to form networks on the surfaces of both sides

of the core layer as well as of dielectric layers as the final contact. The network of AgNWs serve as the conductive layer to constitute the parallel capacitor, with good flexibility. The flexible contact of Ag NWs film is prepared by #8 Meyer Rod coating and different concentrate Ag NWs in ethanol solutions dipped on the platelet result in different optical transmittance and resistant value. The as-coated AgNWs films on the platelete are demonstrated that the overall resistance of films sharply drops from more than 10M ohms/sq to 18 ohm/sq with a slightly decreasing transmittance from 88% to 75% as the dipping suspension concentration rises from 1 mg/ml to 5mg/ml.

The bare action of coating cannot exploit the best performance of Ag NWs because the poor joint condition may increase the junction resistance of the network. Also the physical adhesion of Ag NWs is weak to maintain a reliable contact. Usually either pre-treatment or post-treatment to melt the joints among different wires and improve the adhesion are necessary. Though the Meyer Rod coated AgNWs network shows good performance regarding sheet resistance (less than 50 ohm/sq) and flexibility as well as compatibility on the polymeric surface, the adhesion of AgNWs to both LED die bondpad and the $BaTiO_3$/epoxy is limited because the nanowires are merely precipitated but not attached to the solid substrate after the solution evaporating.

To improve the poor adhesion of Ag NWs network, Indium Tin Oxide (ITO) is deposited on the epoxy embedding dual-LEDs by Radio Frequency (RF) sputtering. Even though the techniques of depositing ITO via RF sputtering are at a mature stage, the challenge in this work includes the following aspects:

1. Mismatch of Coefficient of Thermal Expansion between the rigid LED dies and the thermal stretchable epoxy matrix.

2. Deposition of ITO on polymeric substrate. The atoms of ITO ceramic prefer to nucleate and grow on a crystalline substrate instead of an amorphous substrate.

Indium Tin Oxide (ITO) as the transparent electrode can be applied via Sputtering deposition.

Table 4 Sputtering conditions for ITO film

Sputtering Parameters	Value
Chamber Pressure	5-8 mTorr
RF Power (Watt)	45 Watt
Ar Flow	7.0 sccm
Chamber Temperature	25 - 30 ℃
Deposition time	2-30 mins

The target material of ITO is an In_2O_3:SnO_2(90:10wt%) ceramic and a thin film as the electrode was deposited on the both sides of core layer by Radio Frequency Sputtering.

During the RF sputtering process, the flowing of the plasma and the kinetic energy obtained from the target by the atoms will result in increasing the chamber temperature, and the typical deposition of ITO on thermal stable substrate is more than 400 ℃. Coefficient of Thermal Expansion between the used 301-RF epoxy is $39*10^{-6}$/℃ under the glass transition temperature and main material of LED chips, Gallium Indium Nitride(InGaN), as well

as the Si Substrate, is 3 to $5*10^{-6}$/°C. when the CTE of ITO is approximately $10 *10^{-6}$/°C. The obvious mismatch of CTE among these three materials might causes the thermal crack between the embedding frame of epoxy and LED chip and among the area of Epoxy, which is meant to cause the failure of the conductivity of ITO, if the common high temperature deposition process with typical parameters is utilized in this condition.

To avoid the thermal crack and wrinkle of ITO on the epoxy-based core layer, the condition of RF sputtering and the quality of ITO is investigated, and typical conditions of optimal deposition are obtained, which are shown in Table 4.

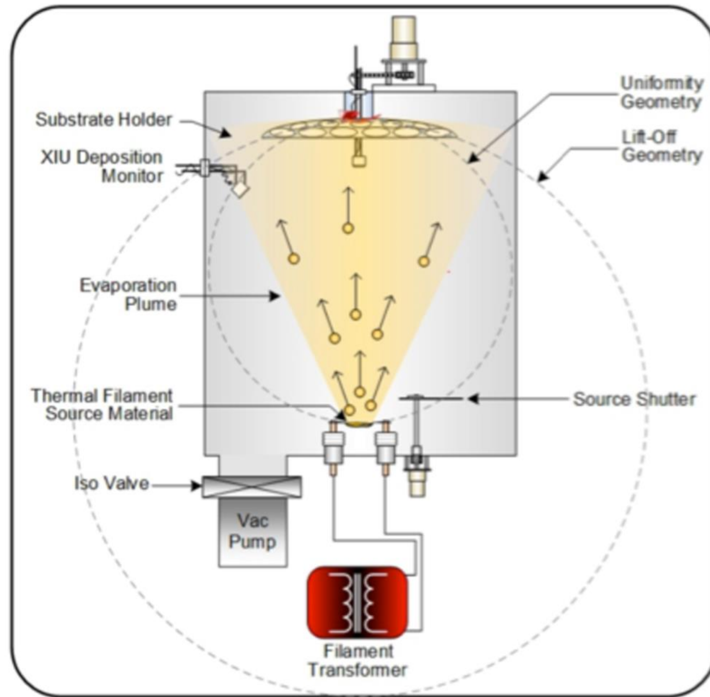

Figure 2.6 Schematic of ITO RF sputtering (Shin, et al., 2009)

After 5 minutes deposition under room temperature, the thickness is around 500 nm.

Then the ITO is further deposited on though RF sputtering coating and the precipitation of the ITO atom can reinforce the adhesion of Ag Nanowires to the substrate, making the contact area more effective. Besides, the deposited ITO could strengthen the joint of individual Ag Nanowires and thus lowering down the junction resistance, which is the one of the key factors to lower the resulting resistance of the overall Ag Nanowires network.

2.2.4 Physically Scattered $BaTiO_3$ Particles for Capacitive Coupling Fabrication

The capacitive coupling, which works as the AC/DC converter, which is explained in details in chapter 4, is comprised of two parallel plate capacitors and each capacitor consists of $BaTiO_3$ particles (2μm $BaTiO_3$ NanoOxide HPB-200, TPL Inc.) reinforced epoxy composite and the dielectric constant of pristine particles is above 1000. However, since the dielectric constant of the epoxy matrix is merely about 2.6, which is comparatively low, the overall dielectric constant of the composite cannot behave as well as the original $BaTiO_3$ particles. Also, the overall dielectric constant of the $BaTiO_3$/Epoxy is decided by the volume ratio.

Thus, to minimize the volume ratio of the epoxy while maintaining the entirety of the dielabectric layer becomes the key goal to achieve an overall dielectric constant as high as possible and to form an optimized dielectric layer. Here, a single layer of 2μm $BaTiO_3$ particles is prepared by physically scratching and scattering by Gel-film provided by Gel-Pak Inc. The Gel-Film is a sticky film with Gel material on a metalized polyester substrate, which can provide a wide range of retention to hold the object materials/devices on the surface, such as kitting of small components and sealing gaskets. After the $BaTiO_3$ particles is well scattered on the Gel-Film, epoxy is applied to fill in the inter-granular space between

the $BaTiO_3$ particles to maintain the integrity of the layer and yet pressure being loaded to minimize the volume ratio of epoxy. After the epoxy totally cures, the semitransparent dielectric layer is obtained with a thickness around 7μm. The main steps to accomplish the monolayer of $BaTiO_3$ particles filling in epoxy are as follows:

Firstly, randomly disperse an excessive amount of $BaTiO_3$ particles onto the surface of soft silicone elastomer film, namely the Gel-Film WF X8. Take another piece of Gel-Film and gently cover it for the first Gel-Pak adhesive with $BaTiO_3$ particles and peel it off, therefore the excessive $BaTiO_3$ particles are attached and transferred to the surface of the second Gel-Pal, so as to remove extra amount of $BaTiO_3$ particles away. Repeat 5-6 times or more times until the $BaTiO_3$ particles form a uniform surface on the Gel-Pak film, and then keep the piece of Gel-Pak with a comparatively smooth and uniform surface consisting of $BaTiO_3$ particles. Repeat the same procedure of first step to make another similar piece of Gel-Pak with $BaTiO_3$ particles. The statuses of $BaTiO_3$ on Gel-Pak are shown in Figure 2.7. The dark white area in the subfigure (A) indicates that $BaTiO_3$ particles are stacking in multiple layers.

Secondly, take these two $BaTiO_3$ particles adhesive Gel-Pak and gently scratch with each other to destroy the physical adhesion of individual $BaTiO_3$ particle and grind off the $BaTiO_3$ particles at outer layers. Then check the topography of the final fine films under optical microscopy to ensure there is no obvious void or bump appeared across the whole film. As seen in subfigure (b) and (c), the opaque film of solid $BaTiO_3$ particles gradually becomes semi-transparent, which shows excessive particles are rubbed and scratched away

by the second layer of Gel-film, and eventually no obvious white spot exists and ideally, there would be a single layer of $BaTiO_3$ particles remained on the surface of Gel-film.

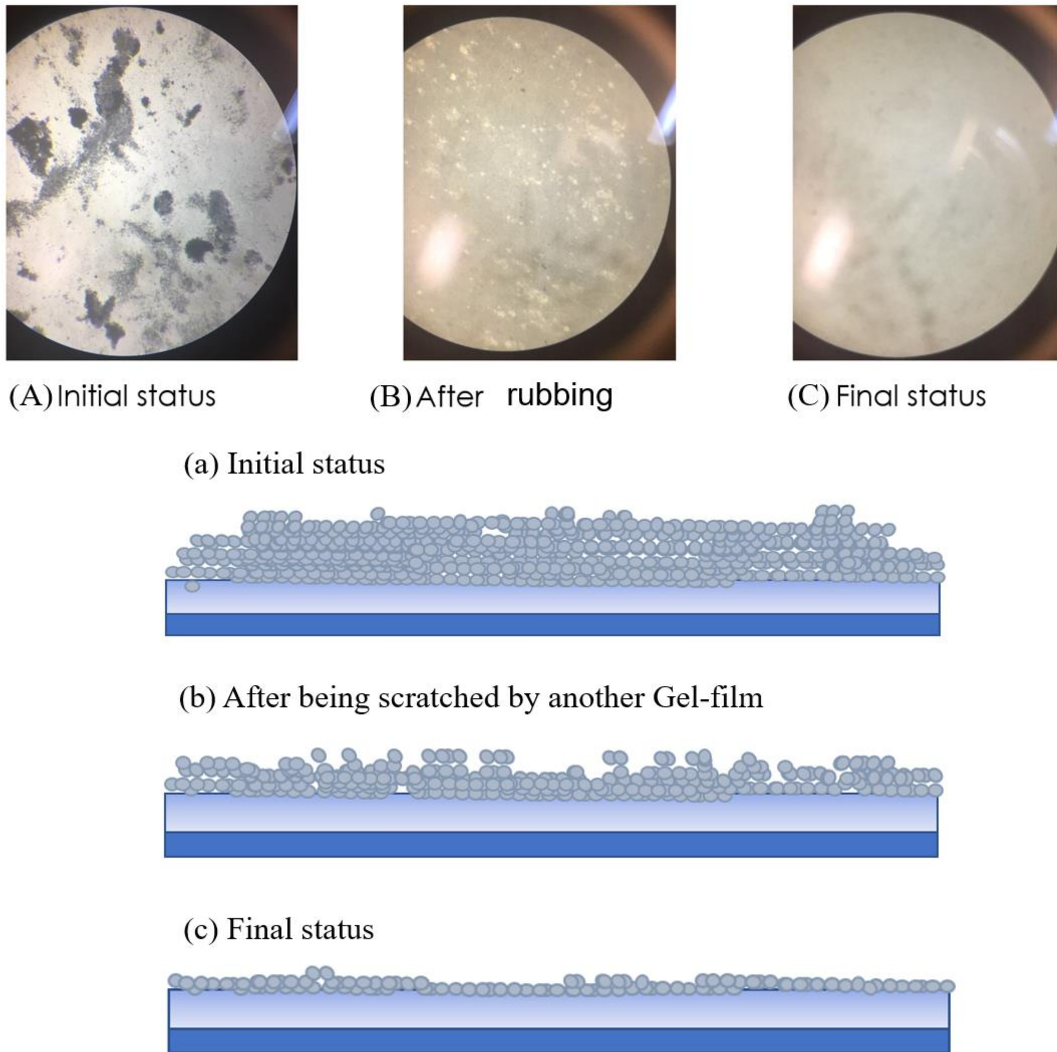

Figure 2.7 Status of the $BaTiO_3$ particles dispersed on the Gel-Pak during the peel-off process: (A), (B) and (C) show the status of each steps under optical microscope; (a), (b) and (c) are the schematics illustrating the status of $BaTiO_3$ particles on the Gel-film

Lastly, drop a suitable amount of Epoxy resin on the two pieces of fine $BaTiO_3$ particles covered Gel-Pak films and entrap the LEDs/Epoxy platelet, the light emitting core layer in between. Then wait for the resin to permeate and fill in porosity of $BaTiO_3$ particles and

apply loading on the top of Gel-Pak to squeeze out the excessive resin. After the epoxy finishes the solidification process, the assembly with the dielectric later on each side is accomplished.

Chapter 3 Results and discussion (regarding to the materials processing and characterization)

In this chapter, a novel transparent electrode of combined ITO/AgNWs has been processed as the transparent conductive layer. Before evaluation the performance of the combined electrode of ITO/Ag NWs, a brief description of the nature of ITO and needs to be clarified before discussing the results of the experiment.

3.1 Optimal Sputtering Conditions for ITO Deposited on Epoxy Substrate

In order to better explain the improved embedding process and evaluate the nature of ITO, a brief background and description of ITO commonly deposited on flexible substrates is provided before the results of the experiment.

Indium Tin Oxide (ITO) is the most commonly used transparent conducting oxide for flat panel displays (FPDs) because of its unique electrical conductivity and high level of optical transparency in the visible part of spectrum. Although many efforts have been made on the deposition of ITO films on polymer substrates (Shin et al., 2001; Craciun et al., 2000; Park et al., 2001), the nature of fragility and brittleness of ITO limit its application in large area flexible electronics, such as curved displays or bendable solar cells.

It has been reported that for ITO films deposited on polyethylene terephthalate (PET) substrates, the sheet resistance of thicker ITO film (105 nm thickness) increases rapidly at low strain, while the sheet resistance for the thinner ITO film (16.8nm thickness) began to increase comparatively slower when suffering from a low strain. The rupture of ITO membranes usually begins with a strain of 2-3% and is associated with a sudden increase in resistance (Cairns et al., 2000). There is a trade-off between the use of thick ITO to reduce

the resistivity and the use of ITO thin films that can withstand greater strain in the substrate. An organic buffer layer can improve the affinity of ITO to polyethersulfone (PES) substrates, thereby improving the mechanical properties of ITO films (Lin et al., 2008). there is also a technical problem of heat treatment required in ITO processing that adds to the difficulty for ITO films on polymeric substrates. Specifically, the requirement of heating substrates during the sputtering process and the high temperature post annealing for the ITO film may trigger the formation of cracks in ITO film, invaliding its application as a conductive layer. It is reported that the deposited substrates are required to be heated up to 250 ℃ (Terzini at el., 2000) and the post-annealing (> 200 ℃) is suggested for optimizing the properties of ITO film. The typical sheet resistance of the optimal sputtered ITO on glass substrate is below 5Ω/sq with the transmittance is above 90% in the visible region. However, most of the thermoplastic polymers cannot tolerant the processing temperatures above 200 ° C, and ITO films must be deposited at low substrate temperatures without post-annealing, and the possibility of annealing temperatures more than 200 ℃ is ruled out. As stated above, the preparation for the ITO transparent conductive layer on polymeric substrates remains a challenge because of the limited flexibility of ITO which is a ceramic. The lack of literature for the deposition of ITO on epoxy makes it necessary to investigate on the optimal conditions of processing ITO films on epoxy at room temperature.

3.1.1 The Thickness of ITO Films Relevant to Deposition Conditions

It is widely accepted that the optical and electrical properties of ITO changes is largely dependent on its thickness (Kim at el., 2006). To investigate the relationship between the sheet resistance and thickness of ITO on epoxy film, ITO film was prepared by RF sputtering using an oxide ceramic target (In_2O_3:SnO_2=90:10 wt%) under DC power of 45W. Working pressure was maintained under the pressure of approximately 10 mTorr according to previous work of deposited ITO film on a plastic film(Kim et al., 2005). The thickness of the ITO film is measured using the PZ2000 ellipsometer.

Given the technical problems of depositing ITO films on polymer substrates, the ITO films were first prepared on glass microscope slides at room temperature without annealing to investigate the relationship of ITO thickness and sheet resistance(R_s). The thickness of ITO films ranges from 40 nm to 210 nm. The variation of the sheet resistance with thickness is shown in the Fig. 3.1. The ITO shows an acceptable value of the R_s (550 Ω/sq) at the thickness of 40 nm. The R_s drops downs fast to 150 Ω/sq as the thickness accumulates to 80 nm. When the thickness increased to approximately 100 nm, the R_s decreased to 75 Ω/sq, as half as the value of 80 nm. As the thickness gets thicker to 120 nm, the sheet resistance of ITO film continues lowering down slowly and gradually approached 48 Ω/sq. Finally, as the thickness grows to >120 nm, the resistance eventually reaches at a stabilized level and the R_s remains at ~ 50 Ω/sq.

Through the graph of the sheet resistance v.s. thickness of ITO film, it can be observed that the thickness of films strongly impacts the sheet resistance of deposited ITO on glass substrates. When the thickness of ITO film reaches 100 nm, even without heating the substrate

during deposition and also without an annealing process, the sheet resistance of ITO film is as low as 70 Ω/sq. Because t capacitive coupling is integrated in the final assembly of our LED assembly, electrodes whose resistance is smaller than 100 Ω/sq is adequate. Since the four-point probe method cannot be applied, the corresponsive sheet resistance of ITO on epoxy substrate was measured based on measurement taken on ITO films deposited on the glass substrate deposited on the same conditions. The results show that the sheet resistance of ITO on epoxy is not as stable as the values of ITO on glass and the uncertainty of measurement is comparably large, which indicates a variation range of ±50%. Nevertheless, the relationship of the thickness and resistance of ITO on glass points out the tendency and proves the sheet resistance of ITO decreases drastically as the thickness increases from 40 nm to 100 nm. Given the influence of the depositing thickness on the sheet resistance of ITO, it is necessary to investigate the optimal sputtering conditions in regard to RF power, and working pressure at room temperature. Besides, once the thickness accumulates to 100 nm, the further growth in thickness will not result in a huge change in the value of sheet resistance, thus, the thickness of 100 nm becomes a critical value for the ITO film to be qualified as the transparent conductive. A further rise in thickness might make the ITO film on epoxy more vulnerable because the chance of thermal cracking increases as the s sputtering process is prolonged. Therefore, it is essential to investigate how the deposition conditions of RF power and working pressure of the vacuum chamber determines the thickness of ITO film on epoxy. It is then possible to optimize the setting of RF power and chamber pressure to determine the minimum resistance of the deposited ITO thin film.

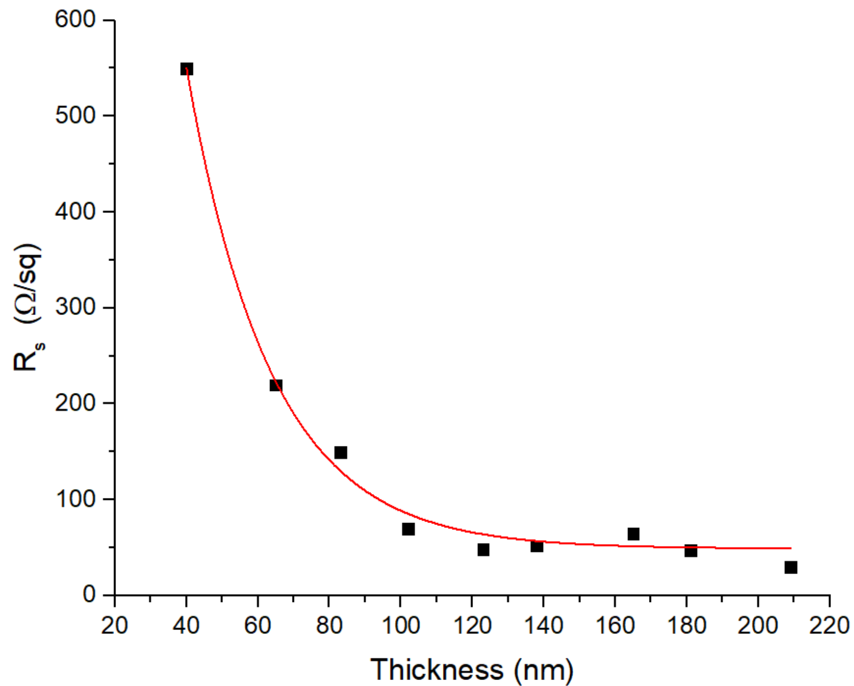

Figure 3.1 Sheet resistance of ITO films in variation of thickness

In the following section, the influencing factors of RF power and working pressure on the deposition rate of ITO will be discussed separately and suitable sputtering conditions will be determined to optimize sheet resistance.

3.1.2 The Influence of RF Power on Deposition Rate

The working pressure of the vacuum chamber was first set at 10 mTorr in a moderate range between 1 to 20 mTorr (Yasrebi et al., 2014) to investigate the relevant deposition rates of various RF power levels. Three groups of ITO films on epoxy substrate that were sputtered were measured in thickness to determine the deposition rates at sputter deposition powers of 30W, 45W and 60W respectively, which are shown in figure 3.2.

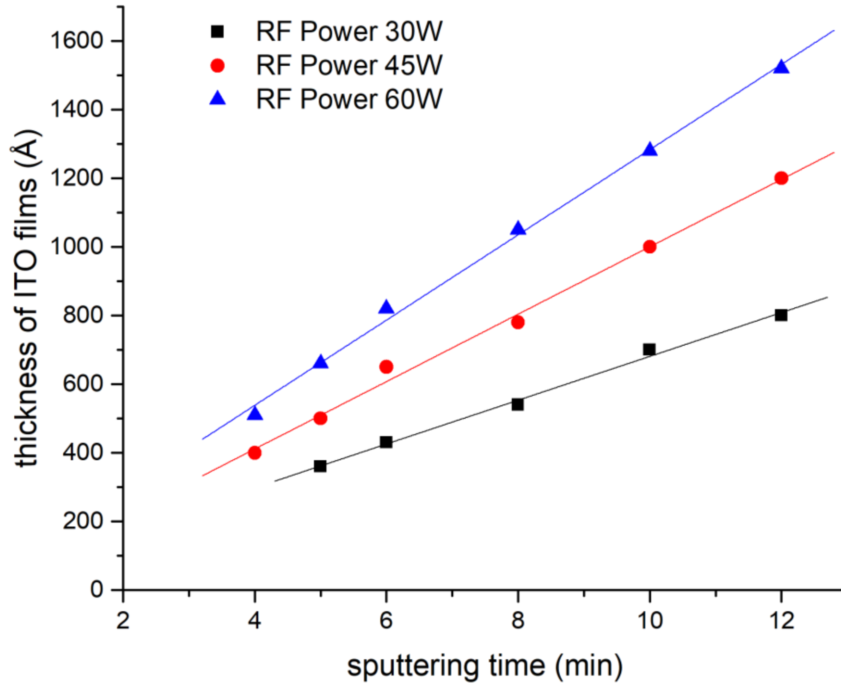

Figure 3.2 Thickness of ITO films in various of sputtering time via different RF powers

The results show that thickness of ITO films increase linearly as the sputtering time increases which means the ITO atoms are accumulated gradually on the epoxy substrate at a nearly constant rate. The deposition rates at various RF powers can be calculated by the slope of thickness-time lines. The deposition rate is (63.84 ± 2.54) Å /min at 30 W, 98.21±3.69 Å /min at 45 W and (123.21± 3.42) Å /min at 60 W respectively. The thickness versus sputtering time shows the linear relationship within the moderate time range.

In the figure 3.3 of the deposition rate versus sputtering power, there is an obvious linear rise of the rate as the RF power increases from 20 W to 60 W when the working pressure keeps at 10 mTorr.

The deposition rate at 20 W is 45 Å /min and the deposition rate at 60 W is 124 Å /min as mentioned above, nearly three time as the one at the low power of 20W. For the range of RF power between 35 W and 50 W, the slope is slightly above the average slope.

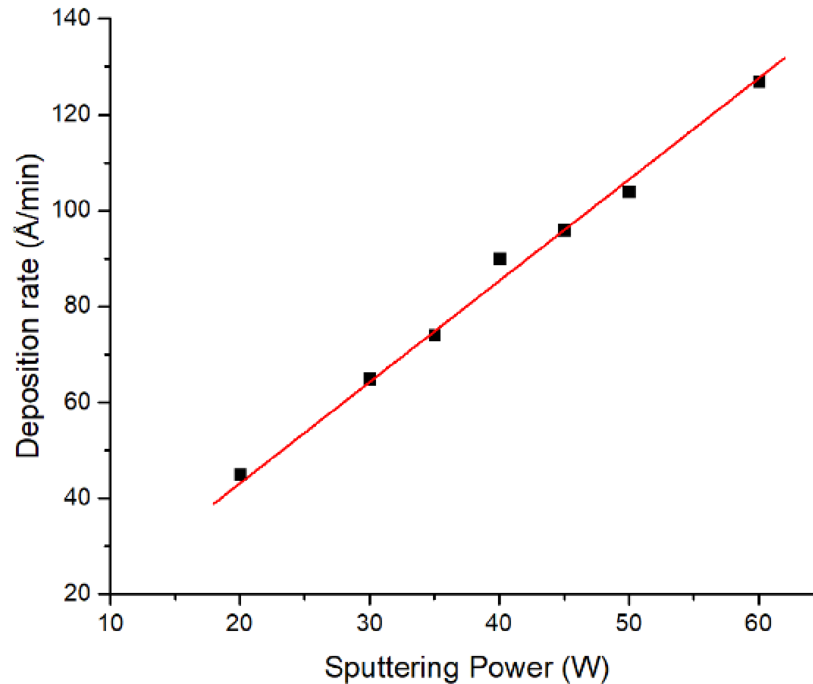

Figure 3.3 Deposition thickness rate of ITO films versus sputtering power

Under a fixed chamber pressure, an appropriate increase in RF sputtering power efficiently improves the deposition rate because the RF power is beneficial to the ionization of the discharge carrier, Argon, increasing the energy of the Ar^+ ions in the vacuum chamber. The higher sputtering energy therefore provides sputtered ITO atoms a higher kinetic energy to adhere to the substrate. On the other hand, the lower RF power produces a lower density of excited ions and lowers the average energy of the sputtered atoms, thereby, slowing down the deposition rate. It is ideal to keep the RF power in an intermediate range, ideally between 30 W to 60 W because when the RF power is set too high, Ar^+ ions will obtain a

large kinetic energy and hit into the deeper depth of the target and can hardly escape and bombard off the ITO atoms at surface. The high-energy ITO atoms that are successfully sputtered out will produce a large thermal effect to the epoxy substrate, which is sensitive to the rising temperature and easily exhibit thermal expansion, causing thermal cracking in the ITO film structure. Considering both the effects of RF power on deposition rate and substrate stability, a RF power should be kept within a moderate range.

3.1.3 The Influence of Working Pressure on Deposition Rate

The working pressure in the vacuum chamber of the sputtering system is another influencing factor on the deposition rate. The vacuum chamber is filled with Argon ions, which are ionized under the electrical potential of alternating current at radio frequency of 13.5 MHz. The ITO atoms therefore are bombarded out from the surface of target materials by the high-energy Argon ions and then impinge on the epoxy substrate, forming the thin film layer. The working pressure of the vacuum chamber mainly affects the number of atoms that can be ejected from the target and further deposited on the substrate and thereby decides the areal density of ITO atoms ejected from the target material.

To investigate the deposition rate as a function of working pressure, a group of the ITO films were measured in thickness, which were prepared under different working pressure, from a several to hundreds of millitorr, with RF power of 45 W for 10 min at room temperature.

The relationship between the deposition rate and chamber pressure is plotted in figure 3.3. The deposition rate of ITO film on epoxy is in a range between 65 and 100 Å /min as the RF power is fixed at 45 W. The results show that the chamber pressure is an important

factor affecting the sputtering rate of the film. The chamber environment is more suitable for the ITO atoms to be sprayed on the substrate at a low working pressure ranging from 3 mTorr to 15 mTorr, while the deposition process of ITO is comparably more difficult at high pressure of 30 mTorr and 40 mTorr. When the chamber pressure is higher than 50 mTorr, though deposition of ITO still can be grown, the quality of film becomes unreliable and the resistance of the ITO film is drastically increased and cannot be used as a transparent electrode. Therefore, only sputtering trials processed under 50 mTorr are recorded. In the low-pressure zone, the deposition rate increases from 84 Å /min to 98 Å /min, reaching at maximum rate, as the pressure rises from 3 mTorr to 10 mTorr. The deposition rate lightly declines to 91 Å /min, almost at the level, when the chamber pressure goes up to 15 mTorr, and the rate drops down to 82 Å /min under chamber pressure of 20 mTorr. The deposition rate at pressure of 30 mTorr and 40 mTorr is approximately 70 Å /min and 65 Å /min respectively.

The possible reason for the variation of rate for the changing pressure is that when the sputtering pressure is low, the number of Argon ions and collapsing atoms is reduced and the energy loss is comparatively small, which can improve the diffusion between the deposited atoms and the substrate, so as to increase the coating rate; if the pressure of the sputtering is smaller than a critical value, however, there would be a problem to start glow discharge and lack in the ions to hit the target. On the other hand, the high sputtering pressure will increase the number of collisions between the ions and target. The energy loss caused by the intense collisions between the ions and ITO atoms will result in the less kinetic energy for Ar^+ to bombard the target and especially for ITO atoms to precipitate on

the substrate. Therefore, the deposition rate drops down in the sputtering environment of the high working pressure. Also, more impurities present in the chamber can incorporate into the film at high sputtering pressures.

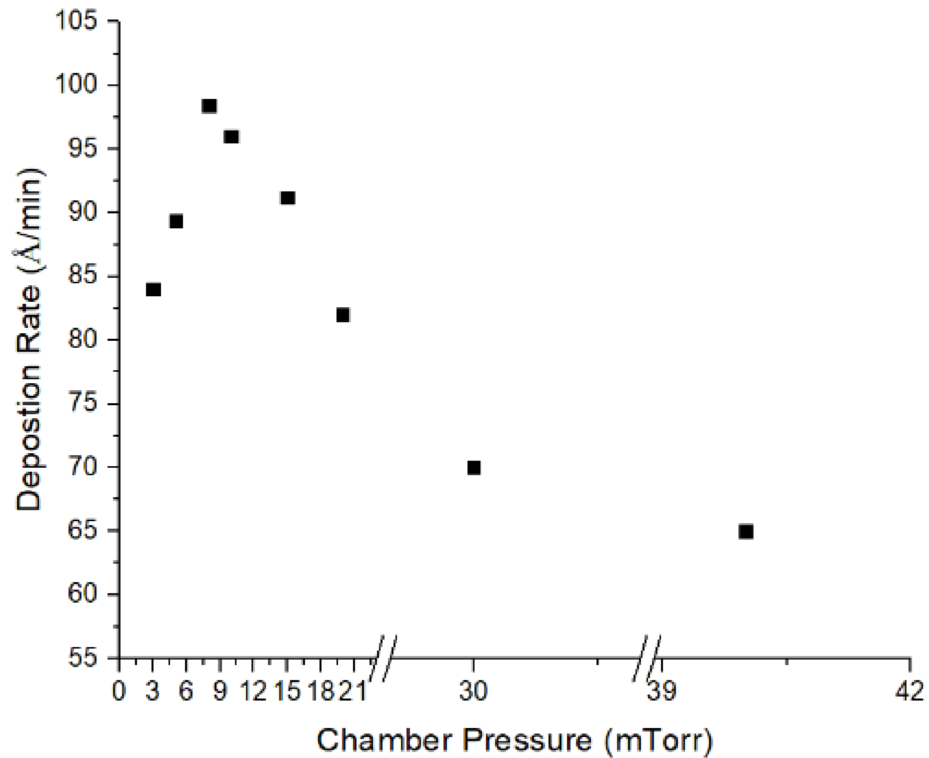

Figure 3.4 Deposition rates of ITO films relevant to the chamber pressure

All the ITO films are sputtered on the epoxy substrate by RF power of 45 W via various working pressure for 10 minutes. The films that are processed under a lower pressure show a better electrical performance than those deposited under higher pressure more than 20 mTorr, seen in figure 3.5. The sheet resistance of film at 3 mTorr, the lowest pressure that can be set for the pumping system, is nearly 80 Ω/sq. The minimum sheet resistance of ITO film drops to 32 Ω/sq at the pressure of 5 mTorr, which is the minimum sheet resistance among all the conductive films prepared. The sheet resistance of film remains

under 50 Ω/sq until the chamber pressure rises to 10 mTorr, at which the sheet resistance is 79 Ω/sq, slightly smaller than that of the film deposited at 15 mTorr. As the pressure is set over 20 mTorr, the quality of ITO film processed significantly falls off andthe sheet resistance increases from 200 Ω/sq to approximately 500 Ω/sq and 1000 Ω/sq as the pressure rises from 20 mTorr up to 30 mTorr and then to 40 mTorr. When the chamber pressure is set higher than 50 mTorr, the electrical properties of ITO films tends to become rather unstable, showing the sheet resistance more than 20 MΩ.

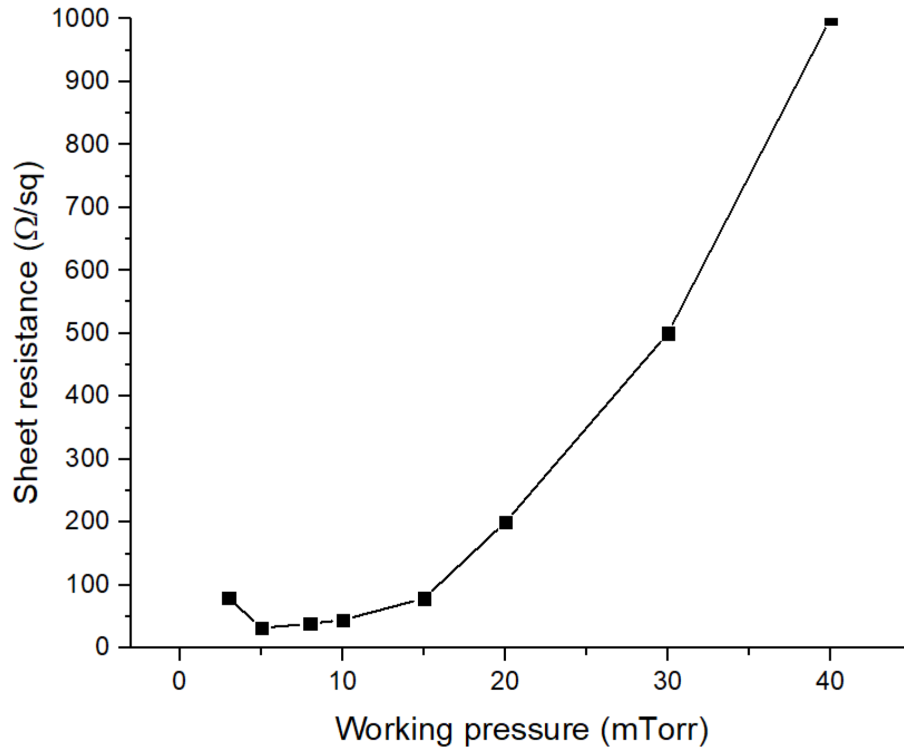

Figure 3.5 Sheet resistance of ITO films deposition at various of chamber pressure

The sheet resistance results of different ITO films indicate that the chamber pressure has a significant impact on deposition process and the quality of films. It is proven that the variation of sheet resistance is as a function of the different Ar^{+} densities on the roughness of

the deposited ITO films (Yasrebi et al. 2014)). In the condition that chamber pressure is lower than 15 mTorr, the increasing chamber pressure elevates the plasma density of Ar^+ and ITO atoms, and the enrichment of ion concentration is beneficial for the ITO atoms to precipitate on the substrate with a compact layer structure. The roughness test by the Atomic Force Microscopy images proved that the value of the sheet resistance is associated with the denser structure with lower roughness. On contrary, the further increase in working pressure will directly increase the resistivity. Song at el. (2007) reported that the Ar^+ ions in the chamber not only bombard the surface of the cathode target, but are also mixed with the sputtered target atoms and deposited on the substrate surface. Therefore, under the sputtering environment with pressure high that 20 mTorr, the excessive Argon ions entrapped in the film will trigger and form defects, loosening the structure, increasing the sheet structure as well as reducing its surface mechanical properties, seriously affecting the film quality.

3.1.4 Degradation of ITO film on Epoxy Substrate

Though the optimal conditions of depositing ITO film on epoxy substrate via RF sputtering method are determined, there is still a technical problem for processing high quality ITO films on polymeric substrate. The designed polymer embedding process for the platelet also makes the traditional method of ITO deposition improper in this LED assembly, regarding the poor mechanical property of flexibility. Even after the deposition parameters of ITO deposition at room temperature has been optimized, the ITO on the polymer substrate still cannot maintain a stable performance in electronic tests. A typical room-temperature deposited ITO on the LED/epoxy platelet is shown in figure 3.6.

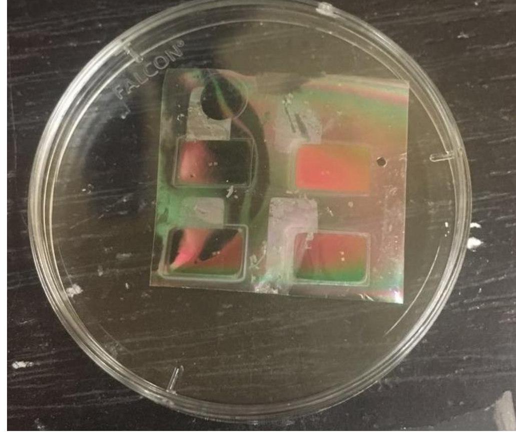

Figure 3.6 ITO deposited on LED/Epoxy plater in 6*3 mm pattern

The failure of the ITO film as the electrode mainly results from the following aspects:

1. The formation of defects because of the irregular surface topography of the LED/epoxy platelet. Imperfections, such as the voids or grooves, forming during the epoxy curing process because of the irregular shape of edges of the LED die are one cause of ITO failure The minor twisting and bumpy surface of the PDMS film also results in the imperfections on the cured epoxy. All the flaws happening in the platelet preparation process increase the difficulty for epoxy to wet the LED chips and increase the chance of forming defects in the platelet. The stress rise at these uneven areas of the platelet substrate can easily cause fracture in the ITO structure. As seen in figure 3.7, the groove covering around the cathode area results from the difference in horizontal level between the passivate layer and cathode area of the LED dies. Epoxy resin cannot properly touch and hold to the edge of die due to the mismatch on the surface of cathode pad. The point A in (c) is the at the bottom of the groove. The cluster of bumps at points B and C, along the edge of groove, are possibly caused by the twist of the PMDS film.

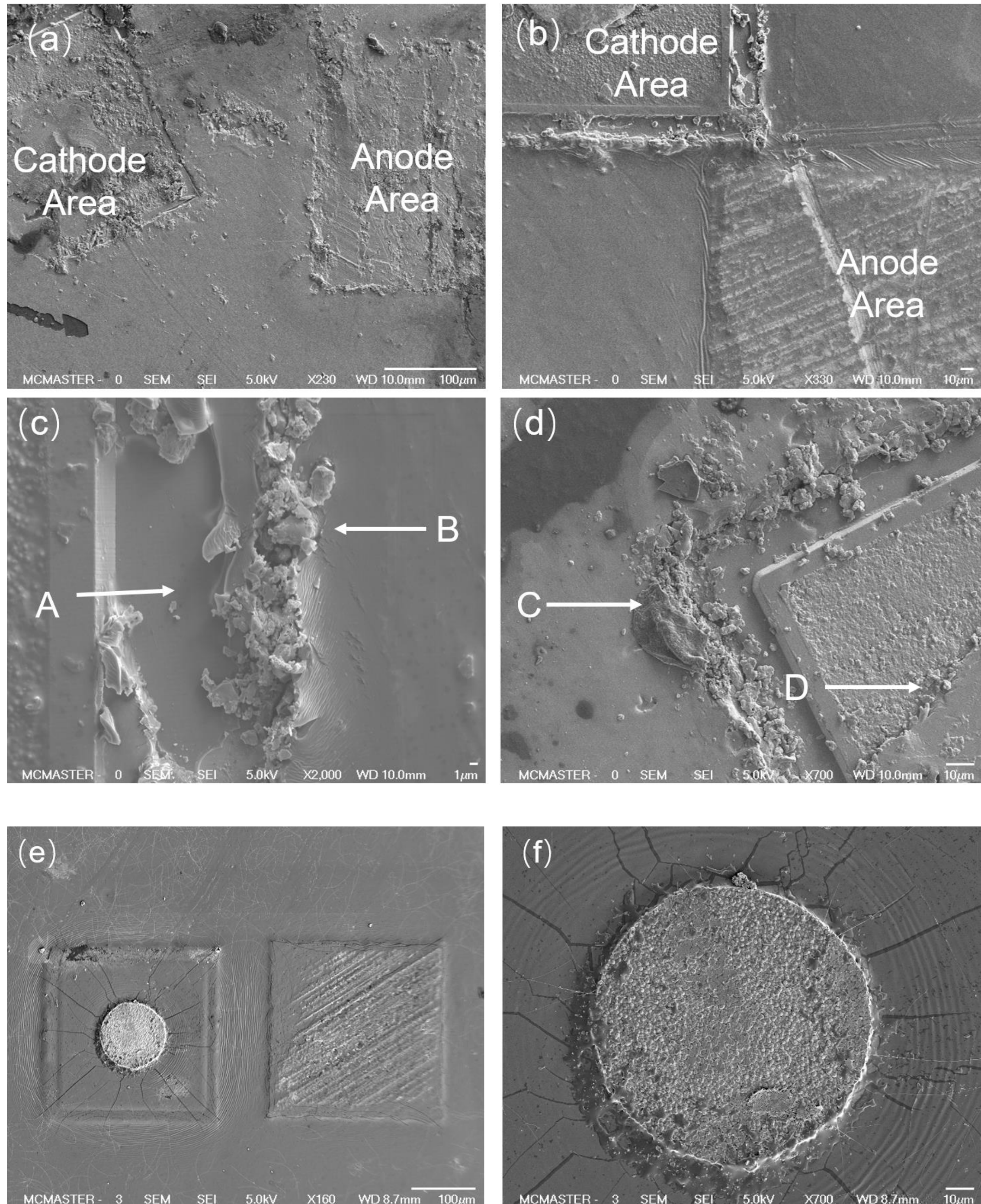

Figure 3.7 Microcracks caused by the irregular surface topography of dual-LEDs/epoxy platelet

Given that the epoxy matrix is free of defects and the area around LED chips is well-wrapped, the protruding bondpad of cathode and Au-terminated anode of dies remains difficult for the ITO film to fully and uniformly to coat. In subplot (e) and (f), the radiating pattern of cracks surrounding the protruding Au contact pad on the cathode area indicates that the internal stress is likely to be generated at the embossment on cathode area due to the difference in height and variation in properties of the two parts on the surface of the LED chip.

2. Thermal cracking on the platelet induced during the deposition process. Although an ITO layer with approximate thickness of 100 nm can be successfully sputtered onto LED/epoxy without obvious warpage, microcracks still occur along the barrier between LED chips and epoxy matrix due to the large difference in thermal expansion coefficient (CTE) during the deposition process. The undesirable condition can be explained from the stress variations between epoxy matrix and the components of metal/semiconductor on LED that are caused by the discontinuity of thermal properties, which triggers and generate the uncoordinated strain among the different parts on the film, sequentially inducing the microcracks along the boundary of LED and epoxy.

While no extra heat is applied during the deposition process at room temperature, the atoms of ITO are still bringing thermal energy to the platelet out of the plasma. The CTE (Coefficient of thermal expansion) of ITO film is less than 6.4 × 10-6 / ℃ and CTE of bulk gold is 13.2×10^{-6} / ℃ and the that of InGaN is 5.7 × 10-6 / ℃; however, the CTE of epoxy film is usually in the range of 61 to 180×10^{-6} / ℃. There is inconsistency between epoxy film and other rigid components.

Due to the large difference in thermal expansion coefficient (CTE) during sputtering, when the temperature in the deposition chamber increases, the polymeric substrate will expand while the rigid materials of LED dies almost constant. Then, the unbalance of the thermal strain will result in thermal cracking, which normally happens along the edge of the individual dies. As shown in figure 3.8, the thermal crack is caused by the unmatched thermal expansion between epoxy and LED die.

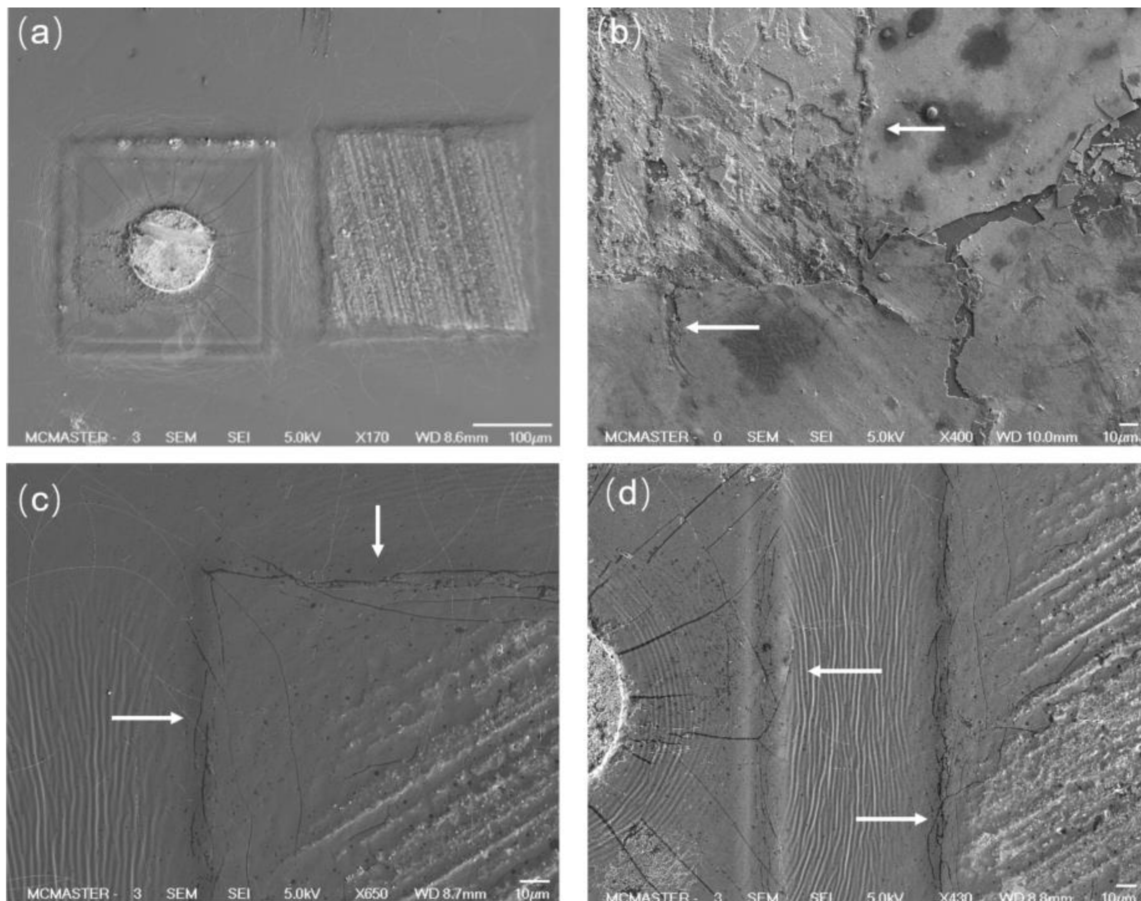

Figure 3.8 Thermal-induced cracks along the barrier between LED chips and epoxy matrix

3. Fracture in operation

Since the flexible display is often subject to stress to some extent, the effect of stress on the performance of the ITO film deposited on the polymeric substrate becomes an important problem. Even if a small stress is applied, the large difference in elastic modulus between the ITO film and the flexible polymer substrate and the deposited ITO film is vulnerable to be cracked on the flexible substrate because of its nature of brittleness, accompanied by a rapid increase in resistance.

Table 5

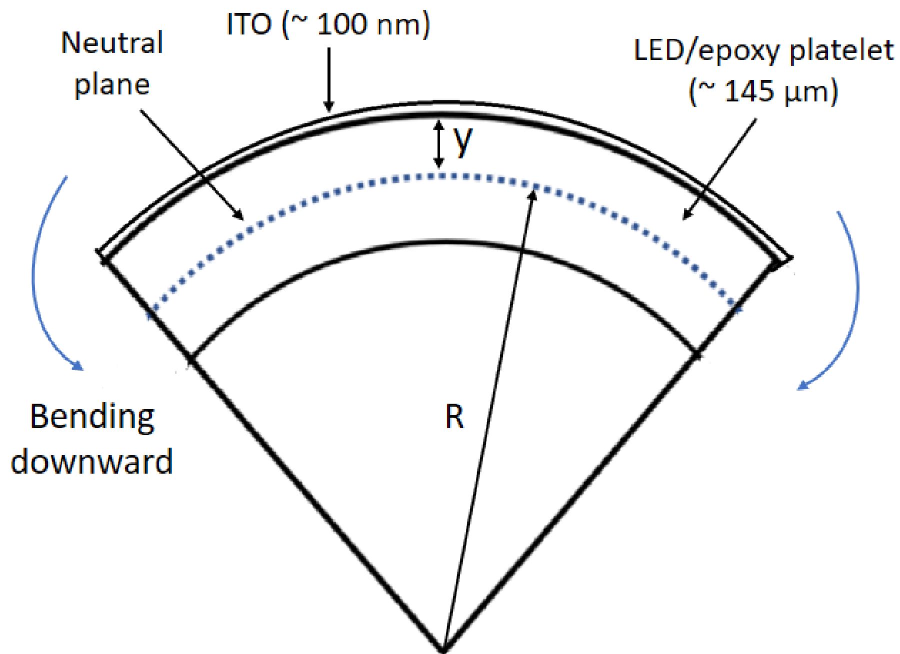

Figure 3.9 Schematic diagram of bending ITO-coated platelet

As shown in figure 3.9, when the ITO coated epoxy film (thickness of 145μm) is bent, the upper part above the neutral surface is subjected to tensile stress and the lower part is affected by the compress stress. The neutral plane is about the central plane of the CPP film.

The maximum strain is expressed as: s = y / R, where y is half the thickness of the epoxy film and R is the radius of the curvature. The platelet can be safely bent to a radius of curvature greater than 6 mm without reaching a destructive strain of an ITO film, nevertheless, the ITO can hardly tolerant any bending deformation.

The operating of LED by AC power in real circuits can also increase the temperature of the platelet. A local temperature rise leads to microcrack growth and coalescence, leading to peeling of ITO fragments on the surface of epoxy film. Accordingly, even after 5 minutes of operation, the resistance of the ITO layer is greatly increased and longer operating will further increase the local temperature, therefore causing irreversible destruction to the ITO film. If subjected to bending stresses, the degradation of the ITO layer is much faster. Under proper conditions, the original brightness from dual LED chips is able to go up to 300 cd /m^2. However, open circuit and turnoff might be caused by the coalescence of cracks in ITO film and failure of the platelet due to degradation of the ITO transparent electrode layer.

3.2 Network of Silver Nanowires(AgNWs) as Transparent Electrode

For the ITO layer used in flexible displays, the mechanical properties of the constant compression and tensile stresses are more challenging than the requirements for sheet resistance and visible light transmittance. As discussed above, the nature of fragility makes the ITO vulnerable in a flexible application and the failure caused by the microcrack initiated for various of reasons jeopardizes ITO suitability in this work. Considering the drawbacks of ITO in flexible/wearable electronics, efforts have been made to find potential substitute materials for ITO.

Silver Nanowires (Ag NWs), as one of promising candidates to replace the ITO, has increasingly attracted considerable attention due to is low sheet resistance and high transparency as well as its moderately flexible nature and ease of processing without requirement of high vacuum deposition (Ye et al., 2014). As a solution-processed nanomaterial (Lee et al., 2008), the networks of Ag NWs have emerged in the application of many flexible and wearable device, such as organic light-emitting diodes(OLED), curved liquid crystal displays, solar cells and touch panels (Sun et al., 2002; Zhou et al., 2014).

The network morphology impacts the overall performance of the AgNWs network. It has been reported that the diameter and length of individual nanowire determine the conductivity. It is reported (Bid et al., 2015) that the reduction in diameter of nanowire leads to the increment of resistivity because the role of surface scattering of electrons becomes dominant when the diameter of nanowire is closed or even shorter than the mean free path of electron for bulk silver (5.3308 nm, Haynes et al, 2014). The decrease of mean free path of electrons in the silver nanowire will consequently increase the resistance compared with that of bulk silver. On the other hand, the lengthening of the nanowire results in improvements in conductivity due to the nature of percolation of the conduction mechanism (Hsu et al., 2013). A percolation theory (Hu et al. 2004), specific to explain the conduction mechanism of the carbon nanotube, explains that it requires fewer nanowires to cover a given area if the nanowires are longer—the minimum number of nanowire to bridge across the area is inversely proportional to the length of the nanowires. Also, it is more difficult for electrons to pass the junctions among the nanowires than to flow within the structure

of a given wire. Thus, the longer wires mean less junctions and transfers for electrons to move, which contributes to the better conductivity of the whole metallic nanowire network. Since the resistivity of one single tube of Ag NW is 1.59×10^{-8} Ω·m, the most conductive metal in nature, the main resistance of the network of Ag NWs is contributed by the junction resistance, which is the resistance of the joint of different individual wires. Besides, as generally understood, it is also essential for AgNWs to strengthen the adhesion to the substrate to maintain a good performance in application. Therefore, either pre-treatment or post-treatment needs to be undertaken to reinforce the combination of individual silver wire so as to immobilize the AgNWs network and lower down the sheet resistance.

The approaches to improve the property of junction area include of thermal annealing, plasmonic welding, mechanical pressing, and encapsulating. The early-stage method is usually to anneal the as-coated AgNWs film at a temperature ranging from 180 to 200 °C for 30 to 60 minutes to fuse the junctions between wires to lower down the sheet resistance of the overall network. The typical sheet resistance of the thermally annealed AgNWs can be a few tens of Ω/sq with a transmittance closed to 90% (Madaria et al., 2010; Zeng et al., 2010). Given that the epoxy matrix is free of defects and the area around LED chips is well-wrapped, the protruding bondpad of cathode and Au-terminated anode of dies remains difficult for the ITO film to fully and uniformly to coat. In subplot (e) and (f), the radiating pattern of cracks surrounding the protruding Au contact pad on the cathode area indicates that the internal stress is likely to be generated at the embossment on cathode area due to the difference in height and variation in properties of the two parts on the surface of the LED die.). The other widely accepted post-treatment method is the photonic/laser sintering

method. (Jinting et al. in 2012) disclosed a strategy to process a highly adhesive Ag NWs film by utilized a radiant lamp with intensity of 1.14J/cm^2 to weld the Ag NWs, attaching the network onto the polymer substrate within microseconds to milliseconds. The film shows a resistance of 19Ω/sq with transmittance at 83%. However, the heating temperature required by the annealing process or welding is not suitable for normal polymeric substrates or matrices used in flexible electronic devices.

The strategy of applying mechanical pressure on the AgNWs networks at room temperature to compress the junctions and strengthen the binding of wires to the organic substrate is one solution. Via applying pressure of 25 Mpa for 5s to compress the junctions, sheet resistance of AgNWs network is successfully reduced to 8.6 Ω/sq while maintaining transparency at 80.0%, achieving the same properties of Ag NWs post-treated by thermal annealing (Tokuno et al., 2011). The method of high pressure loading is highly effective when preparing for a stretchable electrode, but appears not applicable for an incompressible substrate.

Mixing the AgNWs suspension with additives is also an effective and simple solution to achieve a highly conductive layer. Both inorganic additives, such as oxide nanoparticles, and organic additives, e.g. conductive polymers, generate hybrid structures with AgNWs to form transparent composite conductors. Graphene oxides has been reported to be used as a soldering agent to wrap the junctions of Ag NWs (Liang et al., 2014). The oxide-treated Ag NWs show a resistance 14 Ω/sq with transmittance reaching 88% at 550 nm and were successfully applied on a stretching lighting device; Zhu et al. in 2011 added TiO_2 sol-gel to tighten the contact across the AgNWs and applied PEDOT:PSS as a capping

layer to build up a stronger adhesion layer for AgNWs on the substrate. PEDOT:PSS can also be used alone as the additive(Vosgueritchian et al., 2012). The hybrid electrodes based on AgNWs can achieve a similar or better performance at room temperature processing condition while appearing more simple and effective than that made of the network of pure AgNWs (Gaynor et al., 2012). Also, traditional rigid transparent conductive materials, such as ZnO(Kim et al., 2013) and TiO_2(Song et al. 2015), have been deposited on a AgNWs network to act a encapsulated layer to protect the as-coated film as well as to modify the junctions of wires.

In our application, the LED die is composed of semiconductor ceramics, metal and non-metal materials, which are all rigid compounds, and built up in a delicate multiple component. For the method of thermal rolling, it usually requires heating the substrate 200 ℃ to fuse the junctions of Ag NWs and then apply certain pressure to weld the joints or junctions of the Ag NW network, which will easily crush the cuboid of the LED die and break the platelet structure. Because of the typical requirements of thermal rolling to improve the overall properties of AgNWs network, it can be hardly to either lower down the heating temperature below 180 ℃ and decreasing the loading pressure under 15 MPa, otherwise, the influence of the thermal roller cannot have major impact on the AgNWs. On the other hand, however, the epoxy, as a thermosetting polymer, cannot adjust to the thermal rolling for suffering from possibility of the irreversible deformation when being applied the high mechanical and thermal loading. Thus, the treatment of laser sintering is also excluded for this work. In conclusion, the process of coating the pristine AgNWs suspension on the platelet is seen to be a viable option for our requirements.

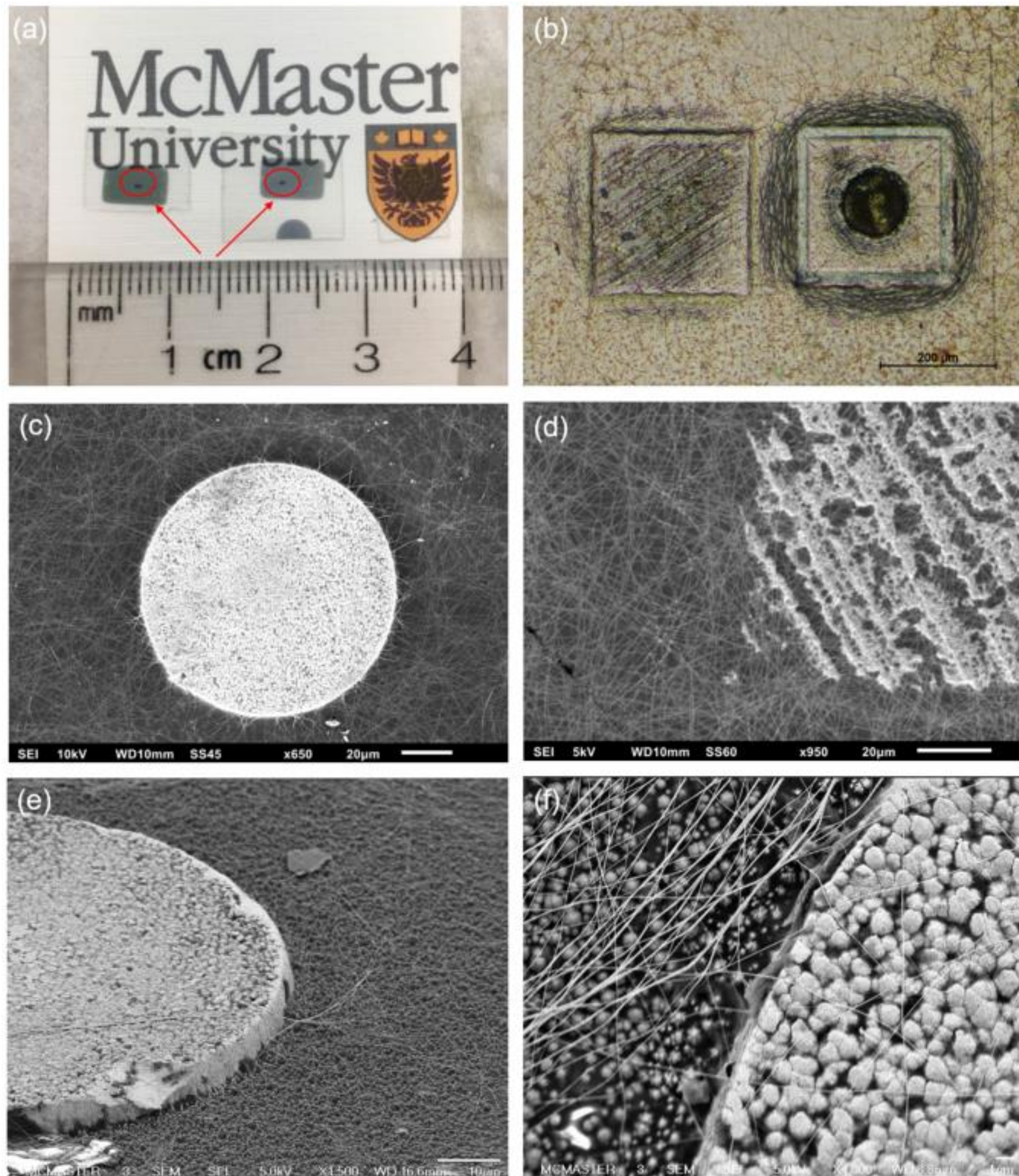

Figure 3.10 Optical microscope(OM) and SEM images of AgNWs networks on LED/epoxy platelet: (a) AgNWs-coated LED/epoxy with transferred Au within the dark pattern; OM of AgNWs as-coated platelet; (c) to (f) SEM images of contact area of LED chips coated with AgNWs

The AgNWs used in this work are commercially available and dispersed in ethanol solution and then coated on the LED/epoxy platelet via spray-coating, spinning coating and Meyer

Rod coating. It is found that the Meyer Rod coating was the easiest processing and most efficient method to form uniform networks of AgNWs. By adjusting the Meyer Rod coating parameters, such as the rod number and coating direction, AgNWs films can be formed without obvious alignment, as shown in figure 3.10 (a).

It needs to be noticed that while the dark spots are coated with the transferred Au layer, the remaining area of epoxy substrate coated with AgNWs films illustrates the high transparency of the conductive network. When the concentration of AgNWs suspension dipped in the substrate is too high, the dense AgNWs might agglomerate, thus leaving clusters of cloudy structure LED/epoxy platelet indicate and decreasing the transparency of as-coated film. In term of this, the suspension concentration of AgNWs plays an important role in influencing the optical transmittance of as-coated film by the density of nanowires on the surface, which indicates that the relationship between the concentration of the AgNWs suspension and transmittance of the AgNWs film needs to be investigated when the parameters of Meyer Rod coating are fixed.

The SEM images (c) and (d) shows the morphology of as-coated AgNWs film on the contact area of cathode and anode of the LED chips in the platelet, confirming that the AgNWs are randomly aligned on the surface contact area of LED dies without obvious alignment and the dense network is able to constitute a conductive layer. The details of subplot (e) and (f) illustrate capability of the wires to bridge the electronic network over height difference on the protruding part of the LED cathode area. Besides, the materials constituting contact pads of LEDs is Au, whose roughness is approximately 1 μm in the because of the variation of condensed Au particles. Nevertheless, thank for the flexibility of the silver

nanowires, they are able of be well accommodated and laid in the approximately 1-μm wide gaps on the surface of cathode and anode area, while it appears to be challenging for the ITO film to be deposited on these areas due to the uneven topography.

The other important property, optical transmittance of the nanowire layer, is directly determined by the density of as-coated wires on the substrate. Both the optical and SEM images clearly show that the density of the wires deposited on the platelet is controllable by varying the concentration of the pristine suspension of AgNWs employed during deposition. The wires coated on the platelet obviously become increasingly dense as the concentration of nanowire suspension is higher. The density of AgNWs coated on the platelet was calculated based on the optical images magnified by two hundred times. To obtain an average number of wires located in the 100*100 μm^2 grid, four grids at the corners and one grid in the center were counted from optical images to obtain a set of concentrations of the AgNWs suspension from 1 mg/ml to 5 mg/ml.

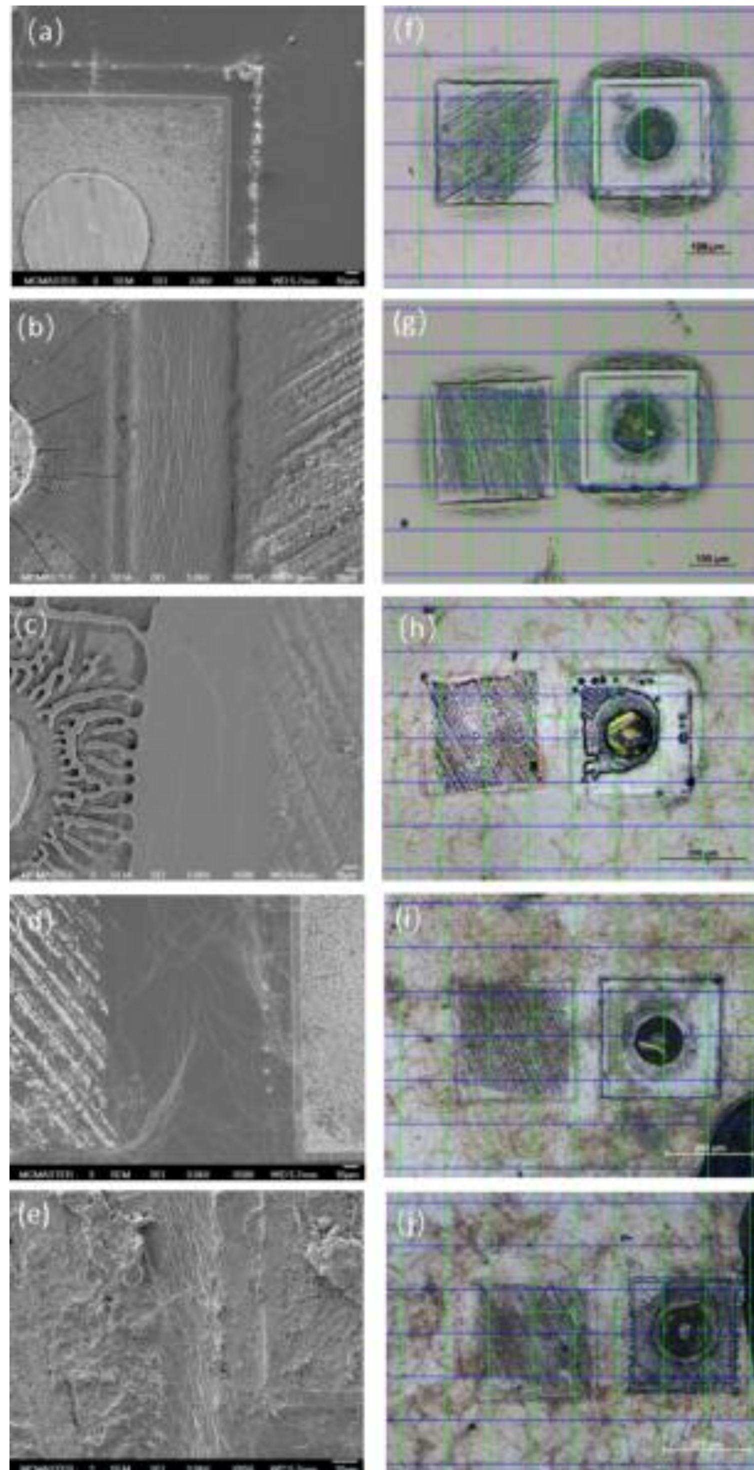

Figure 3.11 AgNWs network coated on LED/epoxy platelet in variation of gradient concentration of AgNWs suspension; (a) to (e): SEM images of AgNWs coated via concentration from 1 ml/mg to 5 mg/ ml; (f) to (j) ground optical images of AgNWs 1 ml/mg to 5 mg/ml

As seen in figure 3.11, the histogram demonstrates that the number of silver nanowires in the area of 100*100 μm^2 firmly corresponds to the dipping concentration of the suspension. The density of nanowires on the platelet is approximately 11 wires per 100*100 μm^2 when the suspension concentration of AgNWs in ethanol is 1 mg/ml, and the densities of the as-coated AgNWs go on a linear rise to 32 wires per 100*100 μm^2 at a concentration of 3 mg/ml and eventually arrive at 54 wires per 100*100 μm^2 at a concentration of 5 mg/ml.

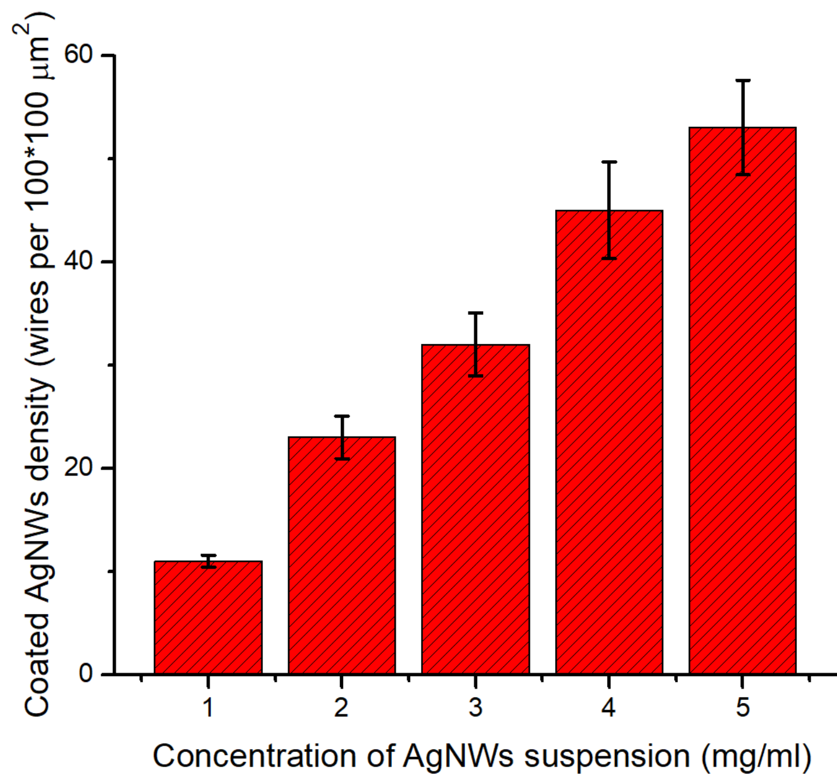

Figure 3.12 Density of as-coated AgNWs network on the platelet in variation of concentration of dipping suspension

Understandable, the density of the as-coated AgNWs network is one of the determining characteristics of the optical and electric properties. The results of transmittance spectra, seen in figure 3.12, illustrate the obvious fact that the wire density plays an essential role

in the electric conductivity of the metallic network. The increase of AgNWs density results in a moderate decreasing transparency but a drastic optimization in electric conductivity. The transmittance of platelet with 1 mg/ml AgNWs is apparently the most transparent sample, with transmittance of above 85% in the most of visible part of the spectrum (450 nm to 700 nm), while the platelet coated by 4 mg/ml and 5 mg/ml suspension is the samples showing a transmittance below 80%. The rest of the as-coated platelets show transmittance between 75% and 86%. The transparency of the as-coated AgNW film is acceptable though the transmittance of coated films is lightly lower than the AgNW film processed by pre- or post-treatment, such as thermal-annealing or laser sintering reported by the literature. However, it does not cause considerable luminance loss when the film shows a transmittance higher than 80%. Maintaining a balance between the optical and electric properties is the key for the conductive layer to achieve high performance and it is demonstrated that the critical value regarding the optical-electric balance could be achievable by the sample deposited from a suspension of AgNWs of 3 mg/ml.

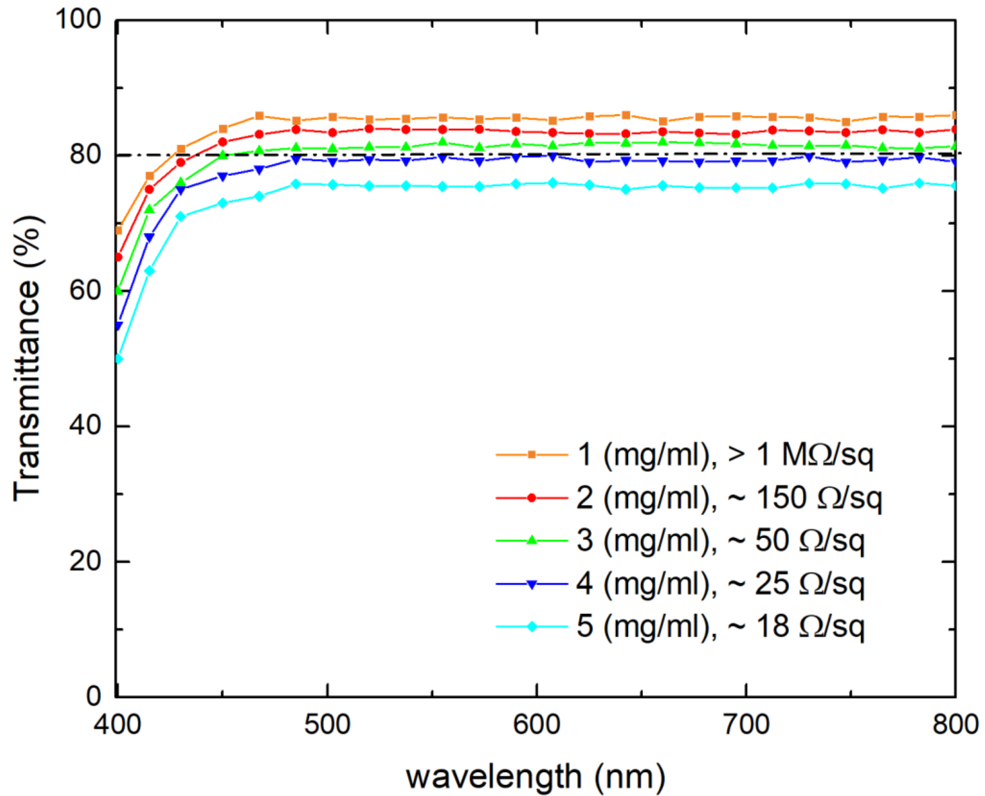

Figure 3.13 Transmittance spectra of the platelet coated by gradient concentration of AgNWs suspension and the corresponding sheet resistance of as-coated films

Sheet resistance is also measured for the as-coated AgNWs films on the platelet and it decreases significantly as the dipping concentration increases from 1mg/ml to 5 mg/ml. The sheet resistance of 50 Ω/sq using 3 mg/ml coated AgNW film becomes competitive to the that of optimal ITO films, which is observed to be 79 Ω/sq, deposited at a pressure of 10 mTorr at room temperature. The AgNW films demonstrated a lower sheet resistance of 25 Ω/sq and 18 Ω/sq, respectively by dropping thicker suspensions of 4 mg/ml and 5mg/ml at the cost of sacrificing light transmittance.

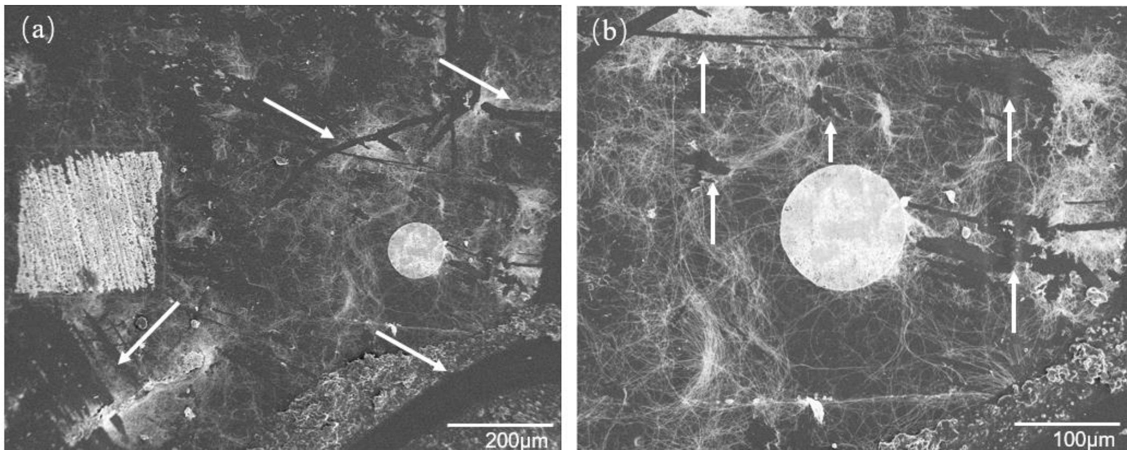

Figure 3.14 SEM images of Peeled-off AgNWs on the platelet

Though both the electrical and optical property of AgNWs network have proved it as a qualified candidate to compete with optimized room-temperature deposited ITO film, however, the adhesion of AgNWs to the substrate remains a problem preventing the metallic network from practical application due to lack of an adhesion-reinforced process. As shown in the SEM images of figure 3.14 of the tested AgNWs films, the white arrows point out peeled-off AgNWs caused by a slight touch or scratch. The distributed exposed areas of substrate indicate that the as-coated AgNWs are so vulnerable that a gentle scratch might interrupt the conductive layer by destroying the integrity of the network morphology with no additional modification, such as thermal pressing or sintering. Thus, the binding to the AgNWs network is too weak and the conductive layer coated on the platelet is not reliable with mere physical contact.

3.3 Combined Electrode of ITO/AgNWs and Inner Structure of Whole Assembly

Although the investigation of the process of room-temperature deposited ITO and Meter Rod coated AgNWs has demonstrated that the both of the ITO and AgNWs can be a good candidate material as transparent electrode, however, the test results also have suggested that a single material as the conductive layer cannot fully satisfy the requirement of transparent electrode regarding the application in flexible dual-LED assembly due to the limitations of each candidate. For ITO ceramic film, the mechanical properties and fragile nature make it hard to keep a stable performance under the frequently varied compressive and tensile strain condition. For as-coated AgNWs layers, the integrity of the metallic network can be barely maintained due to the poor adhesion on the substrate without additional treatment. The luminous test of connecting the dual-LEDs assembly in the Sawyer-Tower circuit (discussed in next session in details) also prove the weakness of utilizing a single material as transparent electrode, whereas the dual-LEDs is able to be powered on by the application of the bare ITO, though the reliability remains to be problem and sanctifying the flexibility \. Hence, the idea of utilizing a combined electrode of ITO/AgNWs is proposed because the merits of ITO and AgNWs can complement each other's limitations when carefully processed.

The ITO films are deposited on the AgNWs network, that are Meyer rod coated by dipping 3 mg/ml suspension, in 1 min, 5 mins and 10 mins to compare the influence of ITO deposition time on the optical and electric properties as well as to prove the improvement in the reliability.

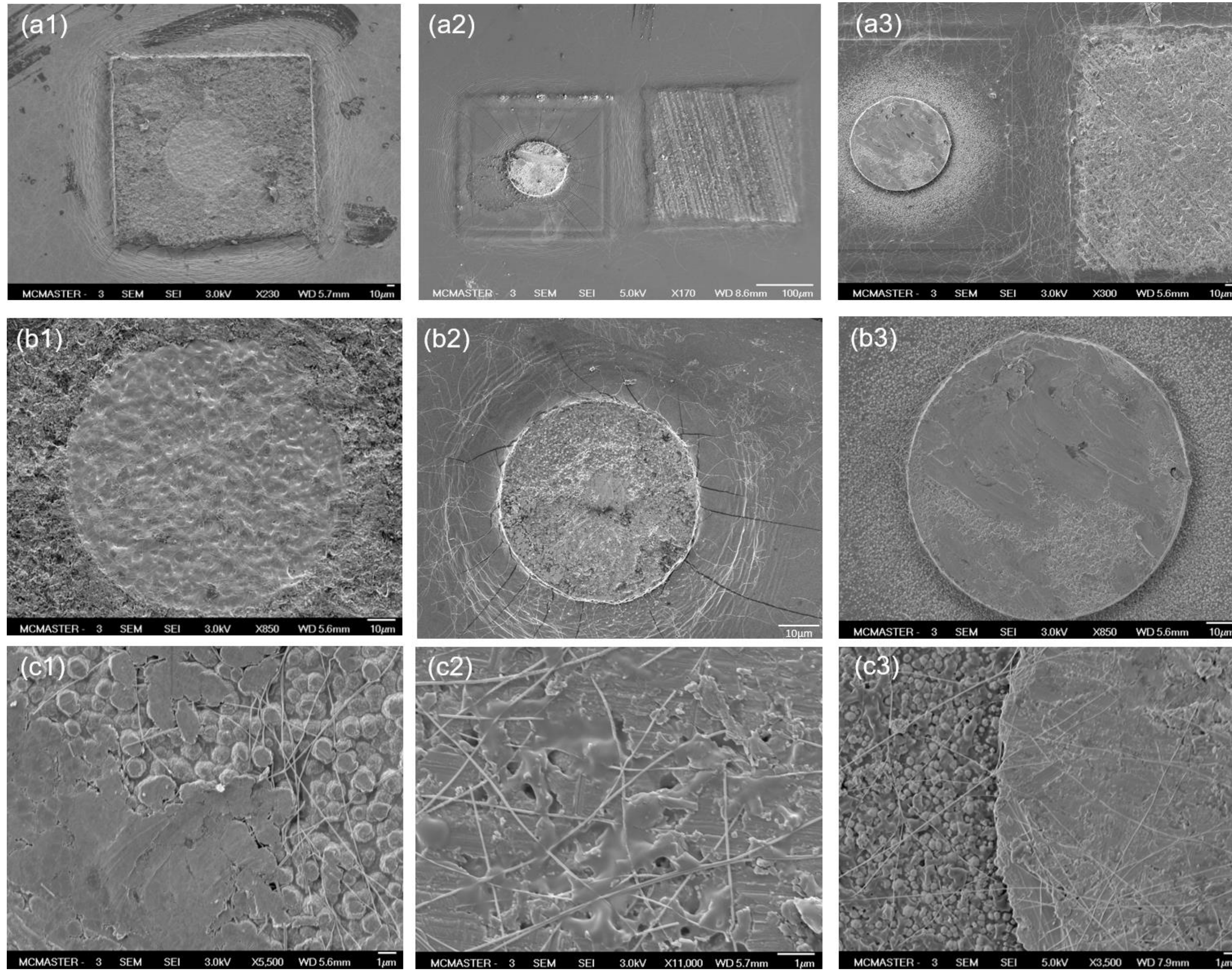

Figure 3.15 SEM images of ITO/AgNWs eletrode in details: (a1), (b1), (c1) shows the AgNWs film with ITO sputtering for 10 mins; (a2), (b2), (c2) for 5 mins; (a3), (b3),(c3) for 1 mins

The measurement results show that both resistance and transmittance of combined electrode are mainly decided by the ITO film when AgNWs is coated with ITO in 5 mins or 10 mins, while these properties of the combined electrode are more closed to that of pure AgNWs when deposition time is 1 min. These results are reasonable and can be explained by the structure and surface morphology of the combined electrode with different ITO coating time. As seen in the figure 3.15, the ITO coating on AgNWs for 5 min and 10 mins almost completely cover the AgNWs and bury the network underneath the ceramic layer, so that the whole structure, especially the surface structure, is mainly composed by the ITO, so that the resistance and transmittance plays the main role in deciding the overall properties. Besides, it is reported that the thin ITO film has a minor influence on the transmittance on substrate (Shigesato et al.,2010) and the experimental results prove that the transmittance of either 1min, 5 mins or 10 mins deposition of ITO layers remains above 90%, which means the ITO layers have a minor influence on the transmittance of the combined electrode.

After improving the wettability of epoxy on PDMS for the embedding processing, optimizing the coating methods and parameters of the transparent conductive layers of combined ITO/AgNWs, as well as fabricating capacitive couplings of dielectric layers via physically scattering the $BaTiO_3$ particles in epoxy matrix, the assembly of final AC-driven polymer-embedded dual LEDs is eventually accomplished. The cross-section images of the final assembly illustrate the layer-by-layer structure, taken by both optical microscope (NIKON LV100) and SEM, JEOL 7000.

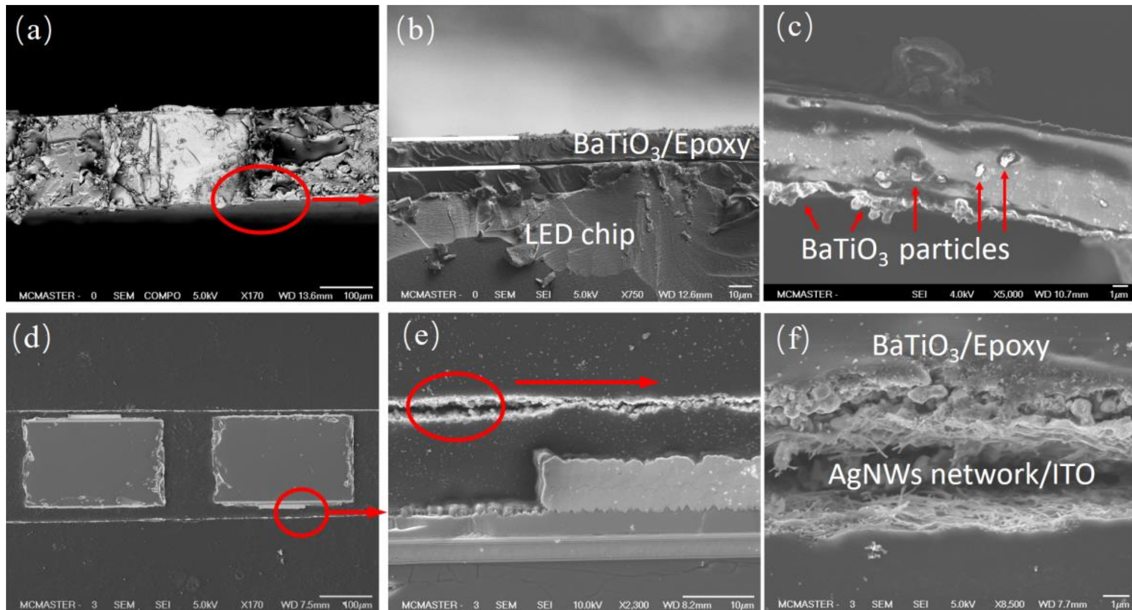

Figure 3.16 SEM images of the cross sections of the whole assembly: (a) to (b) emphasis on inspections of the $BaTiO_3$/Epoxy structure, showing the 2 μm $BaTiO_3$ embedded in the epoxy film, outside the LED chips; (d) to (f) illustrating the final assembly of dual-LEDs, which explicitly showing the topographic structure of combine electrode of AgNWs network coated with thin film of ITO fabricated on the outside of dielectric layer

As seen in figure 3.16, the internal structure of the whole assembly is clearly illustrated by the SEM cross section images and the total thickness is approximately 155 μm. The dielectric layers of $BaTiO_3$/epoxy are symmetrically fabricated on the both side of core lighting layer, which is epoxy-embedded two opposite set LED chips. There are four layers of transparent combined film electrode of ITO/AgNWs, coated in between the central layer and dielectric layer, as well as outside of the dielectric layers as final electrode. In the subplot (b) and (c), it tells that the thickness of a single dielectric layer is less than 10 μm, approximately 8 μm and also, the 2 μm $BaTiO_3$ particles are averagely dispersed among the epoxy matrix. In the subfigure (f), the AgNWs attached on the outside of the dielectric

layers forms a dense network and play an essential role in the transparent conductive layer, along with the ITO layer.

The real final dual-LEDs assembly is shown in the figure 3.7(a). the overall size of the effective lighting unit is small than 1 mm, lightly bigger than the size of 600 μm*300 μm in principle. The dark green area is the ultra-Au deposited area. Though the laye-by-layer assembly is opaque, however, seen in the figure 3.17 (b), the light is capable of being emitting out easily from the wirebonding-free package with the AC source applied.

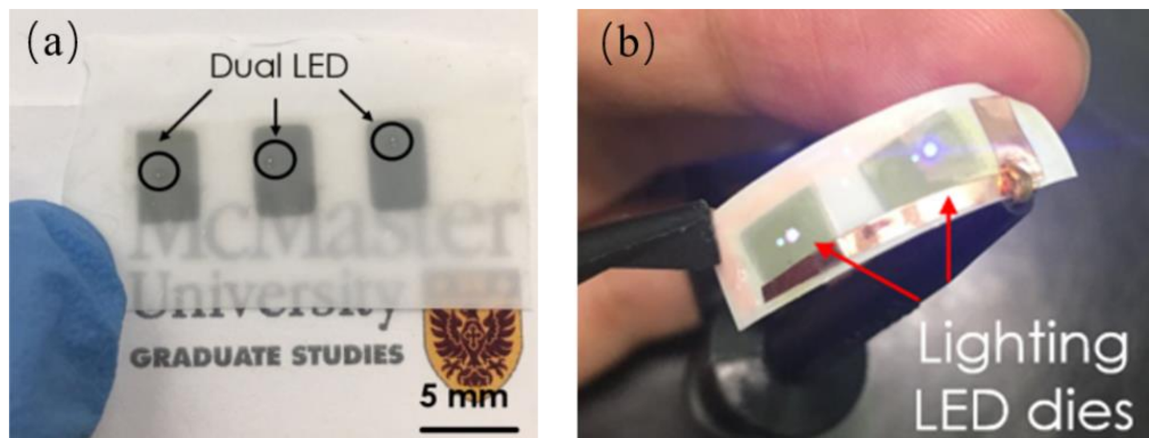

Figure 3.17 Final assembly of dual-LEDs fabricated with dielectric layers: (a) the real assembly measured using Sawyer-Tower circuit; (b) lighting dual-LEDs driven by AC source in the form of sinusoidal voltage waveform

Chapter 4 Luminous Performance of the Dual-LED Assembly with Dielectric Layers

In this chapter, the luminous performance of the polymer-embedded AC-driven LED assembly will be evaluated. The discussion will focus on the relationship between luminance, luminous efficiency and transferred charge into the dual-LED under alternating current drive conditions. Peak-peak sinusoidal voltage ranging from 0 to 20 V, in the frequency range of from 10 kHz to 200 kHz will be employed. The luminous performance of the whole assembly is evaluated with the Sawyer-Tower circuit, which is very useful to characterize the energy and power delivery into the dual-LED assemble through dielectric layers.

4.1 Luminance and Transferred Charge of the Assembly

The intensity of light (luminance) from the assembly is measured by the luminance meter LS-100, (Minolta) and the transferred charge responding to the input voltage into the lighting unit of two LED chips is calculated based on the data recorded by the oscilloscope (Tektronix TDS210).

The shape of light from the final assembly is a light spot instead of a uniform lighting plane because of the limitation of the size of the lighting area of single LED chip which is only at level of micro-size, smaller than 280 μm. However, the diameter of measuring zone of the photometer is 1.5 mm, much bigger than the size of the dual-LEDs (280 μm * 560 μm).

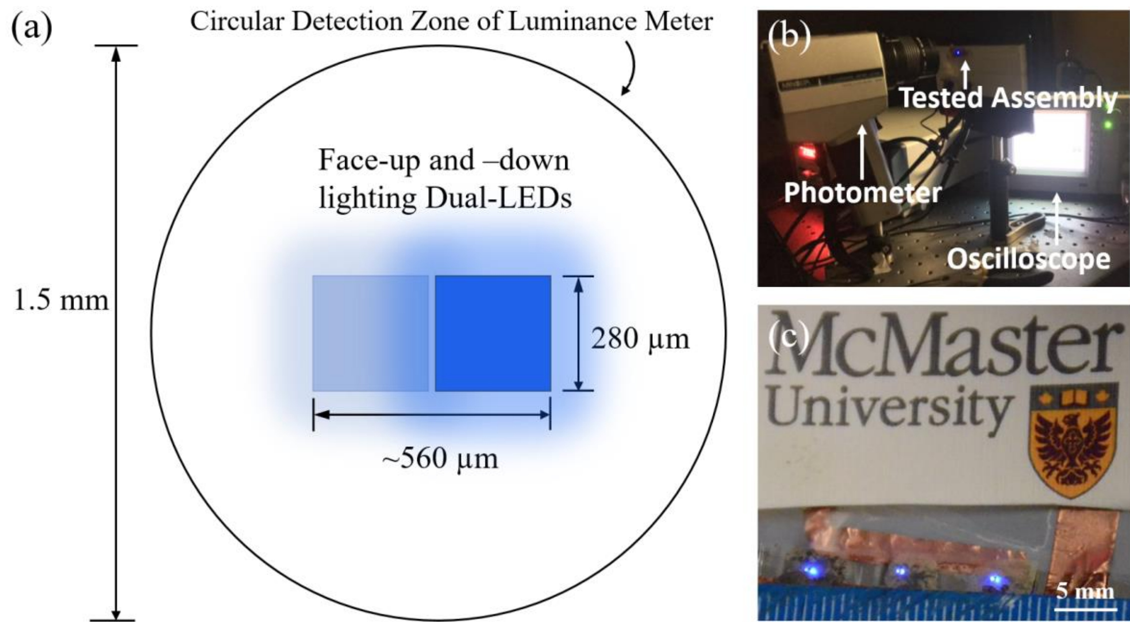

Figure 4.1 Lighting assembly driven by AC source: (a) schematic of dual-LEDs inside the circular detection zone 1.5mm in size. (b) real lighting assembly with dielectric layers in dark environment; (c) three pairs of dual-LEDs in parallel with combined electrode of ITO/AgNWs taken in the measurement of luminance

Admittedly, as the number of the lighting units increases, the accumulative lighting spots within certain area can become a lighting plane in principle. However, due to the limited efficiency of the processing yield for the overall assembly in lab, only a small (<10) number of the fabrication of the final lighting unit of dual-LEDs have been completed with dielectric layers and final electrode layer were obtained. Specifically, as the schematic of single lighting dual-LEDs in the detection zone area of the photometer shown in figure 4.1(a), the tiny lighting units are far from fulfilling the detection area due to the large size difference between the object and the detection zone of the photometer. Besides, since the light emitting from the side of cathode is much brighter than that from the side of anode, there is obvious discrepancy of brightness due to the difference orientation between the two LED

chips, in which one chip is set upward, and the other set downward. Because of the narrow beam of the light generated from LED chips, a common term to describe the luminance of LED sources is the luminous intensity, with a unit of Candela, denoted by cd. On the other hand, another unit of luminance commonly used in literature is luminance in units of candela/m^2 which can be converted to foot-Lamberts (fL) as follows:

$$1\,fL = \frac{1}{\pi} \times \frac{cd}{m^2}\frac{1\,m^2}{1\,ft^2} = \frac{1}{\pi} \times \frac{1\,m^2}{0.0929\,m^2}\frac{cd}{}m^2 = 3.426cd/m^2 \tag{4.1}$$

These units of luminance are used for uniform light emitters such as flat panel displays and the photometer we employed is designed for this application, giving results in either unit of luminance. Both the fL and the cd/m^2 are used to describe the luminance of a light source. Either of two units used for the luminance (foot-Lamberts or Cd/m2) can be converted into the total amount of light (luminous flux in lumens) randomly emitted from one-square-foot lambertian source , which randomizes the reflective direction of the light. If the luminance units are in fL, then the conversion is as follows: 1 fL and a 1 ft^2 light emitting area converts to 1 lumen of luminous flux. If the luminance units are in cd/m^2 then the conversion is as follows: 1 cd/m^2 and a 1 m^2 light emitting area converts to π lumens of luminous flux.

The dielectric layer of $BaTiO_3$/epoxy, in this case, is semi-opaque and can be viewed as a Lambertian surface because it is able to randomize the light in all directions. Given the number of dual-LEDs units fabricated with $BaTiO_3$/epoxy dielectric layer is accumulative so that the lighting panel is large enough, emitting light that passes through this semi-transparent layer is randomized. Hence, light passing through the dielectric is almost solid-

angle-independent and no longer sensitive to the measuring angle, which therefore approximates a Lambertian source.

Either unit of fL or cd/m^2 can be used. The assumption of a lambertian source is valuable. Therefore, given there are an accumulative amount of lighting dual-LEDs, the original data of the luminance of a single assembly, measured by the photometer given by the cd/m^2, is transformed to the fL to evaluate the luminous performance based on assuming the same light flux from a single LED source keeps the same. The conversion is listed above as equation 4.1. Or cd/m^2 can be directly transformed to lumens if the size assuming a lambertian source is known.

Because the luminance data is all obtained through the photometer that measures the one single lighting assembly, it is necessary to do a compensation for the data analysis under an assumption that there are a number of the dual-LEDs assemblies lighting at the same time within a large enough area, bigger than the detection scope, to achieve the requirement of luminance measuring. More specifically, the diagram of luminance-voltage, transferred charge-voltage and luminance-transferred charge of the lighting LEDs are all plotted based on the conversions as following:

$$L_{flat} = L_{spot} \times \frac{area\ of\ measurement\ scope}{lighting\ area\ of\ Dual-LEDs}\ cd/m^2 \tag{4.2}$$

$$L_{flat} = L_{spot} \times \frac{lighting\ area\ of\ Dual-LEDs}{1\ ft^2}\ fL \tag{4.3}$$

To minimize the measurement error, the measuring angle between detection scope of the luminance meter and the perpendicular line of the lighting LED chip is keep as close to

zero degree as possible to catch the maximum luminance when measuring the luminance of a single lighting assembly. The figure 4.2 and figure 4.3 illustrate the luminous performance the assembly and indicate the relationship of luminance and transferred charge.

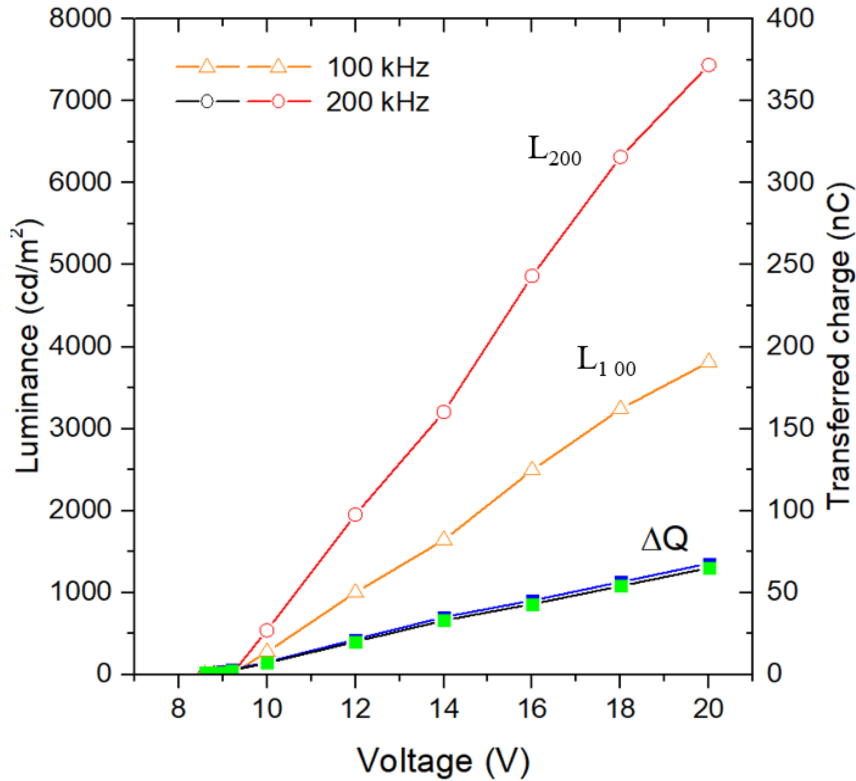

Figure 4.2 Calculated L-V and ΔQ-L characteristics of the dual-LEDs with dielectrics driven by sinusoidal waves of 100 kHz and 200 kHz based on the measuring data of a single lighting dual-LEDs

As seen in the figure 4.2, it clearly shows that the luminance increases proportionally with input sinusoidal waves as the peak-to-peak voltage from 8 V, slightly above the threshold voltage, to 20 V of pk-pk voltage of both 100 kHz and 200 kHz frequency sinusoidal waves. Not surprisingly, the transferred charge increases linearly as a function of the voltage above the threshold voltage, more explicitly illustrated in the figure 4.3. It clearly indicates that

the luminance of LEDs increases up to 3814 cd/m^2 and 7336 cd/m^2 under 100 kHz and 200 kHz sinusoidal wave drives respectively. The luminance of LEDs is proven to increase mostly linearly as a function of transferred charge as it rises from 10 V to 20 V (pk-pk voltage). The rapid rise of luminance is due to the increased transferred charge into the p-n junction of LED, boosting the output of light.

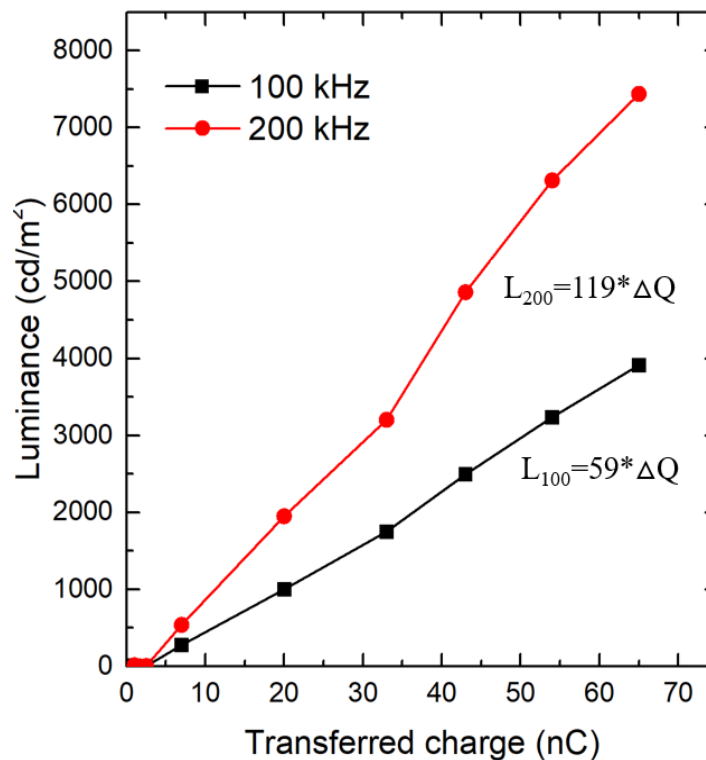

Figure 4.3 Curves of calculated Luminance versus transferred charge under sinusoidal waves of 100 kHz and 200 kHz

Specially, the dual-LEDs assembly needs to be driven by a high-frequency AC voltage because the dielectric constant of the $BaTiO_3$ is not high enough, However, given the dielectric property of the capacitive coupling is strong, with a decent magnitude of the AC voltage, the dual-LEDs LEDs is possible to be powered on by the 50 Hz AC source.

4.2 Analysis of Luminous Efficiency Based on Sawyer-Tower Circuit

The ideal lighting model for the dual-LED assembly can be viewed as the simple equivalent-circuit model of inner structure seen as the figure 4.4. This model was at first proposed(P.M Alt, 1984) to describe the phenomenological physics of thin film electroluminescent device and has proven its accuracy in the characterization of significant parameters in thin-film EL devices. In this model, the phosphor layer behaves both as a capacitor and a non-linearly changeable resistor when emitting light, and the insulating layers are treated as perfect capacitors and incorporated into a single effective capacitive layer, as illustrated by figure 4.4(b).

In this work, the same model can be applied to evaluate the performance of a dual-LED assembly due to the similar physical structure and working mechanism. As seen in the cross section of SEM image, seen in figure 4.4(a), there are symmetrically fabricated two insulating layers of $BaTiO_3$ at the outside of the luminous layer. As for the luminous layer, it is made of two reversed LED dies connected in parallel. When inputting the AC power, the lighting LED chip behaves as a non-linear changeable resistor and the off-lighting LED can be treated a capacitor. The exact same model can be directly applied to discuss the characteristics of the dual-LED. The incorporated capacitive coupling, C_0, is given by,

$$C_0 = \frac{C_{01}C_{02}}{C_{01}+C_{02}}, \tag{4.4}$$

where C_{01} and C_{02} are the capacitances of the two $BaTiO_3$/epoxy composite layers covering the outside of the LEDs' embedding layer respectively and should be equal in value in the case that they are prepared under the same conditions.

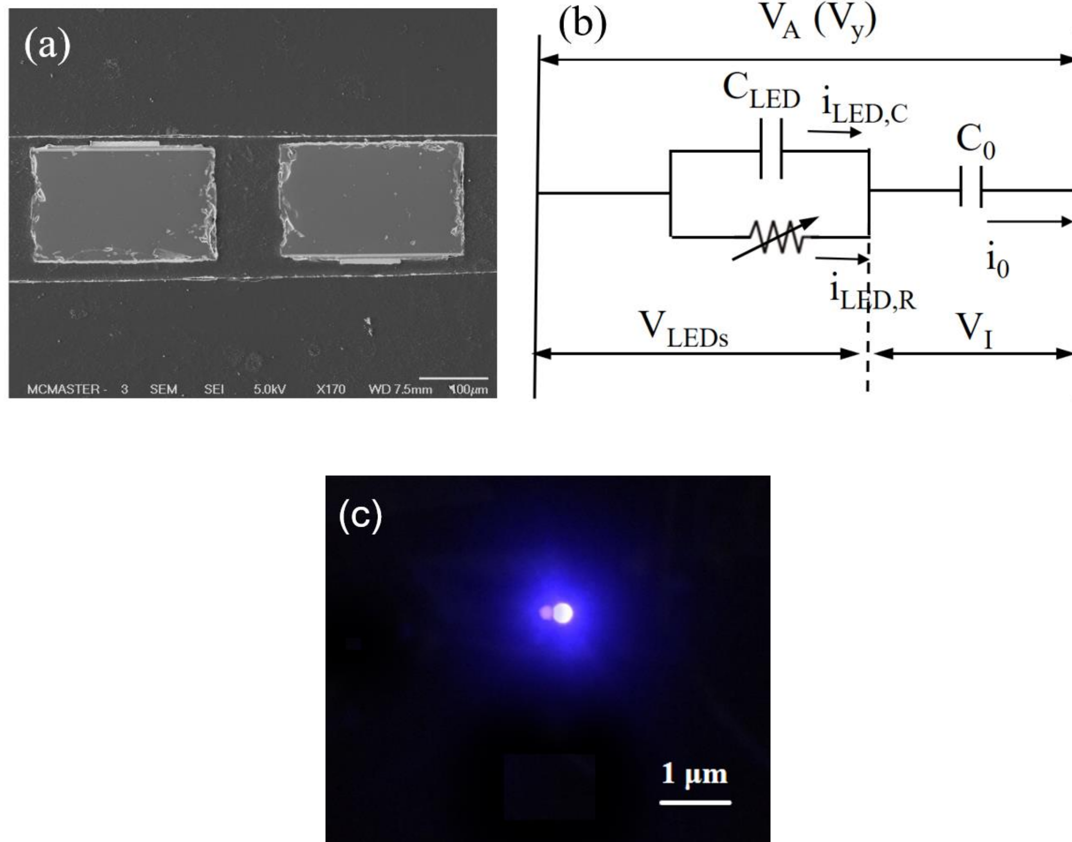

Figure 4.4 Cross section SEM image of the assembly structure: opposite set dual-LEDs embedded in epoxy base, being covered by the $BaTiO_3$/epoxy composite layers with multiple ITO/AgNWs combined electrode; schematic of analog of the working assembly driven by AC source: the lighting LED viewed as a changeable resistor while the other LED in parallel acting as a capacitor; (c) lighting dual-LEDs with dielectrics powered by AC source

When the input voltage is below the threshold voltage, both LED chips act as a capacitor, with the capacitance of C_{LED}. The LED chip behaves as a changeable resistor when the input voltage is above the threshold voltage. The two individual LED chips in parallel are supposed to emit light separately in the half cycle corresponding to the alternating input current. Specifically, one LED lights up in the first half-cycle of the input voltage while the other LED is off. Whereas, the LED working in the first cycle will become dark, the

other LED chip starts to give out light in the subsequent half-cycle of the AC source. The luminance (cd/m2) of the light-emitting layer is proportionally dependent on the power consumed by the resistive branch because the resistive part is the LED chip at work. Besides, the luminous efficiency, η, is also decided by the input voltage and the corresponsive transferred charge into LEDs, in unit of Lumens per watt (lm/W).

The symbols depicted in the schematic of the model are given as follows,

$$\begin{cases} V_A = V_{LEDs} + V_0 \\ V_{LEDs} = \dfrac{C_0}{C_0 + C_{LEDs}} V_A \\ V_0 = \dfrac{C_{LEDs}}{C_0 + C_{LEDs}} V_A \end{cases}, \tag{4.5}$$

where the V_A is the overall voltage applied on the whole assembly, V_{LEDs} is the voltage applied on the in the part of dual-LEDs and V_0 is the voltage on the side of incorporated dielectric layers, as shown in figure 4.4 (b).

The total current passing the whole assembly is responsive to the changing rate/frequency of the AC power, given by,

$$i = C_0 \frac{dV}{dt}, \tag{4.6}$$

where represent the current converted through the assembly, C_0 is the capacitance of the incorporated dielectric layer and the dV/dt is the changing rate/frequency of the alternate current. When the capacitance of dielectric layers is a constant. The current though the branch of the changeable effective resistor of the working LED plays an essential role to

absorb energy for the luminous component, while the other LED of the device behaves as a capacitive component.

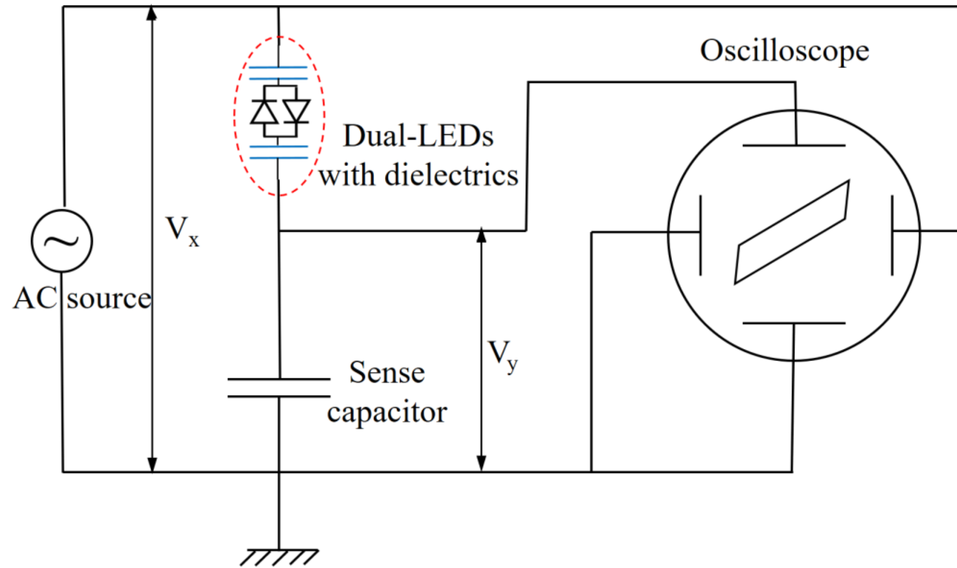

Figure 4.5 Schematic of Sawyer-Tower Test circuit

The performance of the dual-LED assembly is characterized by the method based on the Sayer-Tower circuit, which is used to measure the transferred charge, Q, and the input power, P_{in}, versus the applied AC voltage (Yoshimasa, 1995). The measurement method of Sawyer-Tower circuit was originally built up for the analysis for hysteresis loops of ferroelectric materials and is very useful in investigating the polarization phenomenon. Depicted as figure 4.5, the Sawyer-Tower circuit is built up by the load under test and another sense capacitor. Being connected in series, the capacitance of sense capacitor is expected to be much bigger than that of the load under test so that the source voltage will be mostly applied on the sense capacitor.

After connecting the assembly with a sense capacitor in series, the shape of the pattern shown in the oscilloscope appears as a parallelogram with the input voltage as the x-axis signal and voltage of sensor capacitor as the y-axis signal in the case that the capacitance of sense capacitor is much bigger than the capacitance of the assembly. The capacitance of assembly is given by,

$$C_A = \frac{C_0 C_{LEDs}}{C_0 + C_{LEDs}} \quad (4.7)$$

By changing the y-axis of the voltage applied on the sense capacitor to the transferred charge, Q, into dual-LED assembly, the shape of the diagram of Q-V remains a parallelogram, which is illustrated in figure 4.6, where charge density, Q, is equal to Cs*V, and V represents the voltage applied on the dual-LED assembly. In the diagram of figure 4.6, the slope of other two sides in the high voltage area, in quadrants I and III, is determined by the capacitance of two dielectric layers in series, C_0, while the slope of the sides of the parallelogram across the y-axis is determined by C_A, the overall capacitance of the dual-LED assembly, which is the series capacitance of three capacitive elements, namely two dielectric layers as well as the capacitance of the parallel-connected dual-LEDs.

Meanwhile, the value of threshold voltage can be read at the intersection of the straight lines at the high voltage area and the threshold transfer charge is indicated by the intersection of lines, $Q = C_A V$, at the x-axis. Most importantly, the energy delivered into the dual-LEDs can be calculated based on the encompassed area of parallelograms. For any specific

parallelogram representing the Q-V diagram of a certain input voltage, the input energy, E_{input} , and input power, P_{input}, are given by,

$$E_{input} = 2 \times V_{LEDs,th} \times \Delta Q = 4 \times V_{th} \times Q' \tag{4.8}$$

$$P_{input} = f \times E_{input} = 2 \times f \times V_{LEDs,th} \times \Delta Q = 4 \times f \times V_{th} \times Q' \tag{4.9}$$

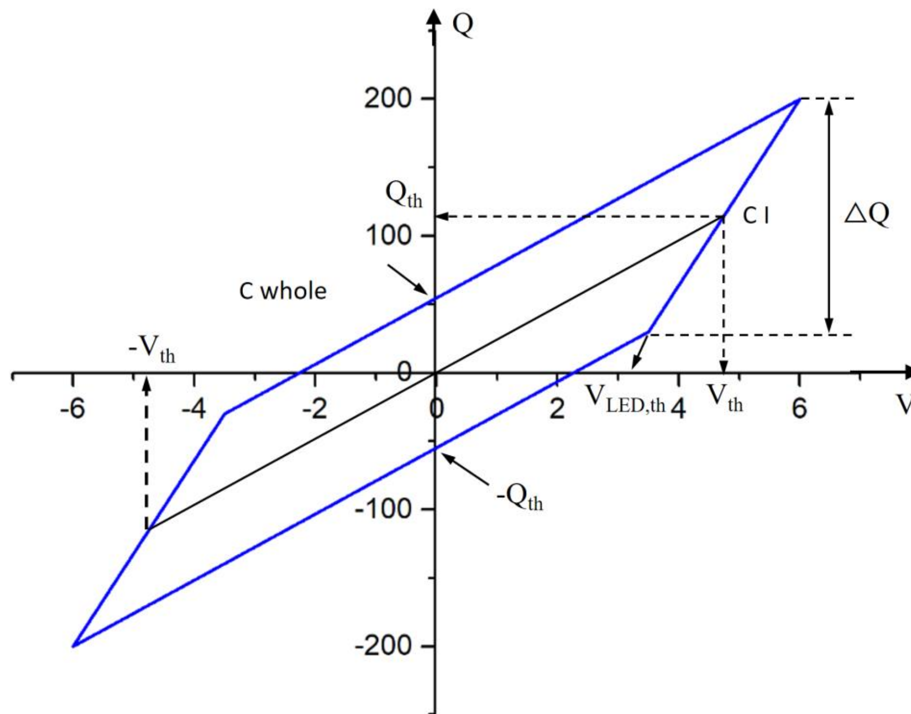

Figure 4.6 Typical Q-V characteristic curve based on the measurement of oscilloscope

As seen in shown in figure 4.7, luminance efficiency, of the whole dual-LED assembly, η, goes through a sharp increase from 9 V to 10 V and obviously shows its maximum efficiency at the threshold voltage, 33 lm/W, which is a very decent and reasonable luminous efficiency for blue-light LED when compared with luminous efficiency of other blue-LED assemblies, ranging from 25 lm/W to 39 lm/W (Klipstein et al., 2008). Then, luminous

efficiency stays at an approximately constant level and decreases slowly until the voltage reaches 20 V, although the luminance keeps rising as the energy delivered into the assembly continuously increases.

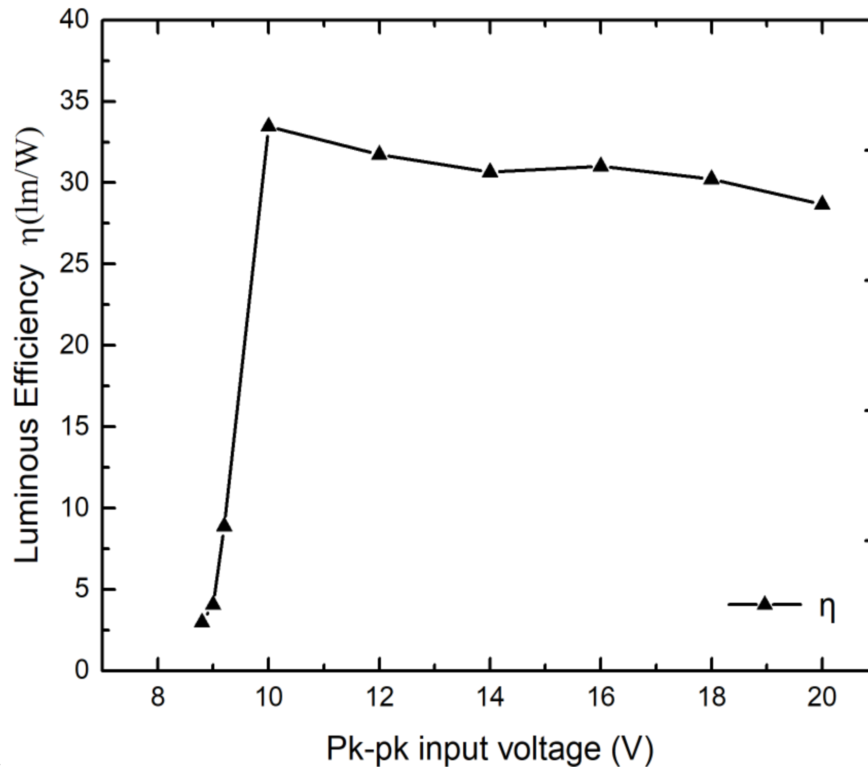

Figure 4.7 Luminous efficiency v.s. input voltage of the dual-LED with dielectrics

When incorporating the series of Q-V loops determined by gradient input pk-pk voltages, as seen in the figure 4.6 of Q-V diagram, the shape of the loops of Q-V appear as a list of independent parallelograms, whose centers are all located at the origin, when the input voltage is above the threshold voltage. Below the threshold voltage, which is approximately at pk-pk voltage of 10 V, the whole assembly could be viewed as a series of capacitors. According to the Sawyer-Tower circuit, the whole the circuit works as a simple

capacitive voltage divider, which means the transferred charge through the assembly shows a linear increase as the voltage increases, and this is therefore shown as a straight dash-point line in the graph, through the origin in the coordinates of the Q-V diagram. The slope of this straight line is given by the capacitance of the sensor capacitance, C_{sensor}, and all sides of parallelograms are determined by the C_{sense}, which are approximately parallel in figure 4.8. Meanwhile, other sides of the series of parallelograms across the ordinate are given by the overall capacitance of the whole assembly, C_A.

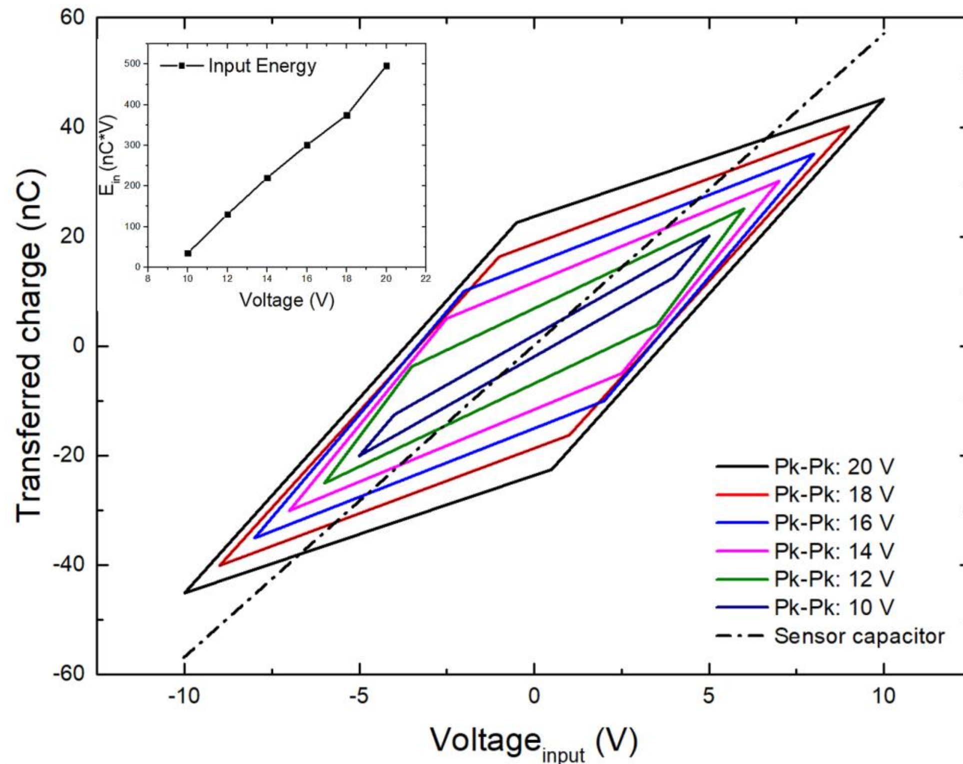

Figure 4.8 Loops of parallelogram of Q-V depicted in variation of input pk-pk voltage in form of sinusoidal wave of 200 kHz

With the increase of peak-peak input voltage gradually rising from 10 V to 20 V, these parallelograms spread out eccentrically. Given the area of the parallelograms responding

to the variation of pk-pk input voltage, encompassed areas reflect consumption of energies from 32 to 498 nJ for variable voltages from 10 V to 20 V. And the corresponding input power is multiplying input power with frequency, 200 kHz, which ranges from (62 to 996)*10^{-4} W. It is not hard to understand that when input voltage exceeds the threshold voltage, a higher input voltage results in a high power delivered into dual-LED and consequently improving the luminance of the whole assembly.

Chapter 5 Conclusion

Based on a novel package method of LED lighting unit, a flexible soldering-free polymer-embedding dual-LEDs assembly has been developed and proven to be able to be driven by alternating current source with the fabrication of two layers of $BaTiO_3$ reinforce epoxy as the capacitive coupling. Embedded in an epoxy matrix, the dual-LEDs assembly is capable of emitting lighting continuously due to its peculiar structure that two LED chips are set oppositely in parallel and light up separately and alternately during the half cycle of AC source periodicity. Multiple layers of ITO/AgNWs combined conductive layer are fabricated symmetrically in between the LED core layer and dielectric layers and at the outside of dielectric layer to realize the soldering- and wirebonding-free characteristics. Thanks to the polymer-based layer-by-layer structure, the rollable dual-LEDs assembly performs a good flexibility with the bending radius as low as 6 mm, maintaining a repeatable and stable luminous performance.

The LED-embedded epoxy is prepared resorting to axial capillary force. The relationship of spinning time-spinning velocity and thickness of later has been investigated to prepare a smooth and uniform PMDS buffering layer, and the optimized PMDS coating layer with thickness of 8 μ is spin-caoting at 3000 rpm for 30 seconds. Besides, the surface of PDMS layer is coated by a thin layer of Au film (approximately 20 to 30 nm) to improve the wettability between PMDS layer and liquid epoxy. The results of contact angle measurement show that the contact angle of liquid epoxy on PDMS film drops from 57° to 17° after the PDMS is coated with Au thin layer for 2 minutes. The big improvement of surface

wettability between liquid epoxy and PDMS later benefits to eliminate the voids/bubbles in the cured epoxy matrix, therefore modify structural integrity of the LEDs/epoxy platelet. ITO ceramic thin film has been firstly deposited on the dual-LEDs/epoxy layer at room temperature as the transparent electrode layer and the influence factors of sputtering time, sputtering power and working pressure on the sputtering rate of ITO on epoxy layer have been investigated. The optimal resistance of ITO with thickness ranging from 40 nm to 210nm on epoxy can be reduced to 50 Ω/sq when being deposited under vacuum pressure of 10 mTorr and sputtering power of 45W at a room-temperature for less than 10 minutes. However, the nature of brittleness prevents the ITO ceramic film being applied in this flexible solid light emitting assembly. To better understand the possible failure mechanism of ITO on the epoxy substrate, the SEM images clearly illustrates that the mismatched of CTE between ITO results in the initiation and coalescence of microcracks across the ITO film on the epoxy due to the temperature rising bot during the vacuum sputtering process and in the electronic test. Besides, the difference in morphology of the dual-LEDs/epoxy platelet also increases the difficulty for ITO to be deposited uniformly on the substrate.

To modify the reliability of ITO on the LEDs/epoxy platelet and overcome its limitation when applied on the flexible substrate, the networks of AgNWs has been introduced to combine with ITO, forming a novel composite transparent electrode. The network of AgNWs prepared by the Meyer Rod coating demonstrates itself as an excellent transparent material as ITO, for showing a sheet resistance < 50 Ω/sq with optical transmittance > 80 % in visible region. Besides, it is found that the key properties of conductivity and transmittance of AgNWs network are highly dependent on the concentration of the AgNWs

suspension and the internal joints of the networks. Results of dipping gradient concentration of AgNWs suspension on the platelet indicates that the density of AgNWs on substrate, after the solution evaporates, is linearly increasing as the dipping centration of AgNWs suspension becomes higher. Though the network of pure AgNWs is demonstrated to a good electric and optical properties, as well as good flexibility and easy-processing feature, yet the adhesion between the network and the LEDs/epoxy remains to be a problem for the reliability for the assembly. Regarding the poor adhesion of AgNWs on the substrate, the sputtered ITO on the network of AgNWs helps improve the binding condition through the deposition on the network. The application of coating layer on the AgNWs network not only maintains the sheet resistance and optical transmittance of the combined electrode to be very closed to those of pure AgNWs network, but also, largely improves the reliability of the combined electrode because the deposition of the ITO ceramic contributes to attach the AgNWs onto the bondpad of LEDs and the surface of LED/epoxy platelet. One the other hands, the uniform network of AgNWs compensates for the limitation of ITO ceramics regarding its brittleness and fragility, because the wires of nano-silver mend and connect the gaps of microcracks across the ITO film.

Last but not least, the luminous performance of the final assembly with capacitive couplings made of $BaTiO_3$/epoxy composite has been evaluated based on the Sawyer-Tower circuit. The threshold voltage of the wirebonding-free dual-LEDs is approximately at 9 V, and the maximum luminance of assembly achieves 7500 cd/m^2 when pk-pk AC voltage is set at 20 V, 200 kHz, within a given area in principle and it maintains a decent luminous efficiency above 30 lm/W when input pk-pk voltage is set from 10 V to 20V. The dual-

LEDs receive energy through the capacitive coupling of two layer of $BaTiO_3$ reinforced epoxy layer, which are capable of converting the high-frequency of alternating current into direct current, so as to enable the dual-LEDs to be driven by AC voltage.

Conclusively, an innovative packaging method of LED chips has been developed to realize the wirebonding-free AC driven characteristic by a polymer embedded structure, and is also demonstrated to be very competitive in terms of the large flexibility, small size and a decent luminous efficiency. This packaging method is promising in the future low-cost printable electronics as well as acting as the basic lighting unit for the next generation rollable display and high-definition large scale display panel.

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