GaAsP NANOWIRE-ON-SILICON TANDEM PHOTOVOLTAIC CELLS

FABRICATION AND CHARACTERIZATION OF GaAsP NANOWIRE-ON-SILICON TANDEM PHOTOVOLTAIC CELLS

by BRENDAN WOOD, B.Eng.Mgt.

A Thesis Submitted to the School of Graduate Studies
in Partial Fulfilment of the Requirements for the Degree of
Master of Applied Science

Master of Applied Science
Engineering Physics

McMaster University
Hamilton, Ontario, Canada
August 2017

TITLE: Fabrication and Characterization of GaAsP Nanowire-on-Silicon Tandem Photovoltaic Cells

AUTHOR: Brendan Wood, B.Eng.Mgt Engineering Physics (McMaster University)

SUPERVISOR: Dr. R. R. LaPierre

NUMBER OF PAGES: xvii, 120

Abstract

One-dimensional vertical nanostructures, nanowire arrays, are investigated for applications in photovoltaics. Specifically, III-V core-shell p-i-n nanowire arrays are grown by molecular beam epitaxy on silicon substrates, using the self-assisted vapour-liquid-solid growth method. $GaAs_{1-x}P_x$ nanowires are grown with an optimized composition to maximize the potential efficiency of a GaAsP nanowire-on-silicon tandem solar cell under AM1.5G illumination. Photovoltaic devices are fabricated and assessed by optical and electrical characterization techniques, to identify areas for refinement of device design and processing.

Combining the unique properties of nanowire arrays, the quality and tunability of III-V materials, and the economics and infrastructure of silicon-based device fabrication, this work examines a novel approach to affordable renewable energy.

Methods of substrate removal via etching are investigated for optical characterization of nanowire arrays, and an improved technique for electrical characterization of ITO contacts is explored. The first nanowire-on-silicon tandem device utilizing a radial p-n junction nanowire structure is reported, achieving an open circuit voltage of 1.2 V, a short circuit current density of 7.6 mA/cm^2, a fill factor of 40%, and an efficiency of 3.5%. Finally, projects for future improvements to the work described herein are suggested.

Acknowledgements

First and foremost, I would like to thank my supervisor, Professor Ray LaPierre, for his guidance throughout this work. Despite the many roadblocks that I encountered, he was always supportive and worked with me constantly to seek creative solutions to move forward, pushing me to achieve better results. I am still in awe at the speed with which he is able to provide revisions to my writing, and with such great attention to detail.

I am grateful for the work of my predecessors, in particular Andrew Chia, who taught me nearly everything I know about semiconductor processing, and Jonathan Boulanger, who remained an invaluable source of knowledge regarding nanowire growth and microscopy. Thank you to the many other members of the LaPierre Research Group: Simon McNamee, Aziz Rahman, Amit Rao, Mitch Robson, Hadi Tavakoli, Paige Wilson, and Mitchell Wong for your unwavering support. Special thanks to Paul Kuyanov for going well out of his way to assist me with PL and EQE measurements and anything else that I needed help with.

I am indebted to Doris Stevanovic and Shahram Tavakoli from the Centre for Emerging Device Technologies at McMaster University for their immense knowledge of all the device fabrication equipment on campus. Thank you to Chris Butcher at the Canadian Centre for Electron Microscopy at McMaster University for his training and assistance in SEM. I would also like to acknowledge Alex Tsukernik at the Toronto Nanofabrication Centre at the University of Toronto for his help with EBL. Thank you as well to the rest of the staff in the Department of

Engineering Physics, in particular Marilyn Marlow and Peter Jonasson, both of whom served as vital resources throughout my graduate studies.

Credit is also due to my colleagues in Engineering Physics for keeping me sane during late nights in the lab and offering their valuable experience and insight into countless problems that I encountered: Ross Anthony, Kevin Boyd, Austin Brown, David Hagan, Bertha Hui, Dixon Paez, Karl Petursson, Abhi Rampal and everybody from WEB.

My family has been incredibly supportive and helpful throughout my graduate studies and beyond. Thank you so much to my mum and dad, Alex, Caitlyn, and Finian.

Special thanks to Gasp Solar and the Natural Sciences and Engineering Research Council whose support made this work possible.

Table of Contents

List of Figures

List of Tables

List of Abbreviations

III-V	compound semiconductor made up of group III and group V elements
AlInP	aluminum indium phosphide
AM1.5G	air mass 1.5 global (ASTM reference solar spectrum)
BCB	benzocyclobutene
BHF	buffered hydrofluoric acid
BSE	backscattered electron
EBL	electron beam lithography
EHP	electron-hole pair
EQE	external quantum efficiency
GaAs	gallium arsenide
GaAsP	gallium arsenide phosphide
GaP	gallium phosphide
HF	hydrofluoric acid
HNA	hydrofluoric acid / nitric acid / acetic acid
IPA	isopropyl alcohol
ITO	indium tin oxide
IV	current-voltage
LIA	lock-in amplifier
MBE	molecular beam epitaxy
nw	nanowire
PV	photovoltaic
QTH	quartz tungsten halogen
RIE	reactive ion etch
SEI	secondary electron imaging
SEM	scanning electron microscope
SOI	silicon-on-insulator
VLS	vapour-liquid-solid
VS	vapour-solid

1 Introduction

This thesis deals primarily with research into the growth and characterization of nanowires (nws). In particular, arrays of nws with spacing on the order of 500 nm, vertical length on the order of 2 µm, and diameter on the order of 200 nm, are grown perpendicularly on crystalline substrates. An example of a nw array is shown in Figure 1-1.

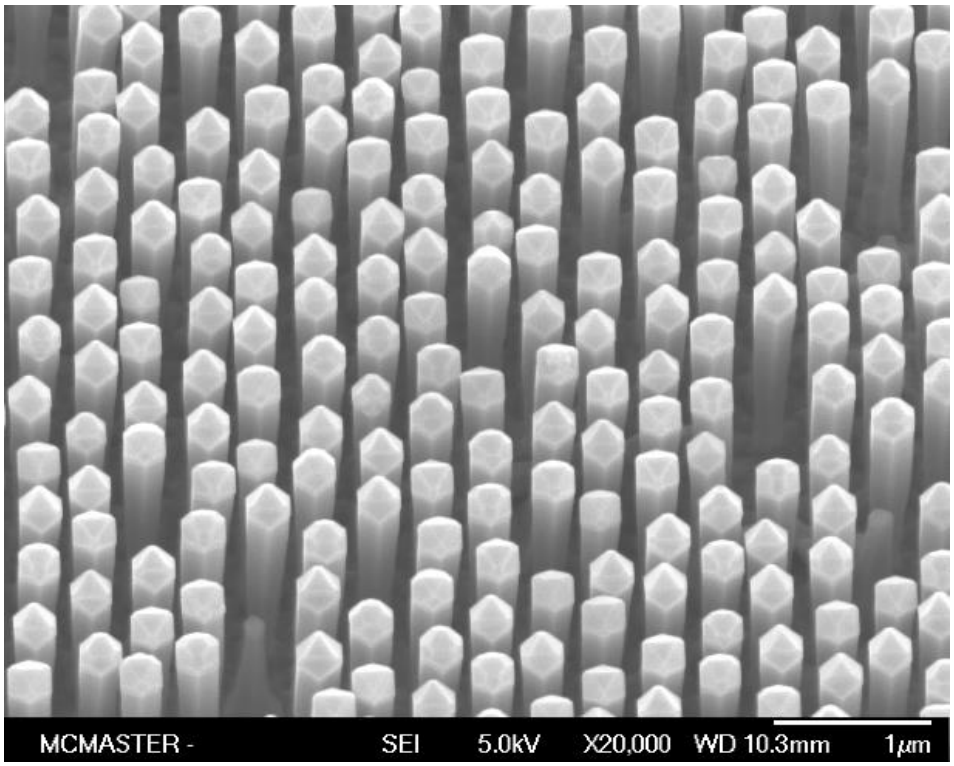

Figure 1-1: Scanning electron microscope image of a nanowire array following sample growth, prior to any device processing; image is taken at x20k magnification and 30° tilt (sample #1874, pad MP0440D3).

These nw arrays are then processed into devices to be characterized optically and electrically, and the results are presented.

1.1 Background on III-V nanowires

The nws studied in this work are III-V semiconductor (GaAs and $GaAs_{1-x}P_x$) nws grown via molecular bean epitaxy (described in detail in Section 2.3) on silicon.

III-V materials have favourable characteristics over silicon for various semiconductor device applications [1,2]; however, III-Vs are generally much more expensive than silicon. Many semiconductor devices have only a thin active region on the surface; ideally, a silicon substrate would be used to support the III-V layer, providing mechanical stability to the device, while taking advantage of the cost effectiveness of silicon and the superior optical and electrical properties of III-Vs. Unfortunately, the relative lattice constants of silicon (5.431 Å [3]) and many desirable III-V semiconductors (e.g. 5.653 Å for GaAs [4]) do not allow traditional thin films to be grown without drastically degrading the film quality with defects [5]. Each successive III-V atomic layer added to the thin film introduces more stress into the system until, at some critical thickness, it becomes energetically favourable to introduce a defect to relax the stress. This is a function of both film thickness and also cross-sectional film area.

The nw structure employed in this work overcomes this problem. By reducing the cross-sectional area, it is possible to grow high-quality lattice-

mismatched III-Vs on a silicon substrate without strain-induced defects. Furthermore, during growth, dopants can be incorporated into the nws to create p-n junctions and, in the case of this work, photovoltaic (PV) devices.

1.2 III-V nanowire arrays as photovoltaic devices

As alluded to above, III-V materials are preferable over silicon for PV devices. Many III-Vs have a direct bandgap, resulting in more efficient absorption of photons for conversion into electron-hole pairs (EHPs). Further, while the actual bandgap of silicon falls at a desirable level for single junction PV devices (1.12 eV), III-V semiconductors can be tuned to finely control the magnitude of the bandgap or the lattice constant, allowing for more flexibility in specialized devices [5]. For example, in the ternary III-V semiconductor $GaAs_{1-x}P_x$, the bandgap can be tuned from 1.42 eV to 1.98 eV (direct bandgap) and further to 2.26 eV (indirect bandgap), and the lattice constant can be tuned from 5.6532 Å to 5.4505 Å by adjusting x, the relative composition of As and P [4]. This property is utilised in this work, as described in Section 6.2.1.

Aside from the superior material properties of III-Vs, the nw structure also has favourable characteristics for PV and other optical devices. Firstly, since nw dimensions are on the order of the wavelength of light, wave optics must be applied when considering photon interactions. It is found that individual nws have a strong

‘waveguide’ effect – essentially funnelling light from an area around the nw into the wire itself, where that light can be absorbed [1].

Secondly, the doping structure of individual nws used in this work provides a unique benefit to maximize photon absorption and EHP collection. The nw devices in this work are grown with a core-shell doping structure, resulting in a p-n junction that runs the full length of the nw (a detailed schematic can be found in Section 2.3.2). This allows a relatively thick active region (the height of the nws) for photons to be absorbed and generate EHPs, but only requires a very short distance for the minority carriers to diffuse to the junction [6]. As seen in Figure 1-2, this contrasts with a standard thin film structure in which a thicker active region for increased absorption results in a greater distance for minority carriers to travel, before being swept across the junction, risking recombination and thereby limiting device efficiency.

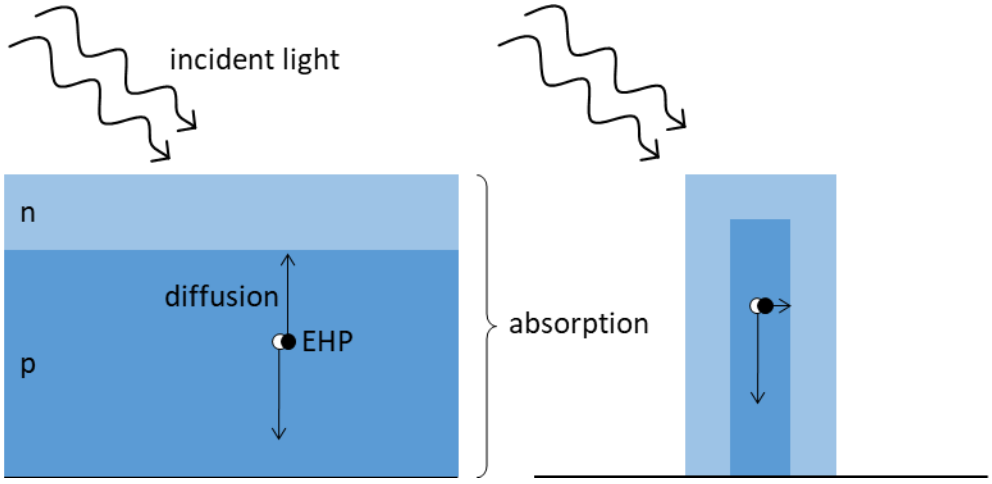

Figure 1-2: Schematic of a thin film versus core-shell nw solar cell structure, comparing absorption of photons and separation of EHPs across the p-n junction.

A third interesting feature of nw arrays is their adjustable absorption spectrum. This is due to the same behaviour of the nw acting as a waveguide, but the strength of this phenomenon is dependent on the wavelength of light and can be adjusted by varying either nw diameter or spacing between nws. Outside of applications in solar photovoltaics, this can be exploited to create an integrated multi-spectral detector, for example, but the nw diameter and spacing can also be optimized to tune the absorption peak to match solar irradiance [7].

1.3 Motivation of present work

The general purpose of this work is to continue exploring III-V nw arrays as PV devices and improve their performance by looking at various characteristics to

refine device design and processing. Specifically, Chapters 2 and 3 detail the general procedure for fabricating and characterizing nw PV devices and explores the background theory into these tools and processes. Chapter 4 investigates substrate removal on nw arrays to improve optical characterization of nws; specifically developing a method to measure the absorption of nws. Chapter 5 examines the transparent metal oxide layer used as a front contact for solar PV devices; the sheet resistance of this layer is very difficult to measure *in situ*, so it is essential to develop a good proxy in order to properly characterize this portion of the cell and develop incremental improvements to the overall contact scheme. Chapter 6 highlights fabrication and characterization of a tandem cell nw PV device; this improves on historical work growing single junction GaAs nw PV cells by growing tuned GaAsP nws on a silicon junction substrate. Lastly, Chapter 7 proposes ideas for future work in this area of research to refine and improve the results reported herein.

2 Device Fabrication

2.1 Introduction

This section describes the background theory behind various processes employed in device fabrication generally, and their specific applications in the procedure employed in this work. The processing steps listed here are meant to serve as a high-level overview of device fabrication. Additional information can be found in the Appendix under Processing Recipes.

The general device processing procedure for nw photovoltaic devices in this work begins with a clean, 3” diameter <111> p-type (boron-doped) Czochralski silicon wafer. The wafers are low resistivity (≤0.005 ohm·cm), approximately 300 μm thick, and the front side has been polished to a surface roughness less than 5 Å. Further detail can be found in the Appendix under Wafer Specifications.

2.2 Electron beam lithography

2.2.1 Background

Electron beam lithography (EBL) is a semiconductor fabrication process used to create high resolution features or structures on a device [8]. Initially the sample is coated in a thin polymer layer (electron beam resist). The polymer is chosen such that the structure is altered when exposed to an electron beam, modifying its solubility in a particular developer. Using a positive electron beam resist, for example, results in a stable polymer film, until exposed to an electron

beam. The area of the film that was exposed will be washed away during development, allowing for a pattern to be transferred onto the sample. The unexposed resist will remain on the sample after development, allowing subsequent processing steps (e.g. chemical etching) to affect only the patterned regions of the sample.

Using an electron-sensitive polymer instead of a more common photon-sensitive layer allows for much finer resolution in pattern transfer, since the de Broglie wavelength of electrons at these energy levels (100 keV) is much smaller than photons in the ultraviolet (UV) range. However, using an electron beam to pattern the device is a serial process, which limits fabrication throughput. The resolution capabilities of EBL are necessary to pattern the device for nw growth (features on the order of 50 nm), whereas UV photolithography, with a much higher throughput, is used in later processing steps to transfer a much coarser pattern for electrical contacting (features on the order of 100 μm), as described in Section 2.5.

Reactive ion etching (RIE) is used briefly in this part of device processing; however, the background of this method will be described in more detail in Section 2.4.1.

2.2.2 Processing

A thin layer (30 Å) of silicon oxide is deposited on the substrate using chemical vapour deposition (note that details surrounding this deposition method

are outside the scope of this work, but can be found in the accompanying references [9]). This oxide is then used as a pattern transfer layer for EBL. The wafer is sonicated in acetone and isopropyl alcohol (IPA) to ensure cleanliness before spin-coating with a ZEP502A:Anisole mixture to act as an electron beam resist. EBL is then performed to transfer the pattern (as shown in Figure 2-1) into the resist layer. During lithography, the electron beam energy used for all exposures is 100 keV with beam currents varying from 500 pA to 25 nA.

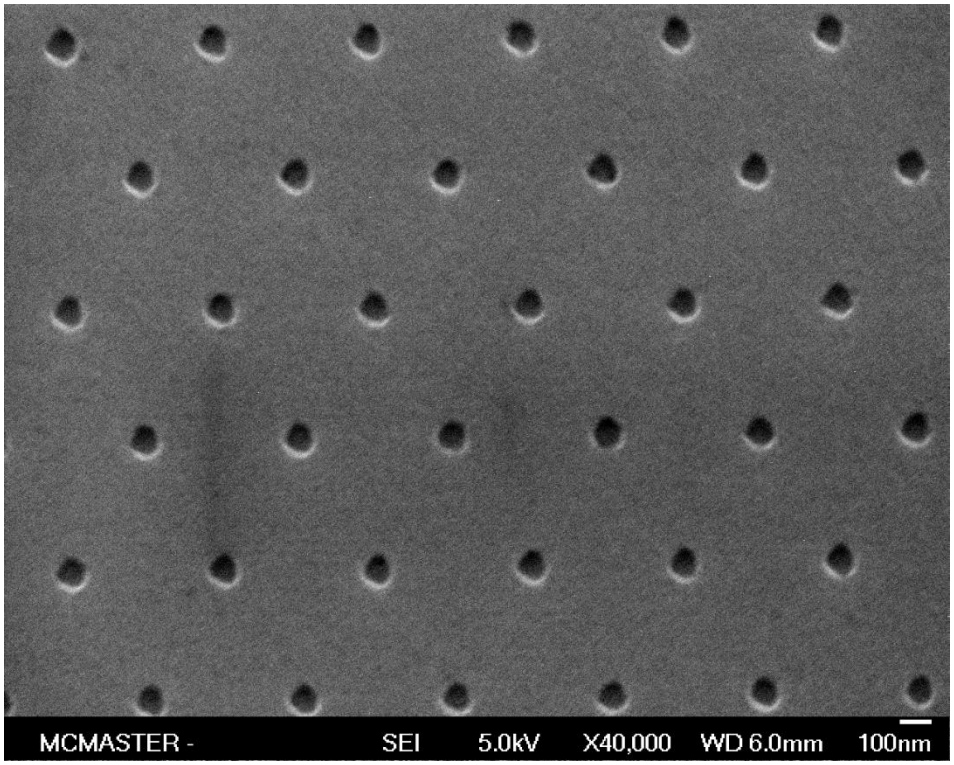

Figure 2-1: Scanning electron microscope image of EBL pattern, following transfer into the oxide layer, to prepare for nw growth. Each hole seeds the growth of a single nw. The EBL dose and pattern is adjusted to vary the diameter and spacing of the holes and subsequent nws.

The resist is then developed in ZED-N50 and cleaned with an MIBK:IPA solution (Figure 2-2). The pattern is further transferred into the oxide layer by a CF_4 RIE, before the EBL resist is fully stripped and the substrate is cleaned by sonication in ZMAC, acetone, and IPA.

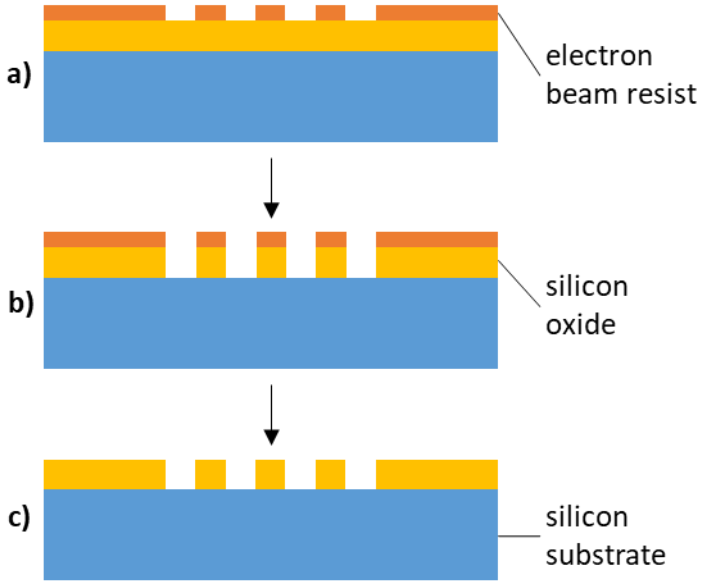

*Figure 2-2: Schematic detailing the EBL pattern transfer from the resist layer into the oxide layer using RIE; the sample is shown following (**a**) EBL exposure and development, (**b**) pattern transfer by RIE, and (**c**) removal of the electron beam resist. Features are not to scale.*

2.3 Molecular beam epitaxy

2.3.1 Background

The III-V nw arrays studied throughout this work are fabricated by a self-assisted growth method, using a gas source molecular beam epitaxy (MBE) system. Group III material (i.e. gallium) is provided by an effusion cell which is heated to evaporate the solid source. Group V materials (i.e. arsenic and phosphorous) are supplied as dimers by cracking hydride sources. During nw growth, there are two main regimes: axial (core) growth and radial (shell) growth. During either regime of growth, dopants can be introduced to control the electrical properties of the device.

Initially, group III adatoms directly impinge on the oxide holes (prepared during the EBL patterning step), or may diffuse along the surface to reach these holes, forming liquid droplets on the silicon substrate. During axial nw growth, group V dimers adsorb on the liquid droplet (desorbing from the oxide or nw sidewalls [1]), precipitating epitaxial nw growth at the base of the droplet. This is known as the vapour-liquid-solid (VLS) method – *vapour* precursors adsorb on the *liquid* droplet at the tip of the nw and the droplet is gradually pushed up as each epitaxial layer precipitates, growing a *solid* crystal structure at its base [10] – a schematic of the VLS process is shown in Figure 2-3. This process continues until the desired nw height is reached. The substrate is then cooled under group V flow to consume the group III droplet, while precipitating the desired III-V structure.

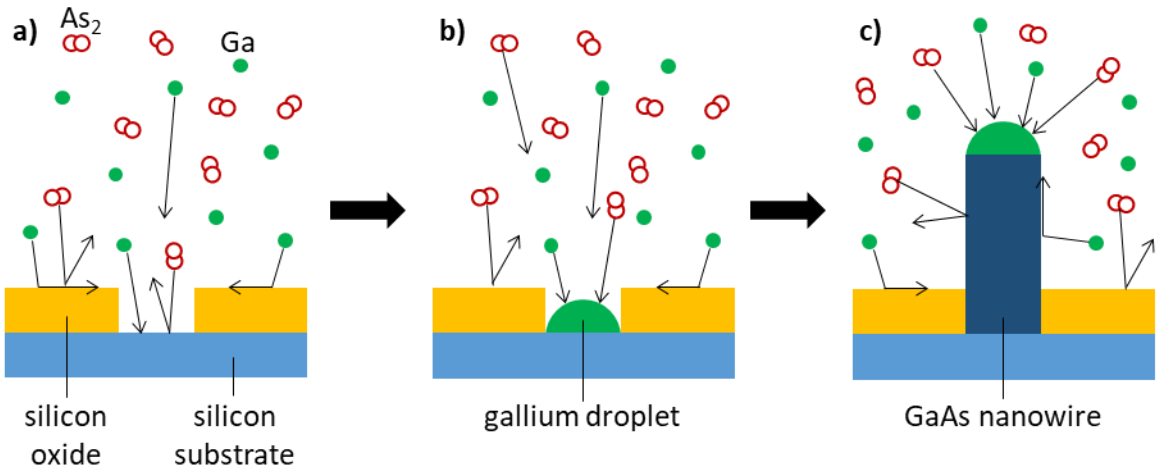

*Figure 2-3: Schematic of the VLS growth method; (**a**) group III and V precursors present in the MBE chamber, (**b**) initial formation of the group III droplet on the silicon substrate (in the oxide hole patterned by EBL), and (**c**) vertical epitaxial growth of the nw. Features are not to scale.*

Radial growth, on the other hand, occurs via the vapour-solid (VS) method. This is a lower temperature process whereby both group III and V adatoms adsorb and diffuse on the sample surface, growing epitaxial layers conformally around the nw. A schematic of the VS process is shown in Figure 2-4. Higher temperatures and lower V-III flux ratios tend to favour axial growth, whereas lower temperatures and higher V-III flux ratios tend to favour radial growth [11].

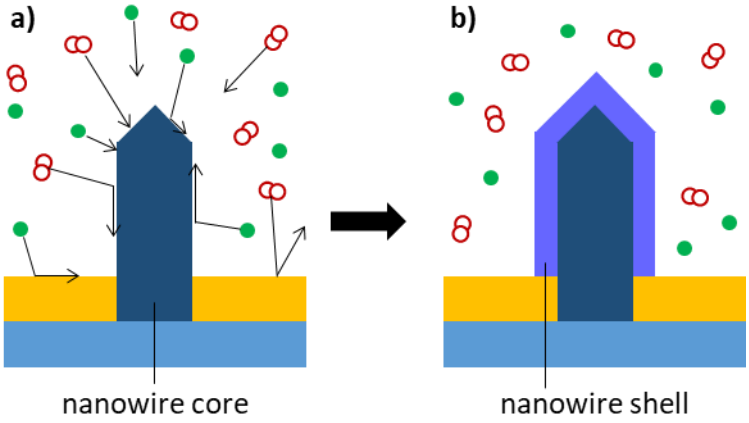

*Figure 2-4: Schematic of the VS growth method following consumption of the group III droplet; (**a**) adsorption and diffusion of group III and V precursors on the nw core, and (**b**) conformal epitaxial growth of a III-V shell. Features are not to scale.*

For the nw arrays prepared in this work, initially a p-doped core is grown, followed by an intrinsic shell, and a n-doped shell, forming a p-i-n diode structure. An additional thin n+-doped shell is added to enhance electrical contact [12] and finally a passivation layer is added to reduce surface recombination effects [13].

Note that the epitaxial nature of III-V nw growth requires the substrate to be in the <111> orientation, to ensure vertical growth of the nw. The more common <100> orientation of silicon results in unwanted nw growth at a 35 degree tilt to the surface [14].

2.3.2 Processing

Following EBL, the wafer is carefully cleaved along its primary crystal planes into six ‘pie-shaped’ pieces using a diamond scribe. Immediately prior to loading in the MBE chamber, the wafer is dipped in buffered hydrofluoric acid (BHF) to remove any subsequent native oxide growth and ensure the bare silicon at the bottom of the holes is fully exposed. The substrate is now ready for nw growth.

Once the substrate is loaded into the MBE chamber and brought under vacuum, it is degassed at 300°C for 15 minutes and subsequently exposed to a hydrogen inductively coupled plasma at 600°C for 10 minutes to remove any residual hydrocarbons from the surface. During MBE, nw growth is seeded in the oxide holes with p-doped (beryllium) GaP (since the lattice mismatch of GaP and Si is only 0.4% [3,4]) and the group V component is gradually ramped from P to $As_{1-x}P_x$ in the desired ratio (maintaining beryllium doping levels). After a specified growth duration, the chamber is cooled (maintaining group V flow to consume the gallium droplet), and an intrinsic (undoped) shell of GaAsP is grown, followed by an n-doped (tellurium) GaAsP shell and an additional thin n+-doped (tellurium) GaAsP layer. Finally, an AlInP passivation shell is grown. The final structure is shown in Figure 2-5. More detail on the specific growth conditions for the nw arrays studied in this work can be found in the MBE growth sheets included in Chapter 6.

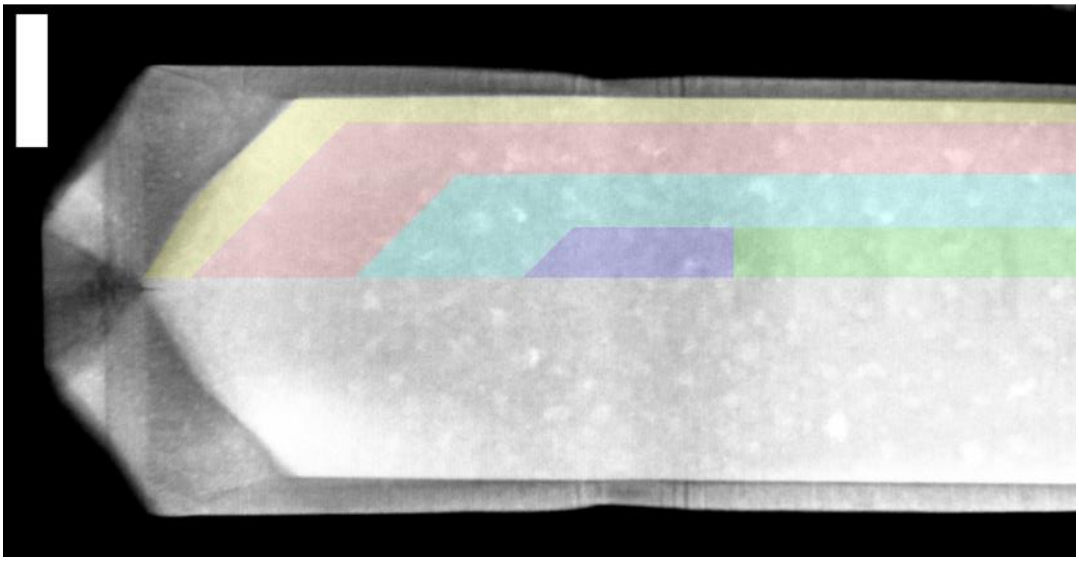

Figure 2-5: Transmission electron microscope image of a single nw, indicating each segment of the MBE growth; the nw begins with vertical p-GaAsP core growth (green) and Ga droplet consumption (purple); intrinsic (blue), n-doped (red), and n+-doped (yellow) GaAsP shells are subsequently grown; and an AlInP passivation layer (uncoloured) is added. Scale bar is 100 nm. Figure adapted from Boulanger et al. [12].

2.4 Planarization & etching

2.4.1 Background

Reactive ion etching (RIE) is employed several times during device fabrication. This technique is used to etch the sample anisotropically (in one preferred direction) and is known as ‘dry etching’ [15]. The sample is loaded into a vacuum chamber and an electric field is created between parallel plate electrodes

(with the sample sitting on the bottom plate). Process gases are pumped into the chamber and the electric field strips electrons from the gas, creating a plasma. The resulting ions are accelerated towards the sample where they collide with the surface and contribute to etching by chemical reaction and sputtering (described in more detail in 2.5). Since the plasma ions are accelerated in the direction of the electric field, RIE will preferentially etch the sample in this same direction, making it possible to create anisotropic structures on the surface of the sample (which is required prior to MBE, for example).

Wet etching is also used in this procedure to remove the passivation layer at the tips of the nws, once they have been exposed by RIE. The sample is immersed in an etchant which chemically reacts with the exposed surface of the sample. Depending on the etchant and the material to be etched, the process can be isotropic (equal in all directions) or anisotropic (as with RIE, above). For example, in the case of the BHF etch described in Section 2.3.2 the silicon oxide layer is etched isotropically. On the other hand, the crystalline AlInP nw passivation shell is preferentially etched by HCl along certain crystallographic facets, resulting in an anisotropic structure. Images of this facet-selective etching process can be found in Chapter 6.

2.4.2 Processing

With the nw growth complete, the next step is to planarize the device and expose the tips of the nws. The polymer benzocyclobutene (BCB) is used to coat the device due to its favourable electrical and optical properties, and its robustness [16]. Two layers of BCB are spun on the device and hard baked under nitrogen, ensuring the nws are fully covered. The BCB is then gradually removed by a CF_4:O_2 RIE until the tips of the nanowires are exposed (this process is monitored by repeatedly observing the sample in a scanning electron microscope). Once the tips are exposed, the passivation layer is removed by a wet etch in an HCl solution to prepare the sample for electrical contacting.

2.5 Contact application

2.5.1 Background

Applying metal contacts to the device is the final step before the device can be characterized. The contacting scheme is divided into three separate parts: the transparent front contact, the opaque front contact, and the rear contact. The desired patterns for the front contacts are applied using photolithography. The transparent contact and rear contact are applied by sputtering and the opaque contact is applied by electron beam evaporation.

Photolithography is very similar to the EBL process described in Section 2.2. In this case, however, a photon-sensitive polymer (photoresist) is employed and

the sample is exposed to UV light instead of an electron beam. By using a UV lamp, the entire sample can be exposed at once, instead of raster scanning an electron beam, as in EBL. The contact pattern is applied by inserting a chrome photomask between the sample and lamp so only the desired area of the sample is exposed to UV light. Since the resolution of photolithography is limited by the wavelength of light, this higher throughput process cannot be used to create the much smaller feature size required for the patterning prior to nw growth, so EBL is used instead.

Both sputtering and electron beam evaporation are methods of thin film deposition. During sputtering [17], an inert process gas (commonly argon) is pumped into a vacuum chamber and, as in RIE, an applied electric field strips electrons from the process gas, creating a plasma. The resulting ions are accelerated towards the sputtering target (cathode) where they collide with the surface, physically ejecting atoms from the target. These atoms impinge onto the sample stage (anode), and surrounding chamber, depositing a thin film of the same material as the target. The applied electric field power and process gas flow rate can be adjusted to control the deposition rate.

During electron beam evaporation [18], electrons are generated by running a current through a filament and are accelerated towards a crucible holding the metal to be deposited. The electron beam heats up the crucible such that a vapour is formed from the metal. The vapour, as with sputtering, impinges on the sample stage and surrounding deposition chamber, depositing the desired thin film. The

beam current and accelerating voltage can be adjusted to control the deposition rate.

In both cases, the deposition process is monitored using a crystal thickness monitor [19]. A piezoelectric crystal (quartz) resonator is mounted close to the sample stage in the deposition chamber. As metal is deposited on the sample, it is also deposited on the crystal. This tool monitors the frequency of the resonator in situ and correlates the change in resonant frequency to thin film growth on its surface; this is then correlated to thin film growth on the sample itself.

2.5.2 Processing

The front contact pattern is applied using standard photolithography techniques. A layer of Microposit S1818 positive photoresist is spun on the sample and soft baked. The sample is selectively exposed to UV light through a mask and then dipped in toluene to harden the top layer of the resist (improving lift-off). The sample is then over-developed in MF319 to remove the exposed photoresist and slightly undercut the photoresist that was not hardened by the toluene dip. This allows for easier lift-off following sputtering or electron beam evaporation [20], as demonstrated in Figure 2-6.

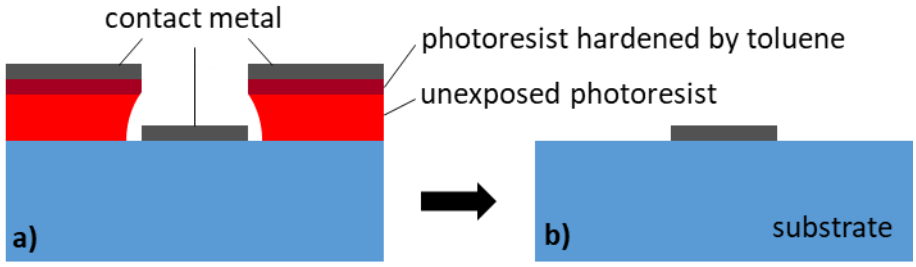

*Figure 2-6: Schematic detailing photoresist development procedure, (**a**) prior to and (**b**) following lift-off. After exposure to toluene, the top layer of the photoresist is not as susceptible to development; therefore, subsequent over-development has the effect of undercutting the photoresist around the desired pattern, allowing for easier lift-off. Features are not to scale.*

A 250 nm thick layer of indium tin oxide (ITO) is sputtered on the front of the sample and the sample is then immersed in acetone for approximately thirty minutes. This dissolves the photoresist that remains on the sample, 'lifting-off' the ITO that was deposited on the photoresist, and leaving behind the ITO that was deposited directly on the sample (i.e. where the sample was exposed to UV light through the mask).

This process is repeated using a second mask pattern and depositing a layer of nickel / germanium / gold (Ni/Ge/Au, 25 nm / 50 nm / 225 nm thick, respectively) by electron beam evaporation. Again, the metal deposited outside of the desired pattern is lifted-off.

The first photolithography pattern corresponds to the transparent contact layer (ITO). This contact layer completely covers the nw arrays and extends into a 'contact finger', providing enough room such that electrical measurements can be made on the sample. The second pattern corresponds to the opaque contact layer (Ni/Ge/Au) which only covers the contact fingers (leaving the nws exposed, in order to perform measurements under illumination). The nickel adheres strongly to the ITO layer, while the gold provides a soft surface to achieve effective electrical contact to the electrical probes. An image of the contact finger layout is included below in Figure 2-7:

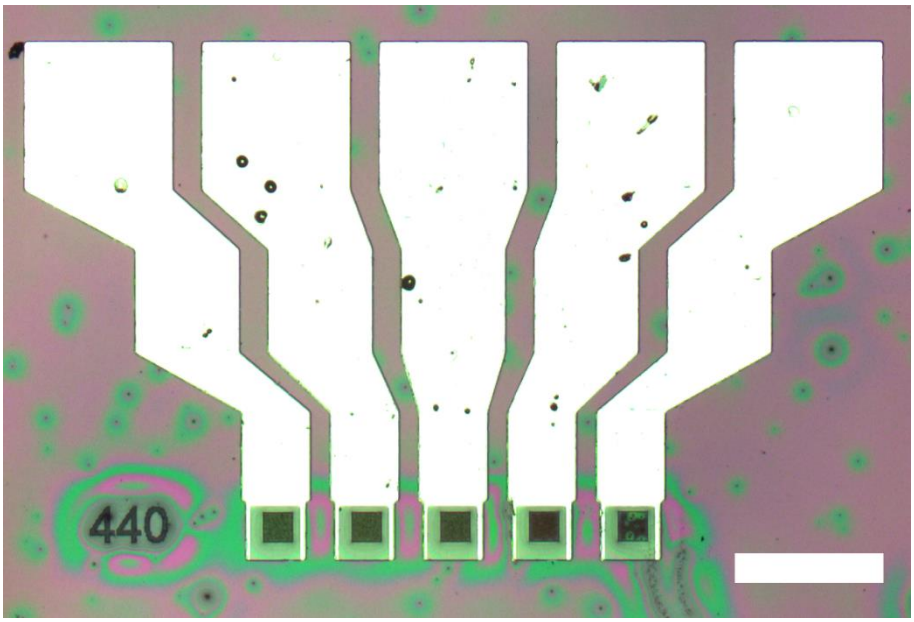

Figure 2-7: Layout of the front contact layer patterned on #1865 using photolithography, sputtering, and electron beam evaporation; the small black squares are the nw arrays covered in ITO, the white fingers are Ni/Ge/Au. Scale bar is 500 µm.

The rear contact does not require a photolithography mask. The edges of the sample are simply covered in vacuum tape (to prevent any possible device shorting) and a 400 nm thick layer of aluminium is sputtered on the back of the sample. The final contact scheme is shown below in Figure 2-8:

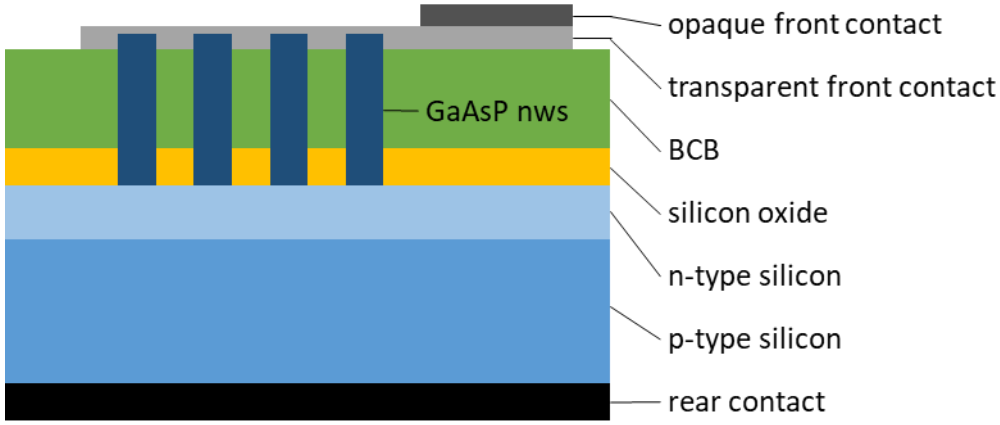

Figure 2-8: Schematic showing the final device structure of a tandem cell following front and rear contacting. Details regarding the core-shell structure of the nws have been omitted. Features are not to scale.

2.6 Annealing

Finally, the device is annealed using a rapid thermal annealer. This serves two primary purposes: to ensure effective electrical contact between the sample and the deposited metals, and to improve the transparency of the ITO contact layer [21]. During this process, the sample is loaded into a carbon susceptor which is then exposed to a high power lamp. The susceptor efficiently converts the light

energy into thermal energy, heating up the sample over a short time period (typically on the order of one minute).

A quartz microscope cover slide is included as a ‘witness’ sample during ITO sputtering to characterize the transparency of the film. Prior to annealing, the transparency of the ITO layer is approximately 76%, when weighted to the AM1.5G solar spectrum and accounting for the bare quartz baseline. After annealing, the transparency improves to 89%. Details of the electrical properties of the front contact layer are investigated in Chapter 5.

3 Device Characterization

3.1 Solar simulation

Characterizing photovoltaic devices using the sun can be difficult and unreliable. Local irradiance, seasonal changes, daily cloud cover, and time of day, for example, can all have vast impacts on the measured performance of a device. For this reason, it is important to be able to take measurements against a standard reference.

The standard spectral irradiance used for solar cell testing is referred to as the AM1.5G spectrum [22]. In this work, a xenon arc lamp was used to mimic this spectral output. Figure 3-1 shows the AM1.5G spectrum and the typical output from a xenon arc lamp.

The lamp is powered by a Newport 69907 lamp controller and the light is passed through a neutral density filter. The lamp controller is adjusted to achieve an output power density of '1 sun', or 100 mW/cm^2, as measured by a Newport 91150 Reference Cell. The reference cell is a robust PV device, designed to provide reproducible and reliable electrical behaviour. Its characteristics are verified by the National Renewable Energy Laboratory and it is used to calibrate subsequent solar simulator measurements. Once the lamp has been set up and calibrated, the electrical characteristics of a device can be measured.

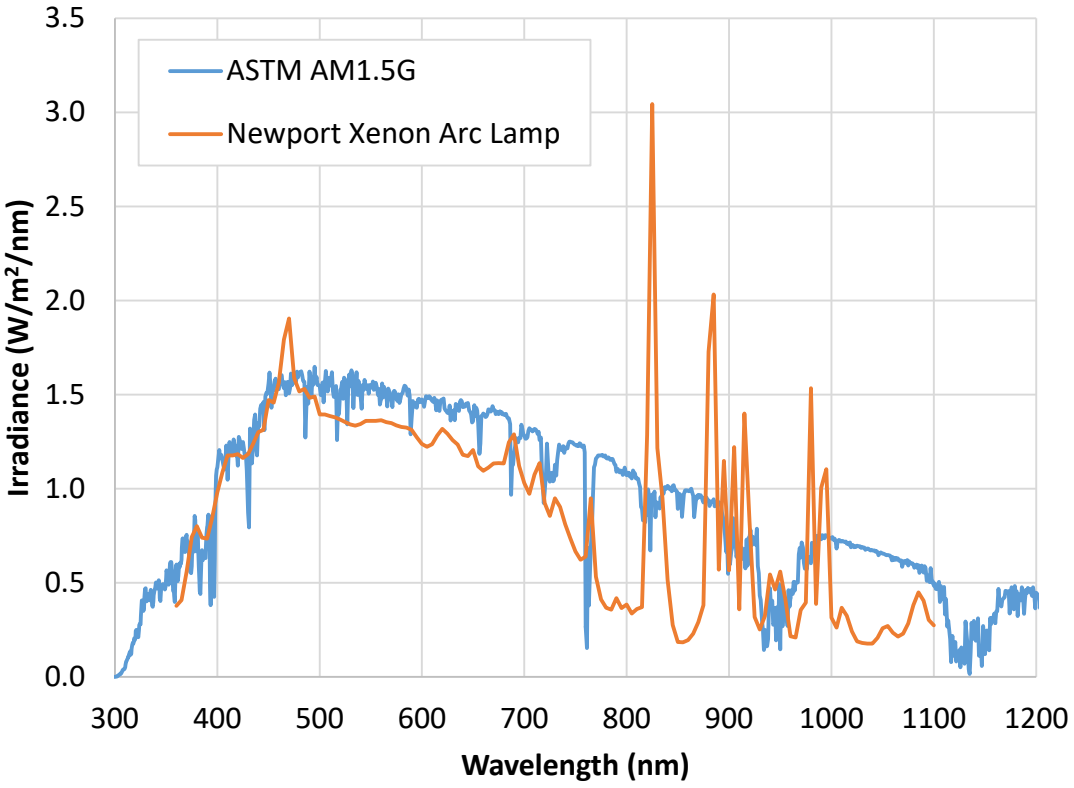

Figure 3-1: AM1.5G compared to xenon arc lamp spectra, the broadband output of the lamp can be scaled up or down by changing the input power or the neutral density filter.

The device is mounted on a metal stage, ensuring good electrical contact between the aluminium rear contact and the stage. The sample is then probed, using Micromanipulator 250 / 350 probes in a four-point arrangement – two hard probes in contact with the stage and two soft probes on the contact finger of the cell under measurement, as seen in Figure 3-2. While sourcing voltage and sensing current, the four-probe arrangement is used to improve the accuracy of

the measurement [23]. In the simpler two-probe arrangement, there is a voltage drop at either side of the sample arising from the contact resistance present due to the probe-sample interface. Since the current flows through the same source probes, this voltage drop is equal to $V_{contact} = I_{probe} \times R_{contact}$, per Ohm's Law. The overall bias on the cell is reduced from V_{source} to $V_{source} - V_{contact1} - V_{contact2}$. The four-probe arrangement eliminates the effect of this contact resistance between the probes and the sample surface by using a high impedance pair of probes to bias the sample, minimizing I_{probe} (and therefore $V_{contact}$), and a low impedance pair to measure the current.

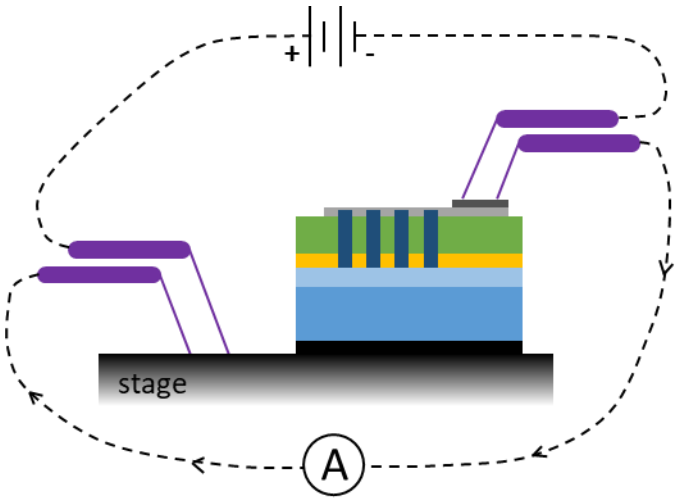

Figure 3-2: Schematic of four-probe arrangement used for IV measurements.

The probes are connected to a Keithley 2400 SourceMeter which performs a voltage sweep, typically between -2 V and +2 V, measuring the current flowing

through the sample for each input voltage at a specified step size, creating a graph of current versus voltage, or an 'IV curve'. This measurement is taken in the dark and repeated under illumination. The light and dark IV curves can be analysed to characterize the device based on its open circuit voltage, short circuit current density, fill factor, efficiency, reverse saturation current, breakdown voltage, etc.

3.2 Quantum efficiency measurement

As described briefly in Chapter 1, PV devices operate by absorbing energy from incident light and converting this to electrical energy. The quantum efficiency of a solar cell is a ratio of the number of electrons collected by the cell to the number of photons. External quantum efficiency (EQE) considers the number of photons *incident* on the cell, whereas internal quantum efficiency (IQE) considers the number of photons *absorbed* by the cell. This work is concerned with the measurement of EQE which can then be used to infer IQE by separately measuring the reflection and transmission of the same device, in order to calculate its absorption.

EQE is measured at a range of wavelengths to determine the spectral response of the device. In this work, the output from a broadband light source is passed through a monochromator, to select a narrow wavelength band, and is directed to the sample stage. Initially, the output power density for each wavelength range is measured using a power meter. The power, in Watts, can

simply be converted to a number of photons per second using the relationship between wavelength and photon energy ($E = \frac{hc}{\lambda}$), which can further be converted to photon flux ($\Phi(\lambda)$, number of photons per second per unit area), by inserting an aperture of known area between the source and the power meter.

The sample itself is then mounted on the stage in place of the power meter and the wavelength sweep is repeated. The short circuit current density is recorded at each wavelength ($j_{sc}(\lambda)$) and divided by the charge per electron to calculate the number of electrons per second per unit area. The EQE is then simply the ratio of this value to the photon flux, per Equation 3-1:

$$EQE(\lambda) = \frac{j_{sc}(\lambda)/q}{\Phi(\lambda)} \tag{3-1}$$

A quartz tungsten halogen (QTH) lamp is used as the light source for determining EQE due to its smooth broadband output over the wavelength range of interest (in contrast, the xenon arc lamp discussed in Section 3.1 would be unsuitable for this application due to the 'irradiance spikes' between 800 nm and 1000 nm). A Horiba iHR550 Imaging Spectrometer and Newport 2936-C Optical Power Meter were used as the monochromator and power meter, respectively.

Unique challenges associated with measuring the EQE of tandem and multi-junction solar cells will be discussed in detail in Chapter 6.

3.3 Scanning electron microscopy

In the context of the present work, scanning electron microscopy (SEM) is an invaluable tool used for directly observing the structure of nw arrays (and was also used to image ITO films) [24]. Images were captured using a JEOL JSM 7000F Field Emission SEM. To prepare for SEM, the sample is mounted and loaded into a vacuum chamber. An electron beam, on the order of 5 keV and 100 μA, is focused on the sample. The beam is raster scanned (as with EBL, described in Section 2.2) across an area of the sample to produce a 2-D image.

There are a number of different ways in which this beam interacts with the sample, but the majority of the images captured for this work are recorded by secondary electron imaging (SEI). In SEI mode, atoms on the surface of the sample eject ‘secondary’ electrons from their outer orbitals, which are captured by a detector [24]. SEI mode is an excellent method for observing surface topography and crystallographic faceting, as seen in the images in Section 6.3.1.

The accelerating voltage can be adjusted to improve the quality of the resultant image, depending on the sample and features of interest. For example, increasing the accelerating voltage will increase the signal-to-noise ratio, but decrease the resolution as the electron beam is now interacting with a larger volume of the sample. Imaging samples with higher atomic number usually requires a higher accelerating voltage, and vice versa.

Observing insulating samples under SEM can be difficult, since a negative charge is built up on the surface by the incident electron beam, causing imaging artifacts. This is commonly avoided by coating an insulating sample with a very thin layer of conducting material (e.g. carbon) [25].

During typical device fabrication, the sample will be observed in the SEM following growth to see nw morphology (height, taper, faceting, uniformity, etc.) and nw yield (the percentage of EBL-patterned holes which seeded growth of a nw with good morphology) for each array, and to determine if the sample is a good candidate to proceed with processing. The sample is also observed in the SEM during, and after, the planarization and etching step described in Section 2.4.2 to monitor the total etch depth and stop after an appropriate amount of material has been removed. This step, in particular, can be challenging as the BCB used to planarize the device is insulating, but the sample cannot be carbon-coated for proper imaging since this would destroy the PV device.

3.4 Sheet resistance measurement

Once a semiconductor junction has been created, each side of the junction must be electrically contacted before a PV device can be of any use. As described in Section 2.5, a layer of transparent ITO is deposited over the nw array of the PV devices in this work. This contact layer will impact device performance, acting as a resistor in series with the cell. For a resistor with length L, width w, thickness t,

and resistivity ρ (and current flowing in the direction of L), its resistance is given by Equation 3-2:

$$R = \rho \frac{L}{t * w} \tag{3-2}$$

When operating at any point less than the open circuit voltage of the cell, some of the power output will be dissipated in this resistor. Ultimately, this has the effect of lowering the fill factor of the device and reducing the overall efficiency, so it is clear that the resistance of this contact layer should be as small as possible [26]. Since resistance is inversely proportional to thickness, a thick contact layer could address this problem, but this would in turn decrease the transparency of the film. It is important to be able to accurately characterize this resistance to design an optimal front contact structure.

For the same reasons described in Section 3.1, a four-probe arrangement is typically employed. In this case, however, a current is sourced through the sample via one pair of probes and the voltage is measured via another pair. This technique is used to measure the 'sheet resistance', R_s, of the ITO film which is a function of material resistivity and film thickness [27], per Equation 3-3:

$$R_s = \frac{\rho}{t} \tag{3-3}$$

One such arrangement of probes is the 'in-line' method. Four equally spaced collinear probes are placed on the surface of the thin film; a current is passed through the outer probes and the potential difference between the inner probes is recorded [27]. The relationship between applied current and measured voltage is affected by the sample geometry, but an accurate measure of sheet resistance can be calculated if certain criteria are met. Smits showed that for a sample of uniform thickness and dimensions much larger than the probe spacing, the sheet resistance can be calculated using Equation 3-4 [27]:

$$R_s = \frac{\pi}{\ln 2} * V/I \tag{3-4}$$

Specific challenges of measuring the sheet resistance of ITO, and alternate techniques, will be discussed in detail in Chapter 5.

3.5 Photoluminescence

Photoluminescence is a technique used to characterize the band structure of a semiconductor [28]. The target material is illuminated using a laser with enough energy to excite carriers above the bandgap. These excited carriers will quickly dissipate energy via heat (thermalize) and move to the edge of the band, before recombining by radiant emission, as shown in Figure 3-3. The emitted light is then passed through a monochromator before striking a detector. The resultant

data shows the relative intensity of light emitted from the sample as a function of wavelength. A strong peak in the photoluminescence spectrum will typically indicate the bandgap for a direct gap semiconductor, such as GaAsP.

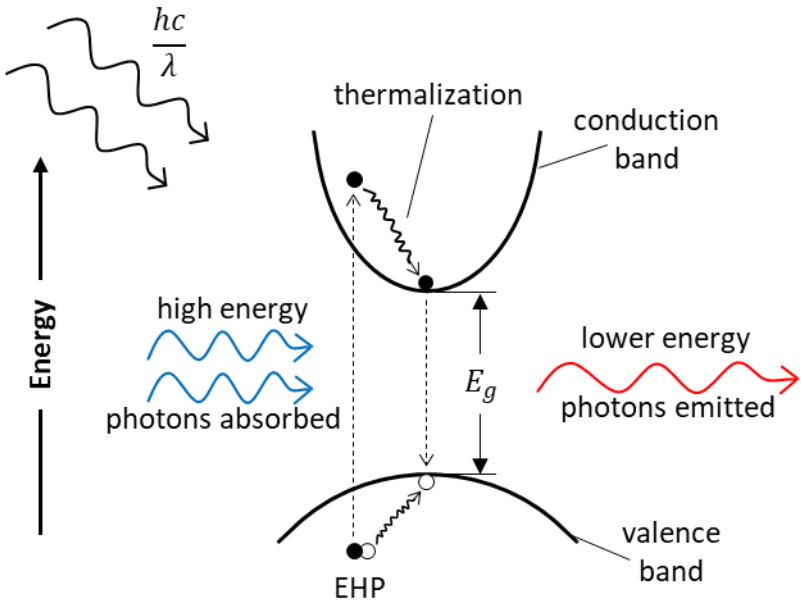

Figure 3-3: Photogeneration of an EHP, exciting an electron from the valence band to the conduction band, followed by rapid thermalization, recombination, and photon emission near the bandgap energy.

For sample characterization in this work, a 488 nm wavelength argon ion laser was used to excite the sample. The photoluminescence signal was passed, via a filter (removing any reflected laser light), through a Horiba iHR550 Imaging Spectrometer to a Horiba Symphony II detector.

3.6 Ellipsometry

Ellipsometry is an optical technique used to characterize thin film structures [29]. In this work, a J.A. Woollam M-2000UI Ellipsometer was used to measure the thickness of silicon oxide films and to measure the transparency of ITO films.

In the case of film thickness measurements, the sample is placed on a stage such that light will reflect off the sample and strike a detector. The light source is a broadband lamp (either deuterium or QTH lamp, depending on desired wavelength range) that is passed through a linear polarizer; a grating is situated in front of the detector to provide wavelength-selective measurements. Some light will reflect off the surface of the thin film, while some light will be transmitted through the film and reflect off the top of the substrate instead. As linearly polarized light is reflected, it becomes elliptically polarized and this change in polarization is different for reflections from the film and the substrate. The phase interference of these two reflections is measured at the detector across a range of wavelengths and for several angles of incidence, as seen in Figure 3-4. Knowing the index of refraction of both the substrate and the thin film (in this case, silicon and silicon oxide, respectively), the film thickness can be inferred by adjusting model parameters to match the collected data.

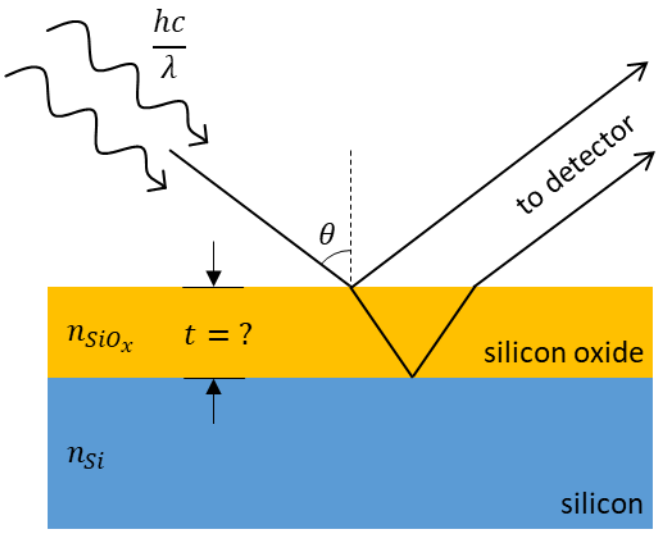

Figure 3-4: Schematic showing the operation of the ellipsometer for film thickness characterization; as the angle of incidence and wavelength vary, so will the interference recorded by the detector, allowing determination of the unknown thickness (t = ?).

For film transmittance measurements, the source light shines directly on the detector and the sample is placed perpendicularly in between them. The detector records the intensity of light for a range of wavelengths, compared to a reference measurement (with no sample present). When sputtering samples with ITO for electrical contacting, a transparent quartz microscope slide ('witness sample') is included on the sample stage. The transparency of this witness sample is then measured (before and after annealing), in place of the actual device. In order to calculate the transmission of the ITO film in isolation, the measurement is repeated with a blank quartz slide as a baseline.

4 Optical Characterization of Nanowires by Substrate Removal

4.1 Introduction

As described in Section 1.2, the waveguide nature of nws offers unique advantages in photovoltaic applications. The strength of this effect depends on a number of nw properties including material, spacing, and diameter [2]. Further, since the absorption of light is a function of material thickness, the length of the nws must also be considered. It is useful to be able to characterize the absorption of a nw sample to optimize these properties for a given application and to verify optical absorption models. However, it can be challenging to measure absorption directly.

When light is incident on some material, it can either be reflected off the surface, absorbed within the material, or transmitted through the material. This is represented in Equation 4-1 where R, A, and T represent the fraction of light reflected (reflectance), absorbed (absorptance), and transmitted (transmittance), respectively [30].

$$R + A + T = 1 \tag{4-1}$$

It is therefore possible to measure both reflectance and transmittance, and calculate absorptance. Measuring reflectance requires a relatively straightforward experimental set-up and is outside the scope of this work [31]. On the other hand, to measure transmittance, it is necessary to isolate the absorptance due to the

material itself (in this case nws) from the absorptance due to the substrate (upon which the nws are grown). Measuring the transmittance of an ITO film is demonstrated in Sections 3.6 and 6.3.5, for example, but this method relies on the use of a transparent substrate (quartz). The nw arrays described in the present thesis require growth on a relatively thick silicon substrate (hundreds of microns), which absorbs virtually all the light passing through the nw array. Thus, the method used to measure transmittance of ITO films cannot be used for nw arrays.

Instead, substrate removal was attempted to measure transmittance of the nw arrays directly, and to ultimately calculate absorptance using Equation 4-1.

4.2 Experimental approach

There are several approaches which can be taken to remove the silicon substrate while leaving the nw array intact. One such method would employ a selective etch based on the material difference between silicon and the nws. Another method would be to use a process with a known etch rate and calculate the time required to etch through the substrate, stopping as soon as the nw array has been exposed (or very close).

It is important to note, however, that besides providing a base upon which to seed nw growth, the substrate also provides structural stability to the nw array. In both of the methods outlined above, there are structural stability issues with removing the substrate entirely. Two major issues, in particular, must be

addressed. First, since the absorptance of the nws depends on spacing and orientation, the nw array must stay in place after the substrate has been removed. This can be achieved by applying a thick coat of BCB over the nw array, as in Section 2.4.2, to provide a stable matrix to hold the nws in place once the substrate is removed. Secondly, the substrate also provides stability in order to handle the sample itself. Attempting to characterize a sample that is only a couple of microns thick would be extremely difficult. To that end, the sample can be masked to etch only a 'window' into the substrate, leaving the majority of the substrate intact. The window can be aligned with the nw array on the front surface. An example schematic of such a set-up is shown in Figure 4-1.

Both wet and dry etches were initially considered. However, standard RIE recipes for silicon etching achieve etch rates on the order of 100 nm / min [15], taking over 24 hours to completely etch through the substrates used for this work. Therefore, based on available equipment, dry etching via RIE was not attempted. 'Deep RIE' could be investigated as a possible dry etch alternative, achieving etch rates in excess of 25 µm / min, but was not explored for this work [32].

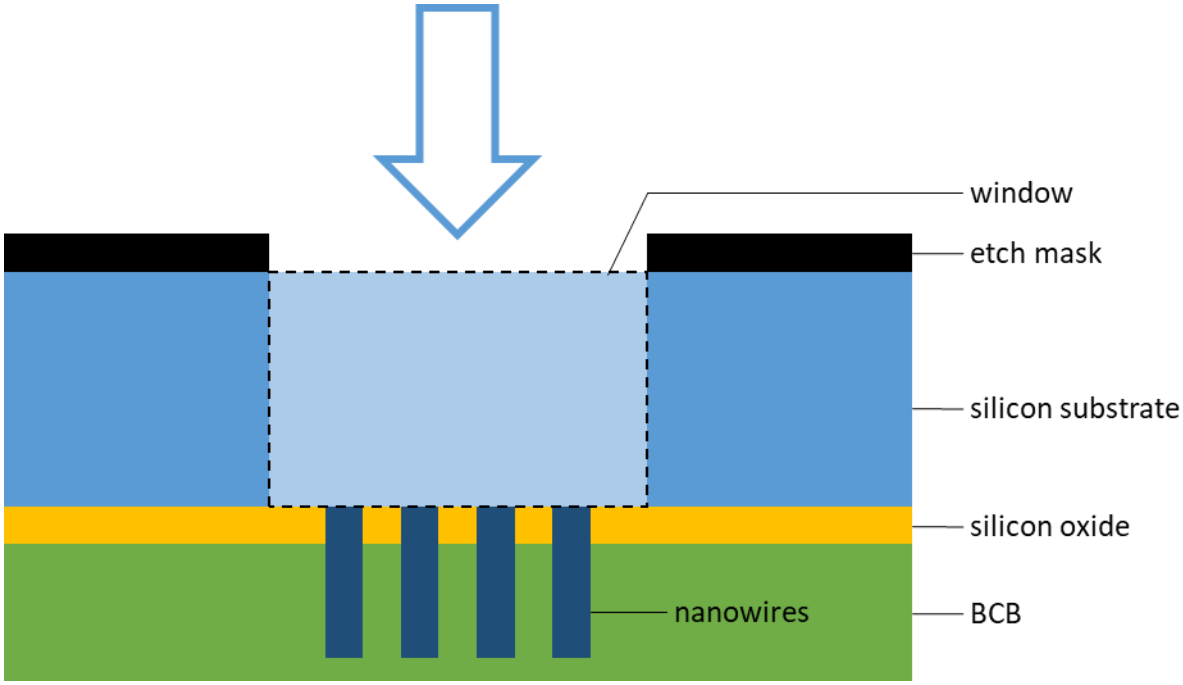

Figure 4-1: Schematic showing inverted nw sample and proposed set-up for substrate removal. The BCB provides a matrix for the nw array to maintain its structure after the substrate is etched; and the mask opens an etch window, protecting the surrounding substrate to maintain overall structural stability of the sample. The arrow indicates etch direction. Features are not to scale.

Wet etching through a silicon <111> wafer can be challenging. Many common silicon etchants, such as potassium hydroxide or ethylenediamine pyrocatechol, are anisotropic and etch the <111> plane much slower than the <100> and <110> planes [33]. For this work, a combination of hydrofluoric acid (HF), nitric acid, and acetic acid, known as HNA, was used to etch silicon isotropically, to achieve reasonable etch rates to fully remove the silicon substrate

[34]. In an HNA etch, the nitric acid oxidizes the silicon, forming silicon dioxide; the HF chemically etches the oxide, forming aqueous hexafluorosilicic acid; and the acetic acid acts as a dilutant [35]. Note that acetic acid is preferred as a dilutant since it enhances the oxidation power of the nitric acid, compared to using water as a dilutant. The combined chemical reaction is shown below in Equation 4-2:

$$Si + HNO_3 + 6HF \rightarrow H_2SiF_6 + HNO_2 + H_2O + H_2 \quad (4\text{-}2)$$

The samples used for this experiment consisted of separate GaAs, GaAsP, and GaP nw arrays on silicon <111> substrates. Unfortunately, the selectivity of HNA on silicon versus GaAs, GaAsP, and GaP is not well documented [36], so the 'timed etch' method described above was employed.

The HNA solution was prepared by mixing one part 48% HF to two parts 69% nitric acid to three parts acetic acid [37]. This composition was chosen to give an etch rate on the order of 5 µm / min for an expected total etch duration of approximately 1.5 hours. The sample was submerged in the etchant using a polytetrafluoroethylene dipper basket. The sample was agitated every minute and visually inspected to monitor etch depth. After the substrate was fully removed, the sample was quenched in deionized water and rinsed thoroughly.

After some preliminary attempts, the etchant was observed to have a visible effect on the BCB coating so this was further protected by adhering the sample to a quartz microscope slide using a transparent epoxy (EPO-TEK 301-2).

Additionally, an etching wax (Apiezon Wax W) was used as a mask for the etch window and also to protect the exposed surface of the microscope slide. Following substrate removal the protective wax was dissolved using trichloroethylene. The final schematic used for the etching procedure is shown in Figure 4-2.

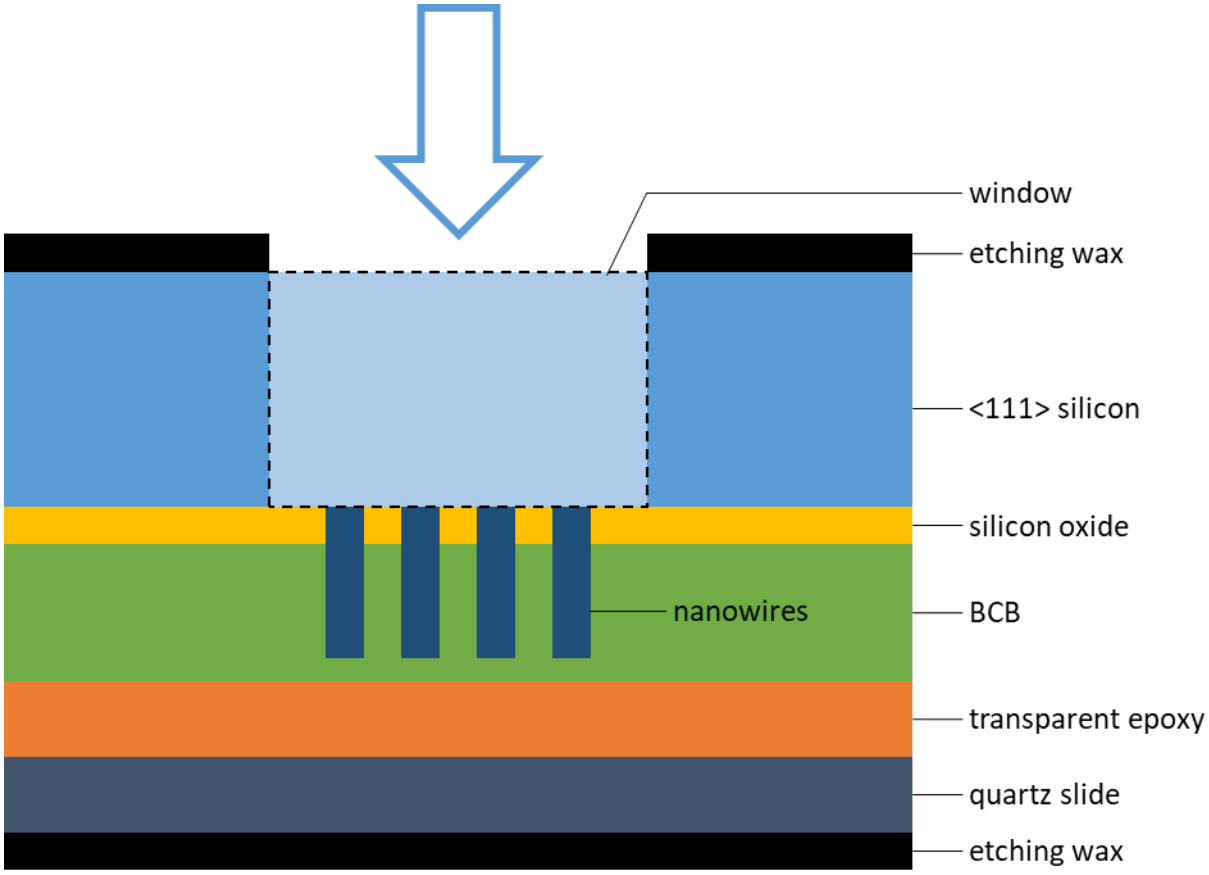

Figure 4-2: Updated experimental schematic showing the transparent epoxy, quartz microscope slide, and etching wax included to protect the front of the sample from the HNA etchant. The arrow indicates etch direction. Features are not to scale.

4.3 Results

Light microscope images of various samples are presented below. Figure 4-3 and Figure 4-4 show a single nw array before and after substrate removal by HNA etching; the nw materials are GaAs (sample #1710) and GaAsP (sample #1709), respectively. The pre-etch images are taken top-down, following BCB application. The post-etch images are taken from the rear of the sample (i.e. in the direction of the arrow in Figure 4-2), after wax removal. Lastly, Figure 4-5 shows a series of GaP nw arrays (sample #1677) following the same etching procedure.

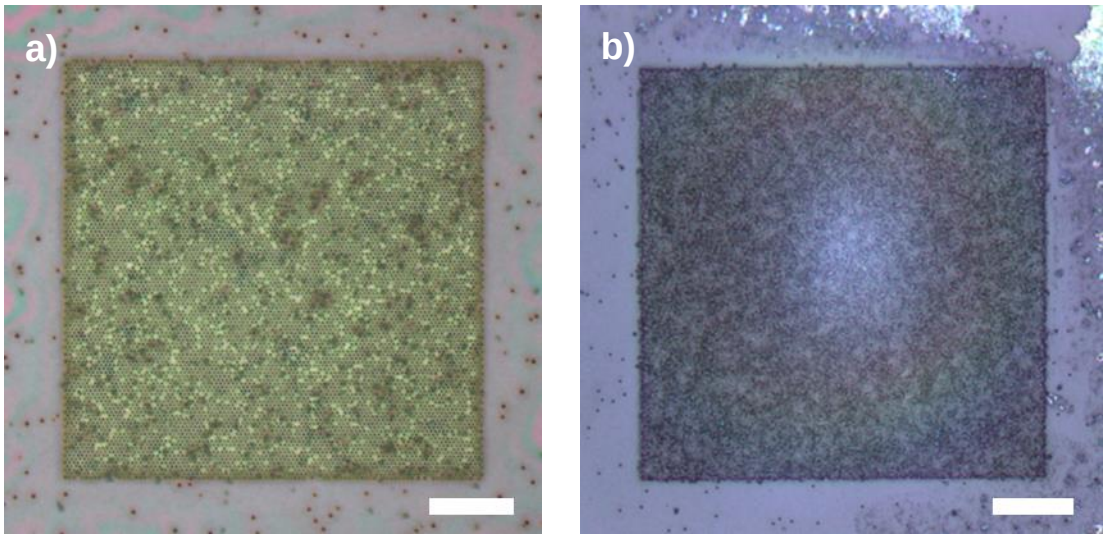

*Figure 4-3: Light microscope image of sample #1710, a GaAs nw array, (**a**) before and (**b**) after a 98 minute HNA etch. Scale bars are 20 µm.*

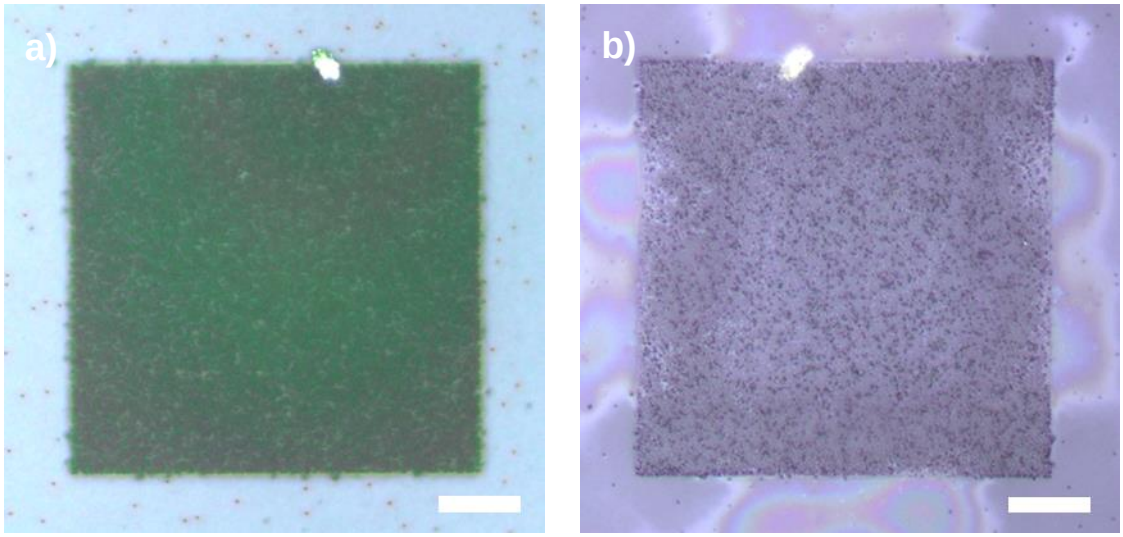

*Figure 4-4: Light microscope image of sample #1709, a GaAsP nw array, (**a**) before and (**b**) after a 77 minute HNA etch. Scale bars are 20 µm.*

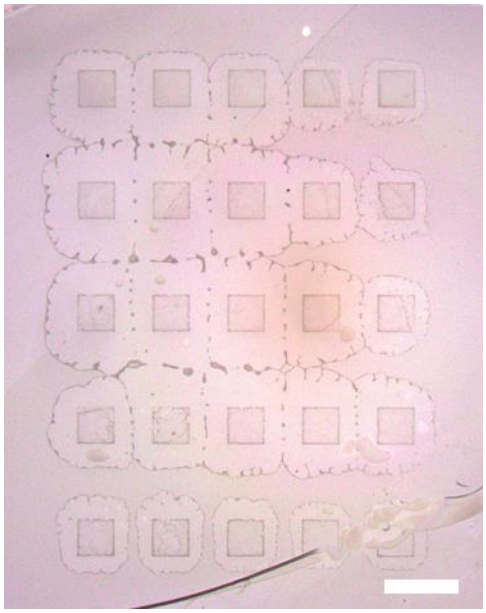

Figure 4-5: Light microscope image of sample #1677, showing a series of GaP nw arrays after substrate removal by HNA etching. Scale bar is 200 µm.

The integrity of the nw arrays is difficult to tell from light microscopy alone. The arrays in both Figure 4-3 and Figure 4-4 show good contrast following the HNA etch procedure. On the other hand, the GaP nw arrays in Figure 4-5, seem to have been completely etched away. This removal is evidenced by the 'cloudy' outline surrounding each array, indicating the etchant has penetrated through the nws and made its way in between the BCB and epoxy layers. Note that this outline was not present in the GaAs and GaAsP samples. Thus, further characterization is required to investigate these samples. An SEM image of the GaAsP nw sample is shown below in Figure 4-6.

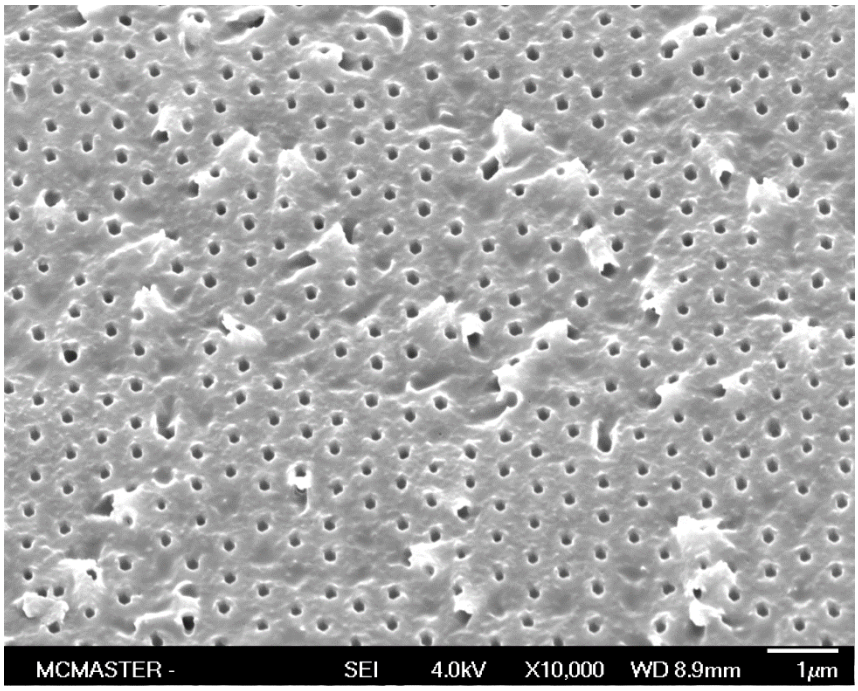

Figure 4-6: 30° tilted SEM image of the GaAsP nw array shown in Figure 4-4. The material is BCB, with holes evident where the nws sat prior to substrate removal.

The SEM shows empty holes in the BCB layer where the nw would have sat before the etching procedure, indicating the nws were etched away by the HNA. However, as described in Section 2.3.1, the nw growth is initially seeded by a GaP segment, before transitioning to either GaAs or GaAsP core growth. It is possible that the GaP segment at the base of the wire was etched away, leaving the remaining GaAs or GaAsP segment buried within the BCB. Photoluminescence was therefore attempted on the etched sample to detect the presence of any buried nws. Unfortunately, no appreciable signal was measured, further suggesting that the nws had been etched away during substrate removal. This is in contrast to the strong photoluminescence signal measured from the unetched GaAsP nws (outlined in more detail in Section 6.4.4).

However, one of the nw arrays, in particular, of sample #1709 showed different colouration under light microscopy and was investigated further. The backscattered electron (BSE) detector of the SEM was used to obtain compositional information from the sample, as shown below in Figure 4-7. In contrast to the more common SEI mode, described in Section 3.3, BSE imaging captures high energy electrons from the incident electron beam which have been elastically scattered from the sample [24]. Material with a higher atomic number (i.e. gallium, arsenic, and phosphorous) will be more likely to produce BSEs than that of a lower atomic number (i.e. hydrogen and carbon) and will appear brighter in the resulting image. The bright spots in Figure 4-7 indicate the presence of GaAsP nws, in contrast to the hydrocarbon composition of BCB.

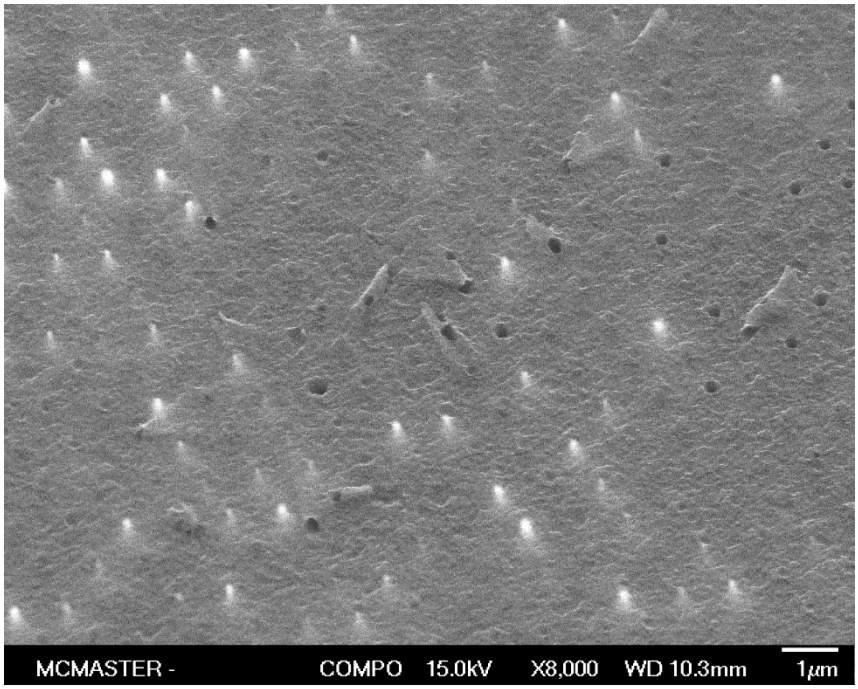

Figure 4-7: 30° tilted SEM image of one of the nw arrays of sample #1709, following substrate removal. The BSE detector was used to indicate compositional variation across the sample. The bright spots are attributed to the tips of GaAsP nws embedded in BCB.

The different colouration of the nw array, noted above, was only present in one of the twenty-five arrays in the sample. For the remaining arrays, in the absence of nws, the contrast seen in the post-etch light microscope images may be due to the etching process itself. It is possible that the etchant was not fully washed away following substrate removal and was stuck in the holes of the BCB (where the nws initially sat), causing the discolouration. Alternatively, the darker shade could be attributed to residue from the dissolution of the black etching wax.

Overall, the efficacy of the etching was inconclusive and no absorptance measurements were ultimately taken. The etching procedure would need to be refined to ensure a cleaner and more reproducible result for any further characterization work to be done. The elimination of any contaminants or residue is crucial for optical characterization, in particular. While it initially seems the HNA etch method is not suitable for GaP nws, further exploration on GaAs and GaAsP nw arrays may be warranted. However, an alternative method of substrate removal is suggested in Section 7.2.1, which would be preferred to the HNA etching method described herein.

5 Electrical Characterization of Transparent ITO Front Contacts

5.1 Introduction

The performance of any PV device relies on being able to achieve good electrical contact to the p- and n-regions of the cell. For the nw devices described in this thesis, the rear contact is applied by sputtering aluminum on the p-doped silicon <111> substrate, as outlined in Section 2.5. As there are no optical considerations to take into account for the rear contact, this is a relatively straightforward procedure and achieving good electrical contact is well documented [38,39].

On the other hand, applying the front contact to a nw solar cell can be challenging for several reasons. The primary issue is that the front contact must be designed such that it does not prevent light from reaching the active region of the cell. Other complications for nw devices, in particular, include a non-planar surface (caused by both nws protruding out of the BCB layer and a rough BCB surface following RIE etch-back) and effective removal of the passivation layer on the nw tip (in order to contact the n-shell directly). With a much more complicated application of the transparent front contact layer (ITO, in this case), it is important to be able to characterize the quality of the contact to design and fabricate the best possible PV device.

The two properties of interest of the ITO layer are the transparency and the sheet resistance of the film. Both of these properties are inversely proportional to film thickness, but since both a high transparency and low sheet resistance are

desired, an optimal thickness must be chosen to provide the best device performance.

Measuring the transparency of the film cannot be done *in situ*, since the film is deposited on an opaque substrate (though it would be possible to investigate this alongside a substrate removal experiment, as in Chapter 4). Instead, a 'witness' sample is prepared alongside the nw device and characterized independently, per Section 3.6. This method can also be used to measure sheet resistance [21], but there is some uncertainty in how well this serves as a proxy for the actual sheet resistance of the sample. SEM images of an ITO film deposited on a quartz slide compared to etched BCB on a silicon substrate are shown in Figure 5-1.

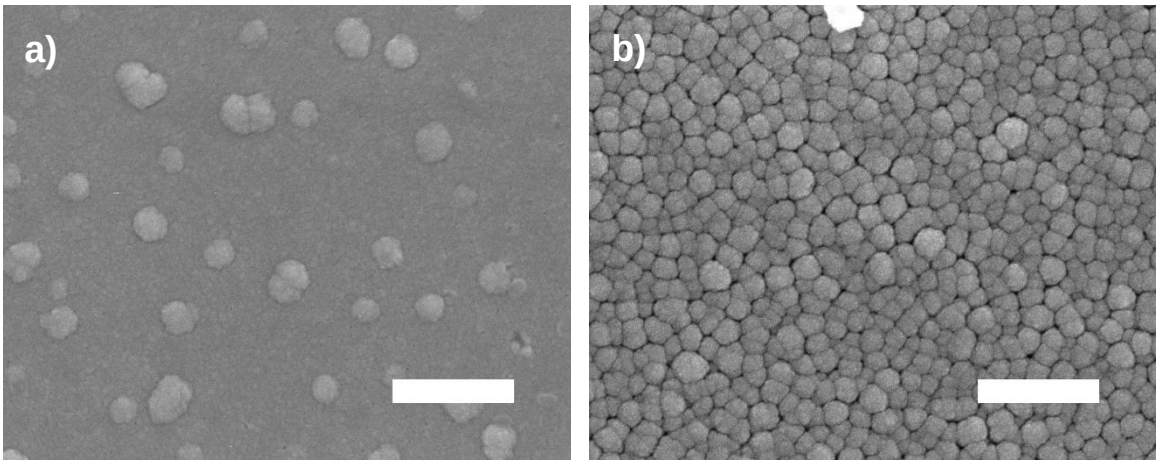

*Figure 5-1: SEM images showing the film quality of (**a**) sample F2 – 250nm of ITO deposited on a quartz substrate; and (**b**) sample F7 – 250nm of ITO deposited on etched BCB on a silicon substrate. Scale bars are 500 nm.*

It is clear that the ITO film deposited on the quartz slide is much smoother, on a nano-scale, than the same film deposited on the etched-BCB-on-silicon substrate. Therefore, in order to more accurately characterize the sheet resistance of the ITO contact of a nw device, a more representative proxy sample must be prepared. Ideally the sheet resistance measurement would be taken of an ITO film deposited on an array of undoped nws after planarization with BCB and RIE per Section 2.4.

Samples for this project were initially prepared without nw arrays for simplicity. Once an accurate and reliable method for characterizing sheet resistance has been achieved, new samples would be prepared, with the nw array included, to observe any differences.

5.2 Experimental approach

Sample substrates (without nw arrays) were prepared following the same processing steps outlined in Section 2.4, and ITO films, on the order of 1 cm^2, were deposited and annealed, as described in Sections 2.5 and 2.6. Note that annealing the sample is required to reduce the sheet resistance of the ITO film to an acceptable level [40]. However, the ITO cracked during the annealing process, as seen in Figure 5-2, preventing any sheet resistance measurements from being taken. This has been reported previously and is caused by the large difference in

the thermal expansion coefficients of BCB and ITO (42×10^{-6} K^{-1} and 8.5×10^{-6} K^{-1}, respectively) [31].

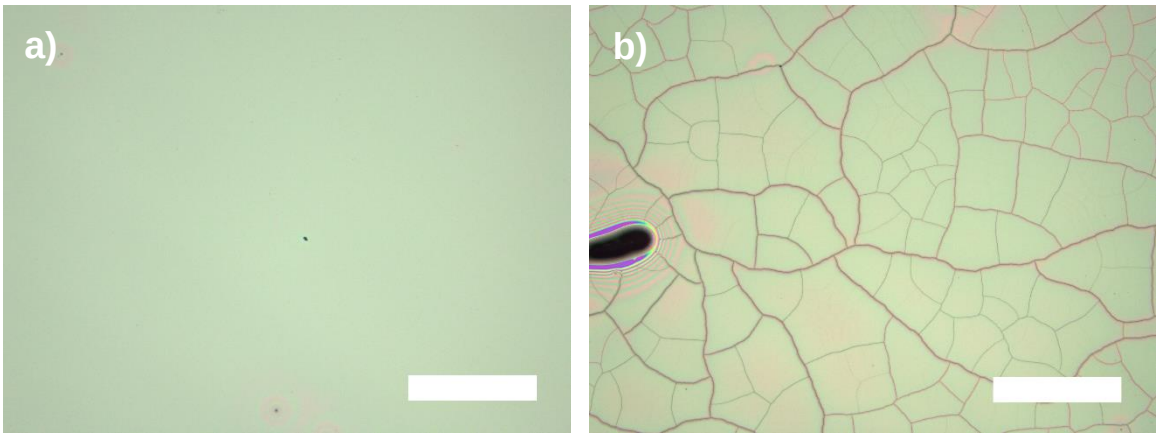

*Figure 5-2: Light microscope images of sample G6 (**a**) before and (**b**) after annealing at 400°C for 1 minute. The sample consisted of 250 nm of ITO deposited on BCB (following RIE etch-back) on a silicon <111> substrate. Scale bars are 500 µm.*

To obtain uncracked films after annealing, additional sample substrates were prepared and smaller square ITO pads of various sizes were applied, using standard photolithography techniques. It was found that pads with side length less than 200 µm remained uncracked following the annealing process; these smaller pads were then processed for sheet resistance measurements. This threshold for cracking is consistent with the nw devices fabricated throughout this thesis – the width of the ITO contact fingers as shown in Figure 2-7, for example, are 150 µm

and cracking is not observed. It was noted that the inclusion of a thin layer of indium did not prevent ITO cracking on etched BCB samples (compared to previously reported results on unetched BCB [31]).

Unfortunately, using ITO pads with side length less than 200 μm does not allow for the use of the in-line four point probe set up as described in Section 3.4, since the probe spacing is 1 mm. Instead the 'van der Pauw' technique [41] is employed by applying Ni/Ge/Au contact pads on the corners of the ITO square and probing these pads individually, as shown below in Figure 5-3. The contacts are applied using standard photolithography techniques and electron beam evaporation. The Ni/Ge/Au contacts are highly conductive and are assumed to not contribute substantially to the ITO sheet resistance measurement (with gold being approximately 40 times more conductive than ITO [42,43]).

In this arrangement, a current is sourced through one pair of adjacent contact pads and the voltage across the other two pads is measured. A resistance measurement for a particular probe arrangement is calculated using Ohm's Law [41], as in Equation 5-1:

$$R_{AB,CD} = \frac{V_{CD}}{I_{AB}} \tag{5-1}$$

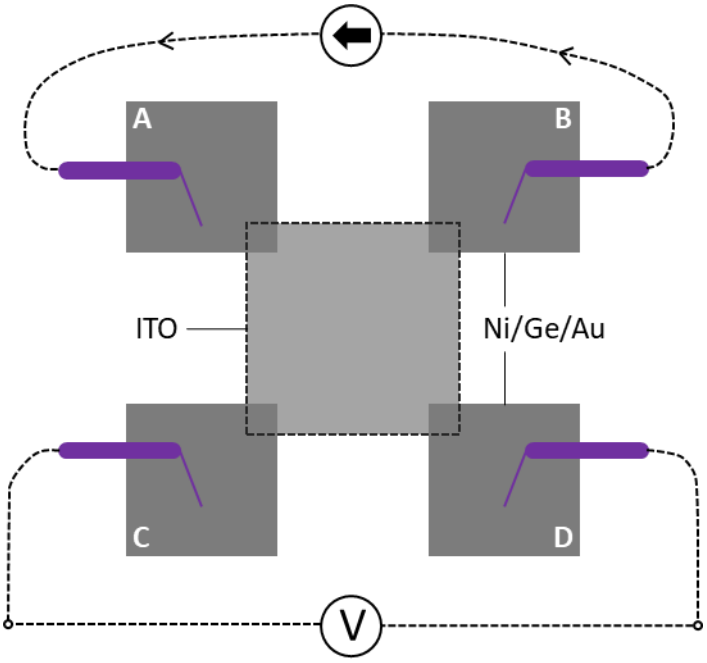

Figure 5-3: Schematic showing Ni/Ge/Au contact placement, in a square van der Pauw arrangement, for taking sheet resistance measurements of ITO pads. The current is sourced through the two upper pads (A–B) and the voltage across the two bottom pads (C–D) is recorded.

The measurements are repeated by sourcing the current through each pair of adjacent contacts (and measuring the voltage across the remaining contacts) to account for any asymmetries in the sample. In the case where all resistance measurements are equivalent, the calculation for sheet resistance reduces to the same formula as Equation 3-4 [41].

5.3 Subsequent challenges

During characterization of the first van der Pauw sample, the measurements yielded an open circuit. Further inspection by SEM revealed that the ITO layer curled up around the edges during processing, as seen in Figure 5-4. This resulted in a physical gap between the ITO and Ni/Ge/Au pads and ultimately in open circuit voltage readings.

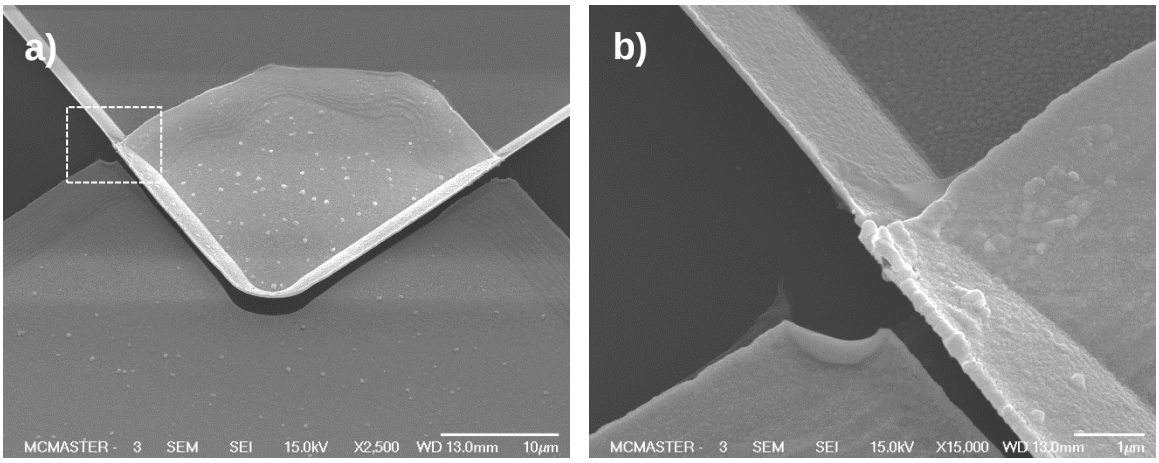

*Figure 5-4: 30° tilted SEM images of initial ITO test pads using a van der Pauw arrangement; (**a**) shows the central ITO pad on the top, with one of the Ni/Ge/Au contact pads on the bottom (overlapping in the middle of the image); (**b**) shows a magnified image of the dashed box – the ITO pad is seen to curl up along the edges, preventing electrical contact to the Ni/Ge/Au pad. Scale bars are 10 μm and 1 μm, respectively.*

Two different methods were investigated to address this problem. Initially, sonication was performed following ITO deposition. This successfully removed the 'wings' around the edge of the pad and allowed for a contiguous Ni/Ge/Au contact pad to be deposited on each of the corners. Alternatively, a 'clover-leaf' ITO pad was deposited, instead of a square pad, with the four Ni/Ge/Au contacts completely covering each 'leaf' of the ITO, as seen in Figure 5-5. This negates the effect of any wings around the edge of the ITO. However, because the contact area to the ITO is much larger in this configuration, additional consideration must be made to ensure accurate sheet resistance calculations are made [41].

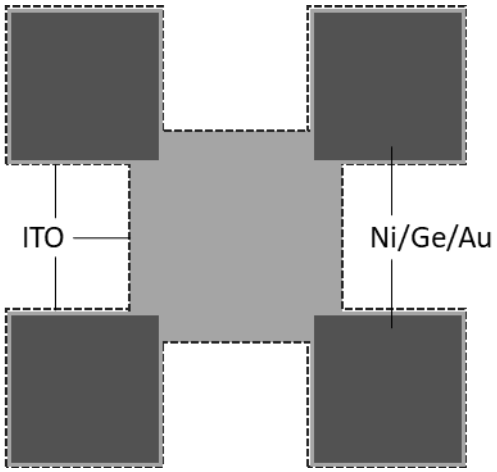

Figure 5-5: Schematic of ITO contact scheme in 'clover-leaf' configuration. The ITO layer extends underneath the Ni/Ge/Au contact pads.

Ultimately, further problems with characterization arose with the ITO cracking during testing (compared to the previously addressed issue of cracking

during annealing). This is likely attributed to high current densities in the sample, so alternate ITO and Ni/Ge/Au pad configurations and probing methods are still being explored to achieve reliable sheet resistance measurements. Although attempts to electrically characterize transparent ITO front contacts were made, a number of issues arose that precluded a full evaluation. Further research in this area is required, but is outside the scope of this thesis.

6 Fabrication of GaAsP Nanowire-on-Silicon Tandem Cell

6.1 Introduction

Due to bandgap limitations in semiconductors, only a portion of the sun's power spectrum is available for conversion into electrical energy. Incident photons with energy below the bandgap of a single junction cell will pass through the cell unabsorbed, and photons with excess energy above the bandgap will contribute to thermal losses. For example, just considering these spectral losses, a single junction silicon cell can only harness a maximum of 49% of the sun's power, before considering any recombination or other loss mechanisms – this is referred to as the 'ultimate efficiency', as described by Shockley and Queisser [44].

Assuming perfect quantum efficiency, each photon with energy above the bandgap will generate one EHP within the device and each EHP can be extracted with a maximum energy equal to the bandgap of the material. The incident solar spectral irradiation density is given by $P_{incident}(\lambda)$ (in units of W/m^2/nm). The spectral irradiation density in terms of photon flux (# photons/m^2/nm) is obtained by dividing $P_{incident}(\lambda)$ by the energy of a single photon ($E = \frac{hc}{\lambda}$). The maximum power generated by the cell is then proportional to this irradiance multiplied by the energy of the bandgap ($E_g = \frac{hc}{\lambda_g}$) – i.e. $P_{incident}(\lambda)\frac{\lambda}{\lambda_g}$. This can be converted to a power density (in units of W/m^2) by integrating $P(\lambda)$ over all wavelengths. However, since photons with energy below the bandgap are not absorbed, the limits of integration can be adjusted to only include wavelengths below λ_g. Finally

the ‘ultimate efficiency’ can be calculated by dividing the generated power density by the incident power density, using Equation 6-1:

$$u = \frac{\int_0^{\lambda g} P_{incident}\ (\lambda)\frac{\lambda}{\lambda_g} d\lambda}{\int_0^{\infty} P_{incident}\ (\lambda) d\lambda} \tag{6-1}$$

Using the AM1.5G spectral irradiance and a 1.12 eV bandgap (1107 nm) for silicon yields an ‘ultimate efficiency’ of 49%, as noted above. This is visualized in Figure 6-1.

By using a tandem cell structure, higher energy photons can be absorbed and converted more efficiently in the upper junction, letting lower energy photons pass to the next junction before being absorbed. The bandgaps can be selected to minimize these overall spectral losses. The equation above can be applied to two separate junctions, where λ_{g1} and λ_{g2} correspond to the bandgap of the upper and lower junction, respectively:

$$u = \frac{\int_0^{\lambda_{g1}} P_{incident}\ (\lambda)\frac{\lambda}{\lambda_{g1}} d\lambda + \int_{\lambda_{g1}}^{\lambda_{g2}} P_{incident}\ (\lambda)\frac{\lambda}{\lambda_{g2}} d\lambda}{\int_0^{\infty} P_{incident}\ (\lambda) d\lambda} \tag{6-2}$$

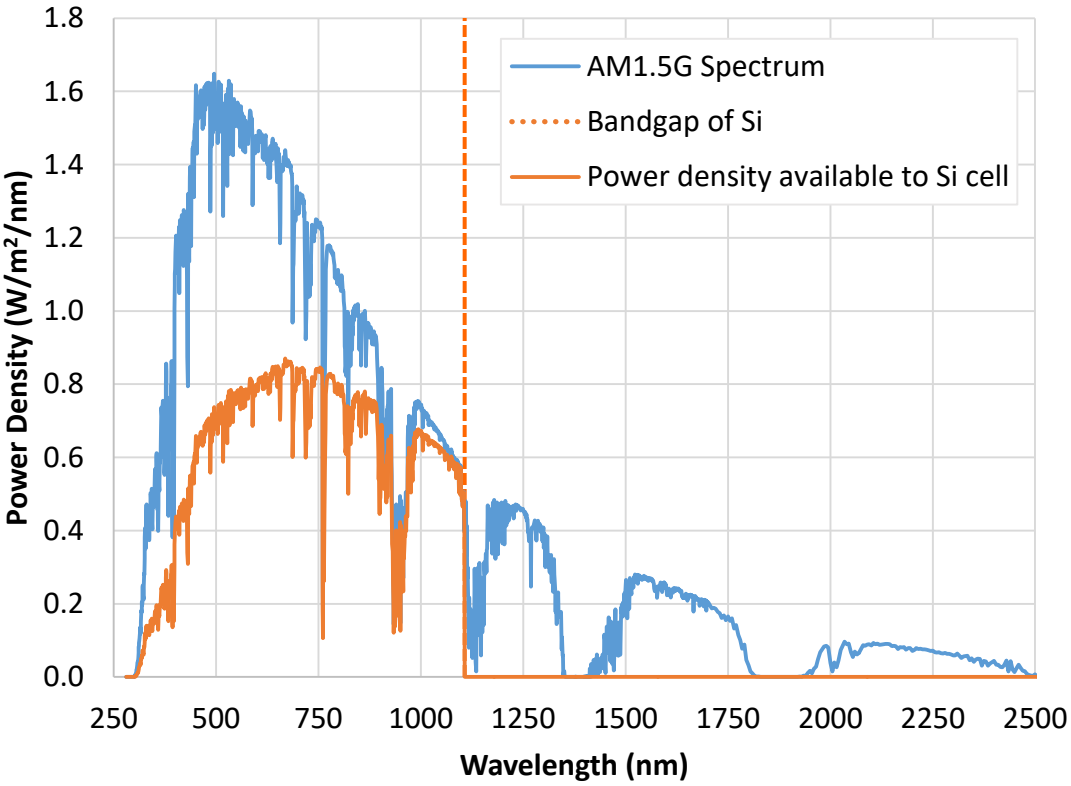

Figure 6-1: Solar energy available for conversion to electrical energy, using a single junction silicon cell. The numerator of Equation 6-1 is equal to the area under the orange curve and the denominator is equal to the area under the blue curve.

Simply considering a tandem structure with a silicon substrate as the lower junction, the optimal bandgap for the upper junction is found to be 1.81 eV, using the AM1.5G spectral irradiance.

However, in a series-connected multi-junction device, EHPs must be generated in each subcell simultaneously. The overall current output is limited by

the subcell generating the fewest EHPs. In an ideal structure, the current generated in each subcell would be equal. This is known as 'current-matching' and is dependent on the spectrum of light incident on each subcell [45].

The power density generated in each subcell individually (each term in the numerator of Equation 6-2) can be converted to a current density by multiplying by q and dividing by the bandgap energy. The current output of both subcells is then limited by the lower current density of the two subcells. To achieve current-matching, the bandgap for the upper junction is found to be 1.72 eV (720 nm), assuming silicon for the lower junction. This results in 62% of the sun's power available for conversion by considering the combined structure of the tandem cell, as demonstrated in Figure 6-2.

By employing a ternary $GaAs_{1-x}P_x$ composition for the upper junction, a 1.72 eV bandgap can be achieved by optimizing the phosphorous fraction, x, as calculated in Section 6.2.1. Of course, utilizing a nw structure allows the upper subcell to be mismatched to the lattice of the silicon substrate while simultaneously taking advantage of the other unique properties of nw arrays [1].

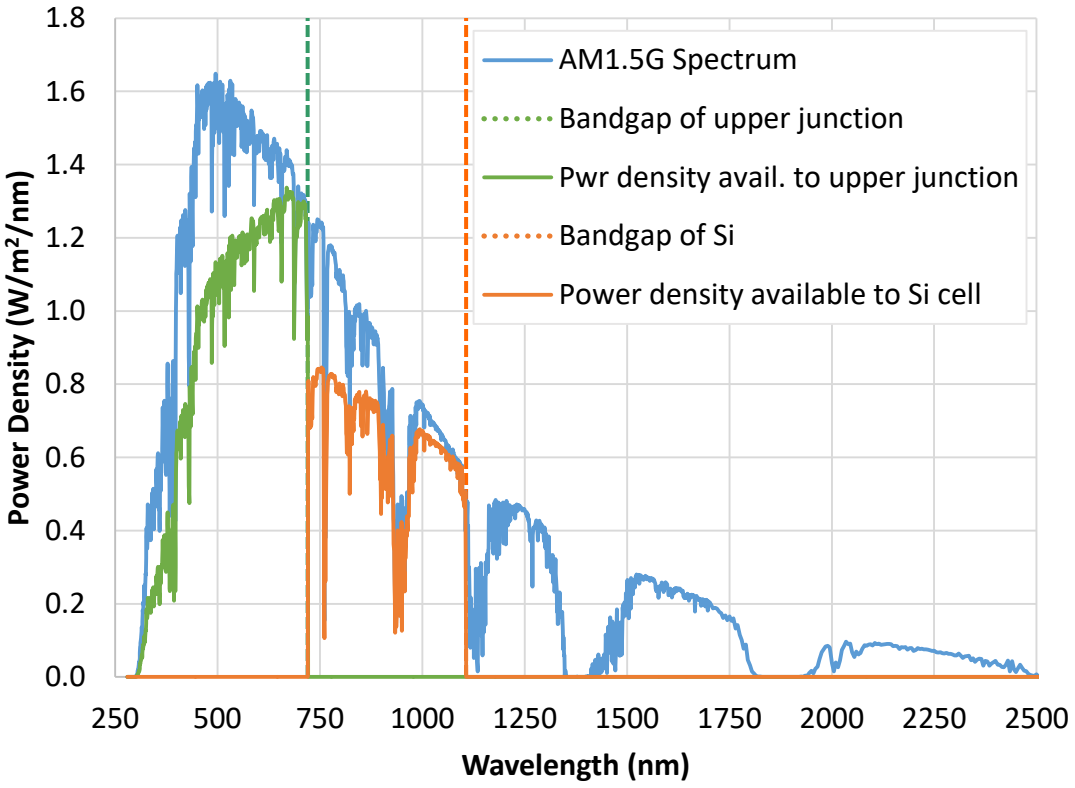

Figure 6-2: Solar energy available for conversion to electrical energy, using a tandem cell (with silicon substrate). The first and second terms in the numerator of Equation 6-2 are equal to the area under the green and orange curves, respectively; and the denominator is equal to the area under the blue curve.

6.2 Experimental approach

The device processing procedure for single junction nw cells on silicon was adapted for a tandem cell design. Initially, GaAs nw arrays were grown on the silicon cell substrates to achieve preliminary results. After refining the device

processing procedure, GaAsP nw samples (with an optimized bandgap) were grown and processed (Section 6.3). To properly characterize the two subcells of the tandem device, single junction cells of GaAsP and silicon were processed and characterized independently (Sections 6.4 and 6.5). Unless otherwise noted, both electrical and optical characterization was done using the methods described in Chapter 3.

6.2.1 GaAsP composition

Parameters from Vurgaftman et al. can be used to determine the necessary composition to achieve the desired bandgap of 1.72 eV for the upper nw subcell. The bandgap of a ternary semiconductor, as a function of alloy composition, can be approximated by Equation 6-3 [4]:

$$E_{gA_{1-x}B_x} = (1-x)E_{gA} + xE_{gB} - x(1-x)C \tag{6-3}$$

Vurgaftman recommends a bowing parameter, C, of 0.19 eV for $GaAs_{1-x}P_x$. Using 1.42 eV and 2.78 eV as the direct bandgap energies for GaAs and GaP, respectively [4], corresponds to $x = 0.25$ in order to achieve a 1.72 eV direct bandgap (the Γ-valley remains the minimum for $x < 0.45$).

During $GaAs_{1-x}P_x$ nw growth, the value of x can be adjusted to yield this nominal composition based on calibration growths. After MBE growth, the actual

bandgap of the nw array can be characterized by photoluminescence (as described in Section 3.5).

6.2.2 Sample layout

The EBL pattern applied to each sample includes 75 individual nw arrays, or ‘pads’, which are each 100 µm x 100 µm, as shown in Figure 6-3. There are three identical sets of pads (left / middle / right), referred to as L, M, R (only a single set of pads is shown in Figure 6-3). Each of the three sets has five rows of pads with a different nw pitch (spacing) on each row, ranging from 360 nm to 1000 nm (measured from the centre of each nw), referred to as P0360, P0440, P0520, P0600, and P1000. Finally, each row has five columns, each containing a single pad with a different dose applied during EBL, referred to as D1, D2, D3, D4, and D5. EBL dosages range from 10 mC/cm^2 for the D1 pads to 100 mC/cm^2 for the D5 pads. For example, a cell on the left set of pads, on the second row, in the third column would be referred to as ‘LP0440D3’.

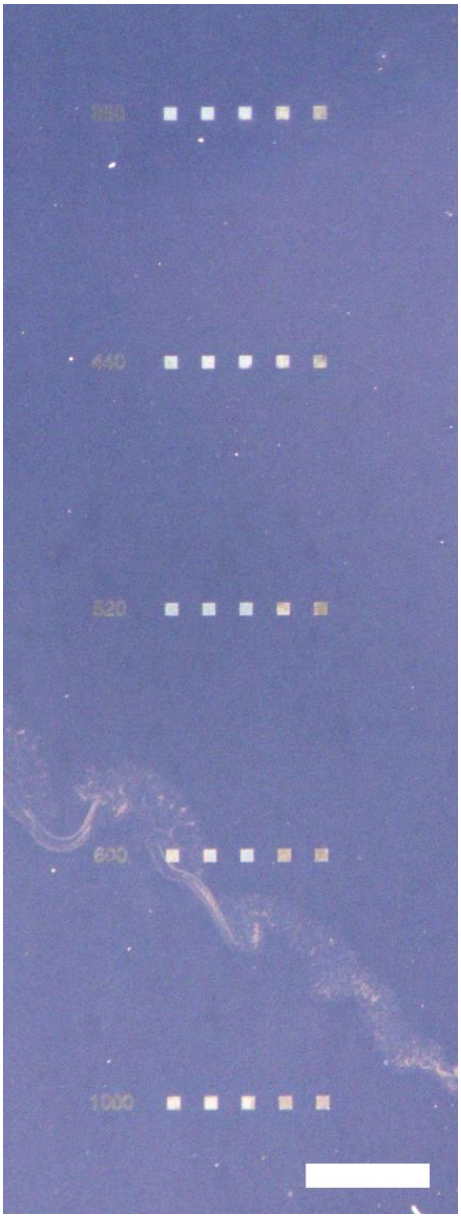

Figure 6-3: Light microscope image of sample #1849 after nw growth, showing a single column of the EBL pattern; this column is repeated three times per wafer to produce a total of 75 separate 100 µm x 100 µm nw pads (white squares). Scale bar is 1 mm.

Different doses are included for any given nw pitch to accommodate deviations in processing leading up to and including nw growth. For example, small adjustments of RIE or BHF etching can have large implications for the resulting nw yield. Using a series of doses for the same pitch typically results in at least two or three columns with 'good' nw yield (i.e. over 80%).

6.3 GaAsP nanowire-on-silicon tandem junction cell

6.3.1 Fabrication

The substrates that were used for this project were provided by *The Institute for Solar Energy Research Hamelin* (ISFH) and started as 4" diameter <111> p-type (boron-doped) double-side polished float-zone silicon wafers. The n-type emitter layer was applied to the front side using $POCl_3$ diffusion, followed by the growth of a thermal oxide (38 nm thick on the n-type front and 30 nm on the p-type rear). The total wafer thickness was approximately 525 µm, with a junction depth (emitter thickness) of 650 nm. Further detail can be found in the Appendix under Wafer Specifications.

The fabrication of the tandem junction cell closely followed the general procedure outlined in Chapter 2, with a few adjustments. Firstly, because of the thermal oxide on both surfaces of the silicon wafer provided by ISFH, there was no need to deposit an additional oxide for front-side processing. However, the oxide layer of the rear surface needed to be removed prior to applying the blanket rear

contact. Following the application of the front contact, the top of the sample was covered in photoresist and the sample was etched in BHF to strip the rear oxide. After sputtering aluminum on the back of the sample, the sample was cleaned in acetone and IPA to remove the photoresist on the front.

The other change to the standard processing steps was related to the wafer size. The MBE system used for nw growth does not have a 'pie-shaped' holder for 4" wafers. Instead, the holder was designed for a 'quarter-wafer' (originally intended for <100> crystal orientation wafers). The <111> oriented ISFH wafers needed to be diced into quarters (against the natural cleaving planes of the crystal) instead of cleaved.

Following the initial CF_4 RIE, the entire wafer was mounted face-down on dicing tape (in order to protect the EBL pattern) and diced into quarters. Following dicing, the EBL resist was stripped and the sample was cleaned, as described in Section 2.2.2. Parameters for the subsequent nw growth can be found in Table 6-1.

Table 6-1: MBE growth sheet used for sample #1865.

Segment	Time (min)	Temperature (°C)	Doping (cm^{-3})	Growth Rate (µm/h)	V/III Flux Ratio
Start					
GaP	5	600	Be @ $5x10^{18}$	0.125	2
Ramp from GaP to $GaAs_{0.75}P_{0.25}$	5	600	Be @ $5x10^{18}$	0.125	2
$GaAs_{0.75}P_{0.25}$	40	600	Be @ $5x10^{18}$	0.125	2
$As_{0.75}P_{0.25}$	20	600	-	-	0.4
Cool under $As_{0.75}P_{0.25}$	-	500	-	-	Keep same flow to consume Ga seed
$GaAs_{0.75}P_{0.25}$	17	500	-	1	2
$GaAs_{0.75}P_{0.25}$	12.5	500	Te @ $2x10^{18}$	1	2
$GaAs_{0.75}P_{0.25}$	3.5	500	Te @ $8x10^{18}$	1	2
$Al_{0.52}In_{0.48}P$	30	420	-	0.25	8
End					

Figure 6-4 shows an SEM image of a GaAsP nw sample immediately following MBE growth. Figure 6-5 and Figure 6-6 show SEM images of the same sample following planarization in BCB and subsequent etching by both RIE and HCl, respectively. After these processing steps the sample is ready for contacting. Note that these SEM images are of sample #1874, which used the same nw growth parameters as sample #1865 (the tandem cell characterized in Section 6.3). Sample #1874 (as described in Section 6.4) is a single junction GaAsP nw sample grown on a 3” p-type silicon wafer.

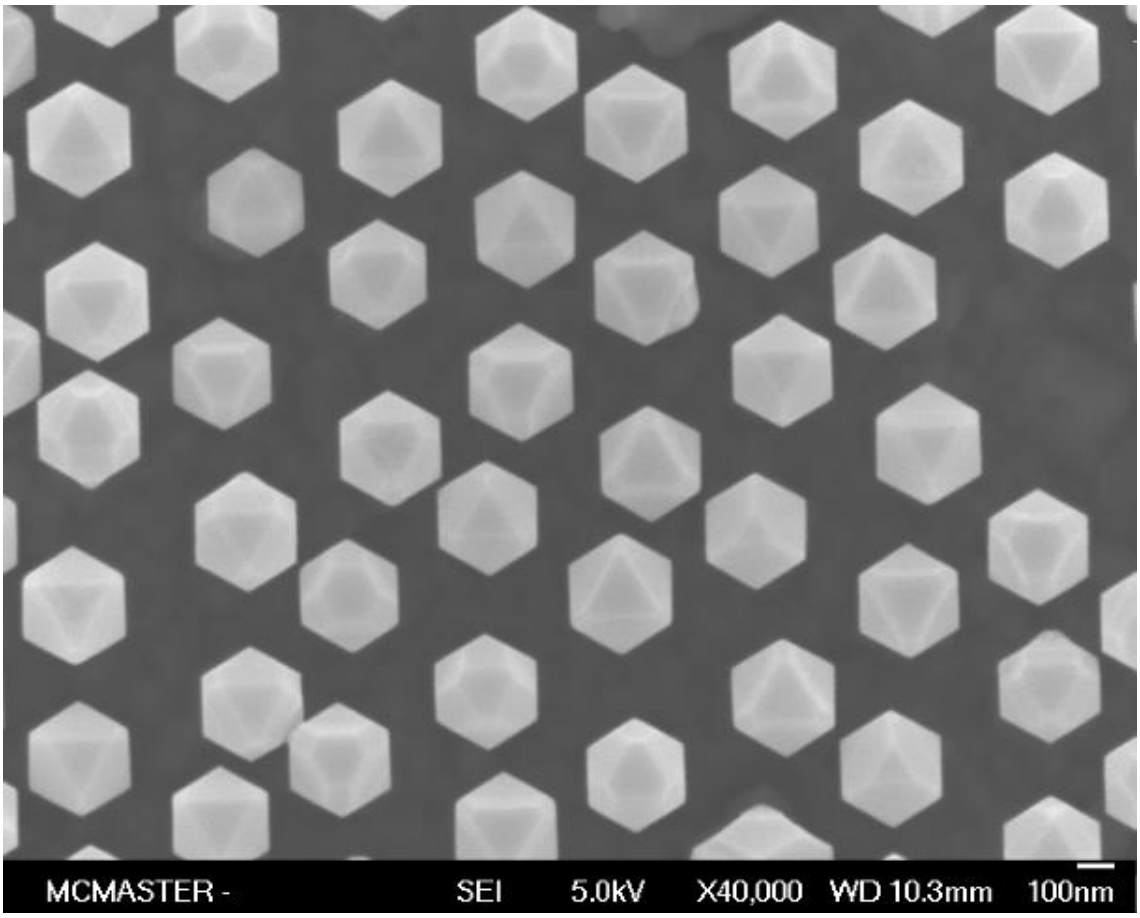

Figure 6-4: Plan view SEM image of sample #1874, pad MP0440D3, following GaAsP nw growth by MBE; the hexagonal structure of the GaAsP nws is clearly visible.

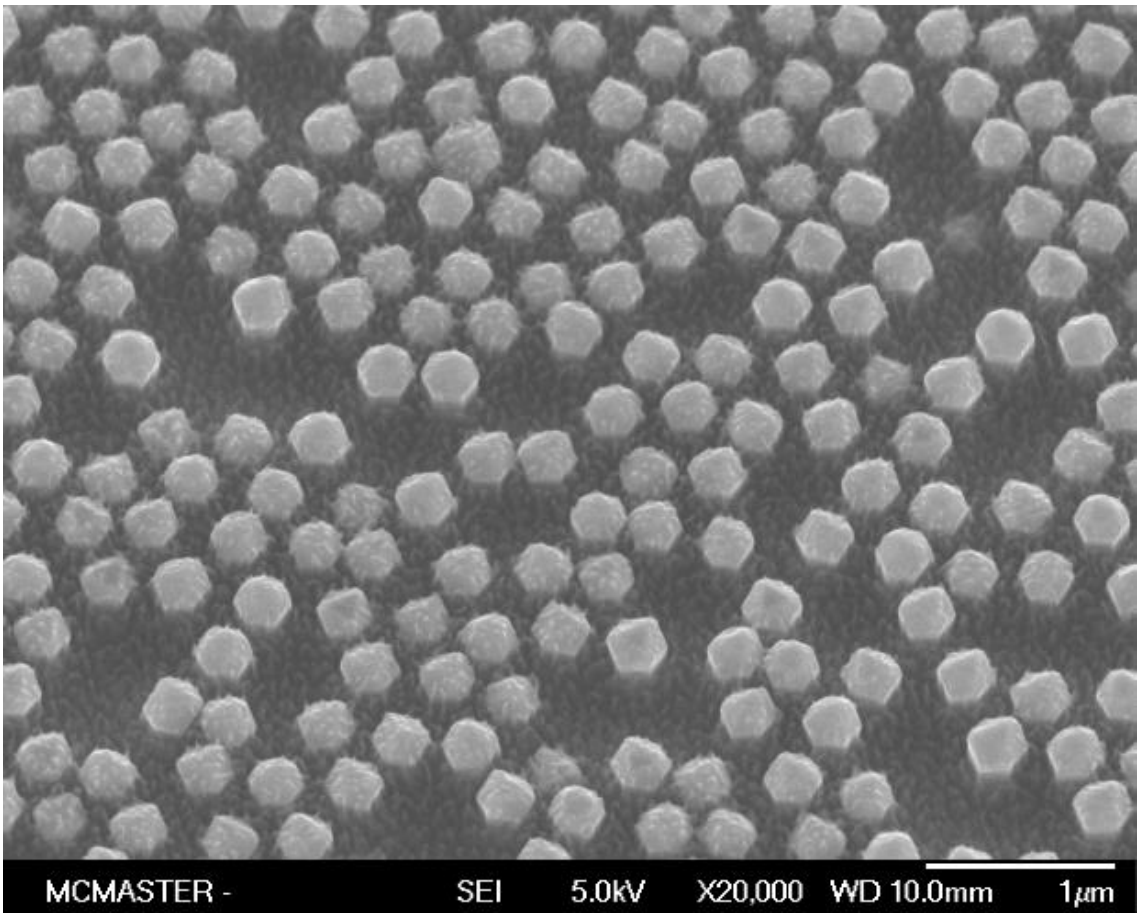

Figure 6-5: 30° tilted SEM image of sample #1874, pad MP0440D3, following planarization in BCB and 6 minutes of RIE; the tips of the GaAsP nws are seen protruding through the surface of the BCB.

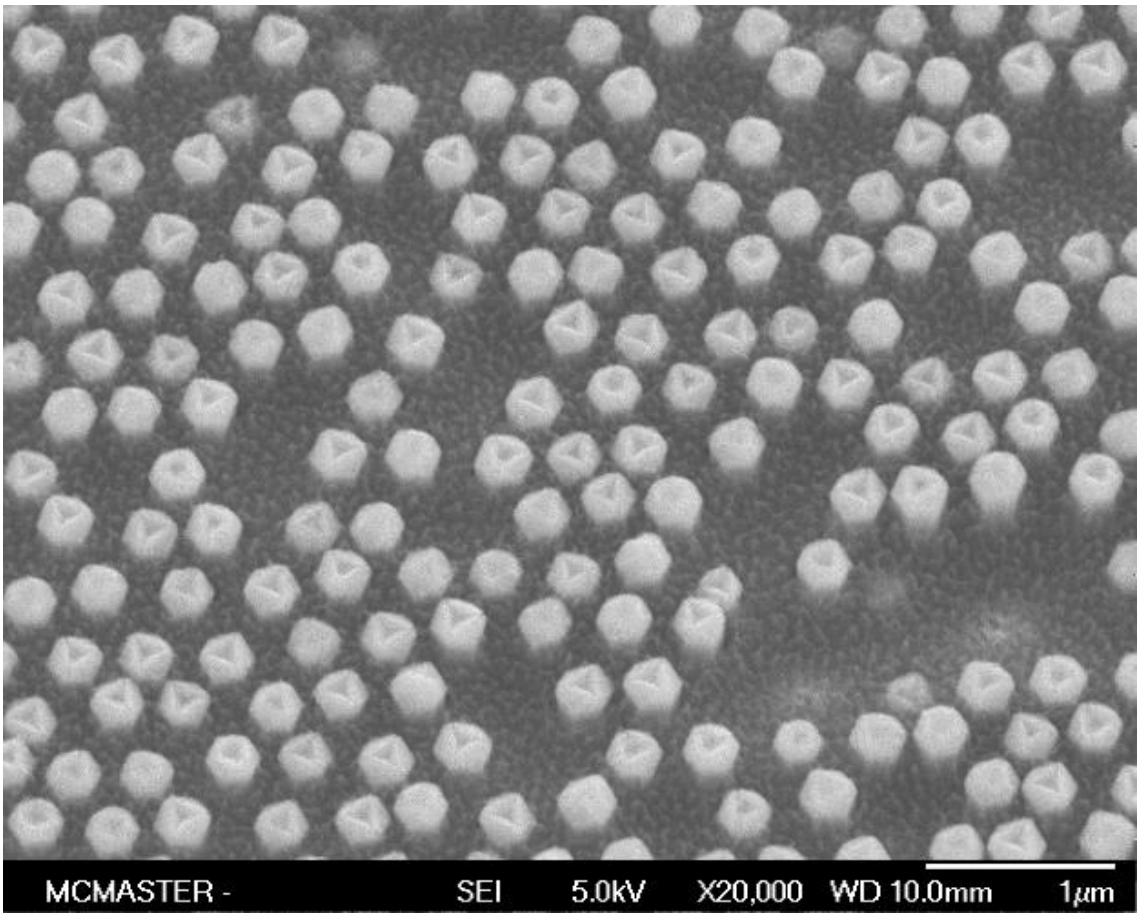

Figure 6-6: 30° tilted SEM image of sample #1874, pad MP0440D3, following a 45-second HCl wet etch; the AlInP passivation layer is removed from the tips of the GaAsP nws, as seen by the inverted triangular pyramid structure. The sample is ready for contacting.

6.3.2 Solar simulation

IV data recorded for a subset of pads on sample #1865 are presented below. The data was collected using the solar simulation methods detailed in Section 3.1. Figure 6-7 focuses on the 'fourth quadrant' (i.e. forward bias, reverse current) where solar cells operate, with the cell under AM1.5G illumination. By inspecting the data, the open circuit voltage (V_{oc}) and short circuit current density (J_{sc}) are found to be 1.16 V and 7.65 mA/cm^2, respectively. The total power output of the cell is dependent on the operating voltage; selecting the maximum power point of the IV curve (660 mV and 5.3 mA/cm^2, as indicated by the dashed lines in the accompanying figure) results in a fill factor of 39.6% and device efficiency of 3.51%.

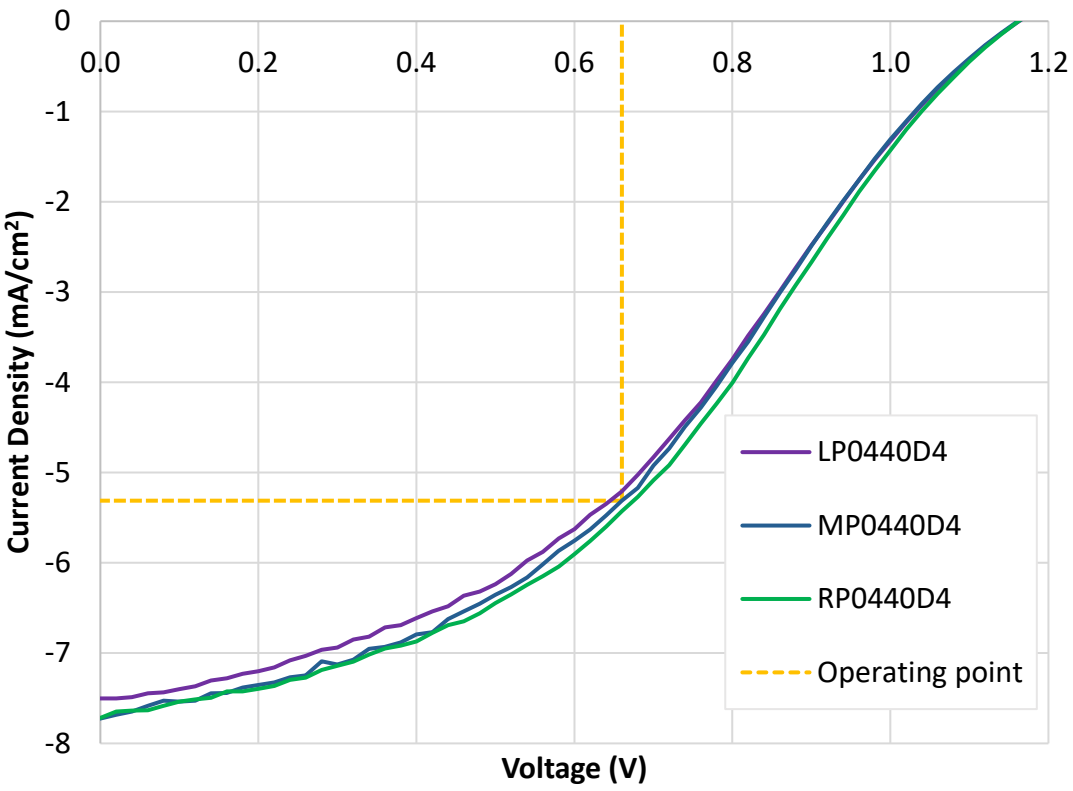

Figure 6-7: Light IV curves for each column of the P0440D4 pads from sample #1865. V_{oc}, J_{sc}, maximum power point, fill factor, and cell efficiency are all extracted from this data.

Figure 6-8 shows light and dark IV curve data for the full range of measurement on a semi-log plot.

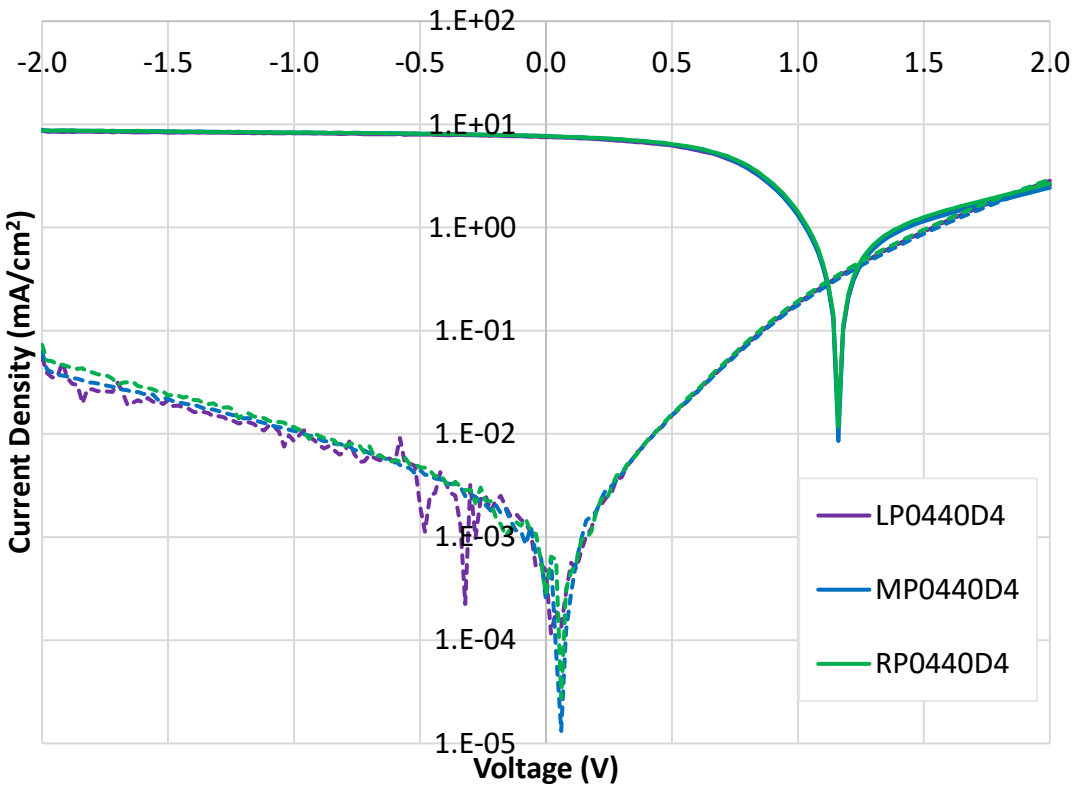

Figure 6-8: Light (solid lines) and dark (dashed lines) IV curves for each column of the P0440D4 pads from sample #1865.

6.3.3 EQE measurements

The general procedure for measuring quantum efficiency is described in Section 3.2. However, there are some unique challenges associated with measuring the EQE of multi-junction PV devices which must be considered.

Quantum efficiency measurements use monochromatic light to determine the spectral response of the device. But as the wavelength of the incident light

changes, the current-matching condition, described in Section 6.1, also changes. Consider measuring the EQE response of a GaAsP:Si tandem cell in the infrared region. Since the incident light is below the bandgap of GaAsP, there would be no absorption in the upper subcell, limiting the overall current output of the device to zero (despite the fact that the cell is absorbing infrared light in the lower subcell at these wavelengths and generating EHPs). Therefore, a 'bias' light is applied to illuminate one subcell while ensuring that the other subcell under monochromatic light is current-limiting the overall output of the device [45]. Thus, any response from the monochromatic light can be attributed directly to the subcell of interest. A schematic of the experimental set-up is shown in Figure 6-9.

Since an additional bias light is incident on the sample during testing, it is necessary to isolate the EHP generation due to the monochromatic light. This is done by inserting an optical chopper between the QTH lamp and monochromator and using a lock-in amplifier (LIA) to detect the signal [45].

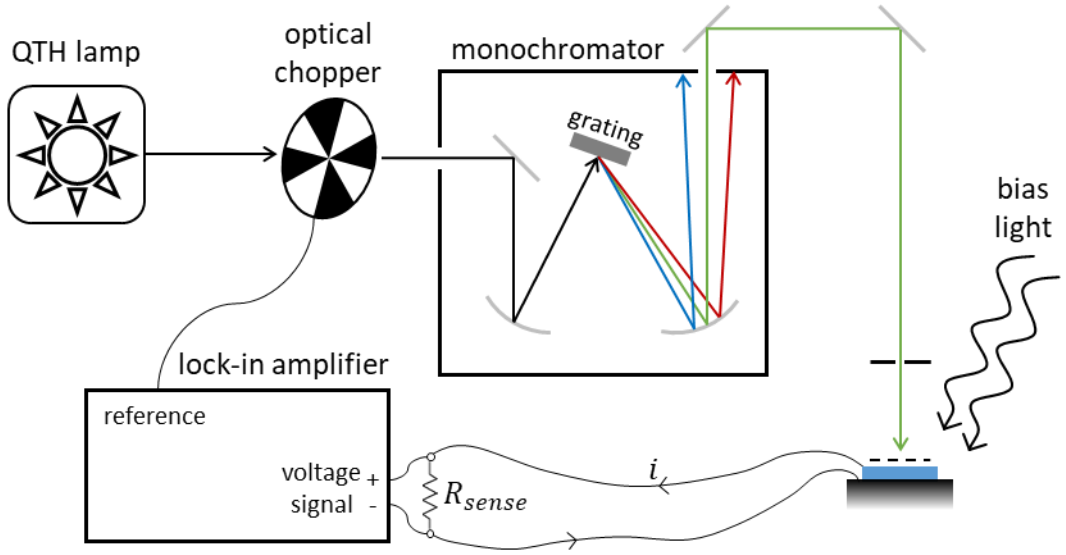

Figure 6-9: Experimental set-up for EQE measurements of tandem cell samples; the chopped monochromatic light passes through an aperture before illuminating the sample through a shadow mask; the resulting photocurrent is measured across a sensing resistor using a lock-in amplifier.

For testing of the upper nw subcell, a bias light is not necessary since the spot size of the monochromatic light is much larger than the nw pad itself. There is an excess EHP generation in the silicon cell from the surrounding area, thus the upper subcell is already current-limiting the device, as required. This is shown below in Figure 6-10 a).

On the other hand, testing of the lower subcell does require an external bias light. The bias light is selected to maximize absorption in the upper subcell to produce an excess of EHPs and ensure the lower subcell is current-limiting the

device. Additionally, to prevent EHP generation from the surrounding substrate from both the monochromatic light and bias light, a shadow mask is placed over the sample as shown in Figure 6-10 b).

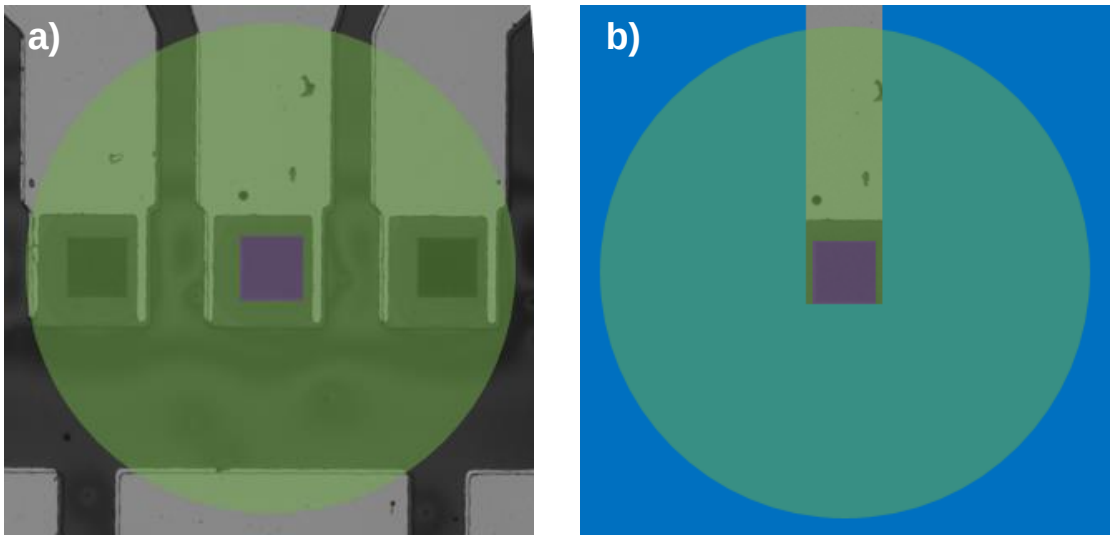

*Figure 6-10: Schematic showing illumination and EHP generation in each subcell. The green area indicates the incident light (either monochromatic or bias light) illuminating the nw pad (upper subcell, purple) and surrounding substrate (lower subcell); (**a**) without shadow mask, (**b**) with shadow mask (blue).*

Due to the device structure, it is virtually impossible to completely shadow the surrounding substrate. However, a good result can be achieved by masking three sides of the nw pad and letting the contact finger serve as a shadow mask for the fourth side (with a small portion unmasked, between the nw pad and contact finger). This was achieved by transferring a gold film to a piece of tape and cutting

a thin slit in the tape, to serve as the mask. The mask was manually placed over the sample during testing and adjusted to maximize coverage of the substrate. As this masking process was refined over successive measurements, the EQE response of the cell in the infrared region became apparent.

The response of a nw pad on sample #1865 is presented in Figure 6-11. A helium-neon (HeNe) laser, with a wavelength of 633 nm, was used to bias the device while measuring the EQE response of the lower subcell.

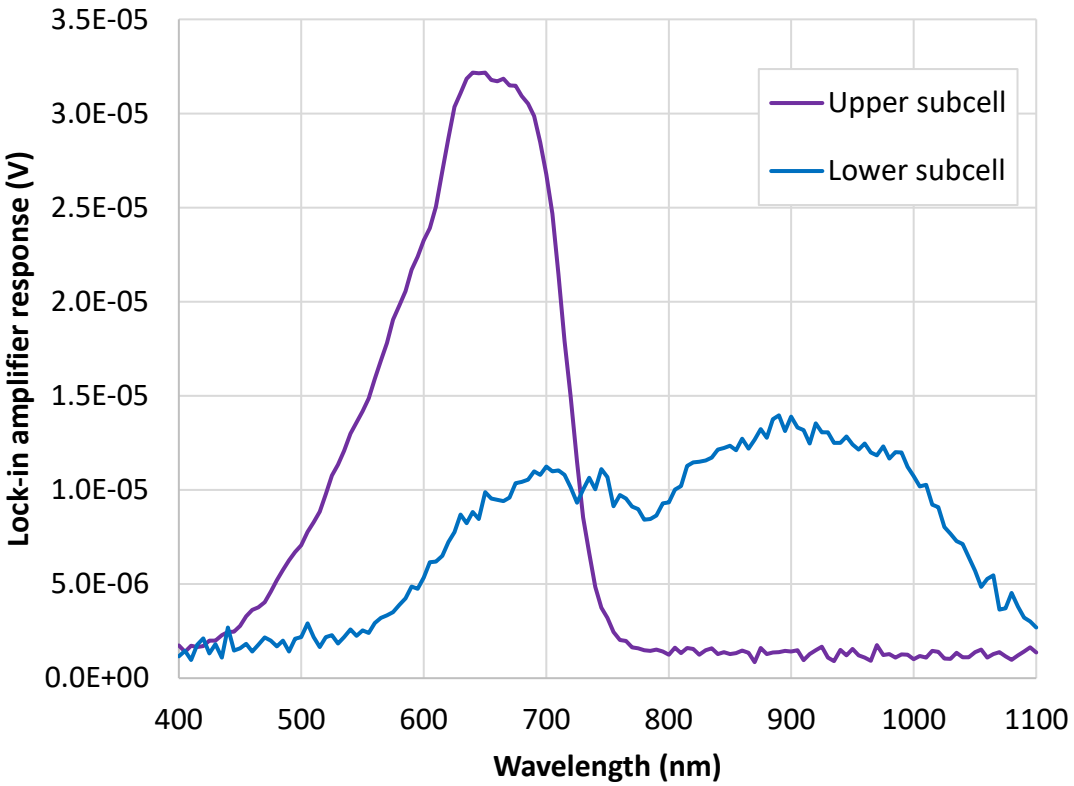

Figure 6-11: Response of sample #1865 MP0440D4 as measured with a LIA. The response of the lower subcell included the use of a bias light and shadow mask.

However, there are several steps which must be taken in order to convert the LIA response to an EQE response. Firstly, the number of photons incident on the sample must be calculated, as described in Section 3.2.

Secondly, the current (i.e. number of electrons) produced by the cell must be calculated. As shown in the schematic of the experimental set up, the LIA is actually measuring a voltage signal across a sensing resistor, so this must be converted to a current. The voltage across the resistor due to the HeNe bias light was measured to be 3.0 mV; and as seen in Figure 6-11, the peak voltage across the resistor due to the monochromatic light was only 32 μV. The combined effect of these voltages does not move the operation of the solar cell far from short-circuit conditions (based on the IV curves shown in Figure 6-8), so loading of the cell due to the inclusion of this sensing resistor was ignored.

Thirdly, the initial power meter measurement did not use the LIA or optical chopper, so the EQE response must be scaled to accommodate this difference. This is done by comparing two unbiased measurements on the same sample: the output current for unchopped light using a Keithley 2400 SourceMeter, and the voltage signal for chopped light using a SRS SR810 Lock-In Amplifier. The LIA voltage signal is converted to a current and multiplied by a scaling factor in order to match the current signal measured by the SourceMeter. This scaling factor is determined by minimizing the residual sum of squares between the scaled LIA response and the original SourceMeter measurement.

Finally, due to the difficulty associated with manually positioning the shadow mask to measure the lower subcell, a portion of the nw pad itself will invariably be masked as well. The EQE response can be scaled to accommodate these shadow losses. Again, the loss can be estimated by comparing two unbiased measurements on the same sample: with and without the shadow mask. With no bias light in place, the output signals will correspond to the upper subcell, but it is assumed that the shadow loss associated with the lower subcell measurements are equivalent.

Equation 3-1 is adjusted to include these factors, as shown below in Equation 6-4. Here $f_{chopper}$ corresponds to the scaling factor to accommodate the difference in input power between chopped and unchopped light, f_{mask} corresponds to the scaling factor associated with the shadow mask covering a portion of the nw pad, $v_{LIA}(\lambda)$ is the voltage signal measured by the LIA, R_{sense} is the resistance of the sensing resistor, and $\Phi(\lambda)$ is incident photon flux of the unchopped monochromatic light.

$$EQE(\lambda) = \frac{f_{chopper} * f_{mask} * \frac{v_{LIA}(\lambda)}{R_{sense} * q}}{\Phi(\lambda)} \tag{6-4}$$

Using Equation 6-4, the data in Figure 6-11 is converted to the EQE response shown in Figure 6-12.

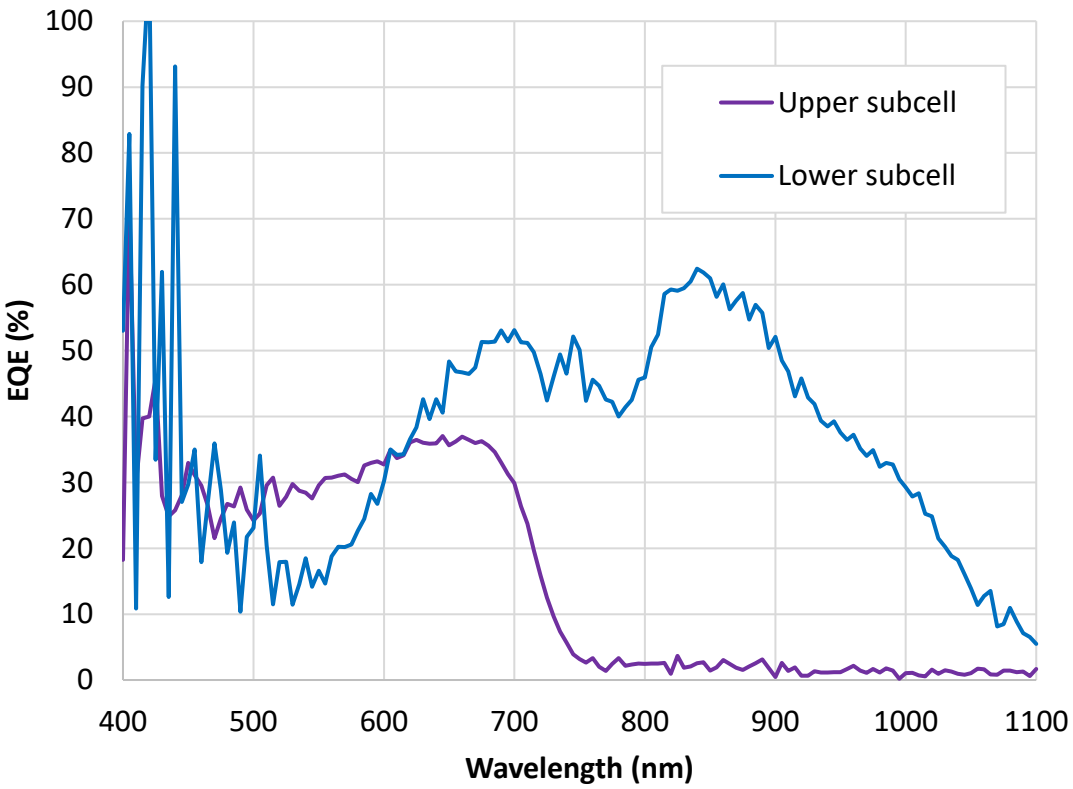

Figure 6-12: EQE response of sample #1865 MP0440D4.

As expected, the EQE response of the upper subcell falls off as the incident photon energy exceeds the bandgap of the nws (measured to be 724 nm in Section 6.3.4). These photons are transmitted through to the lower subcell to be absorbed in the silicon substrate (lower subcell). The response of this lower subcell peaks in the near infrared region and declines as the incident photon energy approaches the bandgap of silicon (1107 nm). This EQE measurement can be validated by integrating the product of the EQE and the AM1.5G spectrum and comparing to the short circuit current density measured by solar simulation, as per Equation 6-5:

$$J_{sc} = \frac{e}{hc}\int_0^{\infty} P_{AM1.5G}(\lambda) * \lambda * EQE(\lambda) d\lambda \quad (6\text{-}5)$$

Applying Equation 6-5 to the upper GaAsP and lower Si subcells results in current densities of 6.98 mA/cm^2 and 15.8 mA/cm^2, respectively. Since the overall output is limited by the subcell generating the lowest current, the overall short circuit current density should be the current generated in the upper subcell, which is comparable to 7.65 mA/cm^2, as determined from the IV characteristics in Figure 6-7. Discrepancies between the value measured during solar simulation and the value calculated by this equation can be attributed to differences between the IV and EQE set ups; for example, non-uniformity across the illumination area on the sample stage and variations of the xenon arc lamp spectrum compared to the standard AM1.5G spectrum used in Equation 6-5.

6.3.4 Photoluminescence

The bandgap of the GaAsP nw subcell can be estimated by photoluminescence, as described in Section 3.5. The room temperature photoluminescence spectra of the nw pads is shown in Figure 6-13. By fitting a Gaussian function to the data (minimizing the residual sum of squares), the peak wavelength is found to be 724 nm (1.71 eV) with a full width half maximum of 41 nm. This peak is expected to correspond to the bandgap of the GaAsP nws.

Applying this value to Equation 6-3 results in an actual $GaAs_{1-x}P_x$ alloy composition of $x = 0.24$, very close to the nominal value of $x = 0.25$ given in the MBE growth sheet.

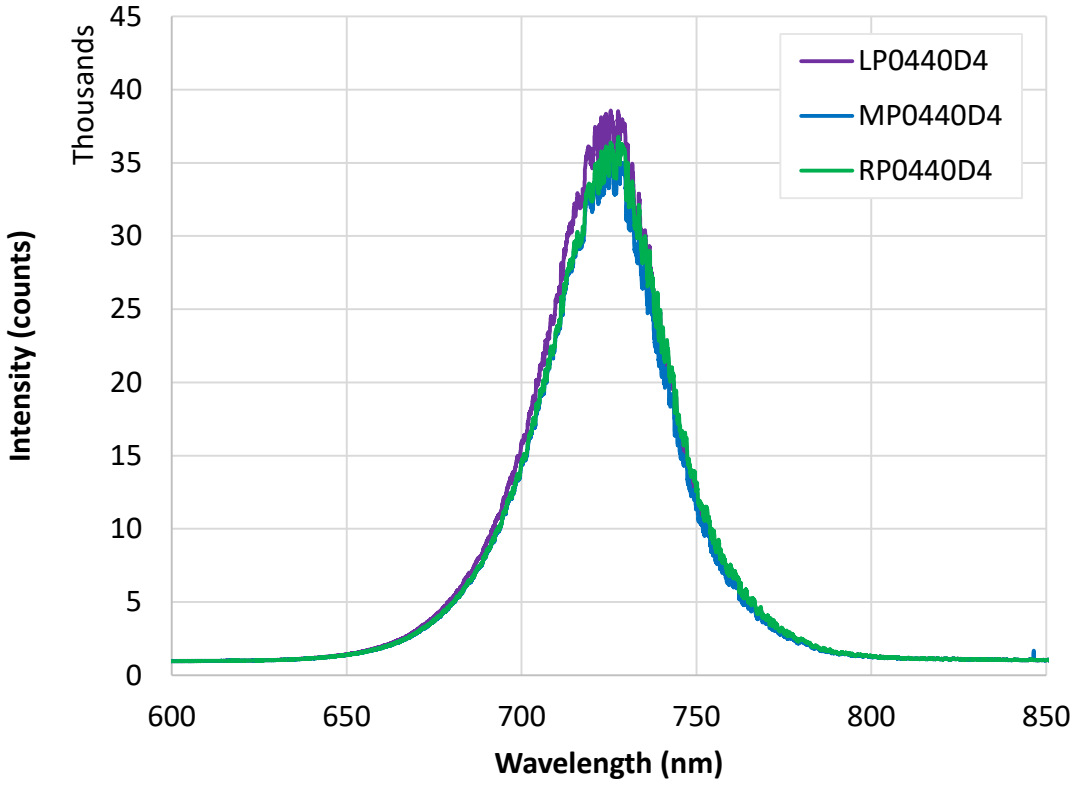

Figure 6-13: Room temperature photoluminescence spectrum for each column of the P0440D4 pads from sample #1865.

6.3.5 Transparency measurements

The final technique used in PV device characterization is to test the transparency of the transparent front contact layer, as outlined in Section 3.6.

Since the transparency of the film on the sample cannot be measured directly, a 'witness' is included on the sample stage during ITO deposition. Three transparency measurements are taken: a reference measurement of a blank quartz slide, a measurement of the ITO witness sample prior to annealing, and a measurement of the same sample after annealing. Dividing the sample data by the baseline reference yields the transparency of the ITO film itself, as a function of wavelength, as shown in Figure 6-14.

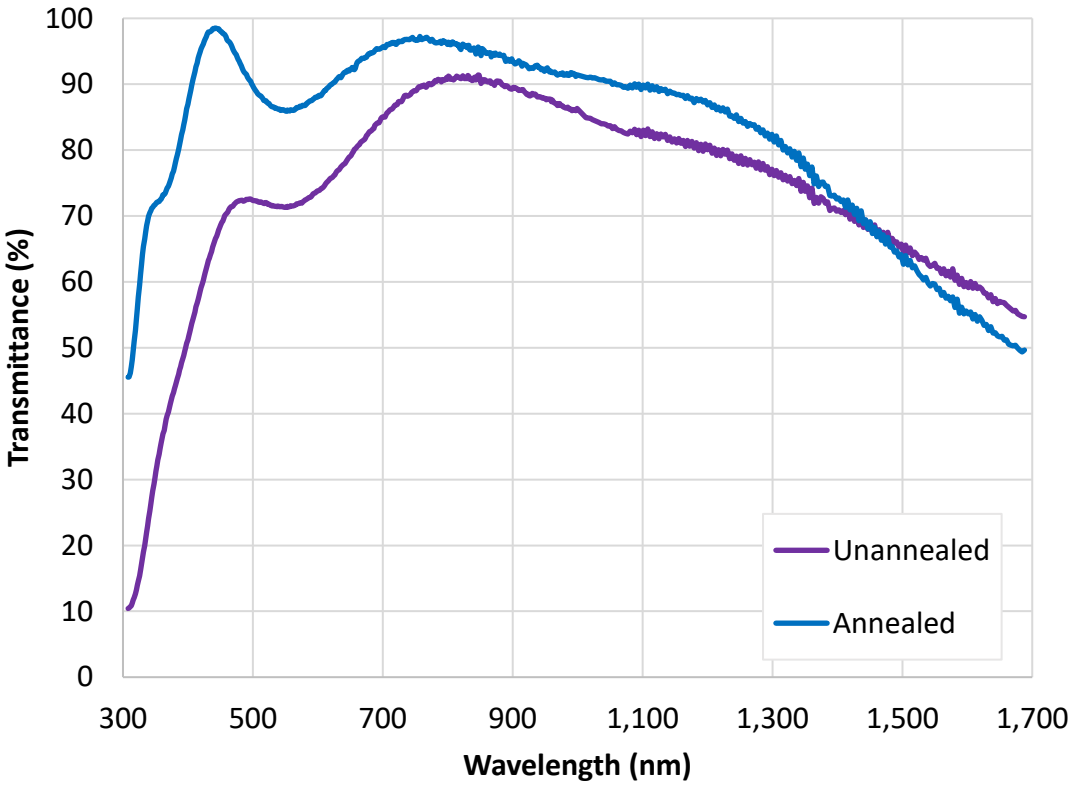

Figure 6-14: Transmittance of ITO film before and after annealing.

For applications in PV devices, this transmittance data ($T_s(\lambda)$) can be integrated over the AM1.5G spectrum to give a solar weighted transmittance (T), according to Equation 6-6:

$$T = \frac{\int_0^\infty P_{AM1.5G}(\lambda) * T_s(\lambda) d\lambda}{\int_0^\infty P_{AM1.5G}(\lambda) d\lambda} \quad (6\text{-}6)$$

It is clear, in Figure 6-14, that annealing improves transparency in the visible range of the spectrum. Despite the decline in the infrared region, annealing the sample increases the solar weighted transmittance, from 76% to 89%.

6.4 GaAsP nanowire single junction cell

6.4.1 Fabrication

As discussed earlier, a nw sample was prepared that matched the growth profile for the tandem cell, outlined in Section 6.3.1. Unfortunately, due to issues with lift-off of the front contact, and subsequent setbacks with equipment maintenance, the sample (#1874) could not be characterized and an additional device could not be prepared. To that end, a previously processed sample with slightly different growth parameters was characterized in its place. This sample (#1709) followed the standard fabrication procedure outlined in Chapter 2, and parameters for the nw growth can be found in Table 6-2.

Table 6-2: MBE growth sheet used for sample #1709.

Segment	Time (min)	Temperature (°C)	Doping (cm^{-3})	Growth Rate (µm/h)	V/III Flux Ratio
Start					
GaP	5	600	Be @ $5x10^{18}$	0.125	2
Ramp from GaP to $GaAs_{0.75}P_{0.25}$	5	600	Be @ $5x10^{18}$	0.125	2
$GaAs_{0.75}P_{0.25}$	40	600	Be @ $5x10^{18}$	0.125	2
Cool under $As_{0.75}P_{0.25}$	-	420	-	-	Keep same flow to consume Ga seed
$GaAs_{0.75}P_{0.25}$	8.5	420	-	1	2
$GaAs_{0.75}P_{0.25}$	12.5	420	Te @ $5x10^{18}$	1	2
$GaAs_{0.75}P_{0.25}$	3.5	420	Te @ $8x10^{18}$	1	2
$Al_{0.52}In_{0.48}P$	7.5	420	-	1	2
End					

Since the original growth of sample #1709, various adjustments were made to growth parameters, in order to improve nw morphology and device performance. The following changes were made for sample #1865 (as reported in Section 6.3) as compared to sample #1709 reported here. An additional step was added to consume the gallium droplet at core growth temperature (instead of consuming the droplet while cooling the sample to shell growth temperature) – in order to improve the morphology of the nw tip. The shell layers were grown at higher temperature (500°C versus 420°C) – this was found to improve the faceting of the nw shell. The intrinsic shell was grown for a longer duration (17 minutes of growth versus

8.5 minutes) – the thicker intrinsic region improved the short circuit current density. The tellurium doping in the n-region was lowered (2×10^{18} cm^{-3} versus 5×10^{18} cm^{-3}) – this improved the open circuit voltage. Finally, the growth rate of the passivation layer was decreased (0.25 µm/h versus 1 µm/h, though the duration was increased in order to maintain the same thickness) – this change was also made to improve the faceting of the nws. These process modifications resulted in a few percent (absolute) increase in nw solar cell efficiency. The detailed description of these improvements is outside the scope of the present thesis.

6.4.2 Solar simulation

IV data recorded for a subset of pads on sample #1709 are presented below. As reported above for the tandem cell, Figure 6-15 shows light IV curves in the fourth quadrant and Figure 6-16 shows both dark and light IV curves on a semi-log plot. V_{oc} and J_{sc} are found to be 507 mV and 4.54 mA/cm^2, respectively. Operating at the maximum power point of the IV curve (280 mV and 2.7 mA/cm^2, as indicated by the dashed lines in the accompanying figure) results in a fill factor of 32.2% and device efficiency of 0.75%.

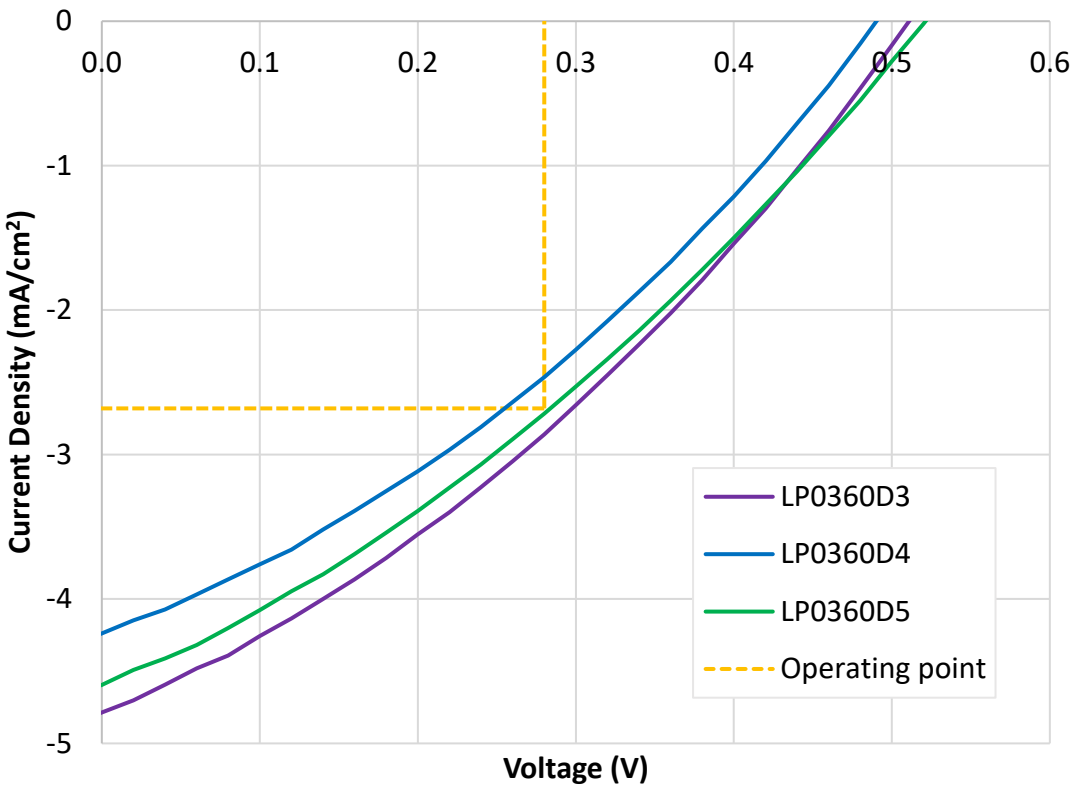

Figure 6-15: Light IV curves for the LP0360 set of pads from sample #1709.

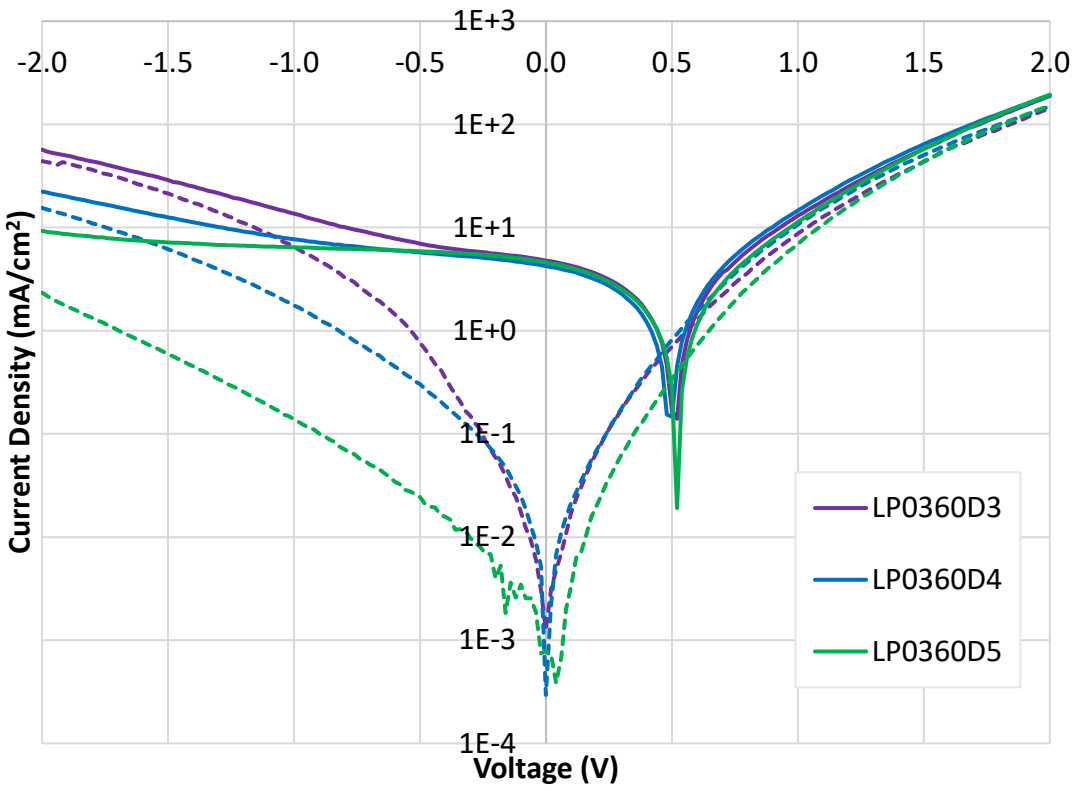

Figure 6-16: Light (solid lines) and dark (dashed lines) IV curves for the LP0360 set of pads from sample #1709.

6.4.3 EQE measurement

Since current-matching is not a concern for single junction cells, the EQE measurements do not require an external bias light or lock-in amplifier, simplifying the procedure and subsequent analysis. The EQE of sample #1709 is shown in Figure 6-17.

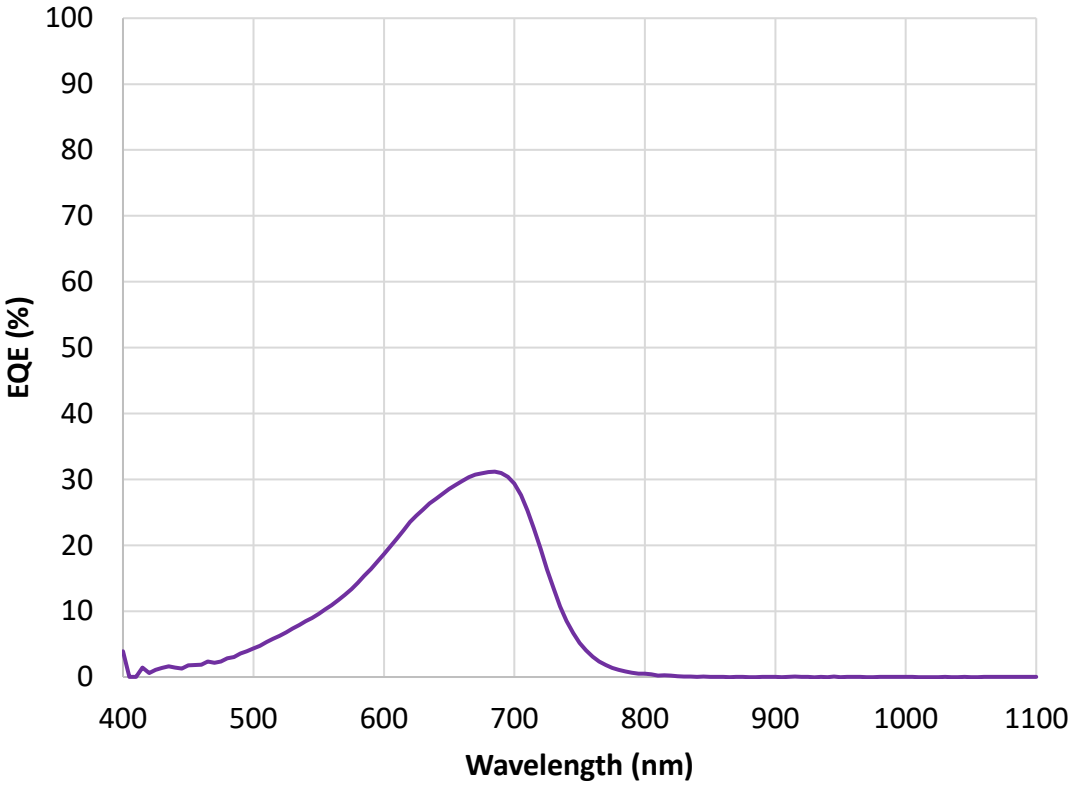

Figure 6-17: EQE response of sample #1709 LP0360D3.

Again, as expected, the EQE response diminishes as the incident photon energy exceeds the bandgap of the nws (measured to be 718 nm in Section 6.3.4). Applying Equation 6-5 yields a short circuit current density of 3.45 mA/cm^2, compared to 4.54 mA/cm^2, as determined from the IV characteristics in Figure 6-15.

6.4.4 Photoluminescence

The photoluminescence response of the device is shown in Figure 6-18. The peak wavelength is found to be 718 nm (1.73 eV) with a full width half maximum of 52 nm (by Gaussian fitting). This bandgap energy corresponds to a $GaAs_{1-x}P_x$ alloy composition of $x = 0.25$.

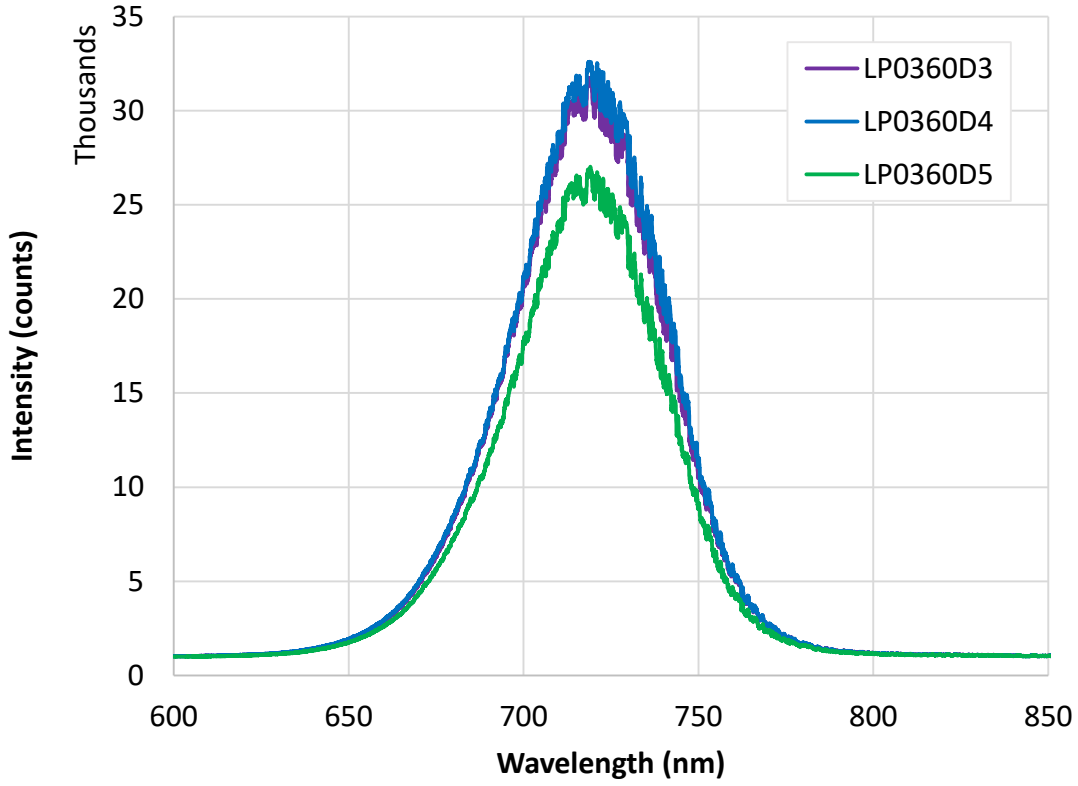

Figure 6-18: Room temperature photoluminescence spectra for the LP0360 set of pads from sample #1709.

6.5 Silicon single junction cell

6.5.1 Fabrication

Since this sample did not have any nw growth, the processing was more straightforward. Starting with a wafer equivalent to the one described in Section 6.3.1, the sample was simply etched in a BHF solution to remove the thermally grown oxide on both sides of the sample. A standard aluminum rear contact was sputtered, a titanium / platinum / gold (25 nm / 50 nm / 225 nm) front contact was deposited by electron beam evaporation, and the sample was annealed using the standard recipe. The front contact was applied using a 'busbar' mask resulting in the layout shown in Figure 6-19. The opaque metal front contact blocks incident light during device characterization, contributing shadow losses of 17.5%.

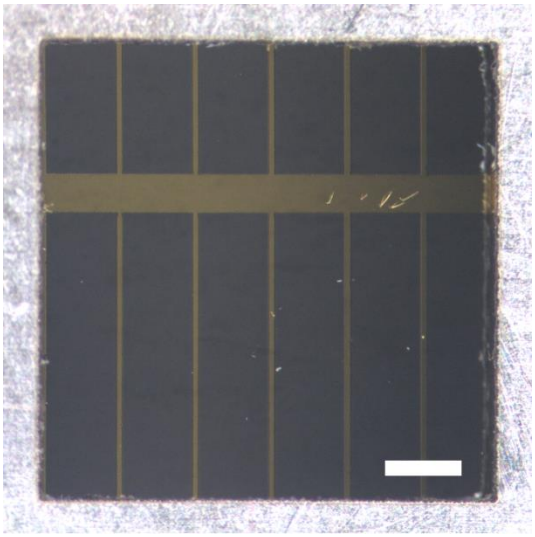

Figure 6-19: Busbar layout for sample #3-II. The thick horizontal busbar is 0.5 mm wide, the thin vertical contact fingers are 0.1 mm wide, and the aluminum aperture is 6 mm x 6 mm. Scale bar is 1 mm.

6.5.2 Solar simulation

IV data recorded for sample #3-II is presented below. As reported above for the nw cells, Figure 6-20 shows the light IV curve in the fourth quadrant and Figure 6-21 shows both dark and light IV curves on a semi-log plot. V_{oc} and J_{sc} are found to be 536 mV and 27.8 mA/cm^2, respectively. Operating at the maximum power point of the IV curve (400 mV and 23.3 mA/cm^2) results in a fill factor of 62.5% and device efficiency of 9.33%.

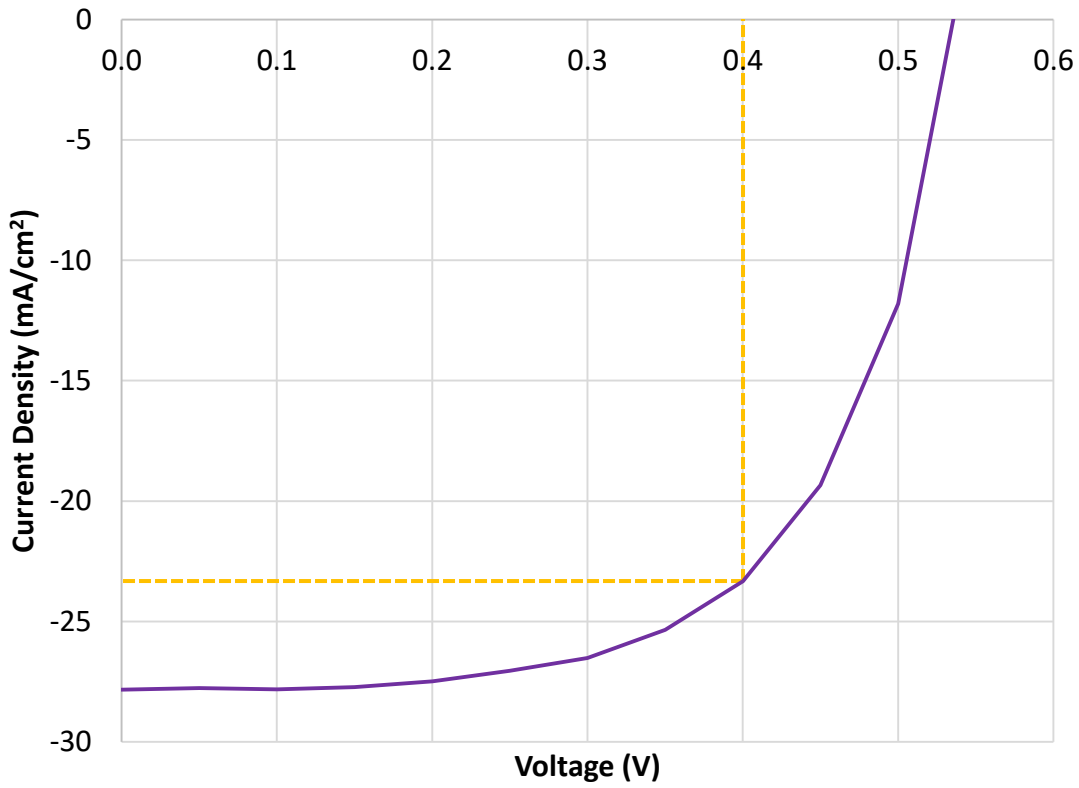

Figure 6-20: Light IV curve for sample #3-II.

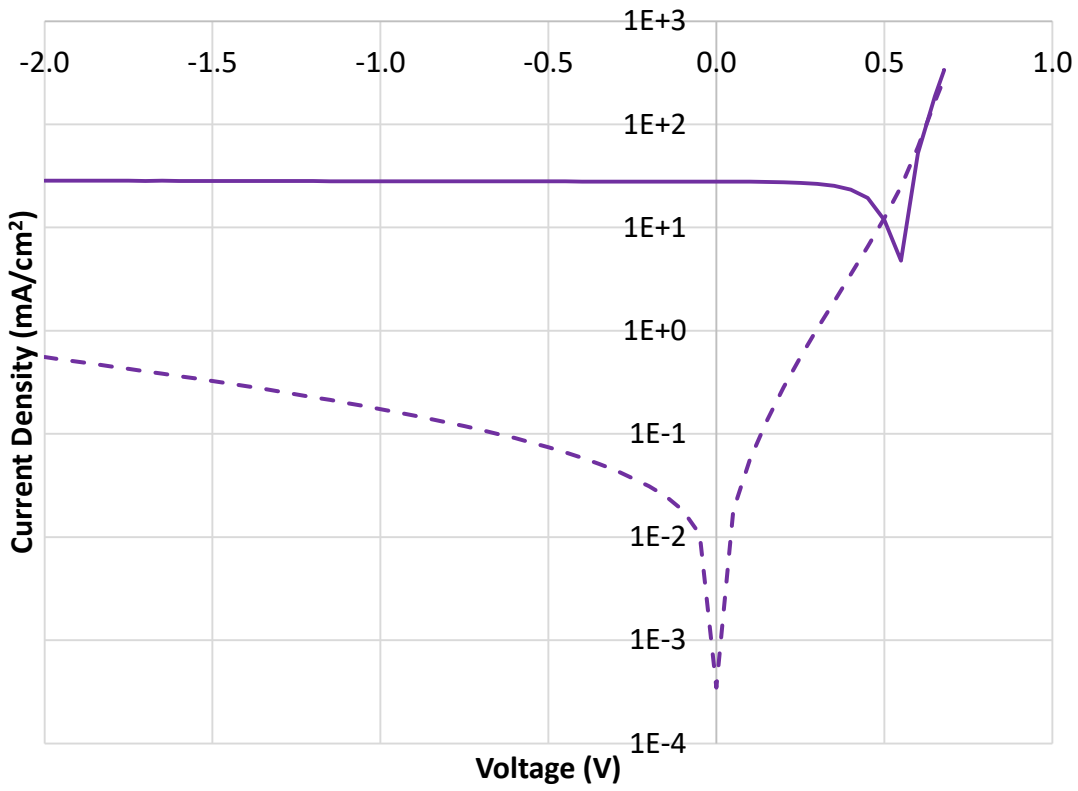

Figure 6-21: Light (solid lines) and dark (dashed lines) IV curves for sample #3-II.

The performance of this silicon cell is compared with the results reported for the world record device (based on conversion efficiency) produced by Kaneka in 2016 [46]. This is shown below in Table 6-3. Compared to an ideal cell, the open circuit voltage of sample #3-II is reduced due to recombination effects, while the fill factor is reduced due to parasitic resistance (described in more detail in Section 6.6). The short circuit current density is strongly limited by both reflection and shadow losses, as discussed in Section 6.5.3.

Table 6-3: Comparison of sample #3-II to state-of-the-art device.

	Silicon single junction cell (#3-II)	State-of-the-art crystalline silicon cell [46]
V_{oc} (mV)	536	744
J_{sc} (mA/cm^2)	27.8	42.3
Fill factor (%)	62.5	83.8
Efficiency (%)	9.33	26.3

6.5.3 EQE measurement

The EQE of sample #3-II is shown in Figure 6-22. Applying Equation 6-5 yields a short circuit current density of 24.9 mA/cm^2, compared to 27.8 mA/cm^2, as determined from the IV characteristics in Figure 6-20.

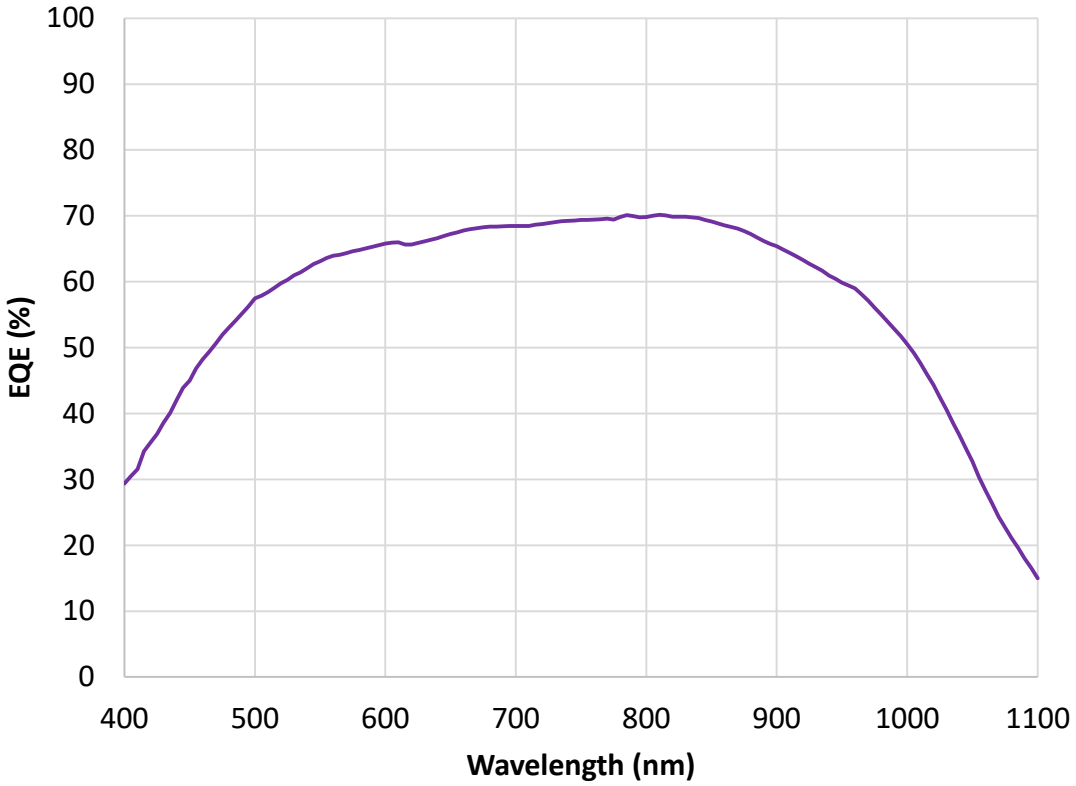

Figure 6-22: EQE response of sample #3-II.

Besides the unavoidable spectral losses described in Section 6.1, the other two main sources of loss in this device are shadow losses and reflection losses. The shadow losses, described above, are due to the upper opaque metal contact on the device, physically blocking light from reaching the cell. 17.5% of the device is shadowed, affecting all wavelengths equally.

Reflection losses, on the other hand, are dependent on the wavelength of incident light. According to the Fresnel equations, reflectivity (at normal incidence)

is given by Equation 6-7, where $\hat{n}$ corresponds to the complex refractive index of the materials at the interface (with light travelling from $\hat{n}_1$ to $\hat{n}_2$) [47]:

$$R = \frac{|\hat{n}_2 - \hat{n}_1|^2}{|\hat{n}_2 + \hat{n}_1|^2} \tag{6-7}$$

Considering light incident on a silicon solar cell, $\hat{n}_1$ is taken to be 1 (for air) and $\hat{n}_2 = n - ik$ (for silicon). However, both n and k vary with wavelength, so the equation above can be rewritten as shown in Equation 6-8:

$$R(\lambda) = \frac{(n(\lambda) - 1)^2 + k(\lambda)^2}{(n(\lambda) + 1)^2 + k(\lambda)^2} \tag{6-8}$$

Under illumination by the AM1.5G spectrum, the maximum output power of an ideal silicon cell, as calculated in the numerator of Equation 6-1, can be further adapted to incorporate these losses due to both reflectance and shadowing, according to Equation 6-9:

$$P_{max} = f_{shadow} \int_0^{\lambda g} R(\lambda) * P_{AM1.5G}(\lambda) \frac{\lambda}{\lambda_g} d\lambda \tag{6-9}$$

Experimental values of n and k for silicon at 300K at various wavelengths are tabulated by Green and Keevers [48]. Using this data to calculate $R(\lambda)$ and

using $f_{shadow} = 82.5\%$ corresponds to a theoretical maximum output power of 26.2 mW/cm^2. Finally, as in Section 6.1, assuming each carrier is extracted with energy equal to the bandgap of silicon (1.12 eV), this yields a maximum short circuit current density of 23.4 mA/cm^2.

It should be noted that the growth of a native oxide on the surface of the cell following the initial BHF etch would reduce the reflectance of the cell by introducing a thin film with an intermediate index of refraction (on the order of 1.5). Therefore, it is likely that the losses due to reflection are slightly overestimated in this theoretical analysis. However, with this in mind, it is clear that the quality of the silicon substrates used for this project is very high based on the calculation of the short circuit current density by EQE integration.

6.6 Comparison of results

A summary of the electrical characterization of the three devices described above are tabulated in Table 6-4.

Table 6-4: Electrical characterization results for samples #1865, #1709, and #3-II.

	GaAsP nw-on-Si tandem junction cell (#1865)	GaAsP nw single junction cell (#1709)	Silicon single junction cell (#3-II)
V_{oc} (V)	1.16	0.51	0.54
J_{sc} (mA/cm^2)	7.65	4.54	27.8
Fill factor (%)	39.6	32.2	62.5
Efficiency (%)	3.51	0.75	9.33

Two notable results can be observed from the table, while also revealing areas for future improvement. Firstly, the open circuit voltage of the tandem cell is approximately equal to the sum of the open circuit voltages of each single junction subcell. This is expected since the subcells are connected in series [45]. Secondly, the short circuit current density of the tandem cell is drastically limited by the addition of the upper nw subcell. This can also be seen by comparing the current densities calculated by integrating the EQE curves of the two subcells. A large portion of the incident light is absorbed in the lower silicon subcell and lost to recombination since there is deficient EHP generation in the nw subcell. This, in turn, limits the efficiency of the overall device. Methods for improving the current density in the nw subcell to ensure proper current-matching are discussed in Section 7.2.

Furthermore, a reduction in fill factor is also evident when comparing the thin film silicon cell to the single junction nw and tandem cells. As alluded to in Section 3.4, this is attributed to an increase in parasitic resistance. As the device structure and processing procedure becomes more complex, there are more opportunities for these parasitic resistances to manifest. A solar cell schematic is shown in Figure 6-23, where R_s represents 'series resistance' and R_{sh} represents 'shunt resistance'.

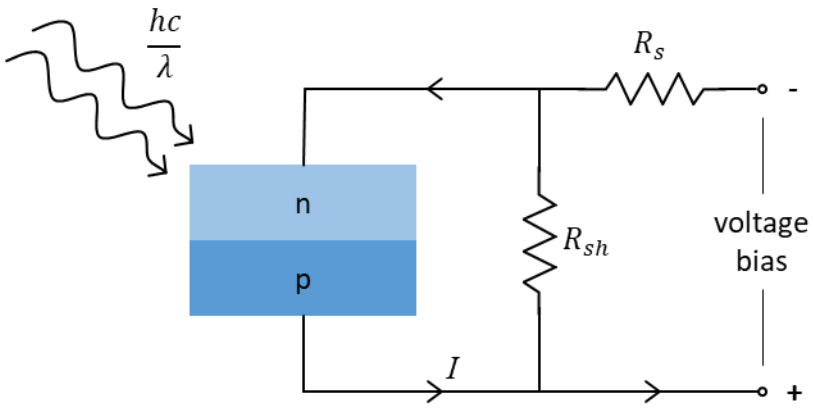

Figure 6-23: Schematic modelling parasitic resistances in a solar cell.

Sheet resistance of the ITO front contact, for example, contributes to series resistance, dissipating power during solar cell operation. In a perfect cell, R_s would be zero, but as this resistance increases, the fill factor decreases, eventually limiting the short circuit current. On the other hand, imperfections in nw growth, for example, can contribute to shunt resistance, providing an alternate current path for carriers during operation. Ideally, R_{sh} would be infinite, but as this resistance decreases, so too does the fill factor, and in extreme cases the open circuit voltage is limited as well [26].

7 Conclusions & Discussion

7.1 Summary of present work

The goal of this thesis work was to investigate III-V nw arrays as PV devices, specifically addressing areas of improvements to characterization and device design. Substrate-free optical characterization of nw arrays and front contact characterization were pursued (Chapters 4 and 5), though attention from these projects were ultimately shifted to the research into tandem cells detailed in Chapter 6. NW-on-Si tandem cell results have been reported in literature previously; for example, Yao et al. reported an axial GaAs nw-on-Si tandem device with 11.4% efficiency in 2015 [49]. However, the present work is the first reported nw-on-Si tandem device utilizing a radial p-n junction nw structure, taking advantage of the perpendicularity of light absorption and carrier collection. There is still much work to be done in terms of device performance to rival current high efficiency PV devices, but the initial success reported herein shows promise and already indicates several areas for future improvements.

As mentioned in Chapter 4, a novel method for effective substrate removal is presented below in Section 7.2.1. Research on developing an accurate proxy for electrical characterization of front contacts, as described in Chapter 5, is ongoing. Finally, further improvements to the initial design and fabrication of nw-based tandem cells, as detailed in Chapter 6, are suggested below. These, and other ongoing research projects, will continue to drive incremental improvements to III-V nw-based photovoltaics, combining the unique optical and electrical

properties of nws with the tunability of III-V materials and the economics and infrastructure of silicon-based device fabrication. Exploring novel approaches to affordable renewable energy solutions is critical to meeting ever-increasing global energy demands.

7.2 Future work

7.2.1 Substrate etching on SOI wafers

The main challenge with substrate removal is finding a suitable etchant that can controllably remove the sample substrate while leaving the nw array intact. Most standard silicon etchants preferentially etch the <100> plane, and the <111> plane commonly serves as an etch stop layer (a feature frequently used to texture PV devices [50]). With nw arrays grown on <111> silicon, it can be difficult to controllably etch a relatively thick substrate. Device substrates are on the order of hundreds of microns thick and nws grown for PV applications are typically less than two microns tall. Even using a strongly selective etchant, it would still be very difficult to completely remove the substrate without damaging the nw array.

Previous work has incorporated a lattice-matched InGaP etch stop layer to perform measurements on substrate-free GaAs nw arrays [51]. However, this relied on employing a GaAs substrate and a lattice-matched top-down fabrication method, whereas the nw devices presented in this work are grown using a bottom-up method on silicon substrates. In lieu of adding an etch stop layer between the

substrate and nws, it would be possible to begin processing on a silicon-on-insulator (SOI) wafer instead.

An SOI wafer is made up of a ‘device layer’ (typically 2 to 20 microns thick) and a ‘handle wafer’ (around 400 microns thick) with a thin ‘buried oxide’ layer in between (a few microns thick) [52]. One method for preparing SOI wafers involves four steps: hydrogen ion implantation of a silicon wafer capped with a thermally grown oxide (which will become the device layer); hydrophilic bonding to a second silicon wafer (the handle wafer); heat treatment of the bonded wafers to split the first wafer (at the depth of hydrogen implantation) and to strengthen the chemical bonds between the two wafers; and finally a chemomechanical polishing step to smooth the surface of the device layer and ensure an even thickness across the SOI substrate [53]. For substrate removal, a nw array could initially be grown on a SOI wafer with a <111> device layer and a <100> handle wafer, as shown in Figure 7-1, allowing for a much faster etching procedure.

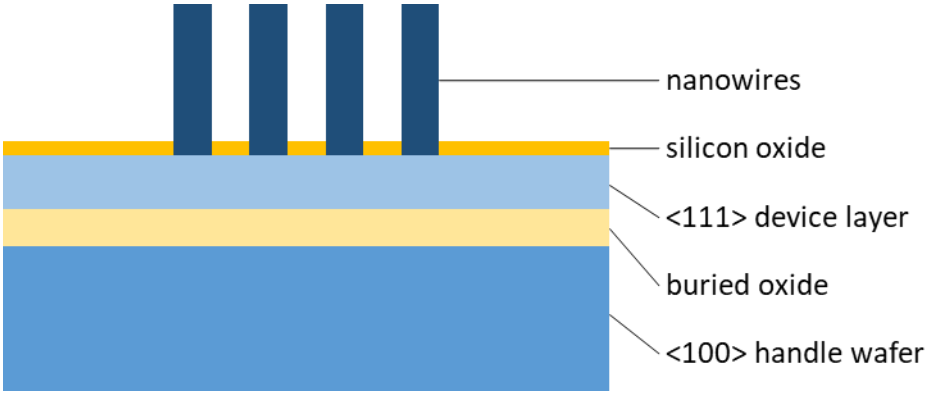

Figure 7-1: Schematic demonstrating the proposed SOI structure. Note that the upper silicon oxide layer would be deposited via chemical vapour deposition separately, in order to pattern nw growth. Features are not to scale.

Using a comparable masking scheme to that outlined in Chapter 4, it would be straightforward to etch a 'window' into the handle wafer using a standard KOH etch [54], for example, with the buried oxide layer acting as an etch stop. This would serve as a fast and simple method to remove the bulk of the substrate. The buried oxide layer could then be removed by a simple HF etch, leaving behind the device layer as the only remaining portion of the substrate. A variety of options could be pursued at this point in order to obtain transmittance measurements of the nw array.

A 2 µm thick silicon membrane will transmit approximately 60% of the photons corresponding to the AM1.5G spectrum [55]. Assuming a uniform thickness of the device layer, a baseline transparency measurement of the membrane can be taken and used to calculate the transmittance of the nw array,

using the method described in Section 6.3.5. Alternatively, with a much smaller layer of silicon to work with, a controlled etch is more viable. Complete substrate removal may be preferred, depending on the specific wavelength range of interest, and for SOI device layers with variable thickness. Either wet or dry etching could be explored, with more flexibility around etch rates and selectivity, producing a clean, substrate-free nw array upon which to perform transmittance measurements.

7.2.2 Improvements to current density of nanowire cell

While the tandem nw cell characterized in this work exhibited an improvement in performance over the single junction GaAsP nw cell, the overall efficiency was lower than that of the single junction silicon cell. This is largely attributed to a reduction in short circuit current density due to the current-matching requirement of series-connected multi-junction devices.

The bandgap optimization calculations in Section 6.1 indicate a balanced maximum current density of 21.9 mA/cm^2 for each cell under AM1.5G illumination. Factoring in recombination, blackbody radiation, and other sources of loss (e.g. parasitic resistances) reduces this even further. The calculations in Section 6.3.3, derived from EQE measurements, indicated short circuit current density contributions of 6.98 mA/cm^2 and 15.8 mA/cm^2 from the upper and lower subcells, respectively. Since the nw subcell is current-limiting the device, shifting absorption

from the silicon substrate into the nw array would improve the overall output of the device.

As discussed in Chapter 4, the absorption of nw arrays is dependent on a variety of factors. The EBL patterning step used in device fabrication varies both pitch and diameter of the resulting nw arrays but variation in nw length was not explored. Based on optical simulations, increasing the length of GaAs nws from 1.5 µm to 2 µm notably increased the absorption of the array, particularly in the visible range [7], and this trend is expected to continue for even longer nws (albeit diminishingly). Increasing the length of the GaAsP nws in the tandem cell design is presumed to increase the absorption in the nw array, reducing the amount of light reaching the silicon substrate, and achieving a better balance in subcell current density contributions. A study varying nw length (i.e. p-core growth duration) across a set of otherwise identical samples would be useful to investigate the impact that this change would have.

7.2.3 Lattice matched passivation layer

Due to the high surface area of nw structures, an outer passivation layer is required to reduce harmful effects, such as surface recombination and carrier depletion, which limit device performance [1,13]. For the tandem cell described in Chapter 6, the $Al_xIn_{1-x}P$ passivation shell grown during MBE was based on earlier research in GaAs nw devices. The composition ($x = 0.52$) was designed to match

the lattice constant of GaAs. An improvement in device quality and overall performance of the tandem cell could be achieved by adjusting the composition of the passivation layer for lattice-matching to the $GaAs_{0.75}P_{0.25}$ nws instead.

The lattice constant, a, of a ternary III-V semiconductor alloy can be linearly interpolated from its binary constituents [4], per Equation 7-1:

$$a_{A_{1-x}B_x} = (1-x)a_A + xa_B \tag{7-1}$$

Using $x = 0.25$ for the $GaAs_{1-x}P_x$ nws (to optimize the bandgap) yields a ternary lattice constant of 5.6031 Å. The binary lattice constants for AlP and InP at 300 K are 5.4672 Å and 5.8697 Å, respectively [4]. Therefore, an $Al_xIn_{1-x}P$ composition of $x = 0.66$ would result in a lattice-matched passivation layer. This adjustment is not expected to have a significant impact on the bandgap, or other optical properties of the shell. However, with an improved surface passivation structure, future device performance is anticipated to improve as well [13].

7.2.4 Adjust lithography patterns to improve characterization

One of the major challenges with characterization of the tandem cell detailed in Chapter 6 is accurately measuring the EQE of the individual subcells. This is due to the current-matching condition of multi-junction devices. The masking

process employed to isolate the lower Si subcell, in particular, could be improved by adjusting the lithography patterns in the device processing procedure.

For example, the opaque mask shown in the schematic in Figure 6-10 could be deposited via lithography instead of manually aligning the mask. Note that this would also likely require the nw pads to be spaced further apart, to accommodate the spot size of the incident light. One possible solution would be to expand the Ni/Ge/Au contact finger to cover all four sides of the nw pad. However, consideration must be made to any capacitive effects this may cause [56] and also how this might affect the lift-off procedure. Another possibility, to address capacitance, would be to deposit an insulator (e.g. silicon nitride) via lithography before applying the mask layer, to prevent any electrical connection between the contact finger and opaque mask.

Having isolated nw pads with precisely aligned shadow masks would allow for simpler and more accurate EQE measurements to be taken. By probing the individual subcells of a multi-junction device, EQE measurements, in particular, are critical to fully understanding the behaviour of the solar cell [45]. An improved lithography scheme would expedite device characterization to indicate areas for improvement on cell design.

8 References

[1] R. R. LaPierre, a. C. E. Chia, S. J. Gibson, C. M. Haapamaki, J. Boulanger, R. Yee, P. Kuyanov, J. Zhang, N. Tajik, N. Jewell, and K. M. a. Rahman, “III-V nanowire photovoltaics: Review of design for high efficiency,” *Phys. status solidi - Rapid Res. Lett.*, vol. 7, no. 10, pp. 815–830, Oct. 2013.

[2] K. M. Azizur-Rahman, “SIMULATION OF III-V NANOWIRES FOR INFRARED PHOTODETECTION,” McMaster University, 2016.

[3] W. C. O’Mara, R. B. Herring, and L. P. Hunt, *Handbook of Semiconductor Silicon Technology*, 1st ed. William Andrew, 1990.

[4] I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, “Band parameters for III-V compound semiconductors and their alloys,” *J. Appl. Phys.*, vol. 89, no. 11 I, pp. 5815–5875, 2001.

[5] B. G. Streetman and S. K. Banerjee, *Solid State Electronic Devices*, 6th ed. Prentice Hall, 2005.

[6] B. M. Kayes, H. A. Atwater, and N. S. Lewis, “Comparison of the device physics principles of planar and radial p-n junction nanorod solar cells,” *J. Appl. Phys.*, vol. 97, no. 11, 2005.

[7] K. M. Azizur-Rahman and R. R. LaPierre, “Wavelength-selective absorptance in GaAs, InP and InAs nanowire arrays,” *Nanotechnology*, vol. 26, no. 29, p. 295202, 2015.

[8] P. Rai-Choudhury, *Handbook of Microlithography, Micromachining, and Microfabrication: Volume 1*. SPIE, 1997.

[9] M. Hitchman and K. Jensen, *Chemical Vapor Deposition: Principles and Applications*, 1st ed. Academic Press, 1993.

[10] A. Fontcuberta i Morral, “Gold-free GaAs nanowire synthesis and optical properties,” *IEEE J. Sel. Top. Quantum Electron.*, vol. 17, no. 4, pp. 819–828, 2011.

[11] S. Gibson, “GA-ASSISTED NANOWIRE GROWTH ON NANO-PATTERNED SILICON,” McMaster University, 2014.

[12] J. P. Boulanger, A. C. E. Chia, B. Wood, S. Yazdi, T. Kasama, M. Aagesen, and R. R. LaPierre, “Characterization of a Ga-Assisted GaAs Nanowire Array Solar Cell on Si Substrate,” *IEEE J. Photovoltaics*, vol. 6, no. 3, pp. 661–667, 2016.

[13] A. C. E. Chia, M. Tirado, F. Thouin, R. Leonelli, D. Comedi, and R. R. LaPierre, “Surface depletion and electrical transport model of AlInP-passivated GaAs nanowires,” *Semicond. Sci. Technol.*, vol. 28, no. 10, p. 105026, 2013.

[14] A. Mikkelsen, N. Skold, L. Ouattara, M. Borgstrom, J. N. Andersen, L. Samuelson, W. Seifert, and E. Lundgren, “Direct imaging of the atomic structure inside a nanowire by scanning tunnelling microscopy,” *Nat. Mater.*, vol. 3, no. 8, pp. 519–523, 2004.

[15] R. G. Poulsen, “Plasma etching in integrated circuit manufacture—A review,” *J. Vac. Sci. Technol.*, vol. 14, no. 1, p. 266, 1977.

[16] A. C. Chia and R. R. LaPierre, “Contact planarization of ensemble nanowires,” *Nanotechnology*, vol. 22, no. 24, p. 245304, 2011.

[17] G. N. Jackson, “R.F. sputtering,” *Thin Solid Films*, vol. 5, no. 4, pp. 209–246, Apr. 1970.

[18] J. Singh and D. E. Wolfe, “Review Nano and macro-structured component fabrication by electron beam-physical vapor deposition (EB-PVD),” *J. Mater. Sci.*, vol. 40, no. 1, pp. 1–26, Jan. 2005.

[19] E. Benes, M. Schmid, and G. Thorn, “Progress in monitoring thin film thickness by use of quarz crystals,” *Thin Solid Films*, vol. 174, pp. 307–314, 1989.

[20] M. Hatzakis, B. J. Canavello, and J. M. Shaw, “Single-Step Optical Lift-Off Process,” *IBM J. Res. Dev.*, vol. 24, no. 4, pp. 452–460, 1980.

[21] J. Zhang, A. C. E. Chia, and R. R. LaPierre, “Low resistance indium tin oxide contact to n-GaAs nanowires,” *Semicond. Sci. Technol.*, vol. 29, p. 54002, 2014.

[22] National Renewable Energy Laboratory, “Reference Solar Spectral Irradiance: Air Mass 1.5.” [Online]. Available: http://rredc.nrel.gov/solar/spectra/am1.5/. [Accessed: 03-Aug-2017].

[23] J. Janesch, “Two-Wire vs. Four-Wire Resistance Measurements: Which Configuration Makes Sense for Your Application?,” 2013. [Online]. Available: http://jp.tek.com/sites/tek.com/files/media/document/resources/2Wire_4Wire Resistance Article.pdf. [Accessed: 31-Jul-2017].

[24] J. I. Goldstein, D. E. Newbury, P. Echlin, D. C. Joy, C. E. Lyman, E. Lifshin, L. Sawyer, and J. R. Michael, *Scanning Electron Microscopy and X-ray Microanalysis*, 3rd ed. Boston: Springer US, 2003.

[25] JEOL USA Inc., “Sample Coating for SEM,” 2015. [Online]. Available: http://www.jeolusa.com/RESOURCES/Sample-Preparation/Documents-Downloads. [Accessed: 03-Aug-2017].

[26] A. Jain and A. Kapoor, “Exact analytical solutions of the parameters of real solar cells using Lambert W-function,” *Sol. Energy Mater. Sol. Cells*, vol. 81, no. 2, pp. 269–277, 2004.

[27] F. M. Smits, “Measurement of Sheet Resistivities with the Four-Point Probe,” *Bell Syst. Tech. J.*, vol. 37, no. 3, pp. 711–718, May 1958.

[28] K. K. Smith, “Photoluminescence of semiconductor materials,” *Thin Solid Films*, vol. 84, no. 2, pp. 171–182, Oct. 1981.

[29] H. Fujiwara, *Spectroscopic Ellipsometry: Principles and Applications*. Wiley, 2007.

[30] E. Fest, *Stray Light Analysis and Control*. SPIE, 2013.

[31] J. Zhang, “ELECTRICAL AND OPTICAL CHARACTERIZATION OF GaAs NANOWIRE ARRAYS,” McMaster University, 2014.

[32] Toronto Nanofabrication Centre, “Deep Reactive Ion Etching Recipes.” [Online]. Available: http://tnfc.utoronto.ca/home/user-resources/process-database/drie-recipes/. [Accessed: 21-Jul-2017].

[33] H. Seidel, “Anisotropic Etching of Crystalline Silicon in Alkaline Solutions,” *J. Electrochem. Soc.*, vol. 137, no. 11, p. 3612, 1990.

[34] B. Schwartz and H. Robbins, “Chemical etching of silicon: IV. Etching technology,” *J. Electrochem. Soc.*, vol. 123, no. 12, pp. 1903–1909, 1976.

[35] R. B. Darling, “MicroFabrication: Wet Etching,” *Lecture Notes for EE-527: Solid-State Laboratory Techniques*. University of Washington.

[36] A. R. Clawson, “Guide to references on III-V semiconductor chemical etching,” *Mater. Sci. Eng.*, vol. 31, pp. 1–438, 2001.

[37] X. B. Zou, H. Liang, and K. M. Lau, “Light extraction enhancement from GaN-based thin-film LEDs grown on silicon after substrate removal using HNA solution,” *Phys. Status Solidi Curr. Top. Solid State Phys.*, vol. 7, no. 7, pp. 2171–2173, 2010.

[38] A. Wang, “HIGH EFFICIENCY PERC AND PERL SILICON SOLAR CELLS,” University of New South Wales, 1992.

[39] M. A. Green, “The path to 25% silicon solar cell efficiency: History of silicon cell evolution,” *Prog. Photovoltaics Res. Appl.*, vol. 17, no. 3, pp. 183–189, 2009.

[40] K. Sreenivas, T. Sudersena Rao, A. Mansingh, and S. Chandra, “Preparation and characterization of rf sputtered indium tin oxide films,” *J. Appl. Phys.*, vol. 57, no. 2, pp. 384–392, Jan. 1985.

[41] L. J. van der Pauw, “A method of measuring the resistivity and Hall coefficient on lamellae of arbitrary shape,” *Philips Technical Review*, vol. 20. pp. 220–224, 1958.

[42] J. D. Cutnell and K. W. Johnson, *Physics*, 4th ed. New York: Wiley, 1998.

[43] C. G. Granqvist and A. Hultåker, “Transparent and conducting ITO films: new developments and applications,” *Thin Solid Films*, vol. 411, no. 1, pp. 1–5, 2002.

[44] W. Shockley and H. J. Queisser, “Detailed balance limit of efficiency of p-n junction solar cells,” *J. Appl. Phys.*, vol. 32, no. 3, pp. 510–519, 1961.

[45] A. Luque and V. Andreev, *Concentrator Photovoltaics*, 1st ed. Springer, 2007.

[46] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, E. D. Dunlop, D. H. Levi, and A. W. Y. Ho-Baillie, “Solar cell efficiency tables (version 49),” *Prog. Photovoltaics Res. Appl.*, vol. 25, no. 1, pp. 3–13, Jan. 2017.

[47] M. Born and E. Wolf, *Principles of Optics*, 4th ed. Pergamon Press, 1970.

[48] M. A. Green and M. J. Keevers, “Optical properties of intrinsic silicon at 300 K,” *Prog. Photovoltaics Res. Appl.*, vol. 3, no. 3, pp. 189–192, 1995.

[49] M. Yao, S. Cong, S. Arab, N. Huang, M. L. Povinelli, S. B. Cronin, P. D. Dapkus, and C. Zhou, “Tandem Solar Cells Using GaAs Nanowires on Si: Design, Fabrication, and Observation of Voltage Addition,” *Nano Lett.*, vol. 15, no. 11, pp. 7217–7224, 2015.

[50] J. Zhao, A. Wang, P. Altermatt, and M. A. Green, “Twenty-four percent efficient silicon solar cells with double layer antireflection coatings and reduced resistance loss,” *Appl. Phys. Lett.*, vol. 66, no. 26, p. 3636, 1995.

[51] J. Zhang, N. Dhindsa, A. Chia, J. Boulanger, I. Khodadad, S. Saini, and R. LaPierre, “Multi-spectral optical absorption in substrate-free nanowire arrays,” *Appl. Phys. Lett.*, vol. 123113, pp. 19–23, 2014.

[52] Ultrasil Corporation, “Inventory: SOI Wafers.” [Online]. Available: http://www.ultrasil.com/get_quote_all_products_new.aspx. [Accessed: 21-Jul-2017].

[53] M. Bruel, “Silicon on insulator material technology,” *Electron. Lett.*, vol. 31, no. 14, p. 1201, 1995.

[54] K. Sato, M. Shikida, Y. Matsushima, T. Yamashiro, K. Asaumi, Y. Iriye, and M. Yamamoto, “Characterization of orientation-dependent etching properties of single-crystal silicon: effects of KOH concentration,” *Sensors Actuators A Phys.*, vol. 64, no. 1, pp. 87–93, 1998.

[55] E. Janssen and R. Kleiman, “Novel process flow and cell architecture for 10 µm thick membrane single-crystalline silicon solar cell,” *2012 38th IEEE Photovolt. Spec. Conf.*, no. i, pp. 001205–001208, 2012.

[56] A. Edler, M. Schlemmer, J. Ranzmeyer, and R. Harney, “Understanding and overcoming the influence of capacitance effects on the measurement of high efficiency silicon solar cells,” *Energy Procedia*, vol. 27, pp. 267–272, 2012.

9 Appendix

9.1 Processing Recipes

EBL procedure

- Sonicate wafer in acetone for 1 minute followed by IPA for 1 minute; dry using N_2
- Mount wafer on spinner and apply ZEP520A : Anisole mixture (in 1 : 1 ratio) to cover approximately two thirds of the sample surface; spin at 6000 rpm for 1 minute (with 584 rpm / second ramp); bake at 180°C for 3 minutes
- Mount wafer on sample stage and perform EBL
- Develop sample for 1 minute in ZED-N50; clean wafer for 30 seconds in solution of 45 mL MIBK : 15 mL IPA; dry using N_2

RIE and BHF etch for EBL pattern transfer

- Etch wafer under 10 sccm of CF_4 flow at 100 W RF power and 320 mTorr chamber pressure (typical total etch duration of approximately 80 to 140 seconds, depending on oxide thickness)
- Dice 4” wafer into quarters, if necessary
- Strip resist and clean sample by sonicating in ZMAC for 5 minutes followed by acetone for 3 minutes and IPA for 3 minutes; rinse in DI water and dry using N_2
- Cleave 3” wafer into pie pieces, if necessary
- Immediately prior to loading in MBE chamber, etch sample for 25 seconds in solution of 20mL BHF : 200mL DI water; rinse in DI water and dry using N_2

Planarization with BCB

- Prepare 5-10 mL of BCB in a small beaker; place beaker in desiccator and degas using vacuum pump for 2 minutes or until bubbles stop appearing
- Using a syringe and filter, apply degassed BCB to front of sample and wait for 5 minutes (to let the resist settle between nws); spin at 5000 rpm for 77 seconds (with 300 rpm / second ramp); soft bake at 100°C for 90 seconds; let sit for 2 minutes
- Apply second layer of BCB by repeating the previous step
- Transfer sample to hotplate in N_2 glove box; ramp temperature to 250°C at 300°C / hour (approximately 45 minutes); hard bake at 250°C for 30 minutes

RIE for BCB etch-back

- Etch sample under 2 sccm O_2 : 2 sccm CF_4 flow at 50 W RF power and 180 mTorr chamber pressure; monitor etch depth in SEM and continue etching until nws tips are exposed; mask individual rows of nw pads using glass cover slides if necessary (typical total etch duration of 5 to 15 minutes)

HCl etch for passivation layer removal

- Etch sample for 45 seconds in solution of 5 mL HCl : 400 mL DI water; rinse in DI water and dry using N_2

Photolithography for lift-off

- Using a syringe and filter, apply S1818 photoresist to front of sample and wait for 5 minutes (to let the resist settle between nws); spin at 4000 rpm for 30 seconds; bake at 110°C for 2 minutes
- Align mask pattern corresponding to desired contact scheme and expose sample using 150 mJ/cm^2
- Immerse sample in toluene for 6 minutes; dry using N_2; bake at 90°C for 45 seconds
- Develop sample in MF319 for 75 seconds, gently agitating; rinse in DI water and dry using N_2

ITO sputtering

- Mount sample on sputtering stage using Kapton tape; sputter 2500 Å of ITO under 0.2 sccm O_2 : 36 sccm Ar flow at 130 W RF power and 5 mTorr chamber pressure (typical deposition rate of 1.6 Å / second)

Ni/Ge/Au electron beam evaporation

- Mount sample on e-beam evaporation stage using clips or Kapton tape; evaporate 250 Å of Ni, 500 Å of Ge, and 2250 Å of Au using accelerating voltage of 10 kV, beam current from 1.35 to 1.65 A (depending on target), and 5×10^{-8} Torr chamber pressure (typical deposition rate of 2.0 Å / second)

Al sputtering

- Place sample face-down on sputtering stage, being careful to protect the device on the front; mask edges using Kapton tape (to prevent any 'wrap-around' of the rear contact); sputter 4000 Å of Al under 20 sccm Ar flow at 90 W RF power and 5 mTorr chamber pressure (typical deposition rate of 1.1 Å / second)

Annealing

- Anneal sample in RTA at 400°C for 1 minute under N_2 flow

BHF etch for rear oxide removal on tandem junction cell

- Prior to application of rear contact, apply S1827 photoresist to front of sample; spin at 1000 rpm for 30 seconds; bake at 110°C for 2 minutes
- Etch sample for 6 minutes in solution of 20mL BHF : 200mL DI water; rinse in DI water and dry using N_2
- Strip photoresist and clean sample by immersing in acetone for 1 hour followed by IPA for 5 minutes; rinse in DI water and dry using N_2

BHF etch for oxide removal on silicon single junction cell

- Prior to application of rear and front contacts, etch sample for 6 minutes in solution of 20mL BHF : 200mL DI water; rinse in DI water and dry using N_2

9.2 Wafer Specifications

Standard silicon substrate

Specifications provided by *Virginia Semiconductor, Inc.*:

Diameter: 76.2mm ± 0.3mm
Orientation: <111> ± 0.9°
Dopant: Boron
Resistivity: ≤0.005 ohm-cm
Cz
Primary Flat Length: 22.22±3.17mm
Primary Flat Orientation: <110> ± 0.9°
Secondary Flat Length: none
Secondary Flat Orientation: none
Bow: <40µm
Center Thickness: 275µm ± 25µm
Total Thickness Variation (5 point measurement): ≤10µm
Surface: Single side polished, backside etched
Micro Roughness: ≤5Å
Edge Round: Yes
Thermal Oxidation Layer (Wet Process): None
Additional Thin Film Specifications: None
Laser Marking: None
Additional Cutting or Machining: None
COC Required: Yes
Measurement Data Required: None
Other Specifications: None

Tandem cell silicon substrate

Specifications provided by *The Institute for Solar Energy Research Hamelin*:

The wafers are (111) p-type FZ boron doped made by Wacker Siltronix, both sides are CMP. They state a thickness of 525 ± 25 µm. We measured the thickness of one wafer to be 553 µm. We made a marking on the "rear" side by use of a diamond pencil (this causes less damage than laser marking). "rear" means the not diffused side. We made a wet chemical cleaning (RCA, instead of $NH_4OH/H_2O_2/H_2O$ we used Piranha etch). We applied 150 nm of PECVD SiN (n = 1.9) on the rear side. After this we made the above mentioned RCA cleaning followed by a $POCl_3$ diffusion. We removed the PSG by 30-40 minutes 40% HF bath. Again above mentioned RCA cleaning followed by a dry thermally grown oxide of 38 nm on the diffused n-emitter and 30 nm on the p-type side.

The diffused emitter has a peak surface concentration of $N_{surface}$ = 6.5 $\times 10^{19}$ cm^{-3} and a sheet resistance of approximately R_{sheet} = 100 Ω/□. The junction depth is about 650 nm. We calculated the efficiency of this cell by assuming only optical losses by the top cell resulting in a short circuit density of j_{sc} = 19 mA/cm^2 and no other losses to η = 10.02%, V_{oc} = 628 mV, FF = 81.79. In the case of better surface passivation done by Corona charging of the surfaces: η = 10.77%, V_{oc} = 668 mV, FF = 84.89.