An Integrated Power Electronic System for Off-Grid Rural Applications

AN INTEGRATED POWER ELECTRONIC SYSTEM FOR OFF-GRID RURAL APPLICATIONS

BY

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To my family.

Abstract

Distributed energy is an attractive alternative to typical centralized energy sources specifically for remote locations not accessible to the electricity grid. With the continued advancement into new renewable technologies like solar, wind, fuel cell etc., off-grid standalone systems are becoming more attractive and even competing on a cost basis for rural locations. Along with the environmental and sustainable movement, these technologies are only going to get more and more popular as time goes on. Power electronic converters are also advancing which will help the shift in electricity options. Creating innovative power electronic systems will be important when moving toward smaller, more efficient and higher power density solutions.

As such, this thesis will aim to design and create an integrated power electronic system for an off-grid standalone solar application designed for remote rural locations with no access to electricity, or in locations which could benefit from such a system. It is designed for a DC input source from 24V-40V, such as a solar panel, and can operate four different loads; one 12V-24V 100 W DC load, charge a 48V battery, run three 5V cell phone charger outputs and run one 230V, 50Hz, 1 kW AC load. A boost converter, buck converter, phase shifted full bridge isolated DC-DC converter and a single phase inverter are implemented in the integrated system to achieve these outputs. A comparison of similar products on the market are presented and

compared with the proposed design by showing the product specifications, advantages and disadvantages of each.

A discussion of each converter in the system is presented and will include operation, design and component selection. An in-depth design process for the inductor within the boost converter is presented and will cover core, winding design and an optimization algorithm using the Genetic Algorithm (GA) is used to compare different ferrite based C-C shaped inductors. More specifically, the core material selected is Ferroxcube 3C97 and the inductor comparisons are between different Litz bundled windings from New England Wire Technologies and a customized rectangular winding. The GA optimizes around the lowest volume by comparing the different inductor designs using the different Litz winding constructions and the custom rectangular winding constriction. The rectangular winding achieves the lowest volume and will be compared with a three phase interleaved boost design implementing a CoilCraft inductor. The buck converter is the simplest converter and is designed using the traditional methods in literature. An in-depth design process for the phase shifted full bridge converter is also done wherein the zero voltage switching (ZVS) is achieved. The DC-AC inverter is the last converter designed within the integrated system and covers input capacitor sizing, and output filter design. There are specific distributed energy standards that must be followed when connecting loads to the system and so the purpose of the filter is to filter out the voltage harmonics. The control techniques for each converter is also discussed and shown to operate in both simulation and in experimentally.

The losses within the system are discussed and the required equations are defined so that a comparison between the experimental and simulated system can be made.

Indepth discussion on gate driver mosfet turn-on and turn-off operation is discussed, which is required for determining the switching losses. MATLAB/Simulink models are made for both the system level simulation in which the control and operation of the entire system is shown over three seconds, and also for individual converter simulations which model the losses to determine the converter efficiency over varying loads. These individual simulations are compared to the experimental tests to show the modeling accuracy. For the system level control, different loading powers and voltages are applied to see how the system reacts to real life expected changes that system would normally see.

A prototype of the integrated system is designed, manufactured and tested to verify correct operation of each converter within the system and to compare the estimated losses. A few challenges occured during the prototyping which is discussed in more detail in the following chapters, however, each converter will be tested at their full load conditions.

Acknowledgements

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Notation and abbreviations

CCM - Continuous Conduction Mode

PSFB - Phase shifted full bridge converter

GA - Genetic Algorithm

DC - direct current AC - alternating current

MPPT - max power point tracking

ESS - energy storage system

HV - high voltage

LV - low voltage

iGSE - improved generalized Steinmetz equation

i^2GSE- improved-improved generalized Steinmetz equation

MTL - mean turn length

AP - area product method

Kp - core geometry method

E - core width

D - core depth

WAW - window width

WAH - window height

Lg space - air gap space

NG - number of air gaps

Pos - wire row position

H - wire height

W - wire width

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Chapter 1

Introduction

1.1 Background and Motivation

Access to electricity is the main factor limiting the developing world today since it directly influences all aspects of life and living standards [1]. It has been shown that access to electricity allows students the opportunity to have a better education due to longer available hours spent studying at night or in low light conditions [2, 3]. It improves health by providing clean water and health services [2, 3]. It provides more free time by eliminating the need to gather resources for families since most families use fuels to power their homes [2, 3]. This applies even more to women who are typically the ones gathering resources for the family while the men earn the income. Eliminating the time spent gathering resources allows families to have both people earning for the family [2, 3]. Also, by improving the reliability of electricity access, businesses can make more electricity- dependent investments [2, 3]. In short, all around improved human development is attributed to access to electricity as shown in Fig. 1.1 [2].

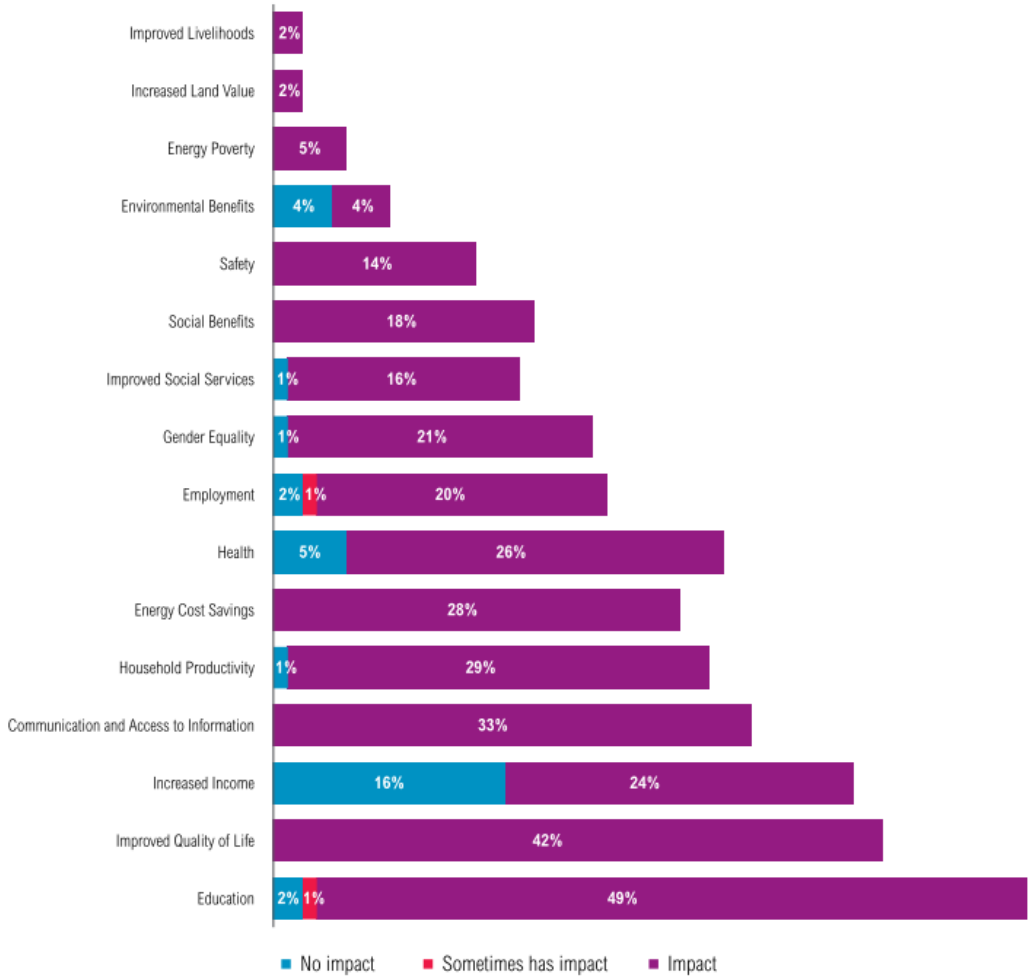


Figure 1.1: Impacts of Electricty Consumption for Households Reported in Literature [2]

	2009			2030		
	Rural	Urban	Share of population	Rural	Urban	Share of population
Africa	466	121	58%	539	107	42%
Sub-Saharan Africa	465	121	69%	538	107	49%
Developing Asia	595	81	19%	327	49	9%
China	8	0	1%	0	0	0%
India	268	21	25%	145	9	10%
Rest of developing Asia	319	60	36%	181	40	16%
Latin America	26	4	7%	8	2	2%
Middle East	19	2	11%	5	0	2%
Developing countries	1106	208	25%	879	157	16%
Wolrd*	1109	208	19%	879	157	12%

*Includes countries in the OECD and Eastern Europe/Eurasia

Figure 1.2: World population without access to electricity by region (millions) [6].

In Africa alone there are around 600 million people that have no access to electricity with most living in rural locations [4, 5]. The world population without access to electricity has been broken down by region in Fig.1.2 [6] and indicates that the

number of people without access will decrease over time, while more recent sources estimate that the number of people without access to electricity will continue to increase over the coming years [7, 8]. Either way, there will be a significant amount of people who will have no access to electricity so the question becomes, how best can this issue be solved? A renewable option would be the most ideal since it is sustainable and will also help fight climate change. However in reality, the most ideal and desired option is not always the most practical one since cost is usually the driving factor.

Traditionally, rural electrification is powered either by grid connection, distributed energy such as solar, wind or hydro, or through the use of biofuels like wood, oil or diesel with diesel being the most common off-grid option for rural locations [5, 7, 8]. Renewable energy options are gaining in popularity and will continue to do so as time goes on due to the advancement into energy storage technologies, improvements in power electronic converter efficiencies and energy resources like solar and wind. For example, the cost of solar has fallen by 80 percent and could continue to fall another 60 percent by the end of the decade [4, 9]. The efficiency of solar is also rising over the past 40 years [10]. 60 percent of the new energy generation is estimated to come from off-grid solutions [8] and there are estimated to be 730 million people that currently rely on biomass for their electricity needs in Africa, as discussed in [4, 5, 7], so the potential output for switching to a renewable alternative, like solar and wind, is vast. It is also important to mention that these locations which are energy deprived have a strong correlation with solar irradiation, meaning that there is a convergence for these locations to move toward a solar option due to the mentioned reasons above. Even though there may be locations in more developed countries which could benefit

from an off-grid application, this work is targeting those in developing countries which could benefit the most from electricity access.

Currently, the most common methods to provide rural and off-grid locations with electricity is to either extend the current electricity grid to reach these locations, use oil, wood or other biofuels to run generators, or by implementing distributed energy systems [4, 5, 8, 11]. Extending the grid has a lot of downsides in terms of cost, time and reliability. Rural locations are usually a bit harder to get to and extending the grid to these locations would require new roads, transmission lines, maintenance etc., and even those connected to the grid do not always receive reliable energy due to power outages, and typically the demand of electricity outweighs that supplied by the utility making grid extension a poor choice in some situations [4–12]. Oil and biofuels are the most common option, but again, getting these fuels requires time. Not to mention these options are not sustainable and contribute to global warming. Distributed energy has higher initial costs but it is sustainable, quick to implement, low maintenance, and does not require large transportation costs compared with the other methods [4–13]. These systems also provide reliable electricity by integrating multiple sources together.

A more in-depth analysis into the cost effectiveness of the available energy options in Africa are discussed in [11]. More specifically, this report comprises a cost comparison between grid extension versus diesel, solar, and other options for locations in Africa. The pricing level and subsidies each country has for each energy option are taken into account during this comparison as discussed in [11]. Fig. 1.3 to Fig. 1.5 show which energy method is most ideal for each location on a cost basis. The colouring indicates the locations where each option is best on a cost basis. Areas in

yellow are locations where solar is most ideal, brown shows locations where diesel is most ideal, red shows locations where solar or diesel are best, green indicates locations where solar and diesel are not ideal, orange indicates grid extension being best, and blue shows locations where both grid and either solar or diesel are the most attractive options [11].

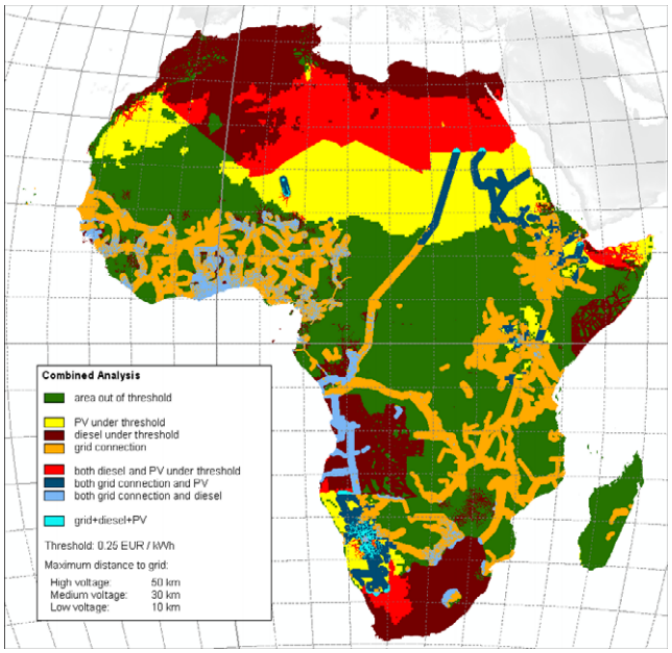


Figure 1.3: Geographical distribution of technologies with electricity costs lower than 25 c per kWh and conservative assumption on grid extension [11].

Fig. 1.5 shows the cost comparison for just solar and diesel where solar is in yellow and diesel is in blue. Refer to [11] for a more in-depth explanation, however the point to take from this analysis is that solar has a very large area where it is the most ideal energy source on a cost basis and is a viable alternative to the current energy options in these locations.

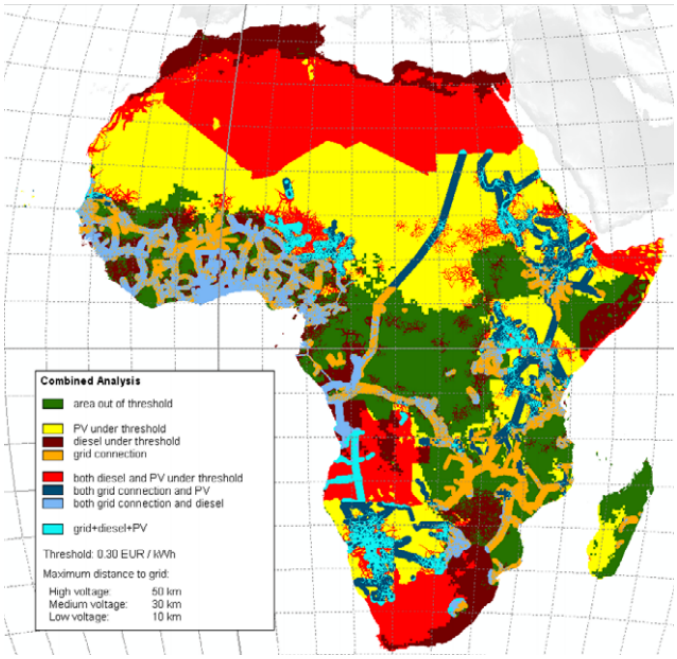


Figure 1.4: Geographical distribution of technologies with electricity costs lower than 30c per kWh and conservative assumption on grid extension [11].

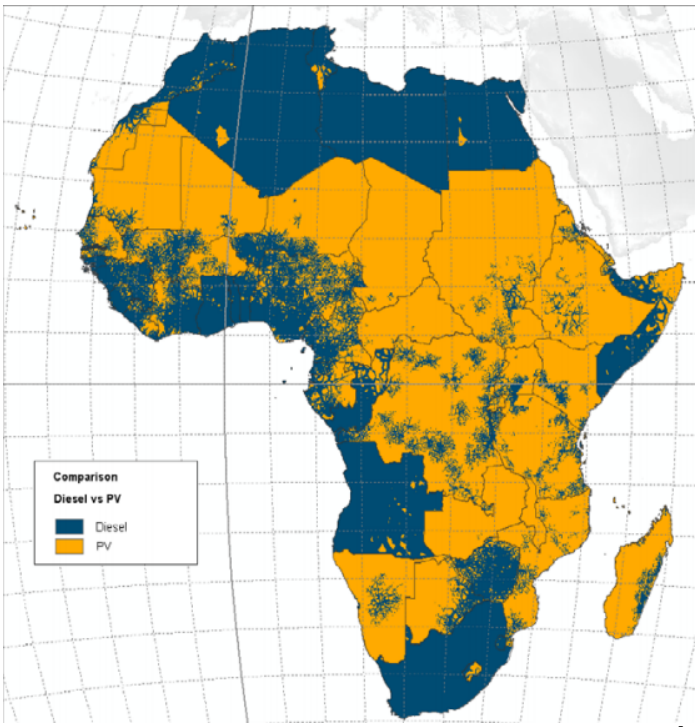


Figure 1.5: Economic Comparison of Diesel Versus PV [11].

Based on the presented information it was decided to design and create an integrated power electronic converter which can provide all the energy needs in these remote locations. This converter will have a DC input source which will provide energy to charge a battery system, multiple cell phone charging ports and it will also power one low voltage (LV) DC and one high voltage (HV) AC load. The DC and AC loading is dependent on the customer, although it was decided to provide 100W of DC electricity at either 12V or 24V and 1000W of AC electricity at 230V, 50 Hz. Note that, the proposed system is not strictly limited to applications in Africa as there are many locations around the world which can benefit from a distributed solar system such as countries in South America, the Middle East, and Asia.

1.2 Thesis Outline

The thesis mainly focuses on the design of each converter within the integrated system, with more detail regarding the inductor design of the boost converter as will be discussed.

Chapter 2 will be a literature review of related off-grid systems and past applications reviewing the type of systems available and the advantages and disadvantages of each.

Chapter 3 will go into the topology breakdown of different energy systems, discussing their advantages and disadvantages. Design concerns for each and a discussion about when certain topologies are more suitable than others for certain requirements or situations. The basic integrated topology will be selected and justified for this application.

Chapter 4 will go into the integrated converter design of each individual converter

within the system. A quick review on the operation of each converter, showing the typical waveforms and necessary equations for the design will be discussed, followed by the design and component selection. An in-depth design process for the inductor within the boost converter will be done. This will cover core and winding design, as well as implementing an optimization technique using the genetic algorithm (GA) in which the inductor is designed around the smallest inductor volume for different winding types. A comparison of these inductor designs will be done followed by the final selection of the inductor to be used. Another comparison between the custom inductor and an off-the-shelf inductor will be done to demonstrate the advantages the custom inductor provides. For the buck converter a simple design method using ripple requirements is used. The phase shifted full bridge (PSFB) converter design implements nest loops to arrive at the converter values. And lastly, a simple inverter design will be discussed involving the input capacitor design and output filter design based on the HVDC link ripple and output voltage harmonic respectively.

Chapter 5 will discuss the implemented control methods for both the simulation analysis, and experimental testing. A brief discussion on the most common and well known control methods implemented within power electronic converters will be discussed, followed by the implemented control method to be used for each converter. The required hardware will also be discussed which will cover the gate driver selection, DSP selection, current and voltage measurement sensors and circuits, and finally the designed PCB layout and manufactured PCB.

Chapter 6 will discuss component and converter modeling, simulation, and loss estimation. Each component within each converter will be modeled and the losses defined and calculated. The losses can be used to determine the efficiency of the

converter over varying load power. The system modeling will be done using MATLAB/Simulink and will first be simulated over a time range of 3 seconds while the input voltage, output buck voltage, output buck power and output AC power change. This will show the integrated converter being controlled over these applied changes. The efficiency will then be found for each converter over their respective load ranges to determine each converters efficiency map.

Chapter 7 will discuss the experimental testing and simulation comparison for each converter. Each converter will operate at their max powers to both validate the designed converters, and also to compare the experimental modeling to the simulated modeling. It will be shown that there were a few experimental issues with the PSFB converter and single phase inverter that will be discussed in more detail in their respective sections. However, after a few modifications, the tests will be complete at the full load conditions for each. A comparison between the designed inductor using the implemented GA inductor design, and an inductor off-the-shelf will be done. The GA based inductor will be shown to have lower total volume and losses when compared with the boost converter using an off-the-shelf inductor.

Chapter 8 finalizes the thesis with a conclusion on the work presented, and future tasks to be completed.

The main goals/targets of this work include:

- Design, simulate, build, and test a prototype for an off-grid standalone integrated power electronic system for a rural application
- Build and test each converter at its full load conditions and if possible, tests the entire converter operating together
- Create models which can be used to estimate system transients, waveforms and

predict losses

- Have a custom inductor design method which can be applied to future inductor designs. Show that the inductor design provides advantages over the traditional inductors available

Chapter 2

Review of Off-Grid System Products and Past Applications

There are many different products and technologies which provided solutions for off-grid distributed energy applications. These mainly fall into either portable or stationary systems or a mixture of the two [13]. Both can further be broken down into DC [14,15], AC [14–16] or a combination of the two known as hybrid systems [14–18]. For AC systems, there is a main AC bus which can be centralized or decentralize. Centralized systems have the main AC bus connected to the grid or load, while decentralized systems have each AC source connected individually to the grid or load. Centralized and decentralized systems can be applied in the same manner for DC systems, however the connection type is typically centralized due to simplicity [19, 20]. Hybrid systems can come in many different topologies either implementing a main DC bus connection, a main AC bus connection, or both an AC and DC bus connection [19,20]. For safety reasons, high voltage (HV) must have galvanic isolation from low voltage (LV), therefore, depending on the application; a variety of topologies

can be adopted. The following sections will go into portable and stationary systems and discuss details of each and their respective advantages and disadvantages.

2.1 Portable Applications

Portable systems almost always have a portable battery pack which is used to power either the DC or AC loads and are sometimes combined with solar panels or input ports that are connected with other DC or AC sources to recharge the battery. Some are designed for camping applications which can be carried by the user, while others are for off-grid homes which are heavy and require a trailer to move the system [13]. The off-grid systems can be considered stationary for the most part since they will not be moved in the same way the camping systems are. Therefore, the trailer systems will be considered stationary. A list of portable systems is found in [13] and a few others are shown in Table 2.1. These include EnerPlexs Generator 1200 solar generator, Be Prepared Solar, Wagan Tech Solar e Power Cube, PowerOak hand and home power products, Renogys Lycan PowerBox and Goal Zero Yeti 1250 Solar Generator. The internal circuitry of these products is unknown for the most part; however it appears most of these converters use a 12V DC to 120V AC inverter for either pure sine or modified sine wave output. The input charging capability is low so the charge times are quite long and it appears as if most are meant to run off of the battery pack and not through the input. Meaning the battery first needs to be charged for the system to run the outputs since the input power is not enough to operate all the loads at full power without the battery.

Table 2.1: Protable Off-Grid Products and Applications

EnerPlexs Generatr 1200 solar generator [21]:

- Input:
  - 4x Solar Panel DC Jack 16-34V, 120W Max
  - Wall Charger DC Jack 19V, 120W Max
  - 2x Anderson Jacks 12V, 120W Max
- Output:
  - USB, 12V, Standard AC Wall Outlet
  - 3x USB 2.4A/12V-10A, 120W max total
  - 12V Anderson- 10A, 120W max total
  - 19V- 6.3A, 120W max total
  - AC (3x)-100V AC 60Hz pure-sine wave 1000W Max total continuous (1100 Max over loading)

Wagan Tech Solar e Power Cube 1500 [22]:

- Solar controller 20A
- 1x 100Ah, 12V, 15A max continuous AGM/Gel hybrid Battery
- Input:
  - 2x 100V-240V AC charger 50/60Hz
  - 5x 16W solar panels (80W total), 17% eff, 20A max
- Output:
  - 2x 5V USB Outlet, 2.1A max
  - 2x 115VAC,60Hz 1.5kW continuous 3.6kW peak ac output, modified sine wave, 90% eff
  - 2x 12V DC outlet

Goal Zero Yeti 1250 Solar Generator [23]:

- 1200Wh, 100Ah, 12V AGM Lead Acid Battery
- Input Specs:
  - 120V AC Wall Charger (72W)
  - 12V Car Charger (30W)
  - 8mm Solar 16V-48V, 10A, 160W max
  - Power Pole 16V-48V, 20A, 240W max
- Output:
  - 3x 5V, 2.1A USB outlets
  - 8mm 12V, 10A, 120W
  - 12V, 33A Power Pole Port
  - 3x 110V AC, 60Hz, 1200W pure sine wave

Renogy's Lycan PowerBox [24]:

- 24Ah, 1075Wh, 12V Lead Acid Battery
- 20A Max power point tracking (MPPT) 1200W Pure Sine Wave Inverter
- Input:
  - Solar Panel
  - Wall Outlet
  - 12V Car Charger
- Output
  - 2x 12V DC
  - 3x 110V AC
  - 4x 2.4A USB

2.2 Stationary Applications

As discussed previously, stationary systems provide more power and are typically used for home or village applications, or as charging stations for different loads such as cell phone charging, repurposed automobile batteries or portable battery kits [13, 25] Stationary systems on the smaller side tend to be for home energy applications wherein a single home or a few homes use the same energy system [13, 25] They can also be in trailer systems, storage containers, or carts [13]. Larger systems fall into the micro grid category and can supply small villages or communities with their electricity needs if it is large enough [13, 18, 25]. In most cases these are hybrid systems that implement both AC and DC sources due to reliability since the base load requirement can be large. Typically these systems use AC sources such as diesel generators, wind turbines or hydro, while solar is used as DC supplies with battery storage. Some stationary systems are shown in Table 2.2 below and many others can also be found in [18, 25, 26]. Since this application is targeting small scale DC systems, AC and hybrid architectures will be ignored. Of the systems found in literature which fall into this category, the Sunblazer II and Universal Charge Controller, by IEEE Smart Village, is very similar to the system proposed herein as will be shown in Chapter 3. There is also a bit more documentation discussing the internal circuitry used for the universal charge controller discussed in [27] and shown in Fig. 2.1. The demo board DC2069A was used in this product as a proof of concept to show that the controller works and is able to charge batteries [28]. The demo boards solar input is from 17V to 54V volts and can go up to 200W [28]. This board is used to charge a 12V SLA battery with a max input charge current and output charge current of 10A and 16.6A

respectively.

Table 2.2: Stationary Off-Grid Products and Applications

Sunblazer II Unit [29]: • MPPT solar charge controller • Input: – 6x 300W solar panels – 4x 24/48V AGM/GEL batteries – 1000W AC input charger (Wind/Diesel) backup power • Output: – 10-20x 12V, 9-18Ah universal portable battery units – 1.5 kW AC 230V, 50Hz/60Hz	Smart Village Universal Charge Controller [27]: • Input: – 18V-24V solar panel – 45V-55V solar panel – 50V-60V DC microgrid – 24V Sunblazer-Lite or storage – 110/220 AC microgrid • Output: – 12V home battery – 12V appliances (fan, lights etc)
Leading Edge Power Box [30]: • 360Ah/24V battery with 24V/(10, 25, 50, or 70 A charger) • Input: – 2x 140W solar panels – 300-450W wind power – 187-265V/16A/45-65Hz AC input • Output: – 12V/9A and 24V/ 6A – 230V/16A AC output	Other Products/Manufacturers: • Tesla PowerWall [31] • SMA products [32] • Schnider electric products [33] • SolarEdge [34] • Enphase Energy [35] • ABB [36]

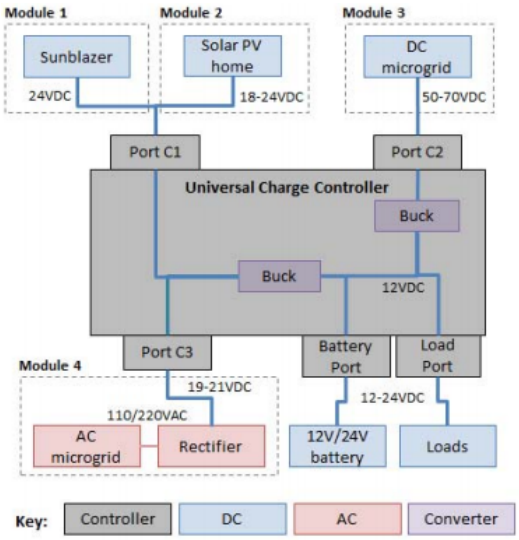


Figure 2.1: Smart village universal charge controller [27].

Figure 2.2: Sunblazer II unit [29].

The Sunblazer II Unit [29] is the other mentioned product by IEEE implemented in village applications. This is a solar charge station that consists of six 300W solar panels, four 24V or 48V batteries (AGM or GEL), solar charge controller using MPPT, ten or twenty charging channels for 12V 9-18Ah universal portable battery units, and the option to have both a 1000W AC input charger and a 1500W AC output load at 230V, 50 Hz or 60Hz as shown in Fig. 2.2. From the comparison discussed between portable and stationary systems, it was decided to design and build a prototype of

a stationary energy system using strictly DC sources. The main reason for making this a stationary system is because it has been reported as being more popular than portable applications by people who have used both systems in these remote locations. This is mainly due to the fact that people do not want to carry around a battery pack and would rather have the electricity closer to them [37]. The system will be very similar to the Sunblazer II Unit shown above and more detail will be discussed in the following sections.

This section covered different products and applications on the market which can be used to provide off-grid electricity. They typically fall into either portable or stationary wherein portable use battery packs to power the system while stationary can be powered using both energy storage or from the AC or DC sources. For this application the Sunblazer/Universal Charge Controller are the most similar products available to the application herein since both are stationary, both provide DC and AC power and both are in the 1kW range.

Chapter 3

Proposed Integrated Power Electronic System for Off-Grid Rural Applications

3.1 System Topology Comparison

From the discussion in Chapter 2 it was mentioned that this system will be targeting a strictly DC architecture. Therefore, the following section will discuss possible topologies for the proposed system which will lead to the overall topology selection. DC off-grid systems were mentioned previously and their topology selection comes down to the application and system structure. For this system, strictly DC sources will be targeted but DC and AC loads will be present. Topology and converter selection usually comes down to the voltage level since the converter ratio, along with other converter requirements, determine which converter type will be implemented. Higher conversion ratios in which low and high voltages are present usually require

galvanic isolation due to safety reasons. Thus, depending on the voltages of each component, isolated or non-isolated converters will be implemented.

Fig. 3.1 and Fig. 3.2 below show possible topologies for different voltage levels and desired bus levels. Red colouring indicates low DC voltage, green indicates high DC voltage, and blue indicates high AC voltage. It is assumed that the DC load is at low voltage for all topologies since most DC loads are at low voltages (5V, 12V, 24V, 48V), while AC loads are designed to work with the current electricity grid in most countries (110V-120V 60Hz or 220V-240V 50Hz). Most developing countries use 220V-240V 50Hz so it is assumed that the AC load for this system will be 230V 50Hz. This leaves the DC sources and Energy Storage System (ESS).

The ESS must have bidirectional operation due to charging and discharging so a bidirectional converter must be used for the ESS. Since this is an off-grid/standalone application, there will be no grid connection and so the ESS must be charged using the supply. It will also be assumed that isolated converters will have more losses than non-isolated converters due to the additional losses attributed to the transformer winding and core material. Fig. 3.1 shows three different classes of topologies incorporating a single bus. Fig. 3.1 a shows the topology for a single AC bus in which all the sources are connected individually to it, either through isolated or non-isolated converters depending on the voltage of each. If a main LVDC or a HVDC bus is desired then Fig. 3.1b and Fig. 3.1c will be used. Fig. 3.1b and Fig. 3.1c are more common than Fig. 3.1a if only one AC load is present, or if there are multiple DC loads and/or sources since the AC load can be connected without the use of an AC bus, and if there are multiple DC loads/sources then it makes more sense to connect them to a DC bus rather than using Fig. 3.1a which would require the power to first be converted

to AC then back to DC.

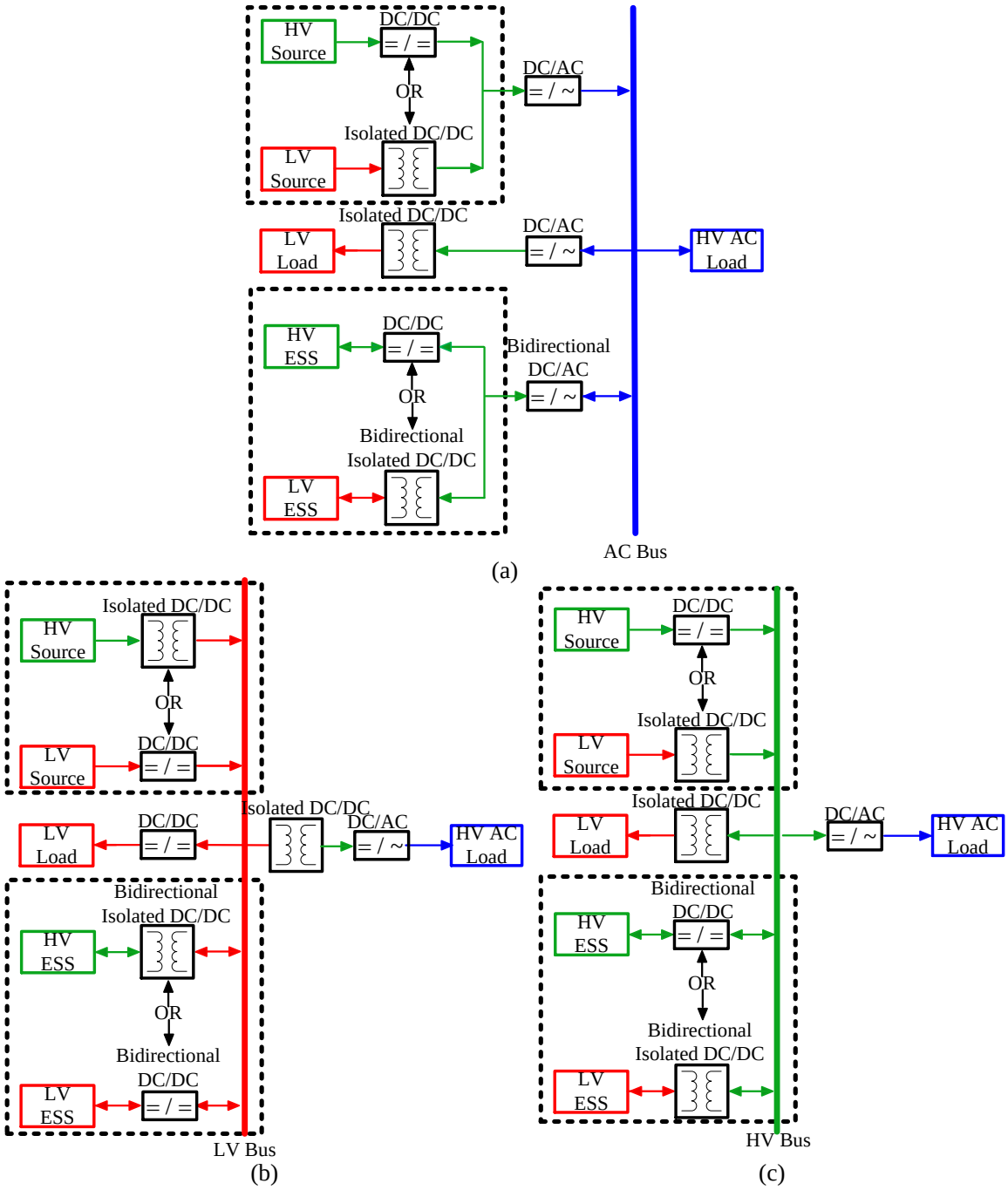


Figure 3.1: Single bus topologies (a) single AC bus (b) single HV DC bus (c) single LV DC bus.

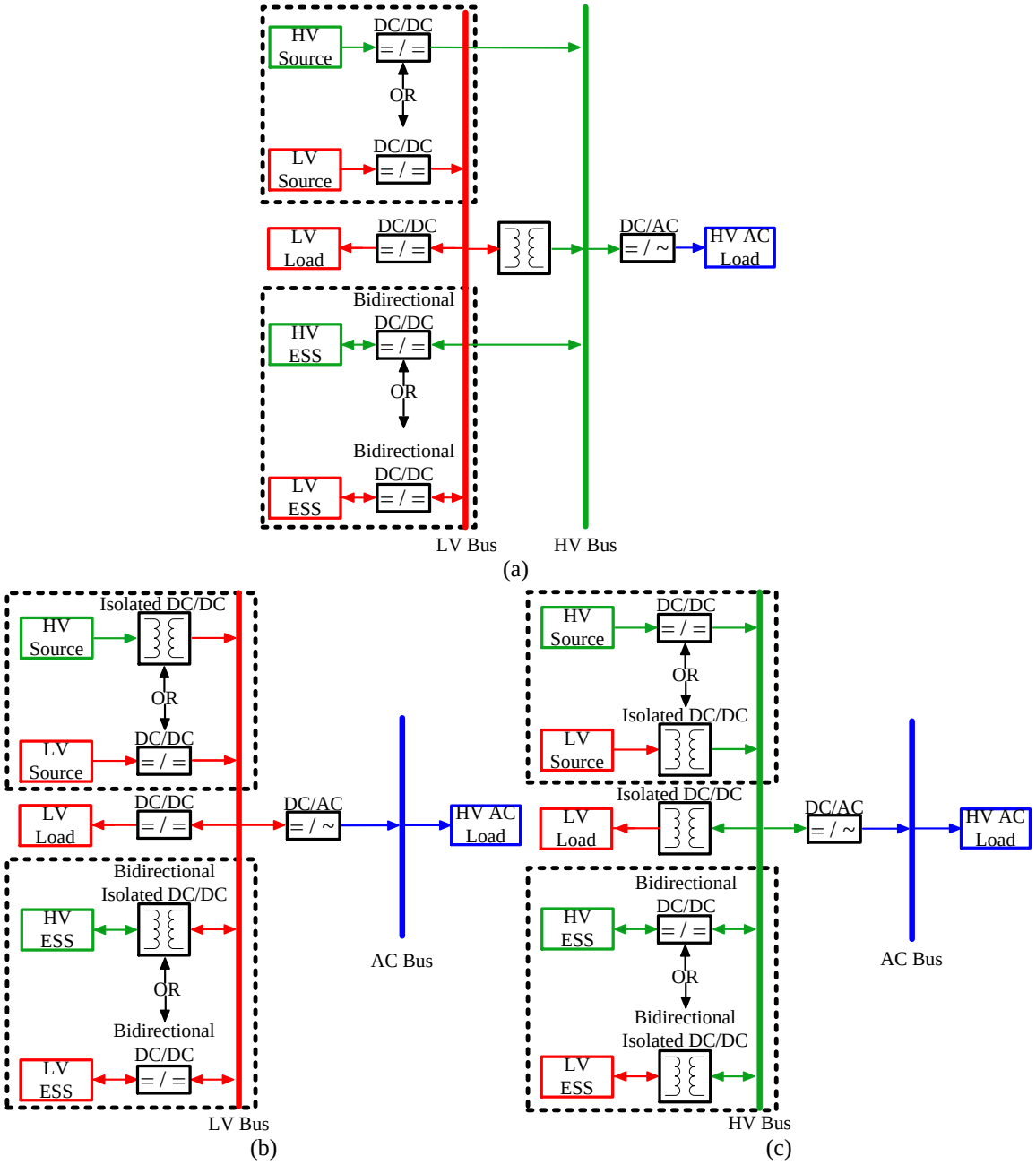


Figure 3.2: Double bus topologies (a) LVDC and HVDC bus (b) LVDC and HVAC bus (c) HVDC and HVAC bus.

Fig. 3.2 shows topologies implementing two buses using either HVDC and HVAC, LVDC and HVAC or both HVDC and LVDC. If there is only one AC load then there

is no point to have a main AC bus unless there are multiple AC loads and/or sources. Therefore, Fig. 3.1b, Fig. 3.1c and Fig. 3.2a are ideal for topologies with only one AC load, while topologies Fig. 3.1a, Fig. 3.2b, and Fig. 3.2c are ideal for multiple AC loads and sources. This application is targeting off-grid DC sourced applications with no AC sources and no grid connection, so topologies in Fig. 3.1b, Fig. 3.1c and Fig. 3.2a are the most applicable.

When deciding between topologies, influence will be dictated by which topology has fewer conversions and which topology has fewer isolated converters, assuming isolated converters have higher losses. Since most DC loads are 5V, 12V, 24V, or 48V, the voltage range of the first DC load will be 12V-24V and the second DC load will be for cell phone charging which is 5V. As mentioned previously, the mains voltage for most developing countries is between 220V-240V so the AC voltage will be 230V at 50 Hz. The DC source and DC ESS voltages are the main variables in the decision between topology selection since they can be low or high voltage. Therefore, topologies in Fig. 3.1b, Fig. 3.1c and Fig. 3.2a are ones that are more applicable for this system. There are four different possible combinations for the DC source and ESS for each of the three topologies: HVDC source and HVDC ESS, HVDC source and LVDC ESS, LVDC source and HVDC ESS and finally LVDC source and ESS. There are a few advantages and disadvantages for going with either high voltage or low voltage DC source and DC ESS. Higher voltages result in lower currents and would also introduce non-isolated conversion from the source to the AC load, however isolation would still be required between the low voltage DC loads. One advantage for selecting low voltage is that parallel connection is less problematic than series when faults arise and it is safer to do maintenance at lower voltages. Also, most batteries

on the market are around 12V, 24V, or 48V so a low voltage battery would be easy to apply. As such, for the proposed integrated system, the DC source will range from 24V-40V, there will be three cell phone charging ports at 5V each, a low voltage DC load from 12V-24V and a high voltage AC load at 230V 50 Hz. Most developing countries have mains voltages between 220V-240V operating at 50Hz so this is the reason for selecting the voltage and frequency. As such, the topology in Fig. 3.3 will be targeted for the integrated system.

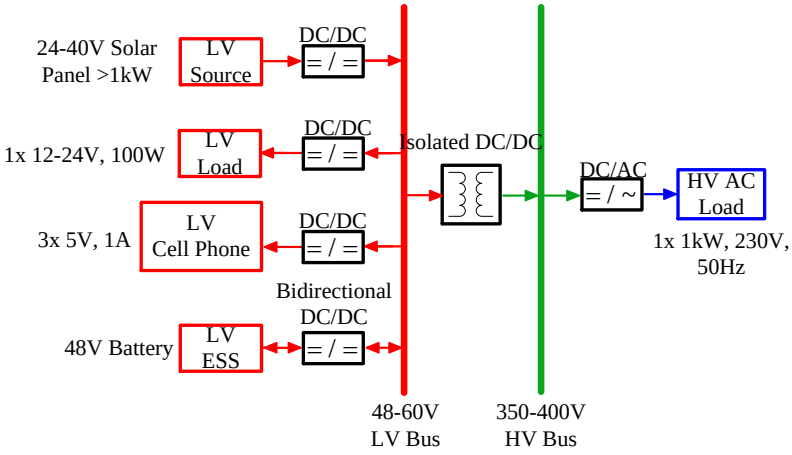


Figure 3.3: Proposed standalone off-grid integrated power converter system topology.

3.2 Proposed Integrated Converter

Based on the desired topology show in Fig. 3.3, the first DC-DC converter connecting the 24V-40V source to the 48-60 LVDC bus will need to be some form of non-isolated boost converter. The basic single phase boost converter will be adequate, however moving to higher number of phases helps with reducing the phase current, input and output current and voltage ripples, at the expense of adding more complexing, cost and reduced reliability. Section 4.1 will go into the boost converter

design in much more detail.

The second DC-DC converter connects the 12V-24V load to the 48V-60V LVDC bus, however the power flow is from the 48V-60V LVDC bus to the load so this will need to be a non-isolated buck type converter. This converter is meant for a power load in the range of 100W so a single phase buck converter should work based on these requirements. It is simple and easy to control as well. Section 4.2 will go into more detail regarding the buck converter design.

The third converter connects the 48V-60V LVDC bus to three 5V cell phone USB ports for cell phone charging. This conversion ratio is larger than four times so isolation will be required. There are many off-the-shelf converters which can meet this requirement while also being cheap and having a low footprint. As such, the design of the cell phone charging converter will not be discussed because it is quite easy to buy a converter off-the-shelf so it will be done herein.

The fourth DC-DC converter connects the battery system to the LVDC bus so this will need to be a non-isolated bidirectional boost converter. However, for this work, the design of the bidirectional converter is beyond the scope of this work so it is assumed that an ESS will be connected to the LVDC bus using an off the shelf battery system since most battery systems come with their own charge controller.

The fifth converter is meant to convert the 48V-60V LVDC link into the 350V-400V HVDC link. This ratio is quite large so isolation will be required. Selection of the isolated converter can be challenging since there are many different possible topologies, with varying adjustment made to each, with the goal to improve the performance and efficiency [38, 39]. The standard primary topologies include, forward,

flyback, push-pull, half bridge and full bridge. The switch, inductor, diode and capacitor voltage and current waveforms of these converters are discussed and shown in [40] so they will not be shown here.

The flyback converter is the simplest isolated DC-DC converter and is basically an isolated version of the non-isolated buck-boost converter. It uses only one switch and one diode within the circuit, resulting in lower costs compared with other isolated topologies. However, this converter is usually used for lower power applications due to the high voltage and current stresses seen by the device at high powers. It also has poor transformer core utilization since only one quadrant is used. Because of this, the core size will need to be larger than other isolated topologies which use both quadrants of the core. As such, it requires a reset circuit due to core saturation issues attributed to the single ended use of the BH curve [40].

The forward converter is similar to the flyback in that it is simple, uses one switch, single ended, but it is mainly used for low power applications since it also suffers from the same issues mentioned for the flyback [40, 41].

The push-pull converter has double the switching voltage stress on the primary side versus the half and full bridge converters because there is only one switch on the primary side. One disadvantage of the push-pull converter is the flux imbalance of the transformer due to DC current in the primary [40].

The full bridge and half bridge topologies are more ideal and much more popular in literature than the flyback, forward, and push-pull converters. They do not have the transformer utilization issue, resulting in a smaller transformer cores for the same power level. However, the cost will be higher due to the increased amount of switching components. The voltage and current stresses are also lower, depending on the

conversion ratio.

This application is targeting 1kW loads so the push-pull, half and full bridge topologies are the most ideal with the half and full bridge being more ideal as the power level increases. The full bridge converter has an advantage compared with the half bridge for a few reasons. First, the output current of the full bridge is half as large as the half bridge for the same power requirement and the same input voltage making the conduction losses lower. Using equations (3.1) and (3.2) we can compare the conduction losses of the full bridge and the half bridge; assuming the same input voltage, output power and on resistance of the switching devices. As can be seen, the conduction losses of half bridge will be twice as high as the full bridge.

$$P_{HB} = 2R_{ON}(I)^2 \tag{3.1}$$

$$P_{FB} = 4R_{ON}\left(\frac{I}{2}\right)^2 = R_{ON}(I)^2 \tag{3.2}$$

A further improvement to the traditional full bridge converter is by using the phase-shifted full-bridge converter (PSFB) and gains an advantage due to the zero voltage switching. By implementing a phase shift between legs of the full bridge converter, the output capacitors of the MOSFETs discharge and the anti-parallel diodes conduct prior to MOSFET gate turn-on resulting in zero voltage switching (ZVS). However, there is a range in which ZVS can be accomplished as will be shown in section 4.3. There are other advancements that have been made to the traditional PSFB converter in literature, either through the use of external auxiliary circuits [42], or the addition of leakage inductance and blocking capacitors [42]. These are grouped into resonant converters which help in achieving ZVS and zero current switching (ZCS). Since this converter is unidirectional, the secondary side does not need to be active so a

standard rectifier can be implemented. The center tapped rectifier is suited for low output voltage because only one diode conducts while the full wave rectifier has two conducting which means double the voltage drop. The voltage stress will be lower for the full wave because the voltage stress on the diodes is half that of the half wave rectifier. Therefore, for high output voltage, low output current applications the full bridge rectifier is a better choice while for low voltage high current the half wave is better. As such, the PSFB converter using the full wave rectifier will be discussed and designed in section 4.3.

The last converter is the DC-AC converter which will run the AC loads. There are different types of inverters ranging from single phase up to three phase, multiphase systems and more complex topologies [43,44]. For this application the input is 350V-400V and the output is a 1kW, 230V 50Hz load. Therefore, a single phase inverter will be adequate to meet these requirements. Section 4.4 will go into the design of the DC link capacitor, and the output filter design. 50 Hz was selected because this application is targeting third world countries which usually have 50Hz, but this system can easily be changed into 60Hz.

From the discussion above, the proposed topology for the off-grid integrated converter is shown in Fig. 3.4 with the converter specifications in Table 3.1. The proposed system is designed to operate using either the solar input port or an energy storage system, ideally a battery pack. Meaning the solar input can provide all the required energy without the need to charge the battery first. This system is closer to what is used in an actual off-grid home application wherein the ESS is charged during the day and used at night. Once the ESS is fully charged, the input can still provide energy and power the loads. The advantage of this system over other similar systems is that

it is integrated incorporating multiple converters in one, by integrating the converters they can share input and output capacitors reducing the number of components, it is designed to provide continuous power at 1kW and can power different DC loads. The proposed system is more suited for a home system, however the possibility to use it as a battery charging station is available.

Table 3.1: Integrated Converter Specifications

Converters	Boost	Buck	PSFB	Inverter
Input Voltage (V)	24-40	48-60	48-60	330-450
Output Voltage (V)	48-60	12-24	330-450	230
Ripple Current (A)	<=40% Io	<=40% Io	<=10%Io	<=40%Io
Ripple Voltage (V)	<6%Vo	<=5%Vo	<=5%Vo	<=5%Vo

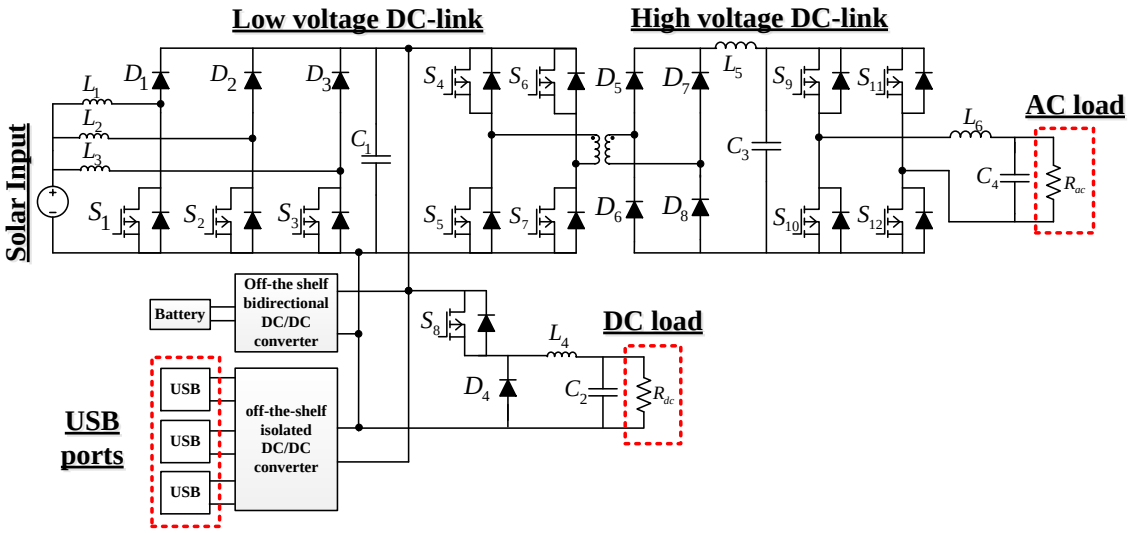


Figure 3.4: Proposed standalone off-grid integrated power converter system for rural applications.

This chapter discussed possible topologies for the proposed integrated off-grid system. The topologies are broken down into single or double bus topologies in which it is assumed there is a low voltage DC load and a high voltage AC load. The DC source and energy storage system can either be high voltage or low voltage. The

system is designed for three cell phone chargers at 5V/1A each, one 12-24V/100W DC load, one 230V/1kW/50Hz AC load, while the ESS is assumed to be connected with its own battery charging system. The DC load and ESS can either be high voltage or low voltage. Low voltage was selected because it is safer and because the power is only 1kW so the currents are small. For a higher power system the current will be larger so higher voltages will help to reduce the losses. Each converter within the system was then selected based on the specifications and the final integrated circuit shown.

The following sections will discuss the various converter topologies, their operation, and how to select the components based on voltage and current ratings.

Chapter 4

Design of Integrated Power Electronic System

This section will go into the design of each individual converter within the integrated system. This will include an overview of each converter and its waveforms if required, the converter design, and component selection.

4.1 Boost Converter

4.1.1 Boost Converter Overview

The first converter within the integrated power converter system is the boost converter. It is used to boost the input from 24V-40V, up to 48V-60V. For off-grid applications this DC source could be solar panels, fuel cells or a large battery bank. However, as was discussed previously, this converter is ideally for a solar powered system. Fig. 4.1 shows the single phase boost converter, where the inductor current

and voltage waveforms are shown in Fig. 4.2 and Fig. 4.3 respectively, assuming steady state continuous conduction mode (CCM). Using these waveforms the change in inductor current is described in (4.1) for both the on and off times of the bottom switch. During DT, the lower switch is turned on and current flows through the inductor which causes the current to rises as energy is stored in the magnetic core of the inductor shown in Fig. 4.2, while during turn-off time D^*T the current flows into the output capacitor. Equating the on and off times in (4.1), the duty cycle can be found as shown in (4.2). The duty cycle can also be described by (4.3). From Fig. 4.2 the peak and rms currents are found in (4.4) and (4.5) respectively.

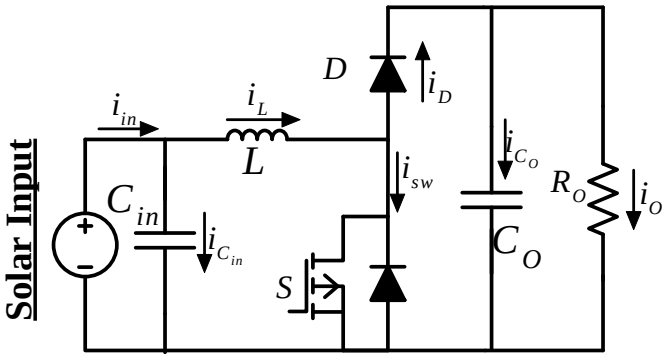


Figure 4.1: Boost converter circuit.

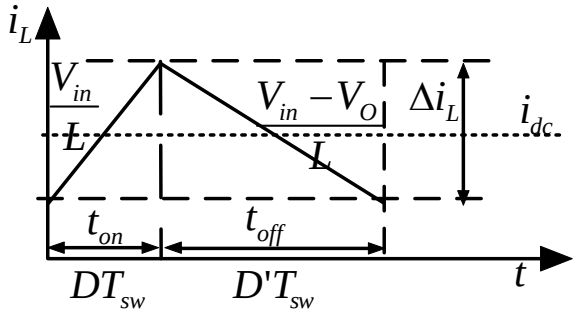


Figure 4.2: Boost converter inductor current waveform [40],[45].

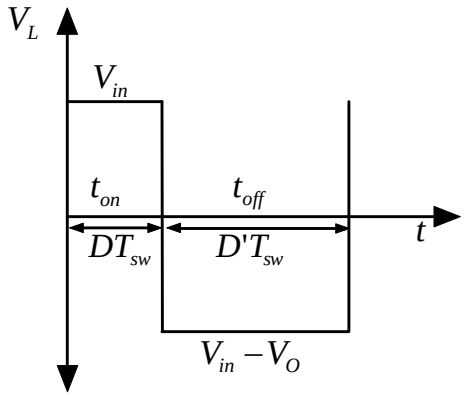


Figure 4.3: Boost converter inductor voltage waveform [40],[45].

$$\begin{cases} \dfrac{DV_{in}}{Lf_{sw}} = \Delta i_L & t_{on} \\ \dfrac{D^*\left(V_o - V_{in}\right)}{Lf_{sw}} = \Delta i_L & t_{off} \end{cases} \tag{4.1}$$

$$\frac{\left(1-D\right)\left(V_o - V_{in}\right)}{Lf_{sw}} = \frac{DV_{in}}{Lf_{sw}} \rightarrow D = 1 - \frac{V_{in}}{V_O} \tag{4.2}$$

$$1 = D + D^* \tag{4.3}$$

$$I_{L,\max} = I_{DC} + \frac{\Delta i_L}{2} \tag{4.4}$$

$$I_{L,rms} = I_{DC} + \frac{\Delta i_L}{\sqrt{12}} \tag{4.5}$$

During the on and off times the capacitor current also goes through a change, as shown in Fig. 4.4 where ΔQ is the amount of charge accepted by the capacitor for both the on and off times. The general equation for calculating the capacitance is then found from (4.6) and is further developed into (4.7) in relation to Fig. 4.4. The rms current in the capacitor is described by (4.8). For the input capacitor, the current waveform is shown in Fig. 4.5 and using the same method as was done for the

output capacitor, the input capacitance can be found by finding the amount of charge accepted by the capacitor, leading to (4.9) with an rms current in (4.10) [40, 45].

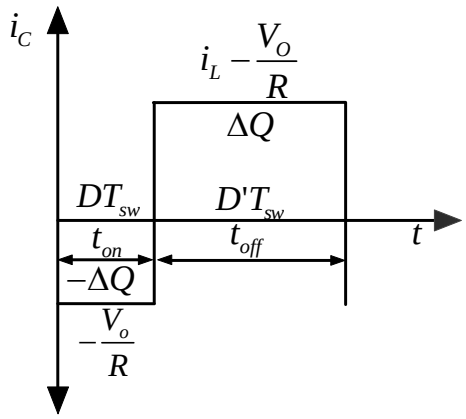


Figure 4.4: Output capacitor current waveform [40],[45].

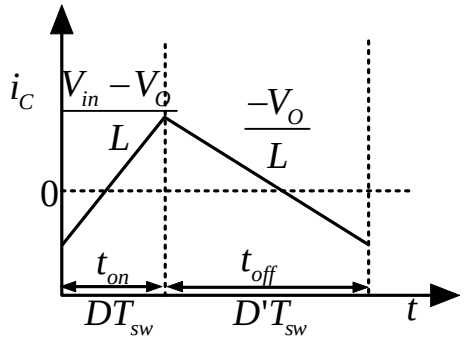


Figure 4.5: Input capacitor current waveform [40],[45].

$$\begin{cases} \dfrac{-DV_O}{CRf_{sw}} = \Delta V_C & t_{on} \\ \dfrac{D^*\left(I_L - \dfrac{V_O}{R}\right)}{Cf_{sw}} = \Delta V_C & t_{off} \end{cases} \tag{4.6}$$

The peak currents for the MOSFET and the diode are the same as the peak current for the inductor, however the rms current for the MOSFET is estimated from (4.11) while the diode rms is estimated from (4.12). Table 4.1 shows the voltage and current ratings for each component within the boost converter. When selecting the components these ratings must be satisfied. For a more in-depth explanation, refer to [40]

and [45].

$$C = \frac{\Delta Q}{\Delta V_c} \rightarrow C_O = \frac{I_{out} D_{on}}{f_s \Delta V_c} \tag{4.7}$$

$$I_{C_O,rms} = I_O \sqrt{\frac{D}{1-D}} \tag{4.8}$$

$$C_{in} = \frac{\Delta i_L}{8 f_{sw} \Delta V_{C_{in}}} \tag{4.9}$$

$$I_{Cin,rms} = \frac{\Delta i_L}{\sqrt{12}} \tag{4.10}$$

$$I_{M,rms} = I_{in} \sqrt{D} \tag{4.11}$$

$$I_{D,rms} = I_{in} \sqrt{1-D} \tag{4.12}$$

Table 4.1: Boost Converter Component Ratings

Component	Voltage Rating	Current Rating
Inductor	$V_{L,peak} = V_{O,max} - V_{in,min}$	$I_{L,peak} = I_{dc} + \frac{\Delta i_L}{2}, I_{L,rms} = I_{dc} + \frac{\Delta i_L}{\sqrt{12}}$
Switch	V_O	$I_{M,peak} = I_{dc} + \frac{\Delta i_L}{2}, I_{M,rms} = I_{in}\sqrt{D}$
Diode	V_O	$I_{D,peak} = I_{dc} + \frac{\Delta i_L}{2}, I_{D,rms} = I_{in}\sqrt{1-D}$
Output Capacitor	V_O	$I_{C,rms} = I_o \sqrt{\frac{D}{1-D}}$
Input Capacitor	V_{in}	$I_{C,rms} = \frac{\Delta i_L}{\sqrt{12}}$

4.1.2 Design of Boost Converter

The requirements in Fig. 3.4 state that the input voltage will range from 24V-40V, inductor current ripple will be 40 percent and the output and input voltage ripples will be 6 percent for each while the range on the low voltage DC link bus is

from 48V-60V. If an efficiency of 90 percent is assumed as the worst case efficiency for each converter, the input power required would be 1371.7W. The output power of the boost converter would then be 1234.57W. Ideally the efficiency should be greater than 95 percentage for each converter but some extra margin will be provided in the design.

The worst case input current occurs for the highest conversion ratio, which in this case occurs for an input voltage of 24V and an output voltage of 60V giving a duty cycle value of 0.6, when using (4.2), and an output DC current of 20.57A. The input peak current is found from (4.4) and is 55.56A, assuming CCM, while the ripple current is 8.23A when applying the 40 percent output current ripple requirement. Based on this worse case condition, the calculated inductance is found from (4.1) and is $17.5\mu H$. This is actually the minimum required inductance because if the inductance increases then the ripple will decrease and the max current the inductor and switches will see will also decrease a bit.

Using (4.7), the minimum required output capacitance is $44.6\mu F$, assuming an output voltage ripple of 6 percent, input voltage of 24V, output voltage of 48V and a switching frequency of 100 kHz. The rms current flowing through the output capacitor is found from (4.8) and is 25.7A. The input capacitor value is found from (4.9) while its rms current is found from (4.10). For an input voltage of 24V and an output of 60V, the calculated capacitance and rms current are $7.15\mu F$ and 2.38A respectively.

4.1.3 Inductor Design

The inductor is one of the main components within any power electronic converter. Depending on the application, the inductor can be large, costly, lossy and heavy when

comparing it to other components. Therefore, any method which can improve its design is ideal. In general, low volume, low cost, and high efficiency are all ideal qualities, however not all of these can be accomplished and usually it depends on the application and specifications. Therefore, some designs will be more advantageous over others. Such is the case for electric transportation where design constraints are very strict when it comes to volume, weight, and cost. Vehicle applications are also one of the more intense and hash environments for electronics to be in since the temperature can change drastically depending on geographical location. The size constraint for the application herein does not have to be as strict as it would be for an EV/PEV application, but it is always ideal to optimize the design as much as possible.

Inductor design covers a wide variety of design techniques ranging from simple methods using the area product (A_P), core geometry methods (K_g), and more complex methods implementing optimization techniques [45, 46]. For this work, an optimization technique involving the genetic algorithm (GA) will be used to design the inductor within the boost stage of the integrated off-grid converter. This design method can be applied to any inductor within the system, although, it was only applied to the boost converter due to the large inductor currents. As will be discussed, this design method is also advantageous due to its scalability since it can be used for designs of varying power levels. This design is more customizable and only requires the inductance, current and frequency specifications.

The following sections will first lay out the ground work for the optimization by giving an overview of the core and winding design. The core design will touch on material selection, core geometry, magnetic equations and core losses while the

winding design touches on the wire selection and winding losses. Both core and winding designs are interdependent on each other, and require some iteration to arrive at a final design. Because of this interdependence, implementing an optimization method helps with speeding up the design by efficiently designing multiple inductors and applying the appropriate design constraints to see if the designs work.

4.1.3.1 Core Design

There are many different core materials with some being better suited than others for different designs. The main core materials fall into powder, ferrite, steels, and magnetic glass cores [47, 48]. A great comparison between core materials is discussed in [48] in which different core materials are compared using the A_P method over a frequency range from 20-150 kHz operating at varying current ripples. Typically ferrite is used at high frequencies due to its lower core losses compared with other core materials. Ferrite is also cheaper than most other magnetic core materials as well. However, for applications implementing cooling, the advantages of ferrite diminish as shown in [48]. One of the main reasons why is because ferrite has low thermal conductivity and does not transfer heat as well as other core materials. This makes ferrite more temperature sensitive and limits its performance due to overheating. Most ferrites have their lowest core losses between $100°C$ to $140°C$ although the magnetic performance isn't as good as ones with lower temperatures. The magnetic performance begins to degrade for temperatures beyond this point. While for other non-ferrite material, their temperature performance is better making them a more attractive option and can be as high as $180°C$ to $200°C$ range [48]. This advantage can play a role when volume is the main target since a smaller volume will have less

surface area, resulting in less area for heat dissipation, which effectively increases the temperature. This is even more advantageous for situations where the inductor loss is small in comparison to other losses within the converter. The converter efficiency is limited by the component which generates the majority of the losses. If the inductor produces more losses from non-ferrite materials but this loss is still smaller in comparison with other losses within the converter, the inductor can be smaller without a big concern for the overall converter efficiency. [49] is an example of this exact situation wherein the inductor losses are smaller in comparison with the rest of the converter losses. However, for this application, the power is only around 1-1.5kW so the inductor design should aim for the best efficiency and lowest volume making ferrite more ideal on a loss basis.

Unfortunately, ferrite has low flux density in comparison to other core materials so to improve its performance to compete with these other core materials, discrete air gaps must be added to the flux path. Adding an air gap to the magnetic path effectively shifts the BH curve to the right, allowing more energy storage since the core now saturates at a higher current, although it will still saturate at some level [47]. Adding an air gap also introduces fringing effects which will cause extra losses, while also increasing the magnetic flux which could saturate the core prematurely. Typically to mitigate the fringing effect the air gap is split into smaller gapes which minimizes the fringing effect [47].

Fig. 4.6 shows the power loss density versus temperature for different ferrite core materials operating at a flux swing of 0.2 tesla. The core loss data for these materials is shown in Table 4.3 while Table 4.2 shows the core saturation values at $100°C$ for each core material. This temperature was selected because Fig. 4.6 indicates that

most of the core materials achieve their minimum power loss around $100°C$, with a few being either higher or lower. This data was gathered from the Ferroxcube and Hengdian Group DMEGC Magnetics websites and through communication with their employees. Comparing both the core losses and the saturation values, 3C97 appears to be the best material with 3C95 being a very close second. They both have the same core saturation at $100°C$ so the selection will come down to the designer and cost. For this analysis, 3C97 will be selected and used within the GA design process as will be discussed in the following sections.

Table 4.2: Saturation Flux Density of Different Ferrite Cores at 100^oC

Core Material	3C90	3C91	3C92	3C93	3C94	3C95	3C96	3C97	DM90
Saturation Flux Density (T)	0.38	0.37	0.46	0.43	0.38	0.41	0.44	0.41	0.45

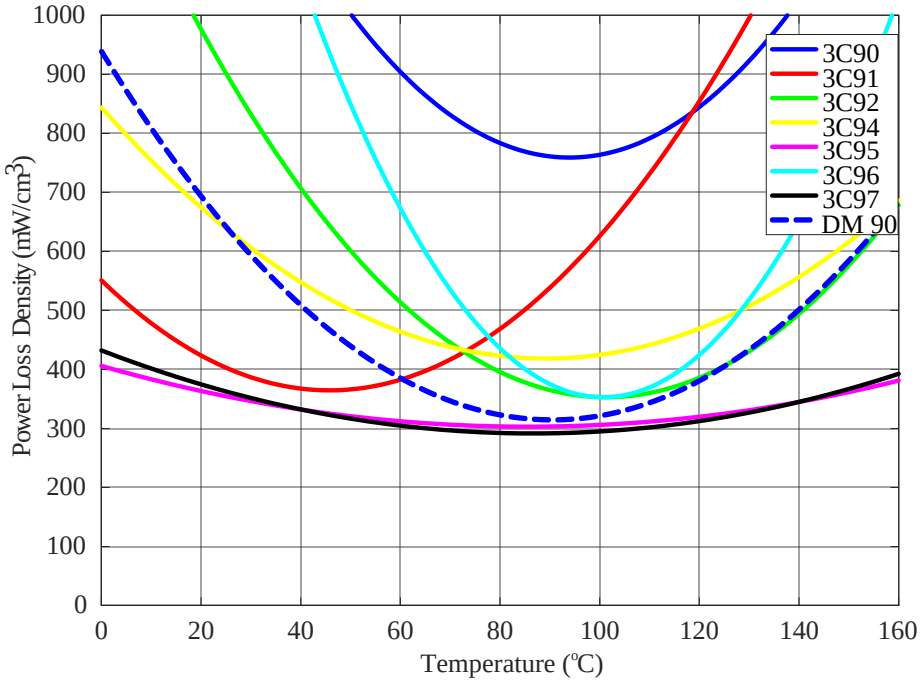


Figure 4.6: Core loss material comparison at 0.2T 100kHz.

Table 4.3: Ferrite Core Loss Data for DM90 and 3C97

$P_{DM90} = C_m f^x B^y \left(Ct_o - Ct_1 T + Ct_2 T^2\right)$ where f is in kHz, B is in mT, $P_{DM90}$is in mW/cm^3 and T is in $°C$

$P_{FXC3C97} = \frac{C_m f^x B^y \left(Ct_o - Ct_1 T + Ct_2 T^2\right)}{1000}$ where f is in Hz, B is in T, $P_{FXC}$is in mW/cm^3 and T is in $°C$

Material	Freq (Hz)		Cm	x	y	Ct2	Ct1	Cto
	Min	Max						
3C90	20	200	3.2	1.46	2.75	1.65e-04	0.031	2.45
3C91	10	100	3.5	1.4	2.5	1.42e-04	0.013	0.88
3C91	100	200	3.5	1.4	2.5	1.42e-04	0.013	0.88
3C91	200	400	3.33e-14	4.05	2.5	1.42e-04	0.013	0.88
3C92	20	100	26.52	1.195	2.65	2.68e-04	0.054	3.754
3C92	100	200	0.349	1.59	2.675	1.51e-04	0.0305	2.548
3C92	200	400	1.19e-04	2.245	2.665	2.08e-04	0.0437	3.29
3C94	20	150	3.53	1.42	2.885	1.25e-04	0.0223	1.973
3C94	150	400	5.88e-04	2.125	2.705	1.17e-04	0.0233	2.161
3C94	400	>400	2.10e-06	2.6	2.75	1.65e-04	0.031	2.45
3C95	20	150	92.166	1.045	2.44	4.62e-05	7.94E-03	1.332
3C95	150	300	7.47e-03	1.955	3.07	6.06e-05	0.0126	1.654
3C95	300	400	7.87e-04	2.055	2.535	9.55e-05	9.78E-03	1.023
3C96	20	100	5.121	1.34	2.665	5.48e-04	0.11	6.563
3C96	100	200	8.27e-03	1.72	2.805	1.83e-04	0.0366	2.827
3C96	200	400	9.17e-05	2.22	2.465	2.33e-04	0.047	3.392
3C97	20	150	42.366	1.16	2.8	6.36e-05	0.011	1.465
3C97	150	300	3.45e-03	1.99	2.935	7.85e-05	0.0136	1.575
3C97	300	400	4.49e-04	2.055	2.415	8.75e-05	0.014	1.528
DM90	25	300	6.91e-08	1.53006	2.849	2.68e-06	0.04843	3.2958

Now that the core material has been selected, the core geometry and the magnetic calculations typical for inductor design can be discussed. The first thing which needs to be specified is the required inductance and current profile. Once the current and inductance are selected, and the core geometry defined, the fringing effect in (4.13), the number of turns in (4.14), and the flux calculations in (4.15), (4.16) and (4.17) can all be found. The number of turns N is dependent on the core cross sectional area A_C, the air gap space l_g , the mean path length MPL, the fringing effect $Fringe$, the material permeability μ_r and the inductance L. The AC, DC and max flux densities are dependent on the AC current, DC current and peak current respectively, as well as the number of turns, air gaps space, material permeability, mean path length MPL, and fringing effect.

$$Fringe = 1 + \frac{\mathrm{l}_g}{\sqrt{A_C}} \log\left(\frac{2G}{\mathrm{l}_g}\right) \tag{4.13}$$

$$N = \sqrt{\frac{L\left(\mathrm{l}_g + \frac{MPL}{\mu_r}\right)}{0.4\pi A_C Fringe 10^{-8}}} \tag{4.14}$$

$$B_{ac} = \frac{0.4\pi N Fringe \Delta i_L 10^{-4}}{2\left(\mathrm{l}_g + \frac{MPL}{\mu_r}\right)} \tag{4.15}$$

$$B_{dc} = \frac{0.4\pi N Fringe I_{dc} 10^{-4}}{\left(\mathrm{l}_g + \frac{MPL}{\mu_r}\right)} \tag{4.16}$$

$$B_{\max} = \frac{0.4\pi N Fringe I_{\max} 10^{-4}}{\left(\mathrm{l}_g + \frac{MPL}{\mu_r}\right)} \tag{4.17}$$

$$P_{core} = k f^{\alpha} {B_{ac}}^{\beta} Vol_{core} \tag{4.18}$$

The maximum flux density, found in equation (4.17), must be less than or equal to the materials saturation value at a specific core temperature and is one of the design constraints which will be discussed in the optimization section 4.1.3.3. The core losses are caused by hysteresis losses, eddy-current losses and residual losses as explained in [47, 50]. Typically, the standard Steinmetz equation, shown in (4.18), is used to find the core loss of an inductor for a specific frequency and flux swing [47, 51]. The constants k, α, β and are empirically found by the core manufacturers but sometimes the manufacturer only provides the core loss tables. (4.18) is a very basic loss equation and is mainly used for transformers with sinusoidal excitation [50, 51]. More accurate loss equations have been found which make steps to account for different current profiles, as is the case for most power electronic converters. The improved generalized Steinmetz equation (iGSE), shown in equation (4.19), is such an equation which takes into account the current waveforms found in different converter topologies where T is the period and D is the percentage of on time [50]. A further advancement of $iGSE$ is done in [50] which arrives at the new improved-improved generalized Steinmetz equation (i^2GSE). However, these methods do not need to be used for 3C97 because Ferroxcube provides the temperature dependent equation shown in Table 4.3.

$$\begin{cases} P_V = \dfrac{1}{T}\displaystyle\int_T k_1 \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \\ P_V = \dfrac{k_i}{T}\left[DT\left(\dfrac{\Delta B}{DT}\right)^{\alpha}(\Delta B)^{\beta-\alpha} + (1-D)\,T\left(\dfrac{\Delta B}{(1-D)\,T}\right)^{\alpha}(\Delta B)^{\beta-\alpha}\right] \\ k_1 = \dfrac{k}{(2\pi)^{\alpha-1} 2 \displaystyle\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-1} d\theta} \end{cases} \tag{4.19}$$

4.1.3.2 Winding Design

The winding can generate a large amount of losses and heat so minimizing these effects is always ideal. As was mentioned, the core cannot go above a certain temperature or the magnetic performance of the core begins to degrade. So if the winding gets too hot it may transfer its heat to the core. Therefore, minimizing the losses is the best ideal to improve the design. Different winding constructions will also have different losses due to the geometry of the winding. Windings usually come in foil, rectangular, circular, square or Litz constructions and the selection between these winding types comes down to the design requirements since some are more advantageous than others in specific situations. Foil is a great choice for low frequency and high current, while Litz is ideal for high frequency due to its reduction in skin effect losses. For a more in-depth discussion refer to [51], however the main point to make about the winding selection is the generated losses.

There are two main aspects which contribute to winding loss, proximity effects and skin effects, both of which cause eddy currents to flow within the winding [51] The skin effect is due to the changing current within the conductor and increases with frequency. As eddy currents increase, these currents counteract the main current flow and effectively push the main current towards the outer edges of the conductor [51]. The depth at which a majority of the current flows is known as the skin depth, as shown in equation (4.20) where f is the frequency, μ_o is the permeability of air, μ_r is the permeability of the conductor material, and σ is the conductivity of the conductor. The skin depth is defined as the radial distance from the outer edge of the conductor towards the center. This section of wire is the location where a majority of the current flows and is why smaller gage wire does not become influenced by the

skin effect [51].

$$\delta = \frac{1}{\sqrt{\pi \mu_o \mu_r f_{sw} \sigma}} \tag{4.20}$$

One method to minimize the skin effect is to use multiple strands of Litz wire bundled together. Litz wire is constructed with very fine strands, each of which are insulated and twisted together. If the conductor area of each strand is smaller than the skin depth then there will be no skin effect, however the bundle diameter increases compared to magnet wire due to the space used by the insulation of each individual strand and the spacing between strands during the twisting operation [47]. This means that the winding diameter will be larger for Litz wire versus magnetic wire for the same current density due to the loss in cross sectional area resulting from the insulation and space between each strand. Therefore, there is a trade-off between loss and winding size.

The second winding effect is known as the proximity effect and it results from interacting magnetic fields of conductors in close proximity with each other. These interacting magnetic fields induce the flow of eddy currents in opposing conductors. These effects are well documented for different types of windings and are explained in more detail in [51]. In short, the proximity effect increases exponentially as the number of winding layers increases so having lower number of layers is the most ideal to reduce the effect [51].

To calculate the total winding loss both the DC and AC resistance of the winding needs to be found since the AC resistance is related to the DC resistance by a factor F_R. The DC resistance can easily be found from (4.21) for rectangular or Litz wire types. For Litz wire, p_w is the conductor resistivity, k_l is the number of strands in the

Litz bundle, N is the number of turns of the winding, l_T is the winding mean turn length, and d_{str} is the strand diameter of the Litz wire. For rectangular wire, w_r is the rectangular wire width, and h_r is the wire height. The AC resistance is found by calculating F_R , which is the AC to DC resistance ratio shown in (4.22) where F_P is the proximity effect factor and F_S is skin effect factor [51]. The difference between Litz and rectangular windings is shown in (4.23) and (4.24) when calculating the ratio. For Litz, p_{Litz} is the distance between strands inside the Litz bundle, η is the porosity factor, and N_{ll} is the number of strand layers inside the bundle, while for rectangular wire, p_r is the winding pitch and p_{Litz} is the distance between turns, and N_l is the number of bundle layers in the winding [51]. These parameters can be understood when referring to Fig. 4.7, in which both Litz and rectangular windings are shown [52]. For Litz wire it is assumed that the strands will have a square structure so that the number of Litz layers can be estimated by taking the square root of the number of Litz strands inside the Litz bundle to be used in (4.23). After calculating F_P, F_S and F_R, the DC and AC losses can be found using (4.26) and (4.27) respectively and the total loss is then found in (4.28).

$$\begin{cases} R_{DC} = \dfrac{4p_w N l_T}{k_l \pi d_{str}^2} & Litz \\ R_{DC} = \dfrac{p_w N l_T}{w_r h_r} & rec \end{cases} \tag{4.21}$$

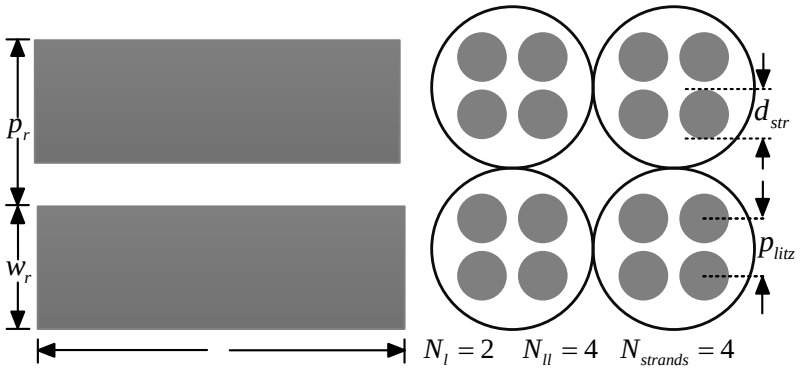


Figure 4.7: Difference in winding constructions (a) rectangular (b) Litz winding.

$$F_R = F_S + F_P \tag{4.22}$$

There are Litz bundle level proximity effects, however these can be mitigated by appropriate twisting of the strands so that each strand occupies each position within the bundle [51, 52]. For the Litz based inductors, it was decided to implement pre-bundled wires from New England Wire due to the uncertainties and variability in the Litz wire construction and because they provide all the required information such as DC resistance per thousand feet, nominal diameter, and the number of strands for each bundle. An example of a simplified table provided by New England Wire is shown for Litz wire AWG36 in Table 4.4 [53].

$$\underbrace{\begin{aligned} \eta &= \frac{d_{str}}{p_{Litz}} \\ A_{Litz} &= \left(\frac{\pi}{4}\right)^{0.75} \frac{d_{str}}{\delta_w} \sqrt{\eta} \\ N_{ll} &= N_l \sqrt{k} \\ F_P &= A_{Litz} \frac{2\left(N_{ll}^2 - 1\right)}{3} \frac{\sinh\left(A_{Litz}\right) - \sin\left(A_{Litz}\right)}{\cosh\left(A_{Litz}\right) + \cos\left(A_{Litz}\right)} \\ F_S &= A_{Litz} \frac{\sinh\left(2A_{Litz}\right) + \sin\left(2A_{Litz}\right)}{\cosh\left(2A_{Litz}\right) - \cos\left(2A_{Litz}\right)} \end{aligned}}_{\text{Litz}} \tag{4.23}$$

$$\underbrace{\begin{gathered} A_{rec} = \frac{h}{\delta_w}\sqrt{\frac{w}{p_r}} \\ F_P = A_{rec}\frac{2\left(N_l^2-1\right)}{3}\frac{\sinh\left(A_{rec}\right)-\sin\left(A_{rec}\right)}{\cosh\left(A_{rec}\right)+\cos\left(A_{rec}\right)} \\ F_S = A_{rec}\frac{\sinh\left(2A_{rec}\right)+\sin\left(2A_{rec}\right)}{\cosh\left(2A_{rec}\right)-\cos\left(2A_{rec}\right)} \end{gathered}}_{\text{rectangular}} \tag{4.24}$$

$$R_{AC} = F_R R_{DC} \tag{4.25}$$

$$P_{DC} = I_{DC}^2 R_{DC} \tag{4.26}$$

$$P_{AC} = I_{AC}^2 F_R R_{DC} \tag{4.27}$$

$$P_{winding} = P_{DC} + P_{AC} \tag{4.28}$$

New England Wire also provides other information for the bundles, however this information is not required to calculate the AC resistance of the winding [53]. There are multiple Litz wire gauges to choose from, with some being better suited than others for different frequencies. New England Wire has a table suggesting ideal operating frequencies for specific wire gages 28 to 48 however for this work, a comparison between all of them will be done to see which provide the smallest inductor volume and losses. In the results section a comparison between AWG28, 30, 33, 36, 38, 40, from New England Wire, and customized rectangular windings will be done using GA. Once the winding and core losses are found, the temperature estimation can be calculated by using equation (4.30) where SA is the total surface area of the inductor, P_{total} is the total inductor loss found in (4.29), and $T_{ambient}$ is the ambient environment temperature [47]. It is assumed there is no cooling system applied to

the inductor so that only natural convection will cool it.

Table 4.4: Simplified New England AWG 36 Litz Wire Data

Pos	Number of Wires	Nominal Outer Diameter (inches)	DC resistance per 1000ft (Ohm/1000ft)
1	4	0.013	110.1
2	7	0.017	62.9
3	10	0.023	44.05
4	16	0.029	27.53
5	27	0.037	16.32
6	41	0.044	10.74
7	65	0.059	6.98
8	105	0.074	4.32
9	165	0.092	2.75
10	265	0.116	1.71
11	420	0.158	1.11
12	660	0.197	0.71
13	1050	0.247	0.45
14	1800	0.322	0.26
15	2660	0.373	0.18
16	3360	0.548	0.14
17	4320	0.655	0.109
18	5400	0.728	0.087
19	6840	0.87	0.069
20	8460	0.962	0.055

$$P_{total} = P_{winding} + P_{core} \tag{4.29}$$

$$T_{core} = 450\left(\frac{P_{total}}{SA}\right)^{0.826} + T_{ambient} \tag{4.30}$$

4.1.3.3 GA Implementation

Now that the core and winding designs have been reviewed and the required equations found, the actual inductor design can begin. Inductor design is an iterative process done by hand or by computer aided design methods. There are design methods for standard cores provided by the manufacturers, such as the area product method (A_P) and the core geometry method (K_g), while other design methods

use custom cores and usually involve some sort of computer aided help for the design [47, 50, 54, 55]. Designs using custom core blocks will have higher costs due to the customization of the dimensions of the core blocks, although if the inductor is mass produced the cost will reduce. This can involve extra manufacturing processes compared to standard cores which are produced in large quantities. However, better inductor design occurs when you can customize the dimensions. For this work, GA is used because many different inductor designs can be solved as the algorithm runs, making it much faster as well as covering a wider range of design parameters which would take much longer if done by hand.

4.1.3.3.1 GA Parameters

First, the parameters must be defined, along with the design population, number of iterations, parameter limits, design constraints, initial guesses and the objective function/fitness function; GA will work towards the defined objective function and search for an optimal result as it compares the fitness function to other designs which also pass the design constraints. The parameters have lower and upper limits on their possible values and must be initialized with an initial guess to begin the algorithm. The initialization file includes settings such as the population size, the number of iterations, initial guesses and some other settings discussed in more detail on the MathWorks website. The design constraints will be applied to the inductors and the inductors which satisfy the constrains will pass their genes onto their children and the process continues. These children will use the old parameters of the successful parents to create new inductors with small adjustments made to these parameters to see if those small adjustments result in a new inductor which better meets the

objective function, which in this case will be the smallest inductor volume.

This process will continue to work towards the specified objective function until the last iteration or until the fitness between iterations is smaller than a specified limit which the GA requires during its initialization. The inductors which do not satisfy the constraints will be assigned a fitness value far from the target. Thus, as the algorithm runs, the lowest inductor volume for each iteration will pass on its parameters (genes) to the next iteration. Small modifications to these values will be applied to see if the minimum has been reached. For inductors which do not satisfy the constraints, they will be assigned a large volume to ensure that these inductor parameters are not passed on.

It was decided to use the C-C core shape implementing core blocks illustrated in Fig. 4.8, where the core blocks are shown in grey, while blue represents the winding and yellow the air gap. The parameters used inside the GA program are shown in Table 4.5. For Litz wire, the wire row position parameter is actually a lookup table parameter referring to the row position in the simplified New England Wire table shown in Table 4.5. For example, if GA populates an inductor with the Pos parameter equal to 10, then the number of strands would equal 420, the nominal outer diameter would be 0.117 inches and the DC resistance per thousand feet would be 1.74 ohms per 1000ft for that specific build. Parameter WT is the winding build width and depends on the wire diameter and the number of layers. For rectangular wire, WT is dependent on the wire width parameter W and the wire height H shown in Fig. 4.7. To calculate the actual winding build width WT, the number of winding layers needs to be multiplied by the width of one layer. For Litz, WT is found by multiplying the nominal diameter of the Litz bundle by the number of winding layers.

Table 4.5: C-C Core GA Inductor Parameters

Litz Wire		Rectangular Wire	
Parameter	Description	Parameter	Description
E	Core Width	E	Window Width
D	Core Depth	D	Core Depth
WAW	Window Width	WAW	Window Width
WAH	Window Height	WAH	Window Width
Lg space	Air Gap	Lg space	Air Gap
NG	# Air Gaps	NG	# Air Gaps
Pos	Wire Row Position	H	Wire Height
-	-	W	Wire Width

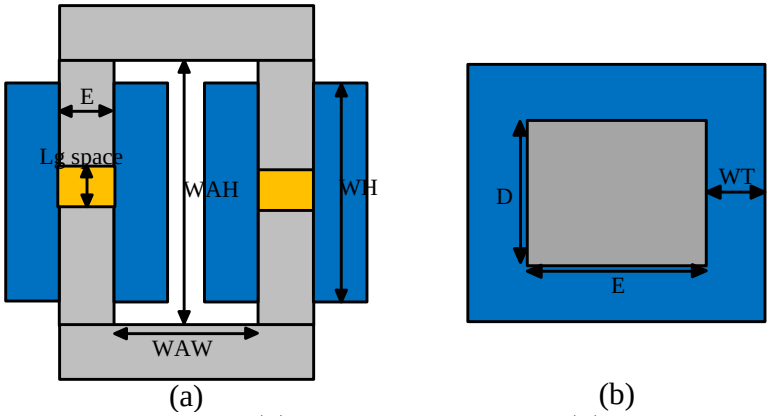


Figure 4.8: C-C core inductor (a) Cross sectional view (b) top view of single column.

4.1.3.3.2 GA Constraints

The constraints cover the winding height and width, temperature and flux density. The winding must fit inside the available window area and as the winding is wound on the inductor, there needs to be some clearance for the winding to fit both vertically and horizontally inside the window. Therefore, for this design, the vertical and horizontal clearance will be 93 percent for both. Meaning, the winding height

must be less than or equal to 93 percent of the total window height WAH, as well as being less than or equal to 93 percent of half of the total window width WAW. The half comes from the fact that this is a C-C core shaped inductor with two coils on either leg so two coils must fit inside the window width as shown in Fig. 4.8. As mentioned previously, the core flux density must be within a certain limit due to core saturation, which in the case for 3C97 is 0.41 tesla. The last constraint will be the temperature constraint. 3C97 has a maximum flux density of 0.41 tesla at a core temperature of $100°C$. Typically the max core temperature of ferrite is in the range of $100°C$-$140°C$ and as was discussed in the core design section, it was decided to use 3C97 from Ferroxcube which achieves its lowest core loss at $100°C$.

Inductors which satisfy these constraints will be optimized for the lowest volume. It should be noted that this inductor design technique can be applied to any inductor at any power level making it a very useful technique.

4.1.3.4 Results

The inductor comparison between different wire constructions is shown in Fig. 4.6, after running the genetic algorithm for a population size of 100000 and for 50 iterations, using the calculated inductance of $17.5\mu H$, maximum current of 55.5546A, DC current of 51.4403A, and a ripple current of 8.2286A. A visual breakdown of each type of loss is also presented in Fig. 4.9 to Fig. 4.13.

From the analysis and presented results, the inductor volumes for those implementing Litz wires are quite similar and range from 0.060 to 0.0796 liters. However, the inductor using the rectangular winding is about half the size at 0.035 liters mainly due to the reduced DC losses. The AC losses for the Litz winding do reduce as the

wire gage diameter decreases, shown in Fig. 4.10. However the amount of AC loss is quite small in comparison to the DC loss, shown in Table 4.6. The DC loss from the rectangular winding is almost 1 watt less than the lowest DC loss from the Litz windings. What this means is that even though the AC loss advantage gained from Litz windings versus rectangular is present, the DC losses represent the major contribution of losses. For the same current value, the Litz winding will be larger than one using a solid conductor because of the extra air and strand insulation within Litz bundles. If the ripple current was larger, the AC core and AC winding losses would increase and so in these situations, inductors using Litz wires might achieve lower inductor volumes. The low core loss in Fig. 4.10 may lead to one to believe that another core material with larger core losses should be used instead because of the advantages to be gained by switching to a non-ferrite core material such as increased core saturation, decreased number of turns, and reduced number of air gaps.

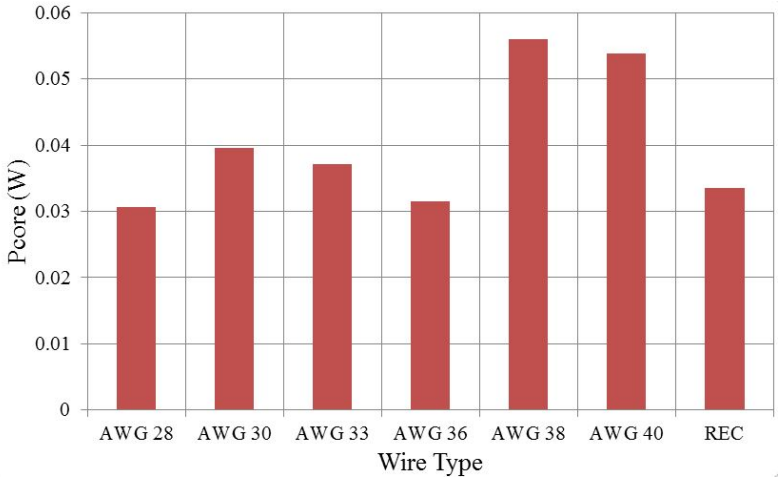


Figure 4.9: Core loss comparison for different winding types.

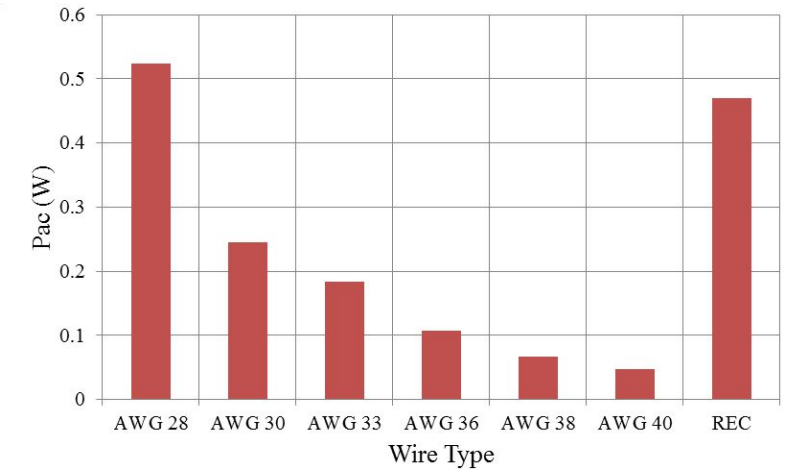


Figure 4.10: AC winding loss comparison for different winding types.

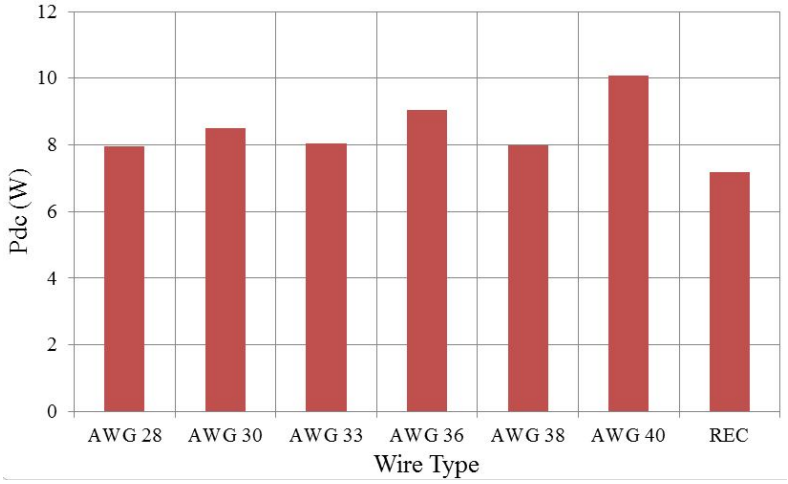


Figure 4.11: DC winding loss comparison for different winding types.

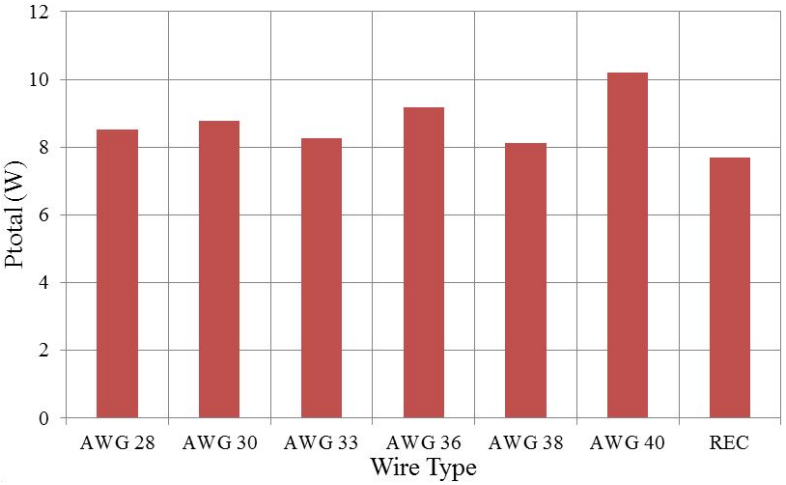


Figure 4.12: Total inductor loss comparison for different winding types.

Table 4.6: Inductor Comparison Between Litz and Rectangular Wires Using FXC 3C97

AWG Type	Litz 28	Litz 30	Litz 33	Litz 36	Litz 38	Litz 40	Rec
Inductance (μH)	17.5	17.5	17.5	17.5	17.5	17.5	17.5
Frequency (kHz)	100	100	100	100	100	100	100
Imax (A)	55.55	55.55	55.55	55.55	55.55	55.55	55.55
Idc (A)	51.44	51.44	51.44	51.44	51.44	51.44	51.44
IL Ripple (A)	8.2296	8.2286	8.2286	8.2286	8.2286	8.2286	8.2286
# Turns	16	8	12	16	14	10	24
E (cm)	0.953	1.239	0.87	0.842	0.93	1.17	0.7196
WAW (cm)	1.203	1.065	0.961	1.039	1.449	2.859	0.755
D (cm)	1.645	2.794	2.746	1.973	1.844	2.114	1.413
WAH (cm)	4.16	1.682	2.899	4.423	3.949	2.209	4.722
AC (cm^3)	1.568	3.464	2.389	1.662	1.718	2.479	1.017
Air Gap Space (cm)	0.056	0.087	0.072	0.057	0.074	0.105	0.17
# Air Gaps	6	2	4	6	4	2	4
MPL (cm)	13.38	9.217	10.17	13.23	13.427	13.61	12.53
Bdc (T)	0.367	0.34	0.321	0.366	0.378	0.378	0.379
Bac (T)	29	27	0.026	0.029	0.03	0.03	0.03
Bmax (T)	0.397	0.3678	0.3471	0.395	0.408	0.4078	0.4096
# Turns in 1 Layer	9	4	6	9	7	5	4
# Layers Per Coil	1	1	1	1	1	1	3
# Strand Layers	11	11	19	26	33	34	N/A
AWG Type	Litz	Litz	Litz	Litz	Litz	Litz	REC
Row Position	9	9	10	12	9	13	N/A
# Strands	105	110	329	660	1050	1100	N/A
Strand Dia (in)	0.0126	0.01	0.00708	0.005	0.00397	0.00314	N/A
Dia Bundle (in)	0.177	0.145	0.175	0.186	0.2	0.157	N/A
RDC/1000ft (Ω/ft)	0.66	1.01	0.68	0.697	0.7	1.13	N/A
Rec Width (cm)	N/A	N/A	N/A	N/A	N/A	N/A	1
Rec Height (cm)	N/A	N/A	N/A	N/A	N/A	N/A	0.102
Rec Spacing (cm)	N/A	N/A	N/A	N/A	N/A	N/A	1.0526
WT (cm)	0.177	0.145	0.175	0.186	0.2	0.157	0.306
WH (cm)	3.6	1.4732	2.667	3.77952	3.556	1.9939	4.2104
FR ratio	30.88	13.536	10.682	5.5443	3.9142	2.2113	30.654
Rdc ($m\Omega$)	3	3.2	3	3.4	3	3.8	2.7
Rac ($m\Omega$)	92.9	43.5	32.4	18.9	11.8	8.4	83.2
Pdc (W)	7.96	8.5	8.03	9.05	7.99	10.09	7.19
Pac (W)	0.52	0.25	0.183	0.107	0.0667	0.0476	0.47
Pcore (W)	0.03	0.04	0.04	0.03	0.06	0.05	0.03
Ptotal (W)	8.52	8.79	8.25	9.19	8.11	10.19	7.69
Total Inductor Volume (L)	0.0619	0.063	0.0606	0.065	0.072	0.0796	0.035
Width (cm)	4.008	4.28	3.59	3.668	4.32	6	2.8
Height (cm)	6.06	4.16	4.64	6.1	5.81	4.55	6.16
Depth (cm)	2.54	3.53	3.63	2.92	2.8	2.91	2.02
Tcore ($^\circ C$)	98.68	100.27	96.81	100.89	91.03	102.26	111.27

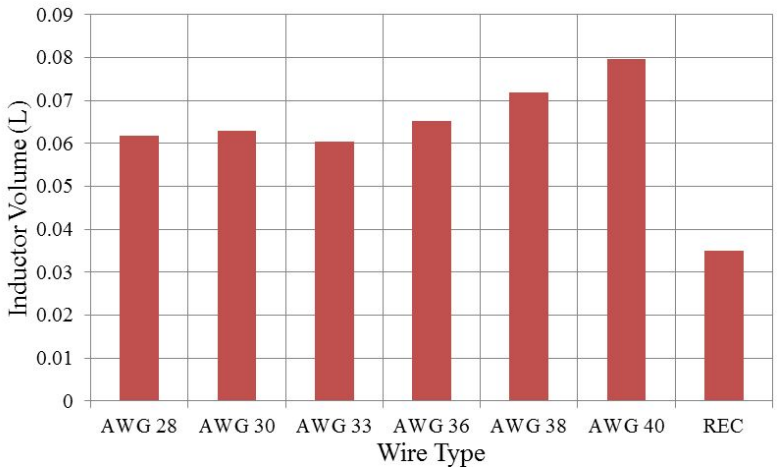


Figure 4.13: Total inductor volume comparison for different winding types.

As such, table 4.7 shows a core loss comparison between Ferroxcube 3C97 and Magnetics Inc. High Flux FeSi 160μ for the same core volumes. It is clear that the core losses will be much higher if the core material is replaced with High Flux FeSi 160μ. However, it is uncertain if the other losses in the inductor will be lower unless a similar analysis is done using GA. It was decided to just stick with the ferrite based inductor for now, but for future work a comparison between different core materials and for different winding types should be done to see which achieves a smaller total inductor volume. A transient magnetic simulation and steady-state thermal simulation were completed using JMAG to verify that the designed inductor will work and operate properly within the core and temperature limits specified.

Table 4.7: Inductor Core Loss Comparison for 3C97 Ferrite for Different Wire Types

$P_{HF160} = 447.6 B_{ac}^{2.3} f^{1.41}$ where B_{ac} is in tesla, f is in kHz, and P_{HF160} is in mW/cm^3							
Wire Type	Litz 28	Litz 30	Litz 33	Litz 36	Litz 38	Litz 40	REC
Pcore Ferrite (W)	0.0306	0.0396	0.0371	0.0315	0.056	0.0538	0.033
Pcore FeSi (W)	1.24	2.65	2.56	2.04	3.56	3.42	2.13

There are a few things which should be addressed about these simulations. First,

JMAG uses FEA for the magnetic simulations, however the thermal simulations use lumped parameter networks, meaning the thermal estimation is very basic. In the thermal simulations, the bobbin and spacer material between the airgaps and the core material are ignored since it is assumed it would not have a large influence on the heat transfer. It was assumed that the winding is entirely copper with no insulation material, and the winding also makes perfect contact with the core. There will be no cooling system added and it is assumed that the ambient temperature is $30°C$. The magnetic estimation shown in Table 4.6 is fairly close to the JMAG magnetic simulation results shown in Fig. 4.14a and Fig. 4.15. The temperature is also matching both Table 4.6 and Fig. 4.14b so it appears that the inductor design is within the designs constraints, with the estimated flux and temperatures matching simulation. Therefore, the inductor should work under the specified voltage and current profiles. One thing to note about Fig. 4.14 is that there are actually two coils on either column of the inductor but only one is shown. It was removed merely to show the inner core block details.

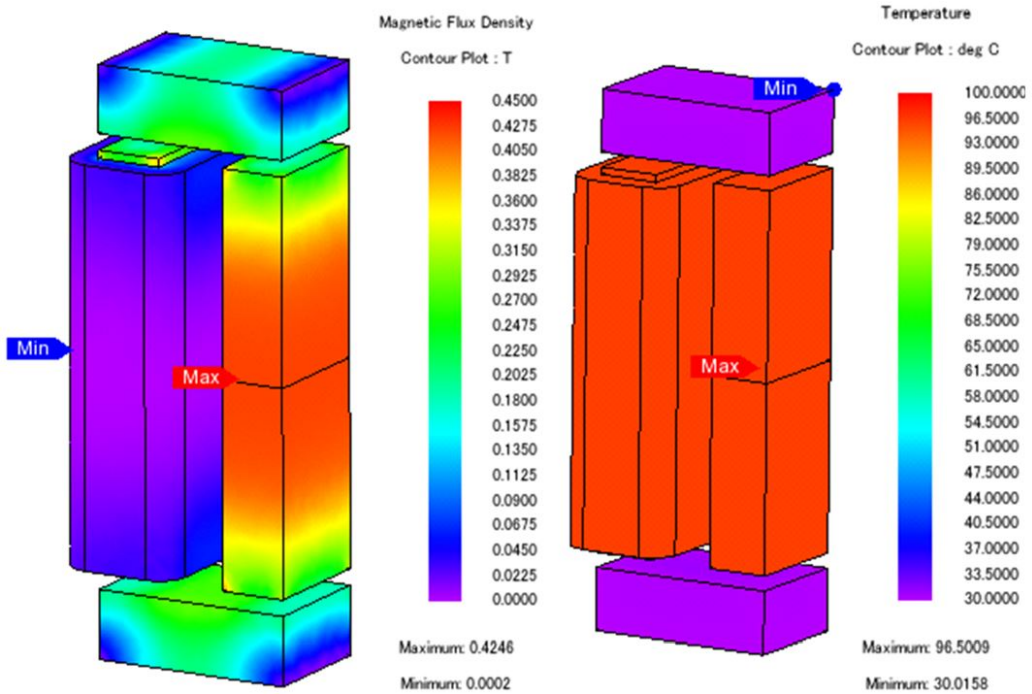


Figure 4.14: JMAG simulation results (a) magnetic simulation (b) thermal simulation.

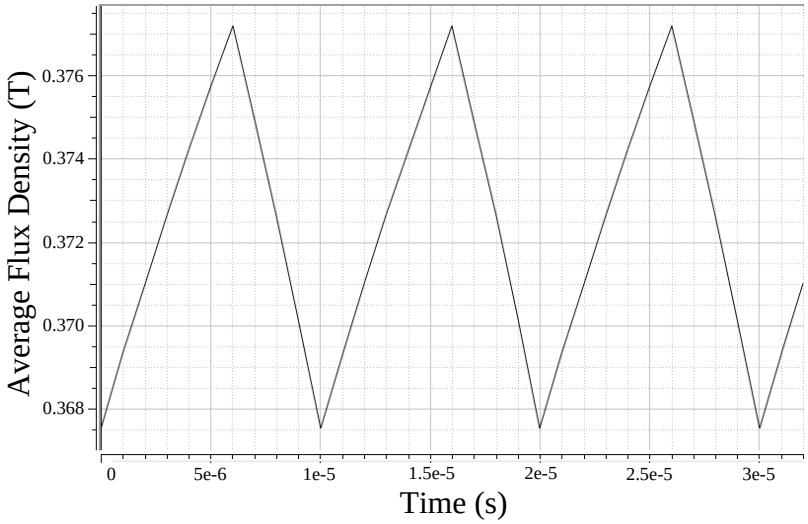


Figure 4.15: 3C97 rectangular winding inductor average flux density vs time.

4.1.4 Boost Component Selection

Unfortunately, the cost and time to manufacture a custom inductor is quite high. As such, it was decided to buy off-the-self inductors just for prototyping of the converter. One downside to this is that the required inductance for the specific current profile is challenging to find off the self. However, if the single phase boost converter is changed into an interleaved three phase converter, the phase current will reduce by roughly three times for each phase which allows a wider range of inductors to choose from. This is not to say the total size of the converter will be lower, since there will be three times as many components, but it does help with higher power converters in which large DC currents are present due to the current sharing of multiple phases [56].

The dc current will now be 17.1A with a peak current of 21.2A and an rms current of 19.5A. CoilCraft provides a few inductors which can be used to meet these conditions so it was decided to put two $10\mu H$, AGP4233-103ME inductors in series to meet the minimum inductance requirement of $17.5\mu H$ [57]. Therefore, there will be a total of six inductors for the three phase system. AGP4233-103MEs parameters are shown in Table 4.8 and the loss parameters will be discussed in section 6.1.4.1. From a volume standpoint, using a three phase interleaved system incorporating the CoilCraft AGP4233-103ME inductors will provide a total inductor volume of 0.2538 liters which is three times larger compared with the GA designed inductor using rectangular wire which has a total volume of 0.035 liters. In 7.1 it will be shown that the loss of the single phase inductor, designed using GA, will have lower losses than the three phase system. However, the total boost converter system will have higher conduction and switching losses resulting in lower total efficiency even though the inductor losses and volume are smaller. If AGP4233-103ME is replaced with the GA

inductor, both the losses and the volume will be smaller making it the more ideal selection out of all three. This analysis will be discussed and shown in Chapter 7 since a review of the switching losses is required first.

Table 4.8: AGP4233-103ME Parameters [54]

L(μH)	DCR($m\Omega$)		Saturation Current (A)			RMS Current (A)		Dimensions		
	Nom	Max	10%	20%	30%	20% rise	30% rise	W (cm	D (cm)	H (cm)
10	2.8	2.95	56	60	63	24	34	4.22	3.58	2.8

As for the MOSFET selection, there are many MOSFETs to choose from on Digikey or Mouser. Typically, selecting a MOSFET which has low on-state resistance, low turn-on and turn-off times, low delay times and low reverse recovery charge and reverse recovery time are all ideal. The MOSFET must also be able to handle the current and voltage ratings of the converter. As was mentioned, for the three phase interleaved boost converter the peak and rms currents for the MOSFET are 21.2A and 19.5A respectively. The voltage rating has not changed from being 60V. When selecting the switch a factor of 1.5 times will be applied to the voltage and current ratings calculated to provide some extra margin, therefore the MOSFET must be able to handle a peak current of 32.25A, an rms current of 29.25A and a peak voltage of 90V. Looking online it was decided to select IPP083N10N5 from Infineon shown in Table 4.9 [58].

Table 4.9: IPP083N10N5 Parameters [58]

V_{DS}	I_D	I_{Fpuls}	$C_{oss(typ)}$	$Q_{g(typ)}$	t_r	t_f	$t_{d(on)}$	$t_{d(off)}$	$t_{rr(typ)}$	$Q_{rr(typ)}$
(V)	(A)	(A)	(μF)	(nC)	(ns)	(ns)	(ns)	(ns)	(ns)	(μC)
100	73	8.3	337	30	5	5	13	21	58	118

A similar process was done for the diode; selecting low on resistance, reverse recovery time, low reverse recovery charge, and low on-state voltage. The peak current seen by the diode will be the same but the rms current for the diode is found from (4.12), and is equal to 12.13A for an input of 24V and an output of 48V and 18.12A with 1.5x margin. IDW30E65D1 [59] from Infineon will work for these specifications and is shown in Table 4.10.

Table 4.10: IDW30E65D1 Parameters [59]

$V_{DS}(V)$	I_F(A)	I_{Fpuls}(A)	V_{Fmax}(V)	$t_{rr(typ)}$(ns)	$Q_{rr(typ)}(\mu C)$
650	30	90	1.35	154	0.98

The calculated output capacitance is $44.6\mu F$ and must withstand an rms current rating of 25.7A while the input capacitor is $7.15\mu F$ and must withstand an rms current rating of 2.38A. For the input capacitor, one MKP1848C61060JK2 can be used since it is $10\mu F$ and has an rms current rating of 9A, while for the output five MKP1848C61060JK2 capacitors are placed in parallel giving a total of $50\mu F$ and a rms capability of 45A total. Table 4.11 shows the parameters of MKP1848C61060JK2 [60].

Table 4.11: MKP1848C61060JK2 Parameters [60]

Capacitance (μF)	I_{peak}(A)	I_{rms}(A)	ESR($m\Omega$)	tanδ
10	500	9	8	85

4.2 Buck Converter

4.2.1 Buck Converter Overview

Fig. 4.16 shows the typical buck converter with high input, low output voltage while Fig. 4.17 and Fig. 4.18 show the inductor current and voltage waveforms respectively.

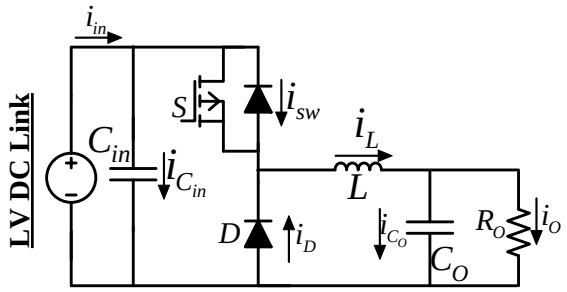


Figure 4.16: Buck converter circuit [40],[45].

As was done for the boost, equating the on and off times of the ripple current (4.31) provides the duty cycle equation for the buck converter shown in (4.32), assuming the converter will be running in CCM.

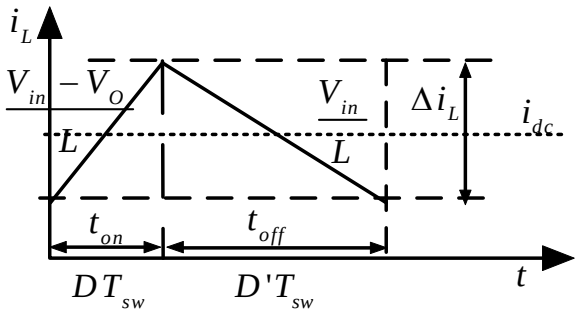


Figure 4.17: Buck converter inductor current waveform [40],[45].

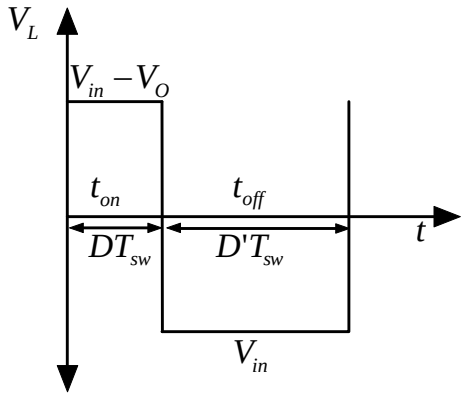


Figure 4.18: Buck converter inductor voltage waveform [40],[45].

The inductor peak and rms current equations for the buck are the exact same as the boost, as shown in (4.33) and (4.34). The equations for the input and output capacitance and rms currents are found in (4.35) to (4.38).

$$\begin{cases} \dfrac{D\left(V_{in}-V_o\right)}{Lf_{sw}} = \Delta i_L & t_{on} \\ \dfrac{-D'V_o}{Lf_{sw}} = \Delta i_L & t_{off} \end{cases} \tag{4.31}$$

$$\frac{D\left(V_{in}-V_o\right)}{Lf_{sw}} = \frac{-\left(1-D\right)V_o}{Lf_{sw}} \rightarrow \frac{V_o}{V_{in}} = D \tag{4.32}$$

$$I_{L\max} = I_{DC} + \frac{\Delta i_L}{2} \tag{4.33}$$

$$I_{L,rms} = I_{DC} + \frac{\Delta i_L}{\sqrt{12}} \tag{4.34}$$

$$C_{in} = \frac{I_{in}D_{on}}{f_s \Delta V_{in}} \tag{4.35}$$

$$I_{C_{in,rms}} = I_{in}\sqrt{\frac{D}{1-D}} \tag{4.36}$$

$$C_O = \frac{\Delta i_L}{8 f_s \Delta V_{C_O}} \tag{4.37}$$

$$I_{Co,rms} = \frac{\Delta i_L}{\sqrt{12}} \tag{4.38}$$

The capacitor waveforms of the buck converter are opposite to what the boost converter waveforms are. Meaning, the output capacitor waveforms for the buck converter are the same as the input capacitor waveforms of the boost, while the input capacitor for the buck are the same as the output capacitor of the boost. This is because the buck is a boost converter with opposite power flow so that the input of the boost is the output of the buck, while the output of the boost is the input of the buck. Therefore, the waveforms for the capacitors will not be repeated due to redundancy. The voltage and current ratings for the buck converter are shown in Table 4.12 and will be required when selecting the components.

Table 4.12: Buck Converter Voltage and Current Ratings

Component	Voltage Rating	Current Rating
Inductor	$V_{L,peak} = V_{O,max} - V_{in,min}$	$I_{L,peak} = I_{dc} + \frac{\Delta i_L}{2}$,$I_{L,rms} = I_{dc} + \frac{\Delta i_L}{\sqrt{12}}$
Switch	V_O	$I_{M,peak} = I_{dc} + \frac{\Delta i_L}{2}$,$I_{M,rms} = I_O\sqrt{D}$
Diode	V_O	$I_{D,peak} = I_{dc} + \frac{\Delta i_L}{2}$,$I_{D,rms} = I_O\sqrt{1-D}$
Output Capacitor	V_O	$I_{Co,rms} = \frac{\Delta i_L}{\sqrt{12}}$
Input Capacitor	V_{in}	$I_{Cin,rms} = I_{in}\sqrt{\frac{D}{1-D}}$

4.2.2 Design of Buck Converter

The buck requirements in Table 3.1 state that the input voltage ranges from 48V-60V, while the DC load is either 12V or 24V since most DC loads are either 12V or 24V. The inductor current ripple will be 40 percent of the output current

and the output voltage ripple will be 5 percent of the output voltage. With an output power of 100 W, the maximum output current occurs at the minimum output voltage and maximum input voltage of 12V and 60V respectively, resulting in an output current of 8.33A and an inductor current ripple of 3.332A. The max voltage ripple will also be 1.2V for a 24V output. Using the inductor equation in (4.31), the maximum inductance to maintain the ripple requirement occurs for an input and output voltage of 60V and 24V respectively, giving an inductance of $86.4\mu H$. The minimum output capacitance to maintain an output voltage ripple of 5 percent is found from (4.37) and occurs for the lowest output voltage and highest ripple current giving $6.94\mu F$. The current rating is found from (4.38) and is found to be 0.962A. The input capacitor can be found from (4.35) and occurs for the highest output current and duty cycle and lowest ripple voltage, giving an input capacitance of $34.7\mu F$. The input current requirement is found from (4.36) and is 0.962A. Based on these calculated component values it was decided to select an inductance value of $100\mu H$ and an output capacitance of $10\mu F$.

4.2.3 Buck Component Selection

The inductance needs to withstand around 8.86A peak, 8.64A rms. 1140-101K-RC is a $100\mu F$ inductor with a saturation current of 20.6A and an rms current of 10.5A so it should work for this application while also reducing the ripple current. The parameters for this inductor are shown in Table 4.13 [61].

Table 4.13: 1140-101K-RC Parameters [61]

Inductance(μH)	DCR($m\Omega$)	Saturation Current (A)	RMS Current (A)
100	25	20.6	10.5

The input capacitor will be ignored since there is an output capacitor from the boost converter, so only the output capacitor of the buck will be implemented. The minimum calculated output capacitance is $6.94\mu F$ and must be able to handle around 0.96A rms. Using the same output capacitor from the boost, MKP1848C61060JK2, provides a capacitance of $10\mu F$ which is enough for the buck specifications. The converter will also implement the same switch within the boost converter since the buck switch must be able to withstand a peak current of 8.89A, an rms current of 4.166A and a maximum voltage of 58.8V. The diode selected again is the same as the boost diode for simplicity. For the buck, it must withstand a peak current of 8.89A, an rms current of 7.43A and a maximum voltage of 58.8V. As such, the MOSFET, diode and capacitor parameters were already mentioned in the boost section 4.1 so they will not be repeated here.

4.3 Phase-Shifted Full-Bridge Isolated Converter

4.3.1 Phase-Shifted Full-Bridge Converter Overview

The proposed PSFB converter is shown in Fig. 4.19 and its operation can be broken down into six modes shown in Fig. 4.21, where T_S is the switching period, V_P is the primary voltage, I_P is the primary current, V_S is the secondary voltage D is the percentage of time the primary is either $-V_P$ or V_{DS} for half the period, φ is the phase shift angle between S_5 and S_6 , t_{dead} is the dead-time between leg switches, D_{eff} is the percentage of time the secondary is either $-nV_P$ or nV_P where n is the secondary to primary turns ratio, and ΔD is the amount of duty cycle lost

from primary to secondary [56, 62, 63]. Looking at Fig. 4.20, (4.39) can be found, along with (4.40), where the effective duty cycle D_{eff} is found in (4.41) [56, 62, 63]. For further clarification on following equaitons and discussion in this section, refer to [56, 62, 63].

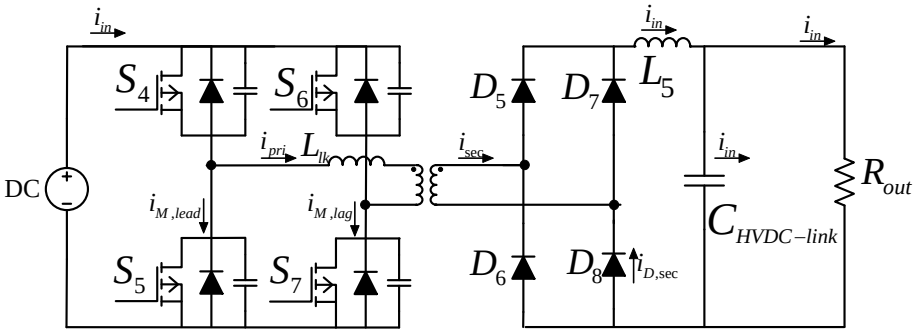


Figure 4.19: Phase shifted full bridge converter circuit.

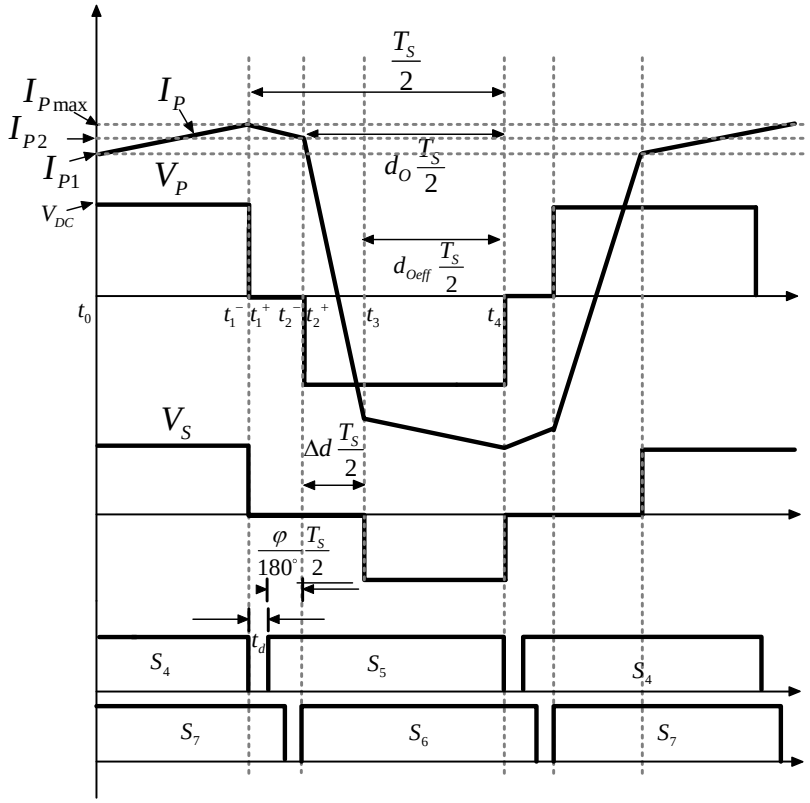


Figure 4.20: Phase shifted full bridge converter waveforms [56],[62],[63].

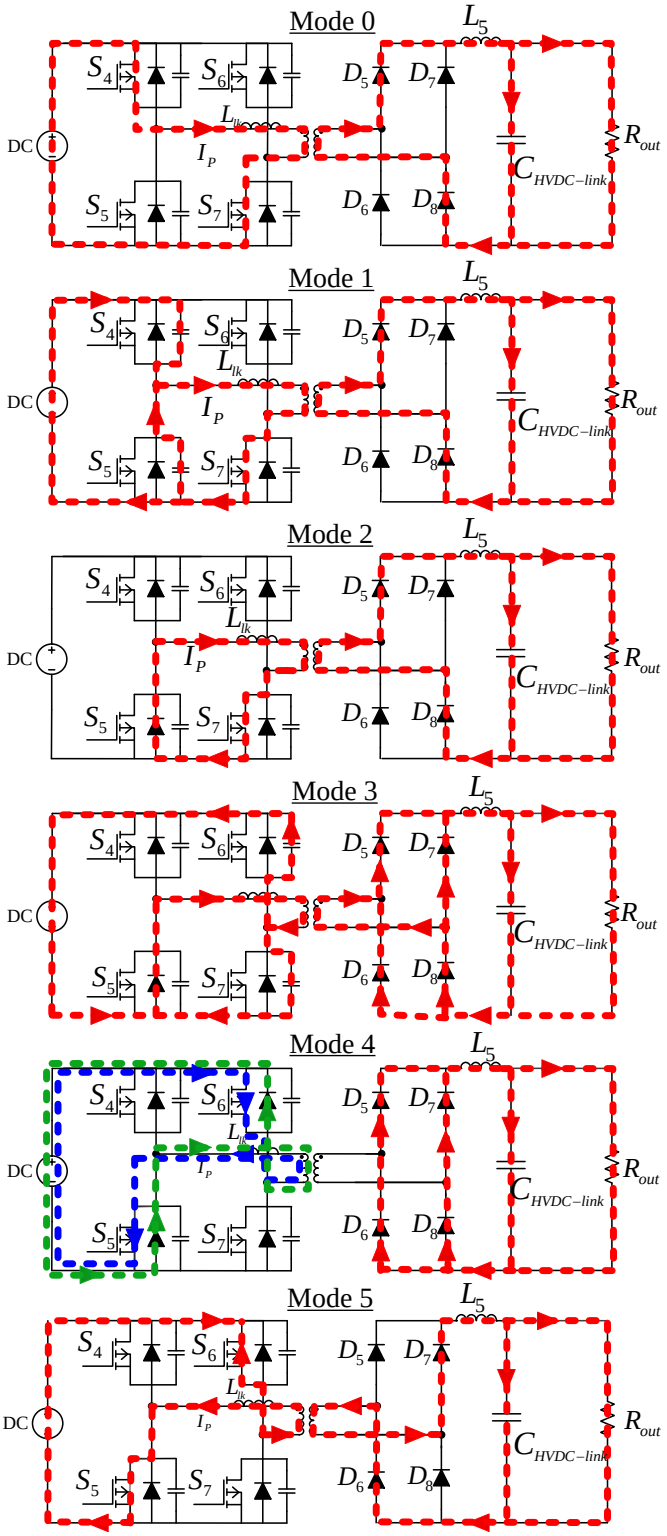


Figure 4.21: Phase shifted full bridge converter operation modes [56],[62],[63].

$$D = 1 - \frac{\varphi}{180} - \frac{2t_{dead}}{T_S} \tag{4.39}$$

$$D = \Delta D + D_{eff} \tag{4.40}$$

$$D_{eff} = \frac{N_P V_O}{N_S V_{in}} \tag{4.41}$$

$$\frac{1}{2} L_{lk} I_{P2,ZVS}^2 \geq \frac{1}{2} 2 C_{oss} V_{DC}^2 \rightarrow I_{P2,ZVS} \geq \sqrt{\frac{2C_{oss}}{L_{lk}}} V_{DC} \tag{4.42}$$

$$\frac{1}{2}\left(L_{lk} + \frac{L_O}{n^2}\right) I_{P2,ZVS}^2 \geq \frac{1}{2} 2 C_{oss} V_{DC}^2 \rightarrow I_{P2,ZVS} \geq \sqrt{\frac{2C_{oss}}{(L_{lk} + \frac{L_O}{n^2})}} V_{DC} \tag{4.43}$$

$$t_{dead} = \frac{\pi}{2}\sqrt{2 L_{lk} C_{oss}} \rightarrow L_{lk} = \left(\frac{2t_{dead}}{\pi}\right)^2 \frac{1}{2C_{oss}} \tag{4.44}$$

During mode zero $\left(t_0 - t_1^-\right)$, S_4 and S_7 are conducting and energy is transferred from the primary to the secondary as current builds in the primary and the primary voltage equals the input voltage V_{DC}.

Mode one $\left(t_1^- - t_1^+\right)$ begins and S_4 turns off. Current then charges the output capacitor of S_4 to V_{DC} and discharges the output capacitor of S_5 to zero. The voltage across the primary falls from V_{DC} to zero as the load current flows through the secondary. Once the capacitor voltage across S_5 falls to zero, it can be turned on with ZVS. The time required to charge and discharge these capacitors must be less than or equal to the dead-time in (4.44) [56, 62, 63]. This is the dead-time requirement for ZVS and if the time required to charge and discharge the switch capacitors is larger than this time, ZVS will not be achieved. To achieve ZVS there also needs to be enough energy to fully charge and discharge the switch capacitors and for S_4 and S_5

the energy required is (4.43) [56, 62, 63]. It is easier to achieve ZVS for these switches because the output filter inductor and leakage inductor contribute to the energy used to charge and discharge the output capacitors of S_4 and S_5 respectively [56, 62, 63]. At the end of this mode the primary current is at its max value.

During mode two $\left(t_1^+ \rightarrow t_2^-\right)$, the primary current decreases with a slope $\frac{-V_O N_S}{L_O N_P}$ as it freewheels through the body diode of S_5 and switch S_7 shown in Fig. 4.21. Once the body diode starts to conduct, the switch of S_5 can be turned on with ZVS. At the end the primary current is equal to I_{P2}.

During mode three $\left(t_2^- \rightarrow t_2^+\right)$, S_7 is turned off and current charges the output capacitor of S_7 up to V_{DC} while discharging the output capacitor of S_6 to zero. The primary voltage falls from zero to $-V_{DC}$ and the secondary voltage remains zero since all the diodes are conducting. Diodes D_6 and D_7 are forward biased due to the negative primary voltage but diodes D_4 and D_5 do not turn-off right away so this causes the secondary side to become zero since all the diode are conducting. The energy needed to charge output capacitor of S_7 and discharge the output capacitor of S_6 is only supplied from the leakage inductor and is found in 4.42 [56, 62, 63]. At the end of this quick transition the body diode of S_6 will start conducting and then S_6 can be turned on with ZVS if enough time has passed before the switch is turned on. Otherwise, hard switching will occur. This required time is found in (4.44) where L_{lk} is the leakage inductance, C_{oss} is the switch output capacitance [56, 62, 63]. This equation can be used to find the required inductance or even capacitance if the other two parameters are defined. For example, if a certain output capacitance and dead-time are needed, then the required leakage inductance to achieve ZVS would be found from (4.44) [56,62,63]. As far as the required energy to charge and discharge the

output capacitors, (4.44) is used to find the required leakage inductance [56, 62, 63]. Therefore, either increasing the dead-time or leakage inductance will help achieve ZVS. At the end the output capacitor of S_6 is fully discharged and the body diode conducts just before the switch can be turned on.

During mode 4 $\left(t_2^+ \rightarrow t_3\right)$, the primary current decreases at a slope of $\frac{-V_{in}}{L_{lk}}$ and the body diodes of S_6 and S_5 conduct for a short time. The primary current continues in the negative direction and by the end of mode four the primary current reaches $-I_{P1}$. The primary voltage is now $-V_{DC}$ and the secondary voltage is still zero since the rectifier diodes are still all conducting, shorting the secondary.

In mode five $(t_3 \rightarrow t_4)$ the secondary goes from zero to $-V_{DC}$ as the secondary current now flows through the transformer and diodes D_6 and D_7. The output filter inductor begins to store energy and at the end of mode five the primary current is at its lowest value $-I_{Pmax}$.

Modes zero to five repeat again but for the opposite switches and so it is redundant to repeat the process again. Mode three is the one in which only the energy in the leakage inductor is used so it will be the limiting case. If ZVS can be achieved in this leg then it will be achieve for switches S_4 and S_5.

Using Fig. 4.20, the actual primary current at t_2^- is described in (4.45) when relating it to the secondary side where I_O is the load current, Δi_{Lo} is the inductor ripple current, L_O is the filter inductor, V_O is the output voltage, n is the secondary to primary turn ratio N_S/N_P, f_{sw} is the switching frequency, and D is the primary duty cycle [56, 62, 63]. This means that to achieve ZVS, the primary current in 4.45 must satisfy expression (4.42) [56, 62, 63]. Combining (4.42) (4.44) and (4.45) and rearranging these equations the required primary duty cycle can be found in

(4.46). Using (4.39), the required phase shift to achieve ZVS is then shown in (4.47). Therefore, for a specific L_O, f_{sw}, C_{oss}, ΔI_o, n, L_{lk}, V_O, V_{DC}, and t_{dead}; the phase shift must be less than or equal to expression (4.47) to achieve ZVS.

The next restriction on the phase shift comes from achieving the desired output voltage. The actual duty cycle value of the PSFB converter is shown in (4.39) for a specific phase shift and dead-time value, while the effective duty cycle required to achieve the desired output voltage is found in (4.41) [56,62,63]. Therefore, to achieve the desired output voltage, the effective duty cycle must be greater than or equal to (4.41). The loss of duty cycle can be found from Fig. 4.20 and spans from t_2^+ to t_3 as the primary current goes from I_{P2} to $-I_{P1}$ and is defined in (4.48) [56, 62, 63]. I_{P2} was already found in (4.45) so all that is needed is I_{P1}. Looking at Fig. 4.20, I_{P1} begins at the same time the secondary current turns on, which is the minimum output point of the ripple current. As such, I_{P1} can be explained by (4.49) [56,62,63]. Substituting (4.45) and (4.49) into (4.48) gives (4.50) and using (4.40) and (4.41) the actual duty cycle required to achieve the desired output voltage must satisfy (4.51). Substituting (4.39) into (4.51) gives the required phase shift to achieve the desired output voltage shown in (4.52).

$$I_{P2} = n\left(I_O + \frac{\Delta i_{Lo}}{2} - \frac{V_O}{2f_{sw}L_f}(1-D)\right) \tag{4.45}$$

$$D \geq \frac{2L_O f_{sw}}{nV_O}\sqrt{\frac{2C_{oss}}{L_{lk}}}V_{DC} - \frac{\Delta I_O L_O f_{sw}}{V_O} - \frac{2I_O L_O f_{sw}}{V_O} + 1 \tag{4.46}$$

$$\varphi \leq 180^\circ\left(1 - \left(\frac{2L_O f_{sw}}{nV_O}\sqrt{\frac{2C_{oss}}{L_{lk}}}V_{DC} - \frac{\Delta I_O L_O f_{sw}}{V_O} - \frac{2P_O L_O f_{sw}}{V_O^2} + 1\right) - 2t_{dead}f_{sw}\right) \tag{4.47}$$

$$\Delta D = \frac{2\left(I_{P1} + I_{P2}\right) f_{sw} L_{lk}}{V_{DC}} \tag{4.48}$$

$$I_{P1} = n\left(I_O - \frac{\Delta i_{Lo}}{2}\right) \tag{4.49}$$

$$\Delta D = \frac{2n f_{sw} L_{lk}}{V_{DC}}\left(2I_O - \frac{V_O\left(1-D\right)}{2 f_{sw} L_O}\right) \tag{4.50}$$

$$D \geq \frac{\frac{V_O}{n} + 4n L_{lk} I_O f_{sw} - \frac{n L_{lk} V_O}{L_O}}{V_{DC} - \frac{n L_{lk} V_O}{L_O}} \tag{4.51}$$

$$\varphi \leq 180^\circ\left(1 - \left(\frac{\frac{V_O}{n} + 4n L_{lk} I_O f_{sw} - \frac{n L_{lk} V_O}{L_O}}{V_{DC} - \frac{n L_{lk} V_O}{L_O}}\right) - 2 t_{dead} f_{sw}\right) \tag{4.52}$$

For the converter to work properly, (4.52) must be satisfied and will be the maximum value that the phase shift can be since the maximum duty cycle occurs when the phase shift is zero as shown in (4.39). The voltage ratings for the switches on the primary side must be approximately 1.5 times larger than the LVDC link voltage. 1.5 times adds some margin due to voltage transients. Therefore, for a LVDC link voltage of around 60V, the switches must be able to handle around 90V. Using the same method, the maximum expected output voltage should be around 400V which gives 600V. For the current ratings, the rms and peak currents will be required. These currents are a bit challenging to find since the current waveforms are oddly shaped as shown in Fig. 4.20. The required currents for each component within the PSFB converter have already been found in [56] and are presented in (4.53) to (4.63) where the primary rms current is (4.53), secondary is (4.54), leading MOSFET current is

(4.58), lagging MOSFET current is (4.59), body diode of leading leg is (4.60), body diode of lagging leg is (4.61), rectifier diode current is (4.62) and the filter inductor rms current is (4.63) [56]..

$$I_{TRpri,rms} = \sqrt{\begin{array}{l} \frac{m_1^2(D-D_{eff})^3}{12f_s^2} - \frac{m_1 I_{p2}(D-D_{eff})^2}{2f_s} + I_{P2}^2(D-D_{eff}) + \\ \frac{m_2^2 D_{eff}^2}{12f_s^2} + \frac{m_2 I_{P1} D_{eff}^2}{2f_s} + I_{P1}^2 D_{eff} + \frac{m_3^2(1-D)^3}{12f_s^2} + \\ \frac{m_3 I_{p2}(1-D)^2}{2f_s} + I_{P2}^2(1-D) \end{array}} \tag{4.53}$$

$$I_{TR\sec,rms} = I_{TRpri,rms} n \tag{4.54}$$

$$m_1 = \frac{V_{DC}}{L_{lk}} \tag{4.55}$$

$$m_2 = \frac{(V_{DC} - V_O)\, n}{L_O} \tag{4.56}$$

$$m_3 = \frac{n V_O}{L_O} \tag{4.57}$$

$$I_{Mlead,rms} = \sqrt{\frac{m_1 f_s}{2}\left(\frac{I_{P1}+I_{P2}}{2m_1} - \frac{D-D_{eff}}{4f_s}\right)^2 + \frac{I_{P1} D_{eff}}{2} + \frac{m_2 D_{eff}^2}{8f_s}} \tag{4.58}$$

$$I_{lag,rms} = I_{lead,rms} + \sqrt{\frac{I_{P2}(1-D)}{2} + \frac{m_3(1-D)^2}{8f_s}} \tag{4.59}$$

$$I_{Dlead,rms} = \sqrt{\frac{I_{P2}(1-D)}{2} + \frac{m_3(1-D)^2}{8f_s} + \frac{m_1 f_s}{2}\left(\frac{I_{P1}+I_{P2}}{2m_1} + \frac{D-D_{eff}}{4f_s}\right)^2} \tag{4.60}$$

$$I_{Dlag,rms} = \sqrt{\frac{m_1 f_s}{2}\left(\frac{I_{P1}+I_{P2}}{2m_1} + \frac{D-D_{eff}}{4f_s}\right)^2} \tag{4.61}$$

$$I_{rec,rms} = \frac{I_O}{2} \tag{4.62}$$

$$I_{Lo,rms} = I_{Lo,DC} + \frac{\Delta i_{Lo}}{\sqrt{12}} \tag{4.63}$$

The design variables and values will determine the current ratings of the converter, however the voltage ratings for the primary MOSFET will need to be rated to at least 90V while the rectifier diodes will need to be 600V assuming a 1.5 times margin for an input of 60V and an output of 400V.

4.3.2 Design of PSFB Converter

The design of the PSFB converter begins with first defining the desired specifications. As was mentioned previously, the specifications for the integrated power electronic converter were shown in Table 3.1. From these specifications the worst case current will occur for the lowest output voltage giving the highest output current. To maintain a 230V AC load, the HVDC link must be at least 330V. However, there will be an AC ripple component on the HVDC bus resulting from the AC load [64, 65]. Some of the AC ripple on the HVDC link will be absorbed by the HVDC link capacitor. For this design, 5 percent ripple will be allowed on the HVDC link. Due to this ripple allowance, it was decided to have the minimum DC link voltage of 350V which will have a min value of 341.25V and a peak value of 358.75V. If the inverter efficiency is assumed to be at least 90 percent, the input power required to achieve 1kW will be 1111.11W, which gives an output current of 3.17A.

The selection of the leakage and output filter inductance values are determined by sweeping over a specified range of inductance values and incorporating both the ZVS and output voltage phase shift expressions. The minimum input voltage for the phase shifted full bridge converter is 48 volts and it was also mentioned that ZVS for the lagging leg shrinks as the load decreases, therefore, there will be a range of design parameters than will be able to achieve both ZVS and also achieve an output voltage of at least 350V at the lowest output power for this converter. The design specifications state that this converter is designed to operate around a full load of 1kW with a minimum load requirement of 25 percent full load. The designed code will sweep over a specified range of leakage inductance values, output filter inductance values and number of turns to find the values at which both the output HVDC bus voltage is achieved, as well as the ZVS phase shift condition. Nested for loops were created in a MATLAB script to achieve this with the parameters and their ranges shown in Table 4.14.

Table 4.14: MATLAB PSFB Converter Design 'For Loop' Parameters

Parameter	#of turns	Leakage Inductance Range (μH)	Filter Inductance Range
Range	1-25	$1\mu H$-$50\mu H$	$10\mu H$-$400\mu H$

An input voltage of 48V and an output voltage of 350V were selected for the design because the output voltage is harder to achieve at an input of 48V, and ZVS is harder to achieve at low loads. Fig. 4.22 shows the results when comparing the ZVS phase shift constraint in (4.47) and the output voltage phase shift constraint in (4.52) for different number of turns, leakage inductance and output filter inductance values for a 250W load and while Fig. 4.23 is for a 1kW load. The lower value of the two phase shift constraints will be the limiting case shown in both figures. Meaning, if the ZVS

phase shift constraint is lower than the phase shift constraint, the ZVS value will be the limiting condition, while the opposite is true when the ZVS condition is larger than the condition. The x-axis indicates the direction of increasing leakage inductance while the y-axis indicates the direction of increasing output filter inductance. The orange colouring indicates the ZVS condition being smaller than the V_O condition while blue is if the V_O condition is smaller than the ZVS condition. Yellow indicates regions where both conditions are not possible. Such is the case for phase shift values lower than zero or greater than 180.

Looking at the results in Fig. 4.22 and Fig. 4.23, the first thing to notice is that the 250W case has no blue regions meaning that for low power, the V_O condition is never smaller than the ZVS condition. This plays into the notion that ZVS is harder to achieve at light loads. The blue area also decreases for the 1kW loading condition as the number of turns increases. This is due to that fact that as the number of turns increases, the required HVDC link voltage of 350V is easier to achieve. As a result, the required V_O phase shift condition will have a higher limit than the ZVS condition. For both the 250W and 1kW situations, the yellow area decreases as the number of turns increases. If everything remains constant with only the number of turns increasing, (4.60) will increase as the number of turns increases. Results for designs using less than 8 turns are not able to achieve the minimum of 350V so they are not shown or discussed. As the number of turns goes passed 12, the output voltage begins to get quite large so the phase shift will have to be lowered. Fig. 4.25 shows the V_O phase shift condition for varying leakage and output filter inductance values for a dead-time of 0 and 50ns in Fig. 4.25a and Fig. 4.25b respectively. Green indicates phase shift values that are greater than 0 and smaller than 180 while red

indicates values that are out of this range.

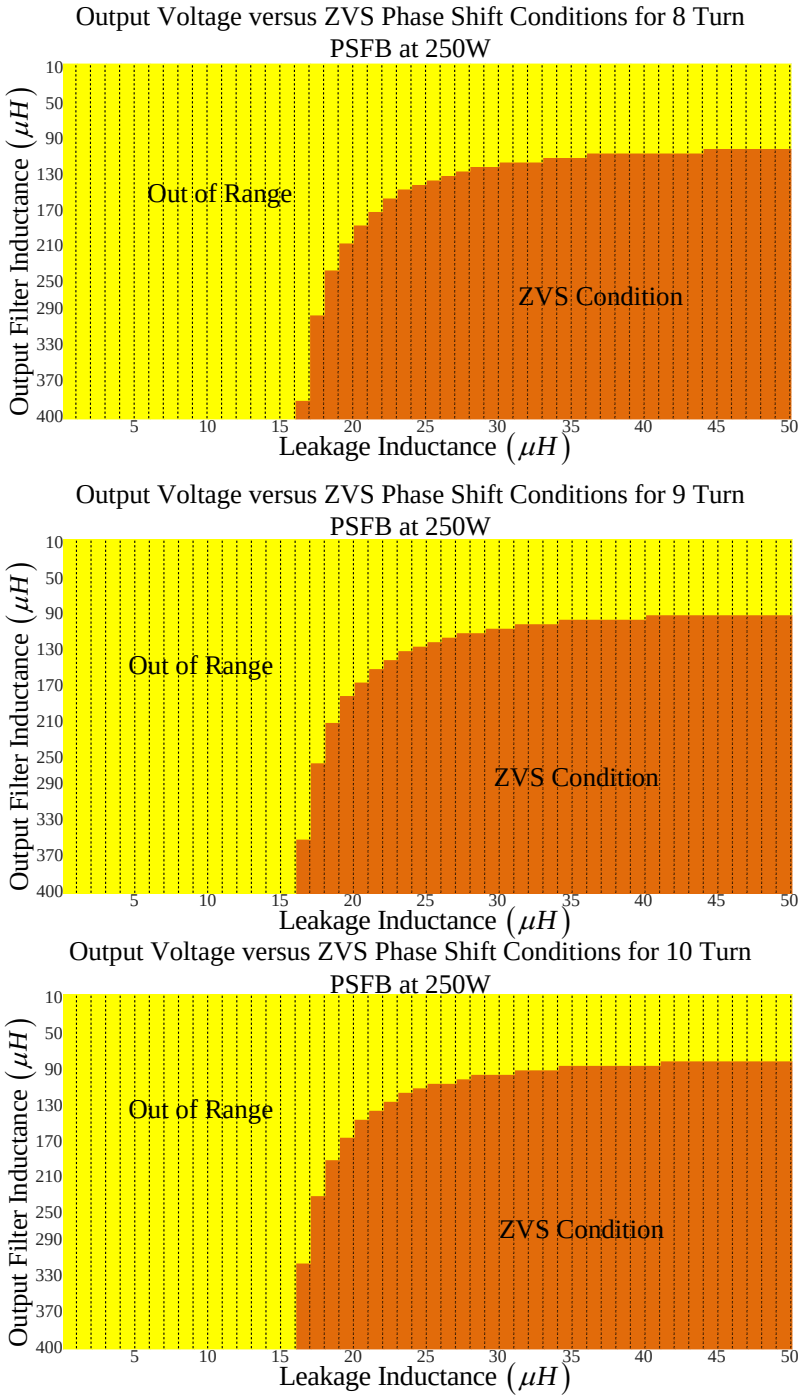


Figure 4.22: Comparison between output voltage and ZVS phase shift constraints for different L_{lk}, L_O and number of turns for 250W load.

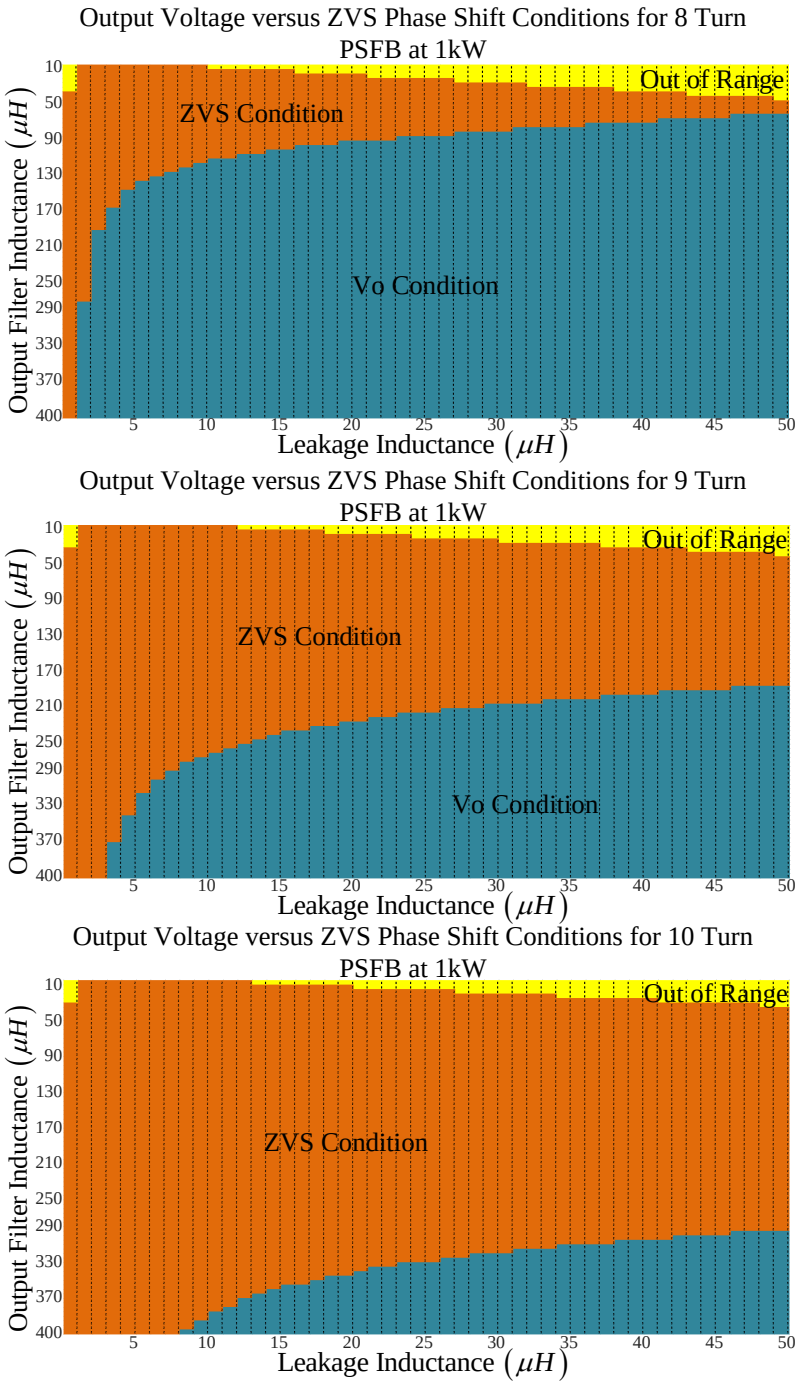


Figure 4.23: Comparison between output voltage and ZVS phase shift constraints for different L_{lk}, L_O and number of turns for 1 kW load.

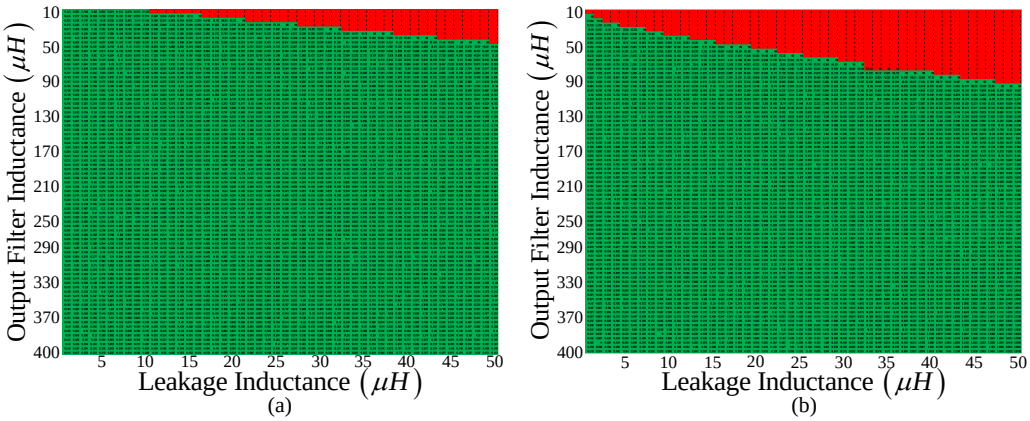


Figure 4.24: Vo phase shift condition for varying leakage and output filter inductance values at different dead-time values (a) normal dead-time calculation via (4.55) (b) 50ns extra dead-time.

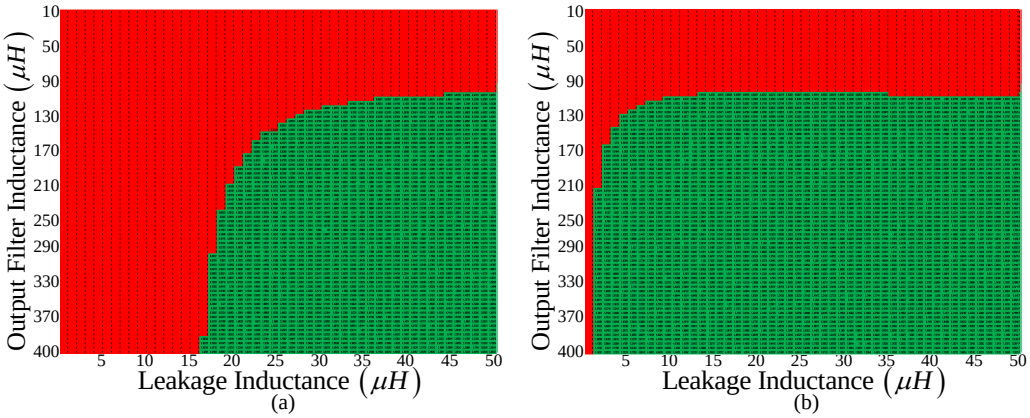


Figure 4.25: ZVS phase shift condition for varying leakage and output filter inductance values at different dead-time values (a) normal dead-time calculation via (4.55) (b) 50ns extra dead-time.

The V_O phase shift condition is used to determine the maximum phase shift value required to achieve the desired output voltage. For example, if the phase shift value is 50, then a phase shift value greater than 50 will not achieve the output voltage of 350V. Looking at Fig. 4.25, if the leakage inductance value is low, it is easier to achieve the desired output voltage indicated by the green area. This makes sense since a higher leakage inductance means the loss of duty cycle will be higher which in turn means the effective duty cycle is lower resulting in a lower output voltage.

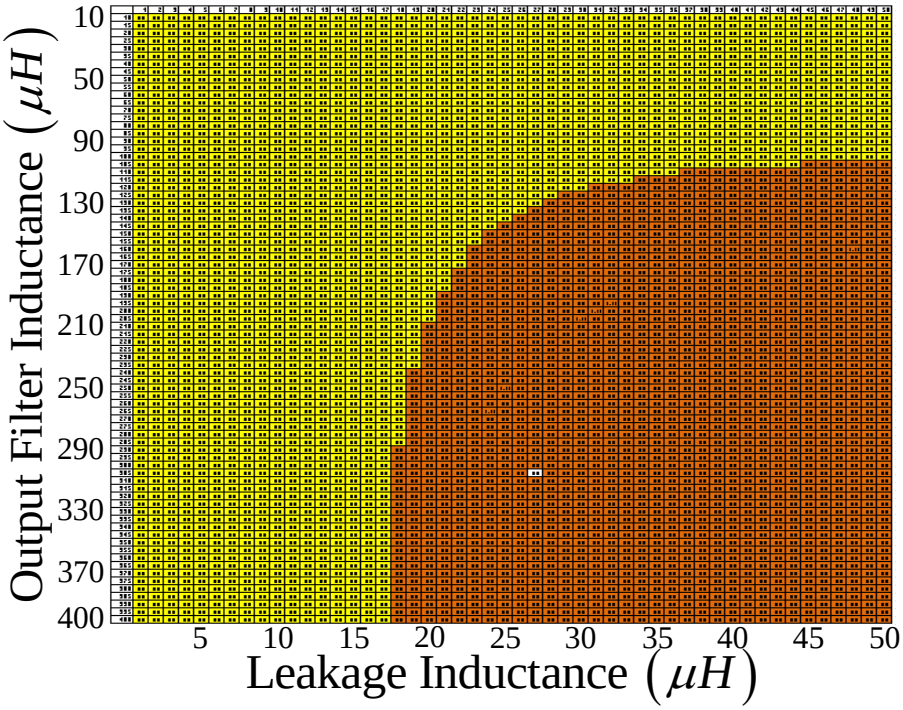


Figure 4.26: ZVS vs output voltage conditions for 8 turn converter.

Fig. 4.25b shows the ZVS phase shift condition for a 50ns increase in dead-time. Clearly the red area decreases meaning that ZVS is easier to achieve for larger dead-times which makes sense since a higher dead-time results in more time for the energy to be transferred from switch capacitor to the inductor before the switch is turned on. Therefore, there is a trade-off between achieving ZVS and achieving the desired output voltage.

Fig. 4.26 shows the 8 turn phase shift comparison. As either the leakage inductance or the output filter inductance values increase, the phase shift value also increases with the maximum value occurring at the far bottom right corner. Meaning, the largest leakage and output filter inductance values provide the larger ZVS phase shift values. Any combination within the orange area will work so somewhere in the middle should be adequate for the PSFB design. A more in-depth selection process

could be used, however in reality; these values will probably be slightly changed to fine tune the system during experimental testing so it was decided to select a condition achieving a phase shift value of at least 2 with the lowest inductance values possible to reduce losses. The value highlighted in white is the phase shift condition that was selected. This is the 27th position on the x-axis and the 60th position on the y-axis which correlates with a leakage inductance value of $27\mu H$ and an output filter inductance value of $305\mu H$.

4.3.3 Component Selection

For the component selection the voltage and current rating must first be found for each component. As was mentioned previously, assuming the inverter has an efficiency of 90 percent, the input power must then be 1111.11W. This means that the output DC current should be approximately 3.174A. The ripple current is 40 percent of the output current giving 1.267A which is therefore a peak current of 3.809A as a worst case limit. From the specifications, the minimum input voltage to the isolated converter is 48V. For an 8 turn transformer this will boost the voltage up to 384V which is above the 350V limit, assuming no voltage drops across any components. For a peak current of 3.809A, the input peak current will then be approximately 30.47 A. Depending on the switch selected, the output capacitance of the switch will change and the dead-time required for ZVS will also change. For this application, 50 kHz is targeted so MOSFETs would be the best choice of the switching devices to choose from.

Based on the voltage and current values, it was decided to select FDP045N10A [66] from Fairchild Semiconductor shown in Table 4.15 due to its high voltage and current

ratings, low on resistance and small gate capacitance. Section 6.1 will go into more detail regarding the turn-on and turn-off transitions of the MOSFET when calculating the switching losses within the converter. However, for the PSFB converter to achieve ZVS there is a minimum dead-time required. The only issue is that if the assigned dead-time is too large, the output voltage might not be achieved. Each MOSFET will require a certain amount of time to fully turn on and off. The delay time will also need to be taken into account when setting the dead-time in the controller. The total turn-on and turn-off times are shown in (4.64) and (4.65) respectively, where t_{don} is the turn-on delay time, t_r is the total rise time, t_{doff} is the turn-off delay time, and t_f is the turn-off time.

$$t_{ON} = t_{don} + t_r \tag{4.64}$$

$$t_{OFF} = t_{doff} + t_f \tag{4.65}$$

Table 4.15: FDP045N10A Parameters [66]

V_{DS} (V)	I_D (A)	R_{ON} ($m\Omega$)	C_{oss} (pF)	Q_g (nC)	t_r (ns)	t_f (ns)	$t_{d(on)}$ (ns)	$t_{d(off)}$ (ns)	$t_{rr(typ)}$ (ns)	$Q_{rr(typ)}$ (μC)
100	120	3.8	925	54	26	15	23	50	75	120

From the previous analysis the output capacitance was assumed to be $3500pF$. However, the selected MOSFET in Table 4.15 has an output capacitance of approximately $925pF$ which means the required dead-time for ZVS, using (4.44), would be 43.88ns for the same leakage inductance. The total turn-on and turn-off times can be approximated using the datasheet values shown in Table 4.15. From these values, the total on time is 49ns and the total turn-off time is 65ns. Therefore, a dead-time of about 80ns will provide some margin and should be large enough for the switch to fully

turn-on and off. To ensure the lowest voltage of 48V will achieve the desired output voltage of 350V for a dead-time of 80ns, the output voltage phase shift condition can be used to see if the value is larger than zero. From these parameters, (4.52) is found to be less than 13.95 for a 250W output and 8.04 for a 1kW system. If the dead-time is increased to 100ns these values become 13.59 and 7.68 respectively. This shows that the dead-time does not have a huge impact on the output voltage.

The transformer design will not be completed here as it is beyond the scope of this work. Therefore, an off the shelf transformer will be selected instead. An 8 turn transformer from Payton, (T1000DC-1-8), will be used within the prototype. The parameters of the transformer are shown in Table 4.16 while the loss information will be discussed in section 6.1.4.3.

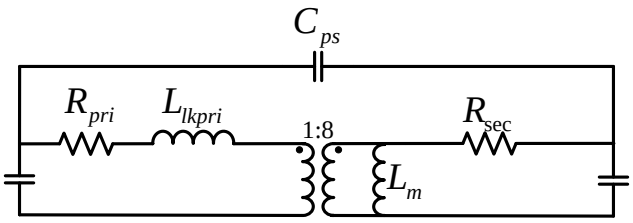


Figure 4.27: Payton T1000DC-1-8 Transformer.

Table 4.16: Payton Transformer T1000DC-1-8 Parameters

$R_{pri}(m\Omega)$	$R_{sec}(m\Omega)$	$L_{lk}(\mu H)$	$L_m(\mu H)$	$C_{cp}(nF)$	N_P:N_S
6.4	2.1498	0.22	102	2.79	1:8

For the secondary side, the rectifier diodes selected are the same as the ones used by the boost and buck converter so they won't be repeated here again. Refer to Table 4.10.

The output filter inductance selected was $300\mu H$, which is very close to the designed $305\mu H$. Looking online the 1140-151K-RC 150 inductor from J. W. Miller

will be adequate to meet the inductance requirement if two are in series. The specifications for this inductor are shown in Table 4.17 with the loss calculation shown in section 6.1.4.3 [61].

Table 4.17: 1140-151K-RC Filter Inductor Parameters [61]

$L(\mu H)$	$DCR(m\Omega)$	I_{rms}(A)	I_{sat}(A)	V_{core}(mL)
150	0.04	8.3	16.9	13

The secondary leakage inductance selected was $27\mu H$ and must be able to handle the max secondary current of 4.04A. Based on these requirements it was decided to select AIRD-03-270 from Abracon with the inductor parameters shown in Table 4.18 [67]. Having the leakage inductor in the secondary is more ideal because the current is lower which helps because many inductors that are cheap do not have high current ratings and having low current also reduces the losses. The last component which will be required is the output filter capacitor. This will be discussed in the next section since it depends on the inverter specifications and AC current propagation onto the HVDC bus.

Table 4.18: AIRD-03-270 [67]

Inductance(μH)	$DCR(\Omega)$	Saturation Current(A)	RMS Current (A)
27	0.012	23	13.5

4.4 Inverter

4.4.1 Inverter Overview

The inverter is the final converter within the integrated off-grid system which needs to be discussed. The inverter is required to convert DC to AC electricity and

will be required to run the AC load from the DC sources. Based on the specifications in Table 4.19, a single phase voltage source inverter, shown in Fig. 4.28, is adequate to operate a 230V, 50Hz, 1kW AC load, while also filtering the voltage to meet the harmonic requirements. The following sections will go into the design of the inverter including the input capacitor design and selection, and the output filter design and selection.

Table 4.19: Inverter Specifications

Load Voltage (VACrms)	Load Current (A)	Load Power (W)	DC Load Voltage (V)	DC Link Ripple (%)
230	4.348	1000	330-450	5

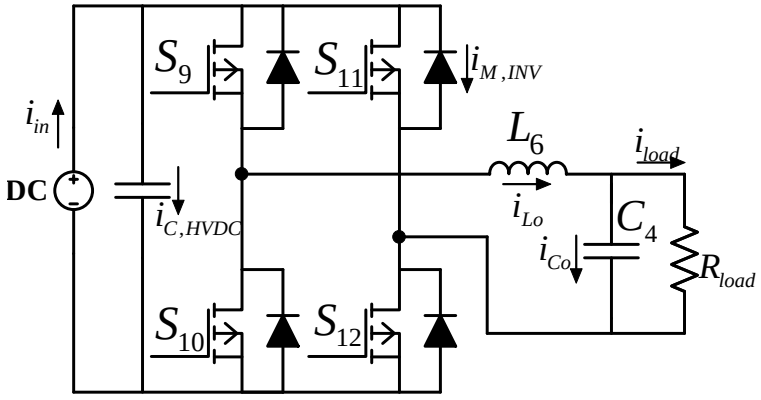


Figure 4.28: Full bridge single phase inverter.

4.4.2 Design of Inverter

4.4.2.1 Input Capacitor

The input capacitance to the inverter is the HVDC link capacitor and will see double the frequency of the output load due to the output load AC variation as shown in Fig. 4.29 [64, 65, 68]. The output current will be sinusoidal in nature and is

described in (4.66), where I_l is the peak current and ϕ is the phase difference between the voltage and current. For resistive loads, ϕ is zero meaning the current and voltage are in phase.

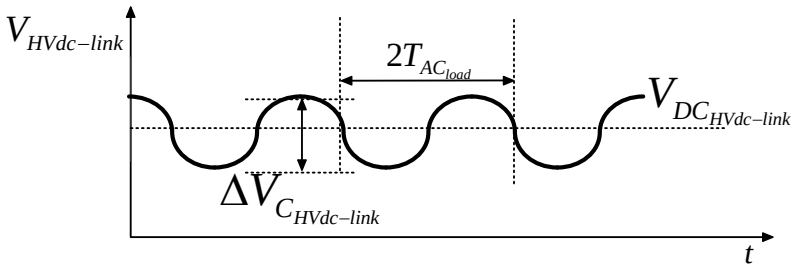


Figure 4.29: HVDC link voltage waveform.

$$i_{load}(t) = I_l \cos(\omega_l t - \phi) \tag{4.66}$$

$$V_{load}(t) = V_l \cos(\omega t) \tag{4.67}$$

Multiplying (4.66) and (4.67) together arrives at the instantaneous power of the load in (4.68) which becomes (4.69) after applying the trig identity. The DC components and AC components are split in (4.70) and equated to the input power if it is assumed the input power equals the output. The capacitor current can now be described by (4.71) and (4.72) to find the required DC link capacitance. If the AC capacitor voltage is assumed to be (4.73), then the ripple voltage across the capacitor is then two times the peak voltage as shown in (4.74). Substituting the voltage (4.73) into the current equation (4.72) and taking the derivative and equating the currents in (4.71) and (4.72) to each other arrives at (4.76). This can be simplified into (4.77) to find the capacitance value [64, 65].

$$P_l(t) = V_l \cos(\omega_l t) I_l \cos(\omega_l t + \phi) \tag{4.68}$$

$$P_l(t) = \frac{V_l I_l}{2}\cos(2\omega t + \phi) + \frac{V_l I_l}{2}\cos(\phi) \tag{4.69}$$

$$P_l(t) = \underbrace{\frac{V_l I_l}{2}\cos(2\omega t)}_{AC} + \underbrace{\frac{V_l I_l}{2}}_{DC} \tag{4.70}$$

$$i_C(t) = \frac{P_l}{V_{DC}}\cos(2\omega t) \tag{4.71}$$

$$i_C(t) = C\frac{dV_C(t)}{dt} \tag{4.72}$$

$$V_C(t) = V_{Cpeak}\sin(2\omega t) \tag{4.73}$$

$$\Delta V_C = 2V_{Cpeak} \tag{4.74}$$

$$i_C(t) = 2\omega V_{Cpeak}\cos(2\omega t)\, C \tag{4.75}$$

$$2\omega V_{Cpeak}\cos(2\omega t)\, C = \frac{P_l}{V_{DC}}\cos(2\omega t) \tag{4.76}$$

$$C = \frac{P_l}{2\omega V_{DC} V_{C,peak}} = \frac{P}{2\pi f_l V_{DC}\Delta V_C} \tag{4.77}$$

$$i_{C,rms} = \frac{P_O}{\sqrt{2}V_{DC}} \tag{4.78}$$

4.4.2.2 Output Filter

The harmonic content is also important when providing power to AC loads since there are electrical standards which need to be met for certain applications. The standard for standalone distributed sources is shown in Table 4.30 [69] To help reduce

the harmonic content of the voltage or current, output filters are implemented. The most common filters include L, LC and LCL with LCL being very common for grid tied converters due to their improved current and voltage harmonic elimination. For grid connected converters both the current and voltage harmonics have to be within a certain limit so the LCL is very common for grid connected applications while for standalone applications usually just the voltage is of concern so an LC filter is adequate.

Odd harmonics, non-multiples of 3		Odd harmonics, multiples of 3†		Even harmonics	
Harmonic order, *h*	Harmonic voltage, %	Harmonic order, *h*	Harmonic voltage, %	Harmonic order, *h*	Harmonic voltage, %
5	6	3	6	2	2
7	5	9	3.5	4	1
11	3.5	15	2	6	0.5
13	3	21	1.5	8	0.5
$17 \le h \le 49$	$2.27 \times (17/h) - 0.27$	$21 < h \le 45$	0.2	$10 \le h \le 50$	$0.25 \times (10/h) + 0.25$

**Reproduced from Table 1 of CAN/CSA-C61000-2-2.*
†The levels given for odd harmonics that are multiples of three apply to zero-sequence harmonics. Also, on a three-phase network without a neutral conductor or without a load connected between line and ground, the values of the third and ninth harmonics can be much lower than the compatibility levels, depending on the unbalance of the system.

Figure 4.30: Compatibility levels for individual harmonic voltage in low-voltage networks (rms values as a percentage of rms values of the fundamentals component [69].

Harmonic content also depends on the converter topology. The two most common topologies used for inverters are the half bridge and full bridge current source and voltage source inverters, however for this application, only the voltage source inverter will be discussed. There are a few reasons why the full bridge will be selected over the half bridge. First, as mentioned previously, the half bridge has twice the conduction loss compared with the full bridge assuming the same input voltage, output power and on-state resistance of the switch [45]. This allows selection of switches with lower current ratings, and if required, a reduction in the number of switching devices in parallel for higher power applications. Another downside to the half bridge topology

is that it can only use bipolar modulation while the full bridge can implement unipolar or bipolar modulation [40, 45]. Unipolar modulation is more ideal than bipolar modulation because it has reduced harmonic content which also results in a lower output voltage rms ripple, and a lower filter inductance. [40, 70, 71]. This reduces the required filter inductance by four times when compared with bipolar as shown in (4.80) and described in [71, 72]. Using the inductor ripple in (4.79) , the output filter inductance can be found from (4.80).

$$\Delta i_{Lf} \leq \frac{P_{O,rms}\sqrt{2}}{V_{O,rms}} 0.4 \tag{4.79}$$

$$\begin{cases} L_f = \dfrac{V_{DC}}{8 f_{SW} \Delta i_{Lf}} & unipolar \\ L_f = \dfrac{V_{DC}}{2 f_{SW} \Delta i_{Lf}} & bipolar \end{cases} \tag{4.80}$$

Assuming that both the low frequency and high frequency currents are at steady state, the low frequency rms current is the output AC current seen by the load which is (4.81), while the high frequency component due to the PWM switching is described by (4.82). Adding these together gives the rms current flowing through the filter inductor [45].

$$I_{AC,rms} = \frac{P_{O,avg}}{V_{O,rms}} \tag{4.81}$$

$$I_{Lfripple,rms} = \frac{\Delta I_{Lf}}{\sqrt{3}} \tag{4.82}$$

$$I_{Lf,rms} = \frac{P_{O,rms}}{V_{O,rms}} + \frac{\Delta I_{Lf}}{2\sqrt{3}} = \frac{P_{O,rms}}{V_{O,rms}} + \frac{0.4 P_{O,rms}\sqrt{2}}{V_{O,rms}\sqrt{3}} \tag{4.83}$$

$$I_{Lf,peak} = I_{O,peak} + \frac{\Delta i_{Lf}}{2} \tag{4.84}$$

The output filter capacitance can be calculated from (4.86) when the cut-off frequency of the LC filter is known while the capacitor rms current is equal to the high frequency AC rms component within the inductor since the capacitor is used to filter out this harmonic component.

$$I_{C,rms} = \frac{0.4 P_{O,rms}\sqrt{2}}{V_{O,rms}\sqrt{3}} \tag{4.85}$$

$$C_f = \frac{1}{(2\pi f_{cross})^2 L_f} \tag{4.86}$$

4.4.3 Component Selection

Now that the voltage and current ratings have been discussed, as well as the required component values, the selection of the components must be made. Based on the requirements in Table 3.4, the HVDC link capacitance can be found from (4.77), where its rms current is found from (4.78). For a output of 1kW, and rms output voltage of 230V, a load frequency of 50 Hz and a voltage ripple requirement of 5 percent, the required DC link capacitance is $398\mu F$. The rms current seen by the DC link capacitor can be found in (4.78) and is 2.02A. There are many options available for different combinations of capacitors in series and parallel to meet the voltage, current and capacitance requirements. It was decided to have two LLS2W221MELA capacitors in series with four groups of two in parallel providing a voltage rating of 900V and a maximum rms current rating of 6.36A and a capacitance of $440\mu F$ [73]. This will provide enough margin for the stated requirements.

Using (4.79), the inductor ripple current is 2.46A for an output rms voltage of 230V, a power of 1kW, and a ripple percentage of 40 percent. Using the calculated

ripple, the inductance found in (4.80) needs to be at least $203\mu H$, and must withstand a peak and rms current of 8.6A and 4.277A respectively when using (4.82) and (4.84). Most inductors in the range of $200\mu H$ to $2mH$ have either, low current rating, or are expensive. DENO-23-0001 is cheap and has high rated current of 16A-25A so it will be selected as the output filter [74]. This is ten times larger than the required inductance of $200\mu H$ so the ripple will be reduced.

Using this inductance value, along with designing the LC filter to have a cut-off frequency of 10 kHz, the required output filter capacitance will be $0.1267\mu F$ when using (4.84). The closest capacitance to this value is $0.1\mu F$ and using these new values the rms current seen by the capacitor is then 1.42A found from (4.85). Since this is an AC current the output filter capacitor must be able to accept AC currents. Therefore, film capacitors will be used for the output filter capacitor. A capacitor value of $0.1\mu F$ is widely available so 940C12P1K-F was selected as the filter capacitor [75].

The last component required is the inverter MOSFETs. The voltage rating must be equal to the HVDC link voltage plus some margin. In this case the largest voltage will be around 400V and with 1.5x margin this becomes 600V. The peak current seen by the switch will be the same as the peak current seen by the filter inductor, which in this case is 8.6A found from (4.84). The rms current is a bit more challenging to find, but it has been defined in [76] when calculating the conduction losses. The rms current seen by the switch can be found from (4.87), where m_a is the modulation index, and $I_{O,peak}$ is the peak of the output load current seen by the load. The rms current is then 2.9A for a HVDC bus voltage of 350V, a output voltage of 230V and a power of 1kW; assuming a resistive load. Based on these current and voltage ratings,

it was decided to choose STP28N65M2 from STMicroelectronics [77].

$$I_{rms} = I_{O,peak}\sqrt{\left(\frac{1}{8} + \frac{m_a}{3\pi}\cos\phi\right)} \tag{4.87}$$

Table 4.20: LLS2W221MELA-HVDC Link Capacitor [73]

Rated Voltage (V)	Capacitance (μF)	Rated Ripple Current (mArms)	Leakage Current (mA)
650	220	(1590)	(0.94)

Table 4.21: DENO-23-0001-LC Filter Inductor [74]

Inductance (μH)	Max Current (A)	DC Resistance ($m\Omega$)
2	16	15

Table 4.22: 940CL12PIK-F-LC Filter Capacitor [75]

Capacitance (μF)	DC Voltage Rating (V)	AC Voltage Rating (V)	ESR (mΩ)	Ipeak (A)	Irms @ 70°C kHz (Arms)
0.1	1200	500	9	114	6.1

Table 4.23: STP28N65M2- MOSFET [77]

V_{DC} (V)	$I_{D25°C}$ $I_{D100°C}$(A)	R_{DSon} (Ω)	C_{oss} (pF)	Q_G (μC)	T_{jmax} (°C)	t_r (ns)	t_f (ns)	t_{rr} (ns)	Q_{rr} (μC)
450	20,13	(0.15)	(115)	(1.83)	(150)	10	8.8	384	(8.2)

This chapter went into the converter design of each individual converter within the integrated system. The operation, waveforms, equations, and component selection for each converter was discussed with more focus on the inductor design for the boost

converter and the PSFB converter design. The inductor design was for a single phase system and was optimized around the lowest volume. The core material selected was 3C97 from Ferroxcube while a comparison between different Litz windings and rectangular windings was done to see which winding type achieved the lowest volume and losses. The Litz winding was assumed to be built from New England Wire while the rectangular winding was customized within GA. The rectangular winding achieved the lowest losses and volume so it was selected. Due to long lead time and cost the boost converter was changed into a three phase interleaved boost converter and off-the-shelf inductors from CoilCraft were bought to test the prototype. A comparison in simulation between the GA designed inductor and the CoilCraft inductors will be done in following chapters. The PSFB converter design used compared different leakage inductor, output filter inductor and number of turns values for a 250W and 1kW system. The phase shift condition for achieving ZVS and the desired output voltage is not always mutual so only under specific conditions does each occur. As such, the design values are selected to ensure this does occur even at low powers.

Chapter 5

Control and Hardware Implementation

5.1 Implemented Control Technique

There are many different control methods in literature, some more complex than others and each have their advantages and disadvantages. Some of the more common control methods include voltage mode, average current mode, peak current, sliding mode, and fuzzy logic. Voltage control implements one control loop where the measured voltage is compared to the desired voltage and the error between these two values is sent to the voltage loop PI controller [40]. The output of the voltage loop is then used as the duty cycle value and is compared to the gate drive triangular signal which generates the PWM gate signal [40].

Current mode incorporates an extra control loop in which the output of the voltage control is used as the current reference for the inner current loop. This reference is compared with the measured current and the error is sent to the current PI controller.

The output of the PI is the duty cycle value which is fed to the PWM generation for the gate signal [40].

For peak current control the peak current is measured and used to control the duty cycle of the converter [78]. The controller will increase the measured current up to the desired value and then once the current is at the desired value the current begins to decrease. It has a few advantages such as overcurrent protection by controlling the peak current. This is ideal if the peak current has a specific limit. However, for high switching frequencies, the bandwidth must be high and finding a current sensor that is cheap with high bandwidth and high current abilities can be a challenge if an off-the-shelf current sensor is used [79, 80]. Other techniques are available which help with this limitation. There are also subharmonic oscillations which require mitigation usually in the form of slope compensation which is not required in average mode current control [80]. There have been many improvements to traditional peak current control such as improved compensation strategies, sensor less and predictive control methods [79, 81, 82].

Sliding mode current control [83,84] implements discontinuous control which drives the system state onto a control surface of the state-space system. One advantage to sliding mode control is its insensitivity to parametric variation and external influences [85]. However, it is subject to chattering which is due to the fast dynamics of switching across the sliding surface usually caused from non-modeled effects which propagate through the system and influence the output [85].

5.1.1 Boost/Buck Converter Control

For the boost and buck converters it was decided to implement the average mode current control method due to its simplicity and improved stability versus single loop control [86]. Average mode current control implemented in the buck and boost converter is shown in Fig. 5.1 and Fig. 5.2 respectively.

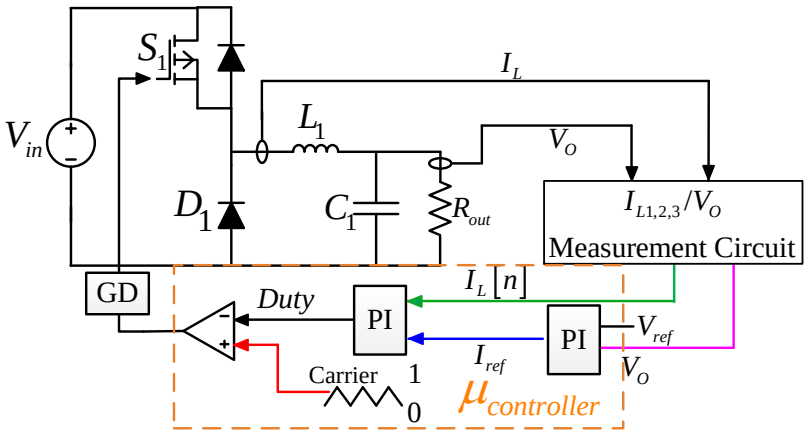


Figure 5.1: Average mode current control for Buck converter.

The output voltage is measured using a voltage measurement technique. This will convert the voltage into a low voltage equivalent in the range of 0V to 3V. This voltage is processed by the microcontroller and within the controller the voltage level is processed and converted back into its actual voltage to be processed by the microcontroller. This actual voltage within the microcontroller is then compared to the desired reference output voltage of the buck converter. The error is sent to the voltage PI controller and then the output of the PI is compared with the measured inductor current. The error between these values is sent to the current loop PI controller to generate the required duty cycle value used in the PWM generation. The PWM gate signal is then sent to the gate driver circuit which applies the PWM gate signal to the switch which will control the main circuit.

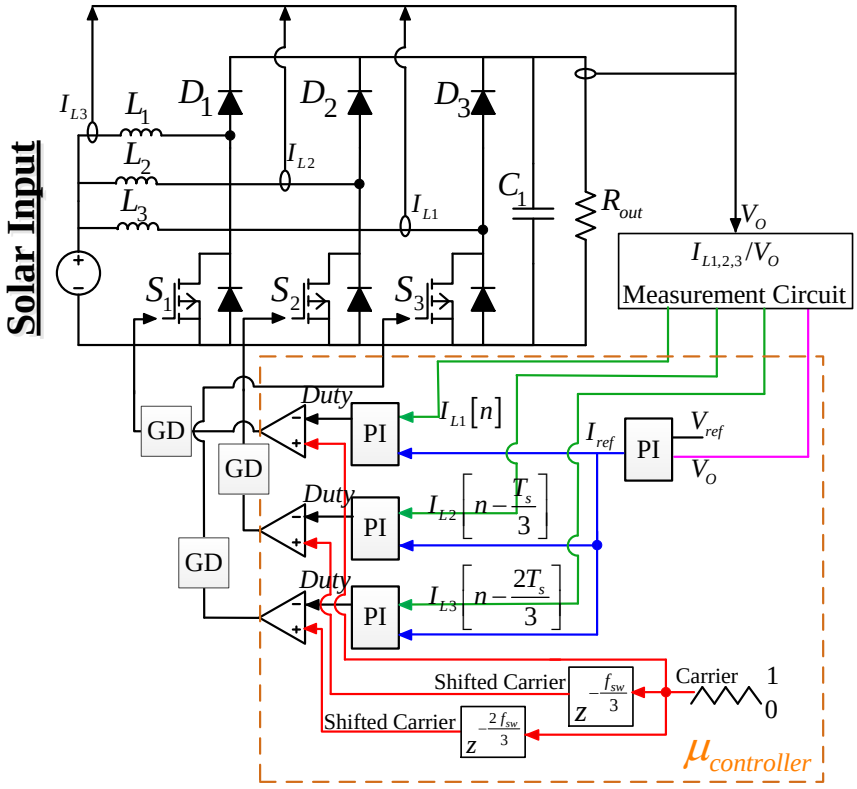


Figure 5.2: Average mode current control for 3 phase interleaved boost converter.

Since this is an interleaved three phase boost converter, the carrier signal within the microcontroller needs to be phase shifted. Phase two will be phase shifted by a third of the switching period while phase three requires two thirds, ensuring equal current sharing. The midpoint sampling locations must also be at the same points for each phase. Therefore, the triggering of the sampling locations must be at the min and max locations of the carrier signal, assuming the carrier is triangular as shown in Fig. 5.4.

When taking the current samples for average mode current control it is much easier to use a triangular carrier than it is using a saw tooth carrier because the min and max points of the triangular carrier align exactly with the midpoints of the inductor current for different duty cycle values, while the saw tooth clearly does

not align with the midpoints of the inductor current as seen in Fig. 5.3. The red dashed lines indicate the midpoint locations of the DC inductor current. Clearly, the midpoints of the current waveforms are always aligned with the min and max locations of the triangular waveforms at any duty cycle value. If the current is not sampled at the same locations for each phase, unequal current sharing occurs because the measured currents will be different for each phase which means the duty cycle values will be different. This results in different on and off times for the phases which means there will be different currents in each phase. Technically, if each phase has the same switching devices and components, the current flowing through each phase should be the same for the same duty cycle reference. This will reduce the amount of current sensors, however each phase cannot be controlled so it is not the best practice. The boost and buck PI parameters were found using MATLABs PID tool and after some manual adjustments. Table 5.1 shows the PI parameters for both the boost and buck converters and will be implemented within the controller in the same manner shown in Fig. 5.1 and Fig. 5.2.

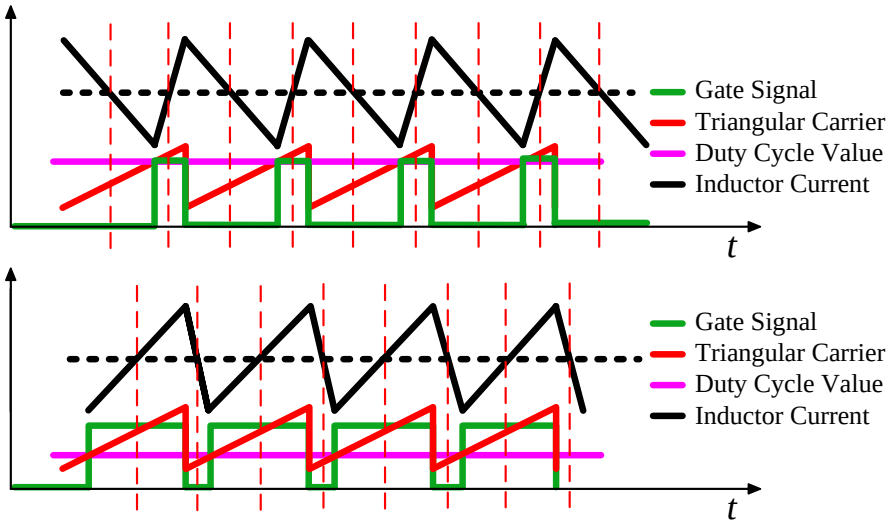


Figure 5.3: saw-tooth carrier PWM generation.

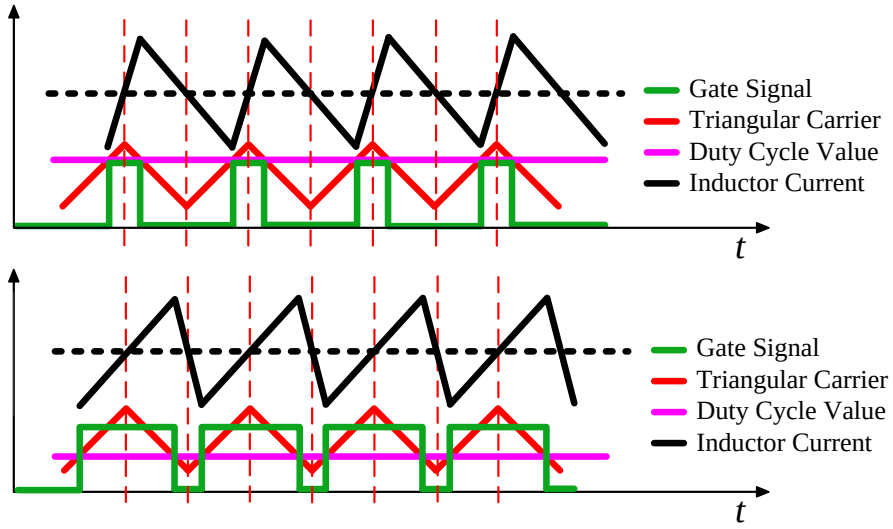


Figure 5.4: triangular carrier PWM generation.

Table 5.1: Boost/Buck PI Parameters

	Voltage Loop			Current Loop		
	ki	kp	sampling freq (kHz)	ki	kp	sampling freq (kHz)
Boost	20	0.5	100	0.08	0.03	200
Buck	10	0.1	100	1	0.05	200

5.1.2 PSFB Converter Control

For the isolated PHFB converter only voltage mode control will be implemented as shown in Fig. 5.5 below. As was mentioned in the inverter section, there will be an AC ripple on the DC link voltage due to the AC component of the AC load which will propagate onto the HVDC link bus which is shown in Fig. 4.29. If nothing is done, this ripple will influence the control of the PSFB converter since the frequency of the AC ripple is double the AC load frequency. For this application, the AC ripple will have a frequency of 100 Hz, or double the load frequency, while the sampling rate will

be 50 kHz. As the controller samples the voltage, it will try to push the positive and negative halves of the AC signal to the reference voltage which will cause improper action and possibly impose a larger AC ripple as the controller tries to correct the voltage. As such, the sampled voltage used in the PI controller needs to be close to the DC value for proper operation.

Even after adding the designed DC link capacitors, there may still remain an AC component. Therefore, it was decided to use a notch filter to filter out the 100 Hz AC component, as shown in Fig. 4.29. In reality the AC component will remain, but the controller will be able to filter out the AC data so that the DC voltage can be controlled.

As was mentioned in section 4.3 for PSFB converter implementation, each switch has the same duty cycle value reference but the control comes from the phase shift between leading and lagging legs within the PSFB converter. Only half of the switching period can be used since the operation for duty cycles greater than 50 percent is the exact same as those lower than 50 percent. Meaning, a phase shift value of 25 percent will provide the same output voltage as a phase shift of 75 percent, or if the value is 40 percent it is analogous to 60 percent. The only difference is that the leading and lagging legs switch as shown in Fig. 5.7 and Fig. 5.8. Based on the dead time the constant duty cycle for each switch is found from 5.1 where t_{dead} is the dead time. Therefore, for a dead time of 80ns, the constant duty cycle value will be 0.496. The internal PI voltage loop controller is shown with the calculated PI parameters in Table 5.2. Again, the PI parameters were found using PID tool from MATLAB and with some trial and error tuning. Obviously a more in-depth control method is required, however this is beyond this work.

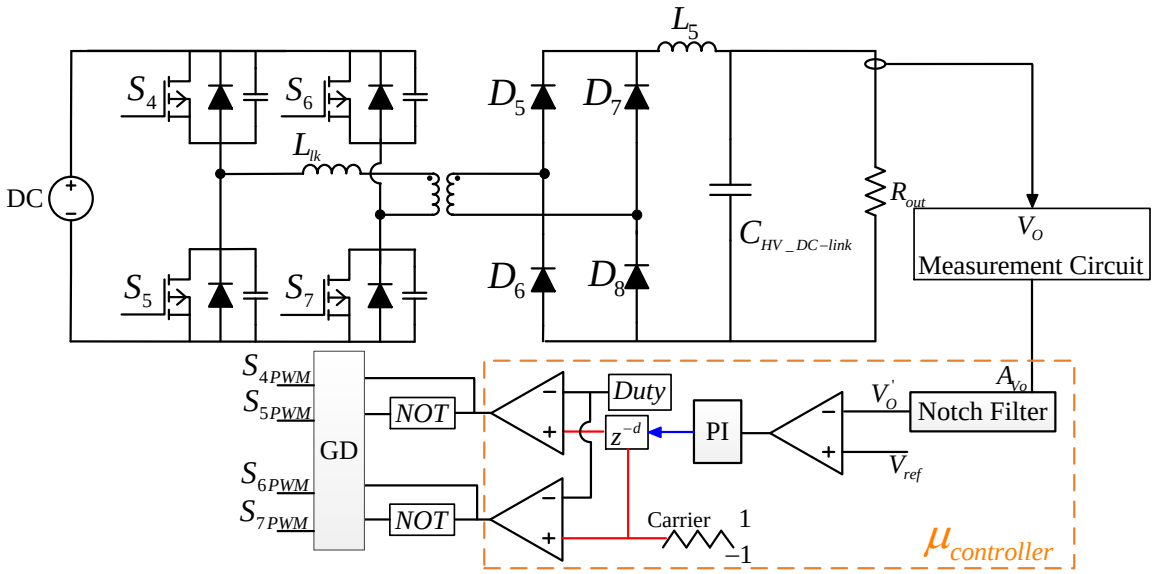


Figure 5.5: PSFB converter using voltage mode control.

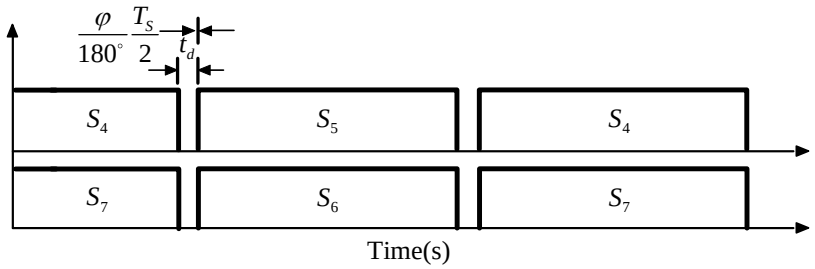


Figure 5.6: PSFB PWM generation 50 percent phase shift.

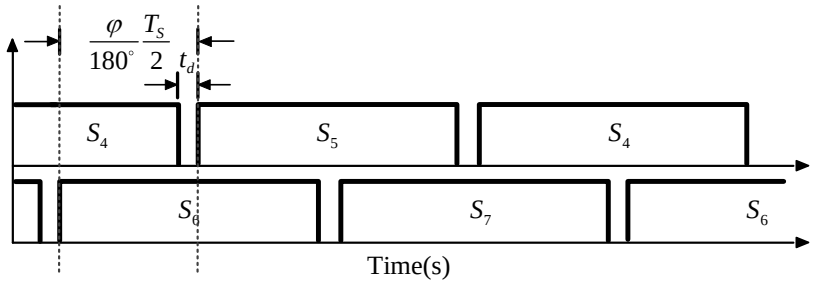


Figure 5.7: PSFB PWM generation 25 percent phase shift.

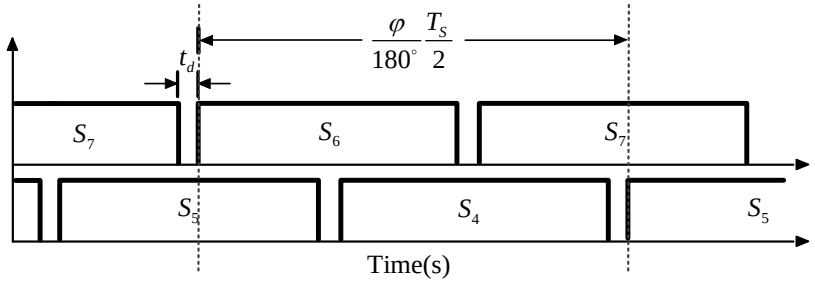


Figure 5.8: PSFB PWM generation 75 percent phase shift.

$$D_{New} = \left(\frac{1}{2f_{sw}} - t_{dead} \right) f_{sw} \tag{5.1}$$

Table 5.2: PSFB PI Parameters

Ki	Kp	Sample Frequency (kHz)
0.4	0.01	100

5.1.3 Single Phase Inverter Control

For single phase VSI there are a many analog and digital control methods such as hysteresis band, predictive, droop control, space vector pulse width modulation (SVPWM), and sinusoidal pulse width modulation (SPWM) control techniques [87, 88]. However again, an in-depth control method is beyond this work so a simple PI based control technique will be used here.

The difference with the inverter is that the carrier has to be a sinusoid that ranges from negative one to positive one and has a carrier frequency that matches the output load frequency, which in this case is 50 Hz. The triangular carrier is also different as it now goes from negative one to positive one as well, instead of just zero to one as is the case for PWM generation. The frequency of the triangular waveform is at the switching frequency. The waveforms for bipolar and unipolar SPWM can be found in [40] so they will not be shown here. But basically, the difference between unipolar and bipolar can be seen from the gating signal in Fig. 5.9 and Fig. 5.10. For bipolar modulation, switches S_9, S_{12} and S_{10} and S_{11} use the same gate signal, while for unipolar the gate signals for S_9 and S_{12}, S_{10} and S_{11} are out of phase by 180°. The advantages unipolar provides were already discussed in Chapter 4 so they will not be mentioned again, but it was decided to use unipolar for the inverter. A voltage

loop PI controller will be used to control the single phase inverter and is shown in Fig. 5.11 below, where m_a is the modulation index. Table 5.3 shows the voltage PI controller parameters that will be implemented for this controller.

Table 5.3: Single Phase Inverter PI Parameters

Ki	Kp	Sample Frequency (kHz)
1	0.01	25

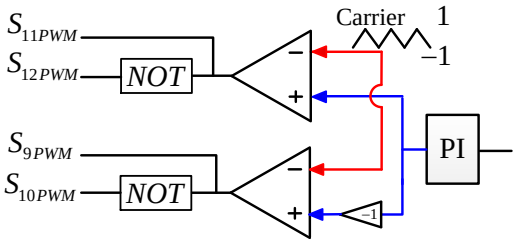


Figure 5.9: Unipolar SPWM.

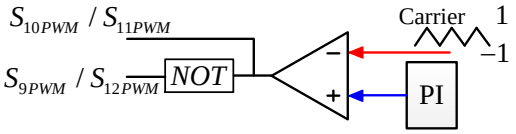


Figure 5.10: Bipolar SPWM.

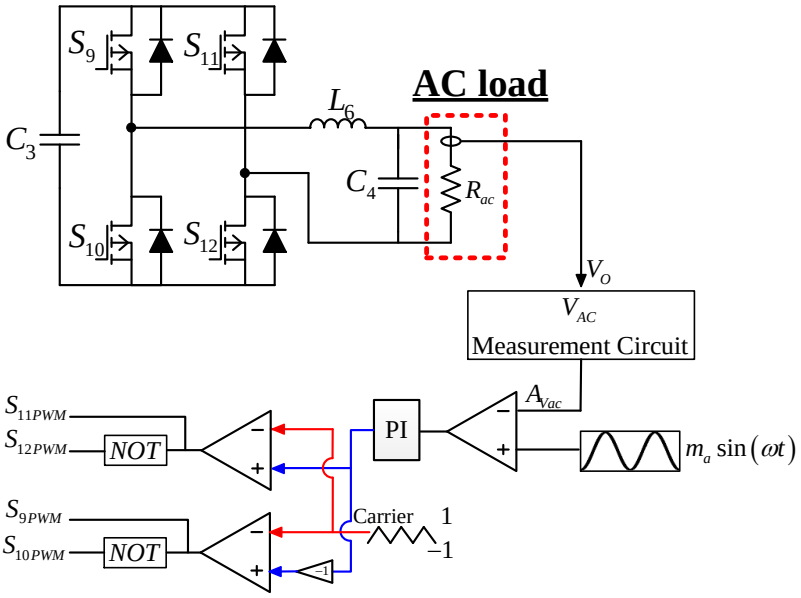


Figure 5.11: Single phase inverter voltage mode control using unipolar SPWM.

5.2 Hardware

5.2.1 Gate Driver

The gate driver for each switch will be 2ED020I12-F2 2A IGBT/MOSFET isolated gate driver from Infineon [89]. It is an isolated half bridge gate driver able to provide 2 amps to each switch. The bipolar configuration was used, as shown in Fig. 5.12, since it has a negative turn-off supply which will turn the switch off faster than the unipolar configuration which only has a turn-off voltage of zero volts. The supply for the gate driver V_{CC} and V_{EE} is provide from VQA-S15-D15-SIP isolated power supply from CUI INC. which will provide the +15V/-8V on/off voltages. The +5V supply is provided from the linear voltage regulator MIC5205. The 2ED020L12-F2 gate driver has many features such as: Active miller clamp, short circuit clamping, desaturation protection, and active shut down.

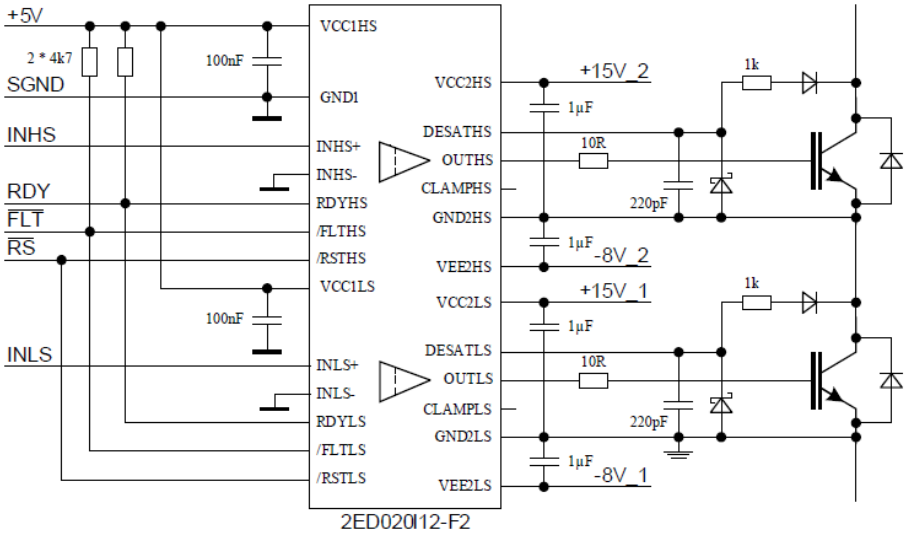


Figure 5.12: Bipolar mode of 2ED020M2-F2 gate driver [89].

5.2.2 DSP

The voltage and current measurements will be converted to 3V to operate correctly with the TMS320F28335-DSP by TI. This DSP has an operating clock of 200MHz, it has a total of 12 PWM channels, and 24 ADC channels. The EPWM modules are used to drive the gate drivers of each switch within the integrated converter at the desired switching frequency. Each EPWM output has two PWM signal outputs; EPWMA and EPWMB.

5.2.3 Current and Voltage Measurement

Most common current and voltage measurement techniques include: Shunt resistor, Current Transformer, Hall effect sensor, and Voltage divider. One thing to note is that depending on the current and voltage level, certain methods are more suitable than others. Based on the proposed specifications in Table 3.4 it is required that the high voltage AC and DC be isolated from the LV digital control circuit. For the boost converter both the phase current and the output voltage will need to be measured to implement average mode current control. Since this is average mode and not peak control, the bandwidth of the current sensor does not need to be able to pick up the high frequency current ripple at 100 kHz because only the DC current is required. This allows a wider selection of current sensors from the available selection on Digikey/Mouser websites. The peak current through each phase was estimated to be 21.1A so a phase current sensor with 40A tolerance should be adequate for this application. Selecting a current sensor with a high current rating means that the current resolution will be poor and so the current sensor max current rating should

not be too high. As such, it was decided to select ACS723LLCTR-40AU from Allegro for both the boost and buck current measurement. For the voltage measurements, all of them will be done with LEM 25-P voltage transducer. Fig. 5.13 to Fig. 5.13 show the current and voltage measurement circuits that will be used here in.

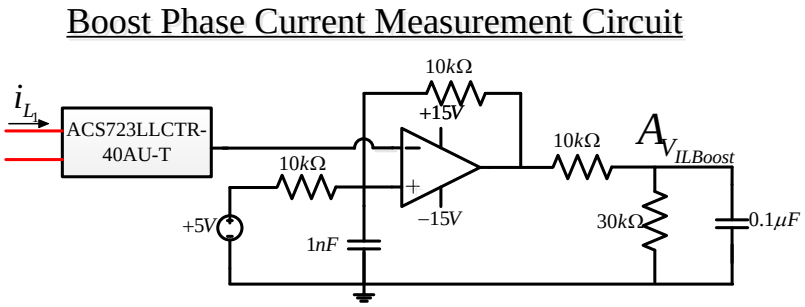


Figure 5.13: Boost converter phase current measurement circuit.

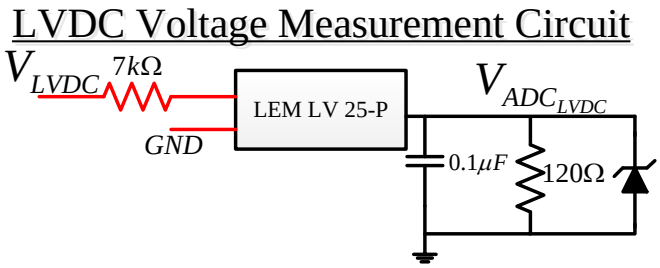


Figure 5.14: LVDC voltage measurement circuit.

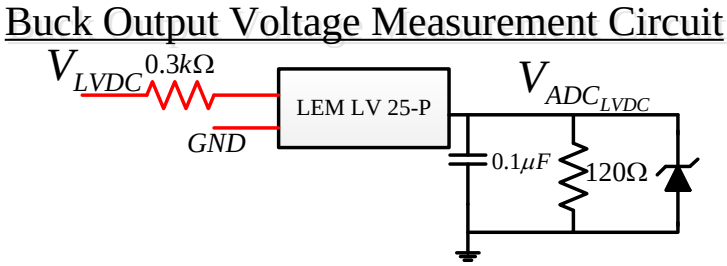


Figure 5.15: Buck output voltage measurement circuit.

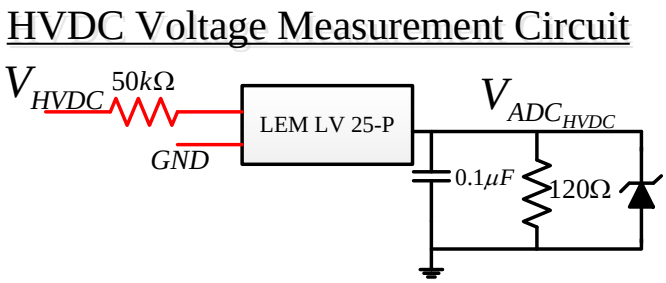


Figure 5.16: HVDC link voltage measurement circuit.

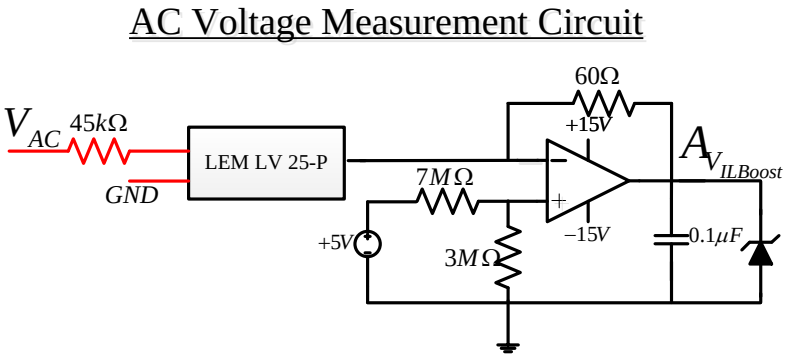


Figure 5.17: AC load voltage measurement circuit.

5.2.4 PCB

Fig. fig:PCB and Fig. 5.19 show the designed PCB in Altium and the manufactured PCB respectively.

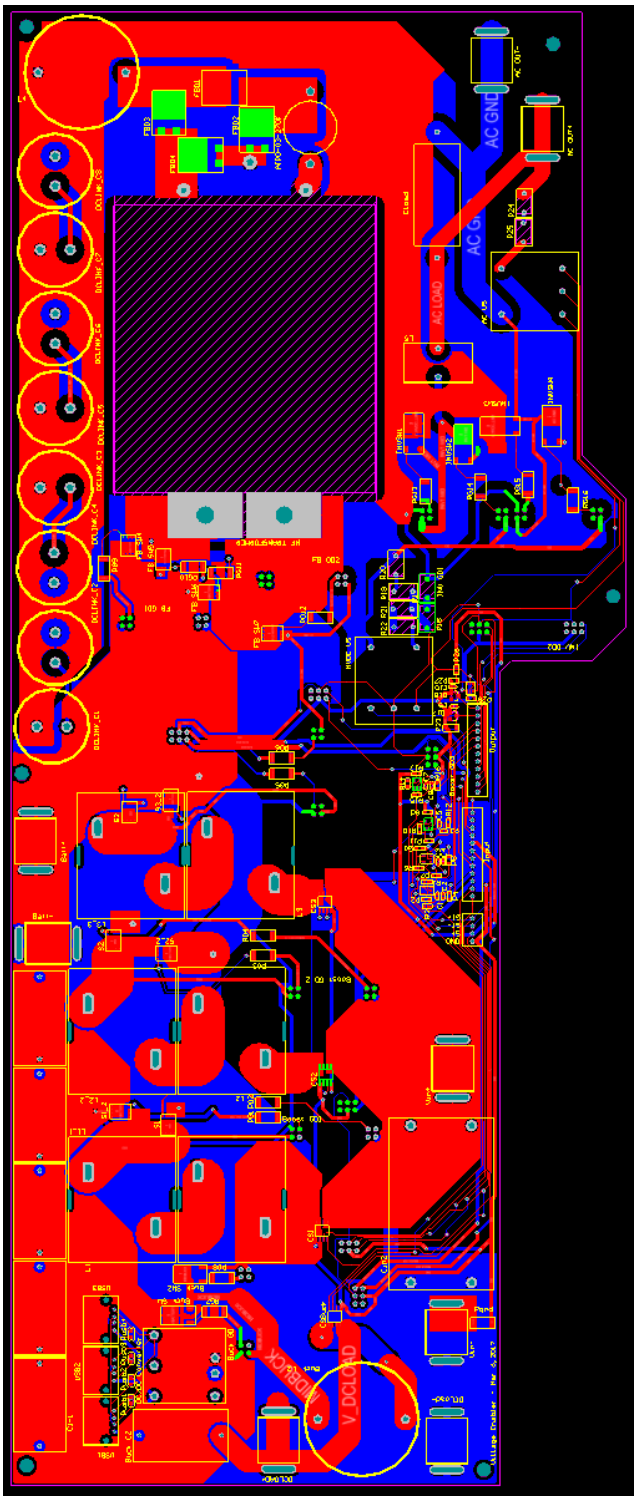


Figure 5.18: Altium PCB layout.

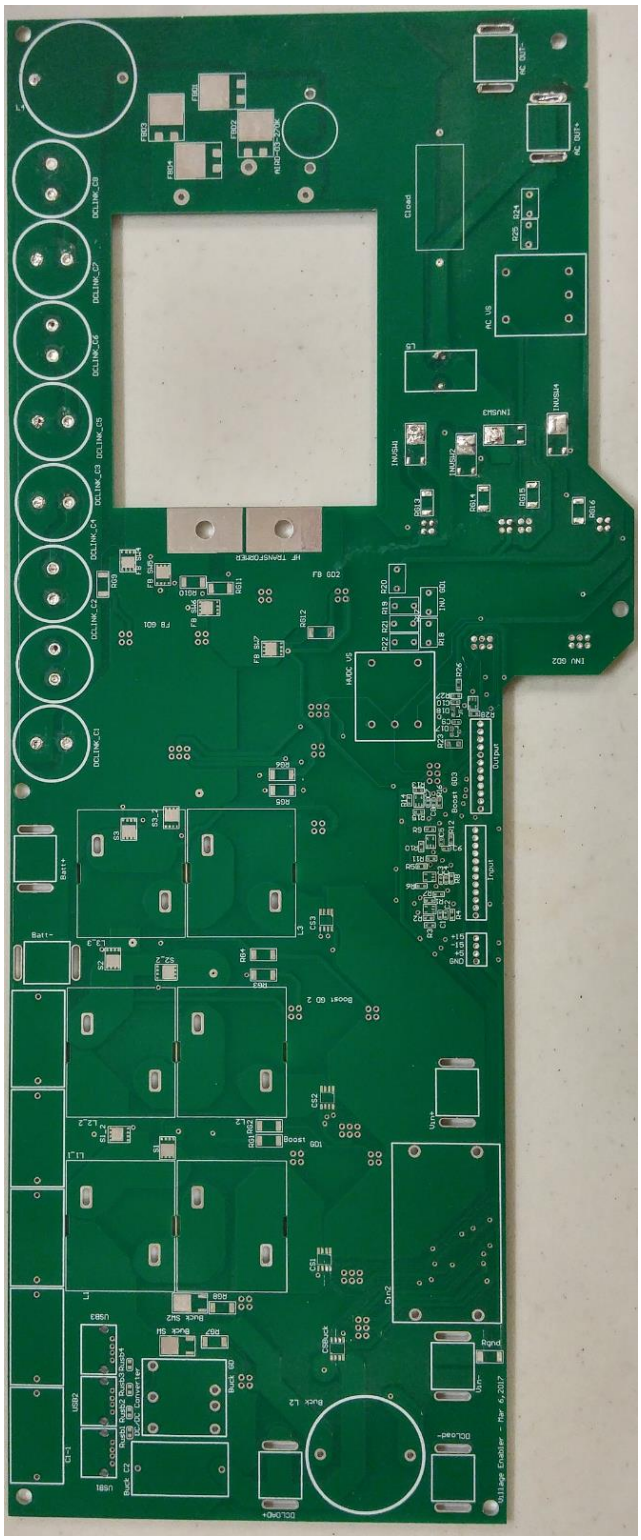


Figure 5.19: Manufactured PCB.

In this chapter the control and hardware for the simulation and prototype was discussed. The control method for each of the converters within the integrated system was discussed and defined. The boost and buck converters will implement the average mode current control while the PSFB and inverter will implement voltage mode control. For the PSFB there will be an AC voltage component on the HVDC link that much be filtered before sending it to the voltage PI loop. As such, a notch filter is used to filter the double line frequency of the AC load, which in this case is 100Hz. For the hardware all gate drivers will use the isolated dual channel Infineon gate driver 2ED020I12-F2, while all the voltage measurements will be gathered using LEM 25-P voltage transducers. The current measurements for the boost and buck phase currents are done using the 40A ACS723LLCTR-40AU hall-effect current sensors from Allegro. The DSP used is TMS320F28335 from Texas Instruments. Finally, the integrated PCB is also shown for reference.

Chapter 6

System Modeling, Simulation, Analysis and Efficiency Assessment

The component parameters for the integrated power electronic system must be defined in order to model the system losses accurately. Some of the loss calculations have already been mentioned, however some have yet to be defined. The following sections will discuss the required equations to estimate the losses for each component within the integrated converter. Once the general equations are defined, the loss equations for each converter will be shown and discussed. These will then be used during and run with the converter models in MATLAB/Simulink. This will provide an estimate of the losses which will be compared with experimental tests of the converters.

6.1 Loss Equations of System Components

6.1.1 Gate Driver Operation

Fig. 6.1 shows the internal circuit of the MOSFET while Fig. 6.2a and Fig. 6.2b show the turn-on and turn-off transitions and waveforms respectively. The transitions will be broken down into the listed sections to better understand the operation and internal workings during each transition.

During transition (1), the gate current charges both C_{GS} and C_{GD} as is seen by the rise of the gate to source voltage V_{GS} reaching the threshold voltage by the end of (1) [90–93]. (1) is known as the turn-on delay time since no current or voltage changes during this transition.

During (2), V_{GS} has reached the threshold voltage V_{th} and continues to rise until the plateau voltage $V_{plateau}$ [90–93]. I_{DS} starts conducting through the MOSFET as it rises and reaches its maximum value at the end of (2) [90–93]. This is the total on current the MOSFET will see.

During (3), I_{DS} remains constant at the maximum on state current while V_{GS} remains constant at the plateau voltage [90–93]. The MOSFET is now allowing the full amount of conduction current and because of this, C_{DS} begins to discharge as indicated by V_{DS} decreasing during this transition [90–93]. (3) is known as the fall-time in relation to the falling V_{DS} [90–93]. At the end of transition (3), V_{DS} and I_{DS} have reached their final values and will remain at these values until the turn-off transition period [90–93].

During (4) V_{GS} continues to rise beyond the plateau voltage due to the charging of C_{GS} and C_{GD} to its final value at the end of (4) [90–93]. This value of V_{GS} is the one

used to determine the on-resistance of the MOSFET during gate driver design [90–93].

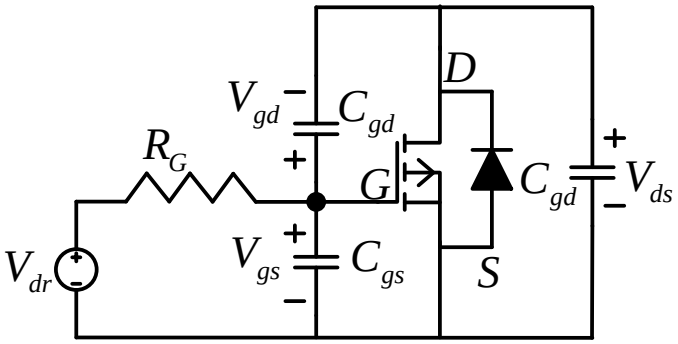


Figure 6.1: Inverter MOSFET circuit [40],[45].

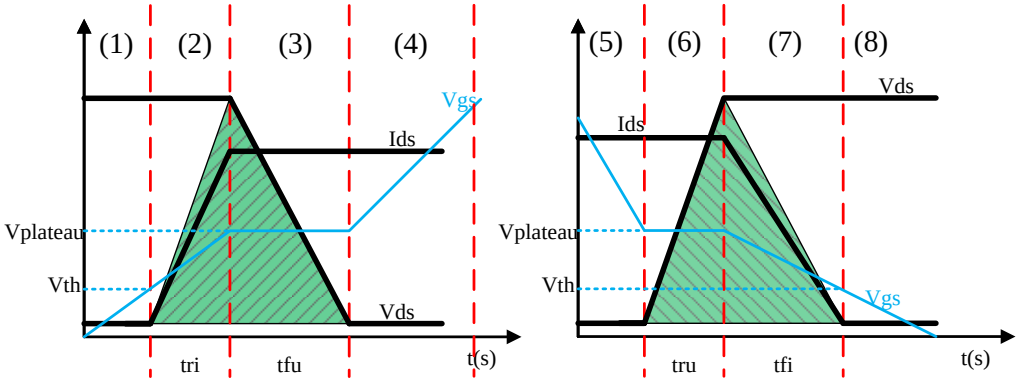


Figure 6.2: MOSFET turn-on and turn-off switching waveforms [40],[45].

The turn-off transition is broken down into sections (5) to (8) as shown in Fig. 6.2b During (5), the gate voltage drops from its fully on value to the plateau value due to the discharging of C_{GD} and C_{GS} [90–93]. (5) is known as the turn-off delay since V_{DS} and I_{DS} remain unchanged during this transition [90–93].

Once V_{GS} reaches the plateau voltage it remains constant at this value during transition (6), while V_{DS} rises from its on voltage $I_{DS}R_{DSon}$ to its off voltage V_{DS} and remains at this value until the turn-on transition [90–93]. I_{DS} remains constant during this transition until the end of (6) [90–93]. (6) is known as the voltage rise time, t_{ru}, in relation to the rising V_{DS} [90–93].

During transition (7), V_{GS} goes from the plateau voltage to the threshold voltage

while I_{DS} goes from its fully on current to its off current [90–93]. This is known as the fall time, t_{fi}, of the conduction current and at the end of transition (7), the MOSFET is fully off since V_{DS} and I_{DS} have reached their final values [90–93].

During transition (8) the MOSFET is fully off so the only thing left is to fully discharge the input capacitors as shown by the continued decrease in V_{GS} past the threshold voltage [90–93]. Transition (1)-(4) is the amount of time needed to fully turn the MOSFET on while (5)-(8) is the amount of time needed to turn the MOSFET fully off [90–93]. The green area represents the turn-on and off energy generated during both transitions and is needed to determine the switching losses of the MOSFET. As is well known, power equals voltage times current and the green areas are the times where power is generated during these on-off transitions as will be discussed next [90–93].

6.1.2 MOSFET Losses

Switching losses are broken down into turn-on and turn-off losses. As was discussed, the green areas of Fig. 6.2a and Fig. 6.2b are the energies generated during these transitions and must be quantified to determine the efficiency of any converter which uses them. The total MOSFET loss is shown in (6.1) where f_{sw}, E_{onM} and E_{offM} are the switching frequency, MOSFET turn-on energy and MOSFET turn-off energy respectively [94].

$$P_{swM} = (E_{onM} + E_{offM})\, f_{sw} \tag{6.1}$$

The turn-on and off energies are further broken down using the rise and fall times of the on-state current, the drain to source voltage, gate capacitance, gate plateau voltage, and gate resistance. The turn-on and off energies are shown in (6.2) and

(6.3) respectively where t_{ON} is the time from the beginning of (2) to end of (3) in Fig. 6.2a and described by (6.4), while t_{OFF} is the time from the end of (5) to the end of (7) in Fig. 6.2a and described by (6.5) [94]. Q_{rr} is the reverse recovery of the body diode, t_{ri} and t_{fi} are the current rise and fall times provided in the datasheet, t_{fu} and t_{ru} are the voltage fall time and rise times which need to be calculated since they are dependent on the gate current flowing through the gate to drain capacitance (C_{GD},C_{rss}) shown in Fig. 6.3 for IPP083N10N5 [58].

$$E_{on} = V_{DS} I_{DSon} t_{ON} + Q_{rr} V_{DS} \tag{6.2}$$

$$E_{off} = V_{DS} I_{DSoff} t_{OFF} \tag{6.3}$$

$$t_{ON} = \frac{t_{ri} + t_{fu}}{2} \tag{6.4}$$

$$t_{OFF} = \frac{t_{ru} + t_{fi}}{2} \tag{6.5}$$

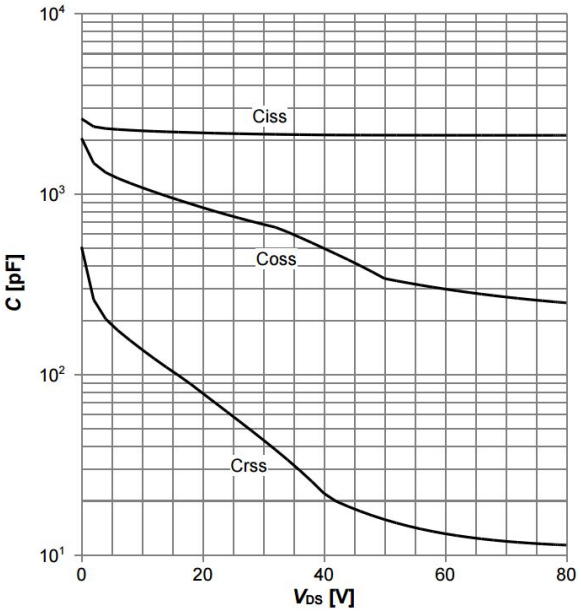


Figure 6.3: Typical MOSFET capacitance vs V_{DS} [58].

The accuracy of the voltage rise and fall times depends on how accurate C_{GD} is calculated. One method takes two points on Fig. 6.3, as explained in [94] and calculates the average of the fall times t_{fu1} and t_{fu2} and rise times t_{ru1} and t_{ru2} shown in equations (6.6) to (6.9) resulting in the new on and off times (6.10) and (6.11) respectively.

$$t_{fu1} = \frac{(V_{DS} - R_{DS_{ON}} I_{ds})\, R_G C_{GD1}}{V_{Dr} - V_{plateau}} \tag{6.6}$$

$$t_{fu2} = \frac{(V_{DS} - R_{DS_{ON}} I_{ds})\, R_G C_{GD2}}{V_{Dr} - V_{plateau}} \tag{6.7}$$

$$t_{ru1} = \frac{(V_{DS} - R_{DS_{ON}} I_{ds})\, R_G C_{GD1}}{V_{plateau} - V_{Dr}} \tag{6.8}$$

$$t_{ru2} = \frac{(V_{DS} - R_{DS_{ON}} I_{ds})\, R_G C_{GD2}}{V_{plateau} - V_{Dr}} \tag{6.9}$$

$$t_{on} = t_r + \frac{t_{fu1} + t_{fu2}}{2} \tag{6.10}$$

$$t_{off} = t_f + \frac{t_{ru1} + t_{ru2}}{2} \tag{6.11}$$

Equations (6.10) and (6.11) are then used in (6.2) and (6.3) to find the total turn-on and turn-off losses. Another more accurate method proposed in [95] takes the same idea proposed in [94] but instead of averaging over two points, the output capacitance is broken down into much smaller sections which are averaged and then added together to get the total capacitance. This is because the capacitance verses drain voltage is a non-linear function shown in Fig. 6.3, so breaking this figure down into smaller sections will give a more accurate result [95]. The voltage fall and rise times can then be explained via (6.12)-(6.15) when applying this method, where n is the current data point [95]. It is up to the designer to define how many discrete points they want to break Fig. 6.3 up into.

$$\Delta t_{fu} = \frac{\left(V_{DS}\left(n\right) - V_{DS}(n-1)\right) R_G \left(C_{GD}\left(n\right) + C_{GD}\left(n-1\right)\right)}{2\left(V_{Dr} - V_{plateau}\right)} \tag{6.12}$$

$$t_{funew} = t_{fuold} + \Delta t_{fu} \tag{6.13}$$

$$t_{fu} = \sum_{i=1}^{n} \Delta t_{fu}\left(i\right) \tag{6.14}$$

$$\Delta t_{ru} = \frac{\left(V_{DS}\left(n\right) - V_{DS}\left(n-1\right)\right) R_G \left(C_{GD}\left(n\right) + C_{GD}\left(n-1\right)\right)}{2\left(V_{plateau} - V_{Dr}\right)} \tag{6.15}$$

$$t_{runew} = t_{ruold} + \Delta t_{ru} \tag{6.16}$$

$$t_{ru} = \sum_{i=1}^{n} \Delta t_{ru}\left(i\right) \tag{6.17}$$

The old values are added to the new values and the process continuous until the entire

range has been covered. All the small sections are added together to get the total voltage rise and fall times to be used in (6.16) and (6.17) to find the total turn-on and turn-off times respectively [95]. These are then used in (6.2) and (6.3) to calculate the turn-on and off energies. For the conduction losses, the average current flowing through the MOSFET during its on time will be required. The average MOSFET conduction loss equation is shown in (6.18) where R_{DSon} is the on-state resistance and I_{Drms} is the on-state rms conduction current flowing through the MOSFET.

$$P_{Mcond} = R_{DSon} I_{Drms}^2 \tag{6.18}$$

The constant on-state resistance can be found in the datasheet, shown in Fig. 6.4, however a more accurate estimation incorporating the temperature dependence is shown in Fig. 6.5 [58]. Using a look up table or by curve fitting the data, this curve can be used to calculate a more accurate on-state resistance taking the temperature effects into account. For this work, curve fitting was completed for each switch used within the integrated converter. Finally, the total MOSFET loss can be found in (6.19) taking into account conduction and switching losses [94].

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	V_{DS}=V_{GS}, I_D=49 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	1	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	7.3 8.9	8.3 11.0	mΩ	V_{GS}=10 V, I_D=73 A V_{GS}=6 V, I_D=37 A
Gate resistance[1)]	R_G	-	1.2	1.8	Ω	-
Transconductance	g_{fs}	48	96	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=73 A

Figure 6.4: Static characteristics for IPP083N10N5 [58].

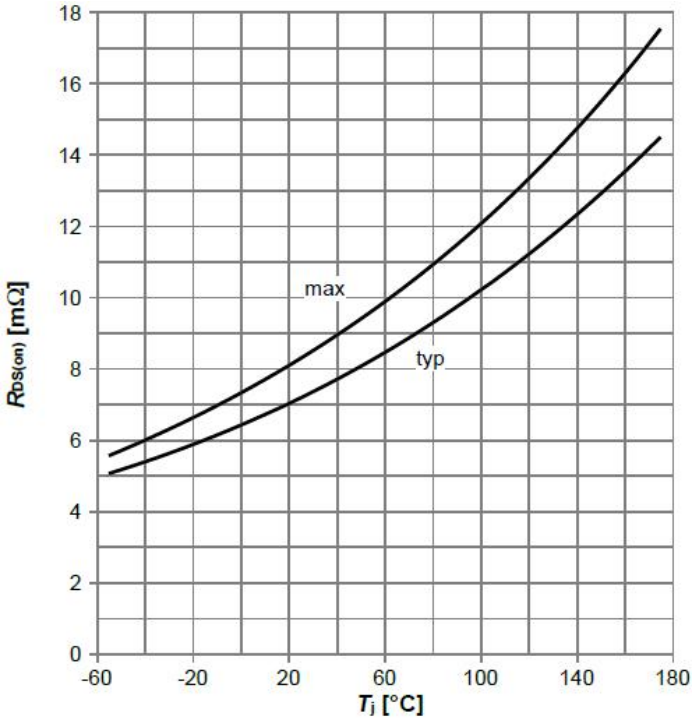


Figure 6.5: $R_{DS(on)}$ vs junction temperature for IPP083N10N5 [58].

$$P_{Mtotal} = P_{Mcond} + P_{Msw} = R_{DSon} I_{Drms}^2 + (E_{onM} + E_{offM})\, f_{sw} \tag{6.19}$$

6.1.3 Diode Losses

The diode losses are also broken down into conduction and switching losses with the switching losses coming from reverse recovery effects of the diode. Turn-off effects of the diode are ignored so only the turn-on reverse recovery losses are taken into account [94]. The turn-on energy of the diode can be found using (6.20) where V_{Drr} is the voltage across the diode during reverse recovery and Q_{rr} is the reverse recovery charge which is found in the datasheet shown in Fig. 6.6 for the body diode of IPP083N10N5 [58]. The same method applies for normal diodes as well. The power loss is then found by multiplying the energy by the frequency shown in (6.21) [94].

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continous forward current	I_S	-	-	73	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	292	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	1.0	1.2	V	V_{GS}=0 V, I_F=73 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	58	116	ns	V_R=50 V, I_F=I_S, di_F/dt=100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	118	236	nC	V_R=50 V, I_F=I_S, di_F/dt=100 A/µs

Figure 6.6: Reverse recovery charge for IPP083N10N5 [58].

$$E_{onD} = \frac{1}{4} Q_{rr} V_{Drr} \tag{6.20}$$

$$P_{Dsw} = E_{onD} f_{sw} = \frac{1}{4} Q_{rr} V_{D_{rr}} f_{sw} \tag{6.21}$$

The diode conduction losses can be found from (6.22) in which the diode is modeled as a series connection of the on state voltage, V_{D0}, and the diode on state resistance R_D. V_{D0} multiplied by the average current flowing through the diode I_{Dav} and R_D is multiplied by the square of the rms current flowing through the diode I_{Drms}.

$$P_{Dcond} = V_{D0} I_{Dav} + R_D I_{Drms}^2 \tag{6.22}$$

V_{D0} and R_D are found using the technique discussed in [94] and shown in Fig. 6.7 for IPP083N10N5 [58]. R_D can be found by finding the slope of the tangent line between two points on one of the temperature curves while the x intercept of this tangent line is V_{D0}. One thing to notice about Fig. 6.7 is that it has a log scale on the y axis so for large forward currents, the tangent line would have a negative x-intercept. Therefore, for datasheets which provide log scaled data, converting it to a normal scale ensures the x-intercept is always positive. This can be done by collecting the data and converting it into a non-log form. One thing to note is that the body diode for the boost and buck converters will not conduct so it will be ignored but the top diode in the boost and bottom diode in the buck will conduct so apply the same

method. The total diode losses can now be found using (6.23) taking into account the switching losses in (6.21) and conduction losses in (6.22).

$$P_D = P_{Dcond} + P_{Dsw} = V_{D0} I_{Fav} + R_D I_{Frms}^2 + \frac{1}{4} Q_{rr} V_{Drr} f_{sw} \tag{6.23}$$

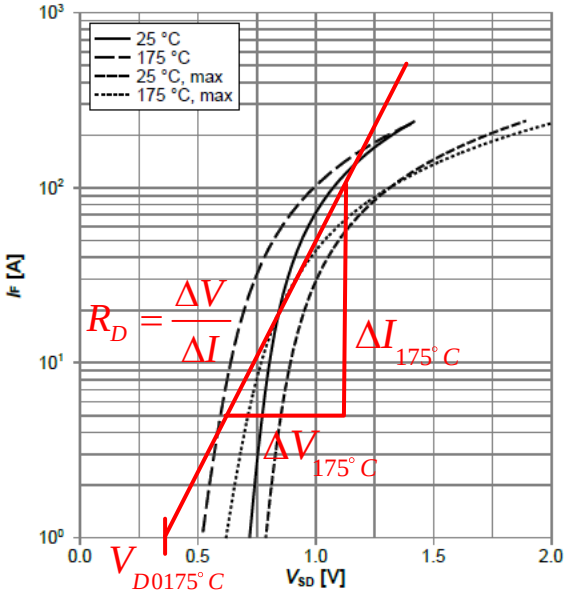


Figure 6.7: Forward characteristics of reverse diode of IPP083N10N5 [58].

6.1.4 Integrated Converter Loss Equations

6.1.4.1 Boost Converter Loss Definitions

The equations have already been defined so now all that remains is to gather the data and determine the currents, resistances, and turn-on and turn-off times. For the boost converter, no current will flow through the body diode of the MOSFET so it will be ignored. The currents flowing through the switch can be explained via (6.24) to (6.26) while the currents flowing through the top diode are described by (6.27) and (6.28).

$$I_{Mon} = I_{in} - \frac{\Delta I_{in}}{2} \tag{6.24}$$

$$I_{Moff} = I_{in} + \frac{\Delta I_{in}}{2} \tag{6.25}$$

$$I_{Mrms} = I_{in}\sqrt{D} \tag{6.26}$$

$$I_{Dav} = (1 - D)\, I_{in} \tag{6.27}$$

$$I_{Drms} = I_{in}\sqrt{(1 - D)} \tag{6.28}$$

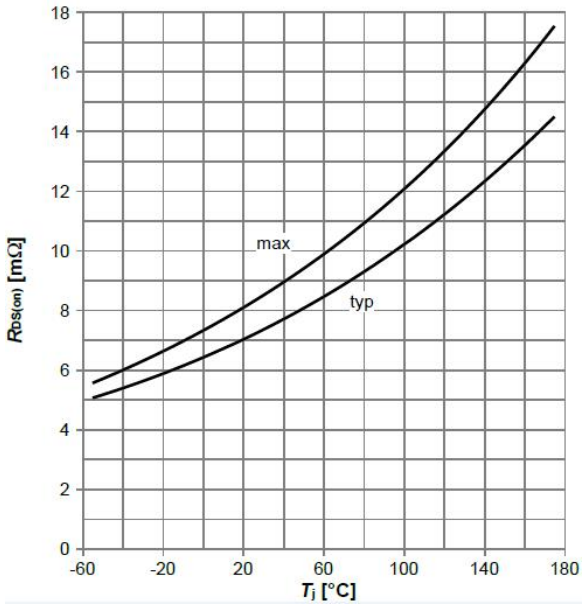


Figure 6.8: R_{ON} vs junction temperature for IPP083N10N5 [58].

Using the graph grabber tool, the on resistance data for IPP083N10N5 is gathered from Fig. 6.8 [58], the top diode forward characteristics for IDW30E65D1 are gathered from Fig. 6.9 [59], and the C_{rss} data for IPP083N10N5 is gathered from Fig.

6.10. Assuming a junction temperature of $125°C$, the on resistance is $11.5m\Omega$, the x-intercept of Fig. 6.9 was found to be 0.7856 and the on resistance of the diode is $5.4m\Omega$.

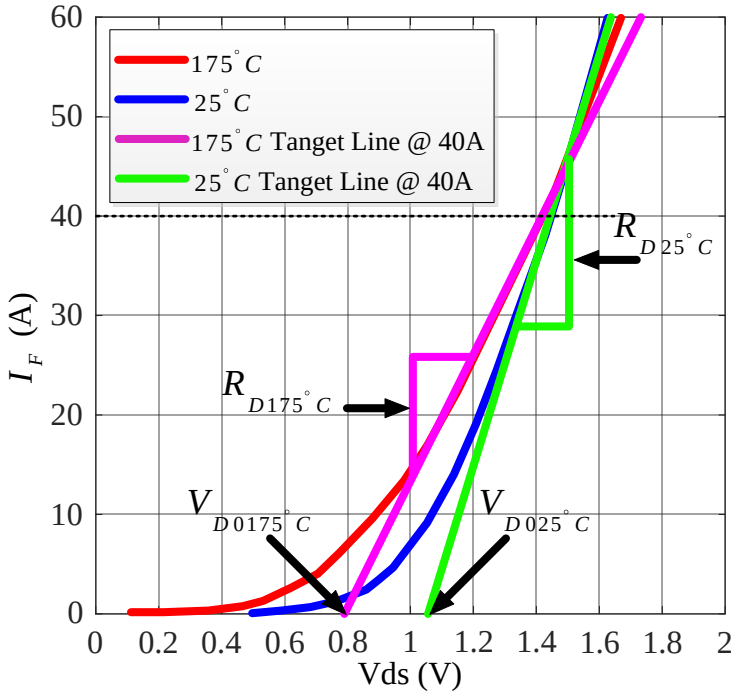


Figure 6.9: Forward characteristics of IDW30E65D1 [59].

Using the more accurate turn-on and turn-off time calculation in [95], the turn-on and turn-off times are found to be 4.9547ns and 4.3225ns respectively, when using (6.4) and (6.5). The reverse recovery charge of IPP083N10N5 is $118nC$ and so the total MOSFET loss of IPP083N10N5 can be found from (6.29). The diode switching losses are found using the reverse recovery equation in (6.20), while the conduction losses are found in (6.22) and simplified in (6.32).

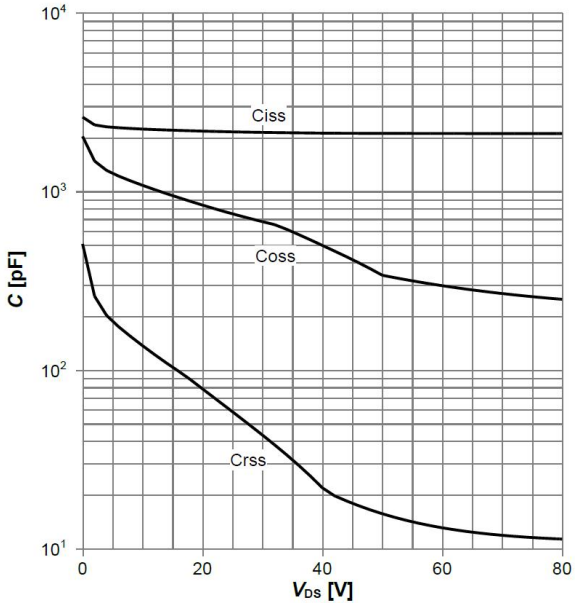


Figure 6.10: C_{rss} vs V_{DS} for IDW30E65D1 [59].

$$P_{M_{x3}} = \left(4.955 V_{DS} I_{Mon} + 118 V_{DS} + 4.322 V_{DS} I_{Moff}\right) 10^{-9} f_{sw} + 0.0115 I_{Mrms}^2 \quad (6.29)$$

$$P_{Dsw} = 0.4575 V_{DS} f_{sw} 10^{-6} \quad (6.30)$$

$$P_{Dcond} = 0.7856 I_{Fav} + 0.0054 I_{Frms}^2 \quad (6.31)$$

$$P_{D_{x3}} = 0.7856 I_{Fav} + 0.0054 I_{Frms}^2 + 0.4575 V_{DS} f_{sw} 10^{-6} \quad (6.32)$$

For the input and output capacitors MKP1848C61060JK2, the input capacitor losses for the boost will be ignored here so only the output capacitor losses will be calculated using the output rms current (6.33) which will be substituted into (6.34).

$$I_{C_O rms} = I_O \sqrt{\frac{D}{1-D}} \quad (6.33)$$

$$P_{CAP_{x5}} = 0.04 I_{rms}^2 \quad (6.34)$$

$$P_{CAP_{x5}} = 0.04\left(I_O\sqrt{\frac{D}{1-D}}\right)^2 \tag{6.35}$$

For the inductor, it was mentioned that there would be a comparison between the CoilCraft inductors AGP4233-103ME and the GA inductor using 3C97 core material with rectangular windings. The winding losses for the 3C97 inductor were defined in (4.26) to (4.28) where the DC and AC currents are found from (4.5), while the core loss equation and data for 3C97 is shown in Table 4.3. For the 3 phase boost converter inductor AGP4233-103ME, the winding loss is found using (6.36) where $R_{DC@25°C}$ is $2.95m\Omega$. While the core loss is found using (6.37), where f_{sw} is in kHz and P_{103ME} is in mW/cm^3. The core loss data for this inductor is shown in Table 6.1 and was provided by the CoilCraft engineers. For the loss calculation, the AC winding losses are combined with the core losses so they will not be calculated. During the loss calculation it is assumed the temperature is $60°C$. In chapter 7 the losses will be compared for each converter.

Table 6.1: AGP4233-103ME Core Loss Data

k1	k2	x	y	f_{sw} (kHz)
0.0862	0.0212	1	2	200
0.00108	0.0212	1	2	100
0.001133	0.0212	1	2	75
0.00119	0.0212	1	2	50
0.00124	0.0212	1	2	25
0.00127	0.0212	1	2	10

$$P_{DC} = I_{DC}^2 R_{DC@25°C}\left(1 + 0.00393\left(T_{\max} - 25°C\right)\right) \tag{6.36}$$

$$P_{103ME} = k_1 f_{sw}^{x} (k_2 \Delta i_L)^{y} \tag{6.37}$$

6.1.4.2 Buck Converter Loss Definitions

The since the buck uses the same switch and diode as the boost, it will not be discussed here again. However, the current will be different since the active switch in the boost is the lower switch while the active switch in the buck is the upper switch. Therefore, the same diode and MOSFET loss equations apply, shown in (6.29) and (6.32), but with the currents shown in (6.38) to (6.43).

$$I_{Mon} = I_O - \frac{\Delta I_O}{2} \tag{6.38}$$

$$I_{Moff} = I_O + \frac{\Delta I_O}{2} \tag{6.39}$$

$$I_{Mrms} = I_O \sqrt{D} \tag{6.40}$$

$$I_{Dav} = (1 - D)\, I_O \tag{6.41}$$

$$I_{Drms} = I_O \sqrt{1 - D} \tag{6.42}$$

Also, there is only one MOSFET and diode so the factor of three will not be applied for the buck losses. The capacitor is also the same so its equation does not need to be repeated here. The inductor is the only component that is not used from the boost. The inductor used is 1140-101K-RC and its parameters were provided in Table 4.13. After speaking with the inductor manufacturer, they provided the core loss figures showing the loss density versus flux swing. This data was curve fitted using MATLAB

curve fitting tools and is shown in Fig. 6.11 while the core loss information is shown in Table 6.2 showing the polynomial coefficients of the curve fitted equations. For the winding loss, only the DC resistance of $25m\Omega$ is provided so the rms current through the inductor will be used. Therefore, the AC losses will be ignored since the winding geometry is unknown. Therefore, the total inductor loss for 1140-101K-RC is shown in (6.44).

$$B_{1140-101\text{K}-\text{RC}} = 119\Delta i_L \tag{6.43}$$

$$P_{T,1140-101K-RC} = 0.025 I_{rms}^2 10^{-3} + 13 P_{core1140-101K-RC} \tag{6.44}$$

Table 6.2: 1140-101K-RC 77 Core Material Data

$P_{core1140-101K-RC} = aB^4 + bB^3 + cB^2 + dB + e$					
Fsw	a	b	c	d	e
10	0	2.84e-09	8.48e-06	0.0027893	0.69047
25	0	0	3.99e-05	-0.015861	0.0332
50	1.2509e-11	-4.78e-08	0.00016898	-0.087985	16.373
100	0	4.02e-08	0.00017532	-0.066774	10.75

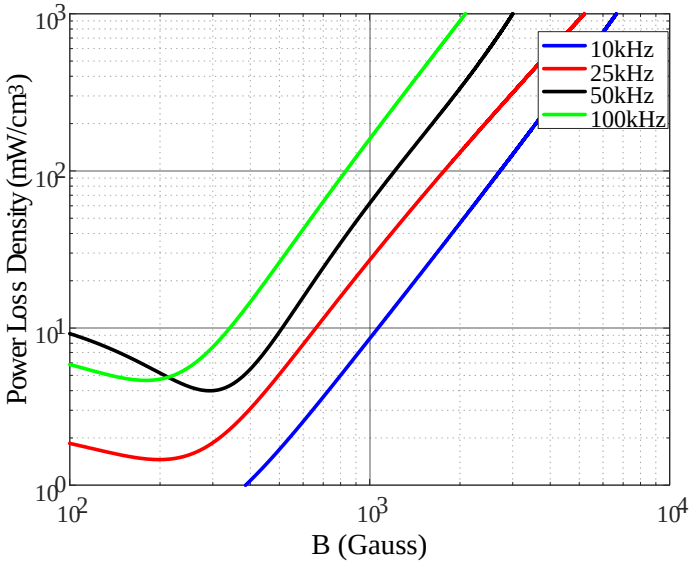


Figure 6.11: Power loss density vs flux density for 1140-101K-RC.

6.1.4.3 PSFB Converter Loss Definitions

For the PSFB converter, ZVS will be achieved so there will be no switching losses analyzed herein. However, for the conduction losses, the on-state resistance for FDP045N10A is shown in Fig. 6.12 for a junction temperature assumption of $125°C$ the on state resistance is $6.5m\Omega$ [66]. Therefore, the MOSFET conduction losses are found from (6.45). The diode used in the PSFB converter is the same as the one used within the boost and buck converters so the loss equation can be found in (6.32). For the transformer, the primary and secondary resistances can be found from Table 4.27 while the core loss information is provided in Table 6.3. The required information to calculate the winding AC losses of the transformer were not provided so only the DC primary, secondary and the core losses will be calculated. The primary resistance is $6.4m\Omega$, the secondary resistance is $2.1498m\Omega$, the frequency is 50kHz, the flux swing is $77mT$, a is 1.061, b is 2.5376, k is 3.0565 and T_{change} is 1.54735 assuming the ambient is $25°C$. Using these values the transformer loss equations are

found in (6.47), (6.48), and (6.49) respectively.

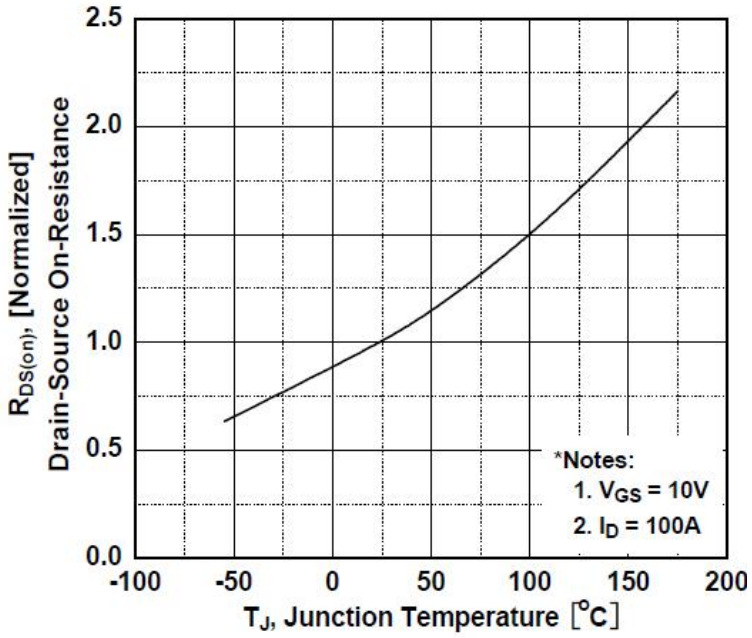


Figure 6.12: normalized $R_{DS(on)}$ vs junction temperature for FDP045N10A [66].

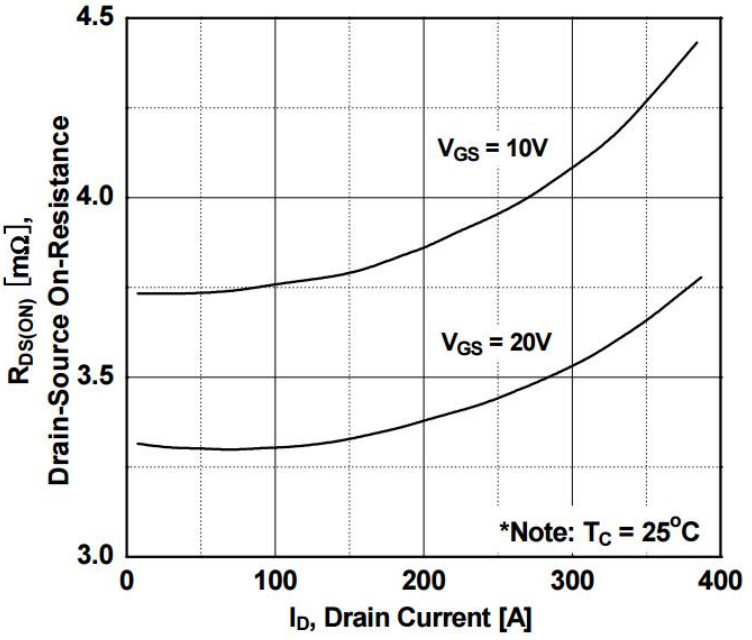


Figure 6.13: $R_{DS(on)}$ vs I_D for FDP045N10AF102 [66].

Table 6.3: T1000DC-1-8 Core Loss Parameters

f_{sw}(kHz)	a	b	k	T1	T2	T3	T4
25 to 100	1.061	2.5376	3.06E-06	2.5376	0.03468	-1.97E-04	0
>100	2.419	2.68	2.28E-09	2.277	0.00354	-0.0003025	2.14E-06

$$P_{Mcond} = 0.0065 I_{M,rms}^2 \tag{6.45}$$

$$T_{change} = T_1 - T_2 T_a + T_3 T_a^2 + T_4 T_a^3 \tag{6.46}$$

$$P_{core} = k f_{sw}^a B_{AC}^b T_{change} = 4.729(100)^{1.061}(77)^{2.5376} \tag{6.47}$$

$$P_{pri} = 0.0064 I_{pri,rms}^2 \tag{6.48}$$

$$P_{\text{sec}} = 0.0021498 I_{\text{sec},rms}^2 \tag{6.49}$$

$$P_{Trans} = P_{pri} + P_{\text{sec}} + P_{core} \tag{6.50}$$

The output inductor is 1140-151K-RC, which has a DC resistance of $40m\Omega$. The core loss data is shown in Table 6.4 and the core loss equation in (6.51) while the total inductor loss is shown in (6.52).

Table 6.4: 1140-151K-RC Core Loss Parameters

f_{sw}(kHz)	x_4	x_3	x_2	x_1	x_0
10	0	2.18e-09	8.48e-06	-0.0027893	0.69047
25	0	0	3.99e-05	-0.015861	3.0332
50	1.254e-11	-4.784e-08	1.69e-04	-0.088	16.4
100	0	4.024e-08	1.754e-04	-0.066774	10.75

$$P_{1140-151K-RC} = V_{core}\left(x_4B^4 + x_3B^3 + x_2B^2 + x_1B + x_0\right) \tag{6.51}$$

$$P_{1140-151\mathrm{K-RC}} = 0.04I_{Lo,rms}^2 + 13P_{core1140-151K-RC} \tag{6.52}$$

6.1.4.4 Inverter Loss Definitions

The inverter uses four STP28N65M2 switches which have an on-state resistance of $55.4m\Omega$ if the junction temperature is $100°C$ while the body diode forward characteristics are shown in Fig. 6.14 [77]. The MOSFET rms current has been explained in [94,96] and is shown in (6.54), while the conduction loss is shown in (6.55), where ϕ is the angle between the output voltage and current, and m_a is the modulation index in (6.53). For the core loss, the ripple rms current can be used if the core information is provided. For the switching loss, the same equations will be used from boost and buck converter, (6.1)-(6.5), with the only difference being the current definition shown in (6.56) [94]. Combining the calculated turn-on and turn-off times of 8.5321ns and 7.166ns respectively, the switching loss can be explained in (6.1) using the datasheet reverse recovery charge value of $8.2\mu C$.

$$m_a = \frac{\sqrt{2}V_{AC,rms}}{V_{HVDC}} \tag{6.53}$$

$$I_{Mrms} = \sqrt{I_O^2\left(\frac{1}{8} + \frac{m_a\cos\phi}{3\pi}\right)} \tag{6.54}$$

$$P_{Mcond} = 0.0554I_O^2\left(\frac{1}{8} + \frac{m_a\cos\phi}{3\pi}\right) \tag{6.55}$$

$$I_{DC} = \frac{I_O}{\pi} \tag{6.56}$$

$$P_{swM} = \left(8.532 V_{DS} I_O 10^{-9} + 8.2 V_{DS} 10^{-6} + 7.166 V_{DS} I_O 10^{-9}\right) f_{sw} \tag{6.57}$$

For the MOSFET body diode, the conduction losses are estimated using (6.58) where the on voltage and resistance are 0.7031 and 0.0129 respectively, using the same technique discussed previously in the other chapters [94].

$$P_{Dcond} = V_O I_O \left(\frac{1}{2\pi} + \frac{m_a \cos\phi}{8}\right) + R_D I_O^2 \left(\frac{1}{8} - \frac{m_a \cos\phi}{3\pi}\right) \tag{6.58}$$

$$P_{Dcond} = 0.7031 I_O \left(\frac{1}{2\pi} + \frac{m_a \cos\phi}{8}\right) + 0.0129 I_O^2 \left(\frac{1}{8} - \frac{m_a \cos\phi}{3\pi}\right) \tag{6.59}$$

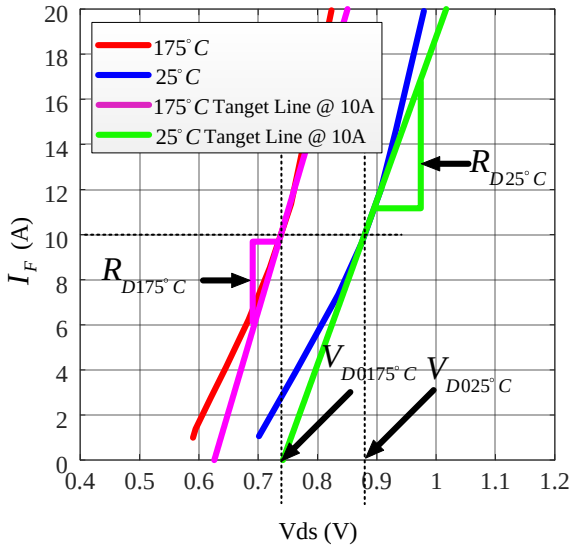


Figure 6.14: Forward characteristics of STP28N65M2 body diode [77].

The rms ripple current, the rms current and the peak current through the filter inductor are provided in (4.82), (4.83), (4.84) respectively. The rms current is used

to find the conduction losses in of the filter inductor while the ripple rms current is used to find the core losses. For the winding loss, the manufacturer did not provide any information other than DC resistance. However, this inductor has an open winding so the number of turns and the number of layers can all be found manually. The F_R ratio, as described in section 4.1.3.2, can be calculated for circular magnet wire where A_{str} is found in [47], as shown in (6.60). For an inductor with one layer and a A_{str} value of 3.8036, the F_R ratio is 3.8082 which gives an AC resistance of $57.1m\Omega$ for a DC resistance of $15m\Omega$. Using these resistance values, the winding losses can be found from the AC and DC losses in (6.61) and (6.62) respectively. The core loss was not provided so only the winding loss will be used.

$$A_{str} = \left(\frac{\pi}{4}\right)^{0.75} \frac{d\sqrt{p}}{\delta} \tag{6.60}$$

$$P_{AC,Lf} = \left(\frac{\Delta I_{Lf}}{\sqrt{3}}\right)^2 R_{AC} = 0.0571\left(\frac{\Delta I_{Lf}}{\sqrt{3}}\right)^2 \tag{6.61}$$

$$P_{Lf,DC} = I_O^2 R_{DC} = 0.015 I_O^2 \tag{6.62}$$

$$P_{winding} = P_{AC} + P_{DC} \tag{6.63}$$

The HVDC link capacitor has a total of eight capacitors, two in series and four in parallel. Looking at its datasheet, the tangent loss angle at 350 volts is 0.15, which will give an ESR value of 0.0207 when using (6.64), if the AC ripple is at 100Hz.

$$ESR = 2\pi f_{grid} C_{HVDC} \tan\delta \tag{6.64}$$

In reality the amount of loss generated by this capacitor will be quite small in comparison to the rest of the switches and inductors so it can be ignored. For example, if the capacitor dissipates 0.5W, the required current flowing through it would need to be 4.9A when using the traditional I squared R formula. This is already close to the current on the secondary so it is safe to assume the current will be smaller making the losses less than 0.5W. The output filter capacitor will also generate a small amount of loss so it can be ignored herein.

6.2 System Level Simulation and Converter Loss Estimation

In this section the converter losses are modeled and run with the MATLAB/Simulink models to be compared with the experimental tests to see how accurate the models are. System level simulations will also take place showing the controller operating correctly during input and output changes.

6.2.1 Simulated Control of System

MATLAB/SIMULINK is a great tool for circuit simulation and control since SIMULINK provides circuit modeling tools, such as SimPowerSystems, which can be used to create complex models in both discrete and continuous time. The circuit can then be combined with the control methods to model actual converter operation and its transient response to specific changes in the system. The control program can easily be exported to a DSP which will control the actual circuit using the same control which was modeled in Simulink.

For the simulation the time step must be small enough to capture the switching transients. As such, the step time is in the range of 10ns to have enough resolution to monitor the waveforms. Unfortunately, this prevents longer simulation times because the program will crash if too much data is being processed. One method is to create the average model of the system so that the simulation step size can be reduced. However, this requires analysis of the entire system and is beyond this work. Fortunately, the system can respond to the parameter changes assigned so that both the system response and the system switching transients can both be seen.

Each control method mentioned in Chapter 5 is developed in MATLAB/Simulink and run within the entire system to see how the system responds to applied changes. The controlled parameters of the system are shown in Fig. 6.15. As the converter runs these parameters will change to see how the system responds. The full converter is simulated and the results are shown in Fig. 6.16 to Fig. 6.21. For these results, the LV and HV DC buses were fixed at 55V and 350V respectively. For most converters there will be a set DC voltage but if required, these buses can be changed within their voltage range. For this simulation there are a few locations in which the voltage and power settings are changed for the input and output loads. This was done to show that the converter can maintain correct control when step changes are applied to the system.

The figures on the left hand side show the entire converter simulation over 3 seconds while figures on the right shown the converter operating over a much smaller time range. This was done to show the controllability and stability of the system subject to the applied changes, while also showing the switching waveforms at steady state. From the simulations the system is able to control the LV, HV and output AC

voltages at 55V, 350V and 230V respectively over the entire operating time, subject to the DC Load voltage, output AC load power, input DC source voltage, and output buck power changes in Fig. 6.15. The boost, buck, PSFB, and inverter waveforms are shown over the total operating range in Fig. 6.16, Fig. 6.17, Fig. 6.18 and Fig. 6.19 respectively. For each of these figures the left hand column has the full simulated range while the right hand column has a snap shot showing the switching waveforms. For the boost converter it is clear that the converter is able to maintain equal current sharing as shown in Fig. 6.16c, and also maintain the desired output voltage of 55 volts subject to the applied changes. The buck, PSFB and inverter also maintain the correct operation subject to the applied changed. The current through the bottom switches of the lagging and leading legs of the PSFB converter are shown in Fig. 6.18e and Fig. 6.18g respectively. The short negative current for these waveforms indicates ZVS and it is also clear that the amount of time the current is negative is different for each switch in each leg. The difference in ZVS capabilities is clearly seen since a longer negative period means easier ZVS. This is why the negative period is longer for the leading leg since it is easier to achieve ZVS as discussed before. One issue that may arise is the voltage overshoot across the rectifier diodes in Fig. 6.18j. The steady state value is 350V while the peak is roughly 600V higher which can be an issue if left unattended.

For the inverter all the waveforms look correct and the AC load voltage is able to maintain the desired output voltage of 230V rms shown in Fig. 6.19. However, the voltage ripple on the HVDC is larger than the 5 percent requirement. In this case the voltage ripple is slightly larger than 20V which is 5.7 percent HVDC (350V). Fig. 6.20 shows the input and output powers of the simulated converter while Fig.6.21

shows the system level modeling comparison between HVDC link capacitor values. Blue shows the converter system for a HVDC link capacitor of $440\mu F$ while red is for $1.44mF$.

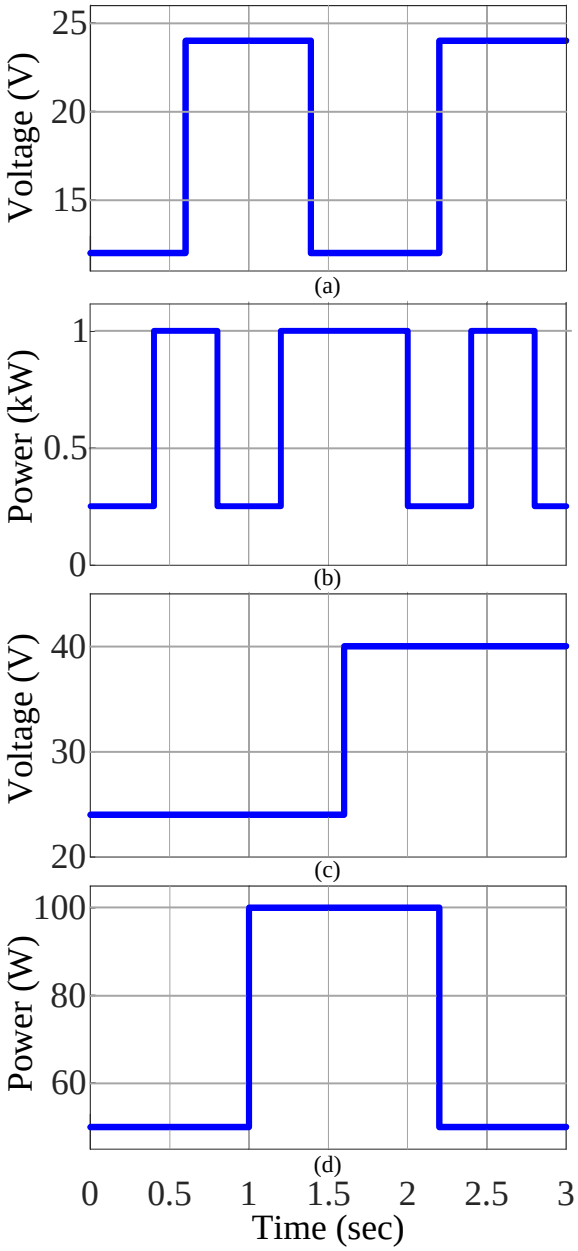


Figure 6.15: System simulation control variables (a) buck output voltage (b) output AC power (c) input boost voltage (d) output buck power.

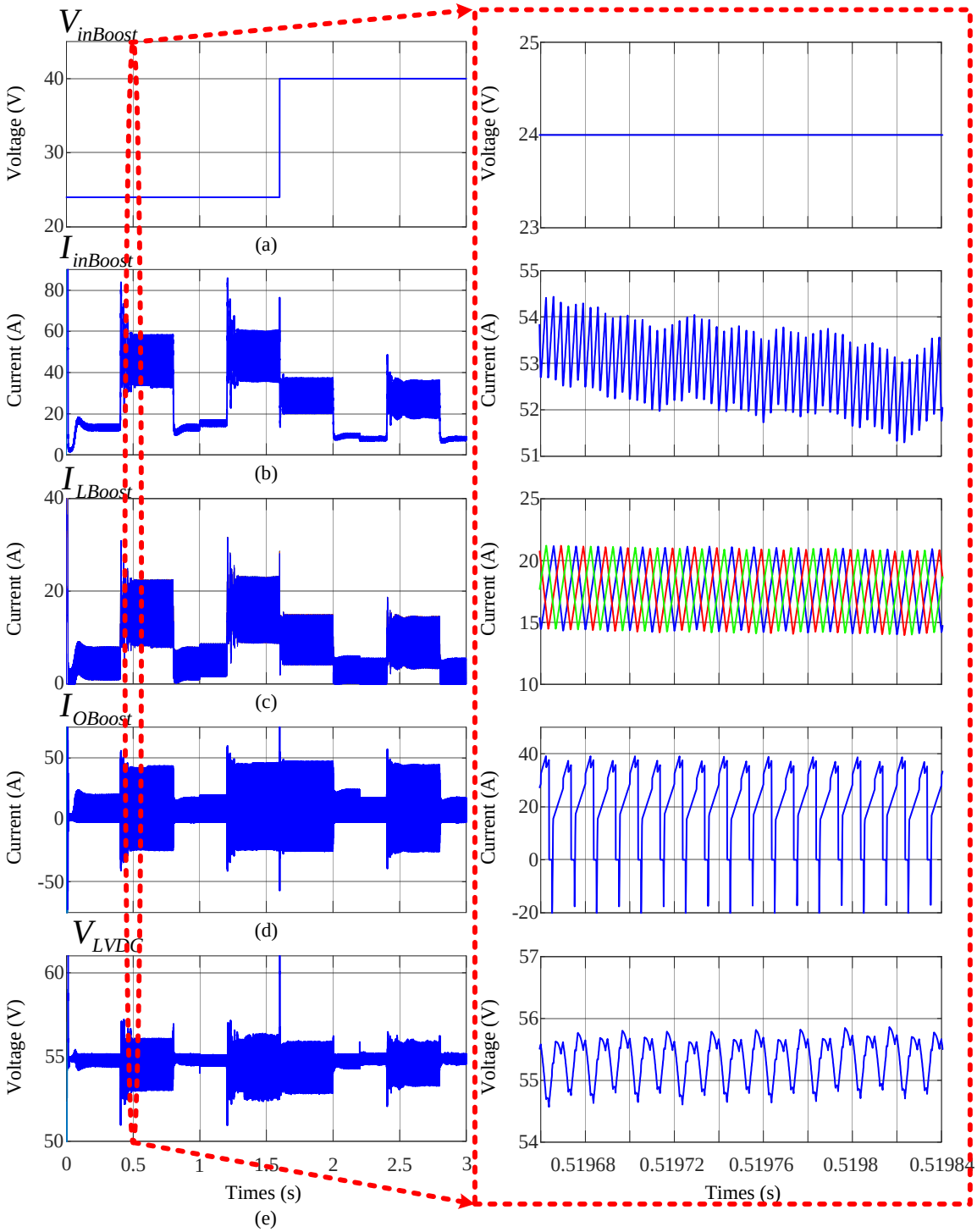


Figure 6.16: Boost converter simulation waveforms (a) input voltage (b) input current (d) output current (e) LVDC link voltage.

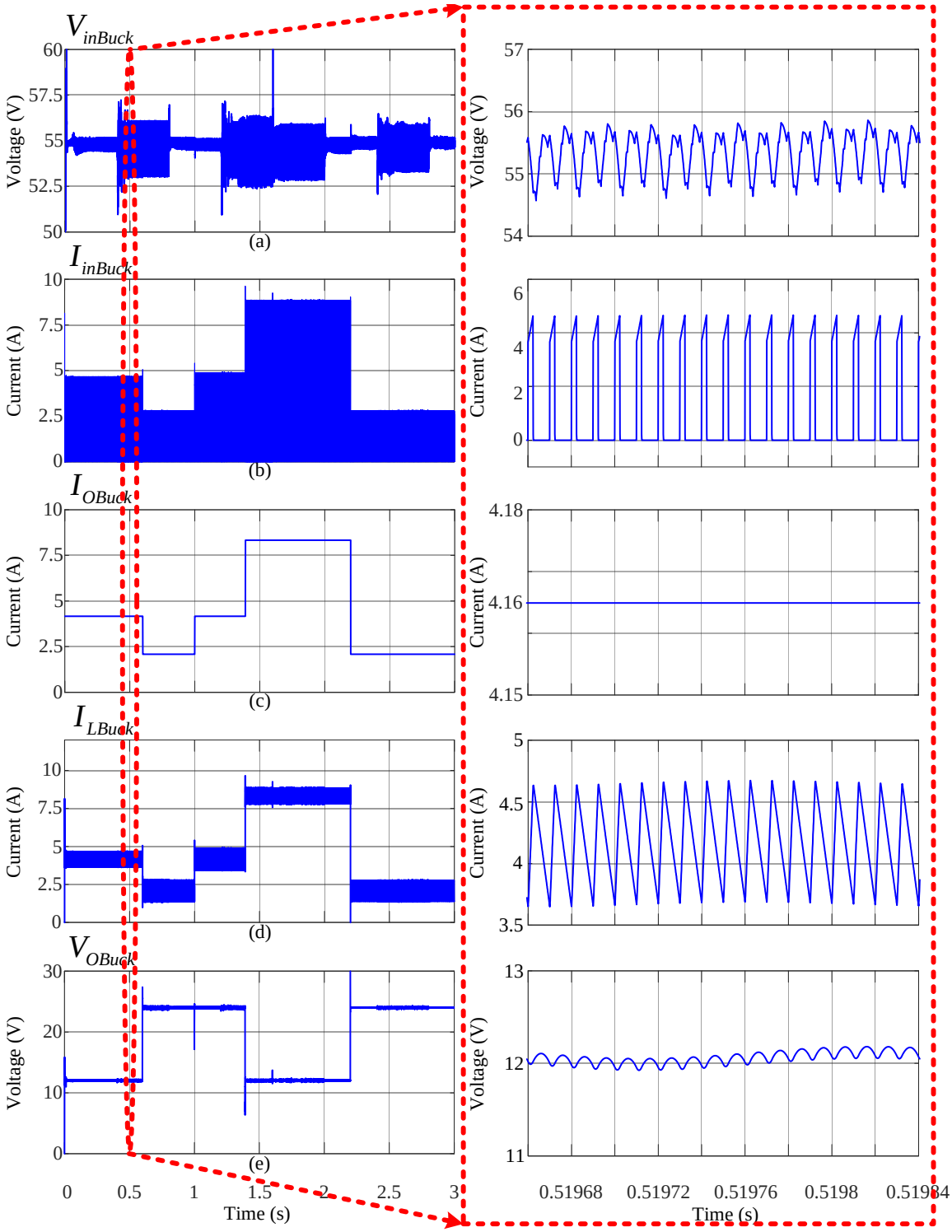


Figure 6.17: Buck converter simulation waveforms (a) input voltage (b) input current (c) output current (d) inductor current (e) LVDC link voltage.

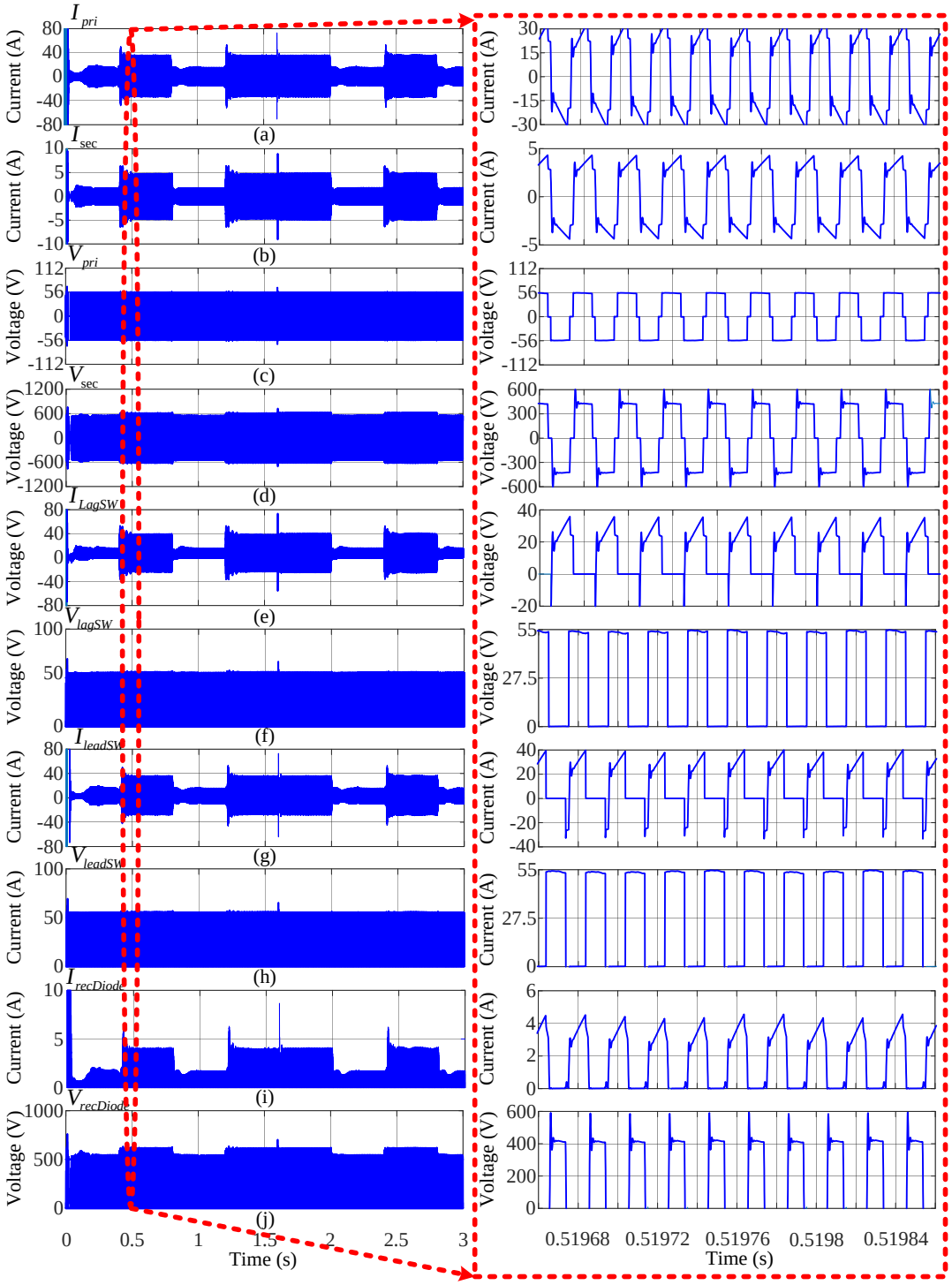


Figure 6.18: PSFB converter simulation waveforms (a) primary current (b) secondary current (c) primary voltage (d) secondary voltage (e) lagging MOSFET current (f) lagging MOSFET voltage (g) leading MOSFET current (h) leading MOSFET voltage (i) secondary diode current (j) secondary diode voltage.

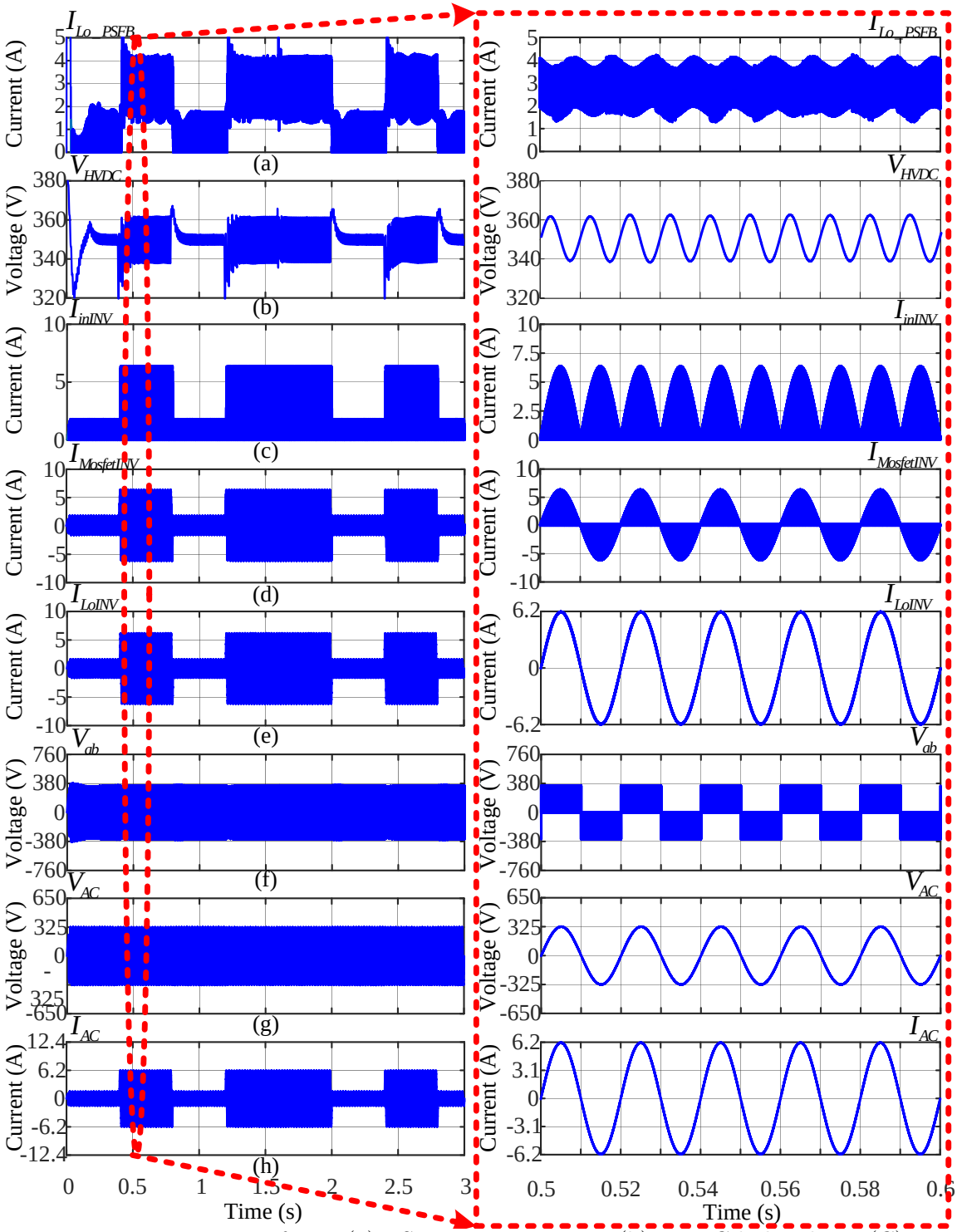


Figure 6.19: Inverter waveforms (a) PSFB output current (b) HVDC link voltage (C) INV input current (d) INV MOSFET current (e) filter inductor current (f) unfiltered voltage Vab (g) AC voltage (h) AC current.

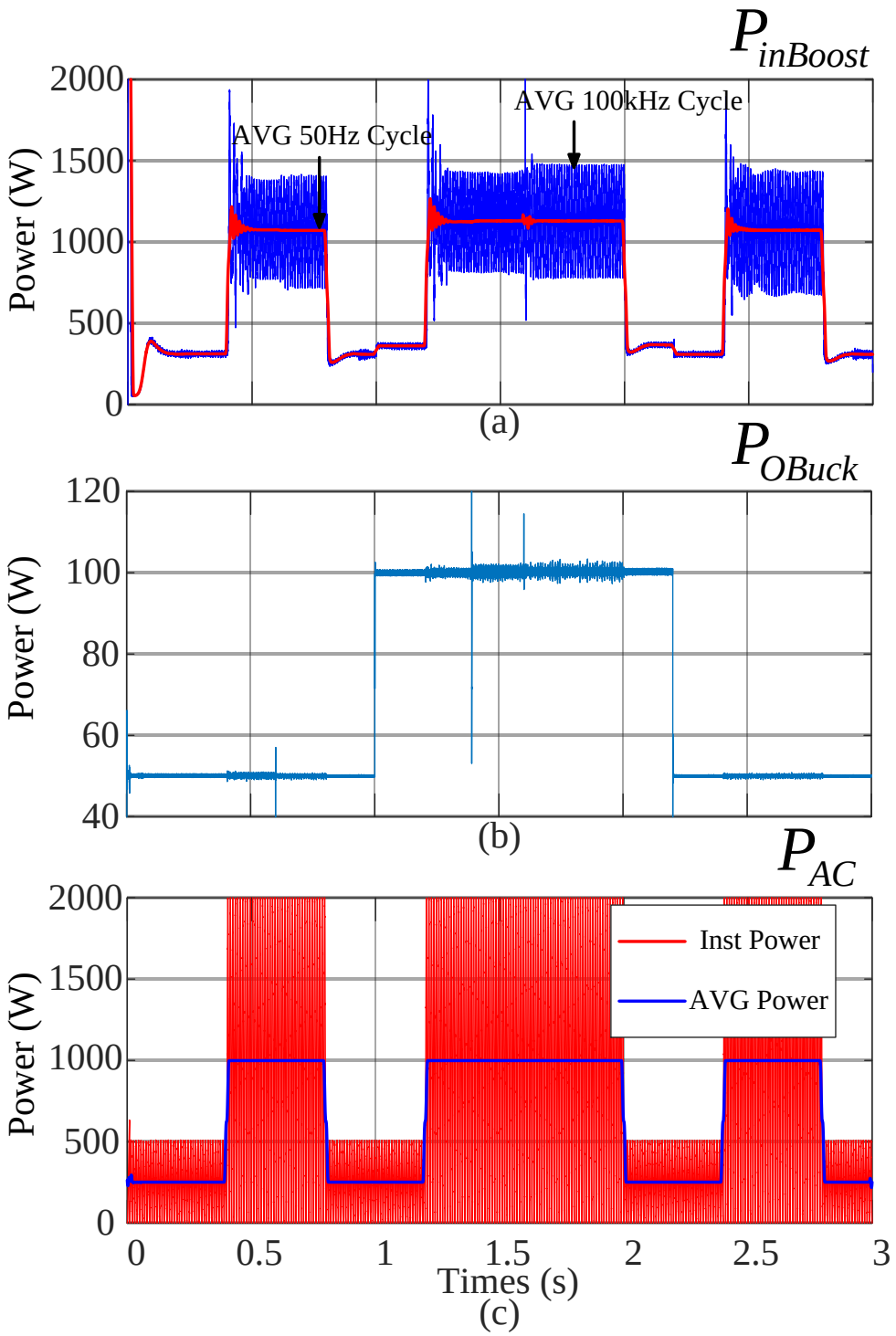


Figure 6.20: Input and output power for source and loads within integrated system (a) input boost power (b) buck output power (c) inverter output AC power).

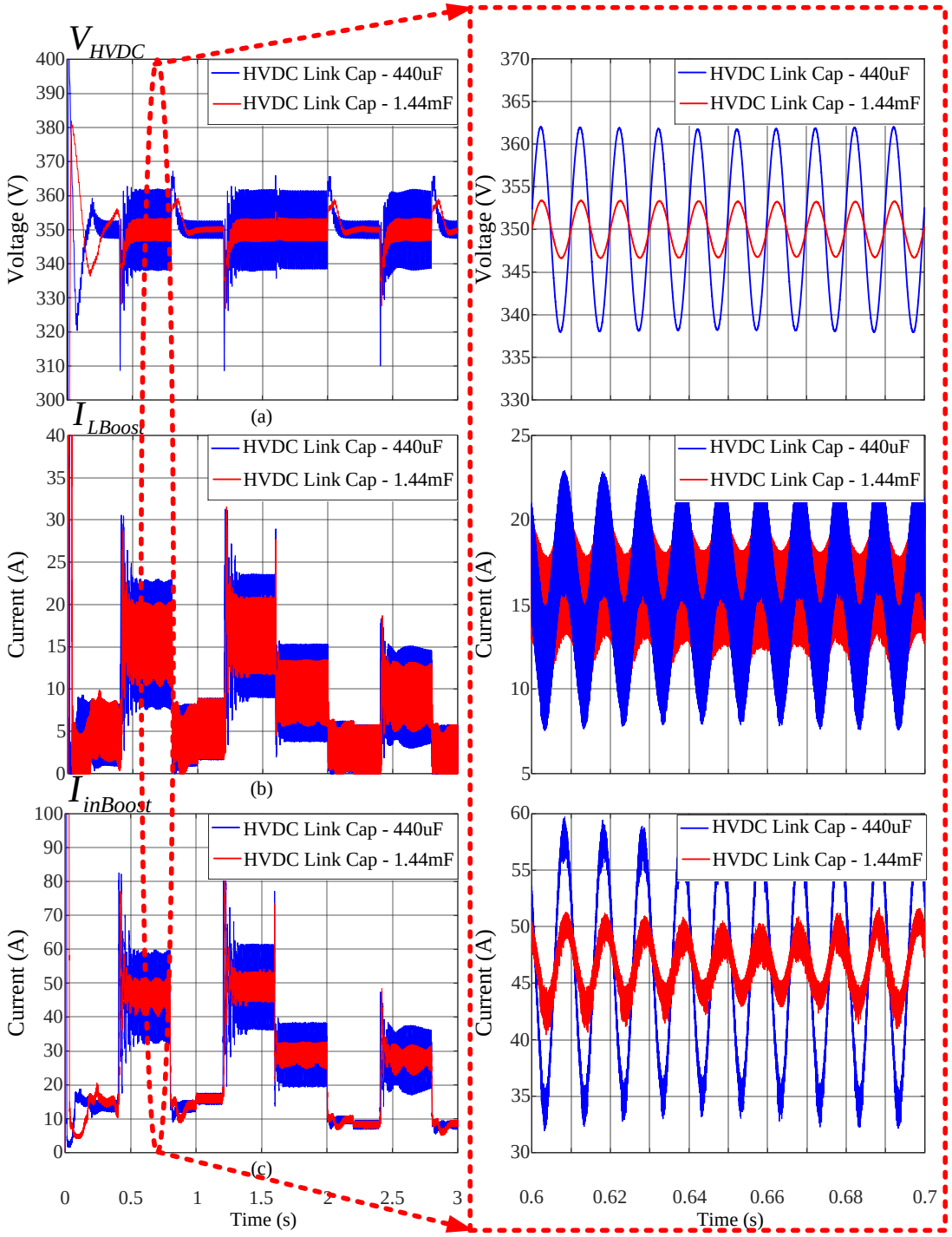


Figure 6.21: System level modeling comparison between different HVDC link capacitor values (a) HVDC bus voltage (b) boost converter phase current (c) boost converter input current.

Smaller capacitor values result in larger fluctuations for the input voltages and currents due to the AC back propagation. The ripple current is quite large and if a battery is used this ripple is definitely too high and will possibly damage the battery. The easiest method to mitigate these issues is to add extra HVDC link capacitors to remove the ripple. There are other more complex methods however they are beyond the scope of this work. The simulation was run again but this time the HVDC link capacitor was increased by $1mF$ up to a total of 1.44 mF. Clearly the ripple comes down quite a bit with the HVDC voltage ripple ranging from approximately 352V to 347V giving a ripple of 5V (1.4 percent). Even with a low ripple value on the HVDC link, the input currents are still quite large so in the future another method to improve the current harmonics should be applied. Also, the harmonic content must be within the limits shown in Fig. 4.30 over the entire operating range. From the full simulation of 0 to 3 seconds Fig. 6.23 and Fig. 6.24 show the single phase inverter TDH calculation for the non-filtered and filtered output AC voltage. The output voltage before the LC filter is shown in Fig. 6.23 and clearly the harmonic content is very high (60 percent). However, after the LC filter, the harmonic content decreases to around 0.31 percent which is much lower than the required 5 percent as indicated in Fig. 6.24. Clearly the LC filter is able to filter out the high frequency harmonics over the entire load range subject to the applied changes.

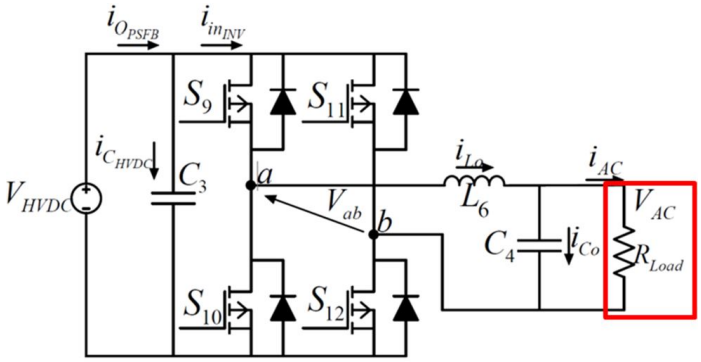


Figure 6.22: Single phase inverter output voltage THD.

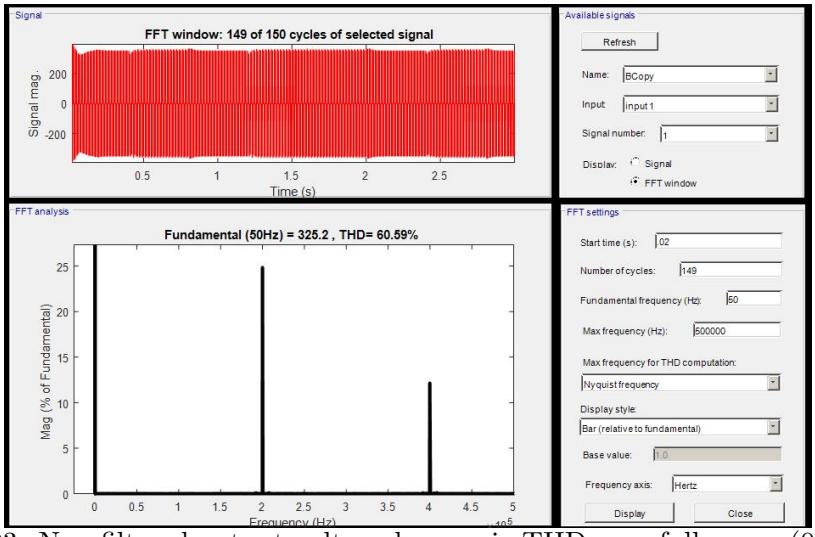


Figure 6.23: Non-filtered output voltage harmonic THD over full range (0 to 3 sec).

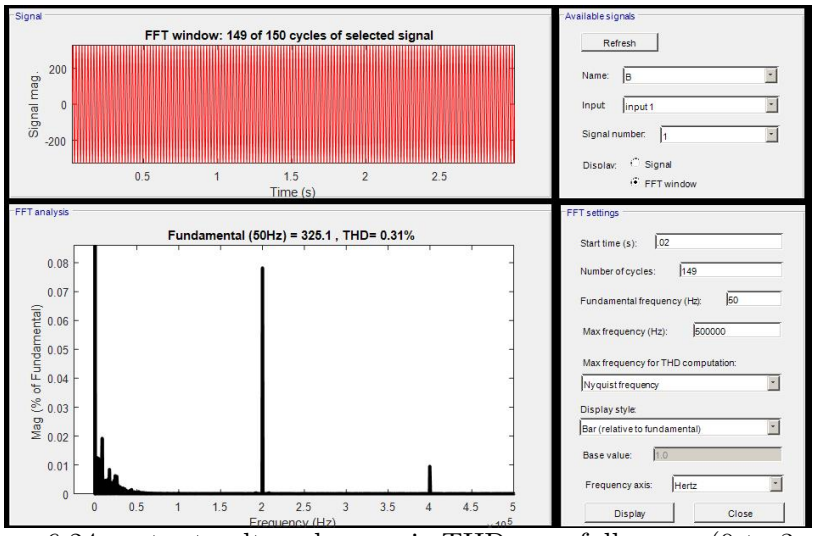


Figure 6.24: output voltage harmonic THD over full range (0 to 3 sec).

6.2.2 Boost Converter Efficiency Simulation

The simulated boost converter efficiency for different loading conditions from zero to full load at different input boost voltages are shown in Fig. 6.25 while Fig. 6.26 shows the range from 0 to 300W. There are small differences in efficiency for LVDC link voltages of 48V, 54V, and 60V but 60V has the highest efficiency over the entire range followed by 54V and then 48V. The difference between the input voltages 24V and 40V are quite similar as well with 40V being slightly higher than 24V. On average the efficiencies are greater than 96 percent for a majority of the load range.

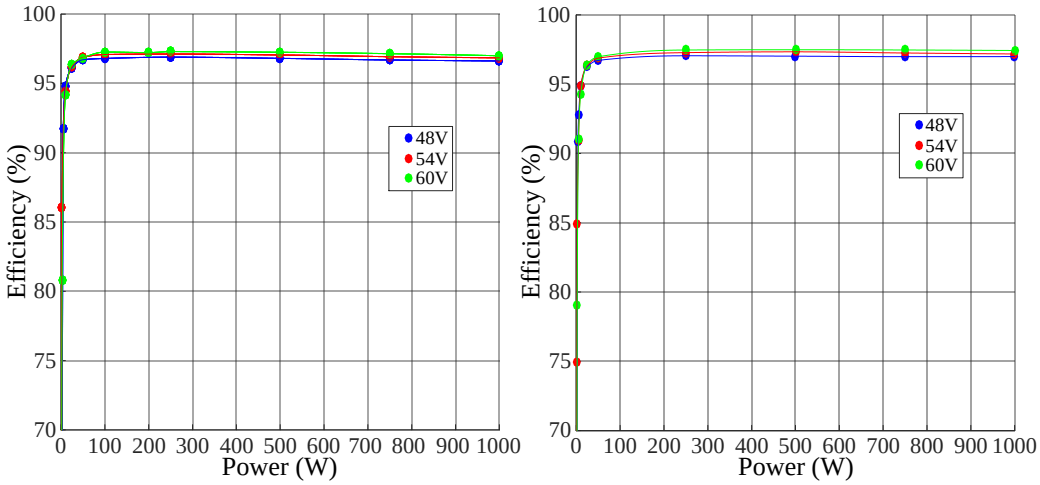


Figure 6.25: Boost converter efficiency map over full range for 24V input and 40V input.

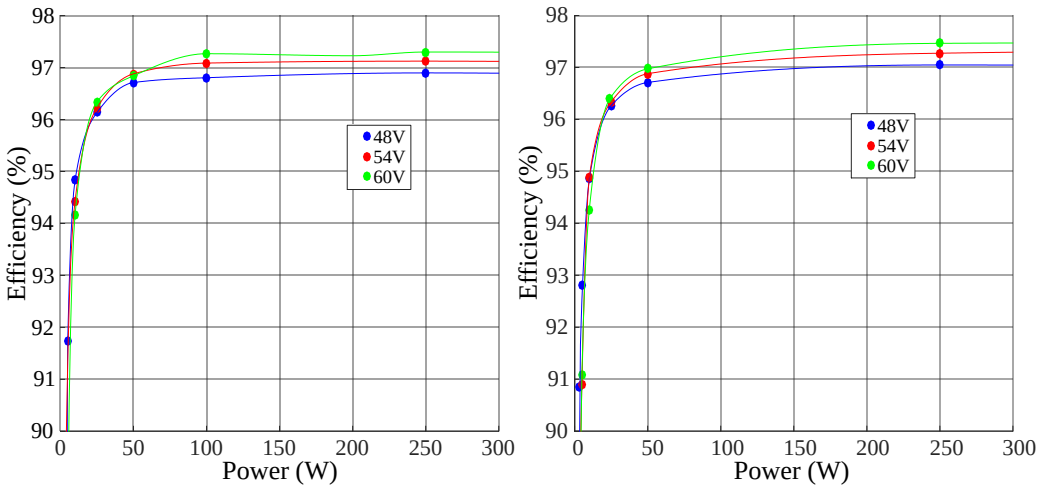


Figure 6.26: Boost converter efficiency map over 0 to 300W range for 24V and 40V input.

6.2.3 Buck Converter Efficiency Simulation

The simulated buck converter efficiency for different loading conditions from zero to 100W at different input buck voltages are shown in Fig. 6.27. For output voltages 12V and 24V there is a difference of around 4 percent with 12V achieving approximately 94 percent while 24V achieves 98 percent. The efficiency difference between the input voltages of 48V, 54V, and 60V is very similar; within 0.5 percent. The converter has the highest efficiency at 48V input followed by 54V and then 60V for both 12V and 24V output conditions. There is a larger difference between the 12V output and the 24V output as can be seen but the trend is the same.

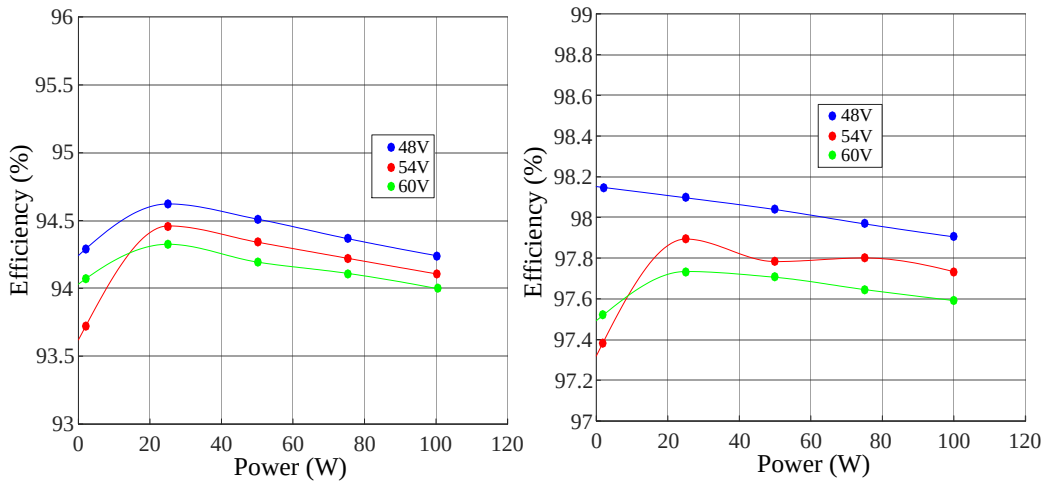


Figure 6.27: Buck converter efficiency versus load power over wide load range for different output voltage (a) 12V input (b) 24V input.

6.2.4 PSFB Efficiency Simulation

The simulated PSFB converter efficiency for different loading conditions from zero to 1200W is shown in Fig. 6.28a, while a load range of 0 to 400W is shown in Fig. 6.28b for a fixed HVDC link voltage of 350 volts. The difference in efficiency for input voltages 48V, 54V, and 60V are fairly close over the entire load range. However, at lower powers the difference increases between them. 48V has the highest efficiency followed by 54V and then 60V over the entire operating range.

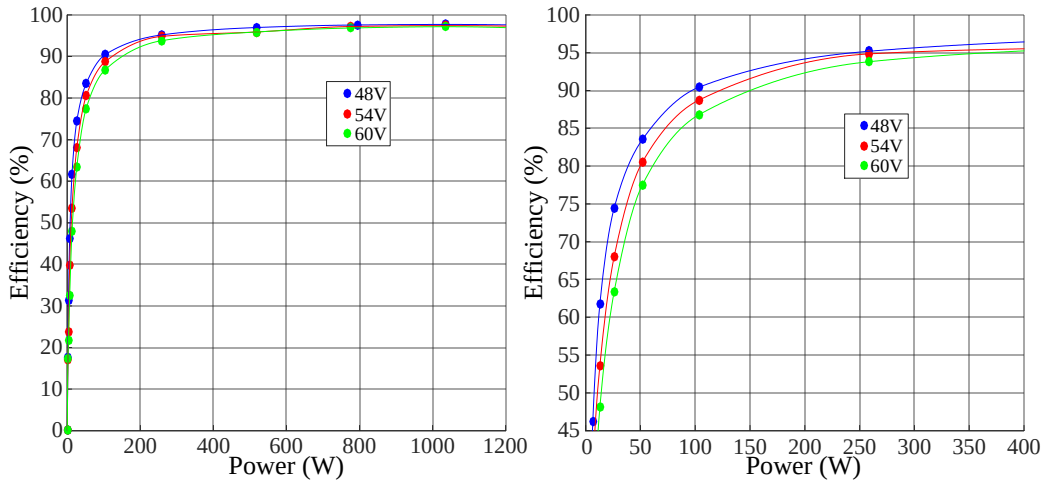


Figure 6.28: PSFB converter efficiency versus load power for different input voltages (a) complete load range (b) load range from 0 to 400W.

6.2.5 Inverter Efficiency Simulation

The simulated efficiency versus varying load power for the inverter is shown in Fig. 6.29 for a fixed input voltage of 350V and an output voltage of 230V rms. The efficiency is very constant over the entire operating range at around 98 percent which is a bit questionable since the efficiency usually goes down as the power decreases but the opposite is true in this case.

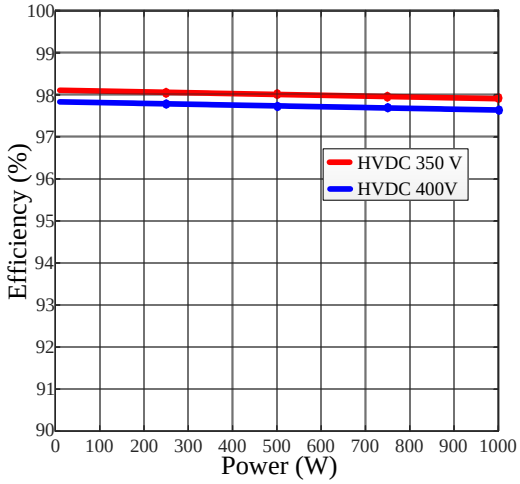


Figure 6.29: Simulated inverter efficiency map for 350V and 400V HVDC input voltage.

This chapter discussed the integrated converter system modeling, simulation, analysis and efficiency assessment. First, the losses for each component within the integrated system were defined so that the converter losses could be found. Next, the integrated converter was run at the defined operating conditions over a total time range of 3 seconds. Different voltages and powers were changed for the input source, DC load and AC load to see how the system responded and operated. The system was able to maintain stable operation and achieve the desired voltage and power levels defined over the total operating range. However, there were large current ripples due to the AC propagation of the AC load. Another simulation was run after adding extra HVDC link capacitance to help reduce the ripple. It was able to reduce the ripple but not completely. The inverter THD was also found over the entire operating range and was always less than the defined standards for off-grid distributed energy connections, indicating the designed LC filter on the inverter works as intended. Finally, the efficiency mapping for each converter within the integrated system was shown from no load to full load. All the converters were able to achieve high efficiency over a majority of the load range.

Chapter 7

Experimental Results and Simulation Comparison

In this section, the converters will be run at their full load conditions individually as separate converters to verify their correct operation. The converter models in MATLAB/Simulink will be run at the same operating conditions simulated at the same experimental testing conditions to see how accurate they match followed by a discussion on improvements to each.

7.1 Boost Converter Experimental Results

Fig. 7.1 to Fig. 7.6 shows the boost converter operating at full load under closed loop control for different combinations of input and output voltages. Full load operation is only shown to indicate that the converter is able to operate at the maximum requirement. If full load is achieved then lower loads should also work as well. The experimental test conditions and the results are tabulated in Table 7.1 along with the

respective efficiencies. For each screen shot yellow is the output voltage, green is the input voltage and red is the input current and blue is the output current. Only the steady state waveforms are shown however, these tests were done under closed loop control implementing the average mode current control technique. Fig. 7.1 and Fig. 7.2 are for 50V output, Fig. 7.4 and Fig. 7.5 are for 55V output, and Fig. 7.5 and Fig. 7.6 is for 60V output. One thing to note about the efficiency calculation is that it was done using the scope data shown in each screenshot and some of the plots have a bit of noise shown which can influence the measurement.

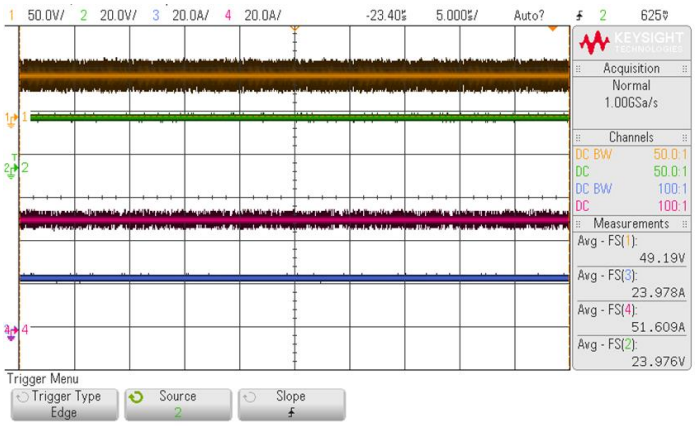


Figure 7.1: Boost converter testing 50V out 24V in, Pin 1237.4W, Pout 1179.5W, eff 95.3 percent.

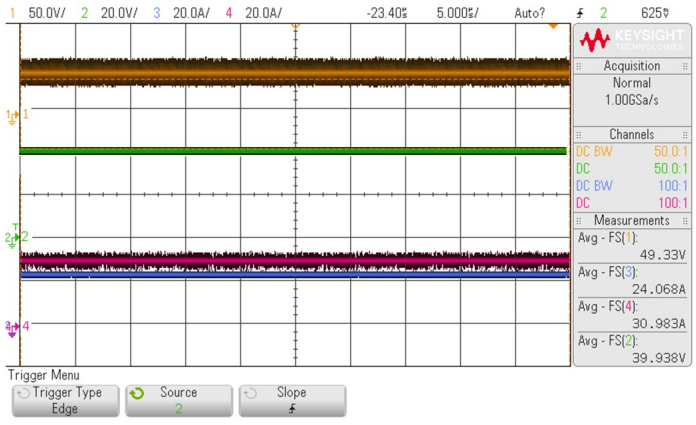


Figure 7.2: Boost converter testing 50V out 40V in Pin 1237.4W, Pout 1187.3W, eff 95.95 percent.

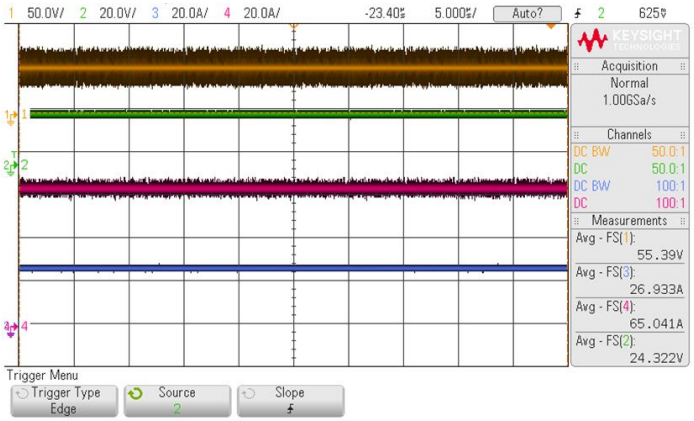


Figure 7.3: Boost converter testing 55V out 24V in Pin 1581.9W, Pout 1491.8W, eff 94 percent.

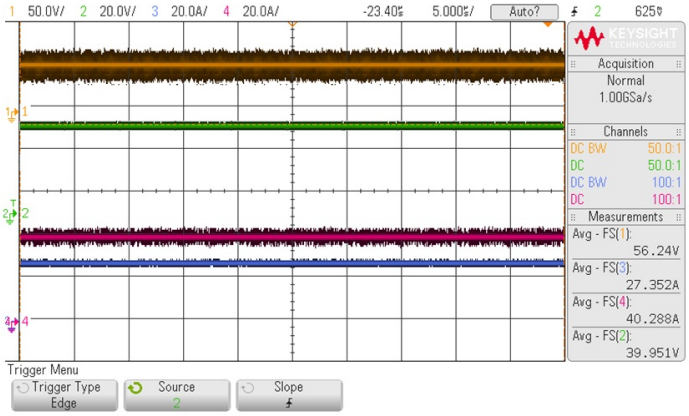


Figure 7.4: Boost converter testing 55V out 40V in Pin 1609.55W, Pout 1538.3W, eff 95.57 percent.

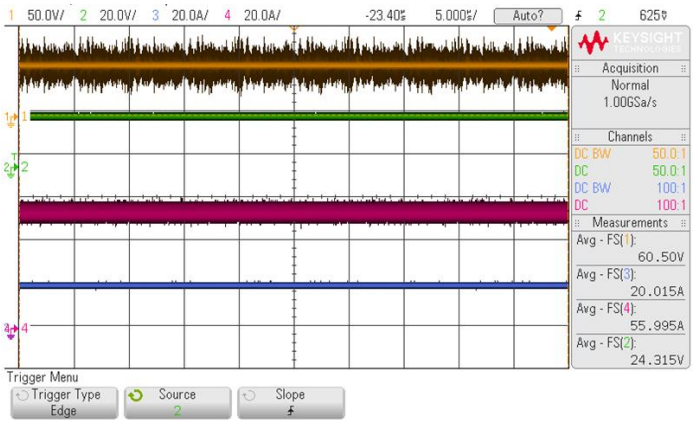


Figure 7.5: Boost converter testing 60V out 24V in Pin 1361.5W, Pout 1210.9W, eff 88.97 percent.

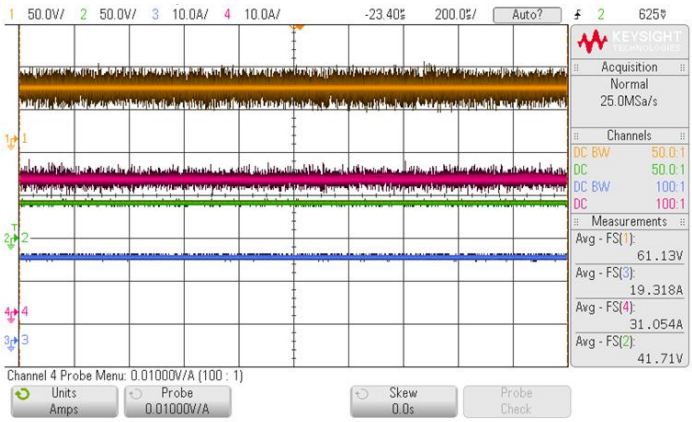


Figure 7.6: Boost converter testing 60V out 40V in Pin 1295.3W Pout 1180.91W eff 91.17 percent.

Table 7.1: Experimental Boost Converter Results

Vo (V)	Iout (A)	Pout (W)	Vin (V)	Iin (A)	Pin (W)	Eff (%)
49.19	23.978	1179.478	23.976	51.609	1237.377	95.32
49.33	24.068	1187.274	39.938	30.983	1237.399	95.95
55.39	26.933	1491.819	24.322	65.041	1581.927	94.30
56.24	27.352	1538.276	39.951	40.288	1609.546	95.57
60.5	20.015	1210.908	24.315	55.995	1361.518	88.94
61.13	19.318	1180.909	41.71	31.05	1295.096	91.183

Each voltage reference is achieved using the closed loop control at the full load conditions indicating that the designed boost converter is able to both maintain correct operation and achieve the desired power level. Here the highest efficiency is for the smallest output voltage of approximately 49V, followed by 55V and then 60V. The different between input voltages 24V and 40V is no more than 3 percent for each.

Table 7.2: Boost Converter Inductor Comparison

3 Phase System with 3C97							
Test Condition	P_{Ltotal} (W)	P_{MCond} (W)	P_{Msw} (W)	P_{DCond} (W)	P_{Dsw} (W)	P_{Cap} (W)	P_{total} (W)
1	3.34	5.25	2.853	26.7	<0.07	0.11	38.253
2	1.27	0.735	2.43	24.6	<0.08	0.04	29.075
3	4.86	8.91	3.4965	31.5	<0.09	0.14	48.9065
4	2.36	1.83	2.9745	28.8	<0.10	0.02	35.9845
5	3.78	6.24	3.5055	22.35	<0.11	0.078	35.9535
6	1.97	1.08	2.958	19.65	<0.12	0.008	25.666
Single Phase System with 3C97							
1	7.43	15.9	1.691	37.9	<0.07	1.06	63.981
2	2.66	2.23	1.24	31.3	<0.07	0.236	37.666
3	11.47	27.2	2.209	47.3	<0.07	1.542	89.721
4	4.56	5.5	1.633	38.9	<0.07	0.533	51.126
5	7.69	18.8	2.075	31.6	<0.07	0.995	61.16
6	2.69	3.2	1.496	24.6	<0.07	0.293	32.279
3 Phase System with CC Inductor							
1	16.6	5.24	2.85	26.7	<0.07	0.11	51.5
2	6.76	0.74	2.43	24.6	<0.07	0.04	34.57
3	22.2	8.9	3.49	31.6	<0.07	0.14	66.33
4	13.5	1.85	2.975	29	<0.07	0.02	47.345
5	20.68	6.2	3.518	22.3	<0.07	0.0774	52.7754
6	14.8	1.09	2.96	19.6	<0.07	0.0062	38.4562

As was mentioned in the boost design section 4.1, there will be three comparisons

between the 3 phase interleaved system using AGP4233-103ME inductors from Coil Craft, the single phase system using the 3C97 inductor designed using GA optimization and a 3 phase interleaved system using three 3C97 inductors. The results for this comparison are shown in Table 7.2 showing the breakdown of the data. This comparison was done using MATLAB/Simulink subject to the same operating conditions shown in Table 7.1 which are categorized as the test conditions one through to six in Table 7.2. The single phase inductor has the highest converter losses while the three phase has the lowest. As was mentioned, the single phase has the lowest volume while the three phase CoilCraft design has the highest volume and highest inductor losses. Overall the three phase system using three of the 3C97 inductors would be the best based on volume and losses.

7.2 Buck Converter Experimental Results

The buck converter test results are shown in Fig. 7.8 to Fig. 7.10 with the converter operating at full load for different operating conditions. In Fig. 7.7 and Fig. 7.8 the buck converter is operating at an input of 50V and 60V respectively for an output of 12V, while Fig. 7.9 and Fig. 7.10 are for an input of 48V and 60V respectively for an output voltage of 24V. The plots show the input voltage in green, input current in red, output voltage in yellow and output current in blue. The buck converter was simulated at the same input and output voltages for the four conditions and the results are shown in Table 7.3. Each test condition has roughly the same efficiency while the simulated results are different for an output of 12V verses 24V. The simulated results make intuitive sense since a higher voltage results in a lower current and lower losses. But clearly the difference between the simulated

and experimental results, specifically for 24V output, is quite large. Further analysis is needed to close this gap.

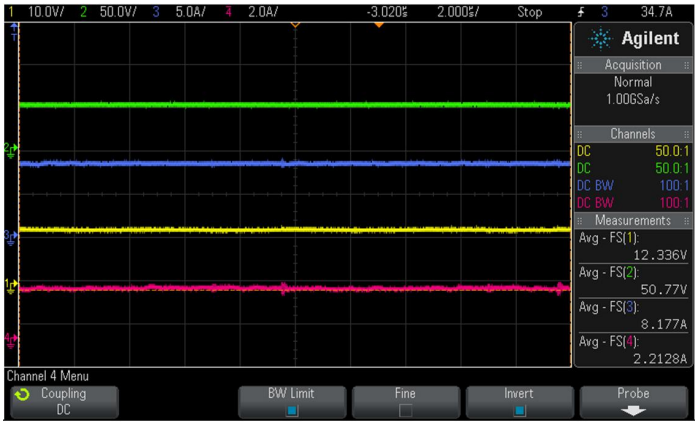


Figure 7.7: Buck converter 12V out 50V in Pin 112.34W, Pout 100.9W, eff 89.8 percent. input voltage (green), output voltage (yellow), output current (blue), input current (red).

Figure 7.8: Buck converter 12V out 60V in Pin 109.4W, Pout 98W, eff 89.66 percent. input voltage (green), output voltage (yellow), output current (blue), input current (red).

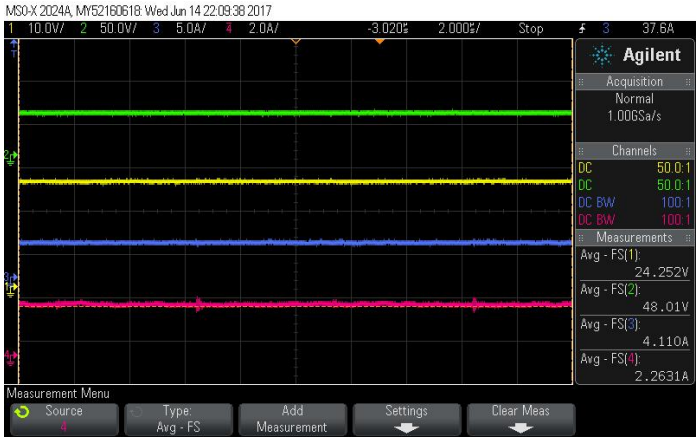


Figure 7.9: Buck converter 24V out 48V in Pin 108.65W, Pout 99.67W, eff 91.7 percent. input voltage (green), output voltage (yellow), output current (blue), input current (red).

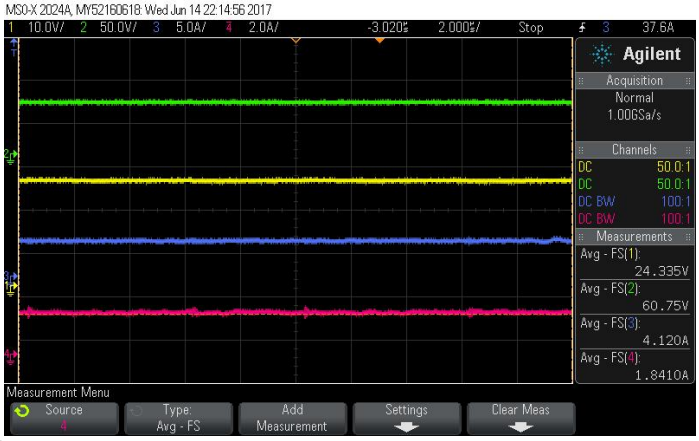


Figure 7.10: Buck converter 24V out 60V in Pin 111.8W, Pout 100W, eff 89.6 percent. input voltage (green), output voltage (yellow), output current (blue), input current (red).

Table 7.3: Experimental and Simulated Buck Converter Data

Experimental Buck Converter Data							
Test	V_O(V)	I_O(A)	P_O (W)	V_{in} (V)	I_{in}(A)	P_{in} (W)	Eff (%)
1	12.12	8.09	98.03	59.66	1.83	109.42	89.59
2	12.34	8.18	100.87	50.77	2.21	112.34	89.79
3	24.25	4.11	99.68	48	2.26	108.62	91.7
4	24.34	4.12	100.26	60.75	1.84	111.84	89.65
Simulated Buck Converter Data							
Test	V_O(V)	I_O(A)	P_O (W)	V_{in} (V)	I_{in}(A)	P_{in} (W)	Eff (%)
1	12.15	8.09	98.27	59.66	1.79	106.67	92.12
2	12.35	8.18	100.99	50.77	2.15	109.16	92.52
3	24.25	4.11	99.67	48.01	2.13	102.14	97.58
4	24.35	4.12	100.32	60.75	1.70	103.28	97.14

7.3 Cell Phone Converter Experimental Results

There are three 5V, 1A charging ports available for cell phone charging using the integrated converter SHHD003A0A [97]. Fig. 7.11 shows the total output power if one port is drawing 15W. This matches closely with the performance data provided by the DC-DC converter manufacture shown in Fig. 7.12 which show the efficiencies of the converter at different operating conditions. The test was done at an input of around 48V so the blue line is used. Here the output current is 3.047A so from Fig. 7.12 the experimental efficiency matches closely with the efficiency in Fig. 7.12. The simulation of the cell phone charging was not done since the internal circuit and control technique is not available. It is also a minor component of the proposed system and it not the main focus of this work.

Figure 7.11: Cell phone Testing. Pin 17.62W, Pout 15.36W, eff 87.19 percent. Input voltage (green), output voltage (yellow), output current (blue), input current (red).

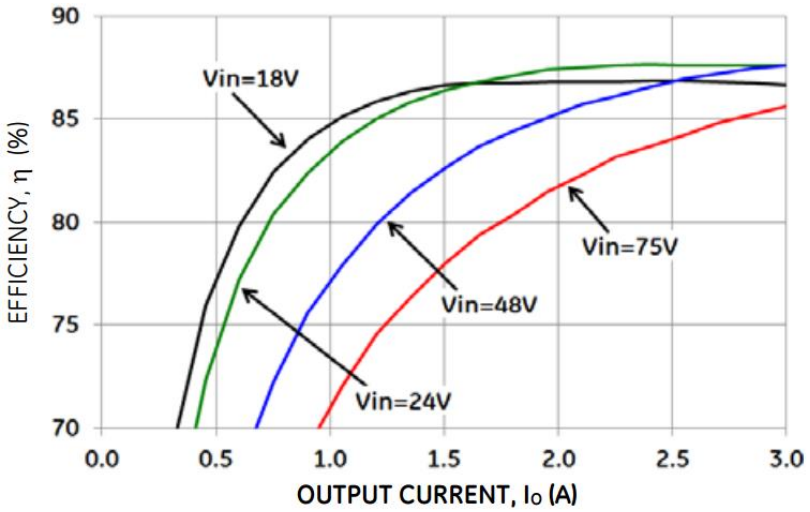


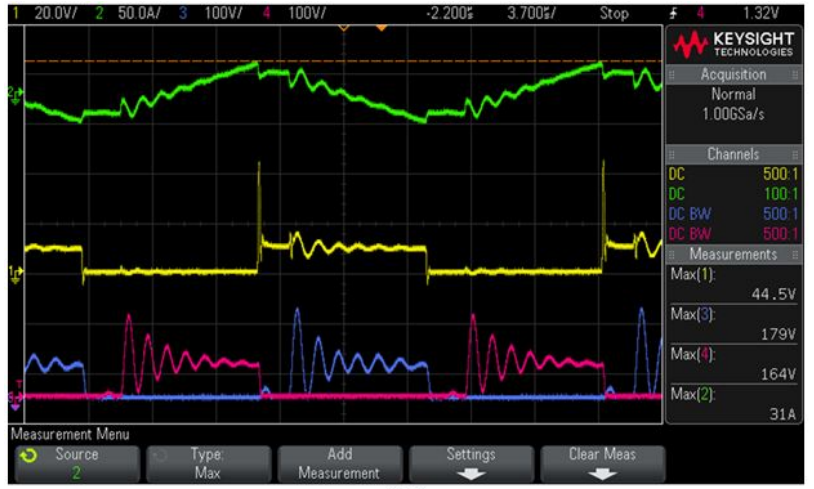
Figure 7.12: SHHD003A0A performance charts eff vs output current [97].

7.4 PSFB Converter Experimental Results

Fig. 7.13 shows the waveforms for the PSFB converter using the 8 turn planer transformer from Payton. There are high voltage peaks and resonance across the output rectifier as expected, however the resonance is quite more present in the experiment which restricts the operation of the converter due to the voltage limits

of the devices. This is due to the resonance between the transformer leakage inductance, capacitance, and the junction capacitance of the rectifier diodes [56, 98]. Planer transformers have low leakage inductance and but higher capacitance than other transformer types due to the stacking of PCBs. To reduce this oscillation, a 6 turn E core transformer was tested to see if the resonance and peaks in Fig. 7.13 disappear. Fig. 7.14 shows the waveforms for the 6 turn E core transformer and clearly the resonance frequency increased, but the voltage peaks are still present. The resonance frequency increased because the capacitance of the 6 turn foil transformer is lower than the planer transformer. This is due to stacking of multiple PCBs which builds the capacitance between stacks.

An RC snubber is designed in an attempt to help mitigate the peaks and resonance. The method discussed in [99] was used to design the RC snubber for the output diodes and the results are shown in Fig. 7.15 using the 6 turn transformer operating at an input voltage of 10V and output resistance of 100 ohms with a snubber circuit added across the low side diode of leg 2 using a calculated snubber capacitance of $470pF$ and snubber resistance of 300Ω. Clearly the snubber helps in reducing the resonance and reducing the voltage peaks, however the peaks are still quite high and will continue to increase as the input voltage increases. This peak voltage can be three times the voltage across the secondary so care must be taken to ensure these peaks are not too high during operation [63]. Using (7.1), the power loss of the RC snubber is 3.76W per diode for a capacitance of $470\mu F$, and output voltage of 400V. If the snubber capacitance is further increased the voltage peak reduces, however the losses are now larger which will result in lower efficiencies.



(a)

(b)

Figure 7.13: PSFB converter with 8 turn planer transformer operating at input voltage of 10 volts and output resistance of 100 ohms. Primary current (green), primary low side MOSFET (yellow), secondary leg 1 low side diode (blue), secondary leg 2 low side diode (purple) (a) snap shot showing voltage and current levels (b) snap shot showing resonance period.

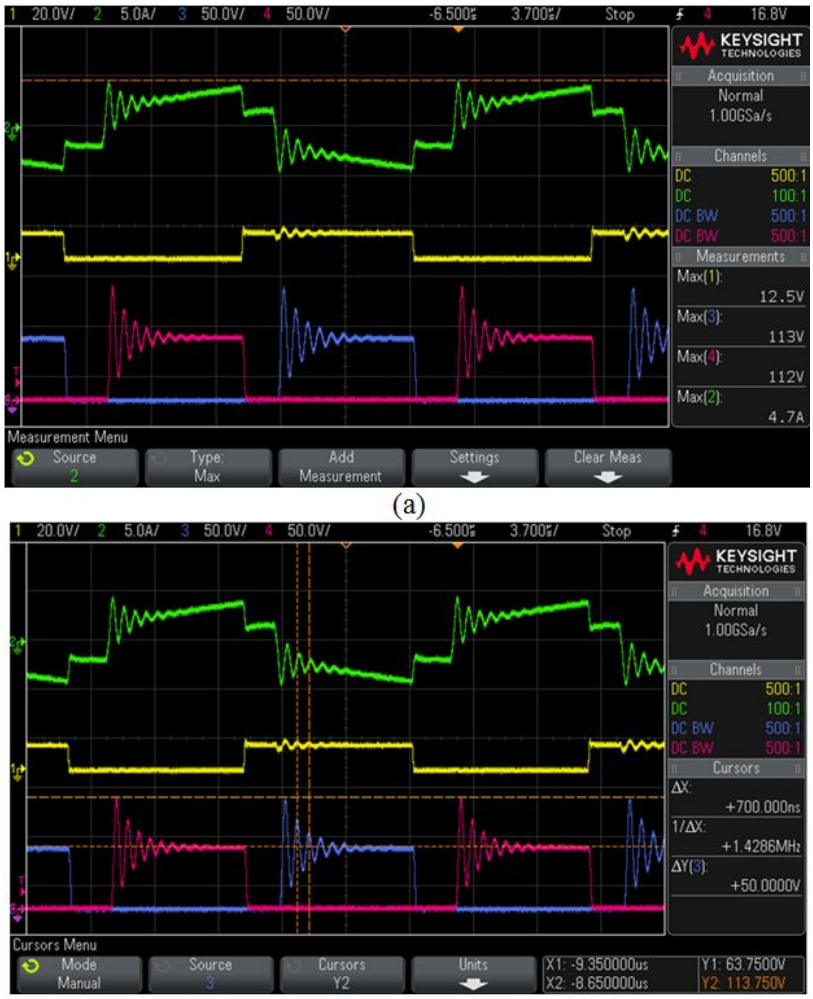


Figure 7.14: PSFB converter with 6 turn E core transformer operating at input voltage 10 V and output resistance of 100 ohms. Primary current (green), primary low side MOSFET (yellow), secondary leg 1 low side diode (blue), secondary leg 2 low side diode (purple) (a) snap shot showing voltage and current levels (b) snap shot showing resonance period.

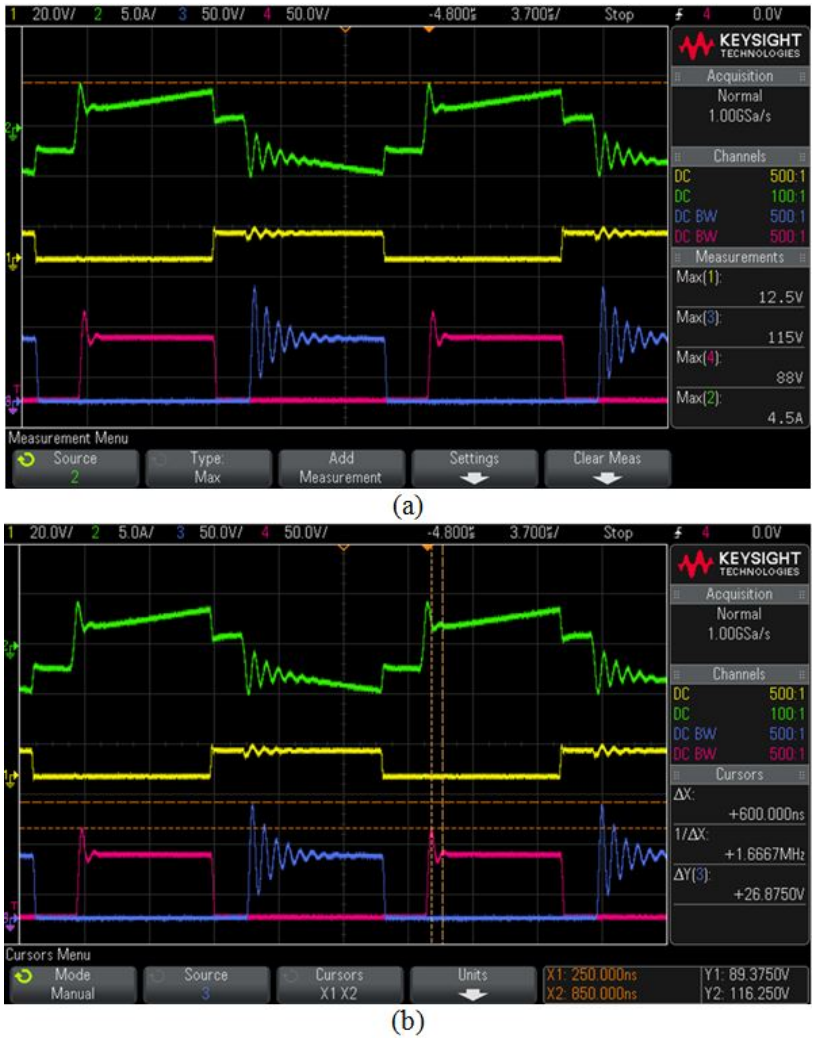


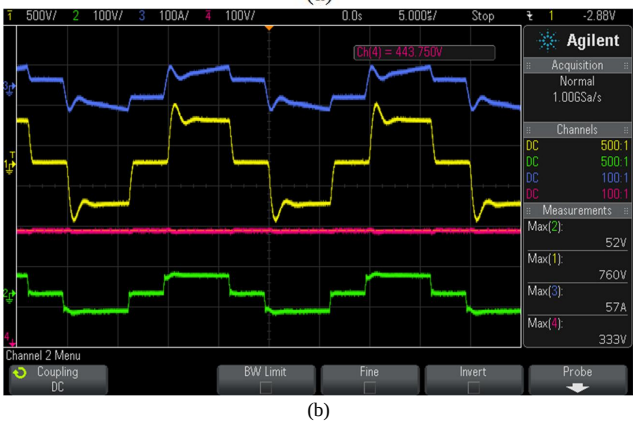
Figure 7.15: PSFB Converter. Primary current (green) output voltage (yellow) low side diode voltage with no snubber(blue) high side diode voltage with added snubber across diode (purple) (a) snap shot showing voltage level (b) snap shot showing resonance period.

$$P_{snubber} = C_{snubber} V_{DC}^2 f_{sw} \tag{7.1}$$

The best option is to redesign the PCB to minimize the stray inductance and capacitance as well as redesigning the high frequency transformer, or using a different circuit such as a voltage doubler on the secondary so that the voltage stress for the output is not as bad. In this situation some resonance might be acceptable. However,

this is beyond the scope of this work so it was decided to try two 6 turn transformers in series to help with the required conversion ratio which a single 6 turn transformer cannot achieve. This is easier than redesigning the PCB since there were available transformers. The input voltage range is 48V to 60V; using a 6 turn transformer means the best conversion ratio for 48V and 60V would be 288V to 360V which might not achieve the minimum output voltage requirement of 350V. Therefore, two 6 turn transformers were attached in series, achieving a 1:12 ratio which will help with reaching a minimum HVDC link bus voltage of 350V. It was also decided to switch the secondary side diodes for 900V SiC diodes to help with the voltage peaks across the rectifier diodes shown.

(a)

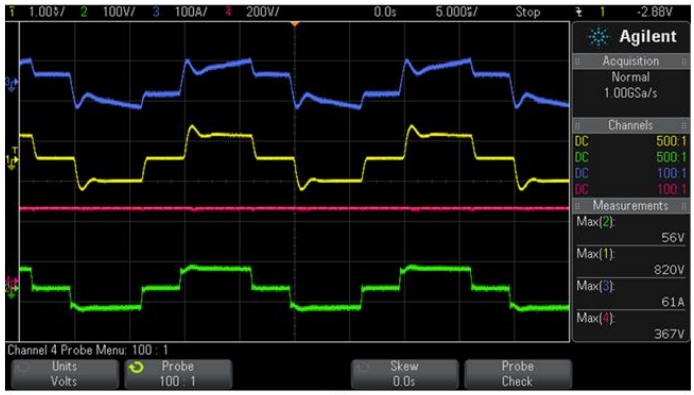


(b)

Figure 7.16: PSFB converter operating at 1.1kW for input voltage of 45V. (a) ZVS of lagging leg. Switch current (green), Vgs (blue), Vds (red). (b) primary current (blue), secondary voltage (yellow), output voltage (red), primary voltage (green).

Using the same snubber circuit, Fig. 7.16 and Fig. 7.17 show the PSFB converter operating at 1.1kW and 1.35kW respectively. ZVS is achieved for both operating conditions for the leading and lagging legs as can be seen from the waveforms shown in Fig. 7.16a and Fig. 7.17a where the red waveform is the voltage across the switch, green is the current through the switch and blue is the PWM gate signal. One thing to note is that the voltage peak across the secondary is still present and quite large, especially for the 50V input condition shown in Fig. 7.17. The peak is 820V which is approaching the 900V rating of the SiC diode, shown by the secondary voltage in yellow.

(a)



(b)

Figure 7.17: PSFB converter operating at 1.35kW for input voltage of 50V. (a) ZVS of lagging leg. Switch current (green), Vgs (blue), Vds (red). (b) primary current (blue), secondary voltage (yellow), output voltage (red), primary voltage (green).

Even when using the RC snubber and the 900V SiC diodes, the peak voltage across the diodes is closely approaching the 900V limit for an output voltage of 367V. Meaning that for higher input and output voltages greater than 367V, the voltage across the rectifier diodes will be greater than 900V. Possible solutions are:

- Redesign PCB and transformer to minimize stray/leakage inductance and capacitance
- Use a different snubber circuit with lower losses to allow higher capacitance and resistance values to further reduce voltage peaks across diodes
- Use voltage doubler secondary topology to reduce voltage peaks. (best choice)
- Use different isolated topology like the dual active bridge which has many advantages to the PSFB [100]

Figure 7.18: Experimental primary current (green).

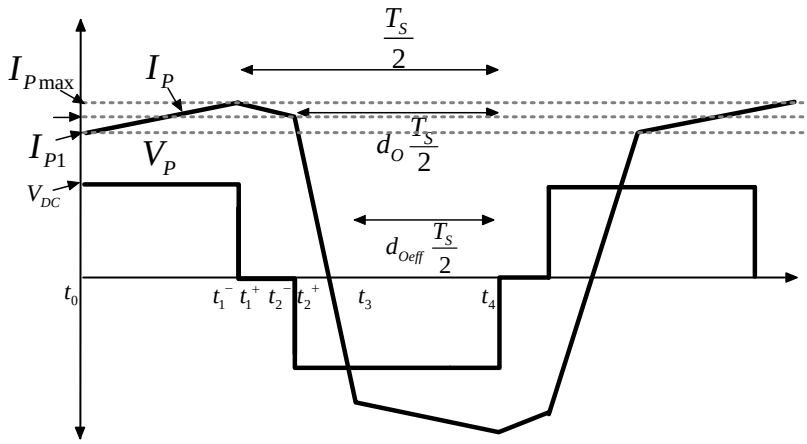


Figure 7.19: Theoritical primary current.

Another thing to notice about the experimental waveforms is that the primary current in Fig. 7.18, has a step which is not shown in the ideal waveform in Fig. 7.19. This drop is mainly caused by the output junction capacitance of the secondary diode rectifier and stray capacitance of the transformer [101, 102]. Things which should be done for the new PSFB converter include and not limited to:

- Redesign PCB to minimize stray inductance
- Select/Design new transformer which has higher number of turns, lower stray capacitance and inductance
- Use the voltage doubler topology to reduce voltage stresses on secondary rectifier diodes It might be a better idea to select a different isolate converter like the dual active bridge as there are many advantages it has over the PSFB converter

7.5 Inverter Experimental Results

The inverter was first tested using the designed integrated PCB. However, there were harmonic issues with the gate charging circuit as the current level increased.

These issues were present at low power, shown in Fig. 7.20 and Fig. 7.21. The inverter load current I_{AC} is in red, the load voltage V_{AC} is in yellow and the unfiltered load voltage V_{ab} is in blue, in relation to the single phase circuit shown in Fig. 7.22.

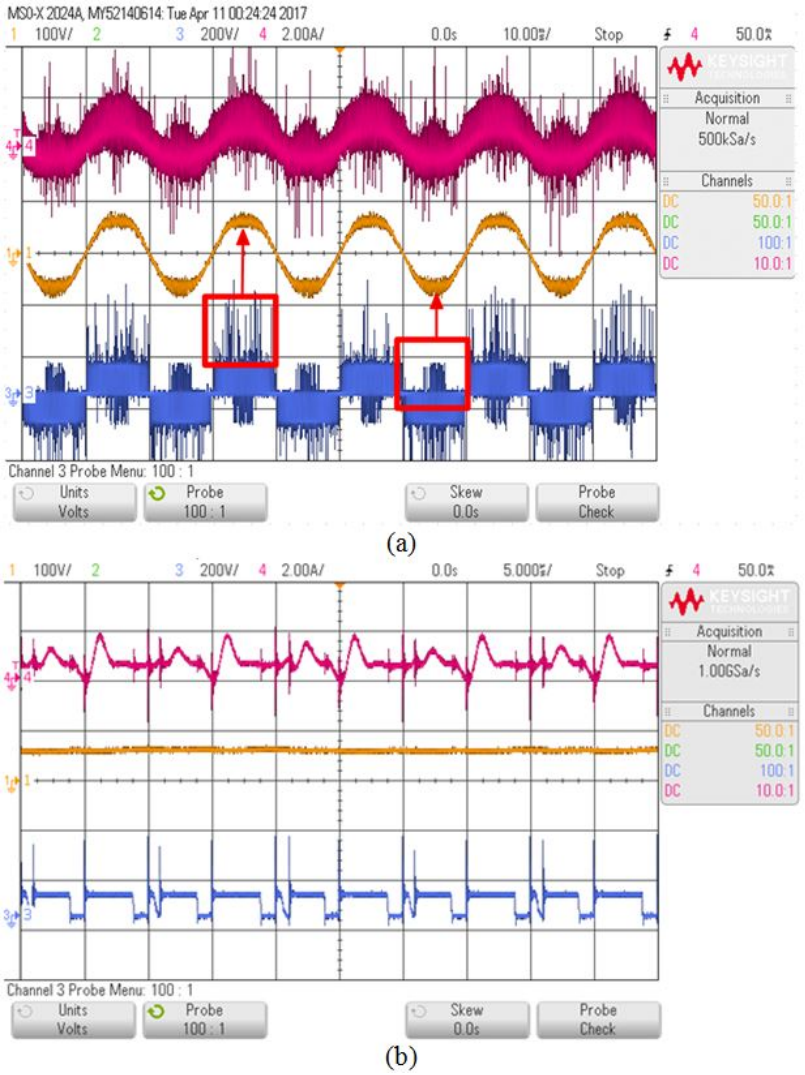


Figure 7.20: Inverter waveforms using integrated PCB. AC load current (red), AC load voltage (yellow) and unfiltered load voltage V_{ab} (blue) (b) zoomed in section of (a).

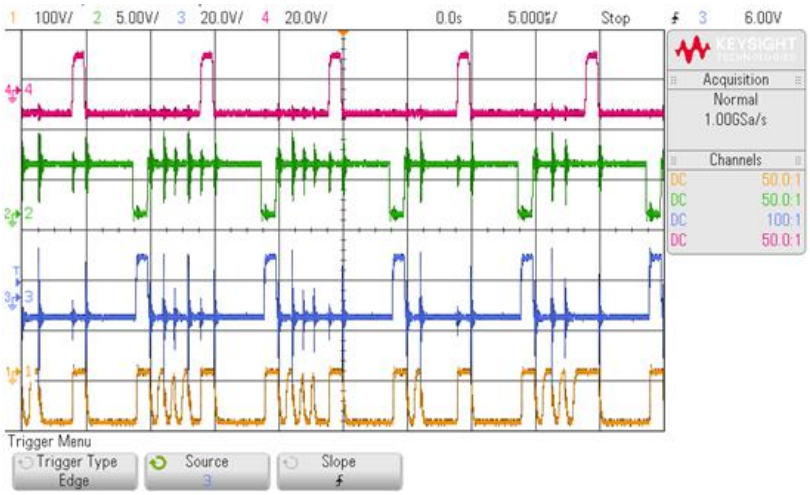


Figure 7.21: Gate signal during AC harmonics for each leg. Red and yellow are gate signals for leg 1 (S_9, S_{10}) while green and blue are gate signal for leg 2 (S_{11}, S_{12}).

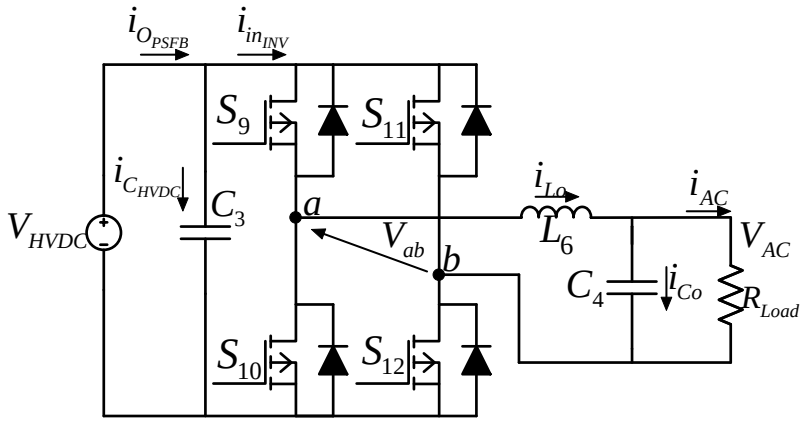


Figure 7.22: Single phase inverter off-grid inverter using LC filter.

At input voltages less than 100V this issue is not present. However, as the input voltage increases past this level, the resonance increases as the gate signals begin to have accidental turn-on and turn-off shown in Fig. 7.21, which clearly influences the inverter waveforms in Fig. 7.20. If the load resistance decreases, this issue occurs at a lower input voltage indicating that the resonance is current dependent and not voltage dependent. This is mostly likely due to poor PCB layout clearance, or from overlapping PCB conducting layers/pads which cause interlayer capacitance. A few things were attempted to mitigate these harmonics such as using different gate drivers,

adding extra gate resistance to slow down the charge time, adding pull down resistor etc. Unfortunately, these did not work so instead, it was decided to use a different PCB designed by a fellow Ph.D student Deqiang Wang for his grid connected 10kW Smart Home System. Since this is a high power inverter the MOSFETs implemented within this circuit are C2M0025120D SiC MOSFETs from Cree. The output filter is also different because this is a grid connected inverter which requires the current harmonic to be within a specified limit when connecting the inverter to the grid. As such, an LCL filter was implemented shown in Fig. 7.23 where L_6 is $49.5\mu H$, L_7 is $15\mu H$, C_4 is $8\mu F$ and R_{damp} is $0.6m\Omega$. The converter was run at roughly 250W, 500W, 750W and 1kW shown in Fig. 7.24 to Fig. 7.27 respectively.

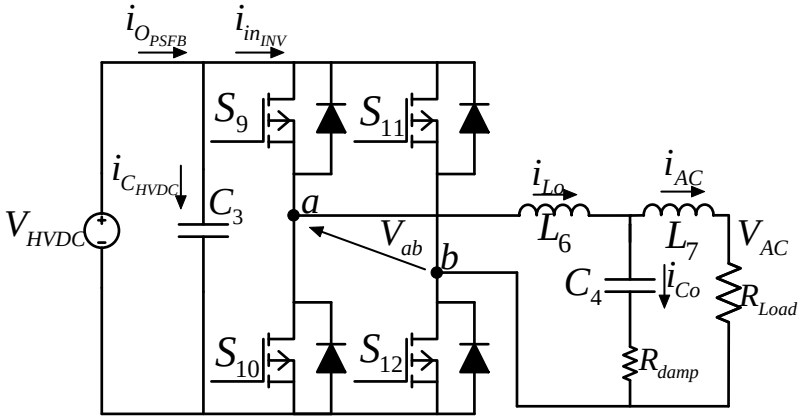


Figure 7.23: 10kW single phase grid connected smart home inverter using LCL.

For improved accuracy, a power analyzer (Yokogowa WT1800), and more accurate current transducers (Ultrastab 867-200IHF) powered by LEM IST ULTRASTAB power supply were used during the testing to measure the input and output voltage and current waveforms. The input current was measured using both a multimeter clap (FLUKE 325 Clamp meter), the Ultrastab 867-200IHF current transducer and a oscilloscope current probe. While the input voltage and output voltages were measured using FLUKE 115 multimeter and the power analyzer. All current measurements

were a bit different from each other with the data shown in Table 7.4. This is most likely due to the fact that the power analyzer can pick up harmonics which causes the input power to be different in comparison with the clamp meter and oscilloscope current probe methods which have lower bandwidth. Even a small current change will have a large effect on the efficiency. For example, if the input voltage is 350V and the measured input current is 1A the power will be 350W and if the current measurement is now 1.1A the power will be 385W making a difference of 35W. Just this small difference in current will create 35W difference which shows how the current measurement needs to be accurate as it greatly influences the efficiency calculation. The comparison between the scope measurements, the power analyzer measurements and the clamp current measurements are shown for each test condition in Table 7.4 and the efficiencies shown in Fig. 7.28.

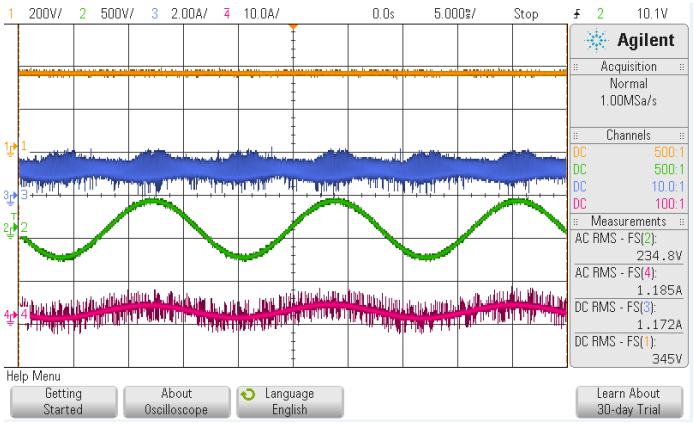


Figure 7.24: Single phase inverter experimental testing at 350V HVDC link voltage, 230V AC load voltage and 250W.

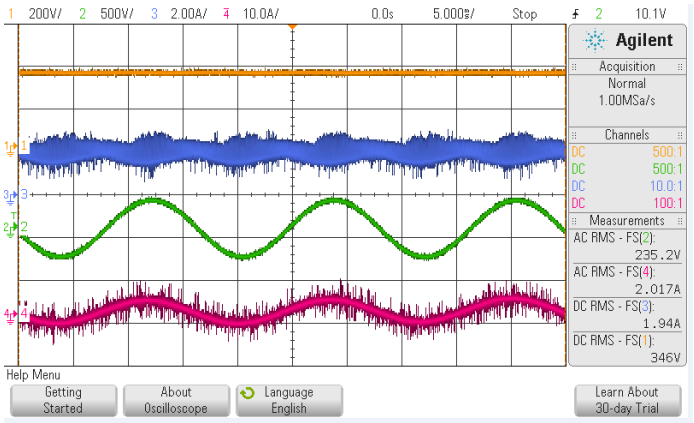


Figure 7.25: Single phase inverter experimental testing at 350V HVDC link voltage, 230V AC load voltage and 500W.

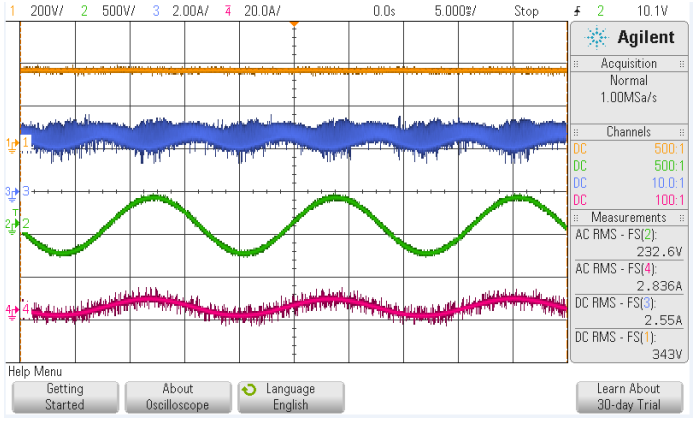


Figure 7.26: Single phase inverter experimental testing at 350V HVDC link voltage, 230V AC load voltage and 750W.

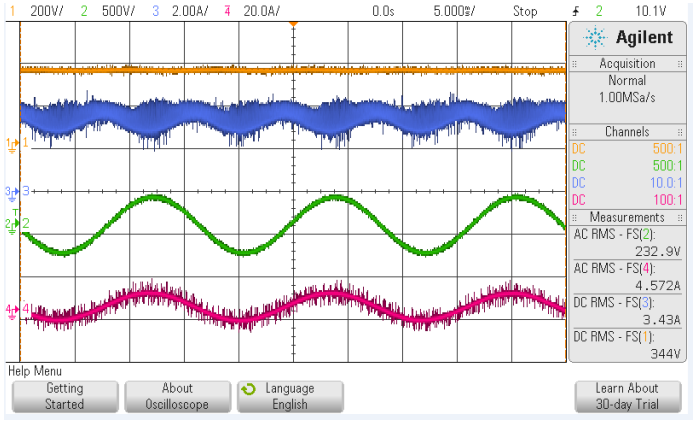


Figure 7.27: Single phase inverter experimental testing at 350V HVDC link voltage, 230V AC load voltage and 1kW.

Table 7.4: Single Phase Inverter Test Results

Scope Only Data							
Vout (V)	Iout (A)	Vin (V)	Iin (A)	Pout (W)	Pin (W)	Eff (%)	Losses (W)
234.8	1.185	345	1.172	278.238	404.34	68.81	126.1
235.2	2.017	346	1.94	474.398	671.24	70.67	196.84
232.6	2.836	343	2.55	659.653	874.65	75.42	214.99
232.9	4.572	344	3.43	1064.81	1179.92	90.24	115.1
Power Analyzer Data using current Clamp							
230.62	1.1435	352.01	0.97	263.72	341.45	77.236	77.73
231.21	2.2735	353.23	1.72	525.66	607.56	86.521	81.89
228.19	3.2112	349.1	2.33	732.76	813.4	90.086	80.64
228.86	4.4924	350.49	3.18	1028.1	1114.6	92.245	86.44
Power Analyzer Data using LEM ULTRASTAB 867-200IHF current transducer							
230.62	1.1435	352.01	1.5777	263.72	555.35	47.487	291.63
231.21	2.2735	353.23	2.341	525.66	826.91	63.569	301.25
228.19	3.2112	349.1	2.957	732.76	1032.3	70.984	299.53
228.86	4.4924	350.49	3.759	1028.1	1317.5	78.036	289.37

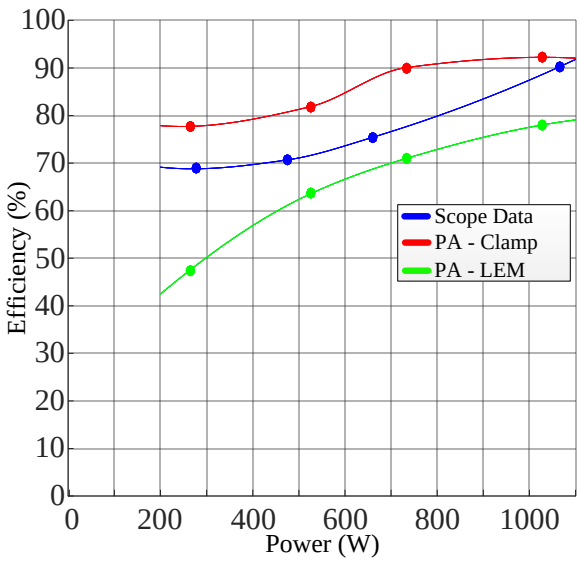


Figure 7.28: Comparison in testing methods for single phase inverter.

Using the more accurate measuring techniques results in lower efficiency shown by the green line in Fig. 7.28. Although, the efficiency is quite low. This could be because this inverter is designed for 10kW so the low powers will have low efficiencies. However, after some digging, it was found that one of the switches was malfunctioning and was producing more losses than the others so this is most likely the reason for the lower efficiency. Although, it is uncertain when this occurred so the best thing would be to replace the switch and test the inverter again.

This chapter discussed the experimental testing and simulation comparison for each converter. Each converter was tested at their full load conditions to both validate the designed converters, and also to compare the experimental modeling to the simulated modeling. The boost and buck converters were tested at full load using the integrated converter while the PSFB and inverter were tested using different components and PCBs because of some complications during testing. The PSFB had a few issues with the transformer and the secondary peak voltage and resonance while the inverter had issues with the gate driver due to accidental turn-on and turn-off.

Instead, a 12 turn transformer, and 900V SiC diodes were used in the PSFB and it was tested up to its full load. Unfortunately, the input voltage could not be increased because the voltage peak was approaching the voltage rating of the SiC diodes even after using a RC snubber. The inverter was tested with the help of a fellow Ph.D student Dejance Wang by using this designed single phase 10kW inverter. The inverter was tested at the loading conditions design herein without any issues. Finally a comparison between the designed GA inductor and an off-the-shelf inductor was done to compare losses and volume using the same testing conditions for the three phase interleaved boost converter prototype. The single phase boost converter using the design GA inductor has the lowest inductor losses and total converter volume but the total converter losses are the largest due to the large currents. Using the same designed inductor in a three phase system resulted in the lowest losses and can second in volume behind the single phase system indicating that the designed inductor is able to be the implemented boost converter in losses and volume.

Chapter 8

Conclusions and Future Work

This thesis presented the analysis and design of an integrated power electronic system for off-grid rural applications. This system is suited for a stationary application in which a large battery bank or another ESS. The input can be any DC source, however, it was presented that the move to solar is the most practical. Either way, the input will power one 12V-24V 100W DC load, three 5V cell phone charging ports, and one 230V 50Hz 1kW AC load.

Novelty of the system includes the proposed inductor design method incorporating the genetic algorithm technique used to optimize the design around specified current and inductance values. This method provides advantages over other techniques due to its scalability in that it can be applied to any inductor design, it is a faster design method than the traditional methods which can be tedious, time consuming and not arrive at an optimal results, and the customization also allows variability in the design as far as the inductor core geometry and winding selection. Comparisons were done between different inductor design using different windings covering different Litz bundles, from New England Wire, and also a custom rectangular wire construction.

After this comparison it was found that the rectangular wire construction achieved the lowest volume of 0.035 liters. Magnetic and thermal analytic estimations were then compared with results from a JMAG magnetic and thermal simulation to verify the results. Both matched closely with the simulations indicating the designed inductor will both operate within the design parameters, as well as verifying the design. Three boost converter designs were compared; a three phase interleaved boost system using AGP4233-103ME inductors from CoilCraft, a single phase system using the GA design inductor and an interleaved three phase system using the GA designed inductor. Results show that a single phase system using the designed inductor has the lowest inductor losses and inductor volume, but a higher system loss, while a three phase system using the designed inductor has both lower system losses but higher system volume than the three phase but lower system volume than the three phase system using the CoilCraft inductors. Therefore, based on volume, the single phase system would be best, but if loss and volume are both considered then the three phase system using the designed GA inductor would be the best. Due to the lead time and cost, the three phase interleaved boost converter using the CoilCraft inductors were prototyped to test the functionality and to verify the converter actually works with the control. Closed loops average mode current control was found to work and the converter was tested at its full load conditions, validating the design and control.

Next the buck converter design was completed using traditional methods such as the ripple requirements. This was a fairly simple and straight forward section on buck converter design. The converter was also tested using the average mode current control technique and was shown to achieve the full load requirements of 100W at both 12V and 24V.

The PSFB converter design required two different phase shift constraints; ZVS and output voltage. A comparison between both was done for varying leakage, output filter inductance and number of turns. A colour map indicated the trends in the design results and also the locations in which the ZVS constraint took precedence over the output voltage constraint and vice versa. The output voltage requirement must be met for the correct desired operation, along with achieving ZVS during its operation to decrease the losses of the converter. In the end, it was decided to select a leakage inductance of $27\mu H$ on the secondary, meaning the primary leakage inductance is $0.422\mu H$ while the output filter inductance value was determined to be around $300\mu H$. There were some testing issues due to resonance caused by the capacitance within the PCB circuit so attempts were made to mitigate these issues. Improvements were gained from the use of two 6 turn transformers in series, as well as adding a snubber circuit. However, there were still large voltage spikes on across the secondary rectifier diodes so future task will be required to improve on the design.

The inverter design covered input capacitor sizing and also output filter design. Input capacitor design is used to mitigate the propagated AC ripple which can cause significant issue. The output filter design is meant to filter the harmonics on the output voltage. There are specific THD limits that much be met when connecting any load. The filter was designed to have a cut off frequency of around 10kHz and the simulated results indicated the LC filter was able to achieve a THD of 0.31 percent. Unfortunately, due to most likely poor PCB layout and design, the inverter was unable to be tested using the integrated converter so another PCB from a student was used to test the single phase system only for testing purposes. The inverter was tested from about 250W up to 1kW for an input voltage of 350V and an AC output voltage

of 230V. Although, the inverter efficiency was quite low. This is most likely due to one switch malfunctioning, resulting in larger losses.

Full integrated converter simulations showing its operation and response to voltage and load changes was discussed and shown. During simulation the converter was able to meet the requirements and remain stable over the applied changes, indicating that the designed controllers and the system itself achieves the desired operation. However, it was shown that the input boost waveforms had non-ideal ripples if it was a real system. Meaning, if these current and voltage waveforms were actually present there could be issues. This is due to the AC propagation of the load. Thus, a simulation was done to improve this by increasing the HVDC link capacitance by $1mF$. This reduced the ripple by quite a bit but it was not entirely removed so this is something that needs to be looked into in the future. Each converter was also simulated to determine its efficiency over varying loads by simulating each component and estimating it loss.

A comparison between the estimated losses and experimental losses was done for the boost, and buck converter individually. For some of the test converter points the difference between simulation and experiment were close, but for other test points, there were larger differences. These differences could be due to inaccurate measuring techniques and methods, mistakes made during loss estimation, or by losses that were not simulated such as PCB trace losses.

There are many things which need to be done to improve this system. First would be to redesign the integrated PCB so that the harmonic issues do not occur for the inverter. This was the main issue with the inverter which resulted in using another PCB to do the testing. Having no overlapping trace paths will help in reducing the capacitance, reducing the trace lengths will help reduce the stray inductance, or

adding filter capacitors after these longer traces will help mitigate the stay inductance.

Next, the designed GA inductor needs to be manufactured and tested within the boost converter circuit to compare both the losses and temperature estimation to fully validate the design. A comparison between other core materials should also be done to see which core material provides the best performance and volume subject to the design specifications. Magnetic equations used were very simple, but more advanced magnetic circuits can be used to design the inductor and should be looked into for future designs. The air gap effect is another area which can be further developed and made more accurate since this design did not go into great detail into the effect the air gap has on the magnetic and electrical aspects of the inductor.

Change the PSFB secondary into a voltage double circuit to remove the large voltage stresses across the diodes. The voltage doubler will also reduce the number of diodes by half. The other option is to implement a different isolated topology such as the dual active bridge, which has lower losses but larger number of switching devices. This would also be advantageous if an AC source was added to the AC side since the dual active bridge is bidirectional and would allow the AC source to power the DC side loads. If the same topology is going to be used then redesigning the isolated transformer to have lower capacitance would be another important thing to consider for future work

Design the system level control incorporating the ESS controller and the MPPT controller would be another area to work on in the future. To really make this a full system it needs to have the MPPT controller and the ESS controller. The only issue is that both of these are dependent on the size of the solar panel and size of the ESS. Getting the entire system to run is the end goal of this application so both of these

would need to be achieved.

The last thing would be the cooling system design for the switching devices and possibly inductor if required. This is even more relevant if the power of this system increases.

Appendix A

A1. GA MATLAB Code

Rec Winding Initilization File:

```
clc
clear all
close all
nvars=8;
air_gap_number_percol_lb=1;
air_gap_number_percol_ub=4;
w_lb=.1; %in cm
w_ub=5;%in cm
h_lb=.1;%in cm
h_ub=10;%in cm
lg_space_lb=0.05;%in cm
lg_space_ub=.3;%in cm
E_lb=0.5;%in cm
```

```
14 E_ub=10;%in cm
15 WAWidth_lb=.5;%in cm
16 WAWidth_ub=10;%in cm
17 WAHeight_lb=1;%in cm
18 WAHeight_ub=10;%in cm
19 D_lb=1;%in cm
20 D_ub=10;%in cm
21 lb = [air_gap_number_percol_lb,w_lb,h_lb,lg_space_lb, E_lb,
       WAWidth_lb, WAHeight_lb, D_lb];
22 ub = [air_gap_number_percol_ub,w_ub,h_ub, lg_space_ub, E_ub,
       WAWidth_ub, WAHeight_ub, D_ub];
23 PopInitRange_Data = [lb; ub];
24 PopulationSize_Data =100000; % fill here changed from 2500;
25 Generations_Data =50; % fill here;
26 %% Variable Initialization
27 w_init=0.7; %in cm
28 h_init=0.1; %in cm
29 air_gap_number_percol_init=1;
30 lg_space_init=0.05; %in cm
31 E_init=0.749; %in cm
32 WAWidth_init=.7; %in cm
33 WAHeight_init=4; %in cm
34 D_init=1.4; %in cm
```

```
35 InitialPopulation_Data  = [air_gap_number_percol_init, w_init,
       h_init, lg_space_init, E_init, WAWidth_init, WAHeight_init,
       D_init];
36 %% Start with the default options
37 options = gaoptimset;
38 %% Modify options setting
39 options = gaoptimset(options,'PopInitRange',
       PopInitRange_Data);
40 options = gaoptimset(options,'PopulationSize',
       PopulationSize_Data);
41 options = gaoptimset(options,'Generations', Generations_Data)
       ;
42 options = gaoptimset(options,'InitialPopulation',
       InitialPopulation_Data);
43 % options = gaoptimset(options,'Display', 'diagnose');
44 options = gaoptimset(options,'PlotFcns', {  @gaplotbestf
       @gaplotbestindiv });
45 % options = gaoptimset(options,'Vectorized', 'off');
46 options = gaoptimset(options,'UseParallel', 'always');
47 options = gaoptimset(options,'TolFun', 1e-19);
48 % ConstraintFunction = @simple_constraint_AWG38;
49 [x,fval,exitflag,output,population,score] = ...
50 ga(@Thesis_InductorDesign_REC_GA,nvars,[],[],[],[],lb,ub
       ,[],[1],options);
```

```
51 fprintf('The best function value found was : %g\n', fval);
```

Rec Winding Objective File:

```
1  function [OBJ] = Thesis_InductorDesign_REC_GA(param)
2  L=17.5e-6;
3  fsw=100000;
4  3c97_perm=2300;
5  Idc=51.4403;
6  deltaIL=8.2286;
7  Imax_new=Idc+deltaIL/2;
8  a20=.00393;
9  Tmax=100;
10 Ta=30;
11 p20=1.68e-8;
12 air_gap_number_percol=param(1);
13 w=param(2); %in cm
14 h=param(3); %in cm
15 p=w/0.95; %cm
16 lg_space=param(4);%cm
17 E=param(5); %cm
18 WAWidth=param(6);%cm
19 F=WAWidth; %cm
20 WAHeight=param(7); %cm
21 D=param(8); %cm
22 Ac=D*E;
```

```
23 lg_total=air_gap_number_percol*lg_space*2; %cm
24 G=WAHeight; %cm
25 if G<lg_total/2 % air gap can't be larger than the window
       height
26 Volume=10000000;
27 else
28 MPL=((WAWidth+WAHeight)*2+pi*E)-lg_total; %in cm
29 if air_gap_number_percol<1
30 Fringe=1;
31 else
32 Fringe=1+lg_space*log(2*WAHeight/lg_space)/sqrt(Ac);
33 end
34 N_Coil=ceil(sqrt((lg_total+MPL/3c97_perm)*L/0.4/pi/Ac/Fringe
       /(10^-8))/2);
35 Bac=0.4*pi*2*N_Coil*Fringe*deltaIL*(10^-4)/2/(lg_total+MPL/3
       c97_perm); %tesla
36 Bdc=0.4*pi*2*N_Coil*Fringe*Idc*(10^-4)/(lg_total+MPL/3
       c97_perm); %tesla
37 Bmax=Fringe*0.4*pi*N_Coil*2*Imax_new*(10^-4)/(lg_total+MPL/3
       c97_perm); %tesla
38 if Bmax>0.41 %max core saturation
39 Volume=10000000;
40 else
41 Ntl=floor(G*0.93/p);
```

```
42 if Ntl<1
43 Volume=10000000;
44 else
45 Num_Bundle_Layers=ceil(N_Coil/Ntl);
46 if Num_Bundle_Layers<2
47 display('1 layer')
48 coil_height=N_Coil*p; %in cm
49 %  For a single layer coil the height equals the numbr of
      turns times the winding spacing
50 else
51 display('> 1 layer')
52 coil_height=p*Ntl; %cm % For more than 1 layer the coil
      height equals the number of turns in one layer times the
      winding spacing
53 end
54 EB=Num_Bundle_Layers*h; %cm  total coil width
55 if G < (coil_height/0.93) %window height limit
56 Volume=10000000;
57 elseif (EB*2>(F*0.93))% assume 1 bundle layer  window width
      limit
58 Volume=1000000;%allows WAWidth > EB*2.54*2/0.9
59 else
60 skin_depth=sqrt(1/(4*pi*10^-7*pi*fsw*58.5e6)); %m
61 Astr=h*sqrt(w/p)/(skin_depth*100);
```

```
62 FR=Astr*((sinh(2*Astr)+sin(2*Astr))/(cosh(2*Astr)-cos(2*Astr)
       )+2*(Num_Bundle_Layers^2 -1)*(sinh(Astr)-sin(Astr))/3/(
       cosh(Astr)+cos(Astr)));
63 if isnan(FR)
64 Volume=1000000000;
65 else
66 MTLin=pi*EB+2*E+2*D; %cm
67 res=(MTLin/100)*N_Coil*p20*(1+a20*(Tmax-20))/(w/100)/(h/100);
       %REC winding
68 Rdc_coil=res;
69 Rdc_total=Rdc_coil*2; %DC winding resistance
70 Rac_total=res*2*FR; %AC winding resistance
71 Pdc=Idc^2*Rdc_total; %DC winding losses
72 Pac=Rac_total*deltaIL^2/12;%AC winding losses
73 Pcore_density=(42.366*(fsw^1.16)*(Bac^2.8)*(((6.36e-5)*Tmax*
       Tmax)-(0.011*Tmax)+1.465)/1000); %3c97 ferroxcube core
       loss density
74 %Core Loss Calculation depends on the number of core blocks,
       which depends on the number of air gaps
75 if air_gap_number_percol==0;
76 display('No air gaps')
77 block_height=G;
78 block_vol=D*E*block_height;
79 top_bottom_vol=D*E*(2*E+F);
```

```
80  Pcore_block=Pcore_density*block_vol/1000;
81  Pcore_top_bottom=Pcore_density*top_bottom_vol/1000;
82  Pcore_total=Pcore_top_bottom*2+Pcore_block*2;
83  elseif air_gap_number_percol==1;
84  display('1 air gaps')
85  block_height=(G-lg_total/2)/2;
86  block_vol=D*E*block_height;
87  top_bottom_vol=D*E*(2*E+F);
88  Pcore_block=Pcore_density*block_vol/1000;
89  Pcore_top_bottom=Pcore_density*top_bottom_vol/1000;
90  Pcore_total=Pcore_top_bottom*2+Pcore_block*4;
91  else
92  display('> 1 air gaps')
93  block_height=(G-lg_total/2)/(air_gap_number_percol-1);
94  block_vol=D*E*block_height;
95  top_bottom_vol=D*E*(2*E+F);
96  Pcore_block=Pcore_density*block_vol/1000;
97  Pcore_top_bottom=Pcore_density*top_bottom_vol/1000;
98  Pcore_total=Pcore_top_bottom*2+...
99  Pcore_block*(air_gap_number_percol-1)*2;
100 end
101
102 Ptotal=Pcore_total+Pdc+Pac; %total losses
```

```
103 SANEW=2*(2*E+F)*D+4*D*E+4*E*(2*E+F)+2*coil_height*2.54*(2*EB
        *2.54+D)+coil_height*2.54*4*(2*EB*2.54+E)+8*EB*2.54*(2*EB
        *2.54+E)+4*EB*2.54*D; %inductor surface area
104 Tr_surface=450*(Ptotal/(SANEW))^0.826; %surface temperature
        rise
105 Tcore=Tr_surface+Ta ;%core temperature calculation
106 if Tcore<=105 %core temperature limit
107 IND_Width=F+2*E+EB*2;
108 IND_Height=G+2*E;
109 IND_Depth=D+EB*2;
110 Volume=IND_Width*IND_Height*IND_Depth; %inductor volume
111 else
112 Volume=1000000000;
113 end
114 end
115 end
116 end
117 end
118 end
119 OBJ_VT = Volume; %objective
120 OBJ = OBJ_VT;
121 end
```

Litz Winding Initilization File:

```
1 clc
```

```
clear all
close all
nvars=7;
position_lb=1;
position_ub=20;%<----need to change depending on the AWG
    selected
air_gap_number_percol_lb=1;
air_gap_number_percol_ub=4;
lg_space_lb=0.05; %in cm
lg_space_ub=.2;  %in cm
E_lb=0.2; %in cm
E_ub=5; %in cm
WAWidth_lb=0.5; %in cm
WAWidth_ub=20; %in cm
WAHeight_lb=0.5; %in cm
WAHeight_ub=20; %in cm
D_lb=1; %in cm
D_ub=20; %in cm
lb = [position_lb,air_gap_number_percol_lb,lg_space_lb,E_lb,
    WAWidth_lb, WAHeight_lb,D_lb];
ub = [position_ub,air_gap_number_percol_ub,lg_space_ub,E_ub,
    WAWidth_ub, WAHeight_ub,D_ub];
PopInitRange_Data       = [lb; ub];
PopulationSize_Data     =100000;
```

```
23 Generations_Data          =50;
24 %% Variables Initialization
25 E_init=0.5; %in cm
26 WAWidth_init=1; %in cm
27 WAHeight_init=4; %in cm
28 D_init=2; %in cm
29 position_init=5;
30 air_gap_number_percol_init=3;
31 lg_space_init=0.05; %in cm
32 InitialPopulation_Data  = [position_init,
       air_gap_number_percol_init,lg_space_init, E_init,
       WAWidth_init,  WAHeight_init,D_init];
33 %% Start with the default options
34 options = gaoptimset;
35 %% Modify options setting
36 options = gaoptimset(options,'PopInitRange',
       PopInitRange_Data);
37 options = gaoptimset(options,'PopulationSize',
       PopulationSize_Data);
38 options = gaoptimset(options,'Generations',Generations_Data);
39 options = gaoptimset(options,'InitialPopulation',
       InitialPopulation_Data);
40 % options = gaoptimset(options,'Display', 'diagnose');
```

```
options = gaoptimset(options,'PlotFcns', {  @gaplotbestf
    @gaplotbestindiv });
% options = gaoptimset(options,'Vectorized', 'off');
options = gaoptimset(options,'UseParallel', 'always');
options = gaoptimset(options,'TolFun', 1e-19);
% ConstraintFunction = @simple_constraint_AWG38;
[x,fval,exitflag,output,population,score] = ...
ga(@Thesis_InductorDesign_GA,nvars,[],[],[],[],lb,ub
    ,[],[1,2],options);
fprintf('The best function value found was : %g\n', fval);
```

Litz Winding Objective File:

```
function [OBJ] = Thesis_InductorDesign_GA(param)
%New England Wire Data. Change depending on AWG selected.
%str28=[3,5,7,10,17,26,42,66,105,165,...
%266,420,665,840,1080,1368];
% OD28=[0.027,0.035,0.042,0.05,0.065,0.08,0.102,0.14,...
%0.177,0.222,0.285,0.431,0.537,0.657,0.787,0.941];
% rdc28=[22.57,13.54,9.67,6.77,3.98,2.6,1.61,1.06,0.66,...
%0.42,0.26,0.17,0.11,0.084,0.065,0.051];
str30=[3,5,7,11,17,26,42,65,110,168,259,266,413,...
525,665,805,1250,1350,1950,2520];
OD30=[0.022,0.028,0.033,0.045,0.055,0.064,0.082,0.112,
0.145,0.191,0.237,0.24,0.3,0.338,0.38,0.421,0.631,0.667,...
0.794,0.981];
```

```
rdc30=[35.98,21.59,15.42,9.81,6.35,4.15,2.57,1.71,1.01,...
0.66,0.43,0.42,0.27,0.21,0.17,0.14,0.09,0.083,0.057,0.045];
% str33=[6,8,13,21,32,53,100,150,210,329,525,850,1320,...
%1800,2100,2700,3360,4200,5940,10176,14400,18200,31200];
%OD33=[0.025,0.025,0.035,0.044,0.054,0.066,0.099,0.121,...
%0.143,0.175,0.237,0.302,0.484,0.558,0.6,0.675,0.85,0.987,...
%1.29,1.8,2.42,3.12,3.99];
% rdc33=[35.99,26.99,16.61,10.28,6.75,4.07,2.22,1.48,1.06,...
%0.68,0.44,0.27,0.171,0.127,0.107,0.084,0.067,0.054,0.038,...
%0.022,0.016,0.012,0.007];
% str36=[4,7,10,16,27,41,65,105,165,265,420,660,1050,1800,...
%2660,3360,4320,5400,6840,8460];
%OD36=[0.013,0.017,0.024,0.029,0.037,0.045,0.061,0.073,...
%0.091,0.116,0.149,0.186,0.234,0.305,0%.37,0.548,0.655,...
%0.728,0.87,0.962];
%%rdc36=[109.6,62.7,43.9,27.4,16.3,10.7,6.91,4.26,2.72,...
%1.7,1.1,0.697,0.438,0.255,0.173,0.14,0%.109,0.087,0.069,55];
%%str38=[7,10,16,25,40,66,100,162,260,420,...
%660,1050,1650,2625,4140,5250,6600,8500,10500,13200];
% %OD38=[0.017,0.019,0.024,0.029,0.036,0.045,0.059,...
%0.069,0.093,0.117,0.149,0.2,0.249,0.32,...
%0.49%4,0.551,0.613,0.749,0.828,0.966];
%rdc38=[99.36,69.55,43.47,27.82,17.39,10.75,...
%7.16,4.38,2.76,1.74,1.11,0.7,0.45,0.29,...
```

```
%0.18,0.14%1,0.112,0.087,0.07,0.056];
% str40=[4,7,11,17,27,42,66,108,170,270,435,700,1100,1800,...
%2790,4455,7200,11000];
%OD40=[0.008,0.011,0.016,0.02,0.024,0.029,...
%0.038,0.045,0.056,0.069,0.093,0.126,0.157,...
%0.236,0.%293,0.431,0.572,0.668];
%rdc40=[293.84,167.91,106.85,69.14,43.53,...
%27.98,18.34,11.1,7.05,4.53,2.84,1.78,...
%1.13,0.7,0.451%,0.282,0.174,0.114];
fsw=100000;
3c97_perm=2300
L=17.5e-6
%AWG28_dia=0.0126; %in  inches
AWG30_dia=0.0100;  %in  inches
%AWG33_dia=0.00708; %in  inches
%AWG36_dia=0.00500; %in  inches
%AWG38_dia=0.00397; %in  inches
%AWG40_dia=0.00314; %in  inches
Idc=51.4403;
deltaIL=8.2286;
Imax_new=Idc+deltaIL/2;
Tmax=100;
Ta=30; %ambient Temp
position=param(1) %row selector
```

```
62 air_gap_number_percol=param(2)
63 Strand_Number=str30(position) %change depending on AWG
       selected
64 Dia_Bundle=OD30(position) %in inches %change depending on
      AWG selected
65 res_per_1000ft=rdc30(position) %change depending on AWG
       selected
66 lg_space=param(3) %in cm
67 lg_total=air_gap_number_percol*lg_space*2 %in cm
68 E=param(4)%in cm
69 WAWidth=param(5)%in cm
70 F=WAWidth %in cm
71 WAHeight=param(6)%in cm
72 G=WAHeight %in cm
73 D=param(7) %in cm
74 Ac=D*E %in cm
75 MPL=((WAWidth+WAHeight)*2+pi*E)-lg_total %cm
76 Fringe=1+lg_space*log(2*WAHeight/lg_space)/sqrt(Ac)
77 N_Coil=ceil(sqrt((lg_total+MPL/3c97_perm)*L/0.4/pi/Ac/Fringe
       /(10^-8))/2)
78 Bac=0.4*pi*2*N_Coil*Fringe*deltaIL*(10^-4)/2/(lg_total+MPL/3
       c97_perm) %tesla
79 Bdc=0.4*pi*2*N_Coil*Fringe*Idc*(10^-4)/(lg_total+MPL/3
       c97_perm) %tesla
```

```
80 Bmax=0.4*pi*2*N_Coil*Fringe*Imax_new*(10^-4)/(lg_total+MPL/3
       c97_perm) %tesla
81 Ntl=floor(G/(Dia_Bundle*2.54))
82 Num_Bundle_Layers=ceil(N_Coil/Ntl)
83 if Num_Bundle_Layers<2
84 display('1 layer')
85 coil_height=N_Coil*Dia_Bundle %inches
86 else
87 display('> 1 layer')
88 coil_height=Ntl*Dia_Bundle %inches
89 end
90 EB=(Num_Bundle_Layers*Dia_Bundle) %inches
91 Winding_Width=EB
92 if G<lg_total/2
93 Volume=10000000;
94 elseif Bmax>.41%max core saturation
95 Volume=10000000;
96 elseif G < (coil_height*2.54/0.93) % 93% margin
97 Volume=10000000;
98 elseif (Winding_Width*2*2.54>F*0.93) % If the winding width
       is larger than 93 percent of the total avaliable window
       width then this inductor is too large
99 Volume=1000000;
100 else
```

```
skin_depth=sqrt(1/(4*pi*10^-7*pi*fsw*58.5e6)) %m
Astr=AWG30_dia*2.54*sqrt(0.95)*((pi/4)^0.75)/(skin_depth*100)
    %change depending on the AWG slected
Num_Layers=ceil(Num_Bundle_Layers*sqrt(Strand_Number))
FR=Astr*((sinh(2*Astr)+sin(2*Astr))/(cosh(2*Astr)-cos(2*Astr)
    )+2*(Num_Layers^2 -1)*(sinh(Astr)-sin(Astr))/3/(cosh(Astr)
    +cos(Astr)))
MTLin=pi*EB+2*E/2.54+2*D/2.54 %in inches
Rdc_coil=MTLin*N_Coil*res_per_1000ft*(1+(Tmax-20)*0.00393)
    /12000
Rac_coil=Rdc_coil*FR
Rdc_total=Rdc_coil*2
Rac_total=Rac_coil*2
Pdc=Idc^2*Rdc_total
Pac=Rac_total*(deltaIL^2)/12%winding ac loss
Pcore_density=(42.366*(fsw^1.16)*(Bac^2.8)*(((6.36e-5)*Tmax*
    Tmax)-(0.011*Tmax)+1.465)/1000) %3c97 ferroxcube
if air_gap_number_percol==1 ;
num_blocks=2
block_height=(G-lg_total/2)/num_blocks
block_vol=D*E*block_height
top_bottom_vol=D*E*(2*E+F)
Pcore_block=Pcore_density*block_vol/1000
Pcore_top_bottom=Pcore_density*top_bottom_vol/1000
```

```
120 Pcore_total=Pcore_top_bottom*2+Pcore_block*4
121 else
122 num_blocks=air_gap_number_percol-1
123 block_height=(G-lg_total/2)/num_blocks
124 block_vol=D*E*block_height
125 top_bottom_vol=D*E*(2*E+F)
126 Pcore_block=Pcore_density*block_vol/1000
127 Pcore_top_bottom=Pcore_density*top_bottom_vol/1000
128 Pcore_total=Pcore_top_bottom*2+Pcore_block*(num_blocks)*2
129 end
130 Ptotal=Pcore_total+Pdc+Pac
131 SANEW=2*(2*E+F)*D+4*D*E+4*E*(2*E+F)+2*coil_height*2.54*(2*EB
        *2.54+D)+coil_height*2.54*4*(2*EB*2.54+E)+8*EB*2.54*(2*EB
        *2.54+E)+4*EB*2.54*D %inductor surface area
132 Tr_surface=450*(Ptotal/(SANEW))^0.826 %surface temperature
        rise
133 Tcore=Tr_surface+Ta %core temperature calculation
134 if Tcore>105 %max core temp limit
135 Volume=100000000;
136 else
137 IND_Width=F+2*E+EB*2*2.54
138 IND_Height=G+2*E
139 IND_Depth=D+EB*2*2.54
140 Volume=IND_Width*IND_Height*IND_Depth
```

```
141 end
142 end
143 OBJ_VT          = Volume;
144 OBJ             = OBJ_VT;
145 end
```

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