Three-Phase Dual Active Bridge Converter: Design Considerations and Planar Transformer Design

THREE-PHASE DUAL ACTIVE BRIDGE CONVERTER: DESIGN CONSIDERATIONS AND PLANAR TRANSFORMER DESIGN

By

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谨以此献给我的家人

To My Family

ABSTRACT

This thesis discusses comprehensive design considerations for the three-phase dual-active-bridge (DAB) converter and presents a planar transformer design for the three-phase DAB converter used in smart home applications.

An overview of the planar transformer, including magnetic cores, planar windings as well as its advantages and disadvantages are presented first. The review on analysis of transformer losses, leakage inductance and stray capacitance provides a guideline for transformer design.

The operating principle of three-phase DAB converter is presented and the closed form expression of zero-voltage-switching (ZVS) condition, current stress of switching devices and DC link capacitors are obtained. Analytical results are applied in the parameter design of the DAB converter.

A new design method for the three-phase DAB converter parameter selection is proposed. A new parameter fL is defined to simplify the analysis from three dimensions (n, f, L_k) to two dimensions (n, fL), from which the feasible value of n is determined. Together with the constraint of transformer design, the effective operating area (EOA) of f and L_k is obtained. The main losses that vary with the selectable parameters are studied and the corresponding converter efficiency is presented at different voltage and power levels. The parameters (n, f, L_k) are determined based on the comprehensive parameter design considerations of the three-phase DAB converter.

A planar transformer for the three-phase DAB converter is designed based on the mathematical analysis and finite element analysis (FEA). The parameters that determine core selection are derived for the three-phase DAB converter. The winding design is accomplished using the FEA simulations. The impacts of different winding structures on the AC resistance, leakage inductance and stray capacitance are investigated, and the fully-interleaved design is selected for its low resistance and structural simplicity.

The planar transformer prototype is built and tested in a three-phase DAB converter. The experimental waveforms at different voltage levels and power ratings demonstrate the effectiveness of the converter and transformer. The converter ZVS behavior and efficiency performance are measured, which validate the analysis.

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CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

2D	two dimensional
3D	three dimensional
AC	alternate current
CM	common mode
DAB	dual active bridge
DC	direct current
EMI	electromagnetic interference
EOA	effective operating area
ESR	equivalent series resistance
FEA	finite element analysis
HV	high voltage
IGSE	improved generalized Steinmetz equation
kHz	kilohertz
LV	low voltage
MHz	megahertz
MMF	magnetomotive force
OC	open circuit
PCB	printed circuit board
PWL	piecewise linear model
RMS	root mean square
SC	short circuit
ZVS	zero voltage switching

Chapter 1
INTRODUCTION

1.1. BACKGROUND

With the advancements in industry technology around the world, the continuously increasing energy consumption is becoming a major concern. Due to the shortage of fossil energy storage and the greenhouse emission, it is of great importance to reduce the energy consumption as well as seek alternative energy sources [1, 2].

In traditional power grid, electric power is delivered to users through long distance transmission line, which results in voltage drop and causes significant power losses. The power quality and reliability are degraded, especially in the rural area. By placing the power source close to the demand, the power loss on transmission line is reduced, which improves the efficiency and power quality in power distribution [3 - 5].

Smart home/grid with renewable energy sources such as solar and/or wind provide a solution to reduce carbon emissions as well as improve the power quality and efficiency. The solar/wind power sources installed in home or community provide power to household. It also has the ability to feed the excess energy back to the grid. By doing so, the power losses in the transmission lines are greatly reduced and the power quality and reliability are enhanced [6 - 8].

As a benefit of renewable energy, sustainable power supply can provide a lot of energy to meet the rapidly increased demand. However, the electric power generated by the renewable energy sources relies greatly on the weather condition, which makes it hard

to predict the power generation at a specific time period [1]. Energy storage systems are needed to absorb the instantaneously generated power, store the energy and provide power to the household when power generation is not enough.

Fig. 1.1 shows a conceptual smart home structure for future residential application [2], where the solar panel and/or wind turbine are placed on the roof. The renewable power generations are connected to the grid through high voltage (HV) DC bus and the corresponding DC/AC converter. To eliminate the impact caused by the intermittent nature of the renewable energy, energy storage devices are applied. In general, the storage devices consist of multiple 6- or 12-V battery cells. The standard voltage level of the battery pack is 48 V [9], which is named as low voltage (LV) battery in this thesis.

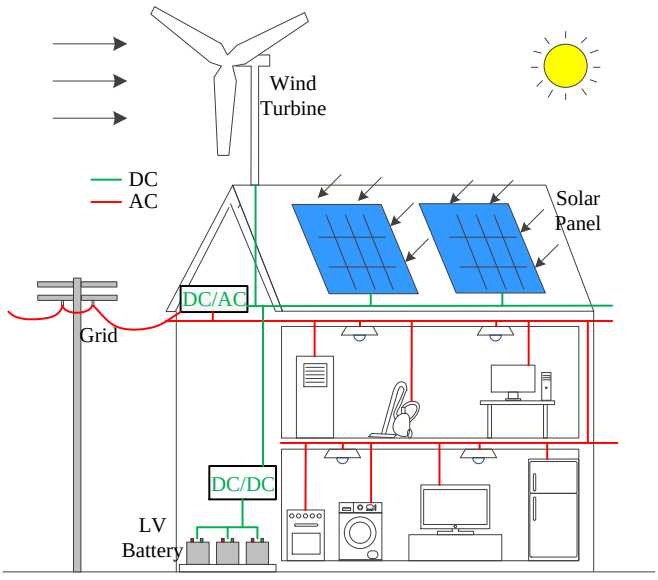


Fig. 1.1. Example of smart home for residential application [2].

The interface between HV DC bus (400 V) and the energy storage system desires a DC/DC converter with the ability of bidirectional power transfer. On one hand, this converter should be able to transfer the instantaneous electrical energy generated from

solar/wind to the LV battery pack. On the other hand, it should also allow the power transfer from the LV batteries to the load or back to the grid. In addition, galvanic isolation between HV DC bus and the LV battery pack is required for safety issues.

Considering residential power consumption of an average household, [10] gives the information provided by utility in the Middle Atlantic portion of the United States. For a household with footage area between 2000 ft^2 and 3000 ft^2, the maximum averaged daily electricity demand is 10.93 kWh. This data deviates with regional difference, seasonal variation, and it also depends if the dwelling is with electric heat or gas heat. In order to meet the average household needs, a 10 kW DC/DC converter is desired. Considering the terminal voltage variation of the LV batteries, the specifications of the target DC/DC converter is given in Table 1.1.

Table 1.1 Specifications of DC/DC converter

Primary DC voltage (LV side)	V_1	48 V (40 V - 56 V)
Secondary DC voltage (HV side)	V_2	400 V
Maximum power	P_N	10 kW

The bidirectional dual-active-bridge (DAB) converter is a promising candidate for smart home applications because of its bidirectional power flow capability, galvanic isolation and high efficiency [9, 11 - 13]. The configuration of single-phase DAB converter is shown in Fig. 1.2 [14]. Phase shift is applied between the primary and secondary bridges to control the transmitted power in both directions. Due to the ability to realize zero-voltage-switching (ZVS), high efficiency is achieved. This is very important

in applications that use MOSFET, as its turn-on loss is more significant compared to turn-off loss [15]. Contributed by the transformer applied in the DAB converter, galvanic isolation is realized between primary and secondary side.

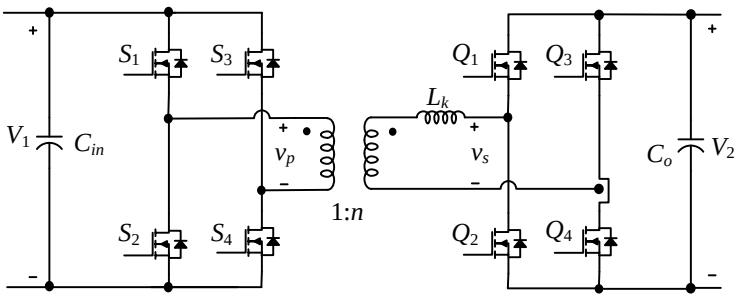


Fig. 1.2. Configuration of single-phase DAB converter.

However, due to the wide voltage range of the LV battery, the voltage ratio between primary and secondary side will deviate from the transformer turn ratio. In that case, hard switching happens, which leads to significantly lower converter efficiency, especially at light load. Improved modulation strategies [16 - 19] can be applied to improve the converter performance when the voltage mismatch happens. However, the output ripple current is still high, which increases the capacitor volume and decreases power density.

Different from single-phase DAB converter, three-phase DAB converter is composed of two three-phase half bridges and a three-phase transformer. Higher output power capability is achieved compared to single-phase DAB converter with the same current stress of devices. With higher ripple frequency, lower ripple current on the DC side is also achieved. Thus three-phase DAB converter is favored for its lower capacitor volume and higher power density [14, 15]. Details of three-phase DAB converter will be explained in Chapter 3.

The main parameters of the DAB converter include transformer turn ratio n, switching frequency f, and leakage inductance L_k. For a fixed set of parameters, the performance at different operating conditions (corresponding to different LV battery voltage and output power level) are quite different and need to be considered comprehensively in the design stage. Some optimization methods have been proposed for single-phase DAB converter. For example, in [20], the control variables are optimized to achieve highest efficiency for given parameters. The combination of selectable parameters (f, L_k) and (L_k, n) are studied in [21] and [22] respectively to achieve the tradeoff between converter efficiency and its volume. However, no comprehensive study that deals with the impacts of all the selectable parameters (n, f, L_k) on three-phase DAB performances, including ZVS range, converter efficiency and capacitor ripple current, are conducted.

In order to provide galvanic isolation, transformers must be incorporated between HV and LV side, as well as step up/down the output voltage to a proper level. However, they take up significant volume in the converter. The planar type transformer is advantageous to achieve a compact package. Due to the utilization of planar magnetic cores and windings as copper foils or printed circuit board (PCB), the converter profile can be reduced considerably. In addition, the manufacture process is also significantly simplified, and consistency of the transformers between unit to unit is also improved [23 - 25].

With the development of semiconductor devices, the switching frequency has been extended to hundreds of kilohertz (kHz) or even megahertz (MHz), which helps reduce

the size of magnetic components significantly. However, the transformer design is a great challenge. At high frequency, extra eddy current losses are introduced in the windings, which is difficult to estimate using traditional analysis. The increased parasitic parameters in planar transformer may also impact the converter performance [23], which should be taken into consideration in the transformer design.

1.2. OBJECTIVES

For smart home application, the DC/DC converter applied between HV DC bus and LV batteries requires high efficiency and power density. The converter performance is related to its parameters, and this should be considered in the converter design. Planar transformer is beneficial to achieve low profile and improve power density, and the design related issues should be addressed. The main objectives of this thesis are listed as below:

A comprehensive parameter selection for the three-phase DAB converter design is the first research objective. Considering the design of three-phase DAB converter, a comprehensive study of the impacts of all the selectable parameters on the converter performance are needed, including transformer turns ratio n, switching frequency f, and leakage inductance L_k. The ZVS range, converter efficiency and capacitor ripple current should be investigated under different voltage and power levels.

Planar transformer design for the three-phase DAB converter is the second research objective of this thesis. The impact of non-sinusoidal excitation waveform on magnetic core selection and core loss calculation needs to be considered. In high frequency

application, the effect of winding design and arrangement need to be investigated in the aspects of AC resistance, leakage inductance and stray capacitance.

1.3. THESIS OUTLINE

This thesis is organized as follows:

Chapter 2 presents a brief overview of the planar transformer as well as the related issues. The advantages and disadvantages of adopting planar transformer are discussed. Different types of planar core shape and material, as well as planar windings are presented. The eddy current effect due to the high operating frequency and the resulting AC resistance are also overviewed. Finally, the parasitic parameters and their impacts on the transformer performances are discussed.

Chapter 3 explains the basic configuration and operation characteristics of three-phase DAB converter. The operating scheme, waveforms as well as control strategy are discussed. The current stress of switches, ZVS condition and the ripple current through DC capacitors are presented in closed forms.

Chapter 4 presents comprehensive design considerations of three-phase DAB converter. The impact of parameters (n, f, L_k) on the converter performances, including ZVS operation area, switching device power losses, capacitor ripple current and system efficiency are studied. By taking different operating conditions into consideration, feasible range of the selectable parameters are determined to achieve overall high performance.

Chapter 5 presents the planar transformer design for the three-phase DAB converter. The transformer core is selected based on its power handling capability taking the excitation waveform into consideration. Winding design and arrangement are presented by considering their impacts on eddy current effect and parasitic parameters. The performances of the designed transformer are validated in ANSYS Maxwell 2D and 3D.

Chapter 6 presents the implementation of the transformer prototype and the experimental performance of the three-phase DAB converter with the transformer prototype.

Chapter 7 concludes the thesis and presents the possible future work.

Chapter 2
PLANAR TRANSFORMERS

2.1. OVERVIEW OF PLANAR TRANSFORMER

The desire for high power density and high efficiency power converters in industrial applications encourages the development of high frequency switching devices. As the switching frequency increases, the size of passive components, such as capacitors, inductors and transformers, can be significantly reduced. The use of conventional wire-wound transformers is becoming a big obstacle in applications that require low profile. In recent years, planar transformer has become increasingly popular in high frequency applications due to its lower profile, excellent thermal characteristics, good repeatability and easy manufacturing process [23, 26, 27].

2.1.1. Magnetic Cores

The key parameters of the core material include the saturation flux density, core loss and effective permeability. Materials with high saturation level and lower core loss are desired to reduce the core size and the temperature rise. High permeability is desired for higher magnetizing inductance and lower reluctance in magnetic path [25, 27].

Silicon steel is widely used in low frequency applications with high saturation (> 1.8 T). To further reduce the core losses, laminated magnetic steel is employed to mitigate the eddy current effect [28].For high frequency application, different magnetic materials are compared in Table 2.1. Ferrite core is widely used due to its high permeability and

resistivity. However, the saturation flux density is relatively low (0.39 T @ 100 ℃), which may results in a large core size. The amorphous material features high saturation level and high permeability, which help improve power density. However, it also has the highest loss density compared to other materials [29]. Nanocrystalline forms metallic tape-wounded core, which exhibits high saturation flux density and lower loss density. Thus higher power density and efficiency can be achieved with nanocrystalline core, but the cost is higher [30 - 32].

Table 2.1 Comparison of magnetic material properties

Material type	Ferrite	Nanocrystalline	Amourphous
Manufacturer	N87 Epcos	FT-3M Hitachi	2705M Metglas
Saturation flux density B_{sat} (T)	0.39	1.23	0.77
Effective permeability μ_e	1490	15 000	290 000
Core loss density (W/kg) (100kHz, 0.2T)	77	41	100

Ferrite material can be sintered into different core shapes, such as planar E, ER, RM and PQ cores. These core shapes feature very low profile, as shown in Fig. 2.1 (a), and they are commonly applied in high frequency power electronics applications. Nanocrystalline and amorphous material are commonly formed as toroidal cores and C cores, as shown in Fig. 2.1(b).

Compared to the wire-wound transformers, the planar cores with same power capability is usually 25% to 50% less in height [23]. A fair comparison of conventional

(EE 35/18/10) and planar core structure (EE 38/8/25) with similar power rating is given in Fig. 2.2. With lower profile, planar core has greater ratio between surface area and the core volume. As more surface area is attached to heatsink or exposed to air, more effective heat conducting and smaller thermal resistance can be achieved [24]. However, along with the low profile and good thermal performance, the large footprint area it occupies is an issue of planar transformer.

(a) (b)

Fig. 2.1. Core geometry (a) planar E, ER, RM and PQ core (b) toroidal and C core [33, 34].

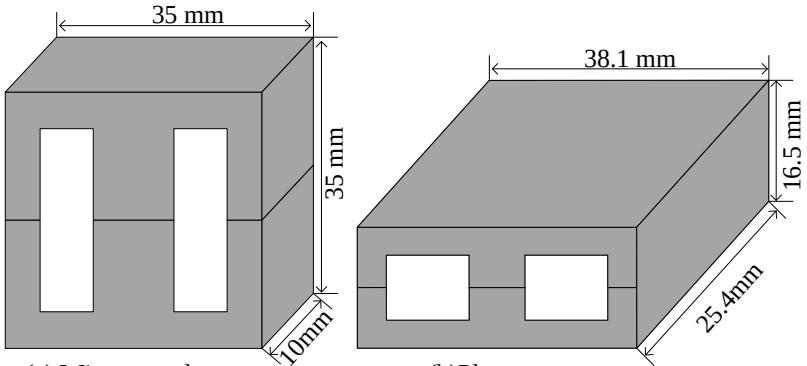


Fig. 2.2. Comparison of planar and wire-wound structure.

2.1.2. Planar Windings

The windings in planar transformers are usually constructed using PCB based windings and/or copper foils, as shown in Fig. 2.3 (a). Multilayer PCB provides a good solution for highly integrated windings with dielectric substrate. Stamped copper foils are

usually used in high current applications, where insulation film is applied between winding layers. To form parallel or series connection, extra connection between terminations of each layer is also needed, as depicted in Fig. 2.3 (b) and (c) [23, 24].

By applying multilayer PCB or copper foil windings, manufacturing can be simplified since manual or complex automatic wire-wound process are no longer needed. Repeatable and consistent manufacture is much easier to achieve, which is perfectly suitable for modular power converters or multi-phase converters where identical parameters are required. The thickness of flat conductors can be reduced to skin depth, which helps mitigate skin effect and reduce copper losses in high frequency applications [35]. Additionally, the transformer can be modeled in FEA simulation with high fidelity, and its performance can be predicted with high accuracy. Hence the design and validation of planar transformer are also simplified.

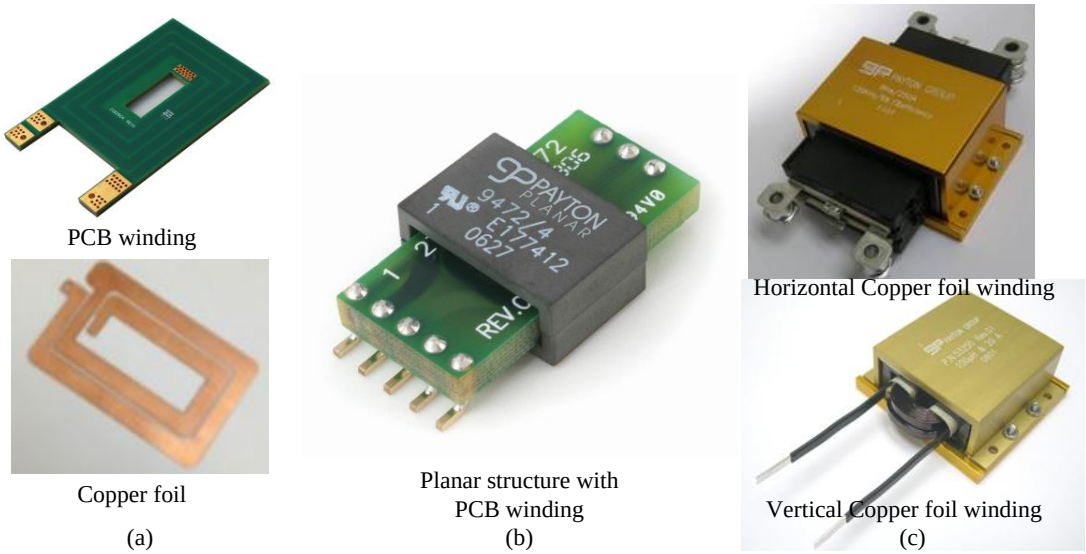


Fig. 2.3. Different implementation structure of planar windings [36, 37].

The use of PCB winding or copper foils also provides flexibility to interleave the primary and secondary windings, which reduce the leakage inductance and proximity effect significantly [23, 24, 38]. For example, two different winding arrangements and their magnetomotive force (MMF) distributions along the vertical direction of the windings are illustrated in Fig. 2.4. Taking advantage of the proximity effect, interleaved windings have more evenly distributed current. As a result, lower copper losses and leakage inductance are achieved. The effect of interleaving will be discussed in detail in next section.

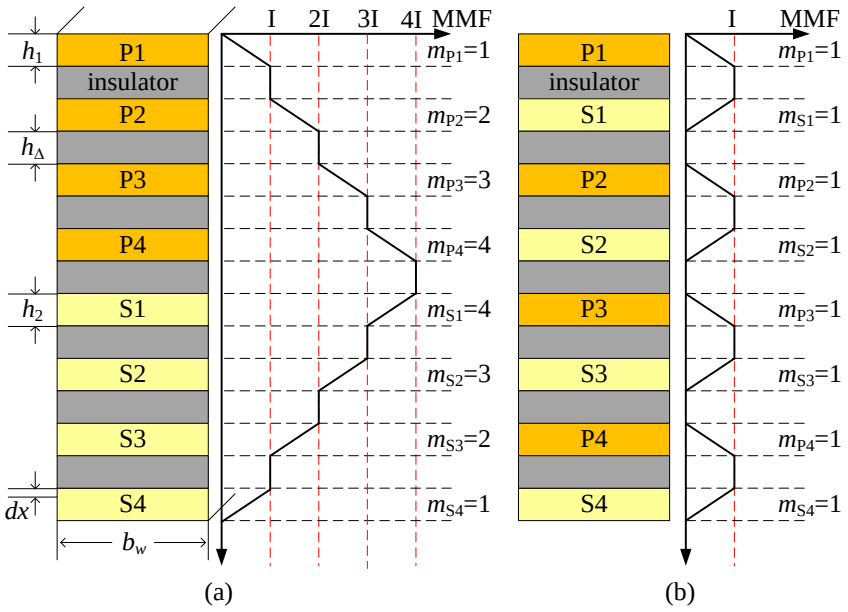


Fig. 2.4. MMF distribution of (a) non-interleaved winding (b) fully-interleaved winding.

Compared to wire-wound windings, the major drawback of planar windings is the lower utilization factor (0.18 to 0.25) [23, 39]. Due to the dielectric spaces required between turns, the number of turns and width of traces are also limited, hence the DC

resistance is increased. Additionally, the large overlap between planar windings results in increased stray capacitance, which is not desired in most applications [38].

2.2. TRANSFORMER LOSSES

2.2.1. Core Loss

There are mainly three methods to determine core losses: hysteresis model, loss separation approach [40, 41] and empirical methods. The first two approaches characterize satisfactory results but require excessive computations to extract the parameters in the models. The Steinmetz equation [42, 43] is the commonly used empirical method to characterize core losses.

$$p_v = KB_m^{\alpha} f^{\beta} \tag{2.1}$$

where, p_v is the core loss density. The core loss coefficient K, α, β can be obtained by curve fitting of the measured core losses provided by manufacturers, and $\alpha < \beta$.

2.2.2. Copper Loss

In high frequency applications, the transformer performance is significantly impaired by eddy current effect, including skin effect and proximity effect. Both skin and proximity effect causes non-uniformly current distribution in the cross-section of the conductor, hence decreases the effective cross-section area and increases the resistance of the windings. This leads to dramatically higher copper losses at higher frequency.

When high frequency current flows through a conductor, according to Lenz's law, the alternating flux in the conductor will induce eddy current, which tends to oppose the

alternating flux. Therefore, as shown in Fig. 2.5 (a), in the center of the conductor, the eddy current is in opposite direction to the main current *i*(t); while at the surface of the conductor, the eddy current and main current share the same direction. This results in increased current density near the conductor surface. Based on Maxwell's equation [44], the current distribution within the conductor can be obtained. The current density decreases exponentially along the radius distance to the center of the conductor, and mainly distributed within the skin depth δ of the conductor. At a certain frequency, the skin depth is given as

$$\delta = \sqrt{\frac{1}{\pi f \mu_0 \sigma}} \tag{2.2}$$

where, μ_0 = 4πx10^{-7} H/m is the vacuum permeability, σ = 5.7x10^{7} S/m is the copper conductivity.

The proximity effect shows similar characteristics. Take two flat conductors in Fig. 2.5 (b) with opposite current as an example, the flux induced by current i_A(t) further induces current in the adjacent conductor, which tends to oppose the AC flux. Therefore, current density is increased on the adjacent sides and decreased at the opposite side of the conductors.

AC resistance R_{ac} is the effective resistance that generate copper losses. Dowell's equation is the most commonly used method in characterizing copper loss. As the planar winding structure features high width to thickness ratio, it can be regarded as infinite foil conductor. Under sinusoidal excitation, the current density distribution within the planar conductor can be solved by general field solutions. Based on Dowell's assumption, the

eddy current effect can be represented by the ratio between AC resistance and DC resistance of a single (*m*th) layer [45 - 47], as shown in (2.3).

$$\frac{R_{ac,m}}{R_{dc,m}} = \frac{\xi}{2}\left[\frac{\sinh\xi+\sin\xi}{\cosh\xi-\cos\xi}+(2m-1)^2\cdot\frac{\sinh\xi-\sin\xi}{\cosh\xi+\cos\xi}\right] \tag{2.3}$$

where $\xi = h/\delta$, h is the conductor thickness, the DC resistance $R_{dc} = \rho\, l/A_s$, ρ is the copper resistivity, l is the winding total length, A_s is the cross-section of the winding. The ratio m is related to winding arrangement and it is defined as

$$m = \frac{F(h)}{F(h)-F(0)} \tag{2.4}$$

where $F(h)$ and $F(0)$ are the MMF at the vertical edges of a layer, which is also annotated in Fig. 2.4. The first term in (2.3) represents the skin effect, and the second term refers to proximity effect. The ratio between AC and DC resistance not only depends on ξ, but also relates to the ratio m, and their relationship can be plotted in Fig. 2.6 (a).

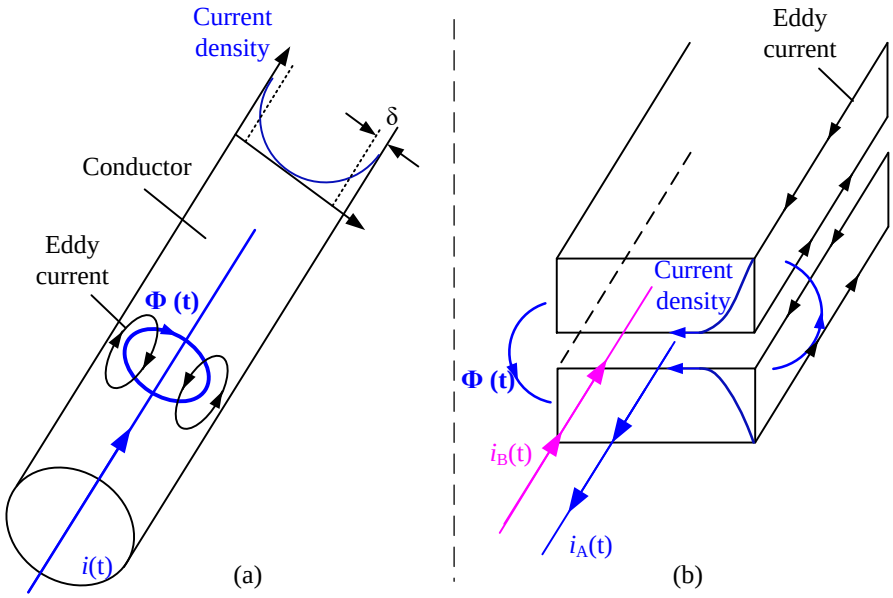


Fig. 2.5. Eddy current effect (a) skin effect (b) proximity effect.

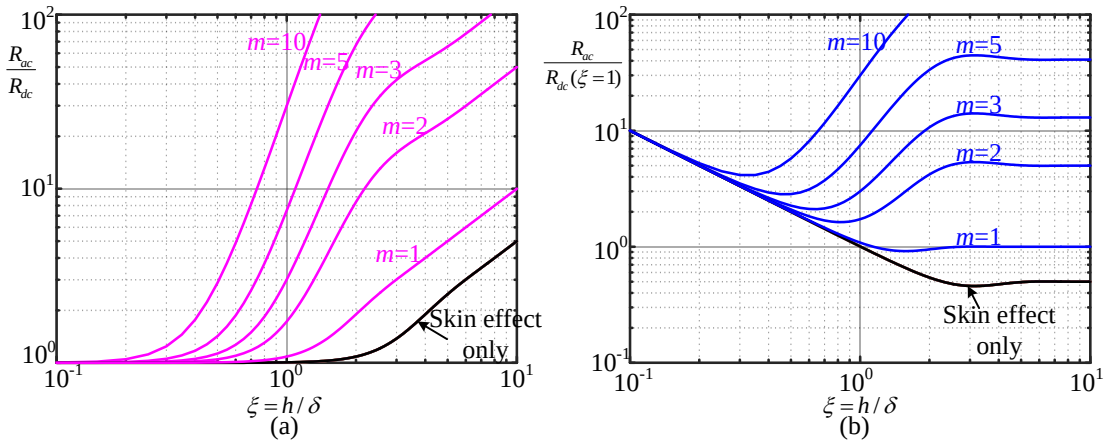


Fig. 2.6. (a) Ratio of AC to DC resistance
(b) ratio between AC and DC resistance with thickness of skin depth.

As indicated in Fig. 2.6 (a), the resistance ratio R_{ac}/R_{dc} increases dramatically with conductor thickness, which makes the selection of conductor thickness a key parameter in winding design. At a large ratio m, the proximity effect dominates over skin effect and increases the resistance dramatically. With reduced conductor thickness ($\xi < 1$), the resistance ratio decreases to 1, which suggests a low eddy current effect. The absolute AC resistance is calculated referred to the DC resistance when $h = \delta$ ($\xi = 1$).

$$\frac{R_{ac}}{R_{dc}(\xi=1)} = \frac{R_{ac}}{R_{dc}} \cdot \frac{1}{\xi} \tag{2.5}$$

Substituting (2.3) to (2.5), the ratio R_{ac}/R_{dc} ($\xi = 1$) can be obtained and plotted in Fig. 2.6 (b). From Fig. 2.6 (b), at given frequency and specified winding arrangement (corresponding to different ratio m), minimal AC resistance can be achieved by properly choosing conductor thickness [43]. To better estimate AC resistance with finite foil conductor and nonsinusoidal excitation, the correction factor is given in [46, 47]. More accurate AC resistance can be obtained by FEA simulation.

2.3. PARASITIC EFFECTS

2.3.1. Leakage Inductance

In a typical transformer, the magnetic flux generated by current in the primary winding is supposed to follow the magnetic circuit and link with the secondary winding, and vice versa [48, 49]. Realistically, although the main flux follows the magnetic path, some flux leaks from the core and returns to the air, the winding layers and insulation layers without linking the secondary winding. This imperfect flux coupling results in leakage inductance. The main flux and leakage flux paths are shown in Fig. 2.7. Almost all of the leakage energy is stored within the window area, and it can be calculated by integrating the energy density within this region.

$$E_{Lk} = \int_V \frac{1}{2} BHdV = \frac{1}{2} L_k I^2 \tag{2.6}$$

where the field intensity $H = F/b_w = NI/b_w$, flux density $B = \mu_0 H$, NI is the MMF distribution of each layer, and the differential volume $dV = l_w \cdot b_w \cdot dx$, l_w and b_w are the core window area length and width, dx is the vertical distance to the reference surface of each layer, as indicated in Fig. 2.4 [49].

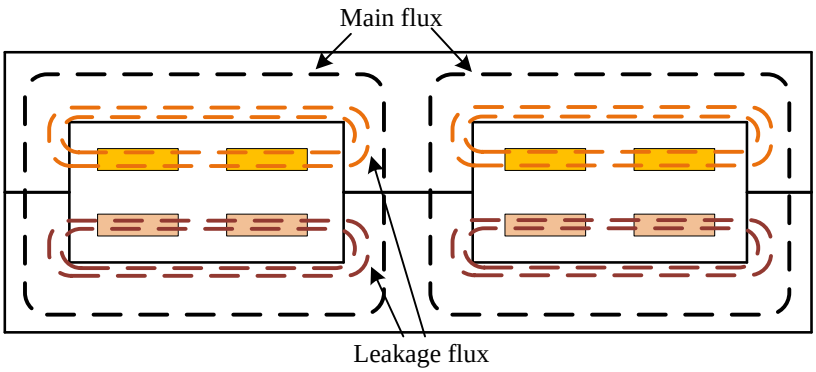


Fig. 2.7. Main flux and leakage flux paths.

The leakage inductance is related to the MMF distribution, which varies with different winding arrangements. For a non-interleaved winding structure in Fig. 2.4 (a), the leakage energy stored in all layers (primary, secondary and insulation layers) can be calculated as

$$E_{Lk} = \frac{\mu_0}{2} \sum \int_0^h H^2 \cdot l_w \cdot b_w \cdot dx \tag{2.7}$$

where, the field intensity H depends on the ampere-turns (NI) linked with the leakage flux path. The field intensity H in the primary winding in Fig. 2.4 can be expressed as (2.8) [48].

$$H = \begin{cases} \dfrac{(k-1)I}{b_w} + \dfrac{I}{b_w} \cdot \dfrac{x-(k-1)(h_1+h_\Delta)}{h_1} & (k-1)(h_1+h_\Delta) < x \le h_1 + (k-1)(h_1+h_\Delta) \\ k\dfrac{I}{b_w} & h_1 + (k-1)(h_1+h_\Delta) < x \le k(h_1+h_\Delta) \end{cases} \tag{2.8}$$

where the thickness of primary, secondary and insulation layer are h_1, h_2 and h_Δ, and they are indicated in Fig. 2.4. Substituting H to (2.7), the total leakage energy can be derived as

$$E_{Lk} = \frac{\mu_0}{2} \cdot l_w \cdot b_w \left[\begin{array}{l} 4\int_0^{h_1} \left(\dfrac{I}{b_w} \cdot \dfrac{x}{h_1} \right)^2 dx + 4\int_0^{h_2} \left(\dfrac{I}{b_w} \cdot \dfrac{x}{h_2} \right)^2 dx + \dfrac{\left(I^2 + 4I^2 + 9I^2\right)}{b_w^2} \cdot \\ \left(h_1 + h_2 + 2h_\Delta\right) + \dfrac{\left(I^2 + 2I^2 + 3I^2\right)}{b_w^2} \cdot \left(h_1 + h_2\right) + \dfrac{16I^2}{b_w^2} \cdot h_\Delta \end{array} \right] \tag{2.9}$$

Therefore, the closed form of total leakage inductance in Fig. 2.4 (a) can be expressed by [43]

$$L_k = \mu_0 \cdot \frac{l_w}{b_w} \left[\frac{64(h_1+h_2)}{3} + 44h_\Delta \right] \tag{2.10}$$

For the fully interleaved winding arrangement in Fig. 2.4 (b), the field intensity H is much lower. By applying similar approach, the leakage inductance can be derived as

$$L_k = \mu_0 \cdot \frac{l_w}{b_w} \cdot 4\left[\frac{(h_1 + h_2)}{3} + h_\Delta\right] \tag{2.11}$$

It is obvious that interleaved winding layout has significant advantage in reducing leakage inductance. The layer thickness (h_1, h_2 and h_Δ) can also be used to adjust the leakage inductance.

2.3.2. Stray Capacitance

In planar transformers, the windings are compactly placed in the core window area with a large overlap between adjacent layers. The small distance between windings results in significant inter-and intra-winding capacitance [50, 51].

The high inter-winding capacitance between primary and secondary windings provides a low impedance path for the high-frequency current, which can cause serious common mode (CM) problems and contribute to electromagnetic interference (EMI) issues. In addition, self-resonance might happen between the leakage inductance and stray capacitance, which results in voltage spike across the switches and deteriorate the converter performance [52 - 54].

A complete equivalent circuit of the planar transformer with parasitic parameters and winding resistance is illustrated in Fig. 2.8. R_p and R_s are the resistances of primary and secondary windings, L_{k1} and L_{k2} are the leakage inductance on primary and secondary side, L_m is the magnetizing inductance, C_p and C_s are the intra-winding capacitance of primary and secondary windings, and C_{ps} is the inter-winding capacitance.

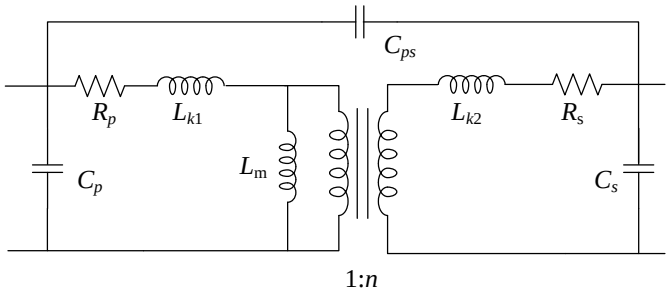


Fig. 2.8. Equivalent circuit of the planar transformer model.

In most applications, small stray capacitance is desired. The inter- and intra-winding capacitance can be reduced by decreasing overlapping area and/or increasing distance between two layers. However, this will reduce the window utilization factor and increase winding DC resistance. Different insulation thickness (h_Δ) can be applied between layers to tune the capacitance value. In some transformer designs, zero voltage gradient is applied between two paralleled layers, thus these layers can be placed very close to each other without generate any intra-winding capacitance [53]. Additionally, reducing the interleaving level between primary and secondary windings can decrease the inter-winding capacitance but increase intra-winding capacitance.

2.4. SUMMARY

This chapter gives an overview of planar transformer. The advantage and disadvantage of planar transformer are discussed. The most commonly used core material, core geometry and winding structures are presented. Transformer losses and parasitic parameters, including core loss, copper loss, leakage inductance and stray capacitance are discussed.

Chapter 3
THREE-PHASE DUAL ACTIVE BRIDGE CONVERTER

3.1. BASIC CONFIGURATION

The basic configuration of a three-phase DAB converter is depicted in Fig. 3.1 [14]. A three-phase high frequency transformer with turn ratio n is connected between the AC link of two three-phase active bridges to provide galvanic isolation and enable bidirectional power flow.

In smart home application, the primary side is connected with LV battery pack, and the secondary side is the HV DC link, which is connected to the grid through a DC/AC inverter. Three symmetrical auxillary inductors (corresponding to the leakage inductance L_k) are usually connected on the HV side to enable power transfer between the primary and secondary side.

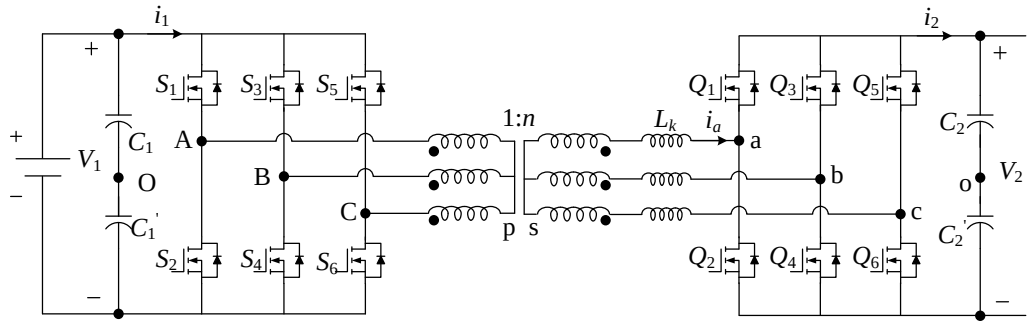


Fig. 3.1. Basic configuration of three-phase DAB converter.

3.2. OPERATING SCHEME

Phase shift modulation is the commonly used control strategy for DAB converter, and it has good performance at nominal operating condition. However, due to voltage variation of LV batteries, the voltage ratio between primary and secondary side may not match the transformer turn ratio. In that case, hard switching may occur and significantly increase the switching losses. For single-phase DAB converter, advanced modulation strategies [16 - 19, 55, 56] have been proposed to improve the overall efficiency. However, for three-phase DAB converter, due to fixed phase shift (120°) angle between phases, the advanced modulations are not applicable.

During operation, the switches in one phase leg are driven by complementary signals with 50% duty cycle, and the three half bridges are operated with 120° phase shift. Subtracting the square waveform v_{AO} or v_{ao} by the zero-sequence voltage v_{pO} or v_{so} in Fig. 3.1, the phase voltage of the transformer is derived. As shown in Fig. 3.2, six-step line-to-neutral voltage waveforms are imposed on both side of the transformer, where v_{Ap}' is referred to the HV side.

A phase shift angle ϕ is applied between primary and secondary voltage, and the voltage difference across L_k is generated. The waveforms of the other two phases are identical with 120° phase delay.

For power transfer from primary to secondary side ($P > 0$), the relationship between the phase shift and transmitted power is given as (3.1) [22]. For reverse power flow ($P < 0$), the operating waveforms are symmetrical but the primary side is delayed with respect to secondary side, i.e., $\phi < 0$ is applied [57, 58].

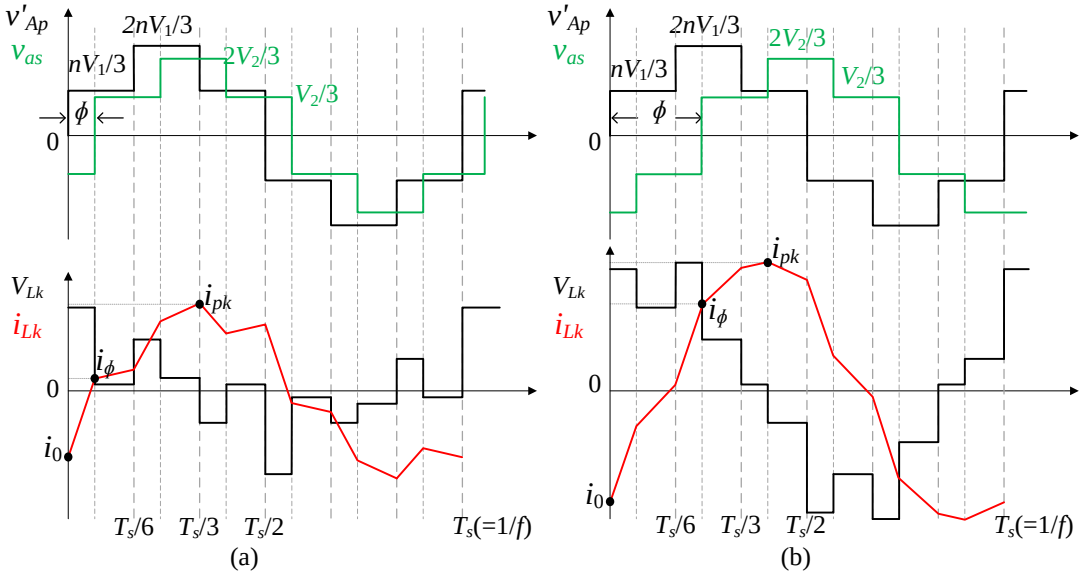


Fig. 3.2. Operating waveforms of three-phase DAB converter (a) $\phi \le \pi/3$ (b) $\phi > \pi/3$.

$$P = \begin{cases} \dfrac{nV_1V_2}{12\pi^2 fL_k} \cdot \phi(4\pi - 3\phi) & 0 \le \phi \le \dfrac{\pi}{3} \\ \dfrac{nV_1V_2}{36\pi^2 fL_k} \cdot (18\phi^2 - 18\pi\phi + \pi^2) & \dfrac{\pi}{3} < \phi \le \dfrac{2\pi}{3} \end{cases} \tag{3.1}$$

where, f is the switching frequency, n is the transformer turn ratio, V_1 and V_2 are the DC voltage of primary and secondary side, respectively.

As shown in (3.1), when $0 < \phi \le \pi/3$, the output power increases monotonically with phase shift ϕ; when $\pi/3 < \phi \le 2\pi/3$, the output power first increases with ϕ and reaches its maximum at $\phi = \pi/2$, and then decreases after $\phi > \pi/2$. $\phi > \pi/2$ is not adopted since it leads to increased reactive power and higher RMS current. Therefore, for a desired transmission power P, the phase shift ϕ can be calculated as (3.2).

$$\phi = \begin{cases} \frac{2\pi}{3}\left(1-\sqrt{1-\frac{9fL_kP}{nV_1V_2}}\right) & 0 \le P \le P_{\max 1} \\ \frac{\pi}{6}\left(3-\sqrt{7-\frac{72fL_kP}{nV_1V_2}}\right) & P_{\max 1} < P \le P_{\max 2} \end{cases} \tag{3.2}$$

where, $P_{\max 1}$ (= $nV_1V_2/12fL_k$) is achieved at $\phi = \pi/3$, and $P_{\max 2}$ (= $7nV_1V_2/72fL_k$) is achieved at $\phi = \pi/2$.

3.3. ZERO-VOLTAGE-SWITCHING CONDITION

The turn-on currents of the switches on the primary and secondary side are indicated in Fig. 3.2 as i_0 and i_ϕ. ZVS turn-on can be achieved when the body diode of the switch is conducting before turned on, and thus the voltage across the switch is nearly zero. The sufficient constraints for ZVS turn-on are derived as: negative current i_0 for primary bridges and positive current i_ϕ for secondary bridges [58].

$$\begin{aligned} i_0 &= \begin{cases} \frac{2(V_2 - nV_1) - 3V_2\phi/\pi}{18fL_k} \le 0 & 0 \le P \le \mathrm{P}_{\max 1} \\ \frac{(3V_2 - 2nV_1) - 6V_2\phi/\pi}{18fL_k} \le 0 & \mathrm{P}_{\max 1} < P \le \mathrm{P}_{\max 2} \end{cases} \\ i_\phi &= \begin{cases} \frac{2(V_2 - nV_1) + 3nV_1\phi/\pi}{18fL_k} \ge 0 & 0 \le P \le \mathrm{P}_{\max 1} \\ \frac{(2V_2 - 3nV_1) + 6nV_1\phi/\pi}{18fL_k} \ge 0 & \mathrm{P}_{\max 1} < P \le \mathrm{P}_{\max 2} \end{cases} \end{aligned} \tag{3.3}$$

3.4. SWITCH AND CAPACITOR CURRENT STRESS

The expression of the piecewise current i_{Lk} is derived from the voltage across the leakage inductance v_{Lk} [14]. The peak current of switches and transformers in Fig. 3.2 can be derived as

$$i_{pk}=\begin{cases}\begin{cases}\dfrac{V_2-nV_1+6nV_1\phi/\pi}{18fL_k} & nV_1\le V_2\\ \dfrac{nV_1-V_2+6V_2\phi/\pi}{18fL_k} & nV_1>V_2\end{cases} & 0\le\phi\le\dfrac{\pi}{3}\\ \begin{cases}\dfrac{nV_1+3V_2\phi/\pi}{18fL_k} & nV_1\le V_2\\ \dfrac{V_2+3nV_1\phi/\pi}{18fL_k} & nV_1>V_2\end{cases} & \dfrac{\pi}{3}<\phi\le\dfrac{2\pi}{3}\end{cases} \tag{3.4}$$

Similarly, the RMS current flowing through the leakage inductor I_{rms_Lk} can be obtained by integrating the current square in one switching period.

$$I_{rms\_Lk}=\begin{cases}\dfrac{\sqrt{-9nV_1V_2\phi^3+18\pi nV_1V_2\phi^2+5\pi^3(nV_1-V_2)^2/3}}{18fL_k\pi^{3/2}} & 0\le\phi\le\dfrac{\pi}{3}\\ \dfrac{\sqrt{nV_1V_2(-18\phi^3+27\pi\phi^2-3\pi^2\phi)+\pi^3(5n^2V_1^2/3+5V_2^2/3-3nV_1V_2)}}{18fL_k\pi^{3/2}} & \dfrac{\pi}{3}<\phi\le\dfrac{2\pi}{3}\end{cases} \tag{3.5}$$

Corresponding to Fig. 3.2 (a), the current flowing through the upper switches S_1, S_3 and S_5 on the primary side are depicted in Fig. 3.3. Because the switches conduct half of the switching period, the RMS current through switches I_{rms_sw} can be calculated by (3.6).

$$I_{rms\_sw}=I_{rms\_Lk}/\sqrt{2} \tag{3.6}$$

The input current i_1 in Fig. 3.1 is obtained by combining the current of the three upper switches, which is also shown in Fig. 3.3. The output current i_2 can be obtained

similarly by adding the current flowing through the upper switches on the secondary side (Q_1, Q_3 and Q_5). The RMS value of i_1 and i_2 is expressed by (3.7) [22].

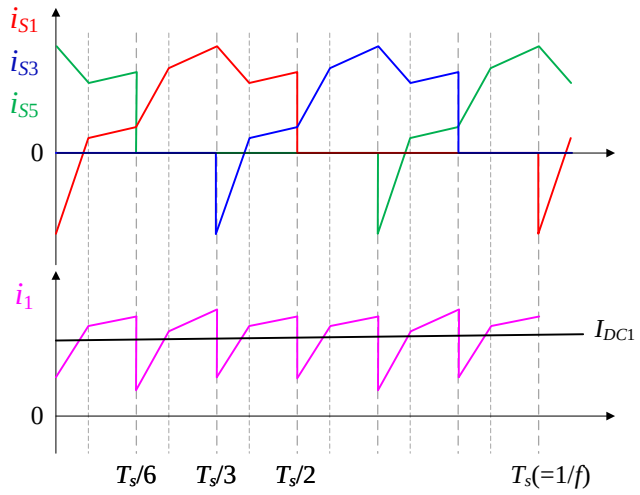


Fig. 3.3. Input current and current through switches.

$$I_{rms1}=\begin{cases}\dfrac{n}{18fL_k}\sqrt{\begin{matrix}-9V_2(2nV_1+3V_2)\cdot(\phi/\pi)^3\\+9V_2(nV_1+3V_2)\cdot(\phi/\pi)^2+(nV_1-V_2)^2/3\end{matrix}} & 0\le\phi\le\dfrac{\pi}{3}\\ \dfrac{n}{18fL_k}\sqrt{\begin{matrix}-36nV_1V_2\cdot(\phi/\pi)^3+27V_2(2nV_1-V_2)\cdot(\phi/\pi)^2\\+3V_2(9V_2-8nV_1)\cdot(\phi/\pi)+(n^2V_1^2+9nV_1V_2-11V_2^2)/3\end{matrix}} & \dfrac{\pi}{3}<\phi\le\dfrac{2\pi}{3}\end{cases}$$

$$I_{rms2}=\begin{cases}\dfrac{1}{18fL_k}\sqrt{\begin{matrix}-9nV_1(3nV_1+2V_2)\cdot(\phi/\pi)^3\\+9nV_1(3nV_1+V_2)\cdot(\phi/\pi)^2+(nV_1-V_2)^2/3\end{matrix}} & 0\le\phi\le\dfrac{\pi}{3}\\ \dfrac{1}{18fL_k}\sqrt{\begin{matrix}-36nV_1V_2\cdot(\phi/\pi)^3+27nV_1(nV_1-2V_2)\cdot(\phi/\pi)^2\\+3nV_1(9nV_1-8V_2)\cdot(\phi/\pi)+(V_2^2+9nV_1V_2-11n^2V_2^2)/3\end{matrix}} & \dfrac{\pi}{3}<\phi\le\dfrac{2\pi}{3}\end{cases} \quad (3.7)$$

Substituting the RMS value in (3.7) with their DC components, $I_{DC1} = P/V_1$ (input current) and $I_{DC2} = P/V_2$ (output current), the RMS value of the ripple current through the DC capacitors C_1 and C_2 can be obtained by (3.8).

$$I_{rms\_c1}=\sqrt{I_{rms1}^2-I_{DC1}^2},\ I_{rms\_c2}=\sqrt{I_{rms2}^2-I_{DC2}^2} \quad (3.8)$$

3.5. SUMMARY

This chapter presents the basic configuration and operating principles of the three-phase DAB converter. The sufficient conditions of ZVS turn-on is analyzed and presented. The closed form of the peak and RMS current of both switches and the DC capacitors are also obtained.

Chapter 4
THREE-PHASE DUAL ACTIVE BRIDGE CONVERTER DESIGN CONSIDERATIONS

4.1. KEY INFLUENCE OF TURN RATIO

The analysis of three-phase DAB converter in (3.1) – (3.8) indicates that the parameters f and L_k together influence the characteristics of the converter. To simplify the analysis, a new parameter fL is defined here in (4.1). Based on this, the impacts of parameters n and fL on the ZVS boundary, RMS current and ripple current through DC capacitor are studied respectively.

$$fL = f \cdot L_k / fL_{base} \tag{4.1}$$

where, $fL_{base} = 7n_{\max}V_{1\min}V_2/72P_N$, $n_{\max}$ = 10, $V_{1\min}$ = 40 V and V_2 = 400 V.

Due to the voltage variation of LV batteries, the performance of the converter under a wide voltage range and different power ratings need to be considered. To reduce computation efforts, 9 different LV side voltages, and 2 different output power levels (full load and half load) are chosen to represent different operating conditions.

$$\vec{V_1} = [40,\ 42,\ 44,\ 46,\ 48,\ 50,\ 52,\ 54,\ 56]^T \text{ V}, V_2 = 400 \text{ V}, P = [5,\ 10]^T \text{ kW}$$

4.1.1. Zero-Voltage-Switching Boundary

At full load, ZVS is desired at any voltage level of V_1. In order to find the worst input voltage that limits the ZVS range, the maximum value of i_0 and minimum value of i_ϕ need

to be considered. By substituting (3.2) into (3.3), the derivative of i_0 and i_ϕ with respect to V_1 can be obtained.

$$\frac{\partial i_0}{\partial V_1}=\begin{cases} n\cdot\dfrac{3\,fLP/(nV_1)^2-2\sqrt{1-9\,fLP/nV_1V_2}\,/3}{6\,fL\cdot\sqrt{1-9\,fLP/nV_1V_2}}<0 & 0\le P\le \mathrm{P}_{\max 1} \\ n\cdot\dfrac{12\,fLP/(nV_1)^2-2\sqrt{7-72\,fLP/nV_1V_2}\,/3}{6\,fL\cdot\sqrt{7-72\,fLP/nV_1V_2}}>0 & \mathrm{P}_{\max 1}<P\le \mathrm{P}_{\max 2} \end{cases}$$
$$\frac{\partial i_\phi}{\partial V_1}=\begin{cases} -\dfrac{n\cdot(2-9\,fLP/nV_1V_2)}{18\,fL\cdot\sqrt{1-9\,fLP/nV_1V_2}}<0 & 0\le P\le \mathrm{P}_{\max 1} \\ -\dfrac{n\cdot(7-36\,fLP/nV_1V_2)}{18\,fL\cdot\sqrt{7-72\,fLP/nV_1V_2}}<0 & \mathrm{P}_{\max 1}<P\le \mathrm{P}_{\max 2} \end{cases} \quad (4.2)$$

From (4.2), when $P \le \mathrm{P}_{\max 1}$, i_0 decreases monotonically with V_1, and the maximum value of i_0 happens at $V_{1\min}$ (= 40 V); i_ϕ decreases with V_1, and the minimum value of i_ϕ happens at $V_{1\max}$ (= 56 V). If the converter operates at $\pi/3 < \phi \le \pi/2$, i.e., $\mathrm{P}_{\max 1} < P \le \mathrm{P}_{\max 2}$, i_0 increases with V_1, and $i_{0\max}$ will happen at $V_{1\max}$; i_ϕ keeps decreasing with V_1, and $i_{\phi\min}$ happens at $V_{1\max}$.

The converter only operates at $\pi/3 < \phi \le \pi/2$ when V_1 is lower. In most input voltages when V_1 is higher, the converter operates at $\phi \le \pi/3$. Thus $i_{0\max}$ can be considered happening at $V_{1\min}$, and $i_{\phi\min}$ happens at $V_{1\max}$. A visualized solution is shown in Fig. 4.1 by solving the ZVS condition at different input voltages at full load.

The feasible range of n and fL which guarantees ZVS at maximum power is highlighted in Fig. 4.1. At higher V_1 and turn ratio n, the LV side ZVS limit (solid line) has a wider range. At lower V_1 and turn ratio n, the HV side ZVS limit (dashed line) features wider range. The applicable value of turn ratio is 7, 8, 9, and n = 8 provides wider range of fL compared to n = 7 and 9.

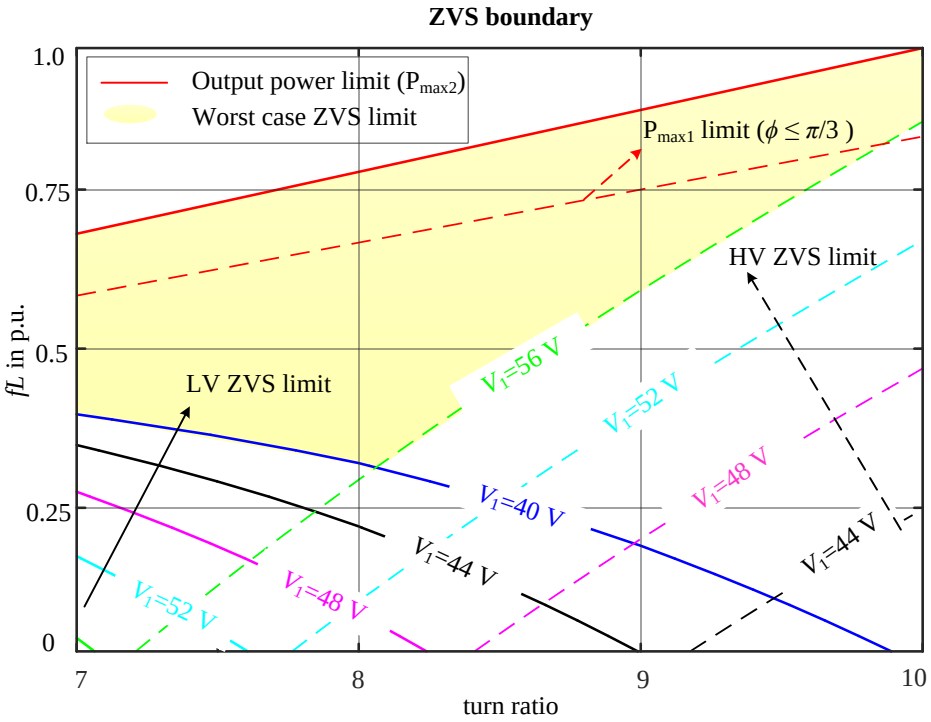


Fig. 4.1. LV and HV ZVS boundary at different V_1.

4.1.2. RMS Current

If ZVS is achieved, conduction loss of the switches dominates the total converter losses and the conduction loss is proportional to the square of the RMS current through switches/transformer. Therefore, the characteristics of RMS current versus n and fL under different voltage level of V_1 are studied. A weighted sum of the RMS current at different input voltages is used to study the variation of conduction loss, where the weight factor α_i depends on the importance of each operating voltage [59].When equivalent weight factor is applied, the weighted sum of RMS current becomes average RMS current.

$$\overline{I_{rms\_sw}} = \sum_i \alpha_i I_{rmsi} \quad (\sum_i \alpha_i = 1) \tag{4.3}$$

Under different *n* and *fL*, the average RMS current of switches is demonstrated in Fig. 4.2. At fixed turn ratio *n*, as *fL* increases, the average RMS current first decreases and reaches its minimum; but as *fL* further approaches its maximum, which is limited by the maximum output power, the RMS current increases again. At fixed *fL*, the averaged RMS current is lower at larger turn ratio *n*.

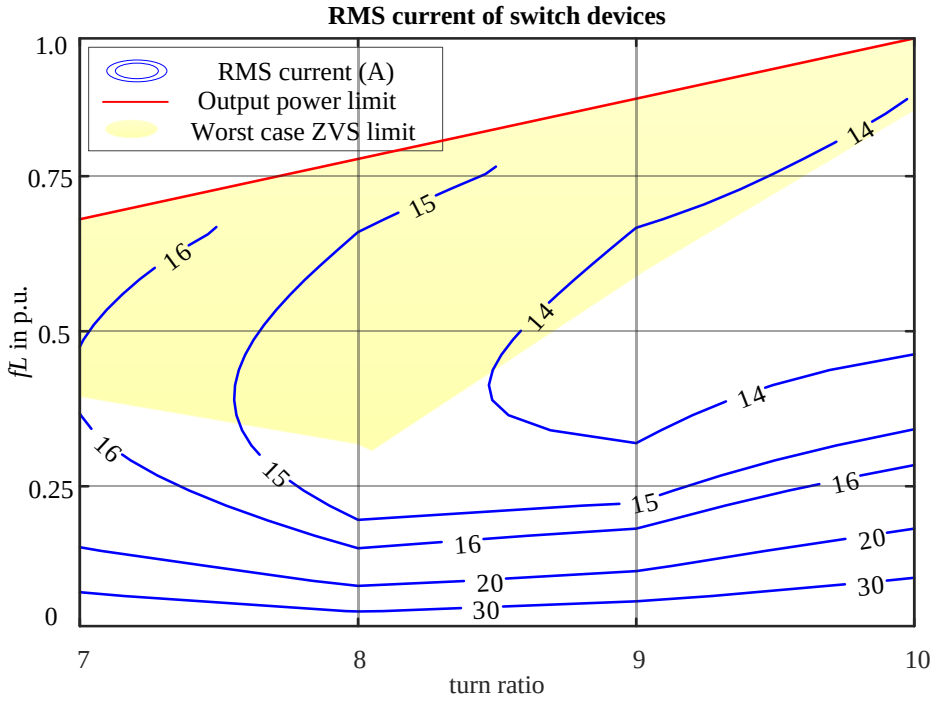


Fig. 4.2. Averaged RMS current at different *n* and *fL* under full load.

4.1.3. Ripple Current of DC Link Capacitor

The DC link capacitor smooths the voltage on DC link and absorbs the ripple current. The design of the capacitor is based on the maximum ripple current at all input voltages. From 3.2.3, the closed form of I_{rms_c1} and I_{rms_c2} as well as their partial derivative with respect to V_1 is very complex. For given values of *n* and *fL*, the maximum ripple current

on both LV and HV side are computed under different input voltage levels. The results are depicted in Fig. 4.3.

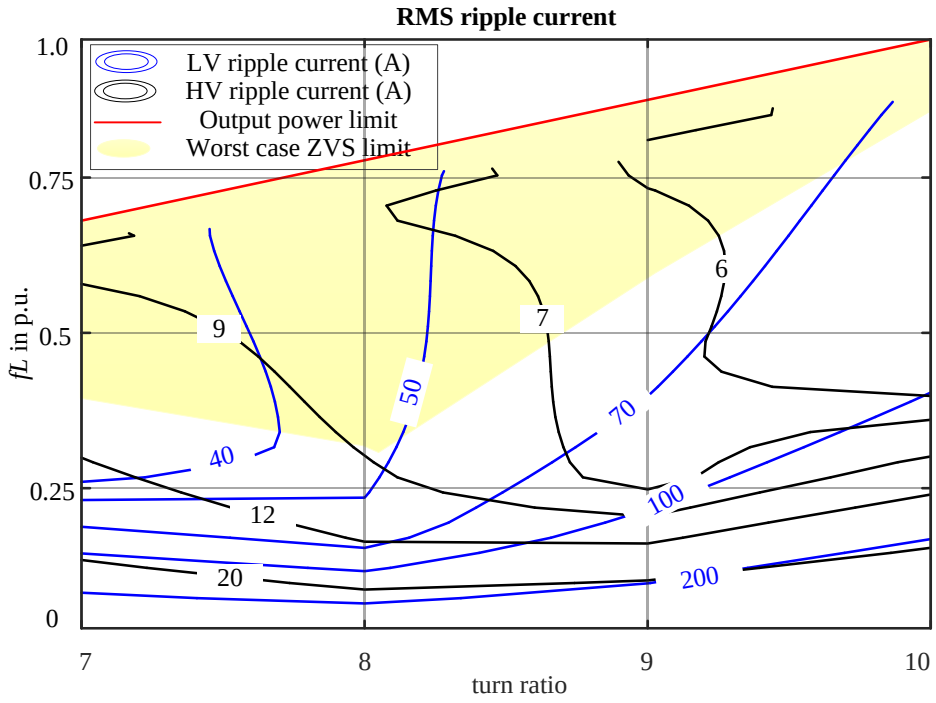


Fig. 4.3. Worst case LV and HV ripple current at different *n* and *fL*.

For a fixed turn ratio *n*, the ripple current on both side decreases as *fL* increases, and reaches its minimum when *fL* approaches its maximum. Within the ZVS area, when $n = 7$, lower ripple current is achieved on LV side; when $n = 9$, lower ripple current is achieved on the HV side.

In summary, wider HV side ZVS range and lower LV side capacitor ripple current are achieved at lower turn ratio ($n = 7$); on the contrary, wider LV side ZVS range and lower HV side ripple current are achieved at higher turn ratio ($n = 9$). In addition, higher turn ratio *n* leads to relatively lower RMS current in the switches and transformer, and vice versa.

4.2. EFFECTIVE OPERATING AREA OF FREQUENCY AND LEAKAGE INDUCTANCE

At fixed turn ratio *n*, with the constraints of converter power capability and feasible transformer design, the effective operating area (EOA) defines the feasible range of switching frequency *f* and leakage inductance L_k.

4.2.1. Effective Operating Area Limited by Transmission Power

The maximum output power $P_{\max 2}$ has to be higher than the power rating of the converter P_N. This power requirement should be fulfilled at any input voltage level, thus the upper limit of fL is specified by lowest V_1.

$$f \cdot L_k \le \frac{7 \cdot n \cdot V_{1\min} V_2}{72 P_N} \tag{4.4}$$

Regarding to different turn ratio, the power constraint are depicted in Fig. 4.4 as red hyperbolic curves. The feasible range of f and L_k that meets the power requirement is located on the left side of the power constraint curve.

4.2.2. Effective Operating Area Limited by Transformer Design

With the specified magnetic core, the EOA is further constrained by the allowable flux density, the power loss density of the core, and the feasible winding structure design that fits into the core window area. The constraints are given in (4.5) - (4.7).

$$B_m = \frac{V_1}{9 f A_e} \le B_{\max} \tag{4.5}$$

$$p_v = K B_m^{\alpha} f^{\beta} \le p_{v\max} \tag{4.6}$$

$$A_s = \frac{I_{rms\_tf}}{J} \le A_w \cdot K_u / 2 \tag{4.7}$$

where A_w and A_e are the core window area and effective area, as shown in Fig. 5.3, A_s is the cross section of the designed winding. Details of transformer design will be explained in Chapter 5.

Because the leakage inductors are connected to the HV side, LV side voltage waveforms will be applied on flux density and power loss density constraints. The EOA of the converter at different turn ratio are illustrated in Fig. 4.4 as the shaded area. It is observed that the constraints of flux density and core loss density are at the same level for different values of n. The winding design constraint and output power constraint change with the turn ratio.

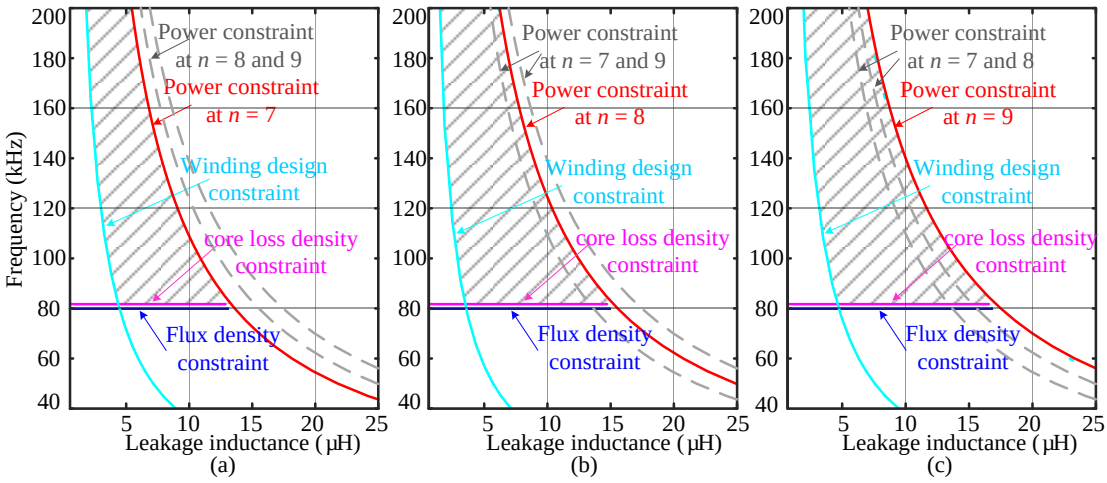


Fig. 4.4. EOA limited by transmission power and transformer design at (a) n = 7, (b) n = 8 and (c) n = 9.

4.2.3. Switch and Capacitor Current Analysis

The peak and RMS current of the switches are investigated under 9 different input voltages at full load. The highest current among the 9 input voltages is selected to represent the current stress of the switches, and the results are shown in Fig. 4.5.

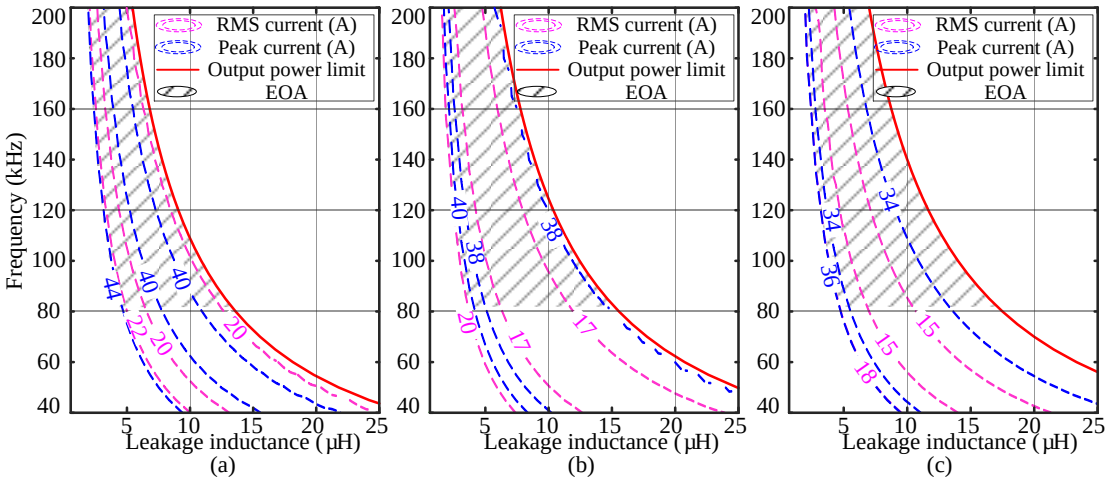


Fig. 4.5. Switches current stress analysis at (a) n = 7, (b) n = 8 and (c) n = 9.

Consistent with the analysis in 4.1.2, the peak and RMS current decreases with the increase of the product of f and L_k, and the minimum value is achieved when f and L_k are close to the power constraint curve. From Fig. 4.5, it is also observed that for lower turn ratio n, the peak current stress and RMS current is slightly higher.

By taking the maximum value of the ripple current among 9 input voltages at full load, the ripple current stress of the DC capacitor at different turn ratio are plotted in Fig. 4.6. Corresponding to Fig. 4.3, the LV and HV ripple current decreases when the product of f and L_k increases, and reaches their minimum as the value of f and L_k approaches the power constraint curve. Lower turn ratio leads to higher HV ripple current and lower LV ripple current and vice versa.

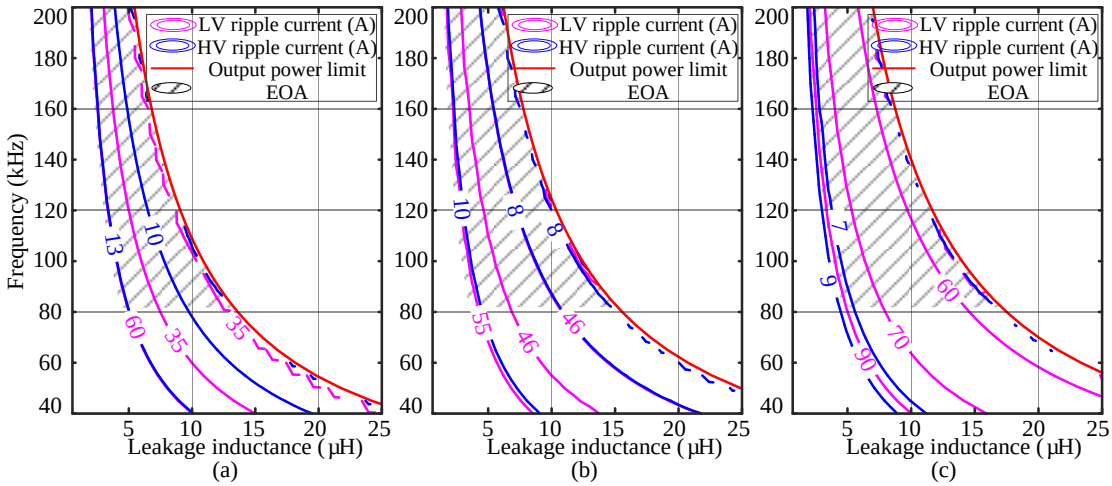
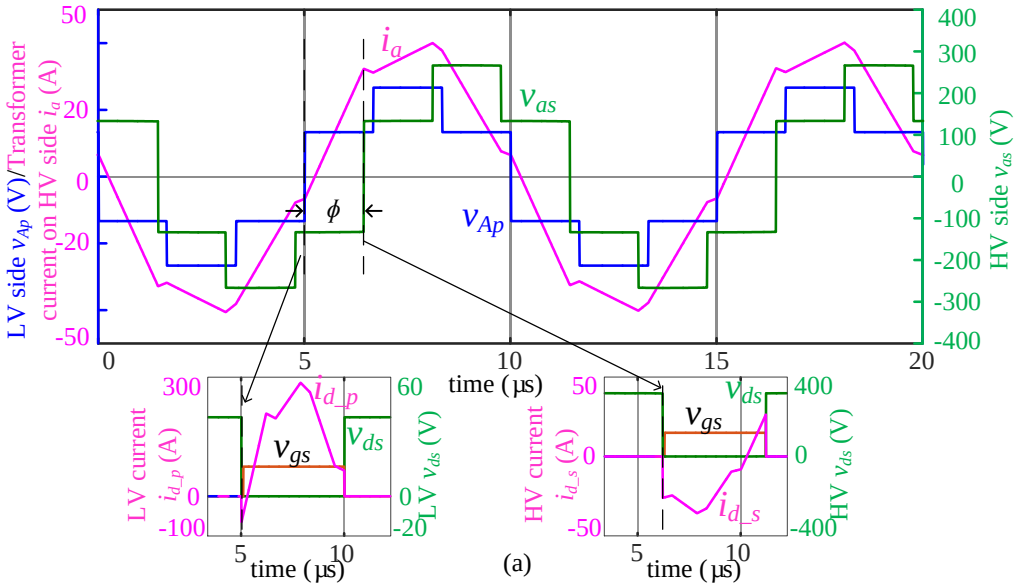


Fig. 4.6. Capacitor ripple current analysis at (a) n = 7, (b) n = 8 and (c) n = 9.

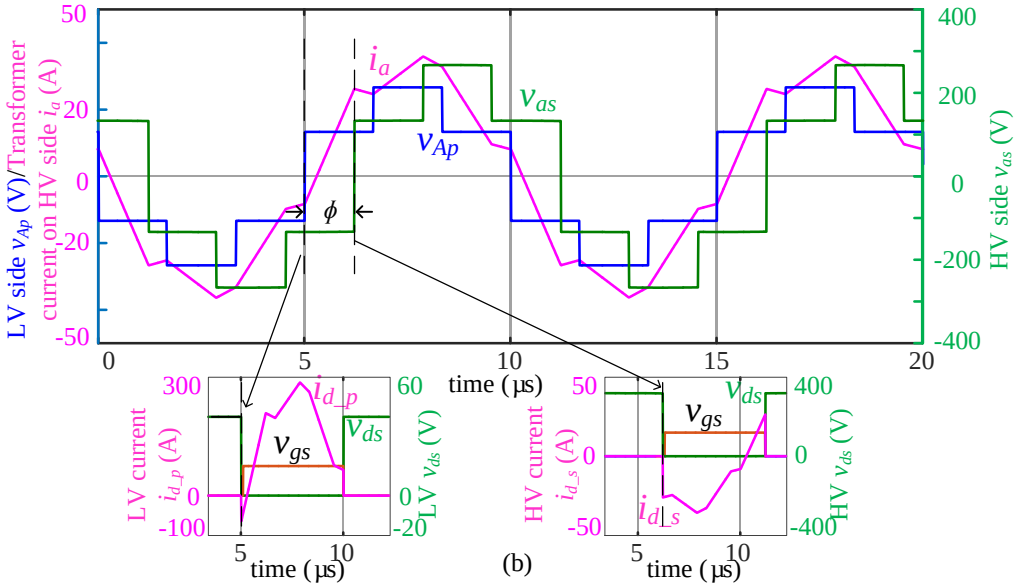
4.2.4. MATLAB/Simulink Verification

A three-phase DAB converter is built in MATLAB/Simulink to verify the analysis. Three different values of turn ratio n (= 7, 8, 9) and two different combinations of f and L_k (f = 100 kHz, L_k = 8 μH and f = 120 kHz, L_k = 4 μH) are selected to compare the impacts of the parameters on the converter performances. For different combinations of (n, f, L_k), the simulated voltage and current waveforms at full load are depicted in Fig. 4.7 and Fig. 4.8.

Fig. 4.7 depicts the operating waveforms at V_1 = 40 V with parameters f = 100 kHz and L_k = 8 μH. This parameter combination corresponds to fL = 0.5 *p.u.* in Fig. 4.1. The ZVS behavior is highlighted in each figure with the gate drive signal v_{gs}, voltage across the switches v_{ds} and the current i_d flowing through it. At the turn-on instant, the negative current flow indicates that ZVS is achieved on both side.


LV side v_{Ap} (V)/Transformer current on HV side i_a (A)
HV side v_{as} (V)
i_a
v_{as}
v_{Ap}
ϕ
time (μs)
LV current i_{d_p} (A)
LV v_{ds} (V)
i_{d_p}
v_{gs}
v_{ds}
HV current i_{d_s} (A)
HV v_{ds} (V)
i_{d_s}

(a)


LV side v_{Ap} (V)/Transformer current on HV side i_a (A)
HV side v_{as} (V)
i_a
v_{as}
v_{Ap}
ϕ
time (μs)
LV current i_{d_p} (A)
LV v_{ds} (V)
i_{d_p}
v_{gs}
v_{ds}
HV current i_{d_s} (A)
HV v_{ds} (V)
i_{d_s}

(b)

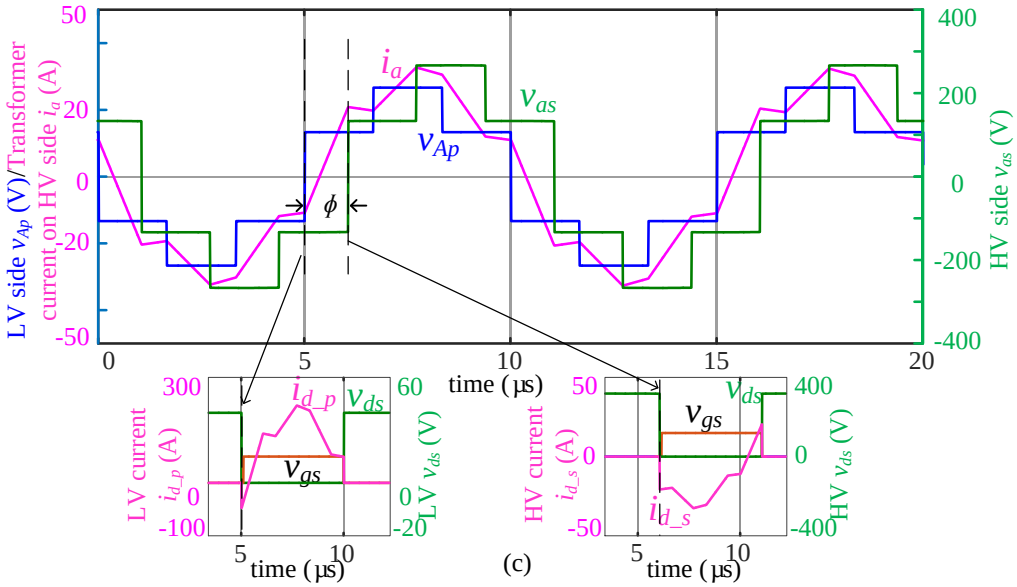
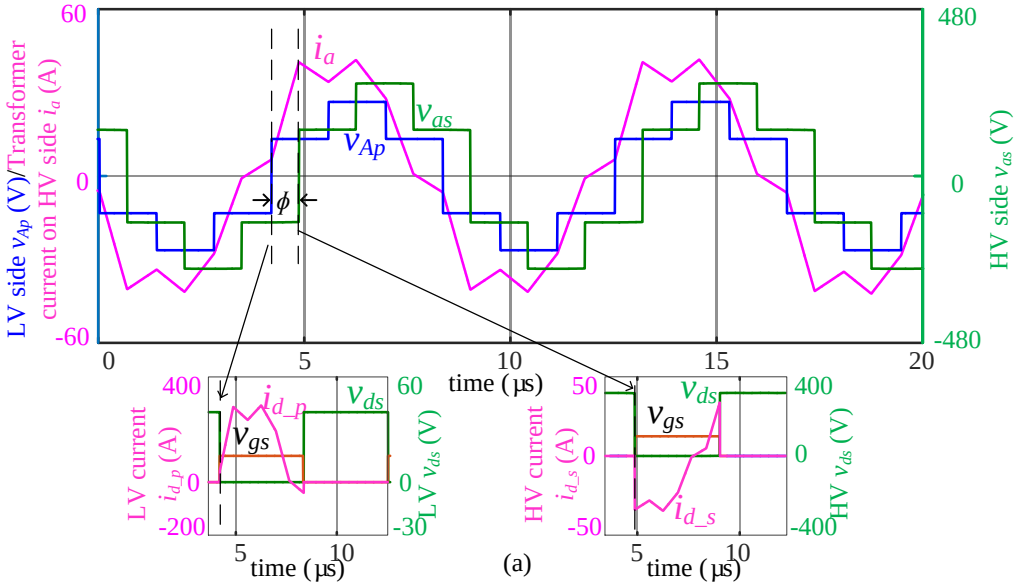


Fig. 4.7. Simulated voltage and current waveforms at (a) *n* =7, (b) *n* =8 and (c) *n* = 9 under 100kHz, 8 μH.

When the parameters are set as f = 120 kHz and L_k = 4 μH, the operating waveforms are shown in Fig. 4.8, which corresponds to fL = 0.3 *p.u.* in Fig. 4.1. Consistent with the analysis in 4.1.1, the positive current at the turn-on instant shows ZVS is not achieved on LV side when n = 7 and 8; and when n = 9, ZVS is not realized on HV side.



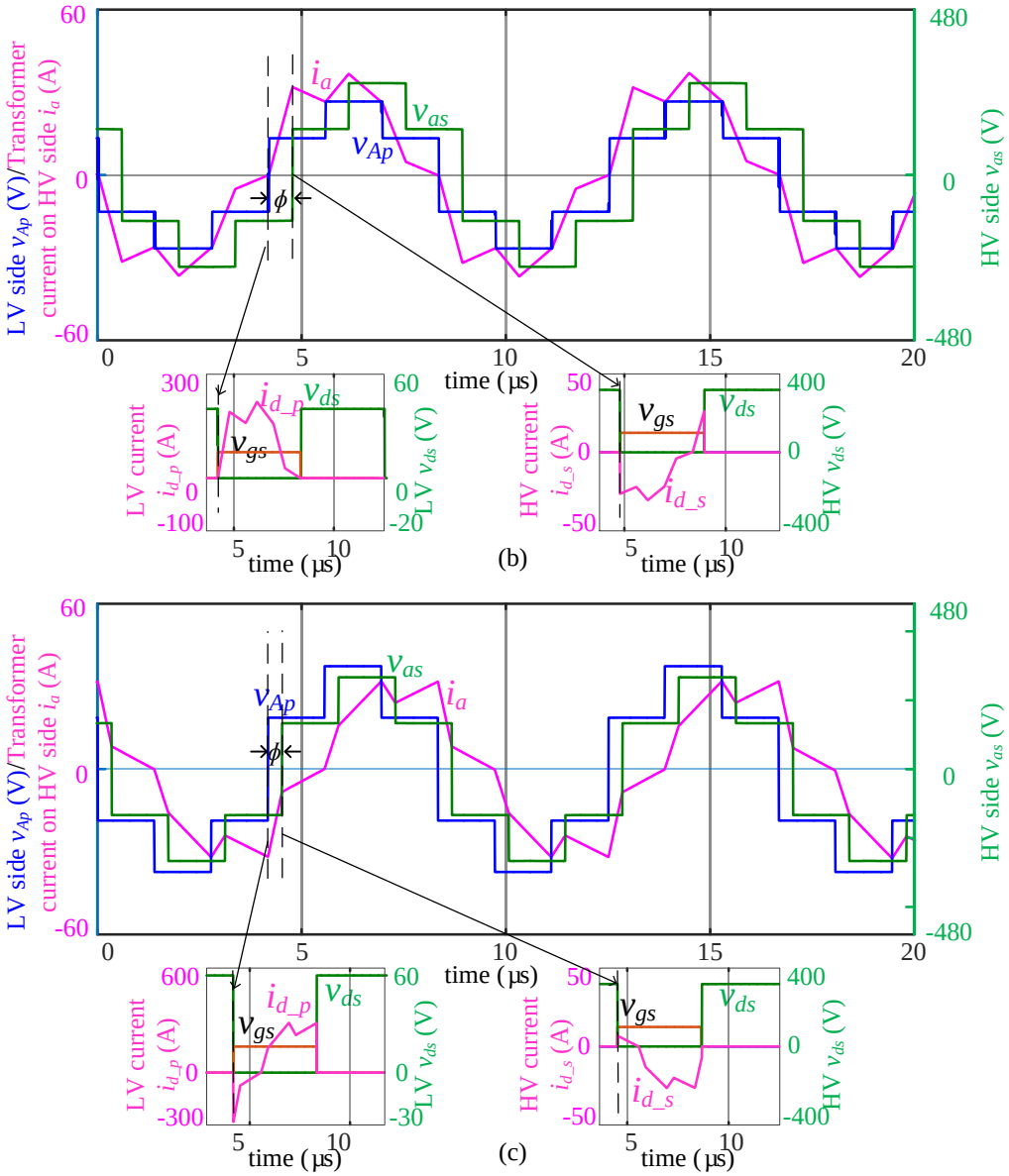


Fig. 4.8. Simulated voltage and current waveforms at (a) *n* =7, (b) *n* =8 and (c) *n* = 9 under 120kHz, 4 μH.

The peak and RMS current of the switches on LV and HV side from MATLAB simulations are summarized in Table 4.1. When f = 100 kHz and L_k = 8 μH, the current stress shows small increase when the turn ratio n decreases. When f = 120 kHz and L_k = 4 μH, significant current increase on the LV side is observed.

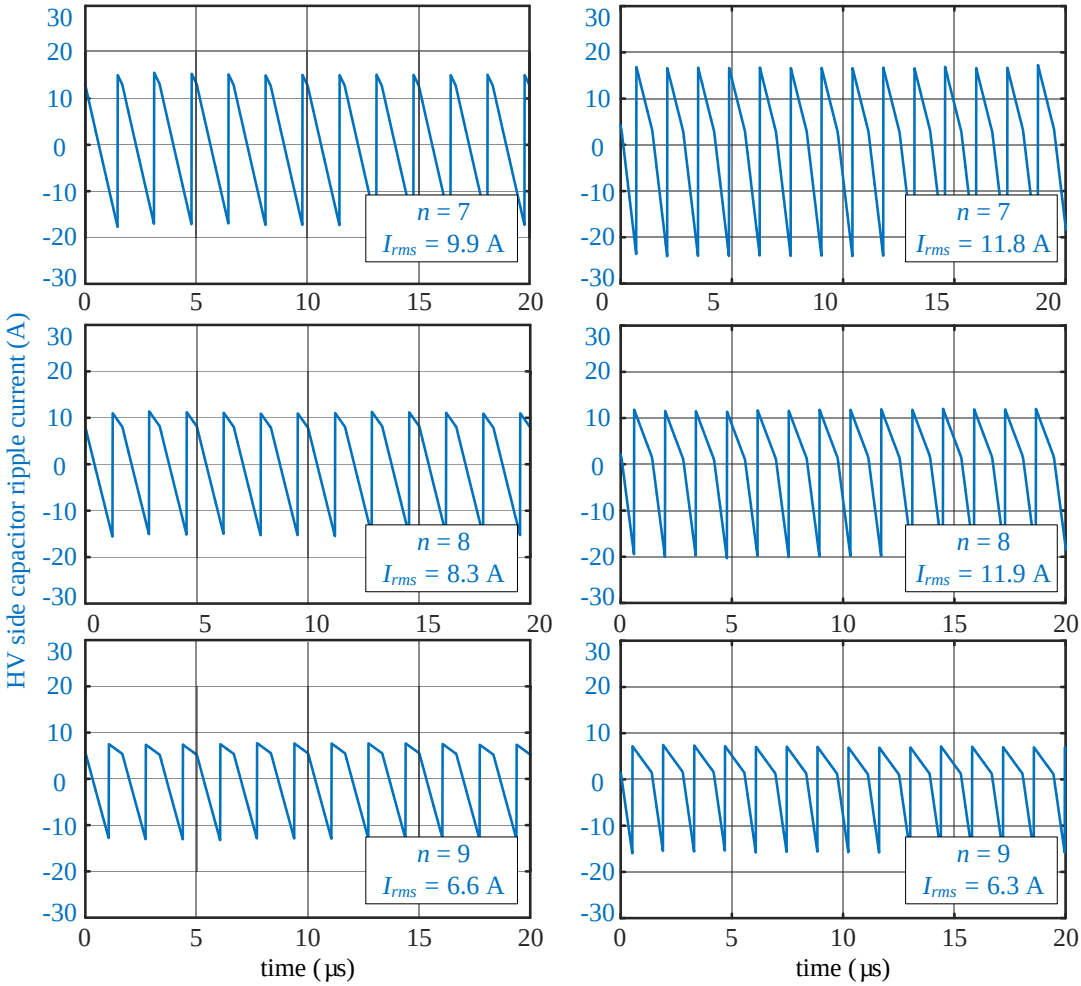
Table 4.1 Current stress of switches under different parameters

	Current stress of LV switches (A)				Current stress of HV switches (A)			
	100 kHz, 8 μH		120 kHz, 4 μH		100 kHz, 8 μH		120 kHz, 4 μH	
	Peak	RMS	Peak	RMS	Peak	RMS	Peak	RMS
n = 7	280	135	287	140	39.7	19.3	41.4	19.9
n = 8	289	134	374	153	35.5	16.8	46.9	19.2
n = 9	294	135	286	163	32.5	15	31.8	18.1

The capacitor ripple currents are also compared under different parameters. The capacitor current waveforms on HV side are shown in Fig. 4.9, corresponding to different parameter combinations. The RMS value of the ripple current on both side are shown in Table 4.2. Consistent with the analysis in 4.2.3, with fixed f and L_k, lower LV ripple current and higher HV ripple current are observed at lower turn ratio, and vice versa. When the parameter f = 120 kHz and L_k = 4 μH, higher ripple current is observed on both side compared to the parameter f = 100 kHz and L_k = 8 μH.

Table 4.2 Capacitor ripple current under different parameters

	LV side ripple current (A)		HV side ripple current (A)	
	100 kHz, 8 μH	120 kHz, 4 μH	100 kHz, 8 μH	120 kHz, 4 μH
n = 7	44	47	9.9	11.8
n = 8	51	73	8.3	11.9
n = 9	67	85	6.6	6.3



(a) f = 100 kHz, L_k = 8 μH (b) f = 120 kHz, L_k = 4 μH

Fig. 4.9. Ripple current of DC capacitors on HV side at different (n, f, L_k)

4.3. LOSS ANALYSIS

From the analysis above, trade-offs need to be made between ZVS range and ripple current on LV and HV side for the selection of turn ratio n. Higher turn ratio leads to lower HV ripple current and wider LV ZVS range. On the other hand, lower turn ratio results in lower LV ripple current and wider HV ZVS range. In addition, lower RMS current of switches is achieved at higher turn ratio. In this section, further investigation of

power losses and converter efficiency is carried out to determine the turn ratio n and values of f and L_k.

4.3.1. Power Loss of Switches

Conduction Loss

Conduction loss in power MOSFET can be calculated using the drain-source on-state resistance $R_{DS(on)}$ and the current i_D. By integrating the instantaneous power losses in one switching period, the averaged conduction loss can be obtained by (4.8) [60]. In this case, the conduction loss caused by the anti-paralleled body diode of the MOSFET is assumed to be small enough to be neglected.

$$P_{cond} = \frac{1}{T_s}\int_0^{T_s}\left(R_{DS(on)} \cdot i_D^2(t)\right)dt = R_{DS(on)} \cdot I_{rms\_sw}^2 \tag{4.8}$$

where I_{rms_sw} is obtained from (3.5) and (3.6).

Switching Loss

When the switches are not operated under ZVS condition, the switching loss cannot be neglected. The turn-on and turn-off losses in the MOSFET and its body diode can be calculated by linear approximation of the MOSFET switching process [60]. The turn-on energy is the sum of the energy during the current rise time t_{ri} and voltage fall time t_{fu}, as well as the energy caused by reverse-recovery of the body diode. Similarly, the turn-off energy is calculated using the voltage rise time t_{ru} and current fall time t_{fi}. The turn-off energy loss caused by diode is usually neglected.

$$\begin{aligned} E_{onM} &= E_{onMi} + E_{onMrr} = U_{DS} I_{Don} \cdot \frac{t_{ri} + t_{fu}}{2} + Q_{rr} U_{DS} \\ E_{offM} &= U_{DS} I_{Doff} \cdot \frac{t_{ru} + t_{fi}}{2} \\ E_{onD} &\approx E_{onDrr} = \frac{1}{4} Q_{rr} U_{DS} \end{aligned} \tag{4.9}$$

where, E_{onM} and E_{offM} are the turn-on and turn-off energy loss of the MOSFET, E_{onD} is the turn-on energy loss of the body diode, which is mostly the reverse recovery energy (E_{onDrr}), Q_{rr} is the reverse recovery charge of the diode, U_{DS} is the DC voltage, and I_{Don} and I_{Doff} are the turn-on and turn-off current at the switching instant, respectively.

The total switching loss of a MOSFET and its body diode are the product of the switching energies and switching frequency.

$$P_{sw} = (E_{onM} + E_{onD} + E_{offM}) \cdot f \tag{4.10}$$

At full load, the losses of the switches are calculated at 3 different voltage level of V_1: nominal input voltage (V_1 = 48 V), minimum input voltage (V_1 = 40 V) and maximum input voltage (V_1 = 56 V). At different turn ratio n, the conduction and switching losses are calculated and shown in Fig. 4.10. It has to be noted that although the RMS current is lower at n = 9, the conduction loss is not necessarily lower than n = 7 or 8. That's because on LV side, conduction loss is not only proportional to $I^2_{rms\_sw}$, but also proportional to n^2.

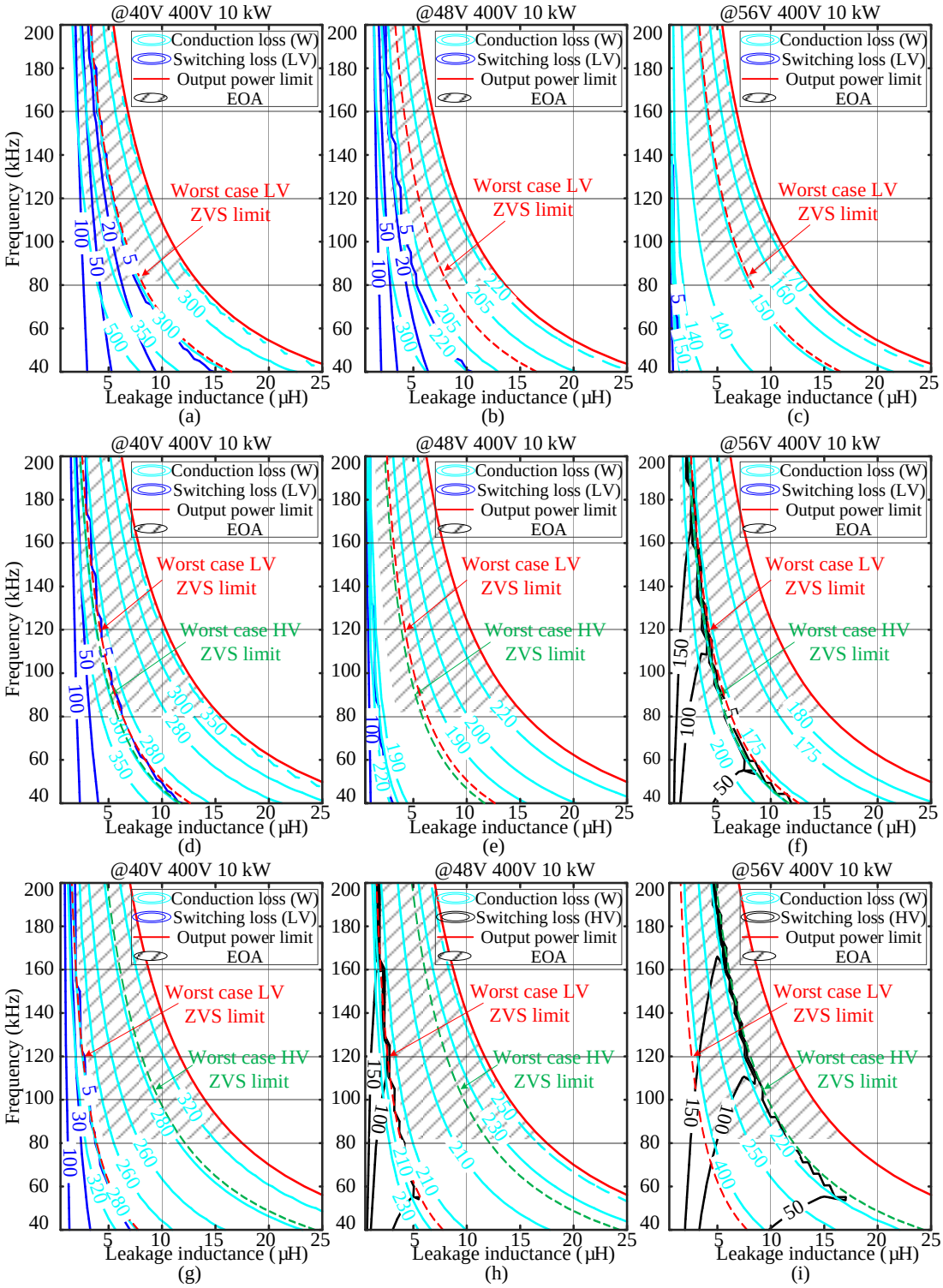


Fig. 4.10. Conduction and switching loss under different V_1 at (a, b, c) n = 7, (d, e, f) n = 8 and (g, h, i) n = 9.

The switching loss of LV and HV side are also depicted at different turn ratio in each figure. When at n = 7, ZVS operation can always be achieved on HV side, and hard switching happens on LV side at lower input voltage (V_1 = 40 V). When n = 9, ZVS operation is guaranteed on LV side within EOA; but switching loss exists on HV side at higher input voltage (V_1 = 56 V). When n = 8, hard switching happens in a small area of EOA, which can be avoided by choosing the value of f and L_k from the right side of ZVS limit curve. It is interesting to notice that the LV switching loss increases slowly as f and L_k moves away from the ZVS limit. On the other hand, the HV switching loss in (i) is dramatically higher and comparable with the conduction loss. Due to the significant high switching loss on HV side, it is obviously more important to achieve ZVS on the HV side.

4.3.2. Transformer Loss

The transformer core loss is calculated using the Steinmetz equation in (2.1) [42]. By substituting the flux density equation in (4.5) to Steinmetz equation, core loss density is obtained. The transformer core loss can be calculated by

$$P_{core} = 3 \cdot V_e \cdot p_v = 3 \cdot V_{core} \cdot K \frac{1}{f^{\beta-\alpha}} \left(\frac{V_1}{9A_e} \right)^{\beta} \tag{4.11}$$

where V_e is the volume of the transformer core. For a fixed design of transformer, because $\alpha < \beta$, the transformer core loss decreases when switching frequency increases.

The transformer copper loss can be calculated using its RMS current I_{rms_tf}.

$$P_{core} = 3 \cdot I_{rms\_tf}^2 \cdot R_{ac} \tag{4.12}$$

where R_{ac} is the AC resistance of the transformer winding with eddy current effect. The AC resistance varies with switching frequency, as described in 2.2.2.

The transformer total losses at nominal input voltage are illustrated in Fig. 4.11 with different turn ratio n. The core losses decrease as f increases, and they are independent of n. The copper losses are proportional to the AC resistance and square of RMS current. The total transformer losses increase as f decreases, and they are insensitive to changes in L_k or n. For different input voltages, the transformer losses share similar trends.

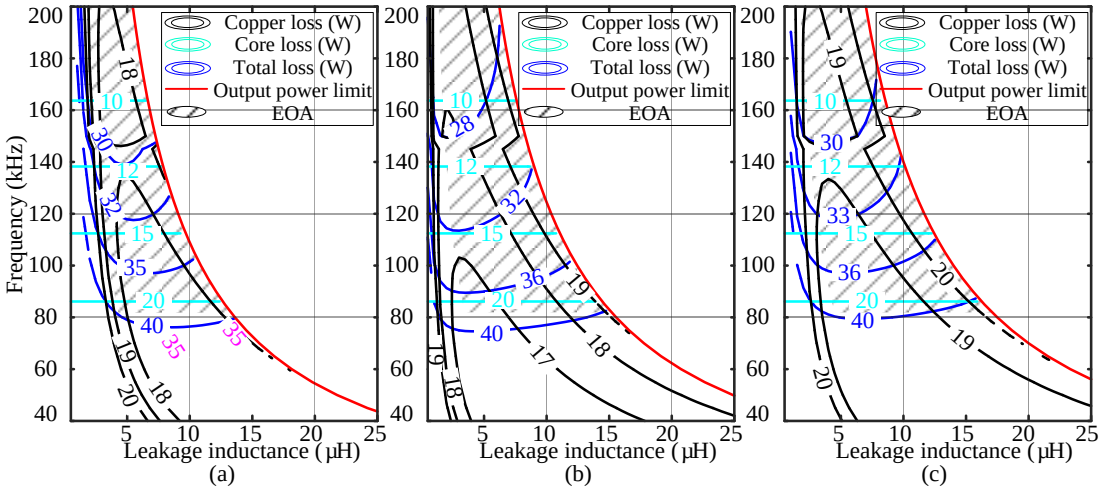


Fig. 4.11. Transformer losses under nominal operating voltage at (a) n = 7, (b) n = 8 and (c) n = 9.

4.4. CONVERTER EFFICIENCY

The losses variation with the design parameters (n, f, L_k) is the major concern, thus only losses on switches and transformers are considered. Other power losses such as the DSP controller, gate driver, components equivalent series resistance (ESR) and auxiliary inductor losses are very small and not included here. At different turn ratio, the converter

efficiency is calculated when it is fully loaded and half loaded, and they are plotted in Fig. 4.12 and Fig. 4.13 respectively.

When n = 7, at full load, the converter efficiency under different input voltages are depicted in Fig. 4.12 (a)-(c). The EOA can be divided into 2 sections by the LV ZVS boundary as well as the LV ripple current contour, and they are marked as zone **A1** and **A2**. In zone **A1**, both LV and HV ZVS are guaranteed. LV ripple current is lower than 35 A and HV ripple current is about 10 A. In zone **A2**, hard switching happens at LV side when V_1 is lower, and both LV and HV ripple current are higher (60 A and 13 A) compared to zone **A1**. Thus the converter efficiency is lower in zone **A2**.

At half load, same conclusion can be drawn from the efficiency analysis, which is shown in Fig. 4.13 (a)-(c). In zone **A1**, though hard switching occurs at LV side, the switching loss is quite small, and conduction loss dominates the converter total loss.

When n = 8, at full load, the converter efficiency at different input voltages are illustrated in Fig. 4.12 (d)-(f). The EOA is divided into 3 sections by the LV ripple current contour and ZVS limit curve: zone **B1**, **B2** and **B3**. ZVS is realized on both LV and HV side in zone **B1** and **B2**. In zone **B2**, lower LV ripple current (46 A) is obtained compared to zone **B1** (50 A), but the HV ripple current is slightly higher (> 8 A). Lowest RMS current is achieved in the area where f and L_k approach the power constraint curve, which makes the converter efficiency in zone **B2** higher than zone **B1**. In zone **B3**, the ripple current on both side are higher (55 A and 10 A), and ZVS cannot be guaranteed. The highest efficiency may happen at zone **B3** when ZVS can be achieved (see as Fig. 4.12 (e)). However, the efficiency gain is not significant.

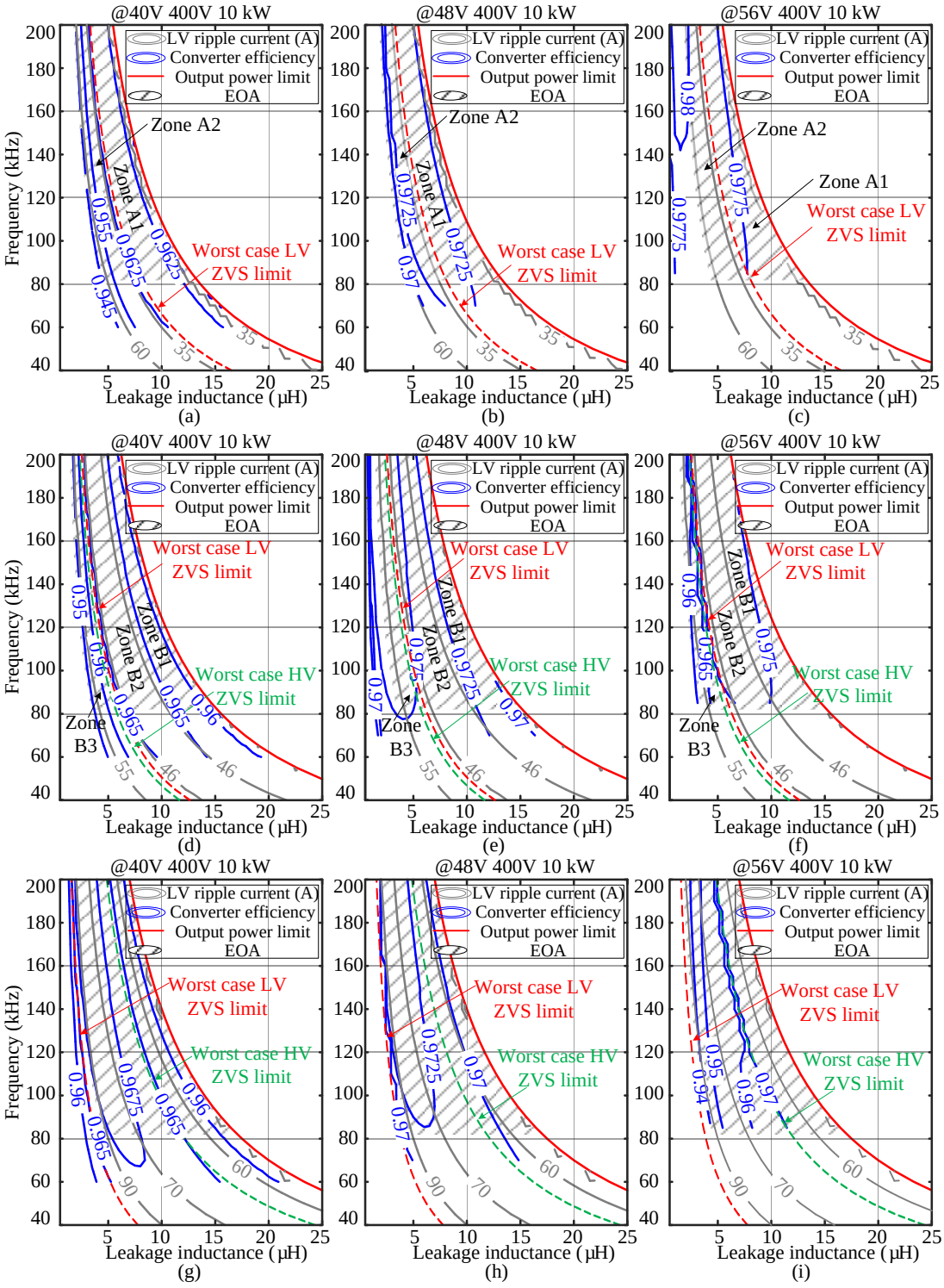


Fig. 4.12. Converter efficiency under full load at (a ~ c) *n* = 7, (d ~ f) *n* = 8 and (g ~ i) *n* = 9.

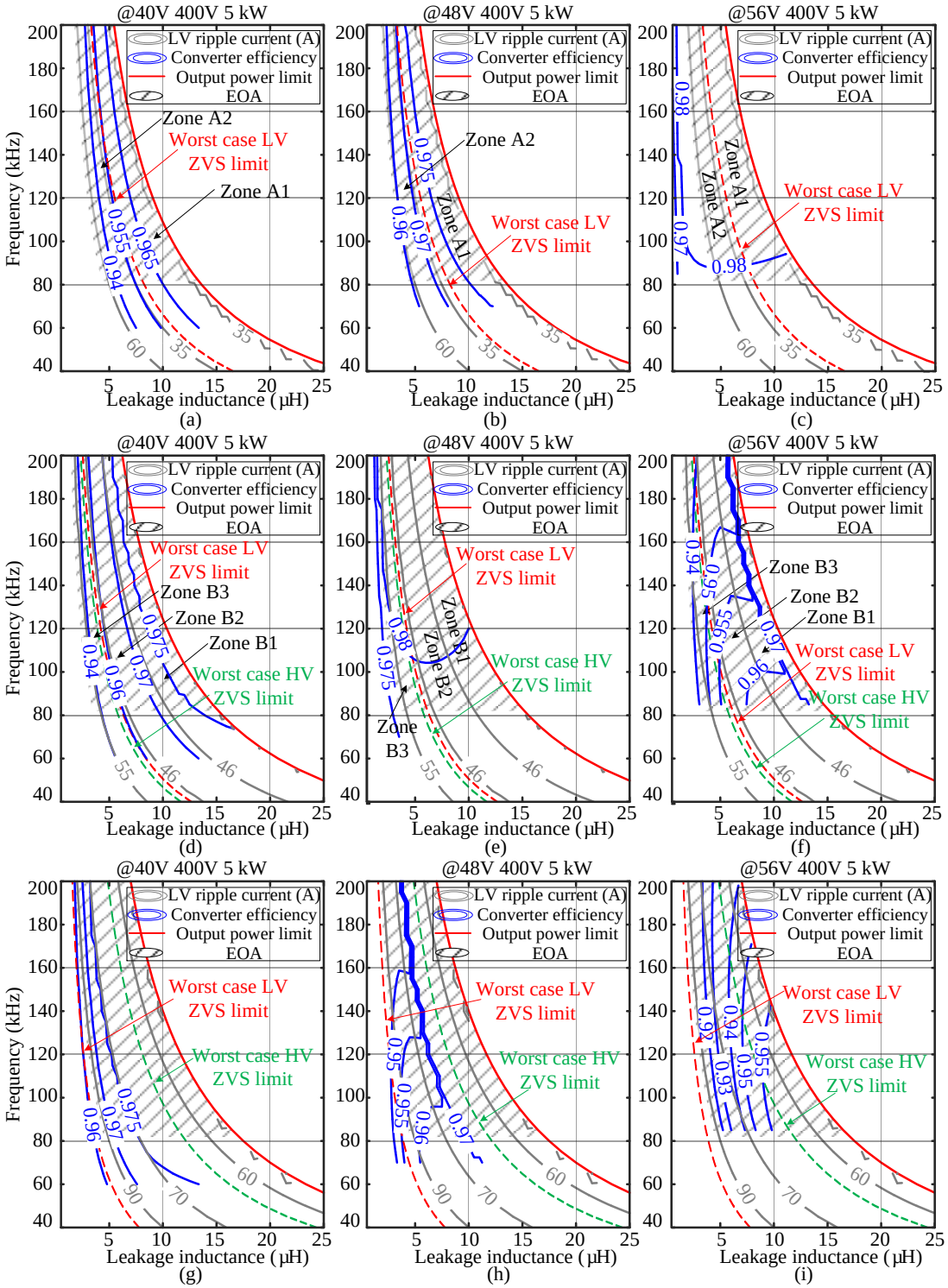


Fig. 4.13. Converter efficiency under half load at (a ~ c) n = 7, (d ~ f) n = 8 and (g ~ i) n = 9.

When converter is half loaded, the operating area with highest efficiency moves toward the power constraint, and high efficiency can be achieved in zone **B1**. When V_1 = 56 V (see as Fig. 4.13 (f)), hard switching happens on HV side, and the efficiency is much lower in zone **B2** and **B3**, especially at higher frequency.

When n = 9 and V_1 = 56 V, the converter efficiency becomes much lower at full load and half load due to the limited HV ZVS range, as shown in Fig. 4.12 and Fig. 4.13 (i). At nominal input voltage (V_1 = 48 V), the efficiency is lower at half load. Additionally, the ripple current on LV side is much higher (70 ~ 90 A) compared to n = 7 and 8, which will possibly result in a larger DC capacitor. Therefore, n = 9 is not recommended for this converter.

Combining the analysis above, within EOA, the converter efficiency at n = 7 and 8 are comparable. At n = 8, relatively higher efficiency is achieved at nominal input voltage (V_1 = 48 V) and lower input voltage (V_1 = 40 V). Slightly lower efficiency is achieved at higher input voltage (V_1 = 56 V) at half load, because of the narrower HV ZVS area compared to n = 7. In terms of capacitor ripple current, when n = 7, LV ripple current is lower and HV ripple current is higher.

In this converter, more emphasis is placed on converter efficiency at nominal operating voltage at any load condition. Hence n = 8 is preferred as the transformer turn ratio. The parameters f and L_k are chosen in zone **B2** and close to the boundary between zone **B1** and **B2** with lower frequency. The final parameters are chosen to be L_k = 8 μH, f = 100 kHz, which delivers maximum efficiency at most operating conditions.

4.5. SUMMARY

This chapter presents comprehensive considerations for three-phase DAB converter design. The impact of selectable parameters (n, f, L_k) on the converter performance, including ZVS operation area, switching device power losses, capacitor ripple current and system efficiency are studied.

A new parameter fL is defined to simplify the analysis from 3 dimensions (n, f, L_k) to 2 dimensions (n, fL). Based on this, the impact of transformer turn ratio n on ZVS range, RMS current and ripple current are analyzed and feasible values of n are determined.

With each fixed turn ratio n, the EOA of f and L_k are defined considering the transformer constraints. In the EOA, the losses analysis shows that HV side switching loss is more significant compared to LV side and should be avoided at any operating voltage. The feasible range of f and L_k is determined using the criteria of ZVS, converter efficiency and capacitor ripple current.

Chapter 5
PLANAR TRANSFORMER DESIGN FOR THE THREE-PHASE DUAL ACTIVE BRIDGE CONVERTER

5.1. DESIGN METHODOLOGY

According to the converter specifications in Table 1.1 and the designed parameters of the three-phase DAB converter in Chapter 4, the specifications of the transformer are summarized in Table 5.1.

Table 5.1 Specifications of the planar transformer

Description	Symbol	Value
Input voltage	V_1	40~56 V
Output voltage	V_2	400 V
Transformer RMS current (HV side)	I_{rms_tf}	22 A
Turns ratio	n	1:8
Switching frequency	f	100 kHz
Leakage inductance	L_k	8 μH
Allowable temperature rise	$\Delta T_{\max}$	60 ˚C
Ambient temperature	T	25 ˚C

The design methodology of planar transformer is similar to the standard transformer design in many aspects [61]. For example, the power handling capability can be estimated

by the area product of the magnetic core; the volt-second applied to the transformer should not saturate the core. The major difference in designing the planar transformer is the winding design. Higher current density is allowed, and the window utilization factor is usually much lower due to insulation material between winding layers. The flowchart of planar transformer design is summarized in Fig. 5.1.

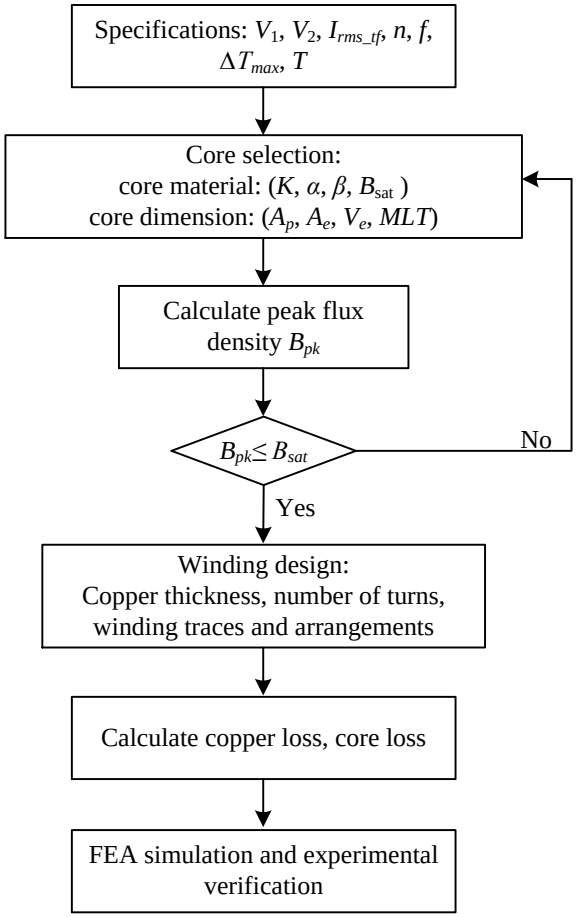


Fig. 5.1. Design flowchart of planar transformer.

In this particular case, due to the limited area product of the available magnetic cores in the market, single planar EE core cannot accommodate three-phase windings. To design an integrated three-phase transformer, paralleled cores can be applied, as shown in

Fig. 5.2 [39, 62]. In Fig. 5.2 (a), two EE cores are stacked together to increase the core area, the three phases windings are wound around the center and outer legs, respectively. However, due to uneven cross-section area, the flux density is not symmetrical in three phases, hence the parameters of three phases may not be symmetric. In Fig. 5.2 (b), two EE cores are parallel together to increase the window area. However, the window area around the center column needs to accommodate windings of two different phases, which limits the size of the winding.

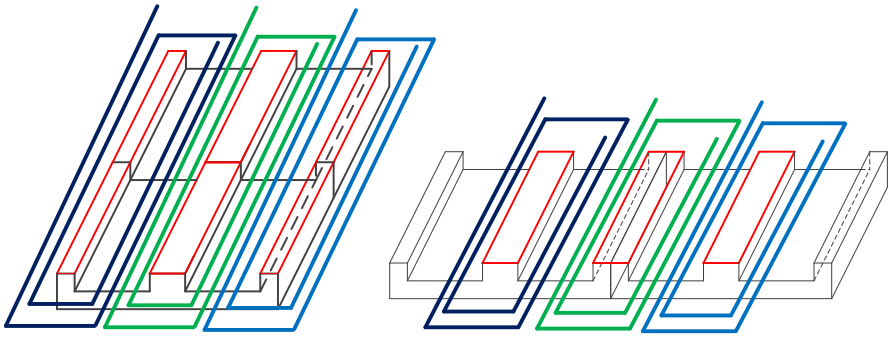


Fig. 5.2. Cores in parallel to extend power capability.

The ease of duplication makes three single-phase transformers a practical realization in three-phase DAB converter, and equal stray parameters can be achieved, which is beneficial to current balancing among three phases. As a result, three single-phase transformers will be designed and implemented.

5.2. TRANSFORMER CORE SELECTION

The power handling capability of a transformer core is proportional to its area product A_p, which is the product of its window area A_w and cross-section area A_e, as

shown in Fig. 5.3. The relationship between A_p and the transformer apparent power P_t can be described as

$$A_p = \frac{P_t \times 10^4}{K_f K_u B_m J f} \tag{5.1}$$

where, K_f is the waveform coefficient, K_u is the window utilization factor, B_m is the maximum flux density, J is the current density and f is the operating frequency. For this specific transformer design, the parameters (P_t, K_f, B_m) will be discussed in the following sections.

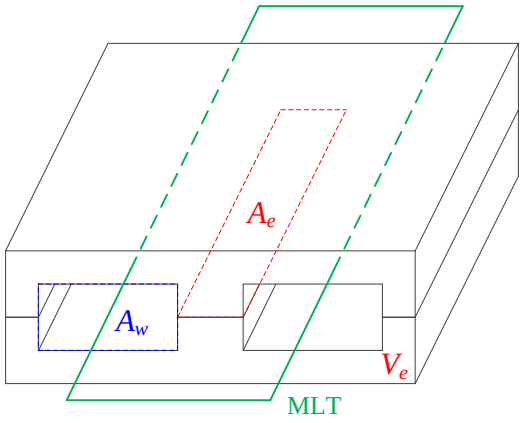


Fig. 5.3. Dimensions of planar EE core: A_w, A_e, V_e and MLT.

The window utilization factor K_u is much lower than the conventional transformer because of the PCB substrate or insulation layer between windings. A conservative but reasonable window utilization factor is estimated to be 0.21 in the preliminary design, which needs to be verified once the design is finalized [39].

Due to wide winding width and higher surface to volume ratio of the planar core, relatively faster heat dissipation and better temperature characteristics are realized. The

thin copper will reduce the skin effect significantly. As a result, higher current density J is achieved in planar transformer. In this design, J is initialized as 1000A/cm^2.

Transformer kVA Rating and Apparent power

The kVA rating of the transformer used in three-phase DAB can be calculated as

$$(KVA)_T = \frac{1}{2}\cdot 3\left[V_{Ap(rms)} I_{p(rms)} + V_{as(rms)} I_{s(rms)}\right] \tag{5.2}$$

where, $I_{p(rms)}$ and $I_{s(rms)}$ are the RMS current of the transformer on primary and secondary side, respectively. The RMS value of the six-step line-to-neutral voltage $v_{Ap(rms)}$ and $v_{as(rms)}$ in Fig. 3.2 can be calculated by averaging the square root over one switching period, and

$$v_{Ap(rms)} = \sqrt{\frac{1}{3}\left((\frac{2}{3}V_1)^2 + 2\cdot(\frac{1}{3}V_1)^2\right)} = \frac{2}{3}\cdot\frac{V_1}{\sqrt{2}}, v_{as(rms)} = \frac{2}{3}\cdot\frac{V_2}{\sqrt{2}} \tag{5.3}$$

By substituting (5.3) to (5.2), the transformer kVA rating can be calculated as

$$(KVA)_T = \frac{(nV_1 + V_2) I_{rms\_tf}}{\sqrt{2}} \tag{5.4}$$

where the transformer RMS current on HV side I_{rms_tf} is specified in Table 5.1. Thus the total power rating of three transformers is 12.5 kVA, or 4.2 kVA per single transformer. The transformer needs to accommodate both primary and secondary windings, corresponding to input power P_{in} and output power P_o. The apparent power P_t is calculated as

$$P_t = P_{in} + P_o = P_o(1+\frac{1}{\eta}) \tag{5.5}$$

where, P_o=$V_{as(rms)}$·I_{rms_tf}, the converter efficiency η is estimated at 0.97. The calculated transformer apparent power P_t is 8.13 kW.

Waveform Coefficient

In three-phase DAB converter, the phase voltage applied to the transformer as well as the induced flux waveform can be obtained by means of Faraday's law, as shown in Fig. 5.4. The peak flux Φ_m can be obtained by integrating the voltage in half a period as:

$$\Phi_m = \frac{1}{N} \cdot \left(\frac{2V_{DC}}{3} + \frac{V_{DC}}{3} \cdot 2\right) \cdot \frac{1}{6f} = \frac{V_{DC}}{9fN} \tag{5.6}$$

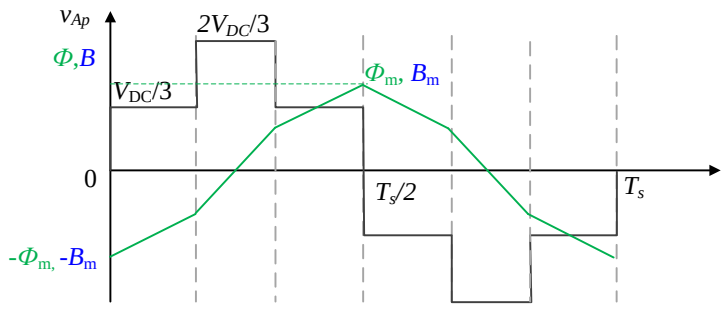


Fig. 5.4. Voltage, flux and flux density waveform of transformer.

By substituting (5.3) to (5.6), the relationship between RMS voltage and peak flux flow Φ_m can be derived.

$$V_{rms} = 3\sqrt{2} fN\Phi_m \tag{5.7}$$

Therefore, the waveform coefficient $K_f = 3\sqrt{2}$, and the peak flux density can be calculated by $B_m = \Phi_m/A_e$.

Maximum Flux Density

For the first iteration of core selection, peak flux density B_{pk} = 0.15 T is assumed at f = 100 kHz. Substituting the parameters (P_t, K_f, K_u, J, B_{pk}) into (5.1), a ferrite core with $A_p \geq 6.08$ cm^4 is required. From the available planar cores on the market, EE 58/11/38 and

EE 64/10/50 with material N87 from Epcos are selected. The core parameters of EE 58 and EE 64 are listed in Table 5.2.

Assume half of the transformer losses are core loss [63], the temperature rise caused by core loss P_{core} should not exceed half of the allowable temperature rise $\Delta T_{\max}$.

$$P_{core} \cdot R_{\text{th}} \le \Delta T_{\max} / 2 \tag{5.8}$$

Table 5.2 Steinmetz coefficient of N87 and core dimension of EE 58 and EE 64

Steinmetz coefficient	K		α	β	
N87	10.2494		1.296	2.374	
Core dimension	A_e (cm^2)	A_w (cm^2)	A_p (cm^4)	V_e (cm^3)	B_{pk} (T)
EE 58/11/38	3.08	2.72	8.37	24.6	0.1
EE 64/10/50	5.19	2.22	11.54	40.7	0.09

Empirical formula is used here to estimate the transformer thermal resistance R_{th} by its core volume V_e, where $R_{\text{th}} = 53 \cdot (V_e)^{-0.54}$ [64]. The calculated thermal resistance for EE 58 and EE 64 are 9.3 K/W and 7.1 K/W, respectively. Assuming the converter operates at room temperature (25 ℃), and the allowable temperature rise is 60 ℃. Thus the allowable core loss density p_{v_pk} can be determined by

$$p_{v\_pk} \le \frac{\Delta T_{\max}}{2R_{\text{th}} \cdot V_e} \ [\text{W/m}^3] \tag{5.9}$$

According to (2.1), the maximum allowable flux density B_{pk} can be approximated by

$$B_{pk} = \left(\frac{p_{v\_pk}}{Kf^{\alpha}} \right)^{1/\beta} \tag{5.10}$$

The allowable peak flux density B_{pk} of EE 58 and EE 64 can be obtained accordingly. For EE 58, B_{pk} = 0.1 T and for EE 64, B_{pk} =0.09 T. Resubstituting B_{pk} into (5.1), the required area product $A_p \geq 10.14$ cm^4. Hence, EE 64 core is selected for this converter.

5.3. WINDING DESIGN

5.3.1. Winding Trace Design

According to Faraday's law, the number of turns can be calculated from (5.11), and the number of turns on primary and secondary side are designed as n_p = 1 and n_s = 8, respectively.

$$n_p = \frac{V_1 \times 10^4}{9 f B_m A_e} = 1.14 \tag{5.11}$$

To reduce the winding resistance, fully interleaved winding arrangement (m = 1) is adopted in this design. From the AC resistance curve in Fig. 2.6, the minimum value of AC resistance is achieved when the copper thickness h is smaller or equal to the skin depth δ. At f = 100 kHz, δ = 210 μm. Considering the PCB manufacturing simplicity and cost, a two-layer PCB with 5-oz (175 μm) copper is selected.

From Table 5.1, the RMS currents flow through the primary and secondary windings are 176 A and 22 A, respectively. The minimum trace width and the clearance between traces are calculated and listed in Table 5.3. The trace widths are specified under the constraint of temperature rise. The clearance between trace and the core and the clearance between traces (turn-to-turn clearance) are also calculated [65, 66].

Table 5.3 Minimum trace width and clearance between traces

	Current (Arms)	Voltage (V)	Turn-to-turn voltage (V)	Minimum trace width (mm)	Minimum clearance (mm)	Turn-to-turn clearance (mm)
Primary winding	176	50	50	196 (ΔT=10 ℃)	0.9	N/A
Secondary winding	22	400	50	11 (ΔT=10 ℃)	2.6	0.9

The designed primary and secondary windings are shown in Fig. 5.5. The secondary winding is formed by connecting two secondary windings in series. The specifications of the finished PCB based windings are listed in Table 5.4.

Table 5.4 Specifications of primary and secondary winding

Description	Symbol	Value
Copper thickness	h_1	0.175 mm
PCB substrate (FR4) thickness	$h_{\Delta 1}$	0.3 mm
Insulation thickness between PCBs	$h_{\Delta 2}$	0.2008 mm
Primary trace width	w_p	18.5 mm
Secondary trace width	w_s	3 mm
Paralleled layers of primary winding	n_1	12
Paralleled layers of secondary winding	n_2	6
Mean length per turn of E64 core	MLT	209.2 mm

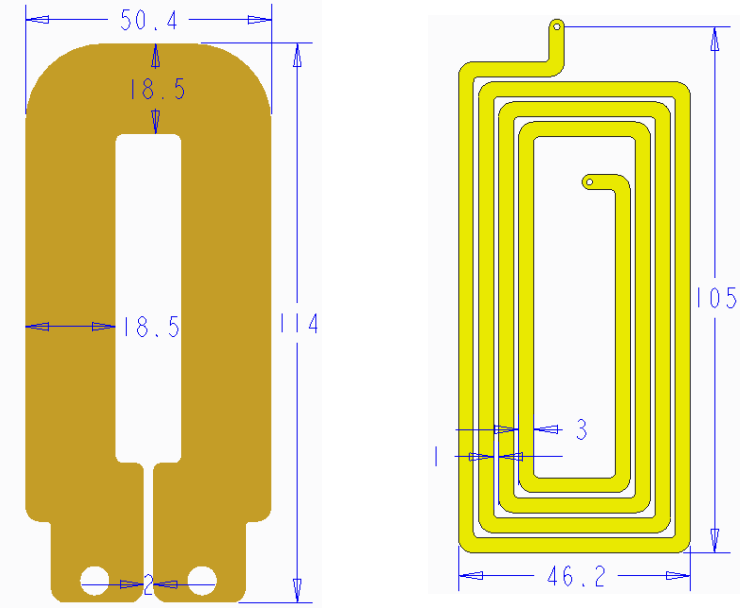


Fig. 5.5. Trace width and spacing of primary and secondary winding.

Kapton insulation film is applied between PCBs to provide isolation. The finished PCB board has a total thickness of 0.8 mm, which added 0.075 mm thickness insulation on top of the windings on each side. The DC resistance of primary and secondary windings can be calculated as:

$$R_{dc\_p} = \rho \frac{n_p MLT}{w_p h_1 \cdot n_1} = 0.106\ \text{m}\Omega$$
$$R_{dc\_s} = \rho \frac{n_s MLT}{w_s h_1 \cdot n_2} = 9.2\ \text{m}\Omega \quad (5.12)$$

5.3.2. Winding Arrangements

In order to minimize the copper loss, in this particular design, the windings are fully interleaved. The winding arrangement of the primary and secondary windings is illustrated in Fig. 5.6 (c). As a comparison, two different winding arrangements are also investigated, as shown in Fig. 5.6 (a) and (b), both of which can be constructed by using

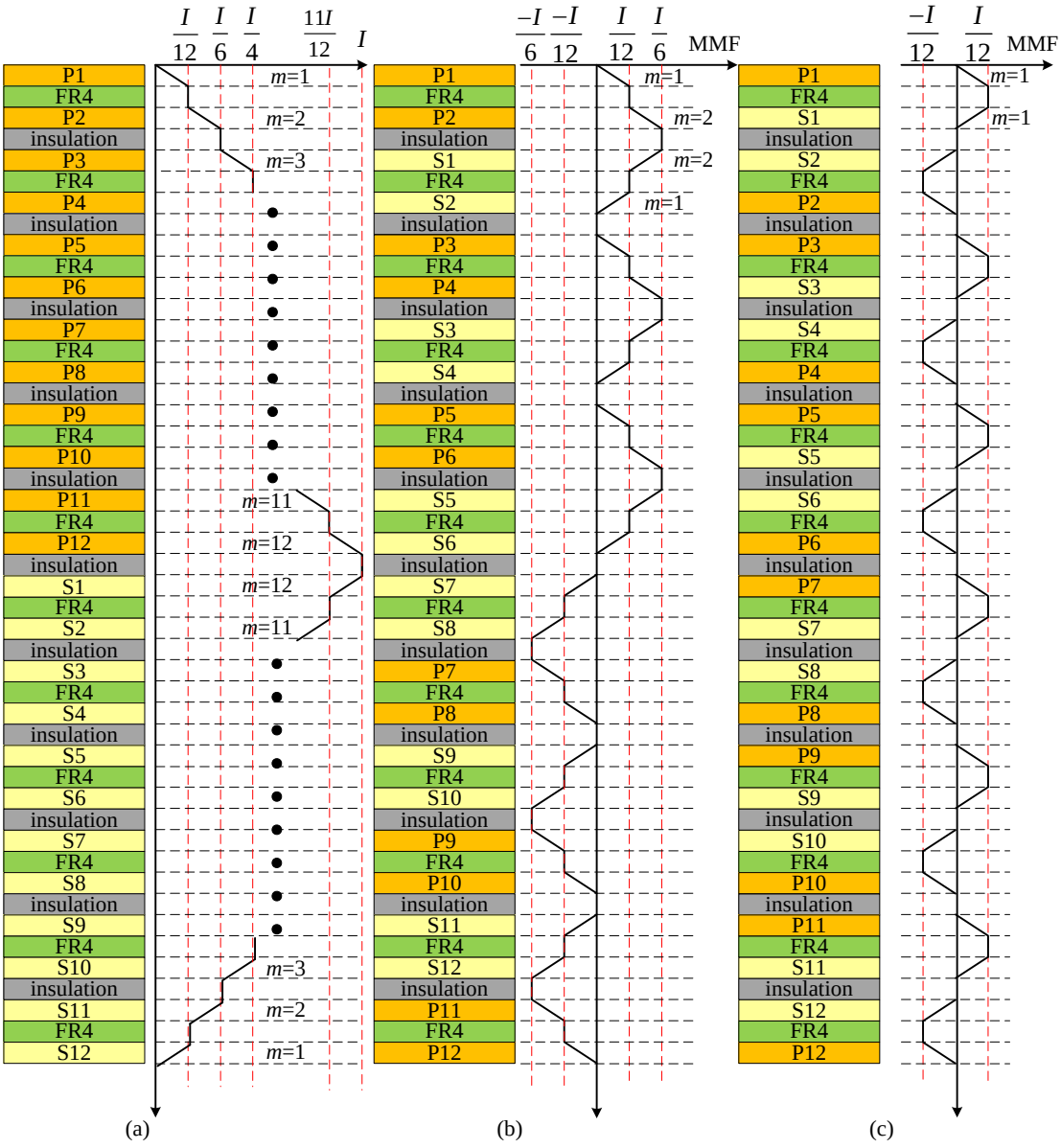


Fig. 5.6. MMF distribution of (a) non-interleaved, (b) partial-interleaved and (c) fully-interleaved winding.

two different types of PCBs, one with primary winding and the other with secondary winding. The MMF distributions of these three winding arrangements are also shown on the side. The non-interleaved winding in (a) features continuously increasing MMF and the ratio *m*. The MMF of the partial-interleaved winding in (b) increases within two

consecutive layers of the PCB and the maximum m = 2. The fully-interleaved winding in Fig. 5.6 (c) has the lowest MMF amplitude and m = 1.

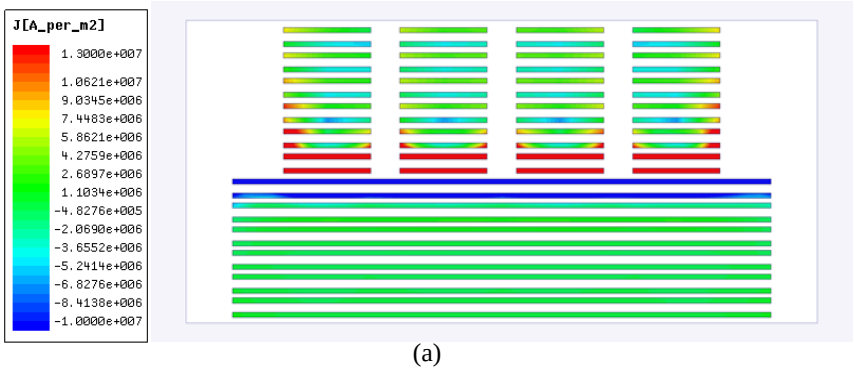
Impact on Copper Losses

For selected 5-oz copper, the ratio $\xi = h/\delta = 0.83$. Substituting m and ξ to (2.3), the ratio between AC and DC resistance under each winding arrangement can be calculated.

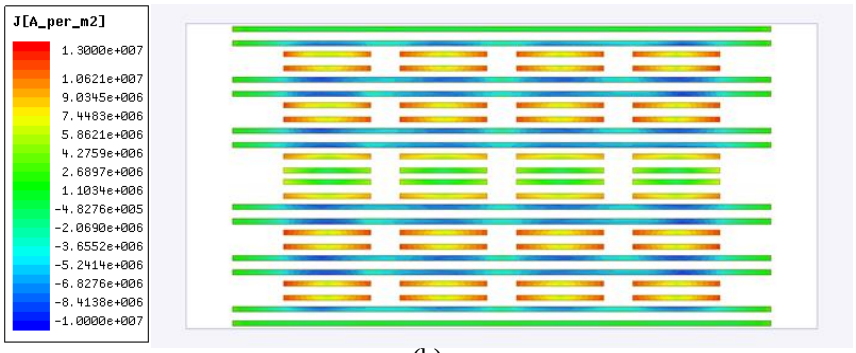
$$\begin{aligned} R_{ac}/R_{dc(a)} &= 8.4419 \\ R_{ac}/R_{dc\,(b)} &= 1.1968 \\ R_{ac}/R_{dc(c)} &= 1.0415 \end{aligned} \tag{5.13}$$

The analytical results are verified by finite element analysis (FEA). Three winding structures corresponding to Fig. 5.6 are built in Maxwell 2D. The current distributions are simulated at full load, and the simulated results are depicted in Fig. 5.7. The scales of the three different winding arrangements are all specified from -1000 A/cm^2 to 1300 A/cm^2.

The current in primary and secondary windings are in opposite direction, because of the proximity effect, when they are arranged in adjacent layers, the current tend to attract each other. Therefore, current is distributed more evenly in the fully-interleaved winding.



(a)



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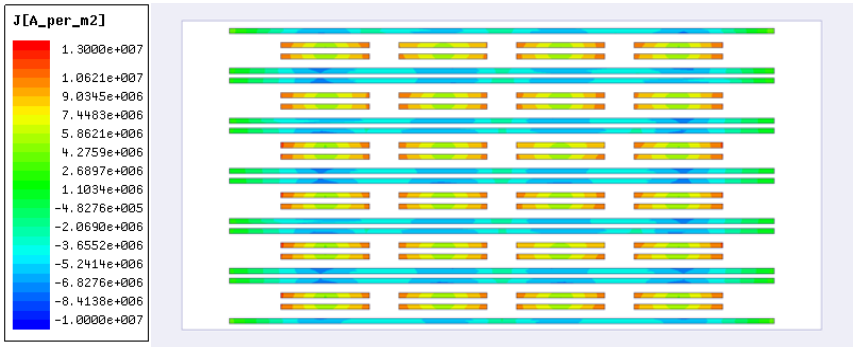


(c)

Fig. 5.7. Current distribution in (a) non-interleaved, (b) partial-interleaved and (c) fully-interleaved winding (2D).

In the primary side of the interleaved winding arrangement, it is observed that the current is concentrated in the area overlapped with secondary windings. This is also verified by 3D FEA simulation, and the 3D transformer model is shown in Fig. 5.8. As shown in Fig. 5.9, the current distribution of the fully interleaved winding is illustrated.

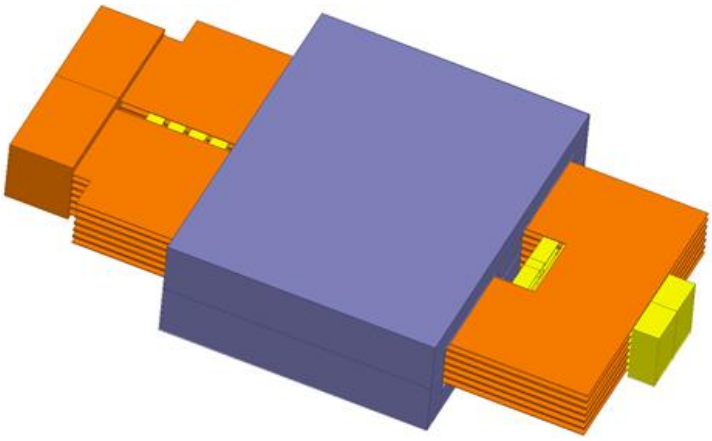
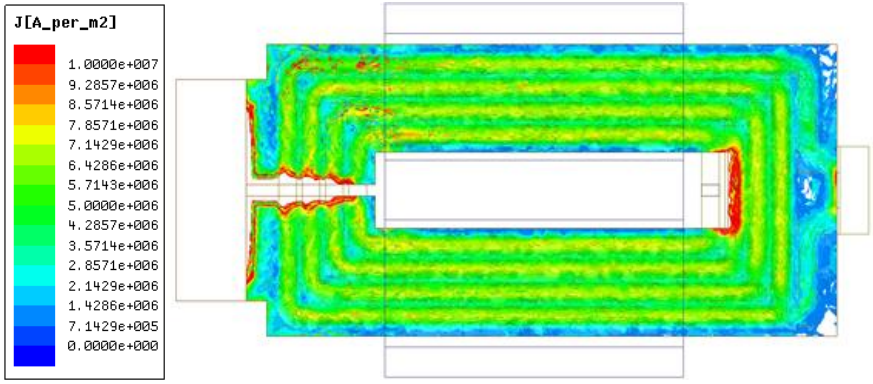
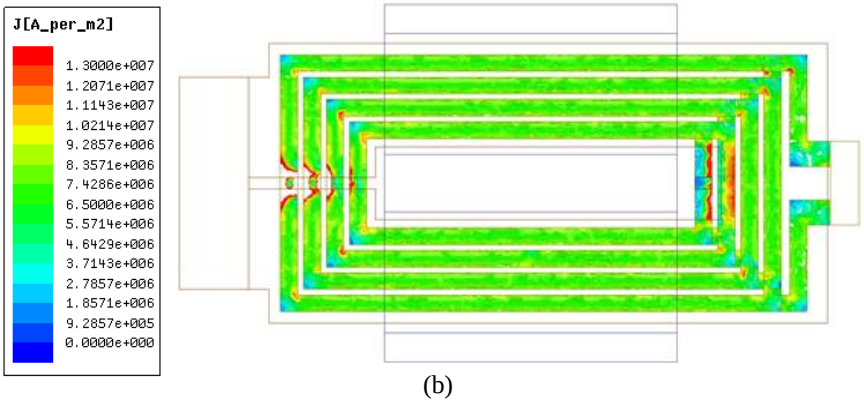


Fig. 5.8. Maxwell 3D transformer model



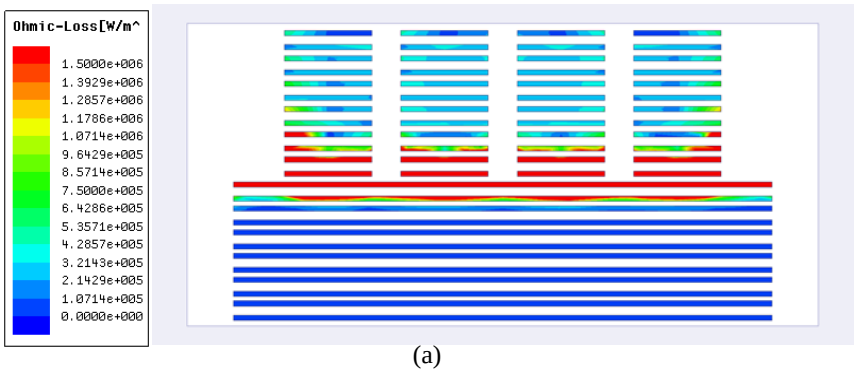
(a)



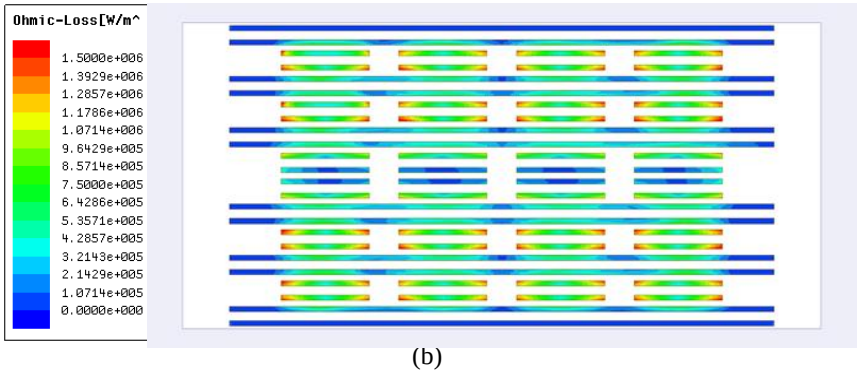
(b)

Fig. 5.9. Current distribution of fully interleaved winding structure in (a) primary winding (b) secondary winding (3D).

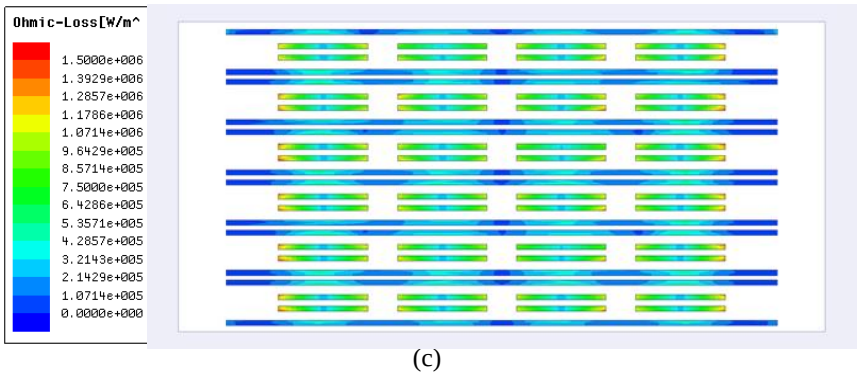
The copper loss distributions of the three winding structures are also investigated in Maxwell simulation. As shown in Fig. 5.10, much higher copper loss density is observed in the non-interleaved winding, and the fully-interleaved winding shows the best loss performance.



(a)



(b)



(c)

Fig. 5.10. Ohmic loss distribution of (a) non-interleaved, (b) partial-interleaved and (c) fully-interleaved winding.

The AC resistances are solved at different frequencies in 2D Maxwell using eddy current solver. The AC resistances of primary and secondary windings are displayed in Fig. 5.11. Under three different winding arrangements, the AC resistance increases with frequency. The partial- and fully-interleaved winding features much lower resistance under all frequencies. Comparing the partial-interleaved and fully-interleaved winding, partial-interleaved winding features slightly lower primary resistance and slightly higher secondary resistance. The fully-interleaved winding structure is also simulated in Maxwell 3D to account for end winding resistance, and the results are given in Fig. 5.12. Compared to the theoretically calculated resistance in (5.12) and (5.13), much higher AC resistance is observed.

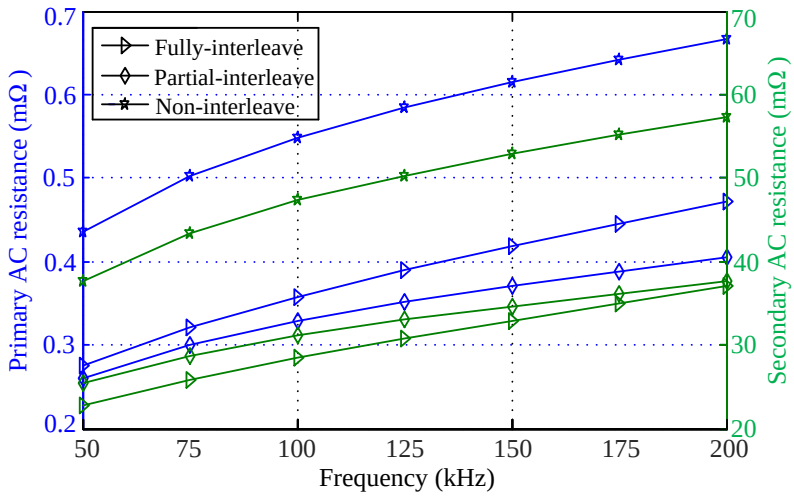


Fig. 5.11. Simulated AC resistance of three winding structures (2D)

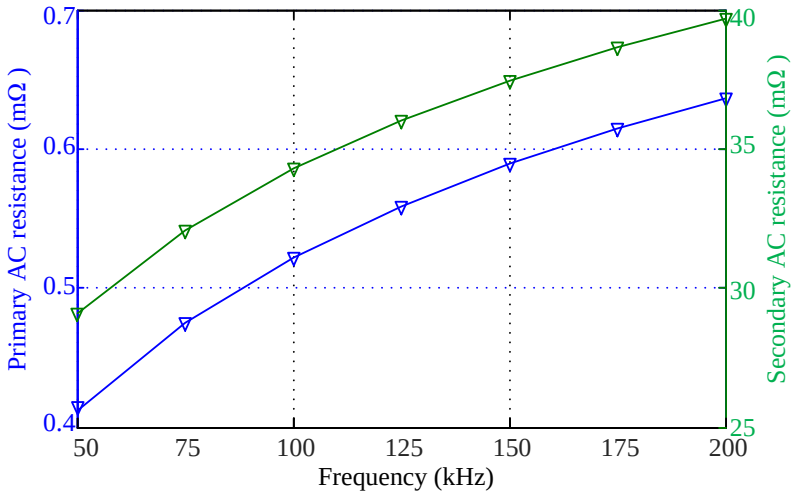


Fig. 5.12. Simulated AC resistance of fully-interleaved winding (3D).

Impact on Leakage Inductance

Based on the leakage inductance analysis in section 2.3.1, the leakage inductance of these three types of winding arrangements are also calculated assuming the leakage flux lines are parallel with the winding layers. The results are given in (5.14) - (5.16), corresponding to the winding arrangements in Fig. 5.6 (a) – (c), respectively. It is obvious that interleaved winding features significantly lower leakage inductance.

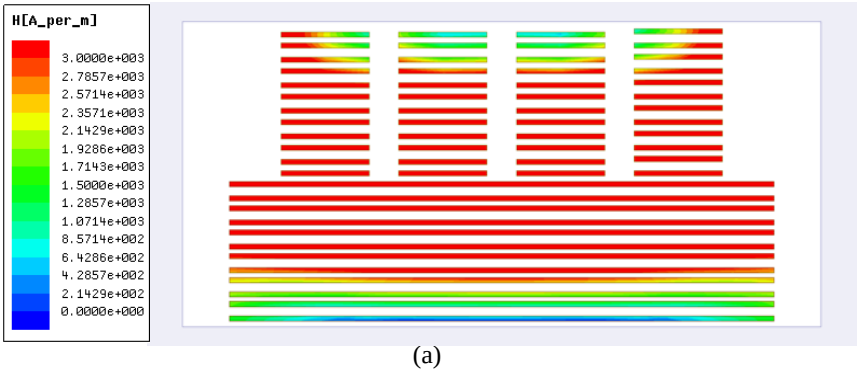
$$L_{k(a)} = \mu_0 \cdot l_w \cdot b_w \left[\begin{array}{l} 2 \cdot 12 \left(\dfrac{I}{12 b_w} \right)^2 \cdot \dfrac{h_1}{3} + \dfrac{\left(I^2 + 4I^2 + 9I^2 + \cdots + 121I^2 \right)}{\left(12 b_w \right)^2} \cdot \\ \left(2h_1 + h_{\Delta 1} + h_{\Delta 2} \right) + \dfrac{\left(I^2 + 2I^2 + 3I^2 + \cdots + 11I^2 \right)}{\left(12 b_w \right)^2} \cdot 2h_1 + \dfrac{I^2}{b_w^2} \cdot h_{\Delta 2} \end{array} \right] \quad (5.14)$$

$$= \mu_0 \cdot \frac{l_w}{b_w} \cdot \frac{1}{144} \cdot \left(1152 h_1 + 506 h_{\Delta 1} + 650 h_{\Delta 2} \right)$$

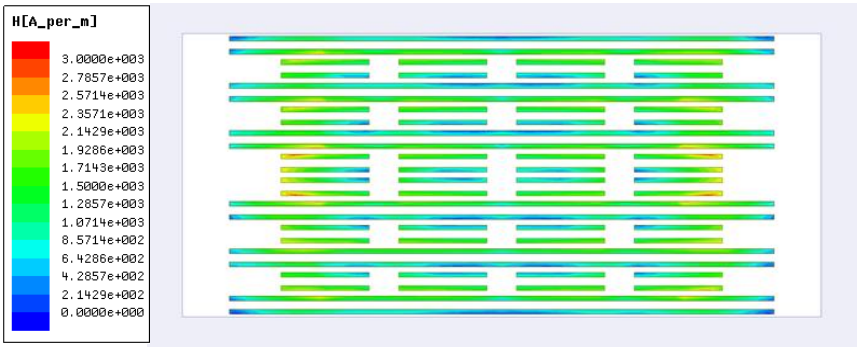
$$L_{k(b)} = \mu_0 \cdot \frac{l_w}{b_w} \cdot \frac{1}{144} \cdot 6 \cdot \left(\frac{16}{3} h_1 + 2h_{\Delta 1} + 4h_{\Delta 2} \right) \quad (5.15)$$

$$L_{k(c)} = \mu_0 \cdot \frac{l_w}{b_w} \cdot \frac{1}{144} \cdot \left(8h_1 + 12 h_{\Delta 1} \right) \quad (5.16)$$

The leakage flux is also simulated in Maxwell 2D. For all three winding arrangements, the magnetic field strength and flux line distribution are displayed in the window area, as shown in Fig. 5.13 and Fig. 5.14, respectively. The scale in Fig. 5.13 (a)-(c) all measured in the range of 0 to 3000 A/m.



(a)



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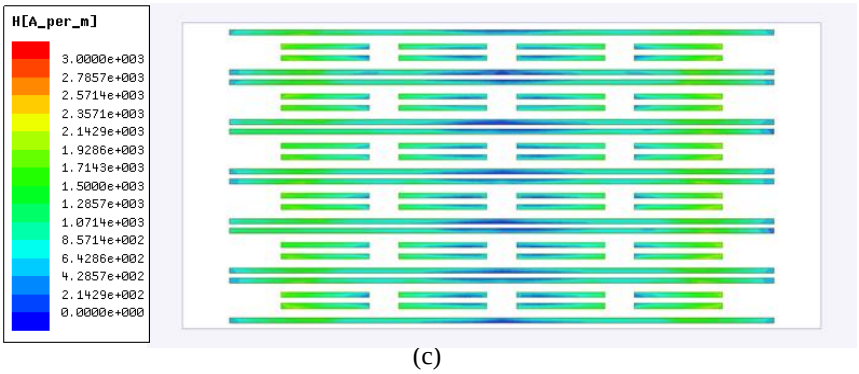
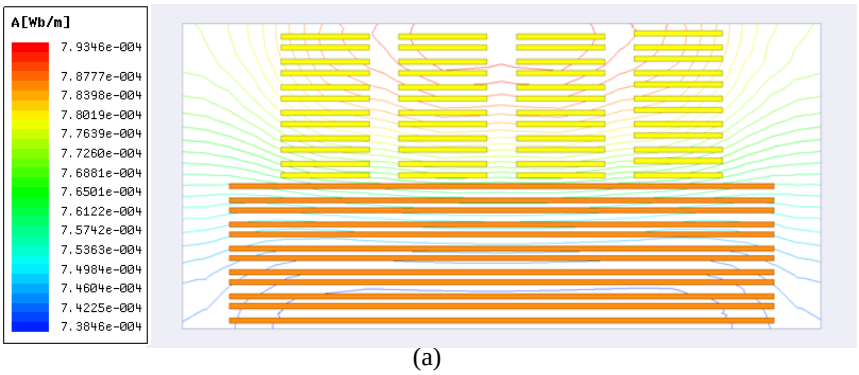
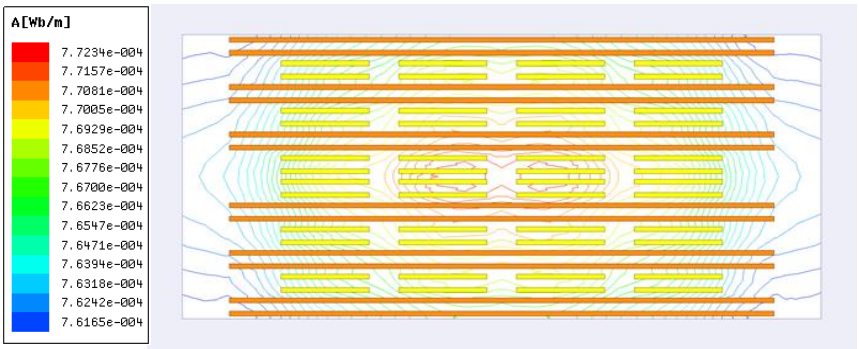


(c)

Fig. 5.13. Magnetic field strength distribution of (a) non-interleaved, (b) half-interleaved and (c) fully-interleaved winding



(a)



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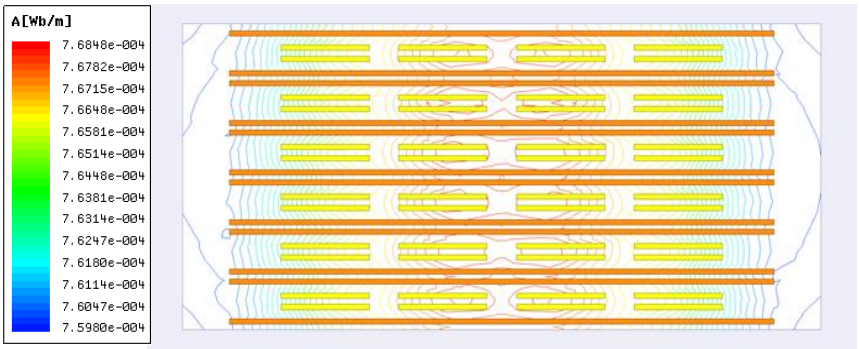


(c)

Fig. 5.14. Flux line distribution of (a) non-interleaved, (b) half-interleaved and (c) fully-interleaved winding.

The flux lines of non-interleaved winding in the window area are mostly parallel to the conductor. Hence the magnetic field strength *H* can be considered increasing linearly along the window breadth, and the assumption for the calculation of leakage inductance holds true. However, in the interleaved winding, a large portion of the leakage flux lines

are in the vertical direction, which makes the H distribution deviates greatly from assumption, and hence the calculated leakage inductance in (5.15) and (5.16) cannot be trusted. Therefore, the leakage inductances are computed using the FEA simulations and the results are given in Table 5.5. The computed leakage inductances are referred to the HV side. The interleaved winding features lower leakage inductance.

Table 5.5 Leakage inductance of different winding structure

Winding structure	Analytical (μH)	Simulation (μH)
Non-interleaved winding	1.26	1.315
Partial-interleaved winding	0.036	0.295
Fully-interleaved winding	0.013	0.195

For non-interleaved winding arrangement, the simulated result of L_k (1.315 μH) is very close to the calculated result (1.26 μH). The simulated inductance of partial-interleaved and fully-interleaved winding arrangements deviate from the theoretical analysis in (5.15) and (5.16), and much higher inductance values are observed. However, it is still observed the leakage inductance decreases as the windings get more interleaved.

Impact on Stray Capacitance

Since the windings are flat and placed in parallel, the inter-winding capacitance between two adjacent layers can be calculated by

$$C_{\text{inter}} = \varepsilon_0 \varepsilon_r \frac{A_t}{d} \tag{5.17}$$

where, ε_0 and ε_r are the permittivity of air and the insulation material between the two layers, A_t and d are the overlapping area and the vertical distance between the two layers, respectively. For a transformer with m intersections between primary and secondary windings, the capacitance at each intersection add up together to form the total inter-winding capacitance [53].

The intra-winding capacitance between two adjacent layers in the same winding can be obtained by calculating the electrostatic energy stored between the layers. For the primary side, there is only one turn, and between the paralleled primary windings, the voltage gradient is zero. Thus no intra-winding capacitance exists on primary side. On the secondary side, due to the high width-to-height ratio of the planar winding, the energy stored between two consecutive turns in the same layer can be considered negligible. In this particular design, for two adjacent layers in series, the electrostatic energy stored between the overlapped areas can be calculated by integrating the energy density within this region [53].

$$E_c = \int_V \frac{1}{2} D \cdot E dV = \frac{1}{2} C_s V_2^2 \tag{5.18}$$

where the electric field strength $E = V_x/d$, $V_x = V_2 x/L$, the electric displacement $D = \varepsilon_0 \varepsilon_r E$, L is the total winding length in one layer, $dV = W \cdot d \cdot dx$ is the differential volume, W is the winding trace width, dx is the horizontal distance to the reference point of the winding, as indicated in Fig. 5.15 [53].

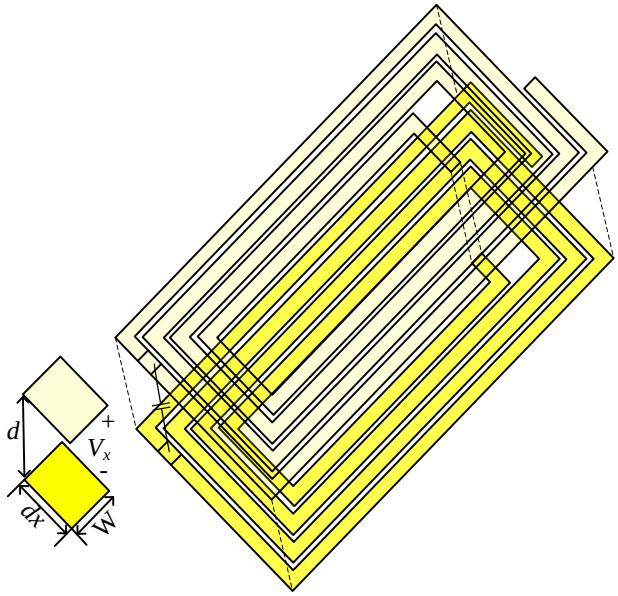


Fig. 5.15. Intra-winding capacitance of two adjacent winding layers in series.

The intra-winding energy between overlapped traces can be expressed by

$$E_c = \int_0^L \frac{1}{2}\varepsilon_0\varepsilon_r \left(\frac{V_2 \cdot x}{L \cdot d}\right)^2 \cdot W \cdot d \cdot dx = \frac{1}{6}\varepsilon_0\varepsilon_r V_2^2 \cdot \frac{W \cdot L}{d} \tag{5.19}$$

Therefore, the intra-winding capacitance of two layers in series with fully overlapped winding area can be calculated as

$$C_{intra} = \frac{1}{3}\varepsilon_0\varepsilon_r \frac{W \cdot L}{d} = \frac{1}{3}\varepsilon_0\varepsilon_r \frac{A_t}{d} \tag{5.20}$$

In (5.20), if the same overlapping area A_t and vertical distance d is applied, the intra-winding capacitance is one-third of the inter-winding capacitance. The inter- and intra-winding capacitances are also obtained from FEA using electrostatic solver, and the results are given in Table 5.6.

Table 5.6 Inter- and intra-capacitance of different winding structure

Winding structure	Inter-winding capacitance (nF)		Intra-winding capacitance (nF)	
	Calculation	Simulation	Calculation	Simulation
Non-interleaved winding	0.5	0.29	1.5	2.4
Partial-interleaved winding	5.0	3.01	0.78	1.75
Fully-interleaved winding	4.0	2.25	1.0	1.93

For non-interleaved winding structure, lowest inter-winding capacitance is achieved due to lowest intersection (= 1) between primary and secondary windings. Although partial-interleaved winding has lower intersections (= 10) than fully-interleaved winding (= 12), it features higher inter-winding capacitance contributed by closer distance between different winding layers.

Similarly, highest intra-winding capacitance is observed in non-interleaved winding structure, as it features highest intersection number between secondary windings. Compared to fully-interleaved winding, despite of the fact that partial-interleaved winding has higher number of intersections, lower intra-winding capacitance is observed due to the larger distance between secondary windings.

5.4. MAGNETIZING INDUCTANCE

The magnetizing inductance L_{m} is preferred to be much higher than the leakage inductance; otherwise the magnetizing current $i_{L\mathrm{m}}$ is not negligible. The value of L_{m} is determined by the parameters of the selected core and the number of turns applied.

$$L_m = \frac{N^2}{R} = \frac{n_s^2}{\frac{1}{\mu \cdot \mu_0} \cdot \frac{l_e^{'}}{A_e}} \tag{5.21}$$

where, R is the magnetic reluctance of the core, μ is relative permeability (for selected material), A_e is the effective area, n_s is number of turns, and $l_e^{'}$ is the equivalent length of the magnetic path. In this design, the magnetizing inductance is calculated to be 778 μH.

The magnetizing inductance is also simulated from FEA, and the result (826.86 μH) is close to the theoretical value with an error at 6%. As shown in Fig. 5.4, the flux density varies in one period. At $t = T_s/2$, the flux density approaches its maximum value and its distribution in the magnetic core is shown in Fig. 5.16, with scale ranges from 0 to 0.15 T. In most of the core area, the flux density is around 0.10 to 0.11 T.

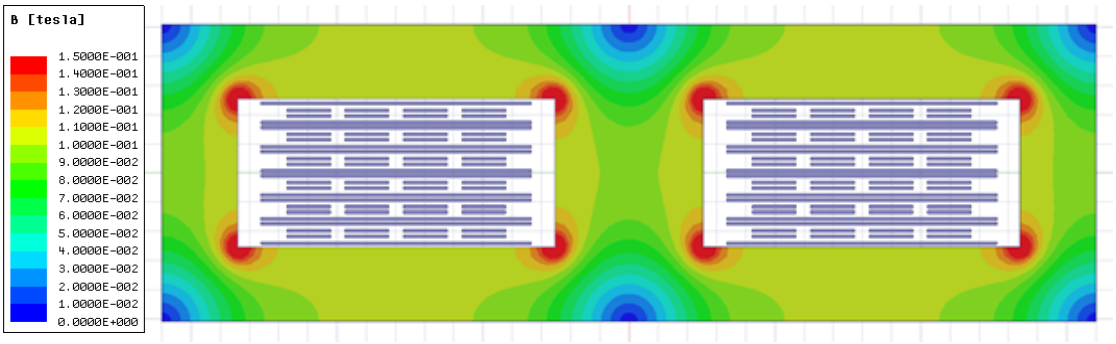


Fig. 5.16. Flux density distribution of fully-interleaved winding.

The magnetizing current can be therefore determined by the volt-second applied to the windings. The peak value of i_{Lm} is calculated by

$$i_{Lm\_pk} = \frac{1}{L_m} \cdot \left(\frac{2V_2}{3} \cdot \frac{1}{12f} + \frac{V_2}{3} \cdot \frac{1}{6f}\right) \tag{5.22}$$

At f = 100 kHz, i_{Lm_pk} is 0.54 A, which is much lower than the current flowing through the converter.

5.5. CORE LOSS

The commonly used Steinmetz equation in (2.1) is only valid for sinusoidal excitation, which is not the case in the three-phase DAB converter according to the flux waveform in Fig. 5.4. Several modified expressions of Steinmetz equation have been proposed [67, 68], among which the improved generalized Steinmetz equation (IGSE) features best core loss estimation under a wide variety of waveforms.

$$\begin{aligned} p_v &= \frac{1}{T}\int_0^T K_i \cdot \left|\frac{dB(t)}{dt}\right|^{\alpha} \cdot \Delta B^{\beta-\alpha} \cdot dt \\ K_i &= \frac{K}{(2\pi)^{\alpha-1} \cdot \int_0^{2\pi} \left|\cos\theta\right|^{\alpha} \cdot 2^{\beta-\alpha} \cdot d\theta} \end{aligned} \tag{5.23}$$

where, K, α, β are the same coefficients used in (2.1) under sinusoidal excitation, θ represents the phase angle of the sinusoidal waveform, $\Delta B = 2\,B_{\mathrm{m}}$ is the peak-to-peak flux density.

The non-sinusoidal flux density waveform in Fig. 5.4 can be described by a piecewise linear model (PWL), where

$$\left|\frac{dB(t)}{dt}\right| = \begin{cases} \dfrac{V_1}{3A_e} & t \in [0, T_s/6], [T_s/3, 2T_s/3], [5T_s/6, T_s] \\ \dfrac{2V_1}{3A_e} & t \in [T_s/6, T_s/3], [2T_s/3, 5T_s/6] \end{cases} \tag{5.24}$$

By combining the PWL in (5.24) with IGSE in (5.23), the equation of core loss density can be derived.

$$p_v = K_i f^{\alpha} B_m^{\beta} \cdot 3^{\alpha-1} \cdot \left(2^{\beta} + 2^{\beta-\alpha+1}\right) \tag{5.25}$$

where K_i can be obtained by curve fitting of the integrated results of $\int_0^{2\pi} \left|\cos\theta\right|^{\alpha} d\theta$ under different values of α [69]. The calculated core loss is 6.48 W.

$$K_i = \frac{K}{2^{\beta+1}\pi^{\alpha-1}(0.2761+\frac{1.7061}{\alpha+1.354})} \tag{5.26}$$

The transformer core loss is simulated in Maxwell 2D under transient solver. By imposing the six-step voltage excitation with phase shift on both windings, the flux linkage and core loss waveforms are shown in Fig. 5.17. The average value of core loss over a period is 5.2 W.

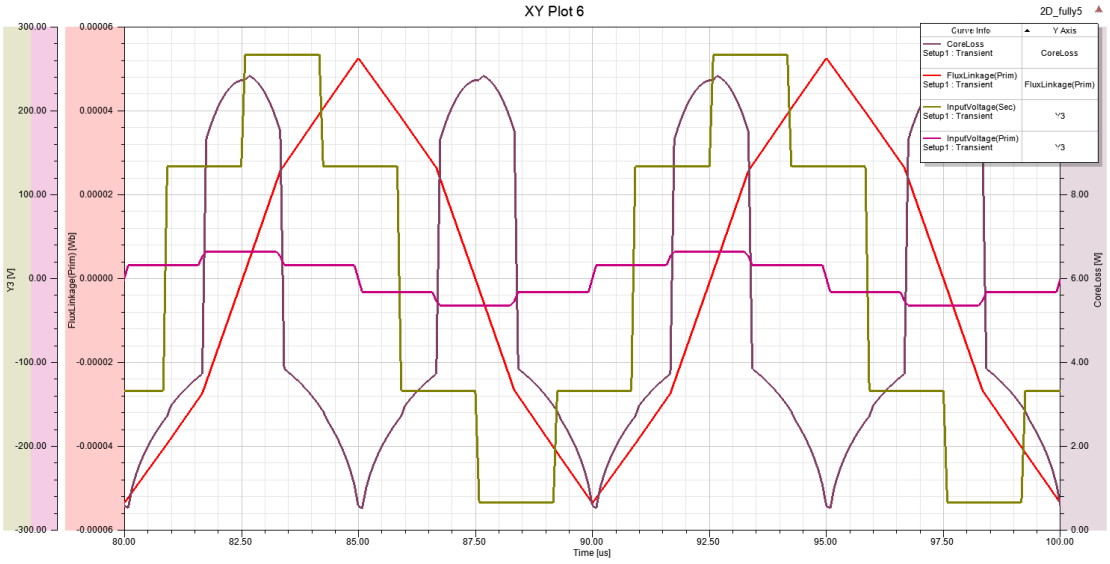


Fig. 5.17. Voltage, flux linkage and core loss waveforms of the designed transformer.

The instantaneous core loss density changes with the gradient $|dB(t)/dt|$. The maximum core loss occurs when $|dB(t)/dt|$ approaches its maximum. In this case, the maximum core loss is achieved when the flux linkage is zero. The core loss distribution is shown in Fig. 5.18.

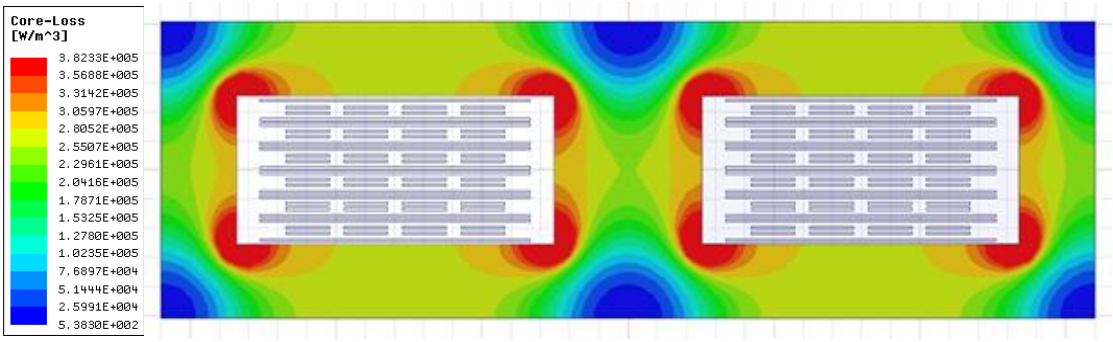


Fig. 5.18. Core loss density distribution of fully-interleaved winding.

The winding stack arrangement of the designed transformer is shown in Fig. 5.19. The window utilization factor is achieved at 0.293. The primary and secondary windings are located on the top and bottom layers of the same PCB, thus only one type of PCB is needed, which is very simple and cost effective to construct.

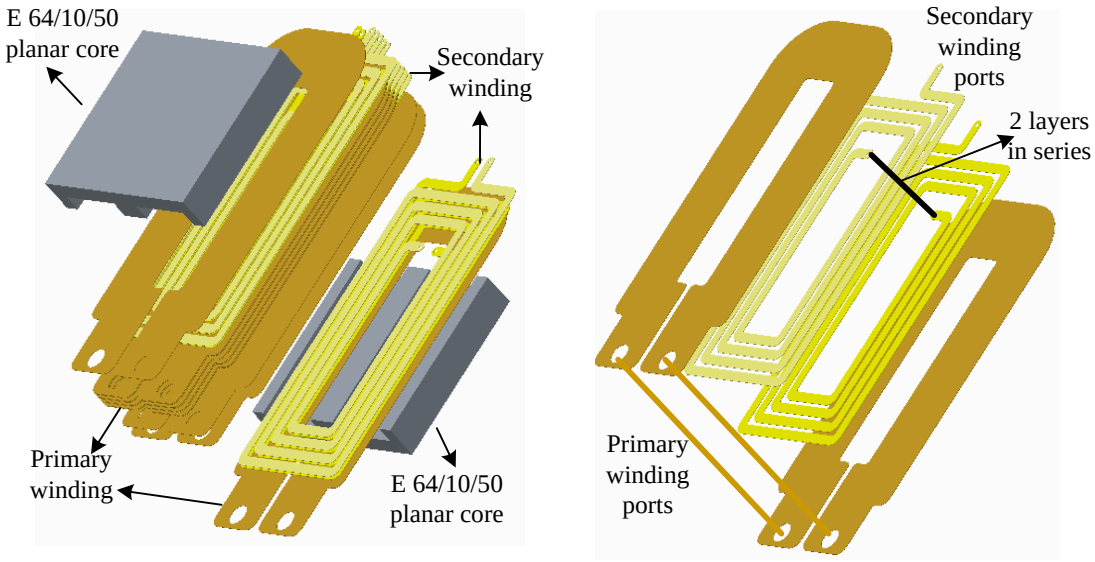


Fig. 5.19. Winding stack arrangement of the designed transformer.

From the studies above, the simulated core loss is slightly lower than analytical result. However, the winding loss is much higher than analytical result, which will lead to excessive heat generation under heavy load condition. As a result, an aluminum case is

designed and machined to enhance the heat dissipation capability of the transformer, which will be introduced in Chapter 6.

5.6. SUMMARY

In this chapter, the planar transformer design for three-phase DAB converter is presented. The magnetic core selection and the effects of winding arrangement are discussed in detail. A single-phase PCB based planar transformer is designed with minimum complexity of construction.

The magnetic core is selected based on the transformer apparent power. The waveform coefficient and maximum flux density are specified for this particular design under the constraints of saturation and specific core loss.

Planar winding traces and the winding interleave arrangement are designed. The AC resistance, leakage inductance and stray capacitance with different winding arrangement are calculated analytically and numerically using Maxwell 2D and 3D simulations.

Chapter 6
EXPERIMENTAL VERIFICATION

6.1. TRANSFORMER PROTOTYPE

The PCB based windings, transformer assembly, aluminum case and the final assembly are shown in Fig. 6.1. The aluminum case works as a heat sink to help dissipate the heat. Additionally, the aluminum case also holds the transformer together and provides pressure on the EE core.

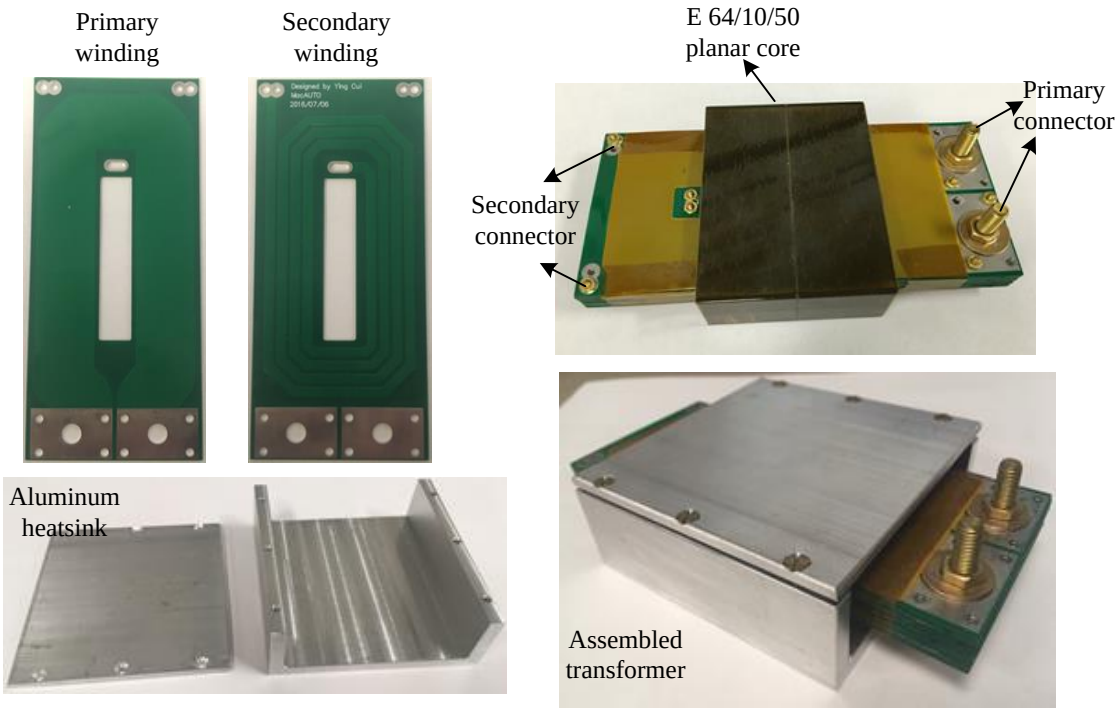


Fig. 6.1. Photo of designed PCB winding and assembled transformer.

6.2. TRANSFOREMR PARAMETER MEASUREMENT

The standard methods to measure the transformer parameters include the DC test, the short circuit (SC) test and the Open circuit (OC) test. DC test is applied to measure the DC resistance, SC test is used to measure the equivalent leakage inductance, and OC test is used to measure the magnetizing inductance [39, 70]. A Bench LCR/ESR meter (model 889B) is applied here for the OC and SC tests.

The SC test is applied to the secondary side such that total leakage inductance referred to the secondary side can be directly measured. The terminal connection and the equivalent circuit are shown in Fig. 6.2. When the primary winding is short circuited, the total impedance of the primary side, including the winding resistance and leakage inductance, is significantly lower than the magnetizing inductance, hence the impedance of the magnetizing inductance can be neglected, and the measured inductance corresponds to the total leakage inductance referred to the secondary side. However, the measured leakage inductance is very sensitive to the length and thickness of the strip copper which short the primary winding. The measurement shows 2 to 4 μH measurement change with different strip copper, which makes the measurement of leakage inductance not accurate.

$$L_{k2\_eq} = L_{k2} + L_{k1}^{'} = L_{k2} + L_{k1} \cdot n^2 \tag{6.1}$$

The OC test is also applied to the secondary windings to extract the magnetizing inductance. The terminal connection and the equivalent circuit are shown in Fig. 6.3. The measured inductance corresponds to the total self-inductance of the secondary winding, i.e., the magnetizing inductance and secondary leakage inductance. Nevertheless, in this

case, the leakage inductance is negligible compared to the magnetizing inductance. Hence, the measured value is considered as the magnetizing inductance.

The inter-winding capacitance is also obtained by impose voltage between the primary and secondary winding directly. The terminal connection and the equivalent circuit are shown in Fig. 6.4. Because the primary winding only has one turn, there is no intra-winding capacitance. On the secondary side, the intra-winding capacitance is obtained by impose voltage on the secondary side.

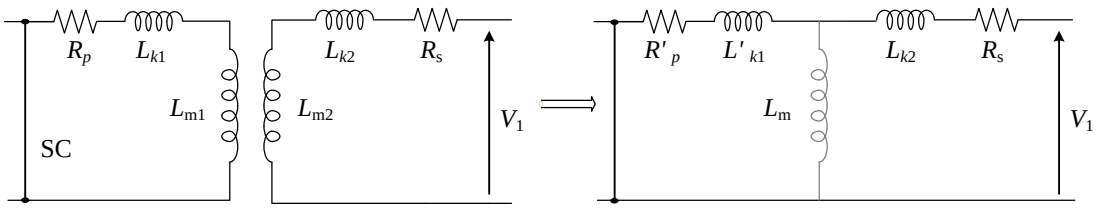


Fig. 6.2. Equivalent leakage inductance measurement by SC test.

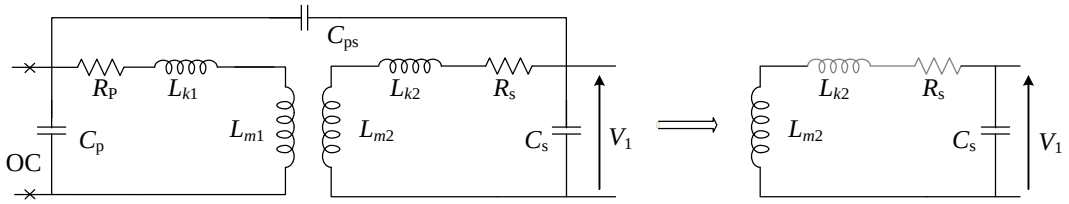


Fig. 6.3. Magnetizing inductance and intra-winding capacitance measurement by OC test.

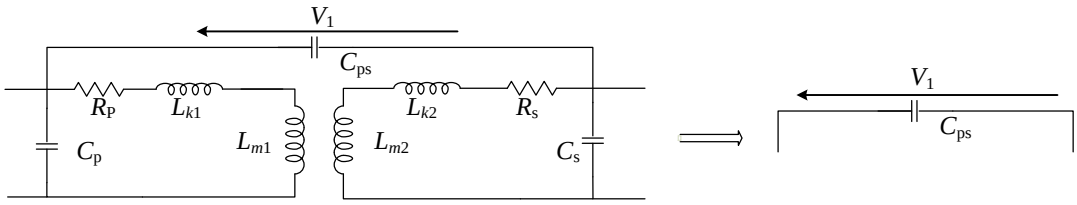


Fig. 6.4. Inter-winding capacitance measurement.

The measured parameters are shown in Table 6.1, where parameters obtained from theoretical calculation and FEA simulation are also listed for comparison.

Table 6.1 Transformer parameters

Parameters	calculation	simulation	measurement
L_{m2} (μH)	778	826.86	803.6
L_{k2_eq} (μH)	N/A	0.195	N/A
R_{dc_s}(mΩ)	9.2	N/A	12
C_{ps} (nF)	4.0	2.25	3.11
C_s (nF)	1.0	1.93	3.16

6.3. THREE-PHASE DUAL ACTIVE BRIDGE CONVERTER TEST

The transformer is tested in a 3 kW three-phase DAB converter prototype built in the lab, which has the same input voltage and output voltage range. The leakage inductance is optimized following the methodology proposed in Chapter 4.

The optimal value of the selectable parameters of the three-phase DAB converter are chosen as f = 100 kHz and L_k = 30 μH, which are designed with the consideration of peak/RMS current of the switching devices, ripple current of the capacitors and system efficiency. The designed parameters guarantee ZVS at 3 kW within the input voltage range, and high converter efficiency can be achieved.

The test setup is shown in Fig. 6.5. The designed transformers are connected with Y-Y configuration, and they are installed between the AC interface of primary and secondary bridges. The LV side of the converter is connected to DC power supply and the HV side is connected with resistive load. Hence the power transfers from LV side to HV side. The converter is controlled by DSP TI TMS320F28377D.

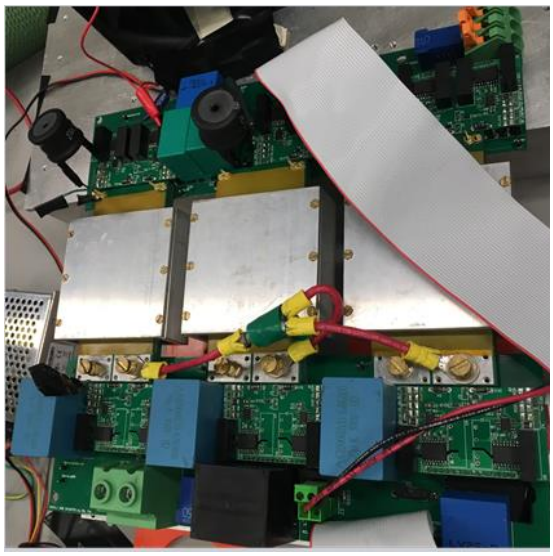
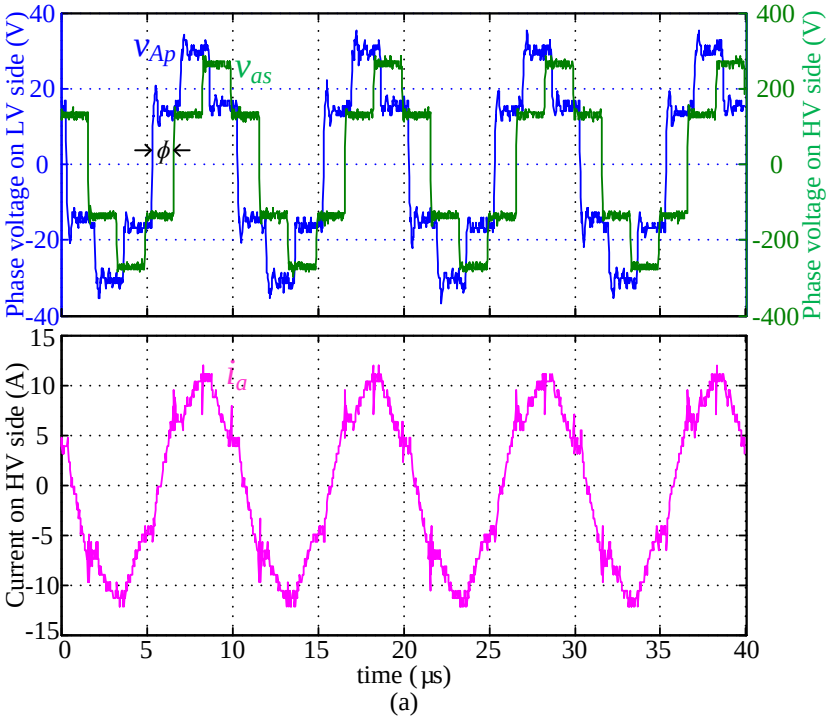


Fig. 6.5. Picture of the three-phase DAB converter prototype.

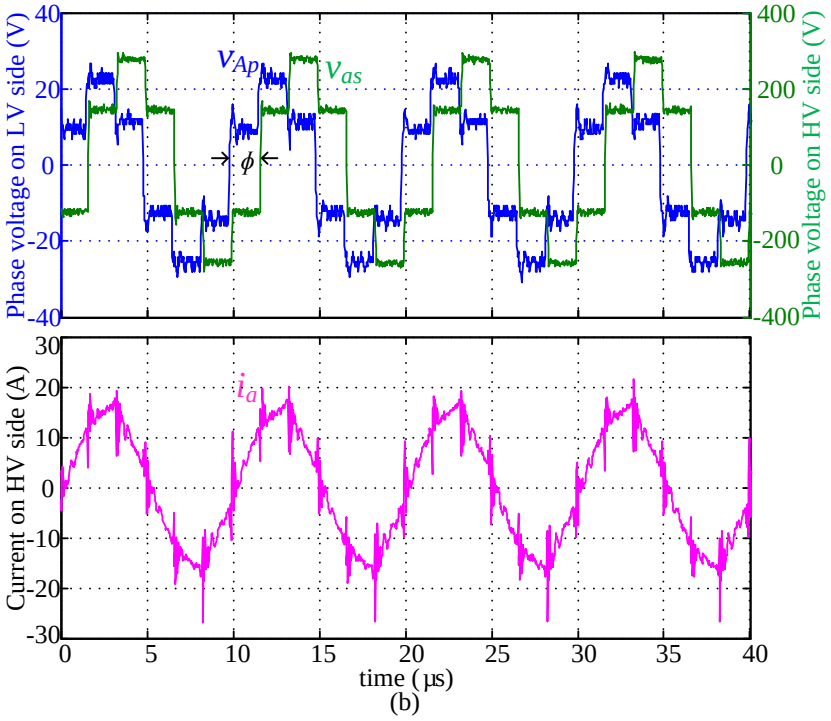
6.3.1. Voltage and Current Waveforms

The DAB converter prototype is tested at full load (3 kW) with different input voltages. At nominal operating point (V_1 = 48 V, V_2 = 400 V), the measured phase voltages of primary and secondary side (v_{Ap} and v_{as}) are shown in Fig. 6.6 (a). The phase shift between primary and secondary side along with the corresponding current i_a in the same phase are also depicted in Fig. 6.6 (a). The measured phase voltages are six-step, and the measured current matches the theoretical waveform in Fig. 3.2.

The converter is also tested under minimum and maximum input voltages, i.e., V_1 = 40 V and 56 V. The voltage and current waveforms are depicted in Fig. 6.6 (b) and (c). At the same output power, lower input voltage corresponds to larger phase shift between two bridges, and the current is also higher.


Phase voltage on LV side (V)
Phase voltage on HV side (V)
v_{Ap}
v_{as}
ϕ
Current on HV side (A)
i_a
time (μs)

(a)


Phase voltage on LV side (V)
Phase voltage on HV side (V)
v_{Ap}
v_{as}
ϕ
Current on HV side (A)
i_a
time (μs)

(b)

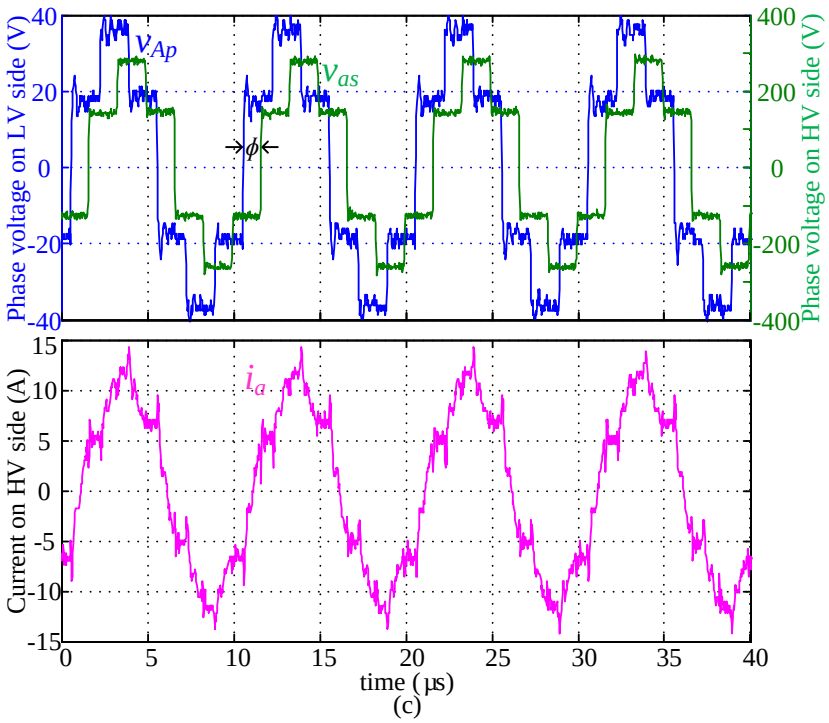


Fig. 6.6. Voltage and current waveforms of (a) 48/400 V, (b) 40/400 V and (c) 56/400 V operating at 3 kW.

The three-phase current waveforms are also measured and they are shown in Fig. 6.7. It is observed that the current in three phases are very close to each other, though not identical. This is possibly be caused by the unbalanced leakage inductance in three phases.

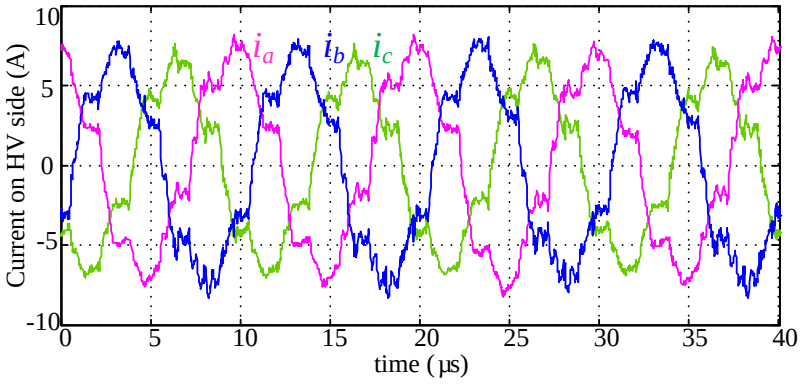
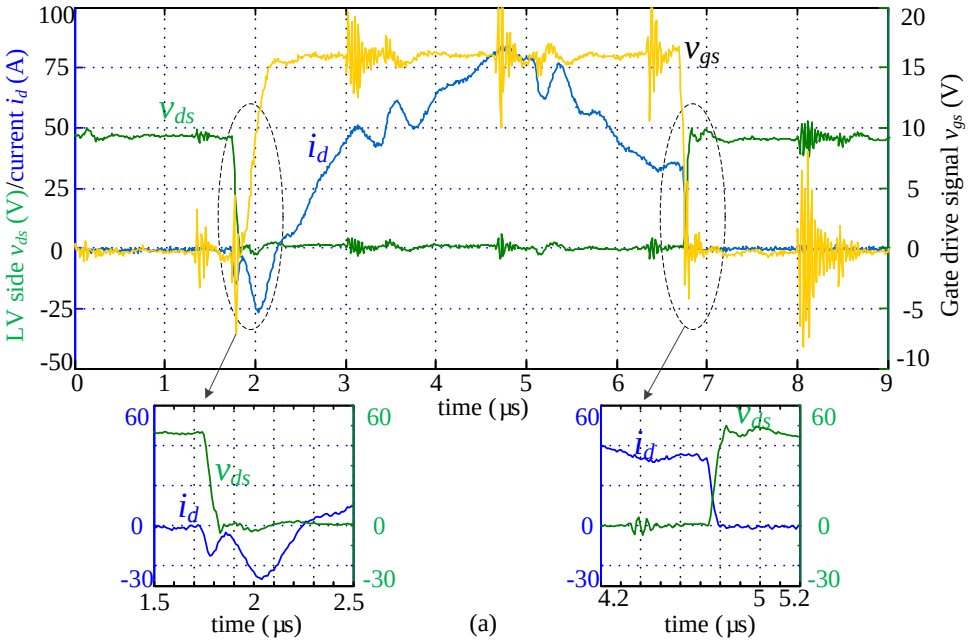


Fig. 6.7. Current waveforms of three phases operating at 48/400 V 2.4 kW.

6.3.2. Zero-Voltage-Switching Verification

Full Load Operation

The gate drive signal v_{gs} and voltage across the switches v_{ds} together with the current i_d flowing through the switches are measured to validate the ZVS behavior of the converter. At nominal operating voltage (V_1 = 48 V), the voltage and current waveforms of LV and HV side at full load are shown in Fig. 6.8 (a) and (b), respectively. At turn-on instant, v_{ds} is decreased to zero before v_{gs} began to increase. The negative current i_d flows through the body diode, and ZVS turn-on is achieved. Zero turn-on losses exist on both LV and HV side. At the turn-off instant, the current i_d drops to a small value before the voltage v_{ds} began to increase, hence the turn-off losses are also very small. At other input voltage levels, the measured waveforms are very similar and not given here.



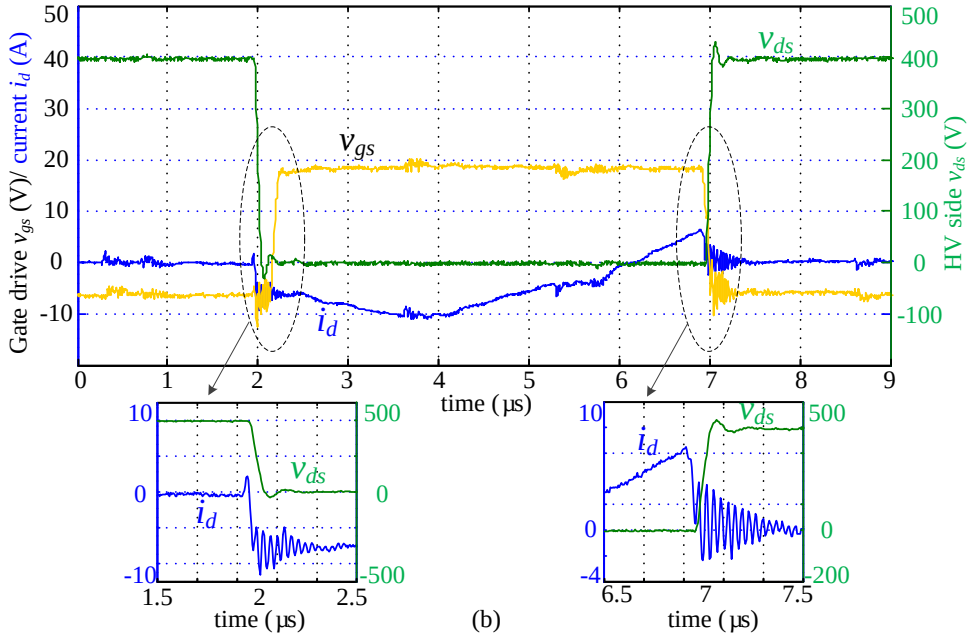


Fig. 6.8. Voltage and current waveforms of switching behavior on (a) LV and (b) HV side at full load.

Half Load Operation

The voltage and current of the switches are also measured at half load (1.6 kW) to demonstrate the ZVS behavior of the converter. The voltage and current waveforms are shown in Fig. 6.9 – Fig. 6.11, corresponding to V_1 = 48 V, 40V and 56 V, respectively. When V_1 = 48 V, on HV side, the negative current i_d shows that ZVS turn-on is achieved; on LV side, the intersection between v_{ds} and i_d is negligible, thus LV ZVS turn-on is also achieved. When V_1 = 40 V, ZVS turn-on is realized on HV side only. When V_1 = 56 V, LV ZVS can be achieved while hard switching happens at HV side, as shown in Fig. 6.11. By comparing the current waveforms in Fig. 6.9 – Fig. 6.11, at lower input voltage (V_1 = 40 V), the current through the switches is higher, which contributes to the conduction loss. At the turn-off instant, the current i_d drops to zero before v_{ds} begin to increase, thus turn-off loss is also negligible.

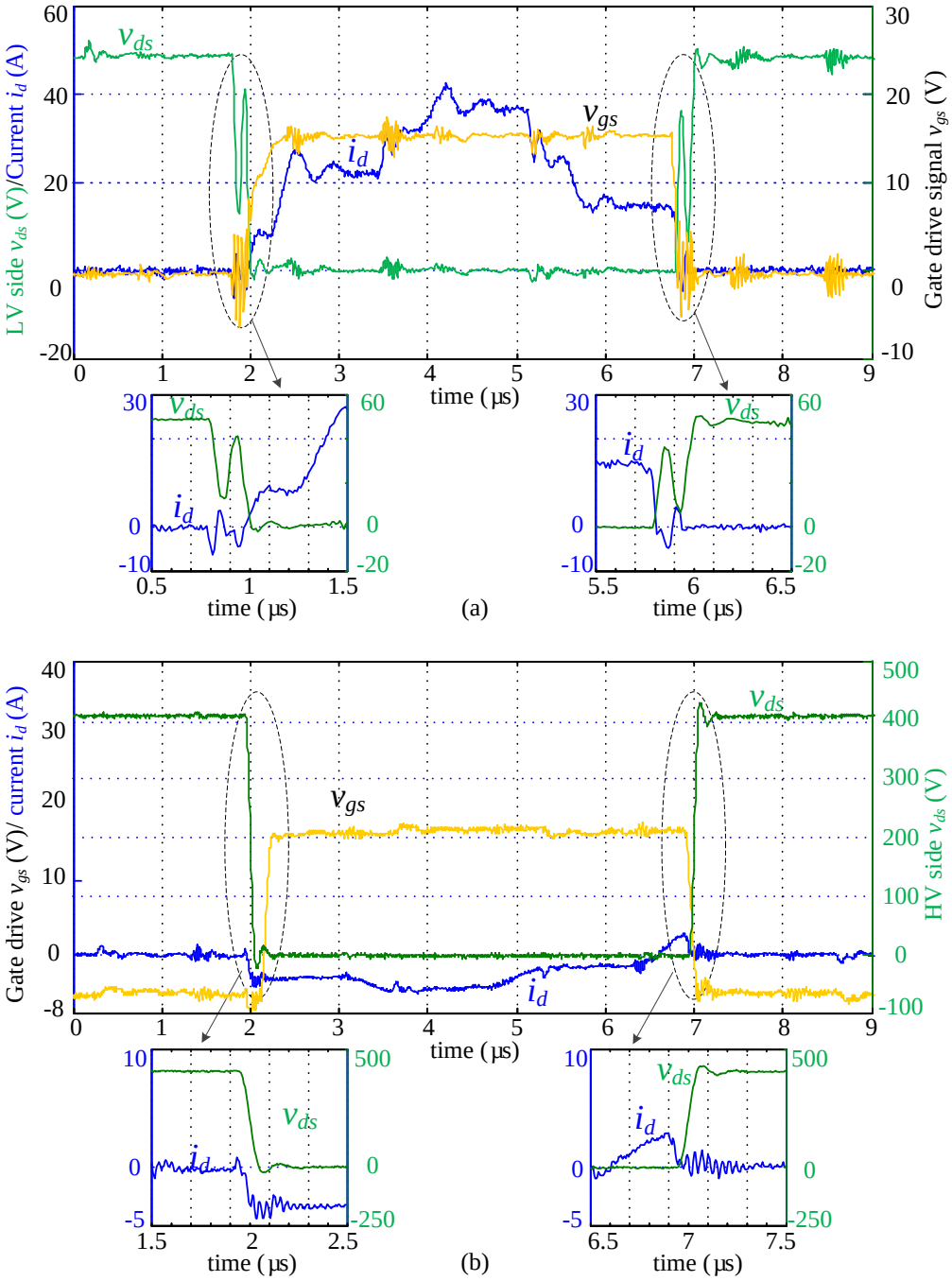


Fig. 6.9. Voltage and current waveforms on (a) LV and (b) HV side operating at V_1 = 48V, 1.6 kW.

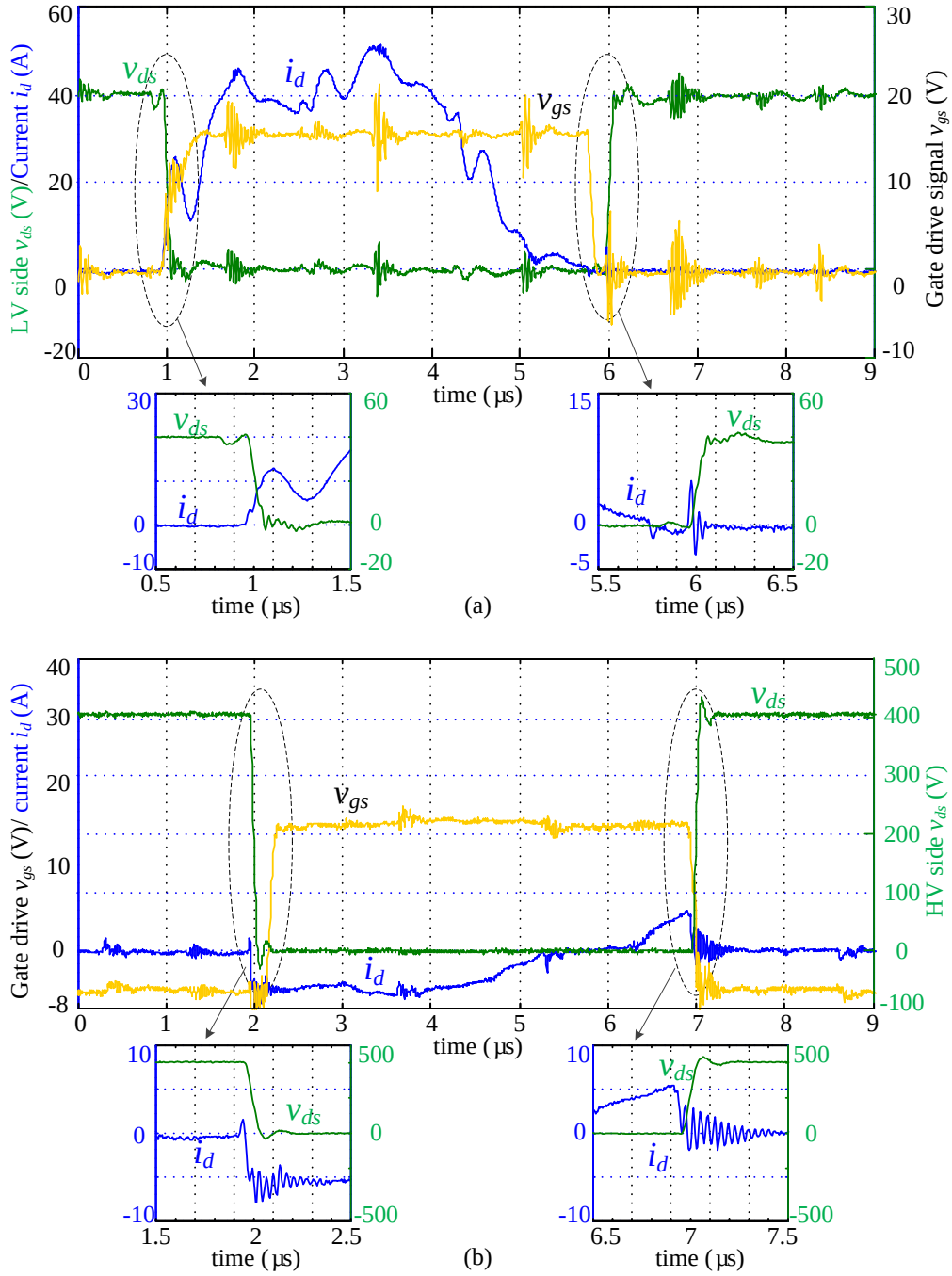


Fig. 6.10. Voltage and current waveforms on (a) LV and (b) HV side operating at V_1 = 40V, 1.6 kW.

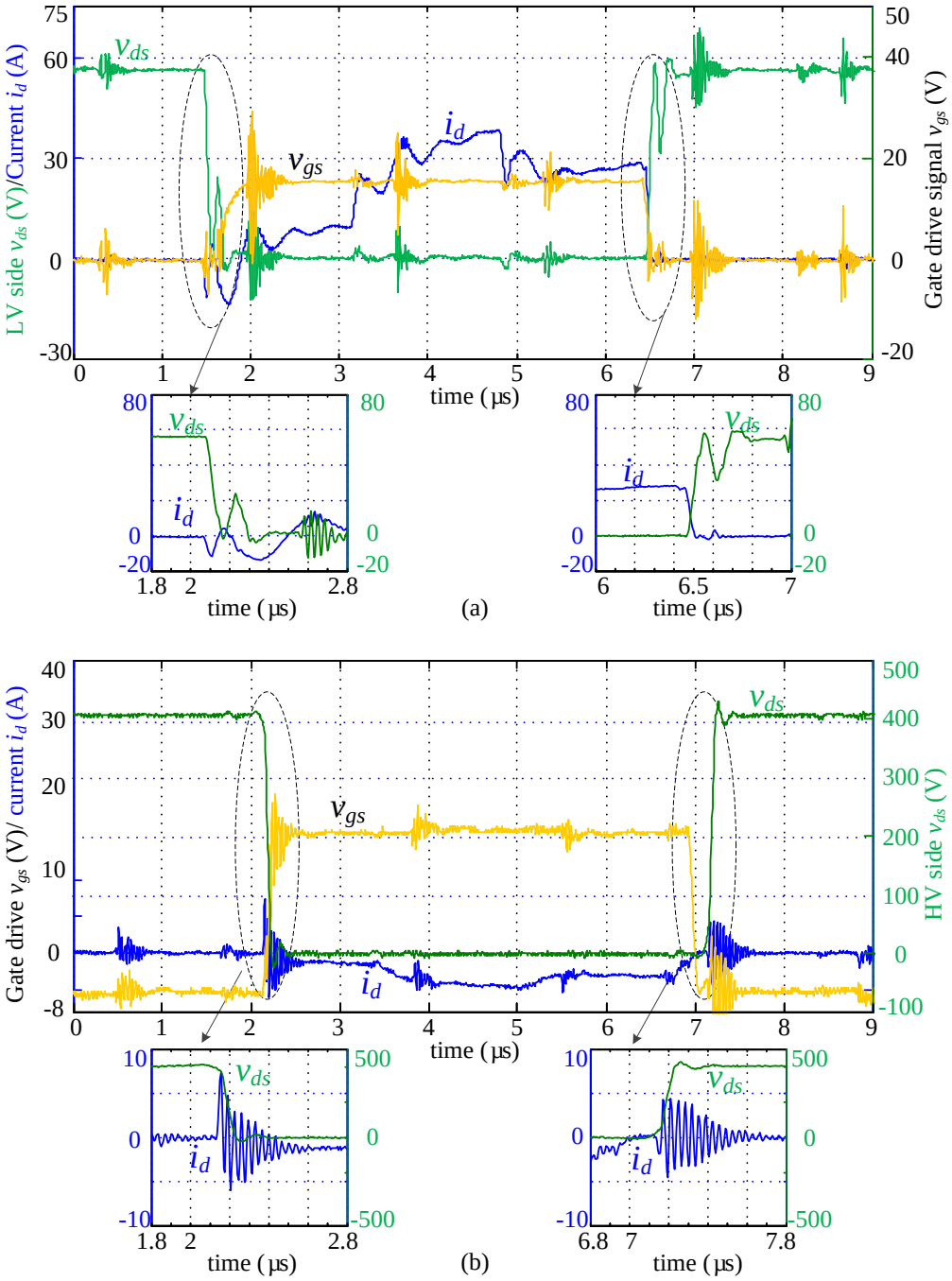
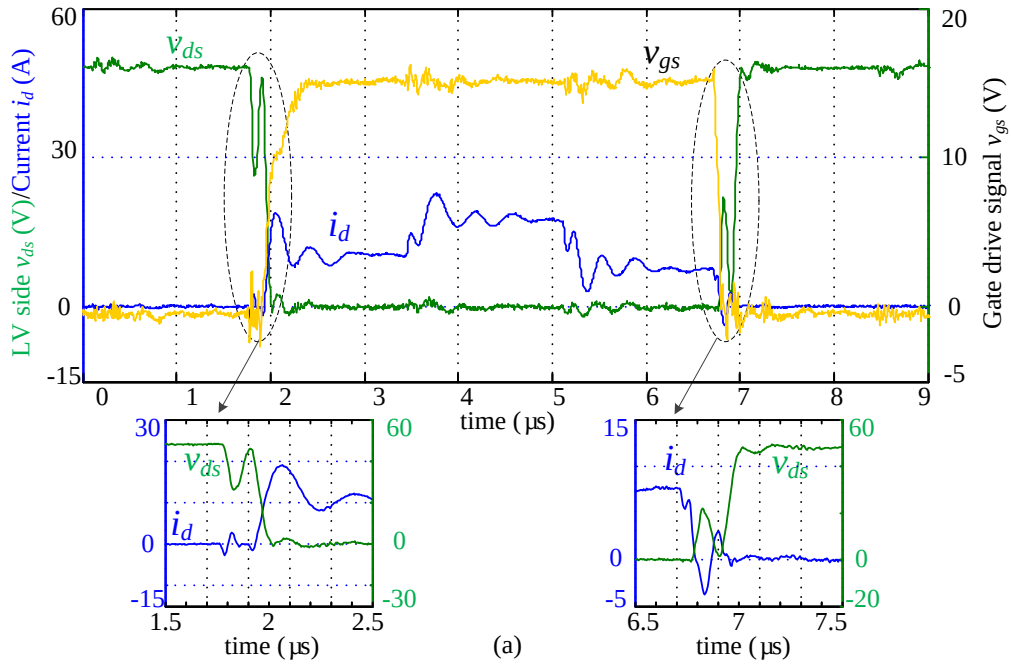


Fig. 6.11. Voltage and current waveforms on (a) LV and (b) HV side operating at V_1 = 56V, 1.6 kW.

Light Load Operation

ZVS operation of the converter is also tested at 800W as light load operation under different input voltage. The measured voltage (v_{ds} and v_{gs}) and current (i_d) waveforms on LV and HV side are shown in Fig. 6.12 – Fig. 6.14, corresponding to V_1 = 48 V, 40V and 56 V, respectively. At nominal input voltage (V_1 = 48 V), ZVS turn-on is achieved on HV side because the current is negative. On LV side, the switch is turned on with positive current i_d flowing through it before the voltage v_{ds} drops to zero, which indicates ZVS turn-on is not achieved. At V_1 = 40 V, ZVS turn-on is also realized on HV side. However, a larger intersection between i_d and v_{ds} is observed on LV side, which results in higher turn-on loss. At V_1 = 56 V, ZVS turn-on is only realized on LV side. The ZVS behavior is consistent with the ZVS analysis in Fig. 4.1. Similar to the full load and half load condition, ZVS turn-off is achieved on both side and results in negligible turn-off loss.



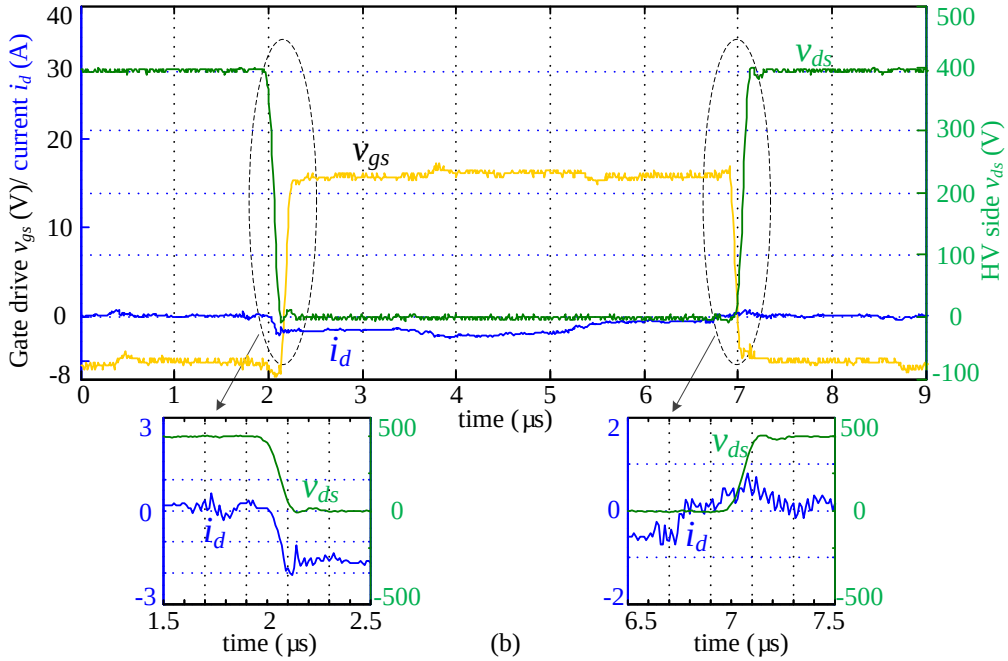
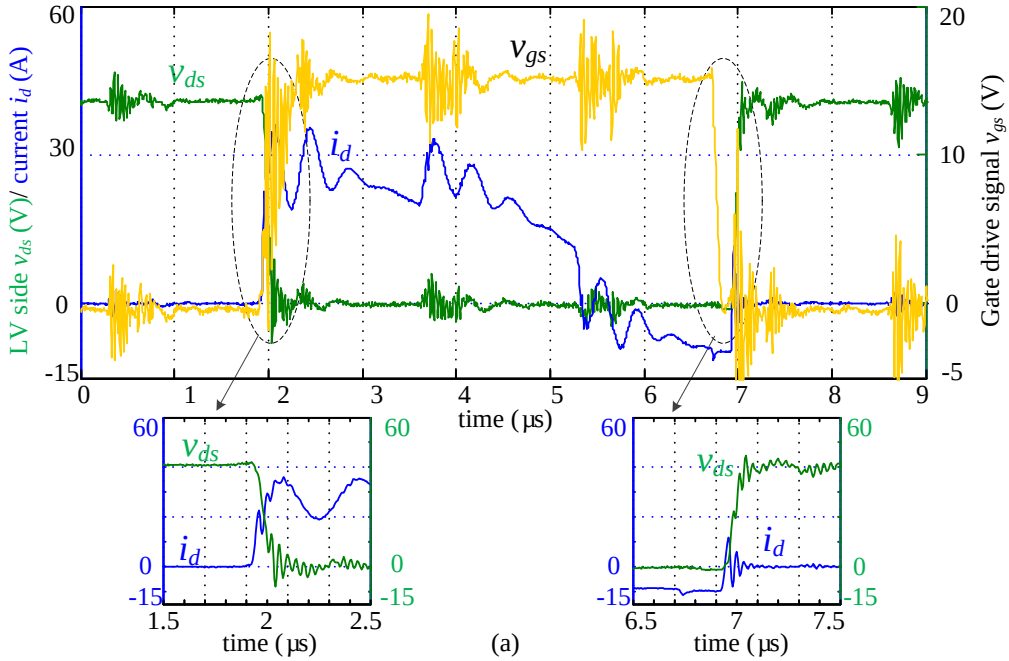


Fig. 6.12. Voltage and current waveforms on (a) LV and (b) HV side operating at V_1 = 48V, 800 W.



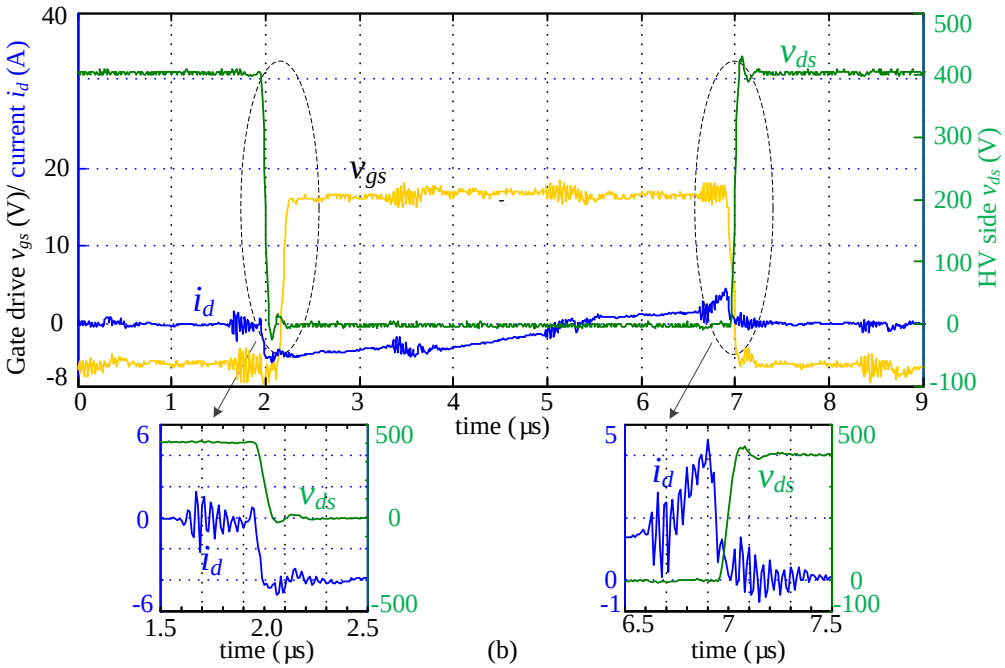
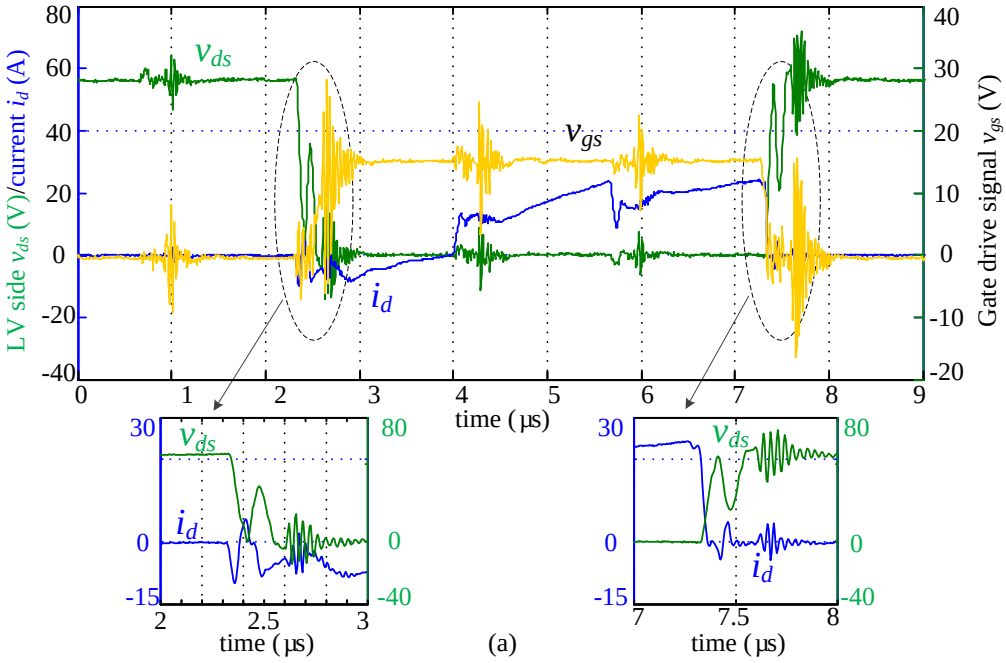


Fig. 6.13. Voltage and current waveforms on (a) LV and (b) HV side operating at V_1 = 40V, 800 W.



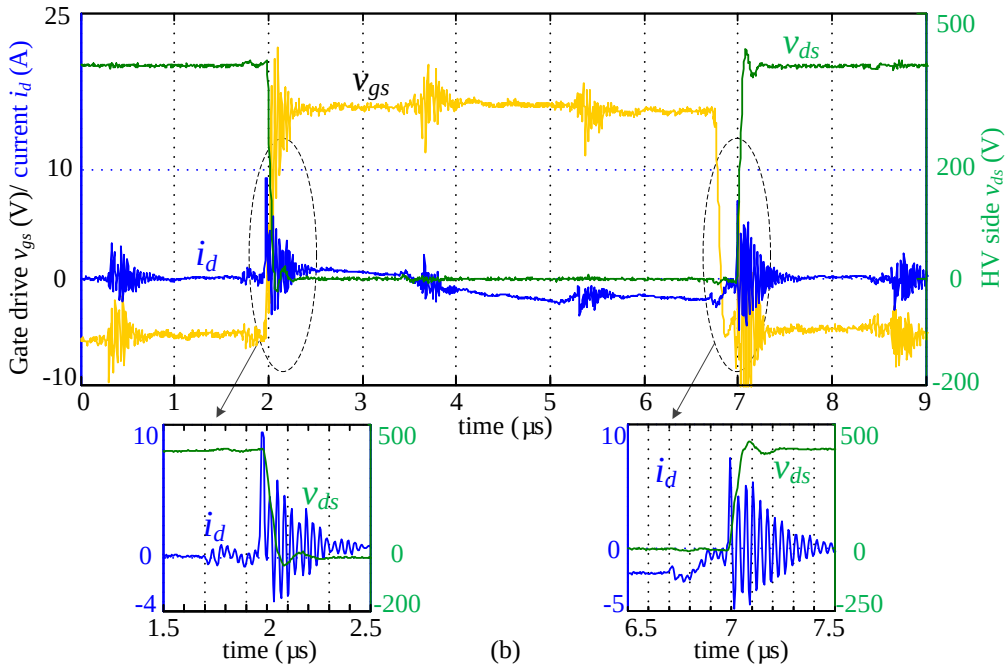


Fig. 6.14. Voltage and current waveforms on (a) LV and (b) HV side operating at V_1 = 56V, 800 W.

6.3.3. Efficiency Test

The converter efficiency is obtained by measuring the input and output power of the LV and HV sides of the converter. YOKOGAWA WT 1800 high performance power analyzer and LEM ULTRASTAB 867-200I precision current transducer are used in the measurement. To reduce the error caused by the current sensor range, multiple turns of current are measured. The converter efficiency is calculated by

$$\eta = \frac{P_o}{P_{in}} = \frac{V_2 I_2}{V_1 I_1} \tag{6.2}$$

where P_o and P_{in} are the output and input power, V_1, I_1 are the input voltage and current, and V_2, I_2 are the output voltage and current.

The efficiency of the converter is measured at three different input voltages. The results are shown in Fig. 6.15. The efficiency curve shows similar trends throughout the

power range. 92% efficiency is achieved over a wide power range (1 kW – 3 kW) at all input voltage levels. At light load when power ranges from 400 W to 800 W, the efficiency drops dramatically. This is expected as the designed parameters f and L_k are not optimal for light load operation.

Highest efficiency is achieved at nominal input voltage (V_1 = 48 V), because the voltage ratio between the HV and LV matches the transformer turn ratio. The efficiency is above 94% from 1 kW to 2.4 kW and the peak efficiency is 95%. At V_1 = 40 V, the efficiency is lower under heavy load due to higher current flowing through the switches and transformer. At V_1 = 56 V, the converter efficiency also drops significantly at low power level mainly due to switching loss on HV side.

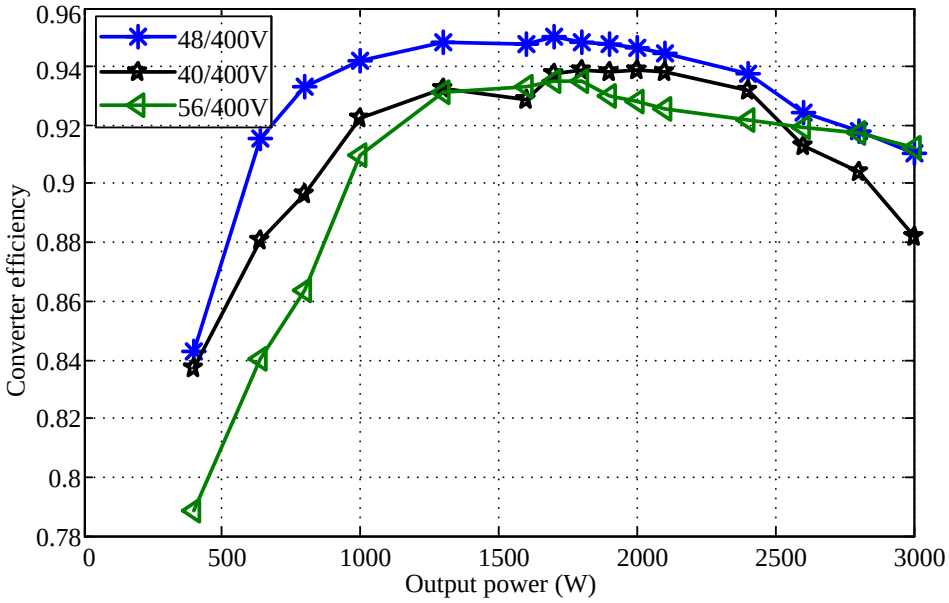


Fig. 6.15. Measured converter efficiency at different input voltage and power level.

6.4. SUMMARY

This chapter presents experimental verification of designed transformer and the performance of three-phase DAB converter. LCR meter is used to measure the parameters of the transformer prototype. The three-phase DAB converter is tested at different input voltage and power levels. The converter operating principle is validated experimentally. The ZVS behavior and converter efficiency are also measured under different operating conditions.

Chapter 7
CONCLUSIONS

This thesis has presented a parameter design guideline for three-phase DAB converter, which takes the converter efficiency as well as the capacitor ripple current into account. The design method of planar transformer for the three-phase DAB converter is also studied and the details are presented. The parameters of a three-phase DAB converter for smart home application are optimized and a planar transformer is designed and prototyped accordingly.

An overview of planar transformer is conducted in Chapter 2. The advantages and disadvantages of planar transformer are discussed. The transformer core loss, copper loss, leakage inductance and stray capacitance are included.

The configuration of three-phase DAB converter and its operating scheme under phase shift modulation are reviewed in Chapter 3. The ZVS condition, current stress on switching devices and capacitors are analyzed in closed form. It is discovered that the parameters f and L_k together influence the converter performances, which needs to be considered as one combined factor in the converter design.

In Chapter 4, the impact of the selectable parameters (n, f, L_k) on the converter performances, including the ZVS range, RMS current of switches and DC capacitors, are investigated based on the analysis in Chapter 3. A new parameter fL is defined to simplify the analysis from 3 dimensions to 2 dimensions. Taking the constraints of transformer design into consideration, the feasible range of parameters (n, f, L_k) is determined. At

different voltage and power levels, the converter efficiency is analyzed in the feasible range, and the optimized values of (n, f, L_k) are determined.

A planar transformer is designed for the three-phase DAB converter in Chapter 5. The parameters for core selection are derived based on the operating scheme. The winding design is accomplished with the consideration of copper loss and leakage inductance, and the stray capacitance is also calculated. ANSYS Maxwell simulations are employed to help the design and derive the transformer parameters.

Finally, three single-phase planar transformers are built and tested in a three-phase DAB converter. The transformer parameters, including DC winding resistance, magnetizing inductance on the secondary side, and stray capacitance are measured. The planar transformer based three-phase DAB converter is validated experimentally.

FURTHER WORK SUGGESTED

Possible future works related to the research topics in this thesis are as follows:

1) More accurate estimation of switching loss can be established to improve the efficiency study in Chapter 4. Experimental waveforms at the switching instant can be used to help improve the switching loss model.
2) The AC resistance obtained from Maxwell 3D simulation is discovered to be much higher than theoretical value, and heatsink case is employed to enhance the heat dissipation capability. A thermal network needs to be developed to validate the power capability of the transformer.

3) Higher value of fL is desired to achieve higher efficiency at low power levels. Since L_k is fixed, frequency variation can be applied to help improve the converter efficiency. More investigation is required to determine the frequency value within different power ranges.

PUBLICATIONS

Y. Cui, R. Hou, P. Malysz and A. Emadi, "Improved combined modulation strategy for dual active bridge converter in electrified vehicles," published in *Proc. 2017 IEEE Transportation Electrification Conference and Expo (ITEC 2017)*, 2017.

Y. Cui, D. Wang, and A. Emadi, "Three-phase dual active bridge converter design considerations," accepted by *2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society (IECON 2017)*, 2017.

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