Loss Minimization using Linear Soft-Switching with Wide Bandgap Devices in Efficient High-Frequency DC-DC Converters

LOSS MINIMIZATION USING LINEAR SOFT-SWITCHING WITH WIDE BANDGAP DEVICES IN EFFICIENT HIGH-FREQUENCY DC-DC CONVERTERS

BY

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Dedicated to my parents for their constant support and motivation for me to excel in all my endeavors.

Abstract

Switching power converters are used for voltage-level conversions in various applications. With progress in device technology, the wide bandgap devices offer smaller parasitic capacitances and lower switching energy values. Efforts are being made to use higher frequencies to realize more power-dense converters with smaller volume of the passive components. The maximum switching frequency is limited by the ability of the switching devices to dissipate their losses. This thesis presents a framework for the design and modeling of efficient high-frequency high-energy density DC/DC converters using soft-switching techniques with wide bandgap devices. Various online switching loss estimation methods are discussed demonstrating improved accuracies, enabling a better cooling system design. A comparison is made between various soft-switching methods and the use of turn-off snubbers to reduce the switching losses. A linear soft-switching method is proposed and validated for both SiC and GaN devices. A simplified analytical model is presented which predicts the actual turn-off losses very accurately. This method is found to enable buck converter operation at 1 MHz switching frequency and 1 kW output power with switch losses smaller by nearly five times from a hard-switched system using GaN devices. These losses are further reduced with the use of SiC schottky diodes, with future scope to achieve higher efficiency using custom inductors designed for high frequency and current ripple values.

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List of abbreviations

AC	Alternating Current
BJT	Bipolar Junction Transistor
DC	Direct Current
GaN	Gallium-Nitride
HSW	Hard-Switching
Hz	Hertz
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal-Oxide-Semiconductor-Field-Effect-Transistor
PWM	Pulse Width Modulation
QSC	Quasi-Square-Wave-Converter
Si	Silicon
SiC	Silicon-Carbide
SSW	Soft-Switching
W	Watt
WBG	Wide Bandgap
ZCS	Zero-Current Switching
ZCT	Zero-Current-Transition
ZVS	Zero-Voltage Switching
ZVT	Zero-Voltage-Transition

List of symbols

C_{DS}	MOSFET Drain-Source Capacitance
C_{gs}	MOSFET Parasitic Gate-Source Capacitance
C_{gd}/C_{rss}	MOSFET Reverse Transfer Capacitance
C_{iss}	MOSFET Parasitic Input Capacitance
C_{oss}	MOSFET Parasitic Output Capacitance
D	Duty Cycle
E_{cond}	Conduction Energy Loss
E_{on}	Turn-on Switching Energy Loss
E_{off}	Turn-off Switching Energy Loss
E_{rr}	Diode Reverse Recovery Energy Loss
F_{sw}	Switching Frequency
I_{CDS}	Drain-Source Capacitance Current
I_{DS}	Drain-Source Current
I_{gate}	Gate Current
I_L	Inductor Current
I_{out}	Output Current
L	Inductance

M_1	High-Side MOSFET
M_2	Low-Side MOSFET
η	Power Conversion Efficiency
P_{out}	Output Power
Q_{rr}	Diode Reverse Recovery Charge
$R_{ds(on)}$	MOSFET On-State Resistance
R_g	Gate Resistance
t_{fi}	Current Fall-Time
t_{fu}	Voltage Fall-Time
T_j	Junction Temperature
T_{off}	Switching Off-Time
T_{on}	Switching On-Time
t_{ri}	Current Rise-Time
t_{ru}	Voltage Rise-Time
T_{sw}	Switching Time-Period
V_{drive}	Gate Driver On-State Voltage
$V_{drive,off}$	Gate Driver Off-State Voltage
V_{DS}	Drain-Source Voltage
V_{gd}	Gate-Drain Voltage
V_{gs}	Gate-Source Voltage
V_{in}	Input Voltage
V_{out}	Output Voltage
V_p	Miller-Plateau Voltage
V_{th}	Gate-Source Threshold Voltage

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Chapter 1

Introduction

1.1 Power Electronic Converters

Power electronic converters are used to match the properties of the electrical source with the load. These converters may be categorized based on various parameters. Depending on the nature of the source and the load, there exist DC-DC, AC-DC and DC-AC converters. Various applications may need electrical isolation between the source and the load, or between the different outputs [1], giving rise to isolated and non-isolated converters. There also exist other topologies derived from the basic topologies, as listed in Fig. 1.1 [2–4].

For the case of DC-DC converters, linear regulators were initially developed which vary the impedance of a pass transistor to regulate to a constant output voltage [3]. A basic circuit for a linear regulator using a bipolar junction transistor (BJT) is shown in Fig. 1.2 [5].

Linear regulators can only generate a smaller output voltage from a higher input voltage. The voltage differential between the input and output terminals is placed

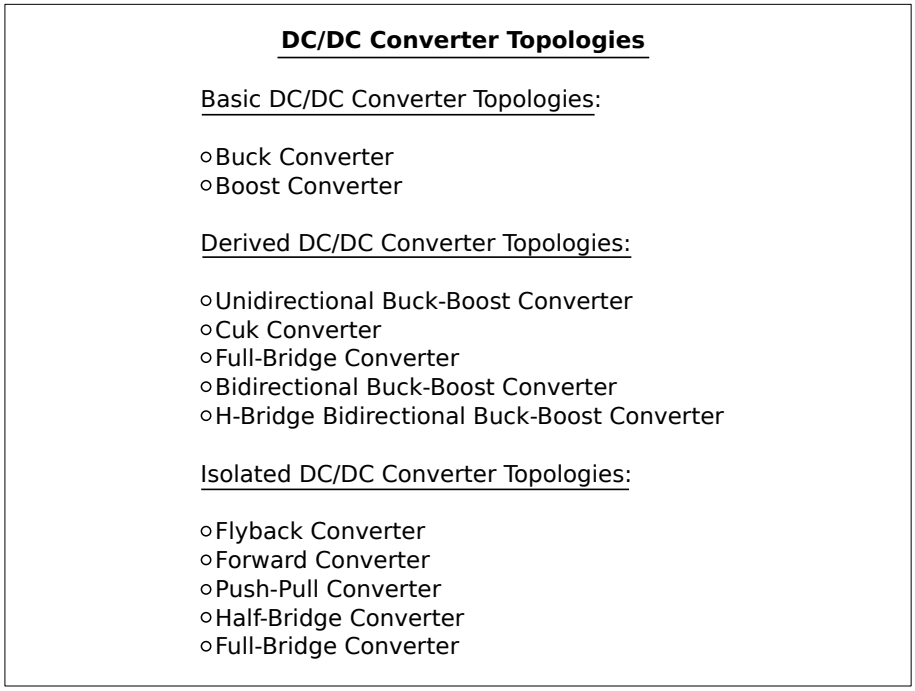


Figure 1.1: DC/DC Converter Topologies

across the pass transistor Q_1. The power loss in a device is equal to the product of its voltage and the current through it [3,6]. Since the input and output current is equal in a linear regulator, its efficiency is independent of the current, and is given by:

$$\eta = \frac{V_{out}}{V_{in}} \tag{1.1}$$

where V_{in} and V_{out} are the input and output voltage, respectively. It is due to this reason that a linear regulator exhibits a very low conversion efficiency and needs a large heat sink to dissipate its losses. It is generally preferred for use in low noise applications or in cases with small output current I_{out}.

In pursuit of the design of high efficiency converters, switching power converters were designed which used a BJT or an insulated gate bipolar transistor (IGBT) as a

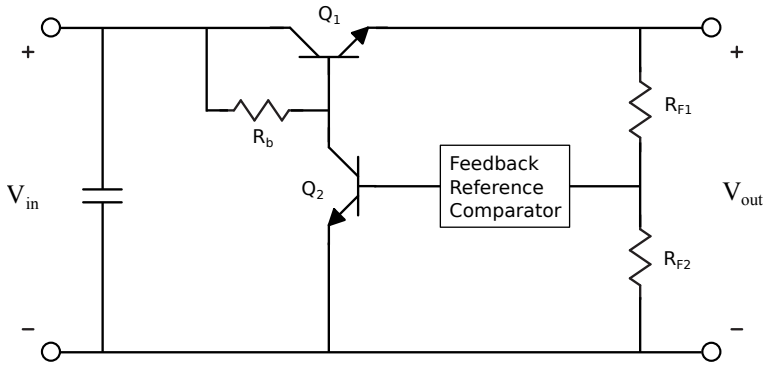


Figure 1.2: Linear Regulator

switch in the saturation and cut-off regions [2,3,7]. An IGBT offers benefits of a high impedance input at its gate terminal with minimal gate drive current requirements. A buck converter is one of the simplest switching DC-DC converters, shown in Fig. 1.3.

A buck converter is a non-isolated DC-DC converter used to obtain a smaller V_{out} from a higher V_{in}. These converters enabled power densities of the order of 1.2 kW/L [3]. The switching frequencies with BJTs and IGBTs were limited to a few kilohertz (kHz). This is because of their slow recovery from saturation region and losses due to the presence of a tail current [8]. The advent of Silicon (Si)

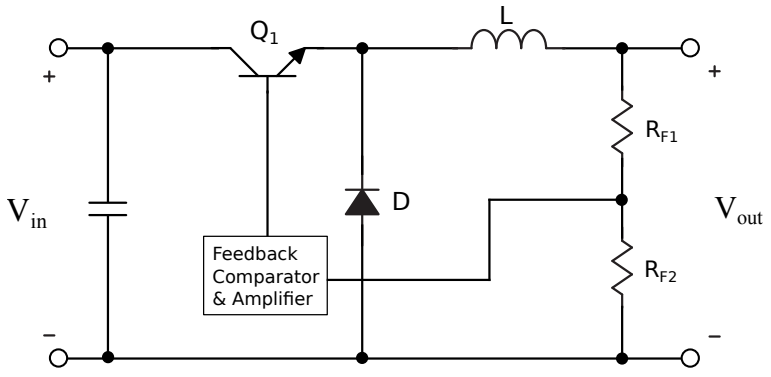


Figure 1.3: Buck Converter Topology

Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs) enabled operation at higher switching frequencies (F_{sw}) of the order of few tens of kHz due to their faster switching characteristics [9]. Moreover, MOSFETs being voltage controlled devices exhibiting an ideally infinite input impedance at their gate terminal imposed minimal gate drive requirements [10, 11].

1.2 Losses in Power Converters

There are two types of losses in the switches in a power converter - conduction losses and switching losses. Conduction losses result from the current through the device and the voltage across it in the on-state condition. The switching losses occur due to the overlap of the device terminal voltage and current during transition between the on/off operating conditions [2, 3, 12].

Fig. 1.4(a) depicts a scenario where both voltage and current transition begin at the same time, while Fig. 1.4(b) shows the worst-case scenario when the device voltage stays at its peak value during current transition from zero to its maximum value at the time of turn-on, and vice versa during turn-off in a power converter [3]. A real-world application exhibits a switching behavior in between these two conditions.

MOSFET power loss estimation is critical for the estimation of efficiency, thermal management and cooling system design. With advancements towards use of higher switching frequencies for power dense designs [13], the switching losses begin to dominate the conduction losses in MOSFETs. While conduction losses are relatively easier to calculate, switching energies may not be provided at all operating points in MOSFET datasheets. Switching losses in a device are a result of overlap of voltage (V_{DS}) across the device and current (I_{DS}) through the device during a switching

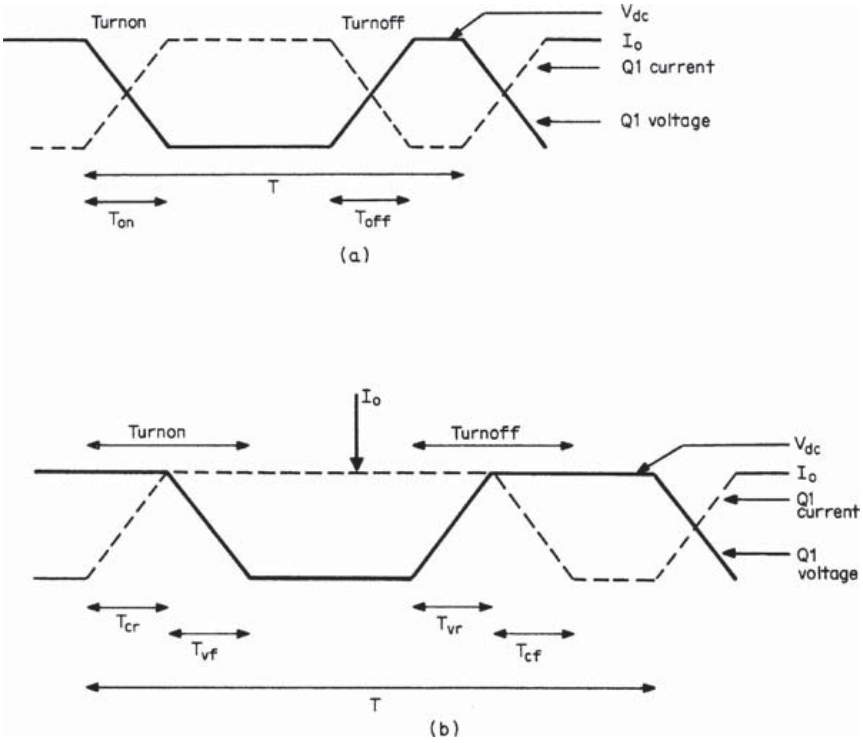


Image Source : Switching Power Supply Design, by Abraham I. Pressman

Figure 1.4: Switching Waveforms

transition [7, 12, 14].

1.2.1 Switching Loss Estimation

There exist a variety of methods for estimation of switching losses. The physical models use finite-element simulations and report best results, but could take a few days to run [15]. The behavioral models use circuit simulation softwares, such as SPICE, are faster than physical models, but exhibit long run times due to small time step. On the other hand, MOSFET switching losses can be calculated easily using analytical models, which are mathematical models based on equivalent circuits, and use values from the product datasheets. In order to estimate switching energies, it

is required to calculate rise-time and fall-time for both V_{DS} and I_{DS}. While on one hand, current rise-time (t_{ri}) and fall-time (t_{fi}) are relatively easier to calculate using MOSFET input capacitance (C_{iss}) [16], on the other hand, computation of voltage rise-time (t_{ru}) and fall-time (t_{fu}) uses reverse transfer capacitance (C_{rss}), which varies significantly as V_{DS} reduces from its maximum ($V_{DS,max}$) to its minimum ($V_{DS(on)}$) value during turn-on, and vice-versa during turn-off [17, 18]. This thesis discusses various methods for arriving at an approximate value for C_{rss}, including a method for the estimation of switching transition times and switching energies for Silicon-Carbide (SiC) MOSFETs with varying miller plateau voltage [19]. Fig. 1.5 shows the characteristic non-flat miller plateau region as seen in CAS300M12BM2 from Cree Inc. [20].

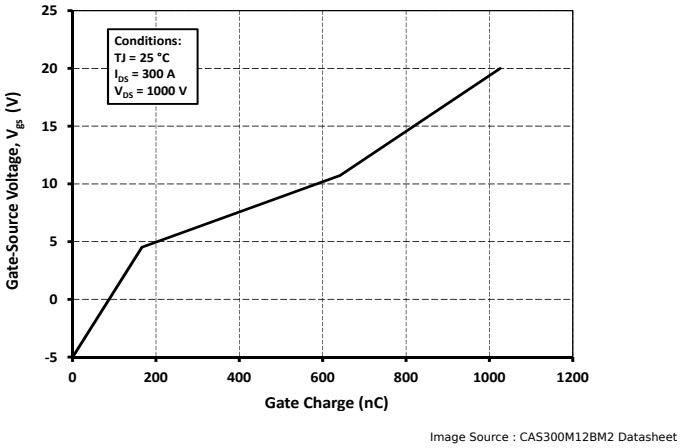


Figure 1.5: Varying Miller Plateau Voltage

Soft-switching techniques are discussed in [21, 22] used to reduce the switching losses in a power converter. These methods turn-on/off the device when either of the voltage or current are at a very small value. This reduces the degree of the voltage/current overlap and the magnitude of the switching energy. The soft-switching techniques overcome the challenges of resonant converters with their large circulating

energy and the associated conduction losses. There exist a variety of soft-switching techniques, discussed below.

1.3 Soft-Switching Methods

The soft-switching techniques could be divided into two main categories based on the parameter being minimized at the switching instant: voltage or current [21–24].

1.3.1 Zero-Voltage Switching (ZVS)

This method minimizes the voltage across a switching device during a switching instant. ZVS quasi-square-wave-converters (QSC) include a resonant inductor to discharge the device's junction capacitance, as shown in Fig. 1.6(a). This method is used in the control of the flyback switcher UCC28700 from Texas Instruments. While on one hand, this method results in minimum voltage stresses on both the switches in the half-bridge in a power converter, on the other hand, it results in high transistor peak currents increasing conduction losses by nearly 40%.

Another technique used in ZVS-PWM converters includes an auxiliary switch across the resonant inductor, as shown in Fig. 1.6(b). This switch creates a free-wheeling stage within the previous quasi-resonant operation. This method suffers from the disadvantages of high voltage stress on the power switch and the rectifier diode not being operated in favorable switching condition.

While the above techniques use a series resonant inductor for ZVS operation with its associated conduction losses, another method used in zero-voltage-transition (ZVT) PWM converters includes a shunt resonant network across the power switch,

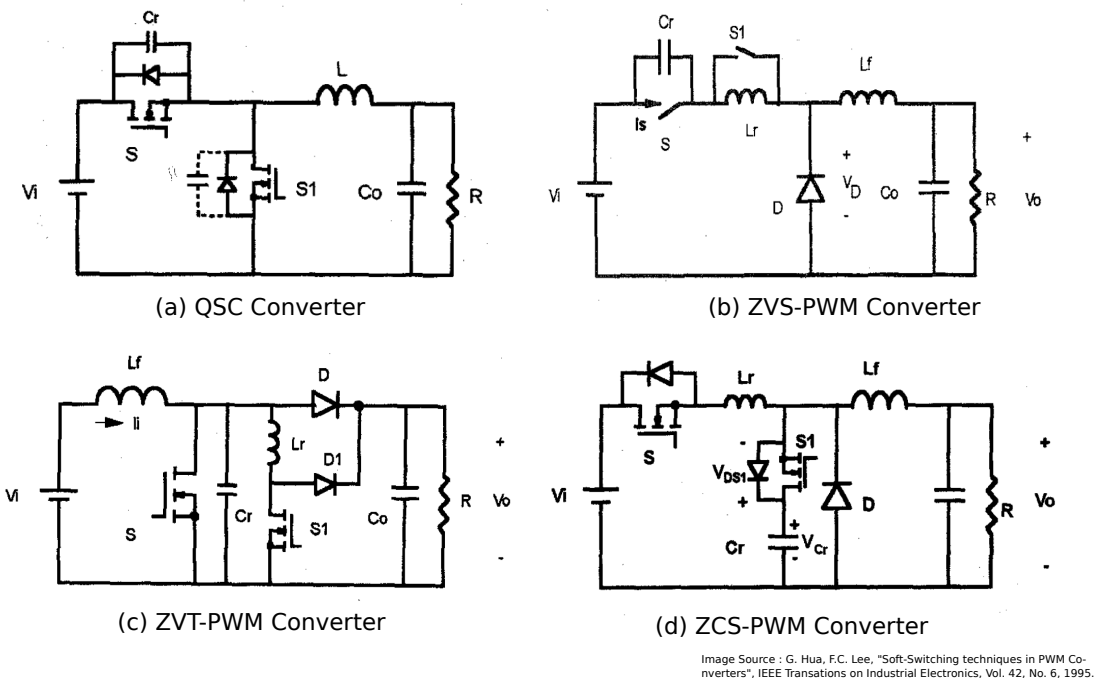


Figure 1.6: Soft-Switching Methods

shown in Fig. 1.6(c). This technique requires use of a greater number of additional components and involves hard-switching in the auxiliary switch.

1.3.2 Zero-Current Switching (ZCS)

These techniques were developed to minimize the losses in converters using IGBTs with their tail current [8]. Fig. 1.6(d) shows the schematic of a ZCS-PWM converter. While this method implements ZCS for the power transistor and ZVS for the rectifier diode, it results in high voltage stress on the rectifier diode with large parasitic ringing with the power switch. It is also sensitive to line voltage and load change. Another method used in zero-current-transition (ZCT) PWM converters includes a resonant branch active for a short switching-transition time to reduce the losses in the main switch. This method also suffers from its drawback of hard-switched operation of the

rectifier diode and its associated losses, requiring use of a fast-recovery diode.

Apart from these soft-switching techniques, the emerging wide bandgap (WBG) devices offer lower switching energy values than the conventional Si-devices. This is due to their small die size and parasitic capacitances [25,26]. These devices extend the operating range of switching frequencies to a few hundred kHz. This thesis discusses the use of a linear soft-switching method to extend the switching frequency range of power converters with WBG devices to MHz range, while remaining within the device power dissipation limits and a given cooling system design [27]. In this method, the turn-on losses are replaced with smaller turn-off losses [28–30]. These turn-off losses are further reduced with the use of additional capacitors between the MOSFET drain-source terminals.

1.4 Thesis Outline

This thesis develops a framework for the design of efficient high-frequency high energy density power converters. The report begins with a discussion of the online switching loss estimation methods, include a novel approach for an improved estimation of the switching losses in power converters using SiC devices with non-flat miller plateau region in Chapter 2. The linear soft-switching method is introduced and the reduction in the turn-off losses with the use of additional capacitors is demonstrated in Chapter 3. The transition time estimation relations for MOSFET current and the analytical model for the estimation of the turn-off losses are used to realize a buck converter with Gallium-Nitride (GaN) devices operating at 1 MHz and 1 kW output power in Chapter 4. Finally, the results are summarized in Chapter 5 including a discussion of the scope of future work.

Chapter 2

MOSFET Switching Behavior and Loss Estimation Strategies for Wide Bandgap Devices

MOSFET power loss estimation is critical for the estimation of efficiency, thermal management and cooling system design. There exist a variety of methods for the estimation of switching losses. In order to estimate the switching energies using analytical models, it is required to calculate rise-time and fall-time for both V_{DS} and I_{DS}. While on one hand, current rise-time t_{ri} and fall-time t_{fi} are relatively easier to calculate using MOSFET input capacitance C_{iss} [16], on the other hand, computation of voltage rise-time t_{ru} and fall-time t_{fu} uses reverse transfer capacitance C_{rss}, which varies significantly as V_{DS} reduces from its maximum $V_{DS,max}$ to its minimum value $V_{DS(on)}$ during turn-on, and vice-versa during turn-off [17]. An existing method estimates t_{ru} and t_{fu} using an approximate value for C_{rss}, which does not

represent the reverse transfer capacitance well in the whole transition interval, introducing large errors. Another method divides the transition intervals into very small sub-intervals, assumes C_{rss} remains constant in each of these intervals, and calculates transition times for each of these periods [18]. These values are later added together to determine the total rise- and fall-time as V_{DS} varies between its initial and final values.

A characteristic feature of few SiC MOSFETs is their non-flat miller plateau voltage V_p, shown in Fig. 1.5 for CAS300M12BM2 from Cree Inc. [20, 31]. During t_{fu}, when V_{DS} is dropping towards $V_{DS(on)}$, almost all of the gate current flows through C_{rss}, but the gate-source voltage V_{GS} also increases slightly for a few SiC devices. This makes it difficult to determine a unique V_p value to calculate switching transition times and switching losses using the existing methods. This thesis introduces a method for the estimation of t_{ru} and t_{fu} for SiC MOSFETs with varying miller plateau voltage. These values are then used to compute the switching energies during turn-on (E_{on}) and turn-off (E_{off}). Simulation and experimental results are presented later in this chapter for the calculation of the transition times and the switching losses for SiC devices using this method.

2.1 WBG Device Switching Characteristics

A few of the SiC MOSFETs differ in switching behavior from Silicon (Si) MOSFETS. Switching behavior for Si-FETs are described in [18, 32] and shown in Fig. 2.1(a) and Fig. 2.1(b). Fig. 2.1(a) shows the ideal switching waveforms for Si devices at the time of turn-on. When a gate drive voltage V_{drive} is applied, V_{gs} rises from zero to its threshold value V_{th}, with no conduction during this period. At this level,

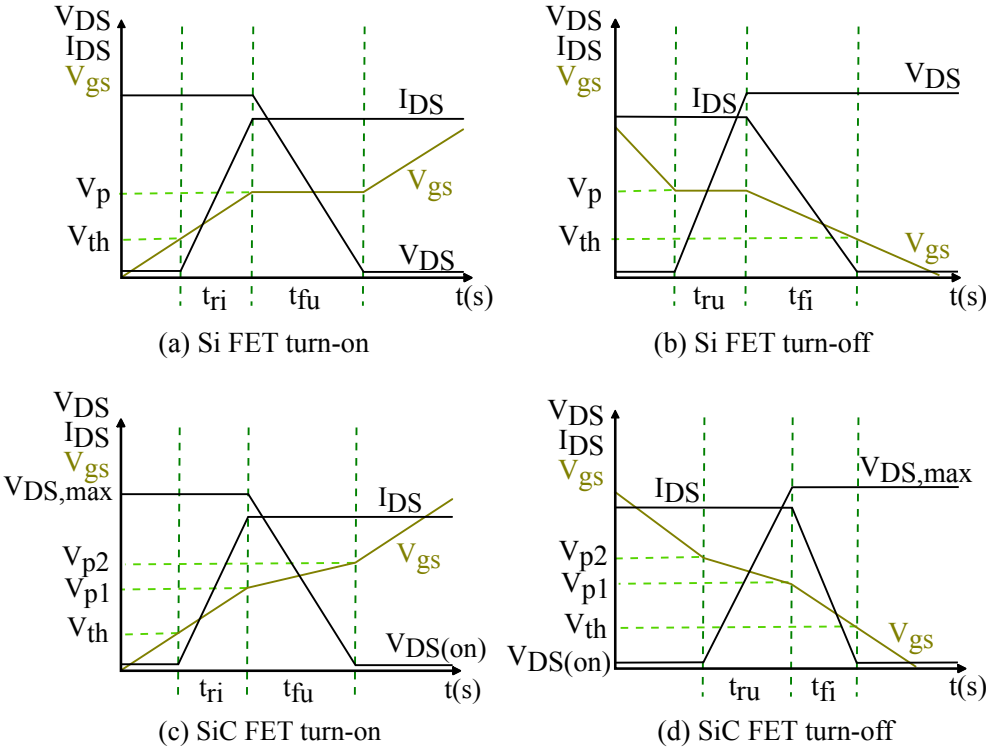


Figure 2.1: MOSFET Switching characteristics

the drain current begins to rise to the specification I_{DS} during t_{ri}, till V_{gs} reaches V_p. The gate voltage now remains constant at V_p, while V_{DS} reduces from $V_{DS,max}$ to switch-on value, $V_{DS,on}$, during t_{fu}. $V_{DS,on}$ is the product of MOSFET on-state resistance, $R_{ds(on)}$ and I_{DS}. Next, the gate voltage increases further to gate driver supply level, fully saturating the MOSFET. At the time of turn-off, as shown in Fig. 2.1(b), V_{DS} first increases from $V_{DS(on)}$ to $V_{DS,max}$ during t_{ru}, while gate-source voltage is at V_p, followed by reduction in I_{DS} to zero during t_{fi}, as V_{gs} reduces to V_{th} and zero, later. A similar behavior is observed in GaN MOSFETs. The switching behavior is different for a few of the SiC MOSFETs, such as CAS300M12BM2 from Cree Inc. As shown in Fig. 2.1(c) and Fig. 2.1(d), SiC MOSFETs exhibit a non-flat gate-plateau voltage region, with V_{gs} increasing from V_{p1} to V_{p2}, while V_{DS} reduces

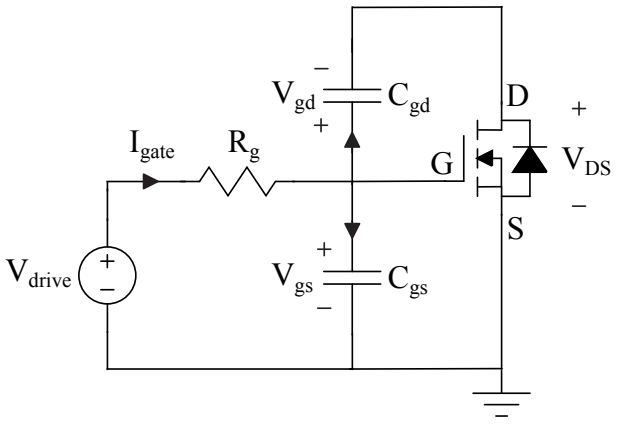


Figure 2.2: MOSFET gate charging and discharging equivalent circuit

to $V_{DS(on)}$ during turn-on, and vice-versa during turn-off, which makes it difficult to calculate switching losses, as given in [33].

Considering the MOSFET equivalent circuit of Fig. 2.2 [18], Eqs. 2.1 and 2.2 represent the gate current (I_{gate}). Since a MOSFET is a voltage controlled device [11], and offers very high input impedance, drive current from the gate driver through the gate resistance R_g flows through gate-source and gate-drain parasitic capacitances, C_{gs} and C_{gd} respectively, to charge and discharge them at turn-on and turn-off, respectively. Eliminating I_{gate} in Eqs. 2.1 and 2.2, along with Eqs. 2.3, 2.4 and 2.5, leads to Eq. 2.6, which is one of the equations used to estimate current and voltage transition times during device turn-on and turn-off [34].

$$I_{gate} = \frac{V_{drive} - V_{gs}}{R_g} \tag{2.1}$$

$$I_{gate} = C_{gs}\frac{dV_{gs}}{dt} + C_{gd}\frac{dV_{gd}}{dt} \tag{2.2}$$

but,

$$V_{gd} = V_{gs} - V_{DS} \tag{2.3}$$

and,

$$C_{iss} = C_{gs} + C_{gd} \tag{2.4}$$

$$C_{rss} = C_{gd} \tag{2.5}$$

$$\frac{V_{drive} - V_{gs}}{R_g} = C_{iss}\frac{dV_{gs}}{dt} - C_{rss}\frac{dV_{DS}}{dt} \tag{2.6}$$

Eq. 2.6 is solved for each of the transition intervals to calculate the V_{DS} and I_{DS} rise- and fall-times.

2.2 Switching Transition-Time Estimation

Depending on the switching characteristics of the MOSFETs, different methods are used to calculate the V_{DS} and I_{DS} transition times. The existing methods for Si- and GaN devices assume the time differential of V_{gs} as zero during V_{DS} transition and a relatively straightforward calculation for I_{DS} transition time independent of C_{rss} [18]. A proposed method accounts for the change in V_{gs} during V_{DS} transition [19]. These methods differ in their approximation of C_{rss} values for computation of the V_{DS} transition times for the case of constant V_{gs} in Si- and GaN devices and varying V_{gs} in SiC devices.

2.2.1 Si- and GaN Devices

Eq. 2.6 is solved for each of the time intervals to obtain the different switching transition times, as outlined below.

Drain-Source Current Rise-Time (t_{ri})

Fig. 2.1(a) shows the turn-on transient for a Si MOSFET. In the interval t_{ri}, V_{gs} increases from V_{th} to V_p, and I_{DS} increases from zero to its final value, $I_{DS,max}$. Since V_{DS} remains unchanged during this time, its derivative with time becomes zero, to give Eqs. 2.7 from Eq. 2.6:

$$\int_0^{t_{ri}} dt = \int_{V_{th}}^{V_p} \frac{R_g C_{iss}}{V_{drive} - V_{gs}} dV_{gs} \tag{2.7}$$

$$t_{ri} = R_g C_{iss} log_e \frac{V_{drive} - V_{th}}{V_{drive} - V_p} \tag{2.8}$$

Drain-Source Current Fall-Time (t_{fi})

Similar to calculations for t_{ri}, I_{DS} reduces from $I_{DS,max}$ to zero during t_{fi}, while V_{DS} remains constant at $V_{DS,max}$, giving Eq. 2.9 from Eq. 2.6:

$$\int_0^{t_{fi}} dt = \int_{V_p}^{V_{th}} \frac{R_g C_{iss}}{V_{drive} - V_{gs}} dV_{gs} \tag{2.9}$$

$$t_{fi} = R_g C_{iss} log_e \frac{V_{drive,off} - V_p}{V_{drive,off} - V_{th}} \tag{2.10}$$

Drain-Source Voltage Fall-Time (t_{fu})

Once I_{DS} reaches $I_{DS,max}$, V_{gs} remains unchanged at V_p while V_{DS} reduces from specification $V_{DS,max}$ to $V_{DS(on)}$. I_{DS} remains unchanged during this interval, indicated as t_{fu} in Fig. 2.1(a). From Eq. 2.6,

$$\int_0^{t_{fu}} dt = \int_{V_{DS,max}}^{V_{DS(on)}} \frac{R_g C_{rss}}{V_{gs} - V_{drive}} dV_{DS} \tag{2.11}$$

$$t_{fu} = (V_{DS,max} - V_{DS(on)}) \frac{R_g C_{rss}}{V_{drive} - V_p} \tag{2.12}$$

Drain-Source Voltage Rise-Time (t_{ru})

During MOSFET turn-off, similar transitions happen for V_{gs}, I_{DS} and V_{DS} as during device turn-on, but in reverse order. Fig. 2.1(b) shows the waveforms for device turn-off. V_{gs} remains unchanged at V_p and V_{DS} increases from $V_{DS(on)}$ to $V_{DS,max}$, giving Eq. 2.13 from Eq. 2.6,

$$\int_0^{t_{ru}} dt = \int_{V_{DS(on)}}^{V_{DS,max}} \frac{R_g C_{rss}}{V_{gs} - V_{drive}} dV_{DS} \tag{2.13}$$

$$t_{ru} = (V_{DS,max} - V_{DS(on)}) \frac{R_g C_{rss}}{V_p - V_{drive,off}} \tag{2.14}$$

The calculations for t_{fu} and t_{ru} using Eqs. 2.12 and 2.14 need value of C_{rss}, which varies considerably with change in V_{DS} between $V_{DS(on)}$ and $V_{DS,max}$. There exist methods which help to determine an approximate value of C_{rss} for computation of V_{DS} transition times [18]. A conventional approach, referred to as *Method* 1 in remainder of this chapter, approximates C_{rss} as the average of reverse transfer capacitance values, $C_{rss,n}$ and $C_{rss,1}$ in Fig. 2.3, at $V_{DS,max}$ and $V_{DS(on)}$, respectively.

Since the average value does not represent C_{rss} well in the full transition interval, this method introduces significant errors, as shown in later sections. An alternate approach, referred to as *Method* 2, divides the switching interval into very small

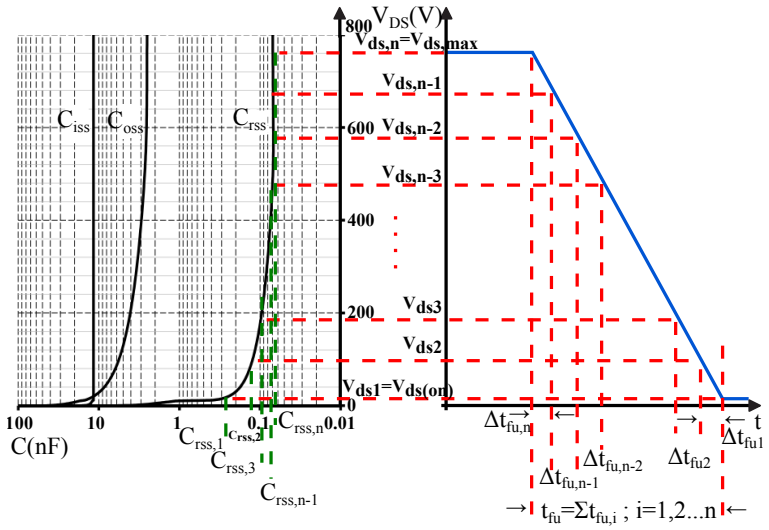


Figure 2.3: Variation of MOSFET parasitic capacitances with drain-source voltage

sub-intervals, as shown in Fig. 2.3 for Cree's CAS300M12BM2 half-bridge MOSFET product, and calculates V_{DS} transition time for each of these small sub-intervals. It is assumed that these sub-intervals are very small, and that C_{rss} remains constant during each of these periods. These individual transition times are added to obtain the total t_{ru} and t_{fu} values. Let us assume there exists only one intermediate level, $V_{DS,mid}$, for ease of understanding:

$$t_{fu} = (V_{DS,max} - V_{DS,mid} + V_{DS,mid} - V_{DS(on)}) \frac{R_g C_{rss}}{V_{drive} - V_p} \tag{2.15}$$

$$t_{fu} = (V_{DS,max} - V_{DS,mid}) \frac{R_g C_{rss1}}{V_{drive} - V_p} + (V_{DS,mid} - V_{DS(on)}) \frac{R_g C_{rss2}}{V_{drive} - V_p} \tag{2.16}$$

where C_{rss1} and C_{rss2} are the approximate values of reverse transfer capacitance, assumed constant for each of the sub-intervals, and represent C_{rss} well if these sub-intervals are infinitesimally small. Similar procedure is repeated for calculating t_{ru}.

2.2.2 SiC Devices

When using SiC MOSFETs, the gate-plateau voltage varies between V_{p1} and V_{p2} during V_{DS} transition interval, shown in Fig. 2.1(c) and Fig. 2.1(d).

Drain-Source Current Rise-Time (t_{ri})

Fig. 2.1(c) shows the turn-on instant for a SiC MOSFET. In the interval t_{ri}, V_{gs} increases from V_{th} to V_{p1}, and I_{DS} increases from zero to its final value, $I_{DS,max}$. Since V_{DS} remains unchanged during this time, its derivative with time becomes zero, to give Eq. 2.17 from Eq. 2.6:

$$\int_0^{t_{ri}} dt = \int_{V_{th}}^{V_{p1}} \frac{R_g C_{iss}}{V_{drive} - V_{gs}} dV_{gs} \tag{2.17}$$

$$t_{ri} = R_g C_{iss} log_e \frac{V_{drive} - V_{th}}{V_{drive} - V_{p1}} \tag{2.18}$$

Drain-Source Current Fall-Time (t_{fi})

Similar to calculations for t_{ri}, I_{DS} reduces from $I_{DS,max}$ to zero during t_{fi}, while V_{DS} remains constant at $V_{DS,max}$, giving Eq. 2.19 from Eq. 2.6:

$$\int_0^{t_{fi}} dt = \int_{V_{p1}}^{V_{th}} \frac{R_g C_{iss}}{V_{drive} - V_{gs}} dV_{gs} \tag{2.19}$$

$$t_{fi} = R_g C_{iss} log_e \frac{V_{drive,off} - V_{p1}}{V_{drive,off} - V_{th}} \tag{2.20}$$

A few of the SiC MOSFET products exhibit variation in V_p during V_{DS} transition, at the time of turn-on and turn-off, which invalidates the assumption of constant V_p for

arriving at Eqs. 2.12 and 2.14 for the calculation of V_{DS} transition times. Product datasheets do not provide details of variation in V_{gs} with change in V_{DS}, and a linear behaviour is assumed for this analysis. As shown in Fig. 2.1(c) and Fig. 2.1(d), it is assumed that V_{gs} increases linearly from V_{p1} to V_{p2} when V_{DS} reduces from $V_{DS,max}$ to $V_{DS(on)}$ at the time of turn-on, and vice-versa during turn-off, giving relation,

$$V_{gs} = K_1 V_{DS} + K_2 \tag{2.21}$$

where,

$$K_1 = \frac{V_{p2} - V_{p1}}{V_{DS(on)} - V_{DS,max}} \tag{2.22}$$

$$K_2 = \frac{V_{p1} V_{DS(on)} - V_{p2} V_{DS,max}}{V_{DS(on)} - V_{DS,max}} \tag{2.23}$$

Eqs. 2.6 and 2.21 are solved below for each of the V_{DS} transition intervals [32,34], with boundary conditions known for each interval, and parameter values from the datasheet.

Drain-Source Voltage Fall-Time (t_{fu})

Once I_{DS} reaches $I_{DS,max}$, V_{gs} increases from V_{p1} to V_{p2} and V_{DS} reduces from specification $V_{DS,max}$ to $V_{DS(on)}$. I_{DS} remains unchanged during this interval, indicated as t_{fu} in Fig. 2.1(c). From Eq. 2.6,

$$\int_0^{t_{fu}} dt = \int_{V_{p1}}^{V_{p2}} \frac{R_g C_{iss}}{V_{drive} - V_{gs}} dV_{gs} - \int_{V_{DS,max}}^{V_{DS(on)}} \frac{R_g C_{rss}}{V_{drive} - V_{gs}} dV_{DS} \tag{2.24}$$

From Eqs. 2.21 and 2.24,

$$t_{fu} = \underbrace{R_g C_{iss} log_e \frac{V_{drive} - V_{p1}}{V_{drive} - V_{p2}}}_{Term\ 1} \underbrace{+ \frac{R_g C_{rss}}{K_1} log_e \frac{V_{drive} - K_2 - K_1 V_{DS(on)}}{V_{drive} - K_2 - K_1 V_{DS,max}}}_{Term\ 2} \tag{2.25}$$

Drain-Source Voltage Rise-Time (t_{ru})

During MOSFET turn-off, similar transitions happen for V_{gs}, I_{DS} and V_{DS} as during device turn-on, but in reverse order. Fig. 2.1(d) shows the waveforms for device turn-off. When V_{gs} reduces from V_{p2} to V_{p1}, V_{DS} increases from $V_{DS(on)}$ to $V_{DS,max}$, giving Eq. 2.26 from Eq. 2.6,

$$\int_0^{t_{ru}} dt = \int_{V_{p2}}^{V_{p1}} \frac{R_g C_{iss}}{V_{drive} - V_{gs}} dV_{gs} - \int_{V_{DS(on)}}^{V_{DS,max)} \frac{R_g C_{rss}}{V_{drive} - V_{gs}} dV_{DS} \tag{2.26}$$

From Eqs. 2.21 and 2.26,

$$t_{ru} = \underbrace{R_g C_{iss} log_e \frac{V_{drive,off} - V_{p2}}{V_{drive,off} - V_{p1}}}_{Term\ 1} + \underbrace{\frac{R_g C_{rss}}{K_1} log_e \frac{V_{drive,off} - K_2 - K_1 V_{DS,max}}{V_{drive,off} - K_2 - K_1 V_{DS(on)}}}_{Term\ 2} \tag{2.27}$$

It should be noted that $Term\ 1$ in Eqs. 2.25 and 2.27 is independent of C_{rss} and V_{DS}, whereas $Term\ 2$ includes these factors, which vary significantly during these transition intervals. A technique similar to one proposed in [18] is used here, by dividing drain-source voltage transition interval into small sub-intervals, as shown in Fig. 2.3, calculating Δt_{fu} and Δt_{fu} in each of these sub-intervals, and adding them together to determine the total transition time. Considering the existence of an intermediate level, $V_{DS,mid}$, $Term\ 2$ in Eq. 2.25 is given by:

$$t_{fu,Term2} = \frac{R_g C_{rss}}{K_1} log_e \frac{V_{drive} - K_2 - K_1 V_{DS(on)}}{V_{drive} - K_2 - K_1 V_{DS,max}} \tag{2.28}$$

$$= \frac{R_g C_{rss}}{K_1} log_e \left[\frac{V_{drive} - K_2 - K_1 V_{DS(on)}}{V_{drive} - K_2 - K_1 V_{DS,mid}} * \frac{V_{drive} - K_2 - K_1 V_{DS,mid}}{V_{drive} - K_2 - K_1 V_{DS,max}} \right] \tag{2.29}$$

$$t_{fu,Term2} = \frac{R_g C_{rss1}}{K_1} log_e \frac{V_{drive} - K_2 - K_1 V_{DS(on)}}{V_{drive} - K_2 - K_1 V_{DS,mid}} + \frac{R_g C_{rss2}}{K_1} log_e \frac{V_{drive} - K_2 - K_1 V_{DS,mid}}{V_{drive} - K_2 - K_1 V_{DS,max}} \tag{2.30}$$

where C_{rss1} and C_{rss2} are the approximate values of reverse transfer capacitance, assumed constant for each of the sub-intervals, and represent C_{rss} well if these sub-intervals are infinitesimally small. Similar procedure is repeated for calculating t_{ru}, to give Eq. 2.31 from Eq. 2.27,

$$t_{ru,Term2} = \frac{R_g C_{rss1}}{K_1} log_e \frac{V_{drive,off} - K_2 - K_1 V_{DS,max}}{V_{drive,off} - K_2 - K_1 V_{DS,mid}} + \frac{R_g C_{rss2}}{K_1} log_e \frac{V_{drive,off} - K_2 - K_1 V_{DS,mid}}{V_{drive,off} - K_2 - K_1 V_{DS(on)}} \tag{2.31}$$

2.3 Simulation and Experimental results

Switching times calculated above are used to estimate switching energy values given by [33, 35],

$$E_{on} = V_{DS,max} I_{DS} . \frac{t_{ri} + t_{fu}}{2} \tag{2.32}$$

$$E_{off} = V_{DS,max} I_{DS} . \frac{t_{ru} + t_{fi}}{2} \tag{2.33}$$

SiC schottky diodes being majority carrier devices with insignificant reverse recovery charge, SiC MOSFETs offer advantage of low reverse recovery losses from their body diodes, and the same is neglected in above equations [36, 37]. The additional term to account for effect of charging/discharging of MOSFET parasitic output capacitance C_{oss} is ignored, since experimental results indicate a good cancellation between E_{on} and E_{off} values [34]. The existing methods and proposed method is used to estimate switching energies from corresponding transition times, and compared with double

pulse test experiment [38] and simulation values given by manufacturer's models in MATLAB/Simulink with PLECS blockset for Cree's CAS300M12BM2 SiC half-bridge MOSFET module. Since MOSFET junction thermal time constants are of the order of a few *msec*, the double pulse test does not increase junction temperature significantly, and a value of 25° Celsius is assumed for this analysis [39].

2.3.1 Simulation Results

The double pulse test circuit of Fig. 2.5 is simulated using manufacturer's models in PLECS blockset of MATLAB/Simulink. Since this is an ideal system, it does not take into account effect of PCB parasitics, discussed in later sections, and results from PLECS model closely resemble switching energy values given in product datasheet. Fig. 2.4(a)-(f) show a comparison of switching energy values from simulation in PLECS, with results obtained using existing and proposed models, for drain-source voltage of 300V and 800V. *Method* 1 and *Method* 2 are used for calculations with V_p approximated as the average of V_{p1} and V_{p2}. *Method* 1 clearly overestimates switching energy values, by a minimum of 140% and 400% for V_{DS}=300V and 800V, respectively, and hence not reported in figures. The proposed method exhibits smaller errors from PLECS models, as compared with *Method* 2, which underestimates switching energies and exhibits greater errors at majority of the operating points. For V_{DS}=300V, *Method* 2 underestimates E_{on} values by a minimum of 42%, with a maximum deviation of nearly 60% from PLECS simulation. The proposed model, on the other hand, exhibits a worst case estimation error of nearly 35%, with values of E_{on} and E_{off} cancelling each other to give total switching energy very close to PLECS values. For V_{DS}=800V, the estimation errors from the proposed model and *Method* 2

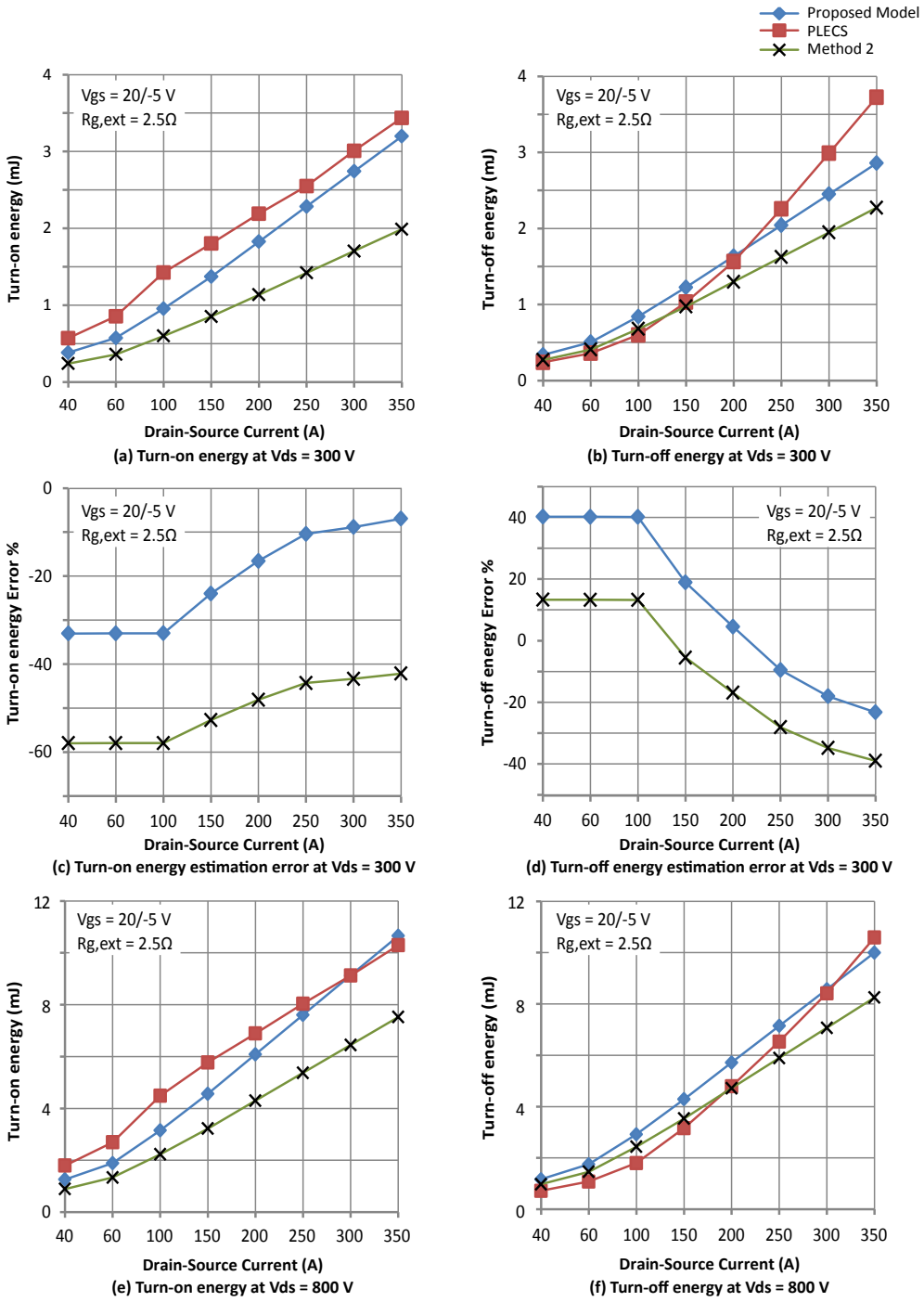
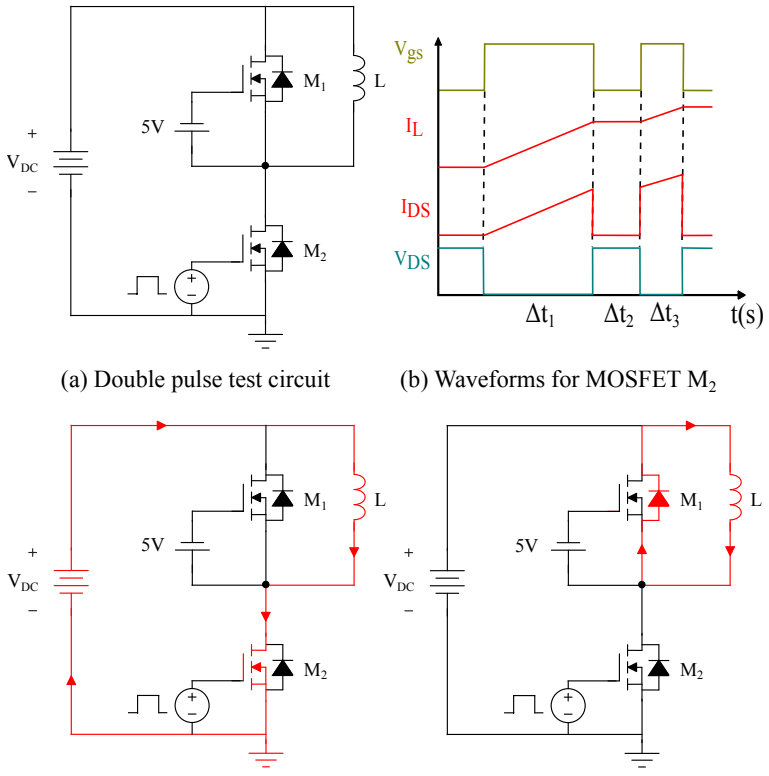


Figure 2.4: Comparison of switching energy values and errors from proposed model, *Method* 2 and PLECS simulation



(a) Double pulse test circuit (b) Waveforms for MOSFET M_2

(c) Conduction path when M_2 is ON (d) Conduction path when M_2 is OFF

Figure 2.5: Double pulse test circuit and waveforms.

approach a maximum of 30% and 50%, respectively. The estimation accuracy of the proposed model is found to improve significantly at higher values of I_{DS}, as the relative magnitude of C_{oss} charge/discharge current reduces with respect to $I_{DS,max}$.

2.3.2 Experimental Results

The double pulse test is used for capturing the switching transitions at the time of device turn-on and turn-off. Fig. 2.5 shows the double pulse test schematic and waveforms for MOSFET M_2. Table 2.1 lists the details of the equipment and components used to perform this test. In this experiment, low-side MOSFET M_2 is first turned

Table 2.1: Experimental test equipment and component values

Type	Specification
Gate Driver	Cree CGD15HB62P1, 9A, 1200V, 2-Ch
MOSFET	CAS300M12BM2, 1200V, 5 mΩ half-bridge module
$R_{g,ext}$	2.5 Ohm
Inductor	80μH
C_{in}	5 * 500μF, 450V, B25655P4507K000, Epcos
Oscilloscope	Tektronix MDO3024, 200MHz/2.5GS/s
Voltage Probe	Tektronix P5200A, 50MHz, Differential Probe
Current Probe	PEM CWTUM/3/B Rogowski Current Transducer

ON for time Δt_1, during which inductor current I_L ramps up to specification I_{DS}. During this time, I_L equals $I_{DS,M2}$, as shown in Fig. 2.5(c). High-side MOSFET M_1 is permanently OFF, with V_{gs} of -5V applied between its gate-source terminals. Once I_L reaches $I_{DS,max}$, M_2 is turned OFF for time Δt_2 (2.5μsec here), short enough to allow only negligible decline in I_L due to freewheeling of body diode of M_1 and circulation of I_L in the indicated conduction path. On completion of Δt_2, M_2 is turned ON again for time Δt_3 (2.5μsec here), before M_2 is finally turned OFF. Due to the benefits of SiC devices, the reverse recovery losses from body diode of M_1 are negligible at the turn-on of M_2, and hence ignored in calculations. The turn-off and turn-on instants at the beginning of Δt_2 and Δt_3, respectively, are used to calculate E_{off} and E_{on} for M_2, respectively. Switching energy loss occurs due to the voltage/current overlap in a device during a switching transition, and is the product of V_{DS}, I_{DS} and time-step (0.4ns here). For computation of E_{off}, this product is evaluated from the last instant when V_{DS} exits 0V, to the first time I_{DS} reaches 0A, and vice-versa for E_{on}, shown in the MATLAB script in Appendix B. These calculations of switching energies take into consideration delays of voltage probe and current transducer.

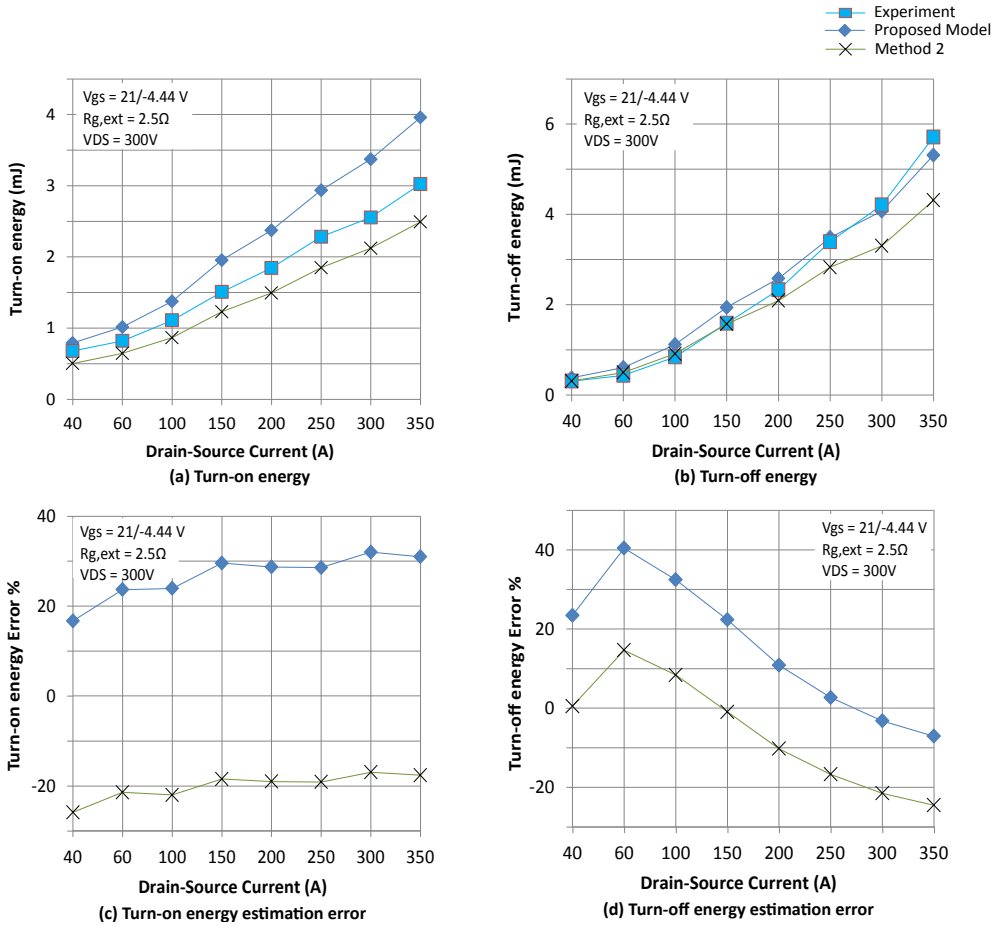


Figure 2.6: Comparison of switching energy values and errors from proposed model, *Method* 2 and double pulse test experiment

Fig. 2.6(a)-(d) show comparisons of switching energy values from experimental hardware with estimations using *Method* 2 and the proposed model. It is seen that E_{off} values from proposed model are closer to experimental results, with overestimations providing for safety margin during cooling system design. *Method* 2 underestimates switching losses at majority of the operating points, by nearly 20%. It may be noted that switching energy values from experiment are larger than those given in the datasheet. Fig. 2.7 shows the turn-off and turn-on transitions for V_{DS}=300V and I_{DS}=200A. A significant ringing is observed in waveforms for both V_{DS} and I_{DS} due

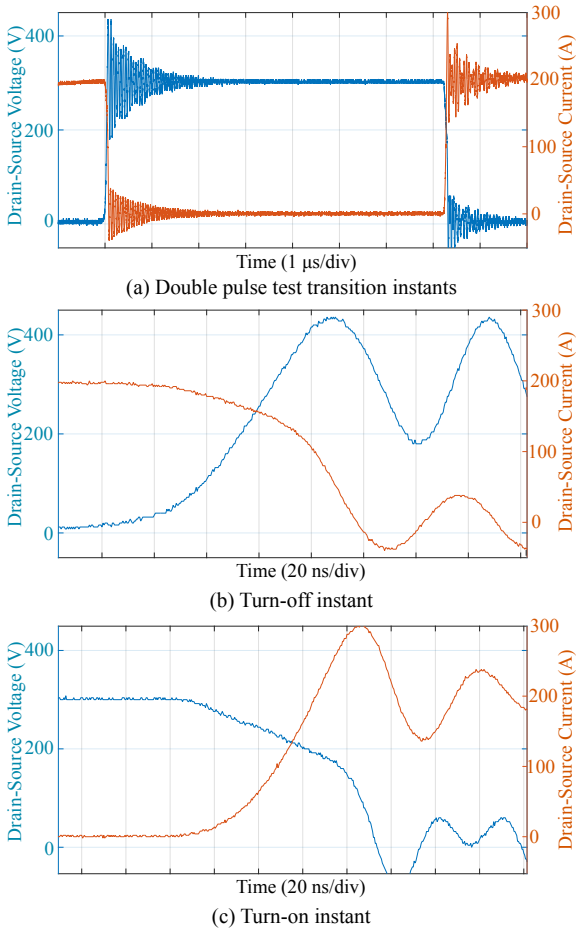


Figure 2.7: Switching waveforms for V_{DS}=300V, I_{DS}=200A

to stray inductance of the bus bars and the half-bridge module under test, resulting in greater losses [38]. Since the proposed model does not account for effects of stray inductance, the switching times and energy loss values are calculated for the actual V_{DS} and I_{DS} transition limits from hardware. The estimation errors are attributed to the initial approximation of linear variation of V_{DS} with V_{gs}, and presence of parasitics, which could be minimized by following the recommended guidelines of layout/PCB design.

2.4 Summary

This chapter presented a method for the estimation of switching energies during turn-on and turn-off of SiC MOSFETs with non-flat miller plateau region. In order to validate results from proposed model, double pulse test circuit is implemented at various drain-source currents, in both PLECS simulation and hardware. It is observed that the proposed model overestimates switching energies, with values close to actual device characteristics, in comparison with existing methods. The estimation errors are attributed to V_{gs}-V_{DS} linear approximation and overshoots due to stray inductance in the circuit. The estimation accuracy is improved at higher values of drain-source current. The proposed method could be used for estimation of switching energies for SiC MOSFETs in cases where these values are not available in the datasheet at all required operating points.

Chapter 3

Switching Loss Minimization Using Soft-Switching Methods

The passive and mechanical components account for a majority of the total cost and volume of a power converter [13,40,41]. Continuous efforts are being made to operate at higher switching frequencies to reduce the overall system size. Operation at high switching frequencies results in greater switching losses, making the cooling system volume larger [42]. The switching transitions involve charging and discharging of a MOSFET's parasitic capacitances. The advent of SiC and GaN technology based products offer lower switching losses than conventional Si substrate based devices. This is due to their smaller die size and reduced parasitic capacitances [25, 26]. This allows the power converters to operate at higher switching frequencies with use of these WBG devices [43]. Despite these advantages, the maximum switching frequency is still limited by the maximum allowed junction temperature and the ability of a MOSFET package to dissipate its losses [27].

In order to operate at even higher switching frequency, a variety of soft-switching

techniques are used to reduce the switching losses in a power converter. These techniques are discussed in Chapter 1 with their benefits and disadvantages. The turn-on losses in most MOSFETs are greater than the turn-off losses [44] (with a few exceptions such as the CAS300M12BM2 half-bridge module from Cree Inc. at a few of the operating points [20]). This research emphasizes on the use of a soft-switching technique which replaces the higher FET turn-on and diode reverse recovery losses with smaller turn-off losses by maintaining at least slightly negative minimum inductor current [28, 29]. The turn-off losses are further reduced with the use of an external capacitor across the MOSFET drain-source terminals, in addition to its intrinsic drain-source parasitic capacitance. The voltage clamping characteristic of a capacitor [45] serves to delay the rise in drain-source voltage at the time of turn-off. This reduces the area of overlap between voltage and current in a MOSFET and the turn-off switching energy.

There exist other methods including use of turn-off snubbers for reducing the turn-off losses in the switching devices. [46] discusses the use of a voltage controlled variable capacitor based snubber for reducing the switch turn-off loss. This technique has a demerit of moving the location of the power loss by dissipating energy of the switch output capacitors on a resistor. In another method, the use of a turn-off snubber across the output diode in the boost converter of [47] enables ZVS characteristic for the switching device, but results in relatively large output current ripple values. Other such techniques in [48, 49] include the use of auxiliary circuits with many additional components with the main power circuit. The proposed method only recirculates energy between the inductor and capacitors in the circuit with minimal dissipation in their parasitic resistances while using only a single additional capacitor at the output

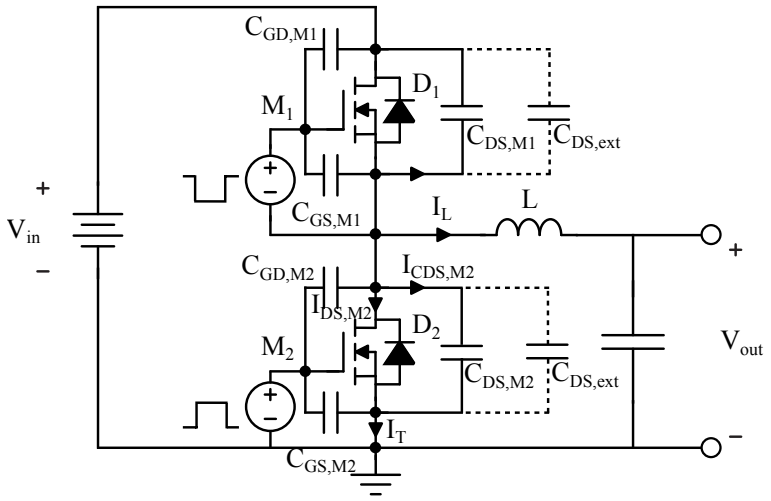


Figure 3.1: Buck Converter Topology

of each MOSFET.

This soft-switching method is delineated for the buck converter topology and is validated using analytical models, simulations and experimentation for MOSFETs from Cree Inc. in this chapter. This method is extended for use with GaN devices in later chapters.

3.1 Proposed Soft-Switching Method

Switching losses in a MOSFET result from the overlap of the voltage V_{DS} across the device and the current I_{DS} through it at the time of turn-on (E_{on}) and turn-off (E_{off}) [2, 3, 7]. A dead-time is included between the conduction periods of the complimentary devices in a half-bridge to prevent cross-conduction. The body diode of a MOSFET may conduct due to freewheeling action during this time [50], which may incur diode reverse recovery losses in case of a hard turn-on.

For a conventional buck converter shown in Fig. 3.1, the MOSFETs M_1 and

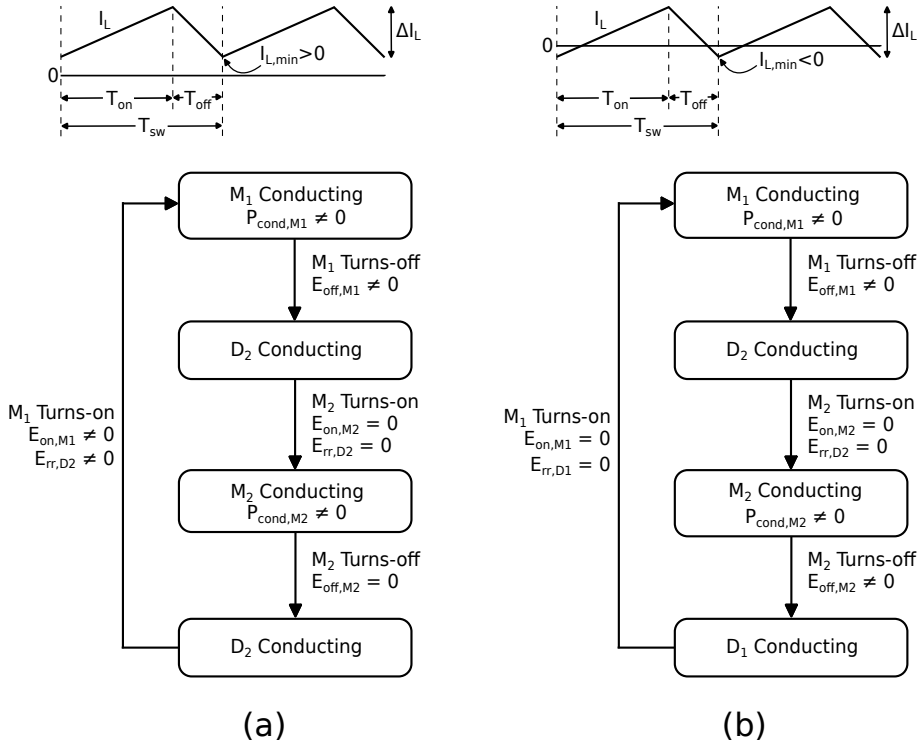


Figure 3.2: Sources of power loss during a switching cycle for a buck converter with (a) $I_{L,min} > 0$ (b) $I_{L,min} < 0$.

M_2 switch complementary to each other, with a small dead time, as discussed earlier. The indicated directions of the currents in the inductor I_L and drain-source capacitors I_{CDS} are assumed positive for the remainder of this analysis. Since in a buck converter, the input voltage V_{in} is greater than the output voltage V_{out}, I_L increases while M_1 is conducting during on-time T_{on} and reduces while M_2 is conducting during off-time T_{off}, according to Eqs. 3.1 and 3.2, respectively.

$$\left(\frac{dI_L}{dt}\right)_{T_{on}} = \frac{V_{in} - V_{out}}{L} \tag{3.1}$$

$$\left(\frac{dI_L}{dt}\right)_{T_{off}} = \frac{-V_{out}}{L} \tag{3.2}$$

where L is the inductance. For a buck converter, V_{out} is given in terms of V_{in} and duty cycle D according to Eq. 3.3,

$$V_{out} = D.V_{in} \tag{3.3}$$

From Eqs. 3.1 and 3.3, the inductor current ripple is given by,

$$\Delta I_L = \frac{V_{in}D(1-D)}{LF_{sw}} \tag{3.4}$$

where F_{sw} is the switching frequency. Since ΔI_L is inversely proportional to the value of L, a buck converter with an inductance large enough such that the minimum inductor current $I_{L,min}$ is greater than zero will exhibit a switching sequence and power losses as indicated in Fig. 3.2(a). A buck converter using a smaller L, such that $I_{L,min}$ is negative, will follow a switching sequence and exhibit power losses as given in Fig. 3.2(b).

From Fig. 3.1, the output capacitance of the MOSFETs is given by Eq. 3.5,

$$C_{oss} = C_{DS} + C_{GD} \tag{3.5}$$

From Fig. 3.2(a), it is seen for cases when $I_{L,min}$ is positive that the energy stored in the effective output capacitance $C_{oss,M1}$ is dissipated in the FET channel at the time of turn-on, resulting in high turn-on loss $E_{on,M1}$. Reverse recovery loss $E_{rr,D2}$ also occurs at this switching instant when the conducting body diode D_2 is forced into reverse bias. Assuming 20% inductor current ripple, the losses in this system are

given as [33],

$$\begin{cases} E_{cond,M1} = I_L^2 R_{ds,on} T_{on} \\ E_{off,M1} = 0.55 V_{in} I_L (t_{fi} + t_{ru}) \\ E_{cond,M2} = I_L^2 R_{ds,on} T_{off} \\ E_{on,M1} = 0.45 V_{in} I_L (t_{ri} + t_{fu}) \\ E_{rr,D2} = Q_{rr} V_{in} \end{cases} \tag{3.6}$$

where E_{cond} represents the conduction energy loss in the FETs and $E_{rr,D2}$ is the loss in M_1 due to the flow of reverse recovery charge of D_2. The values of current and voltage rise and fall times (t_{ri}, t_{fi}, t_{ru}, t_{fu}) vary with V_{DS} and I_{DS} in a FET. For Cree's C2M0025120D SiC FET product, E_{on} is nearly twice the value of E_{off} at an operating point. If E_{off} for this device for its turn-off from (V_{in}, I_L) is equivalent to α, then the total switch energy losses for a switching period are given by,

$$E_T = I_L^2 R_{ds,on} T_{sw} + Q_{rr} V_{in} + 2.9\alpha \tag{3.7}$$

where,

$$\alpha = 0.5 V_{in} I_L (t_{fi} + t_{ru}) \tag{3.8}$$

Alternatively, the proposed method with negative $I_{L,min}$ replaces the higher sum of FET turn-on and diode reverse recovery losses with a few orders of magnitude smaller FET turn-off loss $E_{off,M2}$ (and negligible losses due to diode reverse recovery), as shown in Fig. 3.2(b). The losses for such a system with minimally negative $I_{L,min}$

are given by,

$$\begin{cases} E_{cond,M1} = 1.33 I_L^2 R_{ds,on} T_{on} \\ E_{off,M1} = V_{in} I_L (t_{fi} + t_{ru}) \approx 2\alpha \\ E_{cond,M2} = 1.33 I_L^2 R_{ds,on} T_{off} \\ E_{off,M2} \approx 0 \end{cases} \tag{3.9}$$

This results in total switch energy losses for a switching period:

$$E_T = 1.33 I_L^2 R_{ds,on} T_{sw} + 2\alpha \tag{3.10}$$

Given that the WBG devices have a small $R_{ds,on}$, the total switch losses when $I_{L,min} < 0$ are smaller than the losses with $I_{L,min} > 0$. The ratio E_{on}/E_{off}, at a particular operating point, is even higher for some devices, such as Cree's CAS120M12BM2, enabling greater benefits with use of the proposed method. In a system with varying V_{in} and V_{out} (and hence duty cycle), the feedback loop will vary F_{sw} in order to maintain at least a small negative value for $I_{L,min}$ according to Eq. 3.4, while following the characteristics of Fig. 3.2(b). The turn-off losses $E_{off,M1}$ and $E_{off,M2}$ in M_1 and M_2 respectively, can further be reduced with the use of additional capacitance $C_{DS,ext}$ across the MOSFETs' drain-source terminals, as shown in Fig. 3.1. Fig. 3.3 shows representative waveforms for V_{DS} and I_{DS} during the turn-off of a MOSFET. While on one hand, reduction in I_{DS} is controlled by the gate-source voltage V_{gs}, on the other hand, the increase of V_{DS} is also determined by the magnitude of M_1 and M_2's effective output capacitance, $C_{oss,M1}$ and $C_{oss,M2}$, respectively. Due to the voltage clamping property of a capacitor, addition of $C_{DS,ext}$ reduces the rate of rise of V_{DS},

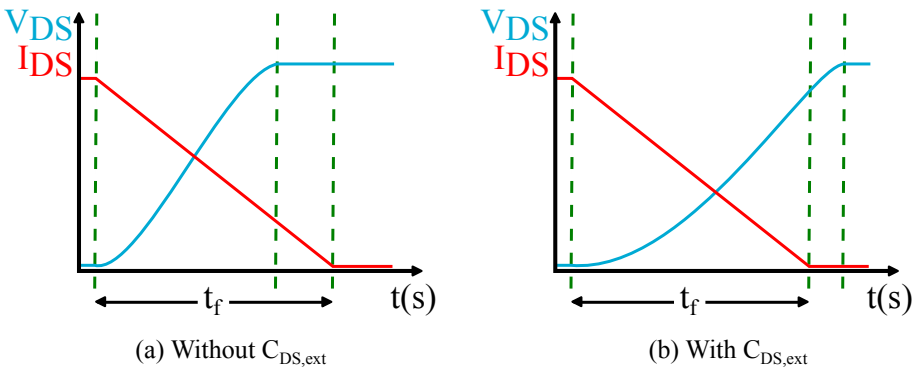


Figure 3.3: Representative waveforms for voltage across and current through M_2 at turn-off.

reducing the energy loss due to the voltage/current overlap during turn-off. This is equivalent to a reduction in the multiplication factor of 0.5 assumed while calculating switching losses for ideal switching behavior in [33]. The non-linear behavior of V_{DS} at the beginning and end of turn-off transition is due to the variation of the FET C_{oss} with V_{DS}, with large values in nF range for small values of V_{DS}. The addition of $C_{DS,ext}$ does not induce additional turn-on losses in the FETs due to the nature of the waveforms and recirculation of energy between the inductor and the capacitors for the case when $I_{L,min}$ is negative. The value of $C_{DS,ext}$ is limited by the operating F_{sw}, to ensure that the longer turn-off time does not occupy a majority of the switching period. An analytical approach to model this behavior is introduced in later sections and its results are compared with simulations using Cree's LTSpice models for discrete FET product C2M0025120D and experimentation, to verify the proposed technique of reduction in turn-off losses.

3.2 The Analytical Model

A soft-switching technique to reduce the switching losses in the presence of negative $I_{L,min}$ and use of $C_{DS,ext}$ was discussed earlier.

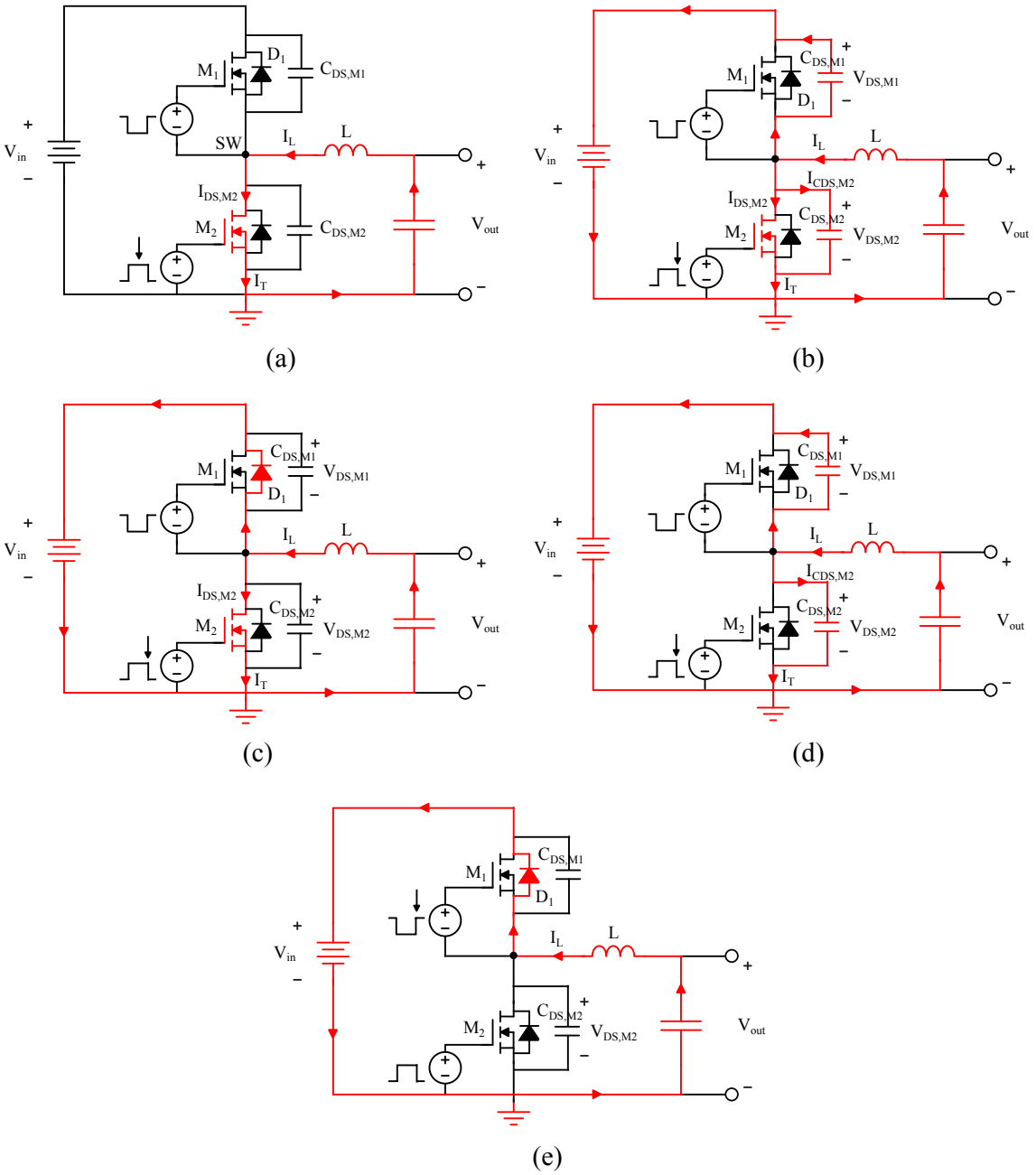
A linear recursive model to mimic the FET turn-off characteristic and the effect of the use of additional $C_{DS,ext}$ is presented here. Fig. 3.4 shows the current flow path at various time instants during the turn-off of M_2. Let us assume that the effective output capacitance of M_1 and M_2, including additional $C_{DS,ext}$, is represented by $C_{DS,M1}$ and $C_{DS,M2}$, respectively. Initially, I_L is negative and M_2 is conducting, as shown in Fig. 3.4 (a). Fig. 3.4 (b) shows the current path at the moment of initiation of turn-off of M_2, when $V_{gs,M2}$ begins to reduce from its ON-level of 20V. Since an inductor opposes a change in flux (and hence current through it) according to Faraday's Law [51], let us assume I_L remains unchanged during the small turn-off interval of the order of a few *nsec*. As $I_{DS,M2}$ reduces from its peak value, currents $I_{CDS,M1}$ and $I_{CDS,M2}$ of total magnitude equal to the difference of I_L and $I_{DS,M2}$ flow through $C_{DS,M1}$ and $C_{DS,M2}$ repectively, increasing $V_{DS,M2}$, according to Eq. 3.11,

$$I_L = I_{DS,M2} + I_{CDS,M1} + I_{CDS,M2} \tag{3.11}$$

$$I_{CDS,M1} = -C_{DS,M1}\frac{dV_{DS,M1}}{dt} \tag{3.12}$$

But,

$$V_{DS,M1} = V_{in} - V_{DS,M2} \tag{3.13}$$



(a) Current conduction when M_2 is ON (b) when $I_{DS,M2}$ is reducing and additional capacitors are charging during $t_{off,1}$-$t_{off,2}$ (c) when $V_{DS,M2}$ reaches V_{in} before $I_{DS,M2}$ reduces to zero (d) $I_{DS,M2}$ reaches zero while current flows through the additional capacitors during $t_{off,2}$-$t_{off,3}$ (e) completion of turn-off of M_2 and reverse conduction through M_1 during $t_{off,3}$-$t_{off,4}$.

Figure 3.4: Switching sequence and current paths during turn-off of M_2 for the buck converter of Fig. 3.1 and waveforms in Fig. 4.4.

From Eqs. 3.12 and 3.13,

$$I_{CDS,M1} = -C_{DS,M1}\frac{d(V_{in} - V_{DS,M2})}{dt} \tag{3.14}$$

Since V_{in} is instantaneously constant,

$$I_{CDS,M1} = C_{DS,M1}\frac{dV_{DS,M2}}{dt} \tag{3.15}$$

$$I_{CDS,M2} = C_{DS,M2}\frac{dV_{DS,M2}}{dt} \tag{3.16}$$

from Eqs. 3.11, 3.15 and 3.16,

$$I_L = I_{DS,M2} + (C_{DS,M1} + C_{DS,M2})\frac{dV_{DS,M2}}{dt} \tag{3.17}$$

According to Eq. 3.17, the output capacitance of the two FETs are equivalent to be placed in parallel for the inductor current distribution. Assuming that $I_{DS,M2}$ reduces linearly with drop in $V_{gs,M2}$, $V_{DS,M2}$ rises towards V_{in} (for an ideal body diode D_1). Once $V_{DS,M2}$ exceeds V_{in}, D_1 begins to conduct while $I_{DS,M2}$ continues to reduce to zero. With addition of a large $C_{DS,ext}$, it is possible for $I_{DS,M2}$ to reach zero before $V_{DS,M2}$ reaches V_{in}, as shown in Fig. 3.3 (b). In this case, for the remainder of the time from the instant $I_{DS,M2}$ hits zero till $V_{DS,M2}$ reaches V_{in}, the output capacitors are charged by the nearly constant I_L, as shown in Fig. 3.4 (d), followed by conduction of D_1 marking the completion of I_L commutation from M_2 to M_1, as shown in Fig. 3.4 (e). A similar process is repeated during current commutation from M_1 to M_2 with positive maximum inductor current, $I_{L,max}$.

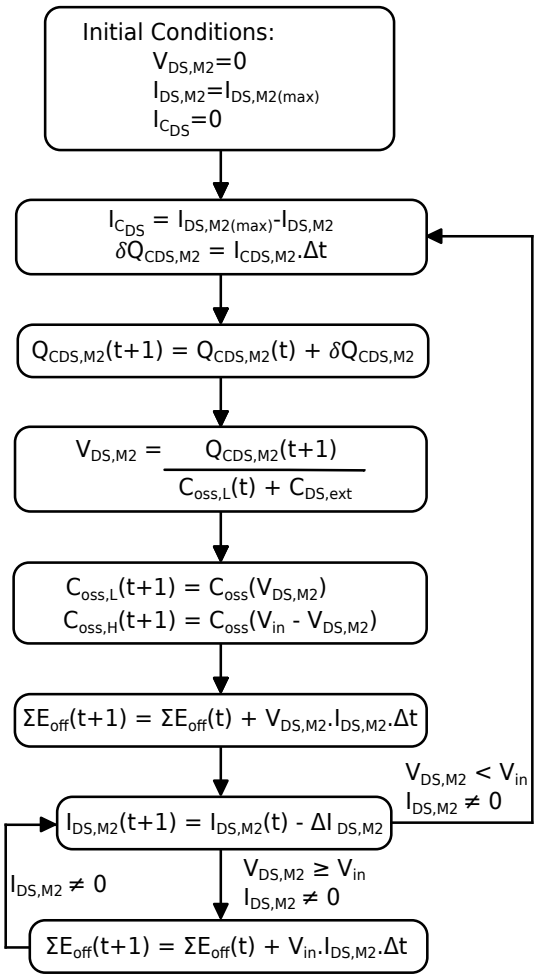


Figure 3.5: Analytical recursive model.

Fig. 3.5 shows the block diagram for the recursive model implemented in MATLAB for the script in Appendix A. The model begins with M_2 conducting and $V_{DS,M2}$ and $I_{DS,M2}$ at their minimum and maximum values, respectively. For the infinitesimally small time interval Δt during the turn-off time of M_2 obtained from equations in [19] using the datasheet parameters, a small charge δQ is delivered to the output capacitors of the FETs due to the current $I_{C_{DS}}$ flowing through them. This charge builds incrementally on the capacitors. The new drain-source voltage is computed,

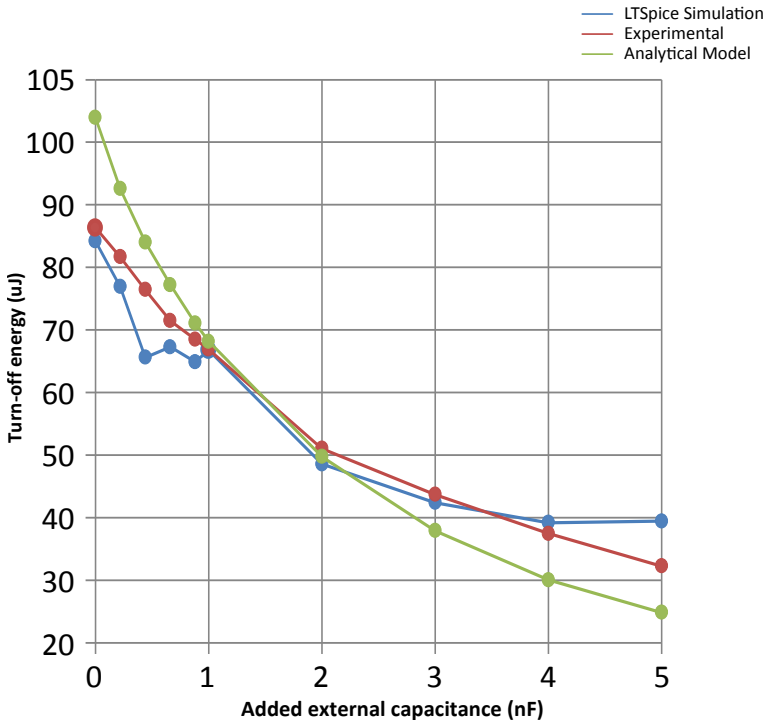


Figure 3.6: Reduction in turn-off losses

and values of effective output capacitances are updated, owing to their non-linear behavior. The turn-off energies from each of the small intervals are added to the summation from the previous iterations, and the process repeats till $I_{DS,M2}$ reaches zero. The results of $E_{off,M2}$ computation using this model are presented in later sections.

3.3 Simulation and Experimental Results

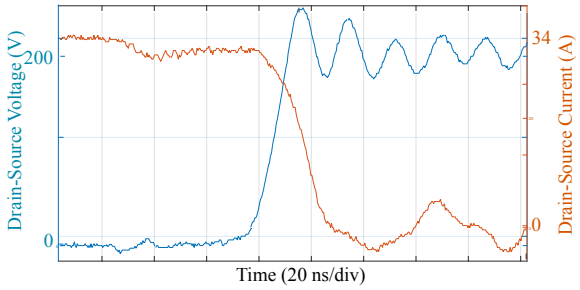
The proposed soft-switching technique is validated for the buck converter of Fig. 3.1, using the above analytical model, LTSpice simulation using device model for C2M0025120D from Cree Inc., and experimentation using hardware in [52]. The

Table 3.1: Test conditions, components and equipment used for testing

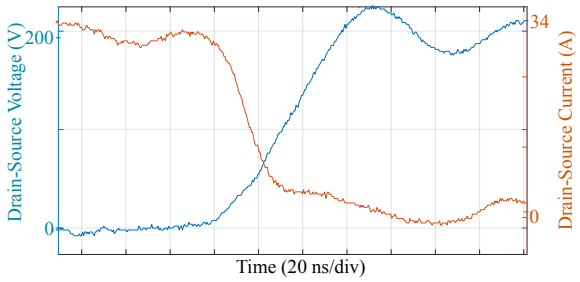
Type	Specification
Input Voltage	200V
Output Voltage	100V (Duty cycle=0.5)
Switching Frequency	3 kHz
$I_{DS,max}$	34A
MOSFET	C2M0025120D,1200V/90A/25mΩ SiC MOSFET
Gate Driver	IXDN609SI, $R_{g,ext}$= 6.67 Ω
Inductor	256μH
Oscilloscope	Tektronix MDO3024, 200MHz/2.5GS/s
Voltage Probe	Tektronix TPP0250, 250MHz, 3.9pF/10MΩ
Current Sensor	PEM CWTUM/3/B Rogowski Current Transducer

switching energy values from experiment are calculated using MATLAB script in Appendix B and are compensated for the delays induced by the probe parasitics. Fig. 3.6 shows the variation in turn-off losses in M_2 for different values of additional capacitance across its drain-source terminals. The results using the three validation methods match closely. The losses from experimentation and simulation in LTSpice are slightly different from those predicted by the analytical model since a linear variation in V_{DS} and I_{DS} is assumed during turn-off, which is not the real case.

This analysis uses test conditions, components and equipment listed in Table 3.1. In order to observe the switching transitions and the degree of reduction in switching loss with use of large additional capacitance, the converter is operated at a switching frequency of 3 kHz with a relatively large value of inductance. For the same value of output current and negative $I_{L,min}$, the value of switching losses without $C_{DS,ext}$ is lower to 68.9% of those with positive $I_{L,min}$. As the external capacitance is increased from zero to $5nF$, the turn-off losses in M_2 are reduced to 37.3% of their original value, helping to reduce the total switching losses to 25.5% of the case with positive



(a) Without external drain-source capacitance



(b) With external drain-source capacitance of 5nF

Figure 3.7: Switching waveforms for turn-off of M_2 for test conditions in Table 3.1.

$I_{L,min}$. For a custom inductor designed for high switching frequency and large current ripple values, the increase in the inductor losses due to larger current ripple with negative $I_{L,min}$ is minimal in comparison with switching energy savings in MOSFETs with the use of this method. This offers an opportunity to go higher in switching frequency while staying within the device power dissipation limits to design a higher power density system. Alternatively, operation at the same switching frequency would result in lower system losses with need for a smaller heat sink of lower cost. It should be noted that external capacitance is added only to the output of M_2 for this analysis, and use of a capacitor at the output of M_1 would help to reduce losses further. Fig. 3.7 shows the waveforms for turn-off of M_2 for the case of zero and $5nF$ of external capacitance added across its drain-source terminals. It is seen that due to the voltage clamping characteristic of the additional capacitor, the voltage waveform is delayed

and has a smaller rate of increase, reducing the voltage/current overlap to result in smaller switching energy loss. It also reduces the frequency of resonance between the stray inductance of the bus bars and FET output capacitances which appears as an overshoot in V_{DS}, making it easier to achieve EMI compliance.

3.4 Summary

This chapter discussed a soft-switching method to reduce switch losses in a buck converter with negative minimum inductor current. The turn-off loss is diminished to 37.3% of its original value, and total switching losses to 25.5% of their value in a system with positive minimum inductor current and no additional output capacitance. Results from an analytical model proposed to validate this technique closely match the switching energy values obtained from simulation using manufacturer's device models in LTSpice and experimentation. With a majority of power converter topologies including a half-bridge, this technique can be extended to reduce losses in other such systems. It is planned to validate this soft-switching technique in hardware for a power converter operating at high power and switching frequency with GaN devices for an estimate of its advantages in terms of the losses and volume of the overall system in later chapters.

Chapter 4

Use of Linear Soft-Switching for Design of High Power Density High Frequency DC/DC Converters

This chapter discusses the use of a linear soft-switching method to replace the greater turn-on losses with smaller turn-off losses in a switching cycle with negative minimum inductor current in a buck converter with GaN devices [28–30]. The use of GaN devices takes advantage of their even smaller parasitics in comparison with SiC devices while also extending the use and validation of the linear soft-switching method to different types of wide bandgap devices. It is called 'linear' soft-switching since the proportionality between duty cycle and output voltage is maintained, unlike few other soft-switching techniques [53]. The voltage clamping characteristic of a capacitor is used to further reduce the turn-off losses. The use of an additional capacitor across the MOSFET drain-source terminals reduces the rate of increase of drain-source voltage

and the resultant voltage/current overlap at the time of device turn-off. This soft-switching method requires use of minimum number of additional components with no added losses in the device channel at the time of turn-on, due to only recirculation of energy between the passive components in the DC/DC converter.

The linear soft-switching method is used for reducing the switching losses to enable operation with switching frequency in the MHz range for a buck converter using GaN devices. A discussion of the soft-switching method and design considerations for buck converter topology is included. The analytical model in Section 3.2 is used to understand the various stages of turn-off of a device from GaN Systems Inc. and reduction in its turn-off losses with use of additional capacitance. The results for the reduction in turn-off losses with added capacitance are presented, calculated using the analytical model and validated in hardware. The soft-switching technique is shown to enable operation at 1 MHz switching frequency with reduced losses per switching cycle as compared to a traditional buck converter with positive $I_{L,min}$ and hard-switching.

4.1 Linear Soft-Switching Method

The MOSFETs in the buck converter of Fig. 3.1 switch complementary to each other with a suitable dead-time to avoid cross-conduction. Since an inductor opposes an instantaneous change in its current according to Faraday's law, one of the MOSFETs exhibit reverse conduction characteristic during the dead-time, resulting in ZVS characteristic on the corresponding device. GaN devices do not have an intrinsic body diode and the associated reverse recovery losses but are capable of reverse conduction with a relatively larger voltage drop equal to the sum of the gate threshold voltage and the negative gate drive voltage in off-state condition [30]. This reverse conduction

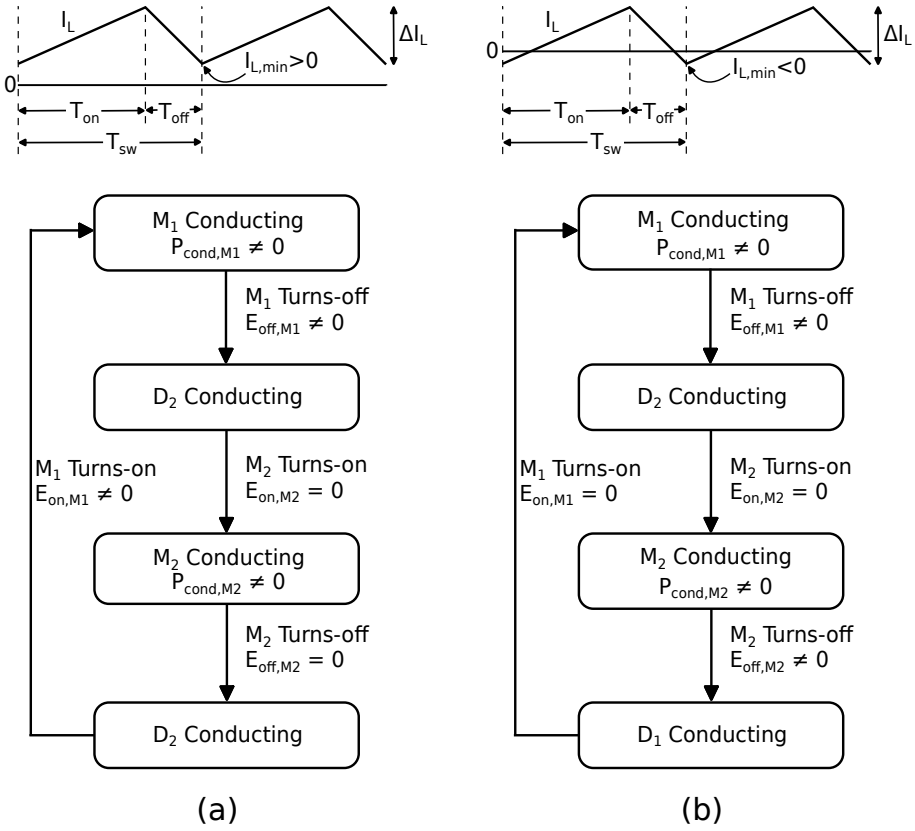
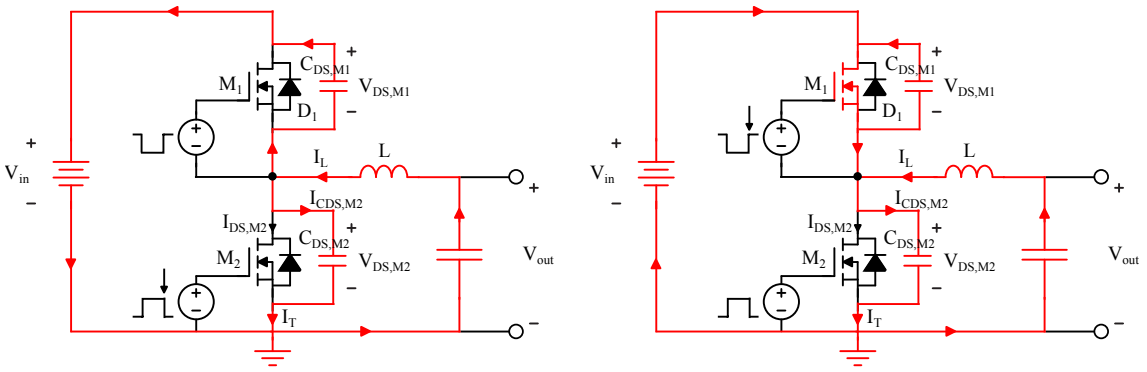


Figure 4.1: Switching events and the associated losses during a switching time period in a buck converter using GaN devices with (a) $I_{L,min} > 0$ (b) $I_{L,min} < 0$.

characteristic of GaN MOSFETs in the off-state condition is modeled and referenced as anti-parallel body diode operation in this paper. Depending on the value of the output current I_{out} (equal to the average inductor current $I_{L,0}$) and the inductance L, the minimum inductor current $I_{L,min}$ may be positive or negative. Fig. 4.1 shows the sequence of switching events and the associated losses during a switching cycle in a buck converter using GaN devices with positive and negative $I_{L,min}$. In the linear soft-switching (SSW) method, $I_{L,min}$ is intentionally made negative to enable ZVS behavior at turn-on for both the switches [28, 29]. The greater turn-on losses in M_1 are replaced with smaller turn-off losses in M_2 reducing the total losses per



(a) Current flow just before turn-on of M_1.

(b) Current flow after M_1 is turned-on with excessive losses.

Figure 4.2: Buck converter using large additional capacitors with MOSFETs and small dead-time

switching cycle. The degree of reduction in switching losses depends on the ratio of the turn-on and turn-off losses which varies between devices. For GaN Systems Inc. GS66516T MOSFET product, the turn-on losses are nine times the turn-off losses at the 400V/20A operating point in the datasheet [30]. The turn-off losses are further reduced with the use of an additional capacitance across the MOSFET drain-source terminals. This reduces the rate of increase of voltage V_{DS} and the resultant voltage-current overlap. This technique is found to reduce the switch losses to nearly 25.5% of the losses occurring in a system with large inductor and positive $I_{L,min}$ using Cree's C2M0025120D MOSFET product, shown in Section 3.3.

While a negative $I_{L,min}$ is needed to reduce the switching losses, this current should be sufficiently large to charge and discharge the MOSFET output capacitors within the dead-time. A system with large additional MOSFET output capacitors and a small switching dead-time would cause large instantaneous currents through the MOSFET channel charging/discharging these capacitors, inducing excessive additional losses. Fig. 4.2 shows the current paths during the occurrence of such a

phenomenon during the turn-off of M_2. Initially, the negative I_L is discharging M_1's output capacitance $C_{DS,M1}$ and charging M_2's output capacitance $C_{DS,M2}$ while M_2 drain-source current $I_{DS,M2}$ has reduced to zero, as shown in Fig. 4.2(a). M_2 drain-source voltage $V_{DS,M2}$ is at an intermediate value between zero and buck converter input V_{in}. At the turn-on instant of M_1, the remaining charge on $C_{DS,M1}$ is instantaneously removed through the M_1 channel. Another large current charges $C_{DS,M2}$ to V_{in} through M_1. Both these instantaneous currents cause excessive losses in M_1 and increase the system losses, opposite of what is intended with the use of the linear SSW method. A similar phenomenon would occur during the turn-off of M_1. Thus, the degree of capacitive loading on the MOSFETs and the benefits of reduction in switching losses are limited by the values of the dead-time and $I_{L,min}$.

The linear SSW method requires the current ripple to be sufficiently large, i.e. $\Delta I_L > 200\%$. However, PWM switching in a buck converter leads to the inductor current ripple:

$$\Delta I_L = \frac{V_{in} D(1-D)}{L F_{sw}} \tag{4.1}$$

where D is the duty cycle and F_{sw} is the switching frequency. The inductor current ripple depends on D and is maximum at $D = 0.5$ and decreases as D approaches 0 or 1. Hence, a variable F_{sw} is introduced to keep ΔI_L approximately constant. It is calculated according to Eq. 4.1 requiring a constant $\Delta I_L > 200\%$. The F_{sw} is lower bounded to limit the output voltage ripple ΔV_{out} and to ensure a high control bandwidth. Lower bounding F_{sw} results in hard switching, which is acceptable when F_{sw} falls below a certain threshold, e.g. 100 kHz here. The passive components are sized at the $D = 0.5$ worst-case operating point with maximum switching frequency

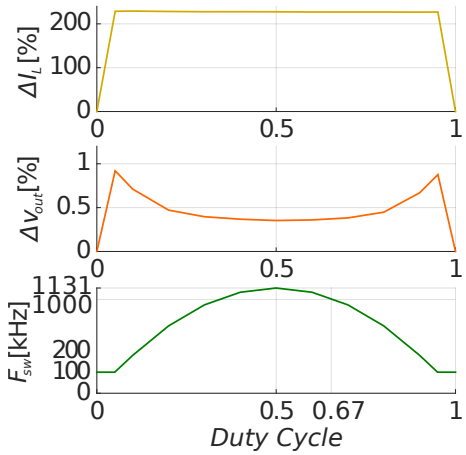


Figure 4.3: Variation in inductor current ripple, output voltage ripple and switching frequency with change in duty cycle in a buck converter using linear SSW.

and losses. A deviation from the $D = 0.5$ point would reduce the switching frequency and the associated high-frequency losses in the MOSFETs and the inductor for a better power conversion efficiency. The large high-frequency current ripple leads to challenges in the inductor design. For instance, the off-the-shelf planar inductor features significant AC losses in these operating conditions. A dedicated inductor needs to be developed that is optimized for operation in the given conditions, similar to ones in [54, 55]. Fig. 4.3 shows the variation in F_{sw} with change in duty cycle and its effect on the values of ΔI_L and ΔV_{out}, obtained using the simulation of such a system.

The linear SSW technique is evaluated for a buck converter using GaN Systems Inc. GS66516T MOSFETs. The advantages of reduction in losses which enable higher switching frequency operation are discussed in later sections.

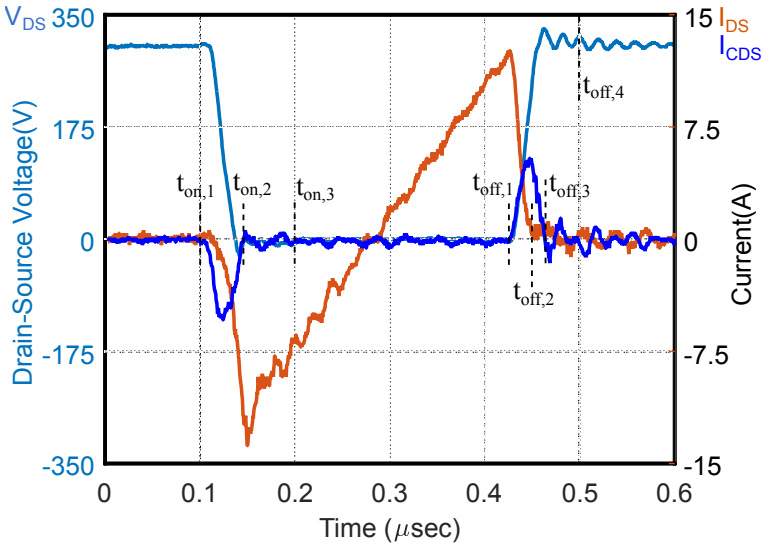


Figure 4.4: Waveforms for the turn-on and turn-off of M_2 with use of additional 330pF capacitor with the MOSFETs.

4.2 The Analytical Model

An analytical model in Section 3.2 depicts the different stages of the turn-off of a MOSFET. For the buck converter in Fig. 3.1, assuming that the inductor current remains unchanged during a switching transition, its value during the turn-off of M_2 is given by:

$$I_L = I_{DS,M2} + (C_{DS,M1} + C_{DS,M2})\frac{dV_{DS,M2}}{dt} \tag{4.2}$$

Fig. 3.4 shows the various stages during the turn-off of M_2 for the circuit of Fig. 3.1 and their occurrence in GS66516T MOSFET as shown in the waveforms of Fig. 4.4. Initially, the buck converter is operated with 300V V_{in} and 200V V_{out} in no-load condition (i.e. $I_{L,0} = 0$) with inductor current varying between ±13A. Turn-off of M_2 is initiated at time $t_{off,1}$, when $I_{DS,M2}$ begins to reduce from its peak value. $C_{DS,M1}$ and $C_{DS,M2}$ begin to discharge and charge, respectively, and $V_{DS,M2}$ increases,

shown in Fig. 3.4(b). At time $t_{off,2}$, M_2 ceases to conduct, while there is still finite current through $C_{DS,M1}$ and $C_{DS,M2}$, shown in Fig. 3.4(d). Time $t_{off,3}$ marks the completion of the turn-off of M_2 with $I_{CDS,M2}$ reduced to zero, $V_{DS,M2}$ reaching V_{in} and the reverse conduction through M_1, shown in Fig. 3.4(e). Reverse current through M_1 during the $t_{off,3} - t_{off,4}$ interval involves much greater conduction losses, as discussed earlier. From Eq. 4.2, the value of inductor current I_L flowing through $C_{DS,M1}$ and $C_{DS,M2}$ is proportional to their respective values. In this analysis, equal values of additional capacitors are used across the drain-source terminals of the two MOSFETs, resulting in equal currents through the capacitors at the time of turn-off. Since the soft-switching method results in a symmetrical system, the current $I_{CDS,M1}$ during the turn-off of M_2 is similar to $I_{CDS,M2}$ during the turn-off of M_1 between $t_{on,1} - t_{on,2}$, which have the same magnitude as $I_{CDS,M2}$ between $t_{off,1} - t_{off,3}$ when the magnitudes of $I_{L,max}$ and $I_{L,min}$ are equal. During the turn-on of M_2 in Fig. 4.4, $C_{DS,M2}$ first discharges to zero (represented by finite $I_{CDS,M2}$ during $t_{on,1} - t_{on,2}$), followed by reverse conduction through M_2 with a large on-state voltage drop between $t_{on,2} - t_{on,3}$.

Fig. 4.6 shows the waveforms during the turn-off of M_2 in a buck converter using GS66516T MOSFETs. With increase in $C_{DS,ext}$ from zero to 430 pF, the I_{DS} fall-time changes negligibly while the V_{DS} increase from zero to V_{in} is slower. The current I_{CDS} is zero in Fig. 4.6(a) due to absence of additional FET output capacitance. The magnitude of I_{CDS} increases with increase in value of $C_{DS,ext}$. A reduced rate of increase of V_{DS} due to the voltage clamping characteristic of the added capacitance reduces the voltage/current overlap and the losses during the turn-off of a MOSFET, as indicated by the analytical model. The analytical model in [19] is modified for the

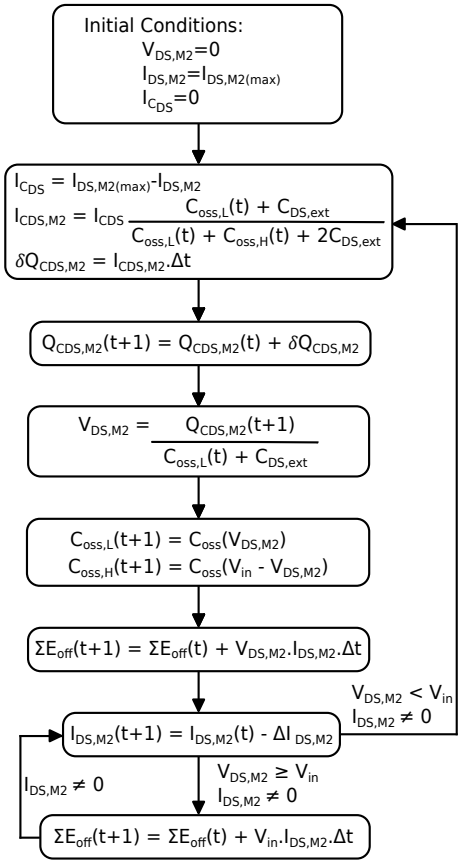
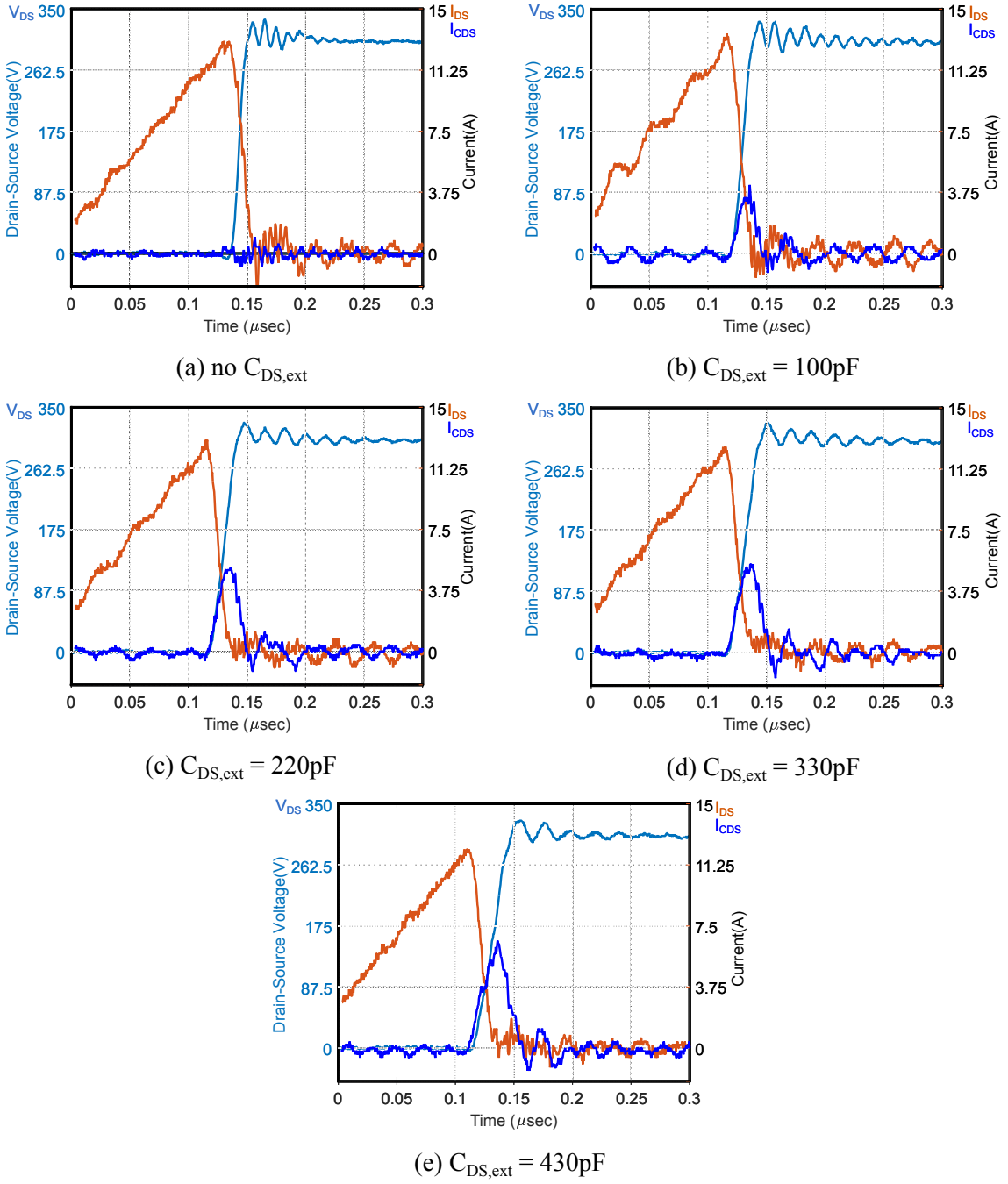


Figure 4.5: Analytical recursive model

use of additional capacitors across the drain-source terminals of both the MOSFETs in the buck converter, and shown in Fig. 4.5 and the MATLAB script in Appendix A.

4.3 Simulation and Experimental Results

The linear SSW method is validated using the discussed analytical model and in hardware with the GaN Systems Inc. GS66516T-EVBDB daughter card used with the GS665MB-EVB motherboard in a buck converter topology. Fig. 4.7 shows the



(a) no $C_{DS,ext}$

(b) $C_{DS,ext}$ = 100pF

(c) $C_{DS,ext}$ = 220pF

(d) $C_{DS,ext}$ = 330pF

(e) $C_{DS,ext}$ = 430pF

Figure 4.6: Waveforms for the turn-off of M_2 with use of additional capacitors across the MOSFETs' drain-source terminals.

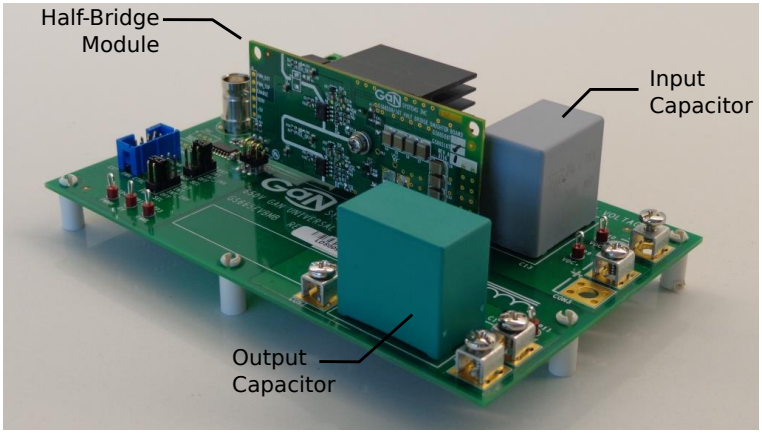


Figure 4.7: Buck converter experimental hardware.

hardware used for testing the specifications of Table 4.1. The system is run in open-loop condition with a duty cycle of 0.67 to generate 200V output from 300V input voltage. Initially, the buck converter is tested in no-load condition due to the use of MOSFETs in surface mount package and the presence of a current shunt only with the low-side switch in hardware.

The waveforms for the drain-source voltage V_{DS}, total M_2 switch position current I_T and the current through the added capacitance I_{CDS} are recorded. These waveforms are calibrated for the probe offsets and delays. Current through the M_2 channel I_{DS} is computed as the difference of I_T and I_{CDS}. It should be noted that I_{DS} still includes the current charging the parasitic output capacitance inherent to the device at the time of turn-off, but which does not contribute to the actual turn-off loss. According to Eq. 4.2, since the current through the output capacitors varies in proportion to their instantaneous values, this current through the internal capacitance could be computed and subtracted from I_{DS} to get the actual current through the M_2 channel for a more accurate calculation of its turn-off losses. The losses from experiment are calculated as the time integral of the product of the instantaneous

Table 4.1: Test conditions, components and equipment used for testing

Type	Specification
Input Voltage	300V
Output Voltage	200V (Duty cycle=0.67)
Switching Frequency	1 MHz
Output Power	No-Load to 1kW
MOSFET	GS66516T,650V/60A/25mΩ GaN MOSFET
Gate Driver	SI8271GB-IS, $R_{g,ext}$(On/Off)= 10 Ω/2 Ω
Inductor	2.1μH
Oscilloscope	Tektronix MDO3024, 200MHz/2.5GS/s
Voltage Probe	Tektronix TPP0250, 250MHz, 3.9pF/10MΩ
Current Sensor	PEM CWTUM/3/B Rogowski Current Transducer

V_{DS} and I_{DS} for M_2 using the MATLAB script in Appendix B.

Fig. 4.8 shows the variation in the turn-off losses with use of an additional capacitance between zero to 430pF across both the MOSFETs in the buck converter. It is seen that the turn-off losses reduce on loading with additional capacitance according to both the analytical model and in hardware. The analytical model predicts a reduction in the turn-off losses to 22.1% of those in the unloaded condition with use of 430pF capacitors with both the MOSFETs. The losses from experiment are greater than the predictions from the analytical model due to the inclusion of the current charging the intrinsic device parasitic capacitance, as discussed earlier. The aberrant data point for the experimental turn-off loss with 330pF additional capacitance is attributed to measurement error. The experimental losses, when compensated for the current through the MOSFET's inherent parasitic output capacitance, yield values very close to those from the analytical model. This underscores the utility of the analytical model for computation of the actual MOSFET turn-off losses and their

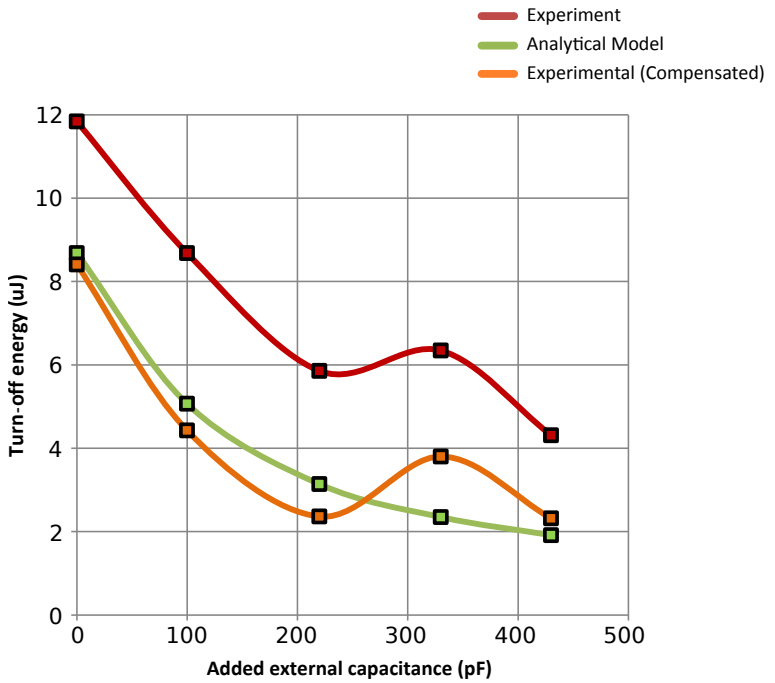


Figure 4.8: Reduction in the turn-off losses using the analytical model and in experiment (with and without effect of current in the FET inherent parasitic capacitance)

reduction with the use of the additional capacitance for linear SSW. The loss calculations with compensation in experiment show a reduction by 27.6% from 8.41μJ to 2.31μJ with use of the same capacitor values.

Next, the buck converter is tested at increased output power P_{out} levels upto 1kW. The increase in P_{out} and $I_{L,0}$ reduces the magnitude of the negative $I_{L,min}$ from the no-load condition. Fig. 4.9 shows the waveforms for M_2 with P_{out} of 1 kW and 330 pF additional capacitors with the MOSFETs. Since the magnitude of $I_{L,max}$ is greater than $I_{L,min}$, the amplitude of I_{CDS} is greater at the turn-on instant than at the turn-off instant. This causes a faster commutation from M_1 to M_2 than from M_2 to M_1. The values for voltage and current are measured at the buck converter input and output terminals to determine the overall system losses with increase in P_{out}. In order

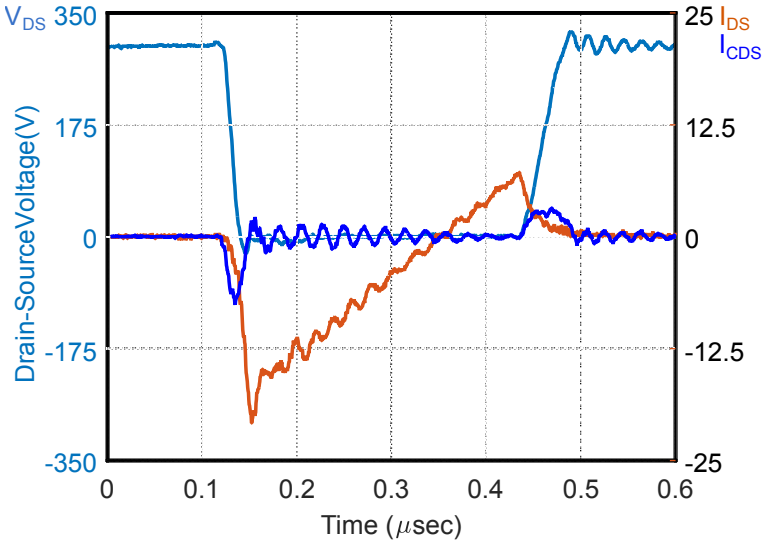


Figure 4.9: Waveforms for the turn-on and turn-off of M_2 with use of additional 330pF capacitor with the MOSFETs in the buck converter at 1kW output power.

to estimate the benefits with the use of the linear SSW method, the buck converter is also tested with a larger $20.7\mu H$ inductance (realized using 23 units of Coilcraft's SER2009-901MLB $0.9\mu H$ inductors in series) and positive $I_{L,min}$ with hard-switching (HSW). Due to the large values of the turn-on losses, the HSW system is operated only upto 500 W with the same 300 V input and duty cycle. For comparison with the linear SSW results, the values of losses with HSW are extrapolated upto 1 kW, shown by the shaded region in Fig. 4.10. It is also seen that:

1. The losses in experiment with linear SSW increase marginally with increase in P_{out}, shown in figures (a) and (c). This is due to the small change in the values of MOSFET current with output load at the time of device turn-off.

2. Using linear SSW, the overall losses in the system and the switches reduce with the use of 330pF capacitors with the MOSFETs, shown in figures (a) and (c). The degree of reduction in the turn-off losses with use of additional capacitors is not

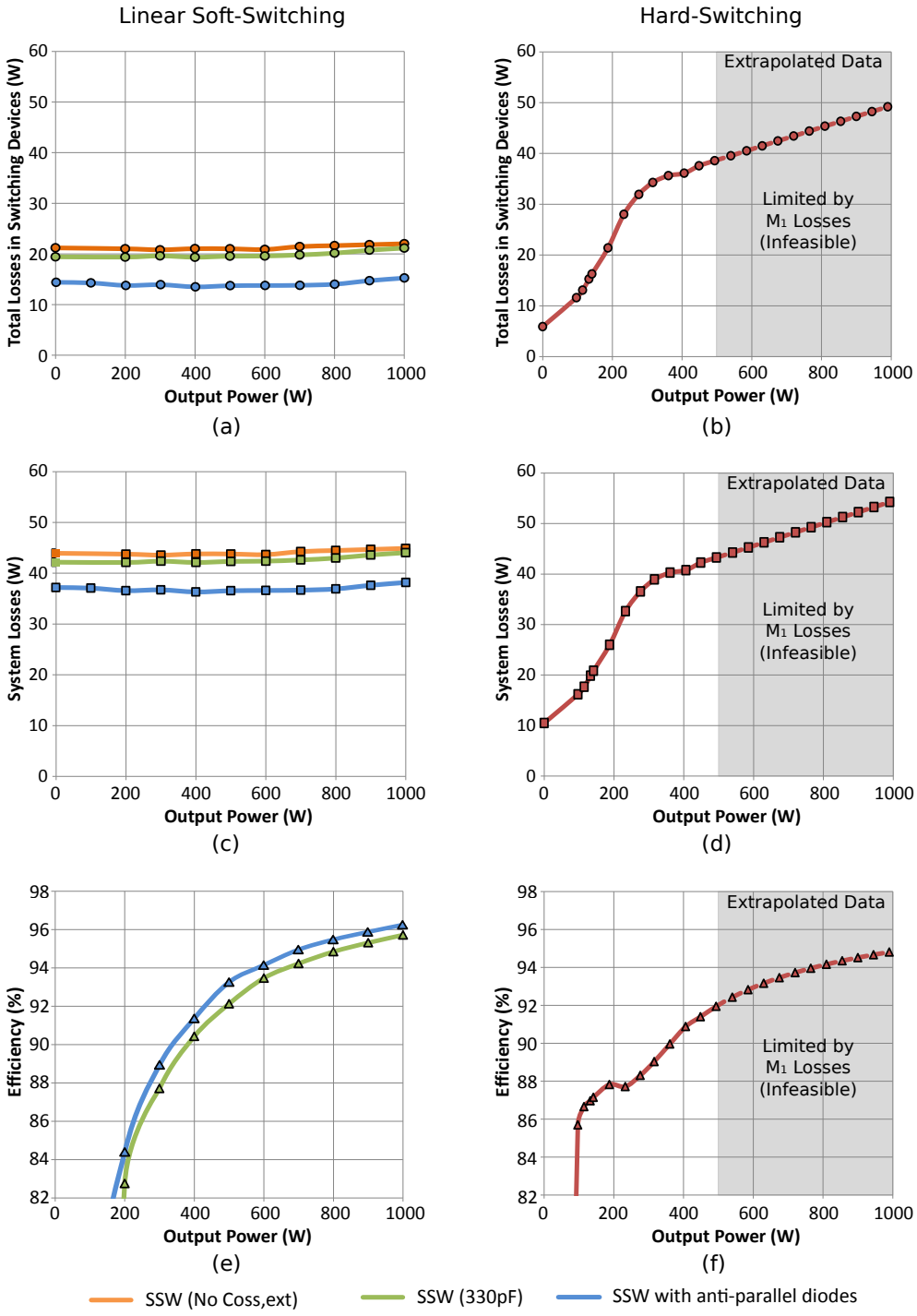


Figure 4.10: Losses and efficiency in a buck converter at 1MHz switching frequency with linear soft-switching and hard-switching.

clearly evident since these do not dominate the total losses in the switches.

3. For simplicity, the linear SSW testing uses off-shelf inductors from Coilcraft which have significant AC losses for given large ΔI_L values. It is due to this reason that the inductor losses form a major portion of the overall losses in figure (c). A dedicated inductor designed for the given F_{sw} and ΔI_L values would cause a significant reduction in the inductor losses.

4. The losses in the switches with HSW exceed those with SSW for P_{out} greater than 200 W, shown in figures (a) and (b). The inductor losses, which form a major portion of the overall losses with SSW, are calculated using the loss models from Coilcraft [56], and these along with the losses in the input and output capacitors are subtracted from the overall losses to get the total losses in the switches which limit the maximum F_{sw}.

5. The overall losses with HSW exceed those with SSW for P_{out} greater than 450 W, as seen in figures (c) and (d).

6. The greater losses in the switches with HSW are concentrated in M_1, while these are evenly distributed between both M_1 and M_2 in a system with linear SSW, enabling higher F_{sw}.

7. Further, the use of anti-parallel SiC schottky diodes (C3D10065E from Cree Inc.) with small junction capacitance, in addition to the 330 pF capacitors with M_1 and M_2 reduces the overall losses and improves the system efficiency, as seen in figures (a), (c) and (e). This is due to their smaller forward voltage drop, lower by nearly 60-70% of the voltage drop across M_1 and M_2 during reverse conduction. This also moves the dead-time conduction losses away from M_1 and M_2, making

scope for buck converter operation at P_{out} greater than 1 kW or use of even higher switching frequency.

The losses for P_{out} of 500 W and 1 kW are also estimated analytically with the sources of contributing losses for operation with both HSW and linear SSW, shown in Fig. 4.11 using the relations:

$$\begin{cases} P_{c(R_{DS})} = R_{DS,on}\left[(I_{L,0})^2 + \dfrac{(\Delta I_L)^2}{12}\right]\left[1 - \dfrac{\sum t_{rev}}{T_{SW}}\right] \\ P_{c(rev)} = \dfrac{1}{T_{sw}}\sum V_{SD} I_{SD} t_{rev} \\ P_{C_{in}} = R_c D\left[I_{L,0}^2(1-D) + \dfrac{(\Delta I_L)^2}{12}\right] \\ P_{C_{out}} = R_c \dfrac{(\Delta I_L)^2}{12} \end{cases} \tag{4.3}$$

where $P_{c(R_{DS})}$ are the conduction losses for current flow through the FET channel, $P_{c(rev)}$ are the FET conduction losses during reverse conduction in the off-state condition for duration t_{rev}, $P_{C_{in}}$ and $P_{C_{out}}$ are the losses in the ESR of the input and output capacitors [57], respectively. The inductor losses are obtained using the Coilcraft models [56] and the MOSFET turn-off switching losses are computed using the analytical model discussed earlier.

The analytical estimations in Fig. 4.11 for linear SSW system (with and without anti-parallel SiC schottky diodes) match closely with the results from experimentation. These calculations with HSW operation assume linear variation in the turn-on losses with change in V_{DS}/I_{DS} [52]. This causes an underestimation of these losses since the turn-on losses for small values of I_{DS} are greater than those given by linear approximations [44]. It is seen that the turn-on losses in M_1 in Fig. 4.11(a) and Fig. 4.11(b) are replaced with the turn-off losses in M_2 as seen in Fig. 4.11(c) and

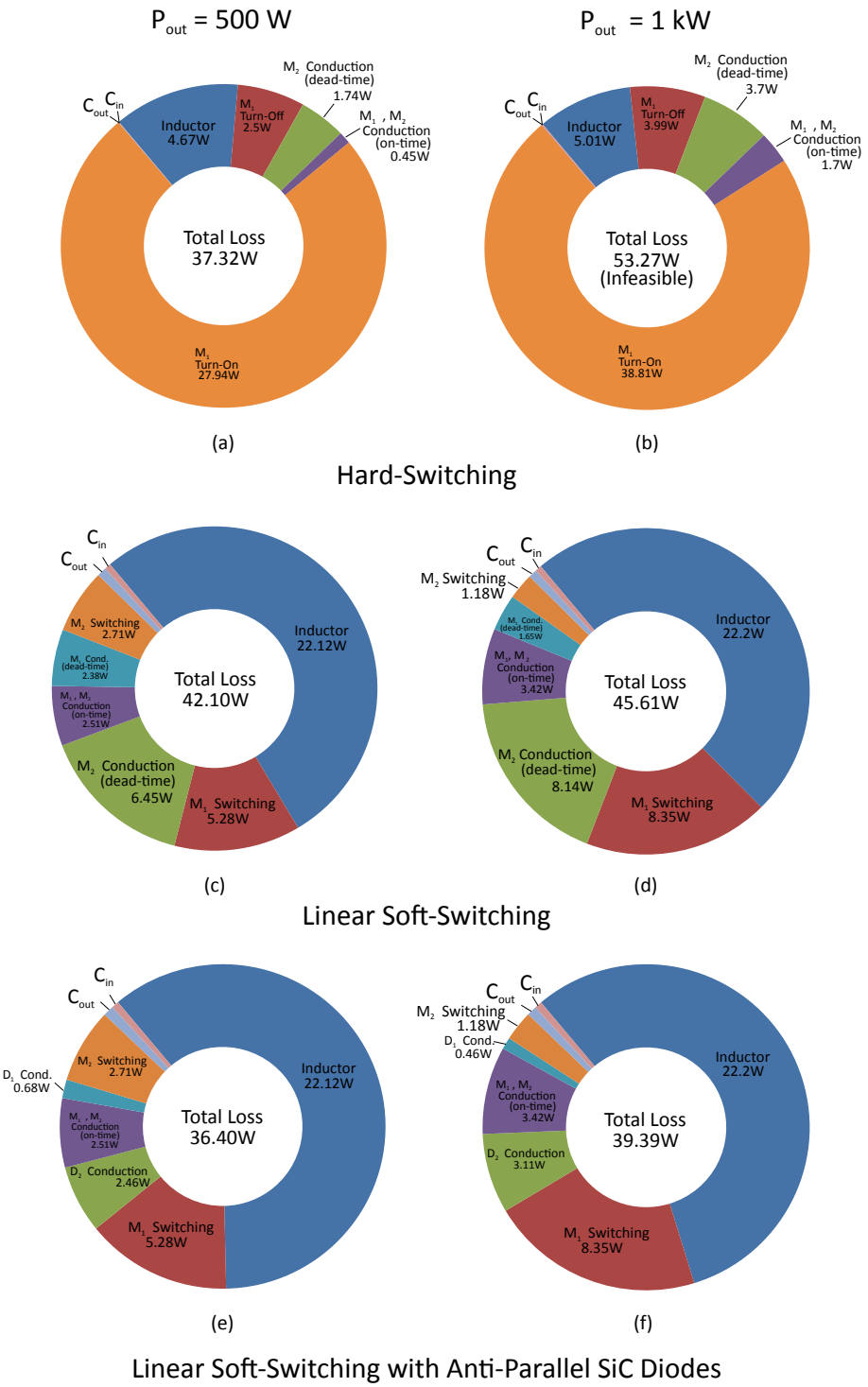
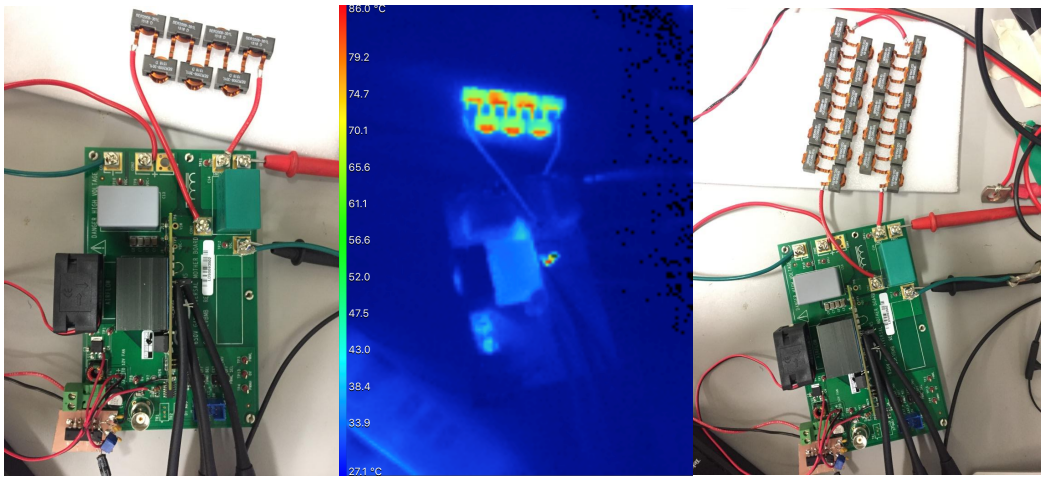


Figure 4.11: Power loss estimation using analytical calculations and models at 1MHz for different P_{out}.

Fig. 4.11(d) with the use of the linear SSW method. Buck converter testing with 330pF capacitors at 1 kW P_{out} result in overall losses of 44.04W and 95.7% conversion efficiency. The use of anti-parallel SiC diodes with the MOSFETs is shown to reduce losses further and improve efficiency in Fig. 4.11(e) and Fig. 4.11(f). The system efficiency would be further improved with the use of gate drive dead-times just sufficient for the design specifications and the intended capacitive loading on the MOSFETs or predictive dead-time control techniques [43], unlike the use of large $100ns$ dead-time values per transition in this analysis to prevent device failure when loading with large capacitors. This open-loop experimentation is a validation near the worst-case operating point and the losses in the switches and the inductor will reduce significantly with reduction in F_{sw} at points away from the $D = 0.5$ condition. Loss predictions of nearly 43.82 W on M_1 in Fig. 4.11(b) would cause a device failure at 27^oC ambient.

Fig. 4.12(b) shows the steady state thermal image with forced air cooling at 27^oC ambient for the top-view of the buck converter of Fig. 4.12(a) using $2.1\mu H$ inductor and the linear SSW method. The inductors reach a maximum temperature of 78.4^oC due to their large losses. The heat sink with the MOSFETs is at 35.1^oC. Considering the half-bridge module, input/output capacitors and inductors which form the buck converter unit, a power conversion density of 7.8 kW/L is achieved. The buck converter of Fig. 4.12(c) with HSW is larger in volume and dissipates similar losses at a smaller P_{out}. A reduction in its switching frequency to reduce the switching losses would require a larger inductance value for same ΔI_L which would make the inductor even bigger. The switch losses in a HSW system are greater than those in a system using the linear SSW method. For the case with 500 W P_{out}, the



(a) (b) (c)

(a) Top-view of the buck converter board using 2.1 µH inductor and the linear SSW method (b) Thermal image for operation of the top system at 1 kW with forced air cooling at 27°C (c) Top-view of buck converter using 20.7 µH inductor and hard switching. Its steady-state thermal image is not captured to avoid system failure due to large switch losses and the resultant heating.

Figure 4.12: Buck converter setup including inductors with linear SSW and HSW control

reduction in the losses in M_1 by nearly five times from a HSW system with the use of the linear SSW technique would enable an increase in the switching frequency by the same ratio with the given cooling system between the different control methods. This highlights the utility of the soft-switching method in reducing the losses per switching cycle, to enable operation at higher switching frequencies for a given cooling system design and smaller size of the passive components.

4.4 Summary

This chapter discussed the use of the linear soft-switching method in extending the operating switching frequencies of power converters using wide bandgap devices to

MHz range. An analytical model was validated for GaN System's GS66516T MOSFET product and the reduction in its turn-off losses was verified in hardware. This reduction in losses per switching cycle was used to realize a buck converter with a 1MHz switching frequency, 1 kW output power and a 7.8 kW/L power conversion density with forced air cooling. A comparison with the traditional hard-switched buck converter indicates a potential to use five times higher switching frequency with the use of this method while staying within the device power dissipation limits and a given cooling system design. The use of anti-parallel SiC diodes with the MOSFETs is shown to reduce losses and improve efficiency further. Since a majority of the power converter topologies include a half-bridge, this soft-switching method could be extended to other such systems to realize power converters with high switching frequency and small size of the passive components.

Chapter 5

Conclusions & Future Work

5.1 Conclusion

Power loss calculations are critical to a power converter design, helping with estimation of efficiency, switch selection and cooling system design. Power losses in a MOSFET limit the maximum switching frequency in a power converter. Continuous efforts are being made for the design of high power density converters switching at high frequency. Switching energy values aren't always available in MOSFET datasheets at all operating points, and calculation of voltage and current rise-time and fall-time is needed. This thesis discussed various methods for estimation of the switching transition times and power losses, using datasheet parameters, including SiC MOSFETs with varying miller plateau voltage. Three methods are used to evaluate a certain MOSFET product, and calculated values were compared with results from PLECS simulation and double pulse test experiment. It is observed that the proposed model overestimates switching energies, with values close to actual device characteristics with worst-case 30% deviation from experimental values, in comparison with existing

methods and could be used for the estimation of switching energies for MOSFETs in cases where these values are not available in the datasheet at all required operating points.

The advent of Silicon-Carbide and Gallium-Nitride MOSFETs offers potential to realize power converters operating at even higher switching frequencies. At a given value of drain-source voltage and current, the turn-on losses in a MOSFET are usually greater than the turn-off losses. A linear soft-switching technique is introduced for power converters using wide bandgap devices to replace the larger turn-on losses with smaller turn-off losses and thus reduce the power dissipation of the overall system. The turn-off losses are further reduced with use of additional capacitance across the MOSFET drain-source terminals. An analytical model is realized for estimation of the turn-off energies and their reduction with the use of additional drain-source capacitance. Results from an analytical model, LTSpice simulation and experimentation are shown to match closely for SiC MOSFETs.

The linear soft-switching method is further evaluated for use with Gallium-Nitride devices switching at 1 MHz frequency in a buck converter topology. Switching energy computations from hardware are modified to include the effect of the current through the MOSFET stray output capacitance, and results from the analytical model are found to predict the actual values of turn-off energies closely. The proposed method moves the location of losses from the high-side MOSFET in a hard-switched system to both the switching devices with use of linear soft-switching, making it possible to use higher switching frequencies. The results from an analytical model and experimentation show benefits of reduction in the switch losses leading to a possible increase in the switching frequency and reduction in the values of the passive components

by five times as compared to a buck converter with a larger inductance and small current ripple for a given cooling system. The overall losses in a system with linear soft-switching are shown to further reduce with the use of anti-parallel SiC schottky diodes with the MOSFETs.

5.2 Future Work

The linear soft-switching is found to have enabled operation at switching frequencies in MHz range in a buck converter using GaN devices, and use of minimum number of additional components. The higher reverse conduction losses in the GaN MOSFETs are reduced with the use of anti-parallel SiC schottky diodes. Unlike the off-shelf inductors used in this analysis, an inductor designed for large current ripple values and switching frequencies in MHz range would reduce the core losses seen here significantly. With use of SiC schottky diodes and a custom inductor, the buck converter could be tested at output power greater than 1 kW to realize even higher efficiency and power density.

Appendix

A Analytical Model MATLAB Script

```
%% Read Coss values from the datasheet
Vds_Coss  = csvread('Coss_66516.csv',1,0);
Voltage           = Vds_Coss(:,1);
Coss              = Vds_Coss(:,2)*1e-12;
func              = polyfit(Voltage,Coss,10);

%% Test condition and user inputs
Vin=300;
Ids_max=18;
Cextra  = 330*1e-12;
tfi=20.8e-9;
DeltaT=0.1e-9;
steps=tfi/DeltaT;

%% Initial conditions
Vds=0;
Q=0;
Eoff=0;
Ids = Ids_max;

Coss_L          = polyval(func,Vds);
Coss_H          = polyval(func,(Vin-Vds));

%% Calculate turn-off switching energy
while Ids > 0
    Icds = Ids_max-Ids;
    IcdsM2 = Icds*(Coss_L+Cextra)/(Coss_L+Coss_H+2*Cextra);
    Icds_int=IcdsM2*Coss_L/(Coss_L+Cextra);
    if Vds < (Vin+3.33)
        dQ = IcdsM2*DeltaT;
        Q = Q + dQ;
        Vds = Q/(Coss_L+Cextra);
        Coss_L = polyval(func,Vds);
        Coss_H = polyval(func,(Vin-Vds));
        Vds_plot=[Vds_plot Vds];
        Ids_plot=[Ids_plot Ids];
        Eoff=Eoff+Vds*(Ids)*DeltaT;
    else
        Eoff=Eoff+Vin*Ids*DeltaT;
    end
    Ids=Ids-(Ids_max/steps);
end
```

B Experimental Loss Calculations MATLAB Script

```
%% Read experimental data from excel file
Data   = csvread('tek0003.csv',1300,0);
Time   = Data(:,1)*1e6;

%% Compensate for probe offsets
time_offset=Time(1);
Time   = Time-time_offset;
V_R = Data(:,4)-1;
I_total = Data(:,3)+0.3;   % adding offset to make current value 0
I_Coss = Data(:,2)-0.1;
V_R = [0;0;0;V_R];
I_total = [1 ; 1 ; 1 ; I_total];
I_Coss = [I_Coss ; 0 ; 0 ; 0];
Time = Time + 0.0012;
Time = [0; 0.0004;0.0008;Time];
I_delay=-0.0032;
I_delay_samples=I_delay/0.0004;

%% Calculate variables of interest
I_R = I_total-I_Coss;

%% Determine last time when voltage exits 0V
for i=1:numel(Time)
    if(V_R(i)<=0.5)
        T1=i;
    end
end
T_V_last0=Time(T1)

%% Determine first time when current reaches 0A
for i=1:numel(Time)
    if(I_R(i)<=1e-3)
        T2=i;
        break;
    end
end
T_I_first0=Time(T2)

%% Calculate switching energy
Eoff=0; % Initial Value

for i=(T1+1):1:(T2-I_delay_samples)
    Eoff = Eoff + ((V_R(i-1))*(I_R(i-1+I_delay_samples))*(Time(i)-Time(i-1)));
end
```

References

[1] R. Hou, P. Magne, B. Bilgin, and A. Emadi, "A Topological Evaluation of Isolated DC/DC Converters for Auxiliary Power Modules in Electrified Vehicle Applications," *Proc. IEEE Applied Power Electronics Conference and Exposition*, pp. 1360–1366, 2015.

[2] N. Mohan, W. P. Robbin and T. Undeland, "Power Electronics: Converters, Applications, and Design," *2nd ed. New York: Wiley, 1995.*

[3] A. Pressman, K. Billings, and T. Morey, "Switching Power Supply Design," *New York, NY, USA: McGraw-Hill Books, 2009.*

[4] J. Mahdavi, A. Emaadi, M. Bellar, and M. Ehsani, "Analysis of Power Electronic Converters Using the Generalized State-Space Averaging Approach," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 44, no. 8, pp. 767–770, 1997.

[5] B. Agrawal and S. Dixit, "Isolated 70-W Streetlight LED Driver Using UCC28810," pp. 1–24, 2015. [Online]. Available: http://www.ti.com/lit/an/slua752/slua752.pdf[2017,May.05]

[6] A. Emadi, "Advanced Electric Drive Vehicles," *Boca Raton, FL, USA: CRC Press, 2014.*

[7] R. W. Erickson and D. Maksimovic, "Fundamentals of Power Electronics," *2nd ed. New York, NY, USA: Springer, 2001.*

[8] M. Trivedi and K. Shenai, "Evaluation of planar and trench IGBT for hard- and soft-switching performance," *Proc. IEEE Industry Applications Conference,Phoenix, AZ*, pp. 717–721, 1999.

[9] H. Qin, B. Zhao, W. Xu, J. Wen, and Y. Yan, "Evaluation of performance improvement of Silicon Carbide MOSFETs based DC-DC converter," *Proc. IEEE 7th International Power Electronics and Motion Control Conference*, pp. 889–894, 2012.

[10] B. J. Baliga, "The Future of Power Semiconductor Device Technology," *Proceedings of the IEEE*, vol. 89, no. 6, pp. 822–832, 2001.

[11] R. L. Boylestad and L. Nashelsky, "Electronics Devices and Circuit Theory," *11th ed. Toronto: Prentice Hall, 2001.*, vol. 11, 2015.

[12] Y. Xu, J. Gu, H. Chen, Z. Chen, Y. Pu, and A. L. Category, "Power Loss Calculation for the Power Converter in Switched Reluctance Motor Drive," *Proc. IEEE International Conference on Information and Automation, Hailar*, pp. 19–24, 2014.

[13] B. Bilgin, P. Magne, P. Malysz, Y. Yang, V. Pantelic, M. Preindl, A. Korobkine, W. Jiang, M. Lawford, and A. Emadi, "Making the Case for Electrified Transportation," *IEEE Transactions on Transportation Electrification*, vol. 1, no. 1, pp. 4–17, 2015.

[14] C. Xiao, G. Chen, and W. G. Odendaal, "Overview of Power Loss Measurement Techniques in Power Electronics Systems," *IEEE Transactions on Industry Applications*, vol. 43, no. 3, pp. 657–664, 2007.

[15] Y. Rao, S. P. Singh, and T. Kazama, "A Practical Switching Time Model for Synchronous Buck Converters," *Proc. IEEE Applied Power Electronics Conference and Exposition, Long Beach, CA*, pp. 1585–1590, 2016.

[16] "Power MOSFET Basics: Understanding Gate Charge and Using it to Assess Switching Performance," 2016. [Online]. Available: https://www.vishay.com/docs/73217/an608a.pdf[2017,Jun.07]

[17] Y. Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical Loss Model of Power MOSFET," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 310–319, 2006.

[18] J. Guo, H. Ge, J. Ye, and A. Emadi, "Improved method for MOSFET voltage rise-time and fall-time estimation in inverter switching loss calculation," *Proc. IEEE Transportation Electrification Conference and Expo, Dearborn, MI*, pp. 1–6, 2015.

[19] B. Agrawal, M. Preindl, B. Bilgin, and A. Emadi, "Estimating Switching Losses for SiC MOSFETs with Non-Flat Miller Plateau Region," *Proc. IEEE Applied Power Electronics Conference and Exposition, Tampa, FL*, pp. 2664–2670, 2017.

[20] "Cree: CAS300M12BM2 Silicon-Carbide Half-Bridge Module Datasheet," 2014. [Online]. Available: http://www.wolfspeed.com/downloads/dl/file/id/183/product/101/cas300m12bm2.pdf[2017,May.05]

[21] G. Hua and F. C. Lee, "Soft-switching techniques in PWM converters," *IEEE Transactions on Industrial Electronics*, vol. 42, no. 6, pp. 595–603, 1995.

[22] T. W. Ching and K. U. Chan, "Review of soft-switching techniques for high-frequency switched-mode power converters," *Proc. IEEE Vehicle Power and Propulsion Conference, Harbin*, pp. 1–6, 2008.

[23] M. D. Bellar, T. S. Wu, A. Tchamdjou, J. Mahdavi, and M. Ehsani, "A review of soft-switched DC-AC converters," *IEEE Transactions on Industry Applications*, vol. 34, no. 4, pp. 847–860, 1998.

[24] C. A. Canesin, "Novel zero-current-switching pwm converters," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 3, pp. 372–381, 1997.

[25] H. Zhang, L. M. Tolbert, and B. Ozpineci, "Impact of SiC devices on hybrid electric and plug-in hybrid electric vehicles," *IEEE Transactions on Industry Applications*, vol. 47, no. 2, pp. 912–921, 2011.

[26] X. Li, L. Zhang, S. Guo, Y. Lei, A. Q. Huang, and B. Zhang, "Understanding Switching Losses in SiC MOSFET: Toward Lossless Switching," *Proc. IEEE 3rd*

Workshop on Wide Bandgap Power Devices and Applications, Blacksburg, VA, pp. 257–262, 2015.

[27] J. Cao, D. Bharathan, and A. Emadi, "Efficiency and Loss Models for Key Electronic Components of Hybrid and Plug-in Hybrid Electric Vehicles' Electrical Propulsion Systems," *Proc. IEEE Vehicle Power and Propulsion Conference*, pp. 477–482, 2007.

[28] B. Agrawal, M. Preindl, and A. Emadi, "Turn-off Energy Minimization for Soft-Switching Power Converters with Wide Bandgap Devices," *Proc. IEEE International Conference on Industrial Technology, Toronto, ON, Canada*, pp. 236 – 241, 2017.

[29] J. Zhang, J.-S. Lai, and R.-Y. Kim, "High-Power Density Design of a Soft-Switching High-Power Bidirectional dc-dc Converter," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1145–1153, 2007.

[30] "GaN Systems: GS66516T Top-side cooled 650 V E-mode GaN transistor datasheet." [Online]. Available: http://www.gansystems.com/datasheets/GS66516TDSRev170413.pdf[2017,May.10]

[31] T. Horiguchi, S. I. Kinouchi, Y. Nakayama, and H. Akagi, "A fast short-circuit protection method using gate charge characteristics of SiC MOSFETs," *Proc. IEEE Energy Conversion Congress and Exposition, Montreal, QC*, pp. 4759–4764, 2015.

[32] L. Balogh, "Design and Application Guide For High Speed MOSFET Gate Drive Circuits." [Online]. Available: http://www.radio-sensors.se/download/gate-driver2.pdf[2016,Oct.10]

[33] D. Graovac, M. Pürschel, and A. Kiep, "MOSFET Power Losses Calculation Using the Datasheet Parameters," *Infineon Application Note*, 2006.

[34] Y. Xiong, S. Sun, H. Jia, P. Shea, and Z. John Shen, "New physical insights on power MOSFET switching losses," *IEEE Transactions on Power Electronics*, vol. 24, no. 2, pp. 525–531, 2009.

[35] Z. J. Shen, Y. Xiong, X. Cheng, Y. Fu, and P. Kumar, "Power MOSFET Switching Loss Analysis : A New Insight," in *Proc. IEEE Industry Applications Conference Forty-First IAS Annual Meeting, Tampa, FL*, 2006, pp. 1438–1442.

[36] A. K. Agarwal, "An overview of SiC power devices," *Proc. International Conference on Power, Control and Embedded Systems, Allahabad*, pp. 1–4, 2010.

[37] F. Xu, B. Guo, L. M. Tolbert, F. Wang, and B. J. Blalock, "An All-SiC Three-Phase Buck Rectifier for High-Efficiency Data Center Power Supplies," *IEEE Transactions on Industry Applications*, vol. 49, no. 6, pp. 2662–2673, 2013.

[38] H. Li and S. Munk-Nielsen, "Detail study of SiC MOSFET switching characteristics," *Proc. IEEE 5th International Symposium on Power Electronics for Distributed Generation Systems, Galway*, pp. 1–5, 2014.

[39] K. Yang, J. Guo, H. Ge, B. Bilgin, V. Loukanov, and A. Emadi, "Transient electro-thermal analysis for a MOSFET based traction inverter," *Proc. IEEE*

Transportation Electrification Conference and Expo, Dearborn, MI, pp. 1–6, 2014.

[40] J. Popovic-Gerber, M. Gerber, and B. Ferreira, "An approach to building more compact power electronic converters," *Proc. European Conference on Power Electronics and Applications, Aalborg*, pp. 1–10, 2007.

[41] J. Rivas, D. Jackson, O. Leitermann, A. Sagneri, and D. Perreault, "Design considerations for very high frequency DC-DC converters," *Proc. IEEE 37th Annu. Power Electronics Specialists Conference*, pp. 2287–2297, 2006.

[42] J. W. Kolar, F. Krismer, and H. P. Nee, "What are the Big Challenges in Power Electronics?" *Keynote Presentation at the 8th IEEE International Conference on Integrated Power Electronics Systems*, 2014.

[43] L. Schirone, M. Macellari, and F. Pellitteri, "Predictive dead time controller for GaN-based boost converters," *IET Power Electronics*, vol. 10, no. 4, pp. 421–428, 2017. [Online]. Available: http://digital-library.theiet.org/content/journals/10.1049/iet-pel.2015.0551

[44] "Cree: C2M0025120D Silicon Carbide Power MOSFET Datasheet." [Online]. Available: www.wolfspeed.com/media/downloads/161/C2M0025120D.pdf[2017, Apr.24]

[45] E. A. Jones, F. Wang, D. Costinett, Z. Zhang, and B. Guo, "Temperature-dependent turn-on loss analysis for GaN HFETs," *Proc. IEEE Applied Power Electronics Conference and Exposition, Long Beach, CA*, pp. 1010–1017, 2016.

[46] B. Wang, T. Q. Zheng, and J. Zhang, "Voltage controlled variable capacitor based snubber for the further reduction of IGBT's turn-off loss," *Proc. IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA*, pp. 935–940, 2014.

[47] H. H. Chang, S. Y. Tseng, and J. G. Huang, "Interleaving boost converters with a single-capacitor turn-off snubber," *Proc. IEEE Annual Power Electronics Specialists Conference, Jeju, Korea*, pp. 1–7, 2006.

[48] S. S. Saha, B. Majumdar, T. Halder, and S. K. Biswas, "New Fully Soft-Switched Boost-Converter with Reduced Conduction Losses," *Proc. International Conference on Power Electronics and Drives Systems, Kuala Lumpur, Malaysia*, pp. 107–112, 2005.

[49] M. Mohammadi, E. Adib, and M. R. Yazdani, "Family of soft-switching single-switch PWM converters with lossless passive snubber," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 6, pp. 3473–3481, 2015.

[50] C. Henze, H. Martin, and D. Parsley, "Zero-voltage switching in high frequency power converters using pulse width modulation," *Proc. IEEE Applied Power Electronics Conference and Exposition, New Orleans, LA*, pp. 33–40, 1988.

[51] H. Gamo, "A General Formulation of Faraday's Law of Induction," *Proceedings of the IEEE*, vol. 67, no. 4, pp. 676–677, 1979.

[52] M. Eull, M. Preindl, and A. Emadi, "Analysis and Design of a High Efficiency, High Power Density Three-Phase Silicon Carbide Inverter," *Proc. IEEE Transportation Electrification Conference and Expo, Dearborn, MI*, pp. 1–6, 2016.

[53] K. H. Liu and C. Y. Lee, "Zero-voltage switching technique in DC/DC converters," *IEEE Transactions on Power Electronics*, vol. 5, no. 3, pp. 293–304, 1990.

[54] A. Merkert, J. Muller, and A. Mertens, "Component Design and Implementation of a 60 kW Full SiC Traction Inverter with Boost Converter," *Proc. IEEE Energy Conversion Congress and Exposition, Milwaukee, WI*, pp. 1–8, 2016.

[55] G. Sarriegui, S. Beushausen, and R. W. D. Doncker, "Comparison of high frequency inductors for bidirectional DC-DC converters for electric vehicles," *Proc. European Conference on Power Electronics and Applications, Karlsruhe*, pp. 1–8, 2016.

[56] "Coilcraft: Inductor Loss Calculation Tool." [Online]. Available: http://www.coilcraft.com/apps/power{_}tools/compare/[2017,May.16]

[57] R. C. Wong, H. A. Owen Jr., and T. G. Wilson, "Parametric study of minimum converter loss in an energy-storage DC-to-DC converter," *Proc. IEEE Power Electronics Specialists conference, Cambridge, MA*, pp. 411–425, 1982.