LOW-VOLTAGE, LOW-POWER CMOS DOWNCONVERSION MIXERS

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By

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ABSTRACT

In past years, wireless technology has seen an incredible boom. As a result, industry has gone to great lengths to make wireless devices cheaper, smaller, faster and less power-hungry. This has prompted a significant interest in the research world to design circuit components that would facilititate these goals. However, much of the focus has been on wireless technology for communications applications, such as wireless telephony and wireless computer networking. More recently, there has been a focus on developing circuits for other wireless applications, one of which is wireless sensor networks. Such applications would demand extremely low-power operation, especially from the RF front-end. We have concentrated on achieving low-power operation for one of the important building blocks of the RF transceiver, which is the frequency downconversion mixer.

In this thesis, we describe the design and results of two mixers, both designed in CMOS 0.18μm technology offered by the Canadian Microelectronics Corporation (CMC). The first design uses the body terminal of the transistor as one of the inputs. This method allows for the radio-frequency (RF) and local oscillator (LO) stages in traditional switching mixers to be collapsed into one stage, thereby allowing for operation at lower supply voltages and lower power comsumption levels. This mixer was designed to downconvert a 1.9GHz RF signal to a 250MHz intermediate-frequency (IF) signal. The measured performance characteristics resulted in a power consumption of 400μW from a 0.8V supply,

a conversion gain of 1dB, a single sideband (SSB) noise figure of 11dB, and an input-referred 3rd-order intercept point (IIP3) of -9dBm.

The second mixer design used a folding architecture to reduce the supply voltage headroom needed, as well as distribute the current appropriately for high-gain and low-power operation. This mixer was designed to downconvert a 2.4GHz RF signal to a 100MHz IF signal. The simulated performance characteristics showed a power consumption of 640μW from a 1V supply, a conversion gain of 4dB, a SSB noise figure of 19dB, and an IIP3 of -6.5dBm.

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There are several people who made my graduate studies at McMaster both enjoyable and fruitful. I would like to start by thanking Dr. M. Jamal Deen for his supervision of my Master's thesis work. His supervision, assistance and constant feedback are what have made this thesis, and the work presented herein, possible.

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On a personal level, I could never have accomplished what I have without constant encouragement and help from my parents, Akber and Sabira, and my siblings, Nashat and Zahra. Towards the end of my graduate studies, I also had the added support of my fiancée Samina, without whose support I could not have completed this work.

LIST OF ACRONYMS

BER	Bit Error Rate
BJT	Bipolar Junction Transistor
CG	Conversion Gain
CMC	Canadian Microelectronics' Corporation
CMOS	Complementary Metal-Oxide-Semiconductor
DC	Direct Current
DSB	Double Sideband (referring to Noise Figure)
FET	Field Effect Transistor
LO	Local Oscillator
IF	Intermediate Frequency
IIP3	3rd-order Input-Referred Intercept Point
IM3	3rd-order Intermodulation Distortion Level
LNA	Low-Noise Amplifier
mds	Minimum Detectable Signal
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NF	Noise Figure
nMOS	n-type Metal-Oxide-Semiconductor (transistor)
OIP3	3rd-order Output-Referred Intercept Point

PLL	Phase-Locked Loop
pMOS	p-type Metal-Oxide-Semiconductor (transistor)
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
SFDR	Spurious-Free Dynamic Range
SNR	Signal-to-Noise Ratio
SSB	Single Sideband (referring to Noise Figure)
VCO	Voltage-Controlled Oscillator

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Chapter 1

INTRODUCTION

1.1 MOTIVATION

The significant increase in interest in wireless communication systems in recent decades has given rise to an increased level of investment into research in radio-frequency integrated circuits (RFICs). As wireless communication systems push for longer operation on smaller batteries, and as new applications that demand extremely low-power operation emerge, power consumption of RFICs has become a very important area of research [1].

CMOS technology used in digital circuits has become ubiquitous and extremely cost-effective, as a result of the economies of scale involved in the mass production of chips for everything from light switches to elevators. As these digital circuits require higher performance and as the technology has been pushed to a tiny physical dimension, the performance of the technology is such that high-frequency analog circuits can be realized in the same process. Although certain limitations exist, the cost-effectiveness of the technology when compared to other processes is extremely attractive.

This demand of implementing high-frequency analog circuits in digital CMOS technology is what has propelled our research into low-voltage, low-power RFICs in CMOS technology [2],[3],[4].

This work concentrates on the design of downconversion mixers, which are an integral part of the RF transceiever. The designs were developed with a focus on low-voltage and low-power operation. The 0.18μm CMOS process, available as part of the services offered by the Canadian Microelectronics Corporation (CMC), was used to develop these designs. A complete set of design tools were used to come up with the designs presented in this thesis.

1.2 THESIS ORGANIZATION

The thesis is divided into six chapters. It is divided in such a way as to present the reader unfamiliar with the work with some background prior to explaining the designs presented.

The motivation behind this work is presented in Chapter 1 (this chapter), along with a brief outline of how the thesis is organized.

Chapter 2 covers the receiver front-end and common architectures used for the receiver, along with the building blocks that form the receiver. It also details the parameters used to described the performance of a receiver.

The next chapter, Chapter 3, explains the theory behind mixer operation and the characteristics important to mixer performance. It also includes a review of important mixer topologies described in literature.

Chapter 4 is dedicated to the first design described in this thesis, the body-input mixer. In addition to a description of the circuit design and implementation, the results of simulation and measurements are also presented.

The second design, the folded mixer, is presented in Chapter 5. The circuit design and implementation is presented, followed by results of simulation on the circuit.

Finally, Chapter 6 concludes the thesis by presenting a summary of the work presented. Also in that chapter is a list of possible future work that could be done to further the work presented in this thesis.

The Appendix includes information on the measurements performed and should be useful for anyone attempting to recreate the measurement results presented in this thesis, or measuring any downconversion mixer for that matter.

Chapter 2

RECEIVER ARCHITECTURES

Any communication system can be represented by three elements: the modulator, the demodulator and the channel. Since there are many elements in the channel that degrade the signal considerably, there is a need for a front-end in the demodulator that is able to strengthen and clean up the signal received.

The main aim of any receiver front-end is to be able to get a usable signal from a received signal of low signal-to-noise ratio (SNR). There are a few different architectures that have been employed to achieve this, and each of them consist of several different building blocks. The most common one in use today is the heterodyne architecture.

2.1 HETERODYNE RECEIVER ARCHITECTURE

The representation of the heterodyne receiver architecture is shown in Figure 2.1. This architecture results in an intermediate frequency (IF) signal that must then be processed.

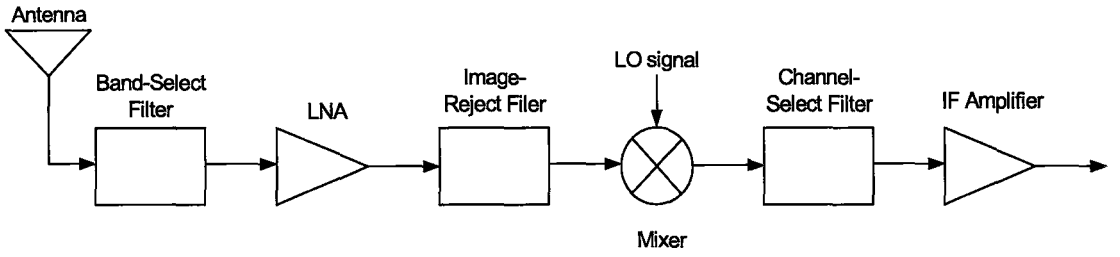

Figure 2.1: Block diagram of heterodyne architecture receiver front-end.

The signal is received at the antenna and fed into the band-select filter. This is a bandpass filter at the RF frequency, but its passband is relatively wide and allows the entire band of interest (which could be from tens to hundreds of MHz) to be passed. This is to eliminate out-of-band interferers that could have a negative effect on the sensitivity of the later parts of the receiver.

The output of the band-select filter is fed into the low-noise amplifier (LNA). As its name indicates, the LNA is designed to amplify the received signal, which has been considerably attenuated in the channel, without contributing very much noise. The LNA needs to be there in most circuits of this architecture because the later stages (particularly the mixer) tend to contribute a relatively high amount of noise.

The output of the LNA is fed into the image-reject filter, which ensures that the image signal is attenuated. This ensures that the image signal is not downconverted to the IF and does not corrupt the desired signal.

Following this, the signal is fed into the mixer which downconverts the signal of interest, using a variable local oscillator (LO) signal to achieve this. The LO signal is usually fed into the mixer by a voltage-controlled oscillator (VCO) or a phase-locked loop

(PLL). Neither of these are shown in the figure, but their performance is very important to ensure the signal of interest is isolated correctly and that there is no added noise as a result of the mixer's LO-IF feedthrough.

Finally, the downconverted signal is passed through another filter. This filter is a narrow band-pass filter that attempts to ensure that the adjacent channel signals are attenuated as much as possible and only the signal of interest is left unattenuated. The output of this filter is then fed into the demodulator or detector, where the low-frequency signal processing would be done.

This scheme is called single-IF, where the signal is downconverted to a frequency where it can be detected efficiently by the low-frequency signal processing circuitry. Although the image-reject filter attempts to attenuate the image signal, it is never completely successful in eliminating that signal. At the same time, the choice of the IF also changes how the image signal affects the desired signal - if the IF is high, then the image signal is far away from the desired signal, and vice-versa [5].

When the IF signal is high, it is difficult for the low-frequency signal processing circuitry to detect it. When the IF signal is low, the image-reject filter would require a high Q-factor to suppress it properly. The Q-factor is defined as the ratio of the center frequency of the filter to its 3dB bandwidth.

The heterodyne architecture, therefore, introduces a trade-off between sensitivity and selectivity. One solution to this problem is to use dual-IF receivers, where the RF signal is first downconverted to a high IF where the image reject filter requirements are relaxed, then to a lower IF where the signal can be detected easily.

Other solutions include the Hartley and Weaver Architectures [5], where the incoming signal is mixed with signals 90° out of phase and then added together, resulting in the IF signals adding but the image signals cancelling each other.

2.2 HOMODYNE RECEIVER ARCHITECTURE

Unlike heterodyne receivers, homodyne receivers do not have an IF. Instead, the LO signal is at the same frequency as the desired RF signal, and therefore the desired signal is converted to baseband. These receivers are, therefore, also known as direct downconversion receivers.

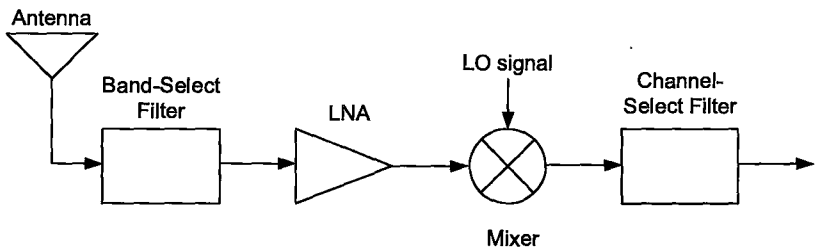

Figure 2.2: Block diagram of homodyne architecture receiver front-end.

As can be seen in Figure 2.2, the homodyne architecture has a few less blocks as compared to the heterodyne receivers. The image-reject filter is not needed, since the image signal is not an issue in these kinds of receivers. Further, the output of the channel-select filter is fed into baseband signal processing circuitry, where the detector's performance requirements are relaxed. Finally, since there is no high-frequency narrow band-pass filter required, the passive components used for the filter (which are sometimes realized off-chip

in heterodyne receivers) are no longer required, significantly reducing the area of the receiver circuit.

The homodyne receiver is not without disadvantages. One of the major issues of this kind of receiver is the fact that the LO leakage signal could mix with the LO signal and, since the downconverted product is at the baseband, would introduce DC offsets. These DC offsets, fed through the gain-inducing blocks of the receiver, could saturate the following components of the receiver and prevent amplification and detection of the desired signal.

Secondly, the LO signal will also leak into the preceding components of the receiver and find its way to the antenna. This can be a serious problem, since regulations in most countries limit the amount of in-band LO radiation that is inadvertantly transmitted.

Finally, the level of flicker noise of MOS transistors at the baseband is significant when compared to the low level of the amplified and downconverted signal at the baseband. The distortion can introduce significant flicker noise in the output signal.

2.3 RECEIVER PERFORMANCE PARAMETERS

There are several parameters that define the performance of a receiver. The most general ones are the sensitivity and dynamic range of the receiver. Further, both of these parameters are based on the gain, noise figure and linearity performance of the individual cascaded components of the receiver.

2.3.1 Sensitivity

The sensitivity of a receiver is defined as the minimum signal level that the system can detect with an acceptable SNR ratio. In [5], the sensitivity is defined to be measured by the minimum detectable signal (mds), which is expressed as:

$$P_{mds} = -174 + 10\log B + NF + SNR, \tag{2.1}$$

where B is the bandwidth of the receiver, NF is the overall noise figure of the receiver and SNR is the required value to achieve a BER of 10^{-3}.

2.3.2 Dynamic Range

The dynamic range is defined as the ratio of the maximum input level that the circuit can tolerate to the minimum input level at which the circuit provides a reasonable signal quality [5]. One method of defining the dynamic range is spurious-free dynamic range (SFDR).

The upper end of the SFDR is defined by the linearity of the receiver, measured by the 3rd-order input-referred intercept point (IIP3). The IIP3 defines to what level interferers at the 3rd harmonic frequency do not affect the desired signal. It is discussed in more detail in Chapter 3.

The lower end of the SFDR is defined by the sensitivity of the mixer. This is the point below which the noise is so high relative to the desired signal that the desired SNR cannot be achieved.

2.3.3 Parameters of Cascaded Stages

To determine the performance parameters of the receiver, the overall gain, noise figure and IIP3 of the receiver would be needed. To determine these values based on the values of the individual components would require having expressions for overall values of these three parameters based on the values for cascaded stages.

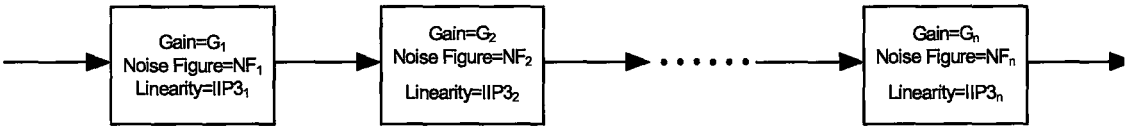

Figure 2.3: Cascaded stages.

Figure 2.3 shows a block diagram containing n such stages, each with its individual available gain G_i (in dB), noise figure NF_i (in dB) and linearity $IIP3_i$ (in dBm). To determine the values for the overall system, the following expressions can be used [6]:

$$G_{overall} = G_1 + G_2 + \ldots + G_n, \tag{2.2}$$

$$NF_{overall} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \ldots + \frac{NF_n - 1}{G_1 G_2 \ldots G_{n-1}}, \tag{2.3}$$

$$\frac{1}{IIP3_{overall}} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + \ldots + \frac{G_1 G_2 \ldots G_{n-1}}{IIP3_n}. \tag{2.4}$$

By determining the values of the individual components (filters, LNA, mixer, amplifiers, etc.) and calculating the overall values of these parameters, the overall performance of the receiver can be determined.

Similarly, given expected performance parameters of the overall system, the expected performance of each component in the receiver can be determined. This should be

done keeping in mind, for example, that the LNA need contribute more gain and less noise than the mixer.

The equations to determine the values of these measures for the mixer will be discussed in detail in the following chapter.

Chapter 3

MIXER THEORY & ARCHITECTURE

In this chapter, the basic operation of the mixer and how it performs its function, which is frequency translation, will be explained. The characteristics that are used to evaluate the performance of a mixer, as well as the factors that affect these characteristics, will also be introduced and explained. Finally, some mixer topologies will be presented, and their advantages and disadvantages will be explored.

As discussed in Chapter 2, the most common transceiver architecture used today is the heterodyne receiver, which is shown in Figure 3.1. This architecture has a low intermediate frequency (IF) to which the input radio frequency (RF) signal is downconverted.

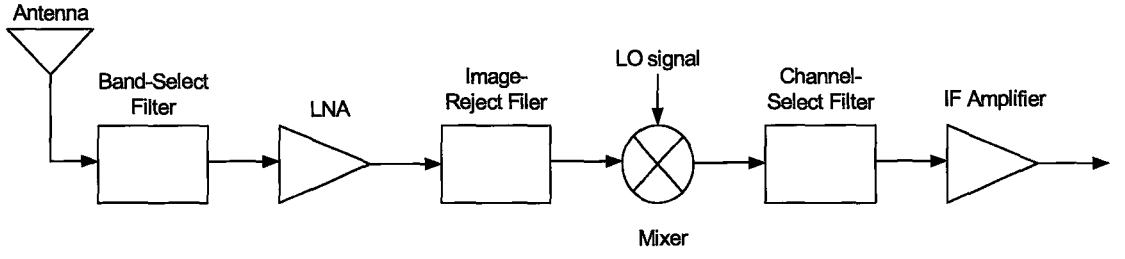

Figure 3.1: Heterodyne transceiver architecture.

One of the important functions in this and any transceiver is that of frequency translation, where the frequency of the signal is changed to a lower frequency to allow the

signal to be processed easily and more efficiently. The advantages of downconversion have been mentioned in Chapter 2, and include improved selectivity, since the filters are now fixed at the IF frequency, and improved stability from oscillation, since the gain stages are now distributed over several different frequency bands.

3.1 DOWNCONVERSION MIXER OPERATION

The basic operation of a mixer is to convert a signal from one frequency to another. Linear, time-invariant systems do not produce spectral components at the output that are not present at the input. As such, the mixer needs to behave in a non-linear or time-variant fashion.

Mixers are designed so that operation in this fashion results in the multiplication of two signals. If we were to consider two sinusoidal signals in the time domain, each represented by a magnitude and a frequency, multiplying them would give:

$$[A\cos(\omega_1 t)][B\cos(\omega_2 t)] = \frac{AB}{2}\{\cos[(\omega_1 - \omega_2)t] + \cos[(\omega_1 + \omega_2)t]\}. \qquad (3.1)$$

This multiplication results in two spectral components at the output, one at the difference frequency and one at the sum frequency. The magnitude of each of the output signals is the magnitude of the input signals multiplied together and divided by 2. In practice, the higher frequency term can be ignored, as a result of filtering at the output.

If A in the above equation is a varying signal and B is of constant amplitude, the varying signal, centered around ω_1, would be downconverted to be centered around $(\omega_1 - \omega_2)$. In essence, the amplitude modulation in the higher frequency (RF) signal would be transferred to the lower frequency (IF) signal. By changing ω_2, which corresponds to

the local oscillator (LO) frequency in a receiver, we are therefore able to tune the mixer to select the RF channel of interest.

In practice, the multiplication is realised by switches, and therefore the RF signal is multiplied by a square wave of the LO frequency, instead of a sinusoid. If we expanded this product using a Taylor series, we would see the fundamental sinusoid of the LO frequency and its harmonics. The expansion is covered in more detail in the derivation of the output of the circuit in Chapter 4.

In addition, there are other higher-order non-linearities that distort the output signal, and would result in cross-modulation at the output. These factors affect the linearity of the mixer and limit its usable range of operation.

3.2 MIXER CHARACTERISTICS

In the analysis of mixers, there are several characteristics that define the performance of a mixer. It is important to know and understand these characteristics as they are used to compare mixer designs to one another. Similarly, understanding these characteristics and how they are affected by differences in topology and design criteria allows for the design of better mixers and mixers that satisfy the requirements that are important for a specific application.

3.2.1 Conversion Gain

The gain of the mixer from the RF input to the IF output is defined as the conversion gain. The word conversion is used since the signal is converted from one frequency to

another. This gain, measured in in dB, contributes to the overall gain of the system and can be defined in terms of power or voltage as:

$$G(power) = 10\log\left(\frac{P_{out}}{P_{in}}\right) \tag{3.2}$$

$$G(voltage) = 20\log\left(\frac{V_{out}}{V_{in}}\right) \tag{3.3}$$

where P_{out} and V_{out} are the output power and voltage at the IF frequency, and P_{in} and V_{in} are the input power and voltage at the RF frequency.

If the input and output resistances are matched, these two measures of gain are exactly the same. However, in the case where they are not matched, the relationship between the two values is:

$$G(power) = G(voltage) + 10\log\left(\frac{R_{in}}{R_{out}}\right) \tag{3.4}$$

where R_{in} is the input resistance and R_{out} is the output resistance of the circuit. In our work, we have consistently used power conversion gain, as it is the one predominantly used in the literature and is more intuitive when doing simulation and measurements. Furthermore, the power conversion gain reflects losses resulting from mismatches in the input and output resistances and therefore presents a more realistic result.

This characteristic is referred to as conversion gain even though some mixer circuits may have a negative value, i.e. conversion loss. Nonetheless, for the sake of consistency, the metric used is always gain and losses are simply reported as negative values of gain.

In amplifying the signal of interest, the conversion gain also has the added effect of reducing the effect to the entire receiver of the noise contribution from the stages following the mixer. Conversely, a conversion loss would, in effect, cause an amplification of the noise contribution of any stages that follow the circuit.

3.2.2 Noise Figure

The noise that the mixer contributes to the system is measured by its noise figure. The definition of this characteristics is the amount the circuit degrades the signal-to-noise ratio (SNR). This is defined as:

$$NF = \frac{SNR_{input}}{SNR_{output}} = \frac{N_s + N_a}{N_s} \tag{3.5}$$

where SNR_{input} and SNR_{output} are the signal-to-noise ratios at the input and output of the mixer, N_s is the noise at the output caused by the source (and amplified by the mixer), and N_a is the noise at the output caused by the mixer.

In a mixer, the noise input and output is considered at two different frequencies, as a result of the frequency translating nature of the circuit. However, there is one subtlety that must be grasped to properly understand noise in mixers. As explained in Section 3.1 above, the frequency translation is performed by multiplication in the time domain. However, the frequencies at the output are the absolute values of the difference and sum frequencies. To simplify the explanation, we will rewrite (3.1) above and add an additional

term with a varying amplitude at a different frequency. Ignoring the upconverted part of the output signal, we get:

$$[A_1(t)\cos((\omega_{LO}+\omega_{IF})t)+A_2(t)\cos((\omega_{LO}-\omega_{IF})t)][B\cos(\omega_{LO}t)] = \frac{B}{2}[A_1(t)\cos(\omega_{IF})+A_2(t)\cos(\omega_{IF})] \quad (3.6)$$

where $A_1(t)$ and $A_2(t)$ are signals at frequencies at an offset of the IF frequency (ω_{IF}) above and below the LO frequency (ω_{LO}). As can be seen from this equation, when downconverting, two spectral components are downconverted to the IF frequency, the component at the frequency of interest and an image component. When considering the downconverted signal of interest, we can usually ignore the image component because there is usually no input signal present at that frequency. However, when considering noise, the question arises whether we should consider input noise at that image frequency, which may have been contributed by the stages before the mixer.

As such, there are two methods of defining and measuring the noise figure: single sideband (SSB) and double sideband (DSB). Sidebands refer to the components that are downconverted to the IF frequency. When the desired signal only exists at one frequency, we generally consider the SSB noise figure, and therefore the noise input considered is only the noise at the frequency of interest, and noise downconverted from the image frequency is considered as noise contributed by the circuit. In the rarer case that the signal of interest is also present at the image frequency, we would consider the DSB noise figure.

The DSB noise figure will generally be lower than the SSB noise figure. This is because in the former case, the noise power considered as being from the input is higher

than that of the latter case (since it is noise at two different frequency points), while the signal power is the same. As such, the SNR_{input} is lower than that for the SSB case. In the case that the noise powers for both sidebands of the input are equal, the DSB noise figure would be 3dB lower than the SSB noise figure.

In some cases, published results do not indicate which noise figure is being used. Further, sometimes DSB noise figure is used even when the SSB noise figure would be a more appropriate measure, since the DSB case generally results in a lower value for a given circuit. In the case of a non-zero-IF downconversion mixer, the SSB noise figure is the most appropriate characteristic to use.

There are four main sources of noise in mixers. First, there is the the noise coming in from the RF port. Having a good LNA stage before the mixer and good RF-IF isolation would help reduce the effect of this noise. The second source is noise coming in from the LO port. It is important to have a low-noise voltage-controlled oscillator (VCO) and (if applicable) frequency doubler. However, it is even more important to have good LO-IF isolation in the mixer to prevent small-signal noise from entering the circuit through this port. Third, there is the thermal noise as a result of the intrinsic device noise and the load of the circuit. This can be minimized by appropriately designing the transistors in the circuit and choosing the device values appropriately. Finally, there is the noise due to imperfect switching in the LO stage. This noise can be reduced by have a large amplitude signal on the LO, having appropriately sized transistors in the switching stage, and having a low DC current through those transistors.

The noise figure in mixers is generally higher than that for amplifiers, because noise components from frequencies other than RF can downconvert to the IF (such as differences of the frequencies of the various harmonics of the many signals involved). The typical noise figure value of a mixer is anywhere from 10 to 20dB. This relatively high noise figure is what necessitates a low-noise amplifier (LNA) stage before the mixer. The LNA amplifies the signal considerably while contributing very little noise, so that the SNR of the signal going into the mixer is already high.

3.2.3 Gain Compression

The conversion gain and noise figure together give you an idea of the amplitude and SNR of the output signal for a fixed input signal. Further, as the amplitude of the input signal increases, so do both the amplitude and SNR of the output signal. However, this relationship only holds for a certain range of signal levels. Above a certain level, the circuit deviates from this ideal behaviour due to devices in the circuit leaving their intended mode of operation.

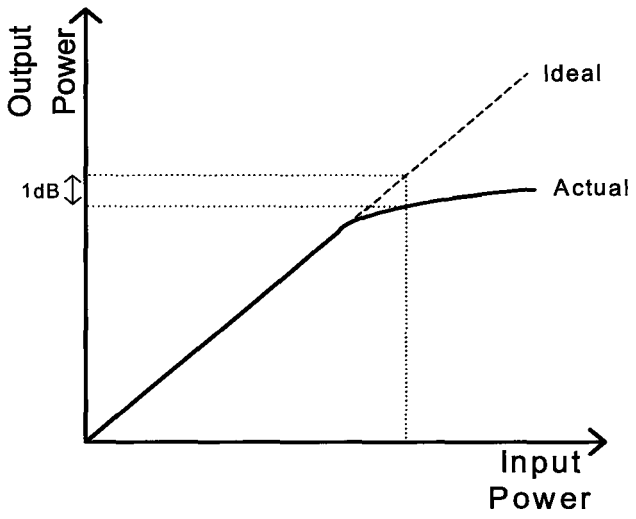

Figure 3.2: Ideal and actual input vs. output power curves, 1dB compression point is shown.

As the peaks of the input signal pass this level, known as the compression point, the amplitude modulation of the RF signal would no longer be properly transferred to the IF signal. As such, the signal would be disorted and clipping would occur.

To identify this level, we define the compression point as the point at which the curve departs from the ideal by a specific amount. The most commonly used amount for this deviation is 1dB (although 3dB is sometimes used), and therefore the point that most commonly represents the power level above which the circuit's gain is no longer constant is the 1dB compression point (P_{-1dB}).

3.2.4 Linearity

As mentioned in Section 3.1, there are higher-order non-linearities in mixer circuits that result in intermodulation of the downconverted signals. One measure of how

these non-linearities affect the performance of the circuit is the 3rd-order intermodulation distortion level (IM3), which is the ratio of the fundamental power to the intermodulation distortion power for a given input power. Another measure, more suited to mixer circuits because of the varying input power, is the 3rd-order input- or output-referred intercept point (IIP3 or OIP3, respectively). This is the point at which the ideal input vs. output curves of the fundamental and the 3rd-order intermodulation distortion would intersect, referred to either the input or output power, respectively. Both of these measures are illustrated in Figure 3.3 and are always measured in dBm.

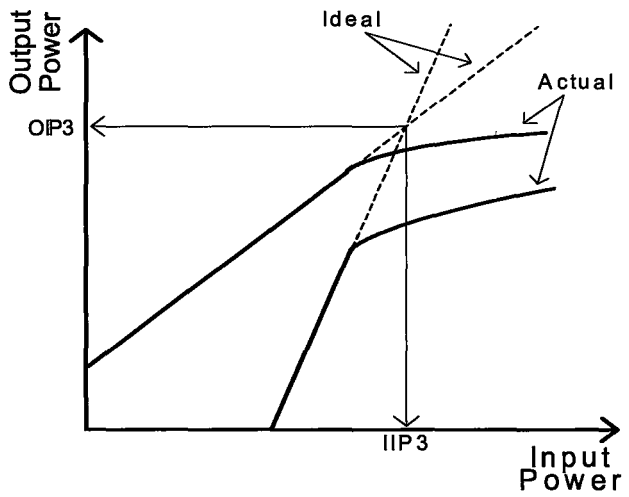

Figure 3.3: Ideal and actual input vs. output curves for fundamental product and intermodulation distortion product.

To realize how these non-linearities affects the output signal, we represent the input stage of a mixer as a non-linear circuit:

$$S_o = A_1 S_i + A_2 S_i^2 + A_3 S_i^3 + \ldots \tag{3.7}$$

where the coeffecients A_n are constants.

Using (3.7), we can perform an analysis of the intermodulation products. Intermodulation occurs when more than one harmonic wave is applied to the input of a circuit. In zero-IF (direct downconversion) systems, major emphasis is on the second-order intermodulation product, since that distortion appears close to the baseband. However, in our case of low-IF communication systems, the third-order intermodulation product is of primary interest [5], since it appears close to the RF signal and is therefore also downconverted to the IF band.

If we were to consider the input to this non-linear system as the sum of two signals. The first is our signal of interest and is centered around ω_1, while the second is an unwanted signal (perhaps an interferer in an adjacent channel), centered around ω_2, which is close to ω_1. Therefore, the input is:

$$S_i = S_1\cos(\omega_1 t) + S_2\cos(\omega_2 t) \tag{3.8}$$

where the coefficients S_n are the amplitudes of the respective signals.

If we use the input signal of (3.8) in the non-linear system described by (3.7), our output signal would include the cubic term:

$$A_3 S_i^3 = A_3[S_1\cos(\omega_1 t) + S_2\cos(\omega_2 t)]^3 \tag{3.9}$$
$$= \ldots + \frac{3}{4}A_3 S_1^2 S_2\cos[(2\omega_1 - \omega_2)t] + \frac{3}{4}A_3 S_1 S_2^2\cos[(2\omega_2 - \omega_1)t] + \ldots$$

For the sake of clarity, we have only shown the intermodulation products in the expansion above, which appear at $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$. The cubic term would also include spectral components outside the band around the fundamental and these are not as important.

As can be seen from the equation, the non-linear input stage would result in components above and below the higher and lower fundamental components, respectively. The difference between the frequencies of the intermodulation product and it's nearest funadamental would be the same as the difference between the frequencies of the two fundamentals.

The IM3 is defined as the ratio of the amplitude of the third-order intermodulation products to the amplitude of the fundamental signal. If we set the input signal amplitudes of the wanted and unwanted signal to be the same (i.e. S_1=S_2 in (3.8)), then IM3 can be written as:

$$IM3 = \frac{\frac{3}{4}A_3 S_1^3}{A_1 S_1} = \frac{3}{4}\frac{A_3}{A_1} S_1^2 \tag{3.10}$$

The IIP3 is the point at which the fundamental and intermodulation distortion power levels are equal, i.e. when the ratio of the two powers is 1. Therefore, we set IM3 equal to 1 and solve for the input signal:

$$IIP3 = \sqrt{\frac{4A_1}{3A_3}} \tag{3.11}$$

To get the OIP3, we would simply multiply the IIP3 by the gain of the fundamental signal, A_1.

This method of measuring the IIP3, using two input signals, is known as the two-tone test. As mentioned, the derivation above has been done considering the input stage of the mixer as a non-linear circuit. Therefore, in a mixer, both the input signals and the intermodulation distortion products would be downconverted to the IF band. Intermodulation

distortion products of signals in channels adjacent to the signal of interest could very easily fall at the frequency of the signal of interest, and therefore downconvert to the IF frequency of the fundamental signal. This added signal power at the downconverted fundamental frequency would cause the amplitude of that component to no longer correspond to the amplitude of the input signal, thereby corrupting the signal. The higher the linearity, the higher the input power level before this would occur.

3.2.5 Port-to-Port Isolation

Another important characteristic is the isolation of the signal between the three ports of the mixer. The LO-RF isolation is important to prevent the LO signal from leaking through the LNA and eventually to the antenna. The RF-LO isolation is important to prevent strong interferers in the RF path from interacting with the LO, causing other mixing components. The LO-IF and RF-IF isolations are important to ensure the following stages do not get large out-of-band interferers, although this problem is less important, since the mixer has a natural band-limited characteristic and mixers are usually followed by filter stages.

3.3 MIXER ARCHITECTURES

Before examining the different mixer topologies, it is important to understand balanced architectures in mixers and the reasons for using them. A mixer achieves its objective of frequency translation by multiplying the input signal by a square wave in the time domain. However, a mixer can be single-balance or double balanced, depending on whether the LO signal alone or both the RF and LO signals are taken differentially. We will first

discuss single- and double-balanced mixers first only by showing their equivalent representations. Circuit diagrams for topologies (primarily those that are of single-balanced nature) will be discussed in the next section.

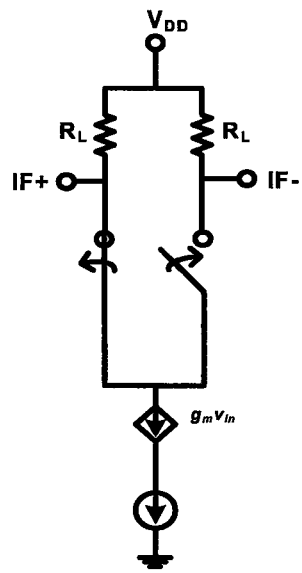

Figure 3.4: Equivalent representation of a single-balanced mixer.

Figure 3.4 shows the equivalent representation of a single-balanced mixer. In such a mixer, the RF signal is fed single-ended into the circuit and the LO signal is fed in differentially. The LO switches turn on alternatingly, as a function of the LO signal. The output is taken differentially, and as such, in any one phase of the LO signal, one side contains the downconverted and amplified version of the RF signal and other side is small-signal ground. The output signal is therefore equivalent to a downconverted and amplified version of the RF signal being multiplied by a square wave which varies in amplitude from +1 to -1.

The advantage of designing a mixer in this way is avoiding the use of a complicated and potentially lossy balun for the RF signal. At the same time, VCOs are usually de-

signed with a differential output (owing to their differential topology), so therefore a balun would not be needed for the LO input signal. However, in a single-balanced architecture, the LO signal transconducted through the LO switches, as well as any noise, is only present on one side of the differential output, and is therefore transferred to the output.

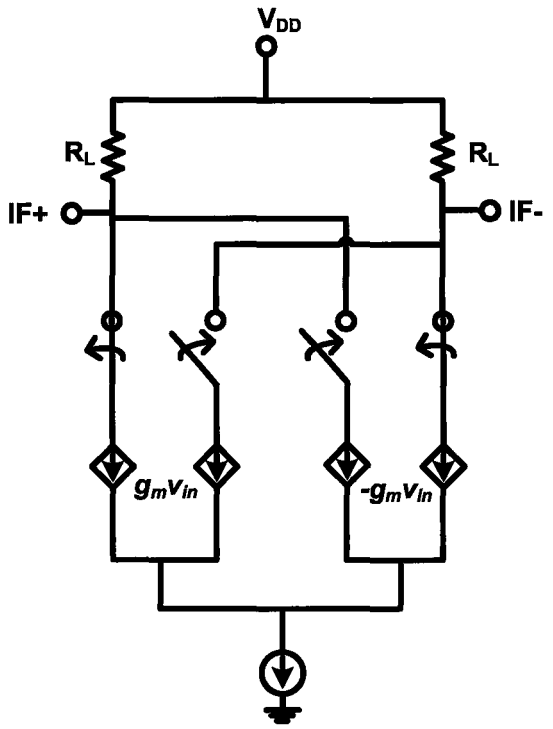

Figure 3.5: Equivalent representation of a double-balanced mixer.

Figure 3.5, on the other hand, shows a double-balanced mixer. In this architecture, both the RF and LO signals are fed into the circuit differentially. The output is also taken differentially. However, in this case, each side of the output contains a downconverted and amplified version of the RF signal which is out of phase on the two different ends of the output, and, similarly, contains any common-mode noise and LO feedthrough, which is in-

phase on the two different ends. As a result, any common-mode noise and most LO feedthrough is eliminated. In practice, a small amount of this undesirable output remains, as a result of the mismatch between the differential devices and their biases. A second advantage is that the gain is twice as high, since the RF signal is transferred to both ends of the output.

However, more devices in parallel translates to a higher power consumption. In addition, since there are twice as many transconductors, the noise contribution of the circuit will increase. Finally, the baluns would introduce added complexity, noise and potential mismatch.

Nonetheless, recent research in downconversion mixers has concentrated mainly on double-balanced architectures. The ideal solution would be a fully differential receiver stage, since it would mean a differential signal would be the norm throughout the circuit and most common-mode noise would be eliminated.

Now that we have explained the balanced nature of mixer designs, we need to explore the different architectures. The way a mixer peforms its function of frequency translation is by multiplying two time-varying signals. There are a few different methods by which this multiplication function is realized, and are separated into two different classes: passive and active mixers. The difference between the two is in how the RF signal is coupled into the circuit.

3.3.1 Passive Mixers

The very first mixers designed were of the passive kind, made using vacuum tubes and then diodes [7]. They are still used in their CMOS version, although they are not as common as active mixers. Figure 3.6 shows a typical passive mixer in CMOS.

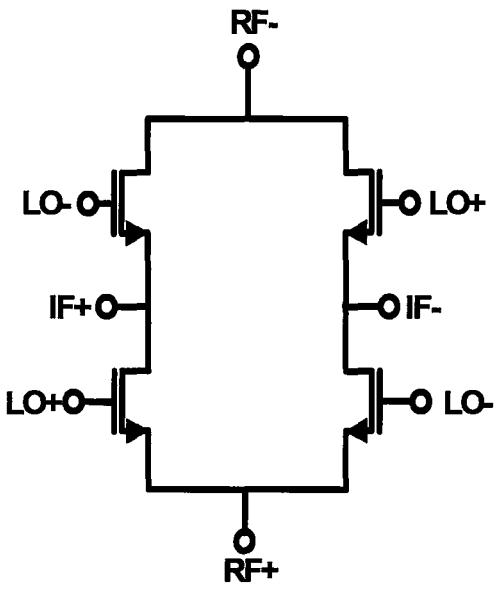

Figure 3.6: Passive mixer topology.

The LO transistors switch alternatingly, thereby continuously changing the signal at the output. This is equivalent to multiplying V_{RF} by a a square wave of the same frequency as V_{LO}. As explained earlier, the output would therefore include a term that is a down-converted version of the RF input signal.

The passive mixer has the advantage of having very good linearity performance, since there is no transconductor to limit it, as long as the switching transistors are in strong

inversion so that the RF signal does not affect their on-resistance. In addition, it draws no power from the DC supply.

However, at the same time, one of the disadvantages is that it has a low conversion gain. Theoretically, the square wave multiplying the RF signal should result in a conversion gain of $\frac{2}{\pi}$, which is approximately -2dB. This low gain results in the noise figure being impacted as well, since the noise contribution of the stages following the mixer is effectively amplified when referred to the input of the mixer.

Further, in the case of a low supply voltage, which is the primary interest of this thesis, the on-resistance of the switches can no longer be kept very high, since the gate overdrive voltage is limited. This would result in distortion in the signal, and linearity would be degraded [5].

3.3.2 Active Mixers

The more commonly-used kind of mixers are those using transistors as transconductors as well as switches. In an active mixer, the RF signal is transconducted from a small-signal voltage to a small-signal current. The transistor that does this conversion has a certain gain associated with it. Further, after the switching stage, the current is changed back into a voltage by measuring the voltage across a load. The resistance of the load also contributes to the net gain of the circuit. Therefore, unlike the passive mixer, it is possible to have significant gain from an active mixer.

Further, active mixers generally exhibit lower linearity than their passive counterparts as a result of the non-linearities in the input stage of the mixer, the transconductors.

This device, along with the load, also contributes more noise to the circuit that is usually seen in passive mixers.

The multiplication function in active mixers is realized using large-signal switching. Designs using this method are also collectively called switching mixers.

3.4 ACTIVE MIXER TOPOLOGIES

Among the oldest and most common mixer topologies is the Gilbert cell mixer, proposed in 1968 by Barrie Gilbert using BJTs [8]. Gilbert's design is the basis of most mixers in commercial applications today, both in BJTs and CMOS. Further, many mixer topologies that have been proposed, for normal and low-power applications, borrow from his topology [9].

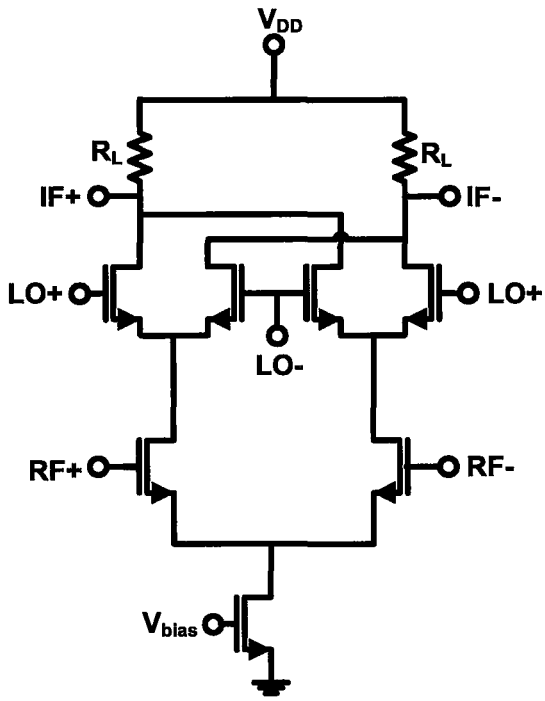

Figure 3.7: Gilbert cell mixer topology.

In this section, we will cover some of the mixer topologies that have been used in the literature in recent years. The topologies examined will consist mostly of those designed to achieve low-power operation.

3.4.1 Low-Voltage, Low-Power Gilbert Cell Mixers

The Gilbert cell mixer can be designed to achieve low-power and low-voltage operation. However, there is a lower limit on the minimum supply voltage requirement, and very low-power operation causes significant tradeoffs in the other important mixer parameters, such as conversion gain and linearity.

One of the first publications to present a low-voltage design for a Gilbert cell mixer in CMOS was [10], although there have been several other designs presented since, including [11].

The topology of the Gilbert cell mixer has already been shown in Figure 3.1. The authors in [10] achieved low-voltage operation by appropriating sizing of the transistors and appropriate selection of the biases. They have been able to maintain good performance, but the current consumption in their mixer core (between 2 and 6mA) is an order of magnitude higher than some of the lowest-power mixer designs available today. However, this is in large part due to the older fabrication technology used in that design. The second Gilbert cell mixer design mentioned [11] reported a similar level of power consumption, although the voltage supply requirement is lower. It should be mentioned that the latter design's power consumption level includes the power consumed by the buffer circuitry,

whereas the former design and many other designs published (including the designs presented in this work) consider power consumption for the mixer core alone.

3.4.2 Mixer Without Current Source

In the Gilbert cell mixer topology, the tail current source is present to provide a stable biasing point for the RF transconductance transistors. For low-voltage operation, the minimum voltage drop of the current source, which is the saturation voltage of the transistor, is no longer negligible.

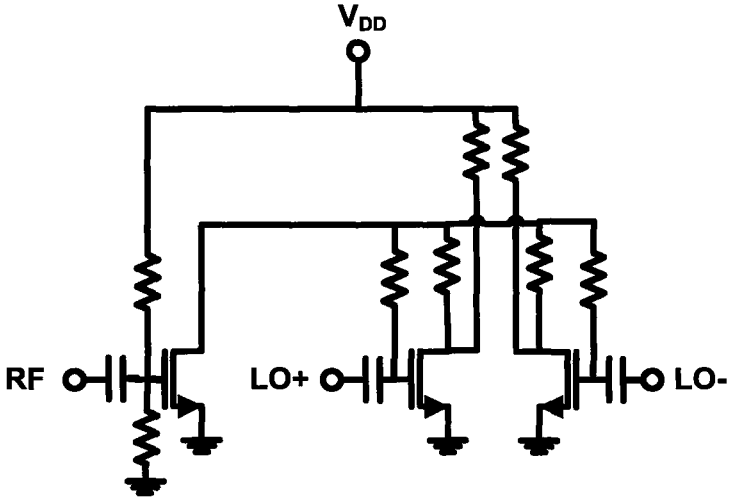

Figure 3.8: Mixer topology eliminating tail current source.

The design shown in Figure 3.8 [12] uses a topology that eliminates the need for the tail current source. Instead, appropriately sized resistors that are placed between the transistor's gate and the supply, and the transistor's gate and ground, provide the stable bias point needed. The circuit shown is a single-balanced version of the circuit described in [12].

The primary advantage is lowering the minimum supply voltage, which is achieved by eliminating one of the stacked stages in the circuit. There is also a reduced complexity in the design, since the biasing of the RF and LO inputs is done entirely within the circuit.

However, the added resistors result in added noise to the circuit. In addition, mismatches in the resistors (which are known to be up to 30% in some CMOS processes) could cause huge differences in the biasing of the circuit, resulting in degraded linearity, reduced common-mode noise immunity and reduced LO-IF isolation.

3.4.3 Current Injection/Bleeding

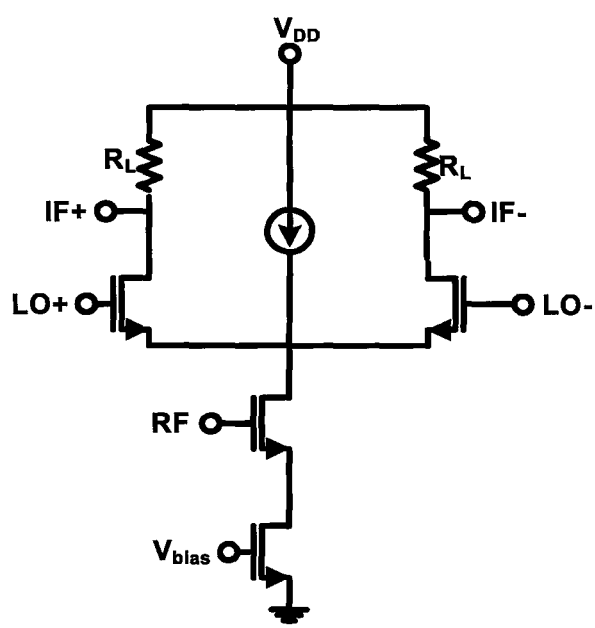

Figure 3.9: Mixer topology using current injection into transconductance stage.

Increasing the current through the current source, and therefore in the transconductance stage, would improve the gain and linearity of the transconductors. At the same time, however, this increased current would have to flow through the switching transistors, degrading their switching time, and through the load, increasing the voltage drop across the load. This increased voltage drop would in turn reduce the voltage headroom of the transconductance stage and degrade the linearity.

To get the best of both situations, the increased linearity of the transconductance stages as a result of increased current, and good switching and low voltage drop across the load as a result of lower current, we can use an idea called current injection or current bleeding [13].

Figure 3.9 shows a current source that adds to the DC current flowing from the switching stage to the transconductance stage, thereby "injecting" current into the transconductance stage. We therefore have a higher current through the transconductance stage to improve gain and linearity, and lower current through the switching stage and the load. In addition, we can afford to have a larger load to increase the gain, since the voltage drop across this load would not be as large.

However, the extra current that is drawn from the supply but essentially bypasses the load and switching stage, is wasted since it adds to the power consumption. In addition, the added current source introduces extra noise into the circuit.

Although the idea of current injection is not new and it does not directly result in low-voltage and low-power operation, it is presented here because the idea is used in many different forms in low-voltage, low-power mixers.

3.4.4 Transformer Coupling of Stacked Stages

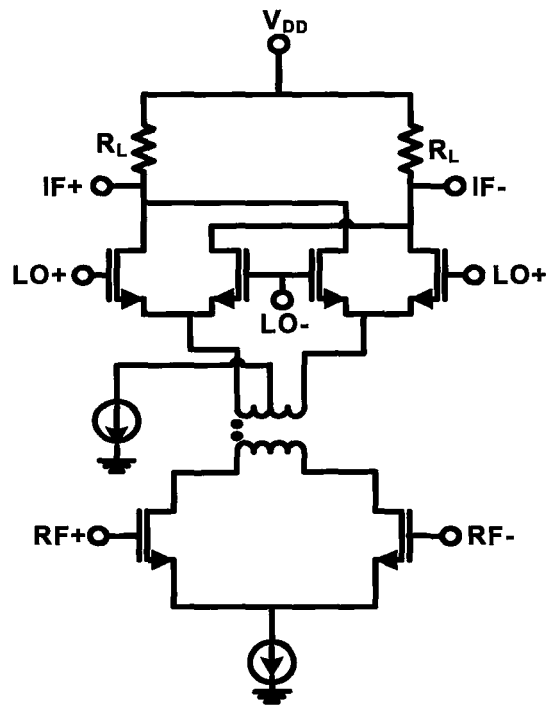

Figure 3.10: Mixer topology using transformer coupling of Gilbert cell transconductance and switching stages.

One proposed method [14] of lowering the relatively high minimum supply voltage caused by stacking stages in the Gilbert cell mixer is to separate the stages with respect to DC and then use a transformer to couple the signal between these two parts.

Figure 3.10 shows the architecture of the circuit designed using this idea. In this circuit, the RF signal is fed into the transconductance stage, whose DC current is controlled by the current source. The differential RF signal is then coupled into the switching stage using a monolithic integrated transformer. The switching stage current is controlled by a separate current source. Using the same idea as the current injection method, this could al-

low for lower current through the switching stage and the load, which is good for faster switching and allows for a larger load to increase gain.

This circuit is therefore able to achieve a lower minimum supply voltage. However, the cost is a significant amount of added complexity and chip area as a result of the monolithic transformers, as well as a degradation in linearity caused by the signal coupling through the transformer. Further, there would be an increase in noise as a result of the added current source.

3.4.5 Folded-Switching Mixer with Current-Reuse

Another method of current injection, also known as current-reuse, is to fold the stages of the mixer around the DC supply. Similar to the transformer coupling method, the added current is not wasted, but there is less added complexity involved, compared to the transformer coupling method. There have been several topologies that make use of some kind of folded architecture, and one of these is presented in [15] and shown in Figure 3.11.

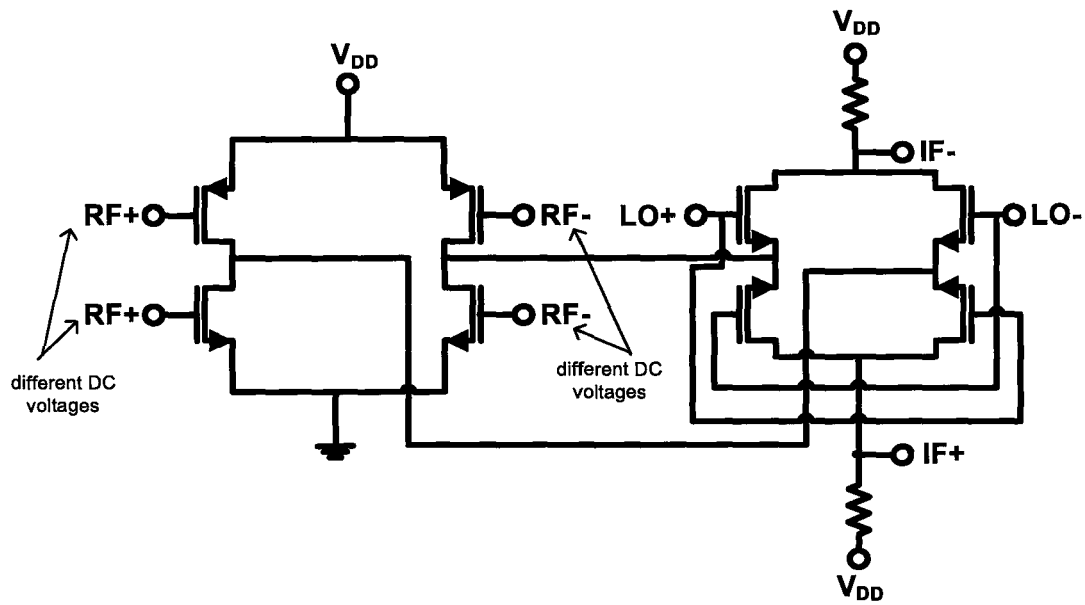

Figure 3.11: Folded-switching mixer.

In this design, the transconductance stages consists of a double-balanced set of complementary nMOS and pMOS transistors. The complementary transistors on each side of the differential structure have different DC biases, but share the same small-signal input.

This small-signal voltage is transconducted onto the DC current held steady by the biases on the respective complementary transistors. The small-signal current is then bled into the switching stage (which is why the design is said to employ current-reuse). Finally, the output is taken across the loads.

Just like the basic current bleeding idea and the transformer coupling topology, this topology is able to achieve higher linearity and gain through the transconductors, and good switching and low voltage drop. However, unlike those two designs, it eliminates the extra transistors acting as current sources, thereby reducing the noise contribution of the

circuit. In addition, the folded nature of the topology allows for low-voltage operation of the circuit. Appropriate design would, therefore, result in low-voltage and low-power operation.

However, the complementary transistors on each side of the differential structure, which are necessary since the current source has been eliminated, necessitates the use of coupling capacitors between the differently-biased input signals. These capacitors, besides adding to the chip area of the design, would also affect the linearity performance of the transconductors.

3.4.6 Subthreshold Mixers

An idea that has been used more and more in recent low-power RF designs is operating the transistor in the subthreshold region. By operating the transistor in this region, it is possible to achieve comparable gain, while reducing the current through and voltage across the transconductor considerably. The design in [16] presents a Gilbert cell mixer designed with all the transistors operating in the subthreshold region. The topology of the design is, therefore, exactly the same as Figure 3.7.

The design presented is able to achieve extremely low-power operation while realizing a good conversion gain. However, since the transconductors are operating almost at the extreme lower limit of their usable operating range, the dynamic range of the transconductors is limited, which impacts its linearity performance.

Furthermore, the design of such a circuit is difficult due to the inaccuracies of the small-signal models involed. This is especially true for the noise models for subthreshold

operation because the noise models in Cadence are developed for devices operating in strong inversion. Since transistors in subthreshold generate more noise, the noise performance is expected to be poor, but this information was not provided in [16]. Finally, it is also expected that the circuit would be extremely sensitive to minor changes in the voltage biases, since a slight change in the biasing could essentially turn the transistor completely off.

3.4.7 Comparison of Mixer Topologies

To achieve low-power operation, it is necessary to reduce the voltage supply and the current drawn. To minimize the voltage supply, it is necessary to reduce the stacking nature of the Gilbert cell, either by eliminating certain stages or by folding them around the DC supply. To reduce the current drawn by the circuit and maintain a level of performance, it is necessary to design the circuit so that the appropriate parts of the circuit are provided with the appropriate level of current to maximize performance. This is achieved by current bleeding, but is achieved more efficiently in the different folded architectures.

A comparison of the different performance characteristics of the topologies presented are given in Table 3.1.

Table 3.1: Comparison of mixer topologies.

	Gain	Linearity	Noise Figure	Supply Voltage	Power Consumption	Complexity
Passive	low	high	low	low	low	low
Gilbert cell	high	medium	medium	high	high	low
No current source	high	high	high	low	medium	medium
Current injection	high	high	high	low	medium	low
Transformer coupling	high	high	high	low	low	high
Folded-switching	high	medium	medium	low	low	medium
Subthreshold	high	low	high	low	low	low

The best solutions for low-voltage, low-power operation are the transformer coupling, folded-switching and subthreshold mixer topologies. As discussed in the descriptions for the different topologies, each has its advantages and limitations that would need to be weighed before designing a mixer for a specific application.

Chapter 4

BODY-INPUT MIXER

As mentioned earlier, the focus of this thesis is in low-power radio-frequency integrated circuits (RFICs), more specifically low-power downconversion mixers. In Chapter 3, we discussed the different mixer topologies that have been proposed to achieve low-power operation. Nonetheless, the primary topology used today is still the Gilbert cell.

A major limitation of Gilbert cell mixers is their stacked topology. Since the tail current, radio-frequency (RF) input stage, local oscillator (LO) input stage and load need to be stacked on top of one another, the minimum voltage supply requirement of the circuit is increased. Many methods have been proposed to overcome this limitation. The one used in the design of the circuit discussed in this chapter is to collapse the RF and LO stages into one by using the MOS transistor as a true four-terminal device.

Applying a voltage to the body of the MOSFET changes the threshold voltage of the transistor. This idea, called body biasing, has been used in several CMOS circuits, both digital and analog, to either lower the power consumption [17], increase the speed of the transistor [18], compensate for process variations [19], or control the transistor [20], and it's effects have studied in many publications [21],[22],[23]. In some cases, active schemes

have been employed that change the body voltage, and therefore change the threshold voltage, based on whether the circuit is in "active" or "sleep" mode [24],[25].

When the voltage of the body is higher than that of the source, the transistor is said to be forward body biased ($V_{BS}>0$ for a nMOS transistor). In this case, the threshold voltage of the transistor is decreased. Conversely, when the voltage of the body is lower than that of the source, it is said to be reverse body biased ($V_{BS}<0$ for a nMOS transistor), in which case the threshold voltage of the transistor is increased.

Therefore, applying a changing voltage to the body would modulate the threshold voltage. If the input voltage swing was large enough, this change in threshold voltage would be large enough to turn the transistor on and off. If the LO signal of the mixer was applied to the body of the RF transistors, it would have the effect of turning the RF transistors on and off as a function of the LO signal.

This operation would be similar to the switching operation performed in the Gilbert Cell mixer. However, unlike the Gilbert cell mixer, this operation would be done in a single stacked stage, thereby reducing the minimum voltage supply requirement.

In this design, to allow the nMOS transistors of the mixer to be accessible, it was necessary to use the deep n-well option available in the 0.18μm CMOS process that we used and many other CMOS processes (including IBM and Intel's recent CMOS processes). The deep n-well surrounded each set of nMOS transistors and therefore isolated the p+ bodies of those transistors from the p+ substrate. This allowed the voltage of the transistor's body to be different than the substrate, but this option has also been used to provide greater

isolation from substrate-coupled noise [26]. A cross-section of a transistor in a deep n-well is shown in Figure 4.1.

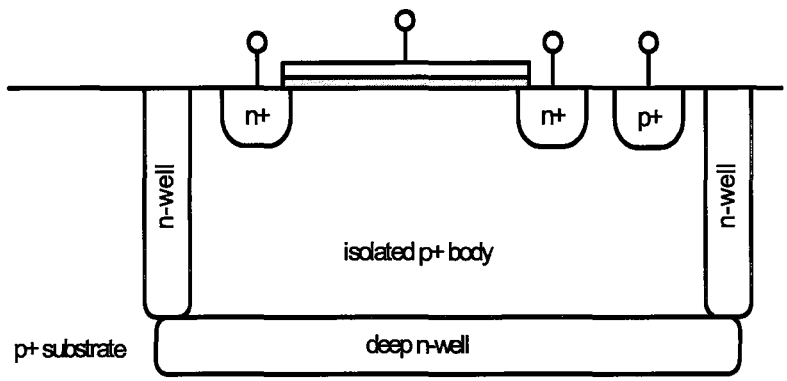

Figure 4.1: Cross-section of a nMOS transistor in a deep n-well.

4.1 CIRCUIT ANALYSIS

The circuit of the body-input mixer is shown in Figure 4.2.

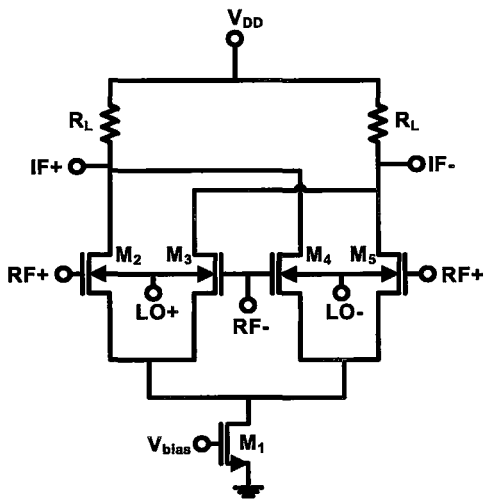

Figure 4.2: Circuit diagram of double-balanced body-input mixer.

As discussed above, the RF signal is applied differentially to the gates, while the LO signal is applied differentially to the body (in anti-phase with respect to the RF signal). The circuit is of a double-balanced nature, to improve noise figure performance and minimize the LO-IF feedthrough. This is accomplished because common-mode noise and common-mode feedthrough is cancelled at the output since the output is taken differentially.

The equivalent circuit representation of a double-balanced body-input mixer is shown in Figure 4.3. The figure is shown for the case when the LO signal is high.

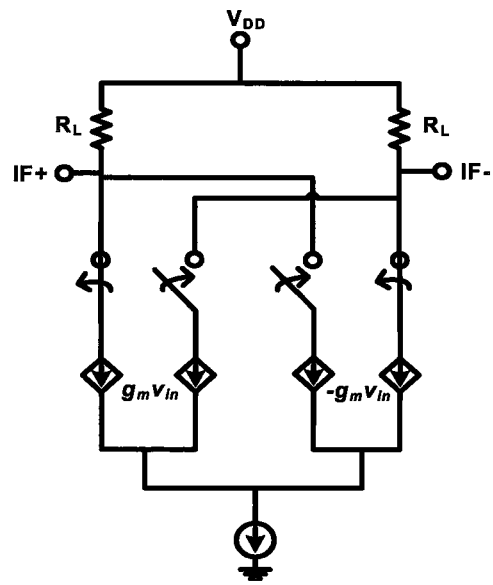

Figure 4.3: Equivalent circuit representation of double-balanced body-input mixer.

The combined RF/LO stage can be represented by two separate parts. The RF or transconductance part of this stage can be represented by dependent current sources which multiply the input signal v_{in} by the gain of the transistors g_m. At the same time, the LO or switching part of the stage can be represented by switches that connect and disconnect the

dependent current sources from the loads, depending on whether the LO signal is in its positive or negative phase. The output signal v_{out} at the intermediate-frequency (IF) is taken differentially as shown.

4.1.1 Gain

When the LO signal is in its positive phase, the switches dependent on LO+ are connected and $v_{out} = g_m v_{in} R_L - (-g_m) v_{in} R_L = 2 g_m v_{in} R_L$. Conversely, when the LO signal is in its negative phase, $v_{out} = (-g_m) v_{in} R_L - g_m v_{in} R_L = -2 g_m v_{in} R_L$. This operation is equivalent to multiplying the current from the transconductance part by a square wave with the same frequency as the LO signal.

To analyze how this switching results in the expected mixing operation, the Fourier series expansion of the LO switching needs to be taken. The Fourier series expansion of any periodic signal $x(t)$ is given by:

$$x(t) = \sum_{k=-\infty}^{\infty} a_k e^{jkt}, \tag{4.1}$$

where $a_k = \frac{1}{T}\int_T x(t) e^{-jkt} dt$ are the Fourier series coefficients and T is the period of the signal $x(t)$.

If we assume the switches operate in an ideal manner, we can represent the multiplier as $LO(t)$, a square wave of the LO frequency. The Fourier series expansion of this square wave is:

$$LO(t) = \frac{4}{\pi} \sum_{k=1}^{\infty} \frac{1}{k} \sin\left(\frac{k\pi}{2}\right) \cos(k\omega_{LO} t). \tag{4.2}$$

The output of the mixer would then be:

$$v_{out}(t) = 2g_m v_{in}(t) R_L LO(t) \tag{4.3}$$

$$= 2g_m v_{in}(t) R_L \left(\frac{4}{\pi} \sum_{k=1}^{\infty} \frac{1}{k} \sin\left(\frac{k\pi}{2}\right) \cos(k\omega_{LO} t) \right)$$

$$= \frac{8}{\pi} g_m v_{in}(t) R_L \left(\cos(\omega_{LO} t) - \frac{1}{3}\cos(3\omega_{LO} t) + \frac{1}{5}\cos(5\omega_{LO} t) + \ldots \right)$$

Ignoring the higher frequency terms, we get:

$$v_{out}(t) = \frac{8}{\pi} g_m v_{in}(t) R_L \cos(\omega_{LO} t) . \tag{4.4}$$

If we define $v_{in}(t)$ as a sinusoidal signal with amplitude V_{in} and angular frequency ω_{RF}, then the output would be:

$$v_{out}(t) = \frac{8}{\pi} g_m V_{in} \cos(\omega_{RF} t) R_L \cos(\omega_{LO} t) \tag{4.5}$$

$$= \frac{4}{\pi} g_m V_{in} R_L \left[\cos((\omega_{RF} - \omega_{LO})t) + \cos((\omega_{RF} + \omega_{LO})t) \right]$$

Again, ignoring the higher frequency term, we get the desired output of the mixer as:

$$v_{out}(t) = \frac{4}{\pi} g_m V_{in} R_L \cos\{(\omega_{RF} - \omega_{LO})t\} . \tag{4.6}$$

As can be seen from this equation, the output consists of a signal with a frequency that is the difference between the RF and LO frequencies. Therefore, the RF signal has been downconverted to the IF frequency.

From (4.6), we can derive the gain of the circuit from the RF input to the IF output, which is defined by the gain of the input transconductors (g_m) and and the load resistance (R_L):

$$G = \frac{V_{out}}{V_{in}} = g_m R_L \frac{4}{\pi} \tag{4.7}$$

In an ideal system, these two variables, g_m and R_L, are the ones that would be tweaked to affect the gain. In reality, imperfect switching also has an effect on the gain.

Increasing the transconducting transistors' g_m would increase the gain, but would require increased current, which would result in increased power consumption. Increasing R_L would also boost the gain, but would increase the noise as a result of the added resistor noise, and result in a higher minimum supply voltage, as a result of the voltage drop across the resistor.

4.1.2 Linearity

To analyse the linearity of the body-input mixer, we must use Volterra series to relate the input and output signals of the circuit. Since the topology of the body-input mixer is similar to the Gilbert cell, the linearity analyses of the transconductance stages of the two types of mixers are identical. The linearity analysis has been done for CMOS Gilbert cell mixers in [27], and has been followed for the linearity analysis of this circuit.

For any two-port system, it is possible to relate the input and output variables using a Volterra series expansion. If V is the input (composed of a small-signal input v_{sig} at a DC bias V_{DC}) and I is the output of a two-port system, the system can be described by:

$$I(V) = I(V_{DC} + v_{sig}) = A_1(s_1)v_{sig} + A_2(s_1, s_2)v_{sig}^2 + A_3(s_1, s_2, s_3)v_{sig}^3 + \ldots \quad (4.8)$$

where $A_n(s_1, \ldots, s_n)$ are the Volterra series coefficients.

For a narrowband signal $v_{sig} = M\cos(\omega_0 t)$, the corresponding output narrowband signal i_{sig} is the sum of all the terms containing $\cos(\omega_0 t)$, which is:

$$i_{sig} = A_1(s_1)M + \frac{3}{4}A_3(s_1, s_2, s_3)M^3 + \frac{5}{8}A_5(s_1, s_2, s_3, s_4, s_5)M^5 + \ldots \quad (4.9)$$

In general, most systems are of low-order and the coefficients of the higher terms are much smaller than those of the low-order ones. To find the 1dB compression point, the ratio of all the terms in (4.9) to the linear term $A_1(s_1)$ needs to be taken and that ratio set equal to -1dB. Ignoring the higher-order terms, this gives:

$$\frac{A_1(s_1)M + \frac{3}{4}A_3(s_1, s_2, s_3)M^3}{A_1(s_1)M} = 10^{-1/20} \quad (4.10)$$

$$0.109A_1(s_1)M + \frac{3}{4}A_3(s_1, s_2, s_3)M^3 \approx 0 \quad (4.11)$$

Solving the equation above for M^2, we get the input-referred 1dB compression point under matched conditions as:

$$P_{1db} = \frac{M_{odd}^2}{2R_S} \approx \left| \frac{A_1(s_1)}{13.8A_3(s_1, s_2, s_3)R_S} \right| \quad (4.12)$$

Similarly, the input-referred third-order intercept point (P_{IIP3}) is given by:

$$P_{IIP3} = \frac{M_{3rd}^2}{2R_S} \approx \left| \frac{2A_1(s_1)}{3A_3(s_1, s_2, s_3)R_S} \right| \tag{4.13}$$

To determine the coefficients to solve for these values, the circuit of the mixer must be analysed and the system be represented as a Volterra series, since the system is not memoryless and, therefore, a Taylor series would not be appropriate to represent the system. In a switching mixer, the linearity is mostly determined by the transconductance stage. As such, analysing this stage and writing the current output as a function of the signal input as an expanded Volterra series would result in the values we need.

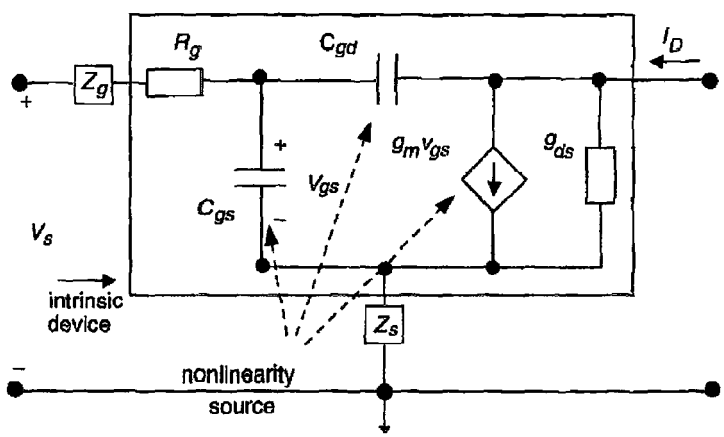

Figure 4.4: Nonlinear model of mixer transconductance stage [27].

Figure 4.4 shows a nonlinear model of a CMOS mixer's transconductance stage. KVL and KCL equations on this circuit result in:

$$V_s = X_1(V_{gs1} - V_{gs2}) + X_2(I_{d1} - I_{d2}) \tag{4.14}$$

$$0 = Y_1(V_{gs1} + V_{gs2}) + Y_2(I_{d1} + I_{d2}) \tag{4.15}$$

where

$$X_1 = 1 + Y_1(Z_g + Z_s + R_g) \tag{4.16}$$

$$X_2 = Y_2(Z_g + Z_s + R_g) - (Z_g + R_g) \tag{4.17}$$

$$Y_1 = j\omega C_{gs} + g_m + \frac{g_{ds}(j\omega C_{gd} + g_m)}{g_{ds} + j\omega C_{gs}} \tag{4.18}$$

$$Y_2 = \frac{g_{ds}}{g_{ds} + j\omega C_{gs}} \tag{4.19}$$

The drain current of either transistor can therefore be expressed as a Taylor series, which results in [27]:

$$I_d = WC_{ox}v_{sat}\frac{V_{od}^2}{V_{od} + L\varepsilon_{sat}} = T_0 + T_1 V_{gs} + T_2 V_{gs}^2 + \ldots \tag{4.20}$$

where C_{ox} is the gate capacitance per unit area, ν_{sat} is the saturation velocity, ε_{sat} is the field strength of velocity saturation, $V_{od} = V_{gs} - V_t$ and the Taylor series coefficients T_n are:

$$T_0 = WC_{ox}\nu_{sat}\frac{V_T}{-V_T + L\varepsilon_{sat}} \tag{4.21}$$

$$T_1 = \frac{-WC_{ox}\nu_{sat}V_T\left(2 + \frac{1}{-V_T + L\varepsilon_{sat}}\right)}{-V_T + L\varepsilon_{sat}} \tag{4.22}$$

$$T_2 = \frac{WC_{ox}\nu_{sat}\left(1 + V_T\frac{-V_T + 2L\varepsilon_{sat}}{(-V_T + L\varepsilon_{sat})^2}\right)}{-V_T + L\varepsilon_{sat}} \tag{4.23}$$

$$T_3 = -WC_{ox}\nu_{sat}\varepsilon_{sat}^2\frac{L^2}{(-V_T + L\varepsilon_{sat})^4} \tag{4.24}$$

The gate-source voltages of the transistors can be expressed as a Volterra series:

$$V_{gs1} = C_1(s_1)V_s + C_2(s_1, s_2)V_s^2 + C_3(s_1, s_2, s_3)V_s^3 + \ldots \tag{4.25}$$

$$V_{gs2} = -C_1(s_1)V_s + C_2(s_1, s_2)V_s^2 - C_3(s_1, s_2, s_3)V_s^3 + \ldots \tag{4.26}$$

Substituting (4.20), (4.25) and (4.26) into (4.14) and (4.15) would allow us to solve for the Volterra series coefficients, which results in:

$$C_1(s_1) = \frac{1}{2(X_1(s_1) + T_1 X_2(s_1))} \tag{4.27}$$

$$C_2(s_1, s_2) = -\frac{T_2 C_1(s_1) C_1(s_2) a_1(s_1 + s_2)}{a_1(s_1 + s_2) + T_1 a_2(s_1 + s_2)} \tag{4.28}$$

$$C_3(s_1, s_2, s_3) = -\frac{X_2(s_1 + s_2 + s_3)[2T_2\overline{C_1 C_2} + TC_1(s_1)C_1(s_2)C_1(s_3)]}{X_1(s_1 + s_2 + s_3) + T_1 X_2(s_1 + s_2 + s_3)} \tag{4.29}$$

where

$$\overline{C_1 C_2} = \frac{C_1(s_1)C_2(s_2, s_3) + C_1(s_2)C_2(s_1, s_3) + C_1(s_3)C_2(s_1, s_2)}{3} \tag{4.30}$$

$$X_1(s) = 1 + (Z_g + Z_s + R_g)\left[sC_{gs} + g_m + \frac{g_{ds}(sC_{gd} - g_m)}{g_{ds} + sC_{gd}}\right] \tag{4.31}$$

$$X_2(s) = \frac{g_{ds}}{g_{ds} + sC_{gs}}(Z_g + Z_s + R_g) - (Z_g + R_g) \tag{4.32}$$

$$a_1(s) = sC_{gs} + g_m + \frac{g_{ds}(sC_{gd} - g_m)}{g_{ds} + sC_{gd}} \tag{4.33}$$

$$a_2(s) = \frac{g_{ds}}{g_{ds} + sC_{gs}} \tag{4.34}$$

We now know the Taylor series coefficients for (4.20) that describe the drain current as a function of the gate-source voltages. We also know the Volterra series coefficients for both (4.25) and (4.26) that describe the gate-source voltages as functions of the input voltage. We can now cascade these two equations to get the coefficients for the Volterra

series equation that describes our two-port system, which is given in (4.9). The coefficients for that equation are:

$$A_1(s_1) = T_1 C_1(s_1) \tag{4.35}$$

$$A_2(s_1, s_2) = T_1 C_2(s_1, s_2) + T_2 C_1(s_1) C_1(s_2) \tag{4.36}$$

$$A_3(s_1, s_2, s_3) = T_1 C_3(s_1, s_2, s_3) + 2T_2 \overline{C_1 C_2} + T_3 C_1(s_1) C_1(s_2) C_1(s_3) \tag{4.37}$$

Now that we have these coefficients, they can be used to solve for P_{1dB} by substituting their values into (4.12). They can also be used to solve for P_{IIP3} by substituting their values into (4.13). This would give us calculated values for these two important mixer parameters.

4.2 CIRCUIT IMPLEMENTATION

The mixer described was designed and fabricated in TSMC's 0.18μm CMOS process. The mixer was implemented in a double-balanced configuration. The deep n-well option available in this process and in many modern CMOS processes was essential for the implementation of this circuit.

The circuit diagram of the design is shown in Figure 4.5. M_1 acts as the current source, regulating the current to ensure stable operation. M_2-M_5 perform the transconducting of the RF signal and switching the transconducted signal according to the LO signal. Finally, the two resistors R_L act as the load, converting the current back to a voltage. These components comprise the mixer core of this circuit.

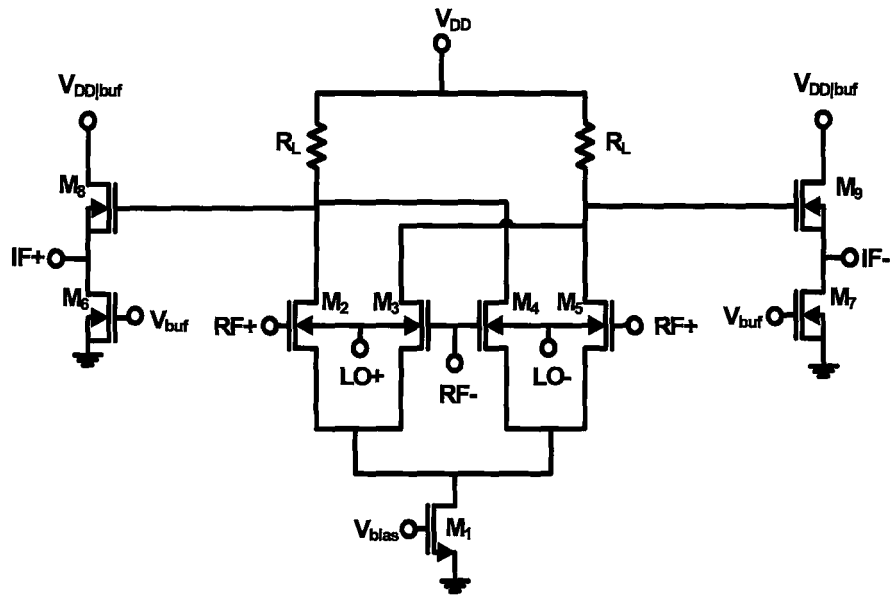

Figure 4.5: Circuit diagram of fabricated body-input mixer.

However, for purposes of measurement, a buffer must be used. This is because any equipment connected to the output of the mixer core (Figure 4.2) would load down that point and change all the biasing points of the circuit, resulting in inaccurate measurement results. By using a buffer, we are extracting the signal at the output of the mixer core without affecting its operation. Since a low voltage supply of 0.8V was used in this design, it was necessary to use a separate V_{DD} (of 1.2V) for the buffer to ensure that the buffer did not degrade the performance of the mixer considerably.

While designing the mixer circuit, M_2-M_5 were biased very close to their threshold voltage. The reason for this was two-fold. Firstly, this would allow the saturation drain-source voltage of those transistors to be low, thereby allowing the required voltage drop across those transistors to be low as well. Secondly, the required swing at the LO port to

cause the transistor to turn on and off would be decreased. This is equivalent to saying that it reduces the LO power requirement.

The physical layout of the design is shown in Figure 4.6. The large pads surround the circuit, and were used for bonding the design into a 80-pin package for testing purposes. Table 4.1 lists the sizes and values of all the important parameters in the design.

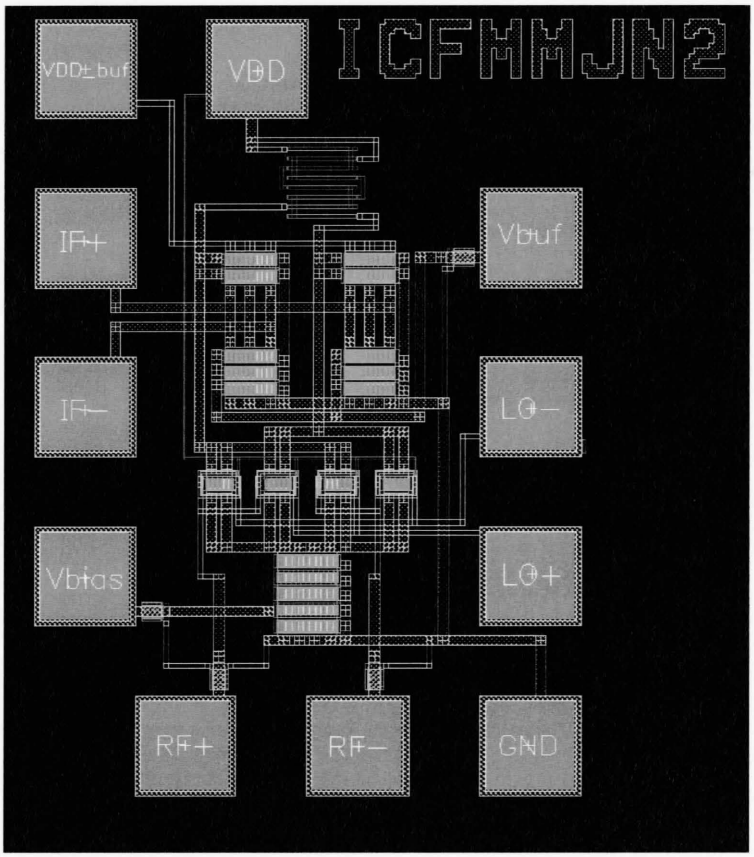

Figure 4.6: Physical layout of body-input mixer.

Table 4.1: Design Parameters.

M_1	W/L = 500μm/1μm
M_2-M_5	W/L = 50μm/0.18μm
M_6-M_7	W/L = 200μm/0.18μm
M_8-M_9	W/L = 300μm/0.18μm
R_L (Ω)	500
Supply Voltage (V)	0.8
Buffer Supply Voltage (V)	1.2
RF Bias Voltage (V)	0.7
LO Bias Voltage (V)	0
RF Input Power (dBm)	-25
LO Input Power (dBm)	0

4.3 SIMULATION RESULTS

Simulations for this circuit were done in SpectreRF, a simulation tool available under the Cadence environment. The models used for the devices were provided by CMC. The circuit was designed to operate at a supply voltage of 0.8V.

Figure 4.7 shows two simulated performance characteristics of the circuit, the conversion gain and noise figure, as a function of the LO input power. The conversion gain increases with increasing LO input power upto a point - this is as a result of the improvement in the switching characteristic with increasing LO power since the transistors are turned on and off completely. After that point, the conversion gain begins to decrease as a result of the RF transistors' biases being changed. The noise figure decreases with increasing LO input power, since the LO power approaches a value that alternatingly turns the

transistors pairs off completely. However, at a certain point, the increasing LO power begins to increase the noise figure since the conversion gain drops off as well. The optimum point to both maximize conversion gain and minimize noise figure is chosen as the LO input power, in this case 0dBm. At this point, the simulated conversion gain is 3dB and the simulated noise figure is 10dB.

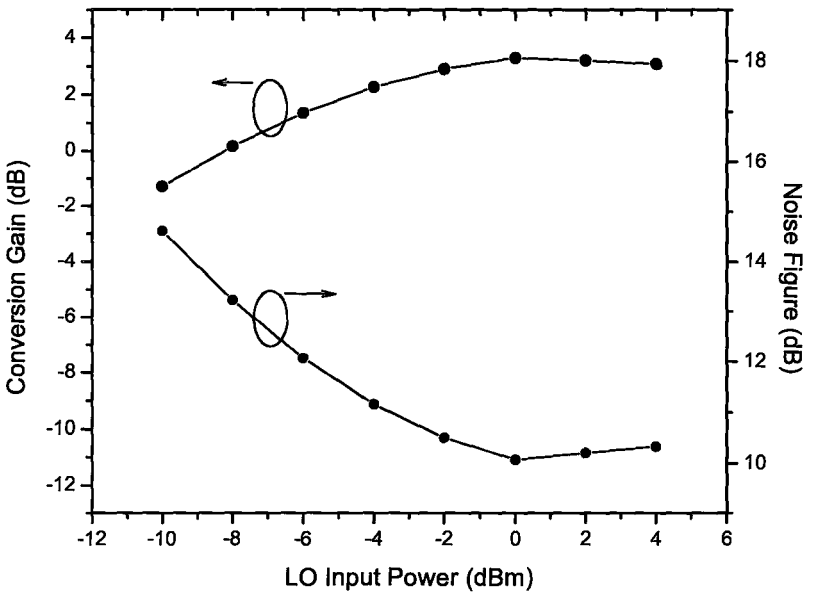

Figure 4.7: Simulated conversion gain and noise figure vs. LO input power of body-input mixer, with RF input power constant at -25dBm.

Figure 4.8 shows the output power as a function of the RF input power. The curve is shown for both the 1st and 3rd harmonics of the output signal. For the output, the power increases proportionally to the input power until it reaches a level where the dynamic range of the transistor is reached. The increase in the 1st order output power compared to the input power is the conversion gain, and is seen to be 3dB.

The linearity of the circuit is determined by taking the intersection of the ideal 1st and 3rd harmonics. This point, the IIP3, is simulated to be -11dBm, as can be seen in the figure.

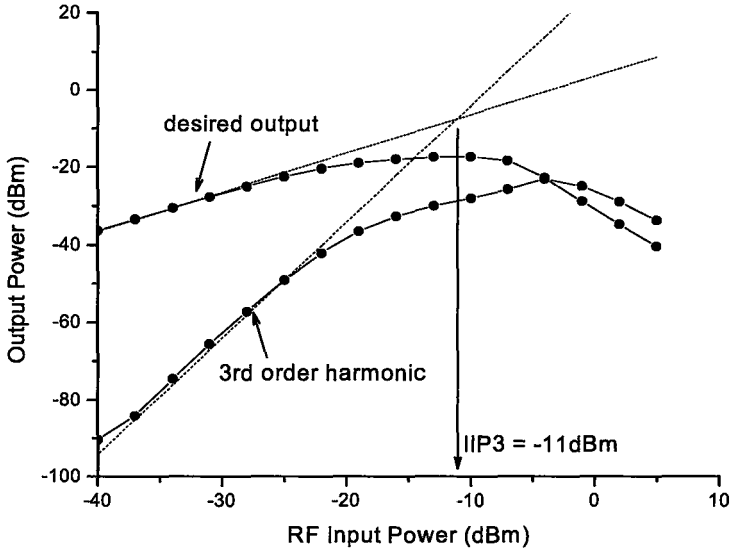

Figure 4.8: Simulated output power of 1st and 3rd harmonics vs. RF input power of body-input, with LO input power constant at 0dBm.

Figure 4.9 shows the supply voltage effects on the conversion gain and noise figure. As can be seen from the figure, the conversion gain and noise figure is relatively stable for the range 0.2V above the chosen supply voltage of 0.8V, since most of the biases remain the same. This means that small increases in the supply voltage would not have a significant effect on the performance of the mixer. However, since the mixer is biased so close to its threshold, decreases in the supply voltage can have an adverse result on the performance parameters, since a decrease in supply voltage would in turn decrease the source voltages

of the RF transistors and take them into the cut-off region of operation. When this mixer is implemented, care should be taken to ensure the supply voltage is relatively stable.

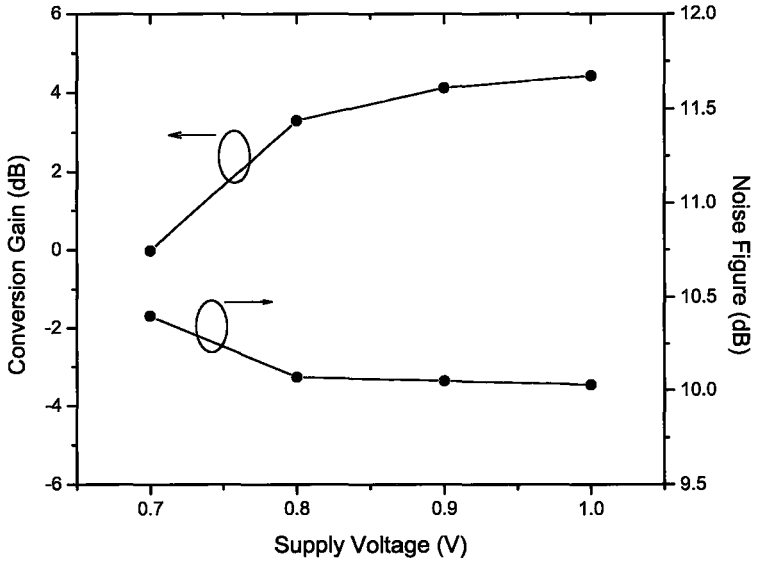

Figure 4.9: Simulated conversion gain and noise figure vs. supply voltage of body-input mixer.

The important simulated parameters and performance characterics are summarized in Table 4.2.

Table 4.2: Summary of simulation results for body-input mixer.

Supply Voltage (V)	0.8
Power Consumption (mW)	0.4
RF Input Frequency (GHz)	1.9
RF Input Power (dBm)	-25
LO Input Frequency (GHz)	1.65
LO Input Power (dBm)	0
IF Output Frequency (MHz)	250
Conversion Gain (dB)	3
SSB Noise Figure (dB)	10
IIP3 (dBm)	-11

4.4 MEASUREMENT RESULTS

The fabricated circuits were measured in the lab. The actual experiment procedure, including the equipments that were used, is outlined in the Appendix. We got good correspondence between the simulation and measurement results.

As in simulation, the mixer core was operated at a supply voltage of 0.8V, which was provided by a Semiconductor Parameter Analyzer. The other voltages necessary in the circuit were also provided by the same equipment. The LO and RF signals were produced by Signal Generators and fed through bias-Ts and 0°/180° splitters to achieve the necessary non-zero centered and differential signals.

Figure 4.10 shows the output power as a function of the input power. On this curve, as discussed in Chapter 3, the intersection of the ideal 1st- and 3rd-order harmonic curves is identified as the IIP3. The measured result of the IIP3 was -9dBm. From this

graph, we can also ascertain the conversion gain of the circuit. At -25dBm of input power, the measured conversion gain is 1dB.

The measured value of the IIP3 being higher than the simulated value may seem counterintuitive. However, what has happened in this circuit is that, due to uncompensated non-idealities in the cables, test fixture, pins, bonding wire and pads, the signal delivered to the circuit is attenuated, and so the point on the linearity-gain tradeoff that the circuit operates has changed. As a result, the lower gain is compensated by the higher linearity. Overall, however, we still see a lower measured result, as expected, since the linearity is higher by 2dB but the conversion gain is lower by 3dB compared to simulation.

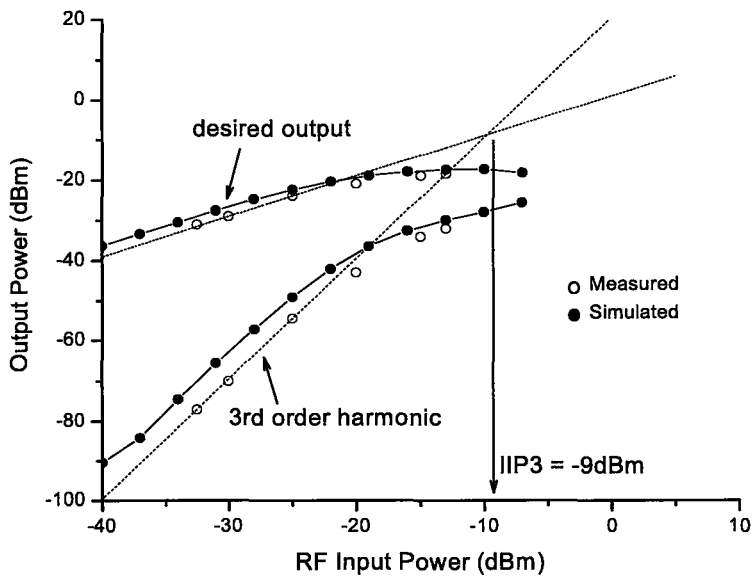

Figure 4.10: Measured output power of 1st and 3rd harmonics vs. RF input power of body-input mixer, with LO input power constant at 0dBm.

Figure 4.11 shows the supply voltage dependence of the conversion gain and noise figure. As can be seen from that figure, above 0.8V (which is the operating voltage of this

circuit), the parameters are relatively steady. Compared to the simulation results, the conversion gain is lower, as mentioned, and the noise figure at 0.8V is 11dB, 1dB higher than the simulated value.

Below a supply voltage of 0.8V, the RF transistors are no longer biased properly in saturation. This causes the conversion gain to drop off. The noise figure, in turn, increases as a result of this drop in conversion gain and imperfect switching.

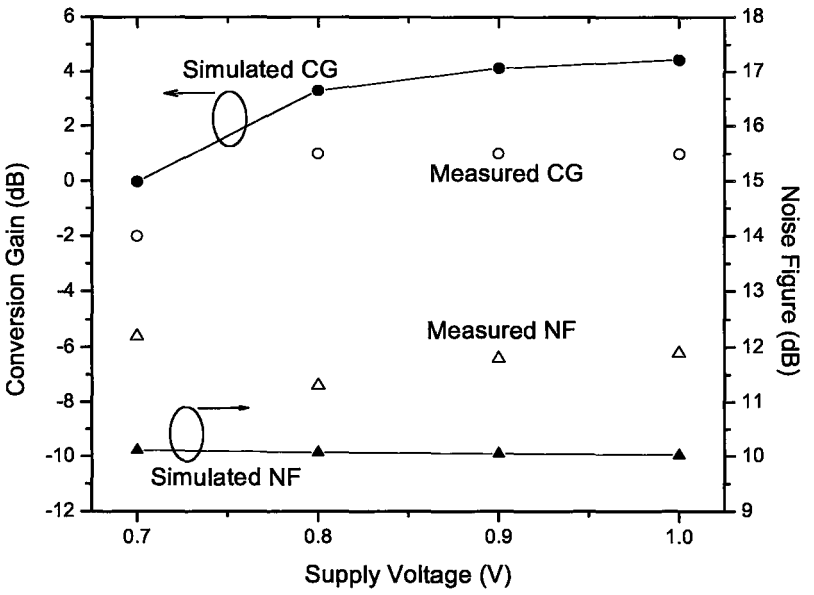

Figure 4.11: Measured conversion gain and noise figure vs. supply voltage of body-input mixer.

The important measured parameters and performance characterics are summarized in Table 4.3.

Table 4.3: Summary of measurement results for body-input mixer.

Supply Voltage (V)	0.8
Power Consumption (mW)	0.4
RF Input Frequency (GHz)	1.9
RF Input Power (dBm)	-25
LO Input Frequency (GHz)	1.65
LO Input Power (dBm)	0
IF Output Frequency (MHz)	250
Conversion Gain (dB)	1
SSB Noise Figure (dB)	11
IIP3 (dBm)	-9
LO-IF Isolation (dB)	31
RF-IF Isolation (dB)	33

4.4.1 Temperature Effects

To get an idea of how this circuit would perform in a real-world setting, we measured the different performance parameters under varying temperatures. As a result of the limitation of the only equipment we had access to, the measurements were only performed over the range from room temperature (approx. 23°C) to 75°C.

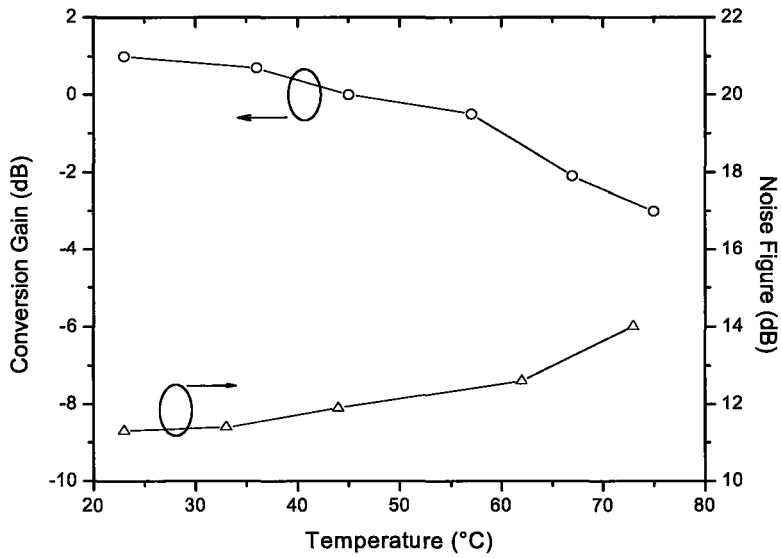

Figure 4.12: Measured conversion gain and noise figure vs. temperature of body-input mixer.

As can be seen in Figure 4.12, both the conversion gain and noise figure degraded with increasing temperature. The conversion gain went from 1dB at room temperature to -3dB at 75°C. The noise figure went from 11dB to 14dB in approximately the same range of temperature. Note that this degradation would have been more significant if the current had not increased with temperature as well.

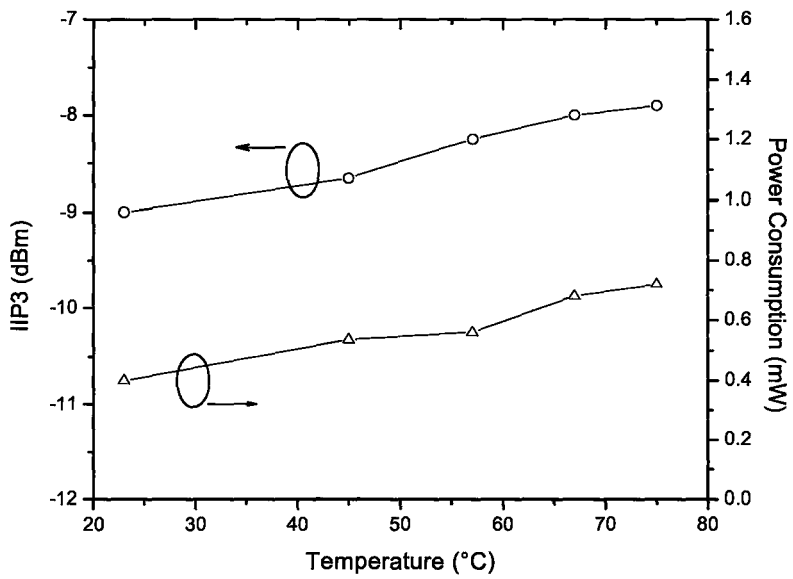

Figure 4.13: Measured linearity and power consumption vs. temperature of body-input mixer.

Considering the current, which increased from 0.5mA (corresponding to 0.4mW) at room temperature to 0.9mA (corresponding to 0.72mW) at 75°C with all voltages constant, together with the other performance parameters would be more complete in gauging the overall performance impact of the temperature on the circuit.

The linearity changed only slightly in the same range, going from -9dBm at room temperature to -8dBm at 75°C. This improvement in linearity can be explained as a result of being compensated by the increasing current and decreasing conversion gain.

4.5 COMPARISONS

To compare this circuit to other mixer circuits, we must make use of a performance metric that can take into account all the common parameters that define the performance of a mixer. The measure, called a figure of merit (FoM), that we use in this work is:

$$FoM = 20\log(f_{RF}) + CG - NF + IIP3 - 10\log(P_C) \ , \tag{4.38}$$

where f_{RF} is the frequency of the RF signal in Hz normalized to 1Hz, CG is the conversion gain in dB, NF is the noise figure in dB, $IIP3$ is the measure of linearity in dBm and P_C is the power consumption in W normalized to 1W.

Table 4.4 shows the simulated and measured FoMs of the design presented in this chapter compared to the FoMs of other recently published mixer designs. Note that [11] is a design from a member of the same research group as the author and [29] is a mixer design that also makes use of the body as an input.

Table 4.4: Comparison of FoMs of mixer designs.

	Technology	**f_{RF}** *GHz*	**CG** *dB*	**NF** *dB*	**IIP3** *dBm*	**P_C** *mW*	**FoM**
Simulated	*0.18μm*	*1.9*	*3*	*10*	*-11*	*0.4*	*202*
Measured	**0.18μm**	**1.9**	**1**	**11**	**-9**	**0.4**	**201**
[11]	0.18μm	1.9	-2	17	8	3.95	199
[28]	0.25μm	1.9	3.6	12.5	-1	4.5	199
[29]	0.18μm	2.4	10	14	-5	12	198
[30]	0.8μm	0.9	-8.4	28	25.5	1.5	196
[12]	0.35μm	0.9	2	13.5	3.5	4.7	194
[10]	0.8μm	1.9	0.5	10.2	-6	4	194
[30]	0.5μm	0.9	-2.2	22	6	3	186

4.6 DISCUSSIONS

Our primary interest in the design of this mixer circuit was low-voltage and low-power operation. The body-input mixer is able to achieve these goals with good performance parameters. This would allow this circuit to be used in receivers where voltage and power performance is critical.

One of the disadvantages of this circuit is that it has a high LO power requirement because the signal is fed into the body of the transistor. Effort would need to be put into the design of a VCO which would provide this LO signal while maintaining low voltage and low power performance. Also, the possibility of reducing the LO power requirement by applying a DC bias to the body needs to be investigated.

Another disadvantage is the relatively low linearity performance. However, for the applications for which this circuit is designed, where input power levels are very low, this should not be a significant problem.

Chapter 5

FOLDED MIXER

As we mentioned in Chapter 4, the Gilbert cell mixer topology is used extensively even today, but has some inherent limitations. The stacked nature of the topology limits how much you can reduce the supply voltage. In Chapter 4, we described one method to alleviate this limitation of lowering the minimum supply voltage by using the body of the transistor as an input. Another method of achieving this lower supply voltage requirement is explored in this chapter.

Unlike the previous chapter's design where we used one set of transistors to do two functions, the folded mixer topology continues to use two seperate sets of transistors doing the two functions; however, it puts the two transistors in parallel, instead of stacking them. As a result, we are able to lower the minimum supply voltage as compared to the Gilbert cell mixer, since the supply voltage needs to be enough only to keep one transistor in saturation (allowing for the voltage drop across the load).

Another advantage of the folded mixer topology is the fact that, since the transistors are placed in parallel, they have separate DC current paths. This is particularly important since, as mentioned in Chapter 3 in the discussion on the current bleeding mixer topology, the optimal current for the two sets of transistors doing the two functions

(transconducting and switching) are completely different. The transconducting transistors require a higher DC current, so as to increase the g_m of the transistors and therefore increase the overall gain of the circuit. Conversely, the switching transistors need to have a lower DC current to allow for lower LO power required for complete switching, as well as lower gate-source voltage and smaller sizes for those transistors. This is because the less the charge in the transistors, the easier it is to turn them on or off.

Finally, the lower current in the switching transistors' path would also be the same current through the load; this would allow for a larger load than would normally be used in a Gilbert cell, since the voltage drop would not significantly limit the mixer's performance. As the output voltage is taken across this load, this would result in a higher overall gain of the circuit. Since our focus is low-power, a circuit using this topology could be designed for lower power consumption by sacrificing some of the gain, and still have an acceptable level of gain.

The idea of folded topologies has been used in other circuits where stacked devices limit performance. In mixers, this idea has also been used previously. In [30], the authors designed two folded mixers - however their target voltage levels were much higher, at 2V and 3V, and their noise figure levels were relatively high. In addition, their paper does not discuss the advantage of having the two separate DC current paths - it is not clear if they made use of this in their design or not.

The authors in [15] have taken a very novel approach in developing a folded topology. This design was discussed in Chapter 3 and uses a very simple idea to achieve very good results. The topology also achieves very good efficiency by employing current-reuse,

which allows the current through the RF stage to flow into the LO stage, despite the fact that they are parallel with respect to the voltage source. However, a minor disadvantage is that the design requires the differential RF signals to be fed in two times each, with different voltage biases; this cannot be achieved without either extra off-chip circuitry or complicated on-chip components.

5.1 CIRCUIT ANALYSIS

The circuit of the folded mixer is shown in Figure 5.1.

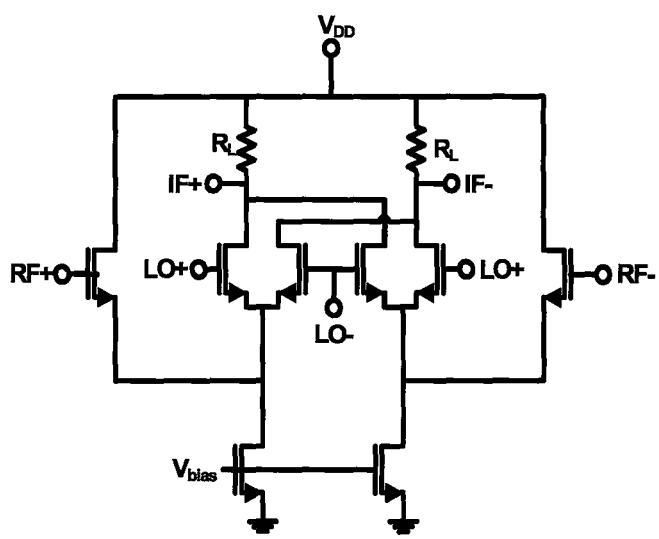

Figure 5.1: Circuit diagram of folded mixer.

The RF signal is applied differentially to the gates of the two transconducting transistors. The LO signals are applied differentially to the gates of the switching transistors, in anti-phase to the RF signals. Just like the body-input mixer, this circuit is also of a double-balanced nature. This property reduces the noise figure and also reduces the LO-IF feedthrough in the circuit.

The circuit requires two separate current sources for each differential side of the circuit. This is because the differential RF signals would mix if there was only one current source. This is not an issue in the Gilbert cell topology because the LO switching transistors are stacked above the RF transconductance transistors, and any RF signal mixed at the current source does not make a difference to the LO stage.

The equivalent circuit representation of the folded mixer is shown in Figure 5.2. The figure is shown for the case when the LO signal is high.

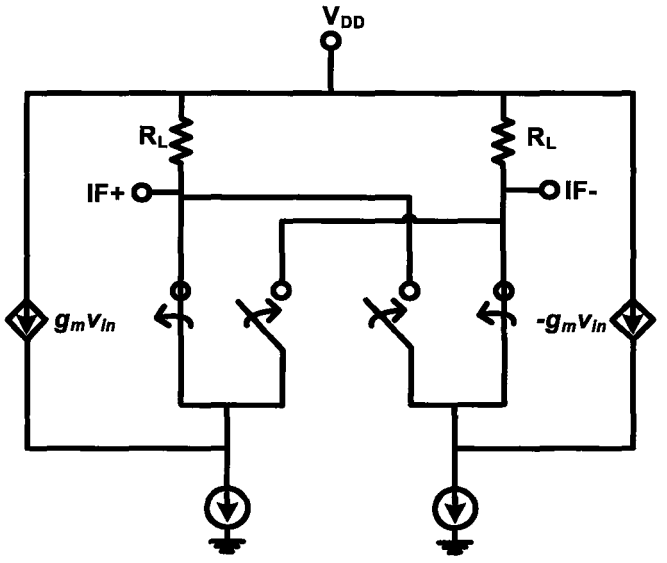

Figure 5.2: Equivalent circuit representation of folded mixer.

The RF transconducting transistors in this circuit can be represented by dependent current sources, since they convert the input signal v_{in} to a current multiplied by the gain of the transistors g_m. This small-signal current sees the DC tail current source as an open circuit and, therefore, most of it flows into the LO switching transistors, which are represented by switches that connect these small-signal currents to the loads.

For the case when the LO signal is high (as is shown in the figure), one of each of the two sets of LO switching transistors is conducting. Therefore, the signals flow to the output v_{out}, which is taken differentially as shown.

5.1.1 Gain

The derivation of the expression for gain for this circuit is very similar to the expression for gain for both the Gilbert cell and body-input mixers. This is because all of them have the same two parts of the circuit that dictate the gain - the transconducting transistors and the load. The only difference is that the direction of the dependent current sources are different.

When the LO signal is in its positive phase (as in Figure 5.2), the switches connected to LO+ are closed and $v_{out} = (-g_m v_{in})R_L - (g_m v_{in})R_L = -2g_m v_{in} R_L$. Conversely, when the LO signal is in its negative phase, $v_{out} = (g_m v_{in})R_L - (-g_m v_{in})R_L = 2g_m v_{in} R_L$. This is equivalent to multiplying the current from the transconductance part by a square wave with the same frequency as the LO signal.

In Chapter 3, the gain was derived based on the outputs during the two different phases of the LO for the body-input mixer and is the same in this circuit. Therefore, the expression for the gain of this circuit is:

$$G = \frac{V_{out}}{V_{in}} = g_m R_L \frac{4}{\pi}. \tag{5.1}$$

Since the g_m in this topology is higher as a result of the higher current flowing through the transconductance transistors, the gain is therefore also higher.

5.1.2 Linearity

The linearity of any switching mixer is limited by many different parts, including the transconducting transistors, the switching transistors, the tail current source and even the load to a certain extent. However, it is the transconducting transistor that has the largest effect on the linearity, since it is those transistors that convert the small-signal input voltage into a small-signal current [6]. Although one could derive the linearity based on the switching transistors, current source and the load as well, their contributions are relatively small and beyond the scope of this thesis.

In this circuit, the main focus of improving linearity was on the RF transconducting transistors. As mentioned earlier, one of the advantages of the folded mixer topology is the fact that more DC current is supplied to the RF transistors, where it is beneficial. The distortion introduced by the transconductance transistors is inversely proportional to the tail current in a Gilbert cell mixer [6]. In this circuit, the equivalent statement would be that the distortion is inversely proportional to the current going through the transconductance transistors. Therefore, as a result of the increased DC current in the RF transistors, the linearity in this topology is improved.

5.2 CIRCUIT IMPLEMENTATION

The mixer described was designed for the 0.18μm CMOS process. It was designed in a double-balanced configuration and made use of the simulation models made available by the Canadian Microelectronics' Corporation (CMC).

The circuit diagram of the design is shown in Figure 5.3. M_1 and M_2 act as the current sources, regulating the current to ensure stable operation. M_3 and M_4 perform the transconducting of the RF signal. M_5-M_8 are switching the transconducted signal according to the LO signal. Finally, the two resistors R_L act as the load, converting the current back to a voltage. These components comprise the mixer core of this circuit.

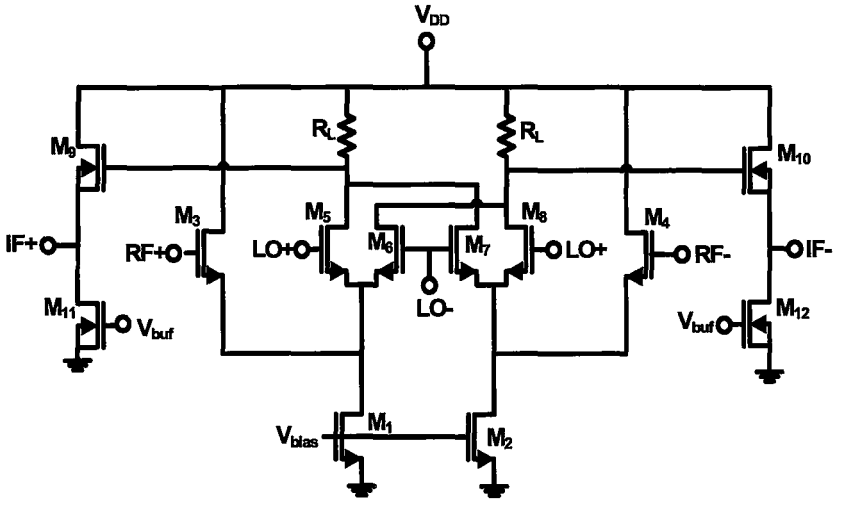

Figure 5.3: Circuit diagram of fabricated body-input mixer.

To be able to measure the output of the circuit without affecting its function, a buffer must be used. Since the voltage drop across the resistor was relatively low, the voltages at the gates of M_9 and M_{10} was also very low. As a result, the buffer was designed with those two transistors being pMOSFETs, since they are able to operate with the gate voltage close to V_{DD}.

M_3 and M_4 are biased such that the gate overdrive voltage is significantly higher than typical biasing in a Gilbert cell. Whereas in a Gilbert cell, the current through these transistors is a concern as it would impact switching and voltage across the load, in this circuit it is an advantage to have relatively higher current flowing through the transconductance transistors.

On the other hand, M_5-M_8 are biased such that the current through those paths are lower. As mentioned earlier, this is to allow for better switching and also to allow for a larger load to be used (which would, in turn, increase the gain).

Table 5.1 lists the sizes and values of all the important parameters in the design.

Table 5.1: Design Parameters of folded mixer.

M_1-M_2	W/L = 50μm/1μm
M_3-M_4	W/L = 10μm/0.18μm
M_5-M_8	W/L = 20μm/0.18μm
M_9-M_{10}	W/L = 100μm/0.18μm
M_{11}-M_{12}	W/L = 200μm/0.18μm
R_L (kΩ)	5
Supply Voltage (V)	1
RF Bias Voltage (V)	0.8
LO Bias Voltage (V)	0.7
RF Input Power (dBm)	-25
LO Input Power (dBm)	-15

5.3 SIMULATION RESULTS

Simulations for this circuit were done in SpectreRF under the Cadence environment. The models used for the devices were made available by CMC. The circuit operates at a supply voltage of 1V.

Two performance characteristics of the circuit, the conversion gain and noise figure, as a function of the LO input power are shown in Figure 5.4. The noise figure decreases with increasing LO swing, since the LO transistors begin to turn on and off completely. The conversion gain, on the other hand, increases with increasing LO swing upto a point as the switching characteristic improves. At that point, the excessive LO drive reduces the gate overdrive of the RF transistors because of the increase in their source voltages. This is because part of the voltage of the LO transistors gets coupled to its source, which is the same as the source of the RF transistors. The LO swing chosen for this circuit is -15dBm, which results in the best combination of noise figure and conversion gain for the given circuit.

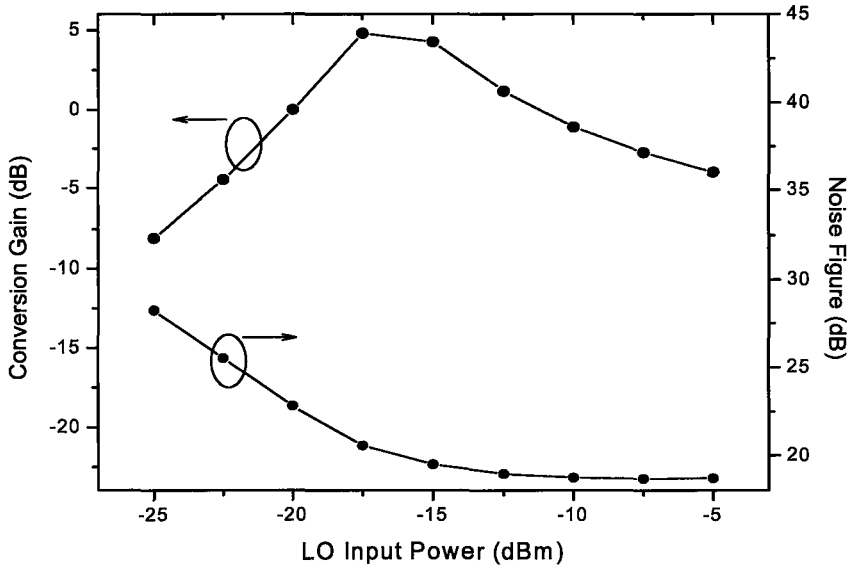

Figure 5.4: Simulated conversion gain and noise figure vs. LO input power of folded mixer, with RF input power constant at -25dBm.

The output power at the IF as a function of the RF input power is shown in Figure 5.5. The curve is shown for both the 1st-order desired output signal and the 3rd-order harmonic undesired signal. The output power increases proportionally to the input power until it exhibits gain compression and leaves the dynamic range of the transconductance transistors. The increase in the 1st order output power compared to the input power is the conversion gain, and is seen to be 4dB on the graph.

The linearity of the circuit can be determined by taking the intersection of the ideal 1st order and 3rd order harmonic lines. This point, the IIP3, is simulated to be -6.5dBm, as can be seen in the figure.

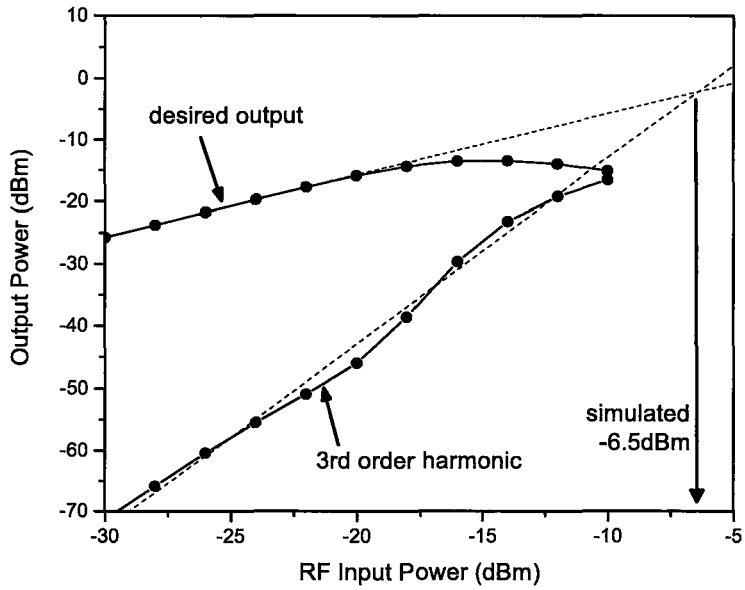

Figure 5.5: Simulated output power of 1st and 3rd harmonics vs. RF input power of folded mixer, with LO input power constant at -15dBm.

Finally, Figure 5.6 shows the supply voltage effects on the conversion gain and noise figure. At the supply voltage value that the circuit was designed for, which is 1V, the conversion gain is maximum and the noise figure is minimum. As the voltage reduces, the RF transistors no longer are in deep saturation, which results in an overall reduced gain and increased noise. In addition, the LO transistors biasing point is changed, resulting in imperfect switching since the LO signal is no longer centered at the threshold voltage, which causes an additional reduction in gain and an increase in noise. As the voltage increases, the RF transistors' gain also increases, resulting in an increased overall gain. However, the LO transistors again experience imperfect switching, resulting in increased overall noise figure.

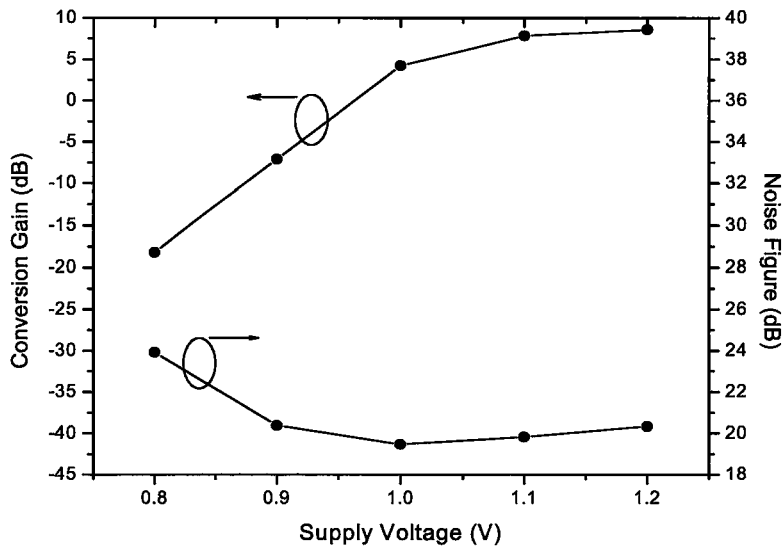

Figure 5.6: Simulated conversion gain and noise figure vs. supply voltage of folded mixer.

The important simulated parameters and performance characterics are summarized in Table 5.2.

Table 5.2: Summary of simulation results for folded mixer.

Supply Voltage (V)	1
Power Consumption (mW)	0.64
RF Input Frequency (GHz)	2.4
RF Input Power (dBm)	-25
LO Input Frequency (GHz)	2.3
LO Input Power (dBm)	-15
IF Output Frequency (MHz)	100
Conversion Gain (dB)	4
SSB Noise Figure (dB)	19
IIP3 (dBm)	-6.5

5.4 COMPARISONS

We again use the figure of merit (FoM) presented in Chapter 4 to compare this design with other recently published mixer designs.

Table 5.3: Comparison of FoMs of mixer designs.

	Technology	**f_{RF}** *GHz*	**CG** *dB*	**NF** *dB*	**IIP3** *dBm*	**P_C** *mW*	**FoM**
Chapter 4 - simulated	0.18µm	1.9	3	10	-11	0.4	202
Chapter 4 - measured	0.18µm	1.9	1	11	-9	0.4	201
[11]	0.18µm	1.9	-2	17	8	3.95	199
[28]	0.25µm	1.9	3.6	12.5	-1	4.5	199
Folded Mixer	**0.18µm**	**2.4**	**4**	**19**	**-6.5**	**0.64**	**198**
[29]	0.18µm	2.4	10	14	-5	12	198
[30]	0.8µm	0.9	-8.4	28	25.5	1.5	196
[12]	0.35µm	0.9	2	13.5	3.5	4.7	194
[10]	0.8µm	1.9	0.5	10.2	-6	4	194
[30]	0.5µm	0.9	-2.2	22	6	3	186

5.5 DISCUSSIONS

The folded mixer is able to achieve better gain and linearity performance as compared to the body-input mixer, at the sacrifice of noise figure and power consumption. For situations where low-voltage and low-power operation is essential, but the relatively lower conversion gain and linearity performance of the body-input mixer is not acceptable, the

folded mixer would be an attractive alternative. Further, it does not have the high LO power requirement of the body-input mixer.

The folded mixer design, as a result of also being folded with respect to the tail current source, has a "leakage" of the AC current into the terminal of the tail current source. This is because the current source is not an AC short as in the ideal case. An idea to limit this leakage and therefore improve gain could be to put a capacitor to be an AC short. However, the effect of that capacitor on the linearity performance of the transconductor would need to be investigated.

In this chapter, the measurement results of the folded mixer have not been presented. This is because the buffer of the fabricated circuit, which is necessary to measure the mixer on it's own, did not perform as intended. Referring to Figure 5.3, the problem is that the gates of M_9 and M_{10} need a voltage lower than V_{DD} by at least the threshold voltage. However, the voltage it is receiving is not that low and therefore the buffer is not operating. This is likely as a result of a layout error or severe mismatch of the load resistance R_L.

Unfortunately, unlike in the design in Chapter 4, the buffer circuitry does not have a separate supply voltage connection. Therefore, there did not appear to be a solution to overcome this problem using the fabricated chip.

Chapter 6

CONCLUSION

6.1 SUMMARY

Downconversion mixers are an integral part of the RF receiver front-end. In this work, we have presented two mixer designs, both designed with the goal of low-voltage and low-power operation.

The first design made use of the body of the transistors as an RF input to allow the functions of two sets of transistors to be done by only one set of transistors. This allowed the voltage supply requirement to be reduced as a result of the reduced stacking of the transistors. This circuit was designed to operate at 1.9GHz, and the measured results showed 1dB of conversion gain, a noise figure of 11dB and an IIP3 of -9dBm, while consuming 0.4mW of power from a 0.8V supply. For this circuit, temperature effects were also investigated, which showed a degradation in power consumption, conversion gain and noise figure, while showing an improvement in linearity.

The second design made use of a folded architecture to allow the voltage supply requirement to be reduced, while at the same time taking advantage of the separate DC current paths to optimize the performance of the transconductance and switching transistors separately. This circuit was designed to operate at 2.4GHz, and the results of simulation

showed 4dB of conversion gain, a noise figure of 19dB and an IIP3 of -6.5dBm, while consuming 0.64mW from a 1V supply.

The ideas used in this work to achieve low-voltage and low-power operation could likely be used in other circuits to achieve the same, especially circuits where stacked transistors are the limitation to achieving this goal.

6.2 FUTURE WORK

There are many mixer topologies that have been proposed to achieve low-voltage and low-power operation. Some of these topologies were discussed in Chapter 3, and two designs were presented using other topologies.

Combining the advantages of the different topologies could further improve performance, for example as done with the design in Chapter 5, where the good parts of the regular folded topology and the current bleeding/injection topology were both used.

Further, generally when measuring packaged chips, there is a disparity between simulation and measurements, partly as a result of losses and non-idealities of the package and board. Either simulating for these losses or measuring on-wafer would result in more accurate measurement results.

6.2.1 Body-Input Mixer

One item that needs to be investigated is ways of making the circuit operate with a lower LO power requirement. The body could be biased at such a value so as to reduce this requirement. This would remove one of the significant disadvantages from the circuit.

The effects of DC body biases on the performance parameters could also be investigated. This will likely show an improvement in the circuit performance, but it is unclear how this would effect the LO power requirement, since the DC bias on that port would no longer be at the centre of the LO swing needed to turn the transistor on and off.

Further, as with any differential mixer, implementing the balun on-chip would greatly reduce the errors due to mismatch in the differential inputs.

6.2.2 Folded mixer

In the fabricated circuit for this design, the issues with the buffer that resulted in this chip not being measurable need to be investigated and resolved. This will likely involve another iteration of the layout and fabrication.

Further, putting a capacitor above the tail current source would likely result in higher gain as a result of lower AC leakage. This needs to be investigated, along with the impact on the linearity of the transconductor.

APPENDIX

To measure the circuit described in Chapter 4, we needed equipment to provide the DC biases and the RF and LO signals. For the DC biases, rather than use several different pieces of equipment for the different biases, we use an Agilent 4156C Semiconductor Parameter Analyzer (SPA) to provide all the DC biases. For the RF and LO signals, we used Signal Generators.

Figure A.1 shows the experiment setup, including all the connections between the device under test (DUT) and the necessary equipment. The RF and LO Signal Generators are connected to 0°/180° splitters that produce differential versions of the respective signal. This is then fed into a Bias-T, which adds the necessary DC offset, produced by the SPA, to the signal. In addition to these inputs, the supply voltage for the mixer core and the buffer, the tail current source bias voltage and the buffer bias voltage are also provided to the circuit by the SPA (refer to Chapter 4 for more information on each input). Only one end of the differential output of the circuit is taken into the Spectrum Analyzer, to simplify the experiment setup. The other end is loaded with 50Ω and, therefore, 3dB would need to be added to the measured output to get the actual result.

The second Signal Generator connected to the RF port is to generate the spurious tone for a two-tone test used to determine the linearity performance of the circuit. This Sig-

nal Generator would usually product a second tone 1MHz higher than the signal of interest generated by the first Signal Generator.

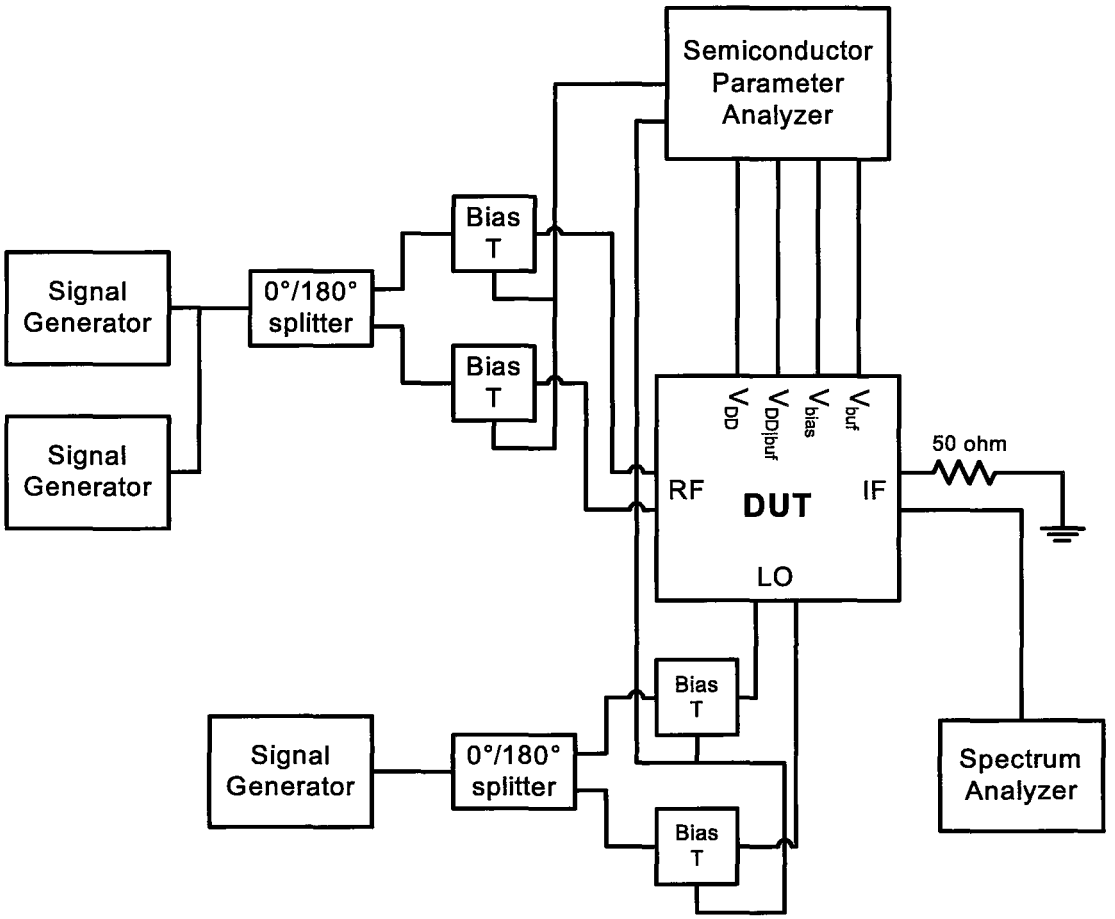

Figure A.1: Experiment setup for body-input mixer.

The losses in the cables and connection were compensated by connecting the inputs to the circuit to the Spectrum Analyzer and increasing the amplitude at the Signal Generators until the desired amplitude is read on the Spectrum Analyzer. For example, if -20dB is required, the Signal Generator amplitude may need to be increased to -17.5dB to realize

a signal of -20dB at the Spectrum Analyzer. Note that this method does not, therefore, compensate for losses in the test fixture, package or bonding wires.

To measure for noise figure, we use a Agilent 8970B Noise Figure Meter. The connection for calibrating the Noise Figure Meter is shown in Figure A.2. After connecting the equipment in this manner, the frequencies and other options in the Noise Figure Meter should be set, and then calibration should be started. This calibration compensates for the losses in the input connections of the experiment setup. The losses in the output connections should be estimated and entered manually into the Noise Figure Meter. We estimated the losses by putting a Signal Generator at one end and measuring the output on the other end using a Spectrum Analyzer.

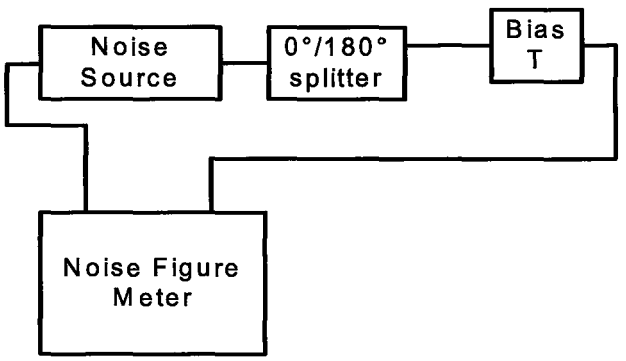

Figure A.2: Noise figure calibration setup for body-input mixer.

After calibration, the setup should be connected as shown in Figure A.3. The frequencies do not need to be set again. The measurement of the noise figure should be done

by selecting "corrected noise figure", which would correct the measured value for the losses calibrated for and the losses in the output connection that have been manually entered.

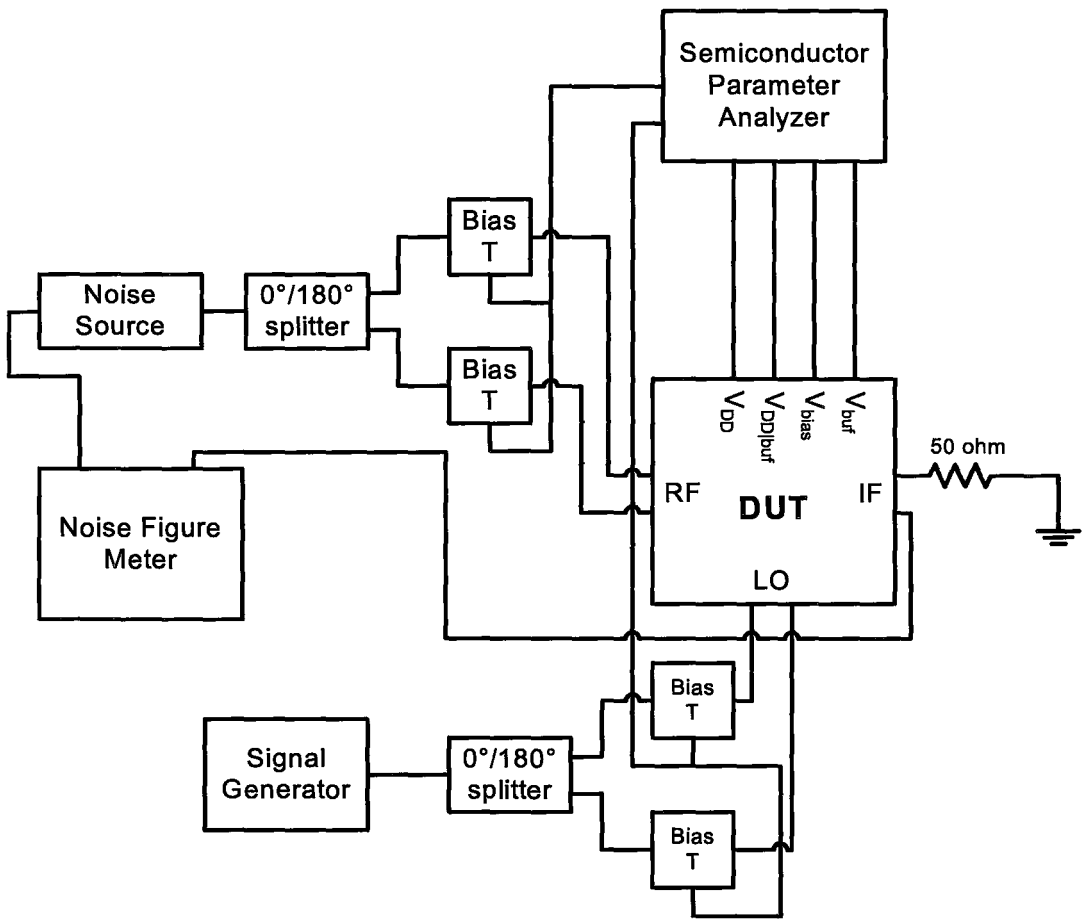

Figure A.3: Noise figure measurement setup for body-input mixer.

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