# MOSFET HIGH-FREQUENCY NOISE

# IMPLEMENTATION OF MOSFET HIGH-FREQUENCY NOISE FOR RF ICS

By

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# ABSTRACT

This thesis focuses on the noise model verification at both device and circuit levels using circuit simulators. The techniques and procedures developed in this thesis are general and can be applied to any proposed RF noise model equations. To fulfil the two tasks, three main topics have been accomplished. First, a general noise source implementation method has been presented in detail in this thesis and is verified with measurements for both long and short-channel MOSFETs. This method provides a simple and effective way to implement the enhanced channel noise and induced gate noise of MOSFETs without increasing the simulation complexity for the simulators.

Second, a systematic procedure to refine the model parameters used in noise calculation is presented. For a model to accurately predict the HF noise characteristics, the accuracy in the prediction of both DC and AC characteristics has to be ensured. The procedure proposed in this thesis provides both DC and AC model parameter verification and optimization for RF noise simulation purpose.

Third, as for benchmark circuits to verify noise model at the circuit level, two LNA designs are proposed in the thesis. The first design gives the emphasis on the noise reduction technique and the LNA design procedure. The proposed noise reduction technique gives circuit designers more control on noise figure minimization through noise matching. The second design is used to experimentally verify the noise model at the circuit level.

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# Chapter 1

# INTRODUCTION

## 1.1 Current Status of MOSFET's Application

From the early 1990s, the development of radio frequency integrated circuits (RF ICs) started to accelerate because of the booming of digital cellular telephone [1]. Bipolar transistors dominated in that area for many years before complementary metal-oxide semiconductor (CMOS) wireless transceivers were widely adopted with the development of very large scale integration (VLSI). In the past, metal-oxide semiconductor field-effect transistors (MOSFETs) were considered as "slow" and "big" devices because of the lower-field mobility in MOSFET's channel and the relatively larger device dimensions than those of bipolars [2]. VLSI not only results in high level of integration but also fast speed CMOS by forcing MOSFETs to scale down. This size reduction of MOSFETs in the past few years helped MOSFET overcome its "shortcomings" and result in strongly improved RF performance metrics which include improved cutoff frequency ($f_T$), maximum oscillation frequency ($f_{max}$), power gain ($g_m$), noise figure ($NF$), linearity and $1/f$ noise [3]. These good features are very attractive for RF designers and they confirm the potential of MOSFETs for RF applications up to tens of gigahertz frequency range. Further more, the appearance of Bluetooth system and IEEE 802.11 WLANs lead to the

trend of wireless transceiver system-on-chip (SOC) which will make MOSFETs more widely adopted for future applications. A statistic result of market share of different semiconductor technologies shows that in the early 2000s about 90% of the market belongs to CMOS and MOSFETs [2].

However, when the transistor's size scales down and the working frequency goes high, small dimensional effects begin to appear and the noise generated within the device itself starts to play an increasingly important role in the overall system performance [9]. This demands that the noise model can not only accurately predict the high frequency noise performance of long-channel MOSFETs but also that of short-channel devices. In addition, although the enhanced channel noise are observed for short-channel MOSFETs working at high frequency, the exact reason and intensity for the enhancement are still not clear and conflict research results are published [5][6][7][8][9] which are difficult to evaluate the accuracy of the proposed noise models. Moreover, in the real RF ICs design, designers are facing challenges due to the strong constraints on power consumption and noise that leave little design margin [4]. In order to ensure the design performance and shorten the time-to-market, compact models that can accurately predict circuit performance (including noise) at high frequency are both crucial and urgent. Therefore, after the high frequency noise model for short-channel devices has been obtained, the next task is how to effectively verify the model at both device and circuit level and then implement it into currently available commercial circuit simulators for real applications.

## 1.2 Problems Solved in the Thesis

Providing that accurate noise models for high frequency deep-submicron MOSFETs have already been obtained, the main focus of this thesis is the noise model verification at both device and circuit levels. To fulfil these two tasks, three main topics have been accomplished in this thesis. They are the new technique to implement the channel noise and the induced gate noise with experimental verifications at both device and circuit levels, the systematic procedure for fine tuning model parameters for RF noise simulation, and the LNA design procedure with the new noise reduction technique.

For noise source implementation, by now, only flicker noise and channel thermal noise of MOSFETs are implemented in commercial circuit simulators (e.g. Spectre). The enhanced channel noise due to short-channel effects and the induced gate noise have not been implemented into any circuit simulators yet. Provided that the accurate noise models for channel noise and induced gate noise are obtained, how to use circuit simulators to verify them and further implement them into circuit simulators are the next concern. Therefore, a general noise source implementation method has been presented in detail in this thesis and is verified with measurements at the device level for both long and short-channel MOSFETs.

For a model to accurately predict the HF noise characteristics, the accuracy in the prediction of both DC and AC characteristics has to be ensured even if the accurate noise model equations have been obtained. However, due to the process variation, default parameter values from foundries have to be verified and fine tuned. A systematic

procedure to refine the model parameters used in noise calculation is presented. This procedure provides both DC and AC parameter verification and optimization for RF noise simulation purpose.

As for benchmark circuits to verify the noise models at the circuit level, two LNA designs are proposed in the thesis. The first design gives the emphasis on the noise reduction technique and the LNA design procedure. The proposed noise reduction technique gives circuit designers more control on noise figure minimization through noise matching. The second design is used to experimentally verify the noise model at the circuit level.

## 1.3 Structure of the Thesis

In order to obtain an accurate noise model, understanding noise mechanism and noise analyzing methods are important. In Chapter 2, a brief introduction of noise in MOSFETs, definition of noise parameters and noisy two-port network theory are introduced.

There are three noise sources of interest at high frequencies in an intrinsic MOSFET: channel noise, induced gate noise and their correlation. Among them, channel noise is not only dominant but also intensified by MOSFETs' down scaling. Noise models of intrinsic MOSFETs are introduced in Chapter 3 with emphasis on the small-dimensional effects on short-channel MOSFETs. A model review for the explanation of the enhanced channel noise is also given in Chapter 3.

By now, only the flicker noise and the channel thermal noise model are implemented in commercial circuit simulator (e.g. Spectre). In Chapter 4, an new effective method of implementing the enhanced channel noise and the induced gate noise is introduced and verified with experimental results.

Before verifying noise models by using compact models, accurate model parameters for both AC and DC characteristics are crucial. In Chapter 5, a systematic procedure for parameter optimization is introduced in order to obtain accurate model parameters for RF noise simulation.

With accurate model parameters and the noise models implemented in circuit simulators, Chapter 6 presents the model verification at circuit level via the design of low-noise amplifiers (LNA). The design strategies of LNAs and two LNA designs are discussed. By applying the noise models, both simulation and measurement results of the proposed LNAs are presented.

Finally, Chapter 7 will conclude the thesis and suggest future work.

## 1.4 Main Contributions of the Thesis

There are three main contributions in the thesis.

First, new noise source implementation method using two equivalent circuits for the channel noise and the induced gate noise in MOSFETs is proposed and verified with experimental results. This implementation method can be applied to any commercial circuit simulators for RF ICs design.

Second, noise source verification at device level using compact models is conducted and systematic model parameter optimization procedure is proposed. This procedure leads to accurate determination for the values of the model parameters to calculate the noise sources of interest.

Lastly, noise source verification at circuit level using low-noise amplifiers with both simulation and measurement results is conducted. The impact of noise model accuracy is also demonstrated.

# Chapter 2

# NOISE SOURCES IN SEMICONDUCTOR DEVICES AND NOISE ANALYSIS METHODS

## 2.1 Noise

What is noise? Let us look at an example.

In an ideal MOSFET transistor with proper bias conditions, it is supposed to see that the drain current should not vary with time as long as none of the terminal voltages varies with time. However, this is not what we actually get due to the existence of noise. A careful examination of the drain current shows that small fluctuations are always present no matter if external signals are applied or not. Such fluctuations are called *noise*. Fig. 2.1(a) shows a common-source biased MOSFET with fixed noiseless bias and (b) shows its drain current versus time.

Generally speaking, noise is unwanted random fluctuations in electronic circuits. In this thesis, we will concentrate on the fluctuations that are generated by the device itself, which is usually called *inherent noise*. It should be mentioned that there is another kind of noise called *interference noise* which refers to unwanted interaction between the circuit and the outside world, or between different parts of the circuit. Examples of

interference noise are atmospheric interference on radio signals and power supply noise on ground wires. However, interference noise will not be covered in this thesis.

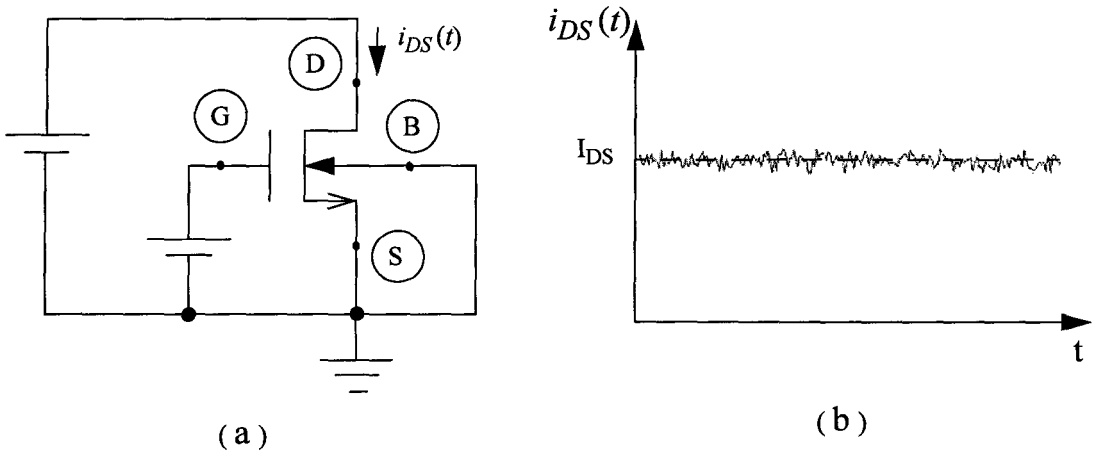



Fig. 2.1: Indication of (a) a common-source biased MOSFET and (b) its drain current versus time.

Noise is the main factor that directly limits the sensitivity of communication systems. Without noise, it would only be the matter of providing enough gain in order to receive any signal, no matter how small it is. In fact, people found that simply cascading more amplifiers eventually produces no further improvement in system sensitivity because of the existence of noise which is amplified along with the signal [11]. The facing of this problem leads to the desire of understanding and controlling noise.

H. Nyquist and J. B. Johnson are the first two persons who successfully explained the physical reasons of noise and did measurement of noise in resistors. By now, it is understood that noise origins from the random motion of carriers in solid state devices.

For example, the collision among the carriers and between the carriers and the atoms of the solid body cause the continuos changing of the direction and the speed of the carriers which results the fluctuation in current.

Since noise is random with time in nature, it is often analyzed in frequency domain. One of the most powerful methods of analyzing fluctuation quantities is by using Wiener-Khinchin theorem which is the Fourier transform of the autocorrelation function of a time-domain signal. This method describes a fluctuation quantity $X(t)$ in terms of its spectral density $S_x(f)$. We know that periodic signals (such as a sinusoid) have power at distinct frequency locations while random signals have their power spread out over the frequency spectrum. Thus, noise voltage spectral density $V_n^2(f)$ is defined as the average normalized noise power over a 1-Hz bandwidth with the unit of $V^2/Hz$. Similarly, noise current spectral density $I_n^2(f)$ can be defined with the unit of $A^2/Hz$. The measurement of noise power spectral density is carried out by using a spectrum analyzer to measure the mean-squared value over each 1-Hz bandwidth within the specified frequency range. Notice that it is also convenient to express noise spectral density in its square root value with the unit of $V/\sqrt{Hz}$ for voltage and $A/\sqrt{Hz}$ for current.

Since spectral density measures the mean-squared value over a 1-Hz bandwidth, the total mean-squared value can be obtained by integrating the spectral density over the entire frequency range. Thus, the rms value of a noise signal can be obtained in frequency domain by

$$V_{n(rms)}^2 = \int_0^\infty V_n^2(f)df \tag{2.1}$$

for noise voltage, and

$$I_{n(rms)}^2 = \int_0^\infty I_n^2(f)df \tag{2.2}$$

for noise current. The advantage of these relationships is that we can always express a noisy device as a noiseless device serial with a voltage source with the corresponding root-mean-squared noise voltage or express it as a noiseless device parallel with a current with the corresponding root-mean-squared noise current. This makes it possible to analyze circuit noise performance with the help of ac circuit theories.

## 2.2 Noise Sources in Semiconductor Devices

There are four major noise sources in semiconductor devices, which are flicker noise, thermal noise, shot noise and generation-recombination (GR) noise, respectively. Among them, flicker noise, GR noise and thermal noise are the major noise sources in MOSFETs.

Fig. 2.2 shows a typical plot of spectral density of the drain current noise in a MOSFET. It has two distinct frequency regions with different noise behaviors. The two regions are separated by the *corner frequency* $f_c$, whose value is about several MHz. The noise dominating at high frequencies is called *thermal noise* and the noise dominating at low frequencies is called *flicker noise.*

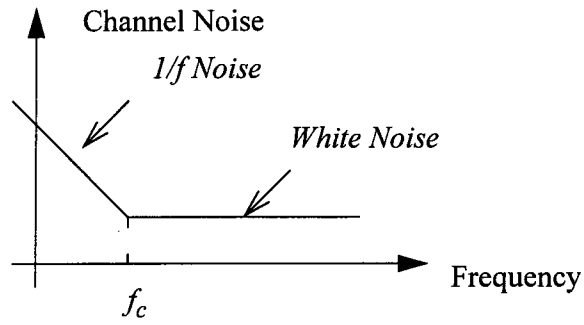



Fig. 2.2: A typical plot of drain-noise current spectral density versus frequency.

### 2.2.1 Flicker Noise (1/*f* Noise)

Flicker noise was first observed in vacuum tubes about eighty years ago. Since its frequency dependency is $1/f^n$ with $n$ close to unity, flicker noise is often called *1/f noise*. So far, many theories have been proposed to explain the physical origin of $1/f$ noise in MOSFETs, which can be categorized in three major types.

***A. Carrier Number Fluctuation Theory***

This theory was first proposed by McWhorter [12]. It was found that $1/f$ noise is due to the random fluctuation of the number of carriers in the channel, which is caused by the trapping and de-trapping of charge carriers in traps located in the gate oxide. These traps are due to the defects located near the Si - $SiO_2$ interface. According to this theory, the power spectral density of the equivalent input noise voltage can be expressed as [12]

$$V_n^2(f) = \frac{K_1}{WLC'^2_{ox}f}, \tag{2.3}$$

where $W$ and $L$ are transistor's width and length respectively, $C'_{ox}$ is gate capacitance per unit area, and $K_1$ is a bias independent constant which depends on fabrication processing. Cleaner fabrication processing can result lower $K_1$ value. Usually, for n-channel devices, $K_1$ is typically between $5 \times 10^{-31}$ and $1 \times 10^{-30}$ $C^2 \cdot cm^{-2}$ [10].

### *B. Mobility Fluctuation Theory*

This theory, also called Hooge model [13], states that $1/f$ noise is due to bulk mobility fluctuations caused by phonon scattering. Based on this theory, the power spectral density of the equivalent input noise voltage can be expressed as [13]

$$V_n^2(f) = \frac{K(V_{GS})}{WLC_{ox}'f} \tag{2.4}$$

where $K(V_{GS})$ is a bias dependent constant. It is found that, for p-channel devices, the typical value of $K(V_{GS})$ is between $6 \times 10^{-26}$ and $2 \times 10^{-23}$ $V^2 \cdot F$ at $| V_{GS} - V_T |$ of about 1V [10].

### *C. Unified 1/f Noise Model*

This model ([14] and [15]) managed to describe the measured $1/f$ noise characteristics for both n- and p- channel devices using a single model. The main idea of it is that when charges are trapped, they cause correlated surface mobility fluctuations in the trapped charges in the inversion layer due to Coulomb scattering. The unified $1/f$ noise model is adopted in many of today's compact MOSFET models, such as BSIM3v3 model [26].

Although it is supposed that $1/f$ noise is due to both effects (i.e. carrier number fluctuation effect and mobility fluctuation effect), one effect may dominate at a time. For example, carrier number fluctuation effect is found to be dominated in n-channel devices while mobility fluctuation effect is believed to be dominated in p-channel devices.

It is important to notice that $1/f$ noise is inversely proportional to the transistor's area $WL$, i.e., larger devices have less $1/f$ noise. Also, p-channel device is quieter than their n-channel counterparts because it is found that holes are less likely to be trapped.

It should be mentioned that although $1/f$ noise dominates in the low frequency range, it also has serious impact on RF CMOS circuits due to up-conversion. After up-conversion, $1/f$ noise causes a significant increase of the phase noise in VCO [11]. Therefore, a good $1/f$ noise model is also important for CMOS based RF circuit simulators.

### 2.2.2 Thermal Noise

Thermal noise origins from the random motion of carriers in a solid state device. The collisions among the carriers and between the carriers and the atoms cause the continuous changing of the direction and the speed of the carriers which results the fluctuation of the current.

An important theory called Nyquist's theorem showed that the available noise power of a thermal noise source at the absolute temperature $T$ in a frequency interval $\Delta f$ is a universal function of $T$ and can be expressed as [19]

$$P_{av} = kT\Delta f \tag{2.5}$$

where $k$ is Boltzmann's constant (about $1.38\times10^{-23}$J/K). This equation implies that the maximum power that can be delivered from a thermal noise source to a load is constant over any given bandwidth at a given temperature. For example, at room temperature, the thermal noise power per hertz is about 4 x $10^{-21}$ W (or -174 dBm). Since this noise power is constant throughout the frequency spectrum, thermal noise is often called "*white noise*". Equation (2.5) also implies that the total noise power is the integration over the whole frequency range which in practice depends on the passband of the circuit or the bandwidth of the measurement system.

Resistors generate thermal noise. In general, the spectral density of a short-ciruited thermal noise current generated by a resistor $R$ can be expressed by [19]

$$S_{I,T} = 4\cdot\left(\frac{1}{2}hf + \frac{hf}{\exp(hf/kT)-1}\right)/R, \tag{2.6}$$

where $h$ is Planck's constant, $k$ is Boltzmann's constant, $T$ is the absolute lattice temperature, and $f$ is the frequency. For $hf/kT \ll 1$, $S_{I,T}$ can be reduced to the widely used expression [19]

$$S_{I,T} = 4kT/R. \tag{2.7}$$

Based on (2.7), the mean-square open-circuit thermal noise voltage of a resistor can be expressed by [19]

$$\overline{v_n^2} = 4kTR\Delta f \tag{2.8}$$

and the corresponding mean-square short-circuit thermal noise current can be expressed by [19]

$$\overline{i_n^2} = \frac{4kT\Delta f}{R}. \tag{2.9}$$

Therefore, in circuit level noise analysis, any physical resistor can be expressed as a noise voltage source in series with the resistor according to Thevenin representation (Fig. 2.3 (a)) or a noise current source in parallel with it according to Norton representation (Fig. 2.3 (b)). The values of the voltage source and the current source are given by equations (2.8) and (2.9).

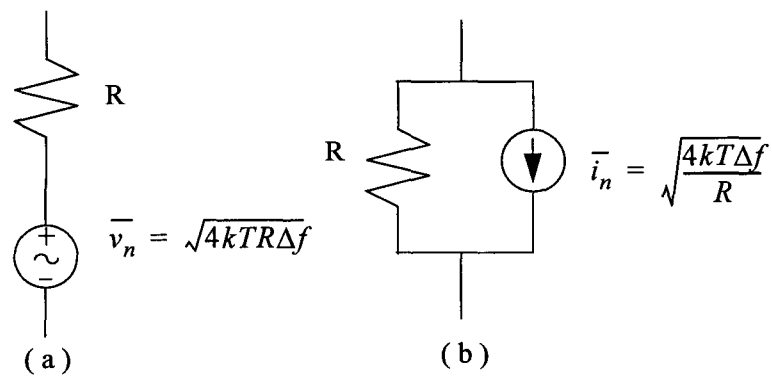



Fig. 2.3: Resistor's thermal noise models.

It is important to know that reactions do not generate thermal noise. Therefore, ideal capacitors and ideal inductors are noiseless. However, real capacitors and real inductors always contribute thermal noise due to the parasitic resistance.

Thermal noise in MOSFETs is due to the resistive inverted channel. When the drain-source voltage is close to zero, the inversion charge density can be regarded as constant along the entire channel. Therefore, the thermal noise current in the drain due to the channel resistance can be given by $\overline{i_d^2} = 4kTg_{d0}\Delta f$, where $g_{d0}$ is the output conductance for zero drain-source bias. However, since the channel cannot be considered homogeneous when drain-source voltage is increased, the total channel thermal noise should be obtained by integrating over small pieces of the channel which results in the channel thermal noise current being given by [19]

$$\overline{i_d^2} = \gamma 4kTg_{d0}\Delta f \tag{2.10}$$

with the value of $\gamma$ changing from unity in triode region toward the value of 2/3 in saturation region. This noise source is often modeled by a current source connected between the drain and the source terminals of a MOSFET.

Thermal noise of deep-submicron MOSFETs has received considerable attention since a severe enhancement of thermal noise compared with long-channel devices is reported in publications [5][7][33]. In this case, it will seriously limit the viability of deep-submicron MOSFETs in RF applications. Therefore a detailed study is urgent and this discussion will be given in Chapter 3.

### 2.2.3 Shot Noise

Shot noise is generated when carriers surmount energy barriers such as a p-n junction. This causes statistical variations in the number of electrons in the electrical current flow. Since the electrons arrive at the terminal individually and discretely at random time, the so called *shot noise* is detected at the terminal.

The double-sided band power spectral density of the shot noise current can be expressed as $qI_{DC}$, where $I_{DC}$ is the dc current flowing across the junction and $q$ is the electronic charge ($1.602 \times 10^{-19}$C). The usual expression for shot noise in single-sided power spectral density form is [19]

$$S_{ib} = 2qI_{DC}. \tag{2.11}$$

It can be seen that the frequency dependency of shot noise is like that of thermal noise which is constant in frequency domain. So shot noise is also "white".

From its physical origin, it is known that in order to generate shot noise, two conditions must be satisfied. One is the existing of a potential barrier; the other is that there is dc current flowing through the barrier. So shot noise is usually found in non-linear devices such as diodes and bipolar junction transistors.

When MOSFETs work in subthreshold, the white noise current spectre density reduces to $2qI_{DS}$, which is shot noise [10]. So MOSFETs exhibit shot noise instead of thermal noise when working in subthreshold.

Gate leakage current ($I_G$) in MOSFETs due to the direct tunneling is also shot noise. Although gate shot noise (GSN) is usually neglected in MOSFET analog and RF models [4], it is declared that for ultrathin gate oxides (e.g. $t_{ox}$ is less than 1nm), gate shot noise significantly affects the noise performance of MOSFETs at RF and it may dominate over thermal noise at $I_G$ levels above a threshold value [17].

Besides gate shot noise, there are two other shot noise sources which are related with MOSFETs' substrate. One is due to the impact ionization current, and the other is due to the body-source diode current. Impact ionization current exhibits shot noise because only those carriers obtain sufficient kinetic energy can generate electron-hole pairs. For the body-source current, carriers have to overcome the build-in potential barrier of the body-source diode. It is claimed that the above shot noise causes fluctuation in body potential and threshold voltage, and will consequently leads to excess low-frequency noise in drain current [18].

### 2.2.4 Generation-Recombination (GR) Noise

There are two main components in MOSFET low-frequency noise: interfacial *1/f* noise and bulk GR noise. In contrast to flicker noise caused by traps due to the defects in the oxide, GR noise is caused by the traps due to bulk silicon defects, spatically situated in the MOSFET's depletion region (Fig. 2.4) [20]. The GR noise is very weak compared with the $1/f$ noise, therefore it is usually overshadowed by $1/f$ noise.

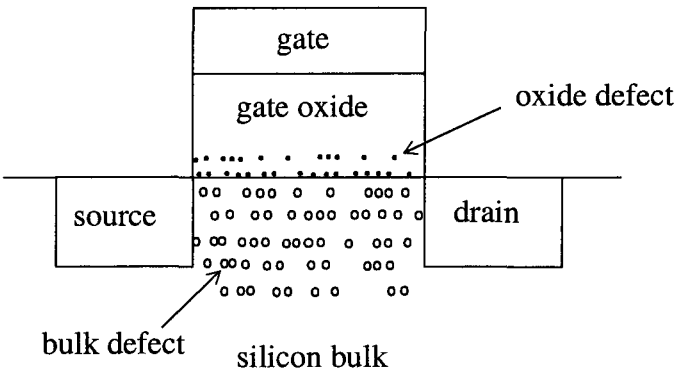



Fig. 2.4: Low-frequency noise sources in MOSFETs: defects in the oxide and the bulk.

The power spectral density of G-R noise is given by [19]

$$S_n(f) = \Delta N^2 \cdot \frac{4\tau}{1 + (2\pi f\tau)^2}, \tag{2.12}$$

where $\Delta N^2$ is the variance of the number of free carriers per unit time and $\tau$ is the lifetime of the carriers. In experiment, GR noise can be easily distinguished from $1/f$ noise in frequency domain since the power spectral density of GR noise shows a Lorentzian shape with a plateau and a steep with $1/f^2$ frequency dependent (Fig. 2.5). GR noise causes fluctuation in the number of carriers, and thus fluctuation in the bulk conductance.

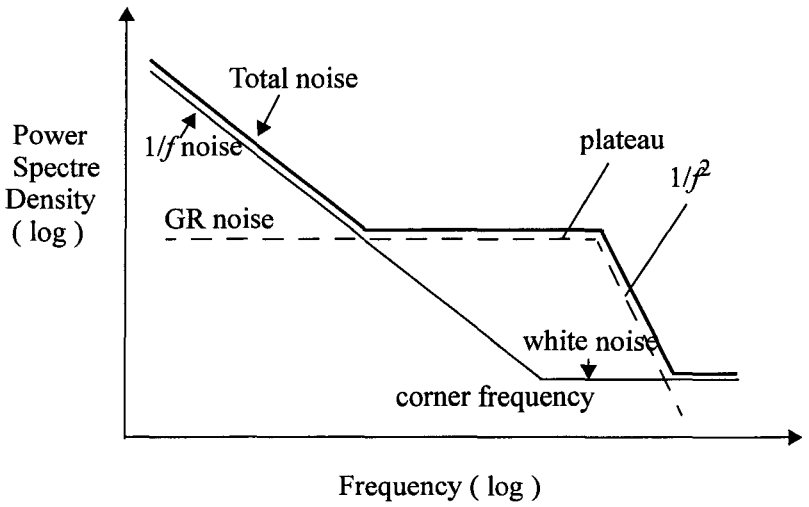



Fig. 2.5: Main low-frequency noise components in MOSFETs.

## 2.3 HF Noise Modeling of MOSFETs

In order to accurately predict noise performance of MOSFETs working at high frequencies, an accurate high frequency noise modeling of MOSFETs is important for circuit simulation. However, when investigating RF noise, an accurate RF MOSFET equivalent circuit is essential.

Compared with MOSFETs working at low frequency, some important features must be added into the MOSFET equivalent circuit when working at RF. These addition features should include at least following three effects [54][68][56]. First, terminal resistance should be included into the equivalent circuit especially the gate resistance due to the distributed gate resistance effect at high frequencies. Second, substrate network should be included into the equivalent circuit. This is due to the signal coupling through

the substrate at high frequencies. Third, the Non-Quasi-Static (NQS) effect should be included in the RF model due to the distributed channel at high frequencies.

Although it is possible to obtain a very detailed equivalent circuit with all the physical effects being taken into account, it is usually too complex and very time consuming. Further more, there are some physical values that are difficult to be extracted. Therefore, trade-off need to be made between model accuracy and model efficiency. Fig. 2.6 shows an practical equivalent circuit of MOSFETs with all the noise sources for RF applications.

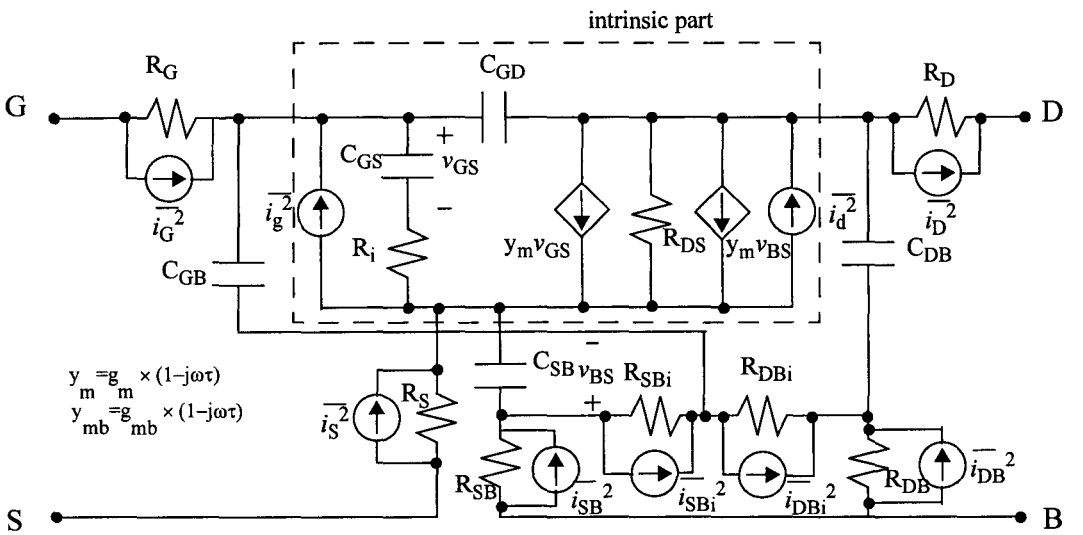



Fig. 2.6: Equivalent circuit of high-frequency MOSFETs with noise sources included.

In Fig. 2.6, for the intrinsic part, $C_{GS}$ and $C_{GD}$ are the gate-source capacitance and gate-drain capacitance, respectively. They both include the intrinsic and the overlap

capacitances. $\overline{i_d^2}$ is the channel thermal noise. $R_i$ is the channel resistance and its corresponding noise is represented by induced gate noise $\overline{i_g^2}$. $\overline{i_d^2}$ and $\overline{i_g^2}$ are correlated. These are the two noise sources of interest. Resistor $R_{DS}$ is the output resistance. It is used to model the channel length modulation (CLM) effect of the transistor. Since it is not a physical resistor, it dose not generate thermal noise in the equivalent circuit. The terms $y_m v_{GS}$ and $y_{mb} v_{BS}$ are the two voltage controlled current sources used to model the small-signal drain current and the body effect, with NQS effect taken into account by using the time constant $\tau$ to model the transcapacitance [10]. The terms $g_m$ and $g_{mb}$ are the transconductance and the bulk transconductance, respectively. For the extrinsic part, $C_{GB}$ is the gate-bulk capacitance. $R_S$ and $R_D$ are the source and drain parasitic resistance. $R_G$ is the poly silicon gate resistance. Capacitances $C_{SB}$ and $C_{DB}$ and resistances $R_{SB}$, $R_{DB}$, $R_{SBi}$ and $R_{DBi}$ are used to model the substrate network. Among them, $C_{SB}$ and $C_{DB}$ are source-substrate and drain-substrate junction capacitances, $R_{SB}$ and $R_{DB}$ are the source-bulk and drain-bulk resistance, and $R_{SBi}$ and $R_{DBi}$ are the resistance between source and intrinsic substrate and the resistance between drain and intrinsic substrate, respectively. $\overline{i_S^2}$, $\overline{i_D^2}$, $\overline{i_G^2}$, $\overline{i_{SB}^2}$, $\overline{i_{DB}^2}$, $\overline{i_{SBi}^2}$ and $\overline{i_{DBi}^2}$ are the thermal noise sources associated with resistances $R_S$, $R_D$, $R_G$, $R_{SB}$, $R_{DB}$, $R_{SBi}$ and $R_{DBi}$, respectively, and their values are know ($4kT/R$) as long as their resistance values ($R$) are determined. All the resistances and capacitances values are bias dependent and can be obtained from dc and ac measurements.

Another way to do noise simulation is by using commercial circuit simulators. The general method adopted by the circuit simulators is using compact MOSFET model (such as BSIM3v3 model) as the core (intrinsic MOSFET) and adding a subcircuit for RF applications. Fig. 2.7 shows a noise equivalent circuit of a MOSFET. The intrinsic MOSFET uses BSIM3v3 model as the core. The subcircuit includes terminal resistances ($R_D$, $R_G$ and $R_S$) and the substrate network ($D_D$, $D_S$, $R_{DB}$, $R_{SB}$ and $R_{DSB}$). Since the channel noise models in circuit simulators are not adequate and induced gate noise is not included in circuit simulators, two additional noise sources, which are enhanced channel noise and induced gate noise need to be added to the circuit with accurate noise models to calculate the noise values. This will be discussed in Chapter 4.

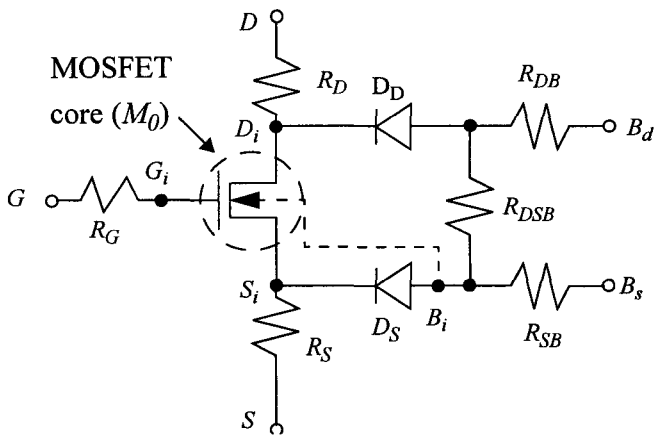



Fig. 2.7: Noise equivalent circuit of a MOSFET including the MOSFET core ($M_0$), parasitic resistance ($R_D$, $R_G$ and $R_S$) and substrate network ($D_D$, $D_S$, $R_{DB}$, $R_{SB}$ and $R_{DSB}$) for RF IC applications.

## 2.4 Two-port Noise Theory and Four Noise Parameters

After an accurate equivalent circuit is obtained, how to evaluate noise performance of the circuit becomes another issue. Noise performance is usually evaluated by noise figure and it is accomplished by the aid of two-port noise theory.

### 2.4.1 Noise Figure and Noise Parameters

Noise figure is the widely used parameter to evaluate noise performance of a noisy two- port network. It is defined as the ratio of input signal-to-noise ratio and output signal-to-noise ratio of a two-port network. For a two-port network with source impedance $Z_S$ ($Z_S = R_S + jX_S$), load impedance $Z_L$ and $T_0$ is 290K. If the noise voltage related with the source is given by $4kT_0R_S$, the power of the input signal is $S_{in}$, the gain of the device-under-test (DUT) is $G_a$ and noise power generated by the DUT is $N_{DUT}$, from the noise power point of view, noise figure of the system can be expressed as

$$NF = \frac{\frac{S_{in}}{4kT_0R_S}}{\frac{G_a \cdot S_{in}}{G_a \cdot 4kT_0R_S + N_{DUT}}} = \frac{(G_a \cdot 4kT_0R_S + N_{DUT})/G_a}{4kT_0R_S} \tag{2.13}$$

From equation (2.13), we can see that noise figure can also be defined as the ratio of the total noise power referred to the input port and the noise power generated by the source only. Noise figure is often expressed in decibels and it is always greater than $0dB$.

The noise figure expression of a two-port network with arbitrary source impedance is derived in [23] [24] and is given by

$$NF = NF_{min} + \frac{R_n}{G_s} \cdot |Y_S - Y_{opt}|^2 \tag{2.14}$$

where the following definitions apply:

$Y_S$: source admittance presented to the input of the two-port;

$Y_{opt}$: optimum source admittance that results in minimum noise figure;

$NF_{min}$: minimum noise figure of the DUT, obtained when $Y_S = Y_{opt}$;

$R_n$: equivalent noise resistance of the DUT;

$G_S$: source conductance.

When working in microwave region, the reflection coefficient $\Gamma_s$ and $\Gamma_{opt}$ are often used instead of the admittances $Y_S$ and $Y_{opt}$, where

$$Y_S = \frac{1}{Z_0} \cdot \frac{1 - \Gamma_S}{1 + \Gamma_S} \tag{2.15}$$

$$Y_{opt} = \frac{1}{Z_0} \cdot \frac{1 - \Gamma_{opt}}{1 + \Gamma_{opt}} \tag{2.16}$$

Apply (2.15) and (2.16) to (2.14), noise figure can be expressed in terms of $\Gamma_S$ and $\Gamma_{opt}$:

$$NF = NF_{min} + \frac{4R_n|\Gamma_S - \Gamma_{opt}|^2}{(1 - |\Gamma_S|^2) \cdot |1 + \Gamma_{opt}|^2} \tag{2.17}$$

where $\Gamma_S = \frac{R_S + jX_S - Z_0}{R_S + jX_S + Z_0}$. Equation (2.17) shows more details of the composition of noise figure and gives design insights. In the equation, the quantities $NF_{min}$, $\Gamma_{opt}$ and $R_n$ are characteristics of the device-under-test (DUT) and are called the noise parameters of the device. They can be obtained from the measured S-parameters by using the theory introduced in section 2.4.2. From equation (2.17), we can see that noise figure of a two-port network is contributed by two sources. One is by the DUT itself, which, when carefully designed, will generate $NF_{min}$. The other is by mismatch between the optimized source reflection coefficient ($\Gamma_{opt}$) and the source reflection coefficient ($\Gamma_s$), which, when perfectly designed, will contribute no noise. However, perfect match is hardly to obtain in real design. In this case, any deviation from perfect match will be accelerated by the factor of $R_n$ and contributes to the total noise figure.

### 2.4.2 Noise Theory of Two-ports

A noisy two-port may be represented by a noise-free two-port with two noise current sources connected at the input port and the output port as shown in Fig. 2.8(a). The two noise sources are usually correlated. By using y-parameters of the two port, Fig. 2.8(a) can be transformed into the form shown in Fig. 2.8(b) which has a serial noise voltage source and a shut noise current source both connected at the input port of the noise-free two-port. Thus, we have following relationships for $u$, $i$ and the correlation factor $Y_{cor}$ [21]

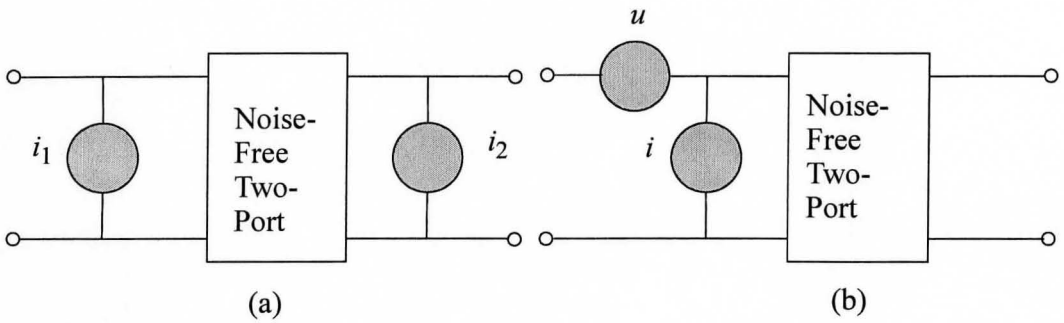



Fig. 2.8: Different representations of noisy two-port networks.

$$i = i_{un} + uY_{cor} \tag{2.18}$$

and

$$\overline{iu^*} = Y_{cor}\overline{|u|^2}, \tag{2.19}$$

where

$$u = -\frac{1}{Y_{21}} i_2, \tag{2.20}$$

$$i = i_1 - \frac{Y_{11}}{Y_{21}} i_2, \tag{2.21}$$

$$Y_{cor} = Y_{11} - Y_{21}\frac{\overline{i_1 i_2^*}}{\overline{|i_2|^2}} = G_{cor} + jB_{cor}, \tag{2.22}$$

and the mean-square values for $u$ and $i$ are given by

$$\overline{|u|^2} = \frac{\overline{|i_2|^2}}{\overline{|Y_{21}|^2}} = 4kT\Delta f R_u \tag{2.23}$$

and

$$\overline{|i|^2} = \overline{|i_1|^2} + \overline{|i|_2^2} \cdot \left|\frac{Y_{11}}{Y_{21}}\right|^2 - 2Re\left\{\overline{i_1 i_2^*} \cdot \frac{Y_{11}^*}{Y_{21}^*}\right\} = 4kT\Delta f G_i . \tag{2.24}$$

From equations (2.22) - (2.24), the four noise parameters can be obtained by [21]

$$R_n = R_u , \tag{2.25}$$

$$G_{opt} = \sqrt{\frac{G_i}{R_n} - B_{cor}^2} , \tag{2.26}$$

$$B_{opt} = -B_{cor} \tag{2.27}$$

and

$$NF_{min} = 1 + 2R_n(G_{cor} + G_{opt}) . \tag{2.28}$$

In order to take the advantage of computer simulation, the generalized matrix approach [21] is developed for the noise analysis of two-port networks. In this approach, the admittance node equations at input port and output port are expressed as

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} B \\ D \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} , \tag{2.29}$$

where B = [1 0] and D=[0 1] according to the noise network shown in fig. 2.8(b). The noise correlation matrix C for a two-port network can be defined as

$$C = \begin{bmatrix} \overline{i_1 i_1^*} & \overline{i_1 i_2^*} \\ \overline{i_2 i_1^*} & \overline{i_2 i_2^*} \end{bmatrix}. \tag{2.30}$$

By applying y-parameters and the B, C, D matrixes defined in equation (2.29) and (2.30), the generalized matrix calculation for $R_u$, $G_i$ and $Y_{cor}$ are given by [21]

$$R_u = \frac{1}{4kT\Delta f} Re\left\{ \frac{1}{|Y_{21}|^2} \times [D]^* \times [C] \times [D]^T \right\}, \tag{2.31}$$

$$G_i = \frac{1}{4kT\Delta f} Re\left\{ \left( [B] - \frac{Y_{11}}{Y_{21}} \times [D] \right)^* \times [C] \times \left( [B] - \frac{Y_{11}}{Y_{21}} \times [D] \right)^T \right\} \tag{2.32}$$

and

$$Y_{cor} = G_{cor} + jB_{cor} = \frac{-1}{4kT\Delta f R_n Y_{21}^*} \left\{ [D]^* \times [C] \times \left( [B] - \frac{Y_{11}}{Y_{21}} \times [D] \right)^T \right\}. \tag{2.33}$$

By applying equations (2.31) - (2.33) to equations (2.25) - (2.28), the four noise parameters $NF_{min}$, $G_{opt}$, $B_{opt}$ and $R_n$ can be obtained. This generalized matrix approach can be applied to noise analysis of arbitrary topologies as long as the two ports are defined.

# Chapter 3

# NOISE MODELS OF MOSFETs

## 3.1 Conventional Noise Models of MOSFETs

There are three noise sources in intrinsic MOSFETs that are of interest at high frequencies. They are channel noise, induced gate noise and the correlation between channel noise and induced gate noise. Conventional noise models of these three noise sources are based on the models proposed by van der Ziel [19]. These noise models are adequate in predicting noise performance of long channel devices working in triode region, but are found to be not accurate for short channel devices working in saturation region.

### 3.1.1 Channel Noise

In a MOSFET, when the gate voltage is properly biased, an inversion charge layer is induced under the oxide between the source and the drain terminal. Thus, a MOSFET can be regarded as a voltage-controlled resistor with the channel conductance being controlled by the gate voltage.

Channel thermal noise generated by the MOSFET channel resistance can be modeled by [19]

$$\overline{i_d^2} = \gamma 4kTg_{d0}\Delta f \tag{3.1}$$

where $T$ is the device temperature in Kelvin, $k$ is Boltzman's constant ($1.38\times10^{-23}$ J/K), $g_{d0}$ is the channel conductance with zero drain-to-source voltage. Parameter $\gamma$ is called excess noise factor which is a bias dependent factor. For long-channel devices, it has a value of unity in triode region and it decreases toward the value of 2/3 ($\gamma_{sat}$) in saturation region.

This channel noise model works well for long-channel devices, but for short channel devices, it is not adequate especially when the short-channel devices work in saturation region which is the case for RF applications.

### 3.1.2 Induced Gate Noise

At high frequencies, the MOSFET channel should be considered as "an RC distributed network, with the capacitive coupling to the gate representing the distributed capacitance and the channel itself representing the distributed resistance" [19]. In this case, since the high frequency gate admittance of a MOSFET contains a conductive component, any potential fluctuation in the channel will be coupled to the gate. This coupling leads to noise current at gate terminal which is called *induced gate noise*. It is negligible at low frequencies but can be dominate at RF.

Induced gate noise current model can be expressed as [19]

$$\overline{i_g^2} = \beta 4kTg_g\Delta f \tag{3.2}$$

where $g_g = \frac{\omega^2 C_g^2}{5g_{d0}}$ is the real part of the gate admittance, $C_g$ is gate-channel capacitance and $\beta$ is a constant which is 4/3 for long-channel devices. Notice that induced gate noise is proportional to frequency square.

In saturation region, $C_g = \frac{2}{3} \cdot C_{ox}WL$. Substituting it into (3.2), we will obtain [19]

$$\overline{i_g^2} = \delta_{sat} 4kT\Delta f \frac{\omega^2 (C_{ox}WL)^2}{g_{d0}} \tag{3.3}$$

where $\delta_{sat}$=4/135 for long-channel devices.

### 3.1.3 Correlation Noise

Since the physical origin of the induced gate noise and the channel thermal noise are the same, these two noise sources are correlated. The noise spectral density of correlation noise from a small section $\Delta x_0$ is defined as $\overline{\Delta i_g(x_0)\Delta i_d(x_0)^*}$ and the total correlation noise can be obtained by integrating over the channel length. For long channel devices, correlation noise can be modeled as [19]

$$\overline{i_g i_d^*} = \frac{1}{6} j\omega C_g 4kT\Delta f. \tag{3.4}$$

In saturation, $C_g = \frac{2}{3} \cdot C_{ox}WL$, we have [19]

$$\overline{i_g i_d^*} = \varepsilon_{sat} 4kTj\omega(C_{ox}WL)\Delta f \tag{3.5}$$

where $\varepsilon_{sat} = 1/9$ for long-channel devices.

A correlation factor is defined as $c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g i_g^*} \cdot \overline{i_d i_d^*}}}$. By applying (3.1), (3.2) and (3.5), the cross correlation coefficient ($c$) is 0.395j for long channel devices.

## 3.2 Small-dimensional Effects for Short-channel MOSFETs

The conventional MOSFET noise models described in previous sections are valid for long channel devices. Short-channel MOSFETs are found more noisy than long-channel ones. The reason why conventional models fail to predict the enhanced noise for short-channel MOSFETs is because they do not take into account the short-channel effects of MOSFETs such as channel length modulation effect, velocity saturation effect and hot carrier effect.

### 3.2.1 Mobility Variation

In a real MOSFET model, mobility of carriers in the inversion layer can not be treated as a constant. This is because of several scattering mechanisms experienced by the carriers as they travel along the channel. When the scattering happens, traveling carriers will exchange momentum and kinetic energy with their environment. As the result, carriers' mobility is changed.

The scattering mechanisms inside a MOSFET can be divided into two catalogues. One is called phonon scattering, which is due to the interaction between carriers and the vibrated lattice. The other is called Coulomb scattering, which is mainly related with ionized impurity atoms. When carriers flow through the channel, a vertical electric field caused by the gate voltage produces a force on them toward the oxide surface. However, due to coulomb forces from the ionized impurity atoms, the interface trapped charges, the oxide trapped charges and also from the surface roughness, the carriers are repelled back [10].

All these scatting effects happen simultaneously, tending to limit the carriers' mobility. Although the actual carrier mobility (usually called *effective mobility*) is the result of all scatting effects, different effect dominates the behavior in different vertical electric field range. For example, at low field, Coulomb scattering is dominated; at high field, phonon scatting starts to dominate and at even higher field, surface roughness becomes significant. These scattering mechanisms cause mobility degradation at high gate bias voltages.

From the measured $I_{DS}$ - $V_{GS}$ characteristic, we can see the effective mobility dependence on $V_{GS}$. Fig. 3.1 shows the measured $I_{DS}$ - $V_{GS}$ of an nMOSFET at a given bias condition. If mobility $\mu$ is a constant (i.e. not a function of $V_{GS}$ bias), from equation $I_{DS} \cong (W/L)\mu C'_{ox} V_{DS}(V_{GS} - V_T)$, we expect a straight line for $I_{DS}$ vs. $V_{GS}$ which is the dash line shown in Fig. 3.1. However, due to mobility degradation, the measured result is not straight as shown in Fig. 3.1. The data shown in Fig. 3.1 is measured at a very small

$V_{DS}$ bias ($V_{DS}$ = 0.05 V). From the figure, we can see that with very small $V_{DS}$ (which means in triode region), there is a linear dependence at small $V_{GS}$, indicating that the mobility degradation is still weak. With $V_{GS}$ increasing, the curve starts to bent, indicating a strong mobility degradation.

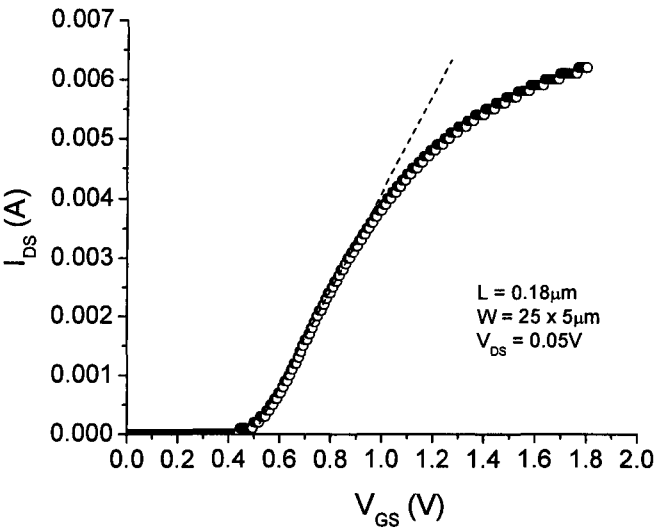



Fig. 3.1: Measured (symbols) $I_{DS}$ vs. $V_{GS}$ characteristic for the specified geometry and a very small $V_{DS}$ bias ($V_{DS}$ = 0.05 V).

In circuit simulator, the effective mobility is usually expressed in the form of [26]

$$\mu_{eff} = \frac{\mu_0}{1 + (U_a + U_c V_{BS})\left(\frac{V_{GS} + 2V_{TH}}{T_{ox}}\right) + U_b\left(\frac{V_{SB} + 2V_{TH}}{T_{ox}}\right)^2} \tag{3.6}$$

where $T_{ox}$ is the oxide thickness, $V_{TH}$ is the threshold voltage, $\mu_0$ is the effective mobility at low transverse field, $U_a$ and $U_b$ are fitting parameters used to represent first-order

mobility degradation coefficient and second-order mobility degradation coefficient, respectively due to the mobility degradation. The effective mobility is strongly temperature-dependent mainly due to lattice scattering. It increases as temperature reduced.

### 3.2.2 Velocity Saturation Effect

For short-channel devices, mobility variation in saturation region is shown as velocity saturation. In this case, phoning scattering dominates while all other scattering mechanisms are screened.

For long-channel devices with inversion layer presented, when a small $V_{DS}$ is applied, it is found that the drain current is proportional to $V_{DS}$. However, when $V_{DS}$ is increased to a certain level, this proportionality is not valid anymore and the drain current becomes saturated. This phenomena is called *velocity saturation.* The existence of velocity saturation effect indicates that when $V_{DS}$ value becomes large, the transverse field due to gate voltage loses the full control of the mobility and the effect of longitudinal field due to $V_{DS}$ bias cannot be ignored any more.

When $V_{DS}$ is small, the longitudinal field $|E_x|$ is small and the carrier velocity $|\upsilon_d|$ is proportional to $|E_x|$. However, the longitudinal electric field is generally large for short-channel devices. When the field is larger than a certain value (called *the critical electric field*), the proportional relation between velocity and lateral field is not valid. The critical electric field is defined as $|E_c|$. So

$$|v_d| \approx \mu|E_x|, \text{ where } |E_x| << |E_c|;$$

$$|v_d| \approx v_{sat}, \text{ where } |E_x| >> |E_c|.$$

A usually adopted equation which shows the dependence of $\upsilon_d$ on $E_x$ is [27]

$$v_d = \left.\frac{\mu_{eff} E_x}{1 + \frac{E_x}{E_c}}\right|_{|E_x| < |E_c|} \tag{3.7a}$$

and

$$v_d = v_{sat}\Big|_{|E_x| \geq |E_c|} \tag{3.7b}$$

where $E_c = \frac{2v_{sat}}{\mu_{eff}}$.

Velocity saturation effect becomes more significant in short-channel devices since the corresponding lateral electric field becomes larger. It will occur when the horizontal electric field is approximately $10^4$ V/cm. For example, when $V_{DS} = 5$ volts is applied to a 1μm channel length device, the average horizontal electric field will be $5\times10^4$ V/cm at which velocity saturation effect will take place. Fig. 3.2 shows $g_m$ vs. $V_{GS}$ with different $V_{DS}$ bias for a short-channel nMOSFET.

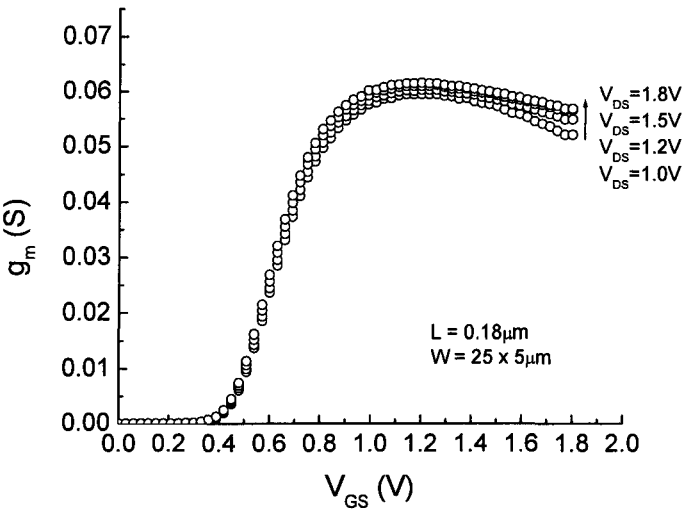



Fig. 3.2: Measured $g_m$ vs. $V_{GS}$ characteristic for the specified geometry and different $V_{DS}$ bias.

### 3.2.3 Channel Length Modulation Effect

From the measured $I_{DS}$ vs. $V_{DS}$ characteristics, it is observed that the curves have small positive slops instead of strictly parallel to the horizontal axis. These positive slops become larger for short-channel devices. This phenomenon shows the existence of channel length modulation effect.

When $V_{DS}$ increases to the value that the potential dropping across the oxide at the drain terminal equals threshold voltage ($V_T$), the inversion charge density at the drain end becomes zero which causes the pinchoff of the conducting channel. If $V_{DS}$ is further increased, the widen depletion region at the drain terminal pushes the pinchoff point moving toward the source terminal. The phenomenon causes the shrinking of the

inversion charge layer is call *channel length modulation.* Thus, the MOSFET's channel can be regarded as two distinct sections: one is from the source-end to the pinch off point; the other is from the pinch off point to the drain-end. By using this model, in order to obtain the effective channel length ($L_{eff}$), the length from pinch off point to the drain-end need to be obtained by calculating the width of the depletion region.

Another method to obtain the effective channel length ($L_{eff}$) is by using the velocity saturation theory. In this approach, it is assumed that when the field near the drain becomes high enough, it causes velocity saturation. When drain voltage becomes higher, the electrons will travel at their maximum velocity starting from the critical electric field point ($E_c$). Therefore, the whole channel can be divided into two regions. One is called the gradual channel region which is from the source-end to the $E_c$ point; the other is called the velocity saturation region which is from the $E_c$ point to the drain-end. Fig. 3.3 shows the schematic of the two-region channel which is consisted of the a gradual channel region (I) and a velocity saturation region (II).

When dividing the channel into gradual channel region and velocity saturation region in the long-channel transistor, it is assumed that the pinchoff point and the critical electric field point ($E_c$) happen at the same place. However, for short-channel devices, there is a portion of the channel before pinchoff where the carrier velocity saturation has already happened [10].

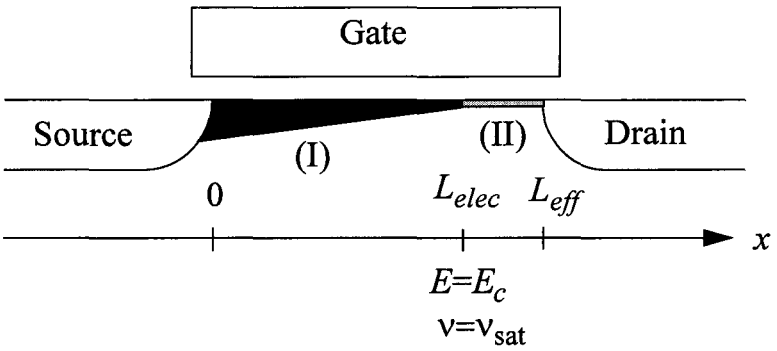



Fig. 3.3: Schematic of two-section channel model which consists of a gradual channel region (I) and a velocity saturation region (II).

Channel length modulation does not only happen in short-channel devices. In long-channel devices, channel length modulation also happens when working in saturation region. However, as MOSFETs scale down, the width of the depletion region near the source terminal (length of region II in Fig. 3.3) becomes a large fraction of the total channel length. Therefore, short-channel devices have sever CLM effect than long-channel devices.

### 3.2.4 Carrier Heating Effect and Hot Carriers

When carriers travel along the channel, the carrier temperature ($T_e$) will be different from the lattice temperature ($T_0$) due to the existence of the lateral electric field. For the gradual channel region in which the lateral electric field is weak, the effect of carrier heating can be modeled by a carrier effective temperature which can be expressed as [28]

$$T_e(x_0) = T_0\left(1 + \delta\left(\frac{E(x_0)}{E_c}\right)^2\right), \tag{3.8}$$

where $T_0$ is the lattice temperature, $E(x_0)$ is the longitudinal electric field at position $x_0$, and $\delta$ is a fitting parameter in the range of 5 ~ 20. When carriers travel in the gradual channel region, their effective temperature is higher than the lattice temperature, which can obtain excess channel noise using (3.8).

When carriers enter into the velocity saturation region, their velocity becomes saturated due to the collision with the lattice, but they still acquire kinetic energy from the electric field. Eventually, some portion of carriers acquired significant amount of kinetic energy that they are usually called *hot carriers*. The appearance of hot carriers indicates that the thermal equilibrium between the travelling carriers and the lattice is broken.

Will the hot carriers in the velocity saturation region cause excess channel noise? When the excess channel noise for short-channel MOSFETs was first reported by Jindal [32] and Abidi [33], many of the later literatures [5][35] including [32] and [33] attributed the excess channel noise to the hot carrier effect in the velocity saturation region. However, Chen and Deen in [9] firstly pointed out that velocity saturation region can not contribute any noise to the drain noise current because of the zero output conductance in that region. In recent publications [6][29][30][31][37][40], this theory has been addressed by many experimental and simulation works and becomes widely accepted. People now focus their attention on the gradual channel region when trying to explain the excess channel noise of deep-submicron MOSFETs.

When the hot carriers travelling through the depletion region gain even higher energy, they create impact ionization with silicon lattice atoms near the drain and generate new electron and hole pairs. This is called *weak avalanche.* For n-type MOSFETs, some of the newly generated electrons join the flow of the channel electrons, others are injected into the oxide by the force of gate voltage and generate gate current. For the newly generated holes, most of them are pushed into the substrate by the build-in electric field in the depletion region near the drain and causes drain-to-substrate current.

It should be noticed that, under the normal bias condition, weak avalanche won't happen. When drain voltage is biased within the supply voltage range, there is only a gradual increasing in channel noise current with the increasing of drain voltage, which is due to channel length modulation. Only when drain voltage is far above the supply voltage, there will be a significant raising in channel noise current, which is due to week avalanche. Since in most of the RF IC designs, transistors are operated under the supply voltage, e.g. for 0.18 μm technology, the supply voltage is 1.8 V. Under this drain voltage, weak avalanche is invisible in the drain current as well as in the channel noise current. Therefore, in this thesis, the operation region which causes weak avalanche will not be covered.

Will the carrier heating effect in the gradual channel region cause excess channel noise? In [9], equation (3.8) is adopted in the derivation of channel thermal noise and found out that carrier heating effect in the gradual channel region is negligible compared with channel length modulation (CLM) effect and can be ignored. In [29], using an approach that modulates the carrier heating and number of hot carriers by a reversed body

bias, it qualitatively confirmed a negligible role of carrier heating effect on channel thermal noise in deep-submicron MOSFETs. On the contrary, [40] and [30] confirm an un-negligible effect of carrier heating on channel thermal noise of deep-submicron MOSFETs. [40] proposed that the carrier heating effect in gradual channel region is important at high gate biases compared with that the channel length modulation effect is important at low gate biases. It is pointed out in [30] that the temperature model in (3.8) can not be used solely without a consistent field dependent mobility model which is due to the velocity saturation effect in the gradual channel region. For example, the approach in [30] adopted a pair of temperature model and field dependent mobility model which are

$$\mu_{eff} = \mu_0 \cdot \sqrt{\frac{T_0}{T_e}}, \tag{3.9}$$

and

$$\mu_{eff} = \frac{\mu_0}{1 + \frac{(dV)/(dx)}{E_c}}. \tag{3.10}$$

It is further pointed out in [30] that carrier heating and mobility reduction have opposite effect on excess channel noise. If one effect is ignored, the other effect will be over compensated by the proposed channel noise model.

## 3.3 Enhanced Channel Noise for Short-Channel MOSFETs

### 3.3.1 Tsividis' Model

The channel noise model in [10] is not specially derived for short-channel MOSFETs. It is a general channel thermal noise model for MOSFETs working in strong inversion mode. Since many short-channel MOSFET thermal noise models [5][7][34] derived latter are based on Tsividis' model and the derivation procedure of [10] is very typical, Tsividis' model is briefly introduced in this section.

The drain current flowing through a position $x_0$ within the channel of a MOSFET which works in linear region can be expressed as [10]

$$I_D(x_0) = \mu(x_0)W(-Q(x_0))E(x_0), \tag{3.11}$$

where $\mu(x_0)$ and $Q(x_0)$ are the electron mobility and the electron concentration respectively at the position $x_0$, $W$ is transistor's channel width, $E(x_0)$ is the longitudinal electric field at the position $x_0$ and it can be expressed as $E(x_0) = \frac{dV}{dx}$. Therefore, the channel resistance of the small section around $x_0$ is obtained as [10]

$$\Delta R(x_0) = \frac{\Delta V}{\Delta I_D(x_0)} = \frac{\Delta x}{\mu(x_0)W(-Q(x_0))}. \tag{3.12}$$

From the thermal noise theory for resistors, the mean square thermal noise voltage generated from $\Delta R(x_0)$ is given by [10]

$$\overline{\Delta v(x_0)^2} = 4kT\Delta R(x_0)\Delta f = \frac{4kT\Delta x\Delta f}{W\mu(x_0)(-Q(x_0))}. \quad (3.13)$$

After transforming the local mean square noise voltage into local mean square noise current and integrating along the entire channel, the corresponding power spectral density of the channel noise current is given by [10]

$$\overline{i_d^2} = 4kT\frac{\mu}{L^2}(-Q_{inv}), \quad (3.14)$$

where $\mu$ is the carrier mobility, $L$ is the transistor's channel length and $Q_{inv}$ is the total inversion charge. However, equation (3.14) can not be directly applied to short-channel devices. First, short-channel effects of MOSFETs such as velocity saturation effect and hot carrier effect should be included in the model; Second, mobility fluctuation effect should be included in the model; Third, the effective channel length should be accurately defined based on a proper channel division model.

### 3.3.2 Model Review: Enhanced Channel Noise for Short-Channel MOSFETs

Enhanced channel noise need to be considered for short-channel MOSFETs when channel length is less than 1μm [5][6][7][8][9][34][35][40]. Different theories are published to explain the reasons for the noise enhancement. The opinions of these publications can be categorized into following types:

- Hot carrier and velocity saturation explanation;
- Channel length modulation explanation.
- Impedance Field Method explanation;

In this section, we give a brief review of typical publications for each explanation.

### *A. Noise Models Based On Hot Carrier Effect*

A number of publications (e.g. [5] and [33]) have reported a considerable enhanced channel thermal noise in submicron MOSFETs, which is attributed from hot-carrier effects. In [33], a sever noise enhancement was reported for a 0.7μm n-channel MOSFET with the excess noise factor (γ) more than 10. In [5], it is reported that, if hot carrier effect is not taken into account, simulation errors will be up to 100% and it will be more for the transistor whose channel length is less than 0.25 μm.

Based on equation (3.14) and substitute mobility μ with effective mobility $\mu_{eff}$, it is pointed out that this equation is only valid for long-channel devices [5]. With the downscale of MOSFET dimensions, the increasing lateral electrical field makes the thermal equilibrium assumption questionable for channel length less than 1μm. Therefore, an equivalent noise temperature $T_e$ is used to replace the absolute temperature $T$ in (3.14).

However, in the derivation of the analytical equation for channel noise in [5], the entire channel ($L$) is treated as the source to generate thermal noise which is not correct. Moreover, the velocity saturation effect on carrier velocity has not been taken into account which is also not correct for short-channel MOSFETs.

### *B. Noise Models Based On Velocity Saturation Effect*

Some publications (e.g. [6] and [34]) reported good fitting results between simulation and measurement for channel noise of submicron MOSFETs by taken into account of velocity saturation effect only.

The noise model in [34] is also based on equation (3.14), which uses $\mu_{eff}$ as mobility and further replaces $L$ in (3.14) with $L_{elec}$, where $L_{elec}$ is given by $L_{elec} = L_{eff} - \Delta L$, $L_{eff}$ is the effective channel length between the drain and the source, and $\Delta L$ is the reduction in effective channel length due to the channel length modulation effect when $V_{DS} > V_{DSsat}$.

It is proposed that the major reason for the electrical characteristics of short channel devices deviating from those of long channel devices is the saturated velocity of carriers caused by the high lateral electric field [34]. When taking into account the high lateral electric field, the drift velocity of carriers in the channel should be expressed as (3.7). This expression for the drift velocity of carriers is adopted by [34] in calculating the inversion charge ($Q_{inv}$) of equation (3.14). Analytical equations for the drain thermal noise current of MOSFETs working both in triode region and in saturation region are derived in [34].

However, since equation (3.14) is based in the assumption that the effective mobility ($\mu_{eff}$) is independent of lateral electric field, which is acceptable for long-channel devices, it is not adequate to take into account velocity saturation effect only in calculating inversion charge ($Q_{inv}$) for short-channel noise models.

In [6], simulation results are shown by taken both hot-electron effect and velocity saturate effect into account. It is found that the best agreement between simulation and measurement is obtained when hot carrier effect is switched off in simulation. For *n*-channel devices with 0.17μm gate length, γ value is found between 1 and 2 due to velocity saturation only. However, no analytical equations for short-channel drain noise are given in [6].

### *C. Noise Models Taking Into Account Both Velocity Saturation Effect and Hot Carrier Effect*

The common short coming of the approaches in previous sections is that they all based on one-section channel model in which the channel is defined from intrinsic source to intrinsic drain (Although [34] used the $L_{elec}$ instead of the total channel length $L$, the noise mechanism of region II is not mentioned.). By this approach, the noise mechanism in the gradual channel region and in the velocity saturation region is either not clearly explained or regarded as the same. Further more, since we already know that both hot-carrier effect and velocity saturation effect have impact on noise performance of short-channel MOSFETs working in saturation region, previous noise models fail to give reasonable explanations for why only one of the effects is taken into account while the other is omitted.

On the contrary, the models in [7] and [35] adopted another approach. Both of them are based on the two-section channel model in which the channel of a MOSFET is divided into two regions which are a gradual channel region with length $L_{elec} = L_{eff} - \Delta L$

and a velocity saturation region of length $\Delta L$. When a transistor works in triode region, $L_{elec}$ becomes $L_{eff}$ naturally. The two-section channel model is shown schematically in Fig. 3.3.

Also based on (3.14), the model in [7] applied both hot-carrier effect and velocity saturation effect to the two-section channel model and obtained the analytical equation for channel noise model of short-channel MOSFETs. After implemented into circuit simulator, it is found that the hot carrier effects in region I and the thermal equilibrium noise from region II are relatively small compared to thermal equilibrium noise of region I and hot carriers contribution from region II. However, since equation (3.14) is only true in the absence of velocity saturation [10], it can not be applied to region II. This makes the noise derivation in [7] questionable in region II.

The model in [35] uses the similar approach as [7] does. However, when calculating power spectral density of local fluctuation, it uses the noise voltage of each small section as the noise sources and integrates the noise voltage spectral density along the entire channel, then multiplies the total noise voltage spectral density by $g_{ds}^2$, where $g_{ds}$ is the output conductance. This method is essentially not correct because a local noise voltage source $\Delta v(x_0)$ can be translated into a terminal fluctuation $\Delta v_{DS}$ which is only true for resistors. For MOSFETs' channel, this is not applied. The correct method should be the method introduced in section 3.3.1 which models the local fluctuation as a local current source $\Delta i(x_0)$ which is obtained by multiplying the local voltage fluctuation by the local conductance, then integrates the current spectral density along the entire channel.

### *D. Noise Models Based On Channel Length Modulation Effect*

The model in [9] uses channel length modulation effect to explain the enhanced channel thermal noise and presents an analytical equation for channel noise of deep submicron MOSFETS with measurement verification. The model is based on two important assumptions. One is that the lateral electric field for most of the sections in the gradual channel region is much less than the critical field so that the carrier local mobility in the gradual channel region is about the same as the effective mobility. The other is that the noise current generated from the velocity saturation region is zero. Based on these two assumptions, channel thermal model is derived by adopting the two section channel model with hot carrier effect being taken into account.

The second assumption is the key point to understand how channel length modulation effect explains the enhanced channel noise for short-channel MOSFETs. By now, no noise mechanism can accurately explain the channel noise contribution from region II. Suppose that there do exists certain noise mechanism and it generates a local fluctuation which causes a change of local electric field. Since the carriers in region II travel at their saturated velocity, therefore, there is no response to the local fluctuation so that the local fluctuation can not be detected at the drain terminal. However, any local fluctuation in region II may modulates the channel length in region I ($L_{elec}$). The local conductance of region I is given by [9]

$$g(x_0) = \frac{W\mu(x_0)(-Q(x_0))}{L_{elec}} \tag{3.15}$$

in which the fluctuation of $L_{elec}$ will change the local conductance of region I. So, it is proposed in [9] that "the enhancement of the delivering capability of the channel, instead of extra noise sources in region I or II by hot electron effects, is the main reason causing the enhancement of the noise current in short-channel MOSFETs".

Furthermore, in [9], it is proposed that the impact of velocity saturation on channel noise in region I is week and it can be considered as a secondary effect compared to channel length modulation effect.

### *E. Other Noise Models for the Enhanced Channel Noise*

The methods of noise analysis given so far are all based on one-dimensional analysis in which we assume that electric field lines induced by the gate voltage were perpendicular to the surface every where along the channel. This assumption is valid for long and wide devices in which the edge effects can be ignored. However, when MOSFETs' size scales down, the edge effect becomes significant. For example, when channel gets short, the component of the transverse field along the channel becomes significant. For narrow transistor width, a similar case exists. Under this condition, a two or even three dimensional analysis becomes necessary. Furthermore, when performing noise analysis using the traditional approach, e.g. the method introduced in section 3.3.1, it is assumed that the small noise voltage sources along the channel are uncorrelated. Each of them contributes noise at the drain terminal. In fact, spatial correlation exists among the voltage noise sources. To overcome these shortcomings, some publications [8][36][37] adopted another way to model the high frequency noise of short-channel MOSFETs.

In [8][36][37], to avoid the spatial correlation, local fluctuation are modeled by current noise sources instead of voltage noise sources. A method called *impedance field method* is used to calculate the noise at both drain and gate terminals. In this method, device noise at terminals is determined by two independent factors: local fluctuations and their propagation to terminals. The propagation is called *impedance field* [38][39].

By using the impedance field method, it is announced in [8] that drain noise is dominant by the contribution at the source side due to the higher local ac resistance near the source. This high local ac resistance causes the higher impedance field near the source, which, by the impedance field method, obtained enhanced drain current noise. However, the physical mechanism for the higher local ac resistance near the source is still unknown.

A recently publication in [40] claimed that the well-know equation (3.14) remains valid for short-channel devices. However, when derive (3.14), "since the mobility of carriers in short-channel MOSFETs is degraded due to the lateral electric field, the infinitesimal channel segment cannot be regarded as a linear resistor any more" [40]. In this case, equation (3.13) can not be applied, and the derivation procedure in 3.3.1 is not valid. Therefore, it adopted the impedance field method. Local fluctuation is modeled as diffusion noise sources with which carrier heating in region I was taken into account implicitly. In the mean time, velocity saturation effect was taken into account by the impedance field method itself. It also assumed that region II does not contribute drain thermal noise. After deriving with reasonable approximations, compact analytical equation for channel thermal noise valid for deep submicron MOSFET is obtained as [40]

$$\overline{i_d^2} \cong 4kT_0\Delta f\frac{\mu_{eff}}{L_{elec}^2}Q_{inv}, \tag{3.16}$$

which has the same form as equation (3.14).

From the result of [40], we may get two conclusions. First, although it is claimed in [40] that, due to mobility degradation, infinitesimal channel segment cannot be regarded as a linear resistor any more, however, the same result as (3.14) is obtained which verified that the first assumption in [9] is correct, i.e. the carrier local mobility in the gradual channel region is about the same as the effective mobility. The other conclusion is that although the motivation of using impedance field method is to avoid spatial correlation of voltage sources, however, with reasonable approximation, the impedance field method and the traditional method come to the same compact analytical equation. This indicates that the traditional method, if properly applied, can effectively predict the noise performance of deep submicron devices, and in the mean time does not lose the accuracy.

# Chapter 4

# NOISE SOURCE IMPLEMENTATION

## 4.1 Noise Models and Their Verifications

The noise models for high-frequency noise in MOSFETs adopted in this thesis are the models proposed in [9] and [48]. The detail derivations of the models are given in [48].

The drain noise model is based on the two-section channel model shown in Fig. 3.3, in which the length of the gradual channel region ($L_{elec}$) is $L_{elec} = L_{eff} - \Delta L$ and $\Delta L$ is the length of the velocity saturation region given by [9]

$$\Delta L = \frac{1}{\alpha}\ln\left[\frac{\alpha(V_{DS} - V_{DSsat}) + E_D}{E_{crit}}\right], \tag{4.1}$$

where

$$E_D = E_{crit}\sqrt{1 + \left[\frac{\alpha(V_{DS} - V_{DSsat})}{E_{crit}}\right]^2}, \tag{4.2}$$

and

$$\alpha = \lambda\sqrt{\frac{3}{2}\frac{C_{ox}}{x_j \varepsilon_{si} \varepsilon_0}}. \tag{4.3}$$

Here, $E_{crit}$ is the critical lateral electric field, $x_j$ is the junction depth for source and drain, $C_{ox}$ is the gate-oxide capacitance per unit area, and $\lambda$ is a fitting parameter to adjust the channel length modulation. The channel thermal noise from the velocity saturation region (region II in Fig. 3.3) is assumed to be negligible [9]. Thus, the drain noise model with the channel length modulation effect can be obtained by [9]

$$S_{i_d^2} = \frac{4kT_0}{L_{elec}^2}\mu_{eff}(-Q_{inv}) + \delta\frac{4kT_0 I_D}{L_{elec}^2 E_{crit}^2}V_{DSsat}, \tag{4.4}$$

where $-Q_{inv}$ is the total inversion charge in gradual channel region. When the device working in the linear region, $V_{DSsat}$ will become $V_{DS}$ and $L_{elec}$ will become $L_{eff}$.

The approach used to calculate the induced gate noise is also based on the two-section channel model. Because the induced gate noise from each section of the channel is fully correlated with the channel noise [19], and the channel noise in region II is negligible [9], the induced gate noise from region II is assumed to be negligible as well, and only the noise contribution from the graduate channel region is calculated. For the induced gate noise based on the noise model in [19] including the CLM effect through $L_{eff}$ and the drain current $I_{DS}$, its spectral densities can be obtained by [47]

$$S_{i_g^2} = \frac{4kT_0\omega^2 W_{eff}^4 C_{ox}^4 \mu_{eff}^2}{I_{DS}^3} \times \Big( V_{GT}^2 V_{as}^2 V_{DS} - V_{GT}V_{as}(V_{GT}+V_{as})V_{DS}^2 \quad , \tag{4.5}$$
$$+\frac{1}{3}(V_{GT}^2 + 4V_{GT}V_{as} + V_{as}^2)V_{DS}^3 - \frac{1}{2}(V_{GT}+V_{as})V_{DS}^4 + \frac{1}{5}V_{DS}^5\Big)$$

where

$$V_{as} = V_{DS} - \frac{\frac{1}{2}(V_{GS} - V_{TH})V_{DS} - \frac{1}{6}V_{DS}^2}{V_{GS} - V_{TH} - \frac{1}{2}V_{DS}}, \tag{4.6}$$

where $V_{GT} = V_{GS} - V_{TH}$ and $V_{DS} = V_{DSsat}$ when transistors work in the saturation region.

Both of the channel noise and the induced gate noise models are verified by the devices-under-tests (DUT) which are fabricated in a 0.18 μm CMOS technology with channel width W = 10 × 6 μm and channel lengths L = 0.18 μm, 0.42μm and 0.97μm, respectively. Fig. 4.1 [9] shows the extracted and simulated channel noise spectral density $\overline{i_d^2}$ versus $V_{GS}$ for the n-type MOSFETs with channel width W = 10 × 6 μm and channel lengths L = 0.18 μm, 0.42μm and 0.97μm, respectively based at $V_{DS}$ = 1.5 V and with δ = 0. Fig. 4.2 [47] shows the extracted and simulated induced gate noise spectral density $\overline{i_g^2}$ for the n-type MOSFETs with channel width W = 10 × 6 μm and channel lengths L = 0.18 μm, 0.42μm and 0.97μm, respectively based at $V_{DS}$ = 1.5 V. Both of the results indicate that noise models represented in (4.4) and (4.5) can accurately predict channel noise and induced gate noise of deep submicron MOSFETs.

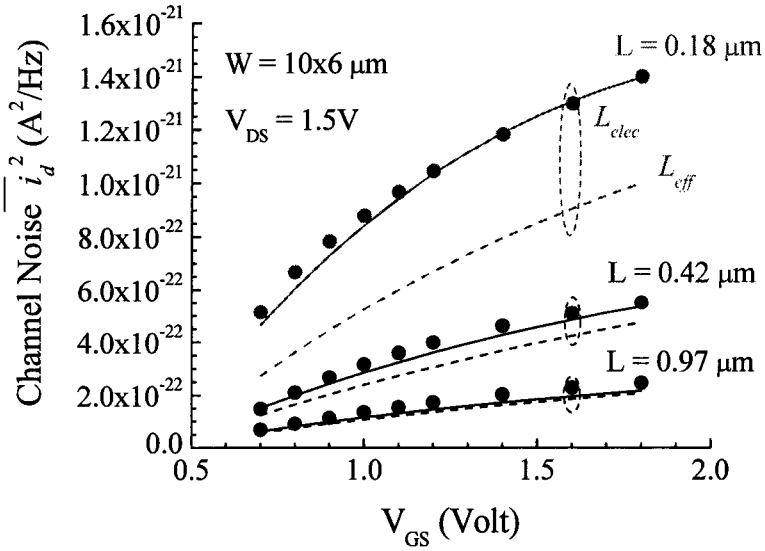



Fig. 4.1: Extracted (symbols) and simulated (lines) spectral density of the channel noise versus $V_{GS}$ characteristics of the n-type MOSFETs. The solid lines are obtained by using $L_{elec}$ and the dashed lines are obtained by using $L_{eff}$ [9].

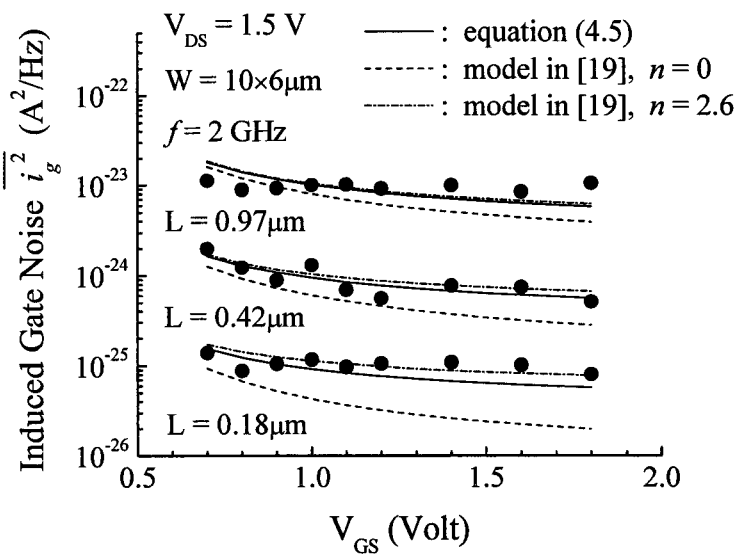



Fig. 4.2: Extracted (symbols) and simulated (lines) spectral densities of the induced gate noise versus $V_{GS}$ characteristics for n-type MOSFETs [47].

## 4.2 Noise Source Implementation

As we have already known so far that accurate noise models are crucial for RF CMOS circuit design. What will be the next step after the accurate noise models are obtained? Given that the spectral densities of channel noise $\overline{i_d^2}$ and induced gate noise $\overline{i_g^2}$ are obtained from either theoretical calculation or experimental results, the next step is how to implement them into circuit simulator so that RF IC designers can benefit from accurate noise models. In this section, we will introduce a solution to implement the channel noise and the induced gate noise into existed compact models using the sub-circuit method. By using this method, the impact of the noise sources can be shown and the noise performance of RF ICs can be predicted by circuit simulator. The implementation method introduce in this section using cub-circuits is very general and can be applied to any compact model (e.g. BSIM3v3, MOS11 or EKV model).

### 4.2.1 Noise Calculation

Assuming that a noisy two-port network with input port (port 1) and output port (port 2) consists of $M$ transistors and $N$ resistors, the total noise current which will appear at the short-circuited output port (port 2) is the sum of the noise contribution from each transistor and resistor in the network, which can be given by

$$\overline{i_{out}^2} = \sum_{i=1}^{M} \overline{i_{out,M_i}^2} + \sum_{j=1}^{N} \overline{i_{out,R_j}^2}, \tag{4.7}$$

where $\overline{i^2_{out,M_i}}$ is the noise current at the output port contributed by the $i^{th}$ transistor and $\overline{i^2_{out,R_j}}$ is the output noise current contributed by the $j^{th}$ resistor. In general, the power spectral density $\overline{i^2_{out,R_j}}$ can be calculated by

$$\overline{i^2_{out,R_j}} = |A_{2j}|^2 \cdot \frac{4kT}{R_j}, \tag{4.8}$$

where $A_{2j}$ is the current gain between port 2 and the noise source associated with the $j^{th}$ resistor $R_j$, and it can be obtained by the circuit simulator. For the noise contribution from transistors, it consists of the noise current contributed from the channel noise $\overline{i_d^2}$, the induced gate noise $\overline{i_g^2}$ and their noise correlation $\overline{i_g i_d^*}$ in each transistor, i.e.

$$\sum_{i=1}^{M} \overline{i^2_{out,M_i}} = \sum_{i=1}^{M} \overline{i^2_{out,i_g^2(M_i)}} + \sum_{i=1}^{M} \overline{i^2_{out,i_d^2(M_i)}} + \sum_{i=1}^{M} \overline{i^2_{out,cor(M_i)}}. \tag{4.9}$$

In most of the compact models used by circuit designers today, only the channel noise is implemented, and it only works well for long-channel devices. Therefore, what is going to be solved next is how to implement the enhanced channel noise in short-channel devices, induced gate noise and their noise correlation based on existed compact models. Because most of the circuit simulators do not handle correlated noise sources, this project mainly focuses on the implementation of the enhanced channel noise and the induced gate noise.

### 4.2.2 Equivalent Circuit Model

Assuming that the spectral densities of channel noise $\overline{i_d^2}$ and induced gate noise $\overline{i_g^2}$ are obtained from either theoretical calculation [9],[19] or experimental results [41], the next step is to implement these noise sources into the circuit simulator. The method proposed in this thesis using sub-circuits can work with any compact model (e.g. BSIM3v3, MOS 11 or EKV model). The proposed noise equivalent circuit model including the substrate network and noise sources is shown in Fig. 4.3. The implementation of each noise source in MOSFETs is presented in the following sections, and the BSIM3v3 compact model is used to demonstrate the noise implementation.

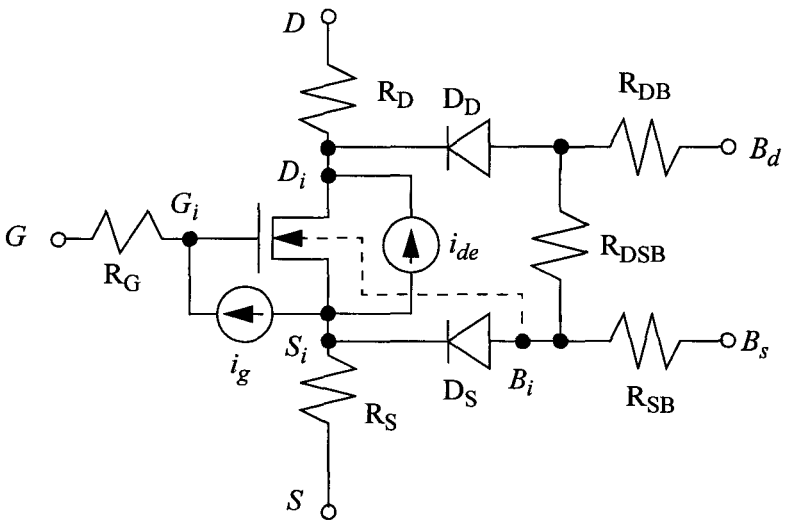



Fig. 4.3: Noise equivalent circuit of a MOSFET including parasitic resistance ($R_D$, $R_G$ and $R_S$), substrate network ($D_D$, $D_S$, $R_{DB}$, $R_{SB}$ and $R_{DSB}$), enhanced channel noise ($i_{de}$) and induced gate noise ($i_g$) for RF IC applications.

### 4.2.3 Enhanced Channel Thermal Noise

The enhanced channel thermal noise $i_{de}$ shown in Fig. 4.3 is implemented by using a **C**urrent **C**ontrolled **C**urrent **S**ource (CCCS), and its value is determined by the noise current which is generated by the reference resistance $R_{de}$ as shown in Fig. 4.4(a) and flows through the voltage source $V_{de}$ with zero DC and AC voltages. With the noise flag ***noiMod*** in BSIM3v3 noise model set to 4, the spectral density of the channel noise generated by the BSIM compact model is given by [42]

$$\overline{i_{dBISM}^2} = \frac{4kT\mu_{eff}}{L_{eff}^2}|Q_{inv}|, \tag{4.10}$$

where $k$ is Boltzmann's constant, $T$ is the absolute temperature, $\mu_{eff}$ is the effective mobility, $L_{eff}$ is the effective channel length and $Q_{inv}$ is the inversion channel charge. Therefore, the proposed noise source $\overline{i_{de}^2}$ should only compensate the difference between $\overline{i_d^2}$ and $\overline{i_{dBSIM}^2}$. The noise spectral density $\overline{i_{dBSIM}^2}$ can be obtained by running noise simulations at the bias condition without the flicker noise which can be done by setting the flicker noise parameter $Kf$ to zero. The next step is to determine the value of $R_{de}$. From the thermal noise theory, the noise current from $R_{de}$ is given by

$$\overline{i_{de}^2} = \overline{i_d^2} - \overline{i_{dBSIM}^2} = \frac{4kT}{R_{de}}. \tag{4.11}$$

Therefore the value of $R_{de}$ can be obtained by

$$R_{de} = \frac{4kT}{\overline{i_d^2} - \overline{i_{dBSIM}^2}}. \tag{4.12}$$

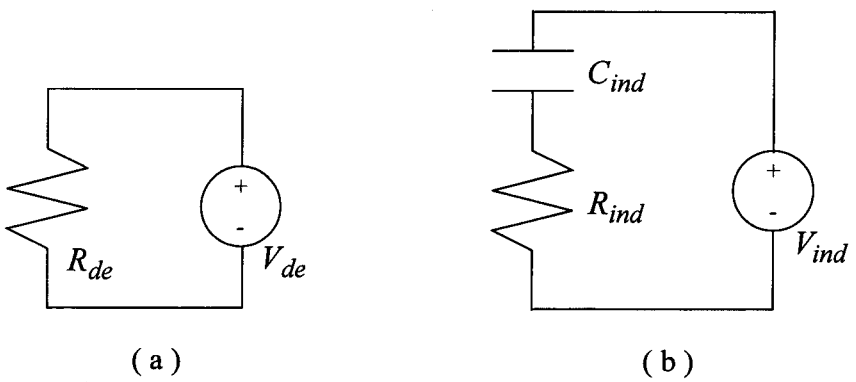



Fig. 4.4: Noise reference circuits to generate noise currents for (a) the enhanced channel noise $i_{de}$ and (b) the induced gate noise $i_g$ shown in Fig. 4.3.

### 4.2.4 Induced Gate Noise

The induced gate noise $i_g$ shown in Fig. 4.3 is also implemented by using a Current Controlled Current Source (CCCS). Because there is no induced gate noise included in the BSIM3v3 model, and it is shown in (4.5) that the induced gate noise is proportional to frequency square, the task is to find out a reference circuit for $i_g$ whose spectral density is proportional to frequency square without worrying about the contribution from the compact model. By trying different RLC circuits, it is found that an RC circuit shown in Fig. 4.4(b) can generate the noise spectral density with the desired frequency dependency by a proper selection of the resistance value $R_{ind}$ and the capacitance value $C_{ind}$ as described below.

For the noise reference circuit shown in Fig. 4.4(b), the noise current $i_{ind}$ flowing through the DC voltage source $V_{ind}$ is given by

$$i_{ind} = \frac{v_{ind}}{R_{ind} + \frac{1}{SC_{ind}}} = \frac{v_{ind} \cdot SC_{ind}}{1 + SR_{ind}C_{ind}}, \tag{4.13}$$

and its spectral density is given by

$$\begin{aligned} i_{ind}^2 &= i_{ind} \cdot i_{ind}^* = \frac{v_{ind}(SC_{ind}) \cdot v_{ind}^*(SC_{ind})^*}{(1 + SR_{ind}C_{ind}) \cdot (1 + SR_{ind}C_{ind})^*} \\ &= \frac{v_{ind}^2(j\omega C_{ind})(-j\omega C_{ind})}{(1 + j\omega R_{ind}C_{ind})(1 - j\omega R_{ind}C_{ind})} = \frac{v_{ind}^2 \omega^2 C_{ind}^2}{1 + \omega^2 R_{ind}^2 C_{ind}^2} \end{aligned} \tag{4.14}$$

If the values for $R_{ind}$ and $C_{ind}$ are properly selected in a way such that

$$\omega^2 R_{ind}^2 C_{ind}^2 \ll 1, \tag{4.15}$$

or

$$f \ll \frac{1}{2\pi R_{ind}C_{ind}}, \tag{4.16}$$

then

$$i_{ind}^2 \approx v_{ind}^2 \omega^2 C_{ind}^2 = 4kTR_{ind}C_{ind}^2\omega^2 = \overline{i_g^2}. \tag{4.17}$$

If the induced gate noise $\overline{i_g^2}$ is defined as a bias dependent constant $P_{ind}$ multiplied by the frequency square, from (4.17), we can obtain that

$$\overline{i_g^2} = P_{ind} \cdot f^2 = 4kTR_{ind}C_{ind}^2 \cdot 4\pi^2 f^2 . \tag{4.18}$$

After rearranging (4.18), we can obtain

$$R_{ind}C_{ind}^2 = \frac{P_{ind}}{16kT\pi^2} \tag{4.19}$$

or

$$R_{ind}C_{ind} = \frac{P_{ind}}{16kT\pi^2 \cdot C_{ind}} . \tag{4.20}$$

Because (4.17) is obtained when (4.16) is satisfied, substituting (4.20) into (4.16), it requires

$$\frac{16kT\pi^2 C_{ind}}{P_{ind}} \cdot \frac{1}{2\pi} \gg f \tag{4.21}$$

or

$$C_{ind} \gg \frac{P_{ind} f}{8kT\pi} . \tag{4.22}$$

For example, if we want this model to be valid up to 10 GHz (i.e. $f = 10$ GHz) and choose $C_{ind}$ to be 100 times $P_{ind}f/8kT\pi$ to satisfy (4.22), then $C_{ind}$ can be obtained by

$$C_{ind} = 100 \cdot \frac{P_{ind} \cdot 10^{10}}{8kT\pi} = \frac{P_{ind} \cdot 10^{12}}{8kT\pi} . \tag{4.23}$$

Substitute (4.23) to (4.19), $R_{ind}$ can be calculated by

$$R_{ind} = \frac{P_{ind}}{16kT\pi^2 C_{ind}^2} = \frac{4kT}{P_{ind} \cdot 10^{24}}. \quad (4.24)$$

## 4.3 Measurement and Discussion

This section will conduct circuit level verification for the channel noise model given by (4.4) and the induced gate noise model given by (4.5) by using the noise source implementation method introduced in section 4.2. Simulation and experimental results are compared for the four noise parameters - $NF_{min}$, $|\Gamma_{opt}|$, $\angle\Gamma_{opt}$ and $r_n$ based on two types of nMOSFETs. Long-channel nMOSFETs (channel length are 0.64 μm and 0.98 μm respectively) are used to verify the induced gate noise model, in the mean time, a short-channel nMOSFET (channel length is 0.18 μm) is used to verify the channel noise model.

### 4.3.1 Induced Gate Noise

Because the induced gate noise is pronounced in long-channel transistors operating at high frequencies, Fig. 4.5 to Fig. 4.8 show the measured (symbols) and simulated (lines) noise parameters - minimum noise figure ($NF_{min}$), normalized equivalent noise resistance ($r_n = R_n$ normalized to 50Ω) and optimized source reflection coefficient ($|\Gamma_{opt}|$ and $\angle\Gamma_{opt}$) versus frequency characteristics for two long-channel transistors working in the linear region, where the BSIM3 channel noise model is accurate. The non-quasi-static (NQS) effect is taken care of by the BSIM3 model. All the parameter values used in equation (4.5) are directly calculated based on the BSIM3v3 model parameters

without any fitting parameters. From Fig. 4.5 to Fig. 4.8, it is shown that with the proposed induced gate noise model and the implementation method, the four noise parameters can be accurately predicted, especially for $NF_{min}$ and $|\Gamma_{opt}|$.

For most of the RF applications, transistors will work in the saturation region. Fig. 4.9 to Fig. 4.12 show the noise parameters in the saturation region. It can be seen that the induced gate noise also has the dominant effect in the modeling of $NF_{min}$ and $|\Gamma_{opt}|$.

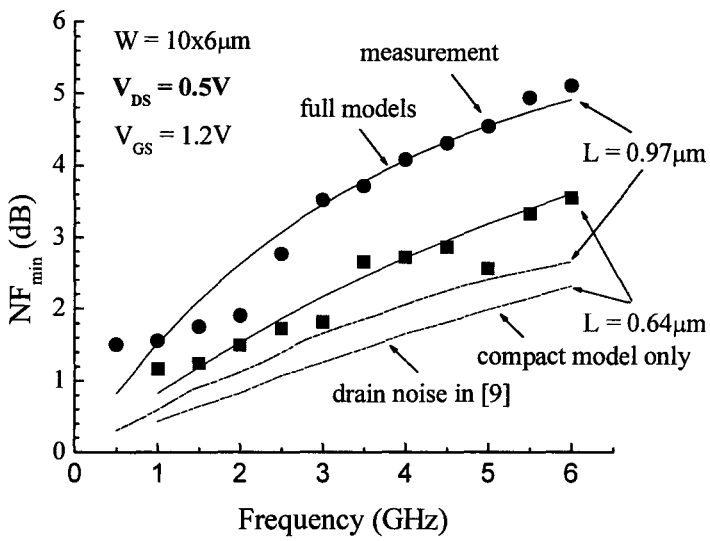



Fig. 4.5: Measured (symbols) and simulated (lines) $NF_{min}$ vs. frequency characteristics for long-channel transistors working in the linear region.

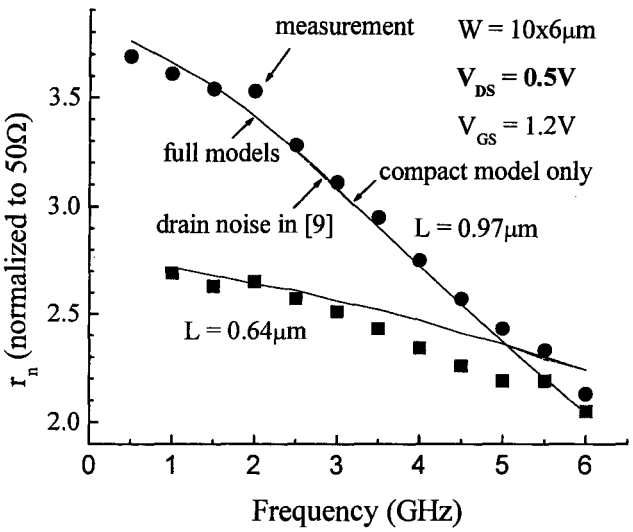



Fig. 4.6: Measured (symbols) and simulated (lines) $r_n$ vs. frequency characteristics for long-channel transistors working in the linear region.

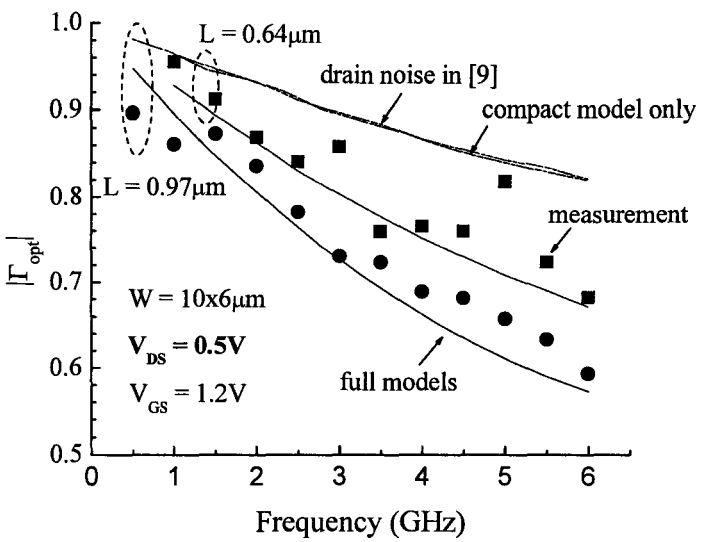



Fig. 4.7: Measured (symbols) and simulated (lines) $|\Gamma_{opt}|$ vs. frequency characteristics for long-channel transistors working in the linear region.

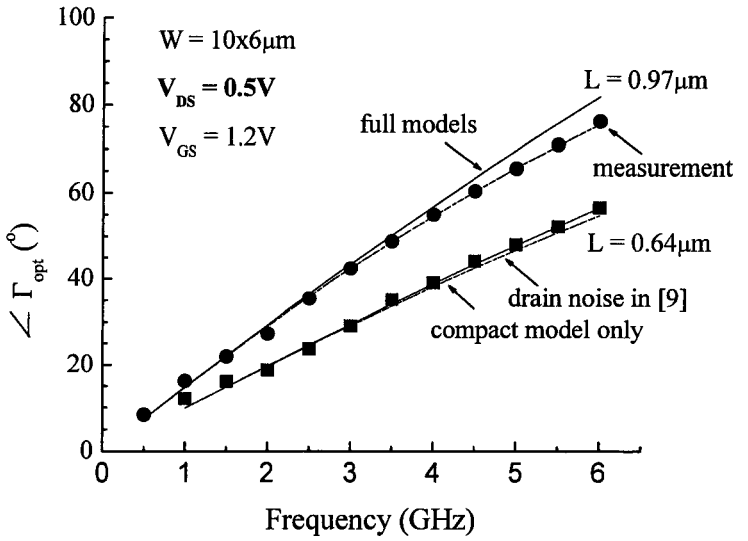



Fig. 4.8: Measured (symbols) and simulated (lines) $\angle\Gamma_{opt}$ vs. frequency characteristics for long-channel transistors working in the linear region.

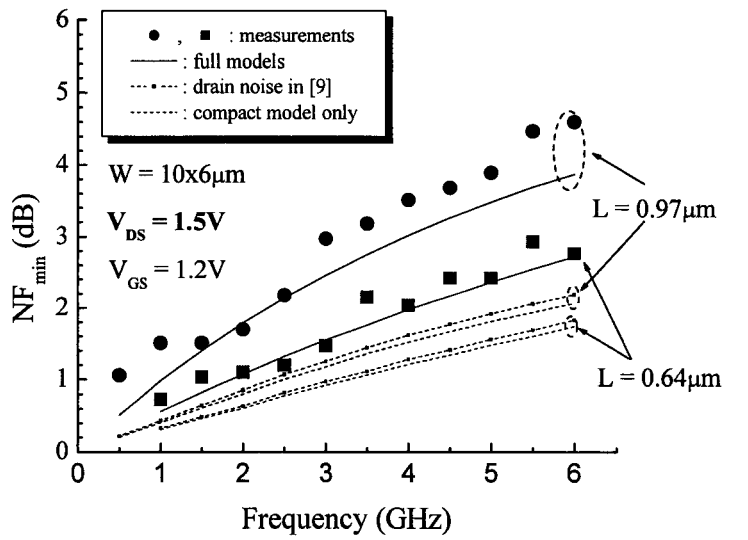



Fig. 4.9: Measured (symbols) and simulated (lines) $NF_{min}$ vs. frequency characteristics for long-channel transistors working in the saturation region.

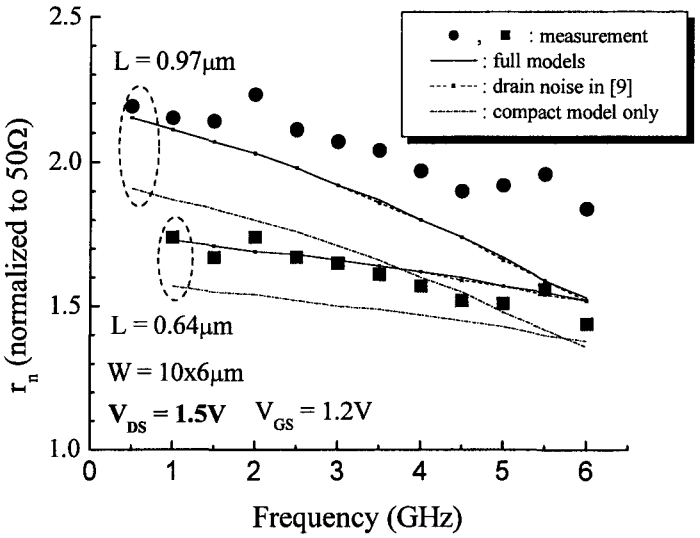



Fig. 4.10: Measured (symbols) and simulated (lines) normalized $r_n$ vs. frequency characteristics for long-channel transistors working in the saturation region.

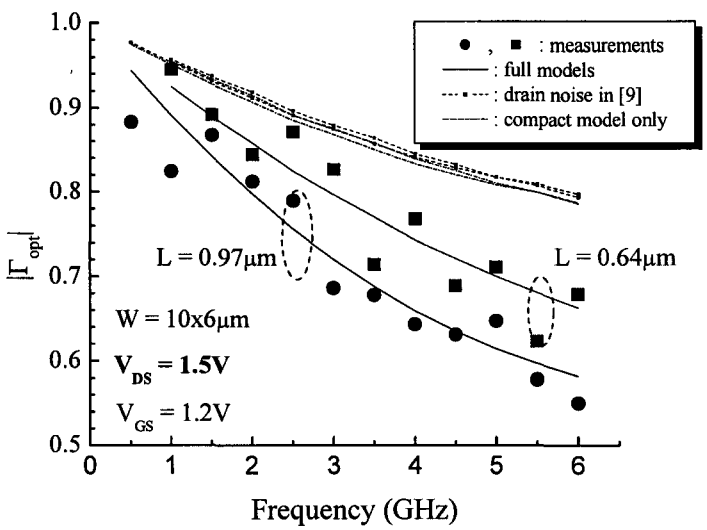



Fig. 4.11: Measured (symbols) and simulated (lines) $|\Gamma_{opt}|$ vs. frequency characteristics for long-channel transistors working in the saturation region.

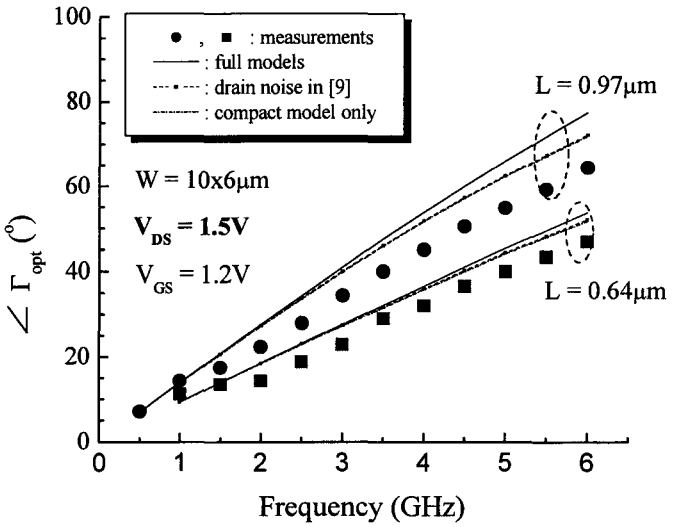



Fig. 4.12: Measured (symbols) and simulated (lines) $\angle\Gamma_{opt}$ vs. frequency characteristics for long-channel transistors working in the saturation region.

### 4.3.2 Channel Noise

For short-channel devices, the induced gate noise does not affect the noise parameters as much as it does in long-channel transistors. In order to give a comparison between the contribution from the induced gate noise and the contribution from the channel noise to the total device noise, Fig. 4.13 shows the $NF_{min}$ versus frequency characteristics for a 0.18μm transistor working in the saturation region, using the same process as the long-channel transistors shown in section 4.3.1. All short-channel effects are taken care of by the BSIM3 model. It is shown that the induced gate noise does not affect $NF_{min}$ as much as it does in long-channel transistors. On the contrary, the CLM effect becomes the most important effect in the noise modeling of short-channel transistors. For example, in Fig. 4.13, the induced gate noise only contribute 0.05dB to the

total $NF_{min}$ (which is 1.6dB at 5GHz), while the enhanced channel noise caused by the CLM effect contributes 0.45dB. It indicates that for short-channel devices, channel noise is the dominant noise source. In addition, noise due to the CLM effect has a significant contribution to the entire noise performance therefore can not be neglected anymore. Notice that if the channel width of the transistor is not wide enough, both measured and simulated $NF_{min}$ will fluctuate as shown in Fig. 4.13, and that's why it becomes more difficult to accurately measure the noise parameters of short-channel devices than those of long-channel devices.

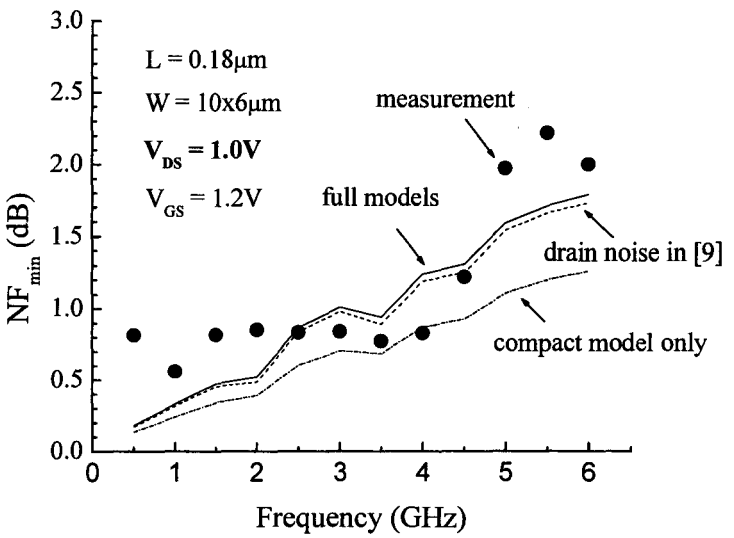



Fig. 4.13: Measured (symbols) and simulated (lines) $NF_{min}$ vs. frequency characteristics for a short-channel transistor working in the saturation region.

In order to accurately show the impact of enhanced channel noise for short-channel devices, another DUT fabricated in 0.18 μm CMOS technology with channel width W = 25 × 5 μm and channel lengths L = 0.18 μm is examined. Fig. 4.14 shows the

measured (symbols) and simulated (lines) $NF_{min}$ versus frequency characteristics working in the saturation region, where CLM effect shows its impact. It can be seen that with the enhanced channel noise due to channel length modulation effect included, the prediction of $NF_{min}$ becomes more accurate.

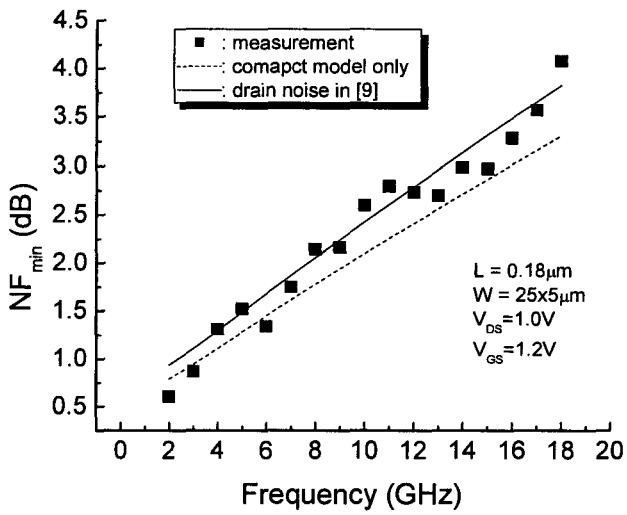



Fig. 4.14: Measured (symbols) and simulated (lines) $NF_{min}$ vs. frequency characteristics for short-channel transistors working in the saturation region.

It should be noticed that the presented noise implementation method for channel noise is not limited to implementing enhanced channel noise only. It can also implement the total channel noise. To do this, the total channel noise can be calculated by (4.4). Then, assuming $\overline{i_{dBSIM}^2}$ in (4.12) to be zero, the reference resistance $R_{de}$ can now be used to generate the total channel noise. The rest of the method keeps the same. This method is

valuable for some research purposes which are based on MOSFET's small-signal equivalent circuit instead of using compact models.

# Chapter 5

# IMPROVEMENT OF MODEL ACCURACY FOR RF NOISE SIMULATION

## 5.1 Objective

In order to accurately predict the channel noise of MOSFETs, the value of fitting parameter $\lambda$ in equation (4.3) must be accurately calculated. To do this, accurate mode parameters are required. Moreover, for a model to accurately predict the HF noise characteristics, the accuracy in the prediction of both DC and AC performance has to be ensured [68], even if the accurate noise model has been achieved. However, due to process variation, default parameter values from foundries have to be verified. Therefore, this chapter presents a systematic procedure to refine the model parameters used in noise calculation (including channel noise calculation and noise parameter calculation) based on the values provided by foundries.

## 5.2 DC Parameter Extraction

The first parameter to be verified in noise equation for channel noise shown in (4.4) is mobility $\mu_{eff}$. Equation (3.6) is adopted to calculate $\mu_{eff}$ in equation (4.4). In (3.6),

DC parameters such as $V_{th0}$, $\mu_0$, $U_a$ and $U_b$ should be accurate. The accuracy of these parameters can be seen from the comparison between measured and simulated drain current versus drain voltage characteristic shown in Fig. 5.1 and drain current verses gate voltage characteristic shown in Fig. 5.2. When conducting the DC parameter optimization, we also want to fit transconductance $g_m$ because $g_m$ is crucial for some RF applications such as low noise amplifiers.

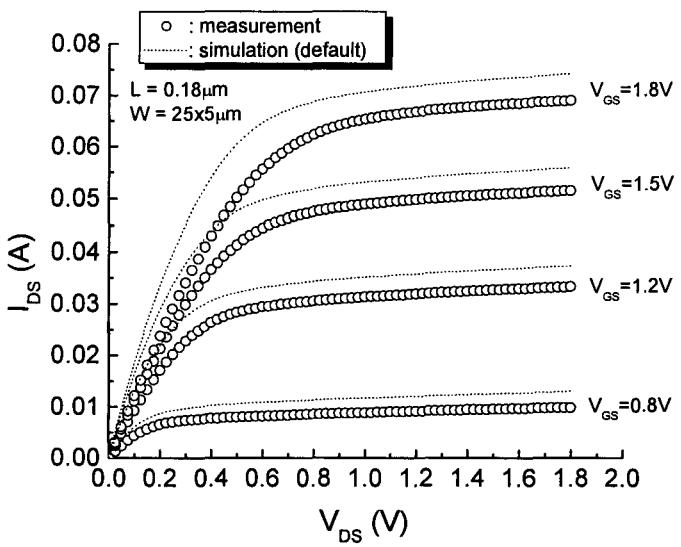



Fig. 5.1: Measured (symbols) and simulated (dash lines) $I_{DS}$ vs. $V_{DS}$ characteristic for the specified geometry and bias conditions with default parameter values.

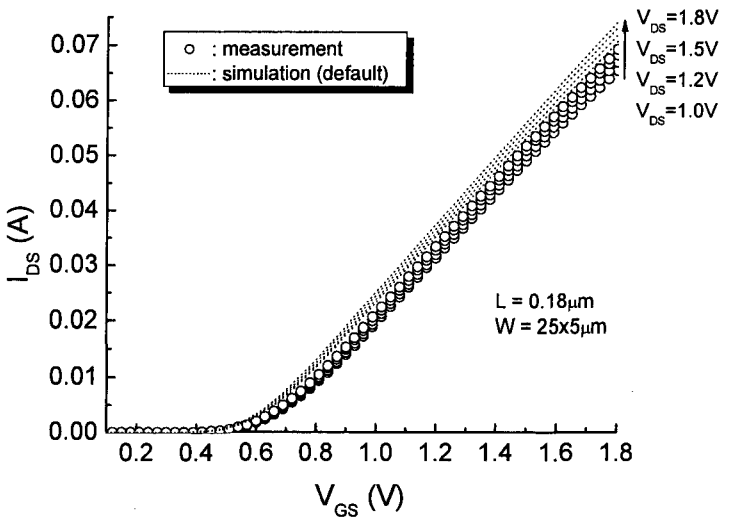



Fig. 5.2: Measured (symbols) and simulated (dash lines) $I_{DS}$ vs. $V_{GS}$ characteristic for the specified geometry and bias conditions with default parameter values.

### 5.2.1 Refining Threshold Voltage ($V_{th0}$)

When $V_{DS}$ is very small, transistors work in the linear region in which mobility degradation is weak and velocity saturation does not happen. In this case, the interception between the tangent line on the bias point at which the peak $g_m$ happens and the $V_{GS}$-axis is approximately $V_{th}$. Threshold voltage ($V_{th0}$) refinement is based on this theory

Based on this, the optimization for $V_{th0}$ is conducted by fitting the simulated $I_{DS}$ vs. $V_{GS}$ with the measurement at small $V_{DS}$ ($V_{DS}$ = 0.05V) within the $V_{GS}$ range between 0.2V and 0.4V. Since we will fit $V_{th0}$ at small $V_{GS}$ values, $U_a$ and $U_b$ can be set to zero to eliminate the mobility degradation effect. In the mean time, based on doping concentration

(*nch*), physical mobility value $\mu_0$ is adopted during the optimization. The optimization procedure for $V_{th0}$ is shown in Fig. 5.3.

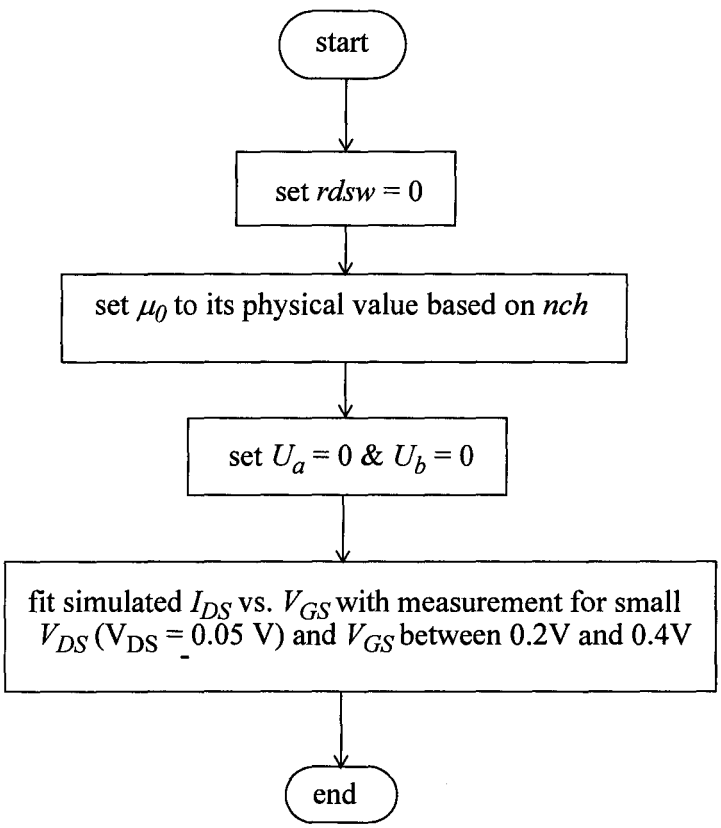



Fig. 5.3: Optimization procedure for refining $V_{th0}$.

The optimization result of $V_{th0}$ can be examined by the maximum transconductance method. Since this method is only applicable for the linear region (small $V_{DS}$ values), measured $I_{DS}$ vs. $V_{GS}$ characteristics for $V_{DS} = 0.05$ V is used. Based on the method, at the bias point corresponding to the maximum transconductance, a tangent line

is drawn at the point where the tangent line intercepts the $V_{GS}$-axis and gives the value of the threshold voltage ($V_{th0}$). Fig. 5.4 shows the fitting result for $V_{th0}$. It is shown that, by using this fitting procedure, the position of the interception between the tangent line corresponding to the maximum-transconductance point and $V_{GS}$-axis is accurately adjusted. The refined threshold voltage ($V_{th0}$) is given in Table 5.1 compared with its default parameter value.

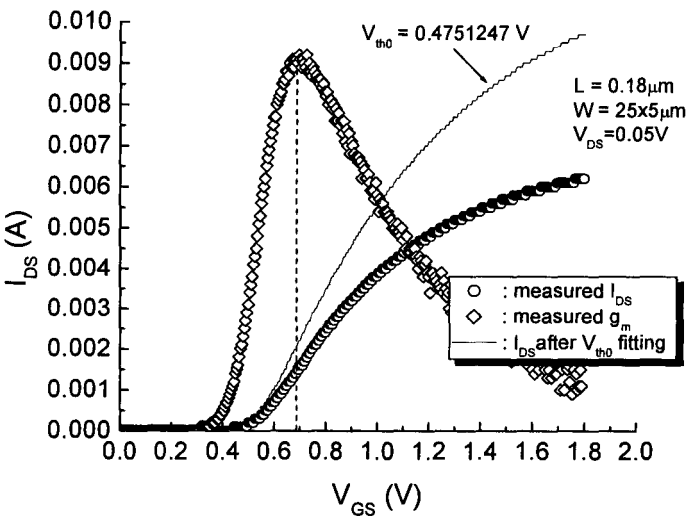



Fig. 5.4: Threshold voltage ($V_{th0}$) fitting result examined by the maximum-transconductance method for the specified geometry biased at low $V_{DS}$ ($V_{DS}$ = 0.05V).

Table 5.1 Comparison between optimized and default threshold voltage ($V_{th0}$).

| Parameters | Optimized Parameter Values after Fitting | Default Model Parameter Values before Fitting |
|---|---|---|
| $V_{th0}$ (V) | 0.4857 | 0.4751247 |

### 5.2.2 Refining Effective Mobility ($\mu_{eff}$)

Mobility degradation happens at high gate voltage bias. In equation (3.6), when setting $V_{BS}$ = 0 V, the effect of $U_c$ will be eliminated and equation (3.6) becomes

$$\mu_{eff} = \frac{\mu_0}{1 + U_a\left(\frac{V_{GS} + 2V_{TH}}{T_{ox}}\right) + U_b\left(\frac{V_{SB} + 2V_{TH}}{T_{ox}}\right)^2}. \tag{5.1}$$

When conducting optimization for $\mu_0$, $U_a$ and $U_b$ in equation (5.1), we need to compare the ratios between the measured and simulated $I_{DS}$ vs. $V_{GS}$ characteristics. If the ratios are constant, then the discrepancy is mainly due to the inaccurate of $\mu_0$. Otherwise, $U_a$ and $U_b$ are also responsible for the discrepancy. In this work, based on the doping concentration, the default model parameter value for mobility $\mu_0$ (0.04387662 $m^2$/Vs at T=300 K) is adopted [50]. Optimization of $U_a$ and $U_b$ is conducted by fitting both the measured $I_{DS}$ vs. $V_{GS}$ and $g_m$ vs. $V_{GS}$ simultaneously within the $V_{GS}$ range between 0.5V and 1.8V for different $V_{DS}$. The optimization procedure for $\mu_0$, $U_a$ and $U_b$ is shown in Fig. 5.5. The refined $U_a$ and $U_b$ are given in Table 5.2 compared with their default values.

Table 5.2 Comparison between optimized and default mobility-degradation coefficients ($U_a$ and $U_b$).

| Parameters | Optimized Parameter Values after Fitting | Default Model Parameter Values before Fitting |
|---|---|---|
| $U_a$ (m/V) | -2.2453e-10 | -9.0576310e-10 |
| $U_b$ $(m/V)^2$ | 3.4421e-18 | 2.7604860e-18 |

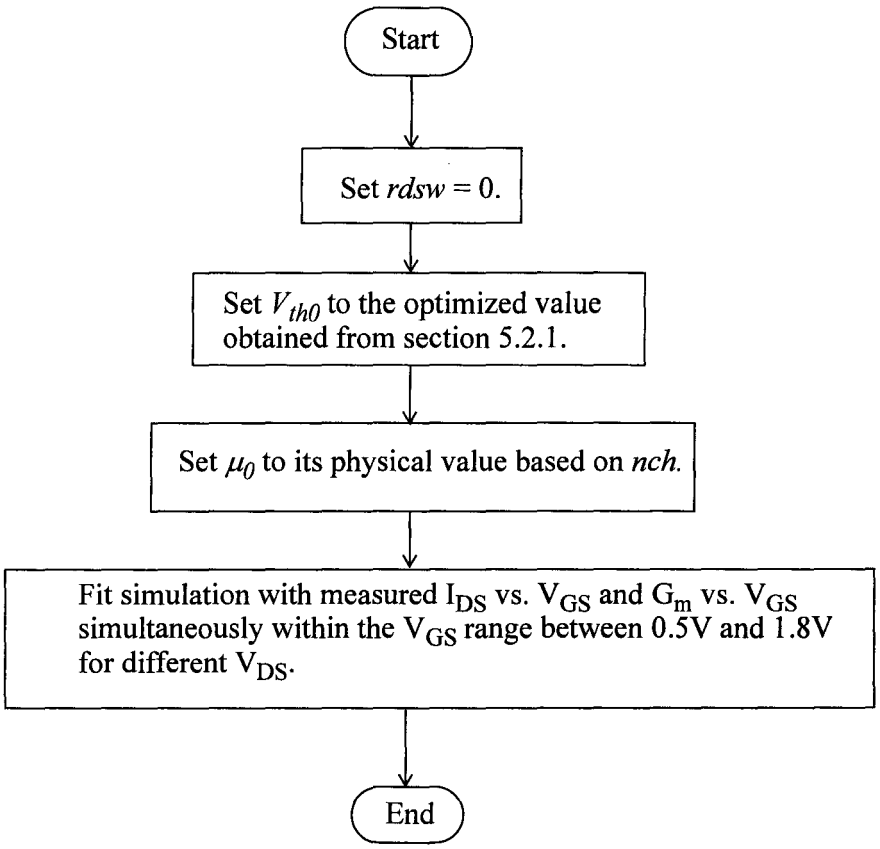



Fig. 5.5: Optimization procedure for refining $\mu_0$, $U_a$ and $U_b$.

The detail definition of the parameters used in DC parameter extraction here are listed in Appendix B. Fig. 5.6 and Fig. 5.7 shows the comparison among the measurement, the simulations based on default values and the simulations based on optimized values for drain current and transconductance versus gate and drain voltage characteristics, respectively.

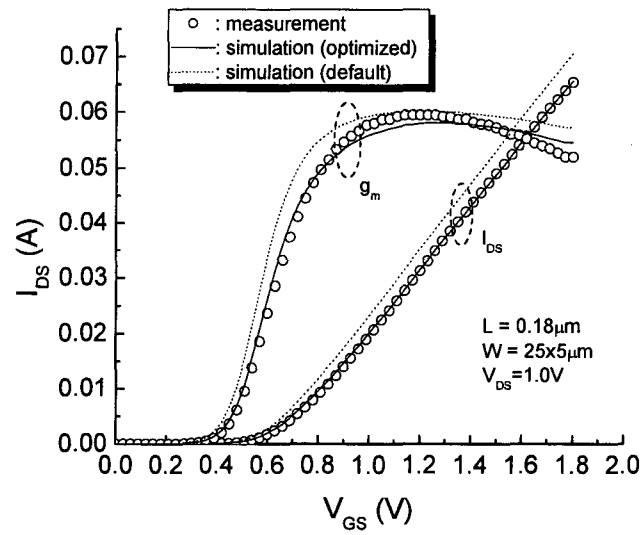



Fig. 5.6: Measured (symbols) and simulated results with default values (dash lines) and optimized values (solid lines) for drain current ($I_{DS}$) and transconductance ($g_m$) versus gate voltage ($V_{GS}$) characteristics.

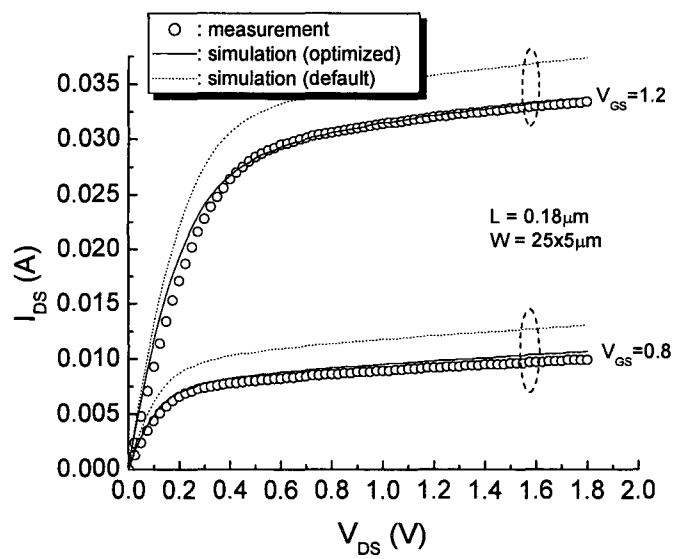



Fig. 5.7: Measured (symbols) and simulated results with default values (dash lines) and optimized values (solid lines) for drain current ($I_{DS}$) versus drain voltage ($V_{DS}$) characteristics.

## 5.3 Parameter Extraction for noise parameter λ

After the DC parameter optimization, the value of λ in equation (4.3) can be obtained by fitting the measured channel noise with the simulated channel noise. The optimized parameter values obtained in section 5.2 are applied into the optimization. The fitting result is shown in Fig. 5.8. The extracted value for noise parameter λ is 4.6607. It is shown that without DC model parameter optimization, using the default parameters will predict higher channel noise than the channel noise obtained from measurements. In addition, the simulated channel noise which includes the enhanced channel noise with the extracted λ value can also predict the correct trend of channel noise versus frequency characteristics. On the contrary, this trend can not be demonstrated by using the compact model only.

After λ is obtained, the length of the velocity saturation region can be calculated by using (4.1). Fig. 5.9 shows $\Delta L$ vs. $V_{GS}$ for the given transistor size and $V_{DS}$ bias. For example, it is shown that for an nMOSFET with channel length L = 0.18μm, channel width W = 5μm, and number of finger NF = 5, biased at $V_{DS}$=1.0 V and $V_{GS}$ = 1.2 V, the length of the velocity saturation region is about 14% of the total channel length.

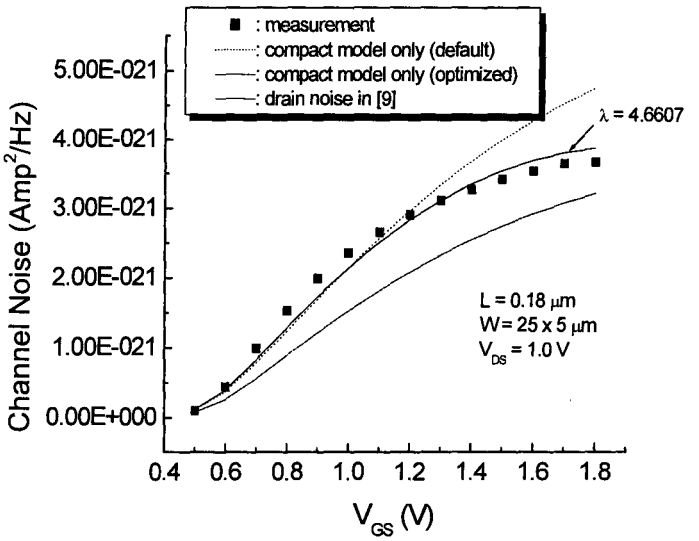



Fig. 5.8: Measured (symbols) and simulated (lines) channel noise vs. $V_{GS}$ characteristics for the nMOSFET with channel length L = 0.18μm, channel width W = 5μm, number of finger NF = 5 biased at $V_{DS}$=1.0V.

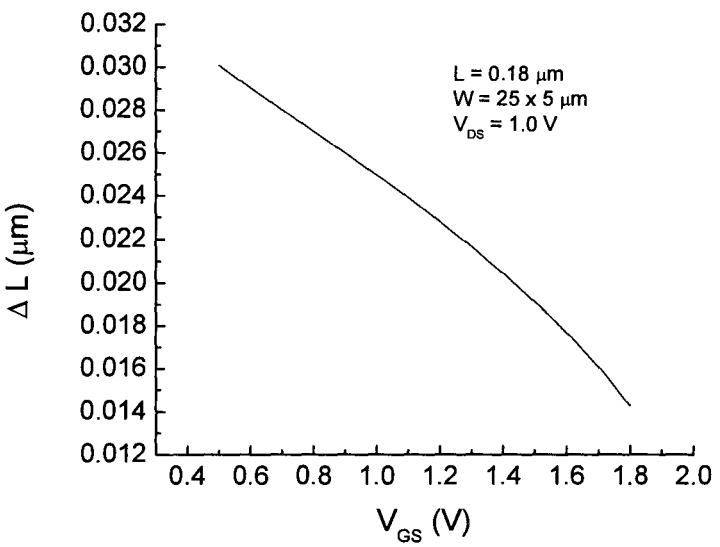



Fig. 5.9: The length of the velocity saturation region (ΔL) vs. $V_{GS}$ for the nMOSFET with channel length L = 0.18μm, channel width W = 5μm, and number of finger NF = 5 biased at $V_{DS}$=1.0V.

## 5.4 AC Parameter Extraction

In order to predict the noise performance at RF, model parameters related to AC characteristics should also be accurate. This can be done by fitting the measured intrinsic Y parameters which are obtained after performing the de-embedding procedure introduced in [51].

Most of the commercially available MOSFET compact models, such as BSIM3v3, MOS Model 9 and EKV model, are originally designed for digital or low-frequency analog circuits. When extending their application to RF IC design, some parasitic effects at high frequencies must be added into the models. These effects include the non-quasi-static (NQS) effect, distributed gate resistance and substrate parasitics. In our Y-parameter fitting procedure, gate resistance and substrate parasitics are modeled by the RF subcircuit. Since NQS effect is pronounced in RF application for long-channel devices, where the input signals have rise or fall time comparable to the channel transit time [52], the model accuracy of NQS effect is not serious for short-channel devices. Also because quasi-static (QS) assumption is valid up to about transistor's transit frequency ($f_T$) [10] and short-channel devices have very high $f_T$ (tens of giga Hertz), therefore, in this work, we adopt the core model approach in which the NQS effect can be modeled by the intrinsic core of compact models [26].

In the Y-parameter fitting procedure, we will optimize intrinsic Y-parameters by directly optimizing simulated C-V characteristics. Both the optimized simulation of C-V characteristics and Y-parameters will be shown.

### 5.4.1 Fitting C-V Characteristics

From [53] and [54], it is shown that gate-drain capacitance ($C_{gd}$) can be extracted from $|\mathrm{Im}\{y_{12}\}/\omega|$ and the total gate capacitance ($C_{gg}$) can be extracted from $|\mathrm{Im}\{y_{11}\}/\omega|$. When transistors working in saturation, $C_{gb} << C_{gs}$ and $C_{gb} << C_{gd}$ are hold where $C_{gb}$ is the gate-bulk capacitance, therefore gate-source capacitance ($C_{gs}$) can be obtained by $C_{gs} \approx C_{gg} - C_{gd}$. Furthermore, the gate resistance ($R_g$) can be extracted by $\mathrm{Re}\{y_{11}\}/(\mathrm{Im}\{y_{11}\})^2$. Based on these relations, $C_{gs}$ and $C_{gd}$ values can be directly extracted from measured Y-parameters. Therefore, optimization for $\mathrm{Im}\{y_{12}\}$ and $\mathrm{Im}\{y_{11}\}$ can be done by optimizing the extracted $C_{gs}$ and $C_{gd}$.

Fig. 5.10 shows the indication of $C_{gs}$ and $C_{gd}$ when the transistor is biased at saturation. The total gate-source and gate-drain capacitances ($C_{gs}$ and $C_{gd}$) include both intrinsic and extrinsic components which are given by

$$\begin{aligned} C_{gs} &= C_{gsi} + C_{gso} \\ C_{gd} &= C_{gdi} + C_{gdo} \end{aligned}, \tag{5.2}$$

where $C_{gsi}$ and $C_{gdi}$ are the intrinsic capacitances, and $C_{gso}$ and $C_{gdo}$ are the overlap capacitances. Notice that $C_{gdi}$ is zero in saturation. All these capacitance components (including the intrinsic capacitances and the overlap capacitances) are bias-dependent

[10]. Therefore, to optimize $C_{gs}$ and $C_{gd}$, we need to optimize the C-V characteristics of the transistor.

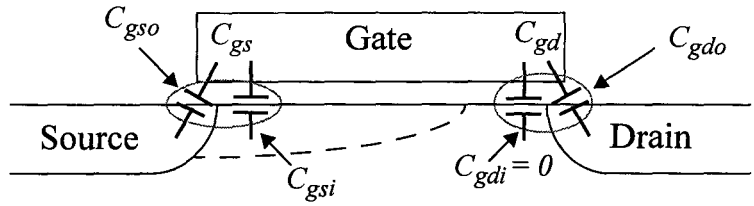



Fig. 5.10: Indication of components in gate-source capacitance ($C_{gs}$) and gate-drain capacitance ($C_{gd}$) when the MOSFET is based in saturation region.

Without parameter optimization, $C_{gs}$ and $C_{gd}$ vs. $V_{gs}$ characteristics are shown as dash lines in Fig. 5.11 compared with the measurement (symbols). We want to fit the gate-source overlap capacitance ($C_{gso}$) and the gate-drain overlap capacitance ($C_{gdo}$) first since it will be seen later that the significant discrepancy of the C-V characteristic between measurement and simulation is mainly due to $C_{gso}$ and $C_{gdo}$.

When the transistor is biased in saturation, the measured total gate-drain capacitance ($C_{gd}$) is equal to the gate-drain overlap capacitance ($C_{gdo}$) which is shown in Fig. 5.10. We assume that the value of the gate-source overlap capacitance ($C_{gso}$) and the gate-drain overlap capacitance ($C_{gdo}$) are equal. It shows that overlap capacitances are dominate in short-channel devices compared with that gate-channel capacitance dominating in long-channel devices. However, since the intrinsic capacitance can affect

the total channel inversion charge ($Q_{inv}$), intrinsic C-V characteristics have impact on the channel thermal noise according to (4.4) [72]. After $C_{gso}$ and $C_{gdo}$ are obtained, the next step is to optimize intrinsic model parameters.

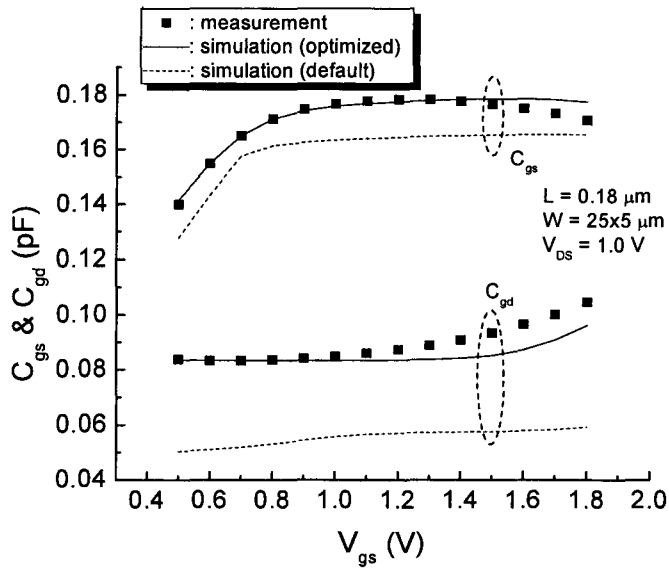



Fig. 5.11: Comparison of $C_{gs}$ vs. $V_{gs}$ and $C_{gd}$ vs. $V_{gs}$ among the measurement (symbols), simulation without parameter optimization (dash lines) and simulation after parameter optimization (solid lines).

In BSIM3v3 model, a charge partition parameter *xpart* is used to assign channel charges between source and drain. When *xpart* is set to one, it corresponds to saturation mode. Furthermore, BSIM3v3 models the bias dependant overlap capacitance by model parameters *cgso*, *cgsl*, *cgdo* and *cgdl*. For the intrinsic part, parameters related to intrinsic C-V characteristics are *dlc*, *clc*, *cle*, *voffcv* and *noff* which need to be optimized. The detail definition of the parameters used in AC parameter extraction here are listed in Appendix

B. Fig. 5.12 shows the indication of $C_{gs}$ vs. $V_{gs}$ and the corresponding model parameters for each region.

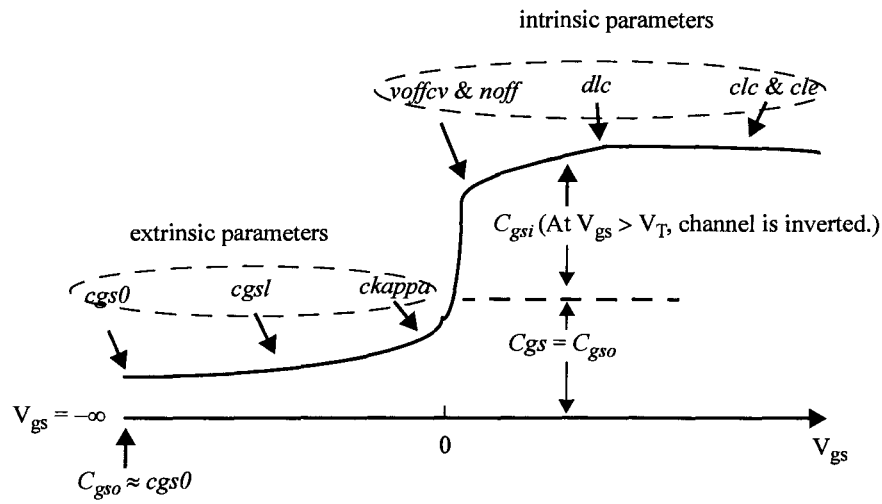



Fig. 5.12: Indication of $C_{gs}$ vs. $V_{gs}$ and the corresponding model parameters for each region.

It is noticed that the C-V characteristics of compact models, such as BSIM3v3, is essentially based on long-channel theory. Therefore, for short-channel devices, the shape of the simulated intrinsic capacitances versus $V_{gs}$ characteristics are slightly different from that of the measured result. This is mainly due to polydepletion [10][44] and short-channel effects [10][45].

The fitting procedure for the C-V characteristic is shown in Fig. 5.13. The final fitted C-V characteristic is shown in Fig. 5.11 and Table 5.3 gives the comparison between optimized and default model parameters.

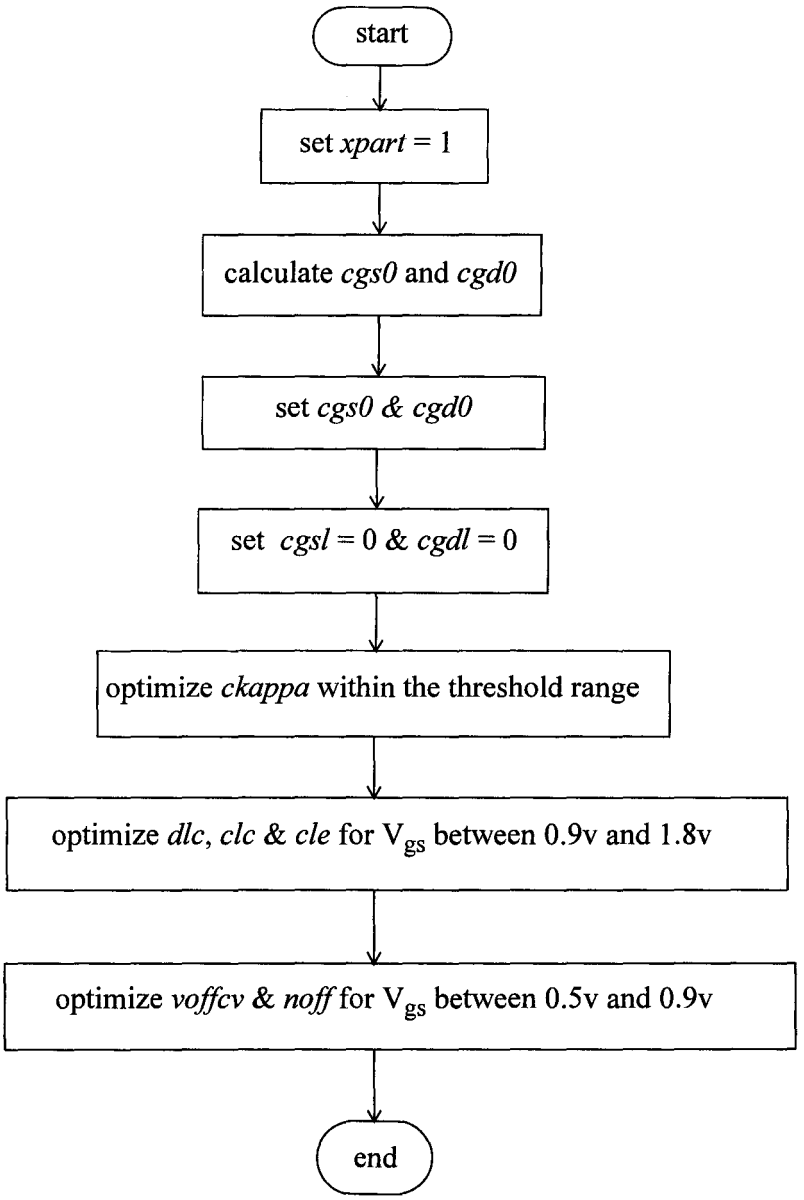


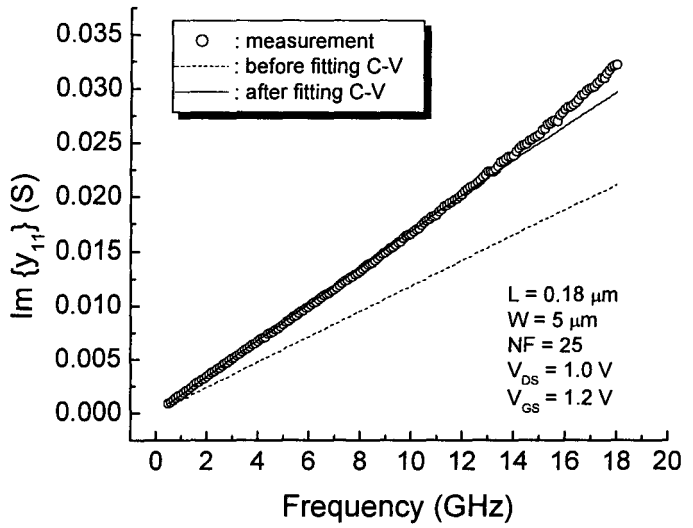

Fig. 5.13: Optimization procedure for fitting $C_{gs}$ vs. $V_{gs}$.

Table 5.3 Comparison between optimized and default model parameter values.

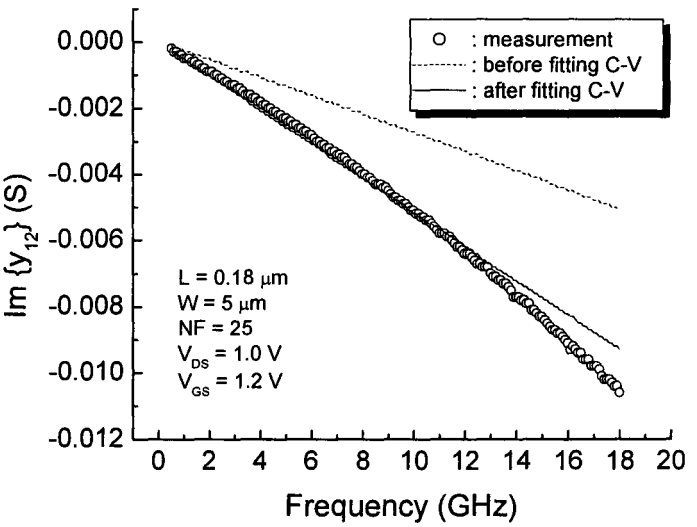
| Parameters | Optimized Values after Fitting | Default Model Parameters |
|---|---|---|
| *xpart* | 1 | 0 |
| *ckappa* | 10 | 1 |
| *cgso* (F/m) | 6.704e-10 | 4.3170e-10 |
| *cgsl* (F/m) | 0 | 6.6175e-10 |
| *cgdo* (F/m) | 6.704e-10 | 3.4367e-10 |
| *cgdl* (F/m) | 0 | 6.6175e-10 |
| *dlc* (m) | 2.2120e-08 | 4.6433e-08 |
| *clc* (m) | 1.6059e-09 | 1.45e-08 |
| *cle* | 1.6863 | 1 |
| *voffcv* (V) | 5.4707e-02 | 0.1261 |
| *noff* | 2.9153 | 1.2 |

### 5.4.2 Y-parameter Verification

After the model parameters related to gate-to-source and gate-to-drain capacitances are optimized as shown in section 5.4.1, the simulated and measured $\mathrm{Im}\{y_{11}\}$ and $\mathrm{Im}\{y_{12}\}$ have been achieved which are shown in Fig. 5.14. If further improvement is required for $\mathrm{Im}\{y_{11}\}$ and $\mathrm{Im}\{y_{12}\}$, separate overlap capacitances $C_{gso}$ and $C_{gdo}$ can be added into the RF subcircuit or simply pull the whole extrinsic capacitance out of the compact model and optimize $C_{gso}$ and $C_{gdo}$ by direct fitting the measured $\mathrm{Im}\{y_{11}\}$ and $\mathrm{Im}\{y_{12}\}$. This will not only account for the bias-dependent overlap capacitances but can also compensate the intrinsic capacitance bias dependence in the case they are not correctly accounted for due to short-channel effects [54]. Furthermore, some other sub-circuit components can also be optimized against Y-parameters. For example, optimize gate resistance ($R_g$) by optimizing $\mathrm{Re}\{y_{11}\}/(\mathrm{Im}\{y_{11}\})^2$ with the measurement.




( a )




( b )

Fig. 5.14: Comparison among the measurement (symbols), simulation without parameter optimization (dash lines) and simulation after parameter optimization (solid lines) for both (a) Im{$y_{11}$} and (b) Im{$y_{12}$}.

# Chapter 6

# DESIGN OF LOW NOISE AMPLIFIERS

## 6.1 Introduction

As the first stage of a receiver's front-end, LNA has the dominant effect on the noise performance of the overall system. According to Friis' formula, the overall noise figure of the receiver can be expressed as [57]

$$NF = NF_{LNA} + \frac{NF_{subsequent} - 1}{G_{LNA}}. \tag{6.1}$$

From this formula, it can be seen that noise of the LNA ($NF_{LNA}$) is directly injected into the received signal, and in the mean time, noise of all subsequent stages ($NF_{subsequent}$) is reduced by the gain of the LNA ($G_{LNA}$). Therefore, both high gain and low noise are important for LNA design in order to maintain a low-noise receiver system. However, as it will be explained in section 6.2.1, it is generally not possible to obtain both minimum noise figure and maximum gain for an amplifier simultaneously, so trade-off is made between noise and gain.

Besides low noise and high gain, some other features also need to be considered in LNA design. For example, in portable systems, low power is often imposed. Therefore,

low power consumption is another design constrain for LNA. Furthermore, input impedance matching, stability and linearity are also the goals for LNA design.

Several different topologies have been proposed for LNA design in order to meet the above design targets. For example, for single-stage LNAs in CMOS process, the common-gate topology [58] and inductively source degenerated common-source topology [59] are two commonly adopted topologies. However, for the common-gate topology in [58], it is shown that the lower bound for NF is 2.2dB for a perfectly matched COMS design [58]; for the common-source topology in [59], it involves more inductors, which will consume more area. For example, recent works have demonstrated good NF performance [60], they involve more inductors which occupy more area. Moreover, in silicon implementation, the loss associated with real inductors will degrade the NF in [59]. Based on the proposed topologies, some literatures [61][62] investigate design procedures through mathematical treatment by using optimization under multi-constrains. However, those procedures do not provide a practical design procedure from circuit designer's point of view.

In this chapter, we will first propose a new noise reduction technique for LNA. This technique gives designers an effective way to achieve low NF. It is shown that, with the noise reduction technique, designers have more control on the LAN's noise performance no matter fully integrated LNAs, bondwire inductor LNAs or off-chip inductor LNAs are adopted according to different applications. Based on the proposed noise reduction technique, a 2.4GHz single-ended input differential output LNA is introduced. A practical LNA design procedure is introduced within the design.

Furthermore, the impact of noise model accuracy on noise performance of LNA will be investigated. Finally, circuit level verification of the channel noise model introduced in section 4.1 will be conducted via the experimental result of a 5.2GHz single-ended input single-ended output LNA.

## 6.2 Noise Reduction Technique

### 6.2.1 Theory of the Noise Reduction Technique

A widely adopted noise matching technique is well explained in [11] and [59], and its basic topology is shown in Fig. 6.1(a). This technique is based on the theory that when input impedance of an LNA is designed to match the source impedance, the maximum power will be delivered from the source to the load and the maximum SNR will be achieved at the same time. However, it is generally not possible to obtain both minimum noise figure and maximum gain for an amplifier simultaneously [63]. This can be seen from the relationship between constant gain circles and constant noise figure circles in Smith chart. Both of them tend to shrink in Smith chart in order to obtain their optimal values. Therefore, in general, a trade-off needs to be decided between noise figure and gain.

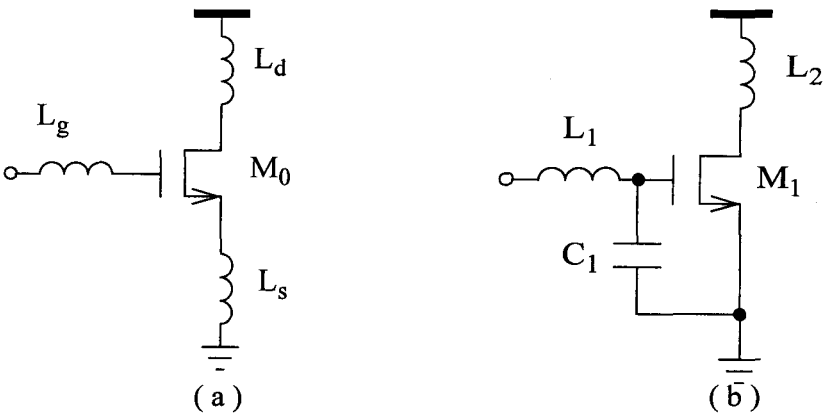



Fig. 6.1: Indication of (a) inductively source degenerated common-source topology [59] and (b) topology of the noise reduction technique.

From equation (2.17) which is given here again for convenience

$$NF = NF_{min} + \frac{4R_n|\Gamma_S - \Gamma_{opt}|^2}{(1-|\Gamma_S|^2)\cdot|1+\Gamma_{opt}|^2}, \tag{6.2}$$

it is shown that NF is contributed by two sources. One is from the device itself, the other is caused by mismatch. The noise reduction method introduced in this section is based on the theory that when $\Gamma_s = \Gamma_{opt}$ is provided, the perfect noise matching is obtained and zero noise figure is generated from mismatch. The definition of $\Gamma_s$ is shown in Fig. 6.2 which is the reflection coefficient seen from the input port of the transistor toward the source. On the contrary, the impedance matching method in [59] matches the impedance seen from input matching network with the source impedance, i.e. $Z_{NIN} = Z_i$ in Fig. 6.2. According to (6.2), we can see that this method generally cannot grantee the lowest noise figure (NF).

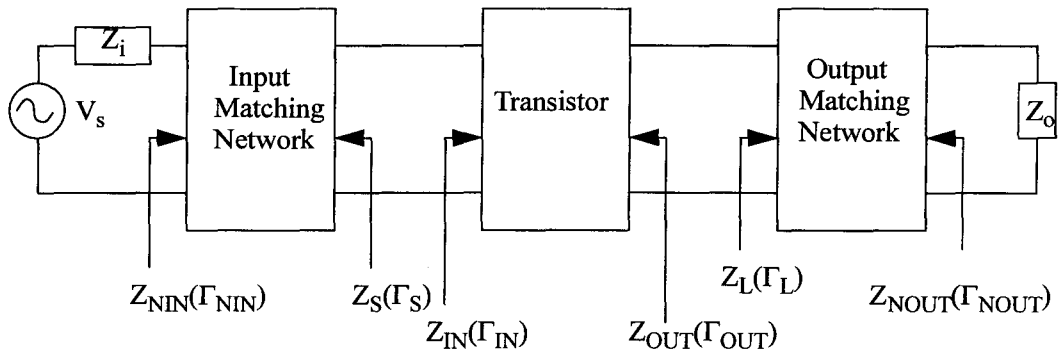



Fig. 6.2: Indication of impedance (reflection coefficient) at each port of a single transistor LNA.

For the given technology and under the power consumption limitation, the transistor's geometry and bias condition are correctly selected such that the lowest $NF_{min}$ is generated from the device. The main task after this is to obtain noise matching so that $\Gamma_s = \Gamma_{opt}$ is realized. Fig. 6.1(b) shows the proposed circuit topology for noise reduction. In order to provide a good noise matching, an input matching network is used to transform the source impedance ($Z_i$) to the optimal impedance ($Z_{opt}$) at the input of $M_1$ seeing toward the source in order to obtain $Z_s = Z_{opt}$. The input matching network mentioned here consists of $L_1$ and $C_1$ shown in Fig. 6.1(b) and their values can be decided by the following procedure.

Before adding the noise matching network, the single transistor's size and bias should have been determined so that minimum noise figure is achieved and the power consumption requirement is also met. Fig. 6.3 shows the constant noise circle (NC) of the

single transistor in Smith chart. The center of the Smith chart represents the 50Ω source impedance. As long as there is an intersection between the 50Ω source impedance circle and the constant noise circle, the matching can be achieved by providing an inductive match ($L_1$) between the 50Ω source impedance circle and the constant noise circle as shown in Fig. 6.3. If there is no intersection, this means the matching can not be accomplished by using $L_1$only. By adding a capacitor ($C_1$) between the gate and the source of $M_1$, the noise circle in Smith chart will be rotated counter-clockwisely. The position of the rotating NC in Smith chart can be adjusted by changing the value of $C_1$ until the intersection happens as shown in Fig. 6.3.

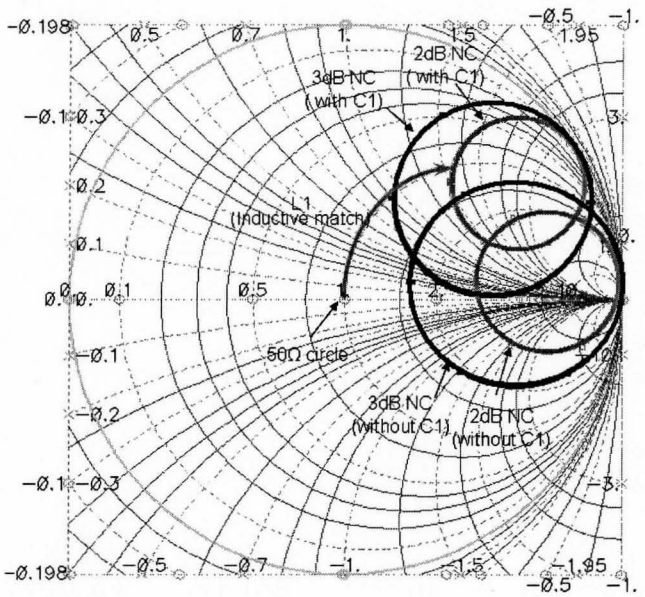



Fig. 6.3: Indication of the NC rotation by using the noise reduction technique.

By adding a capacitor ($C_1$) between the gate and the source of $M_1$, the noise circle in Smith chart will be rotated counter-clockwisely. This can be proved mathematically by the following derivation.

Based on the simplified MOSFET equivalent circuit model, it has been proved that the optimized source conductance ($G_{opt}$) and the optimized source susceptance ($B_{opt}$) can be expressed as [64]

$$G_{opt} = \frac{\omega C_{GS} R_G i_d \cdot \sqrt{\omega^2 C_{GS}^2 i_d^2 + i_G^2 g_m^2}}{i_d^2 + \omega^2 C_{GS}^2 R_G^2 i_d^2 + R_G i_G^2 g_m^2}, \tag{6.3}$$

and [64]

$$B_{opt} = -\frac{\omega C_{GS} i_d}{i_d^2 + \omega^2 C_{GS}^2 R_G^2 i_d^2 + R_G i_G^2 g_m^2}. \tag{6.4}$$

When the noise current due to the gate resistance is ignored, (6.3) and (6.4) can be simplified as

$$G_{opt} \cong \frac{\omega^2 C_{GS}^2 R_G}{1 + \omega^2 C_{GS}^2 R_G^2} \tag{6.5}$$

and

$$B_{opt} \cong -\frac{\omega C_{GS}}{i_d(1 + \omega^2 C_{GS}^2 R_G^2)}. \tag{6.6}$$

So the optimized source admittance ($Y_{opt}$) can be obtained by

$$Y_{opt} = G_{opt} + jB_{opt} \cong \frac{\omega^2 C_{GS}^2 R_G - j\frac{\omega C_{GS}}{i_d}}{1 + \omega^2 C_{GS}^2 R_G^2}. \quad (6.7)$$

Since $\omega^2 C_{GS}^2 R_G \ll 1$ and $\omega^2 C_{GS}^2 R_G^2 \ll 1$ are always true in Gigahertz region, (6.7) can be simplified to

$$Y_{opt} \cong -j\frac{\omega C_{GS}}{i_d}. \quad (6.8)$$

When capacitor $C_1$ is added between the gate and the source of $M_1$, the total gate-source capacitance $C_{GS}$ is increased. Therefore, the imaginary part of $Y_{opt}$ becomes more negative while the real part of $Y_{opt}$ keeps zero. This means that by increasing the value of $C_1$, the noise circle in Smith chart will rotate counter-clockwisely along the big circle whose conductance is zero.

### 6.2.2 Simulation and Discussion

To show the performance of the proposed technique, simulation results are given in Table 6.1, comparing with the simulation results using the topology introduced in [11] and [59]. Transistors with four different channel length which are 0.5μm, 0.35μm, 0.25μm and 0.18μm, respectively, are used in the simulation. In order to make a fair comparison, transistors are biased at the same condition at which 87.6% of the peak $g_m$ is achieved. The same power consumption is obtained by adjusting the channel width in each case. Ideal inductors are used in the simulation.

Table 6.1 Comparison of design results for the two different techniques.

| Channel Length | Using the technique introduced in [11] and [42] | | | | Using the proposed noise reduction technique | | | |
|---|---|---|---|---|---|---|---|---|
| | Lg (nH) | Ls (nH) | NF (dB) | Gain (dB) | L1 (nH) | C1 (fF) | NF (dB) | Gain (dB) |
| 0.50 μm | 33.45 | 0.75 | 1.16 | 10.00 | 13 | 200 | 0.80 | 20.89 |
| 0.35 μm | 55.18 | 0.42 | 1.20 | 18.06 | 15 | 200 | 0.53 | 17.61 |
| 0.25 μm | 73.18 | 0.26 | 1.24 | 23.91 | 16 | 200 | 0.39 | 17.65 |
| 0.18 μm | 94.40 | 0.16 | 1.41 | 20.26 | 17 | 200 | 0.30 | 18.27 |

From the simulated NF listed in Table I, it is shown that the noise reduction technique gives a better NF than the technique introduced in [11] and [59]. This technique also shows the correct trend of NF which decreases with the decreasing of channel length.

Adding capacitor $C_1$ in Fig. 6.1(b) will change the unit gain frequency. From equation

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}, \tag{6.9}$$

it can be asserted that the unit gain frequency $f_T$ will be decreased by adding $C_1$. Table 6.2 shows the changes of $f_T$ before and after adding $C_1$. It can be seen that with $C_1$ added, the unit gain frequency is still high enough for most of the narrow band applications.

Table 6.2 Influence on $f_T$ by adding $C_1$

| Channel Length (μm) | $f_T$ without $C_1$ (GHz) | $f_T$ with $C_1$ (GHz) |
|---|---|---|
| 0.50 | 9.16 | 3.92 |
| 0.35 | 15.70 | 5.13 |
| 0.25 | 24.46 | 6.74 |
| 0.18 | 36.50 | 8.74 |

In the real design, inductor types have strong impact on circuit performance. Although the values of off-chip inductors are easily controlled and using off-chip inductors can obtain good NF performance as adopted in [65], modern applications always demand highly integrated design. On-chip inductors and bondwires are the two choices for this demand. The parasitic effect in this case becomes a big issue which will affect the performance of noise figure. This limitation on inductor's quality factor causes the difference between the simulation result using ideal inductors and the measurement result using real inductors. To give a sense of how big the difference will be, Table 6.3 shows the simulation results of noise figure and gain for 0.18μm transistors using spiral inductor model, bondwire and off-chip inductor for $L_1$, respectively, based on the proposed noise reduction technique. For the bondwire, its inductance value is obtained from [66] and [67].

Table 6.3 Simulation results for real inductor models.

| **Inductor Model** | **NF** (dB) | **Gain** (dB) |
|---|---|---|
| spiral inductor | 2.64 | 7.99 |
| bondwire | 1.04 | 18.27 |
| off-chip inductor | 0.30 | 18.27 |

## 6.3 A 2.4GHz CMOS Single-ended Input Differential Output LNA

Using the proposed technique, Fig. 6.4 illustrates a 2.4 GHz single-ended input, differential output LNA. There are two stages of the LNA. $M_1$, $M_2$, $M_3$ and $M_4$ form the first stage. It minimizes noise figure and converts the single-ended RF signal to the differential RF signals. $M_5$ and $M_6$ form the second stage of the LNA which maximizes

the power gain at output. $L_2$, $L_3$, $L_6$ and $L_7$ act as AC loads of the two stages. At the input stage of the LNA, the noise reduction technique is used to achieve low NF, while a technique of gain matching between stages is used at the output stage of the LNA to boost the gain. The conversion of the single-ended RF signal to the differential RF signals is also accomplished by the LNA. This makes the off-chip balun not necessary since the practical balun which transforms the single-ended signal from the antenna into a differential signal will introduce extra loss which adds directly to the noise figure of the system [59]. The design procedure of section 6.3.1, 6.3.2 and 6.3.4 is general and can be applied to any narrow-band LNA design.

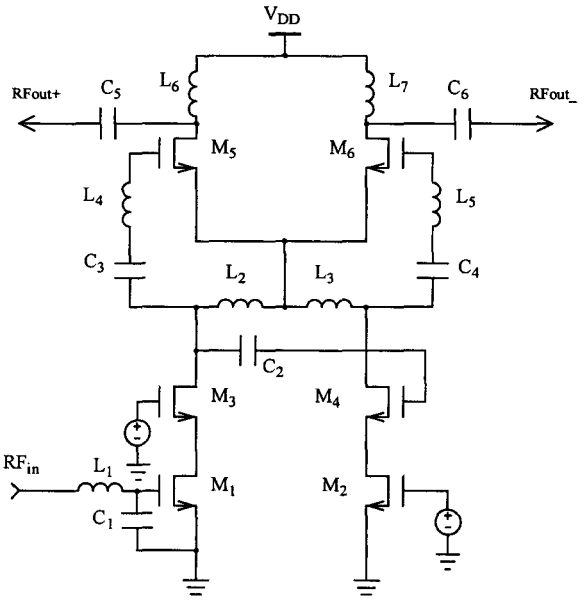



Fig. 6.4: Schematic diagram of the single-ended input, differential output LNA working at 2.4 GHz.

### 6.3.1 Selection of Transistor Size and Bias Conditions

Since $M_1$ locates at the very front end of the LNA, its noise performance is crucial to the entire LNA. Before the noise reduction technique is applied to $M_1$, its geometry and bias condition need to be carefully designed in order to obtain the lowest $NF_{min}$ from the device while satisfies the power consumption specification. First, $V_{gs}$ bias of $M_1$ is selected right before the peak $g_m$ in order to achieve $NF_{min}$ [68]. After that, the transistor width is selected to meet the power consumption requirement. Fig. 6.5 shows the procedure of selecting $V_{GS}$ bias and transistor's channel length W.

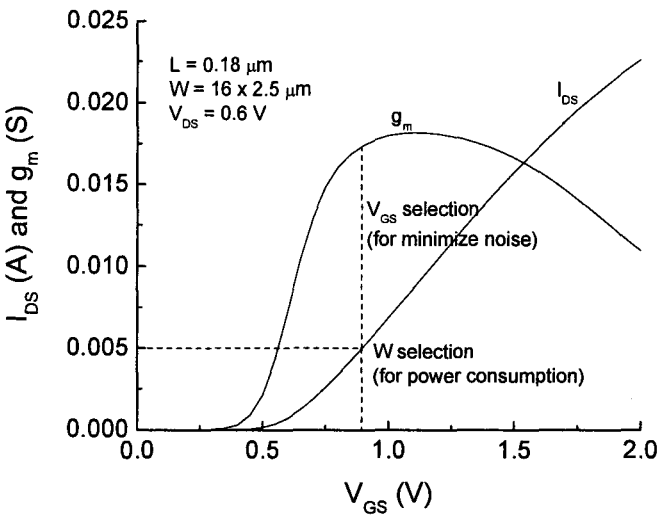



Fig. 6.5: Selection of bias $V_{GS}$ and channel width $W$ for channel Length $L = 0.18\mu m$ and $I_{DS} = 2.5mA$.

### 6.3.2 Noise Matching

After the transistor's size and bias are decided, the noise reduction technique is applied to $M_1$ to achieve noise matching. Based on the technique, $C_1$ is used to rotate the noise circle in Smith chart in order to intersect with the 50Ω source impedance circle, and $L_1$ is used to provide an inductive match. $M_1$ and $M_3$ form a cascode amplifier to further decrease the NF by increasing the gain.

### 6.3.3 Single-ended Input to Differential Output Conversion

Being a common-gate amplifier, $M_3$ provides in-phase signal at its drain compared with the signal at its source. This in-phase signal is connected to the gate of the common-source amplifier $M_4$, which generates an out-of-phase signal at its drain [69]. In this case, the signal at the drains of $M_3$ and $M_4$ are out-of-phase and become a differential pair. $C_2$ is used to provide DC isolation between the drain bias of $M_3$ and the gate bias of $M_4$.

Since the differential pair flows through symmetrical paths except at $C_2$, a tiny phase shift is caused making the differential pair not exactly out-of-phase. To compensate the phase shift, $C_5$ and $C_6$ at output are used to fine tune the phase making the output differential signals exactly out-of-phase.

### 6.3.4 Power Matching Between Stages

After the noise matching is achieved and the single-ended input signal is converted into differential signals, the second stage consisted of $M_5$ and $M_6$ is used to maximize the gain of both branches. The current reuse topology [70] is adopted to maintain the low

power consumption level. Maximum gain will be realized when a conjugate match between the impedance of two stages is provided. In order to realize a conjugate match, $C_3$ and $C_4$ are used to cancel the imaginary part of the output impedance seen from the drains of $M_3$ and $M_4$. After this, a further maximum gain match can be done if necessary by providing inductive match ($L_4$ and $L_5$) between the output of the first-stage and the input of the second-stage.

### 6.3.5 Simulation Results

The LNA simulation is performed by Cadence (Spectre) using 0.18μm RF CMOS process. As discussed in Section 6.2.2, the LNA performance, especially NF, is strongly affected by the inductor's quality factor of $L_1$. Fig. 6.6 shows the NF of the LNA in the right branch using on-chip inductor, bondwire and off-chip inductor for $L_1$, respectively. Fig. 6.7 shows $S_{21}$ of the LNA in the right branch, also using three different types of $L_1$. Table 6.4 gives the summary of the LNA performance.

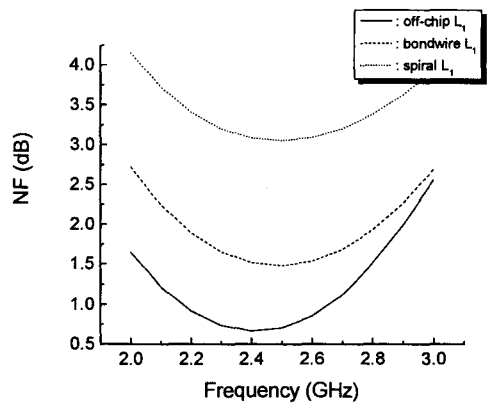



Fig. 6.6: Noise figure for the three different inductor types.

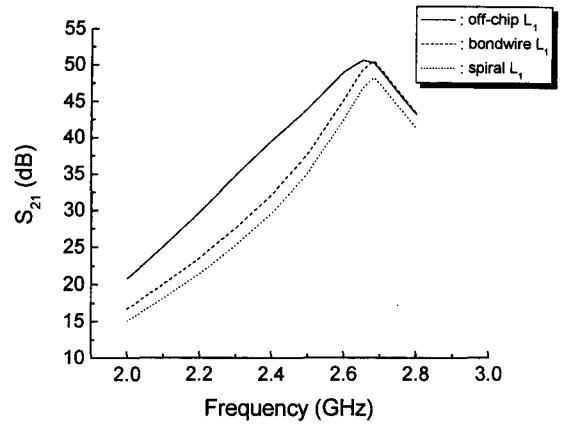



Fig. 6.7: Output power for the three different inductor types.

Table 6.4 Simulated performances of a 2.4GHz 0.18μm CMOS single-ended input differential output LNA.

| 2.4GHz 0.18 μm CMOS SINGLE-ENDED INPUT DIFFERENTIAL OUTPUT LNA | | | | | | |
|---|---|---|---|---|---|---|
| | off_chip L1 | | bondwire | | on_chip L1 | |
| | left branch | right branch | left branch | right branch | left branch | right branch |
| NF (dB) | 0.67 | 0.66 | 1.53 | 1.51 | 3.10 | 3.09 |
| $S_{21}$ (dB) | 34 | 40 | 27 | 32 | 24 | 30 |
| DC | 1.8 v / 5mA | | | | | |

## 6.3.6 Impact of Noise Models on the design of an LNA

In order to investigate the impact of the noise models on the design of an LNA, a single-stage amplifier with an inductor load is designed at 2.4 GHz and simulated by using devices with different channel lengths. Ideal inductors and capacitors are used in the design of input and output matching networks to achieve the lowest noise figure (NF) in each design. The simulation results shown in Fig. 6.8 are obtained by using the channel noise in [9], induced gate noise in (4.5), respectively with (solid line) and without (dashed

line) the CLM effect. It is shown that in this particular design, the LNA with L = 0.18μm gives the best noise performance. However, the enhanced channel noise in short-channel transistors enhances the NF of the LNA at the operating frequency and makes the noise figure improvement of short-channel transistors become less. In addition, the enhanced NF will be further increased when the frequency is deviated from the designed operating frequency. For the impact of $\overline{i_g^2}$, Fig. 6.9 shows the simulated noise figure with (solid lines) and without (dashed lines) induced gate noise. As expected, the induced gate noise does not have too much impact on short-channel transistors as it does on long-channel transistors.

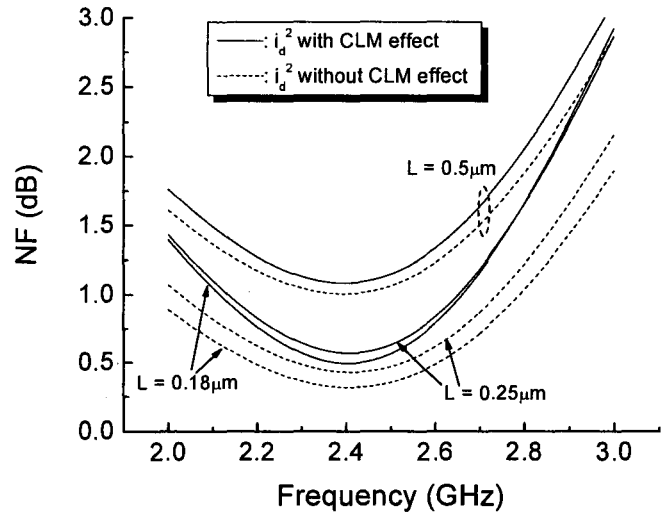



Fig. 6.8: Simulated noise figure (NF) of LNAs versus frequency characteristics with and without the CLM effect.

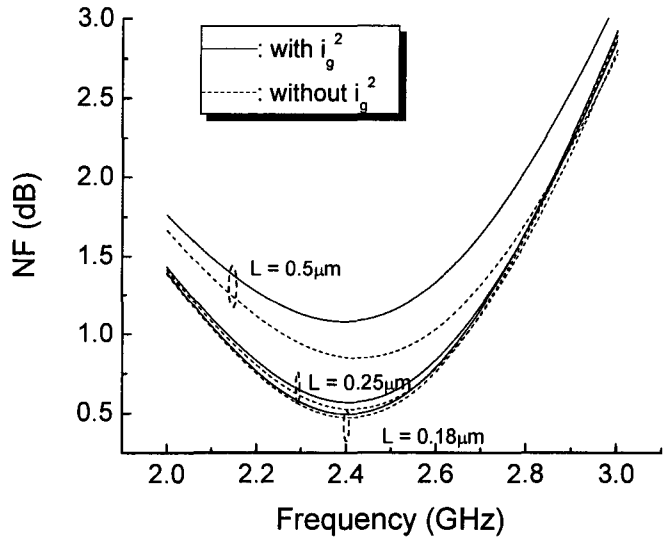



Fig. 6.9: Simulated noise figure (NF) of LNAs versus frequency characteristics with and without the induced gate noise.

## 6.4 Circuit Level Verification

### 6.4.1 Circuit Description

In order to verify the noise model at circuit level, another LNA is designed and measured. It is a single-ended input and single-ended output narrow-band LNA working at 5.2GHz. It uses the source-degenerated folded cascode topology [61] which consists of transistors $M_1$ and $M_2$. The source-degenerated method [11] is applied at the first stage ($M_1$) by using inductor $L_1$ for noise matching (The source-degenerated inductor in omitted because the 0.2nH inductance is too small to be fabricated). An interstage inductor ($L_2$) is

used for interstage impedance matching in order to improve the gain [71]. $L_3$ acts as the AC load. Fig. 6.10 shows the schematic of the LNA.

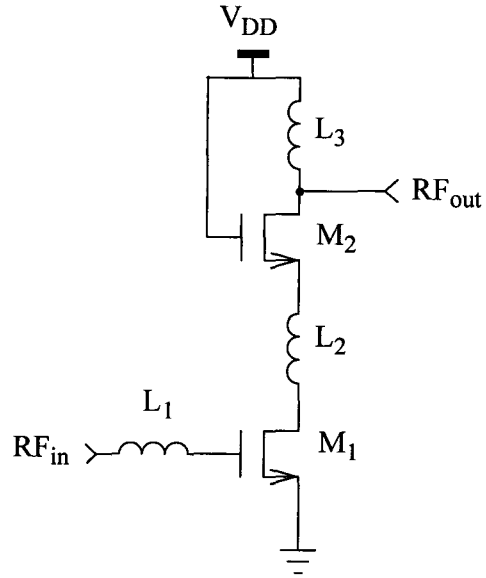



Fig. 6.10: Schematic diagram of the single-ended input, single-ended output LNA working at 5.2GHz.

### 6.4.2 Measurement and Discussion

The LNA including the bias circuit is implemented in CMOS 0.18μm technology. The whole circuit is fully integrated with three spiral inductors. The performance of the circuit is measured using on-wafer measurements. The LNA performance has been measured at $V_{DD}$ = 1.8 V with a power dissipation of 6.8mW. At this specified bias condition, the forward reflection coefficient $S_{11}$ is -6.4dB; the reverse reflection coefficient $S_{22}$ is -28dB; the power gain $S_{21}$ is 10.68dB and the noise figure NF is 7.36dB.

Fig. 6.11 shows the measured S parameters. Table 6.5 gives a summary of the LNA performance.

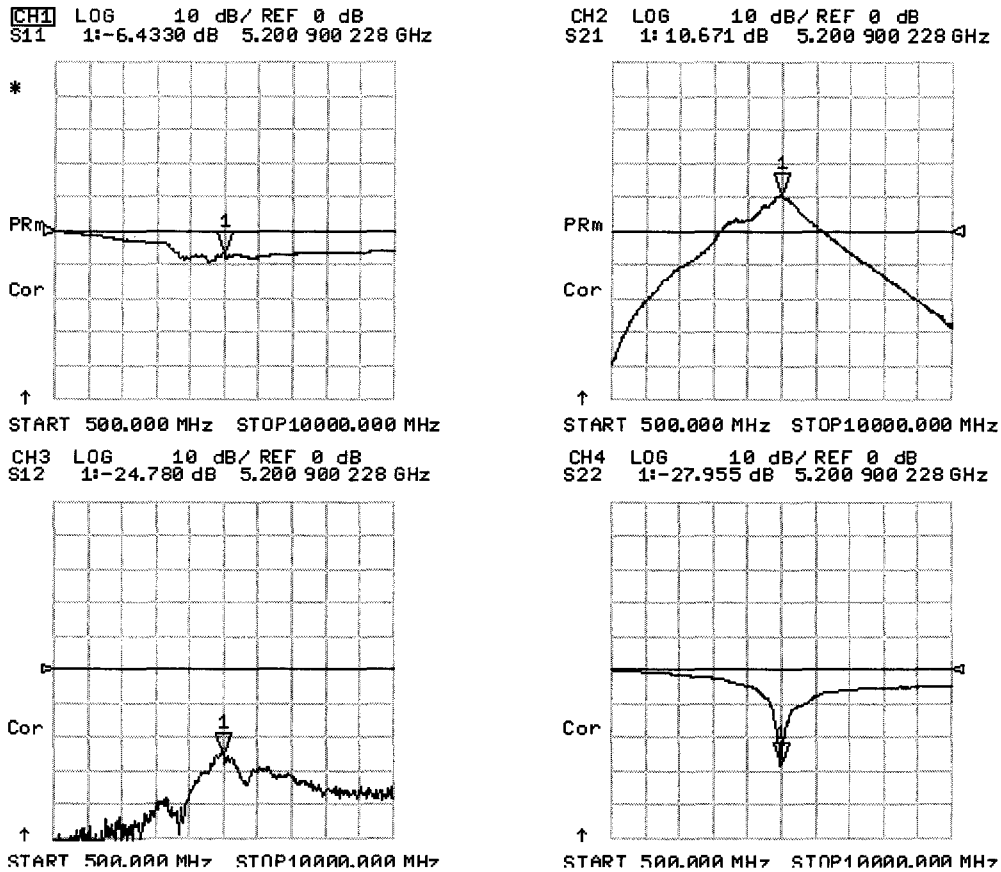



Fig. 6.11: Measured S-parameters at $V_{DD}$= 1.8 V for a power dissipation of 6.8mW for the proposed LNA.

Table 6.5 Summary of the measured 5.2 GHz LNA performances

| Parameters | Values |
|---|---|
| Operation frequency | 5.2 GHz |
| $S_{11}$ | -6.4 dB |
| $S_{12}$ | -24 dB |
| $S_{21}$ | 10.68 dB |
| $S_{22}$ | -28 dB |
| NF | 7.36 dB |
| Power dissipation | 6.8 mW |
| Technology | 0.18 μm |

### 6.4.3 Noise Model Verification by the LNA

In order to verify the channel noise model in (4.4), we want to make sure the simulated S-parameters are accurate compared to the measured S parameters, especially for $s_{21}$. This is because from (6.1) we can see that the gain of the LNA has impact on NF. It is important to notice that when conducting S-parameter simulation, parasitic effects of the layout have to be taken into account. These effects include the parasitic effect from pads and transmission lines, interaction between inductors, and also an accurate inductor model should be applied. Fig. 6.12 and Fig. 6.13 show the comparison between the simulated and measured S-parameters of the LNA with the parasitic effects in the layout being taken into account. It can be seen that the simulation and the measurement results are pretty close.

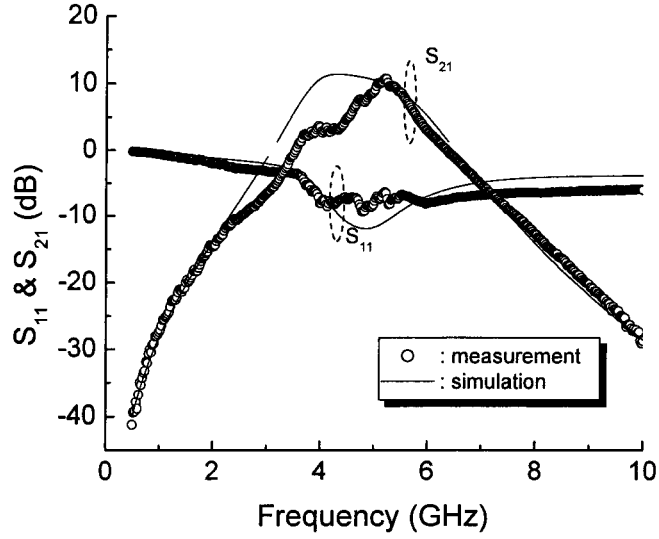



Fig. 6.12: Measured and simulated $S_{11}$ and $S_{21}$ of the LNA with the layout parasitic effects being taken into account by simulation.

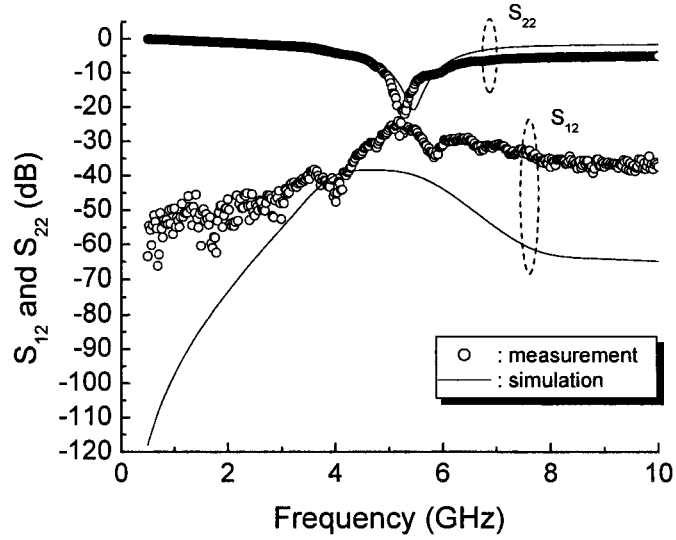



Fig. 6.13: Measured and simulated $S_{12}$ and $S_{22}$ of the LNA with the layout parasitic effects being taken into account by simulation.

After S-parameters are fitted, noise figure comparison can be done between measurement and simulation. It is found that the measured NF is high. This is mainly due to the loss of the RF cables used in the measurement, which can not be de-embedded by the instrument (N8975A Noise Figure Analyzer). By measurement, it is found that the loss of those particular RF cables is about 2dB. Based on this result, a 2dB attenuation is manually entered into the noise figure analyzer and it is found that NF decreased from 7.4dB to 5.7dB at 5.2GHz. Also at this frequency point, simulated NF increased from 4.35dB to 4.97dB by adding the enhanced channel noise into the simulation. The rest of the discrepancy between the measurement and the simulation is mainly due to the parasitic effect of probe pads. Table 6.6 gives the NF comparison between measurement and simulation. It indicates that for the given bias condition and at the given working frequency point, enhanced channel noise adds 0.6dB NF increase in this particular design. In addition, it is shown that the excess channel noise due to channel length modulation effect has to be taken into account for the LNA with targeted NF lower than 2dB.

Table 6.6 Noise figure comparison between measurement and simulation.

| **Measurement and simulation conditions** | **NF at 5.2GHz** |
|---|---|
| measurement (with cable loss included) | 7.4dB |
| measurement (with cable loss manually de-embedded) | 5.7dB |
| simulation (using compact model only) | 4.35dB |
| simulation (using drain noise with CLM effect [9]) | 4.97dB |

# Chapter 7

# CONCLUSIONS AND RECOMMENDATIONS

## 7.1 Conclusions

Providing that accurate noise models for deep-submicron MOSFETs have already been obtained, the main focus of this thesis is the noise model verification at both device and circuit levels. To fulfil these two tasks, three main topics have been accomplished in this thesis. They are the new technique to implement the channel noise and the induced gate noise with experimental verifications at both device and circuit levels, the systematic procedure for fine tuning model parameters for RF noise simulation, and the LNA design procedure with the new noise reduction technique.

For noise source implementation, by now, only flicker noise and channel thermal noise of MOSFETs are implemented in commercial circuit simulators (e.g. Spectre). The enhanced channel noise due to short-channel effects and the induced gate noise have not been implemented into any circuit simulators yet. Provided that the accurate noise models for channel noise and induced gate noise are obtained, how to use circuit simulators to verify them and further implement them into circuit simulators are the next concern. A general noise source implementation method has been presented in detail in this thesis and

is verified with measurements for both long and short-channel MOSFETs. This method provides a simple and effective way to implement the enhanced channel noise and induced gate noise of MOSFETs by only embedding two equivalent circuits into circuit simulators without increasing the simulation complexity for the simulators.

For a model to accurately predict the HF noise characteristics, the accuracy in the prediction of both DC and AC characteristics has to be ensured even if the accurate noise model equations have been obtained. However, due to the process variation, default parameter values from foundries have to be verified and fine tuned. A systematic procedure to refine the model parameters used in noise calculation is presented. This procedure provides both DC and AC parameter verification and optimization for RF noise simulation purpose. It indicates that DC parameters related to the channel noise model equation are crucial for the prediction of channel noise. This can be done by using the measured I-V characteristics as the optimization target. In the mean time, in order to predict the RF noise performance (such as the four noise parameters), AC characteristics should be also accurate. This can be done by using the measured intrinsic Y-parameters as the optimization target. Fitting the C-V characteristics obtained from the measured Y-parameters can effectively improve Y-parameter fitting especially for $\mathrm{Im}\{y_{11}\}$ and $\mathrm{Im}\{y_{12}\}$. For short-channel devices, parasitic capacitance dominates the total $C_{gs}$ and $C_{gd}$. In the mean time, intrinsic capacitance has impact on the total channel charge ($Q_{inv}$), and therefore has impact on the accuracy of channel noise prediction. Substrate network

modeling will affect the simulated Y-parameters especially through $y_{22}$. Therefore, accurate substrate modeling will also improve the RF noise performance prediction.

As for benchmark circuits to verify noise models at the circuit level, two LNA designs are proposed in the thesis. The first design gives emphasis on the noise reduction technique and the LNA design procedure. The second design is used to experimentally verify the noise model at the circuit level. In general, it is not possible to obtain both minimum noise figure and maximum gain simultaneously for an amplifier, the noise reduction technique gives circuit designer more control on noise figure minimization through noise matching. A general LNA design procedure is given which shows how to realize the first stage noise matching, inter-stage signal conversion and output power matching, which are the usual concern of LNA designs.

In this thesis, the techniques for noise model verification at device and circuit levels are general and can be applied to any proposed noise equations. As an example, noise model in [9] is adopted for the verification. This noise model is based on the theory in which velocity saturation region will not contribute any noise at the drain terminal and the enhanced channel noise of short-channel devices is due to channel length modulation (CLM) effect in the gradual channel region. At device level verification, it is proved that the model is accurate for both long and short-channel devices. It also shows that, for long-channel devices, induced gate noise is pronounced when transistors are operating at high frequencies. For short-channel devices, the induced gate noise does not affect the noise parameters as much as it does in long-channel transistors. On the contrary, the CLM effect

becomes the most important effect in the noise modeling of short-channel transistors. For example, for the chosen short-channel device at the given bias condition, the induced gate noise only contribute 3% to the total $NF_{min}$ in decibel, while the enhanced channel noise caused by the CLM effect contributes 28%. It indicates that for short-channel devices, channel noise is the dominant noise source. At circuit level verification, it shows that with the enhanced channel noise due to the CLM effect been included into the simulator, simulated NF is closer to the measured NF. It also indicates that for the chosen LNA design at the given bias condition and given working frequency point, enhanced channel noise adds 0.6dB noise figure increase which is important for LNAs with targeted NF lower than 2dB.

## 7.2 Recommendations

Based on the research results presented in this thesis, there are several recommendations for the future research work. First, in the noise source implementation method, the component values in the noise reference circuits are calculated based on single bias condition. Further improvement is required so that the component values can vary with different bias conditions. This will make it more practical for the implementation method to be used in circuit simulators.

Second, since there are three major noise sources of interest in MOSFETs when working at high frequencies - channel noise, induced gate noise and their correlation, correlation noise, although its influence is supposed to be very tiny compared with the

channel noise and the induced gate noise, need to be implemented in order to obtain a complete implementation method.

Third, since we already know that the accuracy of the substrate network modeling has impact on the prediction of RF noise performance, more investigation to obtain accurate substrate network is needed in the future research.

Finally, in the LNA measurement, the loss of the RF cables are measured separately and the attenuation is entered into the noise figure analyzer manually. The parasitic effect of the probe pads is not taken into account. The more accurate way is to use the measurement system (such as the ATN NP5B measurement system) to remove the impact of the cables and probes and the de-embedding procedure (e.g. introduced in [51]) to de-embedded the parasitic effect of the probe pads. This can further enhance the experimental accuracy for the future research.

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# Appendix A

# MODEL EQUATIONS USED IN NOISE SOURCE IMPLEMENTATION

This appendix lists the model equations for the calculation of the elements used in the noise reference circuits for channel noise implementation ($R_{de}$) and induced gate noise implementation ($R_{ind}$ and $C_{ind}$) introduced in Chapter 4.

## • model equations to calculate $R_{de}$

$$\overline{i_{dBISM}^2} = \frac{4kT_0}{L_{eff}^2}\mu_{eff}(-Q_{inv}), (noimod = 4). \tag{A.1}$$

$$\overline{i_d^2} = \frac{4kT_0}{L_{elec}^2}\mu_{eff}(-Q_{inv}) + \delta \cdot \frac{4kT_0 I_{DS}}{L_{elec}^2 \cdot E_{crit}^2} V_{DSsat}, \tag{A.2}$$

where $V_{DSsat}$ will become $V_{DS}$ and $L_{elec}$ will become $L_{eff}$ when the device operates in the linear mode.

$$\mu_{eff} = \frac{\mu_0}{1 + (U_a + U_c V_{BS})\left(\frac{V_{GS} + 2V_{TH}}{T_{ox}}\right) + U_b\left(\frac{V_{GS} + 2V_{TH}}{T_{ox}}\right)^2}. \tag{A.3}$$

$$L_{elec} = L_{eff} - \Delta L. \tag{A.4}$$

$$\Delta L = \frac{1}{\alpha}\ln\left(\frac{\alpha(V_{ds}-V_{dssat})+E_D}{E_{crit}}\right). \tag{A.5}$$

$$E_{crit} = E_{sat} = \frac{2v_{sat}}{\mu_{eff}}. \tag{A.6}$$

$$E_D = E_{crit}\sqrt{1+\left(\frac{\alpha(V_{ds}-V_{dssat})}{E_{crit}}\right)^2}. \tag{A.7}$$

$$\alpha = \lambda\sqrt{\frac{3}{2}\cdot\frac{C_{ox}}{x_j\varepsilon_{si}\varepsilon_0}}. \tag{A.8}$$

$$Q_{inv} = -W_{eff}L_{eff}C_{ox}(NF)\left(V_{gteff}-\frac{A_bV_{dseff}}{2}+\frac{A_b^2V_{dseff}^2}{12\left(V_{gteff}-\frac{A_bV_{dseff}}{2}\right)}\right), \tag{A.9}$$

where $V_{dseff}$ equals $V_{ds}$ in linear region and $V_{dssat}$ in saturation region.

$$A_{bulk} = \left(1+\frac{K_{1ox}}{2\sqrt{\Phi_s-V_{bseff}}}\left(\frac{A_0L_{eff}}{L_{eff}+2\sqrt{X_jX_{dep}}}\left(1-A_{gs}V_{gsteff}\left(\frac{L_{eff}}{L_{eff}+2\sqrt{X_jX_{dep}}}\right)^2\right)+\frac{B_0}{W'_{eff}+B_1}\right)\right)\cdot\frac{1}{1+KetaV_{bseff}} \tag{A.10}$$

$$X_{dep} = \sqrt{\frac{2\varepsilon_{si}(\Phi_s-V_{bs})}{qN_{ch}}}. \tag{A.11}$$

$$K_{1ox} = K_1\cdot\frac{T_{ox}}{T_{oxm}}. \tag{A.12}$$

$$V_{bseff} = V_{bc}+0.5(V_{bs}-V_{bc}-\delta_1+\sqrt{(V_{bs}-V_{bc}-\delta_1)^2-4\delta_1V_{bc}}), \tag{A.13}$$

where $\delta_1 = 0.001$.

$$V_{bc} = 0.9\left(\Phi_s-\frac{K_1^2}{4K_2^2}\right), \tag{A.14}$$

where $V_{bc}$ is the maximum allowable $V_{bs}$ value.

$$V_{TH} = V_{TH0} - K_1 \cdot (\sqrt{\Phi s} - \sqrt{\Phi_s - V_{bs}}) - K_2 \cdot V_b + K_1\left(\sqrt{1 + \frac{Nlx}{L_{eff}}} - 1\right)\sqrt{\Phi_s}. \quad \text{(A.15)}$$

$$\Phi_s = 2 \cdot \frac{kT}{q} \ln\left(\frac{N_{SD}}{n_i}\right). \quad \text{(A.16)}$$

$$V_{dsat} = \frac{E_{sat} L (V_{gs} - V_{th})}{A_{bulk} E_{sat} L + (V_{gs} - V_{th})}. \quad \text{(A.17)}$$

$$R_{de} = \frac{4kT}{\overline{i_d^2} - \overline{i_{dBISM}^2}}. \quad \text{(A.18)}$$

- **model equations to calculate $C_{ind}$ and $R_{ind}$**

$$P_{ind} = \frac{\overline{i_g^2}}{f^2} = \frac{4kT_0(2\pi)^2 W_{eff}^4 C_{ox}^4 \mu_{eff}^2}{I_{DS}^3} \times \left(V_{GT}^2 V_{as}^2 V_{DS} - V_{GT} V_{as} (V_{GT} + V_{as}) V_{DS}^2 \right. \quad \text{(A.19)}$$

$$\left. + \frac{1}{3}(V_{GT}^2 + 4 V_{GT} V_{as} + V_{as}^2)^2 V_{DS}^3 - \frac{1}{2}(V_{GT} + V_{as}) V_{DS}^4 + \frac{1}{5} V_{DS}^5\right)$$

$$V_{as} = V_{DS} - \frac{\frac{1}{2}(V_{GS} - V_{TH}) V_{DS} - \frac{1}{6} V_{DS}^2}{V_{GS} - V_{TH} - \frac{1}{2} V_{DS}}. \quad \text{(A.20)}$$

$$V_{GT} = V_{GS} - V_{TH}. \quad \text{(A.21)}$$

$$C_{ox} = \frac{\varepsilon_i}{t_{ox}}. \quad \text{(A.22)}$$

$$C_{ind} = \frac{100 \cdot P_{ind} \cdot f_{optmax}}{8kT\pi}, \text{ and} \quad \text{(A.23)}$$

$$R_{ind} = \frac{4kT}{10^4 \cdot P_{ind} \cdot f_{optmax}^2}, \quad \text{(A.24)}$$

where $f_{optmax}$ is the highest operational frequency.

# Appendix B

# MODEL PARAMETERS USED IN MODEL ACCURACY IMPROVEMENT

This appendix lists the model parameters used in model accuracy improvement introduced in Chapter 5.

## • model parameters for I-V characteristics

***rdsw***: source-drain resistance per gate width. When *noimod* = 4, *rdsw* is taken into account in noise simulation by $R_D(R_S)$ = *rdsw* / (wr·nr). When treating $R_D$ and $R_S$ as extrinsic resistance, *rdsw* needs to be set to 0.

***vth0***: long-channel threshold voltage at $V_{BS} = 0$.

***nch***: channel doping concentration.

***u0***: low-field mobility when the device operates at *tnom* (the temperature at which the model parameters are extracted). When temperature is fixed, *u0* is a strong function of doping concentration.

***ua***: first-order mobility-degradation coefficient due to vertical field.

***ub***: second-order mobility-degradation coefficient due to vertical field.

## •model parameters for C-V characteristics

***xpart***: channel charge partition flag. This parameter is used to select the charge partition by which the channel charge is divided between the drain and the source. When *xpart* = 0, BSIM3 uses 40/60 charge partition scheme, which means 40% of channel charge is assigned to the drain and 60% of channel charge is assigned to the source when the transistor works in saturation. When *xpart* = 0.5, BSIM3 uses 50/50 charge partition scheme. When *xpart* = 1, BSIM3 uses 0/100 charge partition scheme.

***cgso***: voltage-independent gate-source overlap capacitance per unit channel width.

***cgsl***: voltage-dependent gate-source overlap capacitance per unit channel width.

***ckappa***: coefficient of the overlap capacitance variation.

When $V_{GS}$ » 0 (in strong inversion), the overlap capacitance is equal to (*cgso* + *cgsl)*. When $V_{GS}$ « 0 (gate-source revers biased), the overlap capacitance decreases toward *cgso*. *Ckappa* is used to adjust the variation between the above two conditions. Usually, when the voltage dependence of the capacitance is weak, *cgsl* can be approximated to 0. Then, *cgso* can be extracted by the measured capacitance at 0 V subtracted by ($cf \cdot W_{eff,cv}$), where *cf* is friging-field capacitance per side [72].

***cgdo***: voltage-independent gate-source overlap capacitance per unit channel width.

***cgdl***: voltage-dependent gate-source overlap capacitance per unit channel width.

***voffcv***: offset threshold voltage in $V_{gsteff,CV}$ for weak-to-strong inversion region in C-V calculation. It enables an offset threshold voltage between I-V and C-V characteristics.

***noff***: smoothing parameter in $V_{gsteff,CV}$ for weak-to-strong inversion region in C-V calculation. It enables a different turn-on slop in the subthreshold region between I-V and C-V characteristics.

*voffcv* and *noff* can independently adjust the optimal fitting in both I-V and C-V characteristics. Otherwise, a good fitting in I-V may result a poor fitting in C-V characteristics [72].

***dlc***: effective channel-length offset fitting parameter from C-V characteristics. The corresponding parameter in I-V is *lint*. It is better to optimize *dlc* and *lint* separately in order to get a better fitting in both I-V and C-V characteristics.

***clc***: coefficient for $A_{bulk}$ in short-channel C-V characteristics.

***cle***: exponential term for $A_{bulk}$ in short-channel C-V characteristics.

BSIM3's C-V characteristics is essentially based on long-channel theory. In order to take the short-channel effects (such as velocity saturation effect) into account, BSIM3 uses $A_{bulk,cv}$ instead of $A_{bulk}$ in I-V model in all the C-V calculations which are originally derived for long-channel devices [72]. The model parameters *clc* and *cle* are the two parameters for adjusting $A_{bulk,cv}$. They may not have impact on extrinsic C-V characteristics due to the dominate parasitic effect of short-channel devices, but they have strong

impact on intrinsic C-V characteristics. Furthermore, since the intrinsic capacitance can affect the total channel inversion charge ($Q_{inv}$), *clc* and *cle* have impact on the channel thermal noise according to (4.4).