

**ULTRA-WIDEBAND, LOW POWER,
SILICON GERMANIUM
DISTRIBUTED AMPLIFIERS**

Ultra-Wideband, Low Power, Silicon Germanium Distributed Amplifiers

By

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ABSTRACT

As modern digital communications evolve, the requirements imposed on the systems than are required to transmit/receive the signals involved become more stringent. Amplifiers are required to provide gain from low frequencies, sometimes down to DC, up to high frequencies in the order of few to tens of gigahertz. Not only is the gain-bandwidth product to be enhanced, but also the amplifier should introduce minimal distortion to the signal and consume as low power as possible.

Distributed amplification is a multi-stage broadband circuit technique that may provide such a function. In distributed amplifiers, inter-stage transmission lines provide the capability to reach higher operational frequencies by absorbing the parasitic capacitances of the transistors used. Unlike other broadband topologies that trade-off gain and bandwidth, distributed amplifiers do not, but rather, the trade-off is between gain and delay. As gain stages are added, the gain increases as the bandwidth remains the same but the signal delay is increased.

This work considers the silicon germanium (SiGe) heterojunction bipolar transistor (HBT) implementation of distributed amplifiers. SiGe HBTs incorporate a thin SiGe base with Ge profiling to achieve high cut-off frequencies. SiGe BiCMOS processes are silicon based and hence have the major advantage of integrability to the low cost CMOS process unlike III-V compound semiconductors. Hence, SiGe is a promising technology capable of bridging the performance gap between silicon and III-V semiconductors.

The proposed amplifier achieves an approximately flat gain of 6.5 dB and a noise figure of 5.8 – 9 dB throughout the –3 dB passband of 10.5 GHz. The power consumed is 12.2 mW, significantly lower than previously published results by up to an order of magnitude in some cases. The group delay of the amplifier was found to be approximately constant in the passband at ~60 ps.

For the first time, temperature measurements are performed on SiGe HBT DAs. Analysis shows that the gain falls drastically with temperature increase due to deterioration in input matching caused by the significant change in the transistors input impedance with temperature. Similarly the NF, increases with temperature due to the decrease in gain. Moreover, noise analysis of SiGe HBT DAs is investigated, producing simulations predicting the NF of the proposed amplifier giving insight as to how noise may be reduced in future designs.

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The lab would be a dry place without my colleagues both Dr. Deen's and Dr. Yaser's groups. You all made this experience bearable and fun. I could always count on you and you too offered a lot for me to learn from. I especially thank you as you have been like a family to me for these two years. I look forward to treasure our friendships for the years to come.

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List of Symbols and Acronyms

α_b	Base line attenuation
α_c	Collector line attenuation
β	Common emitter current gain
β_b, β_c	Base, collector phase constants
ATL	Artificial Transmission Line
BEOL	Back-End of Line
BiCMOS	Bipolar CMOS
BJT	Bipolar Junction Transistor
Bps	Bits per second
BW	Bandwidth
CB	Common Base
CE	Common Emitter
C_{jc}, C_{cb}, C_μ	Base-Collector junction capacitances
C_{je}, C_{be}, C_π	Base-Emitter junction capacitances
CMOS	Complementary Metal Oxide Semiconductor
CPW	Coplanar Waveguide
$C_{\mu x}$	Extrinsic base-collector capacitance
DA	Distributed Amplifier
DUT	Device Under Test
EM	Electromagnetic
ENR	Excess Noise Ratio
FCC	Federal Communications Commission

FEOL	Front-End of Line
FET	Field-Effect Transistor
f_{max}	Maximum oscillation frequency
f_T	Transit frequency or unity gain cut-off frequency
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GBW	Gain-Bandwidth
GD	Group Delay
g_m	transconductance
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HMIC	Hybrid Microwave IC
I_B	DC base current
i_{be}	Equivalent input noise current (CE)
I_C	DC collector current
IC	Integrated Circuit
i_{ce}	Equivalent output noise current (CE)
InP	Indium Phosphide
i_{sb}	Base shot noise current
i_{sc}	Collector shot noise current
ITRS	International Technology Roadmap for Semiconductors
k	Boltzmann's constant
K_f	Stability factor

MESFET	Metal Semiconductor Field-Effect Transistor
MHEMT	Metamorphic High Electron Mobility Transistor
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave IC
NB	Narrow Band
NF	Noise Figure
NFA	Noise Figure Analyzer
PHEMT	Pseudomorphic High Electron Mobility Transistor
PN	Pseudo-random Noise
POTS	Plain Old Telephone System
PPM	Pulse Positioning Modulation
PR	Pseudo-Random
PSD	Power Spectral Density
q	electron charge
Q	Quality factor
R_{π}	Diffusion resistance
R_b	Total base resistance
R_{bb}	Intrinsic base resistance
R_{bx}	Extrinsic base resistance
R_c	Collector resistance
R_e	Emitter resistance
RF	Radio Frequency
RFID	Radio Frequency Identification

RMS	Root mean square
r_o	Output resistance
S_{11}	Input return loss
S_{12}	Reverse isolation
S_{21}	Power Gain
S_{22}	Output return loss
SEM	Secondary Electron Microscopy
Si	Silicon
SiGe	Silicon Germanium
SMU	Source-Measure Unit
SOI	Silicon-on-insulator
SOS	Silicon-on-Sapphire
SPA	Semiconductor Parameter Analyzer
SS	Spread Spectrum
T	Temperature
TL	Transmission Line
TWA	Traveling Wave Amplifier
UWB	Ultra-Wideband
VNA	Vector Network Analyzer
VSU	Voltage Source Unit
v_{tb}	Base resistance thermal noise voltage
v_{tc}	Collector resistance thermal noise voltage
v_{te}	Emitter resistance thermal noise voltage

Z_i	Image impedance
Z_{ib}	Base line image impedance
Z_{ic}	Collector line image impedance

Chapter 1

INTRODUCTION

1.1. Broadband Systems

The field of communications has undergone tremendous growth and evolution in recent years. As communication systems evolve, both speed and cost per function are expected to continually improve. In the domain of telecommunications, broadband systems are becoming the communication means of choice and the desire for bandwidth is increasing exponentially. As more consumers join in the current trend the bandwidth requirements becomes stringent with increase in needed channels multiplexed to accommodate those users. Moreover, individual applications are becoming more interactive, hence also requiring faster and higher capacity channels. This need for high

bandwidth is reflected in the growth of the global Internet backbone market as illustrated in Figure 1.1. Such a backbone requires links operating in the gigahertz and terahertz range using fiber optics, millimeter-wave, and satellite communication systems. Figure 1.2 shows the revenue breakdown of the telecommunications market for the year 2005. The figure clearly demonstrates how the market is going towards advanced fixed services, which include broadband applications. Mobile communications are also up from 19% in year 1997 with the POTS (Plain Old Telephone System) losing ground, falling to 31% from 60%.

Quickly developing as well is the field of consumer electronics. Digital appliances and equipment are naturally being extended to support wireless capabilities. Seamless connections are being implemented with telephones, computer peripherals, home entertainment systems, digital cameras, gaming systems, and the list goes on. Such applications require fast data link connectivity that can handle bursts of digital data.

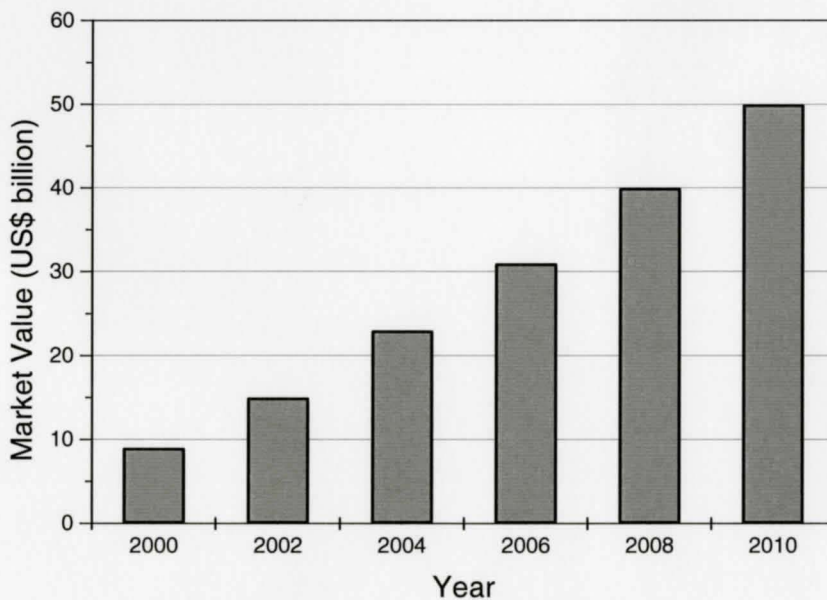


Figure 1.1: Global Internet backbone market growth [1]

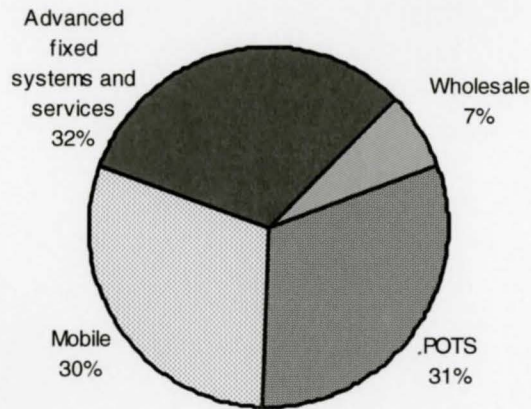


Figure 1.2: Telecommunications revenue breakdown for the year 2005 [1]

The foregoing discussion emphasizes the growing requirement for high bandwidth communications across a variety of application areas. This thesis focuses on a particular component (distributed amplifiers) that is designed for use in systems meeting the requirement for high bandwidth. Before discussing specifically the scope of this thesis, a brief introduction is in order to describe two types of systems that address the need for bandwidth at the systems level. ultra-wideband systems and optical systems.

1.1.1. Ultra-Wideband Systems

1.1.1.1. Definition and Theory

Ultra-Wideband, or UWB, is a promising technology, which was originated for the military in the need to produce radar that can have the capability to “see” through buildings and other opaque obstacles [2]. For military applications, the main requirements were high accuracy and low probability of interference and interception. This was to be accomplished by developing a new engineering technology using no new physical properties.

Currently, the prevalent method of wireless communication is via a sinusoidal carrier even though, historically speaking, wireless communications started off as digital in nature [2]. UWB utilizes narrow pulses without the need for an RF carrier. By directly modulating the signal into the antenna, components such as the local oscillator, mixer, and phase-locked loop in traditional RF systems are no longer needed. This greatly reduces circuit size and complexity, and hence fabrication cost. A typical UWB transmitter and receiver top level schematic is shown in Figure 1.3.

Other benefits of the UWB technique include [2]:

- Less complex circuitry and lower cost
- High data rates
- Multipath immunity
- Simultaneous ranging and communication
- Low power, low interference, and low regulation

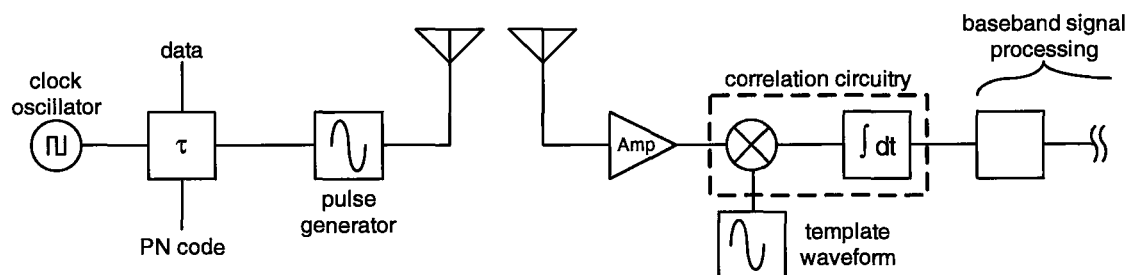


Figure 1.3: Block diagram of a typical UWB transmitter and receiver

The typical UWB pulse shape used is the Gaussian doublet, which is the 2nd derivative of the Gaussian wave. It is generated by a square wave that is easily obtained from a switching transistor combined with limited rise and fall times being shaped through the filtering effects of the transmitter and receiver antennas. The produced signal is shown as in Figure 1.4(a).

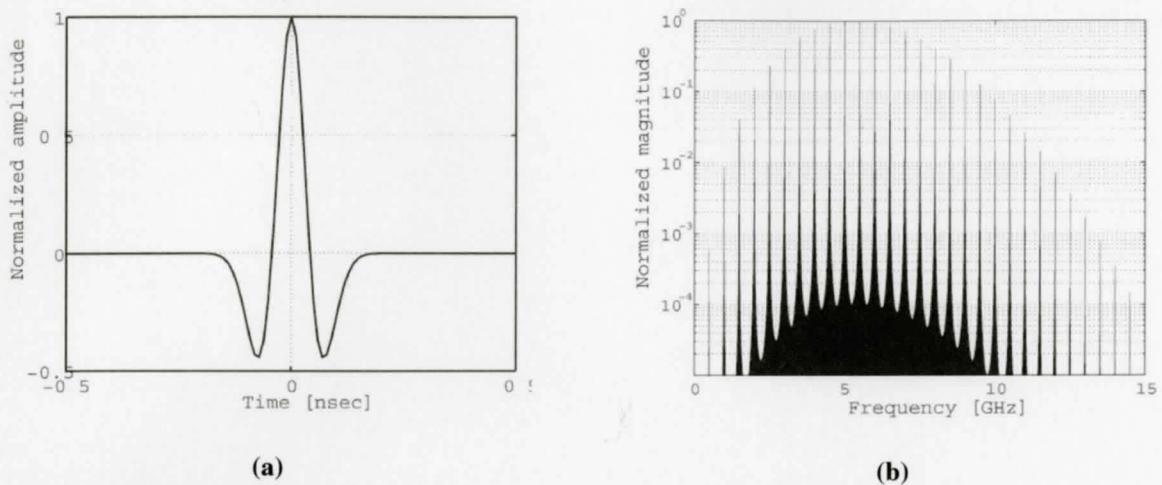


Figure 1.4: A normalized received UWB (a) pulse shape and (b) pulse train spectrum [2]

Depending on the pulse width and the modulation scheme used, the channel bandwidth is determined. One commonly used pulse modulation scheme is the pulse positioning modulation (PPM). The signal has some sort of pseudo-randomness (PR) to it. This, coupled with the fact that the transmitted signal must have low power, makes it appear as noise and hence be difficultly detected unintentionally. This is of particular interest to the military field for covert applications and in consumer electronics for increased security.

As hinted above, UWB signals must be low power. The reason can be arrived at starting from the elemental equation of Shannon's theory stated as:

$$C = B \log_2 \left(1 + \frac{S}{N} \right) \quad (1.1)$$

where:

C = the maximum channel capacity in bps

B = the channel bandwidth in Hz

S/N = the signal to noise ratio of the channel

High data rate wireless communications can be achieved by either increasing the channel bandwidth, increasing the signal strength or reducing the noise. The pulse example given in Figure 1.4(a) is typical of that which would be used. To convey information, a pulse train is needed and the corresponding frequency domain spectrum is shown in Figure 1.4(b). Here, it is clear that an UWB signal will require a large bandwidth extending from low frequencies to several gigahertz. The FCC classifies a system to be UWB if $B_f > 0.2$ where

$$B_f = 2 \frac{f_H - f_L}{f_H + f_L}, \quad (1.2)$$

and f_H, f_L are the high, low -10dB points and that the bandwidth must exceed 500 MHz. Providing a wide bandwidth is key for UWB to potentially achieve very high bit rates.

On the other hand, the required broadband poses a problem when it comes down to standardization and regulation. This large bandwidth will have to span many already allocated channels. The owners of these bands have paid to have exclusive use of these channels and must be convinced that UWB will not in any way interfere with their existing services. For this to be possible, the energy of the transmitted signal should be as small as possible, especially in consumer electronics. Hence, in UWB, the energy is spread over a wide bandwidth and thus the PSD is low. After the FCC proposed the UWB allocation, it got over 1000 written complaints from owners of bands constituted in the allocation [3]. Negotiations led to that the band be reduced to 7.5 GHz wide and the power would have to be very low. The FCC spectral mask for UWB is shown in Figure 1.5.

In contrast to narrowband, UWB does not operate at certain frequencies. The wide bandwidth and very low power levels make UWB transmissions appear as background noise much like in spread spectrum techniques. Because of the low power restriction, UWB is mostly limited to short range and indoor communications. The interference between the UWB signal with current RF narrow band systems is currently the most important topic under research today.

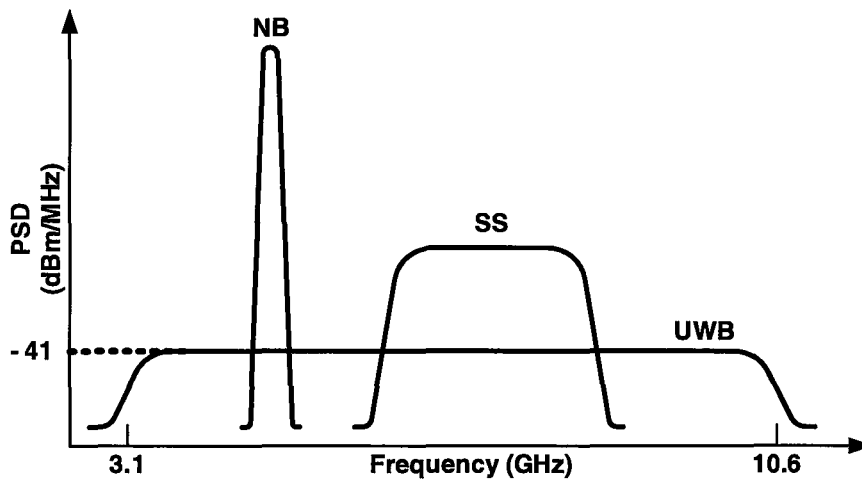


Figure 1.5: The UWB main target band

1.1.1.2. Applications and Uses

UWB systems have found use in a range of applications including, for example, impulse radar, automobile collision avoidance [4], medical imaging systems [5], positioning systems, liquid-level sensing, altimetry, and RFIDs (Radio Frequency Identification) [6]. In impulse radar and imaging, the narrow pulses lead to high resolution and the detection of fine details.

UWB deals with sending a great amount of data very quickly. This comes at the expense of the distance between the transmitter and receiver, with the exception of impulse radar that uses high power signals. The precise trade-offs are complex and

depend on the specific application. Table 1.1 gives a summary of different standards with their corresponding bit rates in comparison with UWB. The table shows three different UWB standards with different operational distances and the higher the bit rate the smaller the range. Practically, speeds exceeding 100 Mbps have been demonstrated and there is the capability of reaching even higher speeds over shorter distances. For example, a wireless UWB solution has been developed by Motorola achieving speeds exceeding 110 Mbps, power consumption of 750 mW, and 10 m range over the proposed band of 3.1 – 10.6 GHz using both 0.18 CMOS and SiGe technologies [7].

Table 1.1: Comparison of UWB bit rate with other wired and wireless standards

Speed (Mbps)	Standard
480	UWB (< 1 m), USB 2
200	UWB (4 m)
110	UWB (10 m)
90	Fast Ethernet
10	Ethernet
1	Bluetooth

1.1.2. Optical Communication Systems

A typical optical communications system consisting of a transmitter, channel, and receiver is illustrated in Figure 1.6. Optical communications systems have seen increasing deployment in recent years. Using fiber to guide optical signals, and optoelectronic devices to generate and receive signals, these systems promise to provide the required communications capacity.

Another advantage of these systems is the reduced cost resulting from requiring less repeater stations than other technology options. The capacity of a communication

system is measured by the BL product where B is the bit rate and L is the repeater spacing. Figure 1.7 compares the BL product for a number of technologies, and demonstrates the advantage of optical systems. Further improvements may be possible for completely optical systems that do not require optical-electronic conversions.

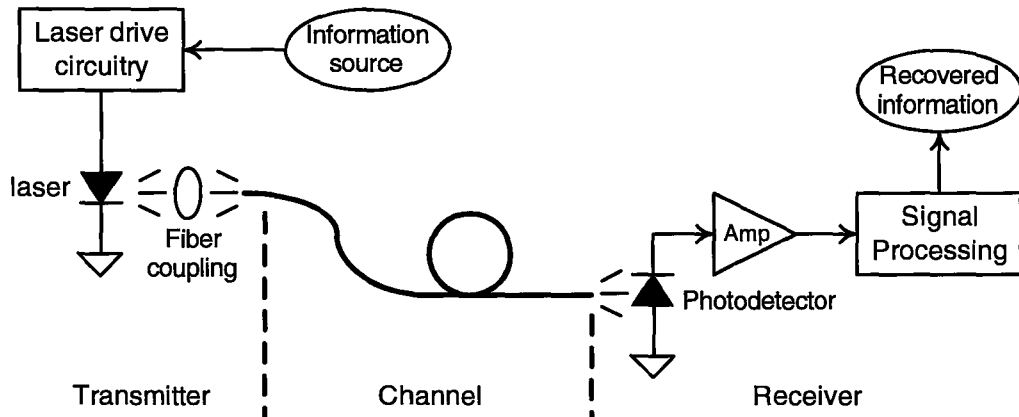


Figure 1.6: A typical high-level representation of an optical communications system

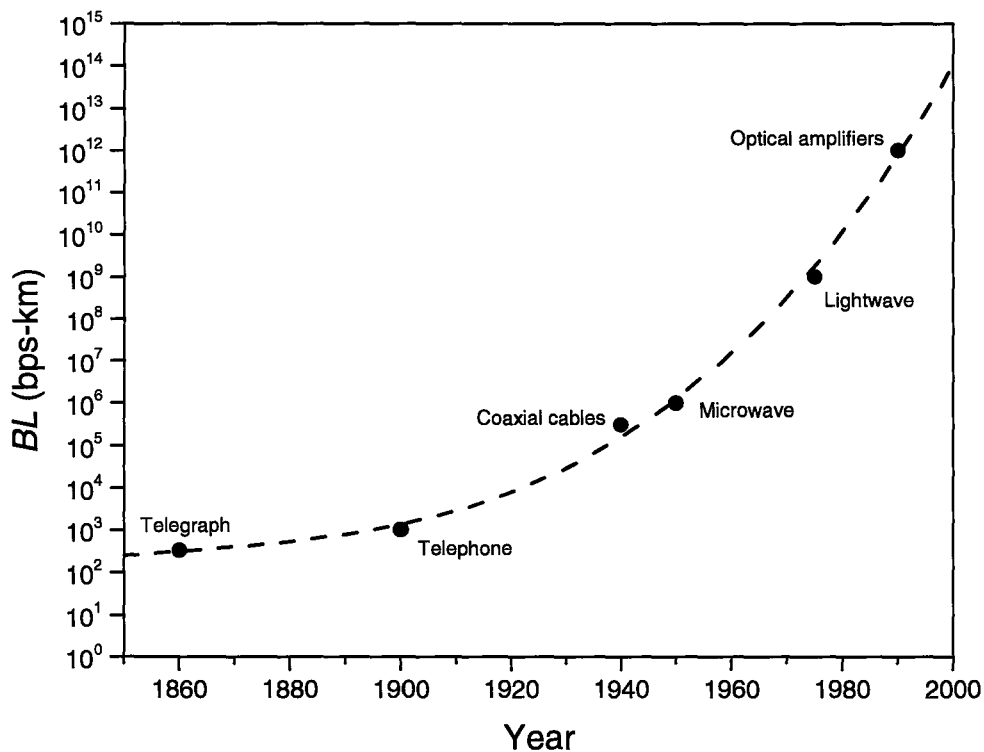


Figure 1.7: Increase in the bit rate-distance product throughout history [8]

1.2. Monolithic Systems

1.2.1. Definition

Circuit design at the high frequencies required for UWB and optical applications poses several challenges: transistors operate close to the cut-off frequency, the circuit is more sensitive to parasitics, model inaccuracies are more noticeable, and layout parasitics (resistive, capacitive and inductive) cause losses, mismatch and coupling/crosstalk that are significant at the operating frequencies.

Microwave integrated circuits may be hybrid or monolithic. In a hybrid microwave IC (HMIC), individual components are bonded to the substrate and connected by routing interconnections in a single metal layer on the substrate. In HMICs, the substrate material usually used is alumina, ceramic, quartz or Teflon. The material used depends on the frequency range of operation, area and rigidity constraints. The metallization used is usually copper or gold. The bonding of individual components is usually done manually and hence is the most costly part of the process. In thin film hybrid ICs, some of the simpler components are included on the substrate with more than one metallization layer, this makes this form more cost effective in some cases.

With the development of GaAs processing in the 1970s [9], came the advent of Monolithic Microwave ICs, or MMICs, wherein passive and active devices can be integrated in a semiconductor substrate with multiple metal layers, resistive films and dielectrics. This led to higher integration and lower manufacturing costs due to the reduction in manual labor. Since then, GaAs FETs have reached high frequencies of operation and have been used extensively in amplifiers, mixers, oscillators, etc. Silicon,

silicon-on-sapphire (SOS), and InP technologies have also been used. Front-end of line (FEOL) processing, operations performed on the semiconductor wafer in the course of device manufacturing up to first metallization, includes creating active regions, transistors, forming ohmic contacts, resistors and capacitors. After that subsequent metallization layers and vias are created in the back-end of line or BEOL. Inductors are formed during these processing steps.

1.2.2. Uses, Advantages and Disadvantages

Table 1.2 summarizes the contrast between HMICs and MMICs [10].

Table 1.2: Advantages and Disadvantages of MMICs

MMIC	HMIC
Cheap when complex circuits are mass produced	More convenient for simpler circuits
Very good reproducibility	Poor reproducibility due to device placement and bond wires
High reliability	Low reliability
Low manual labor	High manual labor involved
Expensive substrate making realization of on chip bulky inductors and transmission lines costly	Cheap substrate, which allows microstrip and lumped elements to be used abundantly
Very limited choice of devices and components	Vast selection of devices and components available
More stringent design procedure required to take into consideration losses, parasitics, and debugging	Design process simpler with less factors to worry about
Low quality factor and wide tolerance range in passive components	Off chip passive components have much higher quality factors and lower tolerances
Limited size and compact circuitry with poor heat dissipation capability leads to the restriction on power levels that can be used.	Typically good thermal transfer depending on the type of substrate

With scaling, integrated components reach high performance rendering MMICs as the technology of choice when it comes down to developing circuits operating at the high frequencies required. Moreover, a fully integrated MMIC is more desirable to reduce the effect of inductive losses introduced by packaging and hence achieving higher bandwidths. This will come more apparent in the following chapter dealing with high performance processes, SiGe in particular. Some other points worth mentioning on MMICs is that the more layers added the more expensive the process becomes due to the increase in processing steps and masks needed to be generated. One final note is that MMICs are evolving to become millimeter-wave integrated circuits and now photonic integrated circuits that can be used in optical communication systems.

1.3.Scope and Organization

The focus of this thesis is distributed amplifiers implemented in silicon germanium (SiGe) technology. As we have emphasized in the preceding sections, there is much interest in ultra-wideband and optical systems to meet high bandwidth requirements for an increasing variety of applications. Regardless of the particular application, and for both the electronic and the optoelectronic solution, an electronic ultra-wideband amplifier is an essential requirement. Such an amplifier has a gain-bandwidth (GBW) product requirement in the tens to hundreds of gigahertz, exceeding the cut-off frequencies of most devices, and necessitating the use of multi-stage amplifier architectures [11], [12]. Even with the use of multiple stages, the speed of each stage needs to be optimized since chip area and cost are directly proportional to the total number of stages required. An ultra-wideband (UWB) amplifier design therefore requires

both the optimization of the gain cell, and an architecture that provides the required GBW. In addition, as outlined in the last section above, a monolithic implementation is strongly preferred to reduce cost and size of the complete system. In this thesis we address each of the three aspects: (1) the cell design is optimized using fast SiGe HBT's; (2) the DA architecture is characterized in terms of its performance, as well as its thermal and noise characteristics; and (3) we optimize the performance of the circuit under the constraint of using all on-chip components to produce a monolithic design.

The thesis is organized to adequately explore these aspects. Chapter 2 addresses the technology platform used. We briefly describe the operation of Heterojunction Bipolar Transistors (HBTs) and in particular SiGe HBTs. We describe the material properties of SiGe and the promise of SiGe technology for MMICs compared with other technologies. Finally, a portion of the chapter is dedicated to briefly explain the HBT equivalent circuit and important model parameters.

The theory of operation of a distributed amplifier (DA) is detailed in Chapter 3. This chapter will also review previous work utilizing this technique, with special emphasis on SiGe implementations.

Chapter 4 details our design, and provides measurement results for the fabricated circuit. We discuss and analyze the simulations and measurements, and characterize the thermal behavior of the circuit.

Chapter 5 is concerned with the noise analysis of a distributed amplifier and that of SiGe HBTs. We provide a model of the noise performance of a DA using HBTs, and compare the predictions of the model with both simulations and measurements.

Conclusions, contributions, and future work are summarized in Chapter 6.

Chapter 2

SILICON GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTORS

2.1. Silicon Germanium

The last decade has witnessed significant growth in research interest and market share captured by silicon germanium (SiGe) technology. To fully appreciate its impact and the interest in it, the benefits of SiGe technology must be understood in the context of two alternatives: silicon (Si) and compound semiconductors. Silicon is by far the dominant semiconductor material in the microelectronics industry. Advantages that have led to such dominance are numerous (see, e.g., [13] and references therein), but the

bottom line that all those factors impact is manufacturability, and the resulting cost per function. The most dominant Si technology has been Complementary Metal Oxide Semiconductor (CMOS) technology. Despite the speed advantages of bipolar circuitry, CMOS has dominated because of its scalability, again resulting in lower cost per function, and its low-power properties for digital ICs.

The primary weaknesses of CMOS are its low carrier mobility and its indirect bandgap. This has allowed other Si technologies and non-Si materials to succeed in niche applications. III-V compound semiconductors such as GaAs and InP provide higher carrier mobilities and have direct bandgaps making them ideal for microwave and optical applications. Ternary compounds such as AlGaAs allow bandgap engineering, the customization of material properties, including the energy bandgap, by varying the composition. Figure 2.1 depicts how III-V semiconductors monopolize high-frequency applications.

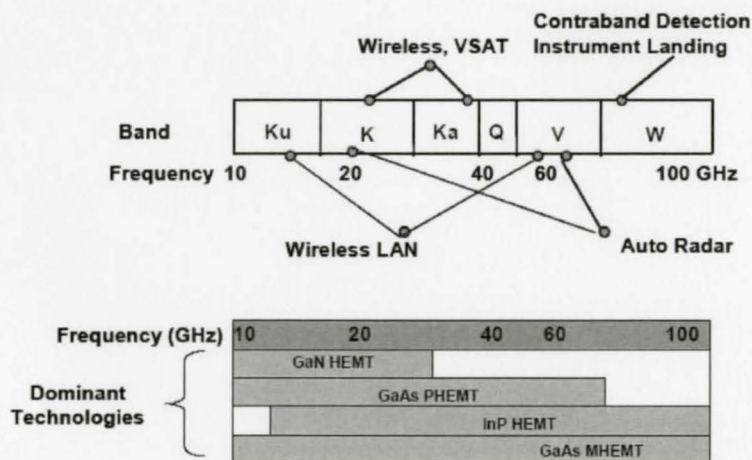


Figure 2.1: Millimeter wave commercial applications and technologies spanning 10 – 100 GHz [14]

Yet, III-V semiconductors have their share of disadvantages. GaAs and InP, for instance, have no thermally grown oxides, have more defects than Si, and wafers are

more brittle, limiting the size at which they may be fabricated. Moreover, they display thermal properties inferior to Si. All these problems render III-V component circuits more difficult to fabricate, producing lower yield and hence higher cost. The appeal of SiGe technology is that it offers some of the advantages of compound semiconductors in a process that is compatible with existing CMOS processing. The compatibility with CMOS processing allows manufacturers to incorporate SiGe technology in the same fabrication facility and using the same equipment used for their pure CMOS products. The resulting cost increment of introducing SiGe into the Si production line is estimated to be no more than 30% [15].

SiGe is a crystalline alloy of the two elements, silicon and germanium (Ge). The properties of the alloy are determined by its composition. Silicon has a slightly smaller lattice constant than germanium causing the SiGe lattice to be compressively strained when grown on a Si substrate as shown in Figure 2.2. The compressive strain alters the band structure enhancing the carrier mobilities, which are already higher than mobilities in pure Si because of the presence of Ge [13]. All this makes bandgap engineering possible, allows for heterojunction devices, and hence enables higher frequency operation suitable for RF and microwave applications. Figure 2.3 shows the evolution of mixed-signal technologies and how SiGe offers a bridge between conventional Si and exotic III-V compound semiconductors.

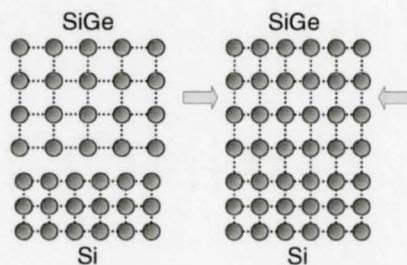


Figure 2.2: 2-D demonstration of strained SiGe on a Si substrate

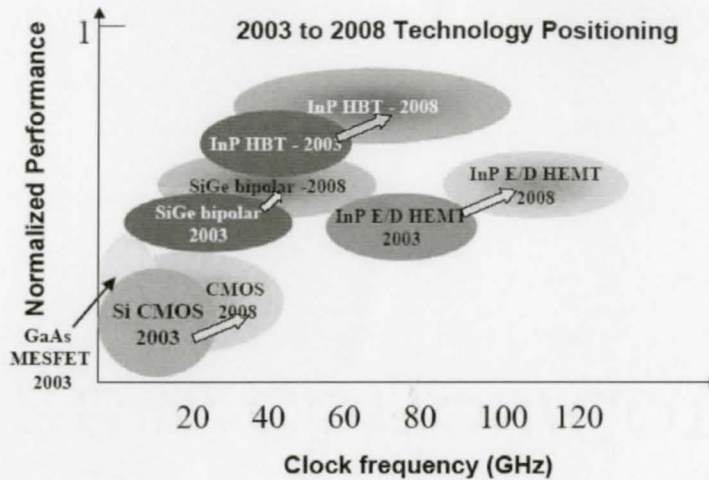


Figure 2.3: Evolution of mixed-signal technologies. Metric used includes dynamic range, signal-to-noise ratio, bandwidth, data rate, and power [14]

2.2. SiGe Heterojunction Bipolar Transistors

A heterojunction bipolar transistor (HBT) is a bipolar transistor where the base is made of a different material than the emitter and collector [13]. The schematic cross-section of a typical SiGe HBT is shown in Figure 2.4. Note that the base is made of a strained SiGe layer whereas the emitter and collector are pure silicon. A cross sectional SEM is shown in Figure 2.5.

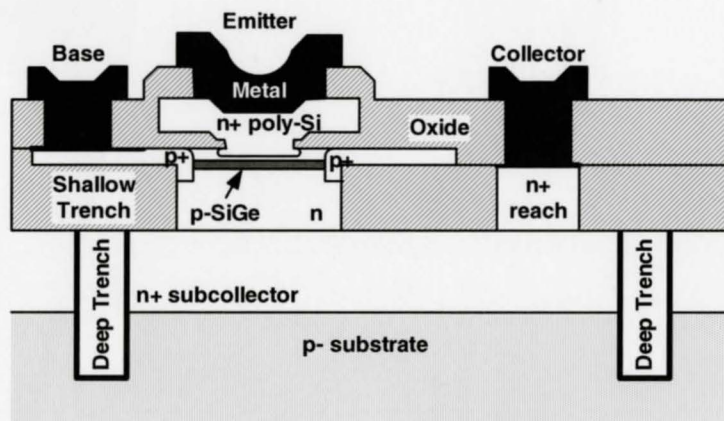


Figure 2.4: Schematic cross-section of a SiGe HBT [13]

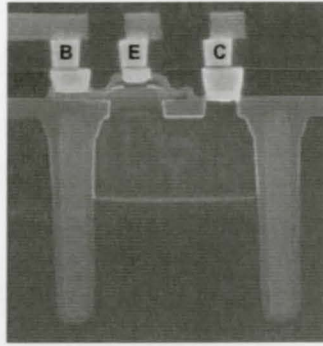


Figure 2.5: Cross-section SEM of a SiGe HBT [16]

Figure 2.6 shows the typical concentration profiles for the Ge and the base dopant (usually boron), as well as the resulting band structure. Because Ge has a lower bandgap than Si (0.7 eV as opposed to 1.1 eV), the bandgap decreases as the Ge fraction increases. This results in a sloped conduction band edge as shown in the figure, which in turn results in further acceleration of electrons as they traverse the base region. Hence, electrons in the base have their speed enhanced by three separate effects: the higher mobility of electrons in SiGe, the increased mobility because of compressive strain, and the increased velocity because of the slope of the conduction band edge. The combination of these effects reduces the base transit time. As a result, the transistor has a higher current gain, β , a higher cut-off frequency, f_T , and a higher maximum oscillation frequency, f_{max} .

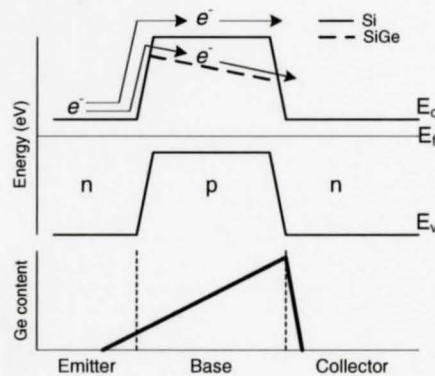


Figure 2.6: Energy band diagram of SiGe and Si-base transistors

The cut-off frequency, f_T , is defined as the frequency at which the common emitter current gain of the transistor drops to 1. It is given by:

$$f_T = \left[\frac{1}{g_m} (C_{be} + C_{cb}) + \tau_b + \tau_e + \tau_c \right]^{-1} \quad (2.1)$$

where g_m is the transistor transconductance, C_{eb} and C_{cb} are the emitter- and collector-base capacitances respectively, and τ_b , τ_e , τ_c are the base, emitter, collector transit times respectively.

The maximum oscillation frequency, f_{max} , is a more important parameter for RF applications. This is because it takes into consideration not only the internal delay of the device, but also the parasitic elements associated with the device physics and structure. f_{max} is given by:

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{cb} R_{bx}}} \quad (2.2)$$

where R_{bx} is the extrinsic base resistance.

Considering equations (2.1) and (2.2) and referring again to Figure 2.6 highlights additional advantages of using SiGe in the base. The presence and grading of Ge in the base lowers the barrier to electron injection from the emitter while keeping the barrier to hole injection high. This improves the emitter injection efficiency, hence resulting in higher β , f_T , and f_{max} . Finally, the conductivity of SiGe is higher than that of Si, and hence R_{bx} is reduced. This further increases f_{max} .

The inherent advantages of using SiGe outlined above, coupled with R&D efforts to optimize the fabrication process and scaling of successive technology generations has resulted in SiGe HBTs with cut-off frequencies in excess of 100 GHz in commercially

available product lines. Figure 2.7 shows the increase in β and f_T as SiGe HBTs have scaled according to the International Technology Roadmap for Semiconductors (ITRS) [14]. In Figure 2.7, the markers represent the minimum requirements identified in the ITRS, and the solid lines show overall trends.

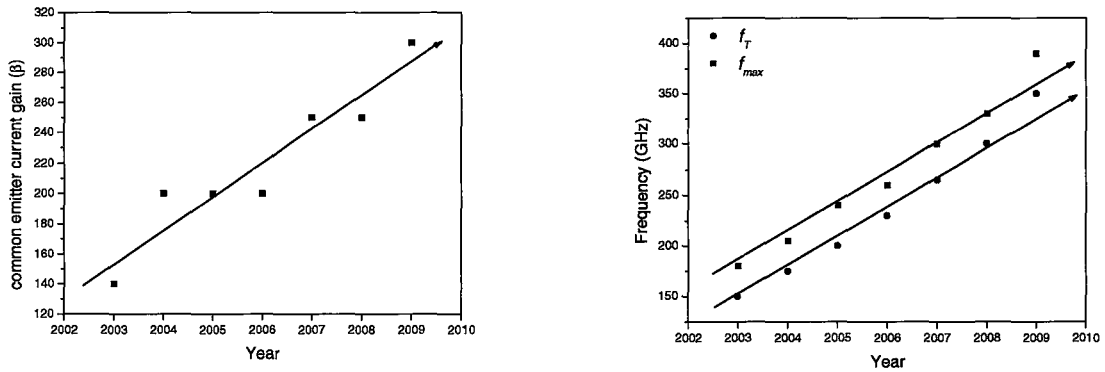


Figure 2.7: Increase trends of β and f_T and f_{max} with scaling over the years [14]

2.3. Properties of the IBM SiGe5AM Process

The design discussed in this thesis utilizes the IBM SiGe5AM process made available through the Canadian Microelectronics Corporation (CMC). Currently the IBM SiGe BiCMOS process has four lithographic generations, all of which are compatible with the associated IBM CMOS technology in terms of devices and interconnection metallization [17]. Figure 2.8 shows the steady improvement of f_T versus I_C for the IBM SiGe BiCMOS generations currently available. The most advanced of these technologies has performance that is competitive with some III-V compounds.

The SiGe 5AM and 5HP processes are 0.5 μm processes with a peak f_T of approximately 50 GHz. The 5AM process is an extension to the predecessor 5HP incorporating a thick top level metal layer suitable for analog applications. The 5AM

process can have 4, 5 or 6 levels of metallization, the last of which is the analog metal. Figure 2.9 shows the cross section of a 4 metal 5AM process. The thick analog metal allows the realization of inductors with quality factors in excess of 10. Additionally, the AM process provides scalable octagonal inductors that are useful for RF applications.

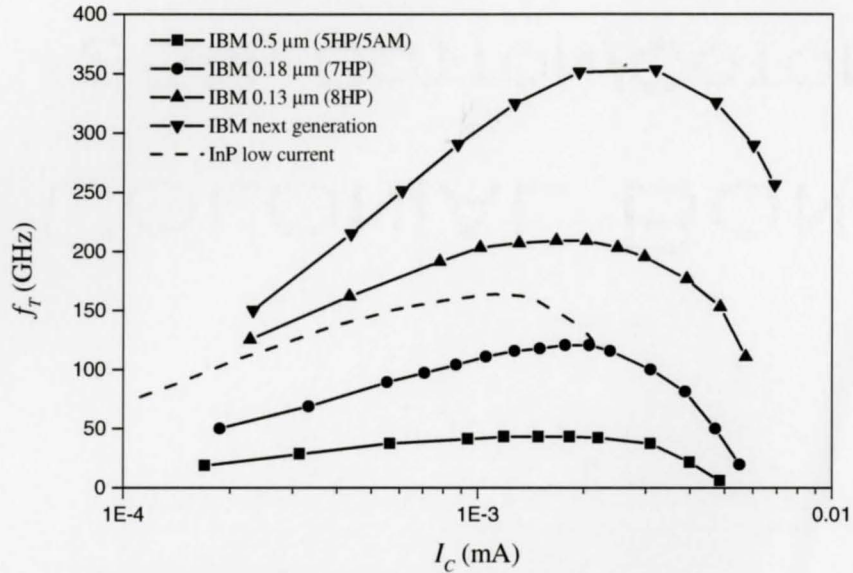


Figure 2.8: f_T vs. I_C of the different IBM SiGe BiCMOS generations [17], [18]

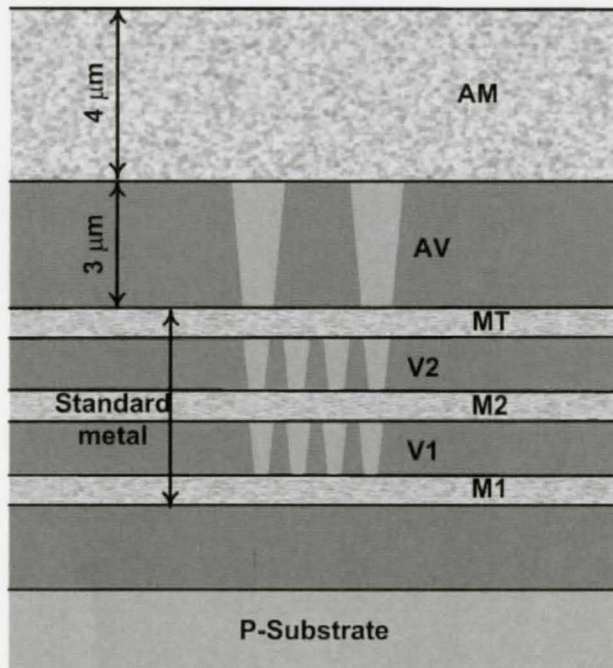
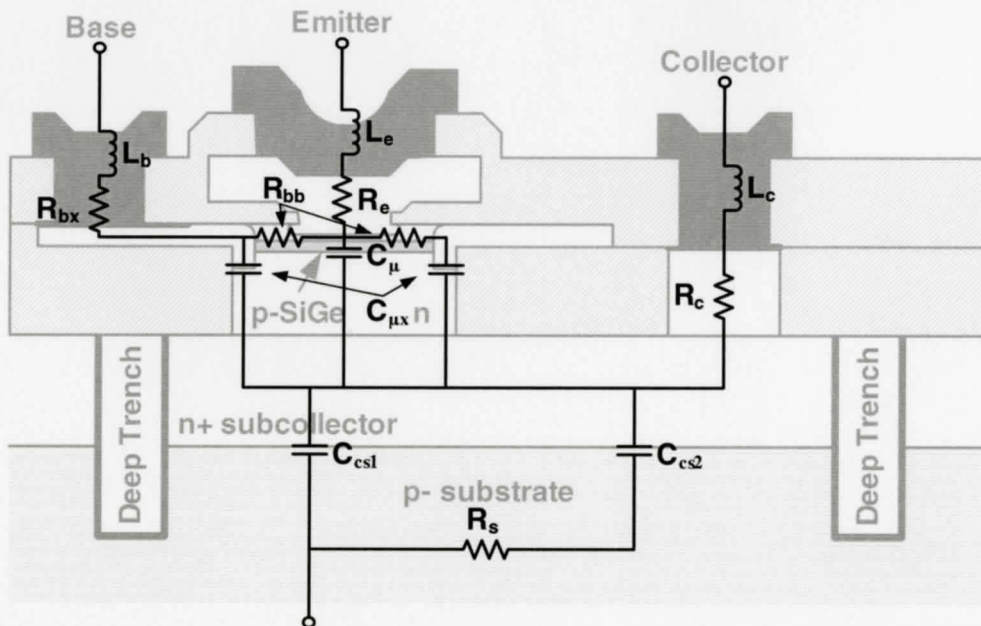


Figure 2.9: Cross section of SiGe5AM metals and vias [19]

2.4. Equivalent Circuit and Important Parameters

As the frequency at which transistors are expected to operate increases, it becomes increasingly important to be able to isolate and quantify the different parasitics and device parameters. Such parameters are needed in order to be able to accurately predict circuit performance. Accurate, predictive circuit simulation is clearly the key to enabling performance optimization without necessitating fabrication of successive prototypes, a process that would be very costly.

Figure 2.10 shows the physical significance of the elements of the small-signal equivalent circuit of an HBT, which is similar to that of a conventional bipolar transistor, differing mainly in the values of some of the parameters related to the SiGe base and the poly-Si emitter. The dashed line in Figure 2.10(b) encloses the elements usually included in simulator models.



(a)

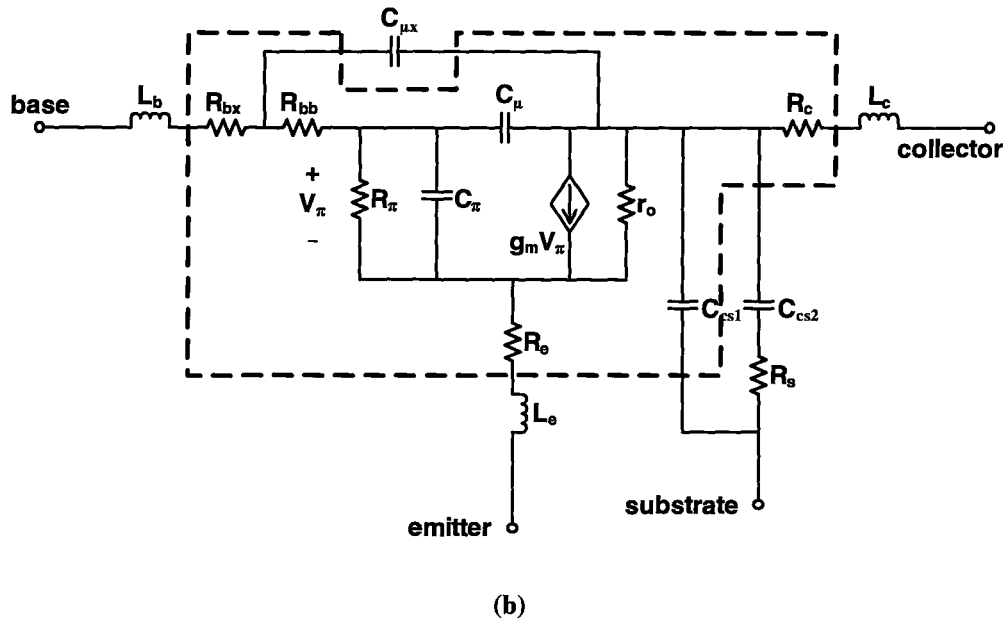


Figure 2.10: (a) Physical significance of the elements in the (b) small signal equivalent circuit of an HBT

While the model of Figure 2.10 may appear complex, the level of complexity and the number of components shown are necessary to capture effects that become significant in high frequency applications. The paragraphs below discuss each element shown in the equivalent circuit shown in Figure 2.10(b) with the assistance of the physical representation depicted in Figure 2.10(a).

Electrons are injected into the base through the base-emitter junction. The capacitance of the junction, C_{π} , can be decomposed into two components: a depletion region capacitance due to space charge made up of dopant ions, and a diffusion capacitance due to the electron charge stored in the base region. The diffusion resistance, R_{π} , describes the relationship between the current and voltage signals across the diode formed by the base-emitter junction.

The base current flows through the extrinsic base resistance, R_{bx} , which connects the base metal to the intrinsic base. This current charges the distributed extrinsic base-

collector capacitance, $C_{\mu c}$. This part of the base resistance is independent of bias. In the forward active mode, the majority of the signal goes through the active, or intrinsic base region immediately below the polysilicon emitter through the intrinsic base resistance, R_{bb} . In general, the value of the base resistance depends on the base active region dimensions and the doping level [20]. Along with $C_{\mu c}$, a second capacitive component is required to model the base-collector junction capacitance. This additional component is termed the intrinsic base-collector capacitance, C_{μ} .

At the collector, g_m represents the transconductance, which is frequency dependent. The output resistance, r_o , represents the change in the collector current with V_{ce} due to the Early effect. This is usually very large in SiGe HBTs and can be neglected. The depletion capacitance due to the collector-substrate junction is distributed in nature and can be modeled by two parts, C_{cs1} and C_{cs2} with the former attributed to the junction beneath the buried layer and the active region. R_s models the distributed substrate resistance.

Finally, R_e and R_c model the resistance of the polysilicon emitter and collector respectively. L_e , L_b , and L_c are series inductances due to the respective metallization contacts to the emitter, base, and collector. Their values are independent of bias.

Chapter 3

DISTRIBUTED AMPLIFIERS

3.1. DA and TWA Principle of Operation

Broadband amplifiers trace their development to video amplifier design in the UHF band for video applications in the early and mid twentieth century [21]. To achieve uniform gain over the required band with minimal distortion, designers resorted to multistage architectures. The simplest multistage design is the cascade amplifier, where the overall gain is the product of the gains of the individual stages. However, the performance of the cascade amplifier is limited by the increased shunt capacitance. The gain-bandwidth product (GBW) of a cascade amplifier is tied to the intrinsic gain and capacitance of the gain cell:

$$GBW \propto \frac{G}{C} \quad (3.1)$$

where G is the active device gain and C is the effective shunt capacitance. The GBW product of a single stage is constant as, for a certain bias, the gain may be increased by increasing the transistor size which, in turn, increases the parasitic capacitances, hence nullifying the improvement achieved in the gain. Moreover, as shown in Figure 3.1, while the total amplifier gain increases as stages are added in a cascade fashion, the shunt capacitances are additive, resulting in the reduction of bandwidth of the single stage and consequently the entire amplifier, hence resulting in a trade-off between gain and bandwidth in the entire configuration. Percival [22] proposed adding inductive elements in between stages to ‘absorb’ this capacitive effect. Ginzton et al. [23] implemented this for the first time in 1948 using thermionic valves and the term Distributed Amplification was coined. Considerable research and development followed, with GaAs FET-based distributed amplifier MMICs debuting in 1981 [24].

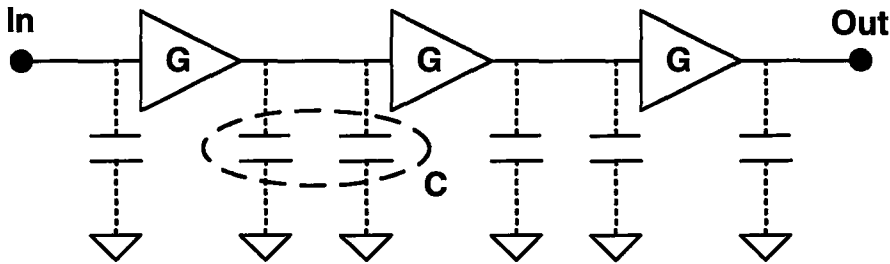


Figure 3.1: Cascade amplifier with accumulated capacitance effect

Figure 3.2 illustrates the concept by which DAs operate. A set of amplification stages are connected together, not directly as in cascade amplifiers, but separated by inductive transmission lines at both the input and output. The inductive elements may be as spiral inductors, coplanar waveguides, microstrip lines, or other alternate components.

Even though the terms distributed amplifier and traveling wave amplifier (TWA) are often used interchangeably, DA is usually used when the lines are composed of discrete elements and TWA is used otherwise. Regardless of the inductive element used, the stages are separated by transmission line-like segments. The signal enters the input line and is tapped periodically by the gain cells as it traverses down the line. The termination load, Z_o , is chosen to match the line and absorb the remainder of the signal preventing it from reflecting back onto the line and causing destructive interference. In each gain cell, the sampled signal is amplified and coupled to the output line through the gain cell transconductance. The fundamental design principle of the DA is to design the input and output transmission lines such that the signals propagating down the two lines remain in phase. This ensures constructive interference of the amplified signals on the output line and hence the total gain is increased through the contributions from successive gain cells.

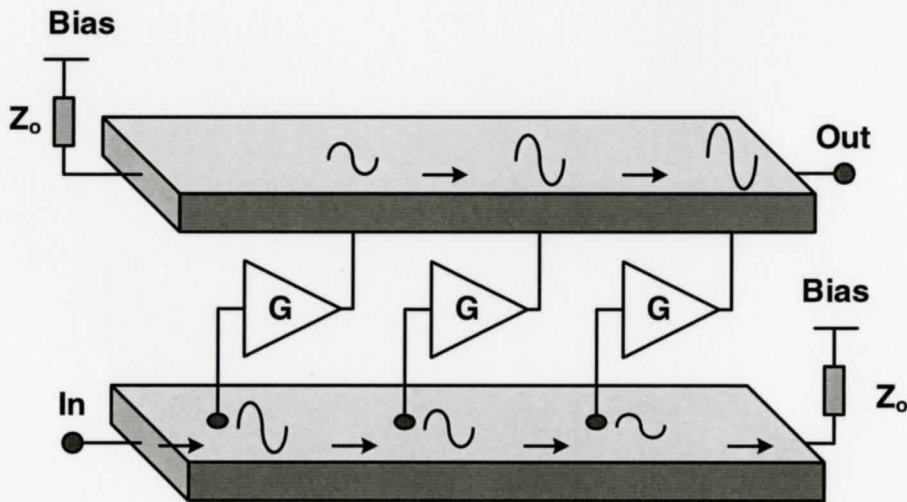


Figure 3.2: Distributed amplifier consisting of two transmission lines

Figure 3.3 shows the equivalent circuit of a DA using a common emitter gain cell, where we have used a simplified unilateral lossless transistor equivalent circuit. Z_b and Z_c terminate the base and collector lines (i.e. the input and output lines) respectively. L_b and

L_c are sized such that matching and phase equality are maintained on both lines. It can be shown that the low-frequency, total gain of such an amplifier, assuming zero losses and equal base-collector phase matching is given by [9]:

$$G_T = \frac{g_m^2 Z_b Z_c n^2}{4} \quad (3.2)$$

where g_m is the transconductance gain of the transistor and n the number of stages. One obvious disadvantage of DAs, apparent from the previous equation, is that the gain is proportional to the square of the transconductance instead of $(g_m)^n$ as would be achieved in cascade amplifiers. Hence DAs display lower gain than cascade amplifiers for the same number of stages. In practice, the limitation is even more severe because of losses. Real input and output lines are lossy due to the input and output resistances of the transistors and the limited quality factor of the inter-stage transmission lines. Hence, the signal amplitude attenuates as it propagates down the base line, as schematically shown in Figure 3.2. This gives rise to a maximum in the gain as a function of the number of stages. The optimum number of stages can be determined from [25]:

$$n_{opt} = \frac{\ln(\alpha_c / \alpha_b)}{\alpha_c - \alpha_b} \quad (3.3)$$

where α_b and α_c are the base and collector line attenuations respectively. Line attenuation is due to the series resistance in line inductors and the loading effect of the transistors. The addition of any stages above the optimum number may result in higher gain at DC and low frequencies but the gain degrades at higher frequencies at which attenuation effects are more severe [26].

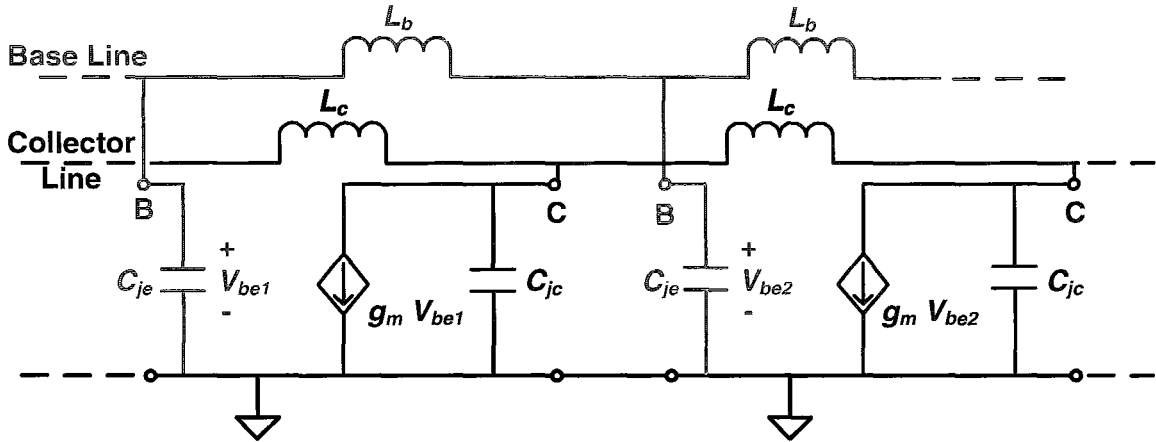


Figure 3.3: Transmission line circuits of DA using simplified BJT equivalent circuit

From the previous analysis, it becomes clear that DA's, unlike cascade amplifiers, do not trade off gain with bandwidth. Rather, the trade-off in DAs is between the gain and the delay the amplifier introduces into the system, since both gain and delay are proportional to the number of stages. Delay is significant because non-linearity in the phase of the gain within the pass band will result in signal distortion. Gain linearity is equivalent to a constant group delay, GD, where the group delay is defined as:

$$GD = -\frac{\partial \angle S_{21}}{\partial \omega} \quad (3.4)$$

where $\angle S_{21}$ is the phase of the gain in radians.

The remainder of this chapter discusses DA design. Section 3.2 discusses two approaches to design flowing from the choice of method of realization of the transmission line. Section 3.3 gives a survey of previous work.

3.2. Realizations of the Transmission Line

The procedure followed to design a distributed amplifier depends on what approach is used in realizing the transmission line: using discrete inter-stage elements or

treating the problem as periodically loaded uniform transmission lines. Both methods are discussed below, followed by a discussion of components that may be used in MMICs to realize these transmission lines.

3.2.1. Artificial Transmission Lines (ATLs)

In the previous section, the general configuration of a DA is shown to be comprised of two transmission networks – the base and collector lines. These lines are decoupled and redrawn in Figure 3.4. C_b and C_c represent the base-emitter and base-collector junction capacitances respectively. These capacitances, along with the inductances $L_b/2$ and $L_c/2$ are repeated throughout the structure and can be grouped into periodic unit cells outlined by the dotted boxes. The unit cell resembles the lumped-element equivalent circuit of an increment of a transmission line and hence the repeated structure is called an artificial transmission line. The unit cell of both lines is in fact a constant- k low-pass filter section as shown in Figure 3.5(a). The filter section operates when the input and output impedances it sees are of a certain value called the image impedance, which is determined by the inductances and capacitances in the line. The image impedance, by definition, is the impedance the individual section, and the entire line, must see at both ends to ensure maximum power transfer and is given by [9]:

$$Z_{ib} = \text{image impedance of base line} = R_{ob} \sqrt{1 - \frac{\omega^2}{\omega_{c,b}^2}}, \quad (3.5)$$

$$Z_{ic} = \text{image impedance of collector line} = R_{oc} \sqrt{1 - \frac{\omega^2}{\omega_{c,c}^2}}, \quad (3.6)$$

where

$$R_{ob} = \text{constant} = \sqrt{\frac{L_b}{C_b}}, \quad (3.7)$$

$$R_{oc} = \text{constant} = \sqrt{\frac{L_c}{C_c}}, \quad (3.8)$$

$$\omega_{c,b} = \text{cut-off frequency of base line} = \frac{2}{\sqrt{L_b C_b}}, \quad (3.9)$$

and

$$\omega_{c,c} = \text{cut-off frequency of collector line} = \frac{2}{\sqrt{L_c C_c}}. \quad (3.10)$$

As mentioned previously, the phase of both lines must be equal for amplification and this is only achieved when $\omega_{c,b} = \omega_{c,c} = \omega_c$. Since the output capacitance of a transistor is usually smaller than the input capacitance, an additional capacitor is usually added across the output to achieve phase matching. It can be seen from equations (3.5) and (3.6) that the image impedance is frequency dependent. With this in mind, the DA gain equation can be rewritten as [24]:

$$G_T = \frac{g_m^2 R_{ob} R_{oc} n^2}{4 \cdot (1 - \omega^2 / \omega_c^2)} \quad (3.11)$$

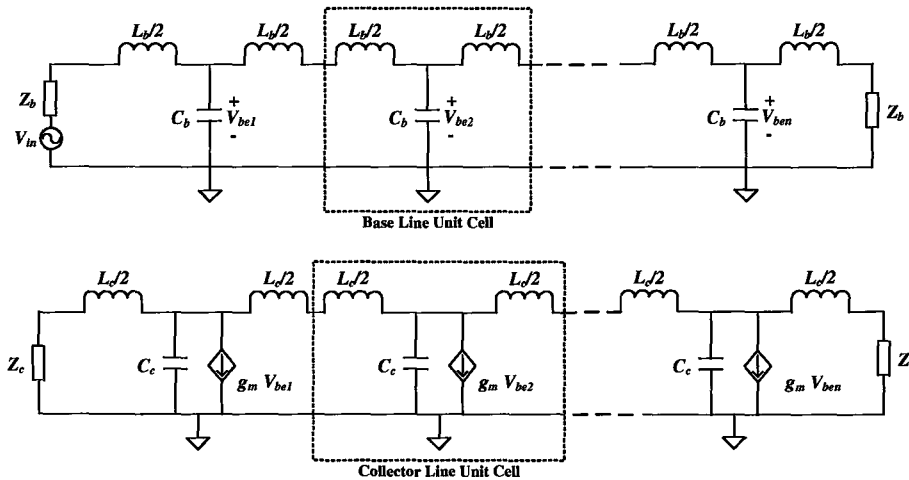


Figure 3.4: Idealized equivalent base and collector lines of a distributed amplifier

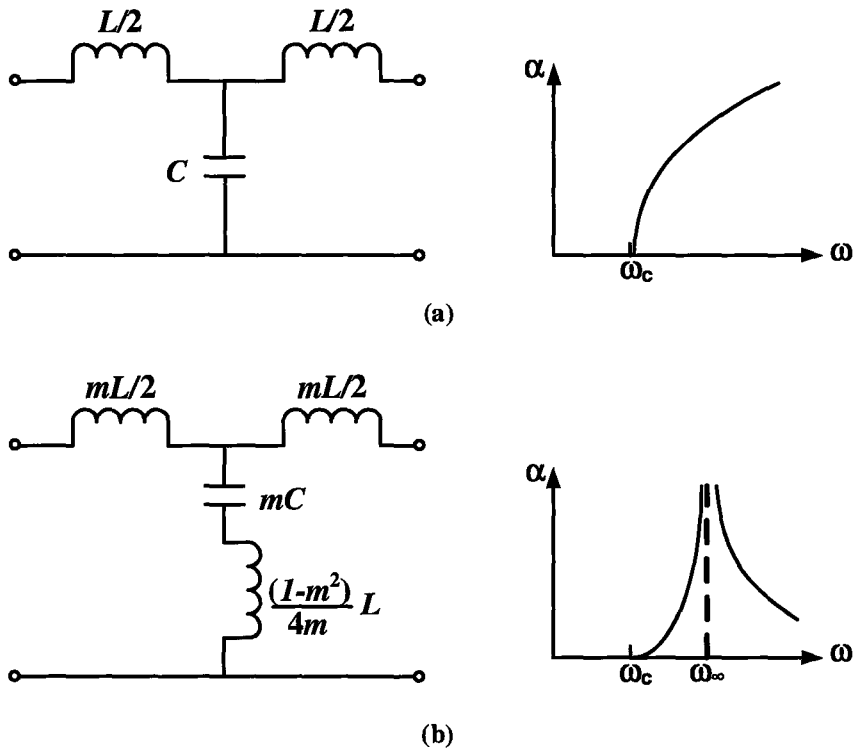


Figure 3.5: (a) constant- k and (b) m -derived low-pass filter sections

Equation (3.11) shows that there is a pole in the gain at the cut-off frequency. This may result in the undesirable effect of gain peaking, which will compromise the gain flatness. Some previous designs have alleviated this problem by allowing for a slight mismatch between the lines cut-off frequencies i.e. $\omega_{c,c} \neq \omega_{c,b}$, a technique called staggering [27]. Even though this may be an issue in III-V DAs, it may be desirable in technologies with lossy substrates such as CMOS and SiGe BiCMOS. With lossy substrates, the gain falls considerably at high frequencies thus making this peaking effect desirable to boost the gain at higher frequencies.

The constant- k filter sections shown in Figure 3.5 have a few disadvantages. First, the attenuation in a line consisting of such sections rises slowly after the cut-off frequency leading to slow roll-off of gain beyond cut-off. Second, and more important,

the image impedance is frequency dependent, which poses a problem when matching the lines to the terminations that are in general fixed at $50\ \Omega$. These problems are solved by using m -derived filter sections.

A low-pass m -derived filter section is similar to a constant- k section, but with an extra inductor in the shunt arm, as shown in Figure 3.5(b). The series inductor value is changed from L to mL where m has a value from 0 to 1. To keep the image impedance equal to that of a constant- k filter, the values of the capacitor and the added inductor in the shunt arm must be sized as shown in Figure 3.5(b). As a result, the cut-off frequency also remains the same as in the constant- k filter, but a pole is introduced in the attenuation at a frequency, ω_∞ , as shown in Figure 3.5(b), and is given by:

$$\omega_\infty = \frac{\omega_c}{\sqrt{1-m^2}} \quad (3.12)$$

The closer ω_∞ is to ω_c , the more abrupt the attenuation rise and the sharper the gain roll-off is. This is controlled by selecting the appropriate m , with smaller values producing steeper roll-offs. For $m = 1$, the filter characteristics reduces to that of a constant- k filter. Note that the closer m is to 0, the larger the shunt arm inductors would be, and hence larger chip areas are needed.

While an m -derived filter section addresses the problem of gradual gain roll-off, its image impedance is identical to that of a constant- k filter so this does not address the varying impedance problem. This issue is resolved by using an m -derived bisected π -matching section as illustrated in Figure 3.6. As shown in the figure, the value of m affects the variation of the image impedance as a function of frequency, and it is possible to select m such that the image impedance seen by the line is matched to an

approximately constant value, R_o . The value of $m = 0.6$ was found to give minimum variation over the intended frequency band [9]. Figure 3.7 shows a complete 3-stage DA consisting of CE gain cells and matching sections on both input and output artificial transmission lines.

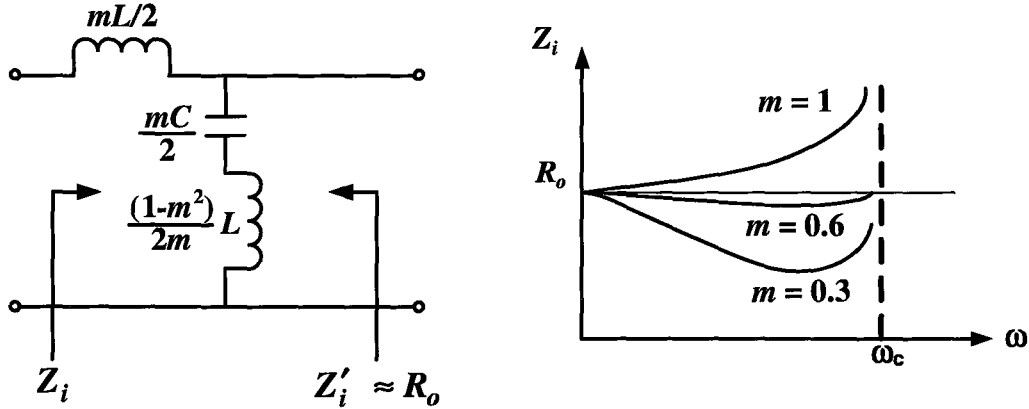


Figure 3.6: Low-pass m -derived bisected π -section and corresponding output impedance with m variation

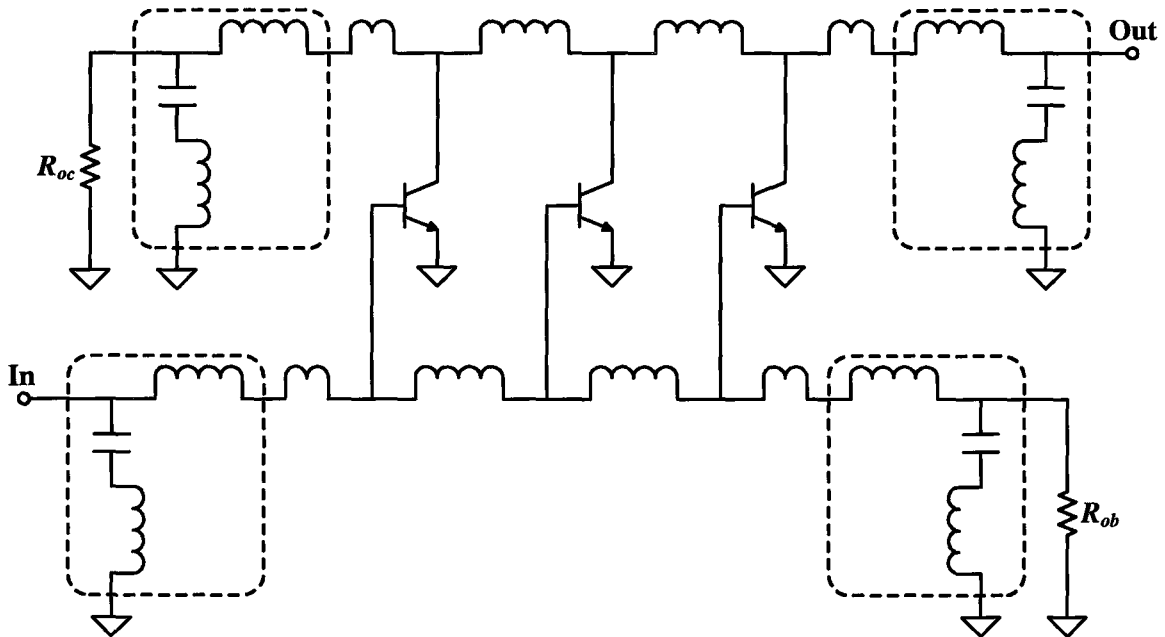


Figure 3.7: 3-stage DA with matching filters, enclosed in dotted boxes, on both input and output lines

3.2.2. Periodically Loaded Transmission Lines

Using planar transmission components, it is possible to design a monolithic TWA using on-chip transmission lines. Figure 3.8 shows a 3-stage TWA utilizing transmission lines and using CE gain stages. The base line consists of lengths of transmission lines, l_b , with characteristic impedance Z_b and propagation constant β_b . The same terminology follows for the collector line. The unit cell equivalent circuit is shown in Figure 3.9 for an arbitrary line where L is the inductance per unit length and C the capacitance per unit length. C_{be}/l_b and C_{cb}/l_c represent the equivalent per unit length loading on the base and collector lines due to the junction capacitances of the transistor.

The condition for proper operation here is the same as in the case of distributed amplifiers: phase matching. In this case, the phase matching condition may be written:

$$\beta_b l_b = \beta_c l_c, \quad (3.13)$$

where

$$\beta_b = \omega \sqrt{L_b \left(C_b + \frac{C_{be}}{l_b} \right)}, \quad (3.14)$$

and

$$\beta_c = \omega \sqrt{L_c \left(C_c + \frac{C_{cb}}{l_c} \right)}. \quad (3.15)$$

To observe proper impedance matching the characteristic impedance of the loaded transmission lines must be equal to the termination impedance. The characteristic impedance of each line is given by:

$$Z_b = \sqrt{\frac{L_b}{C_b + C_{be}/l_b}}, \quad (3.16)$$

and

$$Z_c = \sqrt{\frac{L_c}{C_c + C_{cb}/l_c}}. \quad (3.17)$$

The transmission line unit inductance and capacitance are fixed for a certain configuration. What remains is the selection of line lengths for the base and collector lines such that phase and impedance matching are maintained. As in DAs, extra capacitors may be added to the transistor outputs to equate both input and output capacitances and consequently identical lines can be used for both input and output.

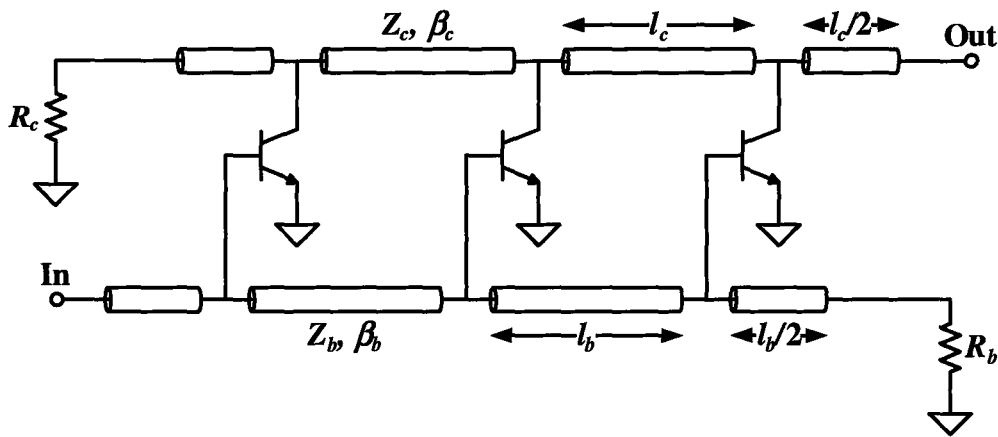


Figure 3.8: A 3-stage traveling wave amplifier

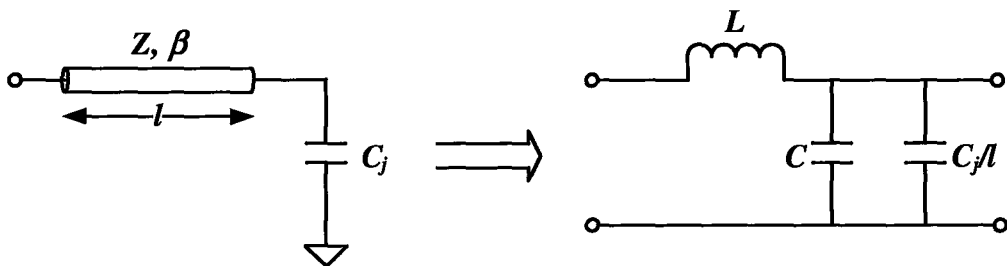


Figure 3.9: Equivalent circuit of a single unit cell of either line where C_j is the equivalent junction capacitance

There are a few advantages to the use of transmission lines in TWAs, as opposed to discrete elements in DAs. GaAs devices are fabricated to be compatible with planar waveguide technologies making interfacing easy. Another advantage is that the lines used

are designed to have characteristic impedances required for matching, which is approximately constant with frequency and hence no matching sections, as in DAs, are required. Nonetheless, when considering non-III-V technologies, such as CMOS and SiGe BiCMOS, several disadvantages emerge. First, transmission lines are dissipative and dispersive in nature, which poses a problem when implemented in lossy substrate technologies yielding relatively low quality passive devices. Also, it has been shown [28] that when transmission lines are used rather than lumped components, for maintaining the same impedance, the bandwidth achieved is lower. This is because long lines are needed to achieve the inductance needed, resulting in an increase in the parasitic capacitive effects. Hence, to be able to have a bandwidth comparable to that of a corresponding DA, high-impedance lines must be used. Such transmission lines are difficult to implement in non-III-V processes. Lastly, DAs are relatively easier to implement because lumped components of various values are readily available and suitable for the design process.

3.2.3. Transmission Line Components

To realize the inductive element in a transmission line, three types of components are predominantly used in modern ICs: inductors, microstrip lines, and coplanar waveguides. In this section, we give a brief description of the components available, and we focus on spiral inductors.

3.2.3.1. Inductors

Inductors required in applications operating beyond the L-band (1 – 2 GHz) have a typical value range of 0.5 – 10 nH [29]. The low-value inductors can be realized as a transmission line inductor, which is quite simply a single metal strip. The larger

inductance values are attained by the use of spiral inductors, which achieve high inductance/area through the coupling between turns. A multilayer process has to be used to be able to realize spiral inductors in order to provide an underpass to connect to the inductor's inner end. While such inductors may have any one of several geometries, the most conventional layouts are circular, octagonal or rectangular. Rectangular and octagonal spiral inductors are preferred over circular ones as they have fewer points and hence masks needed for fabrication are simpler. Circular shapes have the advantage of reduced stress in the structure due to the use of smooth turns. An octagonal spiral inductor with its equivalent circuit is shown in Figure 3.10. Important design layout parameters include inductor inner diameter, number of turns, turn width, and turn spacing. The resonance frequency, determined by the layout parameters and materials used, sets the maximum usable frequency for the inductor.

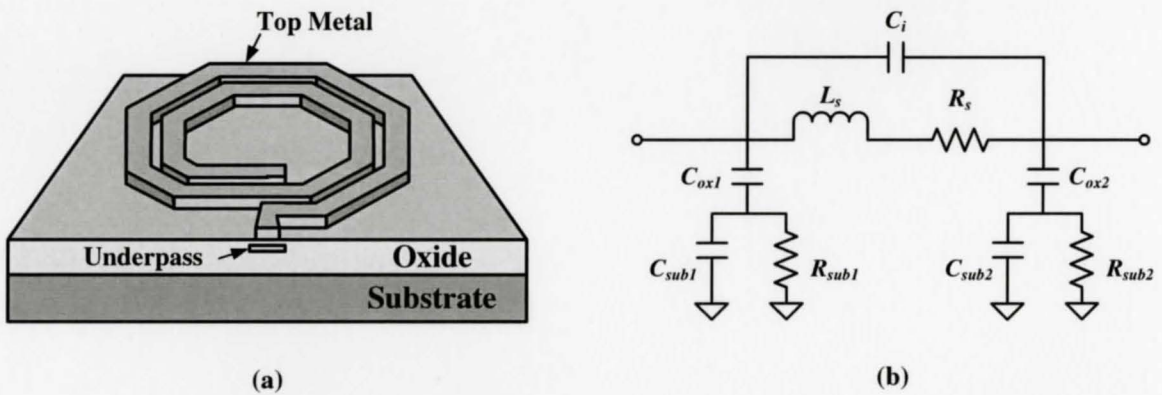


Figure 3.10: (a) Octagonal spiral inductor with 2 turns and (b) its equivalent circuit

The inductance of the inductor is due to L_s shown in Figure 3.10(b) and the rest of the elements shown are parasitic effects. R_s models the resistivity of the metallization used and takes into consideration skin effect and current crowding. C_i is due to the coupling effects between turns and between the coil and the underpass. C_{ox1} and C_{ox2}

correspond to the oxide capacitance. C_{sub1} , C_{sub2} represent the capacitance to the ground and R_{sub1} , R_{sub2} signify losses due to the low-resistivity substrate at the input and output ports, respectively.

Substrate losses are the most significant difficulty in designing and using on-chip inductors in silicon-based technologies. When the substrate has a low resistivity, the magnetic field from the inductor penetrates the substrate inducing eddy currents, which are oriented in a way such that they in turn produce a field that opposes the original field and hence the equivalent inductance and the quality factor are reduced [30]. The substrate is not the only problem as integrated inductors suffer also from the underpass parasitics and the fairly resistive aluminum metallization used in standard processes.

Current research into achieving higher Q inductors in silicon substrate is actively pursued by many groups. Many techniques have been proposed, and a few of them mentioned here. Firstly, it has been found that circular and octagonal inductors have series resistance up to 10% less than rectangular realizations of the same inductance value [31]. It has also been proposed [32] – [34] that processes migrate from Al/SiO₂ technology to thick Cu because Cu has a higher conductivity than Al, thereby reducing resistive effects. However Cu metallization is not part of the standard BEOL process. Also, the dielectric between the inductor and the lossy substrate is still relatively thin. Micromachining techniques can be used to remove the lossy substrate underneath the spiral inductor as a post-processing step. Lastly, patterned ground shields may be used to reduce the parasitic capacitance and increase resistance to the image current by providing a termination to the electric field before it reaches the substrate [35]. The ground plane can be made out of heavily doped polysilicon as in the IBM SiGe BiCMOS process

utilizing a deep trench mesh [36]. All these methods, when implemented correctly, can improve Q by up to 50% [37].

3.2.3.2. Microstrip Lines

Microstrip lines have been extensively used in MMICs due to ease of fabrication and integration. Figure 3.11(a) shows the basic structure of a microstrip line. A microstrip line consists of a thin metal strip running over a ground plane separated by a dielectric layer and hence must be realized in a multilayer process. Most of the electric field lines are contained between the conductor and the ground plane with little field line density in the air above it. Straight sections of microstrip lines can be used for low inductance values typically up to 2 – 3 nH [29]. When the length of a microstrip is less than the operating wavelength, it may be treated as a lumped inductor. Parasitic losses are primarily due to conductor losses arising from the limited conductivity and the skin effect of the metal line.

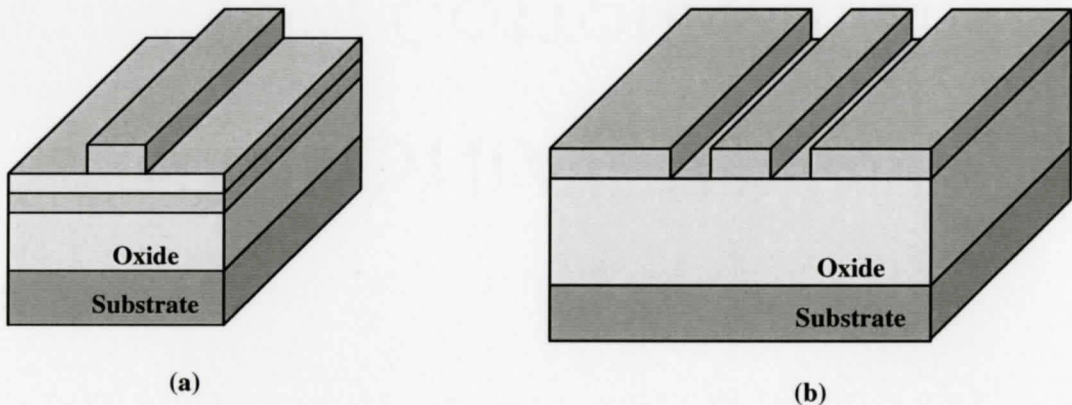


Figure 3.11: Geometry of (a) microstrip line and (b) coplanar waveguide

3.2.3.3. Coplanar Waveguides (CPWs)

Coplanar lines are a family of transmission lines that includes coplanar strips, slotlines, and CPWs. The term ‘coplanar’ refers to the case when lines are all on the same plane on the surface above the dielectric layer and hence multilayer processes are not needed to realize these types of transmission media. Figure 3.11(b) illustrates the CPW geometry with a signal line sandwiched between two ground planes, which ideally should be infinite in width. Characteristics of the waveguide, such as the characteristic impedance, are determined by the central conductor width and slot size. Even though CPWs can achieve similar performance to microstrip lines, they confine the electric field less, thus making them more sensitive to substrate losses. CPWs are widely used in MMICs because active components such as MESFETs are coplanar in nature. They are particularly useful in fabricating active circuitry with the signal on the center conductor and proximity to ground planes easily accommodating series and shunt connected components and T and π networks.

3.3. Previous Work

Since the advent of distributed amplification a few decades ago, much research has been performed on the topic. As mentioned previously, the inspiration started with thermionic tubes and gained popularity with III-V compound semiconductors, previously the main MMIC technology. As CMOS and SiGe BiCMOS processes began operating at very high frequencies and became contenders in the field of MMICs, great effort was spent trying to implement DAs in these less expensive technologies. Even recently a DA has been implemented using GaAs PHEMTs on liquid crystal polymer for UWB RFID

applications [38]. Figure 3.12 shows the GBW product of samples of III-V, CMOS and SiGe DA implementations in the literature extracted from [39] – [55]. It is evident that recently much research has been done in CMOS and SiGe distributed amplifiers and that SiGe implementations are closing the gap between CMOS and III-V semiconductors. Obviously, if a DA accomplishes the required performance using CMOS, that implementation would be preferred over a SiGe implementation because of its lower cost. Table 3.1 summarizes some important performance characteristics of published SiGe HBT distributed amplifiers.

Characteristics indicative of amplifier performance are accounted for in the table and are explained as follows. f_T indicates the cut-off frequency of the HBTs in the technology used, but in the actual design, the transistors need not necessarily be biased for maximum frequency operation. BW indicates the 3-dB bandwidth, which is either specified in the original author's publication or extracted from results provided in the paper. S_{21} , S_{11} , and S_{22} signify the magnitude of the average DA gain, maximum input return loss, and maximum output return loss respectively, all within the bandwidth specified. The group delay, GD , and gain ripple, ΔS_{21} , symbolize distortion effects of the amplifier. The gain ripple is how much the gain fluctuates within the passband and should be minimized. NF is the noise figure of the amplifier; it varies with frequency and should be kept minimal. DAs are in general rather noisy architectures. Along with GD , not many papers publish the noise figure. The 'stages' column indicates how many were used and what type gain cell was implemented. The type of inductors used is specified by the TL type and was found either to be CPW or lumped inductors. P_{dc} indicates the DC power consumed from the supply voltage that is specified in the next column.

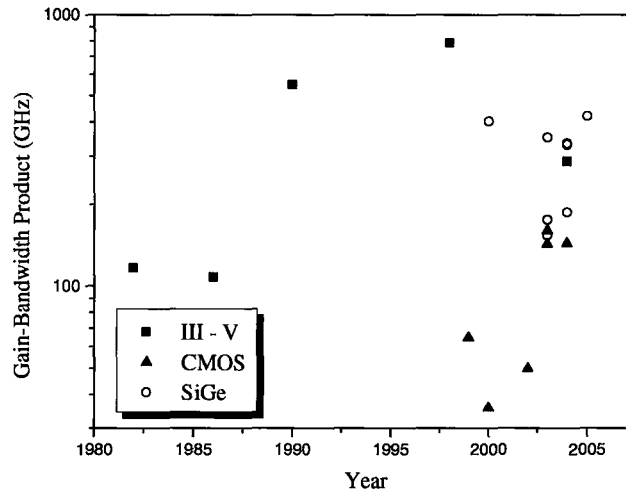


Figure 3.12: Gain-Bandwidth product of samples of DA implementations in III-V semiconductors, CMOS, and SiGe in the literature

Table 3.1: SiGe HBT DA implementations in the literature

Ref.	f_T (GHz)	BW (GHz)	$ S_{21} ^a$ (dB)	ΔS_{21} (dB)	$ S_{11} ^b$ (dB)	$ S_{22} ^b$ (dB)	GD (ps)	NF (dB)	Die Size (mm ²)	Stages ^c	TL method	P _{dc} (mW)	Supply (V)
[50]	100	dc - 67	6	0.5	-15	-25	—	—	1 × 1	3 cc	CPW	75.9	3.3
[51]	120	0.1 - 50	7	2	-10	-15	20 - 30	—	1 × 1.1	3 cc	inductors	125	5.0
[52]	100	0.1 - 23	14.5	1	-9	-10	—	5	0.7 × 2.1	5 cc	CPW	54	3.6
[53]	120	0.5 - 22	15	1	-10	-7	20 - 35	5.5	0.67 × 2.1	5 cc	CPW	72	3.6
[54]	120	dc - 25	7.5	0.5	-7	-7	—	—	0.9 × 1	4 dcc	microstrip	99	3.3
[55]	79	dc - 28	15	2	-5	-7	—	—	0.63	2 css	inductors	48	2.5

a: average gain within the passband, b: maximum loss within the passband

c: cc = cascode, dcc = differential cascode, css = cascaded single-stage distributed amplifier

The following is a summary of the implementations referred to in Table 3.1.

Kerzar *et al.* [50] published one of this first SiGe HBT DAs with a very impressive bandwidth and moderate gain. Actually two designs were implemented, one with 67 GHz bandwidth and 6 dB gain and the other with a bandwidth of 80 GHz and gain of 4 dB. They used the Hitachi SiGe HBT 0.2 μm technology with a f_T of 100 GHz. The high bandwidth was accomplished due to the use of a non-commercial silicon-on-insulator substrate. Consequently, the CPW and microstrip taper structures used were of

high quality factor. The design was optimized for constant group delay, but no figures or data for either was supplied.

One of the first commercial implementations produced was by Aguirre *et al.* [51] using the IBM 7HP BiCMOS 0.18 μm process with $f_T = 120$ GHz. The design was implemented using two forms of transmission line inductors. The first used a microstrip-like structure incorporating the top metal for the signal and the bottom-most metal for a width-limited ground plane, and achieved a gain varying between 9 – 5 dB over 50 GHz. The second used inductor strips over a deep-trench ground mesh to improve the quality factor and had a gain between 8.5 – 6 dB over the same band. ATLs were used with the input line realized using constant- k sections and the output line using m -derived sections. No matching sections were used on either line. Off-chip terminations were used and the electrical length added in the process were not taken into consideration leading to multiple reflections throughout the passband that were evident from the measured s -parameters. The gain varies significantly in the passband with a ripple of ± 2 dB due to the low-quality input line used. The group delay was given as approximately constant at 20 ps rising sharply at cut-off. High power consumption was measured as a result of the high supply voltage used.

Another commercial SiGe BiCMOS process with $f_T = 100$ GHz was used by He *et al.* [52] to realize 2 broadband LNAs, one distributed and the other lumped. Degenerative resistors were added to the emitters of the cascode cell to improve linearity and broaden the bandwidth. Five stages were used, leading to higher than average gain that was relatively flat throughout the band. The metallization material used was not disclosed. CPW transmission lines were used for their high Q and available accurate simulation

models. One disadvantage of their design was the relatively large die size due to the low inductance/area of the lines. For sake of comparison, a lumped LNA was implemented using the same source voltage and was found to provide slightly higher gain over approximately the same bandwidth at 1/5 the circuit size, but with higher power dissipation.

Chan *et al.* [53] have presented a DA utilizing the IBM 7HP process for a receiver in a System-on-a-Chip application. In their design, degenerative resistors were used to reduce low frequency gain and shunt capacitors to nullify their effect at higher frequencies, consequently achieving flat gain throughout the passband. High gain was achieved due to the use of 5 stages. High Q inductive CPW transmission lines were used but due to their low inductive density, long lines varying from 100 – 300 μm per section were requested. Resistive matching was used, which is prone to one disadvantage: process variation is rather high in resistors, especially at high frequencies. This is evident from the discrepancies between the S_{11} and S_{22} simulations and measurements.

Guckengerger *et al.* [54] used an emitter follower stage to drive an emitter-degenerated cascoded differential pair in a 120 GHz process. The emitter followers were used to provide an impedance transformation of the capacitance at the emitters to a negative resistance at the base, hence reducing attenuation on the lines and consequently allowing for more stages and longer lines. Since differential transmission lines were used, special precautions were taken to reduce capacitive coupling by providing ground shields between the input and output lines. S_{11} and S_{22} are worse than the average acceptable values of -10 dB.

Tsai *et al.* [55] have been able to produce a DA with high gain, 15 dB, over a band of 28 GHz in a compact design using a commercial 0.35 μm process with $f_T = 79$ GHz. The reason such a high GBW product was achieved in a technology with an f_T relatively lower than the previous designs was due to the use of a modified loss compensation technique proposed by the authors. The method proposed resulted in a GBW product improvement of 68%, compared with conventional attenuation-compensation techniques. The power dissipated was relatively low due to the reduced supply voltage used. The input and output reflections were worse than the normally accepted values.

There were two other implementations using SiGe, but not HBTs [56], [57]. The first uses only the CMOS transistors of a BiCMOS 0.18 μm process with 6 layers of Cu metallization. Gain stages used common-source transistors and inductors used were modeled to take into consideration the eddy current loss in the Si substrate. Simulation results showed a gain of 7 dB over a bandwidth of 22 GHz and NF varying from 6.5 – 10 dB. Power consumption was 132 mW. The second design used MODFETs with $f_T = 52$ GHz on a high-resistivity substrate. Ti/Au metallization was used for low loss CPW interconnections. Six gain stages were used with common-source transistors with source degeneration and were externally terminated with 50 Ω resistors. A low gain of 5.5 dB, mostly due to the effect of the degeneration, was achieved over a bandwidth of 32 GHz and the power consumption was 105 mW.

From the results discussed above, a few conclusions may be drawn regarding the applicability of SiGe HBT DAs. Even though these designs have shown to be successful, they have also proven to be more difficult to design than their CMOS counterparts. This

is true for mainly two reasons. Firstly, HBTs, and bipolar transistors in general, have lower linearity than CMOS circuits. In most of the above designs, emitter degeneration was used to improve the linearity of the amplifier. This results in lower voltage headroom and consequently higher power consumption. Secondly, even though the transmission lines absorb the parasitic capacitances of the HBTs, the input series base resistances are not compensated for. The intrinsic base resistance, R_{bi} , is typically in the range of 30 Ω , which is significantly higher than the gate resistance in FETs. These resistances contribute greatly to the attenuation of the ATLs, which limits the GBW product. This resistance may be neutralized through loss compensation networks to achieve modest GBW product improvement, as discussed in [58].

There are a few other issues worth mentioning. The gain in many of the designs shows a “dual plateau” pattern peaking at the two extremes of the passband. This ripple should be reduced as much as possible to maintain signal integrity. Moreover, not much information was presented in the literature with respect to the NF and GD in SiGe HBT DAs. Lastly, the power consumption currently in these implementations significantly exceed or are similar to those of CMOS circuits, which dissipate power normally in the 50 – 75 mW range [59]. Regardless, the power is rather high and efforts should be made to reduce it.

The next chapter will consider an implementation of a SiGe HBT DA taking many of these design advantages and limitations into consideration.

Chapter 4

IMPLEMENTATION OF SILICON GERMANIUM HBT DISTRIBUTED AMPLIFIER

In this chapter, the design of a SiGe HBT DA will be studied and simulations and measurements will be reported. Some layout issues will be analyzed along with a general discussion of the results obtained.

4.1. Circuit Design

The 0.5 μm IBM SiGe5AM process was chosen to implement this design. This is the first generation SiGe process. Compared with its more advanced successors, this technology has a relatively low f_T of approximately 50 GHz. We used this technology

platform because it is the SiGe platform available through the Canadian Microelectronics Corporation (CMC). Nonetheless, using this process allows direct comparison with implementations in CMOS 0.18 μm processes since those have a similar f_T .

As discussed in Chapters 1 and 3, the first dimension of designing a UWB amplifier is the gain cell. Most distributed amplifier (DA) implementations have been made using either a single transistor or a cascode configuration for the gain cell. For the circuit implemented here, the common-emitter, common-base cascode configuration was chosen. This provides lower input capacitance due to the reduction of the Miller effect, and better input-output line isolation. The reduction of the input capacitance allows for higher bandwidths to be achieved, compared with the case of a single transistor gain cell.

Next to the gain cell, the selection and design of transmission lines used is the most important factor impacting performance of a DA. As discussed in Chapter 3, the transmission lines may be realized as either periodically loaded TLs or artificial TLs. Both alternatives were explored. The SiGe5AM process has a component similar to a microstrip line. The structure of the component, called Singlewire, consists of a signal bearing metal strip using the AM top metallization (see Figure 2.9) of width W over a finite width metal ground plane made of M1, M2 or MT metallization layer a distance d under the signal strip. Figure 4.1 shows the variation of the per unit length series inductance, resistance, shunt capacitance and characteristic impedance of the line with W and d as simulated using the Agilent ADS EM simulator, Momentum [60].

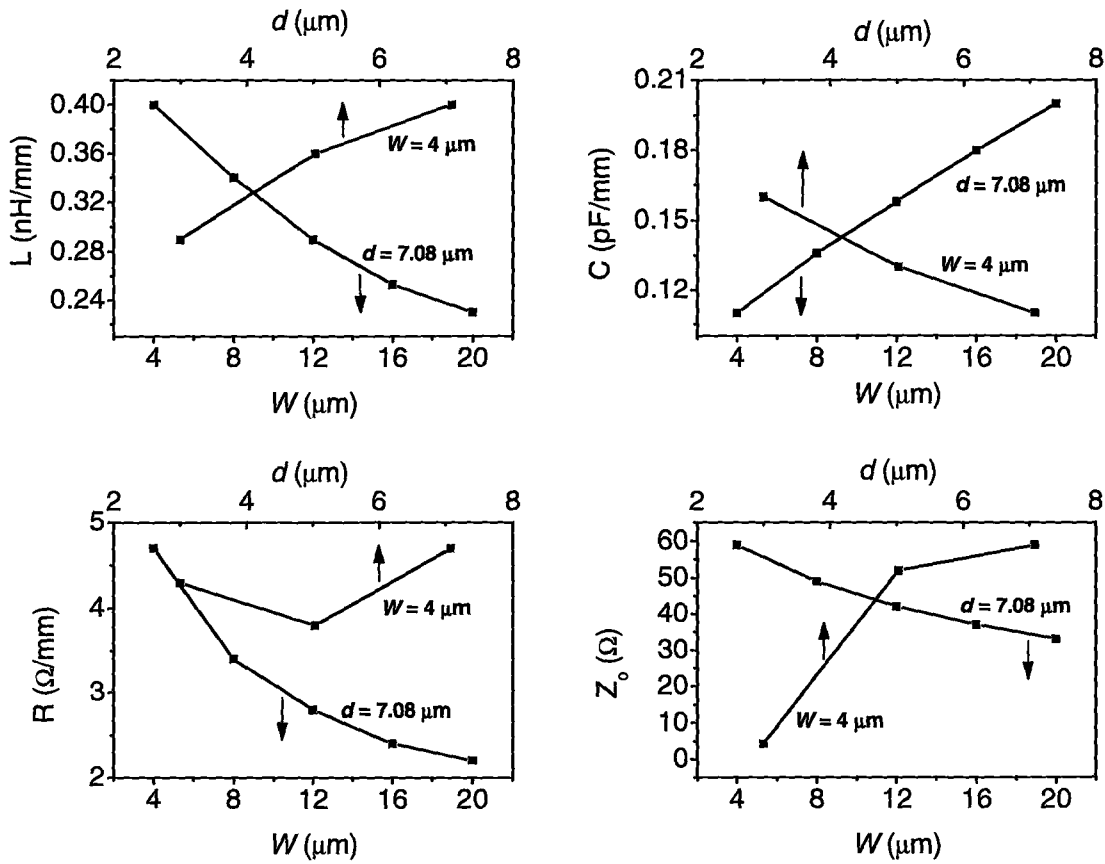


Figure 4.1: Variation of microstrip parameters with strip width, W , and distance between strip and ground, d , which is determined by which metal layer M1, M2 or MT is used for ground

With reference to the figure, it may be seen that as W decreases, the line inductance increases, capacitance decreases and the resulting characteristic impedance increases – all desirable effects. As mentioned in the previous chapter, the higher the Z_0 the closer the TL is to an inductor and hence the better the DA performance. The single-wire component allows a second degree of freedom in the design by allowing some control over the distance d . This design parameter may be increased or decreased, respectively, by choosing a ground plane closer to, or farther from, the substrate (the choices being, in descending order according to distance from the substrate, layers MT, M2, and M1). Referring once more to Figure 4.1, it may be observed that L increases and C decreases

as d increases, with a fixed W of 4 μm . As a result, Z_o increases and is a maximum when the M1 layer is used.

Given these considerations, a highly inductive microstrip line would be realized by decreasing W and increasing d . Given the constraints of the fabrication process, the highest characteristic impedance that may be thus achieved is approximately 60 Ω . This is not sufficient to compensate for the capacitive loading as outlined by equations (3.16) and (3.17). This leads to the choice of lumped inductors and ATLs over periodically loaded TLs.

Figure 4.2 illustrates a complete schematic of the proposed distributed amplifier. Lumped inductors were implemented as spiral inductors for inductances of 1 nH or larger, and as inductive lines for smaller inductances. Both types make use of the top metal and have an underlying deep trench ground mesh to reduce parasitic capacitance. In the schematic, a large spiral indicates spiral inductors, whereas the conventional symbol for an inductor was reserved for the smaller inductive lines. For the base line, these inductances are configured in a constant- k section while the collector line uses m -derived sections with $m = 0.1$. No additional capacitance was needed at the output of the cascode as $C_{cb} = 25.7 \text{ fF} \approx mC_{be} = 0.1 \times 223 \text{ fF}$. Theoretically, if m -derived sections are used on both lines, better characteristics should result. The decision not to implement m -derived sections on the input line was driven by a trade-off of the potential performance improvement against the area requirement of an additional large shunt inductance. Matching filters are used on the output line only since circuit simulations indicated that their addition on the input line results in marginal improvement to input matching. The

capacitors used here, C_1 , are metal-insulator-metal (MIM) capacitors. The base inter-stage inductances have the value:

$$L_5 = R_b^2 \cdot C_{be} = (50)^2 \cdot 223 \text{ fF} \approx 0.55 \text{ nH}$$

The values of the rest of the components needed for both lines were calculated from Figure 3.5 and Figure 3.6.

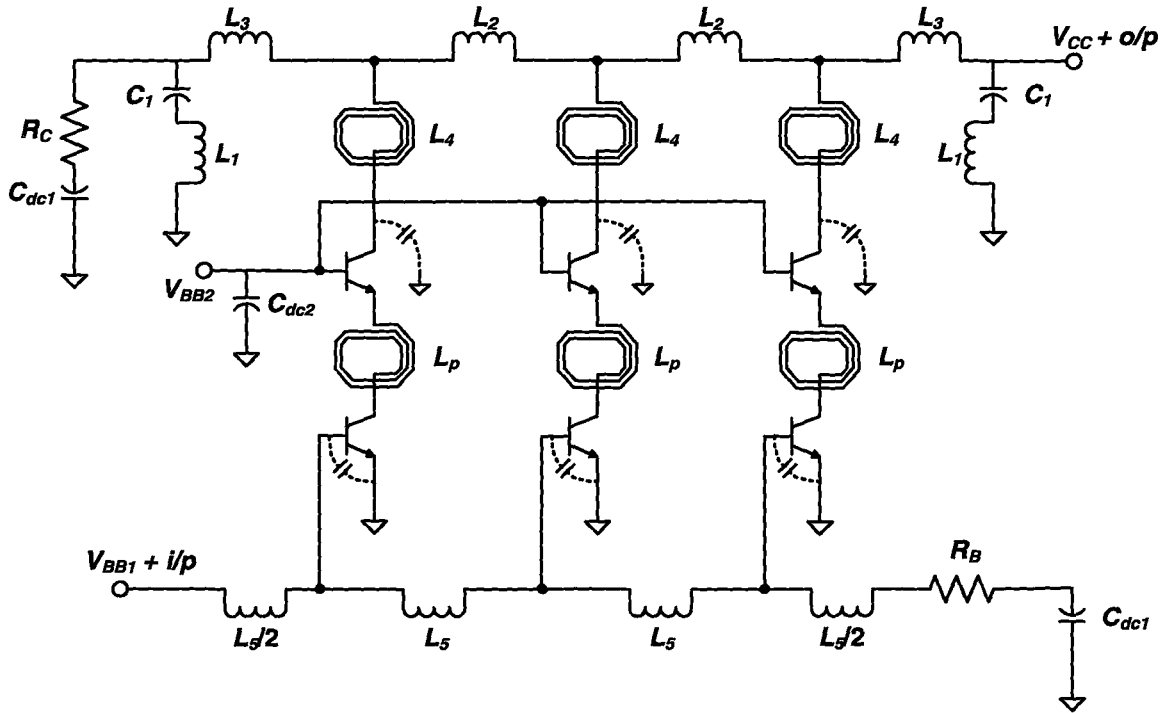


Figure 4.2: The proposed distributed amplifier

Decoupling capacitors, C_{dc1} , are used to block DC current from flowing through the terminations. This reduces the circuit's power consumption. Another decoupling capacitor, C_{dc2} , is used to ensure a proper AC ground. All decoupling capacitors are chosen to be as large as possible with the chip area available. The termination resistances R_b and R_c , are designed to be 50Ω as such was the image impedance of the ATLs. A peaking inductor, L_p , is inserted between the transistors of the cascode cell to provide

higher gain at intermediate and high frequencies by providing matching between the capacitive output and input impedances of the CE and CB transistors. The values of the circuit parameter and components are listed in Table 4.1.

Table 4.1: Values of circuit parameters and components

Component/Parameter	Value
V_{BB1}	0.88 V
V_{BB2}	1.1 V
V_{CC}	2 V
<i>HBTs' emitter area</i>	2 fingers $\times$ 0.5 μm $\times$ 5 μm
C_{be}	223 fF
C_{cb}	25.7 fF
L_1	0.293 nH
L_2	72.6 pH
L_3	0.193 nH
L_4	1.4 nH
L_5	0.55 nH
L_p	0.96 nH
C_1	123 fF
C_{dc1}	21.6 pF
C_{dc2}	15.4 pF
R_b	50 Ω
R_c	50 Ω

4.2. Simulation and Measurement Results

4.2.1. S-Parameters

Scattering (s) parameters were simulated using the Cadence circuit simulator and the results are shown in Figure 4.3. The dashed line shows how the peaking inductor, L_p ,

levels the gain at approximately 10 dB throughout the -3 dB passband of 18.5 GHz. These simulations were done without taking into account the effect of losses in the interconnections. Interconnection losses were simulated using Momentum and the results incorporated in the circuit simulation. In the remainder of this thesis, measurements will be compared with the full simulations that take into account interconnection losses. Due to the complexity of interconnection simulations, this had not been accomplished prior to the fabrication of the circuit, so the extent of performance degradation had not been fully anticipated. This will be taken into account in future designs.

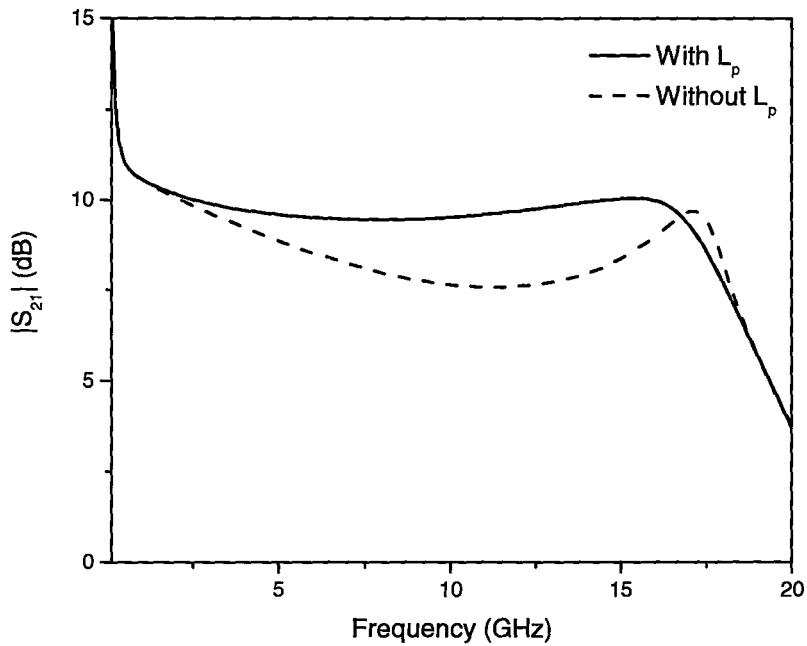


Figure 4.3: Circuit simulations without interconnection losses of the proposed DA showing the effect of the peaking inductor, L_p

S-parameter measurements were done using the experimental setup outlined in Appendix B. A comparison of the simulated, with interconnection losses, and measured gain magnitude, $|S_{21}|$, is depicted in Figure 4.4. The gain is found to be approximately 6.5 dB throughout a -3 dB band from 0.5 – 10.5 GHz. The unity gain cut-off frequency is at

12 GHz. The gain within the specified passband is nearly flat with a ripple of ± 0.5 dB. The sharp rise at low frequencies is due to the effect of the blocking capacitors, C_{dc1} , on the input and output lines. Removing these capacitors, at the expense of higher power consumption, or increasing the size of the capacitors trading off with area, may achieve a flat gain down to DC. The gain also slightly peaks prior to cut-off due to the effect of the m -derived sections on the output line. De-embedding of the circuit showed very small effect on the measured s -parameters due to the use of one metallization layer pads far from the substrate, hence reducing parasitic capacitances.

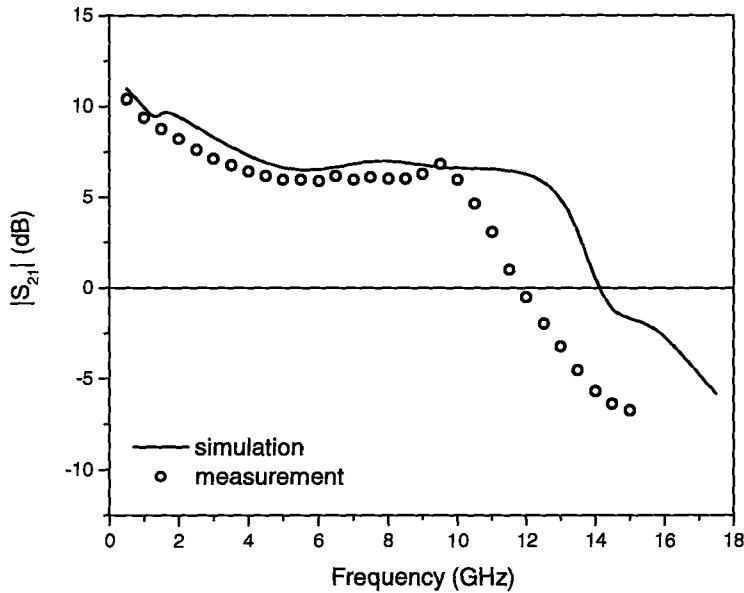


Figure 4.4: Simulated and measured gain of the proposed amplifier

The measured input and output return losses, $|S_{11}|$ and $|S_{22}|$ respectively, shown in Figure 4.5(a), (b), are also found to follow the same trend as their simulations throughout the passband. $|S_{22}|$ is under the acceptable limit of -10 dB over the bandwidth and $|S_{11}|$ goes up to -5 dB at cut-off. The input is not matched as well as the output line because bisected π -sections were not used, as in the output line, and because of the inherent mismatch in the base line due to higher losses added by the transistors' base resistances.

Figure 4.5(c) shows the magnitude of the reverse gain, $|S_{12}|$, with its maximum level at approximately -20 dB, indicating good isolation between the input and output lines. The simulated and measured results are far from each other at low frequencies with improved accuracy at higher frequencies close to cut-off.

All s -parameter simulations show discrepancy from their respective measurements. This is because the circuit simulations took into account separate interconnection s -parameters simulations and not all the circuit interconnections were simulated in one run, which would produce a more accurate result. This was done to be able to determine the effect of each interconnection on overall circuit performance.

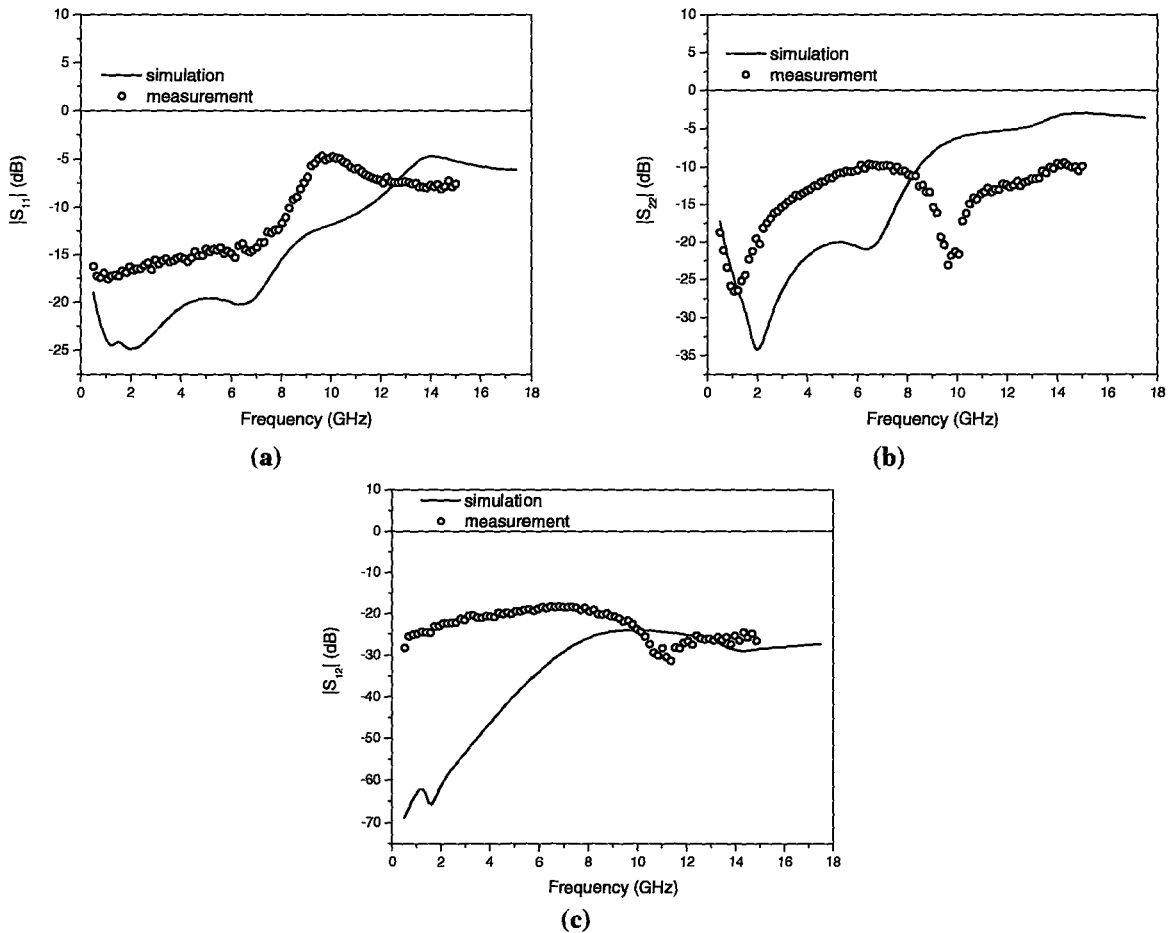


Figure 4.5: (a) $|S_{11}|$, (b) $|S_{22}|$, and (c) $|S_{12}|$ simulations and measurements

The distortion effects of the DA can be quantified through the phase of the gain, $\angle S_{21}$, shown in Figure 4.6(a). The corresponding group delay, GD , is shown in Figure 4.6(b) calculated from $\angle S_{21}$ using equation (3.4). It can be seen that the phase is approximately linear up to 10 GHz and the corresponding group delay is almost constant at 60 ps. The group delay then increases significantly before and at the cut-off frequency because of the peaking allowed in the gain to compensate for losses at higher frequencies.

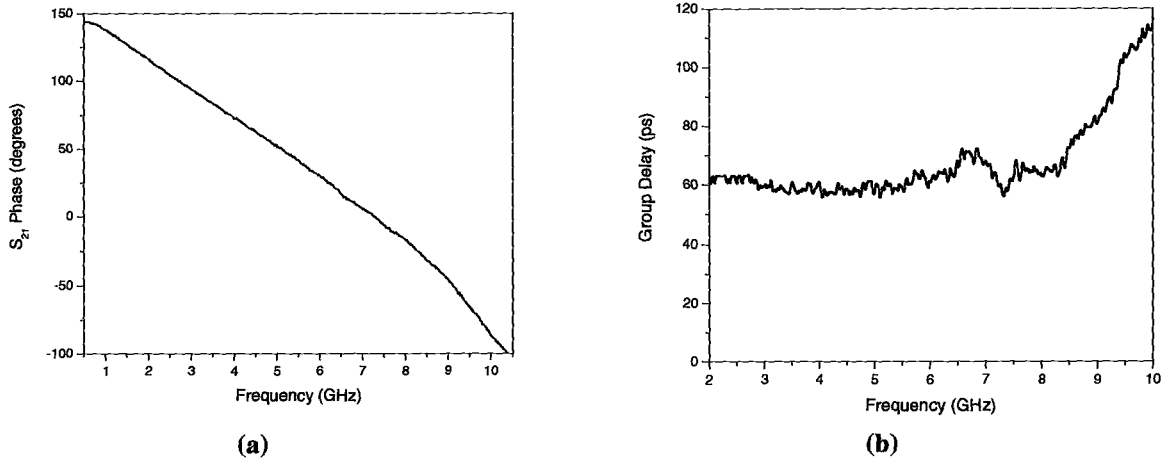


Figure 4.6: (a) measured gain phase and (b) corresponding group delay

4.2.2. Noise Figure

The noise figure of the distributed amplifier was measured using the experimental setup described in Appendix B and the measurement results are shown in Figure 4.7. The noise figure varies from 5.8 dB at low frequencies to 9 dB at the -3 dB cut-off frequency increasing more so afterwards.

When compared to the results predicted by Cadence models the error is over 50%. An analysis of the noise sources within the DA and a more accurate calculation of the NF are given in Chapter 5.

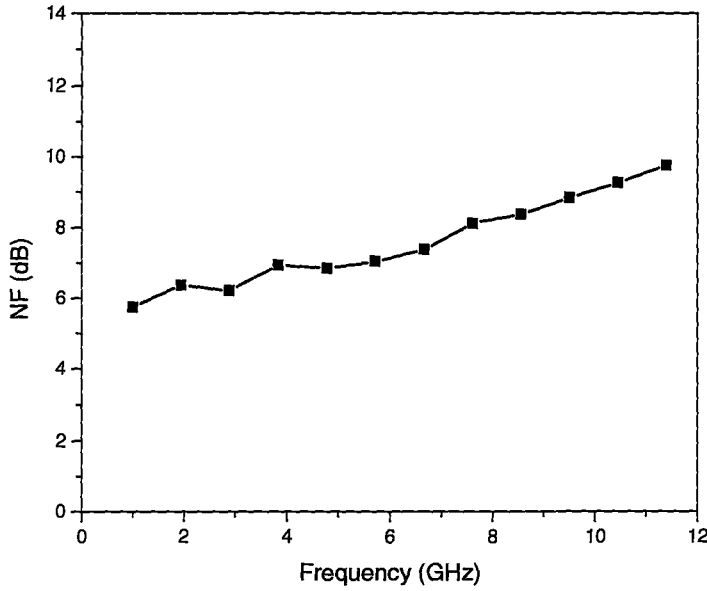


Figure 4.7: Measured NF of the proposed DA

4.2.3. Temperature Effects

All the previous measurements were done at a room temperature of 22 °C. Two publications [49], [61] have reported the effects of temperature on the performance of distributed amplifiers, both in CMOS. Measurements therein [61] showed that gain decreases at a rate of 0.2 dB for every 5 °C increase in temperature. The rest of the s -parameters were found to vary much less with temperature variation.

The proposed amplifier was operated up to 45 °C at 5 °C increments and the s -parameter measurement results are shown in Figure 4.8 – Figure 4.12. The gain magnitude, Figure 4.8, is seen to fall drastically at a rate of approximately 2.5 – 3 dB in the middle of the band for every 5 °C increase in temperature. The gain curves also become less flat as the temperature increases. The same severe temperature impact is witnessed in $|S_{11}|$ as shown in Figure 4.9. $|S_{11}|$ gets worse than –10 dB at lower frequencies due to the temperature effect, but the degradation decreases as the

temperature increases and at cut-off, $|S_{11}|$ actually improves with the temperature increase. $|S_{22}|$ and $|S_{12}|$, shown in Figure 4.10 and Figure 4.11, change at much lower rates, about 0.5 dB/5 °C and actually improve within the passband with temperature increase.

Figure 4.12 depicts the phase of S_{21} and how it changes with temperature. It can be seen that the phase is still linear within the passband. The corresponding group delays are not shown. By definition, they will be approximately constant throughout the passband because the phase is still linear. Since the slope is slightly increasing with temperature, this means that the group delay will slightly increase with temperature. It is also observed that the phase linearity improves with temperature and hence the variation and peaking witnessed at cut-off in Figure 4.6(a) is reduced.

Simulations were run and showed similar temperature effects. Figure 4.13 compares the simulated and measured drop in $|S_{21}|$ with temperature at 9 GHz where the gain was observed to drop the most and they seem to agree quite well.

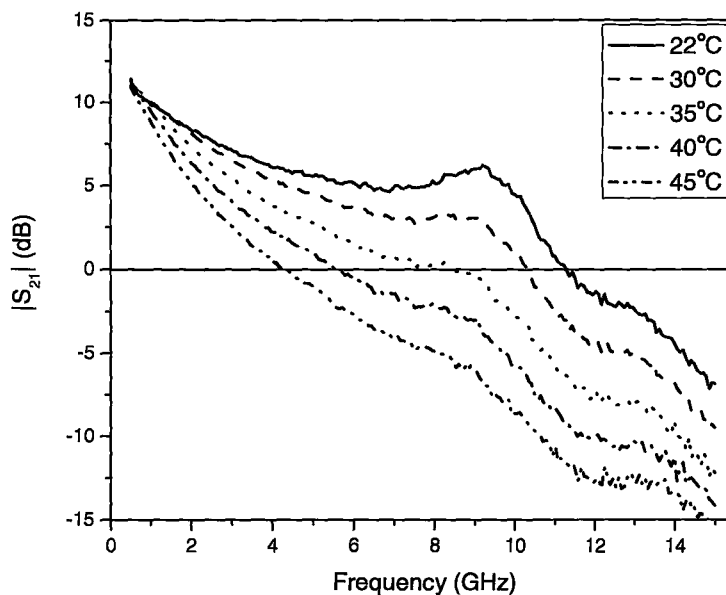


Figure 4.8: $|S_{21}|$ variation with temperature over the range of 22 – 45 °C

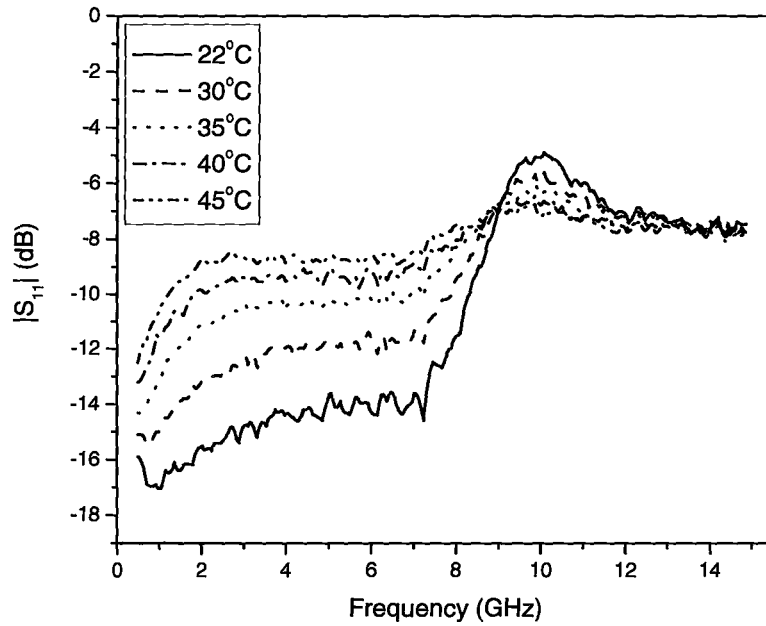


Figure 4.9: $|S_{11}|$ variation with temperature over the range of 22 – 45 °C

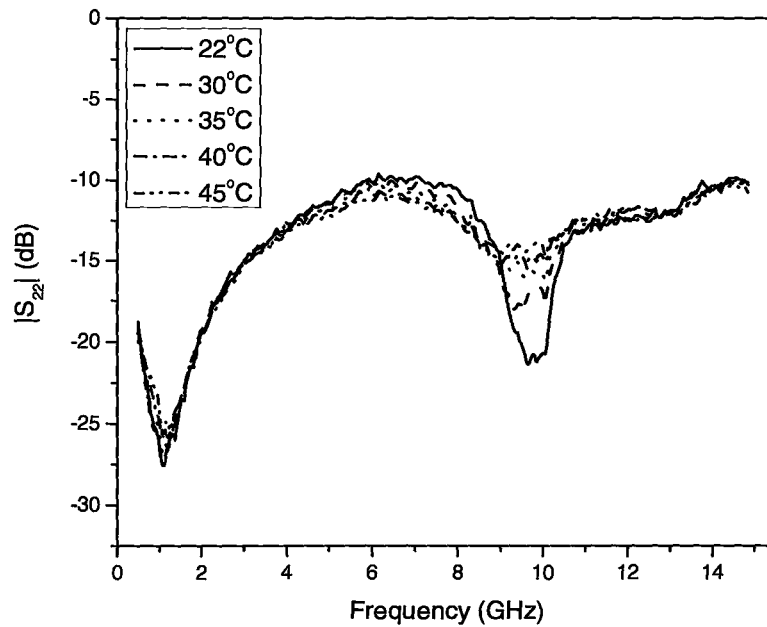


Figure 4.10: $|S_{22}|$ variation with temperature over the range of 22 – 45 °C

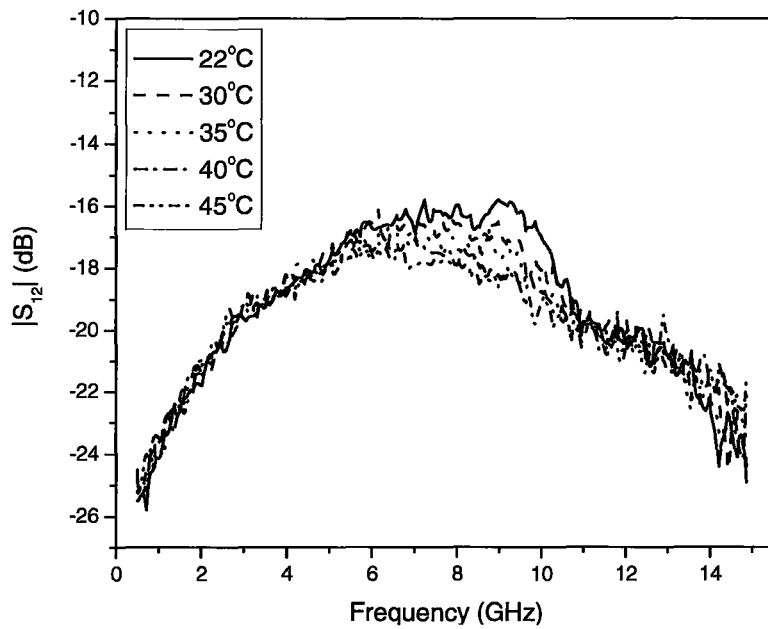


Figure 4.11: $|S_{12}|$ variation with temperature over the range of 22 – 45 °C

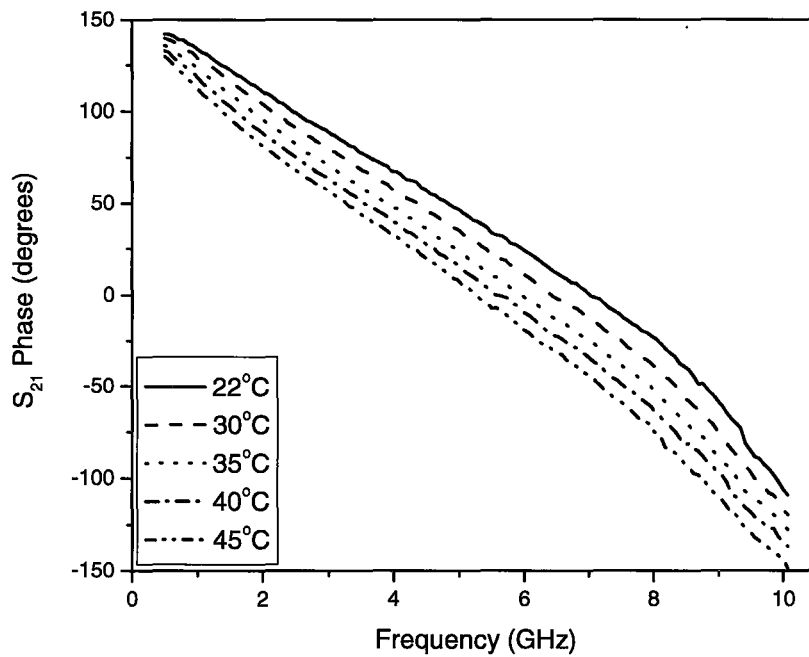


Figure 4.12: S_{21} phase variation with temperature over the range of 22 – 45 °C

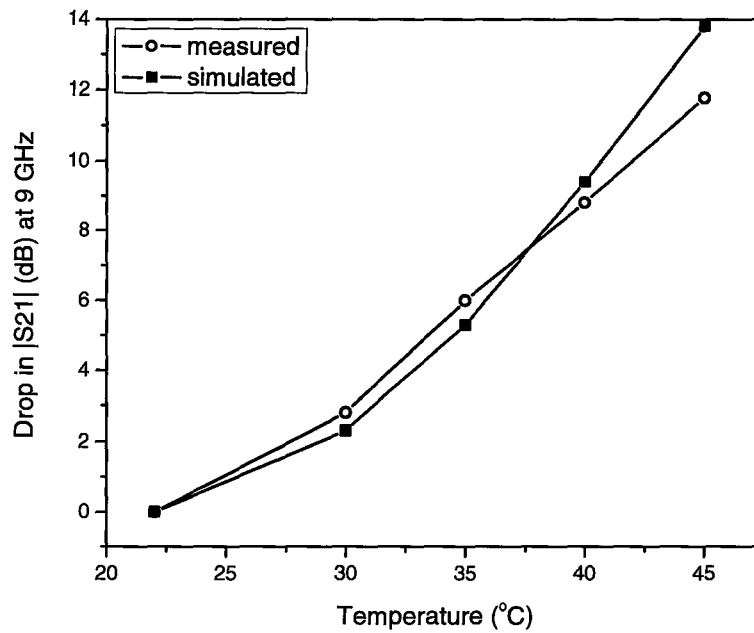


Figure 4.13: Comparison between simulated and measured gain drop with temperature

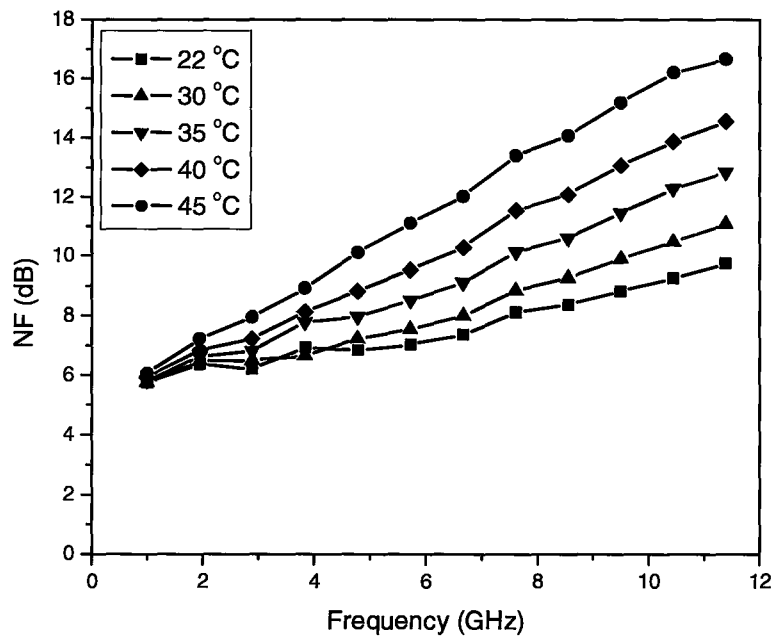


Figure 4.14: Variation of NF with temperature effect

The variation of the noise figure with temperature is illustrated in Figure 4.14. The NF is seen to increase with increased temperature. This may be attributed to the reduced gain at higher temperatures.

4.3. Layout Issues

As with any high frequency microwave integrated circuit design, proper layout of the desired circuit is of utmost importance. Figure 4.15 shows the micrograph of the DA designed taking a die area of 1.55 mm². The input and output 3-probe pads and the spiral inductors used are clearly visible, placed as far away as possible from each other to avoid coupling effects. Interconnections should be sparingly used and made as narrow or wide as possible to reduce capacitive or inductive/resistive effects, respectively, whichever is of most concern at a certain location in the circuit.

Because these effects were not fully taken into consideration, some unexpected problems arose during measurements. A certain set of bias conditions was selected when designing the circuit to achieve a gain of about 10 dB, as shown in Figure 4.3. But when these bias conditions were used in measurements, instability appeared in the s -parameters, which was not present in the simulations. The simulations were repeated taking into account the losses due to all interconnections, and these simulations predicted the instability effect as shown in Figure 4.16(a). Simulations were even able to determine the existence of a potential instability indicated by the stability factor, K_f , defined as:

$$K_f = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \quad (4.1)$$

If $K_f > 1$, then the circuit is unconditionally stable and potentially unstable otherwise. Figure 4.16(b) shows K_f dipping below 1 at around 14 GHz. Simulations show that the primary cause of this instability is the effect of the long ground line enclosed by the dotted line in Figure 4.15.

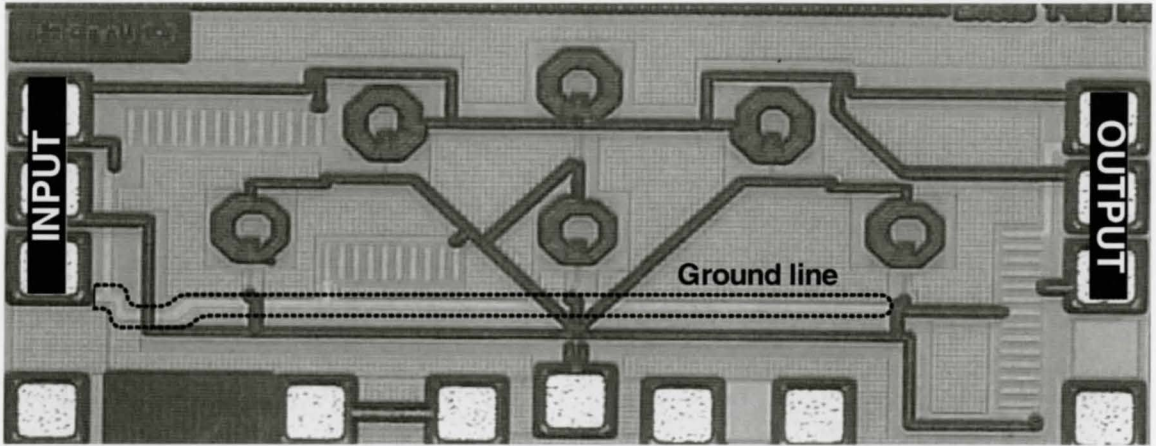
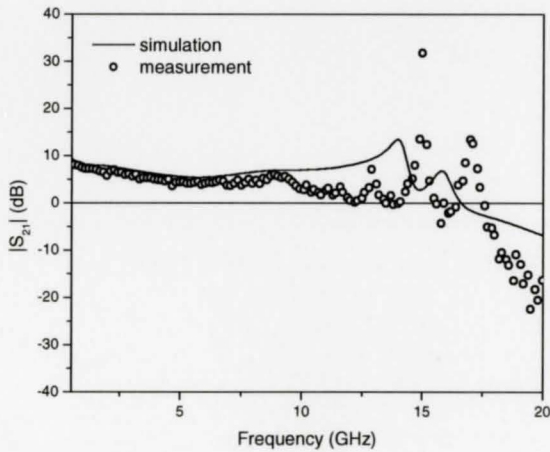
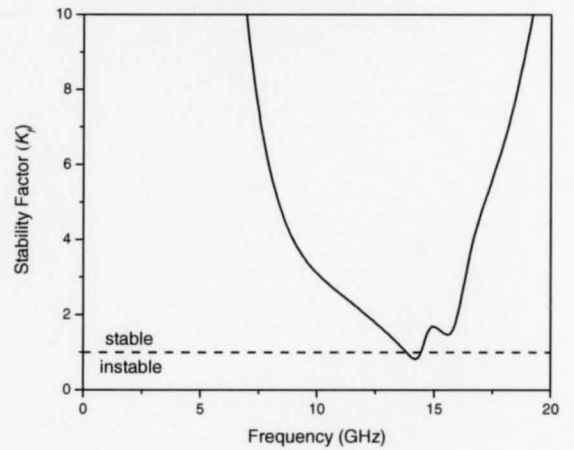


Figure 4.15: Micrograph of the proposed DA with the extended ground line enclosed with the dotted line



(a)



(b)

Figure 4.16: (a) instability in $|S_{21}|$ under original biasing condition and (b) K_f depicting it

4.4. Summary and Discussion

The performance of the designed distributed amplifier at room temperature is summarized in Table 4.2. The values are given for the range determined by the -3 dB bandwidth of $0.5 - 10.5$ GHz. Such a bandwidth is convenient for applications such as UWB receivers with an operating band extending from $3.1 - 10.6$ GHz. The gain of 6.5 ± 0.5 dB is typical for a 3-stage design. The design was limited to three stages because any additional stages were found to reduce the gain rather than increase it, for the reasons discussed in Chapter 3. A mid-band dip in the gain, as seen in [51], was almost eliminated through the use of the peaking inductor, L_p . The GBW product is less than previous designs listed in Table 3.1 due to the use of an older technology than those implementations.

Table 4.2: Proposed distributed amplifier performance

Performance Measured	Value
Forward gain (average), $ S_{21} $	6.5 dB
Bandwidth (-3 dB)	0.5 – 10.5 GHz
Bandwidth (unity gain)	12 GHz
Mid-band gain ripple, $\Delta S_{21} $	± 0.5 dB
Input return loss, $ S_{11} $ (max)	-5 dB
Output return loss, $ S_{22} $ (max)	-10 dB
Reverse gain, $ S_{12} $ (max)	-20 dB
Group delay, GD	60 ps
Power consumption	12.2 mW
Noise figure, NF	5.8 – 9 dB
Die area	1.55 mm ²

The output return loss is within acceptable limits whereas the input return loss is above the -10 dB limit. The line impedances changes dramatically as seen from equation (3.5) resulting in $|S_{11}|$ increasing quickly near the cut-off frequency as can be seen in Figure 4.5(a). This indicates that the use of a matching filter may help to resolve this problem. Furthermore, $|S_{11}|$ may be reduced further, and hence improve the GBW product, by implementing a loss compensation technique [58] to compensate for the base resistances introduced by the HBTs. The reverse gain, or isolation loss, is very low around -20 dB and is not of concern. The group delay is approximately constant at ~ 60 ps, and peaking is observed at cut-off as observed in previous work. The group delay measured here is higher than that reported in other works because longer lines were needed for the lower frequency operation due to the relatively low f_T transistors used.

Little information is available in the literature with regards to the NF in SiGe HBT DAs. The measured NF of $5.8 - 9$ dB is within the range of previous works. The NF reported in [52] and [53] is in the range of $5 - 6$ dB. The lower NF can be attributed to the higher gain and the greater number of stages used, which reduce the NF [62]. In general, the NF in DAs is greater than that of other architectures due to the large number of components used.

One of the major advantages in this design is the low power consumption of ~ 12 mW. This low power is attributed to many factors, including the use of blocking capacitors to eliminate DC current flow through the termination resistances. Also not using emitter degeneration reduces stacking and permits larger voltage headroom hence lower supply voltage was capable of being used. Obviously there is a trade-off with the linearity, but lower linearity is not a problem when designing receiver amplifiers,

especially in UWB applications. The low power consumption achieved allows the proposed DA to be used for portable wireless applications.

It is important that any electronic circuit successfully operate over an extended range of temperatures, up to 125 °C in military applications and up to 85 °C in most commercial applications. The effect of temperature was tested for the first time on a SiGe HBT DA and was found to detrimentally change the gain and input matching. Simulations yielded similar results even though the interconnections were simulated in Momentum at room temperature only. Moreover, it is commonly held that passive devices such as inductors and MIM capacitors have characteristics that change very slightly with temperature. This indicates that the main contributor to the variation is the HBT itself. The increase of ambient temperature has many effects on the different components comprised in the HBT equivalent circuit making the analysis of such an effect complex. The HBT capacitances slightly change with temperature but not enough to greatly impact its performance. The transconductance is known to increase with temperature, and f_T decrease due to the increased delays in the device [see equation (2.1)] [63]. According to simulations the base resistance slightly decreases and base current increases, as does the collector current. In fact, the overall current drawn from the supply increases with temperature, thereby increasing power consumption. The increased base current leads to a lower base-emitter resistance, up half its value at room temperature at 45 °C. Since this resistance is shunting the base-emitter capacitance, an integral part of the input ATL, the input matching is anticipated to be affected adversely as seen in the results presented here.

The effects of temperature variation on the performance of SiGe HBT distributed amplifiers are numerous and a more detailed study is required to provide insight as to how measures may be taken to compensate for these effects. Our study here is a major contribution in that direction as this is the first examination of the temperature performance of HBT DAs and highlights a problem that is unique to HBTs.

Chapter 5

Distributed Amplifier Noise Analysis

5.1. Importance and Previous Work

As outlined in the previous chapters there are several disadvantages that are inherent to the distributed amplifier architecture. Compared with cascade architectures, more stages are needed to achieve a given gain, and the number of components, including components required to realize the transmission lines, is higher. This results in more power consumption as well as a higher noise contribution to the receiving system. The noise performance of a UWB wireless system plays a major role in determining the sensitivity of the system. Hence, modeling and reducing noise are of critical importance.

There have been some attempts in the literature to analytically quantify the noise figure of distributed amplifiers. Aitchison calculated the noise figure of distributed amplifiers consisting of MESFET transistors [62], and Iqbal *et al.* derived analytical expressions for the equivalent input noise current spectral density of a high resistivity HBT distributed amplifier for optical receivers [64]. Neither of these analyses actually compares analytical results to measurement data. An improved analysis considering cascode gain cells in a GaAs FET distributed amplifier was published recently by Ko *et al.* [65] showing a good fit between model simulation and measurement. With the increasing number of research groups investigating low-resistivity Si as an alternative for MMICs, significant attention has been paid to studying the noise figure of CMOS DAs, leading to improvements in the noise modeling of CMOS DAs and better agreement with measurement [59]. To date, there has been little analysis of the noise performance of SiGe HBT distributed amplifiers.

Understanding the different contributions to the noise figure of the amplifier gives insight as to how it may be reduced. The remainder of this chapter discusses the noise sources in an HBT and in the cascode cell, and gives an analysis of the noise figure of an HBT DA.

By definition, the noise figure, NF, of a circuit compares the noise at the output of the circuit with the noise at its input, and is defined as [66]:

$$NF = \frac{\text{total output noise}}{\text{output noise due to source}} \quad (5.1)$$

5.2. SiGe HBT Noise Analysis

The transistors used in a DA contribute significantly to the overall noise performance of the amplifier. Figure 5.1 shows the equivalent circuit of a CE HBT with its internal noise sources. An alternative representation of the noise is to replace all the internal noise sources with equivalent noise sources at the input and output, treating the transistor network as noiseless. The equivalent input and output noise sources are shown in dotted lines in Figure 5.1.

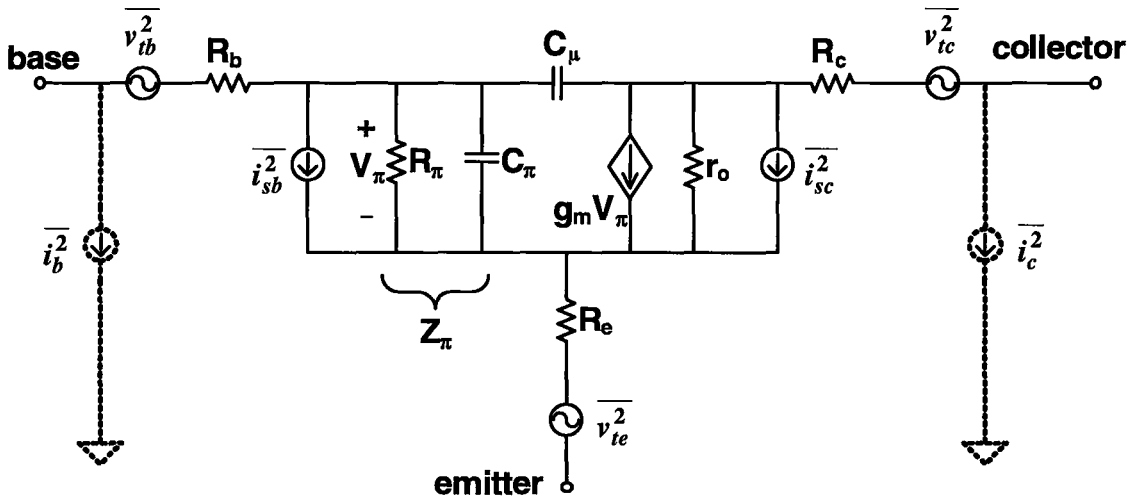


Figure 5.1: Equivalent circuit of CE transistor with intrinsic noise sources and equivalent input and output noise currents

Lumped resistors R_b , R_c , and R_e in the equivalent circuit contribute thermal noise due to the random thermal agitation of carriers. The thermal noise voltage of a resistance R is given by:

$$v_t = \sqrt{4kTBR} \quad (5.2)$$

where B is the noise bandwidth over which the noise measurement is made.

Shot noise is attributed to DC current flowing through the junctions of a transistor. If I is the DC current through a pn junction, shot noise current is given by:

$$i_s = \sqrt{2qIB}. \quad (5.3)$$

Two shot noise sources are shown in Figure 5.1, i_{sb} corresponding to the base-emitter junction, and i_{sc} corresponding to the base-collector junction.

Typically, the impact of the thermal noise due to the collector and emitter resistances is neglected since it is very small compared with the base thermal noise and base and collector shot noises. The expression for the NF of a single CE HBT using a unilateral model, neglecting R_e , R_c , and utilizing the above definitions, was found to be:

$$NF = 1 + \frac{R_b}{R_s} + \frac{(R_s + R_b)^2 qI_B}{2kTR_s} + \frac{(R_s + R_b)\sqrt{2qI_B kTR_b}}{kTR_s} + \frac{qI_C |Z_\pi + R_s + R_b|^2}{g_m^2 2kTR_s |Z_\pi|^2} \quad (5.4)$$

Figure 5.2 shows a comparison between the measured NF of an HBT and that calculated without taking into account v_{te} and v_{tc} and demonstrates that these may be neglected without loss of accuracy.

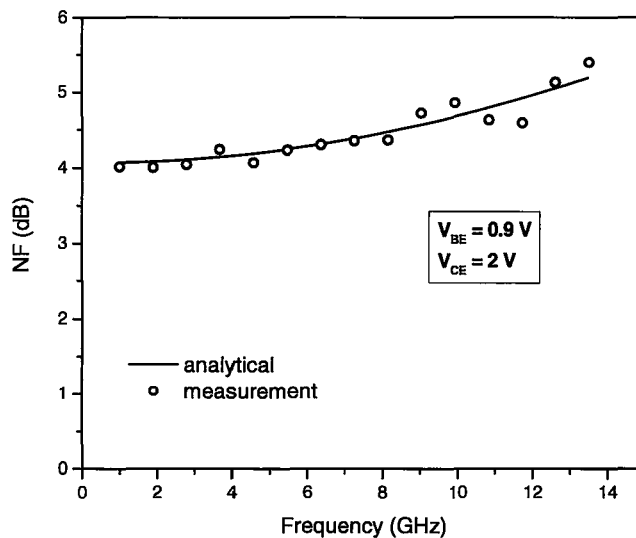


Figure 5.2: Comparison between measurement and analytical calculation of HBT NF. Analytical

expression used does not consider emitter and collector resistance noise sources.

Having multiple noise sources in the equivalent circuit makes analysis difficult when considering the transistor as part of a larger circuit. For this reason, the equivalent circuit with each noise source explicitly included, is replaced with a noiseless network having equivalent noise sources at the input and output terminals. Neglecting the output resistance, and the emitter and collector resistances with their corresponding noise sources, the equivalent input and output current noise sources for an HBT are respectively given by:

$$i_{be} = \frac{-i_{sb}R_{\pi} + v_{tb}[1 + j\omega R_{\pi}(C_{\pi} + C_{\mu})]}{R_{\pi} + r_{tb}[1 + j\omega R_{\pi}(C_{\pi} + C_{\mu})]}, \quad (5.5)$$

$$\text{and } i_{ce} = i_{sc} \quad (5.6)$$

5.3. DA Circuit Noise Analysis

Given the above definition of the noise figure, the calculation of NF of the DA entails identifying each noise source and calculating the noise power delivered to the load due to that noise source. Referring to the discussion of Section 5.2 and the DA design in Figure 4.2, the primary noise contributors may be identified as:

1. Thermal noise from the generator resistance;
 2. Thermal noise from the base line termination load;
 3. Thermal noise from the collector line left hand side termination resistance;
- and
4. Noise associated with each gain cell comprised of cascoded HBTs.

Reference [62] provides analytical expressions for each of the sources listed above as well as for the forward and the reverse gains for a MESFET common source

DA. The gain cells used here are cascode, unlike the common source stages used in [62], but Figure 5.3 shows that the CE transistor of a cascode cell is the main contributor to the output noise as compared to the CB transistor. Furthermore, it can be shown that the equivalent input and output noise current sources of the cascode cell are approximately equal to those of the CE transistor [65]. Hence it is sufficient to consider only the input and output equivalent noise of the CE transistor when calculating the NF of the complete distributed amplifier.

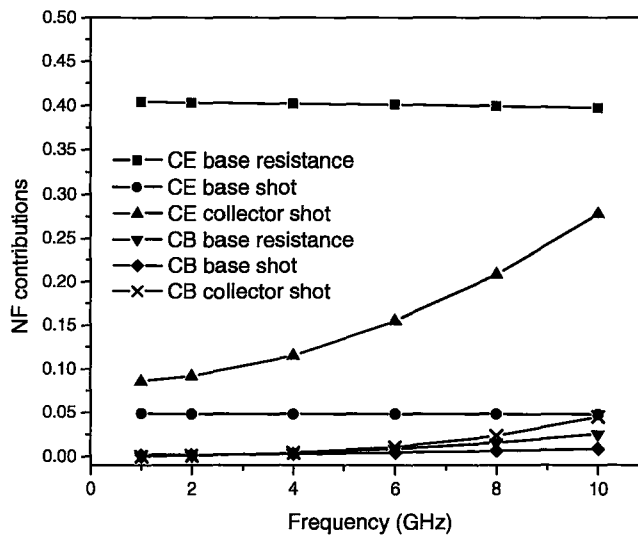


Figure 5.3: Output NF contributions of CE and CB noise sources of cascode cell

The following expression for the NF of a DA may be derived considering all the noise sources mentioned above and assuming phase matching between both input and output lines [62]:

$$NF = 1 + \frac{1}{G} \left(\frac{\sin(n\beta)}{n \sin \beta} \right)^2 + \frac{1}{G} + \frac{1}{kTB \cdot G} \left[\left(\frac{1}{4} g_m Z_{ib} \right)^2 \cdot i_{be}^2 \cdot \sum_{r=1}^n f(r, \beta) + \frac{1}{4} n \cdot i_{ce}^2 \right] \cdot Z_{ic} \quad (5.7)$$

where G is the gain, n the number of stages, i_{be} , i_{ce} the base and collector equivalent noise currents respectively, β the line phase assuming equal base and collector line phases, Z_{ib} , Z_{ic} the base and collector line image impedances and:

$$f(r, \beta) = (n - r + 1)^2 + \left(\frac{\sin(r - 1)\beta}{\sin \beta} \right)^2 + \frac{2(n - r + 1)\sin(r - 1)\beta \cos r\beta}{\sin \beta} \quad (5.8)$$

The image impedances and phase of the lines are themselves complex functions of frequency. It may be seen from equations (5.7) and (5.8) that an accurate determination of their values is critical to predicting the noise figure of the DA. In principle, the image impedances and phase constants may be found from the equivalent sections considering the losses introduced by the transistor loading as seen in Figure 5.4. R_{be} and R_{ce} are the equivalent input and output resistances, and C_{be} and C_{ce} are the equivalent input and output capacitances of the cascode stage. L_b and L_c are the base and collector line inductors and L_s is the shunt inductor of the m -derived section.

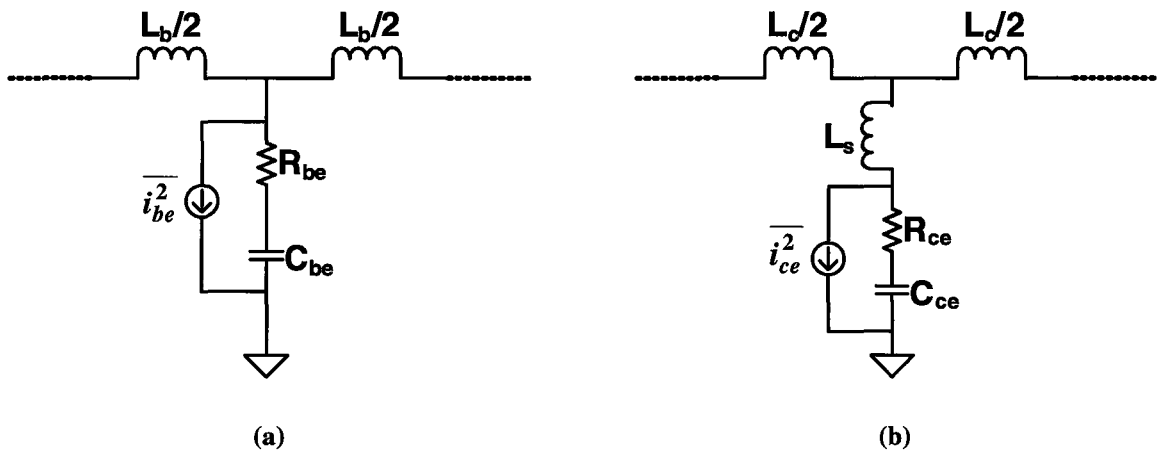


Figure 5.4: Equivalent (a) base line constant- k and (b) collector m -derived sections

There are several effects that would have to be considered to accurately calculate the image impedances and phase constants. The inductors comprising the transmission lines are fabricated over a lossy silicon substrate resulting in significant parasitics. Interconnections introduce additional parasitics that also affect these quantities. To accurately include all these effects would render the problem intractable. However, a model with predictive power may still be obtained using simulations of s -parameters to determine the line image impedances and phase constants. The image impedance is calculated using equations (3.5) and (3.6) and the phase calculated using [24]:

$$\beta = 2n \sin^{-1}(\omega/\omega_c) \quad (5.9)$$

where ω_c is the cut-off frequency. Substituting for these values in equations (5.7) and (5.8) using values for ω_c and the gain, G , extracted from the s -parameters simulations yields the NF shown in Figure 5.5 in comparison to actual measurements.

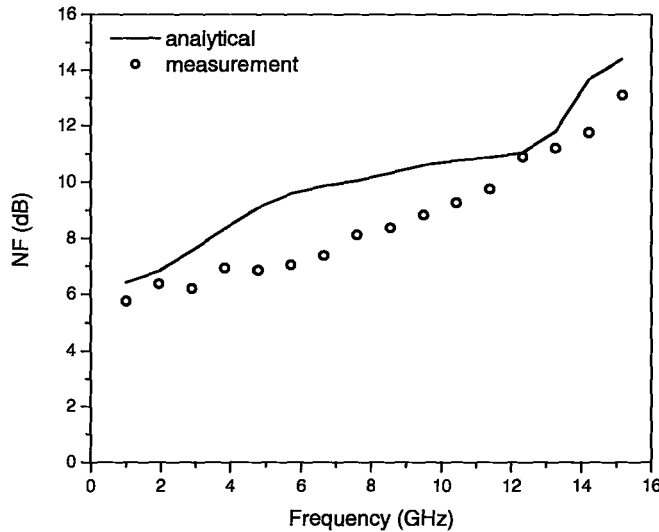


Figure 5.5: Analytically computed NF compared to measured NF of the proposed DA

A few remarks may be made regarding the calculated NF. First, the overall trend as a function of frequency is similar to measured results. Second, the RMS error is 48%,

the maximum error is 77%, and the calculation is conservative, i.e. the NF is overestimated by the calculation. For comparison, conventional circuit simulators grossly underestimate the NF. In the present case, Cadence simulations of the NF were 51% less than measurement. These trends make the calculated NF of considerable value to the circuit designer, and provide confidence in the accurate partitioning of the noise contributions among individual sources. The last observation may allow designers to use noise simulations to explore design options for reducing the NF of the DA.

Even though emitter and collector resistances and their respective noise sources were neglected, the NF calculated was over-estimated, contradicting intuition that it should under-estimate it, as less noise sources are taken into perspective. Their inclusion however, along with the all the losses in the transistors, the lines due to the inductive elements, and interconnections, may produce a more precise estimate of the NF as the expressions in equations (5.7) and (5.8) strongly depend on the image impedance and phase, which in turn rely heavily on these losses. Finally, equations (5.7) and (5.8) may be further refined by taking into account the fact that the phase constants of the input and output lines are different.

Chapter 6

Conclusions

This thesis investigates the design, simulation and experimental results of SiGe HBT distributed amplifiers. SiGe HBTs are new contenders in the field of microwave integrated circuits quickly gaining share in the microelectronics market. Their possession of high operation speeds makes them an attractive alternative to expensive III-V semiconductors in the realization of distributed amplifiers.

Chapter 3 presented the theory behind distributed amplification and the different techniques by which they may be designed. Moreover, a literature review is made comparing the various SiGe HBT DA implementations currently available listing their individual advantages and deficiencies. Capitalizing on that, Chapter 4 considers the design and measurement of a SiGe HBT DA with the goal of reducing power

consumption and to study temperature effects on such an architecture. Chapter 5 analyzes the noise in a SiGe HBT DA comparing it to experimental results.

The following sections summarize the contributions achieved in this work followed by recommendations for future work

6.1. Contributions

This thesis presents and analyzes a novel cascode implementations of a SiGe HBT distributed amplifier. Relatively high gain and bandwidth were achieved suitable for UWB applications at the lowest power consumption reported thus far for a distributed amplifier of any type. This demonstrates that such amplifiers not only may be used in optical communication systems, but also wireless portable devices.

For the first time, the impact of temperature variation on such amplifiers was observed and found to detrimentally affect the gain. The gain was found to decrease significantly for a ~ 25 °C increase above room temperature failing to meet the normal range of operation temperatures required for any consumer circuit. This effect was attributed mainly to the deterioration of the input matching due to the high dependence of the transistor operation on temperature, changing its input impedance drastically. Such an observation poses the question as to the feasibility of using SiGe HBTs in distributed amplifiers for consumer electronics.

Furthermore, this work investigated for the first time the noise intrinsic to SiGe HBT distributed amplifiers. The analysis performed, built on simulation models and values only, accounts for the noise contributions of the passives and the transistors used. Accordingly, simulated results attained closely matched measured results making this

analysis sufficient for preliminary predictions of the noise figure of SiGe HBT DAs during the circuit design stage. Such an analysis proves convenient to provide insight as to how to reduce noise in future SiGe HBT DA designs.

6.2. Future Work

This is one of the first SiGe HBT distributed amplifier circuits designed and many improvements may be made upon it. Incorporating many factors discarded in this design may enhance the gain and bandwidth. Losses due to transistors and transmission lines used were a major issue in this design and should be taken into account in the future. Losses due to transistor loading may be accounted for by implementing a loss compensation technique. Higher quality factor inductors should be investigated and interconnections optimized to reduce parasitic effects. Coplanar waveguides can be used as interconnections to reduce the probability of instability due to extending ground lines as witnessed in this design. Moreover, to fully exploit the advantages of SiGe HBTs a more modern SiGe process should be used to achieve higher gain-bandwidth products.

The influence of temperature variation on SiGe HBT DAs should be more rigorously studied. Temperature effects on the transistors should be analyzed and parameters be extracted from test structures to more precisely identify the cause of the variability observed. Furthermore, the effect of cooling on SiGe HBT DAs is of interest.

Lastly, more analysis needs to be performed on the noise model of SiGe HBT distributed amplifiers. Test structures for transmission lines and cascode cells used should be developed to extract experimental data that may aid in providing better insight towards calculating quantities such as gain cell input and output impedances, equivalent noise

sources, and transmission line impedance and phase constants. CPWs may be used to provide distinct stages with consistent interconnection. This allows for proper signal feed and ground extensions, consequently improving circuit layout and relatively simplifying its analysis. Furthermore, more noise sources and effects such as parasitics may be taken into consideration to produce a more precise noise analysis.

APPENDICES

Appendix A

S – PARAMETERS

“Scattering parameters” or s -parameters are a parameter set that relates traveling waves that are scattered, or reflected, upon insertion of a DUT (Device Under Test) into a transmission line. They are commonly used in describing microwave systems. Other parameter sets such as Z - or Y -parameters are concerned with measuring terminal voltages and currents under successive open and short circuit conditions. Such conditions prove to be difficult when measuring in the microwave frequency range as lead inductances and capacitances make perfect open and short circuits hard to obtain. Also, conventional methods require tuning stubs to provide the required condition at each frequency of measurement. This not only proves tedious, but also may cause the DUT to oscillate.

S -parameters are usually measured with the DUT embedded between a $50\ \Omega$ source and $50\ \Omega$ load, which practically eliminates the danger of oscillation. Figure A.1 shows a two-port network and incident and reflected waves.

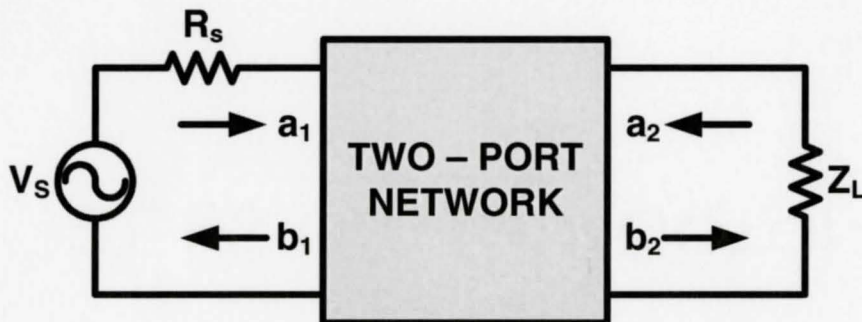


Figure A.1: A two-port network showing incident (a_1 , a_2) and reflected (b_1 , b_2) waves

The following equations describe the 2-port network in terms of s -parameters:

$$b_1 = S_{11} \cdot a_1 + S_{12} \cdot a_2 \quad (\text{A.1})$$

$$b_2 = S_{21} \cdot a_1 + S_{22} \cdot a_2 \quad (\text{A.2})$$

where a_1 , a_2 , b_1 , and b_2 are the amplitudes of the forward and backward traveling waves seen from the input and output ports as indicated in the figure, and:

$$S_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=0} = \text{Input reflection coefficient with output port matched} \quad (\text{A.3})$$

$$S_{22} = \left. \frac{b_2}{a_2} \right|_{a_1=0} = \text{Output reflection coefficient with input port matched} \quad (\text{A.4})$$

$$S_{21} = \left. \frac{b_2}{a_1} \right|_{a_2=0} = \text{Forward transmission gain with output port matched} \quad (\text{A.5})$$

$$S_{12} = \left. \frac{b_1}{a_2} \right|_{a_1=0} = \text{Reverse transmission gain with input port matched} \quad (\text{A.6})$$

Unlike other parameter systems, which deal with voltage and current signals, the previous definitions may be used to find power gain and mismatch loss through the following equations:

$$|S_{11}|^2 = \frac{\text{Power reflected from the network input}}{\text{Power incident on the network input}} \quad (\text{A.7})$$

$$|S_{22}|^2 = \frac{\text{Power reflected from the network output}}{\text{Power incident on the network output}} \quad (\text{A.8})$$

$$|S_{21}|^2 = \frac{\text{Power delivered to a } Z_o \text{ load}}{\text{Power available from a } Z_o \text{ source}} = \text{power gain} \quad (\text{A.9})$$

$$|S_{12}|^2 = \text{reverse power gain with } Z_o \text{ load and source} \quad (\text{A.10})$$

Appendix B

EXPERIMENTAL SETUP

B.1. S-Parameters Measurement

Scattering parameters and DC on-chip measurements may be performed using the setup detailed in Figure B.1. The DUT, in this case the amplifier, is placed on a conductive gold-plated chuck in a probe station, which allows easy manipulation of RF, and DC probes. The chuck is connected to the Temptronic TP0315A digital programmable thermal inducing platform, which may be used to heat chips up to 200 °C.

The *s*-parameters are measured using the Agilent 8722ES S-Parameters Vector Network Analyzer that may conduct measurements over a range of 0.5 MHz – 40 GHz. Since the DUT here requires DC bias feeds coinciding with the RF lines, the DC bias is input to the network analyzer which has internal bias T's to couple the RF and DC signals together. The resultant signal is output from the network analyzer through PORT1 and PORT2 over 2 RF cables with 2.4 mm connectors. The other ends of these cables are connected to GGB Inc. 3-point picoprobes via 3.5 mm connectors and in turn to the DUT's input and output pads.

The Agilent 4156C Precision Semiconductor Parameter Analyzer provides the DC biasing required through Source-Measure Units and Voltage Source Units. SMUs present the capability to provide a voltage source and measure the drawn current whereas VSUs just supply voltage. An SMU is used at the output to provide the V_{CC} bias and

measure the current to calculate the power the circuit consumes. VSUs can be used to supply V_{BB1} and V_{BB2} as the base currents are not of major concern when calculating the power. Regardless, V_{BB1} was monitored using an SMU and V_{BB2} supplied from a VSU via a DC probe needle.

For temperature dependent measurements, the chuck was heated at preprogrammed temperatures with a wait period of approximately 20 – 30 minutes to ensure that the sample is at the same temperature. Temperature measurements were conducted in an ascending manner as when cooling, the chuck takes a much longer time to reach the specified temperature. A final note is that the RF cables and probes introduce parasitic inductances and resistances to the input and output ports of the circuit. These elements should be taken into consideration and be removed by calibration of the entire setup using calibration substrate open, short and through structures.

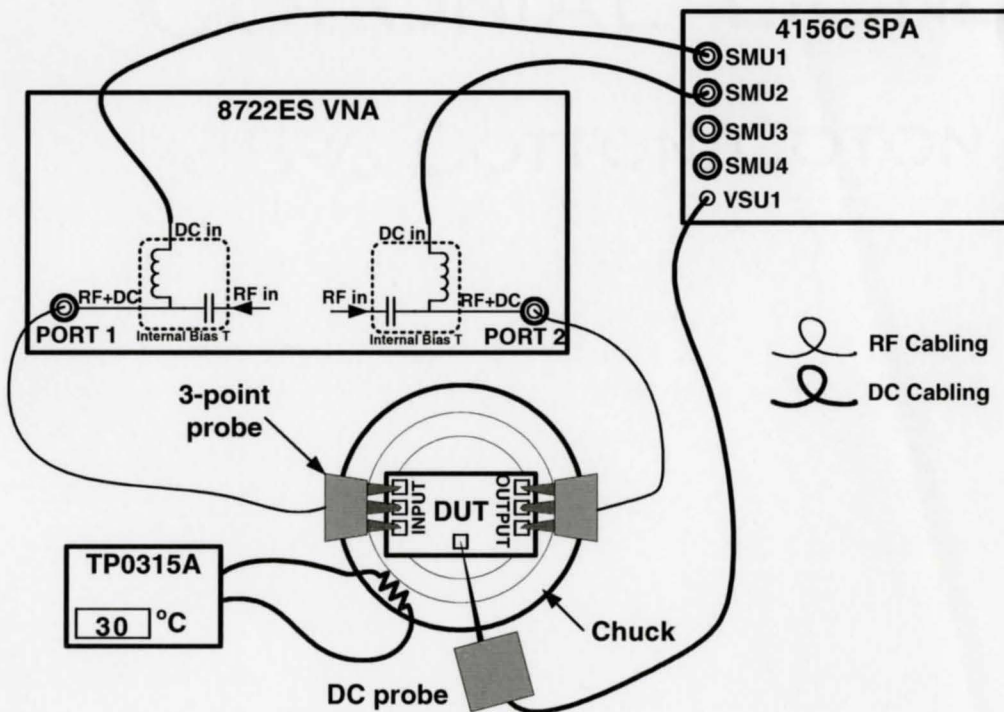


Figure B.1: Experimental setup for DC and s-parameter measurements

B.2. Noise Figure Measurement

As in the s -parameters measurement, the DUT is placed on the conducting chuck in the probe station and 3-point and DC probes are used to supply the noise signal and DC biasing. Likewise the 4156C SPA is used to supply and monitor the DC biasing and the TP0315A is used for temperature dependent measurements.

The Agilent N8975A Noise Figure Analyzer is used to perform the noise measurements and may operate from 10 MHz – 26.5 GHz. It supplies a 28 V level DC voltage to switch on an HP 346C noise source, which in turn is connected to a bias T, coupled with V_{BB1} bias voltage on SMU1, which in turn is connected via RF cable and probes to the input pads. The V_{CC} voltage is fed into the output of the DUT through another bias T and the RF signal is filtered to the 50 Ω input connector for the NFA. The DC voltage, V_{BB2} , is supplied via DC cable and probe. All RF cables used have 3.5 mm precision connectors.

The Excess Noise Ratio, ENR, of the noise source used must be entered into the NFA. The ENR is used to describe the output of the noise source used as an input stimulus. These values are entered for the frequency points at which the measurements will be made in tabular form. An important note is that the number of measurement points and averaging used dictate the total time the measurements will take. The NFA displays both measured gain and NF. Once the correct ENR values are input if the output of the noise source is directly input into the NFA, then the NF displayed should be around zero.

Once measurements have started, it was observed that the gain provided by the NFA was significantly different from that measured using the s -parameter vector network

analyzer explained in the previous section. This is contrary to what one may expect, that the two gains match, and the disagreement is shown in Figure B.3(a). This discrepancy is attributed to the losses due to the connectors and RF cabling used. To compensate for these losses the noise source, bias T and RF cable at the DUT input are directly connected to the NFA input to measure their loss for the required frequency points. These values are then entered into the loss compensation before DUT table in the NFA and the same procedure is followed for the output with losses recorded in the after DUT table. Care should also be taken to enter the correct temperature at which the loss measurements are being conducted. After taking into consideration the losses the measurements are conducted and as shown in Figure B.3(b) the gain produced by the NFA is found to be in good agreement to that of the s -parameter network analyzer and hence the noise figure measured may be accepted with a good degree of confidence.

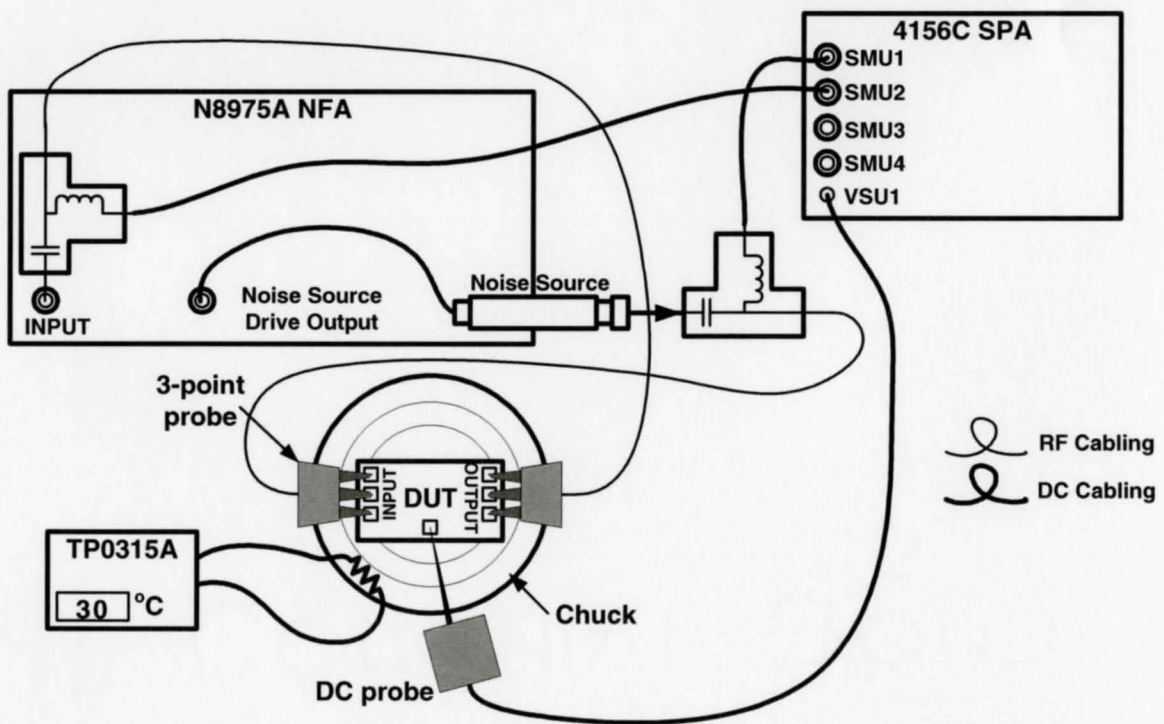


Figure B.2: Experimental setup for noise figure measurement

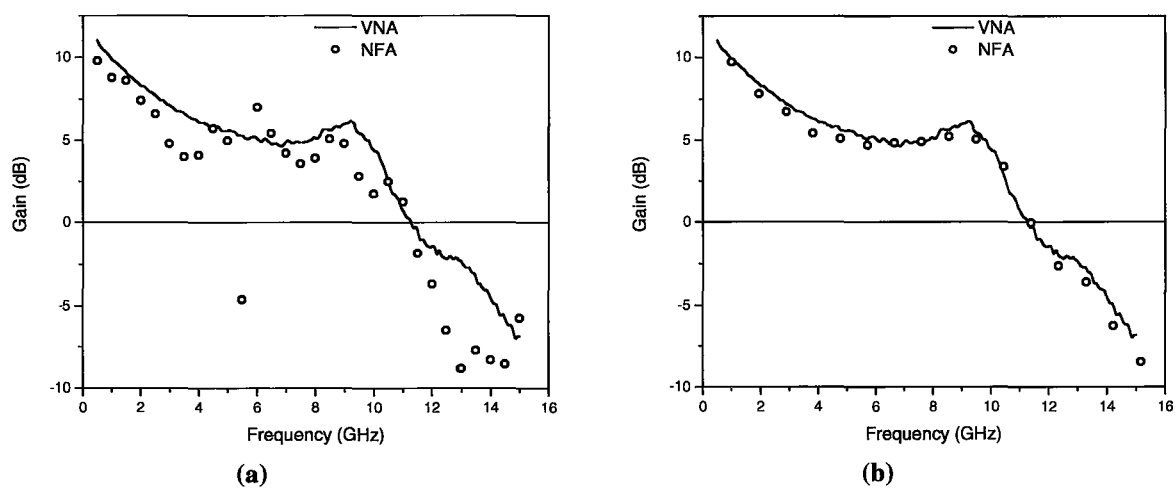


Figure B.3: Comparison between gain from NFA and VNA (a) without and (b) with loss compensation

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