

ECR PECVD OF SION FILMS FOR FLAT PANEL DISPLAYS

**ELECTRON CYCLOTRON RESONANCE CHEMICAL VAPOUR
DEPOSITION OF SiO_xN_y FILMS FOR USE IN FLAT PANEL
DISPLAYS**

BY

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ABSTRACT

Thin silicon based films were produced using low temperature (less than 60° C) electron cyclotron resonance plasma enhanced chemical vapour deposition (ECR PECVD). These films were examined for suitability in flat panel display applications. SiO_xN_y films were tested for use as insulating films in thin film electroluminescent (TFEL) devices. The ECR PECVD method was found to be suitable when the plasma was created using pure nitrogen (as opposed to argon) in high ratios to the silane precursor.

Hydrogenated silicon films were also produced and evaluated for their suitability as semiconductor layers in thin film transistors (TFTs). The silicon films were subject to nickel induced crystallization. The silicon films were found to crystallize at low temperatures, (<950° C) in the presence of nickel. These films were used to produce prototype metal insulator semiconductor (MIS) capacitors and TFTs.

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1 INTRODUCTION

1.1 *Motivation*

The motivation behind this work is the industrial requirement of high quality thin films for flat panel display applications. The flat panel display industry is currently experiencing tremendous growth based on the increase in the need for low cost, low power information displays. Flat panel displays have many advantages over conventional displays, such as the ruggedness, viewing angle, power consumption, ease of manufacture and portability. There are several different types of flat panel displays, such as liquid crystal displays (LCDs), thin film electroluminescent (TFEL) and organic light emitting diodes (OLEDs), of which the last two are of particular concern. These devices typically require the deposition of thin films of varying materials. In particular, TFEL displays require high quality dielectric materials, which are incorporated directly into the devices. Both TFEL and OLED displays require addressing arrays of thin film transistors (TFTs), which require high quality gate dielectrics. In addition, there is a requirement for polycrystalline silicon thin films for the transistors arrays, which are integral to active matrix (AM) addressing schemes.

This work focuses on the use of silicon-based materials produced in an electron cyclotron resonance plasma enhanced chemical vapour deposition (ECR PECVD) chamber for use in flat panel display applications. Silicon based films are produced and characterized for use in three distinct applications. First, silicon oxynitride (SiON) films are analyzed as dielectric insulators in thin film electroluminescent structures, in which ZnS doped with Mn

is the active material. Secondly, SiON films are analyzed as gate dielectrics in silicon based thin film transistors. In both of these cases, the investigations focus on ECR deposition at low temperatures ($<60^{\circ}\text{C}$). Lastly, amorphous silicon films are produced and characterized as the active semiconductor material in thin film transistors. In this case, the focus is on the production and characterization of TFTs made with metal-induced crystallized silicon. Historically, silicon oxynitrides have been produced for flat panel display applications through several methods such as sputtering, low pressure chemical vapor deposition (LPCVD) and, more recently, ion-assisted physical vapour deposition. These methods and the films they produce are assessed and serve as a benchmark for the assessment of the ECR PECVD method of film deposition for use in flat panel displays.

This thesis is organized as follows. In chapter 2, the techniques of device fabrication and analysis are discussed. In chapter 3, the experimental procedures are outlined. In chapter 4, the results obtained are listed and discussed. Chapter 5 gives a brief discussion of the examination of prototype devices produced using nickel induced crystallized silicon films. Chapter 6 summarizes the thesis and gives conclusions.

2 TECHNOLOGY BACKGROUND

2.1 *The Metal Insulator Semiconductor (MIS) Capacitor*

2.1.1 *The Ideal MIS-Capacitor*

In order to examine the interface states and dielectric properties of an insulator, metal-insulator-semiconductor (MIS) capacitors are constructed. The MIS capacitor consists of a metallic contact (aluminum), an insulator (SiO_xN_y in this case), and a semiconductor (c-Si, a-Si:H and polysilicon). In the ideal case, several assumptions must be made; the gate is thick enough to be considered an equipotential region, the oxide is a perfect insulator, there are no oxide or interface charge centers, the semiconductor is uniformly doped, the semiconductor is thick enough to allow for the establishment of a field free region before the back contact, the metallic contacts are ohmic, the device is one dimensional, and the work functions of the gate metal and semiconductor are the same. With the above assumptions, the junction appears as shown in figure 2.-1¹, at zero applied voltage. In the figure; Φ_M is the metal workfunction, Φ'_M is the effective metal workfunction, χ is the semiconductor electron affinity, χ' is the effective semiconductor electron affinity, χ_i is the insulator electron affinity, E_0 is the vacuum level, E_C is the minimum conduction band energy, E_F is the Fermi level, and E_V is the maximum valence band energy.

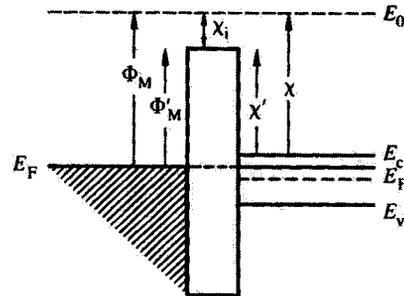


Figure 2-1 Band Structure of an Ideal MIS under Zero Bias¹.

When operating the device the back side is held at ground potential and a DC bias, V_g , is applied to the gate. Under applied bias, the Fermi level of the semiconductor does not change but the Fermi level of the metal is shifted by an amount $-qV_g$. As the barrier heights are fixed, the applied voltage causes band bending in the semiconductor and oxide layers.

There are three distinct biasing regions (in addition to the flat band condition); accumulation, depletion and inversion, which can be readily distinguished in figure 2-2¹. In a p-type Si device, a negative applied gate voltage will cause an accumulation of positive charge at the semiconductor-oxide interface. There will be negative sloping of the energy bands in both the oxide and the semiconductor, figure 2.-2b). This is the accumulation region. A small positive voltage on the gate will lower the Fermi level in the metal, causing

the majority carrier concentration to decrease in the region of the oxide. This will cause positive sloping of the energy bands. When the electron and hole concentrations near the oxide-semiconductor interface are less than the bulk levels, the situation is referred to as depletion, figure 2-2c. When a large positive voltage is applied to the gate, the electron concentration at the oxide-semiconductor surface will increase. This is the inversion biasing region, figure 2-2d. In the ideal device, the dividing line between depletion and inversion can be found when $V_g=0$. This is referred to as the flat band condition where no band bending occurs, figure 2-2a.

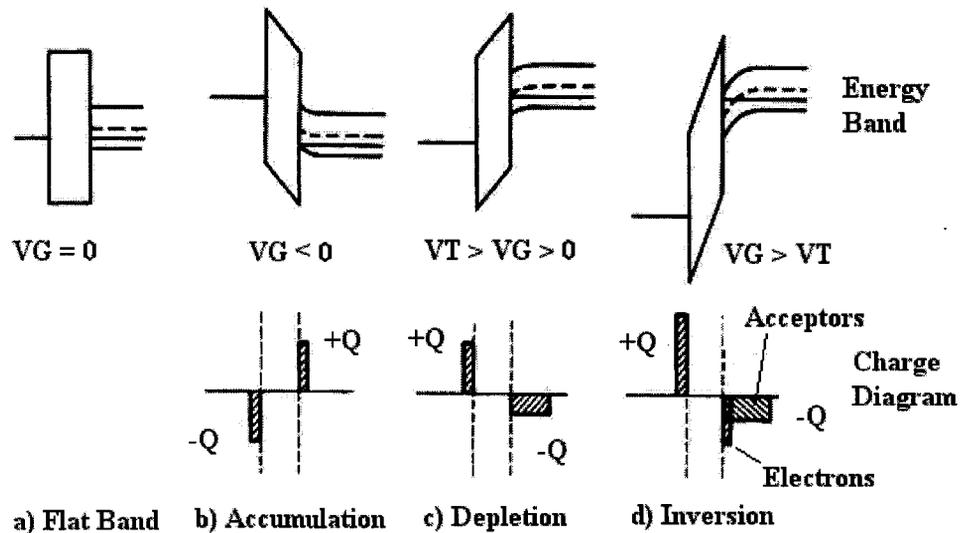


Figure 2-2 Band Structure in Differing Bias Regions¹.

The capacitance of the device consists of the oxide capacitance, $C_o = K_s \epsilon_o A / X_o$, where K_s is the dielectric constant of the oxide layer, A is the area of the device, and X_o is the oxide thickness, in series with the capacitance created by the depletion region in the semiconductor, C_s . The depletion width, W_s , is defined as,

$$W_s = [2K_s \epsilon_o / q N_a * Q_s]^{1/2}, \quad 2-1$$

Where K_s is the dielectric constant of the semiconductor, N_a is the acceptor concentration, and Q_s is the semiconductor work function. The device capacitance is then,

$$C = C_o / (1 + K_o W / K_s X_o X) \quad \text{depletion} \quad 2-2a$$

$$C = C_o \quad \text{accumulation} \quad 2-2b$$

$$C = C_o \quad \text{inversion, low frequency} \quad 2-2c$$

$$C = C_o / (1 + K_o W_T / K_s X_o) \quad \text{inversion, high frequency} \quad 2-2d$$

As the depletion region expands, the depletion capacitance and hence the total capacitance decreases.

Increased reverse bias results in an induced inversion region and minority carriers are created. This region will increase only slightly with voltage, giving the capacitance voltage curve a flat region. Reverse bias beyond this point will result in an increase in the field across the oxide, and eventual breakdown of the film.

2.1.2 The Non-Ideal MIS

There are several deviations from the ideal MIS capacitor that regularly occur in real devices²⁻¹⁶. The work functions of the gate and semiconductor materials are seldom identical. This creates an electric field in the dielectric and semiconductor, and causes band bending in the semiconductor. The work function of the metal is typically less than that of the semiconductor. In a p-type device this will cause a negative shift in the C-V curve, with flat band conditions occurring at an applied voltage equal to the work function difference, figure 2-3¹. In the figure, Φ_{MS} is the metal-semiconductor workfunction difference expressed in volts.

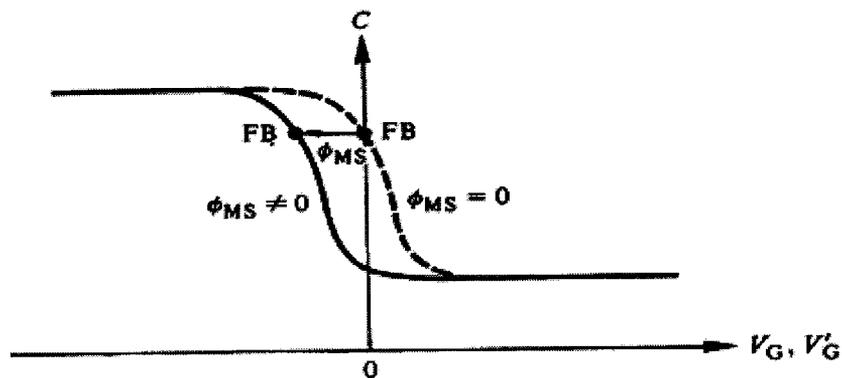


Figure 2-3 Effect of Work Function Difference¹.

Three additional areas of concern are surface states, fixed charge and mobile ions. As most of the activity in a MIS device occurs near the surface as defined by W_T , the depletion depth, artifacts at the surface are crucial. The surface states are associated with a time

constant, t , and an energy level. When applying a bias, only those states near the Fermi level at the semiconductor surface will be affected. As these states are also frequency dependent, they can be probed as a function of applied frequency. At frequencies well above $1/t$, only the oxide capacitance will be measured. The surface state capacitance appears in series with the depletion capacitance and increases the overall capacitance.

When depositing a metal or insulator layer on a semiconductor, a thin disordered semiconductor layer is created. The energy states created are a function of fluctuations in bond length, angle due to stress and interface irregularity. These are the disorder induced gap states (DIGS)⁵, figure 2-4. Figure 2-4 b) maps the surface state density N_{SS} versus the energy state, and three disorder regions are identified. Region I, is defined by the energy state distribution of an ordered insulator-semiconductor (I-S) interface. Region II is defined by a disordered I-S interface and region III is defined by a metal-insulator interface. The interface states in the upper half of the band gap are acceptor like, negative when filled. The states in the lower half of the band gap are donor like, positively charged when empty.

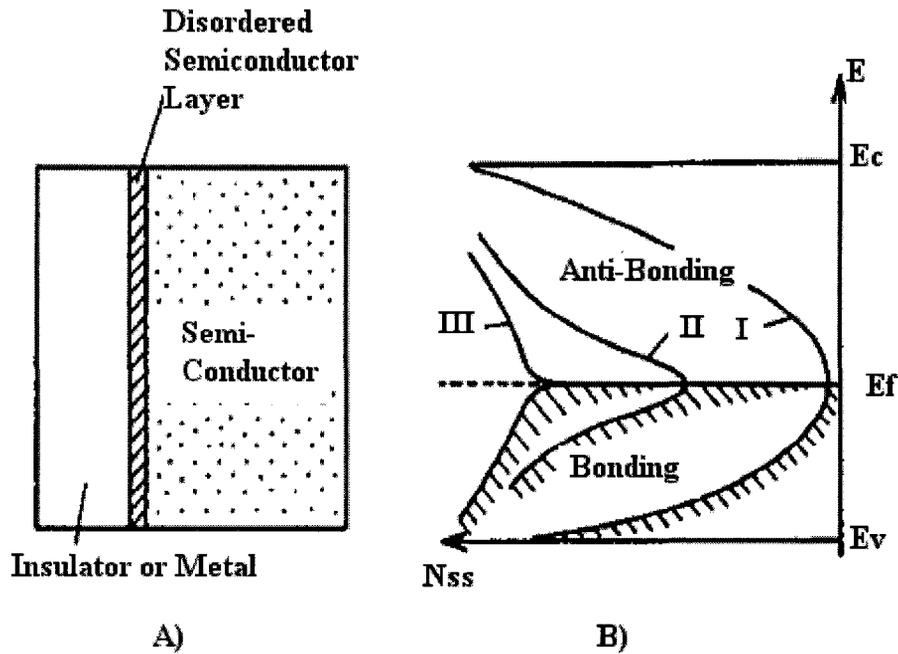


Figure 2-4 Disorder Induced Gap States⁵.

Mobile ions plagued MOS devices at their inception. They consisted of free sodium ions that could migrate through the device, creating charge build-up. If a gate is biased for an extended period of time, charge of the opposite sign builds up at the oxide interface, and shifts the C-V curve tens of volts, figure 2-5¹. Biasing while heating the substrate increases the effect as it increases the ion mobility. In CVD films, deposited from Si-H_4 and NH_3 , free hydrogen is a major concern¹⁷⁻³⁰.

Fixed charge refers to charge residing in the oxide, close to the oxide-semiconductor interface. This charge will also shift the C-V characteristics by several volts.

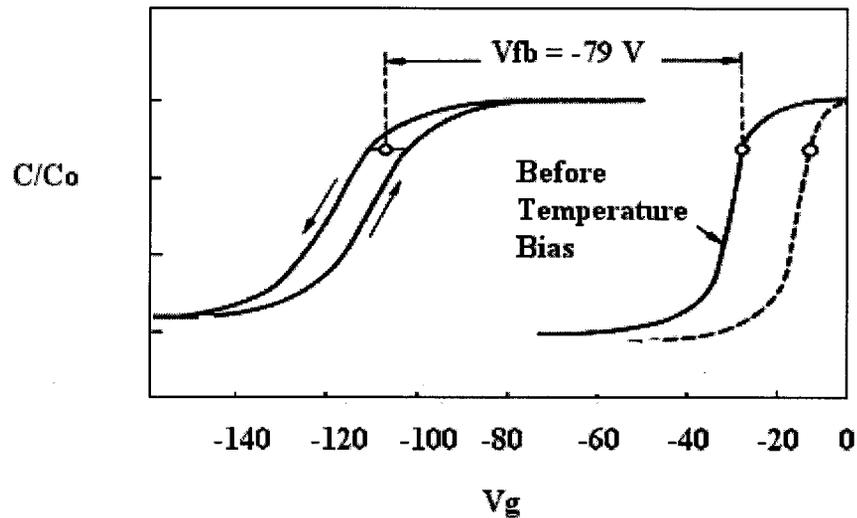


Figure 2-5 Effect of Mobile Ions¹.

Silicon dangling bonds in SiON films have been shown to create trap states, which allow hopping conduction. The absence of a single nitrogen (or oxygen) atom in the film can create 3 silicon dangling bonds. Figure 2-6¹⁶ shows that these silicon traps can exist in 3 charged states. As the trap states capture or emit electrons they will emit or capture holes. When the metal electrode of a MIS capacitor is made positive, the trap state will capture an electron. When the electrode is made negative, the trap will emit an electron and return to a neutral state. When the electrode negative voltage is increased, the trap will emit another electron and turn positive. During CVD, high nitrogen (or oxygen)/silane ratios will provide stoichiometric films and can reduce the dangling bond density.

2.2 Capacitance Voltage Measurements.

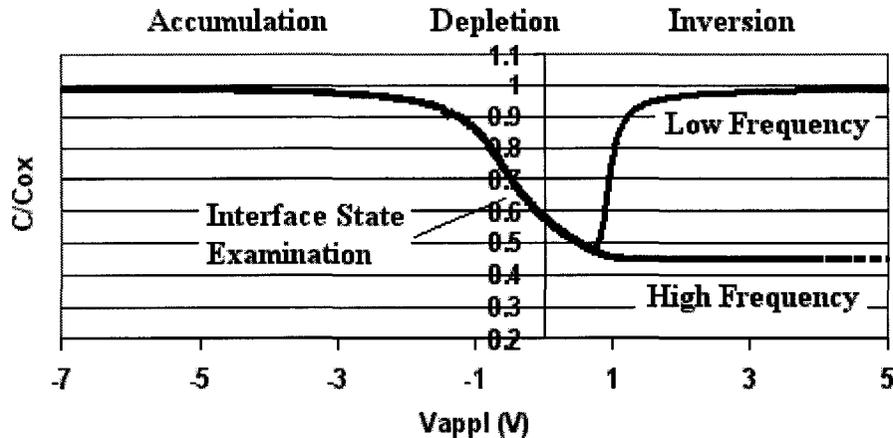


Figure 2-7 Typical Capacitance-Voltage Curves

Many MIS device characteristics can be determined from high and low frequency capacitance-voltage (C-V) measurements³¹⁻³⁴. Typical C-V curves for a p-type MIS capacitor are shown in figure 2.17. A small AC signal, 15 mV, is applied with a DC voltage across the test device and a sense component. The ac response of the device is then measured for the quasistatic and high frequency (typically 1 MHz) cases. The response is dependent on the frequency of the applied ac signal and the DC bias. The mechanism involved can be examined by looking at the three voltage regimes in a MIS capacitor, accumulation, depletion, and inversion.

In accumulation, in a p-type MIS-C, the ac response will be independent of the DC bias. This region is dominated by the majority carriers, in this case holes, which respond to the high frequency ac signal due to their high mobility.

The depletion region, W , is characterized by the withdrawal of majority carriers from a depth W_t in the semiconductor. The capacitance initially decreases with decreasing DC signal as the effective capacitor thickness increases with W . The effective capacitance is given by the oxide and semiconductor capacitance in series. However, the response to the ac signal remains as the majority carriers still dominate.

In inversion the charge fluctuation and hence, effective capacitance, depends on the frequency of the AC signal due to the involvement of minority carriers with much lower mobilities. As the charge on the metal side of the oxide fluctuates at high frequency, the minority carriers cannot respond fast enough to counter this charge. The charge is compensated for by changes in the depletion layer, which will result in a reduced change in charge for a given applied ac voltage. For low frequencies, the minority carriers can respond and charge will accumulate at the oxide-semiconductor interface.

The effect of surface states in MIS capacitors is important. By definition, surface states exist near the oxide-semiconductor interface. Each state will have a specific energy level and time constant. The added capacitance will appear in series with the depletion capacitance but the surface states will not respond to high frequencies as the depletion capacitance will. By varying the bias current, each state can be probed.

2.3 Thin Film Electroluminescent Displays

A typical TFEL³⁵⁻⁴⁶ device consists of a semiconductor phosphor layer that acts as a host material for an emissive center, sandwiched between two insulating layers. There are

additional references available⁴⁷⁻⁸⁶. Figure 2-8 illustrates the functioning of the device. The most efficient devices to date are a combination of a host material of ZnS doped with approximately 0.5% Mn acting as the emissive center. The insulating layers are used to limit current through the device as defects that create conduction paths would allow high current to flow through the phosphor. Electrons tunnel out of interface states at the phosphor/dielectric interface and are ballistically accelerated in the conduction band of the phosphor. Strong internal fields are created by the accumulation of charge at the opposite insulator/phosphor interface. Tunneling efficiencies depend on the interface state densities as well as bulk defect densities in the vicinity of the interface, which may recapture these electrons.

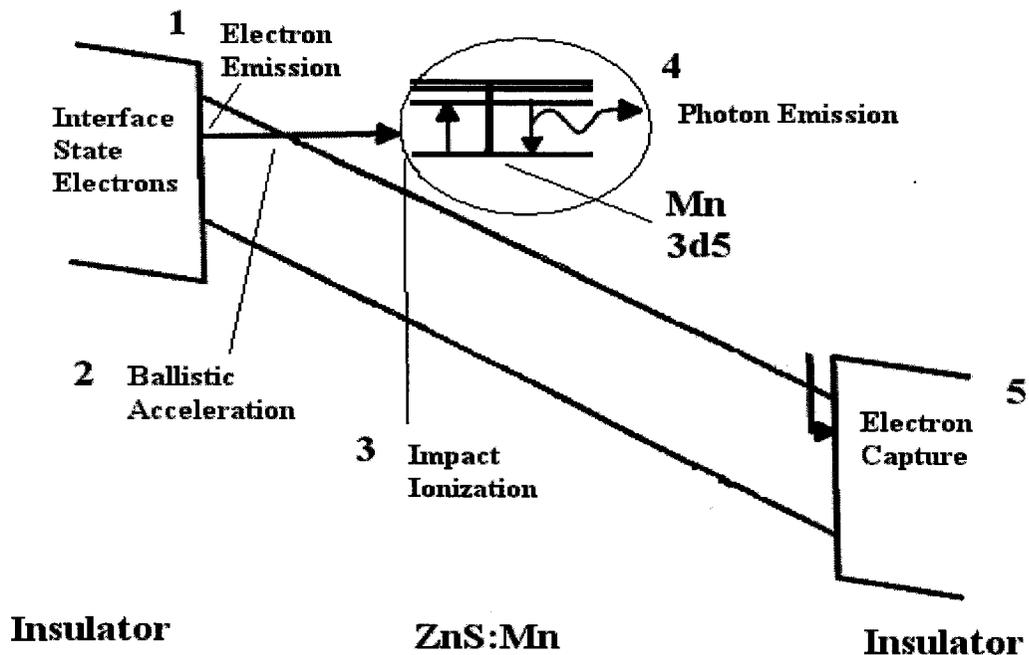


Figure 2-8 Functional Schematic of TFEL Device

Impact ionization of impurity atoms, Mn in this case, can occur when impacted by high-energy electrons. Ballistic electrons with 2.5 eV of kinetic energy are sufficient to ionize Mn. It has been shown that, with the requirement of 2.5 eV for ionization of Mn, a phosphor thickness of 550 nm will produce the highest efficiency. This is a balance of several factors including recapture of electrons by traps, and the distance required to accelerate an electron to an energy of 2.5 eV. In a typical device using ZnS as the host material, the approximate average breakdown field in the phosphor is about 1.5 MV/cm with 7 eV required for band to band ionization, which then has a low probability.

The de-excitation of electrons in the impurity ion, Mn, from one level to another, produces a visible photon. Few efficient emitter dopants have been identified due to the severe demands on the atom. The energy gaps must produce visible light, the excitation cross section must be large enough for efficient emission, and the excited states must be stable in high fields. Excitation of manganese occurs deep in the 3d shell, with the 3d⁵ electron. This state is stable in high fields due to shielding by the other electrons. Also, the excitation cross section is large, $\sigma = 4 \times 10^{-16} \text{ cm}^2$, twice the geometrical cross section of the 3d⁵ Mn²⁺ electron.

An electrical model of this device is shown in figure 2-9³⁶. As the device is capacitive, only a displacement current can flow and the device must be driven AC. Below threshold the phosphor acts like a dielectric and the entire device acts like a capacitor, with the insulator and phosphor

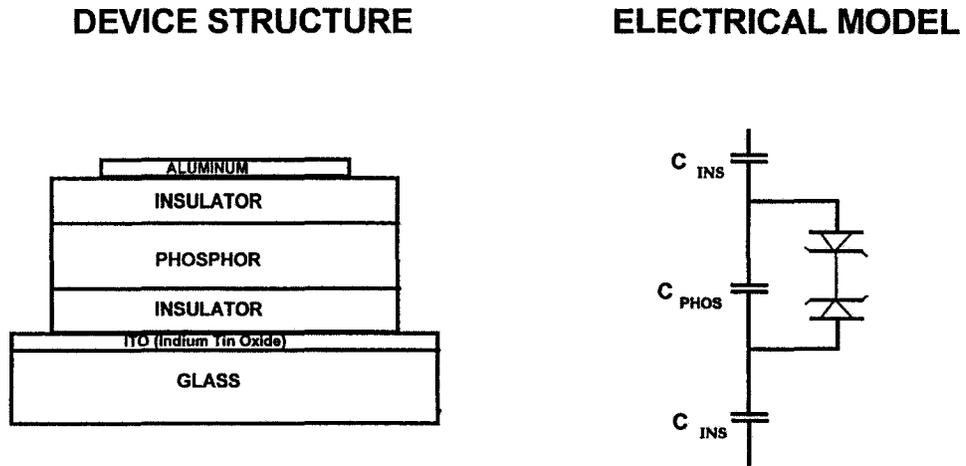


Figure 2-9 TFEL Device³⁶.

capacitance in series. Above threshold the phosphor can be modeled as back-to-back Zener diodes and only the capacitance of the insulator exists. A typical Q-V curve is shown in figure 2-10. The most notable feature of the device shown in the figure is field clamping as seen by the two distinct slopes. After phosphor breakdown, the device capacitance changes from $C_i C_p / (C_i + C_p)$ to C_i . As electrons are accelerated to the anode, charge builds up at the interface creating an opposing internal field, which keeps the phosphor field clamped at the threshold level. In addition, the charge transfer can be determined through, $dQ_e = \alpha dQ_z$, where $\alpha = C_i C_p / (C_i + C_p)$.

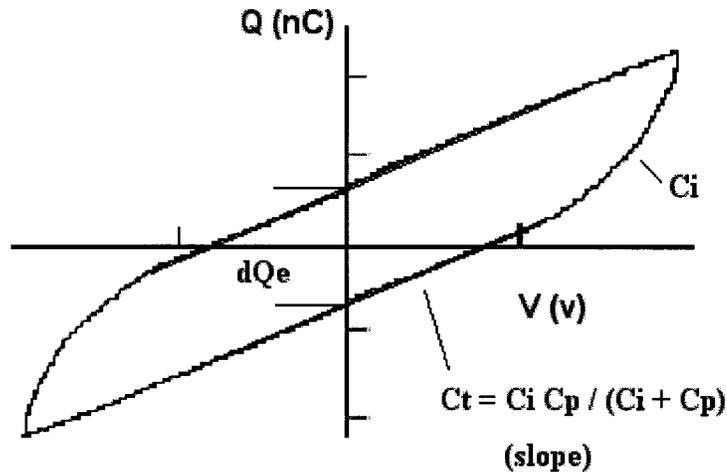


Figure 2-10 TFEL QV Characteristics

The steady state transfer charge is given by,

$$Q = 2 C_i (V_a - V_{at}), \quad 2-3$$

with V_{at} the voltage at threshold and V_a the applied voltage. The charge is transferred at the threshold field, E_t across a phosphor thickness dz , doing work,

$$W = 2 C_i (V_a - V_{at}) E_{zt} dz = 2 C_i (V_a - V_{at}) V_t. \quad 2-4$$

This gives the equation for power consumed,

$$P = 2fC_i V_{app} V_{th}, \quad 2-5$$

where f is the voltage pulse frequency, C_i is the insulator capacitance, V_{app} is the external voltage applied above threshold, and V_{th} is the threshold voltage.

The luminance efficiency is determined by the power consumption and by the internal and external efficiencies. The external efficiency is determined by the outcoupling efficiency. As the phosphor has a high refractive index, ~ 2.3 , at the wavelengths of interest, (400nm to 650 nm), and the insulator, ITO and glass layer indices are 1.6, 1.75 and 1.5, outcoupling efficiency can be poor if care is not taken in determining the layer thickness. In order to allow for the emission of light without absorption, the phosphor, and insulators, must have a large band gap, > 2.5 eV. Also, the impact excitation cross section of the excitation center (Mn in this case) must be large to obtain efficient light emission. The luminance efficiency can be expressed as,

$$\mathbf{L} = 4 \eta f C_i (V_a - V_{at}) V_t, \quad \mathbf{2-6}$$

when the device is driven at frequency f and the efficiency, η , a combination of internal and external efficiencies. With $C_i = \epsilon_0 \epsilon_i / d_i$ and $V_t = dz E_z t$, the equation becomes

$$\mathbf{L} = 4 \eta f \epsilon_0 \epsilon_i (dz/di) E_t (V_a - V_{at}) . \quad \mathbf{2-7}$$

Thus the dielectric layer thicknesses should be minimized and the dielectric constant should be as high as possible. Due to the field clamping of the phosphor, all of the voltage above threshold is transferred to the dielectric, $(V_a - V_{at}) = (Q_i - Q_z)/C_i$, with the effective breakdown field of the dielectric films imposing the upper limit for applied voltage. The efficiency can then be rewritten as,

$$L = 4 \eta f dz E_t (Q_i - Q_z).$$

2-8

In an actual device with complete drive electronics, the power consumption is dominated by the charging of the device capacitance through circuit resistance.

The luminance voltage characteristics can be seen to have three distinct regions, figure 2-11. Below threshold little or no light is emitted. Above threshold there is a steep increase in luminance with voltage. Finally, a region exists in which the Mn excitation centers are saturated.

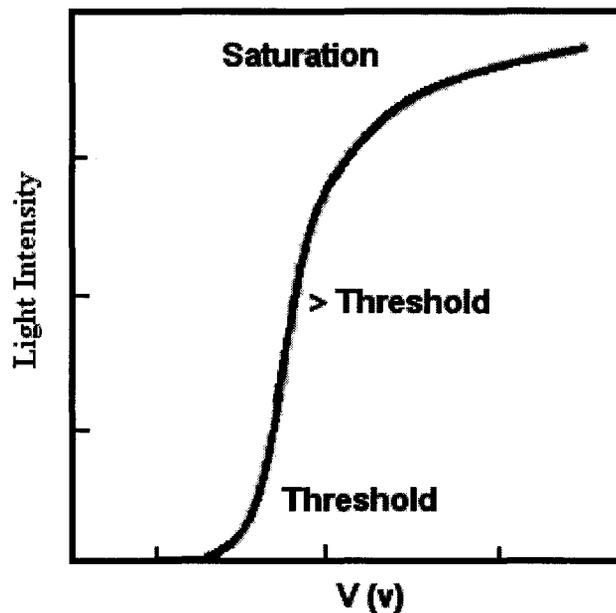


Figure 2-11 TFEL LV Characteristics

The aforementioned interface states are due to the termination of the ZnS lattice at the dielectric interface as well as non-stoichiometry and dangling bonds. The states are also

affected by the fact that the ZnS is typically polycrystalline. The dominance of interface states in device operation is supported by several observations. There is a dependence of the threshold field on the type of insulator as well as asymmetry due to the differences in the two insulator surfaces. Figure 2-12⁴¹ illustrates the variation of interface states with various oxides. From the graph, BaTiO₃ has a high density of deep states and few shallow states. In actual devices, this translates into high efficiencies. Al₂O₃ has similar characteristics with a lower density of states. Y₂O₃ has a broad interface state spectrum with many shallow states. This can translate into poor efficiency and poor ageing characteristics. Si₃N₄ has been shown to suffer from severe degradation. SiON characteristics are dependent on the exact composition.

The electrical characteristics are insensitive to temperature and there is a steep dependence of current on field. Furthermore, the phosphor current can be found by the Fowler-Nordheim tunneling current, $I_t = qncP(E)A$, where q is the electron charge, n_c is the interface state density, A is the area of the device, and $P(E)$ is the tunneling probability from an interface state of energy E_c , given by

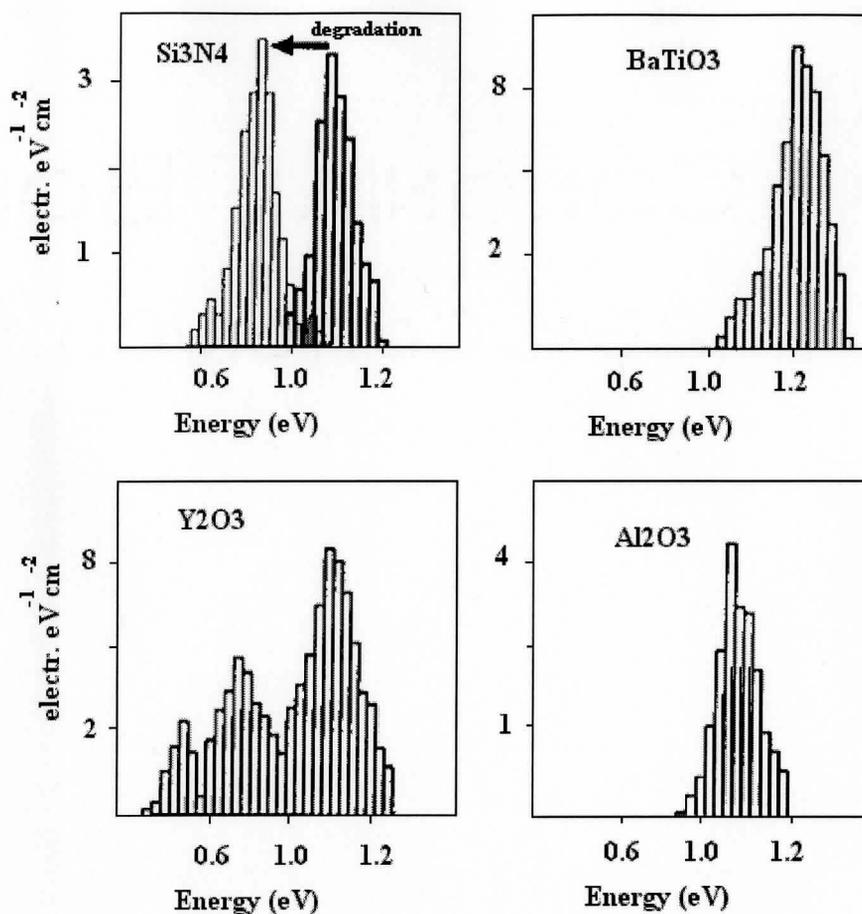
$$P(E) = 3.4 \times 10^{-12} (\text{m/m}^*)^{1/8} E_c^{5/8} E^{1/4} \times \exp(-7 \times 10^7 (\text{m}^*/\text{m})^{1/2} E_c^{3/2}) / E,$$

2-9

where E is the electric field.

The dielectric properties of the insulators are crucial. The dielectric constant and the

breakdown field are critical as the films must withstand large applied voltages and high fields. For high device efficiency, a large dielectric capacitance is preferable (as opposed to the capacitance of the phosphor below threshold). The films must also have a low defect density to avoid catastrophic failure. Silicon oxynitride has been a promising material as the dielectric constant can be varied between 4 and 8 and the breakdown field strength is in the mega volt per cm regime. However, defects generated during deposition using methods such as sputtering and physical vapour deposition (PVD), have limited the usefulness of this material.

Figure 2-12. Variation in ZnS/Oxide Interface States⁴¹.

2.4 Nickel Induced Crystallization

Crystallized amorphous silicon films are known to have better electrical properties than as deposited (high temperature) poly silicon and significantly better than amorphous silicon films. Lowering the crystallization temperature is crucial and can be achieved through metal induced crystallization⁸⁷⁻⁹². Additional references can also be found⁹³⁻¹²⁴. Here, a thin metal layer is deposited on top of an amorphous silicon layer and through diffusion several

reactions occur at the interface. Free electrons from the metal interact with the silicon covalent bonds producing a metal silicide (palladium, titanium, nickel) or eutectic alloy (aluminum, gold, indium, silver, gallium, zinc, tin) . The metal then migrates through the silicide, acting as a catalyst by providing nucleation sites.

Among the various metals used for crystallization, nickel appears to produce films that have larger grains (up to 100 μm), less intergrain defects and smaller boundary size as compared to films produced by other metals. This is possibly due to the lower solubility of nickel in silicon. For example, with palladium, the grains are smaller due to the higher solubility of Pd in silicon, which is orders of magnitude higher than Ni. In addition, when using nickel, the crystals will form into the (111) plane, which has the lowest free energy. Also, the lattice mismatch between Si (111) and NiSi_2 (111) is only 0.4% and nNickel silicides have been found to form at low temperatures (200° C-400° C).

Crystallization progresses through a silicide front. Nickel silicide absorbs silicon atoms from the a-Si region and releases silicon atoms into the crystalline region, figure 2-13.

The chemical potential of Ni is lower at the amorphous silicon / nickel silicide boundary and the potential of silicon is lower at the silicide/crystalline silicon boundary, driving the process by the reduction of free energy. Nickel will then move towards the amorphous silicon and the forward moving Ni forms new silicides. The silicide crystals that form reduce the activation energy for crystallization. When the process begins it is limited by the diffusion of Nickel through the silicide region. As the silicide thins, the reaction is limited by the surface reaction

between Ni and amorphous silicon.

During the process, there are isolated crystallization sites resulting from the discontinuous nature of the ultrathin metal layer and the grain size is determined by the nickel density as the grains will grow until they meet another grain boundary. There is a critical size of a silicide site that will induce crystallization, on the order of 10^7 atoms. However, the critical size of NiSi_2 seed sites decreases with temperature, causing an increase in the number of nuclei at higher temperatures. This in turn decreases the average grain size.

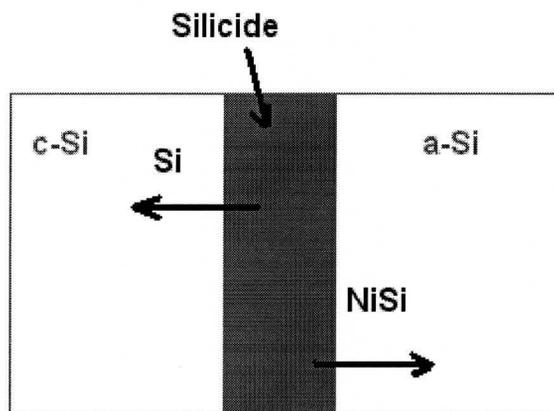


Figure 2-13 Process of Nickel Induced Crystallization of Silicon

The application of an electric field has been shown to increase the growth rate. Boron doping also speeds up the process possibly due to the lowering of silicide formation energy and a faster nickel diffusion rate in the presence of Boron.

There is a problem of contamination as the metals will act as deep level dopants and

as recombination centers. However, increases of three orders of magnitude in conductivity will be induced as long as there are low impurity levels. In actual devices the total impurity levels may be less than that achieved with a high temperature crystallization process as the low temperature of anneal draws less impurities from the surrounding metals (Al, Mo) . Furthermore, the nickel impurities tend to be trapped at the grain boundaries, which can be avoided in properly designed devices.

Metal induced lateral crystallization (MILC) is used to reduce the concentration of nickel metal impurities. In this process, the amorphous silicon has a thin film mask with windows etched to reveal selected portions. The nickel then comes into contact with the silicon only through the windows. The crystallization proceeds in two ways, through the standard process and through lateral migration of the nickel and silicides beneath the windows, through the underlying silicon films. This is the preferred method used to form active devices, including thin film transistors (TFTs).

2.5 Thin Film Transistors

Pixelated flat panel displays can display information through addressing. Addressing can be achieved through two general methods. Passive matrix displays will raster through the rows, while lighting up the desired columns. Active matrix addressing allows for the individual accessing of each pixel. Thin film transistors¹²⁵⁻¹³⁰ are used to turn each pixel on. Additional references can also be found¹³¹⁻¹⁵⁸. As each row is selected, any pixel in that row can be turned off or refreshed through the transistor. Depending on the quality of the matrix,

two or more TFTs can be used for each pixel. Due to the large surface area of an information display, amorphous hydrogenated silicon, a-Si:H, or polycrystalline silicon is typically used, as opposed to crystalline silicon. This is due to the fact that the processing of this material lends itself to large area deposition. Polycrystalline silicon has a higher mobility and is preferred for devices that require higher currents such as active matrix OLEDs. These transistors are metal oxide semiconductor field effect transistors, MOSFETs. A typical device is shown in figure 2-14. The planar TFT structure shown consists of a semiconductor material (silicon), of one dopant type (p or n), with source and drain contacts formed by the opposing dopant type (n or p type). This semiconductor material will typically be crystalline, poly crystalline or amorphous silicon. The gate dielectric is then formed, followed by the gate, source and drain contacts.

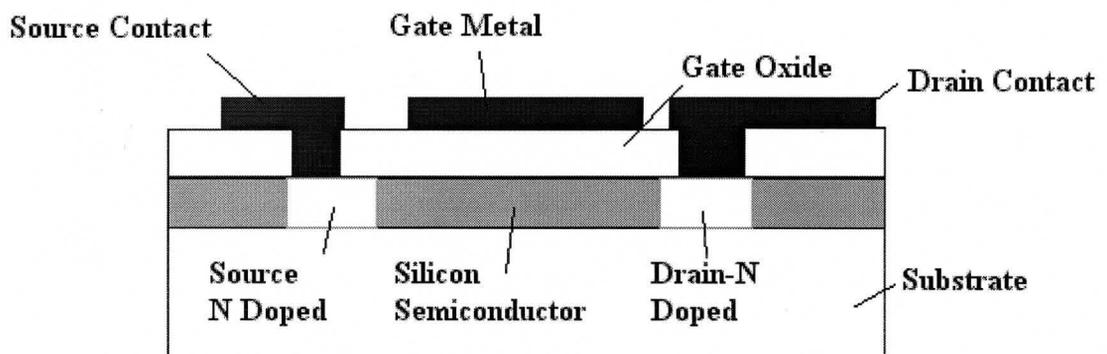
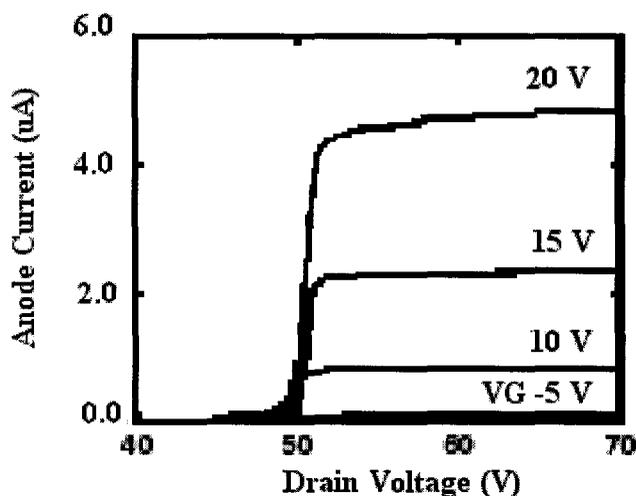


Figure 2-14 Planar TFT

The device operates as a MIS capacitor, acting as the gate, between two pn junctions, the source and drain. In this case, the silicon is p-type, an n-channel device, with n⁺ doped

source and drain contacts. Electrons enter through the source and pass to the drain with the gate acting as control. The gate voltage, V_g , and drain voltage, V_d , are relative to ground and the source and back contact are at ground. This acts to reverse bias the drain pn junction. The device requires an inverting gate bias to draw electrons into the conducting channel between the source and drain. Assuming the gate voltage is above threshold and that the drain voltage is at low positive voltages, a few tenths of volts, the drain current, I_d , is linear with V_d and conduction is ohmic. With higher drain voltages, the voltage drop from source to drain reduces the inverting effect of the gate. Minority carriers are depleted from the area around the drain, causing a decrease in the slope of the I_d - V_d curve. Pinch-off occurs when the carrier concentration around the drain becomes equal to the bulk concentration, and the slope of the I_d - V_d curve goes to zero. As the gate voltage is increased we obtain a family of curves as shown in figure 2-15.

Figure 2-15 TFT I_{ds} Characteristics

For a p-type device the threshold voltage can be expressed as¹,

$$V_T = \phi_s + K_s x_o / K_o ((2qN_A / K_s \epsilon_o) \phi_s)^{1/2} , \quad 2-10$$

where ϕ_s is the semiconductor surface potential, K_s is the semiconductor dielectric constant, x_o is the dielectric thickness, K_o is the oxide dielectric constant and N_A is the acceptor concentration.

The effective mobility of real devices is determined by the fact that there is a gate induced electric field that accelerates carriers towards the surface. However, the carriers have a reduced mobility due to scattering effects at the surface. The effective mobility, μ_n , can be expressed as¹;

$$\mu_n = \mu_o / (1 + \theta(V_g - V_t)) , \quad 2-11$$

where μ_o is the bulk mobility, θ is a constant, V_t is the threshold voltage and V_g is the applied voltage.

MOSFET I_d characteristics can be approximated in a number of ways. With the square law theory¹,

$$I_d = Z \mu_n C_o / L [(V_G - V_T)V_D - V_D^2 / 2] , \quad 2-12$$

saturating at $V_{dsat} = V_g - V_t$. Z is the channel length, C_o is the oxide capacitance and L is the channel width.

However, this formulation neglects the widening of the depletion width of the conducting channel as we move from the source to drain. An alternate representation can be found in the bulk charge theory, with¹,

$$I_d = Z\mu_n C_o/L [(V_G - V_T)V_D - V_D^2/2 - 2/3 V_w \phi_s \{(1 + V_D/\phi_s)^{3/2} - (1 + 3V_D/2\phi_s)\}],$$

2-13

with¹

$$V_{dsat} = V_G - V_T - V_w \{ [V_G - V_T/\phi_s + (1 + V_w/2\phi_s)^2]^{1/2} - (1 + V_w/2\phi_s) \}$$

2-14

Where $V_w = qN_A W_T / C_o$.

Even with this modification there are still limitations to the theory. In actual devices there is a residual drain current resulting from a non-zero channel charge below threshold. Problems can also arise with the gate dielectric as leakage currents reduce the efficiency of the transistors. In addition, interface states at the insulator/semiconductor surface will create charge accumulation and lead to surface conduction. Hence, a low interface state density is desirable.

2.6 Silicon Oxynitride Film Properties

Silicon oxynitride film properties are best examined by looking at the binary

constituents, namely the properties of silicon dioxide and silicon nitride. Even though the properties of both materials are often dependent on the deposition type, process, and parameters, some general properties can be observed¹⁵⁹⁻¹⁶⁶. The refractive index of SiO₂ is typically around 1.46 to 1.48 (@ 550 nm although there is little variation across the visible spectrum, 450 nm to 650 nm) and will shift slightly with density and impurity concentrations. The internal stress of SiO₂ films is low, $\sim 10^9$ dynes/cm², compressive, and is mostly independent of the deposition conditions. The low frequency (DC) dielectric constant is on the order of 4, with breakdown fields greater than 200 MV/cm. The density of SiO₂ ranges from 2.20 to 2.70 g/cm³, depending on the deposition conditions.

The refractive index of silicon nitride, Si₃N₄, lies between 2.0 and 2.1 (@ 550 nm) depending on process parameters. The internal stress is highly dependent on deposition conditions but will typically be on the order of 10^9 dynes/cm², compressive. By varying the deposition conditions, the stress can be changed from compressive to tensile. The low frequency (DC) dielectric constant is around 8 and the breakdown field is on the order of 200 MV/cm. The density of Si₃N₄ ranges from 2.1 to 3.1 g/cm³, depending on the deposition conditions.

Silicon oxynitride properties can be scaled between those of silicon dioxide and silicon nitride. The films are typically single phase, with no distinct silicon dioxide and silicon nitride phases. This scalability is a key factor in the usefulness of silicon oxynitride, as the optical and electrical properties of the films can be modified for specific applications.

The refractive index can range from 1.46 to 2.1 and the DC dielectric constant can range from 4 to 8.

2.7 Deposition of Silicon Oxynitride Thin Films

2.7.1 ECR PECVD of Silicon Oxynitride Thin Films

The ECR plasma utilizes the cyclotron motion of a charged particle in a magnetic field. The frequency of this motion, ω_C , is given by $\omega_C = eB/m$, where B is the magnetic field strength and m is the ion mass. If electrons in such a field are subject to an oscillating electric field at the resonant frequency, ω_C , they will gain energy. Through collisions, these electrons will induce ionization. The collisions may cause excitation of electronic, vibrational and rotational modes of the gas, or ionization and dissociation of gas molecules. Different gases will ionize differently, with diatomic gases, such as N₂ and O₂, having more paths of energy dissipation. Diatomic molecules can undergo excitation of rotational, vibrational, dissociation, electronic and ionization of the molecule. Typically these diatomic plasmas are less uniform and stable than Argon plasmas, and, they can allow the microwaves to propagate through the plasma.

The energy of the plasma is a key parameter and can be described by the velocity of particles in the plasma. This velocity can be defined as a Maxwellian distribution. With three degrees of freedom, the energy of the plasma at a given temperature is $E_{av} = 3/2k_bT$ and the electron temperatures are typically less than 10 eV.

In the plasma there is a magnetic field gradient, dB/dz . This varying magnetic field interacts with the magnetic moment, μ , of the electrons (they rotate around the magnetic field lines). In turn, this generates an electric field, E , from the plasma source to the substrate. Satisfying the neutrality condition, the accelerations of the ions and the electrons are equal, with

$$\mathbf{F}_i/M = \mathbf{F}_e/m, \quad 2-15$$

with F_i , F_e and M and m , the force on the ions and electrons and the mass of the ions and electrons, respectively.

We can also see that the forces are expressed as,

$$\mathbf{F}_i = e\mathbf{E} \text{ and } \mathbf{F}_e = -\mu d\mathbf{B}/dz - e\mathbf{E} \quad 2-16$$

The magnetic moment is determined by the kinetic energy of the electron, as it rotates around the magnetic field and the strength of that field, $\mu = W/B$.

The electric field in the system can then be derived as,

$$\mathbf{E} = (W_0 / e B_0) / (-dB/dz) / (1 + M/m) \quad 2-17$$

Full integration yields an ion potential given by,

$$\Phi = -(W_0 / e) (1 - B/B_0) \quad 2-18$$

The gas pressure controls the mean free path of the electrons and hence the average electron energy. With this, and control of the microwave power, the ion energy can range between 5 to 30 eV.

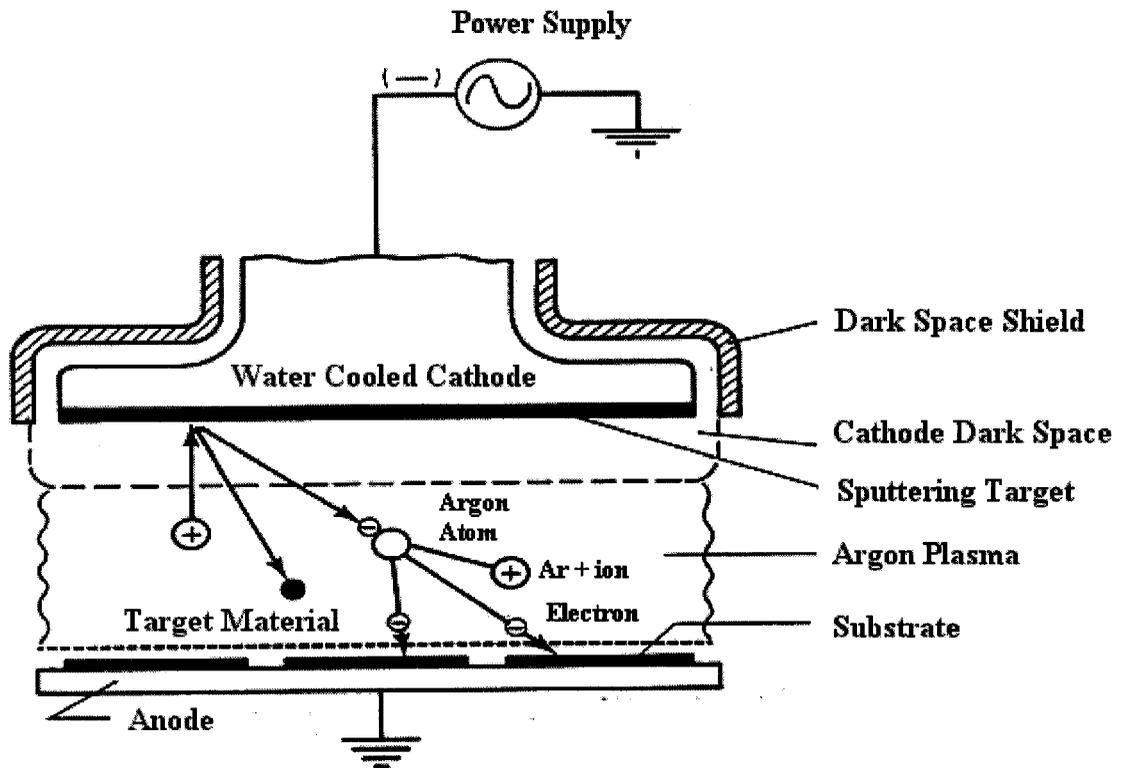
The CVD process of silicon oxynitride has been rigorously studied¹⁵⁹⁻¹⁶⁵. Additional references are available¹⁶⁶⁻²¹⁹. The ion bombardment of SiH₄, by the plasma, will promote the release of hydrogen, with the binding energy of SiH₃-H being about 3.9 eV and the average plasma ion energy being between 5 and 30 eV. This ion bombardment will also reduce the probability of hydrogen rebonding. SiH₃ is adsorbed at the surface, through Van der Waals forces and has a high surface mobility. This allows it to move along the surface to active sites, i.e. sites with open Si, N, or O bonds. A higher surface temperature will reduce the sticking coefficient, particularly to weaker bonds, and improve film quality. In contrast, SiH₂ can insert at any site, causing roughness and pinholes. An ion energy below that required to ionize Si-O, Si-N or N-O bonds is desirable, as once formed, the probability of dissociation will be low. The hydrogen must also be removed from the surface to further reduce its incorporation into the films either substitutionally or interstitially. For silicon dioxide the reaction equation is,



This requires a SiH₄:O₂ ratio of at most 0.66 to provide good quality films. In practice, films require a ratio of less than 0.1 to remove sufficient hydrogen to prevent poor film quality, particularly when depositing at room temperature. Use of a nitrogen-based plasma, as opposed to argon, can dramatically increase the ratio of reactive gas to silane, while still maintaining gas pressures that will allow for a sustained plasma.

2.7.2 Sputtering

Sputtering is a well established thin film deposition process in which a voltage is applied between a target cathode and a substrate, figure 2-16²²⁰. An inert gas, such as argon, is introduced into a high vacuum chamber. The steady state ionization of the gas is enhanced by collisions induced by the accelerating voltage. The ions are then accelerated towards the cathode, sputtering off material (atoms or molecules), through collisions. These particles have significant kinetic energy and are then deposited on a substrate. Reactive gases, such as oxygen and nitrogen, may be added to produce compound films. A primary concern with sputtering is the formation of macroscopic defects. Arcing can occur when depositing dielectric films, as an insulation layer forms over the metallic cathode material. Charge builds in this area until there is breakdown or arcing across the dielectric layer. This material can then sputter unto the substrate. Also, due to the physics of sputtering, the film density cannot be enhanced, except through lowering the deposition rate.

Figure 2-16 Sputtering Process²²⁰.

2.7.3 Ion Assisted Physical Vapour Deposition

In ion assisted deposition, a cathode is heated to thermionic emission temperatures to produce electrons. These electrons are accelerated towards an anode, striking neutral gas molecules or atoms in the path. Electrons moving away from the anode interact with an imposed magnetic field, producing an electric field that accelerates the ions. The ion energy is a function of the potential difference between the anode and cathode and the ion density is a function of the anode voltage and the gas pressure. These accelerated ions are combined with a physical vapour deposition method (thermal, electron beam evaporation) and serve to

densify the deposited films through a ballistic process, figure 2-17²²¹.

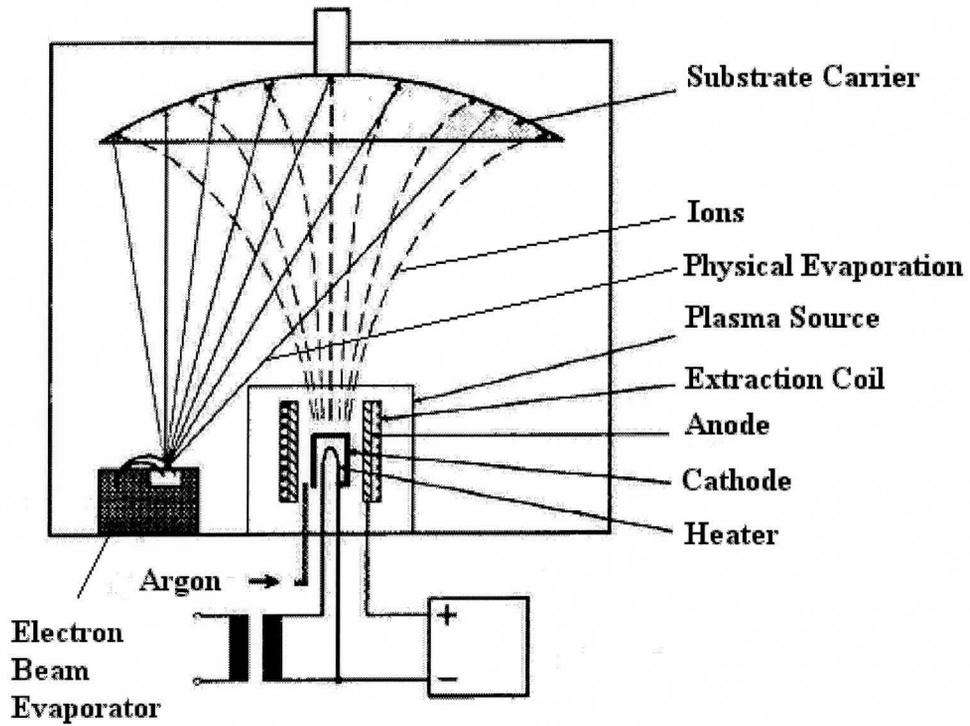


Figure 2-17 Ion Assisted Electron Beam deposition²²¹.

3 EXPERIMENTAL PROCEDURE

Three different methods of deposition were used to manufacture several types of devices based on silicon thin films; sputtering, ion assisted physical vapour deposition (IA-PVD), and ECR-PECVD. SiON thin films for metal insulator metal (MIM) devices were made on all three systems with the sputtered and IA PVD devices acting as benchmarks, against which the quality of the ECR devices can be assessed. The SiON dielectrics for TFEL displays were also manufactured on all three systems.

The ECR PECVD system was used to produce SiON films for the production of metal insulator semiconductor (MIS) structures. In addition, amorphous silicon films were produced on the ECR system for incorporation into TFTs.

3.1 *Sputter system*

A Materials Research Corporation in-line sputtering system, series 900, consisting of a high vacuum chamber, capable of reaching predeposition pressures in the low 10^{-6} Torr regime was used. The system also has a magnetron cathode with a silicon target and a pulsed ENI DC power supply. This process was optimized by varying the gas flow rates including the ratio of reactive to argon gas, chamber pressure and power conditions.

3.2 *IA-PVD System*

A Leybold Advanced Plasma System (APS) 1104 high vacuum thin film evaporation

system consisting of an 1104 litre chamber, with predeposition pressures in the low 10^{-6} Torr regime, was used. Films were deposited using a thermal evaporation source in conjunction with the plasma source, figure 2-17, on pg. 2-34. Optimum plasma conditions were established by varying the argon flow rates through the source, the reactive gas added through a ring above the plasma source as well as the anode voltage. This optimization focused on high breakdown voltages, good uniformity, and low stress.

3.3 ECR-PECVD System

The ECR system consists of a load locked high vacuum chamber, capable of reaching pre-deposition pressures in the 10^{-8} Torr range. The process was optimized for SiON deposition by varying the gas flow rates, microwave power and the shape of the magnetic confinement envelope. The gases utilized were nitrogen and oxygen, both pure and mixed with an argon dilutant. The sole silicon precursor was 30% Silane in argon. No heating was used during the deposition and measured heating of the substrate from the plasma remained below 60° C.

3.4 Devices

Several devices were fabricated to assess the quality of the films produced.

3.4.1 MIM Structures

Metal insulator metal (MIM) capacitors were produced in all three systems as a means of determining the breakdown characteristics and dielectric constants of the films. The

SiON films, 200 nm thick, were deposited on boron silicate glass coated with 200 nm of indium-tin-oxide (ITO) (from Colorado Coatings). Aluminum dots, 150 nm thick, were then deposited on these films, through a metal shadow mask. Although ITO is technically a semiconductor, it is so highly doped as to become degenerate. It is a film commonly used in display manufacturing due to its high transmission in the visible region and good electrical conductivity.

3.4.2 MIS Structures

Metal insulator semiconductor (MIS) structures were manufactured in order to investigate the interface states at the SiON-semiconductor interfaces and to assess the overall suitability of these SiON films for use in MOSFETs. Only films deposited using the ECR system are examined here. SiON films, 100 nm thick, were deposited on n-doped, 3 ohm-cm single crystal silicon. Aluminum contacts were evaporated onto the back of the devices and aluminum dots were evaporated onto the SiON through a shadow mask.

3.4.3 TFEL displays

Thin film electroluminescent (TFEL) displays were manufactured using dielectrics from all three systems using a format of patterned ITO, 180 nm thick and 300 μm wide, onto which 90 nm of SiON was deposited (through the range of refractive indices from 1.55 to 1.95). The structures were then transferred to the Leybold APS 1104 vacuum system. Prior to deposition, the samples were ion bombarded for 15 minutes to remove native oxides. This was followed by the deposition of 550 nm of ZnS, doped with Mn (0.5%). This was capped

with a second SiON layer of 160 nm. Aluminum, 160 nm thick by 0.5 cm wide was then vacuum deposited via electron beam evaporation, through a metal shadow mask in the Leybold APS 1104 system, to provide a back contact. These displays were then annealed in a nitrogen atmosphere at 500° C for 2 hours.

The ZnS and aluminum layers were deposited at the same time for all devices in order to ensure consistency. The annealing was also conducted simultaneously for all samples.

Electrical characterization of alternating current thin film electroluminescent (ACTFEL) devices is accomplished via Q-V or C-V characterization as shown in figure 3-1. An arbitrary waveform generator (Wavetek 275) was used in series with a high voltage amplifier (Apex PA-85) to provide the input signal. The drive consisted of a symmetric bipolar waveform with trapezoidal shape, 5 us rise and fall time, 30 us pulse width, frequency of 1 kHz. A 7.6 ohms sense resistor was used for CV characterization. The CV curve is given by the equation,

$$C (v_2-v_3) = i(t) / d[v_2(t) - v_3(t)]/dt \quad 3-1$$

The current, $i(t)$, is measured across the sense resistor, $i(t)=v_3(t)/R_c$.

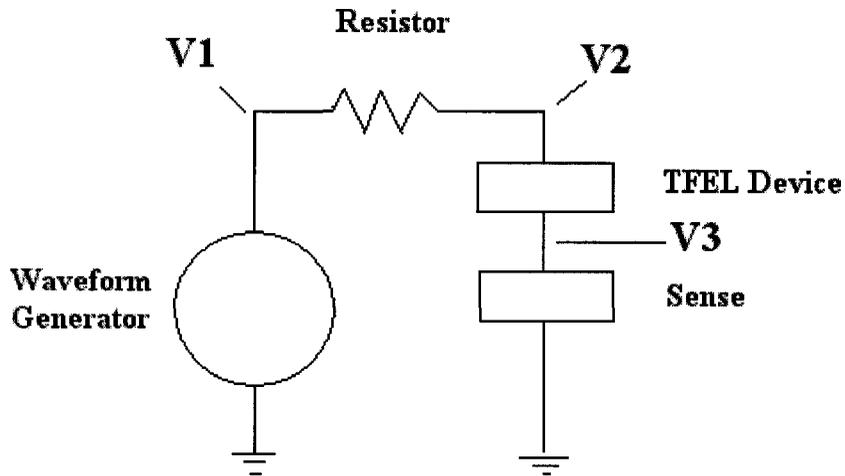


Figure 3-1 TFEL Electrical Characterization Set-up

A typical CV curve is shown in figure 3-2 with the insulator capacitance, C_i , and total capacitance, C_t . The slope of the CV curve can be used as a measure of the interface state density. A decrease in the slope indicates injection of electrons from shallow interface states.

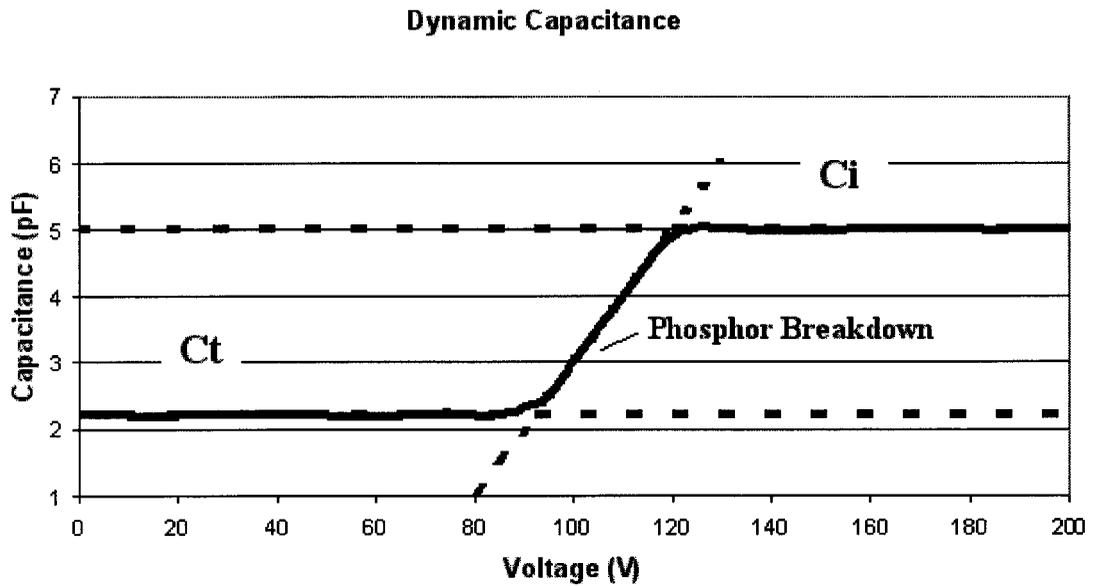


Figure 3-2 Dynamic Capacitance

The current through the device is given by,

$$i(t) = v_3(t)/R_2 \quad 3-2$$

and the charge is given by

$$q(t) = \int_{\tau=0}^{\tau} i(\tau) d\tau. \quad 3-3$$

The dynamic capacitance of the stack is given by,

$$C(v) = i(t)/(d[v_2(t) - v_3(t)]/dt) \quad 3-4$$

The charge stored at the interface is,

$$Q_{is} = C_i^2 C_t / (2qA C_p) [\Delta C / \Delta V]^{-1} \quad 3-5$$

Q-V analysis was conducted with the same waveform as above, using the circuit as shown in figure 3-1, with the sense resistor replaced with a sense capacitor, C_s , of 10 nF. $V_2(t)$ and $V_3(t)$ are measured, with $Q(t)$ the external phosphor charge, $Q(t) = C_s V_3(t)$, and the voltage across the TFEL device is, $V = V_2(t) - V_3(t)$. Also, $Q(t) = C_e V + Q_z C_i / (C_i + C_z)$, where C_e is the device capacitance, V the applied voltage, Q_z is the dipole moment of charges in the phosphor layer divided by the layer thickness. By taking the height of the QV loop at zero applied voltage, we can derive the charge transferred in the phosphor, $Q_z C_i / (C_i + C_z)$. A typical Q-V curve is shown in figure 2-10, pg 2-15.

3.4.4 Nickel Induced Crystallization

Thin films of amorphous silicon, 200 nm thick, were deposited in the ECR PECVD system at room temperature. The films were then transferred to a separate high vacuum system for deposition of thin nickel layers, 3 nm thick. Prior to nickel deposition, the samples were ion bombarded for 15 minutes to remove native oxides. The samples were then vacuum annealed at 950° C for 30 seconds.

3.4.5 MIS Structures Using Nickel Induced Crystallized Films

Silicon substrates coated with an oxide buffer layer were sputter deposited with 200 nm of ITO films to provide back contacts. This was followed by 100 nm of sputtered SiON

films. Next, 200 nm of amorphous silicon was deposited using the ECR PECVD system. The films were then transferred to the Leybold APS 1104 system and ion bombarded for 15 minutes to remove native oxides. Through a shadow mask, 200 nm thick strips of SiON, 50 μm wide, were deposited. This was carried out in order to define areas of metal induced crystallization (MIC) and metal induced lateral crystallization (MILC). Then 1 nm thick nickel layers were deposited using electron beam evaporation. The samples were then vacuum annealed at 950° C for 30 seconds. The films were subject to etching in HCL and then ion bombarded for 15 minutes to remove native oxides and residual nickel. Lastly, front aluminum metal contacts were deposited through a metal shadow mask.

For MIS structures incorporating Boron, the above procedure was followed exactly with the exception of a thin layer of Boron, 1 nm, electron beam evaporated, prior to the thin nickel layer.

3.4.6 TFTs Based on Metal Induced Polycrystalline Films

Thin film transistors were made, based on the polysilicon MOS capacitors produced. The process is outlined in figure 3-3. A silicon substrate was coated with a sputter deposited buffer layer of 200 nm of SiON. This was done to prevent the replication of the substrate crystallinity in the deposited silicon films.

Next, amorphous silicon layers, 200 nm thick, were deposited using the ECR PECVD system. The samples were then transferred to the Leybold APS 1104 system and ion

bombarded for 15 minutes to remove native oxides. Next, the samples were patterned through a shadow mask to produce the gate separation using a thin silicon oxynitride film, 25 μm wide and 100 nm thick. The metal shadow mask was removed and the films were then plasma cleaned and a 3 nm layer of nickel was deposited. The films were then vacuum annealed at 950° C for 30 seconds. This produced MILC films under the gate and MIC film at the source and drain contacts. The source and drain contacts (n type) were then formed in a high temperature furnace while being exposed to phosphorus. The oxide layers were then removed in a buffered HF etch. The gate dielectrics were then reformed by deposition of SiON layers ($n=1.9$, width 125 μm , thickness 100 nm) through a metal shadow mask. Through the same mask, an amorphous silicon layer was deposited for the gate contact. Lastly, aluminum source, drain and gate contacts were deposited through a metal shadow mask.

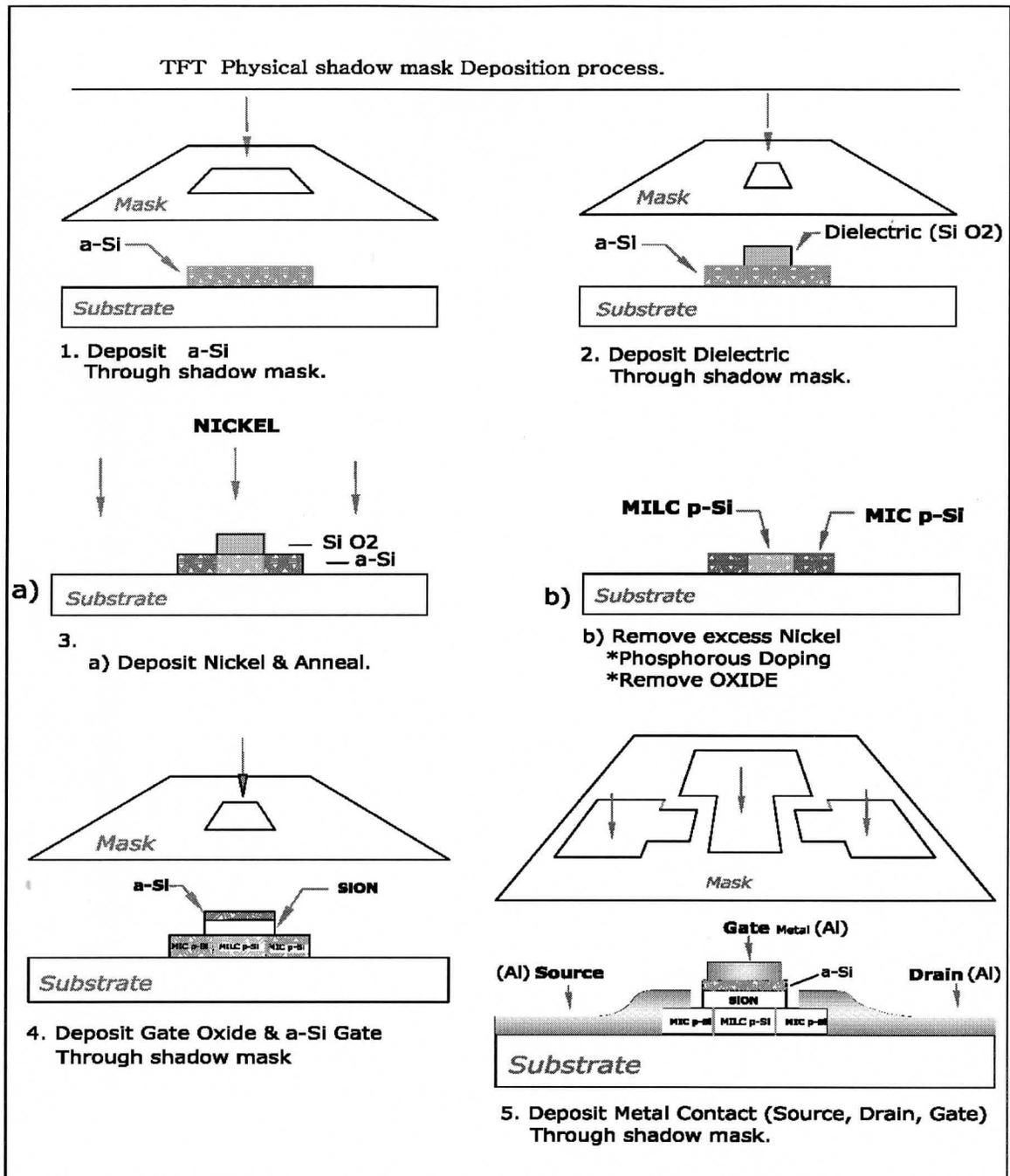


Figure 3-3 Flowchart of the Physical Shadow Mask TFT Process.

4 RESULTS AND DISCUSSION

4.1 Dielectrics

4.1.1 SiON films

Optimization of the ECR plasma conditions can be found in the prior art^{159,160}. When using a low substrate temperature (below 60° C) during ECR PECVD deposition, very poor film quality resulted, with the film quality being measured through the fabrication of simple metal-insulator-metal capacitors. From these devices, the dielectric constant, the dielectric breakdown field strength and the leakage current were found. For standard ECR films using argon plasmas, the devices were predominantly untestable. A few of these samples were made testable by applying high voltages to remove shorts. All of these samples had high leakage currents and low dielectric breakdown field strengths.

The low temperature method used to produce high quality films utilized high ratios of reactive gas (nitrogen) to silane. To achieve this, a nitrogen-based plasma was utilized (as opposed to argon) with very low silane partial pressures. Ionized nitrogen forms NH_3 , which is removed from the system before the atoms bond and reduces the hydrogen content in the deposited films. The drawback to using pure nitrogen as the base gas, as opposed to argon, comes from plasma instability due to the diatomic nitrogen molecule. This can cause plasma instability including fluctuations in the plasma temperature.

Under conditions of high reactive gas ratios, the maximum controllable film growth

rate was 0.15 nm/s. As the ECR plasma will only form in limited pressure regimes, the low growth rate is a consequence of a low silane partial pressure, which is necessary for a high reactive gas ratio.

The analysis of the SiON films consists of, etch rate determination, x-ray photoelectron spectroscopy (XPS), x-ray diffraction (XRD), nuclear reaction analysis (NRA), atomic force microscopy (AFM), and confocal microscopy.

4.1.1.1 Etch Rates

Etch rates (in 10% buffered oxide etch (BOE)) were measured for samples produced by four deposition methods; 1. sputtering (a known baseline), 2. low temperature ECR PECVD using argon based plasmas, 3. low temperature ECR PECVD using nitrogen (reactive) based plasmas, and, 4. ion assisted electron beam evaporation. All films were deposited at a rate of 0.15 nm/s.

In the analysis, the film refractive indices were measured, at 550 nm using ellipsometry. These measurements were done on silicon substrates with the deposited SiON films. The dielectric constants were determined from MIM structures consisting of a glass substrate, sputtered ITO electrode, deposited SiON film and aluminum top contact. The DC dielectric constants were determined through simple DC capacitance measurements. The SiON films were simultaneously evaporated on the two sample types.

The results show the expected drop in etch rates for films with higher refractive

indices, (higher nitrogen content), for all four deposition processes. This is a simple result of the diminishing effect of the BOE on the films as the Si-O bond density decreases. Normalized etch rates for SiON films deposited on silicon wafers are shown in figure 4-1. The refractive indices are related to the nitrogen and oxygen content of the SiON. The film density and other bonds (such as dangling and Si-H bonds) can also alter the refractive index. The etch rates are significantly lower for the ion assisted, sputtered and nitrogen CVD films, for all refractive indices, as compared to the argon CVD films. The most probable causes of the vertical shifts in etch rates are a low film density and weak bonds in the argon CVD films. When a higher substrate temperature is used (250° C or above) during argon based CVD this shift does not occur. In this case, it is probable that lower energy bonds do not form as often or are broken as a result of the higher thermal energy. Dangling bonds are one example of a bond type that is less likely to form. This will result in an overall stronger bond.

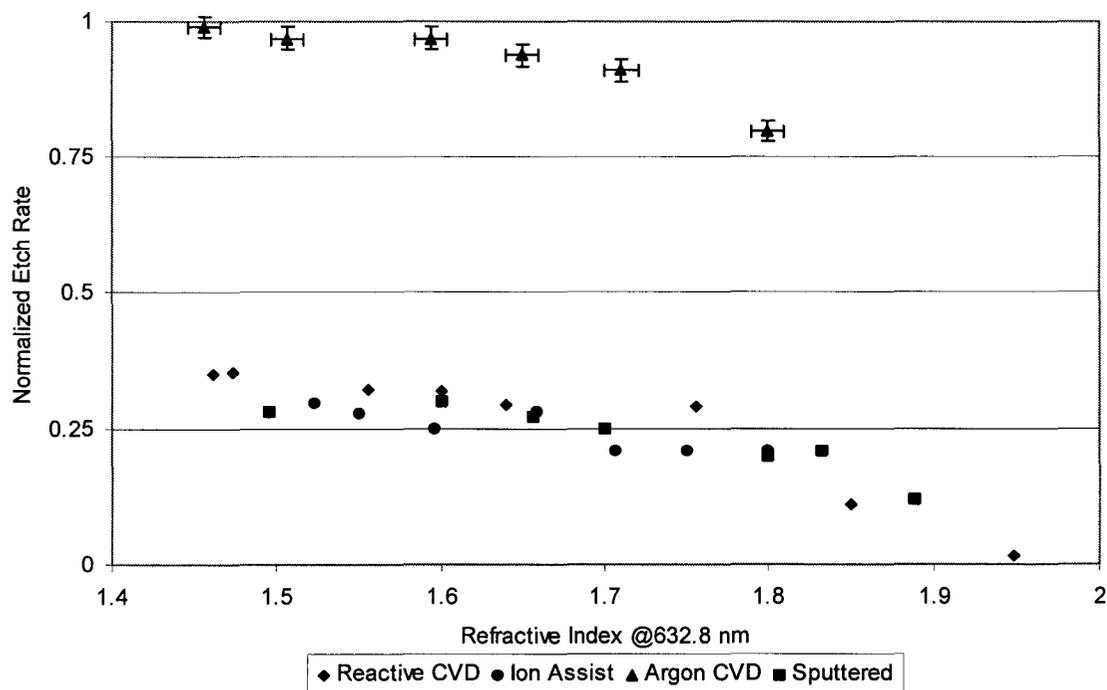


Figure 4-1 Normalized Etch Rates

4.1.1.2 XPS

X-ray photoelectron spectroscopy²²⁴⁻²³⁶ was performed on SiON films deposited on silicon substrates, by the ion assist, and the two CVD methods (argon and nitrogen plasmas). All the XPS measurements shown were made after ion milling 20 nm of surface material. Again, the refractive indices were determined using ellipsometry. From figure 4-2 we see that there is a decrease in the Si2p binding energy for higher dielectric constants. The Si2p XPS peak is a convolution of signals from several bonds such as Si-O and Si-N. The decrease in average binding energy is related to the decrease in the concentration of Si-O bonds. The Si-

N bond results in a weaker affinity of the Si2p electron to the silicon atom. A shift in the concentration of these bonds results in a shift in binding energy. From the figure, one can also see a vertical shift in the binding energy for the three different deposition methods across the refractive index range. Comparing the argon CVD deposited films to either the ion assisted or nitrogen CVD methods, at any given refractive index, the Si2p binding energy is higher for the argon CVD films. This suggests that the overall structure in these films involves statistically weaker interatomic bonding as would result from a higher density of dangling bonds. An increase in Si-OH bonds in the argon CVD films would qualitatively result in such a binding energy shift for a given index.

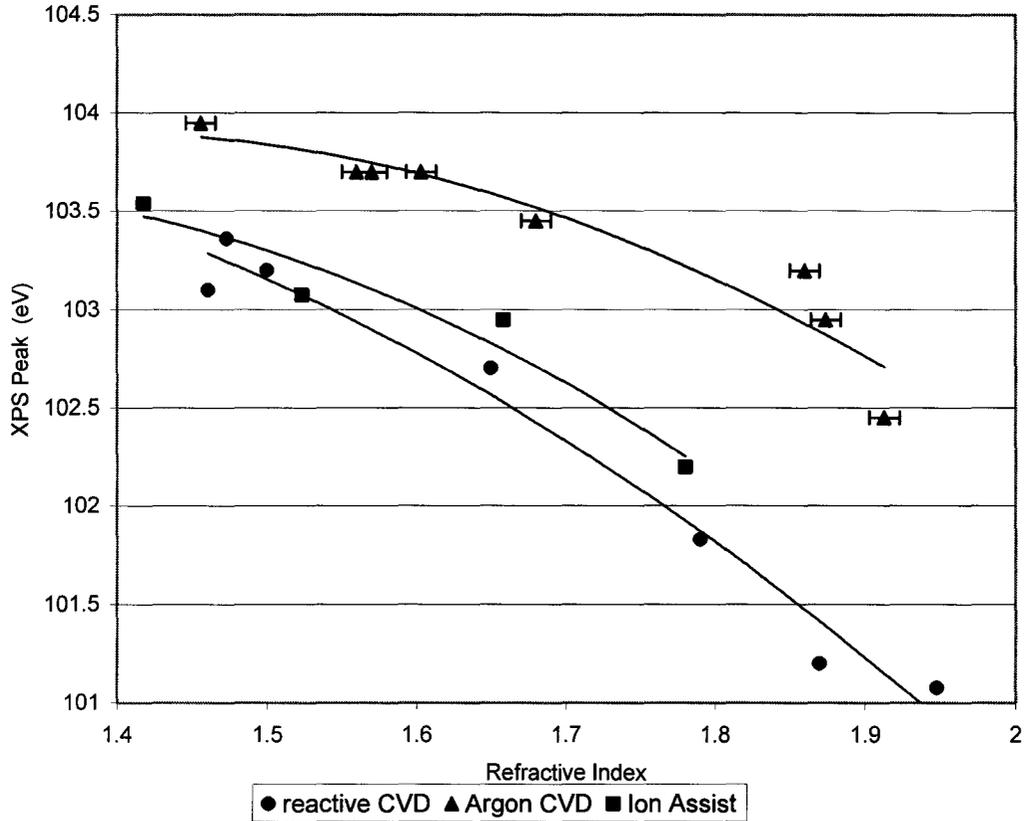


Figure 4-2 XPS Si2p peak as a Function of Refractive index

Examining figures 4-3, and 4-4 we can observe the de-convolution of the Si2p XPS spectra for the argon and nitrogen CVD methods. In each of these graphs the measured data is given along with the de-convolution of the data, which reveals the relative concentration of given silicon bonds. The concentration of each bond type is given by the area under each curve.

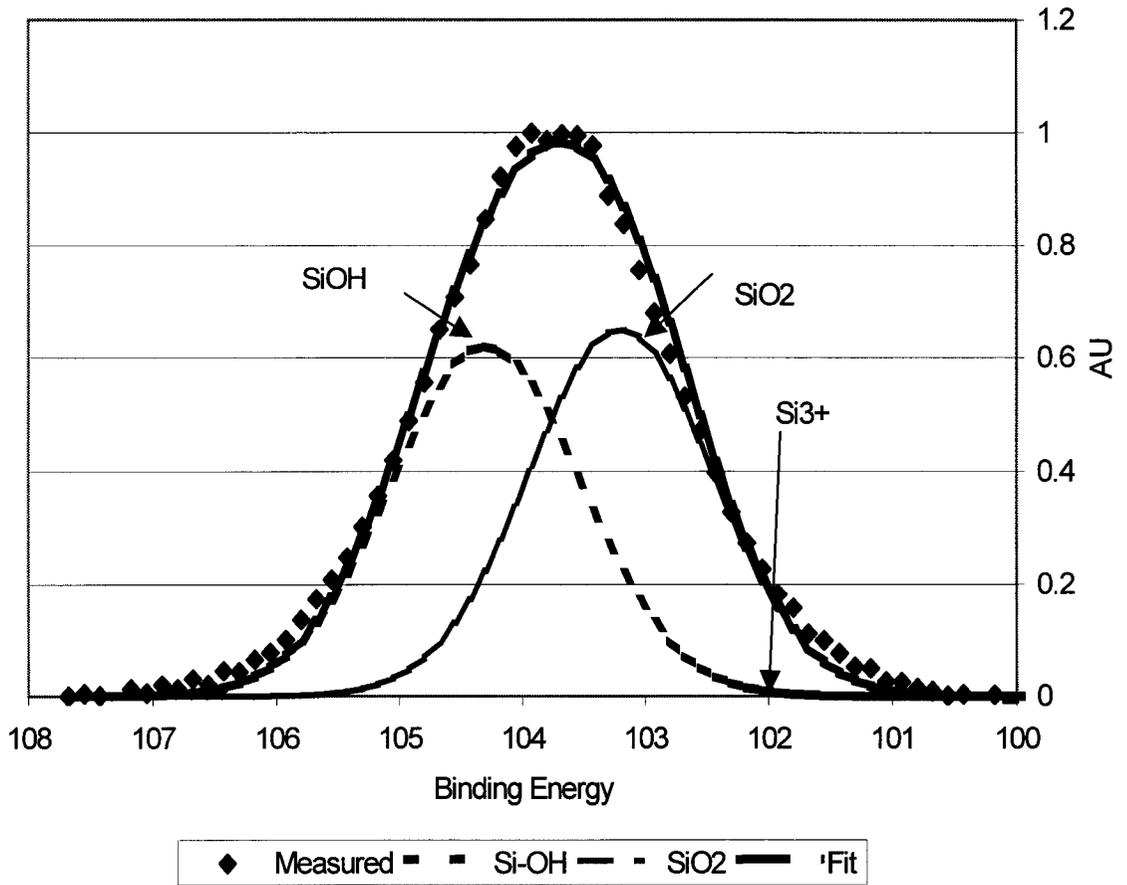


Figure 4-3 Argon CVD Si_{2p} XPS peak

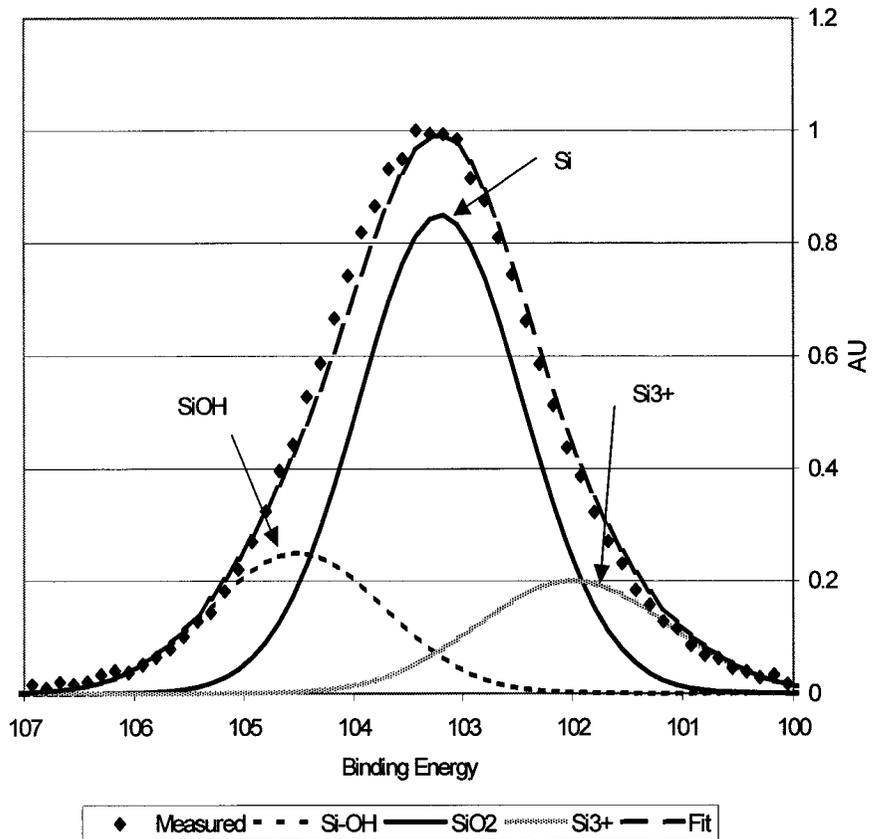


Figure 4-4 Reactive Gas CVD Si_{2p} XPS Peak

Figure 4-3 illustrates the Si_{2p} peak for a single argon CVD film, at a refractive index of 1.46, and indicates a significant concentration of Si-OH bonds, and no significant evidence of unsaturated bonds, Si³⁺. The relative concentrations of each type of silicon bond in the argon CVD method are 52.3% SiO₂ and 47.7% Si-OH as determined by the deconvolution of the peak. In comparison, figure 4-4 shows the XPS spectra for a single nitrogen CVD film, at a refractive index of 1.47. Here one finds a significant decrease in Si-

OH bonds and an increase in the concentration of unsaturated bonds, Si^{3+} . The relative concentrations of each type of silicon bond in the nitrogen CVD method are 67.4% SiO_2 , 18.3% SiOH , and, 14.3% Si^{3+} as determined by the deconvolution of the peak. This suggests that hydrogen plays a role in the formation of Si-O bonds, possibly due to the presence of OH^- , which forms due to the low oxygen to (hydrogen + silicon) ratio. These OH species may stay resident at the growth surface longer than O atoms. In the reactive CVD method the H is taken up as NH_3 and the OH species is less likely to form. This would result in a higher rate of formation of Si^{3+} bonds in the reactive CVD method as a by-product of the reduction of hydrogen in the films.

As the XPS measurements shown in figures 4-3 and 4-4 were made after ion milling 20 nm of surface material, they are then only representative of a specific depth in the films. Assuming that the film composition is uniform, this is a valid approach. From these results it could be concluded that the nitrogen based films would be of inferior quality as compared to the argon based films due to the higher concentration of dangling, Si^{3+} , bonds, 14.3% in the nitrogen films and undetected in the argon films. The silicon dangling bonds would create a conduction path through these films. In contrast, the higher concentration of these bonds in the argon plasma films (50% as opposed to 18.3 % in the nitrogen plasma films) suggests that the argon based films would be inferior to the nitrogen plasma films. These results are contradictory to each other and to the results given by the etch rate measurements.

Figure 4-5 illustrates the XPS profile taken after ion milling through 90 nm of the

film material of the argon plasma film. The results show a significant shift in the binding energy of the Si2p peak (102.8 compared to 103.7 for the profile at 20 nm depth). The deconvolution of the curve also indicates that there is a significant increase in the concentration of Si³⁺ bonds (63% concentration as opposed to undetected in the measurements at 20 nm film depth). There is also a decrease in SiOH bond concentration (<4% concentration as opposed to 47.7% in the measurements taken at a 20 nm film depth). The presence of a high concentration of Si³⁺ is very likely the cause of the faster etch rates. These results indicate that there is a significant change in film constituency for the argon based CVD plasma method. This will be discussed in the following section.

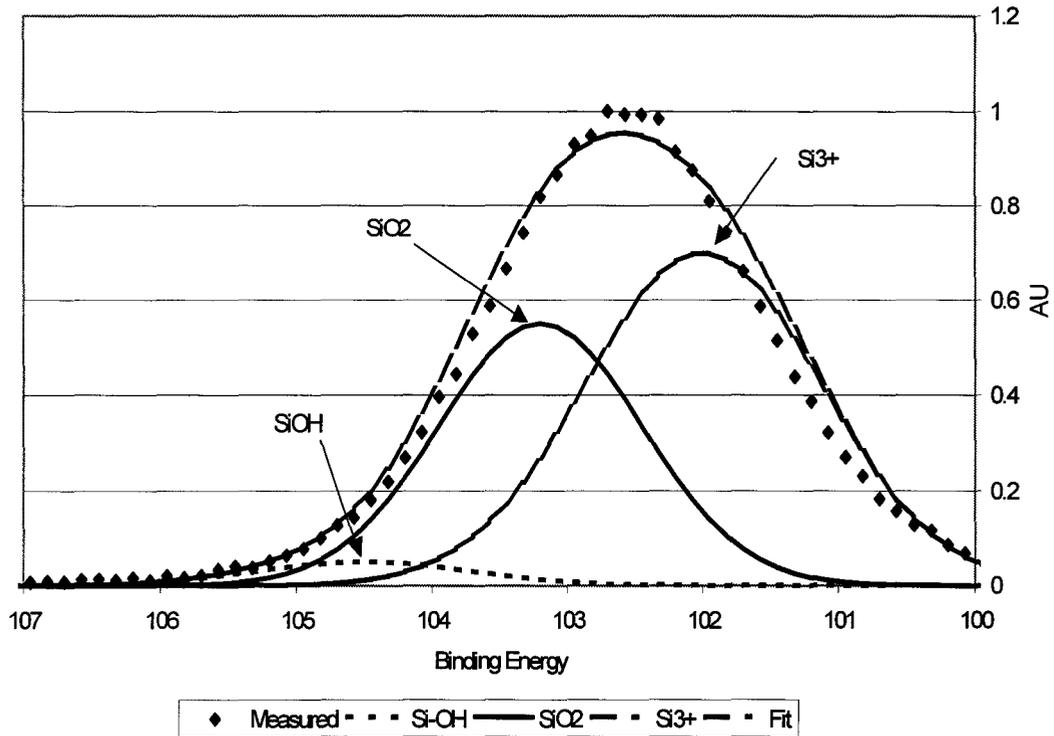


Figure 4-5 Argon CVD Si₂p XPS peak, Ion Milled to 90 nm

4.1.1.3 ERD

Elastic recoil detection (ERD) measurements suggest that the densities of films produced by reactive CVD, figure 4-6 are slightly greater than of films produced with argon CVD, figure 4-7. The obtained values are; reactive CVD $2.23 \text{ g/cm}^3 \pm 0.04$, Argon CVD $2.14 \text{ g/cm}^3 \pm 0.04$. These density values are averages through the films and are converted from the measured readings of atoms/ cm^2 . However, when sources of error are considered, the significance is borderline valid. The hydrogen content is shown to decrease as the depth increases but is seen to be roughly equal for the two film types. Overall, the ERD analysis

suggests that film density and simple hydrogen concentration are likely not dominant factors in determining film quality in this case.

However, the argon films are not stoichiometric throughout and the relative concentrations of silicon and oxygen change as a function of film depth. Near the substrate surface, the concentration ratio is suggestive of many dangling silicon bonds (Si^{3+}). During deposition, this area near the substrate surface correlates to the start of film growth. The presence of many silicon dangling bonds would allow for hopping conductivity through the films and be a cause of the poor performance of MIM capacitors as well as resulting in a high etch rate.

Recalling that these films are produced at substrate temperatures below 60°C and noting that the silicon to oxygen ratio is balanced when using higher (250°C) substrate temperatures¹⁷⁵⁻¹⁸⁵, there is a significant change in film properties, likely due to growth kinetics, when using lower temperatures. Based on the XPS and ERD data, it is likely that the formation of OH groups plays a critical role. At lower substrate temperatures, the hydrogen appears to play a role in the removal of oxygen from the area of film growth. Some of the OH groups will be drawn away from the growth region, producing films with higher concentrations of silicon near the surface. As the film grows, more OH groups appear to bond with the silicon. This is likely a result of substrate heating caused by prolonged exposure to the ECR plasma. As deposition proceeds, the surface simply heats up, mimicking the effects of an induced higher substrate temperature.

At low substrate temperatures and high reactive gas/silane ratios, it is likely that a significant amount of hydrogen is removed via reaction with the ionized nitrogen. There is then more oxygen available for bonding with silicon and a higher substrate temperature is not required. From figure 4-6 we see that there the films are stoichiometric before substrate heating occurs. Using this method the substrates could be cooled, allowing for the use of temperature sensitive materials and substrates.

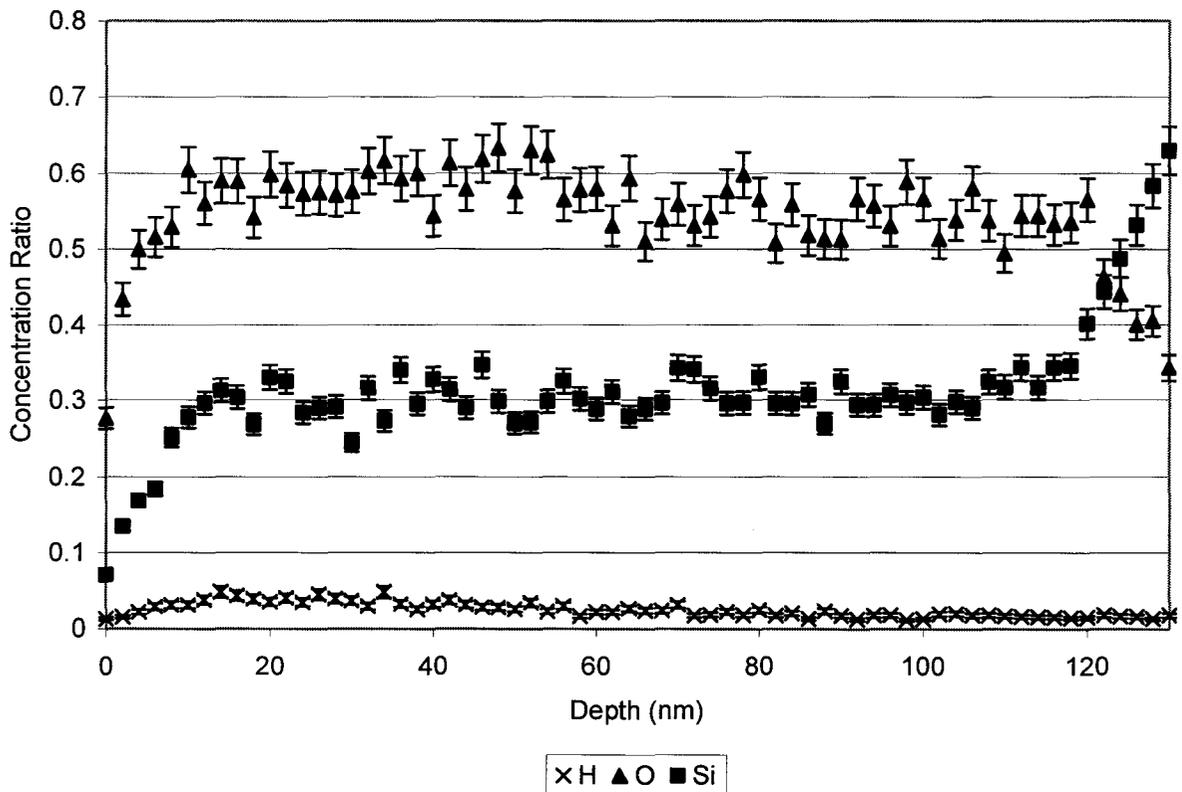


Figure 4-6 Material Concentration Ratios for Reactive ECR PECVD Films

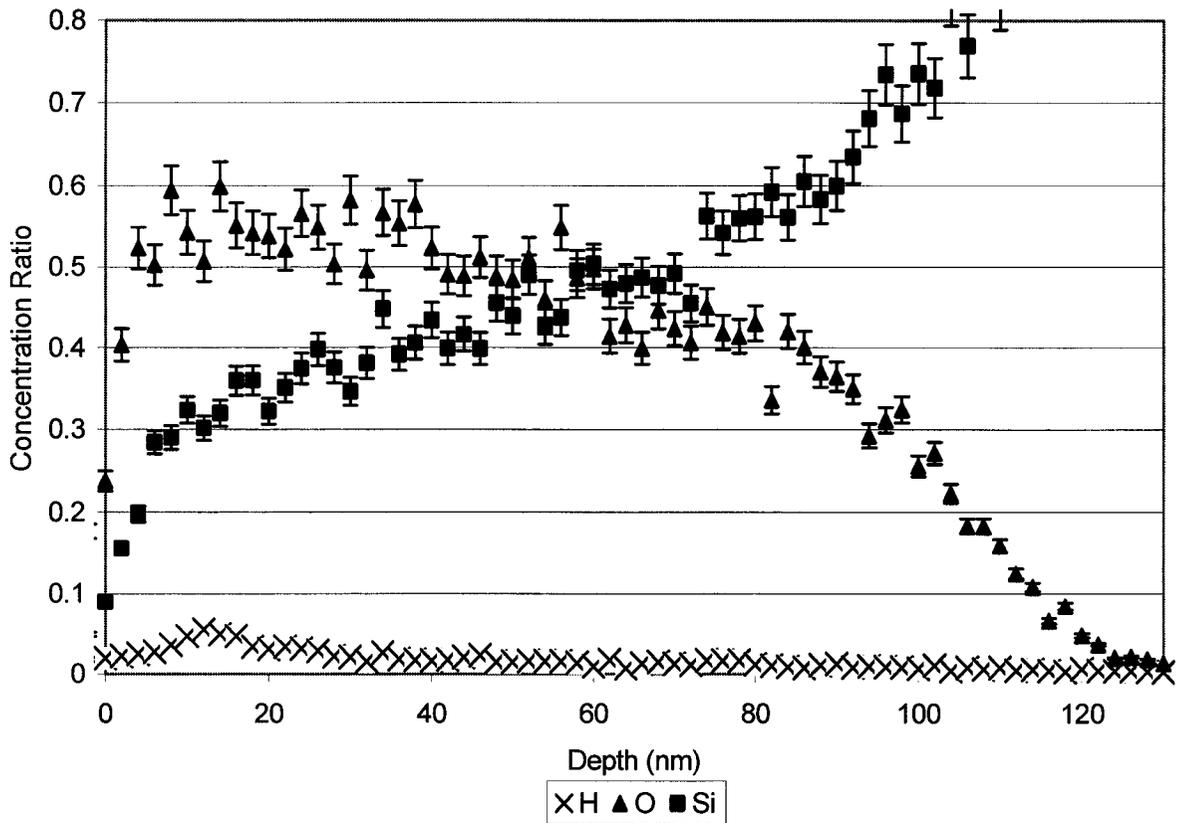


Figure 4-7 Material Concentration Ratios for Argon ECR PECVD films

4.1.1.4 AFM

Atomic Force Microscopy was used to evaluate the physical nature of the films. It was performed on SiON films that had been deposited on ITO coated glass substrates. The images show the presence of significant defects, specifically pinholes, in the argon based

films. There is no evidence of pinholes in the films produced by sputtering or with the nitrogen plasma. As seen in figures 4-8 a and b, there are more than 8 large pinholes, ranging in size from 3 to 6 μm , in the 100 μm square area. The presence of a single pinhole of diameter 3 μm is sufficient to cause catastrophic device failure. As aluminum is deposited on top of this dielectric it has direct contact with the underlying metal film, resulting in a short circuit. The resistance through this pinhole, with a depth of 100 nm, is less than 50 ohms.

Figure 4-8b, showing the same surface as figure 4-8a, illustrates a second defect type. Although the surface roughness of the films is low overall, less than 4 nm RMS, there is clear evidence of peaks that exceed 10 nm in height. Although this defect will not cause a short directly, it will produce a deviation in the applied field in a capacitive device. This would contribute to dielectric breakdown.

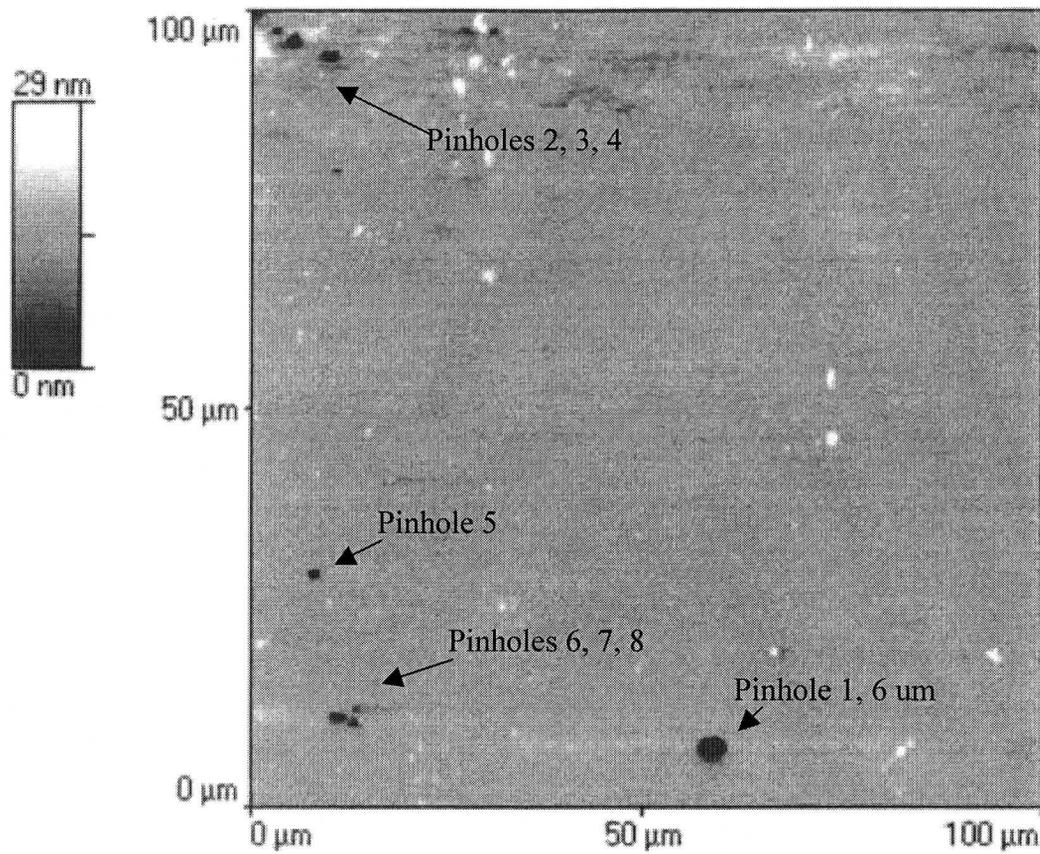


Figure 4-8 AFM Image of Argon Plasma Prepared Films

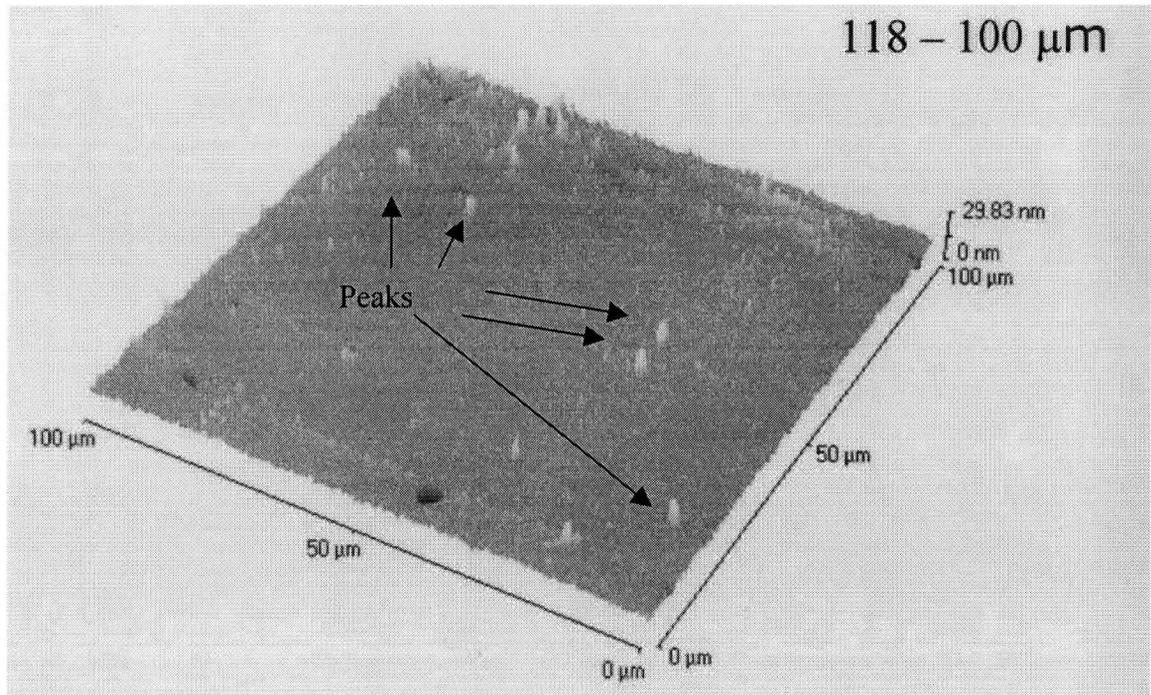


Figure 4-8b AFM Image of Plasma CVD SiON film.

4.1.1.5 Confocal Microscopy

Used in a high-resolution mode, the confocal microscope can reveal features of 0.1 μm in size. This allows for quick scans over large areas and is complimentary to AFM. Scans were done on SiON films that had been deposited on ITO coated glass substrates. The analysis supports the findings of the AFM, showing that there are pinholes throughout the argon produced films, figures 4-9 and 4-10. Pinholes could not be found in the films

fabricated by the nitrogen plasma CVD, sputtering or ion assist electron beam evaporated films.

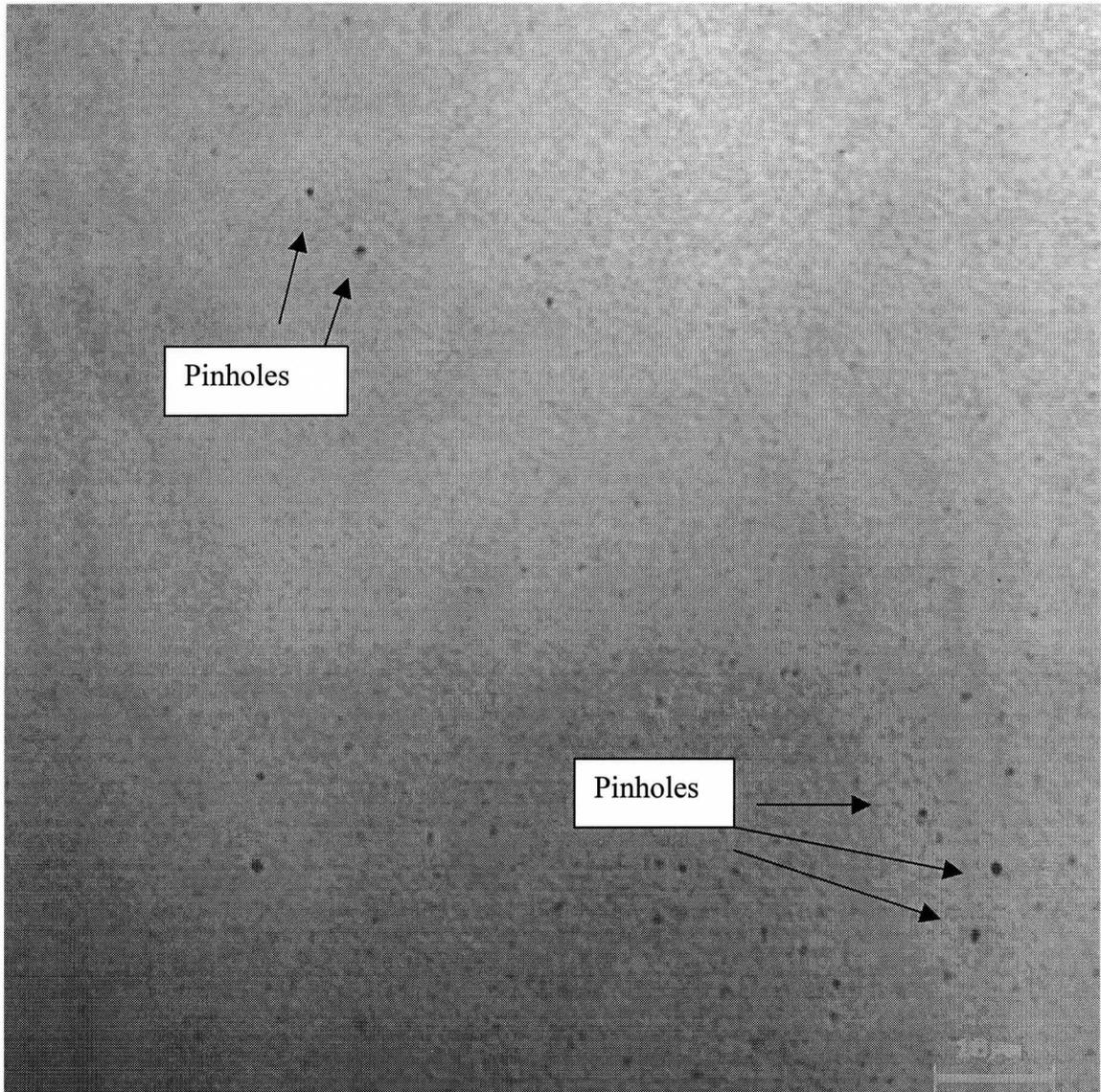


Figure 4-9 Confocal Image of an SiON Film Deposited using Argon CVD Method

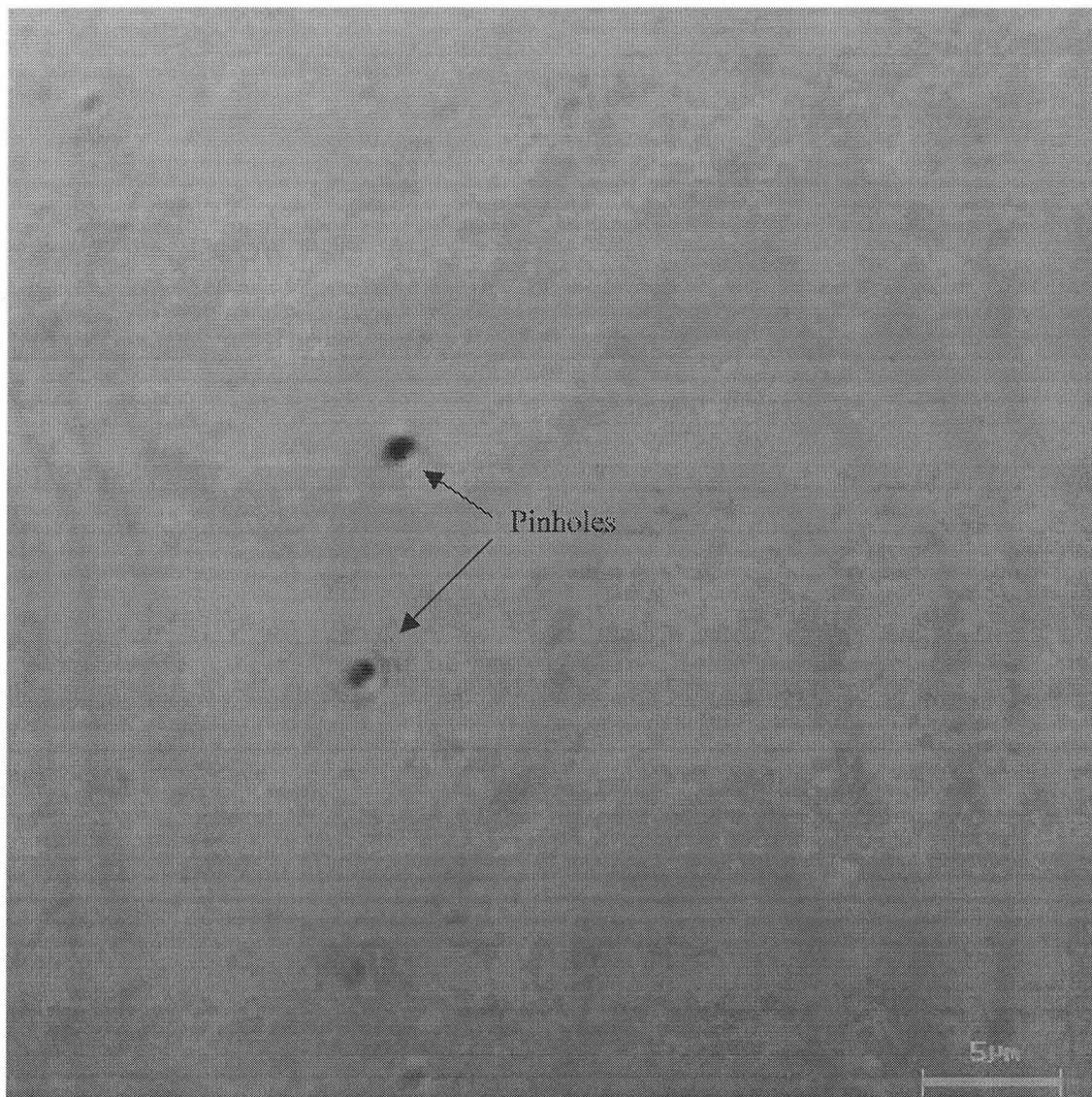


Figure 4-10 Confocal Microscopy Image of an Argon CVD Film.

4.1.2 SiON Devices

Capacitors were fabricated using SiON films, in two configurations. The first (MIM) uses a glass substrate with an indium tin oxide (ITO) semiconductor coating, followed by the SiON and capped with aluminum. The second (MIS) uses a silicon semiconductor substrate (p type) with an SiON film, with aluminum contacts.

4.1.2.1 MIM Capacitors

MIM capacitors of various surface areas were produced using all 4 deposition methods; 1. Sputtering 2. Argon CVD, 3. Nitrogen CVD and 4. Ion Assisted electron beam evaporation. The capacitors were tested primarily for leakage current, dielectric constant and dielectric breakdown. The DC capacitances were measured, from which the dielectric constants were derived using the measured film thicknesses. Film thicknesses were measured using an Alpha step thickness profile ometer and ellipsometry. The breakdown field strength was derived from the applied voltage required to cause 1 mA of current to flow through a 1 ohm sense resistor and the measured thickness. The devices produced with argon type SiON films all had extremely high leakage currents, were predominantly untestable, and are not shown.

The DC dielectric constants for films are shown in figure 4-11. For films produced in all three systems the dielectric constants are essentially the same and scale with refractive index, as expected.

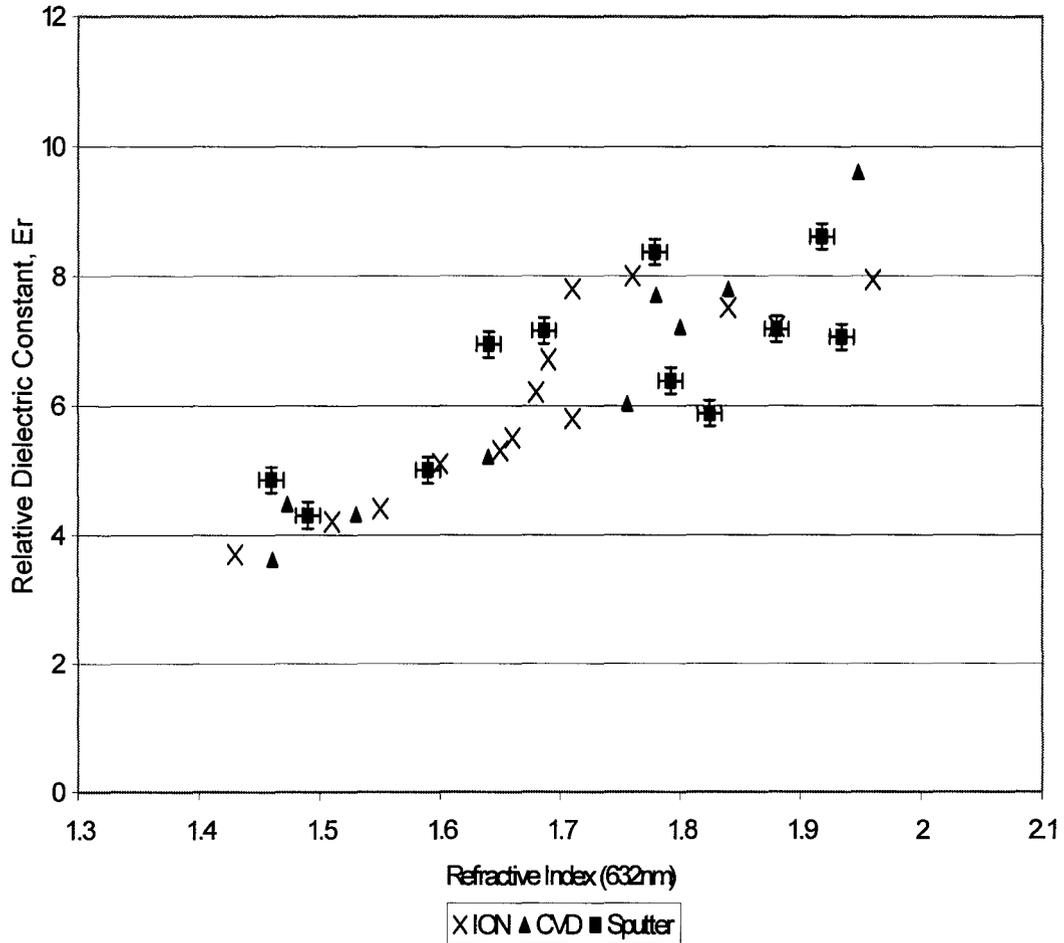


Figure 4-11 Relative DC Dielectric Constant

4.1.2.2 MIS Capacitors

Only nitrogen plasma based MIS capacitors were produced. These qualitatively reveal high interface state densities as shown by the variation between the high frequency measured and the modeled results, figure 4-12. The results confirm that the CVD dielectric films

produced were sufficiently pinhole free to produce working MIS structures as well as providing a high dielectric constant. (The dielectric films were 200 nm thick, with $n=1.85$). It was determined that quantitative interface state evaluation was not practical due to surface contamination of the samples and the accompanying difficulties in measurement²¹⁸⁻²²¹.

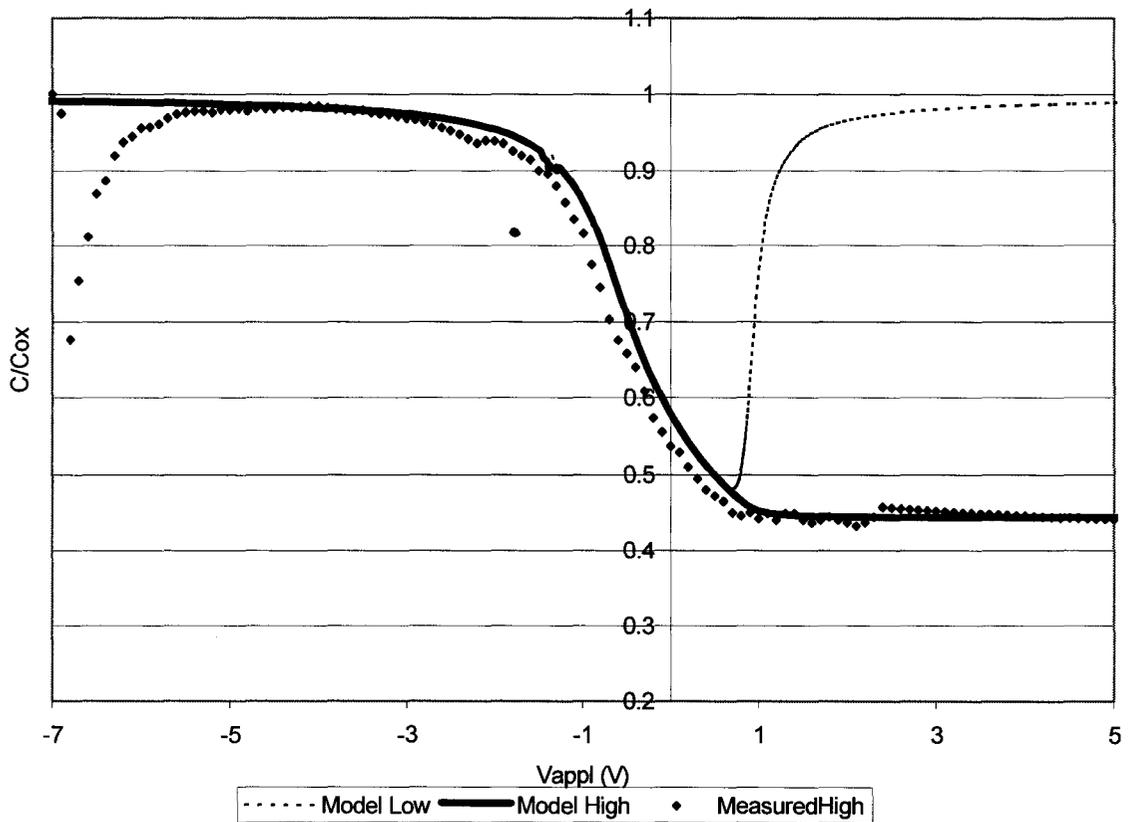


Figure 4-12 CV Characteristics of a Typical MIS Device

4.1.2.3 TFEL Devices

Thin film EL devices were fabricated. They consisted of a glass substrate coated with ITO, an SiON coating, then a ZnS:Mn emitting layer, followed by a second SiON coating, and finally an aluminum contact. Stress is a significant factor in the deposition of SiON films and is particularly important when fabricating TFEL devices. Devices using SiON films with indices greater than 1.85 were unstable and were subject to de-lamination. These devices were tested for CV, QV and LV characteristics.

A comparison of CV characteristics of TFEL devices produced with Nitrogen ECR PECVD SiON dielectrics and sputtered SiON dielectrics is shown in figure 4-13. The CVD devices produce a steeper slope in the CV graph, indicating a low density of shallow interface states as compared to the sputtered films. This is suggestive of a more abrupt transition from the dielectric to phosphor layer in the CVD TFEL devices. The insulator capacitance is also slightly higher for the CVD films. This can result from the presence of space charge in the phosphor. However, as both phosphors were deposited simultaneously this is not the case. The increase in measured capacitance can also be caused by reduced field clamping in the CVD TFEL device. With a reduction of the interface state density, the negative feedback from interface state emission is insufficient to maintain a constant phosphor field.

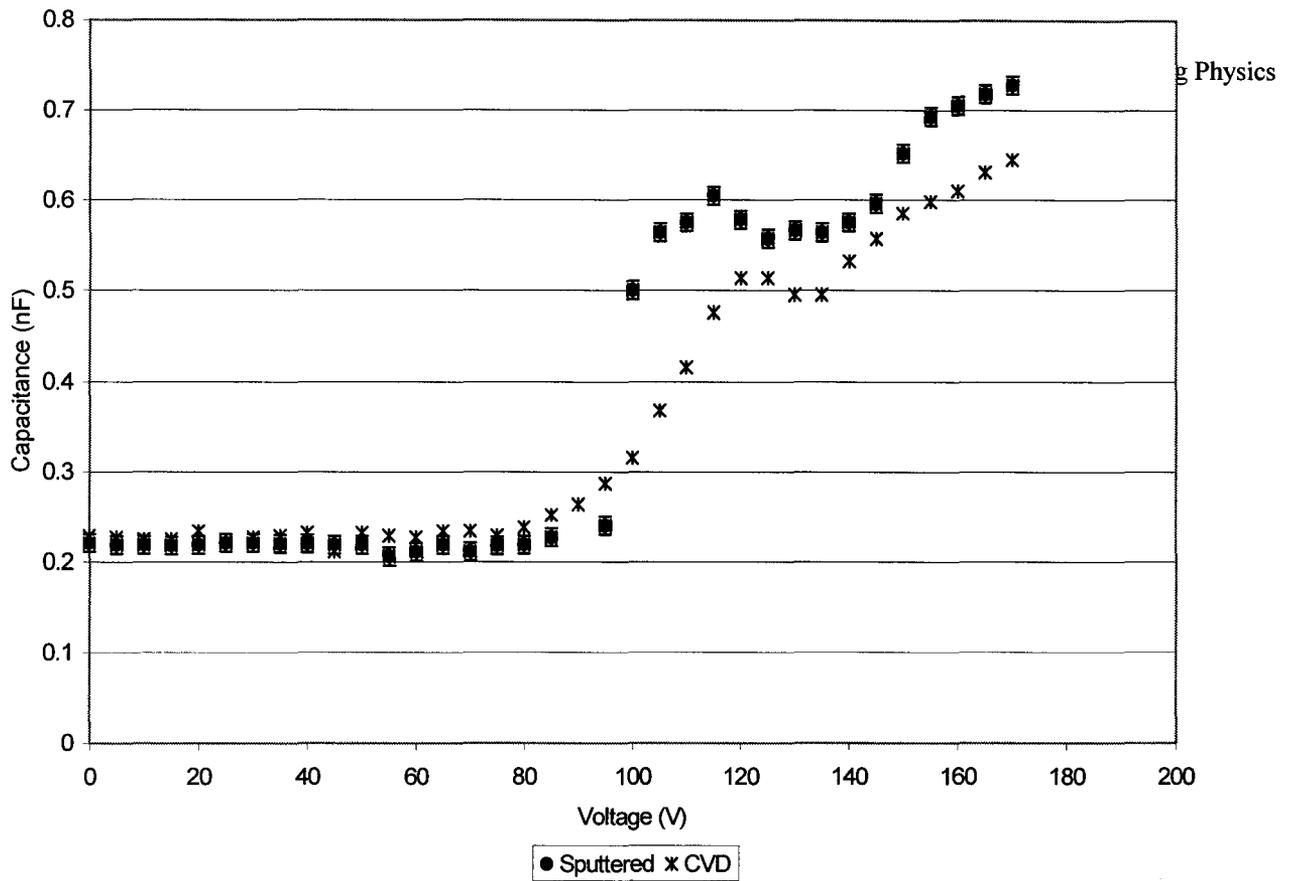


Figure 4-13 Comparison of the CV Characteristics of Nitrogen ECR PECVD and Sputtered TFEL devices

Figure 4-14 shows a comparison of the QV characteristics of typical nitrogen ECR PECVD and sputtered TFEL devices. As both devices utilize identical phosphor layers, the phosphor charge is the same. There is no notable difference between the two devices.

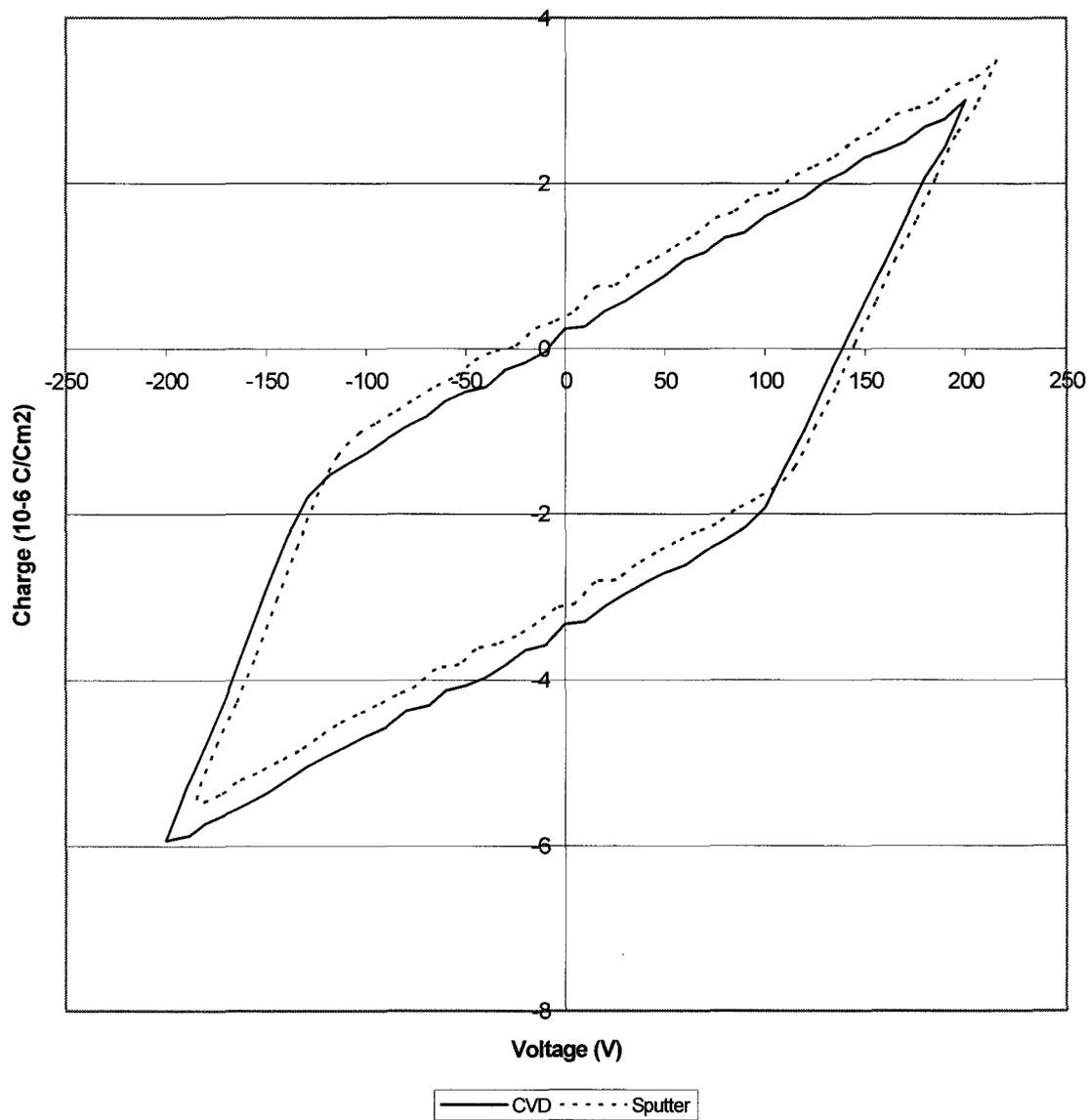


Figure 4-14 Comparison of the QV Characteristics of nitrogen ECR PECVD and Sputtered TFEL Devices.

Finally, comparative LV characteristics, of the nitrogen ECR PECVD, sputtered and ion assist devices are given in figure 4-15. Here we can see nearly identical performance from the nitrogen CVD and Ion Assist devices. The CVD device outperforms the sputtered devices, particularly at higher voltages. This is likely due to field clamping at lower voltages in the sputtered devices that result from a higher interface state density.

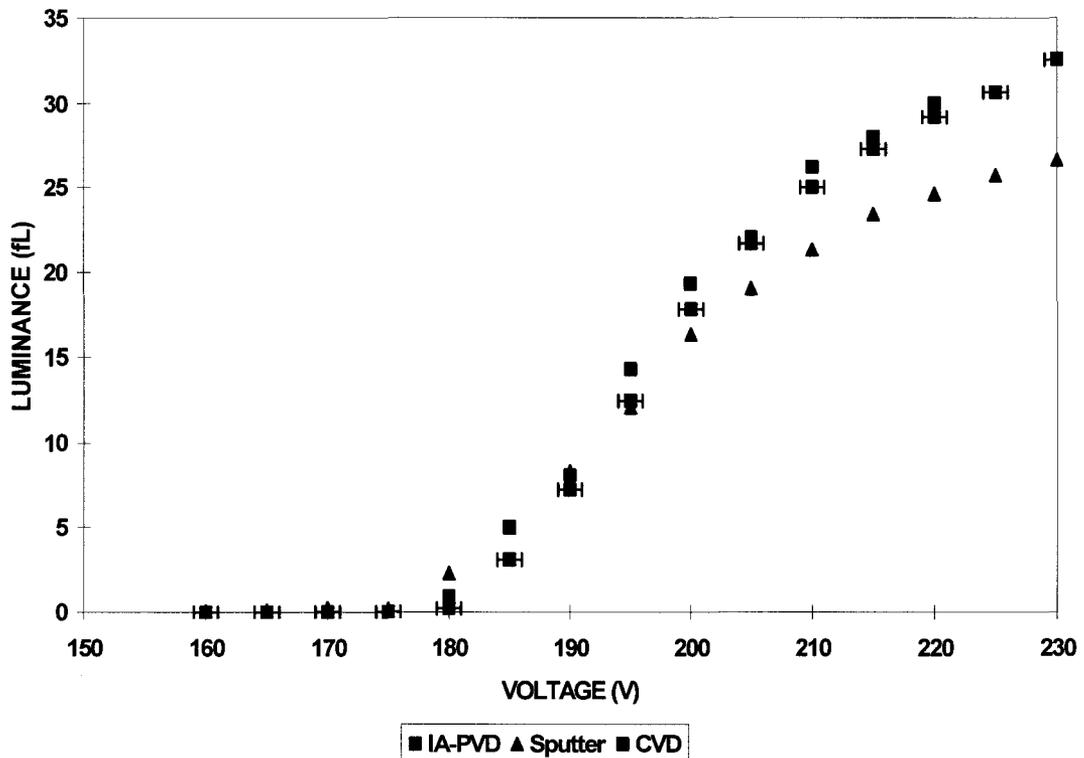


Figure 4-15 Comparative LV Characteristics for TFEL Devices with IAPVD, Sputtered and CVD SION Films.

4.2 Metal Induced Crystallized Silicon films

4.2.1 Nickel Induced Crystallization

Nickel induced crystallization of amorphous silicon films was examined. The 200 nm a-Si:H films were produced by ECR PECVD at room temperature using an argon based plasma. The films were then coated with a 2 nm layer of nickel. The films were vacuum annealed at 950° C for 20 seconds to produce crystallized films. Films annealed in nitrogen all produced highly oxidized films. This was likely the result of trace amounts of oxygen and or moisture during the anneal process.

The substrates used in all cases except for XRD, were silicon wafers coated with a buffer layer of 200 nm of SiON. The buffer layer was used to avoid substrate induced crystallization. For XRD analysis glass substrates were used.

4.2.1.1 XRD

The XRD analysis, figure 4-16 shows that the films crystallized with a (111) orientation as compared to as deposited amorphous silicon samples, which show almost no crystallization. There is also evidence of crystallization with a (220) orientation. The fraction of crystallization with a (220) orientation can be reduced by reducing the film thickness. This will limit the growth along the (220) plane. There is no evidence of low nickel concentration silicides, NiSi, as there are no peaks in the appropriate region as indicated on the graph. It must be noted that peaks at the locations of the Si <111> and Si <220> points can also be indicative of the presence of NiSi₂. However, from the figure, there is an absence of a

significant peak at 57, 2 theta point. If NiSi_2 were present in significant quantities, there would be a significant peak at this point. This suggests that the NiSi_2 species is not present in significant quantities.

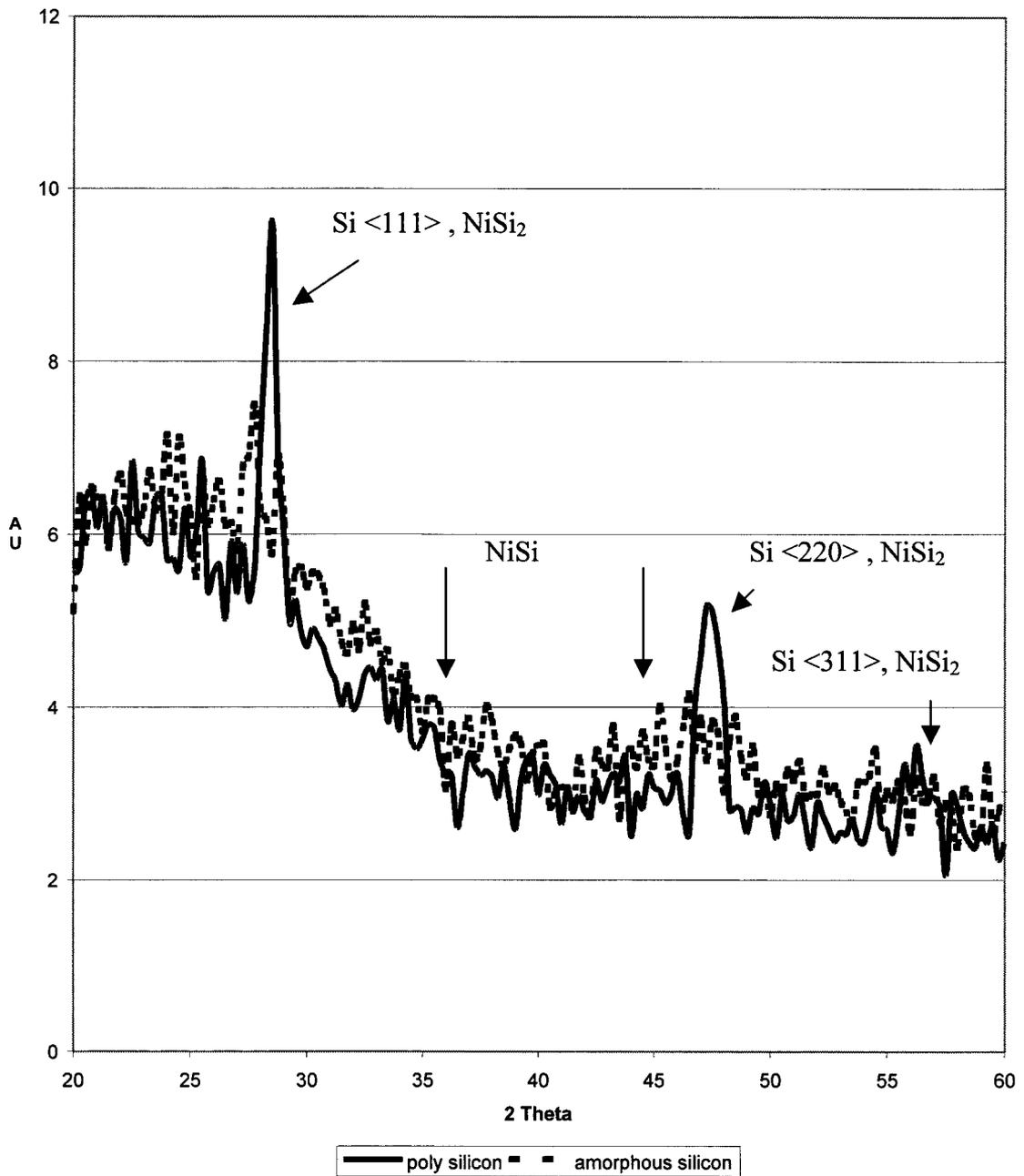


Figure 4-16 XRD 2 Theta Scan of Nickel Induced Crystallized Silicon.

4.2.1.2 XPS

The XPS spectra are shown for partially nickel-crystallized, figure 4-17, and fully nickel- crystallized, figure 4-18, silicon films. From these two graphs we can determine the percentage concentration of silicide to silicon metal by integrating the area under each curve in the deconvolution. For the partially crystallized region, which was annealed at a lower temperature for less time, we get 34.4% silicide in a silicon matrix. For the fully crystallized region we get 27.4% silicide. Then, the relative concentrations of silicides to silicon metal are (34.4%, 27.4%) for the partially and fully crystallized films respectively, showing that the percentage of silicides in the films decrease as the crystallization proceeds. These results are also complementary to the preceding XRD measurements, indicating that there is a large percentage of crystallized silicon in the films rather than a large concentration of silicides. These measurements were done at a depth of 30 nm into the film and are intended to show the progress of the silicide front into the film. Nevertheless, the results indicate that there is still a significant nickel concentration near the surface, 5-10%.

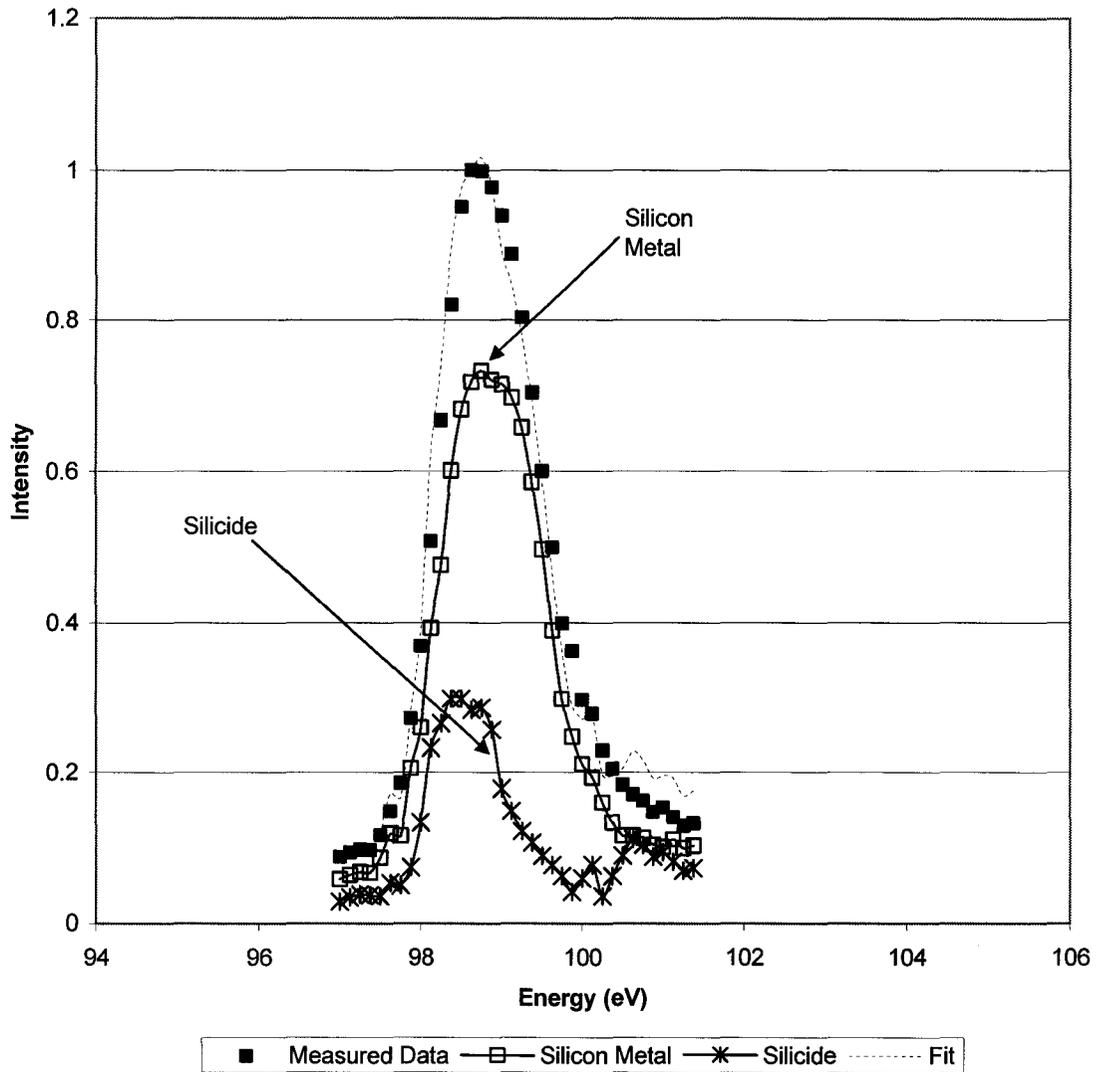


Figure 4-17 XPS Data for Partially Nickel-Crystallized Film

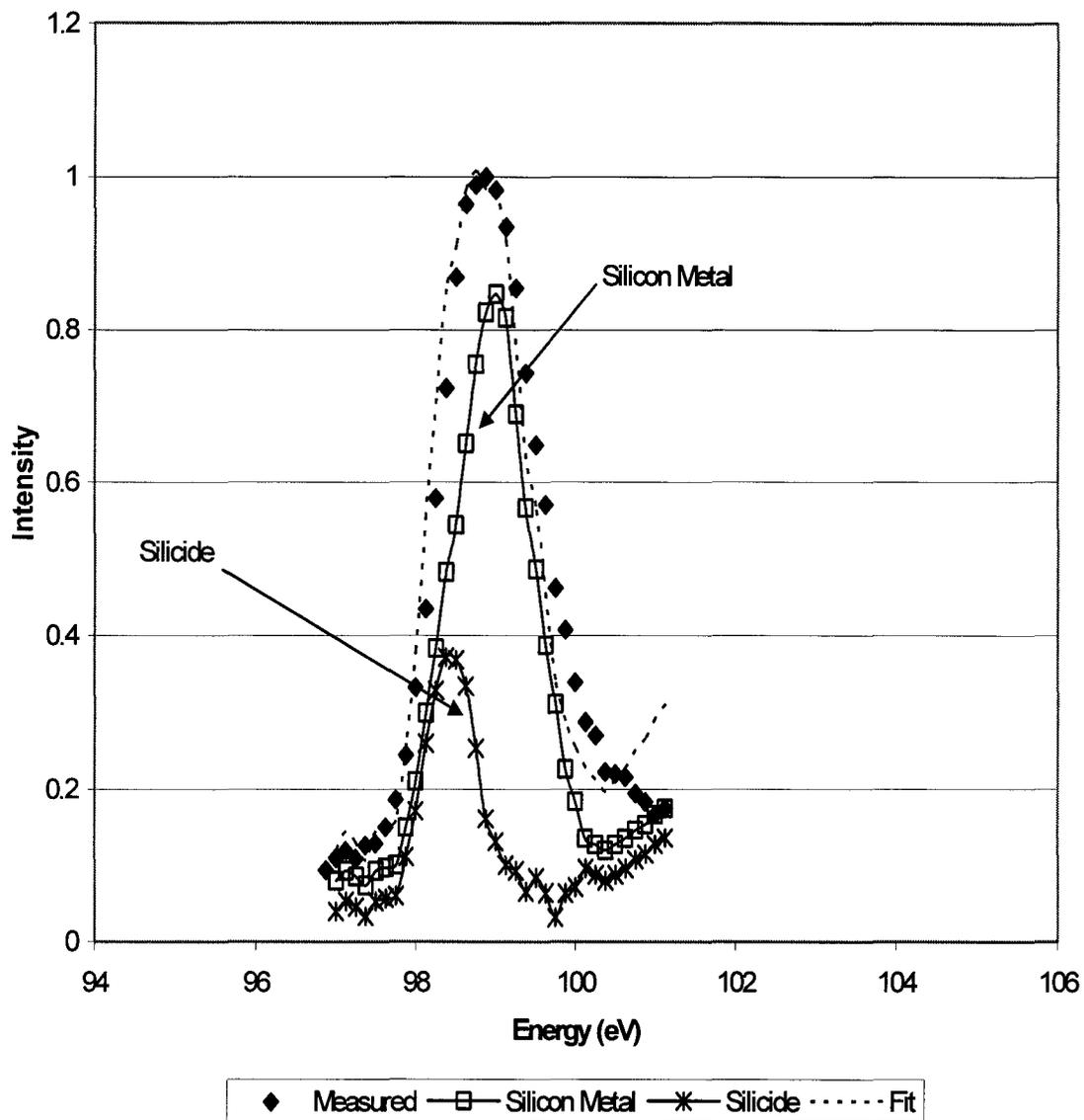


Figure 4-18 XPS Data for Fully Nickel-Crystallized Film

4.2.1.3 TEM

TEM analysis was carried out on the fully crystallized samples on silicon substrates. The TEM image in figure 4-19 shows 3 distinct areas. To the bottom right is the silicon substrate, followed by a buffer layer of SiON. Then there is the nickel induced crystallized silicon film. The crystallized silicon area has distinct variations. This is likely a result of variations in the initial density of the thin nickel metal layer. The crystal size will be dependent on the seed crystal density, which will be dependent on the metal distribution in the thin nickel layer. In turn, this thin nickel layer will be discontinuous and somewhat random. The diffraction pattern, shown in figure 4-20, confirms that the silicon has crystallized. Areas not crystallized or partially crystallized showed the distinctive ring pattern associated with an amorphous film, figure 4-21.

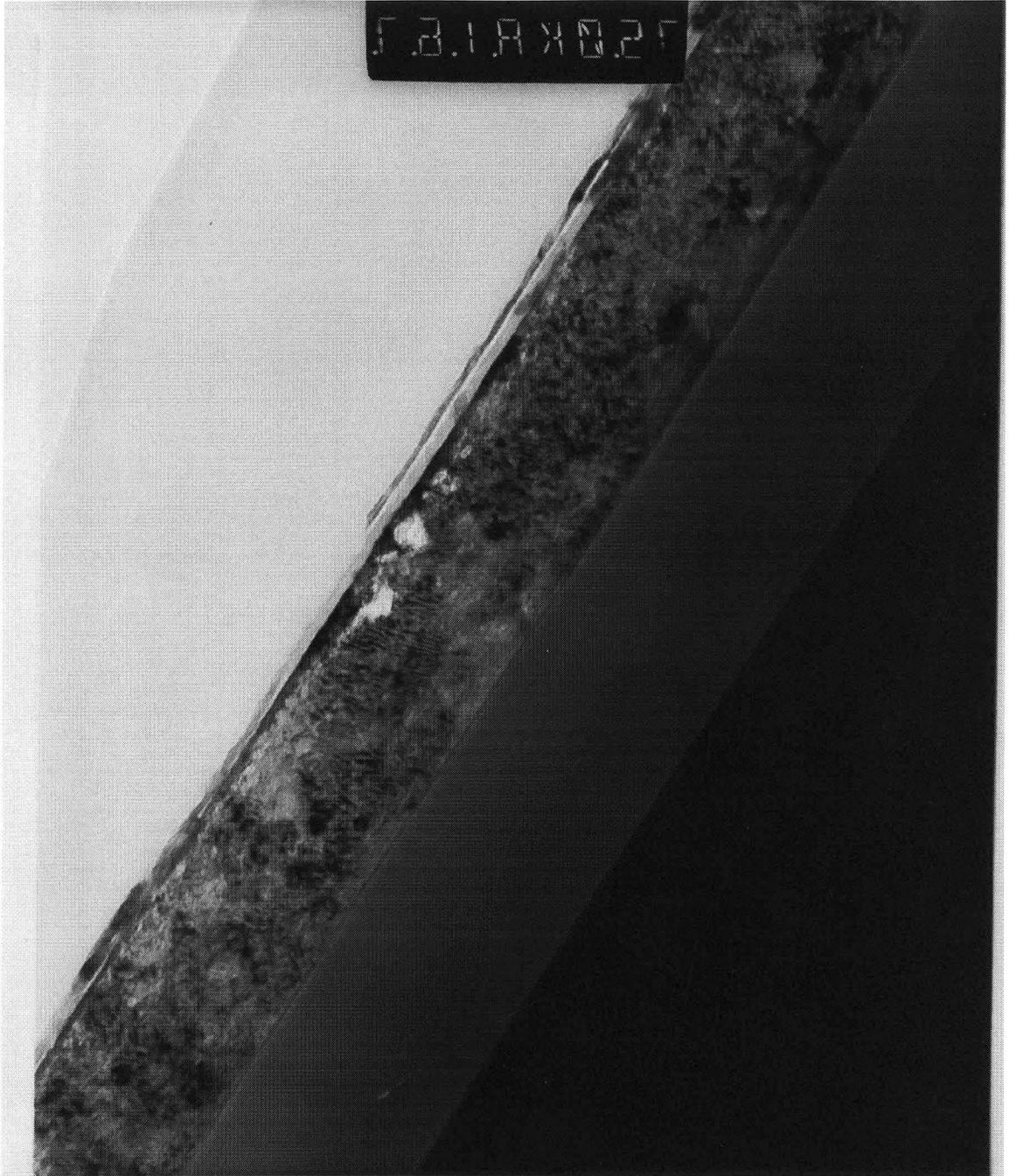


Figure 4-19 TEM Image of Nickel Induced Crystallized Silicon



Figure 4-20 TEM Diffraction Pattern of Nickel Induced Crystallized Silicon Film



Figure 4-21 TEM Ring Pattern Associated with an Amorphous Film

4.2.2 Boron/Nickel Induced Crystallization

These films were produced as above with a 1 nm thick layer of Boron deposited before the 2 nm thick nickel layer. The objective was to examine the potential of simultaneous boron doping and nickel induced crystallization with the objective of simultaneously inducing crystallization and doping. In this case, boron is intended to act as a p-type dopant.

4.2.2.1 XRD

A similar XRD pattern was observed as above indicating that there is no significant effect of Boron co-doping on the crystallization as measured by XRD.

4.2.2.2 XPS

The XPS analysis gave similar results as in section 4.2.1.2 above, in that the fraction of silicide decreases as crystallization proceeds. Figure 4-22 shows the concentration depth profile for the crystallized samples, with the concentrations of silicon, boron and nickel (Si2p, B1s, Ni2p) shown. The graph is divided into three sections that correspond to the sample. Section I comprises the surface area that received the metal capping layer (2 nm nickel and 1 nm boron deposited). This section has a relatively high concentration of boron and nickel. Section II is the region of bulk crystallized silicon. The nickel concentration can be seen to be relatively constant throughout the samples at about 1%. The boron can be seen to drop to near zero at the silicon surface and climbing to over 1% before dropping again near the SiON substrate. This is significant as low temperatures and short time (950° C, 20 s)

annealing produced good doping depth penetration in contrast to standard diffusion conditions (much higher time temperature product). Section II comprises the SiON buffer layer.

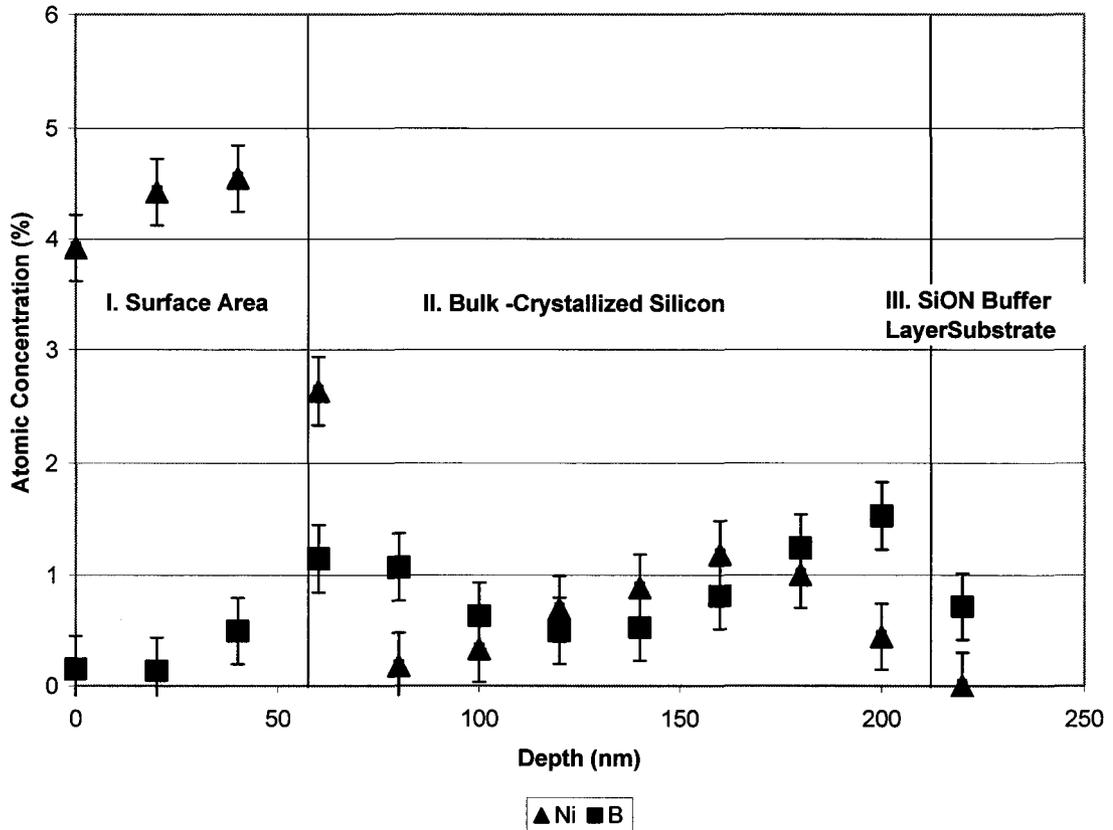


Figure 4-22 XPS Depth Profile of Boron/Nickel Induced Crystallized Silicon Film

There is no significant shift in the bonding states of silicon or nickel in the bulk material as shown in figures 4-23 and 4-24, where there is virtually no change in the binding energy of the peaks. This result suggests that the relative material concentrations are real and

not simply a bi-product of changes in bond states. The profiles illustrate the evolution of the Si2p and Ni2p XPS peaks, respectively. The first XPS trace, which starts at 50 nm into the material, is shown at the bottom of the graph. Silicon is seen to be a convolution of metallic and silicide species as indicated in figure 4-18. In contrast, the nickel appears to be in the form of a silicide only.

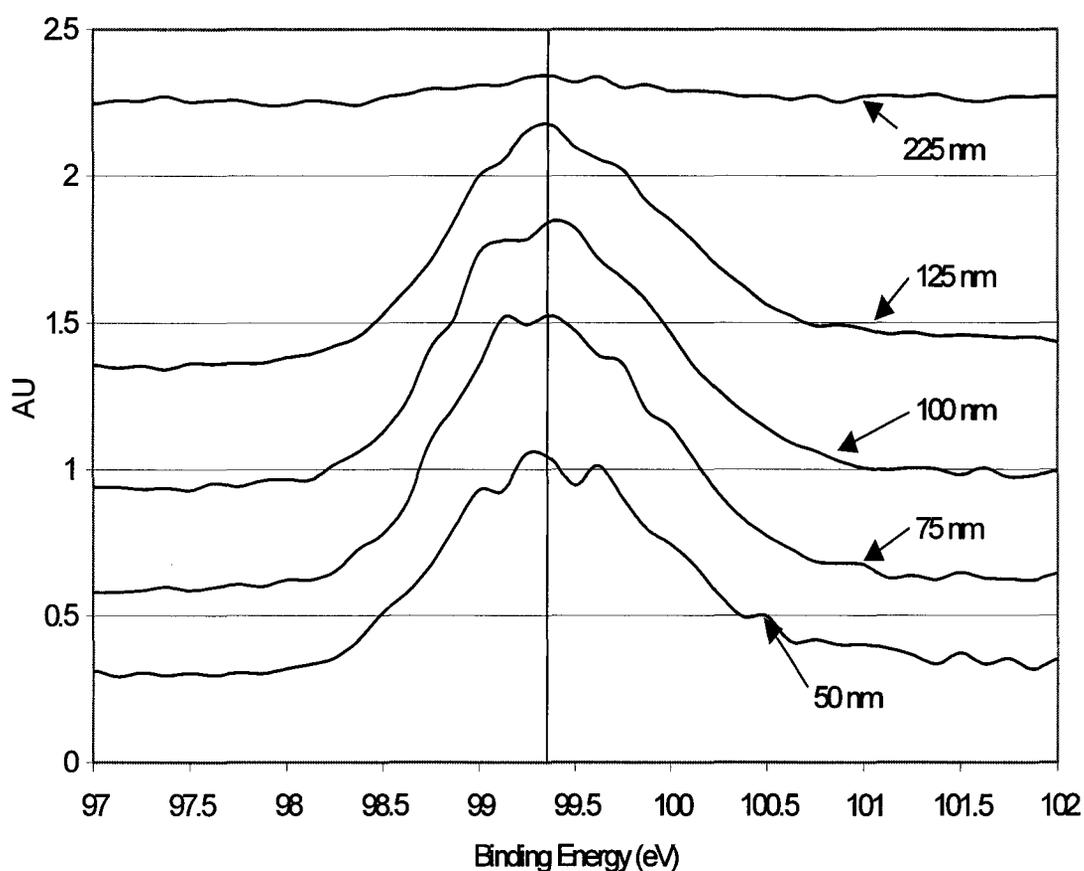


Figure 4-23 Evolution of Si2p Peak (XPS) with Film Depth

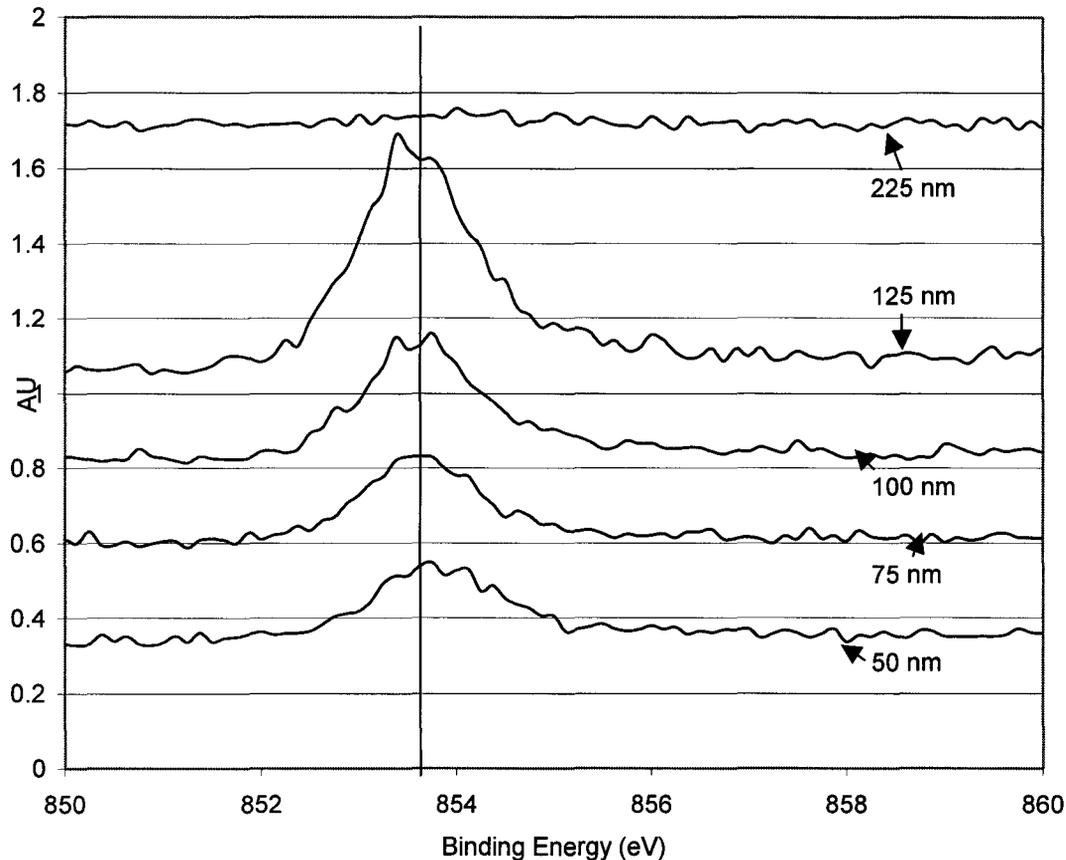


Figure 4-24 Evolution of Nickel 2p Peak with Film depth

4.2.2.3 TOF SIMS

Time of flight secondary ion mass spectroscopy (TOF SIMS) was used to examine the depth profile of the nickel and the boron in the same samples as used for XPS analysis. The results, in figure 4-25, show that the nickel and boron profiles agree with those found by the XPS analysis, figure 4-22. There is significant variation in the concentrations of the species throughout the samples. From TOF SIMS, the boron and nickel concentrations are

found to be approximately 0.05% to 0.8%(0.5-1% XPS) and 0.1% to 1%(0.2-1.2% XPS) respectively. The error in determining concentration in this case is approximately 50% of concentration. This is due to difficulties in calibrating the system for the ion yield from a partially crystallized silicon lattice.

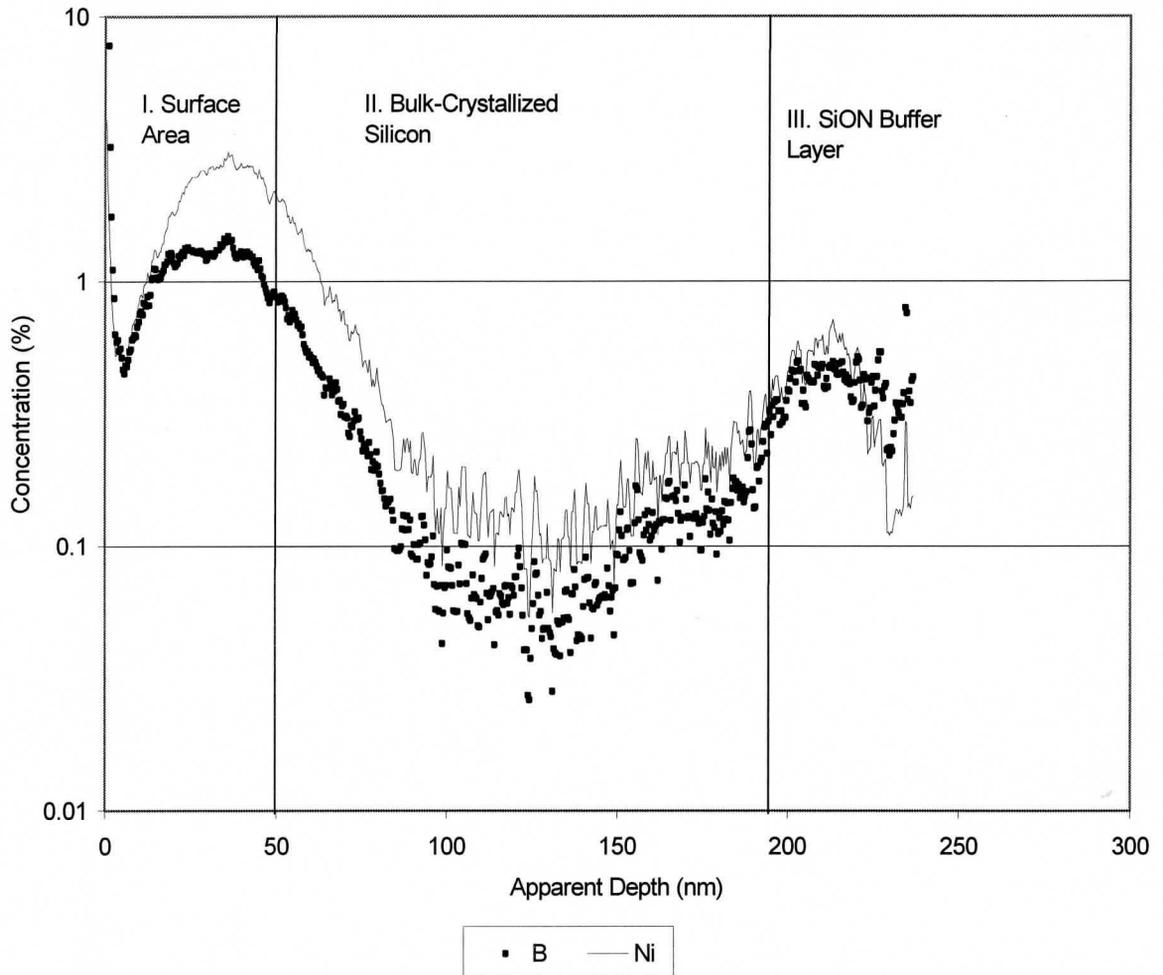


Figure 4-25 TOF SIMS Depth Profile of Boron and Nickel.

4.2.2.4 Dynamic SIMS

For further clarification of the material composition of the films, dynamic SIMS analysis was conducted, as shown in figure 4-26. From this analysis, the relative nickel and boron concentrations range between 0.4-1% and 0.2-1% respectively in the bulk material region.

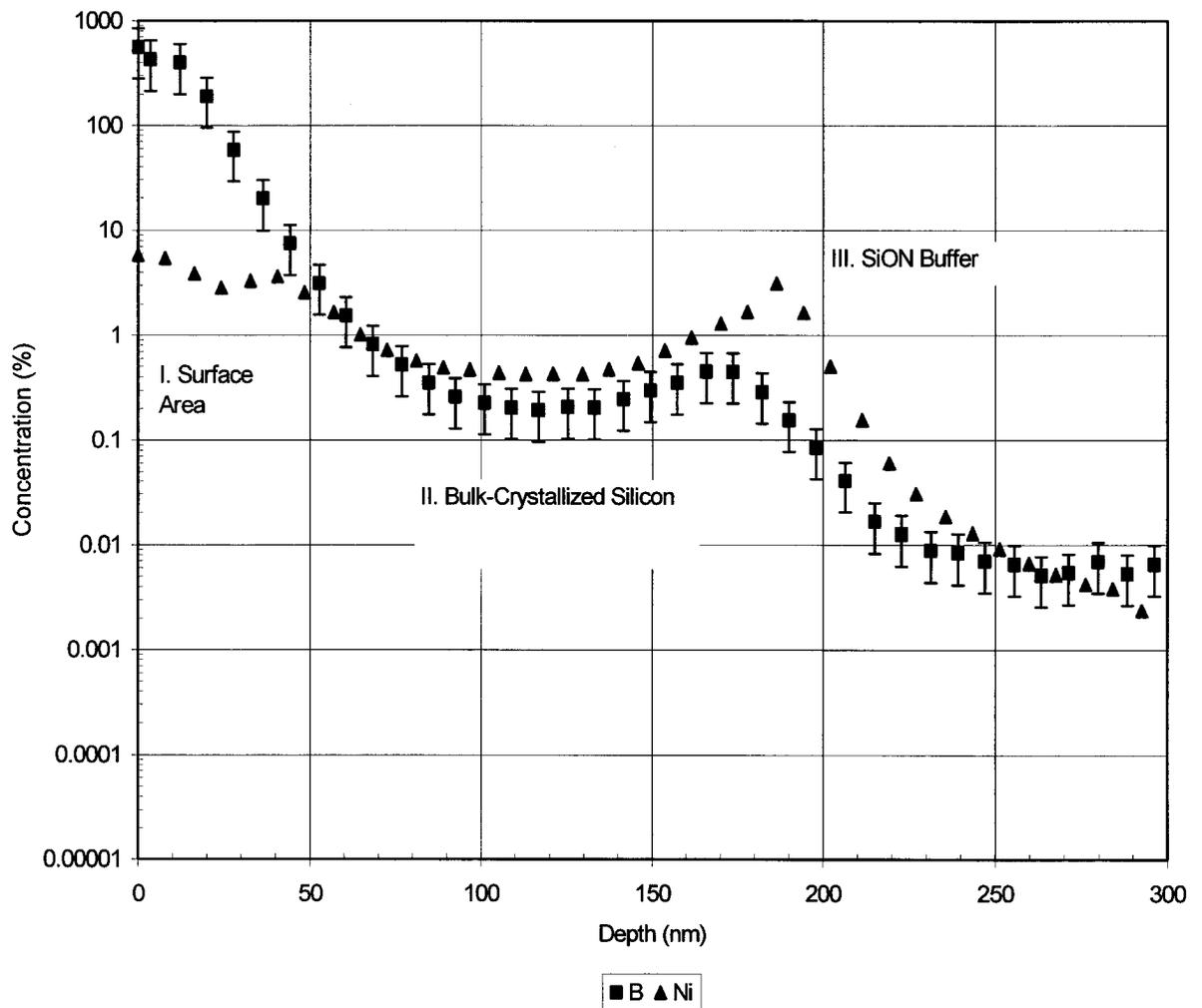


Figure 4-26 Dynamic SIMS of Crystallized Silicon Film

A comparison of the trace metal concentrations is shown in Table 4-1.

| | XPS | ToFSIMS | DynSIMS |
|-----------|------------|----------------|----------------|
| B | 0.5-1.0% | 0.05-0.8% | 0.4-1.0% |
| Ni | 0.2-1.2% | 0.1-1.0% | 0.2-1.0% |

Table 4- 1. Comparison of Trace Element Concentrations in Crystallized Silicon

5 PROTOTYPE DEVICES BASED ON METAL INDUCED CRYSTALLIZED SILICON

5.1 MIS Capacitors

MIS capacitors were produced using the boron doped nickel induced crystallized silicon as the semiconductor material, figure 5-1. The analysis shows that the material is p-type with heavy doping as indicated by the low C/C_0 ratio.

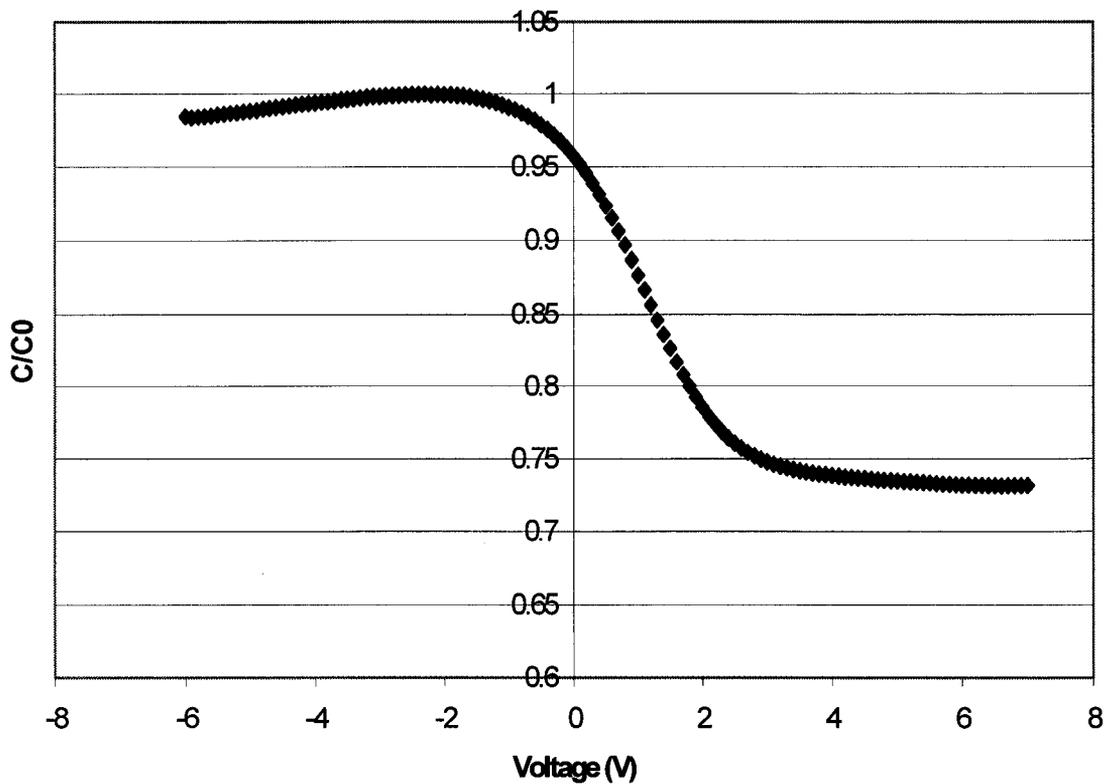


Figure 5-1 P Type MIS Structure, Boron Doped

5.2 Thin Film Transistors

TFTs were produced using boron doped nickel induced silicon as the semiconductor material. The TFTs were planar type deposited using shadow masks. The crystallized silicon was phosphorus doped at the source and drain. The gate dielectric was deposited through a shadow mask, followed by the gate metal. An HP semiconductor parameter analyzer was used to examine the operating characteristics. The $I_d - V_d$ characteristics are shown in figure 5-2 and the transfer characteristics are shown in figure 5-3.

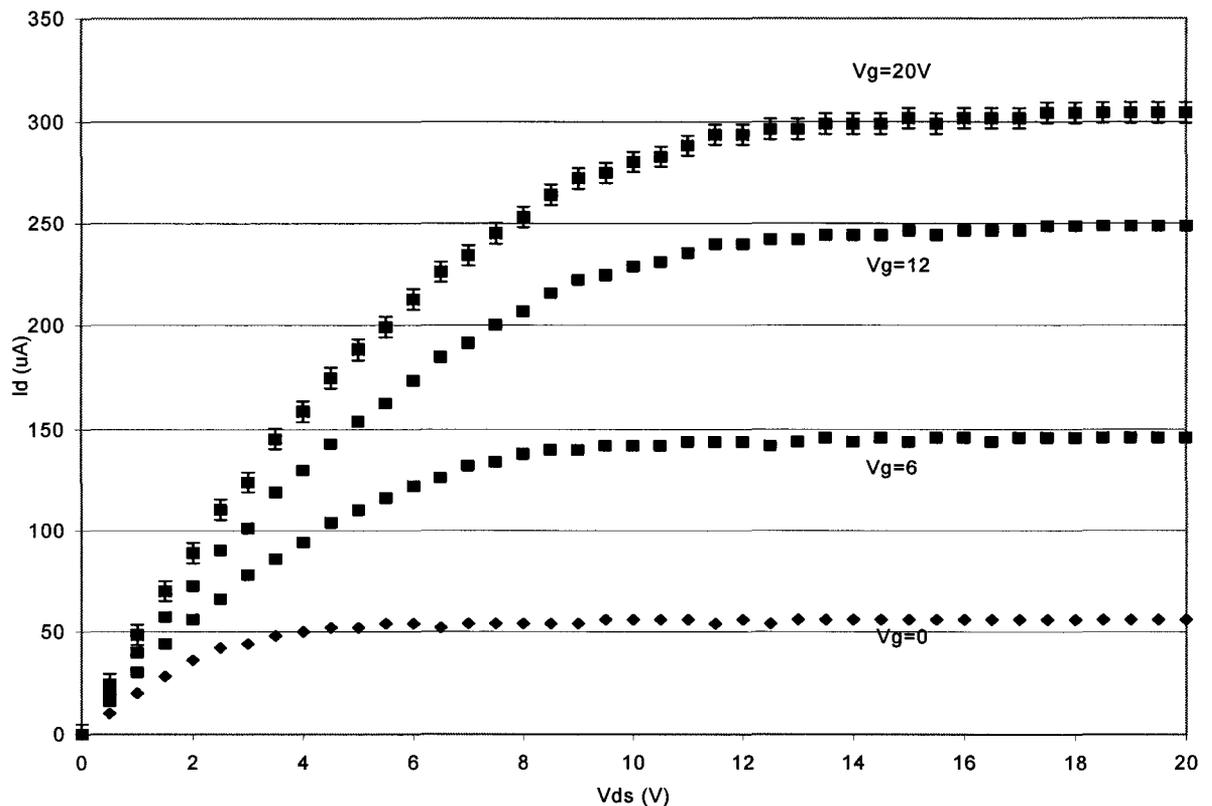


Figure 5-2 I_d vs. V_d Characteristics.

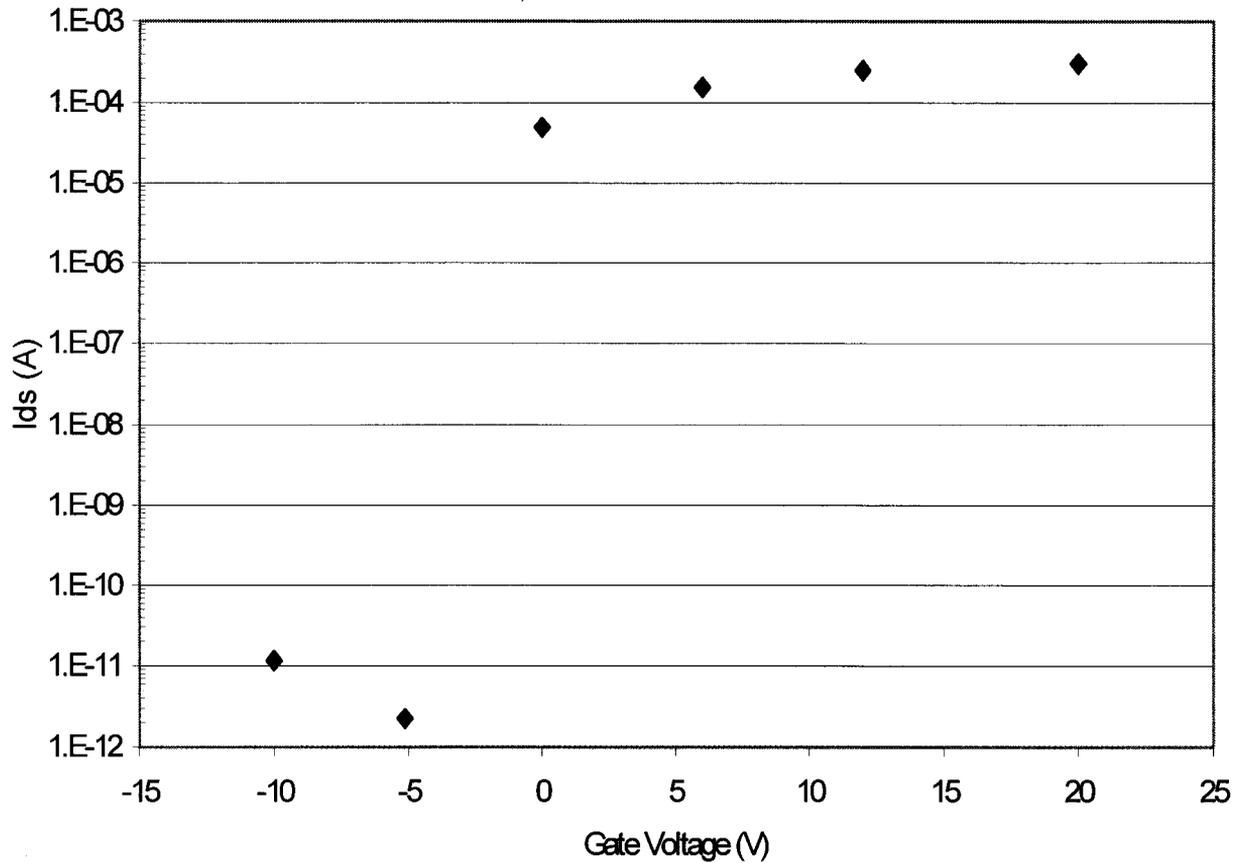


Figure 5-3 Transfer Characteristics.

The $I_d - V_d$ characteristics shown in figure 5-2 indicate large gate voltages. This is a result of relatively thick gate oxides (on the order of 200 nm). Thick gate oxides were used to avoid shorting. These transistors also demonstrated high light sensitivity. The active areas of the

transistors were not covered and carriers were optically created.

These results demonstrate that the general approach indicated is valid. Nickel induced crystallized silicon can be used in large gate thin film transistors. Although further optimization is required, the results are comparable to previously reported results⁹⁵.

6 CONCLUSIONS

The main objective of this work was the examination of the usefulness of the ECR PECVD deposition method for the use in flat panel display applications. Specifically, low temperature ($<60^{\circ}\text{C}$) deposition of SiON dielectric films was examined for use in TFEL displays and as a gate insulator in microelectronic applications. In addition, the use of ECR PECVD amorphous Si:H films was examined as the source film for nickel induced crystallization of silicon.

Among the general findings in this work, two significant findings are noted. The ECR PECVD method can be successfully utilized at low temperatures to produce high quality dielectric films. The key is the use of a high nitrogen to silane ratio, which, due to the limitations of the system, requires the use of a nitrogen plasma as opposed to the standard argon plasma. The ionization efficiency of nitrogen is also significantly higher than argon, resulting in a large percentage of ionized nitrogen ($\sim 5\%$) available for bonding.

The second finding is that the ECR PECVD method can be utilized to produce a-Si:H films that can be crystallized through nickel catalyzation, to produce materials with high mobilities. In turn, these materials can be used to produce thin film transistors using a shadow mask technology and low resolution photolithography. This is due to the fact that the gates can be made relatively large ($>10\text{ }\mu\text{m}$). Also, the films can be simultaneously doped with boron.

There are several areas of research that can be expanded upon in future work. The increase of the deposition rate and effective deposition area is critical to developing a true production process. In regards to the nickel induced crystallization, further work is required on the control of grain size and the effects of contamination caused by the nickel.

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