THE DUAL – GATE MOSFET

DUAL - GATE MOSFET STATIC CHARACTERISTICS GENERATED FOR MIXING APPLICATIONS

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SCOPE AND CONTENTS:

The static electrical characteristics of dual-gate silicon n-channel insulated-gate field-effect transistors are investigated experimentally. A mathematical model based on theoretical expressions and containing twelve parameters adjusted for best fit was developed.

The mathematical model was used to calculate the low frequency conversion transconductance as a function of operating conditions.

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INTRODUCTION

The Dual-Gate MOSFET makes an ideal mixing device. The transistor features a series arrangement of two separate channels, each channel having an independent control gate. The mixing function performed by the device is unique in that the signal applied to one gate is used to modulate the input gate transfer characteristics. This technique is superior to conventional "square law" mixing which can only be accomplished in the non-linear region of the device transfer characteristics.

In the design of mixers, the following are of considerable importance in obtaining a good overall circuit.

a) Conversion gain

b) Noise figure

c) Dynamic Range

d) Cross modulation

The importance of each of the above factors can vary immensely depending on the circuit application.

This work presents a method for obtaining the maximum conversion gain in a mixer circuit using a dual-gate MOSFET. The most direct way of finding the largest gain is to measure and plot the conversion transconductance over the whole operating range of the device. This would be very tedious as there are four applied voltages that have to be varied.

An alternative approach is to record the transconductance or static characteristic curves and convert them to conversion transconductance curves. This technique also requires many measurements as there are still three voltages that have to be varied. A third method of obtaining the maximum conversion gain which requires by far the least number of measurements is used in this thesis. A model of the dual-gate MOSFET is found with the aid of a computer using only thirteen experimental points. The computer program uses this model to generate the static characteristics of the device. The static characteristics are converted to transconductance curves which in turn are changed into conversion transconductance curves. The maximum conversion gain is then easily found from the conversion transconductance curves.

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CHAPTER I

THE SINGLE GATE MOSFET

To make it possible to obtain a model of the dual-gate metal-oxide semiconductor (MOS) field-effect transistor (FET), first order approximation theory will be used. Since the proposed model is essentially two single gate MOSFET's in series the theory of the single gate device will be developed first.

1.1 THEORY OF OPERATION

The approximations used to develop the equations for the single gate MOSFET are as follows:

(a) Doping of the substrate is uniform and nondegenerate.

(b) The variation of the channel thickness is small along the length of the channel.

(c) The channel is completely shielded from the drain, so no drain-to-channel feedback exists.

(d) The drain current consists only of channel current. Leakage currents are neglected.

(e) The gate dielectric is considered to be a perfect insulator.

(f) Extrinsic conditions which affect the conduction properties - such as oxide traps, silicon surface states, interface energy states, ionic centers within the oxide, and work-function

differences - will be lumped together into a single effective charge term, Q_{ss}. Furthermore, Q_{ss} is assumed to be constant and located at the silicon-oxide interface.

(g) Mobility of current carriers in the channel is constant.

(h) The thickness of the dielectric over the channel region is assumed to be much greater than the channel thickness.

Even though the following analysis refers specifically to an N-channel MOS on a P-type substrate, the resulting equations are applicable to both N-channel and P-channel devices.[1]

To develop the current equations for the simple MOSFET we shall refer to Figure 1-1.

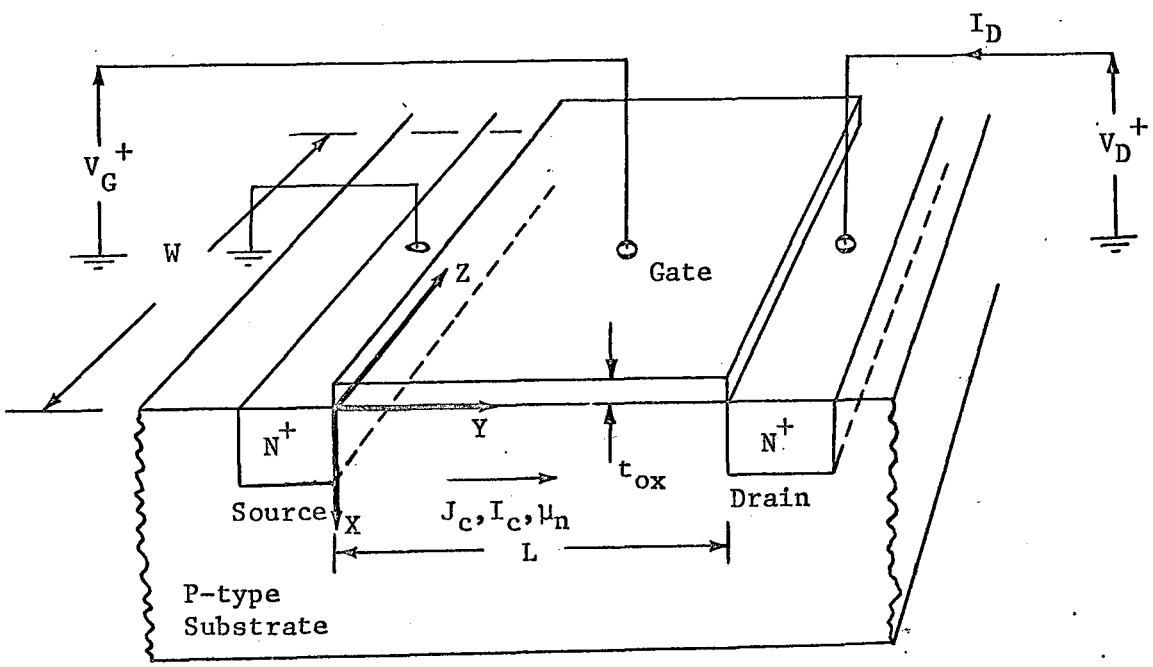


FIG. (1-1) DIAGRAMMATIC SKETCH OF A MOSFET SHOWING DIMENSIONS AND DIRECTIONS USED FOR ANALYSIS

By integrating the channel-current density over a cross section of the channel (Wdx) we obtain the current in Fig. 1-1 which can be written as:

$$I_c = W \int J_c\,(x,y)\,dx \qquad \ldots(1\text{-}1)$$

Where:

W = Channel width in the Z direction. W is perpendicular to the direction of current flow.

J_c = Channel current density.

From Ohm's Law:

$$J_c\,(x,y) = \sigma(x)\,E_y = q\,\mu_n\,n(x)\,E_y \qquad \ldots(1\text{-}2)$$

q = electronic charge

μ_n = electron mobility

n = number of electrons

E_y = electric field in y direction

$\sigma(x)$ = conductivity in x direction

Eq. (1-2) substituted in Eq. (1-1) gives:

$$I_c = W \int q\,\mu_n\,n(x)\,E_y\,dx$$

or
$$I_c = Wq\,\mu_n\,E_y \int n(x)\,dx \qquad \ldots(1\text{-}3)$$

Eq. (1-3) is true with the use of approximation (g) which was that μ_n is constant and independent of x.

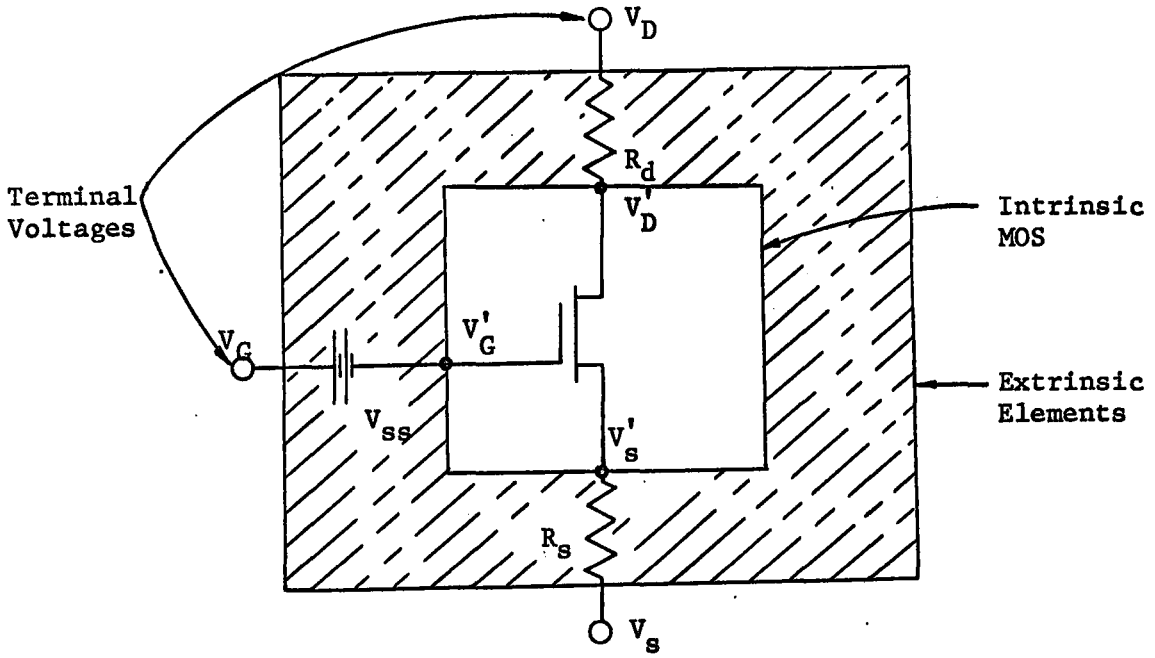


FIG. (1-2) DIAGRAM ILLUSTRATING THE INTRINSIC AND EXTRINSIC ELEMENTS OF A MOSFET

Now $E_y = -(dV/dy)$

So that equation (1-3) becomes:

$$- I_c = W\mu_n \frac{dV}{dy} q \int n(x)\, dx \qquad \ldots(1\text{-}4)$$

where $q \int n(x)dx$ represents the mobile charge per unit area in the channel.

The total MOS-system charge must be zero for a neutral system. Therefore:

$$Q_G + Q_{ss} + Q_C + Q_D = 0 \qquad \ldots(1\text{-}5)$$

Where:

Q_{ss} = Extrinsic charge due to approximation (f)

Q_G = Gate charge

Q_D = Charge in depletion region

Q_C = Channel charge

As shown in Fig. 1-2 $Q_{ss} + Q_G$ represents the charge outside the semiconductor material proper and $Q_C + Q_D$ represents all the charges within the semiconductor material.

Gauss' law can be used to relate the charge induced by the gate to the gate voltage in that:

$$\oint E_{0x}\, ds = \frac{Q_{total}}{\varepsilon_{0x}} \qquad \ldots(1\text{-}6)$$

The above integration of the E field over the gate or channel area gives the charge under that area, divided by the dielectric constant of the oxide. E_{0x} is considered at a given distance y (approximation h) and ds integrates to the differential gate area Wdy so that the relation between E and channel charge is:

$$\varepsilon_{0x}\, E_{0x}\, Wdy = Q_{total} \qquad \ldots(1\text{-}7)$$

E_{0x} is defined as $-\frac{dV_{0x}}{dx}$

Where dV_{0x} = voltage across the oxide

dx = incremental oxide thickness

Then $-\frac{dV_{0x}}{dx} \simeq -\frac{\Delta V_{0x}}{\Delta x}$

Where $\Delta x = + t_{0x}$

$\Delta V_{0x} = -(V_G - V(y))$

So that $$-\frac{dV_{ox}}{dx} = \frac{V_G - V(y)}{t_{ox}} \qquad \ldots(1\text{-}8)$$

Eq. (1-8) states that the voltage across the oxide is simply the gate voltage minus the voltage on the channel. The channel voltage will be a function of the distance in the y direction, ranging from V_D' at the drain to V_s' at the source.

Initially setting R_d and R_s to zero

$$V_D = V_D' \quad \text{and} \quad V_s' = V_s = 0$$

Combining equation (1-7) and (1-8) and letting $\frac{\varepsilon_{ox}}{t_{ox}} = C$ (capacitance per unit area)

$$Q_G = \left[V_G - V(y)\right]C \qquad \ldots(1\text{-}9)$$

Q_G = gate charge per unit area.

Substituting eq. (1-9) into eq. (1-5)

$$Q_C = -\left[V_G - V(y)\right]C - (Q_{ss} + Q_D) \qquad \ldots(1\text{-}10)$$

Equation (1-10) is the mathematical statement of the amount of charge contained in the channel per unit area. It is this charge that allows conduction between the source and drain.

Substitute eq. (1-10) in eq. (1-4) and remembering that

$$Q_C = q \int n\,(x)\,dx$$

Then

$$-I_c = W\mu_n \frac{dV}{dy} \left\{ -\left[V_G - V(y)\right] C - (Q_{ss} + Q_D) \right\}$$

This can also be written as

$$I_c\, dy = W\mu_n\, C\, dV \left\{ \left[V_G - V(y) \right] + \frac{Q_{ss} + Q_D}{C} \right\} \qquad \ldots(1\text{-}11)$$

Integrating between 0 and L for the length, and between 0 and V_D for the voltage:

$$I_c \int_0^L dy = W\mu_n\, C \left[V_G \int_0^{V_D} dV - \int_0^{V_D} V(y)\, dV + \frac{Q_{ss} + Q_D}{C} \int_0^{V_D} dV \right]$$

$$I_c L = W\mu_n\, C \left[V_G\, V_D - \frac{1}{2} V_D^2 + \frac{Q_{ss} + Q_D}{C}\, V_D \right]$$

$C_o = CWL$ = total capacitance under gate.

Then

$$I_c = -\frac{C_o \mu_n}{L^2} \left[- (V_G - V_{TH})\, V_D + \frac{1}{2} V_D^2 \right] \qquad \ldots(1\text{-}12)$$

Where

$$V_{TH} = - (Q_{ss} + Q_D)/C \qquad \ldots(1\text{-}12b)$$

= Threshold Voltage

Equation (1-12) can be written as:

$$I_c = \beta \left[- (V_G - V_{TH})\, V_D + \frac{1}{2} V_D^2 \right] \qquad \ldots(1\text{-}13)$$

Where

$$\beta = + \frac{W\varepsilon_{0x}\,\mu_n}{L\,t_{0x}}$$

$$= + \frac{WC\,\mu_n}{L}$$

$$= + \frac{C_o\,\mu_n}{L^2}$$

Channel current and drain current of Fig. 1-1 are related by the equation

$$I_c + I_D = 0$$

$$\therefore \quad I_D = + \beta\left[(V_G - V_{TH})\,V_D - \frac{1}{2}\,V_D^2\right] \qquad \ldots(1\text{-}14)$$

Equation (1-14) represents the drain current of a device in the triode region.

A second area of operation is called the saturation region. The saturation of the MOSFET or the leveling out of the drain current is associated with the pinching off of the channel near the drain. Once the channel has pinched off, the current is said to have saturated at a given level and is then, to a first approximation independent of drain voltage. Pinchoff occurs because the voltage across the oxide falls below a critical value. The channel IR drop is the factor causing the reduction in electric field. When E_{0x} is decreased to such a value that it cannot support sufficient mobile charge in a given portion of the channel, then that region decreases to approximately zero thickness

and is said to have been pinched off.

Examining Eq. (1-14) we find that for a small V_D the $(V_G-V_{TH})V_D$ term dominates. As V_D is increased the quadratic term becomes significant with the result that the rate of increase of the current falls off. At some drain voltage $|I_D|$ will reach a maximum. Past this point, the equation predicts a decrease. However, at the maximum current point, the device has reached saturation and the device model and equations change. To find the maximum of $|I_D|$ from Eq. (1-14) the expression is differentiated with respect to the drain voltage and set equal to zero. Solving the resulting expression yields:

$$V_D = V_G - V_{TH} \qquad \ldots(1\text{-}15)$$

Once saturation has been reached, the voltage drop across the inverted portion of the channel tends to remain fixed at $V_G - V_{TH}$ while V_D varies. To a first approximation, this constant voltage across a constant channel resistance results in a constant drain current. Once saturation has been reached, the output characteristic curves can be approximated by horizontal lines. The equation for the current in saturation can be found by substituting Eq. (1-15) in Eq. (1-14), which gives the relationship:

$$I_D = \frac{\beta}{2} (V_G - V_{TH})^2 \qquad \ldots(1\text{-}16)$$

Equation (1-16) shows a square law dependence of the drain current upon the gate voltage, and also indicates that the drain current is independent of the drain voltage.

Actual output characteristics of an N-channel MOS device (shown in Fig. 1-3) indicate that the drain current is not constant in the saturation region. The slope in saturation indicates a finite output resistance.

It was stated earlier that the voltage across the pinched-off channel tends to remain fixed at $V_G - V_{TH}$. Any difference in the drain potential and the voltage across the channel must be taken up across the depletion region at the surface, which is designated L'. The voltage supported by this region is $V_D - (V_G - V_{TH})$. As V_D increases, L' must also increase to absorb the additional voltage. L represents the effective channel length. L_T is the total channel length. Then $L = L_T - L'$. Increasing the drain voltage increases L' therefore decreasing L, the effective channel length. This decrease in length results in a drop in resistance. To keep a constant voltage of $V_G - V_{TH}$ across the channel, the drain current must increase to compensate for the decrease in channel resistance.

Equation (1-16) can be written as:

$$I_D = \frac{\beta}{2} (V_G - V_{TH})^2 \quad \frac{L_T}{L_T - L'} \qquad \ldots(1\text{-}17)$$

Where

$$L' = \sqrt{\frac{2\varepsilon_s \left[V_D - (V_G - V_{TH})\right]}{qN}}$$

N = Impurity density of the substrate

ε_s = Silicon dielectric constant

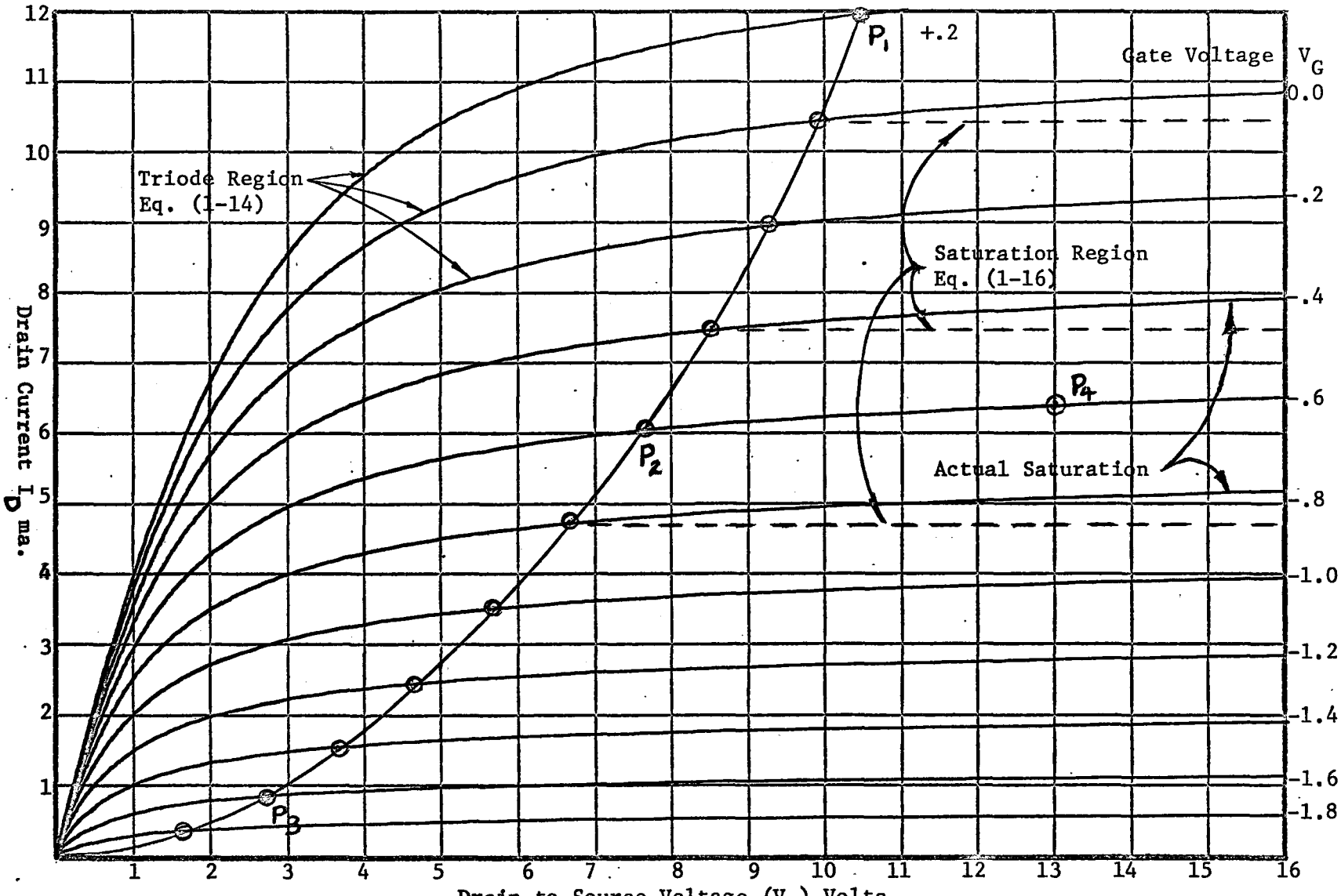


Fig. 1-3 Output Characteristics of a N-Channel MOSFET

Hofstein and Warfield[2] have shown that for the channel-length modulation, the output conductance is directly proportional to the drain current. This can be written as:

$$I_d = K g_{ds} \quad \text{or} \quad K = I_d \, r_d$$

Where

$$\frac{1}{r_d} = g_{ds}$$

The above conclusion is verified in Fig. 1-4 where g_{ds} is plotted as a function of I_d. This graph of measured data for the 3N143 device #II MOSFET shows that the drain conductance is in fact, a linear function of the drain current. A slight deviation occurs at low currents. Therefore one can conclude that for this device the dominant feedback mechanism is the channel-length modulation.

When electrostatic feedback dominates, Hofstein and Heiman[3] have shown that the drain conductance is directly proportional to the effective gate voltage $(V_G - V_{TH})$.

1.2 A MODEL FOR THE SINGLE GATE MOSFET

The symbolic circuit element which represents the MOSFET is shown in Fig. 1-5. The behaviour of the device in saturation is described by:

$$I_D^{\frac{1}{2}} = \sqrt{\beta/2} \; (V_{GS} - V_{TH}) \qquad \ldots(1\text{-}18)$$

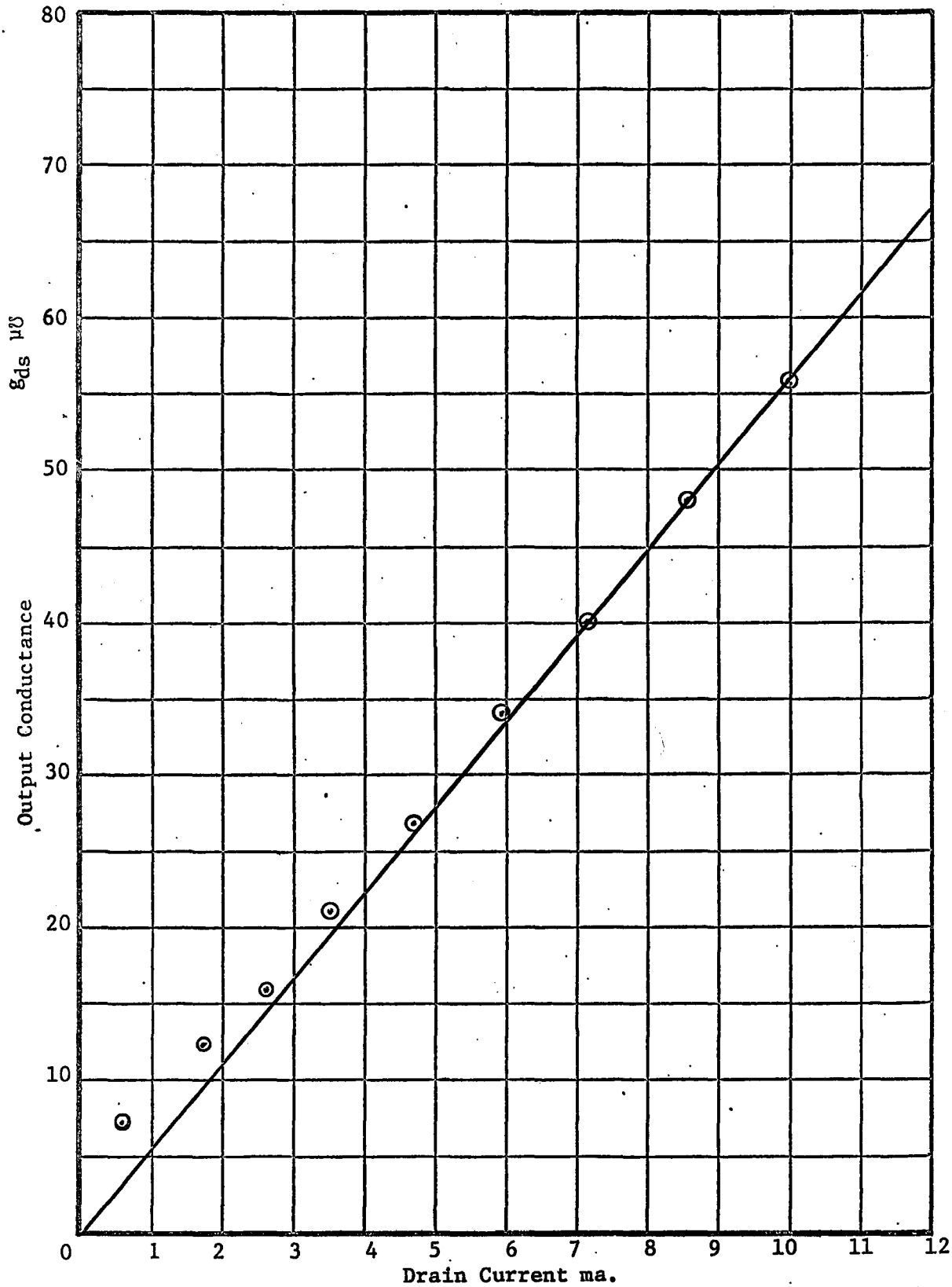


Fig. 1-4 Output Conductance vs. Drain Current for the 3N143 Device #II

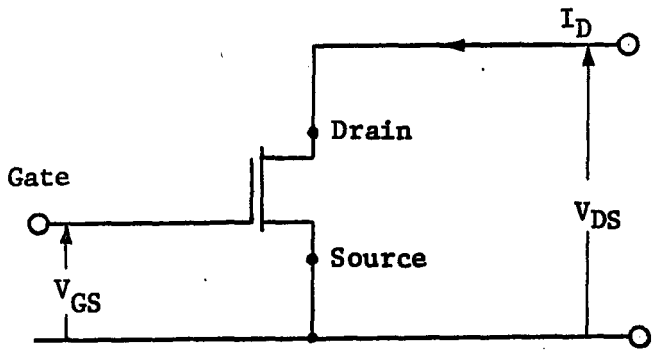


FIG. 1-5 MOSFET SYMBOLIC CIRCUIT ELEMENT

If $I_D^{\frac{1}{2}}$ vs $(V_{GS} - V_{TH})$ is plotted we obtain a straight line with the slope of $\sqrt{\beta/2}$. If the line is extended to $I_D = 0$, V_{TH} can be obtained as $V_{TH} = V_{GS}$ at this intercept.

A more complete representation of the MOSFET in saturation is shown in Fig. 1-6.

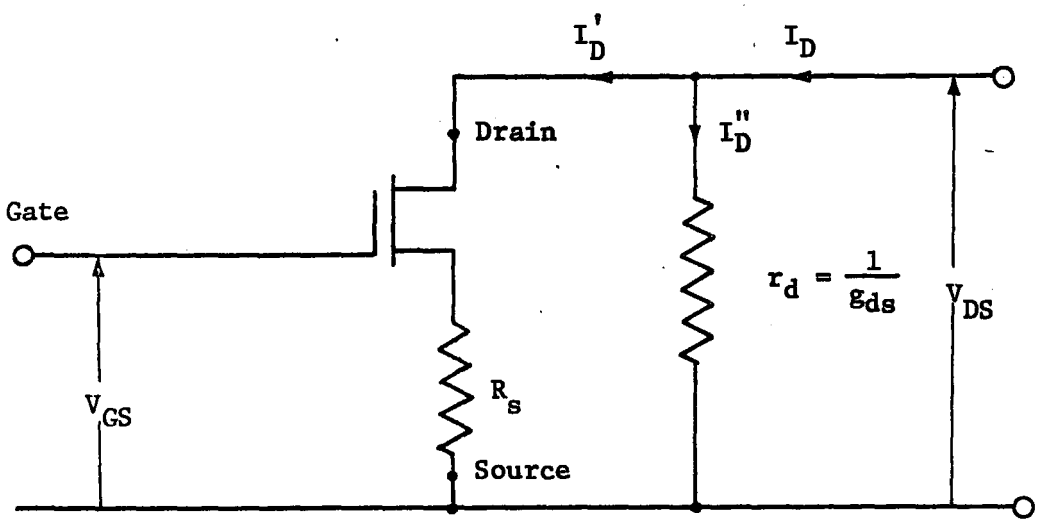


FIG. 1-6 A MORE COMPLETE REPRESENTATION OF MOSFET IN SATURATION

R_s in Fig. 1-6 represents the extrinsic source resistance (also shown in Fig. 1-2). R_s is the total unmodulated source resistance which consists of contact resistance, and unmodulated source channel resistance. The new gate voltage, including the feedback resistance R_s then is:

$$V_{GS} = V_{GS}' - I_D' R_s \qquad \ldots(1\text{-}19)$$

Substituting Eq. (1-19) into Eq. (1-18) we have:

$$I_D'^{\frac{1}{2}} = \sqrt{\beta/2}\ (V_{GS}' - I_D' R_s - V_{TH}) \qquad \ldots(1\text{-}20)$$

Equation (1-20) is no longer a straight line when $I_D^{\frac{1}{2}}$ vs V_{GS}' is plotted. A plot of $(I_D')^{\frac{1}{2}}$ vs V_{GS}' for the 3N143 device #II is found on Fig. 1-7. By taking the current values at the beginning of saturation as shown in Fig. 1-3 $I_D'' = 0$. Therefore $I_D = I_D'$.

Since the bending away from the ideal straight line relationship of Eq. (1-18) is caused by the $I_D R_s$ term in Eq. (1-20), R_s can be found by curve fitting.

There is also a deviation from the ideal square law relationship of Eq. (1-18) at very low currents. The deviation[6] is possibly a result of surface traps immobilizing the few electrons drawn from the P-type bulk towards the silicon-insulator interface. This is an effective reduction of the mobility of all the electrons in the channel region compared to the normal drift mobility. Since it was assumed that the mobility is constant (approximation g) this region of the MOS device must not be used

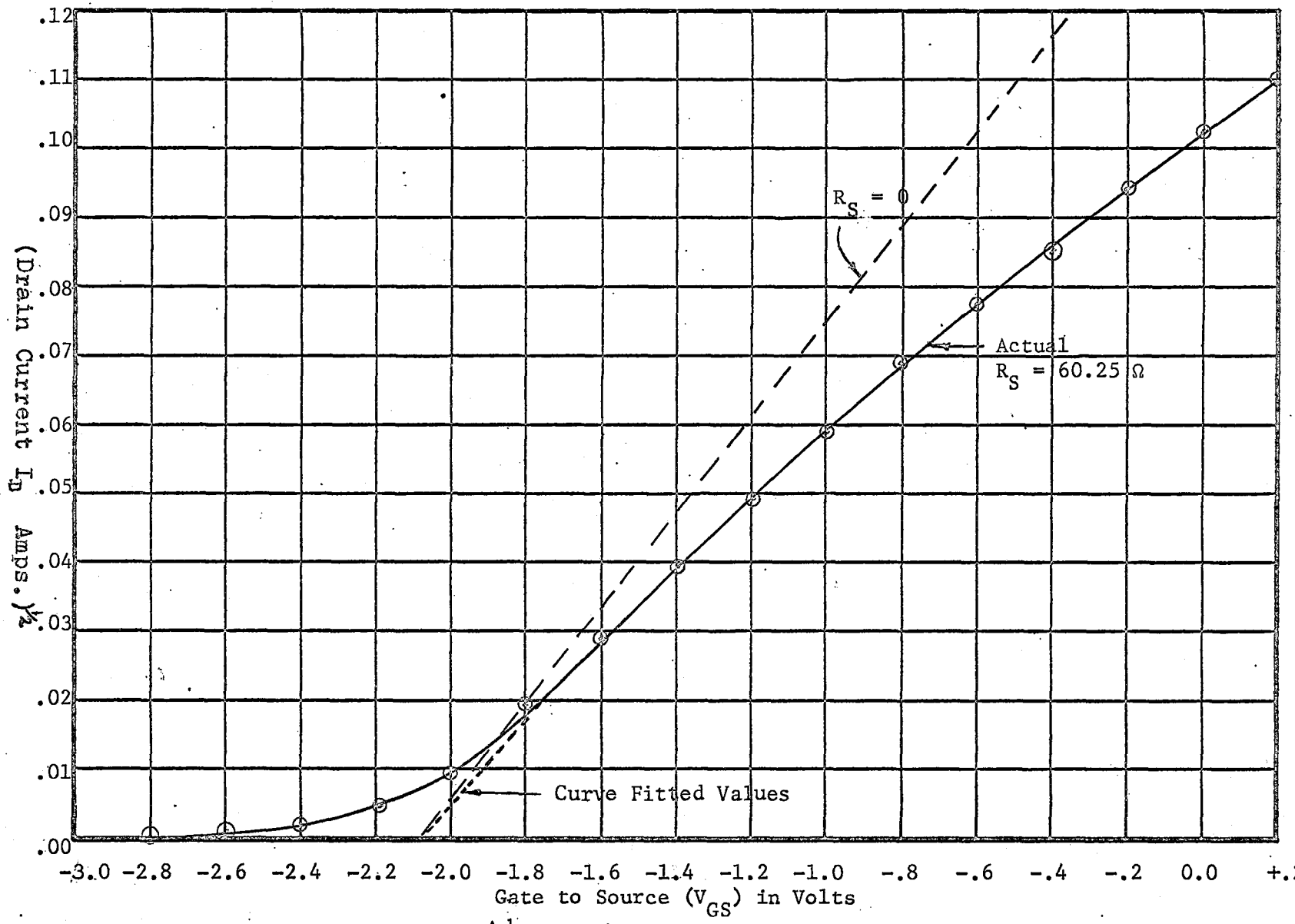


Fig. 1-7 $I_D'^{1/2}$ vs. V_{GS}' plot for the 3N143 Device #II

when obtaining parameters by curve fitting. For the device characterized in Fig. 1-7 this deviation becomes noticeable at $\sqrt{I_{DS}} = .01$ or a current of $I_{DS} = .1ma$. Since the device is normally operated in the 1.0 to 50ma region, the above should only become a restriction in a very few special cases.

The many parameters that have to be found in the dual gate MOSFET make it necessary to resort to curve fitting to solve for the unknown device characteristics. A computer program using specified experimental points will be used to solve for the unknown parameters. Since the dual gate MOSFET is essentially two single gate devices in series the single gate FET program will be discussed first.

Eq. (1-18) being a straight line can easily be solved by using two experimental points for an ideal device. Since a series resistance, R_S, is present in most real devices we have to use Eq. (1-20). This additional term now makes it necessary to use three experimental points to solve the saturation equation.

By taking the three points P_1, P_2, and P_3 marked on Fig. 1-3 we have the following table of values.

POINT NUMBER	GATE VOLTAGE	DRAIN CURRENT
P_1	$V_{GS1} = 0.2$ Volts	$I_{D1} = 11.95$ ma
P_2	$V_{GS2} = -.6$ Volts	$I_{D2} = 6.1$ ma
P_3	$V_{GS3} = -1.6$ Volts	$I_{D3} = 0.91$ ma

By solving Eq. (1-20) V_{TH}, R_s, and β can be found as follows:

Eq. (1-20) can be written as:

$$\sqrt{\beta/2} = \frac{I_D^{\frac{1}{2}}}{V_{GS} - I_D R_s - V_{TH}}$$

By substituting the three points we obtain:

$$\frac{I_{D1}^{\frac{1}{2}}}{V_{GS1} - I_{D1}R_s - V_{TH}} = \frac{I_{D2}^{\frac{1}{2}}}{V_{GS2} - I_{D2}R_s - V_{TH}} = \frac{I_{D3}^{\frac{1}{2}}}{V_{GS3} - I_{D3}R_s - V_{TH}}$$

Cross multiplying and rearranging we have:

$$R_s(I_{D2}^{\frac{1}{2}} I_{D1} - I_{D1}^{\frac{1}{2}} I_{D2}) = V_{TH}(I_{D1}^{\frac{1}{2}} - I_{D2}^{\frac{1}{2}}) - V_{GS2} I_{D1}^{\frac{1}{2}} + V_{GS1} I_{D2}^{\frac{1}{2}} \quad \ldots(1\text{-}21)$$

Similarly:

$$R_s(I_{D3}^{\frac{1}{2}} I_{D1} - I_{D1}^{\frac{1}{2}} I_{D3}) = V_{TH}(I_{D1}^{\frac{1}{2}} - I_{D3}^{\frac{1}{2}}) - V_{GS3} I_{D1}^{\frac{1}{2}} + V_{GS1} I_{D3}^{\frac{1}{2}} \quad \ldots(1\text{-}22)$$

Dividing Eq. (1-21) into Eq. (1-22) eliminates R_s and gives us:

$$\frac{I_{D3}^{\frac{1}{2}} I_{D1} - I_{D1}^{\frac{1}{2}} I_{D3}}{I_{D2}^{\frac{1}{2}} I_{D1} - I_{D1}^{\frac{1}{2}} I_{D2}} = \frac{V_{TH}(I_{D1}^{\frac{1}{2}} - I_{D3}^{\frac{1}{2}}) - V_{GS3} I_{D1}^{\frac{1}{2}} + V_{GS1} I_{D3}^{\frac{1}{2}}}{V_{TH}(I_{D1}^{\frac{1}{2}} - I_{D2}^{\frac{1}{2}}) - V_{GS2} I_{D1}^{\frac{1}{2}} + V_{GS1} I_{D2}^{\frac{1}{2}}} \quad \ldots(1\text{-}23)$$

Introducing F where:

$$F = \frac{I_{D3}^{\frac{1}{2}} I_{D1} - I_{D1}^{\frac{1}{2}} I_{D3}}{I_{D2}^{\frac{1}{2}} I_{D1} - I_{D1}^{\frac{1}{2}} I_{D2}} \quad \ldots(1\text{-}24)$$

Substituting F in Eq. (1-23) and rearranging we have:

$$FV_{TH}(I_{D1}^{\frac{1}{2}} - I_{D2}^{\frac{1}{2}}) + F(V_{GS1}I_{D2}^{\frac{1}{2}} - V_{GS2}I_{D1}^{\frac{1}{2}}) = V_{TH}(I_{D1}^{\frac{1}{2}} - I_{D3}^{\frac{1}{2}}) + V_{GS1}I_{D3}^{\frac{1}{2}} - V_{GS3}I_{D1}^{\frac{1}{2}}$$

Therefore:

$$V_{TH} = \frac{V_{GS1}(I_{D3}^{\frac{1}{2}} - FI_{D2}^{\frac{1}{2}}) + I_{D1}^{\frac{1}{2}}(V_{GS2} - V_{GS3})}{I_{D1}^{\frac{1}{2}}(F-1) - I_{D2}^{\frac{1}{2}}F + I_{D3}^{\frac{1}{2}}} \qquad \ldots(1\text{-}25)$$

Solving equation (1-21)

$$R_s = \frac{V_{TH}(I_{D1}^{\frac{1}{2}} - I_{D2}^{\frac{1}{2}}) - V_{GS2}I_{D1}^{\frac{1}{2}} + V_{GS1}I_{D2}^{\frac{1}{2}}}{I_{D2}^{\frac{1}{2}}I_{D1} - I_{D1}^{\frac{1}{2}}I_{D2}} \qquad \ldots(1\text{-}26)$$

Therefore:

$$\beta = \frac{2I_{D1}}{(V_{GS1} - R_s I_{D1} - V_{TH})^2} \qquad \ldots(1\text{-}27)$$

Using the values shown for P_1, P_2, and P_3 it was found that:

V_{TH} = -2.087 Volts

R_s = 60.25 Ω

β = .00973 A/V^2

The broken line on Fig. 1-7 represents Eq. (1-18); i.e. $R_s = 0$.

As stated before, the output conductance of a MOSFET is directly proportional to the saturation current. To find the output conductance at a certain gate voltage we only have to find the slope of the saturation current vs drain voltage line at that V_{GS}.

For example in Fig. 1-3 points P_2 and P_4 can be used to obtain the following table.

POINT	DRAIN CURRENT	DRAIN TO SOURCE VOLTAGE	GATE VOLTAGE
P_2	I_{D2} = 6.1 ma	V_{DS2} = 7.7 volts	-.6 volts
P_4	I_{D4} = 6.3 ma	V_{DS4} = 13 volts	-.6 volts

The slope then is:

$$m = g_{ds} = \frac{I_{D4} - I_{D2}}{V_{DS4} - V_{DS2}} \qquad \ldots(1\text{-}28)$$

$$= \frac{(6.3 - 6.1)\ 10^{-3}}{13 - 7.7} = 37.8 \times 10^{-6} \mho$$

As stated before $I_d = K\ g_{ds}$. For the 3N143 device #II this is then:

$$K = \frac{I_{D2}}{g_{ds}} = \frac{I_{D2}\ (V_{DS2} - V_{DS2})}{I_{D4} - I_{D2}} \qquad \ldots(1\text{-}29)$$

$$= \frac{6.1 \times 10^{-3}}{37.8 \times 10} = 161.6$$

To complete our model of the single gate MOSFET we need two more parameters for the triode region of operation. These are ϕ and R_D.

$$\phi = + \frac{T_{ox}}{\varepsilon_{oxide}} \sqrt{2N_A\ q\ \varepsilon_{silicon}} \qquad \ldots(1\text{-}30)$$

R_D = The parasitic resistance in series with the drain connection.

In Eq. (1-14) the $\frac{1}{2}V_D^2$ term bends down the I-V characteristics away from the linearity of the resistance line for increasing drain-to-source voltage. Near pinch-off but still in the triode region, another term is added to Eq. (1-14) to bend the drain-to-source I-V characteristics down even further.[4] At conditions slightly below pinch-off Eq. (1-14) becomes:

$$I_D = \beta V_D \left[V_G - V_{TH} - I_D R_s - \tfrac{1}{2}V_D - \tfrac{2}{3} \phi \sqrt{V_D} \right] \qquad \ldots(1\text{-}31)$$

Crimping of the I-V characteristics at higher gate fields is caused by two mechanisms. These are the parasitic resistance and the field-dependent channel mobility. Which of these two major mechanisms dominates usually depends on the design of the particular device. J. Mize[5] and others have concluded that the field dependent mobility causes the crimping at higher gate fields, while Hofstein and Warfield have de-emphasized the effect of the mobility and have indicated the parasitic resistance as responsible. However, if we are content to propose a model that will explain crimping, the effect of the mobility variation can be incorporated into an effective series resistance.[6] The model could have this series resistance placed in the drain or in the source circuit, or it could have two resistors, one in each. For our purpose we will use the two resistor model.

The actual voltage across the ideal device V_D is then

$V_D = V - I_D (R_s + R_D)$. where V = applied voltage.

Therefore, Eq. (1-31) becomes:

$$I_D = \beta\left[V - I_D\,(R_s + R_D)\right]\left\{V_G - V_{TH} - I_D\,R_s - \tfrac{1}{2}\left[V - I_D\,(R_s + R_D)\right] - \frac{2}{3}\,\phi\sqrt{V - I_D\,(R_s + R_D)}\right\} \qquad \ldots(1\text{-}32a)$$

R_D can be found by curve fitting by using the variable resistance region of the MOSFET. This is when $|V_D| << |V_G - V_{TH} - I_D R_s|$. In this region equation (1-32) reduces to:

$$I_D = \beta\left[V - I_D\,(R_s + R_D)\right]\,(V_G - V_{TH}) \qquad \ldots(1\text{-}32b)$$

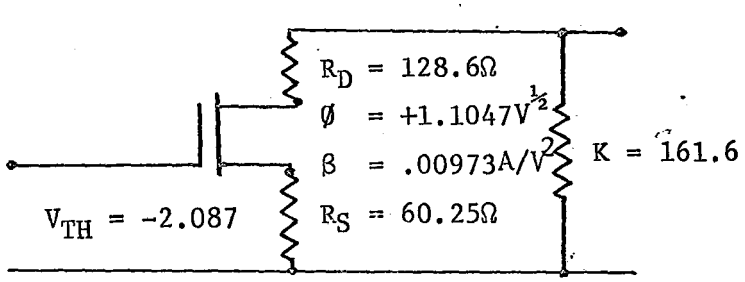
Which gives:

$$R_D = \frac{V}{I_D} - \frac{1}{\beta(V_G - V_{TH})} - R_s \qquad \ldots(1\text{-}33)$$

The only unknown quantity in Eq. (1-32a) is ϕ. By taking a point in the triode region but near saturation we can solve Eq. (1-32a) to give:

$$\phi = \frac{3\left[V_G - V_P - \tfrac{1}{2}(R_s - R_D)I_D - \tfrac{1}{2}V - \dfrac{I_D}{\beta(V - I_D(R_s + R_D))}\right]}{2\sqrt{V - I_D\,(R_s + R_D)}} \qquad \ldots(1\text{-}34)$$

The model obtained by using the curve fitting technique for the 3N143 device #II is:



A computer program was written to generate the V-I curves for the above model. Results will be discussed in chapter #5.

Dov Frohman-Bentchkowsky and Leslie Vadasz[7] have developed a computer simulation based on an analytical device model for MOS integrated circuits. However, their circuit characterization is done in terms of device physical parameters, i.e., oxide thickness, substrate impurity concentration, device geometry, and their statistical variation. Since in the majority of cases this type of information is not available to a person who is designing a mixer circuit solving the circuit entirely from measured results still seems like a more realistic approach.

CHAPTER II

2.1 A MODEL FOR THE DUAL-GATE MOSFET

The dual-gate MOSFET used belongs to RCA's series of field effect transistors. The RCA dual-gate devices all feature the same series arrangement of two separate channels, each having an independent control gate.[8] A schematic representation of one such device is shown in Fig. 2-1.

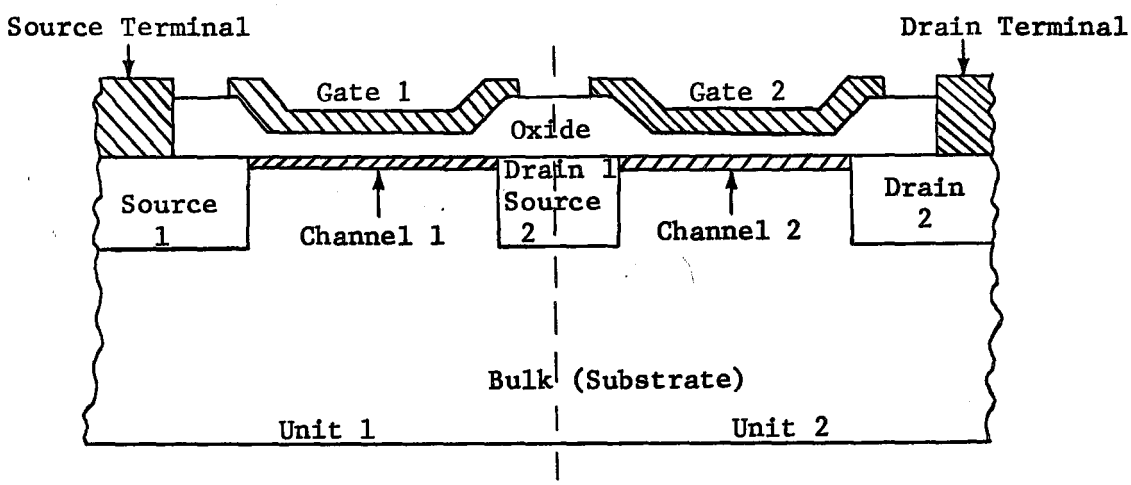


FIG. 2-1 SCHEMATIC REPRESENTATION OF A RCA DUAL-GATE MOS FIELD-EFFECT TRANSISTOR

The main difficulty in finding the parameters of the dual-gate MOSFET is that the middle point, the region between the gates, (point A on Fig. 2-3a) is not accessible. If this point were available as an external lead, the dual-gate model would easily be found by applying the techniques of Chapter I to each half of the device in turn.

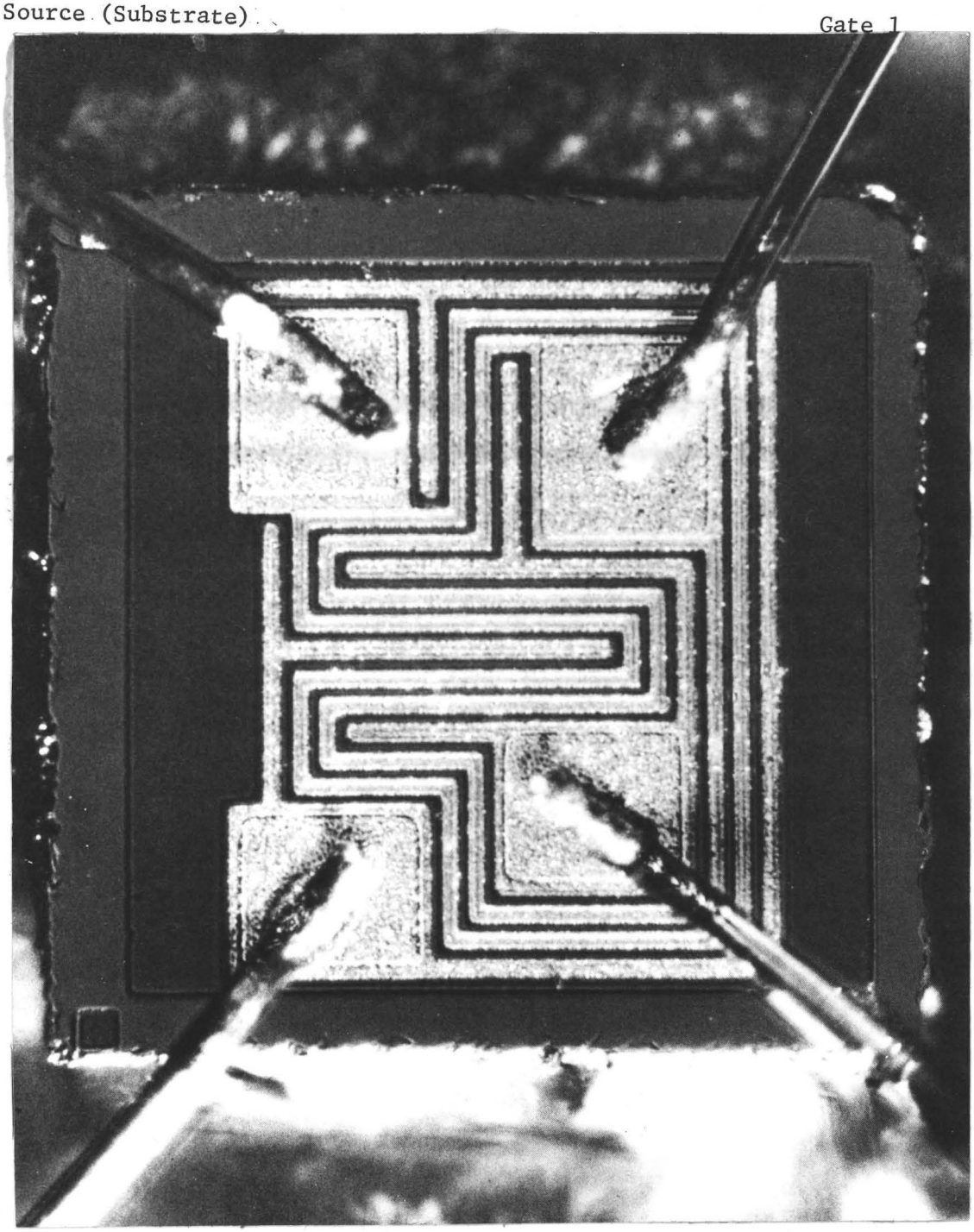


Fig. 2-2 Dual Gate MOSFET Chip with Attached Leads.

The methods developed to overcome the above difficulty were checked against two single gate FET's connected in series as shown in Fig. 2-3b. The results found by not using lead B in Fig. 2-3b and those found by measuring each device separately, as outlined in chapter I, compared favourably. These results and others will be discussed further in chapter V.

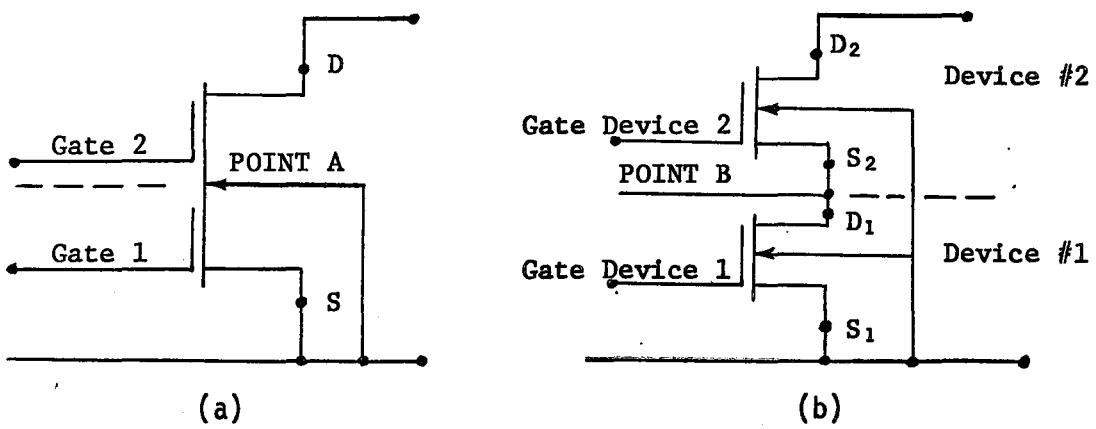


FIG. 2-3 (a) DUAL-GATE MOSFET SYMBOL

(b) TWO SINGLE GATE MOSFET'S IN SERIES TO SIMULATE DUAL-GATE MOSFET

2.2 CURVE FITTING TO OBTAIN THE PARAMETERS OF THE DUAL-GATE MOSFET

To obtain the first three parameters of the dual-gate MOSFET the device is connected as shown in Fig. 2-4. This results in the set of curves shown in Fig. 2-5 for the RCA 3N141 FET used. The particular device used in this part of the discussion shall be referred to as device A.

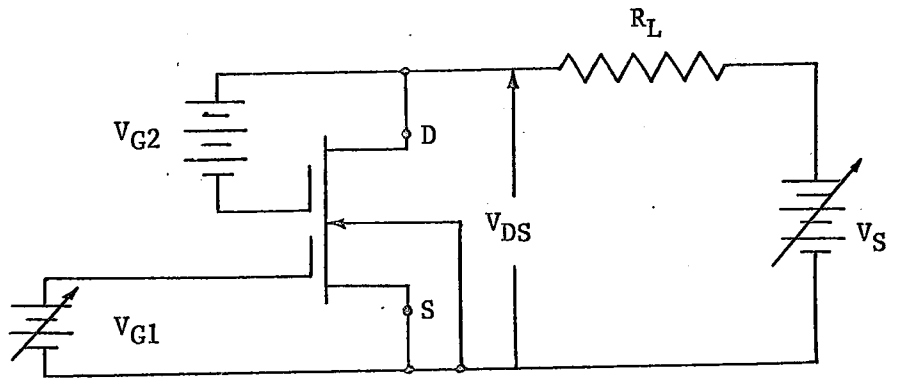


FIG. 2-4 CIRCUIT CONNECTION USED TO GET FIRST THREE PARAMETERS

In the connection shown in Fig. 2-4 the top gate is turned hard on to minimize the voltage drop across the top portion of FET channel. Any voltage drop developed only turns the device on even harder. The bottom part of the device now can be analyzed as a single gate FET as long as we only look at the saturation region. This is possible because in the saturation region the device operates independently of the magnitude of the supply voltage.

This section then is completely analogous to section 1-2. Again using three points at the onset of saturation, (P_1, P_2, and P_3 as shown in Fig. 2-5) we obtain the same equations as in chapter I. Since the device parameters being found belong to the bottom section we replace:

V_{TH} with V_{TH1} in equations (1-25), (1-26), and (1-27)

R_S with R_{S1} in equations (1-26), (1-27)

β with β_1 in equation (1-27)

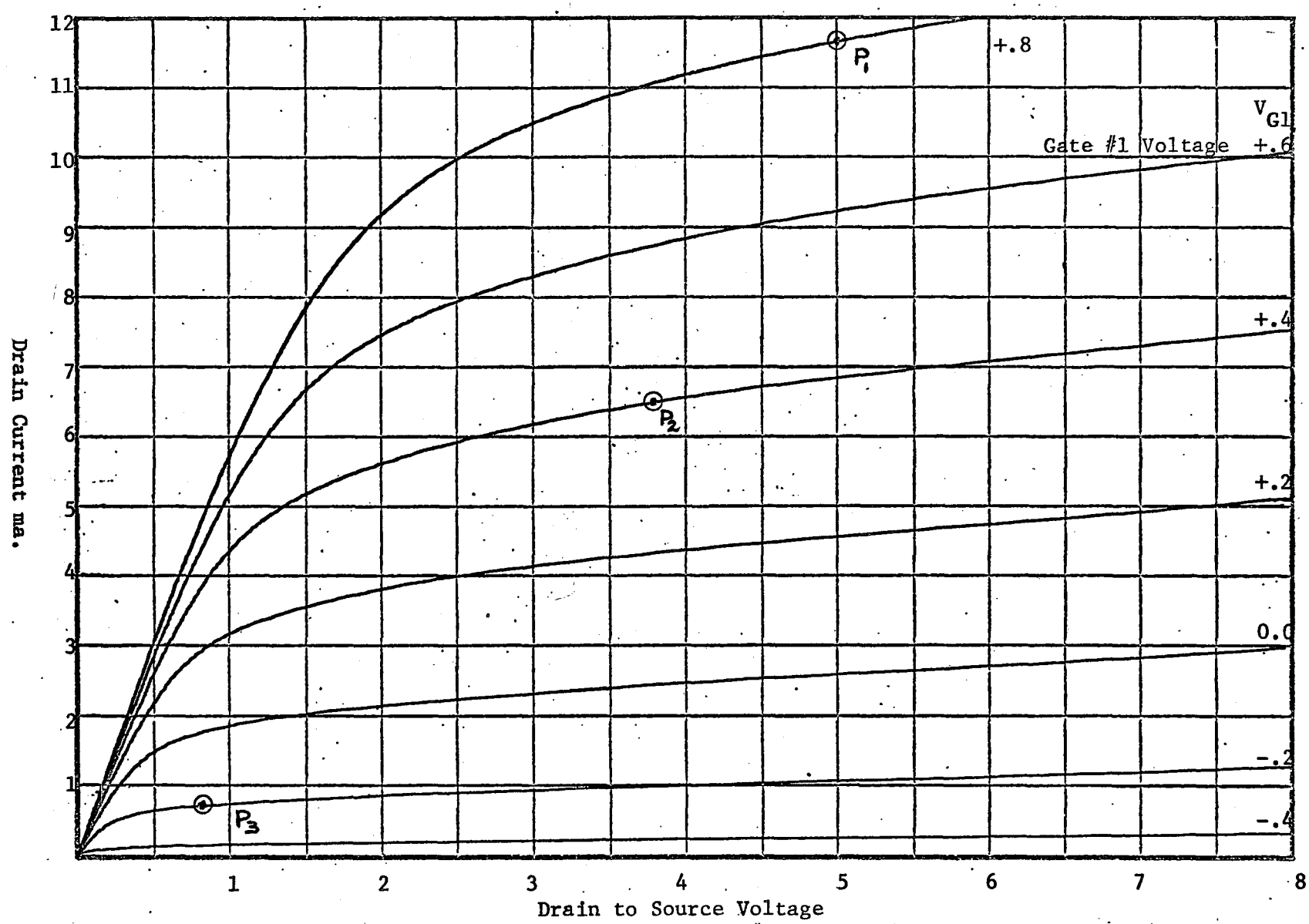


Fig. 2-5 I-V Characteristics with Device #A Connected as Shown in Fig. 2-4.

Next we shall again, as in Chapter I, go to the linear region where $|V_D| << |V_G - V_{TH}|$. Only this time we will use three points so that V_{TH2}, β_2 and R_T can be solved for. If we were to do an exact model using two field-effect devices, we would need R_{S1}, R_{D1}, R_{S2} and R_{D2}, as shown in Fig. 2-6. Since we cannot determine a point between R_{D1}, R_{S2} (which would be completely arbitrary anyway) we shall set R_{D1} to zero. Therefore the value of R_{S2} used will represent the total parasitic resistance between the drain of the lower part of the device and the source of the upper part of the FET. R_T is the sum of all the parasitic resistances.

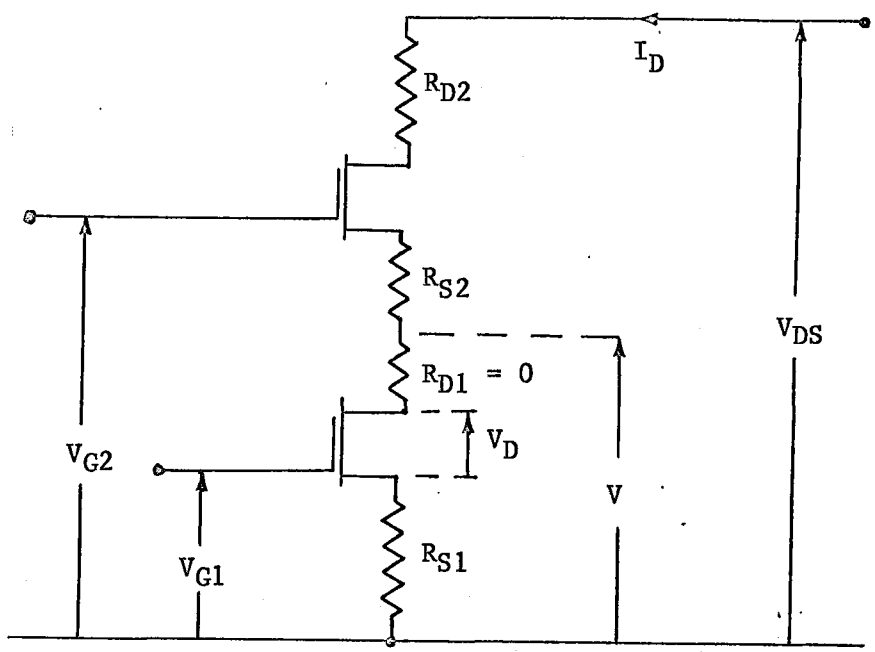


FIG. 2-6 THE CIRCUIT USED TO REPRESENT THE LINEAR REGION OF THE DUAL-GATE MOSFET

In Fig. 2-6 as shown in Eq. (1-32b)

$$I_D = \beta_1 \ (V - I_D R_{S1}) \ (V_{G1} - V_{TH1}) \qquad \ldots(2\text{-}1)$$

For $\quad |V| << |V_{G1} - V_{TH1} - I_D R_S|$

Equation 2-1 can be rewritten as:

$$V = I_D \left[\frac{1}{\beta_1 (V_{G1} - V_{TH1})} + R_{S1} \right] \qquad \ldots(2\text{-}2)$$

Also in Fig. 2-6:

$$I_D = \beta_2 \left[V_{DS} - I_D (R_{S2} + R_{D2}) - V \right] (V_{GS2} - V_{TH2} - I_D R_{S2} - V) \qquad \ldots(2\text{-}3)$$

For $\quad |V_{DS}| << |V_{G2} - V_{TH2}| \qquad \ldots(2\text{-}4)$

Where $V_{DS} - I_D(R_{S2} + R_{D2}) - V$ is the voltage across the top ideal device. The actual voltage being applied to the gate of the top part of the device being:

$$V_{G2}' = V_{G2} - I_D R_{S2} - V$$

If Eq. 2-4 is true then:

$$I_D R_{S2} << V_{G2} - V_{TH2}$$

and $\quad V << V_{G2} - V_{TH2}$

Therefore by substituting Eq. 2-2 in Eq. 2-3 we obtain:

$$I_D = \beta_2 \left[V_{DS} - I_D \left(R_{S1} + R_{S2} + \frac{1}{\beta_1 (V_{G1} - V_{TH1})} + R_{D2} \right) \right] (V_{G2} - V_{TH2})$$

Then:

$$R_T = R_{S1} + R_{S2} + R_{D2}$$

$$= \frac{V_{DS}}{I_D} - \frac{1}{\beta_1(V_{G1} - V_{TH1})} - \frac{1}{\beta_2(V_{G2} - V_{TH2})} \quad \ldots(2\text{-}5)$$

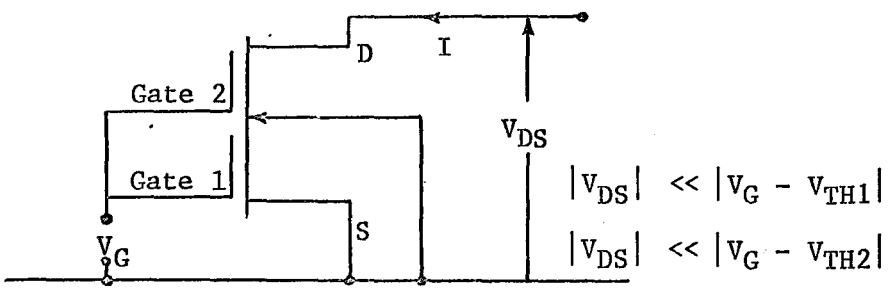


FIG. 2-7 CONNECTION FOR OBTAINING LINEAR CHARACTERISTICS SHOWN IN FIGURE 2-8

The linear V-I curves shown in Fig. 2-8 were obtained by connecting device #A as shown in Fig. 2-7. Using the three points shown on Fig. 2-8 (P_4, P_5, and P_6) we can solve for R_T, V_{TH2} and β_2. The resulting table of values is shown below.

POINT	DRAIN CURRENT	DRAIN TO SOURCE VOLTAGE	GATE VOLTAGE
P_4	I_{D4} = 0.3 ma	V_{DS4} = .05 Volts	V_{G1}' = 1.0 Volts V_{G2}' = 1.0 Volts
P_5	I_{D5} = 0.2 ma	V_{DS5} = .05 Volts	V_{G1}'' = 0.2 Volts V_{G2}'' = 0.2 Volts
P_6	I_{D6} = 0.15 ma	V_{DS6} = .07 Volts	V_{G1}'' = -0.2 Volts V_{G2}'' = -0.2 Volts

Equation 2-5 can be rewritten as:

$$\frac{V_{DS}}{I} - \frac{1}{\beta_1(V_{G1} - V_{TH})} = R_T + \frac{1}{\beta_2(V_{G2} - V_{TH2})} \quad \ldots(2\text{-}6)$$

Substituting P_4 in Eq. 2-6 we have

$$\frac{V_{DS4}}{I_{D4}} - \frac{1}{\beta_1(V_{G1}' - V_{TH_1})} = R_T + \frac{1}{\beta_2(V_{G2}' - V_{TH2})} \quad \ldots(2\text{-}7)$$

This can be written as:

$$A = R_T + \frac{1}{\beta_2(V_{G2}' - V_{TH2})} \quad \ldots(2\text{-}8)$$

where

$$A = \frac{V_{DS4}}{I_{D4}} - \frac{1}{\beta_1(V_{G1}' - V_{TH1})} \quad \ldots(2\text{-}9)$$

Note that A contains all known values and can therefore be treated as a constant. Similarly, substituting P_5 and P_6 into Eq. 2-6 we end up with:

$$B = R_T + \frac{1}{\beta_2(V_{G2}'' - V_{TH2})} \quad \ldots(2\text{-}10)$$

$$C = R_T + \frac{1}{\beta_2(V_{G2}''' - V_{TH2})} \quad \ldots(2\text{-}11)$$

where

$$B = \frac{V_{DS5}}{I_{D5}} - \frac{1}{\beta_1(V_{G1}'' - V_{TH1})} \quad \ldots(2\text{-}12)$$

$$C = \frac{V_{DS6}}{I_{D6}} - \frac{1}{\beta_1(V_{G1}''' - V_{TH1})} \quad \ldots(2\text{-}13)$$

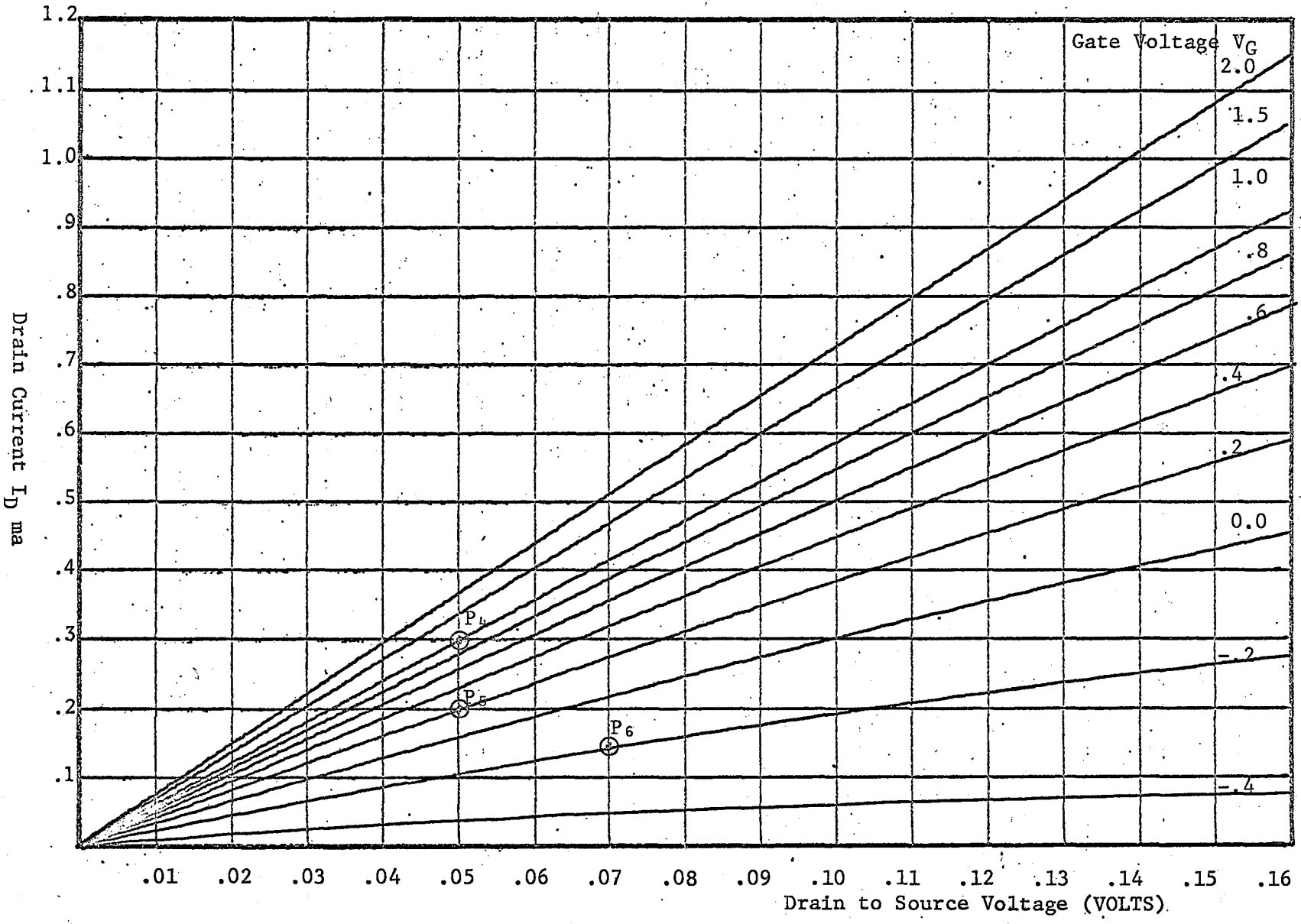


Fig. 2-8 Linear Region of the Static MOSFET Characteristics

Equations 2-8, 2-10, and 2-11 contain only three unknowns: R_T, V_{TH2} and β_2.

β_2 can be eliminated by taking R_T across the equal sign and dividing Eq. (2-8) by equations (2-10) and (2-11).

Then:

$$\frac{A - R_T}{B - R_T} = \frac{V''_{G2} - V_{TH2}}{V'_{G2} - V_{TH2}} \qquad \ldots(2\text{-}14)$$

And:

$$\frac{A - R_T}{C - R_T} = \frac{V'''_{G2} - V_{TH2}}{V'_{G2} - V_{TH2}} \qquad \ldots(2\text{-}15)$$

Solving Eq. 2-14 for V_{TH2} we obtain:

$$V_{TH2} = \frac{R_T\,(V''_{G2} - V'_{G2}) + A\,V'_{G2} - B\,V''_{G2}}{A - B} \qquad \ldots(2\text{-}16)$$

Similarly solving Eq. 2-15 for V_{TH2} results in:

$$V_{TH2} = \frac{R_T\,(V'''_{G2} - V'_{G2}) + A\,V'_{G2} - C\,V'''_{G2}}{A - C} \qquad \ldots(2\text{-}17)$$

Eliminating V_{TH2} in Eq. 2-16 and 2-17 and solving for R_T gives us:

$$R_T = \frac{(A\text{-}B)\,(A\,V'_{G2} - C\,V'''_{G2}) - (A\text{-}C)\,(A\,V'_{G2} - B\,V''_{G2})}{(A\text{-}B)\,(V'_{G2} - V'''_{G2}) - (A\text{-}C)\,(V'_{G2} - V''_{G2})} \qquad \ldots(2\text{-}18)$$

To solve for V_{TH2} we can then use either Eq. 2-16 or 2-17 as R_T is now known. Similarly we can then use Eq. 2-8, 2-10 or 2-11 to solve for β_2.

To find $\emptyset_1$ we only have to modify Eq. (1-31) of chapter I. The equation was:

$$I_D = \beta V_D (V_G - V_{TH} - I_D R_s - \tfrac{1}{2}V_D - \tfrac{2}{3}\emptyset\sqrt{V_D})$$

where V_D was the voltage across the ideal device

$$V_D = V - I_D (R_s + R_D)$$

For the dual-gate MOSFET Eq. (1-31) becomes:

$$I_D = \beta_1 V_D (V_{G1} - V_{TH1} - I_D R_{S1} - \tfrac{1}{2}V_D - \tfrac{2}{3}\emptyset_1\sqrt{V_D}) \quad ...(2\text{-}19)$$

But V_D changes to:

$$V_D = V_{DS} - (V_{DS} - V) - I_D R_{S1} \quad ...(2\text{-}20)$$

If we use the I-V curves generated by the connection shown in Fig. 2-4 and choose a point just before saturation, P_7, we can solve for $\emptyset_1$. The top portion of the device will still be in the linear region of operation, especially if we use a point with a moderate I_D. This assumption was verified using two discrete devices in series. $V_{DS} - V$ in equation (2-20) can then be replaced by:

$$V_{DS} - V = I_D \left[\frac{1}{\beta_2(V_{G2} + I_D R_{D2} + V_{DS} - V - V_{TH2})} + R_{S2} + R_{D2}\right]$$

But

$$V_{G2} - V_{TH2} >> I_D R_{D2} + V_{DS} - V$$

Therefore:

$$V_{DS} - V \simeq I_D \left[\frac{1}{\beta_2 (V_{G2} - V_{TH2})} + R_{S2} + R_{D2} \right] \qquad \ldots(2\text{-}21)$$

Substituting Eq. 2-21 into Eq. 2-20 results in:

$$V_D \simeq V_{DS} - I_D \left(R_{S1} + R_{S2} + R_{D2} + \frac{1}{\beta (V_{G2} - V_{TH2})} \right) \qquad \ldots(2\text{-}22)$$

Also Eq. (2-19) can be rewritten as:

$$\phi_1 = \frac{1.5}{\sqrt{V_D}} \left(V_{G1} - I_D R_{S1} - V_{TH1} - \tfrac{1}{2} V_D - \frac{I_D}{\beta_1 V_D} \right) \qquad \ldots(2\text{-}23)$$

Where

$$V_D \simeq V_{DS} - I_D \left(R_T + \frac{1}{\beta_2 (V_{G2} - V_{TH2})} \right) \qquad \ldots(2\text{-}23a)$$

At this point another operating region restriction will be made. In the model to be developed the top portion of the device will always operate in the saturation mode. The above restriction is fulfilled by choosing a proper bias point for each of the two gates, the correct supply voltage and the appropriate value for the load resistance. Actually, it is found that as long as the voltage across the device never drops below 3 volts, the top portion of the device will stay in the saturation region unless an unusually large voltage is applied to gate #2. This point will be discussed further in chapter IV.

It would now seem that the only unknowns in our model are R_{S2} and R_{D2}. Since we already know R_{S1} and R_T where $R_T = R_{S1} + R_{S2} + R_{D2}$ we only have to find R_{S2} or R_{D2}.

The above would be true if we could forget about the effect of substrate biasing. Through experimental examination of two single gate devices connected in series, as shown in Fig. 2-10 and Fig. 2-11 it was found that a substrate correction has to be made in the top device.

In single gate devices the substrate is commonly used as a second gate, as shown in Fig. 2-9(a). These devices are referred to as four terminal MOSFETS.[9]

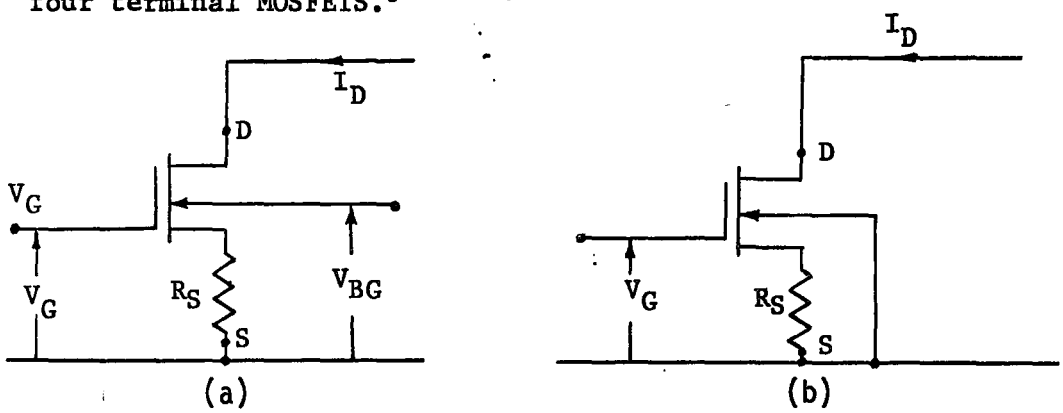


FIG. 2-9 (a) FOUR TERMINAL MOSFET

(b) MOSFET WITH SUBSTRATE GROUNDED

In normal operation the substrate is connected to the source. Therefore as long as R_S and I_D are not too large $V_{BG} \simeq 0$ when the substrate is grounded.

When a voltage is applied to the substrate, often referred to as V_{BG} (voltage on "Back Gate"), the threshold changes from Eq. (1-12b).

$$V_{TH} = -\frac{Q_{ss} + Q_D}{C}$$

$$= -\frac{t_{ox}}{\varepsilon_{ox}} Q_{ss} + \sqrt{2\, q\, \varepsilon_s\, N_A}\ \sqrt{\phi_s}\ \frac{t_{ox}}{\varepsilon_{ox}}$$

$$= V_{ss} + \phi\sqrt{\phi_s} \qquad \ldots(2\text{-}24)$$

To:

$$V_{TH} = V_{ss} + \phi \sqrt{\pm(\phi_s + V_{BG})} \qquad \ldots(2\text{-}25)$$

Where

$$V_{ss} = -\frac{t_{ox}}{\varepsilon_{ox}} Q_{ss} \qquad \ldots(2\text{-}26)$$

And as in Eq. (1-30):

$$\phi = \frac{t_{ox}}{\varepsilon_{ox}} \sqrt{2 N_A q \varepsilon_s}$$

$$\phi_s = 2\phi_F = \frac{2KT}{q} \ln \frac{N_A}{n_i} \qquad \ldots(2\text{-}27)$$

Since the "Back Gate" can have approximately 30% of the control of the front gate, it cannot be neglected in the upper device. This can easily be seen by looking at Fig. 2-10

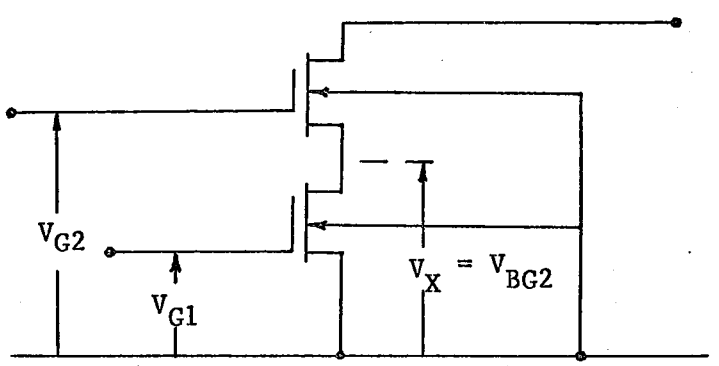


FIG. 2-10 BOTH SUBSTRATES GROUNDED

If the bottom device in Fig. 2-10 has a gate voltage V_{G1}, such that $V_X \simeq 3$ Volts, then the top device has a V_{BG} of $-V_X \simeq -3$ Volts. Since the voltage V_{BG} has approximately 30% of the control that the

front gate voltage has, this is then equivalent to -1.0 Volt added to V_{G2}. The -1.0 volt can easily represent 25% of the existing gate voltage and cannot therefore be neglected.

R_{S1} is usually small, in the range of 5 to 50Ω. Even at 10 ma this only represents a back gate voltage of .05 to .5 Volts on the bottom device. Compared to the V_{BG} of 3 Volts on the top device this is negligible.

Therefore the constants left to be found are R_{S2}, V_{SS2}, ϕ_2 and ϕ_{S2}.

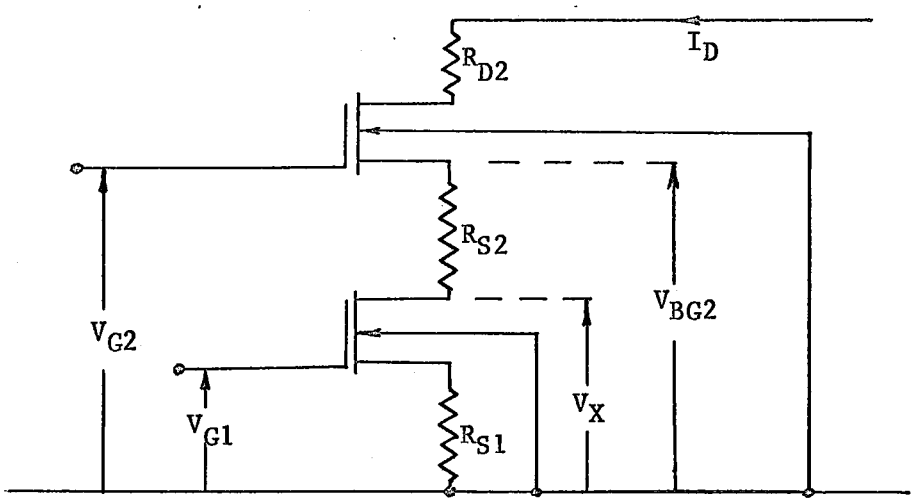


FIG. 2-11 CIRCUIT USED IN OBTAINING THE SUBSTRATE CORRECTION FOR THE DUAL-GATE MOSFET

In Fig. 2-11 it can be seen that

$$V_{BG2} = + (V_X + I_D R_{S2}) \qquad \ldots(2\text{-}28)$$

By connecting the dual-gate MOSFET as shown in Fig. 2-12 and by using three points at saturation on the resulting V-I curves we can

solve for the remaining unknowns. In Fig. 2-12 we are turning the bottom device fully on by applying a large positive gate voltage. The resulting V-I curves are shown in Fig. 2-13.

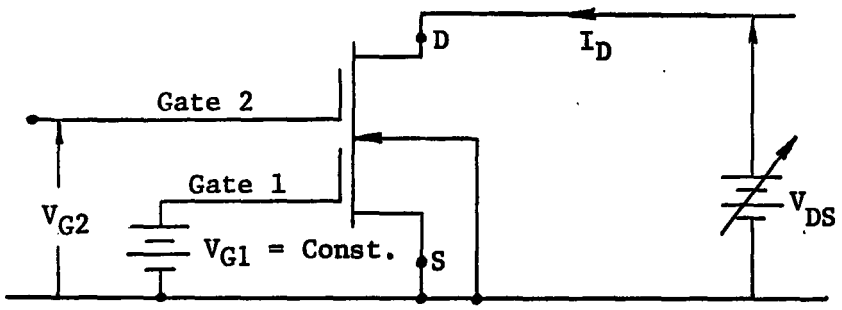


FIG. 2-12 CONNECTION OF DUAL-GATE MOSFET USED TO GENERATE V-I CURVES IN FIG. 2-13

By using the three points P_8, P_9, and P_{10} shown in Fig. 2-13 we can now solve for R_{S2}, V_{SS2}, $\emptyset_2$ and $\emptyset_{S2}$.

For the 3N141 FET device #A the values used are shown in the table below.

POINT	DRAIN CURRENT	DRAIN TO SOURCE VOLTAGE	GATE #1 VOLTAGE	GATE #2 VOLTAGE VOLTS
P_8	I_{D8} = 11.9 ma	V_{DS8} = 4.0 Volts	4.0 Volts	V_{G8} = 2.0
P_9	I_{D9} = 5.35 ma	V_{DS9} = 1.9 Volts	4.0 Volts	V_{G9} = .8
P_{10}	I_{D10}= .4 ma	V_{DS10}= .25 Volts	4.0 Volts	V_{G10}= -.4

Using the computer to solve the triode equation, we obtain three

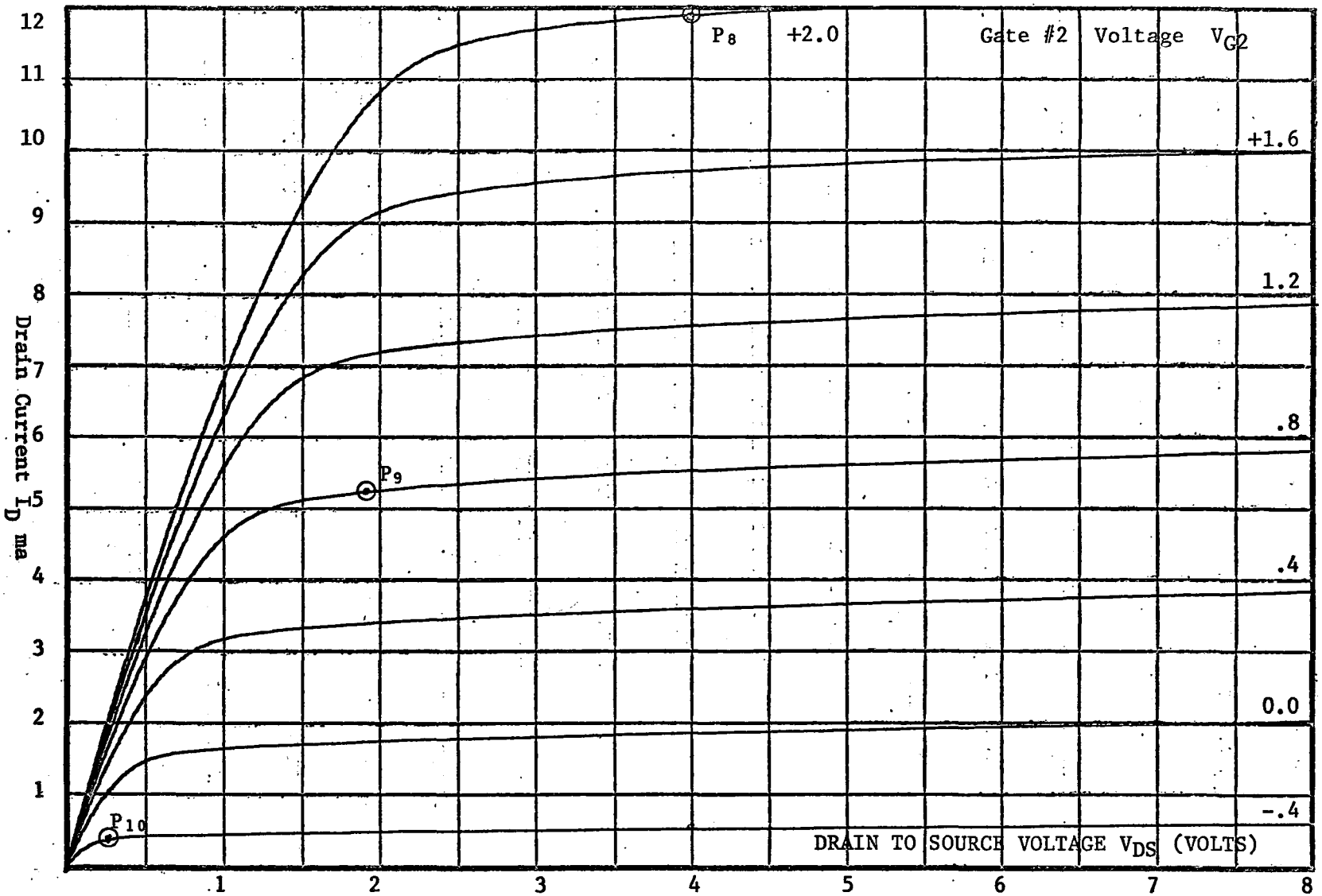


Fig. 2-13 Current vs Supply Voltage Curves with Device #A Connected as shown in Fig. 2-12.

values of V_X for the three saturation currents. The equation that has to be solved is:

$$I_D = \beta_1 V_X (V_{G1} - V_{TH} - I_D R_{S1} - \tfrac{1}{2}V_X - \frac{2}{3}\phi_1 \sqrt{V_X}) \qquad \ldots(2\text{-}29)$$

Solving Eq. (2-29) at P_8, P_9 and P_{10} gives us:

V_{X8} = .58 Volts for I_{D8} = 11.9 ma

V_{X9} = .25 Volts for I_{D9} = 5.35 ma

V_{X10} = .019 Volts for I_{D10} = 0.4 ma

Our equivalent circuit for the saturation region of the upper part of the device can now be described by Fig. (2-14).

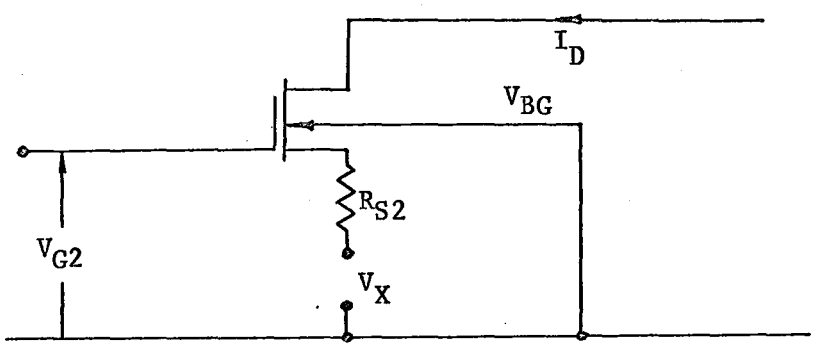


FIG. 2-14 EQUIVALENT CIRCUIT FOR THE UPPER PART OF DUAL-GATE MOSFET

In Fig. (2-14) it can be seen that $V_{BG} = +(V_X + I_D R_{S2})$ as shown in Eq. (2-28).

Therefore the new threshold voltage, V_{TH}, becomes:

$$V_{TH} = V_{SS2} + \phi_2 \sqrt{\pm(\phi_{S2} + V_X + I_D R_{S2})} \qquad \ldots(2\text{-}30)$$

This then gives us the saturation current as:

$$I_D = \frac{\beta_2}{2}\left(V_{G2} - V_X - I_D R_{S2} - V_{SS2} - \phi_2 \sqrt{ABS(\phi_{S2} + V_X + I_D R_{S2})}\right)^2 \qquad \ldots(2\text{-}31)$$

Substituting Eq. (2-28) into Eq. (2-31) we arrive at:

$$I_D = \frac{\beta_2}{2}\left(V_{BG} + V_{G2} - V_{SS2} - \phi_2\sqrt{ABS(\phi_{S2} + V_{BG})}\right)^2 \quad ...(2\text{-}32)$$

This can be rewritten as:

$$V_{G2} + V_{BG} - \sqrt{\frac{2I_D}{\beta_2}} = \phi_2\sqrt{ABS(\phi_{S2} + V_{BG})} + V_{SS2} \quad ...(2\text{-}33)$$

Substituting points P_8, P_9 and P_{10} we obtain:

$$T_1 = \phi_2\sqrt{ABS(\phi_{S2} + V_{BG8})} + V_{SS2} \quad ...(2\text{-}34)$$

$$T_2 = \phi_2\sqrt{ABS(\phi_{S2} + V_{BG9})} + V_{SS2} \quad ...(2\text{-}35)$$

$$T_3 = \phi_2\sqrt{ABS(\phi_{S2} + V_{BG10})} + V_{SS2} \quad ...(2\text{-}36)$$

Where $T_1 = V_{G8} + V_{BG8} - \sqrt{\frac{2I_{D8}}{\beta_2}}$ ...(2-37)

$$T_2 = V_{G9} + V_{BG9} - \sqrt{\frac{2I_{D9}}{\beta_2}} \quad ...(2\text{-}38)$$

$$T_3 = V_{G10} + V_{BG10} - \sqrt{\frac{2I_{D10}}{\beta_2}} \quad ...(2\text{-}39)$$

Eq. (2-34) subtracted from Eq. (2-35) results in:

$$V_{BG8} - V_{BG9} = \frac{1}{(\phi_2)^2}\left[(T_1 - V_{SS2})^2 - (T_2 - V_{SS2})^2\right] \quad ...(2\text{-}40)$$

Subtracting Eq. (2-36) from Eq. (2-34) gives:

$$V_{BG8} - V_{BG10} = \frac{1}{(\phi_2)^2}\left[(T_1 - V_{SS2})^2 - (T_3 - V_{SS2})^2\right] \quad ...(2\text{-}41)$$

Dividing Eq. (2-41) into Eq. (2-40) we arrive at:

$$\frac{V_{BG8} - V_{BG9}}{V_{BG8} - V_{BG10}} = \frac{(T_1 - T_2)\ (T_1 + T_2 - 2\ V_{SS2})}{(T_1 - T_3)\ (T_1 + T_3 - 2\ V_{SS2})} \qquad \ldots(2\text{-}42)$$

Let

$$\frac{(V_{BG8} - V_{BG9})\ (T_1 - T_3)}{(V_{BG8} - V_{BG10})\ (T_1 - T_2)} = TT \qquad \ldots(2\text{-}43)$$

Solving Eq. (2-42) for V_{SS2} we can show that

$$V_{SS2} = \frac{TT\ (T_3 + T_1) - (T_2 + T_1)}{2(TT - 1)} \qquad \ldots(2\text{-}44)$$

Now Eq. (2-40) can be solved for ϕ_2 which becomes:

$$\phi_2 = \sqrt{\frac{(T_1 - T_2)\ (T_1 + T_2 - 2\ V_{SS2})}{V_{BG8} - V_{BG9}}} \qquad \ldots(2\text{-}45)$$

Solving Eq. (2-34) for ϕ_{S2} gives us:

$$\phi_{S2} = \left(\frac{T_1 - V_{SS2}}{\phi_2}\right)^2 - V_{BG8} \qquad \ldots(2\text{-}46)$$

We cannot solve Eq. (2-44), Eq. (2-45) and Eq. (2-46) yet, because we do not know the value of R_{S2} and therefore can not find V_{BG8}, V_{BG9}, and V_{BG10}. This problem can be solved by using the relationship:

$$V_{TH2} = \phi_2 \sqrt{\phi_{S2}} + V_{SS2} \qquad \ldots(2\text{-}47)$$

Equation (2-47) represents the threshold voltage at $I_D = 0$. Since we found the value of V_{TH2} with Eq. (2-16) we can use Eq. (2-47) to find the value of R_{S2} through an iterative approach. A very small value of R_{S2} is assumed. This value of R_{S2} is used to solve Eq. (2-28). Now Equations (2-44), (2-45) and (2-46) can be solved for ϕ_2, ϕ_{S2} and V_{SS2}. These values are substituted into Eq. (2-47) to obtain a trial value of V_{TH2}. If the trial V_{TH2} is not within a specified interval of the actual V_{TH2} found with Eq. (2-16), a new larger value of R_{S2} is tried. This process continues until the trial V_{TH2} is within some specified error of the actual V_{TH2}.

Since R_{S2} has been found we can find R_{D2} because:

$$R_{D2} = R_T - (R_{S1} + R_{S2}) \qquad \ldots(2\text{-}48)$$

We can now solve for all our parameters in the dual-gate MOSFET. The twelve points required can be read directly from a transistor-curve tracer if an additional power supply is used for the other gate bias. The computer program to solve for the twelve unknown parameters is found in appendix II.

V_{TH1}	= -0.406V	K_1	= 26 mho	ϕ_2	= .08215$V^{\frac{1}{2}}$
R_{S1}	= 43Ω	V_{TH2}	= -.525V	ϕ_{S2}	= 1.212V
β_1	= .0469A/V^2	R_{S2}	= 48Ω	R_{D2}	= 3.05Ω
ϕ_1	= .226$V^{\frac{1}{2}}$	β_2	= .0114A/V^2	V_{SS2}	= -0.614V

TABLE I PARAMETERS FOR DUAL-GATE MOSFET DEVICE #A

CHAPTER III

3.1 TRANSCONDUCTANCE CURVES

The transconductance curves we are interested in are those generated with gate #2 voltage remaining constant. The required transconductance, (g_{fS1}), is defined as a small change in gate #1 voltage divided into the corresponding change in the short circuit output current.

The experimental transconductance curves are obtained by equipment set up as shown in Fig. (3-1).

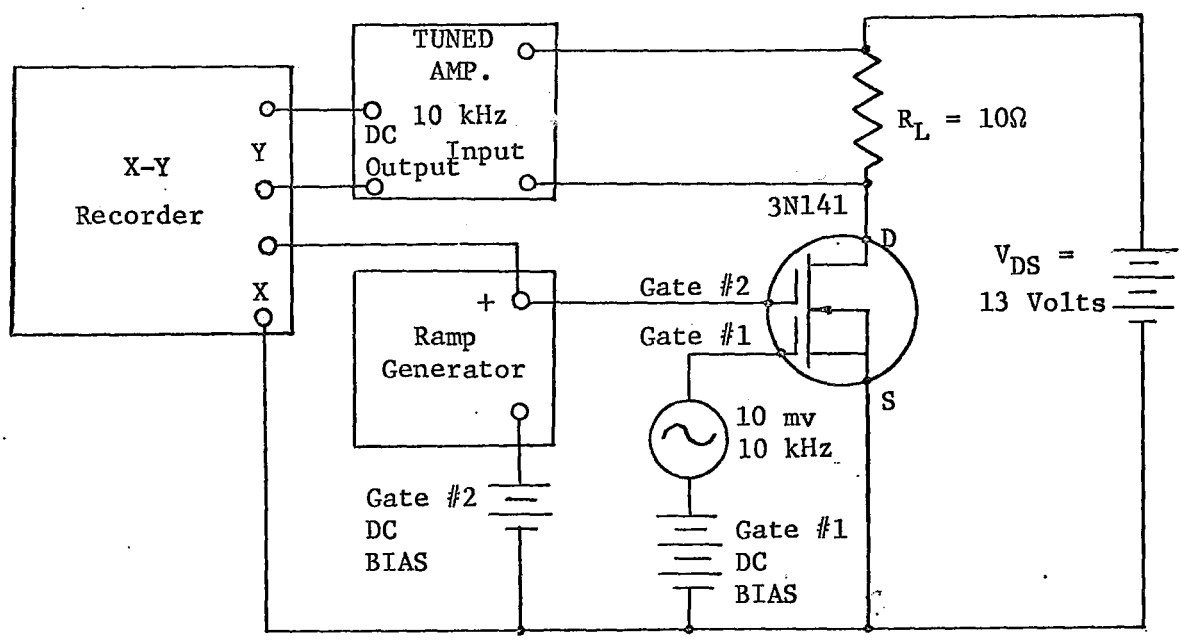


FIG. 3-1 SET-UP FOR OBTAINING GATE #1 TRANSCONDUCTANCE CURVES

A set of experimental results obtained using the set-up shown in Fig. (3-1) is shown in Fig. (3-2). These results are again for the 3N141 device #A.

The theoretical transconductance curves can be generated by a computer program which uses the twelve parameters found in chapter II. To find the transconductance curves with respect to gate #1 we first must obtain the characteristic curves shown in Fig. (3-3). In Fig. (3-3) drain current is plotted against the voltage of gate number one for specific values of V_{G2}. The drain to source voltage is held constant at some value; in this case 13 volts.

To generate the curves in Fig. (3-3) the following procedure is followed.

(1) A specific value is assigned to V_{G1}; for example, .8 volts.

(2) Using a trial current and all the parameters for the bottom portion of the device, the voltage drop across the lower section is found (V_X in figure 2-14).

(3) Knowing the feedback voltage in the gate circuit of the top portion of the device and using the current of step (2) we can solve equation (2-31) to find V_{G2}.

(4) We are looking for a specific value of V_{G2}, i.e. 1.0 volt. Therefore we have an error which is 1.0 volt minus the V_{G2} found in step (3).

(5) Returning to step (2), the new current becomes current plus delta (delta being a small value of current).

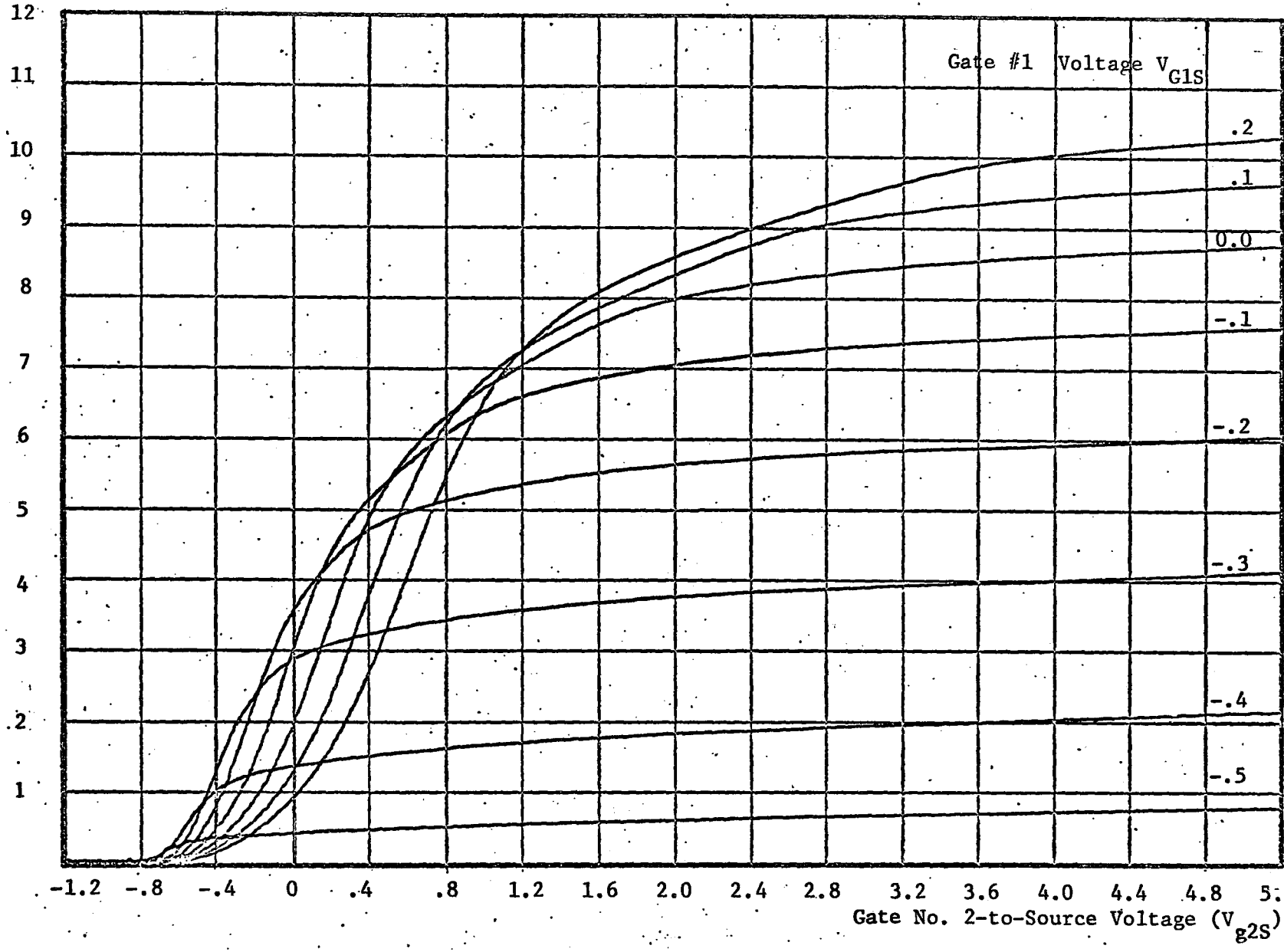


Fig. 3-2 Gate No. 1 Forward Transconductance vs Gate No. 2-to-Source Voltage

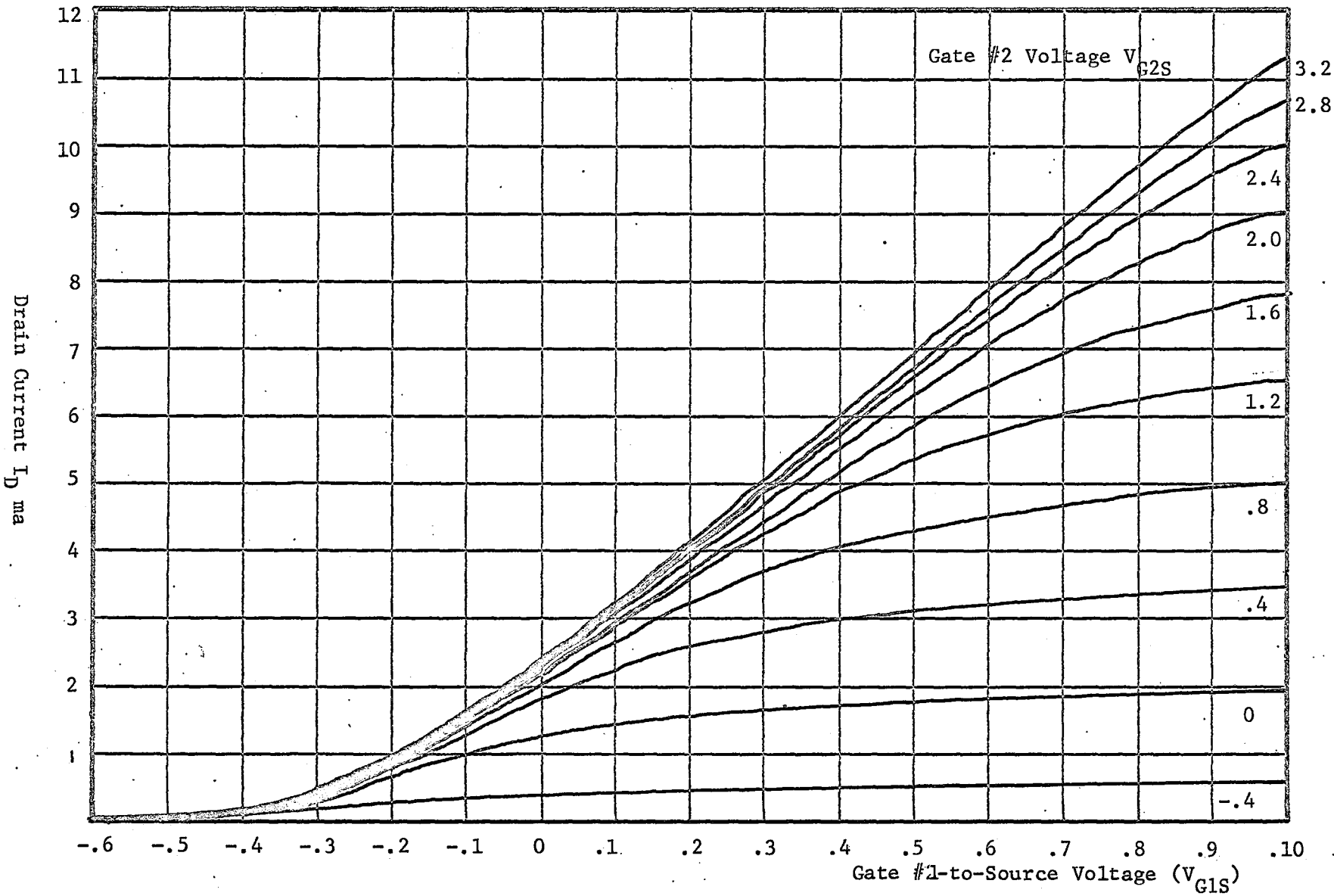


Fig. 3-3 I_D vs V_{G1S} Transfer Characteristics

(6) We continue on to step (4) to find a new error. If the new error is smaller we go back to step (2) and again add delta to our new current. If the error has increased we divide delta by 10 and change its sign.

(7) This process continues until the error is smaller than some specified value at which point the value of V_{G1}, V_{G2} and I_{DS} is stored.

(8) By changing both V_{G1} and V_{G2} in specified increments we can generate the whole set of characteristic curves shown in Fig. (3-3).

It is now easy to find the transconductance curves from Fig. (3-3). The transconductance is the slope of the curve at the point of interest. For example if the computer had stored the values (taken from Fig. 3-3), which are as follows:

$V_{G1}' = .1$ Volts, $V_{G2}' = 1.2$ Volts, $I_{DS}' = 2.9$ ma, $V_{DS} = 13$ Volts

$V_{G1}'' = .3$ Volts, $V_{G2}'' = 1.2$ Volts, $I_{DS}'' = 4.3$ ma, $V_{DS} = 13$ Volts

Then the forward transconductance with respect to gate #1 is

$$g_{fs1} = \frac{\partial I_{DS}}{\partial V_{G1}}$$

$$= \frac{(4.3 - 2.9)\ 10^{-3}}{.3 - .1}$$

$$= 7.0 \text{ mU}$$

The above compares well with a value of 7.2 m℧ found from the experimental results in Fig. 3-2. The small error is due to the large interval of .2 volts used to find the slope of a curved line. The computer program used to generate the curves in Fig. (3-3) and the transconductance curves (g_{fS1}) in Fig. (3-2) is found in appendix II. The experimental and theoretical transconductance curves are compared in chapter V.

CHAPTER IV

THE DUAL-GATE MOSFET MIXER

4.1 CONVERSION TRANSCONDUCTANCE

For mixing, the dual-gate MOSFET is connected as shown in Fig. (4-1). In this circuit the channel is modulated by gate #2 with the pump voltage V_p. The signal voltage, V_s, is applied to gate #1. The load, Z_L, is usually a circuit tuned to the I.F. (intermediate-frequency) which is normally $f_p - f_s$ (pump frequency-signal frequency).

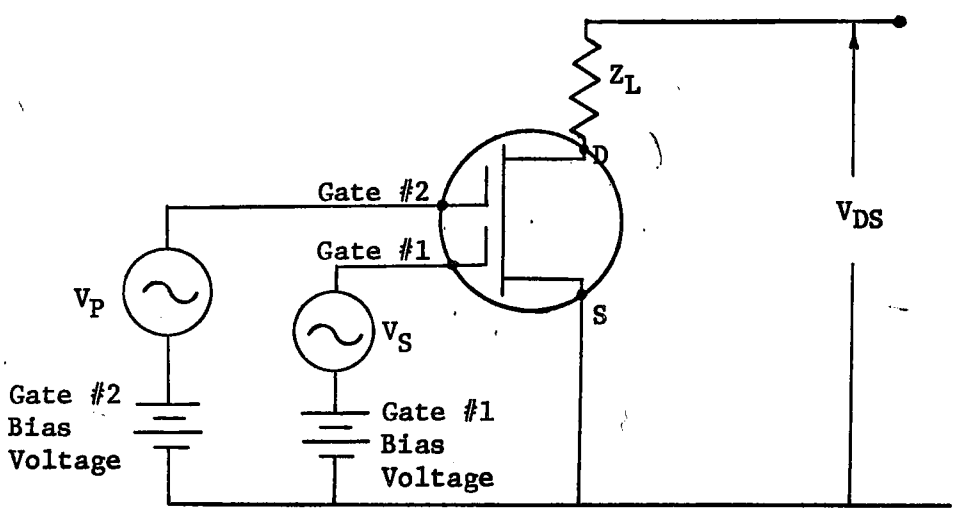


FIG. 4-1 SIMPLIFIED MIXER DIAGRAM

The operation of a mixer can be analyzed because the local oscillator voltage is so large compared to the signal voltage that the transconductance at any instant is determined only by the amplitude of

the local oscillator voltage, and is independent of the signal voltage.[10]

In accordance with the above assumption, the transconductance of the FET will vary during the oscillator frequency in the manner illustrated in Fig. [4-2(c)].

This transconductance can be represented by the Fourier series

$$g_m = a_0 + a_1 \cos\omega_p t + a_2 \cos 2\omega_p t + a_3 \cos 3\omega_p t \qquad \ldots(4\text{-}1)$$

where

g_m = instantaneous transconductance

$\omega_p/2\pi$ = frequency of local oscillator

a_0, a_1, a_2 etc. = coefficients determined by the shape of the g_m curves as a function of time.

The current, i, that flows at any instant as the result of the application of the small signal voltage $V_s \sin\omega_s t$ is the product of this instantaneous signal voltage and the instantaneous signal transconductance as given by Eq. (4-1) and can be written as:

$$i = a_0 V_s \sin\omega_s t + a_1 V_s \sin\omega_s t \cos\omega_p t + a_2 V_s \sin\omega_s t \cos 2\omega_p t + \ldots \qquad \ldots(4\text{-}2)$$

Expanding the $\sin\omega_s t \cos n\omega_p t$ terms into sum and difference of two angles gives:

$$i = a_0 V_s \sin\omega_s t + \frac{a_1}{2} V_s \left[\sin(\omega_s-\omega_p)t + \sin(\omega_s+\omega_p)t\right] + \frac{a_2}{2} V_s \left[\sin(\omega_s-2\omega_p)t + \sin(\omega_s+2\omega_p)t\right] + \ldots \qquad \ldots(4\text{-}3)$$

Examination of Eq. (4-3) shows that the output current contains a component having a difference frequency $(\omega_s-\omega_p)/2\pi$ and a magnitude $a_1V_s/2$. The term $a_1/2$ is termed the conversion transconductance. It is analogous to the transconductance, g_m, of an amplifier and represents the factor which, when multiplied by the amplitude of the applied signal, will give the amplitude of the difference-frequency of the short circuit output current.

Since the conversion transconductance is independent of V_s (as long as V_s is small) we have four variables in the circuit of Fig. (4-1) which have to be maximized. By looking at figure 4-2(c) we can see that the transconductance vs time curve will change in size and shape if:

(a) The D.C. bias on gate #1 is changed.

(b) The D.C. bias on gate #2 is changed.

(c) The magnitude of the pump voltage is changed.

(d) The supply voltage, V_{DS}, is changed.

Actually, condition (d), the supply voltage, had very little effect over a wide range (4 to 20 volts for the 3N141 device #A). Therefore it was ignored as a variable.

A computer program was written to find the Fourier series of the transconductance vs time curves produced by systematically changing conditions (a), (b) and (c). The results are plotted and discussed in chapter V. The computer program is found in appendix III.

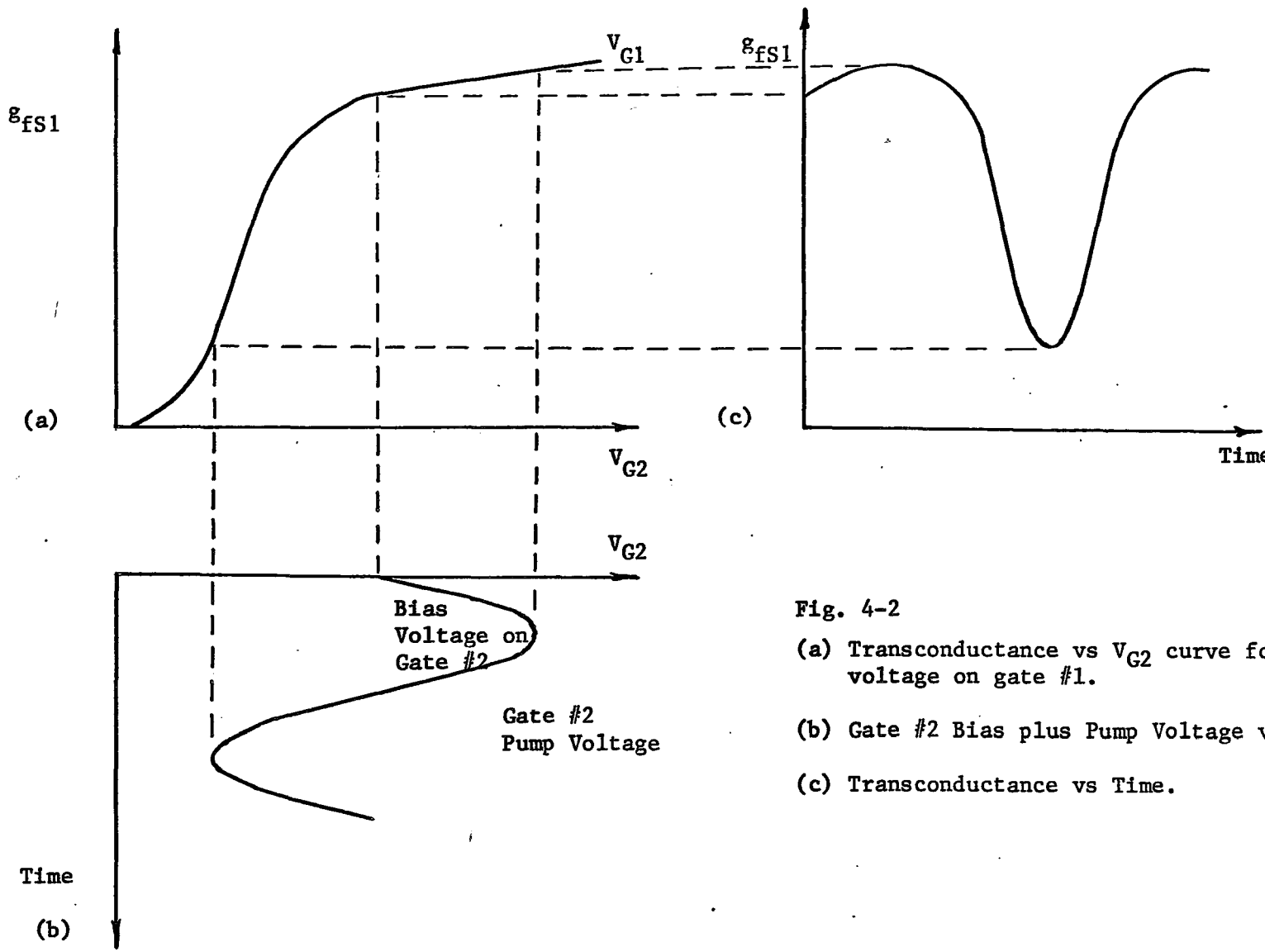


Fig. 4-2

(a) Transconductance vs V_{G2} curve for one bias voltage on gate #1.

(b) Gate #2 Bias plus Pump Voltage vs Time.

(c) Transconductance vs Time.

4.2 OTHER CONSIDERATIONS

(a) Dynamic Range

Dynamic range is the ratio (usually in decibels) of the maximum power to the minimum power. Calculations of dynamic ranges therefore must be based on specific assumptions about what constitutes the "maximum" and "minimum" powers.

The minimum power is usually set by the noise input, or the noise generated internally by the device or both. The maximum power is usually set by undesirable non-linear effects of the device, such as saturation, reduction of gain, generation of harmonics of the signal, distortion, change in phase of the signal, or crosstalk from other signals. In all cases, the pertinent definition of maximum power rests on a clear description, from a system viewpoint, of the maximum tolerable non-linear effects.

(b) Frequencies

Mixing action is done by means of a non-linear device, therefore, many different frequency components will be present in the output of the circuit. These frequency components may be categorized as:

1. Spurious Mixer Products - All frequency components in the output of the mixer other than the desired sum or difference output component.

2. "Crossovers" or "Birdies" - Undesired mixer frequency components which fall within the mixer output passband.

3. "Intermodulation" - Distortion Products - A special class of spurious mixer products falling within the exciter passband, and resulting from interaction between signal components fed into the mixer.

A problem with any mixer is spurious output signals. In addition to the obvious outputs of the local oscillator frequency, the input RF signal frequency, and the undesired sum or difference frequency, many other spurious output signals may be present. Many of these additional spurious outputs are due to third and higher order distortion characteristics which the non-linear device exhibits in addition to the second order distortion utilized by such a device to produce the desired mixing action. MOS field-effect transistors have a transfer characteristic that closely resembles a quadratic curve and therefore have negligible third-order components over a wide range in comparison with bipolar-transistor third-order components.

Third-order effects are most significant in their contribution to cross-modulation distortion. Cross-modulation[11] may be defined as the transfer of information from an undesired carrier to a desired carrier. The first stage of a receiver is the most important in consideration of cross-modulation distortion because the amplitude of the undesired carrier is insignificant in later stages as a result of the selectivity of the initial stage. Therefore, unless a mixer is used as the initial

stage, cross-modulation should not be a problem in the mixing circuit.

(c) Noise

Noise output curves were taken using the circuit shown in Fig. (4-3). As can be seen from the diagram, the gate #1 and drain-to-source voltages were held constant while gate #2 voltage was changed by a ramp generator.

By placing a 1.0 μF capacitor from gate #2 to the source, the shape of the noise curves became an exact duplicate of the g_{fs1} transconductance curves taken previously. The use of the capacitor is not unreasonable, as the normal operation of the dual-gate MOSFET in a mixing circuit is with gate #2 at AC ground potential. A set of experimental noise curves obtained by using the set-up in Fig. (4-3) is found in Fig. (4-4).

The noise curves were taken with the tuned amplifier at 10,000 cps with a bandpass filter Δf, of 3,000 cps. If further investigation shows that the shape of the noise curves remains the same for other frequencies, then a relationship between transconductance and noise could possibly be worked out. An interesting statement made by K. Takagi and A. Van der Ziel[12] in reference to RCA's TA7153 dual-gate MOSFET in saturation is that practically all the noise seems to come from the bottom part of the device. This comment might be useful in establishing a noise model for the dual-gate MOSFET.

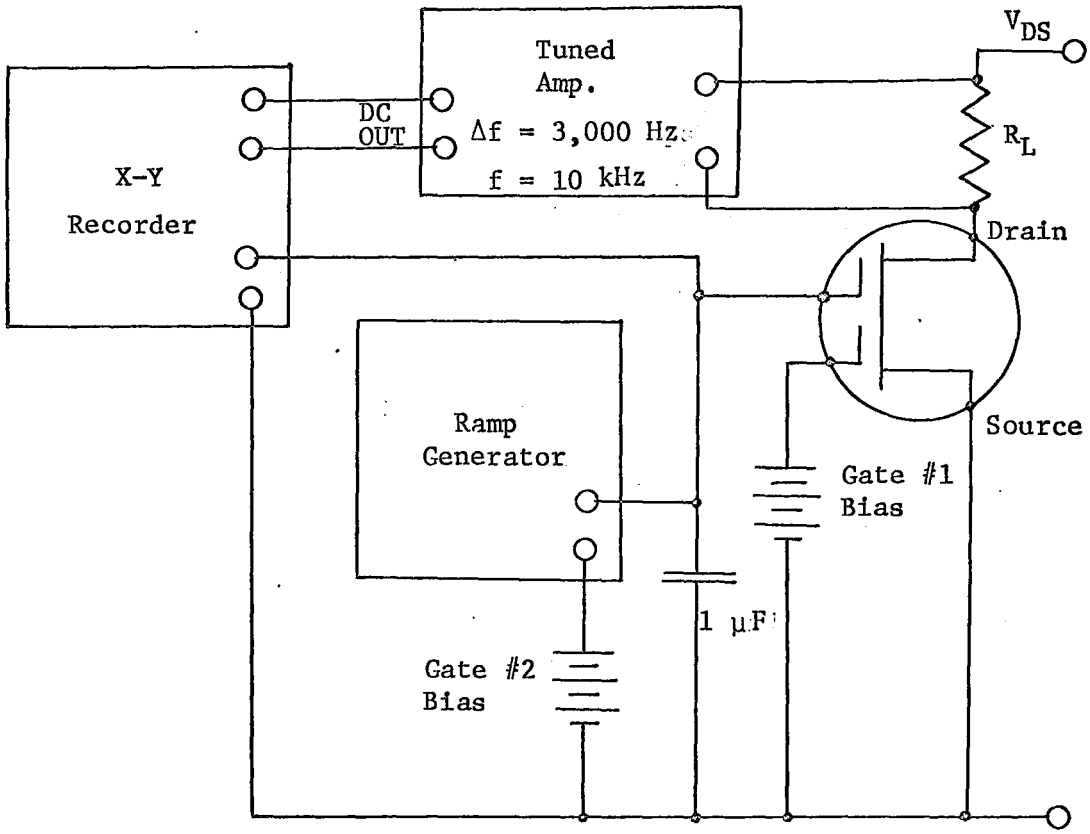


FIG. 4-3 CIRCUIT FOR MEASURING NOISE CURVES

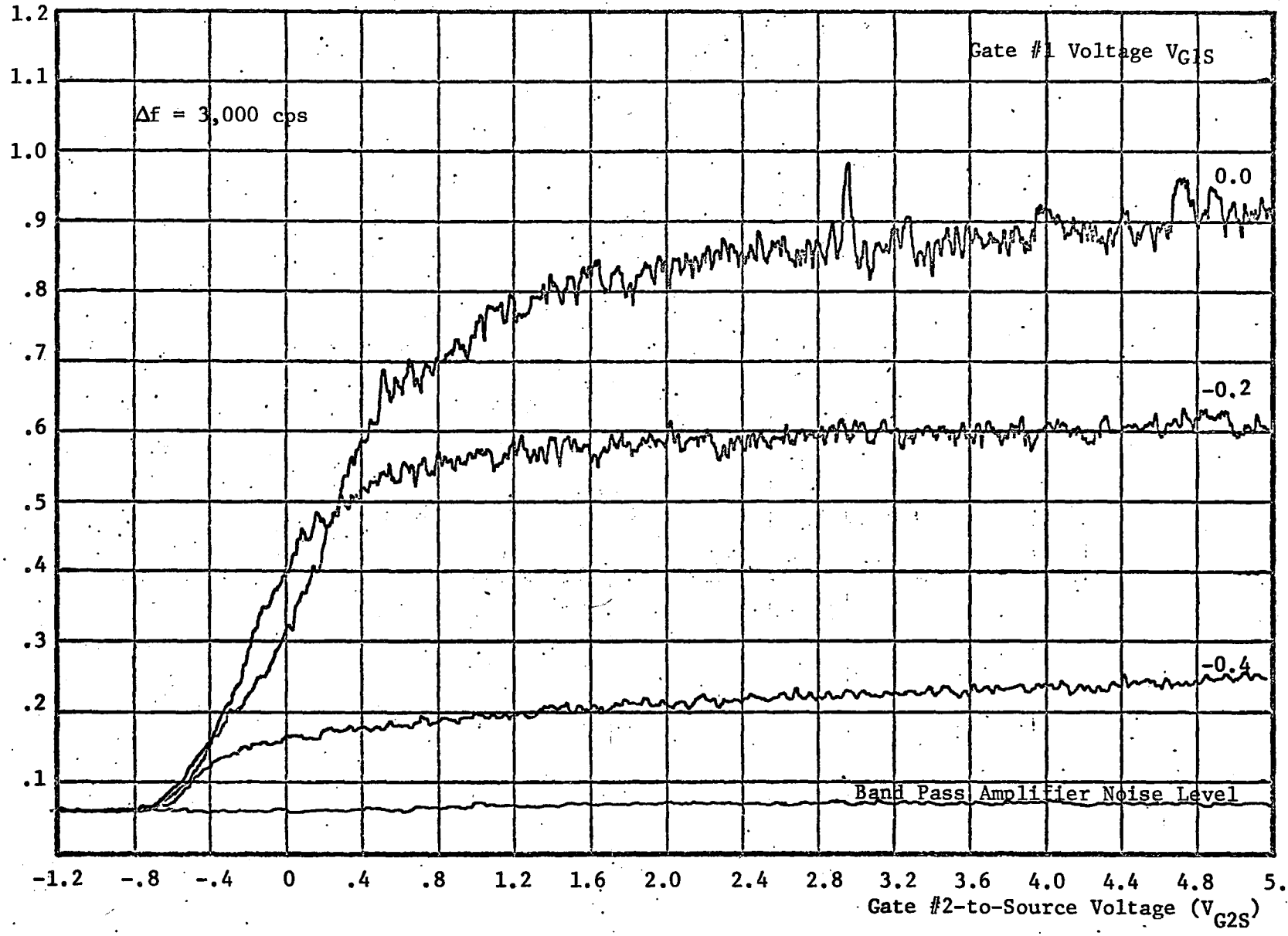


Fig. (4-4) Noise Current as a function of Gate #2-to-source Voltage

CHAPTER V

DISCUSSION OF RESULTS

5.1 RESULTS FOR THE SINGLE-GATE MOSFET

Figures (5-1) and (5-2) show the results for device #I and #II respectively. These are both single-gate devices with the substrate grounded at the source. The solid line represents the experimental results. The broken lines are the theoretical results. The parameters, found by curve fitting, which generated the curves are shown in the table below.

PARAMETERS	DEVICE #I	DEVICE #II
R_S	16.9Ω	60.25Ω
R_D	116.4Ω	128.60Ω
V_P	-2.204 Volts	-2.087 Volts
β	.00681A/V^2	.00973A/V^2
Ø	-.403$V^{\frac{1}{2}}$	-1.1047$V^{\frac{1}{2}}$
K	37.29	161.65

TABLE II PARAMETERS FOR SINGLE-GATE MOSFET DEVICE #I AND #II

As can be seen by looking at Figures (5-1) and (5-2) the difference between the experimental and theoretical I-V curves is very small. One problem was encountered when the computer program was

written to generate the experimental I-V curves. This was that the parameters found by curve fitting gave rise to a triode equation (dotted part of the curve in Fig. 5-3) which reached its peak value below the line obtained for the saturation region (broken line in Fig. 5-3).

Since we are mainly interested in finding the transconductance curves, the problem was avoided by bridging the gap between the triode region and the saturation region with an ellipse (solid line in Fig. 5-3). Dov Frohman-Bentchkowsky and Leslie Vadasz[7] overcame this problem by finding (by an iterative procedure) a new saturation voltage value at which the conductance for a given current level is equal in both the before-and in-saturation regions.

The required equation for the ellipse is found by using the three points: $P_1(V_C,I_C)$, $P_2(V_B,I_B)$ and $P_3(V_S,I_S)$.

At P_3 $\quad x = 0$

The equation of an ellipse is:

$$\frac{x^2}{a^2} + \frac{y^2}{b^2} = 1 \qquad \ldots(5\text{-}1)$$

Therefore at $x = 0$ $\quad y = b$ or in terms of the current voltage axis:

$$x = V - V_S$$

$$y = I - W\, I_S \qquad \ldots(5\text{-}2)$$

where W is some factor less than 1.

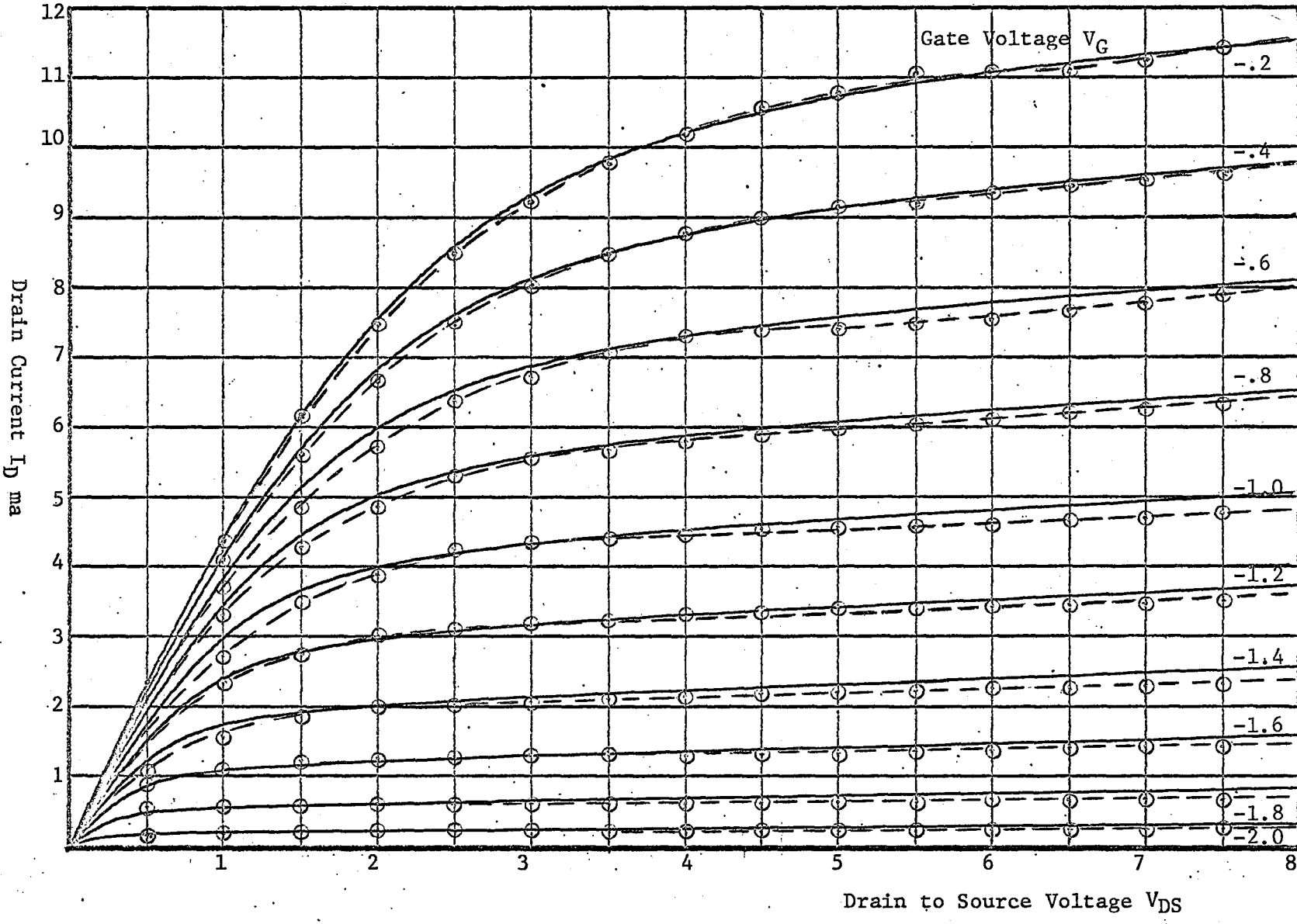


Fig. 5-1 Theoretical static characteristics for the single gate MOSFET Device #I

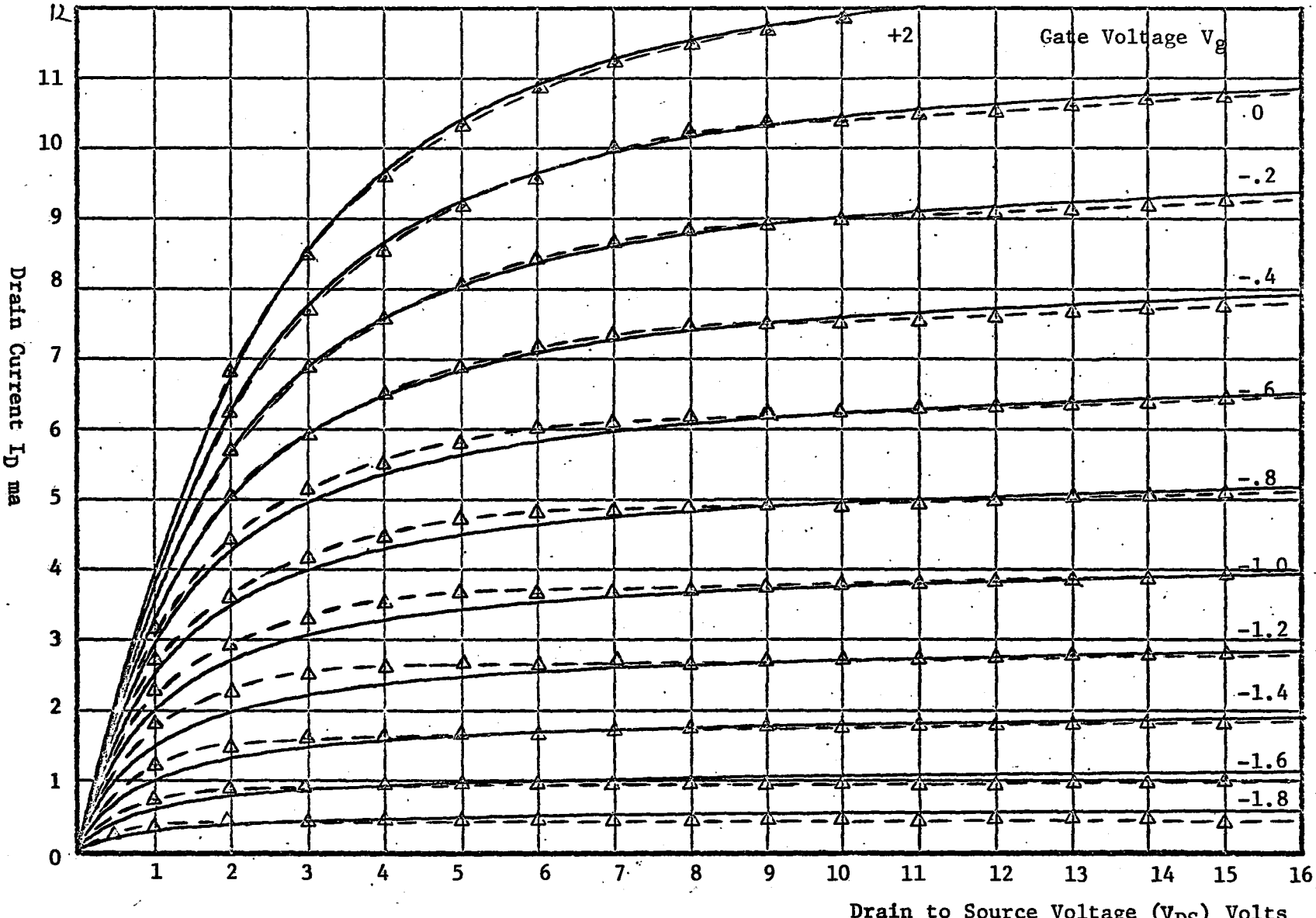


Fig. 5-2 Theoretical static characteristics for Device #II

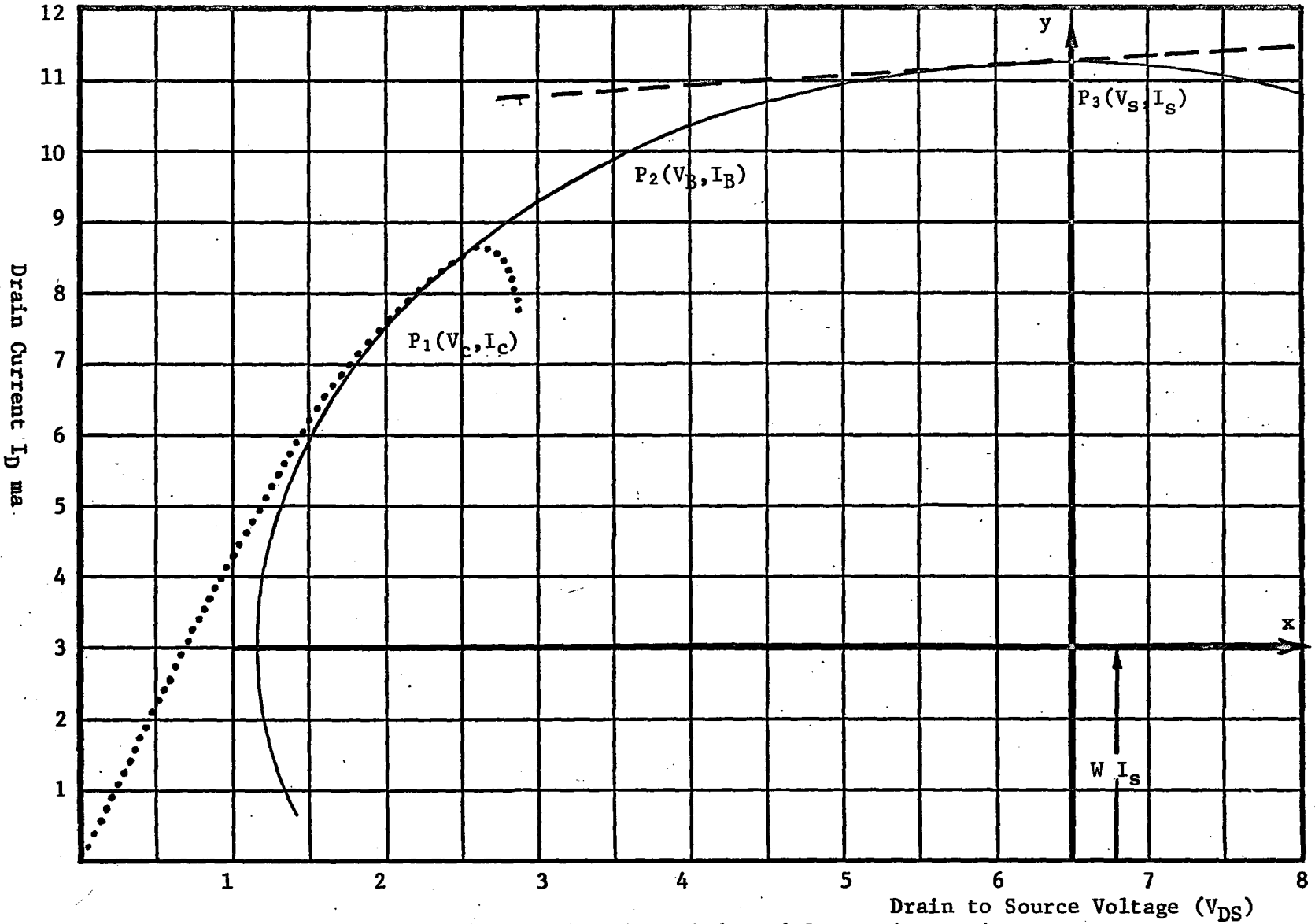


Fig. 5-3 The Ellipse Used to Bridge the Triode and Saturation Region

Using P_1, P_2 and P_3 to solve for a in Eq. (5-1) we have:

$$a = \frac{x}{\sqrt{1 - (y/b)^2}} \qquad \ldots(5\text{-}3)$$

Then:

$$a = \frac{V_B - V_S}{\sqrt{1 - \left(\frac{I_B - WI_S}{(1-W)I_S}\right)^2}} = \frac{V_C - V_S}{\sqrt{1 - \left(\frac{I_C - WI_S}{(1-W)I_S}\right)^2}} \qquad \ldots(5\text{-}4)$$

Rearranging Eq. (5-4):

$$(V_B - V_S)^2 \left(1 - \left\{\frac{I_C - WI_S}{(1-W)I_S}\right\}^2\right) = (V_C - V_S)^2 \left(1 - \left\{\frac{I_B - WI_S}{(1-W)I_S}\right\}^2\right) \ldots(5\text{-}5)$$

$$(V_B - V_S)^2 \left(1 - \frac{I_C - WI_S}{(1-W)I_S}\right) \left(1 + \frac{I_C - WI_S}{(1-W)I_S}\right) = (V_C - V_S)^2 \left(1 - \frac{I_B - WI_S}{(1-W)I_S}\right)$$

$$\left(1 + \frac{I_B - WI_S}{(1-W)I_S}\right) \qquad \ldots(5\text{-}6)$$

Multiplying both sides by $\left((1-W)I_S\right)^2$ we have:

$$(V_B - V_S)^2 (I_S - I_C)(I_S - 2WI_S + I_C) = (V_C - V_S)^2 (I_S - I_B)(I_S - 2WI_S + I_B) \qquad \ldots(5\text{-}7)$$

Let

$$E = (V_B - V_S)^2 (I_S - I_C) \qquad \ldots(5\text{-}8)$$

And

$$F = (V_C - V_S)^2 (I_S - I_B) \qquad \ldots(5\text{-}9)$$

$$\therefore \quad E(I_S + I_C) - 2EWI_S = F(I_S + I_B) - 2FWI_S \qquad \ldots(5\text{-}10)$$

Therefore:

$$W = \frac{F(I_S + I_B) - E(I_S + I_C)}{2I_S(F - E)} \qquad \ldots(5\text{-}11)$$

And:

$$a = \frac{V_B - V_S}{1 - \left\{\frac{I_B - WI_S}{(1-W)I_S}\right\}^2} \qquad \ldots(5\text{-}12)$$

$$b = (1-W)I_S \qquad \ldots(5\text{-}13)$$

Therefore the current as a function of voltage is:

$$I = I_S \left\{ W + (1-W)\sqrt{1 - \left(\frac{V - V_S}{a}\right)^2} \right\} \qquad \ldots(5\text{-}14)$$

As can be seen in fig. 5-1 and 5-2 the ellipse found by equation 5-14 bridges the gap between the saturation and triode region with very little error.

The device used in this work had a maze structure (fig. 2-2). If the gates are not exactly centered in all the sections of the channel we would end up with many paralleled FETs each of which would have

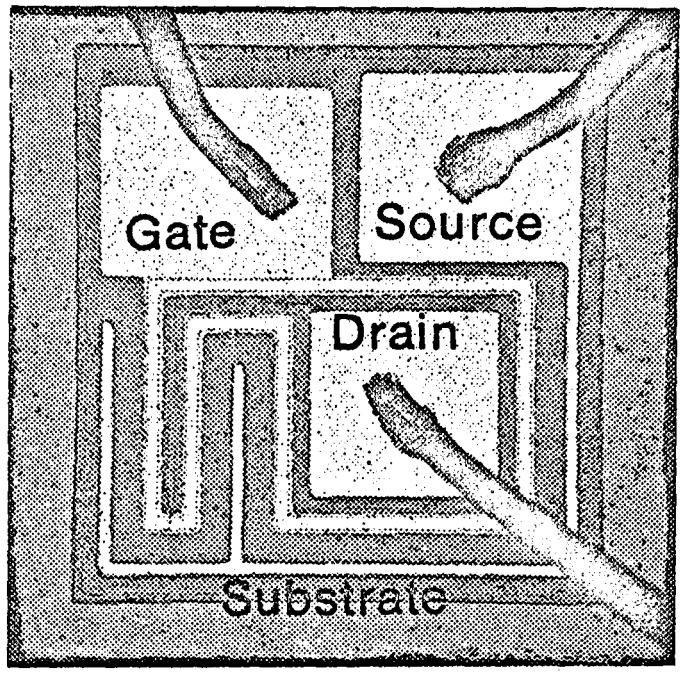
different parasitic resistances. This paralleling of different higher order devices could account for the gap between the triode and saturation region. Further work in this area with simple straight channel devices might provide further information in this area. Another reason for experimenting with straight channel devices is that in the maze structure used, corrections should have been made for the many corners encountered in the device geometry. As these areas are not described by the equations used they are another possible source of error.

5.2 CURRENT - VOLTAGE CURVES FOR THE DUAL-GATE MOSFET

The single-gate MOSFET, device 3N141, has the substrate connection brought out as a separate lead (Fig. 5-4a). By placing two single-gate devices in series, as shown in Fig. 2-3(b), a dual-gate MOSFET was simulated. If the substrate lead of the top device is connected to point B in Fig. 2-3(b) we have a circuit with no voltage applied to the substrate with respect to the source of the top device ($V_{BG} \simeq 0$). By joining the substrate lead to the source of the bottom device (point S_1 in Fig. 2-3(b)) the substrate is connected as it would be in the actual dual-gate MOSFET device 3N143, ($V_{BG} \simeq$ voltage drop across bottom device). By comparing the I-V curves taken for both of the above configurations it was found that a substrate correction would have to be made for the top device.

With the top substrate connected to point S_1 the threshold voltage of the top device shifted approximately -.4 volts at very low currents. Equation 2-25 stated that

(a)



(b)

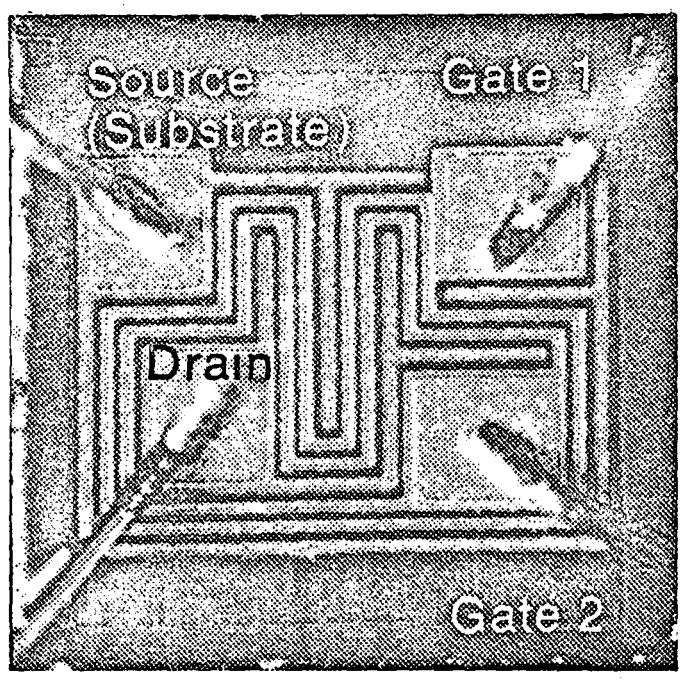


Fig. 5-4 (a) Single Gate MOSFET Chip and Leads

(b) Dual-Gate Chip and Connections

$$V_{TH} = V_{SS} + \emptyset \sqrt{\pm(\emptyset_S + V_{BG})}$$

But for almost zero current $V_{BG} \simeq 0$. Therefore, for very low currents both substrate connections used should give the same threshold voltage of

$$V_{TH} = V_{SS} + \emptyset \sqrt{\pm\emptyset_S}$$

However, experimental results show a difference of .4 volts for V_{TH} (at very low currents) for the two different substrate connections.

This same .4 volt error became apparent when the experimental and computer generated I-V curves for the dual-gate MOSFET were plotted. In Fig. 5-5 I vs V_{G1S} curves are shown for various values of V_{G2S}. The computer generated values are represented by the broken lines while the solid lines are the experimental results. The drain to source voltage, V_{DS}, was held constant at 13 volts for the whole family of curves. The .4 volt shift that could not be explained when the substrate connection was changed for two single gate devices in series also exists here. If -.4 volts were added to V_{G2S} in the theoretical curves a good match would exist between the experimental and theoretical curves shown in Fig. 5-5.

5.3 DISCUSSION OF THE TRANSCONDUCTANCE CURVES

The dotted lines in Fig. 5-6 show the theoretical transconductance values obtained by the computer solution for the dual-gate device #A. The solid lines are again the experimental results. Any

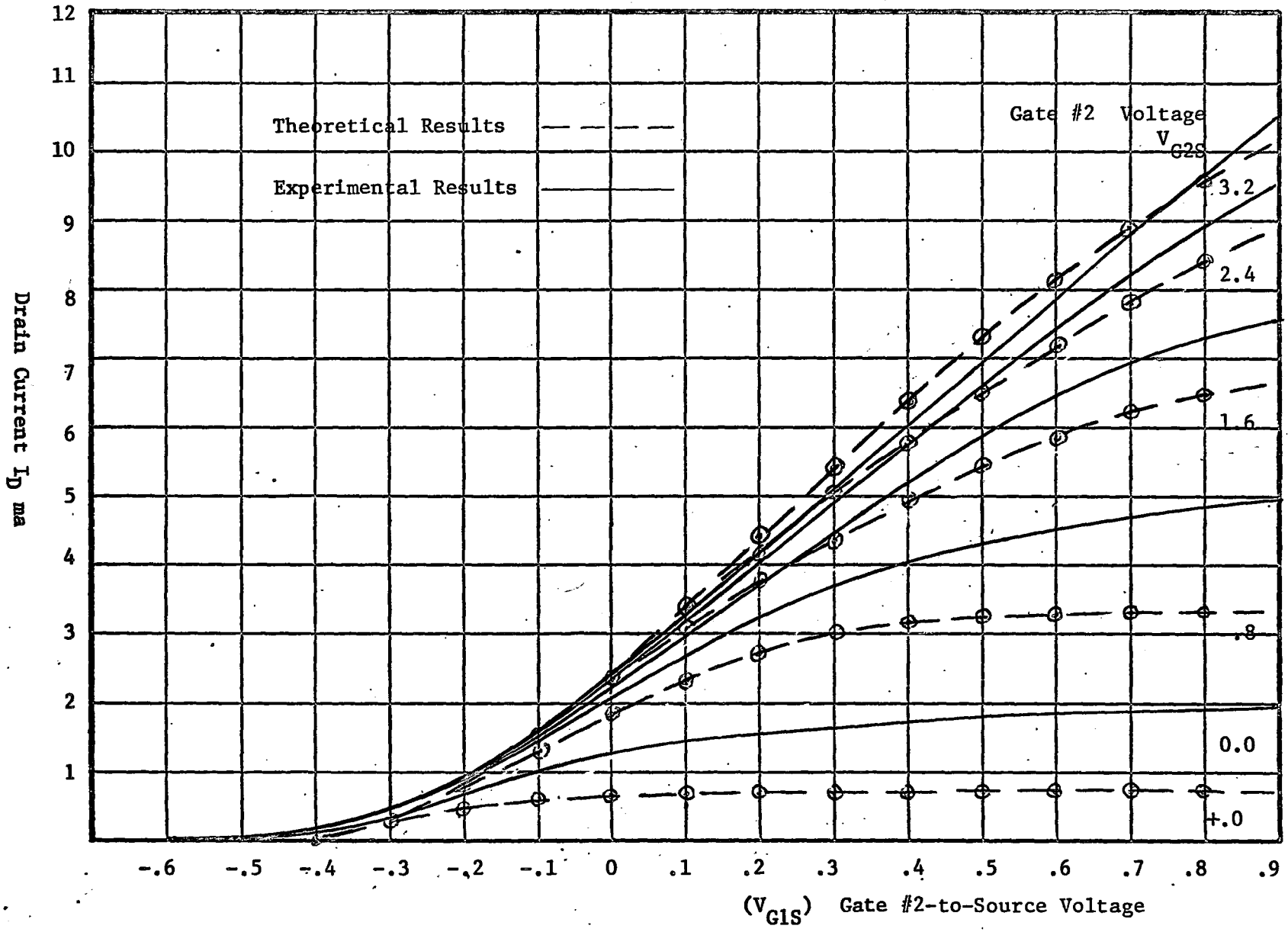


Fig. 5-5 Comparing Transfer Characteristics for the dual-gate device #A

error made in generating the curves in Fig. 5-5 will also show in these curves, as transconductance is the slope of the $I-V_{G1S}$ curves. The .4 volt shift between the theoretical and experimental gate #2 voltage, V_{g2S}, is again apparent. The theoretical curves seem to be shifted approximately .4 volts to the right of the experimental curves.

5.4 CONVERSION TRANSCONDUCTANCE CURVES

By using the computer program in appendix III and a set of experimental transconductance curves it was possible to obtain a set of theoretical conversion transconductance data. As can be seen in Fig. 5-7, experimental computer generated conversion transconductance curves compare very well when accurate transconductance curves are used in the computer solution.

We can therefore generate conversion transconductance curves for a dual-gate MOSFET by two methods.

(a) Using the 12 parameter model found by reading in 13 points as outlined in chapter II.

(b) Reading experimental transconductance curves into the computer program.

Although method (a) is less accurate, in some instances where only an approximate optimum conversion transconductance is required, it has the advantage of speed over method (b). Method (a) requires only that 13 points be read into the computer program where method (b) requires 400 points to be entered.

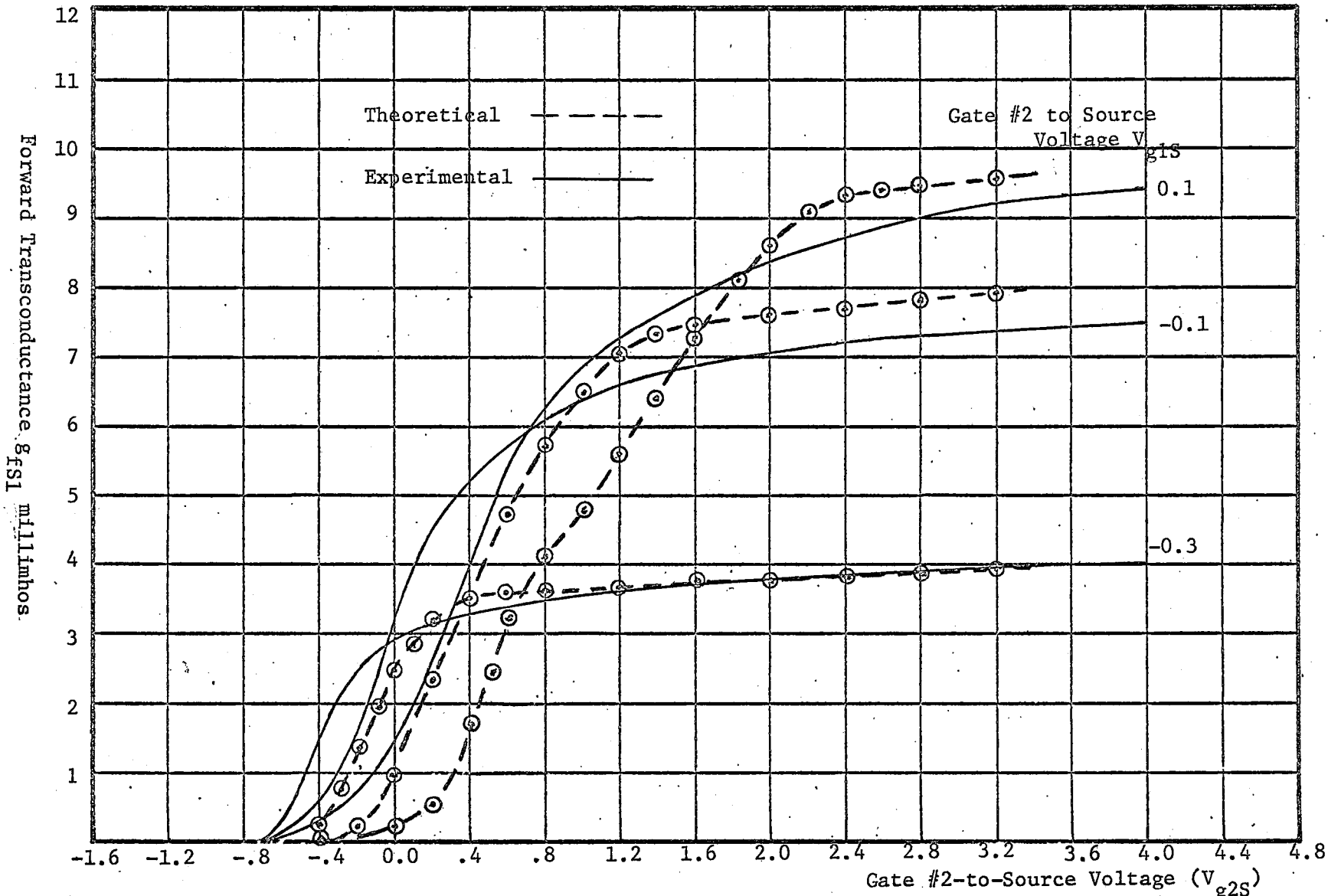


Fig. 5-6 Theoretical and Experimental Transconductance Curves

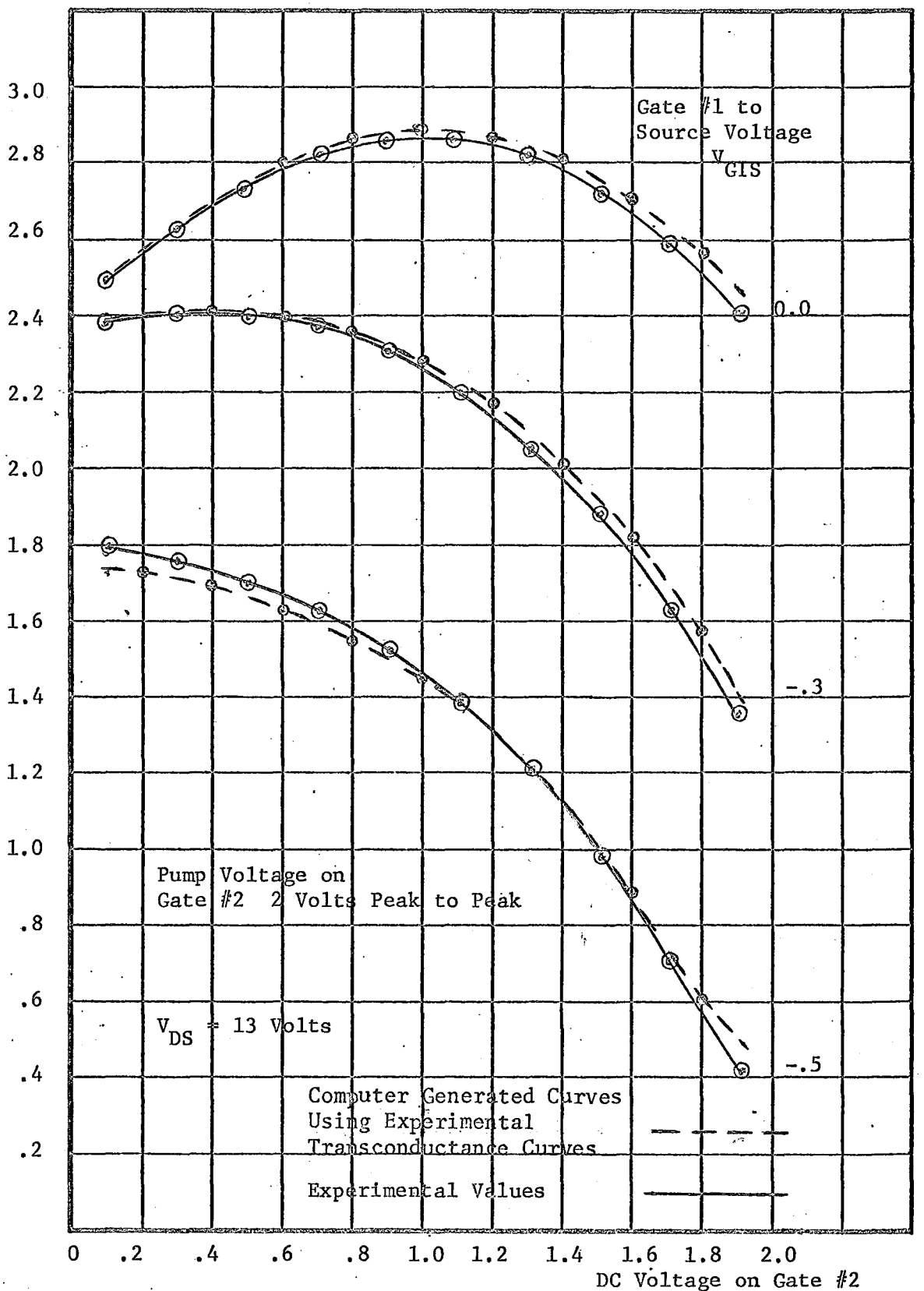


Fig. 5-7 Conversion Transconductance Curves

CONCLUSION

The method used in solving for the parameters of the single-gate MOSFET in Chapter I produced computer generated results which are a very good match to the experimentally obtained values. The model developed would be better still if the gap between the triode and saturation region could be eliminated. By using a straight channel device in further development work, additional refinements could be added to the approach used in these pages to reduce or even eliminate the above mentioned gap. The reasons that it is desirable to use a straight channel device over a maze structure unit for further research are:

(a) The many corners encountered in the maze structure are not covered by the equations developed in Chapter I, and are therefore a source of error.

(b) If the gate is not exactly in the same place in all the different sections of the channel, the result is many parallel FETs, each with different parasitic resistances. This paralleling of higher order devices produces a further deviation between the theoretical and experimental results.

A straight channel device was not used in the development work because no commercially available device could be found.

Further work with two straight channel, single-gate devices connected in series might also produce an explanation of the .4 volt discrepancy noted between the two different substrate connections at low currents. With this error removed, the twelve parameter model developed in Chapter II to represent the dual-gate MOSFET does produce good results.*

For further work in this area, the best results would be achieved if a straight channel dual-gate MOSFET was fabricated with the point between the two gates brought out as a separate lead. This then would make it possible to find the parameters of the two halves of the device individually. These results could then be checked against the values of the parameters found in the dual-gate connection.

The next logical step, after obtaining accurate I-V curves with the dual-gate MOSFET model, would be to extend the frequency range by introducing device capacitances into the model.

* After completion of the thesis an error was detected in the computer program which may have caused this discrepancy. See Page 83, line 35. Change - to +.

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D.M. Griswold, RCA Insulated-Gate MOS Field-Effect Transistors, RCA, Publication No. St-2990A.

APPENDIX I

SINGLE GATE MOSFET COMPUTER PROGRAM

```
      REAL I,II,III,IC,ISAT,KI,M,IB
C     DEVICE NUMBER 12
      C1=0.01195
      C2=0.0061
      C3=0.00091
      C4=0.0063
      G1=0.2
      G2=-0.6
      G3=-1.6
      VSML=0.05
      CSML=0.00021
      VGSML=0.0
      VT1=1.7
      CT1=0.006
      DELV=5.3
      V1=10.5
      VB=3.0
      IB=0.00855
      F=(SQRT(C1*C3)-C3)/(SQRT(C1*C2)-C2 )
      VP=(G1*(SQRT(C3)-F*SQRT(C2))+(SQRT(C1))*(F*G2-G3))/((SQRT(C1))*(F-
     1 1.0)-F*SQRT(C2)+SQRT(C3))
      KI=C2*DELV/(C4-C2)
      RS=(VP*(SQRT(C1)-SQRT(C2))+G1*SQRT(C2)-G2*SQRT(C1))/(C1*SQRT(C2)
     2-C2*SQRT(C1))
      M=(SQRT(C2))/(G2-VP-C2*RS)
      B=2.0*(M**2)
      RD=VSML/CSML-1.0/(B*(VGSML-VP))-RS
      VAT1=VT1-CT1*(RS+RD)
      Q=(3.0/(2.0*SQRT(VAT1)))*(VP-G1+0.5*VAT1+CT1*RS+CT1/(B*VAT1))
      WRITE(6,8)
8     FORMAT( 70H       VP          RS          RD          B           Q
     7 M             KI    )
      WRITE(6,2)VP,RS,RD,B,Q,M,KI
2     FORMAT( /  7F10.5 /// )
      QT=(RS*M)**2
      DIST=0.1
      L9=VP/DIST
      VBE=L9*DIST
      I7=(G1-VBE)/DIST+2.0
      DO 10 K=1,I7
      INDEX = 0
      FF=K
      S=0.0
      V=0.0
      VC=0.0
      IC=0.0
      VGC=0.0
      ISAT=0.0
      A=0.0
      II=0.0
```

```
      III=0.0
      XOX=I7
      VGO=VBE+DIST*(XOX-FF)                                          80
      IF(VGO .LT. VBE) GO TO 10
      WRITE(6,4)
4     FORMAT( //' 95H          V          I MA          VG1          FF
     5    VD          XL          A          VC , / )
      LK=1
44    N3=LK
      DO 30 L=LK,88
      Z=0.05
      AA=L
      IF(L .LE. 10 ) GO TO 451
      IF(L .LE. 58 ) GO TO 452
      GO TO 454
451   V=AA*0.02
      GO TO 455
452   V=0.2+(AA-10.0)*0.1
      GO TO 455
454   V=5.0+(AA-58.0)*0.5
455   IF(INDEX .EQ. 1) GO TO 77
      XL=0.0
      I=III*0.001
19    I=I+0.001*Z
      VD = V- I*(RS+RD)
      IF(VD .LE. 0.0) GO TO 10
      VG=I/(B*VD)+VP+I*RS+0.50*VD-(2.0/3.0)*Q*SQRT(VD)
      GO TO 49
77    VG=VGC
      TIMES=SQRT((TIME*V1)/VC)
      IF(V .GT. TIMES*VC) GO TO 96
      AT=VC*(1.0-TIMES)/SQRT(1.0-((IC-Y*ISAT)/(ISAT*(1.0-Y)))**2)
      XL=((V-TIMES*VC)/AT)**2
      IF(XL .GT. 1.0) GO TO 10
      BE=ISAT*(1.0-Y)
      I=Y*ISAT+BE*SQRT(1.0-XL)
      GO TO 20
96    I=(1.0+(V-TIMES*VC)/KI)*ISAT
      GO TO 20
49    DIFF=ABS(VG-VGO)
      IF(DIFF .LE. 0.0004 ) GO TO 20
      IF(DIFF .GT. DIFF2 ) GO TO 555
      DIFF2=DIFF
      GO TO 19
555   Z=-Z*0.1
      DIFF2=DIFF
99    LK=0.50*V*50.0
      WRITE(6,28)V,III,VG,VGS2,VD,XL,SS,EROR2,EN
28    FORMAT(9F12.6)
      GO TO 19
20    II=I*1000.0
      IF ( INDEX .EQ. 2 ) GO TO 633
      IF(II .LE. III ) GO TO 55
      GO TO 35
55    IF (INDEX .EQ. 0) GO TO 99
      GO TO 35
99    IF(0.8*V .GT. 5.0) GO TO 772
      IF (0.8*V .GT. 0.2 ) GO TO 771
      GO TO 774
772   LK=58.0+(0.8*V-5.0)*2.0
      GO TO 773
```

```
771   LK=10.0+(0.8*V-0.2)*10.0
      GO TO 773
774   LK=0.8*V*50.0
773   III=0.7*III
      INDEX=2
      GO TO 44
633   IC=I
      VC=V
      VGC=VG
      S =2.0*(M**2)*RS*(VP-VGC)
      ISAT =(0.5/QT)*(1.0-S-SQRT(1.0-2.0*S))
      IF(K .EQ. 1) GO TO 25
      GO TO 100
25    E=((VB-V1)**2)*(ISAT-IC)
      F7=((VC-V1)**2)*(ISAT-IB)
      Y=(F7*(IB+ISAT)-E*(IC+ISAT))/(2.0*ISAT*(F7-E))
      TIME=V1/VC
      WRITE(6,32)E,F7,Y,TIME,S,ISAT,IC,VC
32    FORMAT(8F12.7)
100   CONTINUE
      INDEX = 1
35    CONTINUE
      III=II
      WRITE(6,92)V,III,VG,FF,VD,XL,A,VC
92    FORMAT(8F12.3)
30    CONTINUE
10    CONTINUE
      STOP
      END
```

APPENDIX II

DUAL-GATE MOSFET TRANSCONDUCTANCE CURVES

```
      DIMENSION TRANS(40,40),VGS2N(40,40),IN(40,40),VGN(40,40)
      DIMENSION VX(3),C(3),G(3),GG(3),VBG(3),T(3),VR(2),CR(2)
      REAL I,II,III,IC,ISAT,KI,M,IB,KI2,M2,KSQ,K11,IN,IM
C     DEVICE NUMBER AA   DUAL GATE
      C1=0.01165
      C2=0.0065
      C3=0.00072
      C4=0.0075
      G1=0.8
      G2=0.4
      G3=-0.2
      VG2=2.0
C     VSML MUST BE MUCH LESS THAN ( GSML-VP)   BECAUSE I*RS TERM AND V
C     HAVE BEEN IGNORED
      VSML1=0.1
      VSML2=0.15
      VSML3=0.14
      CSML1=0.0006
      CSML2=0.0006
      CSML3=0.0003
      GSML1=1.0
      GSML2=0.2
      GSML3=-0.2
      C(5)=0.0119
      C(6)=0.00535
      C(7)=0.0004
      C8=0.0051
      G(5)=2.0
      G(6)=0.8
      G(7)=-0.4
      VGX=4.0
      VT2=1.25
      CT2=0.00485
      DELV=4.0
      DELV2=1.9
      VV1=5.0
      VVB=2.0
      IB=0.0092
      VDS=13.0
      F=(SQRT(C1*C3)-C3)/(SQRT(C1*C2)-C2)
      VP=(G1*(SQRT(C3)-F*SQRT(C2))+(SQRT(C1))*(F*G2-G3))/((SQRT(C1))*(F-
     1 1.0)-F*SQRT(C2)+SQRT(C3))
      KI=C2*DELV/(C4-C2)
      RS=(VP*(SQRT(C1)-SQRT(C2))+G1*SQRT(C2)-G2*SQRT(C1))/(C1*SQRT(C2)
     2-C2*SQRT(C1))
      M=(SQRT(C2))/(G2-VP-C2*RS)
      B=2.0*(M**2)
      AH=VSML1/CSML1-1.0/(B*(GSML1-VP))
      BH=VSML2/CSML2-1.0/(B*(GSML2-VP))
      CH=VSML3/CSML3-1.0/(B*(GSML3-VP))
```

```
      DH=AH-BH
      EH=AH-CH
      RT=(DH*(CH*GSML3-AH*GSML1)-EH*(BH*GSML2-AH*GSML1))/(DH*(GSML3-GSML
     71)-EH*(GSML2-GSML1))
      VP2=(RT*(GSML3-GSML1)-CH*GSML3+AH*GSML1)/EH
      B2=1.0/((BH-RT)*(GSML2-VP2))
      M2=SQRT(B2/2.0)
      VAT2=VT2-CT2*(RT+1.0/(B2*(VG2-VP2)))
      Q=(1.5/(SQRT(VAT2)))*(G2-VP-0.5*VAT2-CT2*RS-CT2/(B*VAT2))
      WRITE(6,8)
8     FORMAT( 90H       VP          RS          RT          B           Q
     7 M             KI         VP2          B2    )
      WRITE(6,12)VP,RS,RT,B,Q,M,KI,VP2,B2
12    FORMAT( /  9F10.5 /// )
      KI2=C8*DELV2/(C(6)-C8)
      J=7
5     VX=C(J)*RS
3     VX=VX+0.0001
      VD=VX-C(J)*RS
      GG(J)=C(J)/(B*VD)+VP+C(J)*RS+0.5*VD+((SQRT(VD))*Q)/1.5
      IF (VGX .GE. GG(J) ) GO TO 2
      GO TO 3
2     VX(J)=VX
      J=J-1
      IF( J .EQ. 4) GO TO 4
      GO TO 5
4     WRITE(6,17)
17    FORMAT(/ 90H              VX5              VX6              VX7
     7  GG5             GG6              GG7    )
      WRITE(6,11) VX(5),VX(6),VX(7),GG(5),GG(6),GG(7)
11    FORMAT(6F15.4)
      RS2=0.0
909   RS2=RS2+0.1
      DO 420 J=5,7
      VBG(J)=-(VX(J)+C(J)*RS2)
420   T(J)=G(J)+VBG(J)-SQRT(2.0*C(J)/B2)
      TT=((T(7)-T(5))*(VBG(5)-VBG(6)))/((T(6)-T(5))*(VBG(5)-VBG(7)))
      VSS=(TT*(T(5)+T(7))-T(5)-T(6))/(2.0*(TT-1.0))
      KSQ=((T(5)-VSS)**2-(T(6)-VSS)**2)/(VBG(5)-VBG(6))
      K11=SQRT(ABS(KSQ))
       QS=((T(5)-VSS)/K11)**2-VBG(5)
      VPTST=K11*SQRT(ABS(QS))+VSS
      IF ( RS2 .GT. RT) GO TO  969
      TEST =(VPTST-VP2)
      IF (TEST .LT. 0.002) GO TO 969
      GO TO 909
969   WRITE(6,7)
7     FORMAT(90H          TEST             RS2              VSS              QS
     3              VPTST             K11      )
      WRITE(6,996) TEST, RS2,VSS,QS,VPTST,K11
996   FORMAT( / 6F15.5)
      RD2=RT-RS-RS2
      WRITE(6,9)
9     FORMAT(105H          VP2              RS2              M2               B
     22              KI2              RD2              AH       )
      WRITE(6,27) VP2,RS2,M2,B2,KI2,RD2 ,AH
27    FORMAT( / 7F15.5 /// )
      QT=(RS*M)**2
      DIST=0.1
      L9=VP/DIST
      AL9=L9
```

```
      VBE=AL9*DIST
      I7=(G1-VBE)/DIST+1.0
      DO 10 K=1,I7
      INDEX = 0
      FF=K
      S=0.0
      V=0.0
      VC=0.0
      IC=0.0
      VGC=0.0
      ISAT=0.0
      A=0.0
      II=0.0
      III=0.0
      XOX=I7
      VGO=VBE+DIST*(XOX-FF)
      IF(VGO .LT. VBE) GO TO 10
      DIST2=0.1
      L92=VP2/DIST2
      AL92=L92
      VBE2=AL92*DIST2
      BSS=VBE2-DIST2
      N=1
      NMAX=40
      WRITE(6,14)
14    FORMAT( //110H          V          I MA          VG1          VG2
     5    VD          XL          A          VC          N      , / )
      LK=1
44    N3=LK
      WRITE(6,144)LK,INDEX
144   FORMAT(2I15)
      DO 30 L=N3,1000
      IND=0
      EROR2=10.0
      AA=L
      DV=0.005
      V=AA*DV
      H=-0.1*DV
      GO TO 155
166   V=V+H
155   DIFF2=10000.0
      Z=0.05
      IF ( INDEX .EQ. 1 ) GO TO 77
      XL=0.0
      I=III*0.001
19    I=I+0.0001*Z
      VD = V- I*RS
      IF(VD .LE. 0.0) GO TO 6
      VG=I/(B*VD)+VP+I*RS+0.50*VD+(2.0/3.0)*Q*SQRT(VD)
      GO TO 49
77    VG=VGC
      IF(V .GT. TIMES*VC) GO TO 96
      YYY=(IC/ISAT-Y)/(1.0-Y)
      IF(YYY .GT. 1.0 ) GO TO 18
      GO TO 22
18    WRITE(6,21)YYY
21    FORMAT(45H  ERROR. YYY IS GREATER THAN 1.0  .  YYY IS  , 1F15.5 /)
22    AT=VC*(1.0-TIMES)/SQRT(ABS(1.0-YYY**2))
      XL=((V-TIMES*VC)/AT)**2
      IF( XL .GT. 1.0 ) GO TO 30
      BE=ISAT*(1.0-Y)
```

```
      I=Y*ISAT+BE*SQRT(1.0-XL)
      GO TO 20
96    I=(1.0+(V-TIMES*VC)/KI)*ISAT
      GO TO 20
49    DIFF=ABS(VG-VGO)
      IF(DIFF .LE. 0.0004 ) GO TO 20
      IF(DIFF .GT. DIFF2 ) GO TO 555
      DIFF2=DIFF
      GO TO 19
555   Z=-Z*0.1
      DIFF2=DIFF
      GO TO 19
20    II=I*1000.0
      IF ( INDEX .EQ. 2 ) GO TO 633
      IF(IND .EQ. 1 ) GO TO 35
      IF(II .LE. III ) GO TO 55
      GO TO 35
55    IF( INDEX .EQ. 0 ) GO TO 99
      GO TO 35
99    LK=0.50*V/DV
      III=0.45*III
      INDEX=2
      WRITE(6,122)INDEX,III,LK
122   FORMAT(I10,F18.8,I10).
      GO TO 44
633   IC=I
      VC=V
      VGC=VG
      S =2.0*(M**2)*RS*(VP-VGC)
      ISAT =(0.5/QT)*(1.0-S-SQRT(1.0-2.0*S))
      VSAT=VDS-V
      A2=1.0+VSAT/KI2
      VGS2=SQRT(ABS((A2*I*2.0)/B2))+V+I*A2*RS2+K11*SQRT(ABS(QS+V+A2*I*RS
     92))+VSS
      N=(VGS2-BSS)/DIST2+1.0
      WRITE(6,133)LK,INDEX,III,IC,VC,VGC,S,ISAT
133   FORMAT(2I10,6F12.8)
      IF(K .EQ. 1) GO TO 25
      GO TO 100
25    DO 82 NN=1,2
      VR(1)=VVB
      CR(1)=IB
      VR(2)=VV1
      CR(2)=ISAT
      TRY2=100000.0
      P=VR(NN)-CR(NN)*(RS2+RD2)
      U=VG2+0.5*(CR(NN)*(RD2-RS2)+VR(NN))-VSS
      W=QS-CR(NN)*RS2
      VXX=W
      DELTA=1.0
62    VXX=VXX+0.1*DELTA
      CONST=(CR(NN)/(B2*(P-VXX))-U-0.5*VXX)/SQRT(ABS(W-VXX))
      TRY=ABS(K11-CONST)
      IF(TRY .LE. 0.001) GO TO 66
      WRITE(6,210)TRY,CONST,VXX,VR(NN),CR(NN),DELTA,P,U,W
210   FORMAT(9F12.6)
      IF(VXX .GT. VR(NN)) GO TO 64
      IF(TRY .GT. TRY2 ) GO TO 64
      TRY2=TRY
      GO TO 62
64    DELTA=-DELTA*0.1
```

```
      IF(ABS(DELTA) .LT. 0.001 ) GO TO 66
      TRY2=TRY
      GO TO 62
66    IF(NN .EQ. 1) GO TO 84
      GO TO 86                                                    86
84    VB=VXX
      GO TO 82
86    V1=VXX
82    CONTINUE
      WRITE(6,68)VB,IB,V1,ISAT,VVB,VV1
68    FORMAT(6F15.8)
      E=((VB-V1)**2)*(ISAT-IC)
      F7=((VC-V1)**2)*(ISAT-IB)
      Y=(F7*(IB+ISAT)-E*(IC+ISAT))/(2.0*ISAT*(F7-E))
      TIMES=V1/VC
      WRITE(6,16)
16    FORMAT( // 108H        E              F7             Y              TIMES
     4     S              ISAT          IC             VC             V1     )
      WRITE(6,32)E,F7,Y,TIMES,S,ISAT,IC,VC,V1
32    FORMAT( / 9F12.7 /// )
100   CONTINUE
      INDEX = 1
35    CONTINUE
      III=II
      VSAT=VDS-V
      IF (VSAT .LE. 0.0 ) GO TO 10
      A2=1.0+VSAT/KI2
      VGS2=SQRT(ABS((A2*I*2.0)/B2))+V+I*A2*RS2+K11*SQRT(ABS(QS+V+A2*I*RS
     92))+VSS
      EN=N
      SS=BSS+DIST2*EN
      IF(VGS2 .GT. SS ) GO TO 15
      IF( IND .EQ. 1 ) GO TO 15
      GO TO 30
15    EROR=ABS(VGS2-SS)
      IF(EROR .LT. 0.0005) GO TO 177
      IND=1
      IF(EROR2 .LT. EROR) GO TO 188
      EROR2=EROR
      GO TO 166
188   H=-H*0.1
      EROR2=EROR
      GO TO 166
177   IN(K,N)=I
      VGN(K,N)=VG
      VGS2N(K,N)=VGS2
      WRITE(6,92)V,III,VG,VGS2,VD,XL,A,VC,EN
92    FORMAT(9F12.3)
6     N=N+1
      IF ( N .GT. NMAX ) GO TO 10
30    CONTINUE
10    CONTINUE
      I6=I7-1
      DO 38 N=1,NMAX
      DO 23 K=2,I6
      TRANS(K,N)=(IN(K+1,N)-IN(K-1,N))/(VGN(K+1,N)-VGN(K-1,N))
      IM=IN(K,N)*1000.0
      RJ=N
      CK=K
      WRITE(6,34)IM,TRANS(K,N),VGN(K,N),VGS2N(K,N),RJ,CK
34    FORMAT(6F15.6)
```

```
23      CONTINUE
38      CONTINUE
        END
           FINIS
```

APPENDIX III

THE COMPUTER PROGRAM USED IN GENERATING THE CONVERSION TRANSCONDUCTANCE CURVES

```
      PROGRAM TST (INPUT,OUTPUT,TAPE5=INPUT,TAPE6=OUTPUT)
      DIMENSION X(61),Y(61),T(101),XA(101),YA(101),FNT(101),A(6),B(6)
C     THE DC VOLTAGE ON GATE NO 1 FOR THE FIRST TRANSCONDUCTANCE CURVE
C     IS VG1S - DTVG1                DTVG1 IS THE VOLTAGE CHANGE BETWEEN
C     CONSECUTIVE CURVES     THE LAST CURVE  WILL BE V1MAX
      VG1S =0.1
      DTVG1 =0.1
       V1MAX = -0.9
11    VG1S =VG1S -DTVG1
      IF (VG1S .LT. V1MAX ) STOP
      DO 88 I = 1,61
      VGTWO = I
88    X(I) = -2.1 + 0.1 * VGTWO
      READ(5,9)(Y(I), I=1,61 )
9     FORMAT (10F7.2)
C    THE DC VOLTAGE ON GATE NO 2 FOR THE FIRST CALCULATION IS
C     VG2S - DTVG2  DTVG2  IS THE CHANGE IN DC VOLTAGE BETWEEN CALCULATED
C       FOURIER VALUES       THE LAST VALUE WILL BE   V2MAX
      VG2S = -0.1
      DTVG2 =0.2
      V2MAX =2.0
14    VG2S =VG2S + DTVG2
      IF (VG2S .GT.  V2MAX )  GO TO 11
      WRITE ( 6 , 5 ) VG1S
5     FORMAT ( / 30H **************************,24H VOLTAGE ON GATE
     1 IS = , F6.1, 6H VOLTS, 29H**************************** / )
      WRITE (6 ,8 ) VG2S
8     FORMAT (15X, 24H VOLTAGE ON GATE 2 IS = , F6.1, 6H VOLTS  / )
      WRITE (6,13)
13    FORMAT (124H AC VG2S  ERROR  CONST                COSW      SINW
     2 COS2W    SIN2W    COS3W    SIN3W    COS4W    SIN4W    COS5W    SI
     9N5W   )
C   THE PEAK TO PEAK VALUE OF LO VOLTAGE APPLIED TO VG2S IS 2* VAC2S
C     VALUE CHANGES BY DTVAC     MAX VALUE OF VAC2S IS ACMAX
      DTVAC =0.2
      ACMAX = 2.0
      VAC2S = 0.6 -DTVAC
99    VAC2S = VAC2S  + DTVAC
      IF( VAC2S .GT. ACMAX ) GO TO 14
C    ALPHA REPRESENTS NO OF POINTS REQUIRED TO SHIFT ALL POINTS POSITIVE
      ALPHA = 21.0
      DO 12 J =1,101
      R = J
      T(J)=(-0.01 +0.01*R)
      XA(J)=VG2S +VAC2S*SIN(2.0*3.14159*T(J))
      K= XA(J)*10.0+ALPHA
      S=(Y(K)-Y(K-1))/(X(K)-X(K-1))
12    YA(J) = Y(K) + S*(XA(J)-X(K))
```

```
      DO 333 III=1,101
333   FNT(III)=YA(III)
      N=50
      M=5
      CALL FORIT (FNT,N,M,A,B,IER)
      WRITE(6,18) VAC2S,.IER,(A(J),B(J),J=1,6)
18    FORMAT(F6.1,I10,12F9.4)
      GO TO 99
      END
```