Modeling and Design of Inverters using Novel Power Loss Calculation and DC-Link Current/Voltage Ripple Estimation Methods and Bus Bar Analysis

MODELING AND DESIGN OF INVERTERS USING NOVEL POWER LOSS CALCULATION AND DC-LINK CURRENT/VOLTAGE RIPPLE ESTIMATION METHODS AND BUS BAR ANALYSIS

BY

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To my parents, Huiyi Guo and Xiaomin Zhu,

and my aunt, Yingchun Guo

Abstract

This thesis proposes novel methods and comprehensive analysis for power loss calculation, DC-link current and voltage ripple estimation, and bus bar design in two-level three-phase voltage source inverters (VSIs).

A novel method of MOSFET voltage rise- and fall-time estimations for the switching power loss calculation is developed. The estimation accuracy is significantly improved by the proposed method. In order to provide a reference for thermal management design, inverter power loss analysis is presented. Using the parameters obtained from the semiconductor device datasheets and inverter operating conditions, power loss calculations of three types of devices, namely IGBT, MOSFET, and diode, are discussed. The conduction power loss calculations for these three devices are straightforward; and, the switching power loss of IGBTs and diodes can be obtained from the energy losses given by datasheets. However, many MOSFET datasheets do not provide the switching energy losses directly. Therefore, to acquire MOSFET switching energy losses, switching transient times must be estimated as accurately as possible.

The impacts of inverter anti-parallel diode reverse recovery on the DC-link current and voltage ripples are investigated. According to the analysis, the impact of diode reverse recovery on the voltage ripple is negligible, while the RMS value of current ripple is influenced by both diode reverse recovery and inverter switching frequency.

A novel method is developed to calculate the ripple current RMS value and the estimation accuracy is significantly improved. Depending on the calculated current and voltage ripples, DC-link capacitor selection is introduced. Generally speaking, failures in the DC-link capacitors take place more frequently than the failures in other parts of the inverter system, and plenty of research has been focusing on minimizing the required DC-link capacitance. As a result, the accurate estimations of DC-link current and voltage ripples are vital in the optimization methods. In addition, with the accurate estimations, the over-design in the DC-link capacitance could be reduced.

Finally, the design of a practical bus bar is presented. The DC current distribution is affected by the numbers and locations of the DC input tabs, while the AC current distribution is influenced by the numbers and locations of the installation holes for DC-link capacitors and semiconductor devices. Furthermore, parasitic parameters of the bus bar, especially the stray inductance and voltage spikes caused by this inductance during switching turn-off transients, are also discussed from the angle of the design rules and correlation between the parameters and bus bar geometry structure. In the end, a bus bar is designed with balanced current distribution and low stray inductance.

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Notation and abbreviations

Symbol	Description	Unit
A	Bus bar cross-sectional area	mm^2
C	DC-link capacitance	μF
C_{gs}	Gate-source capacitance	nF
C_{iss}, C_{oss}, C_{rss}	Input, output, and reverse transfer capacitance	nF
D	Duty cycle	-
d	Bus bar insulation layer thickness	mm
E_{loss}	Switching energy loss	mJ
E_{on}, E_{off}	Switch turn-on and -off energy loss	mJ
$E_{on,I}$, $E_{off,I}$	IGBT turn-on and -off energy loss	mJ
$E_{on,M}$, $E_{off,M}$	MOSFET turn-on and -off energy loss	mJ
$E_{on,ref}$, $E_{off,ref}$	Testing turn-on and -off energy loss in datasheets	mJ
E_{rr}	Diode reverse recovery energy loss	mJ
$E_{rr,ref}$	Testing diode reverse recovery energy loss in datasheets	mJ
f_{sw}	Switching frequency	kHz
$I_{ave,in}$, $I_{rms,in}$	Inverter input average and RMS current	A

I_g	Gate current	A
I_{ref}	Testing current in datasheets	A
I_{rms}	Inverter output RMS current	A
$I_{rms,D}$, $I_{ave,D}$	Diode RMS and average current	A
$I_{rms,I}$, $I_{ave,I}$	IGBT RMS and average current	A
$I_{rms,M}$, $I_{ave,M}$	MOSFET RMS and average current	A
$I_{rms,ripple}$	RMS value of DC-link ripple current	A
I_{rr}	Diode reverse recovery current	A
i_a, i_b, i_c	Inverter three-phase output current	A
$i_{ave,switch}$, $i_{ave,D}$	Inverter switch and diode average current	A
i_c, i_f	IGBT collector current and diode forward current	A
i_{cap}	DC-link capacitor current	A
i_{ds}	MOSFET drain-source current	A
i_{in}, i_s	Inverter input and DC source current	A
i_o	Inverter output current	A
$i_{rms,switch}$, $i_{rms,D}$	Inverter switch and diode RMS current	A
i_{switch}, i_D	Inverter switch and diode current	A
J	Current density	A/mm^2
L_C, L_{IGBT}	Capacitor and IGBT module equivalent inductance	nH
L_{self}, L_M	Conductor self and mutual inductance	nH
L_{total}, L_{busbar}	Total equivalent and bus bar inductance	nH
l	Bus bar conductor length	mm

M	Modulation index	-
P_c, P_{sw}	Conduction and switching power loss	W
$P_{c,I}$, $P_{c,M}$, $P_{c,D}$	IGBT, MOSFET and diode conduction power loss	W
P_{loss}	Switch power loss	W
$P_{loss,inverter}$	Inverter power loss	W
Q_{rr}	Diode reverse recovery charge	nC
R_g	Gate resistance	Ω
R_I, R_M, R_D	IGBT, MOSFET and diode resistance	mΩ
$R_{th,cs}$, $R_{th,sa}$	Case-heatsink and heatsink-ambient thermal resistance	°C/W
$R_{th,ja}$, $R_{th,jc}$	Junction-ambient and junction-case thermal resistance	°C/W
S_a, S_b, S_c	Three-phase switching function	-
T_a	Ambient temperature	°C
T_j	Junction temperature	°C
T_s	Switching period/carrier period	ms
t	Bus bar conductor thickness	mm
t_a	Time interval for diode current rises from 0 to I_{rr} in the opposite direction of diode forward current	ns
t_b	Time interval for diode current falls from I_{rr} to 0 in the opposite direction of diode forward current	ns
$t_{d,on}$, $t_{d,off}$	Turn-on and -off time delay	ns
t_{ri}, t_{fi}	Current rise- and fall-time	ns
t_{rr}	Diode reverse recovery time	ns

t_{ru}, t_{fu}	Voltage rise- and fall-time	ns
$U_{0,I}$, $U_{0,D}$	IGBT and diode zero current voltage	V
U_{dc}	Inverter DC-link voltage	V
U_{ref}	Testing off-state voltage in datasheets	V
V_{drive}, $V_{dirve,n}$	Gate driver output positive and negative voltage	V
V_{peak}, V_{spike}	DC-link peak and spike voltage	V
V_{rms}	Inverter output RMS voltage	V
V_{th}, $V_{plateau}$	Threshold and plateau voltage	V
v_a, v_b, v_c	Inverter three-phase output voltage	V
v_{ce}	IGBT collector-emitter voltage	V
v_{ds}, v_{gs}	MOSFET drain-source and gate-source voltage	V
v_o	Inverter output voltage	V
w	Bus bar conductor width	mm
ΔT_{ja}, ΔT_{jc}	Junction-ambient and junction-case temperature rise	°C
ΔT_{cs}, ΔT_{sa}	Case-heatsink and heatsink-ambient temperature rise	°C
$\Delta v_{cap,T_0}$	Voltage change in T_0	V
$\Delta v_{cap,T_1}$	Voltage change in T_1	V
$\Delta v_{cap,T_2}$	Voltage change in T_2	V
$\Delta v_{cap,T_3}$	Voltage change in T_3	V
Δv_{cap}	DC-link voltage ripple	V
$\Delta v_{cap,total}$	Voltage change in T_s	V
α	Temperature coefficient of the on-state resistance	-

β	Temperature coefficient of the copper resistivity	-
δ	Skin depth	mm
ρ	Conductor resistivity	Ω·m
μ_0, μ_r	Free space and relative permeability	H/m
ε_0, ε_r	Free space and relative permittivity	F/m
$\cos\phi$	Power factor	-
AC	Alternating current	-
CR	Calculation results by the existing method	-
CRR	Calculation results by the proposed method	-
DC	Direct current	-
EMI	Electromagnetic interference	-
ER	Experimental results	-
IGBT	Insulated-gate bipolar transistor	-
MOSFET	Metal-oxide-semiconductor field-effect transistor	-
PCB	Printed circuit board	-
PWM	Pulse width modulation	-
SPWM	Sinusoidal pulse width modulation	-
SVPWM	Space vector pulse width modulation	-
THI	Third harmonic injection pulse width modulation	-
VSI	Voltage source inverter	-

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Chapter 1

Introduction

1.1 Motivations

In the past two or three decades, about two thirds of the world's electrical power is converted into mechanical power by electrical motor drive systems, in which AC power supplies play an important role. Additionally, uninterruptible power supplies are vital to some critical loads as AC sources, such as in hospitals. Due to the limited supply and global climate change issues of the fossil fuels, renewable energy became the trend in power generation. DC power is usually generated by most renewable energy sources, which leads to demands for DC-to-AC power converters (Chan, 2000; Emadi, 2005; Rashid, 2011; Ye *et al.*, 2012b).

As a result, three-phase DC-to-AC voltage source inverters are widely utilized (Koutroulis *et al.*, 2001; Shin *et al.*, 2012; Mutlag *et al.*, 2013; Vasquez *et al.*, 2013). DC voltages are converted to AC voltages by inverters that are commonly utilized to interface DC sources to loads (Ebad and Song, 2012; Adekol *et al.*, 2016). Meanwhile, the amplitude and frequency of output AC voltages can be regulated depending on

the demands of loads (Rajpriya *et al.*, 2013). A typical topology of a two level three-phase voltage source inverter is shown in Figure 1.1 (Koushki *et al.*, 2008; Ozkan and Hava, 2014), in which various types of DC sources, such as solar panels, fuel cells, batteries, DC-DC converters, and AC-DC rectifiers, can be used as the DC input of the inverter (Selamogullari *et al.*, 2010; Bhutia *et al.*, 2014).

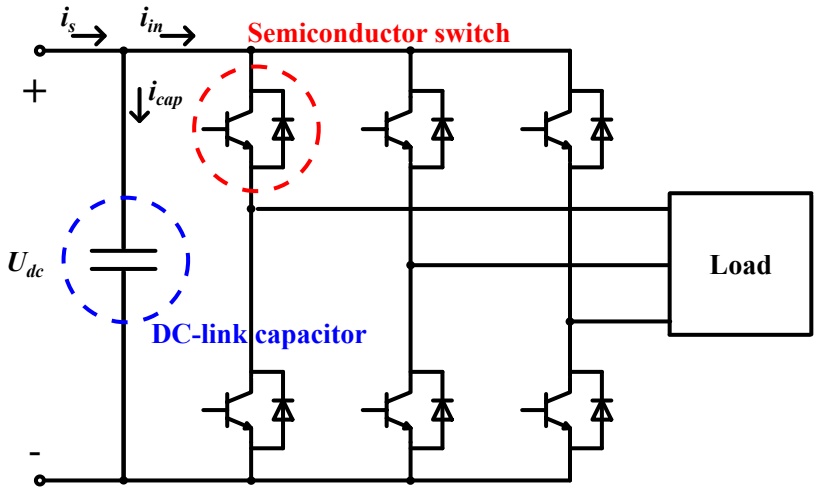


Figure 1.1: Topology of three-phase two level voltage source inverter.

The inverter design generally includes several steps: (1) semiconductor device selection; (2) power loss calculation and thermal management system selection; (3) DC-link current and voltage ripple estimation and DC-link capacitor selection; (4) bus bar design and analysis.

Step 1: semiconductor device selection. Appropriate semiconductor switches should be selected for the inverter system according to anticipated operating conditions. Among the parameters that must be considered, voltage and current ratings of the devices are the most important ones. As it is shown in Figure 1.1, there are three phase legs in the inverter; each phase leg contains an upper and a lower switch that are turned on and off alternately. In addition, a diode is anti-parallel to each

switch. To prevent the DC source from being shorted, upper and lower switch or diode do not conduct at the same time during operation. If the upper switch or diode is on, the lower switch or diode is off, and vice versa. As a result, the switch and diode should be able to sustain the DC-link voltage when they are off, based on which the voltage rating of the device can be determined. According to the system requirements, a method provided in (Backlund *et al.*, 2009) presents how the voltage rating is decided. However, the voltage rating is usually selected based on experiences. Considering spikes, the voltage rating is commonly chosen about 1.5 to 2 times as the required amount in circuits. An example is provided in (Zdanowski *et al.*, 2016). Similarly, current ratings can also be selected by this empirical method depending on the peak value of inverter output current. Besides, attention must also be paid to some other parameters of the semiconductor device module, such as equivalent resistance, equivalent inductance, switching energy loss and time. High power losses are generated by large module equivalent resistance, long switching time and high switching energy loss. Meanwhile, the module's equivalent inductance will contribute to the total stray inductance in the circuit, which results in voltage spikes during switch turn-off transients. Therefore, relatively small values of those parameters are preferred.

Step 2: power loss calculation and thermal management system selection. The inverter power loss is estimated, based on which the thermal management system is selected. Inverter power loss consists of conduction and switching power losses. It is known that when there is current through and voltage across a component in a circuit, power losses are generated. The conduction power loss denotes the power losses generated when a semiconductor device is on, while the switching power

loss indicates the power losses generated during switching transients. In a certain device, higher current, voltage, and switching transient time lead to higher power losses. Generally speaking, it is assumed that the total amount of power losses in six switches and six diodes are equivalent to the inverter power losses. During the inverter operation, the power losses transfer to heat and cause temperature rise of the device. In this case, a thermal management system is needed to control the device temperature under a reasonable level. The temperature rise is estimated by the power losses, and the thermal management system is selected based on this temperature rise and maximum allowable device temperature.

Step 3: DC-link current and voltage ripple estimation and DC-link capacitor selection. The DC-link capacitors are selected by evaluating the DC-link current and voltage ripples. The requirements of DC-link voltage ripple in inverter systems are generally in the range of 5% to 10% (Rashid, 2011). The capacitance required in the DC-link is usually determined by the DC-link voltage and the voltage ripple. On the other hand, the RMS value of DC-link current ripple is utilized to determine the current rating of the capacitor, since the DC-link current ripple component is equivalent to the current flowing through DC-link capacitors. When the current flows through a DC-link capacitor, a small amount of power losses are generated and the temperature rise occurs. A current higher than the current rating of the capacitor might cause overheat and shorter life time of the capacitor.

Step 4: bus bar design and analysis. To connect each power component included in the inverter, various connectors can be used, such as cables, PCBs, and bus bars. The usage of cables results in large stray inductance and high voltage spike, which

increases the voltage stress on semiconductors. Furthermore, the complexity in assembly is another drawback of utilizing cables. Thus, PCBs and bus bars are commonly used. Due to the limitation in current carrying capability and flat structure, PCBs are suitable for low power applications. In high power applications, to carry more current, using bus bars is a better choice. Having large module packages, the power components used in high power applications can be more easily connected by bus bars rather than PCBs. The bus bar design is more complicated than PCB design, since there might be significant differences in the performances of bus bars with different geometrical dimensions. As a result, efforts are mainly spent on bus bar design. With selected semiconductor devices, thermal management system, and DC-link capacitors, the configuration of the inverter can be preliminarily designed. Then, bus bar is designed by taking the packages and locations of semiconductor devices and DC-link capacitors into account; and the finite element analysis is employed to evaluate the bus bar performance before manufacturing.

Various inverter design methods can be implemented to achieve different objectives (Wei *et al.*, 2010). To increase power density of an inverter system, some methods are developed for size and weight minimization (Itoh *et al.*, 2016; Nawawi *et al.*, 2016; Ye *et al.*, 2012a). To improve the inverter efficiency, the power loss is minimized in (Fateh and Gruenbacher, 2014; Amorndechaphon, 2016). Some of the optimization methods are discussed in (Abrishamifar *et al.*, 2010; Enjeti and Shireen, 1992; Nguyen *et al.*, 2014) to achieve small voltage spike, DC-link current and voltage ripples. Additionally, the reliability of an inverter system is also important and improved in (Ye, 2014).

The implementations of most optimization methods rely on the accurate estimations of the inverter performances. Therefore, the estimation accuracies of power loss, DC-link current and voltage ripple, and bus bar performances are crucial in inverter design. However, there are still improvements that are demanded in those estimations.

Therefore, this thesis presents the improvements achieved in the estimations of inverter power loss, DC-link current and voltage ripples; in addition, it also demonstrates the design and analysis of a bus bar.

1.2 Contributions

The author has contributed to comprehensive analysis and design of three-phase voltage source inverters by introducing original developments and novel approaches in power loss estimation, DC-link current and voltage analysis, and bus bar design.

On one hand, power loss estimation plays an important role in the development of optimization methods for power loss minimization and thermal management design that directly affects the volume and weight of inverter systems. Numerical simulation based on the physical model of the semiconductor devices and inverter system is a solution to predict the inverter power losses accurately; however, this method is complicated and time consuming (Bierhoff and Fuchs, 2004; Zou and Zhao, 2013). An alternative way is to estimate the power losses based on the semiconductor datasheets; in this case, calculations are simplified. Nevertheless, some parameters that are used to estimate the MOSFET switching transient times and switching power loss are provided by datasheets in the form of logarithm plots and vary dramatically. To utilize these parameters in switching power loss calculations, both existing and proposed

methods are included in this thesis.

- In some prior studies, approximations are made and an equivalent value is selected to denote the highly nonlinear parameter, MOSFET reverse transfer capacitance. It is obvious that a single value cannot accurately present this kind of parameter during the entire switching transition; thus, the accuracy of switching power loss calculation cannot be guaranteed.

- In this thesis, MOSFET switching transients are analyzed in detail; and, a method is proposed to accurately estimate MOSFET switching transient times, especially voltage rise- and fall-time. The entire switching transition is divided into a group of time intervals, and the nonlinear parameter in each time interval is considered constant when the period is small enough. The length of each time interval is calculated individually, and the entire period is obtained by the sum of all time intervals. With this proposed method, the estimation accuracy of these transient times are significantly improved.

On the other hand, the DC-link current and voltage ripple estimations influence the DC-link capacitor selection, which is also related to the inverter size and weight minimization.

- Most of the prior works related to DC-link current and voltage ripple estimation have been done with the assumption that inverter input current is ideal. In other words, the current spikes that are caused by inverter anti-parallel diode reverse recovery are neglected in the calculations. However, diode reverse recovery current does contribute to the inverter input current. Therefore, it is possible to estimate the DC-link current and voltage ripples more accurately by considering the diode reverse recovery.

- In this thesis, proposed method for DC-link current and its ripple component as well as voltage ripple evaluations are developed. In the proposed method, the occurrence of inverter anti-parallel diode reverse recovery is analyzed within the switching period. Then, the inverter input current is described by considering the anti-parallel diode reverse recovery, based on which the DC-link current is represented by the switching functions and the inverter three phase output currents. Furthermore, the DC-link current and voltage ripples are evaluated by the proposed method. Expressions are derived for current and voltage ripple calculations, and it is mathematically proved that the RMS value of ripple current is irrelevant to the type of PWM technique. The accuracy of the DC-link ripple current RMS value estimation is improved by the proposed method by up to 7%. Besides, the proposed method proves that the RMS value of DC-link ripple current is an inverter switching frequency-dependent parameter. As the switching frequency increases, the ripple current RMS value grows; at the same time, there is no significant difference in the estimation accuracy by the proposed method under different switching frequency. In contrast, the DC-link voltage ripple is not considerably influenced by the diode reverse recovery according to the analysis.

Furthermore, to enhance the reliability of the entire inverter system, the performances of bus bars are also evaluated. Current distribution on the bus bar directly affects the current sharing among DC-link capacitors and inverter output terminals. When more than one capacitor is used in the DC-link, imbalanced current sharing may lead to a shorter life time of the capacitor that carries more current. For different inverter systems, bus bar designs are distinct; to design a bus bar with balanced

current distribution and low stray impedance, especially low stray inductance, is a challenge in each inverter design. However, few studies provide comprehensive analysis in bus bar design and analysis.

- In this thesis, a practical bus bar is designed with balanced current distribution and low stray impedance for an inverter system. Depending on the finite element analysis in simulations and the experimental results, a conclusion obtained during the design is that the DC current distribution on the bus bar is influenced by the numbers and locations of the DC input tabs; however, the AC current distribution is not affected by the DC input tabs and it is related to the numbers and locations of the installation holes for DC-link capacitors and semiconductors. A balanced current distribution is acquired in the design and it is experimentally verified by measuring the RMS current in each DC-link capacitor. The maximum difference in DC-link capacitor RMS currents is defined as "Max diff.", and the maximum and minimum values of "Max diff." obtained by experiments are 8.8% and 1.3%. In addition, low stray inductance is achieved in the design, which leads to relatively low voltage spike during semiconductor device turn-off transients. The amount of voltage spike is estimated by using the predicted stray inductance from the simulation; comparing to the experimental results, the maximum and minimum voltage spike estimation errors are 9.97% and 2.65%.

1.3 Thesis Outline

The comprehensive analysis and design for three-phase voltage source inverters are demonstrated in this thesis and its outline is illustrated as follows.

Chapter 2 briefly presents inverter power loss calculations. For conduction power losses, calculation methods based on different semiconductor devices, IGBTs, MOSFETs and diodes, are presented; and the average and RMS values of current through semiconductors and anti-parallel diodes during the operation of the inverter are derived. For switching power losses, the MOSFET switching transients are analyzed in detail, including current and voltage variation trends, equivalent circuits, and transient time period estimation. The novel method for MOSFET voltage rise- and fall-time calculation is addressed. Considering the variation of current and voltage, MOSFET switching power loss calculations are demonstrated by utilizing the estimated time periods. On the other hand, the estimation methods for switching power losses of IGBT and diode are introduced based on the losses information given by datasheets. Furthermore, the correlation between inverter power loss and thermal management system is also illustrated, according to which the inverter capability is discussed from the point of the thermal limitation.

Chapter 3 presents the evaluations of DC-link current and voltage ripples as well as the rules for DC-link capacitor selection. A general overview of three typical PWM techniques is introduced in the beginning. Then, considering each type of PWM technique, four time intervals within the switching period that are related to the duty cycle are derived. The existing solution, in which the inverter input current is assumed ideal, is described for current and voltage ripple calculations. Nevertheless, the inverter input current is defined by not only the inverter switching functions and output current but also the anti-parallel diode reverse recovery. To improve the estimation accuracy of DC-link current and voltage ripples, the proposed method is developed by considering the diode reverse recovery. The diode reverse

recovery is reviewed and introduced, and the occurrence of reverse recovery within the switching period is determined by analyzing the inverter current flow in detail. After that, the inverter input current is represented by several parameters including switching functions, output current, reverse recovery time and current. With the consideration of diode reverse recovery, the switching frequency appears in the final expression. As a result, it is shown that the DC-link current and its ripple component are switching frequency dependent parameters. While, the DC-link voltage ripple is not significantly affected by the diode reverse recovery. Then the selection of DC-link capacitor is briefly presented in the end of this chapter.

Chapter 4 discusses the bus bar design and analysis based upon a practical designed bus bar for an inverter. Design rules are illustrated by both mathematical analysis and simulation results. DC and AC analysis utilized in the simulations are introduced firstly. Then the DC and AC current density and distribution are evaluated for an initial design. Due to the imbalance in DC current distribution shown by the simulation results, a revised design is demonstrated that achieves balanced current distribution in both DC and AC current on the bus bar. Besides, the relationship between the bus bar geometrical dimensions and the values of stray parameters, including resistance, inductance, and capacitance, is presented; and the bus bar estimated stray parameters of the final design are also shown in this chapter. In the end, with the analysis of current flow in the circuit during switch turn-off transient, the solution for voltage spike calculation is described.

Chapter 5 provides experimental verifications for the analysis in previous chapters. The comparison between the results from analytical calculations and experiments is made. Discussions based upon the results are also addressed.

Finally, conclusions are drawn and future works are illustrated in Chapter 6.

1.4 Thesis Publications

Journal papers

- J. Guo, J. Ye, and A. Emadi, "DC-link current and voltage analysis considering anti-parallel diode reverse recovery in voltage source inverters," *IEEE Transactions on Power Electronics* (Submitted).
- J. Guo, J. Ye, and A. Emadi, "Three-phase voltage source inverter design: a practical guidance," *IEEE Journal of Emerging and Selected Topics in Power Electronics* (Submitted).
- A. D. Callegaro, J. Guo, M. Eull, B. Danen, J. Gibson, M. Preindl, B. Bilgin, and A. Emadi, "Bus bar design for high-power inverters," *IEEE Transactions on Power Electronics* (Submitted).

Book chapters

- R. Hou, J. Guo, L. Dorn-Gomba, and A. Emadi, *Chapter 23: Power Electronics Systems and Control in Automobiles, in Control of Power Electronic Converters and Systems, Edited by F. Blaabjerg*, Amsterdam, Netherlands: Elsevier (To be published).

Conference papers

- J. Guo, H. Ge, J. Ye, and A. Emadi, "Improved method for MOSFET voltage rise-time and fall-time estimation in inverter switching loss calculation," In *Proc.*

IEEE Transportation Electrification Conference and Expo (ITEC), Dearborn, MI, June 2015, pp. 1-6.

- J. Guo and A. Emadi,"DC-link current ripple component RMS value estimation considering anti-parallel diode reverse recovery in voltage source inverters," In *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, September 2016, pp. 1-6.

- K. Yang, J. Guo, H. Ge, B. Bilgin, V. Loukanov, and A. Emadi, "Transient electro-thermal analysis for a MOSFET based traction inverter," In *Proc. IEEE Transportation Electrification Conference and Expo (ITEC)*, Dearborn, MI, June 2014, pp. 1-6.

- H. Ge, J. Guo, B. Bilgin, J. Ye, and A. Emadi, "A reduced-order model based induction machine self-commissioning method," In *Proc. IEEE Transportation Electrification Conference and Expo (ITEC)*, Dearborn, MI, June 2015, pp. 1-6.

Chapter 2

Power Loss Calculation and Thermal Management Selection

Power loss calculation of semiconductor devices and inverters is important since it predicts the inverter efficiency and provides a reference for the thermal management system selection. Unnecessary over-design can be avoided by accurate power loss estimation (Zou and Chen, 2014). Once a certain semiconductor device is selected, the inverter power loss and thermal management system can be calculated and selected depending on the parameters provided by device datasheets and operating conditions of the inverter. Both conduction power losses and switching power losses should be considered. Power loss calculation for inverter and three types of commonly used semiconductor devices, i.e. MOSFETs, IGBTs and diodes, is introduced.

Utilizing the information given in datasheets, such as on-state resistance and switching energy losses, the conduction and switching power losses can be calculated according to the inverter operating conditions. Nevertheless, different from the switching power loss estimation of IGBTs and diodes, most MOSFET datasheets

provide inherent capacitances instead of switching energy losses; thus, switching time calculations are needed to obtain the MOSFET switching energy and power losses. An existing method is provided in (Graovac *et al.*, 2006) for estimation of the MOSFET switching transient times. The estimation accuracy of voltage rise- and fall-time is restricted by the nonlinear variation of MOSFET inherent capacitances. Therefore, a method is proposed in this chapter to improve the estimation accuracy.

In this chapter, power loss calculations for semiconductor three devices, namely MOSFETs, IGBTs, and diodes, are illustrated in Section 2.1, in which both the existing and proposed methods are discussed for the MOSFET voltage rise- and fall-time estimation. In Section 2.2, inverter power losses are derived by considering the inverter operating conditions. Then, the correlation between the inverter power losses and the thermal management system selection is addressed in Section 2.3. In addition, the power capability of the inverter is also discussed. Finally, a summary is given in Section 2.4.

2.1 Power Losses in Switching Devices

The power loss, P_{loss}, of a semiconductor device consists of the conduction power loss, P_c, and switching power loss, P_{sw}. Based on distinct manufacturing techniques, an on-state MOSFET is equivalent to a resistor whereas an IGBT or a diode can be presented by a resistor connected in series with a DC voltage source (Baliga, 2008; Rashid, 2011). Thus, the calculation for MOSFET conduction power loss, $P_{c,M}$, is different from that for IGBT conduction power loss, $P_{c,I}$, and diode conduction power loss, $P_{c,D}$. In contrast, the switching power loss evaluation for these three devices are similar to each other.

Nevertheless, compared with conduction power loss, switching power loss calculation is more complicated. That is because switching energy loss E_{loss} of the device in T_s should be acquired before P_{sw} can be calculated. The solution for acquiring E_{on} and E_{off} may vary depending on the information given by manufacturer datasheets. Although, a lot of datasheets provide E_{on} and E_{off} values under various testing conditions, those values can rarely be directly utilized in calculations; since, the actual inverter operating conditions are usually different from the testing conditions. Additionally, most MOSFET datasheets provide values of the MOSFET inherent capacitances such as, C_{iss}, C_{oss} and C_{rss}, instead of E_{on} and E_{off}; as a result, E_{on} and E_{off} have to be calculated from those capacitances and the MOSFET switching times.

In the following sections, the calculation method for P_c and E_{loss} for MOSFETs, IGBTs, and diodes are discussed.

2.1.1 MOSFET power losses

For MOSFETs, the conduction power loss calculation is more straightforward and easier than switching power loss calculation.

MOSFET conduction power losses

When a MOSFET is conducting, the switch acts as a resistor whose resistance varies along with the junction temperature, T_j. Figure 2.1 shows the equivalent circuit of an on-state MOSFET.

The MOSFET on-state resistance varies along with the junction temperature, T_j. The value of R_M increases when T_j rises; and various values of R_M under different T_j

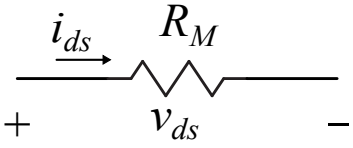


Figure 2.1: Equivalent circuit of an on-state MOSFET.

are provided in datasheets. With the resistance under 25°C junction temperature, R_M is expressed by (2.1), where α is the temperature coefficient and can be calculated by two points on the curve of R_M versus T_j given in datasheets (Huang, 2012). According to (Tiwari *et al.*, 2016), the on-state resistance of a MOSFET can increase by 57.6% when its junction temperature rises from the room temperature to 125°C. The values of R_M under different T_j are also given by datasheets, thus an appropriate value should be used in the conduction power loss calculations by taking the actual operating junction temperature into account.

$$R_M\left(T_j\right) = R_M\left(25^{\circ}\mathrm{C}\right) \cdot \left(1 + \frac{\alpha}{100}\right)^{\left(T_j - 25^{\circ}\mathrm{C}\right)} \tag{2.1}$$

Then, the conduction power loss calculation of a MOSFET, $P_{c,M}$, is similar to that of a resistor. Then, $P_{c,M}$ is represented by (2.2) (Hossain and Reis, 2008).

$$P_{c,M} = {I^2}_{rms,M} \cdot R_M \tag{2.2}$$

With increasing switching frequency, current, or voltage in the inverter, it is possible that the switching power loss gradually dominates the total power loss (Xiong *et al.*, 2009). Therefore, a great deal of efforts are also spent on switching power loss calculation. Compared with the experiment and modeling, the method that calculates power losses based on product datasheets is relatively quick and straightforward. The

switching power loss is usually calculated by the product of switching energy loss and inverter switching frequency; however, there are not many MOSFET datasheets that provide switching energy losses directly. Usually, MOSFET inherent capacitances are provided; and using these capacitances given by datasheets, MOSFET switching transient time can be estimated (Raee *et al.*, 2013; Lirio *et al.*, 2015). Then the switching power losses can be calculated accordingly. In the following part of this section, the MOSFET switching behavior is analyzed before power loss calculation is discussed.

MOSFET switching behavior

To understand the switching behavior of the MOSFET, waveforms of the MOSFET drain-source voltage and current (v_{ds} and i_{ds}) as well as gate-source voltage (v_{gs}) are analyzed. MOSFETs are voltage-driven devices (Hart, 2011) and an equivalent circuit of the MOSFET with its gate driver is shown in Figure 2.2.

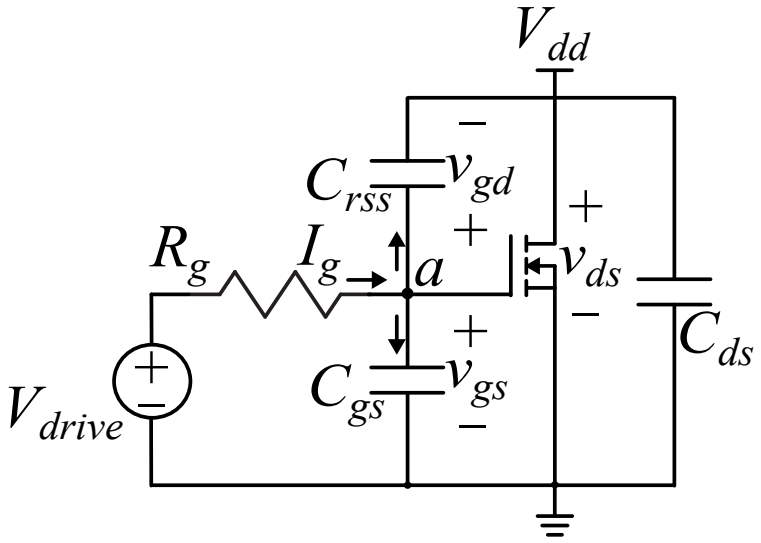
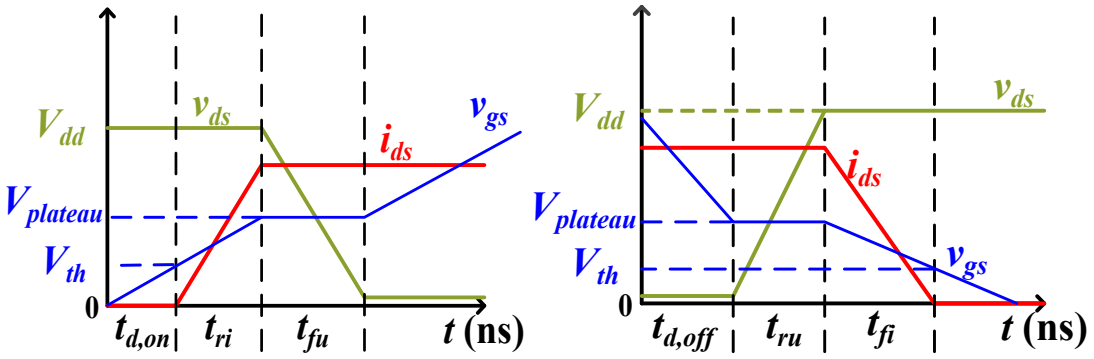


Figure 2.2: Equivalent circuit of the MOSFET with its gate driver.

Usually a gate driver is designed to provide a voltage (V_{drive}) across the MOSFET gate and source terminal to turn on or off the switch. The value of V_{drive} required by various MOSFETs are different. In most datasheets, the value of V_{drive} is suggested between ±20V. On one hand, zero or a negative value is supplied to turn off the switch or to keep the switch in off-state. On the other hand, a positive value is used to turn on the switch or to keep the switch in on-state. There is a threshold voltage (V_{th}) for each switch and the positive V_{drive} should be larger than V_{th} to turn the switch on.

Ideal waveforms of v_{gs}, v_{ds} and i_{ds} during the switching transitions are shown in Figure 2.3 (Sanjeev and Jain, 2013), in which V_{drive} is assumed at 0V when the MOSFET is off. In (Sivkov *et al.*, 2015), the waveforms during practical operation of a MOSFET-based inverter are analyzed. When the MOSFET is in off-state, v_{ds} is kept at the value of the inverter DC-link voltage and i_{ds} is equal to zero; meanwhile, v_{gs} is also zero. After the MOSFET is turned on, v_{ds} drops to its on-state voltage that is usually several volts and i_{ds} is equal to the current value that is defined by the load; at the same time, the value of v_{gs} is positive and it is determined by the gate driver output voltage. There are six important time intervals, $t_{d,on}$, $t_{d,off}$, t_{ri}, t_{fu}, t_{fi}, and t_{ru}, the last four of them play an important role in MOSFET switching power loss calculation. These six time intervals are derived by analyzing MOSFET equivalent circuit during switching transitions.

The MOSFET turn-on transition is discussed based on Figure 2.3a. The effect caused by the inverter anti-parallel diode's reverse recovery and the voltage spike are ignored in the analysis of the MOSFET switching transitions. When the MOSFET is being turned on, v_{gs} starts to increase. Before v_{gs} becomes equal to or larger than V_{th},



(a) Turn-on transition. (b) Turn-off transition.

Figure 2.3: MOSFET current and voltage waveforms during switching transitions.

the switch is still in its off-state. There is no current flowing through the switch and only the MOSFET's gate-source capacitor C_{gs} is being charged. At this moment, the switch is open and a simplified circuit is presented by Figure 2.4. It can be seen that V_{drive} is supplied to the MOSFET's gate and source terminals through a gate resistor R_g. In this case, a gate current I_g flows into C_{gs} and it can be expressed by both (2.3) and (2.4). Then by canceling I_g in (2.3) and (2.4), an equation demonstrating the relationship between time t and v_{gs} is obtained in (2.5).

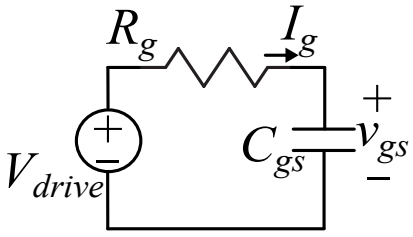


Figure 2.4: Equivalent circuit of the MOSFET with its gate driver during $t_{d,on}$.

$$I_g = \frac{V_{drive} - v_{gs}}{R_g} \tag{2.3}$$

$$I_g = C_{gs} \cdot \frac{\mathrm{d}v_{gs}}{\mathrm{d}t} \tag{2.4}$$

$$\frac{V_{drive} - v_{gs}}{R_g} = C_{gs} \cdot \frac{\mathrm{d}v_{gs}}{\mathrm{d}t} \tag{2.5}$$

According to Figure 2.3a and Figure 2.4, before v_{gs} reaches the value of V_{th}, (2.5) can be rewritten and solved in (2.6) to (2.8). The time for v_{gs} rising from zero to V_{th} is called turn-on time delay $t_{d,on}$.

$$\frac{1}{R_g \cdot C_{gs}} \cdot \mathrm{d}t = \frac{1}{V_{drive} - v_{gs}} \cdot \mathrm{d}v_{gs} \tag{2.6}$$

$$\int_0^{t_{d,on}} \frac{1}{R_g \cdot C_{gs}} \cdot \mathrm{d}t = \int_0^{V_{th}} \frac{1}{V_{drive} - v_{gs}} \cdot \mathrm{d}v_{gs} \tag{2.7}$$

$$t_{d,on} = R_g \cdot C_{gs} \cdot \ln \frac{V_{drive}}{V_{drive} - V_{th}} \tag{2.8}$$

After v_{gs} increases to V_{th}, the switch starts to conduct and i_{ds} begins to rise. During the period when i_{ds} is rising, v_{gs} varies from V_{th} to $V_{plateau}$; this period is named as current rise-time. At this moment, the current going through the switch i_{ds} changes from zero to a desired current value depending on the load requirement; and v_{ds} is kept at $V_{dd} = U_{dc}$. A MOSFET behaves as a resistor during its on-state period, thus the MOSFET equivalent circuit can be simplified and is given in Figure 2.5. It is obvious that during t_{ri}, not only is C_{gs} being charged, but also the MOSFET reverse transfer capacitor C_{rss} is being charged as well. The calculation for t_{ri} is derived by

solving the simplified circuit shown in Figure 2.5. The Kirchhoff's current law can be applied to node "a", as shown in (2.9).

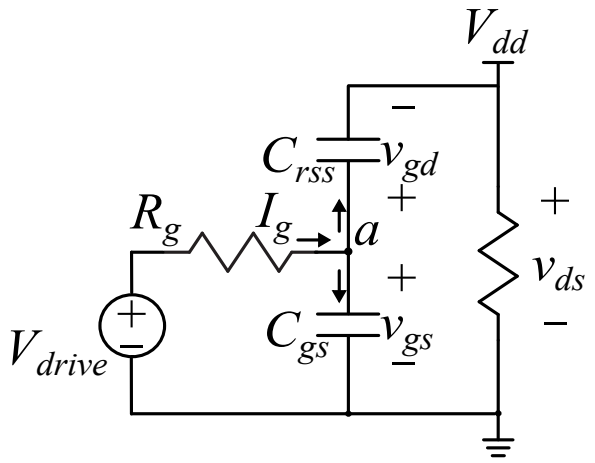


Figure 2.5: Equivalent circuit of the MOSFET with its gate driver during t_{ri} or t_{fi}.

$$\frac{V_{drive} - v_{gs}}{R_g} = C_{gs} \cdot \frac{\mathrm{d}v_{gs}}{\mathrm{d}t} + C_{rss} \cdot \frac{\mathrm{d}(v_{gs} - v_{ds})}{\mathrm{d}t} \tag{2.9}$$

As v_{ds} is constant during t_{ri}, the derivative of v_{ds} with respect to t is equal to zero; then the relationship between v_{gs} and t is finally acquired in (2.10).

$$\frac{1}{R_g \cdot (C_{gs} + C_{rss})} \cdot \mathrm{d}t = \frac{1}{V_{drive} - v_{gs}} \cdot \mathrm{d}v_{gs} \tag{2.10}$$

The sum of C_{gs} and C_{rss} is the MOSFET input capacitance and can be represented in (2.11).

$$C_{iss} = C_{gs} + C_{rss} \tag{2.11}$$

Then, t_{ri} can be calculated by (2.12) and (2.13).

$$\int_{t_{d,on}}^{(t_{d,on}+t_{ri})} \frac{1}{R_g \cdot C_{iss}} \cdot \mathrm{d}t = \int_{V_{th}}^{V_{plateau}} \frac{1}{V_{drive} - v_{gs}} \cdot \mathrm{d}v_{gs} \tag{2.12}$$

$$t_{ri} = R_g \cdot C_{iss} \cdot \ln \frac{V_{drive} - V_{th}}{V_{drive} - V_{plateau}} \tag{2.13}$$

Once v_{gs} reaches the value of $V_{plateau}$, i_{ds} also rises to the load current level at the same time. Then, v_{ds} starts to fall from off-state value to on-state value. As it has been mentioned, in two-level inverter systems the off-state value of v_{ds} is the DC-link voltage U_{dc}; meanwhile, the MOSFET on-state voltage is equal to the value of R_M multiplying by the current through the switch. The time for v_{ds} falling is t_{fu} that is also shown in Figure 2.3a, which also indicates that v_{gs} and i_{ds} are kept constant at the value of $V_{plateau}$ and load current respectively during t_{fu}. Thus, only C_{rss} is being charged at this moment. It is well known that the currents going into both input terminals of an amplifier are equal to zero; and the voltage across two input terminals are negligibly small, which implies that the potentials of these two terminal with respect to the ground are same (Alexander and Sadiku, 2007). Therefore, it can be assumed that the MOSFET behaves as an ideal amplifier during t_{fu}, whose equivalent circuit is shown in Figure 2.6 (Brown, 2004).

Similarly to the derivation of t_{ri}, the calculation of t_{fu} also starts with solving the equivalent circuit. According to Figure 2.6, the amount of current going through C_{rss} is equal to the gate current I_g through R_g; in addition, the voltage across node "a" and ground is equal to v_{gs} whose value is constant at $V_{plateau}$. Thus, I_g can be expressed by both (2.14) and (2.15); as a result, the relationship between v_{ds} and t is indicated in (2.16).

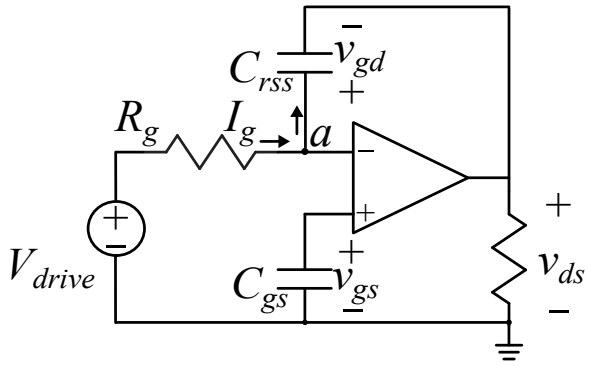


Figure 2.6: Equivalent circuit of the MOSFET with its gate driver during t_{ru} or t_{fu}.

$$I_g = \frac{V_{drive} - V_{plateau}}{R_g} \tag{2.14}$$

$$I_g = C_{rss} \cdot \frac{\mathrm{d}(V_{plateau} - v_{ds})}{\mathrm{d}t} \tag{2.15}$$

$$\frac{V_{drive} - V_{plateau}}{R_g} = C_{rss} \cdot \frac{\mathrm{d}(V_{plateau} - v_{ds})}{\mathrm{d}t} \tag{2.16}$$

Based on the expression given in (2.16), t_{fu} can be calculated by (2.17) to (2.19).

$$\frac{1}{R_g \cdot C_{rss}} \cdot \mathrm{d}t = -\frac{1}{V_{drive} - V_{plateau}} \cdot \mathrm{d}v_{ds} \tag{2.17}$$

$$\int_{(t_{d,on}+t_{ri})}^{(t_{d,on}+t_{ri}+t_{fu})} \frac{1}{R_g \cdot C_{rss}} \cdot \mathrm{d}t = -\int_{U_{dc}}^{R_M \cdot i_{ds}} \frac{1}{V_{drive} - V_{plateau}} \cdot \mathrm{d}v_{ds} \tag{2.18}$$

$$t_{fu} = (U_{dc} - R_M \cdot i_{ds}) \cdot R_g \cdot C_{rss} \cdot \frac{1}{V_{drive} - V_{plateau}} \tag{2.19}$$

Then, when v_{ds} falls to the MOSFET on-state value, the switching transition that influence MOSFET switching power loss ends and the switch is completely turned on. After that, v_{gs} keeps rising from $V_{plateau}$ until it reaches the value of V_{drive}. The output voltage of the gate driver V_{drive} is usually designed higher than $V_{plateau}$.

When the MOSFET is being turned off, waveforms of v_{ds}, i_{ds}, and v_{gs} are shown by Figure 2.3b. Before the MOSFET is turned off, v_{ds} is equal to on-state voltage that is $R_M \cdot i_{ds}$; i_{ds} is at the load current level and v_{gs} is positive. To turn off the switch, a zero voltage or a negative voltage is provided to the MOSFET gate and source terminal. According to Figure 2.3b, there is a turn-off time delay $t_{d,off}$. During this time period $t_{d,off}$, v_{gs} falls from V_{drive} to $V_{plateau}$, while v_{ds} and i_{ds} are kept at the on-state values. The equivalent circuit is shown in Figure 2.7.

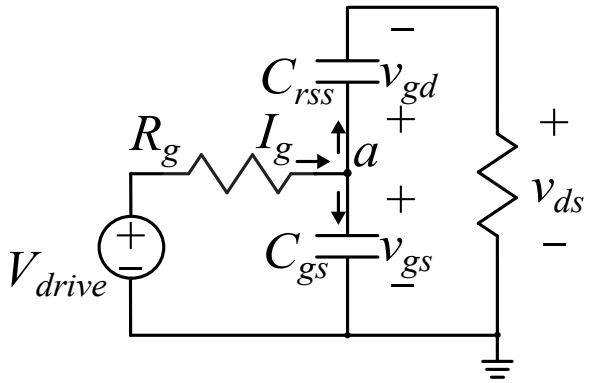


Figure 2.7: Equivalent circuit of the MOSFET with its gate driver during $t_{d,off}$.

Applying the Kirchhoff's current law at node "a", the relationship among I_g and currents through C_{gs} and C_{rss} can be found in (2.20).

$$I_g = \frac{V_{drive} - v_{gs}}{R_g} = C_{gs} \cdot \frac{\mathrm{d}v_{gs}}{\mathrm{d}t} + C_{rss} \cdot \frac{\mathrm{d}v_{gd}}{\mathrm{d}t} \tag{2.20}$$

It should be noticed that during turn-off transition, depending on the current

direction described in Figure 2.7, the gate current is negative and C_{gs} and C_{rss} are discharged. Thus, with a negative value of V_{drive} all of three terms in (2.20) are negative. With constant values of v_{ds} and i_{ds}, $t_{d,off}$ can be acquired by (2.21) to (2.24), where V_{drive} always indicates the positive value of V_{drive} and $V_{drive,n}$ denotes the negative value of V_{drive}.

$$v_{gd} = v_{gs} - v_{ds} \tag{2.21}$$

$$\frac{1}{R_g \cdot C_{iss}} \cdot \mathrm{d}t = \frac{1}{V_{drive,n} - v_{gs}} \cdot \mathrm{d}v_{gs} \tag{2.22}$$

$$\int_0^{t_{d,off}} \frac{1}{R_g \cdot C_{iss}} \cdot \mathrm{d}t = \int_{V_{drive}}^{V_{plateau}} \frac{1}{V_{drive,n} - v_{gs}} \cdot \mathrm{d}v_{gs} \tag{2.23}$$

$$t_{d,off} = R_g \cdot C_{iss} \ln \frac{V_{drive} - V_{drive,n}}{v_{plateau} - V_{drive,n}} \tag{2.24}$$

After v_{gs} falls to $V_{plateau}$, v_{ds} starts to rise. During this time, v_{gs} is constant at the value of $V_{plateau}$ and i_{ds} is also kept as load current. The time period for v_{ds} increasing from $R_M \cdot i_{ds}$ to U_{dc} is denoted by t_{ru}. The equivalent circuit during t_{ru} is same as that during t_{fu}, seen in Figure 2.6. At this moment, there is no current flowing through C_{gs} and C_{rss} is being discharged. The currents flowing in both R_g and C_{rss} are negative depending on the directions given in Figure 2.6. By solving the equivalent circuit, t_{ru} can be obtained by (2.25) to (2.30).

$$I_g = \frac{V_{drive,n} - V_{plateau}}{R_g} \tag{2.25}$$

$$I_g = C_{rss} \cdot \frac{\mathrm{d}(V_{plateau} - v_{ds})}{\mathrm{d}t} \tag{2.26}$$

$$\frac{V_{drive,n} - V_{plateau}}{R_g} = C_{rss} \cdot \frac{\mathrm{d}(V_{plateau} - v_{ds})}{\mathrm{d}t} \tag{2.27}$$

$$\frac{1}{R_g \cdot C_{rss}} \cdot \mathrm{d}t = -\frac{1}{V_{drive,n} - V_{plateau}} \cdot \mathrm{d}v_{ds} \tag{2.28}$$

$$\int_{t_{d,off}}^{(t_{d,off}+t_{ru})} \frac{1}{R_g \cdot C_{rss}} \cdot \mathrm{d}t = -\int_{R_M \cdot i_{ds}}^{U_{dc}} \frac{1}{V_{drive,n} - V_{plateau}} \cdot \mathrm{d}v_{ds} \tag{2.29}$$

$$t_{ru} = (U_{dc} - R_M \cdot i_{ds}) \cdot R_g \cdot C_{rss} \cdot \frac{1}{V_{plateau} - V_{drive,n}} \tag{2.30}$$

When v_{ds} reaches U_{dc}, i_{ds} drops in the following time period t_{fi}. The simplified equivalent circuit is same as that when i_{ds} rises during t_{ri}, seen in Figure 2.5. Meanwhile, both C_{gs} and C_{rss} are being discharged and the value of v_{gs} falls from $V_{plateau}$ to $V_{drive,n}$. In addition, the value of v_{ds} stays at U_{dc} constantly during t_{fi}. Then t_{fi} is solved in (2.31) to (2.34).

$$\frac{V_{drive,n} - v_{gs}}{R_g} = C_{gs} \cdot \frac{\mathrm{d}v_{gs}}{\mathrm{d}t} + C_{rss} \cdot \frac{\mathrm{d}\left(v_{gs} - v_{ds}\right)}{\mathrm{d}t} \tag{2.31}$$

$$\frac{1}{R_g \cdot C_{iss}} \cdot \mathrm{d}t = \frac{1}{V_{drive,n} - v_{gs}} \cdot \mathrm{d}v_{gs} \tag{2.32}$$

$$\int_{(t_{d,off}+t_{ru})}^{(t_{d,off}+t_{ru}+t_{fi})} \frac{1}{R_g \cdot C_{iss}} \cdot \mathrm{d}t = \int_{V_{plateau}}^{V_{th}} \frac{1}{V_{drive,n} - v_{gs}} \cdot \mathrm{d}v_{gs} \tag{2.33}$$

$$t_{fi} = R_g \cdot C_{iss} \cdot \ln \frac{V_{plateau} - V_{drive,n}}{V_{th} - V_{drive,n}} \tag{2.34}$$

With the expressions obtained above, the six time intervals, $t_{d,on}$, $t_{d,off}$, t_{ri}, t_{fu}, t_{fi}, and t_{ru} are calculated; and then the switching power loss can be estimated based on the derived rise- and fall-time of MOSFET current and voltage. Some of the parameters used in the calculations are defined by the inverter operating conditions and the designed gate driver, such as V_{drive}, $V_{drive,n}$, U_{dc}, R_g and i_{ds}; several parameters are given by the MOSFET datasheets, such as R_M, V_{th}, $V_{plateau}$, C_{iss} and C_{rss}. In most of the MOSFET datasheets, C_{iss} and some other parameters that are used for the evaluation of t_{fi} and t_{ri} are constant. As a result, t_{fi} and t_{ri} can be calculated directly from the value of C_{iss} given by the datasheet. In contrast, a more accurate approximation for the value of C_{rss} is needed to acquire t_{fu} and t_{ru}, because the value of C_{rss} varies dramatically during t_{fu} and t_{ru}; furthermore, the selection of C_{rss} directly affects the accuracy of t_{fu} and t_{ru} estimation.

Two methods for acquiring the value of C_{rss} are discussed. An existing method is provided by (Graovac *et al.*, 2006). A new method is also propose to improve the accuracy of t_{fu} and t_{ru} calculation. In addition, because these two methods are implemented based on MOSFET datasheets, one MOSFET product is selected and the calculations are derived according to its datasheet (Microsemi, 2011).

For the existing method, due to the dramatic change of C_{rss} during t_{fu} and t_{ru}, an

approximated value is selected to describe the value of C_{rss} during the entire switching period. An average value of C_{rss} is chosen and used in the calculation by the existing method. The MOSFET parasitic capacitance waveforms given by the datasheet are shown in Figure 2.8 on the left, including input capacitance C_{iss}, output capacitance C_{oss} and reverse transfer capacitance C_{rss}. According to the waveforms in Figure 2.8, when v_{ds} rises from the MOSFET on-state voltage $V_{dson} = R_M \cdot i_{ds}$ to V_{dd} that is U_{dc} in an inverter, the value of C_{rss} changes from C_{rss_n+1} to C_{rss_1}. The average value of C_{rss_n+1} and C_{rss_1} is calculated by (2.35), which is selected as the approximated C_{rss} in t_{fu} and t_{ru} calculations.

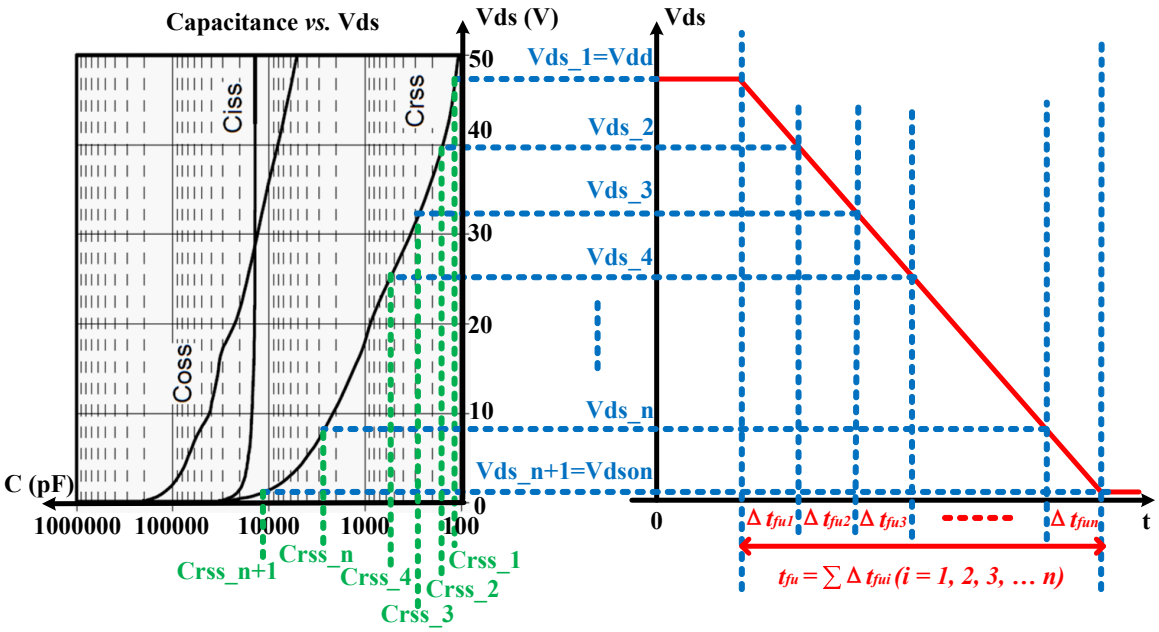


Figure 2.8: MOSFET parasitic capacitance waveforms from (Microsemi, 2011) with respect to the change of v_{ds}.

$$C_{rss} = \frac{C_{rss\_n+1} + C_{rss\_1}}{2} \tag{2.35}$$

It can be seen that the plots in Figure 2.8 provided by the datasheet only contain values of C_{rss} when v_{ds} varies between 0V and 50V. However, the off-state voltage value V_{dd} (U_{dc}) is not necessarily under 50V in different inverter circuits. In addition, the variation trend shows the changing rate of C_{rss} reduces significantly when V_{dd} increases to a value higher than 50V. Therefore, an assumption is made that C_{rss} is considered as a constant parameter at 100pF, when v_{ds} is greater than 50V. Then, by substituting the approximated C_{rss} from (2.35) into (2.19) and (2.30), t_{fu} and t_{ru} can be derived. Nevertheless, as it is shown by Figure 2.8 that there is a large difference between C_{rss_n+1} and C_{rss_1}; thus, the average value calculated by (2.35) cannot describe C_{rss} accurately during the entire period of t_{fu} or t_{ru}.

For the proposed method, instead of selecting an approximated value of C_{rss}, t_{fu} and t_{ru} are divided into several time intervals and an approximated C_{rss} is selected for each of those small periods. If the time intervals are small enough, the value of C_{rss} corresponding to a certain time period can be assumed constant. Thus, each time interval can be calculated by an constant capacitance. In this way, C_{rss} is presented by different approximated values during switching transitions; and time intervals can be calculated individually. In the end, t_{fu} and t_{ru} are obtained by the sum of this group of time intervals. Using this method, C_{rss} is described more accurately throughout the entire switching period, which could renders more accurate estimations for t_{fu} and t_{ru}. As it can be seen from Figure 2.8, the combination of the left chart and right diagram shows that a group of voltage levels can be added between V_{dd} and V_{dson}; and then a group of time intervals are created in the right chart. Thus, several C_{rss} values can be selected; and different time intervals are calculated based on various C_{rss} values.

To understand this proposed method better, an example is discussed. Considering the right part of Figure 2.8, more voltage levels between V_{dd} and V_{dson} are taken into account, such as V_{ds_i}, where $i = 2, 3, 4, , n$. There are $n + 1$ voltage levels in all that correspond to n time intervals. During the MOSFET switching transitions, v_{ds} falls within t_{fu}; and if $n = 2$, a voltage level, V_{ds_2}, is added between V_{dd} and V_{dson}. Then, two time intervals are created; one is the time duration for v_{ds} falling from V_{dd} to V_{ds_2} and it is Δt_{fu1}, the other one is the time duration for v_{ds} falling from V_{ds_2} to V_{dson} that is Δt_{fu2}. Two C_{rss} values are used in calculations, C_{rss_1} and C_{rss_2} are utilized in Δt_{fu1} and Δt_{fu2} calculation respectively. Then, t_{fu} can be represented by (2.36) and (2.37).

$$t_{fu} = (V_{dd} - V_{ds\_2} + V_{ds\_2} - V_{dson}) \cdot \frac{R_g \cdot C_{rss}}{V_{drive} - V_{plateau}} \tag{2.36}$$

$$t_{fu} = (V_{dd} - V_{ds\_2}) \cdot \frac{R_g \cdot C_{rss\_1}}{V_{drive} - V_{plateau}} + (V_{ds\_2} - V_{dson}) \cdot \frac{R_g \cdot C_{rss\_2}}{V_{drive} - V_{plateau}} \tag{2.37}$$

As it has been mentioned that $V_{dd} = U_{dc}$ and $V_{dson} = R_M \cdot i_{ds}$, t_{fu} can be rewritten in the form of (2.38) and (2.39).

$$t_{fu} = (U_{dc} - V_{ds\_2} + V_{ds\_2} - R_M \cdot i_{ds}) \cdot \frac{R_g \cdot C_{rss}}{V_{drive} - V_{plateau}} \tag{2.38}$$

$$t_{fu} = (U_{dc} - V_{ds\_2}) \cdot \frac{R_g \cdot C_{rss\_1}}{V_{drive} - V_{plateau}} + (V_{ds\_2} - R_M \cdot i_{ds}) \cdot \frac{R_g \cdot C_{rss\_2}}{V_{drive} - V_{plateau}} \tag{2.39}$$

Consequently, the total voltage fall-time t_{fu} is obtained in (2.40).

$$t_{fu} = \Delta t_{fu1} + \Delta t_{fu2} \tag{2.40}$$

Additionally, voltage level selection is another aspect to be concerned for the proposed method. On one hand, the selected voltage levels can be evenly distributed between V_{dd} and V_{dson}. When each time interval is small enough, the value of C_{rss} can be assumed constant in each time period; thus, the number of selected voltage levels should be large enough. The more voltage levels are used, the more time intervals are created, as a result, the more accurate C_{rss} can be presented in the entire switching period. On the other hand, the distribution of selected voltage levels also can be uneven. Then, those voltage levels can be selected based on the non-linearity of the C_{rss} curve. At highly non-linear part of the curve, more voltage levels can be used. In other words, more voltage levels can be used when the variation of C_{rss} is dramatic. For instance, according to Figure 2.8, more voltage levels can be set when v_{ds} is low.

MOSFET switching power losses

With estimated time intervals, t_{fi}, t_{ri}, t_{fu} and t_{ru}, switching energy losses $E_{on,M}$ and $E_{off,M}$ are calculated. It should be noticed that t_{fi} and t_{ri} can be obtained directly from (2.13) and (2.34); however, t_{fu} and t_{ru} are not able to be calculated directly; since (2.19) and (2.30) contain a parameter i_{ds} that is used to obtain the MOSFET on-state voltage and it is not a constant value. It is known that inverter output current defines the value and period of the current through each switch i_{ds}. Consider phase A in Figure 2.9 as an example, if the inverter output current is sinusoidal, the positive current flows through T_1 and the negative current goes through T_2. Therefore, the average values of t_{fu} and t_{ru} in T_s need to be determined.

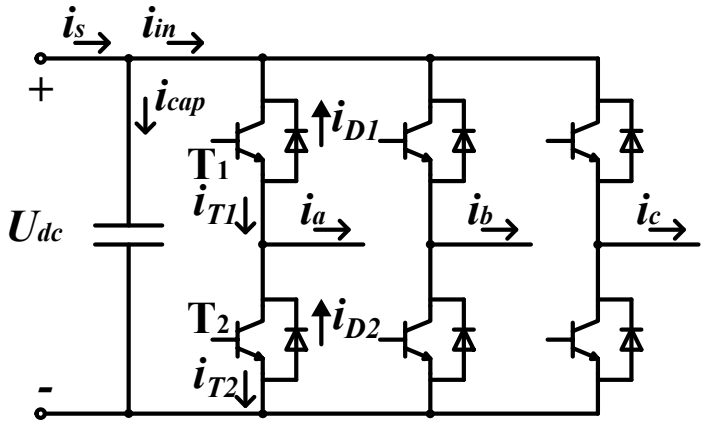


Figure 2.9: Topology of three-phase voltage source inverter.

If there are $n+1$ selected voltage levels and n time intervals, the term i_{ds} only exists in the n^{th} time period and the other $n-1$ time intervals are not influenced by the on-state voltage; and then expressions for the n^{th} time interval can be represented as below.

$$\begin{aligned} \Delta t_{fun} &= (V_{ds\_n} - V_{ds\_n+1}) \cdot \frac{R_g \cdot C_{rss\_n}}{V_{drive} - V_{plateau}} \\ &= (V_{ds\_n} - R_M \cdot i_{ds}) \cdot \frac{R_g \cdot C_{rss\_n}}{V_{drive} - V_{plateau}} \end{aligned} \tag{2.41}$$

$$\begin{aligned} \Delta t_{run} &= (V_{ds\_n} - V_{ds\_n+1}) \cdot \frac{R_g \cdot C_{rss\_n}}{V_{plateau} - V_{drive,n}} \\ &= (V_{ds\_n} - R_M \cdot i_{ds}) \cdot \frac{R_g \cdot C_{rss\_n}}{V_{plateau} - V_{drive,n}} \end{aligned} \tag{2.42}$$

The inverter output current is assumed as (2.43). When i_a is positive and T_1 is conducting, i_{ds} in T_1 is equal to i_a; meanwhile, if i_a is negative and T_2 is conducting, i_{ds} in T_2 is equal to i_a. The waveforms shown in Figure 2.10 can be considered as examples.

$$i_a = \sqrt{2} I_{rms} \cdot \sin(\omega t) \tag{2.43a}$$

$$i_b = \sqrt{2} I_{rms} \cdot \sin(\omega t - \frac{2}{3}\pi) \tag{2.43b}$$

$$i_c = \sqrt{2} I_{rms} \cdot \sin(\omega t + \frac{2}{3}\pi) \tag{2.43c}$$

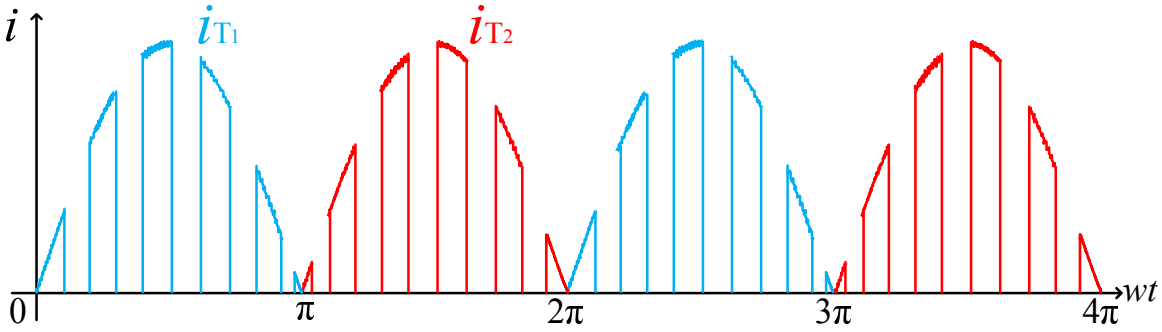


Figure 2.10: Examples for current through upper and lower switches in a phase-leg.

Based on Figure 2.10, by substituting (2.43a) into (2.41) and (2.42), the average values of Δt_{fun} and Δt_{run} are derived in (2.44) and (2.45) .

$$\begin{aligned} \Delta t_{fun} &= \frac{1}{2\pi} \int_0^{\pi} (V_{ds\_n} - R_M \cdot i_{ds}) \cdot \frac{R_g \cdot C_{rss\_n}}{V_{drive} - V_{plateau}} \mathrm{d}wt \\ &= (\frac{V_{ds\_n}}{2} - \frac{\sqrt{2} I_{rms} \cdot R_M}{\pi}) \cdot \frac{R_g \cdot C_{rss\_n}}{V_{drive} - V_{plateau}} \end{aligned} \tag{2.44}$$

$$\begin{aligned} \Delta t_{run} &= \frac{1}{2\pi} \int_0^{\pi} (V_{ds\_n} - R_M \cdot i_{ds}) \cdot \frac{R_g \cdot C_{rss\_n}}{V_{plateau} - V_{drive,n}} \mathrm{d}wt \\ &= (\frac{V_{ds\_n}}{2} - \frac{\sqrt{2} I_{rms} \cdot R_M}{\pi}) \cdot \frac{R_g \cdot C_{rss\_n}}{V_{plateau} - V_{drive,n}} \end{aligned} \tag{2.45}$$

Now with the time intervals, MOSFET energy losses can be estimated. The MOSFET turn-on energy loss in T_s is calculated with its corresponding transition time $t = t_{ri} + t_{fu}$, as it is given in (2.46).

$$\begin{aligned} E_{on,M} &= \int_0^{t_{ri}+t_{fu}} v_{ds} \cdot i_{ds} \cdot \mathrm{d}t \\ &= \int_0^{t_{ri}} U_{dc} \cdot \frac{t}{t_{ri}} \cdot i_{ds} \cdot \mathrm{d}t + \int_{t_{ri}}^{t_{ri}+t_{fu}} \frac{t_{ri} + t_{fu} - t}{t_{fu}} \cdot U_{dc} \cdot i_{ds} \cdot \mathrm{d}t \\ &= \frac{1}{2} \cdot U_{dc} \cdot i_{ds} \cdot (t_{ri} + t_{fu}) \end{aligned} \tag{2.46}$$

The average value of $E_{on,M}$ during the sinusoidal period of the inverter output current can also be calculated in (2.47).

$$\begin{aligned} E_{on,M} &= \frac{1}{2\pi} \int_0^{\pi} \frac{1}{2} \cdot U_{dc} \cdot i_{ds} \cdot (t_{ri} + t_{fu}) \cdot \mathrm{d}wt \\ &= \frac{\sqrt{2}}{2\pi} U_{dc} \cdot I_{rms} \cdot (t_{ri} + t_{fu}) \end{aligned} \tag{2.47}$$

Additionally, there is another part of energy loss included in MOSFET turn-on energy losses that is caused by the anti-parallel diode reverse recovery current (Muhsen *et al.*, 2015). Taking this part of energy losses into account, $E_{on,M}$ can be rewritten in (2.48)

$$E_{on,M} = \frac{\sqrt{2}}{2\pi} U_{dc} \cdot I_{rms} \cdot (t_{ri} + t_{fu}) + Q_{rr} \cdot U_{dc} \tag{2.48}$$

After that, MOSFET turn-off energy losses are estimated by the similar solution. During $t = t_{ru} + t_{fi}$, $E_{off,M}$ is calculated in T_s by (2.49).

$$\begin{aligned} E_{off,M} &= \int_0^{t_{ru}+t_{fi}} v_{ds} \cdot i_{ds} \cdot \mathrm{d}t \\ &= \int_0^{t_{ru}} \frac{t}{t_{ru}} \cdot U_{dc} \cdot i_{ds} \cdot \mathrm{d}t + \int_{t_{ru}}^{t_{ru}+t_{fi}} U_{dc} \cdot \frac{t_{ru}+t_{fi}-t}{t_{fi}} \cdot i_{ds} \cdot \mathrm{d}t \\ &= \frac{1}{2} \cdot U_{dc} \cdot i_{ds} \cdot (t_{ru}+t_{fi}) \end{aligned} \tag{2.49}$$

Then, the average value of $E_{off,M}$ can also be calculated in (2.50); the energy losses that are caused by the diode during switch turn-off transition are negligible.

$$\begin{aligned} E_{off,M} &= \frac{1}{2\pi} \int_0^{\pi} \frac{1}{2} U_{dc} \cdot i_{ds} \cdot (t_{ru}+t_{fi}) \cdot \mathrm{d}wt \\ &= \frac{\sqrt{2}}{2\pi} U_{dc} \cdot I_{rms} \cdot (t_{ru}+t_{fi}) \end{aligned} \tag{2.50}$$

Finally, MOSFET switching power losses are calculated in (2.51).

$$P_{sw,M} = (E_{on,M} + E_{off,M}) \cdot f_{sw} \tag{2.51}$$

2.1.2 IGBT power losses

Next, using the information provided in datasheets, the IGBT conduction and switching power loss calculations are demonstrated.

IGBT conduction power losses

During the on-state, an IGBT is equivalent to two components connected in series, a resistor that is a junction temperature-dependent parameter and a DC voltage source.

Figure 2.11 shows the equivalent circuit of a conducting IGBT, and the power losses in both of the resistor and DC voltage source contribute to the IGBT conduction power losses. The DC voltage $U_{0,I}$ is named as IGBT zero current voltage, which can be obtained from IGBT current and voltage characteristic plot that is shown as U_{CE0} in (Grenzheuser and Lee, 2013).

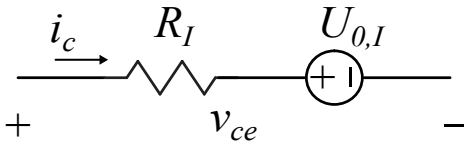


Figure 2.11: Equivalent circuit of an on-state IGBT.

In (2.52), the first item indicates the conduction power loss caused by R_I; meanwhile, the other item presents the conduction power loss generated by the equivalent DC voltage source whose output voltage is $U_{0,I}$. Usually, $U_{0,I}$ is given by IGBT datasheets (Graovac and Prschel, 2009).

$$P_{c,I} = {I^2}_{rms,I} \cdot R_I + U_{0,I} \cdot I_{ave,I} \tag{2.52}$$

IGBT switching power losses

Generally speaking, IGBT switching energy losses, $E_{on,I}$ and $E_{off,I}$, are provided by manufacturer datasheets in the form of data plots. Nevertheless, most of these data are acquired under testing conditions that are usually different from the actual inverter operating conditions. According to (Bierhoff and Fuchs, 2004), $E_{on,I}$ and $E_{off,I}$ are proportional to the current through and the off-state voltage across the IGBT, i_c and U_{dc}. Thus, using the given values in datasheets as references, the actual switching energy losses should be estimated based on (2.53) and (2.54).

$$E_{on,I} = \frac{U_{dc}}{U_{ref}} \cdot \frac{i_c}{I_{ref}} \cdot E_{on,ref} \tag{2.53}$$

$$E_{off,I} = \frac{U_{dc}}{U_{ref}} \cdot \frac{i_c}{I_{ref}} \cdot E_{off,ref} \tag{2.54}$$

Similarly to i_{ds} contained in (2.46) and (2.49), attentions should be paid to i_c in the expressions above. Average values of $E_{on,I}$ and $E_{off,I}$ are given by (2.55) and (2.56).

$$\begin{aligned} E_{on,I} &= \frac{1}{2\pi} \int_0^{\pi} \frac{U_{dc}}{U_{ref}} \cdot \frac{i_c}{I_{ref}} \cdot E_{on,ref} \cdot \mathrm{d}wt \\ &= \frac{\sqrt{2}}{\pi} \frac{I_{rms} \cdot U_{dc}}{U_{ref} \cdot I_{ref}} \cdot E_{on,ref} \end{aligned} \tag{2.55}$$

$$\begin{aligned} E_{off,I} &= \frac{1}{2\pi} \int_0^{\pi} \frac{U_{dc}}{U_{ref}} \cdot \frac{i_c}{I_{ref}} \cdot E_{off,ref} \cdot \mathrm{d}wt \\ &= \frac{\sqrt{2}}{\pi} \frac{I_{rms} \cdot U_{dc}}{U_{ref} \cdot I_{ref}} \cdot E_{off,ref} \end{aligned} \tag{2.56}$$

Then, the IGBT switching power losses are acquired in (2.57).

$$P_{sw,I} = (E_{on,I} + E_{off,I}) \cdot f_{sw} \tag{2.57}$$

2.1.3 Diode power losses

Diode conduction power losses

The equivalent circuit of a conducting diode is presented in Figure 2.12, which is similar to that of an IGBT. Thus, the conduction power loss calculation of the diode is same as that of the IGBT, and it is indicated in (2.58).

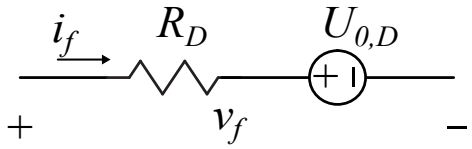


Figure 2.12: Equivalent circuit of an on-state diode.

$$P_{c,D} = {I^2}_{rms,D} \cdot R_D + U_{0,D} \cdot I_{ave,D} \tag{2.58}$$

Diode switching power losses

Diode switching energy losses are mainly generated by its reverse recovery during the turn-off transition, compared to which the diode turn-on energy loss is negligible. Thus, switching energy loss of the diode is also called reverse recovery energy loss E_{rr}.

Some diode datasheets provide the values of E_{rr} under testing conditions. In this case, the method for determining E_{rr} is same as that for $E_{on,I}$ and $E_{off,I}$.

$$E_{rr} = \frac{U_{dc}}{U_{ref}} \cdot \frac{i_f}{I_{ref}} \cdot E_{rr,ref} \tag{2.59}$$

$$\begin{aligned} E_{rr} &= \frac{1}{2\pi}\int_{0}^{\pi}\frac{U_{dc}}{U_{ref}}\cdot\frac{i_f}{I_{ref}}\cdot E_{rr,ref}\cdot \mathrm{d}wt \\ &= \frac{\sqrt{2}}{\pi}\frac{I_{rms}\cdot U_{dc}}{U_{ref}\cdot I_{ref}}\cdot E_{rr,ref} \end{aligned} \tag{2.60}$$

Nevertheless, the diode reverse recovery charge and current are given in some datasheets instead of E_{rr}. In this scenario, according to (Nuutinen *et al.*, 2014), an empirical expression is commonly utilized and is shown by (2.61).

$$E_{rr} = \frac{1}{4}\cdot Q_{rr}\cdot U_{dc} \tag{2.61}$$

2.2 Power Losses in an Inverter

Most of the parameters utilized in P_{loss} calculation are provided by datasheets, however the RMS and average current through the switch and diode need to be determined based on the inverter operating conditions. With the assumption that a balanced three-phase load is connected into the inverter system, the power losses in one of the switches and diodes are discussed and the total inverter power losses can be obtained by multiplying the power losses in one switch and diode by six. Take phase A for instance, I_{ave} and I_{rms} of the upper switch and lower diode are calculated. The output current is assumed as phase A current in (2.62a); and the output phase voltage can be expressed in (2.62b).

$$i_o = \sqrt{2}\cdot I_{rms}\sin(\omega t) \tag{2.62a}$$

$$v_o = \sqrt{2}\cdot V_{rms}\sin(\omega t + \phi) \tag{2.62b}$$

The duty ratio of the switch can be obtained by comparing the modulation signal to the carrier signal; and the current flowing through the switch can be represented by the duty ratio and the output current (Gervasio *et al.*, 2015; Ma *et al.*, 2016). According to Figure 2.13, the phase A upper switch is turned on when the value of the phase A modulation signal is higher than the value of the carrier signal, and the duty cycle D of the phase A upper switch is derived in (2.63).

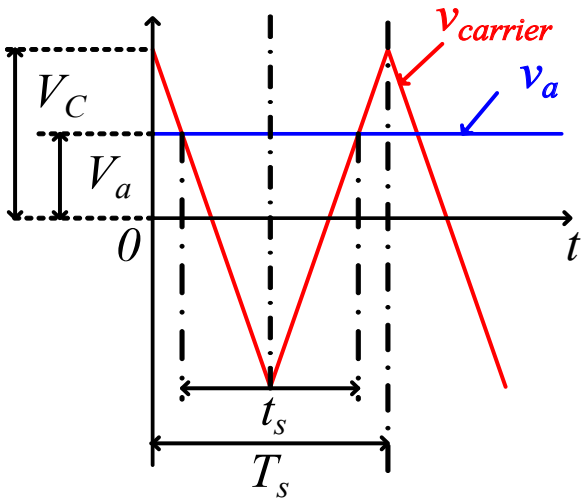


Figure 2.13: Curves of the carrier and phase A modulation signal in T_s.

$$D = \frac{t_s}{T_s} = \frac{v_a + V_C}{2V_C} = \frac{1}{2} \cdot \left[1 + M \cdot sin\left(\omega t + \phi\right)\right] \tag{2.63}$$

During T_s, when i_a is positive and switch T_1 in Figure 2.9 is on, the current flows through T_1. Then the switch current i_{switch} can be expressed by i_o and D in (2.64).

$$i_{switch} = D \cdot i_o = D \cdot \sqrt{2} \cdot I_{rms} \cdot \sin(\omega t) \tag{2.64}$$

After a time duration $t = D \cdot T_s$, switch T_1 is turned off. At this moment, i_a is

still positive, thus the current has to flow through the lower diode in phase A. With the assumption that the inverter is connected to a balanced three-phase load, the power losses of a diode can be estimated firstly and the total power losses in diode are obtained by multiplying by six. Then, the power losses in lower diode of phase A is analyzed. The current in D_2 is expressed in (2.65).

$$i_D = (1-D)\cdot i_o = (1-D)\cdot\sqrt{2}\cdot I_{rms}\cdot\sin(\omega t) \tag{2.65}$$

Consequently, the average and RMS values of the switch current corresponding to sinusoidal period are derived in (2.66) and (2.67). At the same time, the average and RMS values of the diode current are shown in (2.68) and (2.69).

$$\begin{aligned} I_{ave,switch} &= \frac{1}{2\pi}\cdot\int_0^{\pi} i_{switch}\cdot \mathrm{d}\omega t \\ &= \frac{1}{2\pi}\cdot\int_0^{\pi} D\cdot\sqrt{2}\cdot I_{rms}\cdot\sin(\omega t)\cdot \mathrm{d}\omega t \\ &= \frac{I_{rms}}{\sqrt{2}\cdot\pi}\cdot\left(1+\frac{\pi\cdot M\cdot\cos\phi}{4}\right) \end{aligned} \tag{2.66}$$

$$\begin{aligned} I_{rms,switch} &= \sqrt{\frac{1}{2\pi}\int_0^{\pi} D\cdot {i_o}^2\cdot \mathrm{d}\omega t} \\ &= \sqrt{\frac{1}{2\pi}\int_0^{\pi} D\cdot\left(\sqrt{2}I_{rms}\cdot\sin(\omega t)\right)^2\cdot \mathrm{d}\omega t} \\ &= \frac{I_{rms}}{2}\cdot\sqrt{1+\frac{8M\cdot\cos\phi}{3\pi}} \end{aligned} \tag{2.67}$$

$$\begin{aligned} I_{ave,D} &= \frac{1}{2\pi} \cdot \int_0^{\pi} i_D \cdot \mathrm{d}\omega t \\ &= \frac{1}{2\pi} \cdot \int_0^{\pi} (1-D) \cdot \sqrt{2} \cdot I_{rms} \cdot \sin(\omega t) \cdot \mathrm{d}\omega t \\ &= \frac{I_{rms}}{\sqrt{2} \cdot \pi} \cdot \left(1 - \frac{\pi \cdot M \cdot \cos\phi}{4}\right) \end{aligned} \tag{2.68}$$

$$\begin{aligned} I_{rms,D} &= \sqrt{\frac{1}{2\pi} \int_0^{\pi} (1-D) \cdot {i_o}^2 \cdot \mathrm{d}\omega t} \\ &= \sqrt{\frac{1}{2\pi} \int_0^{\pi} (1-D) \cdot \left(\sqrt{2} I_{rms} \cdot \sin(\omega t)\right)^2 \cdot \mathrm{d}\omega t} \\ &= \frac{I_{rms}}{2} \cdot \sqrt{1 - \frac{8M \cdot \cos\phi}{3\pi}} \end{aligned} \tag{2.69}$$

With the calculated conduction and switching power losses in both switch and diode, the total inverter power losses can be obtained accordingly in (2.70) to (2.72), where the subscript "*switch*" denotes $P_{c,M}$ or $P_{c,I}$ depending on the type of semiconductor devices utilized in the inverter system (Zdanowski *et al.*, 2016).

$$P_c = P_{c,switch} + P_{c,D} \tag{2.70}$$

$$P_{sw} = P_{sw,switch} + P_{sw,D} \tag{2.71}$$

$$P_{loss,inverter} = 6(P_c + P_{sw}) \tag{2.72}$$

2.3 Inverter Thermal Management and Capability

2.3.1 Selection of thermal management system

From the calculations of the inverter power loss, it can be found that the junction temperature T_j of the semiconductor device affects the on-state resistance and switching energy losses; as a result, the total inverter power loss is influenced. As T_j rises, the on-state resistance and switching energy loss grow, which leads to the increase in inverter power loss (Drofenik and Kolar, 2005; Tiwari *et al.*, 2016). Meanwhile, the power losses also cause a junction temperature rise. Generally, the amount of temperature rise is proportional to the amount of power losses (Naayagi, 2015). A diagram is shown in Figure 2.14 and it indicates the relationship between the device junction temperature and the inverter power loss (Ye *et al.*, 2014). According to the switching device junction temperature, the values of the on-state resistance and switching energy losses can be found in the datasheets; and then, the conduction and switching power losses are calculated depending on those values. Finally, the total inverter power losses can be obtained.

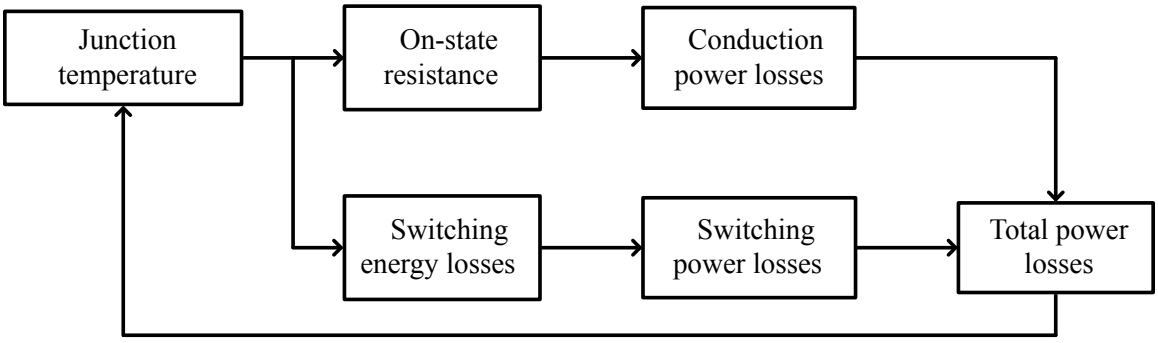


Figure 2.14: The relationship between the power loss and junction temperature.

According to Figure 2.14, during the operation of the inverter, the power losses in the beginning result in a temperature rise in the semiconductor device junction; and then, the increase of T_j further leads to the grow in the total power losses. After that, the increasing power losses further cause the rise in T_j. In this case, thermal management is necessary for the inverter system to control T_j within the maximum allowable value of the device; thus, the overheat and damage in the semiconductor device can be prevented (Muhsen *et al.*, 2015). The relationship between the total power loss and temperature rise is written in (2.73), where $R_{th,ja}$ is the ambient to junction thermal resistance. The temperature rise ΔT from the ambient environment to the semiconductor junction is described in (2.74) (Mirzaee *et al.*, 2014).

$$\Delta T_{ja} = P_{loss} \cdot R_{th,ja} \tag{2.73}$$

$$\Delta T_{ja} = T_j - T_a \tag{2.74}$$

There are three components included in the junction to ambient thermal resistance, they are thermal resistance from junction to case $R_{th,jc}$, case to heat sink $R_{th,cs}$, and heat sink to ambient $R_{th,sa}$; and $R_{th,ja}$ can be written in the form of (2.75) (Lee, 1995). Thus, the temperature rise can also be expressed as in (2.76).

$$R_{th,ja} = R_{th,jc} + R_{th,cs} + R_{th,sa} \tag{2.75}$$

$$\begin{aligned} \Delta T_{ja} &= P_{loss} \cdot (R_{th,jc} + R_{th,cs} + R_{th,sa}) \\ &= \Delta T_{jc} + \Delta T_{cs} + \Delta T_{sa} \end{aligned} \tag{2.76}$$

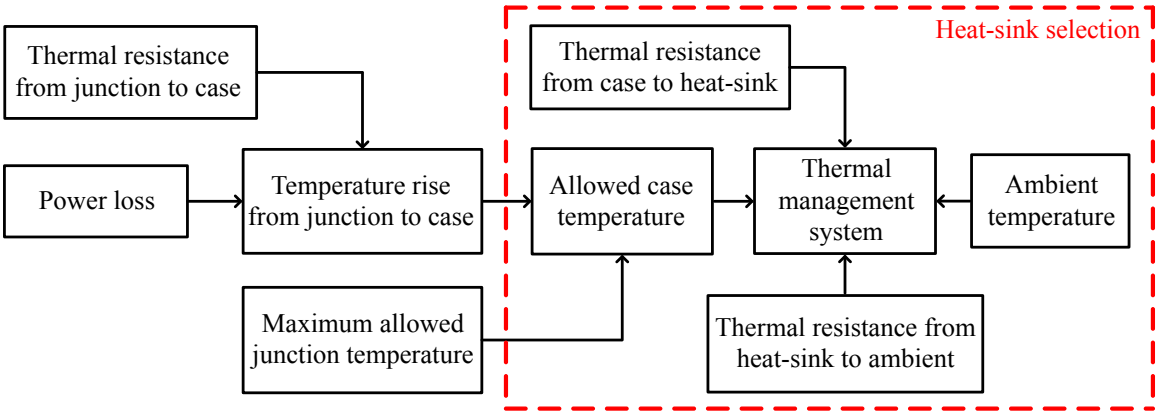


Figure 2.15: Heat sink selection.

Generally speaking, the value of $R_{th,jc}$ is defined by the device package and is given by the datasheets. The value of $R_{th,cs}$ denote the thermal resistance from the case of the semiconductor device to the surface of the heat sink, which is decided by the connection, contact area, and thermal grease materials between the device and heat sink (Yamamoto *et al.*, 2016; Marinov *et al.*, 2016). The heat sink thermal resistance is $R_{th,sa}$ that is determined by the material, geometry dimensions, and cooling types (air, water, or liquid cooling) of the heat sink. To select a heat sink is to determine a thermal management system with minimized case to ambient thermal resistance based on a given ambient temperature and to keep the junction temperature of semiconductor device within the maximum allowable value (Christen *et al.*, 2016). The flow chart for heat sink selection is shown in Figure 2.15; and depending on this flow chart, several steps are summarized. (Hazra *et al.*, 2015; Madhusoodhanan *et al.*, 2016).

- Determine the maximum allowable junction temperature $T_{j,max}$ and thermal resistance $R_{th,jc}$ of the device package based on the datasheets.

- Calculate the temperature rise from the case to junction ΔT_{jc} using the estimated power losses and (2.76).
- Obtain the maximum allowable case temperature $T_{c,max}$ using ΔT_{jc} and $T_{j,max}$.
- Find the ambient temperature T_a.
- Decide the maximum temperature rise from ambient to case, $\Delta T_{cs} + \Delta T_{sa}$.
- Calculate the maximum allowable values of thermal resistances, $R_{th,cs}$ and $R_{th,sa}$.
- Select thermal management system satisfying the requirements of calculated thermal resistance, $R_{th,cs}$ and $R_{th,sa}$.

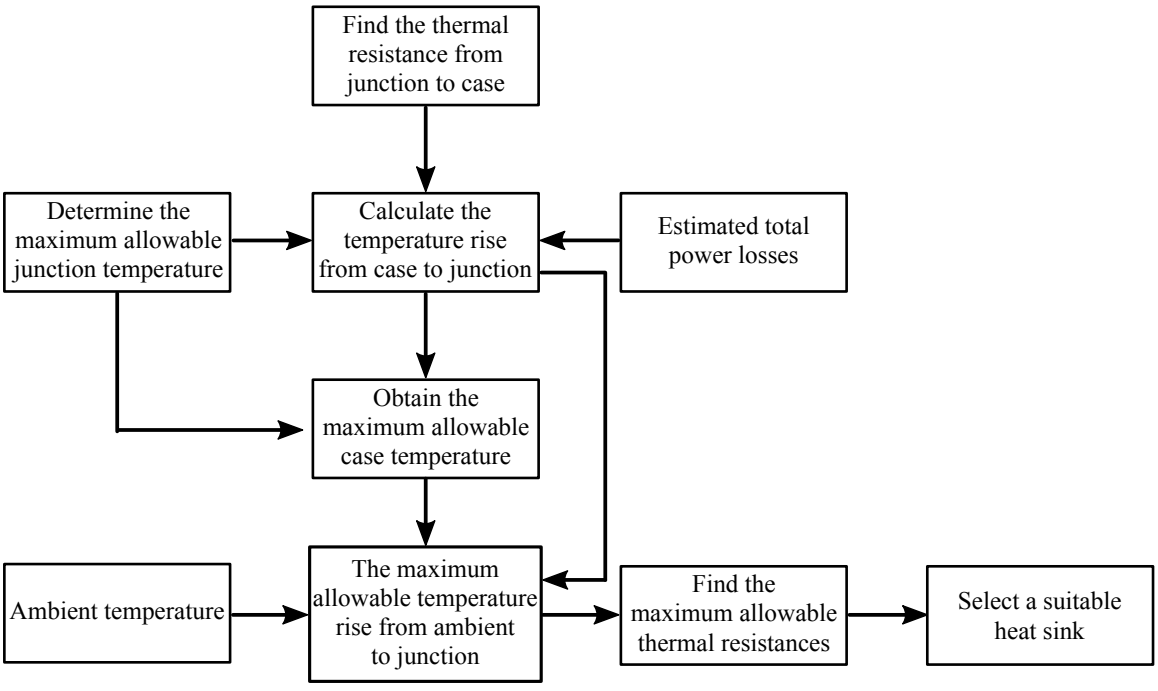


Figure 2.16: Heat sink selection steps.

2.3.2 Inverter capability

The power capability of the inverter is constrained by both semiconductor characteristics and thermal issue. On one hand, the semiconductor devices are usually selected depending on the inverter system requirements, such as output current and DC-link voltage. Thus, the selected devices should be able to carry the rated current, sustain the rated voltage, and handle the rated power of the inverter system; and the characteristics of the semiconductor devices should not be the main constrain of the inverter capability.

On the other hand, as the inverter power losses convert to heat, the thermal management that determines the amount of heat dissipation becomes the main influence in the inverter capability. Generally speaking, there is no significant variation in conduction power losses under rated power conditions, since the values of inverter output current and voltage that contribute to the conduction power losses do not vary dramatically under the rated power conditions. However, dramatic change might occur in switching power losses that are proportional to the switching frequency. The higher switching frequency is, the more power losses and heat are generated. To some extent, the thermal management affects the maximum achievable switching frequency under the inverter rated operating conditions (Mohan and Naik, 2014).

As a result, the thermal management system should be selected based on the power losses that are estimated according to the maximum power and switching frequency that are demanded by the inverter system.

2.4 Summary

The mathematic model of power loss calculation for both semiconductor device and inverter are discussed. Calculation methods of the conduction and switching power losses are demonstrated for three types of devices, MOSFETs, IGBTs and diodes, individually. Due to the differences in on-state equivalent circuits of three types of devices, the conduction power losses of MOSFETs are derived by the product of the switch RMS current ($I_{rms,M}$) and on-state resistance (R_M); meanwhile those of IGBTs and diodes are estimated based on not only the switch RMS current ($I_{rms,I}$ and $I_{rms,D}$) and on-state resistance (R_I and R_D) but also the zero current voltage ($U_{0,I}$ and $U_{0,D}$) and switch average current ($I_{ave,I}$ and $I_{ave,D}$). The switching power loss calculation for IGBTs and diodes is straightforward and can be easily derived by using the switching energy losses provided in the device datasheets and practical inverter operating voltage and current. However, more complicated calculation is developed for MOSFET switching power losses.

The MOSFET inherent capacitances are usually given in the form of logarithm plots by datasheets instead of switching energy losses. As a result, the switching time and energy losses need to be calculated based on the values of those capacitances. An existing method is introduced for MOSFET switching transient time calculation, but the estimation accuracy cannot be guaranteed because of the highly non-linear variation of the reverse transfer capacitance C_{rss}. Then, the proposed method is developed to obtain more accurate results in MOSFET switching time estimation. The principle of the proposed method is to divide the entire switching period into small time intervals, and the value of C_{rss} is considered constant in each time interval that is short enough. After that each small time period can be estimated individually

and the entire period is acquired by the sum of all small time periods.

In the end, the selection of thermal management system is discussed based upon the estimated power losses. In order to prevent overheat and damage in the semiconductor devices, the junction temperature should be kept under the maximum allowable value given by datasheets. Additionally, to operate the inverter under rated conditions, such as output power and switching frequency, the thermal management system should be selected depending on the power losses that are obtained with maximum power and switching frequency required by the inverter system.

Chapter 3

DC-Link Current/Voltage Ripple Analysis and DC-Link Capacitor Selection

With various capacitances connected in the inverter DC-link, the voltage ripples are different; large ripples are obtained with small DC-link capacitance, and vice versa. To some extent, large DC-link capacitance is usually preferred to reduce the voltage ripples. When large capacitance is selected, large volume and high weight of the capacitors are unavoidable. Nevertheless, the sizes of DC-link capacitors should also be kept as small as possible to achieve high power density of the entire inverter system. In this case, the selection of the DC-link capacitor is also important in inverter design. Two parameters should be determined for DC-link capacitor selection, such as rated continuous current and capacitance (Huiqing Wen *et al.*, 2012). On one hand, the DC-link current ripple component is equivalent to the capacitor current. Thus, to prevent overheat, the maximum allowable continuous current of the selected capacitor should

be higher than the RMS value of the inverter DC-link ripple current. On the other hand, the capacitance should be selected depending on the voltage ripple allowed in the DC-link. Some studies have been done to analyze the DC-link current and voltage ripples based on the inverter output phase current in (Dahono *et al.*, 1996; Kolar and Round, 2006; Pei *et al.*, 2015).

Generally speaking, small voltage ripple can be obtained by using large capacitance, however more space is occupied when large capacitors are utilized. To reduce the volume, weight, and cost of the DC-link capacitors, some research has been done in reducing the capacitance demanded by the inverter system in (Kieferndorf *et al.*, 2004; Lu and Peng, 2009; Lu *et al.*, 2009, 2011; Ye and Emadi, 2014). Hence, the optimization methods could be implemented for capacitance minimization. The estimation accuracy of the current and voltage ripple plays an important role in both of DC-link capacitor selection and capacitance minimization. Nevertheless, most of the prior work in current and voltage ripple estimation often neglects the dead time and diode reverse recovery that also affect those ripples in the DC-link. A dead time vector approach is developed to analyze the DC-link current ripple in (Chan *et al.*, 1997); however to the best of our knowledge, there is no research being done with the consideration of inverter anti-parallel diode reverse recovery. In order to improve the estimation accuracy of the DC-link current and voltage ripple, the diode reverse recovery is taken into account.

In this chapter, a brief introduction of PWM techniques is presented in Section 3.1. Based on the discussions in PWM techniques, the DC-link current and voltage of the inverter are analyzed. In Section 3.2, an existing method is described to estimate the average and RMS values of the DC-link current and its ripple component. In addition,

the occurrence of the inverter anti-parallel diode reverse recovery is analyzed in detail. By considering the reverse recovery, the DC-link current is analyzed; and to improve the estimation accuracy of the DC-link current and its ripple component, a proposed method is illustrated. Utilizing the proposed method, the analysis and estimation of the DC-link voltage ripple are demonstrated in Section 3.3. Furthermore, considering the voltage ripple and the RMS value of current ripple, the selection of DC-link capacitor is introduced in Section 3.4. Finally, Section 3.5 summarizes the chapter.

3.1 Pulse Width Modulation Techniques

The carrier based pulse width modulation (PWM) technique is utilized in various power converter control, including the three-phase voltage source inverter control. The sinusoidal pulse width modulation (SPWM), third harmonic injection pulse width modulation (THI), and space vector pulse width modulation (SVPWM) are three types of the most widely used PWM methods (Bowes and Holliday, 2007; Colak *et al.*, 2010; Mudlapur *et al.*, 2013); and a general introduction of these three PWM methods is presented.

3.1.1 SPWM, THI, and SVPWM

In these three PWM techniques, three-phase modulation signal is compared with the carrier signal, if the value of the modulation signal is equal to or higher than the value of the carrier signal, switching function is set at 1 and the upper switch in the corresponding phase is on and the lower switch is off. On the other hand, if the value of the modulation signal is lower than the value of the carrier signal,

switching function is set at 0 and the upper switch in the corresponding phase is off and the lower switch is on (Wu, 2006; Buso and Mattavelli, 2006). Waveforms of the modulation and carrier signals in SPWM, THI, and SVPWM are shown in Figure 3.1 to Figure 3.3 (Haghbin and Thiringer, 2014).

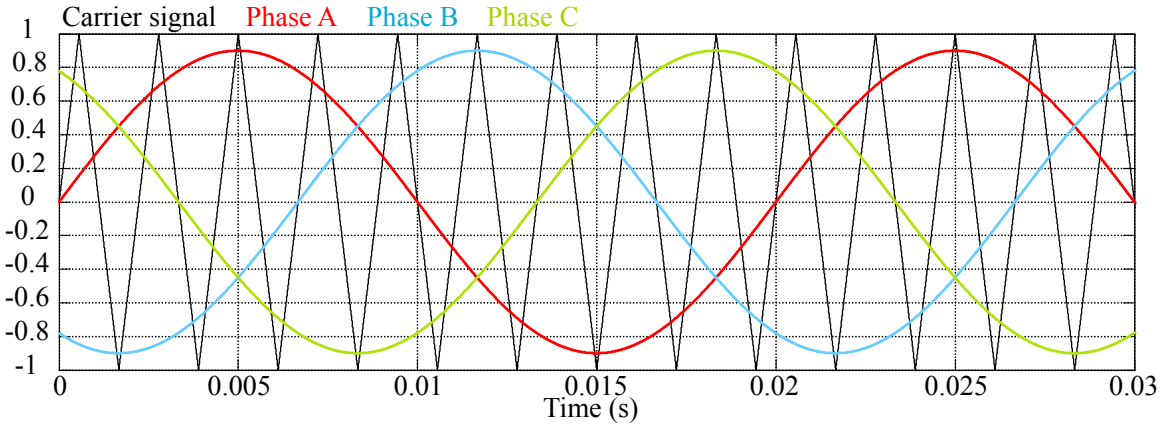
By interpreting the modulation signal peak value in the form of $M \cdot V_C$, where V_C denotes the peak value of the carrier signal, the modulation signals can be expressed with the zero-sequence injection signal in (3.1) (Wen and Yin, 2007). In the expressions, v_0 is the injection component that is given in (3.2) (Pei *et al.*, 2015). The first item in (3.2) indicates that there is not any component added to SPWM modulation signals (Kang *et al.*, 2009; Li *et al.*, 2012). At the same time, the second and the third items denote the injected components for the third harmonic injection and space vector PWM modulation signals (Zeng *et al.*, 2009; Jose *et al.*, 2010).

$$v_a = M \cdot V_C \cdot (\sin \omega t + v_0) \tag{3.1a}$$

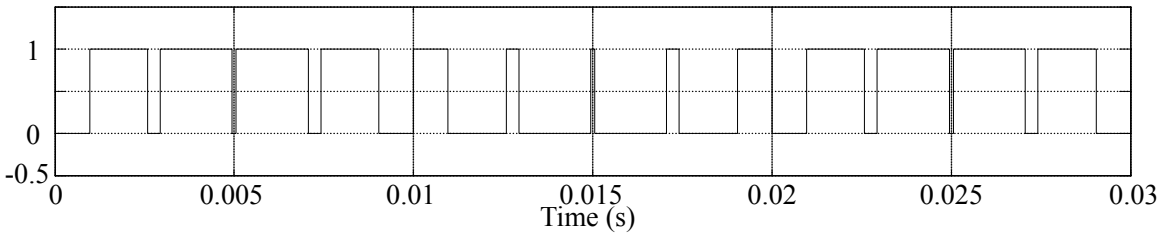
$$v_b = M \cdot V_C \cdot \left[\sin(\omega t - \frac{2\pi}{3}) + v_0\right] \tag{3.1b}$$

$$v_c = M \cdot V_C \cdot \left[\sin(\omega t + \frac{2\pi}{3}) + v_0\right] \tag{3.1c}$$

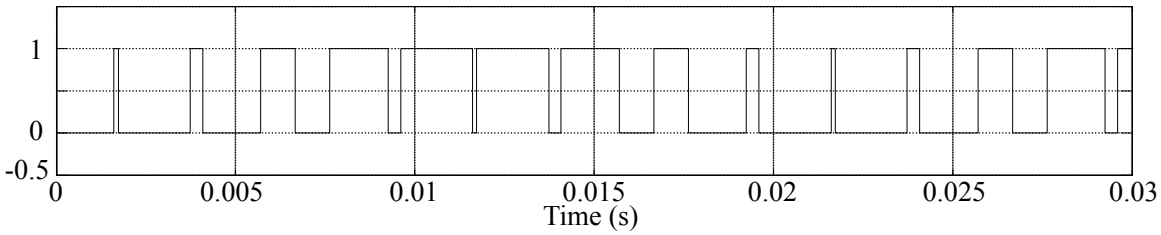
$$v_0 = \begin{cases} 0 & \text{, SPWM} \\ \frac{1}{6}\sin 3\omega t & \text{, THI} \\ -\frac{1}{2}\left(v_{max} + v_{min}\right) & \text{, SVPWM} \end{cases} \tag{3.2}$$



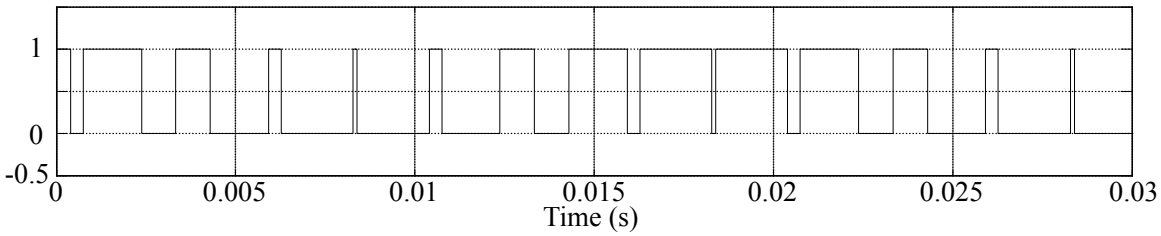
(a) Carrier and modulation signals.



(b) Phase A switching function.

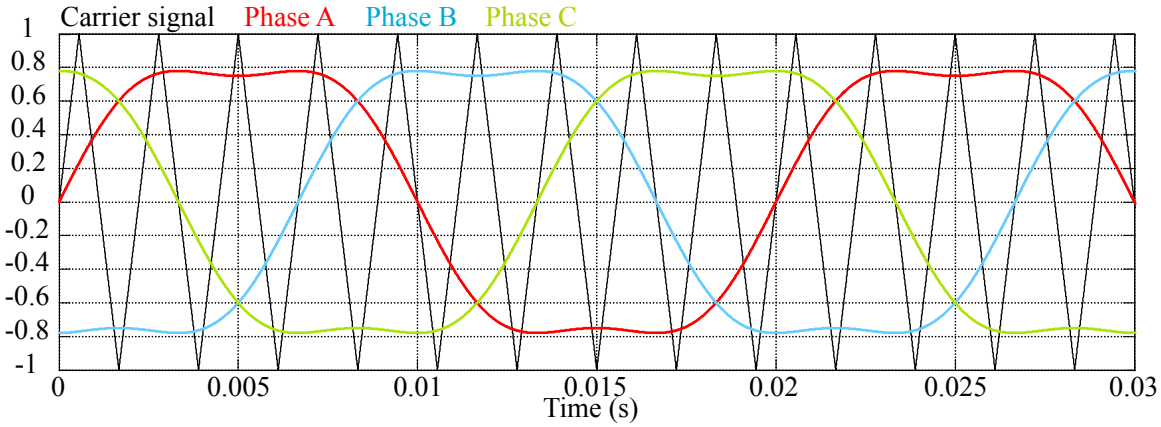


(c) Phase B switching function.

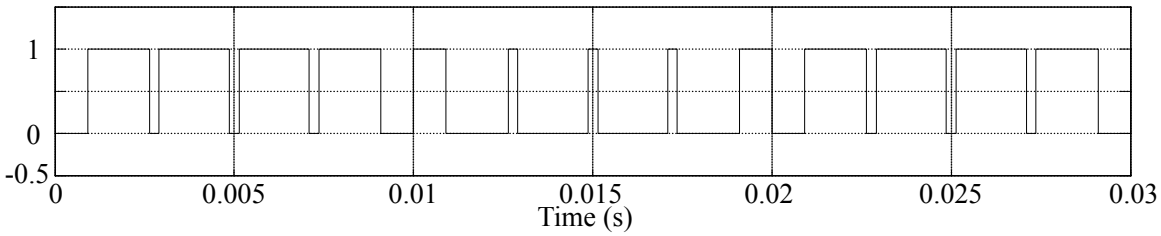


(d) Phase C switching function.

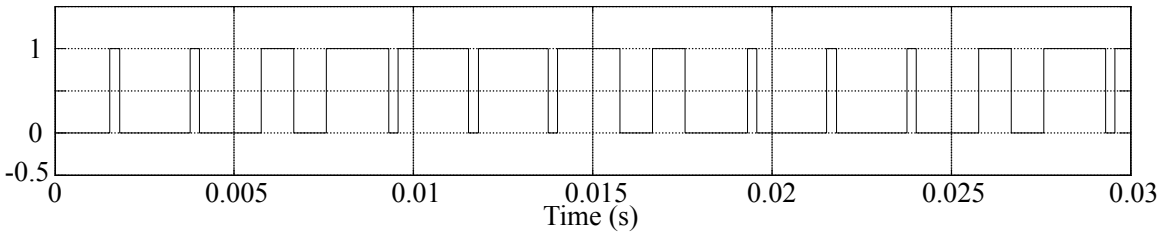
Figure 3.1: Switching functions, carrier and modulation signals of SPWM.



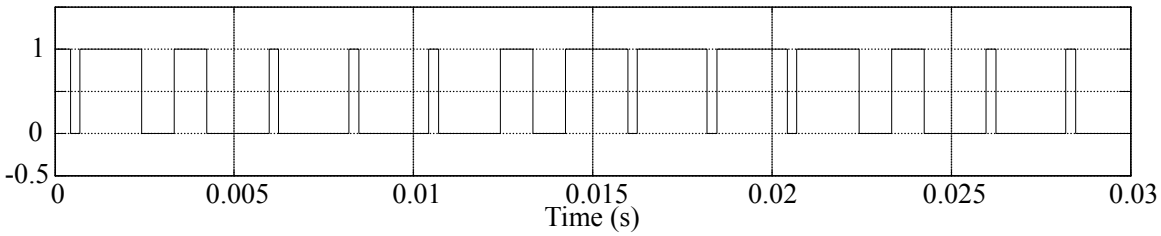
(a) Carrier and modulation signals.



(b) Phase A switching function.

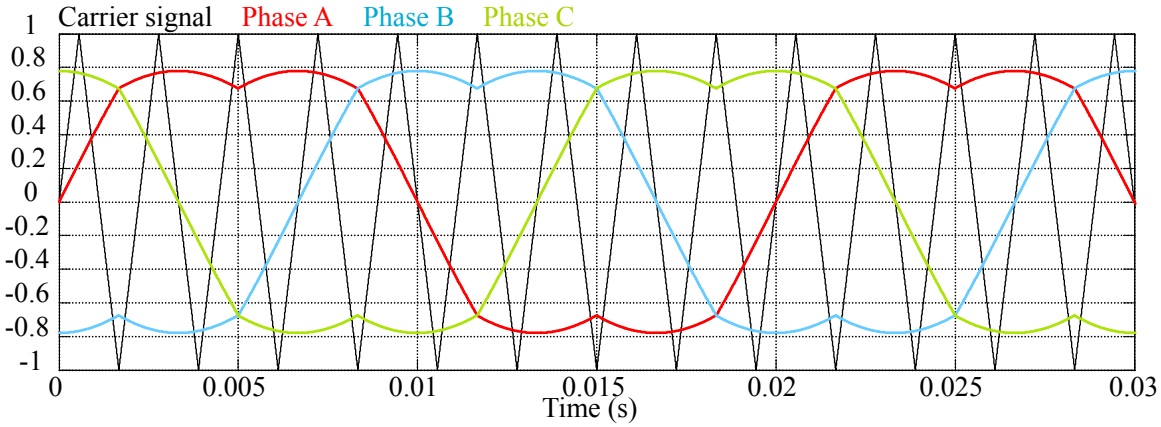


(c) Phase B switching function.

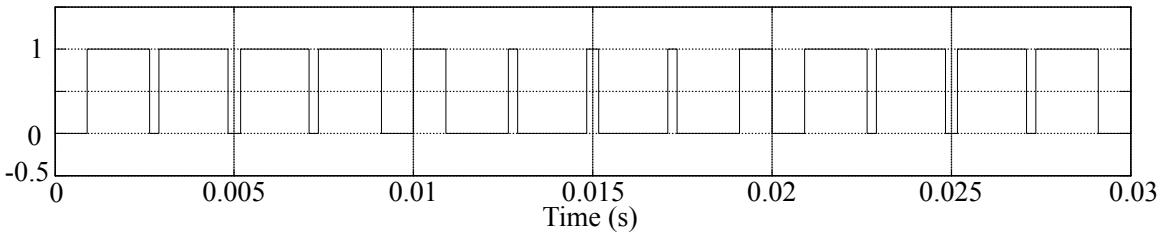


(d) Phase C switching function.

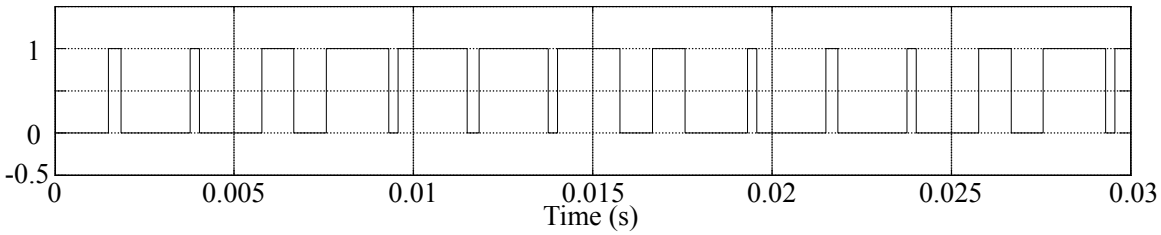
Figure 3.2: Switching functions, carrier and modulation signals of THI.



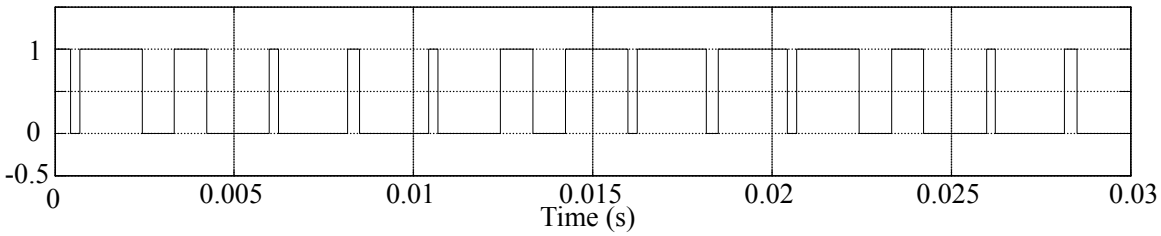
(a) Carrier and modulation signals.



(b) Phase A switching function.



(c) Phase B switching function.



(d) Phase C switching function.

Figure 3.3: Switching functions, carrier and modulation signals of SVPWM.

Different from v_0 in THI, the injection component for SVPWM is not a fixed function of ωt. Two variables are utilized to represent v_0 in SVPWM, they are v_{max} and v_{min} that can be found in (3.3).

$$v_{max} = \max\left[\sin(\omega t), \sin(\omega t - \frac{2\pi}{3}), \sin(\omega t + \frac{2\pi}{3})\right] \tag{3.3a}$$

$$v_{min} = \min\left[\sin(\omega t), \sin(\omega t - \frac{2\pi}{3}), \sin(\omega t + \frac{2\pi}{3})\right] \tag{3.3b}$$

According to the example of modulation signals shown in Figure 3.4, during operating mode 1 and 4, $v_{max} + v_{min} = v_a + v_b$; and, during operating mode 2 and 5, $v_{max} + v_{min} = v_a + v_c$; within operating mode 3 and 6, $v_{max} + v_{min} = v_b + v_c$. Therefore, v_0 in SVPWM can be expressed under these three scenarios respectively, seen in (3.4).

$$v_{0,SVPWM} = \begin{cases} -\frac{1}{2}\sin(\omega t - \frac{\pi}{3}) & \text{, mode 1 and 4} \\ -\frac{1}{2}\sin(\omega t + \frac{\pi}{3}) & \text{, mode 2 and 5} \\ \frac{1}{2}\sin\omega t & \text{, mode 3 and 6} \end{cases} \tag{3.4}$$

3.1.2 Time intervals in a switching period

Different from MOSFET switching transient times discussed in Chapter 2, the time intervals in switching period T_s described in this section are T_0, T_1, T_2, and T_3 shown by Figure 3.6a. The time periods mentioned previously are on the order of nanosecond and are mainly defined by the semiconductor itself. To some extent, the time

intervals in switching transients are characteristics of the MOSFET and could not be regulated. In contrast, the time intervals illustrated here that are usually on the order of millisecond or microsecond are decided by the control algorithms and they are related to duty cycles of the switches. Time intervals in the switching period are related to the control algorithm, thus they are acquired depending on different PWM techniques.

Waveforms of the three-phase modulation signal in SPWM are plotted in Figure 3.4. In this figure, it is clear that there are six operating modes in a sinusoidal period. According to Figure 3.1 to Figure 3.3, there are similar operating modes in the modulation methods of THI and SVPWM. The analysis and derivation of the time intervals in the switching period are illustrated based on different PWM techniques and operating modes.

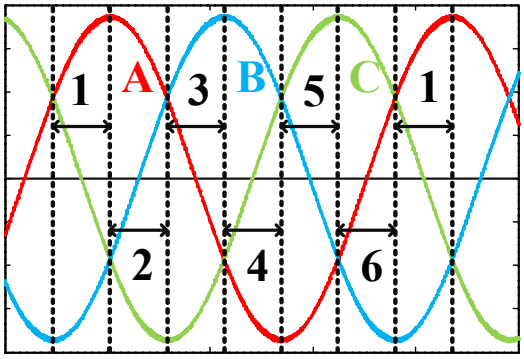


Figure 3.4: Inverter modulation signals.

In order to indicate the relationship between the modulation and carrier signals, waveforms in SPWM are used as an example and are shown by Figure 3.5, in which the phase A modulation signal and the carrier signal are shifted up by V_C for the calculation convenience.

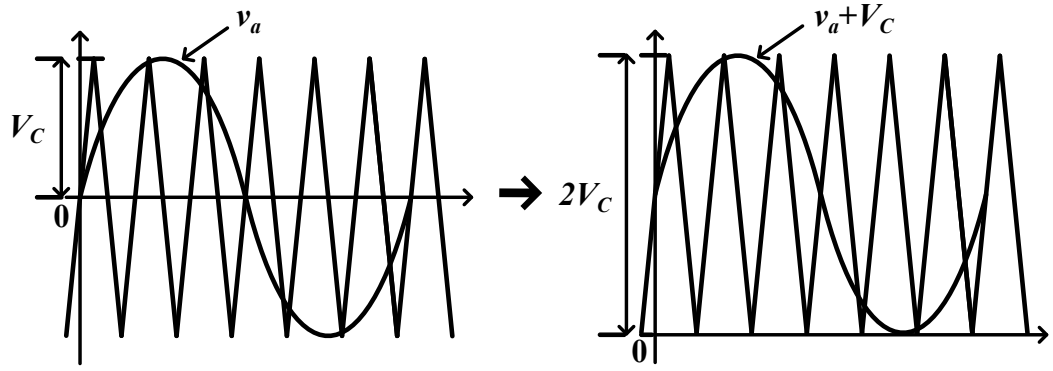
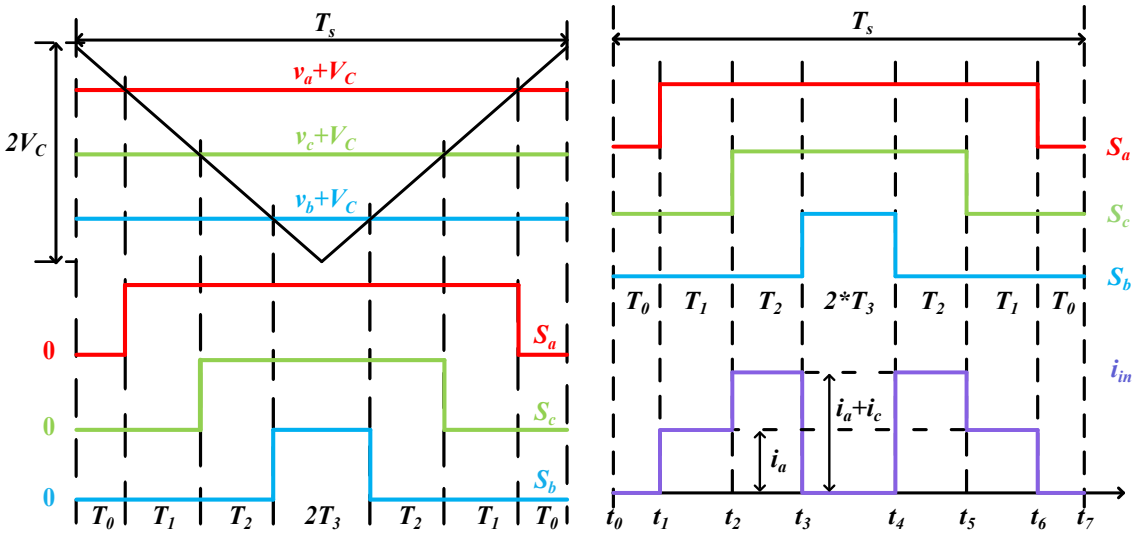


Figure 3.5: Carrier and phase A modulation signals in SPWM.

Although the value of modulation signal varies sinusoidally, it can be assumed constant within the switching period when the switching frequency is high enough. With the hypothesis that values of the modulation signals are constant within T_s, switching functions, S_a, S_b, and S_c, for switches in each phase leg can be derived by comparing the modulation signals with the carrier signal. When the value of the modulation signal is higher than that of the carrier signal, the upper switch in the corresponding phase is on; in contrast, if the value of the carrier signal is higher, the lower switch is on instead. In operating mode 1, the modulation and carrier signals in T_s are shown in Figure 3.6a and the duty cycle of each switch is defined by T_0, T_1, T_2, and T_3. By solving the geometrical problems presented in Figure 3.6a, the correlation between T_1, T_2, T_3, and T_s can be interpreted by (3.5) to (3.7).

$$\frac{2T_3}{T_s} = \frac{v_b + V_C}{2V_C} \tag{3.5}$$

$$\frac{2T_2 + 2T_3}{T_s} = \frac{v_c + V_C}{2V_C} \tag{3.6}$$



(a) Switching functions obtained from modulation and carrier signals.

(b) Ideal inverter input current obtained based on three phase switching functions.

Figure 3.6: Waveforms of the carrier and modulation signals, switching functions and inverter input current in switching period T_s.

$$\frac{2T_1 + 2T_2 + 2T_3}{T_s} = \frac{v_a + V_C}{2V_C} \tag{3.7}$$

After that, T_0 is acquired based on the expressions above in (3.8).

$$2T_0 = T_s - (2T_1 + 2T_2 + 2T_3) \tag{3.8}$$

Now utilizing (3.1), those time intervals are denoted by the modulation signals for the inverter three-phase output voltage; and they are written in (3.9) to (3.12).

$$T_0 = \frac{T_s}{4} \cdot \left(1 - \frac{v_a}{V_C}\right) \tag{3.9}$$

$$T_1 = \frac{T_s}{4} \cdot \frac{v_a - v_c}{V_C} \tag{3.10}$$

$$T_2 = \frac{T_s}{4} \cdot \frac{v_c - v_b}{V_C} \tag{3.11}$$

$$T_3 = \frac{T_s}{4} \cdot \left(1 + \frac{v_b}{V_C}\right) \tag{3.12}$$

Substituting (3.1) into (3.9) to (3.12), T_0, T_1, T_2, and T_3 are expressed by (3.13) to (3.16) including the injection signal v_0.

$$T_0 = \frac{T_s}{4} \cdot \left[1 - M \cdot \left(\sin(\omega t) + v_0 \right)\right] \tag{3.13}$$

$$T_1 = \frac{T_s}{4} \cdot M \cdot \left[\sin(\omega t) - \sin(\omega t + \frac{2\pi}{3})\right] \tag{3.14}$$

$$T_2 = \frac{T_s}{4} \cdot M \cdot \left[\sin(\omega t + \frac{2\pi}{3}) - \sin(\omega t - \frac{2\pi}{3})\right] \tag{3.15}$$

$$T_3 = \frac{T_s}{4} \cdot \left[1 + M \cdot \left(\sin(\omega t - \frac{2\pi}{3}) + v_0\right)\right] \tag{3.16}$$

Obviously, in the calculations for T_1 and T_2, the injected items cancel each other and v_0 does not exist in the final expressions. In contrast, v_0 appears in the equations for T_0 and T_3. It can be concluded that the calculations of T_0 and T_3 are swayed by distinct injection signals; at the same time, the derivations for T_1 and T_2 are irrelevant to v_0.

Consequently, T_1 and T_2 are represented in (3.17) and (3.18) by simplifying (3.14) and (3.15).

$$T_1 = \frac{\sqrt{3}}{4} T_s \cdot M \cdot \sin(\omega t - \frac{\pi}{6}) \tag{3.17}$$

$$T_2 = \frac{\sqrt{3}}{4} T_s \cdot M \cdot \cos \omega t \tag{3.18}$$

Depending on various injection signals, the computations for T_0 and T_3 are different. Thus the derivations of T_0 and T_3 are illustrated individually based on three PWM techniques, SPWM, THI, and SVPWM, and their injection signals.

SPWM

In SPWM, it is known that the injection signal v_0 is equal to zero. Thus, T_0 and T_3 can be obtained by solving (3.19) and (3.20).

$$T_0 = \frac{T_s}{4} \cdot \Big[1 - M \cdot \sin(\omega t) \Big] \tag{3.19}$$

$$T_3 = \frac{T_s}{4} \cdot \Big[1 + M \cdot \sin(\omega t - \frac{2\pi}{3}) \Big] \tag{3.20}$$

THI

With THI technique, v_0 is given by the second item in (3.2). Then, T_0 and T_3 are shown by (3.21) and (3.22).

$$T_0 = \frac{T_s}{4} \cdot \Big[1 - M \cdot \Big(\sin(\omega t) + \frac{1}{6} \sin(3\omega t) \Big) \Big] \tag{3.21}$$

$$T_3 = \frac{T_s}{4} \cdot \left[1 - M \cdot \left(\sin(\omega t + \frac{\pi}{3}) - \frac{1}{6} \sin(3\omega t) \right) \right] \tag{3.22}$$

SVPWM

Due to three different expressions of v_0 when the technique of SVPWM is utilized, T_0 and T_3 are calculated under three scenarios described by (3.4).

During operating mode 1 and 4, T_0 and T_3 are obtained by (3.23).

$$T_0 = T_3 = \frac{T_s}{4} \cdot \left[1 - \frac{\sqrt{3}}{2} M \cdot \sin(\omega t + \frac{\pi}{6}) \right] \tag{3.23}$$

During operating mode 2 and 5, T_0 and T_3 are obtained by (3.24) and (3.25).

$$T_0 = \frac{T_s}{4} \cdot \left[1 - \frac{\sqrt{3}}{2} M \cdot \sin(\omega t - \frac{\pi}{6}) \right] \tag{3.24}$$

$$T_3 = \frac{T_s}{4} \cdot \left[1 - \frac{3}{2} M \cdot \sin(\omega t + \frac{\pi}{6}) \right] \tag{3.25}$$

During operating mode 3 and 6, T_0 and T_3 are obtained by (3.26) and (3.27).

$$T_0 = \frac{T_s}{4} \cdot \left[1 - \frac{3}{2} M \cdot \sin(\omega t) \right] \tag{3.26}$$

$$T_3 = \frac{T_s}{4} \cdot \left[1 - \frac{\sqrt{3}}{2} M \cdot \cos(\omega t) \right] \tag{3.27}$$

So far, the time intervals in T_s are analyzed and they will be used in the DC-link

current and voltage ripple calculations below.

3.2 DC-Link Current Analysis

The current flow in the DC-link is shown in Figure 2.9, by which correlation among the source current i_s, the inverter input current i_{in} and the capacitor current i_{cap} is indicated. In this section, a commonly used and the proposed method for i_{in} and i_{cap} calculation are introduced.

3.2.1 DC-link current

In the beginning, the analysis of the i_{in} in switching period T_s is addressed, based on which the average inverter input current $I_{ave,in}$ and the RMS value of the inverter input current $I_{rms,in}$ are calculated. Then, RMS value of the DC-link ripple current $I_{rms,ripple}$ can be obtained from $I_{ave,in}$ and $I_{rms,in}$. With the switching functions for three phases, S_a, S_b and S_c, i_{in} is expressed by (3.28); and the values of these three switching functions are 1 or 0. When the switching function of a phase leg is at 1, the upper switch in the corresponding phase will be turned on; in contrast, the lower switch will be turned on when the switching function is set at 0.

$$i_{in} = S_a \cdot i_a + S_b \cdot i_b + S_c \cdot i_c \tag{3.28}$$

Obviously, i_{in} can be directly represented by the currents in three upper switches. The inverter input current is zero when all of the switching functions are 0 or 1. It is easy to understand the zero scenario; and, when all of the switching function values are 1, i_{in} can be written in the form of (3.29).

$$i_{in} = i_a + i_b + i_c \tag{3.29}$$

Considering Kirchhoff's current law, the relationship among these three phase currents satisfies (3.30). Thus, when all of three switching functions are 1, the inverter input current is equal to zero.

$$i_a + i_b + i_c = 0 \tag{3.30}$$

Thus, according to the inverter input current waveform shown in Figure 3.6b, this input current can be expressed by (3.31).

$$i_{in} = \begin{cases} 0 & , t_0 \leq t < t_1 \\ i_a & , t_1 \leq t < t_2 \\ i_a + i_c & , t_2 \leq t < t_3 \\ 0 & , t_3 \leq t < t_4 \\ i_a + i_c & , t_4 \leq t < t_5 \\ i_a & , t_5 \leq t < t_6 \\ 0 & , t_6 \leq t < t_7 \end{cases} \tag{3.31}$$

Utilizing RMS value of the output phase voltage, three-phase voltage modulation signals for the inverter can also be represented by (3.32), where $\sqrt{2}V_{rms} = M \cdot V_C$.

$$\begin{aligned} v_a &= \sqrt{2}V_{rms} \cdot (\sin \omega t + v_0) \\ v_b &= \sqrt{2}V_{rms} \cdot \left[\sin(\omega t - \frac{2\pi}{3}) + v_0\right] \\ v_c &= \sqrt{2}V_{rms} \cdot \left[\sin(\omega t + \frac{2\pi}{3}) + v_0\right] \end{aligned} \tag{3.32}$$

Similarly to the output voltage expression above, three-phase output current of the inverter can be written in the form of (3.33).

$$\begin{aligned} i_a &= \sqrt{2}I_{rms} \cdot \sin(\omega t - \phi) \\ i_b &= \sqrt{2}I_{rms} \cdot \sin(\omega t - \frac{2}{3}\pi - \phi) \\ i_c &= \sqrt{2}I_{rms} \cdot \sin(\omega t + \frac{2}{3}\pi - \phi) \end{aligned} \tag{3.33}$$

Then the DC-link input average current $i_{ave,in}$ during T_s is described by (3.34).

$$\begin{aligned} i_{ave,in} &= \frac{1}{T_s} \cdot \int_0^{T_s} i_{in} \cdot \mathrm{d}t = \frac{1}{T_s} \cdot \left[2\int_{t_1}^{t_2} i_a \cdot \mathrm{d}t + 2\int_{t_2}^{t_3} (i_a + i_c) \cdot \mathrm{d}t\right] \\ &= \frac{1}{T_s} \cdot \left(2\int_{t_1}^{t_2} i_a \cdot \mathrm{d}t - 2\int_{t_2}^{t_3} i_b \cdot \mathrm{d}t\right) \\ &= \frac{2}{T_s} \cdot (T_1 \cdot i_a - T_2 \cdot i_b) \end{aligned} \tag{3.34}$$

The calculation for $i_{rms,in}$ in switching period T_s is obtained in (3.35).

$$
\begin{aligned}
{i^2}_{rms,in} &= \frac{1}{T_s} \cdot \int_0^{T_s} i_{in}^2 \cdot \mathrm{d}\omega t = \frac{1}{T_s} \cdot \left[2 \int_{t_1}^{t_2} i_a^2 \cdot \mathrm{d}t + 2 \int_{t_2}^{t_3} (i_a + i_c)^2 \cdot \mathrm{d}t \right] \\
&= \frac{1}{T_s} \cdot \left(2 \int_{t_1}^{t_2} i_a^2 \cdot \mathrm{d}t + 2 \int_{t_2}^{t_3} i_b^2 \cdot \mathrm{d}t \right) \\
&= \frac{2}{T_s} \cdot \left(T_1 \cdot i_a^2 + T_2 \cdot i_b^2 \right)
\end{aligned}
\tag{3.35}
$$

Considering the inverter current during T_s in Figure 3.6b, it is obvious that the inverter average and RMS current should be only related to T_1 and T_2; and it is proved by (3.34) and (3.35). Additionally, injection signals in different PWM techniques do not exist in the calculations for T_1 and T_2. Thus, there is no significant difference among the DC-link currents under different PWM techniques, which is also demonstrated by (Dahono *et al.*, 1996; Kolar and Round, 2006). When substitute the inverter output current in (3.33) into (3.34) and (3.35), the average and RMS inverter input current are the functions of inverter output current and can be rewritten by (3.36) and (3.37).

$$
i_{ave,in} = \frac{2\sqrt{2}T_1}{T_s} \cdot I_{rms} \cdot \sin(\omega t - \phi) - \frac{2\sqrt{2}T_2}{T_s} \cdot I_{rms} \cdot \sin(\omega t - \frac{2}{3}\pi - \phi) \tag{3.36}
$$

$$
{i^2}_{rms,in} = \frac{4T_1}{T_s} \cdot I_{rms}^2 \cdot \sin^2(\omega t - \phi) + \frac{4T_2}{T_s} \cdot I_{rms}^2 \cdot \sin^2(\omega t - \frac{2}{3}\pi - \phi) \tag{3.37}
$$

Now that, the expressions are acquired in the period of T_s, integration can be taken based on the sinusoidal period of the output current. Solutions for $I_{ave,in}$ and

$I_{rms,in}$ calculations during different inverter operating modes shown in Figure 3.4 are the same; thus, to obtain the averaged values, the integration is taken in the period of operating mode 1, from $\frac{\pi}{6}$ to $\frac{\pi}{2}$. Then $I_{ave,in}$ and $I_{rms,in}$ are obtained by (3.38) and (3.39).

$$I_{ave,in} = \frac{3}{\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} i_{ave,in}\cdot \mathrm{d}\omega t = \frac{3\sqrt{2}}{4} I_{rms}\cdot M\cdot\cos\phi \tag{3.38}$$

$$I^2{}_{rms,in} = \frac{3}{\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} i^2{}_{rms,in}\cdot \mathrm{d}\omega t = \frac{3\sqrt{3}M\cdot I^2{}_{rms}}{2\pi}\cdot\left(1+\frac{2}{3}\cos 2\phi\right) \tag{3.39}$$

Utilizing $I_{ave,in}$ and $I_{rms,in}$, the RMS value of DC-link ripple current $I_{rms,ripple}$ is then derived by (3.40) based upon the existing method (Kolar and Round, 2006).

$$\begin{aligned} I_{rms,ripple} &= \sqrt{I^2{}_{rms,in} - I^2{}_{ave,in}} \\ &= I_{rms}\cdot\sqrt{\frac{\sqrt{3}M}{2\pi} + \left(\frac{2\sqrt{3}M}{\pi} - \frac{9}{8}M^2\right)\cdot\cos^2\phi} \end{aligned} \tag{3.40}$$

The inverter input current is assumed ideal in this section, thus the estimation accuracy of the average and RMS input current cannot be guaranteed; since, the practical inverter input current is not ideal and is affected by some other factors, such as inverter anti-parallel diode reverse recovery. In this case, the proposed method is developed to estimate the average and RMS input current as well as the RMS value of the DC-link current ripple by considering diode reverse recovery. In the following section, the inverter anti-parallel diode reverse recovery is discussed before the proposed method is introduced.

3.2.2 Inverter anti-parallel diode reverse recovery

The diode reverse recovery occurs when the diode turns off, which is shown in Figure 3.7. When a diode is turning off, firstly the diode forward current i_f decreases from the load current to zero. After that, the diode current rises in the opposite direction of i_f to discharge the energy stored inside the diode during its turn-on period; at this moment, the diode current is also named as reverse recovery current. When the reverse recovery current reaches its maximum value I_{rr}, it starts to fall. The diode is completely off when its current decreases to zero again (Dastfan, 2007; Schonberger and Feix, 2008). The amount of the charge stored in the diode is reverse recovery charge Q_{rr}. The reverse recovery time t_{rr} is the time duration for Q_{rr} discharging. A detailed analysis of diode reverse recovery transient is presented to derive the solutions to DC-link current and its RMS value estimation; two time intervals within t_{rr}, t_a and t_b, are also discussed individually.

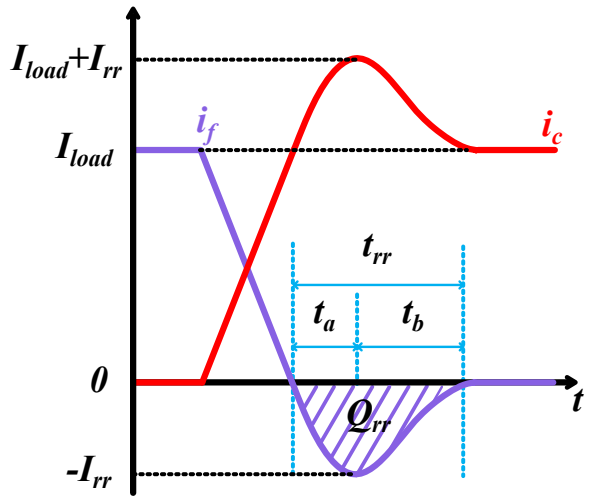


Figure 3.7: Diode reverse recovery current and its corresponding switch current.

Diode reverse recovery transient

Generally, the total reverse recovery time t_{rr}, current I_{rr} and charge Q_{rr} are provided by most of the manufacturer datasheets, while the reverse recovery time can be divided into two parts shown in (3.41).

$$t_{rr} = t_a + t_b \tag{3.41}$$

From Figure 3.7, it can be seen that when the current of a diode falls from I_{load} to zero, the current through its corresponding switch rises from zero to I_{load}, and a change rate s of the switch current i_{switch} can be obtained in (3.42), which is assumed constant before i_{switch} reaches $I_{load} + I_{rr}$.

$$s = \frac{\mathrm{d}i_{switch}}{\mathrm{d}t} = \frac{I_{load}}{t_{ri}} \tag{3.42}$$

Furthermore, the time t_{ri} for i_{switch} rises from zero to $I_{load}+I_{rr}$ is equal to the time for diode current falls from I_{load} to $-I_{rr}$. Thus, s denotes not only the change rate of i_{switch} but also the change rate of i_f and diode reverses recovery current. Therefore, s can also be represented by (3.43).

$$s = \frac{I_{rr}}{t_a} \tag{3.43}$$

As a result, the time interval t_a can be obtained by (3.44).

$$t_a = \frac{I_{rr}}{s} \tag{3.44}$$

Then, t_b can be calculated under two different scenarios. On one hand, when t_{rr} is given by the datasheet, based on (3.41) time interval t_b can be obtained directly by (3.45). On the other hand, when s and Q_{rr} are given by the datasheet rather than t_{rr}, time intervals t_a and t_b can be obtained by (3.46) and (3.47).

$$t_b = t_{rr} - t_a \tag{3.45}$$

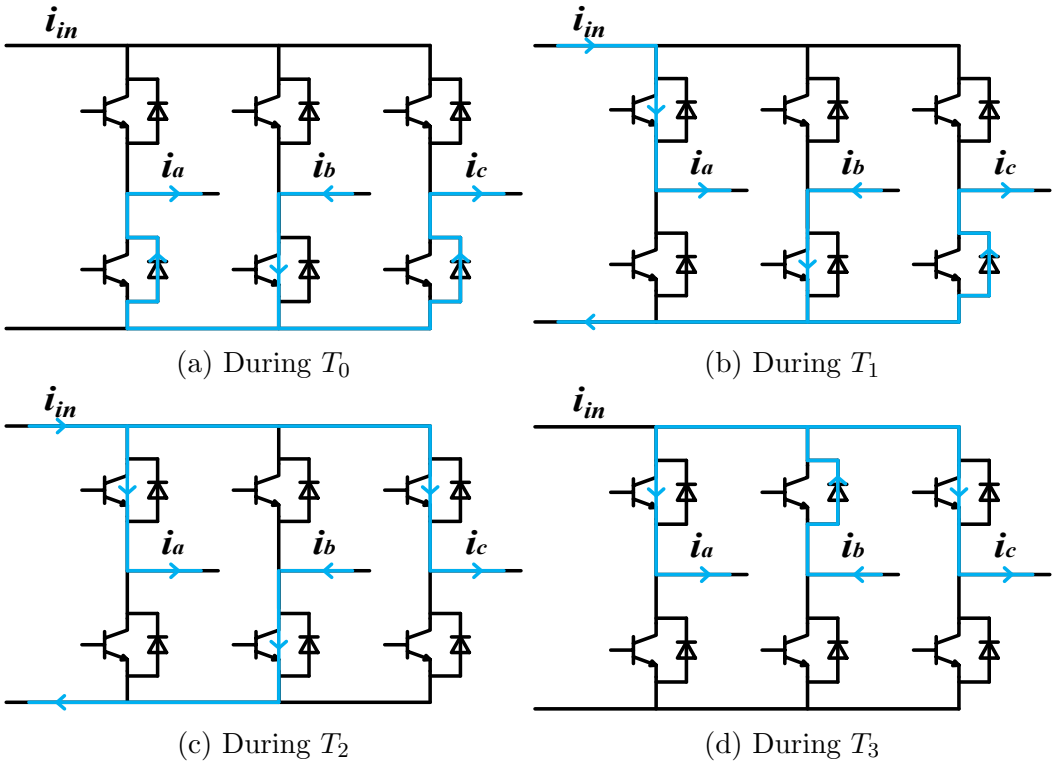
$$Q_{ra} = \frac{1}{2} I_{rr} \cdot t_a \tag{3.46}$$

$$t_b = \frac{2(Q_{rr} - Q_{ra})}{I_{rr}} = \frac{2Q_{rr}}{I_{rr}} - t_a \tag{3.47}$$

Occurrence of diode reverse recovery in T_s

Considering the reverse recovery transient, the expression of the inverter input current i_{in} should be different from the original one during T_s. The proposed method is used to evaluate the DC-link ripple current utilizing the modified current expression that includes t_a and t_b.

With symmetric three-phase load, the inverter performances in six operating modes are similar to each other; as a result, the analysis is illustrated with the assumption that the inverter is operated in mode 1. If currents in phase A and C are positive while it is negative in phase B, current paths are shown in Figure 3.8. During the first T_0 (from $t = t_0$ to $t = t_1$ in Figure 3.6), all of switching functions are at 0 and three lower switches are on. Thus, the inverter input current is equal to zero. As it can be seen in Figure 3.8a, the current is circulating in phase B lower switch, load, phase A and C lower diodes.



(a) During T_0 (b) During T_1

(c) During T_2 (d) During T_3

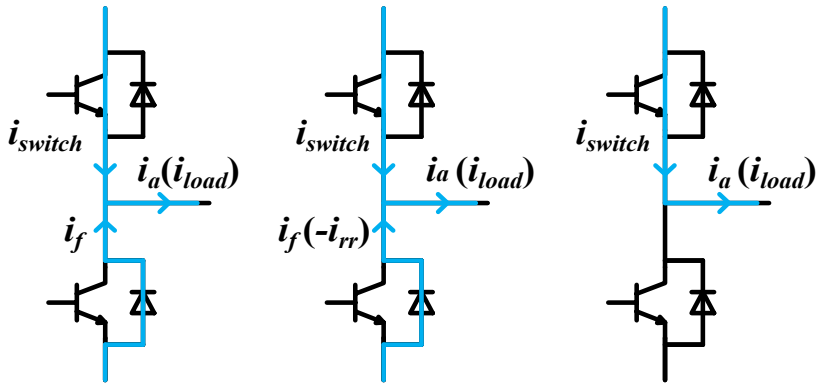
Figure 3.8: Inverter current flow within T_s in operating mode 1, when phase A and C currents are positive and phase B current is negative.

At $t = t_1$, the upper switch is closed and the lower diode turns off in phase A. As it is presented in Figure 3.7, the lower diode current i_f is positive and falls from the load current to zero in the beginning. After that, diode reverse recovery current rises to its peak value I_{rr} in the opposite direction. Finally, when the reverse recovery current falls to zero again, the diode is completely off. At the same time, the current in phase A upper switch rises to load current. During the first T_1 (from $t = t_1$ to $t = t_2$ in Figure 3.6), phase A upper switch and the other two lower switches are on. As a result, the current flow in the inverter is shown in Figure 3.8b. At this moment, the inverter input current is equal to phase A current i_a. Figure 3.9a shows the current flow paths and transient equivalent circuit when $t = t_1$, while the current

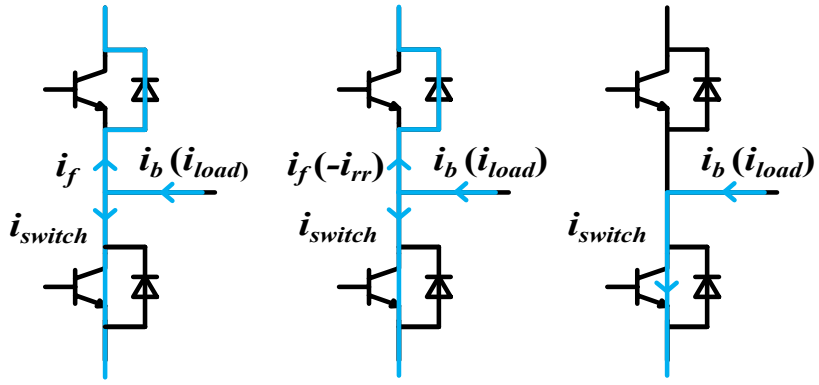
relationship is represented by (3.48).

$$i_{switch} + i_f = i_a \tag{3.48}$$

Therefore, the reverse recovery occurs at $t = t_1$. It is known that the diode reverse recovery only takes place within the diode turn-off transient; consequently, a simple way to determine when the reverse recovery occurs during T_s is to define the moment when a diode turns off.



(a) Phase A.



(b) Phase B.

Figure 3.9: Inverter current flow paths during anti-parallel diode reverse recovery transients in operating mode 1.

When $t = t_2$, the upper switch is turned on and the lower diode turns off in phase C. The current map is shown in Figure 3.8c. Therefore, the reverse recovery also occurs at $t = t_2$. In addition, during the first T_2 (from $t = t_2$ to $t = t_3$ in Figure 3.6), phase A and C upper switch and phase B lower switch are on. The inverter input current is equal to the sum of phase A and C currents. When $t = t_3$, phase B lower switch is turned off and it is not turned on again until $t = t_4$. Similarly, at $t = t_4$ phase B upper diode turns off; and the current flow in phase B upper diode and lower switch during this period is shown in Figure 3.9b. Thus, during T_s, the anti-parallel diode reverse recovery occurs at $t = t_1$, t_2 and t_4.

The occurrence of the anti-parallel diode reverse recovery is validated by both simulations and experiments. Ensuring the simulation result is comparable to the experimental result, the simulation circuit is built with the same topology as that used in practical experiment set-up. Figure 3.10 shows the simulation circuit.

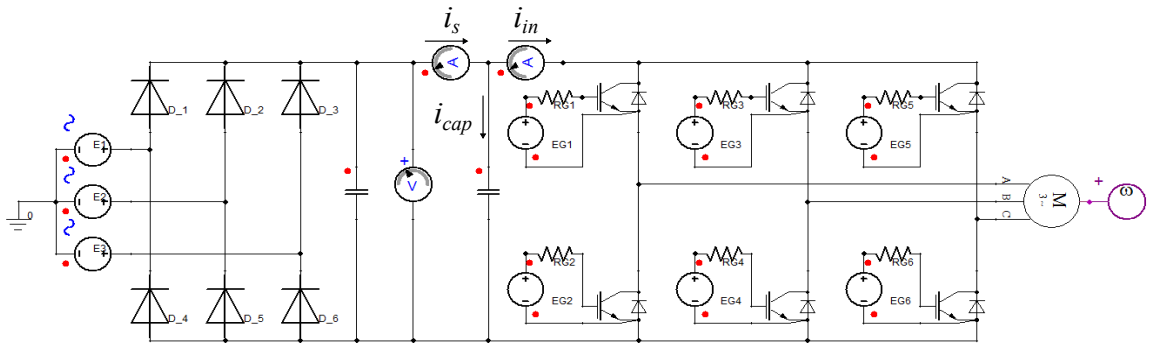


Figure 3.10: Simulation circuit.

The simulation is implemented in ANSYS SIMPLORER. It should be noticed that the switches, IGBTs and anti-parallel diodes, utilized in the simulations are not ideal devices selected from the libraries; instead, they are characterized depending on the manufacturer datasheets of IGBT modules used in the designed inverter. The data

of inverter input current in T_s are obtained and plotted in Figure 3.11, in which one of the switching periods starts at $t = 10.5$ms and ends at $t = 10.6$ms. Comparing the simulation results to the analysis, it is validated that the diode reverse recovery occurs at t_1, t_2, and t_4. Besides, the waveforms captured from experiments also verify the analysis and they are shown in Figure 3.12.

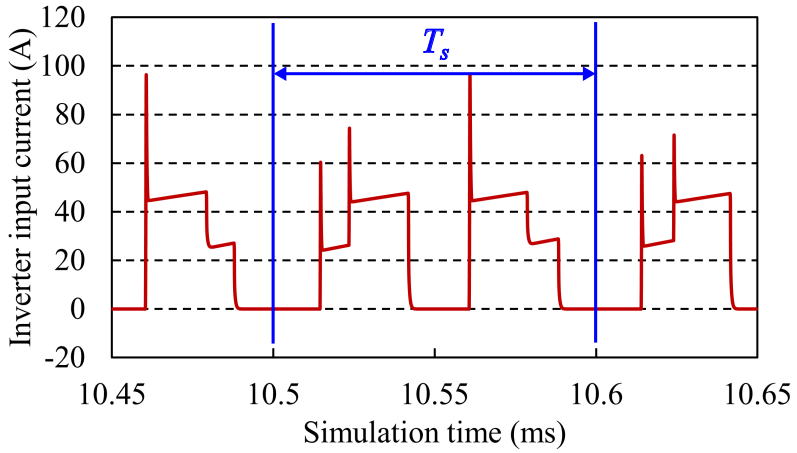


Figure 3.11: Simulation data plot of the inverter input current.

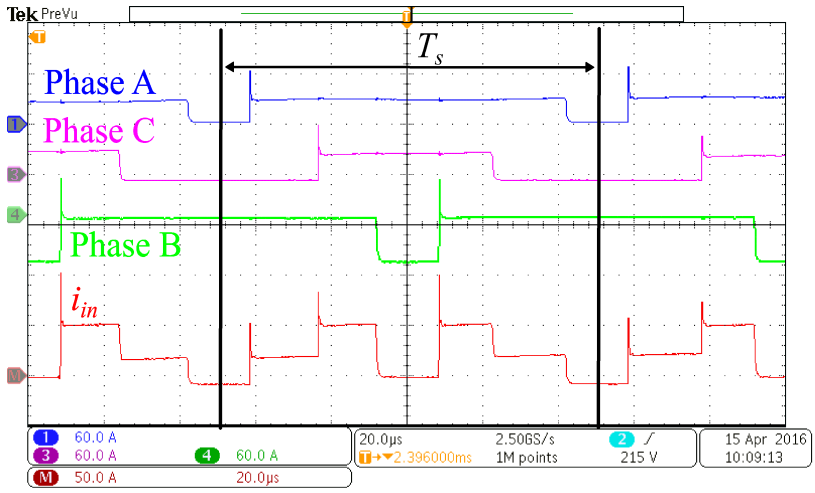


Figure 3.12: Experimental waveforms of the inverter input current.

3.2.3 DC-link current considering anti-parallel diode reverse recovery

The analysis for inverter input current is addressed previously neglecting the influence of diode reverse recovery current that in fact also contributes to the inverter input current and ripple current. Thus, the proposed method is introduced in this section to estimate $I_{rms,ripple}$ by taking the diode reverse recovery current and time into account.

Considering the reverse recovery transient, the switching period T_s is not simply divided into time intervals shown in Figure 3.6, and therefore the expression of the inverter input current i_{in} is different from the original one. As the diode reverse recovery occurs at $t = t_1$, t_2 and t_4, to express the inverter input current i_{in} more accurately, T_s can be divided into more small periods.

Furthermore, with the relationship among inverter three phase currents described by (3.30), the sum of phase A and C currents can also be presented by phase B current shown in (3.49).

$$i_a + i_c = -i_b \tag{3.49}$$

Then, by including (3.49), t_a, t_b, t_{rr}, and I_{rr} in the expression of the inverter input current, i_{in} can be written in the form of (3.50).

$$i_{in} = \begin{cases} 0 & , t_0 \le t < t_1 \\ i_a + \frac{I_{rr}}{t_a} \cdot (t - t_1) & , t_1 \le t < t_1 + t_a \\ i_a + \frac{I_{rr}}{t_b} \cdot (t_1 + t_{rr} - t) & , t_1 + t_a \le t < t_1 + t_{rr} \\ i_a & , t_1 + t_{rr} \le t < t_2 \\ -i_b + \frac{I_{rr}}{t_a} \cdot (t - t_2) & , t_2 \le t < t_2 + t_a \\ -i_b + \frac{I_{rr}}{t_b} \cdot (t_2 + t_{rr} - t) & , t_2 + t_a \le t < t_2 + t_{rr} \\ -i_b & , t_2 + t_{rr} \le t < t_3 \\ 0 & , t_3 \le t < t_4 \\ -i_b + \frac{I_{rr}}{t_a} \cdot (t - t_4) & , t_4 \le t < t_4 + t_a \\ -i_b + \frac{I_{rr}}{t_b} \cdot (t_4 + t_{rr} - t) & , t_4 + t_a \le t < t_4 + t_{rr} \\ -i_b & , t_4 + t_{rr} \le t < t_5 \\ i_a & , t_5 \le t < t_6 \\ 0 & , t_6 \le t < t_7 \end{cases} \tag{3.50}$$

With the consideration of diode reverse recovery,the average inverter input current within T_s is derived by (3.51).

$$
\begin{aligned}
i_{ave,in} = \frac{1}{T_s}\cdot\int_0^{T_s} i_{in}\cdot \mathrm{d}t = \frac{1}{T_s}\cdot\Bigg[&\int_{t_1}^{t_1+t_a}\left[i_a + \frac{I_{rr}}{t_a}\cdot(t-t_1)\right]\cdot \mathrm{d}t + \int_{t_1+t_{rr}}^{t_2} i_a\cdot \mathrm{d}t \\
&+ \int_{t_1+t_a}^{t_1+t_{rr}}\left[i_a + \frac{I_{rr}}{t_b}\cdot(t_1+t_{rr}-t)\right]\cdot \mathrm{d}t + \int_{t_2}^{t_2+t_a}\left[-i_b + \frac{I_{rr}}{t_a}\cdot(t-t_2)\right]\cdot \mathrm{d}t \\
&+ \int_{t_2+t_a}^{t_2+t_{rr}}\left[-i_b + \frac{I_{rr}}{t_b}\cdot(t_2+t_{rr}-t)\right]\cdot \mathrm{d}t + \int_{t_4}^{t_4+t_a}\left[-i_b + \frac{I_{rr}}{t_a}\cdot(t-t_4)\right]\cdot \mathrm{d}t \\
&- \int_{t_2+t_{rr}}^{t_3} i_b\cdot \mathrm{d}t + \int_{t_4+t_a}^{t_4+t_{rr}}\left[-i_b + \frac{I_{rr}}{t_b}\cdot(t_4+t_{rr}-t)\right]\cdot \mathrm{d}t - \int_{t_4+t_{rr}}^{t_5} i_b\cdot \mathrm{d}t + \int_{t_5}^{t_6} i_a\cdot \mathrm{d}t\Bigg] \\
&= \frac{1}{T_s}\cdot(2T_1\cdot i_a - 2T_2\cdot i_b + \frac{3}{2}\cdot I_{rr}\cdot t_{rr})
\end{aligned}
\tag{3.51}
$$

Then the calculation for $i_{rms,in}$ is obtained in (3.52).

$$
\begin{aligned}
{i^2}_{rms,in} = \frac{1}{T_s}\cdot\int_0^{T_s} i_{in}^2\cdot \mathrm{d}t = \frac{1}{T_s}\cdot\Bigg[&\int_{t_1}^{t_1+t_a}\left[i_a + \frac{I_{rr}}{t_a}\cdot(t-t_1)\right]^2\cdot \mathrm{d}t + \int_{t_1+t_{rr}}^{t_2} i_a^2\cdot \mathrm{d}t \\
&+ \int_{t_1+t_a}^{t_1+t_{rr}}\left[i_a + \frac{I_{rr}}{t_b}\cdot(t_1+t_{rr}-t)\right]^2\cdot \mathrm{d}t + \int_{t_2}^{t_2+t_a}\left[-i_b + \frac{I_{rr}}{t_a}\cdot(t-t_2)\right]^2\cdot \mathrm{d}t \\
&+ \int_{t_2+t_a}^{t_2+t_{rr}}\left[-i_b + \frac{I_{rr}}{t_b}\cdot(t_2+t_{rr}-t)\right]^2\cdot \mathrm{d}t + \int_{t_4}^{t_4+t_a}\left[-i_b + \frac{I_{rr}}{t_a}\cdot(t-t_4)\right]^2\cdot \mathrm{d}t \\
&+ \int_{t_2+t_{rr}}^{t_3} i_b^2\cdot \mathrm{d}t + \int_{t_4+t_a}^{t_4+t_{rr}}\left[-i_b + \frac{I_{rr}}{t_b}\cdot(t_4+t_{rr}-t)\right]^2\cdot \mathrm{d}t + \int_{t_4+t_{rr}}^{t_5} i_b^2\cdot \mathrm{d}t + \int_{t_5}^{t_6} i_a^2\cdot \mathrm{d}t\Bigg] \\
&= \frac{1}{T_s}\cdot(2T_1\cdot i_a^2 + 2T_2\cdot i_b^2 + I_{rr}\cdot t_{rr}\cdot i_a - 2I_{rr}\cdot t_{rr}\cdot i_b + I_{rr}^2\cdot t_{rr})
\end{aligned}
\tag{3.52}
$$

Substituting i_a and i_b into (3.51) and (3.52), the average and RMS current during T_s are finally acquired by (3.53) and (3.54).

$$i_{ave,in} = \frac{1}{T_s}\cdot\left(2T_1\cdot\sin(\omega t-\phi) - 2T_2\cdot\sin(\omega t-\frac{2}{3}\pi-\phi) + \frac{3}{2}\cdot I_{rr}\cdot t_{rr}\right) \tag{3.53}$$

$$\begin{aligned} {i^2}_{rms,in} = \frac{1}{T_s}\cdot\Bigg(&2T_1\cdot\sin^2(\omega t-\phi) + 2T_2\cdot\sin^2(\omega t-\frac{2}{3}\pi-\phi) \\ &+ I_{rr}\cdot t_{rr}\cdot\sin(\omega t-\phi) - 2I_{rr}\cdot t_{rr}\cdot\sin(\omega t-\frac{2}{3}\pi-\phi) + I_{rr}^2\cdot t_{rr}\Bigg) \end{aligned} \tag{3.54}$$

Then, the average and RMS input currents with respect to the sinusoidal period are calculated by (3.55) and (3.56).

$$I_{ave,in} = \frac{3}{\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} i_{ave,in}\cdot \mathrm{d}\omega t = \frac{3\sqrt{2}}{4} I_{rms}\cdot M\cdot\cos\phi + \frac{3I_{rr}\cdot t_{rr}}{2T_s} \tag{3.55}$$

$$\begin{aligned} {I^2}_{rms,in} &= \frac{3}{\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} i_{rms,in}^2\cdot \mathrm{d}\omega t \\ &= \frac{3\sqrt{3}M{I^2}_{rms}}{2\pi}\cdot\left(1+\frac{2}{3}\cos 2\phi\right) + \frac{I_{rr}^2\cdot t_{rr}}{T_s} \\ &+ \frac{3\sqrt{2}I_{rms}\cdot I_{rr}\cdot t_{rr}}{2\pi T_s}\cdot\left(3\sqrt{3}\cos\phi + \sqrt{1-\cos^2\phi}\right) \end{aligned} \tag{3.56}$$

Finally, the DC-link ripple current RMS value $I_{rms,ripple}$ could be acquired in (3.57). It can be seen that the component α in (3.57) is the same as the result

given by the original method in (3.40), and the rest of the components are related to the inverter anti-parallel diode reverse recovery. Therefore, the expressions in (3.57) illustrate that the value of $I_{rms,ripple}$ depends on not only the inverter operating conditions, such as I_{rms}, M and $cos\phi$, but also the inverter switching frequency and the reverse recovery time and current of the anti-parallel diode.

$$\begin{aligned} I_{rms,ripple} &= \sqrt{{I^2}_{rms,in} - {I^2}_{ave,in}} \\ &= \sqrt{\alpha + \beta + \gamma + \lambda} \end{aligned}, \tag{3.57a}$$

$$\alpha = {I^2}_{rms} \cdot \left[\frac{\sqrt{3}M}{2\pi} + \left(\frac{2\sqrt{3}M}{\pi} - \frac{9M^2}{8} \right) \cdot \cos^2\phi \right], \tag{3.57b}$$

$$\beta = \frac{9\sqrt{2} \cdot I_{rms} \cdot I_{rr} \cdot t_{rr} \cdot \cos\phi}{2T_s} \left(\frac{\sqrt{3}}{\pi} - \frac{M}{2} \right), \tag{3.57c}$$

$$\gamma = \frac{3\sqrt{2} \cdot I_{rms} \cdot I_{rr} \cdot t_{rr}}{2\pi T_s} \cdot \sqrt{1 - \cos^2\phi}, \tag{3.57d}$$

$$\lambda = \frac{{I_{rr}}^2 \cdot t_{rr}}{T_s} \cdot \left(1 - \frac{9t_{rr}}{4T_s} \right), \tag{3.57e}$$

The estimated RMS value of the DC-link current ripple can provide a reference for the DC-link capacitor current rating selection.

3.3 DC-Link Voltage Ripple Analysis

The DC-link voltage ripple is analyzed by the existing method that neglects the anti-parallel diode reverse recovery in Section 3.3.1, which is followed by the discussions for voltage ripple evaluation considering diode reverse recovery in Section 3.3.2.

3.3.1 DC-link voltage ripple

The relationship among DC source current i_s, inverter input current i_{in} and DC-link capacitor current i_{cap} is shown by Figure 2.9. Thus, the current flows through the DC-link capacitor i_{cap} can be described by (3.58) (Pei *et al.*, 2015).

$$i_{cap} = i_s - i_{in} \tag{3.58}$$

If each parameter in (3.58) is divided into DC and AC components, the expression of i_{cap} can be rewritten in (3.59). In (3.59), the AC component of i_s is negligible and the DC component of i_{cap} is zero; then (3.60) is utilized to describe the capacitor current i_{cap}.

$$\tilde{i}_{cap} + I_{ave,cap} = \left(\tilde{i}_s + I_{ave,s}\right) - \left(\tilde{i}_{in} + I_{ave,in}\right) \tag{3.59}$$

$$\tilde{i}_{cap} = -\tilde{i}_{in} = I_{ave,in} - i_{in} \tag{3.60}$$

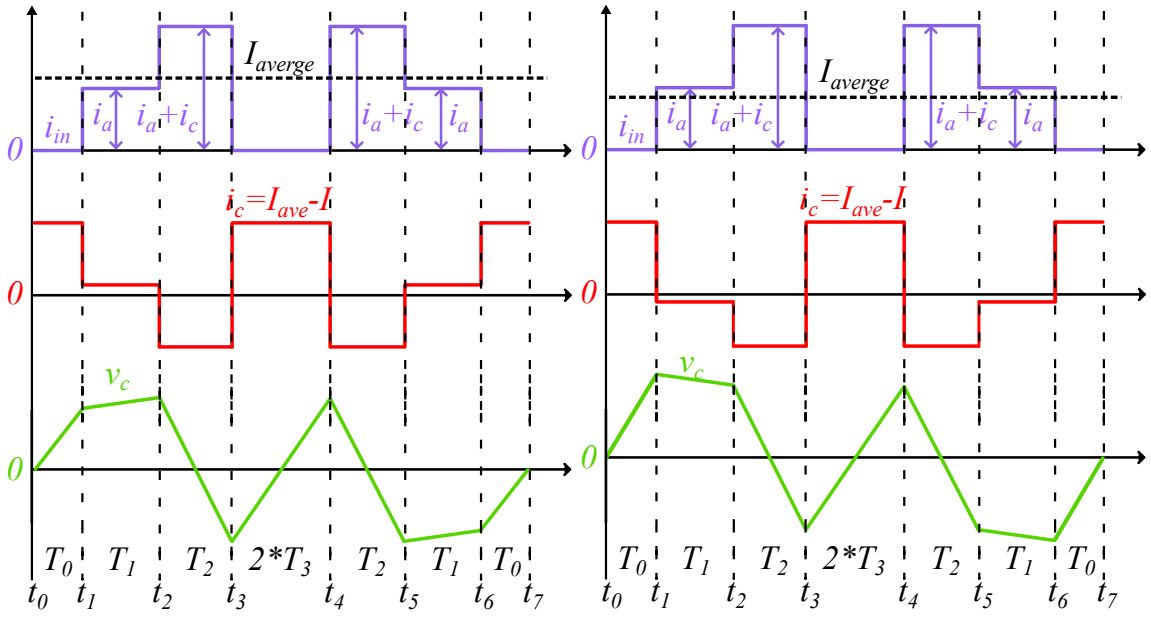
The variation of DC-link capacitor voltage is calculated using i_{cap} in (3.61). Substituting (3.31) into (3.61), the change of DC-link voltage in T_s can be represented by (3.62).

$$\tilde{v}_{cap} = \frac{1}{C} \cdot \int \tilde{i}_{cap} \cdot \mathrm{d}t = \frac{1}{C} \cdot \int -\tilde{i}_{in} \cdot \mathrm{d}t = \frac{1}{C} \cdot \int \left(I_{ave,in} - i_{in}\right) \cdot \mathrm{d}t \tag{3.61}$$

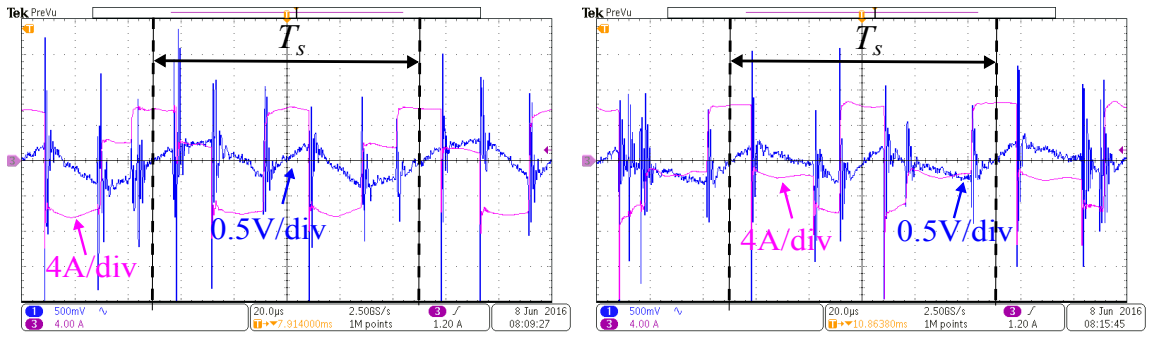
$$\Delta v_c = \frac{1}{C} \cdot \begin{cases} I_{ave,in} \cdot T_0 & , t_0 < t < t_1 \\ (I_{ave,in} - i_a) \cdot T_1 & , t_1 < t < t_2 \\ (I_{ave,in} + i_b) \cdot T_2 & , t_2 < t < t_3 \\ 2 \cdot I_{ave,in} \cdot T_3 & , t_3 < t < t_4 \\ (I_{ave,in} + i_b) \cdot T_2 & , t_4 < t < t_5 \\ (I_{ave,in} - i_a) \cdot T_1 & , t_5 < t < t_6 \\ I_{ave,in} \cdot T_0 & , t_6 < t < t_7 \end{cases} \tag{3.62}$$

It is known that when i_{cap} is positive, the capacitor voltage rises and Δv_{cap} is positive; and, the negative i_{cap} results in the drop of capacitor voltage, then Δv_{cap} is negative. The voltage ripple can be evaluated by the maximum voltage change. Based on (3.60), there are two scenarios shown in Figure 3.13, and the method for Δv_{cap} estimation is shown in (3.63). As a result, the voltage ripple is defined by the maximum voltage change obtained in (3.63). The capacitor current and voltage waveforms analyzed in Figure 3.13a and Figure 3.13b are verified by the DC-link capacitor current and voltage ripples captured by experiments and the waveforms are shown in Figure 3.13c and Figure 3.13d.

$$\Delta v_{cap} = \begin{cases} \Delta v_{cap,T_0} + \Delta v_{cap,T_1} & , i_a < I_{ave} \\ \Delta v_{cap,T_0} & , i_a > I_{ave} \end{cases} \tag{3.63}$$



(a) When $i_a < I_{ave}$. (b) When $i_a > I_{ave}$.



(c) When $i_a < I_{ave}$. (d) When $i_a > I_{ave}$.

Figure 3.13: DC-link capacitor voltage variation in T_s. (a) and (b): waveforms plotted based on analysis; (c) and (d): waveforms captured by experiments, capacitor current is in red and voltage is in blue.

In order to estimate the voltage ripple, the voltage changes in each time interval are calculated individually. Recall the DC-link current ripple evaluation, calculations are only related to the time intervals of T_1 and T_2; thus, the estimations for current ripples are not affected by the modulation injection signals. Different from the current

ripple evaluation, the expressions of DC-link voltage ripple estimation that are shown by (3.62) contain not only T_1 and T_2, but also T_0 and T_3; thus the calculation of voltage ripple is affected by the injection signals. The DC-link voltage changes during T_1 and T_2 are represented by (3.64) and (3.65).

$$\begin{aligned}\Delta v_{cap,T_1} &= \frac{(I_{ave,in} - i_a) \cdot T_1}{C} \\ &= \frac{\sqrt{6} I_{rms} \cdot M}{4C \cdot f_{sw}} \cdot \sin\left(\omega t - \frac{\pi}{6}\right) \cdot \left[\frac{3M}{4}\cos\phi - \sin\left(\omega t - \phi\right)\right]\end{aligned} \tag{3.64}$$

$$\begin{aligned}\Delta v_{cap,T_2} &= \frac{(I_{ave,in} + i_b) \cdot T_2}{C} \\ &= \frac{\sqrt{6} I_{rms} \cdot M}{4C \cdot f_{sw}} \cdot \cos\omega t \cdot \left[\frac{3M}{4}\cos\phi + \sin\left(\omega t - \phi - \frac{2\pi}{3}\right)\right]\end{aligned} \tag{3.65}$$

Then, the voltage changes during T_0 and T_3 are discussed according to different PWM techniques below.

SPWM

With SPWM technique, there is no injection signal added in the modulation waveforms; and according to T_0 and T_3 given in (3.19) and (3.20), the voltage changes during T_0 and T_3 are obtained in (3.66) and (3.67).

$$\Delta v_{cap,T_0} = \frac{I_{ave,in} \cdot T_0}{C} = \frac{3\sqrt{2} I_{rms} \cdot M \cdot \cos\phi}{16C \cdot f_{sw}} \cdot (1 - M \cdot \sin\omega t) \tag{3.66}$$

$$\Delta v_{cap,T_3} = \frac{I_{ave,in} \cdot T_3}{C} = \frac{3\sqrt{2} I_{rms} \cdot M \cdot \cos\phi}{16C \cdot f_{sw}} \cdot \left[1 + M \cdot \sin\left(\omega t - \frac{2\pi}{3}\right)\right] \tag{3.67}$$

THI

When THI is utilized, the injection signal is given by (3.2); then based on (3.21) and (3.22), the voltage changes within T_0 and T_3 are described by (3.68) and (3.69).

$$\Delta v_{cap,T_0} = \frac{I_{ave,in} \cdot T_0}{C} = \frac{3\sqrt{2} I_{rms} \cdot M \cdot \cos\phi}{16C \cdot f_{sw}} \cdot \left[1 - M \cdot (\sin\omega t + \frac{1}{6}\sin 3\omega t)\right] \tag{3.68}$$

$$\begin{aligned} \Delta v_{cap,T_3} &= \frac{I_{ave,in} \cdot T_3}{C} \\ &= \frac{3\sqrt{2} I_{rms} \cdot M \cdot \cos\phi}{16C \cdot f_{sw}} \cdot \left[1 - M \cdot \left(\sin(\omega t + \frac{\pi}{3}) - \frac{1}{6}\sin 3\omega t\right)\right] \end{aligned} \tag{3.69}$$

SVPWM

Depending on the different injection signals used under distinct inverter operating modes, seen in (3.4), when the inverter is operated in mode 1 and 4, the time intervals, T_0 and T_3, are denoted by (3.23); and then the voltage changes are derived in (3.70).

$$\begin{aligned} \Delta v_{cap,T_0} = \Delta v_{cap,T_3} &= \frac{I_{ave,in} \cdot T_0}{C} = \frac{I_{ave,in} \cdot T_3}{C} \\ &= \frac{3\sqrt{2} I_{rms} \cdot M \cdot \cos\phi}{16C \cdot f_{sw}} \cdot \left[1 - \frac{\sqrt{3}}{2} M \cdot \sin(\omega t + \frac{\pi}{6})\right] \end{aligned} \tag{3.70}$$

When the inverter is operated in mode 2 and 5, the time intervals of T_0 and T_3 are represented by (3.24) and (3.25); and then the voltage changes are derived in (3.71) and (3.72).

$$\Delta v_{cap,T_0} = \frac{I_{ave,in} \cdot T_0}{C} = \frac{3\sqrt{2} I_{rms} \cdot M \cdot \cos\phi}{16C \cdot f_{sw}} \cdot \left[1 - \frac{\sqrt{3}}{2} M \cdot \sin(\omega t - \frac{\pi}{6})\right] \tag{3.71}$$

$$\Delta v_{cap,T_3} = \frac{I_{ave,in} \cdot T_3}{C} = \frac{3\sqrt{2} I_{rms} \cdot M \cdot \cos\phi}{16C \cdot f_{sw}} \cdot \left[1 - \frac{3}{2} M \cdot \sin(\omega t + \frac{\pi}{6})\right] \tag{3.72}$$

When the inverter is operated in mode 3 and 6, the time interval of T_0 and T_3 are denoted by (3.26) and (3.27); and then the voltage changes are derived in (3.73) and (3.74).

$$\Delta v_{cap,T_0} = \frac{I_{ave,in} \cdot T_0}{C} = \frac{3\sqrt{2} I_{rms} \cdot M \cdot \cos\phi}{16C \cdot f_{sw}} \cdot (1 - \frac{3}{2} M \cdot \sin\omega t) \tag{3.73}$$

$$\Delta v_{cap,T_3} = \frac{I_{ave,in} \cdot T_3}{C} = \frac{3\sqrt{2} I_{rms} \cdot M \cdot \cos\phi}{16C \cdot f_{sw}} \cdot (1 - \frac{\sqrt{3}}{2} M \cdot \cos\omega t) \tag{3.74}$$

Theoretically, $\Delta v_{cap,total}$ within T_s should be equal to zero and that is proved by substituting the voltage changes acquired above into (3.75).

$$\Delta v_{cap,total} = 2\Big(\Delta v_{cap,T_0} + \Delta v_{cap,T_1} + \Delta v_{cap,T_2} + \Delta v_{cap,T_3}\Big) = 0 \tag{3.75}$$

3.3.2 DC-link voltage ripple considering anti-parallel diode reverse recovery

Combining (3.50) and (3.61), the voltage changes within T_s are derived in (3.76) by taking the diode reverse recovery into account.

$$\Delta v_{cap} = \frac{1}{C} \cdot \begin{cases} \int_{t_0}^{t_1} I_{ave,in} \cdot \mathrm{d}t & , t_0 < t < t_1 \\ \int_{t_1}^{t_1+t_a} \left(I_{ave,in} - i_a - \frac{I_{rr}}{t_a} \cdot (t - t_1) \right) \cdot \mathrm{d}t & , t_1 \le t < t_1 + t_a \\ \int_{t_1+t_a}^{t_1+t_{rr}} \left(I_{ave,in} - i_a - \frac{I_{rr}}{t_b} \cdot (t_1 + t_{rr} - t) \right) \cdot \mathrm{d}t & , t_1 + t_a \le t < t_1 + t_{rr} \\ \int_{t_1+t_{rr}}^{t_2} (I_{ave,in} - i_a) \cdot \mathrm{d}t & , t_1 + t_{rr} \le t < t_2 \\ \int_{t_2}^{t_2+t_a} \left(I_{ave,in} + i_b - \frac{I_{rr}}{t_a} \cdot (t - t_2) \right) \cdot \mathrm{d}t & , t_2 \le t < t_2 + t_a \\ \int_{t_2+t_a}^{t_2+t_{rr}} \left(I_{ave,in} + i_b - \frac{I_{rr}}{t_b} \cdot (t_2 + t_{rr} - t) \right) \cdot \mathrm{d}t & , t_2 + t_a \le t < t_2 + t_{rr} \\ \int_{t_2+t_{rr}}^{t_3} (I_{ave,in} + i_b) \cdot \mathrm{d}t & , t_2 + t_{rr} \le t < t_3 \\ 2 \int_{t_3}^{t_4} I_{ave,in} \cdot \mathrm{d}t & , t_3 < t < t_4 \\ \int_{t_4}^{t_4+t_a} \left(I_{ave,in} + i_b - \frac{I_{rr}}{t_a} \cdot (t - t_2) \right) \cdot \mathrm{d}t & , t_4 \le t < t_4 + t_a \\ \int_{t_4+t_a}^{t_4+t_{rr}} \left(I_{ave,in} + i_b - \frac{I_{rr}}{t_b} \cdot (t_2 + t_{rr} - t) \right) \cdot \mathrm{d}t & , t_4 + t_a \le t < t_4 + t_{rr} \\ \int_{t_4+t_{rr}}^{t_5} (I_{ave,in} + i_b) \cdot \mathrm{d}t & , t_4 + t_{rr} \le t < t_5 \\ \int_{t_5}^{t_6} (I_{ave,in} - i_a) \cdot \mathrm{d}t & , t_5 \le t < t_6 \\ \int_{t_6}^{t_7} I_{ave,in} \cdot \mathrm{d}t & , t_6 < t < t_7 \end{cases} \tag{3.76}$$

Furthermore, the DC-link capacitor voltage changes are solved by (3.77).

$$\Delta v_c = \frac{1}{C} \cdot \begin{cases} I_{ave,in} \cdot T_0 & , t_0 < t < t_1 \\ (I_{ave,in} - i_a) \cdot T_1 - \frac{1}{2} I_{rr} \cdot t_{rr} & , t_1 < t < t_2 \\ (I_{ave,in} + i_b) \cdot T_2 - \frac{1}{2} I_{rr} \cdot t_{rr} & , t_2 < t < t_3 \\ 2 \cdot I_{ave,in} \cdot T_3 & , t_3 < t < t_4 \\ (I_{ave,in} + i_b) \cdot T_2 - \frac{1}{2} I_{rr} \cdot t_{rr} & , t_4 < t < t_5 \\ (I_{ave,in} - i_a) \cdot T_1 & , t_5 < t < t_6 \\ I_{ave,in} \cdot T_0 & , t_6 < t < t_7 \end{cases} \tag{3.77}$$

In (3.77), it is obvious that the voltage changes in T_0 and T_3 are not influenced by the diode reverse recovery, and thus the voltage changes within T_1 and T_2 are introduced and shown in (3.78) and (3.79). The last items in (3.78) and (3.79) are caused by the diode reverse recovery, while rest of the parts in both equations are same as the expressions obtained in (3.64) and (3.65).

$$\begin{aligned} \Delta v_{cap,T_1} &= \frac{(I_{ave,in} - i_a) \cdot T_1}{C} - \frac{I_{rr} \cdot t_{rr}}{2C} \\ &= \frac{\sqrt{6} I_{rms} \cdot M}{4C \cdot f_{sw}} \cdot \sin\left(\omega t - \frac{\pi}{6}\right) \cdot \left[\frac{3M}{4} \cos\phi - \sin\left(\omega t - \phi\right)\right] - \frac{I_{rr} \cdot t_{rr}}{2C} \end{aligned} \tag{3.78}$$

$$\begin{aligned} \Delta v_{cap,T_2} &= \frac{(I_{ave,in} + i_b) \cdot T_2}{C} - \frac{I_{rr} \cdot t_{rr}}{2C} \\ &= \frac{\sqrt{6} I_{rms} \cdot M}{4C \cdot f_{sw}} \cdot \cos\omega t \cdot \left[\frac{3M}{4} \cos\phi + \sin\left(\omega t - \phi - \frac{2\pi}{3}\right)\right] - \frac{I_{rr} \cdot t_{rr}}{2C} \end{aligned} \tag{3.79}$$

The value of $\frac{I_{rr} \cdot t_{rr}}{2C}$ is less than 1% of the total voltage change, thus the impact of diode reverse recovery on the DC-link voltage ripple is negligible.

As it is mentioned above, the theoretical total voltage change during T_s should be zero. Nevertheless, a tiny drop in DC-link capacitor voltage is derived by (3.80) with the consideration of the diode reverse recovery. Although the calculated voltage drop appears in the final expression of the total voltage change, the value of this voltage drop is usually much smaller than the voltage changes and it can be compensated by the DC source. Therefore, the tiny voltage drop caused by the diode reverse recovery is neglected in the analysis.

$$\begin{aligned} \Delta v_{cap,total} &= 2\Big(\Delta v_{cap,T_0} + \Delta v_{cap,T_1} + \Delta v_{cap,T_2} + \Delta v_{cap,T_3}\Big) - \frac{3I_{rr} \cdot t_{rr}}{2C} \\ &= 0 - \frac{3I_{rr} \cdot t_{rr}}{2C} = -\frac{3I_{rr} \cdot t_{rr}}{2C} \end{aligned} \tag{3.80}$$

According to the discussion above, the influence of the inverter anti-parallel diode reverse recovery is negligible in DC-link voltage ripple calculations.

3.4 DC-Link Capacitor Selection

Generally, the DC-link capacitor is selected depending on the requirements of inverter systems; and there are two important parameters that should be evaluated. In order to prevent overheat, the maximum allowable continuous current of the DC-link capacitor must be larger than the calculated RMS value of the DC-link current ripple. Furthermore, based on the requirement of voltage ripple, which is commonly 5% to 10% of the DC-link voltage (Rashid, 2011), the DC-link capacitance demanded

by the inverter are defined by solving (3.63) and (3.77). Additionally, any component connected in the circuit will contribute to the total circuit stray inductance and a large value of this parasitic inductance can lead to high switching loss and EMI (Sivkov *et al.*, 2015). Thus, a DC-link capacitor with the relatively low equivalent series inductance is preferred.

3.5 Summary

A brief introduction of three PWM techniques, SPWM, THI, and SVPWM, is presented. Methods for DC-link current and voltage analysis are demonstrated based upon these three PWM techniques. The original method from prior studies, in which the inverter input current is assumed ideal, is described. According to the existing method, the inverter DC-link current as well as ripple components in the current and voltage are only influenced by the inverter output current, power factor, and modulation index.

In fact, the inverter anti-parallel diode reverse recovery current and time also contribute to the DC-link current and voltage and their ripple components. Therefore, method for the DC-link current and voltage analysis considering the diode reverse recovery is developed. The occurrence of the diode reverse recovery during T_s is analyzed. Both simulation and experimental results are presented to validate the analysis. After that, in order to provide a comprehensive analysis in the derivation of the relationship between the diode reverse recovery and the DC-link current and voltage ripple, the current flow in inverter switching transients and the occurrence of the diode reverse recovery during T_s are discussed. Then, the proposed method is developed by integrating the diode reverse recovery transients in the inverter input

current analysis. In addition, the ripple components in DC-link current and voltage are also estimated by the proposed method. The proposed method reveals that the inverter DC-link current and its ripple component are also decided by the anti-parallel diode reverse recovery and inverter switching frequency. In contrast, the influence of diode reverse recovery in the DC-link voltage ripple is negligible.

Furthermore, depending on the expressions of the DC-link current ripple RMS value, there is no difference in the calculations under different PWM techniques. Nevertheless, the calculations for the DC-link voltage ripple vary in different PWM schemes because of the injection signals appearing in the equations.

Chapter 4

Bus Bar Design

In the inverter, a bus bar is designed instead of utilizing cables to connect each component in the inverter circuit; in this case, the inverter assembly is simplified. Meanwhile, using the laminated structure, the low parasitic impedance of the bus bar can be achieved. The shape of a bus bar should be designed based on the packages and locations of the selected semiconductor devices and DC-link capacitors. Furthermore, the numbers of capacitors and semiconductor modules also influence the bus bar design, because the locations of the connection points and installation holes affect the current distribution on the bus bar and the values of parasitic parameters. To acquire the balanced current distribution, the bus bar impedance in each current path from the inverter DC input to the output should be kept close to each other. Therefore, the installation holes should be uniformly located on the bus bar. Generally, simulations are utilized to predict the performance of the designed bus bar before manufacturing; and the finite element method is usually used in analysis. Then, the current density and distribution on the bus bar can be evaluated; additionally, the parasitic parameters of the bus bar can also be estimated by simulations.

In this chapter, the methods for simulation analysis are discussed in Section 4.1. Then, in Section 4.2, the bar bus current distribution is discussed and the bus bar design is presented depending on the inverter system. Although the parasitic parameters can be obtained by simulations, the analytical methods for bus bar parasitic parameter calculations are also introduced in Section 4.3 to have an insight into the correlation between the bus bar shape and those parameters. Finally, a summary is addressed in Section 4.4.

4.1 DC/AC Analysis of Bus Bar

As it is mentioned previously in Section 3.3, the inverter DC bus current can be presented by the sum of a DC and an AC current component. The DC current component is the average current calculated by (3.55), while the AC current component is the ripple current that is also the DC-link capacitor current, whose RMS value is derived in (3.57). As a result, the current distribution of the DC component and AC component are evaluated in simulations by DC and AC analysis respectively.

For DC analysis, DC current distribution from the DC input tabs to the switching device terminals are evaluated. A DC current is injected from the DC input tabs into the 3D model of the bus bar, and the equivalent circuit is shown in Figure 4.1, where R_n, R_p, L_n, and L_p are resistance and inductance of the negative and positive plates. In the 3D model, the positive and negative conductors of the bus bar are shorted together at the terminals that are designed for the semiconductor device connections (Zare and Ledwich, 2002; Guichon *et al.*, 2006). Then the AC analysis is utilized to examine the bus bar AC current distribution between DC-link capacitors and semiconductors; in addition, the current sharing among DC-link capacitors can also

be evaluated. The equivalent circuit of the AC analysis is shown in Figure 4.2. It can be seen that an AC excitation current is injected into the bus bar; at the same time, DC-link capacitor terminals on bus bar positive and negative plate are shorted.

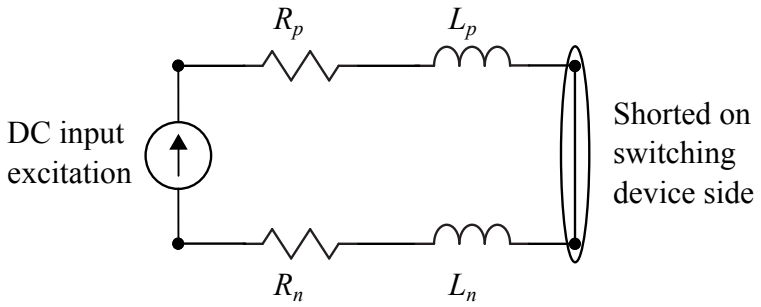


Figure 4.1: Equivalent circuit for the DC analysis.

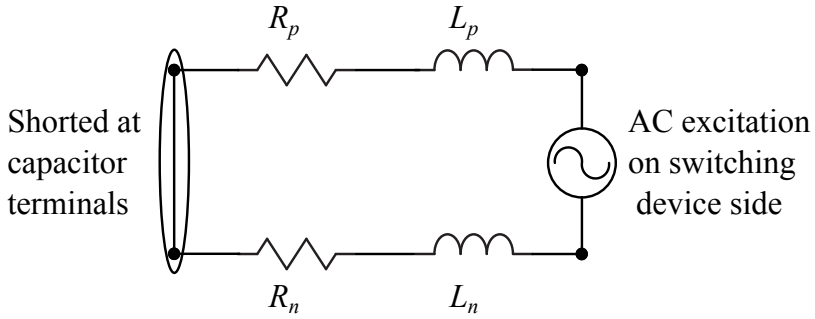


Figure 4.2: Equivalent circuit for the AC analysis.

By implementing DC- and AC analysis, the parasitic parameters of the bus bar including equivalent resistance, stray inductance and capacitance are also predicted.

4.2 Current Density and Distribution

An example of the laminated bus bar structure is shown in Figure 4.3, in which two conductors are coupled together with a layer of the insulation materials inserted between them. In Figure 4.3, t, w, l, and d are conductor thickness, width, length

along the current direction and the distance between two conductors (the thickness of insulation layer), respectively. The width and length of the conductor are usually determined by the packages and locations of the inverter main components, while the thicknesses of the conductor and insulation layer are designed depending on the current and voltage levels of the inverter system. Generally speaking, there is no upper limits of the conductor and insulation layer thicknesses; however, there are lower limits. To sustain the operating DC-link voltage, the insulation thickness should be larger than a minimum value. The dielectric strength of the material is not constant under different insulation thickness. As it is introduced in (DuPont, 2008), the dielectric strength of the material Nomex type 410 from Dupont is 18kV/mm and 33kV/mm when thicknesses of the materials are 0.05mm and 0.38mm respectively. On the other hand, the lower limit of conductor thickness should be satisfied. With the suggestions from manufacturer, the thicknesses of the conductors and insulation layer in a bus bar conducting 600A and sustaining 600V are 2.36mm and 0.18mm, respectively.

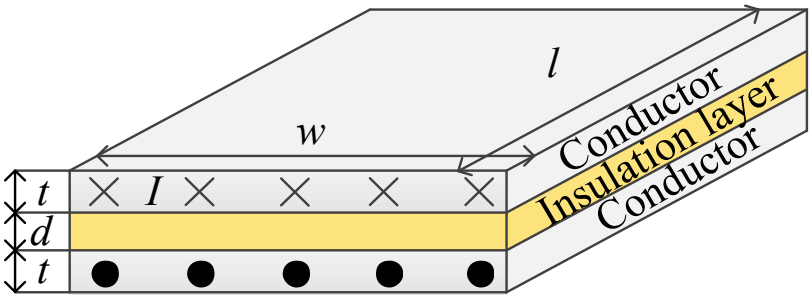


Figure 4.3: An example of bus bar structure.

From Figure 4.3, the cross-sectional area in the current direction can be calculated by the conductor thickness and width in (4.1). Then the current density in the conductors is defined as the amount of current flowing through this cross-section

divided by the area, it is shown in (4.2) (Vanderlinde, 2004).

$$A = t \cdot w \tag{4.1}$$

$$J = \frac{I}{A} \tag{4.2}$$

The current density in each conductor should meet the 5A/mm^2 requirement (Allocco, 1997). In this case, the overheat on entire bus bar or in some of its local areas can be prevented. Furthermore, to guarantee the lifetime of each capacitor and even current sharing at the inverter output terminals, the current distribution should be balanced (Pasterczyk *et al.*, 2005). Therefore, the analysis of current density and distribution is indispensable. Additionally, the current excitations should be defined by the estimated DC-link current values. The average inverter input current is utilized

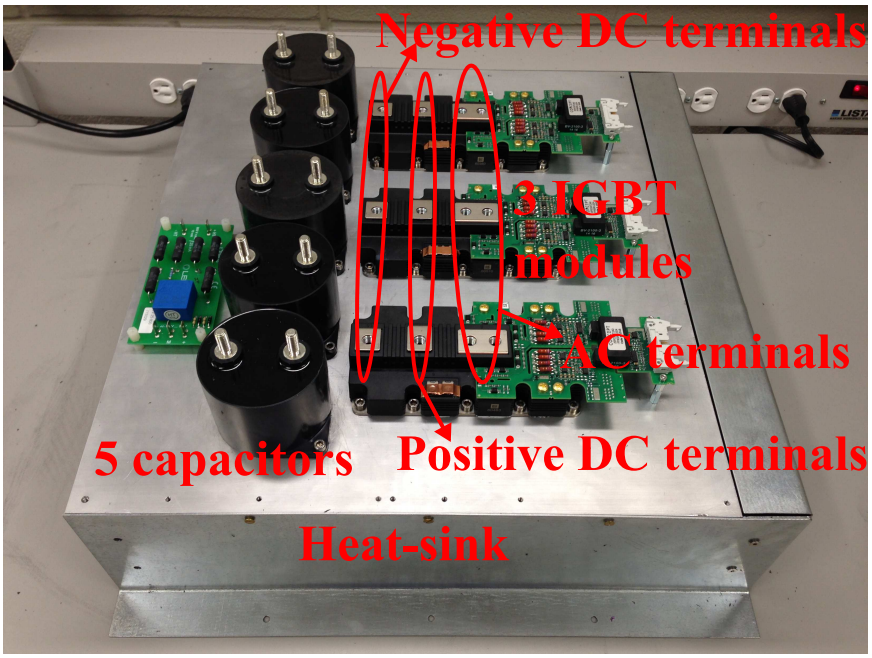


Figure 4.4: DC-link capacitors and IGBT modules in the inverter system.

as the excitation in DC analysis and the RMS DC-link ripple current is utilized as the excitation in AC analysis; since in the DC-link, the average input current is assumed as the DC component current and the ripple current is considered as the AC component current. Main components in the inverter system are five DC-link capacitors and three IGBT modules, and they are located on the top of a heat sink that is shown in Figure 4.4. According to the component locations and the height difference between capacitors and IGBT modules, the bus bar is designed and analyzed.

4.2.1 Initial design

As it is shown by Figure 4.4, the bus bar apparently cannot be simply designed with the flat shape because of the height difference between the DC-link capacitors and IGBT modules. Thus, a bus bar is designed and shown in Figure 4.5.

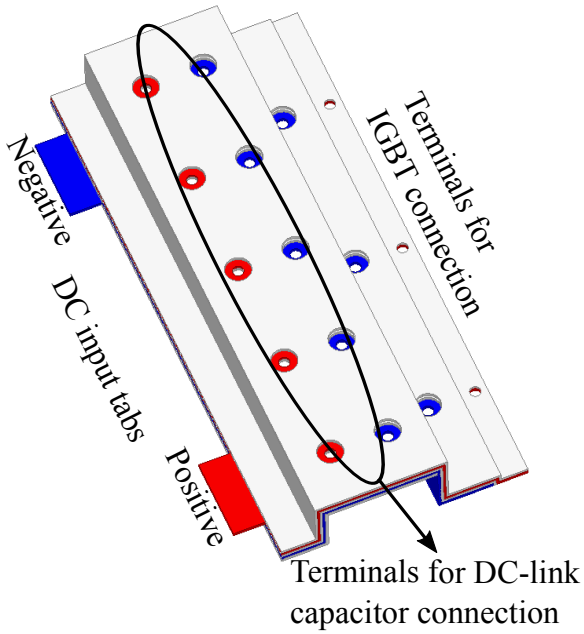


Figure 4.5: Initial design of the bus bar.

It can be seen that five DC-link capacitors and three IGBT phase-leg modules are utilized and there is one set of the DC input tabs. the DC and AC current distributions are evaluated by implementing simulations in ANASYS MAXWELL and Q3D based on the DC and AC analysis described above. For the DC analysis simulation, the DC excitation currents are injected into the 3D model through all the DC input tabs on the positive plate; and all the DC input tabs on the negative plate are set as sinks. At the same time, the positive and negative plates are shorted at the IGBT connection terminals. For the AC analysis simulation, the positive and negative plates are shorted at both DC-link capacitor and IGBT module connection terminals. Three AC excitation currents are injected into the 3D model through three sets of IGBT connection terminals. The short circuit connections and excitation current injections are shown by Figure 4.6.

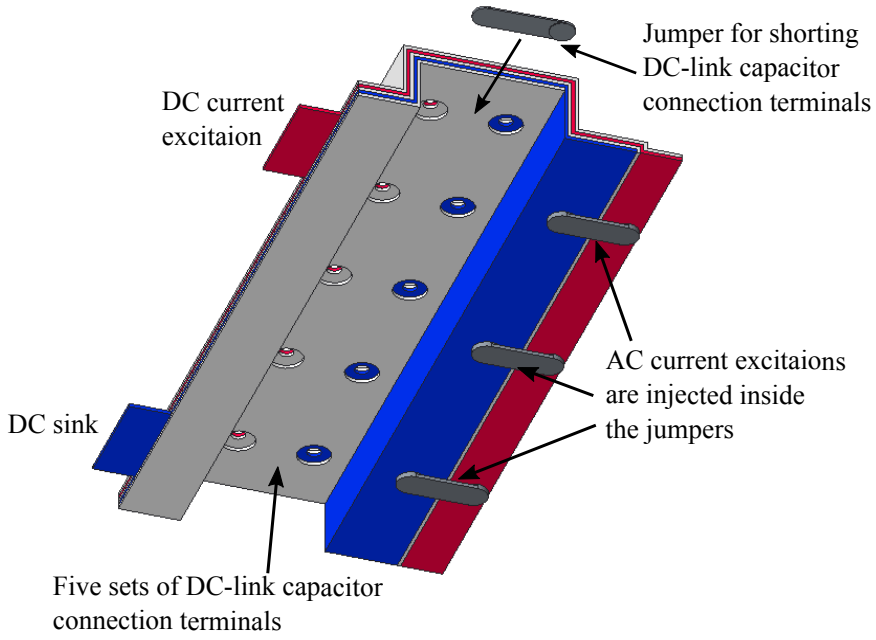


Figure 4.6: Short circuit connections and current injections in the bus bar 3D model simulations.

The simulation results from the DC analysis are obtained in Figure 4.7. According to the results in Figure 4.7, the current density of both positive and negative conductors are higher than the limitation around the DC input tabs; and this issue can be solved by increasing the width of those input tabs. The DC current distribution is also presented by the simulation results and it is imbalanced when only one set of the DC input tabs are designed for the bus bar.

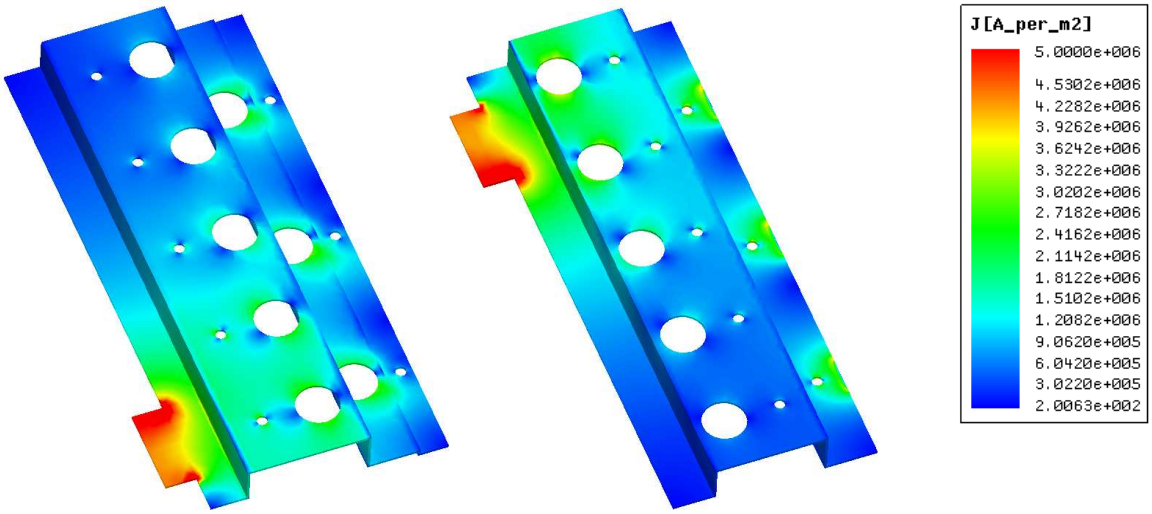


Figure 4.7: DC analysis for the inverter DC-link current density and distribution with one set of the DC input tabs (the positive plate is shown on the left and the negative plate is shown on the right).

The simulation results from the DC analysis indicate that when the DC input tabs are designed as one set, the current distribution on the bus bar is imbalanced. In contrast, the AC analysis is also implemented and the results are presented by Figure 4.8. From the those results obtained by the AC analysis, the AC current is distributed evenly between terminals of the DC-link capacitors and IGBT modules. That is because the AC component of the DC-link current circulates between the capacitors and IGBTs on the bus bar, and the installation holes for both capacitors

and IGBTs are distributed uniformly on the conductors. Therefore, it is rational that the AC current distribution is balanced and it is irrelevant to the numbers and locations of the DC input tabs. Furthermore, the current density derived from the AC analysis satisfies the requirement.

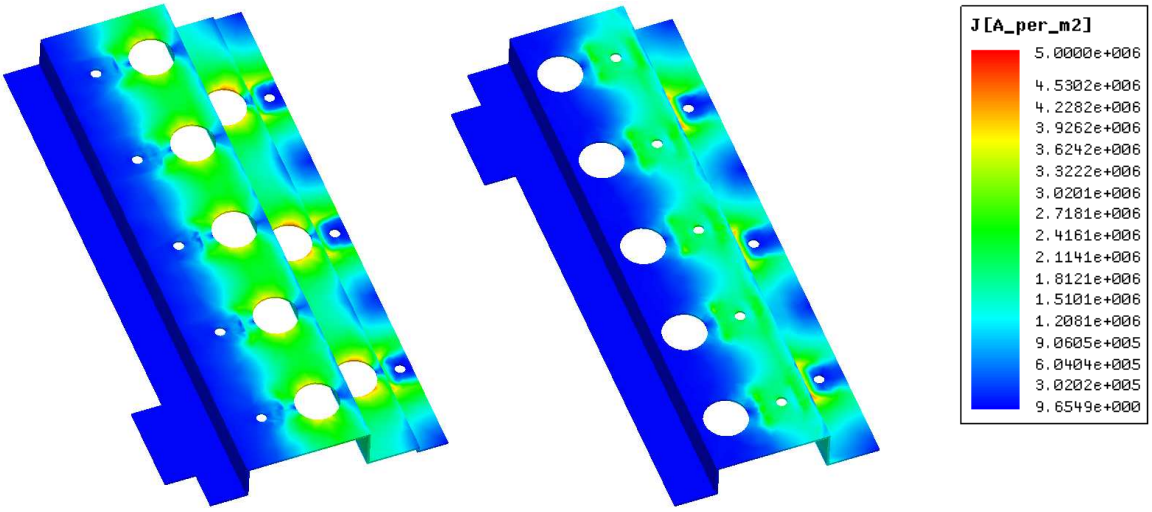


Figure 4.8: AC analysis for the inverter DC-link current density and distribution with one set of the DC input tabs (the positive plate is shown on the left and the negative plate is shown on the right).

4.2.2 Final design

Based upon the simulation results for the initial bus bar model, it can be concluded that design of the DC input tabs should be revised to improve the DC current density and distribution. On the other hand, the AC current density and distribution satisfy the requirements; as a result, design of the installation holes for the DC-link capacitors and IGBT modules could be preserved. Augmenting the input tabs could be a straightforward solution to achieving the balanced DC current distribution; however, considering the complexity of the design, the relatively small number of the DC input

tabs is preferred. Instead of utilizing one set of DC input tabs, the design is modified such that three sets of the tabs are uniformly located along the edge of the bus bar on the input side. The revised model is shown in Figure 4.9.

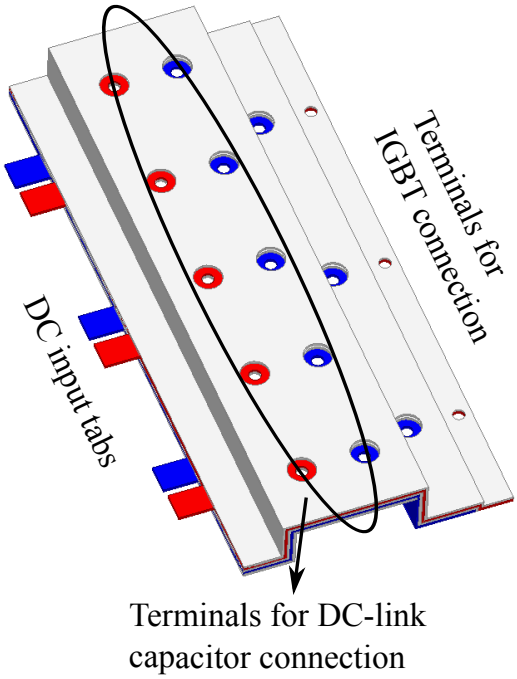


Figure 4.9: Final design of the bus bar.

The simulation results from the DC analysis are presented by Figure 4.10. The DC current distribution is improved when three sets of the DC input tabs are used. The DC current is distributed evenly on both positive conductor and negative conductor. Furthermore, by increasing the total width of the DC input tabs, the cross-sectional area on the input side of the bus bar is enlarged; thus, the DC current density on the input tabs is also improved.

The simulation results of the AC current density and distribution that are obtained from the AC analysis are shown in 4.11, in which the results acquired with three sets of the DC input tabs are similar to those obtained with one set of the input tabs.

Therefore, it is further manifested that the AC current distribution is independent of the numbers and locations of the DC input tabs.

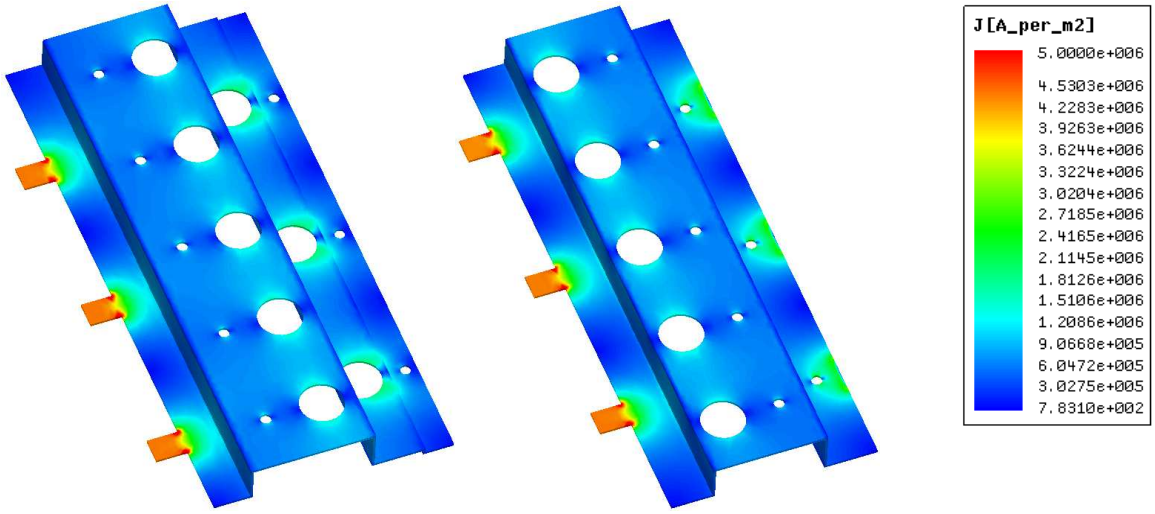


Figure 4.10: DC analysis for the inverter DC-link current density and distribution with three sets of the DC input tabs (the positive plate is shown on the left and the negative plate is shown on the right).

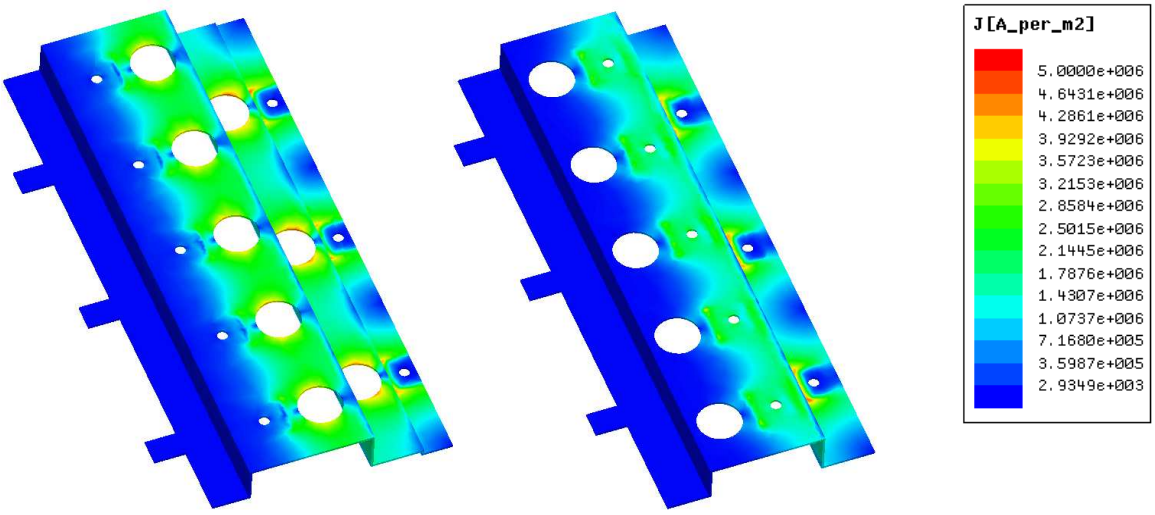


Figure 4.11: AC analysis for the inverter DC-link current density and distribution with three sets of the DC input tabs (the positive plate is shown on the left and the negative plate is shown on the right).

According to the simulation results shown in Figures 4.7, 4.8, 4.10, and 4.11, the DC current distribution is improved by locating three sets of the DC input tabs on the bus bar and the AC current distribution in the preliminary design is similar to that in the revised design. Thus, it can be concluded that the DC current distribution is determined by the locations of the input tabs, while the AC current distribution is defined by the locations of the capacitors and switching devices. After that, the parasitic parameters are also evaluated in the following sections. Finally, the designed bus bar is manufactured and assembled in the inverter system, as shown in Figure 4.12.

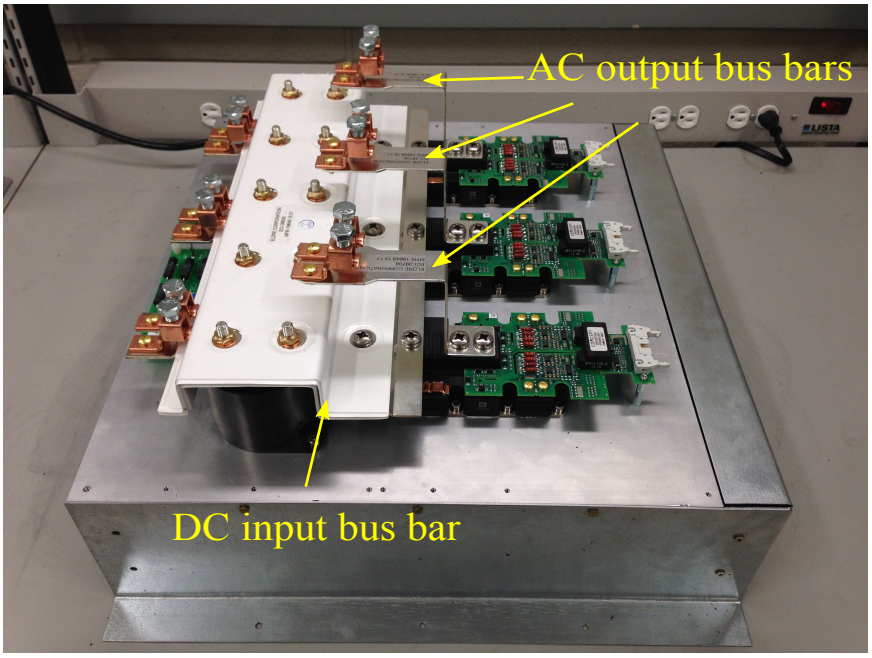


Figure 4.12: DC-link capacitors and IGBT modules connected in the inverter system by the designed bus bar.

4.3 Parasitic Parameters

The parasitic parameters of the bus bar include resistance, stray inductance and capacitance. Although the evaluation of these parameters can be obtained by the simulations, theoretical analysis is still necessary for understanding the rules of the bus bar design.

4.3.1 Resistance

Generally, the bus bar resistance is determined by the materials and shape of the conductors. When a current flows through the bus bar, the power loss is mainly generated and affected by the resistances. Thus, low bus bar resistance is preferred. According to the example of a bus bar structure in Figure 4.3, when a DC current is flowing from one side to the other side in a conductor, this DC current evenly spreads out in the conductor. In other words, the current flows through the entire cross-section and the conductor. Then, the resistance of this conductor under the DC current can be represented by (4.3) (Caponet *et al.*, 2002),

$$R_{dc} = \rho \cdot \frac{2l}{w \cdot t} = \rho \cdot \frac{2l}{A} \tag{4.3}$$

where ρ [Ω·m] is the resistivity of the conductor. Copper is commonly used as the conductor because of its low resistivity, which is $1.72 \times 10^{-8}\Omega \cdot \mathrm{m}$ under the temperature of 20°C (Chan, 2000). Usually, the resistivity varies approximately linearly within a limited temperature range and the value under 20°C is set as the reference temperature. Then the copper resistivity can be finally expressed by (4.4), where

T and β are temperature in degrees Celsius and the temperature coefficient of the copper resistivity that is $3.9 \times 10^{-3°}\mathrm{C}^{-1}$, respectively (Serway *et al.*, 2014).

$$\rho = \rho_{20°\mathrm{C}} \cdot \Big[1 + \beta \cdot (T - 20)\Big] \tag{4.4}$$

From the division in (4.3), it can be found that the denominator is the conductor cross-sectional area while the numerator contains the conductor length along the current direction. In the bus bar design, the length and width of the conductor are somehow decided by the packages and locations of the inverter main components, capacitors and semiconductors. Thus, the conductor thickness is the key factor that influence the bus bar resistance. The larger the thickness is, the lower conductor resistance can be obtained.

When an AC current flows through the bus bar, the AC current has a tendency to concentrate near the area that is close to the conductor surface, as it is shown in Figure 4.13. Furthermore, as the AC current frequency increases, thickness of the AC current layer near the conductor surface reduces. If the current frequency is as high as the level of mega hertz, thickness of the AC current layer in the copper conductor is very thin at 0.067mm (Popovic and Popovic, 2012). This phenomenon is named as skin effect; and the current layer thickness is the skin depth δ that can be found in Figure 4.13. According to (Hayt and Buck, 2012; McLyman, 2004), the skin depth is expressed by (4.5), where μ and f are permeability ($\mu = \mu_0 \cdot \mu_r$) and current frequency. For the copper conductor, the relative permeability μ_r is close to 1; thus, in the calculation the value of μ is assumed same as the permeability of free space μ_0, which is equal to $4\pi \times 10^{-7}$H/m (Salam, 2014).

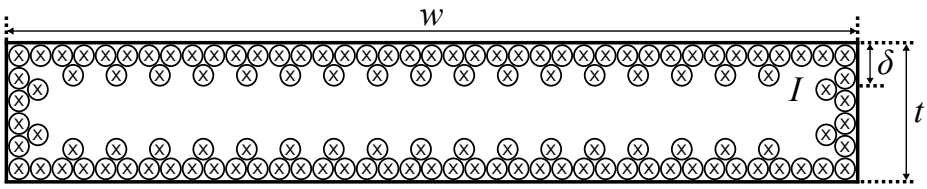


Figure 4.13: AC current flows through the cross-section in a conductor, when the current direction points into the conductor.

$$\delta = \sqrt{\frac{\rho}{\pi \cdot f \cdot \mu}} \tag{4.5}$$

The AC current is not evenly distributed in the conductor, thus the calculation for the conductor resistance is different from that under the condition of DC current. When the AC current flows through the conductor, 85% of the current is distributed in the layer that its thickness is equal to the skin depth. If the thickness of the conductor is much larger than the skin depth, the current within the layer that has a thickness same as the skin depth passes through the resistance that is considered equivalent to the resistance of the entire conductor (Chapman and Norris, 2014). Then the conductor resistance under AC conducting current is given by (4.6) (Caponet *et al.*, 2002). According to Figure 4.13 and (4.6), it can be seen that the skin effect leads to the reduction of the cross-sectional area. Consequently, the conductor resistance increases. Besides, the conductor resistance under AC current varies with the conducting current frequency because of the skin depth contained in (4.6). With the increase in current frequency, the skin depth decreases and the conductor resistance grows.

$$R_{ac} = \rho \cdot \frac{4l}{w \cdot \delta} \tag{4.6}$$

In summary, the conductor resistance obtained under AC current is larger than that under pure DC current; and under AC conducting current, the conductor resistance is influenced by the skin depth other than the conductor thickness. In this case, the increasing thickness of the conductor does not necessarily reduce the resistance any more (Caponet *et al.*, 2002; Zhu *et al.*, 2006; Wang and Chen, 2009). As it is mentioned, as the frequency rises, the current concentrates near the surface in the conductor and the resistance as well as the conductor ohmic loss grow, which is presented by the simulation results in Table 4.1.

Table 4.1: Bus bar resistance and ohmic losses obtained from the simulations

Current frequency	Resistance	Bus bar power loss		
		Negative plate	Positive plate	Total
0Hz	0.158[mΩ]	1.41 [W]	1.53 [W]	2.94 [W]
10kHz	0.219[mΩ]	1.49 [W]	1.42 [W]	2.91 [W]
20kHz	0.251[mΩ]	1.87 [W]	1.77 [W]	3.64 [W]
30kHz	0.270[mΩ]	2.07 [W]	1.96 [W]	4.03 [W]
40kHz	0.284[mΩ]	2.22 [W]	2.14 [W]	4.36 [W]
50kHz	0.295[mΩ]	2.33 [W]	2.21 [W]	4.54 [W]
60kHz	0.304[mΩ]	2.41 [W]	2.28 [W]	4.69 [W]
70kHz	0.311[mΩ]	2.47 [W]	2.35 [W]	4.82 [W]
80kHz	0.317[mΩ]	2.54 [W]	2.41 [W]	4.95 [W]
90kHz	0.322[mΩ]	2.57 [W]	2.44 [W]	5.01 [W]
100kHz	0.327[mΩ]	2.62 [W]	2.48 [W]	5.10 [W]

According to the simulation results in Table 4.1, the bus bar resistance under different frequency is very small that is even less that 1mΩ. Furthermore, the total ohmic power loss of the bus bar is around 5W, which is much lower than the power

losses of the entire inverter. Thus, the conductor resistance and ohmic losses are usually neglected. Then, the equivalent impedance of the bus bar can be approximated as (4.7) (Ariga and Wada, 2012).

$$Z = \sqrt{\frac{L}{C}} \tag{4.7}$$

Based on (4.7), to some extent, designing a low impedance bus bar is to design a bus bar with low stray inductance and high stray capacitance.

4.3.2 Stray inductance and voltage spike

Stray inductance

Generally speaking, the total circuit parasitic inductance includes DC-link capacitor equivalent series inductance, semiconductor module equivalent inductance and the bus bar stray inductance. Low total parasitic inductance in the circuit is usually preferred. That is because a high voltage spike is generated by the large circuit parasitic inductance during turn-off transients of the device, which results in more voltage stress on the semiconductor. To prevent the semiconductor module being damaged, the higher rated voltage is required. Additionally, more switching power losses are obtained under higher voltage spike during turn-off transients. Furthermore, higher voltage spike also causes more EMI (Leferink, 1995). Although it is possible to select switching devices and capacitors with relatively small inductance, there is only a limited improvement in the total circuit parasitic inductance. Nevertheless, bus bar stray inductance can be reduced significantly by laminating two conductors, positive and negative plates, on the DC bus. As a result, the total inductance in

the circuit could be minimized. Then, with the predicted total parasitic inductance in the circuit, the voltage spike can be estimated. Therefore, the stray inductance analysis and evaluation are important in DC bus bar design.

Laminated bus bar structure is commonly used, flux linkages induced by the currents in two conductors cancel each other because of the opposite current directions shown in Figure 4.3. Thus, the total stray inductance of the bus bar is expressed by the self-inductances of two conductors and mutual-inductance in (4.8) (Skibinski and Divan, 1993; Deng *et al.*, 2015; Yu *et al.*, 2015). It can be found in (4.8) that the minimized total bus bar stray inductance can be achieved by maximized the mutual inductance. In other words, by maximizing the over-lap area of two conductors, low total bus bar inductance can be acquired. That is the reason why the laminated bus bar structure is preferred in the design (Ando *et al.*, 2011).

$$L_{total} = 2 \cdot (L_{self} - L_M) \tag{4.8}$$

A laminated bus bar is a collection of the conductor plates coupled by the insulation materials, as the example is given in Figure 4.3. Based on the bus bar shape shown in Figure 4.3, to minimize the DC bus loop area, the distance between two conductor plates are usually designed small that is much smaller than the thickness and width of the conductor. Then, when the AC current frequency is low, the current is assumed spreading out uniformly in the conductor; and the laminated bus bar stray inductance can be approximately calculated in (4.9) (Leferink, 1995; Allocco, 1997).

$$L_{busbar} = \frac{\mu_0 \cdot \mu_r \cdot l}{8\pi} + \frac{2\mu_0 \cdot \mu_r \cdot l}{\pi} \cdot \ln\left(1 + \frac{t}{t+w}\right) \tag{4.9}$$

If the flat conductor is designed with large width and small thickness, $t \ll w$, (4.9) can be simplified and rewritten as (4.10) (Kazimierczuk, 2009).

$$L_{busbar} = \frac{\mu_0 \cdot \mu_r \cdot l}{8\pi} + \frac{2\mu_0 \cdot \mu_r \cdot l}{\pi} \cdot \frac{t}{(t+w)} \tag{4.10}$$

According to (4.10), by shortening the bus bar length l, reducing the distance between two conductors and increasing the bus bar width, the low total stray inductance can be achieved (Qiu *et al.*, 2006; Paul, 2006).

As the current frequency rises, the current starts to tend to flow near the surface of the conductor, which is cased by the skin effect. Then the current is not distributed evenly in the conductor and the skin depth has to be taken into account in the inductance calculation, seen in (4.11) (Kazimierczuk, 2009). Higher current frequency results in smaller skin depth δ as well as lower stray inductance. When the current frequency is extremely high, current flows in a very thin layer near the conductor surface; and then, when $\delta \ll t$, the first item in (4.11) is close to zero and it is negligible.

$$L_{busbar} = \frac{\mu_0 \cdot \mu_r \cdot l}{3\pi} \cdot \frac{\delta}{t} + \frac{2\mu_0 \cdot \mu_r \cdot l}{\pi} \cdot \frac{t}{(t+w)} \tag{4.11}$$

Therefore, the value of the bus bar stray inductance could be estimated under different current frequency in the simulations. In Table 4.2, stray inductances of the designed bus bar shown in Figure 4.12 are obtained when the current frequency varies from 10kHz to 100kHz; and the simulation results prove that the bus bar stray inductance decreases as the current frequency rises.

Table 4.2: Bus bar stray inductance obtained from the simulations

Current frequency	Stray inductance [nH]
10kHz	18.336
20kHz	16.983
30kHz	16.376
40kHz	16.013
50kHz	15.765
60kHz	15.582
70kHz	15.439
80kHz	15.324
90kHz	15.228
100kHz	15.148

Voltage spike

The voltage spike is defined as the over voltage cross the semiconductor device during the turn-off transients. An experimental data plot is shown in Figure 4.14, when an IGBT is being turned off, the current through it decreases to zero and the voltage across it rises to the off-state level, DC-link voltage. As it can be seen in Figure 4.14 that the DC-link voltage is 300V and the amount of over voltage is about 100V. This over voltage is the voltage spike across the IGBT during its turn-off transient and it is caused by the parasitic inductance in the circuit loop. The data plot cannot be acquired until the inverter is built and experiments are implemented; before that, the voltage spike can be estimated with the designed bus bar by utilizing the predicted bus bar stray inductance and the total circuit parasitic inductance.

To have an insight into the voltage spike during inverter operation, the current flow in the circuit within IGBT turn-off transients is analyzed. When the inverter is

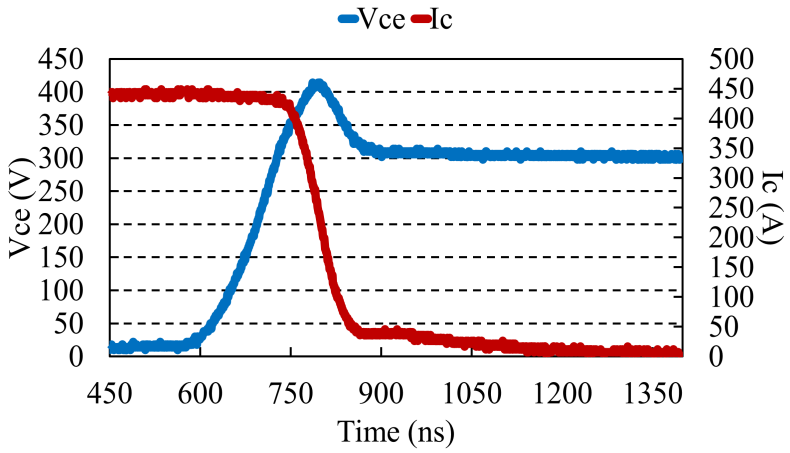


Figure 4.14: Experimental data plot of the IGBT current and voltage waveforms during the turn-off transient.

being operated in mode 1; and the phase A and C currents are positive while phase B current is negative. The equivalent circuit is shown in Figure 4.15. When phase A upper switch T_1 is being turned off, the current i_{a1} through T_1 that is in blue path falls from i_a to zero; meanwhile, the current i_{a2} presented in green path rises from zero to i_a through phase A lower diode. Consequently, there are two current changes leading to the voltage spike across T_1; and then the total voltage spike consists of several components, the voltage spike across both the DC-link capacitor series equivalent inductance and bus bar stray inductance caused by i_{a1} as well as the voltage spike across the IGBT module inductance induced by i_{a2}.

According to the equivalent circuit, with the voltage polarities shown in Figure 4.15 and using Kirchhoff's voltage law, the IGBT collector-emitter voltage V_{ce} across T_1 can be presented by (4.12), where L_C and L_{busbar} are DC-link capacitor equivalent series inductance and bus bar stray inductance, while L_1 and L_2 are IGBT module inductances in upper and lower switches (Abrishamifar *et al.*, 2010; Zhang *et al.*, 2010; Wen and Xiao, 2012; Popova *et al.*, 2012).

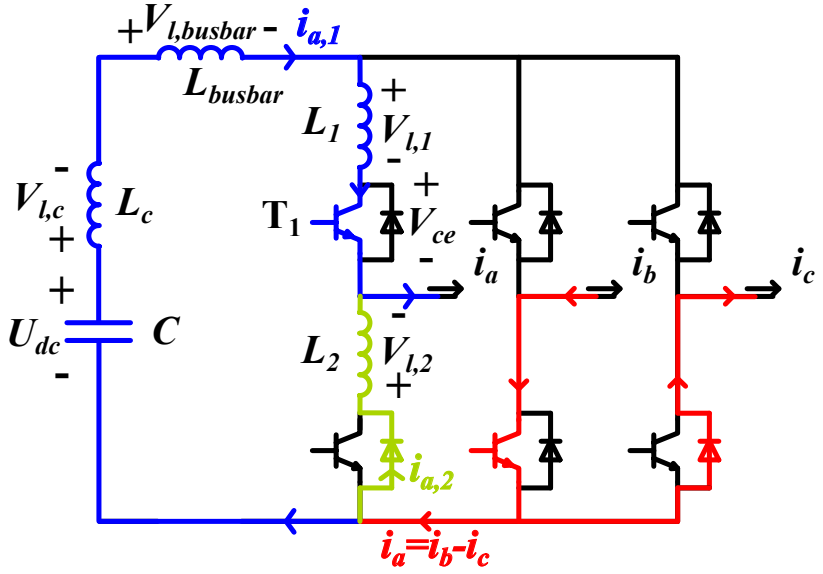


Figure 4.15: Current flow in inverter equivalent circuit during the turn-off transient of phase-A upper switch.

$$V_{ce} = U_{dc} - L_C \cdot \frac{\mathrm{d}i_{a1}}{\mathrm{d}t} - L_{lp} \cdot \frac{\mathrm{d}i_{a1}}{\mathrm{d}t} - L_1 \cdot \frac{\mathrm{d}i_{a1}}{\mathrm{d}t} + L_2 \cdot \frac{\mathrm{d}i_{a2}}{dt} - L_{ln} \cdot \frac{\mathrm{d}i_{a1}}{\mathrm{d}t} \tag{4.12}$$

In addition, within this transient time duration, i_{a1} decreases and i_{a2} increases; considering signs of the current derivatives in (4.12), absolute values can be used to present the voltage changes cross those parasitic inductances in the circuit loop. Then the total voltage across T_1 is given in (4.13) (Wen and Xiao, 2012; Hino and Wada, 2013). To prevent the semiconductor device being damaged, the result derived in (4.13) should be less than the voltage rating of the switch. Otherwise, the semiconductor modules or the DC-link capacitors with smaller equivalent series inductance should be chosen; or the design of the bus bar needs to be revised.

$$V_{ce} = U_{dc} + \left| L_C \cdot \frac{\mathrm{d}i_{a1}}{\mathrm{d}t} \right| + \left| L_{busbar} \cdot \frac{\mathrm{d}i_{a1}}{\mathrm{d}t} \right| + \left| L_1 \cdot \frac{\mathrm{d}i_{a1}}{\mathrm{d}t} \right| + \left| L_2 \cdot \frac{\mathrm{d}i_{a2}}{\mathrm{d}t} \right| \tag{4.13}$$

Table 4.3: Estimated voltage spike under 300V DC-link voltage, 400A IGBT current, and 10kHz switching frequency.

Total inductance and estimated voltage spike	Parameters and calculation results
L_c [nH]	40
No. of caps	5
Equivalent L_c [nH]	8
L_{IGBT} [nH]	18
L_{busbar} [nH]	18.336
ΔI [A]	400
Δt [ns]	150
U_{DC} [V]	300
V_{spike} [V]	118.2
V_{peak} [V]	418.2

Assume the half-bridge IGBT modules are utilized and the laminated conductors are considered as one component, (4.13) can be further simplified and finally described in the form of (4.14).

$$V_{ce} = U_{dc} + \left| L_C \cdot \frac{\mathrm{d}i_a}{\mathrm{d}t} \right| + \left| L_{busbar} \cdot \frac{\mathrm{d}i_a}{\mathrm{d}t} \right| + \left| L_{IGBT} \cdot \frac{\mathrm{d}i_a}{\mathrm{d}t} \right| \tag{4.14}$$

An example for the calculation of voltage spike across T_1 during turn-off transient is given in Table 4.3. The DC-link voltage and current through the IGBT are the inverter operating conditions, and the time interval 150ns is obtained from the experimental measurements.

4.3.3 Stray capacitance

The stray capacitance is another factor considered in bus bar design. It can benefit the system by reducing the total impedance of the bus-bar and filtering the high frequency noise. Due to the several kilo hertz or even higher switching frequency of the inverter, the electromagnetic interference (EMI) becomes an issue in power electronics. High frequency harmonics are generated in the system by fast switching of the devices. Utilizing the laminated structure of the bus bar, a capacitor between two conductor plates in the system is obtained and it helps mitigate the noise propagation (Xuesong *et al.*, 2010; Thomas *et al.*, 2009). Recall the expression of the bus bar impedance in (4.7), it is obvious that a large stray capacitance results in lower total impedance. For this reason, the stray capacitance should be designed as large as possible while the stray inductance is minimized (Caponet *et al.*, 2002; Ariga and Wada, 2012; Wang and Chen, 2009). The value of the bus bar stray capacitance is defined by the geometry of the conductors and thickness of the dielectric material layer. Based on the example of the bus bar structure in Figure 4.3, the stray capacitance is represented by (4.15), where ϵ_0 and ϵ_r are permittivity of free space and the relative permittivity of a medium material, respectively (Hino and Wada, 2013).

$$C = \varepsilon_0 \cdot \varepsilon_r \frac{\omega \cdot l}{d} \tag{4.15}$$

In (4.15), it can be concluded that in order to acquire large stray capacitance, thickness of the dielectric material layer should be designed as thin as possible (Wang and Chen, 2009; Zhu *et al.*, 2006). However, the dielectric layer thickness d also affects the insulation ability of the bus bar. The insulation requirements might not be satisfied, if the value of d is too small. Thus, attentions should be paid to both of the stray capacitance of the bus bar and the DC-link voltage requirements of the inverter system. The estimated bus bar stray capacitance at different current frequency is listed in Table 4.4. The simulation results indicate that unlike the stray inductance, the stray capacitance is slightly influenced by the current frequency.

Table 4.4: Bus bar stray capacitance obtained from the simulations

Current frequency	Stray capacitance [nF]
10kHz	1.986
20kHz	1.984
30kHz	1.981
40kHz	1.977
50kHz	1.973
60kHz	1.971
70kHz	1.968
80kHz	1.965
90kHz	1.963
100kHz	1.96

4.4 Summary

The bus bar design and analysis are discussed based on a practical inverter system. The inverter DC-link current consists of DC and AC components, then the DC and AC analysis are implemented to evaluate the current density and distribution of the bus bar. According to the simulation results, the DC current distribution on the bus bar is affected by the numbers and locations of the DC input tabs, while the AC current distribution is only influenced by the positions of installation holes for the DC-link capacitors and semiconductors. Stray parameters are determined by the conductor shape, and the correlation between the parameter values and the bus bar dimensions is illustrated. Furthermore, values of the bus bar stray parameters are also influenced by the AC current frequency. With the increase in the current frequency, the stray resistance grows and the stray inductance decreases; however, the current frequency has tiny influence in the value of stray capacitance.

Chapter 5

Inverter Design and Experimental Verification

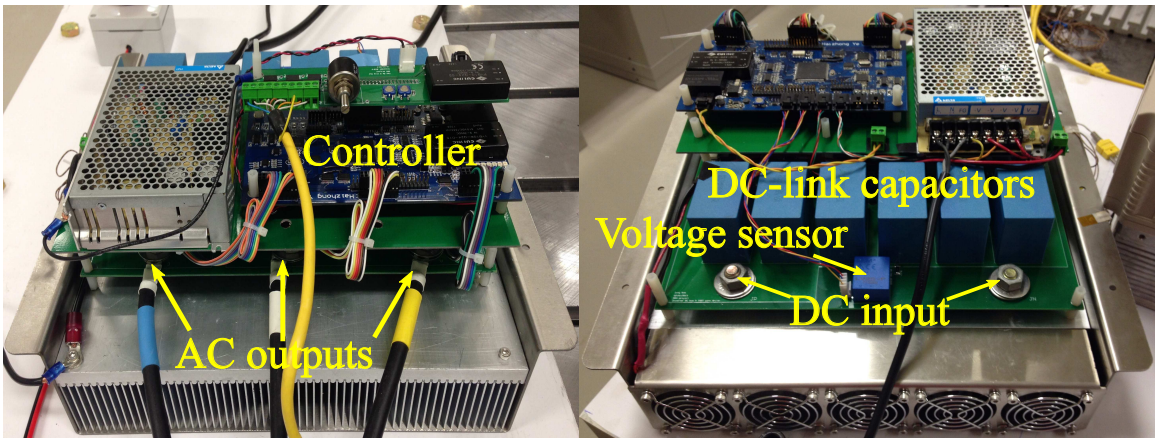
So far, the methods for inverter design are addressed analytically from different aspects, power loss evaluation, DC-link capacitor selection based on the current and voltage ripple estimation, and the bus bar design and analysis. The experimental verifications are provided in this chapter for the analysis and simulation results demonstrated previously,

- MOSFET voltage rise- and fall-time estimation during switching transients.
- Inverter power loss calculations.
- DC-link current ripple estimation with or without the consideration of the inverter anti-parallel diode reverse recovery.
- Frequency dependence of the DC-link current ripple RMS value.
- DC-link voltage ripple estimation.

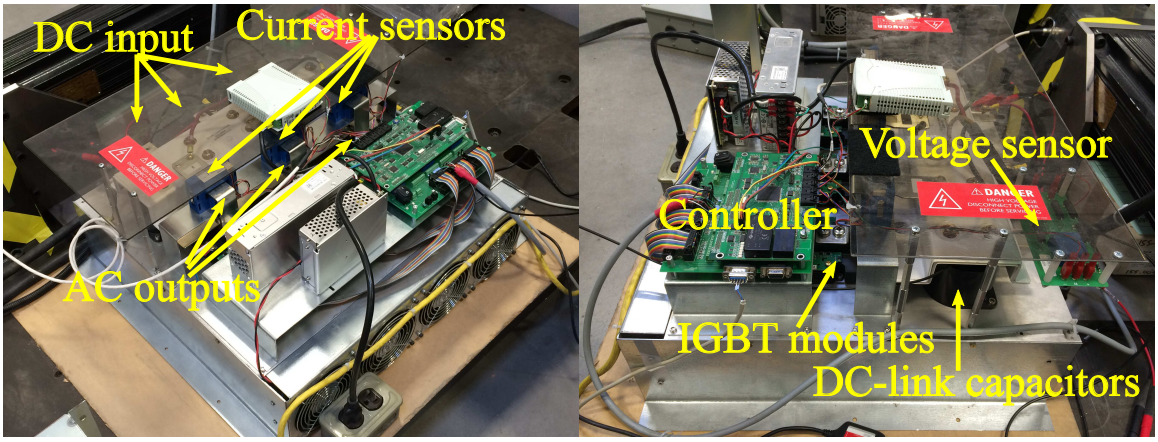
- Bus bar AC current distribution.
- Measurements for the bus bar stray inductance and capacitance.
- Estimation of the voltage spike during the switch turn-off transients.

5.1 Designed Inverter

Two inverters were designed that are shown in Figure 5.1. Inverter A is a PCB bus bar based design, and it is used to validate the power loss calculations and DC-link voltage ripple estimation. In inverter A, all the components, including DC-link capacitors, are soldered on the PCB board and the current flowing through each component cannot be measured directly; besides the DC-link current ripple needs to be obtained by measuring the capacitor current. As a result, inverter B is used for the DC-link current ripple experimental verification. Furthermore, inverter B is a copper bus bar based design, thus it is a suitable example for the bus bar analysis and experimental validation. Following the discussions in previous chapters, the solution to the design



(a) Inverter A.



(b) Inverter B.

Figure 5.1: Two designed inverters.

of copper bar based inverter is clearly illustrated; meanwhile the PCB design for the inverter A will be shown in Appendix A. Main components in the inverter A and B are given in Table 5.1.

Table 5.1: Inverter components.

Components	Inverters	
	A	B
Semiconductor switch	IGBT	IGBT
Module part NO.	FF200R06YE3	FF900R12IE4
NO. of DC-link capacitor	6	5
DC-link capacitance [μF]	75×6	220×5
Bus bar type	PCB	Copper

5.2 MOSFET Voltage Rise- and Fall-Time in Switching Transient

To validate the analytical method for MOSFET voltage rise- and fall-time estimation, the MOSFET drain-source voltage within its turn-on and turn-off transients should be captured by experiments. Double pulse test is a good choice for the current and voltage waveform measurements during the semiconductor switching transients. Thus, solution to the implementation of double pulse tests is introduced. Then the experimental results are obtained by testing a practical MOSFET module.

5.2.1 Double pulse test

The circuit topology for the double pulse test is presented in Figure 5.2, which includes a DC voltage source U_{dc}, an inductor L, and a MOSFET phase leg module. With the topology given in Figure 5.2, the upper switch T_1 in the phase leg is used as the under test device and the lower diode D_2 is used as a free-wheeling diode. Besides, the lower

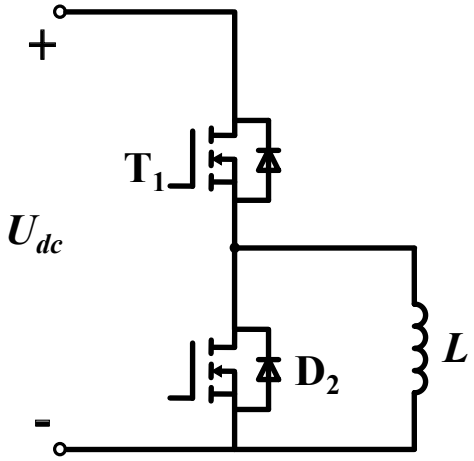


Figure 5.2: Circuit topology of double pulse test.

switch in the phase leg is kept off all the time during experiments (Castellazzia *et al.*, 2007; Xiao *et al.*, 2010; Xu *et al.*, 2012).

Controlling the under test switch T_1, current in the circuit transfers between T_1 and D_2. The switch gate signal v_{gs}, the inductor current i_L and the switch current i_{ds} are shown in Figure 5.3, in which the x-axis presents time. Δt_1 and Δt_2 indicate widths of the first and second pulses, respectively. During Δt_1 and Δt_2, the MOSFET conducts and there is a current flowing through the DC voltage source, T_1, and the inductor L. On the other hand, during the time interval between the first and the second pulse, T_1 is off and the current is only circulating between the inductor L and the free-wheeling diode D_2. In Figure 5.3, the value of I_{load} is set as the current condition, under which T_1 is supposed to be tested.

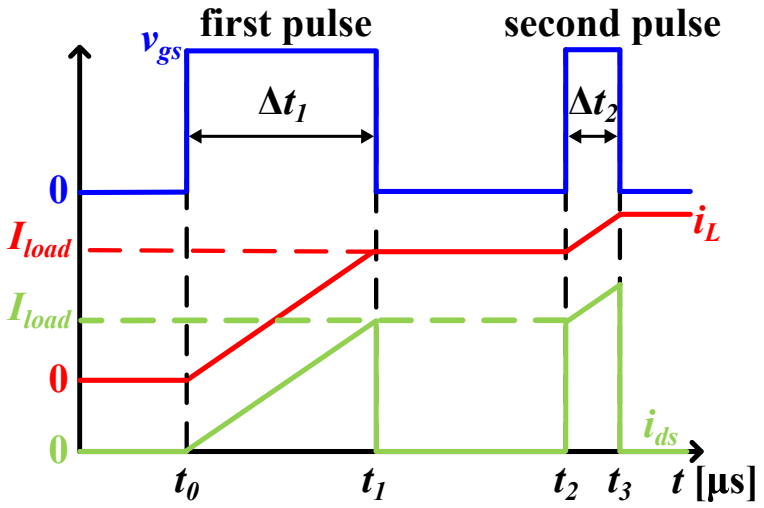


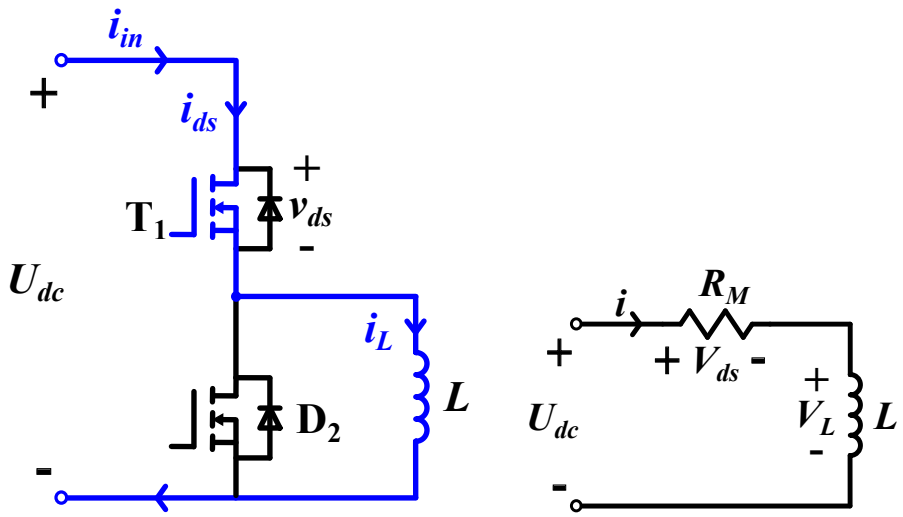
Figure 5.3: Switching scheme used in double pulse test.

Before double pulse tests are implemented, the widths of two pulses as well as the time delay between these two pulses need to be determined by taking DC-link voltage U_{dc}, the current condition I_{load}, and the inductance of L into account. Therefore, the

current flow in the circuit is analyzed depending on different time periods.

In the beginning, both T_1 and D_2 are off and there is no energy stored in the circuit; also the current in the circuit is zero.

T_1 is turned on by the first pulse when $t = t_0$, the current flow path is in blue and shown in Figure 5.4a. During Δt_1, the current in the circuit rises from zero to I_{load}. At this moment, the DC source, upper switch T_1 and inductor L are connected in series in the circuit; then the relationship among the currents through them is $i_{in} = i_{ds} = i_L$. Considering the on-state MOSFET T_1 as a resistor, the circuit can be further simplified and the equivalent circuit is presented in Figure 5.4b. According to the simplified circuit and Kirchhoff's voltage law, the correlation between the DC source and the voltages across T_1 and L is obtained in (5.1).



(a) Current path. (b) Equivalent circuit.

Figure 5.4: Current flow in double pulse test circuit during the first pulse.

$$U_{dc} = L \cdot \frac{\mathrm{d}i}{\mathrm{d}t} + R_M \cdot i \tag{5.1}$$

From the angle of circuit analysis, the current i is obtained by solving (5.1) and it is shown by the following expression in (5.2), where the time constant $\tau = \frac{L}{R_M}$ (Alexander and Sadiku, 2007).

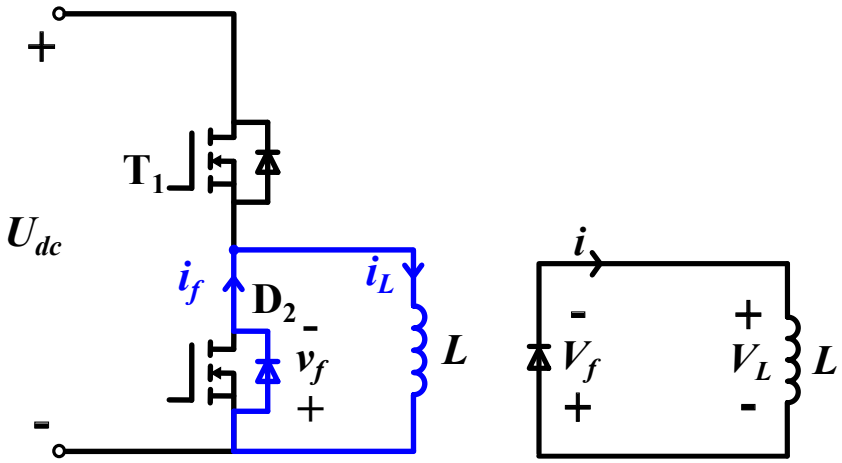
$$i(t) = \begin{cases} 0 & , t < t_0 \\ \frac{U_{dc}}{R_M} \cdot (1 - e^{-t/\tau}) & , t > t_0 \\ \frac{U_{dc}}{R_M} & , t \to \infty \end{cases} \tag{5.2}$$

The equivalent resistance of a MOSFET is very small, on the order of milliohms, and the DC-link voltage is usually several hundreds volts, then the current can be higher than ten thousand amperes in steady state. Thus, to prevent damages in the circuit, attentions should be paid to the pulse width selections in the experiment design. Generally speaking, the pulse width and the time constant are around several microseconds and milliseconds; as a result, the experiments are implemented in the transient state of the circuit. That is the reason why the current waveforms are shown as the curves in Figure 5.3. Assume at the moment when $t = t_1$ and right before T_1 is turned off, (5.1) can be approximately written in the form of (5.3); and then the width of the first pulse can be acquired. Although the time interval can be calculated approximately, to achieve the proposed current level, the pulse width can also be adjusted during the experiments if it is necessary.

$$U_{dc} = L \cdot \frac{I_{load} - 0}{\Delta t_1} + R_M \cdot I_{load} \tag{5.3}$$

Afterwards, T_1 is turned off under the testing current level and the current and voltage waveforms during the turn-off transient can be captured.

When T_1 is turned off at the end of the first pulse, there is no current flowing through the DC source and T_1. The current flow path is shown in Figure 5.5a. During this time period, the current is circulating between D_2 and L. Then the diode forward current is equal to the inductor current, $i_f = i_L$. With the assumption that the diode forward voltage is constant at a value of V_f, the circuit can be simplified in Figure 5.5b. Additionally, relationship between the voltage across D_2 and L is presented by (5.4).



(a) Current path. (b) Equivalent circuit.

Figure 5.5: Current flow in double pulse test circuit during the delay period between two pulses.

$$V_f + L \cdot \frac{\mathrm{d}i}{\mathrm{d}t} = 0 \tag{5.4}$$

Based on (5.4), the current drop during this time period Δt between two pulses is calculated, as it is shown in (5.5). The time delay is selected much smaller than Δt_1. If Δt is small enough and the amount of current drop is negligible comparing to

I_{load}, it is rational that T_1 is assumed being turned on by the second pulse at I_{load}. Therefore, the MOSFET current and voltage waveforms during the turn-on transient under I_{load} can be captured at $t = t_2$.

$$\Delta I = -\frac{V_f}{L} \cdot \Delta t \tag{5.5}$$

Ensuring that the MOSFET is fully turned off and on during the experiments, both of the widths of the time delay and the second pulse can be selected small as long as it is much longer than the MOSFET turn-off and turn-on transient time.

For the purpose of semiconductor switching power loss estimation, set-ups for the double pulse tests should be the same as those of the actual inverter system. In addition, the value of U_{dc} is usually equal to the inverter DC-link voltage; meanwhile, I_{load} is a direct current in the test and its value is set at the RMS value of the inverter output current. In this case the testing results can be obtained under the conditions that are similar to the practical inverter operating conditions. Then, based on the measured switching transient time, the MOSFET switching power loss could be estimated more accurately.

5.2.2 Experimental results

Recall the existing and proposed methods described in Section 2.1.1, t_{fu} and t_{ru} are calculated by these two methods respectively. The parameters used by the calculations in (2.19) and (2.30) are illustrated in Table 5.2. In fact, the MOSFET resistance R_M is a junction temperature-dependent parameter, it is shown by (2.1).

As the current flows through the MOSFET, power losses are generated and the junction temperature rises. As a result, the value of R_M increases when the junction temperature grows. However, it is assumed that the MOSFET junction temperature is equal to the room temperature in the calculations. Thus, the value of R_M under 25°C given by the datasheet is used in calculations.

Table 5.2: Experimental conditions for the double pulse tests.

Parameters	Values
MOSFET module	APTC60AM242G
DC-link voltage U_{dc} [V]	300
MOSFET resistance R_M [mΩ]	24
MOSFET gate-source plateau voltage $V_{plateau}$ [V]	5
MOSFET gate resistance R_g [Ω]	3
Gate driver outputs V_{drive} [V]	±15
Inductor L [mH]	0.2

The junction temperature is not affected by the power loss during very short time period. The time duration for a single experiment is on the order of microsecond (it can be seen in Table 5.3). While, the MOSFET thermal time constant is usually on the order of millisecond and there is an example given by (Yang *et al.*, 2014), in which the thermal time constant of the MOSFET is 60ms. In a word, the junction temperature cannot response that fast during the experiments. Therefore, the temperature rise from the ambient to the semiconductor module junction is assumed zero, and the MOSFET junction temperature can be considered same as the ambient temperature. Besides, depending on the design of gate drivers, output voltage of the gate driver is

positive 15V to turn on the MOSFET, and it is set at a negative value of 15V to turn off the switch. Then the values of V_{drive} and $V_{drive,n}$ used in the calculations are +15 and -15. When the MOSFET works under distinct load currents, its on-state voltage is different because of $v_{dson} = R_M \cdot i_{ds}$. As a result, the calculated t_{fu} and t_{ru} are different under various current conditions. Thus, to evaluate the calculation accuracy under different current levels, a group of t_{fu} and t_{ru} are estimated. In the validation, t_{fu} and t_{ru} are calculated under five different current levels; and corresponding to the values of I_{load}, the pulse widths are estimated and shown in Table 5.3.

Table 5.3: Pulse widths under different current conditions.

Currents I_{load} [A]	Pulse width [μs]		
	Δt_1	time delay	Δt_2
22	13.34	2	2
27	16.75	2	2
31	20.72	2	2
36	23.35	2	2
40	26.8	2	2

Experimental results are presented in the form of time steps in Table 5.4. The MOSFET voltage rise- and fall-time are described by the number of sample times measured during the turn-on and turn-off transients from the oscilloscope. The length of each sample time is 0.3125ns.

Utilizing the number of sample times, the experimental results of t_{fu} and t_{ru} are demonstrated in Table 5.5 with the estimated results by the existing and proposed methods. In Table 5.5, there are significant differences between the results derived

Table 5.4: Number of sample times spent by MOSFET voltage rise- and fall-time.

Currents I_{load} [A]	Experimental measurements	
	t_{fu}	t_{ru}
22	83	57
27	81	58
31	84	58
36	88	51
40	94	48

Table 5.5: Estimation and experimental results of MOSFET voltage rise- and fall-time (the unit is nano-second, ns).

Currents I_{load} [A]	Existing method		Proposed method		Experimental results	
	t_{fu}	t_{ru}	t_{fu}	t_{ru}	t_{fu}	t_{ru}
22	453.7	226.9	35	17.5	26	17.8
27	453.5	226.8	33.9	17	25.3	18.1
31	453.4	226.7	33	16.5	26.25	18.1
36	453.2	226.6	31.9	16	27.5	15.9
40	453	226.5	31.1	15.6	29.4	15

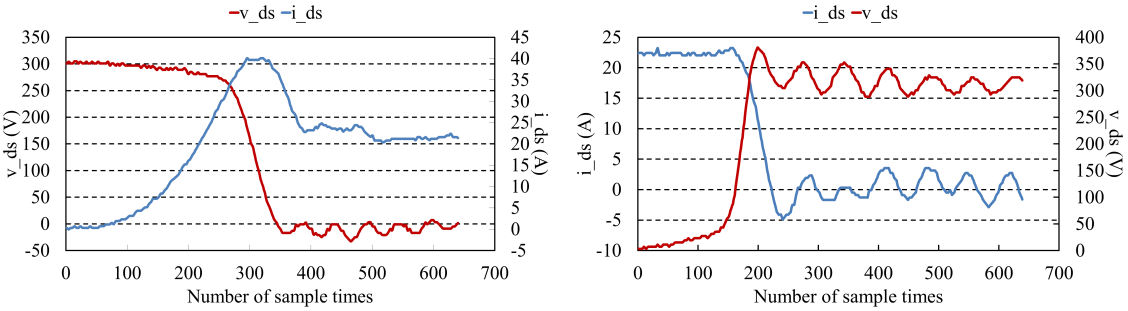
by two calculation methods; both of t_{fu} and t_{ru} calculated by the proposed method are much smaller than those obtained by the existing method. The reverse transfer capacitance, C_{rss}, changes dramatically during the switching transient; the maximum value is about 100 times higher than the minimum value during the entire period. By

using the proposed method, the entire switching period is divided into many small time intervals; and many values of C_{rss} are used in different time intervals. In fact, the average value of these reverse transfer capacitances is much smaller than the average value of the maximum and minimum capacitances. As a result, when an average value of the maximum and minimum capacitances is used by the existing method, large estimation errors are obtained.

According to the calculations, t_{fu} and t_{ru} are affected by I_{load}, as I_{load} increases, t_{fu} and t_{ru} decrease slightly. Considering the relationship among MOSFET on-state resistance R_M, on-state voltage v_{dson} and drain-source current i_{ds} (I_{load}), v_{dson} is proportional to i_{ds} if the value of R_M is constant; furthermore, the value of C_{rss} grows when v_{dson} decreases. Therefore, bigger values of t_{fu} and t_{ru} are obtained under lower i_{ds} in the calculations. That is the reason why t_{fu} and t_{ru} decrease as i_{ds} increases.

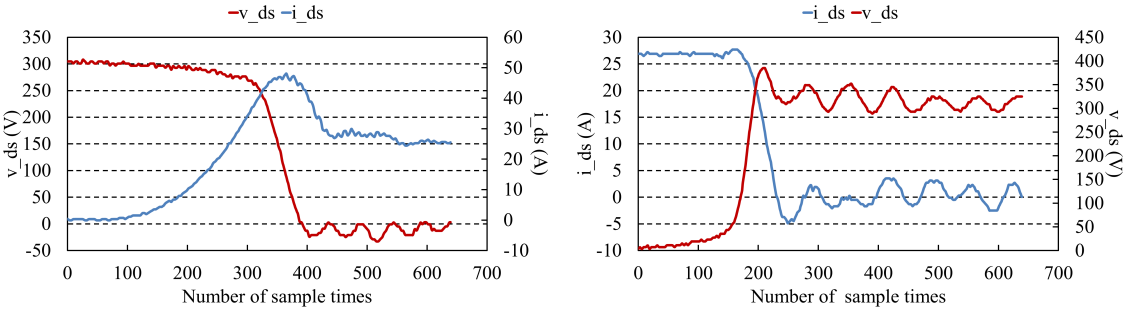
Additionally, comparing the estimated results with experimental results, t_{fu} and t_{ru} estimated by the proposed method are much closer to the experimental values than that derived by the existing method. Thus, it can be concluded that the calculation accuracy is improved significantly by the proposed method. For the proposed method, the calculated results obtained under 40A are more accurate than that acquired under other current levels. When I_{load} is 40A, the calculation error is lower than 6%. It also can be observed in Table 5.5 that the calculation for t_{ru} is more accurate than that for t_{fu}. The maximum error (35%) occurs in t_{fu} calculation under 22A. This might be because the low current flows through the MOSFET, and it leads to low on-state voltage of the MOSFET v_{dson}. According to Figure 2.8, the variation of C_{rss} is highly nonlinear when the v_{dson} is low, which may result in the estimation error during

determining the value of C_{rss}. The waveforms of i_{ds} and v_{ds} during the switching transients are shown in Figure 5.6 to Figure 5.10. There are oscillations appearing in the current waveforms, when the I_{load} is higher than 30A. This is probably caused by the parasitic inductance in the module package and gate drive circuit loop, and these oscillations might be reduced by minimizing the enclosed loop area between the gate driver output terminals and the MOSFET gate-source terminals.



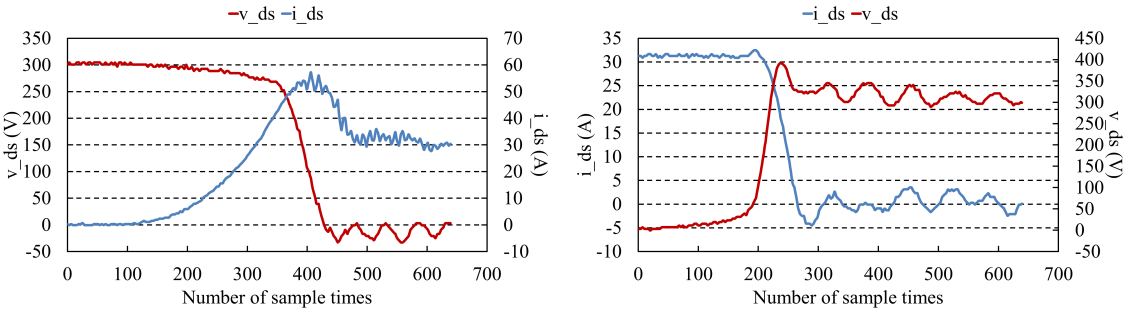
(a) Turn-on transient. (b) Turn-off transient.

Figure 5.6: MOSFET current and voltage experimental data plots, when $I_{load} = 22$A.



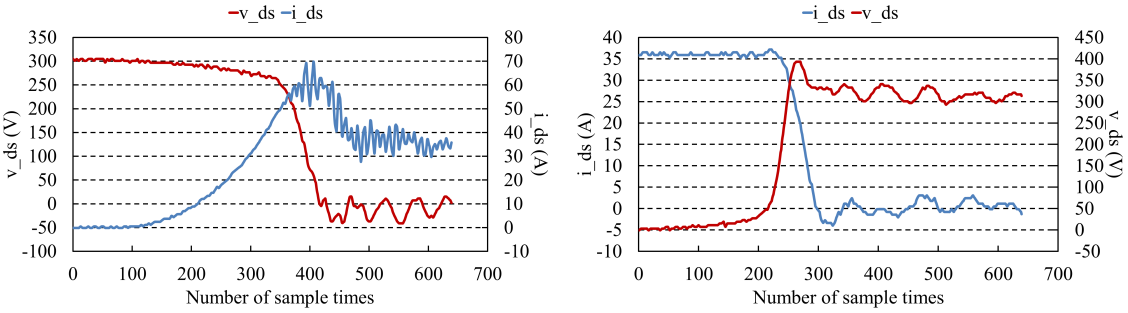
(a) Turn-on transient. (b) Turn-off transient.

Figure 5.7: MOSFET current and voltage experimental data plots, when $I_{load} = 27$A.



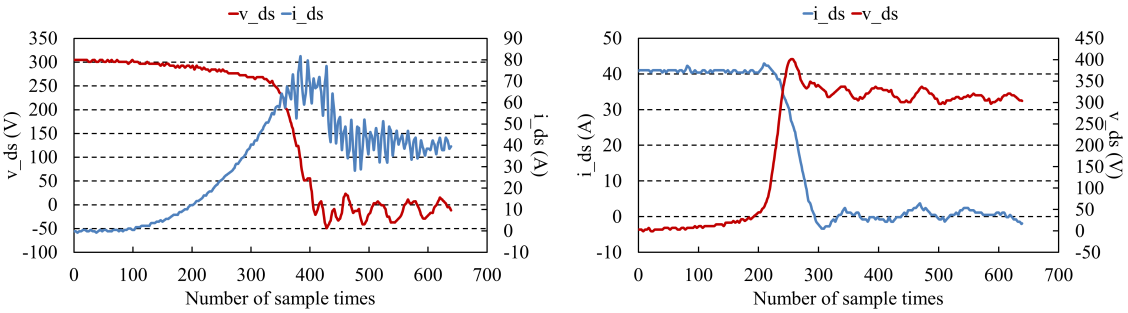
(a) Turn-on transient. (b) Turn-off transient.

Figure 5.8: MOSFET current and voltage experimental data plots, when $I_{load} = 31$A.



(a) Turn-on transient. (b) Turn-off transient.

Figure 5.9: MOSFET current and voltage experimental data plots, when $I_{load} = 36$A.



(a) Turn-on transient. (b) Turn-off transient.

Figure 5.10: MOSFET current and voltage experimental data plots, when $I_{load} = 40$A.

5.3 Power Losses

By utilizing the solutions described in Chapter 2, power losses of inverter A are calculated based on the IGBT module datasheet under various operating conditions. To ensure the calculation results are comparable to the experimental results, the actual inverter operating conditions in experiments are utilized in the calculations. The experimental set-up consists of a PM motor driven by the designed inverter and an induction motor with a commercial rectifier-inverter drive module. The commercial drive module is powered by a three-phase AC source and it is sharing DC-link with the designed inverter. Additionally, different power factor and modulation index can be achieved by regulating the induction motor speed as well as the output current amplitude and angle in the designed inverter. Operating conditions are listed in Table 5.6, where t_{rr} and I_{rr} are measured from the experiments.

Table 5.6: Inverter experimental conditions.

Parameters	Values	
	Inverter A	Inverter B
DC-link voltage U_{dc} [V]	300	300
RMS value of output current I_{rms} [A]	42.5	42.5
Peak value of output current I_{peak} [A]	60	60
Diode reverse recovery time t_{rr} [ns]	153	450
Diode reverse recovery current I_{rr} [A]	43.6	47.3
Switching frequency f_{sw} [kHz]	10	10

The calculation and experimental results of power losses are shown in Table 5.7, in which the values of $cos\phi$ and M are measured by a power analyzer and they are utilized in calculations. From these results, it can be seen that estimation errors are within ±10%; then the the thermal management system can be selected based on the estimated inverter power losses.

Table 5.7: Calculation ($P_{loss,cal}$) and experimental ($P_{loss,ex}$) results of the inverter A power loss.

$cos\phi$	M	$P_{loss,cal}$	$P_{loss,ex}$	Error
0.288395	0.3866	392.5970 [W]	366.05 [W]	-7.25%
0.342625	0.4516	392.4511 [W]	386.265 [W]	-1.6%
0.39102	0.5093	388.1316 [W]	417.32 [W]	6.99%
0.433425	0.5641	391.5745 [W]	414.075 [W]	5.43%
0.49886	0.6540	390.3586 [W]	428.95 [W]	9%
0.5432	0.7273	389.4740 [W]	413.865 [W]	5.89%
0.567935	0.7868	388.8905 [W]	380.305 [W]	-2.26%

According to the results shown in Table 5.7, there is a difference between the estimated inverter power losses and the measured values under each listed operating condition. Besides, when $cos\phi$ and M increase, both of the estimated and measured power losses fluctuate and decrease slightly. Considering the comparison between two groups of results from the estimations and experiments, conclusions are drawn below.

- Referring to the comparison between the calculation and experimental power loss results, the measured power losses are determined by the difference between inverter input and output power, which consists of not only the power loss in

semiconductor devices but also that in DC-link capacitors, bus bars, cables and some other components in the circuit. Although equivalent resistances of the capacitors, bus bars or cables are very small, about several milliohms, power losses in semiconductor devices still should not be assumed exactly same as the total power loss of the inverter. What's more, the junction temperature used in the calculations cannot be guaranteed exactly the same as the actual value during the experiments, which will also results in the difference between the estimated and measured inverter power loss. Therefore, the estimation error cannot be avoided with the calculation and measurement method described here.

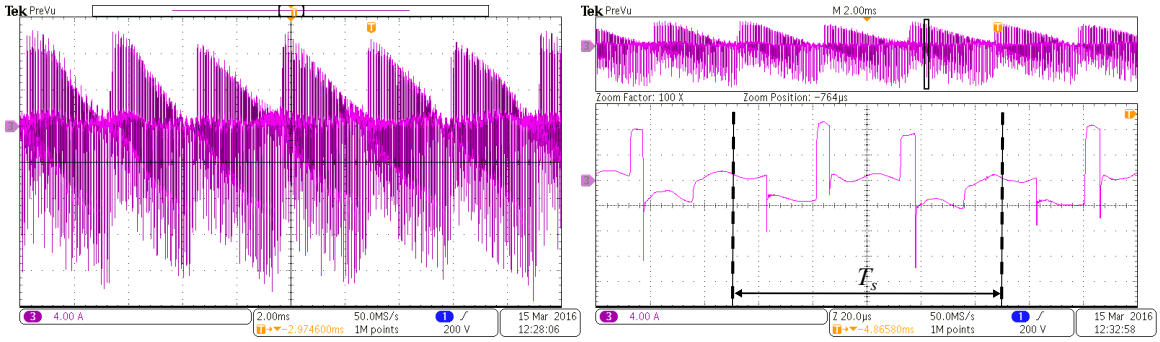
- The fluctuations acquired in both calculation and experimental results are caused by the variations in DC-link voltage and inverter output RMS current. During the operation, the average DC-link voltage of the system changes between 290V and 300V, while the output RMS current varies between 40A and 43A. Furthermore, the analytical evaluation of the total power loss is derived depending on the actual measured average DC-link voltage and RMS value of the output current. Therefore, fluctuations occur in both calculation and experimental results.

5.4 DC-link Voltage and Current Ripple

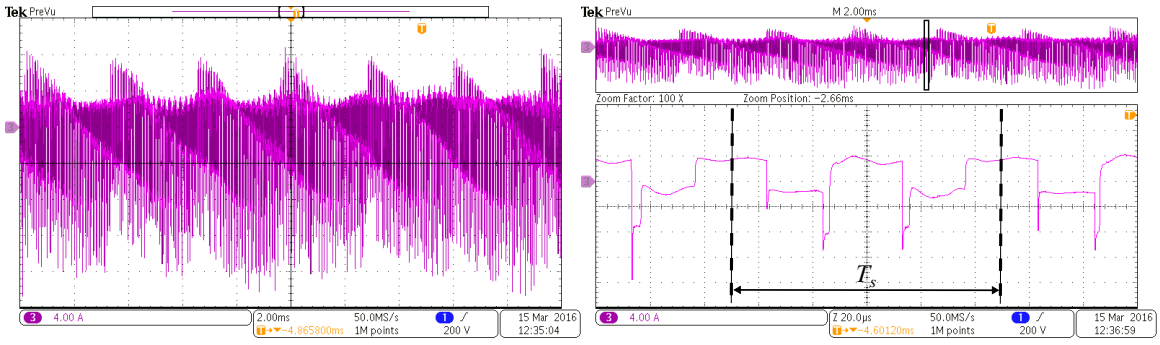
Utilizing the analytical method addressed in Chapter 3, the DC-link voltage and current ripples are estimated based on the measured values of I_{rms}, $cos\phi$, M, t_{rr} and I_{rr}; and the experimental verifications are also discussed in this section.

5.4.1 DC-link capacitor current

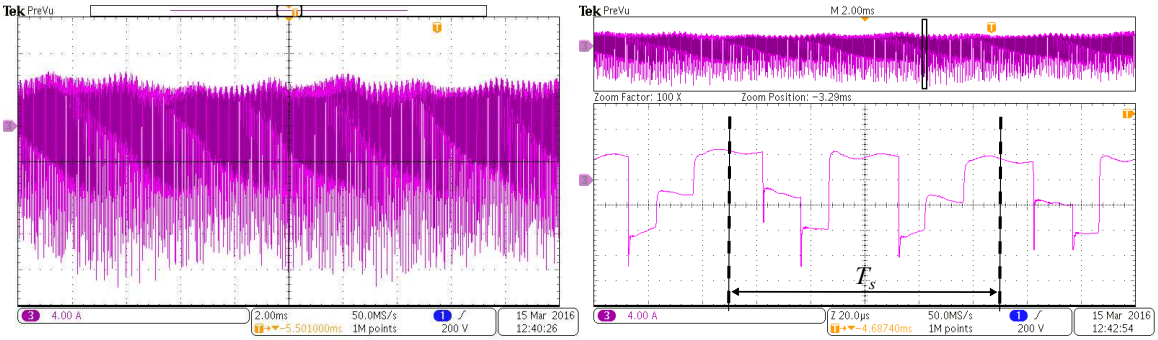
First of all, the DC-link current ripple component is measured. As it has been discussed previously, the ripple component of the DC-link current is equivalent to the capacitor current; therefore, the DC-link capacitor current is measured instead. There are five capacitors used in inverter B and the currents flowing through them are similar to each other. Then the current of one capacitor is shown in Figure 5.11.



(a) When $cos\phi = 0.1$.



(b) When $cos\phi = 0.6$.



(c) When $cos\phi = 1$.

Figure 5.11: Measured DC-link capacitor current.

5.4.2 Voltage ripple

The DC-link voltage ripple is measured under various operating conditions. The PWM technique of SVPWM is implemented to drive the PM motor in experiments, thus the voltage ripple is estimated by using the solutions described in Section 3.3.1. Although the method for voltage ripple calculations is discussed with and without the consideration of the diode reverse recovery, the influence in DC-link voltage ripple

Table 5.8: Calculation (ΔV_{cal}) and experimental (ΔV_{ex}) results of the DC-link voltage ripple.

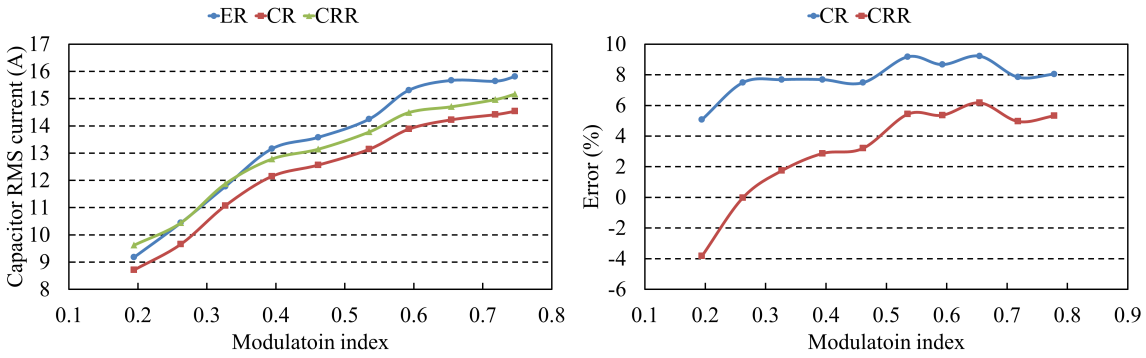
$cos\phi$	M	ΔV_{cal}	ΔV_{ex}	Error
0.288395	0.3866	0.4777 [V]	0.44 [V]	8.57%
0.342625	0.4516	0.6046 [V]	0.66 [V]	-8.39%
0.39102	0.5093	0.7425 [V]	0.79 [V]	-6.01%
0.433425	0.5641	0.8798 [V]	0.97 [V]	-9.3%
0.49886	0.6540	0.9361 [V]	1.01 [V]	-7.32%
0.5432	0.7273	1.4286 [V]	1.48 [V]	-3.47%
0.567935	0.7868	1.6536 [V]	2.68 [V]	-10.13%

caused by the diode reverse recovery is negligible. Therefore, the estimated results are obtained by solving (3.70) to (3.74); and the maximum value among the calculated results is considered as the voltage ripple. The calculation and experimental results are illustrated in Table 5.8.

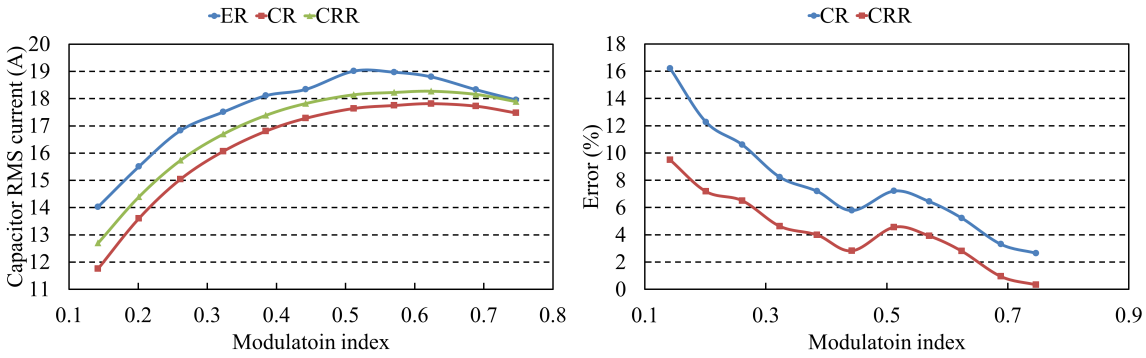
5.4.3 Current ripple

As it is discussed in Section 3.2, two methods are described for the RMS value estimation of the DC-link ripple current. The existing method calculates the RMS value of the ripple current based on the ideal inverter input current without considering the influence of the inverter anti-parallel diode reverse recovery and dead time. On the other hand, a proposed method is developed with the consideration of the diode reverse recovery. According to both of the existing and proposed methods, it can be seen that the RMS value of the DC-link ripple current changes along with the inverter operating condition; in other words, different DC-link ripple current could be acquired depending on the distinct system parameters, such as inverter output current (I_{rms}), power factor ($cos\phi$), modulation index (M). Additionally, from (3.57) that is derived by the proposed solution, the switching frequency f_{sw}, reverse recovery time t_{rr}, and current I_{rr} also contribute to the inverter DC-link current and its ripple component. The estimation accuracies of the existing and proposed methods are evaluated by experimental results. The calculation results are obtained based upon the practical measured parameters. Values of the inverter output RMS current, power factor and modulation index are all acquired by a power analyzer; and the diode reverse recovery current and time are measured by the oscilloscope. In the experimental validation,

the DC-link capacitor currents are measured instead of capturing the DC-link ripple current directly. Data are collected from the calculations and experiments under currents of 40A and 60A. When the power factor is a fixed parameter, the variation trends of the RMS current through DC-link capacitors are shown by the data plots in Figure 5.12 and Figure 5.13, where ER, CR, and CRR denote the data plots of experimental results, calculation results by the existing method, and calculation results by the proposed method, respectively.

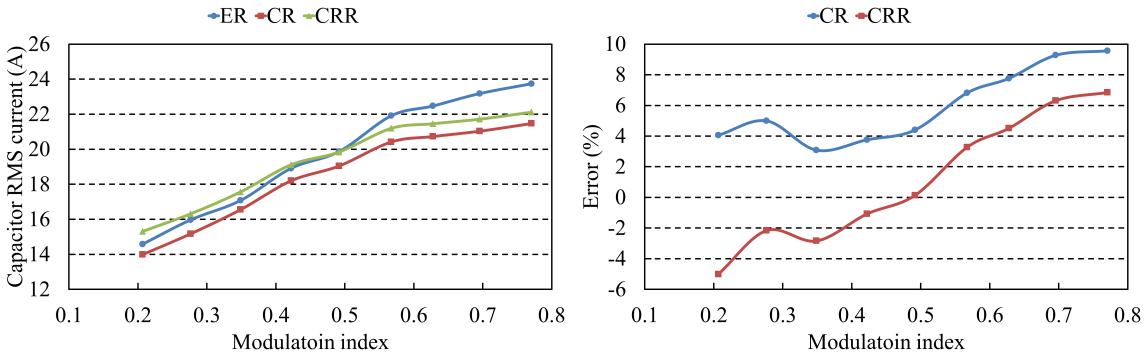


(a) When $cos\phi = 0.5$.

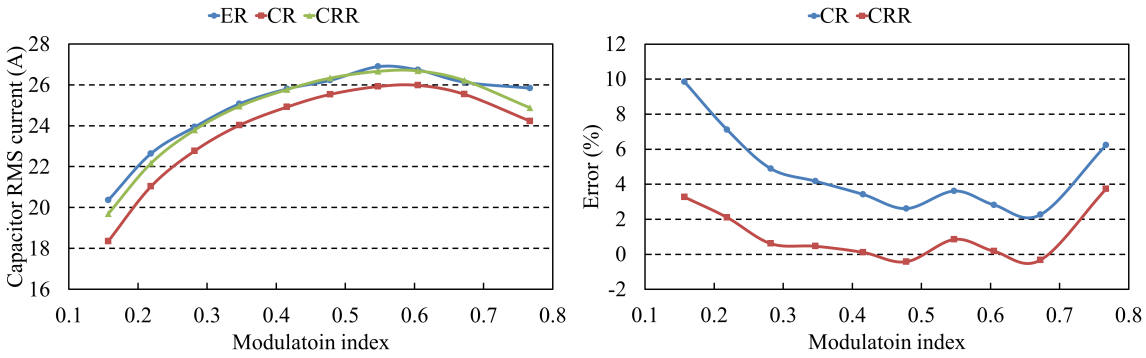


(b) When $cos\phi = 1$.

Figure 5.12: DC-link capacitor RMS current calculation and experimental data plots (left) and error plots (right), when $I_{peak} = 40$A, $f_{sw} = 10$kHz, $\cos\phi$ is constant.



(a) When $cos\phi = 0.5$.

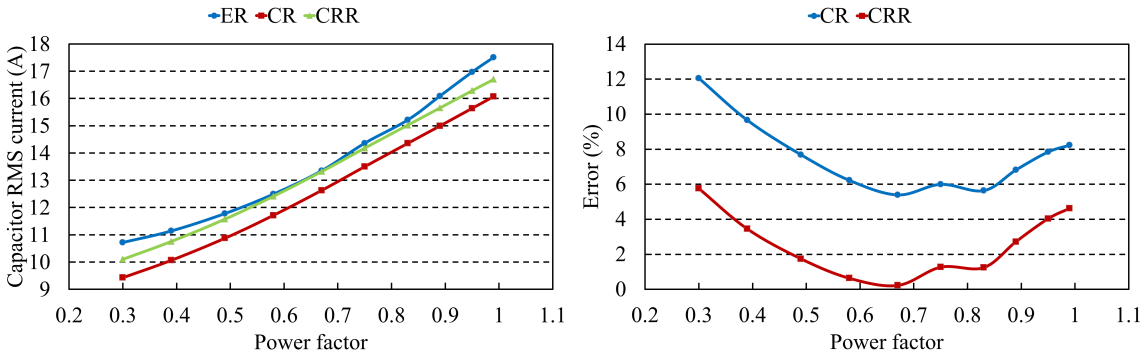


(b) When $cos\phi = 1$.

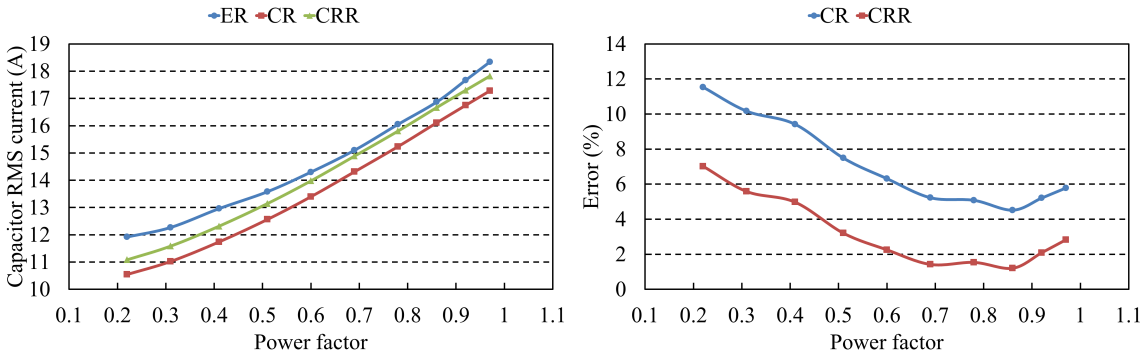
Figure 5.13: DC-link capacitor RMS current calculation and experimental data plots (left) and error plots (right), when $I_{peak} = 60$A, $f_{sw} = 10$kHz, $\cos\phi$ is constant.

The results on the left in Figure 5.12 and Figure 5.13 are obtained under the condition that the power factor is constant and the modulation index varies from 0.1 to 0.8 (Haghbin and Thiringer, 2014; Inazuma *et al.*, 2013). It is obvious that as the modulation index grows, the capacitor RMS current rises. When the power factor is 1, the capacitor RMS current decreases after it reaches a maximum value as the modulation index increasing. In contrast, when the power factor is relatively low around 0.5, the increase of the capacitor RMS current slows down. The variation

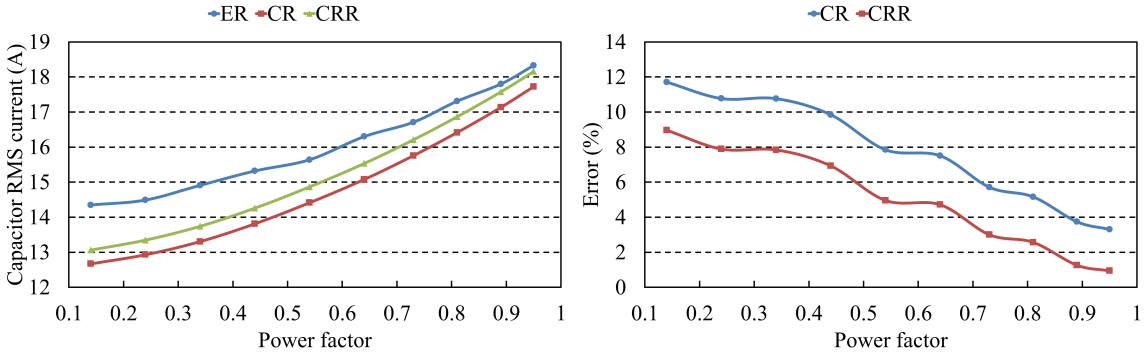
trends obtained from experiments match the analysis in (Kolar and Round, 2006). The estimation errors of the existing and proposed methods are plotted on the right. If the modulation index is set as a constant parameter and when the power factor rises from 0.1 to 1, another two groups of calculation and experimental results are acquired in Figure 5.14 and Figure 5.15. These results are also obtained under the conditions of 40A and 60A inverter output peak current. According to these results, it is indicated that the variation trends of the capacitor RMS current are different from those derived under the scenario of constant power factor. With different modulation index, the DC-link capacitor RMS current rises along with the increase of the power factor. When the power factor rises from 0.1 to 1, the DC-link capacitor RMS current rise is varying under different modulation index. A smaller value of the modulation index leads to a larger current rise. For instance, when $I_{peak} = 60$A and $M = 0.3$, the change in capacitor RMS current as power factor increase from 0.1 to 1 is 9A; in contrast, they are 7A and 5A from the calculations and experimental results when $M = 0.7$.



(a) When $M = 0.3$.

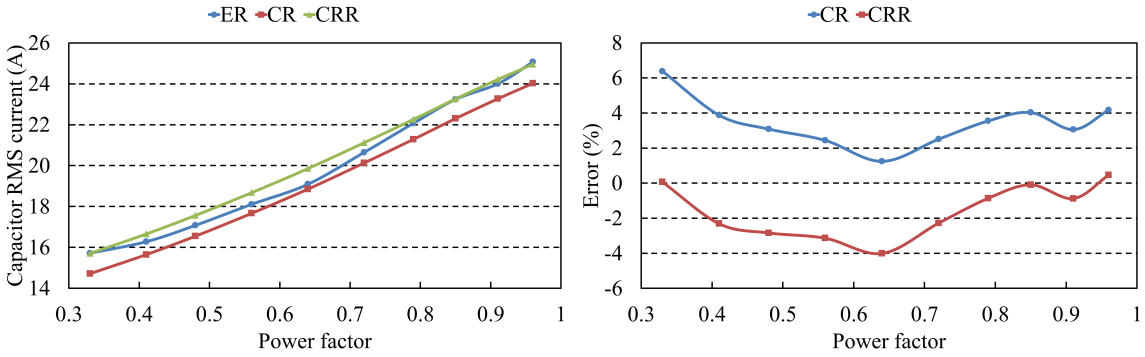


(b) When $M = 0.5$.

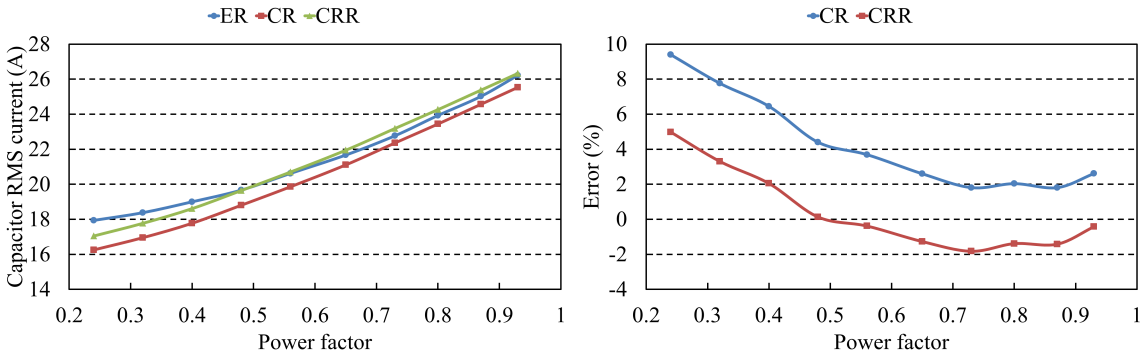


(c) When $M = 0.7$.

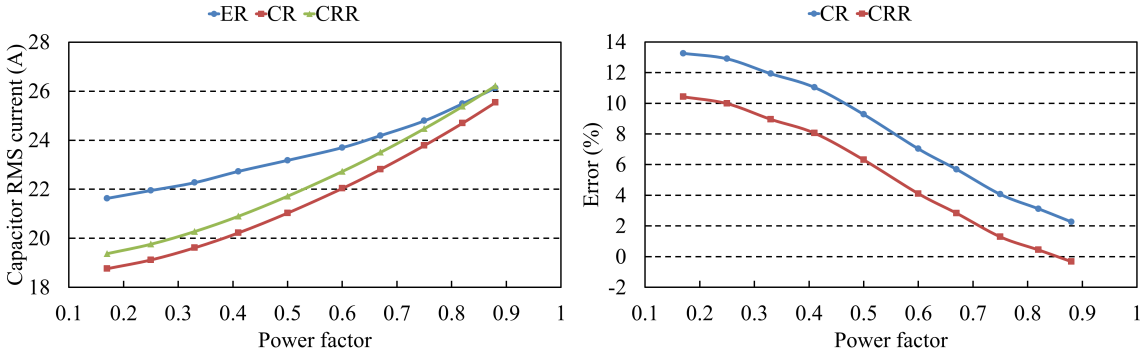
Figure 5.14: DC-link capacitor RMS current calculation and experimental data plots (left) and error plots (right), when $I_{peak} = 40$A, $f_{sw} = 10$kHz, M is constant.



(a) When $M = 0.3$.



(b) When $M = 0.5$.



(c) When $M = 0.7$.

Figure 5.15: DC-link capacitor RMS current calculation and experimental data plots (left) and error plots (right), when $I_{peak} = 60$A, $f_{sw} = 10$kHz, M is constant.

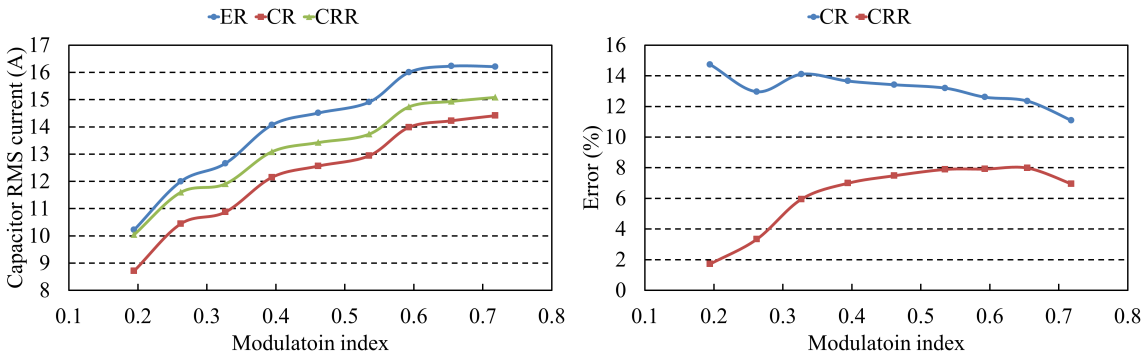
The accuracy of the DC-link capacitor RMS current estimation are shown by the error plots in Figure 5.12 to Figure 5.15. The calculation results acquired by the proposed method is closer to the experimental results than that obtained by the existing method. When both power factor and modulation index are relatively high, estimations are more accurate than those under other inverter operating conditions.

By utilizing the proposed method, the smallest estimation error achieves within $\pm 0.5\%$ and the largest error is around 10%. The smallest and largest error obtained by the existing method are around 2% and 16% respectively. In addition, most of

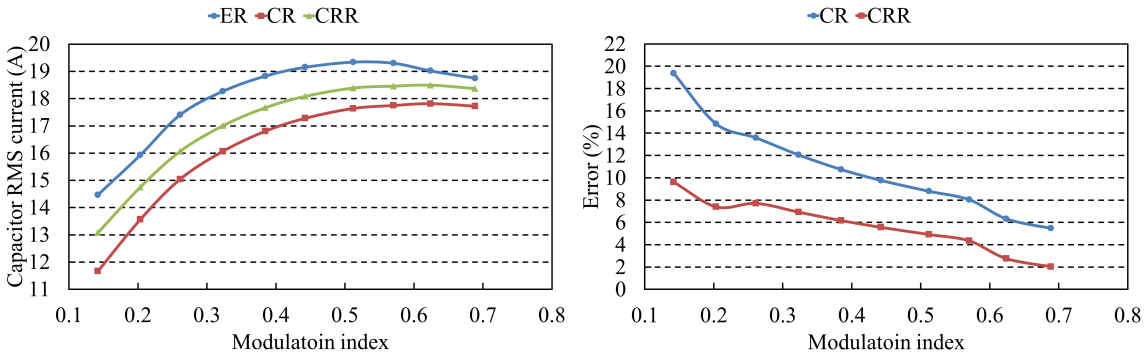
the calculation results by the proposed method have errors in the range of ±5%; however, most of the errors acquired by the existing method are between 5% and 10%. Therefore, by taking the anti-parallel diode reverse recovery into account, the accuracy of the DC-link capacitor RMS current estimation is improved.

5.4.4 DC-link current ripple switching frequency dependence

Recall the proposed method for DC-link current and its ripple component calculations in Section 3.2, according to the expression obtained in (3.57), the DC-link current is influenced by not only t_{rr} and I_{rr} but also f_{sw} when the anti-parallel diode reverse recovery is taken into account. In order to have an insight into the correlation between $I_{rms,ripple}$ and f_{sw}, f_{sw} that is 10kHz in the previous experiments is raised and set at 15kHz. The experiments are also implemented under 40A and 60A inverter output peak current. In addition, other inverter operating conditions are close to those when 10kHz switching frequency is utilized. When the power factor is constant around 0.5 and 1, the calculation and experimental results are acquired as the modulation index varying from 0.1 to 0.8, seen in Figure 5.16 and Figure 5.17. Besides, the estimation accuracies are also evaluated on the right.

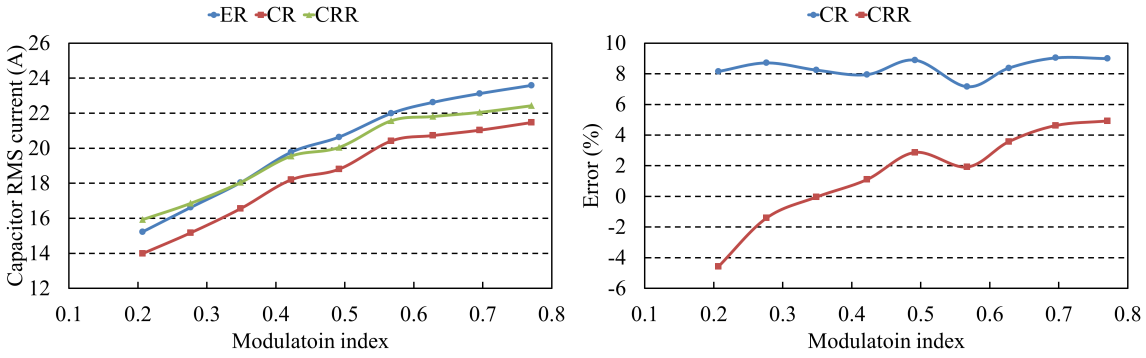


(a) When $cos\phi = 0.5$.

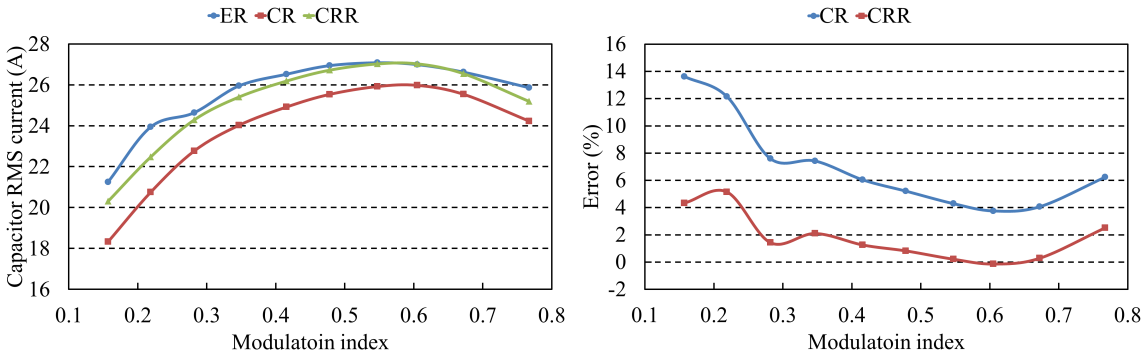


(b) When $cos\phi = 1$.

Figure 5.16: DC-link capacitor RMS current calculation and experimental data plots (left) and error plots (right), when $I_{peak} = 40$A, $f_{sw} = 15$kHz, $\cos\phi$ is constant.



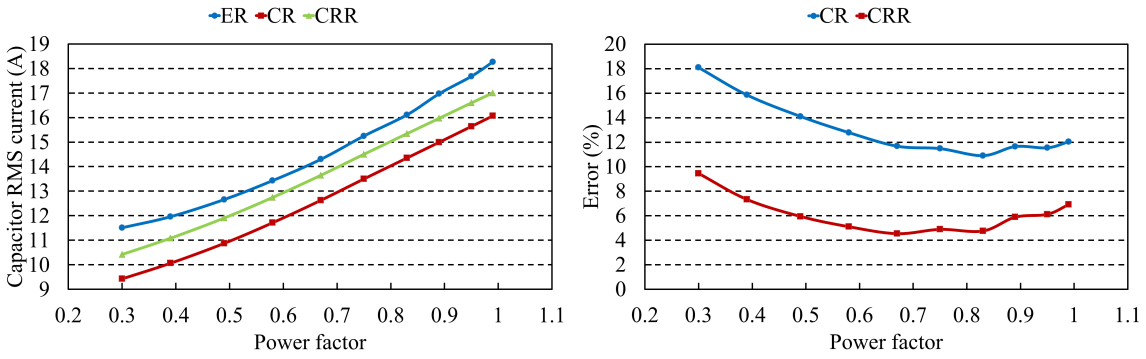
(a) When $cos\phi = 0.5$.



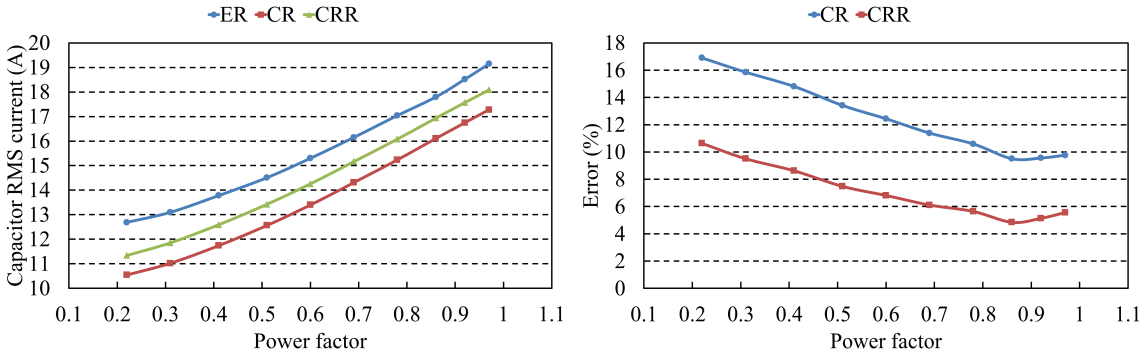
(b) When $cos\phi = 1$.

Figure 5.17: DC-link capacitor RMS current calculation and experimental data plots (left) and error plots (right), when $I_{peak} = 60$A, $f_{sw} = 15$kHz, $\cos\phi$ is constant.

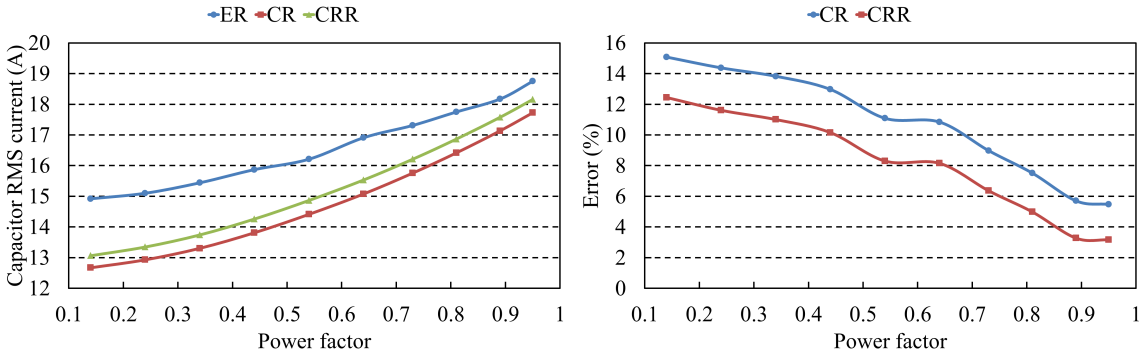
Variation trends of the DC-link capacitor RMS current under 15kHz are similar to those derived under 10kHz, which can also be found in the following results when the modulation index is constant, seen in Figure 5.18 and Figure 5.19.



(a) When $M = 0.3$.

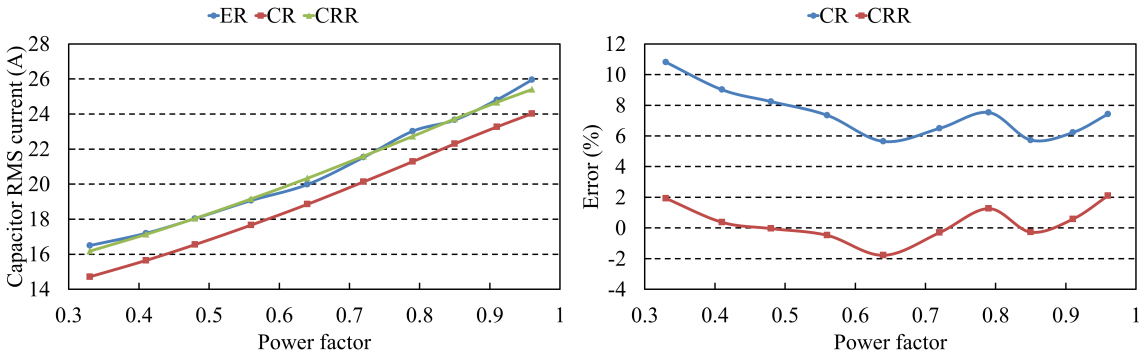


(b) When $M = 0.5$.

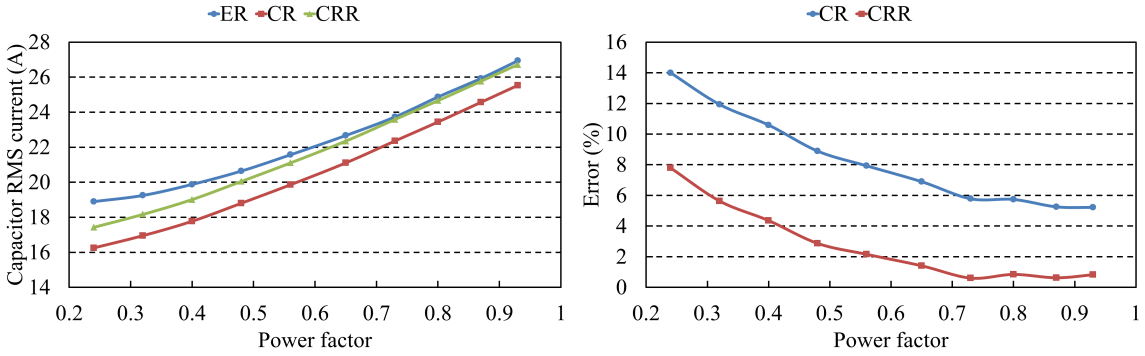


(c) When $M = 0.7$.

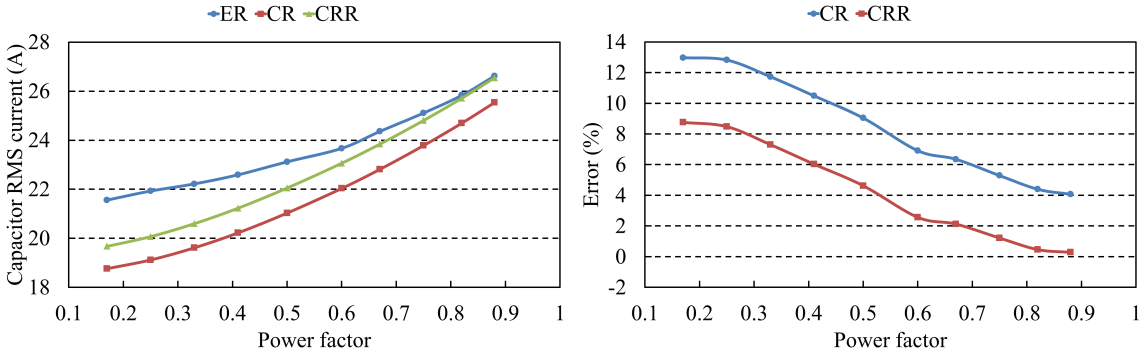
Figure 5.18: DC-link capacitor RMS current calculation and experimental data plots (left) and error plots (right), when $I_{peak} = 40$A, $f_{sw} = 15$kHz, M is constant.



(a) When $M = 0.3$.



(b) When $M = 0.5$.



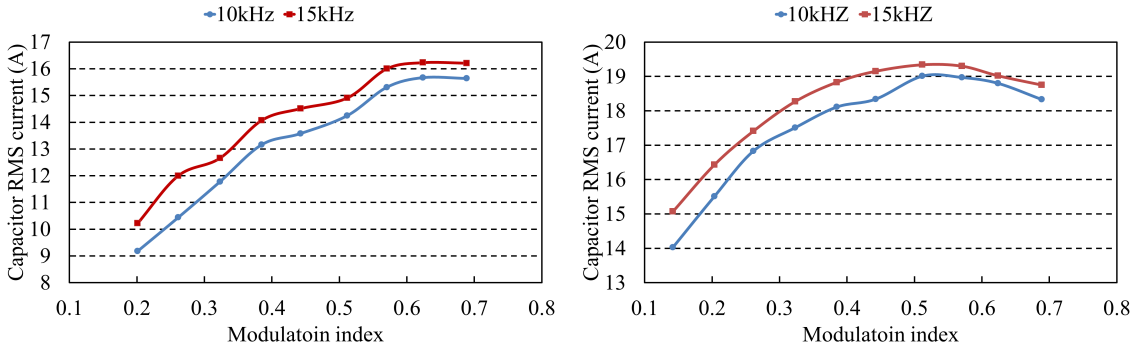
(c) When $M = 0.7$.

Figure 5.19: DC-link capacitor RMS current calculation and experimental data plots (left) and error plots (right), when $I_{peak} = 60$A, $f_{sw} = 15$kHz, M is constant.

The plotted data from calculations and experiments are presented in Figure 5.16 to Figure 5.19, when the switching frequency is 15kHz. These results indicate that the variation trends of the DC-link capacitor RMS current with 15kHz switching frequency are close to those with 10kHz under similar operating conditions. Nevertheless, there are some differences in the estimation accuracies. Comparing to the 10kHz switching frequency scenario, estimations by the proposed method with 15kHz have bigger errors when the output peak current is 40A; especially when the modulation index is low. In spite of this, the accuracy of the proposed calculation method with 15kHz is similar to that with 10kHz; most of the errors are approximately $\pm 5\%$. However, worse estimation accuracy is obtained by the existing method when the switching frequency is 15kHz. For the 40A scenario, most of the estimation errors are above 10%. When the modulation index and power factor are low, some of the errors are even close to 20%. For the 60A scenario, when the power factor and modulation index are high, the estimation errors are in the range of 5% to 10%, which is similar to the results from 10kHz experiments. As the power factor and modulation index decrease, some of the errors grows to the value around 10%. while some of them are about 15% or even higher.

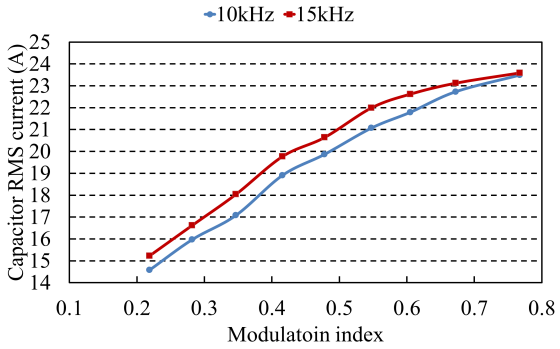
The analysis above reveals that when the switching frequency rises from 10kHz to 15kHz, estimation accuracy of the existing method becomes worse; however, there is not significant change in estimation accuracy of the proposed method. That is because the calculation by the existing method is not related to the switching frequency; and under the same operating conditions the calculation results with 15kHz switching frequency are similar to those with 10kHz. Nevertheless, the capacitor RMS current obtained by the proposed method increases with the rise of the switching frequency.

Furthermore, the actual capacitor RMS current rises when the inverter switching frequency is higher, which can be seen in Figure 5.20. Comparing to the experimental results, it is rational that the estimation errors of the existing method under 15kHz switching frequency are bigger than those under 10kHz switching frequency, while there is no significant difference in the estimation accuracy of the proposed method as the switching frequency increasing.

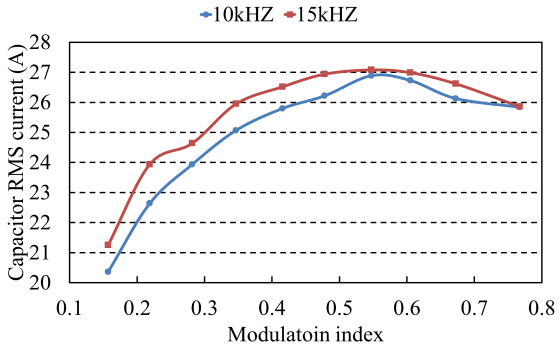


(a) When $I_{load} = 40$A, $\cos\phi = 0.5$.

(b) When $I_{load} = 40$A, $\cos\phi = 1$.



(c) When $I_{load} = 60$A, $\cos\phi = 0.5$.



(d) When $I_{load} = 60$A, $\cos\phi = 1$.

Figure 5.20: DC-link capacitor RMS current experimental data plots with different inverter switching frequency.

5.5 Bus Bar Analysis

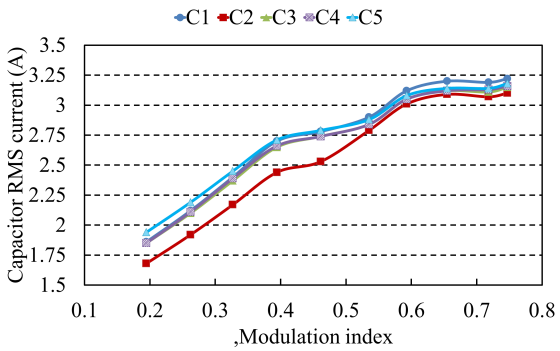
Satisfying the requirement of balanced current distribution and achieving low stray inductance, a laminated copper bus bar is designed for inverter B. Measurements of the stray parameters and experimental verifications for the analysis of the AC current distribution and voltage spikes are demonstrated in this section.

5.5.1 Current distribution

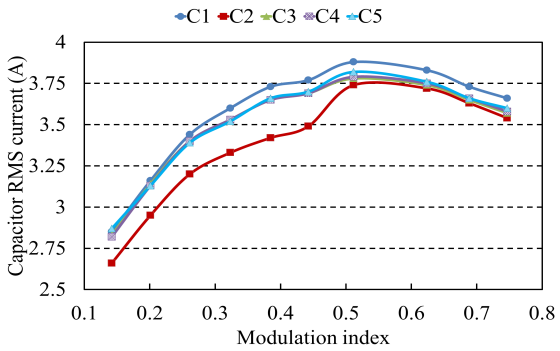
In fact, it is difficult to validate the bus bar DC current distribution between DC input tabs and semiconductor connection terminals by directly measuring the current on the conductor. One alternative way is to measure the temperature of the conductor plate by using thermal camera; since the temperature rise would be caused by the current flowing through the conductor. If the temperature of every part on the bus bar is close to each other, it is assumed that the DC current distribution is balanced. However, the bus bar is designed with laminated structure, temperatures of two conductor plates cannot be measured separately; and it is difficult to obtain convincing results. In contrast, the AC current distribution can be verified by measuring the RMS currents of five DC-link capacitors. The AC current on the bus bar is equivalent to the DC-link capacitor current, as a result, the AC current distribution can be validated by evaluating the current sharing among DC-link capacitors. Therefore, only AC current distribution is experimentally validated in this thesis.

There are five DC-link capacitors and the currents flow through them are measured individually; and Rogowski current probes are utilized for the measurements. The RMS value of each capacitor current is captured by the oscilloscope. The experimental data of these five capacitor RMS currents are acquired when the inverter output peak

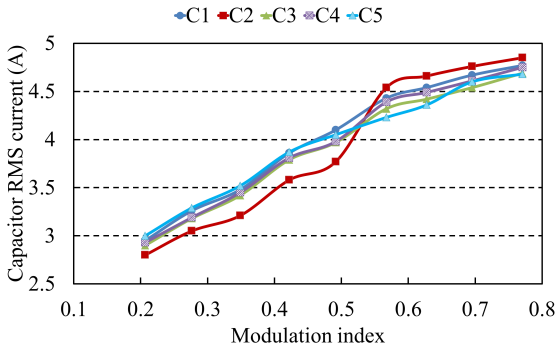
current is 40A and 60A. As the power factor is constant and the modulation index varies, the RMS current through each capacitor is obtained. Figure 5.21 shows the data plots of these five capacitor currents when the switching frequency is 10kHz, while those obtained under 15kHz are presented by Figure 5.22, where C_1, C_2, C_3, C_4, and C_5 denote five DC-link capacitors. According to those plots, most of the RMS currents in the five DC-link capacitors are close to each other. Although there seems an obvious difference among the capacitor currents under 10kHz operation in



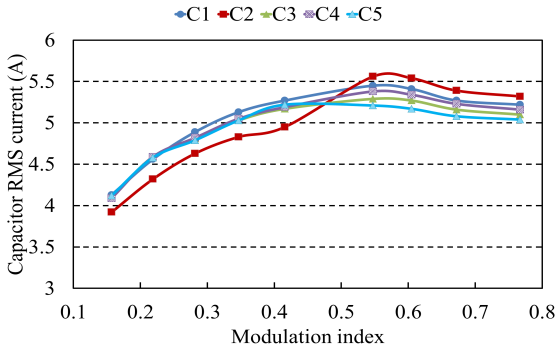
(a) When $I_{load} = 40$A, $\cos\phi = 0.5$.



(b) When $I_{load} = 40$A, $\cos\phi = 1$.

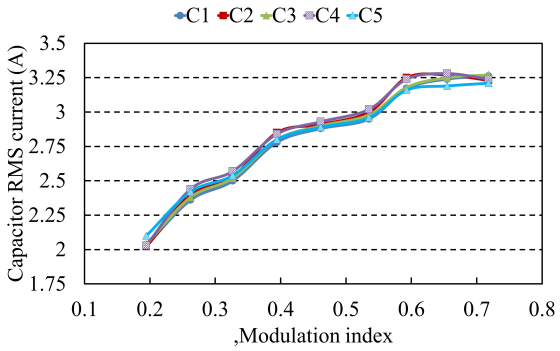


(c) When $I_{load} = 60$A, $\cos\phi = 0.5$.

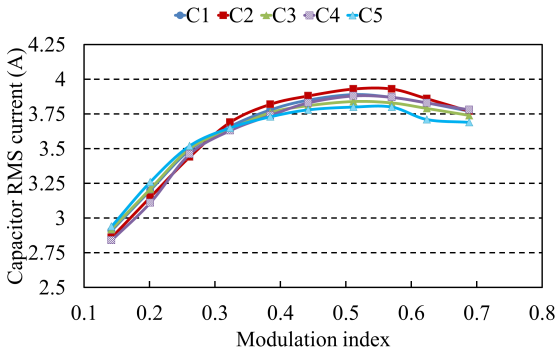


(d) When $I_{load} = 60$A, $\cos\phi = 1$.

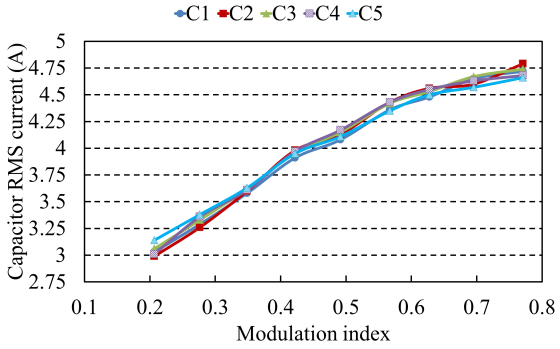
Figure 5.21: Experimental data plots of five DC-link capacitor RMS currents, when $f_{sw} = 10$kHz.



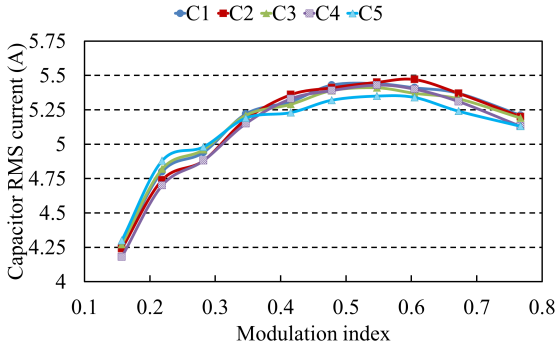
(a) When $I_{load} = 40$A, $\cos\phi = 0.5$.



(b) When $I_{load} = 40$A, $\cos\phi = 1$.



(c) When $I_{load} = 60$A, $\cos\phi = 0.5$.



(d) When $I_{load} = 60$A, $\cos\phi = 1$.

Figure 5.22: Experimental data plots of five DC-link capacitor RMS currents, when $f_{sw} = 15$kHz.

Figure 5.21b and Figure 5.21c, some of these differences are lower than 10% and most of them are around 5%.

Take two of the scenarios for examples, on one hand, when the inverter switching frequency, output peak current, and the power factor are equal to 10kHz, 40A, and 1, data of the current plots presented in Figure 5.21b are listed in Table 5.9. In this table, the RMS current of each capacitor is provided; additionally, the maximum differences in RMS values of those currents are also given. It can be seen that the

Table 5.9: RMS currents in DC-link capacitors and maximum current differences (Max diff.) in percentage, when $I_{peak} = 40$A, $\cos\phi = 1$, and $f_{sw} = 10$kHz.

M	I_{cap1} [A]	I_{cap2} [A]	I_{cap3} [A]	I_{cap4} [A]	I_{cap5} [A]	Max diff.
0.142	2.85	2.66	2.83	2.82	2.87	7.3%
0.201	3.16	2.95	3.14	3.13	3.13	6.6%
0.261	3.44	3.2	3.4	3.4	3.39	7%
0.323	3.6	3.33	3.53	3.53	3.52	7.5%
0.385	3.73	3.42	3.65	3.65	3.66	8.3%
0.442	3.77	3.49	3.69	3.69	3.7	7.4%
0.512	3.88	3.74	3.78	3.79	3.82	3.6%
0.624	3.83	3.72	3.74	3.75	3.76	2.9%
0.689	3.73	3.63	3.65	3.66	3.66	2.7%
0.747	3.66	3.54	3.57	3.58	3.6	3.3%

Table 5.10: RMS currents in DC-link capacitors and maximum current differences (Max diff.) in percentage, when $I_{peak} = 60$A, $\cos\phi = 0.5$, and $f_{sw} = 10$kHz.

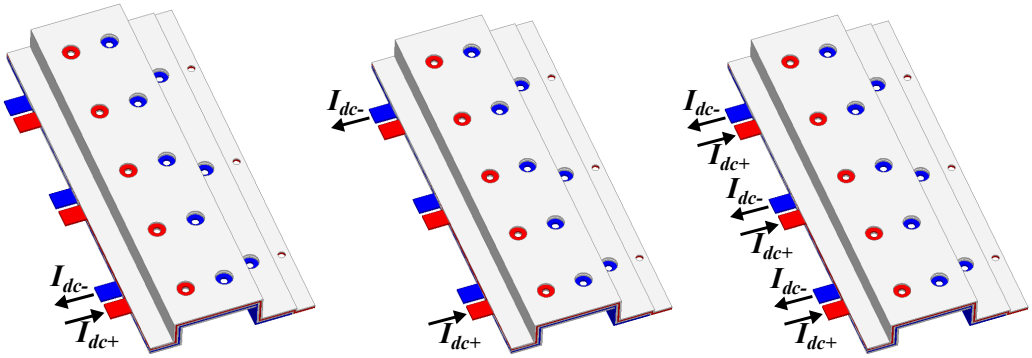
M	I_{cap1} [A]	I_{cap2} [A]	I_{cap3} [A]	I_{cap4} [A]	I_{cap5} [A]	Max diff.
0.207	2.95	2.28	2.9	2.93	3	6.6%
0.276	3.26	3.05	3.18	3.19	3.29	7.3%
0.349	3.48	3.21	3.42	3.45	3.52	8.8%
0.422	3.86	3.58	3.79	3.81	3.87	7.5%
0.492	4.1	3.77	3.97	3.98	4.05	8%
0.567	4.43	4.54	4.32	4.39	4.23	6.8%
0.628	4.54	4.66	4.42	4.49	4.36	6.4%
0.7	4.67	4.76	4.54	4.61	4.6	4.6%
0.771	4.77	4.85	4.69	4.75	4.68	3.5%

maximum value of "Max diff." is 8.3%; meanwhile, the minimum value is 2.7%. On the other hand, when the inverter switching frequency, output peak current, and the

power factor are equal to 10kHz, 60A, and 0.5, the RMS current data and values of "Max diff." are presented in Table 5.10, in which the maximum and minimum values of "Max diff." are 8.8% and 3.5%.

Furthermore, when the switching frequency is 15kHz, the current sharing among five DC-link capacitors is better, which can apparently be found from the data plots in Figure 5.22. Therefore, it can be concluded that the balanced current sharing among five DC-link capacitors is achieved.

The analysis in Section 4.2 mentions that the locations of the DC input tabs do not affect the AC current distribution, which is also experimentally validated. The experiments are implemented by utilizing different numbers and locations of the DC input tabs, and then the AC current distribution is examined under each situation. Three DC input connection types are shown by Figure 5.23, where I_{dc+} and I_{dc-} are DC current on the positive and negative plate.

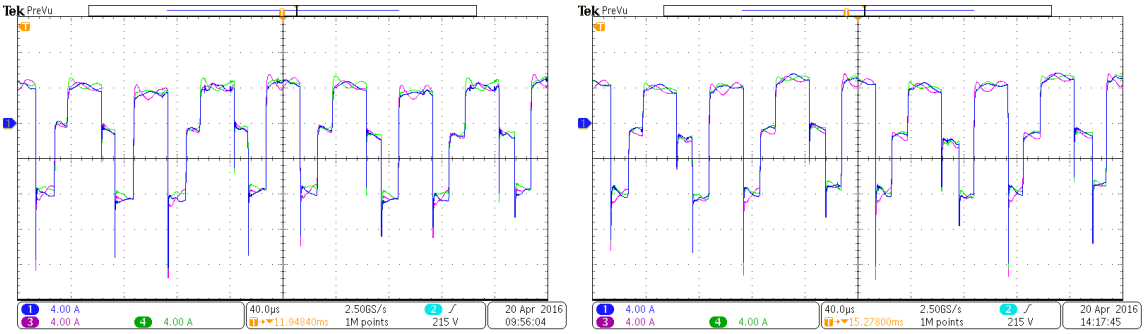


(a) Type 1. (b) Type 2. (c) Type 3.

Figure 5.23: DC input connections.

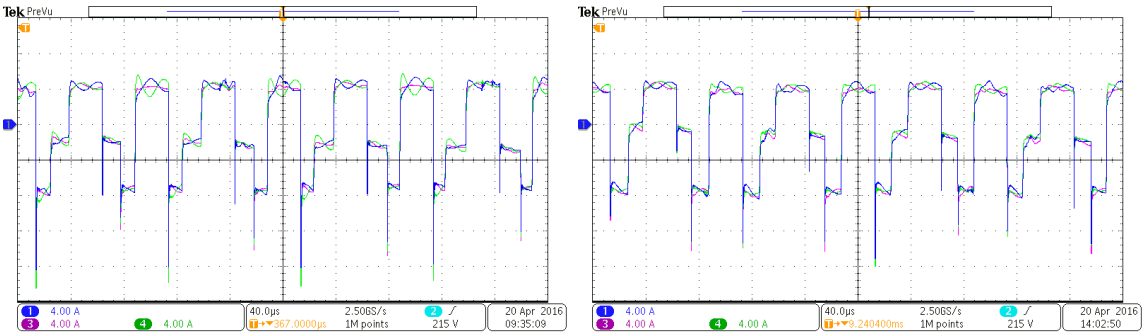
When $I_{load} = 60$A, $f_{sw} = 10$kHz, and $\cos\phi = 1$, the current sharing among five DC-link capacitors is examined by three Rogowski current probes. The currents of

capacitor 1, 3, and 5 are measured at the same time. Then keeping the current probe on the capacitor 3 unchanged, the current transducers on capacitor 1 and 5 are moved to the other two capacitors, 2 and 4; currents in capacitor 2, 3, and 4 are measured under the same conditions when current in capacitor 1, 3, and 5 are obtained. The previous steps are repeated for all three types of the DC input connection scenarios. The captured current waveforms are shown in Figure 5.24 to Figure 5.26, which denote the balanced AC current distribution has nothing to do with the numbers and locations of the DC input tabs.



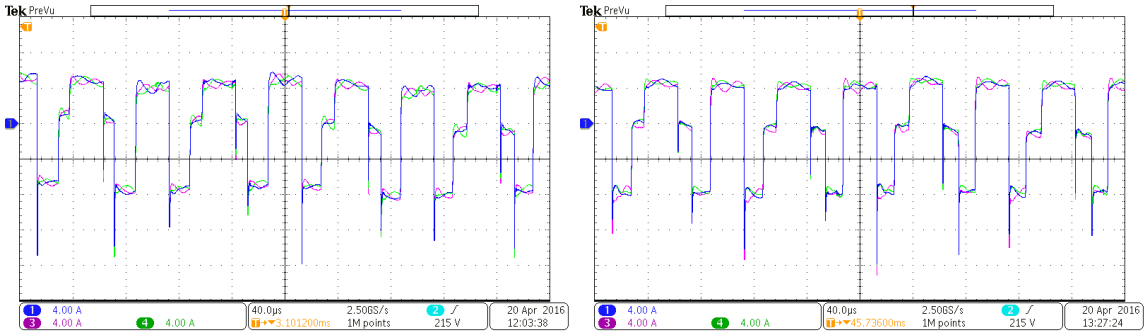
(a) Currents in capacitor 1, 3, and 5. (b) Currents in capacitor 2, 3, and 4.

Figure 5.24: Measured DC-link capacitor currents with DC input connection type 1.



(a) Currents in capacitor 1, 3, and 5. (b) Currents in capacitor 2, 3, and 4.

Figure 5.25: Measured DC-link capacitor currents with DC input connection type 2.



(a) Currents in capacitor 1, 3, and 5. (b) Currents in capacitor 2, 3, and 4.

Figure 5.26: Measured DC-link capacitor currents with DC input connection type 3.

5.5.2 Stray inductance and capacitance

The stray inductance and capacitance are predicted by the simulations, and an impedance analyzer is used to validate the simulated results in Table 5.11. In sim-

Table 5.11: Bus bar stray inductance and capacitance, $L_{total,s}$ and C_s: simulated values; $L_{total,m}$ and C_m: measured values.

Frequency	$L_{total,s}$	$L_{total,m}$	C_s	C_m
10kHz	18.336nH	18.554nH	1.986nF	1.636nF
20kHz	16.983nH	17.67nH	1.984nF	1.632nF
30kHz	16.376nH	17.55nH	1.981nF	1.63nF
40kHz	16.013nH	17.28nH	1.977nF	1.629nF
50kHz	15.765nH	17.37nH	1.973nF	1.628nF
60kHz	15.582nH	17.25nH	1.971nF	1.627nF
70kHz	15.439nH	17.06nH	1.968nF	1.626nF
80kHz	15.324nH	16.96nH	1.965nF	1.625nF
90kHz	15.228nH	16.93nH	1.963nF	1.625nF
100kHz	15.148nH	16.82nH	1.96nF	1.624nF

ulations, AC analysis is utilized to evaluate the stray inductance and capacitance; thus two conductors in the bus bar are shorted together at the installation holes of the DC-link capacitors and the AC current is injected from the terminals for IGBT connections into the 3D model. During the practical measurements, the bus bar is shorted the same way as that in the simulations; and the simulation model is built as close to the actual under testing bus bar as possible. However, it is still difficult to guarantee that the simulation model is exactly same as the practical bus bar, and the difference between the simulation and measured results could not be avoided.

5.6 Voltage Spike

The analysis for voltage spike during the IGBT turn-off transients is experimentally validated. With the stray inductance predicted by the simulations, voltage spikes during the turn-off transients are calculated. Meanwhile, the double pulse tests are implemented to verify the estimated voltage spike. The calculation and experimental results in four cases with different current levels are demonstrated in Table 5.12. The parameters used in the calculations, such as IGBT current I_c, IGBT voltage V_{ce} and time interval Δt for the fall of I_c are acquired from experimental measurements. For the estimated results, simulated bus bar stray inductance and equivalent series inductances given by the capacitor and IGBT datasheets are utilized to estimate the voltage spike. At the same time, for the measured results, the voltage spike is obtained by the oscilloscope and the total stray inductance in the circuit is calculated accordingly by the measured voltage spike.

Table 5.12: Estimated and experimental voltage spikes under four current conditions.

Parameters	Case 1		Case 2	
	Estimated	Measured	Estimated	Measured
I_c (A)	101	101	208	208
V_{ce} (V)	300	300	300	300
Δt (ns)	110	110	115	115
L_{stray} (nH)	44.34	47.92	44.34	42.02
V_{spike} (V)	40.7	44	80.2	76
V_{peak} (V)	340.7	344	380.2	376
Error	7.5%		-5.52%	

Parameters	Case 3		Case 4	
	Estimated	Measured	Estimated	Measured
I_c (A)	306	306	469	469
V_{ce} (V)	300	300	300	300
Δt (ns)	140	140	155	155
L_{stray} (nH)	44.34	43	44.34	40.31
V_{spike} (V)	96.9	94	134.16	122
V_{peak} (V)	396.9	394	434.2	422
Error	-2.65%		-9.97%	

5.7 Summary

In this chapter, the experimental verifications for the analysis in previous chapters are demonstrated. Firstly, inverter power loss calculation and experimental results are

presented. In different operating conditions, the calculation accuracies are within the range of ±10%. Secondly, double pulse tests are implemented to capture the MOSFET switching transients; in this way, the existing and proposed methods for MOSFET voltage rise- and fall-time estimation are experimentally verified. The significant improvements in the estimation accuracy by the proposed method are validated by the experimental results. Thirdly, the calculation and experimental results of the DC-link voltage ripple are listed. Fourthly, by considering the inverter anti-parallel diode reverse recovery, DC-link current and its ripple component are estimated by both of the existing and proposed methods. From the data plots of the experimental results, it is proved that the estimation accuracy is improved by the proposed method by up to 7%. Fifthly, the analysis for the RMS value of the DC-link ripple current switching frequency dependence is verified by the experiments. With different inverter operating switching frequency, a positive correlation exists between the DC-link ripple current RMS value and the inverter switching frequency. In addition, it is also found that, as the switching frequency increases, most of the estimation accuracies of the DC-link ripple current RMS value by the proposed method remain in the range of ±5%. However, an obvious drop appears in the estimation accuracy of the existing method as the switching frequency rises. Sixthly, the AC current distribution of the designed bus bar is evaluated by experiments. RMS values of the currents flowing through five DC-link capacitors are measured and compared. According to the acquired data, the capacitor RMS currents are close to each other under various operating conditions. The maximum and minimum difference among these capacitor currents are about 8% and 1%. Seventhly, the stray inductance and capacitance under different current frequency are measured by an impedance analyzer. Although it is difficult to ensure

that the simulation model is exactly same as the under testing bus bar circuit, the measured results are closed to the predicted values. Finally, voltage spikes during the IGBT turn-off transients are estimated by the bus bar stray inductance obtained in simulations. Then double pulse tests are implemented to verify the estimations. Four cases with various current levels are studied, the maximum and minimum estimation accuracies are 9.97% and 2.65%.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

In this thesis, the design of two level three-phase voltage source inverters is presented with comprehensive analysis.

The power loss estimation for both of the semiconductor devices and entire inverter as well as the selection of the thermal management system are discussed based on datasheets and inverter operating conditions. Comparing to the conduction power loss and IGBT or diode switching power loss calculations, the MOSFET switching power loss estimation is more complicated because of the difficulty in obtaining accurate switching transient times. An existing method for MOSFET voltage rise-time and fall-time estimation during the switching transients is demonstrated. To improve the estimation accuracy, an improved method is proposed. Calculations are derived by both of the existing method and the proposed method. There are large differences among the calculated results obtained by these two methods. In order to verify the

calculated results, double pulse tests are implemented under different current conditions. Then, MOSFET voltage rise-time and fall-time are measured directly from the experimental results. Comparing the calculations with the experimental results, transient times calculated by the proposed method are much closer to the measured values than those calculated by the existing method. Therefore, it is proved that the estimation accuracy of the MOSFET voltage rise-time and fall-time is improved significantly by the proposed method.

In order to provide references for the DC-link capacitor selection, two methods for the DC-link current and voltage ripple estimation are introduced depending on three types of PWM techniques. The existing method neglects the inverter anti-parallel diode reverse recovery and the proposed method considers the influence of diode reverse recovery. The transient and occurrence of the diode reverse recovery during the switching period T_s is discussed. Then, the proposed method is analytically presented and experimentally verified. By considering the diode reverse recovery, the estimation accuracy of the DC-link current ripple RMS value is improved and most of the errors obtained under different inverter operating conditions are within $\pm 5\%$. Furthermore, according to the proposed method, the RMS value of the DC-link ripple current is influenced by the inverter switching frequency; and, it reveals that the inverter DC-link ripple current RMS value is influenced by not only the inverter output current, power factor, and modulation index, but also the anti-parallel diode reverse recovery and inverter switching frequency. In addition, the influence in DC-link voltage ripple by the diode reverse recovery is negligible according to the analysis.

A bus bar is designed with the balanced current distribution and low stray impedance. Bus bar performance is evaluated by the DC and AC analysis in simulations; and most

of them are verified by experiments. The analysis indicates that the DC current distribution is influenced by the numbers and locations of the DC input tabs, while the AC current distribution is affected by the numbers and locations of the installation holes for the DC-link capacitors and semiconductors. The AC current distribution is experimentally verified by measuring the RMS current in each DC-link capacitor. The maximum difference in DC-link capacitor RMS currents is defined as "Max diff.", and the maximum and minimum value of "Max diff." obtained by experiments are 8.8% and 1.3%. Additionally, the stray parameters of the designed bus bar are also evaluated. According to the estimated stray inductance, the voltage spikes are calculated and experimentally validated. Comparing to the experimental results, the maximum and minimum errors in voltage spike estimation are 9.97% and 2.65%.

6.2 Contributions

The contributions of this thesis are listed as the followings.

- A novel method is proposed for the estimation of MOSFET voltage rise- and fall-time during switching transient. The estimation accuracy is significantly improved by the proposed method.
- The impact of the diode reverse recovery on DC-link current and voltage ripple is evaluated. The impact on voltage ripple is negligible; while the current ripple RMS value is influenced by both diode reverse recovery and inverter switching frequency.
- A novel method is developed for the estimation of DC-link current ripple by considering the inverter anti-parallel diode reverse recovery. The estimation

accuracy is improved by the proposed method by up to 7%.

- A positive correlation between the inverter switching frequency and DC-link current ripple RMS value exists, which is analytically and experimentally verified.
- A bus bar is designed. The current distribution and parasitic parameters are analyzed in details.
- Balance bus bar current distribution is achieved, and the AC current distribution is experimentally verified.
- The voltage spike during switch turn-off transient is estimated under different current conditions based on the predicted bus bar stray inductance. The best estimation accuracy is 2.65%.

6.3 Future Work

According to the work included in this thesis, the following suggestions could be considered in the future.

- The MOSFET voltage rise- and fall-time estimation is still not accurate enough, especially when the load current is much lower than the rated current. The estimation model could be further investigated, such as the data extraction from the highly non-linear capacitance curve and the voltage level selection during the calculation.
- The input power and output power of the inverter are measured. Then, the inverter power loss is obtained by the difference between the inverter input and

output power, which is a simple method for the inverter power loss measurement and it is easy to be implemented. The power loss measurements could be further improved. If the junction and ambient temperature as well as the thermal resistance could be measured accurately, the power loss can be estimated by the temperature rise and the thermal resistance of the cooling system.

- The DC-link current and its ripple component are calculated by considering the inverter anti-parallel diode reverse recovery. This method is developed with the assumption that the load inductance is big and the DC-link current within the switching period is constant in each time interval. Nevertheless, if the current cannot be considered constant in each time interval during the switching period, the current rise needs to be taken into account. The calculations with the consideration of this current rise could be further investigated.

- Based on the analysis, the DC-link voltage ripple is influenced by the type of PWM techniques, which is not discussed in detail in this thesis. Thus it could be further studied.

- The bus bar current distribution is discussed and the AC current distribution is validated by experiments. However, the DC current distribution cannot be easily verified. The bus bar is designed with laminated structure, and the positive and negative conductors are integrated. Therefore, the solution to experimental verification of the DC current distribution on the bus bar could be further studied.

- Different shapes of the bus bar could be considered. The bus bar performances,

such as current distributions and parasitic parameters could be further investigated with various bus bar shapes.

- The PCB based bus bar design is not discussed in detail in this thesis, and the PCB design for the inverter A could be further analyzed and improved.

6.4 Thesis Publications

Journal papers

- J. Guo, J. Ye, and A. Emadi, "DC-link current and voltage analysis considering anti-parallel diode reverse recovery in voltage source inverters," *IEEE Transactions on Power Electronics* (Submitted).

- J. Guo, J. Ye, and A. Emadi, "Three-phase voltage source inverter design: a practical guidance," *IEEE Journal of Emerging and Selected Topics in Power Electronics* (Submitted).

- A. D. Callegaro, J. Guo, M. Eull, B. Danen, J. Gibson, M. Preindl, B. Bilgin, and A. Emadi, "Bus bar design for high-power inverters," *IEEE Transactions on Power Electronics* (Submitted).

Book chapters

- R. Hou, J. Guo, L. Dorn-Gomba, and A. Emadi, *Chapter 23: Power Electronics Systems and Control in Automobiles, in Control of Power Electronic Converters and Systems, Edited by F. Blaabjerg*, Amsterdam, Netherlands: Elsevier (To be published).

Conference papers

- J. Guo, H. Ge, J. Ye, and A. Emadi, "Improved method for MOSFET voltage rise-time and fall-time estimation in inverter switching loss calculation," In *Proc. IEEE Transportation Electrification Conference and Expo (ITEC)*, Dearborn, MI, June 2015, pp. 1-6.

- J. Guo and A. Emadi,"DC-link current ripple component RMS value estimation considering anti-parallel diode reverse recovery in voltage source inverters," In *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, September 2016, pp. 1-6.

- K. Yang, J. Guo, H. Ge, B. Bilgin, V. Loukanov, and A. Emadi, "Transient electro-thermal analysis for a MOSFET based traction inverter," In *Proc. IEEE Transportation Electrification Conference and Expo (ITEC)*, Dearborn, MI, June 2014, pp. 1-6.

- H. Ge, J. Guo, B. Bilgin, J. Ye, and A. Emadi, "A reduced-order model based induction machine self-commissioning method," In *Proc. IEEE Transportation Electrification Conference and Expo (ITEC)*, Dearborn, MI, June 2015, pp. 1-6.

Appendix A

Matlab Simulink Model for Inverter Instantaneous Power Loss

The power loss calculation model introduced in Chapter 2 is based on the average and RMS values of the inverter current and it is an average model. In order to understand the instantaneous power losses in the inverter, an example of MOSFET based simulation model is built in Matlab Simulink and it is shown in this chapter. According to the parameters given by the MOSFET datasheet, the switch, diode, and their power losses are modeled individually. The IGBT based model can be built similarly to the MOSFET based model and it will not be presented in detail here.

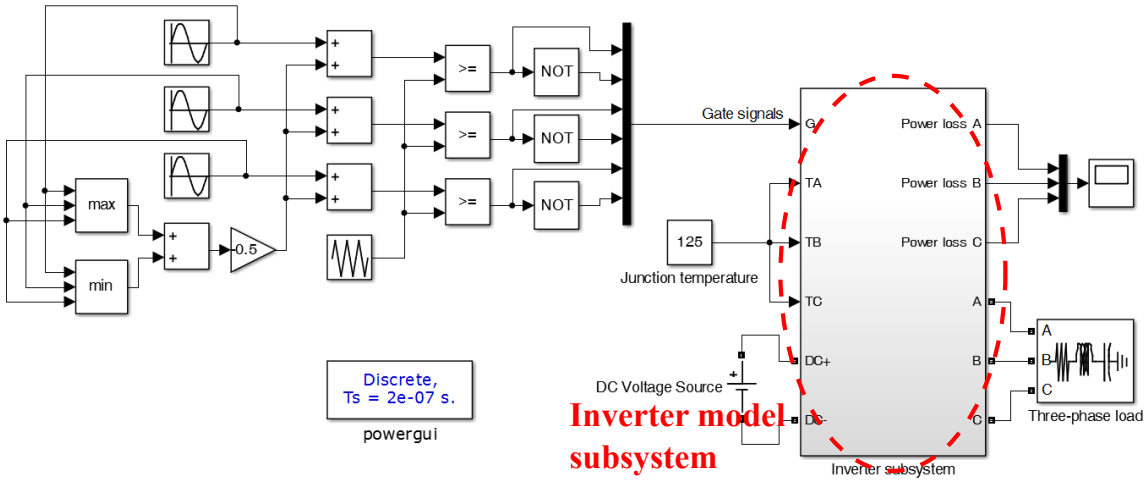


Figure A.1: Modeled inverter system with three-phase RLC load.

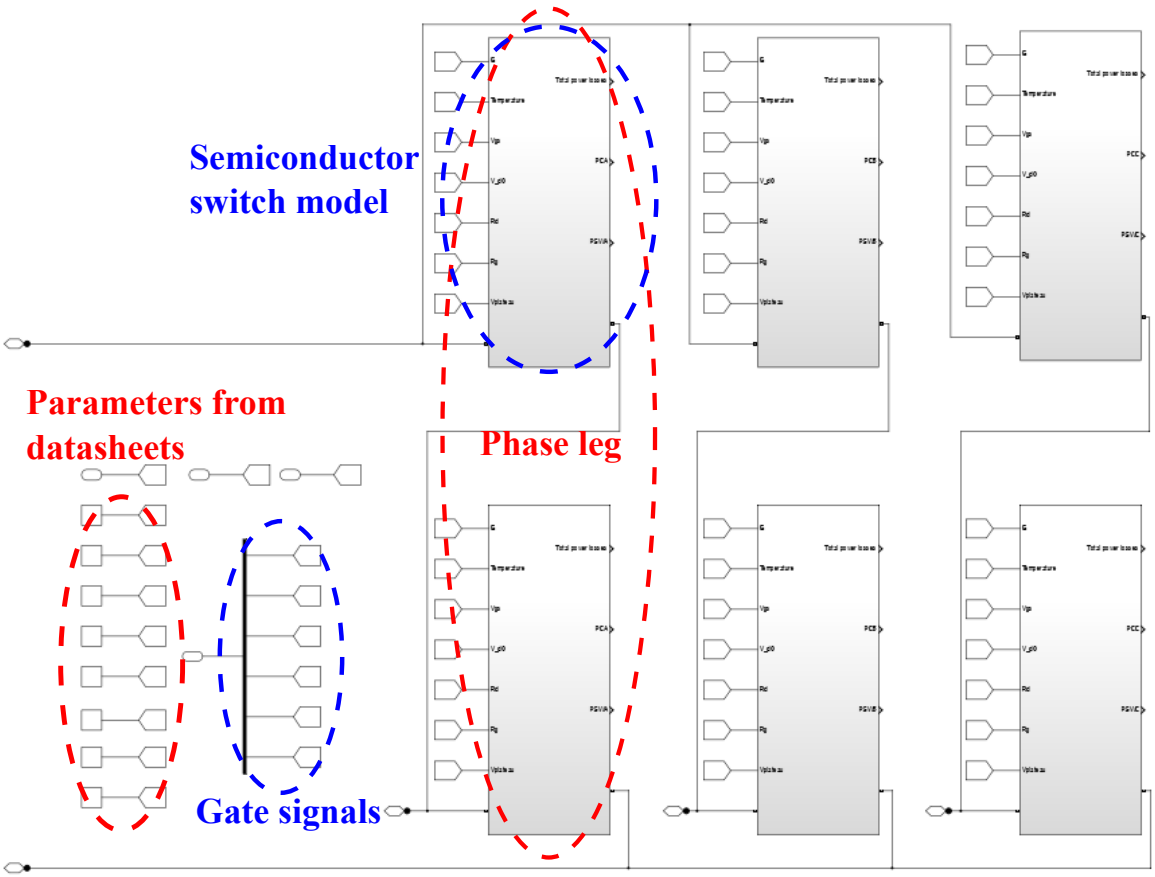


Figure A.2: Inverter model subsystem includes six individual semiconductor modules and power loss models.

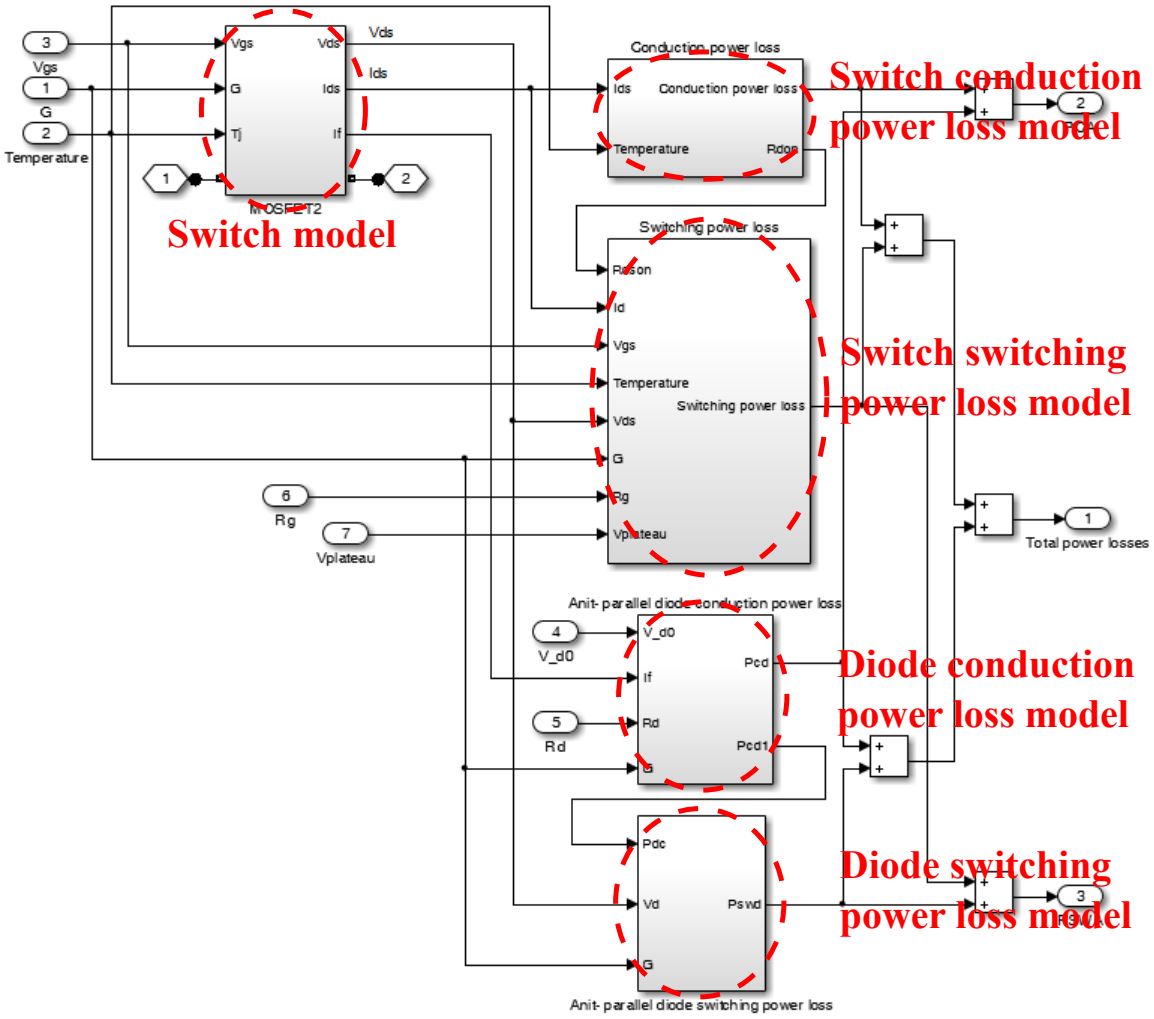


Figure A.3: Semiconductor switch model subsystem.

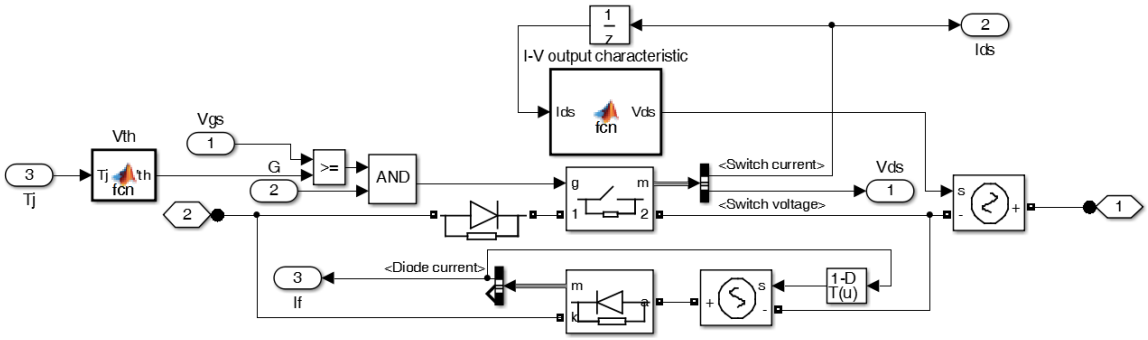


Figure A.4: MOSFET and diode models.

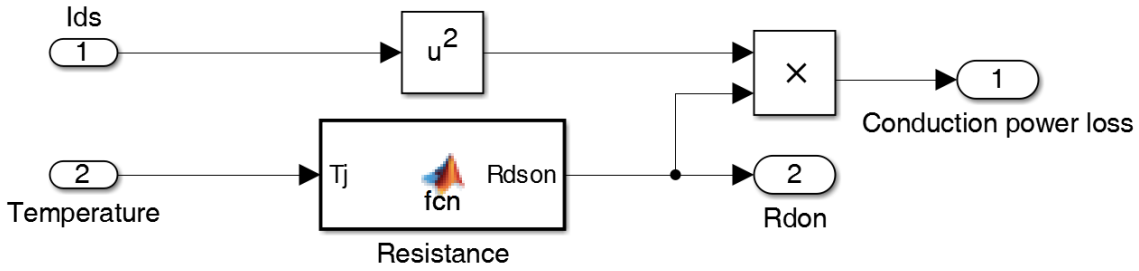


Figure A.5: MOSFET conduction power loss model.

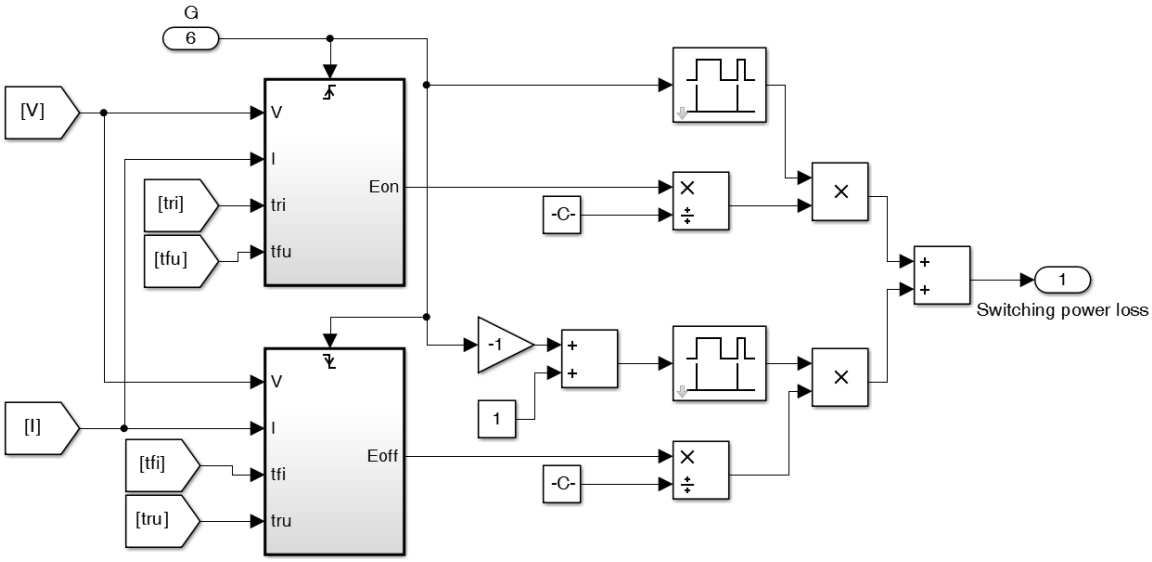


Figure A.6: MOSFET switching power loss model.

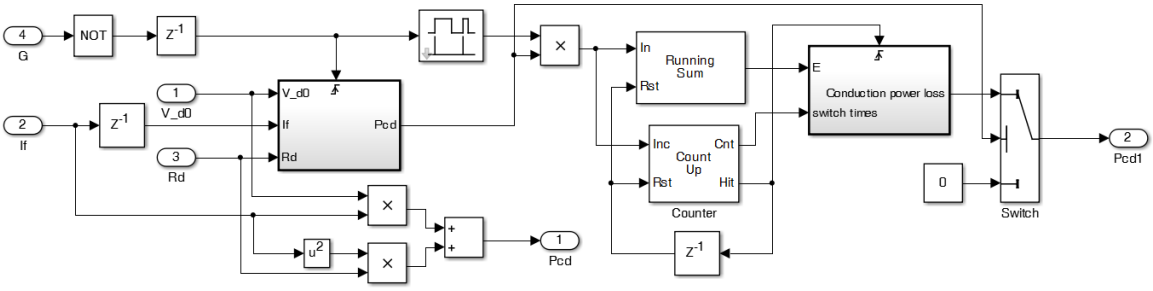


Figure A.7: Diode conduction power loss model.

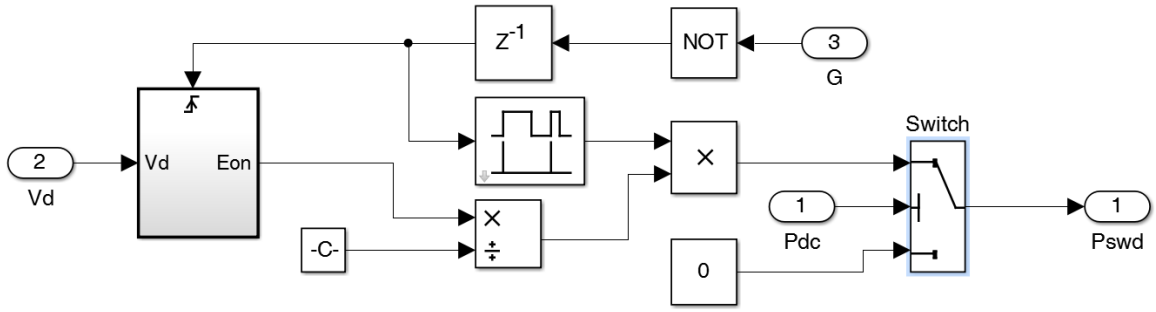


Figure A.8: Diode switching power loss model.

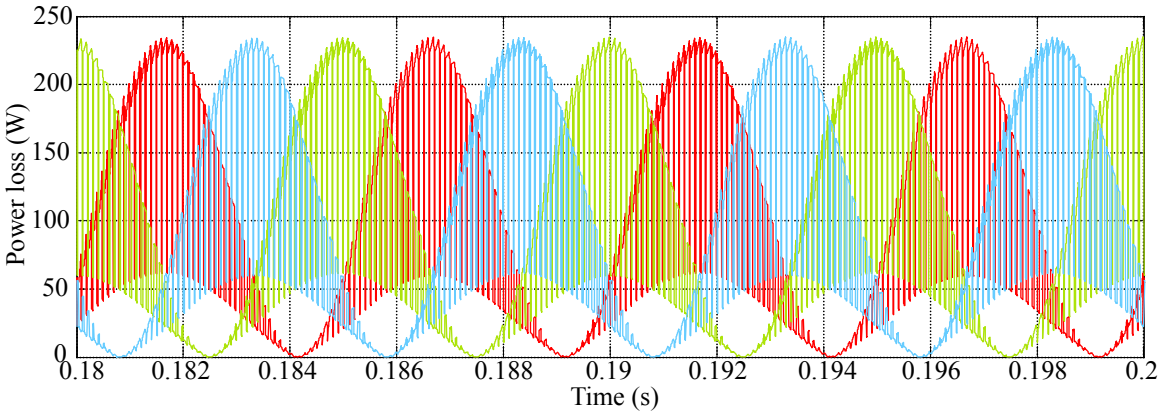


Figure A.9: Inverter three-phase conduction power loss.

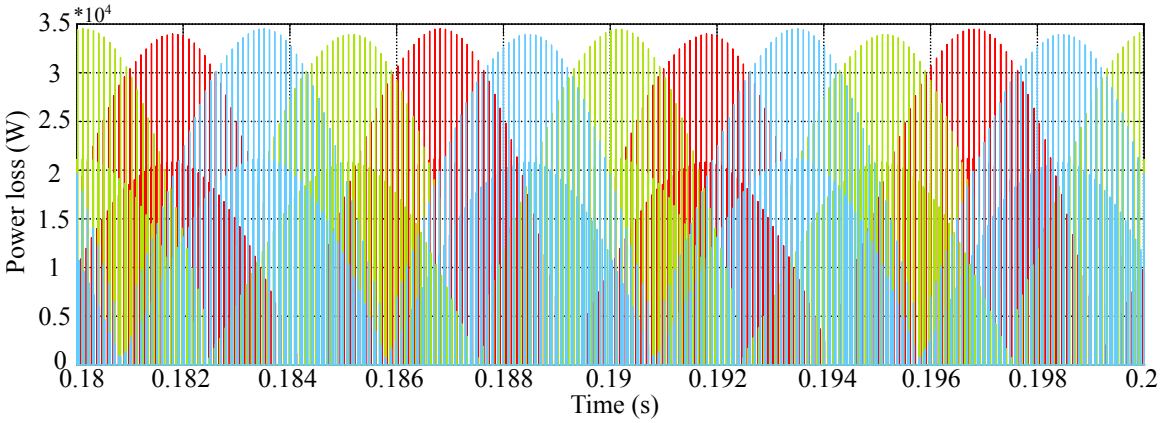
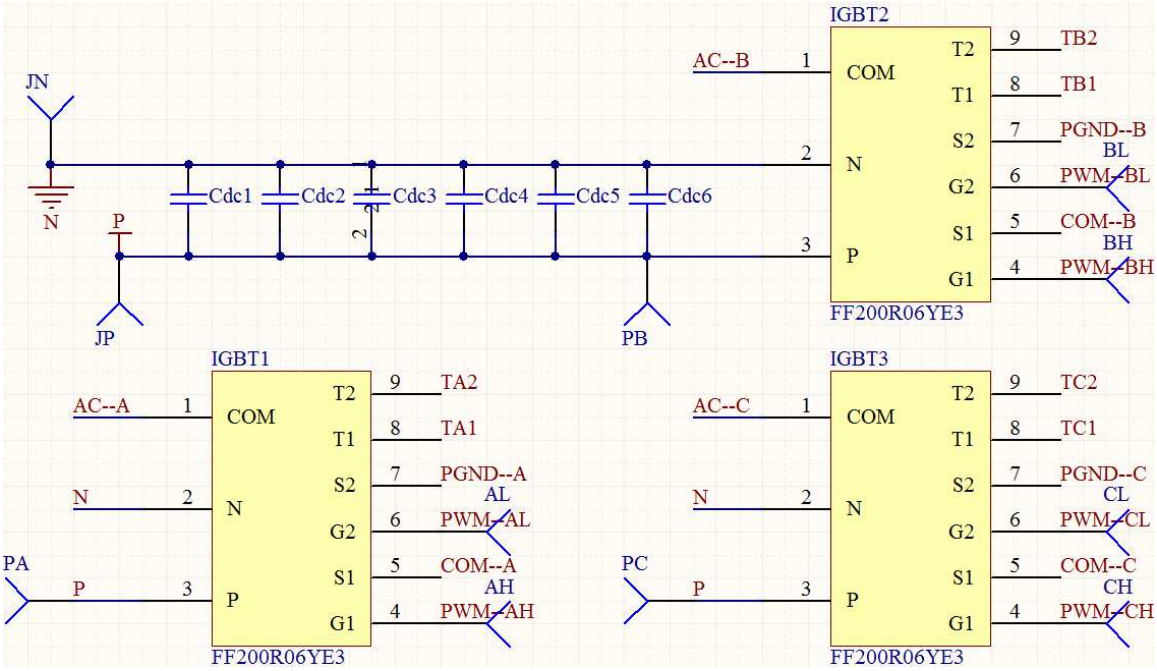


Figure A.10: Inverter three-phase switching power loss.

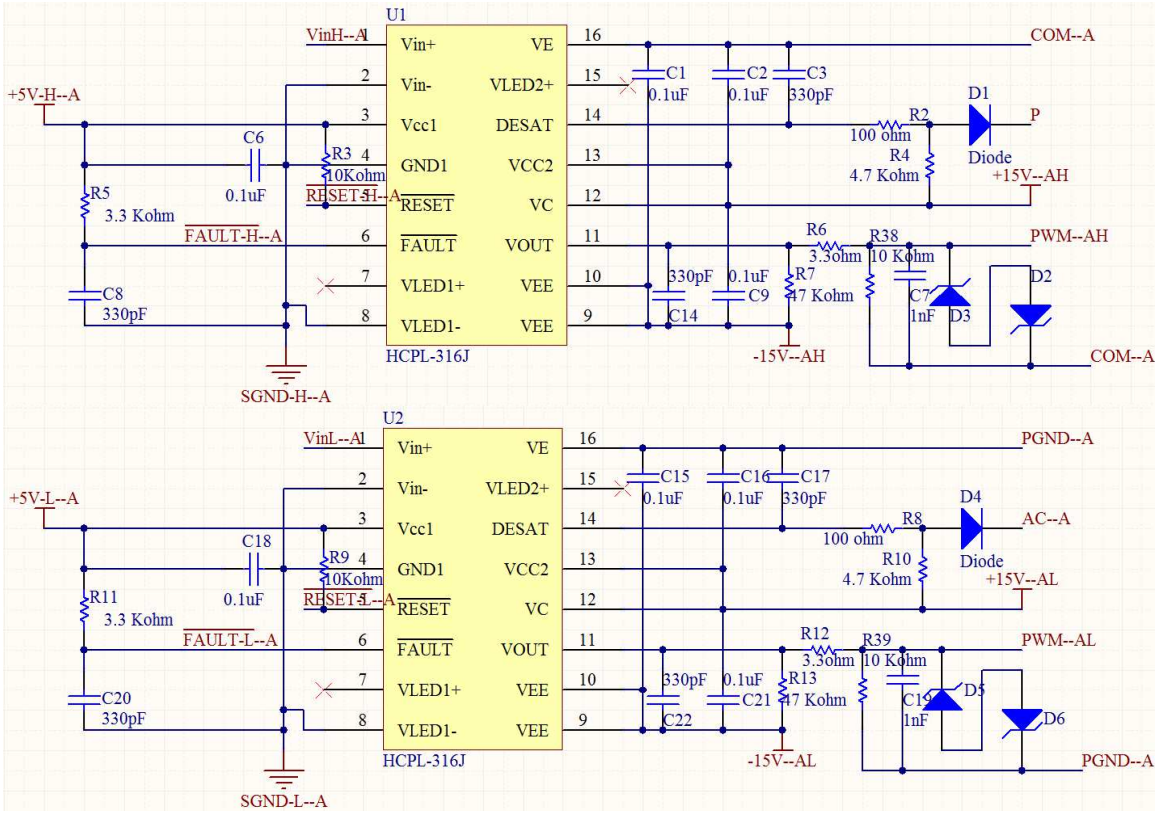
Appendix B

PCB Design for Inverter A

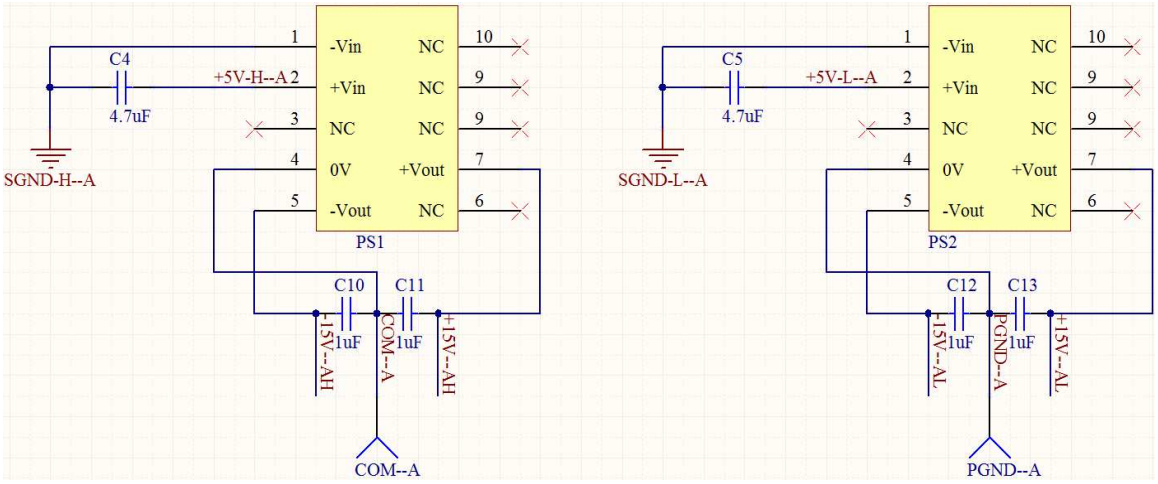
The schematic and PCB board designed for the inverter A are presented in this chapter.



(a) DC bus.



(b) Gate drivers for upper and lower switches.



(c) Power supplies for the gate drivers.

Figure B.1: Schematic drawings in Altium Designer.

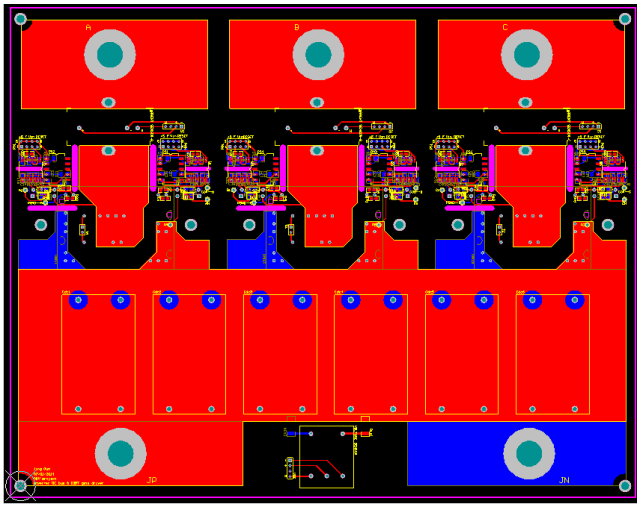
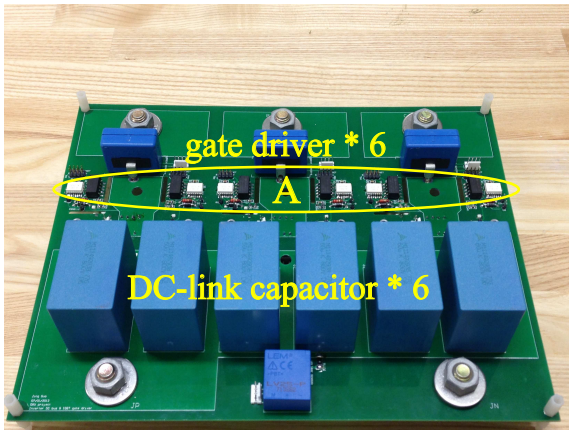
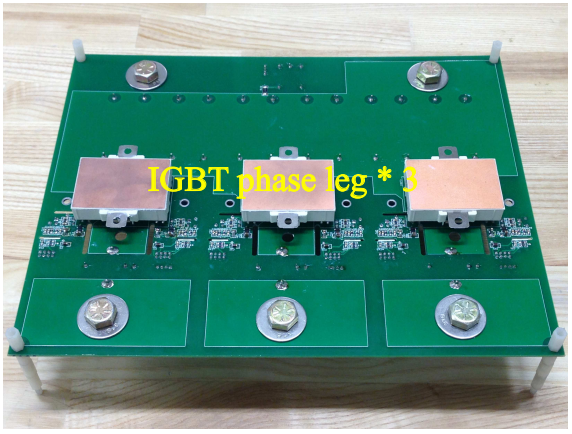


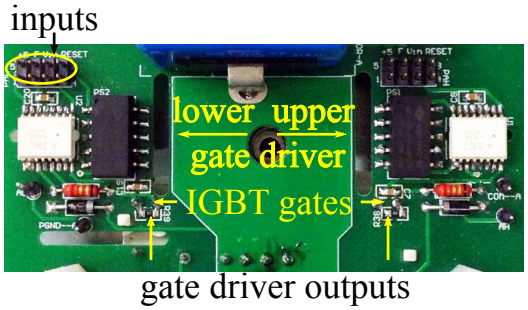
Figure B.2: PCB drawings in Altium Designer.



(a) Inverter A PCB design top view.



(b) Inverter A PCB design bottom view.



(c) Inverter A PCB design zoomed in view: IGBT gate drivers.

Figure B.3: Inverter A PCB design.

Appendix C

Experiment Set-Up

The experiment set-up is shown in Figure C.1.

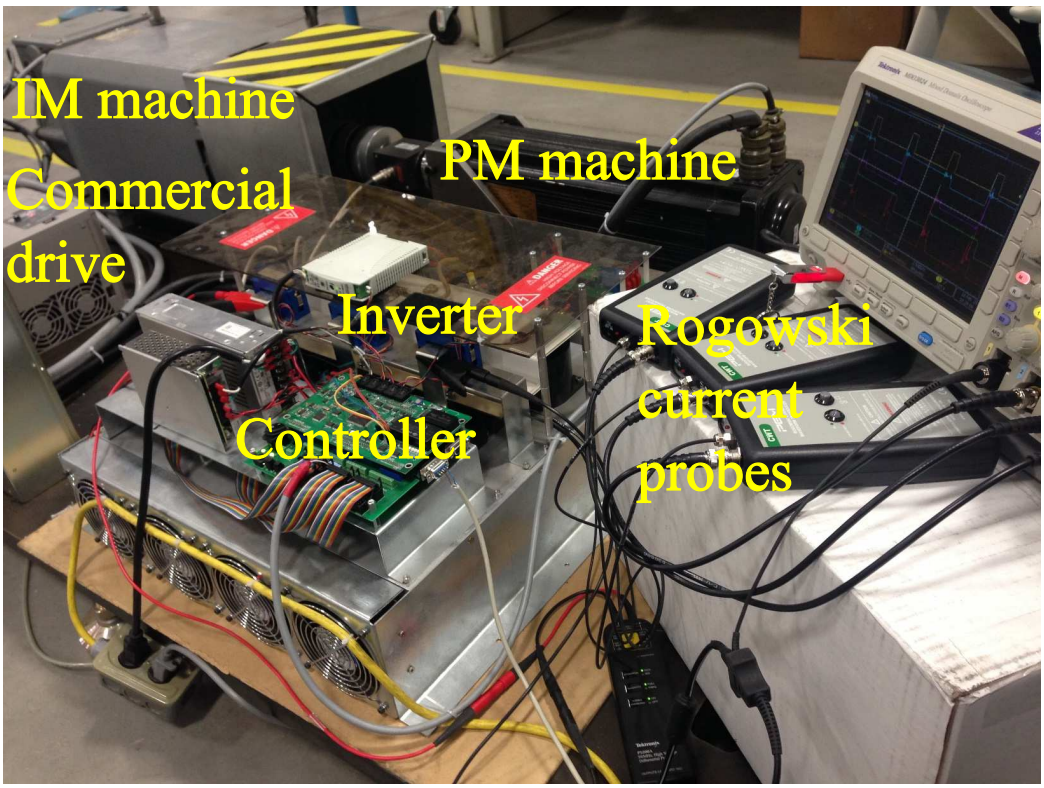


Figure C.1: Experiment set-up.

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