A CIRCUIT AND NOISE MODEL OF METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR

A CIRCUIT AND NOISE MODEL OF METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR

By

CHUAN-SUNG YEH, B.Sc.

A Thesis

Submitted to the Faculty of Graduate Studies

in Partial Fulfilment of the Requirements

for the Degree

MASTER OF ENGINEERING

McMaster University

May 1966

MASTER OF ENGINEERING (1966) McMASTER UNIVERSITY
(Electrical Engineering) Hamilton, Ontario

TITLE: A Circuit and Noise Model of Metal-Oxide-Semiconductor Field-Effect Transistor

AUTHOR: Chuan-sung Yeh, B.Sc. (Naval College of Technology, Taiwan China)

SUPERVISOR: Dr. S. H. Chisholm

NUMBER OF PAGES: vii, 90

SCOPE AND CONTENTS:

The Metal-Oxide Semiconductor Field-Effect Transistor is first analyzed from an active R-C transmission line view-point. The small signal circuit model and the noise model of the device are then derived and experimental results presented.

A Chronologically arranged bibliography concerning MOS devices and associated noise studies is included at the end of this thesis.

ACKNOWLEDGEMENTS

The author wishes to express his deep gratitude to Dr. S. H. Chisholm for his continuous encouragement and valuable advice during the course of this investigation. The author is particularly indebted to him for the time he spent, day and night during the preparation of this thesis. For a summer grant and most of the instruments which made this study possible, the author is grateful to the National Research Council of Canada.

The author is much obligated to Mr. Blythe Williams for his generous help in calibrating the Wayne Kerr Bridge B601, and Miss Joan Armour for her excellent typing of this manuscript.

The author's special thanks also go to his wife Jane, whose patience and understanding made this tedious work much easier to endure.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

CHAPTER I

Introduction

1.1 Introduction to the MOS FET

The Metal-Oxide-Semicondutor Field-Effect Transistor (MOS FET, also called Insulated Gate FET or Surface FET) is a new device working on an old field-effect Concept. In it an electric field is applied perpendicularly through an oxide to the semiconductor surface to modulate the conductance of the surface channel. Extremely high input impedance (of the order of 10^{15} ohms) and pentode like characteristics make it a potentially valuable small-signal device in the solid-state field.

The concept of the MOS Field-Effect-Transistor pre-dates the bipolar transistor. J. E. Lilienfeld[1] first observed the field-effect phenomenon in semiconductor materials in 1926, and attempted to invent an MOS FET, finally obtaining his patent in 1930. Unfortunately, due to the limited knowledge of solid-state and thin-film physics, little progress was made to turn it into a useful device. In 1948, Shockley and Pearson[2] re-examined the modulation of the surface charge in thin semiconductor films at Bell Telephone Laboratories. Their experiment failed to yield the predicted modulation results because of surface states problems. It was their study of the surface problems that led Bardeen and

Brattam to the discovery of bipolar transistors. In 1952, Shockley[3] by-passed the surface states problem and suggested the junction-gate field-effect transistor, in which the conducting channel was inside the semiconductor. However, the junction gate FET, using a reverse biased p-n junction as a control gate can only deplete the channel charge. If operated with the p-n junction forward biased to enhance the channel charge, a heavy current will result in the control gate circuit, which is undesirable. Thus the research work leading to the MOS FET continued. Then in 1960, Kahng and Atalla[4] proposed a Metal-Silicon Dioxide-silicon (MOS) structure in which the insulated metal gate was used to induce the conduction between two normally back-biased diodes. In 1961, Weimer[5] developed a cadmium sulphide (CdS) insulated gate thin film transistor using the evaporation method. In 1962 Hofstein and Heiman[6] described the insulated-gate construction for the MOS FETs. Since then, the increased understanding of semiconductor physics and the related advance of semiconductor technology has enabled the fabrication of MOS FETs with predictable performance.

Unlike the junction gate FET, the MOS FET has an insulated gate which allows the channel charge to be enhanced as well as depleted.

1.2 Summary of Contents

In this thesis, the MOS FET is first analyzed from an active R-C transmission line view-point. The small-signal circuit model and the noise model of the device are then derived, and experimental results presented.

The thesis is divided into four main parts. In Chapter II, the derivation of the theoretical device parameters together with the experimentally observed results are presented. In Chapter III, an analysis based on an active R-C transmission line approach yields a small-signal circuit model from which the Y parameters are derived, and measurements are found to agree with the theoretical model. In Chapter IV, noise-generating mechanisms, noise characterization and noise specification are first discussed, followed by a description of the various noise sources in MOS devices. A noise model of the MOS FET device is derived, then experimental results are compared with theoretically predicted values. In Chapter V, results of the thesis are summarized and discussed, and further studies are suggested.

CHAPTER II

Physical Theory of MOS Device

2.1 Basic Structure of the MOS FET

The schematic diagram of the experimental MOS FET structure is illustrated in Fig. 2.1 with biasing circuitry included. This is the so-called induced p-channel, enhancement - mode MOS FET.

Two heavily-doped p regions are diffused into a high resistivity n-typed substrate and a thin insulating layer of silicon dioxide (SiO_2) is thermally grown on the surface, the oxide thickness being of the order of 1000 Å generally. The metal gate electrode, and the source and drain electrodes which form the ohmic contacts, are made by evaporation and photoengraving techniques[7]. Generally, the substrate is passively connected to the source and just acts as a support. The conduction in the MOS FET takes place in an induced p layer on the substrate.

Fig. 2.2 is the IEEE circuit symbol for the device.

The source and drain regions are both of opposite semiconductor type from the substrate, and thus channel current is normally zero when the gate bias is zero. The gate is negatively biased so the electrons will be first depleted from the surface of the substrate. A further increase in gate bias will induce a p-type layer at the surface which produces an ohmic conduction path from source (p^+) through channel

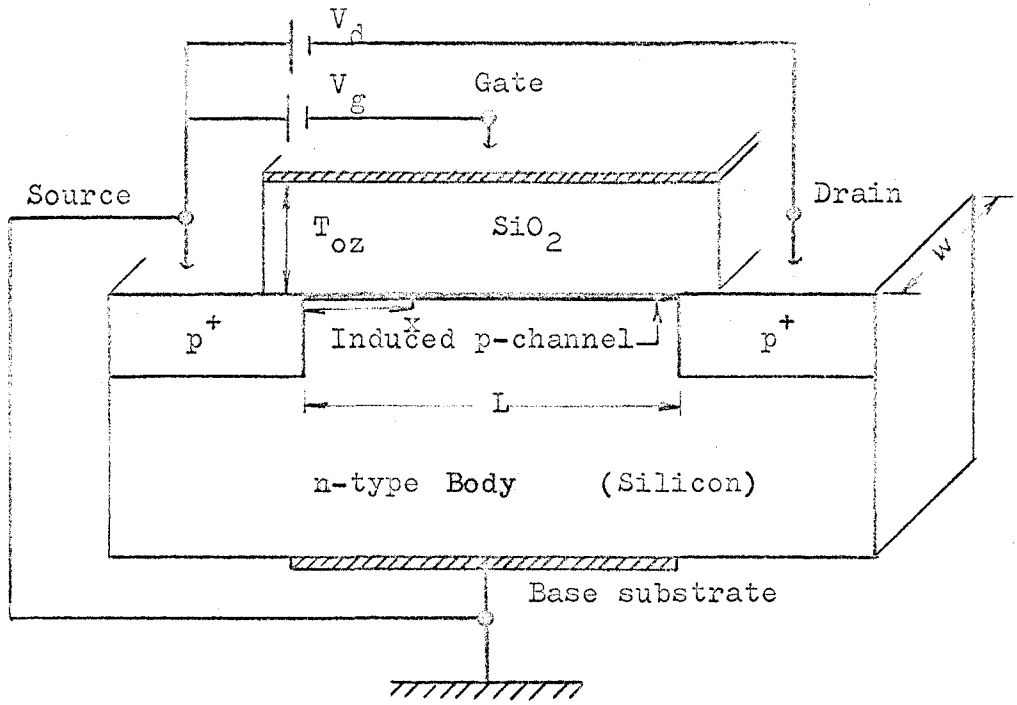


Fig. 2.1 Experimental MOS FET structure

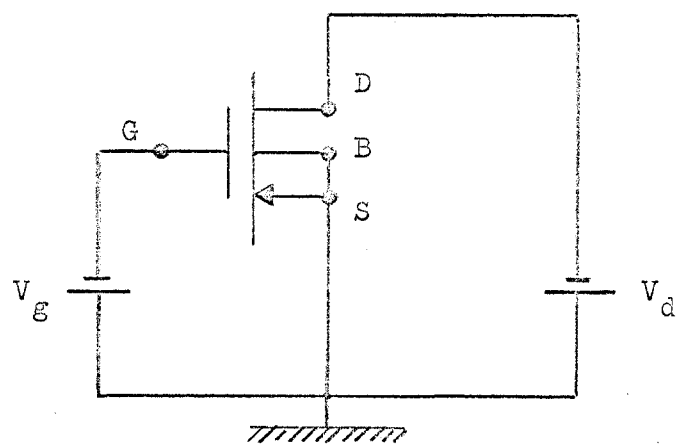


Fig. 2.2 IEEE circuit symbol of MOS FET

(induced p-type) to the drain. The gate bias voltage thus controls the conductivity of the device from source to drain.

2.2 Drain Characteristics of the MOS FET

2.2.1 Assumptions

The following theoretical analysis is based on two important assumptions, namely:

a) Gradual - channel assumption, proposed by Shockley[3]:

The influence of the gradient of the field along the channel on channel charge is neglected, i.e. the potential at X is determined by the charge at X and not by charges lying to either side of X, where X is a point along the channel.

b) The shallow-channel approximation:

The channel depth is much less than the oxide thickness, and thus the voltage drop across the channel is much less than that across the oxide, and may be neglected.

2.2.2 Drain Current I_d

Before deriving the voltage-current characteristics, a special term needs to be defined, viz. the pinch-off voltage (or threshold voltage, gate-onset voltage). The pinch-off voltage is defined[9] as the minimum gate voltage required to induce a surface channel and turn on the drain current.

Let the width of the device be W = 1, and

$\sigma(x)$ = surface channel conductance at point X. It is a function of V_g, V_p and $V(x)$

$V(x)$ = channel voltage at point X referred to the source

V_g = gate voltage

V_p = pinch-off voltage

T_{oz} = oxide thickness, then

$$\sigma(x) > 0 \text{ when } V_g - V(x) > V_p$$

$$\sigma(x) = 0 \text{ when } V_g - V(x) \leq V_p$$

utilizing the gradual-channel assumption, the channel current I at point X, will be

$$I(x) = \sigma(x)\, E(x) \text{ where}$$

$$E(x) = \frac{dV(x)}{dx}$$

Therefore,
$$I(x) = \sigma(x)\, \frac{dV(x)}{dx} \qquad (2\text{-}1)$$

Since the silicon dioxide layer is an insulator, the leakage current through the oxide is assumed negligible (if not, the device is considered as defective), and the channel current from the source to the drain is therefore a constant, thus

$$I_d = \int_o^{V_d} \frac{\sigma(x)\, dV(x)}{L} \quad \text{for } V_g - V_d > V_p \qquad (2\text{-}2)$$

where L = channel length

V_d = d.c. drain voltage

I_d = drain current

Let C_{oz} = gate capacitance per unit channel length (for device of unit width)

$\rho(x)$ = surface channel charge density at X

μ_o = carrier mobility

then
$$\rho(x) = C_{oz}\,[(V_g - V(x)) - V_p] \tag{2-3}$$

$$\sigma(x) = \mu_o\rho(x) = \mu_o C_{oz}[(V_g - V(x) - V_p] \tag{2-4}$$

substituting (2-4) into (2-2) gives

$$I_d = \frac{\mu_o C_{oz}}{L}\left[(V_g - V_p)V_d - \frac{V_d^2}{2}\right] \tag{2-5}$$

or

$$I_d = \frac{\mu_o C_{oz}}{L}\left[\frac{(V_g-V_p)^2 - (V_g-V_p-V_d)^2}{2}\right] \tag{2-6}$$

This drain characteristic is not valid for $(V_g-V_p) < V_d$, since under this condition the pinch off at drain electrode occurs, and the gradual-channel assumption is invalid.

When $(V_g-V_p) < V_d$, the drain current will be saturated and be limited to the value of

$$I_{ds} = \frac{\mu_o C_{oz}}{L}\,\frac{(V_g-V_p)^2}{2} \tag{2-7}$$

or

$$I_{ds} = \frac{\mu_o C_{oz}}{L}\,\frac{V_{ds}^2}{2} \tag{2-8}$$

where $V_{ds} = (V_g-V_p)$ is the drain saturation voltage.

The explanation is as follows: As (V_g-V_p) approaches V_d, the channel conductance is reduced, the ε field gradient along the channel becomes appreciable compared with that of the gate. The gradual-channel assumption is no longer valid, and space-charge dominated currents[10] are generated in the drain region of the channel. The drain current appears to saturate because the length of the space-charge region is generally much smaller than the overall channel length. The source region from the source to the point where space-charge begins is predominant in determining the drain current. Since this source region length is fairly constant and the voltage drop across it is fixed at (V_g-V_p), the current flow is essentially fixed. Further increase in drain voltage above (V_g-V_p) is absorbed across this drain region with only slight modification of the source region length.

In this analysis, Eq. (2-7) or (2-8) will be taken as the drain current beyond saturation.

2.2.3 Drain Conductance g_d

The drain conductance below saturation can be obtained from Eq. (2-5). By definition

$$g_d = \frac{\partial I_d}{\partial V_d}\Big|_{V_g} = \frac{\mu_o C_{oz}}{L}(V_g-V_p-V_d) \qquad (2\text{-}9)$$

It is a linear function of V_d, and will increase as V_d decreases. Theoretically, g_d will be zero at $V_d = V_g-V_p$ (i.e. at saturation). Actually g_d is finite in the saturation region due to invalidity of the gradual-channel assumption.

2.2.4 Transfer Conductance g_m

The transfer conductance is obtained by differentiating Eq. (2-5) with respect to V_g, thus

$$g_m = \frac{\partial I_d}{\partial V_g}\Big|_{V_d} = \frac{\mu_o C_{oz}}{L} V_d \tag{2-10}$$

The maximum g_m occurs at saturation

$$g_{ms} = g_{m(\text{saturation})} = \frac{\mu_o C_{oz}}{L} V_{ds}$$

$$= \frac{\mu_o C_{oz}}{L} (V_g - V_p) \tag{2-11}$$

2.2.5 Voltage Amplification Factor μ

The voltage amplification factor μ is defined by

$$\mu = -\frac{\partial V_d}{\partial V_g}\Big|_{I_d} = \frac{\dfrac{\partial I_d}{\partial V_g}}{\dfrac{\partial I_d}{\partial V_d}} = \frac{g_m}{g_d}$$

$$= \frac{V_d}{V_g - V_p - V_d} \tag{2-12}$$

Theoretically, μ will approach infinity as saturation is reached, i.e. when $V_g - V_p = V_d$, $g_d \to 0$. This does not occur since, as just pointed out, the drain conductance g_d is actually finite. Thus the voltage amplification factor at saturation is also finite.

2.3 D. C. Measurements

The experimental results of I_d vs V_d with V_g as parameter, and I_d vs V_g with V_d as parameter are shown in Fig. 2.3 and 2.4.

The calculated $\sqrt{I_{ds}}$ versus $(V_g - V_p)$ from experimental curves is shown as Fig. 2.5. The linear dependance of $\sqrt{I_{ds}}$ on the gate voltage V_g over a wide range of V_g is observed, which shows that the MOS FET has a square-law characteristic and is just as Eq. (2-7) predicted.

The departure from linearity at large gate voltage is due to the fact that when the gate voltage gets larger, the holes become more concentrated near the SiO_2 interface, and thus the channel holes suffer more surface scattering and the hole mobility decreases. In addition, an increase in temperature in the drain pinch off region reduces the mobility of holes, thus lowering $\sqrt{I_{ds}}$ for higher V_g values.

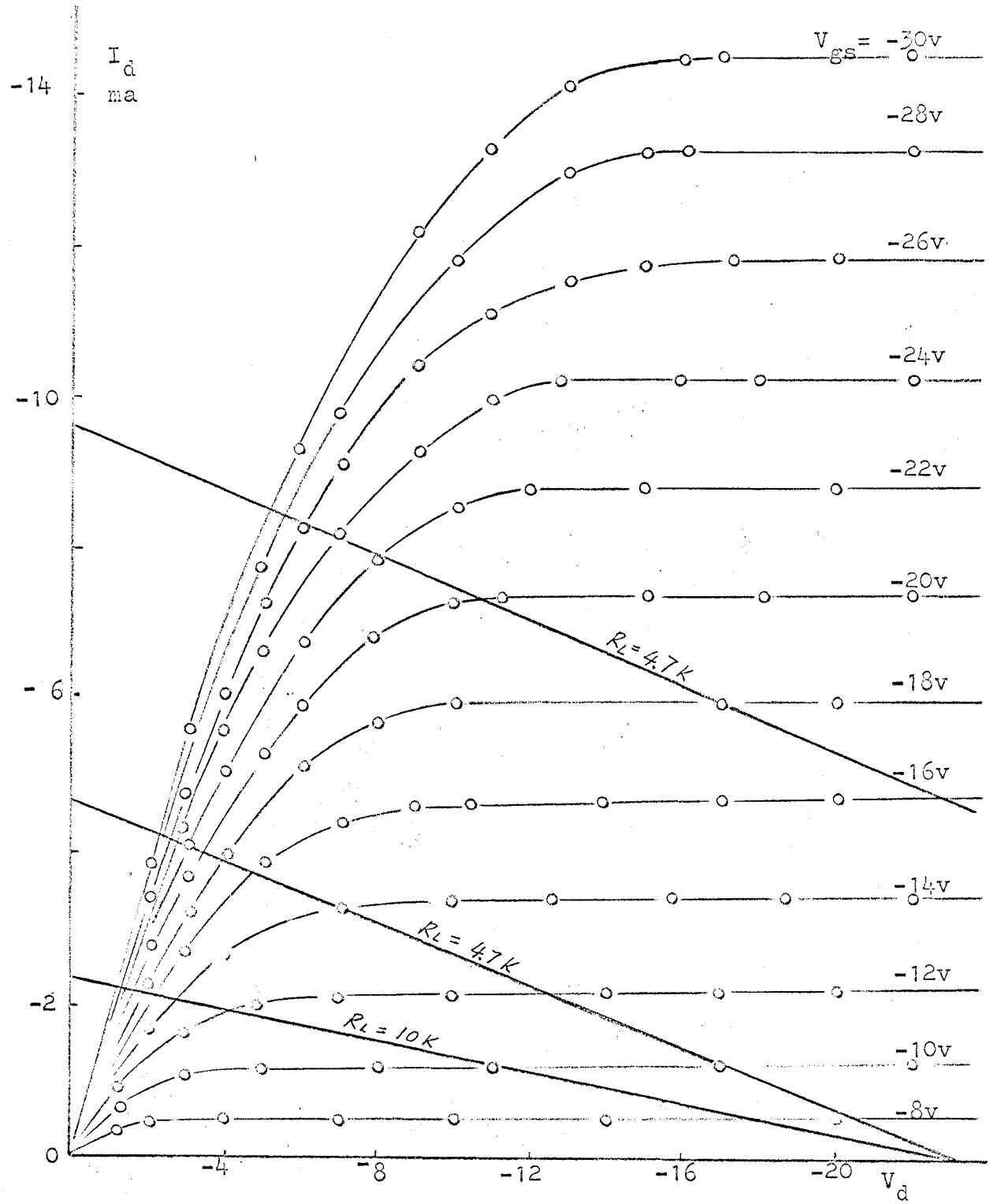


Fig. 2. 3 I_d versus V_d Characteristics

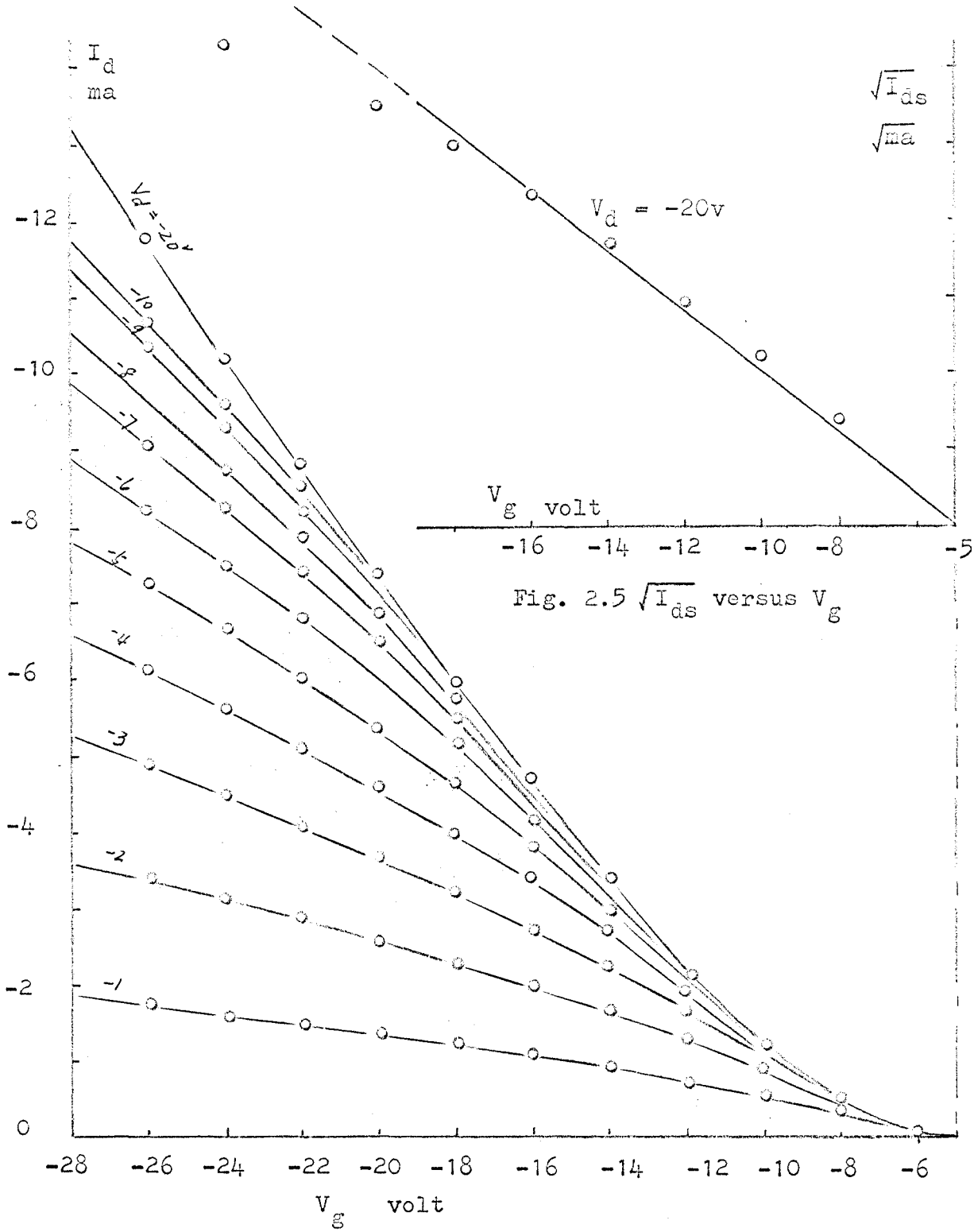


Fig. 2.5 $\sqrt{I_{ds}}$ versus V_g

Fig. 2.4 I_d versus V_g characteristics

CHAPTER III

The Circuit Model of MOS FET

This chapter begins with a transmission line approach to the derivation of the circuit model of MOS FET. A lumped approximation is then made to the distributed line and the Y parameters for the circuit model are derived. The experimental results are shown to agree with this circuit model.

3.1 The Transmission Line Approach

3.1.1 Physical Structure Consideration

To derive a realistic small-signal equivalent circuit is a necessity for thorough understanding of an electron device. Not only does it help for device small-signal applications, it also aids in the study of the noise of the device.

An ideal equivalent circuit should meet the following three requirements, it should:

1) associate itself directly with the physical structure of the device
2) match all the device parameter measurements
3) be reasonably simple and easy to use.

The device investigated in this thesis is physically a distributed one, and the distributed R-C transmission line model may be represented as in Fig. 3.1. The MOS FET is also an active device, its channel resistance being modulated by the gate voltage. For a small variation in gate signal, the channel resistance will be modulated by a corresponding amount. Thus the current flow in this channel will be modulated, and therefore a current generator is put in parallel with each of the small distributed sections to take the channel resistance modulation effect into account.

As far as the channel resistance modulation effect is concerned, the whole channel can be divided into three major regions. Region 1 extends from the source end up to the point where the channel voltage is V_a ($V_a < V_g - V_p$, see Fig. 3.2). This is the full-enhanced region where the channel resistance modulation effect is very small. This can also be seen from Fig. 3.2 where the I_d vs V_d characteristics in this section is nearly a straight line. Region 2 extends from the V_a point up to the point where the channel voltage equals $(V_g - V_p)$. This is a less-enhanced region where the channel resistance modulation has the most effect. The current flows in region 1 and region 2 are essentially ohmic. Region 3 extends from the $(V_g - V_p)$ point up to the drain, and is pinched off completely.

Region 1 represents the larger part of the channel but it only contributes a minor part of the whole channel resistance, since, as mentioned before, the modulation effect is very small and is therefore negligible. Region 2 contributes the major part to the modulated resistance.

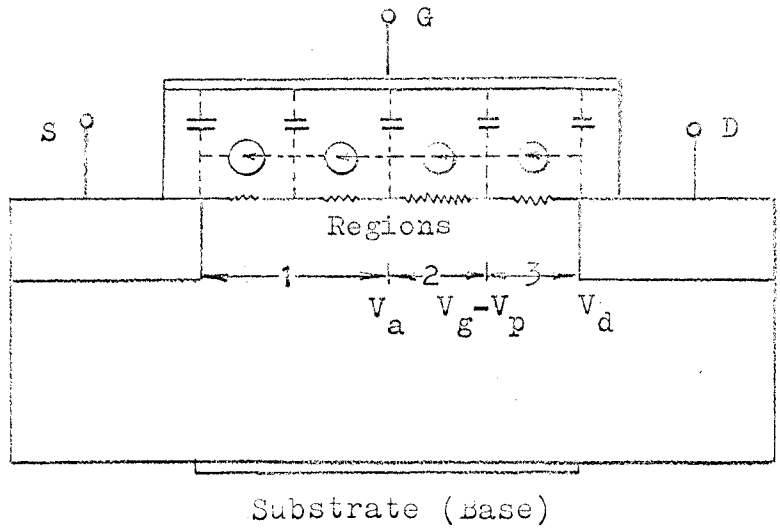


Fig. 3.1 An MOS FET cross-section view showing distributed R-C transmission line model

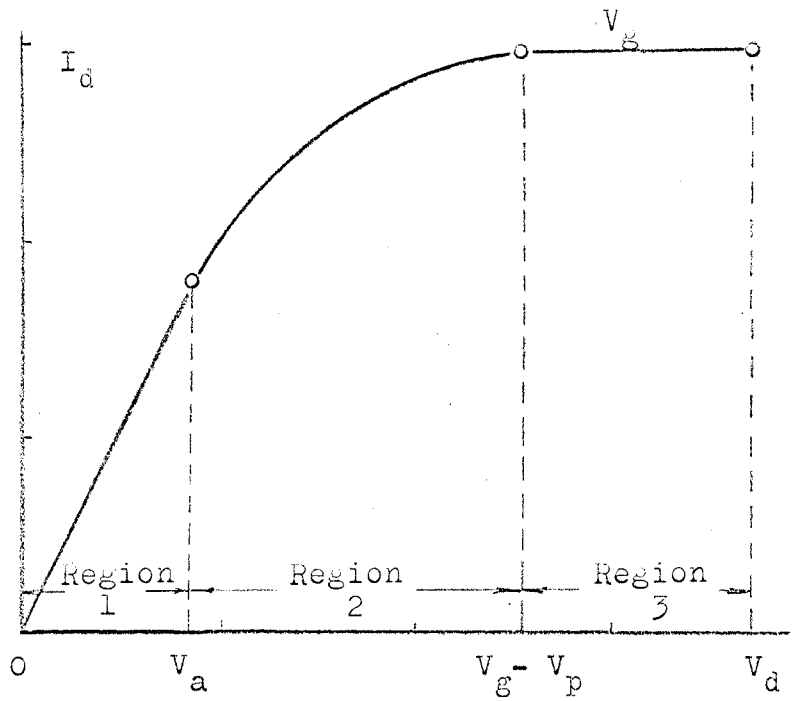


Fig. 3.2 Region Characteristics

Region 3 is only a small portion of the high resistance region near the drain end. Thus the distributed model may be simplified as shown in Fig. 3.3. The various elements in this circuit will be specified after the mathematical treatment which follows.

3.1.2 Mathematical Analysis

As discussed in section 2.2, the channel current I(x) at point X (assume the device width W = 1) is given by the following relationship:

$$I(x) = \sigma(x)\, E(x) = \sigma(x)\, \frac{dV(x)}{dx} \qquad (3\text{-}1)$$

To study the small-signal effects, let $\sigma(x)$ be modulated by the signal and thus it can be expanded into a Taylor series* about a d.c. potential v_o at X. If

$$V = v_o + v$$
$$I = i_o + i \qquad (3\text{-}2)$$

where

v_o, i_o = d.c. components of voltage and current in surface channel

v, i = small a.c. components of voltage and current in surface channel

Since $\sigma_x(V)$ is a function of V, and $V = v_o + v$

$$\sigma_x(V) = \sigma_x(v_o + v) = \sigma(v_o) + \frac{d\sigma(v_o)}{dV} v(x) + \frac{1}{2!} \frac{d^2\sigma(v_o)}{dV}\, v^2(x) + \ldots \qquad (3\text{-}3)$$

---

* Extension of Bechtel's series expansion approach, Tech.Rep. No. 1612-1, Stanford Electronics Lab., April, 1963

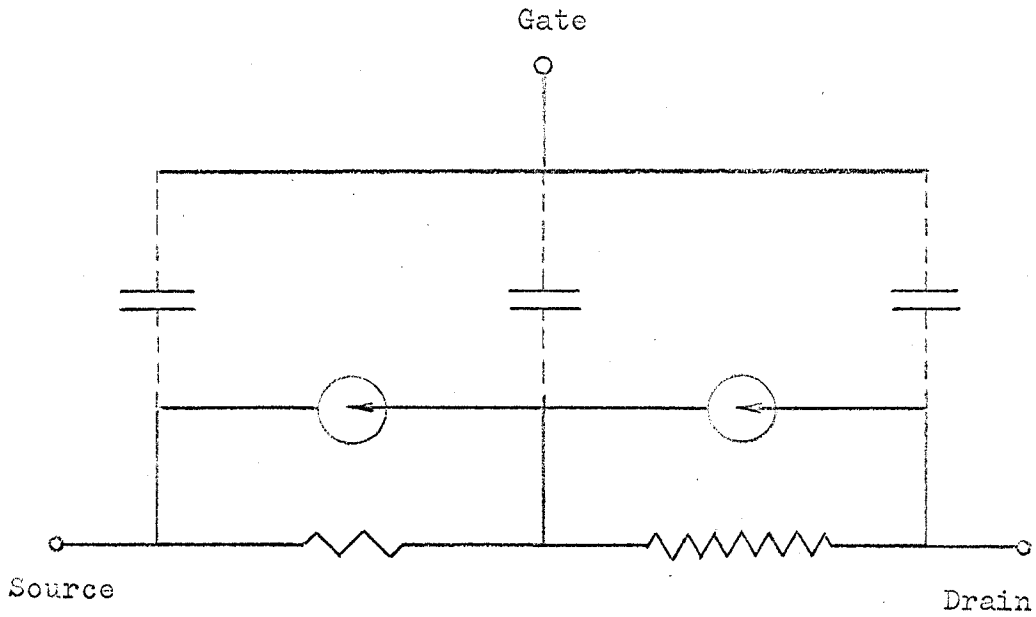


Fig. 3.3 Simplified R-C Transmission Line Circuit Model

where the subscript x of σ on the right-hand side is dropped out.

From Eq. (2-4), it can be seen that σ(x) is a first order function of V(x), therefore, the first two terms will be sufficient to specify $\sigma_x(V)$. Then from Eq. (3-1),

$$I(x) = \left[\sigma(v_o) + \frac{d\sigma(v_o)}{dV}\, v(x)\right] \frac{dV}{dx} \tag{3-4}$$

let $I(x) = I_{o,x} + i_x$

then $$I(x) = I_{o,x} + i_x = \left[\sigma(v_o) + \frac{d\sigma(v_o)}{dV}\, v(x)\right] \frac{dV}{dx}$$

$$= \sigma(v_o) \frac{d(v_o + v)}{dx} + \frac{d\sigma(v_o)}{dV}\, v(x) \frac{d(v_o + v)}{dx} \tag{3-6}$$

Separating the d.c. and a.c. terms, one obtains

1) d.c. part:

$$I_{o,x} = \sigma(v_o) \frac{dv_o}{dx} \tag{3-7}$$

which has the same form as Eq. (3-1)

2) a.c. part:

$$i_x = \sigma(v_o) \frac{dv}{dx} + \frac{d\sigma(v_o)}{dV} \frac{dv_o}{dx}\, v(x) + \frac{d\sigma(v_o)}{dV}\, v(x) \frac{dv}{dx} \tag{3-8}$$

Eq. (3-8) can be simplified somewhat by neglecting the second order term and recognizing that

$$\frac{d\sigma(v_o)}{dV} \frac{dv_o}{dx} = \frac{d\sigma(v_o)}{dx} \tag{3-9}$$

Then the a.c. part of the surface channel current is

$$i_x = \sigma_x(v_o) \frac{dv}{dx} + \frac{d\sigma_x(v_o)}{dx}\, v$$

$$= \frac{d}{dx} \left[v\sigma_x(v_o)\right] \tag{3-10}$$

This is the small-signal mathematical relationship for the channel current i_x, channel voltage v and the channel conductance σ, for a small channel element dx at point X along the channel in the MOS FET.

3.2 The Circuit Model

From the mathematical analysis above, it can be seen from Eq. (3-10) that the current in one section Δx of the channel is combined of two portions:

1) $\frac{\sigma}{\Delta x}\Delta v$, which is proportional to the voltage drop Δv across the section Δx,

2) $\frac{\Delta\sigma}{\Delta x} v$, which is proportional to the voltage at the end of the section.

Thus, from the mathematical analysis, the distributed circuit model of Fig. (3.2) can be thought of as a combination of two such sections as shown in Fig. 3.4.

As discussed in section 3.1, the channel resistance modulation effect in the section near the source end is very small and is assumed negligible. Thus, Fig. 3.4 can be simplified as shown in Fig. 3.5 for a common-source configuration, where

$$g_2 = \frac{\Delta\sigma_2}{\Delta x_2} \tag{3-12}$$

$$R_1 = \left(\frac{\sigma_1}{\Delta x_1}\right)^{-1} \tag{3-13}$$

$$R_2 = \left(\frac{\sigma_2}{\Delta x_2}\right)^{-1} \tag{3-14}$$

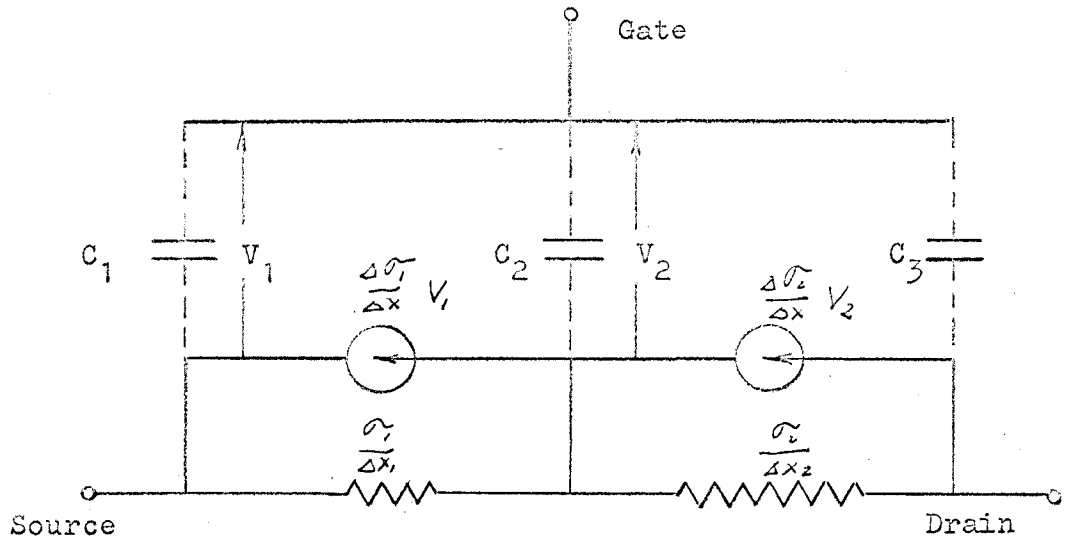


Fig. 3.4 Transmission Line Circuit Model From Mathmatical Analysis

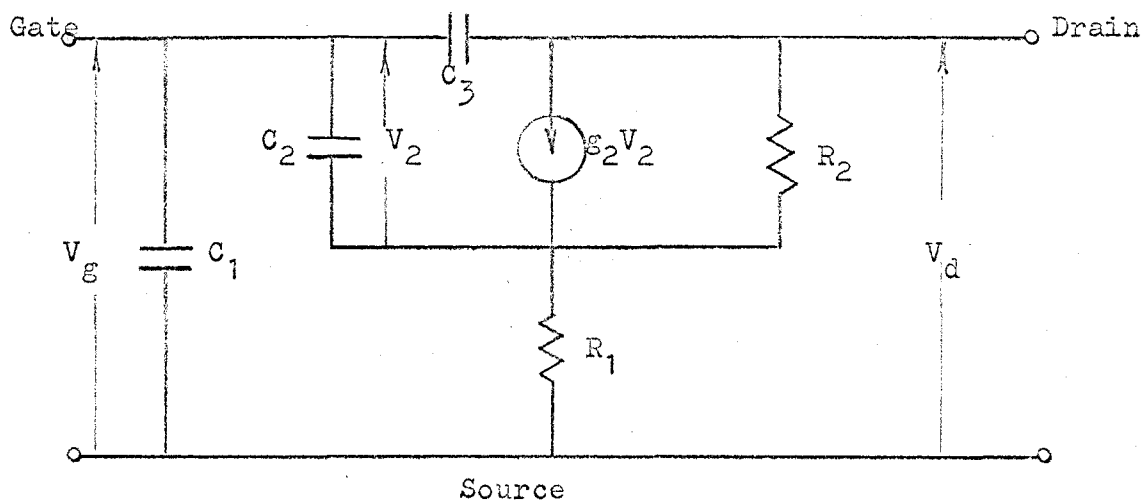


Fig. 3.5 Circuit Model in Commom-Source Configuration

3.2.1 The Small-Signal Y-parameter Derivation

Since the MOS FET is a 4-terminal (2-port) device, its Y-parameters can be found from the following equations for common-source configuration.

$$I_g = Y_{11}V_g + Y_{12}V_d \tag{3-15}$$

$$I_d = Y_{21}V_g + Y_{22}V_d \tag{3-16}$$

From Fig. 3.5, it can be calculated that

$$Y_{11} = \frac{\partial I_g}{\partial V_g}\Big|_{V_d=0}$$

$$= j\omega(C_1+C_3) + j\omega C_2 \left[\frac{1 + \frac{R_1}{R_2}}{(1+\frac{R_1}{R_2} + R_1g_2) + j\omega R_1C_2}\right] \tag{3-17}$$

$$Y_{12} = \frac{\partial I_g}{\partial V_d}\Big|_{V_g=0}$$

$$= -j\omega C_3 \left[1 + \frac{\frac{R_1C_2}{R_2C_3}}{(1 + \frac{R_1}{R_2} + R_1g_2) + j\omega R_1C_2}\right] \tag{3-18}$$

$$Y_{21} = \frac{\partial I_d}{\partial V_g}\Big|_{V_d=0}$$

$$= g_2 \left[\frac{1 - j\omega \frac{R_1C_2}{R_2g_2}}{(1 + \frac{R_1}{R_2} + R_1g_2) + j\omega R_1C_2}\right] - j\omega C_3 \tag{3-19}$$

$$Y_{22} = \frac{\partial I_d}{\partial V_d} \Big|_{V_{g=0}}$$

$$= \frac{1}{R_2} \left[\frac{1 + j\omega R_1 C_2}{(1 + \frac{R_1}{R_2} + R_1 g_2) + j\omega R_1 C_2} \right] + j\omega C_3 \qquad (3\text{-}20)$$

At very low frequencies, $Y_{22} \approx g_d$ (from Eq. 2-9 and 3-20), $Y_{21} \approx g_m$ (from Eq. 2-10 and 3-19). One also sees that the gate charging and discharging time constants (essentially R_1C_2 from Fig. 3.5) determine the high frequency cut-off of the device. This cut-off frequency may be approximated as $\omega_C \approx \frac{1}{R_1 C_2}$ (ω_C will be defined later). Therefore, at very low frequencies, i.e. $\omega << \frac{1}{R_1 C_2}$, accordingly $\omega << \frac{1 + \frac{R_1}{R_2} + R_1 g_2}{C_2 R_1}$ and Eq. (3-17) through Eq. (3-20) can be reduced to

$$Y_{11} \approx j\omega(C_1 + C_3) + j\omega C_2 \left[\frac{1 + \frac{R_1}{R_2}}{1 + \frac{R_1}{R_2} + g_2 R_1} \right] \qquad (3\text{-}21)$$

$$Y_{12} \approx -j\omega C_3 \left[1 + \frac{\frac{R_1 C_2}{R_2 C_3}}{1 + \frac{R_1}{R_2} + g_2 R_1} \right] \qquad (3\text{-}22)$$

$$Y_{21} \approx \frac{g_2}{1 + \frac{R_1}{R_2} + R_1 g_2} \approx g_m \qquad (3\text{-}23)$$

$$Y_{22} \approx \frac{1}{R_2} \cdot \frac{1}{1 + \frac{R_1}{R_2} + g_2 R_1} \approx g_d \qquad (3\text{-}24)$$

The following relationships are found for simplifying the Y-parameters. Let

$$g_o = g_m + g_d \tag{3-25}$$

Then, from Eq. (2-9) and (2-10),

$$g_o = g_m + g_d = \frac{\mu_o C_{oz}}{L} (V_g - V_p) \tag{3-26}$$

and from Eq. (3-23) and (3-24), one finds

$$g_o = \frac{g_2 + \frac{1}{R_2}}{1 + \frac{R_1}{R_2} + R_1 g_2} \tag{3-27}$$

i.e.

$$g_o \left(1 + \frac{R_1}{R_2} + R_1 g_2 \right) = g_2 + \frac{1}{R_2} + \frac{1}{R_1} - \frac{1}{R_1}$$

$$R_1 g_o \left(1 + \frac{R_1}{R_2} + R_1 g_2\right) = R_1 \left(g_2 + \frac{1}{R_2} + \frac{1}{R_1}\right) - 1 = \left(1 + \frac{R_1}{R_2} + R_1 g_2\right) - 1$$

$$1 + \frac{R_1}{R_2} + g_2 R_1 = \frac{1}{1 - g_o R_1} \tag{3-28}$$

Since the circuit model of Fig. 3.4 is assumed to be composed of two sections, and if L is the overall channel length from source to drain, then one may assume that the section near the souce end has a length KL, where K lies between 0 and 1, thus one may relate the channel section length KL to its channel resistance R_1 as:

$$R_1 = \frac{KL}{1/2 \left[\sigma(o) + \sigma(KL)\right]} \approx \frac{KL}{\sigma(o)} \tag{3-29}$$

From Eq. (2-3)

$$\sigma(o) = \mu_o C_{oz} (Vg - V_p) \tag{3-30}$$

i.e.
$$\frac{\sigma(o)}{L} = \frac{\mu_o C_{oz}}{L} (V_g - V_p)$$

$$= g_m + g_d = g_o, \text{ (by 3-26)} \tag{3-31}$$

Combining Eq. (3-29) and (3-31) yields

$$R_1 = \frac{K}{g_o} \tag{3-32}$$

and Eq. (3-28) may be put in terms of K, i.e.

$$1 + \frac{R_1}{R_2} + R_1 g_2 = \frac{1}{1-K} \tag{3-33}$$

From the Y-parameter equations (Eq. 3-17, through 3-20), it is found convenient to define a cut-off frequency ω_C as

$$\omega_C = \frac{1 + \frac{R_1}{R_2} + R_1 g_2}{R_1 C_2} \tag{3-34}$$

which is justified later* and thus Eq. (3-17) through (3-20) may be simplified as follows:

$$Y_{11} = j\omega[C_1 + C_3 + \frac{C_2(1-K)}{1 + j\frac{\omega}{\omega_c}} (1 + \frac{K}{g_o} \frac{g_d}{1-K})] \tag{3-35}$$

$$Y_{12} = - j\omega[C_3 + \frac{\frac{K}{g_o} C_2 g_d}{1 + j\frac{\omega}{\omega_c}}] \tag{3-36}$$

---

* from Eq. (3-41), one finds that g_m will drop to 1/2 gm when ω reaches ω_C.

$$Y_{21} = \frac{g_m}{1 + j\frac{\omega}{\omega_c}} \left(1 - j\frac{\omega}{\omega_c} \frac{1}{(1-K)\mu}\right) - j\omega C_3 \qquad (3\text{-}37)$$

$$Y_{22} = \frac{g_d}{1 + j\frac{\omega}{\omega_c}} \left[1 + j\frac{\omega}{\omega_c} \frac{1}{(1-K)}\right] + j\omega C_3 \qquad (3\text{-}38)$$

As mentioned in section 2.2, the maximum transconductance, g_{ms}, occurs at saturation and the theoretical voltage amplification factor μ will approach infinity, i.e. $g_d \to 0$, and $\mu >> 1$. Then, under saturation conditions, the Y-parameters given by Eq. (3-35) through (3-38) may be further simplified and separated into real and imaginary parts as follows:

From Eq. (3-35)

$$Y_{11} \approx j\omega\left[C_1 + C_3 + \frac{C_2(1-K)}{1 + j\frac{\omega}{\omega_c}}\right]$$

$$= \frac{\omega C_2 \left(\frac{\omega}{\omega_c}\right)(1-K)}{1 + \left(\frac{\omega}{\omega_c}\right)^2} + j\omega\left[C_1 + C_3 + \frac{C_2(1-K)}{1 + \left(\frac{\omega}{\omega_c}\right)^2}\right]$$

$$\approx \frac{\frac{g_m}{K}\left(\frac{\omega}{\omega_c}\right)^2}{1 + \left(\frac{\omega}{\omega_c}\right)^2} + j\omega\left[C_1 + C_3 + \frac{C_2(1-K)}{1 + \left(\frac{\omega}{\omega_c}\right)^2}\right] \qquad (3\text{-}39)$$

From Eq. (3-37)

$$Y_{12} \approx - j\omega C_3 \qquad (3\text{-}40)$$

From Eq. (3-37)

$$Y_{21} = \frac{g_m}{1 + (\frac{\omega}{\omega_c})^2} - j\omega[C_3 + \frac{(\frac{g_m}{\omega_c})}{1 + (\frac{\omega}{\omega_c})^2}] \qquad (3\text{-}41)$$

From Eq. (3-38)

$$Y_{22} = \frac{g_d}{1 + (\frac{\omega}{\omega_c})^2} [1 + \frac{1}{1-K} (\frac{\omega}{\omega_c})^2]$$

$$+ j\omega[C_3 + \frac{g_d}{1 + (\frac{\omega}{\omega_c})^2} (\frac{1}{\omega_c}) (\frac{K}{1-K})] \qquad (3\text{-}42)$$

3.2.2 The Circuit Model

From the Y-parameters derived, Fig. 3.5 can be transformed into a π-model. From Lo, et al[11], a one-generator π equivalent circuit for small-signal, linear, active four-terminal (2-port) device can be formed as shown in Fig. 3.6. Various elements can be found as shown in Fig. 3.7 for relatively high frequencies (i.e. $\omega < \omega_c$) and in Fig. 3.8 for low frequencies (i.e. $\omega << \omega_c$).

To operate at high frequencies (but $\omega < \omega_c$) and at saturation, the following Y- parameters are obtained from Eq. (3-39) to (3-42):

$$Y_{11} = \frac{g_m}{K} (\frac{\omega}{\omega_c})^2 + j\omega[C_1 + (1-K) C_2 + C_3]$$

$$= \frac{g_m}{K} (\frac{\omega}{\omega_c})^2 + j\omega(C_{gs} + C_{gd}) \qquad (3\text{-}43)$$

$$Y_{12} = - j\omega C_3 = - j\omega C_{gd} \qquad (3\text{-}44)$$

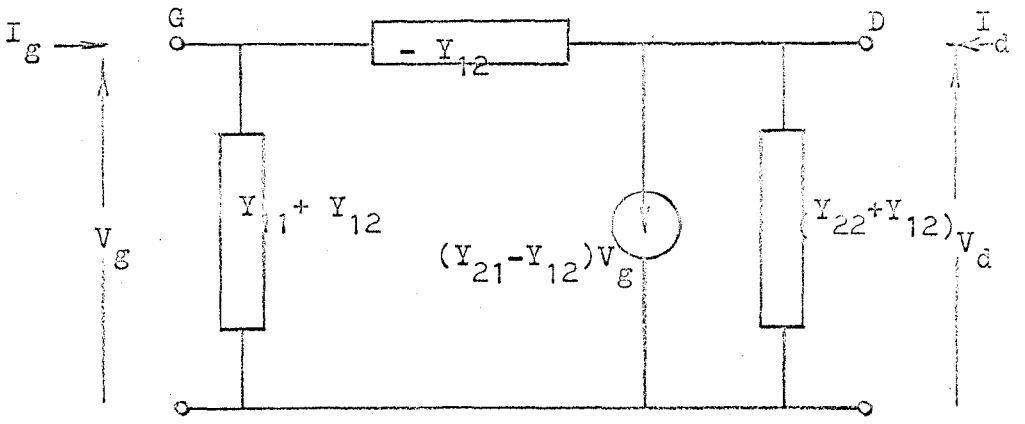


Fig. 3.6 A π-Model in Y-Parameter

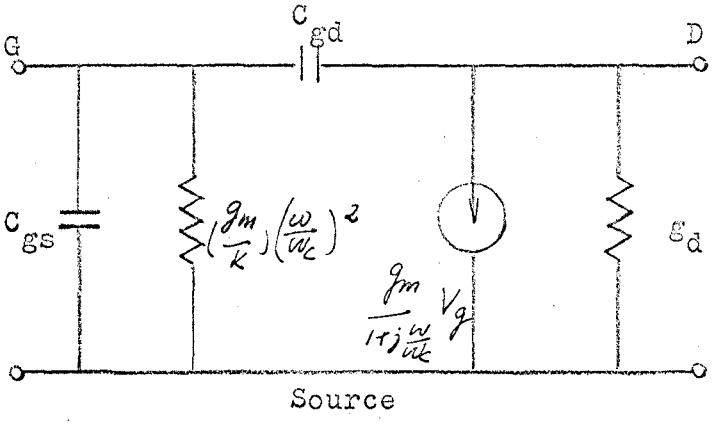


Fig. 3.7 Circuit Model for High Frequencies

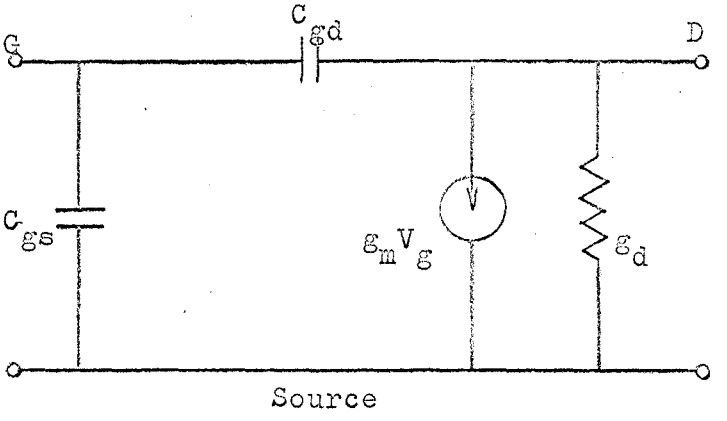


Fig. 3.8 Circuit Model at Low Frequencies

$$Y_{21} \approx \frac{g_m}{1 + j\frac{\omega}{\omega_c}} - j\omega C_{gd} \tag{3-45}$$

$$Y_{22} \approx g_d + j\omega C_{gd} \tag{3-46}$$

where $C_{gs} = C_1 + (1-K)\, C_2$

$C_{gd} = C_3$

For low frequency operation, $\omega << \omega_c$ then

$$Y_{11} \approx j\omega(C_{gs} + C_{gd}) \tag{3-47}$$

$$Y_{12} \approx -j\omega C_{gd} \tag{3-48}$$

$$Y_{21} \approx g_m - j\omega C_{gd} \tag{3-49}$$

$$Y_{22} \approx g_d + j\omega C_{gd} \tag{3-50}$$

The low-frequency circuit model obtained for the MOS FET which is shown in Fig. 3.8 agrees with the device equivalent circuit suggested by Sah[9]. This is the circuit model of the intrinsic device. If the lumped capacitances between the external electrode leads are added, it also agrees with the circuit model given by the manufacturer[12].

3.3 Experimental Results

3.3.1 Methods of Measurement

Y-parameter measurements were made on the Wayne Kerr bridge B601 (a transformer ratio-arm bridge, having a measuring frequency range of 15 KH_z to 5 MH_z) which can measure transfer admittance as well as driving-point admittance. The principles used are as follows:

a) The driving-point admittance (Y_{11} or Y_{22}). The schematic diagram for this admittance measurement is shown in Fig. 3.9.

Since the input transformer T_1 is closely coupled to the secondary windings, there will develop equal and opposite voltages between the neutral point N and the secondary terminals. When Y_s (standard admittance) is adjusted to give a null indication in the detector output, the bridge is at balance, and the value of unknown Y_x is equal to Y_s.

b) The transfer admittance (Y_{12} or Y_{21})

The most important property of this transformer ratio-arm bridge is that its leakage impedance across coils is sufficiently low and thus an unbalanced load across the secondary does not significantly alter the equality of voltages across the two halves of secondary coil. This quality makes the transfer admittance measurements possible. The schematic diagram for the transfer admittance measurement is shown in Fig. 3.10.

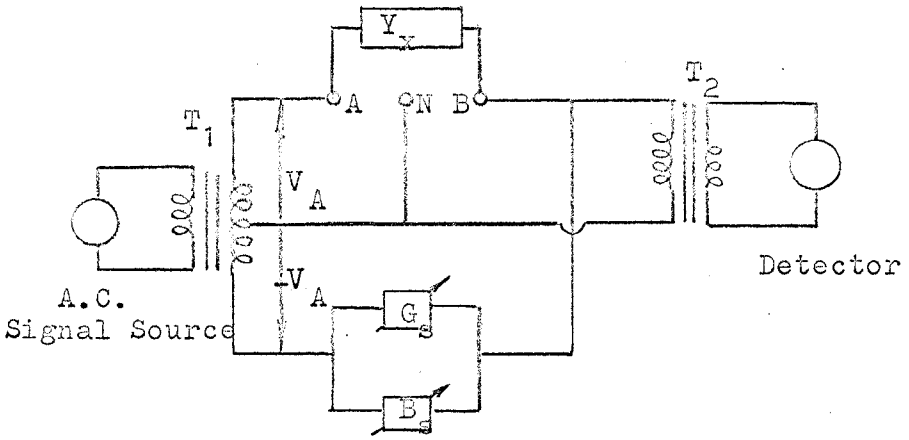


Fig. 3.9 Driving-Point AdmittanceMasurement

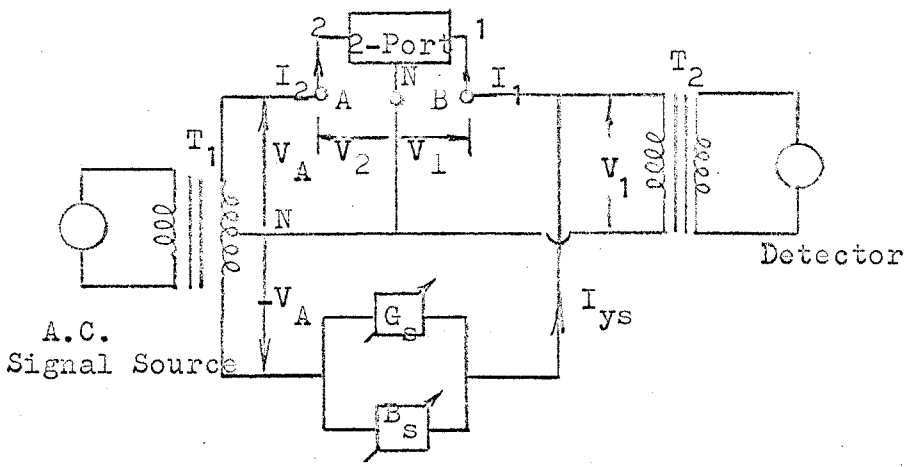


Fig. 3.10 Transfer Admittance Measurement

(i) Y_{12}: The Y-parameter equations are

$$I_1 = Y_{11} V_1 + Y_{12} V_2 \tag{3-51a}$$

$$I_2 = Y_{21} V_1 + Y_{22} V_2 \tag{3-51b}$$

where V_1 and V_2 are the voltages across the input and output terminals of the device respectively.

When the bridge is balanced by adjusting the standard admittance Y_s, $V_1 = 0$, and therefore $I_1 = I_{Y_s}$. It is then obvious from Fig. 3.10 that

$$I_{Y_s} = - V_A (G_s + jB_s) \tag{3-52}$$

From Eq. (3-51a) since $V_1 = 0$

$$I_1 = Y_{12} V_2 = Y_{12} V_A \tag{3-53}$$

combining Eq. (3-52) and (3-53) will give

$$Y_{12}(\text{unknown}) = - (G_s + jB_s) \tag{3-54}$$

(ii) Y_{21}: To measure Y_{21}, the principles involved are the same except that the input terminals 1-N and the output terminals 2-N connections are exchanged.

3.3.2 Comparison of the Measured and the Calculated Y-parameters.

To justify the circuit model derived in Fig. 3.8, the ideal method is to find the theoretical values of various elements such as

C_{gs}, C_{gd}, g_m and $_{gd}$ (Fig 3.8), which requires a knowledge of C_1, C_2 C_3, g_2, R_1 and R_2 (Fig. 3.5). These latter values are associated with the device physical materials and geometry which are unfortunately not available. Thus an alternate approach to check the validity of the circuit model can be adopted as follows:

From the low frequency Y-parameters equations (Eq. 3-47 through 3-50)

$$\begin{aligned} Y_{11} &= j\omega(C_{gs} + C_{gd}) \\ Y_{12} &= -j\omega C_{gd} \\ Y_{21} &= g_m - j\omega C_{gd} \\ Y_{22} &= g_d + j\omega C_{gd} \end{aligned} \tag{3-55}$$

where

$$\begin{aligned} C_{gd} &= \frac{-Y_{12i}}{\omega} = \frac{-Y_{21i}}{\omega} \\ C_{gs} &= \frac{Y_{11i}}{\omega} - C_{gd} \\ g_m &= Y_{21_\gamma} \\ g_d &= Y_{22_\gamma} \end{aligned} \tag{3-56}$$

where subscripts i and γ stand for imaginary and real parts respectively. Thus all these elements can be determined by a set of four measurements at a certain frequency (say 1 MH_z). If the theoretically-derived circuit model can represent the real device, then the Y-parameters calculated at different frequencies using this set of measured quantities, should fit with the actual measurements.

The calculated curves of the low frequency Y-parameters are plotted as solid lines in Fig. 3.11 to 3.14 with dots as the measured values. There is good agreement between the calculated and the measured Y-parameters at least from 15KH$_z$ to 5MH$_z$ (B601 range). Thus we may conclude that the theoretically derived circuit model matches fairly well with the real device and can be used to represent the real device at least in the test frequency range.

Since these Y-parameters should be measured under the actual operating bias condition, four adaptors were designed and built for these needs. The detailed adapter circuits are given in Appendix A.

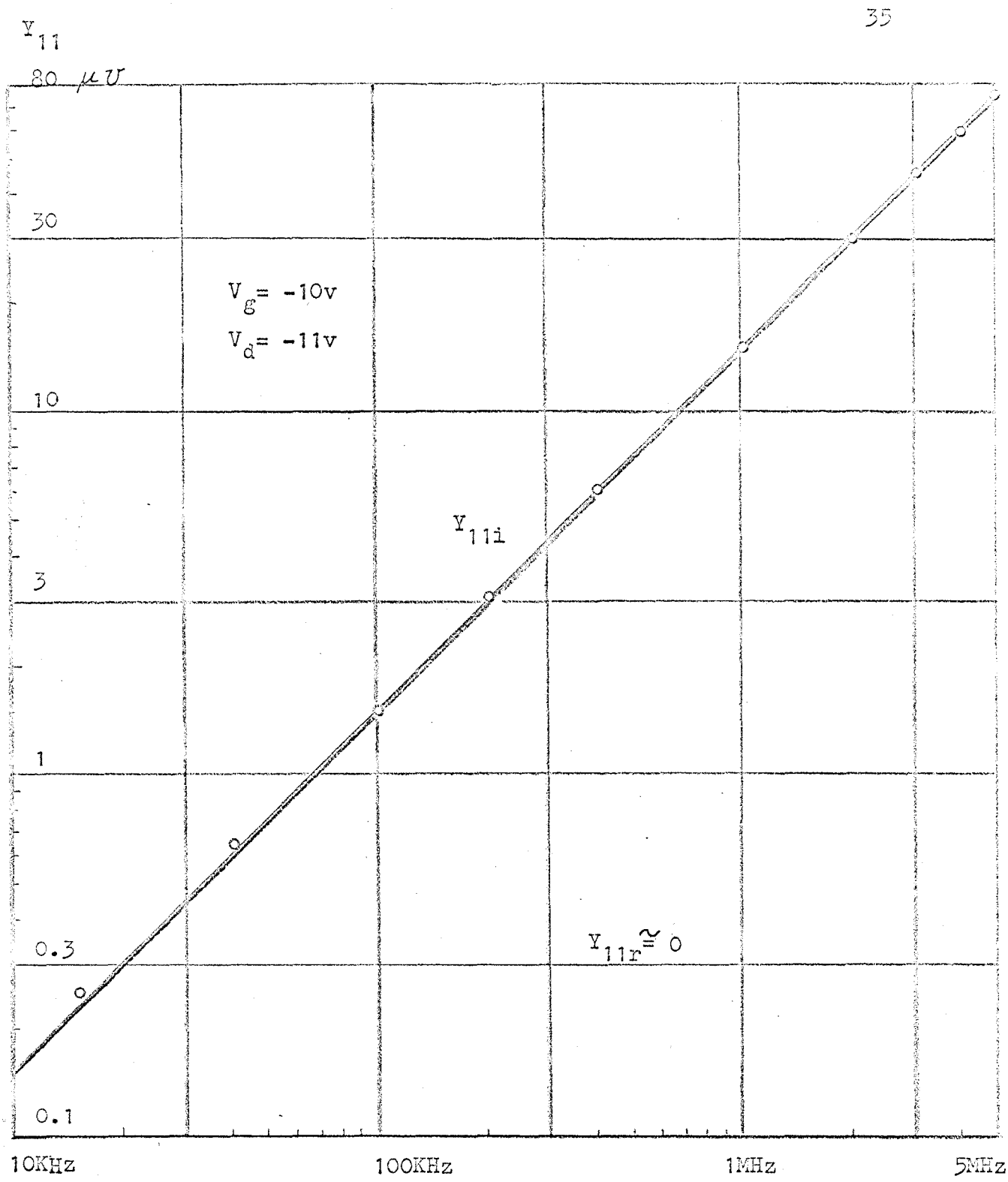


Fig. 3.11 Y_{11} Parameter Measurement Result

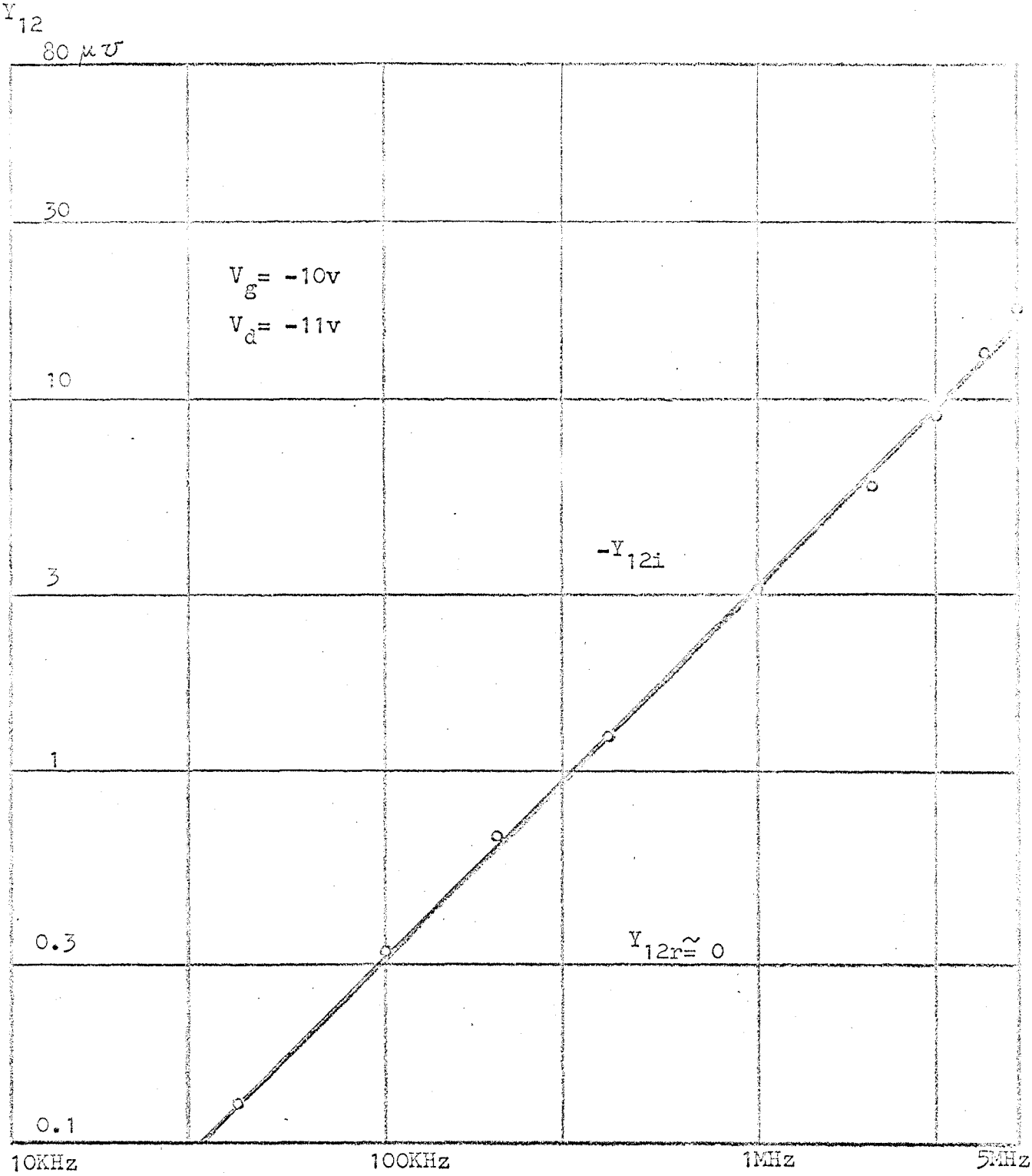


Fig. 3.12 Y_{12} Parameter Measurement Result

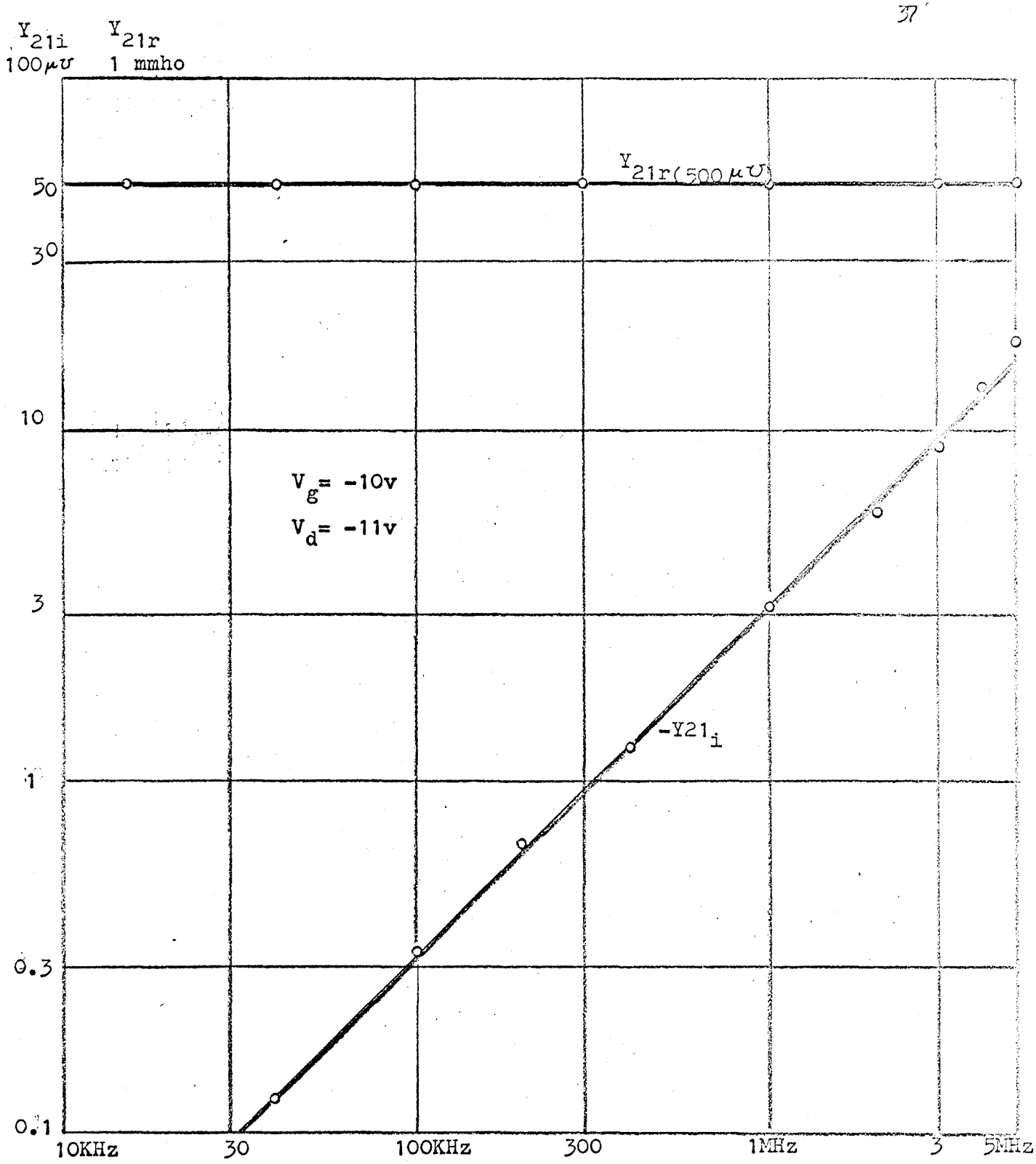


Fig. 3.13 Y_{21} Parameter Measurement Result

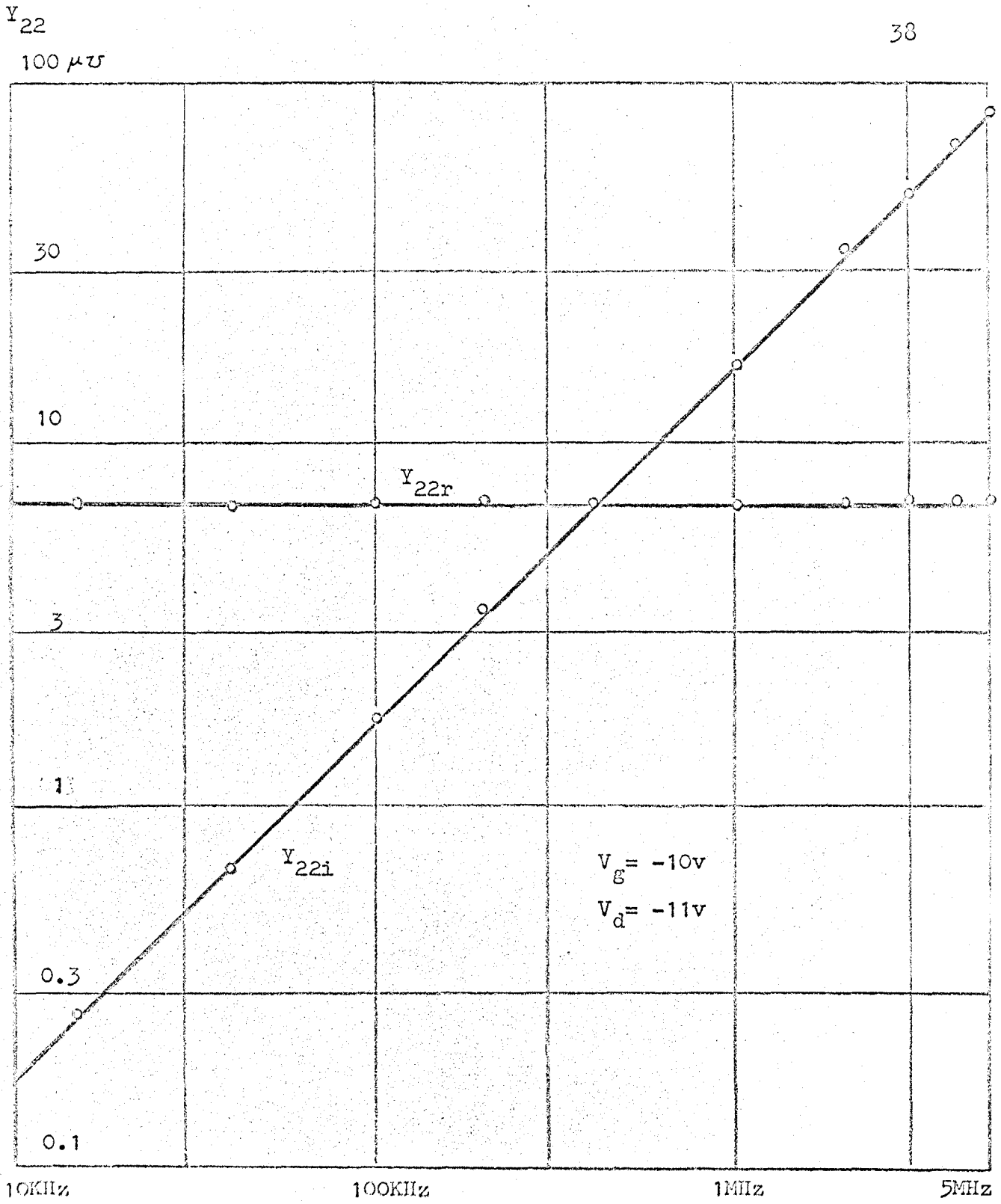


Fig. 3.14 Y_{22}Parameter Measurement Result

CHAPTER IV

The Noise Model of MOS FET

4.1 Introduction

Although many published papers have been devoted to the study of noise in junction-gate FETs, there is at present very little information available on the noise in MOS devices, theoretical or experimental.

A. G. Jordan and N. A. Jordan[13] have presented a theoretical investigation of the noise-generating mechanisms in MOS diodes and triodes, which does not include any experimental evidence. Using the single-level Shockley-Read-Hall state assumptions they first discuss the impedance of an MOS diode, and analyze the gate noise in an unbiased-drain MOS triode. Then following along van der Ziel's line in treating the thermal noise of junction-gate FETs, they analyze the thermal noise in the surface channel of the MOS devices. C. T. Sah[14] has published an abstract* of a report on $\frac{1}{f}$ surface noise, in which he developed, using the gradual channel approximation, a low frequency $\frac{1}{f}$ noise theory which accounts for noise associated with the random emission and capture of charge carriers in bulk states in the surface channel and in the surface states. Referring to measurements

---

* This paper is still not published

made from $5H_z$ to 15 MH_z, he concludes the $\frac{1}{f}$ noise is negligible above 100 KH_z. D. N. Nicol[15], also following van der Ziel, gives without detail a thermal noise formula, but his accompanying experimental results do not fit his theoretical prediction well. It seems that a study of noise in MOS FETs might be a very tricky one. Viewing this situation, it is interesting to make an effort to investigate the MOS device noise properties both theoretically and experimentally.

Since none of these published works gave a combined study (both theoretical and experimental) of noise in this device, this chapter is intended to derive a noise model from the experimentally-tested circuit model given in chapter III. An equivalent noise resistance is also derived and then the calculated results are compared with those measured.

4.1.1 Noise-generating Mechanisms in Semiconductors

Noise may be defined as the spontaneous fluctuations in the number and energy of the charge carriers in any electron device. Since these fluctuations giving rise to the noise occur at random, they are therefore governed by the laws of statistical thermodynamics.

Noise in semiconductors arises from several different physical mechanisms.

a) Thermal noise (also called Johnson noise) having a uniform power spectrum, is associated with the thermal agitation of carriers in the ohmic sections of the semiconductors. According to Nyquist, any solids having resistance and not a absolute zero degree temperature, will exhibit this noise. A quantitative theory relating to the thermal noise

power generated in any resistor (having resistance R, at temperature T, in a frequency bandwidth of Δf) was furnished in 1928 by Nyquist[16] as follows:

$$\overline{e_n^2} = 4kTR\Delta f \tag{4-1}$$

where $\overline{e_n^2}$ = mean-square open circuit noise voltage

k = Boltzmann's constant = 1.38×10^{-23} joules/°K

T = temperature in Kelvin °K

R = resistance in ohms

Δf = bandwidth of observation in Hertz per second

An equivalent expression for the mean-square short-circuit noise current between the resistor terminals is

$$\overline{i_n^2} = 4kTG\Delta f \tag{4-2}$$

where G = conductance of the resistor, in mhos

b) Shot noise, also a white noise, is due to the randomness of carrier diffusion and generation-recombination processes of electrons and holes in semiconductors. The diffusion process gives rise to shot noise because of the flow of carriers by diffusion is made up of transferals of charge in a set of random independent events. The shot noise arising from generation-recombination process is caused by the spontaneous fluctuations in the generation rates and the recombination rates of the carrier, thus causing fluctuations in the free carrier densities.

In 1918 Schottky[17] gave a formula pertaining to the shot noise power generated by a temperature-limited thermionic diode which is widely used as a laboratory noise standard. The formula is

$$\overline{i^2} = 2eI_{dc}\Delta f \qquad (4\text{-}3)$$

where e = electron charge = 1.6×10^{-19} Coulombs

I_{dc} = anode d.c. current in Ampere

c) Low-frequency noise (also called flicker noise, $\frac{1}{f}$ noise or surface noise). The power spectrum of the low-frequency noise varies inversely with frequency, and is of the form $\frac{1}{f^{\alpha}}$, where $\alpha \approx 1$. In semiconductors, it is normally observed at the lower audio frequencies but can manifest itself into the MH_z or even higher frequency regions. For germanium devices, it has been observed at frequencies as low as 10^{-5} H_z [18].

It has been known for many years[19] that the traps in surface states are possibly the main generating mechanisms for this low frequency noise. By suggesting that if the energy levels of the traps are distributed over a considerable energy range, then the frequency spectrum characterizing their charge and discharge by capturing and emitting electrons will be of the $\frac{1}{f}$ type.

Using a mathematical approach, van der Ziel[20], and Du Pre[21] found that a superposition of $\frac{\tau}{(1 + w^2\tau^2)}$ shot noise spectra can result in a $\frac{1}{f}$ law if a distribution of time constants $g(\tau) = \frac{A}{\tau}$ is introduced. Thus the problem in this case is transformed to finding a physical mechanism which can interpret this peculiar distribution of time constants.

McWhorter[22] suggested that the low-frequency noise is due to the random fluctuation in the surface potential barrier, therefore the number of majority carriers trapped in the surface states is modulated and

so is the surface recombination velocity. The range of relaxation time distribution is assumed to arise by suggesting that the surface may be thought of as divided into a number of areas, each with a trap relaxation time τ. But Watkins[23] found that this theory is at variance with experimental facts. It seems that although that the low-frequency noise is associated with the fluctions of surface recombination velocity, these fluctuations are not related to the surface potential barrier fluctuations.

Although many theories have been set forth to explain the low-frequency noise phenomena, it has not proved possible to give a precise low-frequency noise model for even a carbon resistor.

4.1.2 Noise Characterization and Specification of Four-Terminal (Two-port) Networks

a) Noise Characterization:

From circuit analysis, any linear, noisy, 4-terminal (2-port) device can always be represented by a noiseless device equivalent circuit plus two noise generators, each of which can be either a small-signal noise voltage generator or a noise current generator. This gives a total of six possible configurations, of which only two are of comparative importance in device noise study (Fig. 4.1 and 4.2).

In general, these two noise sources are partially correlated. Each generator is assumed to represent the random noise over a frequency interval df, for example, a noise fluctuation e(t) is represented in a

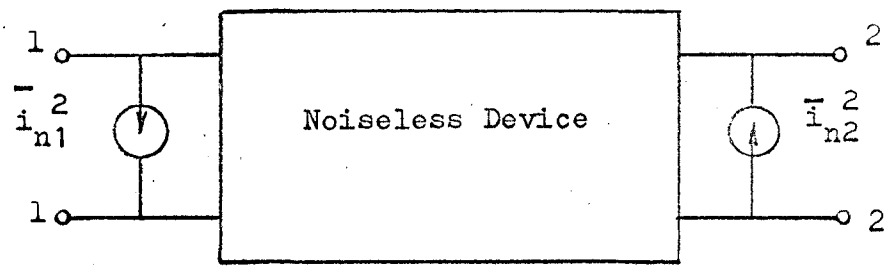


Fig. 4. 1

Noise Representation by Two Noise Current Generators

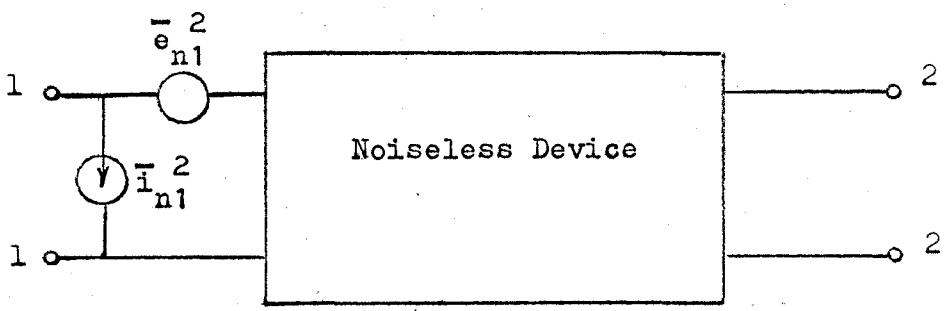


Fig. 4. 2

Noise Representation by a Noise Current and a Noise Voltage Generator

frequency range df at f by

$$e(f) = \sqrt{2}\, e_n\, e^{j\omega t} \tag{4-4}$$

where e_n is a complex random number of such value that

$$\overline{e_n e_n^*} = |\overline{e_n^2}| = S_e(f)\, df \tag{4-5}$$

where $S_e(f)$ is the voltage spectral density and can be observed experimentally, e.g.

$$\overline{e_n^2} = S_e(f)\, df = 4kTRdf$$

generally, $|\overline{e_n^2}|$ is written as $\overline{e_n^2}$ for convenience

In Fig. 4.1, $\overline{i_{n1}^2}$ and $\overline{i_{n2}^2}$ may also be represented by equivalent noise diode currents according to Schottky's formula Eq. (4-3)

$$\overline{i_{n1}^2} = 2eI_{dc1}df$$

$$\overline{i_{n2}^2} = 2eI_{dc2}df$$

where I_{dc1} and I_{dc2} can be easily measured.

In this thesis, the noise representation method of Fig. 4.1 is adopted.

b) Noise Specification

(i) Noise resistance, R_n

A useful noise specification for a noisy 2-terminal device (or a 4-terminal device, ~~if one of the two noise generators in Fig. 4.1 and 4.2 can be neglected~~) is the noise resistance R_n, where

$$\overline{e_n^2} = 4KTR_n\Delta f \tag{4-6}$$

This means that the noise of the device is equivalent to the thermal noise generated in an equivalent noise resistance R_n.

(ii) Noise factor, F

The commonly accepted measure of the noise performance of a 4-terminal (2-port) device is the noise factor. The noise factor F is defined*[24] as the ratio of (1) the total noise power per unit bandwidth available at the output port when the noise temperature of input termination is standard (290°K) to (2) the portion of (1) engendered by the input termination.

For a device having a noise resistance R_n and a source resistance R_s, then according to the definition of noise factor F given above

$$F = 1 + \frac{R_n}{R_s} \tag{4-7}$$

Therefore, when specifying the noise factor of a device, it is important to specify the source resistance and the operating condition. Then, an accurate measure of the noisiness can be obtained.

If a linear, noisy 4-terminal device network is represented by the Y-parameters and two noise current generators as shown in Fig. 4.3 then the noise factor F can be shown to be given by (see Appendix B)

$$F = 1 + \frac{\left|i_{n1} + \left(\frac{Y_n + Y_s}{Y_{21}}\right) i_{n2}\right|^2}{4KTG_s\Delta f} \tag{4-8}$$

---

* From IEEE Standard

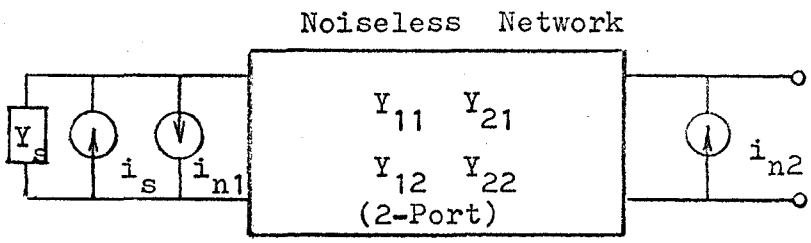


Fig. 4. 3 Circuit Diagram for Eq. 4-8

where Y_s = source admittance = $G_s + jB_s$

$4kTG_s\Delta f$ = mean-square noise current generated by source conductance G_s at room temperature

4.2 Noise in MOS FETs and the Noise Model

Various types[13] of noise in MOS FETs can be considered to be associated with physical regions of the device as follows:

1. Thermal noise associated with the channel conductance
2. Input noise associated with the gate structure
3. Low-frequency noise associated with the surface

The possible theories[13] concerning the above listed noise sources in MOS FET will be investigated first. Then a noise resistance and a noise model will be derived from which the noise factor can be calculated.

4.2.1 Thermal Noise

a) Drain Short-circuit Noise Current

The thermal noise developed in the channel of an MOS FET is associated with the channel conductance. If a small fluctuation voltage ΔV_x is developed in the channel at a distance x_i from the source (Fig 4.4), this fluctuation voltage will modulate the channel conductance and produce a short-circuit current fluctuation ΔI_d in the drain output circuit.

To find the current fluctuation $\Delta I_d(x)$ in the channel at X_i due to the fluctuation voltage ΔV_x, one first recalls that (from Eq. 2-1 and 2-4)

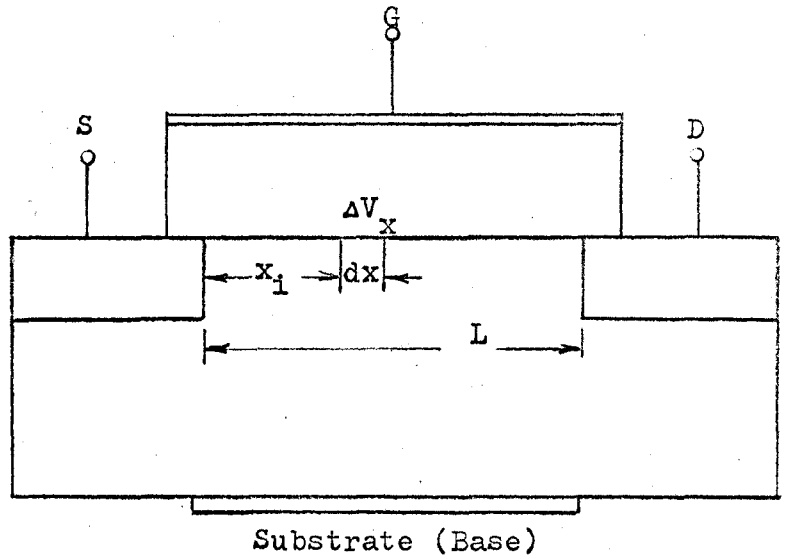


Fig. 4.4 Diagram for Channel Noise Investigation

$$I_d(x) = [\mu_o C_{oz}(V_g - V_p - V(x)] \frac{dV(x)}{dx} \tag{4-9}$$

Then (by analogy with $I = uv$, $\Delta I = u\Delta v + v\Delta u$)

$$\Delta I_d(x) = \mu_o C_{oz} [(Vg - V_p - V(x)\frac{d\Delta V(x)}{dx} + \frac{dV}{dx}(-\Delta V(x)]$$

$$= \mu_o C_{oz} \frac{d}{dx} [(V_g - V_p - V(x))\ \Delta V(x)] \tag{4-10}$$

The total drain current fluctuation due to $\Delta V(x)$ is then found by integrating $\Delta I_d(x)$, with respect to x (from $x=0$ to $x=x_i$, and from $x=x_i + dx$ to $x=L$). Realizing that

$$\Delta V(o) = 0$$

$$\Delta V(L) = 0$$

one finds

$$\mu_o C_{oz}(V_g - V_p - V(x))\Delta V(x) = \Delta I_d(x) \text{ for } o<x\leq x_i \tag{4-11}$$

$$\mu_o C_{oz}(V_g - V_p - V(x))\Delta V(x) = \Delta I_d(x-L) \text{ for } x_i + dx \leq x<L \tag{4-12}$$

since

$$\Delta V(x_i + dx) - \Delta V(x_i) = \Delta V_x \tag{4-13}$$

Then, combining Eq. (4-11), (4-12) and (4-13), one arrives at an expression for the total mean-square drain current fluctuation due to the fluctuation ΔV_x i.e.

$$\overline{\Delta I_d^2} = [\frac{\mu_o C_{oz}}{L}(V_g - V_p - V(x))\ \Delta V_x]^2 \tag{4-14}$$

Since from Eq (2-3), $\rho(x) = C_{oz}(V_g - V_p - V(x))$

$$\therefore \quad \overline{\Delta I_d^2} = [\frac{\mu_o}{L}\rho(x)\ \Delta V_x]^2 \tag{4-15}$$

So far, no restriction has been made on the fluctuation source of voltage ΔV_x, therefore it can be used as a general formula.

To consider the thermal noise associated with the channel conductance, let dR be the channel resistance of the section dx along the channel at X, then

$$\overline{\Delta V_x^2} = 4kTdR$$

where $dR = \frac{dx}{\sigma(x)} = \frac{dx}{\mu_o \rho(x)}$ (4-16)

then

$$\begin{aligned}\overline{\Delta I_d^2} &= [\frac{\mu_o}{L} \rho(x)\ \Delta V_x]^2 \\ &= [\frac{\mu_o}{L} \rho(x)]^2\ 4kTdR \\ &= [\frac{\mu_o}{L} \rho(x)]^2\ 4kT\ \frac{dx}{\mu_o \rho(x)} \\ &= 4kT\ \frac{\mu_o}{L^2}\ \rho(x)\ dx \end{aligned} \quad (4\text{-}17)$$

To find the total short-circuit drain current fluctuation $\overline{I_n^2}$ due to the thermal voltage fluctuation of the whole channel, one integrates Eq (4-17) from x = 0 to x = L,

$$\begin{aligned}\overline{I_n^2} &= 4kT\ \frac{\mu_o}{L^2} \int_o^L \rho(x)\ dx \\ &= 4kT\ \frac{\mu_o}{L^2} \int_o^L C_{oz}\ (V_g - V_p - V(x))\ dx \end{aligned} \quad (4\text{-}18)$$

This integral can be evaluated explicitly by relating dx to dV(x). From Eq. (2-5) and (4-9), one finds

$$dx = \frac{\mu_o C_{oz}}{I} [V_g - V_p - V(x)]\, dV(x)$$

$$= \frac{L(V_g - V_p - V(x))}{[(V_g - V_p)V_d - \frac{V_d^2}{2}]}\, dV(x) \qquad (4\text{-}19)$$

substitution of Eq. (4-19) into (4-18) yields

$$\overline{I_n^2} = 4kT \frac{\mu_o C_{oz}}{L} \int_o^{V_d} \frac{(V_g - V_p - V(x))^2}{[(V_g - V_p)V_d - \frac{V_d^2}{2}]}\, dV(x)$$

$$= \frac{4kT\, \mu_o C_{oz}}{L[(V_g - V_p)V_d - \frac{V_d^2}{2}]} \left[\frac{(V_g - V_p)^3 - (V_g - V_p - V_d)^3}{3}\right] \qquad (4\text{-}20)$$

Let $u = \frac{V_d}{V_g - V_p}$, then

$$(1-u) = \frac{(V_g - V_p - V_d)}{(V_g - V_p)} \qquad (4\text{-}21)$$

and Eq. (4-20) becomes

$$\overline{I_n^2} = \frac{4kT\mu_o C_{oz}}{L} (V_g - V_p) \frac{2}{3} \frac{1-(1-u)^3}{u(2-u)}$$

$$= \frac{4kT\mu_o C_{oz}}{L} (V_g - V_p)\, M(u) \qquad (4\text{-}22)$$

where $M(u) = \frac{2}{3} \frac{1-(1-u)^3}{u(2-u)}$ (4-23)

From Eq. (2-9) $g_d = \frac{\mu_o C_{oz}}{L} (V_g - V_p - V_d)$

then

$$g_{do} = g_d \Big|_{V_d=o} = \frac{\mu_o C_{oz}}{L} (V_g - V_p) \qquad (4\text{-}24)$$

and from Eq (2-10) $g_m = \frac{\mu_o C_{oz}}{L} V_d$

When operating in saturation region (as in linear applications), $V_d = V_g - V_p$, therefore g_m (at saturation) is numerically equal to g_{do}, i.e.

$$g_m(\text{at saturation}) = g_{do} = \frac{\mu_o C_{oz}}{L}(V_g - V_p) \qquad (4\text{-}25)$$

Since $u = \frac{V_d}{V_g - V_p}$, then

$$u \to o \quad \text{as } V_d \to o$$

$$u \to 1 \quad \text{as } V_d \to V_g - V_p, \text{ (saturation occurs)}$$

Therefore from Eq. (4-23)

$$\lim_{u \to o} M(u) = \lim_{u \to o} \frac{2}{3} \frac{1-(1-u)^3}{u(2-u)} = 1$$

$$\lim_{u \to 1} M(u) = \lim_{u \to 1} \frac{2}{3} \frac{1-(1-u)^3}{u(2-u)} = \frac{2}{3}$$

Then Eq. (4-22) may be simplified as follows

$$\overline{I_n^2} = 4kT\, g_{do}\, M(u) = 4kT\, g_{do}, \text{ (at } V_d = 0) \qquad (4\text{-}26a)$$

$$\overline{I_n^2} = 4kT\, g_m\, M(u) = 4kT\, g_m \frac{2}{3}, \text{ (at saturation)} \qquad (4\text{-}26b)$$

It is obvious from Eq. (4-26) that the thermal noise current $\overline{I_n^2}$ (at V_d=0) is exactly equal to the thermal noise current generated by g_{do}, which is as expected from Nyquist formula. $\overline{I_n^2}$ (at saturation) will drop to $\frac{2}{3}$ of that given by Eq. (4-26a).

A plot of the thermal noise modulation factor M(u) of Eq. (4-23) is given in Fig. (4.5). From the M(u) plot, one may state that the short-circuit mean-square drain noise current $\overline{I_n^2}$ will also saturate as drain is approaching saturation.

4.2.2 The Input Noise

Unlike thermal noise or shot noise, the input noise associated with the gate is not a fundamental type of noise. It results from the combined effect of the leakage current through the gate oxide layer and the channel-noise coupling effect due to the channel-gate capacitance. At low frequencies the device could exhibit excessive noise if leakage is pronounced. However, for a normal device the leakage current through the oxide layer is negligibly small. For the device under study, the leakage current has an order of 10^{-5} nano-amperes at 25°C[12]. At higher frequencies, a small increase in input noise may be expected due to the fact that the capacitance between the gate and channel will have some effect in coupling the thermal noise of the channel and noise due to the fluctuation in the occupation of surface states in the surface channel into the gate circuit.

Jordans[13], relying on Lehovec and Slobodskoy's[25] MOS diode equivalent circuit (which in turn is based on the single Shockley-Read-Hall[26] state assumption), have given a theoretical study of this noise (as mentioned in the previous section). Using a number of

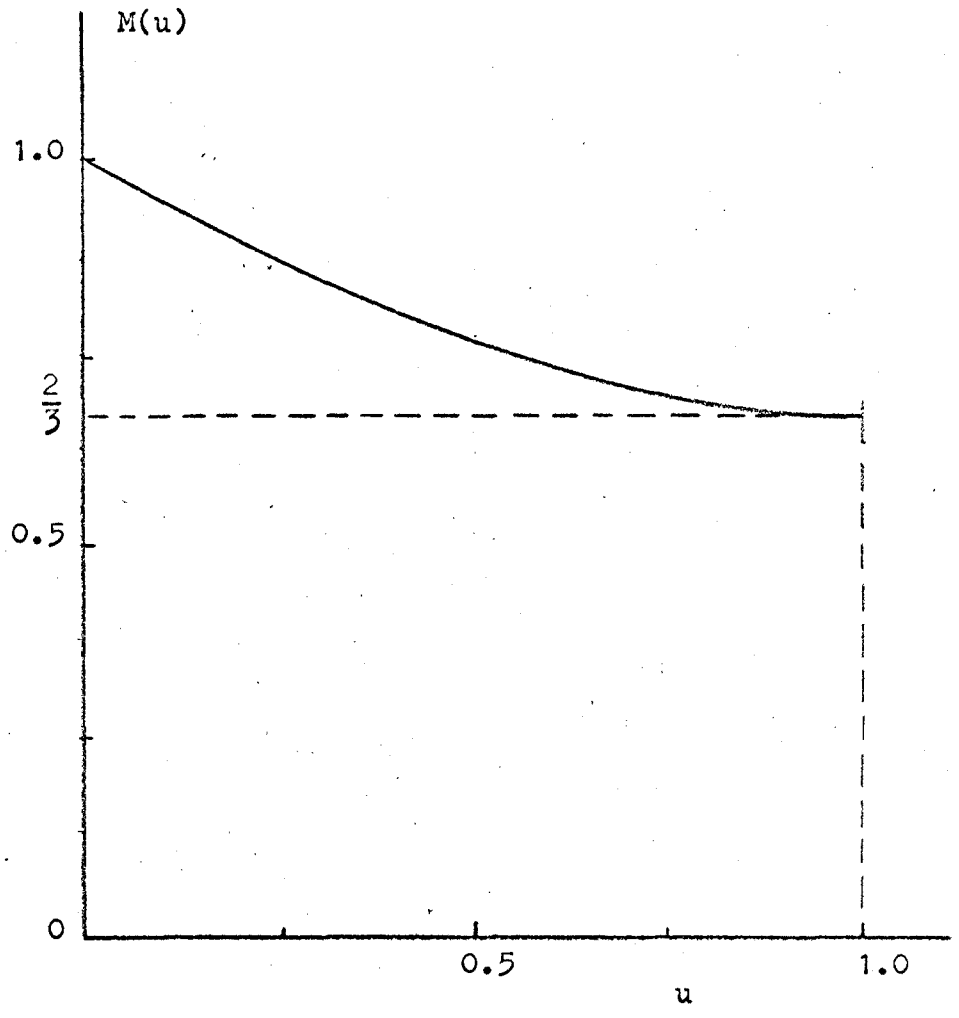


Fig. 4.5 M(u) versus u Plot

approximations, they give an expression for the input noise $\overline{i_g^2}$ (under the drain unbiased condition) which results in nearly the same conclusion about the input noise as mentioned above. The expression is

$$\overline{i_g^2} = 4 \frac{C_o^2}{C_p^2} e^2 c_p p_s f_t \frac{\omega^2 \tau_p^2}{1+\omega^2 \tau_p^2} \qquad (4\text{-}27)$$

where C_o = gate to channel capacitance

C_p = capacitance associated with the valence band of the inversion layer

e = electron charge

c_p = hole capture probability

p_s = hole density at the surface (cm^{-3})

f_t = fraction of surface states occupied by electrons

ω = frequency of operation

τ_p = time constant corresponding to capture of holes

The conclusions they made are mainly as follows.

a) The input noise is a high frequency noise which may become appreciable only when $\omega \rightarrow \frac{1}{\tau_p}$. For the device under study (Silicon device), the order of magnitude of τ_p is 10^{-9} sec. and therefore the frequencies at which $\overline{i_g^2}$ becomes significant are in the hundreds of MH_z (if $\tau_p = 10^{-9}$sec. then $f = \frac{\omega}{2\pi} = 167\ MH_z$).

b) If the oxide layer is very thick as compared to the channel layer (this is usually the case, which the shallow channel approximation is based upon), then C_o may be so much smaller than C_p that the noise is unobservable.

Since the measuring range in this study extends only up to 30 MH_z, the input noise associated with the gate will be assumed negligible.

4.2.3 The Low-Frequency Noise

The low-frequency noise is commonly accepted as being attributed to the fluctuation in the number of carriers in occupation of surface states. Since the surface plays a dominant role in the operation of the device, this is probably why the low-frequency noise in MOS FETs is usually orders of magnitude higher than the junction-gate FETs[27].

Recently, Lauritzen and Sah[27] reported that the charge fluctuations of the Shockely-Read-Hall[26] generation-recombination centers in the p-n junction depletion region is a new type of noise mechanism that gives a major contribution to the low-frequency noise in junction gate FETs. Although the basic structure of the two types of FET is different, there is a p-n junction actually formed by the surface channel and the bulk substrate in the MOS FETs. Therefore, in MOS device the above mentioned generation-recombination centers may also contribute to the low-frequency noise.

Jordans[13] however, by completely ignoring the effect of the generation-recombination centers, derived a low-frequency noise formula for the induced p-channel enhencement mode MOS device. The assumption greatly simplifies their analysis, but may not be realistic

in MOS devices, since the effect of these generation-recombination centers plays another dominant role in determining the relaxation time distribution. Their expression for the low-frequency noise due to the fluctuation in the occupation of surface states (or simply termed as due to the carrier density fluctuation in the surface channel) is given by

$$S_{I_d}(f) = 4kT \frac{\mu_o^2}{L^3} C_D \frac{\tau_n}{1 + \omega^2 \tau_n^2} V_d^2 \qquad (4\text{-}28)$$

where

$S_{I_d}(f)$ = spectral density of the drain current noise

C_D = capacitance associated with the depletion region (between bulk and surface channel)

τ_n = time constant corresponding to capture of electrons

The rest of the terms are the same as introduced before. They conclude that the time constant τ_n in Eq. (4-28) is of the order of tenths of seconds, and will vary along the length of channel as channel voltage varies. Thus, a superposition of $\frac{\tau_n}{(1+\omega^2\tau_n^2)}$ spectra with continuous distribution of τ's will give rise to $\frac{1}{f}$ type noise spectrum[20].

They also neglected the low-frequency noise contributed by holes in the device by saying that the fluctuation due to holes are very fast and only produce high frequency noise in the hundred of MH_z range.

Since they presented no experimental evidence, their theory concerning low-frequency noise with the generation-recombination centers in depletion region completely neglected is not well established. As mentioned in the introduction of this chapter, the knowledge of the physical process concerning low-frequency noise is still a hard nut to crack. The difficulty lies in finding a mechanism which will exhibit a $\frac{1}{\tau}$ distribution of relaxation time over an extensive region (of the order of 6 or more decade). So far, no satisfactory theory has been found yet. However, in the subsequent noise model derivation, an empirical formula which fits the low-frequency noise spectra will be employed, which will allow the noise factor in this peculiar region to be calculated.

Thus if in the low frequency region, the mean-square short-circuit drain noise current exhibits a slope of -10 db per decade up to a $\frac{1}{f}$ corner frequency f_1, then Eq. (4-26b) can be modified to cover the whole frequency range of investigation,

$$\overline{I_n^2} = 4kT\, g_m\, M(u)\, (1 + \frac{f_1}{f})\, \Delta f \qquad (4\text{-}29)$$

where f is the device operating frequency and Δf is the bandwidth of observation.

When operated at saturation as in most applications

$$\overline{I_n^2} = (\frac{2}{3})\, 4kT\, g_m\, (1 + \frac{f_1}{f})\, \Delta f$$

$$= \frac{8}{3} kT\, g_m\, (1 + \frac{f_1}{f})\, \Delta f \qquad (4\text{-}30)$$

4.2.4 The Noise Model and the Equivalent Noise Resistance

a) The Noise Model

The necessary noise relations required for the noise model have now been obtained, and with the assumption that the input noise associated with the gate is neglected as discussed in section 4.2.2, the noise model for the device under study is of the form as given in Fig. 4-6.

b) The Noise Resistance R_n

The noise current generator in the drain circuit of Fig. (4-6) may also be represented by an equivalent noise resistance R_n connected in series with the device input gate terminal.

Introducing the noise resistance R_n of the device, by putting[8]

$$\overline{I_n^2} = 4kT\, R_n \Delta f\, g_m^2 \qquad (4\text{-}31^*)$$

and combining Eq. (4-29) and (4-31) yields

$$R_n = \frac{1}{g_m}\, M(u)\, \left(1 + \frac{f_1}{f}\right) \qquad (4\text{-}32)$$

When operating at saturation

$$R_n = \frac{2}{3}\frac{1}{g_m}\, \left(1 + \frac{f_1}{f}\right) \qquad (4\text{-}33)$$

---

* Eq. (4-31) is an approximation by assuming $Y_{21} = g_m$, this is the case for low frequency operation.

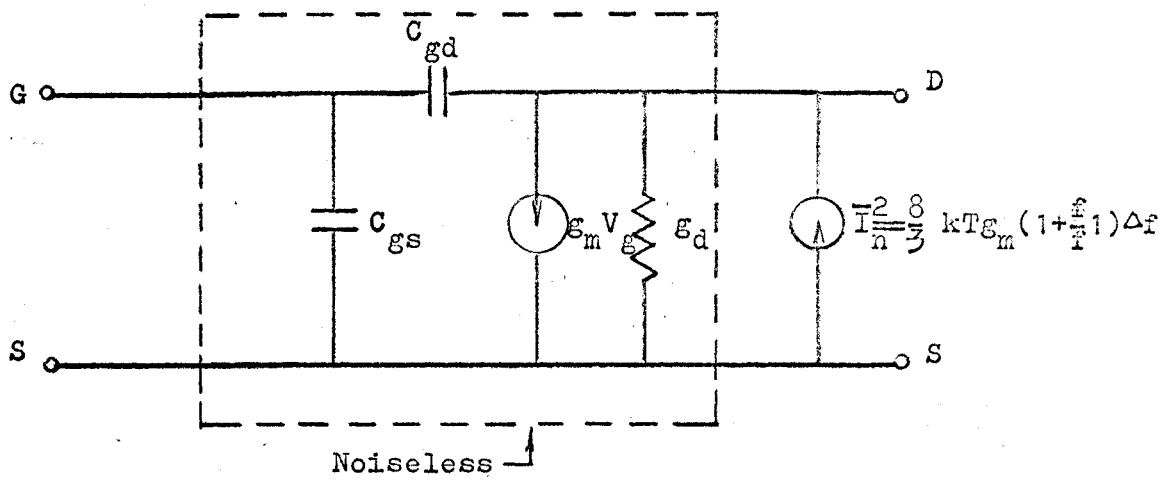


Fig. 4.6 Noise Model Of the MOS FET

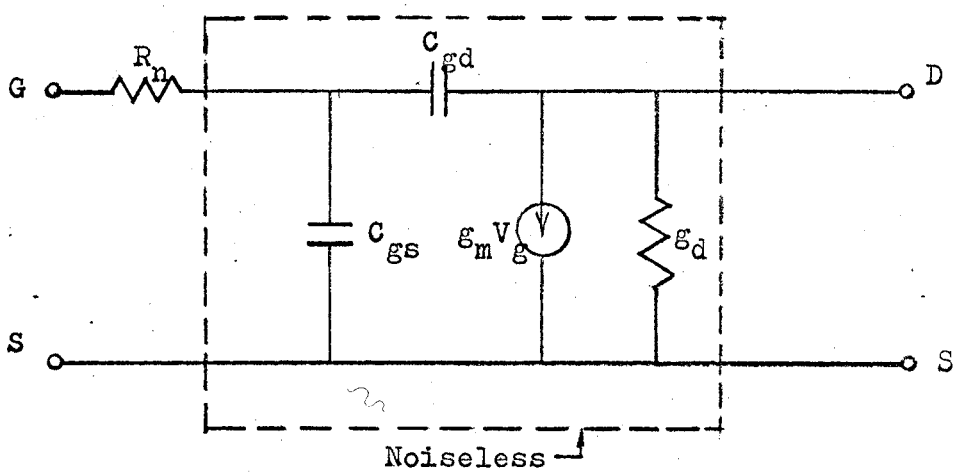


Fig. 4.7 An alternative Noise Model Of the MOS FET

Therefore, an alternative form of the device noise model may be given as Fig. (4-7).

The order of magnitude of R_n (if only the thermal noise is considered) at saturation for the device under study (Fairchild FI-100 MOS FET, the typical value of g_m is 600μ mho) is

$$R_n = \frac{2}{3}\frac{1}{g_m} \simeq 10^3 \text{ ohm} \tag{4-34}$$

4.3 Experimental Results

4.3.1 Experimental Equipment

There are many requirements to meet to ensure a correct noise measurement. The essential equipment needed are:

1. A low-noise linear amplifier which is able to amplify the noise in the desired frequency bands to a level high enough to be detected.
2. A quadratic detector of which the output is proportional to the amplifier output power (or a linear detector with an output proportional to the square root of the noise power detected)
3. A standard noise source having its available power dispersed uniformly over the desired frequency bands and calibrated in terms of available power per unit bandwidth (used as noise reference standard)
4. A wide range sinusoidal signal generator with calibrated output for gain calibration and system tuning purposes.

5. An oscilloscope for monitoring purposes.

There are two sets of equipment used in this study.

a) Low-Frequency Noise Measurement Set (1 KH_z - 100 KH_z)

The block diagram of the low-frequency noise measuring system is shown as Fig. 4.8 (Fig. 4.8A depicts the whole assembly).

(1) The FET test stage was built in a well shielded chassis, the schematic diagram is shown in Fig. 4.9 including noise diode circuit. In this test stage, the necessary circuitry for d.c. biasing is also included with MOS FET shown connected in common source configuration.

(2) A noise generator was built using a type 5722 noise diode. It is operated in the temperature limited voltage saturated region with one fixed and two variable resistors connected in series with the filament to ensure fine control of the noise diode d.c. current to 1 μa. The noise output spectrum was checked and found constant down to 5 KH_z.

(3) The low noise amplifier used in the test set is a Keithley Model 103. It has a frequency response from 0.1 H_z to 100 KH_z (3db points), and a selectable gain of 100 or 1000. With input short-circuited, the noise voltage measured in a 100 KH_z bandwidth is 1.9 microvolts referred to input (with gain of 1000 and at "low noise" operation) which meant an equivalent noise resistance of 1.4 K. This was also checked by measuring mean-square output voltage versus source resistance and found in full agreement. See Fig. 4.10

(4) The wave analyzer used is a Quan-Tech Model 303. It has a frequency range 30 H_z to 100 KH_z, with four selectable bandwidths of 10, 30, 100 and

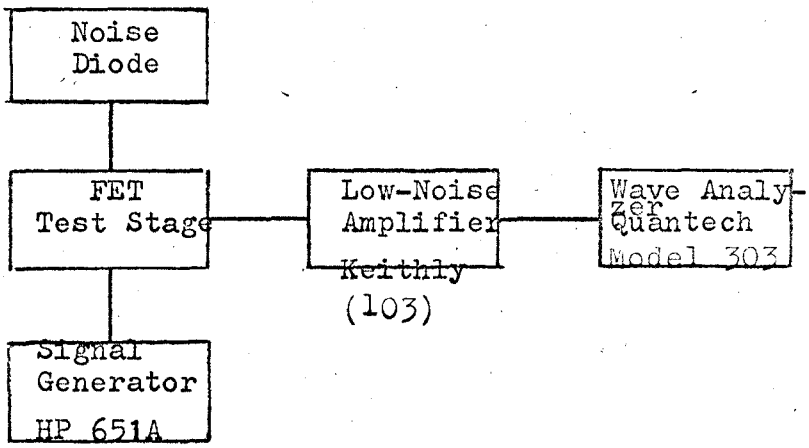


Fig. 4.8 Low-Frequency Noise Measuring System

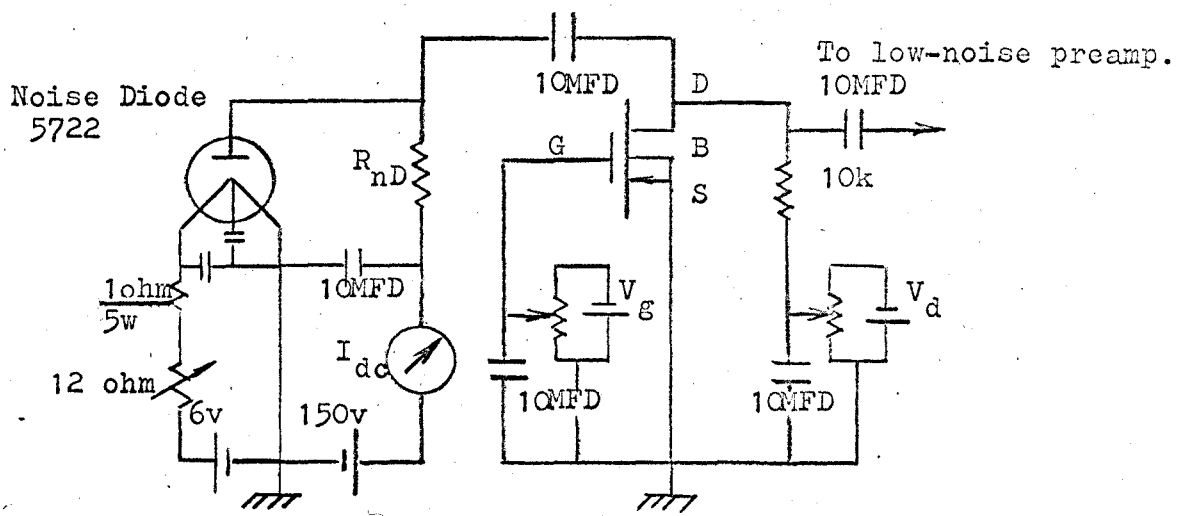


Fig 4.9 Low-Frequency Test Stage with Noise Diode Circuitry included

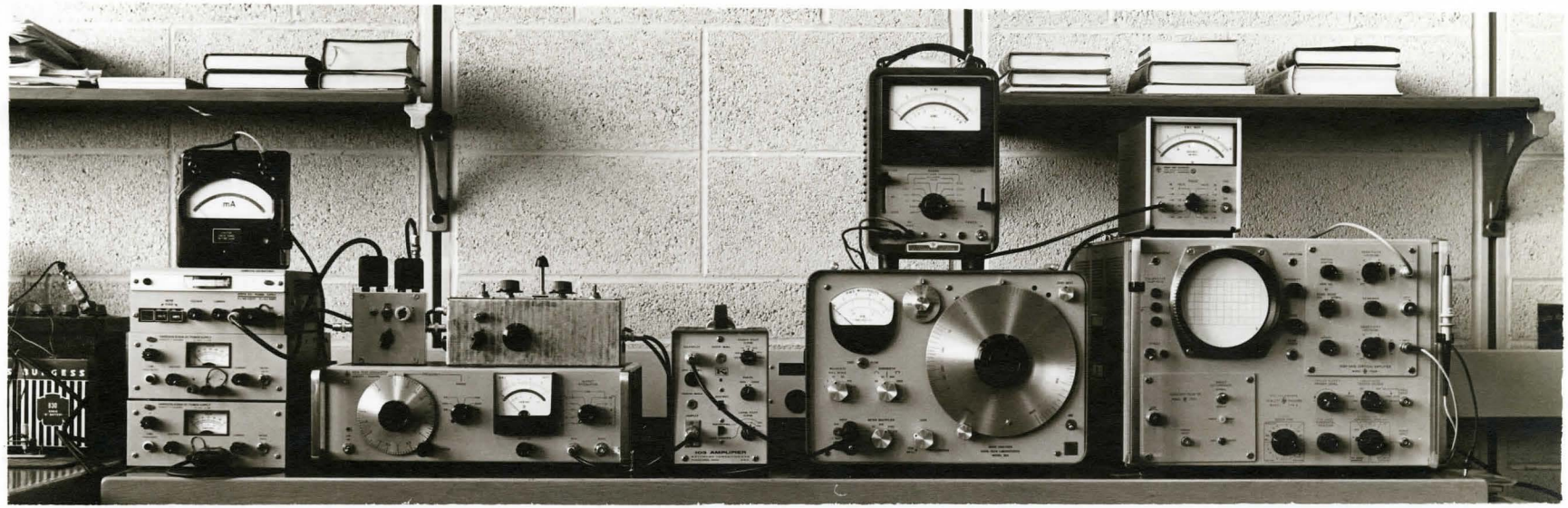


Fig. 4.8A The Complete Assembly of Low-Frequency Noise Measurement

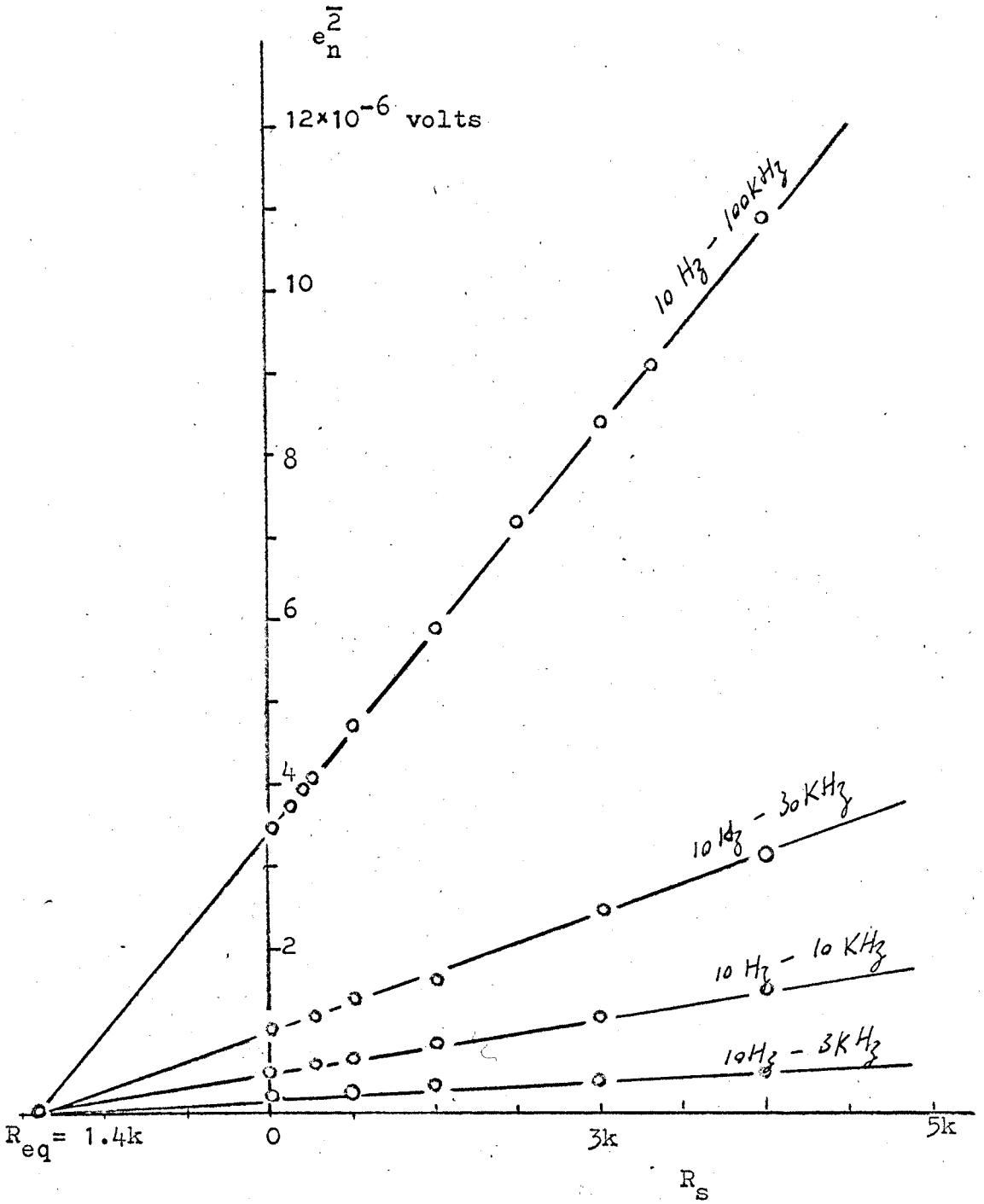


Fig. 4.10 R_{eq} of Keithly 103 Low-Noise Preamplifier

1000 H_z and an accuracy of 5% of full scale reading.

(5) The signal generator used is a Hewlett-Packard Model 651A.

b) High Frequency Noise Measurement Set (100 KH_z - 30 MH_z)

The block diagram of the high-frequency noise measuring system is shown in Fig. 4.11 (Fig. 4.11A depicts the whole assembly).

(1) The FET test stage was modified to enable high-frequency noise measurements. A tuning circuit was built in the FET drain circuit and is shown in the schematic diagram in Fig. 4.12. The drain output circuit is tuned to the signal frequency by adjusting C and L (in noise diode plate circuit) with noise diode off. The method used to determine the mean-square drain noise current will be discussed in the following sub-section.

(2) The low-noise pre-amplifier used in this test set-up is the Tektronix Amplifier Model 1121 which has an measured equivalent noise resistance of 600 ohms.

(3) The narrow band receiver used in this system is the National Radio HRO-500 which has a frequency range of 5 KH_z to 30 MH_z in sixty 500 KH_z bands (continuous coverage), with four selectable bandwidths (500 H_z, 2.5 KH_z, 5.00 KH_z and 8.0 KH_z). This receiver is operated with AVC disabled to ensure the best possible linearity. An output is taken from the last I.F. stage and connected directly to the true RMS voltmeter.

(4) The oscilloscope is Hewlett-Packard Model 175A.

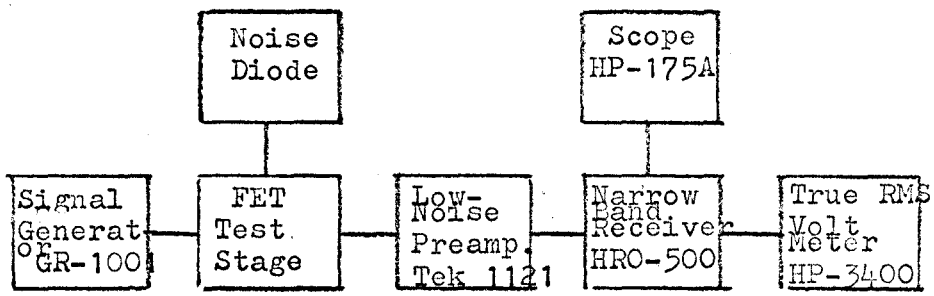


Fig. 4.11 High Frequency Noise Measuring System

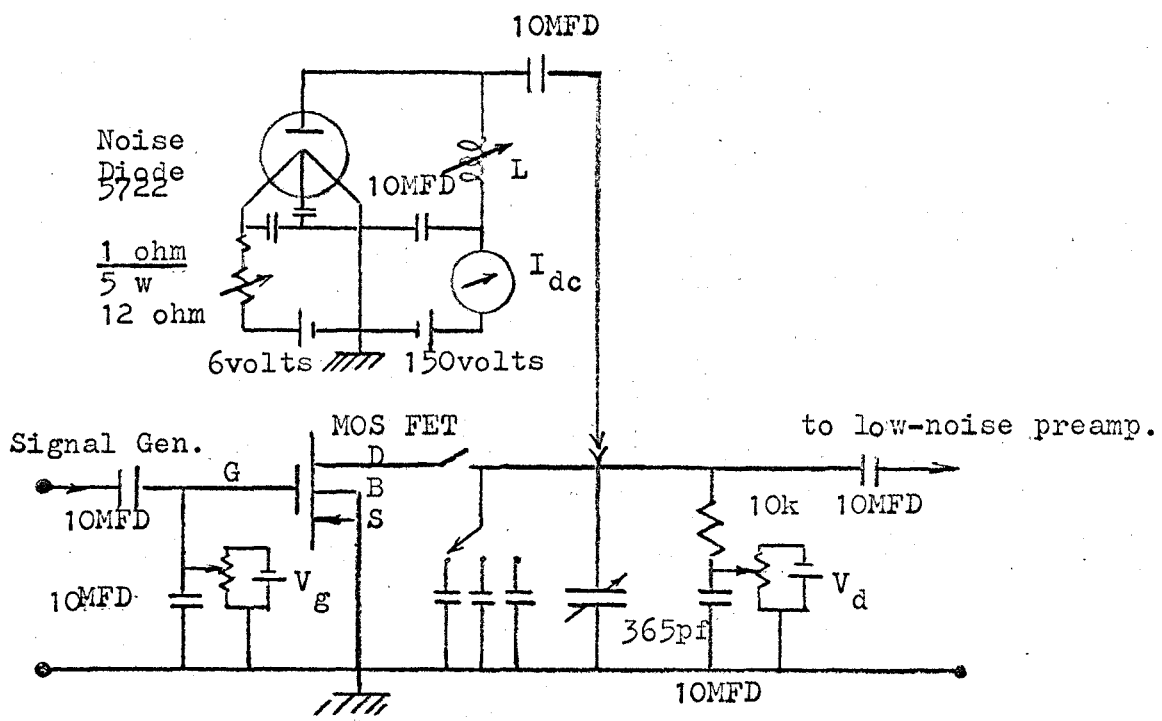


Fig. 4.12 High Frequency Test Stage with Noise Diode Circuitry included

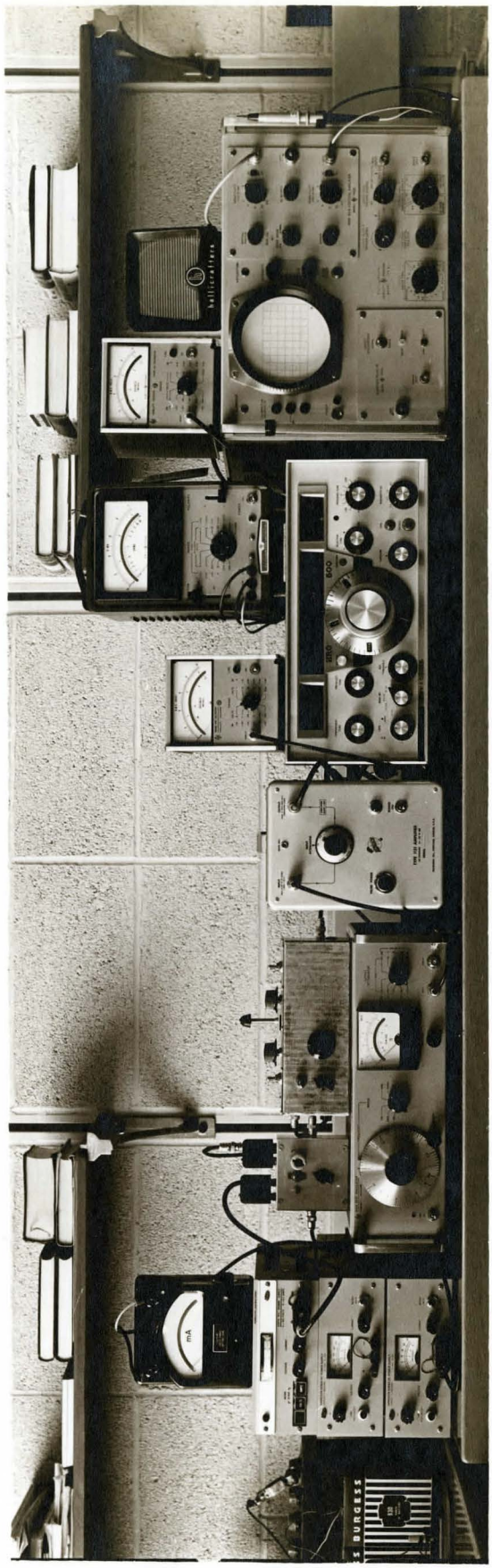


Fig. 4.11A The Complete Assembly of High Frequency Noise Measurement

4.3.2 Method of Measurement

For either low frequencies or high frequencies the following method applies.

The equivalent noise circuit for the two systems of Fig. 4.8 and 4.11 may be shown in Fig. 4.13.

where Y_{22} = device output admittance (input shorted)

$\overline{i_n^2}$ = mean square short-circuit noise current of the device

Y_L = a combination of load admittance, amplifier input admittance and noise diode admittance, the assumption is made that Y_L is unaffected by electrically turning on and off of the noise diode.

$\overline{i_{nD}^2}$ = mean square noise current generated by the noise diode

$\overline{i_L^2}$ = mean square noise current due to Y_L

$\overline{i_{in}^2}$ = mean square noise current due to Y_{in} of the amplifier

$\overline{e_n^2}$ = mean square noise voltage due to R_n of the amplifier

G = amplifier power gain

Δf = band width of the amplifier

The basic difficulty in measuring the device noise is to eliminate the background noise due to subsequent system components. The method used in this measurement consists of a set of five readings, two with the device connected, two with device disconnected and one with the preamplifier input short-circuited. First, the system is tuned with the device connected and the noise diode open (electrically open not mechanically, i.e. the noise diode admittance is still in the circuit)

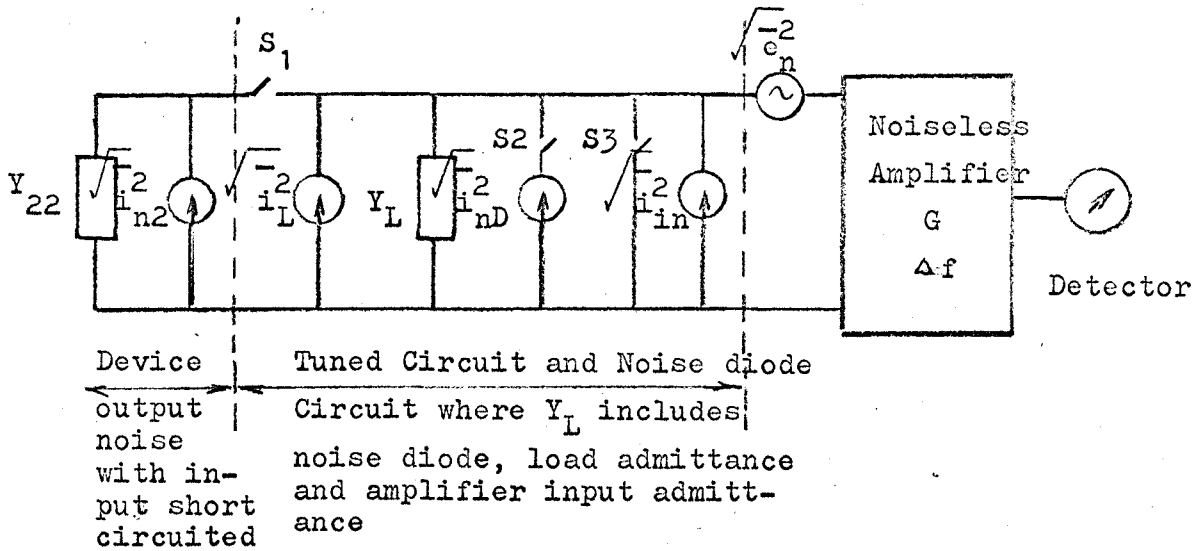


Fig. 4.13 The Noise Equivalent Circuit for the Noise Measuring system

then the readings can be taken in the following order referred to Fig. 4.13:

1. with S_1 and S_2 closed, S_3 open, then the output noise reading will be

$$\Theta_1 = G(\overline{e_n^2} + \frac{\overline{i_{n2}^2} + \overline{i_L^2} + \overline{i_{in}^2} + \overline{i_{nD}^2}}{|Y_{22} + Y_L|^2} \tag{4-39}$$

2. with S_1 closed, S_2 and S_3 open the output noise reading will be

$$\Theta_2 = G(\overline{e_n^2} + \frac{\overline{i_{n2}^2} + \overline{i_L^2} + \overline{i_{in}^2}}{|Y_{22} + Y_L|^2} \tag{4-40}$$

3. with S_1, S_2 and S_3 open, the output noise reading will be

$$\Theta_3 = G(\overline{e_n^2} + \frac{\overline{i_L^2} + \overline{i_{in}^2}}{|Y_L|^2} \tag{4-41}$$

4. with S_1 and S_3 open, S_2 closed, the output noise reading will be

$$\Theta_4 = G(\overline{e_n^2} + \frac{\overline{i_L^2} + \overline{i_{nD}^2} + \overline{i_{in}^2}}{|Y_L|^2} \tag{4-42}$$

5. with S_1 and S_2 open, S_3 closed, the output noise reading will be

$$\Theta_5 = G\,\overline{e_n^2} \tag{4-43}$$

From the above five readings just taken, the noise current contribution by the device, $\overline{i_{n_2}^2}$, may be obtained as

$$\overline{i_{n2}^2} = \overline{i_{nD}^2} \left(\frac{\Theta_2 - \Theta_5}{\Theta_1 - \Theta_2} - \frac{\Theta_3 - \Theta_5}{\Theta_4 - \Theta_3} \right)$$

$$= 2eI_{dc} \left(\frac{\Theta_2 - \Theta_5}{\Theta_1 - \Theta_2} - \frac{\Theta_3 - \Theta_5}{\Theta_4 - \Theta_3} \right) \Delta f \qquad (4\text{-}44)$$

where use is made of $\overline{i_{nD}^2} = 2eI_{dc}\Delta f$ which is the Schottky equation for noise diode generator, I_{dc} is the noise diode d.c. plate current.

Certain precautions should be observed in the above measurement:

a) Amplifier power gain should be kept constant otherwise, it cannot be cancelled in the above manipulations.

b) The noise diode d.c. plate current should be adjusted to the same value when making Θ_1 and Θ_4 measurements.

c) Y_L should be kept constant during one set of 5 measurements which means that once tuning has been accomplished initially, it should not be altered.

d) During the high frequency measurements care must be taken so that disconnecting the device from the circuit (i.e. opening S_1) does not change the resonant situation appreciably. This was achieved by employing low Q resonant tuning.

4.3.3 Experimental Results

Noise measurements were made on a p-channel enhancement-mode MOS FET, type FI-100, a diffused silicon planar II device.

To test the assumption that the thermal noise associated with the channel conductance is the primary source of noise in the high-frequency region, the mean-square short-ckt drain noise current $\overline{i_n^2}$ was measured with the device operated in saturation and with the gate a.c. short-circuited. A plot of $\overline{i_n^2}$ versus frequency is shown in Fig. 4.14. At low frequencies the spectrum has a slope of approximately -10 db per decade which is the characteristic of low-frequency noise. A hump around $2MH_z$ to 20 MH_z is also observed. This could be related to the surface trapping center time constant distribution, or associated with the doping materials, i.e., the charge density fluctuations due to doping material acceptor and donor centers might be important in this frequency range. The corner frequency of this typical curve is found to be approximately $2MH_z$, which is four orders higher than that of junction-gate FET[8]. At frequencies higher than the corner frequency, the device noise has been assumed to be limited by thermal noise produced in the channel. For comparison purposes, a theoretical value of the thermal noise given by Eq. (4-26b) is calculated using the measured g_m of 500 μ mhos for this particular operating point, and is 5.5×10^{-24} amp^2/Hz. The measured value is 1.12×10^{-23}, which means a 50% discrepancy between theory and experiment. This may be explained by considering the experimental and other possible errors involved. The five-reading method

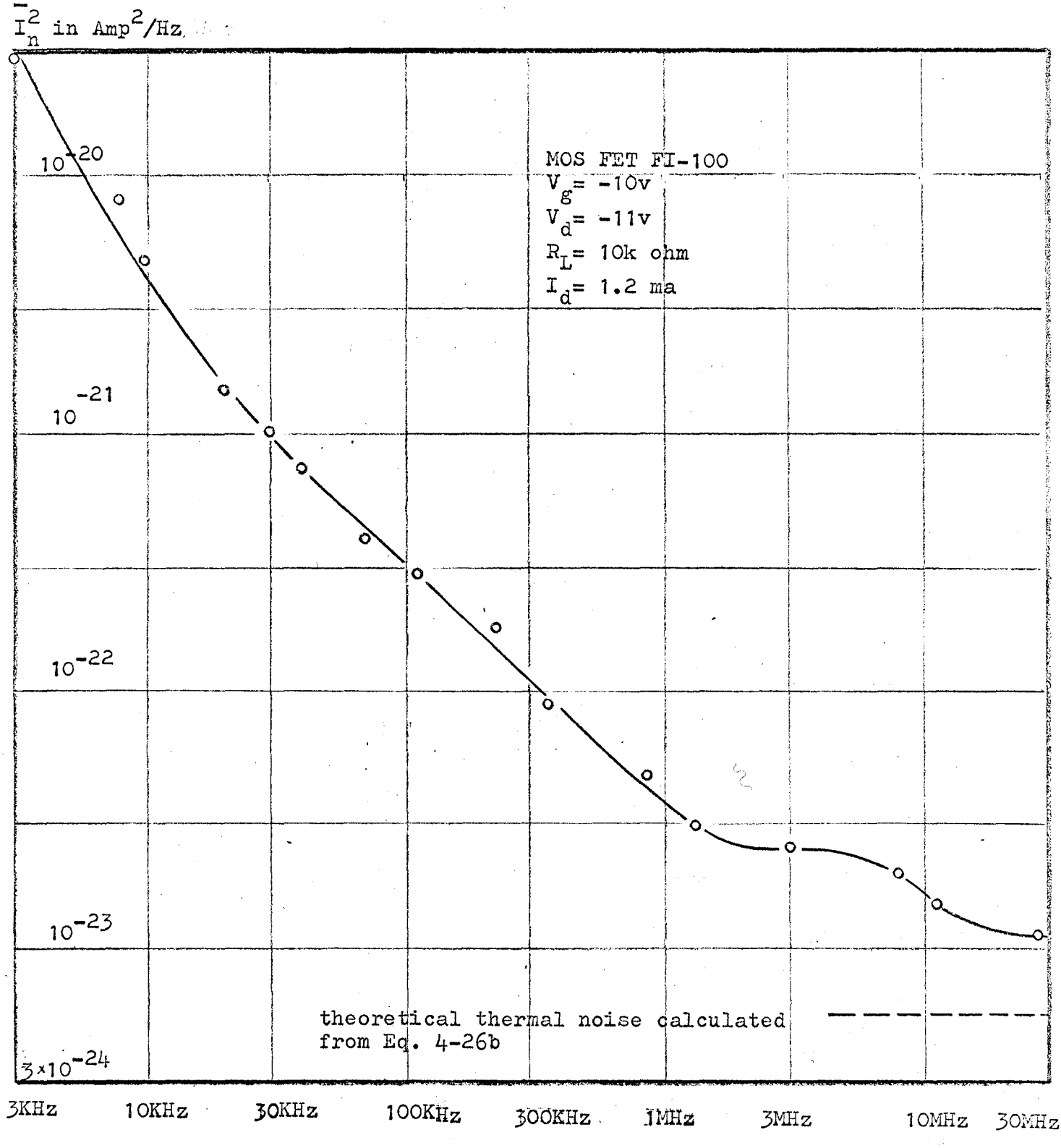


Fig. 4.14 Mean-Square Short-Circuit Noise Current $\overline{I_n^2}$ versus Frequency

of noise measurement may easily introduce an error as high as 40% for only a 1% full scale meter error. Furthermore, in a recent paper*, Sah reports that the equivalent thermal noise resistance expression $R_n = \frac{2}{3} \frac{1}{g_m}$ only holds for a substrate of intrinsic or chemically pure semiconductor. He showed that R_n will be greater than $\frac{2}{3} \frac{1}{g_m}$ for a doped semiconductor due to the effect of the bulk charge from the ionized impurities in the substrate. Thus the experimental results may fit the predicted value within experimental error if the above mentioned effect has been taken into account.

Other measurements were also made with different operating conditions to study the output noise current variations as functions of V_g and V_d. Fig. 4.15 shows the output noise current $\overline{i_n^2}$ versus frequency with V_d constant and V_g as parameter. There is a large change in noise current as gate bias varies. This can be attributed to the fact that g_m will increase as gate bias increases, and thus the noise current will increase (Eq. 4-26b). Fig. 4.16 shows the output noise current $\overline{i_n^2}$ versus frequency with V_g fixed and V_d as parameter. The noise current does not change much as V_d varies. A slight increase might be expected in this case because of the small increase in g_m with increasing V_d.

---

* C. T. Sah, et al, "The Effects of Fixed Bulk Charge on the Thermal Noise in MOS Transistors" IEEE Trans. on Electron Devices, Vol. ED-13 No. 4, April 1966. Not available at time of writing.

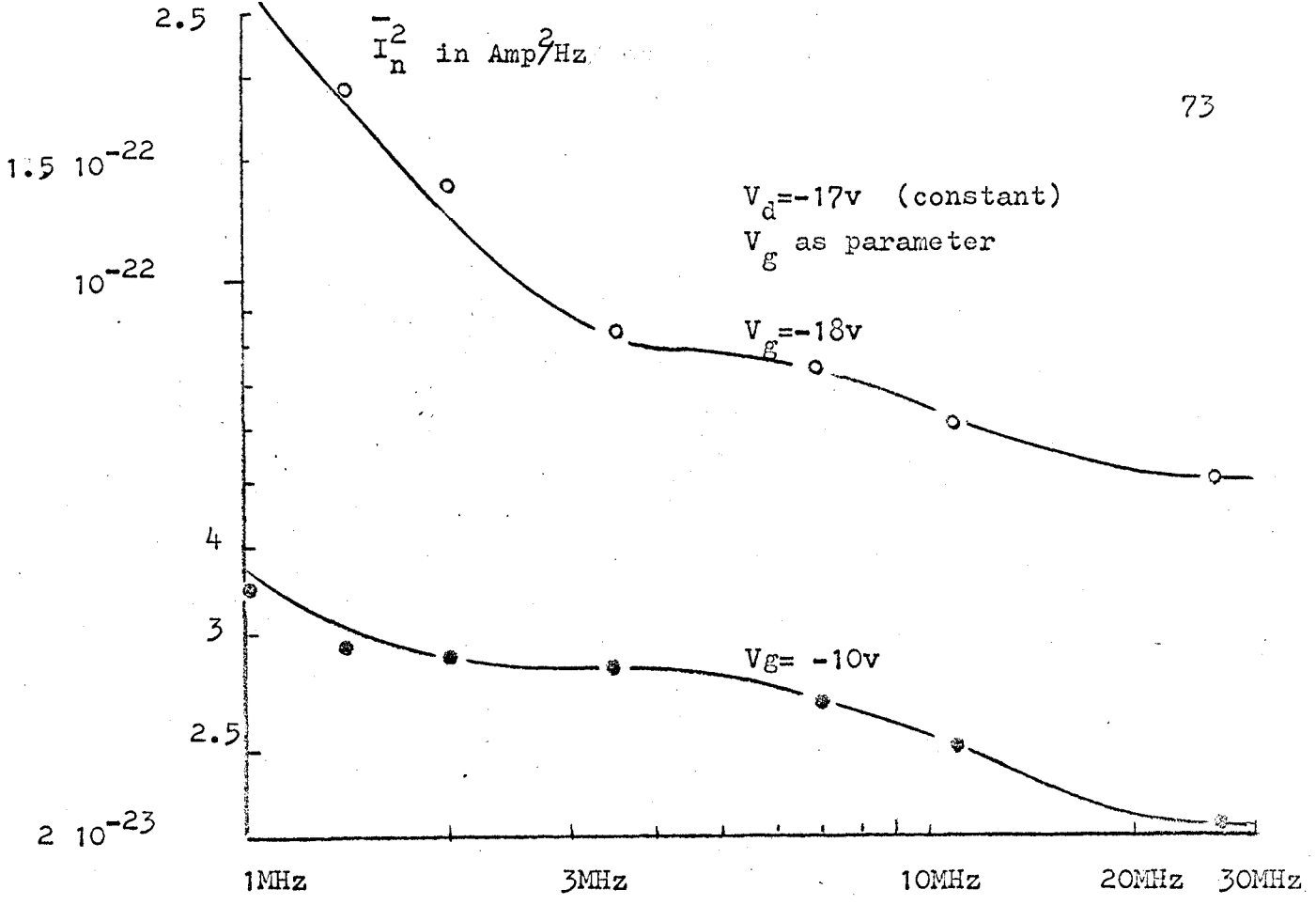


Fig. 4.15 $\overline{I_n^2}$ versus Frequency With V_d Constant and V_g as Parameter

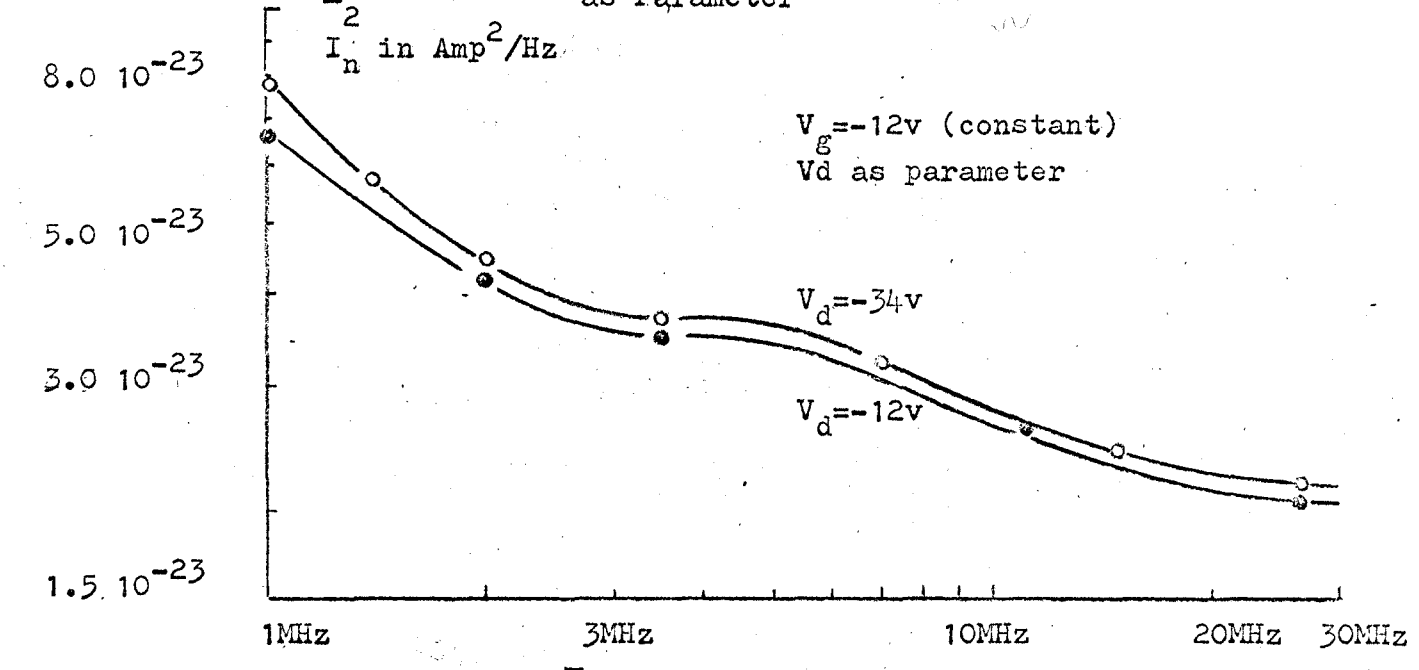


Fig. 4.16 $\overline{I_n^2}$ versus Frequency With V_g constant and V_d as Parameter

CHAPTER V

Conclusions and Discussions

The main results of this investigation have been the derivation and experimental verification of a small-signal circuit model and noise model for the MOS FET.

The d.c. measurements of the device showed that the MOS FET has a square-law characteristic as analysis predicted. The measured Y-parameters were found to agree with the suggested circuit model at least from 15 KH_z to 5 MH_z. and therefore the suggested circuit model can very well represent the real device in this frequency range.

The noise-generating mechanisms in semiconductors have been reviewed and the noise characterization of a noisy four-terminal device discussed. Possible noise theories for MOS devices have been investigated and a noise model derived by assigning a noise current generator to the drain-source output with the input noise associated with the gate neglected. The output current noise generator represents the thermal noise associated with the channel conductance. From the experimental results, it was found that the output noise current is limited by thermal noise beyond $\frac{1}{f}$ and hump regions. The low-frequency noise can be included in the noise model by using an empirical formula. An equivalent noise

resistance R_n which is of the order of 10^3 ohms in the thermal noise region, was calculated from the noise model. This can be compared to the junction-gate FET for which R_n at saturation is given by[8]

$$R_n = \frac{Q(1,y)}{g_m} = \frac{0.60 \to 0.67}{g_m}$$

If operated under same g_m both types of FETs will give the same equivalent noise resistance, and therefore, there is not much choice between these two devices if thermal noise is the only concern. However, the MOS FET has a $\frac{1}{f}$ noise spectrum which extends to much higher frequencies and which would limit its low-noise usefulness to the 30 MH_z or higher frequency region. This statement holds for low impedance sources only. For vacuum tube triodes, $R_n \cong \frac{2.5}{g_m}$, and thus the MOS FET should be less noisy than vacuum tubes with the same transconductance g_m. From the output noise current $\overline{i_n^2}$ versus frequency measurements, it was found that the low-frequency noise corner frequency is approximately 2 MH_z under a typical operating condition and will not change much with varied gate bias voltage V_g. It was also found that output noise current does not change much with V_d, but does change considerably when V_g is varied. In other words, the output noise current is more sensitive to gate bias variations.

Although the method of noise measurement used in this study is not very accurate, it is a commonly used method for minimizing the

background noise problem. From the expression (Eq. 4-44)

$$\overline{i_n^2} = 2eI_{dc}\left[\frac{\Theta_2 - \Theta_5}{\Theta_1 - \Theta_2} - \frac{\Theta_3 - \Theta_5}{\Theta_4 - \Theta_3}\right]$$

it can be seen that if the background noise (Θ_5) is minimized (by using a very low-noise preamplifier) then

$$\overline{i_n^2} \approx 2eI_{dc}\left[\frac{\Theta_2}{\Theta_1 - \Theta_2} - \frac{\Theta_3}{\Theta_4 - \Theta_3}\right]$$

$$= 2eI_{dc}\left[\frac{1}{\frac{\Theta_1}{\Theta_2} - 1)} - \frac{1}{\frac{\Theta_4}{\Theta_3} - 1)}\right]$$

a better experimental accuracy can be obtained if $\frac{\Theta_4}{\Theta_3} >> \frac{\Theta_1}{\Theta_2} >> 1$. Normally $\Theta_1 > \Theta_4$, therefore Θ_2 should be ideally much larger than Θ_3. A large error may therefore be introduced if the backgroun noise is appreciable at some frequency such that the readings Θ_2 and Θ_3 are almost equal. Thus, in order to increase the experimental accuracy, a lower-noise, high-gain preamplifier should be used (the voltage gain of the preamplifier used in this measurement is 100) to minimize the background noise effect.

Suggestions for Further Studies

No attempt has been made to include noise factor calculations or measurements in this thesis. The method of calculating the noise factor and its optimization is straightforward once the device noise model has been

obtained and has been well discussed and presented in the literature. Noise figure measurements at high frequencies could be used to study whether the input noise of the device remains negligible.

As for the device circuit model, the Y-parameter measurements may be extended to high frequencies where the actual cut-off frequency of the device can be determined (g_m drops to $\frac{1}{2}\, g_m$). For high frequency Y-parameter measurements, the stray capacitance and inductance can be troublesome, but this problem may be solved by using printed-circuit-board techniques.

As for the device noise model, further studies may be directed toward a better understanding of the low-frequency noise in the $\frac{1}{f}$ region, the effect of temperature on the humps observed in the $\overline{i_n^2}$ spectrum at middle frequencies, the measurement of input noise at high frequencies and the possible correlation between the input and output noise current generators.

REFERENCES

1. J. E. Lilienfeld, U.S. Patent No. 1745175, filed October 8, 1926; granted January 28, 1930.

2. W. Shockley and G. L. Pearson, "Modulation of Conductance of Thin Films of Semiconductors by Surface Charges", Phys. Rev., Vol. 74, pp. 232-233; July, 1948.

3. W. Shockley, "A Unipolar Field-Effect Transistor", Proc. IRE, Vol. 40, pp. 1365-1376; November, 1952.

4. D. Kahng and M. M. Atalla, "Silicon-Silicon Dioxide Field-Induced Surface Devices", Solid-State Device Research Conference, Pittsburgh, Pa., June, 1960.

5. P. K. Weimer, "An Evaporated Thin Film Triode", Solid-State Device Research Conference, Stanford University, California, June 1961.

6. S. R. Hofstein and F. P. Heimen, "The Silicon Insulated Gate Field-Effect Transistor", Proc. IEEE, Vol. 51, pp. 1190-1202; Sept. 1963.

7. E. Keonjian, Ed., "Principle of Microelectronic Engineering" (Book) Chapter 5, McGraw-Hill Book Co., Inc., New York, N.Y., 1962.

8. A. van der Ziel "Thermal Noise in Field-Effect Transistors", Proc. IRE, Vol. 50, pp. 1808-1812, August, 1962.

9. C. T. Sah, "Characterisitics of the Metal-Oxide-Semiconductor Transistor," IEEE Trans. on Electron Devices, Vol. ED-11, pp. 324-345, July, 1964.

10. G. T. Wright, Proc. IEEE, Vol. 51, p. 1642; 1963.

11. A. W. Lo, et al "Transistor Electronics" (Book), Prentice-Hall Inc., Englewood Cliffs N.J., 1957.

12. Fairchild Semiconductor "Preliminary Specification for FI-100", October, 1964.

13. A. G. Jordan and N. A. Jordan "Theory of Noise in MOS Devices" Westinghouse Scientific Paper 64-1F1-209-P1, August 31, 1964.

14. C. T. Sah "Theory and Experiments on the $\frac{1}{f}$ Surface Noise of MOS Insulated Gate FETs" Solid-State Device Research Conference, Boulder, Colorado, July 1964. Only abstract published on IEEE Trans. on Electron Devices, Vol. ED-11, pp. 534-535, November, 1964.

15. D. N. Nicol, "Noise in MOS Field-Effect-Transistors", IEEE Canadian Electronics Conference Digest, IEEE Cat. No. F17, pp. 52-53, October, 1965.

16. N. Nyquist, "Thermal Agitation of Electric Charge in Conductors" Phys. Rev., Vol. 32, p. 110, July, 1928.

17. W. Schottky, "Uber Spontane Stromschwankungen in Verschienden Elektrizitatsleitern" Ann. d. Phys. (Leipzig) Vol. 57, p. 541 1918.

18. F. J. Hyde, "The Physical Basis of Noise", A chapter of "Noise in Electronic Devices" (Book) Ed. by the Institute of Physics and Physical Society, Chapman and Hall, Ltd., London, 1961.

19. W. Shockely "Eletrons and Holes in Semiconductors" (Book) D. Van Nostrand, New York, 1950.

20. A. van der Ziel, "On the Noise Spectra of Semi-conductor Noise and of Fliker Effect", Physica, Vol. 16, p. 359, 1950.

21. F. K. DuPre, Phys. Rev. Vol. 78, p. 615; 1950.

22. A. L. McWhorter, "$\frac{1}{f}$ Noise and Related Surface Effects in Germanium" Sc.D. Thesis, Electrical Engineering Department; MIT; 1955.

23. T. K. Watkins, Proc. Phys. Soc., Vol. 73, p.59; 1959.

24. H. A. Haus, et al, "IRE Standards on Methods of Measuring Noise in Linear Twoports, 1959", Proc. IRE, Vol. 48, pp. 60-68, January, 1960.

25. K. Lehovec and Sloboskoy, "Impedance of Semiconductor-Insulator-Metal Capacitor", Solid-State Electronics, Vol. 7, pp. 59-79, July 1964.

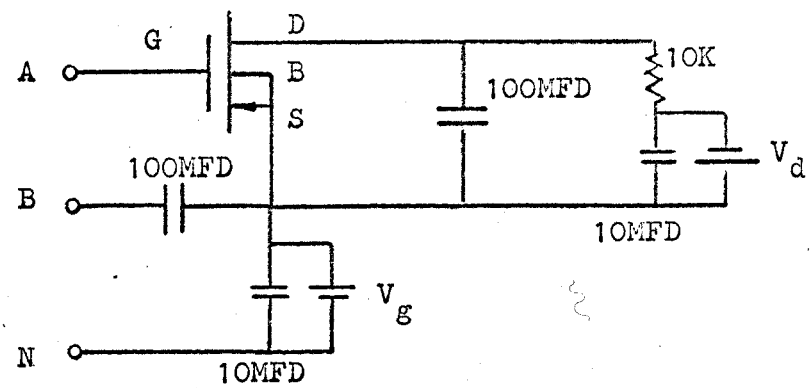
26. W. Shockely and W. T. Read, Jr., "Statistics of Recombination of Holes and Electrons", Phys. Rev., Vol. 87, pp. 835-842; September 1952.

27. P. Lauritzen and C. T. Sah, "Low-Frequency Recombination-Generation Noise in Silicon FETs" Solid-State Device Research Conf., Lansing, Mich., 1963.

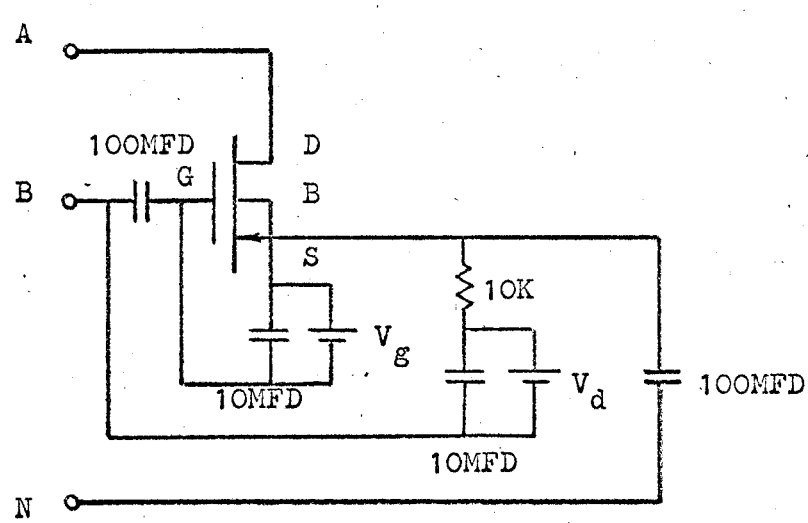
APPENDIX A

Adaptor Circuits for Common-Source Y-Parameter Measurement

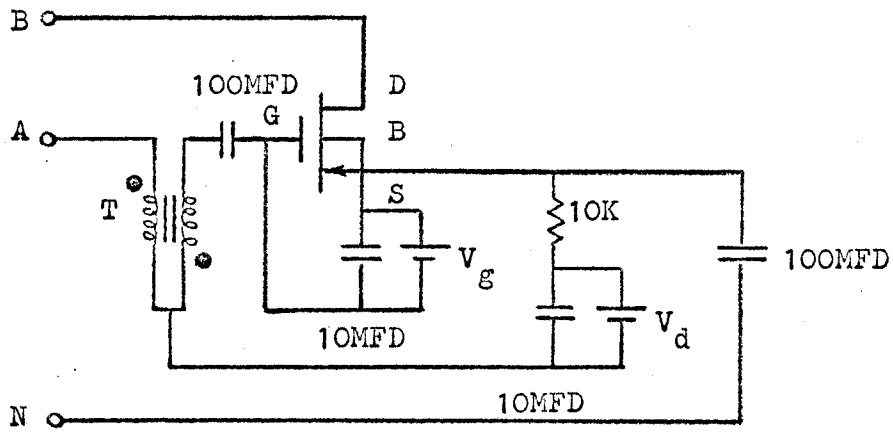
(1) Adaptor Circuit for Y_{11} Measurement



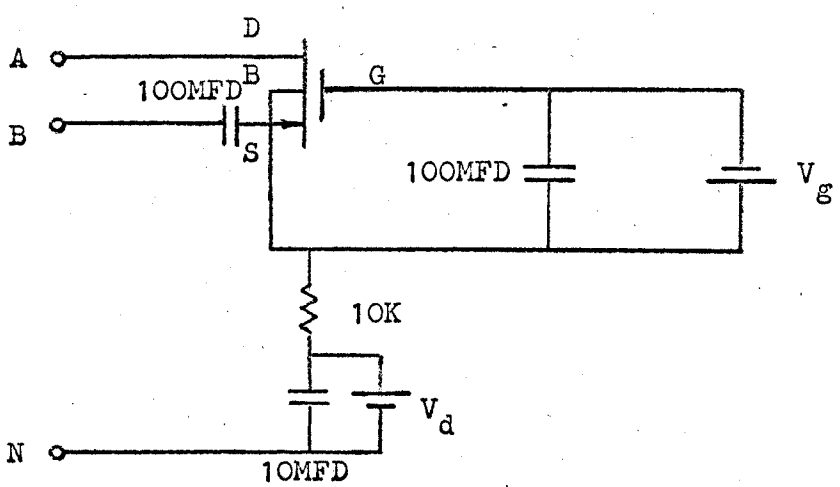
(2) Adaptor Circuit for Y_{12} Measurement



(3) Adaptor Circuit for Y_{21} Measurement



(4) Adaptor Circuit for Y_{22} Measurement



APPENDIX B

Proof of Eq. (4-8), the Noise Factor in Terms of Y-parameters, Noise Current and Source Admittance

$$F = 1 + \frac{\left| i_{n1} + \left(\frac{Y_{11} + Y_s}{Y_{21}}\right) i_{n2} \right|^2}{4kTG_s\, f} \qquad (4\text{-}8)$$

Proof: Although Eq. (4-8) can be shown by employing small-signal nodal equations, it is more clear and straightforward to use Eq. (3-19) i.e.

$$Y_{21} = \frac{\partial I_d}{\partial V_g} \Big|_{V_d = 0} \qquad (B\text{-}1)$$

Thus the equivalent noise voltage of i_{n2}, referred to the input, may be written as

$$e_n = \frac{i_{n2}}{Y_{21}} \qquad (B\text{-}2)$$

Thus e_n may then be transformed into noise current in input circuit as

$$i_n = e_n(Y_{11} + Y_s) = \left(\frac{Y_{11}+Y_s}{Y_{21}}\right) i_{n2} \qquad (B\text{-}3)$$

Thus the total equivalent noise current in the input circuit is

$$\overline{i_{eq}^2} = \overline{i_s^2} + \left| i_{n1} + \left(\frac{Y_{11} + Y_s}{Y_{21}}\right) i_{n2} \right|^2 \qquad (B\text{-}4)$$

Since i_{n1} and i_{n2} may correlate to each other but they are independent of i_s.

Then from definition of noise factor[24], one obtains

$$F = \frac{\overline{i_{eq}^2}}{i_s^2}$$

$$= 1 + \frac{\left|i_{n1} + \left(\frac{Y_{11}+Y_s}{Y_{21}}\right) i_{n2}\right|^2}{4kTG_s\Delta f} \qquad \text{(B-5)}$$

QED

BIBLIOGRAPHY

Papers concerning MOS devices and associated noise studies are arranged chronologically below: papers which deal with noise aspect are indicated thus *.

1926

1. J. E. Lilienfeld, U.S. Patent 1,745,175, filed October 8, 1926; granted Jan. 28, 1930.

1935

2. O. Heil, "Improvements in or Relating to Electrical Amplifiers and Other Control Arrangements and Devices", British Patent 439,457, filed Mar. 4, 1935; granted Dec. 13, 1935.

1948

3. W. Shockley and G. L. Pearson, "Modulation of Conductance of Thin Films of Semiconductors by Surface Charges", Phys. Rev. Vol. 74, Pg. 232-233, July 1948.

1959

4. M. M. Atalla, et al, "Stabilization of Silicon Surfaces by Thermally Grown Oxides", Bell Sys. Tech. J., Vol. 38, pp 749-783; May 1959.

5. J. L. Moll, "Variable Capacitance with Large Capacity Change", 1959 IRE WESCON Convention Record, Part 3, pp 32-36, Aug. 1959.

6. W. G. Pfann and C. G. B. Garrett, "Semiconductor Varactors Using Surface Space-Charge Layers", Proc. IRE (Correspondence) Vol. 47, pp. 2011-2012, Nov. 1959.

1960

7. D. Kahng, "Electrical Field Controlled Semiconductor Devices," U.S. Patent 3,102,230 filed May 31, 1960, granted Aug. 1963.

8. D. Kahng and M. M. Atalla,"Silicon-Silicon Dioxide Field Induced Surface Devices", IRE-AIEE Solid-State Device Research Conference, Pittsburgh, Pa., June 1960.

*9. A. U. MacRae, et al, "Surface-Dependent $\frac{1}{f}$ Noise in Ge", Phys. Rev. Vol. 119, pp.62-69, July 1960.

10. M. M. Atalla, "Semiconductor Triode", U.S. Patent 3,056,888, filed Aug. 17, 1960, granted Oct. 2, 1962.

11. R. Pick and M. Savelli, "The Study of Surface Phenomena in Semiconductors by Field-Effect Techniques," (in French), J. Phys. Radium, Vol. 21, pp. 743-750, Oct. 1960.

1961

12. L. M. Terman, "An Investigation of Surface States at a Silicon/Silicon-Oxide Interface Employing MOS Diodes", Stanford Electronics Lab. Tech. Rep. 1655-1, Feb. 23, 1961.

13. P. K. Weimer, "An Evaporated Thin Film Triode", Solid-State Device Research Conference, Stanford University, Calif., June 1961.

14. H. K. J. Ihantola, "Design Theory of a Surface-Field-Effect Transistor," Stanford Electronics Lab. Tech. Rep. 1661-1, Aug. 1961.

15. C. T. Sah, "A New Semiconductor Tetrode, the Surface-Controlled Transistors", Proc. IRE, Vol. 49, pp. 1623-1634; Nov. 1961.

1962

16. C. T. Sah, "Effect of Surface Recombination and Channel on p-n Junction and Transistor Characteristics", IRE Trans. on Electron Devices, Vol. ED-9 No. 1, pp 94-108, Jan. 1962.

17. R. Linder, "Semiconductor Surface Varactor," Bell Syst. Tech. J., Vol. XLI, No. 3, pp.803-831, May 1962.

1963

18. F. M. Wanless and C. T. Sah, "Nano-watt Logic Using Field-Effect Metal-oxide-Semiconductor Triodes," IRE International Solid-State Conference, Lewis Winner, New York, N.Y. 1963.

19. C. T. Sah and F. M. Wanless, "Metal-Oxide Semiconductor Field-Effect Devices for Micropower Logic Circuitry," International Microwatt Circuit Symposia in Europe, July, 1963.

20. S. R. Hofstein and F. P. Heiman, "The Silicon Insulated-Gate Field-Effect Transistor," Proc IEEE, Vol. 51, pp. 1190-1202, Sept. 1963.

21. K. Lehovec, et al, "Field Effect Capacitance Analysis of Surface States on Silicon", Phys. Stat. Sol. Vol. 3, pp. 447-464, 1963.

22. H. Edagawa, et al, "The Quantitative Evaluation of n-type Conversion of Thermally Oxidized Si Surfaces," Japan J. Appl. Phys. (Correspondance) Vol. 2, p. 814, 1963.

23. J. T. Wallmark, "The Field Effect Transistor, A Review", RCA Review, pp. 641-660, Dec. 1963.

1964

24. K. Lehovec and A. Slobodskoy, "Impedance of Semiconductor-Insulator-Metal Capacitors," Solid-State Electronics, Vol. 7, pp. 59-70, Jan. 1964.

25. G. T. Wright, "Theory of the Space-Charge-Limited Surface-Channel Dielectric Triode", Solid-State Electronics, Vol. 7, pp. 167-175, Feb. 1964.

26. C. Goldberg, "Pinch off in Insulated-Gate Field-Effect Transistors", Proc. IEEE (Correspondance) Vol. 54, pp. 414-415, Apr. 1964.

27. R. D. Lohman, "Some Application of Metal-Oxide-Semiconductors (MOS) to Switching Circuit", Semicond. Prod. Solid State Technol., Vol. 7, No. 5, pp. 31-34, May 1964.

28. H. K. J. Ihantola and J. L. Moll, "Design Theory of a Surface Field-Effect Transistor", Solid-State Electronics, Vol. 7, pp. 423-430, June 1964.

29. C. D. Root and L. Vadasz, "Design Calculations for MOS FETs", IEEE Trans. on Electron Devices, Vol. ED-11, No. 6, pp. 294-299, June 1964.

30. F. P. Heiman, "Surface States and Related Effects Associated with a MOS Structure", Ph.D. dissertation, Princeton University, Princeton N. J., 1964.

31. S. R. Hofstein, "Physical Limitations Associated with Some Surface Effect Devices", Ph.D. dissertation, Princeton University, Princeton, N. J. 1964.

32. L. Blaser and E. Cummins, "Designing FETs and MOSTs into A-M Radios", IEEE Trans. on Broadcast and TV Receivers, Vol. BTR-10, No. 2, July, 1964.

33. C. T. Sah, "Characteristics of the MOS Transistors", IEEE Trans. on Electron Devices, Vol. ED-11, No. 7, pp. 324-345, July 1964.

34. F. P. Heiman and G. Warfield, "The Effect of Oxide Traps on the Performance of MOS Devices", Solid-State Research Conference, Boulder, Colorado, July 1964 (IEEE Trans. on Electron Devices, Vol ED-12, No. 4 April, 1965).

*35. A. G. Jordan and N. A. Jordan, "Theory of Noise in MOS Devices", ibid, July 1964 (Also appeared as Westinghouse Scientific Paper 64-1F1-209-p1, Aug. 31, 1964 and Published in IEEE Trans. on Electron Devices, Vol. ED-12, No. 3, pp. 148-156 Mar, 1965).

*36. C. T. Sah, "Theory and Experiments on $\frac{1}{f}$ Surface Noise of MOS FETs", ibid, July 1964.

37. K. H. Zaininger and G. Warfield, "Hydron Induced Surface States at an Si-SiO_2 Intersurface," Proc. IEEE (Correspondance), Vol. 52, pp. 972-973, Aug. 1964.

38. I. E. Thomas, Jr., and D. R. Young, "Space-Charge Model for Surface Potential Shifts in Silicon Passivated with Thin Isulating Layer," IBM J. Res. Develop., Vol. 8, No. 4, pp. 368-375, Sept. 1964.

39. D. P. Seraphim, et al., "Electrochemical Phenomena in Thin Films of Silicon Dioxide on Silicon", ibid. pp. 400-409, Sept. 1964.

40. F. Fang, et al, "Carrier Surface Scattering in Silicon Inversion Layer", ibid, pp. 410-415, Sept. 1964.

41. H. S. Lehman, "Chemical and Ambient Effects on Surface Conduction in Passivated Silicon Semiconductors," ibid, pp. 422-426, Sept. 1964.

42. C. T. Sah, et al. "Redistribution of Acceptor and Donor Impurities during Thermal Oxidation of Silicon," J. Appl. Phys. Vol. 35, pp. 2695-2701, Sept. 1964.

43. A. B. Kuper and E. H. Nicollian, "Effect of Oxide Hydration on Surface Potential of Oxidized p-type Silicon", Electrochemical Society Meeting, Washington D.C., Oct. 1964.

44. P. Lamond, et al, "Reliability and Failure Modes in MOS Transistor", IEE Electron Devices Meeting, Washington, D.C., Oct. 1964 (Fairchild Technical Rep. No. 193, Nov. 1964.)

45. C. T. Sah, et al, "A Study of Ion Migration in Thin Insulating Films Using MOS Structure", ibid, Oct. 1964 (J. Appl. Phys. 36, May 1965).

46. C. T. Sah, et al, "Observation of Impurity Redistribution During Thermal Oxidation Using the MOS Structure", ibid, Oct. 1964.

47. C. T. Sah, et al, "Recent Advances in the Understanding of the MOS System", Fairchild Technical Report, Nov. 1964.

48. J. S. MacDougall, "Application of the Silicon Planar II MOS FET", Fairchild Application Bulletin, App-109, Nov. 1964.

49. P. E. Kolk, "The Insulated-Gate FET" Technical Report, KMC Semicond. Corporation, Long Valley, New Jersey, Nov. 1964.

50. "Field Effect Transistors" Ed. by ELECTRONICS Magazine.
Part I, Devices, Vol. 37, No. 30, pp. 45-68, Nov. 30 1964.
Part II, Applications, Vol. 37, No. 31, pp.53-76, Dec. 14, 1964.
Part III, Applications, Vol. 37, No. 32, pp. 45-60, Dec. 28, 1964.

1965

51. C. T. Sah, et al, "Investigation of Thermally Oxidized Surface Using MOS Structure," Solid-State Electronics, Vol. 8, No. 2, pp 145-163, Feb. 1965.

52. S. R. Hofstein and G. Warfield, "Physical Limitations on the Frequency Response of a Semiconductor Surface Inverse Layer," Solid-State Electronics, Feb. 1965.

53. IEEE Trans on Electron Devices, Vol. ED-12, No. 3, Mar. 1965
-- A Special Issue dedicated to research activity in MOS devices.

54. S. R. Hofstein and G. Warfield, "Carrier Mobility and Current Saturation in MOS Transistor", IEEE Trans. on Electron Devices, Vol. ED-12, No. 3, pp 129-138, Mar 1965.

55. F. P. Heiman and H. S. Miller, "Temperature Dependance on n-type MOS Transistors", IEEE Trans on Electron Devices, Vol. ED-12, No. 3 pp 142-148, Mar. 1965.

56. T. J. O'Reilly, "Effect of Surface Traps on Characteristics of Insulated-Gate FETs", Solid-State Electronics, Vol. 8, pp 267-274, Mar. 1965.

57. M. H. White and R. C. Gallagher, "MOS Small-Signal Equivalent Circuit", Proc. IEEE, Vol. 53, pp 314-315 (Correspondance), Mar. 1965.

58. V. G. K. Reddi and C. T. Sah, "Source to Drain Resistance Beyond Pinch-Off in MOS Transistor", IEEE Trans. on Electron Devices, Vol. ED-12, No. 3, pp. 139-141, Mar. 1965.

59. R. A. Hilbourne and J.F. Miles, "The MOS Transistor", Electronic Engineering, Vol. 37, No. 445, pp 156-160, Mar 1965.

60. K. H. Zaininger and G. Warfield, "Limitations of the MOS Capacitance Method for the Determination of Semiconductor Surface Properties", IEEE Trans. Vol. ED-12, No. 4, pp 179-192, April, 1965.

61. C. T. Sah, et al, "Electron and Hole Mobilities in Inversion Layers on Thermally Oxidized Silicon Surface", IEEE Trans. on Electron Devices Vol. ED-12, No. 5, pp 248-254, May 1965.

62. D. M. Griswold, "Characteristics and Applications of RCA Insulated-Gate FETs", IEEE Trans. Vol. BTR-11, No. 2, pp 9-17, July 1965.

63. N. A. Jordan, "Insulated-Gate MOS Transistor as Noise Detector", Rev. of Sci. Inst. Vol. 36, No. 7, pp 1049-1050, July, 1965.

64. H. Beck, et al, "Gallium Arsenide MOS Transistor", Solid-State Electronics, Vol. 8, pp 813-823, 1965.

65. D. R. Nicol, "Noise in MOS FETs", IEEE Canadian Electronics Conference Digest, IEEE Cat. No. F17, paper No. 65102, pp 52-53, Oct. 1965.

66. G. E. Moore, "The MOS Transistor as an Individual Device and in Integrated Arrays", 1965 NEC (21st Annual National Electronics Conference) Chicago, Ill., Oct. 1965.

67. H. C. Lin, et al, "MOS Structure for Passive and Active Elements in Integrated Circuits", ibid, Oct. 1965.

68. J. D. Trotter, "Micro-power Digital Circuitry Using Clocked MOST Devices," ibid. Oct. 1965.

*69. A. van der Ziel, "Noise in MOS-type FET," ibid Oct. 1965.

70. N. Ditrick, et al "A Low Power MOS Tetrode", International Electron Devices Meeting, Washington, D.C., Oct. 1965.

*71. R. Q. Lane, "R.F. Noise in N'MOST Transistors", ibid , Oct. 1965

72. F. E. Capocaccia, "Large Signal Transient Behaviour of MOS Transistors", ibid, Oct. 1965.

73. R. Zuleeg, "A Silicon, Planar Space-Charge Limited Current Tetrode", ibid, Oct. 1965.

74. V.G.K. Reddi, "Tunable High-Pass Filter Characteristics of a Special MOS Transistor", IEEE Trans. on Electron Devices, Vol. ED-12, No. 11 pp 581-589, Nov. 1965.

75. M. M. Mitchell and N. H. Dirtrick, "Stability Effects in MOS Enhancement Transistors", Solid-State Design, Vol. 6, No. 11, pp 19-22, Nov. 1965.

76. S. G. Freshour, "Capacitively Tuned FET and MOS Oscillators", Solid-State Design, Vol. 6, No. 12, pp 28-32, Dec. 1965.

77. T. J. O'Reilly, "The Transient Response of Insulated-Gate FETs," Solid-State Electronics, Vol. 8, No. 12, pp 947-956, Dec. 1965.

78. J. R. Hauser, "Small Signal Properties of Field-Effect Devices", IEEE Trans. on Electron Devices, Vol. ED-12, No. 12, pp. 605-618, Dec. 1965.

79. A. S. Grove, et al, "The Origin of Channel Currents Associated with p^+ Regions in Silicon", IEEE Trans on Electron Devices, Vol. ED-12, No. 12, pp 619-625, Dec. 1965.

1966

80. D. P. Stokesberry, "A Large Signal IGFET DC Source Follower," Proc. IEEE, Vol. 54, No. 1, pp 66 Jan. 1966.

81. N. C. Tombs, et al, "A New Insulated-Gate Silicon Transistor", (i.e. MNS, Metal-Nitride-Semiconductor Transistor), Proc. IEEE Vol. 54, No. 1, pp 87-88, Jan. 1966.

82. Z. Lukes, "Characteristics of the MOS Transistor in the Common-Gate Electrode Arrangement", Solid-State Electronics, Vol. 9, No. 1 pp 21-33, Jan. 1966.

83. W. Fisher, "Equivalent Circuit and Gain of MOS FET," Solid-State Electronics, Vol. 9, No. 1, pp 71-81, Jan. 1966.

84. J. A. Geurst, "Theory of Insulated-Gate FET Near and Beyond Pinch-Off", Solid-State Electronics, Vol. 9, No. 2, pp 129-142, Feb. 1966.

85. J. Conragan and R. S. Muller, "Insulated-Gate FET Using Single Crystal Cadmium Sulfide", Solid-State Electronics, Vol. 9, No. 2, p. 182, Feb. 1966.

86. IEEE Trans. on Electron Devices, Vol. ED-13, No. 2, Feb. 1966 -- a special issue denoted to MOS Structures.

87. M. H. White, "A Voltage-Controlled MOS-FET Integrator", Proc. IEEE, Vol. 54., No. 3, p. 421, Mar. 1966.

88. J. Lindmayer, "Field-Effect Studies of the Oxidized Silicon Surface" Solid-State Electronics, Vol. 9, No. 3, pp 225-235, Mar. 1966.

89. N. Goldsmith, et al, "Determination of Silicon Oxide Thickness", Solid-State Electronics, Vol. 9, No. 4, pp 331-332, Apr. 1966.

90. C. T. Sah, et al, "The Effects of Fixed Bulk Charge on the Characteristics of MOS Transistor," IEEE Trans. on Electron Devices, Vol. ED-13, No. 4, April, 1966.

*91. C. T. Sah, et al, "The Effects of Fixed Bulk Charge on the Thermal Noise in MOS Transistors", IEEE Trans. on Electron Devices, Vol. ED-13, No. 4, April, 1966