# SOLID STATE SPEED CONTROL OF A SQUIRREL-CAGE INDUCTION MOTOR

# SOLID STATE SPEED CONTROL OF A SQUIRREL-CAGE INDUCTION MOTOR

by

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ABSTRACT

The speed of a squirrel-cage induction motor is controlled by varying the supply frequency. The design of an SCR controlled inverter, using gating from a logic unit to give a variable-frequency power-level output, is described.

ACKNOWLEDGEMENT

I wish to express my appreciation to Professor C. D. diCenzo for his interest, co-operation and encouragement.

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# INTRODUCTION

The speed of an AC induction motor can be adjusted by varying the stator voltage, changing the rotor impedance, altering the supply frequency, or introducing an external voltage into the rotor circuit. It is the purpose of this thesis to examine the use of an SCR inverter, using logic control, for the provision of a variable frequency at power-levels to control a squirrel-cage induction motor.

The characteristics and limitations of the SCR are reviewed in Chapter 1, and design criteria for their application established. The design of the basic inverter is covered in Chapter 2. This design is directly applicable to a 4 KVA, 3-phase, induction machine. In Chapter 3, the foundation for 3-phase inverter waveforms is laid and the design of the timing, shaping and amplification of the triggering pulses covered. Chapter 4 presents a breakdown of the losses associated with the operation of the induction motor with nonsinusoidal applied voltages.

# CHAPTER ONE

## THEORY OF THE SCR

General:

The silicon controlled rectifier (SCR) is a p-n-p-n semiconductor with two stable states. It has three terminals (anode, cathode, and control gate) and is a unidirectional device -- current flows from anode to cathode only.

The SCR can be visualized as consisting of two transistors, a p-n-p and an n-p-n interconnected to form a regenerative feedback pair, as shown in Figure 1. Current gain around the internal feedback loop (G) is equal to the product of the individual transistor common-emitter current gains, $h_{fe1}$ and $h_{fe2}$. Letting $I_{co1}$ and $I_{co2}$ be the collector-to-base leakage currents of the n-p-n and p-n-p sections respectively, then

for the n-p-n section: $I_{c1} = h_{fe1} (I_{c2} + I_{co1}) + I_{co1}$

for the p-n-p section: $I_{c2} = h_{fe2} (I_{c1} + I_{co2}) + I_{co2}$

and the total anode current $I_a = I_{c1} + I_{c2}$.

Solving for $I_a$ gives

$$I_a = \frac{(1 + h_{fe1})(1 + h_{fe2})(I_{co1} + I_{co2})}{1 - h_{fe1} \cdot h_{fe2}} \qquad \ldots 1$$

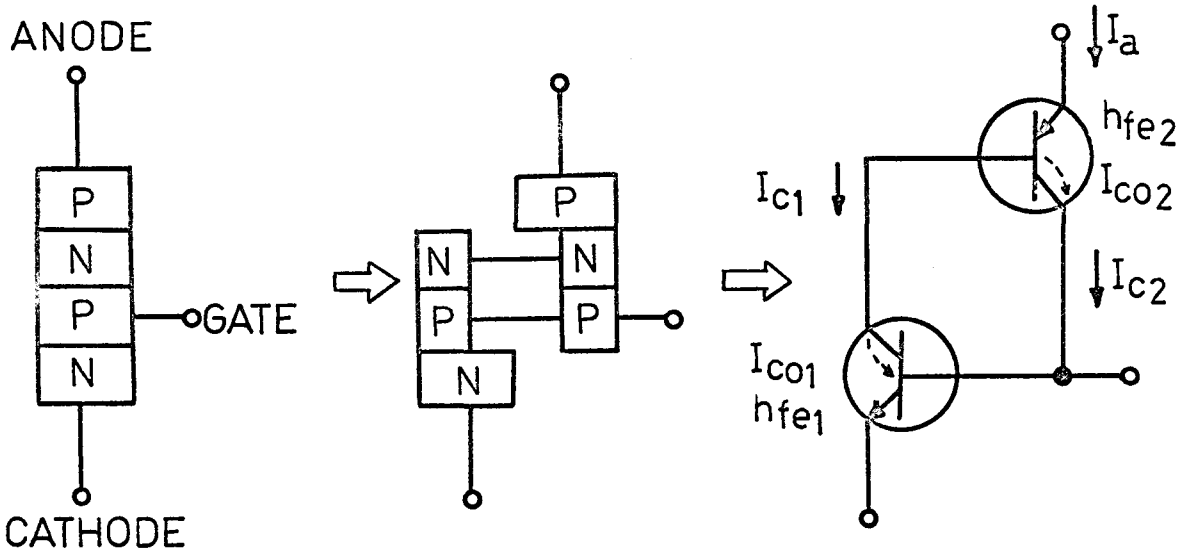



Figure 1. Two transistor analogue of SCR.

When forward bias is applied (positive anode-to-cathode voltage), both $h_{fe1}$ and $h_{fe2}$ are low, and the loop gain G is much less than unity. The denominator of Equation 1 approaches one and the anode current $I_a$ is approximately the sum of the individual leakage currents $I_{co1}$ and $I_{co2}$. In this case, the p-n-p-n structure is in its "forward blocking" or high impedance "off" state. If the loop gain G is raised to unity, the switch to the "conducting", or low impedance "on" state is initiated. It is seen from Equation 1 that as $h_{fe1} \cdot h_{fe2} \rightarrow 1$, then $I_a \rightarrow \infty$. From a physical point of view, as the loop gain approaches one and the circuit starts to regenerate, each transistor drives the other into saturation. At saturation, all junctions are forward biased and the overall potential drop across the device approximates that of a single p-n junction. The anode current $I_a$ is now limited only by the external circuit.

SCR Turn On:

The SCR is turned on by raising the product $h_{fe1} \cdot h_{fe2}$ to unity. There are several mechanisms available for increasing $h_{fe}$ in a transistor and all make use of the emitter-current dependence of $h_{fe}$.

In most silicon transistors, $h_{fe}$ is quite low at low emitter currents and increases rapidly with increasing emitter current (Figure 2). This is due to the presence in the silicon of special impurity centers. Therefore, any

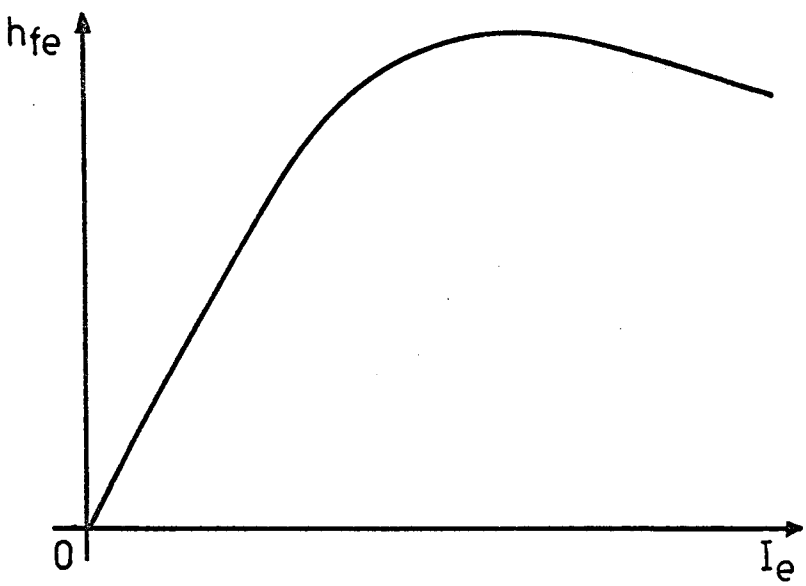



Figure 2. Emitter-current dependence of $h_{fe}$ in a silicon transistor.

mechanism which causes an increase in transistor emitter current is potentially capable of turning on the p-n-p-n device. The more important of these mechanisms are:

1. Voltage. If the collector-to-emitter voltage of a transistor is increased, eventually a point is reached where the energy of the (leakage) current carriers arriving at the collector junction is sufficient to dislodge additional carriers. This process is regenerative and the whole junction goes into a form of avalanche breakdown characterized by a sharp increase in collector current. In the SCR p-n-p-n structure, the avalanche current makes G → 1 and switching to the "on" state takes place. This mechanism is normally used to switch four layer diodes into conduction.
2. Rate of change of voltage (dv/dt). All p-n junctions have capacitance. The charging current flowing from anode-to-cathode in a p-n-p-n device caused by a time rate of change of voltage is given by $i = C\ dv/dt$. If the charging current i is great enough to cause G → 1, then the device will switch on. The phenomenon is known as the "dv/dt effect".
3. Temperature. When operated at higher temperatures, the leakage current in a reverse biased silicon p-n junction approximately doubles with every 8°C increase in junction temperature. If the leakage current so generated rises sufficiently to cause G → 1, then switching on occurs.

4. Transistor Action. In a conventional transistor, collector current is increased by temporarily injecting additional ("gate") current carriers into the base region. This mechanism is normally employed to turn on SCR's and other p-n-p-n devices with an external connection ("gate" lead) to one or more of the transistor bases.
5. Radiant Energy (light). If incident radiant energy within the spectral bandwidth of silicon impinges on and penetrates into the lattice, a considerable number of hole-electron pairs will be generated. This causes an increase in the leakage current and, if it is sufficient to cause $G \rightarrow 1$, then switching on will occur. This mechanism makes possible the light activated SCR (LASCR). The LASCR is provided with a translucent "window" in order that "light" may reach the silicon pellet.

SCR Turn Off:

Once the SCR has been triggered to the high conduction state, the gate loses control, and the anode current must be reduced below the minimum holding level to turn the device off.

When the SCR is in the high conducting state, each of the three junctions of Figure 3 are forward biased and the two base regions ($B_p$ and $B_n$) are heavily saturated with

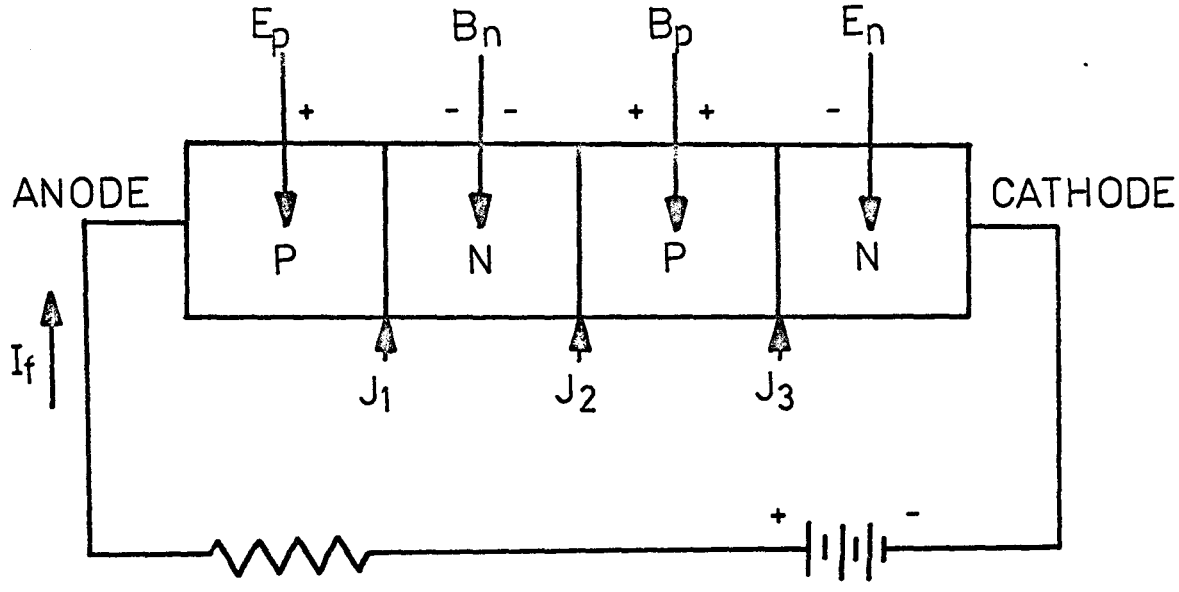



Figure 3. SCR biased in conducting state (gate open circuited).

holes and electrons -- stored charge. To turn the SCR off in minimum time, a reverse anode-to-cathode voltage must be applied. This reverse voltage causes the holes and electrons in the vicinity of the two end junctions ($J_1$ and $J_3$) to diffuse to these junctions and result in a reverse current in the external circuit. The voltage drop across the device will remain at about +0.7 volts as long as an appreciable reverse current flows. When the holes and electrons in the vicinity of $J_1$ and $J_3$ have been removed, the reverse current will cease and the two end junctions will assume a blocking state. The reverse voltage across the device now increases to a value determined by the external circuit. Recovery of the SCR is, however, not yet complete, since a high concentration of holes and electrons still exists in the vicinity of the center junction ($J_2$). This concentration decreases by recombination and is largely independent of the external bias. When the hole and electron concentration at $J_2$ has decreased sufficiently, $J_2$ will regain its blocking state and a forward voltage, less than the breakover voltage, can be applied without causing the SCR to turn on. The total time that elapses from the cessation of forward current to safe reapplication of forward voltage is called the SCR "turn off time" ($t_o$) and is in the order of 10 - 150 microseconds.

There are two basic methods for "commutation" of the SCR as the turn off process is called. The first is to

interrupt the current through the device by means of a switch. The switch must be operated for the required turn off time. This type of operation causes the SCR to see high values of dv/dt. When the method of current interruption is not acceptable, then "forced commutation" must be used. In forced commutation, current is switched from some energy source so as to force more current through the SCR in the reverse direction than is trying to flow in the forward direction. Forced commutation tends to give shortened device turn off time.

SCR Characteristics:

The V-I characteristic of a typical SCR is illustrated in Figure 4. Increasing the forward voltage in the forward blocking region does not tend to increase the leakage current until the point is reached where avalanche multiplication takes place. Beyond this point, the leakage current rapidly increases until the total current through the device is sufficient to raise the loop gain G to unity. Here the device will go into the high conduction region, if the anode current remains above the minimum "holding current" value. If the anode current falls below the holding current level, the SCR reverts to its forward blocking state. When the anode-to-cathode potential is reversed, the p-n-p-n structure becomes two reverse-biased p-n junctions in series, and exhibits characteristics

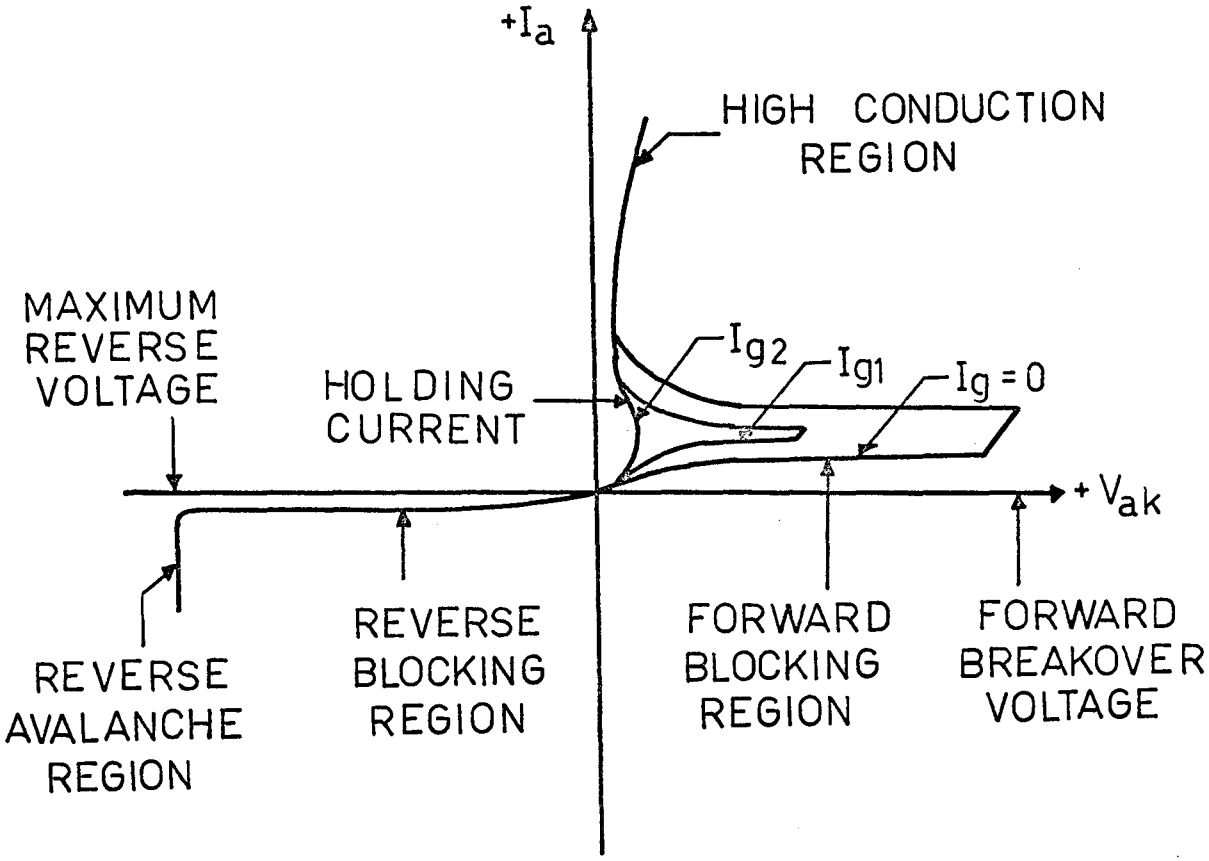



Figure 4. V-I characteristics of an SCR.

similar to that of an ordinary back-biased silicon diode. In most commercially available SCR's, the peak reverse voltage is designed to be at least equal to the minimum forward breakover voltage.

When the gate current is increased, the region of the characteristic between breakover current and holding current is narrowed and the forward breakover voltage is reduced. At sufficiently large gate currents, the forward blocking region is removed, and the V-I characteristic becomes that of a p-n diode.

For normal operation, the SCR is biased below the minimum forward breakover voltage, and the device is triggered on by injecting current into the gate. This mode of operation allows the use of a device with a forward breakover voltage much higher than any voltage to be encountered in the circuit, and to use only a moderate amount of triggering power to switch to the high conduction state. Normally, a ten to fifty microsecond gate pulse will initiate conduction.

The gate-cathode V-I characteristics of an SCR are essentially those of a p-n junction diode. Since the increase in $h_{fe}$ with current is utilized, these devices are current-triggered as opposed to voltage triggering in the gas thyratron.

In ordinary three-layer silicon power transistors, it is desirable to have $h_{fe}$ as high as possible in order to

achieve a high current gain. However, high $h_{fe}$ is obtained in most silicon transistors by using a very thin base region, and this very thin base between two low resistivity regions is incompatible with high voltage. In the SCR, the wide base region necessary to achieve low $h_{fe}$ is compatible with high voltages, so that the SCR is inherently a higher voltage device. The wider base region is also an advantage from the standpoint of ease of manufacture and reproducibility of characteristics. One of the major advantages of the SCR over the power transistor is the small amount of drive necessary to achieve full conduction. For many silicon transistors, it is necessary to inject up to half an ampere of continuous base current to conduct 5 amperes from collector to emitter. The amount of current conducted in the SCR is dependent only on the external circuit once the device has been triggered. Typically, a trigger current of 50 ma applied for only a few microseconds is all that is necessary to allow conduction of any current from a few milliamperes to hundreds of amperes. The high current capabilities of the SCR, as contrasted with the transistor, are due to the more effective use of junction area for conduction.

Limitations of SCR's:

The leakage current through an SCR increases with temperature and, consequently, the forward breakover voltage

tends to be quite temperature sensitive. At temperatures high enough above its rated maximum, the SCR loses its ability to block forward voltage and assumes a p-n diode characteristic.

In smaller SCR's, the temperature effect on the breakover voltage can be minimized by extracting the forward leakage current from the gate by negative bias. This prevents current from passing through the emitter of the n-p-n section of the device. This method can be used to actually increase the forward breakover voltage point. On higher current SCR's this method of negative gate current has little effect on the forward blocking characteristics due to the ineffectiveness of the gate in removing the leakage current from the entire broad area of the n-p-n base region.

Transiently, the SCR may be operated beyond its specified maximum operating temperature. The power generated in the junction region of an SCR consists of the following dissipation components.

1. Conduction. The forward conduction loss is the major source of junction heating for normal duty cycles and power frequencies. This loss, in average watts, is the integrated products of the instantaneous anode currents and forward voltage drops. The integration can be performed analytically or graphically, for the type of conduction used, using the forward V-I

characteristic curves for the device.

2. Blocking. The forward and reverse blocking losses are determined by integration of the appropriate blocking V-I curves for the device.
3. Triggering. The gate loss is normally negligible for pulse types of triggering. The loss, however, may become more significant for high duty cycle gate signals, or for SCR's in small packages. The loss can be calculated from the gate V-I curves for the device.
4. Turn on switching. The SCR may be assumed to turn on instantaneously, if the rate-of-rise of anode current (di/dt) is slow compared with the time required for the junctions to reach a state of full forward conduction at uniform current density. When the rate-of-rise of anode current is very rapid compared to the spreading velocity of the turn on process across the junctions, local "hot spot" heating will occur due to the high current density in those junction regions that have started to conduct. When the frequency of switching is increased, the contribution of the per cycle turn on switching loss integrated over the period of one cycle becomes increasingly significant. For very steep (high di/dt) current waveforms or high operating frequencies the turn on switching loss may become the limiting consideration.

The rated junction temperature can be exceeded on a non-recurrent basis for a brief instant to accommodate some fault overloading. Ratings for this type of condition are given by the Surge Current curve and by the $I^2t$ rating for the device. The $I^2t$ ratings apply for non-recurrent overloads shorter than 0.00834 seconds duration (half period of 60 Hz frequency). For such times the SCR behaves essentially like a resistance with a fixed thermal capacity and negligible power dissipating means, and it displays a current capability which can be expressed as a constant $I^2t$, where I is the RMS value of current over an interval t. The foregoing rating assumes that the SCR is in its conducting state and at operating temperature. If the SCR is turned on into a fault, the rated di/dt of the device must not be exceeded.

CHAPTER TWO

# INVERTER DESIGN

## General:

Squirrel-cage induction motors which are to be controlled within a wide speed range, as in the case of DC motors, require a variable frequency power-level supply. This leads to the problem of generating a 3-phase variable frequency and voltage from a direct voltage; for example, with the aid of an inverter. This type of inverter can be designed for high ratings by using SCR's which are commutated by capacitors. Figure 5 shows an example of a generalized rectifier-inverter in a 3-phase bridge connection.

## Motor Equivalent Circuit:

To successfully design an inverter, the load presented to the inverter must first be analyzed. The load — the induction motor — is simply an electric transformer whose magnetic circuit is separated by an air gap into two relatively moveable portions, one carrying the primary (stator) and the other the secondary (rotor) windings.

As with the case of the transformer, the induction motor can be represented by the T-model equivalent circuit,

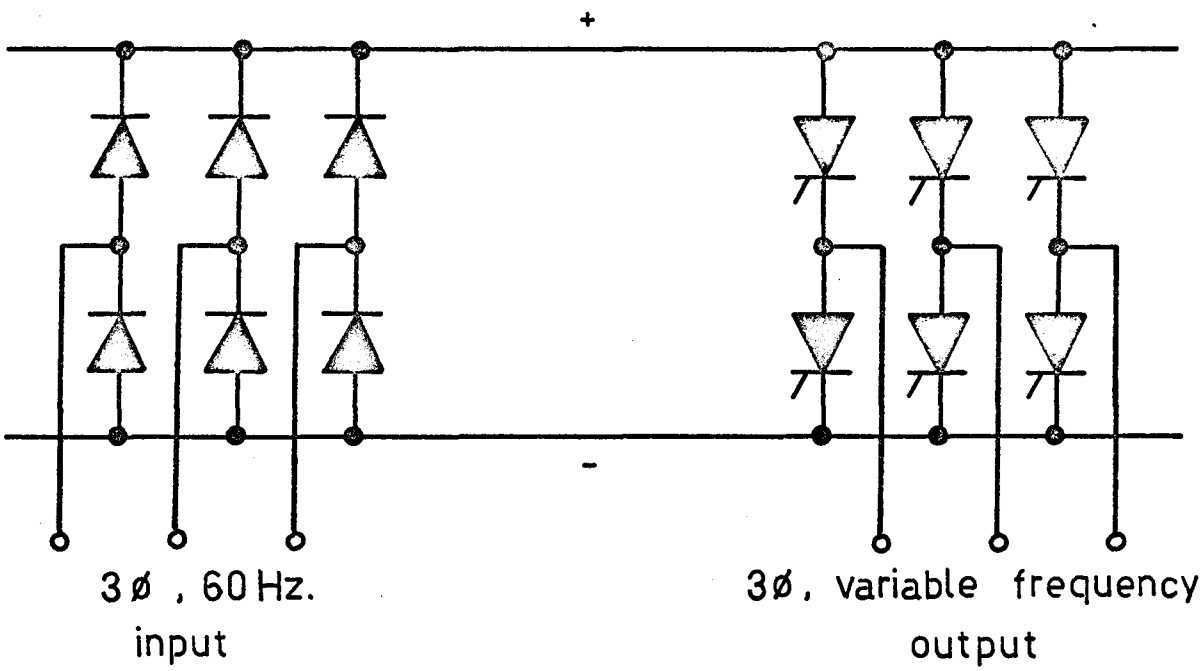



Figure 5. Generalized rectifier inverter.

as shown in Figure 6. In this case,

$E_o$ = applied voltage,

$I_o$ = total applied current,

$I_m$ = magnetizing current,

$I_2$ = rotor current,

$R_1$ = stator resistance,

$R_{fe}$ = iron loss equivalent resistance,

$R_2$ = rotor resistance in stator terms,

$L_1$ = stator leakage inductance,

$L_m$ = magnetizing inductance,

$L_2$ = rotor leakage inductance in stator terms, and

$s$ = slip.

The torque produced by the motor corresponds to the power transferred across the gap by induction. In other words, the torque is proportional to the product of the air-gap flux and the secondary current times the sine of the difference between their respective phase angles. However, the gap flux is proportional to the magnetizing current which, in turn, is directly dependent on the applied voltage and inversely dependent on the source frequency. Consequently to maintain a constant gap flux, a constant volts/hertz ratio must be maintained. This means changing the applied voltage in proportion to a change in frequency.

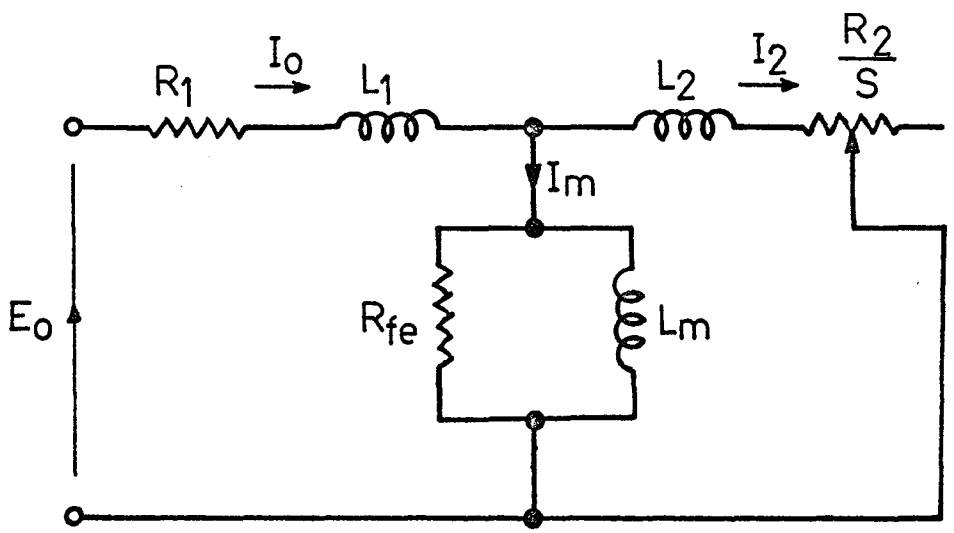



Figure 6. Induction motor equivalent circuit.

Commutation:

The squirrel-cage induction motor offers, primarily, an inductive load to the inverter and this leads readily to a self commutation type of operation. Consider the series circuit illustrated in Figure 7. Elements R and L represent the motor, and element C is the commutation capacitor. The value of C is selected to ensure an under-damped circuit and, also, determines the period of oscillation.

The series RLC circuit is a second order system whose characteristic equation is

$$s^2LC + sCR + 1. \qquad \ldots 2$$

The standard form for the solution of this equation is

$$\frac{s^2c}{w_n^2} + \frac{2\delta sc}{w_n} + c \qquad \ldots 3$$

where $\delta$ is the damping factor and $w_n$ the natural resonant frequency. The only case of interest — for self commutation — is the under-damped circuit where $\delta < 1$. For this case, if the SCR were not a reverse current blocking device the waveforms would be as illustrated by the dotted curves. The voltage across the capacitor C would oscillate about and eventually become charged to the applied voltage step V. The voltage across the inductor element L would oscillate about and eventually decay to zero. The circuit current and the voltage across the resistor would have similar shape, having maxima at the points-of-inflection of $V_C$ and $V_L$ and be zero at the maximum and minimum points of $V_C$ and $V_L$.

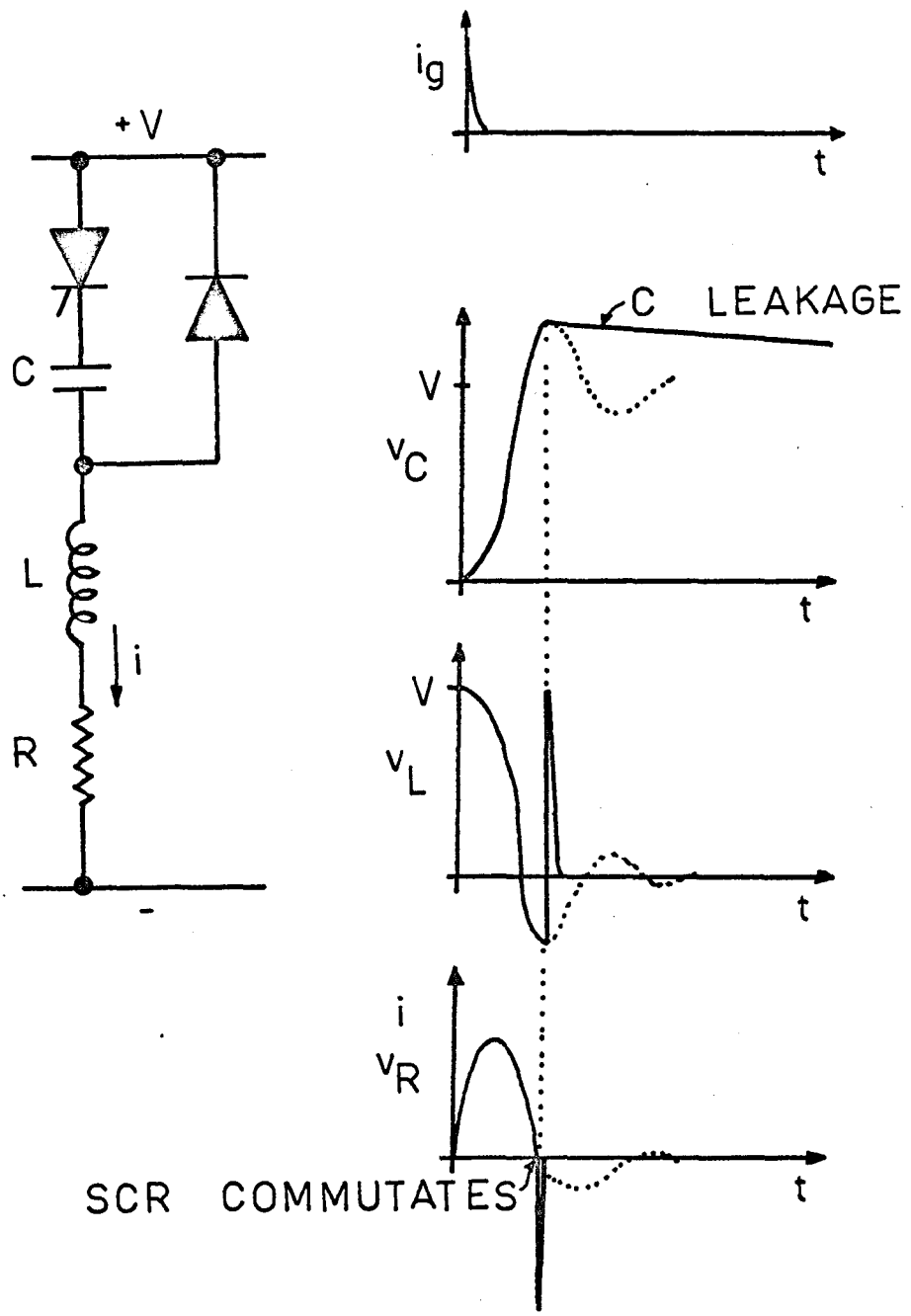



Figure 7. Self-commutating series RLC circuit.

The peak overshoot will occur at time

$$t_p = \frac{\pi}{w_n\sqrt{1 - \delta^2}} \qquad \ldots 4$$

and the normalized maximum amplitude will be

$$c_p = 1 + \exp[-\delta\pi/\sqrt{1 - \delta^2}]. \qquad \ldots 5$$

Comparing Equations 2 and 3, it is seen that

$$w_n = \frac{1}{\sqrt{LC}} \qquad \ldots 6$$

$$\delta = \frac{R}{2\sqrt{L/C}}. \qquad \ldots 7$$

The SCR, however, does have reverse blocking characteristics and, consequently, the circuit behaves as illustrated by the solid curves. A reverse diode provides a path for the inductance energy to decay through the power supply when the SCR commutates and interrupts the flow of reverse current.

When the voltage across the inductance reaches its minimum point (maximum negative), the current through the circuit reverses and the SCR is blocked and reverts to a state that blocks both forward and reverse currents. Consequently, the capacitor remains charged — perhaps losing a small amount through leakage. Because the reverse current flow has been blocked through the SCR, the voltage across the inductance rises quickly until the diode is forward biased, and then collapses through the power supply. The reverse impedance of the supply is high; consequently, the time-

constant of decay, L/R, is very short and appears essentially as a spike. Similarly, a spike of negative circuit current and voltage across the resistor appears, as illustrated.

It has thus been illustrated that the under-damped series RLC circuit is self-commutating. However, the capacitor has remained charged and the circuit cannot repeat the performance. A means, then, must be provided to either remove or reverse the charge on the capacitor.

The circuit, illustrated in Figure 8, meets the requirement for charge reversal of the capacitor. The SCR's are fired in push-pull pairs across the commutating capacitor C. A reactor is provided to limit the capacitor rate-of-discharge current to a value within the limitation of the SCR's.

Consider the case where $SCR_1$ and $SCR_2$ are triggered. It will be noted that the waveforms of the current and voltages are similar to the previously discussed circuit, and the two SCR's are blocked when the circuit current reverses. The capacitor remains charged. Next, $SCR_3$ and $SCR_4$ are triggered, and the capacitor is inverted, and its charge polarity aids that of the power supply; hence, it discharges through the reactor and diode which have a very much shorter time-constant than the R/L of the motor. The rate-of-discharge, of course, is limited by the reactor's inductance.

This circuit, Figure 8, represents only one of the six legs of the generalized inverter circuit introduced in

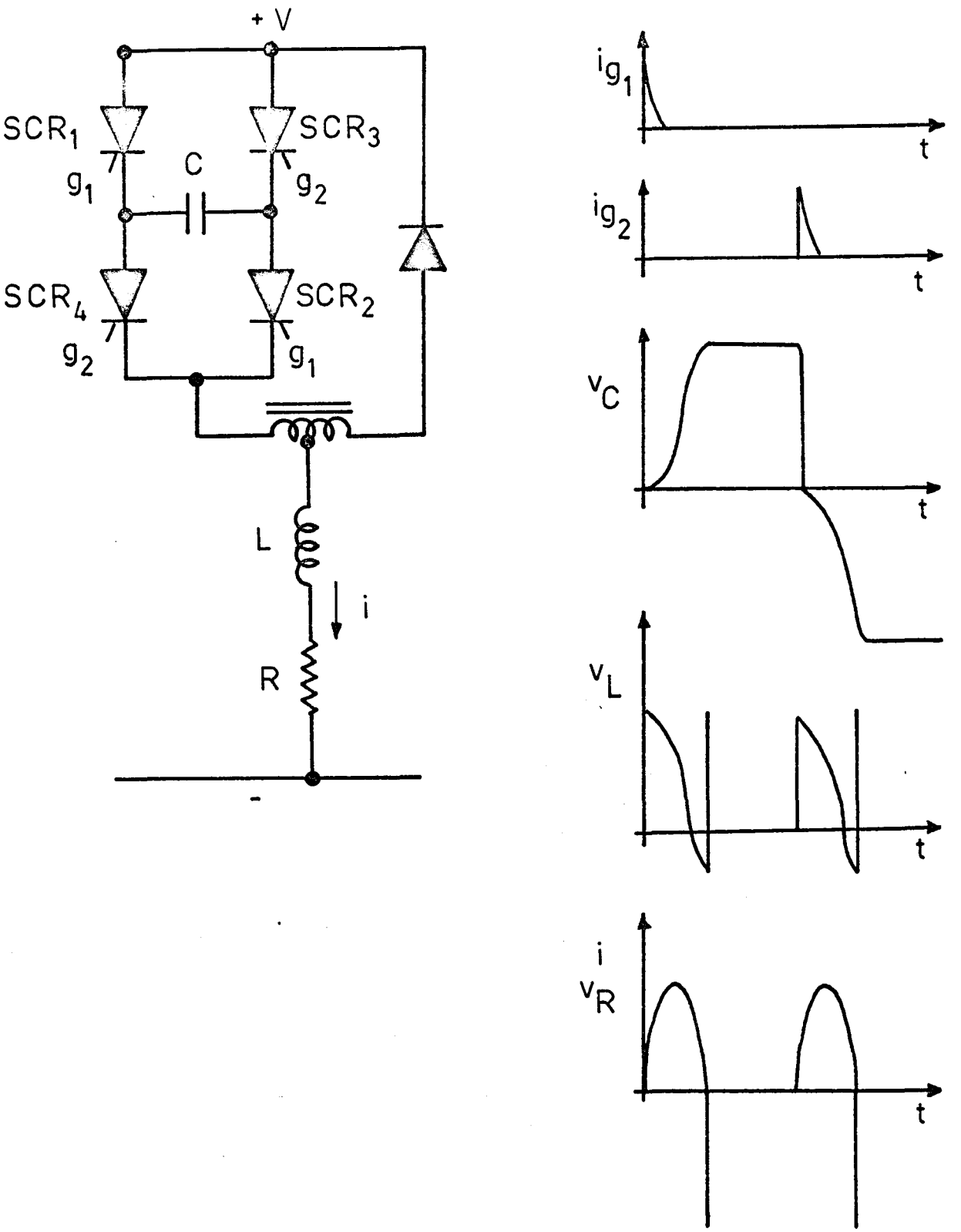



Figure 8. Improved self-commutating circuit.

Figure 5. The overall inverter configuration is illustrated in Figure 9. This is still, basically, the series RLC self-commutating circuit. Consider the motor as being the R and L elements connected between the output phases. Tracing a typical path through the inverter yields the series RLC circuit, as illustrated in Figure 10.

Design Considerations:

The main component in the bridge inverter is, of course, the SCR. The SCR must be capable of continuous operation at rated circuit current and have the reserve capacity for large starting currents. Provision must also be made in the design for commutation failure and associated current over-loading.

The maximum circuit current occurs at motor stand-still and this "locked-rotor" current can sometimes be very large — typically 7 times the full-load current. In the inverter circuit proposed, a variable voltage is achieved by variable pulse repetition of the applied voltage, and this yields a variable average voltage to the motor. However, as far as the SCR's are concerned, they will see the full locked-rotor current at start-up, and, consequently, the SCR's must be rated accordingly.

If external rotor resistance is added during start-up, the rating of the SCR's can be decreased accordingly. In this case, it is good design practice to over-rate the

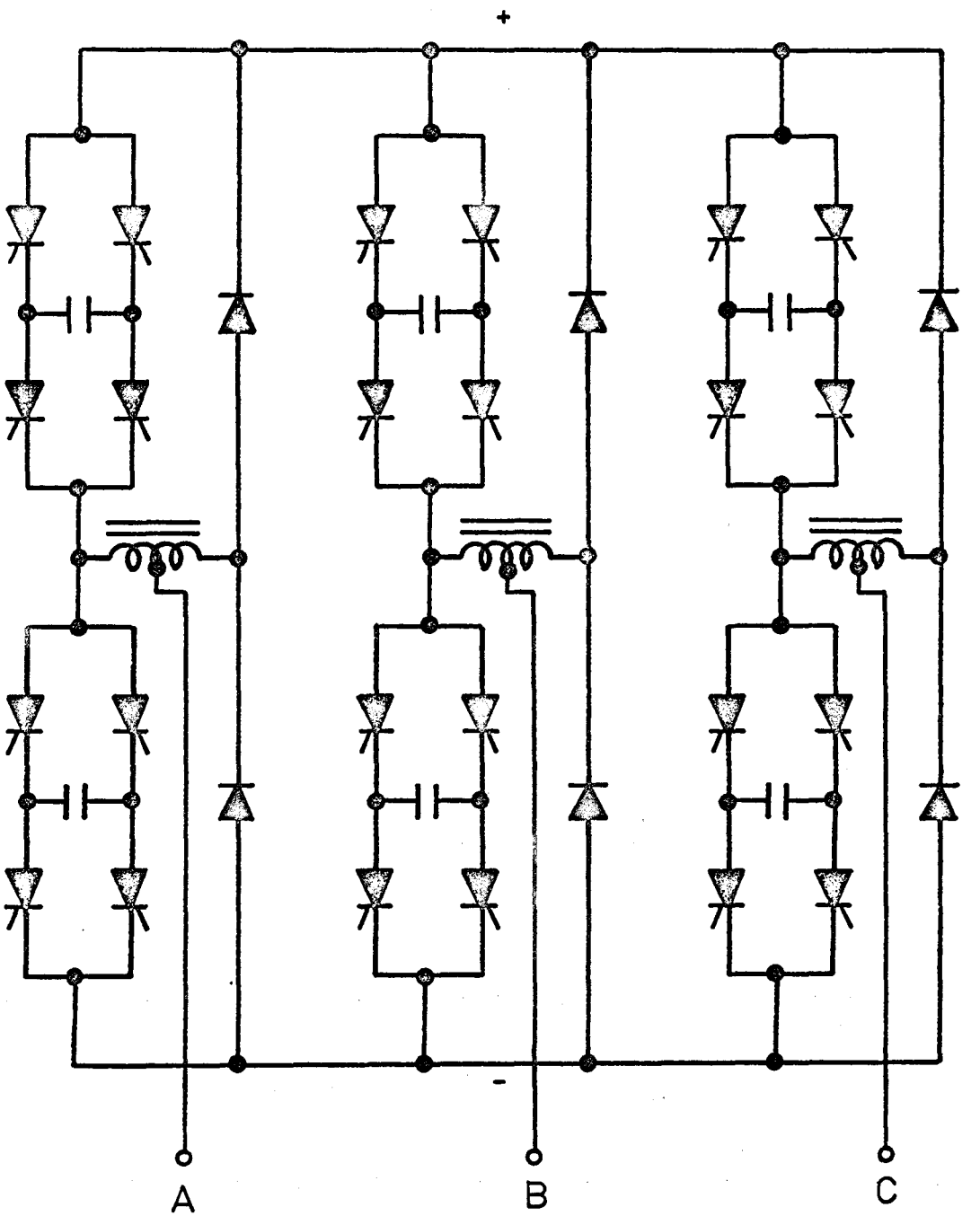



Figure 9. Self-commutating 3-phase bridge inverter.

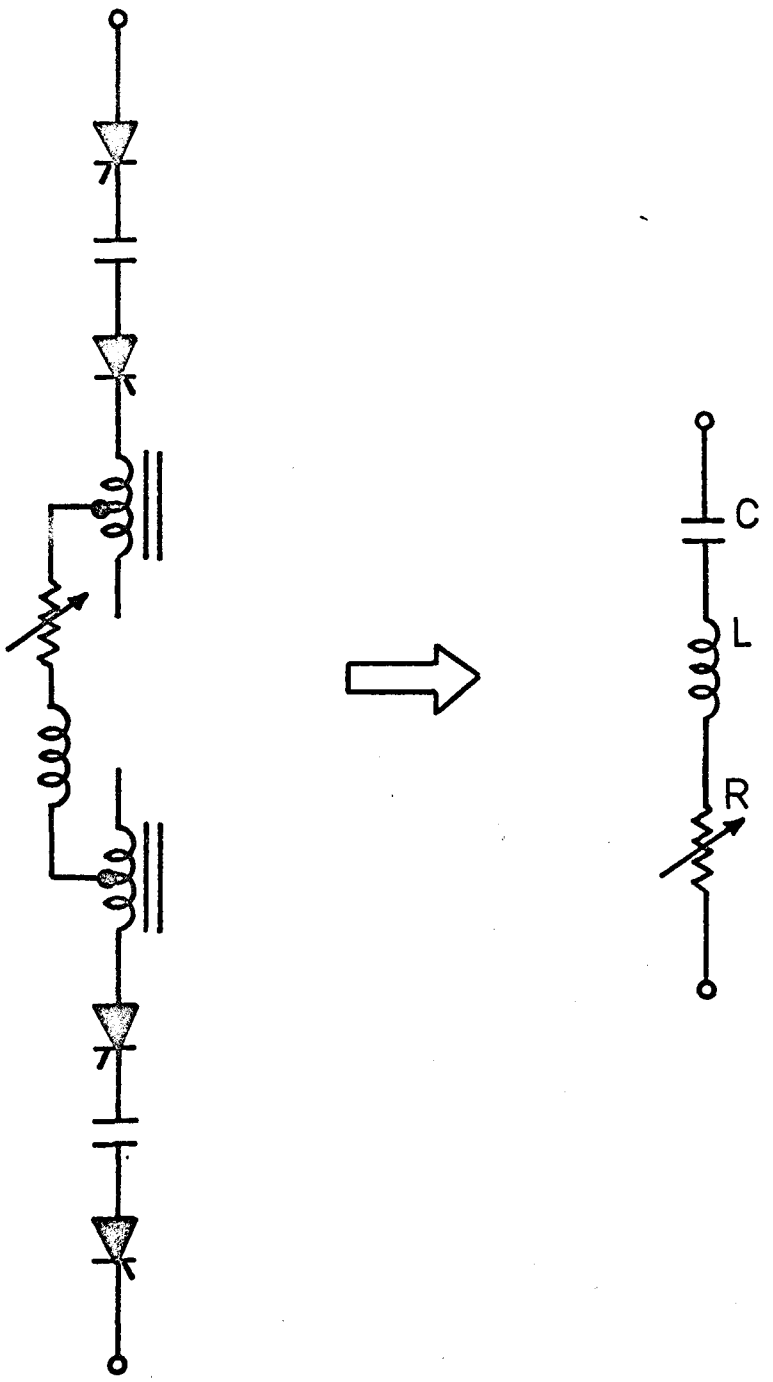



Figure 10. Equivalent circuit of a typical path through the inverter.

capacity of the SCR's over the start-up current associated with the external rotor resistance, to accommodate any slight misadjustment of the rotor rheostat during start-up.

In the series RLC circuit, the maximum voltage that the SCR's will encounter is given by Equation 5, and the SCR's should have a corresponding blocking voltage capability.

The rate-of-rise of current is limited by the circuit, and must be within the specifications of the SCR's. The inductance of the motor is normally fairly large, and the di/dt through the motor is held well within the limits of the SCR's. However, the capacitor discharge through the anti-parallel diode at the beginning of each cycle must be limited by an external reactor. The value of the reactor inductance is given by

$$L = \frac{\frac{1}{2}V_m}{di/dt}$$

where $V_m$ is given by Equation 5. Note that $\frac{1}{2}V_m$ is used because there are two capacitors in series in a particular path — refer to Figure 10.

Provision must be made for dissipation of the heat generated in the SCR's. The major sources will be those due to conduction and high rates of switching. The conduction dissipation is computed by integrating the products of anode currents and forward voltage drops for the wave shape of conduction. Meaningful dissipations for high repetition

rates must be obtained by actual thermal measurements. As a first estimate, for the switching speeds used in the proposed inverter configuration, the dissipation due to switching can be considered to be approximately the same as the conduction dissipation.

If a failure to commutate should occur, the inverter will hang-up, and there is a strong possibility of excessive current flow through the SCR's, especially if both halves of the same phase fail to commutate; in this case, a direct short circuit is placed across the DC supply. In such cases, the current will rise to destructive proportions before conventional fuses can melt. Consequently, a high-speed electronic circuit breaker, or commutation detection and inhibit system, is necessary to avert SCR burn-out.

Design of a 4 KVA Inverter:

The design of a 3-phase inverter to drive a 4 KVA squirrel-cage induction motor will be considered. The inverter should be capable of controlling the synchronous speed of the motor within the range 150—3000 RPM.

The characteristics of the motor are:

230 volts, 3 phase, 60 hertz, 4 pole, squirrel-cage, 9.4 amperes/phase (delta) rated current, and 25 ohms/phase external rotor resistance.

The synchronous speed of the motor is given by

$$N_s = \frac{120\ f}{p} \qquad \ldots 8$$

where $N_s$ = synchronous speed in RPM,

$f$ = supply frequency in hertz, and

$p$ = number of poles.

To operate in the speed range 150—3000 RPM, the inverter must have a frequency capability of 5—100 hertz. Refer to Equation 8.

The inverter configuration as illustrated in Figure 9 will be used. The DC supply will consist of a bridge rectifier operating from the 230 volt, 3-phase, 60 hertz power line.

The average DC rectifier output is given by

$$E_d = \frac{E\sqrt{2}\sin\frac{\pi}{p}}{\pi/p} \qquad \ldots 9$$

where $E_d$ = average DC output in volts,

$E$ = phase voltage, and

$p$ = number of phases.

Therefore

$$E_d = \frac{230\sqrt{2}\sqrt{3}/2}{\pi/3}$$

$$= 269 \text{ volts.}$$

The peak of the ripple voltage will be

$$E_{max} = 230\sqrt{2}$$

$$= 326 \text{ volts.}$$

The SCR's selected should have a blocking capability in the range 600—650 volts (85—100 % overshoot).

The line current at rated conditions will be

$= 9.4 \sqrt{3}$

= 16.3 amperes.

Consequently, the SCR's should have a current capability of 25 amperes for operation with external rotor resistance that limits the starting current to the full load value or, alternatively, 150 amperes for operation without external rotor resistance.

The General Electric type 2N690 SCR is selected and it has the following characteristics —

blocking voltage: 600 volts,

forward current: 25 amperes,

dv/dt: 10 volts/micro-second,

di/dt: 20 amperes/micro-second,

$t_{off}$: 75 micro-seconds,

trigger voltage: 3 volts, and

trigger current: 80 milli-amperes.

The anti-parallel diodes in the inverter should have similar ratings to the SCR's. General Electric type 4JA44M/45M diodes are selected. The characteristics of these diodes are 600 volts, 20 amperes.

The bridge rectifier diodes should be rated to the requirements of the inverter. International Rectifier type 40HF60/HFR60 diodes are selected. These diodes are rated at 600 volts, 40 amperes.

It will be noted that the rectifier diodes are rated slightly higher than the inverter SCR's. This provides slight mismatch of current capability, and if a solid fault occurs and the protection mechanism fails, only the weakest component fails. In this case, it is the SCR. Where economy is not an initial development consideration, or where the protection mechanism is not highly dependable, the diodes should be selected to be the weakest elements, as they are considerably less costly to replace.

Development of the triggering sequence and design of the associated circuitry are covered in Chapter 3. It is established in Chapter 3 that each leg of the inverter conducts for 1/3 cycle of the basic frequency. Assume that, at the maximum repetition rate, the leg sees continuous rated current for 1/3 cycle of the basic frequency; hence, the duty cycle is 1/3.

From the 2N690 forward V-I characteristic, the forward voltage drop, at the rated motor current of 16.3 amperes, is 1.5 volts. A conservative estimate of the conduction dissipation is, therefore

$$= \frac{1}{3} \times 16.3 \times 1.5$$

$$= 7.62 \text{ watts.}$$

The highest repetition rate for each SCR, from Chapter 3, is 750 hertz. The predominant dissipation for the 2N690, at repetition rates below 400 hertz, is that due to conduction.

However, at higher repetition rates, the dissipation due to the repetition becomes increasingly significant. As a first estimate, for operation at 750 hertz, assume the repetition dissipation to be approximately the same as the conduction dissipation; hence, a heat sink capacity of 15 watts is required for each SCR.

The anti-parallel and rectifier diodes should have heat dissipating radiator ratings similar to that of the SCR's. Hence, 15 watt heat sinks are selected.

The current limiting reactors must next be designed. The reactor should preferably be of the iron-core type and not saturate over its operating range. If each of the commutating capacitors is charged to 330 volts, and it is desired to keep the SCR di/dt to 10 amps/micro-sec, then the value of inductance required in the reactor will be

$$L = \frac{\frac{1}{2} V_m}{di/dt}$$

$$= \frac{330}{10} \times 10^{-6}$$

$$= 33 \text{ micro-henries.}$$

The reactor should be capable of continuous operation at 16.3 amperes.

Current overload protection must be provided to detect commutation failures and disconnect the DC supply from the inverter. The design of an electronic breaker with a 10 micro-second fault-to-interrupt time is covered in Appendix I.

Locked rotor tests, on the motor being considered, yield the following equivalent values of series resistance and inductance:

$$R = 3.32 \text{ ohms, and}$$

$$L = 12.7 \text{ milli-henries.}$$

Consider the use of 5 MFD capacitors. The total capacitance in each path will then be

$$= 2 \times 5$$

$$= 10 \text{ MFD.}$$

The damping ratio from Equation 7 is then

$$\delta = \frac{R}{2\sqrt{L/C}}$$

$$= \frac{3.32}{2\sqrt{12.7 \times 10^{-3}/10 \times 10^{-6}}}$$

$$= 0.465$$

The natural resonant frequency from Equation 6 is

$$w_n = \frac{1}{\sqrt{LC}}$$

$$= \frac{1}{\sqrt{12.7 \times 10^{-3} \times 10 \times 10^{-6}}}$$

$$= 2.805 \times 10^3 \text{ radians/sec.}$$

The peak overshoot, using Equation 4, occurs at

$$t_p = \frac{\pi}{w_n\sqrt{1 - \delta^2}}$$

$$= \frac{\pi}{2.805 \times 10^3 \sqrt{1 - .465^2}}$$

$$= 1.26 \text{ milli-seconds.}$$

The normalized overshoot is given by Equation 5 and is

$$c_p = 1 + \exp[-\delta\pi/\sqrt{1 - \delta^2}]$$

$$= 1 + \exp[-.465\pi/\sqrt{1 - .465^2}]$$

$$= 1.185$$

Hence, there is an 18.5 % overshoot.

CHAPTER THREE

# TIMING AND TRIGGERING

## General:

The heart of the inverter operation is the logic unit where the sequential timing pulses of the various phases are generated. The logic unit must have the flexibility to generate, from the inverter, both a variable frequency and a variable voltage level.

It is desirable to generate, as closely as possible, a sinusoidal 3-phase output. Working from a DC source, however, the output will necessarily be a stepped approximation of the sine wave.

## Generation of 3-phase Waveforms:

An approximated sinusoidal 3-phase system can be generated by step triggering of SCR's in a bridge configuration. Consider the bridge configuration illustrated in Figure 11. A hypothetical neutral has been established, in the supply, for illustration of the operation. It is to be noted that the upper SCR's ($SCR_1$, $SCR_3$, $SCR_5$) conduct the current for the positive half cycles of phases A, B, and C, respectively. Similarly, the lower SCR's ($SCR_2$, $SCR_4$, $SCR_6$) conduct the current for the negative half cycles.

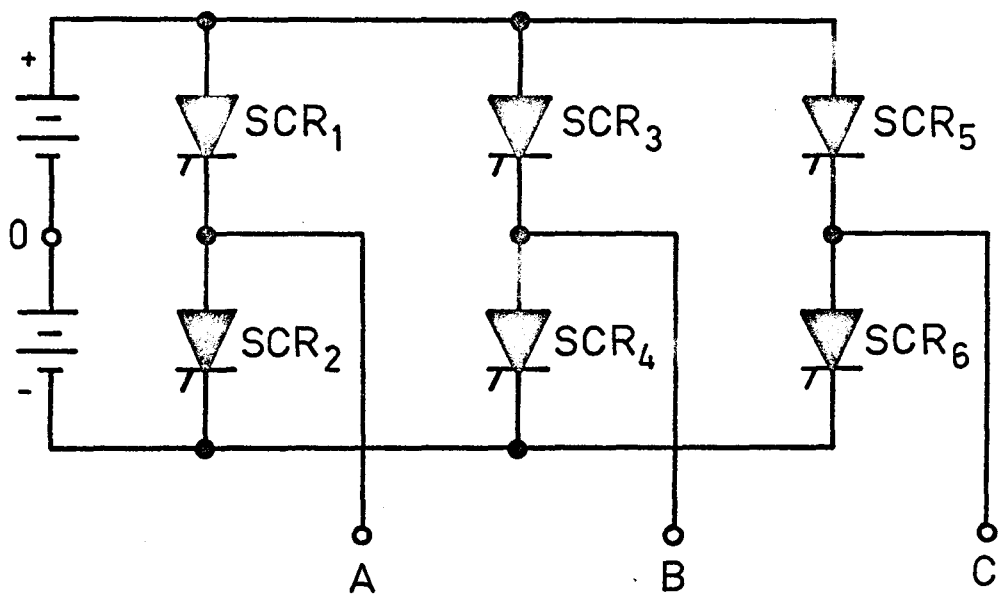



Figure 11. Bridge inverter with hypothetical neutral.

Consider a system with a 6-mode operation, as illustrated in Figure 12. Establish an operation such that $SCR_1$ conducts during modes 1, 2, and 3, which represents the positive portion of waveform $V_{ao}$ — the phase-to-neutral voltage of phase A. Also, $SCR_2$ conducts during modes 4, 5, and 6, which represents the negative portion of $V_{ao}$. Thus, $V_{ao}$ is positive for half the period and negative for the other half. In a 3-phase system, the phases have 120° phase displacements from one another. Consequently, phase B must be positive during modes 3, 4, and 5, and negative for modes 6, 1, and 2, to conform to the 120° displacements. Similarly, $V_{co}$ is positive during modes 5, 6, and 1, and negative during modes 2, 3, and 4.

The inverter outputs are not, however, the phase-to-neutral voltages, but are phase-to-phase voltages. This means, then, combining the various phase-to-neutral voltages. When this is done, the waveforms $V_{ab}$, $V_{bc}$, and $V_{ca}$ are generated. As an example, consider $V_{ab}$ which is the summation of $V_{ao}$ and $-V_{bo}$. For mode 1, this means adding $V_{ao}$, which is positive, to minus $V_{bo}$, which is negative; hence, $V_{ab}$ is maximum (2 phase-to-neutral units) positive. Proceeding in a similar manner for the remaining modes yields the waveform $V_{ab}$, as illustrated. Waveforms $V_{bc}$ and $V_{ca}$ are obtained in a similar fashion.

It will be noted that the various line (phase-to-phase) waveforms are separated by 120° and crudely approximate

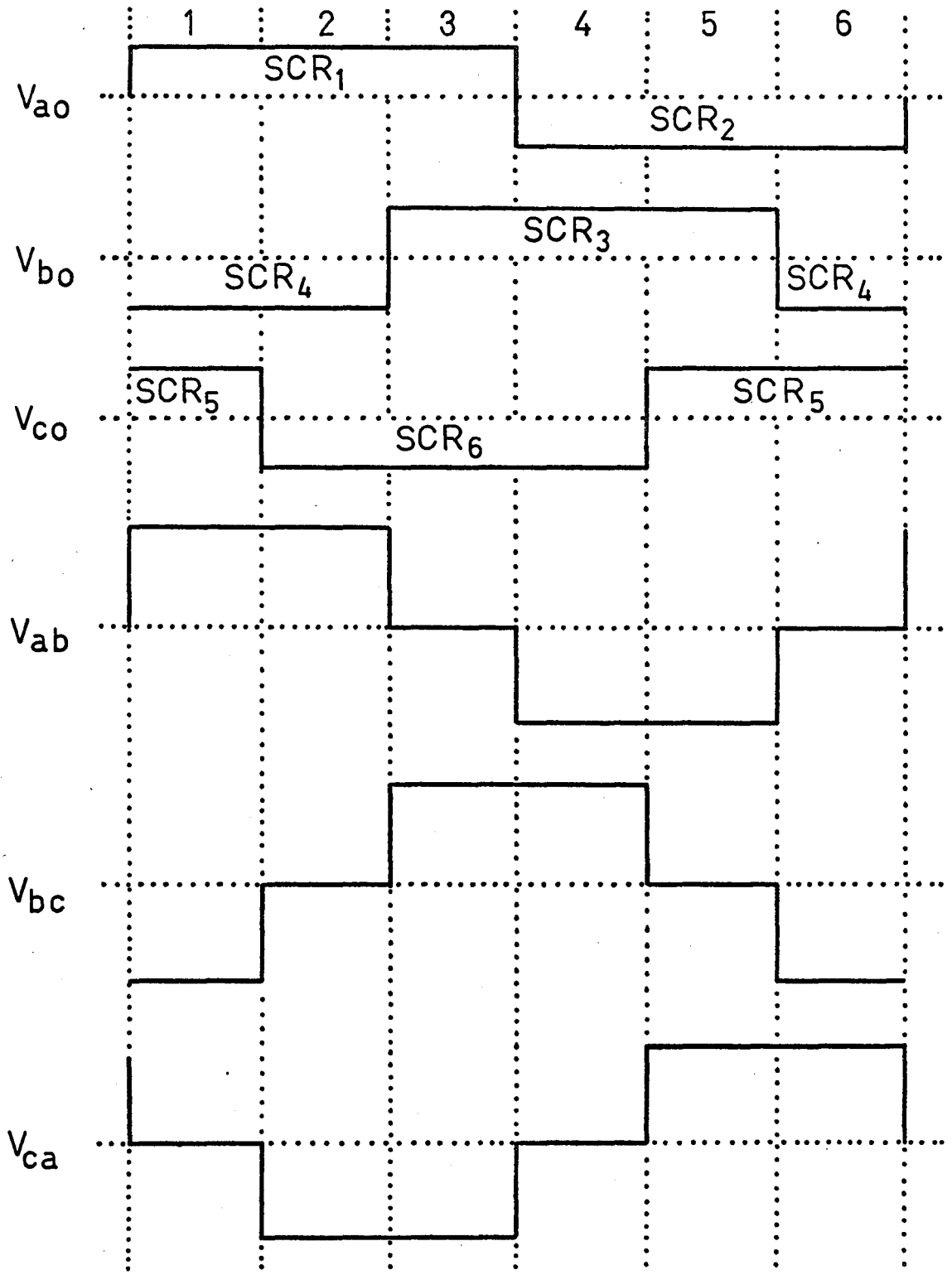



Figure 12. Six-mode inverter waveforms.

a sinusoidal variation. One of the major disadvantages of this construction is that an instantaneous switch from one polarity to the other must be made in the phase-to-neutral conduction. This means a simultaneous turn-on of one SCR, say $SCR_1$, and turn-off of the other, say $SCR_2$. Because of the very fast turn on (typically 1 micro-second), and relatively long turn-off (75 micro-seconds), the circuit will hang up, and both SCR's will remain on. Furthermore, both SCR's being on presents a direct short across the supply, and would result in component failure, if no over-current protection was utilized.

Consider the waveform construction, as outlined in Figure 13. In this case, the individual SCR's conduct for only 2 modes each cycle, and a gap of one mode exists between positive and negative conductions. The three phase-to-neutral waveforms have a 120° phase-displacement with respect to one another.

Summation of the various phase-to-neutral waveforms yields the line waveforms $V_{ab}$, $V_{bc}$, and $V_{ca}$, as illustrated. It will be noted that these waveforms more closely approximate the desirable sinusoidal waveshape.

The highest frequency of operation is 100 hertz; therefore, the shortest period of one mode is

$$= \frac{1}{6} \times \frac{1}{100}$$

$$= 1.67 \text{ milli-seconds.}$$

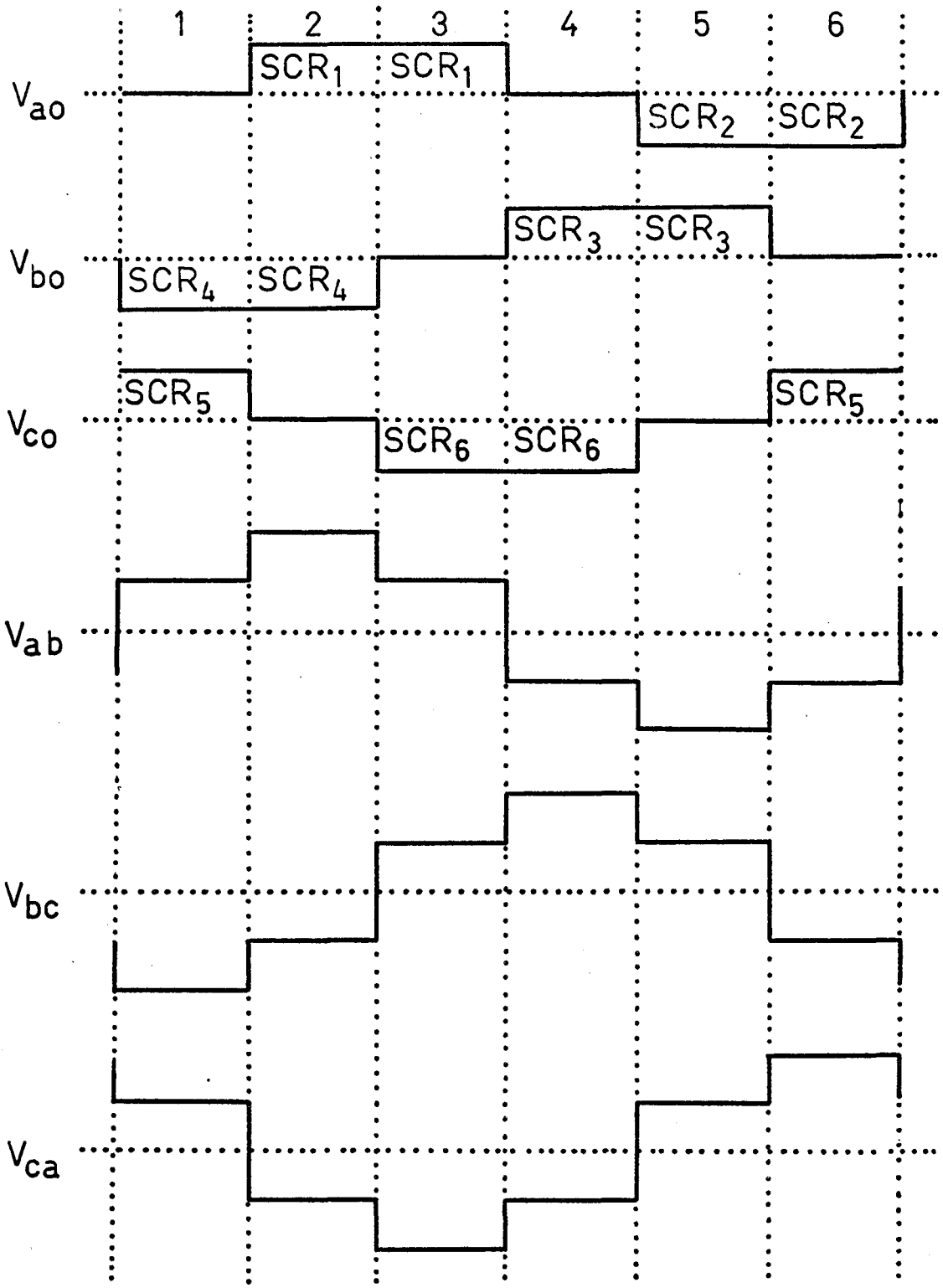



Figure 13. Improved 6-mode bridge inverter waveforms.

To avert commutation failure, the SCR must be commutated in a period of less than 1.67 milli-seconds.

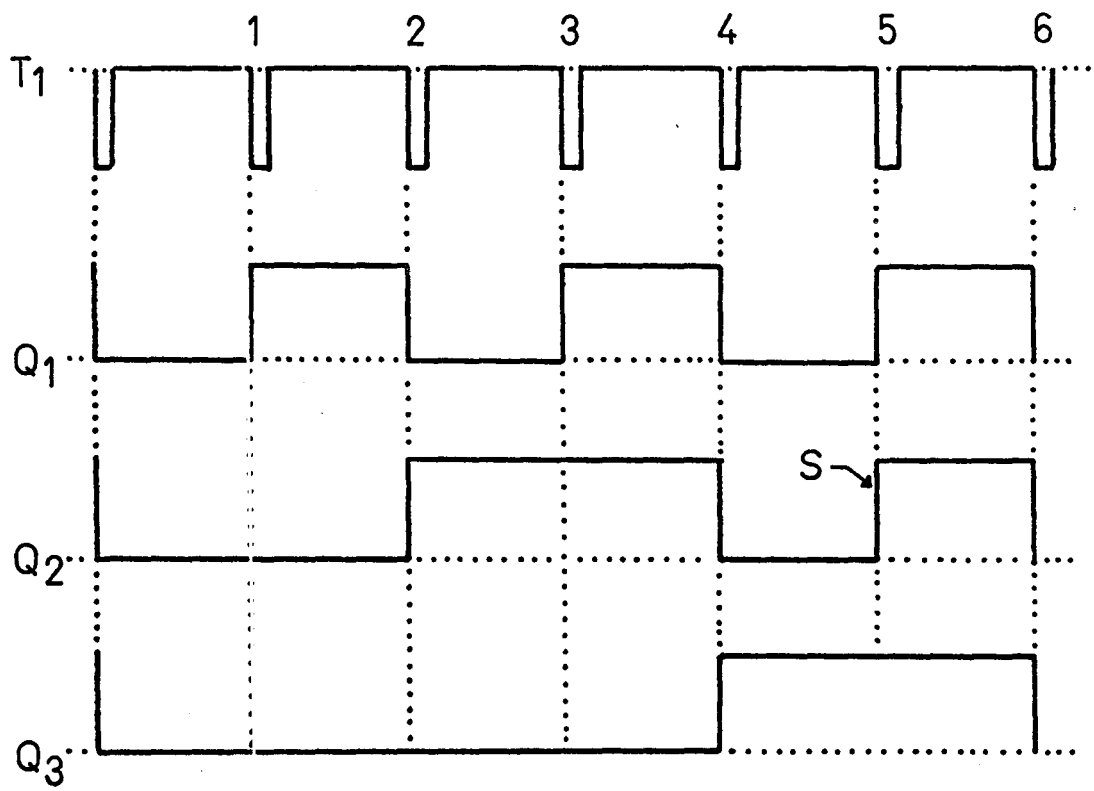
Six-Bit Register:

It has been established, in the foregoing treatment, that a good 3-phase sinusoidal waveshape approximation can be constructed from a 6-mode operation. The 6-bit register generates the necessary outputs for such an operation. Construction of this register involves the use of three binary counting (flip-flops) units. Since three binary units give an 8-mode operation, feedback must be employed to advance the register by a factor of 2 to yield a 6-mode operation.

Consider the operation, as illustrated in Figure 14. The input $T_1$ represents a continuous train of input triggers to the first binary unit. $Q_1$ represents the output of the first binary unit. It will be noted that the binary units respond only to negative going pulses. The binary units are connected in cascade, and $Q_2$ and $Q_3$ represent the outputs of the second and third units, respectively.

The register behaves as a conventional 8-bit counter up to pulse number 5, at which time feedback is employed to advance the second binary unit. The advancing of the second binary unit is accomplished by means of a SET pulse. The logic equation of this SET pulse can be written from the waveforms as

$$S = Q_1 \cdot \bar{Q}_2 \cdot Q_3.$$




$$S = Q_1 \cdot \overline{Q}_2 \cdot Q_3$$

Figure 14. Six-bit register waveforms.

Where $Q_1$ represents the positive or 1 state of the first binary unit, $\bar{Q}_2$ represents the zero or 0 state of the second binary unit (which is the case before the SET pulse S is generated), and $Q_3$ is the 1 state of the third binary unit.

The realization of such a circuit is illustrated in Figure 15. In this circuit, two outputs are available from each binary unit — Q and $\bar{Q}$. The logic for the SET pulse has been established for a 3-input AND gate; however, NAND gates are more commercially available; hence, a $\overline{\text{SET}}$ pulse is generated. The binary units must, therefore, respond to the $\overline{\text{SET}}$ feedback pulse.

Logic Equations:

The 6-bit register defines a 6-mode operation which provides for sequential triggering of the inverter SCR's. Each of the modes can be uniquely defined by writing logic equations from the register waveforms. Referring to Figure 14, let mode 1 represent the interval up to the time that the first trigger pulse arrives. In this case, the first binary unit is in its 0 state, which in logic form is written as $\bar{Q}_1$. Similarly, the second and third binary units are in their 0 states; hence, their logic forms are $\bar{Q}_2$ and $\bar{Q}_3$ respectively. The logic equation for mode 1 can therefore be written as

$$1 = \bar{Q}_1 \text{ AND } \bar{Q}_2 \text{ AND } \bar{Q}_3$$
$$= \bar{Q}_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3 .$$

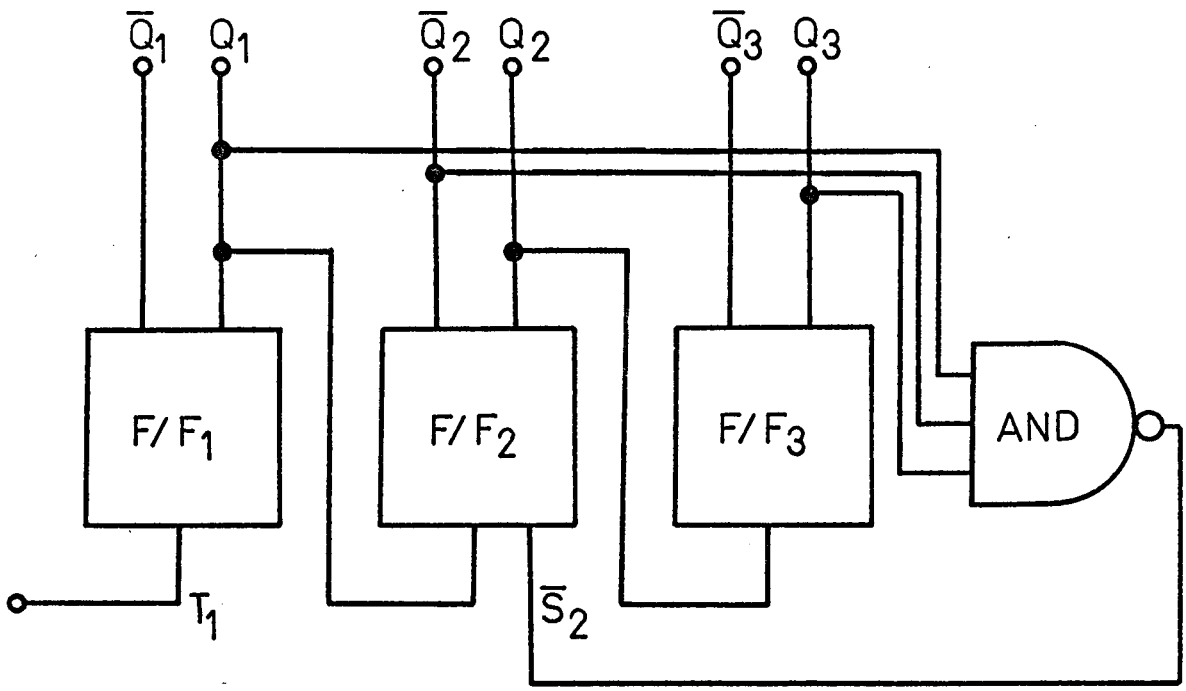



Figure 15. Six-bit register block diagram.

Proceeding in a similar fashion for mode 2 yields the logic equation

$$2 = Q_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 .$$

Consequently, the remaining modes can also be uniquely defined from the outputs of the various binary units. These logic equations are listed in Figure 16(a).

Now that the 6 modes have been defined, the logic equations defining the triggering of the various phases can be established. Referring to Figure 13, it will be noted that $SCR_1$, which represents the positive half of phase A ($\emptyset A^+$), conducts for both modes 2 and 3. This represents a logic OR operation; hence, the logic equation for $\emptyset A^+$ can be written as

$$\emptyset A^+ = 2 \text{ OR } 3$$
$$= 2 + 3 .$$

The logic equations for modes 2 and 3 have already been established; hence, referring to Figure 16(a), the logic equation for $\emptyset A^+$ can also be written as

$$\emptyset A^+ = Q_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 + \overline{Q}_1 \cdot Q_2 \cdot \overline{Q}_3 .$$

Proceeding in a similar manner, the remaining logic equations can be established for all the phases. These are summarized in Figure 16(b).

Circuit realization of these equations is easily established using logic AND and OR gates. The realization of a typical equation ($\emptyset A^+$) using these gates is shown in

$$1 = \bar{Q}_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3$$
$$2 = Q_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3$$
$$3 = \bar{Q}_1 \cdot Q_2 \cdot \bar{Q}_3$$
$$4 = Q_1 \cdot Q_2 \cdot \bar{Q}_3$$
$$5 = \bar{Q}_1 \cdot \bar{Q}_2 \cdot Q_3$$
$$6 = Q_1 \cdot Q_2 \cdot Q_3$$

(a)

$$\phi A^+ = 2 + 3 = Q_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3 + \bar{Q}_1 \cdot Q_2 \cdot \bar{Q}_3$$
$$\phi A^- = 5 + 6 = \bar{Q}_1 \cdot \bar{Q}_2 \cdot Q_3 + Q_1 \cdot Q_2 \cdot Q_3$$
$$\phi B^+ = 4 + 5 = Q_1 \cdot Q_2 \cdot \bar{Q}_3 + \bar{Q}_1 \cdot \bar{Q}_2 \cdot Q_3$$
$$\phi B^- = 1 + 2 = \bar{Q}_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3 + Q_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3$$
$$\phi C^+ = 6 + 1 = Q_1 \cdot Q_2 \cdot Q_3 + \bar{Q}_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3$$
$$\phi C^- = 3 + 4 = \bar{Q}_1 \cdot Q_2 \cdot \bar{Q}_3 + Q_1 \cdot Q_2 \cdot \bar{Q}_3$$

(b)

$$\phi_V A^+ = V.(2 + 3) = V.(Q_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3 + \bar{Q}_1 \cdot Q_2 \cdot \bar{Q}_3)$$
$$\phi_V A^- = V.(5 + 6) = V.(\bar{Q}_1 \cdot \bar{Q}_2 \cdot Q_3 + Q_1 \cdot Q_2 \cdot Q_3)$$
$$\phi_V B^+ = V.(4 + 5) = V.(Q_1 \cdot Q_2 \cdot \bar{Q}_3 + \bar{Q}_1 \cdot \bar{Q}_2 \cdot Q_3)$$
$$\phi_V B^- = V.(1 + 2) = V.(\bar{Q}_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3 + Q_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3)$$
$$\phi_V C^+ = V.(6 + 1) = V.(Q_1 \cdot Q_2 \cdot Q_3 + \bar{Q}_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3)$$
$$\phi_V C^- = V.(3 + 4) = V.(\bar{Q}_1 \cdot Q_2 \cdot \bar{Q}_3 + Q_1 \cdot Q_2 \cdot \bar{Q}_3)$$

(c)

Figure 16. Logic equations.

Figure 17. Of course, six such circuits are required to define the operation for all of the logic equations $\emptyset A^+$ through $\emptyset C^-$.

The logic AND and OR gates are not readily available on the commercial market, and the use of NAND and/or NOR units must be realized. The circuit realization, using NAND gates only, is easily accomplished by applying deMorgan's theorem to the logic equations. Consider $\emptyset A^+$

$$= Q_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3 + \bar{Q}_1 \cdot Q_2 \cdot \bar{Q}_3$$

$$= \overline{\overline{(Q_1 \cdot \bar{Q}_2 \cdot \bar{Q}_3) \cdot (\bar{Q}_1 \cdot Q_2 \cdot \bar{Q}_3)}} \quad \text{by deMorgan's theorem.}$$

Hence cascading of NAND gates, as illustrated in Figure 18, achieves the same result as the use of AND and OR gates.

The overall logic circuit realization, using NAND gates, is shown in Figure 19. From this, it is seen that 12 NAND gates are required — 6 three-input and 6 two-input gates.

Voltage Control Logic:

The foregoing treatment has established the logic equations and circuit realizations for generation of the basic frequency. An operation whereby the phase SCR's are pulsed on and off, to yield a variable average voltage output, can be established by means of an additional logic input to the basic equations. Such an additional input, V, has been added to the logic equations in Figure 16(b) and is shown

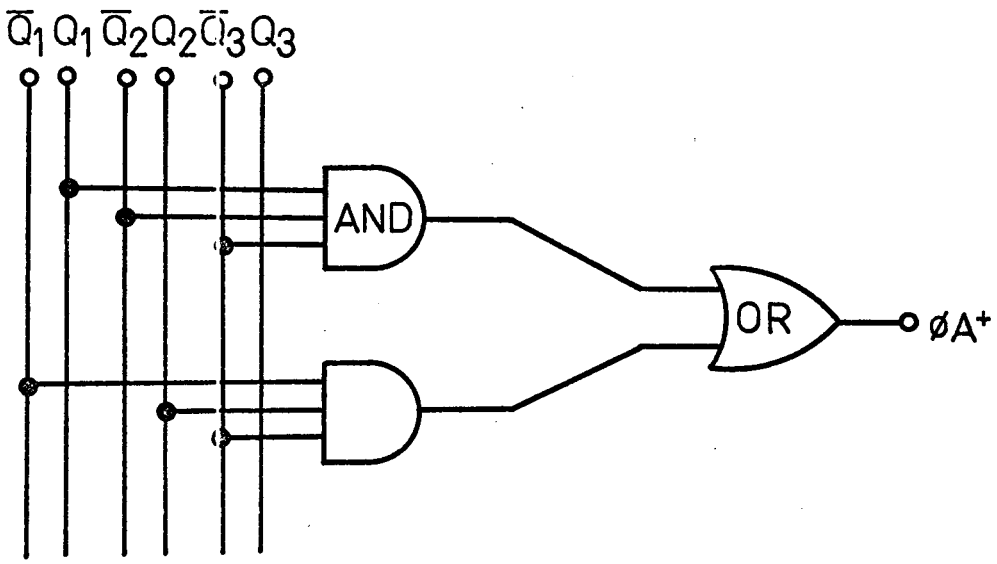



Figure 17. Realization of ø $A^+$ using AND and OR gates.

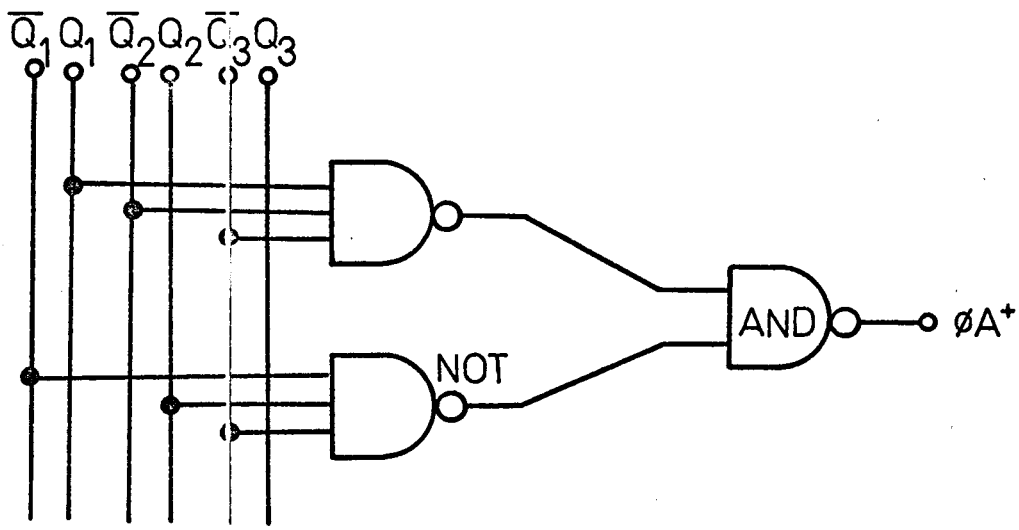



Figure 18. Realization of $øA^+$ using NAND gates.

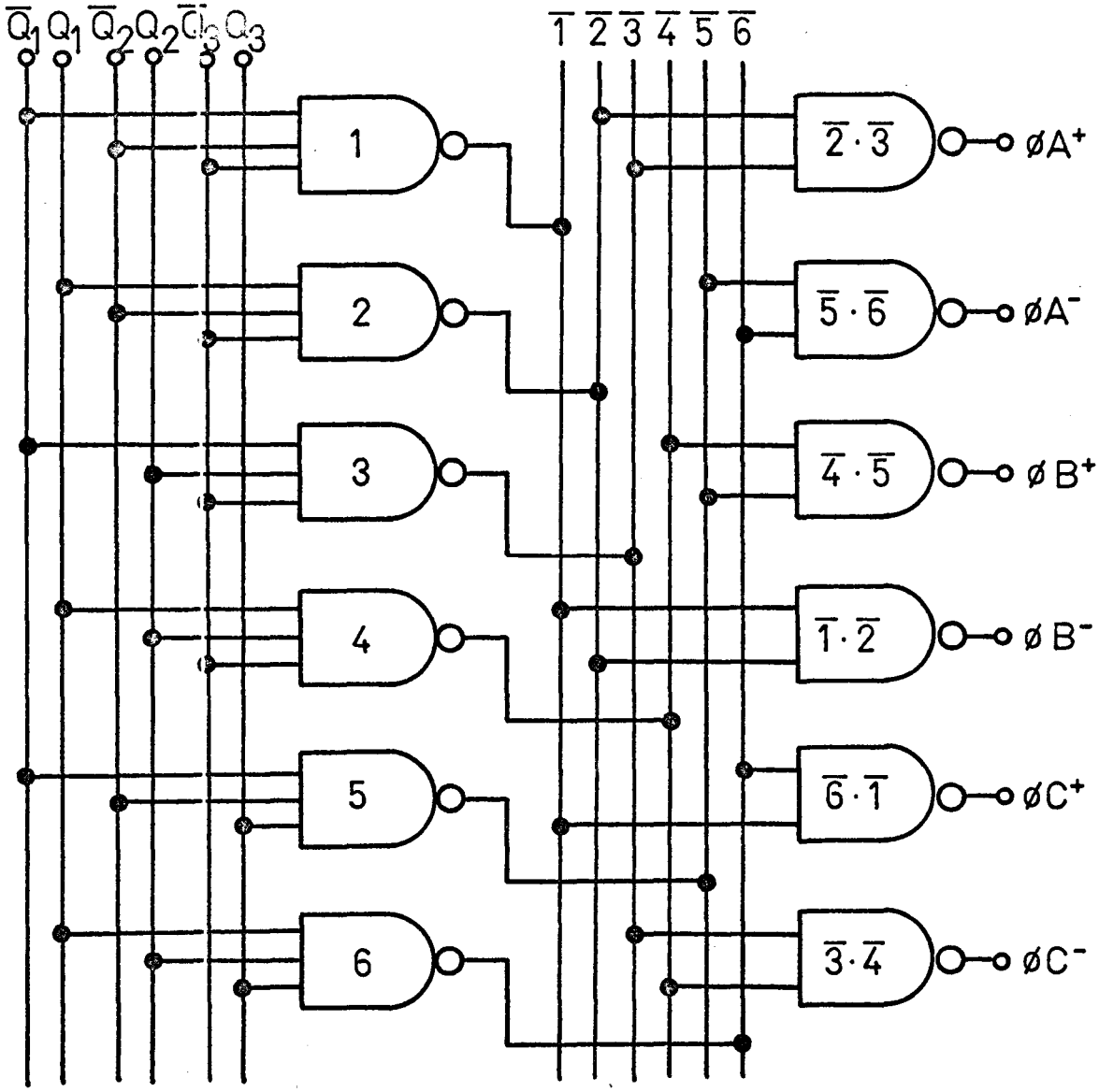



Figure 19. Overall logic realization.

in Figure 16(c).

The realization of this additional input is the use of AND gates. Typically, this is shown for $\emptyset A^{+}$, in Figure 20. Once again, the NAND gate must be used because of commercial availability. This unit should also provide sufficient drive for succeeding stages.

Trigger Requirements:

The logic system described above provides only one set of trigger pulses for each half phase of the inverter; however, the inverter described in Figure 9 requires a double set of trigger pulses for operation. The second set of pulses can be generated with the use of monostable multivibrators. In this case, the second set of pulses is generated at a fixed period of time after the first set is received.

It is desirable to have the second set of pulses occur at a time commensurate with the highest repetition frequency and the circuit commutation time. From Chapter 2, the circuit commutation time is 1.26 milli-seconds. A nearly constant conduction through the circuit would occur at a repetition frequency of 1500 hertz. This represents a period of 0.667 milli-seconds, which is approximately half the circuit commutation time.

The output from the logic unit will be sets of pulse bursts, as illustrated in Figure 21(a). The repetition

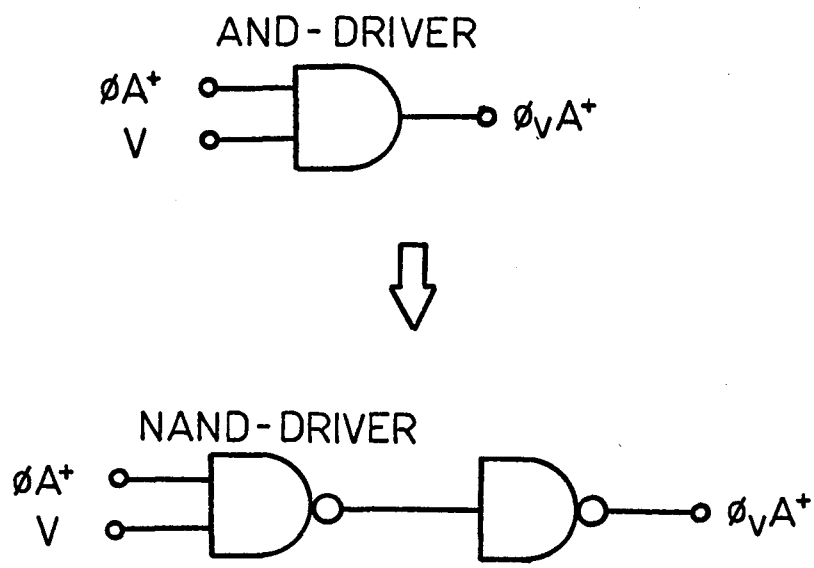



Figure 20. Voltage control logic realization.

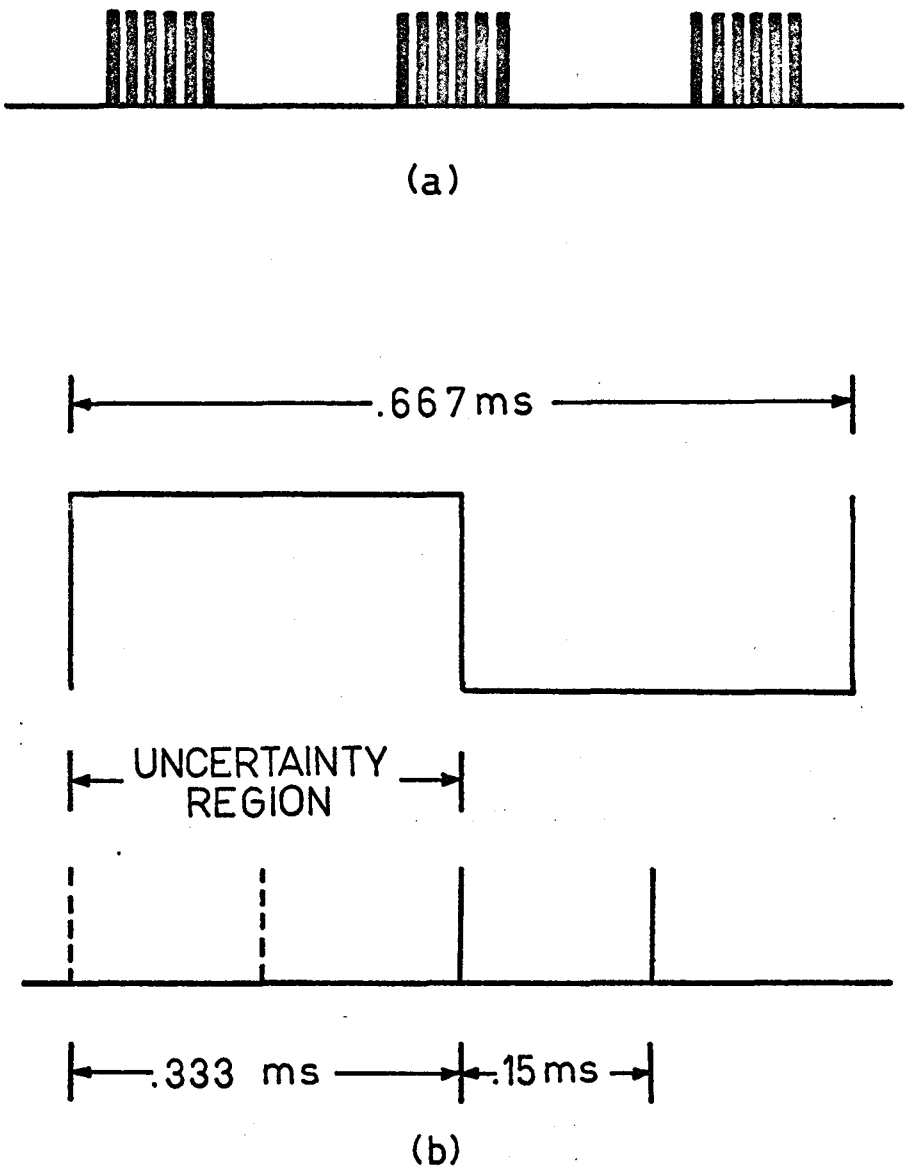



Figure 21. Logic unit output waveforms.

of the sets of pulses dictates the operating frequency of the inverter, and the repetition of the individual pulses in the set gives the average voltage level. The highest burst frequency, as discussed above, is 1500 hertz.

In the logic system proposes, there is a region of uncertainty with the leading pulse in each burst. This is illustrated in Figure 21(b). The highest repetition rate of 1500 hertz represents a time period of 0.667 milli-seconds, and the first half of this period is the uncertainty region. The positive portion of this pulse only occurs when the logic states of the basic frequency and the repetition frequency are coincident. The two VFO inputs, representing these frequencies, are not synchronized and, consequently, the leading edge of the first pulse in the burst will be random.

Although the circuit self-commutates the SCR's in 1.26 milli-seconds, the SCR's are capable of being commutated in 75 micro-seconds. This type of commutation would occur if an opposite pair of SCR's was switched on. In this case the charge polarity on the commutating capacitor would force a reverse current through the original pair of SCR's causing them to commutate. Therefore, the requirement to be met is that a period of at least 75 micro-seconds must be provided between gating of opposite pairs of SCR's in a particular leg of the inverter.

From Figure 21(b), it will be noted that the leading edge of the first pulse could occur at any time up to the

333 milli-second point. Therefore, the longest period between pulses, to allow for SCR commutation, will be 167 micro-seconds.

Consider the monostable multivibrator illustrated in Figure 22. The time constant of this multivibrator is given as

$$T = 0.69\ RC.$$

By selecting R = 10 Kohms and C = 0.022 MFD, the operating time constant will be

$$= 0.69 \times 10 \times 10^{3} \times 0.022 \times 10^{-6}$$

$$= 152 \text{ micro-seconds.}$$

By using this circuit, a second pulse is generated 152 micro-seconds after the initiating pulse, T, is received. The positive going edges of the waveforms at the two emitters provide triggering mechanisms for the pulse shaping circuits that follow.

The desired waveform for triggering the SCR's is shown in Figure 23(a). The pulse should be at least 50 micro-seconds wide and have an amplitude of 10 volts to ensure positive triggering action. This desired waveshape can be obtained from a unijunction relaxation oscillator, as illustrated in Figure 23(b). In this case, the unijunction oscillator should respond to input trigger pulses from the preceeding monostable oscillator stage. The energy in the pulse is stored in the capacitor C and the time constant of charge should be compatible with the highest operating

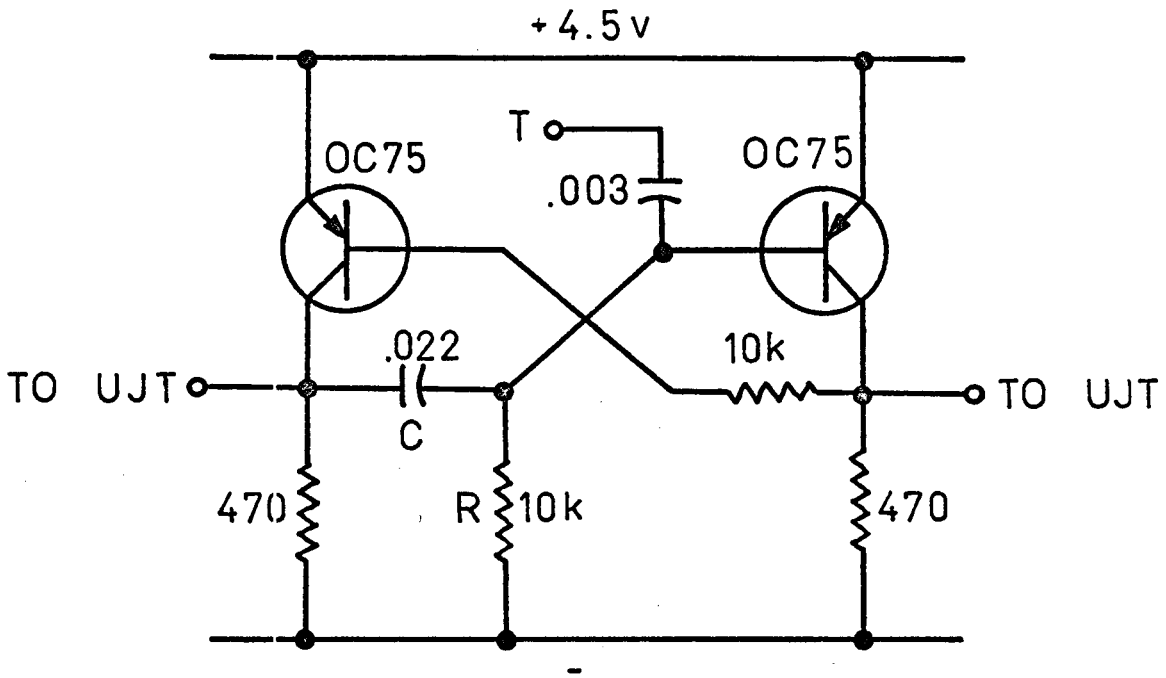
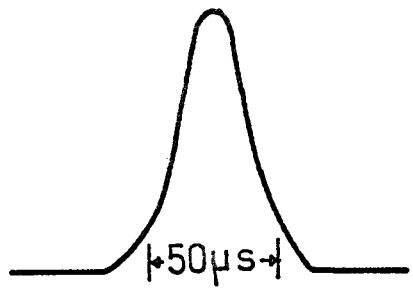



Figure 22. Monostable multivibrator.



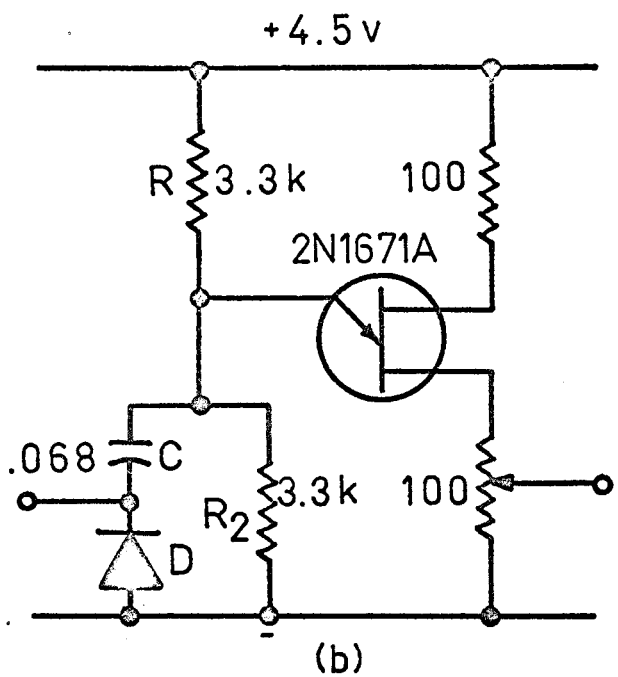




Figure 23. Unijunction stage.

frequency. The oscillation time constant is given by

$$T = CR \ln \frac{1}{1 - n},$$

where n is the intrinsic standoff ratio of the unijunction transistor and varies from 0.47 to 0.62 for the 2N1671A unijunction transistor.

The resistor $R_2$ is used to prevent the oscillator from free-running. The value of $R_2$ is selected to hold the emitter a fraction of a volt below its "peak point voltage", at which time the capacitor is discharged through the lower base and load resistor $R_L$. The unit is triggered by raising the emitter voltage above its peak point voltage. This trigger voltage is developed across the 470 ohm resistor in the previous stage — Figure 22. This 470 ohm resistor is in series with the capacitor and a positive going pulse at this point will cause the unit to discharge the capacitor through the load.

The 470 ohm resistor of the previous stage is in series with the capacitor discharge circuit and, consequently, will absorb a very large fraction (470/570) of the discharge. In most cases, a discharge path greater than 100 ohms leads to an unreliable operation. The use of the diode, D, by-passes the 470 ohm resistor in the discharge path and enables a very reliable operation.

The output from the unijunction circuit is not sufficient to drive the SCR gates directly in the proposed

inverter. Stages of voltage and power amplification must follow. The necessary voltage and power gains are available from the circuit shown in Figure 24. Because of the very low input impedance of the gate circuits, two cascaded emitter-follower stages are necessary. The overall gain of the amplifier is 200, and adjustment of the output level is provided by means of a potentiometer in the unijunction base.

Gate Isolation:

With the inverter configuration selected, pulse transformers must be employed because of the need for isolation of the various SCR's. However, when transformers are employed, a negative current flows through the gate when the SCR is commutated. This negative pulse can cause erratic refiring of the SCR. If unijunction devices are employed in the primary of the transformer, the negative pulse can cause false operation of the trigger circuit. Also, the negative pulse can cause ringing in the secondary of the transformer, when the stray capacitances are considered.

It is desirable to eliminate negative current flow in the gate circuit. This is best accomplished with a diode bridge, as illustrated in Figure 25. The diodes selected should be of the high conductance, and short recovery, type. The use of high conductance diodes reduces the gate drive requirements because the gate characteristics of

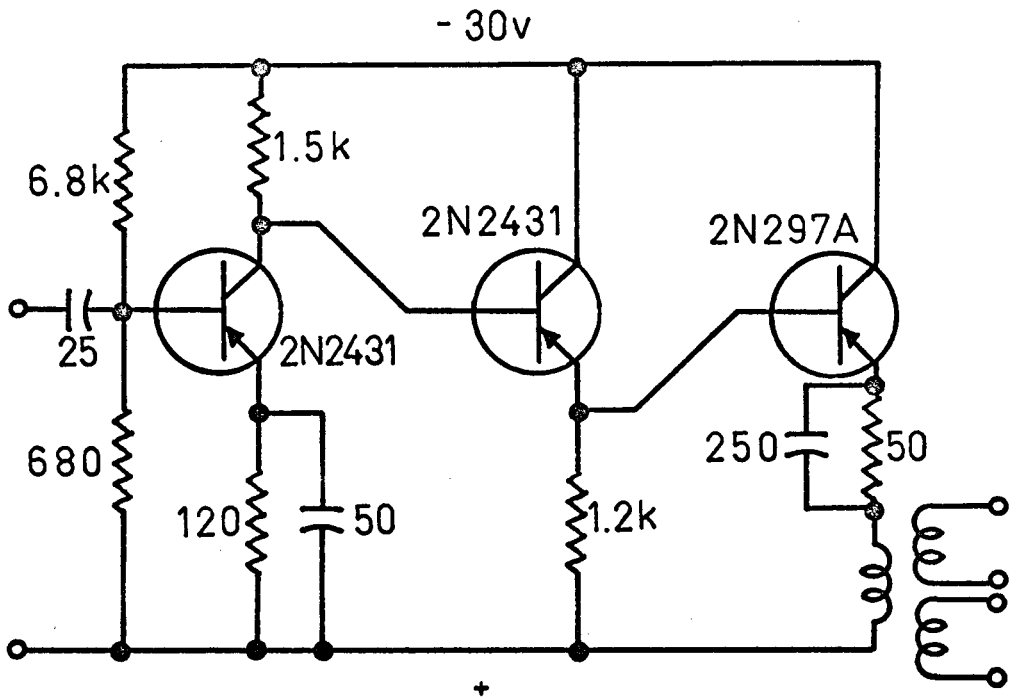



Figure 24. Power amplifier.

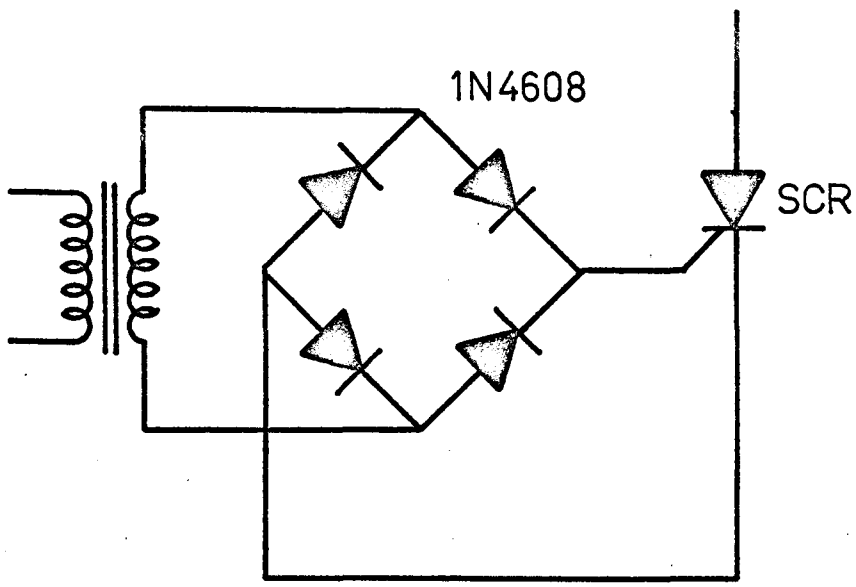



Figure 25. Gate isolation bridge.

the SCR are that of a very high conductance diode. Fast recovery diodes are essential because the frequency of ringing is high, due to the relatively small stray capacitances. The General Electric 1N4608 diode is selected for these characteristics.

Summary:

The timing and triggering requirements are summarized in block diagram form in Figure 26. Two variable frequency oscillators (VFO's) constitute the input control elements, providing basic frequency control and control of the average voltage level output. The flip-flop units are utilized to shape the sine wave inputs to rectangular pulses for reliable operation of succeeding logic stages.

The 6-bit register provides a 6-mode operation, enabling a closely approximated sinusoidal output of the inverter. The logic unit assimilates the outputs of the register and the voltage VFO flip-flop, and generates a set of sequential timing pulses. The monostable multivibrators provide a second set of timing pulses spaced 152 microseconds apart from the initial set. The gate amplifiers provide the necessary gate drive for reliable operation of the SCR's.

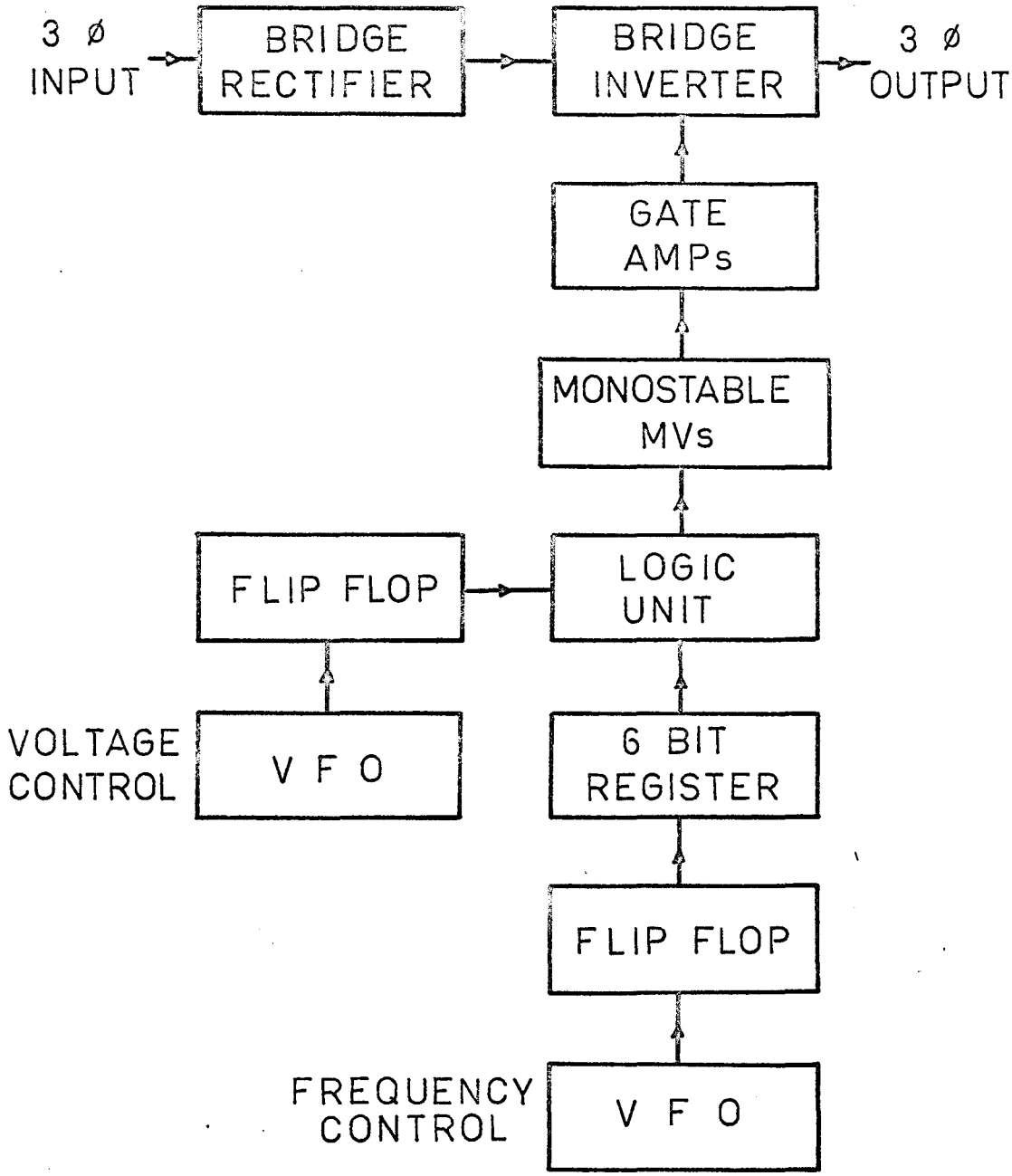



Figure 26. Overall block diagram.

CHAPTER FOUR

# INDUCTION MOTOR LOSSES ASSOCIATED WITH NONSINUSOIDAL VOLTAGE SOURCES

## General:

Induction motors excited with static inverters are subjected to nonsinusoidal voltage waveforms, and the presence of time harmonics in the applied voltage results in currents at the harmonic frequencies. These currents result in additional and sometimes rather large losses.

The voltage waveforms produced by the inverter can be considered to consist of a series of discrete voltage steps, as illustrated in Figures 13 and 21(a). These waveforms are periodic and have a finite number of maxima, minima, and discontinuities within a given period, which makes the waveforms amenable to analysis by the Fourier series. Knowing the voltage waveform, the general expression for the impressed voltage is

$$v(t) = \sqrt{2}[V_1 \sin\omega t + V_5 \sin 5\omega t + V_7 \sin 7\omega t + \ldots + V_k \sin k\omega t] \qquad \ldots 10$$

It will be noted that Equation 10 does not contain any even harmonics or harmonics which are divisible by three.

From equation 10, it is seen that the analysis of the

motor can proceed as if there were a series of independent generators all connected in series. Each generator would represent one of the voltage terms. The T-model equivalent circuit, outlined in Figure 6, is very useful in calculating the performance of a motor under steady-state operating conditions. Because each harmonic current is independent of all others, a series of independent equivalent circuits, one for each harmonic, can be used to calculate the complete steady-state performance.

Motor Losses:

The induction motor operated from a nonsinusoidal supply voltage has the usual motor losses, and some additional losses due to the harmonic currents. The losses are:

stator winding loss,
rotor winding loss,
core loss,
friction and windage loss,
rotor harmonic loss, and
stray load loss.

The stator $I^2R$ loss is given by the usual equation, with an additional term to account for the harmonic currents:

$$W_s = m\, R_1\, (I_1^2 + I_{har}^2).$$

This loss is not only larger by the amount of the second term, but the first term is also increased due to the

increase in magnetizing current. The fundamental component of magnetizing current is increased because of harmonic peaks saturating the iron and reducing the value of $L_m$.

The rotor $I^2R$ loss is given by

$$W_r = \frac{T\ s}{7.04} .$$

This loss is increased by a negligible amount with nonsinusoidal excitation; the increase is due to the increase in slip-speed to overcome the small negative torque produced by the harmonic currents.

The core loss is a function of the flux density in the stator core. It will be larger with nonsinusoidal excitation due to higher peak flux densities associated with the magnetizing current. This loss is normally a small fraction of the total loss and can usually be neglected.

The friction and windage loss is not affected by the voltage waveform.

The rotor harmonic loss can be the largest loss directly attributable to harmonic currents. It is appreciably increased by the rotor deep-bar effect — variation of rotor resistance with frequency.

The stray load loss consists mainly of the following losses:

rotor zig-zag loss,

stator end loss,

rotor end loss, and

other stray losses.

The rotor zig-zag loss is due to pulsating flux in the rotor teeth due to slot permeances and slot MMF harmonics. This flux induces currents into the rotor bars, with an $I^2R$ loss resulting. Because both fundamental no-load current and the total stator current are substantially larger with nonsinusoidal excitation, this loss can be several times larger than with sinusoidal applied voltage.

The stator end loss is the eddy current loss in the stator end laminations due to leakage flux entering these laminations axially.

The rotor end loss, like that described above for the stator, also occurs in the rotor end laminations. For the motor operated at its normal slip, the frequency of the fundamental component of rotor leakage flux is very low, and the loss is negligible. However, each harmonic will produce a loss, and these are summed to produce the total loss.

The remaining stray load losses will probably be slightly larger with harmonics present. However, they are usually small and are taken to be the same as with sinusoidal excitation.

Summary:

The losses of an induction motor with nonsinusoidal applied voltages can be markedly different from its sinusoidal losses depending upon the harmonic content of the

impressed waveform. The increase in motor loss associated with a six-step inverter operation, as illustrated in Figure 13, will be approximately 20 percent.

# CHAPTER FIVE

## SUMMARY

General:

The speed of the squirrel-cage induction motor can be controlled within a wide range by varying the applied frequency. The SCR bridge inverter provides a variable frequency at power levels.

Because of the requirement in the induction motor to maintain a constant magnetizing flux, the applied voltage must be varied in proportion to any variation of the frequency; a constant volts/hertz ratio must be maintained. The average voltage output of the inverter can be varied by employing a secondary pulse repetition of the SCR's.

It has been established in Chapter 3 that a 6-mode operation of the inverter provides a good approximation to the sinusoidal output waveforms. Such a 6-mode operation can be established by utilizing logic circuits.

Two variable frequency oscillators constitute the input control elements. One establishes the basic operating frequency of the inverter, and the other provides an adjustable average voltage output.

Pulse shaping and power driving stages provide the necessary trigger signals for reliable operation of the SCR's. Pulse transformers are utilized for isolation and coupling of the trigger sources and the SCR gates.

When forced commutation of the SCR's is employed, additional circuitry is necessary to eliminate parasitic operation of the inverter. The negative gate current associated with the SCR commutation causes false and random firing of the SCR's when pulse transformers are used. This situation is overcome by utilizing diode bridge circuits in the gate circuit of the SCR's. These circuits eliminate the flow of the negative gate current.

The increase in loss associated with nonsinusoidal waveform inputs to the induction motor is in the order of 20 percent.

# APPENDIX I

## ELECTRONIC CIRCUIT BREAKER

General:

In forced commutation inverter circuits, the fault current due to commutation failure may reach destructive proportions before conventional fuses would melt. This necessitates then, the design of a very fast electronic circuit breaker that will sense the build up of a fault current and provide open-circuit protection.

An SCR current limiting circuit breaker is illustrated in Figure 27. In this circuit, the load current passes through the breaker SCR, a reactor, and a current sensing resistor. The reactor limits the rate-of-rise of the fault current to a value within the limits of the breaker SCR.

A unijunction circuit provides a trip signal when a fault condition is detected. The unijunction circuit is held below its firing point by approximately 200 mv; this point is set by the trip adjust resistor. The value of the current sensing resistor, R, is selected such that a 200 mv signal is developed across it when the level of a fault condition is reached. This 200 mv signal will cause the

unijunction to fire and the trip SCR will force commutate the breaker SCR and place the load in an open-circuit state.

Manual operation of the breaker is provided by the close and trip controls. These controls provide gate signals to the breaker and trip SCR's respectively.

The General Electric 2N3658 SCR is selected for this application. This SCR has the following ratings:

35 amperes,

400 volts,

200 volts/micro-second,

400 amps/micro-second, and

10 micro-second turn off.

This breaker provides open-circuit protection against fault currents for operating current levels up to 35 amperes and operating voltages up to 400 volts DC. The selection of the sensing resistor R determines the level at which the breaker will operate and switch to the open-circuit state. The value of this resistor R, based on the trip current $I_t$ is given by

$$R \doteq \frac{.2}{I_t}$$

By selecting an SCR, such as the 2N3658, the breaker will operate and open-circuit the load within a period of 10 micro-seconds, which provides adequate protection for the devices used in an inverter.

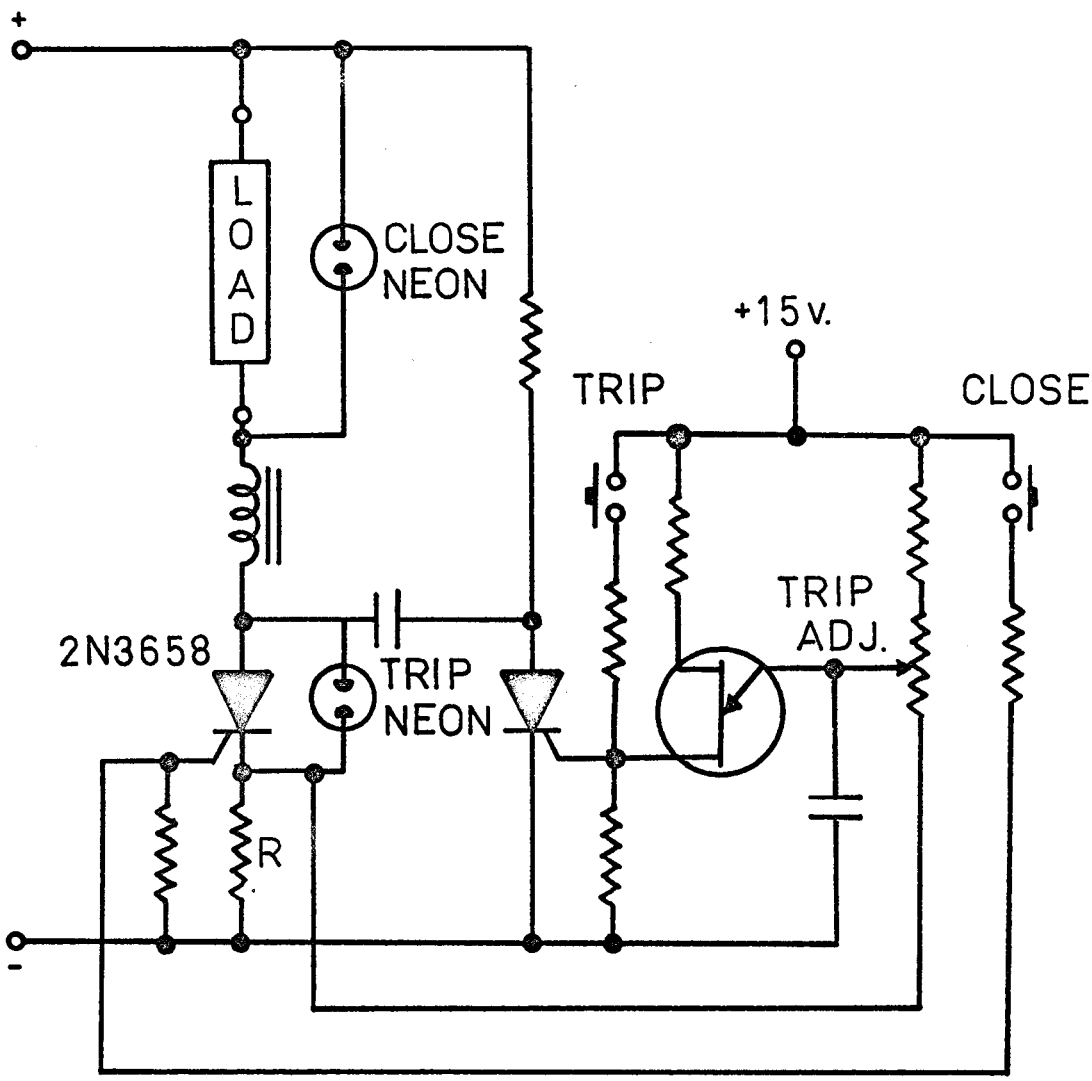



Figure 27. Electronic breaker.

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