PERFORMANCE ENHANCEMENT OF EVAPORATED THIN FILM FIELD EFFECT TRANSISTORS

PERFORMANCE ENHANCEMENT OF EVAPORATED THIN FILM FIELD EFFECT TRANSISTORS

by

FRANK JOSEPH VALLO, B.A.Sc.

A Thesis

Submitted to the Faculty of Graduate Studies

in Partial Fulfillment of the Requirements

for the Degree

Master of Engineering

McMaster University

August 1969.

MASTER OF ENGINEERING (1969) McMASTER UNIVERSITY
(Electrical Engineering) Hamilton, Ontario.

TITLE: Performance Enhancement of Evaporated Thin Film Field Effect Transistors.

AUTHOR: Frank Joseph Vallo, B.A.Sc. (University of Toronto).

SUPERVISOR: Professor C. K. Campbell.

NUMBER OF PAGES: (viii); 83.

SCOPE AND CONTENTS:

Evaporated thin film Field Effect transistors were investigated in an attempt to improve their performance. High resolution masks were constructed to facilitate the evaporation of the devices. Subsequent treatment was examined as a means of improving device stability. As well, some mask manipulation was tried as a means of reducing interelectrode capacitances.

The construction of the devices is discussed with particular reference to cleaning techniques. An attempt is made to relate instability problems in thin film devices to those encountered in MOS devices. Techniques such as mask construction, bonding, and packaging are also described.

ABSTRACT

Device performance as a function of post deposition treatment was studied for evaporated thin film Field Effect Transistors. The generation of suitable masks for device construction was also investigated.

The masks were formed using a nickel electroform process on thin copper foils suspended in a stainless steel blank. The minimum dimension on a mask pattern was .0015 inches.

A staggered electrode structure was employed. The electrodes, semiconductor, and insulator were constructed from Aluminum and Gold, Cadmium Sulphide, and Silicon Monoxide respectively.

Completed devices were bonded, heat treated, and sealed in an atmosphere of dry Nitrogen. The devices were tested for their current-voltage characteristics, their transconductance, and stability. The transistors operated satisfactorily to 50 KHz and showed improved stability. Good saturation characteristics were observed and transconductances of 10 μmhos were measured.

The importance of cleanliness in device preparation is discussed and a comparison with MOS devices is made.

ACKNOWLEDGEMENTS

The author wishes to show his gratitude for the interest and guidance shown by Dr. C. K. Campbell throughout this work.

Special thanks are due Dr. H. I. Ralph for his willingness to answer countless questions and his help in dark moments.

In particular I wish to thank Mr. D. Kuenzig and members of the Research Division of Aerovox Canada Ltd., for their valuable help in the construction of masks without which this thesis would have been impossible.

Canadian Westinghouse Co.Ltd. supplied valuable information on bonding and packaging.

I have also profited from discussions with the following people: Dr. R. C. Dynes, Dr. D. Barber, Dr. S. H. Chisholm, Mr. Jim Carson, Mr. Bob Clarke, Dr. J. Shewchun and Dr. J. S. Kirkaldy.

Dr. J. Shewchun kindly allowed the author the use of his research facilities.

Mr. W. Armstrong of Arbell Equipment has been helpful in solving some of the author's bonding problems.

It has been a pleasure collaborating with Mr. P. L. Swart, on many of the ideas that have come up in the course of this work. His encouragement proved invaluable.

This project was financed through a grant-in-aid from the National Research Council of Canada to Dr. C. K. Campbell. The author is also indebted to McMaster University for financial support in the form of a McMaster Assistantship.

Finally the author wishes to express his appreciation to Mr. J. Van Nynatten and Mrs. Intson for their help in the preparation of this manuscript.

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CHAPTER I

INTRODUCTION

1.1 INTRODUCTION.

Passive thin film circuit elements have been successfully deposited and are commercially available at this time. However the realization of the totally evaporated circuit has been held back for some time by the Thin Film Field Effect Transistor, referred to as the TFT or FET from here on. Some of the associated problems with the TFT have been: poor reproducibility, degradation with time, and marked instability. In comparison the passive circuit elements exhibit good stability, over large temperature ranges, and long periods of time.

For the present, the disadvantages of the TFT are overcome in Hybrid Circuits which contain thin film passive elements and silicon chip active elements. Once the problems of the TFT are solved the completely evaporated thin film circuit may supercede both the IC and Hybrid Circuit in some applications, such as digital to analog conversion.

Many methods are available for deposition of thin film

components. In the experiments described in this thesis, material is evaporated from resistively heated sources in a high vacuum. The vapour thus produced is condensed onto a thin flat insulating sheet called the substrate. The various patterns for a particular device are produced by placing masks close to the substrate. This is known as the additive method of device fabrication.

The masks can consist of thin flat foils with appropriate apertures corresponding in shape to the desired film pattern. The mask method has several advantages and therefore this method is the one used for the purposes of this thesis. It should also be noted that the pattern can be generated by using selective pattern etching. In this case the entire side of the substrate is coated with the desired material. Photo-resist techniques and etching are then used to produce the desired effect.

The properties of the deposited film can be controlled by varying the substrate temperature, rate of deposition, and residual gas pressure. All three techniques are used in the experimental work described in this thesis. The properties of the deposited device are controlled by varying the film thickness and device geometry.

1.2 SCOPE OF THIS THESIS

In this thesis we are interested in improving the performance of TFT's. Specifically we are interested in improving the stability of the devices with time.

A modified version of the basic transistor structure employed by Weimer[1] was used in the experiments. The deposition method and deposition parameters for the TFT's were the same as those used by Morgan[2].

A high precision mask system allowed a simultaneous deposition of forty transistors in groups of five, together with eight four-terminal test devices. The transistors could then be tested individually or in parallel groups of five. The four-terminal devices, employing resistivity and hall measurements, could be used in an analysis of the semiconductor. These devices were evaporated in a checkerboard pattern, alternating with the transistors. In this way the samples could give a good indication as to how the film varied over the exposed area of the substrate.

Cleaning techniques were examined and steps were taken to ensure cleanliness and minimum contamination in the completed devices.

Heat treatment was used as a tool in the stabilization of the completed transistors. Previous devices as developed

by Morgan[2] showed a marked hysteresis loop in their current-voltage characteristics, as well as a slow drift in their family of curves: Also their shelf life was short.

The theory for the devices is discussed in Chapter 2. A field effect model is developed in order to analyze the theoretical behavior of the experimental thin film transistors.

CHAPTER II

THEORY OF THE FIELD EFFECT TRANSISTOR

2.1 INTRODUCTION

The operation of the TFT is discussed in this chapter. The overall I-V characteristics are derived for the TFT operating in the Enhancement mode.

Possible mechanisms for the behavior of the pinch off region are included in the discussion.

2.2 THE FIELD EFFECT TRANSISTOR

Shockley[3] first proposed the theory for Field Effect Transistors. His development of the theory involved the application of an electric field to the semiconductor by means of a back biased P-N junction at the gate. Borkan and Weimer[4] in their work, suggested that the theory for the TFT's was similar to Shockley's theory. In fact, Johnson[5] shows that the equations governing the behavior of the Insulated Gate Transistor are similar to those for the Junction Gate Transistor. A summary development including these theories follows.

(a) Assumptions

In this thesis, unless otherwise specified the following important assumptions are made:

i) The gradual approximation holds (it is explained in the body of the theory).

ii) Mobility remains constant.

iii) Surface states are absent.

iv) All donors are ionized.

v) The occupation of traps is spatially independent.

vi) The thermodynamic limit is assumed; that is the shape of the electrostatic potential is smooth and well defined, in fact equal to the time average of the electrostatic potential. This further assumes a small noise level.

vii) The semiconductor is non-degenerate.

(b) The Junction Gate Field Effect Transistor

The Junction Gate Field Effect Transistor will be considered first. The structure is illustrated in Figure 2-1.

Although Shockley considers a symmetrical structure it is equally valid to consider the above structure since the

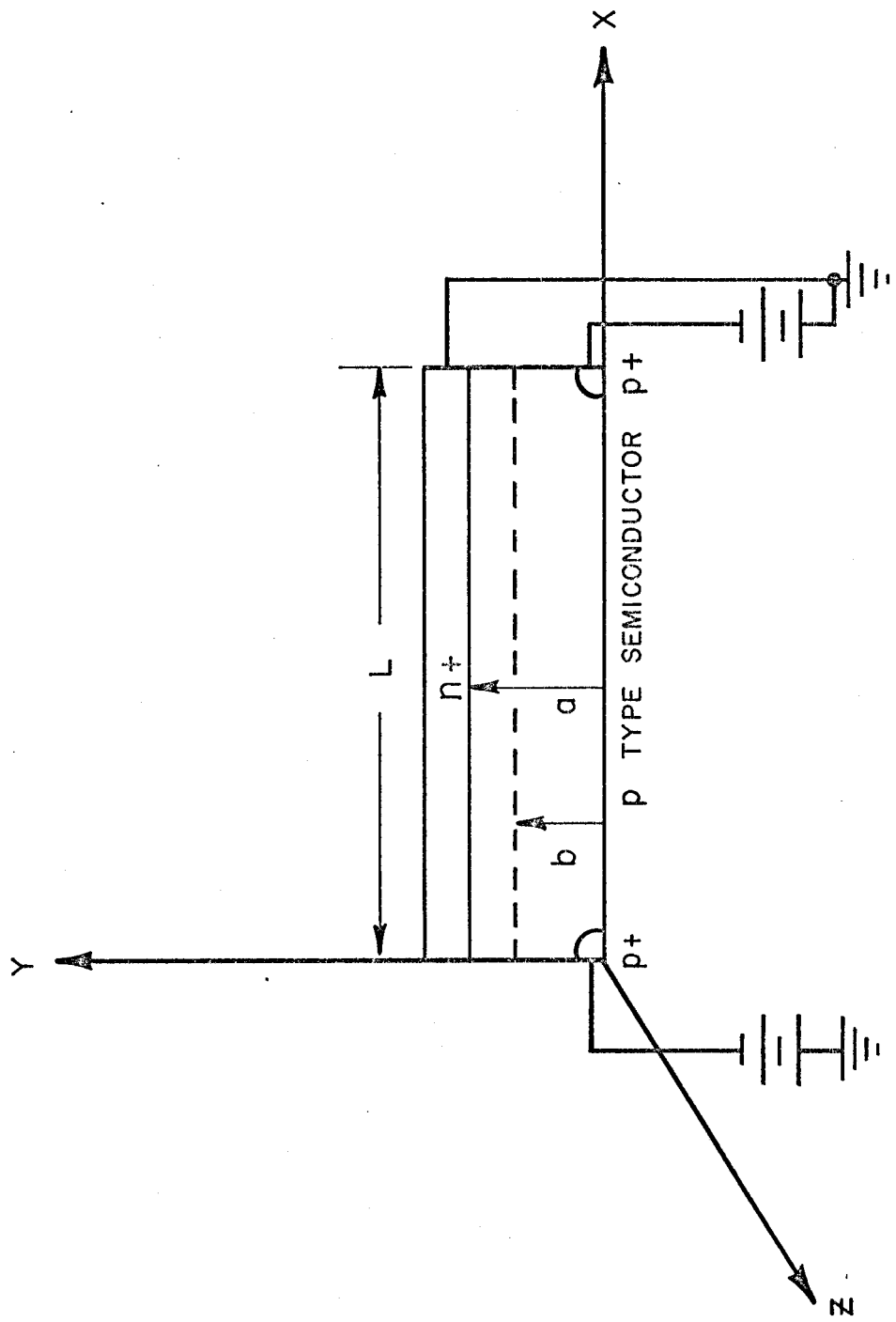


FIG. 2-1 THE JUNCTION GATE FIELD EFFECT TRANSISTOR.

analysis remains substantially unchanged.

The gate region is heavily doped n-type semiconductor and the channel is p-type. Under operating conditions current is carried by holes flowing in the x direction in the p-type layer. The P-N junction is back biased forming a space charge region, thereby restricting the current flow to a channel of p-type material. In the diagram shown, the reverse bias is greater at one terminal thereby narrowing the channel at one end.

We wish to relate the conductance of the channel to the applied gate bias. This can be achieved in the following manner. First of all Poisson's Equation may be written as

$$\varepsilon\varepsilon_0 \frac{d^2V}{dy^2} = - \varepsilon\varepsilon_0 \frac{dE}{dy} = - \rho(y) \qquad \ldots(2:1)$$

$E(y)$ the electric field in the y direction

y the distance through the p-type layer

$V(y)$ the electrostatic potential in the y direction

ε the relative permittivity

ε_0 the permittivity of free space

$\rho(y)$ the charge density

The equation is written in one dimension since $\nabla^2 x$ has a negligible contribution and $\nabla^2 z$ is zero. This follows

directly from the gradual approximation and from the absence of an electric field in the z direction.

The gate region and space charge region form a dipole layer in which the charges add to zero. This must be the case otherwise Gauss' theorem would require an electric field to exist beyond the boundaries of the layer.

The penetration of space charge in the n+ gate region is much less, justifying the assumption that the space charge is located primarily in the p region.

The doping of the regions defines the charge densities:

P region $\rho_0 = q(N_a - N_d)$ ...(2:2a)

n+ region $\rho n = q(N_d - N_a)$ ...(2:2b)

where N_a the number of acceptor levels

N_d the number of donor levels

The following boundary conditions are now assumed:

$$E_y = 0 \text{ at } y = b \qquad \ldots(2:3)$$

$$\frac{dE_y}{dy} = \frac{\rho}{\varepsilon_s \varepsilon_0} = \frac{-\rho_0}{\varepsilon_s \varepsilon_0} \quad y>b \qquad \ldots(2:4)$$

This last condition assumes complete depletion.

A solution of Poisson's Equation under these conditions is:

$$E_y = -\rho_0 \frac{(y - b)}{\varepsilon_s \varepsilon_0} \qquad \ldots(2:5)$$

as shown in Figure 2:2b for y<a.

When y>a, (a-b) $\rho_0 = \rho_n$ (thickness of space charge layer in the n region). Therefore at y = a+, E_y vanishes.

Inspection of Figure 2:2b shows that the average electric field is the same in both regions. This means that the potential difference across each region is proportional to its thickness. It is then safe to assume that the potential drop occurs wholly in the space charge region.

The potential is therefore:

$$V = (\rho_0/2\varepsilon_s\varepsilon_0) \; [(y-b)^2 - (a-b)^2] \qquad ...(2:6)$$

The constant of integration is chosen to make V = 0 at y = a corresponding to grounding the n+ region.

In the channel equation (2:6) reduces to:

$$V = -\rho_0/2\varepsilon_s\varepsilon_0 \; (a-b)^2 \qquad ...(2:7)$$

Equation (2:7) may be rewritten:

$$W = V(b) = [1 - (b/a)]^2 \; W_0 \qquad ...(2:8)$$

where $$W_0 \equiv \rho_0 a^2/2\varepsilon_s\varepsilon_0 \qquad ...(2:9)$$

W_0 is referred to as the "pinch-off voltage" since it will reduce the channel to zero and pinch-off the conducting path.

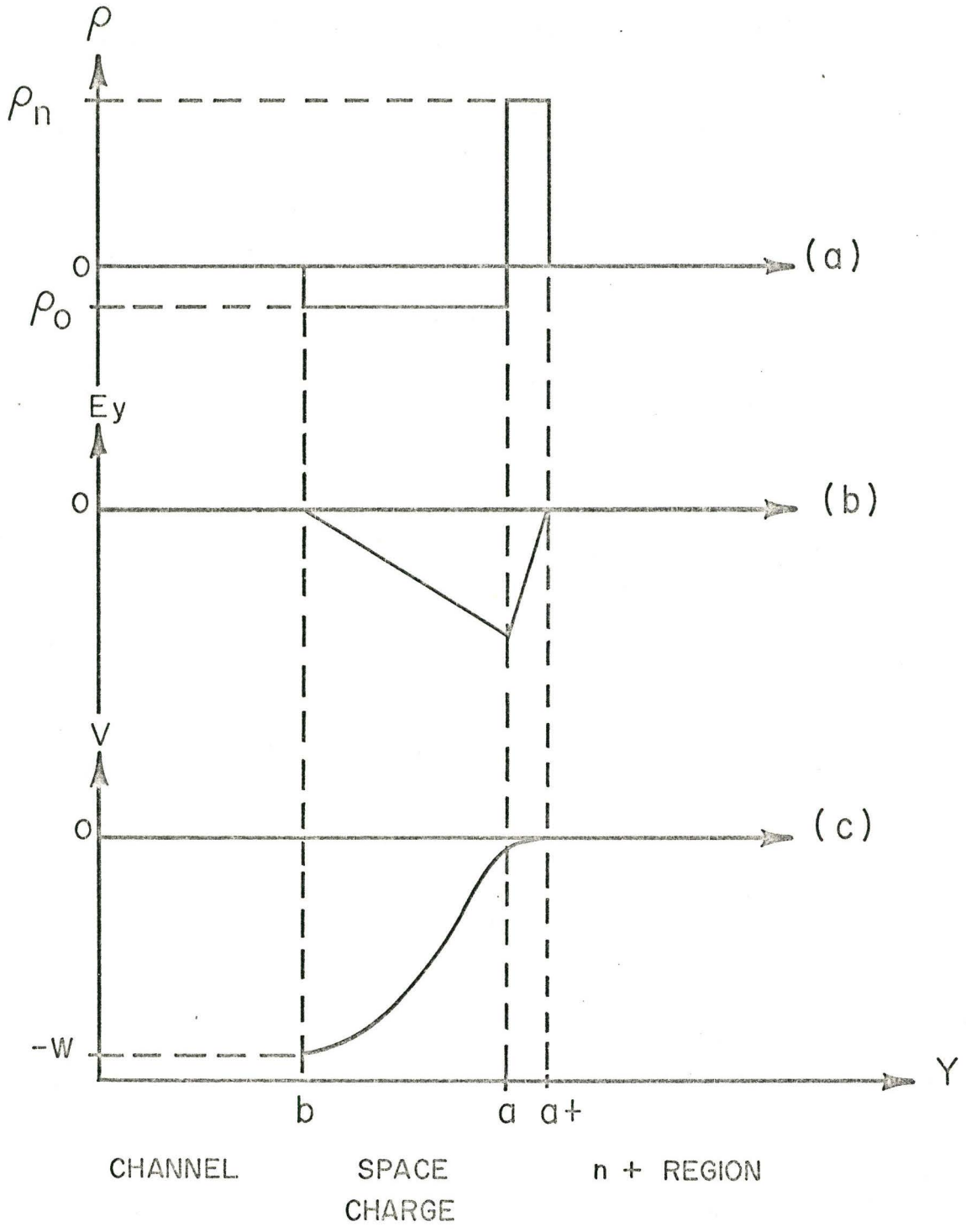


FIG. 2-2 SPATIAL PARAMETERS OF THE JUNCTION GATE FIELD EFFECT TRANSISTOR.

(a) SPACE CHARGE

(b) ELECTRIC FIELD

(c) ELECTROSTATIC POTENTIAL.

The case of different reverse bias at either end of the channel may be denoted by W and W + ΔW. The original assumption of a gradual channel imposes the restriction that $\Delta W << W_0 - W$. Under these conditions the conductivity of the channel may be written:

$$\sigma_0 = \mu_0 \rho_0 \qquad \ldots(2:10)$$

where μ_0 is the mobility of holes in the p type semiconductor.

The current per unit length in the z direction will therefore be

$$I = b\sigma_0 E_x = g(W) E_x \qquad \ldots(2:11)$$

where

g(W) is the conductance of a unit square of the channel

E_x is the electric field in the x direction.

If the channel changes its width appreciably we must include the effect of W and b. Using equation 2:8 the following important equation results:

$$g(W) = \sigma_0 b(W) = [1 - (W/W_0)^{\frac{1}{2}}] g_0 \qquad \ldots(2:12)$$

where

$g_0 = \sigma_0 a$ (the conductance of a unit square of the

p region under zero bias conditions).

Before considering the Insulated Gate Field Effect Transistor the gradual model should be discussed. In writing Poisson's Equation we assumed that

$$\frac{\partial^2 V}{\partial x^2} \simeq 0 \qquad \ldots(2:13)$$

However when current flows

$E_x = -\frac{\partial V}{\partial x} \neq 0$ and in general $\frac{\partial^2 V}{\partial x^2}$ will not vanish. If the one dimensional case is considered the reverse potential W(x) will be the same function of b(x) as for the case of I = 0. This is true, only if conditions vary along the channel gradually. We can write:

$$W = W[b(x)] \qquad \ldots(2:14)$$

Earlier on, in establishing W(b), we assumed that $E_y = 0$ at y = b which is a good approximation for the gradual model. Practically, at the edge of the channel $-\frac{Ey}{E_x} = \frac{db}{dx}$ and for the gradual model this must be much less than unity. If this is not the case the channel narrows abruptly and the analysis fails.

Since g is a function of b (equation 2:12) and, b and W are related (equations 2:8 and 2:9) we may write

$$I = g(W)\, dW/dx \qquad \ldots(2.15)$$

From 2:8 and 2:9

$$dW = -(a - b)\,\rho_0\,\frac{db}{K} \qquad \ldots(2:16)$$

Eliminating dW

$$I\,dx = g(W)dW$$

$$= -g_0\,(a - b)\,(b\rho_0/aK)\,db$$

$$= -I_0\,a\,(1 - u)u\,du \qquad \ldots(2:17)$$

where I_0 = the current at zero gate bias

$u \equiv b/a$ or the fraction of the p layer occupied by the channel.

At $u = 0$, and $u = 1$, $\frac{dx}{du}$ is zero indicating that the channel is changing its width with an infinite value of $\frac{db}{dx}$.

Integrating to obtain x and setting $x = 0$ when $u = 0$; we obtain

$$x = -(aI_0/I)\,[(u^2/2) - (u^3/3)] \qquad \ldots(2:18)$$

The shape of the channel is shown in Figure 2-3.

It can be seen that conditions for the gradual case do not hold unless $(I_0/I) > 18$ or L(I) is greater than 3a, where L(I) may be represented by

$$L(I) = (a/6)\,(I_0/I) \qquad \ldots(2:19)$$

A useful criterion for the gradual approximation can be obtained if a length a of the channel is considered. If we require that over this distance the fractional change in channel width is small then:

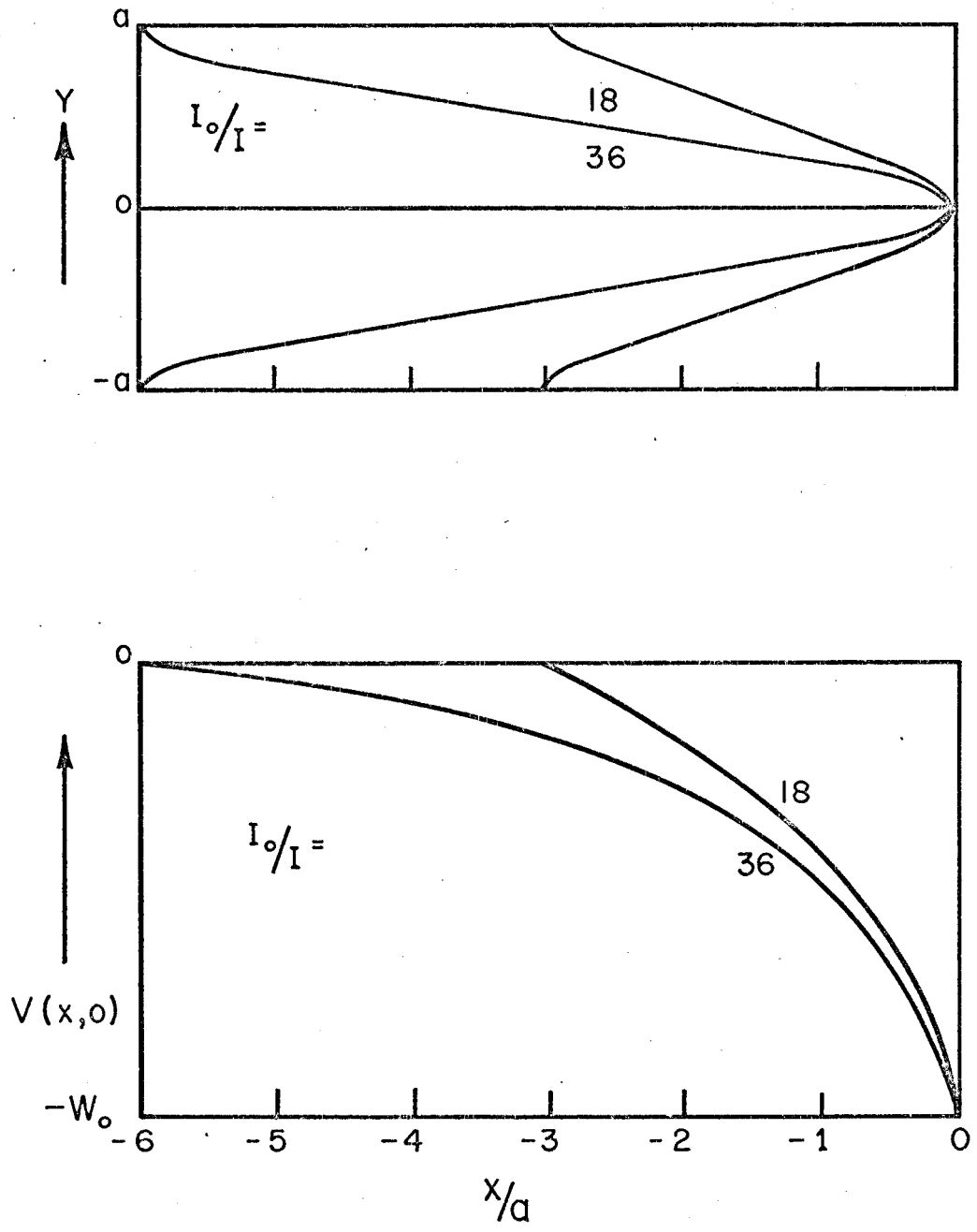


FIG. 2-3 THE GRADUAL APPROXIMATION.

(a) CHANNEL CONTOUR

(b) ELECTROSTATIC POTENTIAL

$$a\, db/dx < b \qquad \ldots(2:20)$$

or

$$(a/b)(db/dx) < 1 \qquad \ldots(2:21)$$

which means that db/dx is small and the arguments given earlier hold.

(c) The Insulated Gate Field Effect Transistor[5&6]

Next, the equations for the insulated gate field effect transistor are derived.

The altered structure is shown in Figure 2-4.

Due to the insulating layer which is blocking for both positive and negative polarities of gate voltage this transistor exhibits two types of behavior, enhancement and depletion. In contrast the p-n junction is blocking for one polarity only and depletion is the single mode of operation.

I Depletion Mode of Operation

Let us consider the depletion type of behavior, that is reduction of drain current from the zero gate bias value. The insulating layer is assumed to be uniform and free of charges. We shall consider the semiconductor to be n type and further to be free of built in potentials and traps.

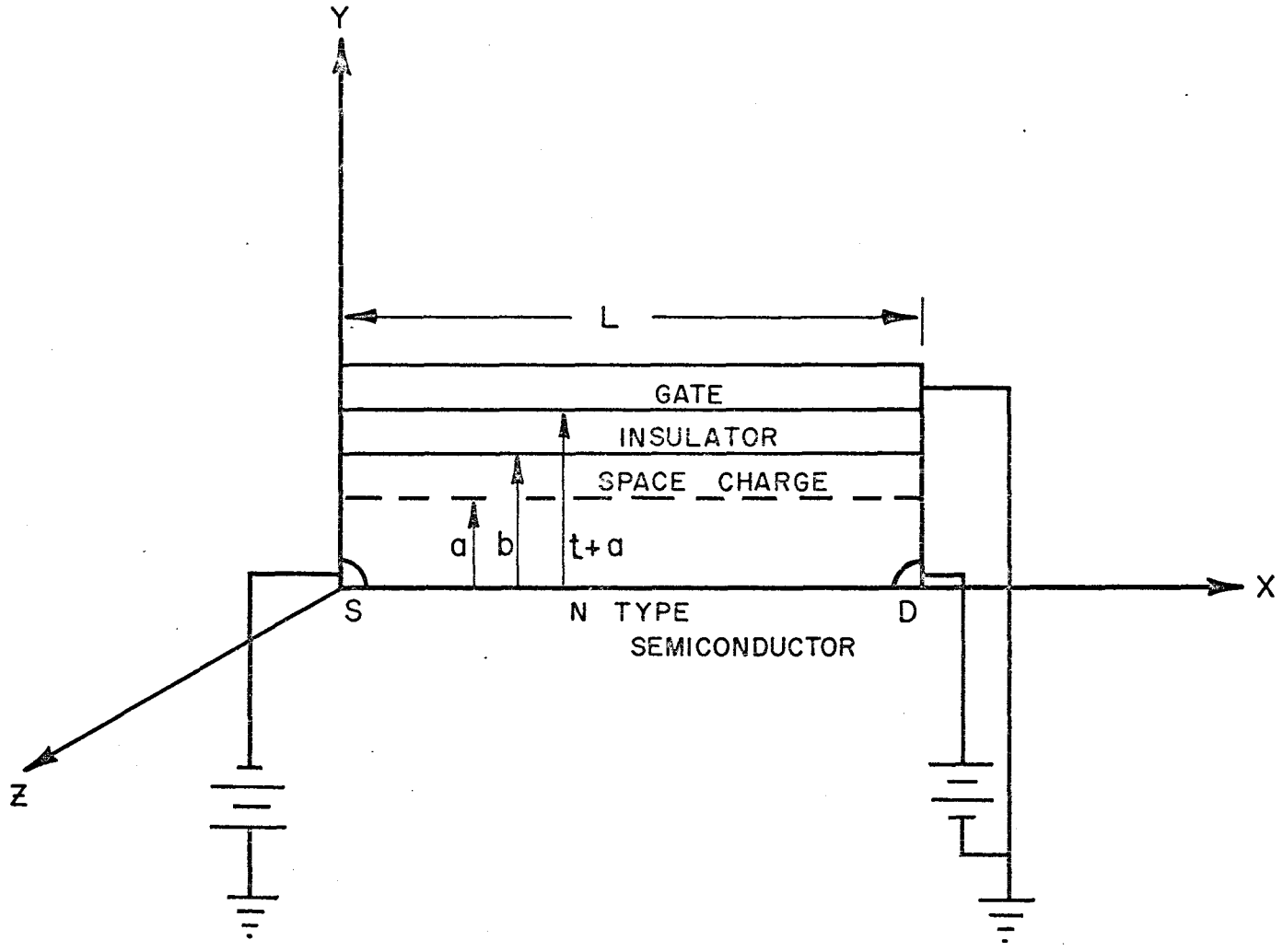


FIG. 2-4 THE INSULATED GATE FIELD EFFECT TRANSISTOR.

The charge density in the semiconductor is

$$\rho_0 = q\,(N_d - N_a) \qquad \ldots(2.22)$$

The depletion condition arises when the gate bias is negative.

Applying Poisson's Equation as before and solving for the electric field:

$$E_{sy} = \rho_0(y - b)/\varepsilon_s\varepsilon_0 \qquad \ldots(2:23)$$

The field in the insulator is constant and may be found from the requirement that the displacement vector must be continuous across the interface.

$$\varepsilon_I E_I = \varepsilon_s E_s \quad E_s \text{ evaluated at } y = a \qquad \ldots(2:24)$$

It follows from 2:23 and 2:24 that

$$E_{Iy} = \frac{\rho_0\,(a-b)}{\varepsilon_0\varepsilon_I} \qquad \ldots(2:25)$$

The potential difference across the insulator and semiconductor is obtained by integration of 2:23 and 2:25.

$$W_I = \frac{\rho_0}{\varepsilon_0\varepsilon_I}\,(a-b)\,t \qquad \ldots(2:26)$$

$$W_s = \frac{\rho_0}{2\varepsilon_0\varepsilon_s}\,(a-b)^2 \qquad \ldots(2:27)$$

The net potential difference W is just the sum of

W_S and W_I

$$W = \frac{\rho_0}{2\varepsilon_0\varepsilon_S} (a-b)^2 \left(1 + \frac{2\varepsilon_S}{\varepsilon_I} \frac{t}{(a-b)}\right) \quad ...(2:28)$$

The pinch off voltage W_0 is

$$W_0 = W_0' (1 + 1/y) \quad ...(2:29)$$

where

$y = \frac{W_S}{W_I}$ and W_0' is Shockley's pinch off voltage.

The unit square conductance of the partially depleted channel is

$$g(W) = G_0 \left(1 - \frac{a-b}{a}\right) \quad ...(2:30)$$

where

$$G_0 = \rho_0 \mu a \quad ...(2:31)$$

Equation 2:30 is obtained by evaluation of the ratio $\frac{a-b}{b}$ in terms of the ratio $\frac{W}{W_0}$. The ratio is obtained by taking the ratio of 2:28 to 2:29.

$$\frac{W}{W_0} = \frac{(a-b)^2}{a^2} \left[\frac{1 + 2\ t\ \varepsilon_S/(a-b)\varepsilon_I}{1 + 2\ t\ \varepsilon_S/a\varepsilon_I}\right] \quad ...(2:32)$$

Solving for $\frac{(a-b)}{a}$

$$\frac{(a-b)}{a} = -1/2\ y + 1/2\ y \left[1 + 4.y\ (y + 1)\frac{W}{W_0}\right]^{\frac{1}{2}}$$

$$...(2:33)$$

The positive root is chosen since the ratio is positive as $\frac{W}{W_0}$ increases. Substituting into equation 2:30 from 2:33

$$g(W) = G_0[1 + 1/2\ y - 1/2\ y\ [1 + 4\ y\ (y + 1\ )\ \frac{W}{W_0}]^{\frac{1}{2}}] \qquad ...(2:34)$$

II ENHANCEMENT MODE OF OPERATION

The enhancement behavior can be shown from a different approach.

The device is considered as a capacitor and resistor series combination. The Source and Drain electrodes are considered to be at the same potential and the gate electrode at a higher potential W.

The total charge at the interface is

$$Q = - CW \qquad ...(2.35)$$

where $$C = \varepsilon_I \varepsilon_0\ (\text{AREA})/t \qquad ...(2:36)$$

The charge is uniformly distributed to a depth d with a density n_s

$$Q = n_s\ d\ q\ (\text{AREA}) \qquad ...(2:37)$$

Substituting from 2:36 and 2:37 into 2:35

$$n_s\ d\ q = \frac{\varepsilon_I \varepsilon_0 W}{t} \qquad ...(2.38)$$

The enhanced conductance of a unit square of the channel can be written

$$g(W) = n_s dq\mu \qquad \ldots(2:39)$$

substituting from 2:38 into 2:39

$$g(W) = \frac{\varepsilon_I \varepsilon_0 W\mu}{t} \qquad \ldots(2:40)$$

which is the conductance of a unit square of the channel.

The current-voltage characteristic can be obtained by integration of the conductance function, that is:

$$I_D \int_0^L dx = \int_{W_D}^{W_S} g(W)\, dW \qquad \ldots(2:41)$$

which yields

$$I_D = \frac{\varepsilon_0 \varepsilon_I \mu}{2tL} (W_s^2 - W_D^2) \qquad \ldots(2:42)$$

$$I_D \doteq \frac{\varepsilon_0 \varepsilon_I \mu}{tL} [(V_g - V_{D/2}) V_D - (V_g - V_s/2) V_s] \qquad \ldots(2:43)$$

This equation breaks down when the gradual approximation fails. That point is reached before pinch-off. The pinch-off region must therefore be treated separately.

Weimer's equation[4] for the Thin Film Transistor operated in the enhancement mode reduces to this equation in the absence of surface states.

Referring all voltages to the source and including

surface states equation 2:43 can be written as

$$I_d = \frac{\mu C}{L^2} \left[(V_g - V_0) V_d - \frac{V_d^2}{2} \right] \qquad \ldots(2:44)$$

where V_0 is the initial gate bias to fill immobile surface states and/or traps in the forbidden band of the semiconductor. This equation assumes a sudden turn on of the transistor.

The form of I_d vs V_d for increasing values of V_g is shown in Figure 2-5

(d) Operation of Field Effect Transistors in the Pinch-Off Region.

Referring to the earlier discussion it was found that at some critical gate and drain voltage the channel would pinch off, that is the space charge layer would occupy the thickness of the semiconductor at some point in the channel.

For the gradual model, potential along the channel changes due to a variation in majority carrier charge per unit length. As pinch-off is approached the hole charge becomes negligible and there is no further variation in the potential from this cause.

At pinch-off a portion of the channel becomes depleted.

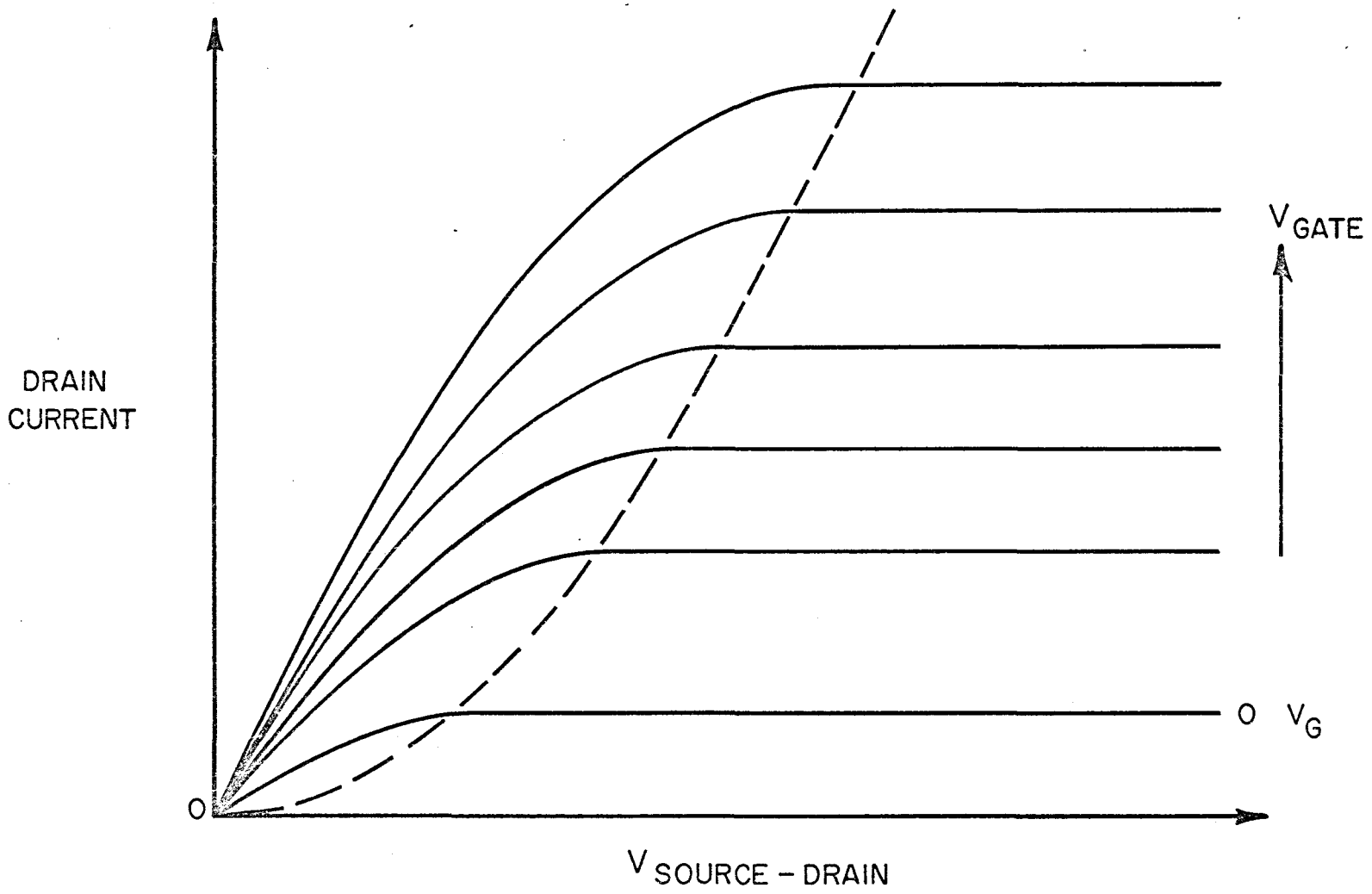


FIG. 2-5 THEORETICAL I-V CHARACTERISTICS OF THE INSULATED GATE FET.

Any increase in drain voltage changes the potential thereby increasing the depletion region. It does not, however, add any more charge carriers and the drain current remains constant - giving rise to the saturated region in the family of curves.

In the pinch-off region $\frac{\partial I_D}{\partial V_D} = 0$ in the ideal case. However for practical devices $\frac{\partial I_D}{\partial V_D}$ is not zero but has some small finite value. Some explanations have been advanced to explain this behavior.

Johnson[5] assumes that the donors present in the semiconducting layer are only partially ionized. The saturation region then corresponds to ionization of donors in deeper lying states. In this situation saturation would occur only at drain voltages greater than the transistor could withstand.

Another explanation put forth by Haering[7], suggests that a leakage conductance in parallel with the channel gives rise to the slope of the saturated region. In the standard asymmetrical structure for the TFT, surface states may be formed at the semiconductor substrate interface. These fix the surface potential at a value which remains relatively unaffected by the gate voltage. O'Hanlon[8] has shown that the surface potential can be controlled by appropriate deposition of insulator at this interface. Large values of

saturation resistance have been obtained this way.

Lately, Grebene and Ghandi[9] have suggested that for a junction gate field effect transistor complete pinch-off does not occur. Part of the channel becomes depleted while the rest remains conducting. In the depletion region a relatively narrow strip remains conducting. The finite length of this region is primarily due to the saturation of the carrier drift velocity at high electric field strengths. It can be shown the channel opening at the depleted region is:

$$T = \frac{I_d}{qN_D v_0 Z} \qquad \ldots(2:45)$$

where

I_d = the desired drain current

q = electronic charge

N_d = carrier charge density

v_0 = carrier drift velocity

Z = the width of the channel.

In terms of the physical dimensions and operating point

$$T = \frac{W_0^2 (3a - W_0)}{6} \qquad \ldots(2:46)$$

where

a = the thickness of semiconductor

W_0 = the pinch-off voltage

($W_0 = a(1 - \sqrt{Vg/Vp})$

A solution of Poisson's equation in the region of conduction in the depleted channel, shows good agreement with experiment for low values of gate voltage.

Disagreement at higher values of gate voltage suggests that possibly all the above mentioned mechanisms contribute to the behavior in the saturation region.

CHAPTER III

EXPERIMENTAL PROCEDURES

3.1 INTRODUCTION

The methods and equipment used in the experimental work of this thesis are outlined in this chapter.

3.2 VACUUM COATING UNIT

The preparation of the devices was carried out in a modified Edwards 19E2-type vacuum-coating unit. The standard unit is equipped with a stainless steel bell jar of 19-inch diameter. The interior can be observed through two glass viewing ports. The bell jar is continuously water cooled to prevent expansion of welded joints during bake out procedures.

The pumping system consists of a 9-inch oil diffusion pump backed by a 450 litres/min single stage rotary pump. With Nitrogen cold trapping, an ultimate pressure of 5×10^{-8} torr may be reached in about ten hours. The working vacuum is however normally in the order of 1×10^{-6} torr provided a pause is made between subsequent evaporations. This technique

prevents internal heating of the vacuum system and maintains the sealing quality of the feed through terminals. The low-tension current feed-throughs are water cooled for the same reason.

A high standard of vacuum is maintained by continuous liquid-nitrogen or cold water "cold trapping". The trap consists of a coil of copper tubing inserted in the throat of the diffusion pump. During evaporations, liquid nitrogen is pumped through the trap;* cold water is used at other times. This procedure has the effect of condensing the back streaming vapors of the diffusion pump on the trap, rather than in the bell jar.

Power for resistance heating of filaments is obtained from a 20V low tension transformer capable of supplying 200 amperes. An autotransformer feeding the low tension transformer provides the required regulation. This same autotransformer provides regulation for the high tension supply and the radiant heater.

The high tension supply with a 5KV open-circuit voltage provides a glow discharge for system cleaning.

The system can be baked to a temperature of 400° C.

* Please see page 71, Chapter 5, Results for a departure from this procedure.

with the radiant heater located in the top of the bell jar. The temperature is limited by the ability of the various spring steel components to keep their temper.

3.3 EQUIPMENT AND TECHNIQUES

(a) Microcircuit Jig Assembly

The devices described in this thesis are made during one pump down cycle of the vacuum system. This is possible because of the microcircuit jig assembly located in the bell jar. The jig assembly is suspended in the bell jar by a tripod stand and is anchored in place with a 1/4 inch stainless steel top plate. The assembly itself attaches to this plate. It consists of two rotating plates which are positioned, one above the other, by means of two conical position pins. The lower plate carries a complement of 6 masks which can be raised into close contact with the substrate assembly during an evaporation. The upper plate is a circular substrate magazine having six substrate positions which rotate about the same axis as the lower plate. During a mask change the lower plate is lowered approximately 3/4 inch. It is then rotated one sixth of a revolution, finally moving up to contact the substrate. After six consecutive mask changes the mechanism is so coupled as to move a new substrate into position. The whole operation is done with a Geneva mechanism

giving a positional accuracy of ± .001 inch. This accuracy is somewhat better for positioning normal to the direction of rotation.

The support plate has three ports; one for loading substrates and the other two for substrate heaters. The first a pre-heater, is capable of raising the substrate temperature to 150° C. while the main heater is capable of effecting a substrate temperature up to 300° C. The substrate temperatures are monitored by a thermocouple located in each heater. Radiant heat is also monitored by a thermocouple, located close to, but not in physical contact with, the micro-circuit assembly. The substrate thermocouples, however, do not accurately indicate the substrate surface temperature which may be as much as 60° C. lower than indicated.

A film thickness monitor, as described in the following section, uses a quartz crystal which is mounted on top of the jig. It is located close to the substrate coating position and very nearly normal to the vapor stream. Effects of temperature changes are minimized by three baffles surrounding the crystal.*

An indexed turret head is located approximately 6 inches

* Please refer to page 65, Chapter 5, Results, for a modification to this system.

below the mask plate. Any one of six different materials may be evaporated from this head. A mechanical shutter is mounted over the turret so that a source may be heated up and outgassed without contaminating the substrate with undesirable deposits. An additional shutter is located close to the substrate evaporating position. It consists of a solenoid which, when energized, uncovers a hole in a plate covering the turret head. The crystal can monitor the vapor stream and the rate of evaporation may be set without exposing the substrate. The evaporation can therefore begin and end sharply by activating and deactivating the solenoid shutter.

(b) Film Thickness Monitor

The quartz crystal monitor is a convenient method of film thickness measurement. At the same time that a film is deposited on the substrate, a film is also deposited on a quartz crystal as described in the previous section. The resultant increase in mass of the crystal causes its natural oscillating frequency to decrease. This frequency change is linear with mass change, provided that the variation of mass is small. The oscillator is mounted under the baseplate of the coating unit in order to reduce lead capacitance. This mounting allows for the shortest lead length without the complication of introducing the circuitry into the vacuum system. The crystal is a 6 MHz AT cut crystal[10]. The

oscillator which is transistorized is followed by an emitter follower. The signal is then measured by a frequency counter or a meter with suitable conversion.

The monitor can be calibrated by preparing a special slide with a step in the deposited film. The frequency change is noted and the film thickness is measured with an optical interferometer.[11] A number of such measurements are plotted on a graph. From this plot, an empirical relationship is obtained relating film thickness to frequency change for a given material.

For the particular monitor used in the experiments here, Groth[12] has determined the following relationship:

$$t = \frac{2.80\ \Delta f}{\rho_m}$$

where t - film thickness in Å^{o}

Δf - frequency change in Hz

ρ_m - density, $gm./cm^3$

The maximum frequency change which may be measured with the 6 MHz crystal system is 200 KHz. Above this range the frequency is no longer linear with mass change and the crystal must be replaced.

(c) Substrates

The substrates used in all experiments discussed in

this thesis were Corning #2 cover glass slides 25 mm. square by .007 inches thick. The cleaning of these substrates is discussed in part (d) of this section.

The substrates were clamped to a 2 inch x 2 inch x 1/4 inch spacer in order to maintain good thermal contact with the substrate heaters. The spacers were spring loaded to prevent movement during mask changes.

The substrate holder is shown in Figure 3-1.

There are three position pins to facilitate positioning if it becomes necessary to remove the substrates at some point in the evaporation. The glass slides are held in place with three Allen key machine screws and teflon washers.

(d) Cleaning Procedures

As discussed in Chapter 4, the problem of cleanliness in Thin Film deposition is of paramount importance. Consequently, in this thesis, particular attention was paid to the following: substrates, substrate holders, masks, vacuum system, material sources, and completed devices.

Care was taken to ensure that the substrates were absolutely clean before films were deposited on them. First, they were ultra-sonically cleaned in a Heat Systems Model HD-50 ultra-sonic cleaner. A solution of Cutscum detergent (mixed

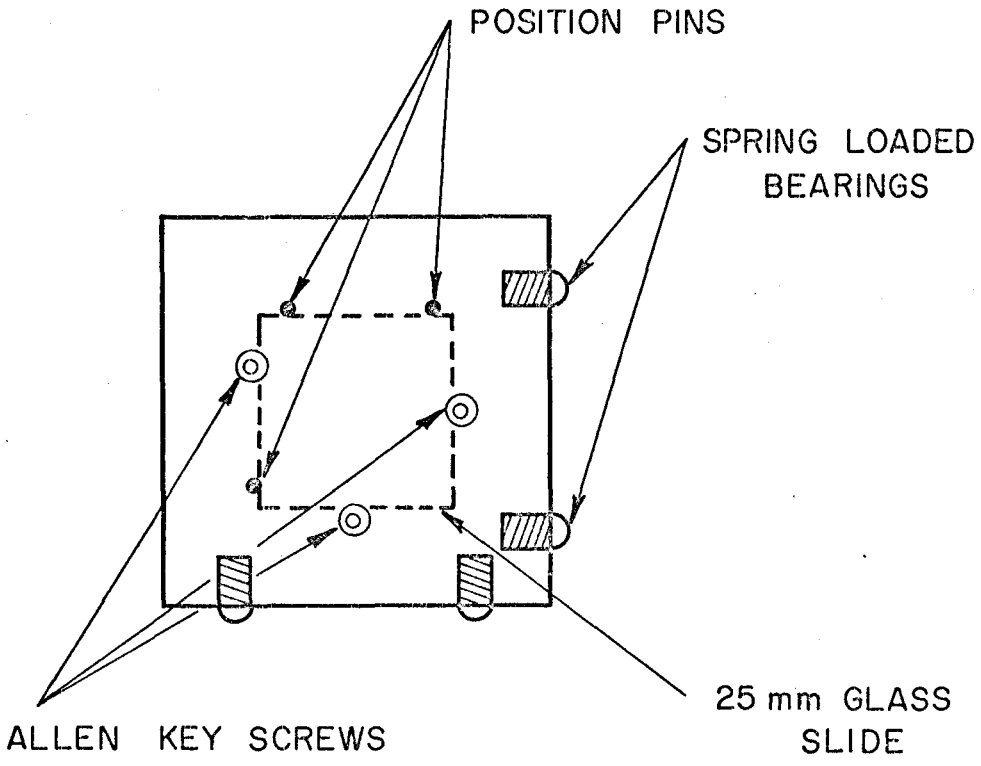


FIG. 3-1 SUBSTRATE HOLDER.

in the proportion 8 oz. to 160 gallons of distilled water) was used. This treatment continued for fifteen minutes. The substrates were then transferred to distilled water for another fifteen minutes. This stage of the cleaning was then completed, with an Isopropyl Alcohol bath for five minutes.

Prior to use or storage the substrates were subjected to an Isopropyl "vapor degrease bath" for fifteen minutes. A diagram of the apparatus is shown in Figure 3-2.

A vacuum chamber at 1 torr and room temperature was used for storing the substrates. Prior to use, the slides were again degreased for fifteen minutes. The slides were handled with rubber gloves and tweezers at all stages of cleaning, while the gloves and tweezers themselves were cleaned with Sparkleen.

After every evaporation, the holders were scrubbed with a toothbrush, and Sparkleen. This was followed by a rinse in distilled water and ultra-sonic cleaning in Isopropyl Alcohol.

The masks were cleaned by letting them soak in a solution of Cutscum detergent for a week with periodic rinses and cleaning in the ultrasonic cleaner. Due to the fragile nature of the masks nothing further was done to them. Cleaning in the ultrasonic cleaner never exceeded three minutes at a time for the same reason. After drying they were placed in the

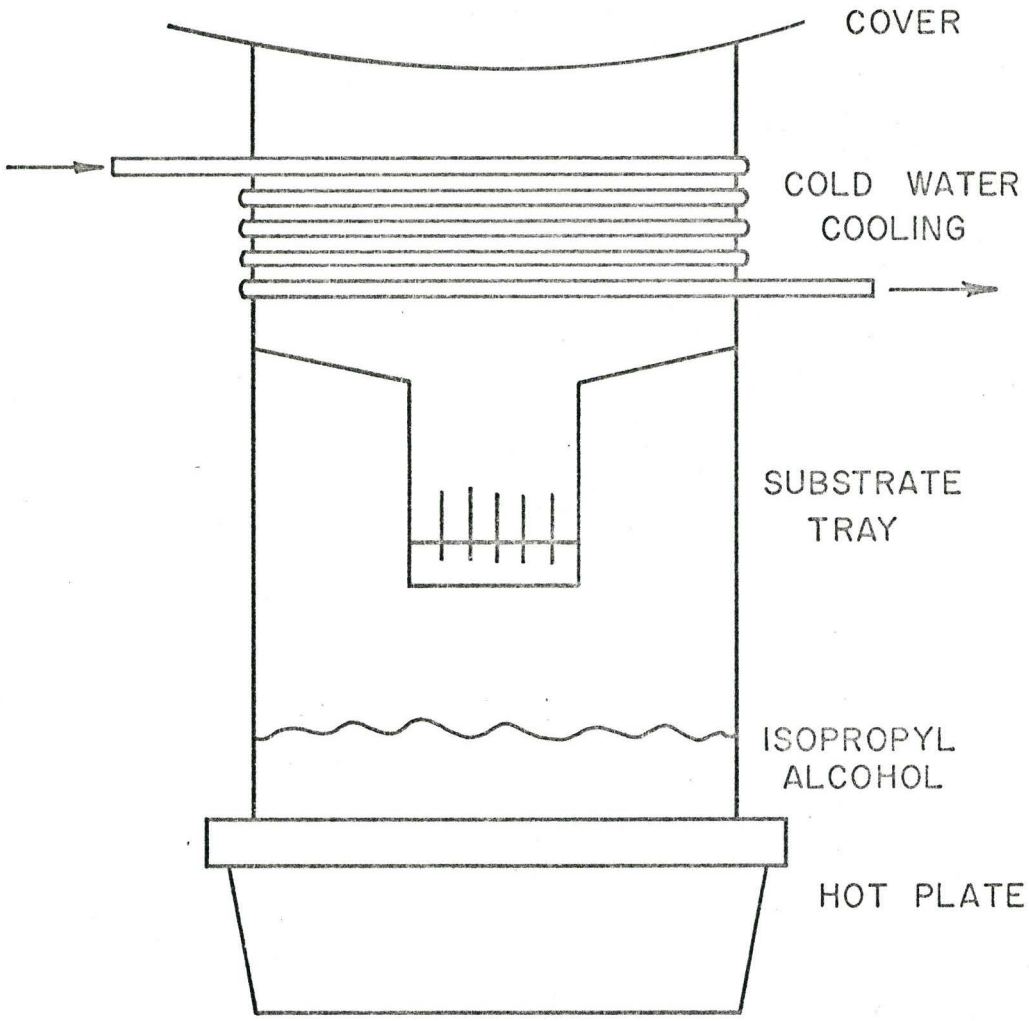


FIG. 3-2 VAPOR DEGREASER.

mask magazine. Again, the handling of such masks is carried out with gloves and tweezers.

After many evaporations the bell jar and vacuum system have a tendency to become contaminated. Those components of the system that can be removed are scrubbed with steel wool and Sparkleen followed by a distilled water rinse and drying with Acetone. This procedure is not carried out often because of the possibility of damage to the system. Prior to every evaporation however, the inside of the system is cleaned with a vacuum cleaner. Plates, shutters, and covers are scrubbed with Sparkleen.

When evaporating some materials, residues can sometimes be concentrated in the source. For example, Zinc Sulphide is left when Cadmium Sulphide is evaporated. Since these residues may be harmful to device performance the sources must periodically be cleaned. The alumina crucible and tungsten filament used as a source for Cadmium Sulphide were cleaned under a fume hood in Aqua Regia, rinsed in distilled water and dryed with Acetone.

The headers, on which the devices are mounted, were also cleaned. To this end a reflux was used as shown in Figure 3-3.

The solvent used was Dupont Freon TF. The headers

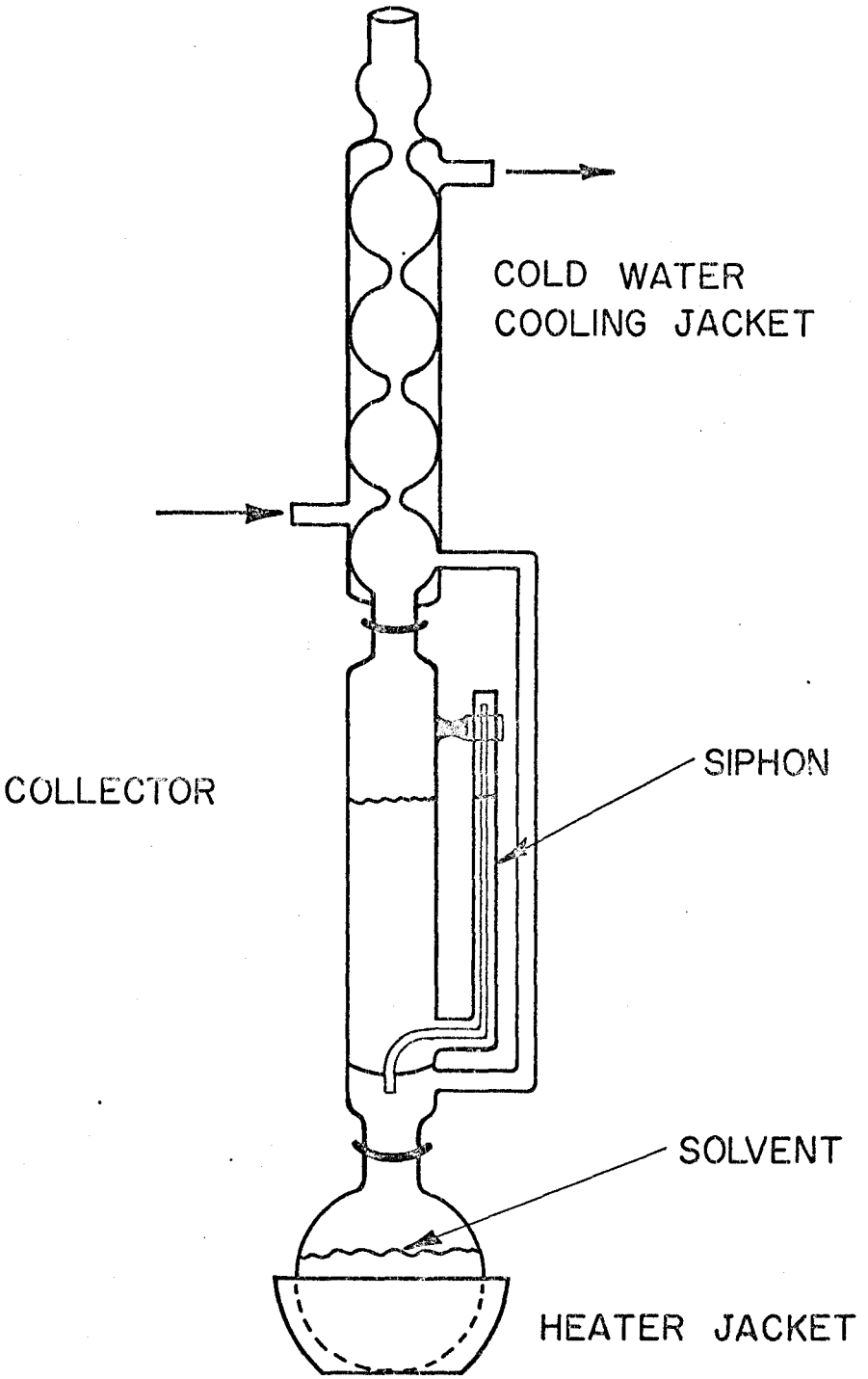


FIG. 3-3 REFLUX.

were cleaned in the reflux for one hour. The devices were similarily cleaned prior to bonding and packaging.

(c) Bonding and Packaging

After appropriate preparation, the devices were bonded in an Axion Model WU 600 Ultra-sonic wire bonder. One mil, 1% Silicon, Aluminum wire was used.

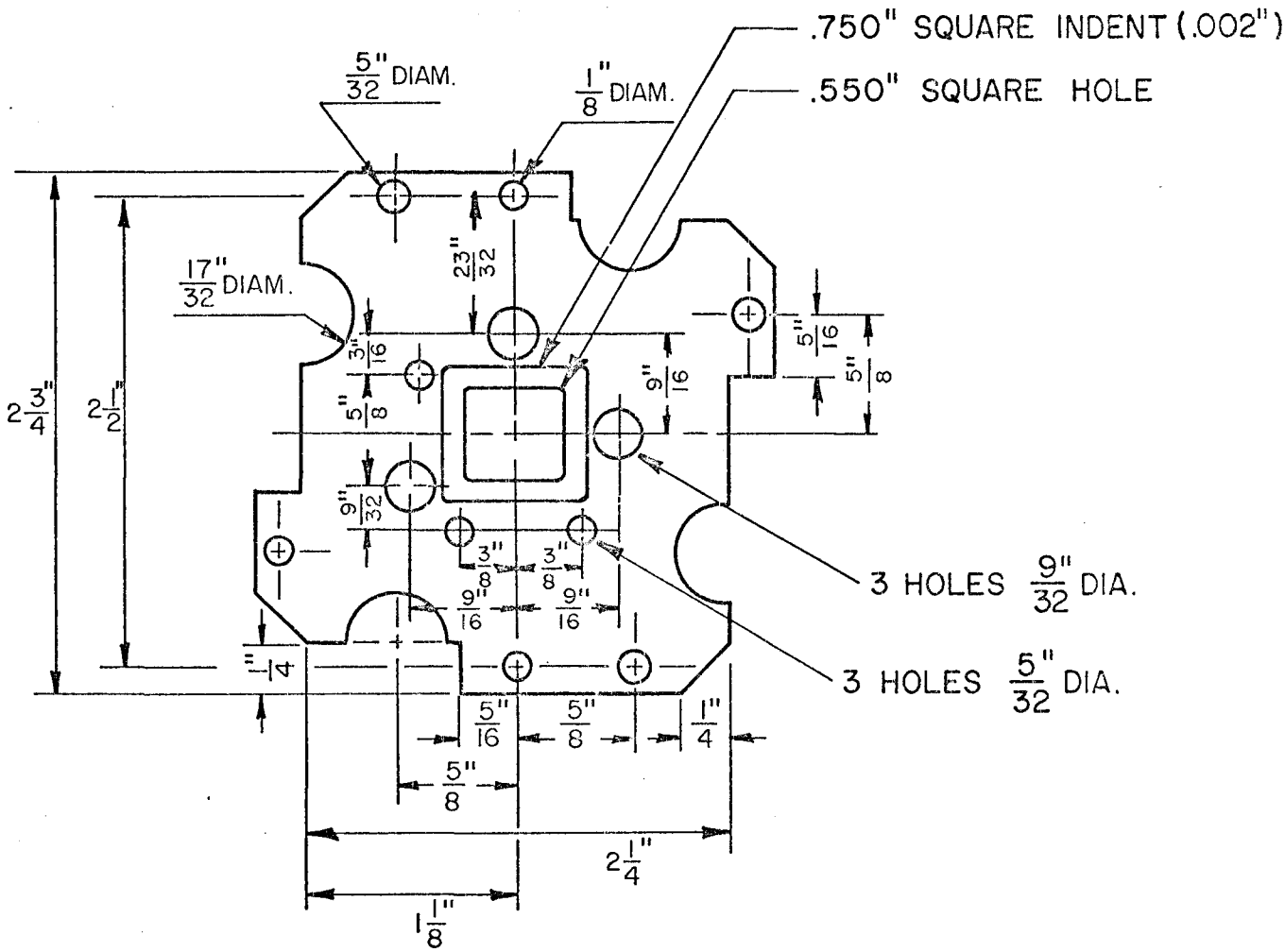
After bonding and heat treatment, the devices were sealed from the atmosphere with a small press specially constructed to accept TO-5 headers and caps. The press was kept in an isolation box which was pressurized to .5 lb/sq.inch with dry Nitrogen filtered with anhydrous Calcium Sulphate.

A good seal was obtained between cap and header using Eastman 910 Adhesive, provided the cap was snug to begin with.

Tests with a Veeco Model MS-9 Leak Detector and a Helium atmosphere showed no appreciable leaks from headers prepared in this way.

3.4 MASK PREPARATION[13]

A standard mask blank was prepared as shown in Figure 3-4. The blank served as a carrier for the thin copper-nickel mask which was mounted in the centre hole.



"300" SERIES STAINLESS STEEL .

FIG. 3-4 MASK BLANK .

To provide stiffness, 1/16" thick 300 series flat stainless steel was used for the blank. This series of steel has the same linear coefficient of expansion as copper, .0008 inches/inch/F°, which prevents buckling of the mask during an evaporation. The copper itself was .003 inches thick.

In preparation for spot welding to the mask blank, the foil was first degreased in Trichlorethylene. It was then scrubbed thoroughly with Tripoli Powder, an abrasive which removes surface irregularities. This was followed by a tap water rinse, drying, and cutting to size. Mounting in the mask blank was carried out with a Hughes Aircraft precision spot welder.

At the completion of this phase of the mask preparation, the artwork was begun. Drawings were made, showing the shape and dimensions of the required mask in terms of the co-ordinate system of the co-ordinatograph which was then used to cut plastic master diagrams. For the devices described, a Corado Co-ordinatograph Model KDF358 was used. The drawing scale gave a diagram twenty times the actual size of the mask required.

The plastic is a two layer plastic with each layer being a different color. The first layer is cut in the outline of the required mask pattern and peeled off leaving

a high contrast image.

Masters prepared in this way were illuminated with a colored light complimentary to the color of the first layer. A Yale precision step and repeat camera was then used to take pictures of the masters. The camera is equipped with vernier dials and can be stepped many times to repeat the pattern being photographed. Thus, one picture was drawn and repeated to produce the pattern described earlier. In this process pictures of two position marks were also made. These were then used in all subsequent positioning of the mask patterns.

The photographs were taken on Kodak High Resolution, High Contrast photographic plates. The nature of the final image required handling of the plates in a dust free atmosphere. Following exposure, they were developed and fixed with Kodak HRP Developer and Kodak Rapid Fix. Contact prints however are more suitable and therefore these were made from the photographic plates. Kodak Estar Thick Safety Base film was used and it was developed in the same manner as the plates.

The contact prints were inserted into a special punch, equipped with two microscopes so that the position marks, mentioned earlier, were clearly visible in the eyepieces. These position marks were lined up with cross-hairs observed in the eyepieces. Two position holes were then punched into

the prints. The holes served as guides in subsequent positioning because they match up with position holes in the mask blanks.

Prior to transferring the pattern to the copper foil, the work area on the mask blank was outlined by coating the front and back with a solution of Apiezon Wax dissolved in Carbon Tetrachloride. After hardening the wax, the blank was soaked in a solution of Hydrochloric acid followed by a good rinse in deionized water. Following attachment to a heavy copper electrode smut removal was carried out in an Aquatone S-R bath. Electric current was passed through the cell for a short time leaving the surface of the copper very clean.

Following this preparation the blank was attached to a spinner and a precisely measured amount of photoresist was dripped on to the copper. Spinning and baking followed producing a photosensitive layer on the copper.

The sensitized blank was then placed on a special jig having two position pins corresponding to the position holes in the blank.

Similarly, the contact prints were brought into close contact with the surface of the mask blank allowing exposure of the photoresist. Developing and fixing followed with Kodak Photoresist Developer and Photoresist Rinse. Removal of excess chemicals was again carried out in an Aquatone S-R

bath.

The Electroform Barrett Nickle Sulfamate[14] process was used to nickel plate the exposed area of the mask blank leaving the desired pattern on the copper foil. Excess chemicals were removed with a rinse in deionized water while the remaining photoresist was removed by scrubbing with a "Q-tip" dipped in Xylene. This left exposed copper which was then etched electrochemically in a solution of Ammonium Persulphate with appropriate catalysts. The fact that the copper comes out unevenly etched is of no consequence, since the actual mask is formed by the nickel plating which is well defined and unaffected by the echant. This is illustrated in Figure 3-5.

The masks were once again cleaned and the reverse side was nickel plated for mechanical strength. All further cleaning is discussed in Section 3.2, part (d).

In use, the masks are aligned in the mask holder of the microcircuit jig by two 1/8 inch diameter dowels and held in place by machine screws in each corner.

3.5 FILM DEPOSITION

(a) Silicon Monoxide*

* Please refer to page 61 Chapter 5, Results, for a discussion of the insulator.

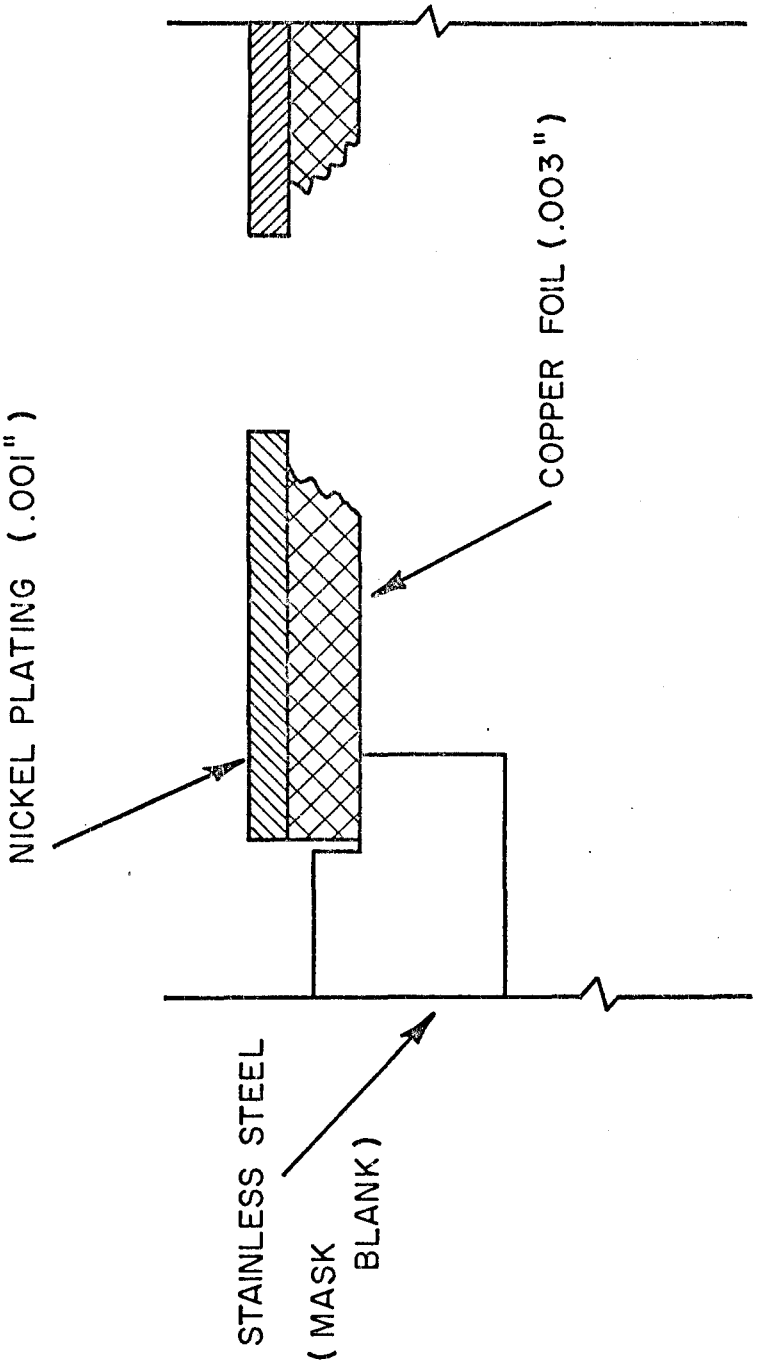


FIG. 3-5 MASK PROFILE.

This material was used as an insulator and for passivation. For film thicknesses up to 2000 Å an evaporation rate of 3 Å/second was used. Thicknesses greater than 2000 Å were evaporated at 3 Å/second which was increased to 5 Å/second after approximately 2000 Å had been deposited.

This material was found to evaporate well from a Molybdenum baffled boat.

A substrate temperature of about 20° C. produced a clear uncolored film which was stable in vacuum but ruptured in air. Therefore the substrate temperature during depositions of Silicon Monoxide was held at an indicated temperature of 250° C. Films deposited in this way were stable in air and had a brown tint indicating Silicon Monoxide. Further all depositions of Silicon Monoxide were carried out in Oxygen at a pressure of 10^{-4} torr.

During the deposition of the gate insulator the evaporation was carried out in four steps; that is the insulator was deposited in four layers. Miksic[15] et al have reported an increase in the breakdown strength of Silicon Monoxide deposited in this way.

(b) Cadmium Sulphide was used as a semiconductor. The material was evaporated from an Alumina Crucible indirectly heated by a Tungsten filament. Best results were obtained

when the substrate temperature was held at an indicated temperature of 200° C. and the evaporation rate held at 8 Å/second.

It is important that this material is well outgassed especially since it comes in powder form. Therefore prior to evaporation the crucible was heated just below the evaporation point for at least forty-five minutes.

Although Cadmium Sulphide dissociates on heating, no attempt was made at controlling the stoichiometry of the deposited film. Films thus produced are believed to be rich in Cadmium, although they have the characteristic yellow orange color of Cadmium Sulphide.

(c) Gold

Gold was used for pads, gates, and field plates due to its relative ease of evaporation. It evaporated well from Molybdenum boats although it has a tendency to attack them. A rate of 10 Å/second produced good results. Substrate temperature was not an important deposition parameter.

(d) Aluminum

For source-drain gaps or direct contacts to the Semiconductor (Cadmium Sulphide) this material gave a good

ohmic contact*. For this reason it was preferred in this application. Good results were obtained with an evaporation rate of 10 Å/second from a tungsten basket. As with the Gold, substrate temperature was not an important deposition parameter.

3.6 DEVICE PREPARATION

Prior to pump down, the substrates, masks, and materials were prepared and placed in the vacuum system. It was then left to pump overnight. During this period cold water was run through the cold trap. During evaporations liquid nitrogen was used.

The substrate temperature was raised to an indicated temperature of 250° C. All evaporations were done at this temperature except for the Cadmium Sulphide which was evaporated at 200° C. A layer of Silicon Monoxide 1000 Å thick was deposited first at a rate of 1Å/sec. In the second step the semiconductor was evaporated at 8Å/sec. to a thickness of 500 Å.

Contact pads were evaporated next. One hundred angstroms of Nichrome were deposited first and the remainder of the deposition was completed with Gold. The thickness

* Please refer to page 66, Chapter 5, Results, for a discussion of this point.

and rate were 10,000 Å and 10 Å/sec. respectively. A conducting path is provided to the contact pads from the semiconductor by the source drain contacts. These consist of Aluminum deposited at 10 Å/sec. to a thickness of 250 Å. Before the gate insulator was deposited a layer of Silicon Monoxide was put on top of the source drain contacts*. The layer was 2500 Å thick, deposited at 3 Å/sec. Since the gate necessarily overlaps the source drain gap due to the positioning error this added layer increases the separation between the two electrodes in the area of the overlap effectively reducing interelectrode capacitance. After this step the gate insulator is deposited. Silicon Monoxide in four steps of 60 Å each forms the gate insulator. There is a pause of five minutes between each step. The layering of the gate insulator helps to increase its breakdown strength. The gate, consisting of gold, was deposited next. The thickness and rate were 500 Å and 10 Å/ sec. Finally the device was encapsulated in a Silicon Monoxide layer 10,000 Å thick deposited at 3 Å/sec. It was observed that this layer would fracture or bubble when exposed to air if the substrate was not heated during the evaporation.

The completed devices were removed from the bell jar

* Please refer to page 68, Chapter 5, Results, for a clarification of this point.

and scribed on a Tempress Model 1713-102 automatic scriber. They were broken and mounted onto TO-5 headers. Forma-Seal #A146 High Temperature Adhesive was used to cement the chips to the headers. Alternately Lepage's Epoxy was also used. When Forma-Seal was used it was necessary to heat the devices for one hour at 100° C. and then two hours at 200° C. to allow the cement to cure. A Delta-Design Model MK 2300 oven was used. The devices were bonded and tested. They were then heated in air for approximately 192 hours at 130°C. The headers were capped using a small press which forced the caps onto the header. Sealing at the joint was provided by Eastman 910 adhesive.

CHAPTER IV

OTHER ASPECTS OF TFT TECHNOLOGY

4.1 INTRODUCTION

Although the theory of the Field Effect Transistor is fairly well understood the physical processes in TFT's and their relationship to evaporation techniques are not.

In this chapter the influence of materials and techniques on device performance are discussed, as are possible links to instabilities in MOS devices.

4.2 The Influence of Materials and Techniques on Transistor Operation.

(a) Surface States and the Control of Surface Potential

In the previous section, one of the assumptions made was concerned with the absence of surface states. In practice, however, these are always present. The bulk of a crystal sufficiently removed from the surface, so as not to be affected by it, may be looked upon as an infinite, uniform periodic structure. At the surface on the other hand, the forces acting on the atoms are no longer symmetrical. Even

if the bulk is perfect, the surface atoms are usually displaced from their ideal lattice positions. Further the fact that the surface constitutes an abrupt termination of the crystal lattice results in a deformation of the crystal potential. These things have far reaching consequences on the electronic processes in the underlying region of the material close to the surface. At the same time the unsaturated bonds of the surface atoms make them highly reactive to any foreign atoms.

These phenomena give rise to surface states. They may be associated with the unfilled orbitals or dangling bonds of the surface atoms each of which may be free to trap an electron or electrons. The states may be divided into two categories, "fast" and "slow". The fast states are normally characterized by time constants of the order of microseconds or less; the slow states by time constants ranging from a fraction of a second to hours, depending on the structure of the oxide layer and gas ambient. Typically, these states may be present with a density of 10^{11}-10^{13} cm^{-2}.

The slow states are located predominantly in the bulk of the oxide while the fast states are presumably situated at the semiconductor oxide interface[16].

It is important to realize that the states may be present in sufficiently large numbers to control the potential at the surface.

Weimer[17] has observed that depletion or enhancement surface layers may be produced on CdS films by suitable choice of the insulating layer and deposition conditions.

Haering[7] has suggested that the bending of the surface potential at the semiconductor interfaces accounts for the observed slope in the saturation region of CdS TFT's. Haering[18] further indicates that the surface potential may be controlled continuously by the evaporation of two different insulators; one providing enhancement type behavior, the other depletion type. Typically these might be Si_yO_x and CaF_2 evaporated in various thicknesses so that one reduces the effect of the other. By suitable choice of thickness any surface potential between the limiting potentials of pure Si_yO_x and CaF_2 is possible. O'Hanlon[8] has verified this behavior experimentally producing CdS TFT's with good saturation characteristics.

(b) SiO_2 Passivation

Another effect that has been noted is the stabilization of SiO_2 passivation layers with P_2O_5. Kerr[19] et al have reported the failure of Bipolar transistors in the absence of P_2O_5 treatment of SiO_2. They suggest that degradation occurs in unstabilized SiO_2 as a result of an accumulation of positive space charge in the Silicon Dioxide. This effect is evident in MOS devices and is discussed in the following section.

This work is significant for TFT's since Si_yO_x is used as a gate insulator as well as for passivation.

Schelhorn[20] indicates that for TFT's it may be sufficient to evaporate a thick Si_yO_x insulating layer for passivation of the devices. This is a more attractive alternative since there is some difficulty in treating TFT's with P_2O_5.

(c) The Influence of Substrate Temperature on the TFT.

The semiconductor properties may also be controlled somewhat. Dresner[21] has shown that the mobility of CdS films increases with increasing substrate temperatures. Mobility has a pronounced effect on the transconductance of a TFT. The transconductance may be obtained from equation 2:44.

$$I_d \text{ (max)} = \frac{\mu C_g}{2L^2} (V_g - V_0)^2 \qquad \ldots(4:1)$$

$$g_m = \left.\frac{\partial I_D \text{ (max)}}{\partial V_g}\right|_{V_d \text{ constant}} \qquad \ldots(4:2)$$

$$g_m = \frac{\mu C_g (V_g - V_0)}{L^2} \qquad \ldots(4:3)$$

Therefore by controlling the substrate temperature during evaporations of CdS TFT's some degree of control over the g_m may be exercised.

(d) Figure of Merit

A useful figure of merit for three terminal devices is the gain-bandwidth product. For the TFT it can be shown that the gain-bandwidth product is

$$GB = \frac{g_m}{2\pi C_I} \qquad \ldots(4:4)$$

where C_I is the input capacitance.

It can be seen that any improvement in g_m will improve the figure of merit for the device. If at the same time C_I can be minimized a further improvement will be realized. This can be done if the interelectrode capacitance is reduced. It arises primarily from the overlap of the gate electrode with the Source and Drain electrodes. Positioning of masks involves some error which means that the gate electrode must necessarily overlap the Source-Drain gap.

However, if the separation between the gate and source-drain electrodes, can be increased in the area of overlap this will serve to reduce the interelectrode capacitance. This can be done if contact pads are first deposited. The source drain electrodes are evaporated, electrically connecting the pads to the semiconductor. The pads however, are not totally covered by the Source-Drain contacts. This mask is not moved and subsequently a heavy layer of insulator is deposited on top of them. The gate insulator can then be deposited through

the following mask followed by the gate. Electrical contact can still be made through the uncovered portion of the pads while the interelectrode capacitance is reduced substantially. Similarly, if positioning is improved so as to reduce the required overlap the interelectrode capacitance will again be reduced.

4.3 Instabilities in MOS Devices; Their Relationship to TFT Performance.

Hofstein[22] has proposed that because of its asymmetrical behavior, instability in MOS devices originates at the metal-oxide interface. In the oxides investigated, it was found that the time required for charge relaxation upon removal of bias could be many orders of magnitude shorter than the time required for the generation of the injected charge.

Measurements were carried out using a sampling technique for monitoring surface conductivity. The block diagram of the circuit is shown in Figure 4-1.

A gate voltage is applied to the transistor for a short period of time. Then it is removed and a feedback voltage is applied momentarily so as to maintain a fixed Source-Drain current.

The feedback voltage is monitored for as many cycles as necessary and a recording of it versus time gives a good

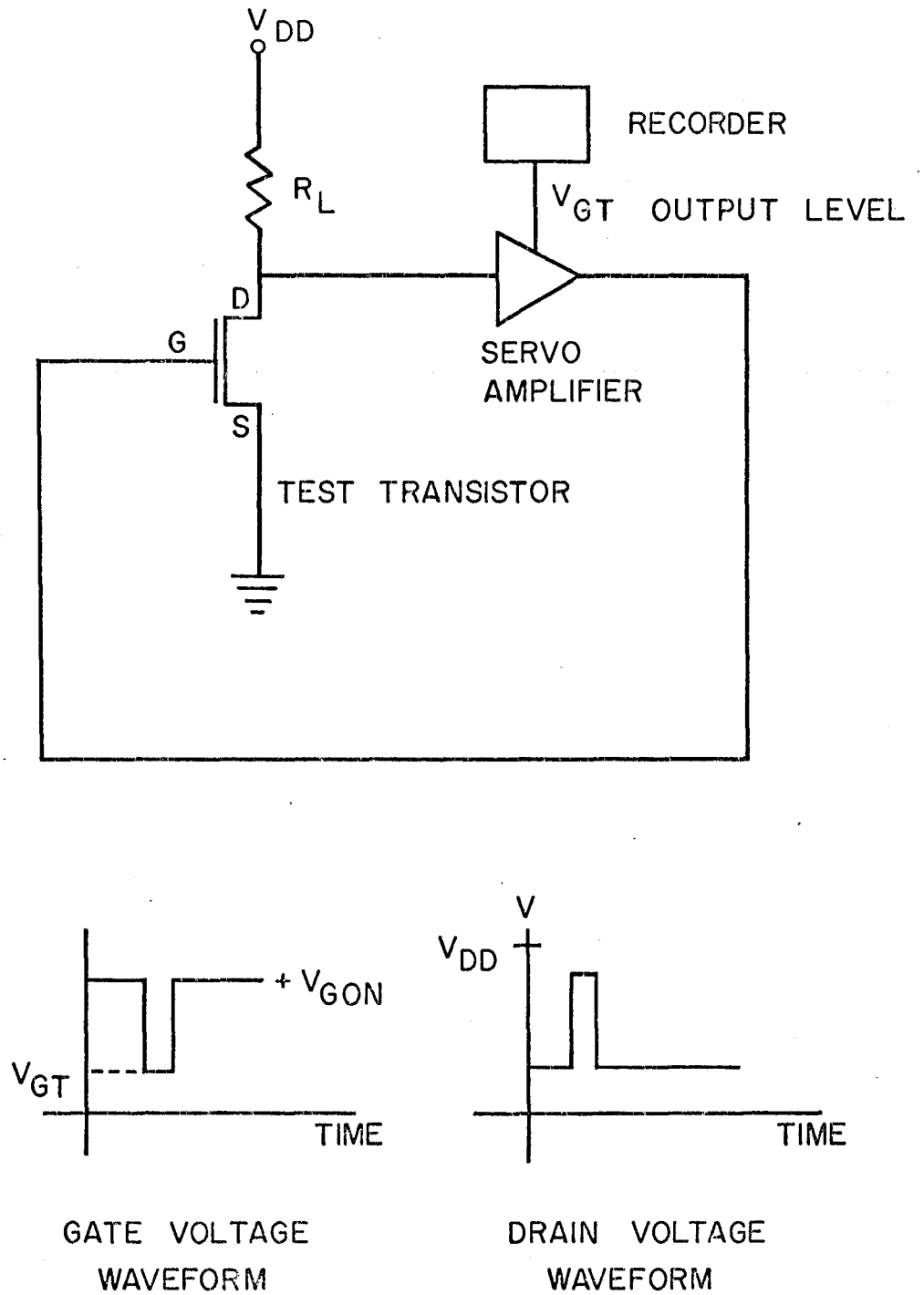


FIG. 4-1 SURFACE CONDUCTIVITY MEASUREMENT.

indication of the ion drift in the gate oxide.

Exposure of the oxide to hot distilled water and to hot saturated Sodium Chloride can decrease the forward drift time constant by as much as four orders of magnitude compared to the control wafer. Similarily the activation energy can decrease as much as one-third. Oxides etched with $HF-H_2O$, on the other hand, show an improvement in stability over the control wafer. The instability can be brought back with a concentrated Sodium Chloride rinse. It would appear that the action of the rinses is dependent on a catalytic agent which is apparently removed with etching.

If after stressing of the oxide a small negative gate voltage is applied the recovery time constant is found to be substantially smaller than the initial drift time constant, even if the reverse voltage is much smaller than the activation voltage.

An interesting effect has been observed in the recovery. If immediately following recovery the positive gate voltage is reapplied the time constant is very short and the feedback voltage returns to its pre-recovery value very quickly.

The oxide obviously has not been restored to its original value. If the gate is maintained at a negative bias condition for several initial drift time constants and then if a positive gate bias is reapplied, the redrift

is identical to the initial drift. The observed behavior is consistent with a trapping or dissociation phenomenon taking place in the oxide at the metal-oxide interface region. Further at room temperature the type of gate metal seems to have little or no effect consistent with this model.

The fact that only one polarity of gate voltage causes drift and C vs. V measurements, indicate that the source of instability is a fixed quantity of positive charge which moves through the oxide from the oxide-metal interface region. The possibility of injection from the gate electrode is ruled out because current flow into the gate reduces to zero after the initial application of gate voltage. The recovery is due to the transport of positive charge back to the oxide-metal interface region. The asymmetrical behavior is attributed to deep trapping at the oxide-metal interface and the lack of trapping at the semiconductor-oxide interface. Measurements on "contaminated units" indicate a trapping level of 1.1 eV. and half widths of the order of 7.5 $\mathring{A}$ of 8.0 $\mathring{A}$.

Calculated trapping time constants (10^{-2} seconds) and observed true recovery time (10^{+2} seconds) suggest that each ion-trap pair slowly changes its internal structure so that the binding energy for the ion increases from some initially small value to a final value equal to the original initial

drift activation energy. The ion responsible has been tentatively identified as hydrogen released from adsorbed water that is hydrolyzed at the metal-oxide interface. Sodium also has been identified as causing instability.

Hofstein[23] in subsequent investigations has found that cleanliness and annealing techniques have helped to reduce Sodium and hydrogen ion contamination reducing the induced positive charge in the oxide and thereby improving the overall stability.

Preliminary investigations by Schelhorn[24] on CdS TFT's indicate a similar type of behavior. A comparison of the results is useful. In both cases the observed instabilities in the SiO_2 gate insulator fall into four groups, two of which appear to be technique dependent. Annealing in either case significantly improves device stability. Although Schelhorn[24] has not identified the drift mechanism he does suggest that oxygen enriched films are more unstable than normally deposited insulator films. There is not enough information to compare this aspect with Hofsteins investigation.

An investigation of technique by Schelhorn[20] indicates that a heavy encapsulation layer both above and below the device helps to reduce instability. Testing has shown that an evaporated SiO_2 encapsulation protects the device from the ambient as well as vacuum encapsulation.

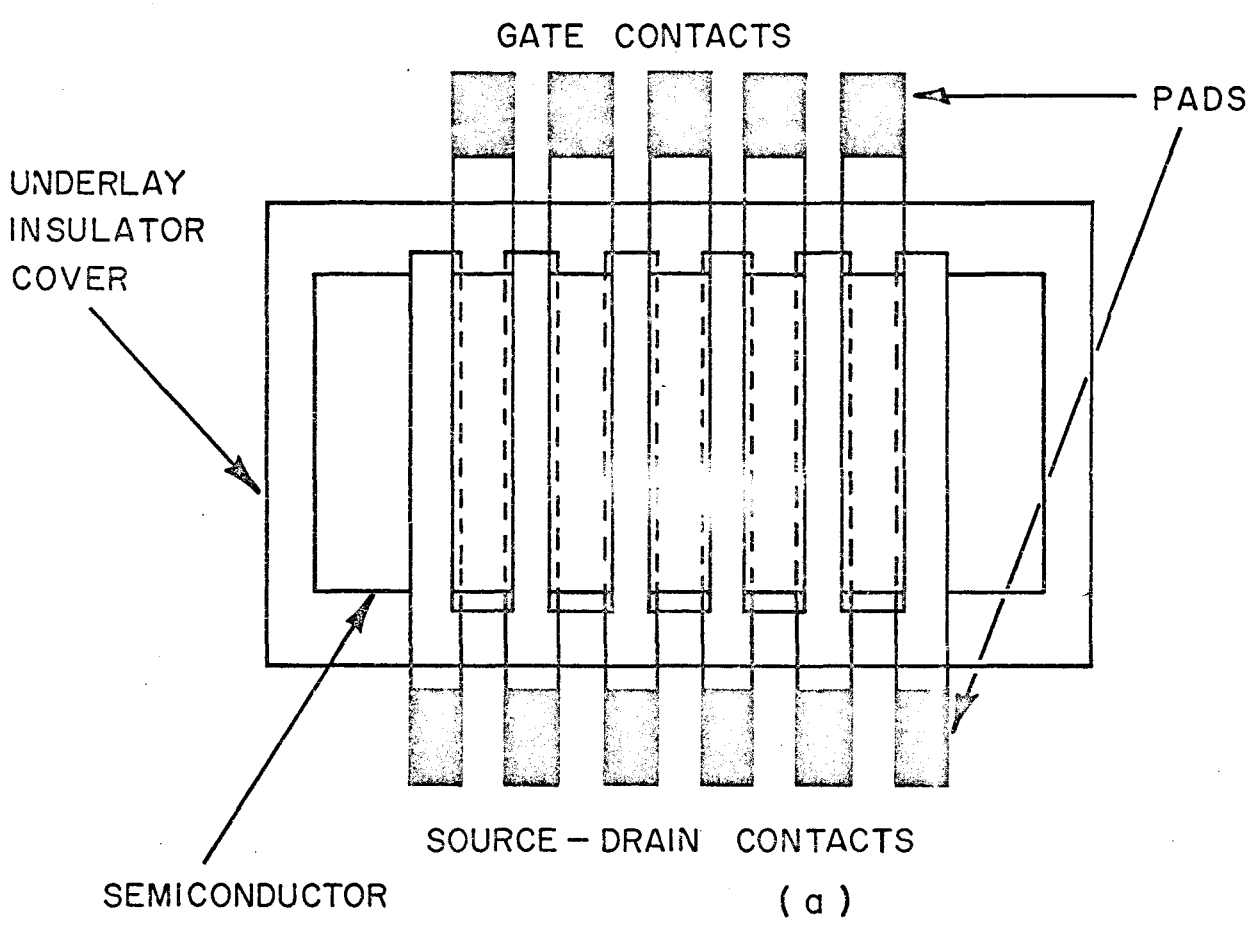
CHAPTER V

RESULTS

5.1 GENERAL

Transistors and four terminal devices were evaporated as outlined in Sections 3.5 and 3.6. About fifty evaporations were carried out, producing about 400 transistor samples. The structures that were used are illustrated in Figure 5-1.

One of the first problems encountered involved mechanical instability in the insulator. It was observed that a heavy insulator (greater than 3000 Å) was unstable in air if it was evaporated at a substrate temperature of 20° C. Although stable in vacuum the film, upon exposure to air, would shatter in a matter of seconds. This problem was overcome by evaporating the insulator at a substrate temperature of 250° C. It was further observed that the boat temperature influenced the stability of the film. A cool boat, judging by its color and light emission, produced a clear, but highly stressed insulator. It would appear that this insulator has a high concentration of SiO_2. This type of film is undesirable because it also shatters after a period of time.



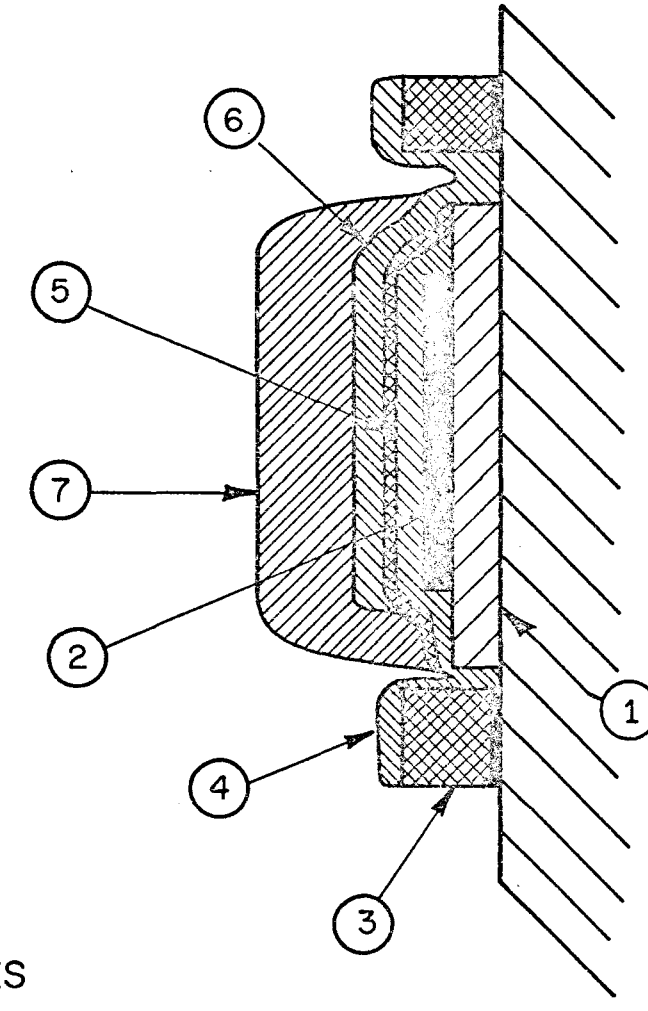
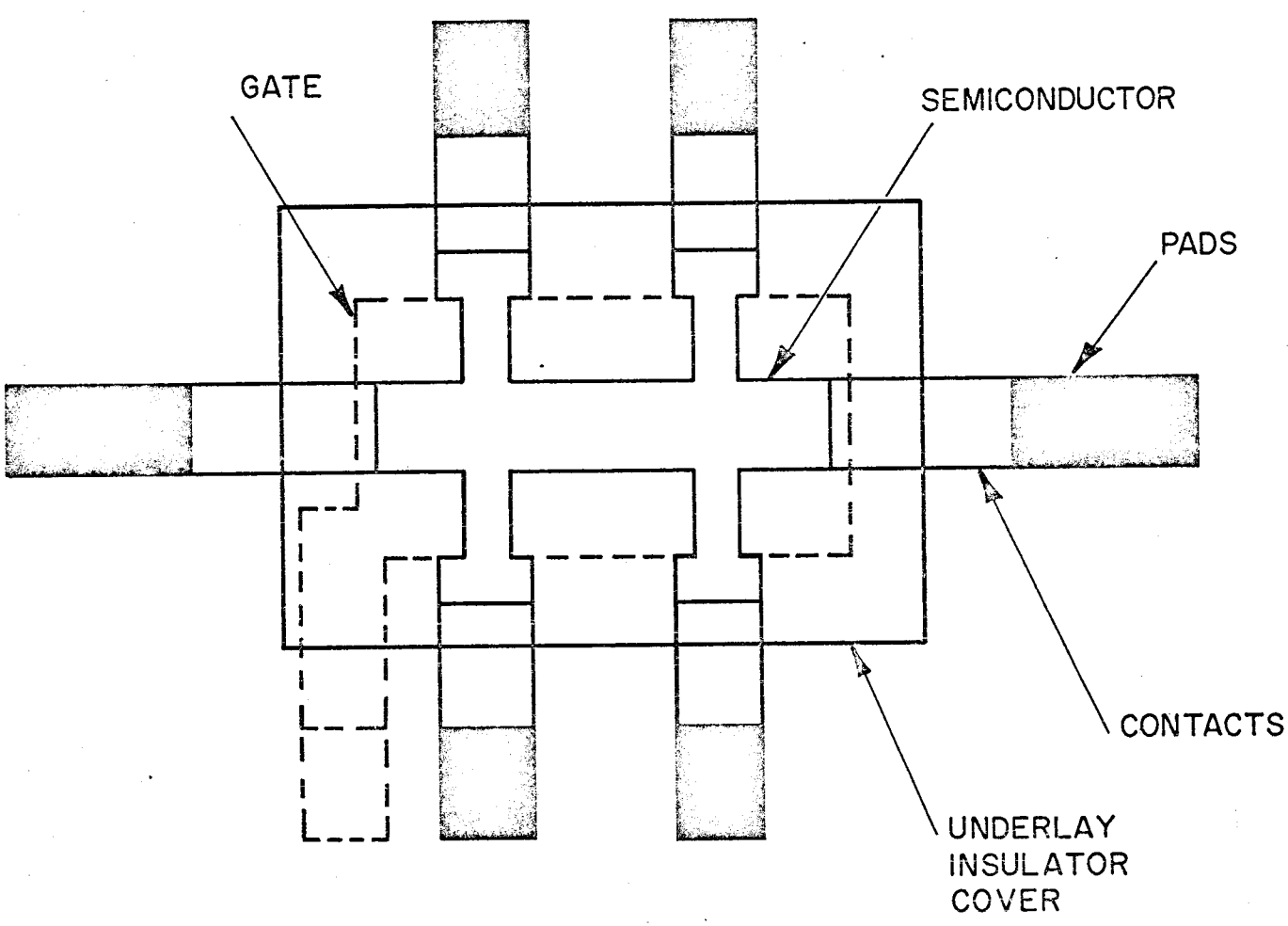
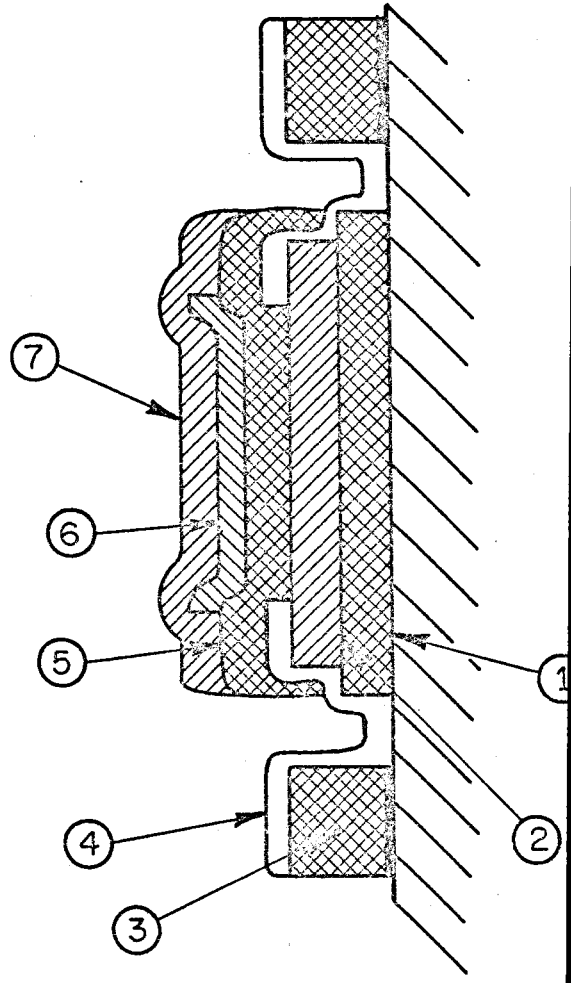


FIG. 5–1 THE EVAPORATED THIN FILM SAMPLES

(a) TRANSISTOR

(b) HALL SAMPLE





(b)

NOTES:

(1)	UNDERLAY	1000 A°	Si_xO_y
(2)	SEMICONDUCTOR	500 A°	Cd S
(3)	PADS	10,000 A°	Au (NUCLEATED WITH NiCr)
(4)	CONTACTS	500 A°	Aℓ
(5)	INSULATOR	250 A°	Si_xO_y IN FOUR STEPS
(6)	GATE	500 A°	Au
(7)	COVER	10,000 A°	Si_xO_y

Similarly, mechanical shocks destroy the film. This behavior was observed only in the transistor samples and therefore was attributed to the transistor's rough surface geometry which probably increased the stress in the insulator.

If the boat geometry is changed slightly, to give a hotter boat, the resultant film is brown in color indicating a high concentration of SiO. This film is stable in air, but appears to be electrically and mechanically "leaky". This last condition seems to be strongly dependent on the evaporation rate. The best films seemed to be evaporated at a rate of from 3 to 5 angstroms per second.

It was further observed that heat treatment reduced the incidence of shattering in the insulator. Those devices which were secured to a header with "Form-a-Seal" adhesive were heated for two hours at 100° C. and at 200° C. for one hour to set the cement. Subsequently, up to a period of two months, there was no mechanical failure of the cover in these devices. However, those devices which were secured with ordinary epoxy shattered within days after exposure to the ambient. This effect was more pronounced in periods of high humidity. Again, this effect was observed only in the transistor samples.

The factor which appears to have the most profound effect on the behavior of the insulator is the presence of

water vapor in the ambient. For example a drop of water placed directly on a transistor, with a hypodermic syringe, destroys the device. Again this effect is very strongly dependent on the evaporation conditions of the insulator.

The shattering of the heavy insulator has been verified by other workers.[25]

Another problem encountered in early evaporations was reproducibility. The problem was traced to heating of the crystal monitor. Prolonged exposure to the evaporation source caused the crystal frequency to drift so as to indicate a thicker film than was actually evaporated. The addition of water cooling to the crystal lessened this effect. A thermocouple placed in close proximity to the water cooled crystal, indicated a temperature of 70° C. This temperature should be sufficiently low to prevent further drifting. Further, device reproducibility across the substrate was good, possibly due to the thin substrates used, which allowed a more uniform heating of the substrate surface. The small active area of the substrate also probably helped improve this reproducibility.

The variation of carrier mobility with substrate temperature was also observed. Typically, devices evaporated at a substrate temperature of 200° C. had a transconductance nearly twice as large as those devices evaporated at 175° C. At a substrate temperature of 225° C. however, it appeared

that the CdS was no longer adhering to the substrate and all devices evaporated at this substrate temperature were open-circuited. An indicated substrate temperature of 200° C. seems to be optimum for the evaporation of the semiconductor.

Problems were also encountered with the bonding of the devices. Although satisfactory bonds could be made to thin contact pads it was observed that the thicker pads consistently gave better bonds. The minimum pad thickness to which satisfactory bonds could be made was 5000 Å. Ultra-sonic bonding proved to be the most suitable method in this case. Thermo-compression bonding was unsatisfactory because of the insulating substrate and poor heat transfer through the adhesive. In most cases the adhesive broke down before the sample temperature reached the point where good bonds could be made.

Nucleation with Nichrome improved the mechanical strength of the bonding pads. Without an underlayer of Nichrome the pads were scraped and lifted off the glass substrate by the scrubbing action of the bonding tip.

Other difficulties were encountered in the deposition of the devices. Of the 400 transistors deposited only about 24 worked. In the remainder of the devices, apart from the previous mentioned problems, the major cause of faulty transistors was non-ohmic contact. This effect could be

observed in the I-V characteristics of these devices. It was characterized by decreasing g_m with increasing gate voltage concluding in a "piling up" or overlap of successive traces. Further, from studies of devices that broke down, it was suspected that the blocking contact was at both the Source and Drain contacts. Other workers[8] have observed similar behavior in this type of structure.

Contact materials other than Aluminum were tried. For example, Cadmium was evaporated to a thickness of 500 Å. However the scattering of Cadmium into the Source-Drain gap even at this thickness was so bad as to be visible under the microscope. The Cadmium thickness was then decreased to 100 Å and the contacts were completed with a deposition of 400 Å of Gold. These composite contacts proved to be unsatisfactory also, because the Gold did not stick to the Cadmium. This is a rather surprising result since it was observed that the Cadmium sticks well to the Gold bonding pads.

After many careful evaporations however, it was observed that ohmic contacts could indeed be produced with Aluminum. This occured only when a fresh tungsten basket was used as a source for the Aluminum. Any attempt to use the same source for a second evaporation produced blocking contacts.

A possible explanation can be arrived at from an examination of the phase diagram for the Aluminum-Tungsten System. As the boat is heated up and the Aluminum melts some Tungsten dissolves in the Aluminum. One of the phases thus formed is WAl_{12}. There is some evidence for the formation of another phase by the reaction of Aluminum and WAl_{12} at temperatures below 580° C., but this reaction is not reversible[26]. Conceivably this phase is formed as the Aluminum source is cooled. Then in subsequent evaporations this phase is evaporated along with the Aluminum, forming a blocking contact, assuming that this phase is a poor conductor.

In the early devices produced a layer of insulator was deposited over the Source-Drain contacts; however, because of the difficulties encountered, this step was omitted in subsequent evaporations. This action was taken to reduce some of the problems involved in the device fabrication. Therefore no evaluation of its effect on device performance was made.

An attempt was made at evaluating the transconductance of the working devices (without insulator over the Source-Drain contacts) against frequency and operating point. No real information could be obtained though, because of noise problems (due to the low g_m) and the shattering of the cover after exposure to air. In one measurement though it was

observed that the g_m did not change appreciably between 100 Hz and 50 KHz which is a considerable improvement over devices produced previously in this laboratory. This improved frequency performance may be attributed to the decrease in overlap of the Gate and Source-Drain contacts. It may also be noted that the Hysteresis effect was evident in the g_m measurement.

The breakdown strength of the devices showed a considerable improvement over previous samples. The transistors could be operated in the enhancement mode with a Source-Drain voltage of 15-20 volts and a similar gate voltage before breakdown occurred. Previously these transistors were operated at Drain voltages of about 10 volts and gate voltages of 5 volts. A possible explanation is that the insulator was better in this case.

With respect to breakdown, peculiar behavior was observed with some devices. At a Drain voltage slightly below total breakdown, transistor action became poor.

This behavior is illustrated in Figures 5-2 and 5-3. In Figure 5-2 the I-V characteristics of the TFT are shown. This device was evaporated with a substrate temperature of 200° C. for the semiconductor. The device was stressed to a Drain voltage of 16 volts and the result is shown in Figure 5-3. This effect seemed to be self-healing in that the device would

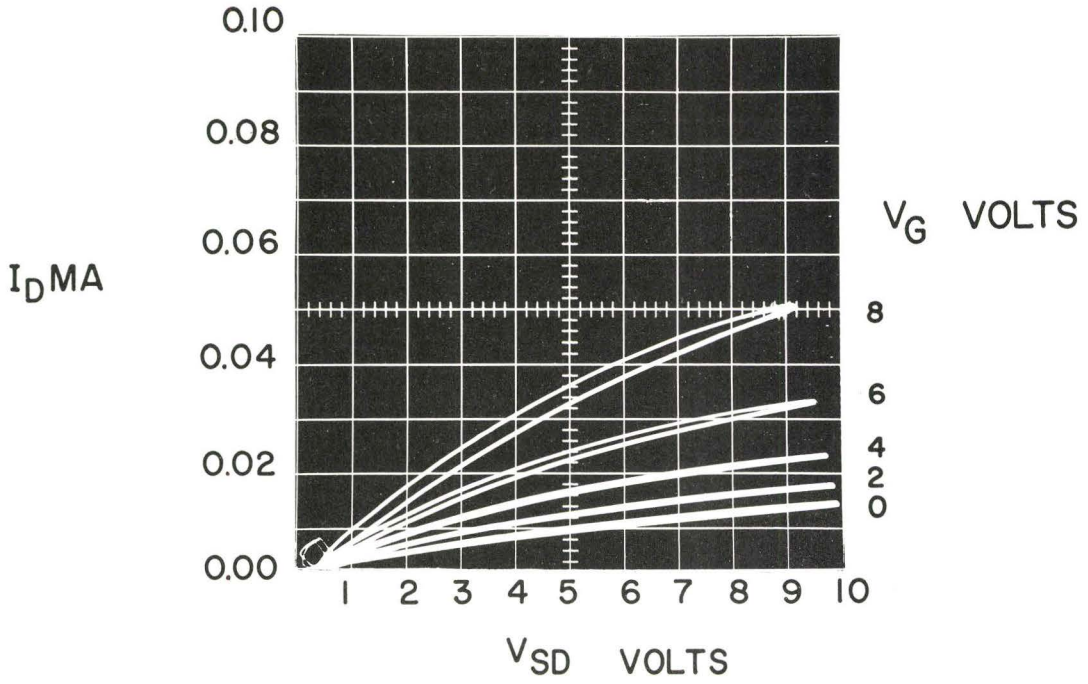


FIG. 5-2 TRANSISTOR SAMPLE # 28
SUBS. T. 200°C. NO HEAT TREATMENT

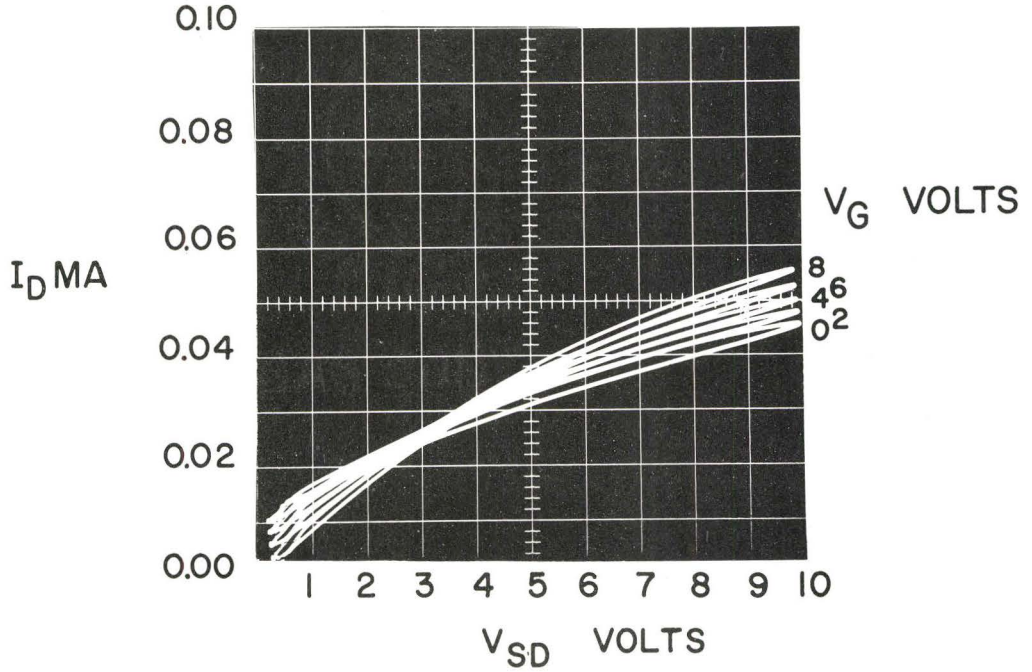


FIG. 5-3 TRANSISTOR SAMPLE # 28
PARTIAL BREAKDOWN

return to normal after about two days. However, since only two devices were tested this way, no conclusion can be reached as to the mechanism or peculiarity to these particular samples.

No conclusive evaluation was carried out of the packaging system. This was primarily due to the difficulty in getting useable quantities of test samples. There is, however, evidence that this system may be unsatisfactory. In an experiment involving samples of a resistor network in a flat pack it was found that after sealing, the resistors had changed value drastically. It is believed that the change resulted from a reaction between the resistor material and fumes from the sealant (Eastman 910 Adhesive) which is a Cynide based system. Extrapolating this behavior to the transistor samples one would expect the results to be unfavorable.

One final general comment could be made about the use of Liquid Nitrogen cold trapping. It did not appear to make any difference as to the quality of the evaporated sample. In fact the last half of all the evaporations carried out were done without Liquid Nitrogen cold trapping. When the cold trapping was discontinued the diffusion pump oil was changed from Dow Corning 704 silicone oil to 705 silicone oil which is a higher quality oil. Any disadvantage from discontinuing cold trapping should be more than offset by the use of this higher

quality oil. Nevertheless cold water was run through the cold trap during evaporations as recommended in the Edwards High Vacuum Manual.

5.2 THIN FILM TRANSISTORS; POST DEPOSITION

Figure 5-4 shows transistor sample #10. This is a device prepared as described previously. The substrate temperature was 175° C. during the semiconductor evaporation. As noted earlier on, the transconductance is lower at this substrate temperature than at 200° C. The curves were measured on a Tektronix Model 575 Curve Tracer.

The transconductance as taken from the photograph is 3.4 μmhos. The output resistance (the slope of the saturated region) is .71 megohms. The voltage amplification factor is then 2.4. The zero gate voltage current is 0.03 ma. Note the presence of the hysteresis effect in the characteristics.

It is suspected that the hysteresis is at least partially caused by the measuring instrument. There is also evidence to indicate that the size of the loop is frequency dependent.

The most significant feature of this device is its stability with time and applied voltage. In the time prior to heat treatment, a period of three days, its characteristics were viewed for periods up to forty-five minutes without any

discernible change. Varying the applied voltage also failed to cause the device to drift.

This is a big improvement over previous devices produced in this laboratory.

5.3 THIN FILM TRANSISTORS; POST ANNEALING

In Figure 5-5 we observe the characteristics of transistor sample #10 after 168 hours of heat treatment (in air) at 130° C.

The first striking improvement over Figure 5-4 is the improved saturation characteristics of the device. Note also that the size of the hysteresis loop has decreased.

There is a considerable improvement in the transconductance as well. The value for g_m is now 6.0 μmhos. The output resistance is 2.5 megohms giving a voltage amplification ratio of 15. The size of the hysteresis loop has decreased. The device is still stable. Referring now to Figure 5-6 the device characteristics are observed after annealing for 193 hours at 130° C. Again considerable improvement has been made over the untreated device.

The transconductance is 6.6 μmhos. Output resistance is 2.5 megohms. The amplification factor is then 16.5 Zero gate voltage current is .01 ma, a reduction to one third of its original value. Stability has not changed.

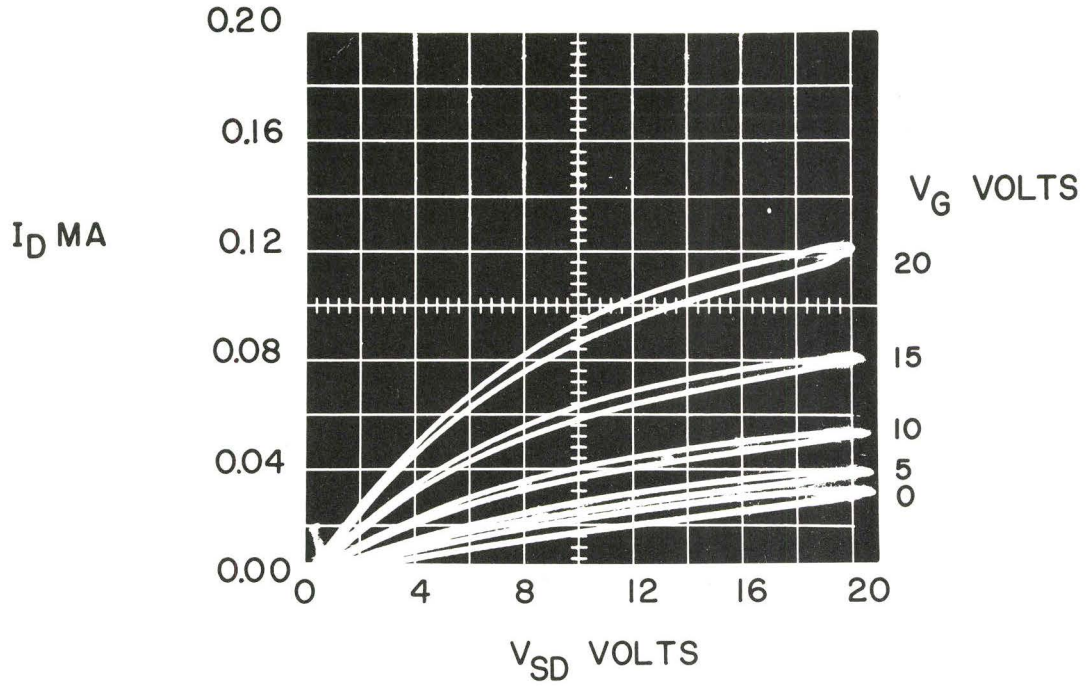


FIG. 5-4 TRANSISTOR SAMPLE # 10
SUBS. T 175°C NO HEAT TREATMENT

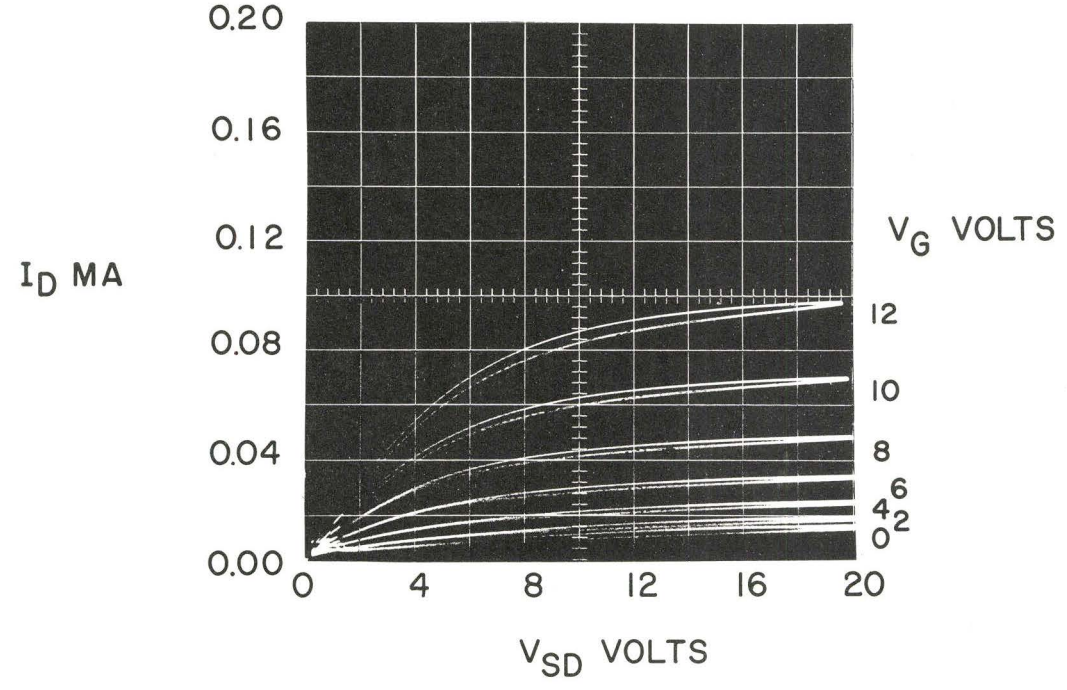


FIG. 5-5 TRANSISTOR SAMPLE # 10
ANNEALING 130°C FOR 168 HRS.

Figure 5-7 indicates a slight deterioration of the characteristics. In this figure the device has been annealed at 130° C. for 288 hours. It appears that the optimum time for annealing has been passed. Transconductance is down to 6.0 μmhos. The output resistance is down to 2.0 megohms. The amplification factor is correspondingly down. Its value now is 12. Zero gate voltage current is still .01 ma. and the device remains stable.

Briefly, the effects of annealing are: the lowering of the zero gate voltage current, an increase in g_m to a maximum value and then a slight decrease with continued annealing, a flattening of the characteristics corresponding to an increase in output resistance, a corresponding increase in amplification factor, and slight decrease in the size of the hysteresis loop.

This particular device was removed from the oven after 288 hours and was left in air. The device remained stable for about three weeks. No observable change occurred in its characteristics during that time. However, the device was re-examined in the fifth week and was found to have failed. The cover was intact so that it is difficult to say why failure occurred.

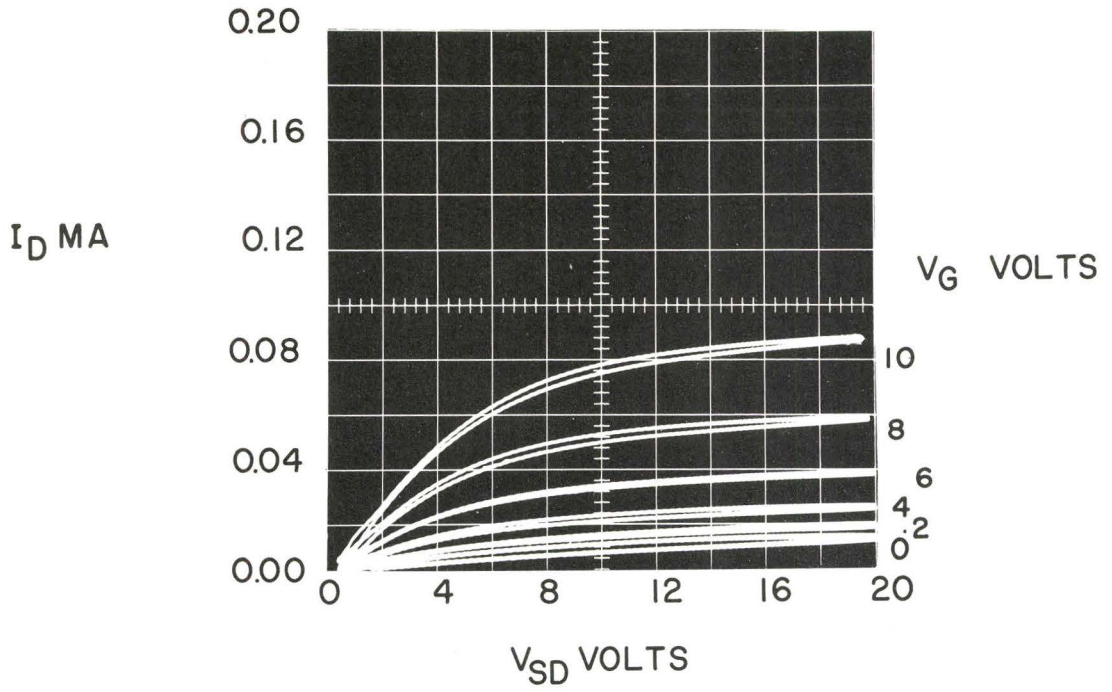


FIG. 5-6 TRANSISTOR SAMPLE # 10
ANNEALING 130°C FOR 193 HRS.

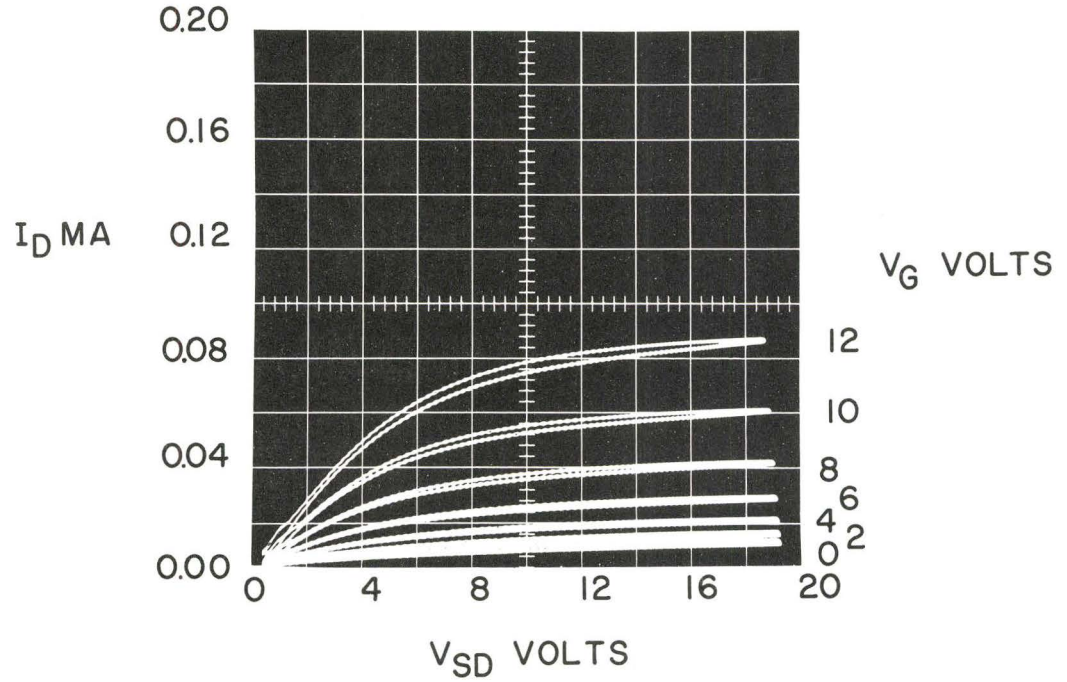


FIG. 5-7 TRANSISTOR SAMPLE # 10
ANNEALING 130°C FOR 288 HRS.

CHAPTER VI

CONCLUSIONS AND RECOMMENDATIONS

Thin Film Field Effect Transistors were produced that were stable with time. This success is attributed to the use of heavy passivation layers (≃ 10,000 Å) and an underlay of insulator (≃ 1,000 Å). In addition the failure of devices due to cover shattering after a period of time indicates the need for some initial heat treatment and hermetic sealing in a header after post deposition annealing.

Reproducible results were obtained by careful attention to technique and a careful evaporation of the semiconductor.

When evaporating the semiconductor the bulk material should be outgassed for a long period of time prior to evaporation. The outgassing should continue until the vacuum system has returned to its initial pressure. Just prior to evaporation the source should be heated up for about ten minutes and the rate brought up slowly to its final value.

The effects of post deposition annealing indicate its usefulness in improving device performance. It may also be used as a tool in "trimming" devices; that is, bringing them all to the same value.

The problems encountered in depositing ohmic contacts indicate another problem area. Even though successful contacts were evaporated there is some need for a thorough investigation in this area. Information obtained from such a study would be useful in the fabrication of thin film diodes.

The problems with the insulator indicate the need for another study of all the factors that influence the evaporation of Silicon Monoxide. It may even be profitable to use another insulator and this possibility should be investigated.

Similarly, the evaporation of Cadmium Sulphide should be more thoroughly investigated. Some thought should also be given to the use of another semiconductor such as Tellurium.

The substrate itself should be re-evaluated. Other materials should be looked at for their desirability as a thin film substrate. For example the use of anodized aluminum for high power devices could be investigated.

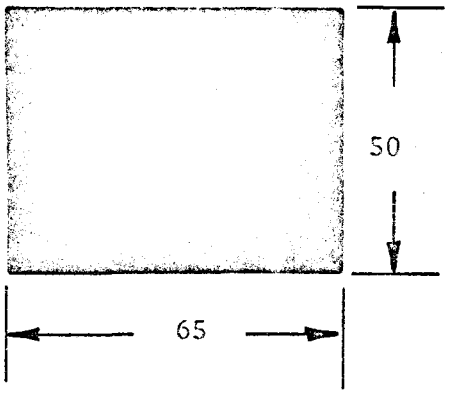
In summary, the feasibility of producing good active thin film devices has been shown. The problem areas have

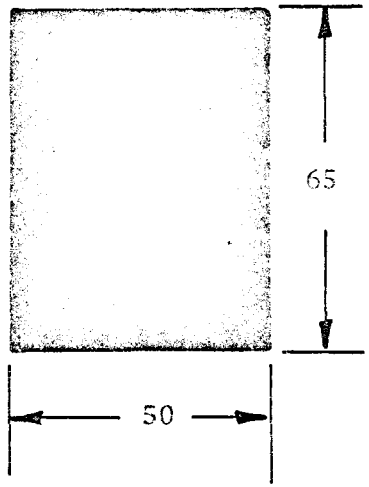
been identified and only those problems which are strictly mechanical (and solvable) have not been discussed. At this point a recapitulation should be made and a more thorough investigation of the problems carried out.

APPENDIX

Included in this Appendix are high contrast pictures of the mask apertures employed in this thesis.

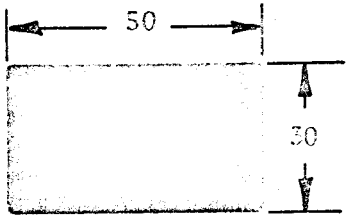
The pictures are enlarged approximately thirty times. Dimensions shown are nominal dimensions. Actual dimensions are shown in brackets. Any distortion in size and shape is primarily due to the enlarging process used to obtain these pictures.

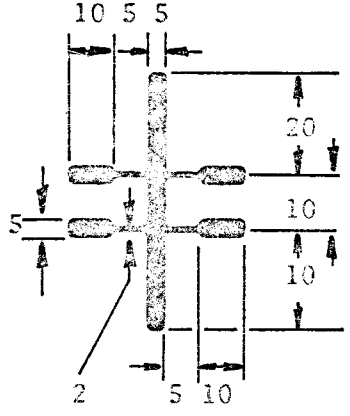




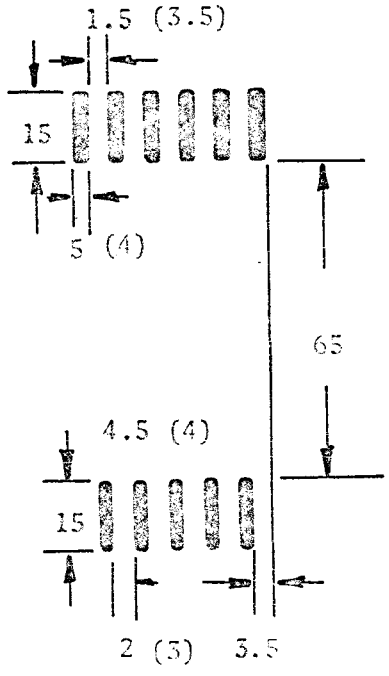
MASK #1 UNDERLAYER

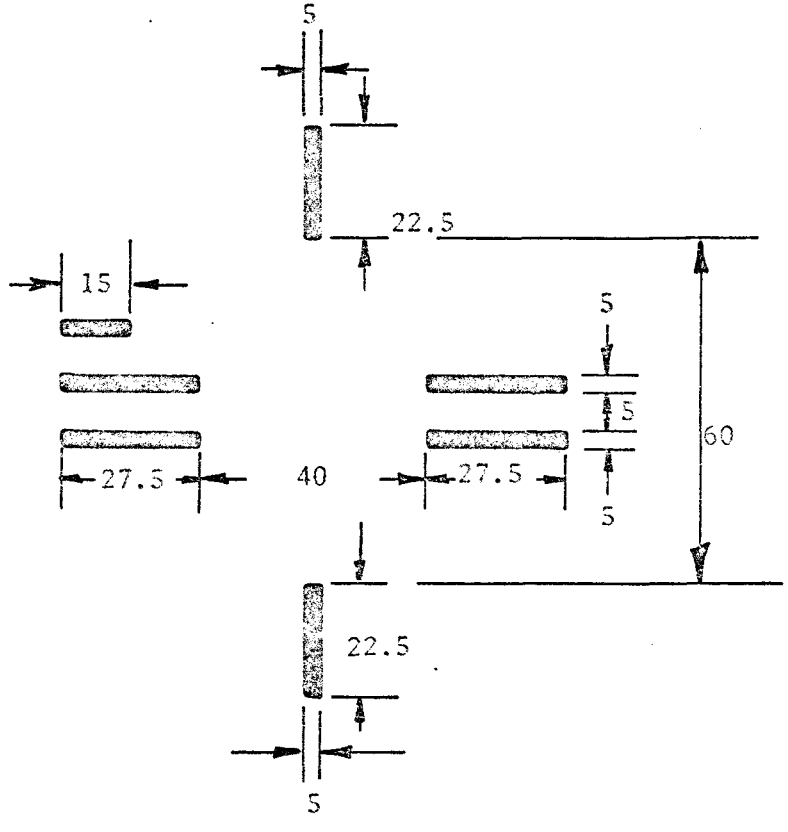
NOTE: In All Cases the Transistor is on the Left.
Dimensions are in Thousandths of an Inch.



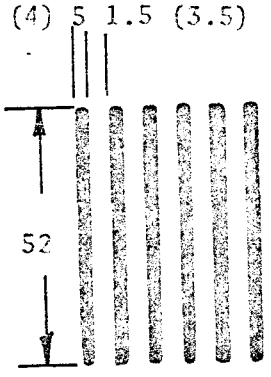


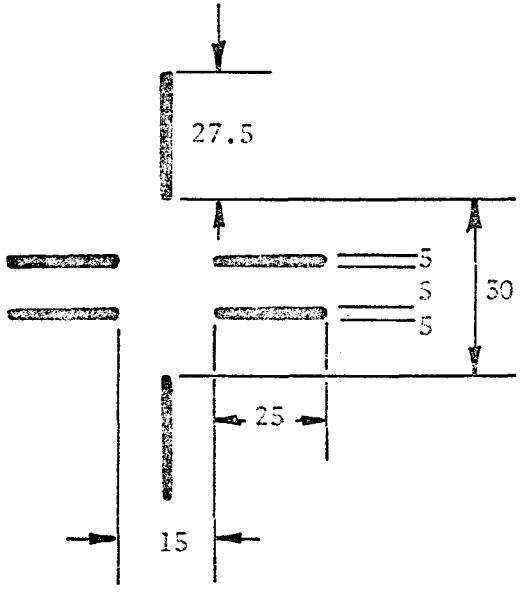
MASK #2 SEMICONDUCTOR



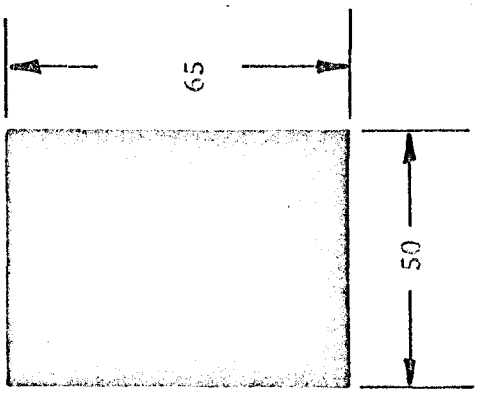


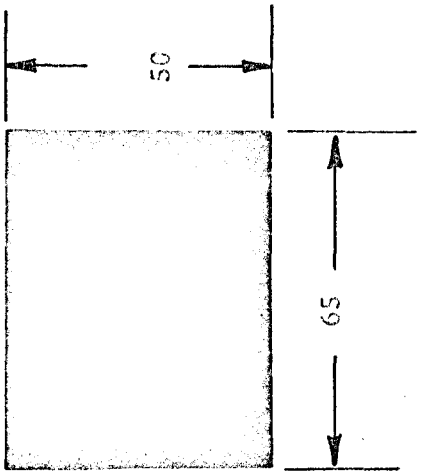
MASK #3 CONTACT PADS



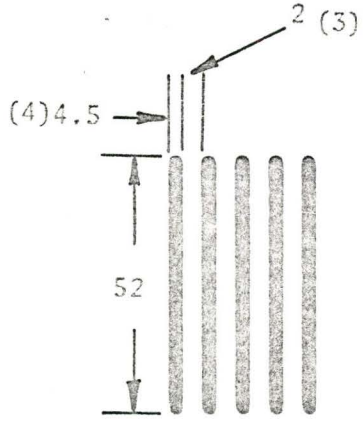


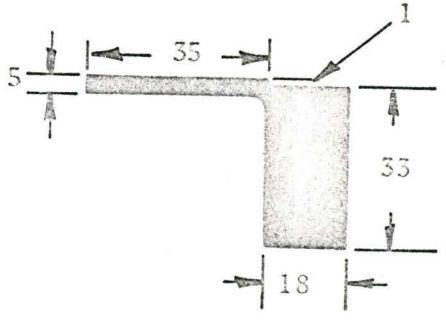
MASK #4 SOURCE-DRAIN CONTACTS



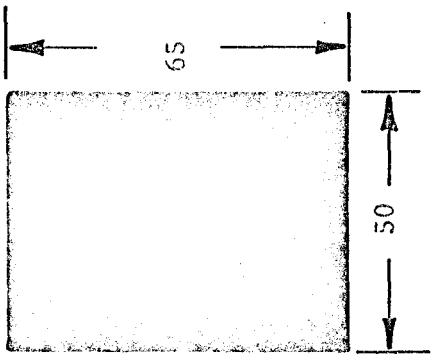


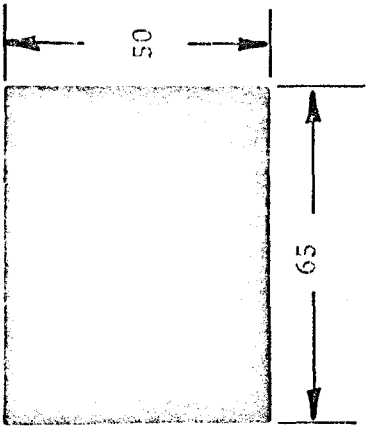
MASK #5 INSULATOR





MASK #6 GATE





MASK #7 COVER

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