MIS TUNNEL DIODES: APPLICATION TO SOLAR ENERGY CONVERSION

MIS TUNNEL DIODES: APPLICATION TO SOLAR ENERGY CONVERSION

by

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A Thesis

Submitted to the School of Graduate Studies

in Partial Fulfilment of the Requirements

for the Degree

Master of Engineering

McMaster University

July 1976

ABSTRACT

The MIS tunnel solar cell has recently attracted most of the attention in the solar energy conversion field. Construction is very simple and eliminates the costly diffusion of dopants. As in the Schottky type, a metal of proper work function is chosen to induce an inversion layer at the surface of the semiconductor (Al in the case of p type Si). An ultra thin (< 1.5 nm) oxide between the semiconductor and the metal passivates the surface by reducing surface states while permitting tunneling from the semiconductor to the metal.

Good fill factors (> .7) have been obtained but high reflectivity of the Al has reduced the current output. Open circuit voltages greater than .61 volts and short circuit current density of 21 ma/cm^2 have been measured. Experimental evidence of the presence of an oxide different from SiO_2 within 1.4 nm of the surface will be given and related to the thickness variation of the open circuit voltage. A maximum in V_{oc} around 1.4 nm was found. A maximum efficiency of 7% was achieved without anti reflexion coating and a curve factor of .81 was observed in one of the cells. A slight variation in efficiency with the cell area was also observed.

ACKNOWLEDGEMENTS

The author wishes to express his gratitude to his research supervisor, Dr. J. Shewchun, for his guidance and patience throughout the course of this work. Thanks also to R. Singh for his many pertinent comments. The technical assistance of L. Goodridge and A. Kazandjian is acknowledged.

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I INTRODUCTION

The new needs in energy have brought to attention the continuous research on alternate sources, particularly the solar energy. In an effort to produce higher efficiency solar cells, scientists have concentrated recently their search on the induced p-n junction type solar cell. A first attempt was made with Schottky cells but up to now the results have been deceiving. Open circuit voltages are lower than .5 volts and recent theoretical calculations[1] have shown that a maximum in efficiency of around 10% is the expected limit and that this is mainly because of surface recombination.

The introduction of an insulating layer between the metal and the semiconductor has been shown to reduce the surface state density by several orders of magnitude.[2] If this insulating layer is made thin enough that electrons can go through by tunnelling without being offered much resistance and thick enough to actually reduce significantly the number of surface states, surface recombination will then become very low.

In the past it has been very hard to produce good uniform thin insulators in a range between 1.1 and 2.5 nm. Thus again Schottky cells with an interfacial layer showed how open circuit voltages[3], the lack of information on the oxide formation and its properties for thickness around 1.5 nm limiting the research activities.

The techniques currently under study in our labs have shown the possibilities of controllable oxide growth even in those regions. Oxide formation due to the reaction at 800°C in a water vapor atmosphere of a Silicon surface, and the reaction in a hydrochloric solution of a Silicon surface have been studied. Cells fabricated by those two methods have permitted us to increase the open circuit voltage V_{oc} to .61 volts and to produce dark current characteristics very close to the ideal values.

Dependence curves of the solar cells open circuit voltages V_{oc}, short circuit currents I_{sc}, curve fill factors CFF, and efficiencies EFF as a function of oxide thickness have been measured. Comparison with the MIS solar cell theory[4] will be performed.

II THEORY

2.1 The Ideal Diode

Under forward bias, the equation giving the current in the ideal case is[5]

$$I = I_s[\exp(\frac{qV_a}{nkT}) - 1] \tag{1}$$

with I_s = saturation current

V_a = applied voltage

n = ideality factor

$\frac{kT}{q}$ = thermal voltage (.026 volts at room temperature)

The saturation current I_s is given by

$$I_s = A\ A^{**}\ T^2\ \exp(\frac{-q\phi_\beta}{kT}) \tag{2}$$

where A = area of the device (cm^2)

A^{**} = Richardson's constant, $\approx$ 32 A $cm^{-2}K^{-2}$ for p type Silicon

ϕ_β = junction barrier height

An extrapolation from the region where the 1 in bracket in eq. (1) is negligible to $V_a = 0$ will give I_s, from which ϕ_β is easily calculated. The value of n (= 1 in the ideal case) can also be computed from the slope of the I-V curve drawn on a semi log graph in the region mentioned above.

Under illumination, the current in eq. (1) becomes

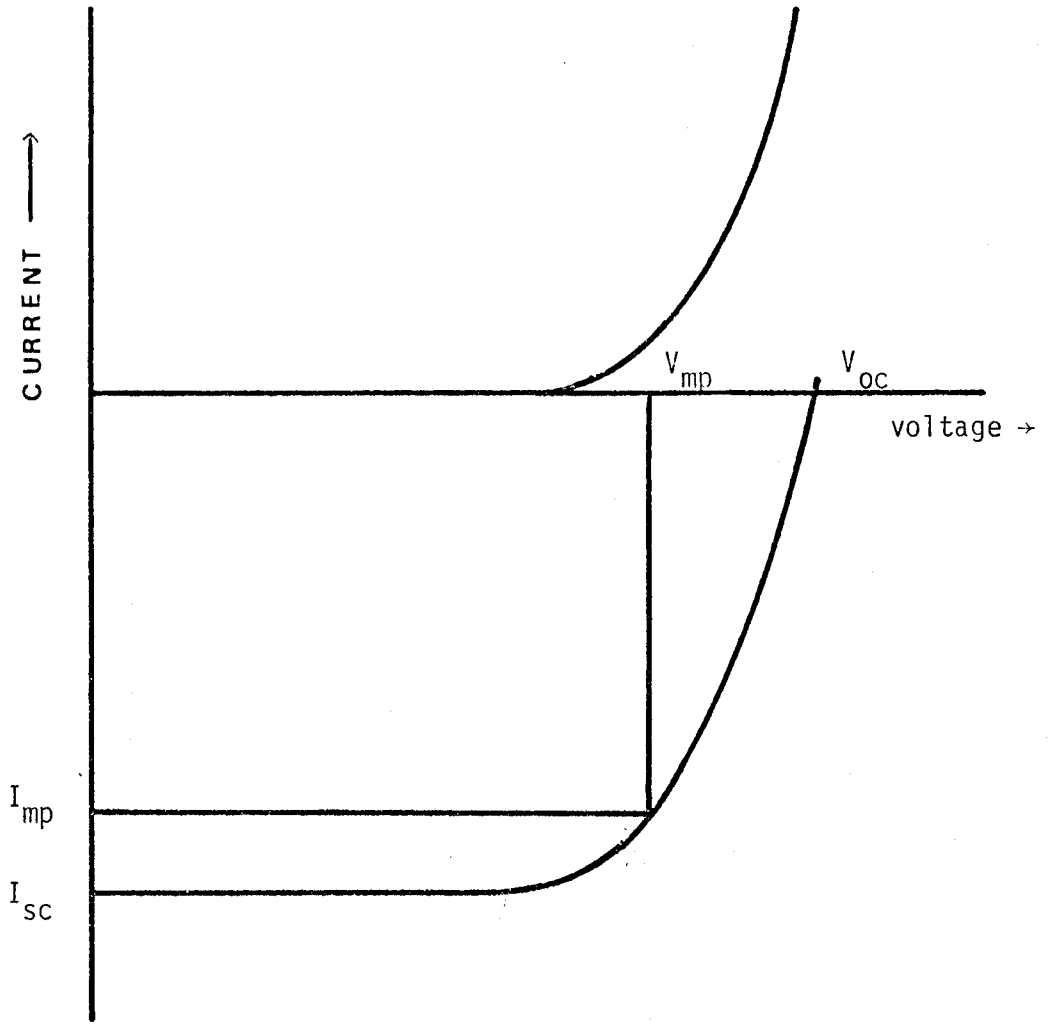
$$I = I_s \left[\exp\left(\frac{qV_a}{mkT}\right) - 1\right] - I_L \qquad (3)$$

where I_L is the current generated by the absorption of light.

Figure 1 shows the I-V curves of an illuminated and unilluminated photovoltaic cell. Four parameters are of interest in analysing the performance of a solar cell. They are, the short circuit current I_{sc}, the open circuit voltage V_{oc}, the current under maximum power transfer conditions I_{mp}, and the corresponding voltage V_{mp}. Those points are indicated in Fig. 1. Another useful value calculated from the previous ones is the curve fill factor CFF. It is by definition equal to $\frac{V_{mp} \times I_{mp}}{V_{oc} \times I_{sc}}$. The higher the values of the curve fill factor, the greater the efficiency of the cell. The efficiency under match load conditions is:

$$EFF = \frac{\text{output power}}{\text{input power}} = \frac{V_{oc} \times I_{sc} \times CFF}{\text{Area of cell} \times \text{incident light density}} \qquad (4)$$

Basic limitations to the performance of the cell can be seen from Eq. (3). A low I_L can be caused by reflection of the incident light on the cell, by incomplete absorption and by utilization of only part of the photon energy for the creation of electron-hole pairs. This results in a low short circuit current, thus a low power output. A low open circuit voltage can be caused by a low barrier height ϕ_β which is the difference in energy between the fermi levels of the n and p region. The higher the ϕ_β, the larger the field between the two regions, thus the more efficient the separation of charges within reach of the junction.



I-V curves: Dark condition and under illumination

FIGURE 1

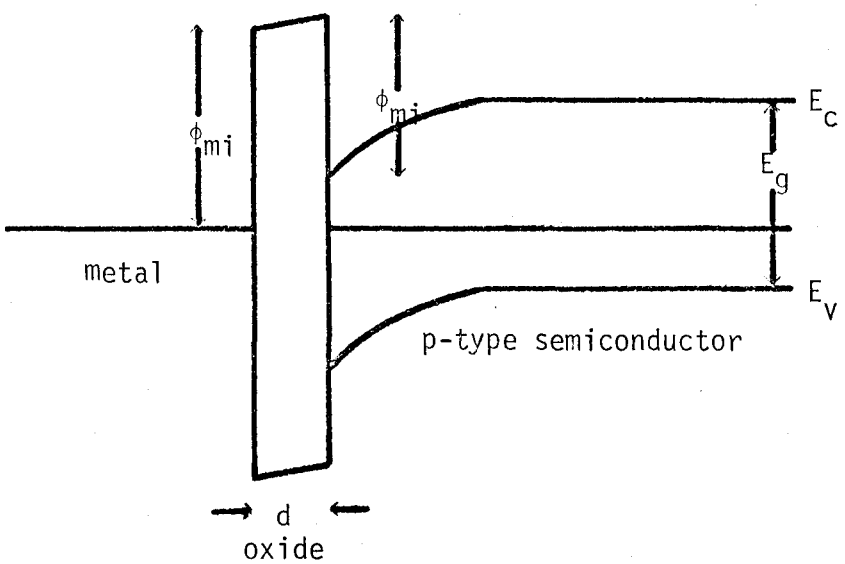
The ideality factor n is also very important. It is an indication of how close to the ideal diode one is. In order to obtain the best possible curve, n has to be at it's lowest value (i.e., 1). But due to recombination processes and series resistance, it rarely has a value lower than 1.1 - 1.3 and more often than not, around 1.4. This value of n directly affects the curve fill factor. The higher the n, the softer the I-V curve and the lower the curve fill factor. Thus in order to obtain good power output, one should aim at an n value very close to 1. Among these limitations, some are mainly determined by techniques employed and improvements of these may be possible up to near elimination of their influence, like reflection losses, series resistance and grid collection efficiency.

The problem of series resistance has been treated by Prince[6]. Assuming an infinite shunt resistance, he calculated the relative values of curve fill factors for different series resistances. Those are 1, 0.77, 0.57, 0.27, 0.14 for a series resistance of 0, 1, 2, 5, and 10 ohms, respectively. Thus one can see that a 5 ohm series resistance reduces the available power to less than 30% of the optimum power with no series resistance.

2.2 MIS Tunnel Diodes

The MIS structure has been under investigation for several years and is now widely used in modern electronic devices.

A band diagram of a MIS tunnel diode is shown in Fig. (2). In this case a semiconductor of type p with aluminum as the metal is



Schematic energy band diagram of a metal insulator semiconductor diode

FIGURE 2

represented. The role of the interfacial layer has been abundantly discussed and only particular aspects will be mentioned here[4,7-9].

Due to the difference in energies between the metal and semiconductor conduction bands, an inversion layer is formed at the surface of the semiconductor. On a p-type semiconductor, the inversion layer is composed of electrons as majority carriers. Oxide charges caused by mobile ions penetrating the insulator or ionized traps, and surface states originating from the interruption of the periodic lattice structures at the surface of the crystal can also affect the energy difference between the semiconductor and the metal. The density of surface states measured on clean oxide free surfaces has been shown to reach the density of surface atoms[11]. But the presence of an interfacial oxide layer proved to be very efficient in reducing the surface state density by several orders of magnitude[12].

Since the insulating layer can be made thin enough that a tunneling probability of the electrons through the oxide is very high, large tunnel currents can flow between the metal and semiconductor. And because the metal and semiconductor have been chosen such that an inversion layer is created at the semiconductor surface which now has a lot less surface states, the device should exhibit characteristics closer to the ideal junction diode[8] than the Schottky device will.

The creation of an inversion layer without the use of a dopant reduces recombination within the semiconductor and also fabrication cost. The use of an interfacial layer reduces surface recombination and increases the barrier height of the solar cell. Such properties motivate the use of an MIS solar cell over the conventional diffusion junction cell.

Theoretical calculations of the efficiency of MIS solar cells made by Singh[4] indicate that an optimum thickness around 1.1 nm for the insulating layer should be used. Dependence courses were also produced which showed a linear decrease of the open circuit voltage V_{oc} with increasing oxide thickness and a constant short circuit current density J_{sc}, curve fill factor CFF and efficiency up to a thickness of 1.5 nm and a subsequent sharp decrease of those three parameters for thicker oxides. This drop can be explained as an increase in the effective series resistance for the tunneling current varies exponentially with thickness. The surface barrier height ϕ_β which should be the largest possible is proportional to the metal to insulator barrier (see Fig. 2). But when taking into account surface states and oxide charges, an effective metal to insulator barrier ϕ'_{mi} has to be introduced

$$\phi'_{mi} = \phi_{mi} - \frac{q(Q_{ss} + Q_c)d}{\varepsilon_i} \qquad (5)$$

Q_{ss} represents the surface state charge, Q_i the oxide charge and ε_i the insulator dielectric constant. The term in parentheses being positive, ϕ'_{mi} will decrease with increasing oxide thickness or increasing charges, and by the same way will the open circuit voltage V_{oc} follow. An increase in Q_{ss} and Q_i will at the same time affect the current by introducing recombination centers and tunneling paths in the oxide. A reduction of the second term in Eq. 5 or a change in sign of this same term will generate an increase in ϕ'_{mi} and thus V_{oc}. If one could control Q_{ss}, Q_i and ϕ_{mi} adequately, a maximum in V_{oc} could be formed for any thickness

and type of oxide. For the Al-SiO_2-Si system, ϕ_{mi} was measured to be 3.2 eV. It is to be noticed that in this theoretical model, Q_{ss} and Q_i are taken as thickness independent and ε_i as a constant evaluated for a thick SiO_2 oxide.

III EXPERIMENTAL PROCEDURE

3.1 Sample Preparation

In order to be able to reproducibly grow oxides less than 2 nm thick, the Silicon surface must be atomically cleaned prior to oxidation. The wafers were bought from Monsanto. The cleaning procedure of the wafers is the following[13] and is the same for all dopings and orientations.

- The wafer is first boiled for 10 minutes in H_2SO_4:H_2O_2 (2:1) to dissolve any organic compounds and greases on its surface.
- It is then rinsed in flowing de-ionized water (18 megohms) for 5 minutes.
- A second boiling in H_2O:HCl:H_2O_2 (4:1:1) is performed (10 minutes) to eliminate the metallic ions from the surface.
- Again the sample is rinsed in de-ionized water (5 min.).
- Finally the wafer is etched in dilute HF (10%) for 5 min. and rinsed.

All the chemicals used are reagent grade. The presence of H_2O_2 in the solution is necessary to produce an oxide on the surface in order to protect it. It is then taken off by the HF.

A residual layer of less than .5 nm of oxide could not be eliminated, for the moment the sample was exposed to air, it started to oxidize. Two types of oxide growth were performed. The mostly used and better known is the water vapor oxide growth. It consists in placing in

a furnace at temperatures between 700°C and 900°C (800°C was found to be the most efficient temperature for our system which had a 2 inch quartz tube in the furnace and a water bubbler containing approximately 3 liters of de-ionized water) a cleaned wafer over which is flowed water vapor. Growth rates of 3nm/100 sec were mainly used. Since the oxide thickness critically depends on the humidity in the lab, the vapor flow rate and cleaning, for each sample made into a solar cell, a twin sample was submitted to the same procedure for thickness measurement purposes.

The second type of oxide (referred to as beaker oxide) was grown in the following way. After carefully cleaning the wafer, 1 to 5% of HCl was introduced as a getterer in the de-ionized water in which the wafer was sitting. At room temperature, oxides of 1.0 nm took as long as two hours to grow. This slow growth rate technique assures us of the uniformity of the oxide across the sample. This beaker growth technique was used elsewhere[14] with HNO_3 to accelerate the growth rate but no measurements were conducted on the electrical characteristics of such oxides by the authors.

3.2 Oxide Thickness Measurement

Oxide thickness measurements were made by ellipsometry using the computer program written by McKrakin[15]. The compensator was situated before the sample. The index of refraction of the oxide was made a variable so that we could follow its variation with oxide thickness. The precision in the thickness measurement is given as .1 Angstrom by computer calculations. But the size of the beam being around 6 mm in

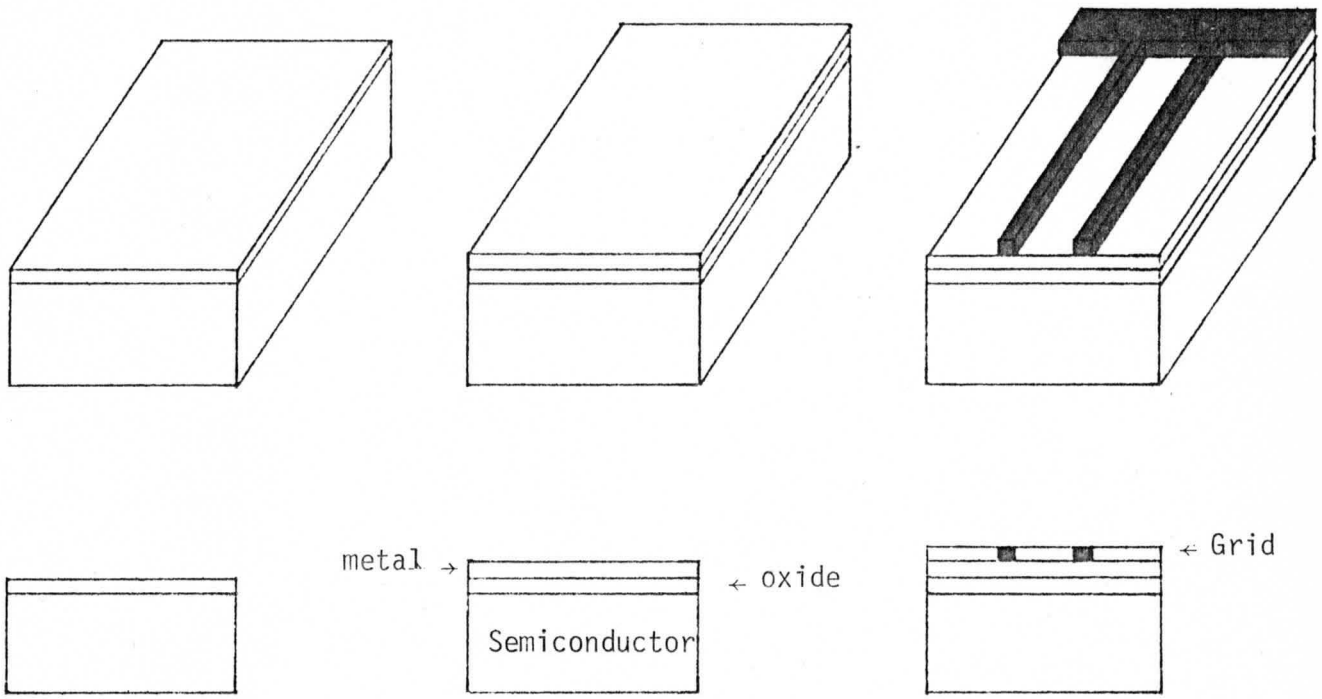
diameter, the result is obviously an average over that dimension. By rotating the sample in such a way that the incident light on the sample is perpendicular to the light used in the previous calculation, it concluded that the oxide was uniform to ± .5Å over .5 cm. This was further verified by electrical measurements which will be discussed later.

3.3 Contact Evaporation

Contact evaporations were made in an NRC vacuum system at bell jar pressure below 5×10^{-6} torrs. The evaporation sequence varied for the two different growth techniques.

For the vapor oxides, a first thin layer of aluminum 5.0 to 6 nm thick was evaporated. Thickness was monitored by a Sloan Thickness Monitor with crystal frequency at 5 Megahertz. Deposition rates were kept below .5 nm/sec for better transmittance as pointed out by Charlson[16]. Then followed the evaporation of an aluminum grid contact for current collection purposes (Fig. 3). Black wax was subsequently spread on the front surface and the back oxide was stripped with HF. The sample was rinsed, the black wax removed and a large area back ohmic contact deposited.

Due to the fabrication procedure of this device, no annealing could be performed. Indeed, it has been shown that the aluminum will migrate through an oxide 2.5 nm thick with ease during a 5 minutes anneal at 500°C.[17] Microcracks were also considered as a possible cause of shorting of the device when annealed but electrical measurements of the uniformity of the oxide proved the assumption to be wrong.



Fabrication sequence of the MIS cell

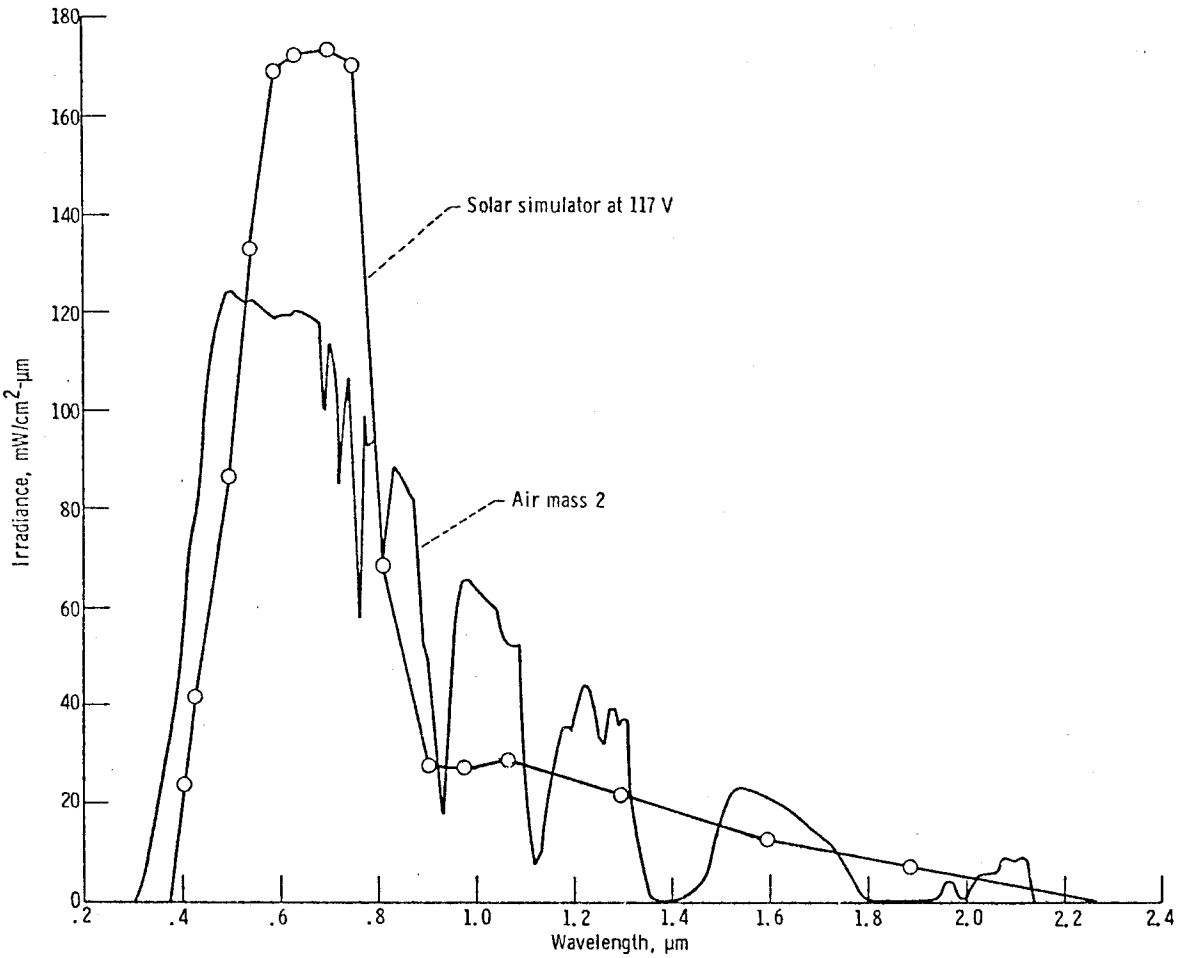
FIGURE 3

In the case of beaker oxides, the large back contact was first evaporated and an anneal under vacuum (5 x 10^{-6}Torr) at 400°C for 30 min. was performed. The front contacts were subsequently deposited. The deposition sequence as described in the case of vapor oxides was also tried here but not good diodes could be formed.

3.4 Experimental Set-Up and Testing Procedures

In order to ensure the relevancy of our measurements to terrestrial applications of solar cells, an air mass 2 (AM 2) solar simulator was built. The low cost and availability of parts as well as the average position of the sun during the day directed our choice.

The simulator consists of four 300 watts quartz ELH lamps (tungsten halogen) from General Electric with incorporated dichroic filters. The filters take the form of a special coating on the inside of the transparent lamp shades permitting transmission of the infrared, thus reducings its intensity at the level of the cells. Each lamp is provided with a filter. The lamps also require forced air cooling to limit the surface temperature at their base, as recommended by the manufacturer, to a maximum of 290°C. Temperatures greater than this value increase the likelihood of electrode seal destruction and subsequent lamp failure. On the other hand, excessive cooling of the bulb itself may also decrease lamp life by interfering with the tungsten-halogen cycle.[18] A spectral energy distribution of the simulator is given[18] in Fig. 4. Fairly close agreement between the AM 2 spectrum and the simulator is noted. Different filters can be incorporated to further reduce the far infrared content.



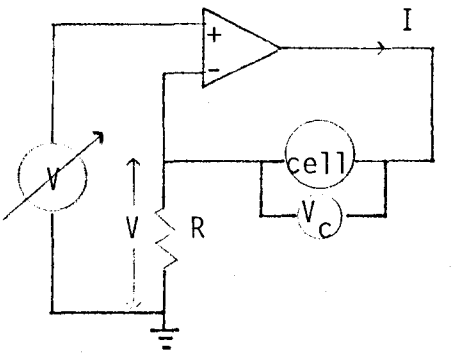
Variation of irradiance with wavelength

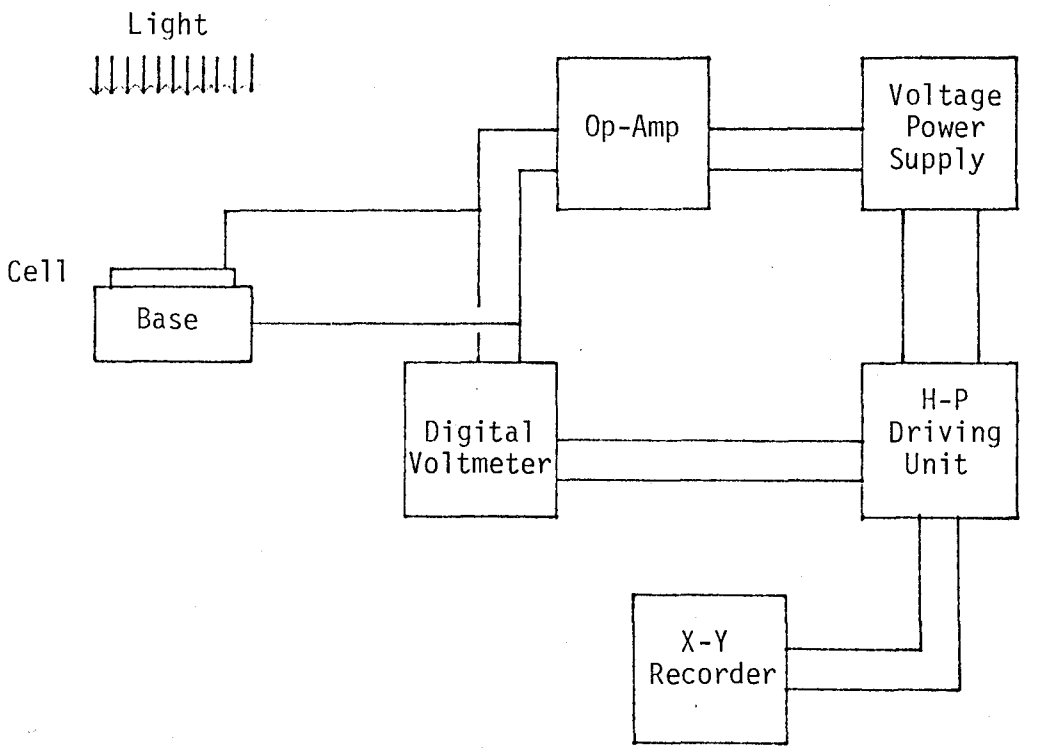
FIGURE 4

The incident light intensity was adjusted with the help of a calibrated cell from NASA Lewis Research Center. The I-V characteristic under AM 2 illumination of the calibrated cell as given by NASA is reproduced in our lab. Provided our cells have the same spectral response as the calibrated one, the error introduced by using the AM 2 simulator instead of a Xenon arc lamp is less than 3%. A water cooled base on which seats the solar cell permits constant temperature measurements. A diagram of the experimental set-up is shown in Fig. 5. From the programable power supply (HP 6131B source) driven by the HP9820 calculator, a voltage V is applied to the op-amp. A current $\frac{V}{R}$ is thus forced into the cell. The induced voltage appearing across the device is then measured by the digital voltmeter and relayed to the computer which transfers it to the recorder. For V = 0, no current goes through the cell. This corresponds to the open circuit configuration. The power supply has a range of -20V to +20V. Thus for R = 10Ω, up to 2 amps can be fed into the cell permitting the short circuit condition to be easily reached.

3.5 C-V measurements

C-V measurements were made solely on thick oxides since no means were available to measure surface state densities for oxides of thicknesses in the vicinity of 2.0 nm or less. At all times this density was kept below $10^{12}/cm^2$ for oxides of 100 nm.





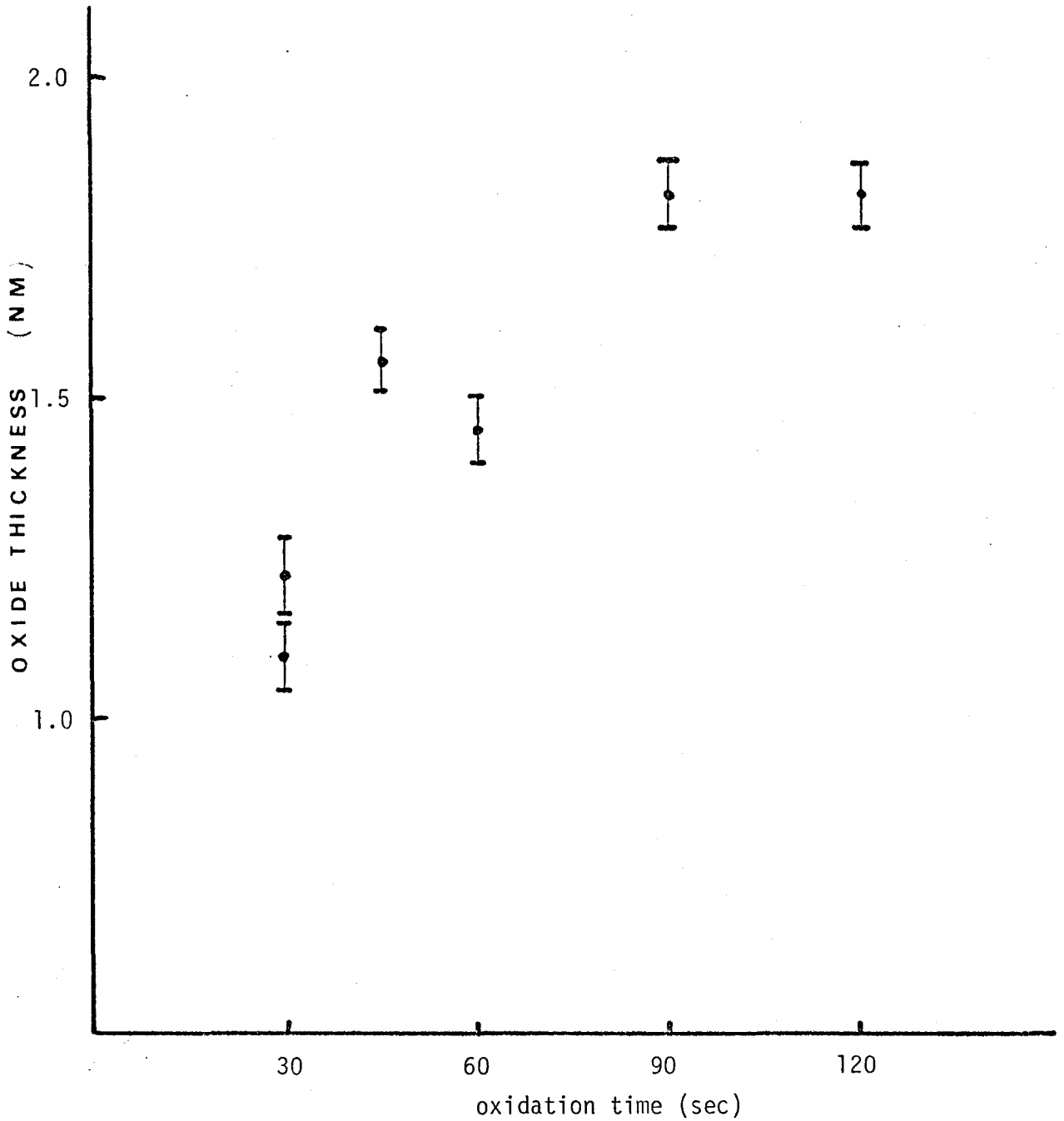
Block diagram of the experimental setup

FIGURE 5

IV RESULTS AND DISCUSSION

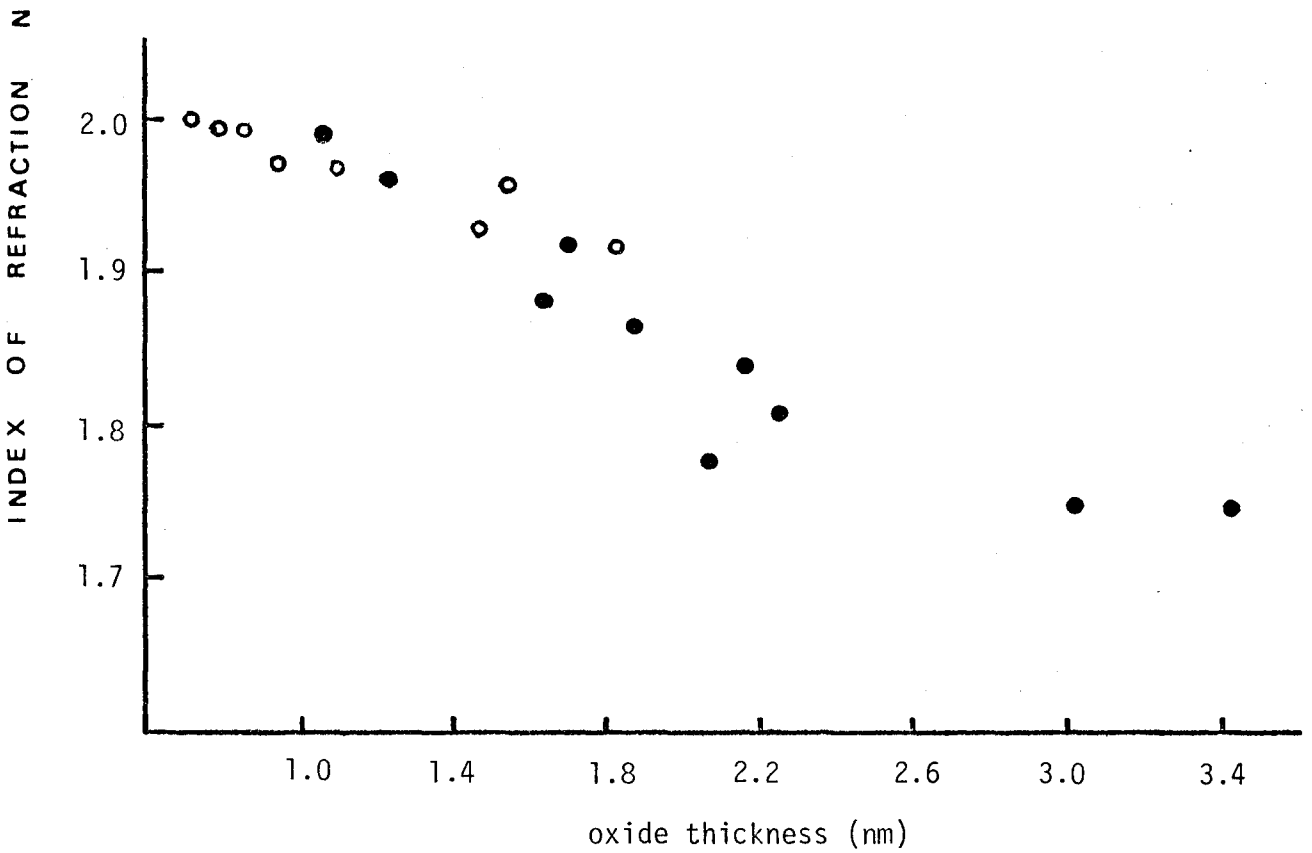
4.1 Physical Properties of the Oxides

The production of ultra thin oxides in a controllable fashion is a very delicate process which is still not nowadays totally mastered. A growth curve shown in Figure 6 illustrates the fluctuations encountered in the vapor oxide thickness for the exact same cleaning procedure. The variations are attributed to changes in the laboratory atmospheric conditions, mainly humidity, which in turn affects the water boiling temperature and vapor pressure. For this reason, each solar cell was produced with a twin sample used for thickness measurements. This method was also applied in the case of beaker oxides. As mentioned earlier, thickness measurements were made by ellipsometry. It was found that the index of refraction of the oxide varied with thickness as illustrated in Figure 7. The reason for this behavior is twofold. First, in that range of thicknesses, the non-uniformity of the oxide over a fairly large area can be a cause of error in the thickness computations. If the oxide exists on the substrate in the form of hills and valleys, the measured index of refraction will be an average over the different optical constants of those imperfections. The second reason is simply that we are not looking at SiO_2 as expected but at another type of insulator. This has been confirmed by Raider[19] who made stoichiometry measurements by X-ray photoelectron spectroscopy and found that the composition of the SiO_x oxide varied with thickness. They determined a transition region around 1.4 nm below which SiO_2 does not exist. Rather this region was found to be graded in composition between the silicon substrate and the stoichiometric SiO_2 film



Oxide thickness vs oxidation time (water vapor) at 800°C for <100> .2 Ω cm p type silicon wafers

FIGURE 6



Index of refraction vs oxide thickness

FIGURE 7

(i.e., x increases with thickness). The fact that the index of refraction does not reach the value of 1.45 attributed to SiO_2 for thick oxides (it is still 1.7 for a 3.0 nm oxide) is simply due to the optical path of the light beam which is traveling mostly in the SiO oxide.

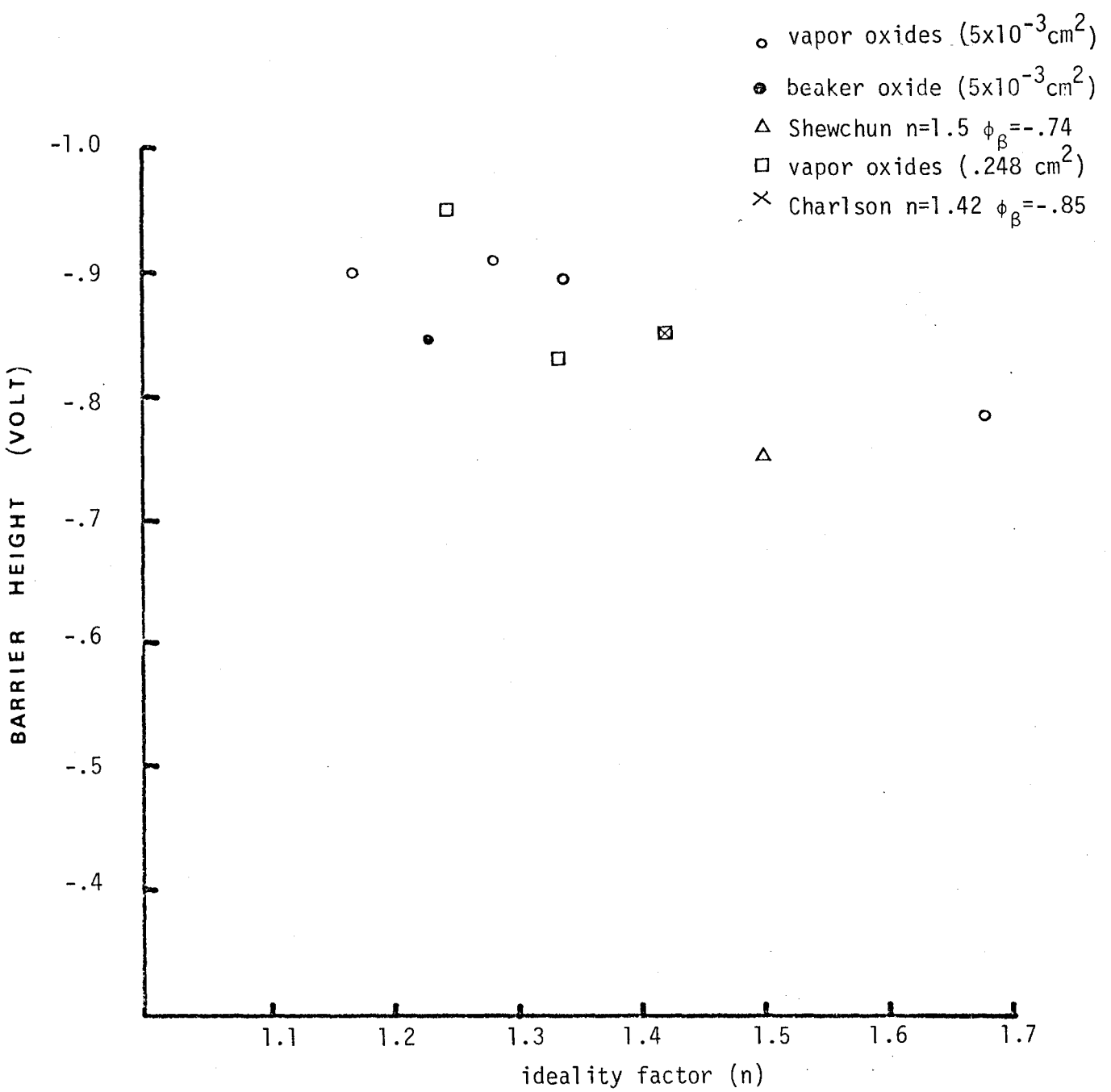
4.2 Electrical Properties of the Oxide

The conclusion drawn in section A will force some changes in the MIS theory. In Eq. 5, the dielectric constant of SiO_2 will have to be replaced by a thickness dependent variable. Also, since the density of dangling bonds at the silicon-insulator interface is proportional to the SiO_2 content in the oxide, N_{ss} will have to vary accordingly with the film composition, i.e. N_{ss} is maximum at d = 0 and diminishes with thickness. It is reasonable then to assume that surface state density measurements on thick oxides (C-V) can only be employed as an indication of the cleanliness of the system and not as an absolute value to be used for ultra thin oxides. Oxide charges and traps cannot be directly measured for the same reasons invoked earlier in the case of surface states and also because, as was recently reported[20], minority carrier tunnel non equilibrium diodes are not suitable for obtaining data on interface and oxide states by C-V analysis.

As a supplementary test of the uniformity of the electrical properties of the oxide, 17 cells were made on a 1 inch wafer. Variations in the open circuit voltages across the wafer were less than 10% with a maximum of .565 volts and a minimum of .54 volts indicating a fairly uniform oxide. Leakage currents were less than 1 μA at -1 volts on all cells.

4.3 Barrier Height and Ideality Factor

In the process of solar cell fabrication, it is of prime importance to know the quality of the p-n junction. The data on the junction is mostly furnished by the dark I-V curve from which one can calculate the ideality factor n and the barrier height ϕ_β. The higher the barrier height and the closer to 1 the ideality factor, the better the diode. Theoretical calculations of values of n for different oxide thicknesses have been performed by Green[8] and measurements made by Shewchun[21], but no systematic studies of the barrier height were included. In our case, both values were measured. A plot of ϕ_β vs n is shown in Fig. (8) including two different diode areas. The same cleaning processes were used for every cell. A decrease in ϕ_β with n is seen. Two experimental points from separate authors are included in the graph and agree fairly well with the observed behavior. A high n value indicates high series resistance effects and recombination thus leading to low current outputs and poor curve fill factor. At the same time, a high n will also indicate a low open circuit voltage of the solar cell since V_{oc} is directly proportional to ϕ_β. It is then in one's interest to try to achieve the lowest n value (between 1.1 and 1.3) for it is where the highest barrier height is found. It is to be noticed that the two areas yield similar results for n and ϕ_β. The data shown in the figure is from vapor oxides. Similar measurements performed on beaker oxide showed that for the same ϕ_β, a lower n value is obtained, that is, the curve is shifted to the left. For example, for ϕ_β = -.84 volts, n = 1.23. This lower value of n is partly due to the anneal which is performed on the back contact of the



Barrier height vs ideality factor
at .5 Volt

FIGURE 8

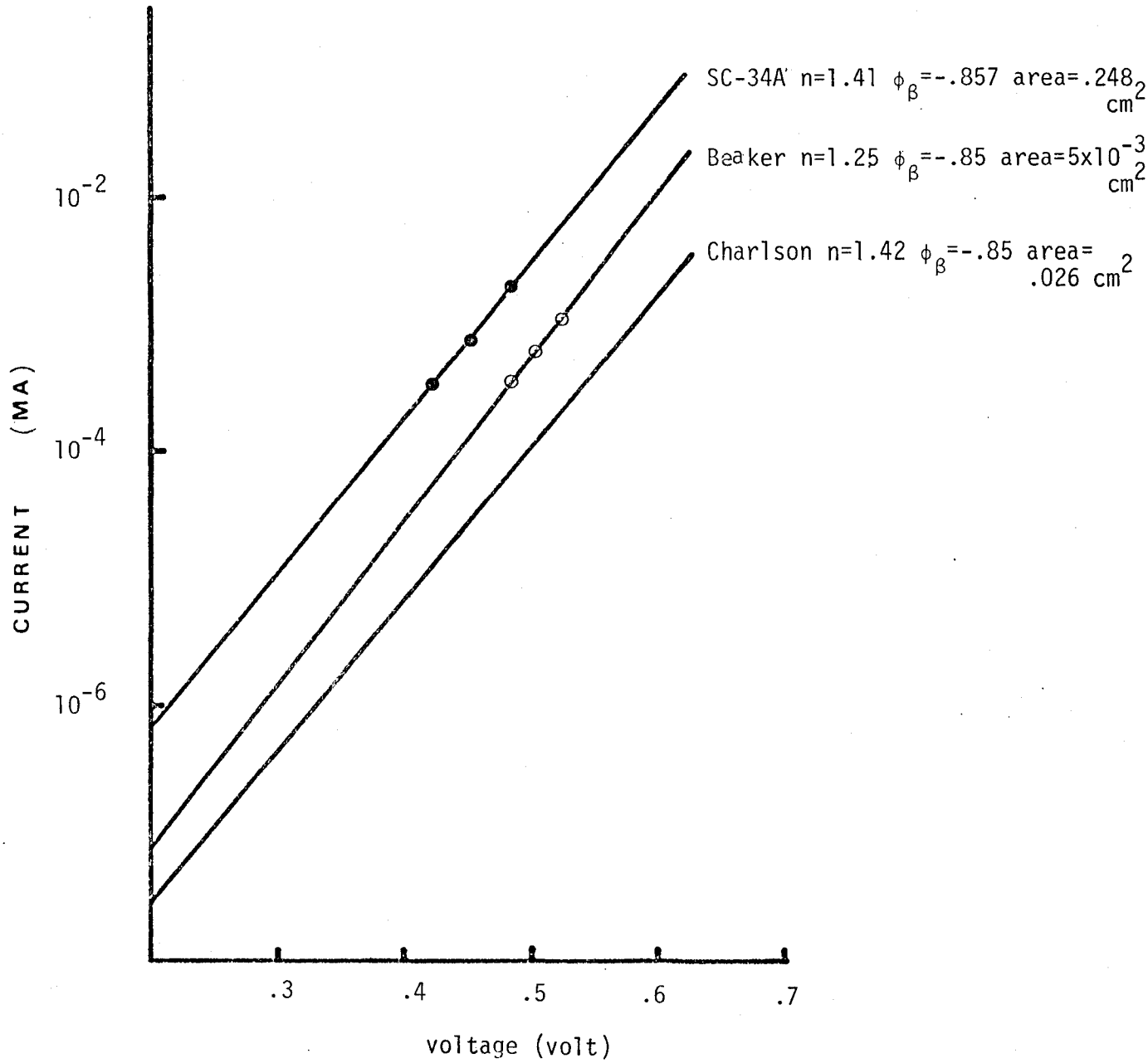
cell and reveals a lower contact resistance, a better ohmic contact. It is also due to the creation of traps originating from the evaporation of water molecules in the oxide. A comparison of the dark I-V curves of vapor oxide and beaker cells and Charlson's cell[12] is given in Fig. 9. As we can see the slope of the vapor oxide cell and Charlson's are nearly identical indicating the same n value.

4.4 Metal Transmission

The first layer of Al which serves to induce the inversion layer in the semiconductor has to be as thin as possible in order to let most of the light through but at the same time the sheet resistance must be kept as low as possible. The influence on the cell's I-V characteristic of a 6.0 nm layer of Al is shown in Fig. 10. From the ratio of the short circuit currents, a transmission of only 70% was calculated for the Al layer. This leads to a difference of 2% in the total efficiency. The resistance of a 1 cm^2 sheet of Al of such a thickness is approximately 3.3 Ω which is not negligible and can reduce the curve factor.

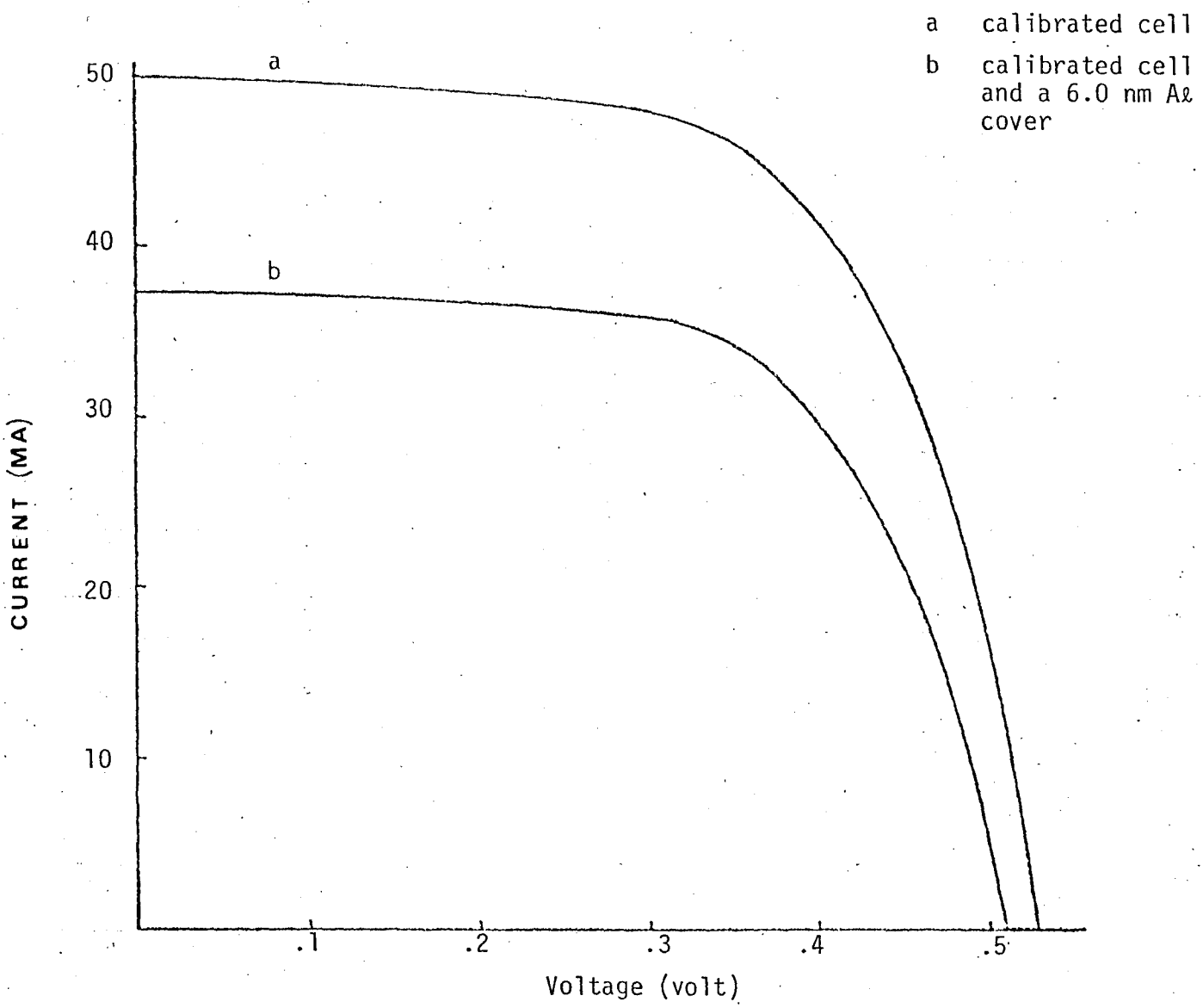
4.5 Effect of Surface States

Surface states tend to reduce the performance of the MIS cell at thicknesses below 1.4 nm but can be an advantage at larger thicknesses.[4] It is known that annealing an oxide will increase the quality of the oxide. A good example is given in Fig. 11 where the dark I-V characteristics of a becker oxide diode is shown prior to anneal and after a 30 minute anneal at 300°C. We see that before the anneal, the diode possesses a very high



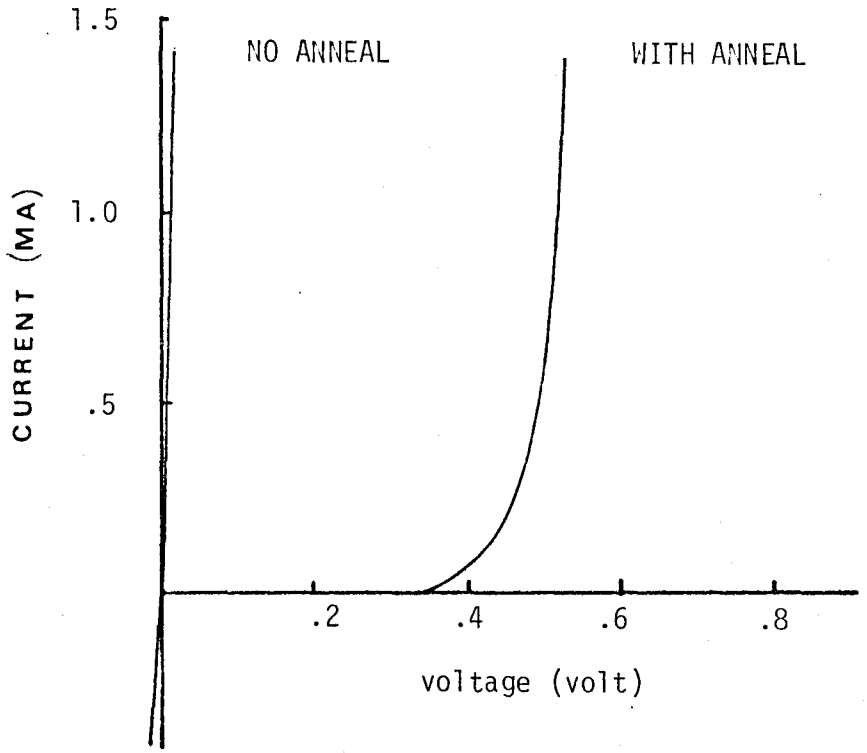
Comparison of dark I-V curves

FIGURE 9



Influence of the 6.0 nm Aℓ layer on the current output

FIGURE 10



Dark I-V curves of an annealed and a non-annealed beaker diode

FIGURE 11

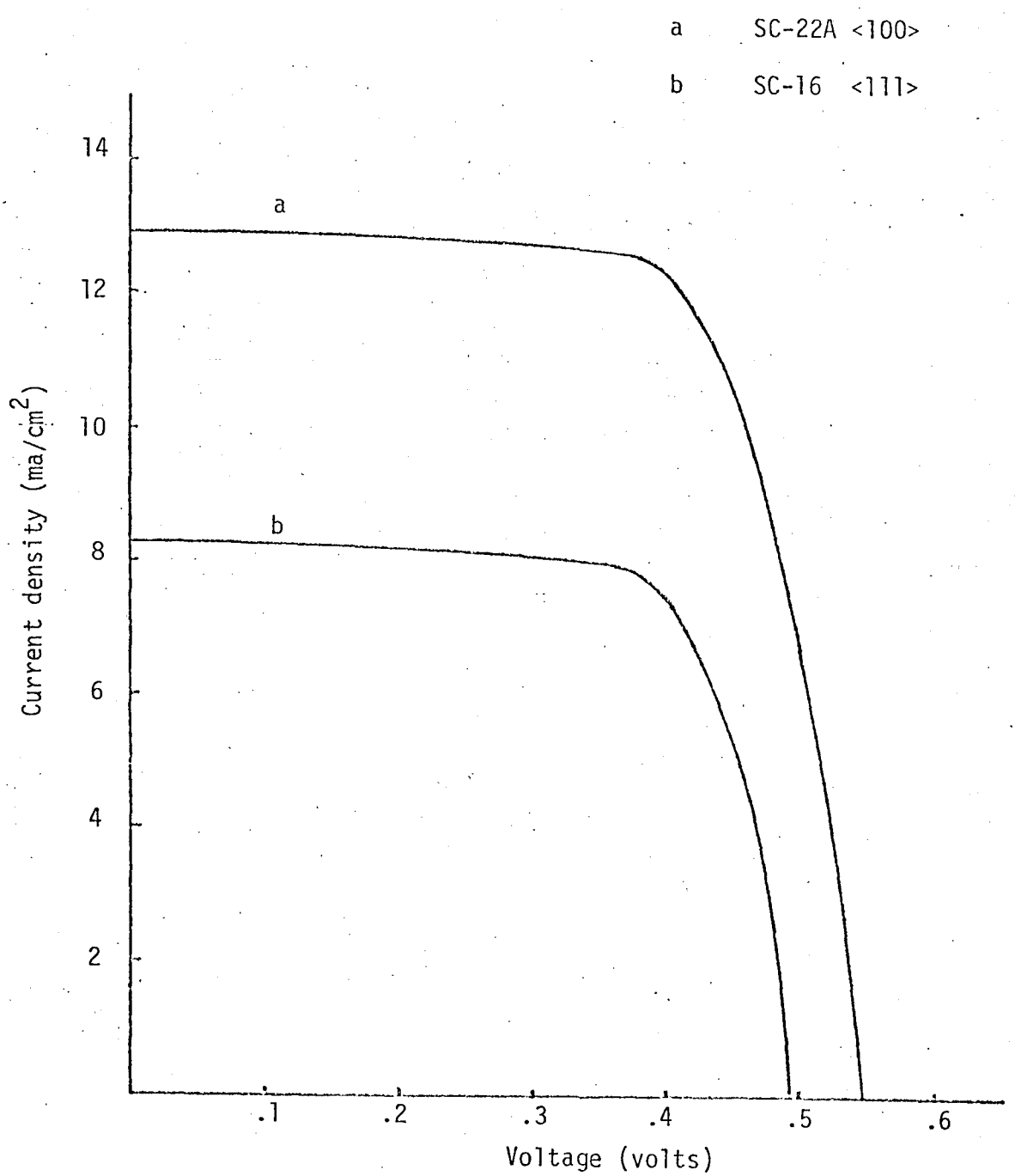
leakage current (- 5 ma at -1.5 volt) and very low turn on voltage. After anneal, the leakage is reduced to -2. μA at -2.5 volt and the turn on voltage is around .45 volt. Ideality factor and barrier height were respectively 1.23 and -.845 around .5 volt. Part of the change is due to a decrease in back contact resistance but mostly to reduction in surface states and interface instability[22]. It is well known that the surface state density will vary when the semiconductor surface orientation is changed[23]. This has also been observed (Fig. 12). The short circuit current is much lower in the case of a <111> because of the large recombination.

4.6 Thickness Dependence of the Cell Parameters

The following results are for p type silicon, .2 Ω cm, <100> and vapor grown oxides at 800°C. The cell area is .248 cm^2. (Under 100 mw/cm^2)

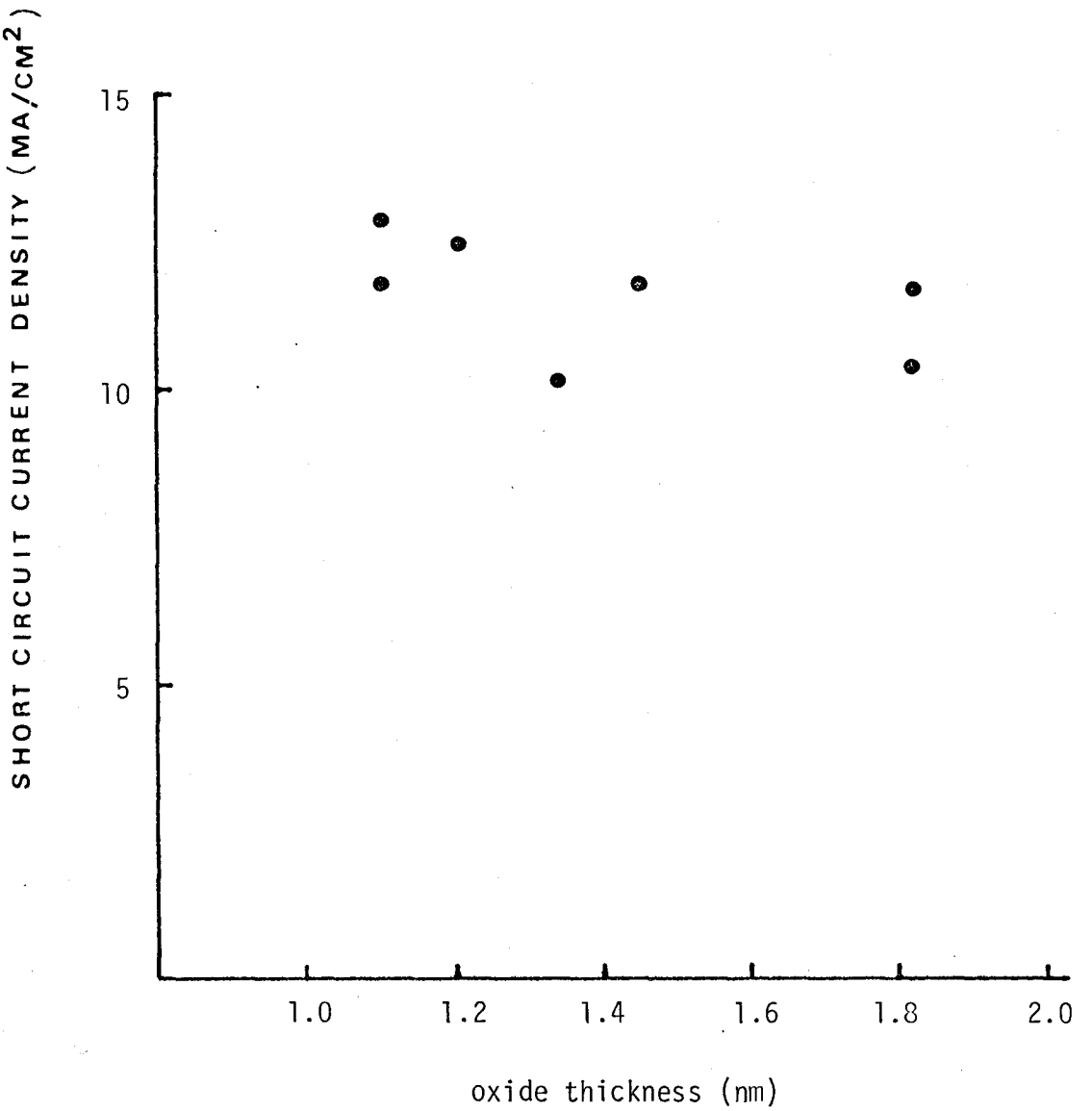
i) Short circuit current density

The short circuit current density was quite low compared to the expected value of 26 ma/cm^2 (AM2) Fig. (13). It was approximately constant over the studied range of thickness (from 1.1 nm to 1.8 nm) which is feature predicted by Singh[4]. A slight variation in J_{sc} was observed with the area of the cell considered. It was maximum (> 21 ma/cm^2) for the smallest area of cell ($\tilde{\sim}$ .85 mm in diameter) which is an indication of collection efficiency problems. The contours of those cells were not shielded which does not exclude the possibility of collection from areas not covered by the Al thus not included in the calculation[23].



I-V characteristics of cells of different crystal orientations

FIGURE 12



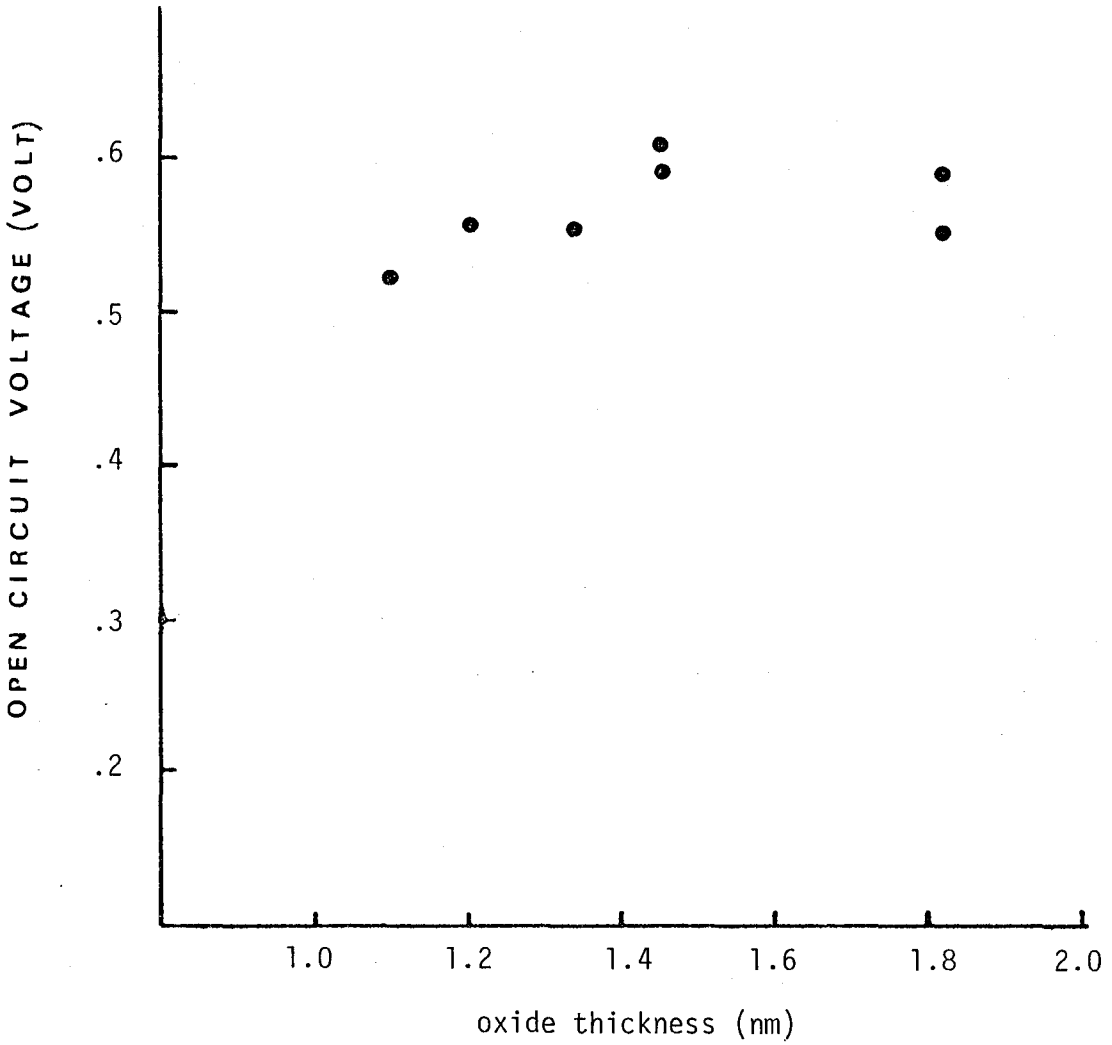
Short circuit current density vs oxide thickness

FIGURE 13

As explained earlier, a 30% difference in current is also due to poor transmission of the Al layer. The low J_{sc} cannot be caused by large series resistance for the curve fill factor would not be as high. It is thus concluded that the low J_{sc} is due to collection and transmission problems. A thinner Al layer could be used but one has to increase the collection efficiency of the grid pattern to counteract the increase in sheet resistance.

ii) Open circuit voltage

The main characteristic of this cell is by far its large open circuit voltage. Reports in the literature[24] show that nobody has yet achieved an MIS cell with an open circuit voltage greater than .45 volts and kept the curve factor high (> .65). We have been able to repeatedly fabricate cells with V_{oc} greater than .55 volts with CFF around .75. As shown in Fig. 14, values up to .61 volts were measured. One has to notice the presence of a maximum in V_{oc} around 1.4 nm. We propose that this bump is caused by two interacting factors. The positive slope, before 1.4 nm, is taken as an indication of a reduction of surface states as thickness increases. This goes accordingly with Raider's measurements which revealed an increase in the oxygen content of the oxide as one goes from 0 to 1.4 nm, thus resulting in a reduction in surface states or a reduction in free silicon bonds. Preliminary calculations performed by Sing[25] tabulated below clearly show the decrease in V_{oc} with increase in surface states for a thickness of 1.1 nm. Since a linear decrease in V_{oc} with thickness exists,



Open circuit voltage vs oxide thickness

FIGURE 14

one can readily see that for a sharp decreasing surface state density with thickness, an increase in V_{oc} will result. The decrease in V_{oc} after 1.4 nm is quite slow and can be attributed from Singh's theory to an increase in oxide resistance. Indeed a variation of .02 V is observed between 1.4 and 1.8 nm in the theory and around .025 V in our experimental measurements for the same range.

Variation of V_{oc} with N_{ss} and Q_{ss}

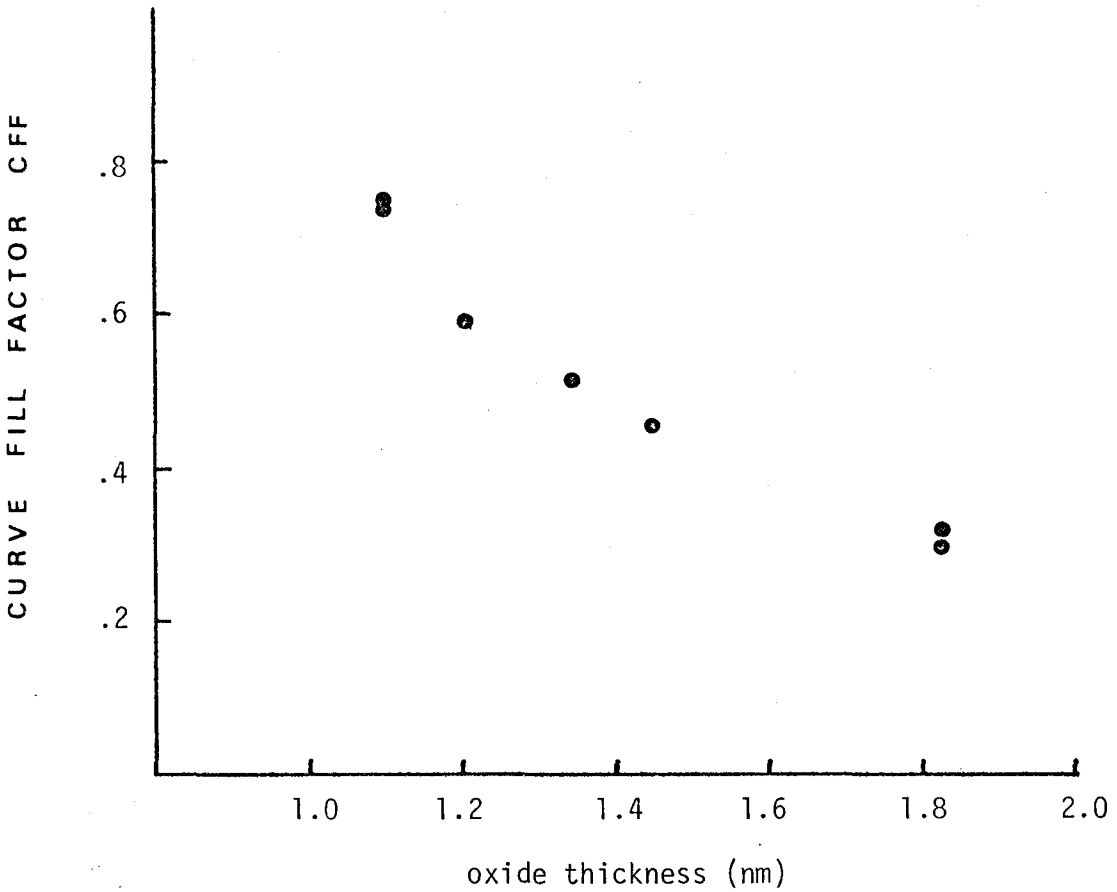
N_{ss} ($m^{-2}eV^{-1}$)	Q_{ss} (m^{-2})	V_{oc} (volt)
2.35×10^{11}	1.0×10^{12}	.706
2.35×10^{14}	5.0×10^{15}	.656
2.35×10^{15}	5.0×10^{16}	.640

$N_A = 8 \times 10^{23} cm^{-3}$, $\tau = 10^{-5}$ sec, d = 1.1 nm.

iii) Curve Factor CFF

The curve factors of the thin oxide cells (d < 1.4 nm) have been very high and for one cell was found to be .81. The high CFF is an indication that contact resistance does not play an important role in reducing the current because a high interval resistance always yields a low CFF. Contrary to theory, there is an extremely fast decrease in CFF with oxide thickness (Fig. 15).

The fast decrease has not yet been explained in terms of the MIS theory but a log log plot of CFF vs d gives a straight line which indicates a high power law dependence with the exponent - 1.78.



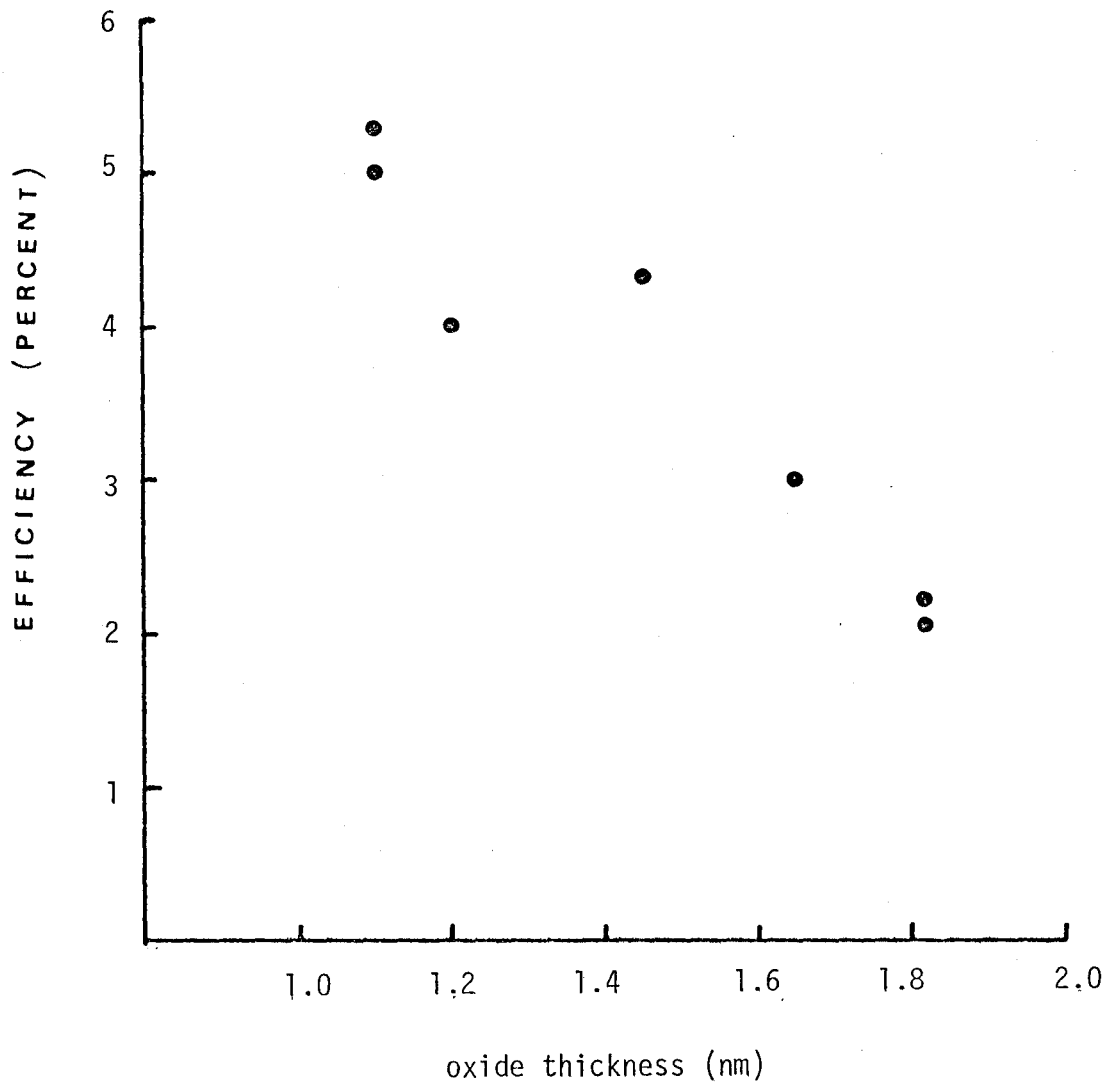
Curve fill factor vs oxide thickness

FIGURE 15

$$CFF = A\, d^{-1.78} = \frac{A}{d^{1.78}} \quad , \quad A = \text{constant}$$

iv) Efficiency

Since the short circuit current density and open circuit do not vary much with thickness in the range of interest, the efficiency will then practically follow the curve factor (Fig. 16). The increase in V_{oc} between 1.1 and 1.4 nm does not suffice to counteract the effect of CFF. A maximum efficiency of 7.0% was obtained without the use of an anti reflexion coating.



Efficiency vs oxide thickness

FIGURE 16

V CONCLUSION

We have showed that MIS solar cells exhibit very high curve fill factors and open circuit voltages. The addition of an interfacial layer to the usual Schottky structure induces major improvements in the ideal diode characteristic, particularly the ideality factor and the barrier height. Ellipsometric measurements revealed that this insulating interfacial layer possessed a different dielectric constant than the expected value of 1.45 for SiO_2. Along with the thickness dependence curve of the open circuit voltage, these results lead us to conclude that below 1.4 nm, the oxide is composed in majority of SiO_1 leaving numerous dangling Si bonds. In fact, this indicates that the surface state density is thickness dependent for those ultra thin oxide and that for thicker oxide, the dependence weakens. The MIS tunnel solar cell theory should then be adjusted to include those important variations. As preliminary calculation demonstrated, the inclusion of a thickness dependent surface state density could account for the maximum in the voltage thickness curve. Further calculations are needed to see the effects on curve fill factors and short-circuit current density. Improvements in the collection efficiency are needed in order to be able to reduce the thickness of the first layer of Al which absorbs and reflects 30% of the incoming light. If the current is brought to 30 ma/cm^2 for AM 1 and if we take the measured values for V_{oc} and CFF respectively .61 volts and .81, the efficiency of the cell is increased to 15%. It was also shown that beaker oxide diodes exhibits even better qualities than the vapor ones. Fabrication permits, with

such diodes, an anneal of the oxide simultaneously with the sintering of the back contact thus simplifying fabrication procedures and applicability to mass production.

The MIS tunnel cell thus shows a large increase in open circuit voltage and curve fill factor which should fully justify the need for further studies. And with the advent of transparent conductors (as tin oxide), the possibility of increasing J_{sc} by 30% is very likely to occur soon and the fabrication of a 15% MIS silicon cell is in sight.

REFERENCES

1. R.F. McQuat and W.L. Pulfrey, J. Appl. Phys. 47, 2113, 1976.
2. A.S. Grove et al, J. Appl. Phys. 33, 2458, 1964.
3. M. Peckerar, H.C. Lin and R.L. Kocher, Proceedings of the Inter. Electron Devices Conf., Dec. 1975, Washington, D.C., p. 213.
4. R. Singh and J. Shewchun, Proceedings of the Electrochemical Society Meeting, Washington, D.C.
5. S.M. Sze, Physics of Semiconductor Devices, John Wiley & Sons, Inc., N.Y., 1969.
6. M.B. Prince, J. Appl. Phys. 26, 534, 1975.
7. S. Kar and W.E. Dohlke, Sol. State Electron. 15, 869, 1972.
8. M.A. Green, J. Shewchun and F.O. King, Sol. State Elect. 17, 563, 1974.
9. S.J. Fonash, J. Appl. Physics, 46, 1286.
10. S.M. Sze, Physics of Semiconductor Devices, Chapter 8, John Wiley & Sons, Inc., N.Y. 1969.
11. F.G. Allen and G.W. Gobeli, Phys. Rev. 127, 150, 1962.
12. E.H. Nicollian and A. Goetzberger, Bell Syst. Tech. J. 46, 1055, 1967.
13. R.C. Henderson, J. Electrochem. Soc. 119, 772, 1972.
14. R.E. Oakley and C.A. Godber, Thin Solid Films 9, 287, 1976.
15. F.L. McCrakin, NBS Technica Note 479, April 1969.
16. E.J. Charlson and J.C. Lien, J. Appl. Phys. 46, 3982, 1975.
17. J.R. Black, NBS Special Publication #337, p. 398, US G.P.O., Washington, D.C., 1970.

18. K. Yass and H.B. Curtis, NASA Technical Memorandum, NASA TM X-3059, Washington, D.C., June 1974.

19. S.T. Raider and R. Flitisch, J. Vac. Sci. Technol. 13, 59, 1976.

20. M.A. Green and J. Shewchun, J. Appl. Phys. 46, 5185, 1975.

21. J. Shewchun, M.A. Green and F.O. King, Sol. State Elect. 17, 563, 1975.

22. A.G. Revesz, Phys. Stat. Sol . 19, 193, 1967.

23. P.V. Gray, Appl. Phys. Lett. 8, 31, 1966.

24. D.R. Lollington and W.G. Townsend, Appl. Phys. Lett. 28, 97, 1976.
A.H.M. Kipperman and M.H. Omar, App. Phys. Lett. 20, 620, 1976.
E.J. Charlson and J.C. Lien, J. Appl. Phys. 46, 3982, 1975.
S.J. Fonash, J. Appl. Physics, 46, 1286, 1975.

25. R. Singh, private communication.