A STUDY OF EVAPORATED THIN-FILM DEVICES

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By

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SCOPE AND CONTENTS:

The deposition techniques for evaporated conducting, semi-conducting, and insulating thin films were investigated. Thin-film resistors, diodes, and transistors were constructed on insulating substrates. The electrical evaluation of these devices was carried out with emphasis on circuit performance for the possible incorporation of such units into thin-film integrated circuits. Difficulties encountered in the fabrication and evaluation of thin-film components have been discussed with special note to the operation of thin-film transistors.

ABSTRACT

The deposition parameters of thin vacuum-evaporated films were studied in the development of thin-film devices. These devices, including resistors, diodes and transistors, were constructed by the use of vacuum deposition techniques and metal masks for pattern generation.

Stable thin-film resistors were fabricated using nichrome as the resistance material. The variation of resistance value with both temperature and time was investigated.

A metal-cadmium sulphide-metal structure was employed as a thin-film diode, the electrodes being of aluminium or gold. The electrical evaluation of such a device demonstrated the importance of the deposition of the semiconductor on the rectifying properties. Forward to reverse resistance ratios of 10^5 were observed for experimental units.

The staggered-electrode structure was incorporated in the production of thin-film transistors. Cadmium sulphide was used as the semiconducting material while silicon monoxide and aluminium were used as the insulator and electrodes respectively. Operating devices exhibiting good saturation characteristics has transconductances of 450μ mhos. Simple circuits were constructed to demonstrate the performance of thin-film transistors.

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TABLE OF CONTENTS

		PAGE
CHAPTER I:	INTRODUCTION	1
1.1	Introduction	1
1.2	Scope of This Thesis	3
	(a) Thin-Film Resistor	3
	(b) Thin-Film Diodes	3
	(c) Thin-Film Transistors	4
CHAPTER II:	THEORY	5
2.1	Single Crystal CdS Diodes	5
2.2	Historical Review of Thin-Film Diodes	10
2.3	Operation of Thin-Film CdS Diodes	10
2.4	Historical Review of Thin-Film Transistors	14
2.5	Operation of Thin-Film Transistors	16
CHAPTER III:	FABRICATION PROCEDURES	22
3.1	Vacuum-Coating Unit	22
3.2	Microcircuit Jig Assembly	23
3.3	Film-Thickness Monitor	24
3.4	Substrate Assembly and Preparation	28
3.5	Mask Preparation	28
3.6	Film Deposition Techniques	33
	(a) Gold	33
	(b) Silver	34

PAGE

(c) Aluminium-- 34

(d) Nichrome--- 34

(e) Silicon Monoxide--------------------------------- 34

(f) Aluminium Oxide---------------------------------- 35

(g) Cadmium Sulphide--------------------------------- 35

3.7 Preparation of Devices--------------------------------- 38

(a) Thin-Film Resistors------------------------------ 38

(b) Thin-Film Diodes--------------------------------- 38

(c) Thin-Film Transistors---------------------------- 40

CHAPTER IV: RESULTS-- 42

4.1 Thin-Film Resistors------------------------------------ 42

4.2 Thin-Film Diodes--------------------------------------- 43

(a) Formation of Rectifying Barriers----------------- 43

(b) Capacitance Measurements------------------------- 48

(c) Forward Bias------------------------------------- 50

(d) Reverse Bias------------------------------------- 52

(e) Temperature Dependence--------------------------- 52

(f) Space-Charge Limited Currents-------------------- 54

(g) Summary-- 58

4.3 Thin-Film Transistors---------------------------------- 59

4.4 Thin-Film Transistor Applications---------------------- 64

CHAPTER V: CONCLUSIONS AND RECOMMENDATIONS------------------- 66

BIBLIOGRAPHY--- 69

LIST OF FIGURES

FIGURE		PAGE
2-1	Energy Band Diagram for Single Crystal Au-CdS-In Diode-------	5
2-2	Energy Level Diagram for n-type Semiconductor in the Presence of Acceptor-like Surface States--------------------	12
2-3	Ohmic Contact to n-type Semiconductor----------------------	12
2-4	Electrode Structure for Thin-Film Transistors---------------	15
2-5	TFT Modes of Operation--	16
2-6	Representation of Thin-Film Transistor----------------------	17
2-7	Theoretical Characteristic Curves of the TFT----------------	20
3-1	Quartz Crystal Oscillator-------------------------------------	25
3-2	Thickness-Monitor Calibration Curve-------------------------	27
3-3	Mask Blank--	29
3-4	Resistor Masks--	30
3-5	Diode Masks---	31
3-6	Transistor Masks--	32
3-7	Insulator I-V Curves--	36
3-8	Complete Thin-Film Devices----------------------------------	39
4-1	Diodes--	45
4-2	Capacitance Measurements------------------------------------	49
4-3	Forward Bias I-V Curve (Diode)------------------------------	51
4-4	Reverse Bias I-V Curve (Diode)------------------------------	53
4-5	Forward Bias Pulse Measurements (Diode)---------------------	55

PAGE

4-6 Forward Bias SCLC (Diode) ---------- 57

4-7 Energy Band Diagram as Evaluated for an Aluminium-Cadmium Sulphide Contact ---------- 58

4-8 TFT Characteristics ---------- 60

4-9 Theoretical TFT Characteristic Curves for Figure 4-8(a) ---------- 62

4-10 Thin-Film Transistor Amplifier ---------- 65

CHAPTER I

INTRODUCTION

1.1 INTRODUCTION:

A thin film circuit is an electronic circuit whose functional elements and interconnections consist of thin solid films. From the earliest days of printed circuits, attempts have been made to print the components as well as conductors. The motivation was, and still is, to reduce the number of electrical connections which have to be made in constructing a given electronic circuit. This is desirable because assembled joints are relatively expensive to make, and are a potential source of failure.

Thin films can be deposited on a flat insulating sheet, known as a substrate, in many varied ways. The commonest method is that of vacuum evaporation where a heated source material is evaporated in a high-vacuum chamber with subsequent condensation of the vapour atoms on the substrate. This is the method used throughout the experiments described in this thesis. Other methods are; cathode sputtering, surface reaction and catalysis, electrodeposition, anodisation, chemical vapour deposition, and silk screening.

Several techniques are available to determine the pattern of the film deposited on the substrate. Pattern generation may be additive or subtractive. That is to say the shape of a film structure may be defined by limiting the area on which film material is deposited or alternatively,

the entire side of the substrate may first be coated prior to selective-pattern etching. In the principal additive method, a foil mask is inserted between the evaporation source and the substrate. The mask itself is usually in the form of a flat metal sheet which contains apertures corresponding in shape to the desired film patterns. In the principal subtractive method on the other hand, selective etching is usually attained by the use of photo-resist techniques.

Thin film circuits which incorporate only resistors and capacitors are already commercially available. In addition, active thin film devices have been successfully fabricated in small quantities in many laboratories, but problems with stability and reproducibility have delayed the commercial production of these devices.

At present, all integrated circuits contain some type of silicon or germanium active device. In the complete monolithic circuit all components, including resistors and capacitors, are produced by the application of diffusion techniques. The extremely poor tolerance of the passive elements in such units, however, largely restricts their application to that of the digital field. Hybrid circuits, containing thin-film passive elements and silicon active elements, cover the field of linear circuits. Not until the device problems associated with the thin-film transistor are solved, however, will complete thin-film integrated circuits become available.

This thesis is concerned with a study of the fabrication and circuit behaviour of certain specific active and passive thin-film components, as may be applied to integrated circuitry. Such component structures as were examined are detailed below.

1.2 SCOPE OF THIS THESIS:

(a) Thin-Film Resistors:

In this thesis, we are interested in developing techniques for the vacuum deposition of thin-film circuit components. In the case of resistors, nichrome was chosen as the resistance material because of its relatively high resistivity and ease of evaporation. Measurements made on the stability of these resistors over a period of ten months showed that there was no drift of resistance value with time. In addition, the temperature coefficient of resistance measured for various resistors was found to be 0.012% per ^{o}C.

(b) Thin-Film Diodes:

A study of the fabrication and characteristics of thin-film diodes was carried out to produce devices capable of useful circuit functions. Such fabrications were in the form of metal-semiconductor-metal sandwiches.

Cadmium sulphide (CdS) was chosen as the semiconducting material for the following reasons. It can be evaporated by resistance-heating of the bulk material, but care must be taken to preserve the stoichiometry of the resultant evaporated film which may otherwise be sulphur deficient. Again, since only n-type conductivity is observed in CdS, problems associated with minority-carrier lifetimes should not arise. Although such evaporated films are not of extremely high purity the presence of a high defect density reduces the carrier concentration so that high-resistivity films may be obtained. Finally, and in connection with space-charge currents, it may be stated that in order to support space-charge limited currents, a material should, in general, have high resistivity, permittivity, and mobility[1]. Although CdS evaporated films exhibit a low carrier mobility,

measurements on such films indicate that space-charge conduction characteristics may still be realized. In certain instances, the application of such characteristics may be of importance in circuit design.

(c) Thin-Film Transistors:

A complete evaporation-masking system was developed in studies as applied to the fabrication techniques for, and the electrical characteristics of, thin-film transistors. The basic transistor structure employed was a modification of that used originally by Weimer[2].

Cadmium sulphide was again employed as the semiconducting material; while silicon monoxide and aluminium were employed in the fabrication of the insulator and electrodes, respectively.

Thin-film transistors were incorporated into a simple amplifier to study the device under working conditions and to see if possible integrated circuits are feasible using the TFT. A voltage gain of 4 was observed when a transistor with a transconductance of 400 μ mhos was employed as the amplifying device.

The field effect model developed by Borkan and Weimer[3] was used to analyse the theoretical behaviour of the experimental thin-film transistors.

CHAPTER II

THEORY

2.1 SINGLE CRYSTAL CdS DIODES:

Extensive work has been carried out by other investigators on studies of cadmium-sulphide diodes employing single-crystal semiconductor material[1,4,5]. High resistivity single-crystal specimens of CdS can be grown from electronic grade powder. Electron injecting contacts to the crystal may typically be made by the application of an evaporated indium layer, while a blocking contact may also be provided by the application of an evaporated film such as gold. A postulated energy level scheme for such a fabrication is as shown in Figure 2-1, below.

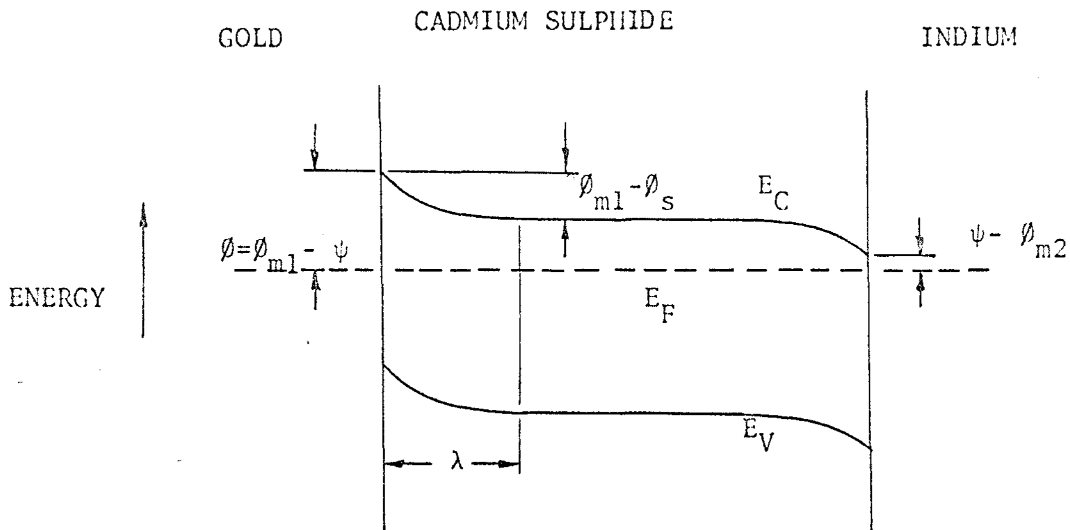


FIGURE 2-1: ENERGY BAND DIAGRAM FOR SINGLE CRYSTAL Au-CdS-In DIODE

where ψ = electron affinity of semiconductor

ϕ_s = work function of semiconductor

ϕ_{m1} = work function of gold

ϕ_{m2} = work function of indium

λ = thickness of depletion layer

$\phi = \phi_{m1} - \psi$

$V_D = \phi_{m1} - \phi_s$

The principle of diode rectification by a potential barrier at a contact can be readily understood by reference to the barrier profile shown in Figure 2-1. In the absence of an external voltage, the electrons in the metals are in dynamic equilibrium with those in the semiconductor. The probability of an electron crossing the rectifying barrier depends on the number of electrons which have energies in excess of ϕ, where $\phi = \phi_{m1} - \psi$, and are moving in the correct direction. Under this equilibrium condition, the net current is zero. If the n-type semiconductor is now given a positive potential with respect to the metal, the probability of an electron transition from the metal is still governed by $\exp(-\phi/kT)$ and is therefore unchanged. On the other hand, the probability of an electron transition into the metal from the semiconductor is diminished by an amount in proportion to the change in the Boltzmann parameter $\exp[-q(V_D + V)/kT]$. The equilibrium thus destroyed results in a small net current flow between metal and semiconductor. On the other hand, if the semiconductor is made negative with respect to the metal, the probability of an electron transfer from the conduction band of the semiconductor into the metal is greatly increased. Since the rate

at which electrons cross the barrier in the opposite direction again remains unchanged, the result of this imbalance is evidenced in the form of a large forward net-current flow.

For a development of the simple isothermal diode characteristic the reader is referred to the analysis of Henisch[6], which yields the following expression for net-current flow, namely,

$$J = J_o \left(e^{\frac{qV}{KT}} - 1 \right) \quad \text{....(2-1)}$$

$$J_o = \frac{4\pi \, m_n^* \, q \, k^2 T^2 \, e^{-\frac{q\emptyset}{kT}}}{h^3} \quad \text{....(2-2)}$$

where,

J = current density

J_o = reverse saturation current

k = Boltzmann constant

T = temperature

m_n^* = effective mass of electron

h = Planck's constant

q = electronic charge

The existence of a predicted Schottky type barrier[4] may be inferred from capacitance-voltage measurements on the above devices and also from current-voltage measurements. It is to be noted, however, that the exponential I-V relationship as given in Equation (2-1) above is derived from considerations of the thermal diffusion of electrons over the rectifying barrier under the influence of small applied potentials. For larger applied voltages, however, the controlling effect of the

Schottky type barrier will be replaced by one of space-charge limitations which results in the dominance of a square law characteristic of the form[7]

$$J = \frac{9 \mu \varepsilon \theta V^2}{8d^3} \qquad \text{....(2-3)}$$

where
- μ = carrier mobility
- d = thickness of crystal
- ε = permittivity of crystal
- V = applied voltage
- θ = ratio of free to trapped charge in the crystal

This square law dependence is characteristic of semiconductor crystals such as CdS in which defects are absent or inactive. In CdS this situation may be achieved by compensation of deep-lying trap levels with shallow donor levels[4].

When a small reverse bias is applied to the diode fabrication, the Schottky barrier extends deeper into the crystal, accompanied by an increase of the electric field in the barrier region. At higher reverse voltages the image forces produce sufficient lowering of the barrier for significant emission of electrons into the crystal to occur[6]. For this reason the reverse current does not saturate at a given value but rather keeps slowly increasing with bias until breakdown ensues. The associated reduction in barrier height is given by[4]

$$\Delta\phi = \left[\frac{qE_c}{4\pi\varepsilon} \right]^{\frac{1}{2}} \qquad \text{....(2-4)}$$

and

$$E_c = \left[\frac{2q\ Nd\ (V + V_D)}{\varepsilon} \right]^{\frac{1}{2}} \qquad \text{....(2-5)}$$

where E_c = contact field

N_d = number of donor atoms

Thus, for the condition V >> kT/q in the reverse-bias situation, the expression for current density becomes[6],

$$J = \frac{4\pi\, m_n^*\, q\, k^2T^2}{h^3}\, e^{-\frac{q}{kT}(\emptyset - \Delta\emptyset)} \qquad \ldots.(2\text{-}6)$$

which may be reduced, by substitution of (2-2) and 2-4), to the form,

$$J = J_o \exp \frac{q}{kT}\left[\frac{q^3 N_d \quad (V + V_D)}{8\pi^2 \varepsilon^3}\right]^{\frac{1}{4}} \qquad \ldots.(2\text{-}7)$$

A relationship for the magnitude of the incremental capacitance of a uniformly -doped semiconductor diode of the above type may be found in the expression[4]

$$C = A\left[\frac{q\ \varepsilon\ N_d}{2(V + V_D)}\right]^{\frac{1}{2}} \qquad \ldots.(2\text{-}8)$$

where C = capacitance

A = junction area

V = reverse applied voltage

The application of this relationship in the form of a $1/C^2$ - V plot thus permits an evaluation of the magnitude of the parameters N_d and V_D. Further, an expression for the thickness of the depletion layer can also be obtained form the solution of Laplace's equation for a metal-semiconductor contact[4], namely,

$$\lambda = \left[\frac{2\ \varepsilon\ (V + V_D)}{q\ N_d}\right]^{\frac{1}{2}} \qquad \ldots.(2\text{-}9)$$

2.2 HISTORICAL REVIEW OF THIN-FILM DIODES:

The results of a number of studies of thin-film diode structures, employing CdS, have been reported in the literature by various investigators[8,9,10,11,12]. In all such cases reported a metal-semiconductor-metal sandwich was used, in which thickness of the CdS semiconductor was in the range 1 - 30 μ. A blocking contact was established by the use of metals, such as gold or tellurium, which have higher work functions than CdS. Hence, a Schottky barrier could be formed even in the absence of surfact states. An ohmic or electron injecting contact was provided by evaporating a low work-function metal such as indium or aluminium as the second electrode.

Zuleeg[9] has shown that the equations relating to single-crystal CdS diode behaviour may also be applied to thin-film diodes, thus demonstrating that a Schottky barrier may indeed exist in such a thin-film structure. Pulse-response measurements show a square-law dependence of current on voltage for large forward-bias voltages, when the diode current becomes space-charge-limited rather than diffusion limited. Measurements of electron mobility in CdS films[11] indicate a much lower mobility than that observed in single crystal material. The electron mobility of a CdS film ranges from 1 - 30 cm^2/V - sec., depending on the preparation of the film, in contrast to a bulk electron mobility value of 200 cm^2/V - sec. This is to be expected of course, since boundary scattering and defects will reduce the electron mobility in thin films of a polycrystalline material.

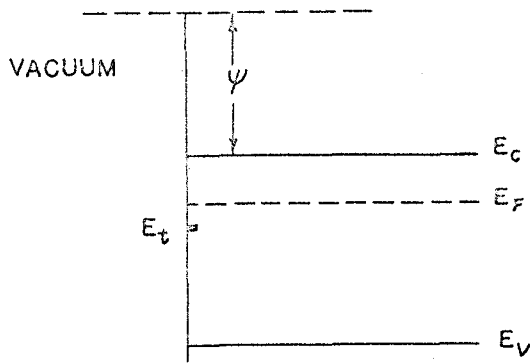
2.3 OPERATION OF THIN-FILM CdS DIODES:

Because of the difficulty in preparing consistent thin films of CdS the rectifying properties of ......

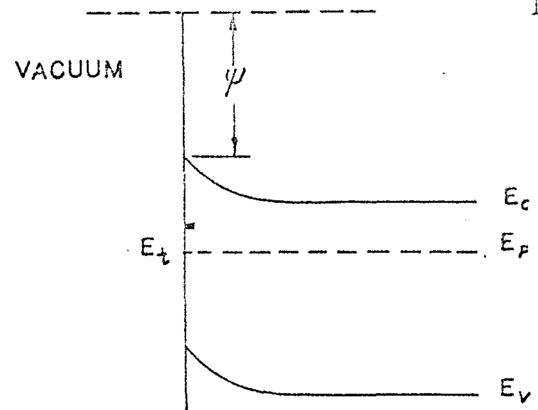
a thin film diode structure may be due to inhomogeneities in the semi-conducting film, rather than the work function of the electrodes used.

At a semiconductor-vacuum interface with a semiconductor containing no surface states, the energy bands of the semiconductor at thermal equilibrium would continue at constant energy levels right up to the surface. However, if acceptor-like surface states are introduced at an energy level below the Fermi level of an n-type semiconductor as shown in Figure 2-2(a), they will not be in equilibrium with the energy bands as long as they remain unoccupied. Since the states below the Fermi level cannot remain totally empty, some of the electrons from the conduction band will fall into them. The surface becomes negatively-charged while a positive space-charge layer forms beneath, causing the energy bands at the surface to bend upwards with respect to the Fermi level as shown in Figure 2-2(b). The amount of band bending is determined by the requirement that overall charge neutrality prevails. The larger the surface-state density, the higher will be the bending of the energy bands at the surface.

If a metal-semiconductor contact is made with such a semiconductor surface, the energy bands at the surface of the semiconductor will be bent before any contact is made. When thermal equilibrium is established and the two Fermi levels coincide, the energy bands of the semiconductor will bend only slightly, depending on the work function of the metal. The height of the potential barrier will be determined by the normal space-charge of the free semiconductor and by the work function of the metal[13]. This means that a gold electrode with a larger work function than CdS would create a higher barrier in the presence of surface states than it

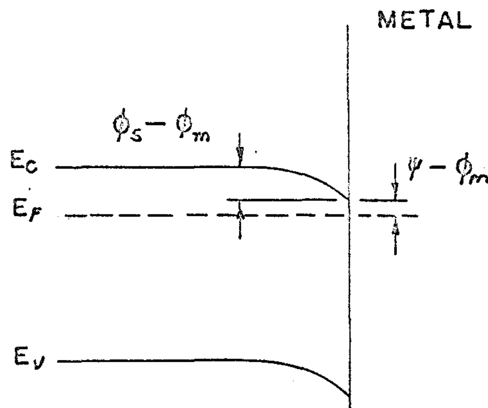


(A) CONDITION FOLLOWING INTRODUCTION OF SURFACE STATES

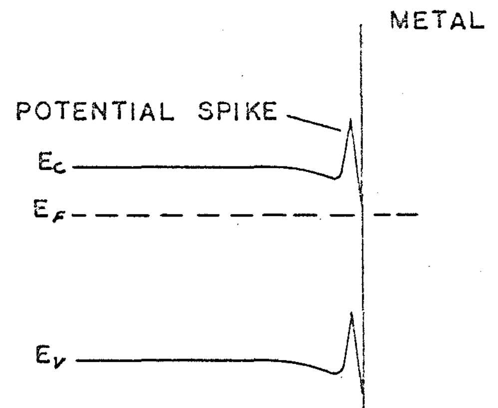


(B) AT THERMAL EQUILIBRIUM

FIG. 2-2 ENERGY LEVEL DIAGRAM FOR N-TYPE SEMICONDUCTOR IN THE PRESENCE OF ACCEPTOR-LIKE SURFACE STATES



(A) WORK FUNCTION OF SEMI-CONDUCTOR > WORK FUNCTION OF METAL



(B) SURFACE HIGHLY DOPED N-TYPE

FIG 2-3 OHMIC CONTACT TO N-TYPE SEMICONDUCTOR

would without. Aluminium, having a work function lower than cadmium sulphide, is normally found to produce an ohmic contact. However, if surface states are present in the CdS film a rectifying barrier already exists and the effect of an aluminium electrode would be to lower the barrier height slightly. Thus we see that the work function of the metal electrode is not the only criterion for the formation of a Schottky barrier.

One method of obtaining an ohmic contact to an n-type semiconductor is to use a metal with a lower work function than that of the n-type semiconductor in question. A contact of this kind causes the lower edge of the conduction band at the surface of the semiconductor to approach the Fermi level of the metal as shown in Figure 2-3(a). Carriers move into the semiconductor by thermal injection. Some workers[5] have explained the injection mechanism by assuming the surface to be of a highly doped n-type nature as exemplified in Figure 2-3(b). In this example the electrode has a work function larger than that of the semiconductor. Charge is transferred from the heavily doped n-type semiconductor to the metal until the Fermi levels are coincident. A narrow potential spike less than 100 Å wide is produced at the surface of the semiconductor. Electrons enter the semiconductor by a combination of thermal injection and quantum mechanical tunneling.

To date, cadmium sulphide has always been found to be n-type. Dominant conductivity by holes has never been observed even when the material has been intentionally doped with acceptor atoms such as silver or copper[14]. It has been suggested[14] that no hole conduction takes place because of a high acceptor-ionization energy as would be associated with

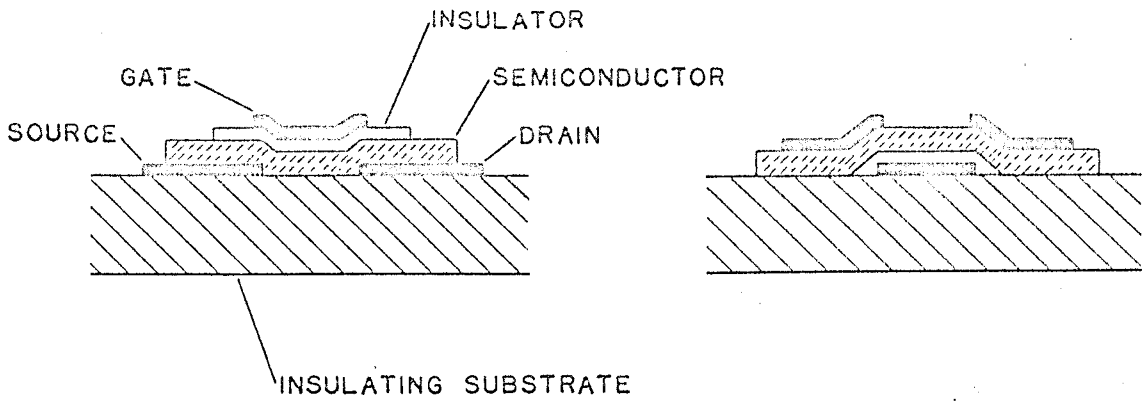
a large hole effective mass. Evaporated CdS films are naturally n-type as excess cadmium will be produced during deposition. CdS tends to dissociate at the temperatures required for evaporation. The difference in vapour pressures of the constituents may also cause the initially deposited film to contain an excess of sulphur resulting in a high resistivity film. At the end of the evaporation the resistivity of the film will decrease as the deposition becomes rich in cadmium. A diode fabricated from a film deposited in this way will not be as sensitive to the work function of the metal electrodes as would a single crystal diode.

2.4 HISTORICAL REVIEW OF THIN-FILM TRANSISTORS:

Oscar Heil[15], in 1935, proposed the first solid-state amplifier based on the use of a space-charge region. This device has since become known as a field-effect transistor. Thin single crystals of cadmium sulphide were used by Ruppel and Smith[16] to construct an "analogue triode". The first really successful device using thin films was built by Weimer[2] in 1961. The practical advantage of Weimer's device was that it could be constructed from polycrystalline thin films that were all vacuum evaporated. Other workers, Haering[17] 1963 and Zuleeg[9] 1963, have also successfully fabricated thin-film transistors using cadmium sulphide.

Cadmium selenide has also been used for thin-film transistors by Shallcross[18] 1963, and De Graaff[19] 1966, while tellurium transistors have been reported by Weimer et al[20].

In these fabrications the source-drain gap dimension is usually in the order of 10 microns, while the width of the channel is in the order of 2 mm. The semiconductor may be as thick as one micron, while the insulator ranges in thickness from 200 - 2000 Å. Successful devices have



(A) (B)

STAGGERED – ELECTRODE STRUCTURE

(C) (D)

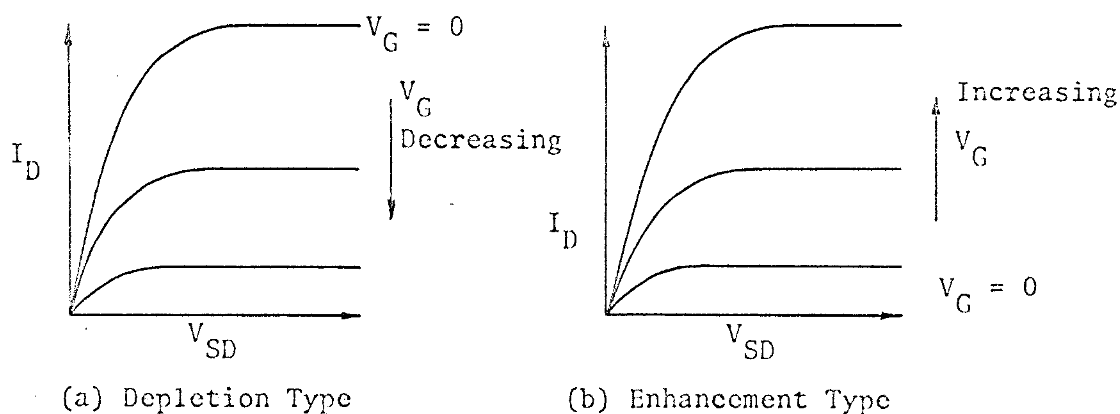
COPLANAR – ELECTRODE STRUCTURE

FIG 2–4 ELECTRODE STRUCTURES FOR THIN-FILM TRANSISTORS

been made using any one of the electrode configurations as illustrated in Figure 2-4. The structure chosen depends greatly on the ease by which ohmic contact can be made to the source-drain regions for the particular materials used.

2.5 OPERATION OF THIN-FILM TRANSISTORS:

Thin-film transistors can be fabricated to operate in either the depletion or enhancement mode, depending on the initial conditions of the channel used. If a high conductance n-type channel is formed when the gate voltage $V_G = 0$, then a negative gate voltage will decrease the conductance of the channel. This is termed a depletion-type device. On the other hand an enhancement type unit exhibits a low-conductance channel when $V_G = 0$ and in this case a positive gate voltage effects an increase in channel conductance. Characteristic curves for these devices are as illustrated in Figure 2-5 below.



(a) Depletion Type (b) Enhancement Type

FIGURE 2-5: TFF MODES OF OPERATION

V_{SD} = source-drain voltage

I_D = drain current

V_G = gate voltage.

Let us now consider a model which may be applied to a description of an enhancement mode transistor, (with minor modifications the results may be applied to the description of a depletion mode device). A simple mathematical model to describe the operation of the thin-film transistor has been developed by Borkan and Weimer[3]. Their development is based on the assumptions that (a) the carrier mobility is invariant with gate voltage, (b) there are no surface states or traps, (c) the semiconductor channel is thin compared to the insulator thickness and (d) only majority carriers are considered. We shall further simplify the development of the above authors by introducing an additional assumption that the initial conductivity of the channel is zero.

Let us now consider a thin-film transistor, as illustrated in Figure 2-6 below, operating in the enhancement mode.

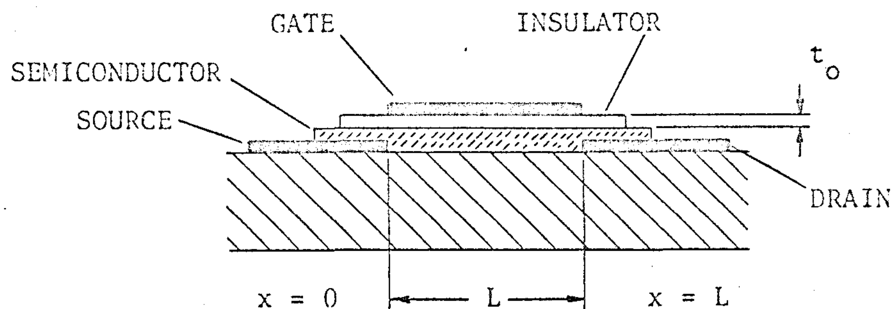


FIGURE 2-6: REPRESENTATION OF THIN-FILM TRANSISTOR

At this point it is convenient to introduce the notation, as listed below, that will be used in the development of an expression for the characteristic curves of such a device.

W = width of channel
L = length of channel
t_o = insulator thickness
t_i = thickness of induced channel
V_G = gate voltage

V_S = source voltage (taken as zero)
V_D = drain voltage
ε_I = permittivity of insulator
E_I = electric field in insulator
E = electric field along the channel
I_D = drain current
N = charge density in the channel
μ = carrier drift mobility

Under the application of some finite applied gate voltage the current in the channel is given by the expression

$$J = q \mu NE \qquad \text{....(2-10)}$$

Further, consider that the potential of the semiconductor at an arbitrary point x, as measured from the source electrode, will be given by V(x). If the charge per unit area induced into the channel by the voltage applied to the gate electrode is

$$Q = \varepsilon_I E_I = \varepsilon_I \left[\frac{V(x) - V_G}{t_o} \right] = q\, Nt_i \qquad \text{....(2-11)}$$

then the charge density in the channel is given by

$$N = \frac{\varepsilon_I}{q\, t_i t_o} [V(x) - V_G] \qquad \text{....(2-12)}$$

on rearrangement of equation (2-11). A further substitution of (2-12) into (2-10) then yields the following expression for current density, namely,

$$J = \frac{\mu\, \varepsilon_I}{t_i t_o} [V_G - V(x)] \frac{dV}{dx} \qquad \text{....(2-13)}$$

If we now integrate the above expression as follows,

$$\int_{o}^{L} J dx = \int_{o}^{V_D} \frac{\mu \, \varepsilon_I}{t_i t_o} \left[V_G - V(x) \right] dV \qquad \ldots .(2\text{-}14)$$

we obtain the following simplified relationship for J

$$J = \frac{\mu \, \varepsilon_I}{t_i t_o L} \left(V_G V_D - \frac{1}{2} V_D^{\,2} \right) \qquad \ldots .(2\text{-}15)$$

Since the drain current I_D is related to current density J by the expression

$$I_D = J t_i \qquad \ldots .(2\text{-}16)$$

then

$$I_D = \frac{\mu \varepsilon_I \, W}{2 \, L \, t_o} \left(2 \, V_G - V_D \right) V_D \qquad \ldots .(2\text{-}17)$$

It is to be noted that equation (2-17) is valid only up to the point where $V_D = V_G$. In this respect, and as indicated in equation (2-11), the charge Q induced at the drain becomes zero in this limit. Thereafter, the drain current is ideally independent of drain voltage. Above this limit, termed the "pinch-off", equation (2-17) simplifies to the relationship

$$I_D = \frac{\mu \, \varepsilon_I \, W \, V_G^{\,2}}{2 \, L \, t_o} \qquad \ldots .(2\text{-}18)$$

Representative characteristics as derived from (2-17) and (2-18) are as illustrated in Figure 2-7 below.

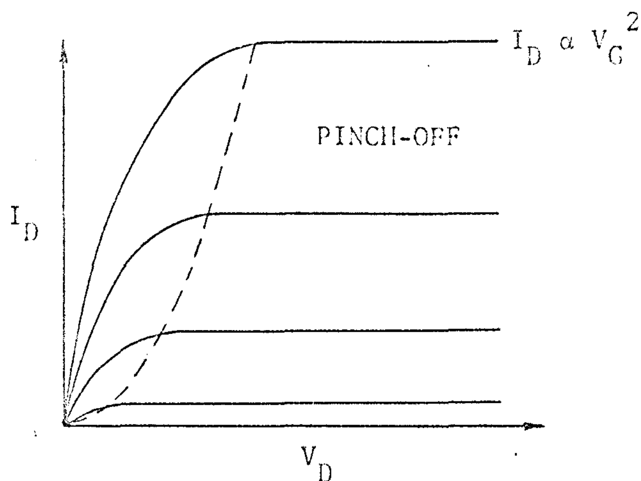


FIGURE 2-7: THEORETICAL CHARACTERISTIC CURVES OF THE TFT

The transconductance, g_m, for such a device operating beyond pinch-off can be obtained from equation (2-18) as follows:

$$g_m = \left(\frac{\partial I_D}{\partial V_G}\right)_{V_D = \text{const}} = \frac{\mu \, \varepsilon_I \, W \, V_G}{L \, t_o} \qquad \ldots.(2\text{-}19)$$

Because of the square-law dependence of drain current on gate voltage, the transconductance is proportional to the square root of drain current.

If initial carriers are present in the channel then equation (2-17) can be modified to:

$$I_D = \frac{\mu \, \varepsilon_I \, W}{L \, t_o} \left[(V_G - V_0) \, V_D - \frac{V_D^2}{2}\right] \qquad \ldots.(2\text{-}20)$$

where

$$V_0 = \frac{t_o N_o q}{\varepsilon \, L \, W} \qquad \ldots.(2\text{-}21)$$

and N_o = total number of initial charges in the semiconductor. Equation (2-20) is the resultant expression obtained in Weimer's development. This equation is valid for drain voltages below pinch-off levels,

$$V_{D\ KNEE} = V_G - V_o \qquad \ldots.(2\text{-}22)$$

where $V_{D\ KNEE}$ = drain voltage at the knee of the curve. For a depletion type transistor V_o is negative.

CHAPTER III

FABRICATION PROCEDURES

3.1 VACUUM-COATING UNIT:

All experimental devices investigated in this thesis were constructed in an Edwards High Vacuum 19E2-type coating unit. The standard unit is equipped with a 19-inch stainless-steel bell jar incorporating two glass viewing ports. The bell jar is water-cooled at the welded joints to prevent expansion during bake-out procedures.

The pumping system consists of a 9-inch oil diffusion pump, backed by a 450 litres/min. single-stage rotary pump. An ultimate pressure of 3×10^{-7} torr may be attained after approximately six hours pumping, while a working pressure of 1×10^{-6} torr may be attained in one hour.

Power for resistance heating of filaments is provided by a low-tension transformer, capable of supplying 400 amp. at 10V or 200 amp. at 20V, depending on the transformer taps used. Power regulation is obtained by use of an auto-transformer feeding the low-tension transformer. The same auto-transformer is also used in regulating a high-tension supply and the radiant heater.

A high-tension supply with a 5 KV open circuit voltage is available for substrate cleaning by glow discharge techniques. Further, a radiant heater, located in the top of the bell jar, can be used to bake the system to a temperature of 400° C.

3.2 MICROCIRCUIT JIG ASSEMBLY:

The coating unit contains a microcircuit jig assembly in the bell jar, for complete deposition of devices during one pump down cycle. The jig assembly is supported by a tripod stand, with a 1/4 inch stainless-steel top plate providing an anchor for a mechanism containing two rotating plates. The lower rotating plate in this assembly will carry six masks, (each 2 inch by 2 inch in size), which can be raised into close contact with the substrate assembly during evaporation. The upper plate is a circular substrate magazine incorporating six substrate positions which can rotate about a central axis. During a mask change the mask carriage drops approximately 3/4 inch, is then rotated one sixth of a revolution and finally moves up to contact the substrate. After rotating six masks, an interlinked mechanism moves a new substrate on the magazine carrier into position. The masks and substrates are locked into position by means of a Geneva mechanism giving a position accuracy of $\pm$ 0.001 inch.

The top support plate of the jig has three ports: one for loading the substrates and the other two for substrate heaters. The first, a pre-heater, is capable of raising the substrate temperature to 150°C while the main heater is capable of effecting a substrate temperature up to 300°C. Thermocouples are located in the main heater and pre-heater assemblies, to monitor substrate temperatures. A third thermocouple is, in addition, located close to, but is not in physical contact with, the microcircuit assembly.

Provisions are also made for monitoring the resistance of a film during deposition. To achieve this, an external resistance measuring

meter may be connected to a subsidiary monitor film laid down during the evaporation cycle. Connections to this film are made through metal contacts located on three of the six mask holders.

A high frequency quartz crystal used in a film-thickness monitor - as will be described in Section 3.3 - is mounted on the top of the jig, close to the substrate coating position and normal to the vapour stream. The crystal is shielded from radiant heat in the unit with the aid of a series of three baffles, so that temperature changes in the system do not affect the crystal frequency appreciably.

The required film is evaporated from one of six vapour sources on an indexed turret head located under the mask. A mechanical shutter is mounted over the turret so that a source may be heated up and outgassed without contaminating the substrate with undesirable depositions.

3.3 FILM-THICKNESS MONITOR:

Measurements of film thickness were carried out with the aid of a quartz-crystal oscillator. For such measurements, and at the same time that a film is deposited on a substrate, a film is also deposited on the quartz crystal as described above. The resultant increase in mass of the crystal causes its natural oscillating frequency to decrease. This frequency change is linear with mass change if the variation of mass is small.

The oscillator circuit was mounted just under the baseplate of the coating unit in order to reduce lead capacitance. Such mounting allows for the shortest lead length without the complication of introducing the circuitry into the vacuum system. The oscillator circuit used is as shown in Figure 3-1. The output signal from the oscillator

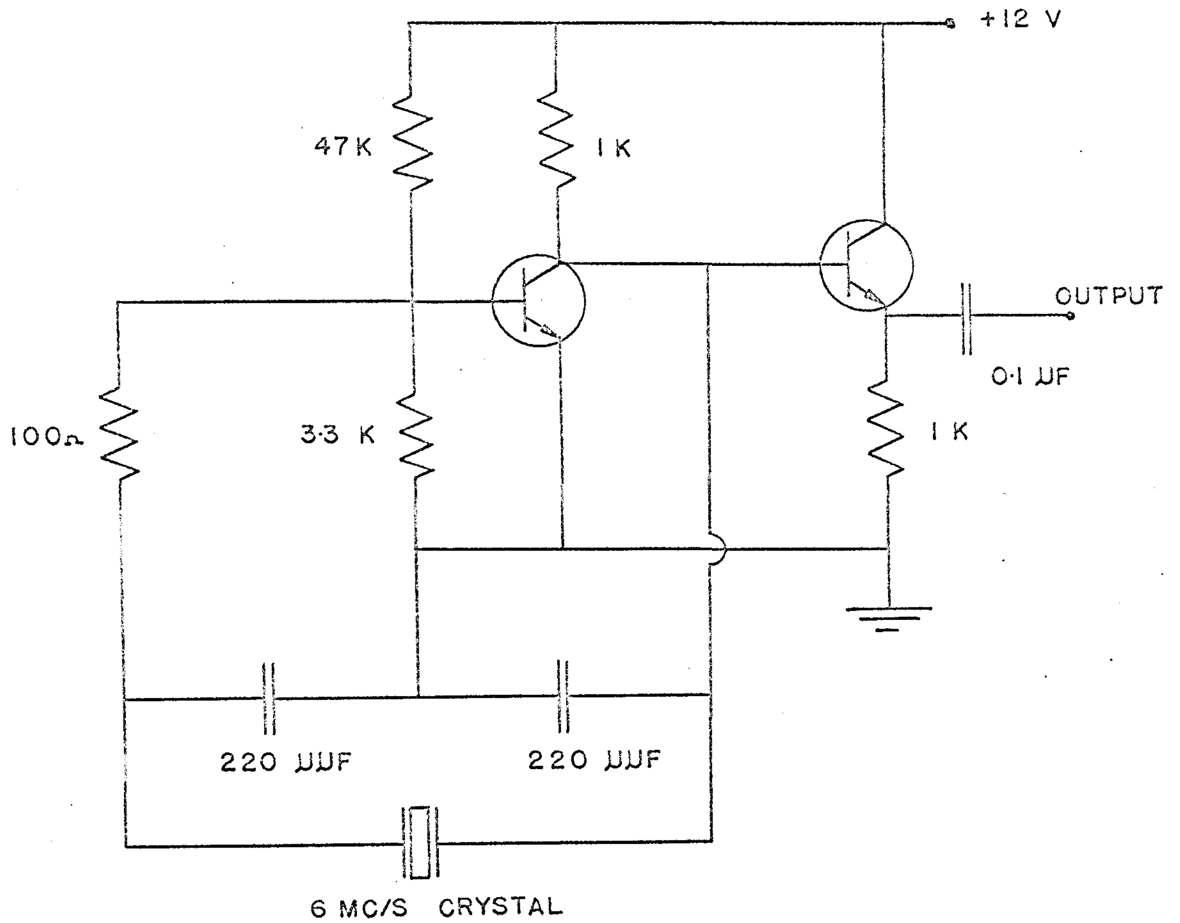


FIG 3-1 QUARTZ CRYSTAL OSCILLATOR

was then fed through a 50 Ω co-axial cable to the frequency counter, (Hewlett Packard type 3734A). Power for the oscillator was supplied by a Harrison Laboratories DC power supply (Model 6200A).

The quartz crystal frequency was calibrated by deposition of five lead films of differing thickness. Glass slides, as will be described in Section 3.4, were used as substrates. The mass of the films was determined by weighing the glass slide before and after deposition. The films were assumed to be thick enough so that the density of the film was the same as that of the bulk material. In this way the thickness of a film could be determined for a given area. A plot of film thickness versus frequency change, from such mass measurements, is as shown in Figure 3-2. From the slope of this curve it was possible to determine an empirical relationship between frequency change and thickness for any bulk density, namely:

$$t = \frac{3.9\ f}{\rho} \qquad \ldots\ldots(3\text{-}1)$$

where
t = film thickness in Å
f = frequency change c/s
ρ = density g/cm^3

This system was sensitive enough to detect a frequency change of 0.1 c/s/s. For a material such as aluminium, this would correspond to a deposition rate of 0.14 Å/sec.

The maximum total frequency change for an initially 6 Mc/s crystal is 200 Kc/s according to the manufacturer's specifications. Above this range the frequency change is no longer linear with the mass change and a new crystal is required.

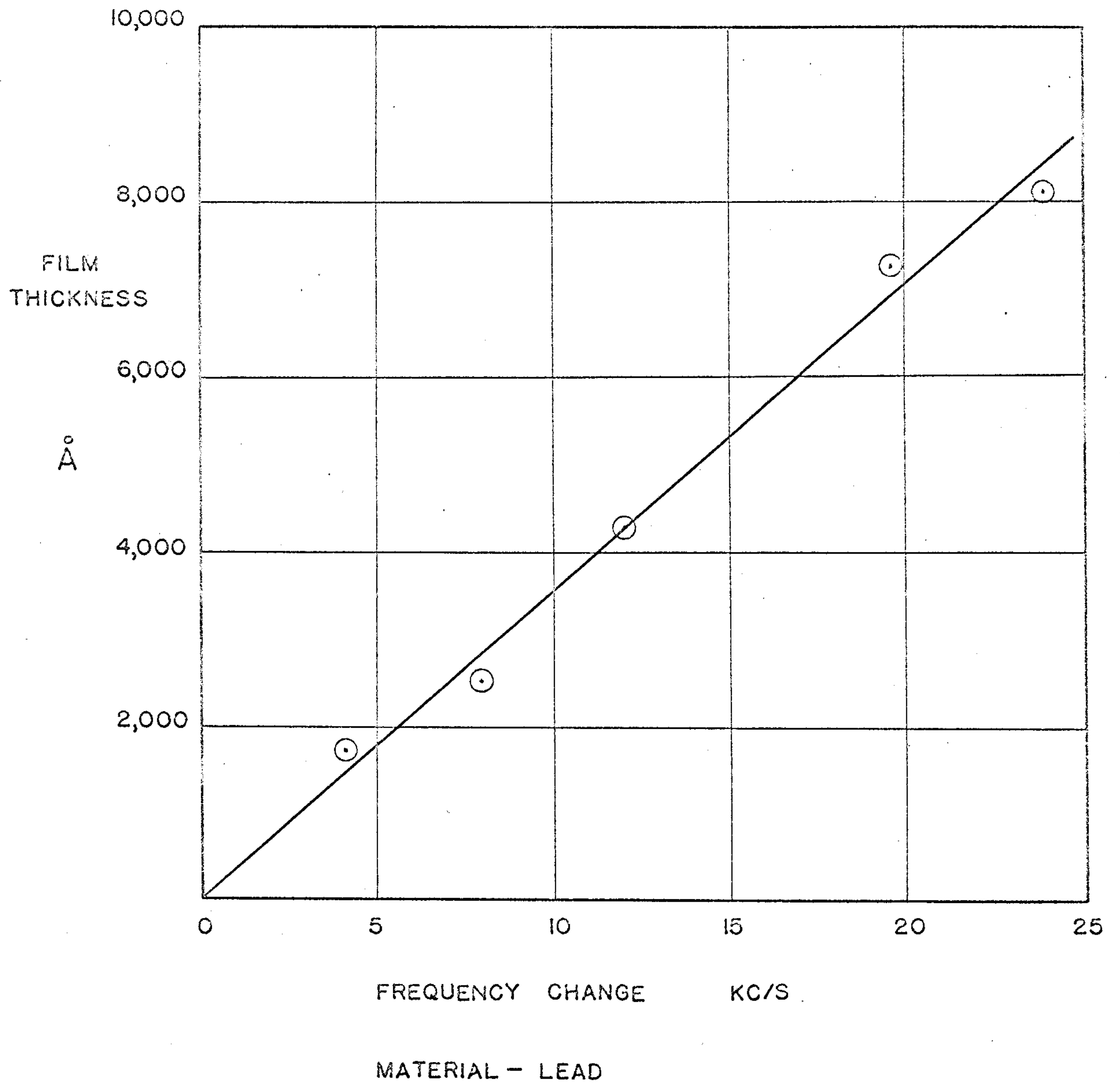


FIG 3-2 THICKNESS-MONITOR CALIBRATION CURVE

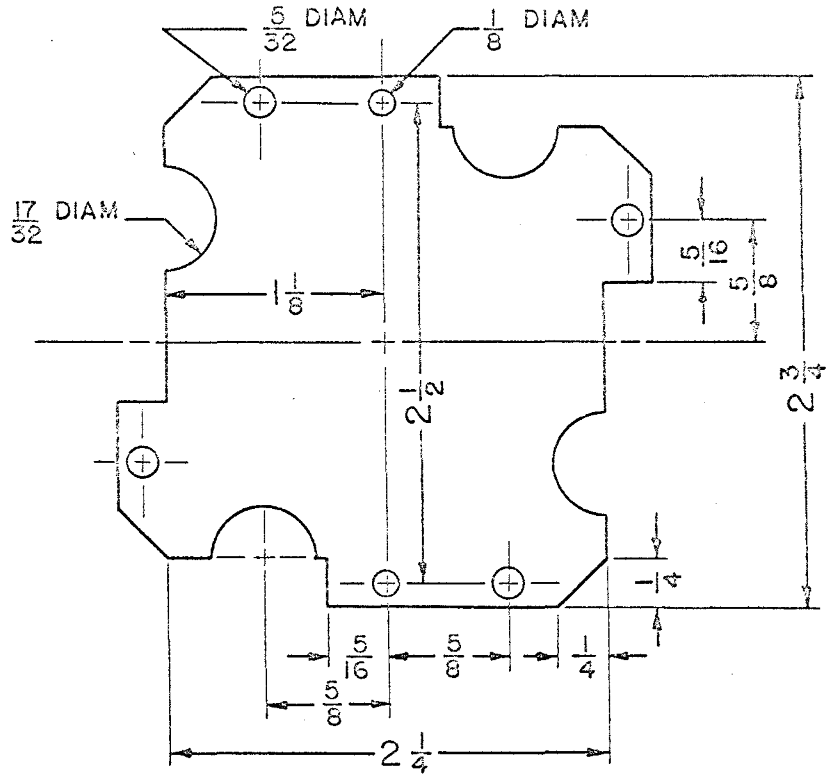
3.4 SUBSTRATE ASSEMBLY AND PREPARATION:

Substrates used in all experiments were cover-glass slides, of dimensions 5 cm by 5 cm by 1 mm thick. In order to maintain good thermal contact with the substrate heaters, the glass slides were clamped to 2 inch by 2 inch by 1/4 inch aluminium spacers that were spring loaded in the substrate magazine to prevent movement. This method assured that the substrates did not move as the different masks were brought into contact.

Care was taken to ensure that the substrates were absolutely clean before films were deposited on them. Batches of glass slides were first outgassed by heating to 200°C in a vacuum of approximately 1 torr for 1 - 2 hrs., and then pumping was continued at room temperature for 24 hrs. As individual substrates were required,both surfaces were washed and rinsed several times with a commercial cleaner. To check whether or not the substrate was grease-free, it was held in a pair of forceps and distilled water sprayed on it. The water covered the substrate in a continuous film if no grease were present. Grease on the substrate would, however, cause spots to appear on the water film. The slide was then rinsed in methyl alcohol, clamped to an aluminium spacer, and allowed to dry. The substrate and spacer were then inserted into the magazine carriage, taking care not to touch the substrate. A final cleaning was done in the vacuum system by a glow discharge over the surface of the substrate, to remove any foreign matter left by the alcohol.

3.5 MASK PREPARATION:

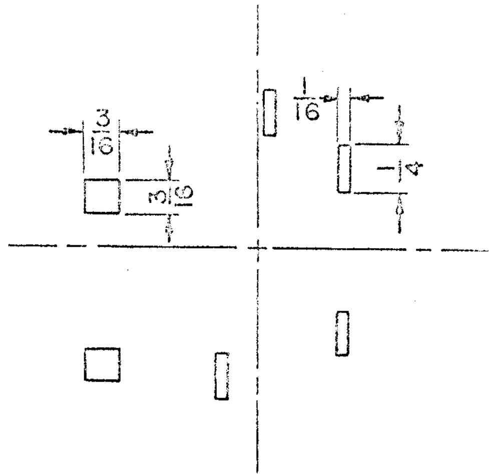
The vacuum deposition of thin-film devices requires the film to be



MATERIAL – 0·005" STAINLESS STEEL OR BRASS

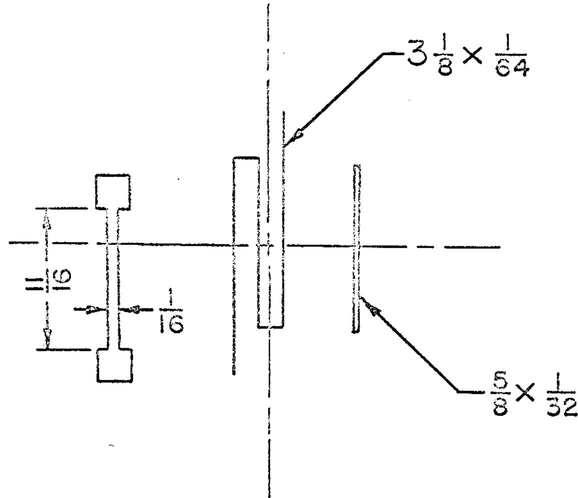
FIG 3–3 MASK BLANK

CONTACTS



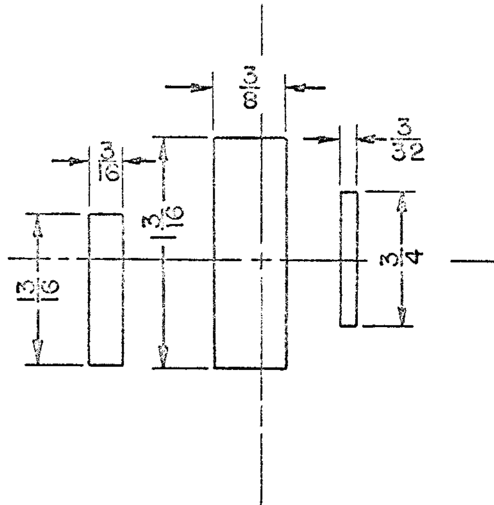
(A)

RESISTOR



(B)

COVER



(C)

FIG 3-4 RESISTOR MASKS

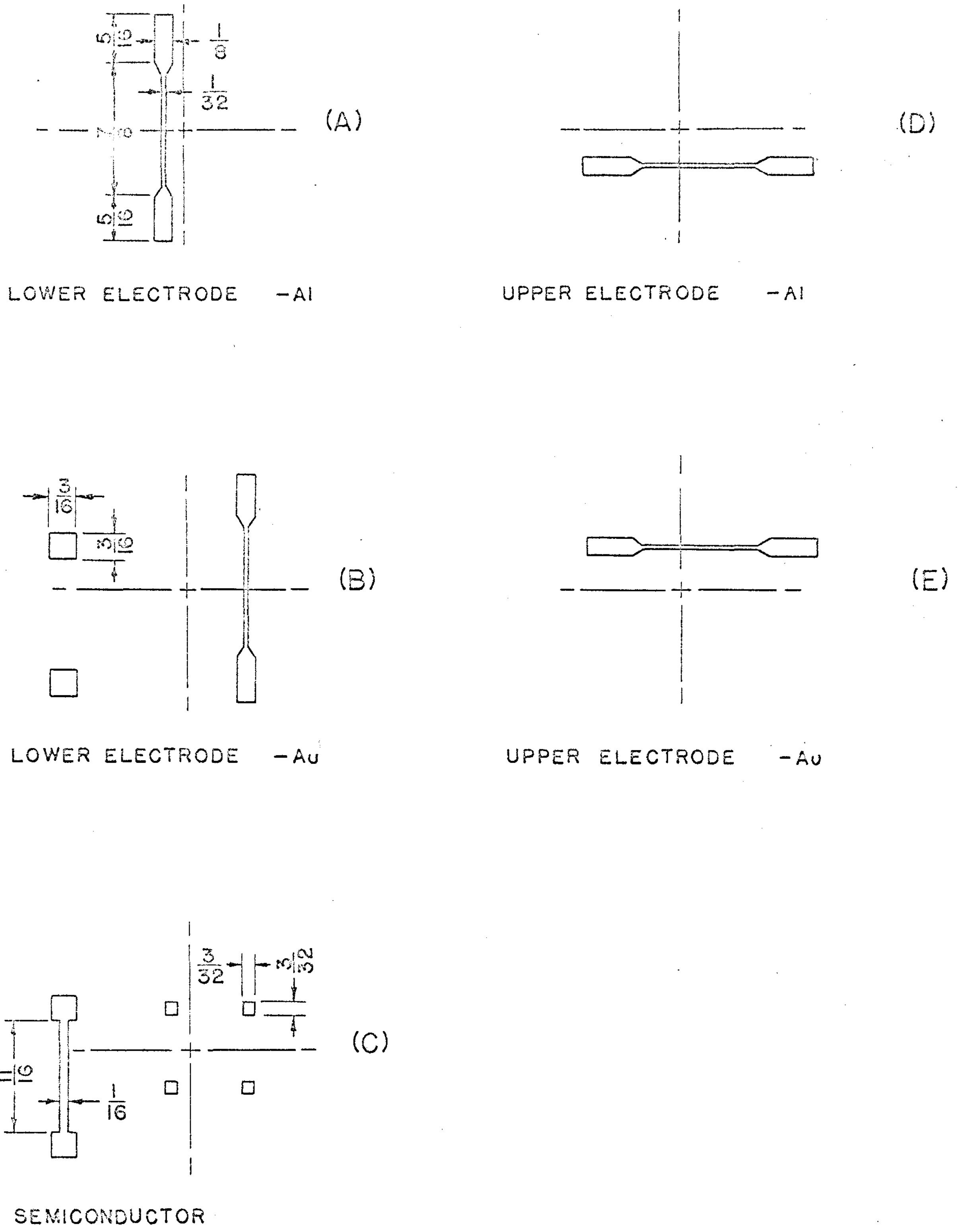
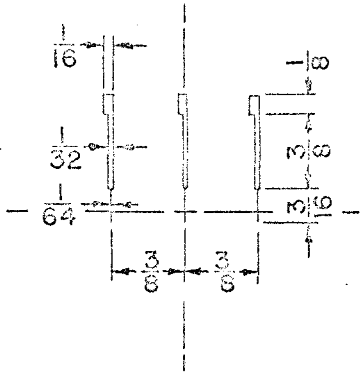
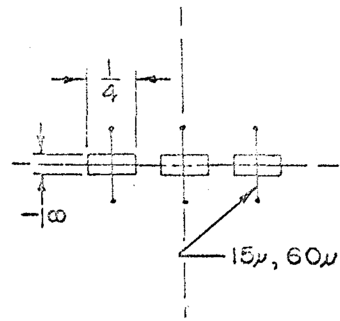


FIG 3-5 DIODE MASKS



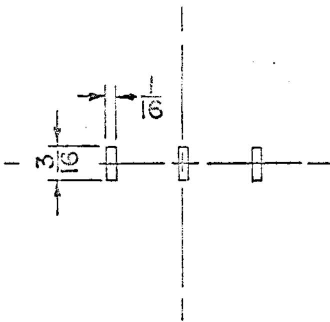
(A)

GATE ELECTRODE



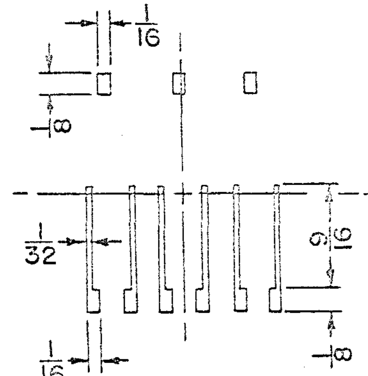
(D)

SOURCE - DRAIN



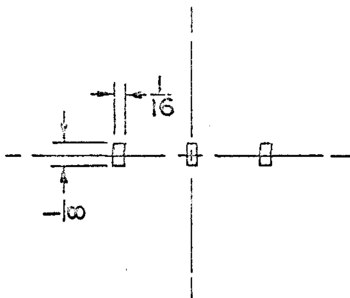
(B)

INSULATOR



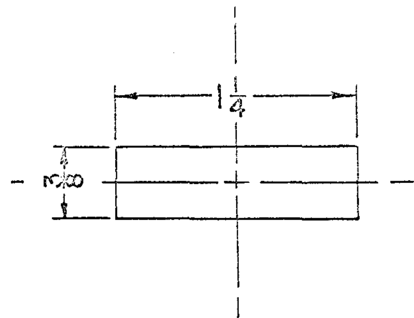
(E)

CONTACTS



(C)

SEMICONDUCTOR



(F)

COVER

FIG 3-6 TRANSISTOR MASKS

deposited on a substrate through some form of mask which thus yields the desired film pattern or patterns. Self-supporting masks, termed "out of contact" masks, are made from metal foils. Such masks are pressed closely against the substrate during deposition. It is to be noted, however, that such contacts are never perfect and some amount of pattern smearing must therefore always prevail.

Masks employed in this thesis were constructed from either 0.005 inch stainless-steel or brass foils. Brass was used in the later stages of experimentation when soft soldering of component parts became necessary in certain fabrications. An illustrative mask blank as was employed is as shown in Figure 3.3. The masks were aligned in the mask holder by two 1/8 inch diameter dowels to a tolerence of ± 0.001 inch and subsequently held in place by machine screws in each corner.

Patterns in the masks, as viewed through a stereo-zoom microscope (Bausch & Lomb), were cut by a razor knife. Final polishing with fine emery paper produced smooth pattern edges. Fine patterns such as the souce-drain gap of a transistor were produced by a composite mask using fine wire stretched across the gap. Mask patterns for the construction of thin-film resistors, diodes, and transistors are as shown in Figure 3-4, Figure 3-5, and Figure 3-6 respectively.

3.6 FILM DEPOSITION TECHNIQUES:

(a) Gold:

Gold films were used for conductors and contacts because of the ease of soldering the external connections with a low melting-temperature metal such as indium.

Although gold may be evaporated from a heated molybdenum boat, it tends to attack the molybdenum at high temperatures. For such boats as were employed in this thesis it was found that this results in a life-time limitation of approximately thirty evaporations. The use of a helical tungsten filament was investigated as an alternative, but in this latter case it was found that gold did not wet tungsten and poor results were generally obtained.

(b) Silver;

Silver films were used as high conductivity contacts. Molybdenum boats provide an excellent source for the evaporation of silver and the life expectancy of the boat is almost unlimited.

(c) Aluminium:

Aluminium films were utilized as electrodes and conductors in particular fabrications. Aluminium may be evaporated from a heated helical tungsten filament.

(d) Nichrome:

Nichrome provides a high resistivity metal film suitable for the production of thin-film resistors. Nichrome is an alloy which in general has a composition of 80% nickel and 20% chromium. It can be evaporated from a heated heavy-tungsten filament.

(e) Silicon Monoxide:

Silicon monoxide was used as an insulator in thin-film transistors as studied in this thesis, and also as an overlay on devices as a protection against atmospheric contamination.

The silicon monoxide used was a commercial-grade type, manufactured in pellet form by Kemet (Linde Company, Division of Union

Carbide Co.). Silicon monoxide must be evaporated from a baffled and covered molybdenum boat as it tends to sputter and produce pin holes in the deposited film. With this system, any large silicon monoxide particles that may be emitted tend to be confined to the interior of the boat rather than proceed to the substrate. It was found that in order to obtain a pin -hole free film of silicon monoxide it was necessary to evaporate it at a rate of 1 Å/sec in a bell jar containing pure oxygen at a pressure of 10^{-4} torr. Further the substrate temperature for these evaporations was held at 150°C.

(f) Aluminium Oxide:

Aluminium oxide, like silicon monoxide, was used as an insulator. Aluminium oxide could be produced on the substrate by slowly evaporating aluminium from a tungsten filament at a rate of 0.5 Å/sec in an oxygen atmosphere at a pressure of 10^{-4} torr, and at a substrate temperature of 150°C. In this way aluminium was found to oxidize and produce an insulating film.

Measurements of leakage currents for silicon monoxide and aluminium oxide films for several film thicknesses showed that silicon monoxide has both a lower leakage current and breakdown voltage than aluminium oxide; for example see Figure 3-7.

(g) Cadmium Sulphide:

Cadmium sulphide was used as the semiconducting material for both thin-film diodes and transistors. CdS films were produced by the evaporation of an electronic grade CdS powder supplied by RCA. (Electronic Components and Device Division) The powder was placed in an alumina crucible and heated from above by a tungsten filament. This

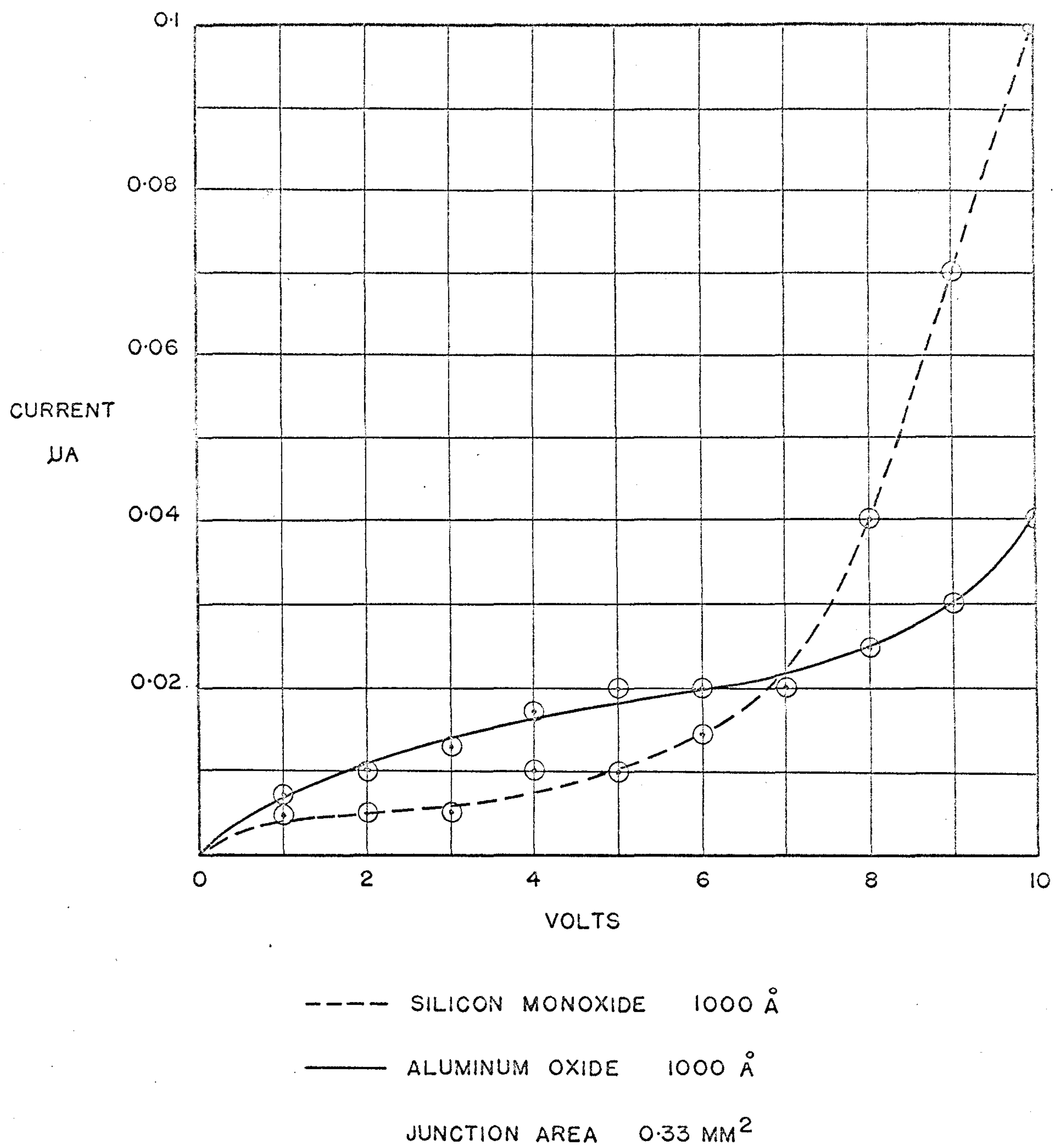


FIG 3-7 INSULATOR I-V CURVES

indirect heating method was found to be the best for fine control of the source temperature.

Unfortunately CdS tends to decompose at the temperatures required for evaporation. Because of this, the deposited film is often non-stoichiometric due to an excess of cadmium. It was found that many of the bulk properties of cadmium sulphide could be restored in the evaporated films if small amounts of free sulphur were added to the CdS source material. The amount used was one part sulphur to 30 parts CdS by weight. The substrate must be held at 200°C in order to prevent an excess of cadmium in the deposited layer[21]. Under these conditions the resistivities of deposited films can be as high as 10^4 Ω-cm. Films of this type are highly photoconductive and have the typical yellow-orange colour of bulk CdS. In experiments conducted with substrate temperatures of 20°C it was observed that excess cadmium would result in low film resistivities.

The following table gives a summary of some of the evaporation parameters for the various materials considered above.

MATERIAL	USE	SOURCE	TEMP.	PRESS.
gold	contacts	Mo boat	1220°C	10^{-6} torr
silver	contacts	Mo boat	958 "	10^{-6} "
aluminium	conductors	W filament	1085 "	10^{-6} "
nichrome	resistors	W filament	1260 "	10^{-6} "
silicon monoxide	insulator	Mo baffle box	1250 "	10^{-4} " O_2
alumium oxide	insulator	W filament	1280 "	10^{-4} " O_2
cadmium sulphide	semiconductor	crucible	840 "	10^{-6} "

TABLE 3-1: SUMMARY OF MATERIALS

3.7 PREPARATION OF DEVICES:

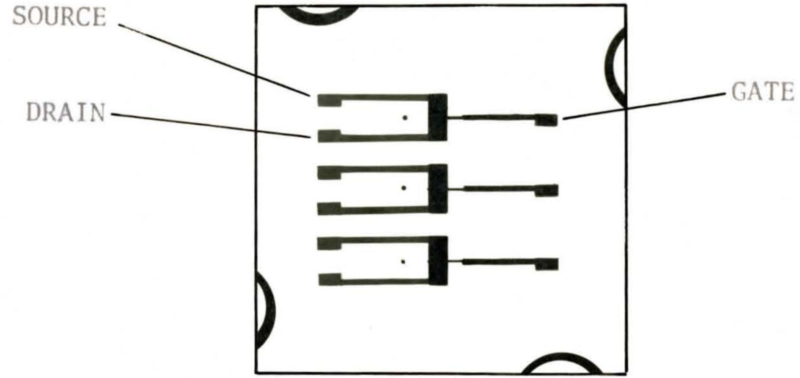
(a) Thin-Film Resistors:

Evaporated films of nichrome can be used as stable thin-film resistors. In the fabrication of such resistors, gold or silver contacts were first deposited on the substrate to facilitate external connections and provide contact pads for resistance monitoring purposes. These films were deposited to a thickness of 600-1000 Å. Next, the substrate temperature was raised to 300°C before the deposition of nichrome commenced. The mask dimensions, as shown in Figure 3-4, were such that nominal resistance values of 1 KΩ and 10 KΩ would be obtained if the evaporation was terminated when the monitor resistance reached 550 Ω. This corresponded to a film thickness of approximately 400 Å. Finally, an overlay of 2000 Å of silicon monoxide was deposited to protect the film from atmospheric exposure. The final unit is as shown in Figure 3-8 (b).

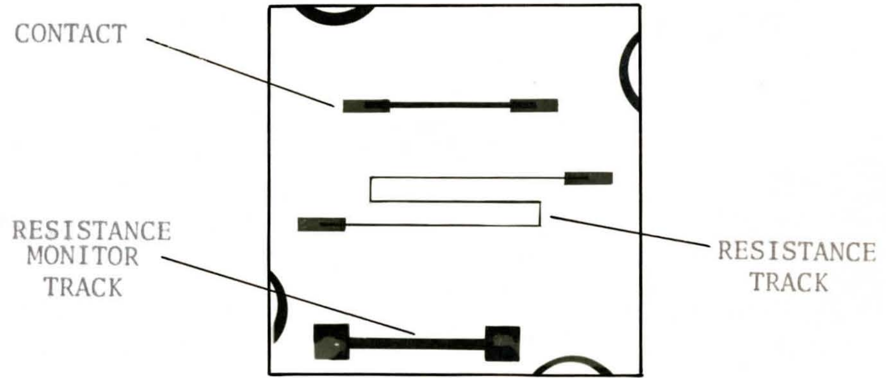
The substrate temperature of 300°C, as indicated above, was required to prevent resistance changes that might result from structural re-ordering of the film[21]. Post-evaporation annealing in air for 12 hrs. at 100°C was also found to be necessary for effective stabilization of resistance values.

(b) Thin-Film Diodes:

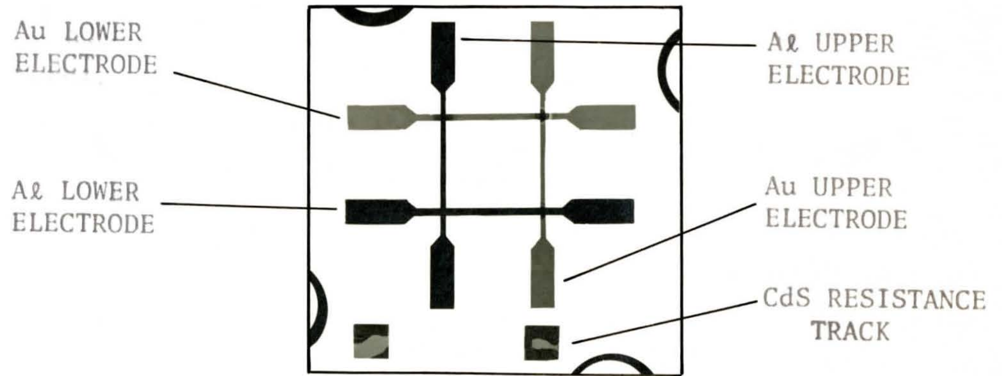
The diode structure as used, consisted of a metal-semiconductor-metal sandwich. Such a complete four-diode structure is as shown in Figure 3-8(c). The substrate temperature was first raised to 200°C, after which the lower aluminium and gold electrodes were deposited through their respective masks, as shown in Figure 3-5, to a thickness of 600 Å



(a) THIN-FILM TRANSISTORS



(b) THIN-FILM RESISTORS



(c) THIN-FILM DIODES

FIGURE 3-8: COMPLETE THIN-FILM DEVICES

in a pressure of 10^{-6} torr. The gold mask also provided the contacts for the resistance monitor described previously. Both metals were deposited at a rate of approximately 10 Å/sec. Next, in the sequence of evaporations, the temperature of the cadmium sulphide-sulphur source was raised very slowly. A source-outgas time of approximately 45 minutes was required if the bell jar pressure was to be held below 10^{-4} torr. This slow heating was also required to stop violent eruptions of the source material in the boat. The cadmium sulphide was deposited to a thickness of 15,000 Å at a rate of 8 Å/sec. and at a pressure of 10^{-5} torr. The resistance of the monitor track was noted throughout the deposition. While the monitor resistance could not be related directly to the diode resistance it gave a good indication of whether the device would or would not work when finally removed from the vacuum chamber. A final monitor resistance of approximately 5 MΩ usually indicated the fabrication of a good diode.

The substrate was then cooled to room temperature before the upper electrodes were applied. It was usually necessary to leave the vacuum system for several hours to allow the substrate temperature to drop to this value. The upper electrodes of aluminium and gold were then deposited following the same procedure as outlined for the lower electrodes, except that the substrate temperature was set at 20°C in this instance.

(c) Thin-Film Transistors:

The staggered-electrode structure shown in Figure 2-4(b) was used for the construction of thin-film transistors. Three transistors were deposited on a single substrate at the same time as illustrated in

Figure 3-8(a).

The gate electrode of aluminium was deposited first to a thickness of 500 Å at a pressure of 10^{-6} torr. Silicon monoxide of 500 Å film thickness was used as the insulator in preference to aluminium oxide because of the greater ease of deposition of the former. Experiments with films of silicon monoxide and aluminium oxide have shown that the films are comparable with regard to leakage current and breakdown voltage, but more care must be taken with aluminium oxide to prevent the occurrence of inclusions of aluminium metal.

Modulation of the semiconductor channel was observed in such devices regardless of whether or not the CdS evaporant contained a free sulphur additive. The CdS was deposited in exactly the same manner as that used for the diode. That is, at a rate of 8 Å/sec and with a pressure and substrate temperature of 10^{-5} torr. and 200°C, respectively. A CdS film thickness of 500 Å was employed in the device construction.

The substrate was allowed to cool to a temperature of less than 100°C before the source-drain electrodes were deposited. Experiments with diodes have shown that aluminium deposited on cadmium sulphide in this manner will give an ohmic contact. The aluminium electrodes thus employed were deposited in a vacuum of 10^{-6} torr. to a thickness of 500 Å.

In the next stage, gold films of 600 Å thickness were deposited as contacts on top of the aluminium electrodes, to facilitate the soldering of external connections with indium. Finally, an overlay of 1000 Å of silicon monoxide was deposited on all but the contacts, to protect the structure from atmospheric contamination.

CHAPTER IV

RESULTS

4.1 THIN-FILM RESISTORS:

In this section we are concerned with studies of thin-film nichrome resistors, which were constructed as outlined in Section 3.7(a). As will be discussed, such studies have embraced the effects of annealing and film composition, on resistance values. The temperature coefficient of resistance was evaluated for three resistors of differing resistance.

First let us consider the effects of annealing on resistance stability. During evaporation, if the substrate temperature was held at 300°C and if no subsequent post-evaporation annealing was performed on the sample, a nominal 550 Ω resistor was found to increase in resistance by as much as 0.5% over a three-week period. If, however, the sample was annealed in air at a temperature of 100°C for a period of 12 hours, the resultant resistance was found to be very stable with time. Various annealed samples exhibited a random resistance change of not more than 0.09% over a period of 10 months. This slight change in resistance could be attributed to changes in ambient conditions at the times of measurement.

Next, let us note the effects on resistance that may arise as a result of alloy composition. Typically, the sheet resistance of the samples was found to be 50 Ω/square for nichrome films whose thicknesses

were in the order of 400 Å. This observed sheet resistance was lower than would be expected in films which had bulk nichrome composition. This could indicate that such films were rich in chromium content[21]. This is reasonable, since chromium has the lower evaporating temperature of the nichrome alloy system.

Finally, the temperature coefficient of resistance was evaluated for three thin-film nichrome resistors. Such evaluations were made by measuring the resistance as a function of temperature over the range -180°C to +150°C with the aid of a Delta Design temperature chamber (Model 2300). Resistance measurements were made with a resistance bridge (Rubicon Instruments Model No. 1071) at every 10°C for both ascending and descending temperatures. All three samples showed a nearly-linear variation of resistance with temperatures over this temperature range. The results of such evaluations are given in Table 4-1 below.

RESISTANCE AT 0°C	T.C.R.
543.75 Ω	0.0127% per °C
1002.5 Ω	0.0125% " "
14.350 Ω	0.0099% " "

TABLE 4-1: TEMPERATURE COEFFICIENT OF RESISTANCE

These temperature coefficients for nichrome are consistent with those values found by other workers [21].

4.2 THIN-FILM DIODES:

(a) Formation of Rectifying Barriers:

Approximately 100 thin-film diodes were made prior to the attainment of those with acceptable I-V characteristics. Final devices

exhibited a forward to back resistance ratio of 10^5.

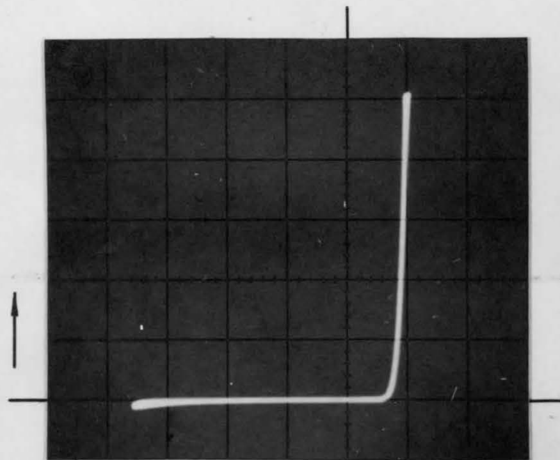
Typical I-V curves for four such diodes, as fabricated on the same substrate, are as shown in Figure 4-1. These diodes were constructed as outlined in Section 3-7(b), with free sulphur being added to the cadmium sulphide source. Four devices were used so that it was possible to have diodes with all combinations of the electrode materials, aluminium and gold, on the same substrate. This ensured identical semiconducting material as the CdS was deposited under the same conditions for each device. This allowed the study of the effect of different metals on the same type of semiconducting material. The diodes formed in this manner had the following structures; Aℓ-CdS-Aℓ, Au-CdS-Aℓ, Au-CdS-Au, and Aℓ-CdS-Au, where the first listed metal represents the lower electrode and the second metal the upper electrode.

The diode I-V curves were measured using the two closest terminals to each junction. Before measurements were made therefore, one of the connections between the four diodes was broken to isolate each device. The resistance of the thin-film connections to the junction, (approximately 10 Ω), was neglected in comparison with the forward resistance of the best diode which was approximately 100 Ω. The characteristics of the devices were traced by applying to the diode a 60 c/s sine wave from a General Radio audio oscillator (Type 1311A) in series with a 1 KΩ resistor. The voltage waveform obtained from the diode was applied to the x-axis of the oscilloscope and the current waveform taken from the voltage drop across the resistor was applied to the y-axis. The oscilloscope used was a Hewlett Packard 140A equipped with a type 1420A time base and a type 1420A dual-trace amplifier. The resulting I-V curves were recorded

(A)

Al - CdS - Al

1 MA/DIV.

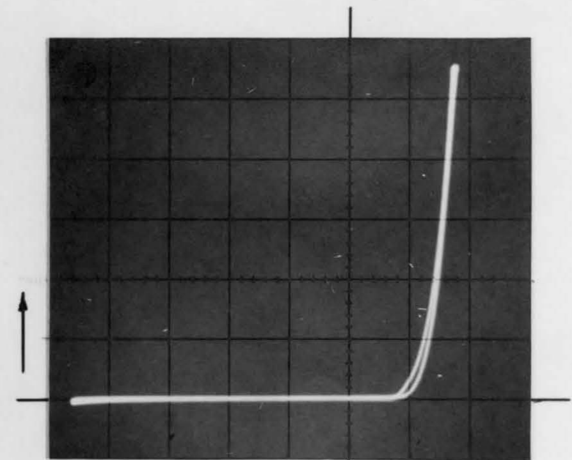


2 V/DIV.

(B)

Au - CdS - Al

1 MA/DIV.

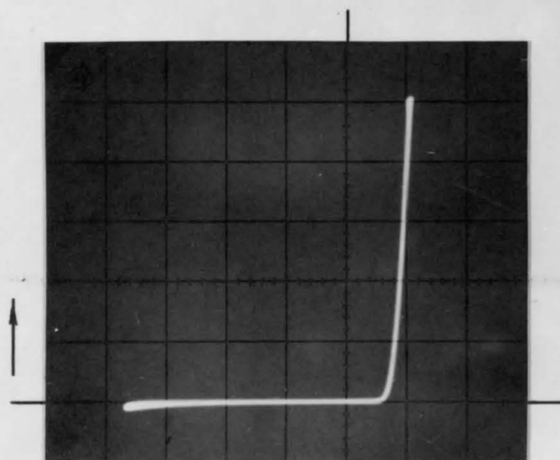


2 V/DIV.

(D)

Al - CdS - Au

1 MA/DIV.

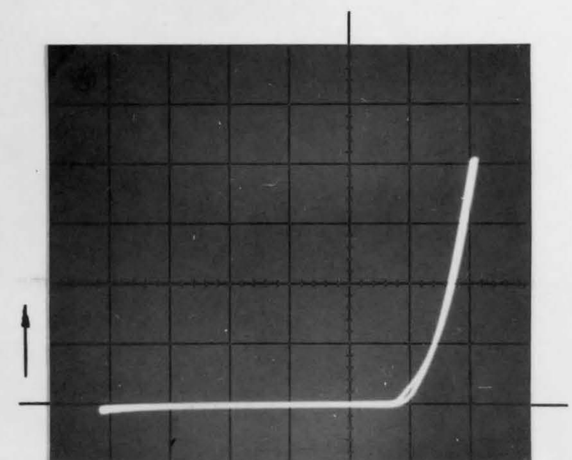


2 V/DIV.

(C)

Au - CdS - Au

1 MA/DIV.



2 V/DIV.

FIG. 4-1 DIODES

on an oscilloscope camera, Hewlett Packard Model 197A. All measurements were made with the diodes contained in a light-proof box.

In all cases the diodes become forward biased when the lower, or first deposited, electrode was made positive with respect to the upper electrode. The diodes with lower electrodes of aluminium, Figure 4-1(a) and (d), had similar I-V characteristics for which the knee of the curves occurred at approximately 1.4V. The other two diodes with a common gold lower electrode also had similar I-V characteristics, Figure 4-1(b) and (c). In this latter case the current rose at approximately 1.8 volts. No similarity was noted between Figure 4-1(a) and (b) which had a common aluminium upper electrode, or Figure 4-1(c) and (d) which had a common gold upper electrode. This would indicate that the rectifying barrier is formed between the lower electrode and the semiconductor. Since a positive lower electrode was required for forward-bias behaviour it was concluded that the semiconductor was of an n-type nature. This is consistent with data of other workers[14] who have found CdS to always be n-type. Further, and for the diodes studied, we observed that a gold electrode caused a larger rectifying barrier than did an aluminium one. This is reasonable since the work function of gold is higher than that of aluminium.

The rectifying properties of the metal-semiconductor contact can be seen to be only partially dependent on the metal used. If the barriers were solely determined by the work function of the metal and semiconductor the four diodes would not all be forward biased with the lower electrode positive. The introduction of acceptor-like surface states, at energies below the Fermi level of the semiconductor at the lower surface, would

cause the energy bands to bend upwards so that the barrier is partially formed by surface states. Since CdS dissociates upon evaporation, there are many possible causes of a high density of such states. The most likely is an excess of sulphur caused by the evaporation of sulphur from the CdS plus free sulphur mixture.

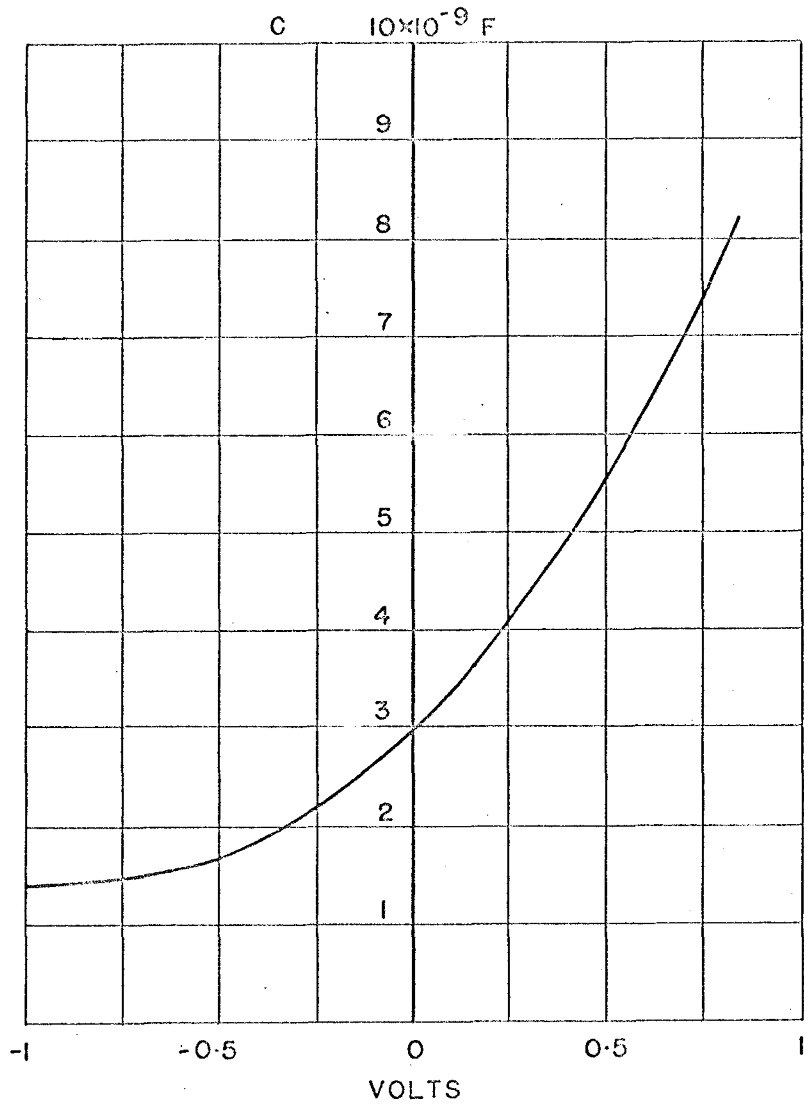
It was found that an ohmic contact was formed at the upper semiconductor-metal junction. This contact may be formed by using a metal with a lower work function than CdS, or causing the surface of the semiconductor to be a heavily doped n-type one. Again, both mechanisms are probably working in conjunction with each other to produce the contact. Aluminium, with the lower work function, should make ohmic contact with CdS. On the other hand, a heavily doped n-type surface may be necessary for gold. The n^+ surface could easily be produced at the end of the evaporation, as any excess sulphur would be driven off from the source in the early stages of evaporation and the final layers of the film would become cadmium rich.

The formation of rectifying barriers in thin-film diode structures does not depend solely on work-function considerations, but also on deposition parameters of the semiconductor. Other diodes were constructed in which no sulphur was added to the CdS source, but otherwise the techniques for evaporation were exactly the same. In this case the knee of the I-V curves occurs at approximately 0.2 volts forward bias. The maximum reverse voltage of such a diode is about 2 volts as compared to the 8-10 volts that results when free sulphur is added. A lower forward voltage indicates a lower barrier height, which is consistent with the lack of excess sulphur in the film.

(b) Capacitance Measurements:

The capacitance across a particular Aℓ-CdS-Au diode was measured as a function of applied voltage for both forward and reverse bias. The measurements were made on a capacitance and conductance bridge. This bridge measures the magnitude of the in-phase or out-of-phase component of a sine wave that is superimposed on the DC bias across the diode. The output of a phase sensitive detector is fed directly to an X-Y recorder, allowing a continuous plot of capacitance or conductance versus applied voltage to be obtained. For the particular measurements made, the modulating signal employed was 10 millivolts at a frequency of 1 Kc/s with a DC bias which could be varied from +1 volt to -1 volts. The results are shown in Figure 4-2(a).

The theory of a Schottky barrier predicts that the capacitance across the barrier varies inversely as the square root of voltage. Hence, if a Schottky barrier exists, a plot of $1/C^2$ versus applied voltage should be a straight line for reverse bias as shown in Figure 4-2(b). Extrapolating this line to the voltage axis gives the value of the diffusion potential V_D. From a knowledge of the slope of this $1/C^2$ plot, the donor concentration Nd can be evaluated with recourse to equation (2-8). For the particular Aℓ-CdS-Au diode under consideration the area of the junction was 0.67 mm^2. Further, the permittivity of CdS was taken to be 10^{-10} f/m[4,10]. This gives a donor-concentration value of $6 \times 10^{17}/cm^3$. The thickness of the depletion layer can also be evaluated from the above information using equation (2-9). The thickness of the depletion layer was evaluated as being 230Å at equilibrium.



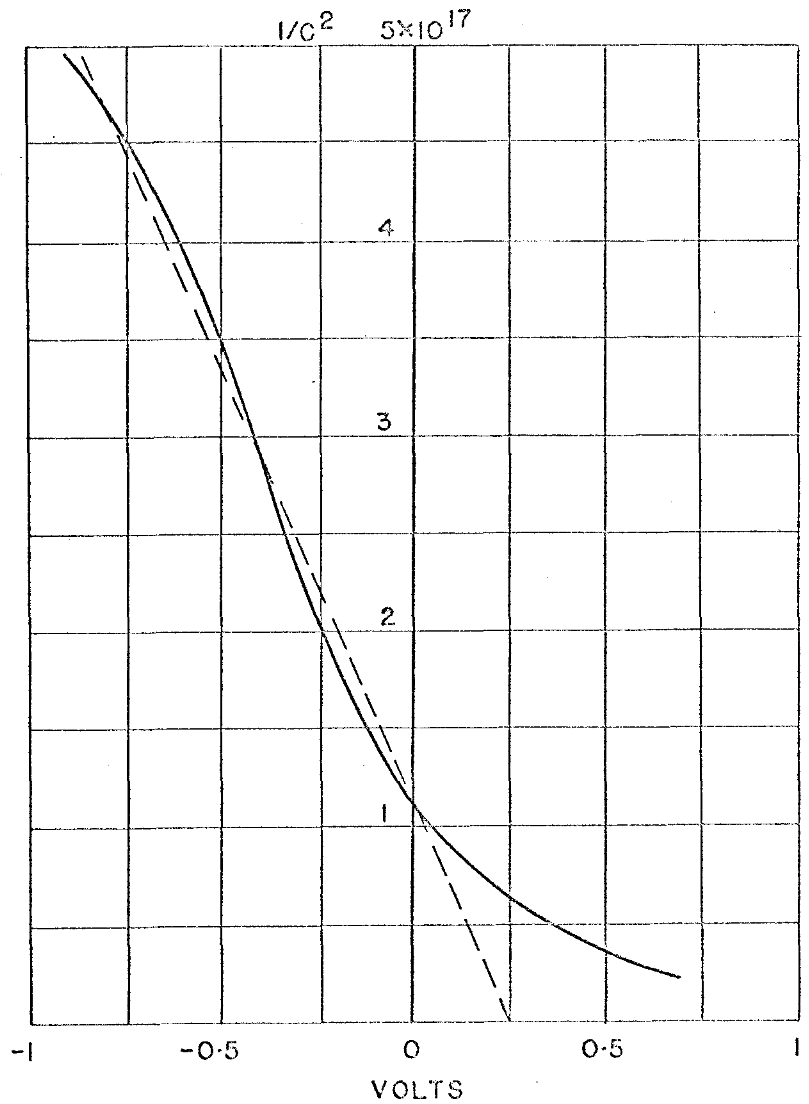


FIG 4-2 CAPACITANCE MEASUREMENTS Al-CdS-Au DIODE

(c) Forward Bias:

Point by point measurements of the I-V curves were made using two DC vacuum-tube voltmeters (Hewlett Packard Model 412A). A Harrison Laboratories Model 6200A power supply was used as the variable DC voltage source. During each measurement, at least one minute was allowed for the readings to stabilize.

If the dominant mechanism limiting the forward current of a diode is that of thermal diffusion over a barrier, then the current should have an exponential dependence on voltage. The basic equation governing this mechanism is as given in (2-1). When applied to a given diode, however, the above must be modified to the following form, namely,

$$J = J_o \left(e^{\frac{qV}{nkT}} - 1 \right) \quad \text{where } n = \text{const} \qquad \ldots.(4-1)$$

For forward voltages such that $V >> nkT/q$, a plot of log J versus V will be linear if equation (4-1) is obeyed. This is as shown in Figure 4-3 for an Aℓ-CdS-Au diode. The extrapolated intercept of this straight line upon the ordinate provides a measure of J_o, where the value of the saturation current J_o is given by equation (2-2). If the effective mass of an electron in CdS is known, then the difference between the work function of the metal, and the electron affinity of the semiconductor at the surface can be calculated. (For CdS, at room temperature, the mass ratio has been established as $m^*/m = 0.27$[14]). This yields a barrier height of 0.7 volts, for the particular Aℓ-CdS-Au diode discussed in Section 4-2(b). It should be pointed out, however, that this method is not a very accurate one.

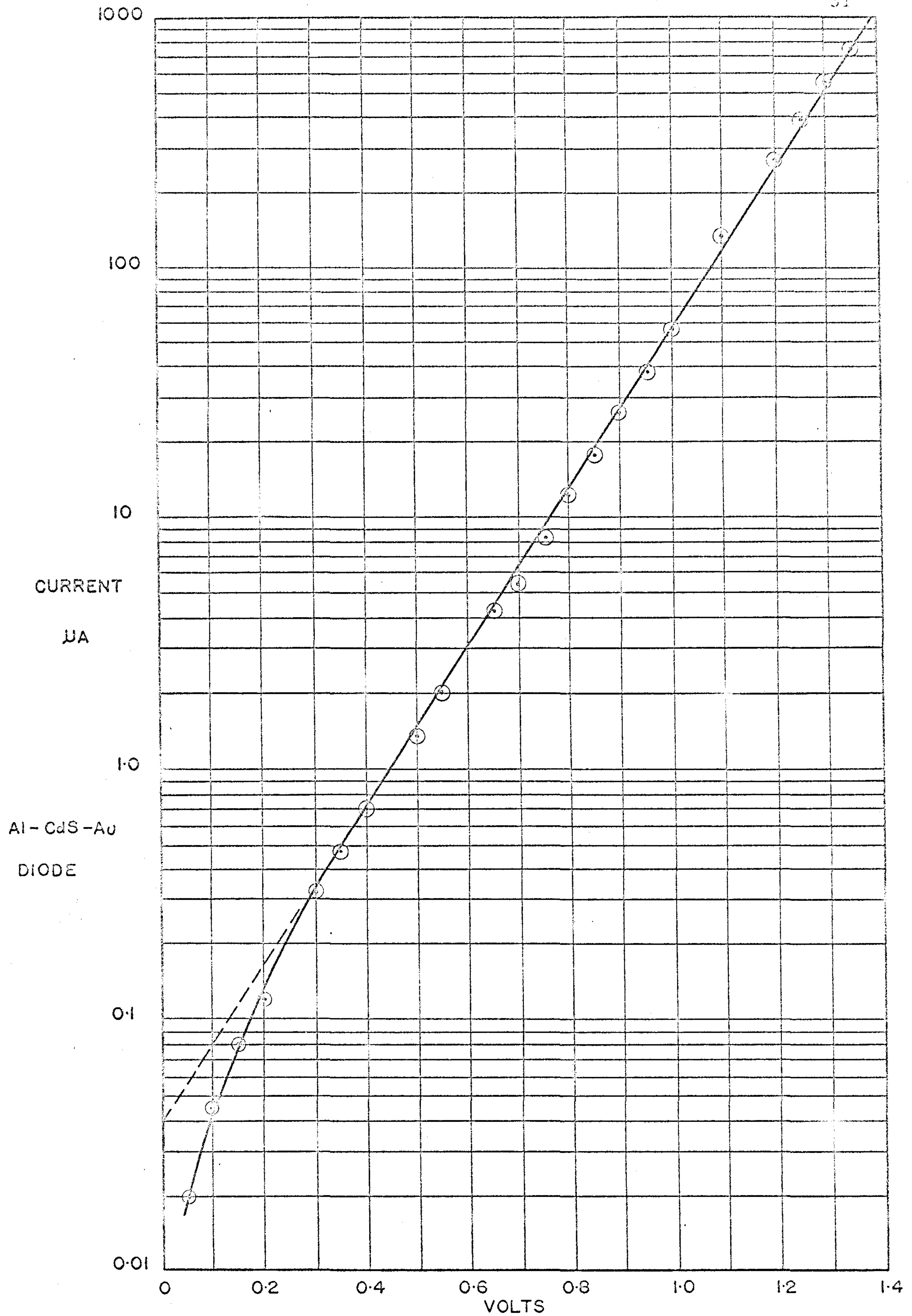


FIG 4-3 FORWARD BIAS I-V CURVE (DIODE)

From the slope of the plot given in Figure 4-3, a value of n can be determined. For this particular diode at room temperature $n = 5.2$. Measurements on other diodes, however, have shown that n may vary from 5 to 7. These values of n are a factor of two larger than those found for single crystal CdS diodes[4].

(d) Reverse Bias:

No current saturation was observed in the reverse bias direction for the thin-film diodes studied; rather the current increased gradually with increasing voltage until breakdown was reached. According to equation (2-7), relating current and voltage in the reverse direction, a linear relationship should be obtained between log J and $(V + V_D)^{\frac{1}{4}}$ for $|V| \gg kT/q$ if a Schottky barrier is present, and the lowering of the barrier height is due to image forces[6]. A plot of the reverse characteristics of the diode discussed in the previous Section 4-2(b) and (c) is as shown in Figure 4-4. The resultant straight-line characteristic for applied voltages greater than $V = 0.25$ volts is a clear indication that equation (2-7) is followed, and that a Schottky barrier does exist at the metal-semiconductor interface.

(e) Temperature Dependence:

Measurements of I-V curves were also made at 77°K, although only limited results were obtained. The low temperatures were attained by inserting the diode into a dewar of liquid nitrogen. Unfortunately, due to the different coefficients of thermal expansion of the metals and the glass substrate, the upper electrode almost always cracked completely across the film at the point where it passed over the cadmium sulphide.

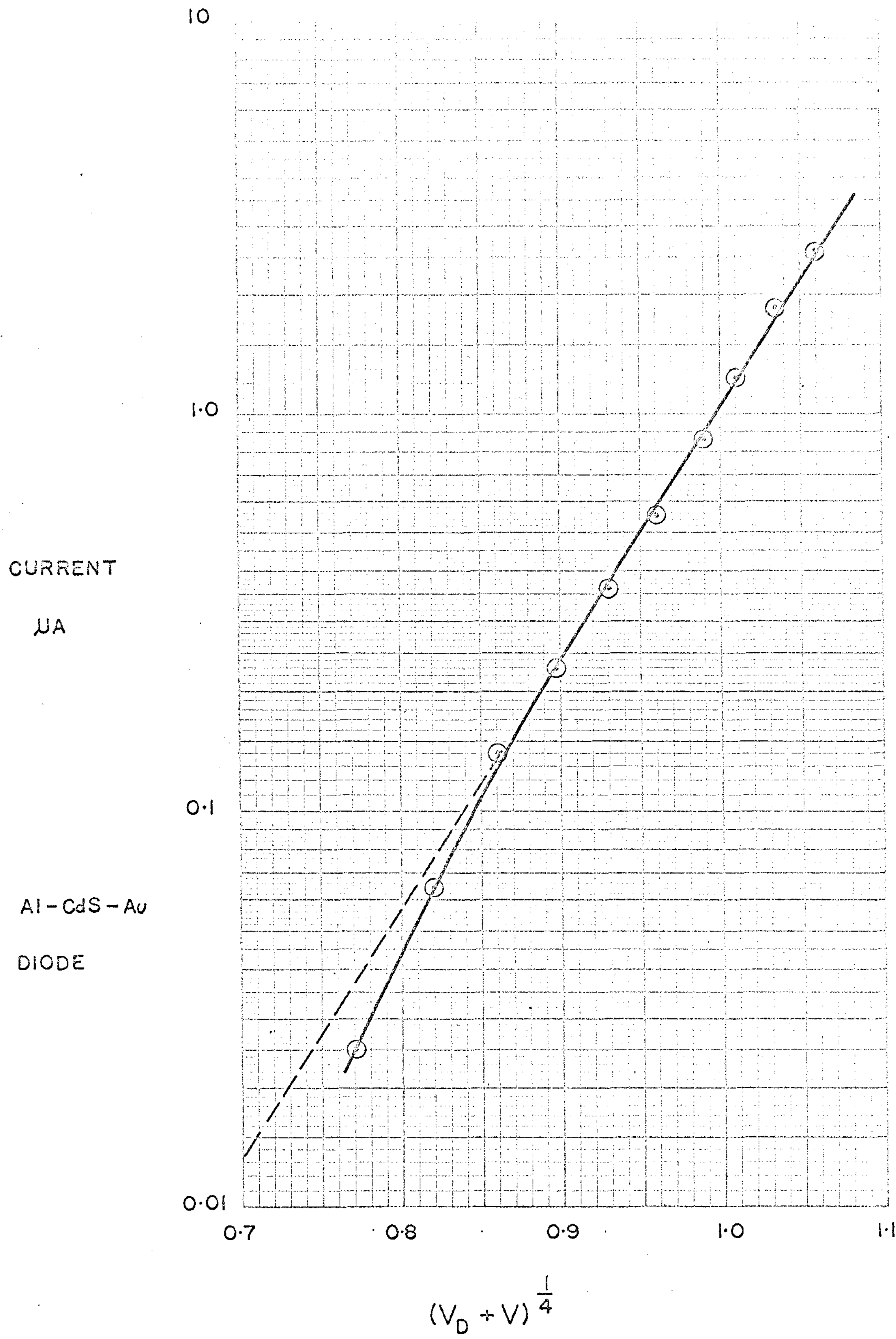


FIG 4-4 REVERSE BIAS I-V CURVE (DIODE)

Comparing results for an Aℓ-CdS-Aℓ diode at room temperature and at 77°K showed that the forward voltage at which the knee occurred was twice as large at 77°K as it was at room temperature. The reverse current was much smaller at the lower temperature, while the breakdown voltage was much higher.

Equation (2-2) shows that the temperature dependence of the saturation current is governed by the relationship $T^2 \exp\left|-\frac{q\phi}{kT}\right|$, in which the exponential term donimates. ϕ is not particularly sensitive to temperature change, being determined by the position of the Fermi level and the work functions of the materials involved. Therefore, as the temperature decreases, the saturation current will also decrease. Because of the lower value of saturation current, the forward knee of the curve would occur at higher voltages, since a larger forward voltage would be required for the same current flow.

(f) Space-Charge Limited Currents:

At lower applied voltages the I-V curves indicate that the current may be limited by thermal diffusion over the barrier. At larger applied voltages, however, the Schottky barrier disappears and the current becomes space-charge limited.

In order to achieve space-charge limited currents, the applied forward voltage must be rather high. The heating effects produced by the large currents necessitate the use of pulse measurements to prevent device burnout. Applied voltage pulses with widths of 5 μsec were used in order to give inherent transients time to die out. Measurements made on a Au-CdS-Aℓ diode were plotted on log-log co-ordinates as shown in Figure 4-5. Unfortunately the square-law characteristic, as predicted

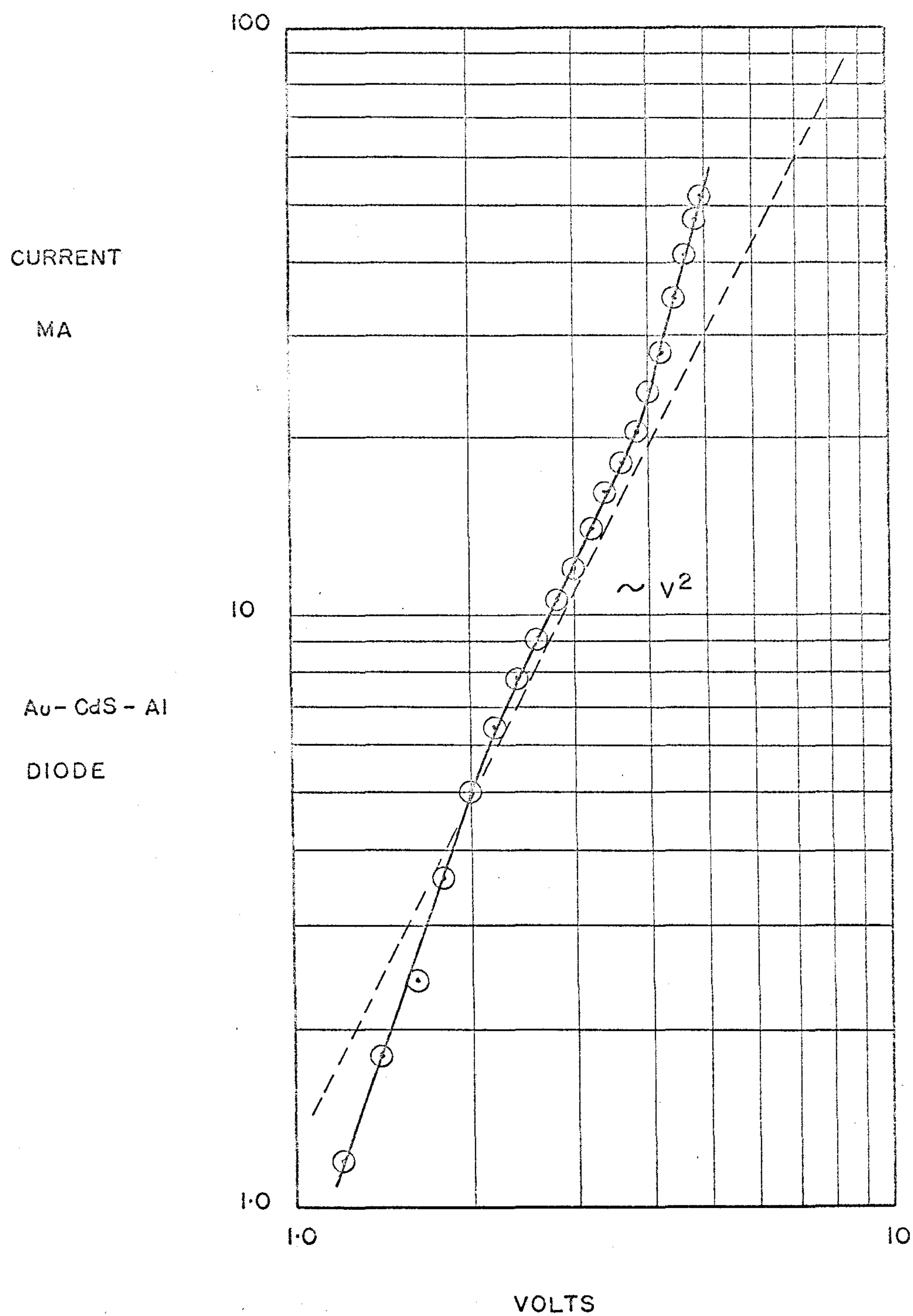


FIG 4-5 FORWARD BIAS PULSE MEASUREMENTS

(DIODE)

above the trap-filled limit by equation (2-3), is not observed exactly. The slope of this line is closer to a cubic fit, rather than to a square law. Lampert[7] shows that the current varies as the cube of applied voltage if double injection exists. This does not seem possible with cadmium sulphide, however, since p-type conductivity has never been observed.

Point by point DC measurements on many other diodes as examined here, have shown straight-line characteristics over a limited range when plotted as log I versus log V. At lower applied voltages, current dependence on voltage varied from V^3 to V^8 depending on the device. Above the trap-filled limit, however, the square-law response was observed. Typical results are as shown in Figure 4-6 for a Au-CdS-Aℓ diode. Results of this type are characteristic of devices operating in a region where the Fermi level is coincident with the trapping level.

Consider the case of a one-carrier space-charge limited system with trapping levels slightly above the Fermi level. As electrons are injected, the Fermi level moves up energy-wise and the traps become filled. The loss of charge carriers to the traps reduces the current significantly from that expected from a square law dependence. When the traps are filled, however, the current will rise rapidly as there is no longer any loss of carriers. Just how fast the current indeed rises with voltage should be determined to a great extent by the distribution of these trapping energy levels. When the traps are filled, the current becomes dependent on the square of the voltage as indicated in equation (2-3).

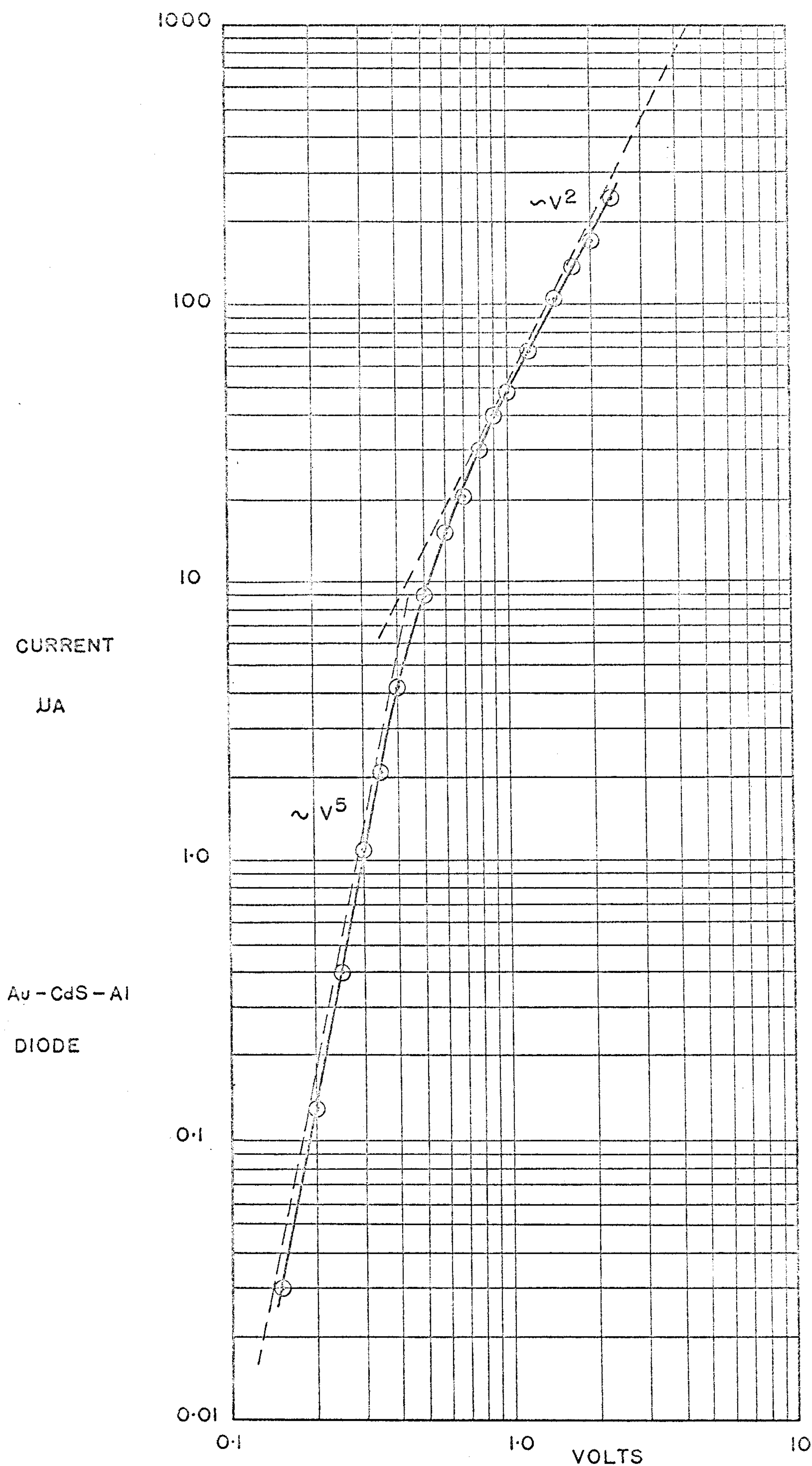


FIG 4-6 FORWARD BIAS SCLC (DIODE)

(g) Summary:

Capacitance, current-voltage and temperature measurements, as performed on the thin-film diodes studied, all indicate that a Schottky barrier is formed as the lower metal-semiconductor contact. The energy band diagram as given in Figure 4-7 shows the results of the calculations made on a particular Aℓ-CdS-Au diode.

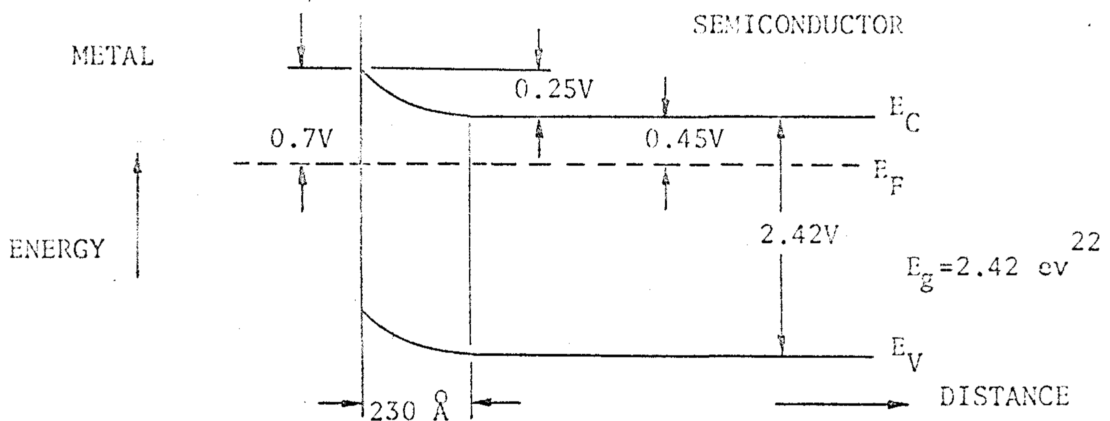


FIGURE 4-7: ENERGY BAND DIAGRAM AS EVALUATED FOR AN ALUMINIUM-CADMIUM SULPHIDE CONTACT

The above results are in reasonable agreement with those obtained by other investigators[4,10]. In this respect, for high resistivity single crystal CdS, the Fermi level is located at energies of 0.3 - 0.5 ev below the conduction band[4], while for thin-film CdS the quoted energy value is in the range 0.4 - 0.5 ev[10]. These positions of the Fermi level correspond to 10^{15} to 10^{13} mobile carriers per cm^3.

Resistance measurements on thin CdS films of 6000 Å thickness have shown the concentration of mobile carriers to be in the order of 10^{14} per cm^3. This concentration is low as compared to the donor concentration, and thus indicates a high density of traps. This is to be expected in a vacuum-deposited polycrystalline film.

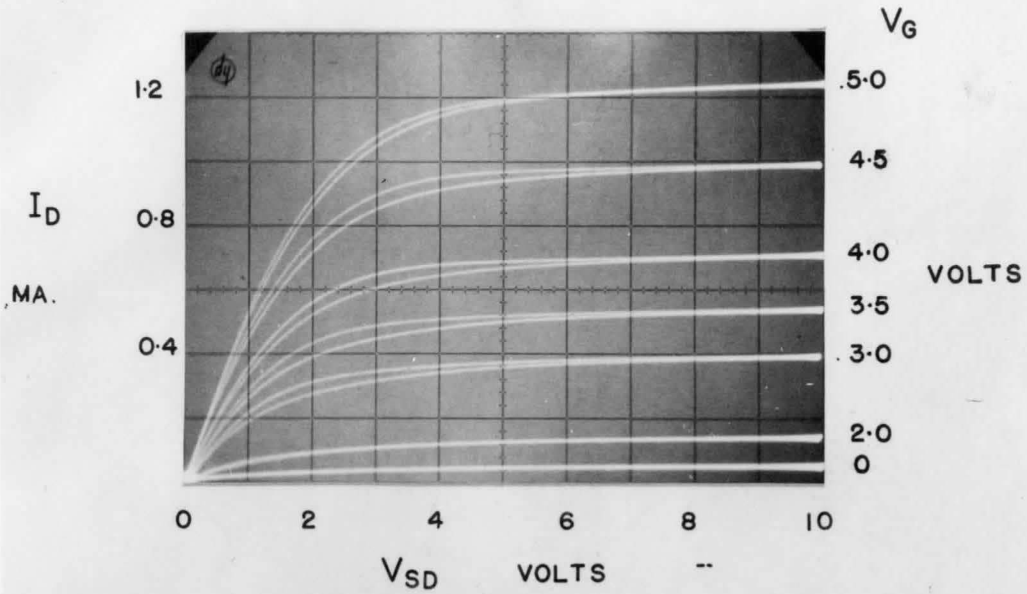
4.3 THIN-FILM TRANSISTORS:

The general outline given in Section 3-7(c) was followed in the fabrication of thin-film transistors using cadmium sulphide. The first devices failed to operate for many reasons, the most predominant being poor insulation between the semiconductor and the gate. Extensive work on aluminium oxide and silicon monoxide showed that the best insulating films were obtained when the oxide was deposited very slowly. A 500 Å film of silicon monoxide was found to have a leakage current of less than 0.01 μa at the operating voltages required for a transistor.

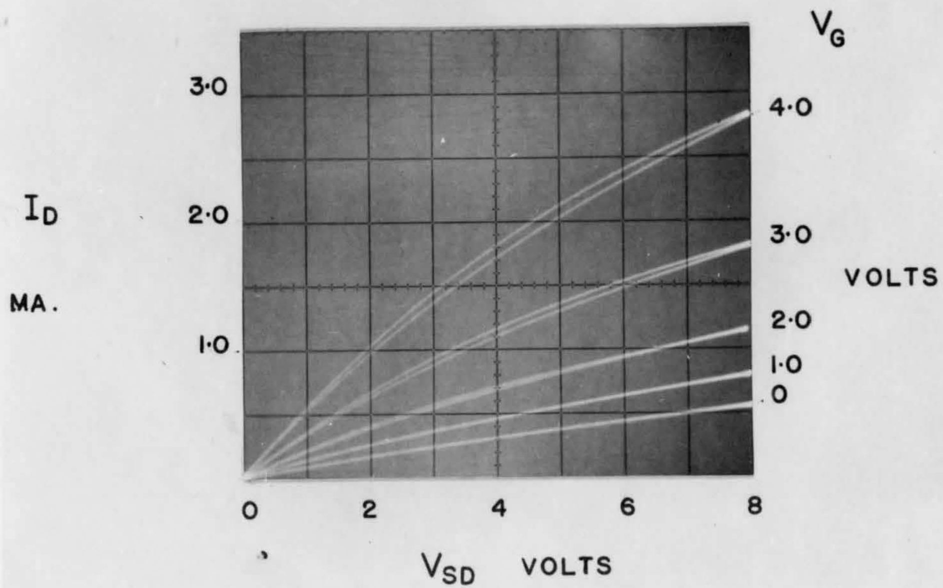
The existence of a shunt conductance between the source and drain was also noted in early devices. In these cases the deposited semiconductor was too thick and any possible modulation was swamped by the effect of the bulk conductance of the semiconductor. A semiconductor thickness of 500 Å appeared to be optimum in devices fabricated in this manner.

The characteristic curves for the transistors were measured with the same general equipment as used for the diodes. A germanium diode 1N34A was placed in the driving-oscillator circuit so that only the positive half of the characteristic was observed. A 1 KΩ resistor was again used to obtain the current waveform for the drain current. The gate bias was supplied by a Harrison Laboratories DC power supply (Model 6200A) using two Hewlett Packard DC vacuum tube voltmeters (412A) to measure gate current and voltage. Multiple exposures of the oscilloscope traces were made to obtain a family of curves for the device characteristics.

TFT. CHARACTERISTICS



(A)



(B)

FIG 4-8

Characteristic curves for operating devices are as shown in Figure 4-8(a) and (b). The second figure is typical of devices that failed to saturate. Failure to saturate would indicate that the channel cannot be pinched-off, at least by any reasonable applied voltage. This may be caused by the insulator being too thick, the source-drain spacing too small, or an unmodulated parallel conductance path between the source and drain. The best operating characteristics were obtained with devices having a very-thin insulating layer. The transistor illustrated in Figure 4-8(a) had an oxide thickness of 240 Å. The hysteresis at the knee of the curve is a function of the device and not the measuring circuit. The size of the loop did not depend on the sweep frequency used but was probably associated with trapping levels in the semiconductor.

The validity of the field-effect model can easily be checked by fitting the characteristic curves (Figure 4-8(a)), of an operating transistor to equations (2-17) and (2-18). Since the drift mobility for this particular sample is not known, it must be determined from the saturation characteristics with recourse to equation (2-18). From a knowledge of the drain current, it is possible to calculate carrier mobility for a given gate voltage and given transistor dimensions. This evaluation further requires a knowledge of the insulator relative permittivity, which for silicon monoxide evaporated under the specified conditions is 2.4[23]. In this particular transistor the channel was 60 microns long and 2.4 mm wide while the oxide thickness was 240 Å. The average drift mobility calculated for all values of gate voltage was found to be 25 cm^2/V-sec -- which compares favourably with results of other workers[10]. This value of mobility was substituted back into

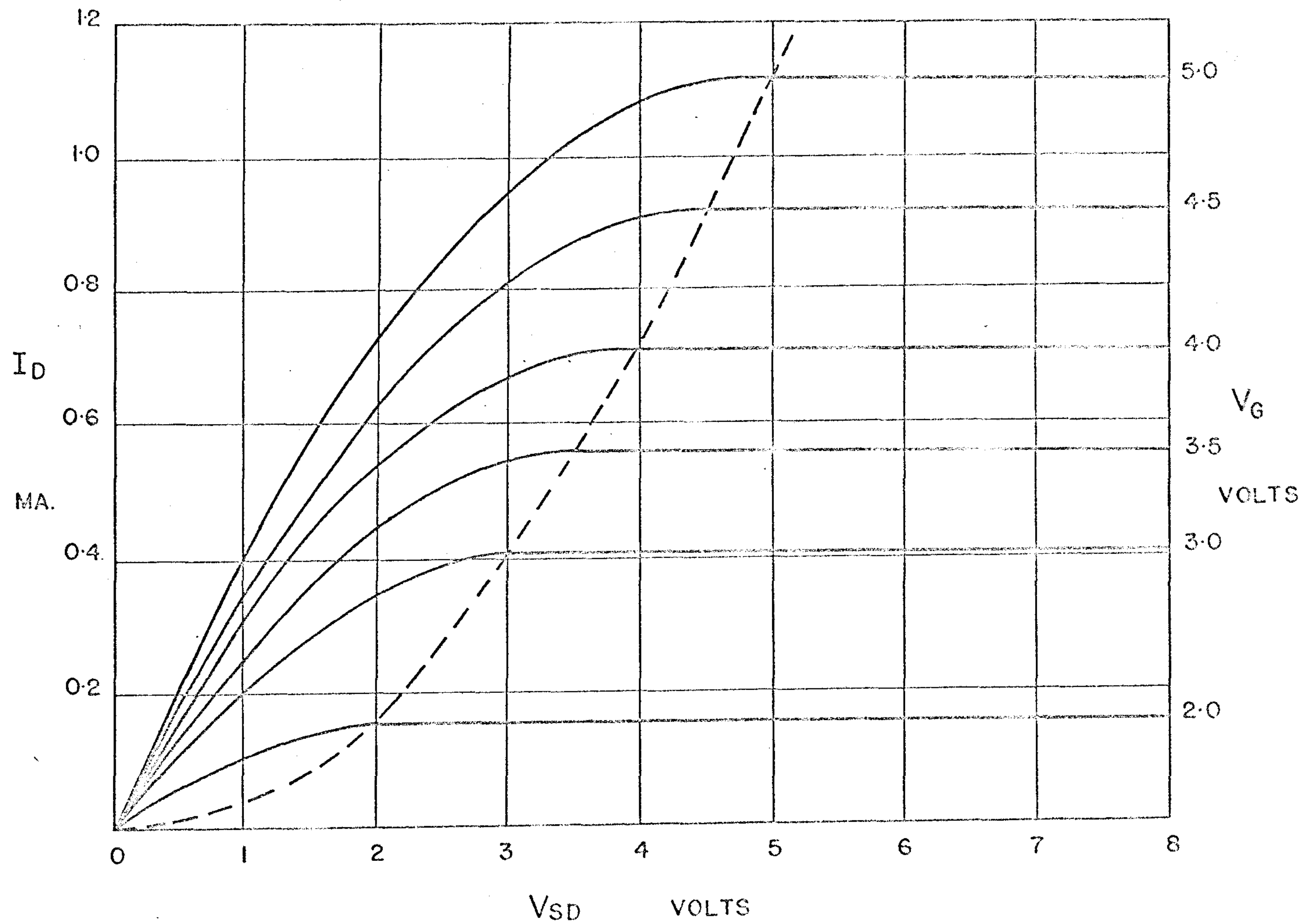


FIG 4-9 THEORETICAL TFT. CHARACTERISTIC CURVES FOR FIG 4-8 (A)

equation (2-17) to generate the theoretical characteristic curves for the particular transistor as given in Figure 4-9. Comparison of the theoretical and experimental curves shows that the field-effect model fits these particular devices.

The transconductance of the above device was found to be 450 μ mhos, while the dynamic output resistance derived from the slope of the saturation position of the curve was 125 KΩ. The product of these two quantities gives an amplification factor of 56.5. Devices were built with transconductances of up to 3,000 μ mhos, but unfortunately these units did not exhibit good saturation characteristics. The input resistance of all devices under operating conditions was greater than 10 MΩ. The value of shunt capacitance will of course depend on the insulator thickness of the particular device. A shunt capacitance of 400 pf was found to be characteristic of a transistor incorporating an insulator of 240 Å thickness. The input capacitance can be reduced, of course, by increasing the thickness of the oxide, but this also decreases the transconductance of the device.

Device performance may best be improved by changing the dimensions of the structure. The input capacitance can be reduced by decreasing the size of the gate electrode. Ideally, the gate electrode should have the same dimensions as that of the source-drain gap. This would reduce the input capacitance while still maintaining modulation of the full channel length. Experimental units were fabricated with source-drain gaps of 60 and 15 microns. Because of the difficulty in lining up the different masks, however, it was necessary to make the gate electrode 150 microns wide. This extra overlap drastically

increased the input capacitance beyond the minimum required value. While a decrease in the source-drain gap dimensions would result in an increased transconductance, it is to be noted that if the spacing is too small there will be insufficient electrostatic shielding of the gap region and no channel will be formed.

Some transistors which were tested frequently over a period of two months exhibited little change in device characteristics. Others, however, which exhibited initially good characteristics were found to fail after a few days. Examination of the latter devices after failure showed a pitting in the insulator which would indicate breakdown of the insulator due to excessive gate voltages. The electric field across such an oxide layer under operating conditions is approximately 10^6 V/cm, which is close to the breakdown field for most insulators. Internal breakdown of the semiconductor channel was also noted for drain voltages above pinch-off values. This semiconductor breakdown was demonstrated by a sudden increase in drain current, unaccompanied by any increase in gate voltage or current.

4.4 THIN-FILM TRANSISTOR APPLICATIONS:

Thin-film transistors were used as amplifiers to test the capabilities of the device in circuit performance. An amplifier, as shown in Figure 4-10, was constructed from conventional carbon resistors having 10% tolerance on resistance values.

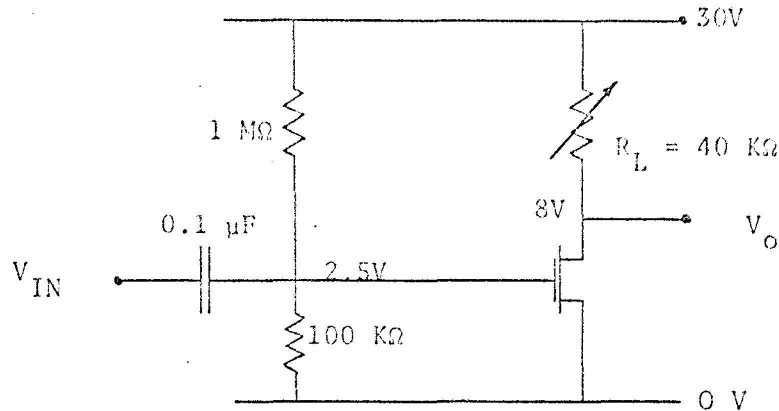


FIGURE 4-10: THIN-FILM TRANSISTOR AMPLIFIER

The gate biasing was supplied by the series combination of a 1 MΩ and a 100 KΩ resistor. The measured gate voltage was 2.5 volts with a drain voltage of 8 volts and a drain current of 0.55 ma at the operating point. The maximum voltage gain derived from this amplifier was 4, using a transistor having a transconductance of 300 μ mhos and a dynamic output resistance of 25 KΩ.

For a fixed supply voltage the voltage gain of such an amplifier would increase as the load resistor R_L was increased if g_m was constant. In thin-film transistors, however, the transconductance varies as the square root of drain current, so that a decrease of I_D results in a decrease of gain. The optimum value of R_L for this particular circuit was 40 KΩ. The measured gain for a 1 Kc/s sine wave was 4. The theoretical gain using the values of g_m and r_p taken from the characteristic curves was 4.6. Very little distortion was seen in the output waveform even with an output of 4 volts p-p.

CHAPTER V

CONCLUSIONS AND RECOMMENDATIONS

A study of the fabrication techniques and electrical characteristics was carried out on thin-film resistors, diodes, and transistors. All devices were vapour deposited through metal masks.

Stable thin-film resistors were produced using nichrome as the resistor material. An average value of the temperature coefficient of resistance of 0.012% per ^{o}C was measured for resistors over a range of 550 Ω to 14 KΩ. By using a resistance monitor, the sheet resistance of a film could be controlled accurately, with the values of individual resistors being determined by the geometry of the mask. This system gives high tolerance on resistance values - allowing the production of high quality resistors for thin-film integrated circuits.

An investigation of a metal-semiconductor-metal sandwich has shown excellent diode characteristics having a ratio of reverse to forward resistance in excess of 10^5. In all cases the lower, or first deposited, metal-semiconductor surface formed the rectifying barrier. While the work junction of the metal electrode does determine the barrier height to some extent, the actual formation of a barrier could be attributed to the presence of surface states in the CdS film. In the forward bias direction the lower electrode was positive with respect to the upper electrode. The upper, ohmic, contact was formed either by using a

metal with a work function lower than that of CdS, or by causing a heavily doped n-region to be formed at the upper surface of the semiconductor. These results show that diode action depends critically on the evaporation of CdS.

Measurements of capacitance, forward and reverse bias I-V curves, and temperature dependence all indicate that a Schottky barrier was formed at the lower metal-semiconductor contact. The forward current was controlled either by thermal diffusion over the barrier or by space-charge limitations. At lower forward voltages, thermal diffusion is the dominant conduction mechanism.As the bias is increased, the current becomes space-charge limited. Experimentally, space-charge limited currents were observed in CdS films which had a high resistivity.

Although the diode characteristics were acceptable for circuit performance, fabrication difficulties do not yet allow predictable results to be obtained.

Thin-film transistors were constructed using a staggered electrode structure. The best operating characteristics were obtained when the silicon monoxide and cadmium sulphide films were both 500 Å thick. The highest transconductance observed was 3000 μ mhos although devices with the best saturation characteristics had a transconductance of only 450 μ mhos. All such transistors operated in the enhancement mode. This mode of operation is best suited for integrated circuit design since multiple stages can be DC coupled. The simple amplifier constructed shows the feasibility of using such devices in practical circuits.

The drawback to the use of thin-film transistors at the present

time is the instability of the characteristics with time. While some experimental units were checked frequently over a period of two months and found to have only slight variations in characteristics, others failed within hours. The reasons for failure are not understood. The insulator, however, appears to play an important role in device performance.

One problem with the experimental system was the mask alignment. The Edwards vacuum-coating unit employed is designed to have a mask alignment of ± 0.001 inch. This tolerance is too large for the exact positioning of the source-drain electrodes. With the suggested introduction of additional alignment pins it should be possible to improve this tolerance limitation by a factor of 10.

More fundamental work must be done on the vacuum deposition of insulators and semiconductors before reliable thin-film devices can be produced. In order to determine more about the semiconductor it would be advisable to do conductivity measurements and Hall mobility measurements on films deposited at the same time as a transistor and on the same substrate.

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