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SEGMENTED LATERAL P–N–P TRANSISTORS

D.C. MODELLING
OF
SEGMENTED LATERAL P-N-P TRANSISTORS

By

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ABSTRACT

An approximate model has been developed for the p-n-p lateral segmented transistor, and used to characterize the behaviour of the common-emitter dc current gain to the collector segment when the control segment is set to arbitrary voltage levels. The model is a development of the type introduced by Ebers and Moll.

The dc current gain is found to be a sensitive function of the control segment voltage, and for changes in this voltage level of the order of $\pm$ 200mV, it can be made to vary between two limiting values which are dependent on device geometry. A number of applications for this device have been suggested, particularly where an a.g.c. function or controlled current source requirement are needed.

An analytic expression has been obtained for the controlled h_{FE} in terms of the control segment voltage and the device parameters, using an approximate analogue for the device geometry. The results have been found to describe the behaviour for a family of p-n-p lateral transistors, having circular geometry with different segment periphery ratios, within the limits of the approximations and experimental errors.

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LIST OF ILLUSTRATIONS

LIST OF SYMBOLS

A	coefficient defined by equation (33)
A_C	area of the upper half of the inner side-wall of the circular collector
A_C'	area of the lower half of the inner side-wall together with an annular floor area at the inner rim of the collector
A_C''	area of the outer side-wall together with the remaining annular floor area at the outer rim of the collector
A_E	area of the upper half of the emitter side-wall
A_E'	area of the lower half of the emitter side-wall together with an annular floor area at the outer rim of the emitter
A_E''	area of the circular floor of the emitter
A_G	an area equivalent to the curved face of one side of the segment gap
a	an effective base width as defined in Fig. A3.
B	coefficient defined by equation (36)
b	an effective base width defined in Fig. A3.
c	an effective base width defined in Fig. A3.
D_n	diffusivity for electrons in the p-region
D_p	diffusivity for holes in the n-region
d	an effective base width defined in Fig. A3.
dA	element of area
$h_{FE(c)}$	controlled common-emitter current gain
$h_{FE(max.c.)}$	the maximum value of $h_{FE(c)}$
$h_{FE(min.c.)}$	the minimum value of $h_{FE(c)}$

$h_{FE(o)}$	the value of $h_{FE(c)}$ with zero control voltage relative to the emitter
I_B	terminal base current
$I_B(V_E,V_C,V_{CS})$	terminal base current with voltage dependence explicitly indicated
$I_{B(C)}$	current injected to the base due to collector segment voltage
$I_{B(CS)}$	current injected to the base due to control segment voltage
$I_{B(E)}$	current injected to the base due to emitter voltage
I_C	lateral current injected by the collector segment, a fraction of which reaches only the emitter
I_C'	lateral current injected by the collector segment, a fraction of which reaches only the control segment by way of the segment gaps
$I_{C(CS)}$	current reaching the collector due to control segment voltage
$I_{C(E)}$	current reaching the collector due to emitter voltage
I_{CV}	vertically injected current from the collector which divides between base and substrate
$I_C(V_E,V_C,V_{CS})$	terminal collector current
I_{CS}	lateral current injected by the control segment, a fraction of which reaches only the emitter
I_{CS}'	lateral current injected by the control segment, a fraction of which reaches only the collector segment by way of the segment gaps
$I_{CS(C)}$	current reaching the control segment due to collector segment voltage

$I_{CS(E)}$	current reaching the control segment due to emitter voltage
I_{CSV}	vertically injected current from the control segment which divides between base and substrate
$I_{CS}(V_E,V_C,V_{CS})$	terminal control segment current
I_E	lateral current injected by the emitter from the area A_E
I_E'	laterally collected current, injected by the emitter from the area A_E'
I_{EL}	the total laterally collected current from emitter injection ($= I_E + I_E'$)
$I_{E(C)}$	current reaching the emitter due to collector segment voltage
$I_{E(CS)}$	current reaching the emitter due to control segment voltage
I_{EV}	vertically injected current from the emitter which divides between base and substrate
$I_E(V_E,V_C,V_{CS})$	terminal emitter current
$I_{S(C)}$	current reaching the substrate due to collector segment voltage
$I_{S(CS)}$	current reaching the substrate due to control segment voltage
$I_{S(E)}$	current reaching the substrate due to emitter voltage
$I_S(V_E,V_C,V_{CS})$	terminal substrate current
J	current density
J_p	current density due to hole injection
k	Boltzmann's constant
L_n	diffusion length for electrons in the p-region
L_p	diffusion length for holes in the n-region

N_A	acceptor concentration
N_D	donor concentration
n_{po}	thermal equilibrium value of electron concentration in the p-region
p	inner perimeter of the complete collector
p'	inner perimeter of the control segment
p_{no}	thermal equilibrium value of hole concentration in the n-region
q	electronic charge
r	arbitrary radius from centre of symmetry
r_E	radius of emitter as defined on the mask
T	temperature (^oK)
V_A	"Early" voltage
V_C, or V_{CB}	collector segment - base voltage
V_{CE}	collector segment - emitter voltage
V_{CS}, or V_{CSB}	control segment - base voltage
V_{CSE}	control segment - emitter voltage
$V_{CSE(o)}$	control segment voltage which results in zero net control segment current, or emitter current, depending on the conditions
V_E, or V_{EB}	emitter - base voltage
V_j	junction voltage
V_T, or kT/q	thermal voltage
w	arbitrary vertical distance as in Fig. 2.
w_1	effective constant base width for the upper half of the diffusion profile
w_o	base width as defined on the mask
w_s	segment width as defined on the mask
w_v	effective vertical diffusion length as defined in equation (6)
x_j	junction depth
x_j'	junction depth including rev. bias depletion layer width

α_F	mean value of common-base dc current gain in the forward mode, for the lateral transistor
α_o	value of α_F with zero bias
α_P	mean value of common-base dc current gain in the forward mode for the parasitic substrate p-n-p transistor
α_R	mean value of common-base dc current gain in the reverse mode, for the lateral transistor
β_F	mean value of common-emitter dc current gain in the forward mode, for the lateral non-segmented form of the transistor
$\beta_{F(S)}$	value of β_F for the stabilised connection of the segmented lateral transistor
β_o	value of β_F for zero collector bias
β_R	mean value of common-emitter dc current gain in the reverse mode, for the lateral non-segmented form of the transistor
β_R^*	value of β_R for the segmented transistor in reverse mode, where the control segment is emitting and the emitter is shorted to the collector segment
θ	arbitrary angle

INTRODUCTION

One of the main difficulties associated with an attempt to analyse the behaviour of the p–n–p lateral transistor, is that one-dimensional expressions are being applied to a structure which undoubtedly behaves three dimensionally as far as current flow is concerned. This is particularly the case for lateral devices of circular geometry illustrated in Figure 1, which are the subject of this paper.

Several analyses have been carried out for lateral devices, but the results have not been found particularly useful in their application to the segmented lateral structure. The approach taken here has been to make reasonable approximations regarding the circular configuration, and reasonable assumptions regarding the properties of the current flow, in order to obtain a tractable solution which includes first-order effects.

In certain respects, the p–n–p lateral transistor is easier to consider than the vertical n–p–n transistor in view of the symmetry introduced by the simultaneous diffusion of emitter and collector through a single mask. In addition the effective base width in the lateral direction becomes well controlled, in spite of the fact that base-width modulation becomes more pronounced because of the lighter doping levels, and proportionately wider depletion regions. In other respects, the structure of the p–n–p transistor needed for it to interface with other devices on the same integrated circuit substrate can cause problems:

1. The base contact has to be made in a region outside the collector segments (Figure 1) and the n^+ buried-layer acts as a distributed connection between base contact and n epi-layer. The built-in field resulting from this graded n-type region opposes the flow of injected holes from the p^+ emitter in a vertical direction, thereby reducing to some extent the effect of the parasitic p–n–p vertical transistor formed with the substrate. However the n^+ buried-layer diffuses

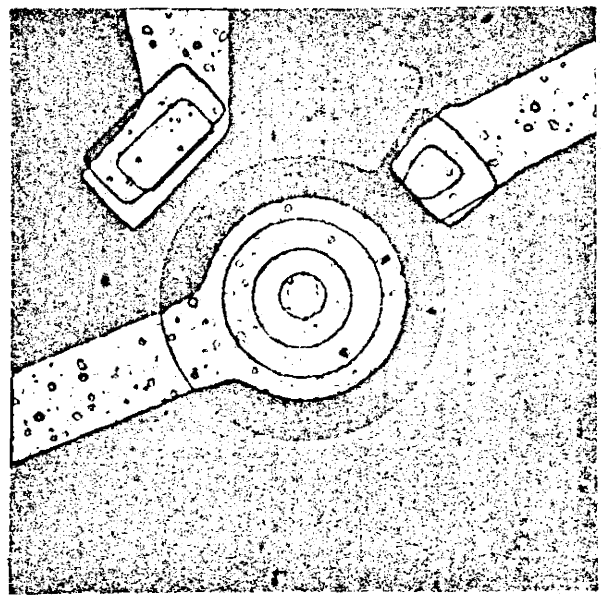

Figure 1(a). Non-segmented p-n-p lateral transistor Q30.

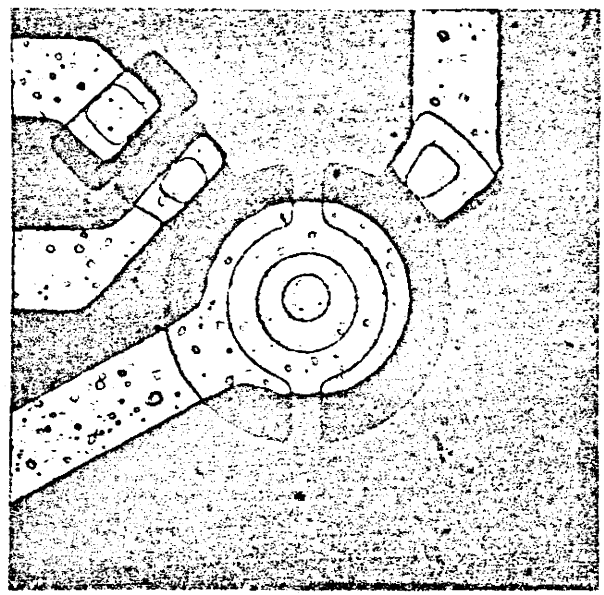

Figure 1(b). Equal-segment p-n-p lateral transistor Q31.

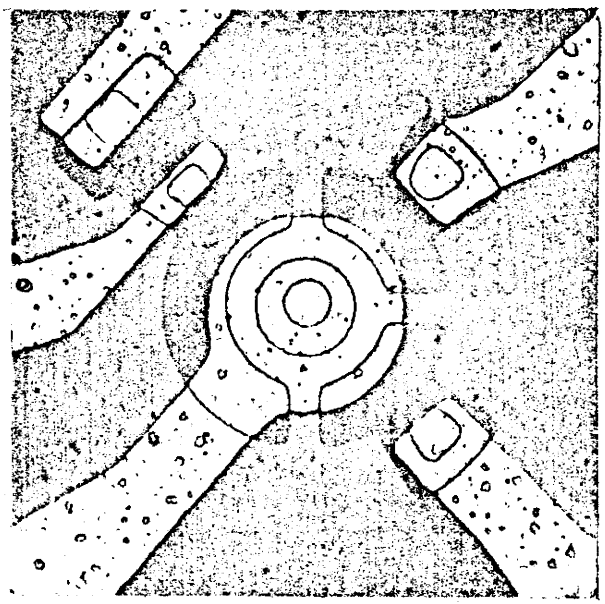

Figure 1(c). A segmented p–n–p lateral transistor which can be connected with a control segment:collector segment ratio of 1:3 (Q34a) or 3:1 (Q34b).

upward into the n epi-layer during subsequent processing resulting in a region of higher recombination below the floor of the emitter and collector regions. As a consequence of this it seems that a fraction of the emitted current which originates from the floor of the region contributes to base current directly, while another fraction may reach the substrate beneath.

2. The doping levels for the p-n-p lateral transistor result from the optimisation of the base and collector regions of the n-p-n devices. Although it is usual to discount the effect of back-injection from base to emitter and set the injection efficiency equal to unity, this may not be as good an approximation in all cases for the p-n-p device. Another effect which is unique for the lateral p-n-p transistor is the equal doping level for emitter and collector, which results in acceptable injection in the inverse mode.
3. There is considerable lateral diffusion of the p^+ isolation walls during subsequent processing. This would normally cause no problem since they are connected to the substrate and become reverse-biased in the usual way, and are physically further than a diffusion length from the emitter. However in the inverse mode or in saturation, the effects of this lateral diffusion coupled with the relatively wide reverse-biased depletion region may well bring a collecting boundary within a diffusion length of the forward-biased collector segment. This is especially true of the collector segment lobes used to make connection. In the devices illustrated in Figure 1, substrate current of the order of magnitude of the base current was observed when the collector segments are driven into saturation.

It is usual in the analysis of any lateral structure to assume that the shape of the diffusion profile which results from lateral

diffusion beneath the protective oxide is that of a quadrant, particularly if the background doping is uniform as is usually assumed for an epi-layer. Analytic expressions have been obtained for the shape of the profile in the case where the background doping is non-uniform; the results indicate that the effect is to make that part of the side-wall nearest the surface more cylindrical in the case of circular geometry. In view of the processing conditions for the p-n-p lateral transistor, however, the profile is assumed to be a quadrant.

Another assumption that is frequently adopted is that current flows either horizontally or vertically, with current emitted from the side-walls being assumed collectable while that emitted from the floor of the emitting region is assumed lost to the substrate. In the case of the p-n-p lateral transistor of circular geometry, this assumption is not adequate. Figure 2 illustrates a half-section of a proposed analogue based upon the actual geometry of the devices shown in Figure 1, and which includes the narrowing of the base caused by the depletion regions. Consideration of this analogue leads to the following conclusions:

1. Injection is most efficient close to the surface where the minority carrier concentration gradient is greatest, and diminishes towards the emitter floor.
2. The n^+ buried-layer diffuses upward into the epi-layer, so greater recombination begins at a distance 'w' below the emitter floor; it is possible for carriers emitted vertically from an annulus of width $\approx w$, to be collected laterally if $w + x_j \leq \frac{1}{2}L_p$, where L_p is the diffusion length for lateral flow in the n epi-layer.
3. Carriers emitted vertically from the emitter floor at distances greater than $\frac{1}{2}L_p$ from the collector/base junction are more likely to recombine in the n^+ region and contribute to base current, or reach the p substrate of the vertical parasitic transistor as substrate current. Either process results in degradation of the lateral h_{FE}.

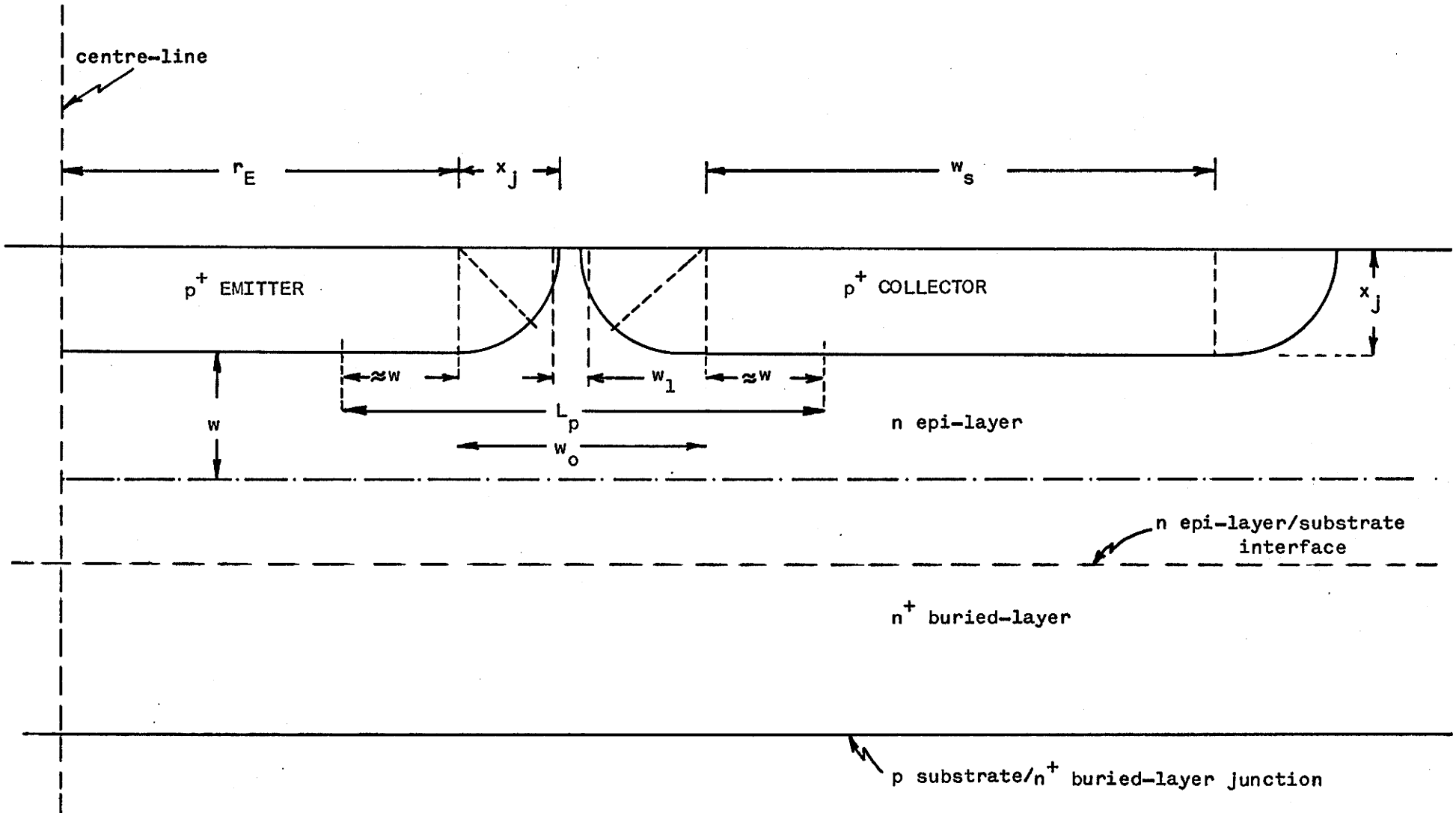

Figure 2. An analogue representing the main structural features of the p-n-p lateral transistor.
(Only one half-section is illustrated)

4. The emitting surface can be subdivided into three main areas (Figure 3(a)) each with its own emitter current component. The effective base width for the dominant current I_E is assumed to be the distance marked w_1; this corresponds to the spacing between depletion regions about a quarter of the distance from surface to floor measured along the curved profile. For the component I_E' which is injected vertically but assumed to travel horizontally, the effective base width is taken to be that of the mask base width, w_o, while the component I_{EV} is assumed to have an effective base width corresponding to the diffusion length in the vertical direction, w_v.(see FORMULATION)
5. The total collecting surface can be subdivided in a similar way as illustrated in Figure 3(b), where the circular areas are denoted by A_C, A_C' and A_C''. The upper half of the profile of the inner collecting side-wall corresponds to A_C; the area A_C' includes the lower half of this same profile together with an annulus from the collecting floor of width $\frac{L_P - w_o}{2}$. The outer curved side-wall is lumped together with the remaining floor area and denoted by A_C''.
6. The fraction of each of these areas appropriate to the control segment is denoted by the ratio p'/p, where p' is the length of the inner side-wall of the control segment at the surface and p is the inner side-wall perimeter.
7. The diagram on the right-hand side of Figure 3(b) illustrates a subdivision of the control segment on the following basis:
   (a) Current component I_{CS} is assumed to be composed of injection from two areas (unshaded in the Figure) which together make up the whole of the inner side-wall plus the floor annulus of width w, and the whole of this component I_{CS} is assumed to flow only towards the emitter.
   (b) Current component I_{CS}' is also assumed to be

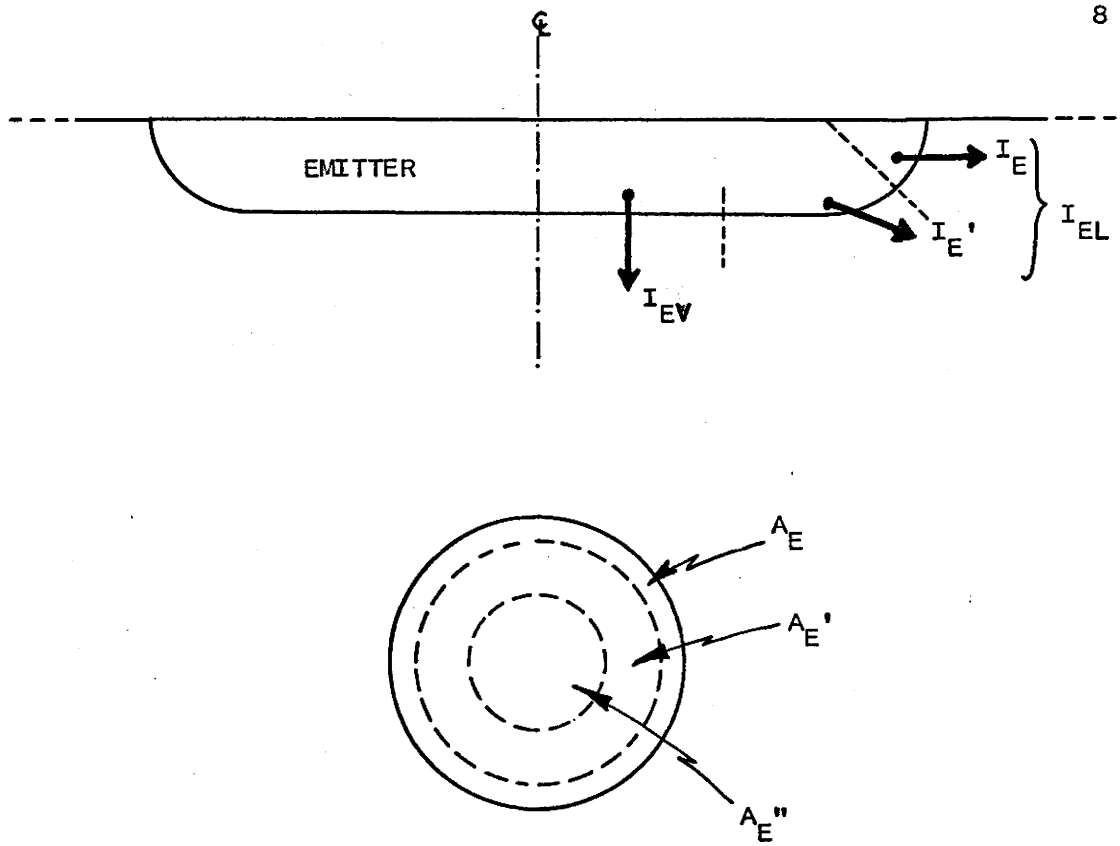

Figure 3(a). The components of emitter current used in the model and the corresponding geometrical areas.

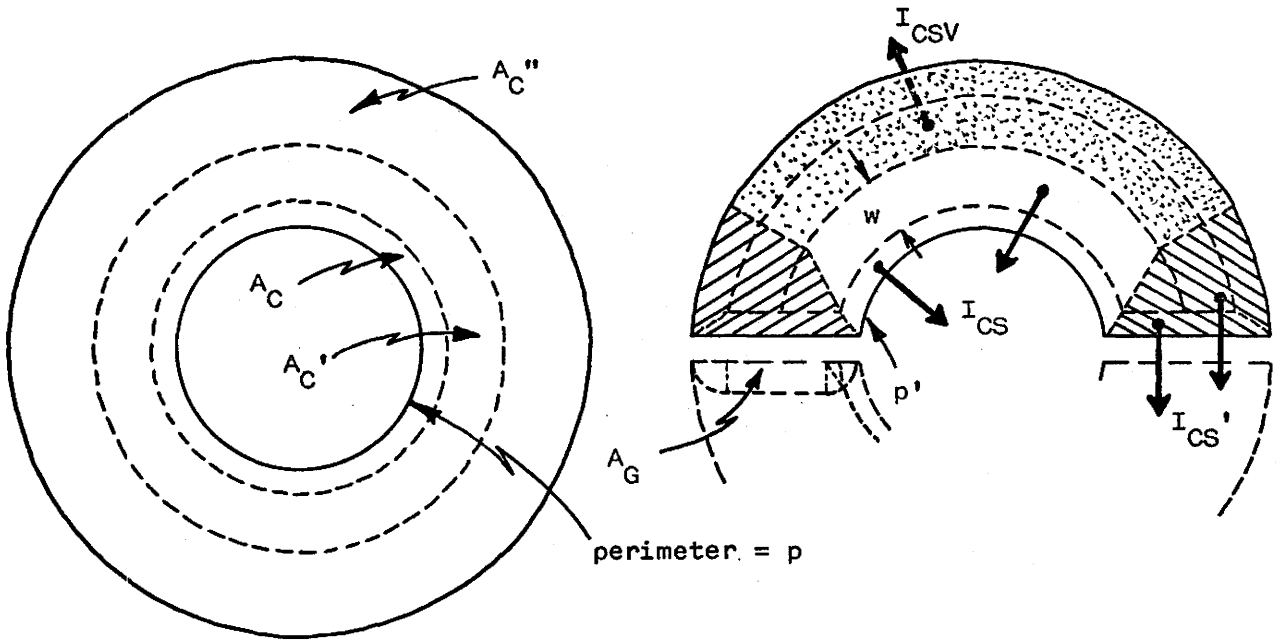

Figure 3(b). The current components with control segment emitting, and the notation used in defining the areas involved.

composed of injection from two areas (shown cross-hatched), one on each side of the control segment. The dominant portion of I_{CS}' consists of injection from the two quarter-cylinder surfaces of the gap faces (ignoring the small corner fillets) with the remainder made up of injection from an appropriate fraction of $A_C' + A_C''$ as suggested in the diagram. I_{CS}' flows only towards the collector.

(c) Current component I_{CSV} is emitted vertically downwards from the remaining area of the control segment (the dotted area of the Figure), and is assumed to be lost either as base current or substrate current in the same manner as described for I_{EV}.

Although the subdivision described in (a), (b), and (c) above is somewhat arbitrary, the proportions appear to be reasonable from the results of measurements described later.

8. When the collector segment is being considered, the same arguments apply except that the expression $1-p'/p$ replaces p'/p where it appears, and the "S" subscript is dropped from the current components. The terms "control-segment" and "collector-segment" are completely interchangeable, but the distinction by way of subscripts avoids confusion of roles since they are biased quite differently at times.

In the next section, the Ebers-Moll equations are developed from the model illustrated in Figure 4, and which applies to the case of a dual segment p-n-p lateral transistor. The model can easily be generalised for a transistor having more than two segments, with each one biased arbitrarily. It is clear that the number of component currents could be increased from the three employed here and computer solution invoked. However, the central interest in this paper concerns a controlled-gain device, and the analysis carried out with this specific end in view, so that a tractable solution could be obtained with manual computation.

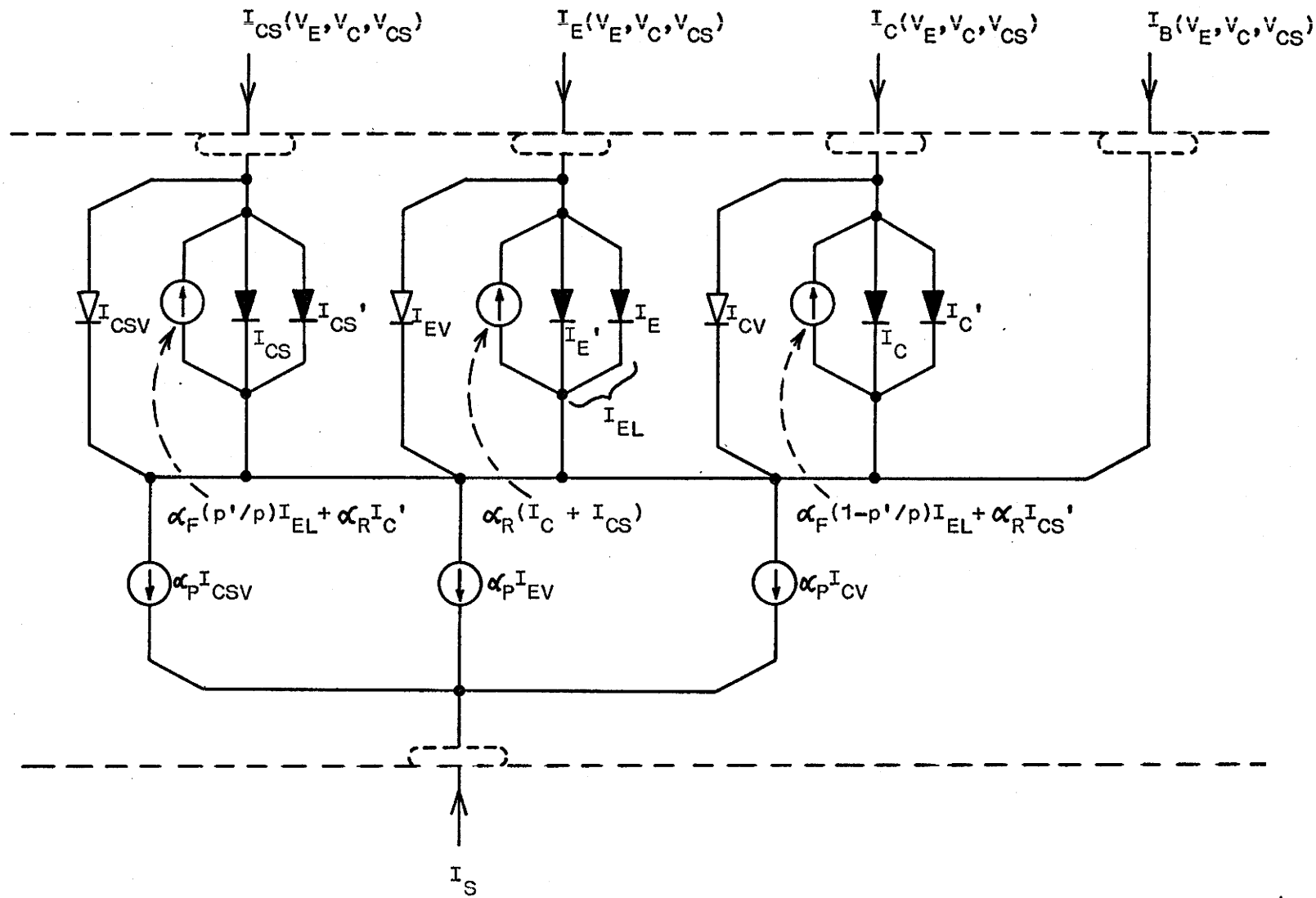

Figure 4. An "Ebers-Moll" type of model developed for the dual-segment p-n-p lateral transistor.

FORMULATION

The analysis which follows is based upon the following assumptions:

1. A one-dimensional expression for diffusion current is adequate under the conditions cited - the Shockley equation.
2. Low-level injection conditions.
3. Abrupt p^+/n junctions with electric fields confined to their transition regions.
4. Quasi-neutral regions on either side of a junction.
5. Recombination/generation currents from the depletion regions are negligible compared with the diffusion components.
6. Surface effects and other leakage currents which do not cross junctions are assumed to be negligible.
7. Validity of the Boltzmann approximation and also the Einstein relation.
8. The only source of carrier generation is thermal.
9. Only a dc analysis is attempted.

The ideal current/voltage relationship for a p-n junction is given by

$$J = \left[\frac{qD_p p_{no}}{L_p} + \frac{qD_n n_{po}}{L_n}\right] \exp(V_j/V_T - 1) \qquad (1)$$

in the case of a long diode, where:

q = electronic charge
L_p = diffusion length for holes in the n-region
L_n = diffusion length for electrons in the p-region
D_p = diffusivity for holes in the n-region
D_n = diffusivity for electrons in the p-region
p_{no} = thermal equilibrium value of hole concentration in the n-region

n_{po} = thermal equilibrium value of electron concentration in the p-region

J = total current density

V_j = junction voltage

V_T = thermal voltage = kT/q

For devices of practical interest, and in particular for the p-n-p lateral transistors considered here, the emitter doping level $N_A \approx 10^{18} cm^{-3}$ and the epi-layer (base) doping level $N_D \approx 5 \times 10^{15} cm^{-3}$.
Therefore $n_{po} \ll p_{no}$, and (1) can be written:

$$J = J_p . \exp(V_j/V_T - 1) \tag{2}$$

where $$J_p = \frac{qD_p p_{no}}{L_p} \tag{3}$$

Consider the emitter injection for the proposed analogue, (Figure 3(a)). An expression for the component I_E can be derived from (2) & (3) by specializing it to the case of a short diode of effective base width w_1:

$$I_E = \frac{J_p L_p A_E}{w_1} . \exp V_E/V_T \tag{4}$$

where it is assumed that the emitter-base junction and terminal voltages can be interchanged and that $V_E >> V_T$. Unless otherwise stated, all voltages are stated with respect to the base as reference.
A similar expression is obtained for I_E':

$$I_E' = \frac{J_p L_p A_E'}{w_o} . \exp V_E/V_T \tag{5}$$

The magnitude of the current I_{EV} depends on the gradient of the electro-chemical potential since a retarding field exists in the vertical direction.

The expression for I_{EV} can be written in the form:

$$I_{EV} = \frac{J_p L_p A_E''}{w_v} \cdot \exp V_E/V_T \qquad (6)$$

where it is assumed that the combined effect of the retarding field in the vertical direction and the gradient of the carrier concentration can be represented by an effective diffusion length w_v, which is likely to be of the same order as L_p. However, since $w_v > w_o \gg w_1$ which makes $I_{EV} \ll I_E$, I_E', the error involved in taking a numerical value for w_v equal to that of L_p in a first approximation may not appear significant.

The total laterally injected current, $I_E + I_E'$, will be denoted by I_{EL} in what follows. The collectable part of this current will be less than I_{EL} because of recombination in a region of the base which varies continuously in width. (This is irrespective of the modulation of base width caused by changes in the reverse bias on the collector segment(s).) Therefore, it becomes necessary to define an "average" common-base short-circuit current gain, α_F, which describes the base transport under these circumstances. If the fraction of injected current $\alpha_F I_{EL}$ does not recombine, and it is assumed that this current subsequently divides in the ratio of the inner peripheries of the collecting segments, the following expressions can be written for the control segment current $I_{CS(E)}$ and collector segment current $I_{C(E)}$ due to the emitter-base voltage:

$$I_{CS(E)} = \alpha_F (p'/p) I_{EL} \qquad (7)$$

$$I_{C(E)} = \alpha_F (1 - p'/p) I_{EL} \qquad (8)$$

Current I_{EV} represents the emitter injection for the vertical p-n-p parasitic transistor, with the substrate as collector. If α_P represents the common-base short-circuit current gain of this transistor, the substrate current $I_{S(E)}$ and base current contribution $I_{B(E)}$ due to the emitter-base voltage can be written:

$$I_{S(E)} = \alpha_P I_{EV} \tag{9}$$

$$I_{B(E)} = (1 - \alpha_P) I_{EV} + (1 - \alpha_F) I_{EL} \tag{10}$$

Suppose that conditions are such that the control segment or collector segment becomes forward biased; because of the symmetry imposed by the processing of the p-n-p lateral transistor, J_p and L_p remain the same for this injection. The equations can be set up in a similar manner to that of the emitter, the only complication being the arbitrary assumption for the way in which the current divides between the collector segment and the normal emitter if, for example, the control segment is in saturation.(This was discussed earlier on in this paper) Assuming that the control segment-base junction and terminal voltages can be interchanged, then the following expressions are obtained for the current components I_{CS}, I_{CS}' & I_{CSV}:

$$I_{CS} = J_p L_p \left[\frac{p' A_C}{p w_1} + \frac{(p' - L_p/2) A_C'}{p w_o} \right] \exp(V_{CS}/V_T - 1) \tag{11}$$

$$I_{CS}' = J_p L_p \left[\frac{A_G}{w_1} + \frac{L_p/2}{p} \cdot \frac{A_C'}{w_o} + \frac{L_p}{p} \cdot \frac{A_C''}{w_v} \right] \exp(V_{CS}/V_T - 1) \tag{12}$$

$$I_{CSV} = J_p L_p \frac{(p' - L_p)}{p} \cdot \frac{A_C''}{w_v} \cdot \exp(V_{CS}/V_T - 1) \tag{13}$$

Note: For these equations to apply to the case of collector segment injection, it is only necessary to drop the "S" subscript from the notation for current and voltage, and replace p' by p - p'.

The same comments apply to the use of w_v in (13) as they did for (6).

With reference to Figure 3(b), the current $\alpha_R I_{CS}$ survives recombination and reaches the normal emitter while the current $\alpha_R I_{CS}'$ reaches the collector segment. α_R is defined as the mean value of common-base short-circuit current gain when operated in the inverse mode, on the same basis as α_F in the normal mode.

The following expressions are therefore obtained for the emitter current $I_{E(CS)}$ and collector segment current $I_{C(CS)}$ due to the control segment-base voltage only:

$$I_{E(CS)} = \alpha_R I_{CS} \tag{14}$$

$$I_{C(CS)} = \alpha_R I_{CS}' \tag{15}$$

Expressions for the substrate current $I_{S(CS)}$ and base current $I_{B(CS)}$ resulting from the parasitic vertical p-n-p transistor formed with the control segment as emitter and the substrate as collector are derived from I_{CSV} as follows:

$$I_{S(CS)} = \alpha_P I_{CSV} \tag{16}$$

$$I_{B(CS)} = (1 - \alpha_P) I_{CSV} + (1 - \alpha_R)(I_{CS} + I_{CS}') \tag{17}$$

where the current components with subscripts in parentheses are those due only to control segment-base voltage.

Note: For equations (14) through (17) to apply to the case of collector segment injection, the "S" subscript is dropped from the notation. (except the left side of (15) which would become $I_{CS(C)}$)

The various current components can now be used to assemble the model illustrated in Figure 4, and Kirchhoff's current law used to write the modified Ebers-Moll expressions for the five terminal currents:

$$\underline{I_E(V_E,V_C,V_{CS})} = (I_{EL} + I_{EV}) - I_{E(C)} - I_{E(CS)}$$

$$= \underline{(I_{EL} + I_{EV}) - \alpha_R I_C - \alpha_R I_{CS}} \qquad \text{(from (14))} \qquad (18)$$

$$\underline{I_C(V_E,V_C,V_{CS})} = -I_{C(E)} + (I_C + I_C' + I_{CV}) - I_{C(CS)}$$

$$= \underline{-\alpha_F(1 - p'/p)I_{EL} + (I_C + I_C' + I_{CV}) - \alpha_R I_{CS}'} \qquad (19)$$

(from (8) & (15))

$$\underline{I_{CS}(V_E,V_C,V_{CS})} = -I_{CS(E)} - I_{CS(C)} + (I_{CS} + I_{CS}' + I_{CSV})$$

$$= \underline{-\alpha_F(p'/p)I_{EL} - \alpha_R I_C' + (I_{CS} + I_{CS}' + I_{CSV})} \qquad (20)$$

(from (7))

$$\underline{I_B(V_E,V_C,V_{CS})} = -(I_{B(E)} + I_{B(C)} + I_{B(CS)})$$

$$= -\Big[\underline{(1 - \alpha_F)I_{EL} + (1 - \alpha_P)I_{EV}} + \underline{(1 - \alpha_R)(I_C + I_C') + (1 - \alpha_P)I_{CV}} + \underline{(1 - \alpha_R)(I_{CS} + I_{CS}') + (1 - \alpha_P)I_{CSV}}\Big] \qquad (21)$$

(from (10) & (17))

$$\underline{I_S(V_E,V_C,V_{CS})} = -(I_{S(E)} + I_{S(C)} + I_{S(CS)})$$

$$= \underline{-\alpha_P(I_{EV} + I_{CV} + I_{CSV})} \qquad (22)$$

(from (9) & (16))

The relationships between the current components in these expressions

and the terminal voltages are provided by equations (4), (5), (6), (11), (12), (13) and their equivalents for collector segment injection where appropriate. Equations (18) through (22) are written in a form which assumes throughout that the substrate is biased to a negative potential which is always several kT/q more than the reverse bias on any collecting segment; were this not so, there would be the possibility of injection from the p^+ isolation walls to such segments.

Application of the Model to the Controlled Gain Transistor

The intention here is to derive an expression for the common-emitter current gain to the collector segment of the p-n-p lateral transistor which is biased to a suitable negative voltage, in terms of the arbitrary bias voltage on the control segment with respect to the emitter. In all cases, the requirement that $V_E >> V_T$ and $V_C << -V_T$ is to be understood, so that in equations (18) through (22) all terms with subscript "C" can be ignored; to simplify the notation in what follows the functional dependence on voltage for terminal currents will not be explicitly stated in the equations.

The common-emitter current gain of the controlled transistor, $h_{FE(c)}$, is obtained for arbitrary control segment voltage with respect to the base (V_{CS}), from the ratio of (19) and (21):

$$h_{FE(c)} = \frac{\alpha_F(1 - p'/p)I_{EL} + \alpha_R I_{CS}'}{(1 - \alpha_F)I_{EL} + (1 - \alpha_P)I_{EV} + (1 - \alpha_R)(I_{CS} + I_{CS}') + (1 - \alpha_P)I_{CSV}} \qquad (23)$$

It is convenient to define two special cases with the aid of this expression:

(i) $V_{CS} = 0$; (to be precise, $V_C = 0$ also)

(ii) $V_{CS} >> V_E$; (" " " " " " ")

Case (i) gives a maximum controlled value for the common-emitter current gain, $h_{FE(max.c.)}$, where

$$h_{FE(max.c.)} = \frac{\alpha_F(1 - p'/p)I_{EL}}{(1 - \alpha_F)I_{EL} + (1 - \alpha_P)I_{EV}} \qquad (24)$$

It is instructive to compare (24) with an expression for the common-emitter current gain of the transistor when both segments are connected together and $V_{CS} = V_C = 0$; this is the normal forward beta (β_F) of the non-segmented transistor, and the expression obtained from (19), (20) and (21):

$$\beta_F = \frac{\alpha_F I_{EL}}{(1 - \alpha_F)I_{EL} + (1 - \alpha_P)I_{EV}} \qquad (25)$$

Therefore, from (24):

$$h_{FE(max.c.)} = (1 - p'/p)\beta_F \qquad (26)$$

Case (ii) gives a minimum controlled value for the common-emitter current gain, $h_{FE(min.c.)}$, where

$$h_{FE(min.c.)} = \frac{\alpha_R I_{CS}'}{(1 - \alpha_R)(I_{CS} + I_{CS}') + (1 - \alpha_P)I_{CSV}} \qquad (27)$$

Equation (27) can be compared with a particular value of common-emitter current gain defined under the conditions where the collector and emitter are shorted and $V_E = V_C = 0$; the transistor is operated in the inverse mode with the control segment acting as the emitter. The symbol β_R^* is used to denote this current gain, to distinguish it from the true reverse beta which would result from the conditions $V_C = V_{CS} >> V_T$ and $V_E = 0$. The expression for β_R^* is obtained from (18),(19) & (21):

$$\beta_R^* = \frac{\alpha_R(I_{CS} + I_{CS}')}{(1-\alpha_R)(I_{CS} + I_{CS}') + (1-\alpha_P)I_{CSV}} \tag{28}$$

Equating the denominators of (27) & (28):

$$\beta_R^* = (1 + I_{CS}/I_{CS}')\, h_{FE(min.c.)} \tag{29}$$

The usefulness of (29) centres on the fact that β_R^* and $h_{FE(min.c.)}$ are both directly measurable, enabling the division of current between emitter and collector to be determined.

It is now possible to re-write (23) in terms of the parameters defined in (24) & (27) as follows:

$$h_{FE(c)} = \frac{\alpha_F(1 - p'/p)I_{EL} + \alpha_R I_{CS}'}{\dfrac{\alpha_F(1 - p'/p)I_{EL}}{h_{FE(max.c.)}} + \dfrac{\alpha_R I_{CS}'}{h_{FE(min.c.)}}}$$

$$= \frac{1 + \left[\dfrac{\alpha_R}{\alpha_F}\cdot\dfrac{p}{p - p'}\right](I_{CS}'/I_{EL})}{1/h_{FE(max.c.)} + 1/h_{FE(min.c.)}\left[\dfrac{\alpha_R}{\alpha_F}\cdot\dfrac{p}{p - p'}\right](I_{CS}'/I_{EL})} \tag{30}$$

Equations (4), (5) & (12) can be used to relate the ratio I_{CS}'/I_{EL} to the voltage of the control segment relative to the emitter by noting that if it is several kT/q more positive than $-V_{EB}$, then to a reasonable approximation,

$$\frac{\exp(V_{CS}/V_T - 1)}{\exp(V_E/V_T)} = \exp(V_{CS} - V_E)/V_T = \exp V_{CSE}/V_T \tag{31}$$

where V_{CSE} denotes the control segment voltage, relative to the emitter.

Under these conditions:

$$I_{CS}'/I_{EL} = A \cdot \exp V_{CSE}/V_T \tag{32}$$

where the coefficient 'A' is given by:

$$A = \frac{\frac{A_G}{w_1} + \frac{L_p/2}{p} \cdot \frac{A_C'}{w_o} + \frac{L_p}{p} \cdot \frac{A_C''}{w_v}}{\frac{A_E}{w_1} + \frac{A_E'}{w_o}} \tag{33}$$

Substituting (32) into (30):

$$h_{FE(c)} = \frac{1 + \frac{\alpha_R}{\alpha_F}\left[\frac{p}{p - p'}\right] A \exp V_{CSE}/V_T}{h_{FE(max.c.)}^{-1} + h_{FE(min.c.)}^{-1} \frac{\alpha_R}{\alpha_F}\left[\frac{p}{p - p'}\right] A \exp V_{CSE}/V_T} \tag{34}$$

It is convenient to define another special case to avoid the product appearing before the exponent:

Case (iii) gives a value for the controlled common-emitter current gain, $h_{FE(o)}$, under the conditions where the control segment and emitter are shorted together to make $V_{CSE} = 0$, and the transistor is operated in forward mode. Then, from (34):

$$h_{FE(o)} = (1 + B)/ h_{FE(max.c.)}^{-1} + B \cdot h_{FE(min.c.)}^{-1} \tag{35}$$

where the coefficient 'B' is given by:

$$B = \frac{\alpha_R}{\alpha_F}\left[\frac{p}{p - p'}\right] A \tag{36}$$

Solving for the coefficient 'B' in (35) gives:

$$B = \frac{h_{FE(min.c.)}}{h_{FE(max.c.)}}\left[\frac{h_{FE(max.c.)} - h_{FE(o)}}{h_{FE(o)} - h_{FE(min.c.)}}\right] \qquad (37)$$

and substitution of (36) & (37) back into (34) gives the required expression for controlled current gain:

$$h_{FE(c)} = h_{FE(max.c.)}\left[\frac{1 + \left[\frac{h_{FE(min.c.)}}{h_{FE(max.c.)}}\right]\left[\frac{h_{FE(max.c.)} - h_{FE(o)}}{h_{FE(o)} - h_{FE(min.c.)}}\right]\exp V_{CSE}/V_T}{1 + \left[\frac{h_{FE(max.c.)} - h_{FE(o)}}{h_{FE(o)} - h_{FE(min.c.)}}\right]\exp V_{CSE}/V_T}\right] \qquad (38)$$

The form of equation (38) suggests that the voltage V_{CSE} modulates the controlled common-emitter current gain between the limiting values $h_{FE(max.c.)}$, when $V_{CSE} \ll -V_T$, and $h_{FE(min.c.)}$, when $V_{CSE} \gg V_T$, and that $h_{FE(c)}$ is a very sensitive function of V_{CSE}. Furthermore, when $V_{CSE} = 0$, $h_{FE(c)} \longrightarrow h_{FE(o)}$.

The validity of (38) has been checked by experiment using the p-n-p segmented lateral transistors illustrated in Figure 1, and the procedure described in the following section. Considering the assumption that α_F, α_R, and α_P were not functions of current injection level or terminal voltage, the agreement between theory and experiment appears adequate. The common-base short-circuit current gains can be multiplied by a factor which is a function of the appropriate terminal voltage and an 'Early' voltage factor in order to account for the rather severe base-width modulation effects for the lateral p-n-p transistor, and where the collector segment reverse bias no longer remains constant. (Figure 8.)

Further consideration of equations (18) and (20) indicates that two conditions exist which enable the validity of the ratio of certain geometrical parameters to be checked, or a separate check on the ratio α_R/α_F to be made:

Case (iv) The condition of zero net terminal current at the control segment, with negative collector segment voltage.

From (20), setting the left side to zero, and using (4),(5),(11), (12) & (13), the following expression can be obtained:

$$\alpha_F \Big|_{I_{CS} = 0} = \left[\frac{\frac{A_C}{w_1} + \frac{A_C'}{w_o} + \frac{A_C''}{w_v} + (p/p')\frac{A_G}{w_1}}{\frac{A_E}{w_1} + \frac{A_E'}{w_o}} \right] \exp V_{CSE(o)}/V_T \qquad (39)$$

where $V_{CSE(o)}$ is the particular value of control segment voltage at which $I_{CS} = 0$.

Case (v) The condition of zero net terminal current at the emitter, with negative collector segment voltage.

From (18), setting the left side to zero, and using (4),(5),(6) & (11):

$$\alpha_R \Big|_{I_E = 0} = \left[\frac{\frac{A_E}{w_1} + \frac{A_E'}{w_o} + \frac{A_E''}{w_v}}{\frac{p'A_C}{pw_1} + \frac{(p' - L_p/2)A_C'}{pw_o}} \right] \exp - V_{CSE(o)}/V_T \qquad (40)$$

where $V_{CSE(o)}$ is the particular value of control segment voltage at which $I_E = 0$.

Application of the Model to a Controlled Current Source Transistor

Suppose that the segmented transistor is biased in such a way that it is operating in the forward active region. If equal reverse bias is present at the collecting segments, at least equal to several kT/q, then equations (19) and (20) indicate that:

$$\frac{I_{CS}(V_E,V_C,V_{CS})}{I_C(V_E,V_C,V_{CS})} = \frac{p'/p}{1 - p'/p} \tag{41}$$

Equation (41) illustrates a very simple way of obtaining current division from the segmented lateral transistor; an appropriate periphery ratio is selected to give the necessary proportion. The principle is easily extended to multi-segment devices, and in fact, the Q34 transistor is used in this way.

It is possible to obtain voltage controlled current division by changing the bias on the collecting segments although the sensitivity of this arrangement is probably too great for practical purposes.

The current division is also apparent in the reverse mode, where the control segment is biased several kT/q more positively than the emitter, and the collector segment remaining reverse biased. Under these conditions, the relationship between the terminal currents is far more complex:

$$\frac{I_{CS}(V_E,V_C,V_{CS})}{I_C(V_E,V_C,V_{CS})} = -\frac{(I_{CS} + I_{CS}' + I_{CSV})}{\alpha_R I_{CS}'} \tag{42}$$

The negative sign here indicates the current reversal associated with the control segment, which is now acting as the major emitter. There may be applications where this reversal is not significant, but it is obvious that (41) is the better way of obtaining the current division.

Application of the Model to the Stabilised-Beta Transistor

It is quite common for the spread in β_F for the family of segmented lateral transistors to be about 4:1 from the same wafer, and even greater when comparing different wafers. If a relatively low β_F is adequate (say around 2 $\rightarrow$ 5), but required to be stable to within say, 20%, it is possible to acquire this stability by internal feedback. In this mode of operation, one of the segments is connected directly to the base, and the remaining segment is used as the collector. For a triple-segment transistor such as the Q34, the largest segment is used in this way, and stabilised gain is achieved at both quarter-segment collectors. The same principle applies in the case of the dual-segment types.

With the control segment (for example) acting as the collector in this case, the stabilised common-emitter current gain, $\beta_{F(S)}$, can be obtained by taking the ratio:

$$\beta_{F(S)} \triangleq \frac{I_{CS}}{I_C + I_B} \tag{43}$$

where it is understood that these currents are terminal values, and functions of V_E,V_C & V_{CS}. Suppose that the transistor is operated in the forward active region. Using equations (19), (20), and (21), and making a substitution from (25), it can be shown that:

$$\beta_{F(S)} = \frac{(p'/p)\beta_F}{1 + (1 - p'/p)\beta_F} \tag{44}$$

It is clear from the form of (44) that for periphery ratios in the range of 3/4 to 9/10, the last ratio probably representing an upper practical limit, and for β_F in the range 15 $\rightarrow$ 60, $\beta_{F(S)}$ can be stabilised within about 20% as required.

DEVICE FABRICATION AND MEASUREMENT

The p-n-p lateral transistors tested originate from the integrated circuit LD501, manufactured by Linear Technology Inc. Several circuit chips were die-bonded to TO5 headers, and since a special metallization mask was used to make the lateral transistors accessible for wire bonding, each type of lateral transistor could be selectively bonded to the header pins. One of each of the types designated Q30, Q31, Q34(a) and Q34(b) was selected at random from a sample set prepared from one complete wafer of IC chips. In all other respects, the wafer was typical of those from a normal production run and considered to be a representative sample, prepared in accordance with Process Parameter Specification LD501.

The parameters listed in Table 1 have been determined from photographs (i.e. enlargements of Figure 1) of such devices or calculations based on the parameters in the specification for the LD501. The areas were calculated from the formulae developed in Appendix 1.

Experimental data was obtained from the group of lateral transistors when each was used in the test circuit illustrated in Figure 5. Base current, collector current and control segment current were monitored directly using Philips PM2421 digital multimeters; emitter and substrate currents were determined from the voltages across 1% resistors. All terminal voltages were measured directly with a Fluke digital EVM. The dc power supplies were continuously variable with 1mV sensitivities, and well stabilised. Temperature variation in the laboratory on a day-to-day basis could only be controlled to $22 \pm 2^{o}C$.

To establish suitable operating ranges for the segmented lateral transistors, a non-segmented version, Q30, was tested first. The results of these tests are illustrated in Figures 6,7 & 8, where it is apparent that for collector currents in the range 30 - 50uA it is reasonable to

Table 1.

PARAMETER	REPRESENTATIVE VALUE
r_E	14
x_j	3.6
w_o	8.8
w_s	18
w_1	1.0
w_v	22
L_p	22
A_E	310
A_E'	710
A_E''	170
A_C	400
A_C'	1500
A_C''	4300
A_G	150
p	120
p'	60 (Q31) 30 (Q34a) 90 (Q34b)

Note: Linear dimensions are in μ, and areas are in μ^2.

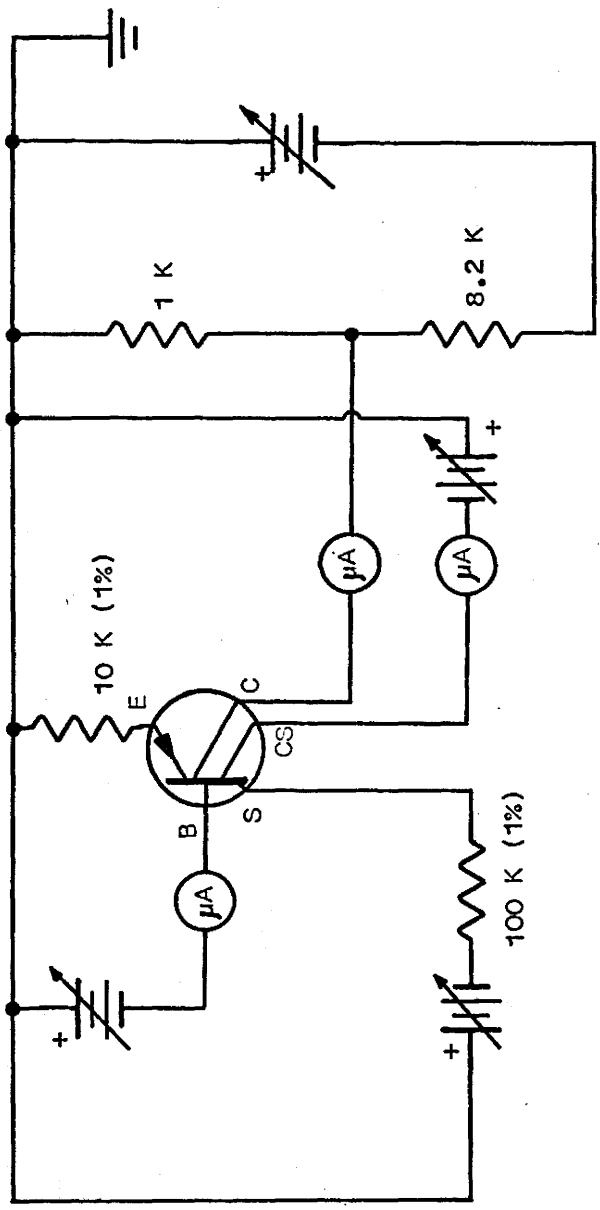

Figure 5. Test Circuit.

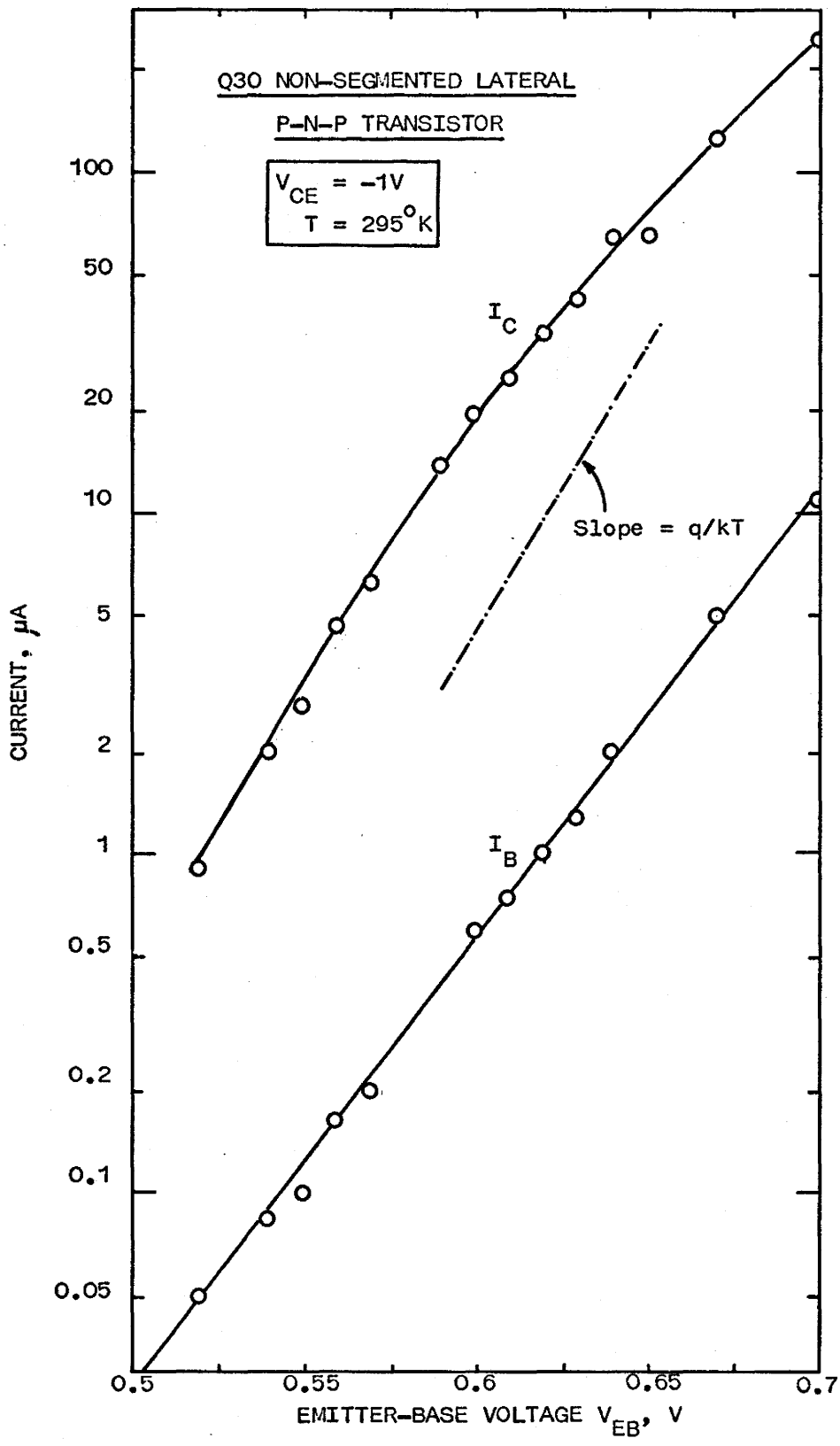

Figure 6. Common-emitter characteristics for the Q30 transistor.

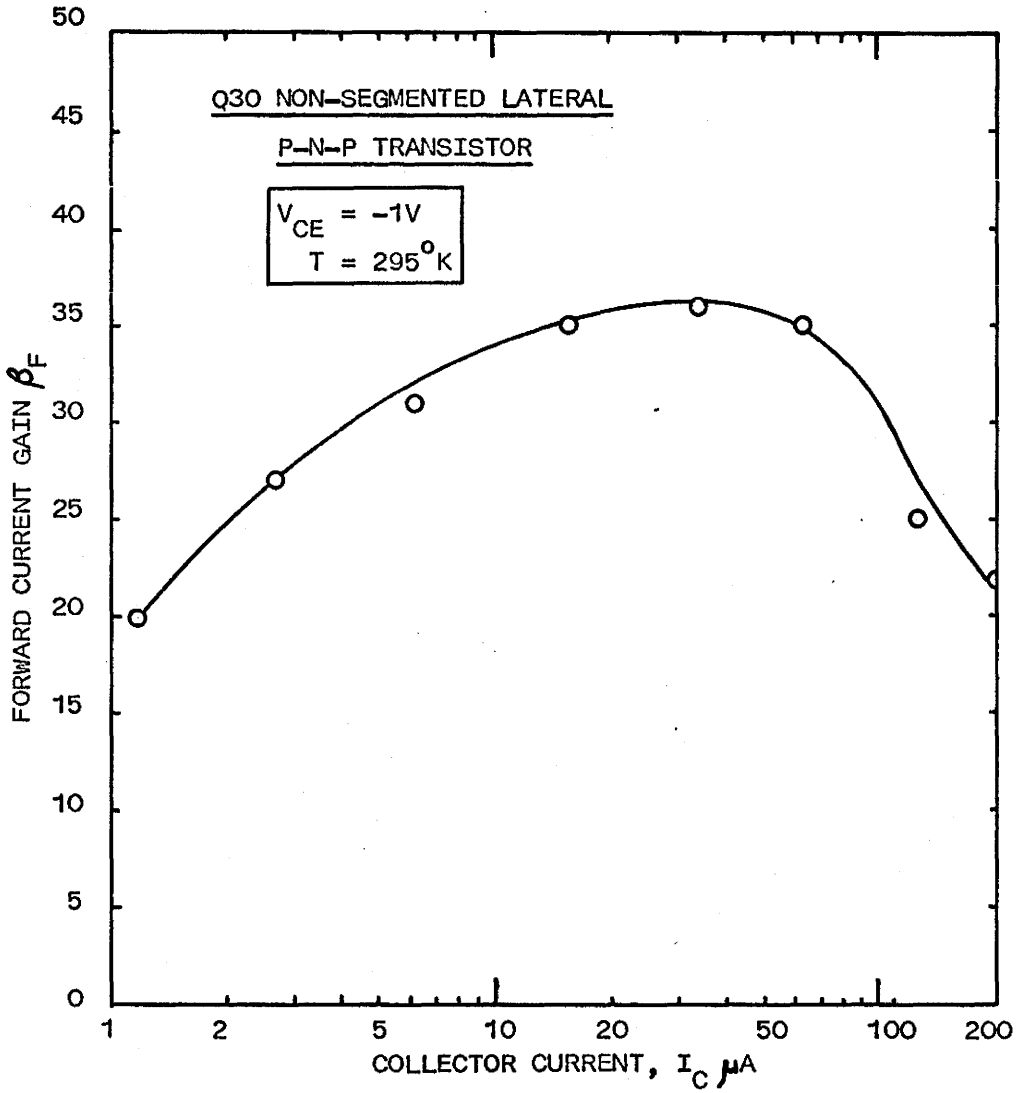

Figure 7. Variation in β_F with collector current for a non-segmented lateral p-n-p transistor.

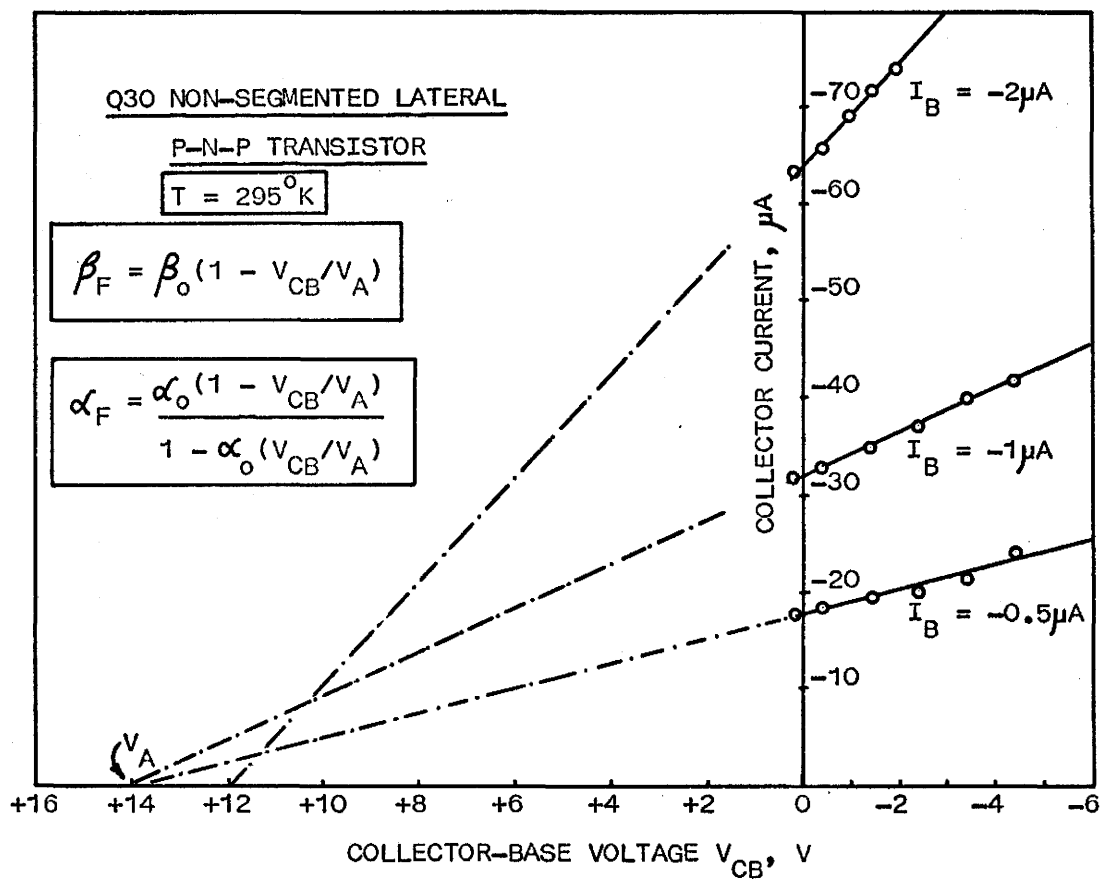

Figure 8. Effect of base-width modulation in the Q30 non-segmented lateral p-n-p transistor. (Early Voltage V_A is illustrated)

assume that β_F is approximately constant, and that equation (1) is an adequate description of the device behaviour in this range. For subsequent tests, the base current was maintained constant at 1μA. Figure 8 shows the effects of base-width modulation and how the value of Early voltage can be obtained; unless separately noted, the collector segment of all transistor types was maintained at a reverse bias of -1V for subsequent tests.

For measurements of the common-emitter controlled current gain, the test conditions for the Q31, Q34(a) and Q34(b) transistors were the same; the base current was maintained at 1μA throughout, and the collector segment at -1V. The substrate was set at -5V to ensure that it remained more negative than any other electrode. In the case of the Q34 series, a change in the external connections was used to change the periphery ratios for control and collector. (see Figure 1(c)) The control segment voltage with respect to the emitter, V_{CSE}, was varied by increments from -0.6V through zero to +0.2V and all currents and terminal voltages recorded. During this series of measurements, current null and reversal occurs, first for the control segment and then for the emitter; this is to be expected in view of equations (39) & (40), as the transistor goes into saturation. The results for the Q31 transistor are plotted in Figure 9, and the results for the Q34(a) and Q34(b) connections are shown superimposed in Figure 10. The variation in the controlled current gain as a function of control segment voltage was determined directly from the series of measurements, and the results for each transistor type plotted in Figure 11.

Figure 12 is a graph of the ratio of the control segment terminal current to that of the collector segment, as a function of control segment voltage V_{CSE}.

A summary of the various common-emitter current gain parameters that were measured directly at the device terminals, is provided in Table 2.

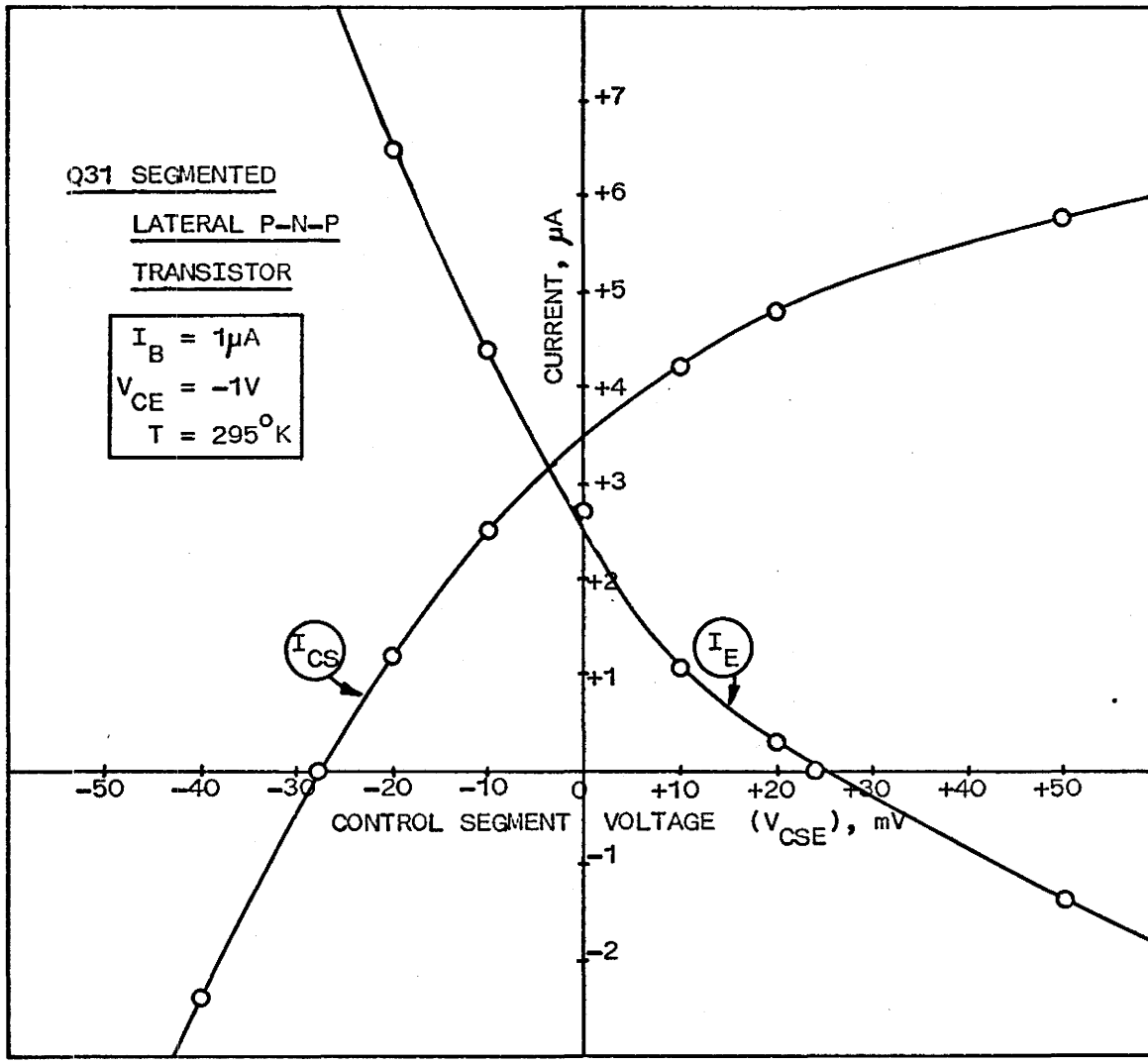

Figure 9. The saturation region of the Q31 transistor.

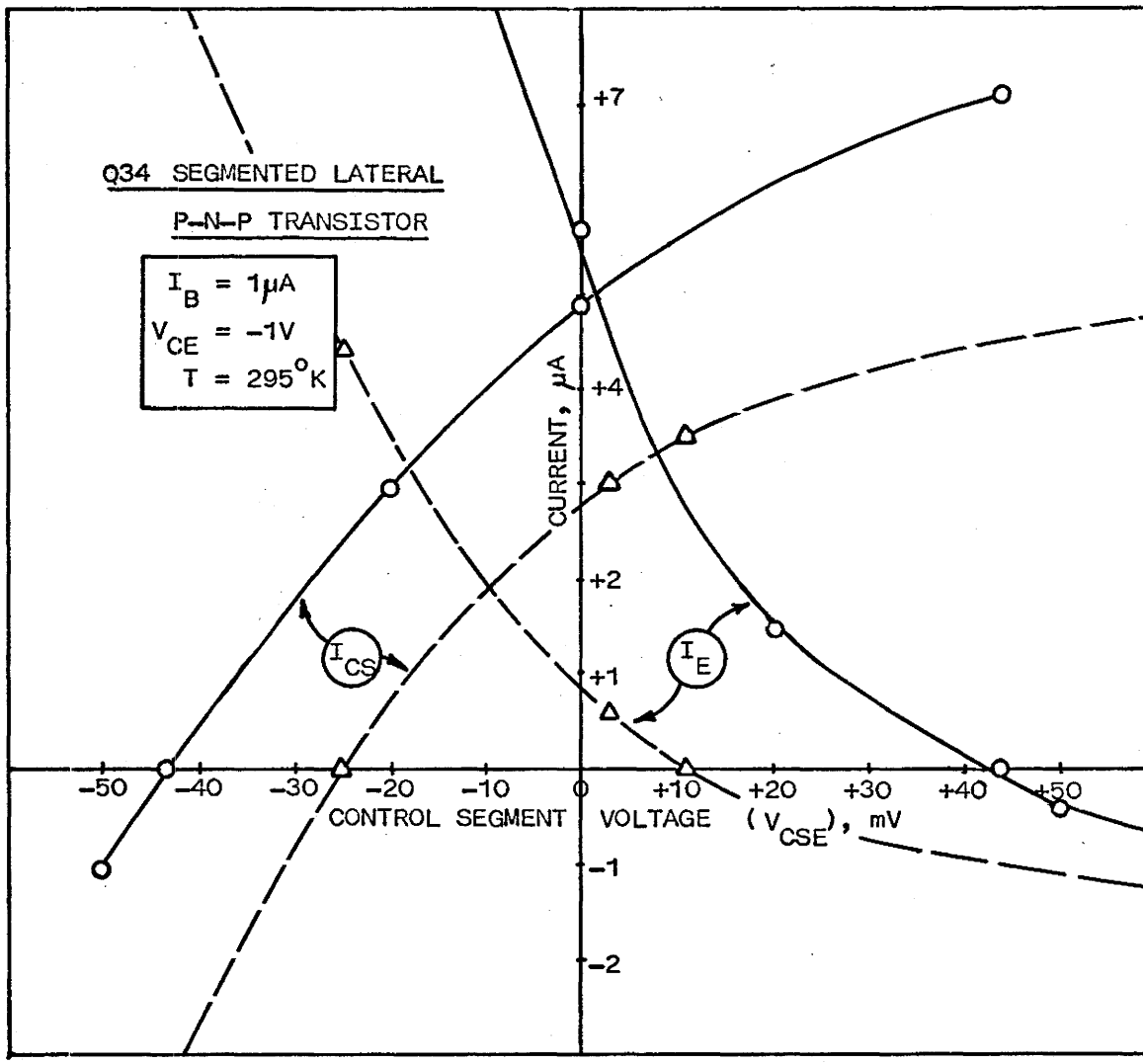

Figure 10. The saturation region of the Q34(a) and Q34(b) transistors.

Q34(a): —o—o—o—

Q34(b): --Δ---Δ---Δ--

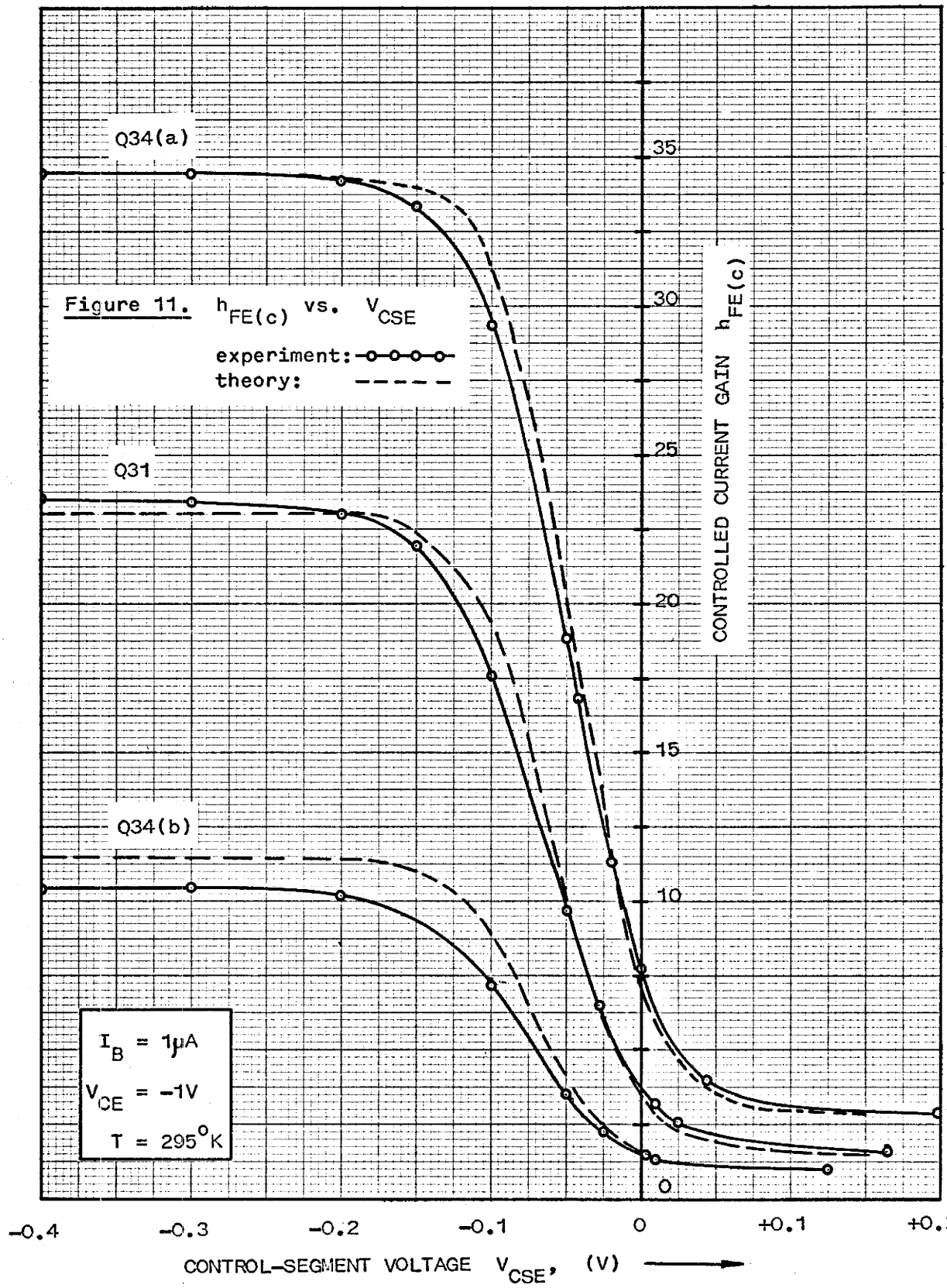

Figure 11. $h_{FE(c)}$ vs. V_{CSE}

experiment: —o—o—o—

theory: – – – –

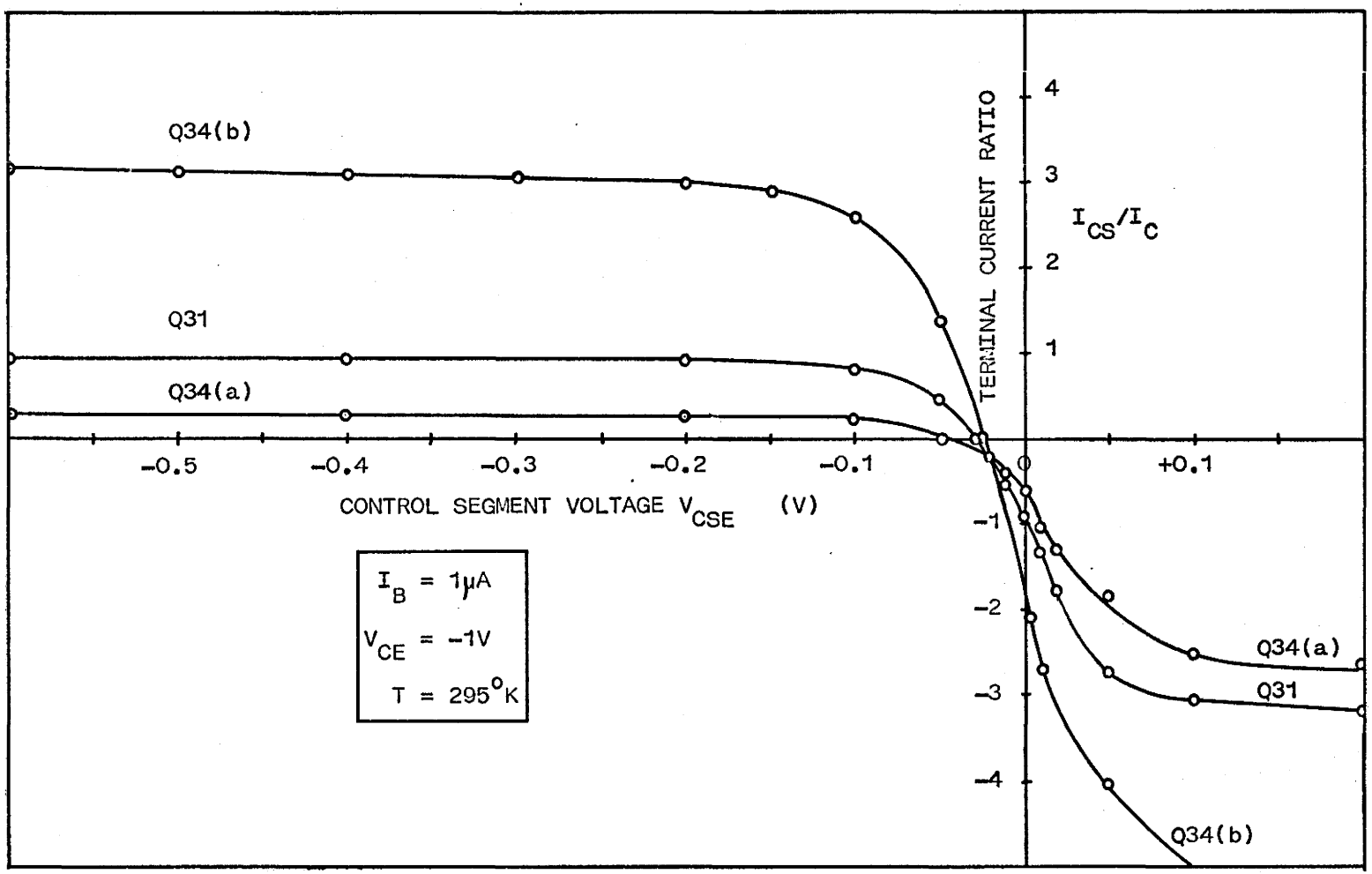

Figure 12. Ratio of control segment current to collector segment current as a function of control segment voltage V_{CSE}, for the Q31, Q34(a) and Q34(b) transistors.

Table 2.

(measured parameters)

TRANSISTOR	p'/p	β_F	$h_{FE(max.c.)}$	$h_{FE(o)}$	$h_{FE(min.c.)}$	β_R*	β_R
Q30		33					1.2
Q34(a)	1/4	45	34.4	7.8	2.8	4.6	0.9
Q31	1/2	48	23.5	3.8	1.6	3.7	1.1
Q34(b)	3/4	45	10.4	1.5	1.0	3.1	0.9

DISCUSSION

The variation in β_F for the segmented transistors selected at random ranged from 45 to 48 when measured at a constant base current of 1μA; the mean emitter-base voltage was found to be 646mV. A check on the validity of equations (2) through (6) can be made on an approximate basis by substituting appropriate values for the parameters in these expressions, and calculating what the total emitter current should be, say, in the forward active region.

With $q = 1.6 \times 10^{-19}$ C, $D_p = 13$ cm^2/sec, $p_{no} = 5 \times 10^3$ cm^{-3}, $V_E = 646$mV, $V_T = 25.4$mV ($T = 295^oK$), and the remaining parameters taken from Table 1, the value calculated was 46μA which compares very favourably with the range of measured values at the same bias level.

Equation (25) suggests that the degradation in β_F results from direct injection of a small current to the n^+ region from the emitter floor. The ratio of I_{EV}/I_{EL} calculated from (4),(5) & (6) using the parameters from Table 1, appears to be 0.02; the measured value for α_P is 0.5 for the parasitic transistor used alone, so that for a calculated value of $\beta_F = 46$, α_F would be close to 0.99 from equation (25). The same equation indicates an estimated value of around 60 as an upper practical limit for this group of devices.

The measured values for the ratio $h_{FE(max.c.)}/\beta_F$ for each of the transistor types tested compares favourably with the calculated value of $1 - p'/p$, as given by equation (26), and the results are given in Table 3. Similarly, the measured value for the ratio $\beta_R^*/h_{FE(min.c.)}$ compares well with the ratio $1 + I_{CS}/I_{CS}'$ calculated with the aid of equations (11) & (12), and the results are also given in Table 3.

An expression for β_R can be obtained from equations (18) & (21) with substitutions from (11), (12) & (13). After some manipulation it can be shown that the value of β_R is given by an expression of the form:

Table 3.

TRANSISTOR	MEASURED VALUES	CALCULATED VALUES
	$h_{FE(max.c.)}/\beta_F$	$(1 - p'/p)$
Q34(a)	0.76	0.75
Q31	0.49	0.5
Q34(b)	0.23	0.25
	$\beta_R^*/\ h_{FE(min.c.)}$	$(1 + I_{CS}/I_{CS}')$
Q34(a)	1.64	1.63
Q31	2.3	2.33
Q34(b)	3.1	3.04
	Coefficient "B"	$\alpha_R pA/\ \alpha_F(p - p')$
Q34(a)	0.44	0.48
Q31	0.6	0.73
Q34(b)	1.7	1.46
	Control Terminal Current/Collector Terminal Current	
	Forward I_{CS}/I_C	
Q34(a)	0.31	0.33
Q31	1.0	1.0
Q34(b)	3.2	3.0
	Reverse I_{CS}/I_C	
Q34(a)	-2.7	-2.4
Q31	-3.9	-3.8
Q34(b)	-5.4	-5.2

$$\beta_R = \alpha_R/1.75(1 - \alpha_R) + 0.23(1 - \alpha_P)$$

the numerical values arising from the geometrical parameters. Since the measured values of β_R are all close to unity as indicated in Table 2, and if $\alpha_P = 0.5$, this implies that α_R should be close to 0.7 for each type of transistor. Similar calculations using measured values of β_R* in (28) suggest a mean value of α_R close to 0.8. Although these are only estimated values, they seem to be reasonable on the basis of what is known about the symmetry of emitter and collector doping and the geometry involved. Assuming a similar dependence of both α_F and α_R on current level, the ratio α_R/α_F would be independent of current level; a reasonable estimate for this ratio would be 0.75.

An alternative method for evaluating the ratio α_R/α_F is based upon (39) & (40) in Case (iv) & (v) described in the FORMULATION. However, since the measurement of voltage was limited to an accuracy of $\pm$2mV and in particular, the temperature variation might well have been $\pm 2^{o}$C, it is reasonable to expect only order of magnitude confirmation for the value of the ratio α_R/α_F. With the appropriate values taken for $V_{CSE(o)}$ from the graphs of Figures 9 & 10 respectively, for the Q31, Q34(a) & Q34(b) transistors, values for the ratio α_R/α_F were calculated using (39) & (40). The results indicate values of 0.64 for the Q31, 0.86 for the Q34(a) and 0.68 for the Q34(b) so that a mean value of 0.72 would be in reasonable agreement with that already estimated.

In the derivation of the expression for common-emitter controlled current gain given by (38), it was shown that the coefficient "B" could be related to parameters which could be measured directly at the device terminals. This enables a cross check to be made between the value of the coefficient calculated from (36), and the measured value resulting from the substitution of the appropriate values from Table 2 into (37), for each of the transistors in turn. A comparison of these results is given in Table 3, where the value of p'/p is from Table 2 and the value of the coefficient "A" has been calculated from (33), as 0.52. In view of the rather gross assumptions made in the derivation leading to an expression like equation (33), and the uncertainties in determining a reasonable value for α_R/α_F, there is fair agreement between the values obtained for

the coefficient "B", both by measurement and calculation from the theory.

The controlled current gain $h_{FE(c)}$ is determined for arbitrary values of control segment voltage V_{CSE} for each of the transistors Q31, Q34(a) & Q34(b), by substitution of the appropriate parameters into (38). Using the calculated mean value of $\beta_F = 46$, $h_{FE(max.c.)}$ is calculated from (26), and using the measured values of β_R^* from Table 2, $h_{FE(min.c.)}$ is calculated from (29). The values for coefficient "B" were used in (35) for the calculation of $h_{FE(o)}$. The results are plotted on the graph of Figure 11 for values of V_{CSE} ranging from -0.4V to +0.2V; the close agreement between the theory based upon the validity of equation (38) and the experimental measurements made on three randomly selected types of segmented transistor is apparent.

For operation in the forward active region, the current division that occurs between collector and control segments for equal reverse bias is shown to be dependent on their periphery ratio in accordance with equation (41); that this is a valid assumption can be shown from a comparison of measured values taken from Figure 12, and the ratio as calculated from (41). These results appear in Table 3, together with those obtained under the conditions for which (42) is valid, and in either case there is close agreement.

From the discussion in the FORMULATION concerning the stabilised beta transistor, it is clear that for the devices tested, a periphery ratio equal to or greater than that for the Q34 type is needed for $\beta_{F(S)}$ values between say, 2.3 and 5.5. Equation (44) can be used to determine the required periphery ratio for values of stabilised common-emitter current gain within the range cited, provided always that such a large ratio of p'/p can be fabricated successfully since the electrode acting as the regular collector must have by far the larger fraction of available area.

CONCLUSION

A development of the basic Ebers-Moll type of Model has been found adequate for a first-order type of analysis of the lateral p-n-p transistor, and the model equations have been used to interpret the behaviour of a family of segmented lateral structures with an accuracy sufficient for most Engineering purposes.

The common-emitter current gain to a collecting segment is controllable by the voltage on an adjacent segment, and is shown to be a sensitive function of this voltage and the ratio of the areas of the segments. A number of applications have been suggested for taking advantage of this feature of a.g.c. in the segmented lateral structures.

Most of the applications of the p-n-p segmented lateral transistor in integrated circuits centre around the current-division property of the segments, and its control by variation of the collecting geometry of the device. A number of multi-collector devices can be designed to take advantage of the cross-talk because the current division is also affected by the relative bias voltages to the segments.

A particularly noteworthy feature of the segmented lateral transistor is the facility for using one of the segments connected to the base to provide internal feedback, thereby stabilising the common-emitter current gain against variations in processing conditions which invariably lead to a wide spread in the value of this parameter.

A better understanding of the behaviour of the lateral transistor would undoubtedly lead to greater use of the device, and it is felt that the inherent limitations of the Ebers-Moll type of model do not represent a serious handicap in cases such as those described in this paper. Knowledge of the terminal behaviour of integrated circuit devices is fundamental in Engineering applications, and the Ebers-Moll model is probably best suited for that case.

APPENDIX

Derivation of Expressions used for Emitter Areas A_E, A_E' and A_E''.

Consider the diagram shown in Figure A1:

The incremental area dA can be written

$$dA = 2\pi r x_j \, d\theta$$
$$= 2\pi x_j (r_E + x_j \cos\theta) \, d\theta$$

Therefore,

$$\underline{A_E} = 2\pi x_j r_E \int_0^{\pi/4} d\theta + 2\pi x_j^2 \int_0^{\pi/4} \cos\theta \, d\theta$$
$$= \underline{\pi x_j (\pi r_E/2 + \sqrt{2}\, x_j)}$$

Similarly,

$$\underline{A_E'} = 2\pi x_j r_E \int_{\pi/4}^{\pi/2} d\theta + 2\pi x_j^2 \int_{\pi/4}^{\pi/2} \cos\theta \, d\theta + \pi\left[r_E^2 - \left(r_E - [L_p - w_o]/2 \right)^2 \right]$$
$$= \underline{\pi x_j (\pi r_E/2 + [2 - \sqrt{2}]\, x_j) + \pi \left[2r_E - [L_p - w_o]/2 \right] [(L_p - w_o)/2]}$$

The area A_E'' can be written directly as

$$\underline{A_E'' = \pi \left[r_E - (L_p - w_o)/2 \right]^2}$$

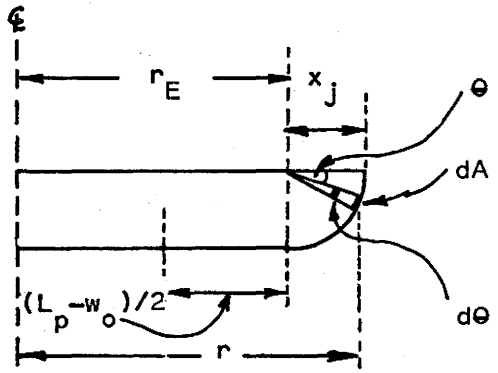

Figure A1. Notation for the derivation of expressions for A_E, A_E' and A_E''.

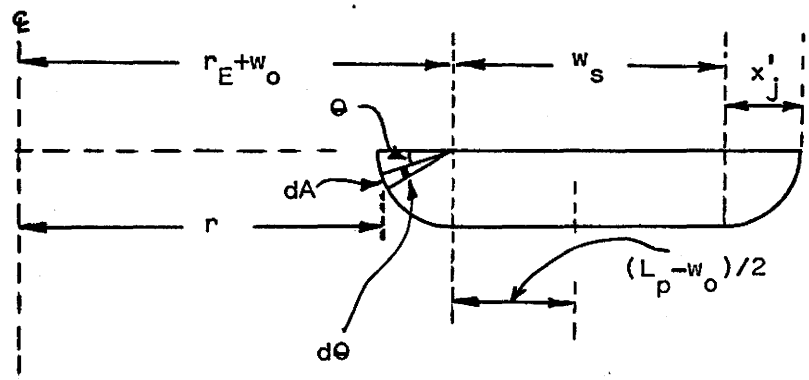

Figure A2. Notation for the derivation of expressions for A_C, A_C' and A_C''.

Derivation of Expressions used for Collector Areas A_C, A_C', and A_C''.

Consider the diagram shown in Figure A2:

The incremental area dA can be written

$$dA = 2\pi r x_j \, d\theta$$
$$= 2\pi x_j (r_E + w_o - x_j \cos\theta) \, d\theta$$

Therefore,

$$\underline{A_C} = 2\pi x_j (r_E + w_o) \int_0^{\pi/4} d\theta - 2\pi x_j^2 \int_0^{\pi/4} \cos\theta \, d\theta$$
$$= \underline{\pi x_j (\pi [r_E + w_o]/2 - \sqrt{2}\, x_j)}$$

Similarly,

$$\underline{A_C'} = 2\pi x_j (r_E + w_o) \int_{\pi/4}^{\pi/2} d\theta - 2\pi x_j^2 \int_{\pi/4}^{\pi/2} \cos\theta \, d\theta + \pi \left[\left[r_E + [L_p + w_o]/2 \right]^2 - (r_E + w_o)^2 \right]$$
$$= \underline{\pi x_j (\pi [r_E + w_o]/2 - [2 - \sqrt{2}] x_j) + \pi \left[2r_E + [L_p + 3w_o]/2 \right] \left[(L_p - w_o)/2 \right]}$$

The area of the outer curved side-wall of the collector, which is part of the area A_C'', can be found from an expression similar to that for A_E by replacing r_E with the sum $r_E + w_o + w_s$ and integrating from zero to $\pi/2$ instead of zero to $\pi/4$. The total area A_C'' becomes:

$$\underline{A_C''} = \underline{\pi x_j (\pi [r_E + w_o + w_s] + 2x_j) + \pi \left[2r_E + w_s + [L_p + 3w_o]/2 \right] \left[(w_s - [L_p - w_o]/2 \right]}$$

Derivation of the Expression used for Area A_G.

To a first approximation, the area of a gap face is considered to be a quarter cylinder of length $w_s + x_j$ and radius x_j. Since the area A_G is considered to be made up of two regions (both end faces of a segment) each of which extends halfway down the cylindrical face,

$$A_G = \frac{2\pi x_j (w_s + x_j)}{4}$$

$$= \pi x_j / 2 (w_s + x_j)$$

Derivation of an approximate expression for "effective" base width, w_1.

To a first approximation, each of the elementary areas marked dA in Figure A3. can be considered equal to ¼ A_E. As a result,

$$\frac{A_E}{w_1} = \left[\frac{1}{a} + \frac{1}{b} + \frac{1}{c} + \frac{1}{d} \right] \frac{A_E}{4}$$

from which w_1 is easily calculated. The numerical values for a, b, c, and d are calculated using the assumed values of $x_j = 3.9\mu$ and $x_j' = 4.2\mu$ (where depletion region widths of 0.3μ for the emitter-base junction and 0.6μ for the collector-base junction have been assumed, and included in the values) and $w_o = 8.8\mu$.

With these values,

$a = 0.7\mu$

$b = 0.86\mu$

$c = 1.31\mu$

$d = 2.07\mu$

and therefore:

$w_1 = 1\mu$ (approx.)

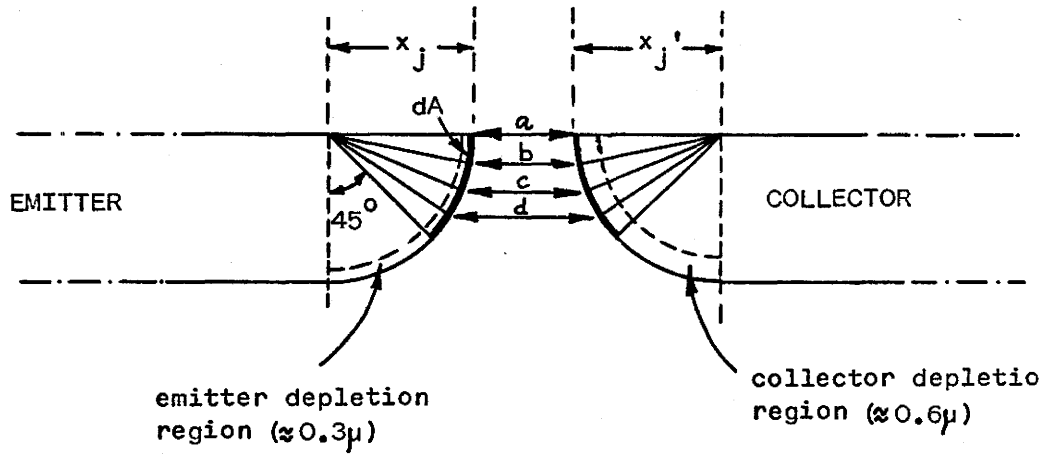

Figure A3. Subdivision of the gap into elementary areas dA, each with their respective "effective base widths", a, b, c, d, etc.

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