# CHARACTERIZATION AND INTEGRATION OF DEFECT-MEDIATED PHOTODETECTORS FOR SILICON PHOTONIC CIRCUITS

# CHARACTERIZATION AND INTEGRATION OF DEFECT-MEDIATED PHOTODETECTORS FOR SILICON PHOTONIC CIRCUITS

by

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# Abstract

Silicon photonic interconnects represent a possible solution to the problems associated with scaling electrical interconnects to higher data rates. Defect-mediated optical detectors fabricated via inert ion implantation incorporated with optical waveguides in such a circuit allow control and monitoring of the optical signal and can be fabricated entirely using standard Complementery Metal-Oxide Semiconductor (CMOS) fabrication steps, thus simplifying the task of integrating optical functionality alongside electronic circuits on a chip.

In the work described in this thesis, the defects involved in the detection process at wavelengths at and around 1550 nm have been investigated. For low-dose ion implantation, the defect which dominates optical absorption and detection is shown to be an acceptor with an energy of 0.41 ± 0.02 eV below the conduction band, properties consistent with the silicon divacancy. A novel technique for optical characterization has been developed and used to determine the optical cross-section of this defect to be 6 x $10^{-17}$ $cm^2$ for a wavelength of 1550 nm. Defect concentration versus thermal annealing temperature was evaluated, and waveguide integrated detectors were fabricated and used to characterize optical absorption and quantum efficiency as a function of the annealing conditions.

A monolithically integrated device comprising a defect-enhanced photodiode and a variable optical attenuator was designed, modeled, fabricated, and demonstrated with the photodiode used to monitor and control the optical output power. To illustrate the potential of such a device, it was operated as a dynamic channel leveller with external software used to mimic an electronic feedback loop between the detector and attenuator. The channel leveller was able to maintain ± 1 dB output power variation across a 7-10 dB input dynamic range for wavelengths ranging from 1530 nm to 1570 nm.

Additionally, a tunable resonant defect-enhanced photodiode was designed, modeled, fabricated, and characterized. It is shown that resonant effects can be used to obtain similar responsivity from a small, lightly absorbent photodiode as would otherwise require a longer, highly absorbent photodiode, thus enabling very low minimum detectable power. The device responsivity was measured to be greater than 0.1 A/W for wavelengths ranging from 1510 nm to 1600 nm, with individual wavelengths selectable by tuning the resonance peak. The device was also demonstrated as a variable optical attenuator with 20 dB extinction, less than 44 mW switching power, and integrated monitoring.

The devices described in this thesis represent the first reported demonstrations of integrated optical power control, dynamic channel levelling, and tunable resonant detection using defect mediation in a silicon photonic circuit.

# Acknowledgments

I would like first to thank my parents, my brothers and sisters (especially Sarah), friends and family for their prayers and encouragement.

My interest in optics and photonics specifically (as opposed to science generally) began at Thomas Aquinas College while reading and discussing works by Huygens, Hertz, Newton, Maxwell, and Einstein and contrasting them to the reasoning in Aristotle's Physics. It was the ensuing discussions with fellow students and with tutors Michael Collins and Ronald Richard that led me to consider optical physics as a pursuit within which much understanding of the natural world could be gleaned. I have never lost the keen interest in electromagnetics which was awakened during those happy years.

It was at the University of Waterloo that I received my first exposure to experimental optical physics while pursuing undergraduate thesis work with ultrafast lasers under the guidance of Donna Strickland – most of what I understand concerning the fundamentals of optics, I learned from Donna.

I have had the privilege to work closely with many top-notch scientists and engineers in industry at JDS Uniphase, Phiar, Dofasco and Intel. I have learned a great deal from these professionals in terms of technical understanding, but also (and more importantly) seen by their example the qualities which characterize a successful engineer and scientist tackling real-world problems.

I owe a great debt of gratitude to the Department of Engineering Physics at McMaster and to those who created and maintain the CEDT. In particular I wish to thank David Thompson both for his role in founding the CEDT and for the time he has taken to answer my questions concerning defects, Adrian Kitai for his willingness both to answer technical questions and loan textbooks over the years, Doris Stepanovic and Zhilin Peng for their endless patience and tireless help in the cleanroom, Graham Pearson, Brad Robinson, Jacek Wojcik, Evgenyi Chelomentsev, Peter Jonasson, Jim Garrett, and Doug Bruce. I also wish to thank the staff of the Brockhouse Institute for Materials Research, especially Andy Duft, Fred Pearson, Steve Koprich, and Chris Butcher, and Dan Deptuck at CMC Microsystems for his assistance with mask development during the LETI work.

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experts Vlademir Markevich and Tony Peaker at the University of Manchester. I cannot thank these gentlemen enough for their time, effort, and willingness to impart hard-won lessons to a newcomer.

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*Non nobis Domine, non nobis, sed Nomini Tuo da gloriam.*

Ps. 113:9

This thesis is dedicated to the memory of Marcus Berquist (1934-2010).

*Requiescat in pace.*

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# Chapter 1

# Introduction

In the effort to improve computing performance, optical interconnects and hence photonic circuits have emerged as a possible solution to the problems associated with scaling electrical interconnects. Although photonic circuits can be monitored via external optical detectors, the advantages of integrating detectors within the circuit itself make such integration inevitable. This chapter presents the argument for silicon-based photonic circuits and summarizes the state of the art of various methods of photodiode integration. A review of the published literature with respect to integrated defect-engineered photodetectors will also be presented.

## 1.1 Optical versus electrical interconnects

The business model for the semiconductor industry originated from the prediction by Gordon Moore (then head of Research and Development at Fairchild Semiconductor and later co-founder of Intel Corp.) in 1965 in the form of "Moore's Law", which stated that transistor density on a chip would double every

one to two years [1, 2]. As illustrated with respect to Intel's technology development in Fig. 1.1 this model was founded on an excellent prediction and continues to be the guideline to which the industry strives to adhere in order to meet demand and take advantage of the economies of scale achievable by manufacturing more devices per chip. [3]

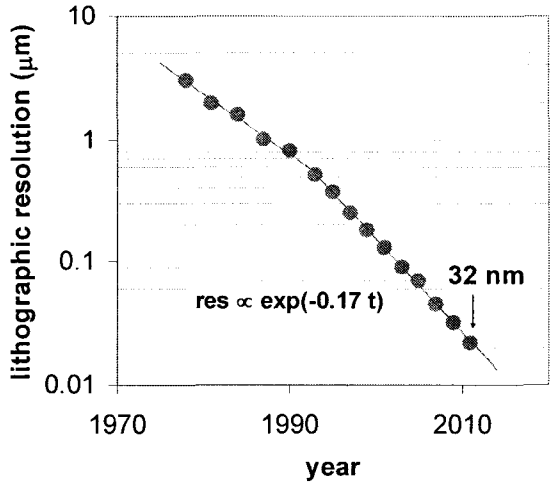


Fig. 1.1: Scale of transistor dimensions adopted by Intel versus time from the mid-1970's to the present day, adapted from [4].

Together with increases in clock frequency (i.e. the speed at which data is synchronized within a processor) increases in device density led to an overall doubling of processor performance every 18-24 months from 1980 to 2002.

### 1.1.1 Device density

With increased transistor density comes increased power density (i.e. power consumed per unit area on-chip), leading not only to power consumption challenges but also to thermal issues: with the same chip area available for cooling, more thermal power had to be dissipated to a heat sink if the operating temperature of the processor was to be held within reasonable limits.

### 1.1.2 Bandwidth in competition with signal power

With thermal budgets already a significant consideration problems arose due to increases in clock frequency.

***RC time constant***

Clock signal distribution and data transmission across a processor are accomplished using "interconnects" – traditionally metal wires – which criss-cross the chip area. The maximum frequency (i.e. bandwidth) manageable by an interconnect is dictated by its *RC* time constant. Since resistance *R* varies directly with length and inversely with width while capacitance also varies directly with length, it is apparent that the *RC* time constant and hence the frequency cutoff degrades *quadratically* with interconnect length [5]. Reductions in interconnect width with increased device density only exacerbated this problem by increasing resistance. For interconnects between neighbouring regions of a processor, length decreased proportionately with device density but for "global" interconnects extending across the length of the chip the problem persisted. The use of repeaters joining shorter interconnect lengths mitigated this problem [6], but only at the cost of on-chip area, increased power density, and added delay.

***Dynamic power density***

The power dissipated during signal transmission across an interconnect is inversely proportional to its impedance, and hence (for a capacitive load) directly proportional to increases in signal frequency. Increasing the clock frequency therefore led to greater power densities within interconnects. Since interconnects were shielded by dielectrics with generally poor thermal conductivity (as compared to transistors in contact with the silicon substrate), power dissipation within the interconnect produced elevated temperatures in the metal wires, which in turn led to reliability issues due to electromigration and open-circuit failures.

***Crosstalk***

With chip clock speeds in the gigahertz regime, signal wavelengths reached the centimetre scale of the metal interconnects intended to convey them, with the result that the interconnects could act as antennae and both radiate signal power and receive signals from nearby vias. This led to interference or "crosstalk" between interconnects such that ever higher signal power was needed to combat the increase in both transmission loss and noise. Coupling between adjacent vias also increased the signal propagation delay, and worse, it increased delay in a manner that depended on the chip design.

### 1.1.3 Advantages of optical interconnects

One possible solution to the problems associated with high-bandwidth electrical interconnects is the use of optical interconnects. In this approach the data is encoded onto an optical wave either by means of a directly modulated laser or an external modulator. Several optical waves can be encoded and transmitted simultaneously (i.e. "multiplexed") since individual optical wavelengths do not interfere with one another in linear systems. The Nyquist frequency rather than an *RC* time constant becomes the bandwidth limiting factor, but with the optical frequency at several hundred terahertz the Nyquist limit of such signals is so high as to be no concern. Both silicon and silicon dioxide are transparent for such optical frequencies, so power dissipation within the interconnect ceases to be a problem, and with wavelengths on the order of 1 μm (i.e. much smaller than the distance between interconnects) there is virtually no unintended crosstalk.

These considerations all lead to the conclusion that the data transmission volume of an optical interconnect is virtually unlimited relative to the data rates in use for the foreseeable future.

### 1.1.4 Chip-chip considerations

Many of the scaling issues associated with intra-chip interconnects are less relevant to interconnects between discrete components within a computer or between individual computers. However, the amount of data to be transferred is generally higher since multiple data streams are bundled together. Furthermore, the distances involved are larger, while the fabrication constraints are relaxed since such interconnects can be implemented in cable form rather than vias fabricated on a planar surface. Due to the large distances and bandwidths, optical transmission via fibre-optic cable is desirable to avoid the loss, crosstalk, and frequency limitations discussed above. However this requires a means to encode data onto an optical beam for transmission, and thus there must either be electrical transmission between the source/receiver chips and electro-optical conversion modules or the optical conversion must be performed on the chip itself for optical transmission off-chip to the fibre. The first approach requires long, high-bandwidth electrical interconnects and is therefore subject to the challenges listed above. The second approach requires photonic functions and interconnects integrated on-chip, even if they are not used for intra-chip data transmission.

### 1.1.5 Challenges associated with optical interconnects

Optical transmission requires the incorporation of optical sources (e.g. either light-emitting diodes (LEDs) or lasers), optical modulators, and optical receivers. Traditionally these functions have been performed in materials foreign to the electronics industry (e.g. III-V compounds) and considerably more expensive than silicon. The relative practicality of electrical versus optical transmission is therefore determined by the data rates required on a particular link, the link length, and the price-point of integrating optical with electronic functionality. Long distance links which bundle many tributary signals together require the

largest data capacity and are therefore the most amenable to optical transmission – hence the first widespread implementation of optical networks was in the form of fibre optic links for inter-city data transmission. With the growth of the internet and ever-increasing data transmission demand, this transition from electrical to optical links became necessary for ever shorter distances such that optical transmission between server racks is now commonplace. The next step – device-to-device optical transmission for standard home use - has recently been developed and is in production. [7,8]

## 1.2 Silicon photonics

Every transition from an established technology to a new one involves cost, however the cost can be minimized by making the transition in a manner as compatible with prior technology as possible. For both chip-to-chip and intra-chip optical interconnects this means adding optical functionality without abandoning the silicon platform which has been the object of decades of fabrication infrastructure and research. Optical interconnects between electrical components must either be fabricated within silicon, or must be fabricated separately and packaged as discrete components. Obviously the former is preferable if the required optical functions can indeed be achieved in silicon.

In parallel to the strong attachment to silicon in the microelectronics industry, the progression from long-distance to shorter distance optical links described above has carved avenues of favourable advancement in the optical realm as well. In particular, the absorption and dispersion properties of glass optical fibre together with the development of the erbium doped fibre amplifier led to the adoption of the wavelengths near 1550 nm for optical transmission (hence their name: the "*C*" or "Conventional" band).

An ideal approach to optical interconnects, therefore, involves the integration of optical functions in silicon at wavelengths around 1550 nm. This is the basis for silicon photonics.

### 1.2.1 Silicon-on-insulator

As will be described in more detail in Chapter 2, a guided optical signal in a planar chip requires a lower cladding layer to confine the beam near the surface. A planar layer of silicon dioxide (i.e. glass) situated below the silicon surface is well suited to this purpose, and fortunately such a material – silicon-on-insulator (SOI) - is already in widespread use in the electronics industry. A diagram of the layers in an SOI wafer is shown in Fig. 1.2.

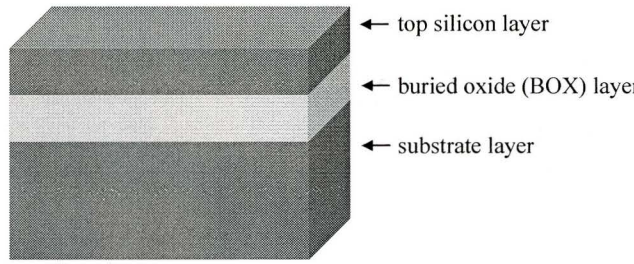


Fig. 1.2: Silicon-on-insulator (SOI) structure showing top silicon layer, buried oxide (BOX) layer, and substrate layer

There are currently three common techniques for fabrication of SOI:

a) SIMOX (separation by implanted oxygen): oxygen is implanted below the surface of the silicon and annealed to form silicon dioxide,

b) BESOI (bond and etch-back SOI): a silicon wafer with a silicon dioxide film is bonded to another silicon wafer and then etched until only a thin layer of silicon remains above the oxide, and

c) SmartCut®: a silicon wafer with a silicon dioxide film is first implanted with a hydrogen-helium mixture, then bonded to a silicon wafer, and finally annealed to cleave the wafer at the end of the implanted ions range,

leaving behind a thin layer of silicon atop the oxide film. The intellectual rights to this process are held by SOITEC Inc. of France.

These fabrication processes are reviewed in detail in [9] and illustrated in Fig. 1.3.

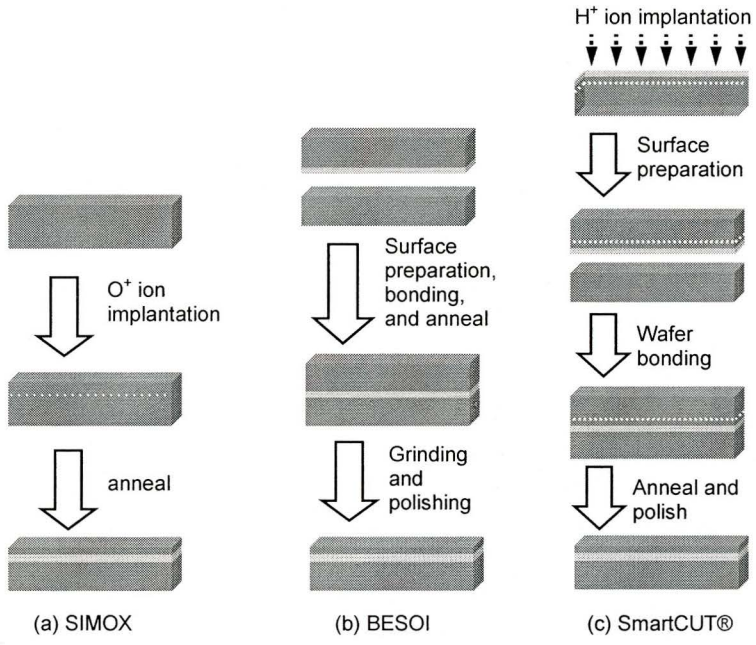


Fig. 1.3: Fabrication processes for SOI. (a) SIMOX process, (b) BESOI process, (c) SmartCut$^{(R)}$ process.

The high contrast between the refractive index of silicon dioxide (approximately 1.5) and silicon (approximately 3.5) for wavelengths in the *C*-band allows excellent optical mode confinement in the vertical direction as described further in Chapter 2. By etching the silicon layer to form either a rib or a wire waveguide, excellent lateral confinement can also be achieved such that optical waveguides with small bend radii, and thus compact photonic circuit architectures, are feasible. Furthermore, for cases in which either the application or the fabrication constraints necessitate large waveguide dimensions, single-mode operation is still possible despite high index contrast by appropriate design of the waveguide [10].

### 1.2.2 Optical functions demonstrated in silicon

The functions required for optical interconnects in silicon are light generation, detection, modulation, transmission and signal routing, and off-chip coupling. The state of the art of silicon photonics with respect to each function will now be summarized.

### 1.2.3 Optical transmission

For planar devices, optical transmission is best integrated by means of planar waveguides which can be fabricated in parallel with other devices on the chip. As discussed above, SOI technology allows a thin slab of silicon to act as a guiding layer with the buried oxide acting to prevent light from escaping into the substrate. Lateral confinement can be achieved by etching regions in the silicon layer to leave either a "rib" waveguide structure or a "wire" waveguide structure as illustrated in Fig. 1.4.

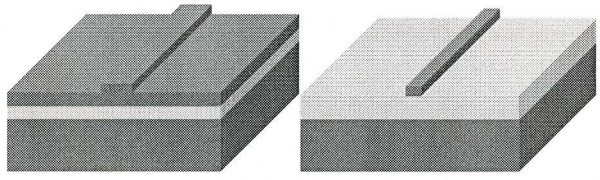

Fig. 1.4: Rib waveguide structure (left) and wire waveguide structure (right) in SOI for transmission and confinement of optical signals.

Optical waveguides in silicon were first conceived and demonstrated by Richard Soref and Joseph Lorenzo using doping density variations in 1986 [11]. SOI with its ready-made cladding layer was used to fabricate optical rib waveguides and demonstrate device operation for undoped silicon in 1990 with losses of 5 dB/cm [12]. Improvements in SOI quality and waveguide fabrication have led to single-mode rib waveguide propagation losses of typically less than 0.5 dB/cm [13] and wire waveguide losses of less than 2.5 dB/cm [14], with 0.92 dB/cm also

demonstrated [15]. Signal routing and filtering can be accomplished using structures such as arrayed waveguide gratings (AWG).

### 1.2.4 Off-chip coupling

The mode mismatch (see Chapter 2) between optical fibre and most silicon waveguides is such that directly coupling from one to the other involves significant power loss. A range of solutions to this problem have been pursued and will be summarized here.

*3D taper*

A three-dimensional taper at the end of the waveguide allows the fibre to be butt-coupled to a large cross-section end facet with good mode match, and then a suitably gradual taper in both the vertical and lateral dimensions causes the mode to evolve as it propagates until both the taper and mode dimensions match the rib waveguide. A schematic is shown in Fig. 1.5.

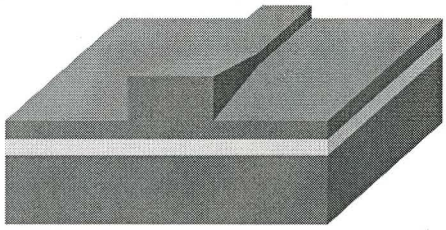

Fig. 1.5: 3D taper input/output facet coupler for fiber to rib waveguide mode conversion in SOI adapted from [16].

This approach was demonstrated by Fritze *et al.* in 2002 [16]. The process involved a non-standard gray-scale lithography step to achieve a non-planar structure, and therefore surface roughness caused high scattering losses.

*Non-vertical taper (NVT)*

By separating the taper into a lower region with height equal to that of the final rib waveguide and an upper region such that the combined height is roughly equal

to the diameter of the optical fiber, the non-planar geometry of the 3D taper can be avoided. The fibre can be coupled to a large square end-facet, after which the upper region width is reduced in lateral width until the mode is confined entirely in the lower region. With the mode confined in the wide lower region, a lateral taper matches the layer to the final rib waveguide width. Excellent coupling with losses of less than 0.5 dB were measured [17] for a 1 mm taper using this approach, however fabrication requires selective epitaxial growth to produce the large upper region (at least several μm thick) or a starting SOI thickness of several microns followed by a two-stage etch to produce the rib waveguide. The former is not a standard CMOS-compatible process, while the latter is subject to yield issues due to the two etch steps required to produce the rib waveguide without the benefit of an etch-stop. The NVT offers excellent low-loss coupling, however, and is largely polarization insensitive. The structure of the NVT is illustrated in Fig. 1.6.

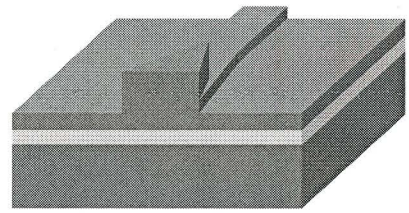

Fig. 1.6: Non-vertical taper (NVT) for fiber to rib waveguide mode conversion in SOI without non-planar fabrication steps, adapted from [17].

A modification to this approach has been suggested by Doylend and Knights [18] in which multiple-layer SOI is used as a starting material (achieved by multiple wafer bonding) such that the upper region can be etched to the first buried oxide layer, which defines the height of the rib layer by acting as an etch-stop. In this configuration the device is no longer an adiabatic taper in which the mode evolves from the fibre mode to the rib mode, but rather an asymmetric vertical directional coupler (see Chapter 2) in which the upper layer is laterally tapered so as to have an overall effective index match to the lower layer, after which the two regions are extended for one coupling length so as to transfer power from the upper layer

to the lower layer. With power transfer complete, the upper layer terminates and optical power is confined in the rib layer which can then be laterally tapered to the width of the final rib waveguide. This structure is illustrated in Fig. 1.7.

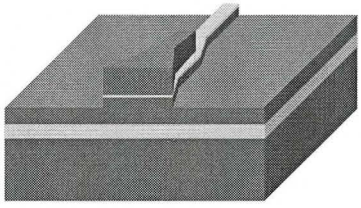

Fig. 1.7: Asymmetric vertical directional coupler approach, in which the top of the rib is masked by an oxide etch-stop for ease of processing. The topmost silicon and the wide rib are effective index-matched such that near-100% power transfer to the rib layer occurs before the top silicon terminates. Adapted from [18].

This technique offers the possibility of near-100% coupling efficiency with high yield, broadband operation, and polarization insensitivity for standard industry manufacturing tolerances according to simulated results [18], but suffers from the requirement for an exotic starting wafer.

A further modification has been demonstrated by Intel Corp. [19] in which two upper taper stages are used rather than one. This allows mode-matching with less than 0.7 dB loss for 1.5 μm wide rib waveguides as well as low polarization sensitivity. Disadvantages of this approach are its length (approximately 1 mm) and a fabrication process that includes both epitaxial growth and chemical-mechanical polishing/planarization between etch steps.

*Inverse taper coupler*

Since it is mode size rather than facet size which dictates the coupling efficiency between optical fiber and the planar waveguide, an inverse taper approach in which the input facet is extremely narrow and then widens laterally to match the rib waveguide can be employed. This approach was demonstrated by Almeida et al. [20] using an input facet width of 100 nm and a final rib waveguide width of 470 nm and achieving losses between 3 dB and 6 dB (depending on polarization)

for taper lengths less than 50 μm. This approach (illustrated in Fig. 1.8) offers the key advantage of compact size relative to the tapers discussed above.

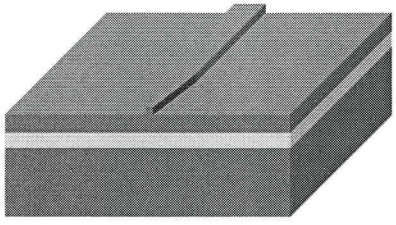

Fig. 1.8: Inverse taper coupler in SOI, adapted from [20].

*Prism coupler*

Bonding a prism to the waveguide allows a fibre to be coupled directly to one facet of the prism, and then have the prism redirect the beam into a tapered rib waveguide at an angle appropriate for efficient coupling. This approach was demonstrated by Lu and Prather [21] with efficiency of 46% (approximately 3 dB coupling loss) for TE polarization and large spectral bandwidth of 80 nm. Although this approach is neither monolithic nor altogether compatible with standard CMOS processes, it holds the advantage of allowing fibre to be coupled to a rib waveguide anywhere on the chip, or indeed anywhere on the wafer. This raises the intriguing possibility of being able to test optical devices at the wafer scale before the final dicing and polishing steps needed to produce input and output facets.

*Grating coupler*

A grating structure etched into the rib layer can be used to redirect optical input at near-normal incidence to an angle suitable for coupling to the rib layer, which can then be tapered laterally to the final rib width. This approach has been demonstrated by Taillaert, Van Laere et al. [22, 23] for an SOI rib layer as thin as 220 nm. Coupling losses for a grating with were reported between 6 dB and 9 dB across the *C*-band for a grating coupler etched to a depth of 50 nm, and 1.6 dB for an enhanced design with a gold reflector on the backside of the sample. The

grating can be very compact (10 μm – 20 μm) and the lateral taper can be 200 μm long for a total coupler length of less than 0.25 mm. As with the prism coupler approach, this technique also holds the advantage of allowing inputs/outputs to be positioned anywhere on the chip such that device architecture is not limited to the standard side-to-side chip traversal required by facet coupling. The design is highly polarization dependent, however, such that for a given fibre input angle only one polarization will be coupled to the waveguide.

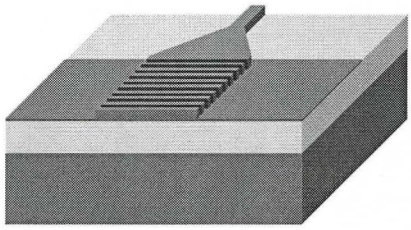

Fig. 1.9: Grating coupler to an SOI wire waveguide, adapted from [22].

Engineering of the grating geometry at sub-wavelength scales can be used to modify the refractive index of the waveguide core [24] while suppressing higher orders of diffraction; this approach has been demonstrated as a means to achieve fibre-chip coupling with 0.9 dB loss [25].

### 1.2.5 Light generation and amplification

Although it is certainly possible to integrate a 1550 nm wavelength optical source with SOI waveguides using fibre-coupling techniques, it may be preferable to have the optical source integrated directly on the chip. This can be accomplished using flip-chip bonding [26, 27], self-aligned assembly [28] or membrane-type integration [29]. For on-chip optical amplification, however, a monolithically integrated approach is required. This can be accomplished either via optical pumping (i.e. energy transfer from an optical beam at another wavelength to the desired wavelength near 1550 nm) or via electrical pumping (i.e. energy transfer from injected electrical current to the optical beam). Since the former ultimately

reduces to the prior problem of coupling an optical beam to the chip, only methods for achieving the latter will be discussed here.

For electrically pumped optical gain, silicon is not a natural material choice due to its indirect band gap which necessitates the interaction not only of an electrical carrier and a photon, but also a phonon to achieve electrical transition from the conduction band to the valence band. However, several approaches to optical emission from silicon have shown promise for wavelengths near 1550 nm. These include defect-engineering to encourage emission at the so-called "D1 line" [30, 31, 32], rare-earth-doped silicon [33, 34], and silicon nanoclusters incorporating either erbium [35, 36] or germanium [37].

An alternative approach is the so-called "hybrid platform": the use of III-V materials to provide gain in SOI waveguides by bonding the gain compound to an SOI waveguide and then etching/polishing away the excess III-V material [38]. This approach bears some similarity to the BESOI process for generating SOI as described in section 1.2.1.

Thus far, only flip-chip bonded lasers [39, 40] and the hybrid platform [41, 42] have been implemented as on-chip optical sources for silicon photonics in products actually brought to market.

### 1.2.6 Modulation and variable attenuation

Controlled attenuation in a photonic circuit is essential both as a means to encode data onto the optical beam and for ensuring uniform performance despite variations in temperature, transmission path length, and wavelength. The term "modulation" is typically reserved for signal bandwidths exceeding 1 GHz; a device which can only vary optical power at slower speeds is called a "variable optical attenuator" (VOA).

Traditional high-speed modulators often rely on either the Pockels effect (refractive index dependence on applied electric field) or the Franz-Keldysh effect (distortion of the semiconductor energy bands due to an applied electric field). However, the former is non-existent in unstrained silicon due to the centro-symmetry of the silicon crystal lattice (the Pockels effect has been reported in strained silicon, however [43]). The latter, while present, is relatively small compared to other approaches such as plasma dispersion and carrier injection [44, 45].

***Electro-absorption***

Controlled absorption in silicon can be achieved via the free-carrier effect [45] by situating the waveguide in the intrinsic region of a *p-i-n* diode such that forward biasing the junction injects carriers into the waveguide. Devices based on this approach have been demonstrated for speeds up to 200 MHz [46, 47] and are in commercial production [48].

Electro-absorption modulators that rely on the quantum-confined Stark effect [49-51] and the Franz-Keldysh effect [52] have also been demonstrated for germanium-on-silicon hybrid devices.

An interesting alternative approach is the use of ion implantation to produce deep-level charge states which can be manipulated to vary attenuation as suggested by Logan *et al.* [53].

***Electro-refraction***

An alternative to direct absorption is the use of either an optical interferometer or a resonant structure together with a means of tuning the optical path length by, for example, varying the real part of the refractive index. In silicon photonics this is generally accomplished using either the thermo-optic effect (i.e. the dependence of refractive index on temperature) or plasma dispersion (i.e. the variation in refractive index induced by the presence of free carriers). Both Mach-Zehnder

interferometers (described in detail in Chapter 4) and ring resonators (described in detail in Chapter 5) are commonly employed using both tuning approaches.

The method of choice for high-speed modulation in silicon is the plasma-dispersion effect [54], i.e. the dependence of refractive index on the free-charge concentration. Switches of this type were first demonstrated in 1987 [55]. Variable attenuation using a Fabry-Perot resonant structure was demonstrated in 1991 [56] and employing the Mach-Zehnder interferometer configuration in 1995 [57]. The cross-over into true modulation at gigahertz speeds was demonstrated in 2005 [58] with the highest modulation speed achieved to date being 40 Gb/s [59, 60].

Modulation using ring resonant structures has also emerged as a popular approach due to its compactness and efficiency. Ring-resonant modulators employing plasma dispersion were demonstrated in 2005 [61], with the fastest such modulator to date having been demonstrated in 2009 at more than 35 GHz [62].

***Thermo-optic variable attenuation***

Thermo-optically tuned Mach-Zehnder interferometers (MZI) were first demonstrated in SOI in 1991 [12] and have since seen significant improvements in both speed and switching power [63-69]. Thermo-optically tuned silicon ring resonators have also been demonstrated [70-74], as well as various other architectures such as Fabry-Perot resonators [75-77] and photonic crystal structures [78]. Thermo-optic tuning can achieve sub-milliwatt switching power [66, 74] and can approach GHz speeds [79], however it is unlikely to reach the multi-GHz speeds required for truly high-bandwidth data links. For slower applications thermal tuning is often a useful and straightforward approach that can be implemented as a back-end process step simply by locating a resistor in the vicinity of the waveguide. Thermo-optic tuning of a MZI will be discussed in detail in Chapter 4, while thermo-optic tuning of a ring resonator will be discussed in Chapter 5.

### 1.2.7 Photodetectors

Optical detection in silicon for wavelengths in the *C*-band is inherently problematic due to the fact that the band gap of silicon is approximately 1.1 eV while the photon energy at 1550 nm is only 0.8 eV. Absorption in silicon as a function of photon energy is shown in Fig. 1.10 (data calculated from [80]).

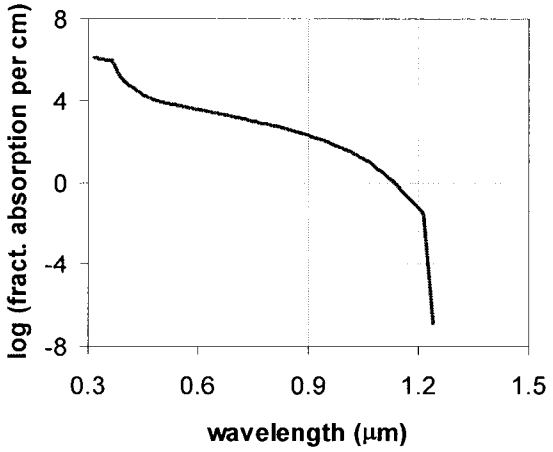


Fig. 1.10: Calculated log (absorption per cm) vs. wavelength in silicon using data from [80]. For the wavelength range shown, absorption drops to zero beyond a wavelength of 1.3 μm.

While coupling light out of the waveguide to a standard III-V photodetector is always possible (e.g. using one of the methods described in section 1.2.4) and has been demonstrated [81], this eliminates the possibility of fabricating the detector alongside the other functions on the chip, thus sacrificing one of the key benefits that make silicon photonics desirable. On-chip integration of the photodiode therefore requires either attaching small-band-gap materials to SOI during device fabrication or adding defect energy levels within the band gap to mediate the transition from the valence band to the conduction band.

***Integration of alternate materials***

As described in section 1.2.5, III-V compounds can be integrated with SOI using a wafer-bonding process followed by etching/polishing excess material such that optical modes travelling in the SOI waveguide overlap with the III-V material to

produce gain. The same approach can be used to produce absorption rather than gain; this technique has been used to fabricate optical detectors in SOI waveguides with an internal chip responsivity of 5.7 A/W operating at 2.5 Gb/s [82, 85].

Another approach is the integration of germanium (band gap approximately 0.7 eV), which can be accomplished either by epitaxial growth directly on silicon [83] or wafer bonding [84] to form a photodiode. The thickness of the germanium for low defect densities is limited by the lattice mismatch with silicon, but for photodiodes integrated within a waveguide the interaction length can be quite long, thus mitigating this problem somewhat [86]. Germanium-on-silicon photodetectors integrated on SOI rib waveguides were first demonstrated by Vivien *et al.* in 2007 [87] with 25 GHz bandwidth and 1 A/W responsivity, and have since been improved to more than 40 GHz bandwidth [88-90]. Germanium-on-silicon photodiodes have been incorporated into industrial products and brought to market [39].

***Defect mediated photodetectors***

Any disruption of the silicon crystal lattice (i.e. "defect") introduces new energy states to the band structure as will be explained further in Chapter 2. Energy states which fall within the band gap can provide a means of absorbing radiation at sub-band-gap photon energies. Waveguide-integrated photodiodes in SOI which take advantage of this effect were first demonstrated and patented in 2003 at Bookham Technology [91] using proton implantation with reported responsivity of 8 mA/W [92]. Similar devices were demonstrated and characterized with respect to annealing and bias for both proton and self-ion implantation by Knights *et al.* [93-95], and were shown to operate at megahertz speeds [96]. Similar devices were demonstrated using helium ion implantation [97], surface defect states [98, 99], and argon ion implantation [100].

Geis *et al.* were the first to show that these devices could operate not only as low-frequency tap monitors, but as high-speed detectors with 10-35 GHz bandwidth [101, 103], responsivities of 20 A/W [102], and even higher responsivities together with low leakage current when configured as phototransistors [103], making them competitive with traditional detector technologies.

## 1.3 Defect-mediated photodetection

There are three avenues of exploration with respect to defect-mediated photodetectors: (1) investigating the underlying physics of defect-mediated detection, (2) optimizing photodiode performance, and (3) monolithically integrating defect-mediated photodetectors with other photonic devices in order to achieve higher-level functionality. The work described in this thesis primarily deals with the first and third; an overview of each will be provided here and further review of what is known concerning the specific defects involved will be provided in Chapter 3.

### 1.3.1 Defect considerations

As illustrated in Fig. 1.10, silicon does not absorb light at wavelengths near 1.55 μm because the photon energy is too low (ignoring the effects of non-linear processes such as two-photon absorption). However, irradiation of silicon with deuterons was shown to induce absorption at wavelengths near 1.8 μm (i.e. 0.7 eV) by Fan *et al.* in 1959 [104]. This absorption band was attributed to the silicon divacancy lattice defect [105] by comparing annealing characteristics for infrared absorption data and electron paramagnetic resonance data obtained previously [106-108], establishing single-charge (i.e. transitions from neutral to either singly negative or singly positive charged) energy levels at $E_v$+0.25 eV and $E_c$-0.4 eV,

where $E_v$ and $E_c$ are the valence and conduction bands respectively. Corelli *et al.* [109] demonstrated via optical absorption studies that 20 minute anneals at 300 °C are sufficient to remove the divacancy, a result that has since been verified many times [e.g. 110-114]. More recently, however, it has been reported that there may be two annealing stages for the divacancy or divacancy complexes [115, 116] with the second occurring above 600 °C [117].

Annealing studies of the insertion loss in ion-implanted SOI waveguides for *C*-band illumination illustrated the same characteristic thermal dependence: low-loss characteristics were generally recovered after annealing at 300 deg C for 10 minutes [118, 94], suggesting that the divacancy is responsible for absorption and possibly photocurrent in defect-mediated waveguide photodetectors. Interestingly, the photocurrent measured by Knights *et al.* in [94] did not show the same monotonic decline seen for insertion loss versus annealing temperature; rather, the photocurrent increased for anneals up to 300 deg C and then fell abruptly for anneals beyond this temperature.

Geis *et al.* also reported large responsivities even after anneals that exceeded 450 deg C [102], a result which stands in marked contrast to the typical annealing characteristic described for divacancies above and which casts considerable doubt on their role. Furthermore, Geis observed bistability – the optical absorption of the devices could be enhanced by applying significant forward current, after which the device could be returned to its original state with time. Bistable behaviour is not a characteristic generally associated with the divacancy and suggests the involvement of other entities. One possibility is the boron-vacancy complex which has been known to exhibit bistable behaviour [119, 120] and has been reported to have donor states which coincide with other well-known deep levels thus rendering it easily confused with other defects such as the carbon-oxygen complex [121].

Bandwidth is another consideration that casts doubt on the potentially dominant role of the divacancy. For example, if optical absorption occurs by excitation of

electrons from the valence band to the $E_c$-0.4 eV defect state, then thermal excitation of the electron from this state to the conduction band at room temperature has a time constant on the order of microseconds without additional considerations such as tunnelling. This suggests that the device would be inherently limited to operation at megahertz frequencies or less, which may be consistent with measurements made by Knights *et al.* in [96] but not with the multi-gigahertz bandwidths demonstrated by Geis *et al.* in [101-103].

Thus although the divacancy is a good candidate for the primary optically active defect in these photodetectors, the evidence to date has largely been based on annealing characteristics and the fact that there is a corresponding absorption band in broad commonality; moreover the annealing characteristic of diode responsivity does not mimic that of absorption, thus casting some doubt on the premise that the divacancy is the primary defect involved.

Measurements done as part of this work shed additional light on the mechanism and involvement of the divacancy in optical absorption at 0.8 eV following ion implantation. Chapter 3 of this work will be devoted to observing and characterizing the optically active defect in defect-mediated photodiodes in order to establish which defect or defects play a significant role.

## 1.4 Thesis purpose and approach

An overview of general theory will be provided in Chapter 2. Theory and background of a more specific nature will be provided at the beginning of each successive chapter.

### 1.4.1 Defect characterization

While efforts have previously been made to identify the defect primarily responsible for detection at wavelengths within the *C*-band by comparing annealing characteristics for optical absorption and photocurrent with those of known defect energy states, the optically active defect energy state is not known with certainty. The work described in Chapter 3 provides a strong argument that the dominant role in defect-mediated detection is held by a defect with emission energy corresponding to the $E_c$-0.41 eV acceptor state of the silicon divacancy. Various properties of this defect were measured and used to model the performance of waveguide detectors also made and characterized as part of this work.

### 1.4.2 Integration of multiple on-chip functions with defect-mediated waveguide photodetectors

There has been excellent progress reported over the last five years by several groups in terms of improving the overall performance - both responsivity and bandwidth - of defect-mediated photodiodes. However, there had not, prior to this work, been a demonstration of the integration of defect-mediated detection with other functions on a chip. Chapter 4 will describe the demonstration of such monolithic integration in silicon in the form of a variable optical attenuator with a photodiode at the output to monitor the attenuator operation. The capabilities of the device will further be demonstrated by feeding back the signal from the monitor to the VOA in such a way as to accomplish channel levelling – i.e. the device will automatically hold optical output power within a narrow range for a wide range of optical input power variation.

Chapter 5 will describe the demonstration of a tuneable resonant defect-mediated detector. By incorporating a resonant structure, this device can achieve higher

responsivity than an in-line device of comparable length as well as the added advantage of improvements in signal-to-noise ratio as will be demonstrated. The tunability of the device serves both to make it operable at any wavelength within the *C*-band and to render it usable as a tap-monitored variable attenuator.

It is hoped that by combining an investigation into the underyling physics (Chapter 3) with demonstrations of higher-level functions (Chapters 4 and 5), the Engineering Physics ideal – to know "how" as well as to know "why" – is furthered.

## 1.5 Summary of contributions to the field

(1) A modified technique for defect optical characterization was developed.

(2) The dominant optically active defect in low-dose silicon-implanted and medium-dose boron-implanted photodiodes was observed and characterized in terms of its energy position in the band gap and photoionization cross-section at 1550 nm.

(3) Commercial variable optical attenuators were converted into photodiodes and used to characterize absorption and responsivity versus annealing temperature and implantation dose.

(4) A defect-mediated photodiode integrated with a variable optical attenuator was demonstrated, characterized, and modelled.

(5) A channel-leveller in which all the photonic functions were monolithically integrated in silicon was demonstrated and characterized.

(6) A tunable resonant defect-mediated photodetector was demonstrated, modelled, and characterized.

# Chapter 2

# Theory and background

The work described in this thesis combines defect characterization with planar waveguide device integration; this chapter will summarize carrier generation/recombination kinetics, optical waveguide theory, coupled mode theory and Complementary Metal Oxide Semiconductor (CMOS) processing techniques.

## 2.1 Defect states within the band gap

Much of the work described in this thesis concerns the identification of defect states produced within the silicon band gap by ion implantation and the role they play in mediating electron-hole pair generation via absorption of optical energy at photon energies below the band gap. This section will give a brief overview of the physics underlying mid-band defect states and the carrier kinetics associated with them.

### 2.1.1 Band gap

The basis of quantum mechanics is the Schrödinger equation:

$$H\Psi = E\Psi \tag{2.1}$$

where $H$ is the Hamiltonian operator, $E$ is energy, and $\Psi$ is the wave function. Expansion of the Schrödinger equation for an electron in one dimension yields Eq. (2.2):

$$\frac{d^2}{dx^2}\psi + \frac{2m}{\hbar^2}\big(E - V(x)\big)\psi = 0 \tag{2.2}$$

where $m$ is the mass of the electron, $\hbar$ is Planck's constant divided by $2\pi$, and $V(x)$ is the energy potential. Within a crystal lattice $V(x)$ is periodic and the solution takes the form of a Bloch function:

$$\psi(x) = u(x)e^{jkx} \tag{2.3}$$

where $u(x) = u(x+a) = u(x+2a)\ldots$ for lattice constant $a$, and $k$ is the momentum.

Treating the potential as a rectangular periodic potential for simplicity (often referred to as the Kronig-Penney model) as shown in Fig. 2.1 yields:

$$\frac{d^2u}{dx^2} + 2jk\frac{du}{dx} + \big(\alpha^2 - k^2\big)u = 0 \tag{2.4}$$

for the region inside the potential well and

$$\frac{d^2u}{dx^2} + 2jk\frac{du}{dx} + \big(\beta^2 - k^2\big)u = 0 \tag{2.5}$$

for the region outside the well, where $\alpha^2 = 2m_0\hbar^{-2}\varepsilon$ and $\beta^2 = 2m_0\hbar^{-2}(V_0 - \varepsilon)$ and $\varepsilon$ are the allowed energy levels of the electron.

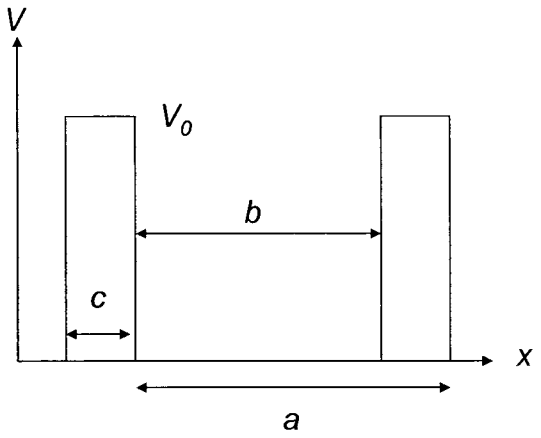


Fig. 2.1: Periodic potential according to the Kronig-Penney model.

The general solutions are given by Eq. (2.6) and Eq. (2.7):

$$u(x) = Ae^{j(\alpha-k)x} + Be^{-j(\alpha+k)x} \qquad 0 \le x \le b \quad (2.6)$$

$$u(x) = Ce^{(\beta-jk)x} + De^{-(\alpha+jk)x} \qquad -c < x < 0. \quad (2.7)$$

The coefficients *A, B, C, D* can be solved using the boundary conditions (i.e. $u(x)$ and $du/dx$ continuous at $x=0$ together with periodicity) to yield solutions for momentum $k(\varepsilon)$ according to Eq. (2.8):

$$k(\varepsilon) = \frac{1}{a}\arccos\left(L\left(\frac{\varepsilon}{V_0}\right)\right) \qquad (2.8)$$

where the function $L$ is defined according to Eq. (2.9)

$$L(E_r) = \frac{1-2E_r}{2\left(E_r - E_r^{\,2}\right)^{1/2}}\sinh\left[\left(4sr^2(1-E_r)\right)^{1/2}\right]\sin\left[4sE_r\right] + \cosh\left[\left(4sr^2\left(1-E_r\right)\right)^{1/2}\right]\cos\left(4sE_r\right) \qquad (2.9)$$

with $E_r=\varepsilon/V_0$, $s=2mV_0(b/2)^2/\hbar^2$, and $r=c/b$.

A plot of $E_r$ versus $L$ is shown in Fig. 2.2.

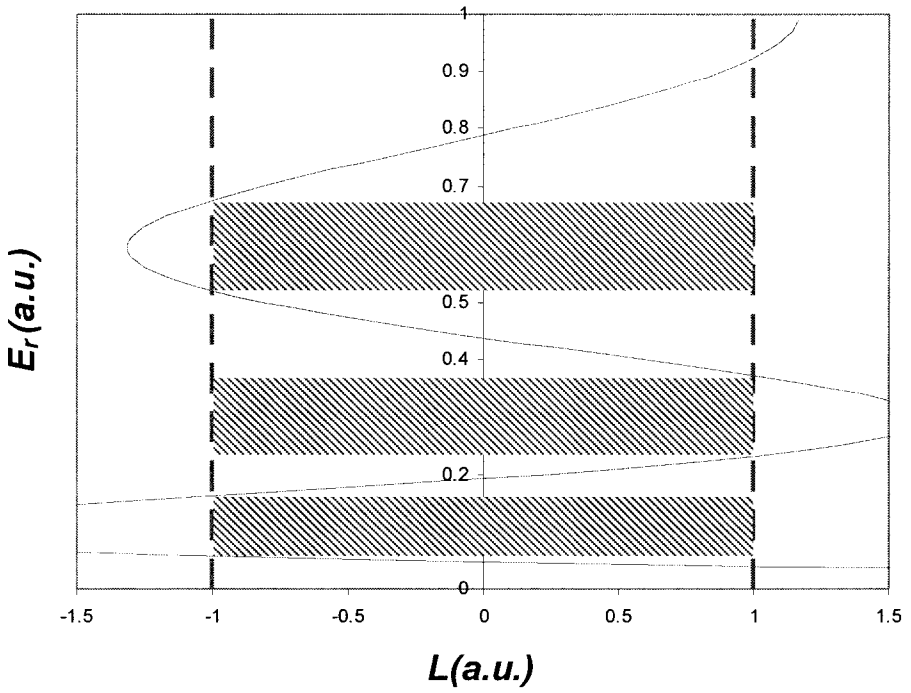


Fig. 2.2: Plot of $E_r$ vs. $L$ for arbitrary values $s = 36$, $r = 0.1$. The regions for which there is no solution within $-1 < L < 1$ are cross-hatched. Adapted from [122].

Since $k(\varepsilon)$ is limited to values for $L$ between -1 and 1, there are energies for which no real-valued solution for $k$ exists. These are the "forbidden" energies, or the "band gap".

### 2.1.2 Localized states

Although there are no energy states corresponding to real-valued $k$ within the band gap, there may be states corresponding to imaginary $k$. Recalling Eq. (2.6) it is apparent that imaginary $k$ implies an exponentially decreasing wavefunction rather than a plane wave solution; the solution is therefore localized in space – i.e. a defect in the crystal lattice. According to the Heisenberg Uncertainty Principle, a state localized in space is inherently non-localized in $k$-space.

Energy states corresponding to localized defects can therefore exist within the band gap and are delocalized in *k*-space. States that are situated more than several *kT* from the nearest band edge are typically described as "deep states" or "deep levels". These states are often referred to as "traps" because charge carriers can be held by them before being re-emitted with a characteristic time constant.

### 2.1.3 Band-to-band optical absorption in silicon

The mechanism by which carriers can be excited from the uppermost filled band (the valence band) to the lowest empty band (the conduction band) via optical excitation is shown in Fig. 2.3. Because silicon is an indirect band gap semiconductor (i.e. the valence band maximum is not aligned in *k*-space with the conduction band minimum) a photon must generally excite the electron to the conduction band-edge well above the minimum, after which the electron can transition to the bottom of the conduction band by releasing a phonon. For excitation by a photon equivalent to the band gap, absorption of both a photon and a phonon is required in order to complete the transition.

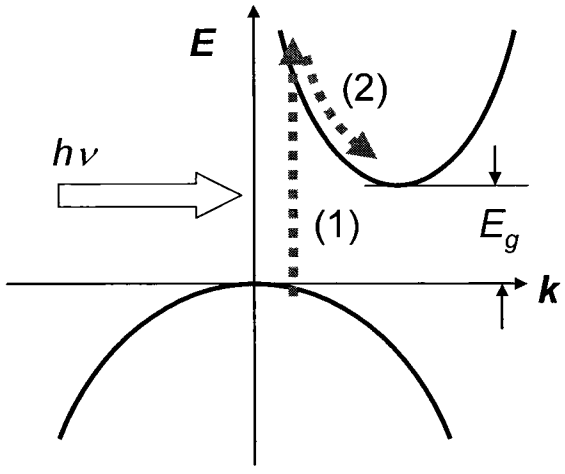


Fig. 2.3: Band-to-band optical absorption in silicon. The process involves two steps: (1) a photon is absorbed, and (2) a phonon is emitted. Adapted from [123].

### 2.1.4 Carrier generation/recombination kinetics

Four charge-carrier transitions are possible between band states and a single trap state: electron capture/emission to the conduction band and electron capture/emission to the valence band. These four transitions are illustrated in Fig. 2.4.

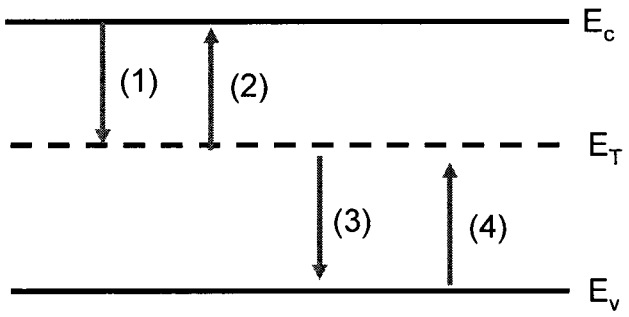


Fig. 2.4: Electron transitions between bands and a trap state: (1) electron capture from the conduction band, (2) electron emission to the conduction band, (3) electron emission (hole capture) to (from) the valence band, (4) electron capture (hole emission) to (from) the valence band. Adapted from [124].

The transition rates are dependent on the concentration of available charge carriers, the concentration of available states to which the carriers can transition, and a proportionality constant; the four transition rates are given in Eq. (2.10) [125]:

$$\begin{aligned} r_1 &= c_n n p_t \\ r_2 &= e_n n_t \\ r_3 &= c_p p n_t \\ r_4 &= e_p p_t \end{aligned} \tag{2.10}$$

where $n$ is the conduction band electron concentration, $p$ is the valence band hole concentration, $n_t = N_T f_t$ is the concentration of trapped electrons, and $p_t = N_T(1-f_t)$ is the concentration of trapped holes. The occupancy probability factor $f_t$ of the

total trap concentration $N_T$ is given according to the Fermi-Dirac distribution function [126]:

$$f_t = \frac{1}{1+e^{(E_t-E_F)/kT}} \tag{2.11}$$

where $E_t$ is the energy of the trap state, $E_F$ is the Fermi energy (i.e. the energy at which the probability of occupancy is 0.5), $k$ is the Boltzmann constant, and $T$ is temperature. Referring to Eq. (2.11), it is apparent that for $E_F >> E_T$ the traps will fill with electrons until $n_t \sim N_T$, while with $E_F << E_T$ the traps will fill with holes until $p_t \sim N_T$.

The coefficients $c_n$, $c_p$ can be expressed as the product of thermal velocity and cross-section of capture for their respective carriers. This is somewhat intuitive: the probability of carrier capture is the ratio of volume a trap occupies to the total volume. The volume occupied by a trap (in terms of mobile carriers) per unit time is the cylinder swept out by its cross-sectional area $\sigma$ and the distance travelled per unit time by a carrier: thermal velocity $v_{nth}$ (electrons) or $v_{pth}$ (holes).

At thermal equilibrium (and for small deviations from thermal equilibrium) the capture and emission rates must be equal:

$$v_{nth}\sigma_n n p_t = e_n n_t \tag{2.12}$$

$$v_{pth}\sigma_p p n_t = e_p p_t \,. \tag{2.13}$$

Solving for the emission rates yields

$$e_p = v_{pth}\sigma_p N_v e^{-(E_t-E_v)/kT} \tag{2.14}$$

$$e_n = v_{nth}\sigma_n N_c e^{-(E_c-E_t)/kT} \tag{2.15}$$

where $N_c$ and $N_v$ are the effective densities of states in the conduction and valence bands respectively.

Thermal velocity is proportional to $T^{1/2}$ according to Eq. (2.16):

$$v_{th} = \left( \frac{3kT}{m^*} \right)^{1/2} \tag{2.16}$$

with $m^*$ the effective mass of the carrier in question, while the effective density of states is proportional to $T^{3/2}$ according to Eq. (2.17):

$$N_{c/v} = 2\left( \frac{2\pi m_{n/p}{}^* kT}{h^2} \right)^{3/2}. \tag{2.17}$$

Therefore the emission rates are proportional to $T^2$ as well as having an exponential temperature dependence.

### 2.1.5 Generation, recombination and trapping

Recalling Eq. (2.10) and Fig. 2.4, it is apparent that there are four possible roles a trap can play in the carrier kinetics:

(1) for $n >> e_p/c_n$ and $p << e_n/c_p$, the trap will be in thermal equilibrium with the conduction band and acts as an electron trap,

(2) for $n << e_p/c_n$ and $p >> e_n/c_p$, the trap will be in thermal equilibrium with the valence band and acts as a hole trap,

(3) for $n >> e_p/c_n$ and $p >> e_n/c_p$, the trap facilitates electron transitions to the valence band and is therefore a recombination centre, and

(4) for $n << e_p/c_n$ and $p << e_n/c_p$, the trap facilitates electron transitions to the conduction band and is therefore a generation centre.

### 2.1.6 Steady-state recombination rate

When carriers are injected (whether through electrical or optical excitation) the carrier concentrations differ from their thermal equilibrium values.

The overall change in trapped electron density is described by Eq. (2.18):

$$-\frac{dn_T}{dt} = r_3 - r_4 - r_1 + r_2 . \tag{2.18}$$

Under the assumption that the capture and emission rates do not significantly change from their equilibrium values, substituting Eqs. (2.10)–(2.15) into Eq. (2.18) leads to an expression for the recombination rate [127]:

$$U = \frac{N_t c_n c_p \left(np - n_i^2\right)}{c_n \left(n + n_i e^{(E_T - E_i)/kT}\right) + c_p \left(p + p_i e^{-(E_T - E_i)/kT}\right)} \tag{2.19}$$

and for the density of trapped charge:

$$n_T = N_T \frac{c_n n + c_p n_i e^{-(E_T - E_i)/kT}}{c_n \left(n + n_i e^{(E_T - E_i)/kT}\right) + c_p \left(p + n_i e^{-(E_T - E_i)/kT}\right)} \tag{2.20}$$

$$p_T = N_T \frac{c_n n_i e^{(E_T - E_i)/kT} + c_p p}{c_n \left(n + n_i e^{(E_T - E_i)/kT}\right) + c_p \left(p + n_i e^{-(E_T - E_i)/kT}\right)} . \tag{2.21}$$

With the simplifying assumption that $\sigma_n = \sigma_p = \sigma$, the recombination rate can be reduced to Eq. (2.22):

$$U = \sigma v_{th} N_t \frac{\left(np - n_i^2\right)}{n + p + 2n_i \cosh\left(\left(E_T - E_i\right)/kT\right)} . \tag{2.22}$$

Defining minority carrier lifetimes $\tau_p$ and $\tau_n$ as the ratio of the excess minority carrier concentration to the recombination rate, expressions for the minority carrier lifetime in *n*-type and *p*-type material are obtained according to Eq. (2.23) and Eq. (2.24) respectively:

$$\tau_p = \frac{1}{\sigma_p v_{th} N_T} \tag{2.23}$$

$$\tau_n = \frac{1}{\sigma_n v_{th} N_T}. \tag{2.24}$$

Thus, increased trap density leads to a reduction in minority carrier lifetime.

## 2.2 *p-n* junction theory

By doping a semiconductor with impurities (e.g. phosphorus or boron in silicon) that introduce energy levels within the band gap very close to the band edge, thermal energy is generally sufficient to ionize the dopant such that the carrier density becomes approximately equivalent to the dopant density. An abrupt junction of two oppositely doped regions causes carriers to diffuse such that a potential is created and carriers are depleted from the space-charge region on either side of the junction. At equilibrium the total ionized charge on either side must be balanced according to Eq. (2.25):

$$qAx_p N_a = qAx_n N_d \tag{2.25}$$

where $N_a$ and $N_d$ are the acceptor and donor dopant concentrations, $q$ is the carrier charge, $A$ is the cross-sectional area of the junction, and $x_p$, $x_n$ are the penetration of the space-charge region into the $p$ and $n$ material respectively.

Employing Poisson's equation in one dimension and neglecting free carriers in the space-charge region yields a relation between dopant density and potential on the $n$ and $p$ sides of the junction according to Eq. (2.26)

$$\begin{aligned} -\frac{\delta^2 V}{\delta x^2} &= \frac{q}{\varepsilon} N_d \\ -\frac{\delta^2 V}{\delta x^2} &= \frac{-q}{\varepsilon} N_a \end{aligned} \tag{2.26}$$

where $\varepsilon$ is the permittivity of the semiconductor.

Solving for $V$ yields Eq. (2.27) for the built-in potential (i.e. potential with no external bias applied):

$$V_0 = \frac{W^2 q N_a N_d}{2\varepsilon\left(N_a + N_d\right)} \tag{2.27}$$

where $W$ is the width of the space-charge region.

For a one-sided abrupt junction (i.e. a junction in which the dopant concentration on one side far exceeds the dopant concentration on the other) the expression simplifies to Eq. (2.28):

$$V_{bi} = \frac{W^2 q N_L}{2\varepsilon} \tag{2.28}$$

where $N_L$ is the lower of the two dopant concentrations. Under applied bias $V_b$, $V_0$ is replaced with $V = V_0 - V_{bi}$.

The depletion-layer capacitance per unit area of the junction (approximating the junction as a parallel-plate capacitor) is derived according to $C = dQ/dV$, or:

$$C = \frac{\varepsilon}{W} = \left( \frac{q\varepsilon N_a}{2(V_{bi} + V_a)} \right)^{1/2} \tag{2.29}$$

with applied reverse bias $V_a$ for the case of an $n^+p$ junction.

Trapped charge within the depletion layer leads to either an increase (acceptor traps in this case) or a decrease (compensating donor traps) in the effective dopant density. Capacitance per unit area for the case of trapped charge is therefore modified according to Eq. (2.30):

$$C = \frac{\varepsilon}{W} = \left( \frac{q\varepsilon\left(N_a \pm fN_T\right)}{2(V_{bi} + V_a)} \right)^{1/2} \tag{2.30}$$

where $N_T$ is the total trap density and $f$ is the occupancy factor.

### 2.2.1 Effect of trap density on junction current

The current density across an ideal junction is given by the Shockley equation:

$$J = q\left(\frac{p_{n0}}{\sqrt{D_p\tau_p}} + \frac{n_{p0}}{\sqrt{D_n\tau_n}}\right)\left(e^{qV/kT} - 1\right) \tag{2.31}$$

where $n_{p0}$, $p_{n0}$ are the thermal equilibrium minority carrier densities and $D_{n,p} = kt\mu_{n,p}/q$ are the diffusion coefficients of holes and electrons.

***Reverse bias leakage current***

Within the space-charge region, $n \sim p \sim 0$ and so the trap acts primarily as a generation centre as described in section 2.1.5, thus increasing the drift component of current density. The diffusion component of current density also depends on minority carrier lifetime; the overall expression for reverse leakage current is given in Eq. (2.32):

$$J_R = q\left(\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D} + \frac{n_i W}{\tau_n}\right). \tag{2.32}$$

Recalling Eq. (2.23) and Eq. (2.24) it is evident that under reverse bias, the leakage current will increase with higher trap densities.

***Low-injection minority current***

At forward bias minority carriers are injected into the junction such that both $n$ and $p$ are of relatively high concentration and the traps act as recombination centres. Integrating the recombination rate (Eq. (2.22)) over the width of the junction produces Eq. (2.33) [127]:

$$J_{rec} \sim \frac{1}{2} qW\sigma v_{th} N_T n_i e^{(qV/2kT)}. \tag{2.33}$$

As with reverse leakage current, the minority current under low-injection conditions increases with trap density.

## 2.3 Optical propagation in planar waveguides

Maxwell's equations summarize the relationship between electrical and magnetic fields in linear, isotropic, homogenous, and non-conducting media as follows:

$$\nabla \cdot \mathbf{E} = 0 \tag{2.34}$$

$$\nabla \cdot \mathbf{B} = 0 \tag{2.35}$$

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \tag{2.36}$$

$$\nabla \times \mathbf{B} = \mu_0 \varepsilon_0 n^2 \frac{\partial \mathbf{E}}{\partial t} \tag{2.37}$$

where **E** and **B** are the electric and magnetic fields respectively, $\mu_0$ is the vacuum magnetic permeability, $\varepsilon_0$ is the vacuum electric permittivity, $n$ is the optical refractive index of the medium, and $t$ is time.

For **E** and **B** treated as optical waves propagating along the $z$ axis with field distribution dictated by the optical index profile of the medium, appropriate expressions are:

$$\mathbf{E} = \mathbf{E}(x, y)e^{j(k_z z - \omega t)} \tag{2.38}$$

$$\mathbf{B} = \mathbf{B}(x, y)e^{j(k_z z - \omega t)}. \tag{2.39}$$

where $\omega$ is the optical angular frequency and $k_z$ is the propagation constant in the $z$ direction.

For propagation in a layered slab waveguide structure composed of materials with optical indices $n_s$,(substrate layer), $n_w$ (waveguide layer), and $n_c$ (cladding layer) as shown in Fig. 2.5, the fields may be decomposed into transverse electric (TE)

and transverse magnetic (TM) polarizations such that the field either has no magnetic component (TE) or electric component (TM) in the $y$ direction.

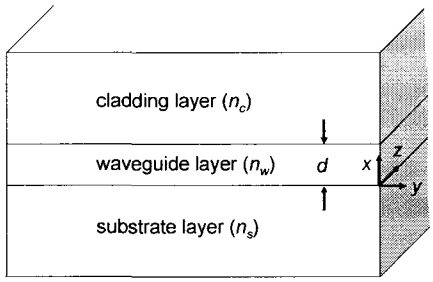


Fig. 2.5: Slab waveguide structure composed of three layers: substrate, waveguide, and cladding.

Considering TE polarization, denoting $E_x$, $E_y$, $E_z$, $B_x$, $B_y$, $B_z$ as the electric and magnetic field components along each axis, and substituting Eq. (2.38) and Eq. (2.39) into Eq. (2.36) and Eq. (2.37) yields:

$$B_z = -\frac{1}{j\omega}\frac{dE_y}{dx} \tag{2.40}$$

$$B_x = -\frac{k_z}{\omega}E_y \tag{2.41}$$

where the symmetry of the problem has been used to infer that derivatives with respect to $y$ must vanish.

Taking the curl of Eq. (2.36) and Eq. (2.37) produces the wave equations:

$$\nabla^2\mathbf{E} = \mu_0\varepsilon\frac{\partial^2\mathbf{E}}{\partial t^2} \tag{2.42}$$

$$\nabla^2\mathbf{B} = \mu_0\varepsilon\frac{\partial^2\mathbf{B}}{\partial t^2} \tag{2.43}$$

and again substituting Eq. (2.38) and Eq. (2.39) together with the restriction to TE polarization yields Eq. (2.44)

$$\frac{d^2E_y}{dx^2} + (k^2 - k_z^2)E_y = 0 \tag{2.44}$$

where $k = \omega n / c$.

Applying the boundary conditions that tangential electric ($E_y$) and magnetic ($H_z$) fields must be continuous at the boundaries of the waveguide layer, and that each must vanish at $x = \pm\infty$ leads to solutions for the electric field in the cladding, waveguide, and substrate:

$$E_y(x) = c_c e^{-\alpha_c x} e^{j(k_z z - \omega t)} \qquad \text{for } x \geq 0 \tag{2.45}$$

$$E_y(x) = c_w \cos(k_x x + \phi) e^{j(k_z z - \omega t)} \qquad \text{for } -d \leq x \leq 0 \tag{2.46}$$

$$E_y(x) = c_s e^{\alpha_s (x+d)} e^{j(k_z z - \omega t)} \qquad \text{for } x \leq -d \tag{2.47}$$

where $c_c$, $c_w$, and $c_s$ are constants in the cladding, waveguide, and substrate respectively determined by boundary conditions, $\alpha_c$ and $\alpha_s$ are decay constants in the cladding and substrate, $k_x$ is a propagation constant within the waveguide layer, and $\phi$ is a phase term for generality. Here we take $x = 0$ at the interface between the cladding layer and the waveguide layer.

Applying Eq. (2.40) to the expressions derived for $E_y$ yields the following for $B_z$:

$$B_z(x) = \frac{-\alpha_c c_c}{j\omega} e^{-\alpha_c x} e^{j(k_z z - \omega t)} \tag{2.48}$$

$$B_z(x) = \frac{-k_x c_w}{j\omega} \sin(k_x x + \phi) e^{j(k_z z - \omega t)} \tag{2.49}$$

$$B_z(x) = \frac{\alpha_s c_s}{j\omega} e^{\alpha_s (x+d)} e^{j(k_z z - \omega t)} \tag{2.50}$$

and from Eq. (2.44) we have the relations:

$$k_x^2 + k_z^2 = k_w^2 \tag{2.51}$$

$$k_c^2 = k_z^2 - \alpha_c^2 \tag{2.52}$$

$$k_s^2 = k_z^2 - \alpha_s^2 \tag{2.53}$$

where $k_s = \varepsilon_0\mu_0 n_s\omega$, $k_c = \varepsilon_0\mu_0 n_c\omega$, and $k_w = \varepsilon_0\mu_0 n_w\omega$.

From the continuity of electric and magnetic fields at $x$=0:

$$c_c = c_w \cos(\phi) \tag{2.54}$$

$$c_c = c_w \frac{k_x}{\alpha_c}\sin(\phi) \tag{2.55}$$

and for $x$=-$d$:

$$c_s = c_w \cos(k_x d - \phi) \tag{2.56}$$

$$c_s = c_w \frac{k_x}{\alpha_s}\sin(k_x d - \phi)\,. \tag{2.57}$$

Eliminating $c_c$ and $c_w$ yields

$$\alpha_c = k_x \tan(\phi) \tag{2.58}$$

and eliminating $c_s$ and $c_w$ yields

$$\alpha_s = k_x \tan(k_x d - \phi)\,. \tag{2.59}$$

Solving for and eliminating $\phi$ provides an eigenequation for the TE modes:

$$\tan(k_x d) = \frac{(\alpha_c + \alpha_s)k_x}{k_x^2 - \alpha_c\alpha_s} \tag{2.60}$$

where

$$\alpha_{c,s} = \left[k^2\left(n_w^2 - n_{c,s}^2\right) - k_x^2\right]^{1/2} \tag{2.61}$$

$$E_y = c_w e^{jk_z z} \begin{cases} \cos\phi e^{-\alpha_c x} & x \geq 0 \\ \cos\left(k_x x + \phi\right) & -d \leq x \leq 0 \\ \cos\left(-k_x d + \phi\right) e^{\alpha_s (x+d)} & x \leq -d \end{cases} \tag{2.62}$$

where $\phi$ is determined by Eq. (2.58) and proportionality constant $c_w$ is determined by normalizing total power flow.

A similar approach leads to solutions for the TM modes in the waveguide [128].

It is clear from Eq. (2.62) that some of the optical power propagates in the cladding and substrate as well as the waveguide layer – this is referred to as the "evanescent field". The electric field strength outside the waveguide layer diminishes exponentially while the field within the waveguide layer is sinusoidal in nature. The eigenmodes are characterized either by 'even' or 'odd' sinusoidal symmetry within the waveguide layer. Fig. 2.6 shows typical electric field profiles for the lowest-order modes in such a structure where $n_c < n_s < n_w$.

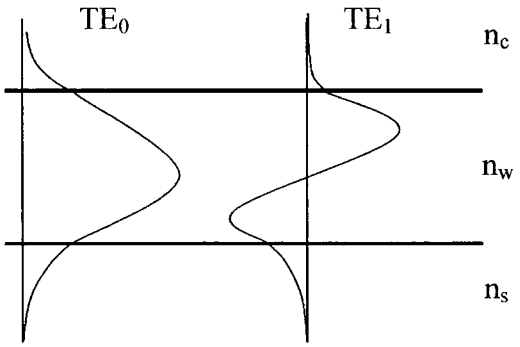


Fig. 2.6: Electric field profile for a TE even ($TE_0$) and TE odd ($TE_1$) mode in a dielectric slab waveguide.

From Eq. (2.52) and Eq. (2.53) it is apparent that for either $n_c > n_w$ or $n_s > n_w$ one or both of the decay constants $\alpha_c$, $\alpha_s$, becomes imaginary such that the field in Eq. (2.62) no longer vanishes at x = ± ∞ outside the waveguide layer; i.e. the waveguide no longer confines the mode but rather radiates power. Considering the second case in which power radiates to the substrate, the mode ceases to be confined for $k_s = k_z$. Then Eq. (2.60) reduces to:

$$k_x d = \tan^{-1}\frac{\alpha_c}{k_x} + m\pi \tag{2.63}$$

and substituting Eq. (2.51), Eq. (2.52) produces the cutoff condition Eq. (2.64):

$$kd\sqrt{n_w^2 - n_s^2} = \tan^{-1}\frac{\sqrt{n_s^2 - n_c^2}}{\sqrt{n_w^2 - n_c^2}} + m\pi\,. \tag{2.64}$$

For a given optical frequency and optical index profile, therefore, Eq. (2.64) determines the slab thickness $d$ at which the waveguide ceases to confine optical power. It is apparent that for the special case in which $n_s = n_c$ (i.e. a symmetric slab waveguide), the equation holds true for all $d$ and $k$ with $m$=0, i.e. the lowest-order mode is not cut off even for arbitrarily small slab widths. For asymmetric guides however, there is a minimum slab width at which each mode will guide; the lowest-order mode (i.e. $m$=0) will be the last to encounter cutoff as $d$ approaches zero. Under the condition that the index profile, slab thickness, and optical frequency are such that every mode is beyond cutoff except the lowest order mode then the waveguide is said to be "single-mode". This is a very useful regime in which to design waveguides since it reduces the electromagnetic field to a single possible profile, thus enabling the designer to know with certainty the distribution of optical power within the waveguide.

A plot of the TE mode solutions for an air-clad slab waveguide in SOI for 1.55 μm wavelength is shown in Fig. 2.7. For these parameters the $d$ = 0.6 μm case supports three modes, while the $d$ = 0.15 μm case is single-mode.

An effective index governing mode propagation can be defined analogously to the bulk material indices according to Eq. (2.65):

$$n_{eff} = \frac{\lambda}{2\pi}k_z \tag{2.65}$$

where $\lambda$ is the free-space wavelength. It is apparent from Fig. 2.7 that the lowest-order mode necessarily has the lowest $k_x$ and therefore the largest $n_{eff}$ according to Eq. (2.51) and Eq. (2.65).

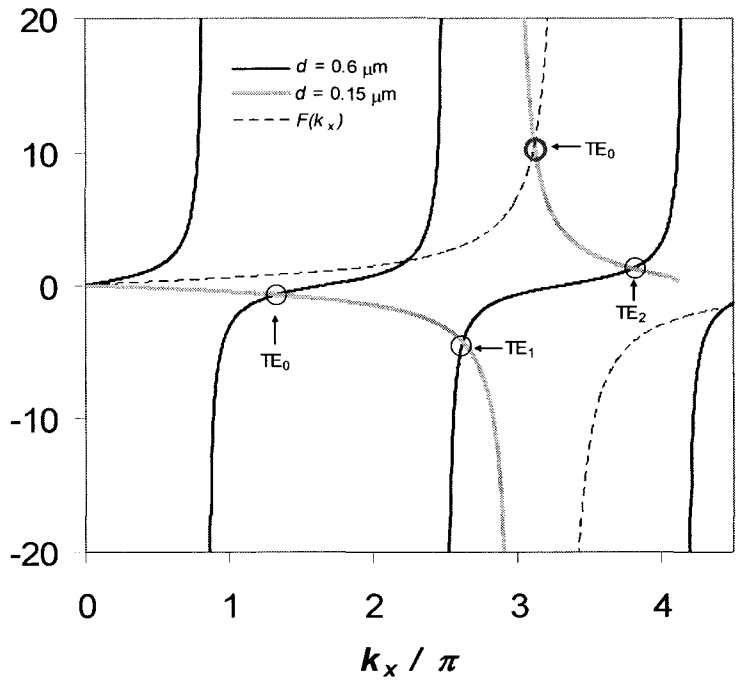


Fig. 2.7: Mode solutions for an air-clad slab waveguide in SOI ($n_c$ = 1, $n_w$ = 3.5, $n_s$ = 1.44) according to Eq. (2.60) where $F(k_x)$ is the right-hand side expression and curves $d$= 0.6 μm, $d$ = 0.15 μm are the left-hand side expression for slab thicknesses 0.6 μm and 0.15 μm respectively.

### 2.3.1 Ray optics approach

Eq. (2.46) suggests that for the electric field within the slab the electric field can be thought of as a plane wave with wave vector $k_w$ reflecting from the surfaces of the waveguide layer via total internal reflection. The angle of $k_x$ relative to $k_z$ is determined by Eq. (2.51); each mode therefore has a characteristic "angle of incidence" $\theta$ associated with it such that $\sin\theta = k_z/k_w$.

## 2.4 Three-dimensional waveguides

Optical transmission within a photonic circuit requires confinement not just in the vertical axis but in the lateral axis as well thus necessitating a region of reduced optical index on either side of the waveguide as well as above and below it. Such a structure is called a "wire" waveguide. However, in practice it is often beneficial to make electrical contact to the waveguide core and it is therefore preferable not to have the waveguide entirely encapsulated in silicon dioxide or air cladding. The most prevalent approach is the "rib" waveguide. Both structures are illustrated in Fig. 2.8.

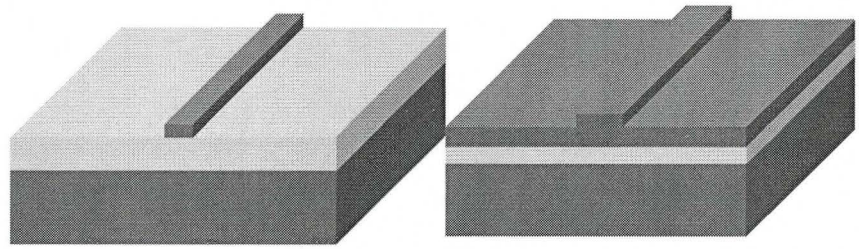

Fig. 2.8: SOI wire waveguide (left) and rib waveguide (right). Vertical confinement is provided by an oxide layer ($n \sim 1.44$) and an upper cladding layer (air, oxide, nitride, etc.) while lateral confinement is provided by the wire or rib geometry.

## 2.5 Effective index method

Approximations of the effective index for guided modes can be generated for a rib or wire waveguide structure using the effective index method (EIM). In this approach the waveguide is treated as an amalgamation of three individual regions, each of which can be treated as a slab waveguide. The effective index derived from each region is then used to construct a conceptual slab waveguide whose core layer corresponds in thickness to the width of the 3D rib structure and solved accordingly. The analytical approach is illustrated in Fig. 2.9.

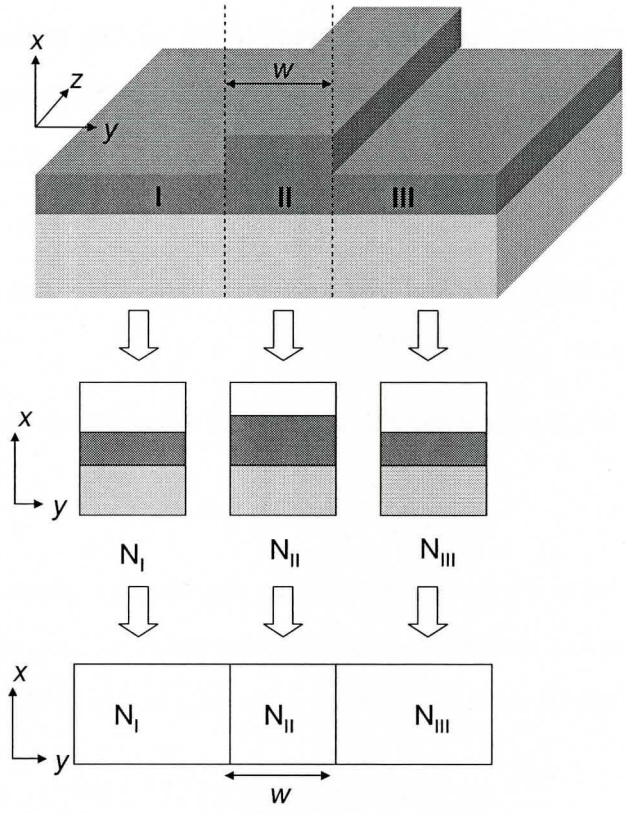


Fig. 2.9: Model of the analysis used in the effective index method, adapted from [129].

## 2.6 Beam propagation method

Although the effective index method provides an estimate of the effective indices for guided modes in a rib structure, it cannot provide a mode profile which is often required in order to calculate the extent to which guided modes interact either with each other or with other features on a chip. There are several analytical approaches which can be used to derive approximate solutions for the mode profile (e.g. Marcatili's method [130]) but in practice it is simpler to use computational algorithms such as the beam propagation method (BPM), for which a commercial software package called RSoft BeamPROP [131] is available.

### 2.6.1 BPM approach

Referring back to the wave equation derived in Eq. (2.42), treating the field as a scalar, and expanding the left-hand side yields the Helmoholtz equation:

$$\frac{\partial^2\varphi}{\partial x^2}+\frac{\partial^2\varphi}{\partial y^2}+\frac{\partial^2\varphi}{\partial z^2}+k(x,y,z)^2\varphi=0 \tag{2.66}$$

where $k(x,y,z) = k_0 n(x,y,z)$, and the scalar electric field has been expressed according to $E(x,y,z,t) = \varphi(x,y,z)e^{-j\omega t}$.

The rapid phase variation in $\varphi$ can be factored out using the ansatz:

$$\varphi(x,y,z)=u(x,y,z)e^{jk'z} \tag{2.67}$$

where $k' = k_0 n'$ is a constant representing the average phase of $\varphi$ called the reference wavenumber for a reference refractive index $n'$. Eq. (2.66) then yields an expression for the slowly varying field according to Eq. (2.68):

$$\frac{\partial^2 u}{\partial z^2}+2jk'\frac{du}{dz}+\frac{\partial^2 u}{\partial x^2}+\frac{\partial^2 u}{\partial y^2}+\left(k^2-k'^2\right)u=0. \tag{2.68}$$

If the variation of $u$ in the $z$ direction can be assumed to be slow such that the second derivative with respect to $z$ may be neglected with respect to the first derivative, then Eq. (2.68) reduces to Eq. (2.69):

$$\frac{du}{dz}=\frac{j}{2k'}\left(\frac{\partial^2 u}{\partial x^2}+\frac{\partial^2 u}{\partial y^2}+\left(k^2-k'^2\right)u\right). \tag{2.69}$$

This is the well-known paraxial approximation, and holds true for optical fields that are (a) propagating in the $z$ direction or at small angles from it, and (b) not subject to abrupt refractive index changes along the $z$ axis. For a straight dielectric/semiconductor waveguide structure both of these approximations are generally valid.

Eq. (2.69) thus provides a means of solving sequential cross-sectional planes of a propagating electric field using an algorithmic approach: the initial field is used as a launch condition at $z$=0 and the right-hand side expression is solved (e.g. by the well known implicit finite difference approach) to yield a modification to the field from one plane to the next. The method can also be adapted to include polarization effects by using the vector wave equation rather than the scalar approximation described here: a complete description of this approach is given in [132].

### 2.6.2 Computing mode solutions using BPM

The BPM method can be employed to solve for the electromagnetic field profile of a guided mode using at least three approaches: filtering, imaginary distance BPM and the correlation method. For the work described in this thesis the first two techniques were generally employed and will be described here.

***Filtering the mode***

The field profile within the waveguide may be expanded in terms of the orthogonal modes of the structure according to Eq. (2.70):

$$\varphi(x,y,z) = \sum_m c_m \varphi_m(x,y) e^{j\beta_m z} \tag{2.70}$$

where $c_m$ are the coefficients of the expansion, $\varphi_m(x,y)$ are the mode profiles, and $\beta_m$ are the propagation coefficients corresponding to each mode.

Launching an arbitrary (e.g. Gaussian) field within a structure known to be singlemode for a given polarization (e.g. by the effective index method) excites many modes, but since only one is guided the remainder – having imaginary propagation constants $\beta_m$ - are gradually radiated from the waveguide until all remaining optical power resides only in the fundamental mode. This approach is very simple and is readily available with any BPM simulation software, however

it can take a very long simulation to achieve a good approximation for the fundamental mode, and requires that the user know the structure to be singlemode. Clearly it is also quite useless as a means to generate field profiles for higher-order modes in a multimode structure.

***Imaginary distance propagation***

The imaginary distance propagation method is the converse of the filtering approach: the $z$ axis is treated as imaginary such that all the guided modes encounter exponential growth with respect to propagation distance $z$. The mode with the largest propagation constant $\beta_m$ expands the most rapidly, however, and since this is by definition the fundamental mode as explained in the previous section, the field rapidly converges to a profile corresponding to the fundamental mode (the field is normalized at each step). Higher-order modes can be obtained by repeating the simulation while subtracting out the previously solved mode(s) such that the higher mode dominates the propagation.

## 2.7 Coupled mode theory

The photonic devices described in this work employ directional couplers to split power between rib waveguides. A directional coupler in this sense consists of a region in which the two waveguides are located adjacent to each other with a small gap in between such that the structure behaves as a single waveguide with two optical modes (henceforth referred to as "compound modes") rather than as two isolated singlemode waveguides. Since the compound modes of the overall structure have different propagation constants, they beat against each other such that optical power cycles between the two waveguides. A diagram of this structure is shown in Fig. 2.10.

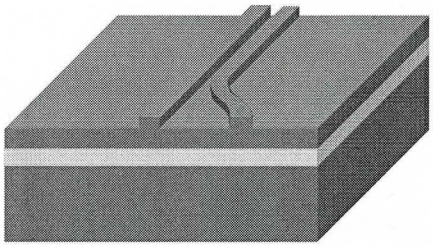

Fig. 2.10: Directional rib waveguide structure in SOI.

### 2.7.1 Derivation of coupled-mode equations

For a device consisting of two rib waveguides $A$ and $B$ in close proximity, the overall structure will support several modes $\Phi_t$. Since the normal modes form a basis set, any field propagating within the overall structure can be expanded as a linear combination of them. Considering the case of a system which either supports only two normal modes or in which the launch fields primarily excite only two normal modes, this expansion yields Eq. (2.71):

$$\begin{aligned} \psi_A(x,y) &= a_1\phi_1(x,y) + a_2\phi_2(x,y) \\ \psi_B(x,y) &= b_1\phi_1(x,y) + b_2\phi_2(x,y) \end{aligned} \tag{2.71}$$

where $\Psi_A$ and $\Psi_B$ are arbitrary field profiles in which the optical power is largely confined either to waveguide $A$ or to waveguide $B$ respectively.

The propagation of modes $\Phi_1$ and $\Phi_2$ is described by Eq. (2.72):

$$\Phi_m(x,y,z,t) = \phi_m(x,y)e^{-j(\omega t-\beta_m z)}. \tag{2.72}$$

For the remainder of this section the time dependence given by the factor $e^{-j\omega t}$ will be left unwritten for clarity.

Although the compound field can be expanded in terms of $\phi_m$ with constant coefficients for a particular propagation length $z$, the composition of the field varies with $z$ according to Eq. (2.73):

$$A(z)\psi_A(x,y) + B(z)\psi_B(x,y) = f_1\phi_1(x,y)e^{j\beta_1 z} + f_2\phi_2(x,y)e^{j\beta_2 z}. \tag{2.73}$$

Substituting Eq. (2.71) into Eq. (2.73) yields

$$\begin{aligned}\left(a_1A(z)+b_1B(z)\right)\phi_1(x,y)+\left(a_2A(z)+b_2B(z)\right)\phi_2(x,y)=\\ f_1e^{j\beta_1 z}\phi_1(x,y)+f_2e^{j\beta_2 z}\phi_2(x,y)\end{aligned} \tag{2.74}$$

and since $\phi_1$, $\phi_2$ are orthogonal the coefficients can be equated to yield Eq. (2.75):

$$\begin{aligned}a_1A(z)+b_1B(z)&=f_1e^{j\beta_1 z}\\ a_2A(z)+b_2B(z)&=f_2e^{j\beta_2 z}.\end{aligned} \tag{2.75}$$

Differentiating with respect to $z$ produces Eq. (2.76):

$$\begin{aligned}a_1\frac{dA}{dz}+b_1\frac{dB}{dz}&=j\beta_1\left(a_1A(z)+b_1B(z)\right)\\ a_2\frac{dA}{dz}+b_2\frac{dB}{dz}&=j\beta_2\left(a_2A(z)+b_2B(z)\right)\end{aligned} \tag{2.76}$$

and solving the system of equations yields the standard coupled mode equations:

$$\begin{aligned}\frac{dA}{dz}&=j\beta_A A+j\kappa_{12}B\\ \frac{dB}{dz}&=j\beta_B B+j\kappa_{21}A\end{aligned} \tag{2.77}$$

where the designations

$$\kappa_{12}\equiv\left(\frac{b_1b_2}{a_1b_2-a_2b_1}\right)\left(\beta_1-\beta_2\right) \tag{2.78}$$

$$\kappa_{21}\equiv\left(\frac{-a_1a_2}{a_1b_2-a_2b_1}\right)\left(\beta_1-\beta_2\right) \tag{2.79}$$

$$\beta_A\equiv\frac{a_1b_2\beta_1-a_2b_1\beta_2}{a_1b_2-a_2b_1} \tag{2.80}$$

$$\beta_A\equiv\frac{a_1b_2\beta_2-a_2b_1\beta_1}{a_1b_2-a_2b_1} \tag{2.81}$$

have been used for simplicity. Eq. (2.77) suggests that for $\kappa_{12} = \kappa_{21} = 0$, $A(z)$ α $\exp(j\beta_A z)$ and $A(z)$ α $\exp(j\beta_B z)$. Thus $\beta_A$ and $\beta_B$ represent propagation constants for the guided modes $\varphi_A$ and $\varphi_B$ associated with waveguides $A$ and $B$ considered in isolation while $\kappa_{12}$ and $\kappa_{21}$ represent the extent to which $\varphi_A$ and $\varphi_B$ perturb each other. It can be shown [130] that $\kappa_{12}$ and $\kappa_{21}$ are proportional to the spatial overlap between $\varphi_A$ and $\varphi_B$.

The general solutions to Eq. (2.77) are given by Eq. (2.82) and Eq. (2.83) [130]:

$$A(z) = \left(c_1 \cos \gamma z + c_2 \sin \gamma z\right) e^{j\left(\frac{\beta_A + \beta_B}{2}\right)z} \tag{2.82}$$

$$B(z) = \frac{1}{\kappa_{12}}\left[\left(-j\gamma c_2 - Dc_1\right)\cos \gamma z - \left(-j\gamma c_1 + Dc_2\right)\sin \gamma z\right] e^{j\left(\frac{\beta_A + \beta_B}{2}\right)z} \tag{2.83}$$

for which $c_1$, $c_2$ are determined by boundary conditions, with

$$D = \frac{1}{2}\left(\beta_A - \beta_B\right) \tag{2.84}$$

and

$$\gamma = \sqrt{D^2 + \kappa_{12}\kappa_{21}}\ . \tag{2.85}$$

## 2.7.2 Power transfer

The initial condition that the field is a scalar multiple of $\psi_A$ produces the boundary condition $B(0) = 0$ in Eq. (2.83), such that the constants $c_1$, $c_2$ are determined according to Eq. (2.86) and Eq. (2.87):

$$c_1 = A(0) \tag{2.86}$$

$$c_2 = j\frac{D}{\gamma}A(0) \tag{2.87}$$

and therefore Eq. (2.82) and Eq. (2.83) produce expressions for the fractional power contained in fields *A*, *B* relative to the incident power according to Eq. (2.88) and Eq. (2.89):

$$\left|\frac{A(z)}{A(0)}\right|^2 = 1 - \left(\frac{\kappa_{12}\kappa_{21}}{\gamma^2}\right)\sin^2 \gamma z \tag{2.88}$$

$$\left|\frac{B(z)}{A(0)}\right|^2 = \left(\frac{\kappa_{12}\kappa_{21}}{\gamma^2}\right)\sin^2 \gamma z . \tag{2.89}$$

It is apparent from Eq. (2.88) that the minimum power associated with waveguide *A* is limited by the ratio $F = (\kappa_{12}\kappa_{21} / \gamma^2)$. For 100% power transfer from *A* to *B*, $D=0$ implies that $\beta_A=\beta_B$, i.e. that the propagation constants associated with the uncoupled waveguides are equal. One solution which satisfies $F=1$ is the case $a_1=a_2$, $b_1=-b_2$, i.e. the compound modes represent even and odd field profiles as illustrated in Fig. 2.11.

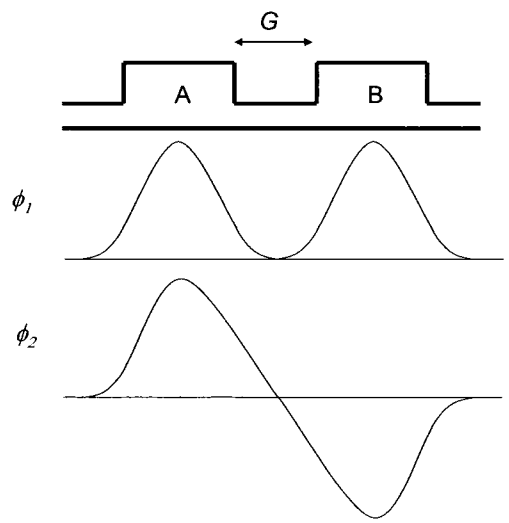


Fig. 2.11: Normal modes $\phi_1$, $\phi_2$ in a typical symmetric compound waveguide structure. The sum $\phi_1 + \phi_2$ corresponds to power localized in waveguide *A* while $\phi_1 - \phi_2$ corresponds to power localized in waveguide *B*.

In the case for a coupler in which the two component waveguides are identical, $\beta_A=\beta_B$ by definition and therefore $F=1$ is satisfied. Furthermore, for $D=0$, Eq.

(2.85) and Eq. (2.88) imply that the propagation length over which power transfer occurs is given by Eq. (2.90):

$$L_c = \frac{\pi}{2\sqrt{\kappa_{12}\kappa_{21}}} \tag{2.90}$$

where $L_c$ is the coupling length. Since $\kappa_{12}$ and $\kappa_{21}$ depend on the spatial overlap between the guided modes of the individual waveguides, Eq. (2.90) suggests that greater overlap between the modes leads to shorter coupling length. In practice this implies that the coupling length can be reduced by (a) reducing the gap $G$ between waveguides, or (b) increasing the evanescent fraction of the mode profile by, for example, reducing the index contrast and/or the rib dimensions relative to the wavelength.

Fig. 2.12 shows a plot of the relative power in waveguides $A$ and $B$ versus propagation length.

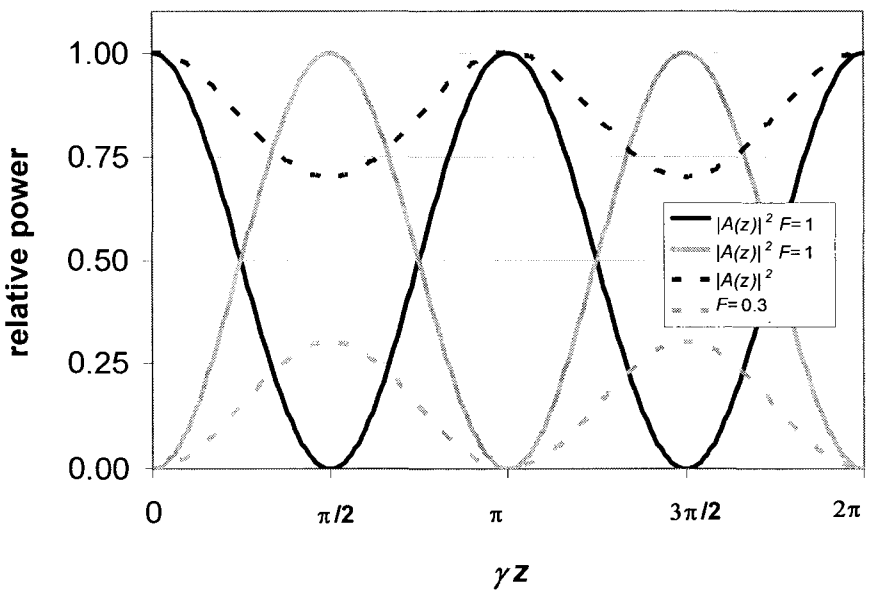


Fig. 2.12: Relative power as a function of propagation length in a directional coupler for $F$=1 (symmetric coupler) and $F$=0.3. Adapted from [129].

For a given waveguide profile and wavelength, the output of a directional coupler therefore depends on the gap $G$ between the individual waveguides and the length of the coupler.

### 2.7.3 Coupler transfer matrix

For a symmetric directional coupler of length $L$ with the initial condition that power is input only to waveguide $A$, Eq. (2.82) and Eq. (2.83) yield expressions for the amplitude of the field in waveguides $A$ and $B$ according to Eq. (2.91) and Eq. (2.92):

$$\frac{A(L)}{A(0)} = \cos\gamma L e^{j\beta L} \tag{2.91}$$

$$\frac{B(L)}{A(0)} = j\sin\gamma L e^{j\beta L}. \tag{2.92}$$

and the relative power coupled to each output is given by Eq. (2.93) and Eq. (2.94):

$$\left|\frac{A(L)}{A(0)}\right|^2 = \cos^2\gamma L \equiv T \tag{2.93}$$

$$\left|\frac{B(L)}{A(0)}\right|^2 = \sin^2\gamma L \equiv K. \tag{2.94}$$

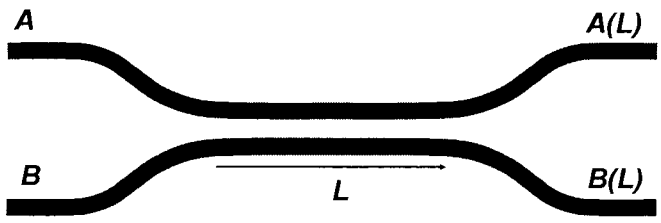


Fig. 2.13: Directional coupler with inputs *A*, *B* and outputs *A(L)*, *B(L)* where *L* is the length of the interaction region between the two waveguides.

Defining $t = (T)^{1/2}$ and $k = (K)^{1/2}$, it is apparent that $A(L)/A(0) = te^{j\beta L}$ and $B(L)/A(0) = jke^{j\beta L}$. Similarly, for power coupled into $B$, $A(L)/B(0) = jke^{j\beta L}$ and $B(L)/B(0) = te^{j\beta L}$. The transfer matrix equation of the coupler is therefore given by Eq. (2.95):

$$\begin{bmatrix} A(L) \\ B(L) \end{bmatrix} = e^{j\beta L} \begin{bmatrix} t & jk \\ jk & t \end{bmatrix} \begin{bmatrix} A(0) \\ B(0) \end{bmatrix}. \tag{2.95}$$

In most cases, the actual phase change incurred by the beam is unimportant or is already accounted for in terms of an overall path length; rather, it is the *relative* phase change difference between output $A(L)$ and output $B(L)$ which is of interest since this can affect the measured intensity in the waveguide if the two outputs are made to interfere with each other. As such, the transfer matrix can be expressed according to Eq. (2.96):

$$\begin{bmatrix} A(L) \\ B(L) \end{bmatrix} = \begin{bmatrix} t & jk \\ jk & t \end{bmatrix} \begin{bmatrix} A(0) \\ B(0) \end{bmatrix}. \tag{2.96}$$

## 2.8 CMOS processing

The prime advantage of silicon photonics is the potential it offers for monolithic integration with electronic devices. As such, the dominant manufacturing processes – i.e. Complementary Metal Oxide Semiconductor - in use throughout the electronics industry are those to which photonic device designs must adhere. A summary of the processes relevant to this work will now be provided.

### 2.8.1 Materials

***Silicon***

Silicon substrates are generally grown using either the Czochralski (Cz) or the Float-Zone (FZ) technique, with Cz prevalent due to the ease with which it can be used to fabricate large-diameter wafers. The Cz method involves melting a silicon "charge" of electronic-grade silicon (EGS) (typically less than $10^{14}$ $cm^{-3}$ impurity density) in a crucible, lowering a seed crystal into the melt, and then drawing it out slowly so as to form a "boule" of crystalline silicon. The FZ process is similar except that no crucible is used; rather a rod of polycrystalline EGS is clamped in contact with a seed crystal and an RF coil is used to melt the rod starting at the seed end and slowly progressing upward so as to form crystalling silicon. Because no crucible is employed, FZ material is of higher purity than CZ particularly with regard to oxygen content. Boules are then diced into wafers and polished to a specified flatness specification.

***Film deposition***

$SiO_2$ (oxide) and $Si_3N_4$ (nitride) films are used for dielectric mask and insulation layers within devices. Films can be deposited via chemical vapour deposition (CVD) in which reactant gases are introduced into a deposition chamber to produce the film, or via physical vapour deposition (PVD) in which the material is vacuum deposited after first being either evaporated or "sputtered" – i.e. bombarded with ions until it vaporizes. Evaporation and sputtering are also used to deposit metallic films (e.g. aluminum, platinum, copper, titanium, and tungsten) for contacts and vias.

Oxide films may also be thermally grown. In this process the silicon is heated to 100 °C or higher and exposed to flowing oxygen (for oxide growth). The oxide thickness can be controlled by the temperature and length of time used for the

growth. The Deal-Grove model [133] provides a means of predicting film thickness according to the growth parameters.

$$x_0 = \frac{A}{2}\left(\sqrt{1+\frac{t+\tau}{A^2/4B}}-1\right) \tag{2.97}$$

where $x_0$ is the film thickness and $A$, $B$ are rate constants determined empirically.

### 2.8.2 Etching

Films can be etched using either chemical ("wet") etchants or reactive ion etching (RIE). The former involves submerging the wafer in an acid or basic solution so as to dissolve exposed material. Silicon can be etched in this manner using a potassium hydroxide solution or a TMAH (tetramethyl ammonium hydroxide) solution. Oxide and nitride films can be etched using buffered hydrofluoric acid (BHF). Chemical etching is generally isotropic for non-crystalline material; for silicon, chemical etching preferentially etches along crystal planes and is therefore useful for producing extremely smooth angled features.

RIE is a technique in which energetic ions are driven toward the wafer so as to vaporize the surface. The ions are chosen so as to combine reactive chemistry with the impact energy for etching. RIE is inherently directional – the preferred etch direction is directly perpendicular to the wafer surface - and is therefore useful for creating vertical features.

### 2.8.3 Lithography

The general lithography process involves applying an easily removable film to a wafer, patterning the film, and then either etching or depositing onto the exposed pattern. Lithography is generally accomplished either by optical exposure (photolithography) or electron beam exposure (e-beam lithography).

***Photolithography***

A photosensitive polymer ("photoresist" or "resist") is spun onto the wafer and baked. Exposure is performed with UV radiation which either causes molecular chains to "cross-link" (negative resist) or to sever (positive resist). A mask is used to shadow parts of the photoresist so as to create a pattern in the film. The coating is then submerged in photoresist developer solution. In the case of negative resist the exposed features remain on the mask; with positive resist only the regions not exposed to UV remain on the wafer after developing. With the pattern imprinted into the photoresist, the underlying material can be etched or a film can be deposited. Once the photoresist is removed from the wafer the patterned film, whether deposited or etched, remains.

The width of the features depends on the "dose": i.e. the brightness and duration of the UV exposure. It is possible to "sweep the dose", i.e. to use a range of optical exposure strength from one side of a wafer to the other. In this manner a single mask can be used to create a range of pattern dimensions when the exact dimensions or process biases are unknown.

***E-beam lithography***

As with photolithography a photoresist is spun onto the wafer and baked, however no mask is employed. Rather the pattern is "written" into the photoresist using a focussed electron beam (e.g. within an electron microscope). E-beam lithography is time consuming and less efficient than photolithography, but can be used to generate finer features that are often difficult or impossible to realize using photolithography.

### 2.8.4 Ion implantation

Ion implantation is used for doping and, as in this work, to produce defects in the bulk material. A schematic of an ion implanter is shown in Fig. 2.14.

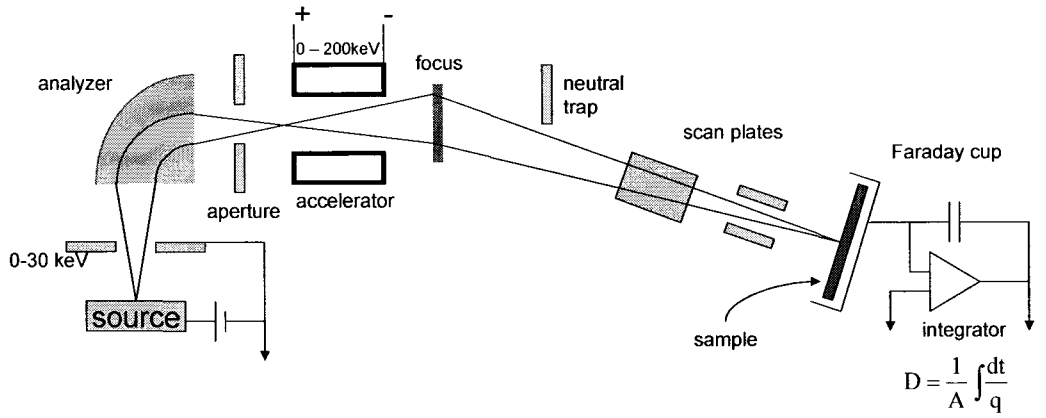


Fig. 2.14: Schematic of an ion implanter. Adapted from [134]

The source (either a vaporized solid source or a gas source) provides the desired ion for the implant. A potential accelerates the ions toward the analyzer magnet, which applies a magnetic field to steer the desired ions into the beam line. Only ions with the desired ratio of mass to charge are selected according to Eq. (2.98):

$$\frac{mv^2}{R} = q\mathbf{v}\times\mathbf{B} \tag{2.98}$$

for radius $R$, magnetic field intensity $B$, ion mass $m$, charge $q$, and velocity $v$. After the analyzer the ions are further accelerated to the desired implantation energy and focused into the target. Scan plates provide an electric field which can be used to raster the beam across the sample. A Faraday cup and an integrator are used to record the beam current, thus providing a measure of the ion dose to which the sample has been subjected.

# Chapter 3

# Defect characterization

An investigation of the defect states responsible for absorption at 1550 nm in ion-implanted photodetectors is presented. The chapter will be divided into five parts: a review of defect characterization with respect to sub-band-gap optical absorption in silicon, a general description of the defect characterization techniques used in this work, fabrication, measurement results, and conversion (by introducing defects into the waveguide) of commercial variable optical attenuators into waveguide photodetectors for optical characterization. Some of the work described in this chapter has been published in [161].

## 3.1 Defects in silicon

### 3.1.1 Known implantation-induced defects

Many of the defects produced by ion implantation or by irradiation of silicon are well-known. Chief among them are the A-centre (oxygen-vacancy complex), the E-centre (phosphorus-vacancy complex) and the divacancy (sometimes referred to

as "E4"). The latter was first shown to be produced by ion implantation (as opposed to irradiation) by Stein *et al.* [135] in 1969 by means of its characteristic optical absorption near 1.8 μm. Energy states attributed to the divacancy included those near -0.4 eV, -0.2 eV, and +0.2 eV (energy states denoted as positive here are with reference to the valence band, while those denoted as negative are listed with reference to the conduction band) as well as a mid-band state near -0.52 eV [107, 136]. More recently only three deep levels are attributed to the divacancy *per se*: $E_c$-0.23 eV, $E_c$-0.4 eV, and $E_v$+0.23 eV [137]. The $E_c$-0.4 eV deep state which will form the central focus of this chapter is generally assigned to the (-/0) transition, the $E_c$-0.23 eV state to the (=/-) transition, and the $E_v$+0.23 eV state to the (0/+) transition [138-140]. Excellent summaries of the various deep levels associated with vacancies and interstitials are provided in [139] and [141].

### 3.1.2 Reported optical absorption near 1.5 μm

The optical absorption of the divacancy was quantified by Cheng and Lori in 1968 [142]; a divacancy concentration per unit peak absorption coefficient of 7.7 × $10^{16}$ $cm^{-2}$ was reported [135] corresponding to a cross-section of 1.3 × $10^{-17}$ $cm^2$. This absorption coefficient together with an equation relating implantation damage density to divacancy concentration has been shown to predict optical loss in ion-implanted silicon waveguides by Foster *et al.* [118]. The equation, developed by Coleman, Burrows, and Knights [143], will henceforth be referred to as the CBK equation. It is noteworthy that although Foster *et al.* observed excellent correlation between the predicted and measured optical absorption, the measured absorption was higher than expected.

### 3.1.3 Mechanism of absorption

The simplest mechanisms envisioned for the absorption process are shown in Fig. 3.1. For a deep level in the lower half of the band gap (i.e. a donor state) a photon excites an electron from the deep level to the conduction band, after which the deep level is refilled via thermal excitation of an electron from the valence band. For a deep level in the upper half of the band gap (i.e. an acceptor state) a photon excites an electron from the valence band to the deep level, after which the electron is thermally emitted to the conduction band.

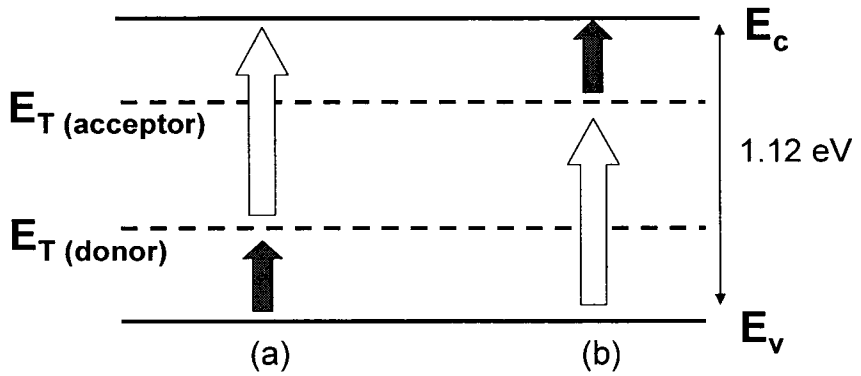


Fig. 3.1: Two different cases of electron transition from the valence to the conduction band mediated by a deep level: (a) optical excitation of an electron from the deep level to the conduction band followed by thermal excitation of an electron from the valence band to deep level, and (b) optical excitation of an electron from the valence band to the deep level followed by thermal excitation of an electron from the deep level to the conduction band. Solid arrows denote thermal transitions while hollow arrows denote optical transitions.

The work described in this chapter strongly supports the argument that the dominant mechanism involved for defect-mediated optical to electrical conversion at wavelengths near 1.55 μm (0.8 eV photon energy) following ion-implantation of silicon is mechanism (b) from Fig. 3.1, and that the dominant deep energy level involved is the $E_c$-0.41 ± 0.03 eV acceptor state commonly attributed to the silicon divacancy.

## 3.2 Standard defect characterization techniques

A brief overview of the standard defect characterization techniques used in this work is provided here. Modified versions of these methods developed as part of this work will be described separately in the experimental results.

### 3.2.1 Capacitance-voltage profiling

As described in Chapter 2, the width of the depletion region in a planar, highly asymmetrically-doped *p-n* junction diode operating according to the depletion approximation is related to the depleted charge density (and hence the doping density) and bias voltage according to Eq. (3.1):

$$V_0 - V_b = \frac{qN_{scr}}{2\varepsilon} w^2 \tag{3.1}$$

where $w$ is the depletion width, $\varepsilon$ is electromagnetic permittivity of the material, $N_{scr}$ is the ionized impurity density within the space-charge region, $V_0$ is the built-in potential and $V_b$ is the bias voltage.

Taking the derivative with respect to voltage and solving for $w$ yields Eq. (3.2):

$$w = \frac{\varepsilon}{qN_{scr}\left(\frac{dw}{d(V_0 - V_b)}\right)} \tag{3.2}$$

and substituting the value for parallel-plate capacitance according to Eq. (3.3):

$$C = \frac{\varepsilon \mathrm{A}}{w} \tag{3.3}$$

yields Eq. (3.4):

$$N(w) = \frac{2}{q\varepsilon A^2 \frac{d\left(1/C^2\right)}{dV}} \tag{3.4}$$

for which *N(w)* can be taken as the doping concentration for diodes in which the ionized trap density is small compared to dopant density, and *A* is device area.

A scan of capacitance versus voltage for a planar diode geometry therefore provides a means of measuring dopant concentration as a function of depletion width, as well as characterizing depletion width versus applied reverse bias.

***Trap compensation***

Since *N(w)* is the charge density, the presence of ionized defects ("traps") within the depletion region can have the effect of either reinforcing or "compensating" – i.e. cancelling out – the charge density from ionized dopant atoms. In such cases *N(w)* is called the "effective concentration" and represents the overall density of all ionized impurities. From Eq. (3.1) and Eq. (3.3) it is apparent that with constant reverse bias, traps which compensate the ionized dopant (e.g. positively charged traps within a *p*-type space-charge region) cause an increase in the space-charge width and hence a decrease in the capacitance of the junction.

For a known dopant density and traps whose ionization state is established, the difference between effective concentration and dopant concentration can be used to calculate the trap density.

***Complications due to traps near the depletion edge***

For cases in which the trap's emission rate is comparable to the frequency of the ac signal used for the capacitance measurement, traps near the depletion width boundary will alternately be filled and emptied by the applied ac voltage. This can lead to additional phase lag between the current and voltage specifically due to the traps rather than due to the parallel plate capacitance. When the trap filling

rate is significantly different from the emptying rate, charge buildup can also occur. Either situation can produce unpredictable capacitance readings. Measurement frequencies of 1 MHz are typical for capacitance meters, and as will be shown in this chapter there are defects introduced by ion implantation that can respond at this frequency at room temperature. Capacitance-voltage measurements for devices with high defect densities, therefore, cannot be trusted. However they provide an excellent means of establishing the "baseline" characteristics of an unimplanted diode.

A good outline of the *C-V* technique is given in [144]; the problems with the technique for abrupt profiles near the depletion edge are discussed in [145].

### 3.2.2 Current-voltage characteristics

A current-voltage characteristic is the *de rigeur* first measurement performed on a diode as a means of establishing whether it is operating correctly (i.e. high current in forward bias and low current in reverse bias). Since reverse leakage current varies with lifetime as described in Chapter 2, an *I-V* characteristic also yields a rough estimate of relative overall defect densities. One expects, for example, that reverse leakage current increases for higher defect density.

### 3.2.3 Thermally stimulated capacitance (TSCAP)

Since the thermal emission rate of a trap increases with temperature as described in Chapter 2, a temperature sweep together with capacitance monitoring can be used to measure defect characteristics. Although this method has been largely supplanted by more sophisticated techniques (e.g. DLTS), it is the basis for a novel technique developed as part of this work and will therefore be described here.

Conventional TSCAP is performed as follows: the sample is cooled to a temperature at which the thermal emission rate of all defects of interest is small relative to the timescale of the measurement. The traps are then filled (e.g. by momentarily reducing the reverse bias or by an optical pulse) and the device is then held under reverse bias such that traps within the depletion width begin to empty. However since the thermal emission rate is very low, emptying of traps is negligible at the starting temperature. The temperature is then ramped while the device is held under reverse bias.

When the thermal ramp reaches a temperature corresponding to a thermal emission rate of 0.1 $s^{-1}$ or less, the traps empty rapidly and the diode capacitance changes abruptly. The height of this capacitance step can be used to calculate the trap density according to Eq. (3.4), the direction of the step reveals whether the defect is acting as a majority or minority carrier trap, and the temperature at which the step occurs yields information on the trap's thermal emission properties [146, 147].

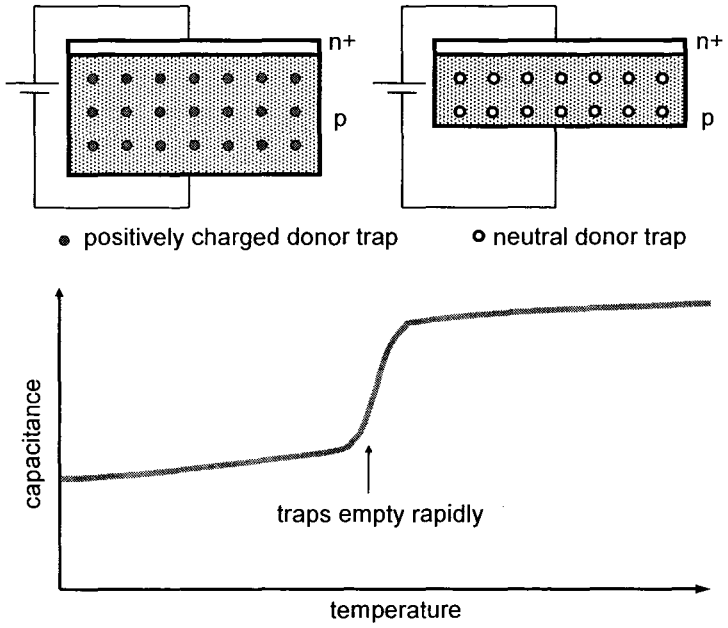


Fig. 3.2: TSCAP trace corresponding to an $n+p$ diode with positively charged (i.e. "filled") compensating donor traps which empty rapidly at a given temperature, thus producing an abrupt upward capacitance step.

### 3.2.4 Capacitance Transient Spectroscopy

Many defect characterization techniques rely on observing the time-dependent recovery of a *p-n* (or Schottky) junction in terms of either capacitance or current after an impulse of voltage, current, or optical radiation. The principles of this approach with respect to capacitance will be outlined here.

***Defect energies and thermal emission rates***

The metric generally pursued in transient measurements for defect characterization is the thermal emission rate of the defect at several temperatures. The correlation between thermal emission rate and defect properties will now be derived.

From Chapter 2 (Eq. (2.14) and Eq. (2.15)) the time constant of thermal emission of electrons to the conduction band from a defect energy state within the band gap is given by Eq. (3.5):

$$\tau_e = \frac{\exp\left(\left(E_c - E_T\right)/kT\right)}{\sigma_n v_{th(electrons)} N_c} \tag{3.5}$$

and for thermal emission of holes to the valence band by Eq. (3.6):

$$\tau_h = \frac{\exp\left(\left(E_T - E_v\right)/kT\right)}{\sigma_p v_{th(holes)} N_v} \tag{3.6}$$

where $E_T$ is the energy of the trap, $E_v$ is the valance band energy, $E_c$ is the conduction band energy, $\sigma_n$ ($\sigma_p$) is the capture cross section of the trap for electrons (holes), $v_{th}$ is the thermal velocity, $T$ is temperature, and $N_c$ ($N_v$) is the density of states in the conduction (valence) band.

Recalling the expressions for the density of states:

$$N_c = 2\left(\frac{2\pi m_n kT}{h^2}\right)^{3/2}, \quad N_v = 2\left(\frac{2\pi m_h kT}{h^2}\right)^{3/2} \tag{3.7}$$

and thermal velocity:

$$v_{th(electrons)} = \sqrt{\frac{3kT}{m_n}}, \quad v_{th(holes)} = \sqrt{\frac{3kT}{m_p}} \tag{3.8}$$

and substituting these into Eq. (3.6) yields Eq. (3.9):

$$\tau_e T^2 = \frac{\exp\left(\left(E_c - E_T\right)/kT\right)}{\gamma_n \sigma_n}, \quad \tau_h T^2 = \frac{\exp\left(\left(E_T - E_v\right)/kT\right)}{\gamma_p \sigma_p} \tag{3.9}$$

where

$$\gamma_n = \frac{v_{th(electrons)} N_c}{T^2}, \quad \gamma_p = \frac{v_{th(holes)} N_v}{T^2}. \tag{3.10}$$

An Arrhenius plot of the natural logarithm of $\tau_e T^2$ for various $\tau_e$ (i.e. the reciprocal of the thermal emission rate constant) versus $(1/kT)$ will therefore have a slope representing the energy difference between the trap state and the band to which it emits, and an intercept from which the electrical capture cross-section can be estimated.

Hence a measurement of the thermal emission rate of a defect at several temperatures provides an estimate of the defect's energy and cross-section.

***Entropy effects***

The thermal energy associated with trap emission to a band is in fact the change in Gibbs free energy, defined by Eq. (3.11):

$$\Delta G = \Delta H - T\Delta S \tag{3.11}$$

where $\Delta G$, $\Delta H$, and $\Delta S$ are the Gibbs free energy, enthalpy, and entropy changes respectively associated with the transition, and $T$ is the temperature. Substituting $\Delta G$ from Eq. (3.11) into Eq. (3.5) and Eq. (3.6) and proceeding with the derivation to Eq. (3.9), it becomes apparent that there will be an extra entropy term which contributes to the intercept on the Arrhenius plot, and further that the slope represents the enthalpy difference $\Delta H$ rather than energy difference $\Delta G$.

This complication is often ignored in published literature concerning the characterization of defect states. In this work the Arrhenius plots are assumed to give reasonable estimates of defect energies and an effort is made to check this assumption by extending the measurement to lower temperatures (i.e. longer emission time constants) where the difference between $\Delta H$ and $\Delta G$ decreases according to Eq. (3.11).

***Determining thermal emission rates from capacitance transients***

Returning to the relation between depletion width and bias voltage in Eq. (3.1), and substituting the expression for parallel-plate capacitance in Eq. (3.3) produces an expression for the capacitance as a function of bias voltage for an asymmetric diode under the depletion approximation as shown in Eq. (3.12):

$$C = A\left(\frac{q\varepsilon N_{scr}}{2(V_0 - V_b)}\right)^{1/2} \tag{3.12}$$

where $A$ is the junction area, $\varepsilon$ is the material permittivity, $N_{scr}$ is the density of ionized impurities in the space-charge region, $V_0$ is the built-in potential of the diode, $V_b$ is the applied bias voltage, and $q$ is the charge of an electron.

Traps in the space-charge region that are not at thermal equilibrium will release charge according to a thermal emission time constant as described in Chapter 2, leading to a time-dependent ionized impurity density $N_{scr} = N_d - n_T(t)$ where $N_d$ is the dopant density and $n_T$ is the ionized majority-carrier trap density. Time-dependence of $N_{scr}$ leads to a time-dependent junction depletion width according to Eq. (3.2), and thus a time-dependent capacitance according to Eq. (3.3), and the expression in Eq. (3.12) reduces to Eq. (3.13):

$$C = A\left(\frac{q\varepsilon}{2(V_0 - V_b)}\left(N_d - n_T(t)\right)\right)^{1/2} \tag{3.13}$$

or

$$C = C_0\left(1-\frac{n_T(t)}{N_d}\right)^{1/2} \tag{3.14}$$

where

$$C_0 = A\left(\frac{q\varepsilon N_d}{2(V_0 - V_b)}\right)^{1/2} \tag{3.15}$$

is equivalent to the capacitance of a diode with no traps.

For minority-carrier traps Eq. (3.14) becomes Eq. (3.16):

$$C = C_0\left(1+\frac{n_T(t)}{N_d}\right)^{1/2} \tag{3.16}$$

since the ionized traps contribute to the net charge density in the space-charge region rather than compensating it.

***Small trap-density approximation***

For the case in which $n_T(t) << N_d$ (i.e. very small electrically active trap density compared to dopant density), a first-order Taylor expansion of Eq. (3.14) yields Eq. (3.17):

$$C \approx C_0\left(1-\frac{n_T(t)}{2N_d}\right). \tag{3.17}$$

Substituting the expression for thermal emission of charge from traps which interact primarily with one band as derived in Chapter 2, one obtains Eq. (3.18):

$$C \approx C_0\left(1-\frac{n_T(0)}{2N_d}\exp\left(-\frac{t}{\tau}\right)\right) \tag{3.18}$$

where $\tau$ is the thermal emission time constant of the trap. The time constant of the capacitance transient, therefore, yields the thermal emission time constant of the trap.

It should be noted that the approximation listed here is valid when trap density is small compared to dopant density, but can also be valid when trap density is large provided that only a small fraction of the traps are made to fill and empty in a time-dependent manner.

***Constant-capacitance transients***

For cases in which the electrically active trap density is comparable to dopant density, Eq. (3.14) must be used, thus precluding a simple exponential relationship between capacitance and trap emission rate. Furthermore, variations in capacitance can lead to second-order effects as the space-charge region expands in response to thermal emission from traps within the depletion width, overtakes traps that were previously outside the space-charge region, and causes their occupancy to change as well. Both of these considerations greatly complicate the analysis of transients.

A simpler approach for large trap densities is the "constant-capacitance transient" method, in which a feedback loop between the capacitance meter and the voltage supply adjusts and records bias voltage so as to maintain constant capacitance while traps undergo thermal emission.

Returning to Eq. (3.13) and solving for $V_b$ yields Eq. (3.19):

$$V_b = V_0 - \frac{q\varepsilon A^2 N_d}{2C^2} + \frac{q\varepsilon A^2}{2C^2} n_T(t) \tag{3.19}$$

and including the time dependence of $n_T(t)$,

$$V_b = V_0 - \frac{q\varepsilon A^2 N_d}{2C^2} + \frac{q\varepsilon A^2}{2C^2} n_T(0) \exp\left(-\frac{t}{\tau}\right). \tag{3.20}$$

By recording the fluctuation in bias voltage required to maintain constant capacitance, the time constant of the trap emission and the average trap density within the space-charge region can be ascertained.

Traps must initially be filled so that the capacitance transient associated with thermal emission within the space-charge region can be observed and sampled. This can be accomplished in several ways, three of which will now be summarized.

***Trap filling via neutral bias***

The steady-state trap occupancy (i.e. the fraction of traps which contain negative charge) was derived in Chapter 2 and is given by Eq. (3.21):

$$\frac{n_T}{N_T} = \frac{p_1 c_p + c_n n}{c_n (n_1 + n) + c_p (p_1 + p)} \tag{3.21}$$

where $n_T$ is the density of traps occupied by electrons, $N_T$ is the trap density, $c_p$ and $c_n$ are the trap capture rate for holes and electrons respectively, $n$ and $p$ are the densities of electrons in the conduction band and holes in the valence band respectively, and $n_1$ and $p_1$ are the conduction band electron density and valence band hole density when the Fermi level coincides with the trap energy.

Considering the region beyond the depletion width of a $p^+n$ junction on the $n$-type side, $p$, $n_1$, and $p_1$ are very small compared to $n$, so for $c_n$ and $c_p$ relatively similar (as compared to $n$ and $p$) it is clear from Eq. (3.21) that the trap occupancy approaches unity.

Within the space-charge region, however, $n$ and $p$ are both zero by the depletion approximation. For traps in the upper half of the band gap (such that $n_1 >> p_1$) the trap occupancy reduces to approximately zero, whereas for traps in the lower half of the band gap (such that $n_1 << p_1$) the trap occupancy approaches unity.

Thus, upper-half-band traps within the space-charge region of a $p^+n$ diode emit majority carriers until their occupancy is zero, whereas outside the space-charge region they fill with majority carriers until their occupancy is unity, whereas lower-half-band traps remain filled with majority carriers regardless of whether

they are inside or outside the space-charge region. The band diagrams for a $p^+n$ junction with upper-half-band traps are shown at two reverse biases in Fig. 3.3.

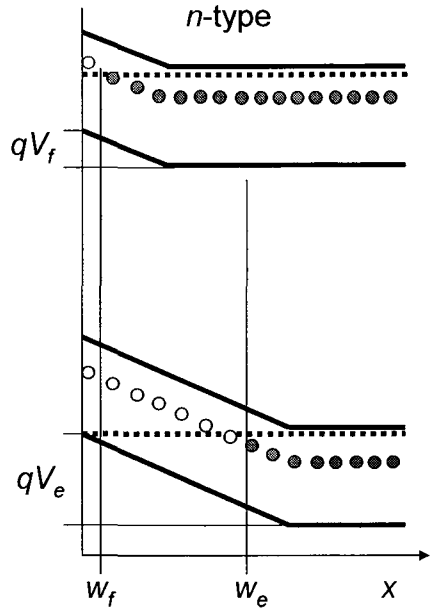


Fig. 3.3: Band diagram of a $p^+n$ diode (n-type region only) showing band bending at two applied biases: $V_f$ (top) and $V_e$ (bottom). The dotted line represents the Fermi level; the circles represent acceptor traps in the upper half of the band gap, with filled circles representing filled (i.e. negatively charged) traps and empty circles representing empty (i.e. neutral) traps. At $V_e$ , traps empty for $x<w_e$, whereas at $V_f$ traps fill for $w_f<x<w_e$.

Similar considerations for the case of an $n^+p$ junction lead to the result that lower-half-band traps within the space-charge region emit majority carriers (holes) whereas outside the space-charge region they fill with majority carriers; upper-half-band traps are empty of electrons regardless of whether they are inside or outside the space-charge region.

Thus, majority carrier traps (i.e. traps whose energy level resides in the same half of the band gap as the Fermi level in the quasi-neutral region) fill when they are outside the space-charge region and empty when they are inside it, while minority carrier traps are empty (of minority carriers) regardless of their location.

Since reducing the applied reverse bias reduces the depletion width of the junction according to Eq. (3.1), majority carrier traps that had been inside the space-charge

region (i.e. $w_f < x < w_e$ in Fig. 3.3) fill with majority carriers during a reduced voltage pulse.

***Trap filling via forward bias***

Under forward bias, minority carriers are injected into the junction. Taking $n \approx p$ and assuming a minority carrier trap, trap occupancy according to Eq. (3.21) will be non-zero. Thus minority carrier traps can be at least partially filled by means of minority carrier injection via a forward bias pulse. Since majority carriers are also present, both minority and majority traps can fill depending on their distance from the junction and the forward injection current density. The actual occupancy of either kind of trap is difficult to predict, but for measurements of the emission rate (as opposed to concentration) the occupancy need not be known, and so forward bias pulses can be useful to observe traps which would otherwise be difficult to detect.

***Trap filling via optical excitation***

Illumination at wavelengths corresponding to photon energies that exceed the band gap can be used to generate electron-hole pairs and thus inject minority charge carriers into the junction. This approach injects only minority carriers and can therefore be used to selectively fill minority carrier traps without filling majority carrier traps.

Optical illumination at sub-band-gap photon energies can be used if the traps are optically active (i.e. if incident photons can excite carriers from the traps to either band). This approach will be discussed in greater detail in the latter part of the chapter.

***Majority versus minority carrier trap filling***

The analysis of results for minority carrier injection via forward bias is considerably more difficult than for majority carrier injection. Under forward bias both minority and majority carriers are available for trap filling in relative

proportions which depend on location and current density, thus making a determination of the trap occupancy inherently difficult.

Minority carrier injection by optical exposure requires either transparent contacts or unusual contact geometries and a means of illuminating the sample while it is sealed in a vacuum chamber. There are also inherent difficulties associated with calculating the intensity of the radiation incident on the junction due to interference effects and the non-uniformity of the beam profile.

For these reasons majority-carrier trap characterization is much more common than minority-carrier trap characterization in the literature. This is problematic, however, since defect characteristics can be affected by the dopant. It is well known, for example, that vacancies can form the "*E*-centre" (i.e. phosphorus-vacancy complex) in *n*-type silicon, whereas no such defect can exist in *p*-type silicon. Conclusions drawn with respect to vacancy-related defect concentrations in *p*-type silicon that rely on trap concentration measurements in *n*-type silicon should therefore be treated with a measure of caution.

### 3.2.5 Deep Level Transient Spectroscopy

An adaptation of capacitance transient spectroscopy which takes advantage of filtering and averaging techniques to reduce noise in the measurement was introduced by Lang in 1974 [148, 149] and together with its various refinements quickly became a standard approach for defect characterization. This technique is called Deep Level Transient Spectroscopy (DLTS) and will be summarized here.

***Correlation filtering of the transient signal***

A filtering function may be applied to the transient in order to extract a signal which corresponds to the time constant. The signal derived from an arbitrary filtering function *f(t)* applied to transient *h(t)* together with averaging over interval *T* is given by Eq. (3.22):

$$\partial h = \frac{1}{T}\int_0^T h(t)f(t)dt\,. \tag{3.22}$$

One of the simplest filter functions (and the one originally used by Lang) is the "boxcar", or sampling the transient at two timepoints and subtracting the values. Boxcar filtering corresponds to a filter function $f(t) = \delta(t-t_2) - \delta(t-t_1)$.

Substituting the capacitance transient of Eq. (3.18) for $h(t)$ and applying a boxcar filter for $f(t)$ over pulse period $T_p$ yields the expression for a boxcar DLTS signal in Eq. (3.23):

$$\partial C = C_0\int_0^{T_p}\left[\left(1-\frac{n_T(0)}{2N_d}\exp(-\frac{t}{\tau})\right)\left(\delta(t-t_2)-\delta(t-t_1)\right)\right]dt = C(t_2)-C(t_1)\,. \tag{3.23}$$

Differentiation $\delta C$ with respect to $\tau$ and solving for the time constant corresponding to the DLTS peak signal produces Eq. (3.24):

$$\tau_{\max} = \frac{t_2 - t_1}{\ln(t_2/t_1)}\,. \tag{3.24}$$

Thus, rather than recording a series of capacitance transients, fitting each one to an exponential, and extracting a time constant, one can instead sample the difference between two points on the transient either for a set of time constants or a set of timepoints, find the member of the set with the highest signal, and calculate the time constant of the transient which corresponds to the timepoints according to Eq. (3.24). This approach has several benefits:

(1) easy automation either via electronics or software since no curve fitting is required,

(2) the timescale $T$ can be shorter than that required to determine the vertical offset of the transient since $\delta C$ eliminates this constant contribution, and

(3) only two points from the transient need be sampled rather than discretizing and storing the entire function.

### *DLTS signal*

In practice, DLTS is most often applied by sampling and averaging the signal $\delta C$ for a large number of transients (this is made feasible due to the second advantage listed above) while subjecting the device to a thermal ramp such that the emission rates of the traps within the space-charge region steadily increase. At a temperature for which the thermal emission rate of a given trap matches the boxcar filter according to Eq. (3.24) the DLTS signal reaches a peak. The overall thermal scan therefore exhibits a signal peak corresponding to each defect. By sampling the DLTS signal corresponding to several pairs of timepoints on the transient (i.e. applying several boxcar filters), several peaks can be extracted for each defect – each at a temperature for which the emission rate corresponds to the filter time constant.

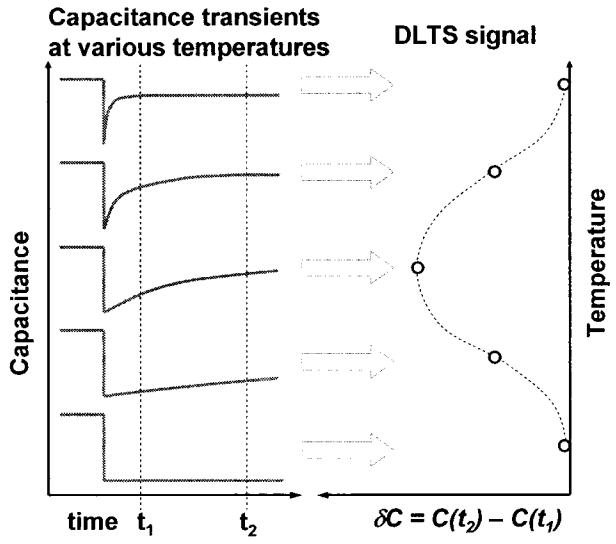


Fig. 3.4: Boxcar DLTS signal corresponding to capacitance transients at a range of temperatures showing the peak DLTS signal at the temperature for which the transient has a time constant corresponding to the time difference between the filter timepoints.

The boxcar filter approach for transients ranging from long time constant (i.e. low temperature) to short time constant (i.e. high temperature) is illustrated in Fig. 3.4.

***Summary of DLTS technique***

The DLTS technique may be summarized as follows:

(1) The sample is cooled to a low temperature. The extent of the cooling is dictated by the emission rate of the trap being characterized: traps with high emission rates may require cooling to very low temperatures before their rate constant is low enough to be measurable by the system. Since the trap emission rate depends largely on the difference in energy between the trap and the band edge, there is a trade-off between the minimum "depth" of traps within the band gap that the system can detect, the minimum temperature to which the system can cool the sample, and the maximum rate constant that the system can measure.

(2) Traps near the junction are filled using either a reduced reverse bias voltage pulse (majority carrier traps), a forward bias pulse (both majority and minority carrier traps), or an optical pulse (minority carrier traps). The length of the filling pulse can be used to determine the fraction of traps that are filled. Filling majority carrier traps causes the capacitance to decrease since they then compensate the ionized dopant impurities (thus reducing the effective charge density as described in section 3.2.1, while filling minority carrier traps causes the capacitance to increase.

(3) Reverse bias is applied to the junction, causing traps to empty at characteristic emission rates which depend on temperature. As they empty, capacitance either increases (majority carrier traps) or decreases (minority carrier traps). The transient is sampled and filtered for a particular emission rate.

(4) The filling and emptying pulses are repeated so that the DLTS signal collected can be averaged for higher signal-to-noise ratio.

(5) Temperature is increased in order to sample a transient with higher trap emission rates.

The technique is illustrated as a flowchart in Fig. 3.5.

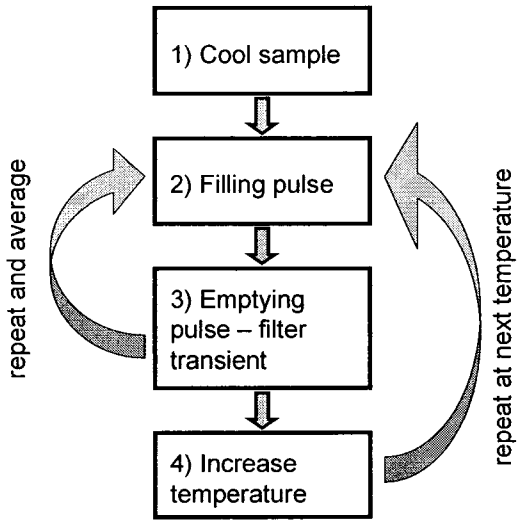


Fig. 3.5: Flow-chart of DLTS technique.

The changes in capacitance with reference to the band diagrams at each bias voltage during a typical DLTS cycle (steady state, filling pulse, emptying transient) are shown in Fig. 3.6.

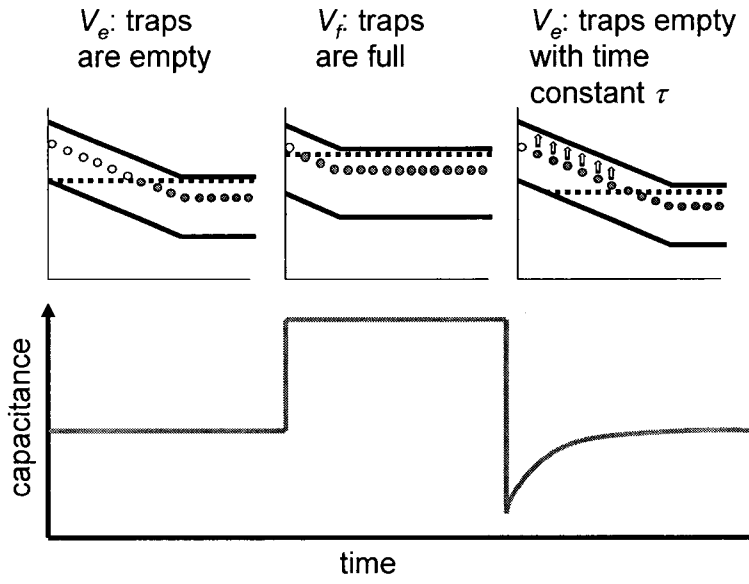


Fig. 3.6: Capacitance and band diagrams during a typical DLTS cycle: steady state with empty traps (left), fill pulse (centre), and transient (right) for a $p^+n$ diode with majority carrier traps.

# 3.3 Device fabrication

## 3.3.1 Starting wafers and preparation

The devices used for defect characterization were fabricated at the Centre for Emerging Device Technologies, McMaster University, as part of this work.

Characterizing defects in epitaxial silicon rather than Czochralski silicon was deemed to be desirable in order to match the defect characteristics as closely as possible to those of the epitaxially-grown thick SOI used for most silicon photonic waveguide devices. For this purpose two single-side polished Czochralski 4-inch <100> silicon wafers (nominal $1\times10^{15}$ $cm^{-3}$ *p*-type doping) with a 4 ± 0.03 μm dopant-matched silicon film epitaxially grown on their top surface were obtained from Lawrence Semiconductor Inc. The film resistivity was measured by the vendor and found to be 9 ± 1 Ωcm, which corresponds to *p*-type doping concentration of $1.5 \pm 0.2 \times10^{15}$ $cm^{-3}$.

The wafers were oxidized by annealing in a Jipelec JetFirst rapid thermal annealer at 1100 °C for 30 minutes in flowing dry oxygen. The oxide film thickness was measured to be 90 ± 10 nm using a surface profilometer.

## 3.3.2 Junction definition and $N^+$ doping

The wafers were cleaved into 1.25 inch squares and open circles of 2 mm diameter were defined by photolithography using Shipley 1827 photoresist. The photoresist was hard-baked and retained on the samples so as to act as an implantation mask. Profilometry confirmed that the photoresist thickness was 4 ± 0.5 μm using the recipe included in Appendix A.

Phosphorus dopant was implanted with 100 keV energy to a dose of $6\times10^{14}$ $cm^{-2}$ at the Tandetron Accelerator, University of Western Ontario. The dose was selected to yield a concentration of at least $1\times10^{19}$ $cm^{-3}$ *n*-type activated dopant after implantation and annealing assuming a junction depth of less than 1 μm.

The exposed oxide was etched for two minutes in buffered hydrofluoric acid (BHF). The windows opened in the oxide film thus provided a self-aligned feature which demarked the positions of the doped regions. The samples were then cleaned using 20 minutes ultrasonic agitation in acetone, isopropyl alcohol, and deionized water followed by a 10 minute "piranha" etch ($H_2SO_4$ / $H_2O_2$ mixture at 1:5 volume ratio) at 140 °C. This step was found necessary to completely remove the photoresist mask after the dopant implantation.

The dopant was activated by annealing at 1200 °C for 3 seconds and then 1000 °C for 10 minutes in flowing nitrogen using the Jipelec rapid thermal annealer. The dopant profiles corresponding to this fabrication process were simulated using the Silvaco Athena software package; the concentrations of activated phosphorus and boron as a function of depth indicate that the depth of the junction was 0.7 μm below the silicon surface. These profiles are shown in Fig. 3.7.

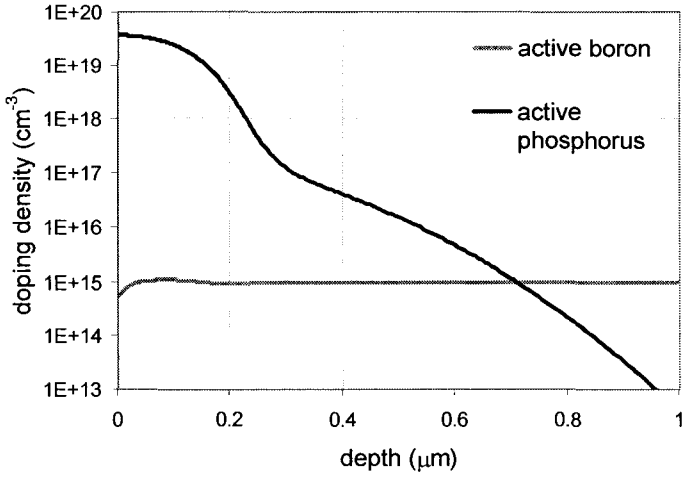


Fig. 3.7: Dopant concentrations simulated by Silvaco Athena for the implantation and annealing steps used in this work.

### 3.3.3 Ion implantation

Defects were introduced into the sample at room temperature via $Si^{3+}$ or $B^{+}$ ion implantation at 7 degrees tilt so as to avoid channelling. The silicon ion implantation energy was 4 MeV energy with a dose of $5\times10^{10}$ $cm^{-2}$; the boron implantation energy was 350 keV with a dose of $1\times10^{13}$ $cm^{-2}$. No implantation mask was used for this step.

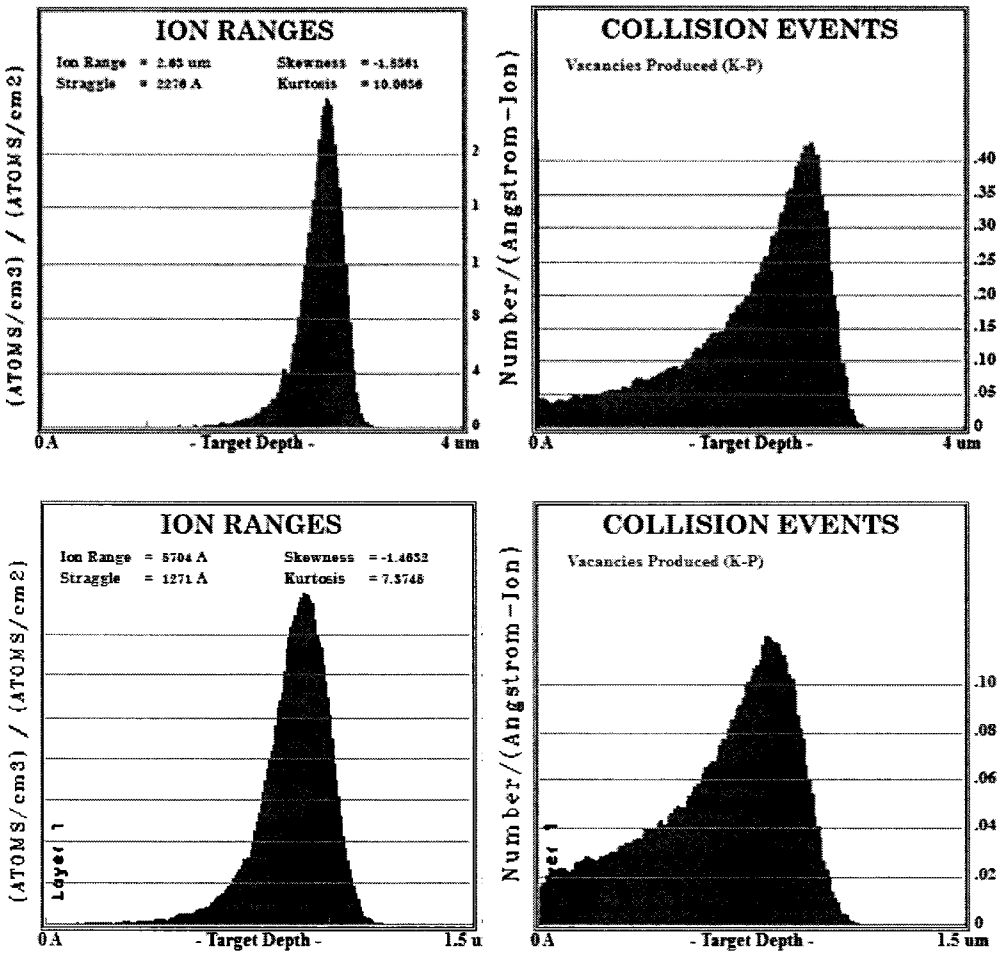


Fig. 3.8: SRIM simulations [150] of ion range (left column) and damage profile (right column) for 4 MeV silicon ion implantation (top row) and 350 keV boron ion implantation (bottom row) in silicon at 7 degrees tilt.

The energy of the implantation step determined the ion range, i.e. the depth to which ions penetrate the silicon substrate before stopping. For majority-carrier

defect detection using Capacitance Transient Spectroscopy and DLTS, one must be able to reduce the depletion width of the diode such that the defects are not contained within it, as explained in section 3.2.4. However, there is a minimum depletion width at neutral bias determined by the effective dopant density; introducing defects which compensate the dopant reduces the effective dopant density. Accordingly, to ensure that majority-carrier traps could be filled using neutral bias pulses, it was important that the range of the ion implantation be larger than the minimum depletion width. Excessive implantation energy, however, can introduce enough damage that characterization of specific defects becomes very difficult. Monte Carlo SRIM simulations [150] indicated that silicon implantation with an energy of 4 MeV produces a silicon ion range of 2.6 μm with most damage occurring between 2 μm and 3 μm while boron implantation with an energy of 350 keV produces a boron ion range of 0.87 μm with most damage occurring between 0 and 1.2 μm. These simulations are shown in Fig. 3.8.

The boron implantation at 350 keV was chosen to characterize the defects implanted for the devices described in chapters 4 and 5. These implantation parameters are more easily implemented in an industrial setting than those described above since high-energy implantation (i.e. energy greater than several hundred keV), and implantations using species other than boron and phosphorus are often not available within a standard semiconductor foundry. From Fig. 3.8 it is apparent that the peak damage density due to boron ion implantation at 350 keV is reduced compared to silicon ion implantation at 4 MeV by a factor of four. Taking into account the relative doses of the two implantations ($1\times10^{13}$ $cm^{-2}$ for the boron implantation versus $5\times10^{10}$ $cm^{-2}$ for the silicon implantation) one can estimate that the peak damage density for the boron-implanted devices will be higher by a factor of 50. The silicon-implanted devices will henceforth be referred to as the "E-Sil" samples and the boron-implanted devices as the "E-Bor" samples.

### 3.3.4 Dicing and defect annealing

The 1.25 inch tiles were diced into 1 $cm^2$ chips using a LoadPoint MicroAce dicing saw, with each chip containing sixteen 2 mm diodes. The E-Sil samples were then separately annealed in the Jipelec for 10 minutes at temperatures from 200 °C to 400 °C at 50 °C increments in order to gather data on the effect of annealing parameters on defect concentrations. No defect annealing step was performed on the E-Bor samples.

All samples were subjected to a 10 minute cleaning step (acetone, IPA, deionized water, nitrogen drying and annealing on a hot plate set to 150 °C) following dicing. Unannealed samples are therefore treated for the remainder of this work as having been annealed at 150 °C.

### 3.3.5 Metal contacts

With the previously etched oxide features as a guide, 1 mm diameter circles aligned approximately to the centre of the doped regions were defined using NR9 negative photoresist. The use of negative photoresist in this instance allows the mask to be light-field rather than dark-field so that the 2 mm diameter diodes can be viewed clearly through the mask while aligning the 1 mm diameter contact features.

After cleaning and a 5 second BHF dip to remove native oxide, aluminum was thermally evaporated onto the samples to a thickness of 250 nm and the metal contacts were then defined by a lift-off in acetone and 10 minute agitation in an ultrasonic bath.

Backside contacts were fabricated by sputtering gold to a thickness of 150 nm and then subjecting the samples to 120 °C on a hot plate for several minutes. Immediately prior to gold deposition, the backside surface was scribed to ensure

direct contact between the gold and the silicon and to damage the surface in order to reduce the possibility of forming a Schottky barrier.

### 3.3.6 Bond pads

Electrical characterization of the samples required that they be easily contacted on both sides, electrically isolated from the test fixture, and in good thermal contact with the temperature controller. Several approaches were tried, including bonding the samples to metal-coated pieces of glass (not sufficiently thermally conductive), slabs of silicon (parasitic capacitance and surface trapping effects became a concern), rolled brass (not flat enough to achieve good thermal contact), and 1 $cm^2$ tiles of copper plate. The copper plate together with thermally conductive paste to provide electrical insulation from the fixture seemed like a successful combination until samples were lowered below 150 K, at which point the disparate thermal expansion coefficients of the silicon and the copper caused the samples to explode spontaneously inside the vacuum chamber, much to the consternation of all involved.

Ultimately, thermally conductive gold-plated alumina ceramic bond pads were purchased from Coorstek; the samples were bonded to these using silver paint. Once mounted to the bond pads the samples were found to be in sufficiently good thermal contact with the temperature controller that thermal ramps of 1 K/min, 3 K/min, and 4.8 K/min produced no discernible change in measurements. Thermal ramps of 6 K/min were found to produce slight hysteresis so thermal characterization was performed with ramp rates of 4.8 K/min for most measurements.

A diagram of the fabrication process is shown in Fig. 3.9.

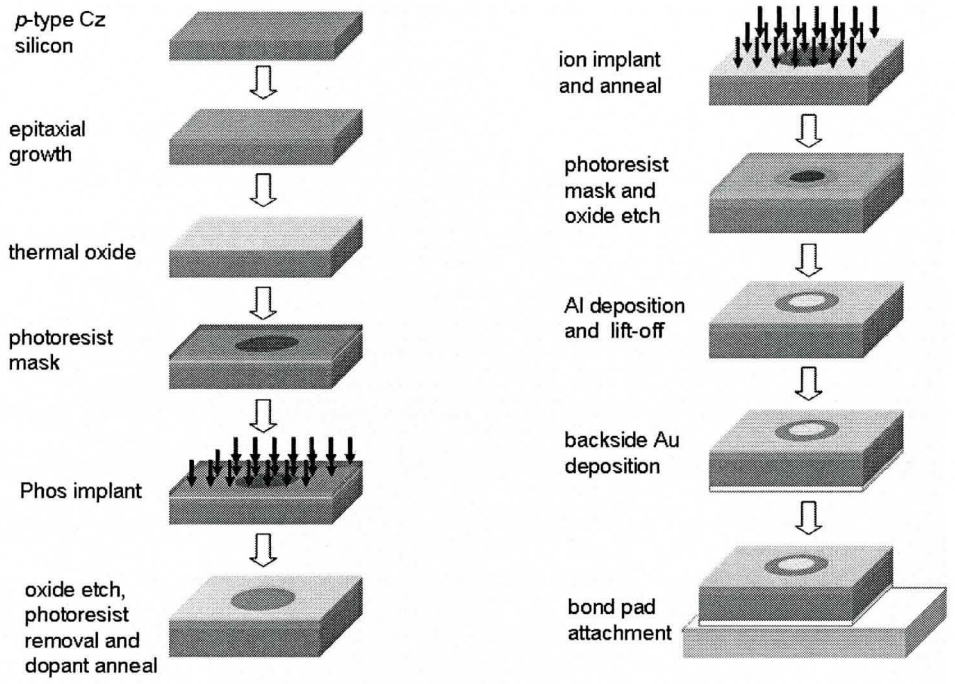


Fig. 3.9: Fabrication process for $n^+p$ junctions used to characterize optically active defects.

### 3.3.7 Fabrication issues

Fabrication of the devices was initially attempted with Czochralski-grown bulk silicon to test the process before consuming the more expensive, and consequently scarce, epitaxially-grown wafers. This led to several process refinements such as (1) the incorporation of negative resist and a light-field mask at the contact definition step, (2) gold backside contacts rather than sintered aluminum so that defect annealing could be accomplished before metal deposition, thus making arbitrary defect anneals possible without introducing the possibility of metal diffusion into the junction, and (3) the aforementioned adoption of ceramic bond pads. Even without these refinements, however, the Czochralski devices were considered satisfactory as $n^+p$ junctions, with unimplanted test diodes having leakage current densities consistently less than $2\times10^{-6}$ A/cm$^2$ at 20 V reverse bias and forward current densities consistently greater than $7\times10^{-3}$ A/cm$^2$ at 1 V forward bias.

Upon repeating the same process (with minor refinements) using wafers with epitaxially-grown silicon films six months later, junction quality was found to be considerably worse with leakage current densities two orders of magnitude higher and unaccounted for peaks appearing in the DLTS spectra. Solving this problem became a long exercise in the process of elimination - unsuccessful attempts to isolate the cause included repeating the fabrication with the original process and wafers, a tube furnace, a different ion implanter, and a different mask set.

Ultimately a methodical reconsideration of every change to the equipment in the intervening six months led to the recollection that the original process had involved a 10 second thermal ramp directly to 1000 °C in the Jipelec during the dopant activation anneal. Subsequent fabrication runs had incorporated a more cautious approach in which the Jipelec was programmed to ramp slowly between 400 °C and 500 °C before ramping to 1000 °C in order to allow the on-board pyrometer sufficient time to begin accurately controlling temperature (this procedure was implemented as a matter of policy after a student's wafer dramatically shattered during annealing because the pyrometer readings were erroneously low while the annealer was ramping to full power). An examination of the Jipelec's recorded data files showed that in the original process the temperature had in fact tended to oscillate past 1200 °C for a brief period (2 seconds to 5 seconds) at the beginning of the original process thermal ramp (in fact it had been noticed after the original process that one sample emerged from dopant activation with partially molten features).

The fabrication was repeated with a deliberately introduced 3-second thermal spike to 1200 °C after the procedurally required slow thermal ramp. Low leakage currents were once again observed with this addition to the process, while samples processed in parallel without the added thermal spike showed high leakage currents. Accordingly, the new thermal recipe was incorporated into the process and the remaining epitaxially-grown samples were successfully processed.

# 3.4 Results

Standard techniques were used initially to show that the dominant optically active defect (at 1550 nm wavelength) in the samples has characteristics consistent with an acceptor state attributed to the divacancy. Further experiments and a novel characterization technique were developed and used to test predictions based on this understanding. The results and conclusions from the standard techniques (*C-V* profiles, *J-V* profiles, conventional DLTS, and optical DLTS) will first be described followed by a discussion of the reasoning and experimental approach used to test those conclusions. A new technique for the characterization of optically active defects (Equilibrium Capacitance Spectroscopy) will be described and the results with respect to measurements of the optical cross-section and concentration profiles will be provided. Finally, the characteristics of waveguide-based photodetectors fabricated from industrial devices will be assessed according to the information gleaned from the prior defect characterization work.

## 3.4.1 Current-voltage measurements

Current versus bias voltage in darkness at 300 K was measured. The *J-V* characteristic curves for a range of anneal temperatures are shown in Fig. 3.10. It is noteworthy that the leakage current at high reverse bias increases drastically with ion implantation and then decreases uniformly with anneal temperature, indicating that defects reduce the carrier lifetime and are removed from the sample during annealing as expected.

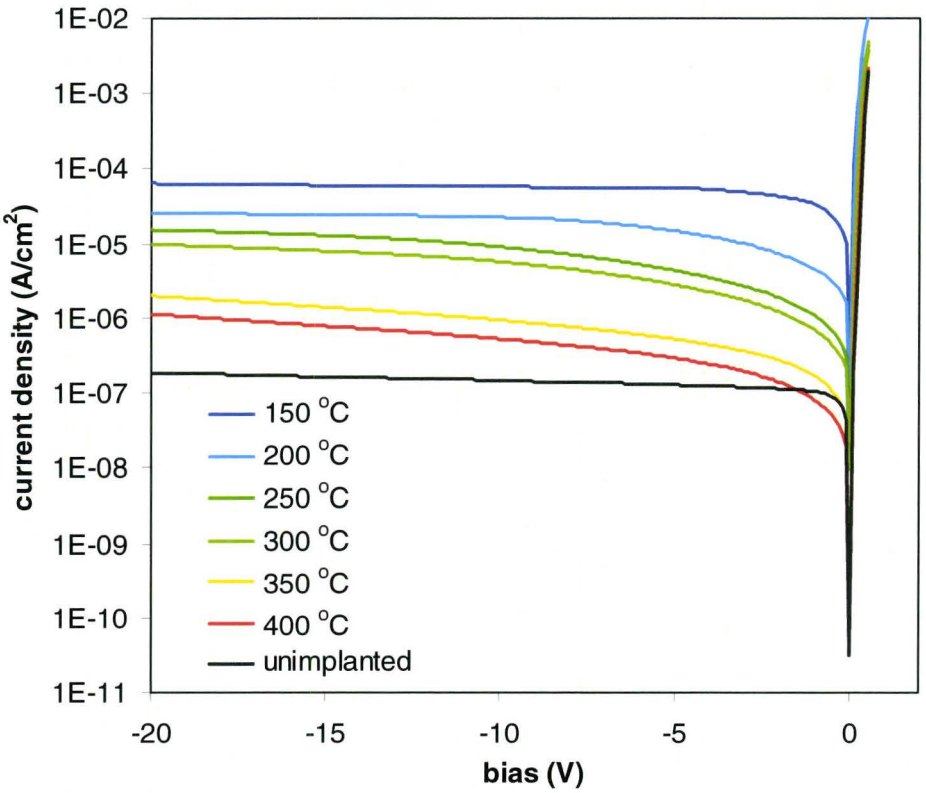


Fig. 3.10: Measured current density versus bias voltage for the E-Sil diodes for isochronal 10 minute anneals at temperatures from 120 °C to 400 °C. Also shown for comparison is the characteristic for the unimplanted diode.

The reverse leakage current of the diode includes both a diffusion component in the quasi-neutral region and a generation component in the space-charge region. For high trap concentration within the space-charge region (i.e. a depletion width that is significantly larger than the range of ion implantation damage for the devices described here), the generation component should dominate the diffusion component and hence leakage current is described by Eq. (3.25):

$$J_{leakage} \approx J_{generation} = qwU_{eff} = qw\frac{n_i}{\tau_{eff}} \tag{3.25}$$

where $J_{leakage}$ and $J_{generation}$ are the leakage current density and space-charge generation current density respectively, $q$ is carrier charge, $w$ is the depletion width, $U_{eff}$ is the effective generation rate (i.e. the sum of the generation rates due

to all participating generation-recombination centres), $n_i$ is the intrinsic carrier density, and $\tau_{eff}$ is the effective minority carrier lifetime. For low-injection forward bias, the current is dominated by recombination and is therefore also proportional to $U_{eff}$. Thus the leakage current density at high bias and the forward current at low forward bias can both be expected to increase with trap concentration, and therefore to decrease with isochronal annealing temperature. Plots of reverse leakage current density at -20 V bias and forward current density at 0.1 V bias are shown in Fig. 3.11.

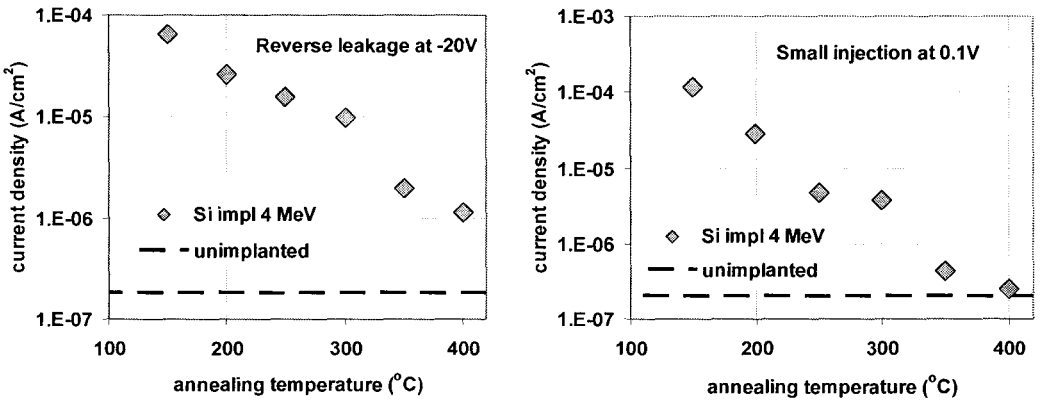


Fig. 3.11: Measured current density for E-Sil devices at -20 V bias (left) and 0.1 V bias (right as a function of isochronal annealing temperature. Note that both show an abrupt decrease at 300 °C.

Both the reverse leakage current and the low-injection forward current exhibit an abrupt drop for annealing at temperatures higher than 300 °C. This is consistent with the presence of the divacancy, which dissociates rapidly at 300 °C.

The current-voltage characteristic of the E-Bor sample compared to the unimplanted $n^+p$ junction is shown in Fig. 3.12. As expected from the relative damage densities discussed in section 3.3.3, the leakage current under reverse bias and the recombination current under low-injection forward bias are both significantly higher than the values measured for the E-Sil devices although by a factor of 100 rather than the expected factor of 50. This suggests that the defects remaining after the implantation step are not directly proportional to the initial

damage density, which is consistent with a second-order defect formed by clusters of first-order defects.

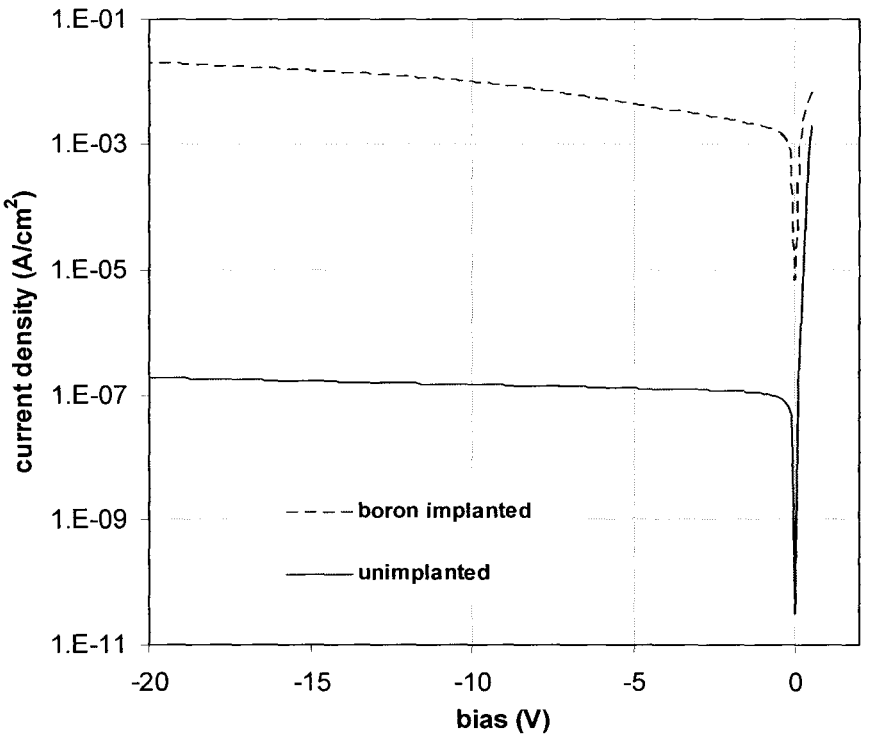


Fig. 3.12: *J-V* characteristic for the boron implanted sample with 150 °C anneal compared to the unimplanted E-Sil sample.

## 3.4.2 Capacitance-voltage measurements

Capacitance as a function of reverse bias voltage was measured for each device in darkness at 300 K and used to calculate depletion width and effective dopant density.

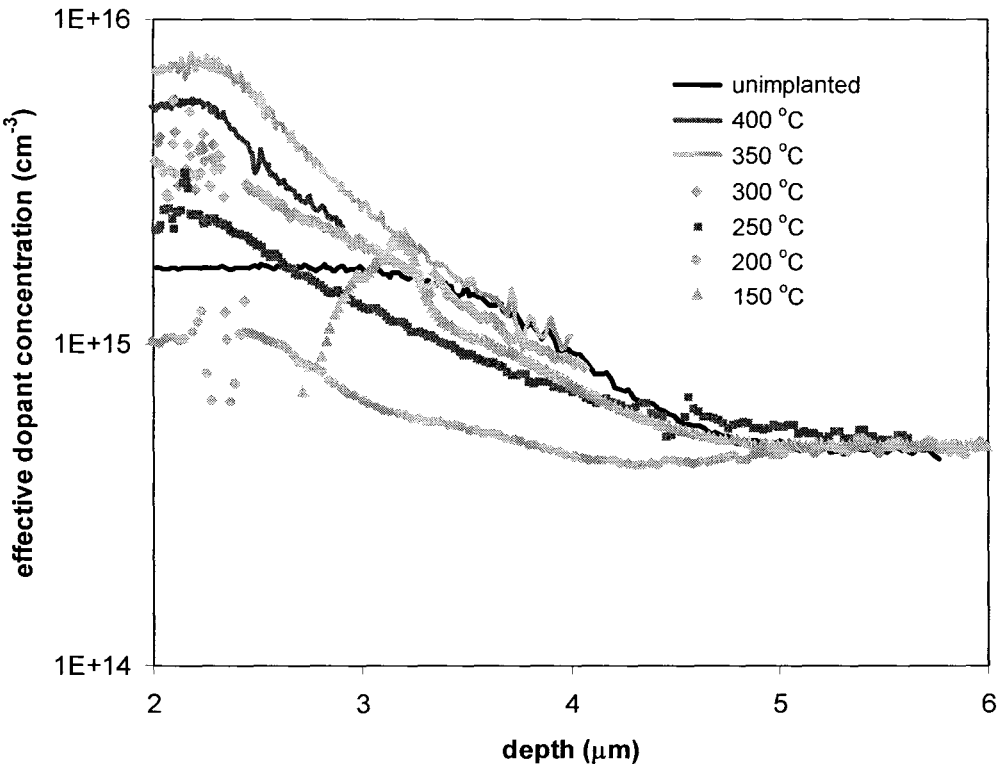


Fig. 3.13: Calculated dopant density versus depletion width for E-Sil diodes subjected to various annealing temperatures. The noise near 2.2 μm depletion width is assumed to be due to overlap between the depletion boundary and very high trap densities.

The calculated dopant concentration versus depth following the *C-V* measurements for the E-Sil samples with respect to annealing temperature are shown in Fig. 3.13. The profiles suggest that the initial implantation produces overall compensation of the dopant for depths less than 3 μm (i.e. hole traps), but subsequent annealing eliminates the compensating defects and instead produces defects which increase the net acceptor density (i.e. electron traps) up to anneals of 350 °C. It is noteworthy that for the two highest anneal temperatures, acceptor concentration exhibits a clearly discernible peak at a depth of 2.2 μm below the junction, which is 300 nm deeper than would be expected from the implantation range calculated using SRIM in Fig. 3.8 together with the junction depth calculated using Silvaco Athena in Fig. 3.7.

The changes in ionized acceptor density with depth in Fig. 3.13 also suggest that implantation-induced defects are present beyond the range of the ion implantation. As with the nonlinear variation in defect density with first-order implantation damage described in section 3.4.1, this indicates the presence of second-order defects formed from first-order defects which are mobile at room temperature and have diffused into the substrate before combining to form more stable defect complexes.

*C-V* results for the boron-implanted sample are shown in Fig. 3.14. A large increase in net acceptor density for depths less than 1.7 μm from the junction (i.e. 1.3 μm from the surface) is readily apparent suggesting that the implantation damage has generated minority-carrier traps predominantly in this range.

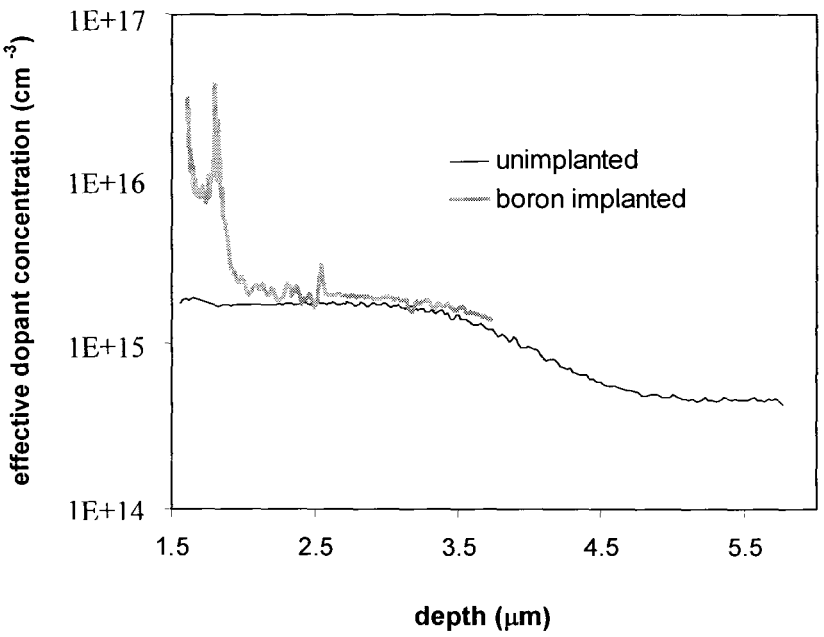


Fig. 3.14: Measurement of effective dopant density versus depth in a 350 keV, $1\times10^{13}$ $cm^{-2}$ boron-implanted sample. Acceptor concentration increases drastically for depths less than 1.7 μm.

### 3.4.3 DLTS measurements

***Measurement setup***

A DLTS system was custom-built to observe and characterize the defects produced by the ion implantation step in the fabrication process. The system was built around a cryostat from an HL5550PC Hall Kit Measurement System (Accent Optical Technologies). Devices were mounted in the cryostat and connected to one of two high-speed capacitance meters; a Boonton 7200 or a Sula Technologies Capacitance Meter Module. Bias pulses were controlled externally by a Tektronix AFG310 programmable function generator. Capacitance transients were amplified using a SULA Technologies Amplifier Module and recorded by a HP Infineon digital oscilloscope. The cryostat temperature, function generator output, and oscilloscope settings were controlled via GPIB commands from a controller PC using a purpose-built LabVIEW VI [151] which also filtered the capacitance transients and recorded the DLTS signal for a range of rate windows at each recorded temperature. The setup is illustrated in Fig. 3.15.

***Rate windows***

A digitally applied boxcar filter was used to process the capacitance transients and generate a DLTS signal. Since the entire capacitance transient was recorded by the digital oscilloscope, several rate windows could be measured simultaneously by filtering a single transient according to several time constants. Substituting $r=t_2/t_1$ into Eq. (3.24) simplifies the expression to Eq. (3.26)

$$\tau = \frac{(r-1)t_1}{\ln(r)} \tag{3.26}$$

from which timepoint sets ($t_1$, $rt_1$) can be derived for arbitrarily selected $r$ and $\tau$ values subject only to the limitations that (a) larger $\tau$ necessarily requires longer

transients, and (b) shorter $\tau$ necessarily requires higher resolution. There is a tradeoff, therefore, between the duration of the measurement and the number of averages made at each temperature, subject to the memory limitations of the oscilloscope.

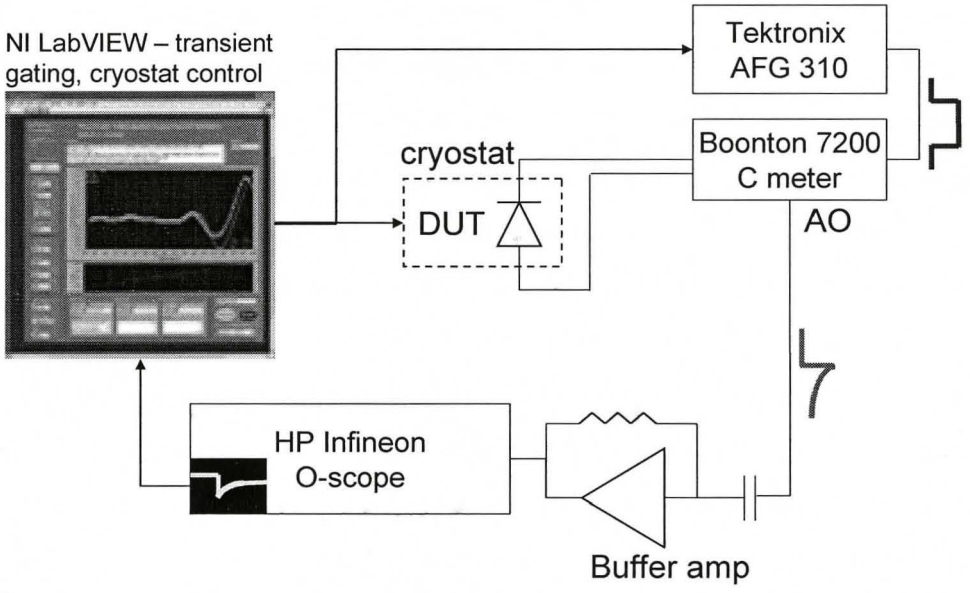


Fig. 3.15: DLTS measurement apparatus. The device under test (DUT) is mounted on a thermal controller in a cryostat and connected to a high-speed capacitance meter. The temperature and pulse parameters were controlled by a LabVIEW VI which also filtered the transients and recorded the DLTS signal.

Averaging was required to reduce the noise floor of the system; for the system described here it was found that signal-to-noise greatly benefited by employing the relationship $N=25*F$, where $N$ was the number of averages and $F$ was the collection rate. Collecting 20 transients per second, for example, required at least 500 averages for the best results. Since the time per datapoint is the number of averages $N$ multipled by the time per transient $1/F$, the time per datapoint was invariably at least 25 seconds to maximize the signal-to-noise ratio of the DLTS system.

The Infineon oscilloscope was found to require at least 25 ms recovery time between individual transients. Accordingly a transient length of 20 ms was employed, allowing 30 ms for oscilloscope recovery and a total repetition rate of

20 Hz. Averaging of 500 transients per data point was used. A timepoint ratio $r$=2.5 was arbitrarily chosen to allow at least five rate windows to be measured simultaneously during the 20 ms transient; substituting this ratio into Eq. (3.26) determined the lowest measurable rate window to be 80 $s^{-1}$. The timepoints used and their corresponding rate windows are listed in Table 3-1.

| rate windows ($s^{-1}$) | 80 | 200 | 400 | 1000 | 2000 | 5000 |
|---|---|---|---|---|---|---|
| timepoint 1 (ms) | 19.089 | 7.636 | 3.818 | 1.527 | 0.764 | 0.305 |
| timepoint 2 (ms) | 7.636 | 3.054 | 1.527 | 0.611 | 0.305 | 0.122 |

Table 3-1: Rate windows and corresponding timepoints used in the DLTS system, as determined by a maximum transient length of 20 ms and arbitrarily chosen $r$=2.5. The sampling rate of 500 kilosamples per second together with sub-microsecond risetimes on the bias source allows timepoints to be selected with ± 1 μs precision.

Rather than simply record the capacitance at each timepoint, the set of 101 points encompassing the timepoint were averaged in order to reduce noise. Consequently the temporal resolution required by the system was 500 kilosamples/second in order to capture at least 50 points prior to the first timepoint (0.122 ms) listed in Table 3-1.

For measurements at smaller rate windows, the sampling rate was divided by 10 and the averaging reduced to 50. The timepoints (rate windows) in Table 3-1 are thus multiplied (divided) by a factor of 10.

***DLTS spectra***

DLTS data were collected using filling pulses of 0 V (majority carrier filling) and 4 V (minority carrier filling) and emptying pulses of -20 V. The result for the E-Sil unannealed sample within the 200 $s^{-1}$ rate window is shown in Fig. 3.16.

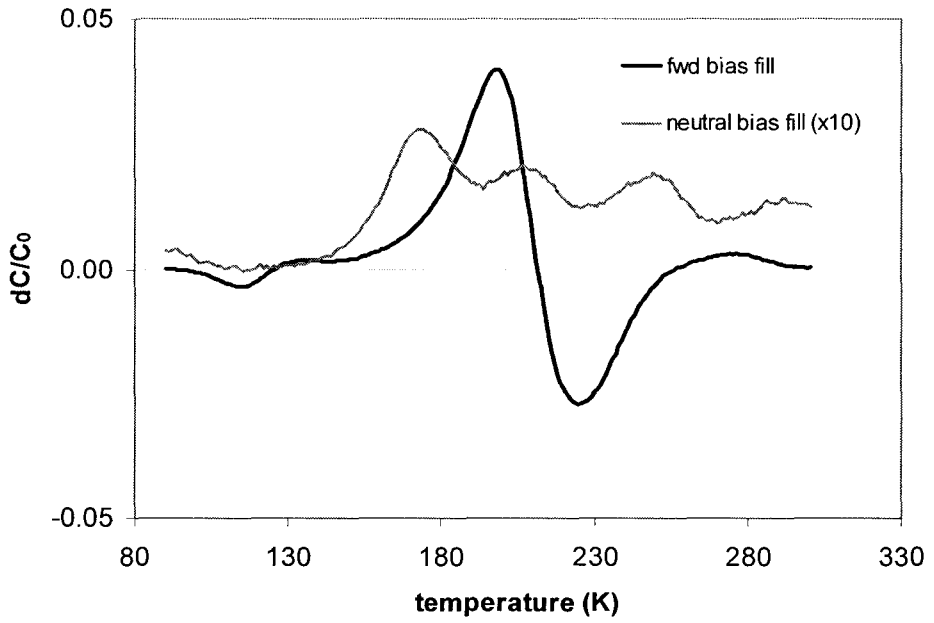


Fig. 3.16: DLTS spectrum for neutral and forward filling pulses for the 200 $s^{-1}$ rate window. The neutral bias fill peak has been scaled by a factor of 10 for clarity. Note that the negative peaks (acceptor states) are not seen when neutral bias (i.e. majority carrier) filling is employed.

DLTS spectra for eight rate windows spanning more than two orders of magnitude are shown in Fig. 3.17. There are four sets of peaks apparent in the DLTS traces with these rate windows: an acceptor trap state at 100 K to 140 K, a donor trap state at 170 K to 230 K, a second acceptor trap state at 190 K to 270 K, and a second donor trap state active at 250 K and higher.

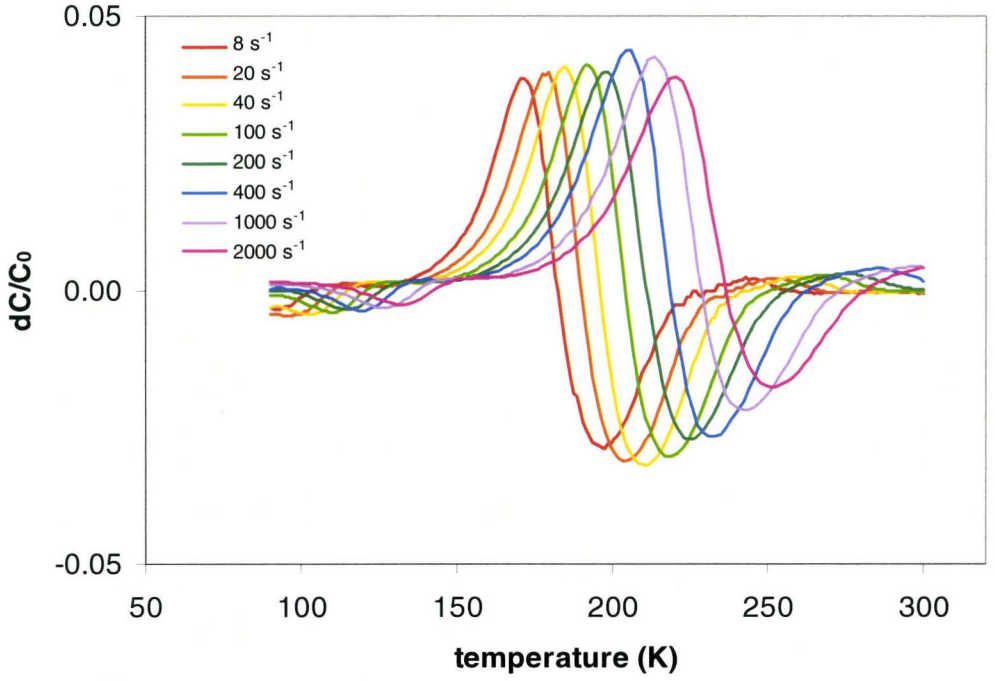


Fig. 3.17: DLTS spectra measured with a silicon-implanted unannealed sample filtered for various rate constants. Filling pulse is 4 V forward bias for 0.5 ms, emptying pulse is -20 V. Note the clearly defined sets of peaks showing four distinct defect levels: two acceptors and two donors.

### *Defect characteristics from DLTS*

The peak temperature for a given defect state in the DLTS spectra represents the temperature at which the defect primarily emits charge with a time constant corresponding to the rate window used in the measurement. Referring to Eq. (3.9) the energy difference between the defect state and the band to which it emits is represented by the slope of an Arrhenius plot of $\ln(T^2\tau)$ versus $1/kT$. Fig. 3.18 shows the Arrhenius plots corresponding to the spectra in Fig. 3.17 for each observed defect state.

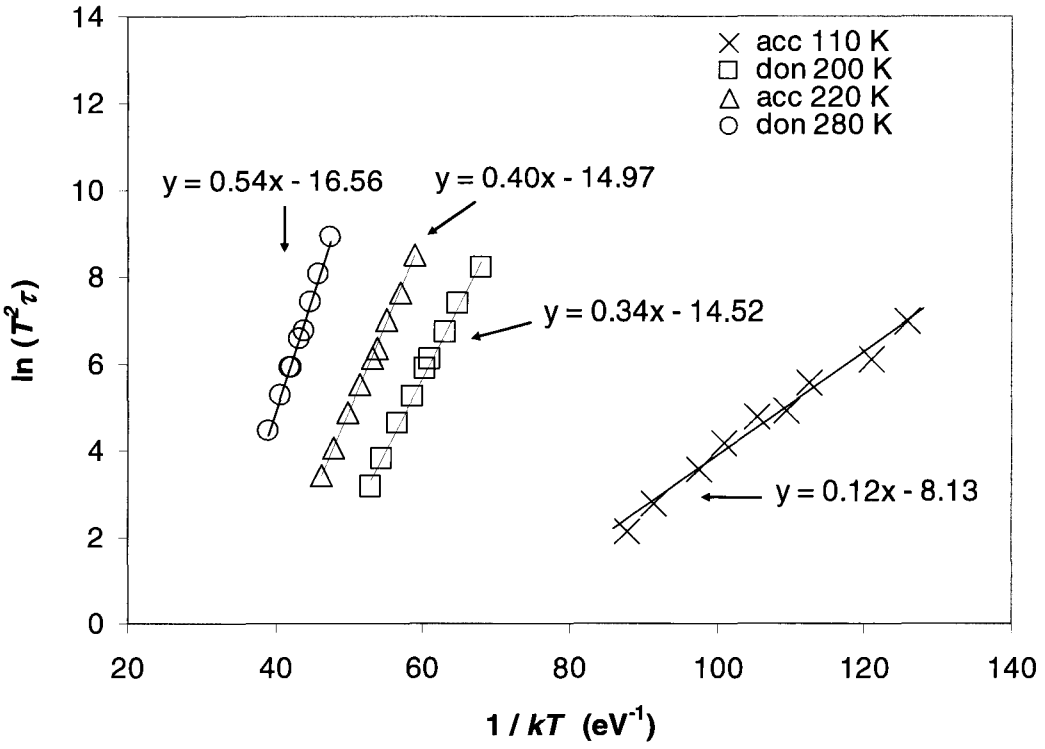


Fig. 3.18: Arrhenius plot for the four defect states detected by DLTS measurements for the unannealed E-Sil sample.

From the Arrhenius plot, the enthalpies of the four observed defects are $E_c$-0.12 ± 0.09 eV, $E_v$+0.34 ± 0.03 eV, $E_c$-0.40 ± 0.03 eV, and $E_v$+0.54 ± 0.03 eV. Since no deviation from linearity was observed in these plots (with the possible exception of the shallow acceptor state) it is assumed that the transition entropy is small compared to the transition energy; accordingly the enthalpy values listed above are assumed to be good approximations of the defect energies. The $E_c$-0.40 eV acceptor state is notable in that it is consistent with the known neutral/negative transition of the divacancy. The cross-sections for carrier capture can be estimated according to Eq. (3.9): using values for $N_c$ and $m_{th}^*$ from Green [152] yielded an electron capture cross-section of 7 (± 3) × $10^{16}$ $cm^2$ for the $E_c$-0.40 eV acceptor state.

### *Optical DLTS Setup*

To establish which of the observed defects are involved in optical detection at 1550 nm, the DLTS system was modified to incorporate optical filling-pulse capability. This technique is well-known [153, 154] although not generally used in tandem with standard telecommunication components and optical fibre as was implemented here; this approach bears strong resemblance to that reported by Harris *et al.* [157] using a "quartz light pipe".

A ThorLabs PRO800 1550 nm WDM module was fibre-coupled to an Anritsu MN9605C variable optical attenuator and the fiber tip was mounted 5 cm directly above the surface of the sample and oriented normal to the sample surface so as to illuminate it through a glass window in the cryostat. The laser output was pulsed via external control from the AFG310 function generator. A schematic of the apparatus is shown in Fig. 3.19 and a photograph in Fig. 3.20.

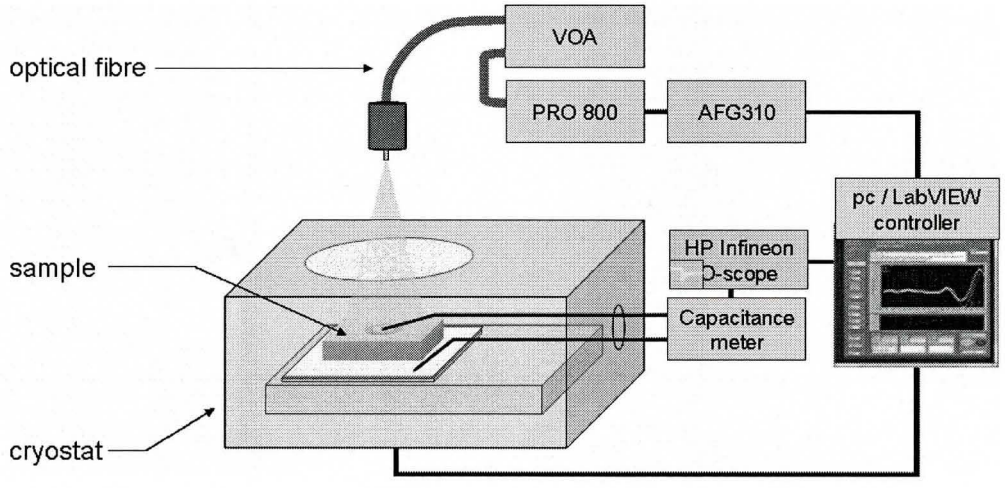


Fig. 3.19: Schematic of the optical DLTS apparatus: the sample (mounted on gold-plated ceramic) was situated inside the cryostat below a glass window through which it was illuminated by pulses from an optical fiber. VOA = variable optical attenuator; PRO800 = PRO 800 WDM laser source, and AFG310 = AFG310 function generator.

### *Optical DLTS Results*

Capacitance transients produced by optical pulses from the laser were observed and recorded while the sample was held under constant bias.

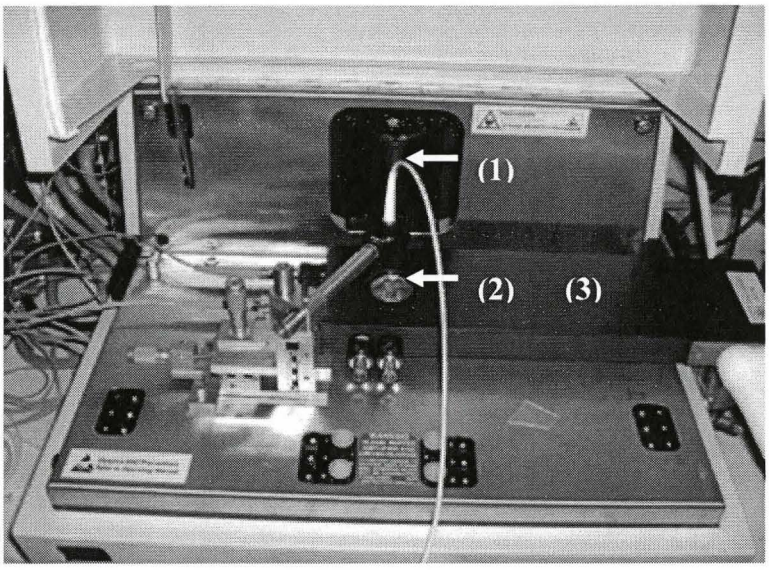


Fig. 3.20: Optical DLTS apparatus: (1) fibre mount, (2) window to sample, (3) cryostat.

The transients were seen to be "negative", i.e. capacitance initially increased during the optical filling pulse and then decreased once the illumination stopped. A typical measured capacitance transient is shown in Fig. 3.21.

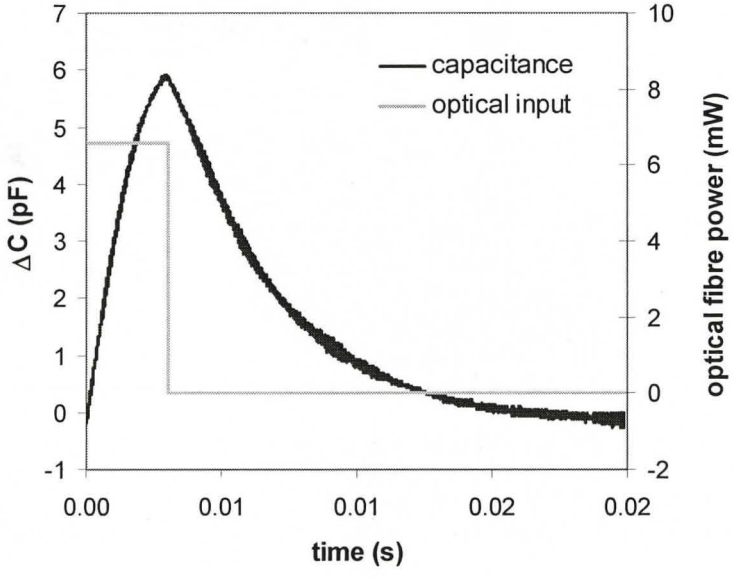


Fig. 3.21: Capacitance transient observed for a self-ion implanted $n^+p$ diode held at -20 V bias, 230 K and subjected to a 3 ms optical pulse at 1550 nm wavelength.

Since the optical pulse causes an increase in capacitance, it can be deduced that defect states within the space-charge region gain negative charge during the pulse, corresponding to the acceptor-trap scenario depicted in Fig. 3.1 (b).

Optical DLTS spectra for the sample held at -20V bias and subjected to optical filling pulses are shown in Fig. 3.22. For longer time constants a filling pulse width of 3 ms was employed whereas for the shorter time constants (400 $s^{-1}$ and higher) 0.75 ms filling pulses were used. Only one defect state was observed to be electrically active.

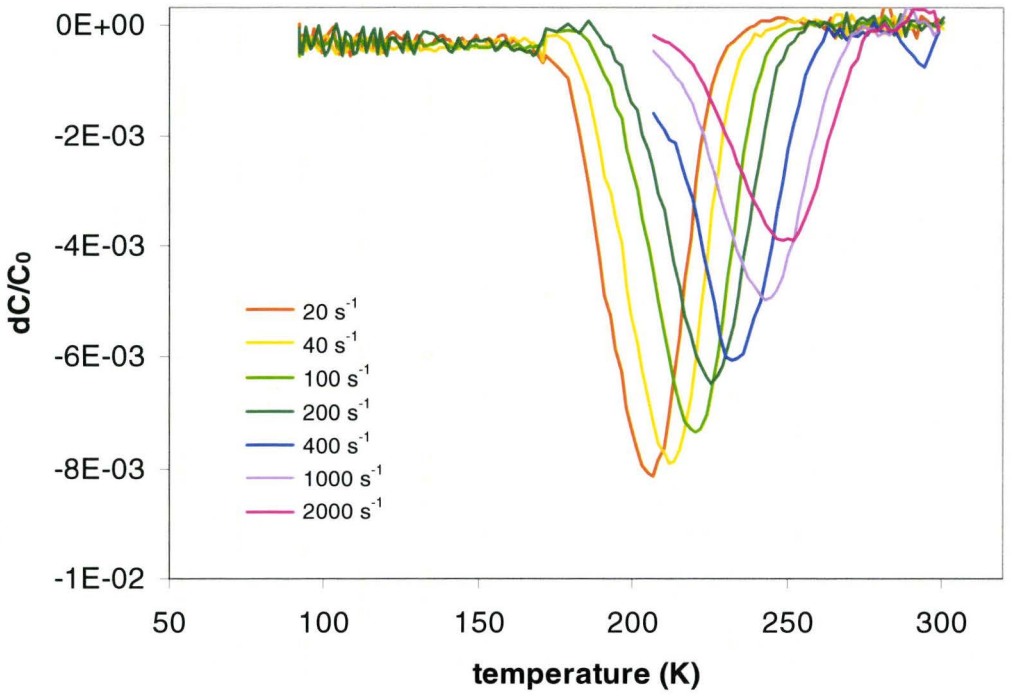


Fig. 3.22: Optical DLTS spectra for the unannealed E-Sil sample. Only one optically active defect state was observed: an acceptor trap with an emission rate constant that varied between 20 $s^{-1}$ and 2000 $s^{-1}$ at temperatures between 200 K and 250 K.

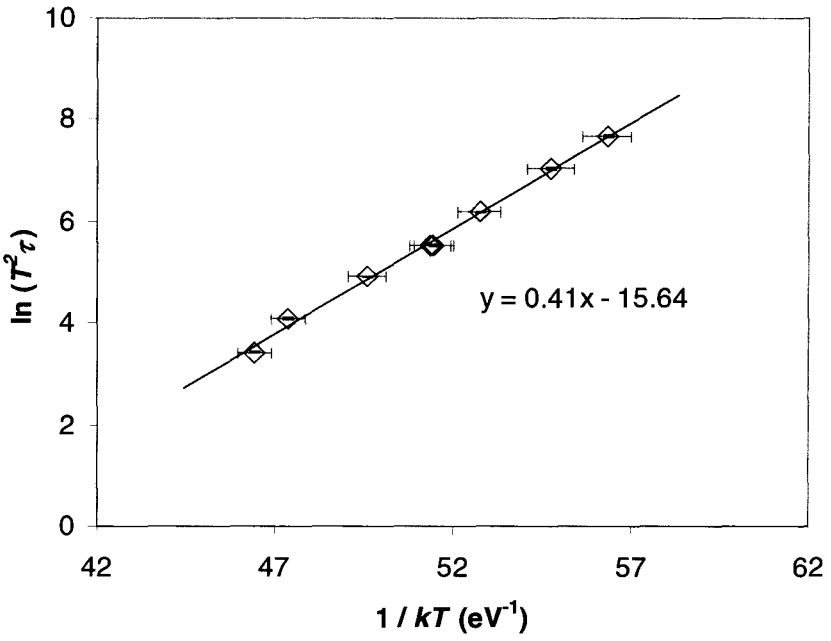


Fig. 3.23: Arrhenius plot for the defect state observed by optical-DLTS in the E-Sil unannealed sample.

The Arrhenius plot derived from the optical DLTS spectra is shown in Fig. 3.23 and establishes that the defect energy (subject once again to the assumption that the transition entropy is relatively small) is $E_c$-0.41 ± 0.03 eV; the electrical cross-section is calculated to be 8 (± 3) × $10^{-16}$ cm$^2$. This energy and carrier cross-section correspond to those found for the second acceptor state observed via conventional DLTS in Fig. 3.17, and also to the known divacancy negative/neutral transition as shown in Table 3-2.

| $E_c$-$E_T$ (eV) | $\sigma_n$ (cm$^2$) | **source** |
|---|---|---|
| 0.43 | $10^{-15}$ | Troxell *et al.* (1983) [137] |
| 0.421 | $2.6 \times 10^{-15}$ | Hallen *et al.* (1996) [141] |
| 0.415 | $1.9 \times 10^{-16}$ | Deenapanray *et al.* (2003) [155] |
| 0.436 | $3 \times 10^{-15}$ | Hazdra *et al.* (2009) [156] |
| 0.40-0.42 | $0.7\text{-}1 \times 10^{-15}$ | (this work) |

Table 3-2: Representative samples of reported energy and electrical cross-section for the divacancy VV(-/0) acceptor state.

Optical DLTS measurements of the E-Bor sample (unannealed) produced virtually identical results for the acceptor trap: energy $E_c$-0.41 ± 0.03 eV and an electrical cross-section of 1.0 (± 0.4) × $10^{-15}$ $cm^2$, suggesting that the dominant optically active defect was again the divacancy. However, a small positive peak was visible in the DLTS scan which indicated the presence of an optically active donor trap as well; this is shown in Fig. 3.24. This donor peak was deemed to be too ill-defined to produce a meaningful Arrhenius plot.

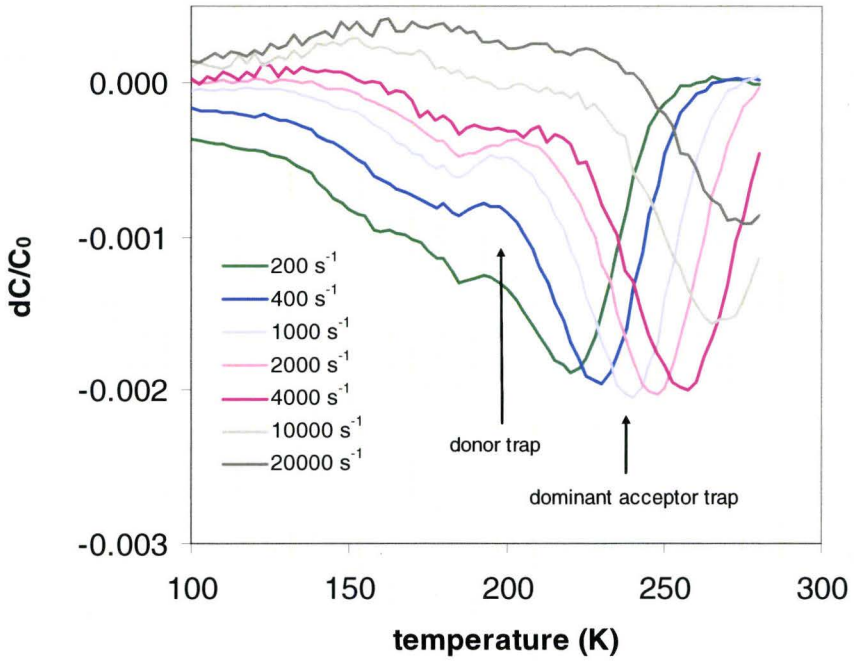


Fig. 3.24: Optical DLTS scan of 350 keV, 1 × $10^{13}$ $cm^{-2}$ boron-implanted sample showing mean acceptor trap peak near 250 K and secondary donor-trap feature at 200 K.

### 3.4.4 Equilibrium Capacitance Spectroscopy (ECS) Technique

The DLTS measurements described above indicate that the mechanism of defect-mediated absorption in the samples tested thus far is that corresponding to Fig. 3.1 (b), i.e. the photon excites an electron from the valence band to the trap state and the trap then thermally emits the electron to the conduction band. From this

hypothesis it follows that the traps should fill with negative charge if the optical excitation rate constant (henceforth denoted as $r_{opt}$) is much greater than the thermal emission rate constant (henceforth denoted as $r_{th}$). Conversely, the traps should empty of negative charge when $r_{opt} << r_{th}$. For the case of an $n^+p$ junction, therefore, the capacitance should increase to a maximum under the $r_{opt} >> r_{th}$ condition and decrease to a minimum under the $r_{opt} << r_{th}$ condition. The following experiment was devised to test this prediction.

***Experimental setup***

The sample was mounted inside a cryostat and subjected to illumination (wavelength 1550 nm) from a standard singlemode fibre as for the optical DLTS measurement illustrated in Fig. 3.19, however in contrast to optical DLTS the optical signal was held constant at 8.2 dBm (fibre output) rather than pulsed. The sample was biased at -20 V and cooled to 100 K, after which the capacitance was recorded while the temperature was increased to 300 K. This procedure was similar in practice to the conventional TSCAP method described in section 3.2.3 except that the device was illuminated during the thermal ramp.

***Results and discussion***

A plot of capacitance for an illuminated silicon-implanted sample versus temperature is shown in Fig. 3.25. As expected, the sample exhibited high capacitance at low temperature and low capacitance at high temperature. An abrupt transition from high to low capacitance was observed between 190 K and 240 K.

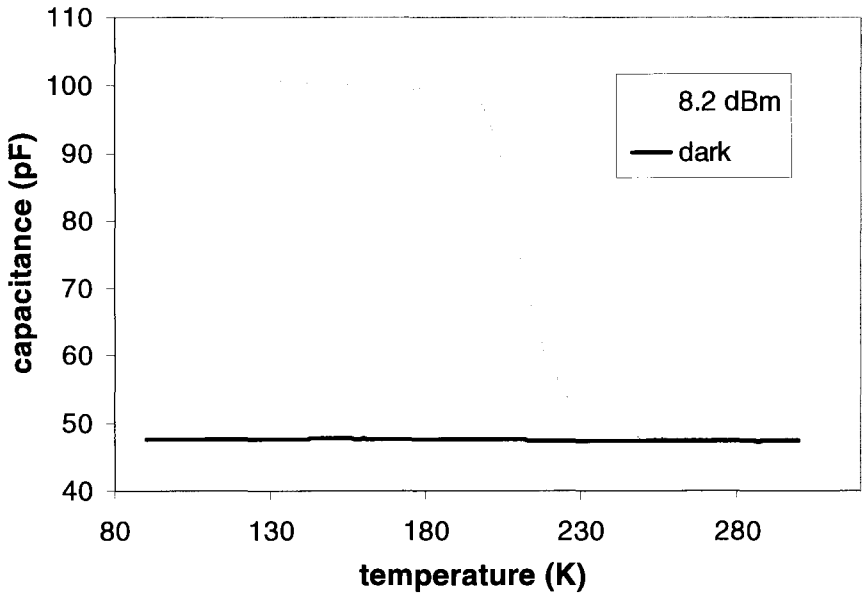


Fig. 3.25: Thermally stimulated capacitance for a silicon-implanted unannealed sample at -20 V bias under 8.2 dBm optical fibre output and in darkness.

Carrying the reasoning one step further, since the capacitance transitioned from high (all acceptor-traps filled) to low (all acceptor-traps empty) because of the changing thermal emission rate constant, this transition marks the range within which $r_{th}$ was comparable to $r_{opt}$. Furthermore, the optical fill rate constant $r_{opt}$ is proportional to the photon flux density $\phi$ according to Eq. (3.27):

$$r_{opt} = \sigma_{opt}\phi \tag{3.27}$$

where the proportionality constant $\sigma_{opt}$ is the trap optical cross-section. Thus, one can expect that reducing the photon flux density causes the transition from high capacitance to low capacitance to occur at lower temperatures. This was confirmed by thermally stimulated capacitance measurements versus fibre optical power as shown in Fig. 3.26.

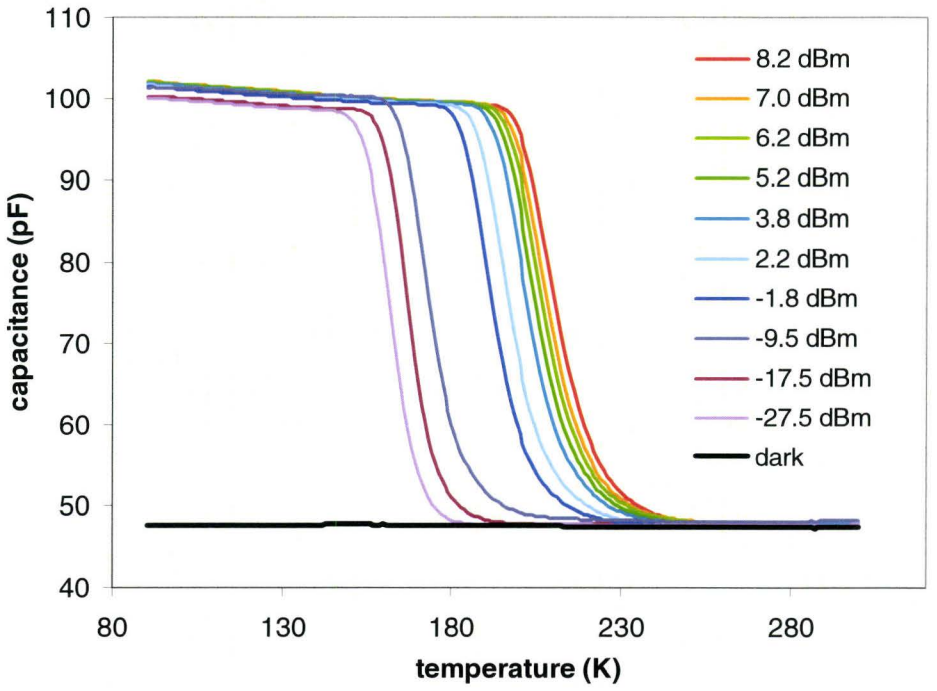


Fig. 3.26: Thermally stimulated capacitance measurements of the unannealed E-Sil sample at -20 V bias and various fibre optical power levels. The transition from high to low capacitance shifts to higher temperatures with higher incident optical power.

***Optical cross-section***

Eq. (3.27) suggests that the optical cross-section of the trap can be measured if the optical filling rate constant is known, thus providing a new technique for measuring this important parameter. The means by which this can be done will now be described.

Under steady-state conditions the density of occupied traps is constant:

$$\frac{dn_T}{dt} = r_{opt}(N_T - n_T) - r_{th} n_T = 0 \tag{3.28}$$

where $n_T$ is the density of occupied traps, $N_T$ is the total trap density, and $r_{opt}$ and $r_{th}$ are the optical and thermal rate constants respectively. Solving Eq. (3.28) for $r_{opt}$ yields Eq. (3.29):

$$r_{opt} = \frac{r_{th} n_T}{(N_T - n_T)}, \tag{3.29}$$

and for the case in which $n_T = \frac{1}{2} N_T$ (i.e. exactly half the traps contain negative charge), $r_{opt} = r_{th}$ . From Eq. (3.16) the capacitance $C_m$ at which $n_T = \frac{1}{2} N_T$ is given by Eq. (3.30):

$$C_m = \left[\frac{1}{2}\left(C_F^{\,2} + C_E^{\,2}\right)\right]^{1/2} \tag{3.30}$$

where $C_F$ and $C_E$ are the capacitances for the cases where the traps are filled and empty respectively. For the measurements shown in Fig. 3.26, $C_F$ = 100 pF (the capacitance at low temperature), $C_E$ = 47 pF (the capacitance at high temperature), and $C_m$ = 77.5 pF. The temperatures $T_m$ at which the capacitance passed through $C_m$ are plotted as a function of optical fibre power in Fig 3.27.

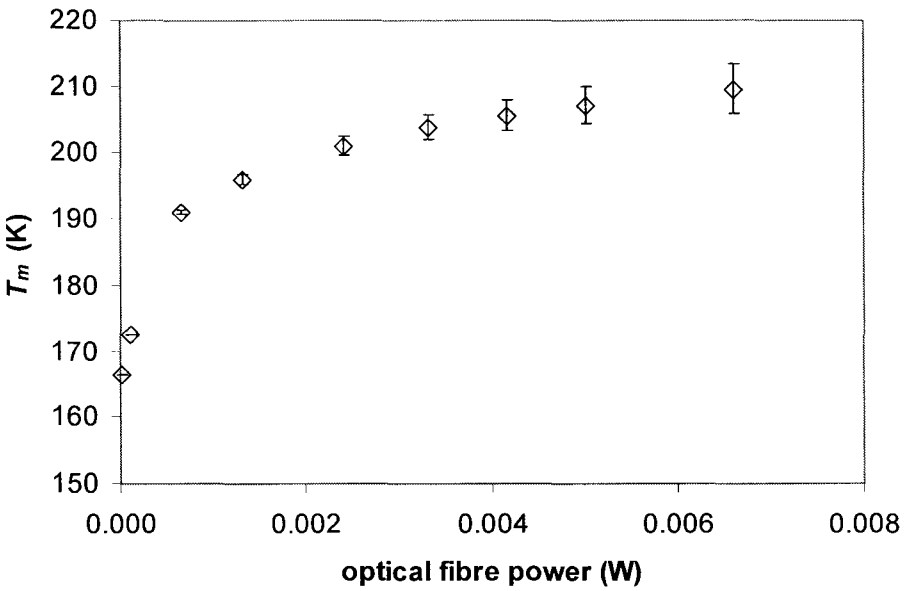


Fig. 3.27: Temperature at which the E-Sil device capacitance crosses $C_m$ = 77.5 pF as a function of fibre optical power.

Using the Arrhenius relationship derived from measured trap thermal emission rates in Fig. 3.23, the rate constant $r_{th} = r_{opt}$ corresponding to each $T_m$ can be calculated from Eq. (3.29). The result of this conversion is plotted in Fig. 3.28

versus photon flux density at the junction. The linearity of the plot suggests that the Arrhenius relationship is correct, and the slope of the plot represents the defect's optical cross-section according to Eq. (3.27); this value was found to be $6.0 \pm 0.7 \times 10^{-17}$ cm$^{-2}$. The measurement of photon flux density versus fibre optical power is described in Appendix B.

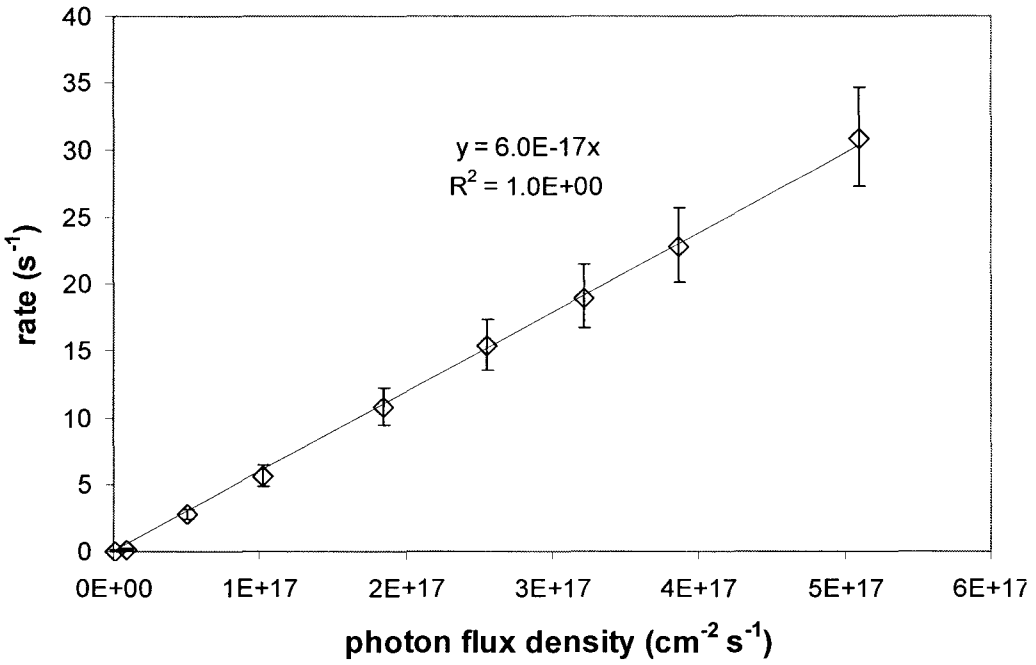


Fig. 3.28: Plot of the thermal rate constant for the equilibrium point capacitance $C_m$ as a function of photon flux density. The linearity of the plot confirms the energy used to calculate thermal emission (-0.41 eV); the slope is a measure of optical cross-section.

The measured value for the optical cross-section is higher than that previously reported in the literature; Cheng *et al.* [142] and Stein *et al.* [135] reported a value of $1.3 \times 10^{-17}$ cm$^{-2}$, and Foster *et al.* [118] reported optical absorption and positron annihilation spectroscopy results which correlated with this value. However Carton-Merlet *et al.* [138] have reported a value of $1.5 \times 10^{-15}$ cm$^{-2}$ for longer wavelengths (3.9 μm) for which Cheng reports a factor of 2 to 5 increase relative to the absorption peak at 1.8 μm. Thus if both Carton-Merlet's estimate for the cross-section at 3.9 μm and Cheng's estimate for the relative absorption compared

to 1.8 μm are true, an optical cross-section at 1.5 μm of (2.5 - 6.5) × $10^{-16}$ $cm^2$ would be expected.

***Thermal emission rates from ECS***

For this work the Arrhenius relationship between the defect emission rate and temperature was first measured via DLTS and then used to calculate the optical cross-section from the ECS measurements. However, the energy of the defect state can also be calculated directly from the ECS results without recourse to alternative measurement techniques by substituting Eq. (3.27) into Eq. (3.9) to obtain Eq. (3.31):

$$\ln\left(\frac{\phi}{T^2}\right) = \ln(\gamma\sigma) - \ln\left(\sigma_{opt}\right) - \frac{E_c - E_T}{kT}. \tag{3.31}$$

The slope of a plot of $\ln(\phi/T^2)$ versus $1/kT$ therefore provides a measurement of the defect energy as illustrated in Fig. 3.29.

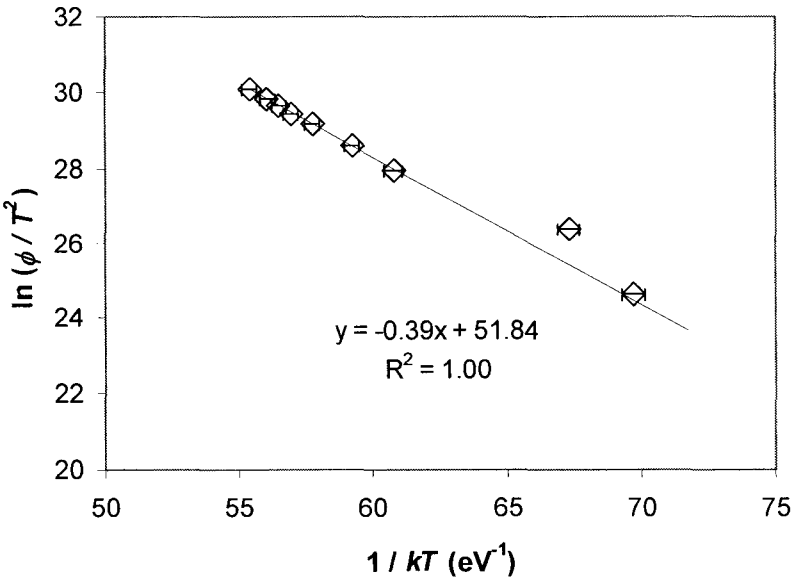


Fig. 3.29: Plot of the expression described in Eq. (3.31) to derive defect energy directly from the measured ECS results. The two points at lowest photon flux density (far right) were not used in the linear fit.

The defect energy calculated via this method was $E_c$-$E_T$ = 0.39 ± 0.03 eV, consistent with the values measured via conventional and optical DLTS. There is no means of distinguishing the contributions of the two cross-section terms in Eq. (3.31) from each other, however, so the technique can provide either defect energy and cross-section, or optical cross-section, but not all three without additional information.

***Average trap density***

Since the transition from high to low capacitance represents the transition from $n_T \approx 1$ to $n_T \approx 0$, the average trap density $N_{T\,(avg)}$ within the space-charge region (optically active trap state only) can be estimated by re-expressing Eq. (3.16) as shown in Eq. (3.32):

$$N_{T(avg)} = N_D\left(\frac{C_F^{\,2}}{C_E^{\,2}} - 1\right) \tag{3.32}$$

where $C_F$ and $C_E$ are the capacitances for all the traps filled and emptied respectively, and $N_D$ is the dopant density. For the unannealed E-Sil sample, $N_{T(avg)}$ for -20V bias corresponding to a depletion width of 6.8 μm was calculated to be approximately a factor of 3 higher than the dopant density, or $3 \times 10^{15}$ cm$^{-3}$.

***Multiple trap states by ECS***

For the case of multiple optically active trap states, the ECS technique would be expected to exhibit an abrupt drop (minority carrier traps) or increase (majority carrier traps) for temperatures corresponding to the $r_{th} \approx r_{opt}$ regime for each trap, thus permitting either the energy and electrical cross-section or the optical cross-section of each to be distinguished.

### 3.4.5 Trap concentration profiles

Although the average concentration of optically active traps can be estimated using the overall change in capacitance caused by optically filling and emptying the traps as described above, the profile of the concentration cannot easily be determined in this manner since at defect concentrations comparable to doping, the depletion width changes drastically as traps empty and fill. As the boundary of the space-charge region encompasses new defects, they fill or empty accordingly, thus causing second-order capacitance changes [158].

Instead, the optically active trap concentration profile can be measured by holding capacitance (and hence the location of the space-charge boundary) constant while the traps are optically filled or emptied [159, 160]. This approach is commonly referred to as Constant Capacitance Transient Spectroscopy (CCTS). The apparatus used for optical DLTS was modified in this work to accomplish CCTS measurements of defect concentration versus depth by sampling the analogue output of the capacitance meter with a data acquisition card which in turn controlled the bias voltage applied to the device. The feedback loop was accomplished using a LabVIEW VI. A sample transient captured during this measurement for the unannealed sample held at 70 pF and 170 K is shown in Fig. 3.30.

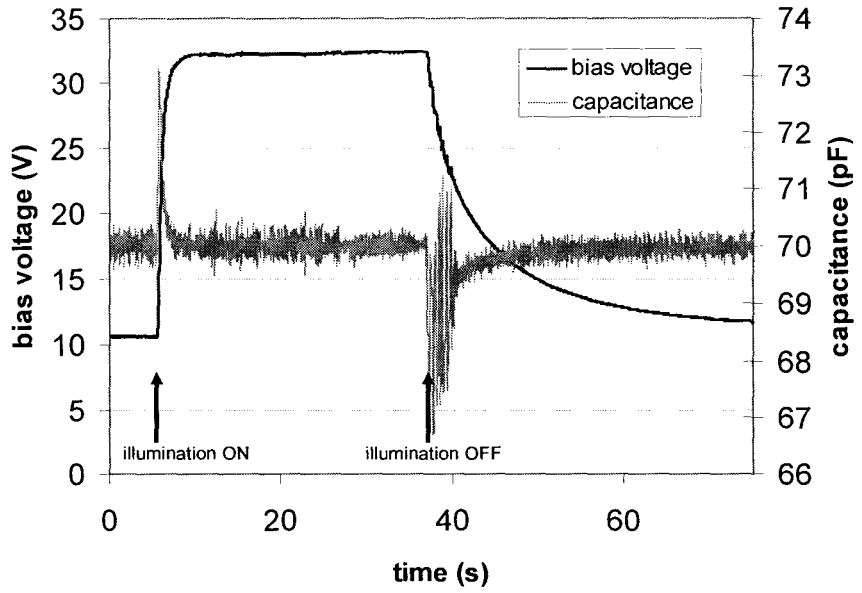


Fig. 3.30: Capacitance and bias voltage traces during a CCTS measurement of trap concentration. The capacitance was held near 70 pF in this measurement while the device was illuminated with an optical pulse. Bias voltage increases during the pulse to compensate for increased charge density within the space-charge region.

From Eq. (3.13) and Eq. (3.3), the change in bias voltage corresponding to a change in ionized trap concentration is given by Eq. (3.33):

$$\Delta V = \frac{qw^2}{2\varepsilon}\Delta n_T \tag{3.33}$$

where $n_T$ is averaged over the width of the space-charge region. Measured results for the average trap concentration and calculated trap concentration profile (calculated as the derivative with respect to depletion width of the product of average concentration and depletion width) as a function of depth (i.e depletion width together with the estimated 700 nm junction depth) are shown in Fig. 3.31 for the E-Sil sample annealed at 350 °C. Measurements of the average optically active trap concentration at 100 pF (approximately 3.3 μm depletion width, or 4 μm depth measured from the silicon surface) versus annealing temperature are shown in Fig. 3.32.

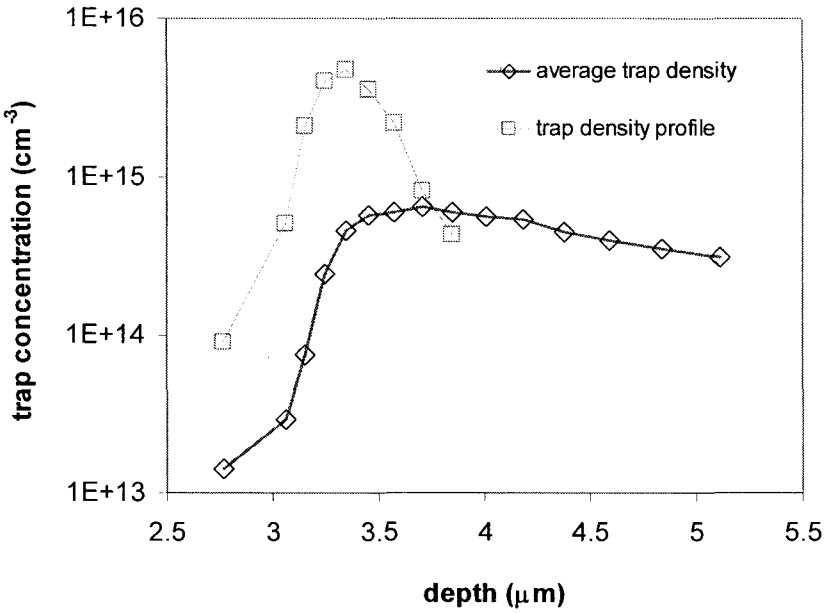


Fig. 3.31: Constant-capacitance measurements of the optically active trap average concentration within the space-charge region together with the calculated trap concentration profile for E-Sil annealed at 350 °C.

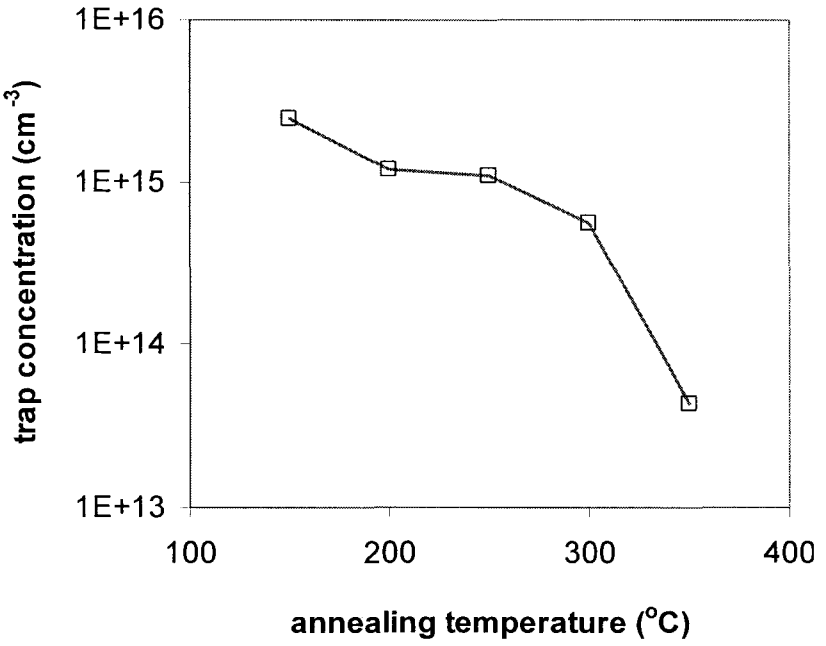


Fig. 3.32: Constant-capacitance measurements of the average optically active trap density within the space-charge region of the E-Sil samples as a function of isochronal (10 minute) annealing temperature.

An estimate of the divacancy concentration at half the ion range for the unannealed sample can also be derived using the Coleman-Burrows-Knights (CBK) equation [143]; this value is calculated to be $3.6 \times 10^{16}$ $cm^{-3}$, which is an order of magnitude higher than the value of the average concentration measured above. It should be noted however that the average concentration over a 3.3 μm depletion width from 0.7 μm depth to 4 μm depth is likely to be considerably lower than the divacancy concentration at half ion range (1.3 μm) if the concentration reaches a peak and then drops to zero well before the edge of the space-charge region, as the measurements of Fig. 3.31 indicate that it does. As shown in Fig. 3.31, the average concentration was indeed an order of magnitude lower than the peak concentration for the E-Sil sample annealed to 350 °C. It is also noteworthy that the depth of the peak concentration in Fig. 3.31 approximately corresponds to the peak measured for the same sample via *C-V* measurements in Fig. 3.13 (i.e. 2.3 μm depletion width together with 700 nm junction depth), but is deeper than the concentration profile calculated by SRIM for the as-implanted sample (see Fig. 3.8).

***Defect concentration in a boron-implanted device***

Thermally stimulated capacitance of the B-Sil sample under 8.2 dBm optical fibre illumination showed a positive capacitance step prior to the expected capacitance drop as shown in Fig. 3.33. This indicates an optically active donor trap and is consistent with the secondary peak observed and commented on in the DLTS results.

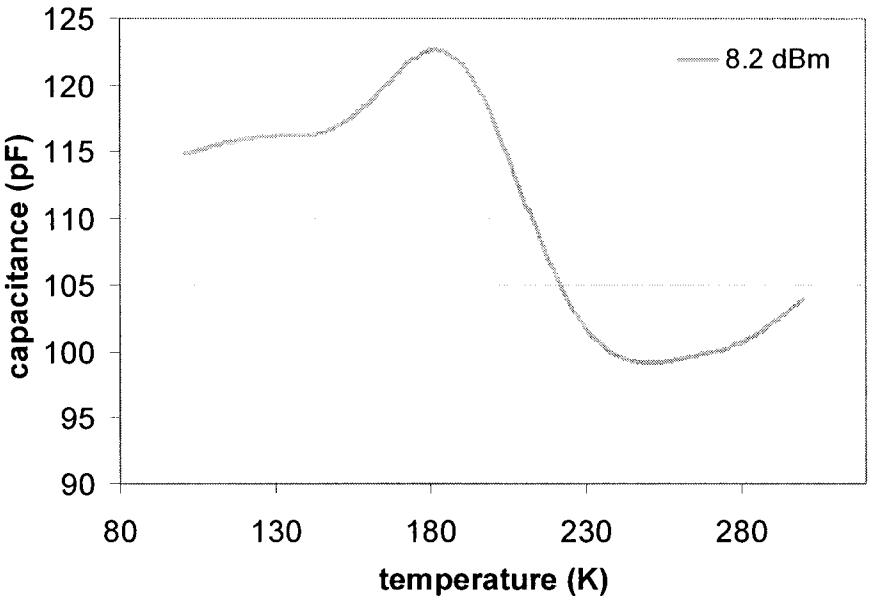


Fig. 3.33: Thermally stimulated capacitance of the B-Sil sample under 8.2 dBm optical fibre illumination. The trace exhibits an upward trend near 170 K corresponding to the optically active donor defect observed in the optical DLTS measurements, as well as the expected downward trend corresponding to the divacancy.

The average concentrations of both the donor state and the acceptor state can be estimated according to Eq. (3.32) as $0.12N_D$ and $0.54N_D$ respectively, or approximately $2 \times 10^{14}$ cm$^{-3}$ for the donor state and $1 \times 10^{15}$ cm$^{-3}$ for the acceptor state across the entire depletion width. Considering the 1 μm ion range (see Fig. 3.8) and the 700 nm junction depth however, the true width of the trap density peak is estimated to be 300 nm; taking this into account the trap density within the implantation range is calculated to be $2.2 \times 10^{15}$ cm$^{-3}$ for the donor state and $1.1 \times 10^{16}$ cm$^{-3}$ for the acceptor state. The CBK equation for divacancy concentration at half ion range in this case is $6 \times 10^{17}$ cm$^{-3}$, considerably higher than the concentrations calculated here. It is likely that the two peaks shown in Fig. 3.33 interfere with one another; since they have opposite sign, artificially low estimates for the concentrations corresponding to each are a distinct possibility.

# 3.5 Waveguide integrated photodetectors

One of the earliest commercial applications of silicon photonics was the development of a silicon variable optical attenuator for operation in the *C*-band with fibre-optic transmission networks by Kotura, Inc. [46, 48]. This VOA incorporates highly efficient NVT couplers similar to the ones described in Chapter 1, Section 1.2.4 for fiber-to-chip mode conversion, and uses forward current injection to induce attenuation in the waveguide via the free-carrier effect as described in Section 1.2.6. A diagram of the waveguide-diode configuration for free-carrier injection adapted from [46] is shown in Fig. 3.34.

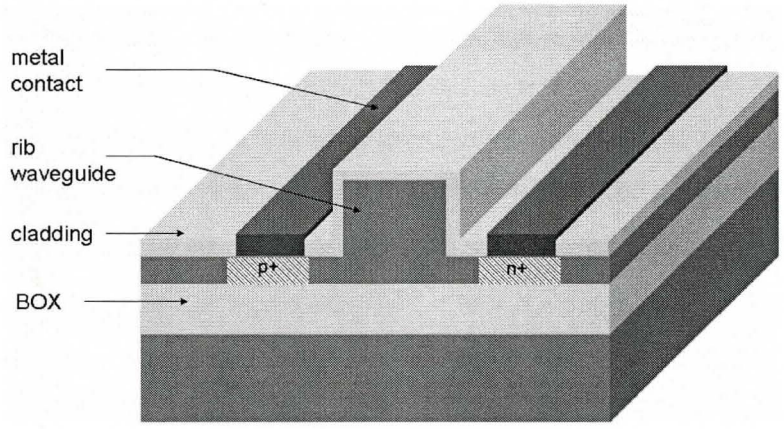


Fig. 3.34: Schematic of the Kotura Inc. carrier-injection VOA, adapted from [46].

Several of these devices in unpackaged form were generously donated by Kotura for this work. These will henceforth be referred to as "K-Sil" samples.

It is apparent from Fig. 3.34 that with the diode operated in reverse bias rather than forward bias, optical absorption within the waveguide via deep level defect states can be expected to produce photocurrent. Such a device has been demonstrated by Knights *et al.* [91-93] and is desirable as an integrated optical

power monitor. The K-Sil samples were therefore subjected to the same ion implantation and annealing process steps which were used for the E-Sil samples discussed in the previous section in order to correlate the device performance with the previously measured defect characteristics.

### 3.5.1 Ion implantation

The bare chips (each containing an array of devices) were subjected to the same implantation (4 MeV energy, $5 \times 10^{10}$ $cm^{-2}$) and annealing steps (isochronal 10 minute anneals in flowing nitrogen at temperatures from 200 °C to 400 °C in increments of 50 °C) used for the defect characterization described in section 3.3.

Because of the cladding dielectric layer on the silicon surface, the implantation range below the silicon was reduced. Simulations of the implantation using the Monte Carlo SRIM program (shown in Fig. 3.35) predicted implantation range in the silicon of 700 nm corresponding to a damage profile peak of 0.4 vacancies per implanted ion per angstrom – this predicted damage peak matched the peak value for the implantation of exposed silicon in section 3.3.

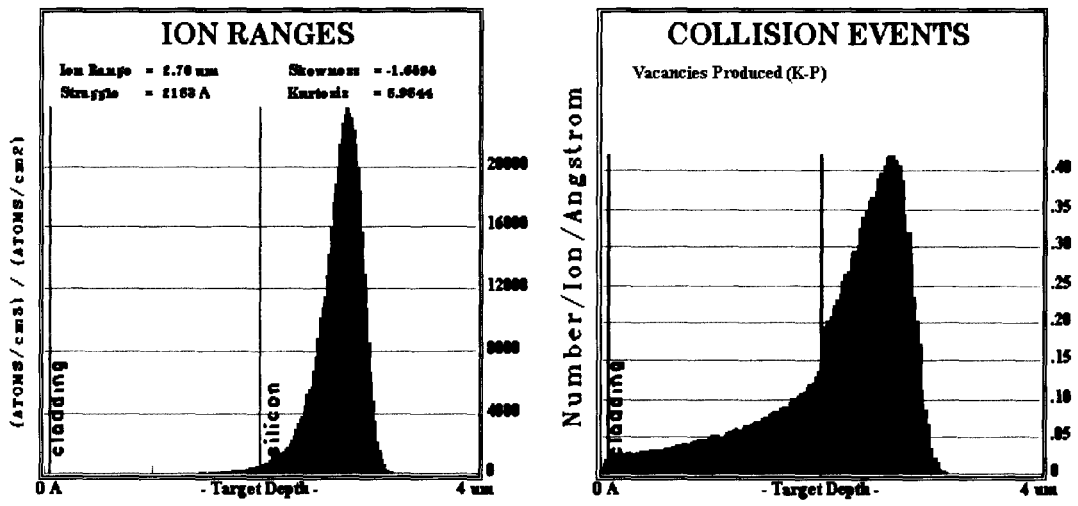


Fig. 3.35: SRIM simulations of 4 MeV self-ion implant into silicon through cladding representative of Kotura Inc. VOA devices. The left panel shows ion range (0.70 μm below the silicon surface) while the right panel shows a damage peak of 0.4 vacancies per ion per angstrom.

### 3.5.2 Characterization

All optical measurements described in this section were made using TE polarized light at 1550 nm wavelength.

***Current-voltage characteristics versus annealing***

Current density versus voltage measurements showed the expected degradation in the reverse leakage current density and the low-injection forward current density after implantation as was observed for the E-Sil samples. Partial recovery of the current densities was observed as a function of annealing temperature. *J-V* characteristic curves for the samples are shown in Fig. 3.36, and plots of reverse leakage at -10 V and low-injection forward current at 0.1 V are plotted in Fig. 3.37.

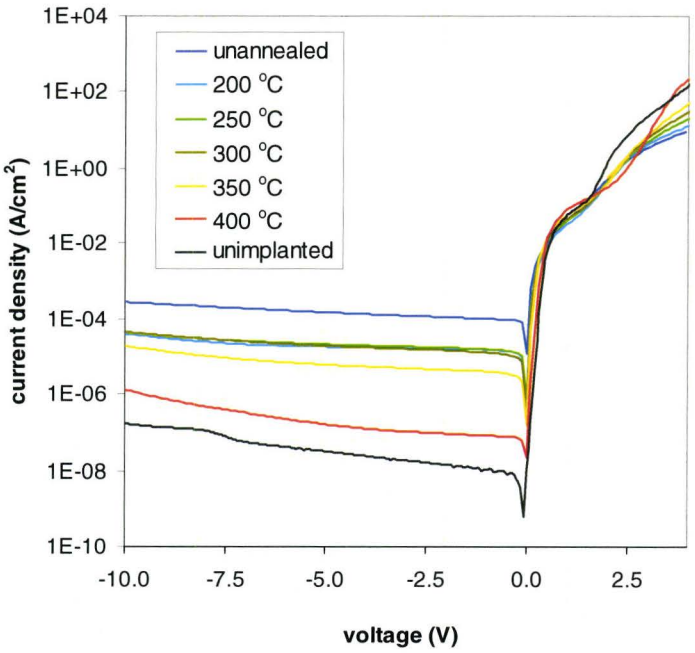


Fig. 3.36: *J-V* characteristic for implanted waveguide devices.

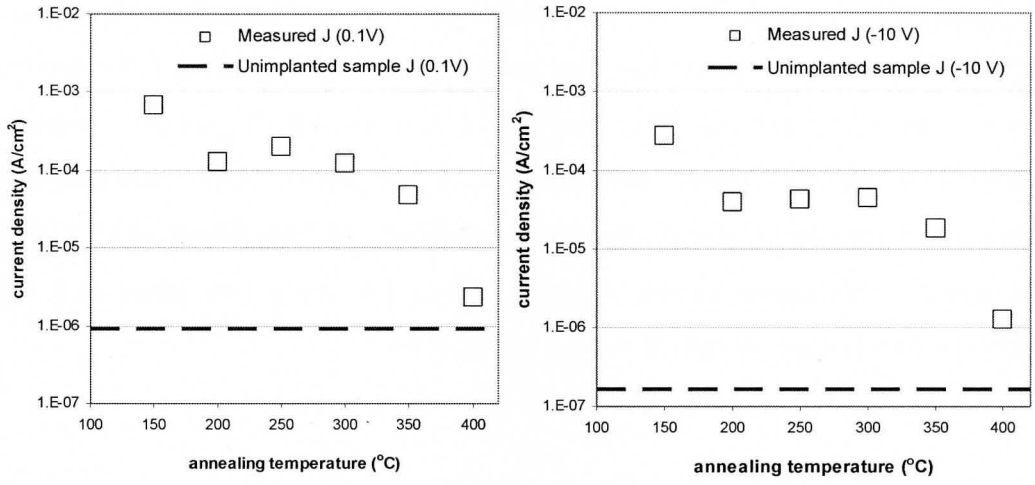


Fig. 3.37: Reverse leakage (left) and low-injection (right) current densities versus isochronal 10 minute annealing temperature of the K-Sil samples.

### *Variable optical attenuator performance*

Recalling Eq. (3.25), reverse leakage current and low-injection forward current are inversely proportional to carrier lifetime. Since operation of the device as a variable optical attenuator relies on free carrier absorption it was expected that attenuator efficiency would degrade after the implantation and recover with annealing. This was confirmed via measurements of optical attenuation versus forward injection current using the setup shown in Fig. 3.38.

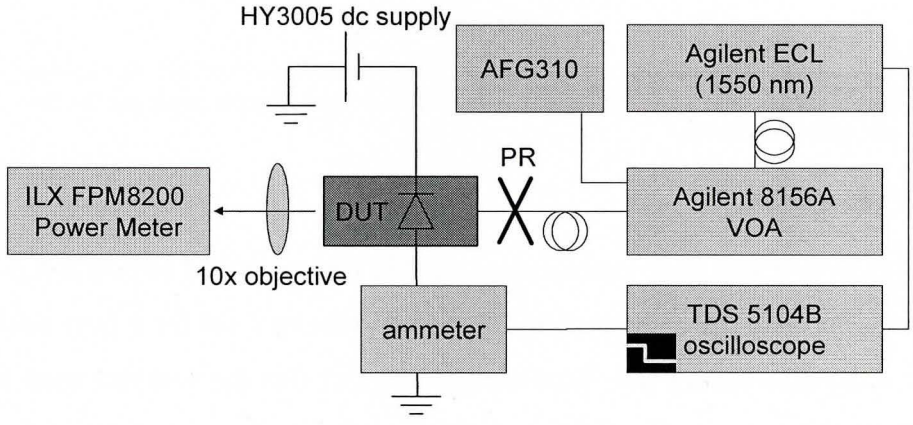


Fig. 3.38: Optical test setup for waveguide integrated photodiode. PR = polarization rotator, ECL = external cavity laser, AFG310 = function generator; VOA = variable optical attenuator; DUT = device under test. The input was standard single-mode fibre while the output was lens-coupled to a power meter.

No measurable injected free-carrier induced attenuation was achievable for as-implanted devices, nor for devices that were annealed up to 300 °C. The 350 °C annealed sample exhibited 0.07 $dBcm^{-1}mA^{-1}$ and the 400 °C annealed sample exhibited a slightly higher efficiency of 0.114 $dBcm^{-1}mA^{-1}$, whereas the unimplanted sample exhibited attenuation efficiency of 1.96 $dBcm^{-1}mA^{-1}$ [161]. The optical attenuation versus injected current for these two cases and the unimplanted reference sample is shown in Fig. 3.39.

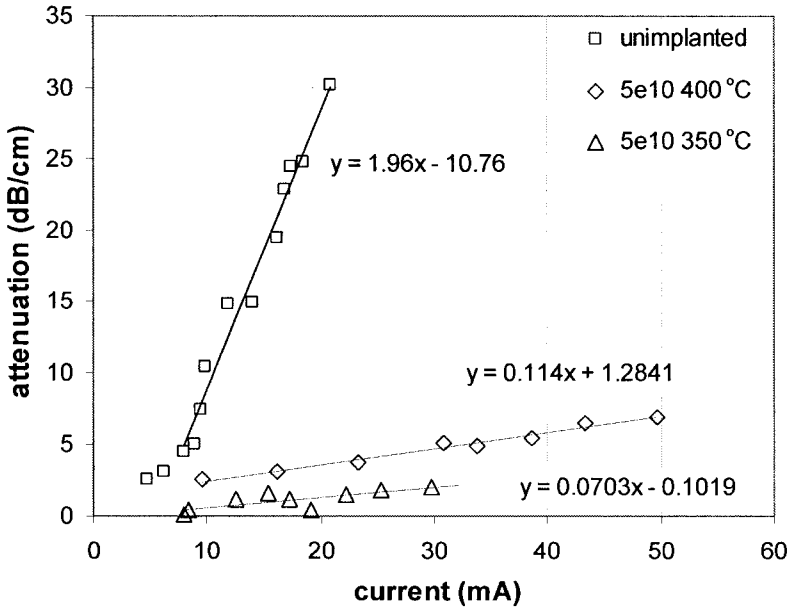


Fig. 3.39: Attenuation versus current of waveguide devices for the lowest implantation dose ($5 \times 10^{10}$ $cm^{-2}$) at two anneal temperatures compared to the unimplanted device.

### *Optical absorption*

Optical insertion loss of an unimplanted sample was measured to be 3.8 ± 0.1 dB. This is higher than the commercially specified value of 2 dB for a fully packaged device – the discrepancy was attributed to the fact that the samples used in this work did not have an anti-reflection coating on the input and output facets. The absorption loss per unit length due to implantation-induced defects was therefore calculated as the difference (in dB) between the optical loss for implanted samples

versus the unimplanted sample divided by the overall length of the chip. This loss was assumed to be entirely due to defect-induced optical absorption.

The optical absorption versus annealing temperature is shown in Fig. 3.40. A relatively small decrease in optical absorption versus annealing was discernible from 0.5 ± 0.12 dB/cm to 0.3 ± 0.12 dB/cm, however the variation was only slightly larger than the error margins of the measurement.

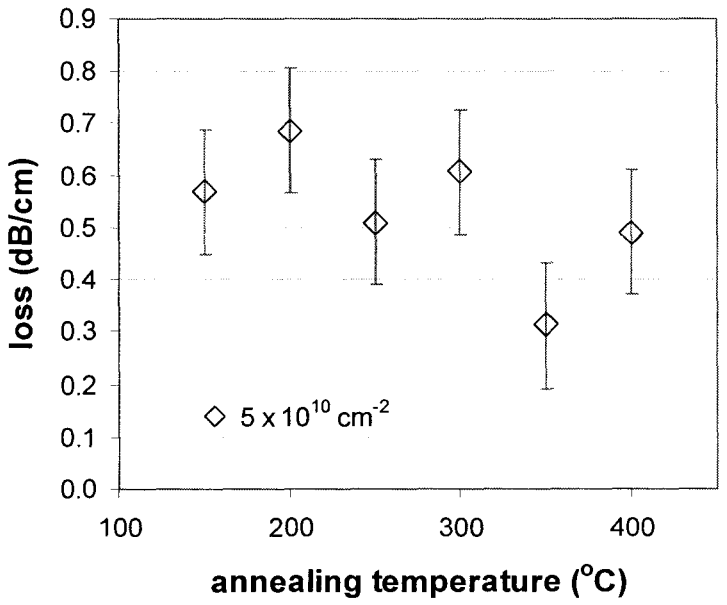


Fig. 3.40: Optical loss at 1550 nm wavelength relative to the unimplanted sample as a function of annealing temperature for the K-Sil samples implanted with a dose of $5 \times 10^{10}$ cm$^{-2}$.

In order to observe a significant variation in implantation-induced optical absorption versus annealing temperature, additional samples were implanted with silicon at the same energy (4 MeV) but higher doses of $1 \times 10^{11}$ cm$^{-2}$, $3 \times 10^{12}$ cm$^{-2}$, and $5 \times 10^{13}$ cm$^{-2}$ and then diced and subjected to the same annealing steps used for the low-dose series. The optical loss relative to an unimplanted sample was measured relative to the unimplanted reference sample is shown in Fig. 3.41 for all four implantation doses as a function of annealing temperature.

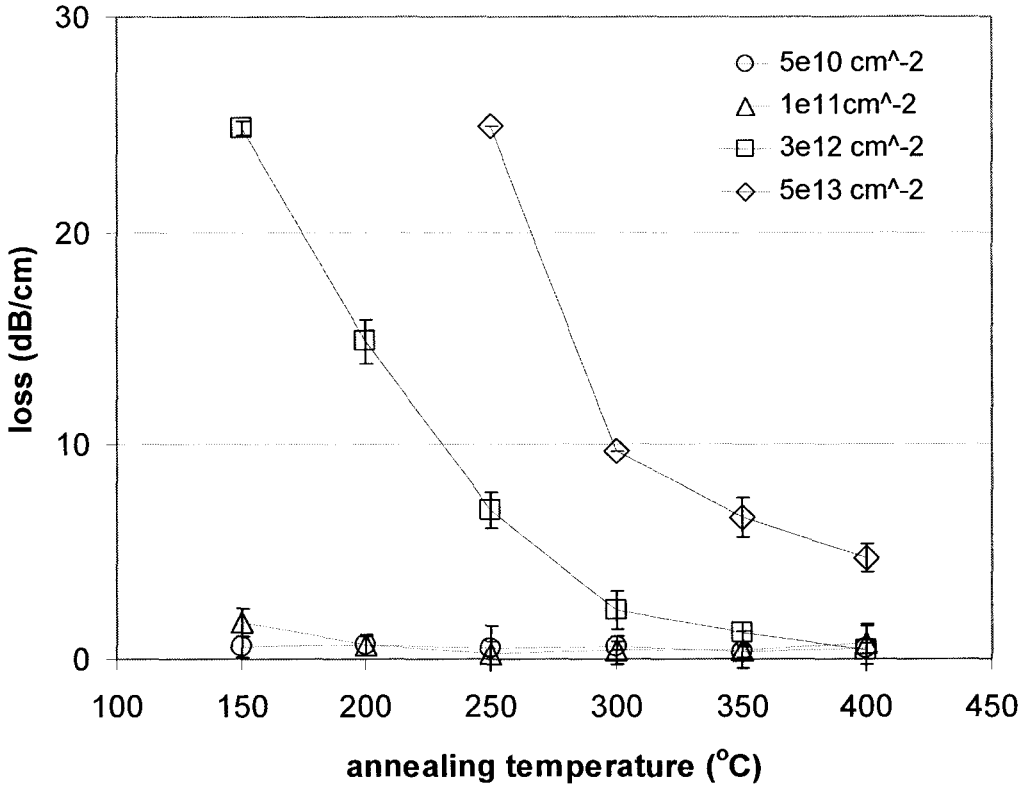


Fig. 3.41: Optical loss relative to the unimplated device as a function of annealing temperature and implantation dose.

For the higher doses, optical absorption which increased with dose and then recovered with annealing temperature was readily apparent.

***Responsivity and quantum efficiency***

The responsivity of the devices was measured by recording the difference between diode dark current and total current at 0.85 mW optical fibre input. The on-chip optical power (i.e. the optical power at the input end of the photodiode) was calculated by estimating the input and output coupling losses as the difference between the commercially specified insertion loss (2 dB) for a device with anti-reflection coatings and the measured insertion loss (3.8 dB) for an unimplanted K-Sil sample (no anti-reflection coatings) – i.e. the total coupler losses were assumed to be 1.8 dB. The remaining 2 dB loss (as specified for the commerical device) on the unimplanted sample was assumed to be propagation

loss evenly distributed across the chip. The input loss from the optical fibre to the diode was therefore calculated as $P_{diode} = P_{fiber} - 0.5(3.8\text{ dB} - 2\text{ dB}) - (2\text{ dB})(z_{in}/z_c) - Lz_{in}$, where $L$ is the absorption loss per unit length measured and plotted in Fig. 3.41, $z_{in}$ is the distance from the input facet to the diode, and $z_c$ is the total length of the chip.

The responsivity versus annealing and implantation dose is shown in Fig. 3.42. The internal quantum efficiency is simply the responsivity quoted here scaled by a factor of 0.8 eV/photon.

It was noted that the internal quantum efficiency of the devices decreases with annealing temperature as expected for the two lowest implantation doses, but exhibits a maximum for mid-range annealing temperatures for the higher doses. The latter result has also been observed by Knights *et al.* [162] and is as yet unexplained. One hypothesis is the possibility that larger vacancy complexes are formed at high doses which are less conducive to optical absorption, and that these complexes begin to dissociate and contribute to divacancy concentrations at temperatures below 300 °C.

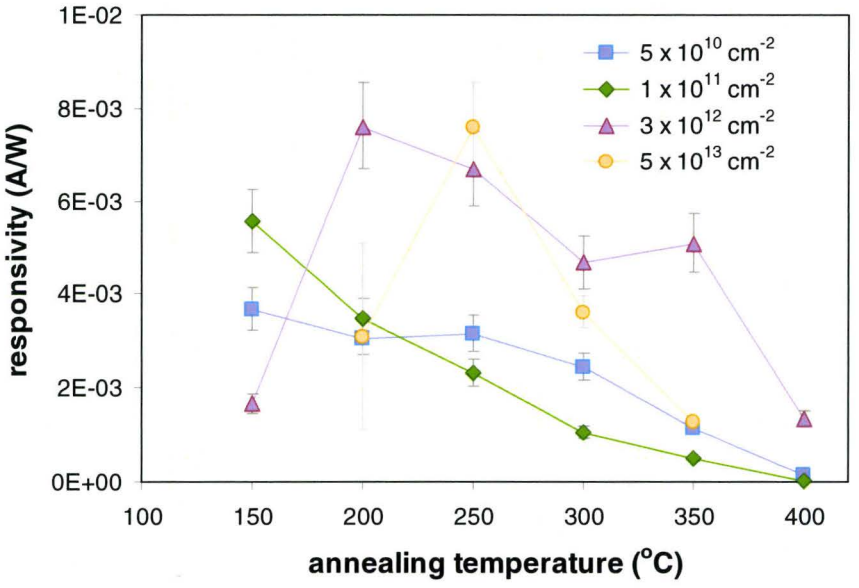


Fig. 3.42: On-chip responsivity of waveguide-integrated photodiode versus implantation dose and annealing temperature. Lines between points are merely a guide to the eye.

### 3.5.3 Correlation of defect properties and photodetector performance

The optical carrier generation rate can be expressed as a function of trap density $N_T$, optical flux density $\phi$, and optical cross-section $\sigma_{opt}$ according to Eq. (3.34):

$$g = \left(N_T - n_T\right)\sigma_{opt}\phi A dz \tag{3.34}$$

where $N_T$ and $n_T$ are the overall and occupied trap densities respectively, and $Adz$ is the volume. At room temperature and low optical flux density $n_T << N_T$; then assuming that all carriers generated are collected and integrating over distance $z$ provides a solution for quantum efficiency:

$$\eta = F\left(1 - e^{-\sigma_{opt} F N_T L}\right) \tag{3.35}$$

where $F$ is the overlap integral of the optical mode and the defect density and $L$ is the length. The optical flux density decreases according to Eq. (3.36):

$$\frac{\phi(z)}{\phi_0} = e^{-\alpha F z} \tag{3.36}$$

where $\alpha$ is the product of $\sigma_{opt}$ and $N_T$. Using the estimates for trap density and optical cross-section derived in the first half of this chapter, quantum efficiency and optical absorption loss can be estimated for the photodiodes characterized in the latter half of the chapter.

Fig. 3.43 shows a plot of the quantum efficiency calculated from the average divacancy density versus annealing (see Fig. 3.32) and the measured quantum efficiency according to Fig. 3.42 for the $5\times10^{10}$ cm$^{-2}$ dose implantation. Since the damage profile was unknown for all but one annealing temperature, it was impossible to calculate the overlap of defect density and the optical mode. However, assuming a constant damage density within the ion range of 1 μm predicted by SRIM calculations (see Fig. 3.35) yields a calculated mode overlap

fraction of 0.05; assuming a step function approximation of the peak measured for the 350 °C annealed sample (i.e. a 0.6 μm wide peak located 0.6 μm beyond the ion range - see Fig. 3.31) yields a calculated mode overlap fraction of 0.16. The quantum efficiencies versus annealing calculated according to these two values are plotted in Fig. 3.43 along with the measured values.

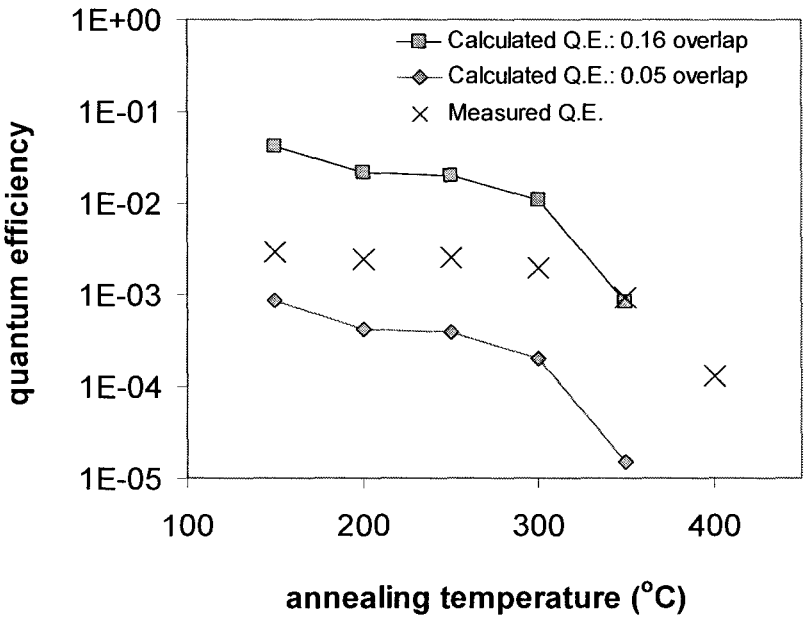


Fig. 3.43: Measured and predicted quantum efficiency versus annealing temperature. The two sets of predicted values are based on the assumption of a step profile matching (a) the defect distribution calculated by SRIM, and (b) the damage distribution measured for the 350 °C annealed sampled.

It is apparent from Fig. 3.43 that neither estimate of the trap density profile holds true across the range of annealing temperatures – the estimate using the profile calculated from SRIM is more accurate for the unannealed sample, while the estimate using the profile measured at 350 °C yields good results at that annealing temperature. This suggests that the defect density profile changes with annealing: i.e. the divacancies migrate deeper into the substrate with annealing, thus producing larger overlap with the optical mode as was hypothesized with respect to Fig. 3.31. The formation of vacancy-related defects below the ion implantation

range has been reported by others [163, 164] and attributed to the formation of second-order defects after the diffusion of vacancies into the substrate.

Calculation of the optical absorption losses according to Eq. (3.36) with the same assumptions concerning damage profiles listed above yields an upper limit for absorption loss of 0.4 dB/cm for the unannealed sample implanted with the lowest dose.

## 3.6 Chapter summary

Using a combination of electrical DLTS and optical DLTS, the process by which low-dose ion-implanted silicon photodetectors detect wavelengths near 1550 nm has been shown to be dominated by a mid-band acceptor state with emission energy corresponding to that of the divacancy. The photoionization cross-section of this defect state was measured using a new technique referred to here as Equilibrium Capacitance Spectroscopy (ECS).

The optical loss and responsivity of waveguide-integrated devices was characterized with respect to annealing temperature and ion-implantation dose. Average trap concentration versus annealing temperature was measured and shown to correlate with the optical responsivity observed for the waveguide devices subjected to the same implantation and anneal steps. A constant-capacitance transient analysis was performed to estimate the defect concentration profile for one sample; the results suggest that the defect density is significant to depths well below the expected ion implantation range.

# Chapter 4

# Photodiode integration with a variable optical attenuator (VOA)

A prime motivation for the development of silicon photonics is the potential for integration of multiple devices on a single chip in a single process flow. With the defect-enhanced photodetector approach outlined in Chapter 1, a first step for such integration is the use of a photodiode optical tap monitor linked to a Variable Optical Attenuator (VOA) such that the output of the VOA can be actively controlled without the need for external optical-to-electrical conversion. An all-silicon approach to this goal holds the prospect of cost-saving advantages by the replacement of costly and time-consuming MBE growth steps with a single ion implantation step. Furthermore, if the ion implantation can be performed using standard implantation species used elsewhere in the process (e.g. phosphorus or boron) and at energies compatible with a single-stage ion implanter then the integrated device can be fabricated entirely in a standard CMOS fab without the need for unconventional fabrication steps.

# 4.1 Introduction

## 4.1.1 Integration of VOA and detection functionality

Waveguide integration of a VOA/modulator with a photodiode has recently been demonstrated using SiGe (silicon/germanium) photodiodes together with carrier-depletion modulators [165], ring-resonator modulators [166], and carrier injection modulators [167]. Integration of amplifiers (which can serve as variable output power elements in much the same manner as a VOA) and photodiodes fabricated via hybrid integration of III-V compounds have also been demonstrated [85]. However the integration of a photodiode with a VOA monolithically in silicon without either III-V or Germanium integration had not, prior to this work, been demonstrated. To further demonstrate the monitoring and control capability of such a device, this work includes operation of the integrated VOA/monitor as a channel leveller for wavelengths in the *C*-band (1530 nm – 1570 nm).

## 4.1.2 Dynamic optical channel equalization

Foremost among the possible applications of a VOA and photodiode integrated in a planar waveguide device in silicon is the dynamic optical channel equalizer. Spectral power variation in telecommunication links occurs due to amplifier spectral gain tilt and is often worsened by subsequent amplification stages. One solution to this problem is to compensate unequal gain distribution by using amplifiers with complementary gain spectra [168] or via attenuation using a filter tuned to match the gain spectrum [169]. However the power distribution between channels and of the overall link can fluctuate as a result of laser or amplifier drift and damage to the optical link. Accordingly a dynamic channel equalizer is useful after channel demultiplexing at the receiver end to level the power

distribution between individual channels and to mitigate power fluctuations in the overall optical link.

Dynamic optical channel equalizers of this nature have been reported using various architectures: MEMS-based [170], planar silica waveguide-based [171], and more recently using a defect-mediated photodetector with an external off-chip VOA [172]. It also has been suggested that the detection and attenuation functions can be integrated together with the electronic circuitry for a feedback loop on-chip and the fabrication process to achieve this has been reported [173].

In this work a defect-mediated photodetector was monolithically integrated with a thermo-optically tuned VOA. An external feedback loop implemented via software written in NI LabVIEW [151] was used to control the VOA from the photodiode to achieve dynamic channel equalization for wavelengths from 1530 nm to 1570 nm. This work was the first reported use of a defect-mediated photodiode integrated monolithically in silicon with a VOA to monitor and control the VOA output as well as the first demonstration of dynamic channel equalization via silicon photonic integration of both the attenuation and detection functions. Some of the work described in this chapter has been published in [174].

# 4.2 Theory

## 4.2.1 Mach-Zehnder Interferometer transfer function

The transfer function of a directional coupler was described in Chapter 2 and is given by Eq. (4.1).

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} t & jk \\ jk & t \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}. \tag{4.1}$$

If the directional coupler is cascaded in series via arbitrary phase shifts $\phi_1$, $\phi_2$ and with a second directional coupler (for simplicity we assume that this directional coupler is identical to the first) the overall structure is that shown in Fig. 4.1. This structure is a Mach-Zehnder Interferometer (MZI).

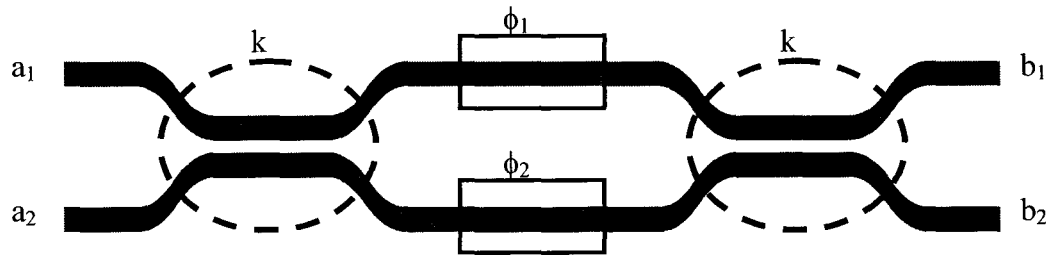


Fig. 4.1: Mach-Zehnder interferometer (MZI) structure showing cascaded directional couplers k, with inputs $a_1$, $a_2$, outputs $b_1$, $b_2$, and phase shifts $\phi_1$, $\phi_2$ between directional couplers.

Applying Eq. (4.1) for each directional coupler and phase shifts $\phi_1$, $\phi_2$ between the couplers, the overall transfer function of the MZI is given by Eq. (4.2):

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} t & jk \\ jk & t \end{pmatrix} \begin{pmatrix} e^{j\phi_1} & 0 \\ 0 & e^{j\phi_2} \end{pmatrix} \begin{pmatrix} t & jk \\ jk & t \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}. \tag{4.2}$$

The phase shifts $\phi_1$ and $\phi_2$ are given by Eq. (4.3)

$$\phi_i = \frac{2\pi L_i}{\lambda_0} n_{eff_i} \tag{4.3}$$

where $L_i$, $n_{eff\,i}$, are the physical length and effective index of each arm and $\lambda_0$ is the free-space wavelength.

Eq. (4.2) simplifies to Eq. (4.4):

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} t^2 e^{j\phi_1} - k^2 e^{j\phi_2} & jkt(e^{j\phi_1} + e^{j\phi_2}) \\ jkt(e^{j\phi_1} + e^{j\phi_2}) & t^2 e^{j\phi_2} - k^2 e^{j\phi_1} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{4.4}$$

which represents the general transfer matrix for a MZI composed of identical directional couplers with arbitrary optical path lengths within the interferometer.

Since phases $\phi_1$ and $\phi_2$ incurred between the two directional couplers are relative, we can consider both with reference to $\phi_1$ such that $\phi_1 = 0$ and $\phi_2 = \theta = \phi_2 - \phi_1$ without loss of generality, yielding Eq. (4.5):

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} t^2 - k^2 e^{j\theta} & jkt(1+e^{j\theta}) \\ jkt(1+e^{j\theta}) & t^2 e^{j\theta} - k^2 \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}. \tag{4.5}$$

For $a_2 = 0$ (as would generally be the case when the MZI is used as a VOA) and denoting $T = t^2$, $K = k^2$ we obtain Eq. (4.6) and Eq. (4.7) for $B_1$ and $B_2$, the "bar" and "cross" relative power outputs of the MZI respectively. Eq. (4.7) is the familiar fractional power coupling transfer function of an MZI.

$$B_1 = \left|\frac{b_1}{a_1}\right|^2 = T^2 + K^2 - 2KT\cos\theta \tag{4.6}$$

$$B_2 = \left|\frac{b_2}{a_1}\right|^2 = 2KT\left(1+\cos\theta\right) \tag{4.7}$$

It is noted that for negligible power lost within the directional couplers, $T = 1 - K$, and Eq. (4.6) and Eq. (4.7) yield $B_1 + B_2 = 1$ as expected.

### 4.2.2 MZI design considerations

It is evident from Eq. (4.6) and Eq. (4.7) that the relative cross-coupled power $B_2$ is maximized (and relative bar-coupled power $B_1$ is minimized) for $\theta = m(2\pi)$ where $m$ is an integer, yielding Eq. (4.8) for the minimum possible relative bar-coupled power

$$B_1(\min) = T^2 + K^2 - 2KT = (2K-1)^2 \tag{4.8}$$

and Eq. (4.9) for the maximum possible relative cross-coupled power.

$$B_2(\max) = 4K(1-K) \tag{4.9}$$

Simiarly, it is evident that maximum possible relative bar-coupled power $B_1 = 1$ and minimum possible relative cross-coupled output $B_2 = 0$ independent of $K$.

With $K = 0.5$, $B_2(max)$ has a maximum of 1 and $B_1(min)$ has a minimum of 0. However for $K \neq 0.5$, the maximum achievable relative cross-coupled power is less than 1, while the minimum achievable relative bar-coupled power is greater than 0. The contrast between "on" and "off" – i.e. the "extinction ratio", defined as the ratio of maximum output to minimum output – is therefore determined by $K$. For $K = 0.5$ unlimited extinction ratio (and thus variable attenuation) is theoretically possible, but extinction ratio degrades as $K$ deviates from this condition. Thus although MZI performance is independent of whether the bar-coupled or cross-coupled output is employed in a VOA for the ideal case of $K = 0.5$, realistic fabrication processes necessitate either reduced extinction ratio (for the bar-coupled output) or reduced maximum throughput (for the cross-coupled output) as $K$ varies from the targeted value of 0.5.

### 4.2.3 Tap Monitor Considerations

As noted in section 4.2.2, for negligible power loss within the device, $B_1 + B_2 = 1$ since total energy is conserved. Thus once $K$ for the MZI is known (e.g. by measuring $B_2(max)$ and using Eq. (4.9), a measurement of power at one output is sufficient to establish power at the other output as well. For a power monitor, therefore, which necessarily consumes some optical power in order to generate photocurrent, it may be advantageous to situate the power monitor on one output while using the other as the active output from the device. With this architecture, power can be tuned with active monitoring but without any excess loss in the output path from the tap monitor.

For a tap monitor with effective responsivity $R = i_{ph}P_n$ where $i_{ph}$ is photocurrent and $P_n$ is the optical power within the waveguide at the tap monitor (i.e. before

any optical power is tapped) then photocurrent as a function of tuning can be expressed as in Eq. (4.10):

$$i_{ph}(\theta) = R \cdot (B_n P_0). \tag{4.10}$$

where $B_n$ is the relative coupled power at output $n$ corresponding to the tap monitor and $P_0$ is the total input power. Then substituting $B_m = 1 - B_n$ where $B_m$ denotes the relative coupled power at output $m$ (i.e. the output without the tap monitor) and solving for $P_m = B_m P_0$ yields Eq. (4.11):

$$P_m = P_0 - \frac{i(\theta)}{R}. \tag{4.11}$$

Thus if, for example, the tap monitor is situated on the bar-coupled output path $b_1$ in Fig. 4.1, then from Eq. (4.7) and Eq. (4.11) one attains the following for photocurrent vs. tuning:

$$i_{ph}(\theta) = RP_0\left[1 - 2K(1-K)(1+\cos\theta)\right]. \tag{4.12}$$

### 4.2.4 Thermo-optic tuning

As described in Eq. (4.3) and Eq. (4.7), the relative optical power division between the two outputs of an MZI can be controlled by changing the optical path length of one arm relative to the other. For planar waveguide devices the physical length of the arms is generally fixed, but the effective index can be changed. One method for adjusting the effective refractive index of the waveguide is to employ the thermo-optic effect via a heat source situated near the waveguide. Silicon has a thermo-optic coefficient approximately equal to $1.79 \times 10^{-4}$ $K^{-1}$ for an optical free-space wavelength of 1550 nm [175], so for a typical interferometer arm length of 1 mm Eq. (4.3) suggests that complete switching (i.e. relative phase-shift $\theta = \pi$) is achievable with $\Delta T$ of less than 5° C. The tuneable heat source can be a resistor composed of a thin slab of metal traversing the waveguide. A

voltage drop applied across the resistor produces current flow and heat dissipation in the form of $i^2R$ losses (where $i$ is current and $R$ is resistance).

### 4.2.5 Mathematical Equivalence of Thermal to Electrical Parameters

In a simple thermal tuning mechanism, thermal energy is injected from the a heat source into a region of interest (e.g. the waveguide) and dissipates to a heat sink (e.g. the substrate). The equation governing thermal energy flow is Fourier's Law:

$$\mathbf{q} = -k\nabla T . \tag{4.13}$$

where $\mathbf{q}$ is thermal energy flux, $k$ is the thermal conductivity, and $T$ is temperature. Recalling Ohm's Law:

$$\mathbf{J} = \sigma\mathbf{E} \tag{4.14}$$

where $\mathbf{J}$ is current density, $\sigma$ is conductivity, and $\mathbf{E}$ is electric field, and substituting

$$\mathbf{E} = -\nabla V \tag{4.15}$$

where $V$ is voltage we get the familiar relation between current and voltage:

$$\mathbf{J} = -\sigma\nabla V . \tag{4.16}$$

It is evident by comparing Eq. (4.16) to Eq. (4.13) that heat flow is analogous to current flow with temperature the analogue of voltage, thermal energy the analogue of charge, thermal energy flux the analogue of current, and thermal conductance the analogue of electrical conductance. Electrical capacitance (the ratio of stored charge to voltage of a component) is analogous to thermal capacity (the ratio of stored thermal energy to temperature of a component).

It is well known that this mathematical equivalence between electrical current flow and thermal energy flow can be used to advantage by applying standard circuit theory to simple thermal models, as has been used to model electrical interconnects (e.g. [176]). It is used here to produce a useful lumped-element circuit model for thermo-optic tuning.

### 4.2.6 Thermal Circuit Model

A typical thermo-optic tuning configuration for SOI rib waveguides (as described in Chapter 1) is shown in Fig. 4.2 overlaid with its equivalent thermal circuit.

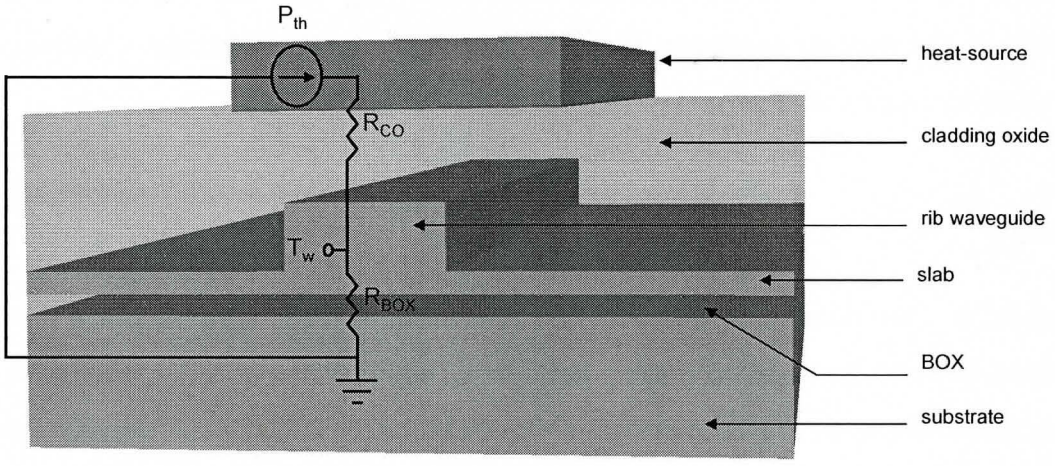


Fig. 4.2: Representative thermo-optic tuning configuration in SOI showing heat-source resistor, cladding oxide, rib waveguide, buried oxide and substrate with equivalent thermal circuit. $P_{th}$ = thermal power, $T_w$ = temperature at the waveguide, $R_{CO}$ = thermal resistance of the cladding oxide, $R_{BOX}$ = thermal resistance of the buried oxide.

For simplicity we assume that thermal radiative losses to the air are negligible compared to heat dissipated to thermal ground through the device. Then the heat-source resistor provides $P = i^2R$ thermal power to the circuit through the cladding oxide, which acts as a thermal resistor. The rib waveguide acts as another thermal resistor, but since the thermal resistance of silicon is approximately two orders of magnitude lower than that of oxide it can be neglected. The BOX acts as a thermal resistor between the waveguide and the substrate. The substrate is

effectively at thermal ground (i.e. room temperature) since it is large compared to the waveguide, relatively thermally conductive in comparison to the oxide, and presumed to be in good thermal contact with other heat sinks beneath it (e.g. the fixture on which it is mounted).

From the circuit shown in Fig. 4.2 it is evident that $T_w$ is independent of the cladding oxide resistance - assuming that the cladding oxide is relatively thin such that there are no leakage paths that would allow significant thermal power to bypass the waveguide - and is given by Eq. (4.17)

$$T_w = P_{th} R_{BOX} \tag{4.17}$$

where $P_{th}$ is the thermal power dissipated into the chip from the heat source and $R_{BOX}$ is the thermal resistance from the waveguide to the substrate. Thermal resistance in general is given by

$$R = \frac{1}{\sigma\left(A/d\right)} \tag{4.18}$$

where $\sigma$ is the thermal conductivity of the material, $A$ is the cross-sectional area through which the thermal energy must flow, and $d$ is the distance across the thermal resistance. Since, according to Eq. (4.18), $R_{BOX}$ in Eq. (4.17) depends on the area of the BOX through which thermal power dissipates to the substrate, our analysis must also take into account lateral power flow outward along the silicon slab. The slab, with much higher material thermal conductivity than the oxide, effectively spreads the heat over a wider area for dissipation through the BOX. Thus area $A$ in Eq. (4.18) is larger than the area beneath the heat source. If the region of interest on the slab (e.g. the rib waveguide) is not centred beneath the heat source, temperature $T_w$ in Eq. (4.17) becomes a decreasing function of $x$ where $x$ is the lateral distance from the heat source. A schematic of the heat flux from source to substrate for the configuration described above is shown in Fig. 4.3.

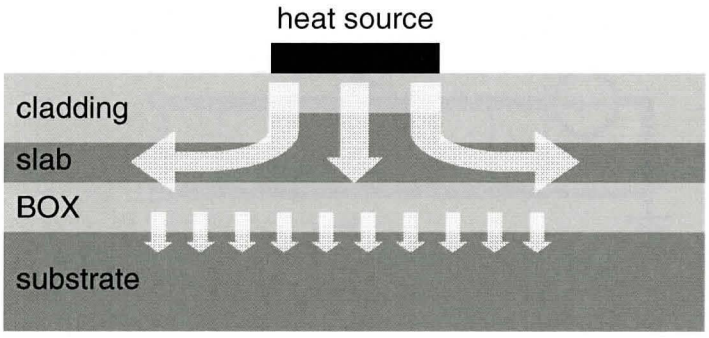


Fig. 4.3: Schematic of heat flux (shown with yellow arrows) from source to substrate through oxide (cladding oxide and BOX) through an intervening silicon slab. Since the slab has much higher thermal conductivity than the oxide, lateral flux along the slab results in a larger cross-sectional area for flux through the BOX than through the cladding oxide.

### 4.2.7 Derivation of temperature as a function of lateral distance along the SOI slab

Continuing the analogy between electrical current and thermal flux established above, the slab can be treated mathematically using the standard distributed model of a transmission line. Ordinarily such a treatment would include capacitance and inductance elements, but for a steady state model these can be ignored and the system may be modeled as a network of resistors. The equivalent circuit diagram is shown in Fig. 4.4.

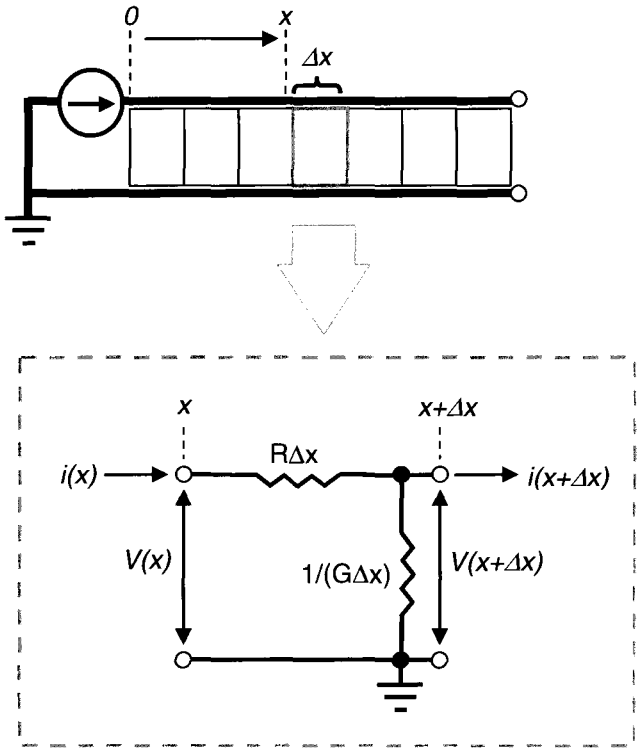


Fig. 4.4: Distributed element transmission line equivalent circuit for heat dissipation through silicon slab and BOX. Each element Δx incorporates a series RΔx resistance and shunt GΔx conductance.

The series distributed element resistance $R\Delta x$ is the thermal resistance of the slab over length $\Delta x$; the shunt distributed element conductance $G\Delta x$ is the thermal conductance of the BOX over slab width $\Delta x$.

From the circuit element in Fig. 4.4, the voltage and current drop across the element are given by Eq. (4.19) and Eq. (4.20) respectively.

$$V(x) - V(x+\Delta x) = i(x) \cdot R\Delta x \tag{4.19}$$

$$i(x) - i(x+\Delta x) = V(x+\Delta x) \cdot G\Delta x \tag{4.20}$$

Then taking the limit as $\Delta x \rightarrow 0$,

$$\frac{dV(x)}{dx} = -R \cdot i(x) \tag{4.21}$$

$$\frac{di(x)}{dx} = -GV(x) \tag{4.22}$$

and taking the derivative of both sides yields

$$\frac{d^2V(x)}{dx^2} = (GR)V(x) \tag{4.23}$$

$$\frac{d^2i(x)}{dx^2} = (GR)i(x). \tag{4.24}$$

The similarity to waveguide electromagnetic theory described in Chapter 2 is apparent.

Considering the general solutions to Eq. (4.23) and Eq. (4.24)

$$V(x) = a_1e^{-kx} + a_2e^{kx} + a_3 \tag{4.25}$$

$$i(x) = b_1e^{-kx} + b_2e^{kx} + b_3 \tag{4.26}$$

and it is immediately evident that $a_2$, $a_3$, $b_2$ and $b_3$ must be zero since both current and voltage (i.e. energy flux and temperature) must vanish as $x \rightarrow \infty$. Accordingly, dropping the subscripts on the coefficients provides

$$V(x) = ae^{-k|x|} \tag{4.27}$$

$$i(x) = be^{-k|x|} \tag{4.28}$$

and from Eq. (4.23) and Eq. (4.24) we have $k = \sqrt{GR}$.

Then substituting Eq. (4.27) into Eq. (4.21) one may solve for coefficient $b$ to get

$$b = \sqrt{\frac{G}{R}}a. \tag{4.29}$$

Denoting $x = 0$ at the centre of the heat source, $x = x_1$ and $x = -x_1$ at the edges of the source, and $i_0$ as the current flow through the BOX for $-x_1 < x < x_1$, then

$$i_0 + i(x_1) + i(-x_1) = I \tag{4.30}$$

where $I$ is total current injected into the system from the source. Treating the source resistor as a bulk element for simplicity (i.e. ignoring lateral thermal variation in the region directly beneath the source resistor) one may obtain

$$i_0 = G \cdot 2x_1 \cdot V(x_1). \tag{4.31}$$

By the symmetry of the problem, $i(x_1) = i(-x_1)$ and so substituting Eq. (4.31), Eq. (4.28), and Eq. (4.29) into Eq. (4.30) and solving for coefficient $a$ one obtains

$$a = I \frac{e^{kx_1}}{2\left(\sqrt{G/R} + Gx_1\right)}. \tag{4.32}$$

Therefore for a silicon slab of thickness $t_s$, a BOX layer of thickness $t_B$, overall device length $L$, and material thermal conductivities $\sigma_s$ and $\sigma_B$ for the silicon and oxide respectively, $R$ and $G$ are defined by

$$R = \left[\sigma_s t_s L\right]^{-1} \tag{4.33}$$

$$G = \sigma_B L / t_B \tag{4.34}$$

and so re-expressing Eq. (4.27) in terms of temperature $T$ and thermal power $P_{th}$ instead of $V$ and $I$ one obtains the solution for temperature change relative to ambient in the slab as a function of position:

$$T(x) = \frac{P_{th}}{2\left(\sqrt{\frac{\sigma_s \sigma_B t_s L^2}{t_B}} + \frac{\sigma_B L}{t_B} x_1\right)} e^{-k(|x|-x_1)}. \tag{4.35}$$

### 4.2.8 Thermo-optical phase shift

Temperature change $T(x)$ in the waveguide induces optical refractive index change $\Delta n$ according to Eq. (4.36)

$$\Delta n(x) = \frac{dn}{dT} T(x) \tag{4.36}$$

where *dn/dT* is specific to the material, wavelength, and temperature. The solution for refractive index change at the waveguide is therefore given by

$$\Delta n(x) = \frac{dn}{dT} \frac{P_{th}}{2\left(\sqrt{\frac{\sigma_s \sigma_B t_s L^2}{t_B}} + \frac{\sigma_B L}{t_B} x_1\right)} e^{-k(|x|-x_1)} \tag{4.37}$$

which can be used to calculate the modal effective index based on the material refractive index changes induced in the core and the cladding of the waveguide.

Substituting Eq. (4.37) into Eq. (4.3), total phase shift $\Delta\phi = \theta$ can be calculated according to Eq. (4.38)

$$\theta = \frac{2\pi L}{\lambda_0} \frac{dn}{dT} \frac{P_{th}}{2\left(\sqrt{\frac{\sigma_s \sigma_B t_s L^2}{t_B}} + \frac{\sigma_B L}{t_B} x_1\right)} e^{-k(|x|-x_1)} \tag{4.38}$$

which simplifies to

$$\theta = \frac{2\pi}{\lambda_0} \frac{dn}{dT} \frac{P_{th}}{2\left(\sqrt{\frac{\sigma_s \sigma_B t_s}{t_B}} + \frac{\sigma_B}{t_B} x_1\right)} e^{-k(|x|-x_1)}. \tag{4.39}$$

It is worth noting the rather remarkable result seen here that tuning efficiency (i.e. phase shift $\theta$ induced for injected thermal power $P_{th}$) is in principle independent of tuner length $L$. However in practice this will not be absolutely correct since the injected thermal power depends on the resistance of the tuner, and hence its length.

### 4.2.9 Thermo-optic tuning speed

The derivations thus far have been confined to steady-state conditions and have therefore neglected thermal capacitance in the thermal circuit model. In principle a full treatment would entail replacing the resistances $R\Delta x$ and $1/(G\Delta x)$ in the equivalent circuit of Fig. 4.4 with complex impedances $Z_s\Delta x$ and $1/(Y\Delta x)$ by taking into account the thermal capacitances of the slab and the oxide respectively. Then the equivalent circuit is as shown in Fig. 4.5.

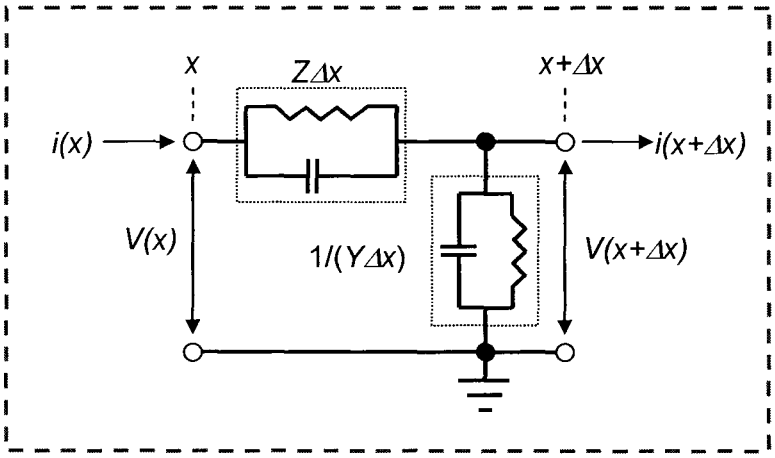


Fig. 4.5: Distributed element transmission line equivalent circuit incorporating time-dependence for heat disspation through silicon slab and BOX. Each element Δx incorporates a series impedance $Z\Delta x$ and shunt admittance $Y\Delta x$.

Calculating the series impedance $Z\Delta x$ in terms of the silicon slab one obtains:

$$Z\Delta x = \left[\frac{\sigma_s t_s L}{\Delta x} + j\omega C_s t_s L\Delta x\right]^{-1} \tag{4.40}$$

$$Z\Delta x = \frac{\Delta x}{\sigma_s t_s L + \omega C_s t_s L\Delta x^2} \tag{4.41}$$

where $C_s$ is the heat capacity of silicon.

Similarly, the shunt admittance $Y\Delta x$ is given by Eq. (4.42) and Eq. (4.43):

$$Y\Delta x = \frac{\sigma_B L\Delta x}{t_B} + j\omega C_B L t_B \Delta x \tag{4.42}$$

$$Y\Delta x = L\left(\frac{\sigma_B}{t_B} + j\omega C_B t_B\right)\Delta x \tag{4.43}$$

where $C_B$ is the heat capacity of silicon dioxide.

Repeating the analysis of section 4.2.7 while substituting $Z\Delta x$, $Y\Delta x$ for $R\Delta x$, $G\Delta x$ yields

$$V(x) - V(x+\Delta x) = i(x)\cdot Z\Delta x \tag{4.44}$$

$$\frac{V(x) - V(x+\Delta x)}{\Delta x} = \frac{i(x)}{\sigma_s t_s L + j\omega C_s t_s L\Delta x^2} \tag{4.45}$$

$$\frac{dV}{dx} = -\left(\frac{1}{\sigma_s t_s L}\right) i(x) \tag{4.46}$$

for voltage (the imaginary term in the denominator vanishes in the limit $\Delta x \rightarrow 0$). It is noteworthy that this is identical to Eq. (4.21), and thus $Z\Delta x = R\Delta x$, i.e. the heat capacity of the silicon slab does not contribute any frequency dependence to the system. This somewhat remarkable result simplifies the calculation considerably.

For current one obtains

$$i(x) - i(x+\Delta x) = V(x+\Delta x)\cdot Y\Delta x \tag{4.47}$$

$$i(x) - i(x+\Delta x) = V(x+\Delta x)\cdot L\left(\frac{\sigma_B}{t_B} + j\omega C_B t_B\right)\Delta x \tag{4.48}$$

$$\frac{di}{dx} = -L\left(\frac{\sigma_B}{t_B} + j\omega C_B t_B\right) V(x)\,. \tag{4.49}$$

Then solving as before (p. 142) provides a solution for temperature change relative to ambient in the slab as a function of position and frequency given by Eq. (4.50).

$$T(x) = \frac{P_{th}}{2\left(\sqrt{\frac{\left(\sigma_B + j\omega C_B {t_B}^2\right)\sigma_s t_s L^2}{t_B}} + L\left(\frac{\sigma_B}{t_B} + j\omega C_B t_B\right)x_1\right)} e^{-k(|x|-x_1)} \quad (4.50)$$

A comparison of Eq. (4.50) and Eq. (4.35) together with Eq. (4.33) and Eq. (4.43) shows that the two expressions for $T(x)$ are identical except that $G$ has been replaced with $Y$ in Eq. (4.50).

Eq. (4.50) can be solved numerically to yield the frequency dependence of thermal tuning efficiency, but the problem can be addressed analytically by taking advantage of the fact that the heat capacity of the silicon slab plays no role in the frequency dependence of the device as shown in Eq. (4.46) and Eq. (4.50). All thermal "capacitance" is due to the shunt admittance of the buried oxide. Accordingly the system shown in Fig. 4.5 may be simplified to the equivalent circuit shown in Fig. 4.6.

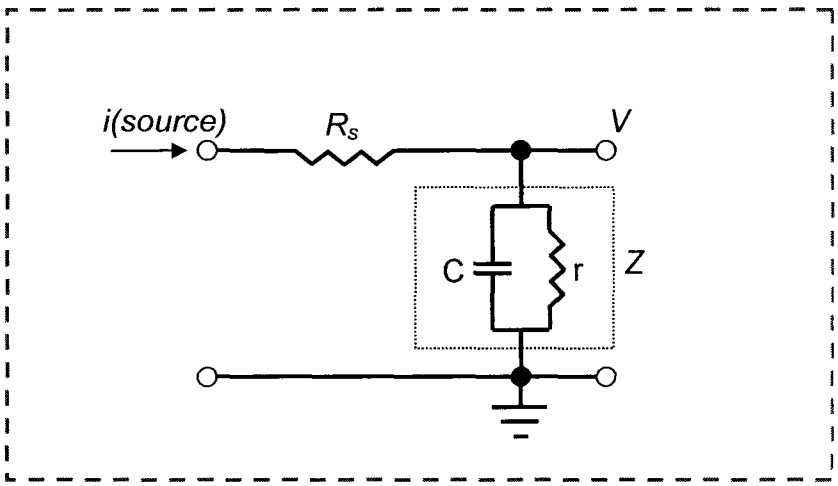


Fig. 4.6: Lumped-element equivalent thermal circuit of the thermal tuning system. The transmission line equivalent has been replaced by an overall thermal resistance between the source and the region of interest, and an overall thermal impedance between the region of interest and thermal ground.

It is apparent from Fig. 4.6 that $V = i\,Z$, that $Z = r\,(1 + j\omega rC)^{-1}$, and that the frequency response of the system is determined by the time constant $\tau = rC$.

Reverting to the thermal characteristics corresponding to the above electrical variables gives $C = \frac{1}{2} C_B t_B A$ and $r = t_B / (\sigma_B A)$ where $C_B$ is the volumetric heat capacity of silica, $t_B$ is the thickness of the buried oxide, $A$ is the effective area over which thermal power is dissipated to the substrate, and $\sigma_B$ is the thermal conductivity of silica. The factor of ½ in the expression for $C$ is because the buried oxide is grounded to the substrate, and hence has a linear temperature drop across it such that its average temperature (and hence total heat capacity) is halved. The effective area $A$ over which thermal power is dissipated is an unknown – hence necessitating the transmission line analysis used above for derivations of actual efficiency. However, the thermal efficiency (defined here as temperature change in the waveguide per unit of injected thermal power) relative to the thermal efficiency at zero frequency is given by Eq. (4.51)

$$\frac{\eta(\omega)}{\eta(0)} = \left|\frac{Z(\omega)}{Z(0)}\right| = \frac{1}{\sqrt{1+(\omega r C)^2}} \tag{4.51}$$

or

$$\frac{\eta(\omega)}{\eta(0)} = \frac{1}{\sqrt{1+(\omega C_B t_B^{\,2} / 2\sigma_B)^2}} \tag{4.52}$$

The frequency at which relative thermal efficiency drops by half is given by Eq. (4.53)

$$f_{1/2} = \frac{\sqrt{3}}{2\pi r C} = \frac{\sqrt{3}\sigma_B}{\pi t_B^{\,2} C_B} \tag{4.53}$$

and is independent of $A$. Eq. (4.52) and Eq. (4.53) therefore yield a simple analytical means of calculating the thermal tuning bandwidth of the VOA.

# 4.3 Device design

## 4.3.1 Waveguide geometry

The waveguides were designed to be comparable to the wire waveguides described by Van Laere et al. [23] so as to take advantage of the same grating coupling architecture. Additionally, the high local confinement of this structure permits small bend radii without excessive attenuation as described in Chapter 2.

In order to situate a *p-i-n* diode straddling the waveguide, however, it is necessary to leave some silicon on either side of the rib; accordingly the rib was designed to leave a 50 nm slab of silicon above the buried oxide. The silicon overlayer thickness was chosen to be 220 nm thick, and a rib width of 500 nm (again, matching Van Laere et al. [23]) was chosen. The BOX was 2 μm thick for these wafers.

Simlations using RSoft BeamPROP for these waveguide dimensions suggest that the waveguide supports only one TE-polarized mode, thus allowing single-mode operation since as described in Chapter 2, the grating couplers used for fiber input to the chip select either TE or TM polarization depending on the angle of the fiber. Considerations are restricted to TE for the remainder of this work.

## 4.3.2 Directional couplers

As shown in Section 4.2.2, the optimal MZI extinction ratio is achieved for directional coupling $K = 0.5$. A directional coupler length of 100 μm was arbitrarily chosen, and simulations of coupling as a function of waveguide spacing

and wavelength were used to explore the parameter-space. These results are shown in Fig. 4.7.

From the simulated K values the ideal gap spacing was shown to be between 0.45 and 0.5 μm. Both 0.45 and 0.5 μm gaps were used in the design of directional couplers drawn on the photomask with the understanding that there would be additional variation due to the photolithographical exposure across the wafer (exposure and thus final device dimension was deliberately swept from 16.5 mJ to 25.5 mJ as described further in section 4.4). In testing of both devices it was found that the nominal 0.5 μm gap devices were unusually lossy (a problem seen with repeatability for many devices on the chip and attributed to errors in the grating and taper mask layers). Therefore the 0.45 μm gap (nominal) devices from the highest-exposure (i.e. larger than designed gap) area of the wafer were used.

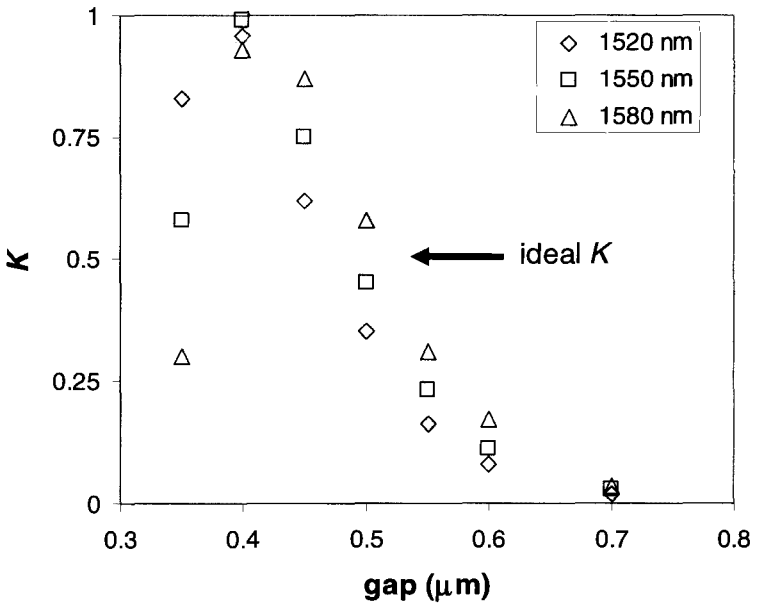


Fig. 4.7: Simulated coupling K for 100 μm length directional coupler for varous gap widths at 1520 nm, 1550 nm, and 1580 nm wavelengths. Rib dimensions are 0.5 μm wide, 220 nm SOI etched 170 nm, 2 μm BOX and 400 nm cladding oxide.

### 4.3.3 Photodiode doping regions

The *p-i-n* photodiode on one of the output arms of the MZI must be designed such that highly doped *p* and *n* regions are as close to the rib as possible while maintaining minimal overlap with the optical mode. Unnecessary separation of the p and n regions increases the reverse bias required to fully deplete the rib waveguide, thus reducing photocurrent as described in Chapter 3, while significant overlap of the optical mode with highly doped regions introduces prohibitive optical attenuation via free carrier absorption according to the Drude-Lorenz equation [45]. For example, for typical electron doping concentrations of $2\times10^{19}$ $cm^{-3}$, absorption coefficient $\Delta\alpha \cong 60$ which suggests attenuation of 260 dB/cm so it is imperative that the doped regions be far enough from the mode to ensure negligible overlap.

The BeamPROP solution for the TE mode at 1550 nm is shown in Fig. 4.8 for the waveguides used in this work. From the plot it is clear that the tail of the mode extends to at least 500 nm from the centre, or 250 nm from the edge of the rib.

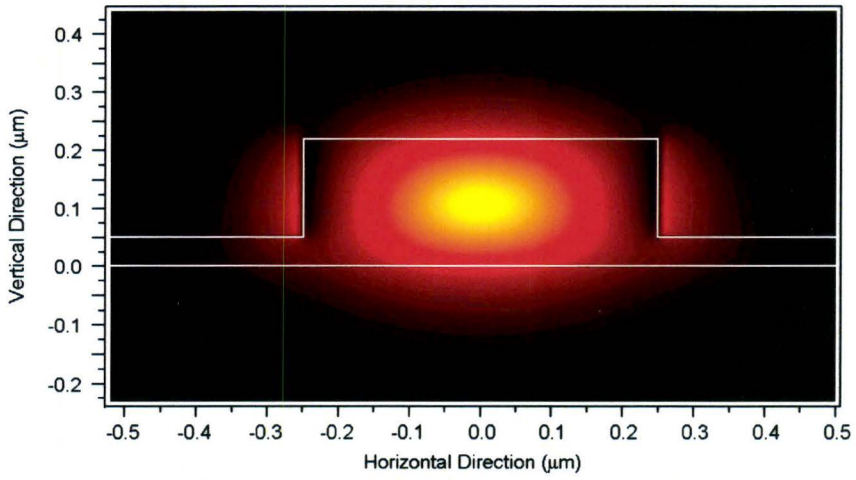


Fig. 4.8: Modal intensity distribution for TE polarization at 1550 nm. White outline indicates the silicon rib.

A software algorithm was written in Microsoft Visual Basic [177] to calculate the integral of mode power propagating in the slab as a function of distance from the

rib by parsing the BeamPROP mode amplitude distribution files at three representative wavelengths, Fig. 4.9 shows the result of this calculation.

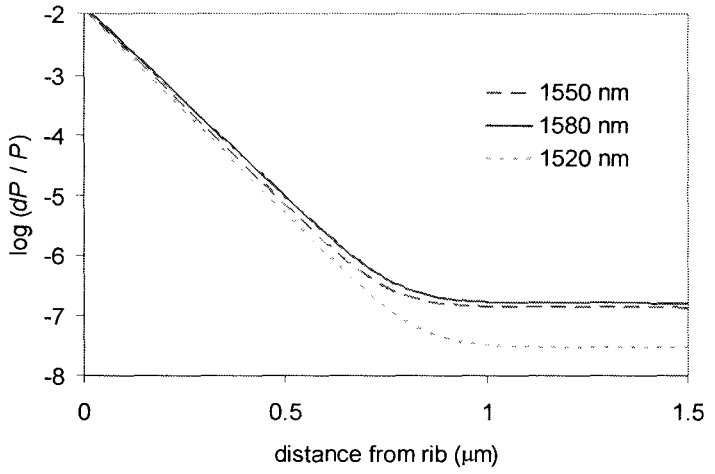


Fig. 4.9: Total fraction of mode power propagating in the slab as a function of distance from the rib.

From Fig. 4.9 it is evident that beyond approximately 0.75 μm from the edge of the rib, the optical power in the slab is equivalent to 'background noise' for the entire wavelength range of interest, and total power propagating in the slab beyond this distance is less than $10^{-6}$ of total waveguide power. Accordingly a doping separation of 0.75 μm from the waveguide was used.

### 4.3.4 Photodiode defect implantation

For the SOI configuration described in Section 4.3.1 (220 nm SOI etched 170 nm to form the rib waveguide) it is possible to implant small mass ions (i.e. ions smaller than the mass of silicon ions) such that the end of range lies within the buried oxide even for energies achievable in a single-stage ion implanter. This provides two advantages: (a) the ion species can be chosen nearly arbitrarily since only collision damage rather than the dopant species itself will remain in the waveguide, and (b) collision damage can be distributed across the entire

waveguide cross-section, thus enabling 100% overlap between the optical mode and the region containing a high density of optically active defects. Accordingly boron was chosen for the implantation species in order to achieve high range at low energy without resorting to exotic implantation species. The highest implant energy available from LETI (350 keV) was used to assure the end-of-range of the boron was below the silicon overlayer.

Implantation range simulations using the software package SRIM [150] suggest that the average damage density for these implant parameters is 0.045 per Angstrom-ion, whereas for the silicon ion implants performed on the Kotura devices described in Chapter 3, SRIM simulations indicated average damage density of 0.55 per Angstrom-ion to a depth of 1 μm below the upper surface of the 4 μm SOI, or 5% overlap with the optical mode. Accordingly for an implantation dose of $1 \times 10^{13}$ $cm^{-2}$ with 350 keV energy, one would expect (by the CBK equation) a seven-fold increase of the defect density in the LETI waveguide relative to the Kotura waveguide. Calculations of optical absorption loss using these values and the optical cross-section estimated in Chapter 3 yields a value of 120 dB/cm.

A dose of $1 \times 10^{13}$ $cm^{-2}$ was therefore chosen to provide approximately 10 dB defect induced absorption for a typical photodiode length of 1 mm such that most of the optical input is absorbed for high responsivity, but the loss is not so high that it cannot be accurately characterized. It is worth noting that additional photodiode length beyond 10 dB defect-induced loss provides very little additional photocurrent since most of the optical signal has already been absorbed.

### 4.3.5 Thermo-optic tuners

From Fig. 4.8 it is evident that the mode extends several hundred nanometres into the cladding oxide above the rib. The cladding oxide was limited in thickness to 400 nm due to restrictions presented by the fabrication facility (LETI) for this particular device fabrication run. Situating the heat-source resistor (or "tuner") directly above the waveguide as in Fig. 4.2 therefore risks attenuation due to possible overlap between the metal and the optical mode. Accordingly a separation of 2 μm was chosen between the waveguide and the edge of the rib. In order to avoid asymmetric heating effects a second resistor was positioned on the opposite side of the waveguide such that thermal energy from the resistors symmetrically heated the slab next to the rib. The relatively high thermal conductance of the slab enables conveyance of heat to the rib according to Eq. (4.35) and Eq. (4.50). The tuning configuration is shown in Fig. 4.10.

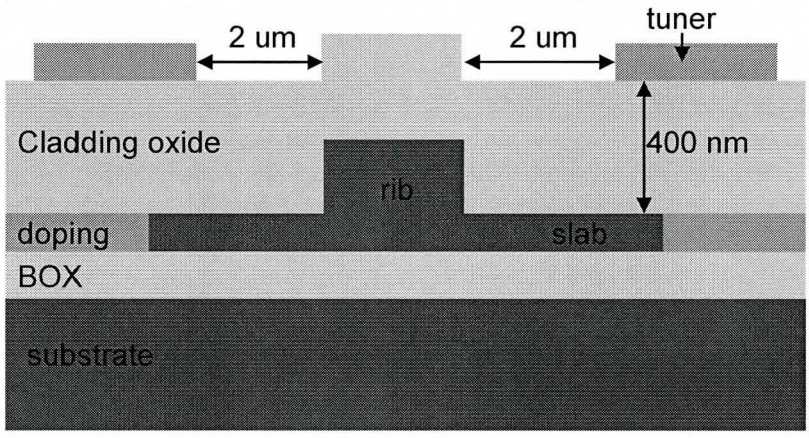


Fig. 4.10: Layout of the thermo-optic resistors on either side of the rib to avoid attenuation from metal proximity.

As was shown in Eq. (4.39) the tuning efficiency is (to first order) independent of length except for the dependence of injected thermal power on tuner resistance – higher tuner resistance will dissipate more thermal power into the system relative to other resistance elements in series with the tuner such as the electrical

connection between probe tips and the contact pad. A tuner length of 0.8 mm was chosen to fit easily on the chip.

### 4.3.6 Integrated device

A schematic of the overall device design incorporating both the tunable MZI VOA and a photodiode tap monitor is shown in Fig. 4.11.

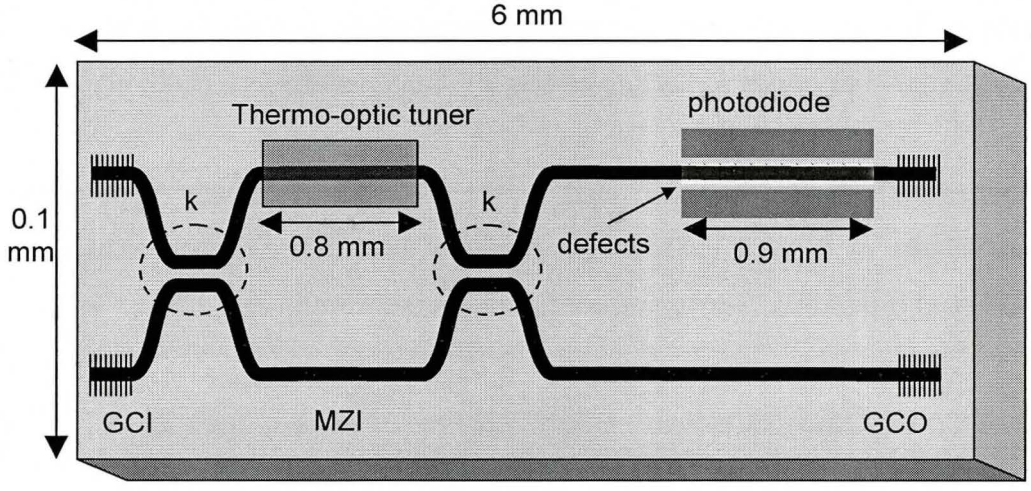


Fig. 4.11: Schematic of integrated VOA and defect-enhanced photodiode. Couplers *k* have length 100 μm and gap 0.45 μm. Separation between input waveguides is 50 μm centre-centre. GCI = grating-coupled input. GCO = grating-coupled output.

## 4.4 Fabrication process

The devices were fabricated at LETI as part of the ePIXFab 2009 shuttle run [178] using the following fabrication steps:

(1) Starting material was 220 nm SOI with 2 μm buried oxide (BOX).

(2) Waveguide features were defined in photoresist using a photomask and 193 nm optical exposure. The exposure dose was adjusted from 16.5 ± 0.3 mJ to 25.5 ± 0.3 mJ in 0.3 mJ increments from the "west" side to the "east" side of the wafer to achieve a range of feature sizes. Critical dimension gaps between waveguides with a nominal width of 200 nm had measured widths

ranging from 166.7 nm to 234.7 nm across the wafer, while standalone ribs (nominal width 500 nm) had measured widths ranging from 549 nm to 487 nm. The gratings were etched separately to a depth of 70 nm.

(3) Exposed silicon was etched to a depth of 170 nm and the remaining photoresist was removed.

(4) *p-type* dopant windows were defined in photoresist and boron was implanted with an energy of 5 keV and a dose of $1 \times 10^{14}$ $cm^{-2}$, after which the remaining photoresist was removed.

(5) *n-type* dopant windows were defined in photoresist and phosphorus was implanted at an energy of 5 keV and dose of $1 \times 10^{14}$ $cm^{-2}$, after which the remaining photoresist was removed.

(6) The wafer was annealed using a rapid thermal annealer at 1000° C for 100 seconds under nitrogen to activate the dopant.

(7) A cladding oxide layer was sputtered onto the wafer to a thickness of 400 nm.

(8) Contact vias were defined in photoresist and etched in the oxide cladding.

(9) Metal was deposited: 30 nm Ti, 60 nm TiN, 440 nm AlCu, 10 nm Ti, 40 nm TiN.

(10) Metal features were defined in photoresist and etched.

(11) Defect implantation windows were defined in photoresist and boron was implanted with an energy of 350 keV and dose of $1 \times 10^{13}$ $cm^{-2}$.

(12) The wafer was diced into 24 mm x 24 mm blocks such that each block contained sixteen identical chips.

Two wafers were processed: one with the defect implantation step (step 11) and one without for comparison.

# 4.5 Integrated VOA / Photodiode Characterization

## 4.5.1 Test setup

Light was coupled into the device using standard singlemode fiber (SMF) angled at 10 degrees from the surface normal of the chip and aligned to the grating as shown in Fig. 4.12.

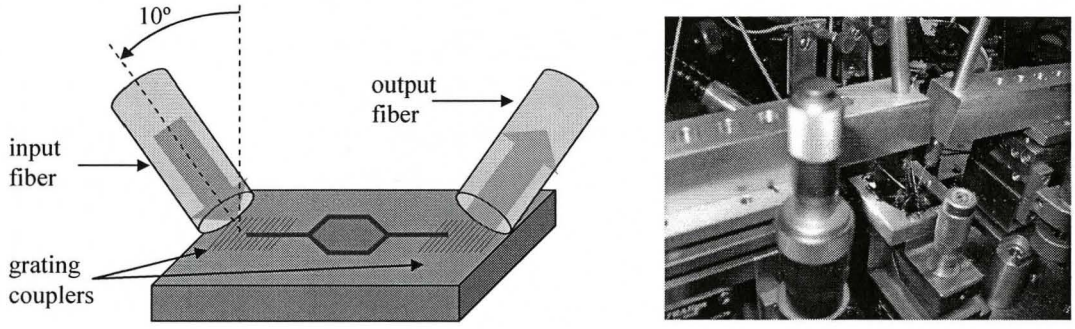


Fig. 4.12: Diagram showing input and output fiber coupling configuration (left) and photograph of corresponding setup (right).

A schematic of the test setup used to characterize the device is shown in Fig. 4.13.

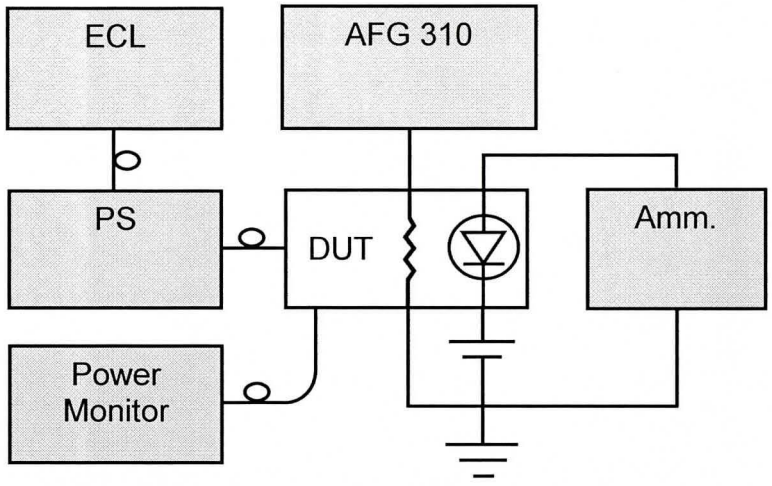


Fig. 4.13: Test setup used to characterize the monitored VOA. ECL = external cavity laser; PS = polarization scrambler; Amm = picoammeter; DUT = device under test. The DUT is shown as a resistor (the thermal tuner) and a diode (the photodetector).

### 4.5.2 Variable attenuation

Grating coupler losses were expected to be 6 dB [23] with additional 3 dB polarization dependent loss since the gratings couple only TE. It should be noted however that the difference in the grating etch depth (70 nm for this work versus 50 nm in [23]) affects the validity of this estimate. Propagation losses were estimated to be 0.24 dB/mm [179] for a coupler-to-coupler length of 3.8 mm although the etch depth (170 nm in this work versus 220 nm in [23]) may affect the validity of this estimate as well. Measurements on test straight waveguides yielded a fibre-fibre insertion loss of 15.5 ± 0.7 dB at 1550 nm wavelength as shown in Fig. 4.14, which corresponds to and justifies the grating and propagation loss estimates (15.8 dB total) listed above.

Fig. 4.15 shows the optical output from both the X and BAR paths of the VOA (without traversing the photodiode) as a function of thermal tuning power for an unpolarized optical input of -5 dBm. The maximum output (-24 dBm) for this device therefore suggests at least an additional 3 dB excess loss either at the gratings or from bend and coupler losses within the Mach Zehnder.

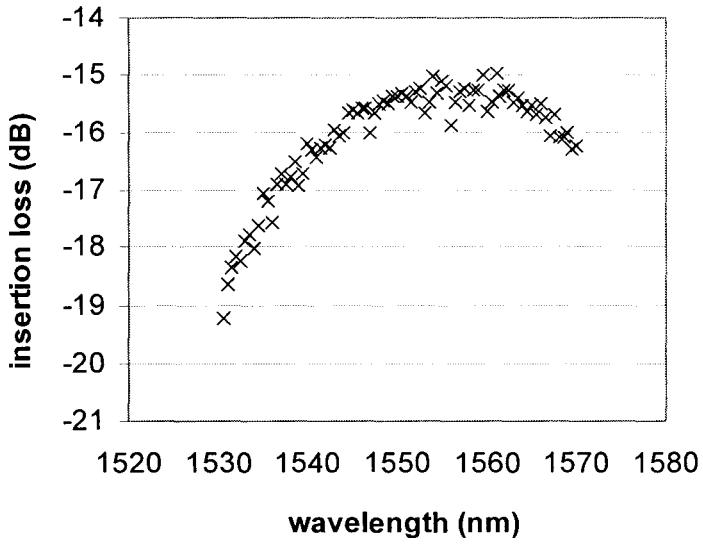


Fig. 4.14: Measured fibre-fibre insertion loss of a test straight waveguide, including grating and propagation losses.

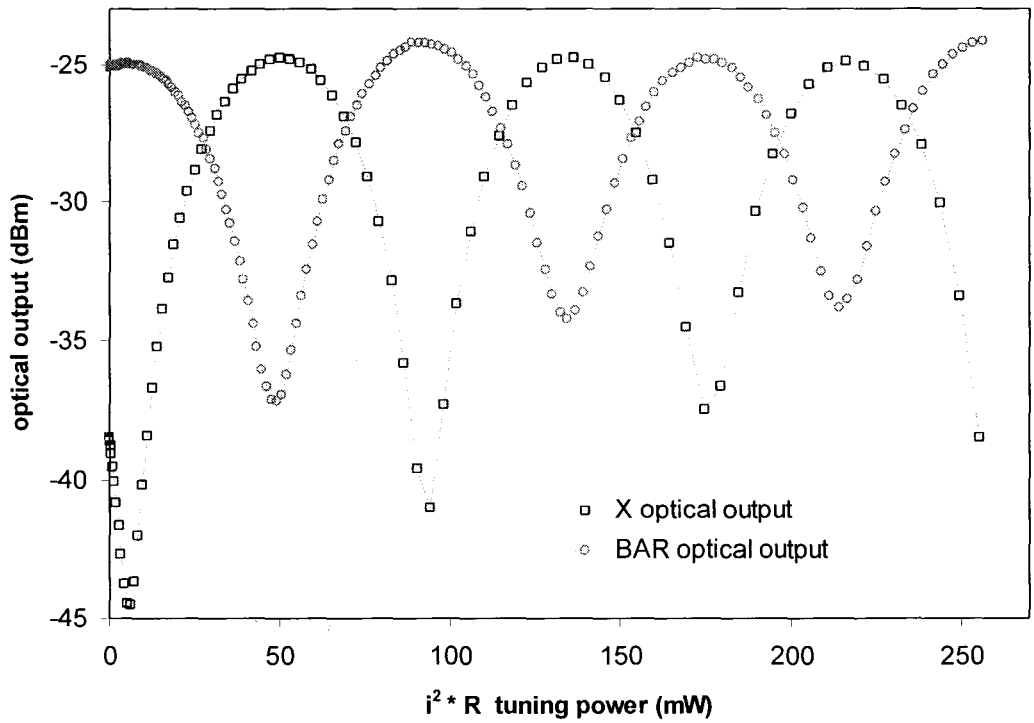


Fig. 4.15: Optical power output from the variable optical attenuator at the X and BAR outputs respectively as a function of thermal tuning power. Optical input power was -5 dBm (unpolarized) at 1550 nm wavelength.

As predicted in Eq. (4.6) and Eq. (4.7) the output of each arm (BAR and X) is a sinusoid with highest maximum transmission along the BAR path and highest extinction ratio along the X path. The variation of extinction ratio with thermal tuning is assumed to be due to variation in the coupler $k$ values due to heating at higher power dissipation. For low thermal power the extinction ratio is seen to be 20 dB for the X path and 12 dB for the BAR path. Thermal tuning power is calculated from Eq. (4.54):

$$P_{tuner} = (V_s - iZ_s)i \tag{4.54}$$

where $P_{tuner}$ is the thermal power dissipated in the tuner, $V_s$ is the nominal source voltage, $i$ is the measured current, and $Z_s$ is the source impedance (50 Ω for the Tektronix AFG 310 function generator used in this measurement).

Fig. 4.16 shows measured extinction ratio and calculated $K$ versus wavelength together with expected extinction ratio and $K$ ranges from BeamPROP waveguide simulations accounting for processing tolerances [180]. These measurements and simulations correspond to the device with (nominal) 450 nm directional coupler gaps taken from the farthest "east" (i.e. largest photolithography exposure dose) column of the wafer.

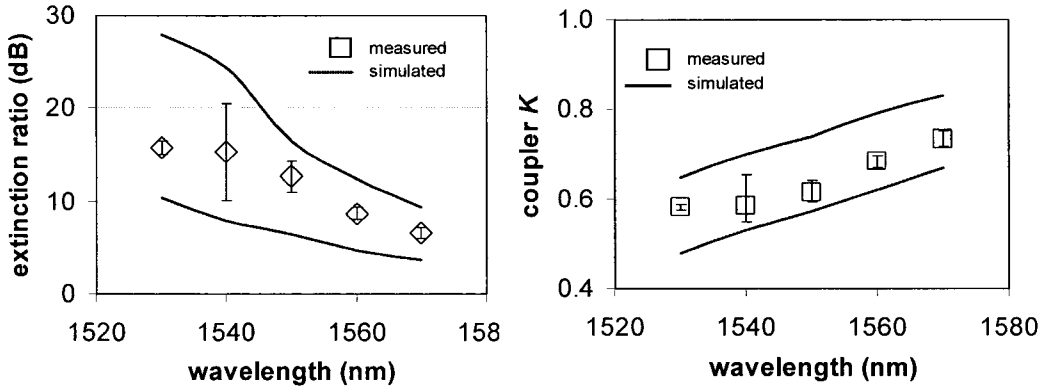


Fig. 4.16: Extinction ratio versus wavelength (left) showing measured values and simulated range based on process tolerances; coupler K (right) calculated from measured extinction ratios showing simulated K range versus wavelength.

### 4.5.3 Tuning Efficiency

Theoretical tuning efficiency can be calculated according to Eq. (4.39) by substituting $\theta = \pi$ and solving for $P_{th}$ to yield the expression shown in Eq. (4.55).

$$P_{th} = \frac{\left( \sqrt{\frac{\sigma_s \sigma_B t_s}{t_B}} + \frac{\sigma_B}{t_B} x_1 \right)}{\frac{1}{\lambda_0} \frac{dn}{dT}} e^{\sqrt{\frac{\sigma_B}{\sigma_s t_s t_B}} (|x| - x_1)} \tag{4.55}$$

The values used for the thermal properties of silicon and silica are shown in Table 4-1.

| constant | value | units |
|---|---|---|
| *dn/dT (silicon)* | $1.79 \times 10^{-4}$ [175] | $K^{-1}$ |
| *dn/dT ($SiO_2$)* | $< 1.8 \times 10^{-5}$ [181] | $K^{-1}$ |
| $\sigma_s$ | 1.48 [182] | W $cm^{-1}$ $K^{-1}$ |
| $\sigma_B$ | $1.35 \times 10^{-2}$ [183] | W $cm^{-1}$ $K^{-1}$ |

Table 4-1: Thermal properties used for calculation of theoretical tuning efficiency.

For the tuning geometry used in this device (see Fig. 4.10) with tuners 1 μm wide (i.e. $x_1$ = 0.5 μm) spaced 2 μm from the edge of the 0.5 μm wide rib waveguide (i.e. distance from the centre of the heat source to the centre of the waveguide $|x|$ = 2.75 μm), BOX thickness $t_B$ = 2 μm, silicon slab thickness $t_S$ = 50 nm, and wavelength of 1.55 μm, a theoretical thermal efficiency of 43.8 mW/$\pi$ is calculated from Eq. (4.55).

However, the expression of Eq. (4.55) neglects the thermo-optic contribution from the oxide cladding surrounding the rib. Although this effect is small due to the approximate order of magnitude difference between the thermal thermo-optic

coefficient of silica relative to silicon (the actual thermo-optic coefficient of the silica is dependent on the fabrication method), it is not insignificant owing to the considerable overlap of the optical mode with the cladding oxide (calculated to be 30%) for a sub-micron waveguide structure at 1550 nm wavelength. Accordingly an effective thermo-optic coefficient was derived by using BeamPROP to solve for the change in mode effective index as a function of temperature change in both the silicon and cladding oxide. A plot of the calculated effective index change versus thermo-optic index change at various temperatures is shown in Fig. 4.17.

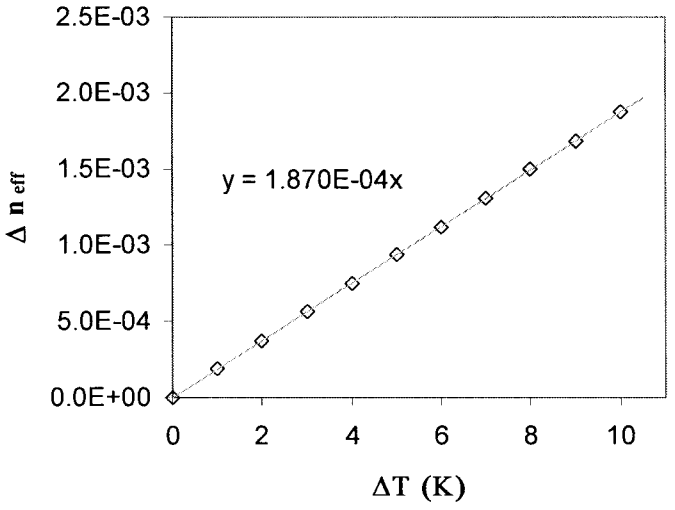


Fig. 4.17: Calculated change in mode effective index for the rib waveguide as a function of temperature increase using dn/dT ($SiO_2$) = 0.1* dn/dT (Si) and dn/dT (Si) = $1.79 \times 10^{-4}$.

Using the effective thermo-optic coefficient of $1.87 \times 10^{-4}$ calculated in Fig. 4.17 yields a value for thermal efficiency of 42 mW/$\pi$. This represents a high-end estimate for the efficiency since the thermo-optic coefficient of silica is less than the value used for the simulations shown in Fig. 4.17. The former value of 44 mW/$\pi$ as calculated above represents the low-end estimate without taking convective cooling into account.

Fig. 4.15 shows the measured tuning efficiency to be 44 ± 1 mW/π for tuning at 1550 nm. Tuning efficiency versus wavelength was measured and found to be

unchanged within the margin of error for wavelengths across the C-band (1520 nm to 1580 nm). The slight discrepancy between the theoretically derived values and the measured value for thermal tuning efficiency is thought to be a result of convective cooling at the tuners via air currents.

### 4.5.4 Tuning Speed

VOA tuning was measured as a function of frequency by replacing the picoammeter shown in Fig. 4.13 with a Tektronix digital oscilloscope to record the signal across a 5 KΩ gain resistor, and the power monitor with a Newport 818-BB high-speed photodetector. The AFG-310 was used to apply a sawtooth function to the device with sufficient amplitude to achieve modulation from maximum to minimum transmission, and the ratio of these optical outputs were measured. A plot of measured amplitude variation (normalized to the low frequency value) versus frequency is shown in Fig. 4.18 with the predicted result from Eq. (4.52) overlaid.

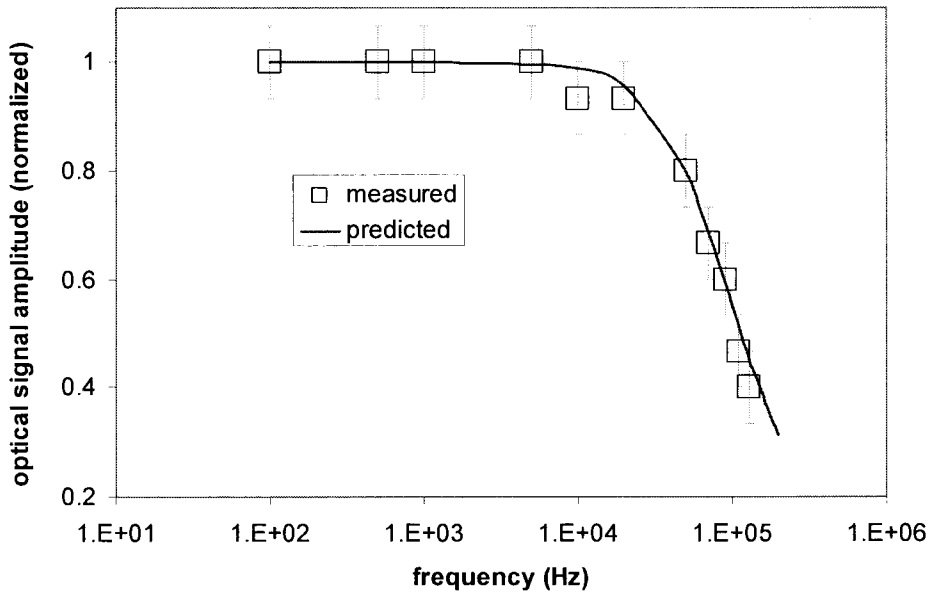


Fig. 4.18: Measured relative output modulation amplitude of the VOA as a function of thermal modulation frequency with the predicted curve from Eq. (4.52) overlaid.

The 3 dB frequency of the VOA was measured to be 105 ± 10 kHz. Calculation of the predicted 3 dB frequency from Eq. (4.53) yields a value of 114 KHz.

### 4.5.5 Integrated photodiode results

A plot of the IV characteristic (in the absence of illumination) is shown in Fig. 4.19. From the IV characteristic it is evident that leakage current for these devices is negligible relative to photocurrent and can be neglected.

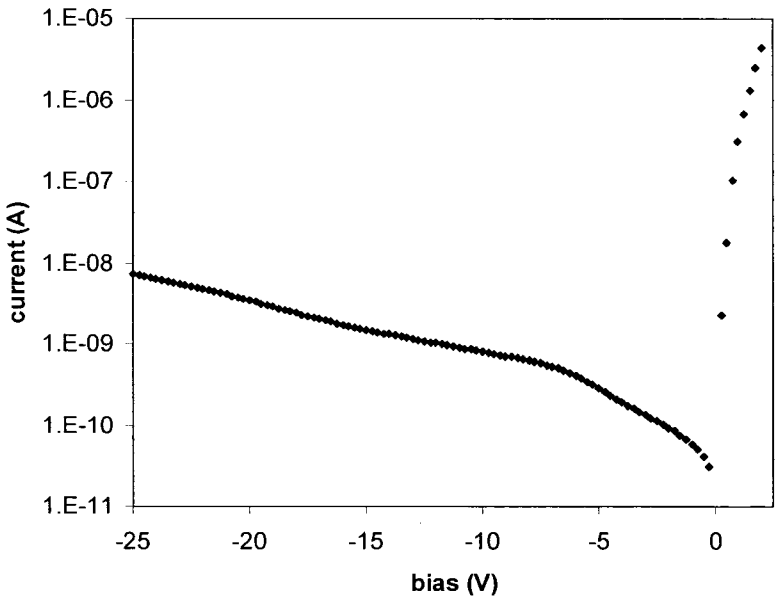


Fig. 4.19: Current vs. applied bias in dark for the 0.8 mm length photodiode employed as a tap monitor on the output arm of the VOA.

Tuning of the VOA was tested with simultaneous monitoring of photocurrent from the integrated photodiode. The optical output and photocurrent for a representative device is shown in Fig. 4.20.

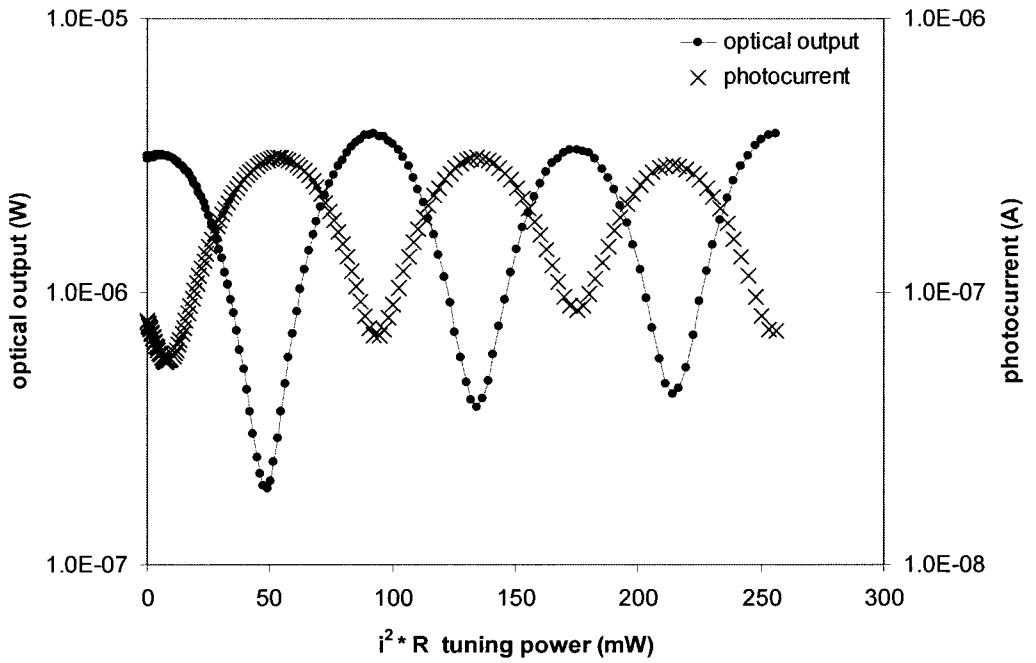


Fig. 4.20: Photocurrent and optical output vs. tuning for -5 dBm unpolarized optical input at 1550 nm.

From the work described in Chapter 3, the dominant defect in the optical absorption process has an optical cross-section of $6 \times 10^{-17}$ cm$^{-2}$ and a location in the band gap consistent with the divacancy. Estimates of divacancy concentration, however, were more than order of magnitude smaller than the CBK estimate and were suspect due to possible interference between the TSCAP and DLTS signal of the divacancy and an unidentified acceptor peak. Accordingly, the calculated CBK concentration estimate ($6.6 \times 10^{17}$ cm$^{-3}$) will be used here. Optical absorption loss estimates for the rib waveguides described in this chapter were therefore predicted to be 120 dB/cm with responsivity at 1550 nm greater than 0.6 A/W. For these calculations the trap density distribution was assumed to be uniform and the overlap fraction $F = 0.7$ was used, corresponding to the calculated mode overlap with the silicon rib. Measured absorption loss on a 1 mm test devices was 45 dB/cm with responsivity of 0.11 A/W. For the 0.8 mm devices integrated with the VOA, responsivity was only 21 mA/W where power

incident on the photodiode was calculated as measured peak optical power at the BAR output (-25 dBm) minus the expected grating coupler and propagation loss of -6.5 dB. The cause of these discrepancies is unclear, but may be due to (a) decreased divacancy density near the surface of the chip relative to the calculated average, and (b) additional optical loss within the MZI prior to the photodiode.

It is noteworthy that although the optical output extinction ratio is approximately 12 dB at the BAR output and (from the measurements shown in Fig. 4.15) at least 15 dB at the X output, the photodiode signal showed extinction of less than 8 dB. The signal at low optical coupling to the X output monitored by the photodiode was more than two orders of magnitude greater than the dark current, and must therefore have been due to collection of radiation scattered from the input grating coupler and from bends within the MZI – since 10 dB (i.e. 90%) of the unpolarized optical input is scattered into the chip, the observed 56 nA minimum photodiode signal with 21 mA/W responsivity corresponds to pickup of 1% of the optical power incident from the fiber to the chip, or 18% relative to the optical power in the waveguide prior to the photodiode.

### 4.5.6 Signal-to-noise ratio

For the responsivity and leakage current described in section 4.5.5 the diode has a theoretical signal-to-noise ratio (SNR) defined according to Eq. (4.56):

$$SNR = \frac{R \cdot P_{incident}}{I_d} \tag{4.56}$$

where $SNR$ is signal-to-noise ratio, $I_d$ is dark (leakage) current, $R$ is responsivity, and $P_{incident}$ is optical power incident on the detector. However, for the situation in which the noise floor is determined not by leakage current but by scattered input radiation collected by the photodiode, $SNR$ is instead determined by Eq. (4.57):

$$SNR = \frac{I_{signal}}{I_{noise}} = \frac{(P_{incident} R)}{(F P_{incident}) R} = \frac{1}{F} \tag{4.57}$$

in which $F$ is the fraction of $P_{in}$ scattered and collected by the photodiode.

The signal-to-noise ratio (*SNR*) of the photodiode in this configuration is therefore determined neither by the leakage current nor the MZI extinction ratio, but rather by input scattering; in this case the *SNR* of the photodiode is limited to a value of 5.6 irrespective of input power. This limitation constrains the capability of the photodiode as a tap monitor for the VOA output: the photodiode cannot effectively monitor the output when optical output on the BAR path exceeds (1-$F$) of maximum output, since this requires that optical signal in the X path (monitored by the photodiode) is less than $F$ and therefore below the *SNR* of the photodiode tap monitor.

# 4.6 Channel Leveller

## 4.6.1 Concept

With a VOA and tap monitor monolithically integrated in silicon, the possibility of using the monitor signal to provide feedback to an autonomous controller circuit is the logical sequitur. As the simplest form of such a feedback loop, photocurrent from the photodiode could be used to control the VOA so as to maintain a constant output irrespective of variations in input power: i.e. a channel leveller. This concept is illustrated in Fig. 4.21.

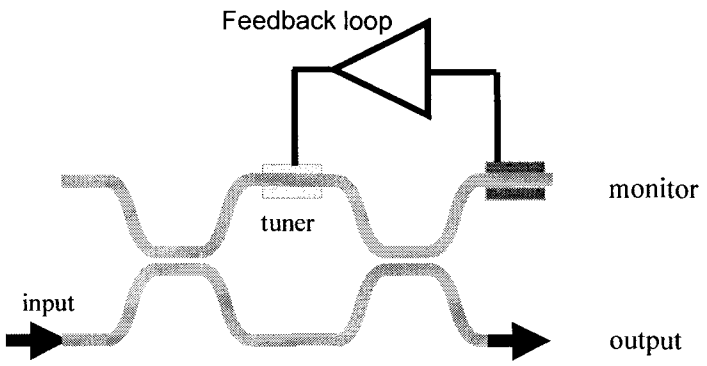


Fig. 4.21: Channel leveller concept - a feedback loop from the photodiode to the VOA tuner compensates for fluctuations in input power by adjusting the VOA output accordingly.

Ideally the electronic components of the circuit could be monolithically integrated alongside the VOA and photodiode. As a proof-of-concept, an external software loop was used in this work to mimic the operation of such a circuit in order to demonstrate autonomous channel levelling functionality.

### 4.6.2 Output path considerations

It is clear that with the tap monitor located on the output path, the relation between monitor signal and output power is simply proportional with the constant of proportionality being the responsivity. With this architecture the levelling algorithm can be very simple: the VOA should be tuned so as to increase BAR path output if the photodiode signal is below the target value, or to decrease BAR path output if the photodiode signal is higher than the target value. The 'target value' in both cases is defined as $i_{target} = R_{out} P_{target}$ where $R$ is the responsivity of the photodiode relative to output power and $P_{target}$ is the desired output power.

However this architecture holds the drawback that the photodiode must necessarily tap power from the output path, thus forcing excess loss. Since the VOA will generally be operated such that some optical power is routed to the non-output path (i.e. the X output for the configuration used in this work and

shown in Fig. 4.11) at all times in order to maintain a 'reserve' of output power with which to compensate for input power drops, it is desirable to locate the photodiode on the X output path such that it monitors the 'throw-away' power rather than the output power directly.

Monitoring the 'throw-away' power, however, adds complexity to the monitoring and correction algorithm, since a photodiode signal that is below a constant target value could denote that input power is low and hence that output power is below its desired target value. Alternatively, low photodiode signal could also denote that the VOA is simply directing too much power to the BAR path rather than the X path on which the photodiode is situated, which case output power is *above* its desired target value. In short, the relative value of the tap monitor signal alone is ambiguous and insufficient to determine the status of the output without additional information.

The output power can successfully be monitored by an off-output photodiode, however, with the inclusion of VOA bias information in the levelling algorithm. This approach is detailed below.

### 4.6.3 Levelling algorithm

Eq. (4.6) and Eq. (4.7) defined the relative outputs of the MZI in terms of thermal tuning power. Taking $K$ (i.e. coupling at each of the directional couplers in the MZI) to be 0.5 for simplicity and recalling that $T = 1 - K$, these relations may be re-expressed in terms of absolute output power and tuning voltage as per Eq. (4.58) and Eq. (4.59).

$$P_{BAR} = P_{in}\left[\frac{1}{2} - \frac{1}{2}\cos\left(\frac{V^2 - V_0^2}{r} + \phi\right)\right] \tag{4.58}$$

$$P_X = P_{in}\left[\frac{1}{2} + \frac{1}{2}\cos\left(\frac{V^2 - V_0^2}{r} + \phi\right)\right] \tag{4.59}$$

where $P_{BAR}$ is output power at the BAR path, $P_X$ is output power at the X path, $P_{in}$ is input power, $\phi$ is the phase of the transfer function at a reference point, $V$ is applied voltage, $V_0$ is the applied voltage at a reference point, and $r$ is the electrical resistance of the tuner.

Since photocurrent $i = RP_x$ where $R$ is responsivity as described in section 4.5.5, Eq. (4.59) may be modified to produce Eq. (4.60) for photocurrent from the tap monitor:

$$i = RP_{in}\left[\frac{1}{2} + \frac{1}{2}\cos\left(\frac{V^2 - V_0^2}{r} + \phi\right)\right]. \tag{4.60}$$

In the vicinity of the VOA transfer function half-maximum (henceforth referred to as the point of "quadrature"), both the output power and the photocurrent can be approximated with linear relations as shown in Fig. 4.22.

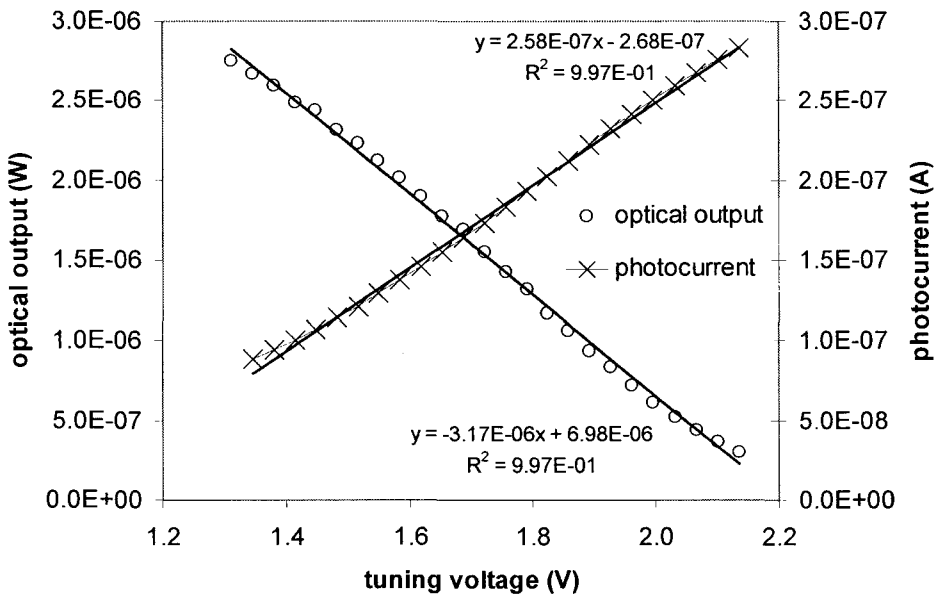


Fig. 4.22: VOA output (BAR path) and photocurrent (X path) vs. tuning voltage near quadrature together with overlaid linear best fits. Input power was -5 dBm at 1550 nm.

General expressions for the linear approximations of output power and photocurrent near a reference point (e.g. quadrature) are given by Eq. (4.61) and Eq. (4.62)

$$P = \alpha\left(\frac{dP}{dV}\Delta V + P_{ref}\right) \tag{4.61}$$

$$i = \alpha\left(\frac{di}{dV}\Delta V + i_{ref}\right) \tag{4.62}$$

where $P_{BAR}$ has been replaced by $P$ for simplicity, $P_{ref}$ is an arbitrarily chosen reference power near quadrature, $i_{ref}$ is the photocurrent corresponding to $P = P_{ref}$, $\Delta V = V\text{-}V_0$ and $\alpha$ is the fractional input power relative to reference input power.

Then setting $P = P_{ref}$ provides an iterative solution for tuner bias voltage as shown in Eq. (4.63):

$$\Delta V = \frac{P_{ref}}{\left(\frac{dP}{dV}\right)i}\left(\frac{di}{dV}\Delta V + i_{ref} - i\right). \tag{4.63}$$

The values $dP/dV$, $di/dV$, and $i_{ref}$ near quadrature for a desired reference output power $P_{ref}$ are constants which can be characterized for a given device at predefined photodiode bias voltage, output reference power, and reference voltage $V_0$. Collecting constants in Eq. (4.63) produces Eq. (4.64)

$$\Delta V = c_1\frac{\Delta V}{i} + \frac{c_2}{i} + c_3 \tag{4.64}$$

in which $c_1 = P_{ref}(di/dV) / (dP/dV)$, $c_2 = P_{ref}\, i_{ref} / (dP/dV)$, and $c_3 = -P_{ref} / (dP/dV)$ are constants characteristic of the device at a particular reference power, wavelength, and photodiode bias. A feedback loop which reads photodiode signal $i$ and MZI voltage $\Delta V$, and applies new MZI voltage adjustment $\Delta V$ according to Eq. (4.64) will therefore hold output power constant at $P = P_{ref}$ subject to the limitations of the linearity approximation for power and photocurrent as functions

of bias voltage used in the derivation above. For the tuning shown in Fig. 4.22 it is clear that the linearity approximation holds for approximately 10 dB of output power variation.

### 4.6.4 Test setup

The levelling algorithm can be implemented using either digital or analogue circuitry integrated on the chip, thus taking full advantage of silicon's potential for the integration of optical and electrical devices. For this work, however, software code written in NI LabVIEW was used to mimic the function of a digital circuit by applying the algorithm described in Eq. (4.64), a Keithley 485 picoammeter was used to read photocurrent from the tap monitor, and a Tektronix AFG310 function generator was used to apply bias to the MZI. The setup used for this purpose is shown in Fig. 4.23.

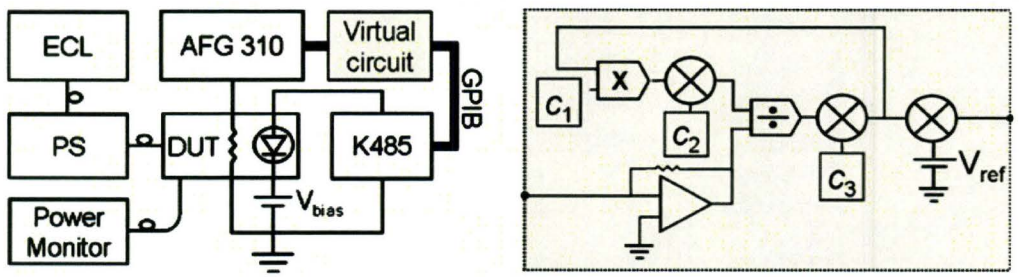


Fig. 4.23: Test setup (left) and virtual circuit (right) used to evaluate the channel leveller. PS = polarization scrambler; DUT = device under test; K485 = Keithley 485 picoammeter; ECL = external cavity laser; AFG310 = Tektronix AFG310 function generator.

### 4.6.5 Results

The device was tested with photodiode bias set at -10V for optical wavelengths ranging from 1530 nm to 1570 nm. The feedback loop described in the previous section was used to apply the algorithm of Eq. (4.64) to the MZI tuner using photocurrent read from the tap monitor. The constants $c_1$, $c_2$, and $c_3$ were determined by sweeping the tuning bias for each wavelength as shown for the

1550 nm case in Fig. 4.22. The reference power used was 5 dB below max transmission (-30 dBm for 1550 nm as shown in Fig. 4.15) for each wavelength in order to allow the algorithm enough reserve power to compensate for input fluctuations of at least 4 dB in either direction (recall that the extinction ratio of this device ranges from 10 dB to 23 dB depending on wavelength). The output power as a function of input fluctuation is shown in Fig. 4.24.

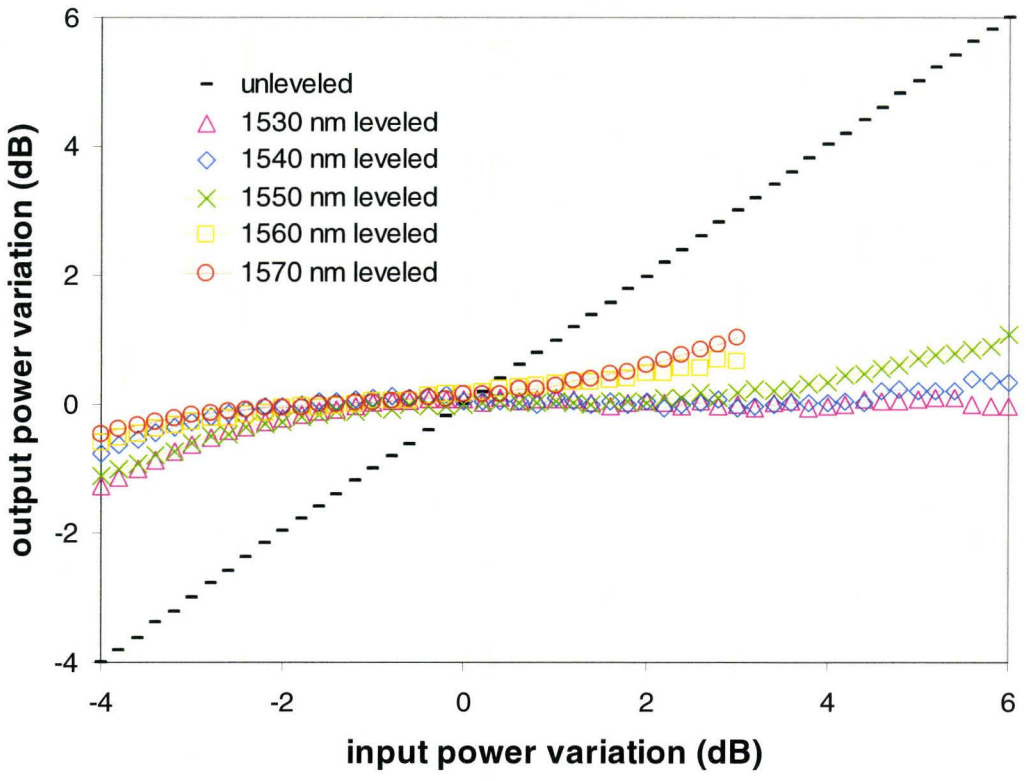


Fig. 4.24: Output power fluctuation as a function of input power fluctuation across a 7-10 dB dynamic range for wavelengths from 1530 nm to 1570 nm. The measured output for the unlevelled case is overlaid for comparison.

Output power was held to within ±1 dB across a 7 dB dynamic range for the full wavelength range. For the wavelength range from 1530 nm to 1570 nm the leveller holds the output to within ± 1 dB across a 10 dB dynamic range or ± 0.3 dB for ± 2 dB input variation as shown in Fig. 4.25.

### 4.6.6 Limitations on dynamic range

For positive input power fluctuations the leveller must compensate by increasing the MZI bias voltage (for the case described here and shown in Fig. 4.22), thus redirecting excess power into the X path. The extent to which the leveller can compensate is dictated by the extinction ratio of the VOA; the linearity of the transfer function (on which the levelling algorithm relies) degrades towards the edges of the attenuator's dynamic range.

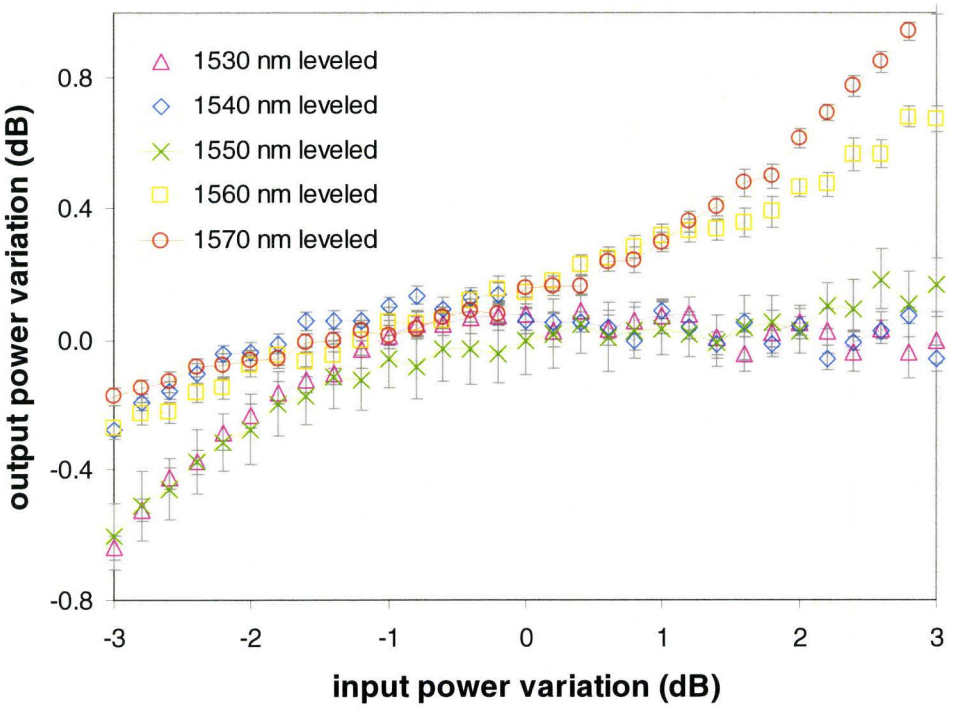


Fig. 4.25: Output power variation versus input variation for wavelengths ranging from 1530 nm to 1570 nm across a 6 dB dynamic range. The error bars denote one standard deviation for 90 feedback loop iterations.

Extinction ratio of the VOA depends on the $K$ value of the MZI couplers and thus varies with wavelength as described in section 4.5.2 and illustrated in Fig. 4.16. A comparison of leveller dynamic range (defined here as the range of input power fluctuation over which the output is held to within ± 0.5 dB fluctuation from the reference value) to VOA extinction ratio versus wavelength is shown in Fig. 4.26.

As expected, the variation in dynamic range shows the same trend with wavelength as VOA extinction ratio. The performance of the channel leveller can therefore be optimized for a given wavelength by fabricating the MZI couplers such that $K = 0.5$.

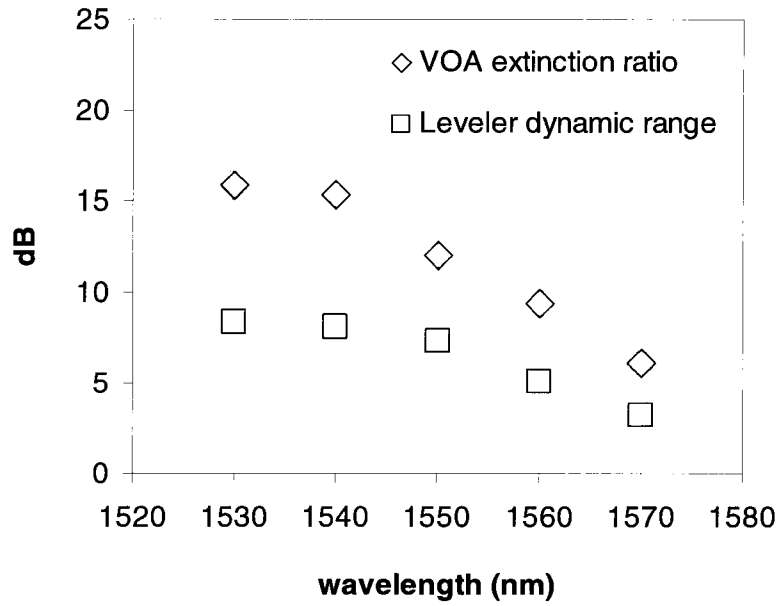


Fig. 4.26: Extinction ratio of the MZI and dynamic range of the channel leveller versus wavelength, where dynamic range is measured as the total input power fluctuation over which the leveller holds the output to within ± 0.5 dB of the reference output power.

For negative input power fluctuations the channel leveller must lower the bias (again, referring to the specific case shown in Fig. 4.22) in order to redirect reserve power into the BAR output path. Optical power incident on the photodiode, therefore, is reduced not only by the reduction in input power but even further by the action of the channel leveller. In consequence, not only is the tap monitor signal reduced as optical input power declines, but it is reduced as the *square* of the decline and thus quickly falls toward the noise floor of the tap monitor, thus invalidating the linear approximation on which the levelling algorithm depends. As discussed in section 4.5.6, this noise floor is determined by optical scattering within the device and is never less than 1/6 of the maximum

signal for the device described in this work. The low-limit of the channel leveller's dynamic range, therefore, is determined by this noise floor. Since optical scattering within the device can be reduced by adding spatial filters (e.g. metal or highly doped regions) around the input grating and the MZI, these tactics may improve the operational dynamic range of the channel leveller.

## 4.7 Further work

### 4.7.1 Spatial filters

As discussed in sections 4.5.6 and 4.6.6, the tap monitor's *SNR* plays a key role in determining the dynamic range of the channel leveller. This metric can be improved by adding spatial filters around key scattering features on the chip such as grating couplers and waveguide bends, as well as in the vicinity of the photodiode to absorb scattered radiation that may otherwise be absorbed by the photodiode. These spatial filters could take the form of metal pads, highly doped regions, or even defect implantation windows situated on all unused portions of the chip surface so as to absorb unconfined light propagating in the silicon slab.

### 4.7.2 MZI power consumption

The device described in this work required approximately 30 mW of tuning power at all times to hold the MZI at its reference point on the transfer function. This power consumption can be eliminated by employing a balanced MZI approach in which either arm can be heated. The optimal design involves either manufacturing or "trimming" (i.e. adding small adjustments to the waveguide effective index after the device has been fabricated) the relative phase of the two arms of the MZI such that without thermal power applied to either arm, the output

sits at the operating point (i.e. near or slightly below quadrature). Tuning in either direction then relies on applying power to either arm, rather than the single-arm tuning approach used in this work.

### 4.7.3 MZI couplers

As described in section 4.6.6, the upper end of the channel leveller's dynamic range is determined by the VOA extinction ratio, which is in turn dictated by the MZI coupler $K$. For coupler $K$ equal to 0.5, unlimited extinction ratio is theoretically possible. Broadening of the dynamic range can therefore be achieved by fabricating the MZI couplers such that they are as close to $K = 0.5$ as possible at the wavelength of interest.

### 4.7.4 Alternate MZI tuning

The VOA used in this work was a thermally tuned MZI, however other approached are possible. An MZI which employs carrier depletion [45, 184, 58] rather than thermal tuning could be implemented which, while retaining the simplicity of the approach described in this work, would be capable of much higher tuning speed and could therefore be used to compensate for fast fluctuations in input power.

### 4.7.5 Carrier-injection attenuation

Non-MZI structures are also possible. A VOA employing carrier injection alleviates the need for an interferometer altogether, offering a highly linear relation between attenuation and injected current for a very large attenuation range [46]. This approach eliminates the difficulties associated with fabricating an MZI with coupler $K = 0.5$ while achieving the same high extinction ratio, and

thus very wide dynamic range. Although channel levelling with this approach has not yet been reported, a device which integrates a carrier injection VOA and a defect-mediated photodiode in silicon has very recently been reported [186].

### 4.7.6 Ring-resonator enhanced detection

As described in detail in Chapter 5, a tuneable ring resonator with an integrated photodiode may be used as the means of variable attenuation rather than an MZI. Such an approach offers the advantages of enhanced sensitivity for the photodiode and hence an improvement in the extent of dynamic range for negative power fluctuations as described in section 4.6.6. The power consumption might also be improved since the resonance peak can be very abrupt, however the device would be very sensitive to small tuning variations and might therefore be more susceptible to issues with stability.

### 4.7.7 On-chip electronics

The levelling algorithm can be integrated on-chip for a completely autonomous "black-box" device that maintains output optical power without any external input beyond electrical and optical power. This is one of the key advantages of silicon photonics and offers the potential for both optimal compactness, reduced packaging cost, and minimal fabrication/assembly cost.

### 4.7.8 Cascaded devices

Cascading two or more channel levellers in series enhances the precision of the output since each brings the output closer to the target value. For example, the device demonstrated in this work holds the output to within ± 1 dB for 10 dB of input dynamic range at 1550 nm (see Fig. 4.24); a sequential leveller would hold

the ± 1 dB variation from the first leveller to within ± 0.1 dB (see Fig. 4.25) for overall channel levelling of ± 0.1 dB for a 10 dB dynamic range.

Cascading devices in parallel allows demultiplexed channels to be levelled individually so as to compensate for spectral variation in the amplification/loss characteristics of an optical link.

## 4.8 Chapter summary

A defect-enhanced photodiode for sub-band wavelengths monolithically integrated in silicon with a variable optical attenuator for monitoring and control of the attenuator output has been demonstrated, characterized, and modeled. As a further demonstration of this capability, the device was operated as a channel leveller using external software to mimic an electronic feedback loop between the tap monitor and the variable attenuator. The channel leveller achieved ± 1 dB output power variation across a 7-10 dB input dynamic range for wavelengths ranging from 1530 nm to 1570 nm.

# Chapter 5

# Resonator integration

Resonant structures can be used to concentrate optical power such that the optical field intensity is magnified relative to a single-pass design. Integration of a photodiode within such a resonant structure therefore offers the prospect of higher quantum efficiency and lower minimum detectable power at select wavelengths. This chapter describes the design and performance of tunable ring-resonant defect-mediated photodetectors. Through the use of tunable resonance the devices were also rendered capable of enhanced responsivity at any wavelength in the *C*-band and of operating as compact optical switches with built-in power monitors.

## 5.1 Ring resonators in silicon

The concept of resonance enhancement for photodiodes is not new; resonance enhancement using Fabry-Perot microcavities emerged in the early 1990's [187]. Resonance enhanced detection in silicon at *C*-band wavelengths has been demonstrated using germanium-based detectors [188] and PbTe films [189] in Fabry-Perot structures. For silicon photonics, however, device structures which

rely solely on planar fabrication steps are generally preferred. Fabry-Perot resonators require reflection from end-facets – these are often awkward to fabricate since they involve a non-planar step and have the added shortcoming that it is difficult to adjust their reflectivity. For example, a vertically etched silicon/air facet has a power reflection coefficient of 0.31; a facet coated in cladding oxide has a reflection coefficient of approximately 0.17, and a facet coated in gold has a reflection coefficient close to unity. However the options are quite limited for a designer who wishes to achieve a facet with an arbitrary reflection coefficient (e.g. in order to control the quality factor of the resonator) since the standard approach of depositing dielectric film stacks of precise thickness is not available for vertically oriented features.

Ring resonators, on the other hand, are entirely compatible with planar process steps and are analogous to Fabry-Perot resonators in which the reflection coefficient of one end-facet is replaced by the coupling coefficient between a "bus" waveguide and the ring resonator, and the other reflection coefficient is replaced by the transmission coefficient of the ring resonator. A diagram of the waveguide arrangement for a simple "racetrack" ring resonator is shown in Fig. 5.1.

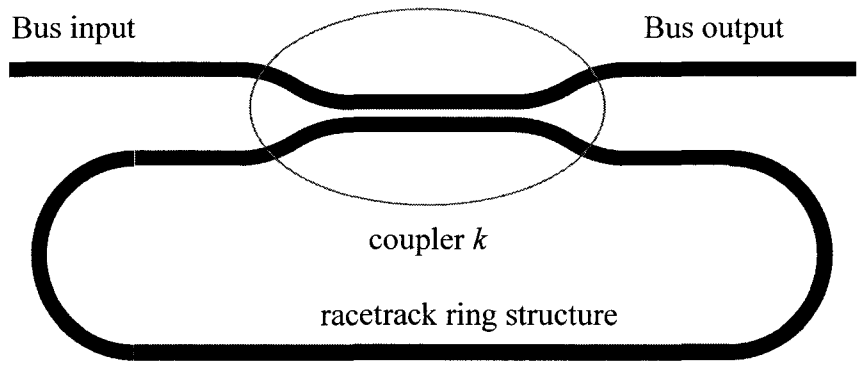


Fig. 5.1: Racetrack ring resonator waveguide layout showing "bus" waveguide which bypasses the ring via a directional coupler with coupling coefficient $k$. Optical power enters and exits the ring via the coupler in exactly analogous fashion to a Fabry-Perot cavity in which optical power enters and exits the cavity via a partially reflective end-facet.

Ring resonators have been demonstrated in silicon for a number of applications including optical modulation [61], Raman amplification and lasing [190-192], and hybrid III-V/silicon lasing [193] and detection at 1550 nm via germanium-based photodiodes integrated with microrings [166]. The use of monolithic ring-resonant structures for enhanced detection of *C*-band wavelengths in silicon was proposed with respect to photoemission at a Schottky barrier by Casalino *et al.* [194] and volume defect-mediated detection by Doylend *et al.* [195] in 2006. Ring-resonator cavity-enhanced defect-mediated detection in silicon was first demonstrated in 2009 by Chen *et al.* [98] using surface-mediated defects. However, the responsivity of these devices was quite low (0.25 mA/W at -15 V bias), likely because of the small overlap between the waveguide optical mode and the surface defect states. Responsivity of 0.1 A/W was recently reported by Shahifa *et al.* [196] and 0.039 A/W by Logan *et al.* [197] for ring-resonant detectors in silicon using defects produced by ion implantation. Some of the work discussed in this chapter has been published in reference [198].

## 5.2 Theoretical considerations

For a waveguide-integrated *p-i-n* photodiode incorporating defects within the waveguide core (see Fig. 3.34) the optical absorption dictates the maximum efficiency of the device assuming that the intrinsic region is narrow enough to extract most of the photoexcited carriers before they recombine. This consideration leads to certain limitations on device signal-to-noise ratio as will be shown below. A properly designed resonant cavity can eliminate these limitations.

### 5.2.1 Responsivity versus length

Optical absorption and carrier generation within a short waveguide diode segment are proportional to the incident optical flux and hence the incident optical power as discussed in chapter 3. For the case in which all free carriers generated in this manner are swept out of the junction (i.e. the entire region is depleted and is narrow enough for carriers to be extracted before they can recombine) the photocurrent may be described by Eq. (5.1):

$$i_{ph} = P(z)\gamma dz \tag{5.1}$$

in which $i_{ph}$ is the photocurrent, $dz$ is the length of the segment, $P(z)$ is the optical power as a function of propagation distance $z$, and $\gamma$ is defined according to Eq. (5.2):

$$\gamma = \frac{q\sigma_{opt}}{h\nu} \frac{\iint_A |E(x,y)|^2 N_T(x,y) dA}{\iint_A |E(x,y)|^2 dA} \tag{5.2}$$

in which $N_T$ is the density of optically active traps, $\sigma_{opt}$ is the photoionization cross-section, $q$ is carrier charge, $A$ is cross-sectional area, and $h\nu$ is the photon energy. For the simple case in which the trap density $N_T$ is approximately constant within the region of overlap the expression simplifies to Eq. (5.3):

$$\gamma = \frac{q\sigma_{opt}}{h\nu} f N_T \tag{5.3}$$

in which $f$ is the fractional overlap of the mode with the region containing defects.

For uniform optical propagation or absorption loss, the evolution of optical power versus propagation length can be described by Eq. (5.4):

$$\frac{dP(z)}{dz} = -\alpha P(z) \tag{5.4}$$

where $\alpha$ is the loss coefficient equal to $4\pi\kappa/\lambda_0$ for $\kappa$ the imaginary component of the effective index and $\lambda_0$ the wavelength in vacuum. Then solving for *P(z)* yields Eq. (5.5):

$$P(z) = P_{inc}e^{-\alpha z} \tag{5.5}$$

in which $P_{inc}$ is the incident power.

Substituting Eq. (5.5) into Eq. (5.1) and integrating over propagation length $L$ produces Eq. (5.6) for overall photocurrent:

$$i_{ph} = \frac{P_{inc}\gamma}{\alpha}\left(1 - e^{-\alpha L}\right) \tag{5.6}$$

and then the expression for responsivity $R_\lambda$ is given by Eq. (5.7):

$$R_\lambda = \frac{i_{ph}}{P_{inc}} = \frac{\gamma}{\alpha}\left(1 - e^{-\alpha L}\right). \tag{5.7}$$

From Eq. (5.7) it is apparent that the responsivity increases with the length of the device up to a maximum of $\gamma/\alpha$, beyond which there is no benefit from additional length since all the guided optical power has either been scattered or absorbed. For example, with absorption loss of 45 dB/cm as measured for the channel leveller devices described in Chapter 4, photocurrent increases up to a device length of 1 mm; beyond this point 4.5 dB or approximately two thirds of the power has been absorbed, and so additional device length provides steadily diminishing photocurrent.

### 5.2.2 Signal-to-noise ratio considerations

Signal-to-noise ratio (SNR) of a detector is a figure of merit which determines the dynamic range of input power over which the detector signal provides useful information. For a detector with constant responsivity $R_\lambda$, the output signal (i.e. photocurrent) is $i_{ph} = R_\lambda P_{opt}$ where $P_{opt}$ is the input optical power. The SNR of

the diode is therefore $R_\lambda P_{opt} / i_{noise}$ where $i_{noise}$ is the noise floor current, and thus increases with optical input power. For a given optical input power, however, the SNR is determined by the ratio of $i_{noise}$ to $R_\lambda$, which can be expressed as the "minimum detectable power" (MDP) equal to the noise current divided by responsivity.

In an ideal photonic circuit in which the photodiode "sees" light only in the waveguide which it is intended to monitor, the noise floor is determined by the leakage current. It is apparent that increasing the responsivity while incurring a commensurate increase in leakage current provides no overall advantage: MDP remains unchanged, and therefore SNR for a given input power also remains unchanged.

This presents a tradeoff for defect-mediated waveguide photodetectors. From Eq. (5.6) the responsivity can be increased (to a point) by increasing the length of the diode. Assuming a constant leakage current density, however, the leakage current increases linearly with diode length while the responsivity decreases as $(1\text{-}e^{-\alpha L})$. The responsivity can also be enhanced by increasing the trap density $N_T$ according to Eq. (5.3), however this also leads to an increase in the leakage current as discussed in Chapter 3.

### 5.2.3 Resonant power

The transfer matrix for a symmetric directional coupler was derived in Chapter 2 and is given in Eq. (5.8):

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} t & jk \\ jk & t \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{5.8}$$

where $a_1$, $a_2$, are the field amplitudes at the two inputs, $b_1$, $b_2$ are the field amplitudes at the two outputs, and $t$, $k$ are the amplitude transmission and

coupling coefficients. For any system in which there is feedback from output $b_2$ to input $a_2$ the two can be related according to Eq. (5.9):

$$a_2 = b_2 r e^{j\theta} \tag{5.9}$$

where $r$ is the fractional amplitude transmission and $\theta$ the phase incurred within the feedback path. The feedback as applied to a ring resonator is illustrated in Fig. 5.2.

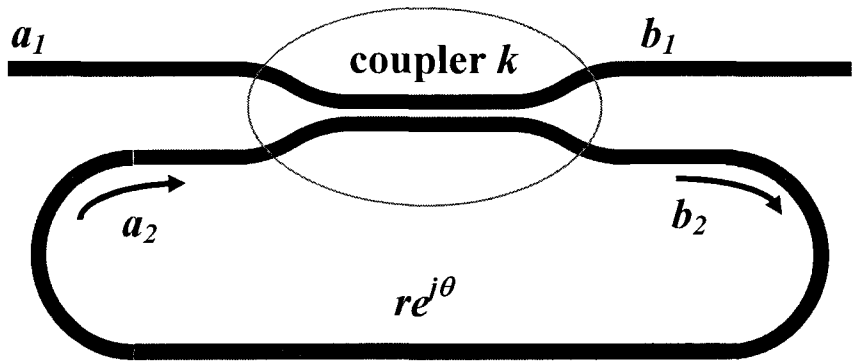


Fig. 5.2: Schematic of ring resonator as a feedback loop with input $a_1$, output $b_1$, ring input $b_2$, ring loopback $a2$ and feedback factor $re^{j\theta}$.

Substituting Eq. (5.9) into the expressions for $b_2$ and $b_1$ from Eq. (5.8) and solving produces the expressions of Eq. (5.10) and Eq. (5.11):

$$b_1 = \frac{t - re^{j\theta}}{1 - rte^{j\theta}} a_1 \tag{5.10}$$

$$b_2 = \frac{jk}{1 - rte^{j\theta}} a_1 . \tag{5.11}$$

Therefore defining the relative power (and intensity) at $b_1$ and $b_2$ according to Eq. (5.12) and Eq. (5.13):

$$\frac{B_1}{A_1} = \left|\frac{b_1}{a_1}\right|^2 = \frac{t^2 + r^2 - 2rt\cos\theta}{1 + r^2t^2 - 2rt\cos\theta} \tag{5.12}$$

$$\frac{B_2}{A_1} = \left|\frac{b_2}{a_1}\right|^2 = \frac{k^2}{1 + r^2t^2 - 2rt\cos\theta} . \tag{5.13}$$

For the case where cos $\theta$ = 1 (i.e. resonance), these expressions simplify to Eq. (5.14) and Eq. (5.15):

$$\frac{B_1}{A_1} = \frac{(t-r)^2}{(1-rt)^2} \tag{5.14}$$

$$\frac{B_2}{A_1} = \frac{k^2}{(1-rt)^2}. \tag{5.15}$$

It is apparent that for the special case in which $r = t$ (referred to as "critical coupling") - i.e. coupling into the ring is equal to the fractional loss during traversal of the ring – the power at the output $B_1$ drops to zero while power within the ring $B_2$ obeys the relationship given by Eq. (5.16):

$$\frac{B_2}{A_1} = \frac{1}{k^2} = \frac{1}{1-r^2} \tag{5.16}$$

where the identity $(1-t^2) = k^2 = K$ (i.e. power is conserved within the directional coupler) has been employed.

Eq. (5.16) establishes that the power stored within the resonator is greater than the power in the input bus waveguide, and can be arbitrarily greater provided that the loss $(1-r^2)$ within the resonator approaches 0. It should also be noted that it is impossible to distinguish $r$ from $t$ in Eq. (5.14) – measurements of the output power from a ring resonator can always be fitted with two solution sets - [$r$, $t$] and [$t$, $r$] - unless additional information is available as to which is which.

An example transfer function showing the relative power transmitted to the output bus waveuide ($B_1$) for the three regimes in which fractional power coupled to the resonator exceeds the round-trip loss (overcoupling), equals the round-trip loss (critical coupling), and falls short of the round-trip loss (undercoupling) are illustrated in Fig. 5.3. It should be noted that for the case of critical coupling the output power falls to zero at resonance, and thus the power stored in the ring is maximized.

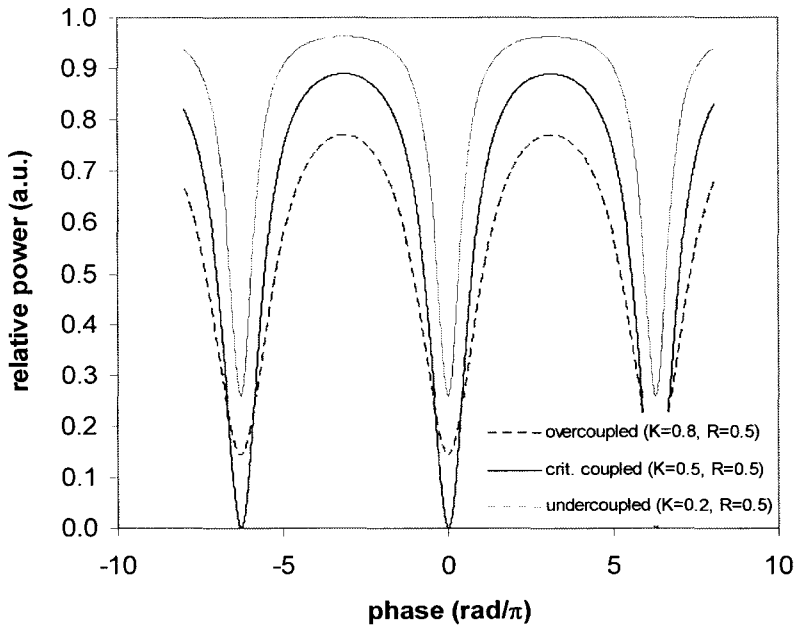


Fig. 5.3: Resonator output $B_1$ for $R=r^2=0.5$ and three coupling conditions: undercoupled with $K = 0.2$, critically coupled ($K = 0.5$), and overcoupled ($K = 0.8$).

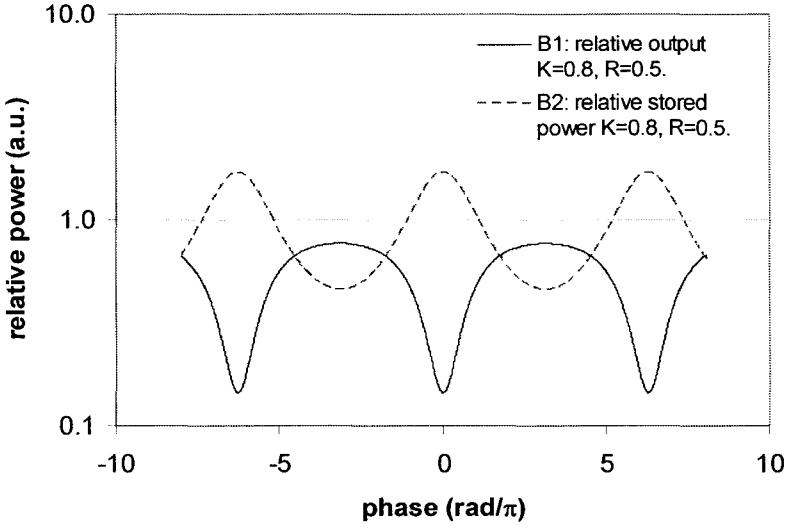


Fig. 5.4: Relative output power $B_1$ and cavity stored power $B_2$ for the overcoupled case $K$=0.8 and $R$=0.5.

A plot of the bus output $B_1$ and cavity input $B_2$ versus phase for the overcoupled case are shown in Fig. 5.4.

### 5.2.4 Cavity enhancement and MDP

At critical coupling and on resonance the power within the ring (prior to round-trip loss) is described by Eq. (5.16). Substituting this expression for the power incident on the photodiode in Eq. (5.6) produces Eq. (5.17):

$$i_{ph} = \left(\frac{P_0}{1-r^2}\right)\left(\frac{\gamma}{\alpha}\right)\left(1-e^{-\alpha L}\right) \tag{5.17}$$

in which $P_0$ is the input power $A_1$ and $L$ is the length of the photodiode within the ring. The factor $(1\text{-}r^2)$, however, is by definition the fractional power lost within the ring resonator. For the special case in which the round-trip loss of the ring is primarily due to absorption within the photodiode, the factor $(1\text{-}r^2)$ approaches the factor $(1\text{-}e^{-\alpha L})$ so that the overall expression simplifies to Eq. (5.18):

$$i_{ph} = P_0\left(\frac{\gamma}{\alpha}\right). \tag{5.18}$$

Overall responsivity therefore approaches $\gamma/\alpha$ independent of diode length. Comparison of this expression with Eq. (5.7) shows that the responsivity approximates the limiting value achievable by extending the diode length in a straight-waveguide device until all the optical power is absorbed. This striking result can be understood intuitively based on the understanding that (1) reduction in photodiode length within the ring (and hence absorption) is compensated by increased cavity enhancement due to the reduction of the denominator in Eq. (5.16), and (2) at resonance and critical coupling, all optical power in the bus is confined to the ring and therefore must be absorbed by the photodiode.

The difficulty of balancing the need to maximize responsivity while limiting the leakage current described in section 5.2.2 can therefore be addressed by situating the photodiode within a resonant cavity: near-total optical absorption can be accomplished without increasing either the length or the defect density of the

diode, thus keeping leakage current to a minimum while enhancing the responsivity such that extremely low MDP is possible.

### 5.2.5 Practical considerations regarding MDP

Optimal resonance-enhanced photodiode performance is possible only under the conditions used in the derivation above, namely:

(1) the ring resonator is critically coupled (i.e. $r = t$ in Eq. (5.13)),

(2) the device is at resonance (i.e. $\cos\theta = 1$ in Eq. (5.13)), and

(3) the round-trip fractional power loss ($1-r^2$) within the ring approximates the fractional power loss ($1-e^{-\alpha L}$) within the photodiode.

In practical terms, condition (1) requires either careful design of the directional coupler $k$ or the incorporation of a tunable coupler (e.g. a MZI). Condition (2) is easily achievable either by careful selection of the wavelength of operation or by employing phase tuning within the resonator, and condition (3) relies on low-loss waveguides, large bend-radii to avoid excessive scattering, and a region of high defect concentration which overlaps the optical mode sufficiently to induce significant loss relative to the other loss mechanisms within the resonator.

### 5.2.6 Modeling resonant detection

Since both $\alpha$ and $\gamma$ are determined solely by the defect and waveguide characteristics of the structure, a test device (i.e. a photodiode integrated with a straight waveguide) can be used to determine $\alpha$ and $\gamma$ for the particular waveguide/detector geometry in use. The excess loss associated with the defects identifies $\alpha$ according to Eq. (5.5) and the responsivity identifes $\gamma$ according to Eq. (5.7). With these two quantities known, Eq. (5.6) determines the photocurrent within the ring where the power incident on the photodiode $P_{inc}$ is

the input power multipled by the resonant cavity factor given by Eq. (5.13). Ring coupling and round-trip loss can be determined by fitting Eq. (5.12) to the output provided that either ring loss or coupling are known.

The overall expression for photocurrent is therefore given by Eq. (5.19)

$$i_{ph} = \frac{\gamma}{\alpha}\left(1-e^{-\alpha L}\right)P_{inc} = R_{\lambda 0}\left(\frac{1-e^{-\alpha L}}{1-e^{-\alpha L_0}}\right)\frac{K}{1+RT-2rt\cos\theta}P_0 \qquad (5.19)$$

where $L_0$ and $R_{\lambda 0}$ are the length and responsivity of a straight test device, $R=r^2$ is the power transmitted during one round-trip of the ring, $T=t^2=(1-k^2)$ is the transmission of the directional coupler, $K=k^2$ is coupling (power) between the bus and the ring, $P_0$ is the bus input power, and $\theta$ can be approximated by $\theta \approx (2\pi L_r d\lambda/\lambda^2)$ for $L_r$ the circumference of the ring. Solving for the responsivity $R_\lambda$ (with respect to bus waveguide input power) in Eq. (5.19) eliminates $P_0$ to yield Eq. (5.20):

$$R_\lambda = R_{\lambda 0}\left(\frac{1-e^{-\alpha L}}{1-e^{-\alpha L_0}}\right)\left(\frac{K}{1+RT-2rt\cos\theta}\right). \qquad (5.20)$$

It should be noted that Eq. (5.20) enables characterization of the responsivity of the ring-resonant photodiode using only relative power variation at the output without recourse to any knowledge of absolute optical power, assuming that $R_{\lambda 0}$ and $\alpha$ have been successfully determined from a prior test structure.

# 5.3 Design and fabrication

The devices were fabricated in the world-class LETI microfabrication complex, France, as part of the ePIXFab 2009 shuttle run [180] using the same fabrication steps described in section 4.4. The waveguide and lateral aspects of the photodiode design were addressed in section 4.3.

### 5.3.1 Ring loss considerations

To achieve cavity enhancement within the ring of at least a factor of 5 (this value is chosen arbitrarily), round-trip loss of less than 1 dB was required according to Eq. (5.16). Propagation loss within the unimplanted waveguide was assumed to be 2.4 dB/cm [179], while absorption loss due to the implantation (as described in section 4.3.4) was expected to be approximately 100 dB/cm. A total ring resonator circumference of 190 μm with a diode length of 60 μm was chosen to correspond to round-trip loss less than 1 dB with at least 90% of the round-trip loss caused by absorption within the diode.

An integrated heater in the form of a 1 μm wide metal trace overlaying the ring was included to allow tuning of the resonance wavelength. The trace was not placed directly over the waveguide due to concerns about metal-induced losses. A schematic of the device is shown in Fig. 5.5.

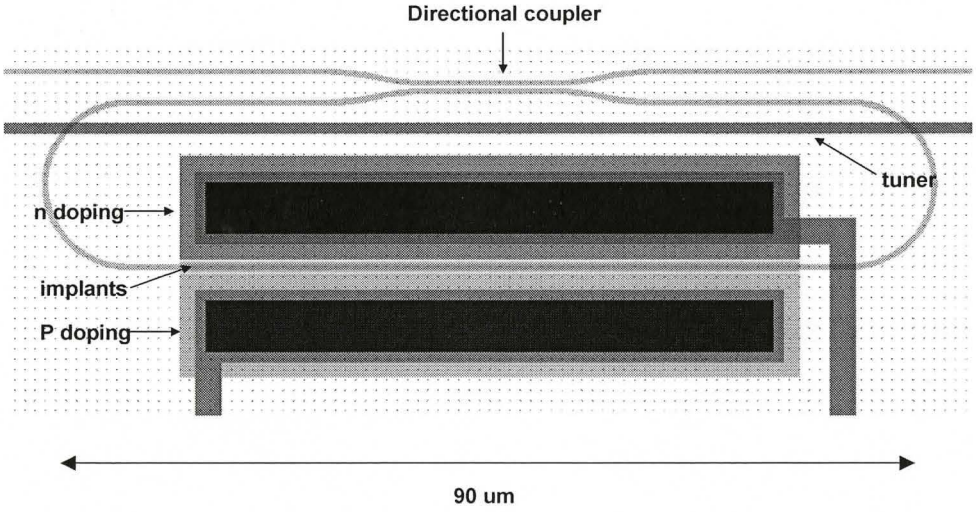


Fig. 5.5: Schematic of ring resonant photodiode. The racetrack-ring structure was coupled to a bus waveguide via a 12 μm directional coupler. The bend radius within the ring was 8 μm, and the overall circumference was 190 μm. The photodiode was 60 μm in length – defects were created by ion implantation only in the waveguide region encompassed by the photodiode.

### 5.3.2 Directional coupler design

The directional coupler was designed to achieve critical coupling to the resonator. Simulation results from RSoft BeamPROP for $k$ versus the gap between waveguides in the directional coupler are shown in Fig. 5.6. Round-trip loss was expected to be approximately 1 dB (20%) and therefore a coupler gap size of 300 nm was chosen as the best candidate for achieving critical coupling. Due to the considerable uncertainty in predicting the round-trip loss, however, coupler gaps ranging from 200 nm to 600 nm were designed into the photomask. Together with the dose sweep used during photolithography as described in section 4.4, this provided sufficient variability between devices to ensure that a close match to critical coupling could be attained.

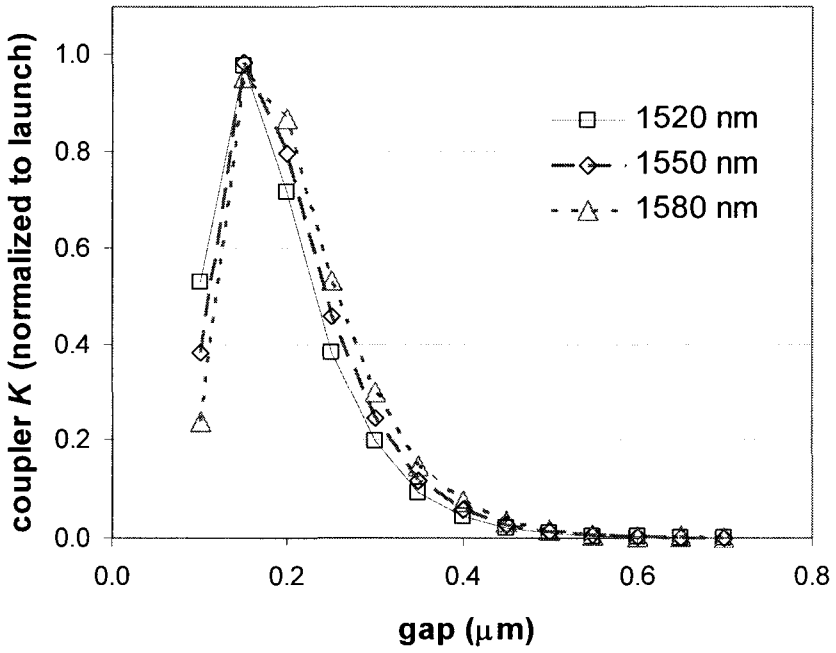


Fig. 5.6: Simulated coupling $k$ as a function of the gap between adjacent waveguides at three wavelengths for the 12 μm directional coupler in the ring resonant structure.

## 5.4 Test setup

The devices were characterized using a tunable laser with a polarization scrambler as the optical source to render the polarization dependent losses at the input grating coupler a known quantity (i.e. 3 dB). The detector was biased using a dc source and the tuner was controlled by a Tektronix AFG310 function generator. Current flow through the tuner was recorded by a Keithley 179A ammeter while photocurrent was recorded by a Keithley picoammeter. The optical output was measured with an ILX FPM8200 power meter. As with the integrated VOA devices described in Chapter 4, the input and output were standard single-mode fibre (SMF) oriented at approximately 10 degrees to the surface of the chip; this ensured that TE polarization only was conveyed into and out of the chip via the grating couplers. The setup is shown in Fig. 5.7.

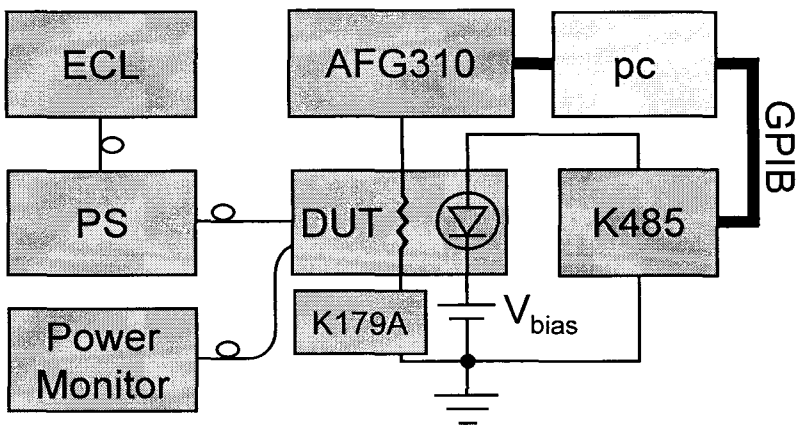


Fig. 5.7: Test setup used to characterize the ring-resonant photodiode. ECL=tunable external cavity laser; PS=polarization scrambler; AFG310=Tektronix AFG310 function generator; K485=Keithley picoammeter; K179A=Keithley ammeter; pc=computer controller using custom LabVIEW code.

# 5.5 Results

## 5.5.1 Test structures

***Straight waveguides***

Fibre-fibre loss at 1550 nm wavelength was measured and found to be 16 ± 1 dB for a test waveguide without ion implantation. As with the devices described in Chapter 4, the overall input-to-output propagation length was 4 mm with propagation losses assumed to be 0.24 dB/mm [179] and grating coupler losses assumed to be 6 dB each together with an additional 3 dB polarization dependent loss at the input [23]. The ring resonators were situated 1 mm from the input coupler, so input loss was calculated to be 3 dB (polarization dependent loss) + 6 dB (grating coupler loss) + 0.24 dB (propagation loss) = 9.25 ± 1 dB. Output losses account for the remaining 6.7 dB (6 dB grating coupler loss + 0.75 dB propagation loss).

***Photodiodes on straight waveguides***

The responsivity (defined as photocurrent divided by on-chip optical power, where on-chip optical power was calculated as input fibre power minus 6 dB grating loss, 3 dB polarization dependent loss, and 0.25 dB waveguide propagation loss prior to the diode) of several 1 mm photodiodes situated on test structures were measured. The devices with the smallest amount of optical loss exhibited responsivity of 0.11 ± 0.02 A/W (with -10 V applied bias) and excess loss due to the photodiode of 4.25 ± 0.5 dB (42.5 ± 5 dB/cm). These data suggest quantum efficiency of 0.09 ± 0.02 for a 1 mm device – a result that corresponds to that reported by Geis *et al.* [101] for a device with 0.25 mm length at -10 V bias, a higher implantation dose, and silicon rather than boron as the implanted ion. Dark current for these devices was less than 1 nA, yielding MDP ≈ 10 nW.

The measured excess loss for the 1 mm photodiode identifies $\alpha \approx 9.8$ cm$^{-1}$; the measured responsivity identifies $\gamma \approx 1.73$ A/Wcm. The maximum possible responsivity of the resonant-cavity photodiode at -10 V bias was therefore expected to be 0.19 A/W according to Eq. (5.18).

***Directional couplers***

Directional coupling for waveguide coupler gaps 300 nm and 350 nm were measured with respect to wavelength and are plotted in Fig. 5.8. In general it was quite difficult to measure the passive couplers due to wavelength-dependent loss which was very pronounced for many of the passive devices (less so for the active devices). The cause of this wavelength "ripple" is unknown but may be due to slab modes which propagate in the SOI being partially recovered at the output gratings. The coupler data presented here were made by sampling upwards of 30 devices for each coupler geometry and averaging the results from those with the least problematic wavelength-dependence.

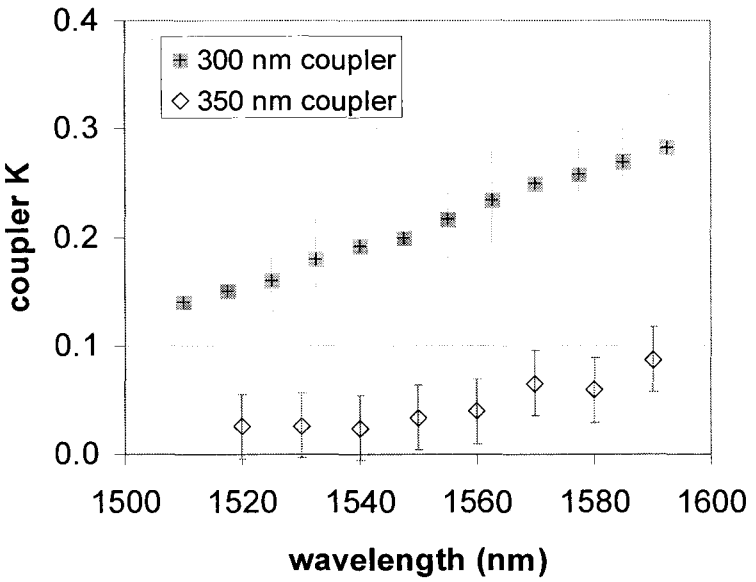


Fig. 5.8: Coupling estimated from passive test structures representative of the directional couplers used in the ring resonator.

The 300 nm gap coupler has $K \sim 0.2$ at 1550 nm while the 350 nm gap coupler has $K \sim 0.02$-$0.07$.

### 5.5.2 Leakage current

A plot of current versus bias voltage for the 12 mm ring-resonant photodiode is shown in Fig. 5.9. The 800 μm channel leveller photodiode of Chapter 4 is included for comparison; since the diodes are identical in every other respect, it is apparent that the leakage current is due to the difference in length.

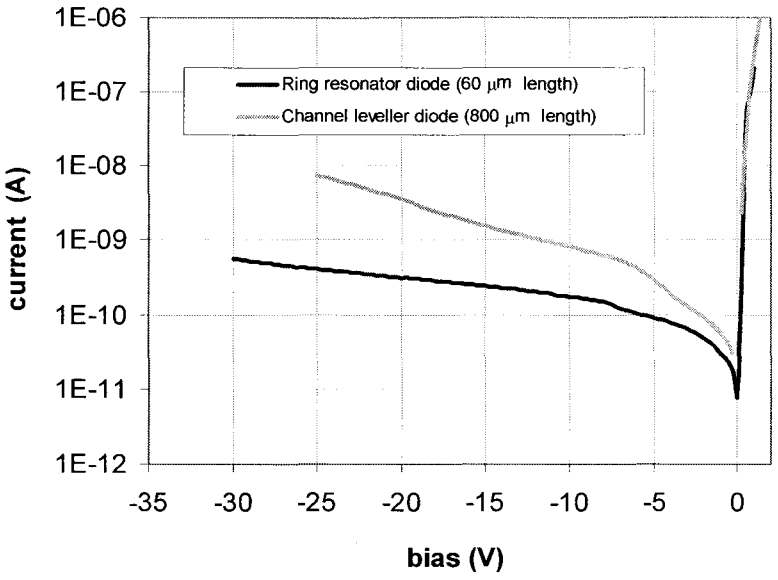


Fig. 5.9: *I-V* plot for the 12 μm ring-resonant photodiode compared to the 800 μm channel leveller photodiode of Chapter 4.

### 5.5.3 Responsivity versus wavelength

The implanted ring resonators that incorporated a directional coupler gap of 350 nm from the "east" side of the wafer were found to have near-critical coupling. These devices will be referred to as "R4". Transmitted optical power (i.e. output from the bus waveguide) and current from the photodiode were measured with

respect to wavelength; a representative plot for R4 biased at -10 V is shown in Fig. 5.10 for three resonant peaks near 1550 nm. The device exhibited optical attenuation of -25 dB at resonance.

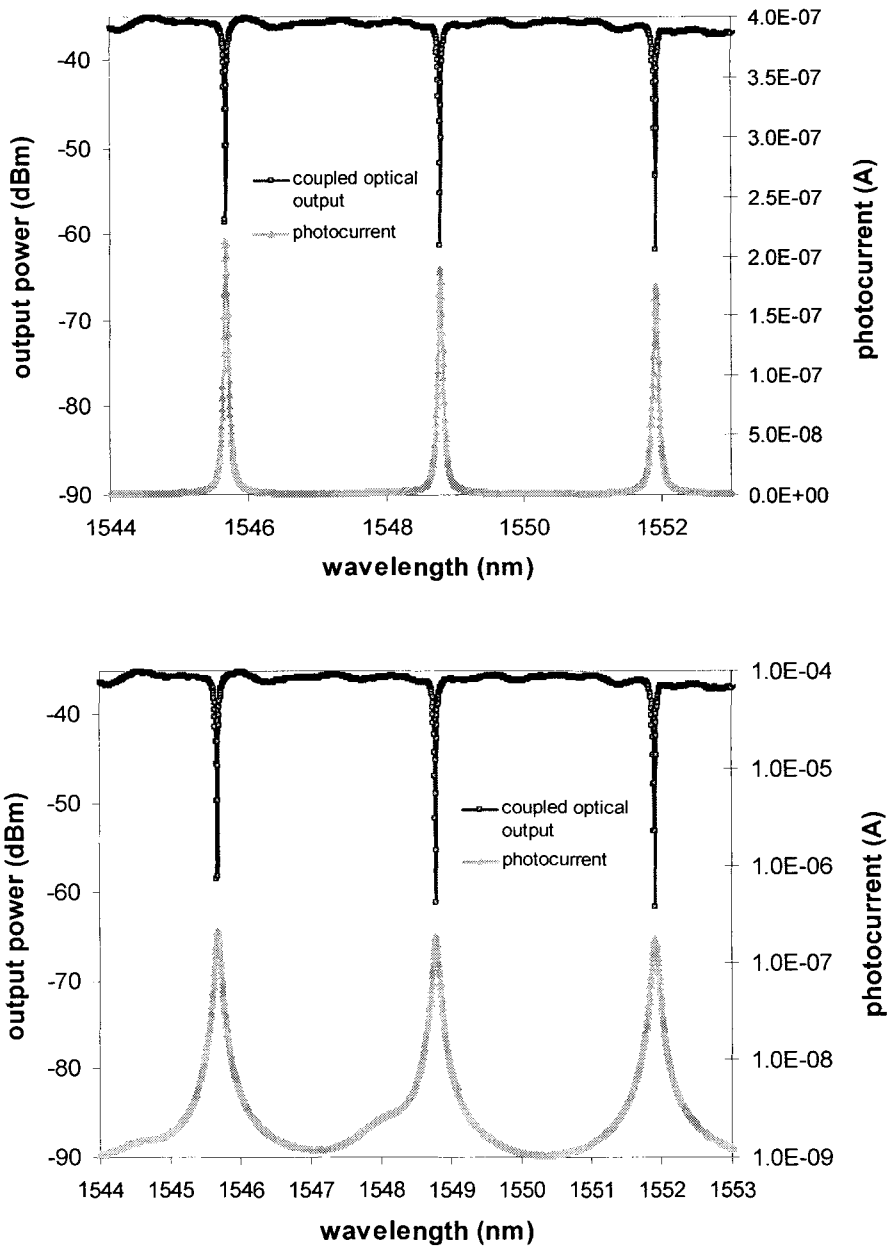


Fig. 5.10: Optical output and photocurrent versus wavelength for R4 at -10 V bias. Input optical power was -18 dBm (off-chip). Upper panel shows photocurrent on a linear scale; lower panel shows photocurrent on a log scale.

The wavelength-dependent "ripple" is clearly visible in both the output power and the photocurrent (log scale) spectra.

***On-chip input power***

Fig. 5.11 shows the peak nearest to 1550 nm in terms of excess power loss (relative to the maximum power off-resonance) and photodiode responsivity. Within the neighbourhood of this resonance peak (wavelengths 1548.5 nm – 1549 nm) the maximum output power was measured to be -36 dBm with fibre input power of -18 dBm. Input grating loss has been estimated as 9 dB (6 dB grating coupler loss and 3 dB polarization dependent loss), waveguide propagation loss as 1 dB (0.24 dB/cm for 4 mm from input taper to output taper) and output grating loss as 6 dB; thus the expected output power was -34 dBm. The remaining 2 dB loss that was measured in this wavelength range was due to the wavelength "ripple". For the analysis which follows it has been assumed that this additional 2 dB loss was divided equally between the input and output gratings; on-chip input power to the ring resonator was therefore calculated as $P_{in\ (on\text{-}chip)}$ = -18 dBm (fibre input) – 6 db (grating loss) – 3 dB (polarization loss) – 1 dB ("ripple") – 0.24 dB (propagation loss for 1 mm distance to ring resonator), for $P_{in\ (on\text{-}chip)}$ = -28.24 dB = 1.5 μW.

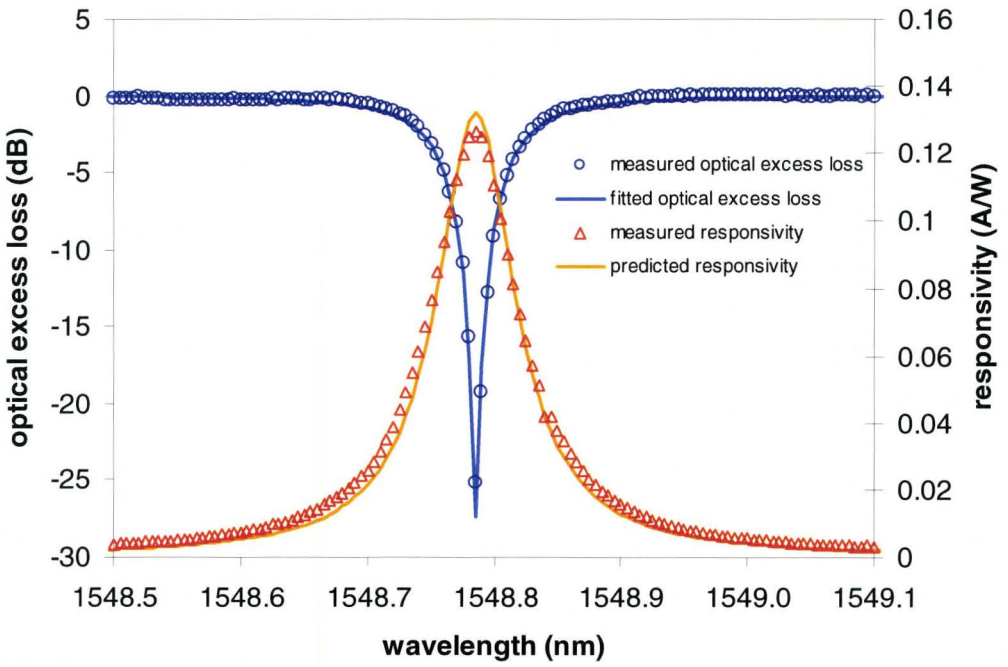


Fig. 5.11: Resonance peak at 1548.8 nm showing the relative attenuation at the output, and the responsivity (relative to on-chip bus input power). A fit of Eq. (5.12) has been used to determine $K$ and $R$ from which the modeled responsivity and $R_\lambda$ is plotted according to Eq. (5.19)

### *Ring round-trip loss and coupling*

The expression from Eq. (5.12) was fitted to the excess loss data (using the value -36 dBm output as the reference power) to determine ring round-trip loss and coupling: these were determined to be 0.075 ± 0.01 (i.e. 0.34 dB round-trip loss, $R$=0.925) and 0.07 ± 0.01 (i.e. $K$=0.07). The inherent ambiguity between round-trip loss and coupling in Eq. (5.12) is irrelevant for cases of near-critical coupling such as the one displayed here since the coupling and loss are equivalent, however for the fit shown in Fig. 5.11 the lower value has been assigned to coupling based on the measurement of the stand-alone coupler shown in Fig. 5.8.

Considering that the calculated round-trip loss (0.34 dB) is a combination of the excess loss due to the implanted defects (estimated to be 0.26 dB for a 60 μm length based on the measured excess loss of 4.25 dB for the 1 mm test diode) and the propagation loss of the waveguide (estimated to be 0.24 dB/mm × 0.2 mm =

0.05 dB) there seems to be an additional component to the round-trip loss of 0.03 dB which may be due to scattering at the waveguide bends.

The resonance peak in Fig. 5.11 exhibits a full-width-half-maximum (FWHM) of 75 pm, corresponding to a Q-factor of 21000.

***Responsivity***

Measured responsivity was calculated as the quotient of measured photocurrent and estimated on-chip input power (1.5 μW) and is plotted in Fig. 5.11. The predicted responsivity (also plotted) was calculated according to Eq. (5.20) using the values derived from the ring output $R$=0.925, $K$=0.07, $r=(R)^{1/2}$, $t=(1-K)^{1/2}$, and the values $L$=60 μm, $L_0$=1000 μm, $R_{\lambda 0}$=0.11 A/W, and $\alpha$=9.8 $cm^{-1}$ derived from the straight-waveguide photodiode results described in section 5.5.1. It is apparent that the model predicts the resonant responsivity of the photodiode very well.

The responsivity at resonance was 0.13 A/W, higher than that achieved for the straight-waveguide 1 mm test device but lower than the maximum possible value of 0.19 A/W predicted by Eq. (5.18). The discrepancy is due to the non-zero propagation loss within the ring apart from the photodiode.

## 5.5.4 Cavity enhancement and MDP

The resonant enhancement factor of the photodiode responsivity was 13.1; the value for true critical coupling calculated according to Eq. (5.16) for $K$=0.07 is 14.3. The discrepancy is due to the fact that the device was not perfectly critically coupled (i.e. coupling was 7% while round-trip loss was 7.5%).

Since the effective responsivity of the device at resonance was 0.13 A/W with leakage current of 0.18 nA, the MDP was calculated to be 1.4 nW. At the same reverse bias the 1 mm straight-waveguide device had lower responsivity (0.11 A/W) and higher leakage current (0.84 nA) for a MDP of 7.6 nW. The resonant

device therefore achieved a reduction in MDP by a factor of 5 together with a reduction in length by a factor of 17 for the photodiode alone or by a factor of 10 for the overall ring resonator.

### 5.5.5 Comparison to other reported results

For straight-waveguide devices with high responsivity, Geis *et al.* reported responsivity of 0.12 A/W and 0.2 μA leakage current (MDP ~ 1.7 μW) for -10 V bias and a diode length of 0.25 mm [101]. Responsivity increased at -20 V bias to 1 A/W, however leakage current increased to 10 μA for a MDP of 10 μW. Also reported by Geis *et al.* were 3 mm devices with leakage current of 10 nA at 0 V bias and responsivity of 0.5 A/W (MDP ~ 2 nW) [102], leakage current of 0.5 nA with responsivity of 0.8 A/W at -5 V bias for a MDP of 0.6 nW [103], and 0.3 mm diodes with responsivity exceeding 50 A/W but high leakage current of 0.1 mA (MDP ~ 1 μW) [103].

For resonance-enhanced devices, reported results include a responsivity of 0.25 mA/W with 2.5 nA leakage current (MDP ~ 10 μW) by Chen *et al.* [98], responsivity of 0.1 A/W and leakage current of 0.1 nA (MDP ~ 1 nW) by Shahifa *et al.* [196], and responsivity of 0.039 A/W with leakage current of 1.1 nA (MDP ~ 28 nW) by Logan *et al* [197].

### 5.5.6 Performance over the *C*-band

Measurements of the photocurrent versus wavelength for the range 1511 nm to 1600 nm are shown in Fig. 5.12 (normalized) overlaid with the relative power throughput for a test straight waveguide.

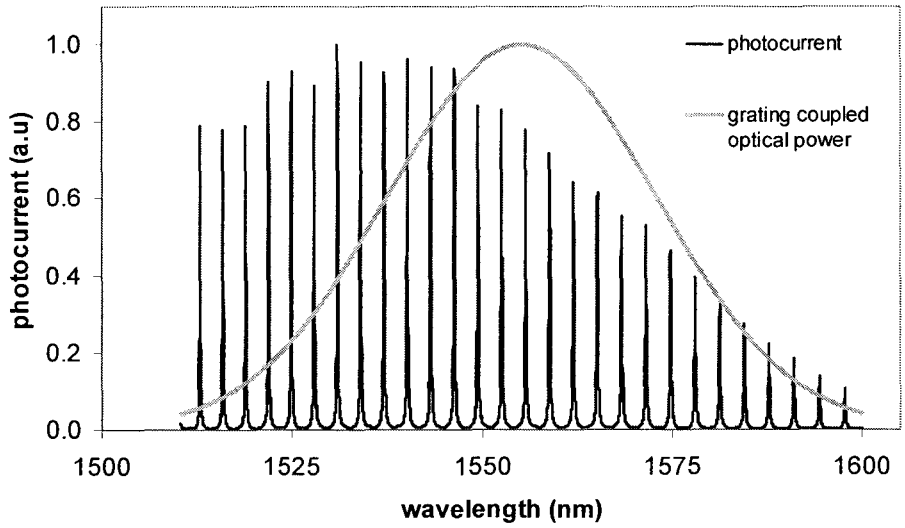


Fig. 5.12: Variation of photocurrent versus wavelength for R4 and corresponding output from a straight waveguide.

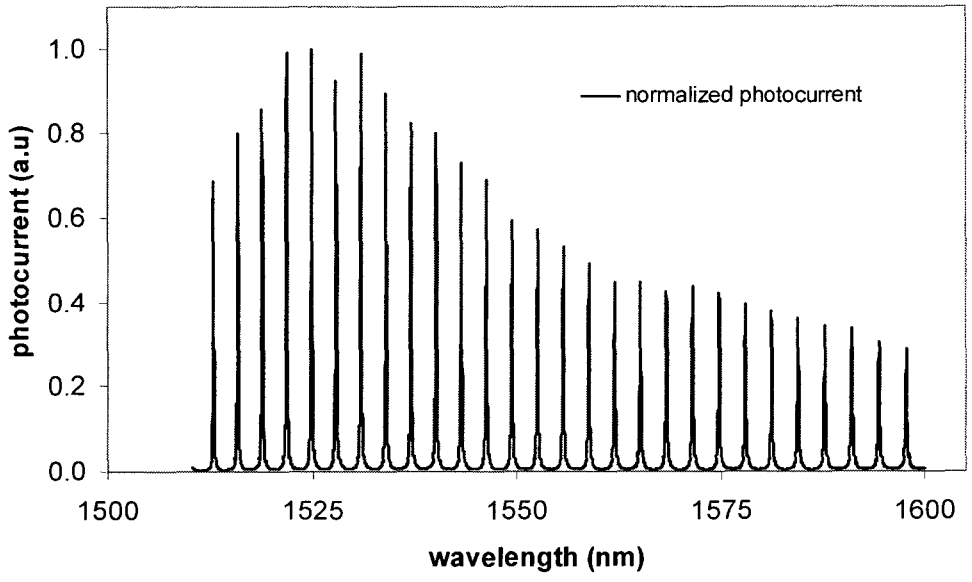


Fig. 5.13: Photodiode signal normalized to the grating response (single grating) and for wavelengths from 1511 nm to 1600 nm.

The wavelength dependence of the straight waveguide throughput is representative of the grating coupler efficiency.

Since the photodiode collects signal coupled through only the input grating, normalization with respect to the square root of the grating function provides an estimate of the ring-resonant detector's wavelength dependence. This result is plotted in Fig. 5.13 and suggests that the responsivity of the device increased at low wavelengths, presumably due to variation of the ring coupling such that it approaches critical coupling more closely (see Fig. 5.8).

### 5.5.7 Tuning

The ring phase was tuned thermo-optically by applying bias to the resistive metal trace which overlaid the ring resonator. Originally the device was tuned in this manner while the silicon substrate was in good thermal contact to the fixture beneath. A plot of tuning relative to the free spectral range (FSR) is shown in Fig. 5.14.

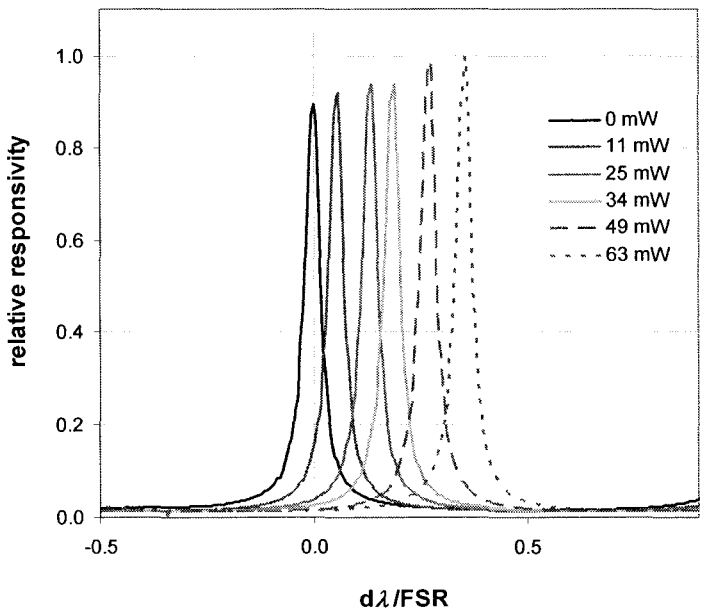


Fig. 5.14: Resonance tuning near 1550 nm with silicon substrate thermally grounded to the fixture beneath. The horizontal axis represents the change in wavelength relative to the free spectral range.

A plot of phase versus electrical tuning power is shown in Fig. 5.15.

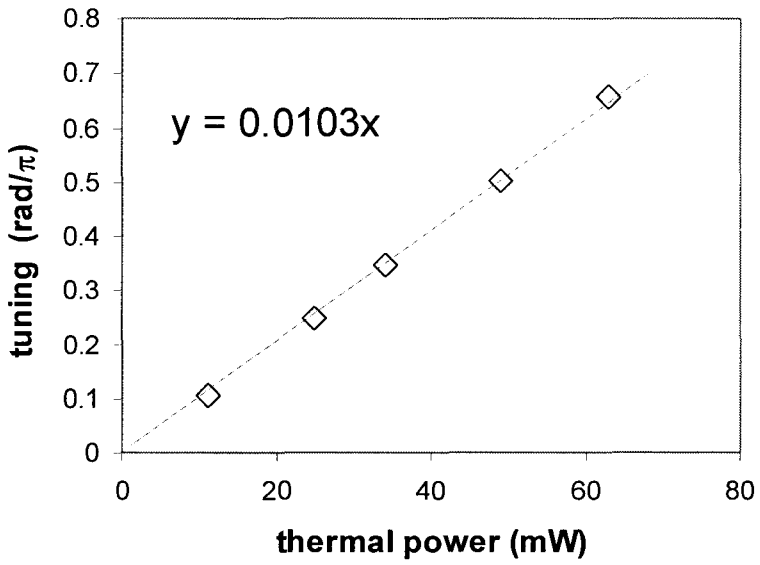


Fig. 5.15: Thermal tuning phase vs. thermal power for poor thermal isolation. Thermal tuning efficiency of 100 mW/π was measured.

The measured thermal tuning efficiency was approximately 100 mW/π, less than half as efficient as the tuning described in the previous chapter for an MZI structure. The difference can be attributed to the fact that much of the tuner was not situated near the waveguide in the ring resonant design, thus dissipating considerable thermal power into the substrate rather than the waveguide.

The thermal tuner was not able to sustain more than 80 mW for more than a few minutes before becoming an open circuit. A number of devices were meticulously destroyed in this manner before the decision was taken to apply thermal isolation (in the form of electrical tape) to the underside of the chip, thus increasing the thermal resistance to ground to preserve a larger temperature on the chip. With this precaution in place, thermal efficiency was improved dramatically such that tuning over a full free spectral range was achieved. The tuning spectrum and efficiency plot are shown in Fig. 5.16. The tuning efficiency was more than doubled via thermal isolation to 44 mW/π, however the high tuning values could only be sustained for a few seconds at a time.

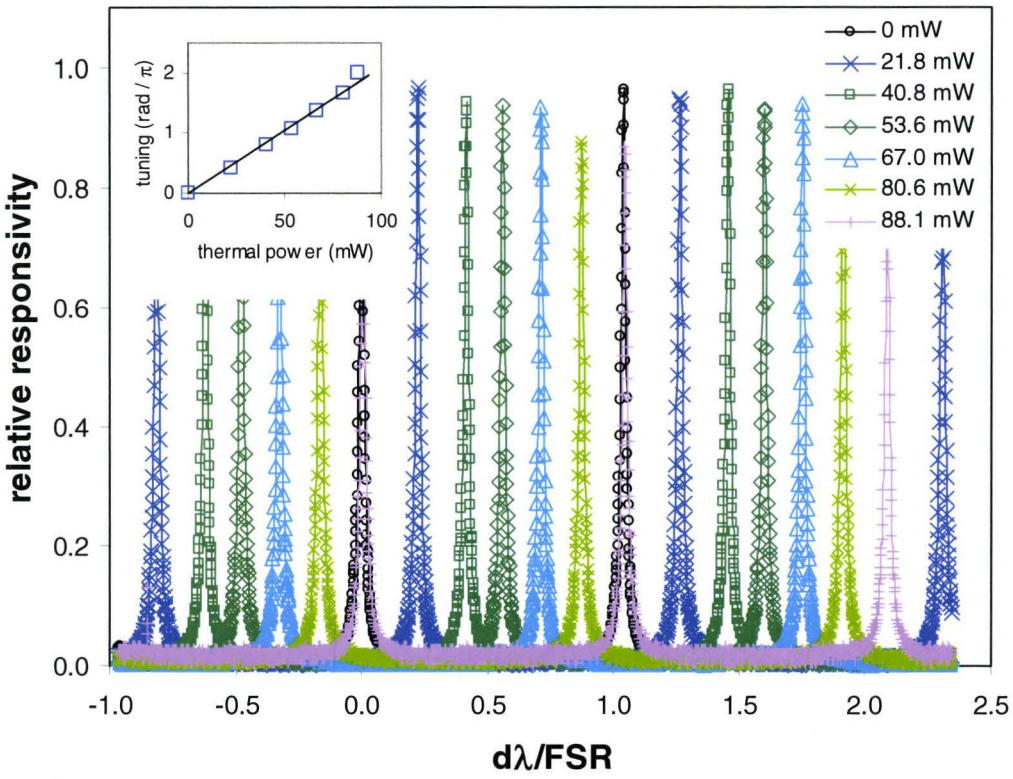


Fig. 5.16: Tuning of the resonance wavelengths for R4. The inset shows tuning efficiency.

With the capability to tune the device through one full free spectral range it is possible to align a resonance peak with any wavelength in the *C*-band. Together with the 25 dB extinction ratio achievable by tuning the ring to resonance, the device functions as an optical switch with integrated monitoring.

# 5.6 Suggested improvements

## 5.6.1 Tuning efficiency

Although thermal isolation was shown to improve the tuning efficiency, this approach necessarily limits the tuning speed by increasing the thermal *RC* time constant of the device. An alternative approach is to widen the resistive metal trace in regions not adjacent to a waveguide so as to avoid wasted thermal power.

## 5.6.2 Bandwidth

At near-critical coupling the detector is inherently bandwidth limited (the full-width-half-max in this case was 9 GHz). By designing the resonator to be over-coupled instead, the bandwidth constraint is relaxed at the expense of responsivity. This can be achieved by increasing $K$ of the directional coupler without altering the round-trip loss.

Alternatively, critical coupling can be retained together with higher ring round-trip loss, e.g. by increasing the defect density within the photodiode and altering the directional coupler to maintain $K = 1\text{-}R$. Assuming that the ratio $\gamma/\alpha$ (i.e. the internal quantum efficiency) remains unaffected, Eq. (5.18) suggests that responsivity can be maintained. MDP, however, is degraded since the increased defect density worsens leakage current, while overall responsivity remains unchanged.

## 5.7 Chapter summary

A tunable ring-resonant defect-mediated photodiode has been demonstrated for the first time in silicon. The device exhibited a minimum detectable power of 1.4 nW, responsivity of 0.13 A/W, and resonant enhancement by a factor of 13 at 1550 nm. The device was shown to operate across the entire *C*-band since resonances were tunable across a full free spectral range. Tuning efficiency and performance versus wavelength were measured. Modeling and theoretical considerations were used to show that a resonant detector can approximate a straight-waveguide detector of infinite length.

# Chapter 6

# Conclusions

Defect-mediated photodiodes in silicon offer a unique benefit: the option to insert optical monitoring and control capability within a photonic circuit. The work described in this thesis was performed in pursuit of two goals: (1) to shed light on the defects and mechanism involved in the operation of silicon photodiodes fabricated by ion implantation for use at wavelengths in the *C*-band; and (2) to demonstrate their potential for monolithic integration.

## 6.1 Defect characterization

With respect to the goal of examining the underlying physics of defect-mediated photodiodes, various standard defect characterization techniques (DLTS, TSCAP, and C-V profiling) were implemented and employed to assess the defects present in ion-implanted test structures in comparison to the performance of identically ion-implanted waveguide photodiodes. While several defects were observed and characterized in this manner, their participation in the optical absorption process was unclear. Accordingly, modifications of the standard techniques were

employed. These included optical DLTS using optical fibre and a laser for pulsed stimuli and a new technique based on TSCAP in which the equilibrium between thermal and optical excitation of the defects of interest was exploited to deduce photoionization cross-sections and to confirm ionization energies. The results obtained via these techniques provided strong evidence that the dominant mechanism of optical absorption for low ion implantation doses is photoexcitation of an electron from the valence band to the $E_c$-0.4 eV energy level of the divacancy. The involvement of an unidentified deep donor state was also observed. An attempt to characterize the depth profiles of the defects yielded results that leant credence to the idea that the divacancy can be present well beyond the projected ion range of the implantation, particularly after annealing.

The waveguide-based photodiodes used for comparison with the defect-characterization samples were fabricated from commercial variable optical attenuator devices. This is an item of note in and of itself: commercial devices intended for one purpose were converted to serve an entirely different purpose by means of a single ion implantation step. The high quality and uniformity of the devices thus obtained enabled characterization with respect to optical loss and responsivity as a function of implantation dose and annealing temperatures.

## 6.2 Device integration

Ultimately, the key advantage of defect-mediated photodetectors (and of all silicon photonic devices) rests in their inherent potential for monolithic integration. As a demonstration of this capability, devices combining optical detection and power control capability were fabricated in a standard CMOS facility without recourse to any non-standard processing steps. The devices were first demonstrated as optical attenuators with built-in monitoring capability, and then demonstrated with a feedback loop as independently-operating optical power

levellers. This was, without question, one of the most satisfying elements of the project.

Photodiodes were also integrated with tunable ring resonators so as to demonstrate both resonant-cavity enhanced responsivity and an alternative form of optical switching with built-in power monitoring. Devices operating at nearly perfect critical-coupling were achieved and exhibited resonant enhancement approaching the theoretical optimum.

## 6.3 Further work

### 6.3.1 Deep donor states

It was noted with great interest that while a deep acceptor state played the strongest role in optical absorption at 1550 nm, a signal from a deep donor state was also present. The characterization of this defect presents a considerable challenge since it was almost entirely masked by the signal from the divacancy (i.e. the deep acceptor). However, concentration calculations suggest that this defect was present in sufficient numbers in a high-dose boron-implanted sample to compensate a considerable fraction of the divacancy signal. An investigation into the identity of this defect might best be carried out through the use of ion implantation at even higher doses.

### 6.3.2 Bistability

Geis *et al.* [102] have reported bistable operation of photodiodes: high current densities under forward bias can change the behaviour of the defects for days or even weeks at a time. ECS and DLTS techniques applied to such devices before and after forward bias could elucidate whether the bistability is due to the creation

of new defects which later dissociate or to changes in the occupancy of defects already present.

### 6.3.3 SOI-specific characterization

It is not clear whether the characterization of defects produced in bulk silicon can be applied without caveats to those produced in SOI. It is entirely possible that implantation through the SOI layer – as was done with the boron-implanted samples in this work – causes differences due to the absence of the implanted species (or interstitials, in the case of self-implantation) in the region of interest. This is notoriously difficult to test with conventional DLTS due to the need for a simple exponential transient; however the ECS technique can potentially be used for this purpose since the measurements are carried out at steady-state. In particular, the constant-capacitance approach could be employed for rectangular devices oriented laterally in the SOI layer and optically illuminated from above.

### 6.3.4 Device integration

The channel leveller demonstrated in this work incorporated all the photonic functions on-chip, but the feedback loop was provided off-chip. Since the feedback loop mimicked a simple circuit, a fully autonomous device could be made in which the circuit is integrated directly on the chip. This would be a key demonstration of the benefits of monolithic electronic and optical integration. With modification the circuit could be made to overcompensate such that increased optical input produces decreased optical output – a form of "negative resistance" in the optical domain. A device of this form would open up the possibility of self-contained optical oscillators – devices which, with the supply of uniform optical input power, produce a time-varying optical output of a specific frequency.

The ring resonant devices also present a number of interesting possibilities. One can envision the use of several such devices operating in an array such that each is resonant at a particular wavelength to form a digital spectrometer with unparalled compactness, no moving parts, electronics included on-chip, and fabrication without recourse to any exotic fabrication steps.

## 6.4 Future of silicon photonics

It has long been the hope of professionals in the optics industry that the field will replicate the successes of the electronics industry seen during the latter half of the 20$^{th}$ century. Silicon photonics is the incarnation of that hope, and there are many striving to become to photonics what Jack Kilby, Robert Noyce, and John Bardeen were to electronics.

One often hears silicon spoken of as the material that isn't much good for optics – even by those within silicon photonics. Certainly silicon would not have been the first choice in many respects, but the joy of engineering isn't in making things that are straightforward. As has repeatedly been demonstrated in this field during the first decade of the new century, no material problem can long obstruct a will to succeed, creativity, and sheer love of a challenge.

From the standpoint of a student, one could not have asked for a better mix of practical purpose and fundamental physics.

# Appendix A

# Photolithography

## A.1 Photoresist recipes for o-DLTS sample fabrication process

### A.1.1 Shipley 1827

Shipley 1827 is a positive photoresist which can be used when thick photoresist is required. It was used in this work as the mask for the 100 keV phosphorus implantation step.

Process:

- spin: 2.2 krpm, 30 seconds
- soft bake: 100 C, 2 minutes
- exposure: 40 seconds 365 nm at 6 mW/cm$^2$

- develop: Microposit 351 diluted 1:5 (i.e. 1 unit developer : 5 units water); develop time is approximately 40 seconds.
- hard bake: 100 C, 2 minutes.
- thickness: $4 \pm 0.5$ μm.

### A.1.2 Futurrex NR9

Futurrex NR9 is a negative photoresist. It was used in this work for the contact deposition lift-off process in order to use a light-field photomask so that the devices could be viewed during alignment.

Process:

- spin: 3 krpm, 40 seconds
- soft bake: 150 C, 60 seconds
- exposure: 110 seconds 365 nm at 6 mW/cm$^2$
- post-exposure bake: 100 C, 60 seconds
- develop: Futurrex RD6; develop time is approximately 15 seconds.
- thickness: $3 \pm 0.5$ μm.

## A.2 Photomasks used for o-DLTS fabrication process

The photomasks used for o-DLTS sample fabrication were manufactured by the University of Alberta NanoFab. The masks were 5" x 5" laser-patterned chrome on soda-lime glass; since the SUSS MA6 mask aligner could not accommodate

this mask size, masks were diced to 4" x 4" size at the University of Western Ontario prior to use. The minimum feature size was 5 μm.

The initial mask design used is shown in Fig. A.1. The lowermost tile was used for the dopant implantation step to define the diodes; the rightmost tile was used for the contact lift-off step. Alternate diode sizes were included on the central and upper tiles but were not used. The left-most tile was used for work not described in this thesis. Each tile included 9 sets of alignment marks distributed around the perimeter.

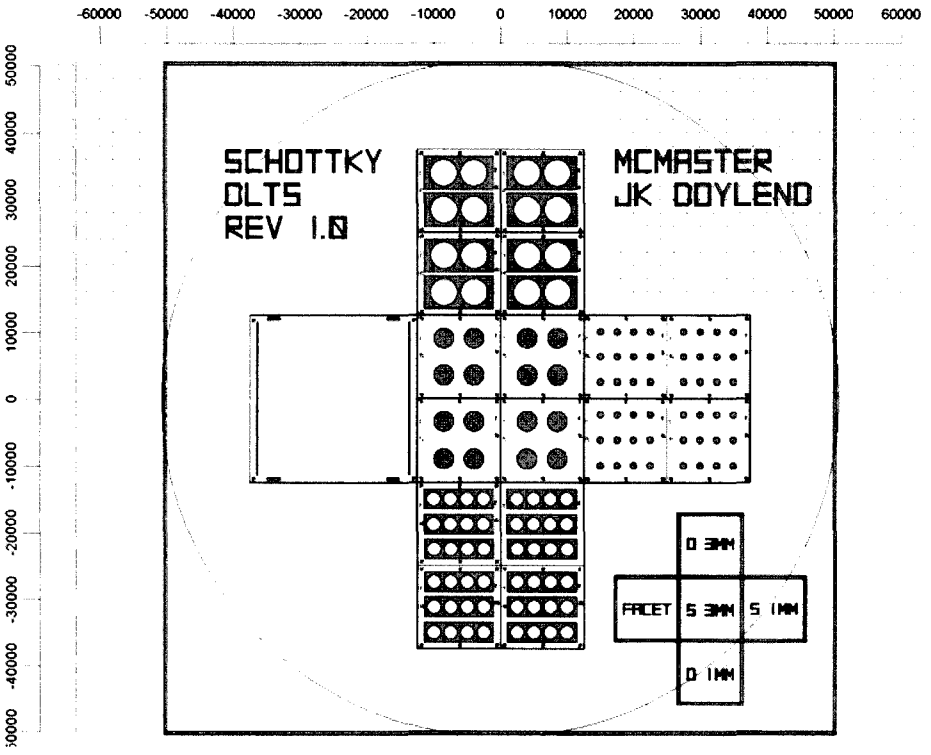


Fig. A.1: Original photomask used for o-DLTS diode fabrication. Shaded areas indicate glass; unshaded areas indicate chrome.

Difficulties were encountered during the photolithography for the metal lift-off step due to the poor visibility afforded through the contact pattern tile (rightmost). Tiles on a second mask (designed for an unrelated purpose) were allocated for use with a negative photoresist process at the contact lift-off step. The dopant

definition and contact definition tiles on this second mask are shown in Fig. A.2 and Fig. A.3 respectively.

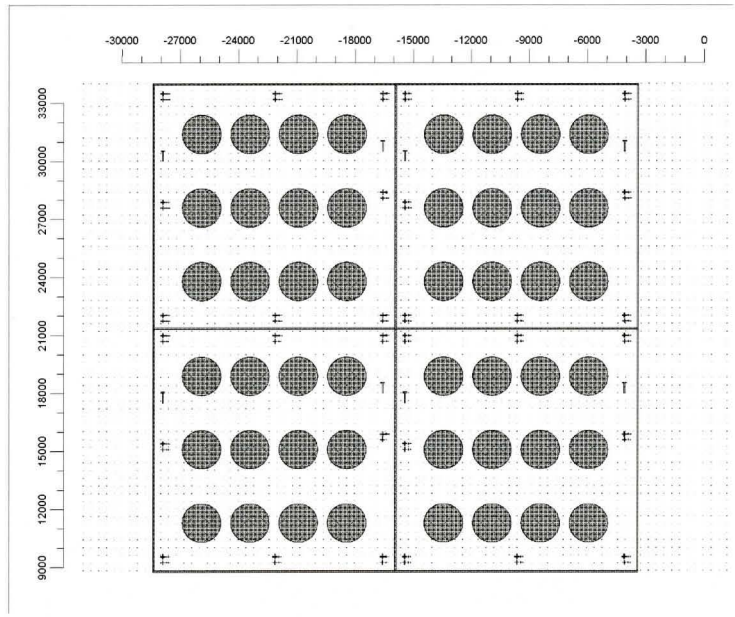


Fig. A.2: Second dopant window mask tile. Shaded areas indicate glass, unshaded areas indicate chrome.

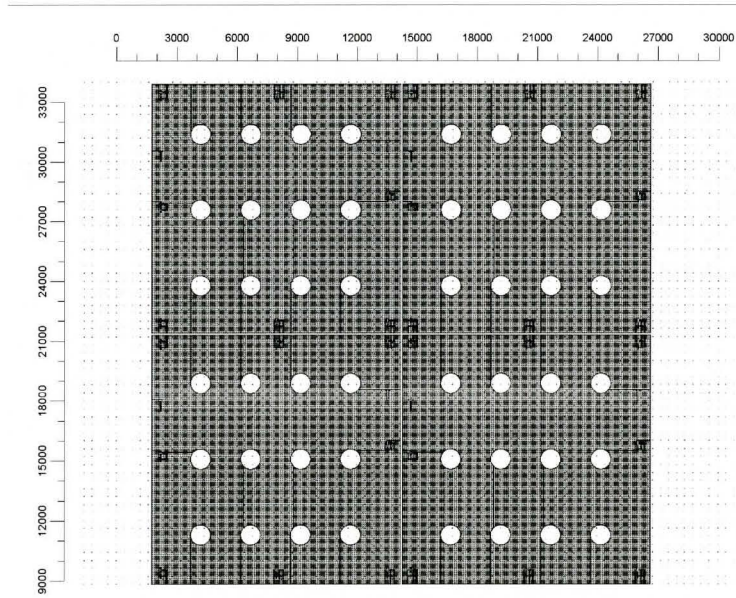


Fig. A.3: Second contact lift-off mask tile. Shaded areas indicate glass; unshaded areas indicate chrome.

# A.3 Photomasks for LETI fabrication process

Manufacturing of the masks designed for use at LETI to fabricate the integrated VOA and ring resonator devices described in this work were coordinated by CMC Microsystems. The mask designs for each layer are shown in Fig. A.4 - Fig. A.10.

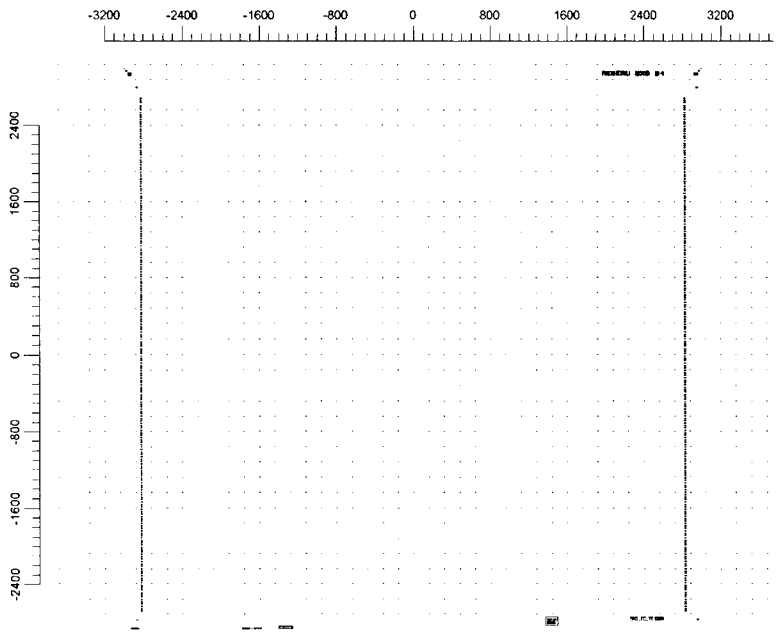


Fig. A.4: LETI mask grating layer.

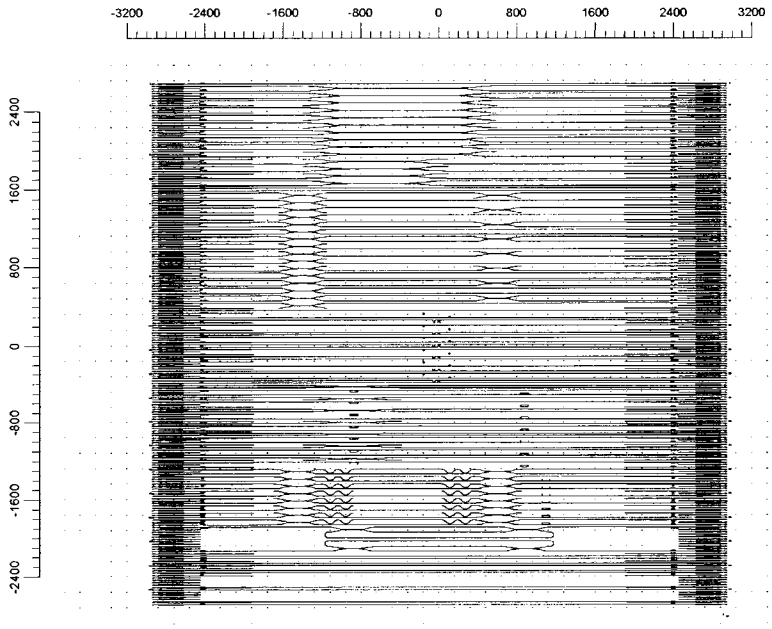


Fig. A.5: LETI mask, rib layer.

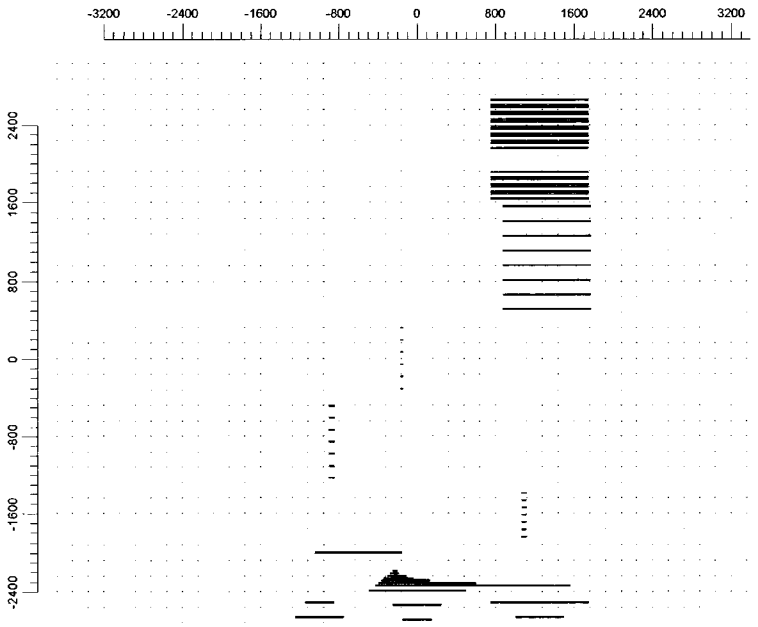


Fig. A.6: LETI mask, *p*-type dopant layer.

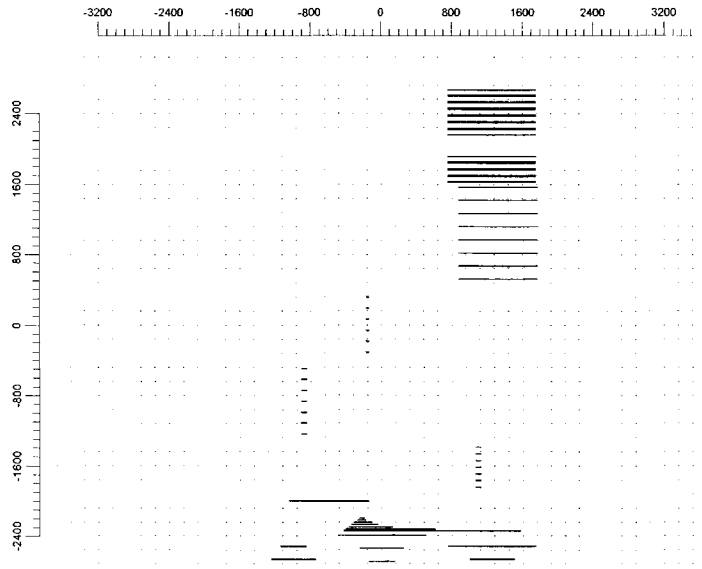


Fig. A.7: LETI mask, *n*-type dopant layer.

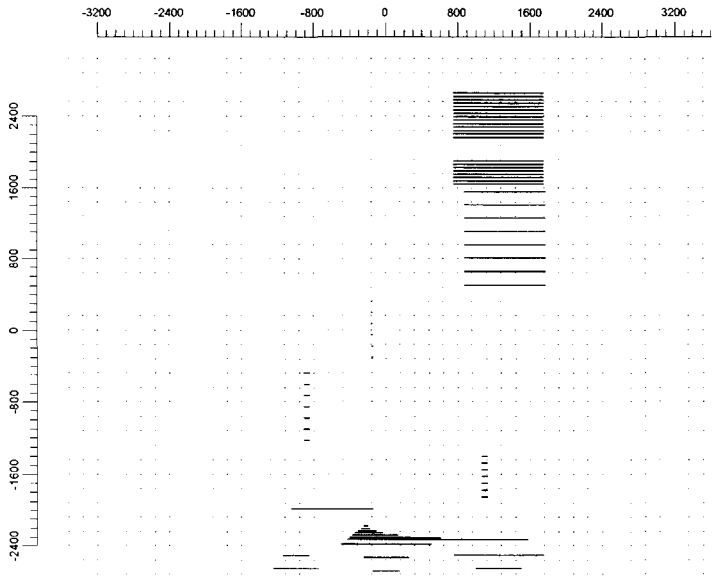


Fig. A.8: LETI mask, via layer.

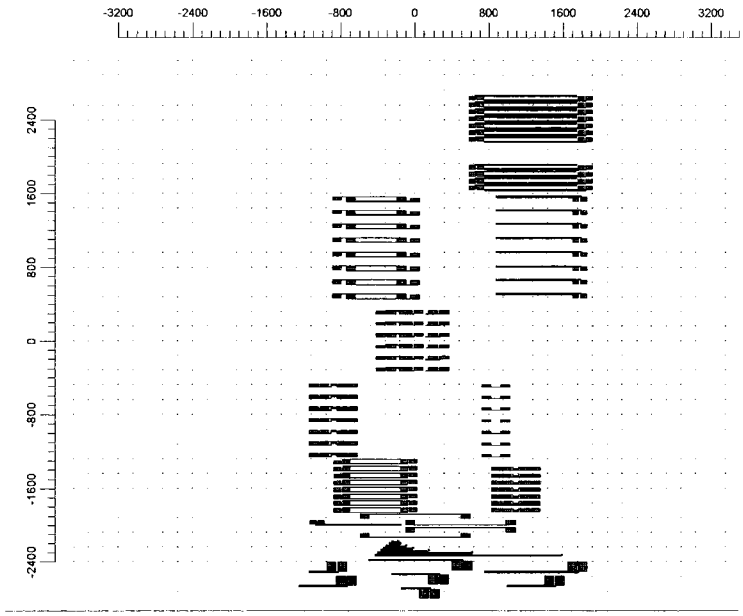


Fig. A.9: LETI mask, metal contact layer.

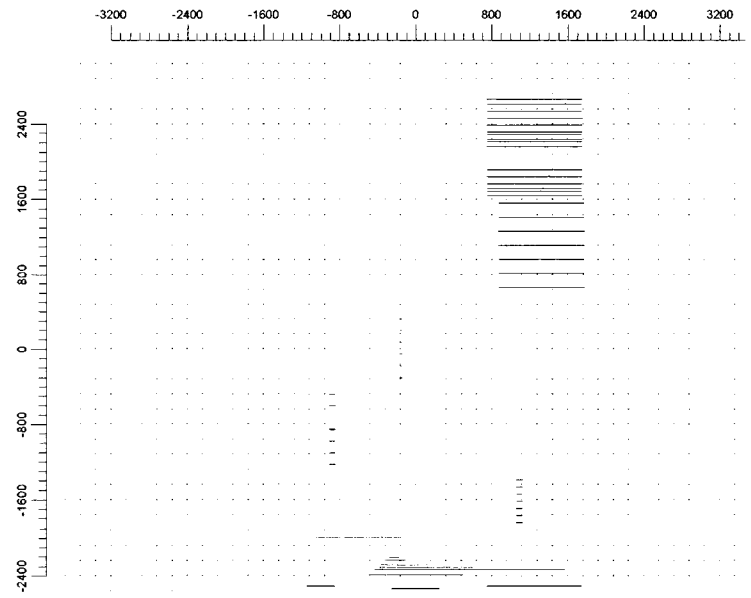


Fig. A.10: LETI mask, ion implantation layer.

# Appendix B

# Determination of photon flux density for ECS measurements

## B.1 Optical beam profile

Since the beam from an optical fiber diverges rapidly in free space, it was necessary to characterize the optical intensity at the distance from the fibre tip corresponding to the location of the test sample. A measurement was also performed to assess the variation of beam intensity across the width of the sample.

The measurement was performed by mounting the fibre on a translation stage with the fibre tip positioned 5 cm from the input of an ILX Lightwave FPM8200 power meter. An Agilent 8164A external cavity laser was used as the 1550 nm source. An attachment connected to the input of the power meter provided a small-area circular aperture such that the measured power could be converted to

irradiance. The fibre tip was then moved laterally and the variation in irradiance was recorded in order to characterize the beam profile. The setup is illustrated in Fig. B.1.

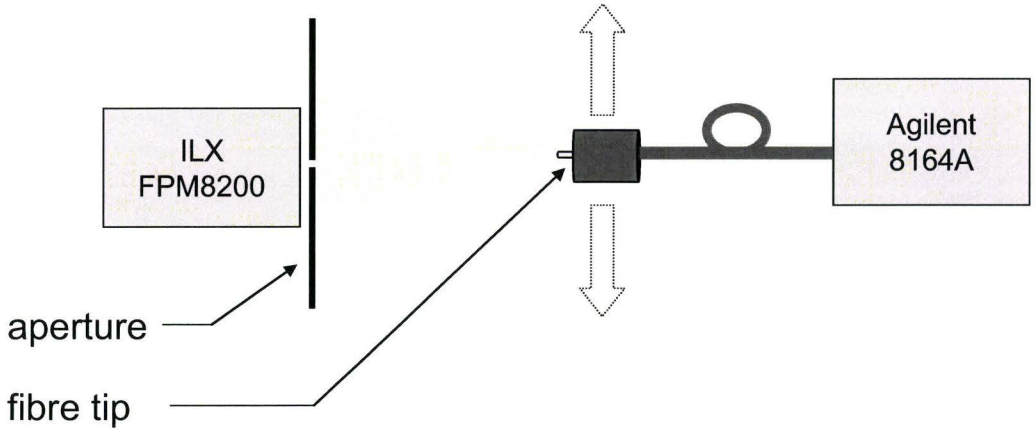


Fig. B.1: Setup for beam profile measurements. The fibre was moved laterally with respect to an aperture attached to the power meter.

The aperture diameter was measured by fitting it to drill bits: a size #75 (0.021" diameter) was found to fit inside the aperture while size #74 (0.0225" diameter) was too large; the diameter of the aperture was therefore estimated to be 0.55 ± 0.02 mm. The drill bit diameters were verified using a micrometer.

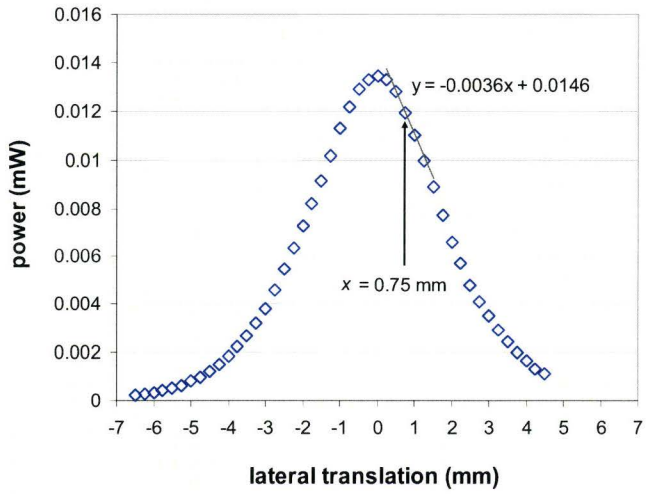


Fig. B.2: Measured optical power at 1550 nm through a 0.55 mm diameter aperture at 5 cm distance from the optical fibre with 1 mW optical fibre output. The variation of optical power at

the location corresponding to the exposed region of the diode ($x$ = 0.75 mm) was assessed by a linear fit.

Measurements of optical power filtered through the aperture were recorded at 1550 nm wavelength while the fibre for a 10 mm lateral scan. The measured beam profile is shown in Fig. B.2. Irradiance was calculated by dividing measured power by the aperture area.

# B.2 Calculation of average photon flux density at the diode

## B.2.1 Average irradiance corresponding to the exposed region of the diode

In the optical ECS and DLTS measurements the 2 mm diameter diode was illuminated from above, with the 1 mm diameter metal contact shadowing its centre. The region exposed to the illumination was therefore from $r$ = 0.5 mm to $r$ = 1 mm for radius $r$ measured laterally from the axis of the beam. The irradiance was calculated for three radii: 0.5 mm, 0.75 mm, and 1 mm from the data shown in Fig. B.2, and a linear fit was used to interpolate the intensity for the exposed 0.5 mm annulus. Integrating the irradiance over the annular area of the exposed region of the diode and dividing by the total annular area yielded a value for the average irradiance of 4.9 mW/cm$^2$.

## B.2.2 Optical reflections

Fresnel reflection losses at the glass window of the cryostat (refractive index ~ 1.4) and the surface of the silicon chip (refractive index ~ 3.5) reduced input

optical intensity by a factor of 0.67. Optical power transmitted into the chip was assumed to be reflected at the bottom surface (gold-coated backside contact) with near 100% efficiency. Since the backside surface of the chip was unpolished it was assumed that the reflections were incoherent and therefore interference effects were neglected. The intensity enhancement at the junction due to the infinite series of reflections between the backside contact and the upper surface of the chip exactly cancels the Fresnel loss of the incident beam at the silicon/air interface so the overall calculation for the photon flux density of the beam just below the surface of the chip yields a factor of two due to the backside reflections.

### B.2.3 Photon flux density

Average photon flux density for the exposed area of the junction was calculated according to Eq. (B.1):

$$\Phi = 2\frac{I_{meas}}{h\nu} \tag{B.1}$$

where $\Phi$ is the average photon flux density, $I_{meas}$ is the average optical irradiance, $h\nu$ is the photon energy, and the factor of 2 accounts for reflections.

# Appendix C

# LabVIEW code

## C.1 DLTS system

The LabVIEW VI at the heart of the DLTS system is shown in Fig. C.1 and Fig. C.2. The subVI which filters the transient according to the selected rate windows is shown in Fig. C.3. The subVI which records and crops the transient, applies noise filtering and averaging, and calculates capacitance values from the recorded voltage points is shown in Fig. C.4.

## C.2 Channel leveller

The LabVIEW VI which mimics an electronic feedback loop between the photodiode and the VOA is shown in Fig. C.5.

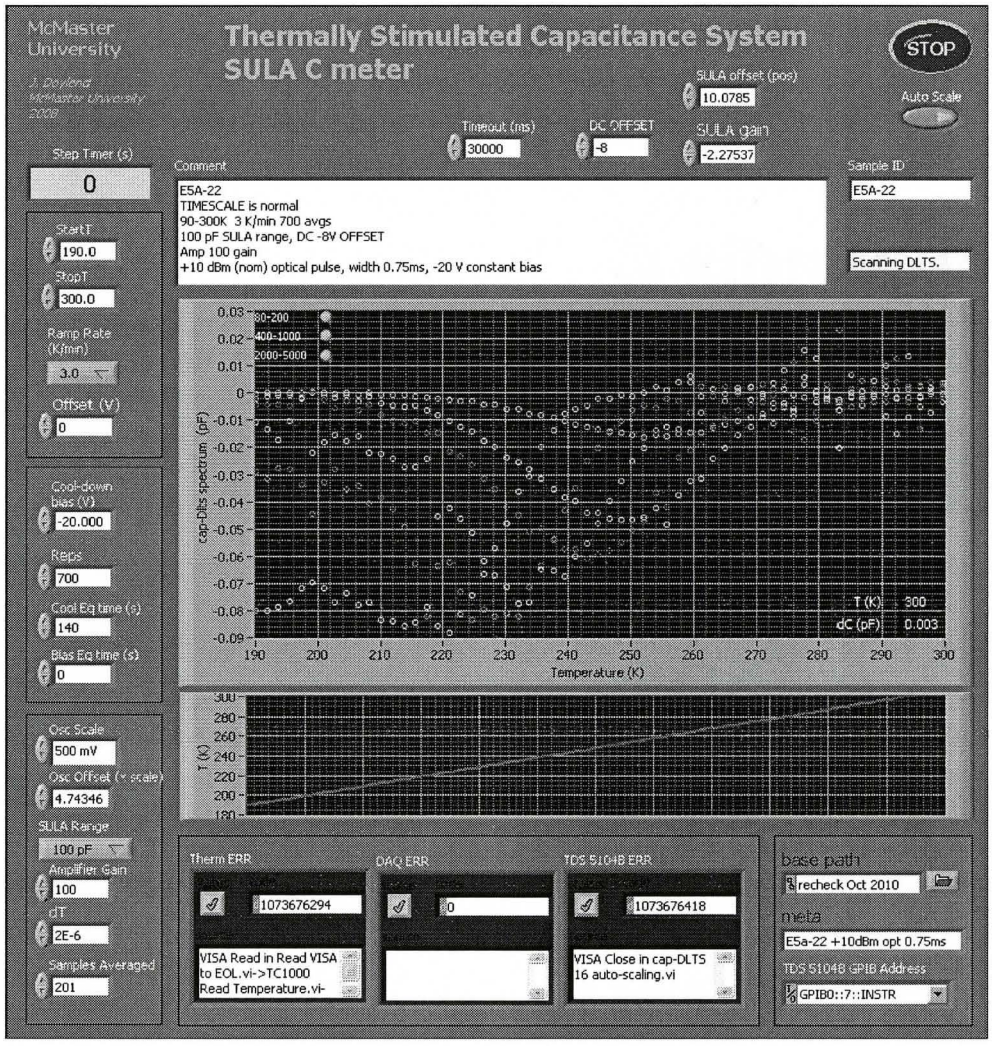


Fig. C.1: DLTS system software: front panel.

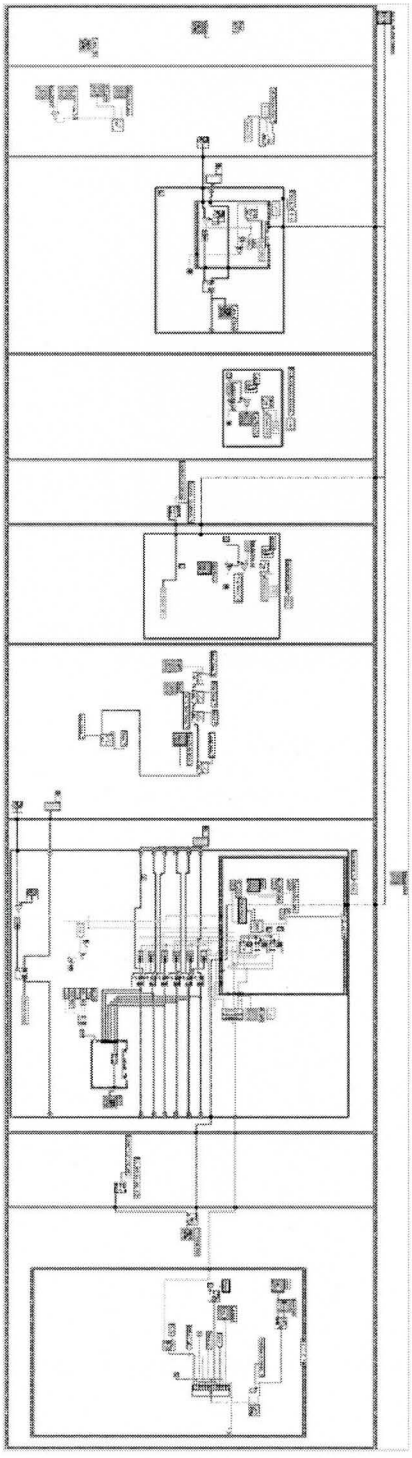

Fig. C.2: DLTS system software block diagram.

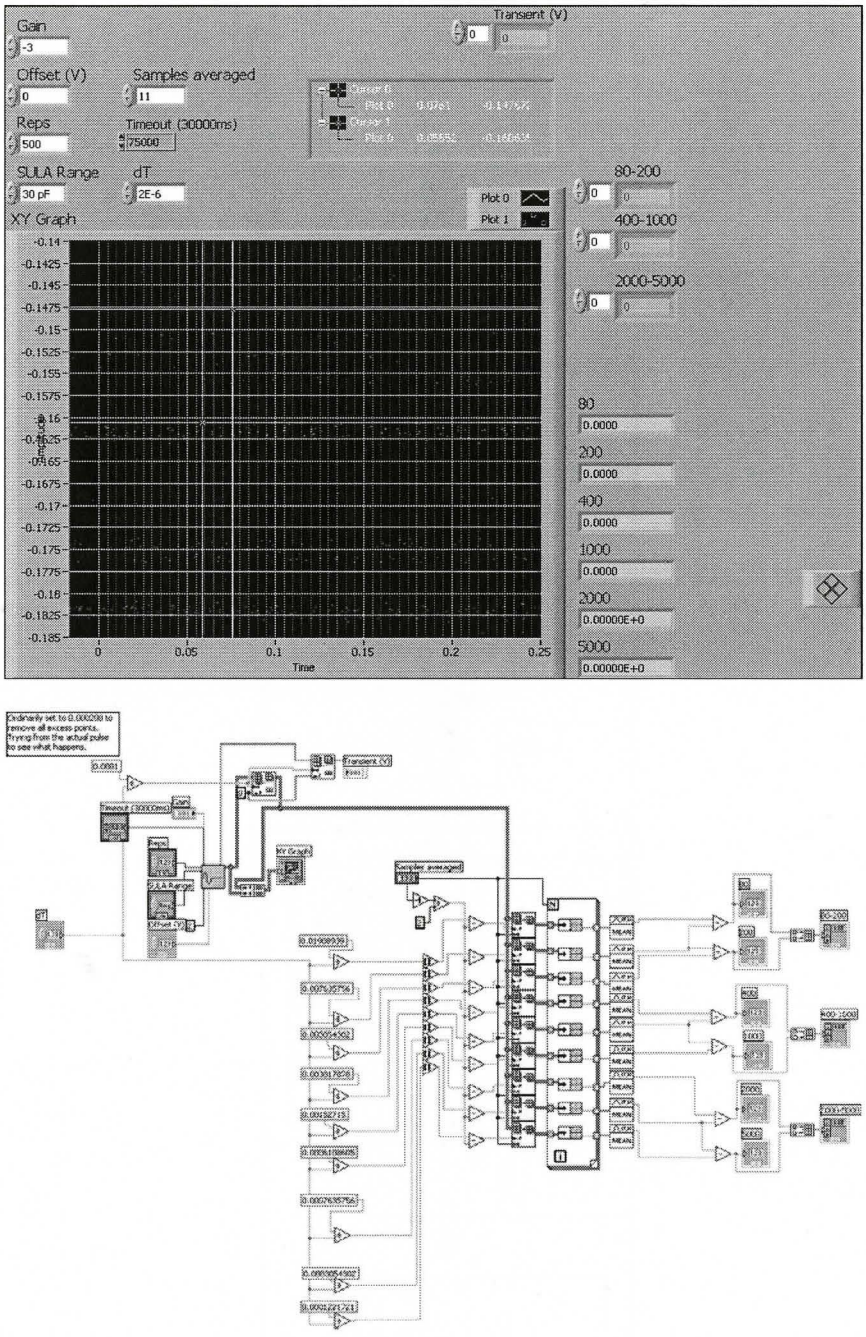


Fig. C.3: Rate window filter subVI front panel (top) and block diagram (bottom).

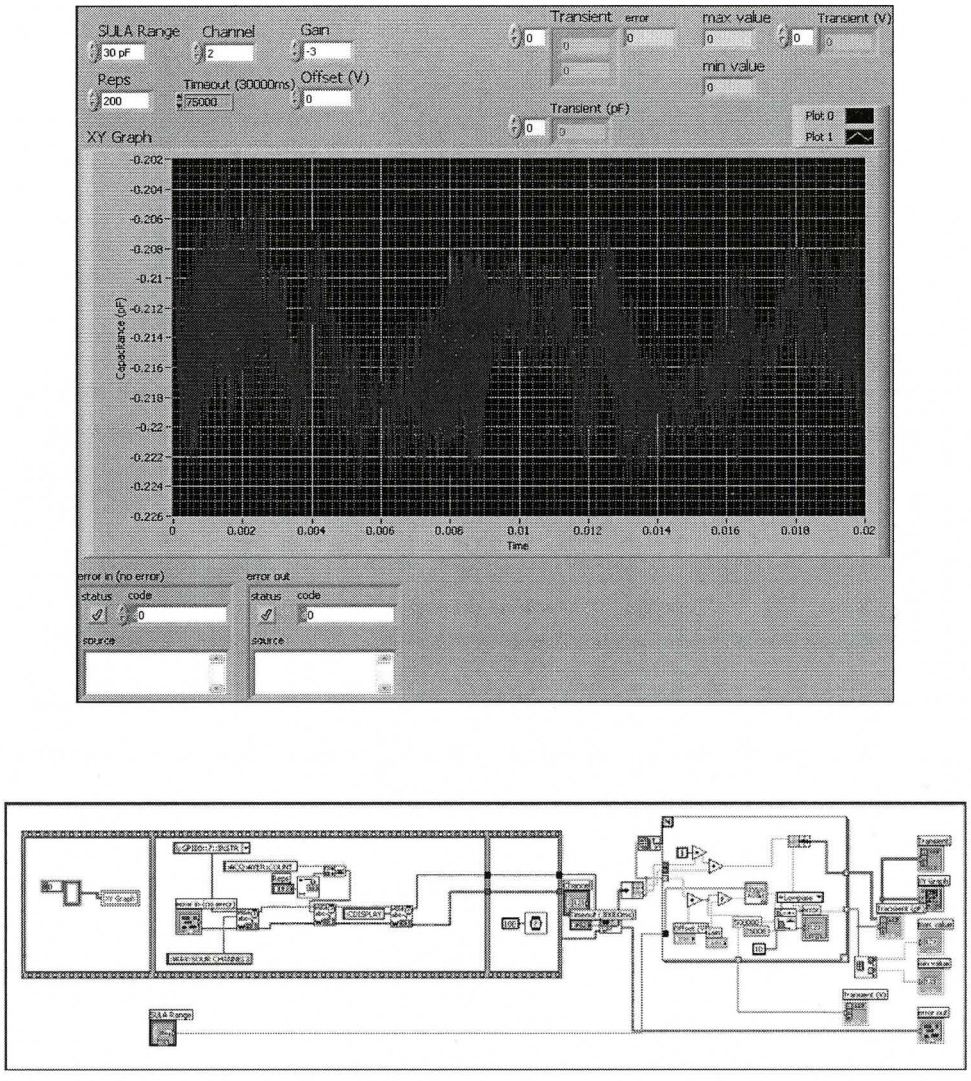


Fig. C.4: Capacitance ransient processer subVI front panel (top) and block diagram (bottom).

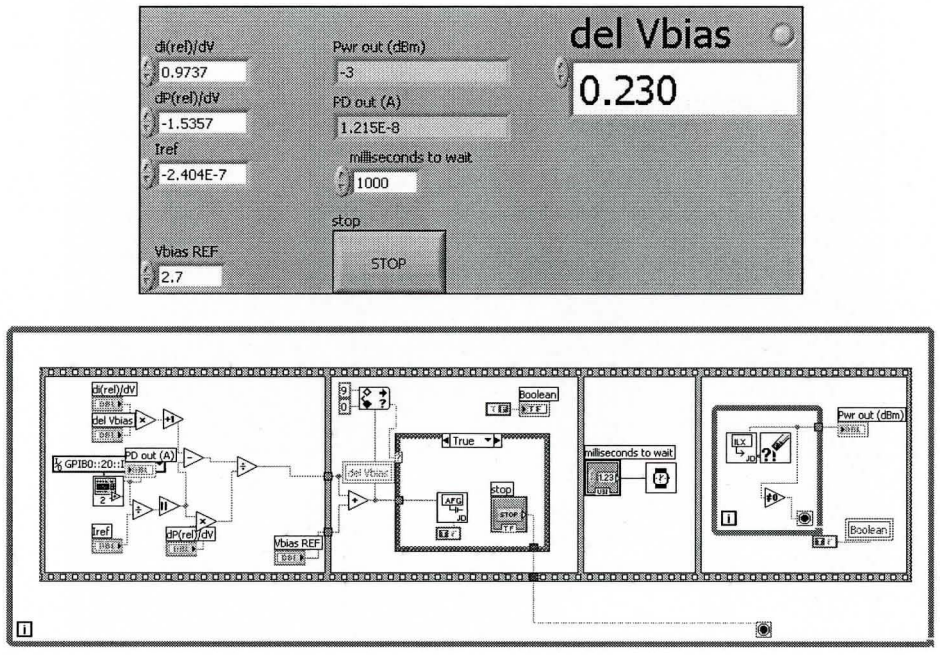


Fig. C.5: Channel leveller feedback loop software front panel (top) and block diagram (bottom).

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