SHUNT ACTIVE POWER FILTERING FOR SMART APPLIANCES

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BY

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A THESIS

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

AND THE SCHOOL OF GRADUATE STUDIES

OF MCMASTER UNIVERSITY

IN PARTIAL FULFILMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

MASTER OF APPLIED SCIENCE

Master of Applied Science (2016) McMaster University
(Electrical & Computer Engineering) Hamilton, Ontario, Canada

TITLE: Shunt Active Power Filtering for Smart Appliances

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NUMBER OF PAGES: xv, 86

I would like to dedicate this thesis to my role model and dear friend, my father. He is a great man, who has always put my interests ahead of his. A special feeling of gratitude goes to my loving mother, whose words of encouragement opened up the doors of success in my life. Also, I would like to dedicate this thesis to my siblings for their endless support throughout my studies. Finally, to my lovely wife, thank you for always being by my side!

Abstract

Due to the increasing trend towards energy saving of white goods appliances and the commercial viability of power electronic components, there has been an expansion in the use of solid state electronics and variable frequency drive motors in these applications. However, a major drawback of using such energy efficient loads is the introduction of current harmonics onto the local distribution grid. Furthermore, the proliferation of such devices elevates the harmonic content of the supply voltage and the ensuing potential impact on residential distribution networks. This thesis investigates the harmonic content generated by some representative household appliances and suggests a solution to minimize current harmonics by means of active filtering. An active filter circuit is proposed and simulations will be undertaken to compare filter performance when used as an active front end versus a feeder input compensator. Further, a hardware design of the filter was implemented to experimentally verify the filter operation.

Acknowledgments

I would like to express my utmost gratitude to my mentor, Dr. Nafia Al-Mutawaly for his encouragement and support for setting me on the path of academic research. Also, I would like to thank my supervisor, Dr. Nigel Schofield for his invaluable guidance and support throughout the course of this work.

Next, I would like to thank Ali Al-Zubaidi and Mehdi Alimardani for the countless inspiring discussions. Also, I owe thanks to Cheryl Gies for her support throughout my Master's program.

Notation and abbreviations

PCC	Point of Common Coupling
THD	Total Harmonic Distortion
TDD	Total Demand Distortion
APF	Active Power Filtering
SAPF	Shunt Active Power Filter
CSAF	Current Source Active Filter
VSAF	Voltage Source Active Filter
VSC	Voltage Source Converter
VSI	Voltage Source Inverter
MCU	Microcontroller Unit
PT	Potential Transformer
VT	Voltage Transducer
CT	Current Transducer
KVL	Kirchhoff's Voltage Law
i_s	Source current
i_f	Filter current
i_f^*	Reference filter current

i_l	Load current
C_{DC}	DC capacitor
v_{DC}	Voltage across the DC capacitor
V_{DC}^*	Reference DC capacitor voltage value (constant)
$V_{DC_{pre}}$	DC capacitor precharged voltage
v_S	Supply voltage
R_f	Filter losses represented as a resistor
L_f	Line inductor for the SAPF
IGBT	Insulated Gate Bipolar Transistor
PI	Proportional-Integral
k_p	Proportional gain
k_i	Integral gain
HB	Hysteresis Band
i_s^*	Calculated source current
i_{l_h}	Harmonic component of the load current
i_{l_q}	Reactive component of the load current
i_{l_p}	Real component of the load current
i_{Loss}	Current losses through the switching action
t_{ON}	The duration when S_1 and S_4 are conducting

t_{OFF}	The duration when S_2 and S_3 are conducting
f_{sw}	Switching frequency
f_{max}	Maximum switching frequency
f_{min}	Minimum switching frequency
V_{PEAK}	Peak supply voltage
f_S	Supply frequency (60 Hz)
PWM	Pulse Width Modulation
HCC	Hysteresis Current Control
R_L	Load resistance
$R_{Charging}$	Inrush current limiter
P_{Filter}	Power consumption of the filter
P_{pre}	Pre-filtering power consumption (load only)
P_{post}	Post-filtering power consumption (load and filter)
SP	Set Point
PV	Processed Variable
RMS	Root Mean Square
DSP	Digital Signal Processing

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Chapter 1: Introduction

1.1 Power Quality: Definition

Electricity has been, and will always be, a vital part of our lives. As stakeholders, we have to ensure that electricity is efficiently distributed, controlled and used. On one hand, it is the duty of utilities to ensure reliable supply of electricity to consumers. On the other hand, large loads customers (factories, large stores and etc.), have to ensure that they bind to electricity standards. So that, their loads will neither affect utility equipment nor disrupt the flow of electricity to adjacent customers. The term Power Quality encompasses all aspects pertaining to the quality of the electrical supply in terms of the magnitude and frequency of the voltage and current waveforms. Numerous phenomena like harmonics, voltage sag/swell, flickers, notching, resonance, unbalanced three phase systems, grounding etc. influence electrical system power quality [29] [30].

1.2 Effects of Poor Quality

The effects of poor power quality are vast and versatile. Among many, it reduces the life expectancy of electrical components [2] and disturbs the operation of protection devices [3] [4] [5].

For example, in North America, the core of any distribution transformer is designed for optimal operation at 60Hz. Distorted currents drawn by large non-linear loads impose higher frequencies on top of the fundamental frequency component of the current waveform. Since transformer iron core eddy current loss is related to the square of supply frequency, hysteresis loss is proportional to frequency to the power of α (where α is the

range of 1.5-2) and excess loss which is proportional to frequency to the power 3/2 [27]. Continuous distorted load currents increase transformer losses and hence contribute to general temperature rise and potential local hotspots. Further, current harmonics cause additional copper losses in all equipment. These additional losses raise the transformer (and other equipment) temperatures above nominal design levels, a feature that could accelerate the aging of distribution transformers through thermal stress and potentially cause premature component failure [1][2]. Keeping that in mind, transformers and other equipment would then require more frequent maintenance which will increase the total operating cost of the electrical system.

Research has shown that high harmonic content can have further negative impacts on power system performance, as protection relays are built to operate at a nominal frequency (50/60 Hz) [3]. Previous research indicated that some relays may mis-operate and trip under what are considered 'normal' operating conditions, or conversely, fail to trip entirely in the presence of harmonics [3-8]. False or missed relay tripping may result in system failure, service discontinuity or other economic losses.

1.3 The Challenge

Global climate change and the security, or insecurity of energy supplies has fostered a trend towards the manufacture of energy saving appliances in recent years [9]. Such loads may typically use variable frequency drive motors and solid state electronics to improve operational efficiency and reduce energy consumption. Since the primary motivation is load energy efficiency at low cost, many designs neglect the load impact in terms of power quality, because this adds to additional circuitry and hence cost. The drawback of these modern loads is therefore, the introduction of harmonics onto the local distribution grid [2]. Although on an individual basis, these devices are low power, multiple loads operating simultaneously can have a severe effect on overall distribution system power quality.

The increased use of such devices elevates the harmonic content of the power system. Moreover, due to the interconnection of the distribution system, harmonics from one customer can harmfully affect the quality of the electrical voltage supply to adjacent customers on the distribution networks and smart appliances on the distribution level.

The proliferation of white goods to customers' households is a pressing issue to many utilities. In the old days, harmonic distortion was not as prevalent as nowadays. Utilities are concerned and are performing case studies to evaluate and quantify the impact of harmonics generated by such devices. Hydro One In. in Ontario, Canada, had previously partnered with McMaster University and Mohawk College to target this issue [10].

Previous research conducted in [10] and [52] intiated the research presented in this thesis. In [10], various non-linear loads, including a Plug-in Hybrid Electric Vehicle (PHEV) were tested to identify the harmonic content for each load. In [52], extensive testing was conducted to assess electromechanical and IED relay operation in the presence of line harmonics.

1.4 Thesis Outline

This Chapter presents an overview of contemporary issues in power quality. Amongst many, harmonic distortion as a phenomenon was discussed thoroughly earlier in this Chapter. The research forms the fundamental problem to be solved in the chapters to follow. In Chapter 2, harmonics will be defined mathematically and data from laboratory measurements of smart appliances current waveforms will be presented. In Chapter 3, a thorough literature review of methods to mitigate harmonics will be investigated. Building on the findings of Chapter 3, Chapter 4 will discuss a proposed solution by means of active power filtering. Comparative computer simulations will be undertaken to simulate the filter operation as a feeder compensator and as an active front end. In Chapter 5, a hardware prototype of the filter will be built to test the filter performance and validate results obtained

from computer simulations. The filter circuit will compensate the harmonics generated by a half wave rectifier load. Finally, Chapter 6 will discuss research outcomes and present ideas for further study.

1.5 Contributions

A design of a SAPF will be proposed, and filter results from simulation will be validated experimentally. The following outcomes will be achieved at the end of this thesis:

- A prototype will be built to filter the current harmonic content generated by a half wave rectifier load.
- Comparing the performance of SAPFs (Shunt active power filters) when used as an active front end or as a feeder compensator.
- A design of the filter will be proposed to compensate for various load conditions through the use of variable line inductor. The new filter design needs to be validated in the future.

Chapter 2: The Power Quality Dilemma

2.1 Harmonics

Harmonic frequencies are multiples of the main supply nominal frequency (60 Hz in North America); it can be even (120Hz, 240Hz, 360Hz…...) or odd (180Hz, 300Hz, 420Hz…….). Mathematically, any current or voltage waveform distortion can be represented by adding specific harmonics with certain magnitudes and phase shifts [31]. For example, a square wave voltage waveform can be decomposed by using the well established Fourier Series technique [31]:

$$V(t) = \frac{4}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \sin(n\omega t) \tag{2.1}$$

where, $\omega = 2\pi/T$ the angular frequency.

The voltage waveform of a square wave can then be deconstructed to a fundamental frequency sinewave and harmonics [31]:

$$V(t) = \frac{4}{\pi} \sin(\omega t) + \frac{4}{\pi} \sum_{n=3,5,7,\ldots}^{\infty} \frac{1}{n} \sin(n\omega t) \tag{2.2}$$

In order to identify the harmonic content of any distorted waveform, Fourier Transform needs to be applied to calculate the magnitude and phase shift of each harmonic present in a signal.

Phase shift of individual harmonics plays a major role in changing the pattern of distortion on the fundamental frequency signal. It could change a textbook sinewave to a square looking waveform or even into a pulse with some phase shift. The following examples will present the effect of phase shift of harmonics on a signal.

Fig. 2.1 shows a distorted waveform which has a third harmonic with a magnitude of 1/3 and a phase shift of 0º superimposed on the 60 Hz fundamental frequency. The distorted waveform in Fig. 2.1 can be written mathematically as:

$$V(t) = \sin(2\pi ft) + \frac{1}{3}\sin(2\pi 3ft + \Phi) \tag{2.3}$$

where, f = 60Hz and $\Phi = 0°$.

Clearly, adding more harmonics could make the waveform in Fig. 2.1 look more like a squarewave. Fig. 2.2 again shows a distorted waveform which has a third harmonic with a magnitude of 1/3 superimposed on the 60 Hz fundamental frequency but now with a phase shift of 180º.

The distorted waveform in Fig. 2.2 can be written mathematically as:

$$V(t) = \sin(2\pi ft) + \frac{1}{3}\sin(2\pi 3ft + \Phi) \tag{2.4}$$

where, f = 60Hz and $\Phi = 180°$.

The effect of phase shifting the third harmonic is evident, with the waveform in Fig. 2.2 approaching more of a thin pulse, while the waveform of Fig. 2.1 appears to be more towards a rectangular pulse. Thus, the harmonic magnitude, number and phase can vary the total waveform much from the fundamental.

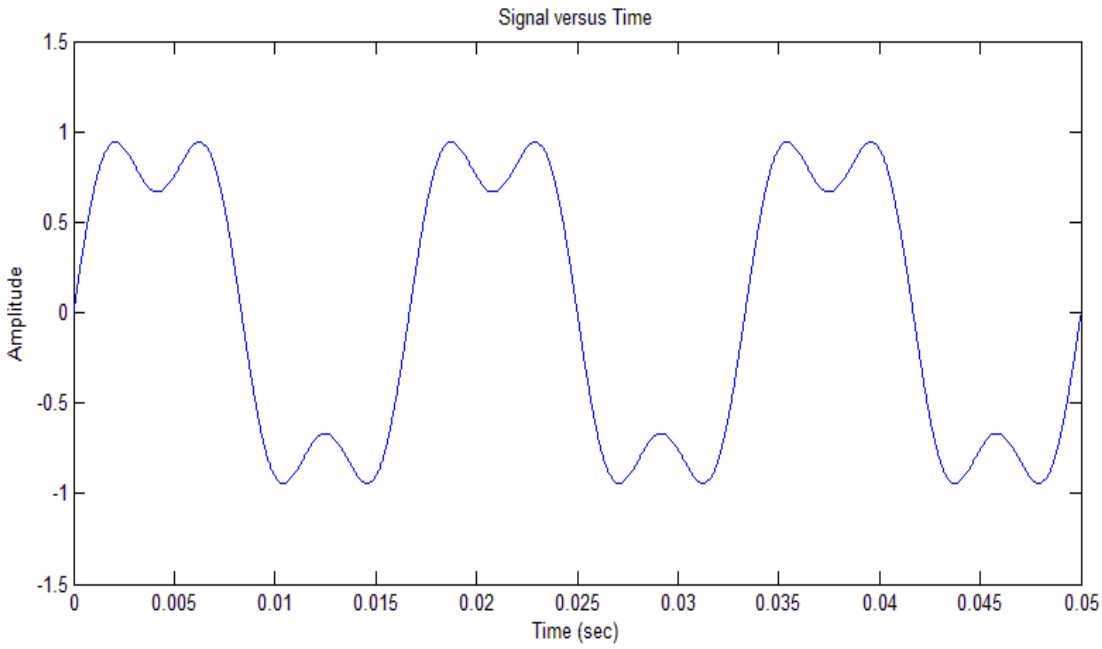


Fig. 2.1 60 Hz signal contaminated with a third order harmonic and no phase shift.

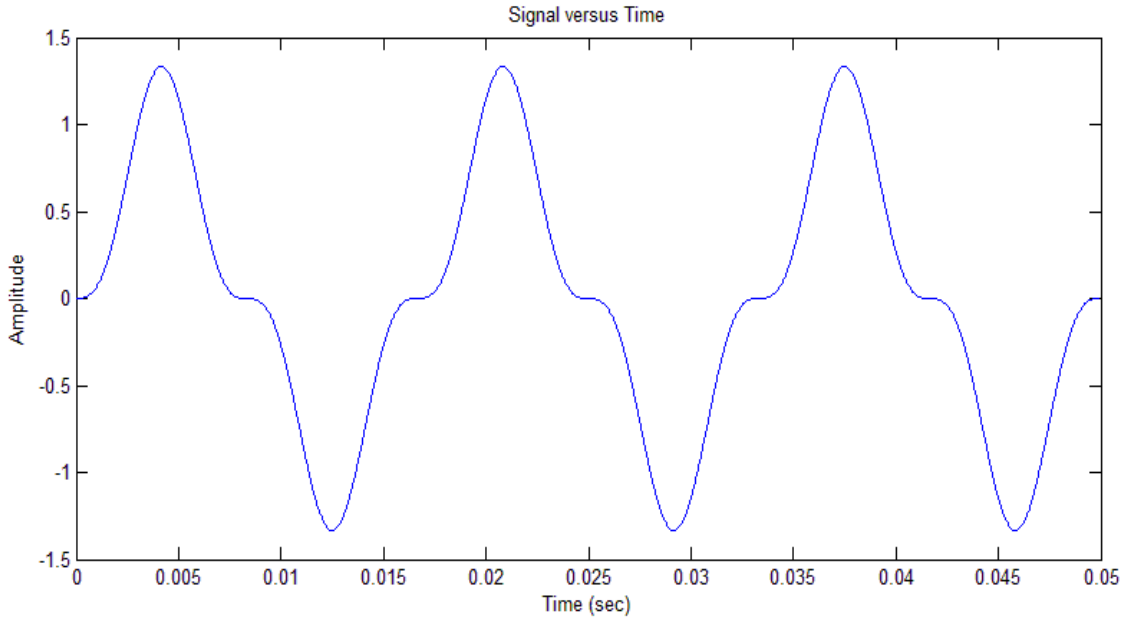


Fig. 2.2 60 Hz signal contaminated with a 180^{o} phase shifted third order harmonic.

2.1.1 Impact

Harmonic distortion is a contemporary undesired electrical phenomenon in power systems that occurs due to increased usage of Variable Frequency Drives (VFDs), solid state inverters and other nonlinear loads. Research has shown that distorted currents have been known to cause overheating of neutral conductors, protection device malfunction [1][52], improper operation of metering devices, de-rating of distribution equipment and resonance [2]. The impact on the circuit current is demonstrated by considering the current RMS value [30]:

$$I_{RMS} = \sqrt{I_{RMS\ Fundamental}{}^2 + I_{RMS\ Harmonics}{}^2} \tag{2.5}$$

where the additional harmonic term will ultimately increase system joule losses.

Referring back to Fig. 2.1 and Fig. 2.2, a quick comparison of the two waveforms shows that even though both of them have the same RMS value, each waveform peaks at a different magnitude. The waveform in Fig. 2.2 shows a higher crest value than the waveform in Fig. 2.1. The presented problem will get amplified in the future as more and more residential loads require AC/DC power conversion. The issues with harmonics are numerous, hence there is a vital need to reduce and possibly eliminate harmonics. In order to properly identify the impact of harmonics present on a system, we need to define terms that could help us quantify the impact.

2.1.2 Quantification

There are primarily two terms that quantify the harmonic content in a waveform; total harmonic distortion (THD) and total demand distortion (TDD). THD can be simply defined as the ratio of the energy of harmonics with respect to the energy of the fundamental frequency. Mathematically, it can be represented as follows [30]:

$$\%THD = \left[\frac{I_{RMS\ Harmonics}}{I_{RMS\ Fundamental}}\right] 100 \tag{2.6}$$

and,

$$I_{RMS(harmonics)} = \sqrt{(I_2)^2 + (I_3)^2 + \cdots + (I_n)^2} \tag{2.7}$$

where, n is the order of the harmonic.

THD is a useful term when describing the distortion of a waveform but it does not give us a full picture of the impact of the waveform distortion on our system. TDD on the other hand, calculates the ratio of the energy of harmonics with respect to the full load [11].

$$\%TDD = \left[\frac{I_{RMS\ Harmonics}}{I_{RMS\ Full\ Load}}\right] 100 \tag{2.8}$$

In both THD and TDD relationships, the lower the ratio implies lower contamination of the waveform. TDD gives a better insight about the impact of harmonic distortion on the system. A THD could be high for a small load, but since the power consumption is low, then the effect on the system will be low. However, multiple 'small loads' ultimately culminate to a significant system problem. Therefore, standards need to be presented to indicate how severe and bad the harmonic content is on the system.

2.1.3 Standards

In order to prevent harmonics from distorting the supply of power from utilities, many standards have been established and reinforced by utilities to force commercial and residential customers to abide by the harmonic limits presented in each standard. There are several standards around the world, below is a list of the most common:

– IEEE 519 (North American) [11]

– IEC61000-3-2 (International) [12]

– G5/4-1 (UK) [32]

– GB/T 14549 (China) [33]

The IEEE 519 North American standard was established as the 'Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems', a summary of which is presented in Table 2.1. The table shows the maximum harmonic limits for medium and low voltage distribution systems as a percentage of the load current. Also, it specifies current distortion limits for general distribution systems (120V through 69 kV), taken from Table 10.3, p78, IEEE 519 [11].

Table 2.1 Maximum harmonic current distortion as a percentage of I_L [11].

$\frac{I_{SC}}{I_L}$ $p.u.$	**Individual Harmonics Percentage Relative to the Fundamental**					
	<11 (%)	11≤h<17 (%)	17≤h<23 (%)	23≤h<35 (%)	35≤h (%)	TDD (%)
<20	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

where:

I_{SC} = the per unit (p.u.) maximum short-circuit current at the point of common coupling (PCC), and I_L = the p.u. maximum demand load current (fundamental frequency component) at PCC.

For example, if the fundamental frequency current is 100 A_{RMS} and the 10th harmonic current is 4.5 A, then, looking at row 2 column B in Table 2.1 we can note that this scenario violates the limit specified in the standard (4%). The point of common coupling (PCC) is a

virtual point that distinguishes the utility from the customer; the PCC is identified by a mutual agreement between a utility and a customer. One issue in the context of this thesis is that although the IEEE 519 standard is widely adopted in North America, it does not clearly specify limits for household appliances. Indeed, it can be noted from the table that the higher the $\frac{I_{SC}}{I_L}$ ratio (smaller load), the higher the harmonic percentage is allowed. Further, since the scope of this research is to compensate for harmonics at the residential level, TDD will not be used, as the PCC is far away from the load side. The IEC61000-3-2 standard [12] is a more descriptive standard, in the sense that it clearly describes the harmonic limits for various load size and type of appliance/household equipment. Hence, there is a need to include the limits for residential loads in the IEEE 519 standard, since it is the standard adopted in Canada [13].

Table 2.2 Limits for Class A equipment; Balanced 3-Phase equipment, Household Appliances, Tools, IEC61000-3-2 [12].

Harmonic Order n	**Maximum Permissible Harmonic Current A**
Odd Harmonics	
3	2.30
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
15≤n≤39	0.15
Even Harmonics	
2	1.08
4	0.43
6	0.30
8≤n≤40	0.23

2.2 Measurements

A laboratory at Mohawk College, Hamilton, Ontario, Canada has been built to emulate a typical modern North American home, consisting of a variety of 120V/240V appliances [14]. The idea of building the laboratory was to study and estimate the effects of harmonics generated by such modern loads on a typical distribution transformer. An ION 7650 power quality meter is a reliable analysis tool that is being used by Hydro One utilities to measure harmonics. Extensive testing has been conducted in the laboratory using an ION 7650 on the appliances presented in Table 2.3. To properly quantify the harmonic content present, two test scenarios were carried out; an individual (single appliance) and combinational (multi appliance) tests.

Table 2.3: Smart appliances tested.

Appliance	Model	Power Requirements	Energy Consumption (kWh/year)
LG Fridge	LFX25778ST	N/A	568
LG Washer	WT4901CW	120V, 10A	N/A
LG Dryer	DLEC855W	220V, 30A	N/A
LG Dishwasher	LDS4821WW	120V, 15A	N/A

2.2.1 Single Appliance Test

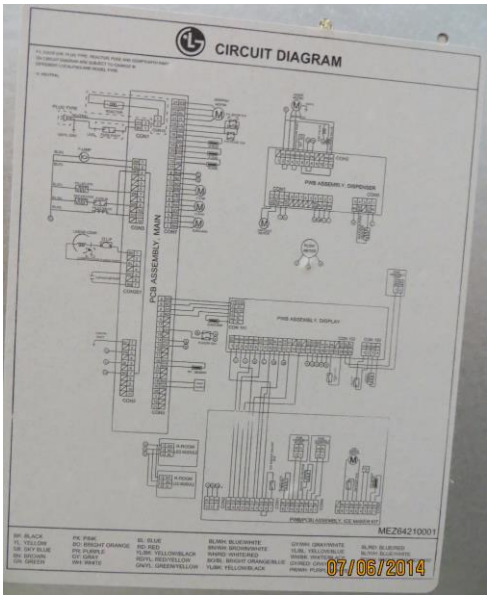
An LG LFX25778ST smart fridge was selected to carry out a single appliance test. Fig. 2.3 illustrates the fridge's general dimensions, circuits and power electronics. The outcome of careful research indicated that the fridge has a linear motor that drives a linear compressor. The position controller detects voltage and current of the linear motor to calculate the stroke [15]. The compressor relies on the pulses generated by the controller

to achieve the highest energy; this happens when the voltage peaks at a maximum of 169.3V. The schematic diagram of the LG fridge controller is illustrated in Fig. 2.4(a) while the circuit diagram of a conventional fridge is illustrated in Fig. 2.4(b). Unlike conventional fridges, operating the fridge efficiently produces high harmonic current as will be discussed later. The phase current coming out of the secondary of the distribution transformer was monitored throughout the operation of the fridge. The fridge was turned on with all of the other appliances in the laboratory being disconnected from power. Using the ION 7650 and a high frequency hall effect current transducer, the line current of the fridge was monitored and data was recorded when the fridge's compressor started working. Figs. 2.5 and 2.6 show the results using the ION 7650 PC software.

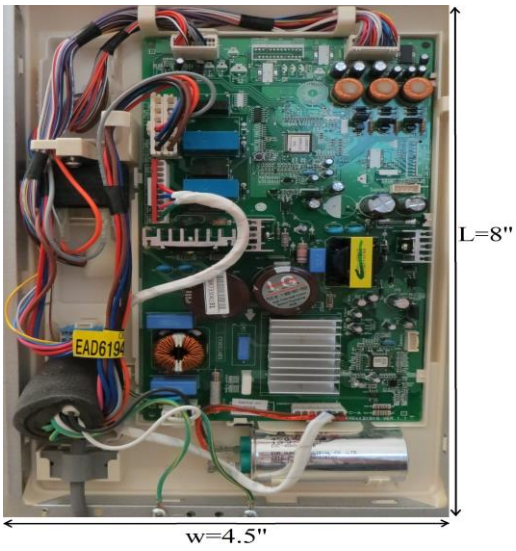
Referring to Fig. 2.4, the TRIAC turns on when the voltage is around the peak value. The power for that duration will be maximum and sufficient to drive the compressor. However, switching the TRIAC to achieve maximum energy savings comes at the cost of poor power quality. Fig. 2.5 shows the distorted supply current waveform and Fig. 2.6 indicates the harmonic spectrum of the current waveform of Fig. 2.5. The Total Harmonic Distortion (THD) for the fridge current waveform of Fig. 2.5 was measured to be 184.35% of the fundamental current.

Further, the fridge operation was tested in a different scenario to prove the conclusion presented earlier. The second test was conducted when the fridge was running without the light bulb (a pure resistive load) to see if this changes anything. The fridge door was left open to force the fridge to compensate for the increase in the cabinet temperature. Fig. 2.7 shows the measured voltage and current waveforms and Fig. 2.8 shows the harmonic content of the current waveform. It can be noted that the frequency spectrum in Fig. 2.8 only consists of odd harmonics, this is merely due to waveform symmetry [31]. In this case, Fourier coefficients of even order harmonics are all zero. The results have been confirmed with a FLUKE 190-162 Scopemeter, as displayed in Fig. 2.9 and Fig. 2.10.

(a) Basic fridge dimensions

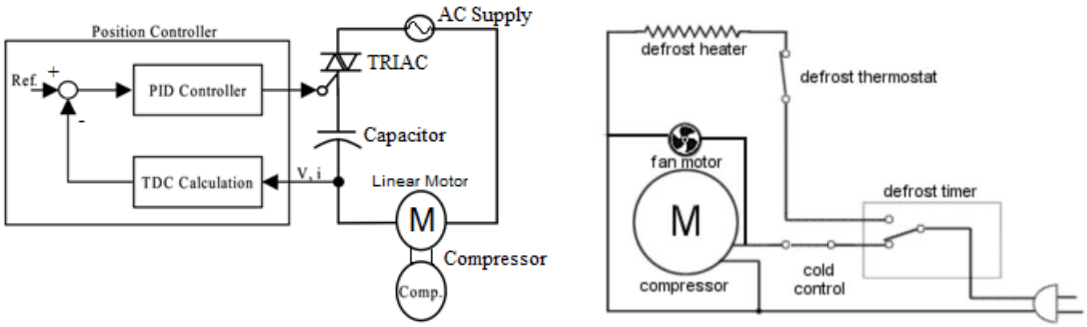


(b) Fridge circuit diagram



(c) Power electronics circuitry

Fig 2.3 LG fridge studied as part of this thesis.



(a) Electrical circuit diagram of the LG fridge [15].

(b) Electrical circuit diagram of a conventional fridge [34].

Fig. 2.4 Fridge electrical circuit diagram.

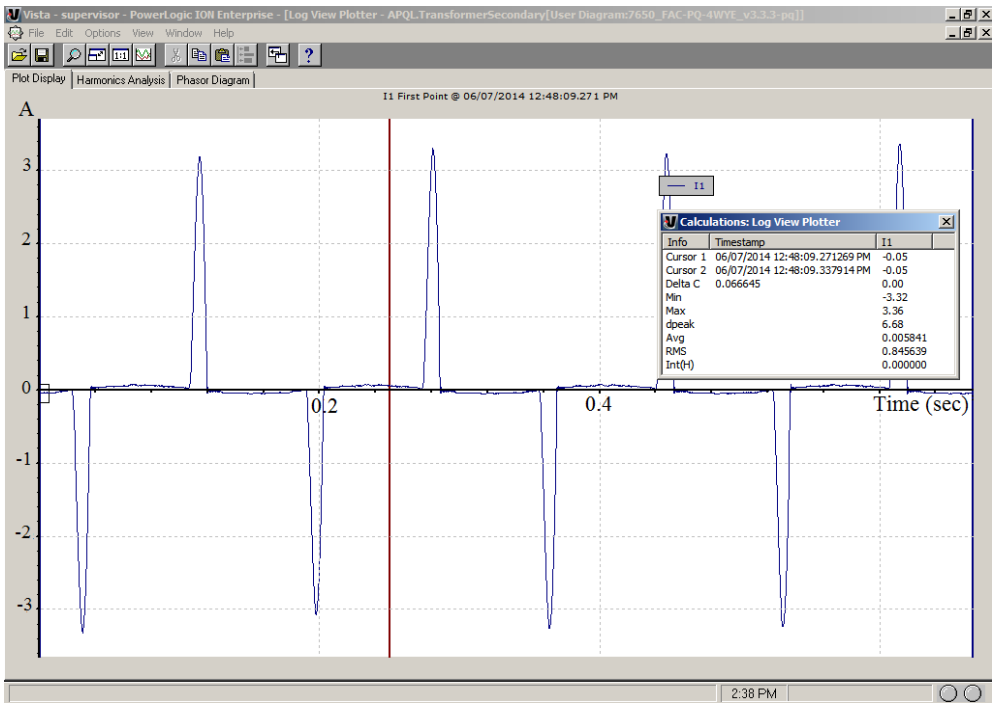


Fig. 2.5 Distorted supply current waveform when the fridge is on.

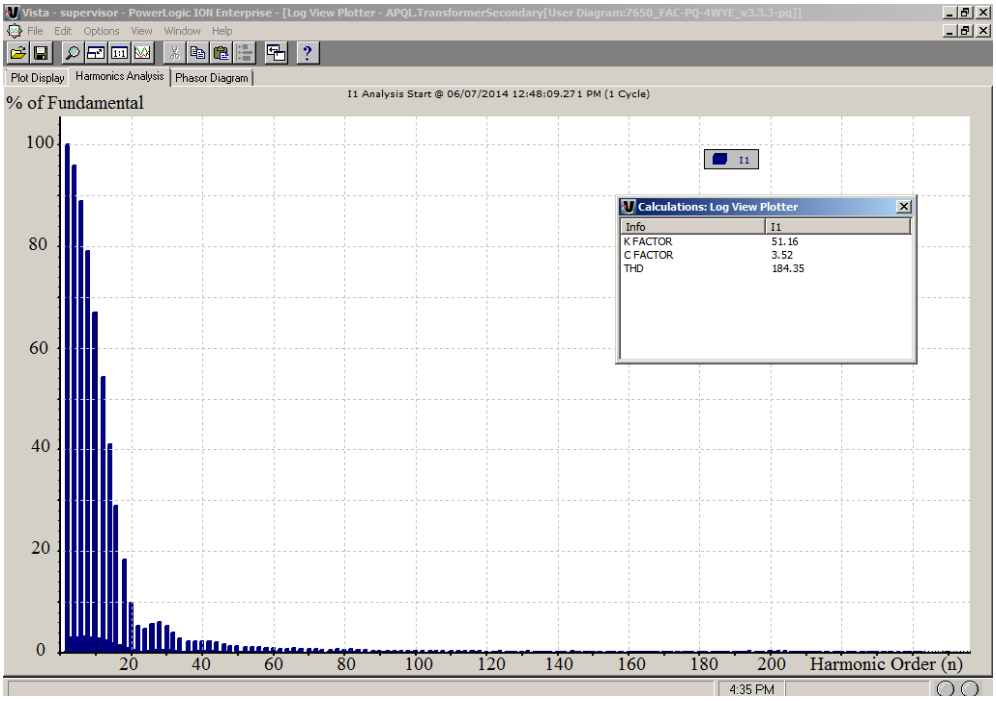


Fig. 2.6 Harmonics of the supply current when the fridge is on.

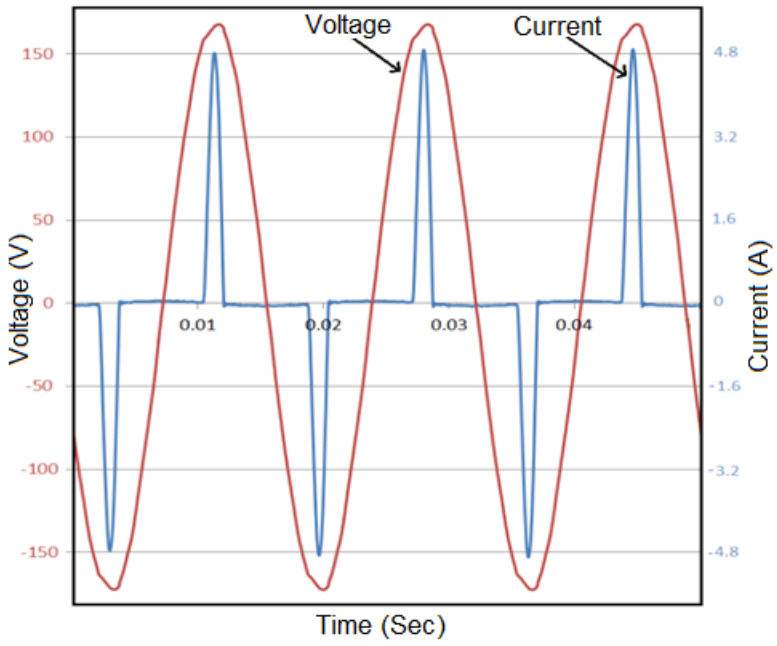


Fig. 2.7 Current waveform without fridge light.

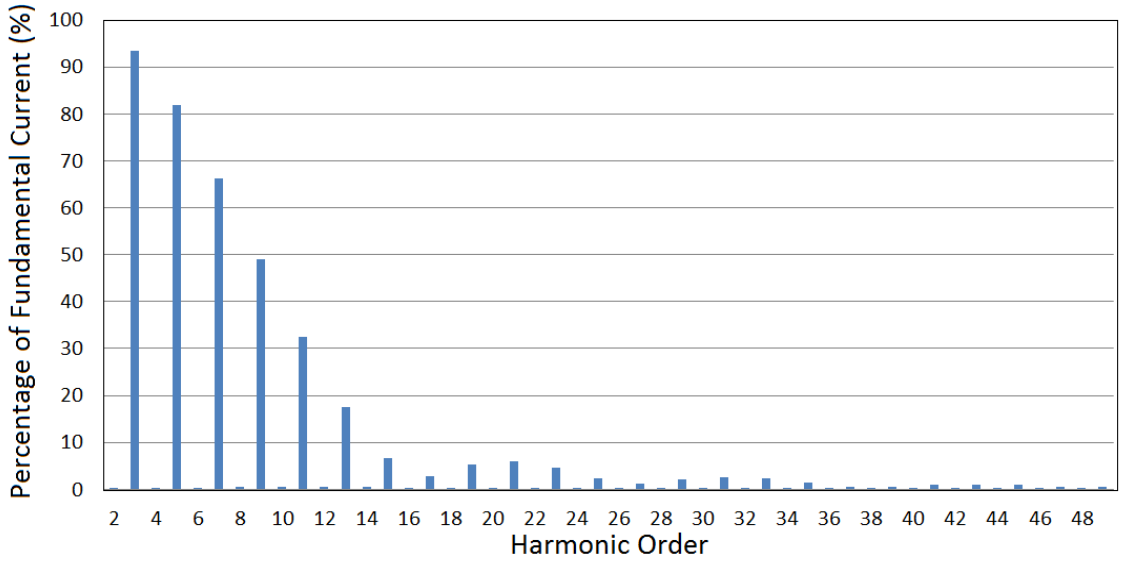
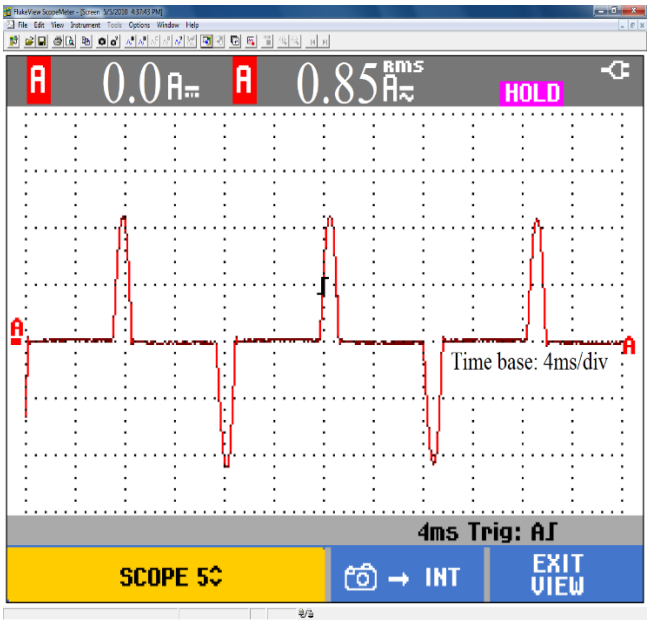
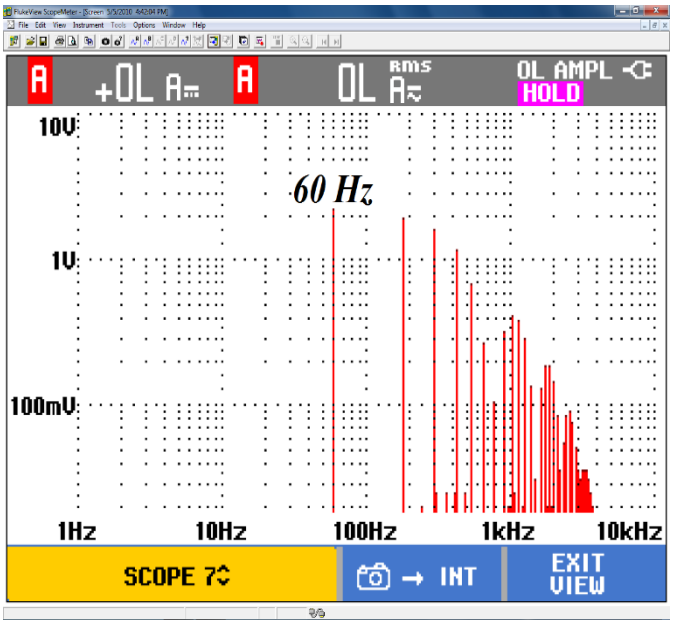


Fig. 2.8 Current harmonics (fundamental not shown) without fridge light.

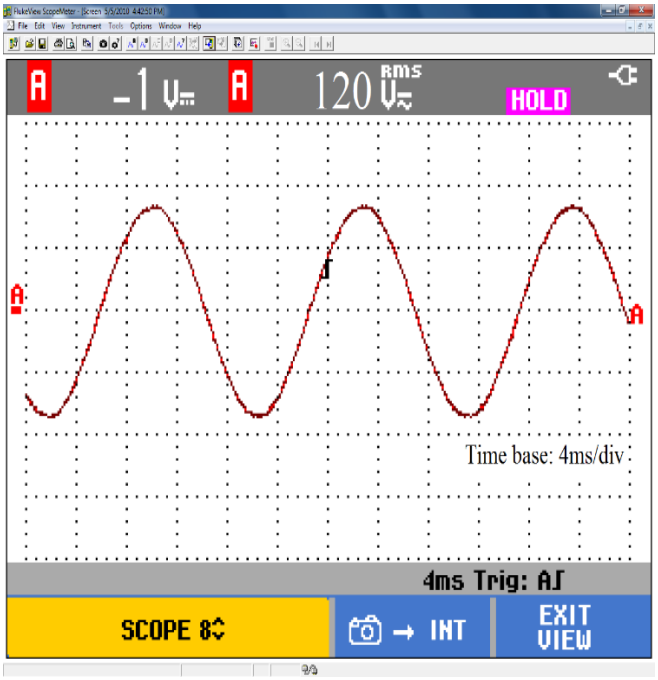


(a) Current waveform

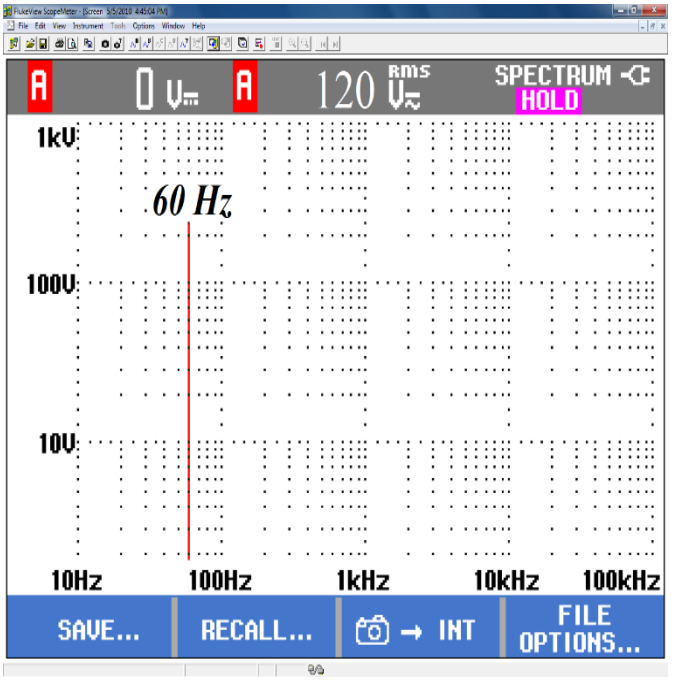


(b) Current harmonics.

Fig. 2.9 Fridge supply current without fridge light, measured with the FLUKE Scopemeter.



(a) Voltage waveform.



(b) Voltage harmonics.

Fig. 2.10 Fridge supply voltage without fridge light, measured with the FLUKE Scopemeter.

2.2.2 Combinational Test

The appliances mentioned in Table 2.3 were energized and their total current was monitored on the secondary of the transformer supplying the laboratory. A clamp-on high frequency current transducer was interfaced to the ION 7650 meter current inputs to accurately measure the total supply current. The test was conducted when loads were operational at steady state. The meter was programmed to capture data based on a 3 cycle interval. Fig. 2.11 shows the supply voltage and current waveforms. The THD was found to be 80.47% of fundamental current. Fig. 2.12 shows the harmonic spectrum of the current waveform of Fig. 2.11.

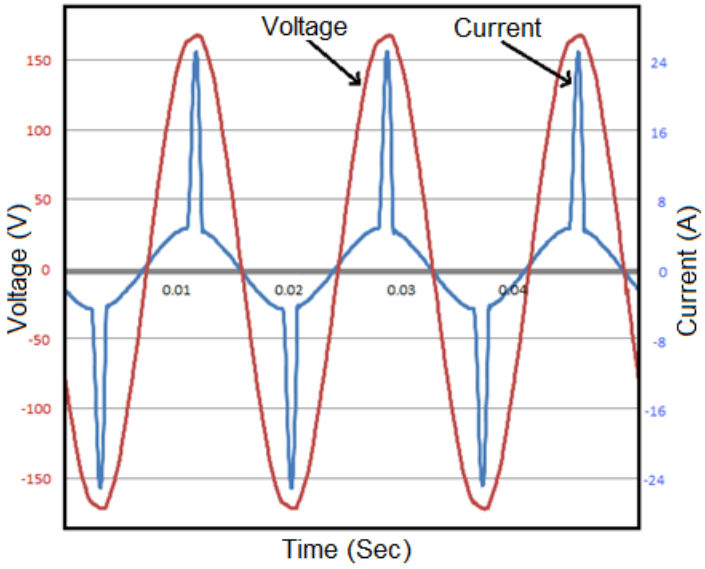


Fig. 2.11 Distorted supply current waveform when all the appliances are on.

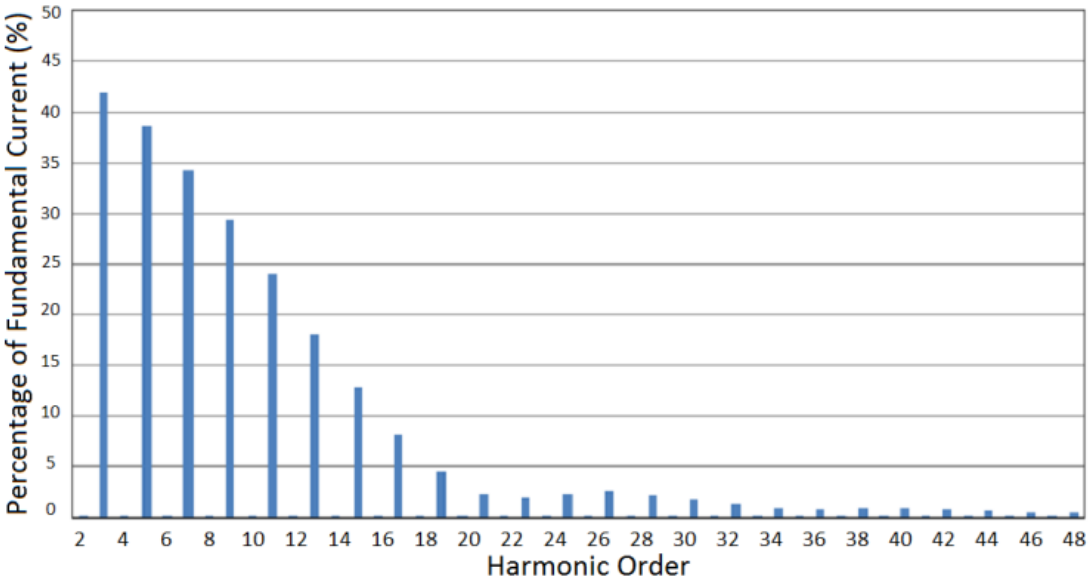


Fig. 2.12 Harmonics of the supply current when all the appliances are on.

2.3 Why not Compensate for Voltage Harmonics?

Compensating voltage harmonics is not widely addressed because power supplies have low impedance, as discussed in page 2 of [35]. The voltages at the PCC are generally assumed to be maintained within the standard limits for voltage sag/swell, but waveform quality is not assessed.

However, non-sinusoidal currents drawn from the supply could cause distortion of the supply voltage, since the inductance of the supply increases the source impedance as the harmonic order increases, as discussed in page 3 of [16]. Excessive current harmonics from non-linear loads can distort a supply's voltage waveform [35], these distortions will create voltage harmonics. Voltage harmonics affect the entire power system, not just the loads which are causing them (i.e. other linear loads in the network).

That being said, effects of using smart house appliances are not major nowadays; since they are usually single phase loads with small wattage consumption. However, the problem will grow to become a great concern for adjacent costumers and utilities in the future when these appliances proliferate the market [16]. Hence there is a need to research and provide solutions to target this issue at the root cause.

Consequently, the problem relating to current harmonics is far more important than voltage harmonics at the residential level. The compensation of current harmonics reduces to a great extent the amount of distortion in the voltage at the PCC since the compensation of voltage and current harmonics are interrelated [17].

2.4 The Need for a Solution

It can be noted that during the single appliance test, some of the individual harmonics have failed the IEC61000-3-2 standard. For example, looking at Fig. 2.8, the 9^{th} harmonic has a percentage of 49%, knowing that the fridge's RMS current is 0.845 A, the current of the 9^{th} harmonic is 0.41 A. Comparing this value with Table 2.2, we can safely say that the fridge has failed to partially meet the standard. Hence, it is very important to propose a solution to reduce and/or possibly eliminate the harmonic content of the appliance current. Passive filtering techniques could be applied to remove certain orders of harmonics, but they in turn could produce series and parallel resonance with the source impedance. Also, due to the relatively large and bulky inductor required by such filters [18], they would not be realistic to apply in each residential home, if this were to be implemented. Since power electronics are cost effective for low power applications (residential loads), it is economical to utilize them in home appliances to aid in harmonic reduction by means of active filtering.

2.5 Summary

In this Chapter, various smart appliances were investigated to measure the harmonic content generated by such loads. Measurements of the line current indicated that almost all of the non-linear loads produced a high harmonic content. Although on an individual basis, these devices are low power, multiple loads operating simultaneously can have a severe effect on overall distribution system power quality. As mentioned previously, continuous distorted load currents increase transformer losses, contribute to temperature rise and hotspots, accelerating aging and potentially causing premature component failure. Chapter 3 will discuss the literature research conducted with respect to active filtering, circuit topologies and control methodologies. Further, a choice for an active filter circuit will be selected for the purpose of this research.

Chapter 3: Active Filter Literature Review

3.1 Active Filtering Introduction

An active power filter could be in series or parallel to a non-linear load. Also, an active filter could be part of a hybrid filter (a filter that consists of active and passive filters to improve efficiency) [18]. Series active filters are located in series between source and non-linear loads, they are meant to compensate voltage harmonics of the load. Parallel (shunt) active filtering has been considered in this research as opposed to series active filtering simply because parallel filters carry only a fraction of the fundamental load current.

The main reason for choosing shunt active power filters (SAPF) is their lower component ratings; since we are interested in removing current harmonics from the load. If we were to have the filter in series with the load, then we will have the total current passing through the filter which would require higher ratings for the circuit power electronic switches [18] [19].

SAPF is simply a voltage source converter, the filter implements power electronic switching to compensate the current harmonics of a non-linear load [18]. There are two kinds of SAPF; Current Source Active Filter (CSAF) and Voltage Source Active Filter (VSAF). The difference between these two topologies is the type of the storage element as shown in Figs. 3.1 and 3.2. VSAF is less expensive, lighter, produces less losses and is easier to control compared to the CSAF [18], hence it was selected as the circuit topology for the filter design in this thesis.

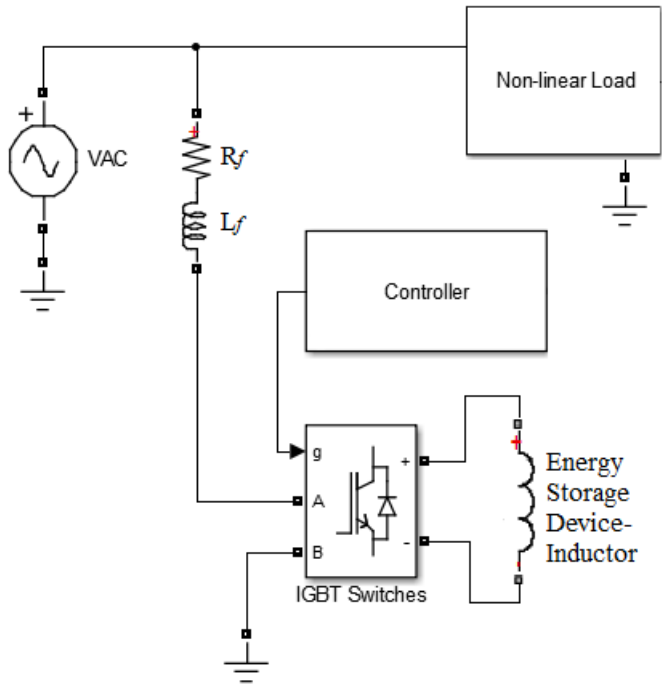


Fig. 3.1 Current source active filter (CSAF) circuit.

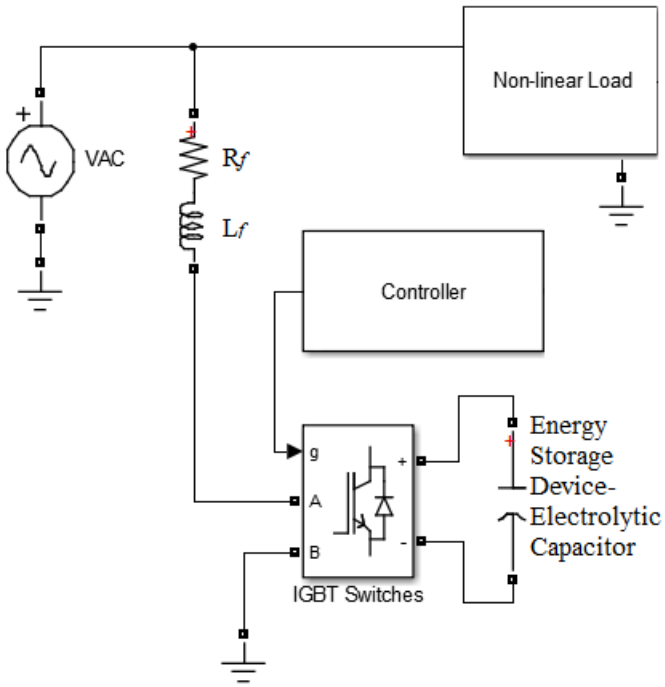


Fig. 3.2 Voltage source active filter (VSAF) circuit.

3.2 Filter Operation

The concept of shunt APF is based on harmonic cancellation by the act of injecting equal but opposite harmonic current to that of the non-linear load. This is achieved by precisely switching the VSI IGBTs using a micro-controller unit (MCU). The only downside of using SAPF is the injection of high switching frequency in the system. However, these effects are minimal and could be eliminated by using a passive low pass filter in conjunction with the SAPF designed at the switching pulse width modulation (PWM) frequency [18].

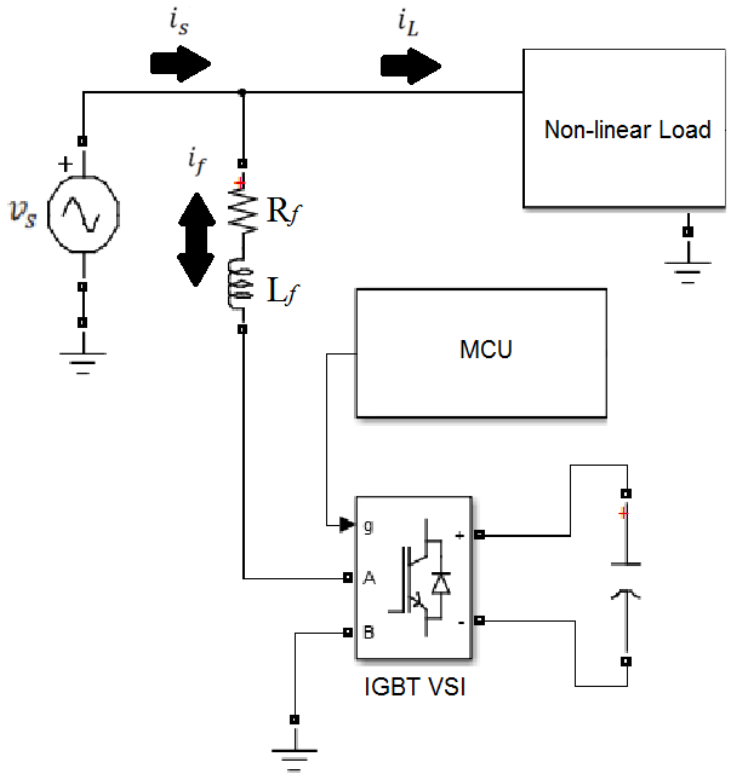


Fig. 3.3 VSAF circuit showing current flow.

The SAPF circuit is composed of the following components, as in Fig. 3.3:

- Two legs of IGBTs (with anti-parallel diodes) as shown in detail in Fig. 3.4. Note, the operation of the switches will be described later.

- A capacitor, C_{DC}, to store the energy required for the filter operation.
- A line inductor, L_f, to smoothen the filter current and prevent high current ripples.
- A line resistor, R_f, representing the losses in the circuit (switches and inductor coil resistance losses).
- An MCU to control the operation of the filter by switching the four IGBT switches.

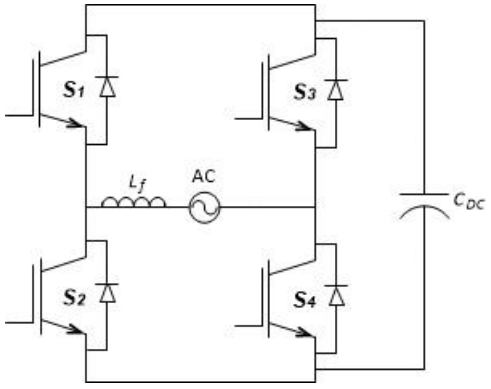


Fig. 3.4 Switch configuration in the inverter circuit.

If Sw =1, then S1 and S4 are on (upper switch in leg 1 and bottom switch of leg 2 of the inverter), also, if Sw = 0, then S2 and S3 are on (bottom switch in leg 1 and upper switch of leg 2 of the inverter). The gates of the IGBT switches are controlled precisely in conjunction with the measured load current.

Using KVL, the equation governing the filter operation can be obtained as follows:

$$\frac{di_f}{dt} = -\frac{R_f}{L_f}.i_f + \frac{S_w}{L_f}.v_{dc} - \frac{v_s}{L_f} \tag{3.1}$$

If S_1 and S_4 are on, the value of S_w will equal to 1, the above equation can then be rewritten as:

$$L_f \frac{di_f}{dt} + R_f i_f = v_{dc} - v_s \tag{3.2}$$

If S_2 and S_3 are on, the value of S_w will equal to -1, the above equation can then be rewritten as:

$$L_f \frac{di_f}{dt} + R_f i_f = -v_{dc} - v_s \tag{3.3}$$

The selection of the smoothing inductance (L_f) and the energy storage capacitor (C_{DC}) values directly affects the performance of the active power filter performance.

3.2.1 Capacitor (Energy Storage) Operation

The capacitor energy is represented by:

$$E = \frac{1}{2} C_{DC} {v_{DC}}^2 \tag{3.4}$$

The DC capacitor acts as a voltage source and an energy storage element [20]. The capacitor will be charged from the same supply that powers the load. The filter circuit has to be run in extreme caution, to avoid a short circuit situation in the filter circuit; the capacitor has to be pre-charged by the supply prior to the filter activation. Since the impedance of X_c is theoretically zero at the moment of filter energization, the initial current will be very high. This excess current could damage the components of the VSC (Voltage Source Converter). One method to prevent the latter is to add a resistor in series with the capacitor; the resistance could then be removed when the capacitor voltage reaches approximately V_{PEAK} of the supply voltage. Fig. 3.5 outlines the pre-charging mechanism, while Fig. 3.6 shows the charging curve of the capacitor.

In order for the filter to compensate load harmonics, the capacitor needs to be charged to a higher voltage magnitude than the maximum peak of the supply voltage. The capacitor voltage is compared to a pre-set reference voltage value that should be 1.5 times that of the line maximum voltage [21] to ensure correct operation of the filter. The way the capacitor is charged is similar to a boost circuit. The VSC circuit boosts up the voltage of the energy storage capacitor through the use of the inductor. Only when the fundamental component of the inverter output voltage is greater than the peak value of supply voltage, the APF can compensate reactive power [20].

The appropriate size of the capacitor could be determined from the following equations:

$$i_f = C_{DC} \frac{dv_{DC}}{dt} \tag{3.5}$$

and the power (Q) across the capacitor can be calculated:

$$Q = i_f v_{DC} \tag{3.6}$$

Substituting (3.5) to (3.6) results in:

$$Q = \left(C_{DC} \frac{dv_{DC}}{dt} \right) v_{DC} \tag{3.7}$$

Equation (3.7) can be rearranged to find C_{DC}:

$$C_{DC} = \frac{Q}{\left(\frac{dv_{DC}}{dt} \right) v_{DC}} \tag{3.8}$$

And $\frac{dv_{DC}}{dt}$ can be derived by looking at Fig. 3.6:

$$\frac{dv_{DC}}{dt} = \frac{v_{DC_{Max}} - v_{DC_{Min}}}{8.33\ ms} \tag{3.9}$$

Equation (3.9) is derived for a half a cycle, but it can be re-written for a full cycle:

$$C_{DC} = \frac{Q}{f_s({V_{DC\,Max}}^2 - {V_{DC\,Min}}^2)} \tag{3.10}$$

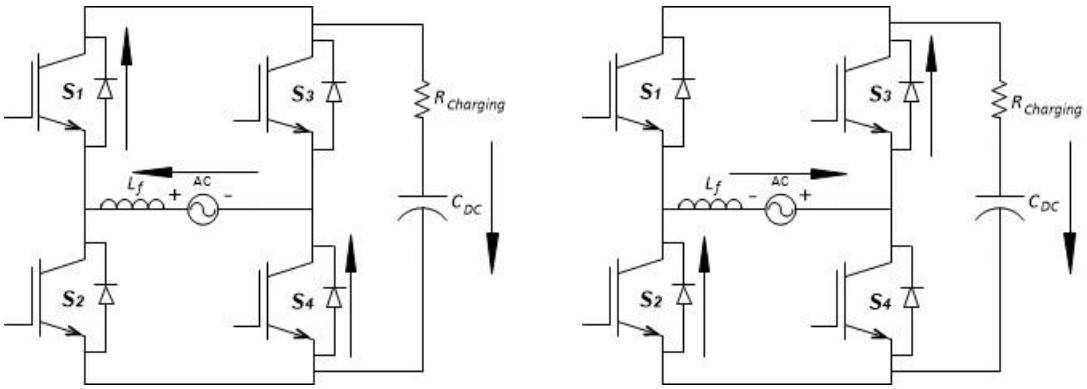


Fig. 3.5 Capacitor pre-charge.

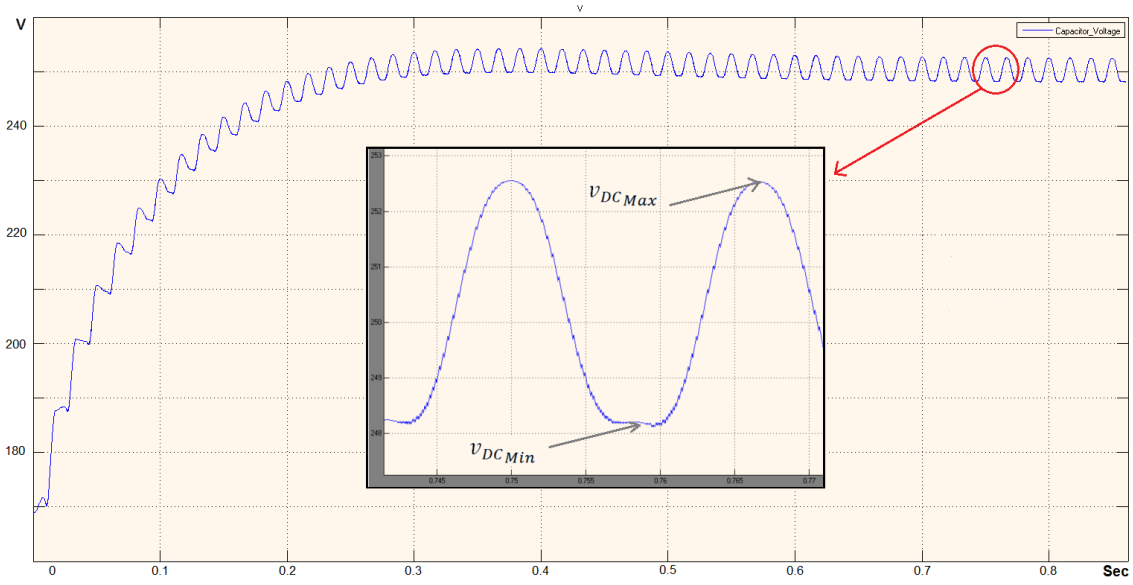


Fig. 3.6 Steady-state capacitor operation.

3.2.2 Inductor Operation

In order to limit the maximum slope of the load current within the compensation capability of the active filter, a smoothing inductor has been inserted before the rectifier, to prevent inverter saturation [21].

The energy through the inductor is represented by:

$$E = \frac{1}{2}Li^2 \tag{3.11}$$

The inductor L_f plays a big role in the filter operation; it smooths the filter current, helps boost the voltage of the capacitor and as a first order passive filter, it prevents switching frequency, which is generated by the inverter [18].

For controllability of the active filter, this inductor should not be large. If the size of the inductor is too large, then the filter wouldn't be able to adjust its current to track sudden load current variations. On the other hand, the inductor shouldn't be too small since this would cause the filter current to have a high ripple content [22]. Typically, a larger compensated current requires a smaller inductor size and vice versa.

Choosing the correct value for the inductor can be achieved. Equations (3.2) and (3.3) describe the voltage across the inductor. Neglecting the $R_f i_{f(t)}$ term, we can re-write these equations to:

$$L_f \frac{di_f}{dt} \cong v_{dc} - v_s \tag{3.12}$$

and,

$$L_f \frac{di_f}{dt} \cong -v_{dc} - v_s \tag{3.13}$$

The ripple current is depicted in Fig. 3.7.

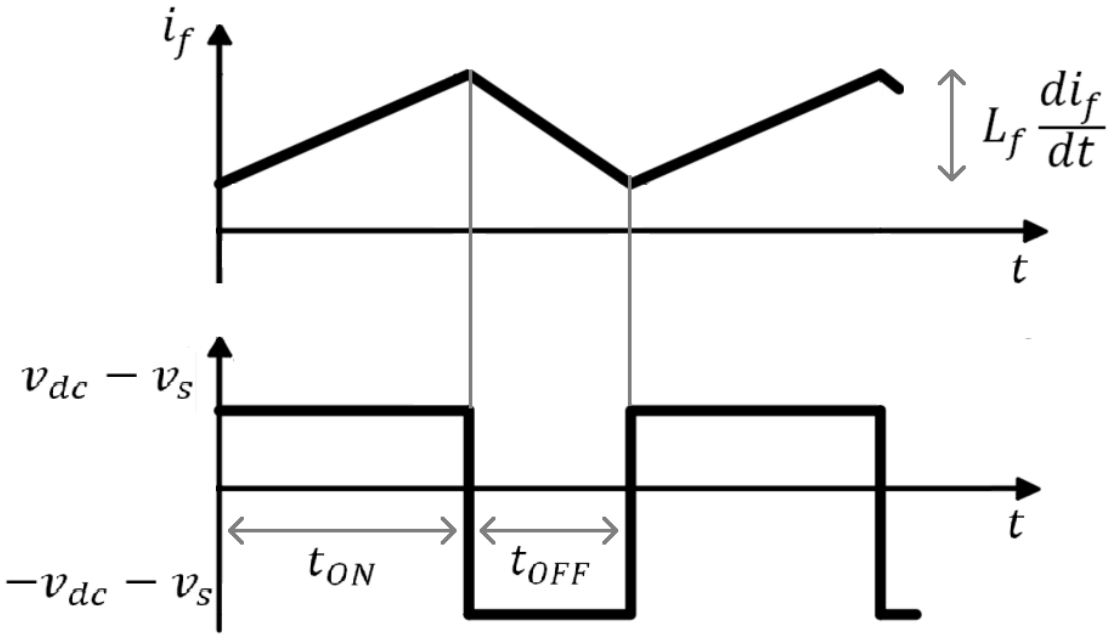


Fig. 3.7 Filter current ripple.

Therefore, the power switch ON and OFF times, t_{ON} and t_{OFF} respectively can be deduced. The t_{ON} equation can be written as:

$$t_{ON} = \frac{L_f \frac{di_f}{dt}}{v_{dc} - v_s} \tag{3.14}$$

and the t_{OFF} equation can be written as:

$$t_{OFF} = \frac{L_f(-\frac{di_f}{dt})}{-v_{dc} - v_s} \tag{3.15}$$

The switching frequency f_{sw} is calculated from:

$$f_{sw} = \frac{1}{t_{ON} + t_{OFF}} \tag{3.16}$$

$$f_{sw} = \frac{1}{\left(\frac{L_f \frac{di_f}{dt}}{v_{dc} - v_s}\right) + \left(\frac{L_f(-\frac{di_f}{dt})}{-v_{dc} - v_s}\right)} \tag{3.17}$$

This can be further simplified to:

$$f_{sw} = \frac{{v_{DC}}^2 - {v_s}^2}{\left(2v_{dc}\, L_f \frac{di_f}{dt}\right)} \tag{3.18}$$

and since the supply voltage is given by:

$$v_S = V_{PEAK} \sin(wt) \tag{3.19}$$

the minimum switching frequency, f_{min} occurs when ${v_s}^2$ becomes maximum. This happens when the supply voltage is at 90º or 270º, i.e. $\sin wt = 1$. Hence, f_{min} is:

$$f_{min} = \frac{{v_{DC}}^2 - (V_{PEAK})^2}{2v_{dc}\, L_f \frac{di_f}{dt}} \tag{3.20}$$

On the other hand, f_{max} occurs when ${v_s}^2$ becomes null, this happens when $\sin(wt) = 0$, hence, f_{max} is:

$$f_{max} = \frac{v_{DC}}{2L_f \frac{di_f}{dt}} \tag{3.21}$$

The value for L_f can be found from (3.21):

$$L_f = \frac{v_{DC}}{2f_{max} \frac{di_f}{dt}} \tag{3.22}$$

3.2.3 Reference Extraction Methods

There are numerous methods to extract the reference current. It can be decomposed mainly to two techniques, frequency domain and time domain [20]. Time domain methods involve fewer calculations compared to frequency domain methods and hence, estimation is achieved faster [20]. The following diagram depicts the methods found in the literature research.

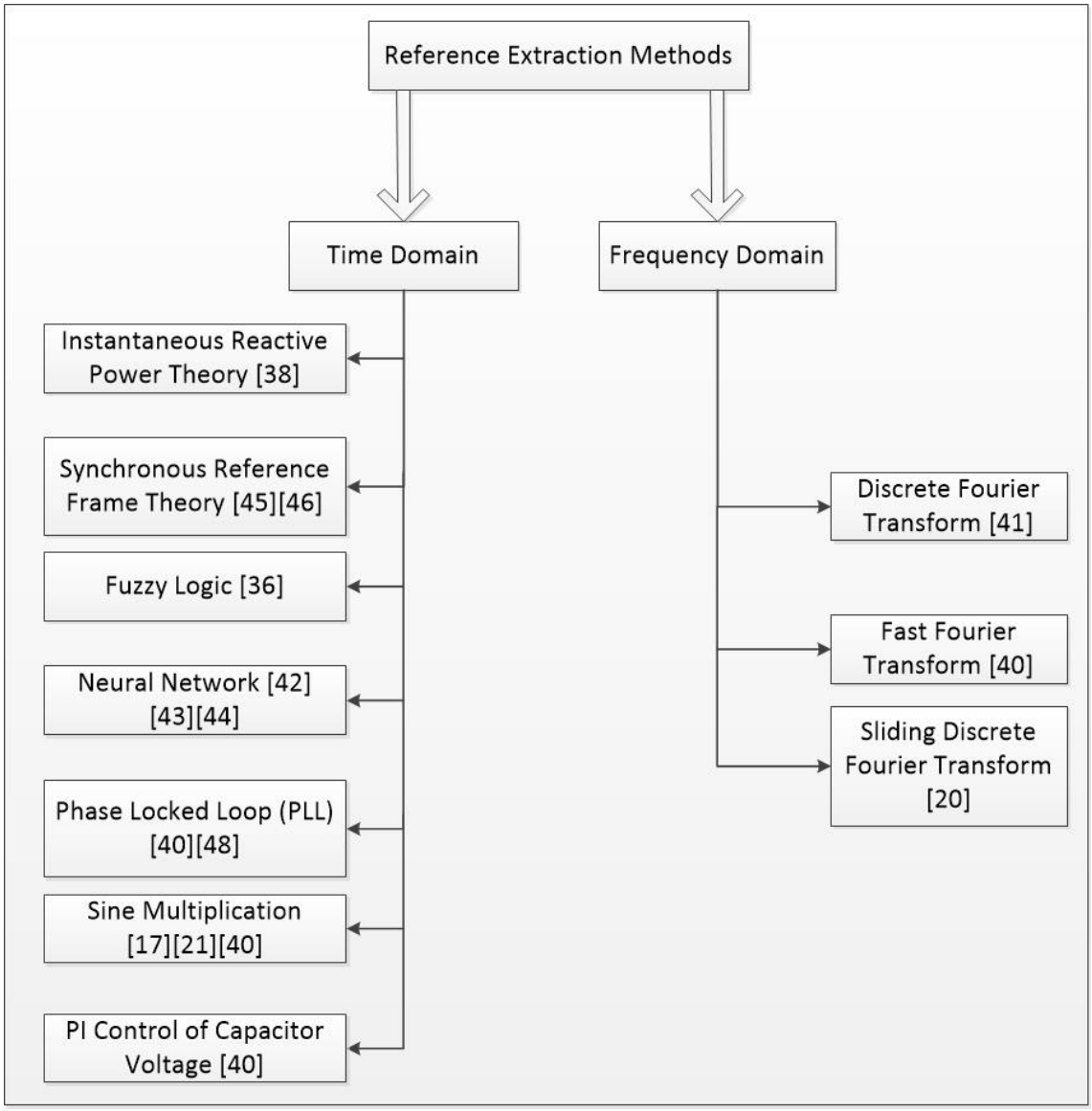


Fig. 3.8 Reference extraction methods.

Assuming a non-distorted power supply, PI Control of Capacitor Voltage was chosen for this research, since this method represents an indirect way of obtaining the desired current and is the easiest to implement in hardware and requires the least calculations. As the name implies, it extracts the required harmonic current by means of capacitor voltage control.

The measured capacitor voltage is compared to a reference voltage value that should be 1.5 times the peak of the source voltage [18]. The error is then passed to a PI controller; the output of the PI controller indicates how much we want to correct the current value. It will then be multiplied with per unitized value of the source voltage to estimate the calculated source current, (i_s^*). Where, i_s^* is the minimum sinusoidal current required from the supply. This should be a very close estimation of the real sinusoidal source current. Fig. 3.9 illustrates the basic control diagram for the technique.

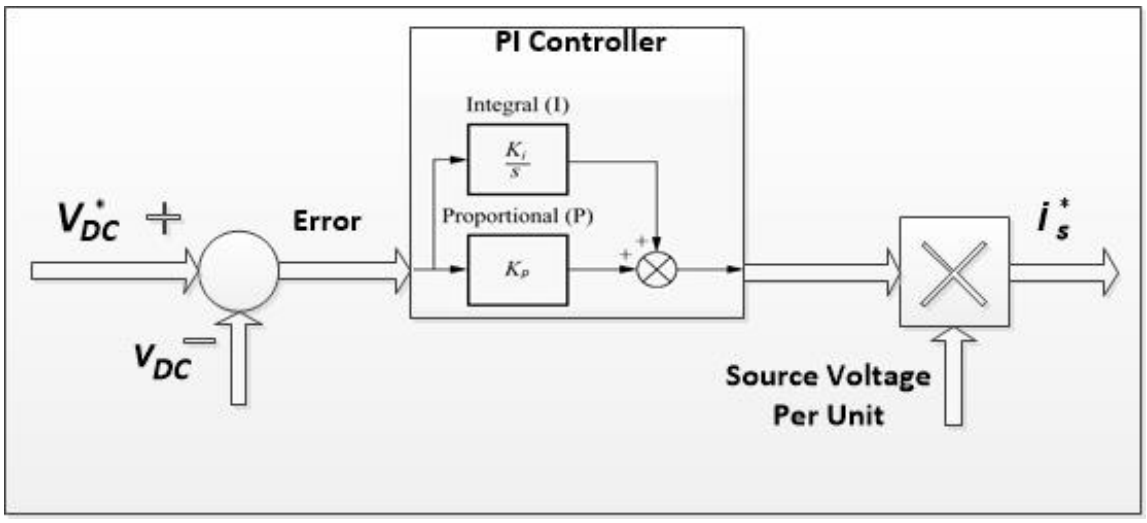


Fig. 3.9 Obtaining the reference current using PI controller.

3.2.4 Control Techniques

Numerous current controlling techniques were researched in the literature [21]; Fig. 3.10 shows different control methods. Regardless of the controlling method, the APF must have the capability to track sudden slope variations in the current reference [21]. Hysteresis

current controller (HCC) possesses certain advantages namely, quick response, easy implementation, maximum current limit and insensitivity to load parameter variations [20]. One drawback using the HCC is that it is difficult to limit the minimum and maximum switching frequencies [23]. However, in this thesis research, maximum switching frequency of the switches has been limited to abide with the sampling time of the micro controller, as discussed later.

The load current, i_l, will be subtracted from the calculated source current (i_s^*), to get the reference filter current (i_f^*). Further, the filter current will be compared with the obtained reference value of the filter current i_f^* through the HCC to trigger the IGBT gates accordingly as illustrated in Fig. 3.11.

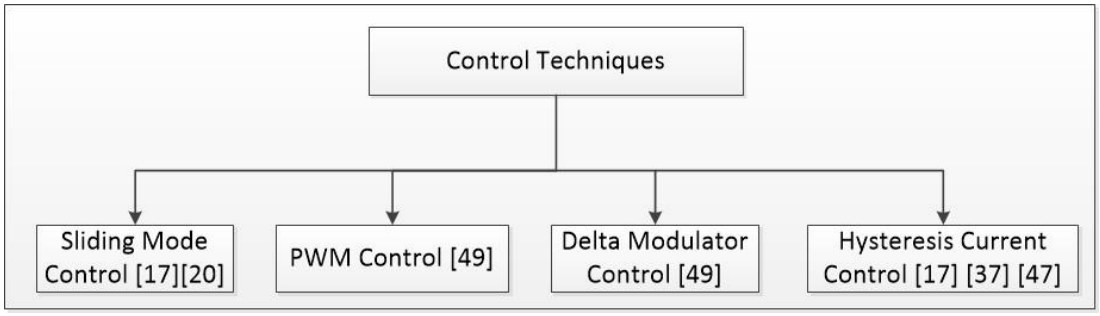


Fig. 3.10 Current control methods.

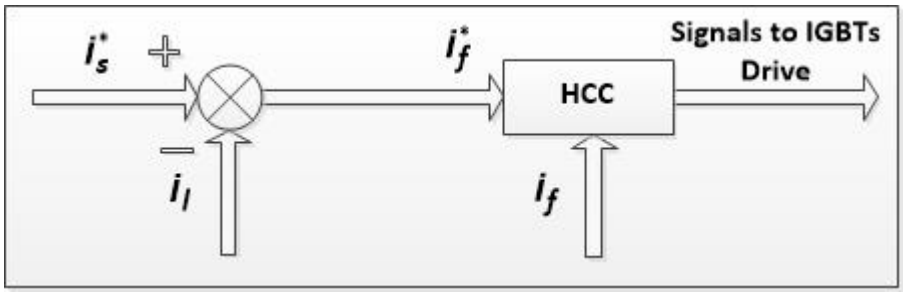


Fig. 3.11 Hysteresis current controller (HCC).

There is a trade-off between tracking error of the filter current and switching losses, the higher switching frequency the lower the tracking error and the higher switching losses and vise-versa [20]. Needless to say, low switching frequency results in waveform deterioration and phase shift [23]. The equations governing the filter current control can be derived by tracing Fig. 3.9, as follows:

$$i_s^* = \left[k_P(V_{DC}^* - v_{DC}) + k_i \int (V_{DC}^* - v_{DC})\, dt\right] \sin(wt) \tag{3.23}$$

We also know that:

$$i_f^* = i_s^* - i_l \tag{3.24}$$

where i_s^* can be represented as:

$$i_s^* = i_{l_p} + i_{Loss} \tag{3.25}$$

Here i_{l_p} is the real part of the load current and i_{Loss} represents the losses in the filter circuit; i_l can be represented as:

$$i_l = i_{l_p} + i_{l_q} + i_{l_h} \tag{3.26}$$

where i_{l_q} and i_{l_h} represent the reactive and harmonics parts of the load current, hence i_f^* can be re-written as:

$$i_f^* = i_{Loss} - i_{l_q} - i_{l_h} \tag{3.27}$$

3.3 Summary

In this Chapter, a literature review on active power filters has been conducted. Active power filters rely on detection of reference current from the load circuit. The MCU unit measures and calculates the reference source current. The filter will then inject an equal but opposite harmonic current so that at the PCC, the current theoretically should be a sinewave. There are numerous ways to extract the reference current including Instantaneous Reactive Power Theory [38], Synchronous Reference Frame Theory [45] [46], Fuzzy Logic [36], Neural Network [42] [43] [44], Phase Locked Loop [40] [48], Sine Multiplication [17] [21] [40], PI Control of Capacitor Voltage [40], Discrete Fourier Transform [41], Fast Fourier Transform [40] and Sliding Discrete Fourier Transform [20]. Since the supply voltage, v_S, is sinusoidal, estimation of the reference source current is accurate, hence, PI Control of Capacitor Voltage was chosen.

Current control techniques can be summarized to the following methods:

(a) Sliding Mode Control [17] [20].
(b) PWM Control [49].
(c) Delta Modulator Control [49].
(d) Hysteresis Current Control [17] [37] [47].

Amongst these methods, the Hysteresis current controller (HCC) technique was chosen for this research as it is accurate, easy to implement and requires the least calculations. Further, it does not add computational burden to the processor/MCU used.

Chapter 4 will model the appliances tested in Chapter 2 using MATLAB/Simulink and will simulate a SAPF to assess the filter compensation capabilities in two scenarios; a single appliance test and a multi appliance test.

Chapter 4: SAPF Circuit Simulations

MATLAB/Simulink software was used to simulate a SAPF. MATLAB is widely chosen among researchers due to its powerful computation capabilities and relative easiness to use for non-programmers. Simulink library in MATLAB provides extensive mathematical tools and specific libraries related to electrical and power engineering. Hence, it minimizes research time and effort to run the APF simulation. As mentioned earlier, the simulations will be carried out to compare the performance of the filter with different loads. Two scenarios were considered:

(a) The fridge as the non-linear load; the active filter circuit is represented as an active front end.

(b) All appliances as the non-linear load; the filter is placed on the feeder input (i.e. transformer secondary).

Simulink's SimPowerSystems library was utilized to run and test the aforementioned simulations. The circuit parameters are kept constant for the two tests to ensure reliable and relative results. The parameters set for the filter circuit are given in Table 4.1.

Table 4.1 Simulation circuit parameters.

Component	Value	Units
L_f	20	mH
C_{DC}	2200	µF
v_S	120	V
V_{DC}^*	360	V
$V_{DC_{pre}}$	169	V
f_{sw}	25	kHz
k_p / k_i	0.1 / 0.6	N/A

The value of V_{DC}^{*} was chosen to be slightly higher than twice the magnitude of $V_{DC_{pre}}$. For a 120 V supply voltage, equation 3.18 becomes:

$$f_{sw} = \frac{{v_{DC}}^2 - [169.71V \sin(wt)]^2}{2v_{dc} \,.\, L_f \frac{di_f}{dt}} \tag{4.1}$$

For V_{DC}^{*}= 360 V, k_P= 0.1 and k_i= 0.6, equation 3.23 becomes:

$$i_s^{*} = \left[(36 - 0.1v_{DC}) + 216 - \int (0.6v_{DC})\, dt\right] \sin(wt)$$

It is important to pre-charge the capacitor, as discussed in Chapter 3 and shown in Fig. 3.9. If the capacitor's initial charge is zero, then the big difference between the set point (SP) and the processed variable (PV) would cause the filter current to overshoot. Fig. 4.1 outlines the inrush current during transient period when the capacitor is not precharged. Therefore, the capacitor has been assigned a pre-charge value of $V_{PEAK} = 169$ V for the simulations in this chapter.

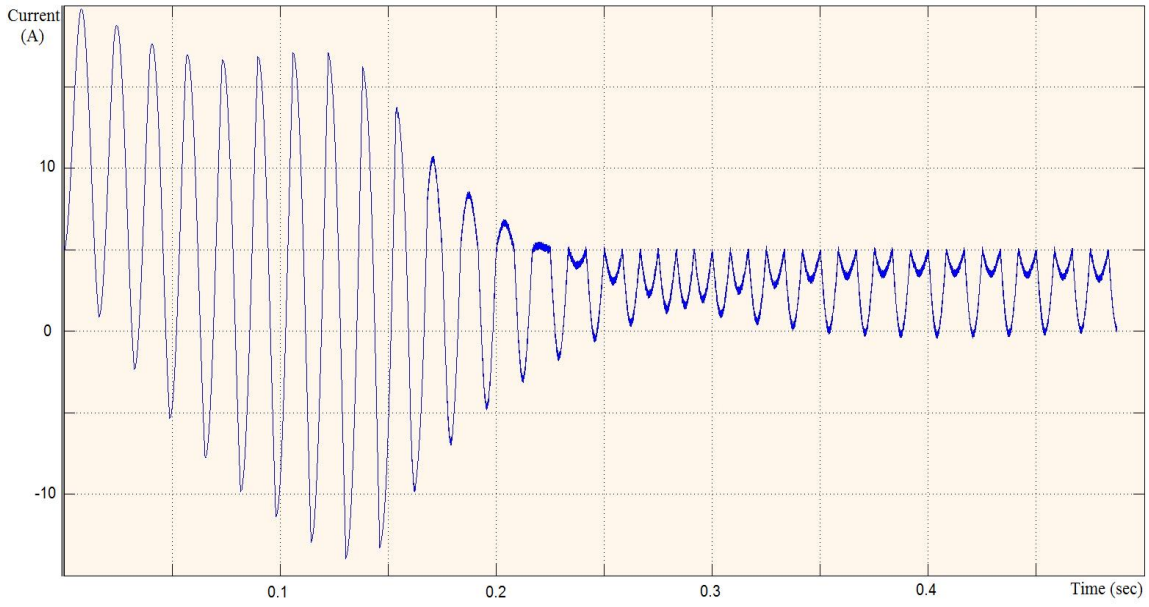
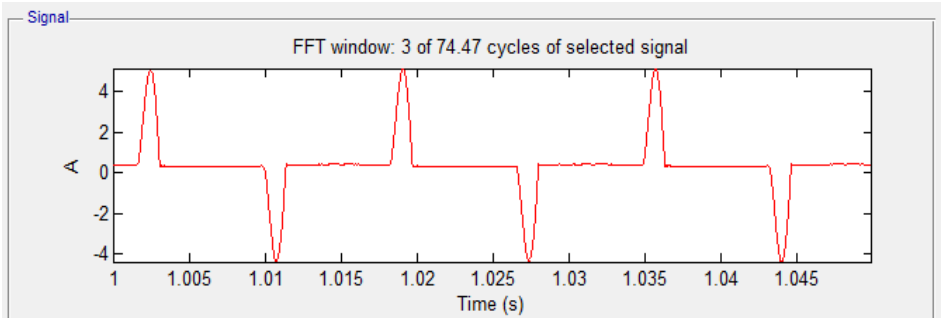


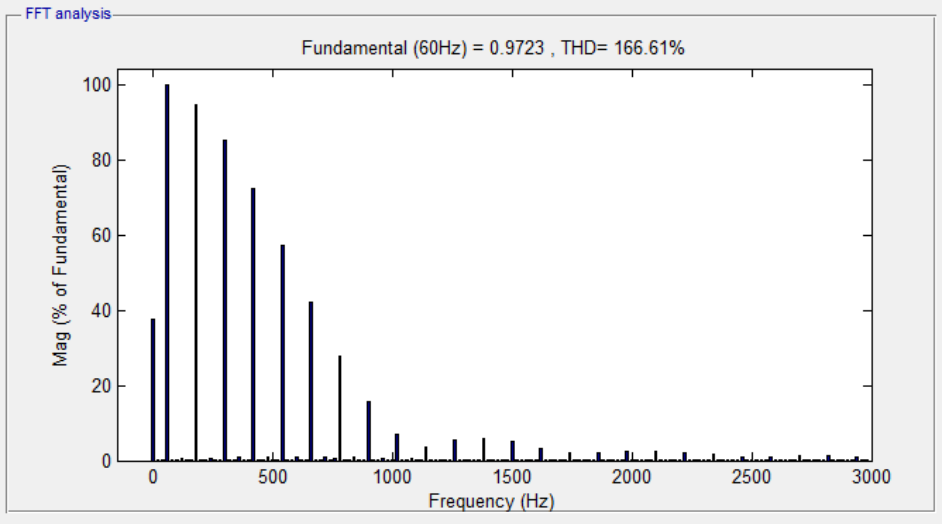
Fig. 4.1. Inrush current of the filter when the capacitor is not precharged.

4.1 Fridge as a Load

The filter, as an active front end, was tested on an LG LFX25778ST fridge. The fridge current measurements captured in Chapter 2 were used to represent the non-linear load in the simulation. The saved fridge current data was imported to Simulink's Signal Builder tool. The data from the Signal Builder block was then fed to a Controlled Current Source block to emulate the non-linear current of the fridge. The load current THD was analyzed and results are depicted in Fig. 4.2.



(a) Load current waveform.



(b) Load current frequency spectrum.

Fig. 4.2 Fridge load current, i_l, time and frequency domain simulation results.

The filter circuit was energized to compensate for the harmonics injected by the emulated fridge current. Fig. 4.3 shows the results obtained at the steady state operation of the filter. The filter was successfully able to bring down the THD of the source current (i_s) from 166.61% to 18.62%. The compensated source current was analyzed in time and frequency domains as shown in Fig. 4.4.

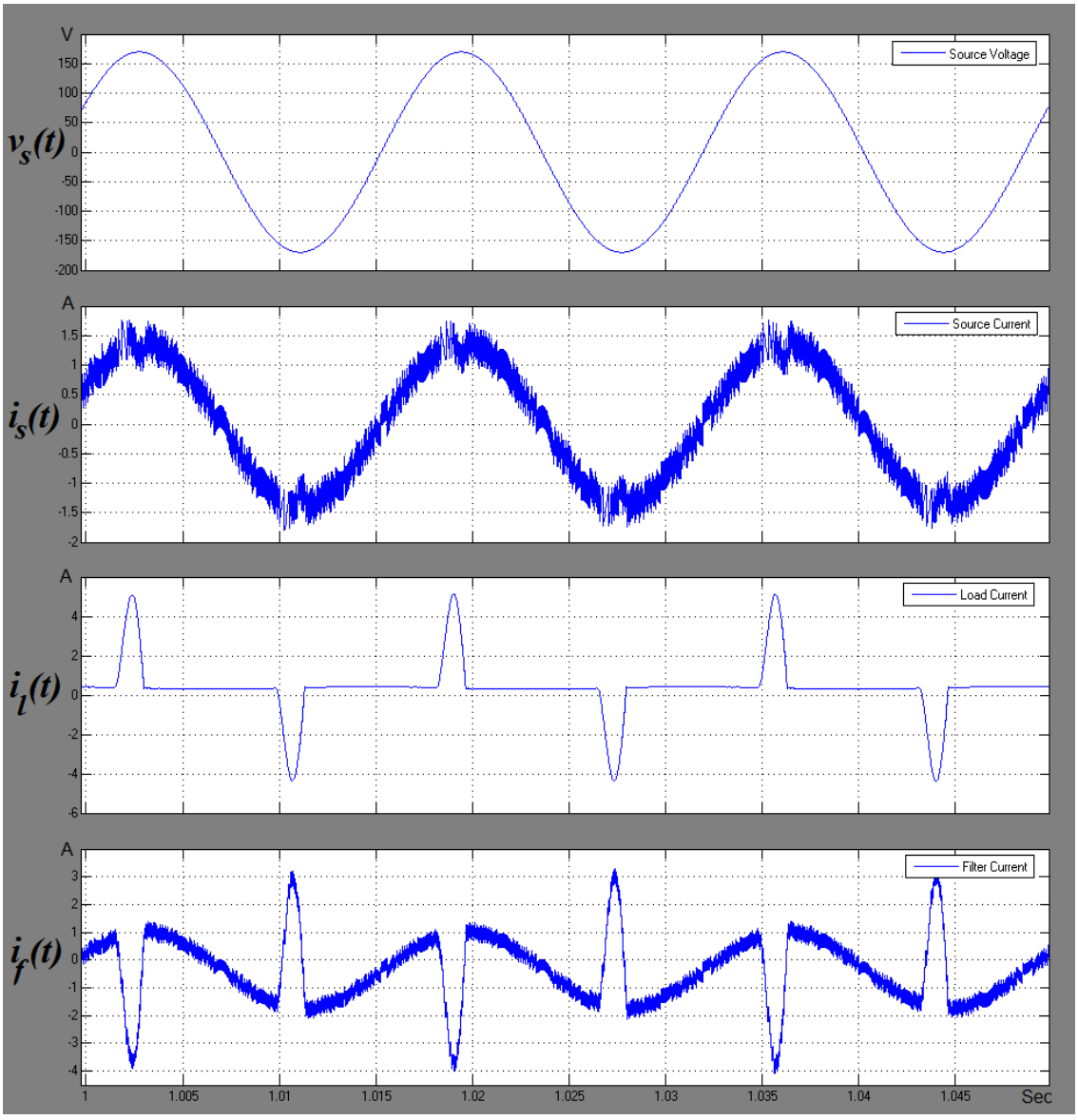
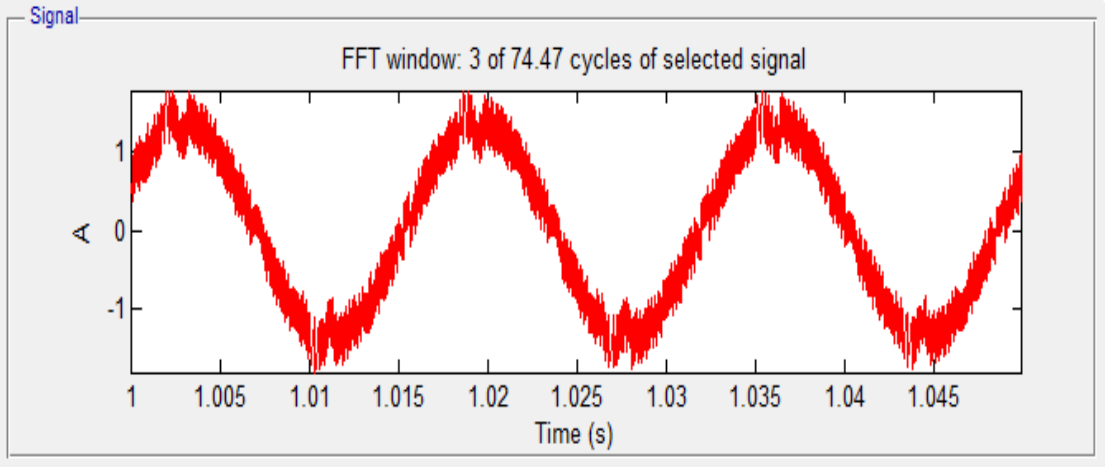
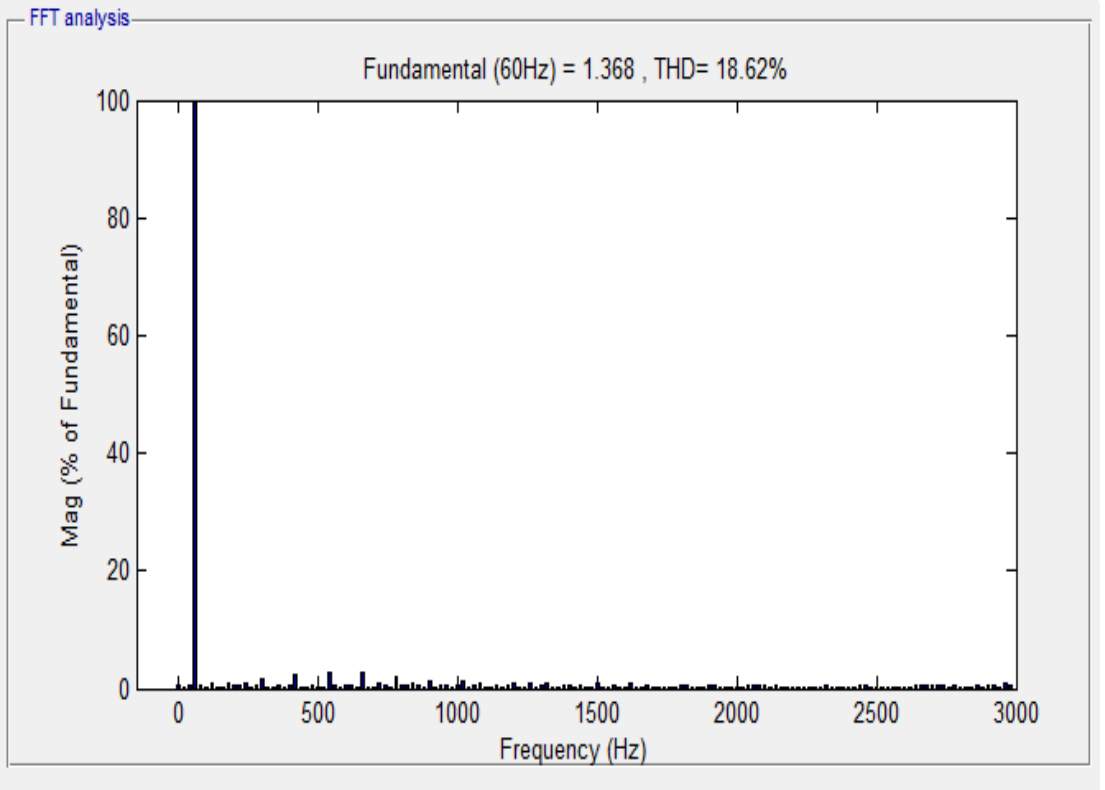


Fig. 4.3 v_s, i_s, i_l and i_f waveforms after filtering of the fridge current.



(a) Source current, i_s, in time domain.



(b) Source current, i_s, in frequency domain.

Fig. 4.4 Analysis results for source current, i_s, after compensation of fridge current harmonics.

4.2 Multi-Appliance Test

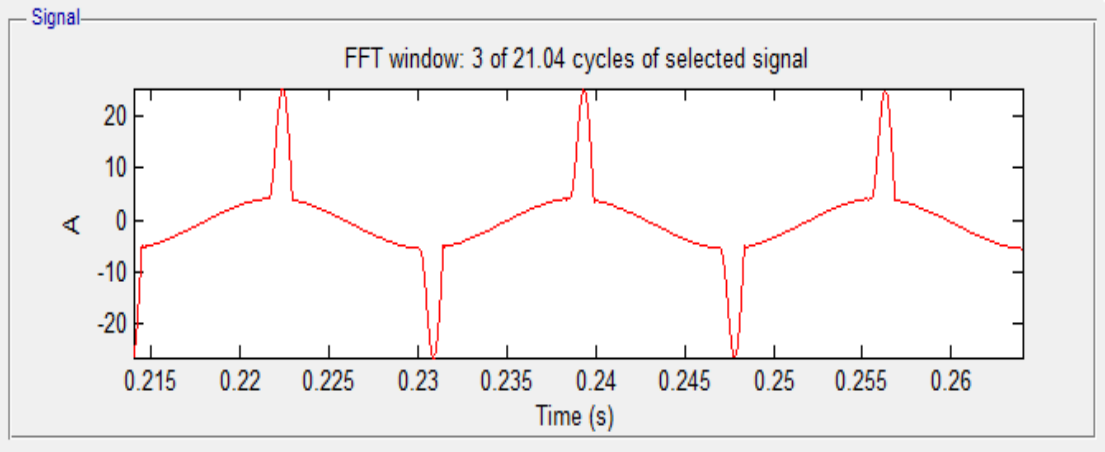
The filter as a feeder compensator was simulated to compensate harmonics generated by all of the appliances mentioned in Table 2.3. All of the filter's parameters were kept the same as in the case of a single appliance test (active front end), since the fridge is our testing benchmark. Similar to the fridge only scenario, the superimposed appliances current data was imported to MATLAB. The load current THD was analyzed and time and frequency domain results are depicted in Fig. 4.5.

The filter circuit was energized to compensate for the harmonics injected by the emulated appliances current. Fig. 4.6 shows the results obtained at the steady state operation of the filter. It can be noted that the source current after compensation is still distorted. The THD analysis also shows a very moderate improvement of the THD as depicted in Fig. 4.7, the THD reducing from 80.72% to only 51.04%. Thus, the filter's parameters need to be changed to properly filter the harmonics of a bigger load (Multi-appliance).

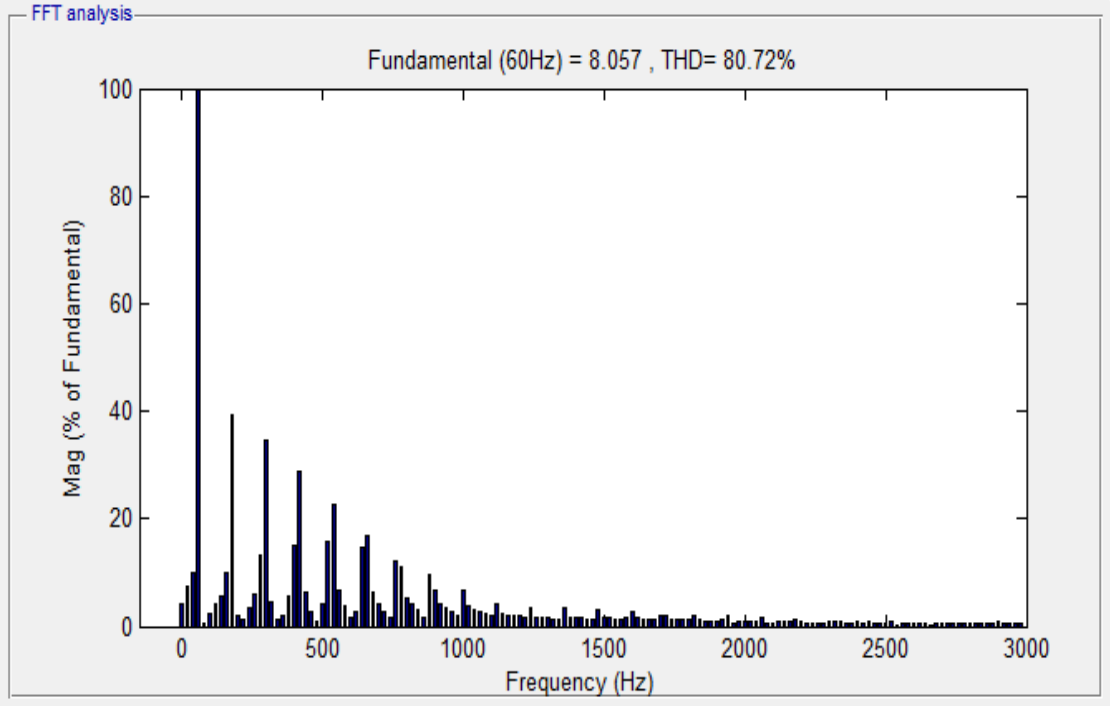
A logical reason for the poor performance of the filter is the inductor size, as it is evident from Fig. 4.6, the load current (i_l) is too large (peaks at 25 A) for the inductor to handle. It may be recalled that the proper inductor size is found by reference to equation (3.22). For a current that peaks at 25 A, an inductor size of 5 mH instead of 20 mH was chosen and the simulation repeated as in Fig. 4.8.

The results for the smaller 5mH inductance looks much better than in the case of the 20mH inductor. The filter was successfully able to bring down the THD of the source current (i_s) from 80.72 % to 13.67 %. The compensated source current was analyzed in the time and frequency domains as depicted in Fig. 4.9.

It can be noted though, that the effect of the switching frequency is prevalent on the source current. Since the inductor size is relatively smaller, this will allow for an increased ripple. To prevent this, carefully tuning the rest of the filter parameters is required so as to achieve a better response.



(a) Load current, i_l, in time domain.



(b) Load current, i_l, in frequency domain.

Fig. 4.5 Multi-appliance load current, i_l analysis results.

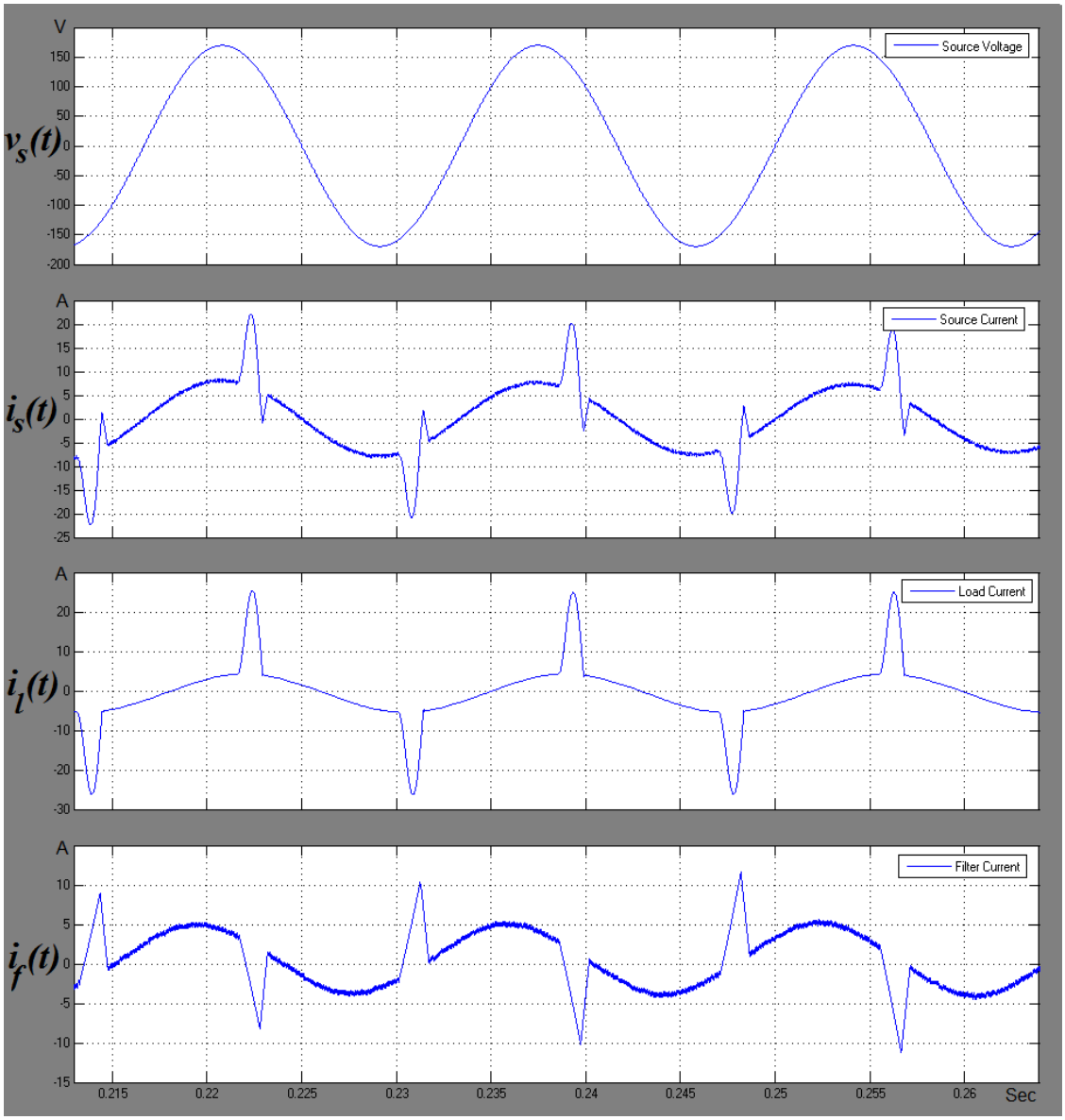
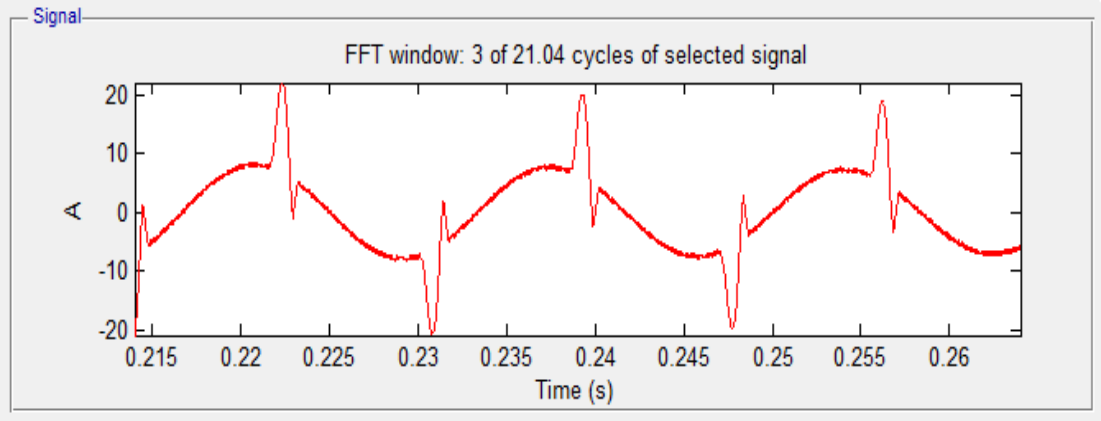
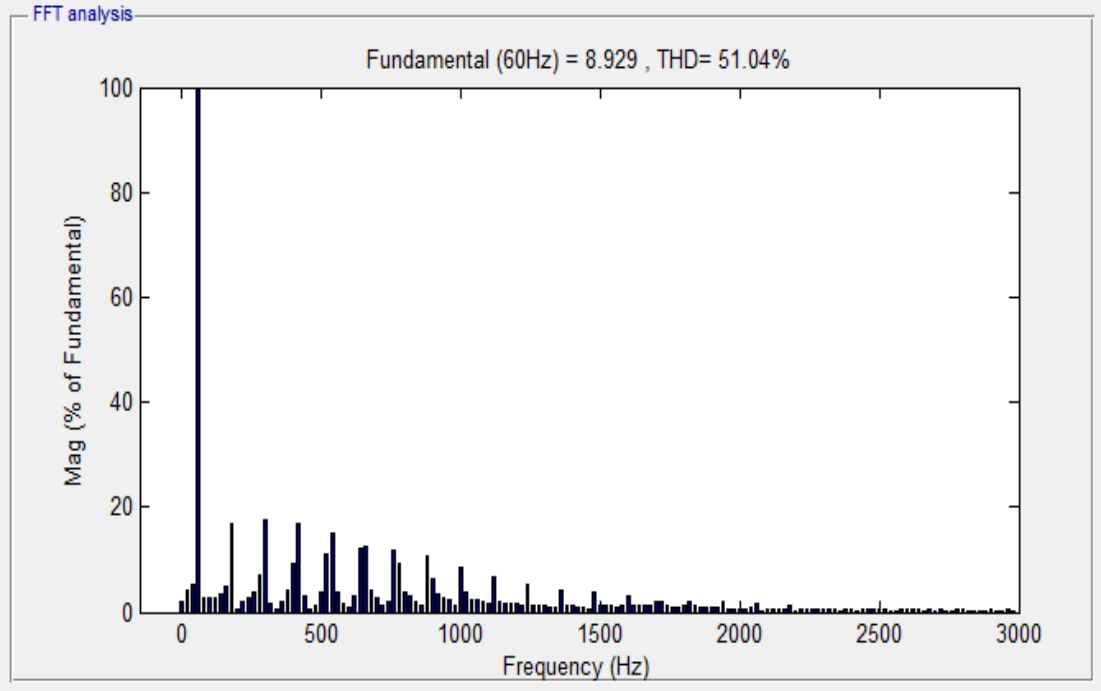


Fig. 4.6 v_s, i_s, i_l and i_f waveforms after filtering of the appliances current.



(a) Source current, i_s, in time domain.



(b) Source current, i_s, in frequency domain.

Fig. 4.7 Analysis of i_s after compensation of appliances current harmonics.

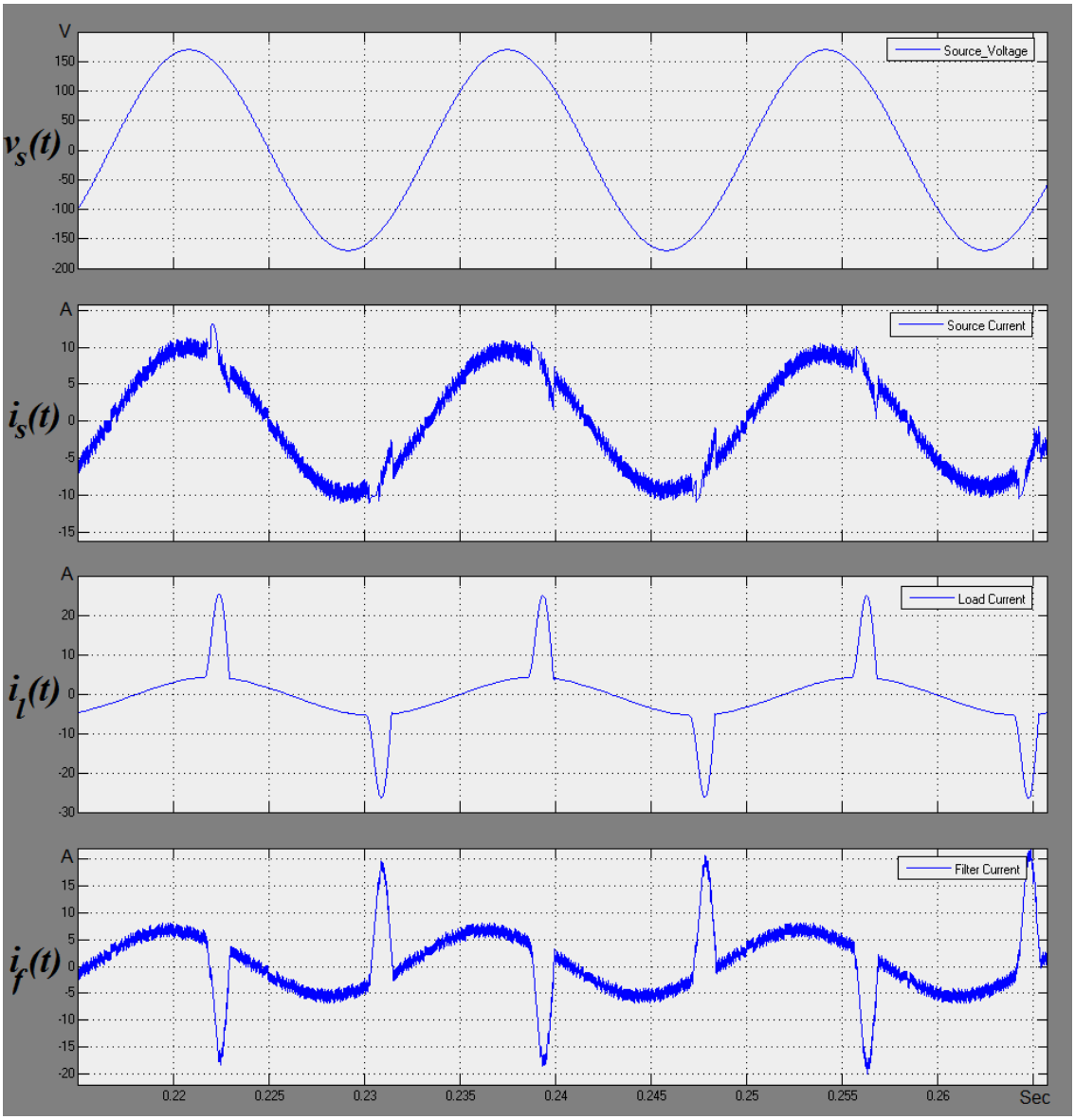
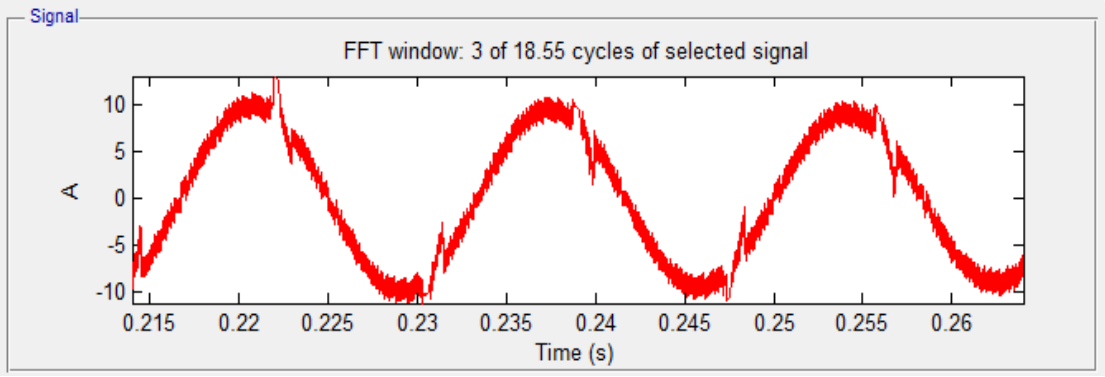
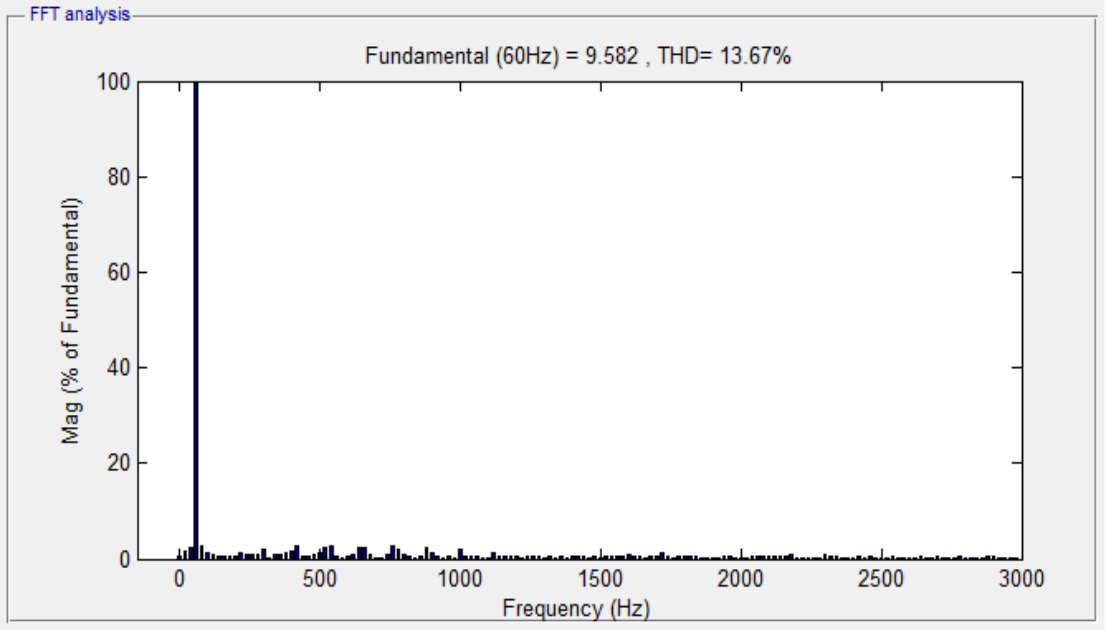


Fig. 4.8 v_s, i_s, i_l and i_f waveforms after filtering of appliances current when L_f =5 mH.



(a) Source current, i_s, in time domain.



(b) Source current, i_s, in frequency domain.

Fig. 4.9. Analysis of i_s after compensation of appliance current harmonics when L_f =5 mH.

4.3 Summary

A SAPF was simulated using MATLAB/Simulink library. Measured non-linear loads data from laboratory tests were imported and modeled using the Signal Builder block of Simulink. The operation of the filter was tested for two scenarios:

- as an active front end, where the filter compensated for current harmonics for a smart fridge.
- as a feeder compensator, where the filter compensated for current harmonics for various smart household appliances.

The filter rendered a better performance when used as an active front end, as the THD of the supply current went down from 166.61% to 18.62%. On the other hand, when used as a feeder compensator, the filter reduced the source current THD from 80.72% to only 50.04%.

It was obvious that the size of the line inductor played a big role in altering the filter performance. It can be noticed that the performance of the feeder compensator when L_f =5mH rendered a better result than when L_f =20mH as in Figs. 4.8 and 4.6 respectively.

In Chapter 5, a prototype will be built in a laboratory to emulate a SAPF in a real life situation. The filter's hardware will be tested to compensate for non-linear load current harmonics. The filter's performance will be assessed based on THD reduction and power consumption.

Chapter 5: Design Validation

5.1 Filter Prototype

To prove the results obtained from simulations in Chapter 4, a hardware prototype was built to attest the operation of the filter circuit and control algorithm. The filter prototype was designed to compensate current harmonics produced by a half wave rectifier load resistor.

A non-linear load was supplied from a 40 V RMS AC supply; the load is a combination of a diode in series with a heater cone (21Ω resistive element). For safety reasons, the supply voltage was not increased to 120 V RMS, since 120 V RMS will require the reference capacitor voltage (V_{DC}^{*}) to reach 350 VDC. Also, since we are interested in compensating the current harmonic distortion of the load, low supply voltage will not affect the filter operation as long as the load current is kept the same RMS magnitude as that of the simulation. This was accomplished by simply using a larger load (lower resistance).

The filter prototype was attached in parallel (shunt) with the non-linear load and the supply as shown in Fig. 5.1. The filter circuitry is decomposed of the following:

- A 2200 μF DC capacitor (C_{DC}) to store the energy required for the filter operation.
- A 250 Ω resistor ($R_{Charging}$) to limit inrush current.
- A mechanical switch to bypass $R_{Charging}$ once the capacitor is fully precharged.
- A 60 mH line inductor (L_f) to smooth and prevent high ripples of the filter current.
- 5A fuse to protect the filter circuit.
- Two IGBT legs, each leg has two IGBTs in series. Each IGBT has a diode in an anti-parallel configuration.
- An MT24 Gate Driver sourced from John G Peck Ltd., UK.
- An MCU to control the operation of the filter by switching the four IGBT switches.
- Measurement and monitoring circuitry.

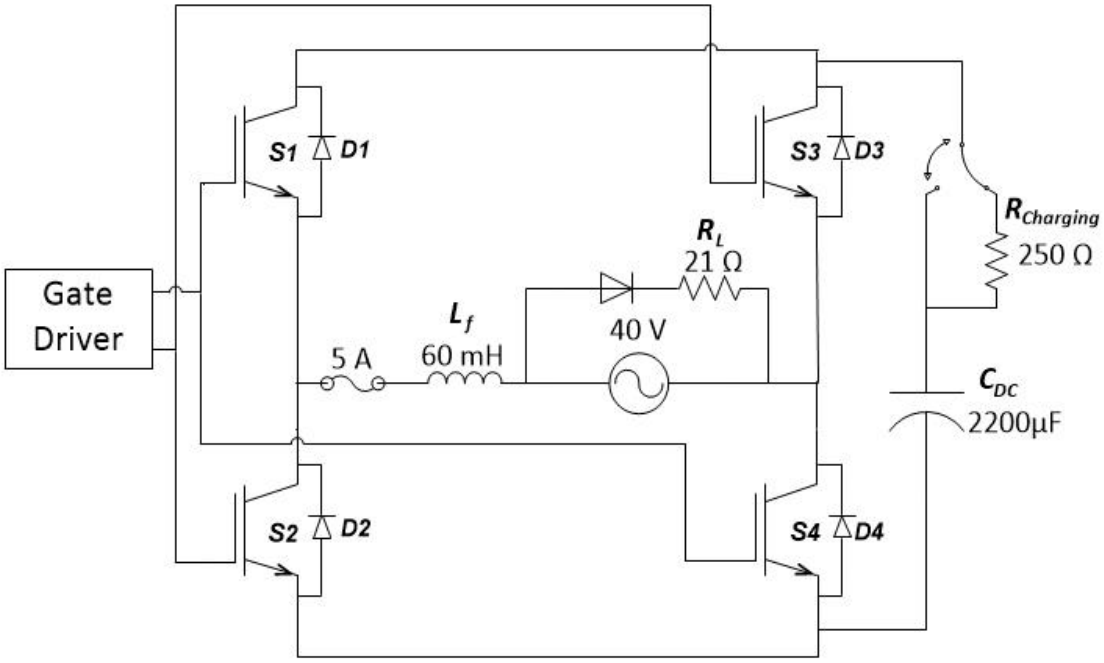


Fig. 5.1 Supply, load and main power circuit components for SAPF (MCU unit and measurement boards are not shown).

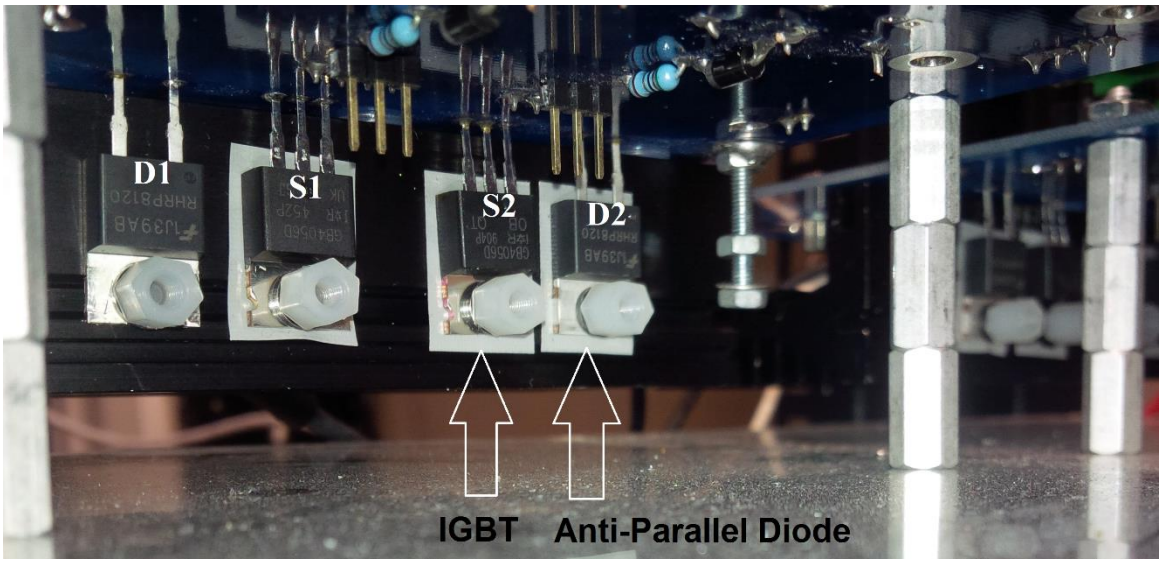


Fig. 5.2 IGBT leg, two IGBTs in series (with anti-parallel diodes).

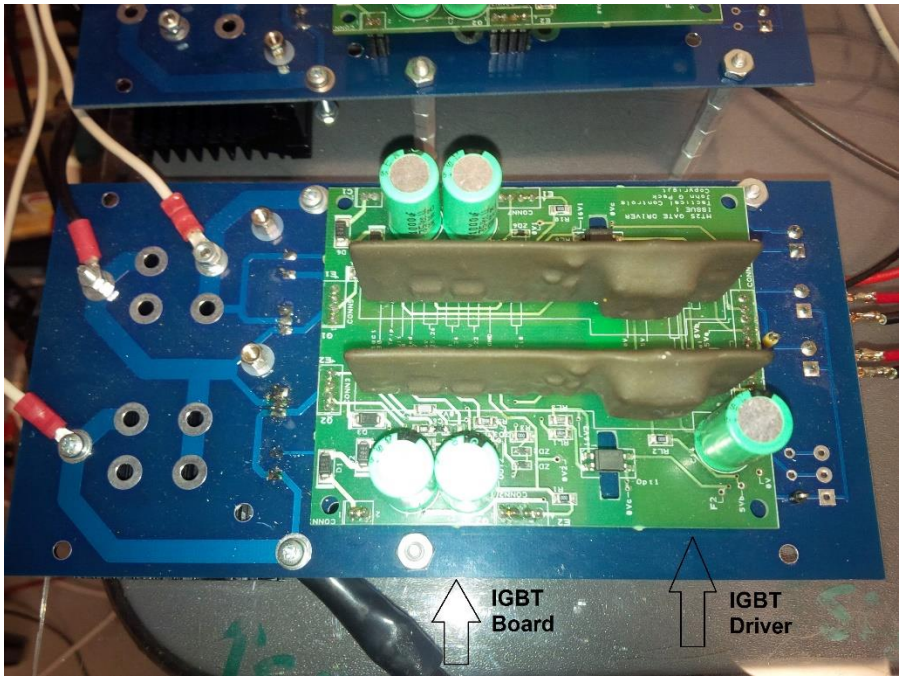


Fig. 5.3 IGBT leg (blue board) plus gate driver (green board).

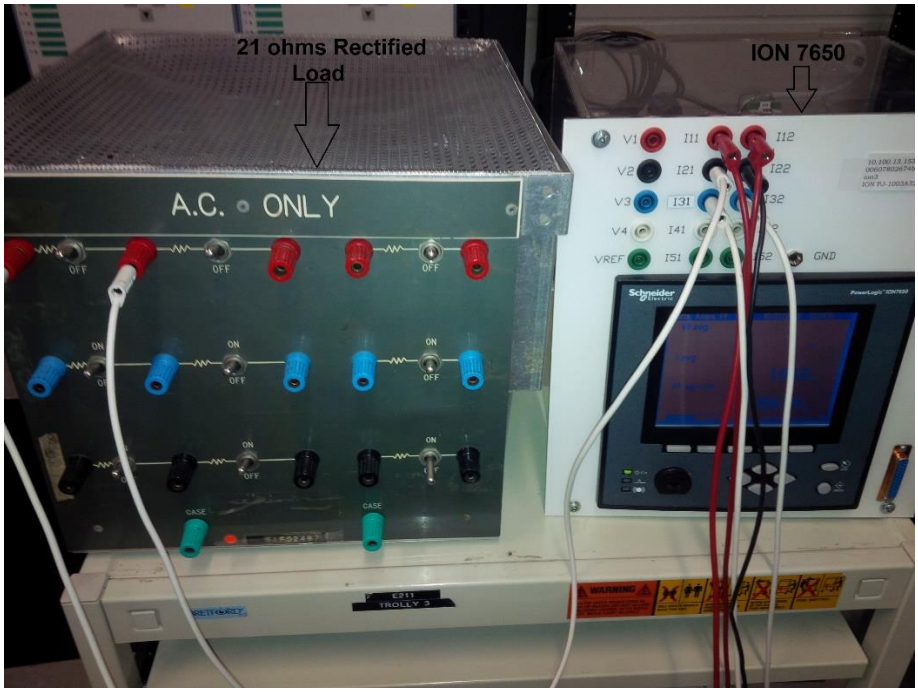
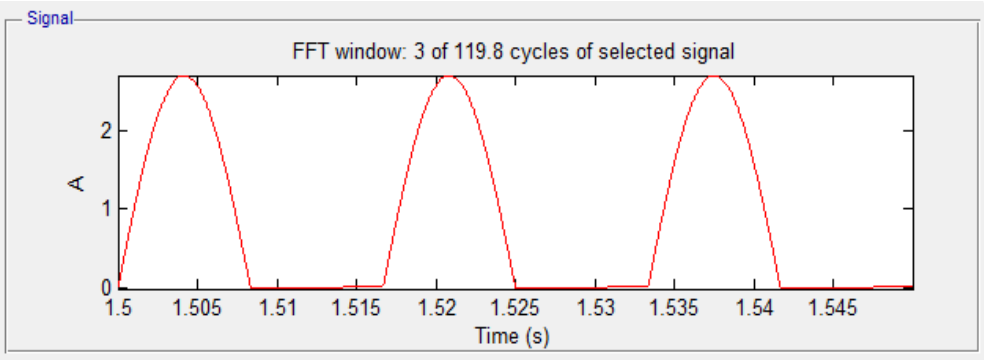


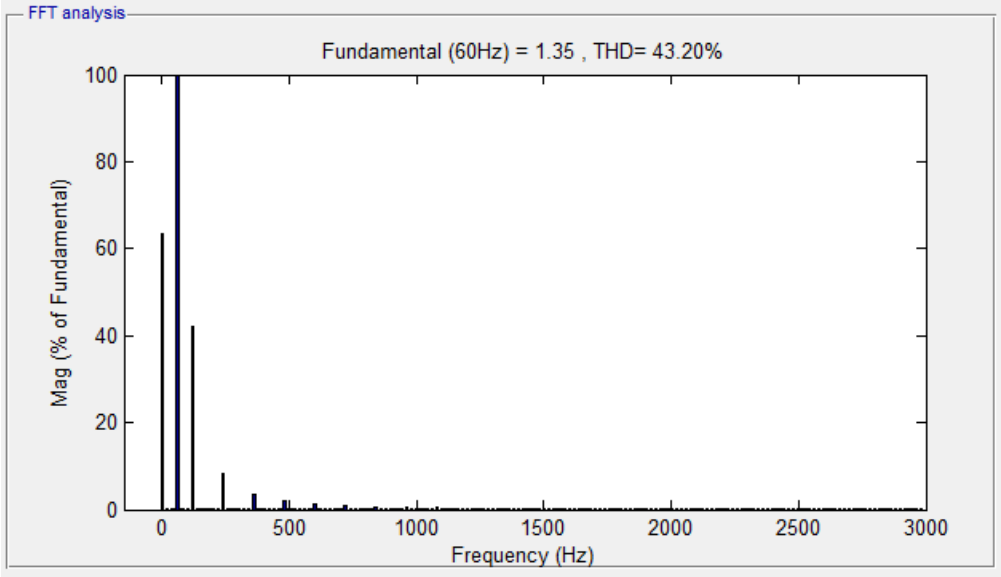
Fig. 5.4 Load and ION 7650 power quality meter.

In Fig. 5.2, the IGBT (denoted as S1 or S2) used has an IRGB4056D part number made by International Rectifier. Further, the diode (denoted as D1 or D2) has an RHRP8120 part number made by Fairchild Semiconductor.

The sizing of the inductor was chosen based on equation 3.22. The anticipated filter current can be calculated if the load THD is known. Therefore, a half wave rectifier load of 21 Ω supplied by 40V RMS has been simulated in Simulink and rendered a THD of 43.2%.



(a) Load current, i_l, in time domain.



(b) Load current, i_l, in frequency domain.

Fig. 5.5 Load current, i_l, for a typical half wave rectifier load.

Since the filter current theoretically should compensate for harmonics of the load current, we can refer to equation (2.6) to calculate i_f. Hence, we can obtain:

$$i_f = \%THD\ I_{fundamental\ of\ HW\ rectified\ Load} \tag{5.1}$$

Therefore, the required filter current:

$$i_{f=}(1.35\ A)\ (0.432) =\ 0.5832\ A$$

Assuming a maximum of 20% variation in the filter current, $\frac{di_f}{dt}$ can be calculated:

$$\frac{di_f}{dt} = (0.2)\ (0.5832\ A) = 0.1166$$

Hence, the filter inductor, L_f, can be calculated from equation (3.22):

$$L_f = \frac{120}{(2)\ (10^4)\ (0.1166)} \cong 51\ mH$$

Table 5.1 Hardware prototype parameters.

Component	**Value**	**Units**
R_L	21	Ω
L_f	60	mH
C_{DC}	2200	µF
v_S	40	V
V_{DC}^*	120	V
$V_{DC_{pre}}$	53	V
f_{sw}	10	kHz
k_p / k_i	0.1 / 0.6	NA
$R_{Charging}$	250	Ω

To cope with component availability in the laboratory, a 60 mH inductor was chosen for the prototype. The parameters set/used for this experiment are presented in Table 5.1.

Equation 3.23 can then be rewritten as:

$$i_s^* = \left[(12 - 0.1v_{DC}) + 72 - \int (0.6v_{DC})\, dt\right] \sin(wt)$$

Also, a 5A fuse was added in series with the inductor as in Fig. 5.1., to prevent excess in filter current in case of filter malfunction.

The theoretical precharge value of the capacitor should almost equal to the peak of the supply voltage ($V_{DC_{pre}} \approx V_{PEAK}$). Hence, $V_{DC_{pre}} = 40\sqrt{2} = 56.6$ V, but in reality, there is voltage drop across the switches, therefore, the full precharge value of the capacitor was about 53 V. In order to prevent the inrush current through the capacitor, the capacitor has to be pre charged through a 250 Ω resistor.

5.1.1 Measurement Boards

A Tamura 3FD-210, which is a regular low frequency (60 - 400Hz) step-down isolated voltage transformer (PT) was used to monitor the supply voltage. The PT's frequency range is optimal since we are only interested in the fundamental component (i.e. 60 Hz). The stepped-down voltage was fed to a signal conditioner to offset the signal above 0V. Fig. 5.6 shows the supply voltage monitor circuit.

The load and the filter currents were measured using an LEM LA 55-P, a high frequency current transducer (CT). The CT has a Hall-effect sensor to accurately measure all of the frequencies in the signal. The two signals were also offset to prevent damaging the MCU's analog inputs. Fig. 5.7 and 5.8 show the acquisition of the load and filter currents respectively.

Finally, the voltage of the capacitor was measured using an LEM LV 25-P, a high accuracy voltage transducer (VT), as depicted in Fig. 5.9. Since the voltage of the capacitor is always positive, there was no need for a signal conditioner circuit.

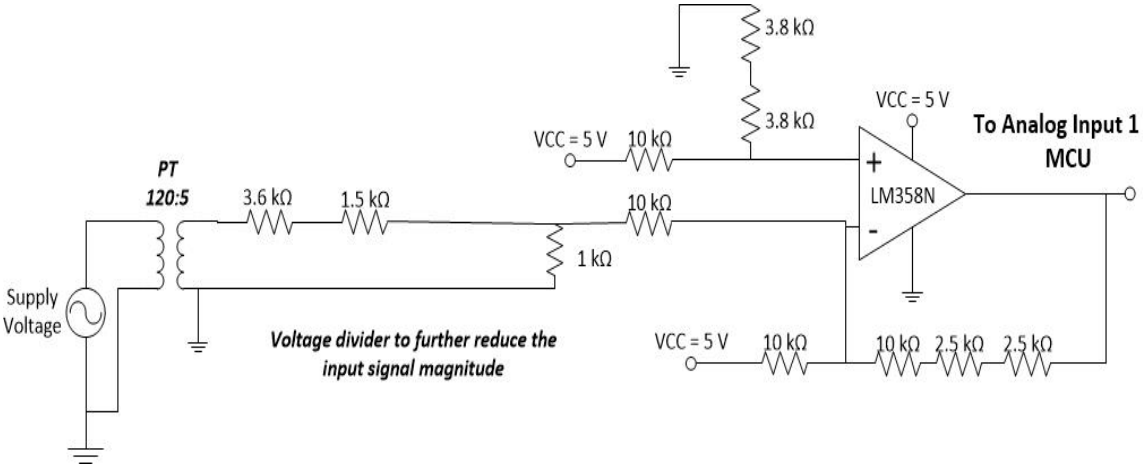


Fig. 5.6 Supply voltage monitor circuit.

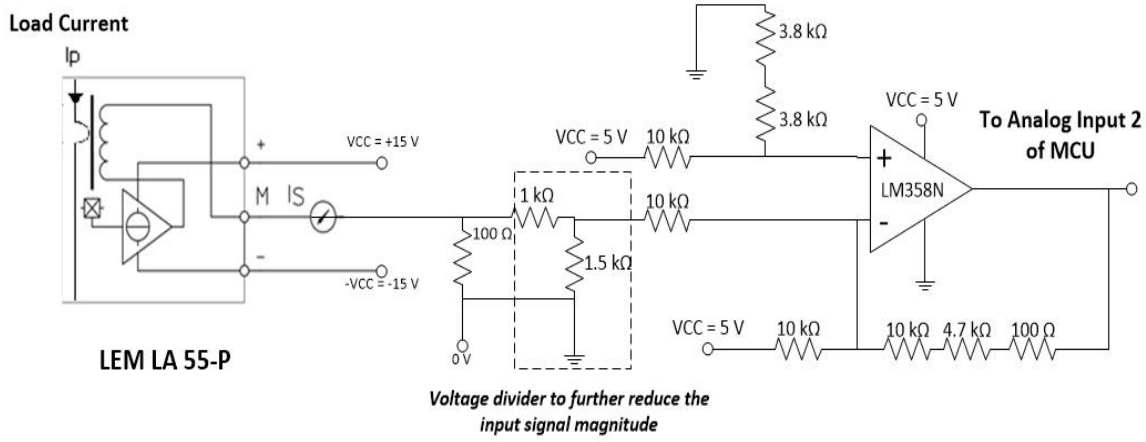


Fig. 5.7 Load current measurement circuit.

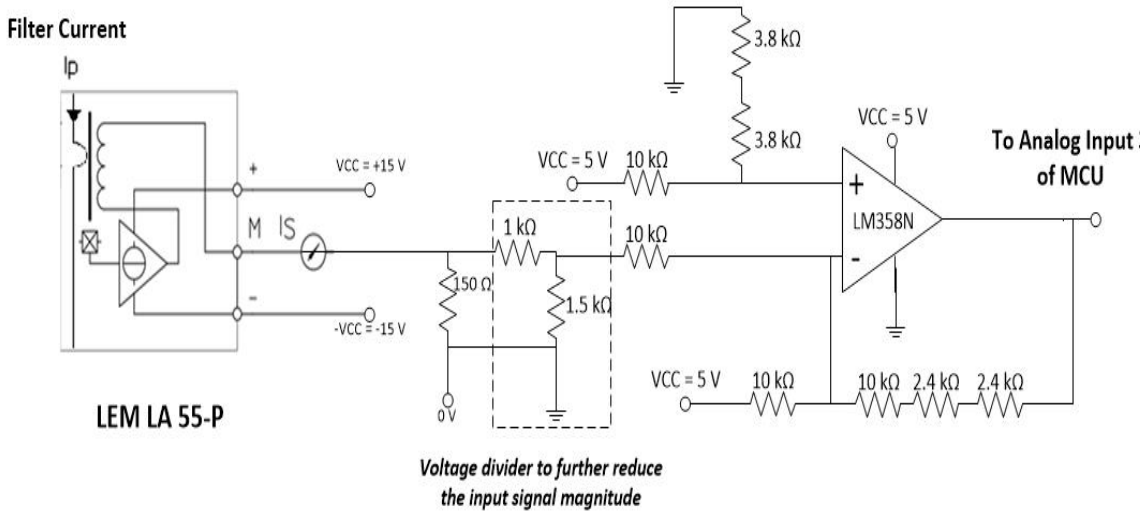


Fig. 5.8 Filter current measurement circuit.

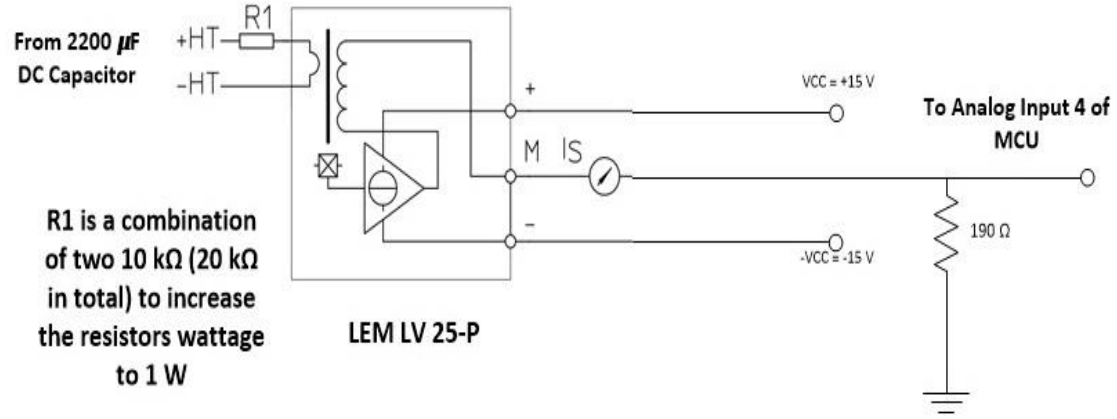


Fig. 5.9 Capacitor voltage measurement circuit.

5.1.2 MCU

There are many available microcontrollers that are fast and reliable. For this application, it was determined that it was preferable to use a microcontroller that allows for automatic conversion of Simulink model to C-code, then download the C-code to a stand alone MCU. This procedure significantly reduces the burden of programming a lengthy code and eliminates possible errors generated from line coding.

An aMG Labkit F4S kit has been used based on a FIO 2 board by Aimagin, the MCU has a built-in 32-bit ARM Cortex-M4 STM32F417IG. With a core frequency operating at up to 168 MHz, the Cortex-M4 core features a Floating Point Unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a Memory Protection Unit (MPU) which enhances application security [26]. The Analog inputs of the MCU are rated to sample voltages between 0-3.3V. Hence, it is crucial to offset and condition the input signals to prevent damage to the analog inputs of the microcontroller as explained earlier in section 5.1.1.

5.1.3 Operating the Filter

Careful measures need to be taken to operate the filter. To ensure safety, the following has to be considered:

- After connecting the filter circuitry to the supply and prior to running the filter, the DC capacitor (C_{DC}) will automatically charge to almost V_{PEAK} through the diode bridge as in Fig. 5.1. A resistor ($R_{Charging}$) must be present in series with the DC capacitor to limit inrush current. Once the capacitor is charged to $V_{DC_{pre}}$ value, then the resistor has to be bypassed by the use of a switch.
- Increasing the electrical quantities (current and voltage) in the circuit would result in higher measurands, which could damage the analog inputs to the MCU if it exceeds the upper and lower limits (3.3V and 0V respectively).

- The filter algorithm can only be run, if the aforementioned steps has been conducted.
- To stop the filter, digital outputs that pulses the gate driver have to be turned off (assigning a value of zero to the outputs).

The code for the MCU was first created using Simulink, Appendix A shows the complete code. Further, the code was converted to C using the Waijung library and got downloaded to the MCU using ST-LINK/V2. The MCU processes real-time discrete measured data (using analog inputs) and outputs pulses (using digital outputs) to trigger an IGBT gate driver, as per the control algorithm described in sections 3.2.3 and 3.2.4. The driver is an MT24 Gate Driver sourced from John G Peck Ltd., UK. The four IGBTs get switched based on the control signal coming from the gate driver. An ION 7650 power quality meter and a TPS2014B Tektronix oscilloscope was utilized to measure the supply voltage, load current, filter current and source current.

Fig. 5.10 display a magnified view of the MCU and the peripherals associated with it, while Fig. 5.11 shows the full laboratory experimental setup.

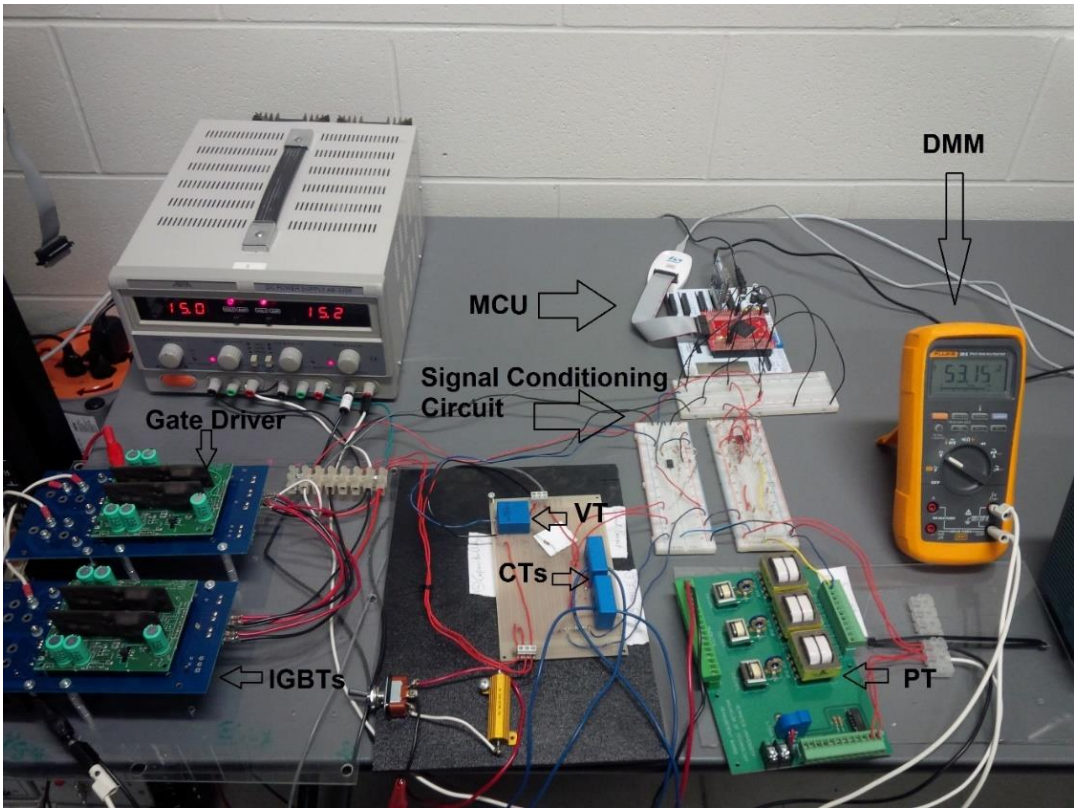


Fig. 5.10 Experimental setup showing gate driver on the left, measurement and data acquisition boards at the bottom and the MCU at the top right.

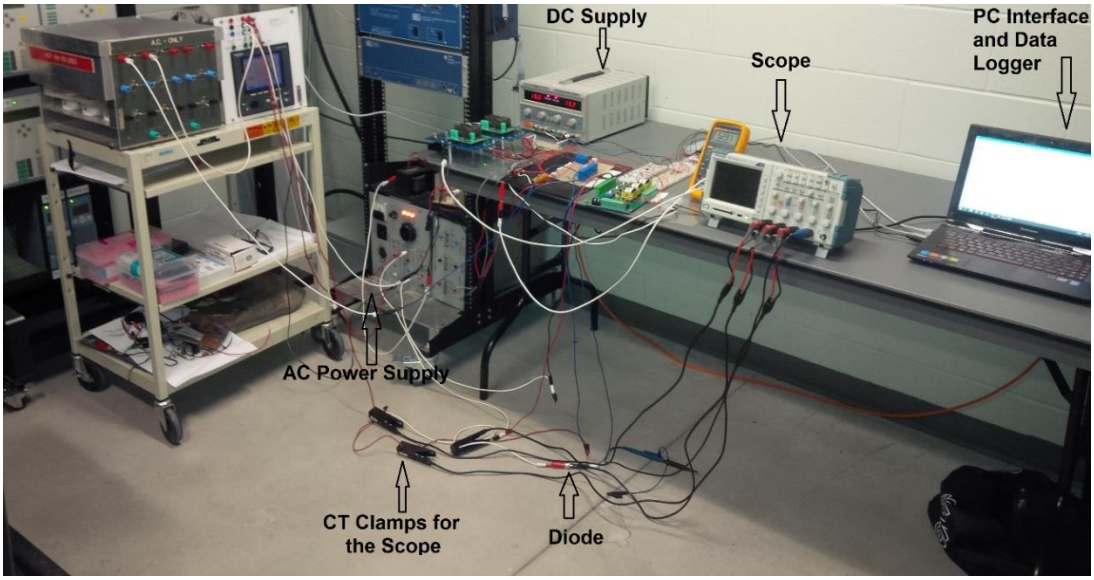


Fig. 5.11 Full laboratory experimental setup.

5.2 Filter Performance and Results

While running the filter, measured waveforms displayed by TPS2014B Tektronix oscilloscope were also recorded using the ION 7650 power quality meter as shown in Figs. 5.4 and 5.11. Vista, the software interface for the ION 7650 was triggered to capture source voltage, source current, load current and filter current at steady state. The hardware results showed a superb improvement of the source current as shown in Fig. 5.12. For the first half cycle, the filter current is acting in a way such that it reduces the magnitude of the load current. For the second half cycle, the filter current is injecting a current in the opposite direction. Superimposing the load and the filter waveforms will result in a sinusoidal waveform of the source. Although the resulted sinewave of the source current has ripples, it certainly looks way better than if it was just half wave rectified sinewave. Fig. 5.12 shows the time domain capture of the source, load and filter currents. The figure not only shows a sinusoidal waveform for the source current, but also shows a great reduction of the peak value of the load current. Further, the frequency spectrum for all three currents is depicted in Fig. 5.13. The harmonic content for each current waveform was calculated based on an average of three cycles. The THD of the supply current greatly improved as it went down from 44.2% to only 5.4% as indicated in Table 5.2 and shown in Fig. 5.13. Fig. 5.16 shows a computer simulation of the hardware prototype to affirm the results obtained. The resultant i_s after filtering of a 21Ω half wave rectifier load renders a THD of 5.36%.

Table 5.2 Old vs. new THD for all measured waveforms.

Waveform	**Old THD % (No Filtering)**	**New THD % (With Filtering)**
Source Voltage	1.8	1.94
Source Current	44.4	5.4
Load Current	44.4	44.4
Filter Current	N/A	273.8

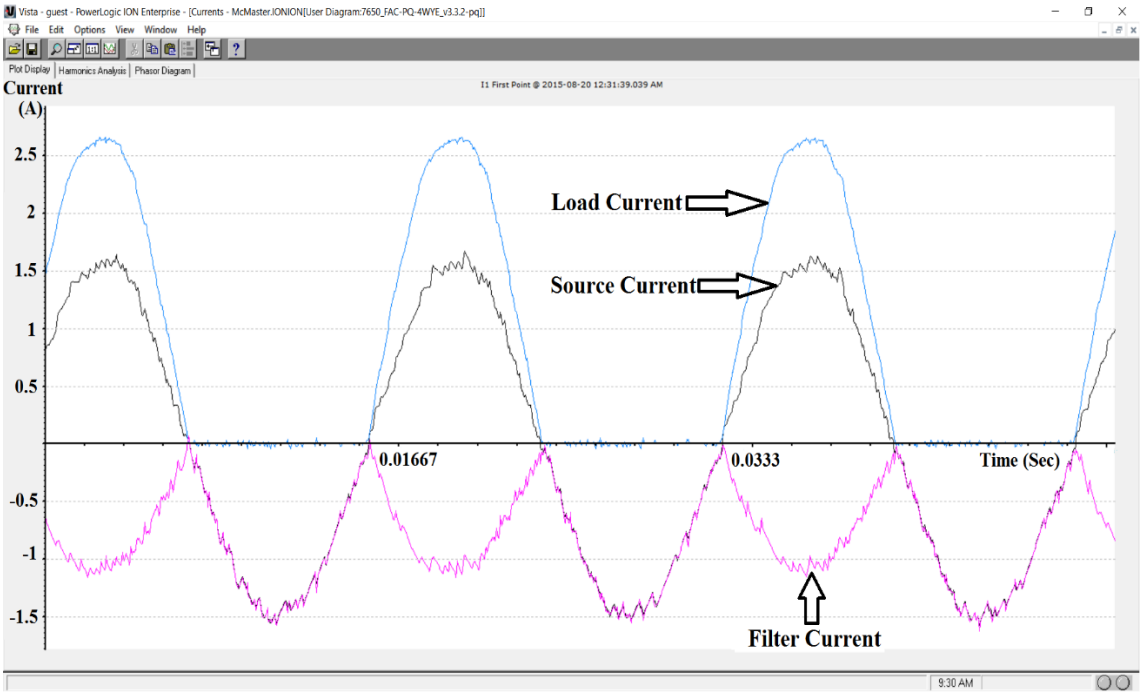


Fig. 5.12 Measured current waveforms for i_s , i_l and i_f after filtering of harmonics.

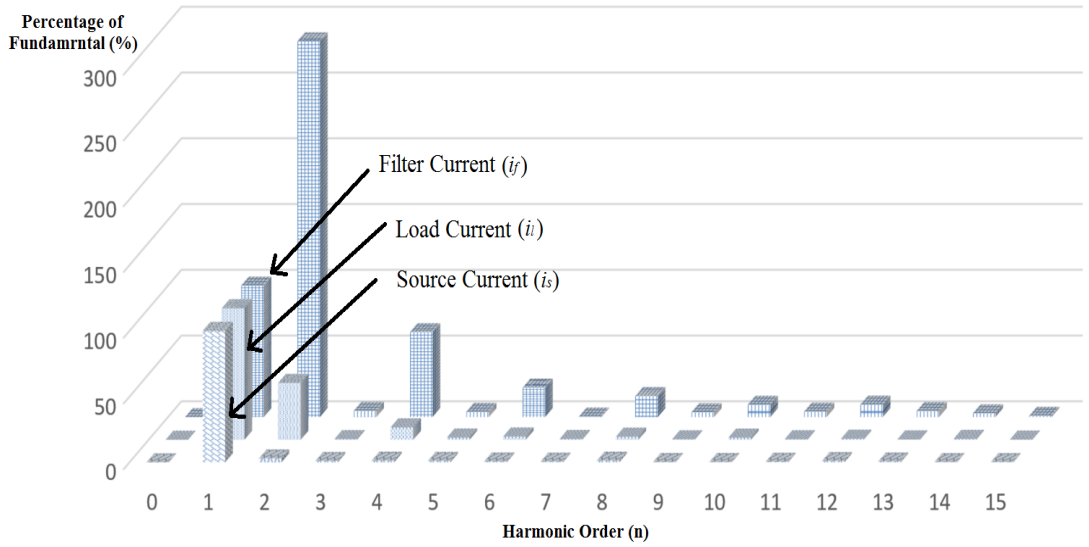


Fig. 5.13 Measured frequency spectrum of i_s, i_l and i_f after filtering of harmonics.

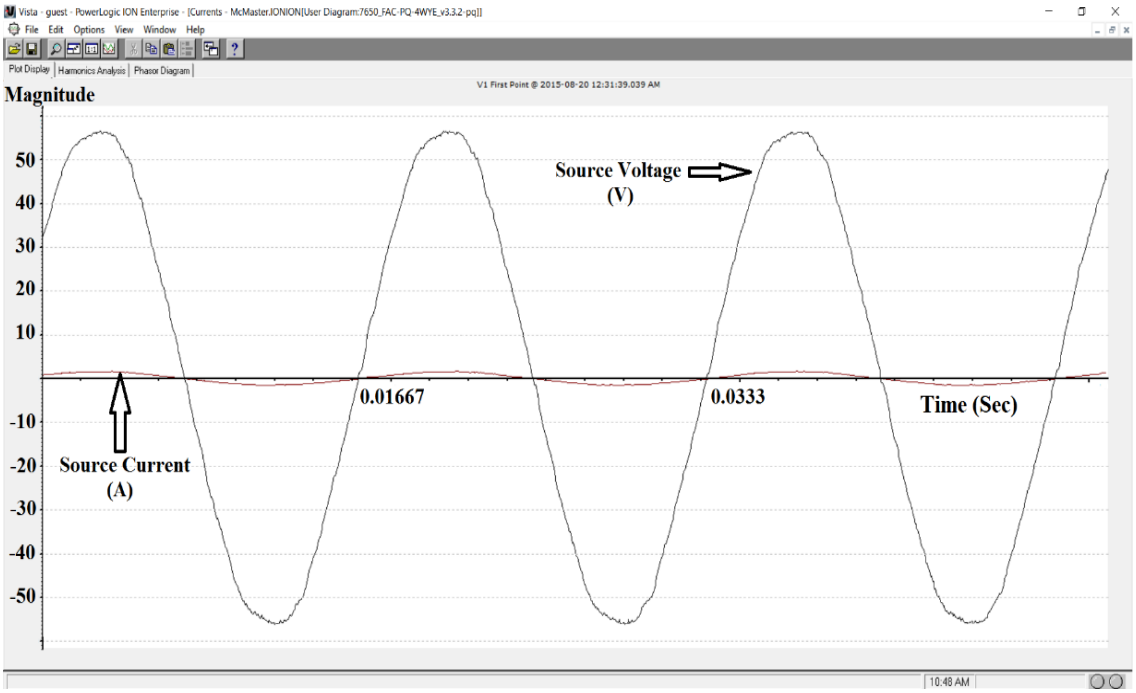


Fig. 5.14 Supply current, i_s, and supply voltage, v_s after filtering of harmonics.

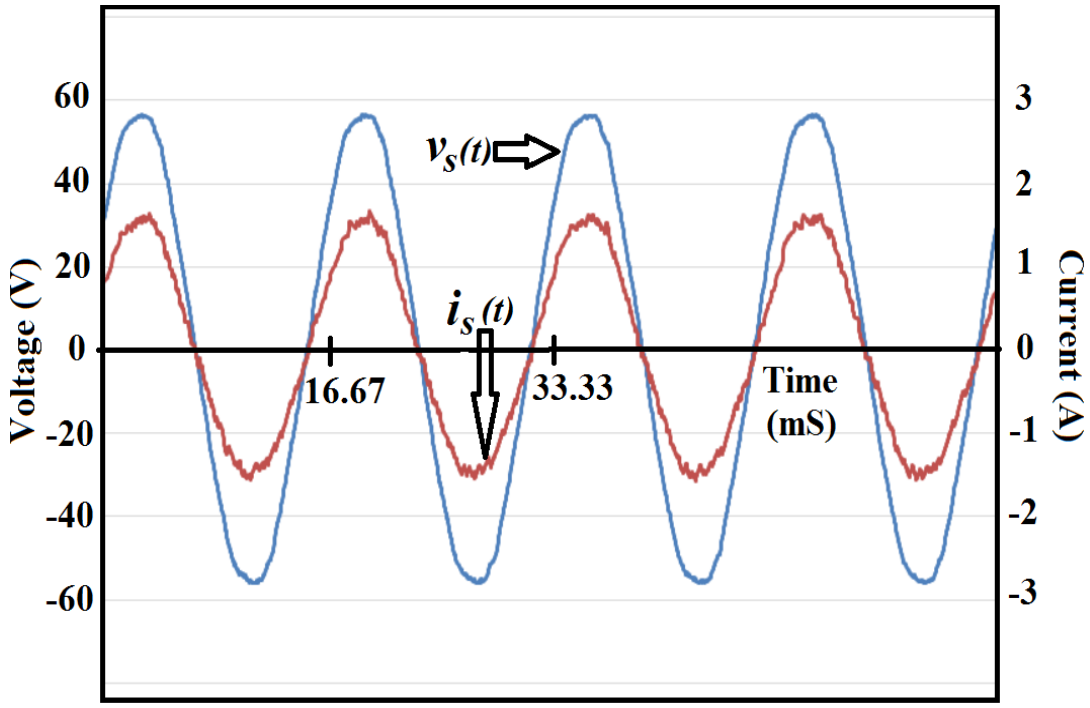
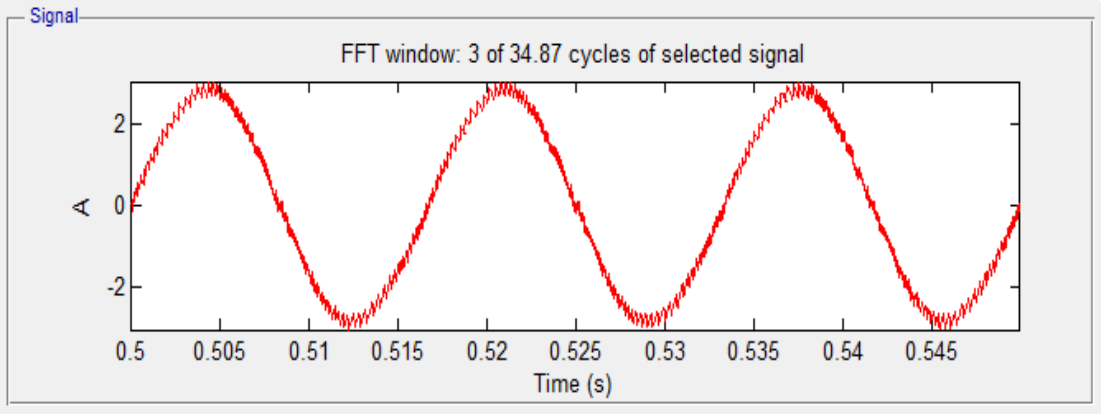
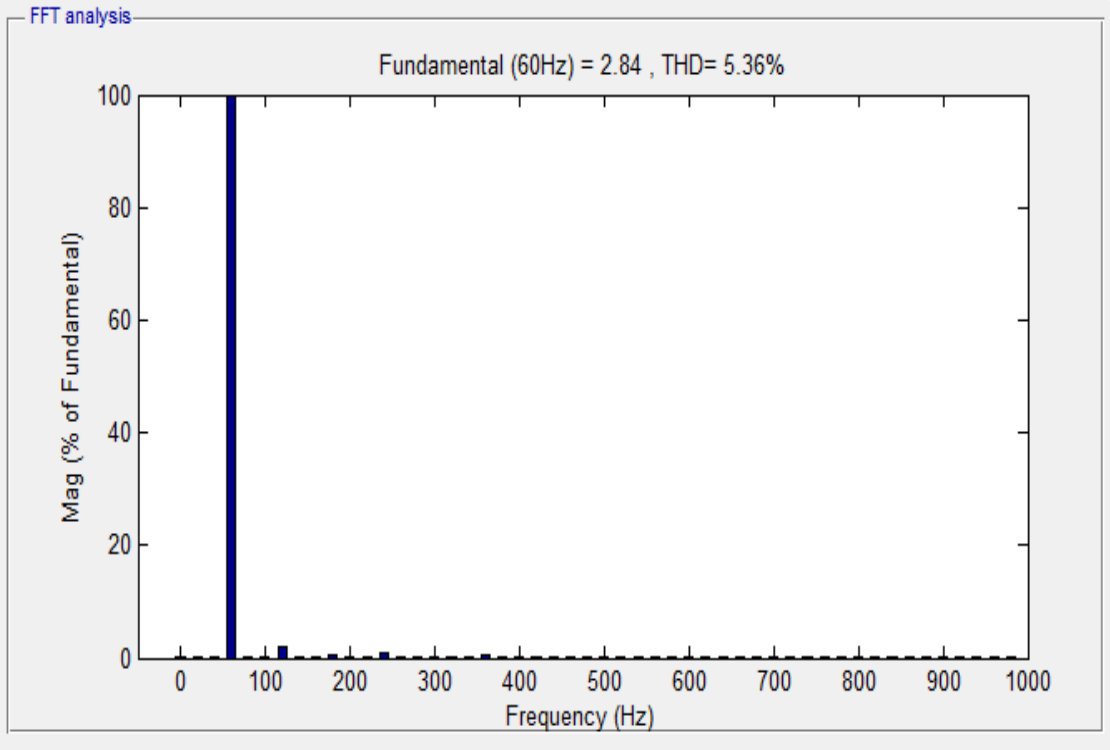


Fig. 5.15 Supply current, i_s, and supply voltage, v_s phase relation.



(a) Supply current, i_s, waveform.



(b) Supply current, i_s, in frequency domain.

Fig. 5.16 Simulation of i_s, after filtering of a 21Ω half wave rectifier load.

5.2.1 Power Consumption

To determine the feasibility of implementing the filter, power consumption by the filter need to be calculated. First, the power was calculated without the filter, meaning, only with the non-linear load. Since there is only the load, the source current, i_s, will equal to the load current, i_s. Knowing the sampled data of source voltage, v_s, and source current, i_s, the apparent power (S) can be obtained:

$$S(n) = v_s(n)\, i_s(n) \tag{5.1}$$

where, n is the sample number.

Since the source voltage and current waveforms are in phase, apparent power and real power are the same. Further, equation 5.1 can be written:

$$P(n) = S(n) = v_s(n)\, i_s(n) \tag{5.2}$$

Fig 5.17 shows the sample product of the source voltage and source current over 3 cycles. The average power was calculated to be 38.47 W.

The calculations were repeated using equation 5.2 to determine the power consumption with the filter in parallel with the load. Fig 5.18 shows the sample product of the source voltage and source current over 3 cycles. This time, the source current consists of the load and filter current. The average power was calculated to be 43.75 W. Hence the filter power consumption can be calculated:

$$P_{Filter} = P_{post} - P_{pre} \tag{5.3}$$

Therefore, the filter power consumption is 5.28 W. This power consumption represents switching losses and energy used by the DC capacitor. Further, adding the filter to the circuit increased the total supply power by 13.7%.

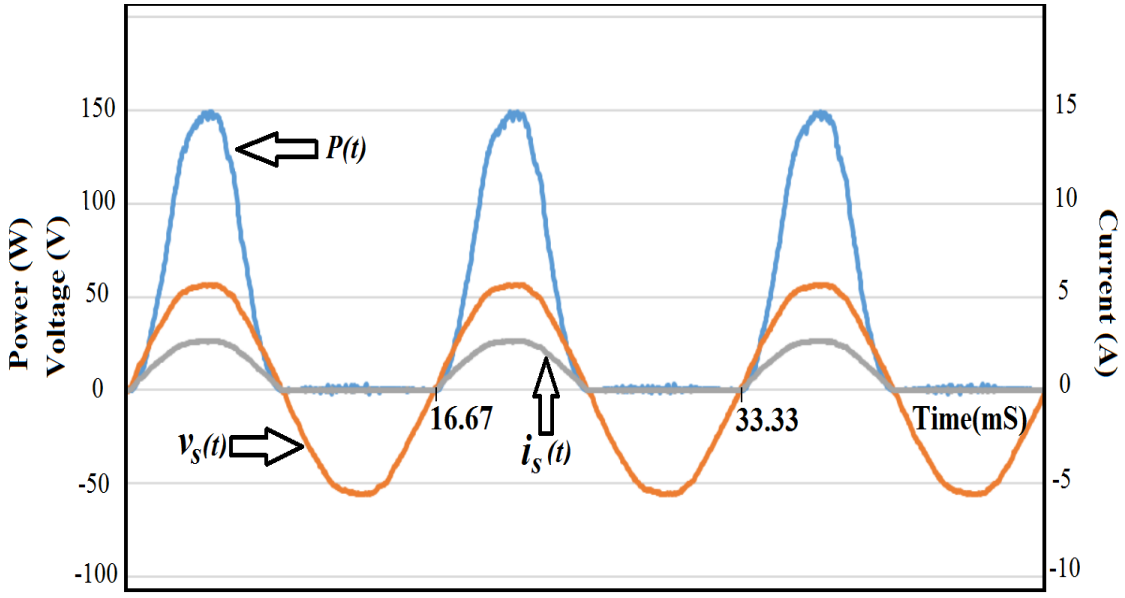


Fig. 5.17 Calculated power, *P*, with load only.

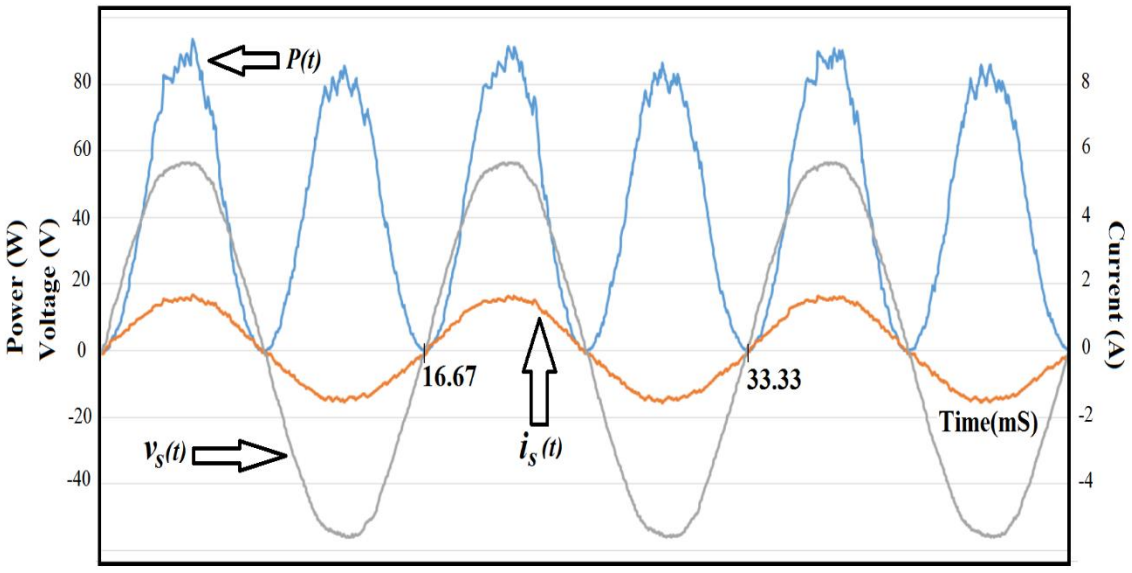


Fig. 5.18 Calculated power, *P*, with load and filter.

5.3 Challenges Implementing the Filter

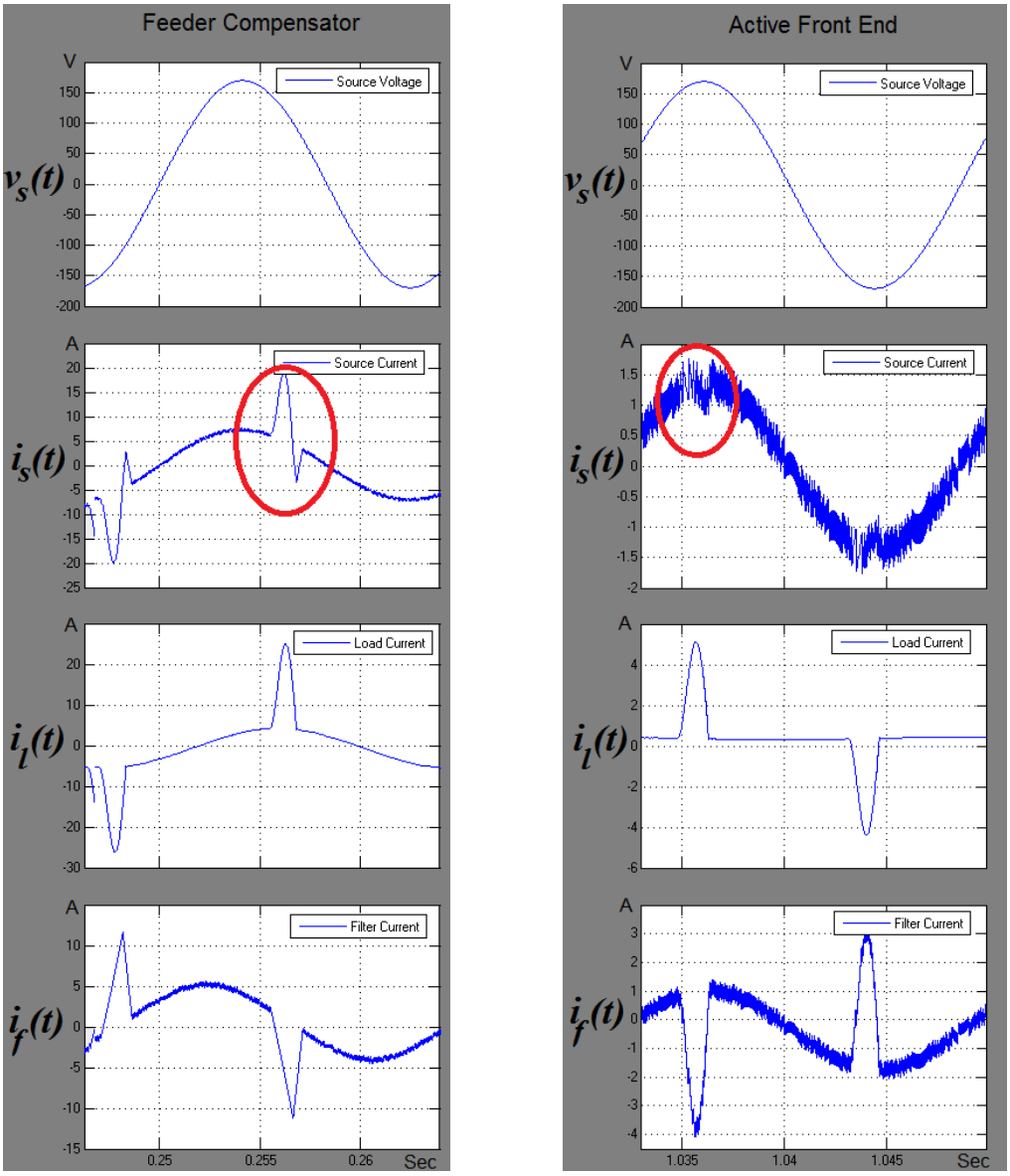
A careful choice of inductor needs to be considered when designing a filter to compensate a certain load current. But how about when that load changes? Since increasing load current (including harmonics amps) is inversely proportional to inductor size, if any load current demand changes, then this will greatly impact the performance of the filter.

If load is increased, then i_f would be high and cannot effectively compensate the THD in i_s because the filter would not be able to track sudden changes as fast as if it had a lower inductor value (L_f). An example is presented in Fig. 5.19 to compare two scenarios. It can be noted that for the same inductor value $L_f = 20\ mH$, the performance of the filter as an active front end is better than the filter as a feeder compensator. A concern that may arise is the high switching frequency of the compensated source current as in Fig. 5.19. Unfortunately, the ripple is due to hysteresis and can not be fully omitted but it can be reduced. Reducing the ripple on the filter current can be achieved by increasing the switching frequency. Recalling equation (3.18), since f_{sw} is inversely proportional to $\frac{di_f}{dt}$, then, if f_{sw} is increased, we obtain a small variation of the filter current and the controller has a better judgement of whether to increase or decrease i_f at a sampled time. Further, the ripple could be reduced by attaching a low pass passive filter.

Reducing the switching frequency will increase the ripple as in Fig. 5.20. The figure shows the time domain capture of the source, load and filter currents when the switching frequency was only 5 kHz. The performance of the filter was weaker as shown in Fig. 5.21 (THD = 9.93%) when compared to Figs 5.12 and 5.13.

That being said, if load is reduced, then the inductance, L_f, would be too small for the load. Decreasing a load and keeping L_f unchanged would result in a compensated source current that has higher switching losses. Yes, the switching frequency can be increased to decrease losses, but this would add more computational burden and would require higher switching

frequency rating for the switches (i.e. IGBTs or MOSFETs). Therefore, there is a need for a variable inductor implementation in the filter to overcome load variation.



(a) Filter as a feeder compensator. (b) Filter as an active front end.

Fig. 5.19 Comparison of filter performance when $L_f = 20\ mH$.

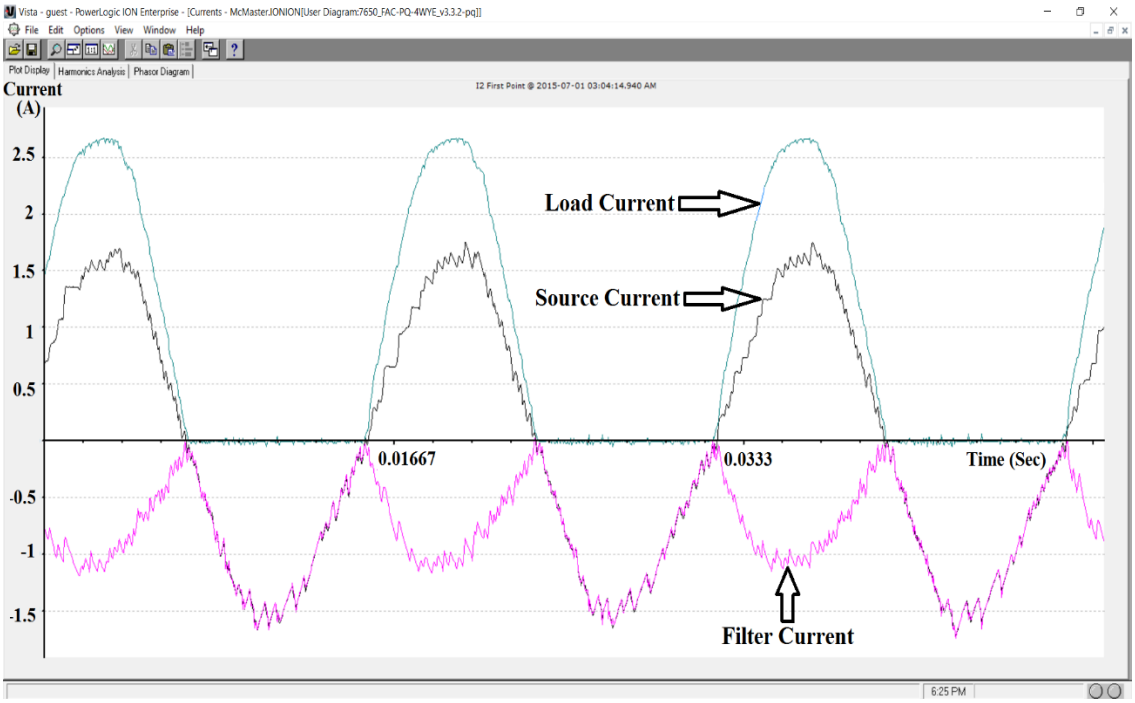


Fig. 5.20 Measured current waveforms for i_s , i_l and i_f after filtering of harmonics, f_{sw}= 5kHz.

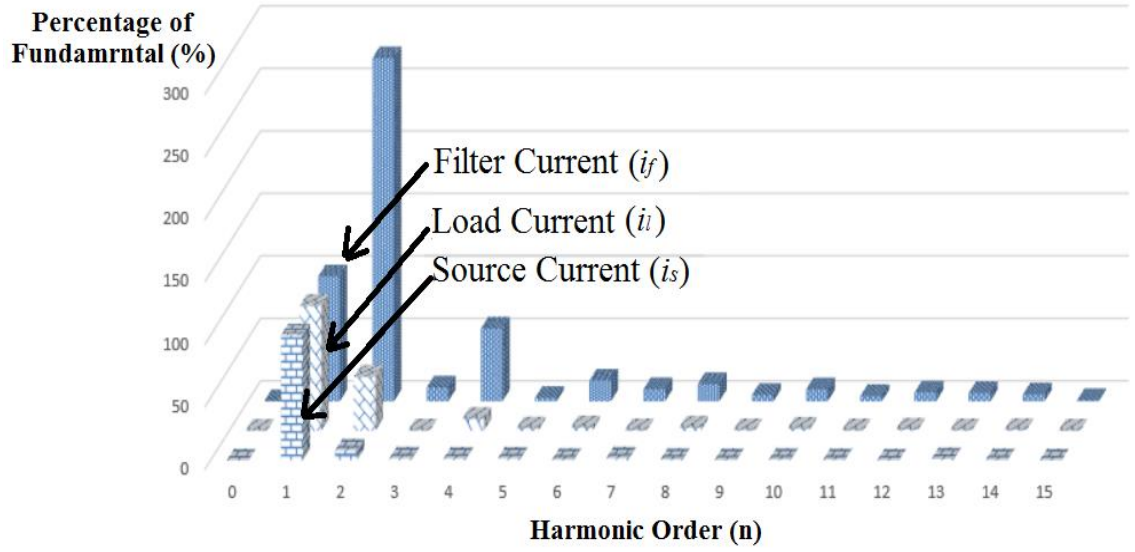


Fig. 5.21 Measured frequency spectrum of i_s, i_l and i_f after filtering of harmonics, f_{sw}= 5kHz.

5.4 Variable Inductor Discussion

From the challenges specified in the previous section, the choice of the inductor size can very well affect the filter performance. A fixed inductor would not allow a filter to operate with the same efficiency if load conditions changes.

One way to efficiently compensate a wide range of loads is to use a variable inductor instead of using a fixed inductor. The use of a variable inductor would improve the overall performance of the filter and the range of current harmonic compensation. A separate control algorithm needs to be utilized to accurately tune the inductor based on the load THD and load current requirement.

The solution of a variable inductor has to be implemented in such a way that the control algorithm looks at the load THD and the desired THD to optimally come up with an optimal value of the line inductor size. The separate control algorithm would be based off of equation 3.22. A separate MCU with low processing capability can be utilized to calculate the inductor size.

Fig. 5.22 shows the variable inductor in SAPF circuit. The inductor value can be changed using an actuator that moves based on a predetermined angle to select the right inductor value required. The actuator could be driven by a drive circuit triggered by the MCU outputs.

Alternatively, the variable inductor circuit could be designed as depicted in Fig. 5.23. A relay could be triggered to force a normally open (N.O.) contact to close any of the three switches shown. The algorithm in this case would calculate an approximate value of the inductor size based on the coil taps. Unfortunately, this circuit was not further studied due to time constraints.

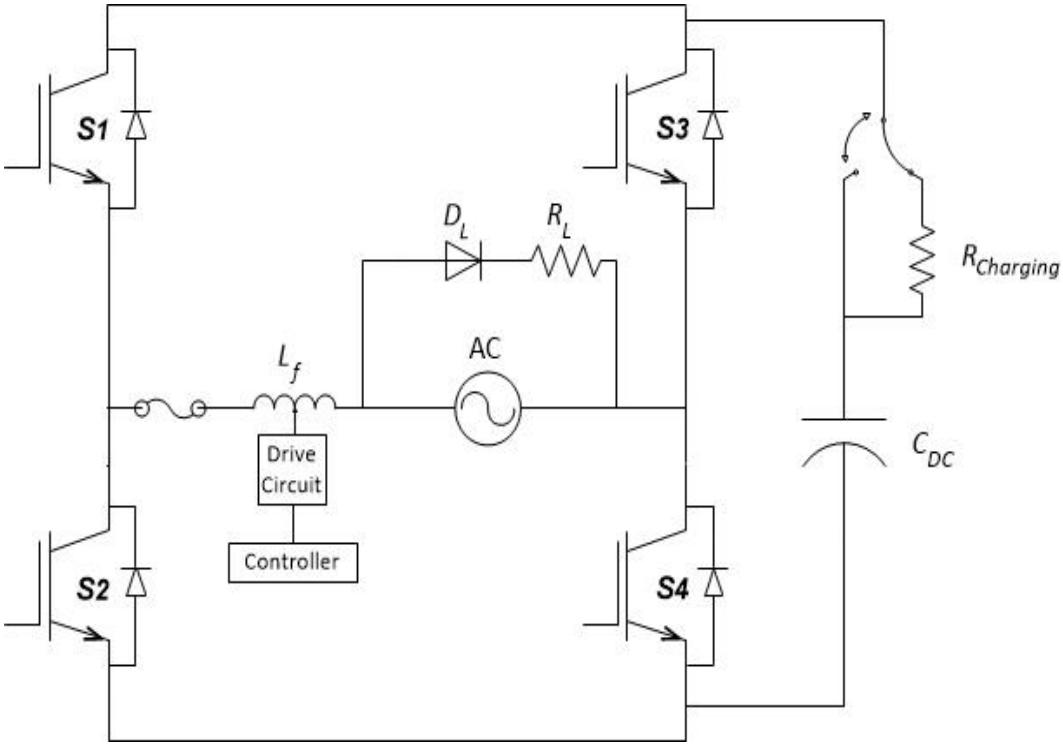


Fig. 5.22 Proposed SAPF with a variable inductor.

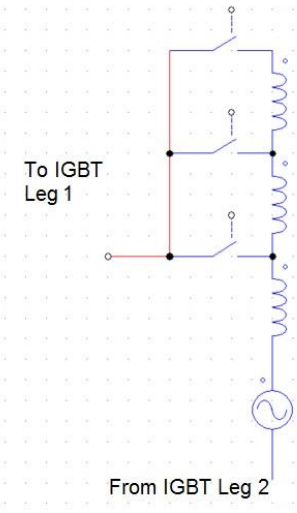


Fig. 5.23 Proposed design of variable inductor.

5.5 Summary

In this Chapter, a prototype for a SAPF was presented to compensate for a 21 ohms half wave rectified load. Although the filter prototype was not tested on a smart fridge, the filter was tested with a non-linear high THD load that draws about the same RMS current to that of the fridge. The hardware results showed consistency with the simulation conducted in this chapter (simulation result in Fig. 5.16); the THD of the line current were reduced significantly. The THD of the supply current went down from 44.2% to 5.4% as indicated in Table 5.2. Also, the results in Figs 5.14 and 5.15 clearly indicate that the source current and voltage are in phase, therefore, improving the source current THD by active filtering didn't introduce any phase shift.

As a rule of thumb, the following can be concluded from the results obtained. The higher the load current, the lower value of inductance need to be used, and vice versa. If an inductor is too large given a specific load current requirement, the filter cannot effectively compensate the THD in i_s. The reason for this shortcoming is the filter would not be able to track sudden changes as fast as if it were to have a lower inductor value (L_f). On the other hand, decreasing a load and keeping L_f unchanged would result in a compensated source current that has higher switching losses.

Several challenges have been encountered but overcame while designing and operating the filter, some are MCU based and some are equipment based. Further, it has been noticed that the filter performance reduces significantly if the load condition changes, hence, a variable inductor concept has been proposed, as discussed in 5.4. From my careful review and analysis of the literature, majority of papers focus on improving the reference extraction methods and enhancing control techniques. Hence, there is a need to investigate the variable inductor concept.

Chapter 6: Conclusions and Recommendations

6.1 Research Outcomes

A design of a SAPF has been proposed, and filter results from simulation have been validated experimentally. SPAF's are capable of significantly reducing the source current THD. Two scenarios were tested; first when the filter was used as an active front end, and second, when the filter was used as feeder compensator. Results have shown in both cases the reduction of the supply current THD (refer to Fig. 4.4 and Fig. 4.7). However, the compensation is minimal in the case of feeder compensation and the filter rendered a better performance when used as an active front end.

A prototype was built to filter the current harmonic content generated by a half wave rectifier load. Results of the hardware setup showed a close THD value to the one obtained in simulation.

The topic of APF is vast and versatile; there are many scholars who have presented state of the art work in this area. Most of the papers published in this field focuses on improving the efficiency of the filter, the method of extraction of reference current or the control algorithm of the filter. However, few papers focus on limitations of filter design. The research presented in this thesis including extensive experimental work has concluded that the use of APF, and SAPF in specific, is best suited for a predetermined load condition. Therefore, SAPF as an active front end renders a better performance than SAPF as a feeder compensator.

The design of the filter could be taken a step further to include variation of load conditions as this will be discussed in section 6.2.

6.2 Further Research

Further research needs to be conducted to improve the designs of SAPFs. Namely, to design a filter that is able to compensate for various combinations of non-linear loads. This type of SAPF utilizes a variable line inductor and a second MCU to be able to determine the required inductor size based on the load THD and current demand. It will be challenging to design a variable inductor with many taps/selections, since this will increase the cost of such a device and will impose computational complexity on the MCU.

6.3 List of Publications

Several parts of the work and ideas presented in this thesis have been published in [1].

[1] Al-Musawi, L.; Al-Mutawaly, N.; Schofield, N., "Shunt active power filtering for smart appliances," Electrical and Computer Engineering (CCECE), 2015 IEEE 28th Canadian Conference on, vol., no., pp.466-470, 3-6 May 2015.

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Appendix A: Source Code

As discussed in Chapter 5, Section 5.1.2, the code was implemented using Simulink. Simulink was chosen for reliability, time efficiency and convenience of programming. Since the MCU chip (STM32F417IG) had to be programmed using C code, the Waijung interface had to be used to allow for flawless code conversion from Simulink blocks to C code. Further, the code was downloaded to the chip through ST-LINK/V2 in-circuit debugger/programmer. Moreover, the ST-LINK/V2 features digital isolation between the PC and the target application board [50]. The original code written using Simulink for the hardware test conducted in Chapter 5 is detailed in Figs. A1 to A6.

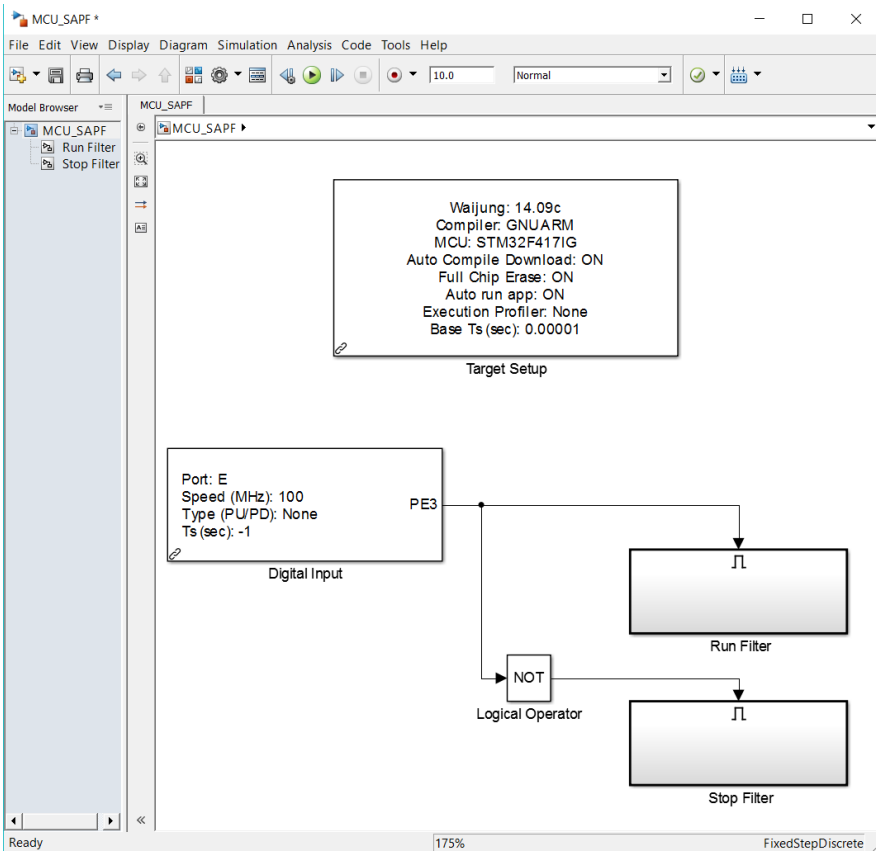

Fig. A.1 Main Simulink block showing target (MCU) setup, run filter and stop filter blocks.

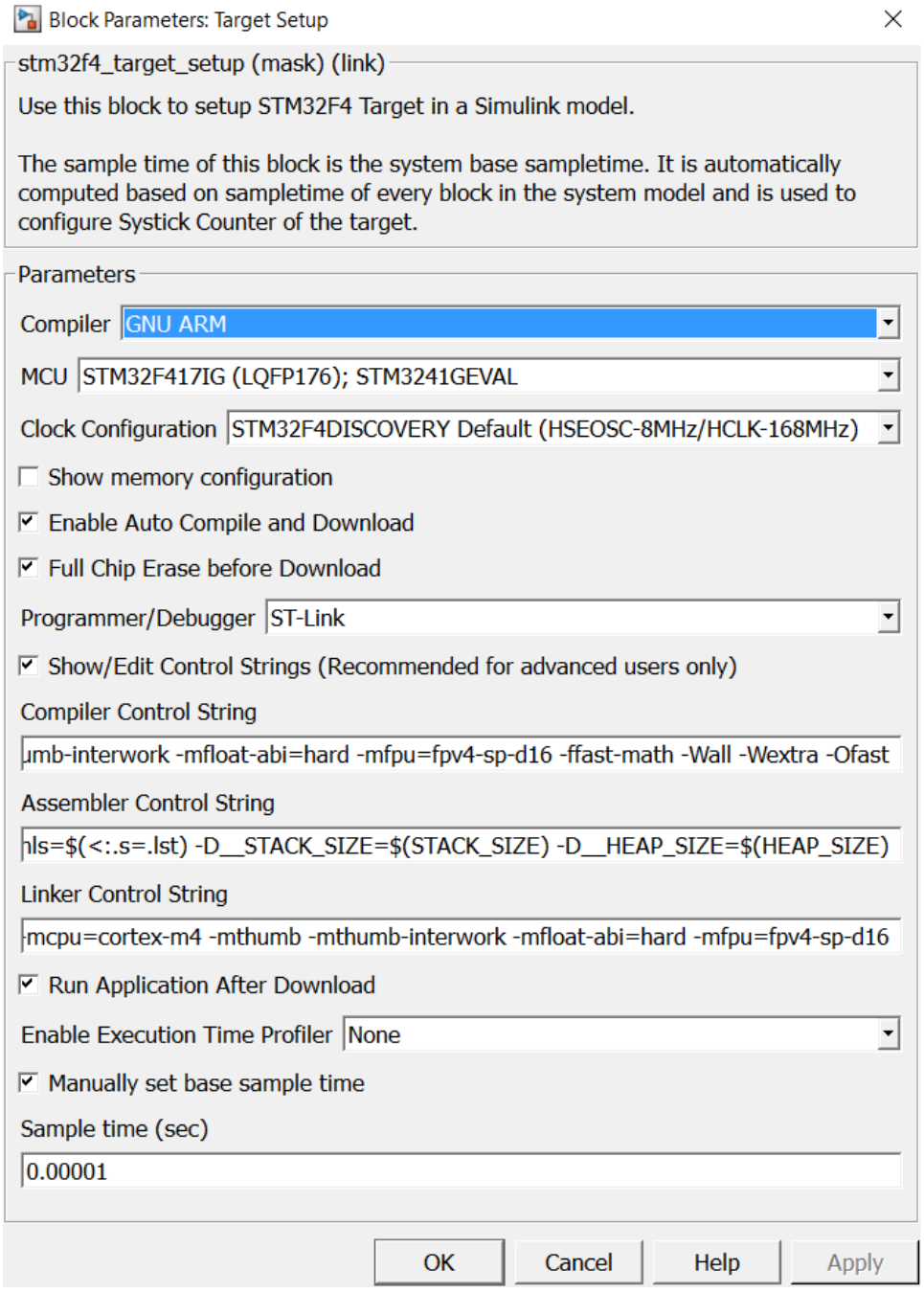

Fig. A.2 Target (MCU) settings.

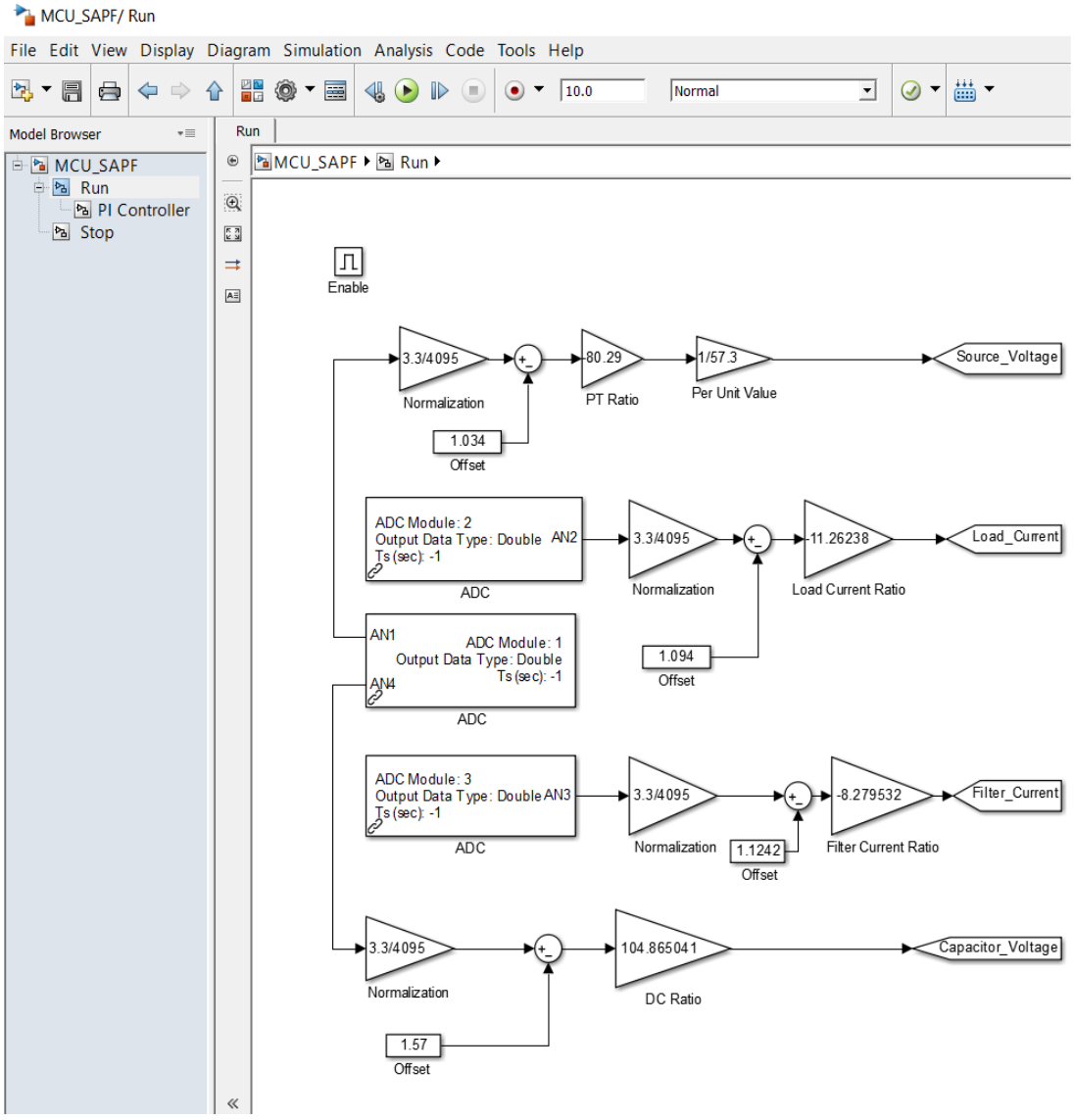

Fig. A.3 Data acquisition of various circuit parameters.

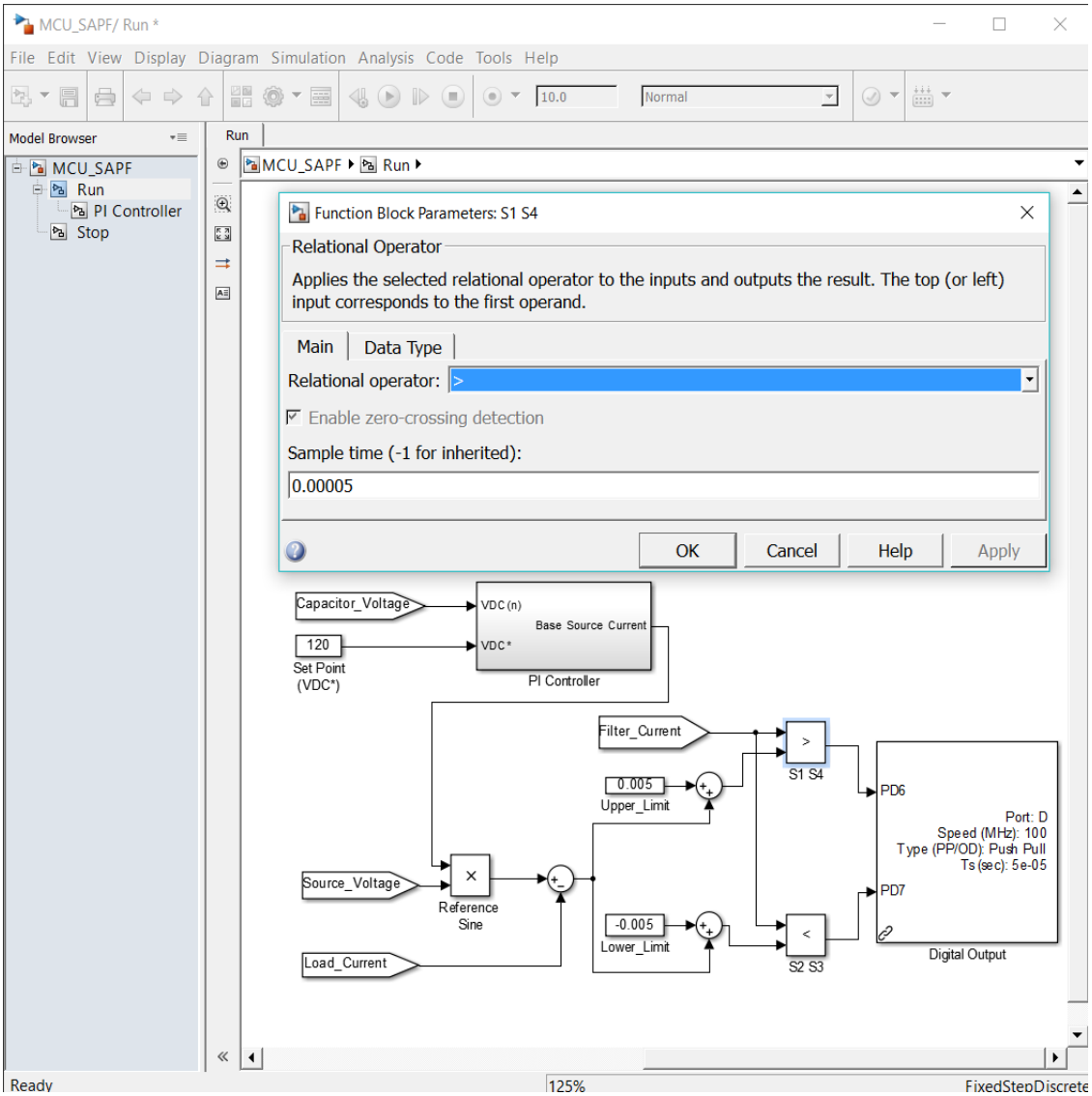

Fig. A.4 Filtering algorithm and switch control.

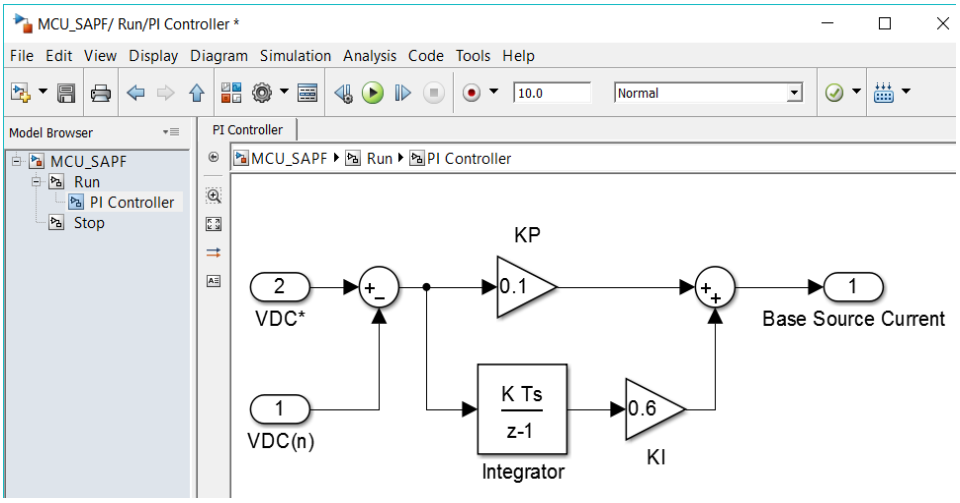

Fig. A.5 PI controller.

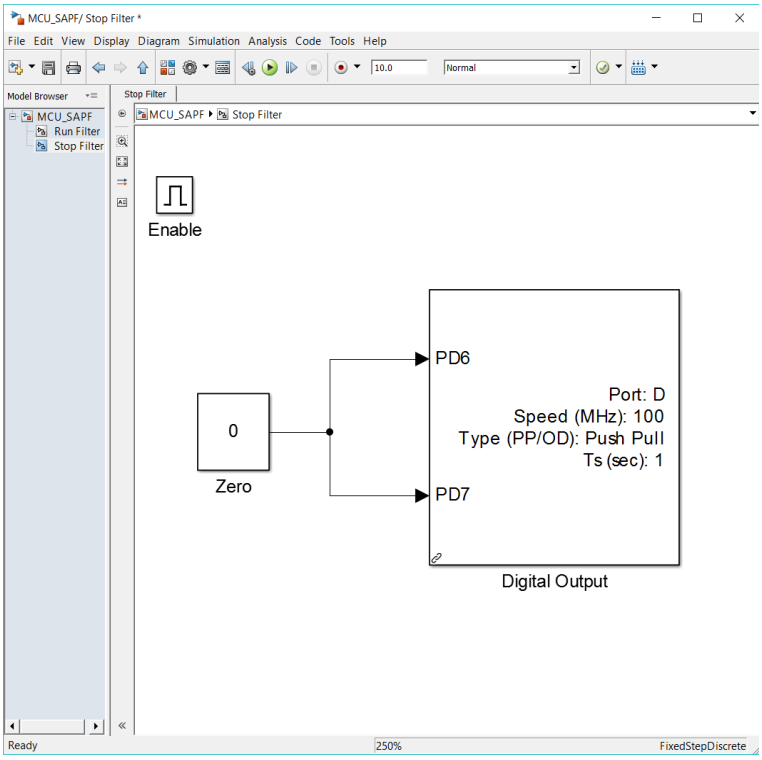

Fig. A.6 Emergency stop of filter operation.