ULTRA LOW FREQUENCY
DIGITAL ANALYZER

ULTRA LOW FREQUENCY DIGITAL ANALYZER: DESIGN AND CONSTRUCTION

By

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TITLE: Ultra Low Frequency Digital Analyzer: Design and Construction

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SCOPE AND CONTENTS: This thesis describes the development of an ultra low frequency digital analyzer from mathematical concepts and error characteristics set out in a publication[2] co-authored by the supervisor. The development is carried to the actual construction of a practical, economical, operating instrument, capable of giving information leading directly to the mean square value and the approximate amplitude probability distribution for ultra low frequency waveforms, both periodic and non-periodic. The final detailed design is described and justified, and the error characteristics derived in the above-mentioned publication are interpreted for the design. No further development of principles or error characteristics is undertaken.

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I. INTRODUCTION

An undergraduate laboratory experiment on the fundamentals of probability and statistics was devised some years ago, and the details were published in an engineering educational journal[1]. The experiment utilizes a simple, manual, voltage amplitude sampling device to collect quantized data on voltage waveforms. These data are used to calculate various statistical measures of the input waveform. This experiment suggested to its originator the possibility of an instrument which would automatically sample the input, and process the data by digital means. The theoretical development of this concept culminated in a publication describing the principles and error characteristics of a digital voltmeter[2].

The instrument described has several remarkable features.

A. It could operate successfully on both familiar and irregular waveforms, both periodic and non-periodic, or random.

B. A data processing equation is derived which leads to a mean square value without performing a squaring operation.

C. The number of quantization levels for the data is surprisingly low for practical error percentages.

D. The instrument has no low frequency limit.

E. The input under measurement does not deliver significant amounts of energy to the device, since the input is used only for amplitude comparison with reference levels.

The above features show the instrument to be unique, especially in its ability to operate on unfamiliar or non-periodic waveforms at ultra-low frequencies.

A model of the instrument was designed and constructed which operated on each data quantization level in turn, serially in time. Data gathering for a periodic wave required a period equal to $2n$ cycles, where n is the number of data quantization levels used.

This thesis describes the design, development and construction of a version of the instrument which requires only one cycle of a periodic input to complete the collection of data. It will operate on familiar periodic waveforms (i.e. sine, triangular and rectangular waves) at frequencies below 5Hz with error from any one source not exceeding 1.0%. Errors are kept as low as is consistent with implementation of a reasonably small number of data quantization levels using relatively inexpensive, practical equipment. The design utilized

readily available components and is economically and commercially feasible.

The design is based upon the principles and error characteristics derived in the publication[2] mentioned previously, this paper being the principle design tool. No further development of error characteristics is undertaken, the scope being the production of a practical, correctly functioning instrument with economy of components, and relating the error characteristics developed in the reference[2] to the device realized. Design and developmental work performed which was not closely related to the design finally adopted is not included here.

The order of presentation is as follows:

A. Basic concepts of design

B. Rectification

C. Level determination

D. Counter input logic

E. Control logic

F. Summary

One section is devoted to each of the above topics.

II BASIC CONCEPTS OF DESIGN

The apparatus constructed was originally conceived from an experiment in probability whose details have been published[1]. In the experiment, random samples were taken from a voltage waveform, and the samples were classified into intervals. Statistical measures of the waveform could then be calculated on the basis of the number of samples occurring in each interval. The experiment led naturally to consideration of a system which could give a measure of mean square or root mean square value for any input waveform. This section traces the development of such a system from its theoretical background to the more general aspects of a functioning instrument.

The concepts of both theory and design which give the system its form are discussed in the following order:

A. The mathematical expression on which the logical design of a practical system is based is developed, and the error characteristics are given.

B. The essential requirements with regard to information output are considered.

C. A means of achieving the required summation expression by use of weighted inputs to a register is explained.

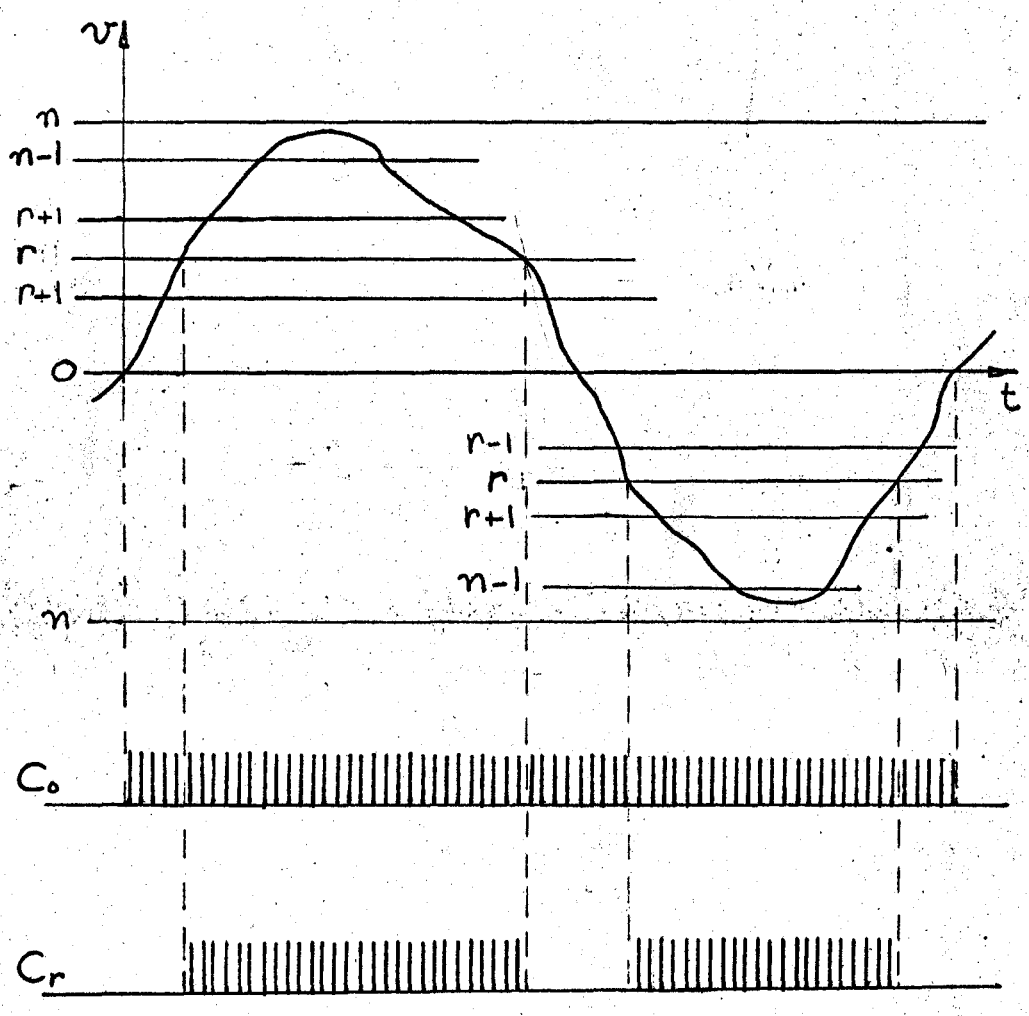
D. Binary addition by use of multiple trigger inputs is proposed as an economical method for increasing the contents of a counter register by a desired amount.

E. A simple system block diagram is shown and explained.

F. Some notes on the components used are included.

MATHEMATICAL FOUNDATIONS

Consider a collection of data from a waveform in the form of quantized samples. That is to say, each one of a large number of samples has been classified into a voltage interval. The reference[2] demonstrates a manner in which these data will give the mean square, or root mean square, value of the waveform. If the waveform is divided in n quantization levels, as shown in Figure 1, "Quantized Sampling", page 6, the number of samples collected in the two rth levels either side of the zero level may be termed C_r'. If V_{mr} is the mid-interval voltage for the rth interval, then the mean



C_r IS FORMED BY GATING CLOCK PULSES WHEN $|v|$ EXCEEDS LEVEL r

FIGURE 1 - QUANTIZED SAMPLING

square voltage, V_n^2, normalized to the voltage of level n, is

$$V_n^2 = \frac{1}{C_o} \sum_{r=1} C_r' \, V_{mr}^2$$

Here, C_o is the total number of samples taken -- it may be called the "base count". If the number of samples is very large,

$$V_n^2 \longrightarrow \sum_{r=1}^{n} p_r' \, V_{mr}^2 \qquad \text{----------(1)}$$

where p_r' is the probability that the voltage lies in the rth interval.

Consider, now, a system of above-level sampling, where the state of the voltage being above level r for the positive portion of the waveform, or below the negative rth level for the negative portion, causes the gating of clock pulses, at p pulses/second, to a counting register. This register then contains count C_r, as shown in Figure 1, page 6. Then, if another register counts C_o, the number of clock pulses occurring during the entire cycle of the waveform, the ratio of the two register contents approaches p_r where p_r is the probability that the voltage is above the rth level. Thus

$$p_r \doteq \frac{C_r}{C_o}$$

It is clear that

$$p_r' = p_r - p_{r+1}$$

and

$$C_r' = C_r - C_{r+1}$$

The normalized mid-interval voltages are as follows:

$$m_o = 1/2n$$

$$m_1 = 3/2n$$

$$m_r = (2r+1)/2n$$

$$m_{n-1} = (2n-1)/2n$$

Equation (1) now becomes

$$V_n^2 = (p_o - p_1)\left(\frac{1}{2n}\right)^2 + (p_1 - p_2)\left(\frac{3}{2n}\right)^2 + \text{---}$$

$$\text{--} + (p_r - p_{r+1})\left(\frac{2r+1}{2n}\right)^2 + \text{---}$$

$$\text{---} + (p_{n-1} - p_n)\left(\frac{2n-1}{2n}\right)^2$$

Note that the nth levels are never crossed, and that $p_o=1$, that is to say, the absolute voltage always exceeds zero. Because the mid-interval voltages are squared, voltage polarity contributes no information and absolute values may be used.

Now, collecting terms in p,

$$V_n^2 = \frac{1}{4n^2}\left\{1 + p_1\,(3^2 - 1^2) + \text{----}\right.$$

$$\left.\text{--} + p_r\,[(2r+1)^2 - 2(r-1)^2] + \text{--}\right.$$

$$-- \; p_{n-1}\left[(2n-1)^2 - (2n-3)^2\right]\Big\}$$

$$\therefore \; V_n^2 = \frac{1}{4n^2}\left(1 + 8\sum_{r=1}^{n-1} rp_r\right)$$

$$\therefore \; V_n^2 = \frac{1}{4n^2}\left(1 + \frac{8}{C_o}\sum_{r=1}^{n-1} rC_r\right) \text{--------(2)}$$

The instrument constructed is primarily a digital realization of the processes implied in equation *(2)*. This equation is the basis of an extensive error analysis which has been performed by F. Deist and R. Kital[2].

The sources of error are defined below.

The error due to some one cause is, say, e^1, so that if the instrument gives V^1 instead of V,

$$e^1 = \frac{V^1 - V}{V}$$

If e^1 is small, it can be shown that

$$e^1 \doteq \frac{1}{2}\left\{\left(\frac{V^1}{V}\right)^2 - 1\right\}$$

This expression is used extensively to determine the following errors.

e_n, error due to the use of n quantization levels either side of the zero level.

e_g, error due to the displacement of all levels from their true value by a constant normalized level error, ΔE.

e_{α}, error due to sampling a non-integral number of cycles of a periodic wave. This error does not occur in the instrument designed here, as precisely one cycle of a periodic wave is sampled.

e_p, error due to the use of a clock pulse of finite rate and duration in systematic sampling.

e_s, error due to finite switching times in gating the clock pulse. This error does not occur in the design described here.

e_N, error due to finite sample size for random sampling. This error is not considered because systematic sampling is used, since it allows the use of smaller sample groups.

e_T, error due to finite sampling time for white noise.

e_W, error due to sampling pulse duration in random sampling. This error is not considered (see e_N).

The expressions for the pertinent errors are given in Table I, page 11. The symbols are defined on page 12. These results are taken from Table 2 of the reference[2]. The normal wave is a periodic waveform having a normal amplitude probability distribution.

TABLE I - ERROR CHARACTERISTICS - GENERAL

Error	Rectangular Wave	Sine Wave	Triangular Wave	Normal Wave	White Noise
e_n	$\pm \frac{1}{2(n-1)}$ maximum	$-\frac{0.41}{(n-1)^{1.5}}$ maximum	$\frac{1}{4n^2}$ maximum	taken from Figure 6 of the reference[2]	
e_k	——	$< \frac{4}{\pi} \Delta E$	$\frac{3}{2} \Delta E$	$< \left[\frac{2}{\pi} \frac{\Delta E}{V_n} \right]^{1/2}$	
$e_{p\ max}$	$(1+\mu) \frac{f}{p}$	$2(1+\mu) \frac{f}{p}$	$3(1+\mu) \frac{f}{p}$	$\frac{1}{V_n^2}(1+\mu) \frac{f}{p}$	——
$e_{p\ avg}$	$\mu \frac{f}{p}$	$2\mu \frac{f}{p}$	$3\mu \frac{f}{p}$	$\frac{1}{V_n^2} \mu \frac{f}{p}$	$\mu \frac{Z}{p}$
e_T	——			$\leqslant \pm \frac{1.29}{[(\Delta f)T]^{1/2}}$ for 99% confidence	

where

f = frequency of periodic waveform under measurement

Δf = bandwidth for filtered white noise

n = maximum number of levels available on each side of the zero level

p = sampling (clock-pulse) frequency

μ = mark/space ratio of clock pulses

V_n = *r.m.s.* voltage under measurement, normalized to the voltage at the nth level

ΔE = error voltage in level position, normalized to V_n

T = time of measurement for a white-noise voltage

Z = number of zero-crossings per second for white noise.

This completes the description of the mathematical foundations of the process and the instrument.

ESSENTIAL REQUIREMENTS OF THE INSTRUMENT

The instrument must be capable of providing information leading readily to V_n with an accuracy of 1%, approximately. It must be able to collect all necessary data in one cycle of a periodic input. Examination of equation *(2)*, page 9, shows that in its least specialized form, the instrument must provide two items of information to the user:

1) a measure of $\sum rC_r$

2) a measure of C_o

The remaining arithmetic is readily carried out by the user. Further, in certain control systems applications, a direct knowledge of $\sum rC_r$ is very valuable, since this quantity is an approximate measure of the time integral of the voltage squared. A common and powerful index of control system performance is

$$I = \int_0^T e^2 \, dt$$

Since the machine is, in effect, a statistical analyzer, and since counters and level discrimination apparatus must be provided, an output display of C_r and C_o, after setting r manually, should be readily realizable. Thus, by selecting each of the levels in turn, the amplitude probability distribution can be determined in terms of n levels either side of the zero level.

It follows that the instrument must have a minimum output display of $\sum rC_r$ and C_o in a mean square mode of operation, and C_r and C_o in a probability distribution mode.

WEIGHTED INPUT CONCEPT

Using the expressions in Table I, it can be shown that sixteen quantization levels either side of the zero level are practical for the design criteria considered here. Sixteen is a power of two, and all numbers from zero to fifteen are possible states for a

four binary register, expressed in binary code, without any redundancies. Figure 6 of the reference[2] shows that fifteen levels will give e_n errors of 1% or less for V_n in the range

$$\frac{1}{2.58} < V_n < \frac{1}{7}$$

Sixteen levels give maximum values of 0.0977% for a triangular wave, -0.707% for a sine wave, and $\pm$ 3.33% for a rectangular wave.

Consider, now, the term $\sum_{r=1}^{15} rC_r$. At first glance, this operation implies counting the number of clock pulses that occur while the wave is above each level, multiplying by the respective levels, and summing the results. One can consider, however, the contribution of any single sample to $\sum rC_r$. If, for a given clock period, the input waveform under measurement is between, say, the fifth and sixth levels, then this pulse contributes to C_1, C_2, C_3, C_4 and C_5 (as well as C_0). When this contribution to each of these levels is multiplied by the level number in each case, that sample's contribution to $\sum rC_r$ is $1+2+3+4+5 = 15$. In general, any given sampling pulse must contribute to $\sum rC_r$ the amount

$$\sum_{q=1}^{r} q$$

where r is the highest level that the input exceeds at

the sampling instant. This amount can be termed the "weighted input" for the rth level. Table II, page 15, shows the weighted inputs for a 16 level system.

From this it can be seen that $\sum rC_r$ can be realized by determining the highest level exceeded at the sampling instant, and adding the binary weighted input for that level to the $\sum rC_r$ register, or accumulator register. This process occurs at every sampling instant.

TABLE II - WEIGHTED INPUTS

Highest Level Exceeded		Weighted Input	
Decimal	Binary	Decimal	Binary
0	0000	0	0
1	0001	1	1
2	0010	3	11
3	0011	6	110
4	0100	10	1010
5	0101	15	1111
6	0110	21	10101
7	0111	28	11100
8	1000	36	100100
9	1001	45	101101
10	1010	55	110111
11	1011	66	1000010
12	1100	78	1001110
13	1101	91	1011011
14	1110	105	1101001
15	1111	120	1111000
16	never exceeded	—	—

MULTIPLE TRIGGER ADDITION

The previous sub-section establishes a need for a method of binary addition which will increase the contents of the accumulator register by the weighted input once each sampling period. A very simple process for realizing binary addition is given below.

If a number *A*, available in binary form, is to be added to the content, *B*, of a binary counter register, this can be accomplished by applying pulses to the trigger inputs of those register binaries whose weightings correspond to bits in *A* which have a value of one. The content of the register is then *A+B*. However, these inputs must not interfere with the normal binary counter function of the register. Furthermore, the pulses must be applied serially in time in order to avoid counter propogation difficulties.

For example, if it is wished to add *25* to the content of a register, a single pulse is delivered to the fifth binary, weighted 2^4 or *16*, another, later, pulse to the fourth or eight-weighted binary, and a third pulse to the first or unity-weighted binary. Thus the counter register content is increased by *16+8+1 = 25*, which is binary *11001*. Thus the presence of a "one" in any given weighting position of the binary number to be added indicates that the binary of the same weight in the register must be pulsed or complimented.

The most significant bit to be added is always operated on first, and the rest are taken in order, down to the least significant bit, which is added last. This is done to allow the effects of successive additions to propogate along the register without interfering with subsequent additions. Figure 2, "Multiple Trigger Addition", on page 18, illustrates the above example.

This means of performing addition is well suited to forming $\sum rC_r$ in the accumulator register by the weighted input method. Each state of a four binary register containing sample level information can be made to gate the appropriate serial timing pulses to the accumulator register to add the weighted input for each sample. The binary weighted input column in Table II, page 15, shows that the highest order accumulator register binary requiring a trigger addition input is the seventh. Using this method, only two registers are required for the generation of $\sum rC_r$. It is not necessary to generate the weighted input in a third, separate register, and the logic used for the actual addition process is minimal.

BASIC SYSTEM

On the basis of the foregoing sub-sections, it is possible to describe the basic system. Taking the fundamental sections in order, the requirements are:

IT IS DESIRED TO ADD 25_{10}, OR 11001_2, TO THE CONTENTS OF THE COUNTER REGISTER. THEREFORE DELIVER PULSES TO INPUTS t_1, t_2 & t_5 IN TURN, THUS ADDING $2^4+2^3+2^0=25_{10}$

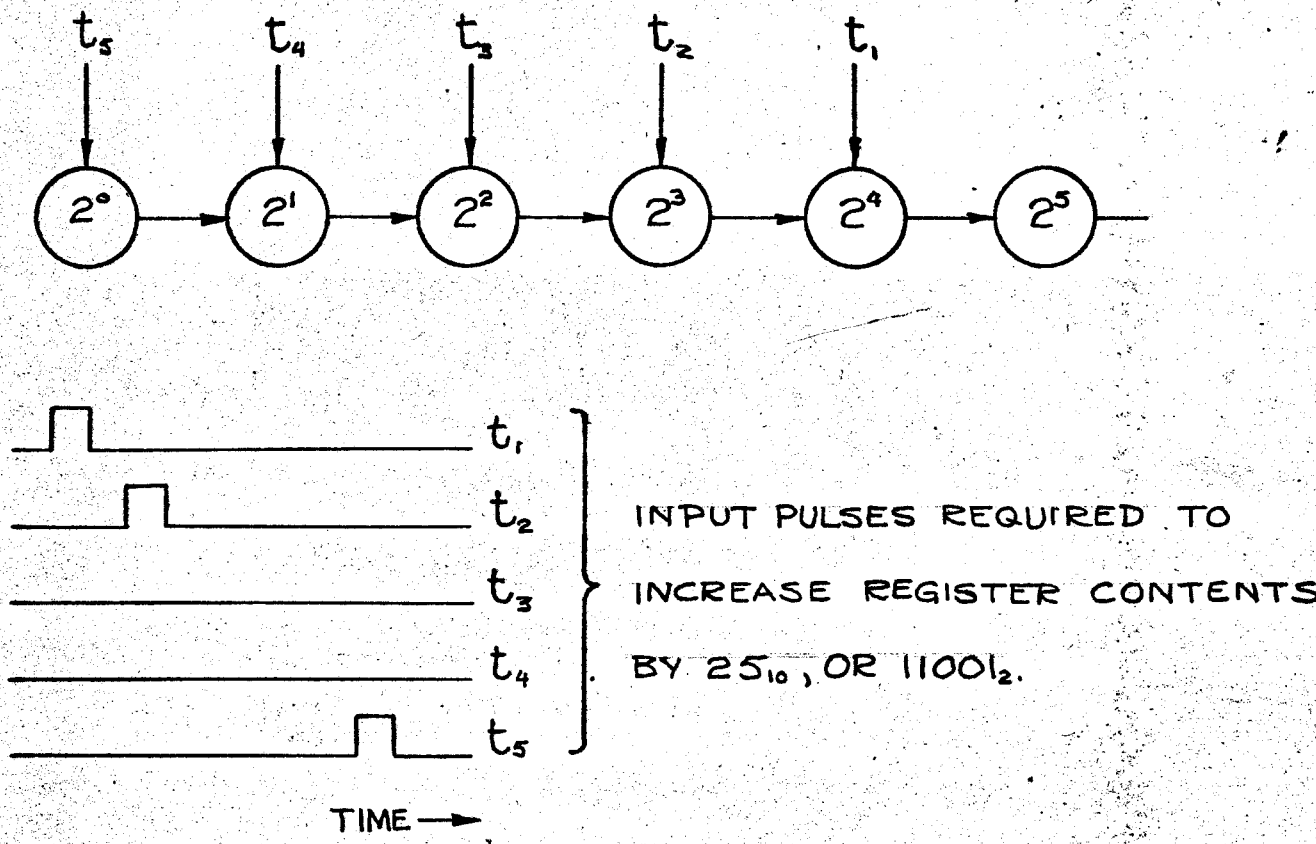
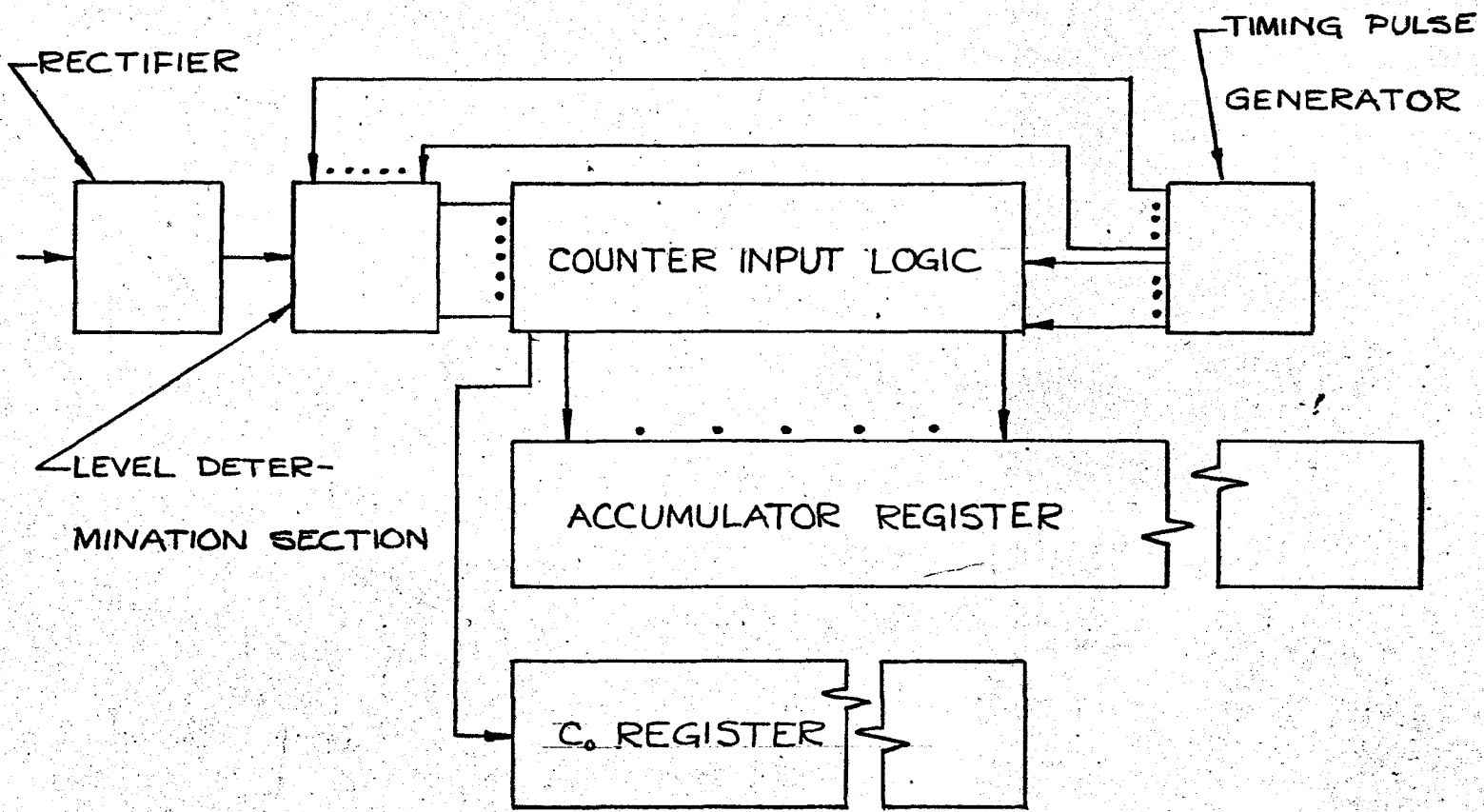


FIGURE 2- MULTIPLE TRIGGER ADDITION

DJB

1) a scaler which will multiply the input in analogue fashion by a factor which will allow utilization of most of the available levels without exceeding the sixteenth.
2) rectifier to allow use of the fact that input polarity is redundant information -- level determination can be carried out over 16 rather than 32 levels.
3) a device for determination of the level of each sample in the form of a four bit binary number.
4) digital logic which will deliver the appropriate pulses needed to add weighted inputs to the accumulator register by the multiple trigger input addition method, and one pulse each sampling period to a simple counter register holding the base count, C_o.
5) accumulator and base count registers.
6) a timing pulse generator to control the level determination and addition processes.

The basic system is shown in block diagram form in Figure 3, "Basic System Block Diagram", on page 20. No details of the control logic are included at this point.



N.B.- ..... INDICATES MULTIPLE INPUTS OR OUTPUTS

FIGURE 3 - BASIC SYSTEM BLOCK DIAGRAM

EQUIPMENT UTILIZED

At this stage in the design process, a decision was made to use purchased logic modules, instead of designing and building the instrument from components. This decision played a major part in forming this thesis. The design problem became one of system design, and the characteristics of the particular modules used came to be of considerable importance. As this is a design problem in essence, the behaviour of a particular module of a particular vendor becomes an integral part of it. Thus, in contravention of the usual practice, modules will be referred to by the manufacturer's model designation, followed by a brief description, as in "W501 Schmitt trigger", or "R111 nor/nand gate".

Most of the equipment used was supplied by Digital Equipment of Canada Limited (D.E.C.). Logic modules are of the R series which operate at frequencies up to 2MHz. D.E.C. modules are of the "card" type, using printed circuits and discrete components, and fitting into a rack of 64 eighteen-pin connectors. Logic levels are zero volts and -3 volts, with binaries triggering on a rising voltage. Power bus voltages are +10 volts ground and -15 volts.

The principal pieces of equipment not supplied by D.E.C. are two operational amplifiers by Data Device

Corporation, a Philips pulse generator, the accumulator and base count registers which were made at Witwatersrand University on Veroboard, and certain manual switches and power supplies.

III RECTIFICATION

The instrument gives information leading to the mean square value of the waveform under measurement, thus the polarity of the input at any instant is of no importance. Sixteen data quantization levels either side of the zero level are required, as shown in section II, so there are two approaches:

1) employ 32 level determination on a scaled waveform
2) employ 16 level determination on a rectified, scaled waveform.

This section will explain the selection and realization of a rectifier circuit. It is presented under the following sub-sections:

A. Reasons for the use of rectification
B. Selection of a rectification method
C. Speed requirements
D. Inversion
E. Rectifier control
F. Development of the rectifier.

REASONS FOR THE USE OF RECTIFICATION

The following sub-section shows why rectification was adopted.

The use of 32 quantization levels obviously requires twice as many "decision points" as a rectified-input, 16 level system, and a five bit level register is needed instead of a four bit register. Thus, as will be seen in the next section (on level determination), measurement to equal accuracy requires one-quarter as much time again for level determination for the 32 level case. The nature of the analogue-to-digital converter that performs level determination requires the use of straight binary code for level designation, with one extreme at zero volts and the other extreme one quantization level above -10 volts. Level widths are thus halved for the 32 level case, and the attainable accuracy for the quantization process is reduced by a factor of two.

The 32 level case also requires the zero level of the input to be offset to -5 volts in order to centre the waveform under measurement in the zero volt to -10 volt range. The obligatory use of straight binary code eliminates the possibility of using a special code to simplify the register input logic. If it is desired to obtain identical four bit expressions for the rth levels both above and below the zero level for a 32 level system, the requirements are not simple. Examine the expressions for the first three levels either side of the zero level.

DECIMAL NO.	BINARY NO.	LEVEL
19	10011	3
18	10010	2 } above zero
17	10001	1
16	10000	Zero Level (offset -5V)
15	01111	1
14	01110	2 } below zero
13	01101	3

To have a level below zero show the last four bits in the same state as the corresponding level above zero, it is necessary, on noting a zero state of the first, 16-weighted bit, to negate the last four bits and then increase the result by one, thus

$15 = 01111 \longrightarrow 0000 + 1 = 0001 = 1$

$14 = 01110 \longrightarrow 0001 + 1 = 0010 = 2$

$13 = 01101 \longrightarrow 0010 + 1 = 0011 = 3$

This process does not offer any simple means of reducing the register input logic for the un-rectified case.

It is evident from the conditions stated above that rectification is desirable.

SELECTION OF A RECTIFICATION METHOD

In practice, conventional rectification methods intended to transform some voltage V to -V volts actually give $-V+v_e$, where v_e is an error voltage. In the application at hand, v_e creates an error equivalent to that resulting from displaced level voltages. Conventional diode rectification gives an error v_e of

considerable size as a result of the barrier voltage effect alone. This fact, compounded by the fairly large, current-dependent forward resistance of semiconductor diodes, indicates that conventional rectifiers are not readily applicable.

Standard methods being inadequate, some advantage might be taken of the extremely low input frequencies involved. Rectification can be considered as the selection of either the unaltered instantaneous value of the input, or its analogue inversion, depending upon input polarity. In order to keep v_e small, rectification must be about zero volts precisely. However, since no input is supplied to the accumulator register for absolute input voltages smaller than the first quantization level, rectification need not be performed precisely at zero volts. Thus rectification may be accomplished by using a SPDT switch to select either the unaltered or the inverted input, according to polarity. The prime virtue of this method is that inversion may readily be carried out with good accuracy by the use of an operational amplifier.

The effect of a displacement of the inverted portion of the wave due to a d.c. voltage drift at the inverter output of amount Δe is equivalent to error e_l where only half of the levels are affected. Error e_l as defined previously results from a normalized constant-

level error ΔE at <u>all</u> levels. Thus, because the error is cumulative through the levels, the expression given for e_l in the reference[2] can be halved for consideration of the rectifier offset on one-half of the waveform.

Therefore, for this case,

$e_l < \frac{2}{\pi} \frac{\Delta e}{10}$ for a sine wave

$e_l < \frac{3}{4} \frac{\Delta e}{10}$ for a triangular wave

$e_l < \frac{1}{2}\left[\frac{2}{\pi} \frac{e}{10V}\right]^{1/2}$ for a normal wave and white noise

SPEED REQUIREMENTS

The operation of the SPDT switch performing the selection function will clearly have restrictions on its switching time. Switching must occur below the first level, in the region where no accumulator register inputs occur, if error from this source is to be avoided. For the system in question, there are 16 levels in 10 volts, thus the "safe zone" is zero to 0.625 volts. For a 5Hz sine wave filling the 16 levels exactly, the time required to rise from zero volts to the first level is 1.99 msec. -- switching must be performed in this period. The speed requirement could readily be met by an electronic switch, but this was rejected as too costly and unnecessarily fast and sophisticated for the application. The requirements can also be met by reed relays at much lower cost. The mercury-wetted type of

reed relay can meet the requirements with absence of contact bounce, although it is not generally as fast as a dry reed relay.

For waveforms which pass through the region of the zero level more rapidly than a sine wave, some error in accumulator register content will arise. This error will usually involve the lower quantization levels, which have small weighted inputs, thus keeping the error small. The worst case is a rectangular wave where the error in $\sum rC_r$ due to a rectifier switching time of T_R seconds is

$$e_{T_R} = \frac{T_R}{1/f}$$

where f is the rectangular wave frequency. For a 5Hz rectangular wave, and T_R equal to 2 msec., the error is 1.0%.

INVERSION

Inversion can be accurately accomplished by an operational amplifier set for unity gain. If an accuracy in gain of 1.0 mv in 10 volts is desired, a minimum forward loop gain of 80 dB is required.

Low output voltage drift is required of the amplifier, since such drift appears as a level displacement. Frequency response is not a problem at the frequencies involved.

Carefully regulated supply voltages are not available from elsewhere in the system, so a separate power supply is required for the inverter. The unit selected was a Data Device Corporation (D.D.C.) module C-1818. This is a card-mounted module containing two high-stability, low drift, solid state, differential operational amplifiers of 85 dB gain, complete with power supplies. Specifications are given in the Appendix, pages 85 to 86. The unit is compact, physically rugged and completely short-circuit protected. Cost is reasonable. Two amplifiers were installed to allow later construction of a scaler, although the scaler was not included in this project.

Inversion was realized with one of the above-mentioned amplifiers, using 1.0 megohm feedback and input resistors.

RECTIFIER CONTROL

The reed relay must be made to change state with changes in the polarity of the input voltage. It can, therefore, be controlled by a comparator with a reference voltage of zero.

The principal vendor, D.E.C., offers two models of comparator. The A502 comparator is a sensitive unit of 1.0 mvolt resolution and a maximum of 5.0 mvolt common mode error throughout its range. It can accommodate

inputs from zero to -10 volts. The W520 comparator is much less sensitive, consisting simply of a four-transistor differential amplifier. In one of the two stable states which it exhibits, the W520 comparator input circuit, when floating, is effectively a +10 volt source in series with 10 kilohms. This is an inconvenient feature, as will be shown later. The unit can, however, operate on input voltages of 10 volts swing of either polarity.

An effort was made to use the more sensitive comparator, A502, at the output of the relay. Here it would be subject only to negative voltages, the waveform being negatively rectified at that point: thus it would operate by changing the state of the relay whenever the rectifier output started to cross the zero level. This configuration was abandoned because, in such a system, the comparator has no knowledge of input polarity, and merely notes zero-crossings. Thus it could get "out of step", and perform positive rectification. The comparator must be connected at the input of the rectifier, therefore the W520 comparator must be used, in spite of its shortcomings.

A further requirement of the rectifier section is the ability to deliver only the positive or only the negative portion of the waveform under measurement, at the operator's choice. This will allow determination of

the amplitude probability distribution of either portion of the input, independently. A block diagram of the rectifier, with this feature incorporated, is shown in Figure 4, "Rectifier - Simple Block Diagram", on page 32.

DEVELOPMENT OF THE RECTIFIER

The following subsection describes the evolution of the final circuit configuration for the rectifier.

As explained previously, when the comparator is placed in the location shown in Figure 4, page 32, the use of the W520 comparator/differential amplifier is obligatory. In order to obtain a true two state output, a W501 Schmitt trigger is placed at the output of the W520 comparator. The W501 Schmitt trigger has internal voltage dividers to give state changes at input levels of -0.8 volts and -2.2 volts. Its output rise times are compatible with the R-series logic modules.

The rectifier circuit as it was first constructed used a W800 relay module. This consists of two SPST dry reed relays, complete with drivers. Both relays were used, one being driven directly from the output of the W501 Schmitt trigger and the other from the logical inversion of that output. Figure 5, "Rectifier Circuit - Not Useable", page 33, shows the circuit.

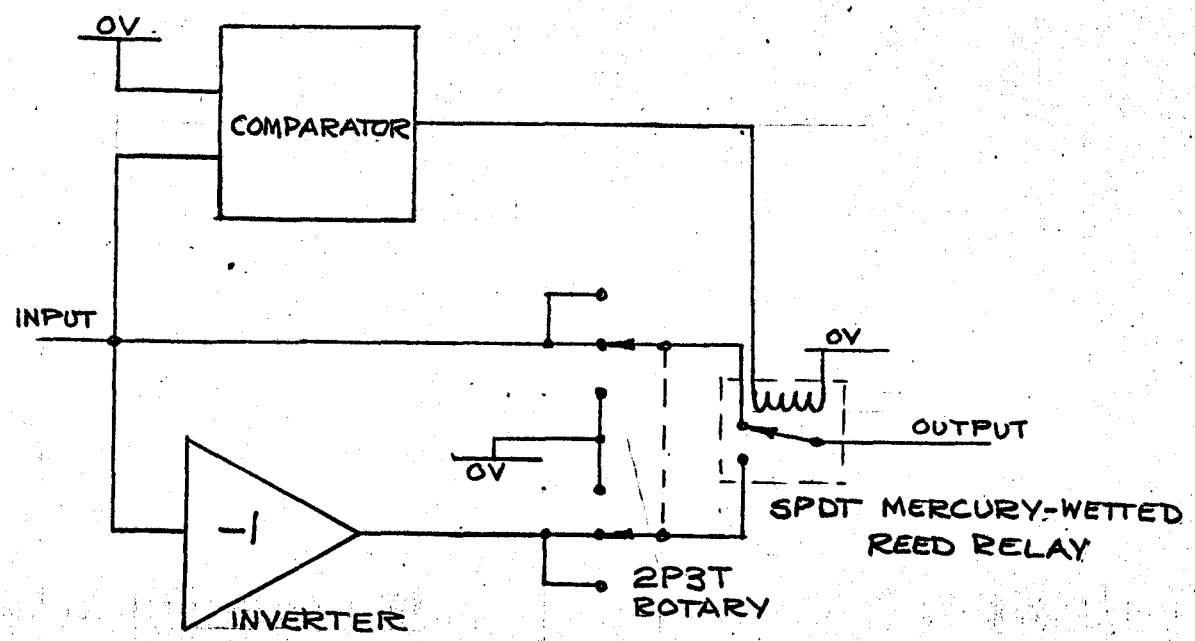


FIGURE 4-RECTIFIER-SIMPLE BLOCK DIAGRAM

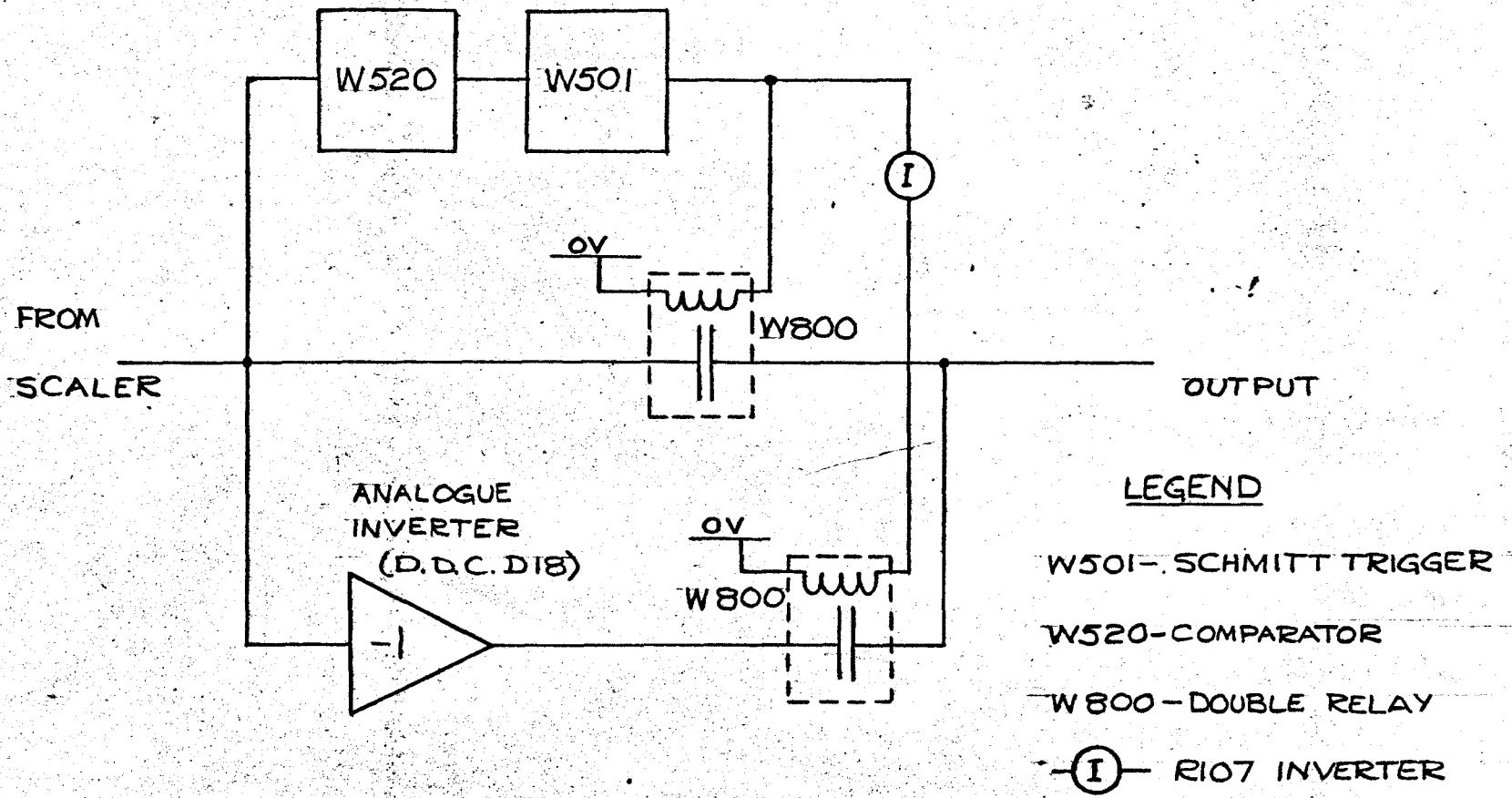


FIGURE 5 - RECTIFIER CIRCUIT - NOT USEABLE

This circuit was rejected because there is no simple way of making the relay pair operate in a break-before-make fashion. When a change of state occurs, field collapse in the initially closed relay takes longer to occur than the closing of the initially open relay. Thus, for a fraction of a millisecond, both sets of contacts are closed, and both the unaltered and the inverted versions of the input voltage are connected to the output simultaneously. This leads to large transient output fluctuations. This problem was overcome by using a break-before-make, SPDT, mercury-wetted reed relay, model HGSM5009, manufactured by C.P. Clare of Canada Ltd. (see Appendix, page 87, for full specifications). The mercury-wetted relay exhibits no contact bounce. It is driven from a W050 30 ma driver connected at the Schmitt trigger output.

Rectifier operation was observed with the input derived from the second operational amplifier, since this will become part of the scaler in a completed instrument. A short burst of high frequency oscillation appeared at the output at the point where the W520 comparator changes state. This was found to result from inductive pick-up from the W050 driver output, which exhibited damped oscillation of considerable magnitude when a change of state occurred. Induced fluctuations resulting from this appeared at the rectifier input and

caused spurious state changes in the comparator and Schmitt trigger. Two measures were introduced to alleviate this problem:

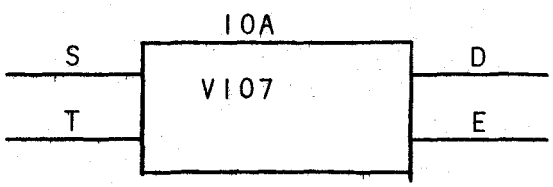
1) the W050 driver output was shunted to ground with a 1.0 mfd capacitor to remove much of the oscillation at its source.
2) a simple RC filter was placed at the output of the W520 comparator. This low-pass filter has a time constant of 0.16 msec, and slows the action of the rectifier slightly, but it serves to prevent short-duration state changes of the comparator from altering the state of the Schmitt trigger, thus eliminating the effect of narrow spikes at the comparator input. The time constant was chosen experimentally.

Another transient disturbance occurs at the closing of the relay contacts. It is of very short duration. Its amplitude is negligible for small output loads, but increases with increasing load. This transient is probably due to induced noise from relay switching under load. The present load of two A502 comparators each drawing a maximum of 1.0 μa, makes the transient very small indeed.

A desired feature of the instrument is a warning light display which notifies the user when the sixteenth level has been crossed. This is accomplished by examining the rectifier output with a comparator having a -10 volt reference input. If the sixteenth level is exceeded, the comparator changes state, setting a binary whose state is displayed by an indicator light. The binary remains in the set condition until manually reset. It would be preferable to use an inexpensive W520 comparator for this purpose, since high accuracy is not essential. However, the previously mentioned input characteristic of the W520 comparator, where the floating input circuit is effectively a +10 volt source in series with 10 kilohms, defeats such an application. During the brief "open" period of the relay state change (between breaking one contact and making the other), the rectifier output exhibits a +10 volt spike. This excursion can be reduced by loading the rectifier, but at the sacrifice discussed in the previous paragraph. To avoid these problems, an A502 comparator is used for this function, as its input circuit does not exhibit this undesirable characteristic.

The W520 comparator changes state at about +0.15 or +0.20 volts above the reference input. In order to straddle the zero level nearly symmetrically, a voltage divider is used to provide a reference input of -0.17 volts.

The final circuit for the rectifier and sixteenth level crossing detection is shown in Figure 6, "Rectifier", on page 38. In this figure and elsewhere the locations of connecting pins are shown in the circuit diagrams in the manner designated below.



A) V107 inside the module block symbol gives its model number. The manufacturer is D.E.C. unless otherwise noted.

B) 10A adjacent to the symbol gives its location in the rack. A designates the top row and B the bottom, with locations numbering left to right. Thus A10 is the tenth location from the left in the upper row.

C) D, E, S, T beside the connecting lines are the identifying letters of the connecting pins.

Note that many modules contain more than one unit. All units on the same module card are similar.

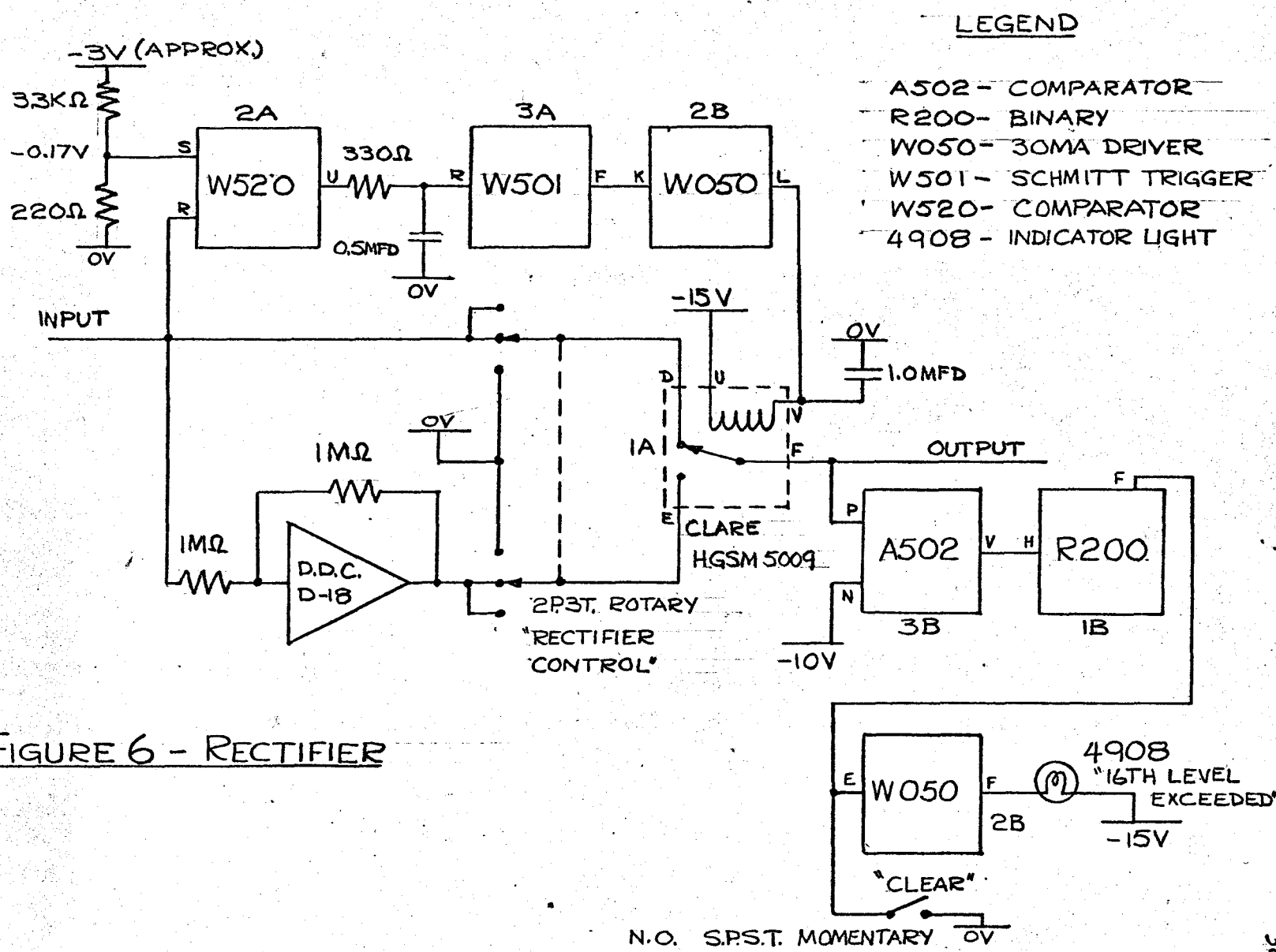


FIGURE 6 - RECTIFIER

IV LEVEL DETERMINATION

After rectification has been performed, the input waveform under measurement is subject to a determination of the highest level exceeded at each sampling instant. If the number of this level is to be made available as the contents of a four binary register, it can readily be appreciated that level determination is actually analogue-to-digital conversion.

The principal supplier, D.E.C., has developed several methods of analogue-to-digital conversion which are readily realizable using D.E.C. modules, and these are described in the D.E.C. "Digital Logic Handbook". In all cases, these methods involve formation of quantized analogue voltages corresponding to the digital states, and comparison of these with the incoming analogue signal. The principal variations of this technique will be discussed in the following order:

1. Simultaneous conversion
2. Counter conversion
3. Continuous conversion
4. Successive approximation conversion

These techniques will be evaluated, a selection made, and the detailed design and its error characteristics described.

SIMULTANEOUS CONVERSION

For simultaneous conversion, each quantization level is formed in a voltage divider network, and each is applied as a reference input to a separate comparator. The second input to all comparators is the analogue input. Binary logic can then be applied to the comparator outputs to determine the number of the highest level exceeded. The form of the output is well suited to use in conjunction with a diode matrix for the formation of the weighted input.

This method is conceptually simple and very fast, with state change times involving only comparator and logic switching speeds. However, as the number of levels increases, it soon comes to require so many comparators that cost, and the number of critical adjustments required become probibitive.

COUNTER CONVERSION

Counter conversion uses a binary counter register, driven by a clock pulse generator, that counts upwards from zero during each conversion. The state of this counter is continuously converted to an analogue

voltage by a digital-to-analogue converter. The output of the converter is compared with the analogue input, and when it exceeds the input, the comparator halts the count at that point. This procedure gives the lowest unattained level as an output, instead of the desired highest attained level, and makes the exceeding of the fifteenth level undetectable with a four binary counter register. These disadvantages can be overcome by starting at the fifteenth level and counting down. A disadvantage that cannot be overcome is the time required for accurate conversion. Time must be allowed for fifteen possible state changes and comparisons, and settling times must be provided for the digital-to-analogue converter and the comparator if accuracy is to be maintained.

CONTINUOUS CONVERSION

The continuous converter holds the digital equivalent of the analogue input in an up-down counter register. A digital-to-analogue converter converts the state of this register, and the result is compared with the input. When the comparator detects a difference exceeding certain limits, it gates a clock pulse to drive the register in the correct direction to reduce the difference. For slowly varying waveforms, the

converter follows the analogue input closely and continuously. Any deviation is corrected at the next available clock pulse.

Usually, the converted quantization levels are set at the mid-interval values, and the comparator hysteresis is set for state changes one interval apart, centred about the reference input. In the application in question, the levels are widely separated (each interval being 0.625 volts wide), and both mid-interval reference levels and a 0.625 volt comparator hysteresis cannot be readily realized with D.E.C. equipment.

SUCCESSIVE APPROXIMATION CONVERSION

Conversion by successvie approximation is realized by a series of decisions on approximations that converge rapidly on the correct digital state. For the 16 level case, the first approximation is the eighth level (i.e. state 1000). The analogue conversion of this state is compared with the input, and if it exceeds the input, the eight-weighted bit is reset to zero. If the approximation is too small, the bit remains a "one". The register now contains either 1000 or 0000. Next the four-weighted bit is set to "one", giving an approximation of either four (0100) or twelve (1100), depending on the first decision. A second decision, similar to the first, is then performed

on this approximation. This cycle is repeated for a number of decisions equal to the number of bits in the level register. Figure 7, "State Diagram for Successive Approximation Conversion", page 44, shows the state diagram for the 16 level case. The numbers in the "states" (circles) are the levels about which the decisions are made, and the numbers over the leaders show the final states of the binaries involved.

Successive approximation conversion is moderately fast and inexpensive. It requires the generation of control pulses, which are also required by the addition functions of the accumulator and base count registers. Thus a single timing pulse generator is used to control both conversion and addition, performing them serially in time, once each sampling period. Conversion requires eight timing pulses (one to set and one for the decision for each bit), addition to the accumulator register requires seven pulses, and addition to the base count register requires one pulse, for a total of 16 timing pulses in each sampling period. The display registers to be used have an upper frequency limit of about 320 kHz for reliable operation, thus the timing pulses can be spaced 3.125 μsec. apart. This allows conversion in 25 μsec., for a sampling rate of 20 kHz. The conversion equipment is capable of operating at

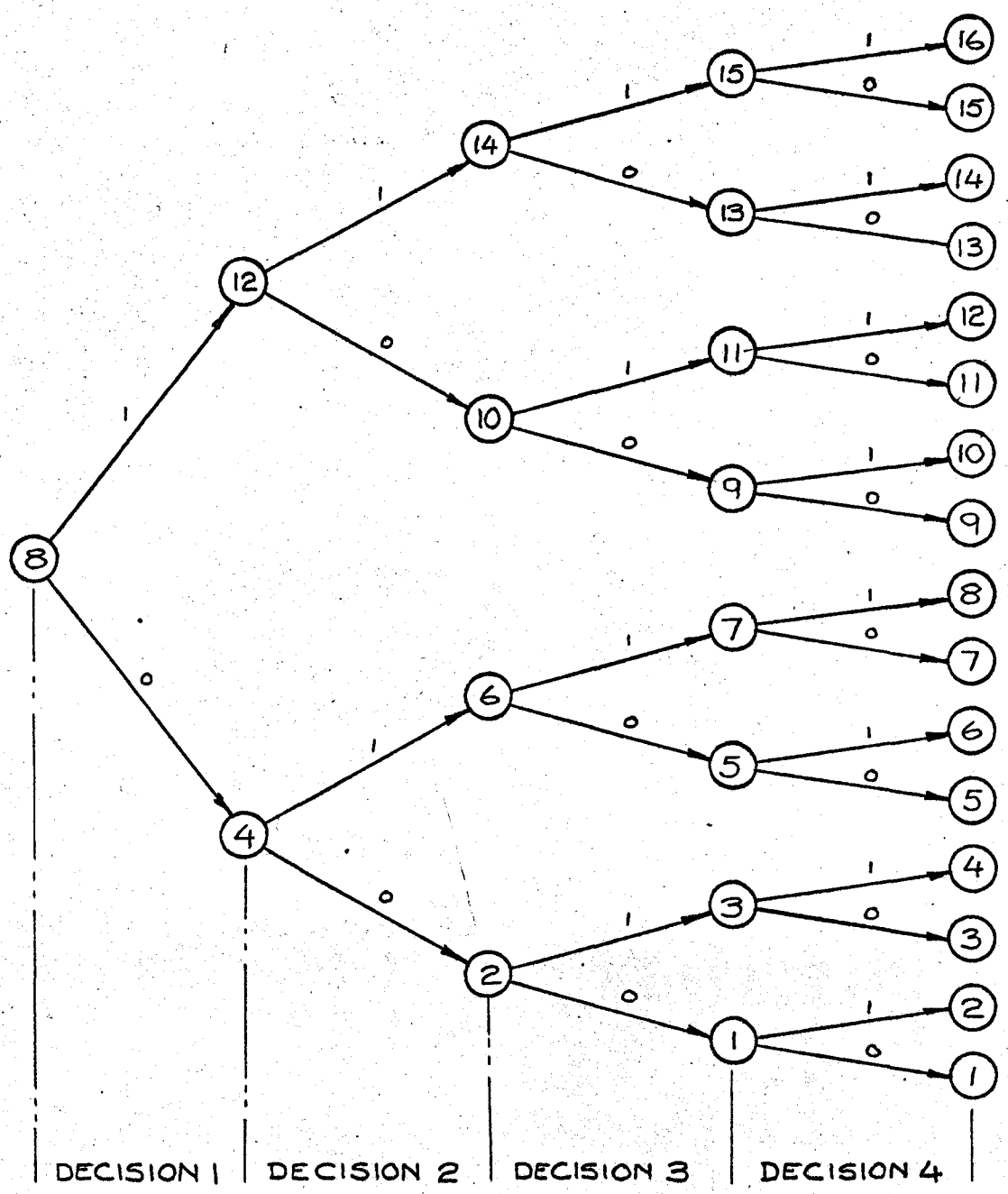


FIGURE 7 - STATE DIAGRAM FOR SUCCESSIVE APPROXIMATION CONVERSION

speeds up to about 1.5 usec. per bit, so that the 6.25 usec./bit allowed gives very generous settling times.

A sampling rate of 20 khz leads to very small error, e_p, due to the use of finite clock pulse rate and duration. For example, for a 5 Hz input frequency, taking the maximum possible mark/space ratio, μ, which is 1.0, the results are

$$e_p \ max = (1+\mu)\frac{f}{p} = 0.05\%$$

for a rectangular wave,

$$e_p \ max = 2(1+\mu)\frac{f}{p} = 0.1\%$$

for a sine wave, and

$$e_p \ max = 3(1+\mu)\frac{f}{p} = 0.15\%$$

for a triangular wave. For the average error values in the above cases, $(1+\mu)$ is replaced by μ, and $e_{p\ avg}$ cannot exceed 0.025%, 0.05%, and 0.075% respectively.

A comparison of the conversion techniques discussed is given in Table III, page 46. Serial operation on conversion and addition is to be utilized because it avoids the provision of a storage register for level information, and because it is within the speed capabilities of the equipment when operating at a desirable sampling rate.

TABLE III - COMPARISON OF CONVERSION TECHNIQUES

Conversion Method	Cost - approx. (D.E.C. Units)	Adjustments	Speed	Comments
Simultaneous	$2,000	numerous	very fast	Too expensive - large number of critical adjustments
Counter	$580	few	100 usec	Too slow (at 6.25 usec/ level)
Continuous	$550	few	very fast	Not accurately realizable
Successive Approximation	$600	few	25 usec (at 6.25 usec/bit)	Most suitable for this application

Accuracy of conversion is similar for all techniques. On the basis of the foregoing analysis, successive approximation conversion is chosen for this application.

REALIZATION

The circuit for the level determination section is shown in Figure 8, "Level Determination Section", page 48. The t_i are the controlling timing pulses. The sequence of operation is as follows:

t_1 - set binary A, reset binaries B, C, and D.

t_2 - reset binary A if required.

t_3 - set binary B.

t_4 - reset binary B if required.

t_5 - set binary C.

t_6 - reset binary C if required.

t_7 - set binary D.

t_8 - reset binary D if required.

t_9 to t_{16} - timing pulses for addition.

In the reference[2], the Cr counts are considered to be created by gating clock pulses of mark/space ratio μ and frequency p. Error due to the finite pulse width and the finite number of samples, e_p, is, for all waveforms considered, a function of μ. The conversion technique adopted possesses a characteristic described as "aperture time" which is analogous to pulse duration.

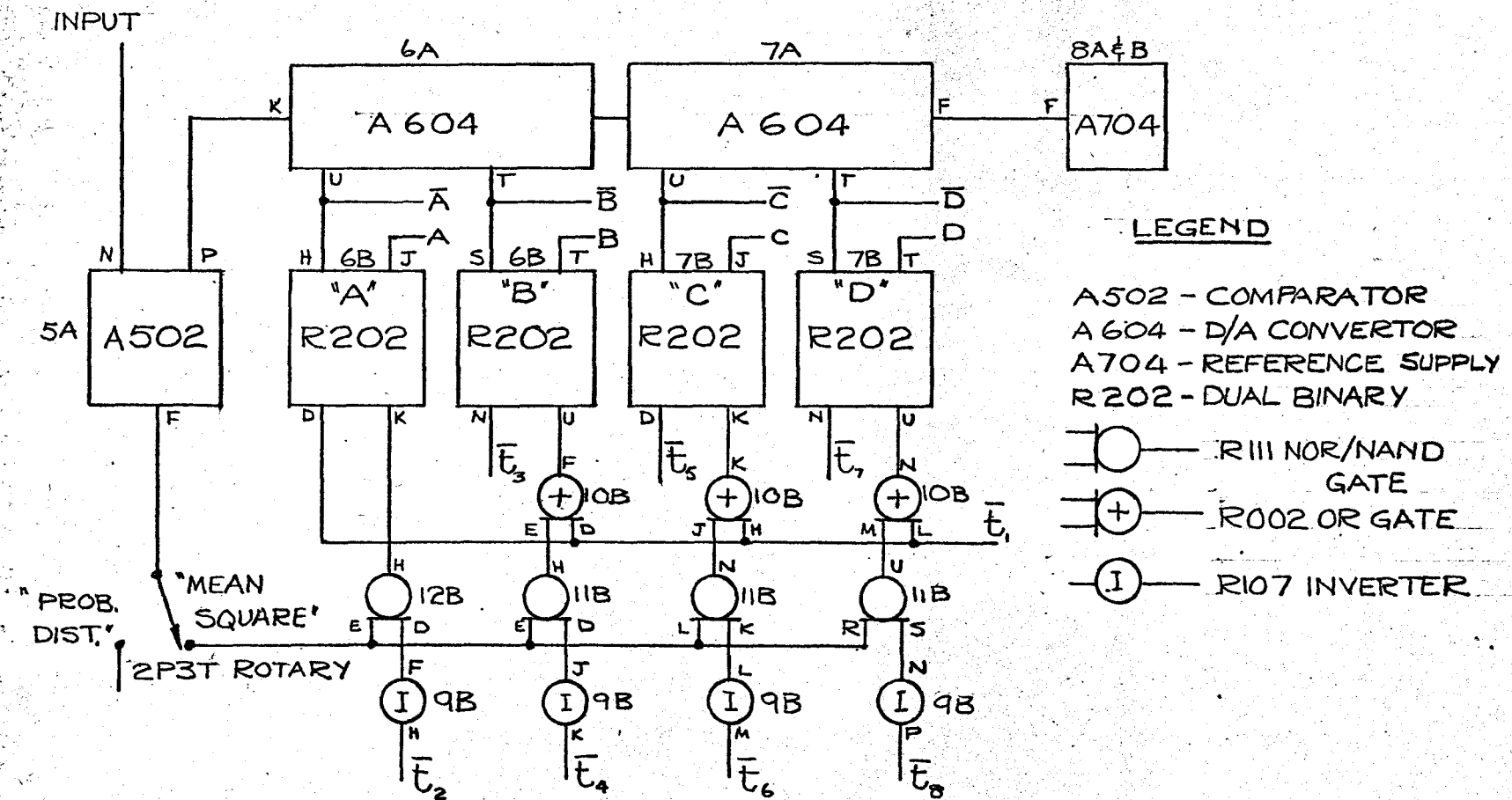


FIGURE 8 - LEVEL DETERMINATION SECTION

Aperture time is the period from the first to the last decision in conversion. This period covers, in this case, seven pulses in sixteen, or 21.875 μsec. at 320 kHz.

The error e_p is a function of μ because if the clock pulse leading edge is taken as the desired sampling instant, it is possible for a count to be attributed incorrectly to a given level if the pulse is gated after its leading edge but before its trailing edge occurs. An analogous error arises from aperture time when a level change occurs during conversion, making it possible for a wrongly weighted input to be entered. Thus in a worst case expression for e_p, if the analogue-to-digital converter timing pulse rate is fixed at 320 kHz, μ is replaced by $(21.875 \times 10^{-6})_p$. If the timing pulse rate is proportional to sampling rate, μ is replaced by 0.4375. This aspect of the instrument is developed further in the next section, where the timing pulse generator design is discussed.

Another form of error resulting from the converter is level displacement error, e_l. This can be seen to be small from the following. The comparator has a resolution of 1.0 mvolt and a common mode error of 5.0 mvolts maximum. The digital-to-analogue converter has a measured maximum error of 5 mvolts. This leads to a maximum possible error of 11 mvolts in

level position. If this magnitude of error existed for all levels the results would be

$$e_l < \frac{4}{\pi} \Delta E = 0.14\%$$

for a sine wave, and

$$e_l = \frac{3}{2} \Delta E = 0.165\%$$

for a triangular wave, due to the converter.

The reference [2] also considers an error e_s resulting from a switching time of T_s for the comparator and gate which admit the pulses to the register. This error does not exist for the conversion method used because input logic settings are completed before the weighted input is added to the accumulator register.

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V COUNTER INPUT LOGIC

Digital logic networks are utilized to transfer weighted input information from the level register to the multiple trigger addition inputs of the accumulator. These networks can be realized with conventional NOR gates alone, or by a combination of gates and a diode matrix. Where level information is available as a unique state of one of sixteen outputs, as can be readily realized from simultaneous conversion, the diode matrix offers considerable economies in logic. However, with successive approximation conversion, where level information is the form of the state of a four binary register, logic requirements are similar for both diode matrix and NOR gate designs. In order to maintain a compatible system using D.E.C. modules wherever possible, the NOR gate realization was used. This section discusses the logic functions required, timing pulse generation, and the modification of the accumulator and count down registers to allow their use in this design.

LOGIC FUNCTION

Vietch-Karnaugh maps for each of the seven multiple trigger addition inputs were generated from a table similar to Table II, page 15. The inputs are the

functions G_i, numbering, in order, from G_1 to G_7, where G_1 is the least significant binary input. The table and maps are shown in Figure 9, "Counter Input Logic Maps", on page 53. The possibility of simplifying the maps by making small changes in the expressions was investigated. The errors created by the alterations were not excessive for familiar waveforms scaled to fill the levels. However, if the instrument is to be used for irregular waveforms that could have high amplitude probability in the altered intervals, the alterations cannot be used -- they severely compromise the generality of the instrument.

Given a Veitch-Karnaugh map, there are two obvious ways to obtain the minimal second order NOR expression:

1) Using the map in the conventional fashion, write the minimal sum of products expression. Then convert the AND terms to NOR terms by use of DeMorgan's theorem. This gives the desired expression at the output of an OR gate.

2) Using a map of the complements, write the minimal sum of products expression. Then use DeMorgan's theorem to obtain the product terms as NOR terms, and complement the entire expression. Here the function is realized entirely with NOR gates.

HIGEST LEVEL EXCEEDED		WEIGHTED INPUT							
DECIMAL	BINARY A B C D	DECIMAL	BINARY G_7	G_6	G_5	G_4	G_3	G_2	G_1
1	0 0 0 1	1	0	0	0	0	0	0	1
2	0 0 1 0	3	0	0	0	0	0	1	1
3	0 0 1 1	6	0	0	0	0	1	1	0
4	0 1 0 0	10	0	0	0	1	0	1	0
5	0 1 0 1	15	0	0	0	1	1	1	1
6	0 1 1 0	21	0	0	1	0	1	0	1
7	0 1 1 1	28	0	0	1	1	1	0	0
8	1 0 0 0	36	0	1	0	0	1	0	0
9	1 0 0 1	45	0	1	0	1	1	0	1
10	1 0 1 0	55	0	1	1	0	1	1	1
11	1 0 1 1	66	1	0	0	0	0	1	0
12	1 1 0 0	78	1	0	0	1	1	1	0
13	1 1 0 1	91	1	0	1	1	0	1	1
14	1 1 1 0	105	1	1	0	1	0	0	1
15	1 1 1 1	120	1	1	1	1	0	0	0

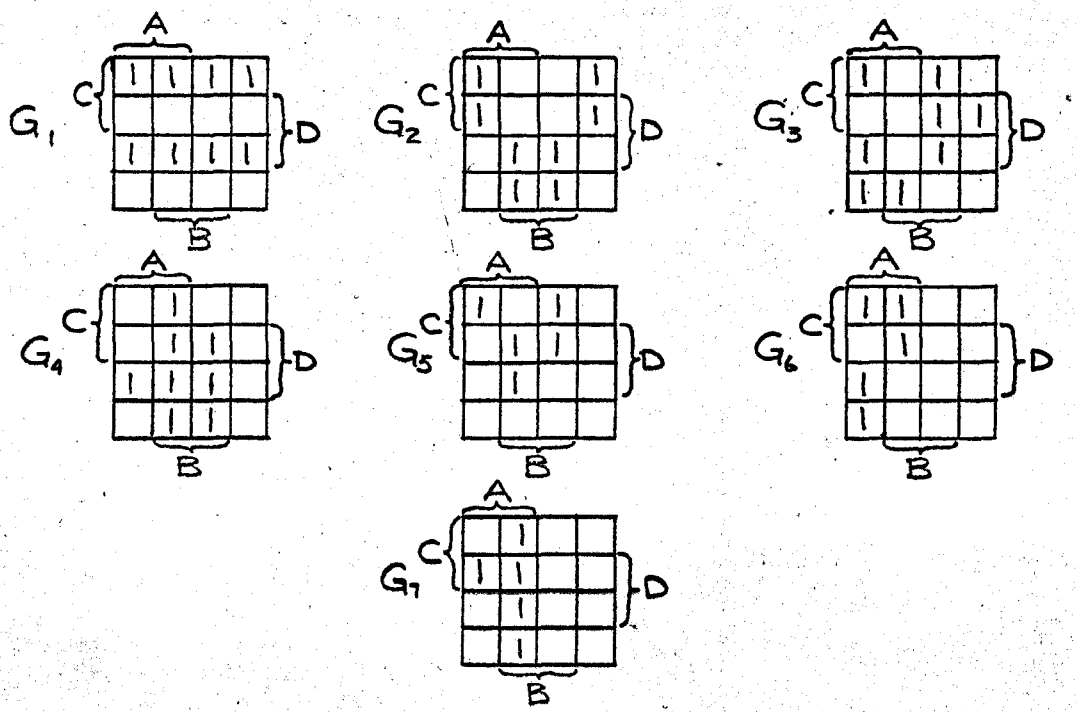
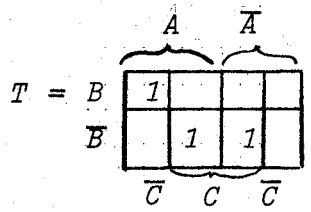


FIGURE 9 – COUNTER INPUT LOGIC MAPS

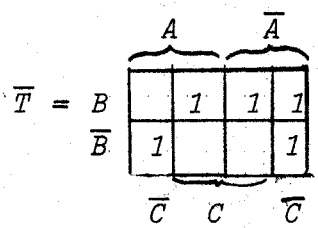
For example, by method 1



$$T = \overline{B}C + A\overline{B}\overline{C}$$

$$\therefore\ T = \overline{\overline{B+\overline{C}} + \overline{\overline{A}+\overline{B}+C}}$$

by method 2



$$\overline{T} = \overline{A}B + \overline{A}\overline{C} + BC + \overline{B}\overline{C}$$

$$\therefore\ T = \overline{\overline{A+\overline{B}} + \overline{A+C} + \overline{\overline{B}+\overline{C}} + \overline{B+C}}$$

In this application, it is necessary to use each function to gate a timing pulse. Thus we need, using the example above

$$G = Tt$$

where t is the timing pulse. Using method 1, this is somewhat complicated in NOR logic

$$G = T\overline{t} = \overline{\overline{T}+\overline{t}}$$

$$\therefore\ G = \overline{\overline{B+\overline{C}} + \overline{\overline{A}+\overline{B}+C} + \overline{t}}$$

However, using method 2, the timing pulse can be incorporated directly into the final NOR gate.

$$G = \overline{\overline{T}+\overline{t}} = \overline{\overline{A+\overline{B}} + \overline{A+C} + \overline{\overline{B}+\overline{C}} + \overline{B+C} + \overline{t}}$$

For the gate functions G_1 to G_7, only one function, G_5, can be realized with fewer gates by method 1 than by method 2. However, since two of the terms derived using method 2 are also required for other expressions, and can be shared, the method 2 result is used for G_5 also. The final expressions are as follows:

$$G_1 = \overline{\overline{C+D} + \overline{C+D} + \overline{t}_{15}}$$

$$G_2 = \overline{\overline{C+B} + \overline{C+B} + \overline{t}_{14}}$$

$$G_3 = \overline{\overline{A+B+C} + \overline{A+C+D} + \overline{A+B+D} + \overline{A+C+D} + \overline{A+B+C} + \ldots \overline{\ldots \overline{A+B+D} + \overline{t}_{13}}}$$

$$G_4 = \overline{\overline{A+B} + \overline{A+C+D} + \overline{B+D} + \overline{A+B+C} + \overline{t}_{12}}$$

$$G_5 = \overline{\overline{A+B} + \overline{A+C} + \overline{C+D} + \overline{B+D} + \overline{A+B+D} + \overline{t}_{11}}$$

$$G_6 = \overline{\overline{A} + \overline{B+C} + \overline{B+C+D} + \overline{t}_{10}}$$

$$G_7 = \overline{\overline{A} + \overline{B+C} + \overline{B+D} + \overline{t}_{9}}$$

Note that $\overline{C+D}$ is common to G_1 and G_5, $\overline{B+C}$ is common to G_2 and G_7, and $\overline{A+B}$ is common to G_4 and G_5. The schematic representation of the logic is shown in Figure 10, "Counter Input Logic", page 56. When a NOR gate on an RIII module is required to assimilate more than two inputs, the diode cards R001 and R002 are used. Connections to diode cards are not shown in the diagrams.

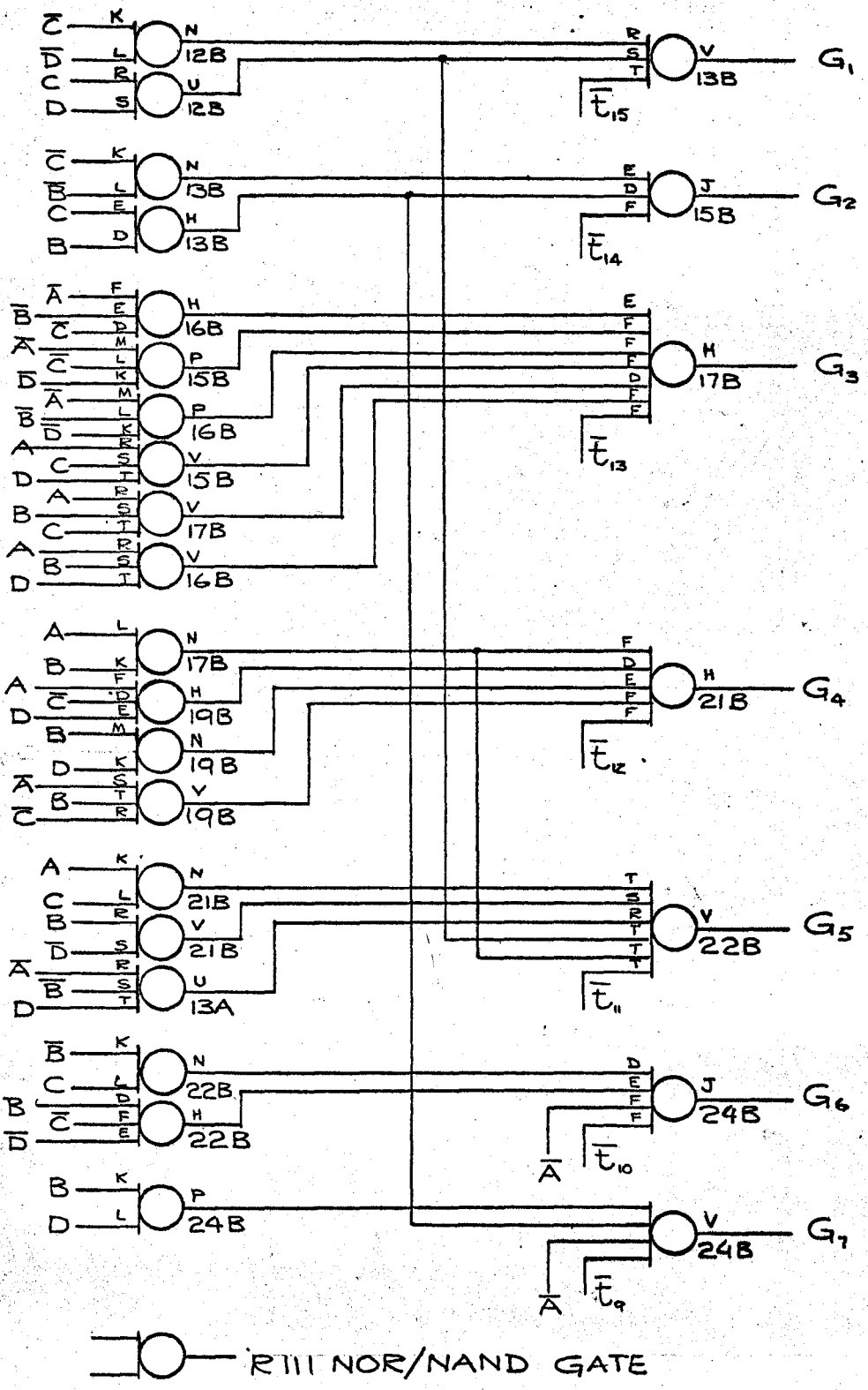


FIGURE 10- COUNTER INPUT LOGIC

TIMING PULSE GENERATION

The timing pulses are formed by counting down from a 320 kHz pulse of 0.5 mark/space ratio with a four bit counter register. Two binary-to-octal decoders (R151) are used to obtain sixteen separate timing pulse outputs. To eliminate spikes in the binary-to-octal decoder outputs due to transient digital states occurring during count propogation, the "enable" inputs of the decoders are derived from two modified R111 NOR gates. One input to each of these gates is the 320 kHz pulse which drives the register, and both gates have a 62 pfd capacitor between the "node" input and ground. This serves to create a 200 nsec delay in gate output rise. Thus the outputs of the decoders are dependent on the 320 kHz pulse, and the rise of the "enable" inputs of the decoders is delayed until count propogation is complete.

The timing pulse clock is an R401 variable clock pulse generator which is set to 640 kHz. This unit delivers only pulses of 100 nsec duration, thus it is used to drive an R202 binary whose output is the 320 kHz desired. The 320 kHz pulse is "enabled" for a period of sixteen timing pulses once each cycle of the master clock generator (Philips PM5720), which operates at the sampling frequency. Thus, once each sampling period, sixteen consecutive timing pulses are delivered at 320 kHz.

The timing pulse generator circuit is shown in Figure 14, "Timing Pulse Generator", page 59.

A proposal to make the timing pulse frequency sixteen times the sampling rate, and thus eliminate a clock pulse generator, was rejected because it gives an aperture-time/sampling-period ratio μ, of 0.4375. This is satisfactory for periodic waveforms, but for non-periodic inputs, specifically low-pass filtered white noise, the error due to the use of a finite sampling pulse rate and duration, e_p, is excessive for μ of 0.4375. In this case

$$e_p = \mu \frac{Z}{p}$$

From the reference[2], Z, the number of zero-crossings per second for white noise through an ideal low-pass filter of cut off frequency f_b is

$$Z = \frac{2}{\sqrt{3}} f_b$$

For non-periodic waveforms, p is set by Nyquist's sampling theorem at $2f_b$, f_b being the highest frequency present in the waveform. Now if μ is 0.4375 and f_b is 5 Hz, $e_p = 25.1\%$. Consider, now, the case at hand. Aperture time is fixed at 21.375 usec., thus as shown before

$$\mu = (21.375 \times 10^{-6})p$$

With this provision, for the example cited above, e_p becomes 0.0123%.

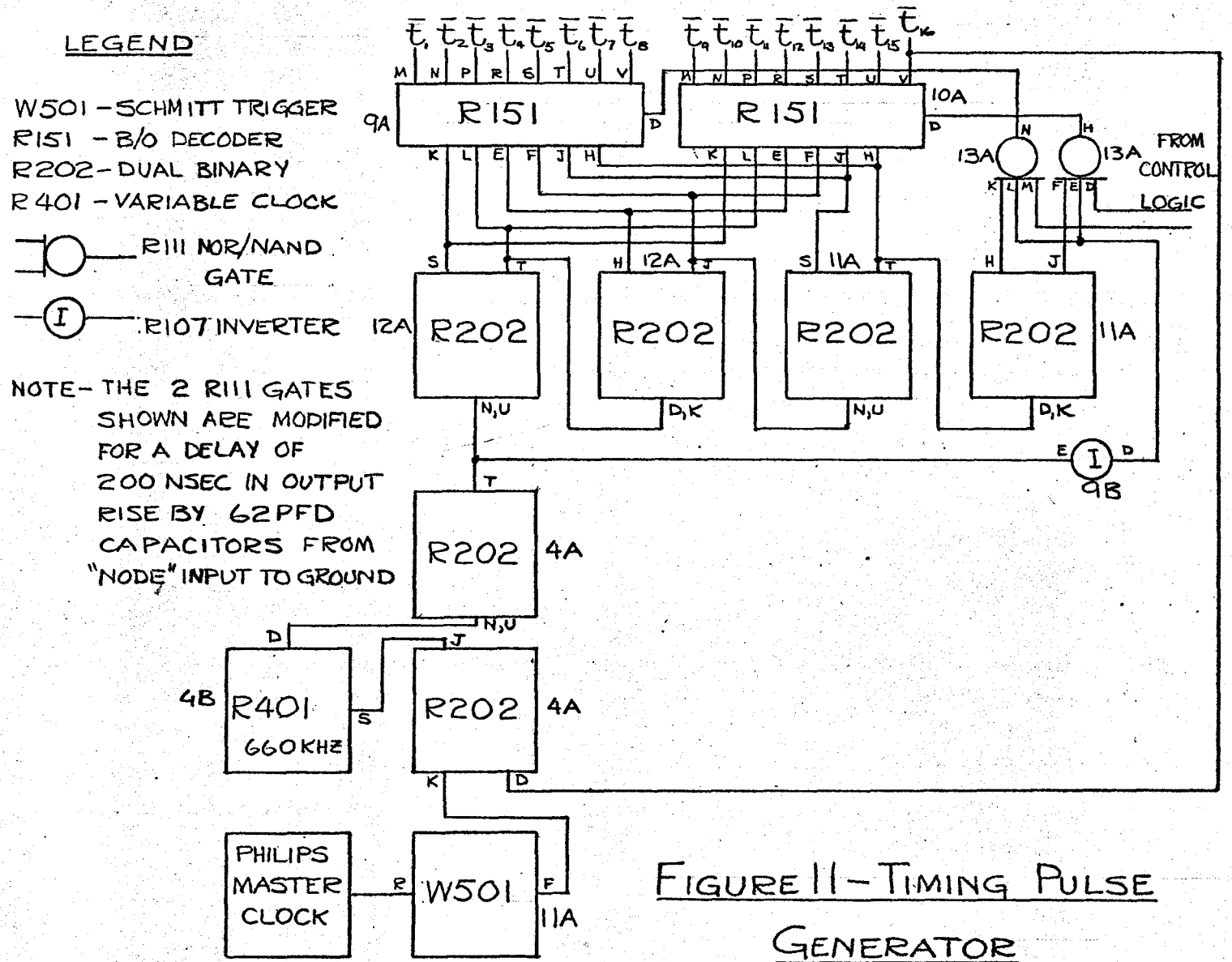
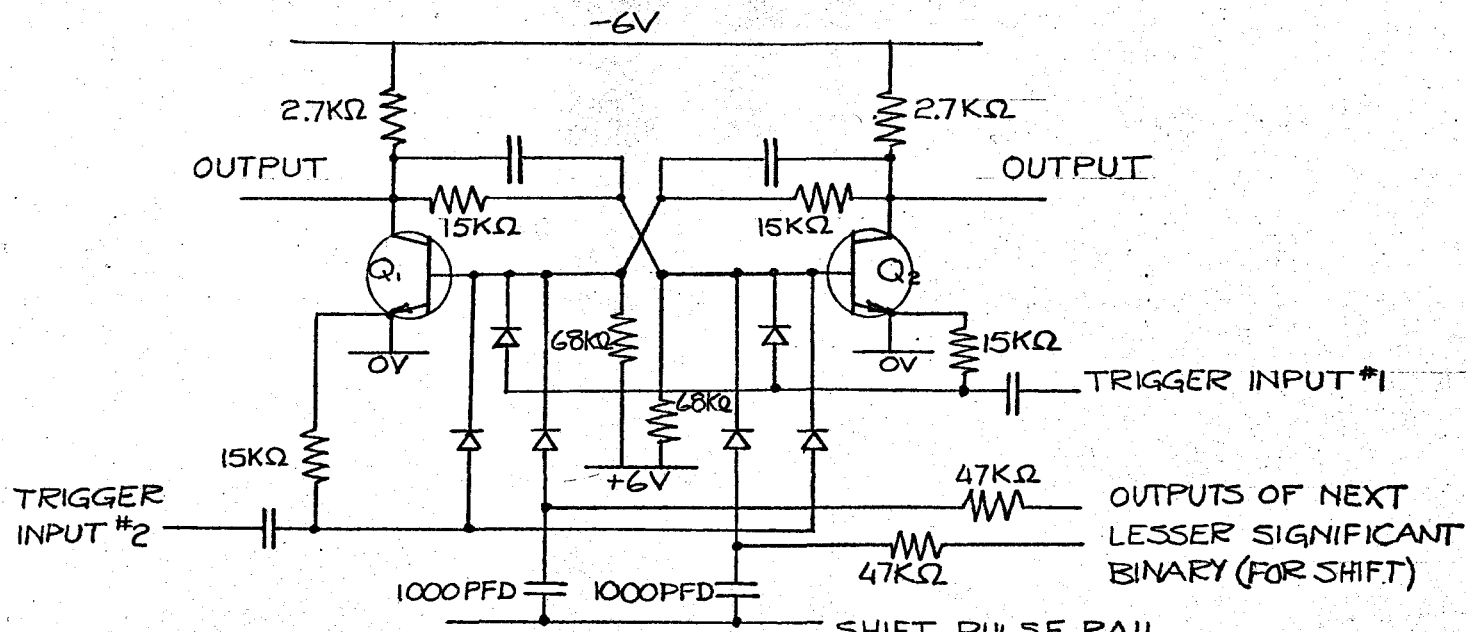


FIGURE 11 - TIMING PULSE GENERATOR

REGISTER MODIFICATIONS

The accumulator and base count registers used were taken from an earlier version of the instrument. Additional trigger inputs to the first eight binaries of the accumulator register are necessary in order to implement multiple trigger addition and an input required for the probability distribution mode of operation. Each input logic gate pulse is differentiated by an RC circuit and then applied to the bases of the transistors (of the Eccles-Jordan binaries) through two diodes of type IN34A or type OC85. The additional trigger circuitry is similar to the original trigger circuits of the registers. Leads from the input logic to the register inputs must be shielded to prevent cross-talk. The circuit for a typical single modified binary unit is shown in Figure 12, "Binary Unit Circuit", on page 61.

The nine most significant bits for both accumulator and base count registers are displayed at the top front panel of the instrument. Since 2^9 is 512, the read-out resolution is about 0.2%. The accumulator register is provided with a manual shift facility to allow nine significant bits to be displayed, even if the register content is small. The read-out registers were originally shift registers only, but modifications were made, adding a count facility.



Q_1, Q_2 - OC44
DIODES - IN34A OR OA85
ALL CAPACITORS 220 PFD DISC.
EXCEPT WHERE NOTED OTHERWISE

SECOND TRIGGER INPUT
PROVIDES FOR MULTIPLE
TRIGGER ADDITION

FIGURE 12 - BINARY UNIT CIRCUIT

It has been shown in the reference[2] that for 1.0% error due to a finite sampling time, e_T, white noise measurements require a base count of 3.4×10^4. This leads to an accumulator register count of 6.53×10^5 for $V_n = 1/2.48$, the largest acceptable value. Thus, using binary registers, the accumulator register must be twenty binaries in length, and the base count register must have sixteen binaries. When the most significant bit of the base count register changes to a "one", the register content is 32,568, which is a reasonable approximation of the 34,000 required.

A possible improvement in the instrument would be the use of decimal counters for the accumulator and base count registers, giving direct decimal read-out. The accumulator register contents could be compiled using a decimal version of the weighted input and addition concepts. A design proposal for the input logic for such an accumulator register is presented in the Appendix, page 88.

VI CONTROL LOGIC

In the foregoing sections of this thesis, the principal portions of the instrument have been developed. This section will develop the control logic which is necessary to allow the instrument to operate on a waveform of 10 volt maximum excursion.

There are two modes of operation to consider, on two basic forms of input waveform to be measured. The device can deliver information leading to the mean square value of the input in the "mean square mode", or to the approximate amplitude probability distribution of the input, in terms of sixteen levels either side of the zero level, in what is termed the "probability distribution mode". The two forms of input are periodic and non-periodic (called "noise" on the control labels of the instrument, for the sake of compactness), each requiring a different means of beginning and ending the sampling process.

The mean square mode compiles $\sum rC_r$ in the upper display register by means of the level determination section, input logic and register trigger inputs described previously. In the probability distribution mode, a level is selected by means of a rotary switch which grounds the appropriate outputs of the level register to hold it in

the binary state corresponding to the level indicated. The polarity of the level is selected by setting the rectifier control switch described in section III to obtain the desired portion of the input waveform. Setting the mode switch to "PROB. DIST." then causes the base count to appear, as usual, in the lower display register, and C_r, the count for the time the input spends beyond the selected level, is compiled in the accumulator register with the same bit weighting in the display as in the base count register display.

The mode switch accomplishes the following when turned from "MEAN SQUARE" to "PROB. DIST."

1) The output of the master clock pulse generator is removed from the timing pulse generation circuit and applied to two NOR gates, one of which is connected to the trigger input of the eighth, or 128-weighted binary of the accumulator register, the other being arranged to drive the C_o register. Both of these gates are also provided with inputs from the binary which controls sampling.

2) The C_o register input is removed from the sixteenth timing pulse output of the timing pulse generator and transferred to the output of the latter NOR gate mentioned above.

3) The level determination comparator output is diverted from the level determination logic to the former of the NOR gates mentioned above. Thus the accumulator register is provided with clock pulses when the input exceeds the analogue equivalent of the selected level. Logic inversion of the comparator output is necessary for this function.

The C_r count is applied to the eighth binary of the accumulator register because in this way equal weighting in both display sections is achieved.

The duration of the sampling process is controlled as follows. Upon depressing the "START" switch momentarily, the timing pulses to the level determination section begin, but the register input pulses are inhibited. If the instrument is set for a periodic waveform, sampling begins with the first negative-going zero crossing of the input after operation of the "START" switch, and ends with the second such crossing. Thus for a waveform with two zero-crossings per cycle, one cycle, the minimum data-gathering period, is sampled. The zero crossings are identified by the change of state of a Schmitt trigger whose input is derived from an emitter follower at the output of the scaler. The thresholds of this Schmitt trigger are zero and -2.2 volts, the

critical change of state being related to the zero volt threshold. The thresholds are obliged to be widely separated to allow the hysteresis characteristic to prevent noise in the waveform from creating undesired, erroneous changes in the module's output.

When the instrument is set for a non-periodic input, it is necessary to momentarily depress the "NOISE START" switch in order to begin the data-collection. Sampling ceases on the change of state of the most significant binary of the C_o register. Thus the period of sampling is controlled by the number of samples taken. This is in accordance with the reference[2], which shows a sample size of 3.4×10^4 samples required for an error due to finite sampling time, e_T, of 1.0% for measurements on low-pass filtered white noise.

A system block diagram showing the control logic in detail is given in Figure 13, "System Diagram Showing Control Logic", pages 67 and 68. Figure 14, "States of Control Binaries During Sampling", page 69, shows the states assumed by the control binaries during

A) a periodic input sampling procedure

B) a non-periodic input sampling procedure.

The sequence of events in gathering data, in either mode, from a periodic input, is as follows:

1. The operator turns on the power switches,

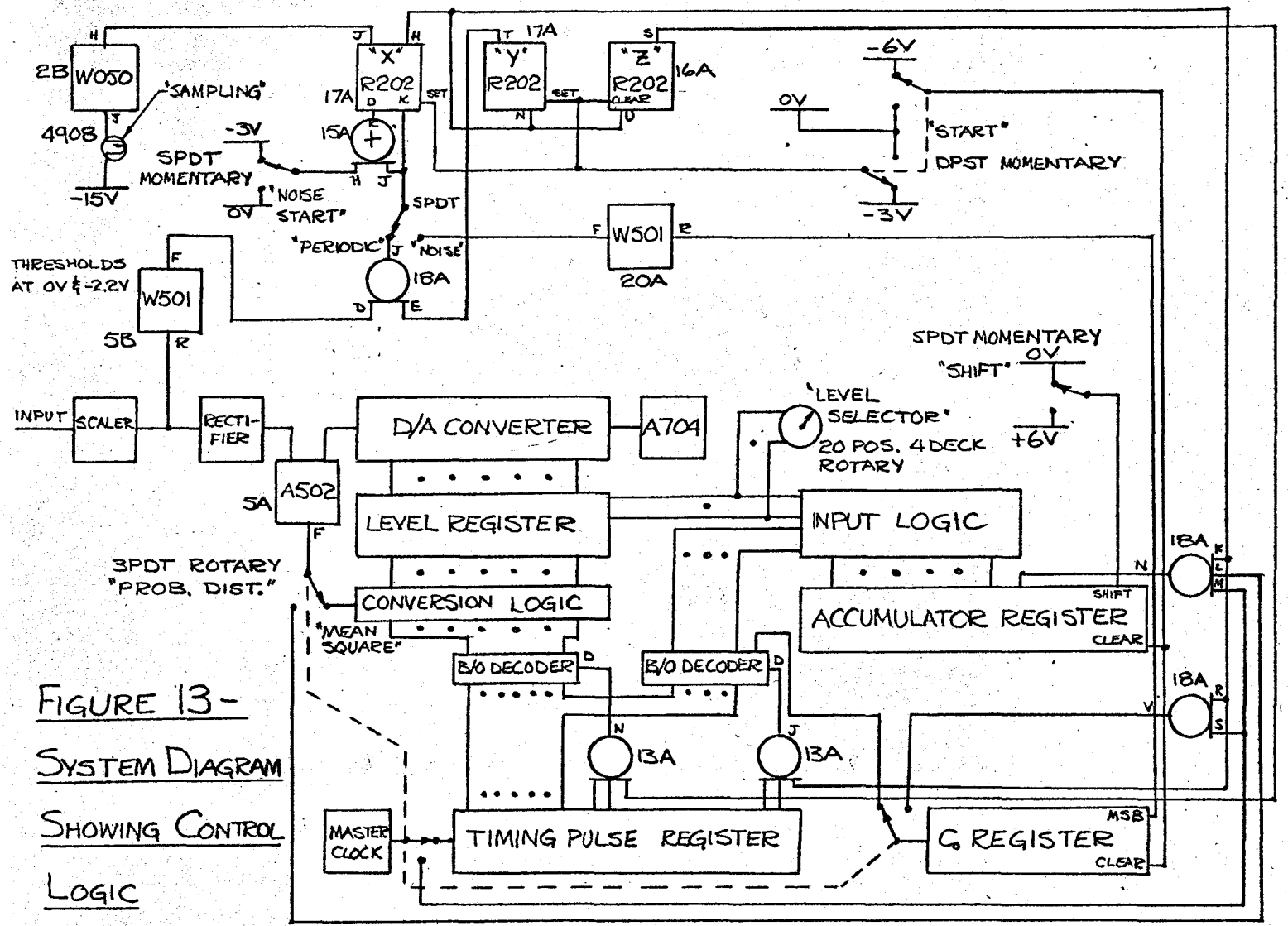


FIGURE 13-

SYSTEM DIAGRAM SHOWING CONTROL LOGIC

SEE LEGEND OVER

LEGEND - FIG. 13

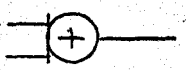
A502 - COMPARATOR

A704 - REFERENCE SUPPLY

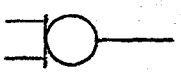
W050 - 30 MA DRIVER

R202 - DUAL BINARY

4908 - INDICATOR LIGHT

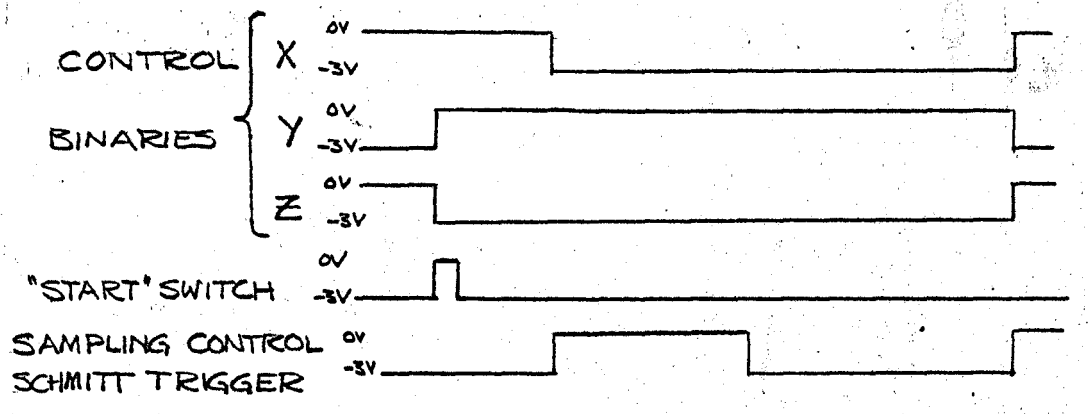


R002 OR GATE

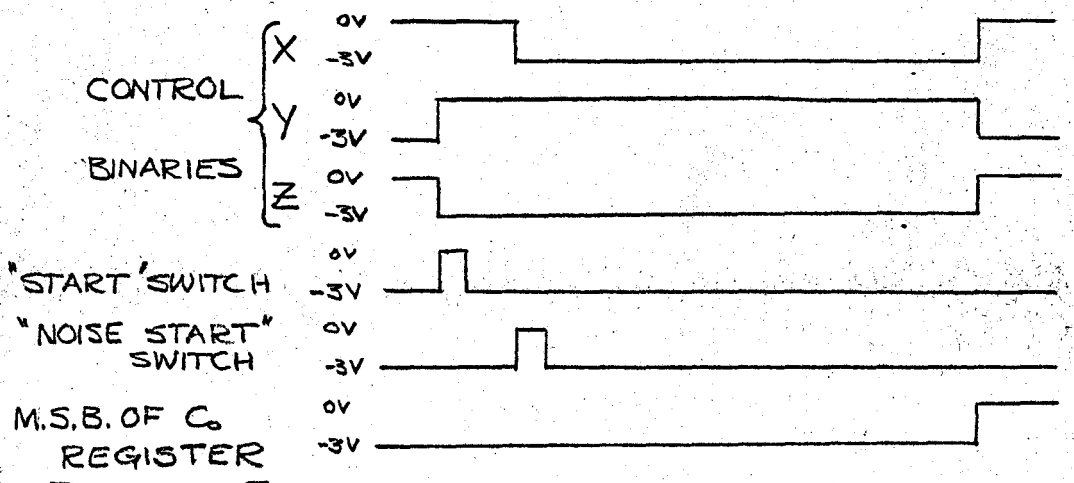


R111 NOR/NAND GATE

A) CONTROL BINARY ACTION – PERIODIC INPUT



B) CONTROL BINARY ACTION – NON-PERIODIC INPUT



BINARY FUNCTIONS

BINARY X ALLOWS SAMPLING WHEN IN -3V STATE
BINARY Y ACTS AS A LATCHING OR "NON-REPEATING" MECHANISM
BINARY Z ALLOWS LEVEL DETERMINATION WHEN IN -3V STATE

FIGURE 14 – STATES OF CONTROL BINARIES DURING SAMPLING

and makes the input connections. The desired mode is selected and the "NOISE/PERIODIC" switch is set to "PERIODIC". The "LEVEL SELECTOR" switch is set to the desired level number for the probability distribution mode, or in any of the blank positions if the mean square mode is in use. The "RECTIFIER CONTROL" is set for the portion of the waveform to be examined. The master clock pulse generator is set to an appropriate sampling frequency, conveniently 4,000 times the input frequency.

2. The "START" switch is depressed momentarily, clearing the accumulator and base count registers and control binary Z, and setting control binaries X and Y. The clearing of binary Z enables timing pulses to be delivered to the level determination section, and this section commences operation. The set condition of binary Y "opens" the NOR gate at the trigger inputs of binary X to allow the gate to pass changes of state of the sampling control Schmitt trigger (described previously) to those inputs.

3. The first change of state of the sampling control Schmitt trigger which produces a rise in the NOR gate output causes binary X to be cleared, and sampling starts as the register input timing pulses are "enabled". The cleared condition of X turns on the "SAMPLING" indicator light.
4. The second rise at the output of the NOR gate, occurring two input zero-crossings later, complements binary X, setting it and ending data-collection. The change of state of X clears Y, thus preventing the NOR gate from changing state again (which would re-start sampling), and sets Z, halting the level determination process.
5. If necessary, the "SHIFT" switch is operated a sufficient number of times to give nine significant bits in the display of the accumulator register contents, the adjustment in bit weighting being noted. The register contents may then be read and converted to decimal code, and the arithmetic required to obtain the desired information may be performed.

For a non-periodic input, the sequence of events is as follows.

1. The settings made are as described above for a periodic input, except that the "NOISE/ PERIODIC" switch is set to "NOISE". This transfers binary X's trigger input from the NOR gate output to the output of a Schmitt trigger driven by the most significant binary of the C_o register.
2. The "START" switch is operated, accomplishing the operations described above for periodic inputs.
3. As no connection now exists between the sampling control Schmitt trigger and binary X, sampling is started by momentarily depressing the "NOISE START" switch. This supplies a rise in voltage to the trigger inputs of binary X, in lieu of the NOR gate output.
4. The change of state of the most significant binary of the C_o register sets binary X, and subsequent events are the same as for the periodic input case.

A convenient test procedure for the register input logic and addition processes can be carried out as follows. Set the instrument for mean square operation on a non-periodic input. However, set the level selector

to some level number. Upon cycling the instrument by operating the "START" and "NOISE START" switches in order, the accumulator register will compile a content equal to the base count multiplied by the weighted input for the level selected. Each level can be tested in this fashion, and correct operation of the logic and the registers can be verified.

VII SUMMARY

The previous sections have described the design of an instrument which utilizes the data-processing concepts advanced in a paper by F. Deist and R. Kitai.[2] Now the use of the instrument, its error characteristics and some possible applications will be considered.

To obtain the mean square value, normalized to the voltage of the highest quantization level, of the waveform under measurement, it is necessary to apply the readings displayed by the instrument to the equation (2).

$$V_n^2 = \frac{1}{4n^2} \left[1 + \frac{8}{C_o} \sum_{r=1}^{n-1} rC_r \right] \text{----------(2)}$$

For the sixteen level case

$$V_n^2 = 0.977 \times 10^{-3} + \frac{1}{128C_o} \sum_{r=1}^{n-1} rC_r$$

A table for the conversion of the accumulator register content in octal form to $\frac{1}{128} \sum_{r=1}^{n-1} rC_r$ in decimal form has been prepared. Some measurements were carried out on low frequency sine and triangular waves generated by Hewlett Packard function generators 203A and 202A.

Evaluation of the results could not be performed accurately because accurate statistical measures of the waveform under measurement could not be carried out by any means other than the instrument under test. However, there were indications that results were consistently within about 2% of the estimated true value, as closely as the latter could be assessed. This degree of accuracy pertains to the mean square value. An evaluation of the cumulative amplitude probability distribution of a 5Hz sine wave gave results shown in the appendix, page 93 . Here a maximum error of 1.28%, occurring at the thirteenth level, was detected. No noise measurements were carried out, but the non-periodic mode of operation was verified as functioning correctly.

The overall theoretical error characteristics of the instrument constructed may now be summarized.

Error due to the use of n levels, e_n, has been shown to be,[2] for sixteen levels

$$e_n = \pm \frac{1}{2(n-1)} = \pm 3.33\% \quad maximum$$

for rectangular wave.

$$e_n = - \frac{0.41}{(n-1)^{1.5}} = -0.707\% \ maximum$$

for a sine wave.

$$e_n = \frac{1}{4n^2} = 0.0977\% \ maximum$$

for a triangular wave.

Figure 6 of the reference[2] shows that for a normal wave and for white noise, e_n ranges from -1.0% to +1.0% for normalized root mean square voltage, V_n, in the range

$$\frac{1}{2.58} < V_n < \frac{1}{7}$$

Error due to a constant level-error, ΔE, at all levels, e_l, would rarely be relevant, but can be used as a severe "worst case test" if the largest level displacement likely to be encountered is considered to exist everywhere. The curve shown in the appendix, on page 86 , for the operational amplifier, indicates that with carefully selected wire-wound resistors for the external elements, in place of the temporary resistors now in use, maximum deviations of 10 mvolts for the rectifier may be confidently expected. It is shown in section IV that not more than 11 mvolts of level-error can be expected from the level determination section. This leads to a maximum level error of 21 mvolts at any level. Thus the "worst case" described above is as follows:

$$e_l < \frac{4}{\pi} \qquad \Delta E = 0.268\%$$

for a sine wave.

$$e_l < \frac{3}{2} \quad \Delta E = 0.315\%$$

for a triangular wave.

$$e_l < \sqrt{\frac{2}{\pi}} \frac{\Delta E}{V_n} = 0.348\%, \quad V_n = \frac{1}{2.58}$$

$$e_l < 0.938\%, \quad V_n = \frac{1}{7}$$

for a normal wave and white noise.

Errors considerably lower than this may be expected.

Error due to the use of a finite clock pulse rate and aperture time, e_p, is dependent on μ. The worst case is considered for periodic waveforms, this being a 5Hz input frequency, f, and a sampling frequency, p, of 20kHz. For this value of p, μ is at its maximum value of 0.4375. For the white noise case, the noise is considered to be ideally low-pass filtered, at a cutoff frequency of 5Hz, leading to p of 10Hz and μ of 2.1875×10^{-4}.

$$e_p \; max = (1+\mu) \frac{f}{p} = 0.0359\%$$

$$e_p \; avg = \mu \frac{f}{p} = 0.00109\%$$

for a rectangular wave.

$$e_p \; max = 2(1+\mu) \frac{f}{p} = 0.0718\%$$

$$e_p \; avg = 2\mu \frac{f}{p} = 0.0218\%$$

for a sine wave.

$$e_{p\ max} = 3(1+\mu)\ \frac{f}{p} = 0.1077\%$$

$$e_{p\ avg} = 3\mu\frac{f}{p} = 0.0327\%$$

for a triangular wave.

For a normal wave

$$e_{p\ max} = \frac{1}{V_n^2}\ (1+\mu)\ \frac{f}{p} = 0.239\%,\ V_n = \frac{1}{2.58}$$

$$e_{p\ max} = 1.76\%,\ V_n = \frac{1}{7}$$

$$e_{p\ avg} = \frac{1}{V_n^2}\ \mu\frac{f}{p} = 0.0729\%,\ V_n = \frac{1}{2.58}$$

$$e_{p\ avg} = 0.535\%,\ V_n = \frac{1}{7}$$

For the noise case stated above

$$e_{p\ avg} = \mu\frac{Z}{p} = 0.0126\%$$

The use of a sampling frequency of 20kHz in spite of the small values of e_p for most 5Hz periodic waves is justified thus: a sampling frequency of 20kHz leads to accumulator register operation at 320kHz, which is the upper frequency limit for reliable counter register operation in this instrument. At this sampling rate the display registers will hold, without overflow, the required counts for familiar periodic waveforms, including the worst-case rectangular wave. The greater the number of samples taken, the lower e_p becomes, thus operation at the rate stated above utilizes the available accuracy which is inherent in the instrument.

If the sampling frequency is set at $4 \times 10^3 \times f$, the base count register will contain 4×10^3, and a substantial portion of its maximum count limit of 8,191 will be available as a precaution against overflow. At this rate, the maximum accumulator register content of over 10^6 will never be exceeded, even for a 10 volt excursion rectangular wave, sampled 8×10^3 times.

White noise is considered to be filtered at 5Hz because this gives approximately the maximum number of zeros per second on which the rectifier can successfully operate without the introduction of error due to the relay switching time. If the rectifier upper frequency limit were increased substantially, perhaps by the use of electronic switching in place of the reed relay, a white noise signal ideally low-pass filtered at 100Hz would lead to

$$e_p = \mu \frac{Z}{p}$$

$$e_p = 0.438\%$$

This is a reasonable value of e_p, indicating that filtered white noise measurements over a much greater frequency range would result from improvements in rectifier speed.

The above results may be compiled in a table similar to Table I, Table IV, Summary of Characteristics, shown on the following page.

TABLE IV - SUMMARY OF ERROR CHARACTERISTICS

Error	Rectangular Wave	Sine Wave	Triangular Wave	Normal Wave		White Noise	
				$V_n = \frac{1}{2.58}$	$V_n = \frac{1}{7}$	$V_n = \frac{1}{2.58}$	$V_n = \frac{1}{7}$
e_n max	$\pm 3.33\%$	-0.707%	0.0977%	-1.0%	$+1.0\%$	-1.0%	$+1.0\%$
e_l	--	$< 0.268\%$	$< 0.315\%$	$< 0.348\%$	$< 0.938\%$	$< 0.348\%$	$< 0.938\%$
e_p max	0.0359%	0.0718%	0.1077%	0.239%	1.76%	--	--
e_p avg	0.0109%	0.0218%	0.0327%	0.729%	0.535%	0.0126%	

Constructed from D.E.C. card modules, the registers described, and a Philip master clock pulse generator, the device is housed in a three-unit relay rack, 21" x 15" x 19", with an external +50 volt power supply for the display register lights. Photographs of the instrument are shown in Figure 15, "Completed Instrument", page 82.

Several possible applications have been suggested for the instrument:

1) the measurement of the ultra low frequency portion of the frequency spectrum of *1/f* noise in electron devices, where a low-pass filter could be used in place of the usual band-pass filter.
2) the evaluation of indices of performance of the form

$$I = \int_o^T e^2 dt$$

in adaptive or optimal control systems.
3) bio-engineering applications, such as, say, the statistical evaluation of electrocardiographic data.
4) Statistical evaluations of the slowly varying parameters that are frequently encountered in chemical processes.

Numerous other applications will almost certainly appear as the availability of the instrument becomes more generally known.

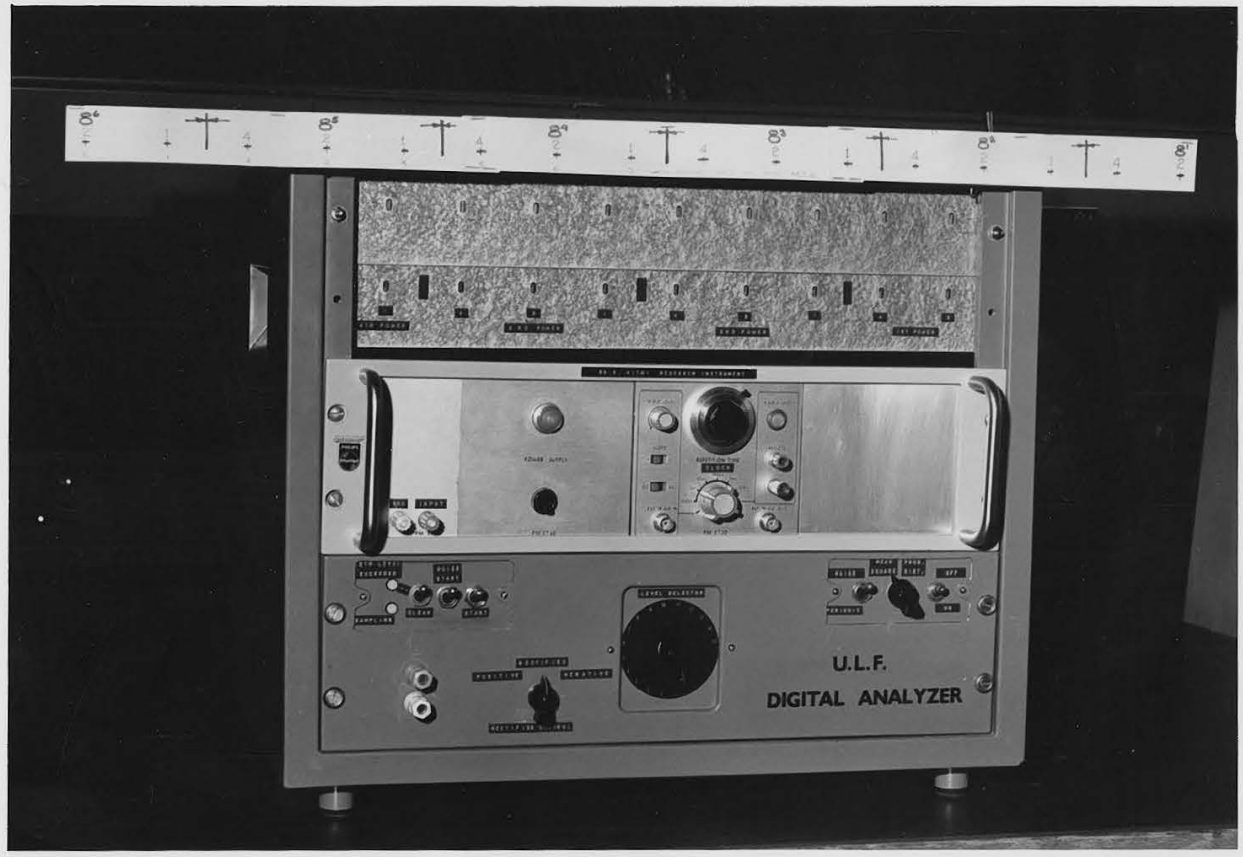


FIGURE 15. COMPLETED INSTRUMENT

The scale above the register display lights is provided to simplify the evaluation of the octal code equivalent of the binary readout.

BIBLIOGRAPHY

1. Kitai, R.: "An Experiment in Probability", Bull. Elect. Eng'g. Education, Vol 23, P. 46, 1959.

2. Deist, F. & R. Kitai: "Digital Transfer Voltmeters: Principles & Error Characteristics", Proc. I.E.E., Vol. 110, No. 10, pp. 1887-1904, Oct. 1963.

APPENDIX

SPECIFICATIONS FOR DATA DEVICE CORP. MODULE C1818

This module consists of two high-stability D-18 operational amplifiers from the maker's "high performance series", complete with regulated power supplies, all card-mounted and requiring only 115VAC for operation. Locations are provided on the card for input and feedback elements. Adjustment potentiometers for the 15 volt regulated supply and for amplifier balancing are included on the card. The amplifiers are short-circuit-proof.

SPECIFICATIONS - D-18 OPERATIONAL AMPLIFIER

Voltage gain: 86dB min., 88dB typ.

Frequency for full output: 15kHz min., 20kHz typ.

Frequency for unity gain: 1.5MHz min., 2.0MHz typ.

Slewing rate: 0.9 volts/μsec. min., 1.25 volts/μsec. typ.

Rated output: ±11 volts at ±2.2ma. min.

Input voltage offset drift:

25 μvolts/24 hr. max.

10 μvolts/°C max., 5 μvolts/°C typ.

Input current offset:

5na. max., 2na. typ. initial offset

1.5na./24 hr. typ. drift

0.65na/°C max., 0.45na./°C typ. drift

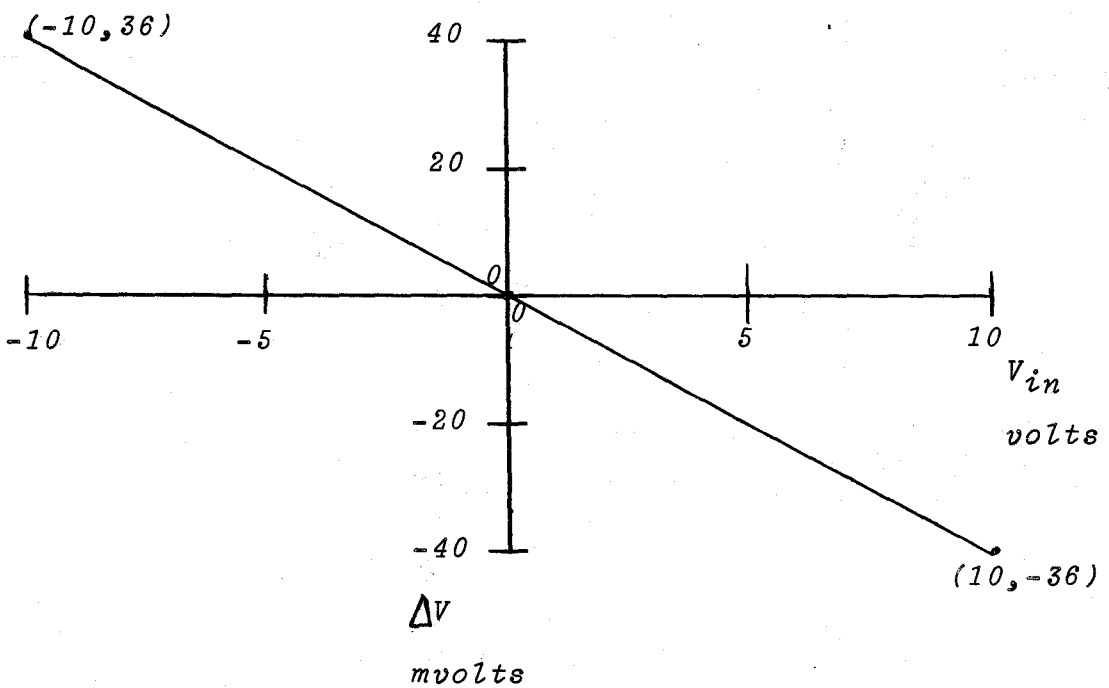
Differential input impedance: 0.6Mohms min., 1.0Mohms typ.

Common mode input impedance: 55Mohm min., 65Mohm typ.

Input noise: 5.0μvolts max., 3.0 μvolts min.

Power requirements: $\pm$15 volts at 12ma max.

The transfer characteristic shown below was recorded on a Moseley "Autograf" X-Y recorder for two amplifiers, each set for unity gain with temporary composition resistors, in series.



$\Delta V = V_{out} - V_{in}$ where V_{out} = output voltage

V_{in} = input voltage

SPECIFICATIONS FOR C.P. CLARE OF CANADA LTD.

RELAY HGSM5009

The relay HGSM5009 is a single-pole, double-throw, mercury-wetted, reed relay. It is mounted, for this application on a D.E.C. blank card W990.

"Must operate" input: 6.4 volts, 12.9ma

Speed: 2 msec max. (at "must operate" level)

Winding: 450 ohm, 28 volts maximum voltage

Contacts: SPDT, mercury-wetted, make-before-break

Relay orientation and winding polarity must be observed.

DECIMAL COUNTER INPUT LOGIC

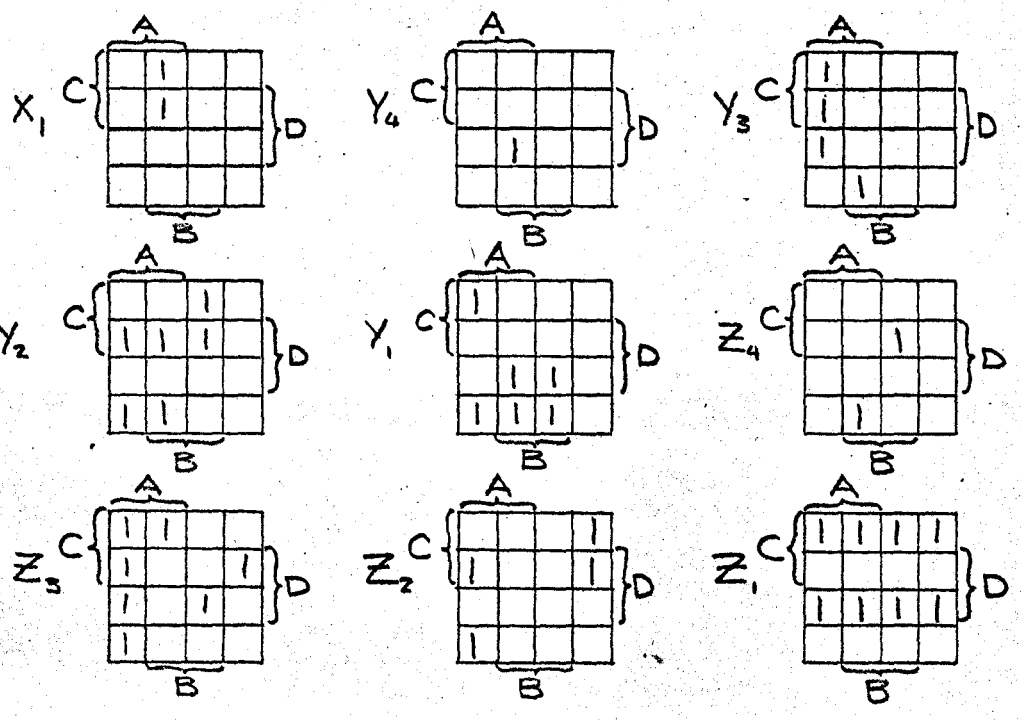
Economic factors led to the use of a binary accumulator register. The weighted input concept could, however, be applied to a decimal counter possessing the ability to assimilate input pulses at its "tens" and "hundreds" sections as well as the normal "unity" input. This section proposes an approach to realization of the weighted inputs to a decimal accumulator register.

Prime consideration is given in this proposal to maintaining a low timing pulse rate. This is done to minimize the input frequency requirements of the counter. Allowing one timing pulse for the hundred-weighted decade (the largest weighted input for a 16 level system is 120), and nine each for the tens and units weighted decades, 19 timing pulses per sampling cycle is the minimum requirement. However, the largest number of pulses actually gated to the decades in one sampling period is 15, when the twelfth level is active and the required weighted input is 78. Thus a reduction in timing pulse frequency results from arranging for the required pulses to be delivered, highest-weighted pulse first, immediately after each other, with any "unused" timing pulses occurring only after all count inputs have been fulfilled.

Using parallel operation on level determination and count input to the accumulator register in order to maintain a low rate of operation, the weighted input for the level determined can be stored in three registers, consisting of one single-binary and two four-binary units. These registers would be count-down registers that would admit count pulses to their respective decades until they had counted down to zero. They would then cause the timing pulse input to be delivered to the next lower-weighted register and decade. Fifteen serial timing pulses from one input line are required for this input system, the level determination requiring, as before, eight serial timing pulses on separate lines, in parallel in time with the counter input operation. The sixteenth pulse is used to transfer the transformed level information to the three storage/count-down registers.

The logic functions required to transform the level register state to the binary-coded-decimal weighted input are shown in Figure 16, "Decimal Counter Input Logic Expressions", on page 90. The expressions are given in AND/OR logic. The X, Y_i & Z_i are the elements of the binary-coded-decimal storage/count-down registers, with register X hundred-weighted, Y ten-weighted and Z unity-weighted. The expressions are derived in a similar fashion to that used for binary counter input logic.

LEVEL REGISTER	DECIMAL WEIGHTED INPUTS								
	100's	10's (BCD)				1's (BCD)			
A B C D	X_1	Y_4	Y_3	Y_2	Y_1	Z_4	Z_3	Z_2	Z_1
0 0 0 1	0	0	0	0	0	0	0	0	1
0 0 1 0	0	0	0	0	0	0	0	1	1
0 0 1 1	0	0	0	0	0	0	1	1	0
0 1 0 0	0	0	0	0	1	0	0	0	0
0 1 0 1	0	0	0	0	1	0	1	0	1
0 1 0 1	0	0	0	1	0	0	0	0	1
0 1 1 1	0	0	0	1	0	1	0	0	0
1 0 0 0	0	0	0	1	1	0	1	1	0
1 0 0 1	0	0	1	0	0	0	1	0	1
1 0 1 0	0	0	1	0	1	0	1	0	1
1 0 1 1	0	0	1	1	0	0	1	1	0
1 1 0 0	0	0	1	1	1	1	0	0	0
1 1 0 1	0	1	0	0	1	0	0	0	1
1 1 1 0	1	0	0	0	0	0	1	0	1
1 1 1 1	1	0	0	1	0	0	0	0	0



$X_1 = ABC$ $\quad Y_4 = AB\overline{C}D$ $\quad Y_3 = A\overline{B}C + A\overline{B}D + AB\overline{C}\overline{D}$

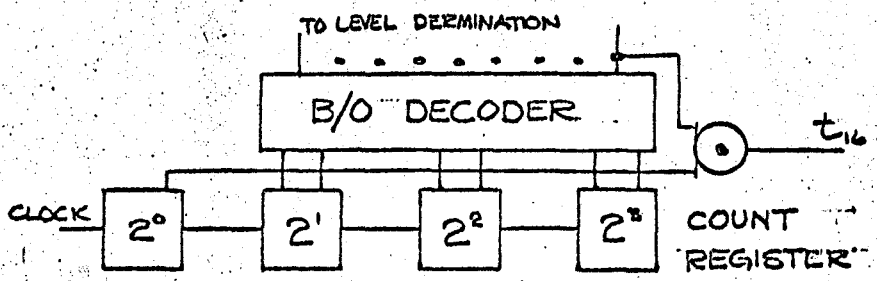
$Y_2 = A\overline{C}\overline{D} + ACD + \overline{A}BC$ $\quad Y_1 = B\overline{C} + A\overline{B}\overline{D}$

$Z_4 = \overline{A}BCD + AB\overline{C}\overline{D}$ $\quad Z_3 = A\overline{B} + AC\overline{D} + \overline{B}CD + \overline{A}B\overline{C}D$

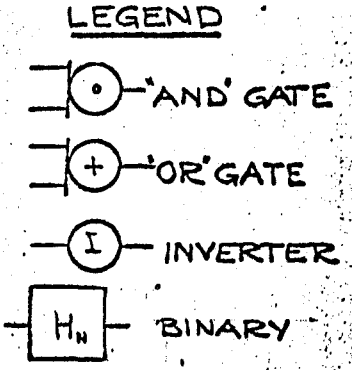
$Z_2 = \overline{A}\overline{B}C + \overline{B}CD + A\overline{B}\overline{C}\overline{D}$ $\quad Z_1 = C\overline{D} + \overline{C}D$

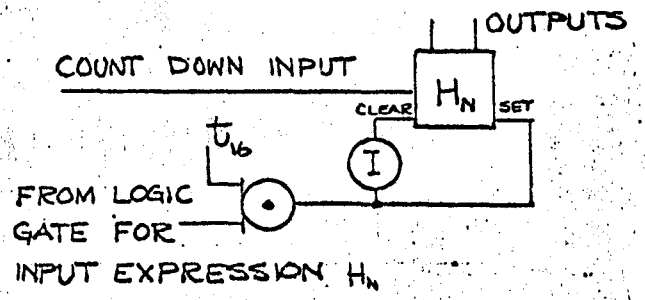
FIGURE 16-DECIMAL COUNTER INPUT LOGIC EXPRESSIONS

The timing pulse generation, a typical information transfer circuit for one binary, and the counter input control logic are shown in Figure 17, "Decimal Counter Input Control Logic", on page 92 .

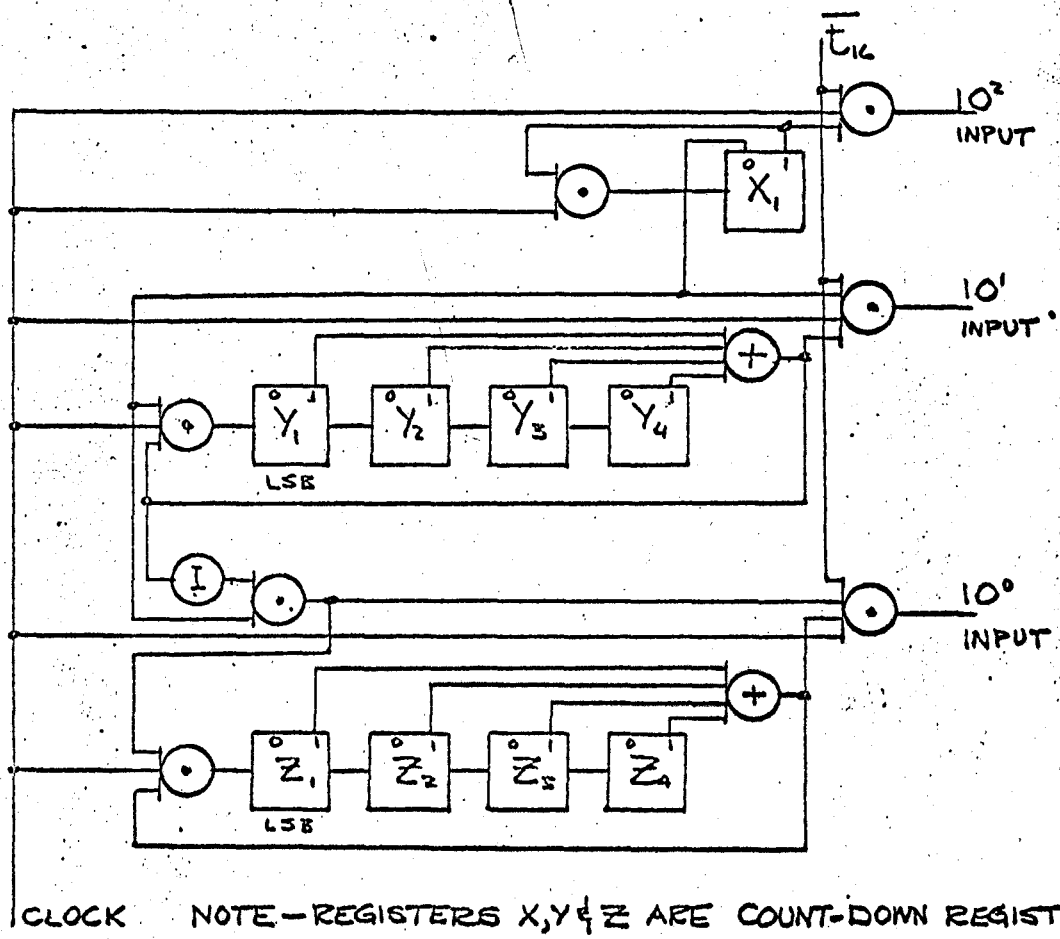


TIMING PULSE GENERATOR





TYPICAL CIRCUIT FOR LEVEL/WEIGHTED-INPUT INFORMATION TRANSFER



NOTE—REGISTERS X, Y & Z ARE COUNT-DOWN REGISTERS

FIGURE 17-DECIMAL COUNTER INPUT CONTROL LOGIC

PROBABILITY DISTRIBUTION OF A SINE WAVE

The completed instrument was used to obtain data on the cumulative amplitude probability distribution of a 5Hz, 10 volt excursion sine wave. The peak of the wave was set as nearly as possible to *10V* as the use of an oscilloscope and the "sixteenth level exceeded" indicator allowed. Table V, Sine Wave Amplitude Probability Distribution, page 94, gives the counts above the levels (the C_r) for a base count of 4096, the resulting measured $P(v)$, the theoretical $P(v)$, and the difference $(P(v)_{measured}-P(v)_{theoretical})$.

TABLE V - SINE WAVE AMPLITUDE PROBABILITY DISTRIBUTION

Level	C_r		P(v)	P(v)	Difference
	Octal	Decimal	Measured	Theoretical	
1	7560	3952	.966	.960	+ .006
2	7300	3776	.921	.921	0
3	7040	3608	.881	.880	+ .001
4	6560	3440	.840	.840	0
5	6300	3264	.798	.797	- .001
6	6020	3088	.755	.756	- .001
7	5540	2912	.711	.713	- .002
8	5240	2720	.664	.666	- .002
9	4740	2528	.618	.620	- .002
10	4420	2320	.567	.570	- .003
11	4100	2112	.515	.518	- .003
12	3520	1872	.457	.460	- .003
13	3100	1600	.391	.396	- .005
14	2430	1304	.318	.322	- .004
15	1620	912	.223	.226	- .003
16	-	-	-	0	-