VACUUM GROWTH AND DOPING OF SILICON FILMS WITH DEVICE APPLICATIONS

VACUUM GROWTH AND DOPING OF SILICON FILMS WITH DEVICE APPLICATIONS

by

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ABSTRACT

The properties and device applications of silicon thin films vacuum evaporated both onto single crystal silicon and onto silicon dioxide substrates have been investigated.

The feasibility of obtaining device quality homoepitaxial silicon thin films by vacuum evaporation onto non heat-treated substrates having temperatures of 700°C has been demonstrated. A new technique, that of gas-doping, has been developed and has been shown to be capable of reproducibly introducing controlled concentrations of doping impurities in the range applicable to device fabrication into the deposited layers. The combined deposition-doping technique has been employed in the production of silicon layers containing impurity steps more abrupt than may be obtained by conventional fabrication techniques.

The electrical properties of the vacuum evaporated homoepitaxial silicon layers have been shown to be comparable in most respects to those of bulk high purity single crystal silicon. The characteristics of rectifying and of varactor diodes prepared by the technique of vacuum evaporation combined with gas doping have been considered.

Silicon films evaporated onto SiO_2 substrates have been shown to possess structures ranging from amorphous through randomly oriented polycrystalline to oriented polycrystalline as the substrate temperature is increased from 25°C to 850°C. The electrical characteristics of doped polycrystalline films obtained both by vacuum evaporation combined with gas doping and by the diffusion-annealing of amorphous films have been shown to be comparable with those reported for similar material deposited

by chemical techniques. The experimentally observed properties of the disordered material have been qualitatively explained employing an inhomogeneous film model. The suitability of thin films of doped polycrystalline silicon on SiO_2 substrates for the production of high value resistors for monolithic integrated circuits has been considered.

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CHAPTER I

INTRODUCTION

1.1 Deposition-doping

The potential advantages of silicon deposition-doping techniques for the direct formation of semiconductor devices has led to considerable interest in these over the last two decades. In such techniques, both the host semiconductor and the electrically active impurity species necessary for device operation are simultaneously deposited onto a suitable substrate. Combined deposition-doping offers, in principle, a greater flexibility in impurity profile for device fabrication than is available by conventional doping techniques where the impurity must be introduced through the surface of the solid host. In addition, by the choice of an appropriate substrate material silicon films possessing a number of crystalline structures applicable for different types of devices may be deposited.

Although a variety of deposition-doping systems have been developed, their application to direct device fabrication has been severely limited by practical limitations. This thesis describes the development and evaluation of a deposition-doping technique which does not suffer from many of the limitations of those previously reported. To set the work in perspective, the general features of silicon deposition techniques applicable to device fabrication will be reviewed and the origin of their limitations considered. Since statements made in this chapter are intended to be of

a general nature, no specific references will be supplied at this point. Further discussion of the topics considered along with appropriate references will be presented in subsequent chapters which describe particular aspects of the present investigation.

Two classes of deposited silicon films find current application in the production of semiconductor devices (a) single crystal films (b) polycrystalline films. While a third class, amorphous films, exists and does possess unique device applications such films will not be considered in this thesis.

1.2 Epitaxial single crystal silicon films

To obtain the single crystal silicon films generally required for active device fabrication, epitaxial growth is employed. In this mode of growth, a single crystal substrate is utilized to provide a regular array of surface sites which, when occupied by depositing atoms, favour the construction of a single crystal lattice. The substrates may consist either of the same material as the deposited layer (homoepitaxy) or, of a different material (heteroepitaxy). For epitaxial growth the adsorbed silicon atoms must possess sufficient mobility to migrate to preferred surface sites. Since the surface mobility of silicon atoms on silicon substrates at room temperature is in general insufficient to permit epitaxial growth, elevated substrate temperatures must be employed. The minimum substrate temperature found necessary to achieve single crystal growth has been found to vary widely for different deposition conditions and systems.

The more commonly employed methods for silicon deposition may be divided into two major categories: those operating at pressures close to atmospheric and those employing high vacuum. In addition to these, a

number of techniques which operate at intermediate pressures ($\sim 10^{-2}$ torr) such as sputtering and vacuum gas decomposition have been evaluated. In the high pressure category the widely characterized chemical epitaxial system employs the partial decomposition of a stream of suitable gaseous silicon compound to obtain deposition on a heated substrate. Dopants are introduced by injection into the gas stream. To obtain appreciable deposition rates and high quality single crystal films by this technique, it has generally been found necessary to employ substrate temperatures in excess of 900°C. At such high temperatures considerable redistribution of doping species may occur both in the substrate and in the depositing layer. Furthermore, since typical present-day chemical vapor transport systems contain sizeable volumes of gas, a finite time will elapse before changes in the injected dopant are reflected in the growing layer. While continued investigations are under way both to minimize autodiffusion by lowering the growth temperature and to eliminate doping-lag by careful reaction chamber design, these processes still limit the application of chemical vapor transport systems to direct device fabrication.

In high vacuum growth techniques the mean free paths of gas and vapor molecules exceed the dimensions of the deposition system. Silicon is supplied to the growth surface either by the evaporation or sublimation of a silicon source or, by the partial decomposition of a gas beam. Recent studies employing ultra high vacuum and severe substrate predeposition heat treatment have indicated that single crystal silicon films having a high degree of structural perfection may be obtained on substrates having temperatures as low as ~350°C for the Si<100> and ~650°C for the Si<111> orientations respectively. At such low growth temperatures autodiffusion

processes are minimal. Vacuum deposition offers,in principle,a number of other advantages for device fabrication. Shadow masking may be employed to directly form active element arrays. Active devices, contacting metals, dielectric layers and passivation materials may,in principal,be deposited in the same pumpdown cycle. In practice it has been found that the system complexity required for multiple source deposition leads to contamination problems. Direct deposition monitoring may be employed in vacuum systems to control layer thickness with an accuracy of ∿10 Å.

Despite their many obvious advantages vacuum epitaxial deposition techniques have not found widespread application in the production of semiconductor devices. The reasons lie in three basic limitations common to systems described in the literature.

(1) The ultra high vacuum ($< 10^{-10}$ torr) under which low temperature epitaxial growth has been demonstrated is difficult to employ in a production facility.

(2) In all studies where low temperature epitaxial growth has been observed, severe heat treatment (typically 1200°C for 10 mins.) has been employed to clean the substrates prior to deposition. Since, in the course of such heat treatment significant diffusion of impurity species may occur, many of the advantages of the subsequent low temperature epitaxial growth are negated.

(3) Although doped epitaxial layers have been obtained by vacuum deposition, no technique for incorporating doping impurities which is sufficiently flexible to utilize the full potentialities of the low temperature growth has been reported.

1.3 Polycrystalline silicon films on amorphous substrates

Since amorphous substrates do not provide an ordered array of preferred energy sites favouring epitaxial growth, silicon films deposited onto these have not been found to form single crystals. Films deposited either by chemical vapor or by vacuum techniques onto substrates having temperatures close to room temperature are observed to be amorphous. Polycrystalline layers may be obtained either by depositing onto heated substrates or by annealing of amorphous films.

Polycrystalline silicon films exhibit electrical characteristics which in general differ widely from those of the bulk single crystal material. Despite the fact that chemically deposited polycrystalline silicon already finds a number of applications in current integrated circuit technology, comprehensive studies of the properties and device applications of this material have only recently been reported. Studies of the properties of silicon films vacuum deposited onto amorphous substrates have been complicated both by inadvertent contamination and by the inability to reproducibly introduce controlled impurity concentrations into the depositing layers.

1.4 Scope of the present investigation

This thesis reports a study of the properties and device applications of silicon films evaporated in high vacuum onto silicon and silicon dioxide substrates. The basic objectives of the investigation were the following:

(1) to determine the feasibility of obtaining device quality single crystal silicon films by vacuum evaporation without employing the restrictive conditions of ultra high vacuum and substrate preheating employed in previous investigations.

(2) to devise and to characterize a flexible doping technique compatible with low temperature vacuum epitaxial growth.

(3) to investigate the electrical properties and device applications of doped evaporated homoepitaxial silicon films.

(4) to investigate the structure, electrical characteristics and device applications of silicon films vacuum evaporated onto SiO_2 substrates.

CHAPTER II

CONDENSATION AND GROWTH OF DEPOSITED FILMS

2.1 Introduction

To serve as a basis for the discussion of some of the experimental results to be presented in later chapters the basic features of current theories which describe the growth of films deposited onto solid surfaces will be considered. The mechanisms resulting in the transfer of an impinging atom from the gas or vapor phase into a solid film may be divided into two steps (a) condensation and (b) incorporation.

2.2 Condensation

An atom or molecule impinging on a substrate surface experiences an instantaneous attraction as a result of surface forces. The interaction between the surface and the incident atom and their energy exchange through van der Waals forces has been treated by several workers.[1,2] Theoretical investigations have considered the problem as a head-on collision of an atom with a one-dimensional lattice of spring connected masses. Such investigations have shown that, if the impinging atoms and those of the substrate have nearly equal masses, the ratio of atoms which condense onto the surface (called "adatoms") to those incident on the substrate should equal unity provided the kinetic energy of the latter is less than 25 times the energy required for an adatom to desorb E_{DES}. The mean relaxation time T_e required for an adatom to equilibrate thermally with the substrate is estimated[3] to be less than $2/\nu$ where ν is the mean adatom-surface vibrational frequency.

Condensed adatoms need not become permanently bound but may migrate over the substrate surface by jumping from one potential well to another, the activation energy for the process being supplied by the substrate. The adatom has a finite lifetime on the surface during which it may migrate to a location where it becomes tightly bound and hence incorporated into the growing layer. If the adatom does not reach such a location it re-evaporates into the vapor phase. The mean residence time T_S is given by

$$T_S \sim \frac{1}{\nu} \exp\left(\frac{E_{DES}}{kT}\right) \tag{2-1}$$

If E_S is the activation energy for adatoms having a surface concentration n_S to jump the distance a from one potential well to the next, the surface diffusion coefficient will be given by

$$D_S \sim a^2 \nu \exp\left(\frac{-E_S}{kT}\right) \tag{2-2}$$

During its stay, an equilibrated adatom will diffuse a distance λ_S over the substrate surface where λ_S is given by the Einstein relation for Brownian motion

$$\lambda_S = (2 D_S T_S)^{\frac{1}{2}} = 2^{\frac{1}{2}} a \exp\left(\frac{E_{DES}-E_S}{2kT}\right) \tag{2-3}$$

Since binding is strong the condensation coefficient for silicon atoms evaporated both onto silicon and onto silicon dioxide substrates may reasonably be expected to equal unity.

2.3 Capture and Growth

2.3.1 Introduction

If the substrate temperature is sufficiently low or the substrate-adatom binding sufficiently high, appreciable migration will not take place

and the adatoms on both single crystal and on amorphous substrates will remain at their original adsorption sites. Deposited films will thus be amorphous. For higher substrate temperatures,the adatom-substrate bond becomes unstable and adatom migration may occur. Adatoms may become trapped by a variety of capture mechanisms. The mechanism predominant for a particular adatom and substrate will depend on the surface structure, the adatom binding, the surface contamination and the adatom supersaturation.

2.3.2 Single crystal substrates

Substrate surfaces which coincide with low index planes of single crystals are, apart from the presence of isolated adatoms and surface vacancies, perfectly flat. In practice,some slight misorientation of the substrate surface is inevitable. Practical surfaces will possess a stepped structure in which wide low index plateaus are separated by monolayer risers or steps. Figure (2-1) shows such a step edge and illustrates the variety of species present which determine the growth process. Under conditions of low supersaturation, growth may be expected to proceed on contamination free surfaces by the step-flow mechanism of Burton, Cabrera and Frank.[4] Adatoms migrate to step edges where they are more tightly bound. Macroscopic growth will take place by the motion of successive steps across the substrate surface. In addition to those steps which result from misorientation, further growth steps may originate at screw dislocations as proposed by Frank.[5]

It has been suggested[6] that adatoms which migrate to step edges travel along these before being finally bound at "kink" sites. Step growth then proceeds by the motion of successive "kinks" along the step edge. Employing a reasonable[7] value of one tenth the heat of vaporization for

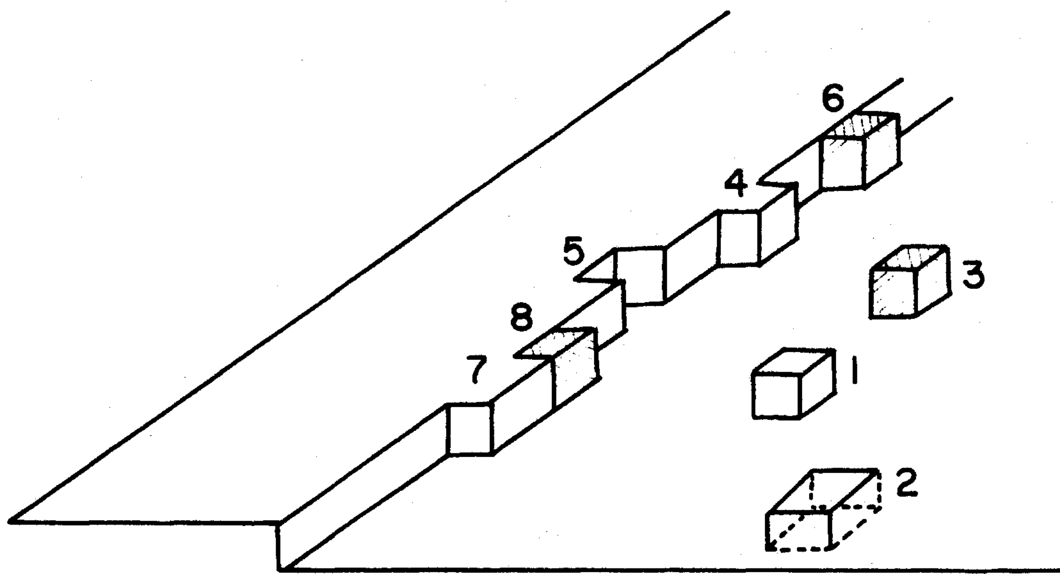


Fig.(2-1) Monomolecular step edge on low index crystal surface (1) adatom (2) surface vacancy (3) adsorbed impurity (4) adsorbed edge molecule (5) edge vacancy (6) adsorbed edge impurity (7) pure kink (8) poisoned kink

the energy of formation of a kink site, "kink" separations are calculated to be approximately four lattice spacings. In the presence of such a high concentration of kinks, diffusion of adatoms along step edges is negligible and such edges may be assumed to act as perfect sinks for adatom capture. In the steady state, the adatom population will maintain quasi-equilibrium with the flux of incident atoms. Mass balancing requires that the incident flux F_{INS} equal the number of adatoms evaporating to the vapor plus those incorporated into the growing layer

$$F_{INS} = \frac{n_s}{T_s} - D_s \left(\frac{d^2 n_s}{dy^2}\right) \tag{2-4}$$

where y = coordinate measured parallel to the surface and perpendicular to the growth step.

The diffusion equation (2-4) may be solved for $\frac{dx}{dt}$, the growth rate perpendicular to the surface by employing the following boundary conditions (1) at the step edge $n_s = n_e$ where n_e is the value of n_s when the surface is in equilibrium with the silicon vapor, (2) in the middle of a step, $dn_s/dy = 0$. The growth rate is given by[8]

$$\frac{dx}{dt} = \frac{h}{L} V_o = \frac{2\lambda_s}{L} \tanh\left(\frac{L}{2\lambda_s}\right) \frac{h}{n_o} \left(F_{INS} - F_{DES}^{EQ}\right) \tag{2-5}$$

where n_o = number of surface adsorption sites/cm^2

h = distance between monolayer planes

V_o = step velocity

L = distance between steps

F_{DES}^{EQ} = desorption flux of adatoms at equilibrium

The effect of impurities on the motion of steps is extremely complex and very poorly understood. Immobile impurities may have the effect of blocking step motion and hence of reducing the number of adatoms incorporated into the growing layer. Mobile impurities may, as illustrated in figure (2-1), be adsorbed at kink sites and hence, by poisoning these, appreciably reduce the capture efficiency of the growth steps. It has been suggested[9] that this process may in turn lead to bunching and to growth by steps which are many monolayers in height.

Under conditions of high adatom supersaturation, if already existing steps are spaced at sufficiently large intervals or are poisoned by contaminating impurities, steps may be continuously created by spontaneous nucleation. Several theoretical studies of this nucleation process have been reported. The approaches used are usually classified either as classical[10] if classical continuous thermodynamics are employed or as atomistic[11-14] if the interactions between individual atoms are considered.

2.3.3 Classical nucleation theory

In the classical theory it is presumed that subcritical adatom clusters are formed by collision on the substrate surface. These grow, initially with an increase in free energy, until a critical size is reached. Further growth then continues with a decrease in free energy. The concentration of single adsorbed atoms on a close packed surface in metastable equilibrium with a supersaturated vapor having pressure p may be obtained by equilibrating the gross vaporization flux ($n_s \nu \exp(\frac{-E_{DES}}{kT})$) with the gross condensation flux ($p/(2\pi mkT)^{\frac{1}{2}}$) giving

$$n_s = [p/(2\pi mkT)^{\frac{1}{2}}]/\nu \exp(-E_{DES}/kT) \qquad (2\text{-}6)$$

We consider the formation of a disk shaped nucleus on the surface. The free energy will be given by

$$\Delta G^{o} = 2\pi r\varepsilon + \pi r^{2} h \Delta G_{v} \qquad (2\text{-}7)$$

where $\Delta G_v = -(\frac{kT}{\Omega})\ \ln\ (\frac{p}{p_e})$ is the Gibbs free energy difference per unit volume of the phase of molecular volume Ω condensed from the supersaturated vapor of pressure p to the equilibrium pressure p_e, r is the radius of the disk, h is the height of the monolayer and ε is the energy per unit length of the monomolecular edge. Minimizing (2-7) with respect to r we obtain the free energy of formation of a critical nucleus

$$\Delta G^{*} = \frac{-\pi\varepsilon^{2}}{h\Delta G_{v}} \qquad (2\text{-}8)$$

If we assume that the population of critical nuclei is equilibrated with that of the single adsorbed atoms we obtain

$$n^{*} = n_{s} \exp\left(\frac{-\Delta G^{*}}{kT}\right) \qquad (2\text{-}9)$$

for the concentration of nuclei of critical size.

Including statistical and non-equilibrium factors the rate of two-dimensional nucleation is given by[10]

$$J = (\Delta G^{*}/4\pi kT\ i^{*2})^{\frac{1}{2}} 2\pi r^{*}\ a\ \nu n_{s} n_{o} \exp\left(\frac{-\Delta E_{s}}{kT}\right) \exp\left(\frac{-\Delta G^{*}}{kT}\right) \qquad (2\text{-}10)$$

where i* = number of atoms in critical nucleus.

Equation (2-10) indicates that the nucleation rate increases from a very small to a very large value in some narrow interval of supersaturation. This effectively critical supersaturation may be obtained from (2-8) and

(2-10) and is given by

$$\left(\frac{p}{p_e}\right)_{CRIT} = \exp\left(\frac{\pi \varepsilon^2 \Omega}{65\, h\, k^2 T^2}\right) \qquad (2\text{-}11)$$

Generally it is assumed that $\varepsilon = h\sigma$ where σ is the specific solid-vapor interfacial free energy. In practice, the presence of sinks on the substrate surface may result in a value of $(\frac{n_s}{n_e})$ which is considerably lower than that of $(\frac{p}{p_e})$. The condition for critical adatom supersaturation may thus be expressed as

$$\left(\frac{n_s}{n_e}\right)_{CRIT} = \exp\left(\frac{\pi h \Omega \sigma^2}{65\, k^2 T^2}\right) \qquad (2\text{-}12)$$

If, for silicon, h is taken to be 3.14 Å and σ is taken to be 1240 erg/cm^2[15] equation (2-12) yields a value of $(\frac{n_s}{n_e})_{CRIT} \sim 8$.

The equilibrium vapor pressure for silicon as a function of temperature has been measured at high temperatures by Honig.[16] Extrapolation of this data to the substrate temperatures (~700°C) and deposition rates (~3 monolayers/sec) of interest for low temperature device fabrication gives a value of $(\frac{p}{p_e}) \sim 3 \times 10^7$. In the presence of such a high pressure supersaturation, if no sinks were present on the substrate surface, i.e. $(\frac{p}{p_e})_{CRIT} = (\frac{n}{n_e})_{CRIT}$, equation (2-12) predicts that spontaneous nucleation would occur. In practice, a number of adatom sinks will be present on the surface whose concentration will depend on the substrate misorientation, dislocation density and degree of surface contamination. The value of $(\frac{n}{n_e})_{CRIT}$ required for spontaneous nucleation will thus be determined by these parameters. Furthermore, since adatom supersaturations as high as 10^6 have been reported on silicon substrates without spontaneous nucleation, the validity of (2-12) is uncertain.

2.3.4 Atomistic theory

The size of the critical nucleus as suggested by the classical nucleation model is typically of atomic dimensions containing only a few atoms. Consequently the applicability of this model and the use of bulk thermodynamical quantities for such small clusters is questionable. The atomistic theory of nucleation considers the interactions between individual adatoms on the substrate surface. The stability of adatom clusters is derived from the decrease in free energy as a result of bond formation. As before, for sufficiently low substrate temperatures, the substrate-adatom bond is stable and the adatom has an effectively infinite surface lifetime. For higher substrate temperatures, the adatom-substrate bond becomes unstable and the adatom migrates over the substrate surface. If this adatom meets a second adatom, the two may form a stable cluster which will then become a centre for further growth. If the adatom fails to meet a second adatom within its surface lifetime T_S, it will re-evaporate. For yet higher substrate temperatures configurations with 3,4,... etc. atoms will constitute the minimum stable cluster.

Walton[11] has treated the problem by calculating the partition function of a two dimensional adsorbed gas comprising of different molecules, each molecule corresponding to a cluster of a given size and structure. Employing statistical mechanics he has derived an expression for the density of critical nuclei.

$$n_{i*} = n_o \left(\frac{n_s}{n_o}\right)^{i*} \exp\left(\frac{E_{i*}}{kT}\right) \qquad (2\text{-}13)$$

where n_{i*} = density of critical nuclei where nuclei contain i* atoms

E_{i*} = binding energy of critical nucleus

From (2-13) the rate of formation of stable nuclei is given by

$$J_{i*} = W_{1i*} n_{i*} \quad (2\text{-}14)$$

where w_{1i*} = the capture rate of single atoms by a cluster containing $i*$ atoms.

By assuming a suitable model of the capture process, w_{1i*}, J_{i*} and hence the saturation density of nucleation centres N_S may be estimated.

Lewis and Campbell[12] have considered the system on the basis of three competitive processes (a) adatom capture by a stable nucleus (b) combination of two adatoms with one another to form a stable nucleus (c) re-evaporation of adatoms which have completed their surface lifetime. These workers have calculated adatom capture areas in terms of ν, E_{DES}, E_S, F_{INS} and n_O and hence, employing expressions (2-1) and (2-3), have obtained values of w_{1i*} in terms of these parameters.

Three basic cases were considered.

(1) when the deposition rate is such that the capture areas of the individual adatoms do not contain a second atom, no nucleation will occur.

(2) when the deposition rate is such that a fraction of the adatom capture areas contain a second adatom, partial nucleation and partial re-evaporation will be observed.

(3) when the deposition rate is such that all of the adatom capture areas contain a second adatom, nucleation will be complete and no re-evaporation will occur.

The following expressions for N_S, the saturation density of nucleation centres, were derived:

case (2) partial re-evaporation: pairs stable

$$N_s = n_O \exp [-(E_{DES}-E_S))/kT] \quad (2\text{-}15)$$

case (3) no re-evaporation: pairs stable

$$N_S = (n_o F_{INS}/\nu)^{\frac{1}{2}} \exp(E_S/2kT) \qquad (2\text{-}16)$$

On the basis of a somewhat different model expressions which are identical to these apart from the values of constants of order unity have been given by Logan[13]. Both Logan and Joyce et al.[14] have given expressions for N_s derived under the assumption that triplets are stable and no re-evaporation occurs.

$$N_S = F_{INS}^{2/3} \left(\frac{n_o}{\nu^2}\right)^{1/3} \exp[(E_2 + 2E_s)/3kT] \qquad (2\text{-}17)$$

where E_2 = binding energy of a pair of atoms.

2.3.6 Amorphous substrates

Condensation coefficients for silicon atoms incident on SiO_2 or, after the first few monolayers of growth, incident on disordered silicon may again be expected to equal unity. For substrate temperatures in excess of that at which the substrate-adatom bond is stable, some recrystallization may take place as a result of annealing within amorphous films. The deposited layers will thus possess a randomly-oriented polycrystalline structure. Since any such recrystallization will favor the further ordering of subsequently deposited material, crystallite size may be expected to increase with increasing film thickness. For higher substrate temperatures, nucleation may occur and a preferred orientation be observed in the crystallites comprising the deposited film. Walton[17] has suggested that, in the absence of absorption of a nucleus possessing any preferred orientation, a <111> orientation will be favored at temperatures where two atoms form a critical nucleus. The growth of oriented films on amorphous substrates has been considered in detail by Bauer.[18]

2.4 Discussion

While the qualitative features of the growth processes of single crystal films on contamination free single crystal substrates are understood, the large number of parameters encountered make detailed growth mechanisms difficult to characterize in practical situations. Moreover, many of the critical parameters such as adatom binding energies and surface vibrational frequencies are difficult to determine from measurements on macroscopic layers. In addition, current theories, in general, consider simplified models and thus fail to account for practical situations where growth is often determined by such phenomena as preferential adsorption and simultaneous "step" and island growth.

Both the "step flow" and nucleation mechanisms described in this chapter are extremely sensitive to small concentrations of contaminating impurities. Such impurities may have the effect of reducing the step velocity, of "bunching" steps, of reducing the adatom supersaturation required for nucleation and of modifying the growth of nucleation centres. Since, in practical situations some degree of contamination is inevitable, these effects further complicate the growth process.

For the case of silicon deposited onto contamination free, low index, single crystal substrates,layer growth for low adatom supersaturations should proceed by the motion of successive steps which originate both at dislocations and, as a result of substrate misorientation. If the adatom supersaturation is raised sufficiently either by increasing the deposition rate or by lowering the substrate temperature spontaneous nucleation may occur at points distant from existing steps. The nucleation centres should initially consist of clusters of a few atoms and should spread rapidly having a thickness of not more than a few monolayers. As the supersaturation

is further increased this spontaneous nucleation may become the predominant source of growth steps.

While detailed discussion of the experimentally observed growth processes of deposited silicon films on silicon substrates will be deferred until chapter (4), features generally observed are as follows.

(1) For silicon substrates which have been cleaned by heating in high vacuum to temperatures close to their melting point, both initial and subsequent growth at 800°C are observed to take place by the propagation of steps having a thickness of not more than a few monolayers. This mode of growth corresponds, at least qualitatively, with the step flow theory of Burton et al.[4]

(2) For substrates which have not been cleaned by high temperature preheating, initial growth under identical conditions is observed to take place by the formation of three dimensional islands. With continued deposition the islands grow in size and finally coalesce to form a continuous layer. The height of these islands may reach many hundreds of angstroms before the films become continuous. This mode of initial growth, subsequently referred to in this thesis as the three dimensional island mode of growth, has been attributed to the presence of mobile impurities on the silicon surface, the precise mechanism being unknown.

CHAPTER III

APPARATUS, MATERIALS, AND DEPOSITION PROCEDURES

3.1 Introduction

The apparatus employed in this investigation was designed to permit the evaporation of high purity silicon films at controlled rates onto heated substrates in a high or ultra high oil free vacuum. The deposited films were doped by directing a stream of suitable doping gas at the substrate surface during deposition. Figure (3-1) shows a photograph of the exterior of the vacuum evaporation system.

3.2 Apparatus

3.2.1 Vacuum system

The vacuum chamber consisted of a Varian model 935-0022 18 inch diameter stainless steel bell jar.This was roughing-pumped to 10^{-3} torr by means of three liquid nitrogen sorption pumps. Further pumping was by a 500 torr-litres/sec ion-pump, a titanium sublimation pump and a large liquid nitrogen cooled cryopanel. System pressures were measured employing a nude ion-gauge calibrated for nitrogen inserted directly into the vacuum chamber. Complementary pressure measurements could be obtained from the ion-pump. The principal residual gases present in the system were identified employing a Varian model 974-0035 partial pressure analyzer. Pressure values subsequently quoted were not corrected for the differences in ionization cross-sections.

In the course of the experiments the system was operated in two pressure modes. In the first, the ultra high vacuum mode, the bell jar-base flange was sealed with a copper gasket and a 24 hour pumpdown bakeout cycle

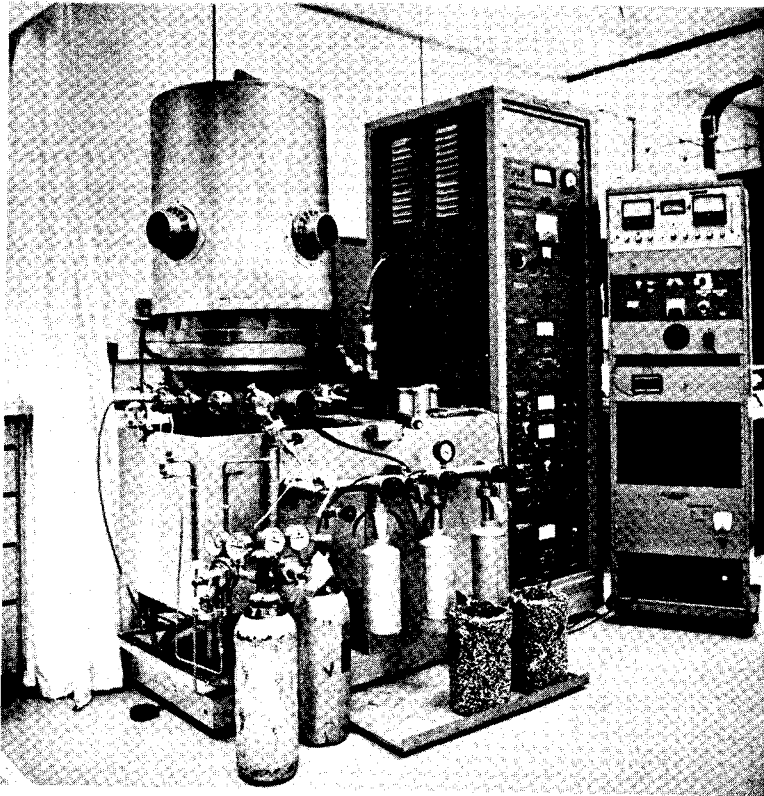


Fig (3-1): Vacuum evaporation system.

with all pumping systems was employed to achieve a base pressure of $\sim 5 \times 10^{-11}$ torr. In the second, the high vacuum mode, the system was not baked and was pumped only by ion and cryo-pumping. Employing a reusable viton bell-jar base seal, system pressures of 5×10^{-9} torr were obtained. The principal residual gas concentrations detected at the base pressures in the two modes are shown in table (3-1).

Table (3-1)

Percentages of Principal Residual Gases Present in System at Base Pressure in High Vacuum and Ultra High Vacuum Modes

Mode	Total Pressure Torr	H^+ and H^{++}	N_2^+ and CO^+	O_2^+	OH^+ and HOH^+	Other
Hi.Vac.	5×10^{-9}	34%	43%	8%	4%	11%
Ultra Hi.Vac.	7×10^{-11}	30%	40%	12%	1%	17%

The walls of the vacuum chamber were screened from the evaporating silicon by employing a removable stainless steel shroud. To minimize contamination by flaking silicon, portions of this shroud which were exposed to the evaporating silicon were etch-cleaned in CP_4-A ($3HF$-$5HNO_3$-$3CH_3COOH$) after each series of 10-15 depositions. After etching, the stainless steel was rinsed well in deionized water before drying and replacing in the system. Prior to ultra high vacuum depositions or, to changes in the injected doping type all the removable parts of the shroud were subjected to the etch-cleaning procedure.

A system of windows and metal mirrors allowed both the substrate and the evaporation source to be directly viewed during deposition.

3.2.2 Silicon evaporation

Silicon evaporation was by electron beam bombardment from Varian model 980-0001, 2 kW, water cooled evaporation units. The design of such units minimizes contamination of the evaporant by the crucible material by permitting evaporation to take place from a molten pool in the centre of an otherwise solid silicon charge. Deposition rates ranged from ∿3 Å/sec to ∿25 Å/sec with a source to substrate distance of 8 inches. Employing this source to substrate distance, the design of the evaporation units permitted ∿1 μ of silicon to be deposited either in a single evaporation or as the sum of a series of evaporations from each silicon charge. For total depositions greater than ∿1 μ the evaporation charge frequently "exploded" showering the system and sample with droplets of molten silicon.

The evaporation rate and film thickness were monitored during deposition employing a Sloan quartz oscillator monitor. Later direct measurements of film thickness were made using multiple beam interferometry.

The evaporation charges were cut, employing a diamond saw from P-type float-zoned single crystal silicon having a resistivity of >100 ohm-cm and an oxygen content $<2 \times 10^{16}$ atoms/cm^3. This low oxygen silicon source has been shown[19] to extend considerably the pressure and temperature ranges within which epitaxy may be achieved. After degreasing, the charges were etched for 5 mins. in CP_4A in a Teflon beaker, rinsed in deionized water, blown dry in helium and placed, employing Teflon tweezers, in the crucible of the evaporation unit.

3.2.3 Substrates

The substrates employed in the homoepitaxial depositions were phosphorus or boron doped Czochralski grown Syton polished wafers obtained

from the Monsanto company. These were chemically cleaned in quartz beakers employing one of the two following cleaning procedures.

Procedure (1)

step (1) D.I. Rinse

step (2) 10 mins. in $2H_2SO_4$-1 H_2O_2 at 70°C followed by D.I. rinse

step (3) 10 mins. in $5H_2O$-$1H_2O_2$-1HCl at 70°C followed by D.I. rinse

step (4) 10 mins. in 20 H_2O-1 HF at 70°C followed by D.I. rinse

Procedure (2)

step (1) 30 sec. dip in concentrated HF acid held in a Teflon beaker.

After either of these procedures the samples were removed from the final rinse employing Teflon tweezers and were blown dry in helium before placing in the vacuum system. Pumping was commenced within ∿2 mins. of removing the samples from the final rinse.

The substrates employed in depositions on SiO_2 were 2 ohm-cm N-type silicon wafers, similar to those described above, on which ∿8000 Å of SiO_2 had been grown by wet thermal oxidation. The oxidation process consisted of heating the substrates for 75 mins. at 1175°C in an ambient consisting of N_2 which had been passed at 1 litre/min. through water held at 95°C. The oxidized wafers were cleaned by steps (1), (2) and (3) of procedure (1) above followed by a 5 sec. dip in 20 H_2O-1HF at room temperature and a deionized water rinse. The samples were again blown dry in helium, placed in the system and pumped on within 2 mins. of removal from the final rinse. The deionized water employed in rinsing both the evaporation charges and the substrates had a resistivity of 18 mΩ cm and was obtained from a Millipore "Super-Q" system.

3.2.4 Substrate heater

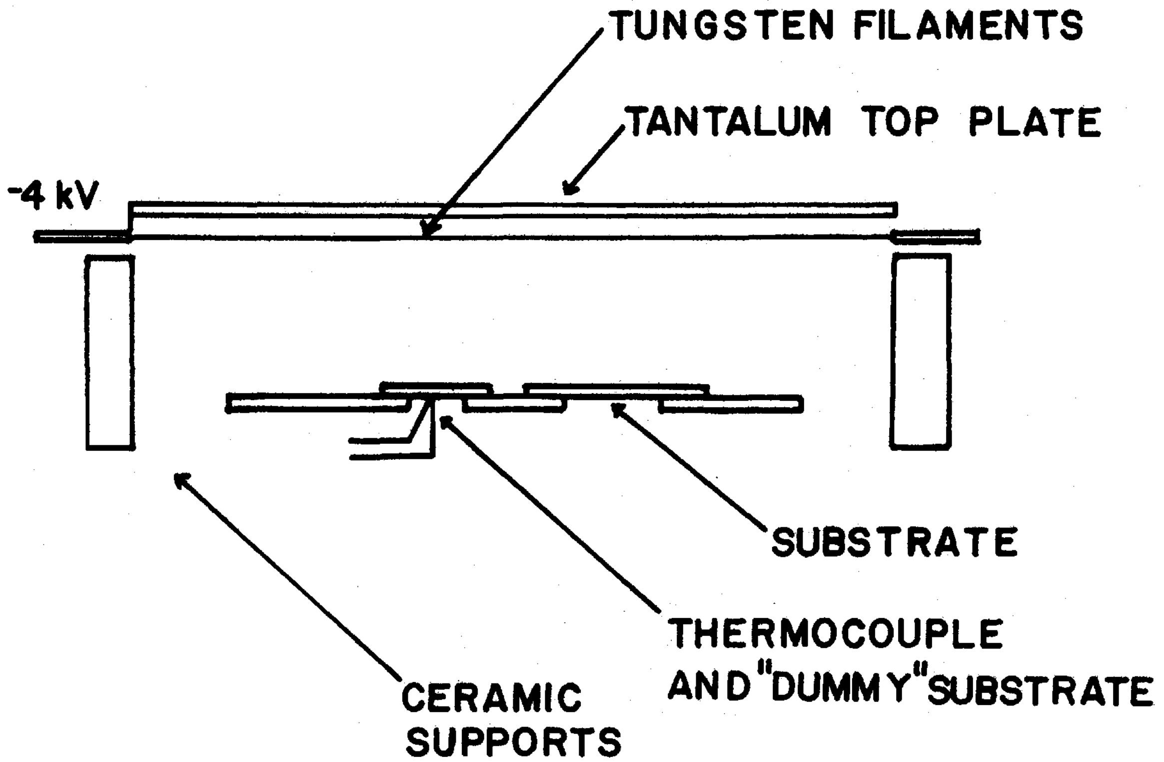
The substrates were heated by 4 kV electron bombardment of the back surface. A schematic of the substrate heater is shown in figure (3-2). High temperature portions of the heater were fabricated from tantalum having a nominal 99.99% purity. Substrate temperatures were monitored employing a Pt/Pt 13% Rh thermocouple fastened to a second silicon slice held in an identical position to that of the substrate. The thermocouple was initially held against the dummy substrate by means of a tungsten spring clip. After fabrication and etch cleaning in CP_4-A, the heater assembly and dummy substrate were placed in the system and heated to $\sim$900°C for 10 mins. in high vacuum. This heat treatment served both to fuse the thermocouple to the dummy substrate and to further clean that portion of the base plate which was subsequently in contact with the real substrate.

Comparisons of substrate temperature measured directly using a Milletron two colour comparator pyrometer with the values given by the thermocouple indicated an accuracy of $\pm$3% in the measurement of substrate temperature.

The heater assemblies were replaced after each series of 10-15 runs or earlier if carry-over doping was a possibility.

3.2.5 Doping

The evaporated silicon layers were doped by the partial decomposition of a stream of suitable doping gas directed at the substrate surface during deposition. The doping gases (Matheson doping gas grade) were leaked into the vacuum system without further purification through ultra high vacuum leak valves and directed at the substrate through a 1/4 inch stainless steel tube whose end was located 3 inches from the silicon surface. Uniformity



HIGH VOLTAGE 4kV, 0-.5A.
FILAMENT 0-5V, 0-20A.

Fig.(3-2) Schematic of substrate heater

of doping was such that carrier concentrations measured at different points in the deposited layers differed by not more than ±20%. The leak valves and stainless steel line which carried the doping gases to the system were pumped to <10^{-8} torr before filling with these gases.

3.3 Evaporation procedure

An abbreviated schematic of the vacuum evaporation gas-doping system is shown in figure (3-3).Figure (3-4) shows a photograph of the top plate. The deposition procedure in general comprised the following steps.

(1) the system was pumped to the high vacuum or ultra high vacuum base pressure.

(2) the substrate was heated to the evaporation temperature for several minutes to outgas and was then allowed to cool.

(3) the substrate was covered by a shutter and the evaporation charge heated until evaporation was detected. The charge was then allowed to cool.

(4) when the system had again attained base pressure the substrate was re-heated to the evaporation temperature.

(5) evaporation was re-initiated and brought to the desired rate

(6) the doping gas was leaked into the system to the desired pressure.

(7) the shutter was removed and a film of the desired thickness deposited.

(8) the shutter was replaced and the evaporation, gas-leak and substrate heating terminated.

In the course of the evaporation,typical system pressures were 2×10^{-7} torr and 5×10^{-9} torr for the high and ultra high vacuum modes

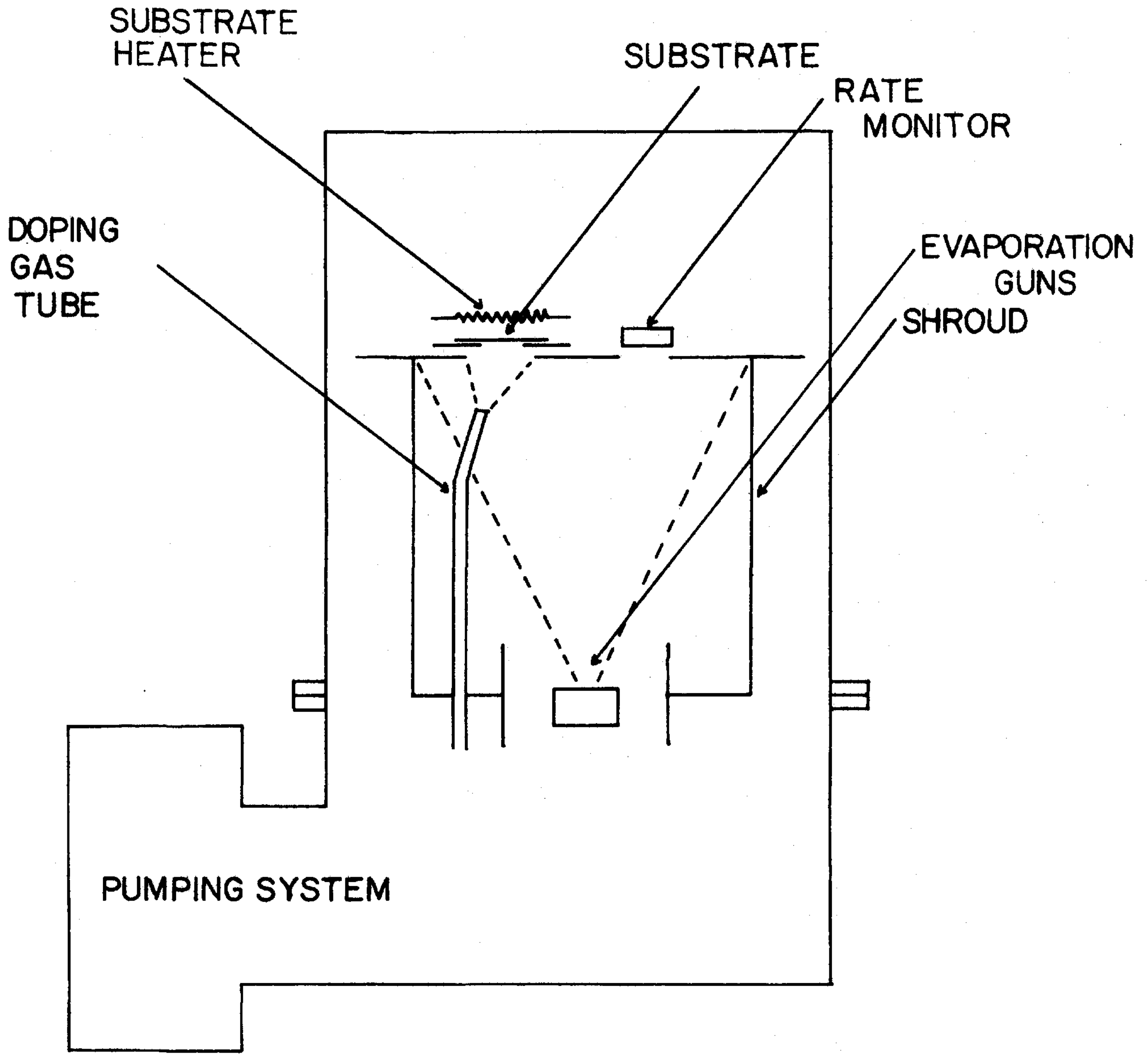


Fig.(3-3) Abbreviated schematic diagram of the evaporation system with gas-doping capability

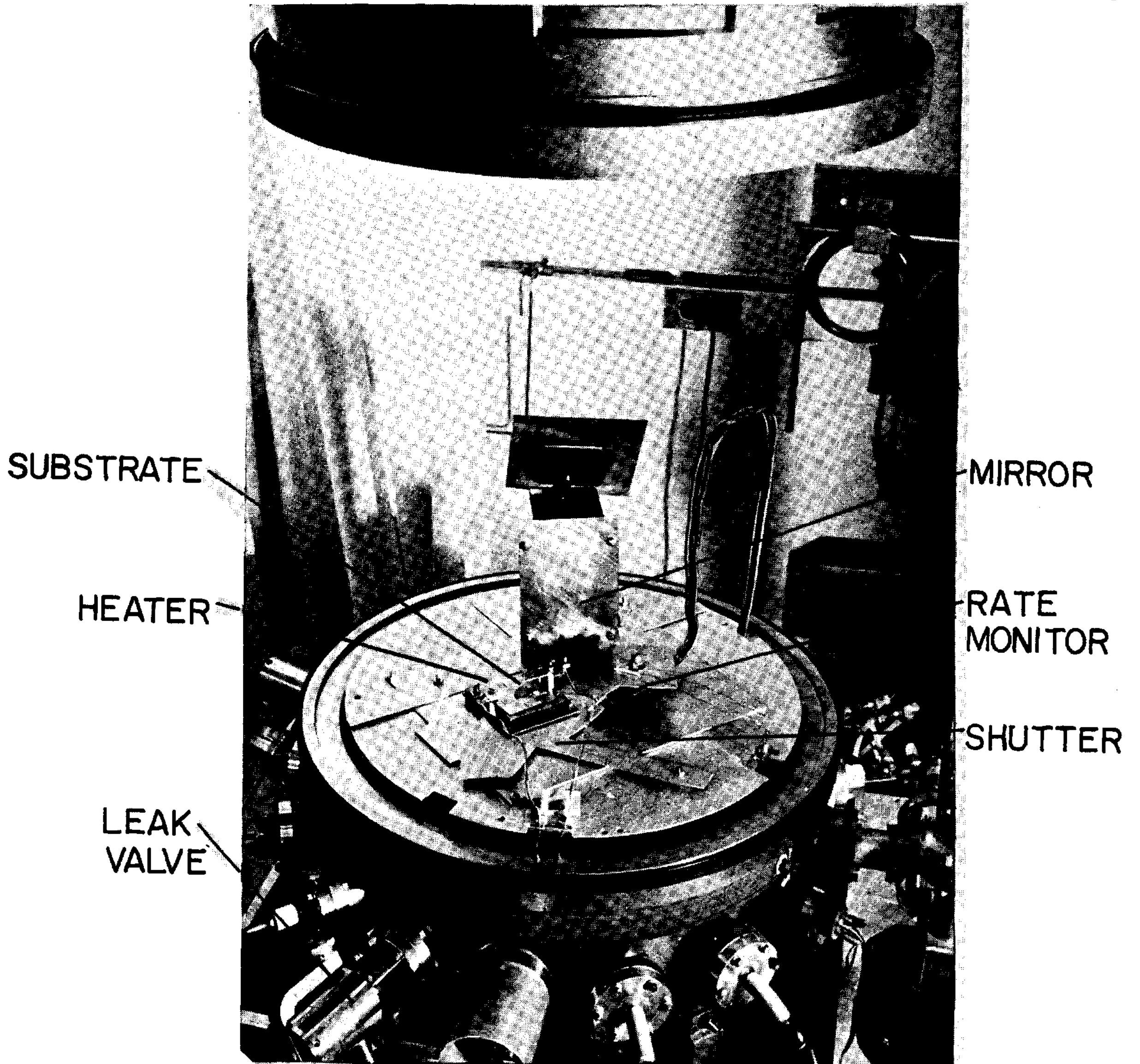


Fig. (3-4): Top plate of stainless steel shroud.

respectively. The principal residual gas concentrations detected in the system during evaporation are illustrated in table (3-2).

Table (3-2)

Concentrations of Principal Residual Gases Present During Evaporation in High Vacuum and Ultra High Vacuum Modes

Mode	Total Pressure Torr	H^+ and H^{++}	N_2^+ and CO^+	O_2^+	OH^+ and HOH^+	Other
Hi. Vac.	1.5×10^{-7}	57%	9%	6%	16%	12%
Ultra Hi.Vac.	5×10^{-9}	70%	8%	10%	2%	10%

CHAPTER IV

HOMOEPITAXIAL GROWTH OF SILICON THIN FILMS BY VACUUM DEPOSITION

4.1 Introduction

Silicon semiconductor devices are, in general, fabricated by such techniques as diffusion[20] or ion-implantation[21] where the impurity atoms necessary for device operation are injected through the surface of the solid-silicon host. The range of impurity profiles which may be produced by these techniques and are thus available for device design is intrinsically limited by the corresponding injection process. In contrast, deposition-doping techniques where both the host semiconductor and the electrically active impurity species are simultaneously deposited onto a suitable substrate offer, in principle, an arbitrary control of impurity profile. However, practical limitations, as outlined in chapter (1), have restricted the application of deposition-doping techniques. While chemical vapor epitaxial deposition is widely employed in the device industry for the production of doped single crystal silicon layers, the high processing temperatures required in the production of such layers results in a considerable redistribution of doping impurity atoms and hence in a partial loss of profile control. While direct device fabrication by chemical vapor deposition has been reported, the technique is generally[20] employed in the production of high resistivity layers for subsequent doping by diffusion or implantation.

Vacuum epitaxial deposition techniques, while possessing many potential advantages as outlined in chapter (1)have not, because of their practical

limitations, found application in device fabrication. In this chapter, the published studies of the growth of vacuum deposited homoepitaxial silicon films are reviewed. The feasibility of obtaining device quality single crystal silicon films by vacuum deposition without employing some of the restrictive conditions of previous investigations is experimentally considered.

4.2 Review

4.2.1 Introduction

For practical application to device fabrication vacuum epitaxial growth techniques must be capable of producing single crystal semiconductor layers whose electrical properties are comparable with those exhibited by bulk single crystal silicon. The presence in significant quantities of electrically active structural defects or of unwanted impurity atoms will result in a deterioration in the electrical characteristics of semiconductor devices fabricated in such layers.

While no specific numbers may be assigned to the stacking fault and dislocation densities which may be tolerated in epitaxial layers for device applications,early work[22] employing chemical vapor techniques produced films having typical stacking fault densities of $10^6/cm^2$. State of the art[23] chemically deposited films contain stacking fault and dislocation densities which are typically of the order of $10/cm^2$ and $500/cm^2$ respectively. The commercially available polished silicon substrates normally employed in epitaxial depositions contain dislocation densities of $\sim 10^3/cm^2$.

The use of high temperature (>900°C) processing steps in the production of vacuum epitaxial layers is undesirable. Atsuch high temperatures diffusion both of doping impurities and of lifetime killing[24] trapping species such as Au, Fe, Ni, etc., will be appreciable. Such diffusion

will result in "auto-doping" of the grown layer, redistribution of doping profiles in devices already present in the substrate and, a general increase in the concentration of undesirable trapping centres.

For high frequency device applications, a total layer thickness of only a few thousand angstroms may be desired. Films which are flat and continuous within a few hundred angstroms of total deposit are thus required. The potential advantages of low pressure deposition techniques for device fabrication have motivated a number of studies of homoepitaxial silicon growth in high vacuum.[19,25-33] Table (4-1) briefly summarizes some of the published data. The results will be reviewed in terms of the various experimental parameters such as vacuum conditions, substrate temperature and orientation, substrate contamination and deposition rate both from the point of view of device fabrication and from that of the growth theory outlined in chapter (2).

4.2.2 Vacuum Conditions

Early[25,28,30] investigations employing oil diffusion pumped vacuum systems having base pressures $>10^{-6}$ torr generally required substrate temperatures in excess of 1200°C to obtain single crystal deposits. Later studies[19,29,34] in oil free ultra high vacuum systems established that single crystal silicon films having a high degree of structural perfection could be obtained on silicon substrates having temperatures as low as 350°C for the <100> and 650°C for the <111> orientations respectively. The presence of residual gases in the deposition system may effect the growth processes either through a reduction in the adatom mobility as a result of collisions with non-contaminating gas molecules, or, by providing a source

Table(4-1): Survey of properties of silicon films vacuum deposited onto single crystal silicon substrates

AUTHOR AND YEAR	DEPOSITION TECHNIQUE	SUBSTRATE	VACUUM	SUBSTRATE PREP.	SUBSTRATE TEMP.	FILM CHARACTERISTICS
HALE[25](1963)	Electron beam and resistive filament	<111>	10^{-5}(oil)	Argon sputter	1150°C	single crystal, defects not examined
HANDELMAN[26] POVILONIS(1964)	Sublimation	<111>	$<1\times10^{-8}$ (ion-pump)		1050°C	single crystal, defects $5\times10^{5}/cm^{2}$
WIDMER[27](1964)	Resistive filament	<111>	10^{-10} (oil-free)	preheat at >1000°C for 3 mins.	800°C	"perfect" single crystal
					550°C	$>10^{7}$ defects/cm^{2}
				above + pre-evaporation at >1000°C	550°C	"perfect" single crystal
BOOKER[28] UNVALA(1964)	Electron beam	<111> and <100>	10^{6}(oil)		1200°C	Rate / Defects
						<.5µ/min $10^{12}/cm^{2}$
						.5-1µ/min $10^{7}/cm^{2}$
						>1µ/min "perfect"
JONA[29](1966)		<111>	$2\text{-}5\times10^{-10}$	annealed to Si{111}7 by LEED	420°C	"perfect" by LEED
		<100>			350°C	
THOMAS[30](1966)	Electron beam	<111>	$<10^{-6}$(oil)	Thermal anneal	1100-1200°C	single crystal with defects
					<800°C	polycrystalline
WEISBERG[19] (1967)	Electron beam	<111>	$2\text{-}5\times10^{-8}$	none	450°C	single crystal, defects
		<100>		predeposition at 830°C	380°C	not examined
ABBINK et al.[31] (1968)	Electron beam	<111>	4×10^{-9} ion-pump	900°C for 1 hour	800°C	single crystal growth pinned at SiC particles having density $1.5\times10^{8}/cm^{2}$
KUZNETSOV[32] POSTNIKOV (1969)	Sublimation			1 hour at 1200°C	830-1130°C	single crystal, defects $3\times10^{4}/cm^{2}$
THOMAS[33] FRANCOMBE(1971)	Sublimation	<111>	10^{-10}	1200°C for several mins.		single crystal with defects
					700°C	$\sim10^{7}/cm^{2}$
					800°C	$\sim10^{6}/cm^{2}$
ibid.[34](1968)		<111>			400°C	numerous faults
					650°C	device quality
		<100>			350°C	device quality
CULLIS[35] BOOKER(1971)	Sublimation	<111>	10^{-10}-10^{-8}	preheat 1250°C 10 mins.	750-1000°C	single crystal growth by steps, pinning particles $10^{8}/cm^{2}$
				none		growth by centres

of contaminating impurity atoms. Since detailed studies[36] have indicated the epitaxial silicon growth process to be highly sensitive to relatively small concentrations of hydrocarbon compounds, the substantial reduction in the epitaxial growth temperature in oil free systems may be attributed to the elimination of hydrocarbon contamination by the vacuum ambient. No systematic studies have been reported of the sensitivity of the growth process to such species as H_2, CO, CO_2 and water vapor which comprise the principal residual gases in ion-pumped vacuum systems. The partial pressures of such gases which may be tolerated in these systems without appreciable interference with the crystalline perfection of the deposited layers are thus unknown.

Since ultra high vacuum conditions are both costly to produce and difficult to maintain in a production facility, it is desirable that homo-epitaxial layers having the required degree of structural perfection may be produced at as a high a system pressure as is possible.

4.2.3 Substrate Temperature and Orientation

Homoepitaxial growth of single crystal silicon films by vacuum deposition has been reported for substrate temperatures as low as ∿350°C for the Si<100> and ∿650°C for the Si<111> orientations respectively[19,29,34]. Differences in the epitaxial growth temperature for the two substrate orientations may probably be attributed to differences in the arrangement and spacing of surface atoms. Such differences in turn give rise to differences in the surface binding and hence to differences in the adatom mobility. To minimize diffusion both of conventional dopants and of lifetime killing trapping centres during device fabrication, it is desirable that the growth temperature should be

as low as possible. The growth temperatures of 350°C and 650°C reported for epitaxial growth by vacuum deposition are some 150°C to 450°C lower than the lowest growth temperatures currently reported for homoepitaxial films deposited by chemical techniques[37]. Furthermore, such low growth temperatures compare favourably with those of >900°C and >650°C employed in the fabrication of silicon devices by conventional diffusion[20] and by ion-implantation[21] respectively.

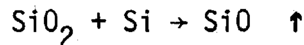
4.2.4 Substrate Preparation and Growth Processes

As seen from table (4-1), in all cases where single crystal silicon films have been obtained at low substrate temperatures, severe heat treatment (typically 1200°C for 10 mins.) of the substrate has been employed prior to deposition. The objective of this high temperature substrate heat treatment has been to remove contaminating impurities from the substrate surface. Two principal sources of contamination have been identified and a variety of other impurity species are probably present in concentrations below the detection limit of present techniques.

Silicon Dioxide

While chemical cleaning of the silicon substrates prior to placing in the vacuum system employs a hydrofluoric acid etch to remove surface oxide, some subsequent exposure to the atmosphere is inevitable. During this exposure 7-15Å of amorphous silicon dioxide will form on the substrate surface.[38] Since the presence of this amorphous overlayer will preclude the formation of single crystal films, the surface oxide must be removed prior to growth. Lander and Morrison[39] have shown that the surface oxide may be removed by heating for $\sim 10^3$ secs at 900°C in high vacuum. They have established that removal

takes place through the reaction:



$$SiO_2 + Si \rightarrow SiO \uparrow$$

at the oxide silicon interface. Heat-treatment of the substrate for at least this time and temperature has thus been employed in most previous studies prior to deposition.

Joyce et al.[14] have suggested that, in the absence of high temperature heat-treatment, an equivalent removal reaction may take place between the depositing silicon and the residual oxide. They have attributed the time delay observed between the first exposure of a heated substrate to a silane beam and, the commencement of observable nucleation, to this process. The kinetics of the silicon-surface oxide reaction have been studied by Bennett and Gale[40] who have obtained activation energies of .8 eV and 4 eV for the vapor-oxide and substrate-oxide reactions respectively.

Carbon Containing Compounds

Auger studies performed by a number of authors[8,41] have established the presence of carbon containing compounds on the surface of silicon wafers cleaned by conventional chemical techniques. Whether these carbon containing compounds originate from the cleaning reagents employed or, from atmospheric exposure is not known. Such compounds result both in fixed and in mobile impurity species which interfere with homoepitaxial silicon growth.

a) Electron microscope studies[31,42] have established the presence of numerous small crystallites on the surface of silicon substrates heated to temperatures in excess of 800°C in ultra high vacuum. HEED investigations have established that these crystallites are in fact silicon carbide. Both the size and the number density of the SiC crystallites are observed

to increase as the substrate temperature is raised above 800°C. At 1200°C the SiC is observed to disappear presumably as a result of dissolution and subsequent carbon diffusion into the bulk silicon substrate.

The carbon content of the SiC crystallites is thought[36,42] to originate from hydrocarbon compounds adsorbed on the substrate surface. The decomposition of these compounds produces a high carbon supersaturation with resultant precipitation of SiC at temperatures in excess of 800°C. The possibility that surface carbon might originate from the decomposition of CO or CO_2 present in the vacuum system has been discounted by Joyce et al.[36] who have shown that carbide free silicon surfaces obtained by high temperature annealing (>1200°C) remained carbon free even if subsequently exposed to relatively high pressures of these gases. Typical SiC particle concentrations of $10^8/cm^2$ for particles having diameters of approximately 200Å have been reported.[31]

The presence of fixed silicon carbide particles seriously interferes with the growth of single crystal films. Pinning of growth steps by these crystallites results in the production of stacking faults in the epitaxial layers. In addition, the particles, although small (∿200Å), may not become covered until the average thickness of the deposit reaches many thousand angstroms.[31] Silicon substrates must thus, if initially heated to 900°C to remove surface oxide, be further heated to 1200°C to remove silicon carbide contamination.

b) Both initial and subsequent growth on "clean" silicon surfaces held at ∿800°C have been shown[31] to proceed by the motion of monolayer steps across the silicon surface. This "step-flow" mode of growth corresponds to

that considered by Burton et al.[4] and described in chapter (2). On substrates which have not been subjected to high temperature cleaning, growth has been observed to take place by the formation of discrete three-dimensional nucleation centres.[14,31,35] These grow in size and finally coalesce to form a continuous film. Further growth then proceeds by step motion.

The formation of three-dimensional nucleation centres on non heat-treated substrates has been attributed[36] to the presence of mobile impurity species, the precise mechanism being unknown. On the basis of the classical nucleation model such impurities may lower the free energy of the critical cluster enabling nucleation to take place at a lower super-saturation than would be the case if no impurities were present. In the step-flow model, impurities may inhibit the capture of adatoms by growth steps by the process of stabilizing kinks. Adatom concentrations on the plateau regions are thus increased and may attain a value sufficient to permit spontaneous nucleation. However, the three-dimensional structure of the growth islands observed on non heat-treated substrates contrasts with the structures predicted by nucleation theory whose height should never exceed a few monolayers.

Joyce et al.[36] have studied the nucleation of films deposited at 800°C as a function of predeposition heat-treatment temperatures from 800°C to >1200°C. They observed that while the number density of nucleation centres depended only on substrate temperature and deposition rate as predicted by nucleation theory, their shape and height to width ratio varied widely with predeposition heat-treatment temperature. For depositions on heat-treated substrates, the growth centres exhibited a regular structure (triangular on <111> substrates) and a height to width ratio approaching unity. As the temperature of the predeposition heat-

treatment was increased, the growth centres become progressively thinner and less regular. In the limit, after predeposition heat treatment at 1200°C, no discrete centres were observed and growth was presumed to take place by monolayer propagation. Similar transitions from three-dimensional island growth on contaminated surfaces to monolayer growth on clean surfaces have been observed in a variety of silicon deposition systems.[31,35] Joyce et al.[36] have attributed the formation of three-dimensional island centres to the presence of mobile carbon containing species, probably hydrocarbons, on the substrate surface. High temperature (>1200°C) heat treatment again has the effect of dissolving the surface carbon and of allowing this to diffuse into the substrate.

Other Impurities

A variety of other impurities are probably present on the surface of the silicon substrates in concentrations below the limit of Auger techniques.[8] Since these have not been identified, their role in the growth processes is difficult to assess. Thomas and Francombe[33] have observed stacking fault densities of $10^6/cm^2$ in homoepitaxial silicon layers deposited onto silicon substrates which had been preheated at 1200°C for 5 mins. in ultra high vacuum and were thus presumably free of both SiO_2 and carbon contamination. The presence of these stacking faults was attributed to the precipitation of fast diffusing low solubility lifetime killing impurities such as Cu, Au, Fe, Ni, Zn, etc. at the substrate surface. Since the diffusion and resultant precipitation of these impurities will be much enhanced by high temperature predeposition heat treatment, such treatments may be expected to produce an increase in the number of stacking faults arising through this mechanism.

4.2.5 Deposition Rate

Several studies have found the crystalline perfection observed in vacuum deposited homoepitaxial silicon films to be a function of deposition rate. Booker and Unvala[28] found that the stacking fault densities in films evaporated in an oil pumped system onto substrates having temperatures of 1200°C decreased with increasing deposition rate over the range 5 Å/sec to 20 Å/sec. In contrast, Thomas and Francombe[33] observed that the stacking fault densities in films sublimed in ultra high vacuum onto predeposition heat-treated substrates at 520°C increased with deposition rate over the range $\sim 3 \times 10^{-2}$ Å/sec to ∿3 Å/sec. and were approximately constant for higher deposition rates. Booker and Unvala[28] attributed the increase in crystalline perfection in their deposited layers to an increased "gettering" effect by the evaporating silicon at higher rates of deposition and hence to a reduction in system pressure. Thomas and Francombe[33] attributed the decrease in crystalline perfection with increasing rate (and decreasing substrate temperature) to an increase in nucleation at microprecipitates formed from fast diffusing impurities.

The nucleation and growth theory outlined in chapter (2) predicts both an increase in the number of nucleation centres under conditions of complete condensation and, an increase in the velocity of step and centre growth, with increasing deposition rate. In addition to the explanations given above, a variety of other mechanisms may be suggested whereby an increased deposition rate may influence layer perfection. These include:

1) With an increase in the number of nucleation centres as a result of the increased deposition rate, growth proceeds on a wider front.

The net influence of a fixed concentration of mobile surface impurities may thus be reduced and an increase in layer perfection observed.

2) For increased rates of deposition, the probability that an adatom will be trapped at a lattice site which does not favour epitaxial growth will increase and a net decrease in layer perfection will thus be observed.

4.2.6 Discussion

While it has been shown that single crystal silicon films having a degree of structural perfection adequate for many device applications may be obtained by vacuum deposition onto substrates having temperatures as low as 350°C, further consideration of the processing employed in obtaining these films indicates a number of severe practical limitations.

In all cases where single crystal silicon films have been obtained at low substrate temperatures,severe heat-treatment (typically 1200°C for 10 mins.) of the substrate has been employed prior to deposition. As was previously stated, high temperature predeposition heat-treatments are most undesirable for device fabrication. At such high temperatures diffusion both of conventional dopants and of lifetime killing trapping centres is appreciable. Thomas and Francombe[34] observed that a heat treatment at 1200°C for 5 mins. in ultra high vacuum was sufficient to produce a P-type surface skin on a 2 ohm-cm N-type substrate.

Furthermore, in all cases where low temperature epitaxial growth has been reported, ultra high vacuum conditions have been employed. Such conditions are costly to produce and not practical in a large volume production facility.

The requirements both of ultra high vacuum and of high temperature predeposition heat treatment have severely limited the application of vacuum growth techniques.

4.3 Silicon Films on Non Heat-Treated Substrates

4.3.1 Introduction

In view of the obvious undesirability of severe substrate heat treatment for device applications, the properties of continuous silicon films deposited onto silicon substrates whose temperatures have at no time exceeded 800°C are of interest for device fabrication. Since no studies of the overall structural perfection of such films have been reported, such a study was conducted and is reported on in this chaper.

Since it has been demonstrated that the adatom mobility on "clean" silicon surfaces is sufficient to permit epitaxial growth on Si<111> and Si<100> substrates having temperatures as low as 650°C and 350°C respectively, the ability to deposit single crystal films onto non heat-treated substrates will depend on the degree to which such clean surfaces may be realized without preheating.

The results of Bennett and Gale[40] indicate that the rate of reaction between depositing silicon and the surface oxide is sufficient to permit removal of the latter at temperatures as low as 700°C. Extrapolation of data published by these workers to deposition rates of interest for device fabrication (>1 Å/sec) suggest that oxide removal should take place in a few seconds from silicon surfaces recently treated with HF and held at 700°C. It was observed that for silicon surfaces not treated with HF, removal times proved

approximately ten times as long under the same conditions. Since the oxide thickness on the etched and unetched surfaces differed at most by a factor of two, an increase in activation energy with a resultant decrease in the efficiency of oxide removal was indicated for thicker oxides.

If the temperature is not allowed to exceed 800°C, SiC particles will not form on the substrate surface. The carbon contamination initially present as isolated atoms on or in the SiO_2 layer or, at the substrate surface will presumably remain close to the substrate film interface during growth. Moderate concentrations ($<10^{18}/cm^3$) of isolated impurity atoms, whether carbon or one of the other species present on the silicon surface, should not seriously disrupt the silicon lattice. Such impurities may however, be expected to effect the electrical characteristics of the deposited material close to the interface region.

For depositions on non preheated substrates having temperatures as low as 700°C initial growth has been shown[40] to take place by the formation of impurity dominated three-dimensional nucleation centres. The number density of such centres has been found to be a function both of the substrate temperature and of the rate of deposition. As deposition continues, these nucleation centres grow in size and finally coalesce to form a continuous layer. Once the layer has become continuous, subsequent growth will presumably take place by the propagation of monolayer steps which originate either from misorientation, from dislocations or from spontaneous nucleation. The mean thickness of the total deposit when the film becomes continuous will depend both on the number of growth centres and on their height to width ratio. Structural imperfections in deposited layers formed by three-dimensional island

growth may be expected as a result both of misorientations between individual growth islands and, through the presence of residual impurities on the substrate surface.

4.3.2 System Parameters

Listed below are the experimental system parameters employed in the investigations being reported.

Pressure: Evaporations were performed both in the high vacuum and in the ultra high vacuum modes. The principal residual gases present in the system during the evaporation in each of these modes have been listed in table (3-2).

Substrate orientation and resistivity: Silicon wafers possessing both <111> and<100> orientations were considered. Etch pit densities in these wafers, as supplied, ranged from 1000 to $2000/cm^2$. Substrate resistivities ranged from 1 to 20 ohm-cm and were chosen to be consistent with the electrical measurements to be considered in chapters (5) and (6).

Substrate temperature: Substrate temperatures in the range 600°C to 900°C were considered. Depositions on substrates having temperatures in excess of 800°C were performed to confirm the role of the SiC crystallites reported in the literature. The lower limit in substrate temperature was set both by subsequent observations of layer perfection and by the doping technique to be described in chapter (5).

Deposition rate and total film thickness: Deposition rates considered ranged from 3 Å/sec to 25 Å/sec. The rates obtained were limited by the evaporation gun system and by the source to substrate distance (8 inches) employed. Total film thicknesses ranged from 800 Å to 10,000 Å, the maximum thickness being limited by the evaporation gun system.

Substrate preparation: The substrates were, in general, cleaned by the first procedure outlined in 3.2.3. A number of samples were considered which were cleaned by dipping for 30 secs. in concentrated HF acid and blowing dry in helium.

In addition to the above cleaning steps, a sample preparation procedure was evaluated which consisted of evaporating 50 Å of silicon onto the substrate at 775°C immediately prior to the main evaporation at a lower temperature.

Since the objective of the present investigation was to determine the suitability of homoepitaxial silicon films deposited onto non heat-treated substrates for device fabrication, an attempt was made to select values of the above parameters affording the optimum layer perfection for subsequent doping and electrical evaluation.

4.4. Experimental Results

4.4.1 Depositions on Si<111>Substrates

To investigate the crystallinity of silicon films evaporated onto non heat-treated silicon substrates having temperatures $\leq$ 800°C a series of 3000 Å films were deposited in the high vacuum mode at ∿10 Å/sec onto 10 ohm-cm P and N-type <111> silicon substrates having temperatures from 600°C to 800°C. The crystal structure of these films was analyzed employing high energy electron diffraction microscopy (HEED). Figure (4-1) shows diffraction patterns obtained at 80 kV from films deposited on substrates having temperatures of 600°C, 700°C and from the substrate material respectively. From a knowledge of the electron beam energy and of the angle of incidence it was estimated that these patterns

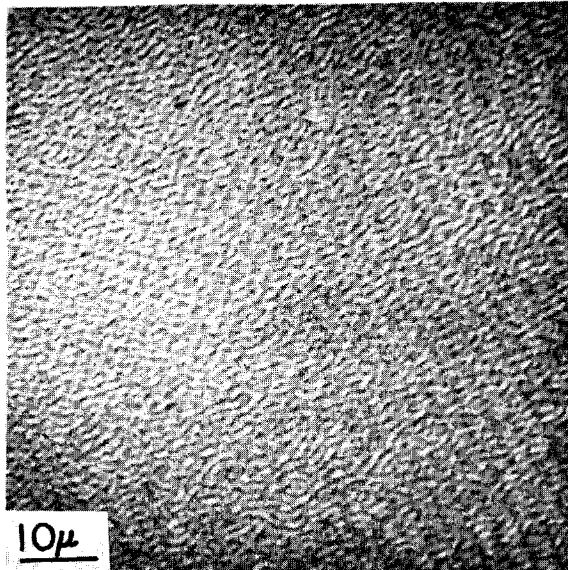
Fig. (4-1): HEED patterns obtained from 3000 Å silicon layers evaporated onto Si<111>substrates having temperatures 700°C, 600°C and from the substrate material.

were obtained from the 100 Å of deposited silicon closest to the surface of the deposited layer. In all cases patterns obtained from the evaporated silicon were characteristic of single crystal material and were identical to those obtained from the substrates.

Having established that single crystal layers could be obtained on substrates held at temperatures from 600°C to 800°C, the mean layer thickness for which continuous films were obtained was investigated. A series of films having an average thickness of 800 Å were deposited in the high vacuum mode at 10 Å/sec onto substrates having temperatures 600°C, 700°C and 800°C. These were examined employing Nomarski interference microscopy. Typical micrographs obtained from layers deposited at 700°C and 800°C are shown in figure (4-2). Deposits at 600°C were observed to be both flat and continuous to the limit of resolution. Those at 700°C were continuous but exhibited a slight surface ripple. The growth centres in the deposit at 800°C are seen to have only partially coalesced. Films evaporated onto substrates having temperatures in the range 600°C to 700°C thus appear sufficiently flat and continuous for device applications.

Figure (4-3) shows Nomarski micrographs of thick ($\sim .7\mu$) films deposited onto substrates having temperatures from 600°C to 900°C. The deposit at 700°C is seen to be totally flat and to exhibit no surface features. That at 800°C possesses a pronounced surface ripple. In the deposit at 900°C a large number of surface pits are observed. The presence of these pits may probably be attributed to the formation of SiC particles on the substrate surface at these high temperatures.

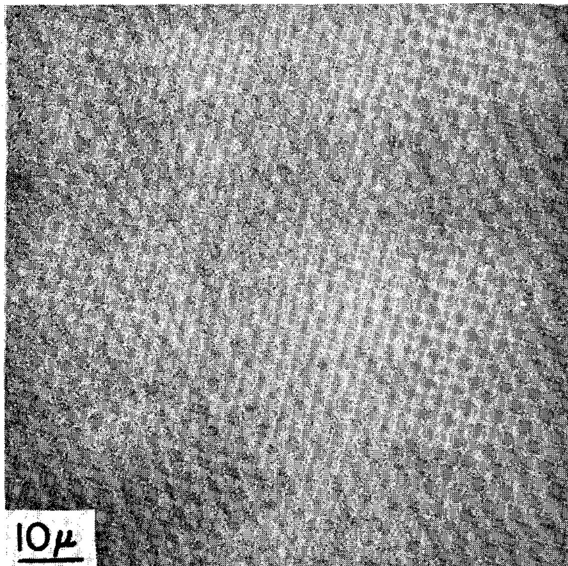
The stacking fault and dislocation densities present in films



Si <111>

800°C

800 Å

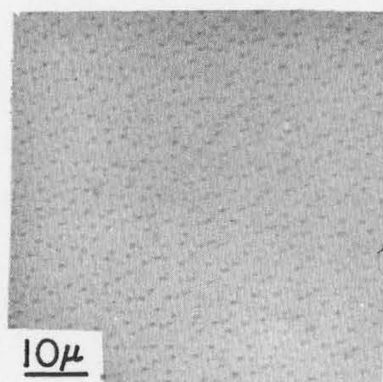


Si<111>

700°C

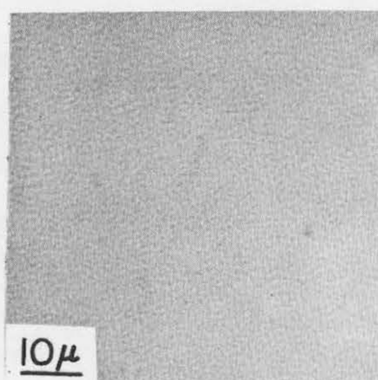
800 Å

Fig. (4-2): Nomarski micrographs obtained from thin (~800 Å) silicon films evaporated onto Si<111> substrates having temperatures 800°C and 700°C.



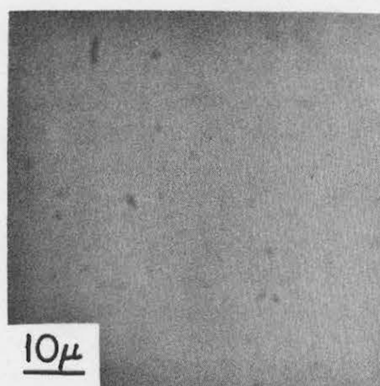
Si <111>

900 °C



Si<111>

800 °C



Si<111>

700 °C

Fig. (4-3): Nomarski micrographs obtained from thick ($\sim .7\mu$) silicon films evaporated onto Si<111> substrates having temperatures 900°C, 800°C and 700°C.

evaporated onto Si<111> substrates having temperatures in the range 600°C to 900°C were determined. Since these features are not directly observable by optical microscopy, a preferential etch which more readily attacks high index lattice planes exposed at such defects was employed. Figure (4-4) shows Nomarski micrographs obtained after etching deposited films for 10 secs in Sirtl[43] etch. As described by Lenie[44] preferential etching at dislocations intersecting a Si<111> surface produces pits which are irregular or roughly triangular and increase in size with continued exposure to the etchant. Etch pits which result from stacking faults at Si<111> surfaces are triangular with raised centres. Since such stacking faults generally originate at the substrate film interface and hence possess dimensions which are defined by the film thickness, their corresponding etch pits remain approximately the same size for reasonable etching times.

Films evaporated onto substrates having temperatures of 900°C are seen to possess a large number ($\sim 10^7/cm^2$) both of stacking faults and of irregular etch pits. The latter probably originate at the SiC pits shown in figure (4-2). The deposit at 800°C exhibits both stacking faults and dislocations having densities of approximately 10^6 and $3 \times 10^6/cm^2$ respectively. At 700°C the stacking fault densities are reduced to $\sim 5 \times 10^4/cm^2$ and the density of dislocations to $\sim 5 \times 10^5/cm^2$. At 600°C no stacking faults are observed but the dislocation densities have increased to $\sim 2 \times 10^6/cm^2$.

4.4.2 Depositions on Si<100> Substrates

The eptiaxial growth temperature for silicon films deposited onto silicon substrates possessing a <100> orientation has generally been found [19,29,34] to be lower than that for deposits on <111> substrates. For

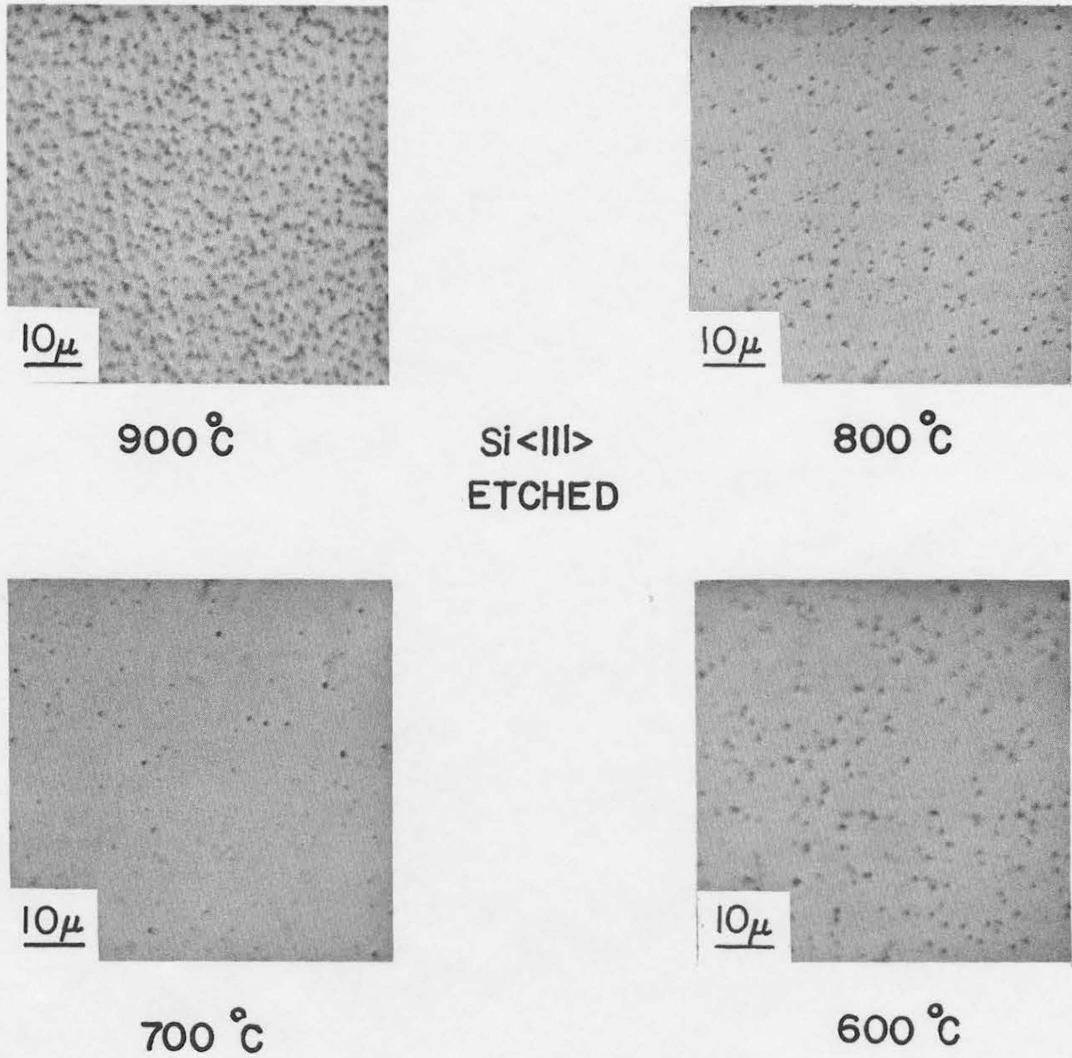


Fig. (4-4): Nomarski micrographs obtained from thick (∿.7μ) silicon films evaporated onto Si<111> substrates having temperatures 900°C, 800°C, 700°C and 600°C after 10 sec. Sirtl etch.

depositions at the same temperature, layers deposited on <100> silicon may be expected to possess a higher degree of structural perfection. A series of films were deposited in the high vacuum mode at 10 Å/sec onto Si<100> substrates having temperatures from 600°C to 800°C. Identical single crystal HEED patterns were again obtained from the substrate material and from the deposited layers. Figure (4-5a) shows a HEED pattern obtained from a 3000Å film deposited onto a Si<100> substrate having a temperature of 600°C. Figures (4-5 b,c) show Nomarski micrographs of deposits on substrates having temperatures of 700°C and 850°C. The film deposited at 700°C is seen to be totally flat and featureless. The deposit at 850°C exhibits a pitted surface similar to that shown in figure (4-3a). Figure (4-6) shows micrographs obtained from films deposited at 600°C, 700°C and 850°C after Sirtl etching for 10 sec. The deposit at 800°C is seen to possess an etch pit density of approximately $10^7/cm^2$. Those at 700°C and at 600°C exhibit a high degree of structural perfection with etch pits densities $<5 \times 10^3/cm^2$.

4.4.3 Pressure

The results reported on in the previous sections were obtained by evaporating in the high vacuum ($\sim 10^{-7}$ torr) rather than in the ultra high vacuum ($\sim 5 \times 10^{-9}$ torr) mode. To determine whether a significant improvement could be effected in the structural perfection of the deposited layers by resorting to ultra high vacuum, a number of depositions were made onto Si<111> and Si<100> substrates held at 700°C under ultra high vacuum conditions. Sirtl etch micrographs of typical layers are shown in figure (4-7a). For this substrate temperature, no significant differences were detected in the etch pit densities in the deposited layers. This relative insensitivity of the layer perfection to system pressure indicates that such

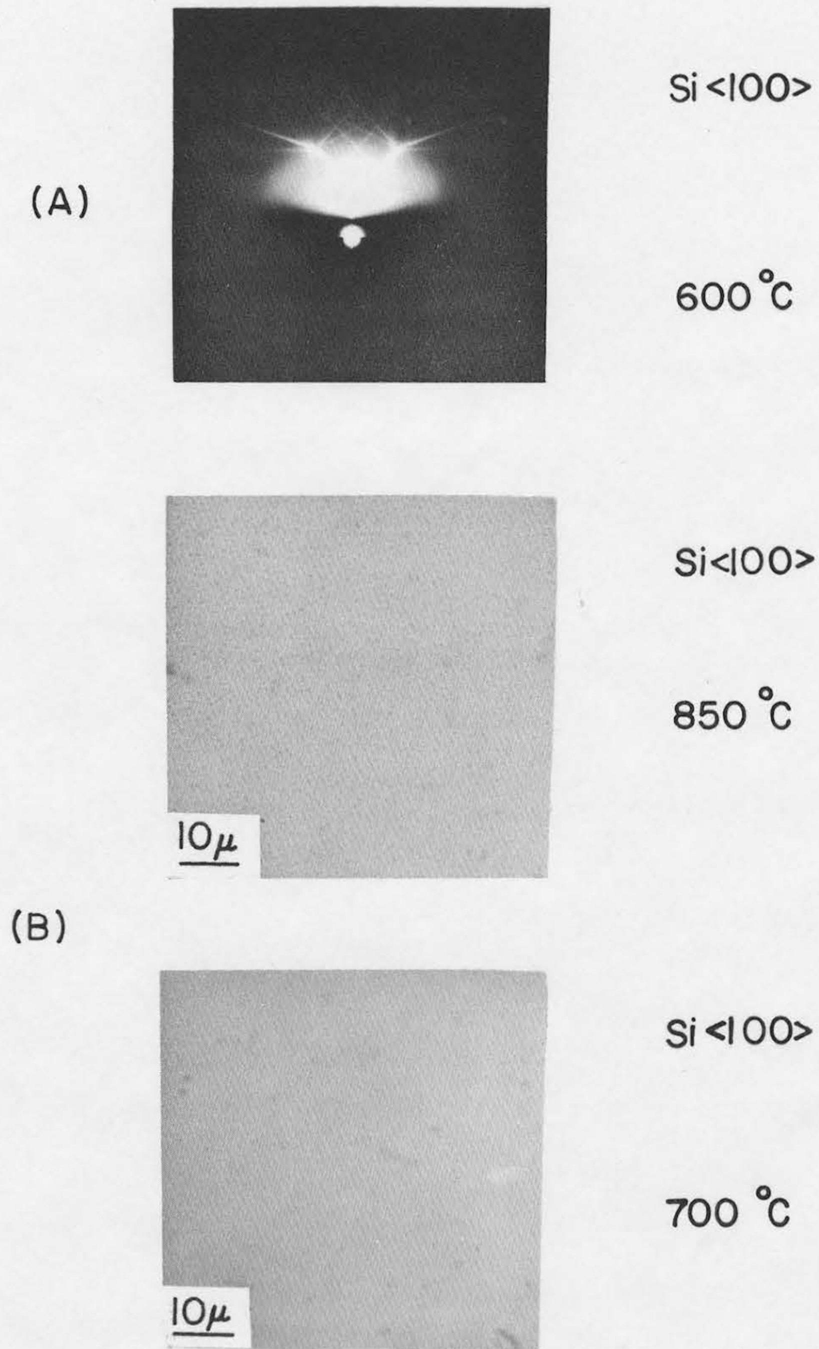
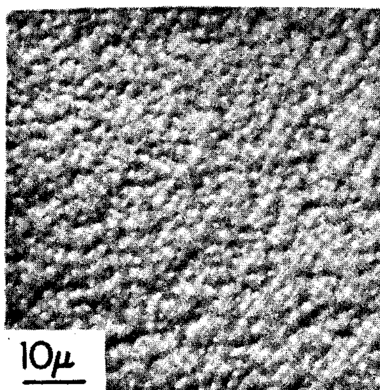


Fig. (4-5): (A) HEED pattern obtained from silicon film evaporated onto a Si<100> substrate having a temperature of 600°C.

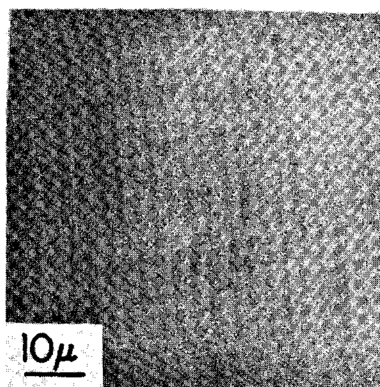
(B) Nomarski micrographs obtained from thick (∿.7μ) silicon films evaporated onto Si<100> substrates having temperatures 850°C and 700°C.



Si <100>

850°C

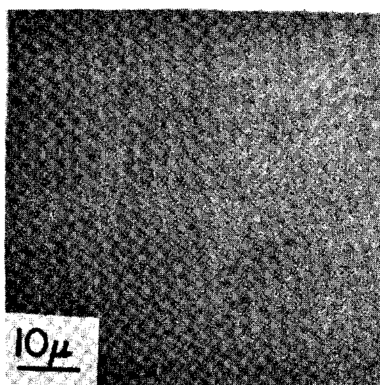
ETCHED



Si <100>

700°C

ETCHED



Si <100>

600°C

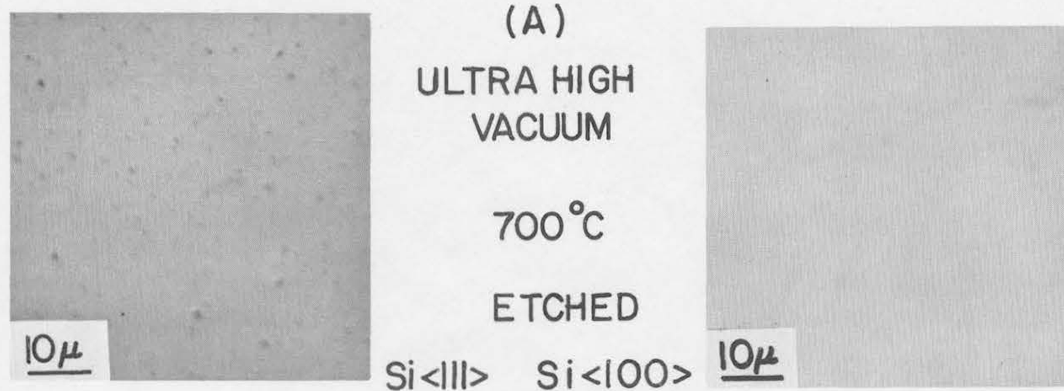
ETCHED

Fig. (4-6): Nomarski micrographs obtained from thick (∿.7μ) silicon films evaporated onto Si<100> substrates having temperatures 850°C, 700°C and 600°C. Sirtl etched 10 secs.

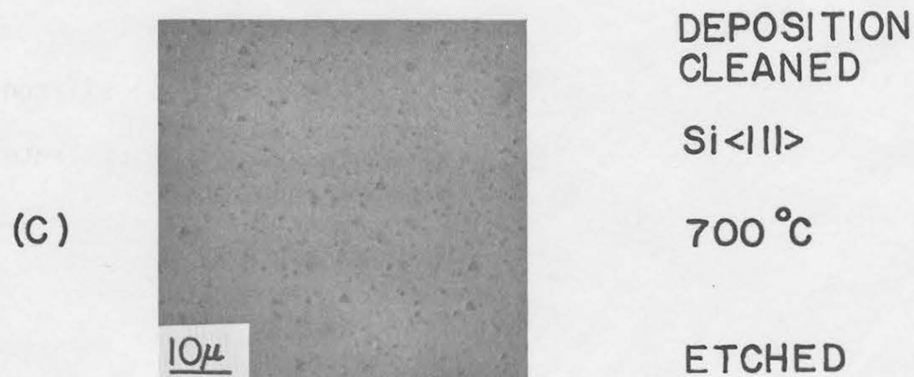
Fig.(4-7) (A) Nomarski micrographs obtained from thick ($\sim .7\mu$) silicon films evaporated in ultra high vacuum onto Si<111> and Si<100> substrates at 700°C after 10 sec. Sirtl etch

(B) Nomarski micrographs obtained from 3000 Å silicon film evaporated onto Si<111> substrate at 700°C after 5 sec. Sirtl etch.

(c) Nomarski micrograph obtained from thick ($\sim .7\mu$) silicon film evaporated onto Si<111> substrate at 700°C. Substrate "pre cleaned" by evaporating 50 Å of silicon at 775°C. Sirtl etch 10 secs.


(A)
ULTRA HIGH VACUUM
700°C
ETCHED
10μ
Si<111>
Si<100>
10μ

(B)
10μ
Si<111>
3000 Å
700°C
ETCHED


DEPOSITION CLEANED
(C)
10μ
Si<111>
700°C
ETCHED

imperfections as are detected probably originate from substrate contamination rather than from interactions with residual gases in the vacuum system.

4.4.4 Deposition Rate

As stated in 4.2.4 the structural perfection in vacuum deposited homoepitaxial layers has been found by several workers to be a function of deposition rate. To determine whether layers having a higher degree of structural perfection than those shown in figures (4-4) and (4-6) could be obtained by depositing at rates other than 10 Å/sec., a number of depositions were made onto Si<111> and Si<100> substrates held at 700°C at rates from 3 Å/sec to 25 Å/sec. While no significant differences could be detected between the samples deposited at different rates, the range which could be considered was limited. The possibility thus exists that layers having a higher degree of structural perfection than those currently deposited could be obtained by employing evaporation rates substantially higher or lower than those considered here.

4.4.5 Total Film Thickness

The possibility exists that the deposited silicon close to the substrate-film interface contains a considerably higher concentration of structural imperfections than are detected at the surface of the evaporated layer. To investigate this possibility etching microscopy studies were performed on films ranging in total thickness from 3000 Å to 10,000 Å evaporated onto Si<111> substrates at 700°C. A typical micrograph obtained from a film having a thickness of 3000 Å is shown in figure (4-7b). The etch pit density in this film is seen to be equivalent to that observed in the thick sample shown in figure (4-4). The structural perfection in the

deposited material thus appears to be uniform throughout the layer and imperfections which originate at the substrate-film interface are propagated during the entire growth.

4.4.6 Substrate Preparation

Etching-microscopy investigations showed no significant differences in the stacking fault and dislocation densities obtained in films deposited onto substrates cleaned either by the steps outlined in 3.2.3 or by the HF acid dip. Since however, the former cleaning procedure proved to be more effective in removing macroscopic impurities such as silicon dust from the substrate surface, this procedure was normally employed.

A further substrate preparation technique was evaluated which consisted of evaporating 50 Å of silicon onto the substrate at 775°C prior to the main evaporation at a lower temperature. Figure (4-7c) shows a micrograph obtained from an etched film deposited onto a Si<111> substrate which had been cleaned by this procedure. Since the stacking fault density in the deposited film is seen to be greater than that observed in the film evaporated without predeposition, the cleaning procedure is shown to be ineffective.

4.5 Discussion

On the basis of the present study, it may be concluded that continuous homoepitaxial silicon films formed by vacuum evaporation onto non heat-treated substrates having temperatures in the range 600°C to 700°C, despite their impurity dominated mode of growth, possess a degree of structural perfection which is at least comparable with that reported for layers deposited onto heat-treated substrates. The process of surface oxide removal by the impinging silicon has been shown to be sufficient to permit the growth of single crystal

films on substrates having temperatures as low as 600°C. The structural imperfections in the deposited layers have been found to be independent of vacuum pressure over the range 2×10^{-7} to 5×10^{-9} torr and may thus probably be attributed to the presence of residual impurities on the substrate surface.

While the mechanisms governing the impurity dominated three-dimensional mode of growth are obviously complex, some tentative explanations of the experimental results may be suggested on the basis both of published studies of similar systems and of the ideal growth processes considered in chapter (2).

Several studies[14,35] of the number density of three-dimensional nucleation centers on non heat-treated substrates as functions of deposition rate and substrate temperature have been reported. Both Joyce et al[14] and Cullis et al.[35] have stated that, on (111) surfaces at approximately 800°C the number density obeys an empirical relation of the form

$$N_s = CF_{1NS}^{n} \exp\left(\frac{E}{kT}\right) \tag{4-1}$$

where E = activation energy of the formation process

C, n are experimental parameters

Joyce et al. have obtained values of 1.25 and 1.81 eV and Cullis et al. .64 and 1 eV for n and E respectively. Employing the latter values, the relationship (4-1) has the approximate form of (2-17)

$$N_S = F_{1NS}^{2/3}\left(\frac{n_o}{\nu^2}\right)^{1/3} \exp[(E_2 + 2E_S)/3kT]$$

which describes the saturation density of nucleation centres with triplets

stable and no desorption. The value of $C = 1.4 \times 10^{-6}$ obtained by Cullis et al. is however about two orders of magnitude smaller than that calculated for $(\frac{n_o}{\nu^2})^{1/3}$ in (2-17) assuming reasonable values of $n_o = 10^{15}/cm^2$ and $\nu = 10^{13}/sec$. Extrapolation of the data published by Cullis et al. to the substrate temperatures and evaporation rates employed in the present investigation yields values of $\sim 9 \times 10^9$, $\sim 2 \times 10^9/cm^2$ and $\sim 5 \times 10^8/cm^2$ for the saturation densities of nucleation centres at 600°C, 700°C and 800°C respectively. The latter value is in reasonable agreement with that of $\sim 2 \times 10^8/cm^2$ obtained* from measurements on partially coalesced films as shown in figure (4-2).

Henderson et al.[8] employing low pressure silane pyrolysis on "clean" substrates found that, for a substrate temperature of 823°C only about 1/3 of silicon adatoms were incorporated into a growing layer. On the basis of the step flow model these workers calculated that adatom supersaturations as high as 10^6 were present on the substrate surface. Despite such high supersaturations the presence of significant re-evaporation was taken to imply that two-dimensional nucleation had not occurred.

To determine whether appreciable temperature dependent re-evaporation was taking place in the present experiments, comparisons were made of the deposit thickness as indicated by the crystal monitor with the final film thickness measured directly using multiple beam interferometry. For substrate temperatures from 400°C to 800°C no significant differences were detected in the proportion of the deposited silicon incorporated into the growing layer. Since, at 400°C re-evaporation may be assumed to be negligible, this must also be true at 800°C. Vapor supersaturations calculated by extrapolating the data published by Honig[16] were approximately 3×10^9 and 3×10^7 for an

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*assuming each surface "hillock" corresponds with a single nucleation centre

evaporation rate of 10 Å/sec and substrate temperatures of 600°C and 700°C respectively. Since re-evaporation was not observed, it might be suggested that for the high vapor supersaturations and reduced adatom mobilities present at the low substrate temperatures employed in the present investigations, two-dimensional nucleation did in fact occur and was the predominant mechanism for step generation.

Micrographs published by Bennett et al.[40] of three-dimensional nucleation centres formed by sublimation-deposition in high vacuum onto non heat-treated Si<111> substrates indicate that such centres possess a regular triangular structure at 900°C but are irregular at 750°C. The number density of nucleation centres at 750°C was approximately one order of magnitude greater than that at the higher temperature. If, as suggested by Joyce et al.[36] the regularity of growth centres is increased by contamination it might be concluded that such centres, being more numerous at 750°C, were less effected by the fixed concentration of surface impurities than those at the higher temperature. Should this be the case, the resultant crystalline perfection will be greater for deposits at the lower temperature as was observed in the present investigation. Furthermore, since it has been shown[45] that, for identical deposition conditions, the density of three-dimensional nucleation centres on Si<111> substrates is approximately ten times smaller than that on Si<100> substrates, a higher degree of structural perfection may be expected in the latter case.

While continuous films formed by the three-dimensional island mode of growth have been shown to possess a relatively high degree of structural perfection, suitable non destructive substrate cleaning procedures which would permit initial growth to take place by "step flow" may reasonably be expected

to result in a considerable improvement in the quality of the evaporated layers. Several potential cleaning procedures are considered in chapter (8).

4.6 Summary

The structural characteristics of homoepitaxial silicon films vacuum evaporated onto non heat-treated Si<111> and Si<100> substrates have been investigated. Single crystal films have been obtained for substrate temperatures ranging from 600°C to 900°C. Defect densities have been shown to be as low as $5 \times 10^3/cm^2$ for films deposited onto Si<100> substrates having temperatures from 600°C to 700°C. Corresponding defect densities of $5 \times 10^5/cm^2$ and $2 \times 10^6/cm^2$ have been obtained in films deposited on Si<111> substrates having temperatures of 700°C and 600°C respectively. These values compare with those of $10^6/cm^2$ reported[33] for depositions on substrates having similar temperatures which had been heat-treated at 1200°C for 10 mins. prior to deposition. Further confirmation of the relatively high degree of structural perfection obtained in these films is provided by the electrical measurements to be described in chapter (7). The defect densities in films deposited on substrates of both orientations have been shown to increase rapidly for temperatures approaching 800°C. Thin films deposited onto substrates having temperatures less than 700°C have been shown to be continuous for layer thicknesses less than 800 Å. The structural perfection obtained in the deposited layers has been found to be independent of system pressure over the range 2×10^{-7} to 5×10^{-9} torr.

CHAPTER V

GAS-DOPING OF EVAPORATED SILICON THIN FILMS

5.1 Introduction

The action of silicon semiconductor devices depends upon the presence in the silicon lattice of controlled concentrations of electrically active doping impurities. If vacuum deposition techniques are to be employed for direct device fabrication, it is necessary that such impurities be introduced in controlled concentrations into the deposited layers.

A number of techniques for incorporating doping impurities into vacuum deposited silicon layers have been reported. The simplest is by the evaporation of doped source material. However, since the silicon and dopant atoms possess widely different vapor pressures,[46] the ratio of these atoms carried-over to the deposited layer is neither the same as is present in the source material nor remains constant throughout the deposition. Handelman and Povilonis[26] and more recently Thomas and Francombe[34] have shown that 1 to 1 carry-over of dopant from sublimed source material may be obtained provided the first 1/2 to 1/3 of the total deposit is rejected. While this technique does provide reproducible doping concentrations,it lacks the flexibility required for the fabrication of multilayer device structures. Itoh et al.[47] have doped silicon layers by independent co-deposition of the dopant during evaporation. This method is however difficult to control especially if low doping concentrations are required.

Since none of the above doping techniques demonstrate either the flexibility or the degree of control required to fully exploit the potential advantages of low temperature vacuum epitaxial growth, a new technique, that of gas-doping was devised. Studies[8] of the growth of homoepitaxial silicon layers formed by the pyrolysis of silane in moderate (.15 - .02 torr) vacuums have indicated that the crystalline perfection obtained in such layers is relatively insensitive to high pressures of non-contaminating gases (notably silane) present in the deposition system. A number of the conventional silicon dopants possess gaseous compounds which are chemically similar to silane. Several of these dopant gases decompose to their elements at temperatures at or below those forming the deposition range (600°C-800°C). It appeared probable that if these doping gases were admitted into the vacuum system and were allowed to impinge on the substrate surface during deposition, partial decomposition would take place allowing a portion of the dopant to pass into the growing layer.

This chapter describes an evaluation of the gas-doping technique for the controlled incorporation of doping impurities into evaporated silicon layers. The basic objectives of the investigation were the following:

(1) to determine the effectiveness of the doping technique for reproducibly introducing controlled concentrations of doping impurities in the range applicable to device fabrication into evaporating silicon layers. The effectiveness of the technique will be determined by the proportion of doping gas molecules incident on the substrate surface which subsequently contribute free carriers to the deposited layer.

(2) to determine the degree of structural deterioration in undoped homoepitaxial films as a result of the doping process. If the doping

process is efficient, the partial pressures of the doping gases which will be required to produce doping concentrations close to their respective solid solubility limits will be small. Provided the doping impurities do not directly interfere with the silicon growth mechanism, structural deterioration as a result of the doping process should be minimal. However, if the process in inefficient and high gas pressures must be employed to obtain useful levels of doping, structural deterioration in the evaporated layers may be considerable.

(3) to investigate the feasibility of impurity profile control by the technique of vacuum evaporation combined with gas-doping.

5.2 Experimental

5.2.1 Doping gases

Arsine (AsH_3), diborane (B_2H_6) and phosphine (PH_3) were selected as potential doping gases since these decompose[48] into their respective elements at or below temperatures that formed the deposition range (600°C to 800°C). Arsine and diborane were employed in a concentration of 1% diluted in high purity hydrogen. The phosphine was nominally 100%. The apparatus employed in leaking these gases into the vacuum system and for directing them at the substrate surface during deposition has been described in chapter (3).

Subsequent measurements to be described in 5.3.5 showed that layers evaporated onto substrates having temperatures of 600°C exhibited a considerably higher degree of structural deterioration as a result of the doping process than did layers deposited onto 700°C substrates. The higher substrate temperature was thus employed in evaluations of the pressure dependence,

rate dependence and flexibility of the doping technique.

5.2.2 Preliminary investigations

Preliminary investigation of films deposited onto substrates having temperatures of 700°C showed no visible deterioration in the single crystal HEED patterns when doping gases were leaked into the system to give pressures as high as 10^{-5} torr during the evaporation. The structural perfection of doped deposited layers is considered in detail later in this chapter.

To establish the effectiveness of the doping technique a series of 3000 Å films were evaporated onto substrates having temperatures of 700°C with a variety of doping gas pressures present in the system. The doping type and concentration in the deposited material were determined from the characteristics of metal-oxide-semiconductor devices fabricated from these layers.

After removal from the system, a layer of SiO_2 having a thickness of 1000 Å was grown on the evaporated silicon by oxidation[49] in steam at 900°C. Aluminium dots were evaporated on the oxide surface and an ohmic back contact made to the sample to create a series of metal-oxide-semiconductor structures. The capacitance-voltage characteristics of these M.O.S. devices were measured at 150 kHz.

From the expressions[50]

$$C_{min} = \frac{\varepsilon_i}{d + (\frac{\varepsilon_i}{\varepsilon_s})W_M} \qquad C_{max} = \frac{\varepsilon_i}{d} \tag{5-1}$$

and

$$W_M = \left(\frac{4\varepsilon_s \, kT \ln(\frac{N_A}{n_i})}{q^2 N_A}\right)^{\frac{1}{2}} \tag{5-2}$$

d = oxide thickness

$\varepsilon_i, \varepsilon_s$ = permittivities of insulator and semiconductor

W_M = maximum depletion layer width

N_A = doping concentration in semiconductor

n_i = intrinsic electron concentration at temperature T

q,K = electronic charge and Boltzmann constant

which give the maximum and minimum high frequency capacitance of an MOS diode on a uniformly doped semiconductor layer, the doping concentration in the evaporated material was determined. The doping type of the deposited silicon was determined from the shape of the C/V characteristic. Such measurements indicated that both P and N-type films possessing carrier concentrations at least as high as $\sim 10^{18}/cm^3$ were produced when the appropriate doping gases were injected into the deposition system.

The range of doping concentrations in thin films amenable to accurate measurement by the M.O.S. technique is limited. For high doping concentrations ($>10^{18}/cm^3$) the ratio of $\frac{C_{max}}{C_{min}}$ approaches unity. For low doping concentrations the maximum depletion layer width will penetrate into the substrate material and expressions more complex than (5-1,2) must be employed.

Since MOS techniques are inaccurate, require a high temperature processing step* (900°C) and do not conveniently provide information on the transport properties in deposited layers,these were employed only in initial investigations.

5.2.3 Room temperature Hall effect and conductivity measurements

Subsequent investigations established that by masking and mesa etching P or N-type silicon films evaporated onto 10 ohm-cm substrates of

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*such a high temperature step may produce a change in both the structure and the doping density of the deposited material

the opposite doping type, rectifying junctions could be obtained. It was found that, provided carrier concentrations in the deposited layers exceeded $10^{16}/cm^3$ for N-type and $10^{17}/cm^3$ for P-type, leakage currents in the deposited diodes were less than 10^{-5} amps/cm^2 for a 1 volt reverse bias. Employing suitable masking techniques van der Pauw[51] clover leaf patterns were mesa etched in the deposited films. By applying a reverse bias these patterns could be electrically isolated from the substrate. Conductivity and Hall effect measurements performed on such isolated patterns allowed the room temperature carrier concentration, resistivity and mobility in the deposited layers to be determined. Temperature dependent Hall effect measurements performed on the evaporated layers are described in chapter (6). Both the techniques employed to delineate the van der Pauw patterns and the subsequent electrical measurements are described in appendix (A).

5.3 Experimental results

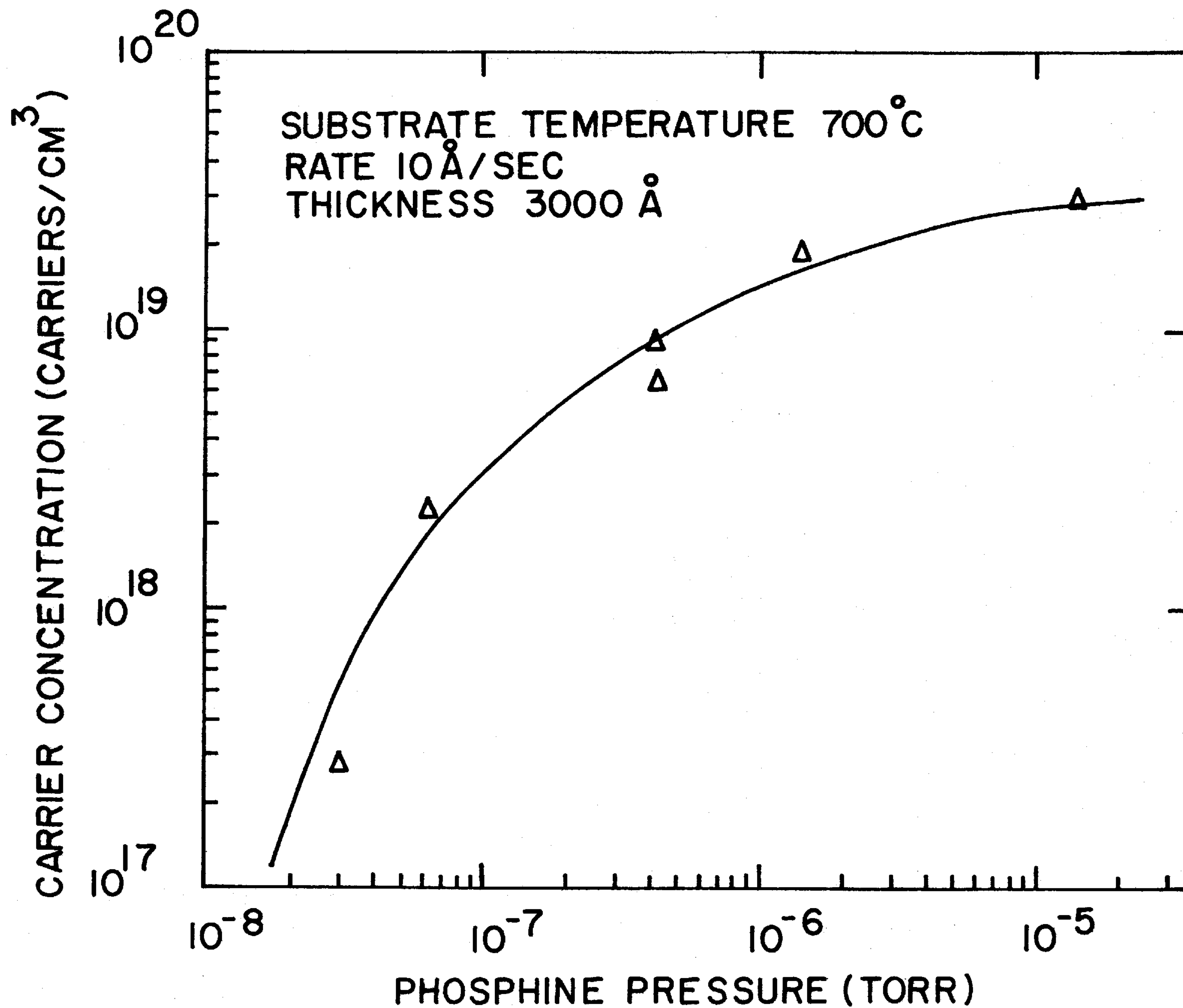
5.3.1 Introduction

To determine the effectiveness of the gas-doping technique and to characterize its dependence on system parameters, the carrier concentrations in a series of epitaxial layers deposited at a variety doping gas pressures, substrate temperatures and silicon evaporation rates were determined.

5.3.2 Doping versus gas-leak

Figures (5-1,2,3) show the carrier concentrations measured in 3000 Å phosphorus boron and arsenic doped layers evaporated at 10 Å/sec onto Si <111> substrates at 700°C as a function of doping-gas leak pressure. Since the pressure of phosphine in the system for a constant gas leak was observed to depend strongly on whether or not a layer of "fresh" silicon was present on the walls of the shroud, the phosphine pressures shown in

Fig.(5-1) Carrier concentrations in evaporated phosphorus doped silicon layers versus phosphine pressure. Substrate temperature 700°C


SUBSTRATE TEMPERATURE 700°C
RATE 10 Å/SEC
THICKNESS 3000 Å
CARRIER CONCENTRATION (CARRIERS/CM3)
10^20
10^19
10^18
10^17
10^-8
10^-7
10^-6
10^-5
PHOSPHINE PRESSURE (TORR)

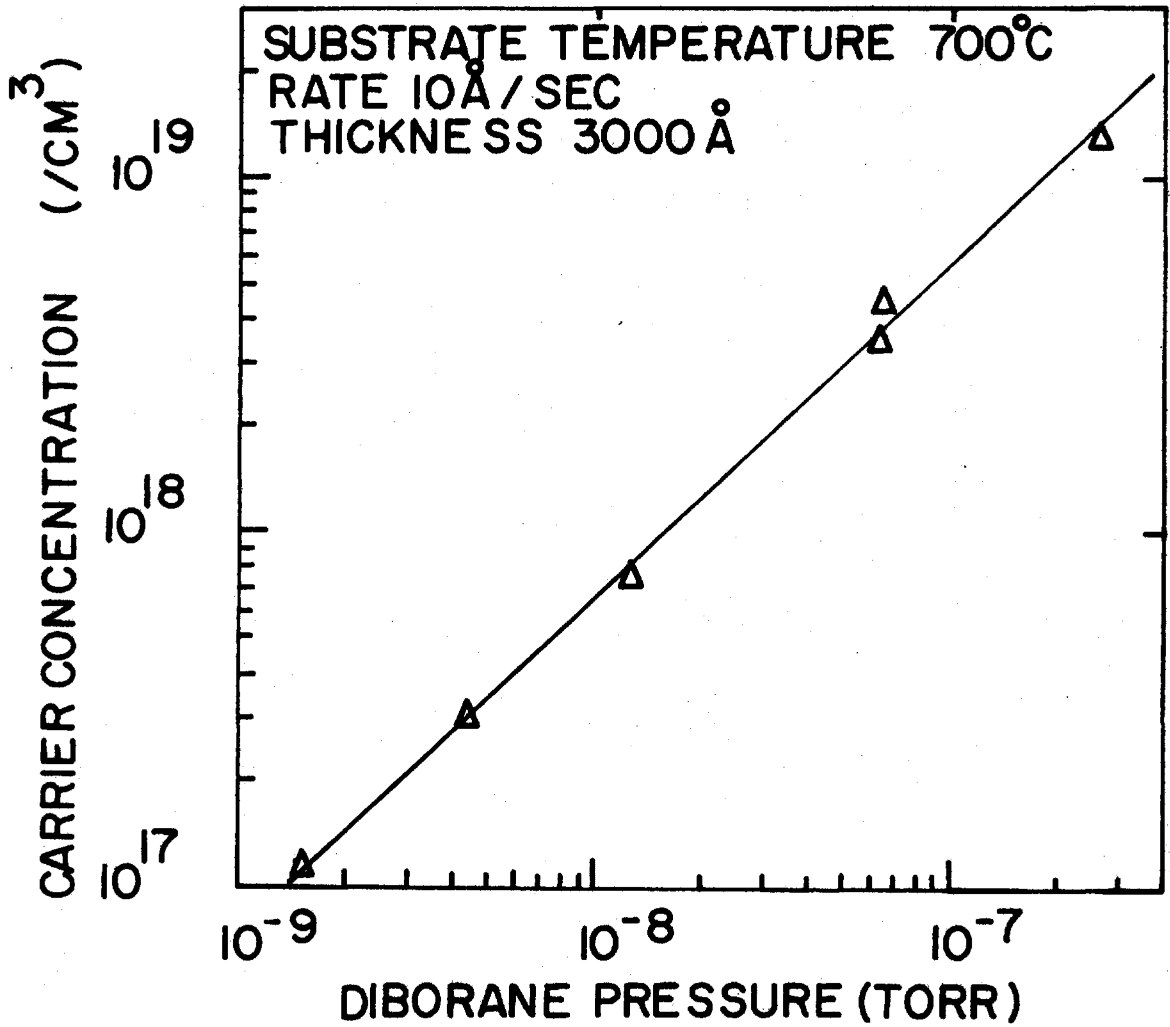


Fig.(5-2) Carrier concentrations in evaporated boron doped silicon layers versus diborane pressure. Substrate temperature 700°C

Fig.(5-3) Carrier concentrations in evaporated arsenic doped silicon layers versus arsine pressure. Substrate temperature 700°C

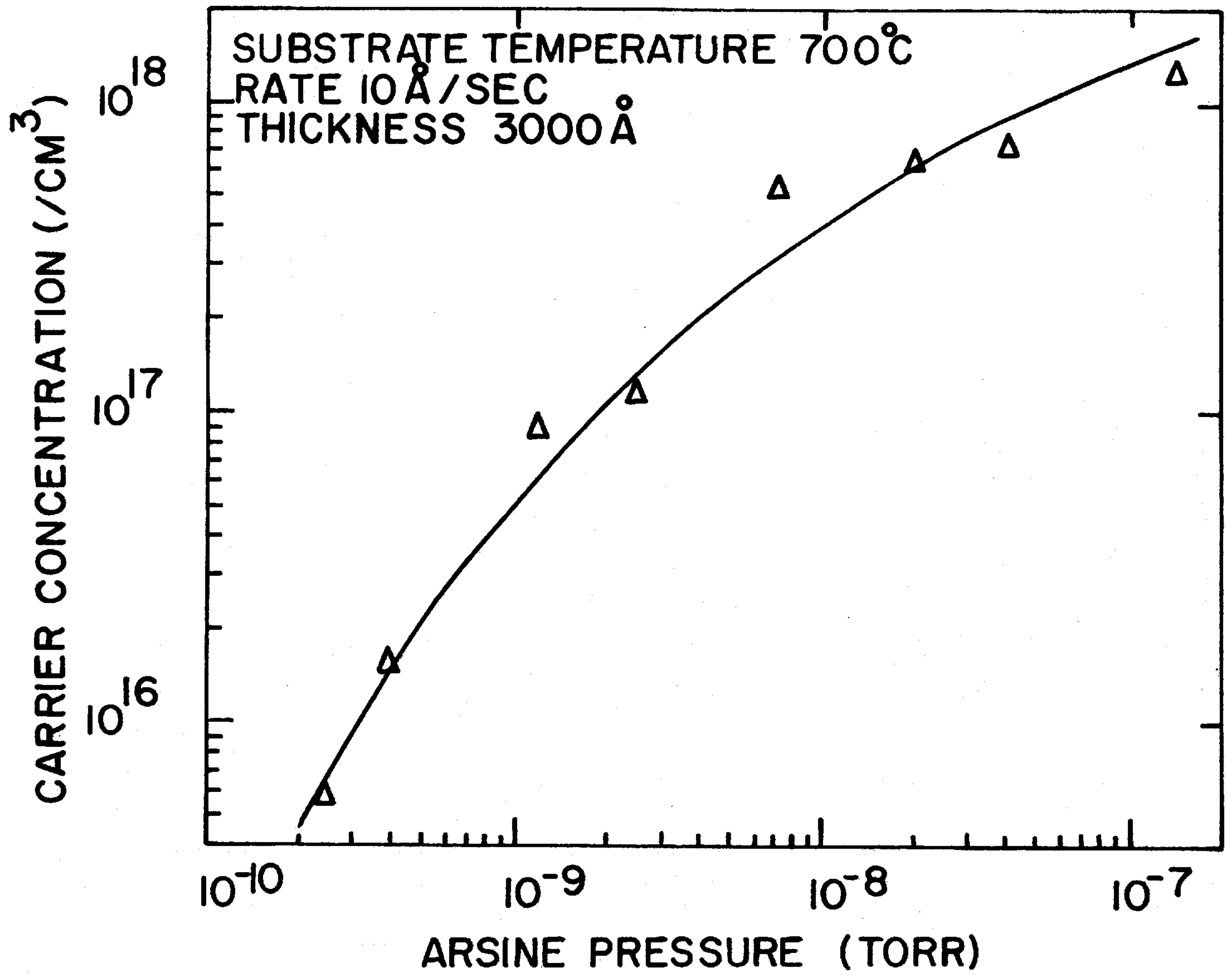

SUBSTRATE TEMPERATURE 700°C
RATE 10 Å/SEC
THICKNESS 3000 Å
CARRIER CONCENTRATION (/CM³)
10^{18}
10^{17}
10^{16}
10^{-10}
10^{-9}
10^{-8}
10^{-7}
ARSINE PRESSURE (TORR)

figure (5-1) represent the total gas leak pressure measured by the ion-gauge prior to deposition. The pressures of the 1% arsine and 1% diborane in hydrogen doping gas mixtures were found to be uneffected by silicon evaporation. Pressure values shown in figures (5-2,3) thus represent 1% of the total leak pressure of these gases measured by the ion gauge. The reduction in phosphine pressure may be attributed to an adsorption-gettering effect by the fresh silicon on the walls of the shroud. Since the pressures of the doping gas mixtures were uneffected by the depositing silicon, adsorption-gettering of hydrogen, their principal constituent, was presumably minimal.

The carrier concentration in the boron doped layers is seen to be an approximately linear function of diborane leak pressure for all the pressures and carrier concentrations considered. If, under conditions of equilibrium, we assume that the gas being leaked into the system is being removed solely by the ion-pump and, that this pump operates at its rated pumping speed (500 torr-liters/sec), the flux of doping gas molecules at the exit of the beam tube may be calculated. While the spatial distribution of molecules leaving the beam tube is not known it appears not unreasonable to assume an inverse square law dependence for the molecular flux as a function of distance from the end of this tube. Employing these assumptions the doping gas flux which impinges on the substrate surface and hence, the proportion of doping gas molecules which contribute to the electrical conduction in the deposited layer, may be calculated.

From figure (5-2) it was estimated very approximately that .003% of the diborane molecules incident on the substrate surface at 700°C resulted in the contribution of one free carrier to the deposited layer.

The proportions of arsine and phosphine incident on the surface which contribute to the free carrier concentration in the evaporated material are seen to decrease with increasing gas pressure. Percentage contributions ranged from .001% to .0003% and from .0005% to .0001% for the lowest and highest gas pressures of arsine and phosphine respectively.

It was found that the use of high phosphine pressures resulted in considerable carry-over doping from one deposition to the next. This carry-over doping could be removed only by chemically etching the shroud and by baking the complete system. Carry-over doping with either arsine or diborane was less than 5×10^{15} carriers/cm^3. Since high carry-over doping is undesirable especially in the fabrication of structures containing more than one doping type, phosphine appears less suitable for this application than do the other doping gases.

To determine whether the doping concentrations in the deposited layers originated from the initial collision of the leak gas beam with the substrate or, through some other process involving the evaporating silicon or the background gas, a number of depositions were made with the beam tube directed away from the substrate. Typical results are illustrated in table (5-1).

Table (5-1)

Carrier Concentrations in Arsenic and Phosphorus Doped Epitaxial Layers with Gas-Leak Beam Directed Towards and Away from the Substrate

Sample	Dopant gas	Gas Leak Pressure (Torr)	Direction of Gas Beam	Carrier conc. /cm^3
PH84	Phosphine	9×10^{-7}	Towards subs.	1.5×10^{19}
PH85	Phosphine	9×10^{-7}	away	9.5×10^{18}
AS67	Arsine	2×10^{-8}	Towards subs.	5×10^{17}
AS68	Arsine	2×10^{-8}	away	2.5×10^{16}

For low pressures, the carrier concentrations are seen to be greatly increased when the dopant gas beam impinges directly on the substrate surface. For high pressures sufficient background doping gas impinges on the silicon surface to saturate the growing layer whether or not the beam is directed at the substrate.

5.3.3 Doping versus temperature

A series of 3000 Å boron, arsenic and phosphorus doped layers were deposited at 10 Å/sec. on substrates having temperatures from 600°C to 800°C. The gas leak and evaporation rates were the same for each sample having the same dopant. Plots of the carrier concentrations versus substrate temperature are shown in figure (5-4). The carrier concentrations in the phosphorus and arsenic doped films are seen to increase by approximately one and two orders of magnitude respectively as the substrate temperature is reduced from 800°C to 600°C. The concentration in boron doped layers is relatively insensitive to temperature changes over the range considered. The dependence of the doping concentration on leak gas temperature was studied for boron doped films. The leak gas temperature was varied by heating or cooling the leak valve and the dopant gas source. Carrier concentrations in the deposited layers, as indicated by this experiment, were independent of leak gas temperature over the range -78°C to +150°C. However, since the doping gas molecules were required to make numerous collisions with the beam tube before reaching the substrate, their impinging energy may not have been effected by heating or cooling the doping gas source.

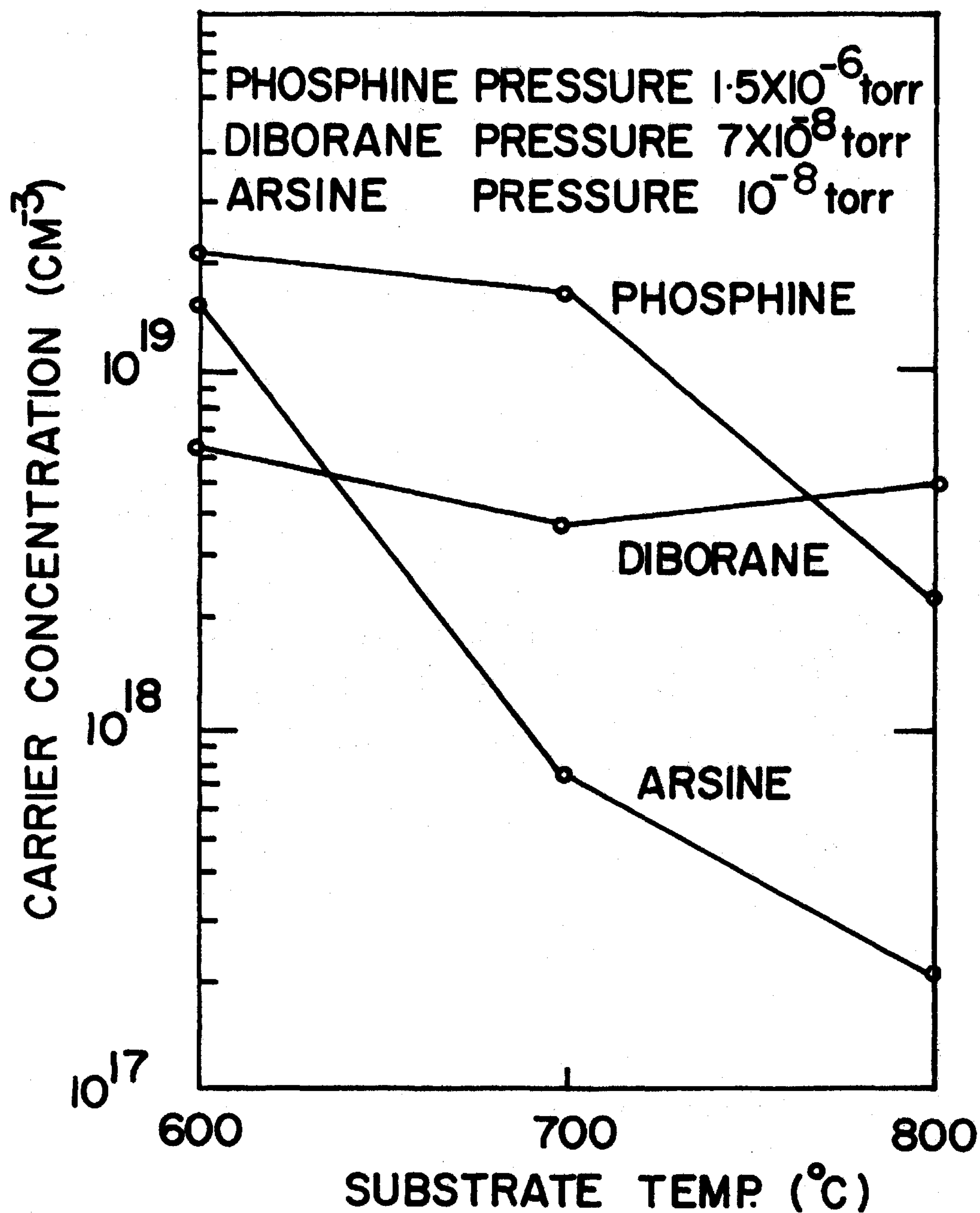


Fig.(5-4) Carrier concentrations in evaporated phosphorus, boron and arsenic doped layers versus substrate temperature

5.3.4 Doping versus rate of evaporation

Arsenic, phosphorus and boron doped layers were deposited at rates from 3 Å/sec to 20 Å/sec onto substrates having temperatures of 700°C. The doping gas pressure was constant for each of the series of samples having the same dopant. The carrier concentrations in boron doped films were found to vary approximately linearly with reciprocal deposition rate as shown in figure (5-5). In arsenic and phosphorus doped layers the measured carrier concentrations were found to be independent of deposition rate. Figure (5-6) shows the carrier concentration profile measured by anodizing and stripping techniques in a phosphorus doped layer evaporated with a constant phosphine pressure of 10^{-6} torr. The evaporation rate employed in depositing this sample was changed from 3 Å/sec to 15 Å/sec half-way through the total evaporation. As may be seen no observable change was detected in the carrier concentration throughout the layer.

5.3.5 Crystalline perfection of doped evaporated layers

To examine the structural deterioration produced in homoepitaxial silicon layers as a result of the gas doping process, the crystalline perfection in a series of relatively thick ($\sim .7\mu$) doped films was determined. Figure (5-7) shows HEED patterns obtained from films having boron or arsenic concentrations of $\sim 10^{19}/cm^3$ deposited onto Si <111> and Si <100> substrates held at 600°C. In all cases films deposited both at 600°C and at 700°C exhibited single crystal patterns identical to those obtained from the substrate. Figure (5-8) shows Nomarski micrographs obtained from heavily doped films evaporated at 700°C after Sirtl etching for 10 secs. Carrier concentrations measured in other parts of each sample are shown in

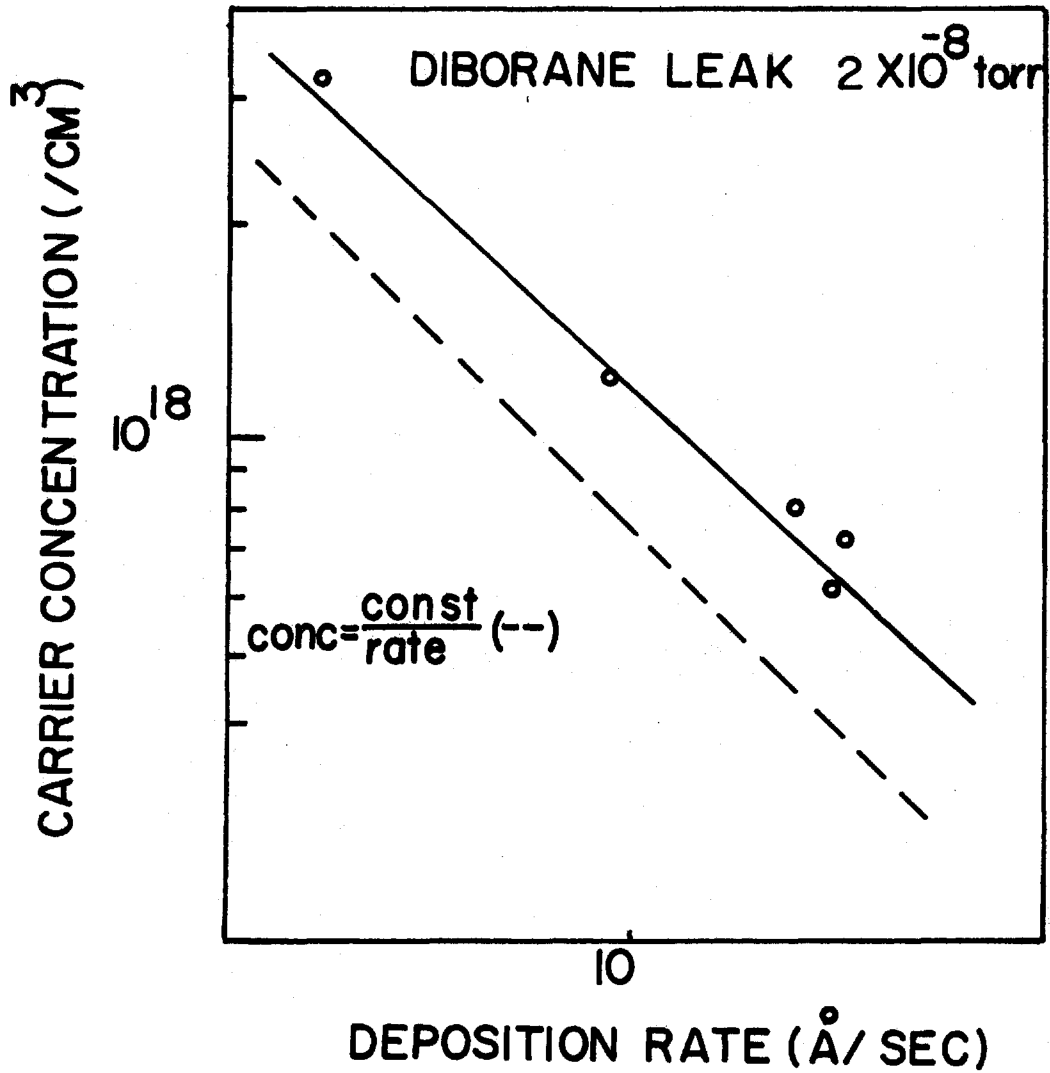


Fig.(5-5) Carrier concentrations in boron doped layers versus deposition rate. Substrate temperature 700°C

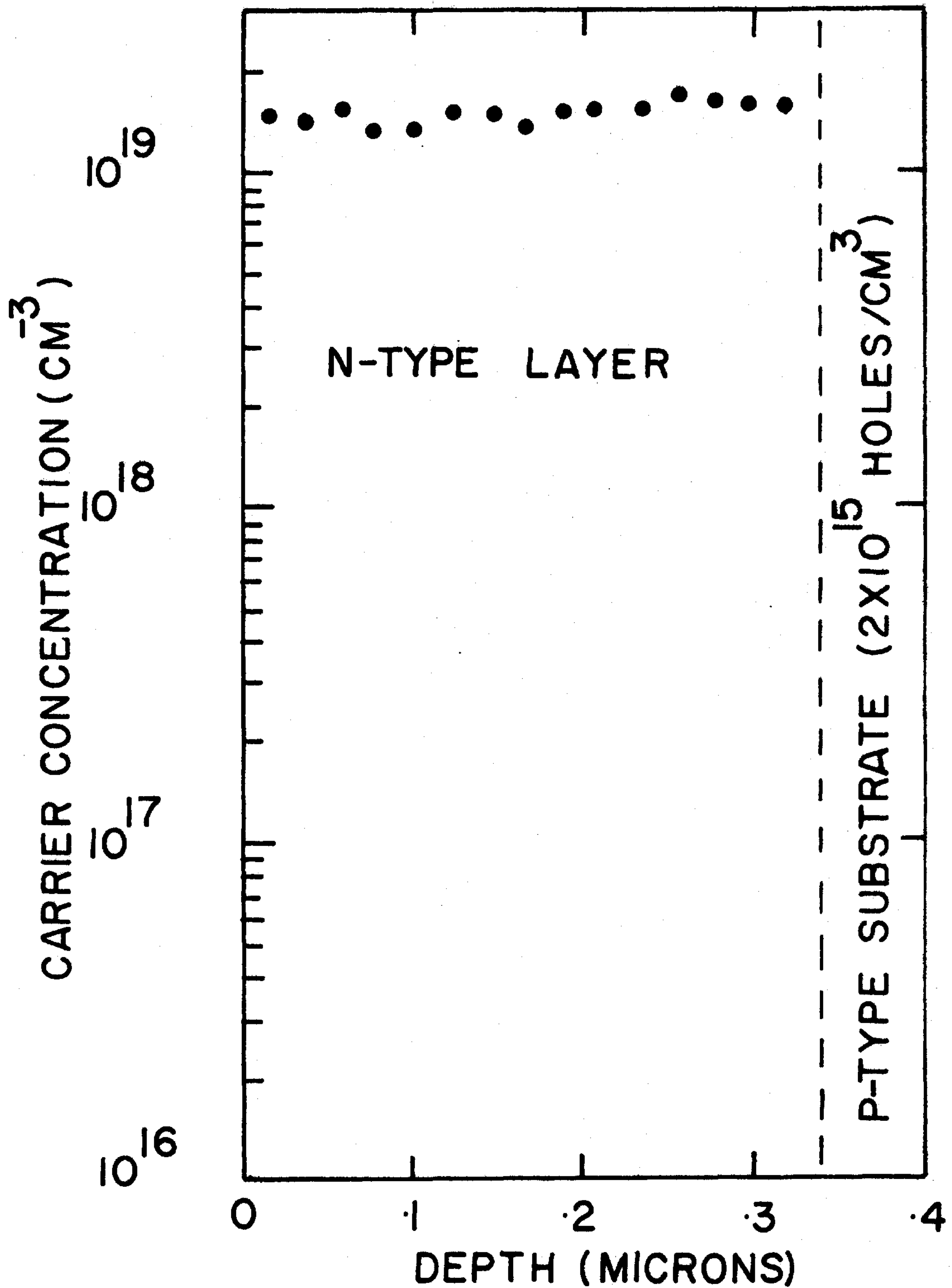
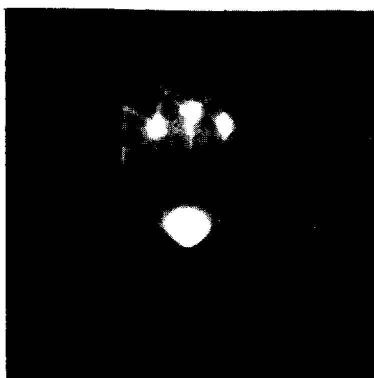
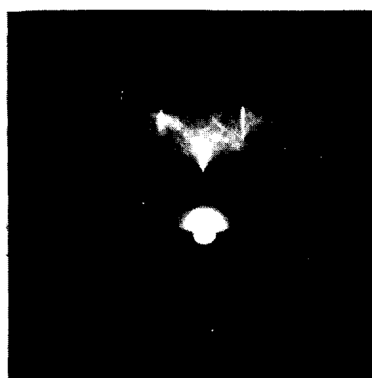


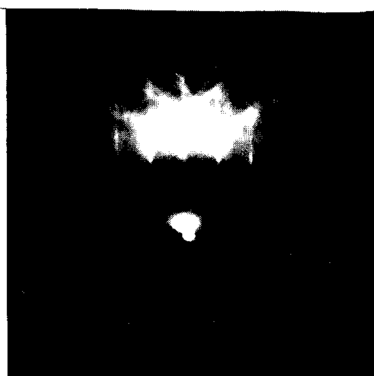
Fig.(5-6) Carrier concentration profile in phosphorus doped silicon layer evaporated with a constant phosphine pressure and a change in evaporation rate from 3 Å/sec to 15 Å/sec half-way through the total evaporation



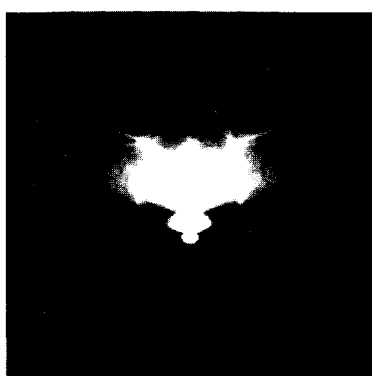
Si <111> 7×10^{18} BORON



Si<111> 2.1×10^{19} ARSENIC



Si<100> 7×10^{18} BORON



Si<100> 2×10^{19} ARSENIC

Fig. (5-7): HEED patterns obtained from silicon films heavily doped with boron and arsenic deposited onto Si<111> and Si<100> substrates having temperatures of 600°C.

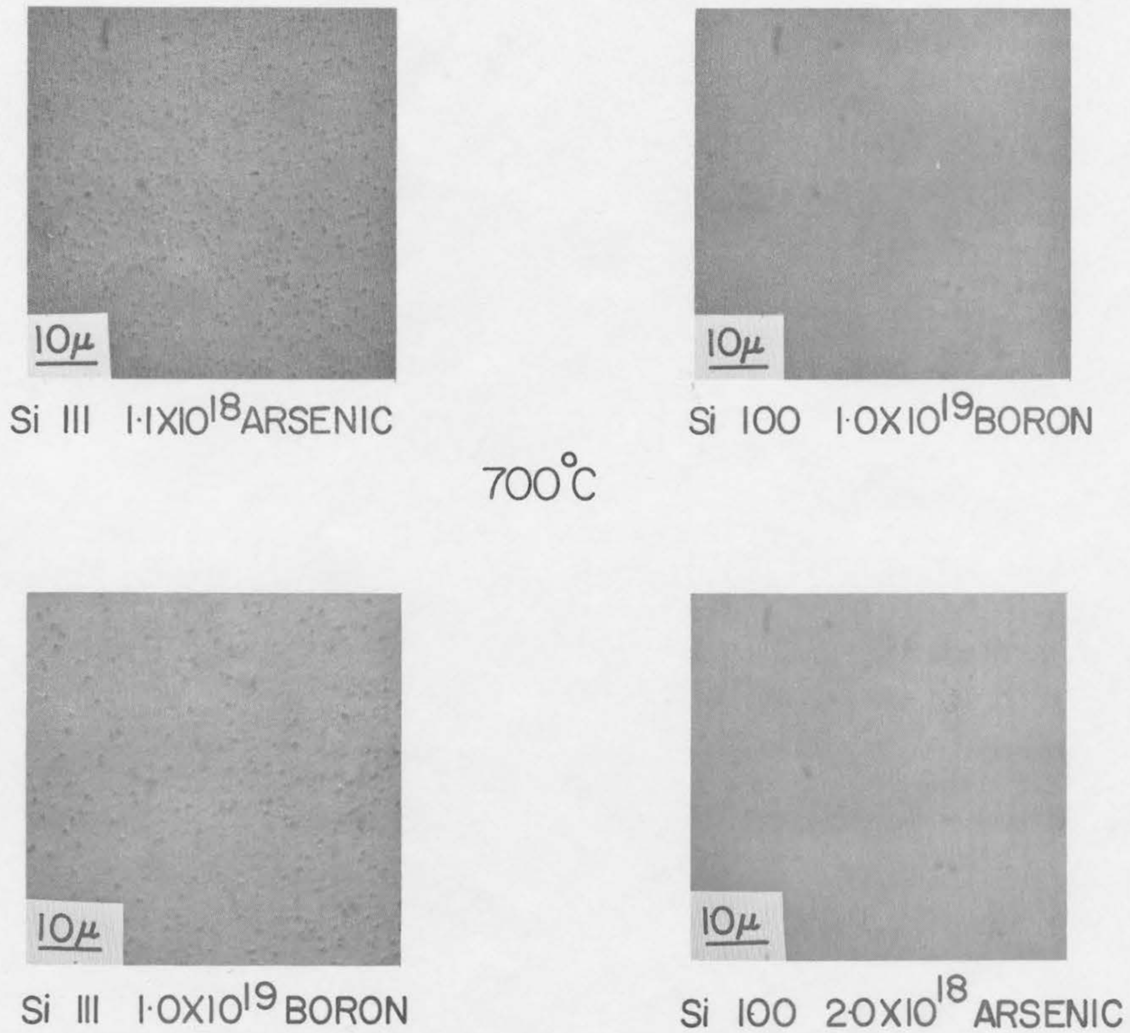


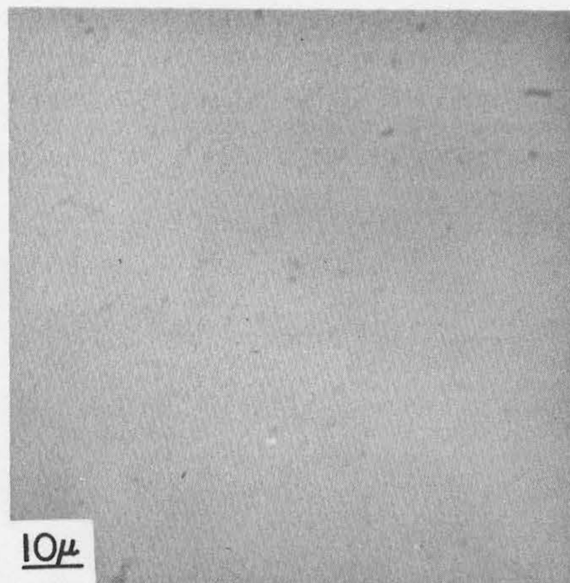
Fig. (5-8): Nomarski micrographs obtained from heavily doped silicon films deposited onto Si<111> and Si<100> substrates having temperatures of 700°C. Sirtl etched 10 secs. Thickness ∿.7μ.

the figures. Films deposited onto Si <111> and Si <100> substrates having temperatures of 700°C with relatively low (< 10^{-7} torr) pressures of doping gas in the system possessed etch pit densities which were identical to those of undoped films shown in figures (4-4) and (4-6). An appreciable increase in etch pit density was observed in films deposited onto Si <111> substrates with high doping gas pressures. Films deposited onto Si <100> substrates were similar to those of (4-6) for the highest carrier concentrations observed.

Films deposited onto substrates held at temperatures of 600°C exhibited a greater deterioration as a result of the doping process. Figure (5-9) shows micrographs of etched films having high arsenic concentrations deposited onto Si <111> and Si <100> substrates at 600°C. The surfaces are seen to display a large number of etch pits indicating the presence of a high concentration of structural defects in these deposited layers.

5.3.6 Doping limits

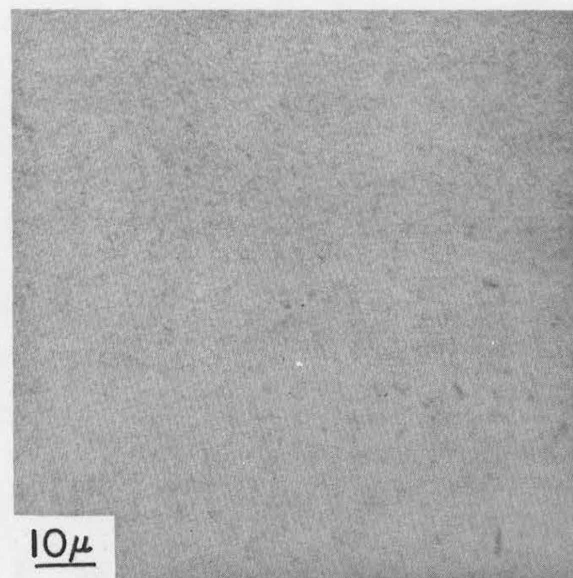
A value of $1.6 \times 10^{19}/cm^3$ has been reported[52] as the solid solubility limit for boron in silicon at 700°C. The maximum carrier concentrations obtained in boron doped evaporated layers were $1.5 \times 10^{19}/cm^3$ and $7 \times 10^{18}/cm^3$ for substrate temperatures of 700°C and 600°C respectively. Substitutional boron concentrations close to the solid solubility limit were thus attained by the gas-doping technique. Maximum carrier concentrations in arsenic and phosphorus doped layers were $1.5 \times 10^{18}/cm^3$ and $3 \times 10^{19}/cm^3$ for substrates having temperatures of 700°C and $1.5 \times 10^{19}/cm^3$ and $2 \times 10^{19}/cm^3$ for substrates having temperatures of 600°C. While values for the solid solubility limits of phosphorus and arsenic in silicon at these low temperatures could not



Si<111>

600 °C

ARSENIC
$2{\cdot}1 \times 10^{19}$



Si<100>

600 °C

ARSENIC
$2{\cdot}1 \times 10^{19}$

Fig. (5-9): Nomarski micrographs obtained from heavily doped silicon films evaporated on Si<111> and Si<100> substrates having temperatures of 600°C. Sirtl etched 10 secs. Thickness $\sim .7\mu$.

be located in the literature, reasonable extrapolation of published[53] data for higher temperatures indicate that the doping concentrations in the layers deposited at 600°C were close to their respective solid solubility limits.

5.4 Profile control by evaporation gas-doping

5.4.1 Introduction

To investigate the feasibility of profile control by the evaporation gas-doping technique a series of silicon layers possessing "step" impurity profiles were fabricated and analyzed. The creation of "step" impurity profiles is probably the most rigorous test of the capabilities of the gas doping technique since such profiles are,in general,readily degraded both by auto-diffusion in the epitaxial layer and by the response time of the system to changes in the dopant concentration. The low fabrication temperature and ease of impurity control in the gas-doping technique suggest that this might be employed to form semiconductor layers possessing impurity steps more abrupt than may be obtained by conventional methods.

5.4.2 Experimental

Step profiles both from lower to higher and from higher to lower doping concentration were investigated. Phosphine of nominal 100% purity was employed as a doping gas. The substrates employed were 10 ohm-cm <111> P-type silicon and were held at a temperature of 700°C.

To produce layers containing step profiles from a lower to a higher doping concentration a film of $\sim$2000 Å was first evaporated with a low pressure of doping gas present in the system. The substrate was then covered with a shutter and the phosphine pressure raised to a higher value. When the system had reached equilibrium, the shutter was removed and a

further thin film evaporated. To obtain step profiles going from a higher to a lower doping concentration,a thin film of ~2000 Å was first evaporated with a high pressure of doping gas present in the system. The substrate was covered with a shutter and allowed to cool and the evaporation and gas leaks terminated. When the system had attained a sufficiently low pressure the gas leak was resumed, the substrate reheated, and a second thin film of low impurity concentration deposited.

Resistivity and impurity profiles were investigated employing Hall effect measurements combined with anodization and HF acid stripping. The techniques and data analysis employed are considered in appendix (A).

5.4.3 Experimental results and discussion

Typical step impurity profiles determined in vacuum evaporated gas-doped silicon films are illustrated in Figs. (5-10) and (5-11). Changes in impurity concentration over two orders of magnitude were readily obtained over distances of approximately 700 Å. The impurity distribution which results from the diffusion of a concentration step in which the material thickness on one side is initially zero and increases linearly with time is given by the expression:[20]

$$N(x,t) = \frac{N_1}{2}\left[\mathrm{erfc}\left(\frac{x - \nu t}{2\sqrt{Dt}}\right) + \exp\left(\frac{\nu x}{D}\right) \mathrm{erfc}\left(\frac{x + \nu t}{2\sqrt{Dt}}\right)\right] + \frac{N_2}{2}\left[1+\mathrm{erf}\left(\frac{x - \nu t}{2\sqrt{Dt}}\right)\right] \quad (5\text{-}3)$$

where

N_1 = mean carrier concentration measured in the first layer

N_2 = mean carrier concentration measured in the second layer

t = time taken to evaporate the second layer

D = diffusion coefficient

ν = growth rate of the epitaxial layer

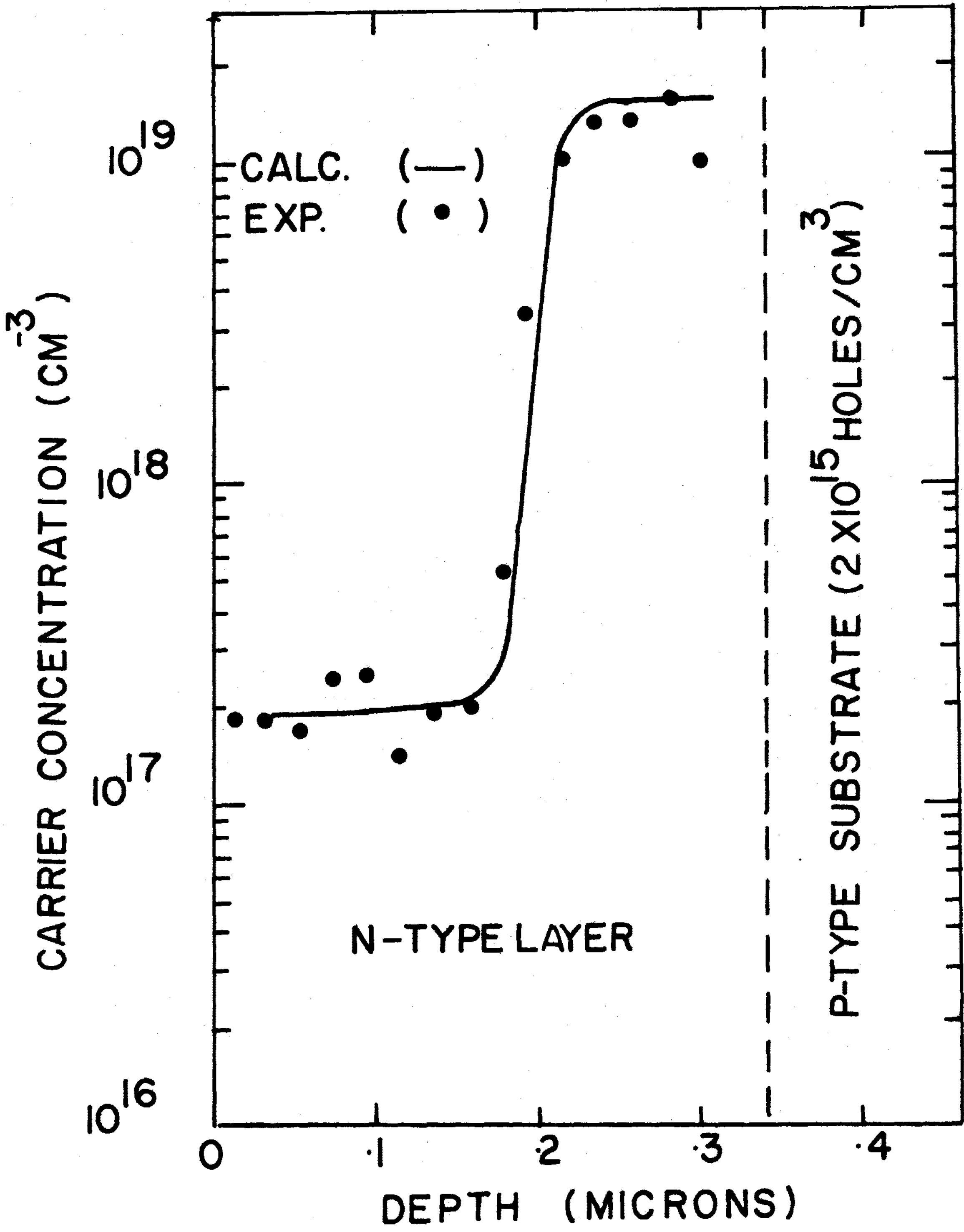


Fig. (5-10) Step impurity profile in vacuum evaporated phosphorus doped silicon film. High to low concentration

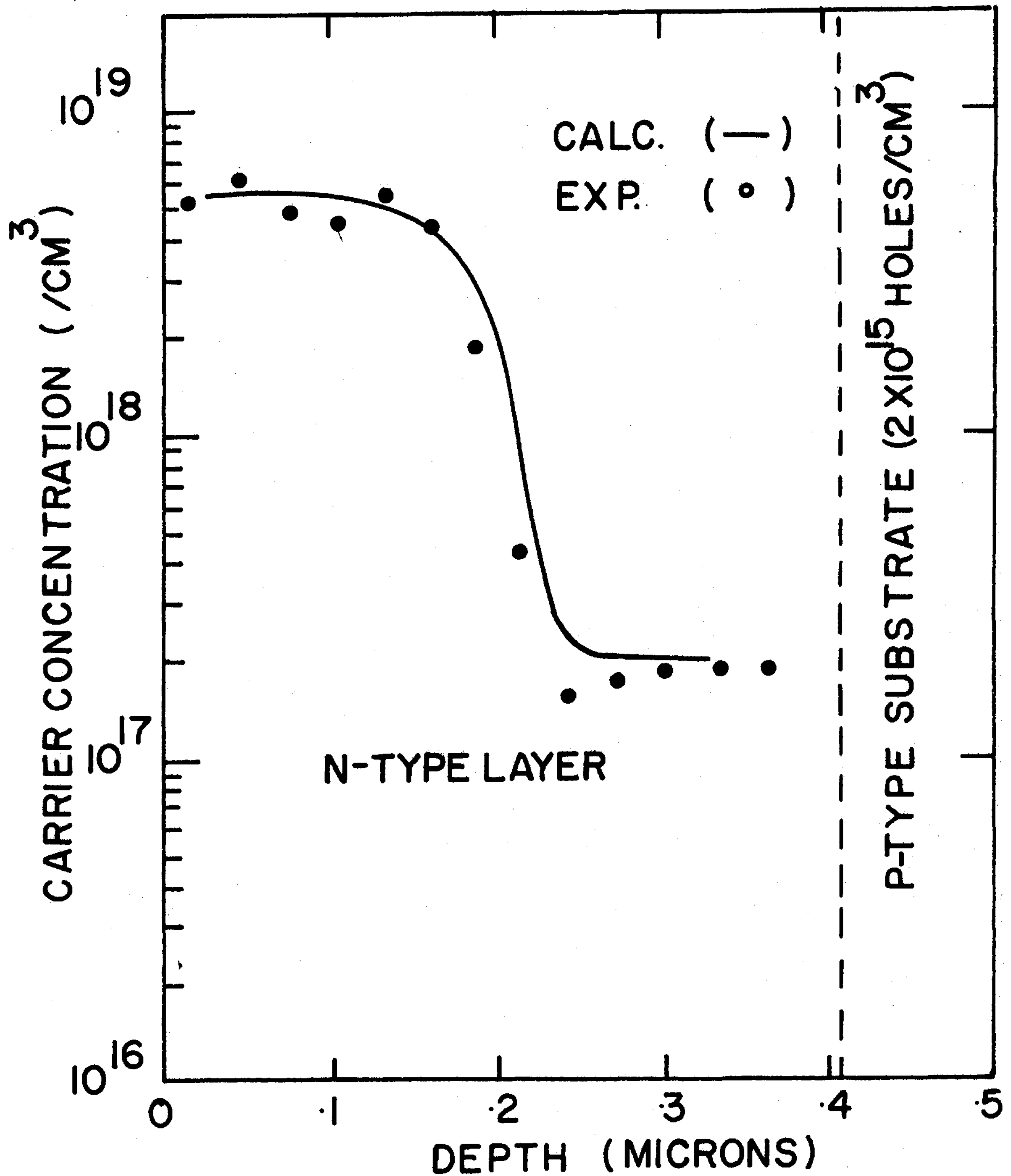


Fig. (5-11) Step impurity profile in vacuum evaporated phosphorus doped silicon film. Low to high concentration

The rate of impurity loss from the silicon surface is assumed to be negligible.

Fitting of profiles calculated from the above expression to those experimentally determined yielded a value of $D \approx 5 \times 10^{-15}$ cm^2/sec. for the diffusion coefficient of phosphorus in the evaporated silicon at 700°C. While this value is larger than that ($D \approx 10^{-18}$ cm^2/sec) extrapolated from data[20] for bulk silicon at higher temperatures,it is evident that the evaporation gas-doping technique may be employed in the fabrication of silicon layers possessing impurity steps more abrupt than may be obtained either by conventional diffusion or by chemical vapor epitaxy. The occurrence of larger apparent D values than might be expected may be attributed either to the interruptions in the deposition or to the enhanced diffusion observed in epitaxial layers containing defects.[54]

5.5 Doping mechanism

5.5.1 Introduction

The most probable sequence of steps which lead to the contribution of one free carrier by an impinging dopant molecule to a deposited silicon film is as follows:

(1) adsorption of the impinging doping gas molecule onto the silicon surface

(2) thermal decomposition of the doping gas molecule

(3) desorption of the hydrogen content of the doping gas molecule

(4) surface migration of the dopant atom

(5) capture at growth step (or island before the formation of a continuous film)

(6) covering of the dopant atom by further deposited silicon

(7) ionization of the dopant to provide a free carrier

Mechanisms whereby the impinging molecule fails to contribute to the free carrier concentration are as follows:

(8) reflection of the impinging molecule from the substrate surface

(9) burial of the dopant molecule without decomposition

(10) desorption of the dopant atom before capture

(11) incorporation of the dopant atom at a non-substitutional lattice site

(12) capture of the free carrier at an electrically compensating centre

Since only a few of the many parameters governing these reactions are known, development of a quantitative model of the gas doping process was not attempted. However, employing the condensation theory outlined in chapter (2) and some general comparisons with somewhat similar deposition systems described in the literature, the general features of the present experimental results may be, at least qualitatively, explained. The fact that no fully satisfactory model has as yet been developed[55] which describes dopant incorporation in the widely studied chemical vapor phase epitaxial system is indicative of the complexity of systems of this type.

5.5.2 Condensation

The interaction of a neutral gas molecule with a solid surface is governed by a combination of van der Waals, repulsive and chemical bonding forces.[56] While published data for such systems is limited, condensation

coefficients are generally observed to be much less than unity. Joyce et al.[14] estimated that approximately .01% of the silane molecules incident on a substrate surface at 845°C in vacuum finally contributed a silicon atom to a deposited layer. In the present experiments it may reasonably be assumed that, as is the case in silane decomposition systems, the vast majority of doping gas molecules which impinge on the silicon surface are not adsorbed but are reflected and subsequently pumped from the vacuum chamber. Estimates of the number of incident doping gas molecules which contributed to the deposited layer have been given in 5.3.2. The maximum values of "conversion" efficiency i.e. .005% for diborane at 700°C and .02% for arsine at 600°C are comparable with the value for silane given by Joyce at al.[14]

5.5.3 Incorporation

Arsine, phosphine and diborane in the gas phase decompose to their elements at approximately 300°C.[48] Studies[57] of phosphine and arsine adsorbed on silicon (111) surfaces at room temperature and subsequently heated showed that complete decomposition of these molecules, as indicated by hydrogen evolution, took place at 500°C. Since the substrate temperatures employed in the present investigations were greater than 500°C, thermal decomposition of the doping gas was unlikely to be a rate limiting step.

The dopant adatom surface diffusion coefficient, diffusion length and surface lifetime are given in terms of the activation energies for desorption and surface diffusion and the adatom-surface vibrational frequency by the expressions (2-1,2,3). Studies of the carrier concentration in phosphorus and arsenic doped silicon films sublimed from doped sources

in high vacuum onto substrates having temperatures between 600°C and 1000°C have been reported by Kuznetsov et al.[58] These workers observed a decrease in the doping concentrations in their deposited layers with increasing substrate temperature similar to that observed in the present experiments. This decrease in doping concentration was attributed to an increase in the desorption of the dopant atoms from the surface with increasing substrate temperature.

If we assume that (1) the number of dopant adatoms desorbing is much greater than that being incorporated into the layer, that (2) both the dopant adatom flux and the proportion of dopant atoms incorporated into the growing layer are independent of temperature and that (3) all the incorporated adatoms become electrically active, we obtain the expression

$$N = \text{const.} \exp\left(\frac{E_{DES}}{RT}\right) \qquad (5\text{-}4)$$

where N = carrier concentration in the layer

R = gas constant

T = absolute temperature

E_{DES} = activation energy for dopant desorption

for the carrier concentration as a function of substrate temperature during deposition. Employing this expression and the data shown in figure (5-4) activation energies of 30 kcal/mole and 40 kcal/mole were obtained for phosphorus and arsenic desorption between substrate temperatures of 800°C and 700°C. Employing these values and the expression (2-1), values of $\sim 1 \times 10^{-7}$ sec. and $\sim 1 \times 10^{-5}$ sec. were obtained for the surface residence times of phosphorus and arsenic adatoms respectively on substrates having

temperatures of 700°C. Since these lifetimes are very much less than the time (∿1 sec) required to deposit one monolayer of silicon, trapping of the dopant adatom by the deposited silicon prior to capture or desorption is most unlikely.

In the case of diborane, no strong temperature dependence was observed and adatom desorption was thus presumably minimal. A relative comparison of the strengths of the bonds between the dopant adatoms and the silicon substrate may be obtained by considering the decomposition activation energies of the three solid dopants. Values of 60 kcal/mole, 75 kcal/mode and 141 kcal mole have been reported[59] for arsenic, phosphorus and boron respectively. If the boron-silicon bonding is approximately twice as strong as that of the other dopants, a value for the adatom surface lifetime of $\sim 5 \times 10^3$ sec. is obtained. Desorption of boron may thus be assumed to be minimal.

Since the expression (5-4) fails to include the possible temperature dependence either of the dopant condensation or of the capture processes, the values derived for the desorption activation energies and associated surface lifetimes are questionable. However, interpretation of the experimental data for the doping concentrations in layers deposited at 700°C as being limited in the cases of arsenic and phosphorus by desorption and in the case of boron by condensation appears reasonable.

Further confirmation of this interpretation may be obtained by considering the rate dependence data of 5.3.4. For a substrate temperature of 700°C the majority of arsenic and phosphorus atoms desorbed before being captured by a growth step. For higher deposition rates, step motion

was more rapid allowing a greater proportion of the adsorbed dopant atoms to be collected. Since this effect was exactly sufficient to offset the decreased ratio of dopant atoms to silicon atoms incident on the surface at higher deposition rates, no net rate dependence was detected. For boron doped films, desorption was not significant and the majority of adsorbed atoms were collected. The doping concentration was thus found to be inversely proportional to the deposition rate as shown in figure (5-5).

The dependence of the observed carrier concentrations on doping gas pressures may not be explained without a knowledge of the detailed mechanisms both of the layer growth and the dopant condensation. The reduction in the proportions of arsenic and phosphorus incorporated into the layer at high arsine and phosphine pressures may probably be attributed to changes in the condensation and desorption kinetics for high surface concentrations. Similar reductions at high phosphine pressures as compared with those of diborane have been reported in chemical epitaxial systems.[60]

Formulation of an explanation for the experimental results is further complicated by the possibility that, as is commonly observed in ion-implanted layers,[21] measurements of carrier concentration do not reflect the true impurity content of the deposited films. Substantial quantities of non-electrically active dopant atoms may exist either as precipitates, or trapped at defect boundaries.

5.5.4 Doping and growth

The presence of relatively high pressures both of hydrogen and of the doping gases at the substrate surface may be expected to modify the growth of homoepitaxial silicon films by several distinct processes.

1) Collisions of the adsorbed silicon atoms with non-reactive molecules may reduce the adatom mobility. Since this reduction is effectively equivalent to that which results from a lowering of the substrate temperature, an increase in the concentration of structural imperfections may be observed.

2) If the doping gas mixture contains even a relatively small concentration of contaminating impurities such as hydrocarbons or oxygen, a severe reduction in the structural perfection of the deposited layers will be observed.

3) The presence of dopant adatoms on the substrate surface may modify the kinetics of growth either by increasing or decreasing the free energy of potential nucleation clusters or, of changing the binding energy of kink sites.

4) For doping impurity concentrations close to their respective solid solubility limits, the possibility exists that clusters of dopant adatoms will form on the substrate surface. Such clusters may result in a deterioration in the structural perfection of the homoepitaxial silicon layers.

The data obtained from the present study does not provide sufficient evidence to allow a decision to be made as to which of the above mechanisms resulted in the structural deterioration in the layers considered in 5.3.5. However, since the structural deterioration in the layers evaporated at 700°C onto Si <111> substrates was much more severe than that observed for similar depositions onto Si <100> substrates, the presence of process (1) i.e. an effective lowering of the substrate temperature might be suspected. The considerable structural deterioration observed in films

containing high doping concentrations evaporated at 600°C onto substrates having both orientations may probably be attributed to process (4).

While the gas-doping technique has been shown to be effective in introducing controlled concentrations of doping impurities into the evaporated silicon layers, the proportion of dopant molecules incident on the substrate surface which contribute to the electrical activity of the deposited material is small. Gas pressures as high as $\sim 10^{-3}$ torr were estimated to be present at the silicon surface during the deposition of layers containing the highest carrier concentrations observed. Modifications of the doping technique which would permit a greater proportion of the injected dopant to be incorporated into the growing layer are considered in chapter (8).

5.6 Summary

In this chapter the feasibility of gas-doping as a technique for reproducibly introducing controlled concentrations of doping impurities into vacuum evaporated homoepitaxial silicon layers has been considered. Employing arsine, phosphine and diborane as doping gases,both P and N-type films containing carrier concentrations up to $\sim 3 \times 10^{19}/cm^3$ have been obtained. The carrier concentrations in the deposited layers have been measured as functions of such system parameters as substrate temperature, deposition rate and doping-gas pressure.

Silicon films evaporated onto both Si <111> and Si <100> substrates at 700°C and 600°C have been found to be single crystal even for the highest carrier concentrations detected. However, increased defect densities as compared with undoped films have been observed both in heavily doped layers deposited at 700°C onto Si <111> substrates and, in doped layers deposited at 600°C onto substrates having either orientation.

The evaporation gas-doping technique has been shown to be capable of producing silicon films possessing highly abrupt step impurity profiles at temperatures as low as 700°C. Variations of up to two orders of magnitude in carrier concentration have been obtained in approximately 700 Å of evaporated phosphorous doped silicon. Fitting of profiles calculated from appropriate diffusion formulae to those determined from experimental data has been employed to yield a value for the diffusion coefficient (D) for phosphorus in the evaporated films. The value of $D = 5 \times 10^{-15}$ cm^2/sec. obtained in films evaporated at 700°C is sufficiently low to permit the fabrication of silicon layers possessing impurity steps more abrupt than may be obtained either by diffusion or by conventional chemical epitaxy.

CHAPTER VI

ELECTRICAL CHARACTERISTICS AND APPLICATIONS

6.1 Introduction

In previous chapters it has been established that single crystal silicon films possessing both controlled impurity concentrations and a high degree of structural perfection may be obtained at temperatures as low as 700°C by the technique of vacuum evaporation combined with gas-doping. To be of practical application in device fabrication the doped evaporated material must possess electrical characteristics which are comparable with those exhibited by bulk single crystal silicon. Deviations from bulk behaviour may result from the presence either of structural defects or of contaminating impurity species in the deposited layers. Such imperfections may provide scattering, doping, trapping and compensating levels in the bandgap of the deposited material.

This chapter describes an evaluation of the electrical properties of the evaporated homoepitaxial silicon layers. The characteristics of some simple active devices formed by the evaporation gas-doping technique are considered. In view of the structural deterioration observed in films evaporated onto substrates having temperatures of 600°C as a result of the gas-doping process, a substrate temperature of 700°C was generally employed in depositing films for electrical evaluation.

6.2 Electrical Characteristics

6.2.1 Undoped Layers

The electrical characteristics of a series of relatively thick ($\cdot 8_{\mu}$) undoped evaporated homoepitaxial layers were investigated. To minimize

carryover doping from previous experiments, the shroud and substrate heater were etched and the entire system baked for ∿100 hours prior to the evaporation of the series of undoped films. Since thermal probe[61] measurements showed undoped films to be N-type, depositions were made onto N-type substrates to avoid the complicating effects of P-N junctions.

Resistivity profiles in the undoped layers were determined employing a spreading resistance probe.[62,63] The spreading resistance probe technique consists of determining the resistance between a pair of closely spaced probes which are stepped along the surface of the sample to be analyzed. The probes are calibrated by measurements on silicon slices whose resistivity is known. By stepping the probes along an angle lapped sample,the resistivity versus depth profile may be determined. While some uncertainty exists as to the accuracy of this technique when applied to layers as thin as those considered here, measurements on doped layers of equal thickness gave results consistent with those obtained by other methods.

Typical resistivity and carrier concentration profiles obtained from a film deposited under ultra high vacuum conditions onto a 2 ohm-cm Si<100> N-type substrate at 700°C are shown in figure (6-1). In calculating the carrier concentrations shown, the mobilities in the deposited material were assumed equal to those of bulk single crystal silicon.[64] Subsequent measurements of carrier mobility to be described in 6.2.2 indicate that this assumption will introduce an error of not more than 30% in estimates of carrier concentration.

Resistivities in the deposited film are seen to range from 2 to 6 ohm-cm. Similar results were obtained for depositions both under high vacuum and under

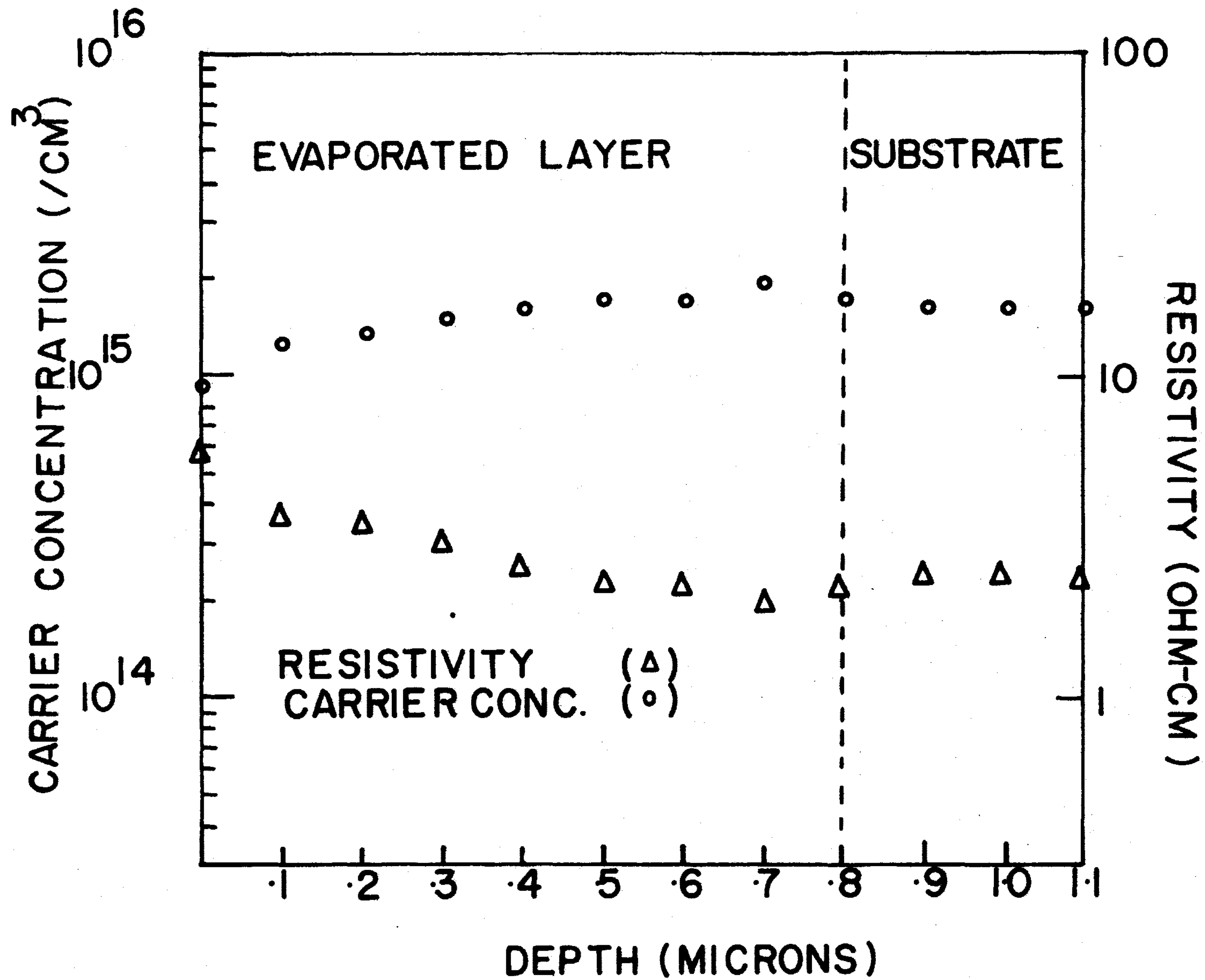


Fig.(6-1) Resistivity and carrier concentration profiles in undoped silicon film evaporated in ultra high vacuum. Substrate temperature 700°C

ultra high vacuum conditions. Since the resistivity of the source material was 100 ohm-cm and was P-type, the results indicate a concentration of $\sim 2 \times 10^{15}/cm^3$ of unintentional N-type impurities to have been introduced into the deposited layer. The presence of these unwanted doping impurities may be attributed either to residual carryover doping or to contaminating species originating from the evaporation units and the substrate heater. Thomas and Francombe[34] have reported that homoepitaxial silicon films sublimed in ultra high vacuum from a 200 ohm-cm P-type source onto resistively heated, predeposition heat-treated substrates possessed resistivities as high as 10^3 ohm-cm.

6.2.2 Room Temperature Mobility in Doped Evaporated Films

Carrier mobilities at room temperature in high purity bulk single crystal silicon are determined by a combination of lattice and ionized impurity scattering.[65] The relative contribution of either scattering mechanism will depend on the doping concentration. In deposited thin films, additional scattering mechanisms may result in a reduced carrier mobility. Factors which increase scattering and hence reduce mobility include surface scattering, scattering from neutral or ionized contaminating impurities and scattering by structural defects.[65] Reduced carrier mobilities are generally observed in heteroepitaxial layers deposited by chemical techniques.[66]

Room temperature Hall mobilities measured in P and N-type gas doped homoepitaxial silicon layers evaporated onto substrates having a temperature of 700°C are shown in figures (6-2) and (6-3) as functions of majority carrier concentration. Since, in calculating carrier concentrations from Hall effect data, the ratio of conductivity mobility to Hall mobility was

Fig.(6-2) Hall mobilities in evaporated P-type films versus carrier concentration. Substrate temperature 700°C

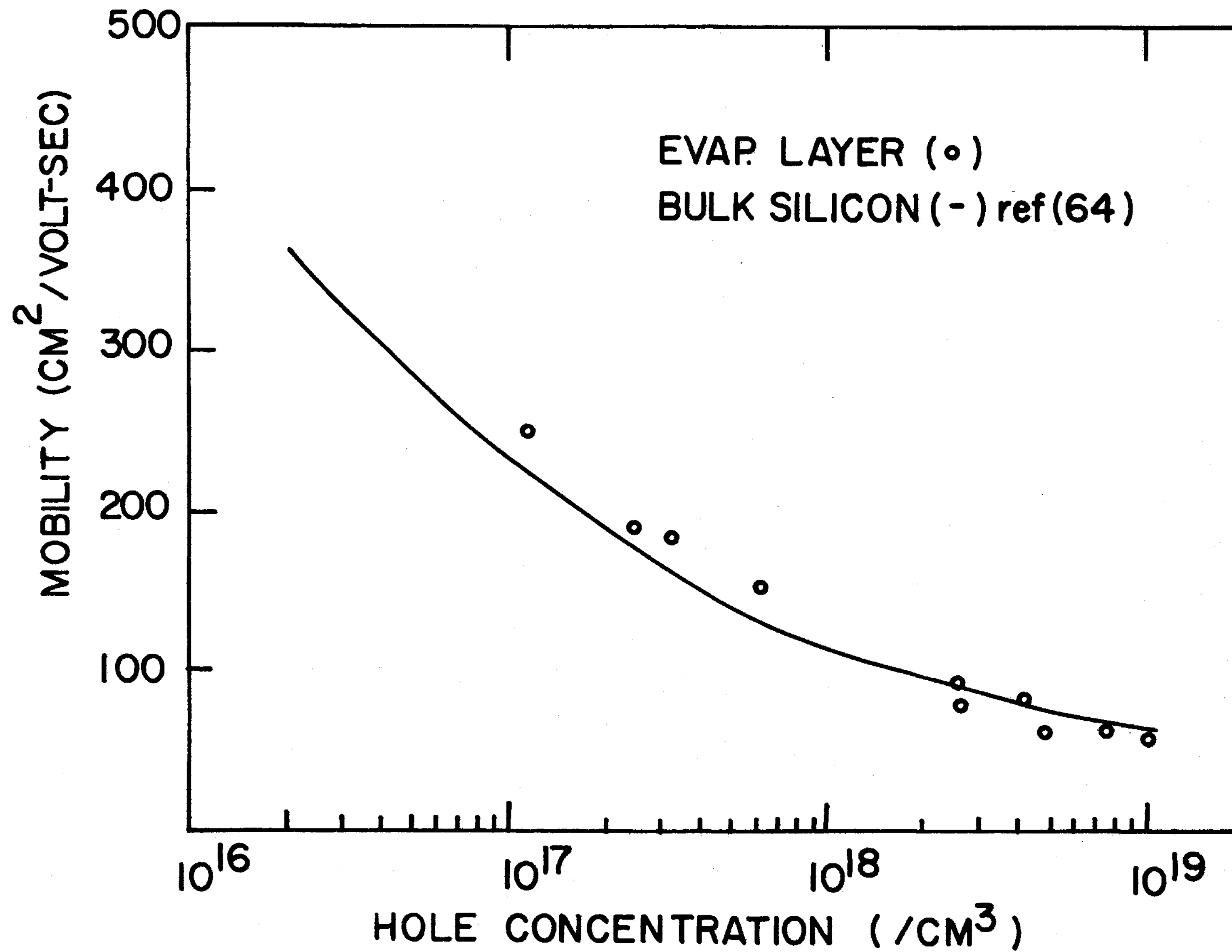
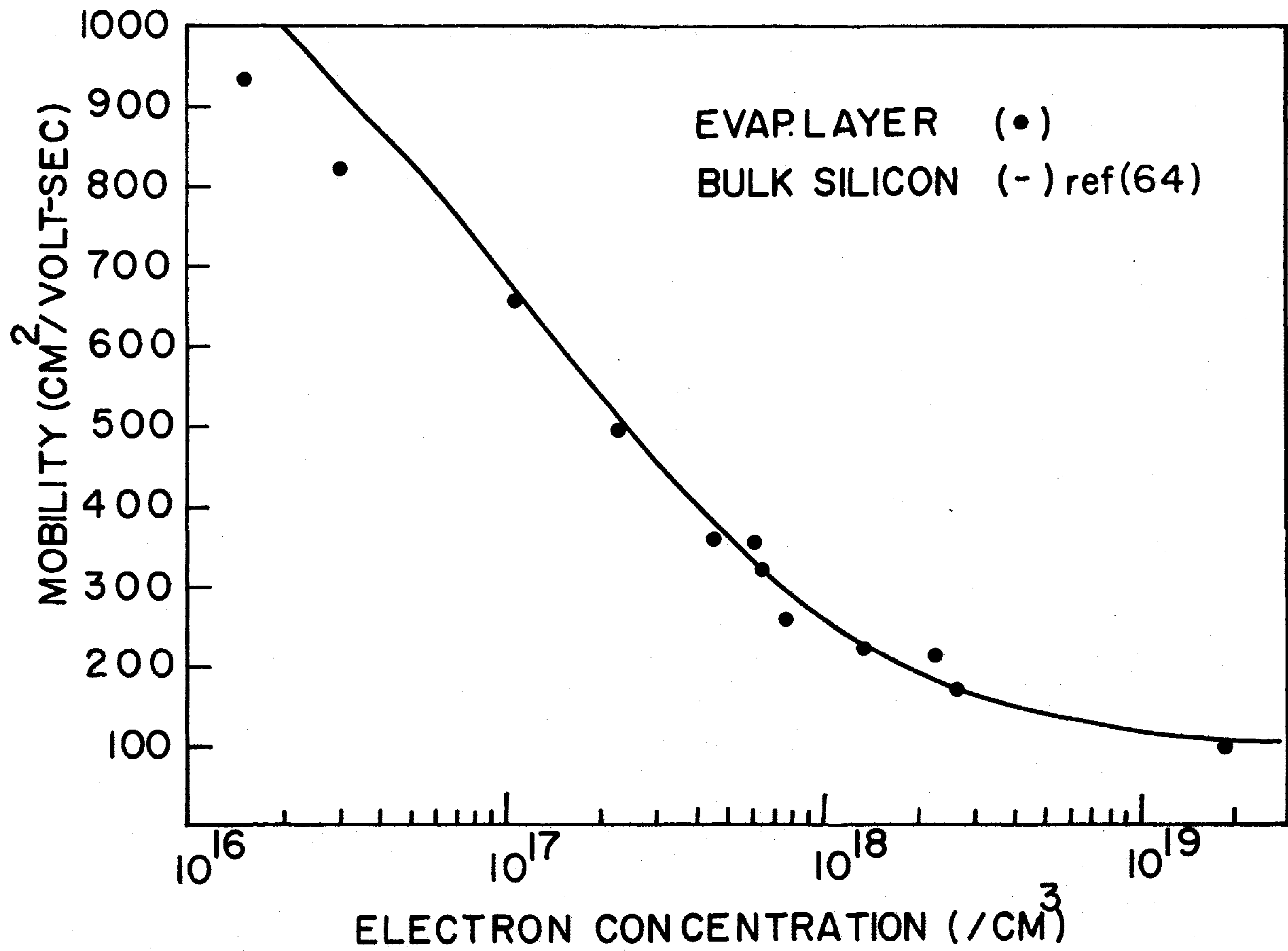

500
400
300
200
100
MOBILITY (CM2/VOLT-SEC)
EVAP. LAYER (o)
BULK SILICON (-) ref (64)
10^16
10^17
10^18
10^19
HOLE CONCENTRATION (/CM3)

Fig.(6-3) Hall mobilities in evaporated N-type films versus carrier concentration. Substrate temperature 700°C


EVAP. LAYER (•)
BULK SILICON (-) ref(64)
MOBILITY (CM^2/VOLT-SEC)
1000
900
800
700
600
500
400
300
200
100
10^{16}
10^{17}
10^{18}
10^{19}
ELECTRON CONCENTRATION (/CM^3)

assumed equal to unity, the conductivity mobility in bulk single crystal silicon[64] is shown for comparison. The techniques and data analysis employed in Hall effect and conductivity measurements on evaporated silicon layers are considered in Appendix (A).

For N-type films possessing carrier concentrations from 10^{17} to $2 \times 10^{19}/cm^3$ the observed carrier mobilities were comparable with those obtained in bulk single crystal silicon. For carrier concentrations between 10^{16} and $10^{17}/cm^3$ the measured values of carrier mobility were approximately 10% lower than those in the bulk material. For P-type films, carrier mobilities were comparable with those of bulk silicon over the range considered $10^{17} - 10^{19}/cm^3$. No significant differences were detected between the carrier mobilities measured in films deposited onto Si<111> and those deposited onto Si<100> substrates.

Carrier mobilities in silicon thin films are frequently observed to be less than those in the corresponding bulk material. The scattering mechanisms which result in these reduced carrier mobilities have been the subject of a number of theoretical and experimental investigations.[68-70] Mechanisms resulting in reduced carrier mobilities in vacuum evaporated layers are considered in the next section.

6.2.3 Temperature Dependent Hall Effect Measurements

By measuring the carrier concentration in a doped semiconductor layer over a suitable temperature range both the ionization energy of the dopant impurity and the approximate concentration of compensating centres in the semiconductor material may be determined.[71] Measurements were performed on arsenic doped evaporated layers deposited both onto Si<111> and Si<100>

substrates having temperatures of 700°C. Figure (6-4) shows a typical plot of carrier concentration versus reciprocal temperature for a film having a thickness of .72μ and a room temperature carrier concentration of $2.3 \times 10^{17}/cm^3$ deposited onto a 10 ohm-cm P-type Si<100> substrate. Comparable data obtained from the literature[67] for a bulk arsenic doped silicon sample having a room temperature carrier concentration of 1.3×10^{17} electrons/cm^3 is included for comparison. The expression[71]

$$\frac{\partial \log n}{\partial (\frac{1}{T})} = -(5.04)E_D - (0.78)T \qquad (6\text{-}1)$$

where E_D = ionization energy of the donor in meV

n = carrier concentration

describes the temperature dependence of the carrier concentration in the low temperature compensated region of the n versus 1/T characteristic. Employing the data shown in figure (6-4) and the above expression a value of 50 ± 1 meV was obtained for the ionization energy of the dopant in the evaporated layer. This value is in good agreement with that of 49 meV generally accepted[67] as the ionization energy for low concentrations of arsenic in bulk single crystal silicon.

The expressions[72]

$$n = \left(\frac{K_D + N_A}{2}\right) \left(\left[1 + \frac{4\, K_D(N_D - N_A)}{(K_D + N_A)^2}\right]^{1/2} - 1 \right) \qquad (6\text{-}2)$$

$$K_D = (2\pi\, m^*\, K\, T/h^2)^{3/2} \exp\left(-\frac{E_D}{KT}\right)$$

$$N_D > N_A$$

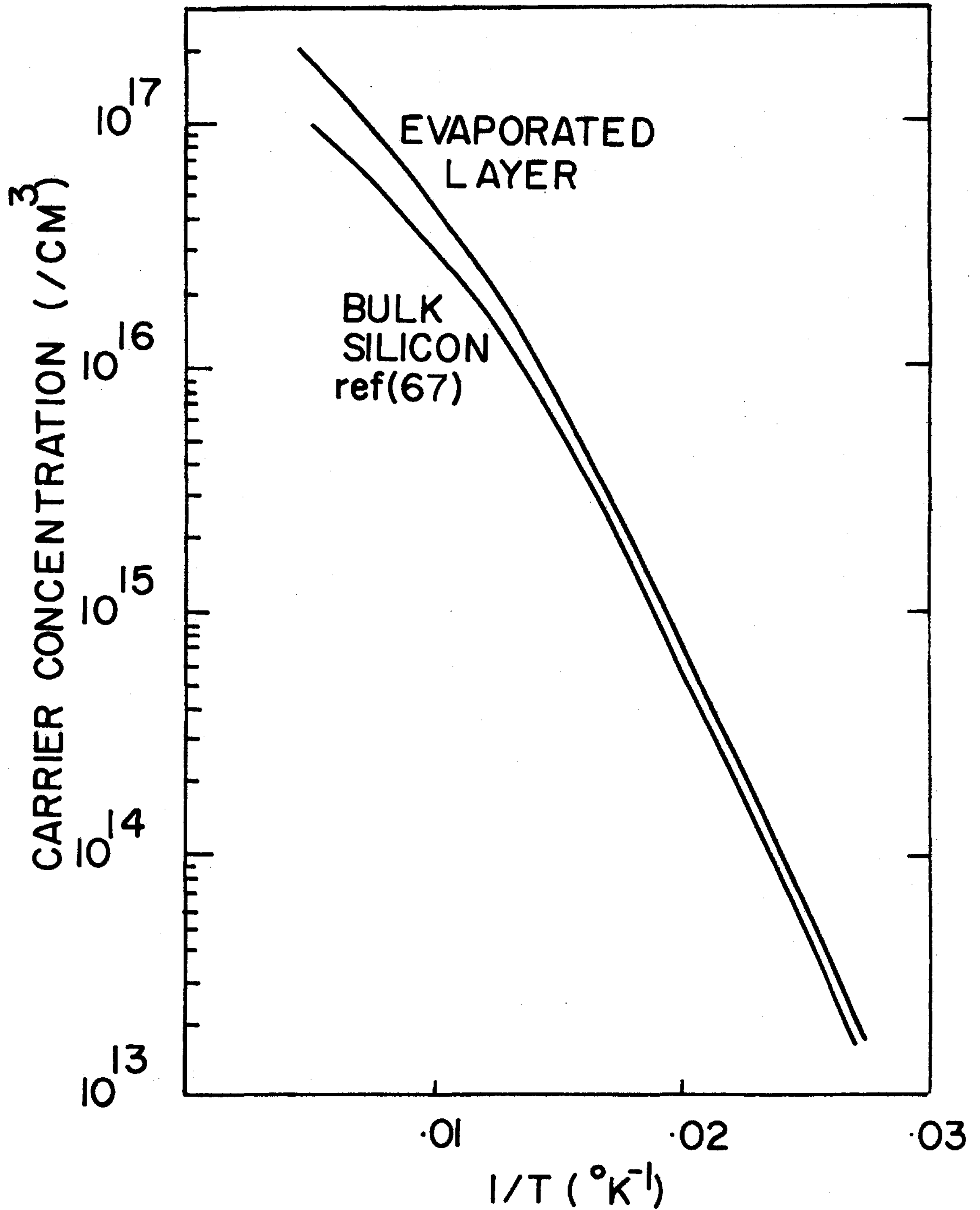


Fig.(6-4): Carrier concentrations in arsenic doped bulk and evaporated silicon versus reciprocal absolute temperature

(where m^*, h = effective mass of electrons, Plancks constant)describe the temperature dependence of the free electron concentration in a sample containing N_D donors and N_A acceptors/cm^3. By fitting these expressions to the data shown in figure (6-4) an approximate value of $N_A = 3 \pm 1 \times 10^{16}/cm^3$ was obtained. This value represents the concentration of P-type compensating levels present in the evaporated layer as a result either of carry-over P-type doping, of structural imperfections or of unwanted contaminating impurities. Comparable values of $\sim 1 \times 10^{16}/cm^3$ have been given for the compensation centre density in a well annealed ion implanted layer.[71]

Figure (6-5) shows the Hall mobility measured in the gas doped sample of figure (6-4) as a function of ambient temperature. Similar data published[67] for bulk single crystal silicon is included for comparison. While the mobilities in the gas-doped and bulk samples are seen to be equivalent at room temperature, considerably higher mobilities are observed in the latter at low temperatures (^60° K). The reduction in carrier mobility in the evaporated films may probably be attributed either to surface or dislocation scattering or to the presence of the compensating centres in the deposited material.

1) Surface scattering: Carriers impinging on the surface of a semiconductor may be reflected either by specular or by diffuse scattering processes.[65] In the former, only the component of the momentum of the carriers normal to the surface is changed and the carrier mobility is uneffected. In the case of diffuse reflection, the final velocity of the carriers is independent of their velocity prior to collision. The carrier mobility in the semiconductor is thus reduced within a distance comparable to the carrier mean free path. Theoretical calculations[65] which assume ionized impurity scattering

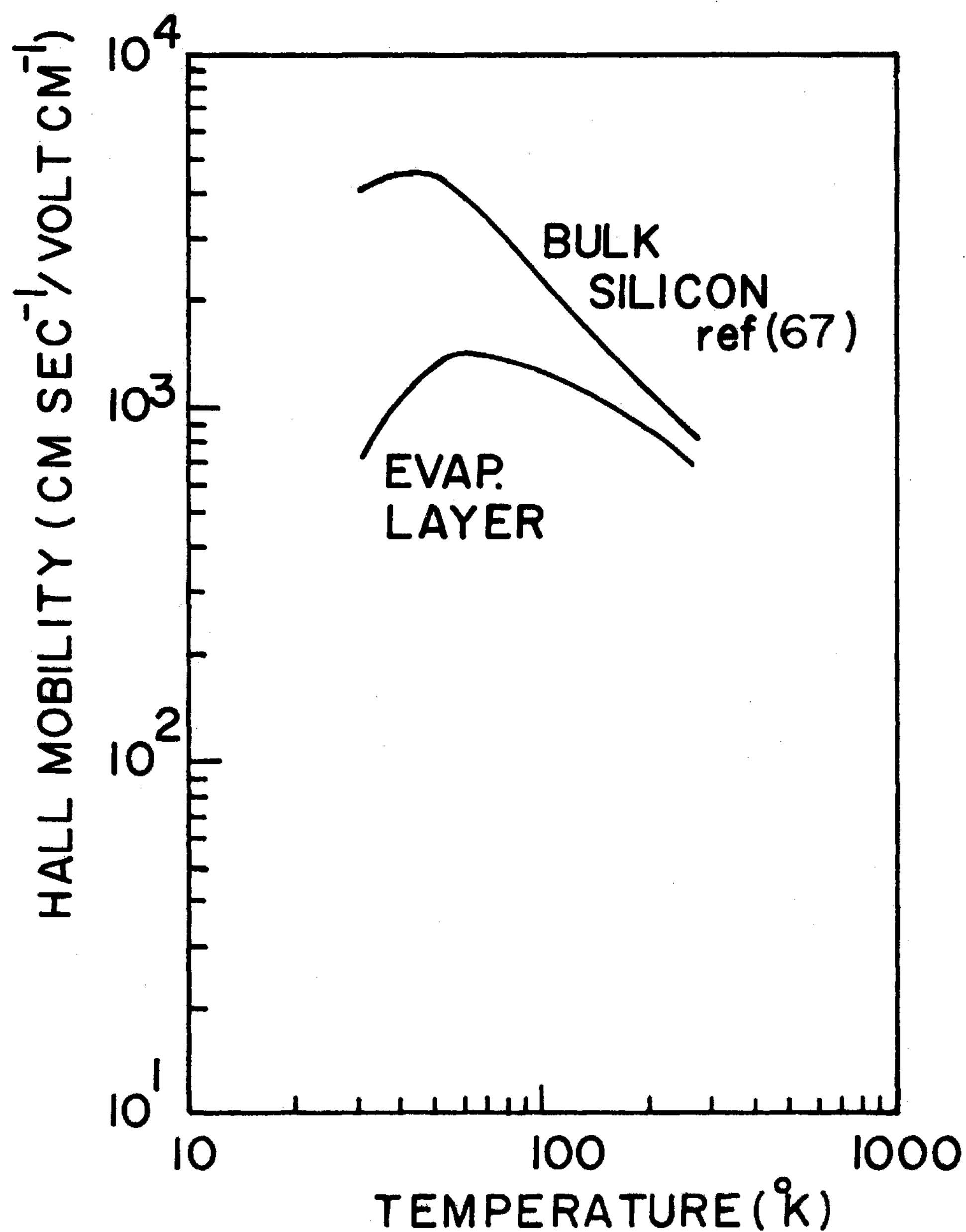


Fig.(6-5) Hall mobility for electrons in arsenic doped bulk and evaporated silicon versus absolute temperature

to be the dominant scattering mechanism indicate that the mean free path in silicon having an impurity concentration of 10^{17} atoms/cm^3 is approximately 1.5μ at 300°K. Since the thickness of the evaporated layers was less than this value, a reduction in the carrier mobility as a result of surface scattering may be expected if diffuse surface scattering is significant. However, since mobility values as high as 5×10^3 cm^2/volt-sec have been reported[71] in ion implanted layers having a thickness of only $\sim$1000 Å it appears unlikely that surface scattering was the mechanism which limited the mobility in the evaporated layers.

2) Dislocation scattering: In a semiconductor layer having a high dislocation density, the contribution of dislocation scattering may not be negligible. Theoretical expressions for the dislocation scattering have been given by Wolf.[65] Since, in the present investigation, carrier mobilities obtained in layers deposited onto Si<111> and Si<100> substrates were identical despite a factor of $\sim 10^2$ difference in their dislocation densities, dislocation scattering was presumably negligible.

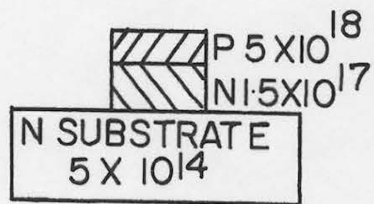
3) Compensating Centres: The reduction in carrier mobility in the evaporated layers may probably be attributed to the presence of compensating centres. For low temperatures, lattice scattering is negligible and the mobility is determined by scattering from ionized impurity centres. For sufficiently low temperatures the concentration of these centres is fixed at approximately twice that of the compensating centres. Since the gas doped layer contained a compensation centre density of $\sim 3 \times 10^{16}$/cm^3 as compared with that of $\sim 4 \times 10^{14}$/cm^3 in the bulk sample, considerably higher mobility values are observed in the latter. Theoretical considerations[65] indicate that

for a fixed concentration of ionized impurity scattering centres, the mobility should vary with temperature as $\mu \propto T^{1.4}$. The dependence of $\mu \propto T^{1.5}$ obtained for the lowest temperature region of the curve in figure (6-5) is in reasonable agreement with the theoretical prediction.

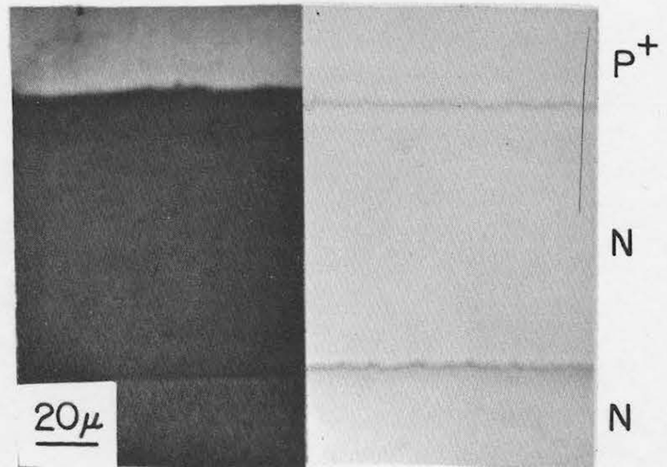
6.3 Device applications

6.3.1 All Epitaxial Diodes

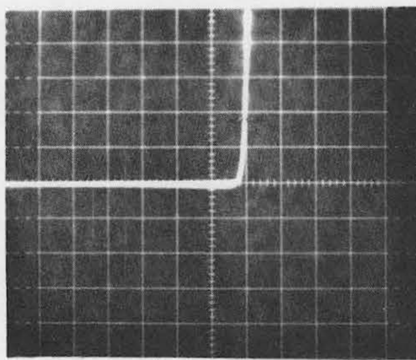
The ultimate test of a deposition-doping technique resides in its ability to produce all deposited rectifying junctions. A number of all epitaxial diodes were thus fabricated and analyzed. Since the total thickness of silicon which could be evaporated during any one deposition was limited to $\sim 1\mu$, the doping concentrations in the deposited structures were chosen to permit the diode depletion regions to remain in the deposited material for voltages up to the breakdown voltage. The structure considered consisted of a $.2\mu P^+$ (5×10^{18}) layer deposited onto a $.6\mu N(1.5 \times 10^{17})$ layer which was in turn deposited onto a 10 ohm-cm N-type substrate. Theoretical considerations[50] indicate that such a structure should possess a breakdown voltage of ~ 10 volts with a maximum depletion layer width at this voltage of $\sim .3\mu$. Figures (6-6 a,b,c) show a sketch of the deposited device, a bevelled and stained edge section and a top view of the edges of the two deposited layers. Figure (6-7) shows the current voltage characteristics of the mesa etched deposited device for forward and reverse bias. Similar characteristics for a typical commercial diffused diode having approximately the same base doping are included for comparison. Leakage currents in the two devices are seen to be comparable for small values of applied voltage (<.5 volt). The rapid increase in the leakage current of the deposited diode for larger voltages may probably be attributed to surface



(A)



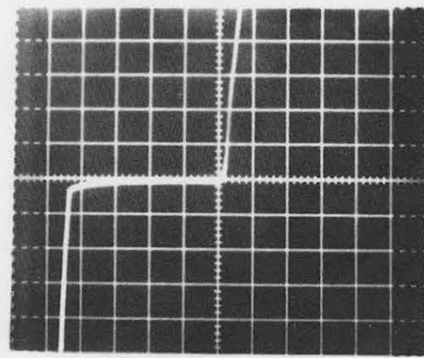
(B) (C)



0·5 VOLTS/DIV

(D)

10 μA /DIV



2 VOLTS/DIV

(E)

Fig. (6-6): (A) Sketch of all epitaxial diode

(B) Bevelled and stained edge section

(C) Top view of two deposited layers

(D) Curve tracer display for low applied voltage

(E) Curve tracer display showing breakdown voltage

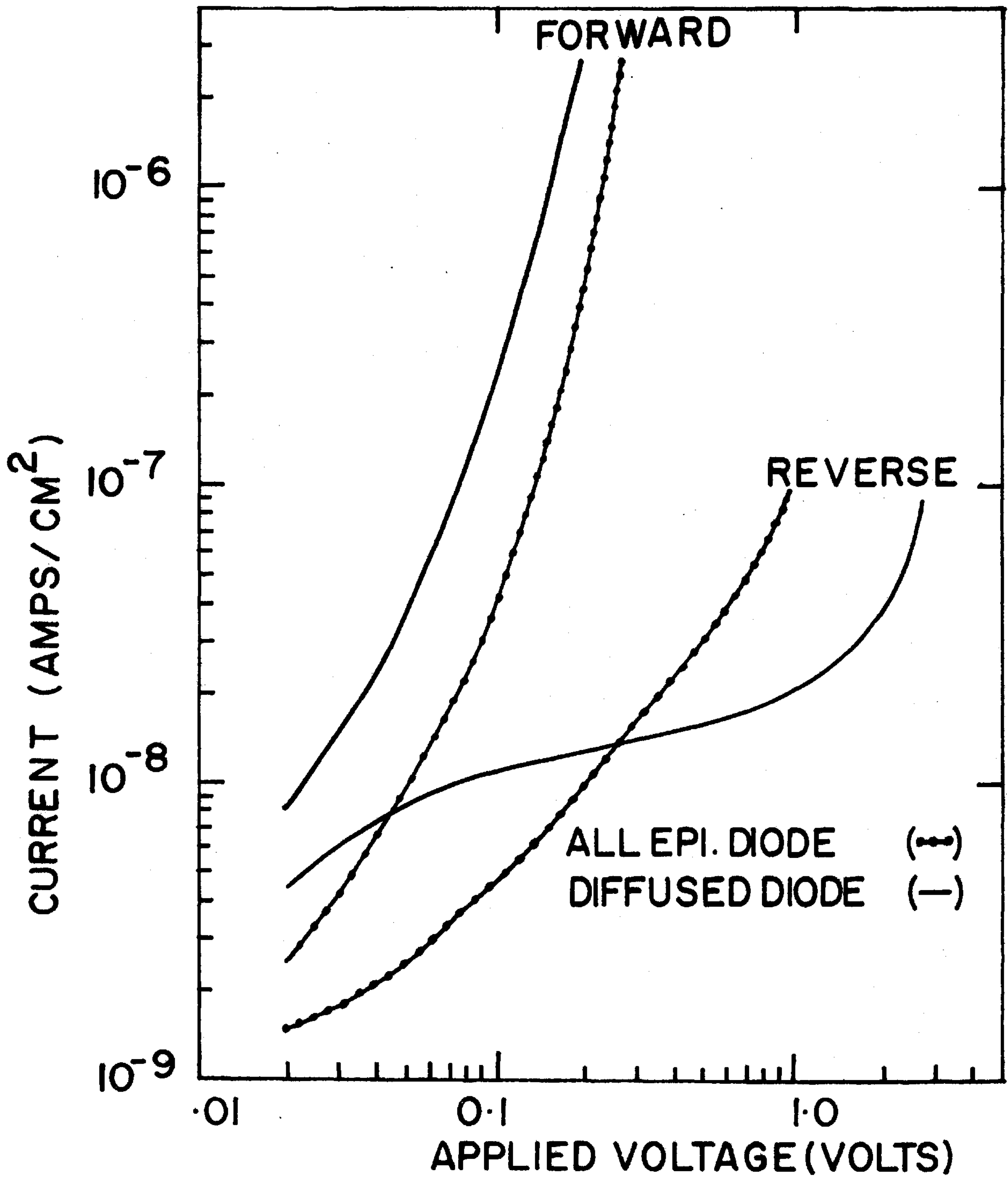


Fig.(6-7) Current-voltage characteristics in forward and reverse bias for an all epitaxial evaporated diode and for a commercial diffused diode having approximately the same base doping

leakage currents which may be significant in unpassivated mesa structures of the type employed.

Under forward bias, the current-voltage characteristic of a P-N junction may be represented[50] by an empirical expression $I = I_0(\frac{eV}{nkT})$ for $eV/nkT >> 1$. In the case of an ideal diode whose current results solely from diffusion processes, $n = 1$. In practical situations the current generated by recombination-generation centers in the diode depletion region may greatly exceed that due to diffusion. In this case $n = 2$. Values of n obtained from figure (6-7) varied from $n = 1.3$ at .075 volts to $n = 1.6$ at .15 volts. Comparable values of $n = 1.2$ and 1.4 were obtained for the diffused device. Figure (6-6 d,e) shows curve tracer plots of the device for high and low applied voltages. The rapid breakdown occurring at $\sim$9 volts is in good agreement with the theoretical prediction.

The capacitance of a P-N junction in reverse bias is proportional to $(V + V_D)^{-1/n}$, where n equals 2 or 3 for abrupt or graded junctions respectively.[50] Figure (6-8) illustrates plots of C versus V and of $\frac{1}{C^2}$ versus V for an evaporated P^+NN diode. The straight lines obtained confirm the abrupt nature of the diode profile. By employing the expression[50]

$$\frac{1}{C^2} = \frac{2}{e\varepsilon_s N_B}(V_D \pm V), \qquad (6\text{-}3)$$

derived from the theory of abrupt P-N junctions, the doping concentration in the substrate material, N_B, may be obtained. The plot in figure (6-8) yielded a value of $N_B = 1.2 \times 10^{17}/cm^3$. Both this value and the value of the intercept (.85 volts) are reasonable agreement with those calculated for the structure selected by the doping conditions.

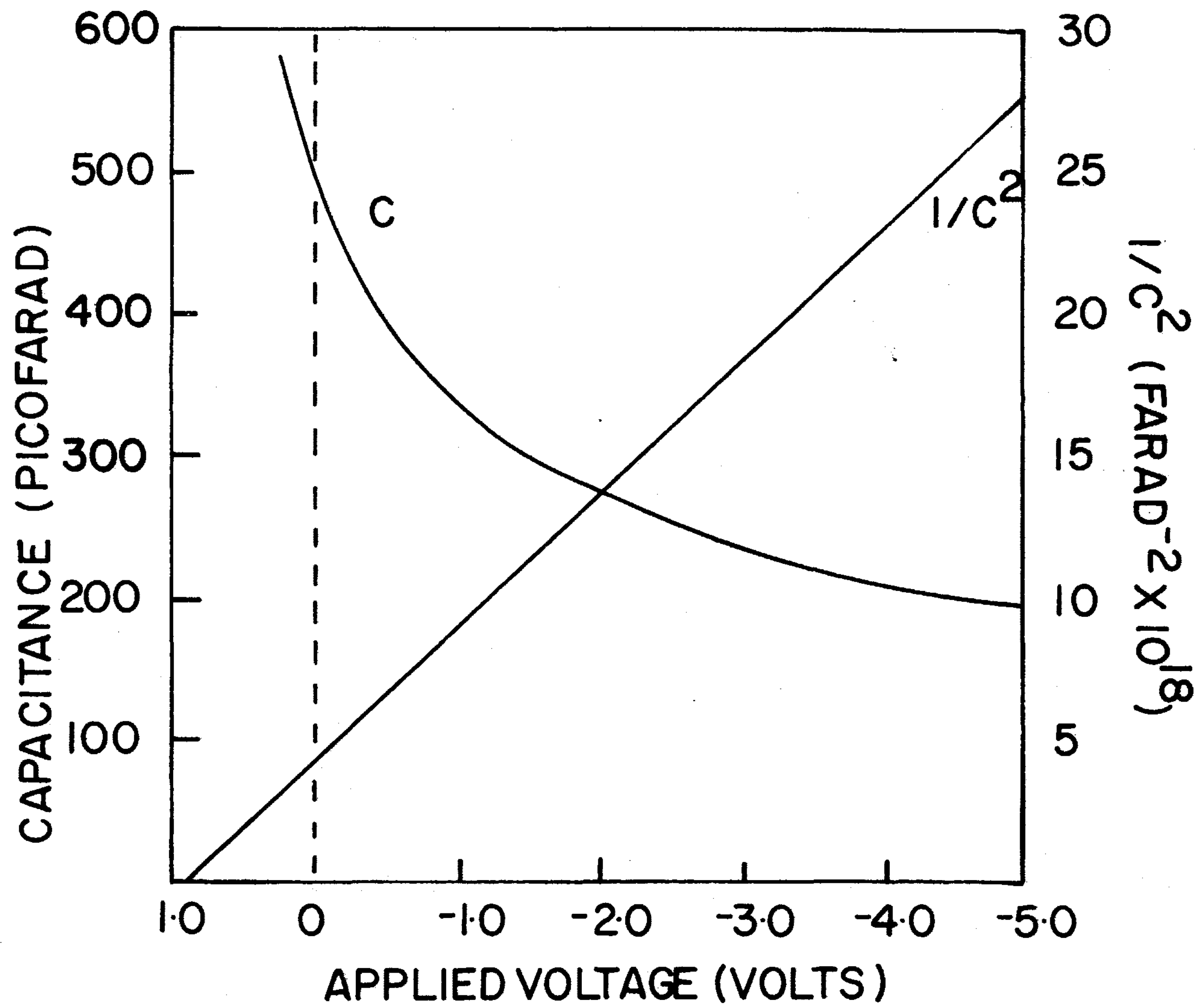


Fig.(6-8) Plots of C versus V and of $1/C^2$ versus V for an all evaporated epitaxial diode

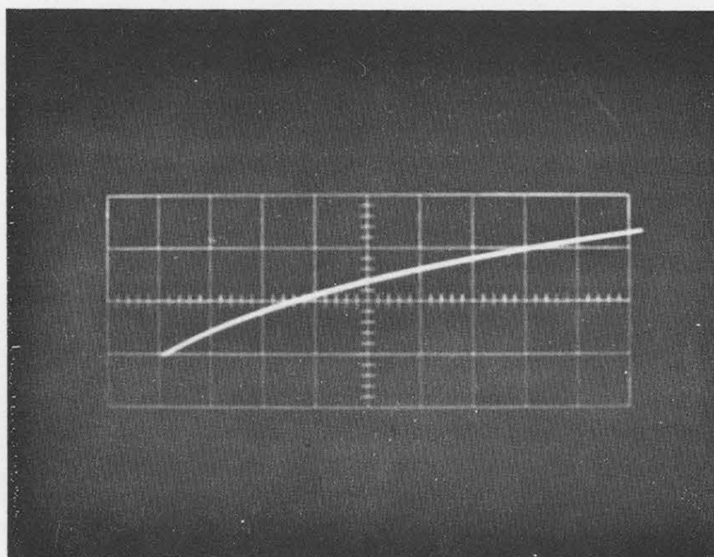
Estimates of the minority carrier lifetime in the base region of the deposited diode were obtained employing the method described by Lederhandler and Giacoletto[73] where the diode is switched from forward conduction to the open circuit condition. Measurements were made employing a Tektronix type S diode recovery module with a Tektronix 545A oscilloscope. Typical oscilloscope traces for the all epitaxial and the commercial diffused diodes are shown in figure (6-9). From the expression[73]

$$\tau_e \cong \frac{KT}{e} \frac{\Delta t}{\Delta V} \qquad t < \tau_e \tag{6-4}$$

where $\frac{KT}{e}$ = .026 volts at room temperature which gives the effective lifetime in terms of the initial voltage decay, a value of $\sim$.1μsec was obtained for the epitaxial diode. However, employing this value for the lifetime and a value of 6 cm^2/sec for the diffusivity[49] of holes in silicon containing an impurity concentration of 1.5 x $10^{17}/cm^3$ a value of 8μ was calculated for the minority carrier diffusion length ($L = \sqrt{D\tau}$). Since this value is $\sim$10 times greater than the thickness of the base region of the epitaxial diode, the majority of the injected carriers recombined in the substrate rather than in the evaporated layer. The value of $\tau_e \doteq$ .1μsec may thus not be simply interpreted as the minority carrier lifetime in the evaporated material.

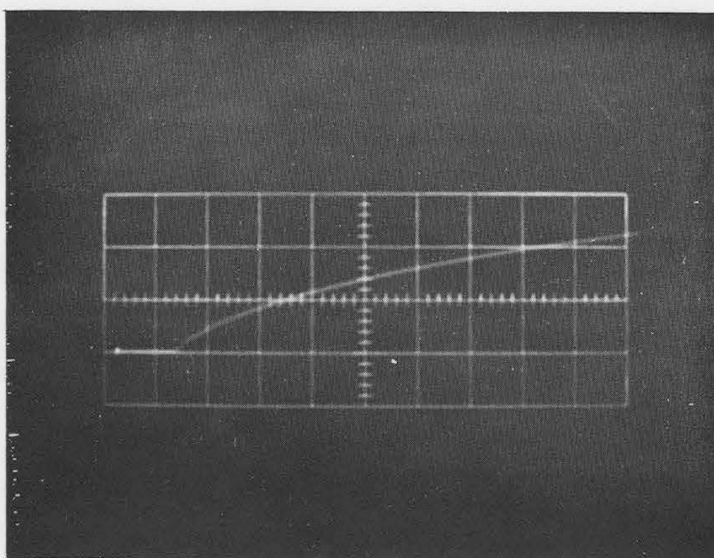
6.3.2 Substrate-Film Diodes

The electrical characteristics of a series of mesa diodes formed from evaporated P and N-type layers on substrates of the opposite doping type were investigated by making current-voltage, capacitance-voltage and minority carrier lifetime measurements.



(A)

0·05 VOLT/DIV↑ 0·1 μSEC /DIV→



(B)

Fig. (6-9): Oscilloscope traces of voltage decay characteristics for (A) all epitaxial and (B) commercial diffused diodes.

Theoretical considerations[74] indicate that, for a silicon P-N junction in reverse bias with conduction dominated by carrier generation in the depletion region, I is proportional to $(V + V_D)^{1/m}$ for $V >> \frac{kT}{e}$, where V_D is the diffusion potential. For abrupt junctions, m equals 2 while for those having a linear gradient of the doping profile in the depletion region m is equal to 3.

Figure (6-10) illustrates current-voltage characteristics obtained for evaporated P-N diodes in reverse bias. Values of m were typically 2 to 2.5 for bias voltages of .5 to 1 volt, providing an approximate indication of the abrupt nature of the evaporated junctions. Deviations from ideal behaviour may be attributed to the presence of defects and contaminating impurities in the deposited layers or,to surface leakage currents in the mesa structures considered.

I-V characteristics for evaporated P and N-type diodes in forward bias are shown in figure (6-11). Values of n were typically 1.3 over a voltage range .075 to .2 volts, indicating the presence of a large diffusion component in the forward diode current.

Breakdown voltages for P and N-type mesa evaporated diodes are illustrated in figure (6-12). On substrates of 1 ohm-cm P-type and N-type resistivity,breakdown voltages are quite sharp and agree well with those predicted from avalanche breakdown theory.[50] On higher resistivity substrates, 15 ohm-cm P-type and 8 ohm-cm N-type roll-off breakdown occurred at voltages from 120 to 180 volts. Theory predicts 330 V for P-type material and 550 V for the N-type material. The observed lower breakdown voltages result either from defects in the evaporated layers or edge breakdown in the mesa structures.

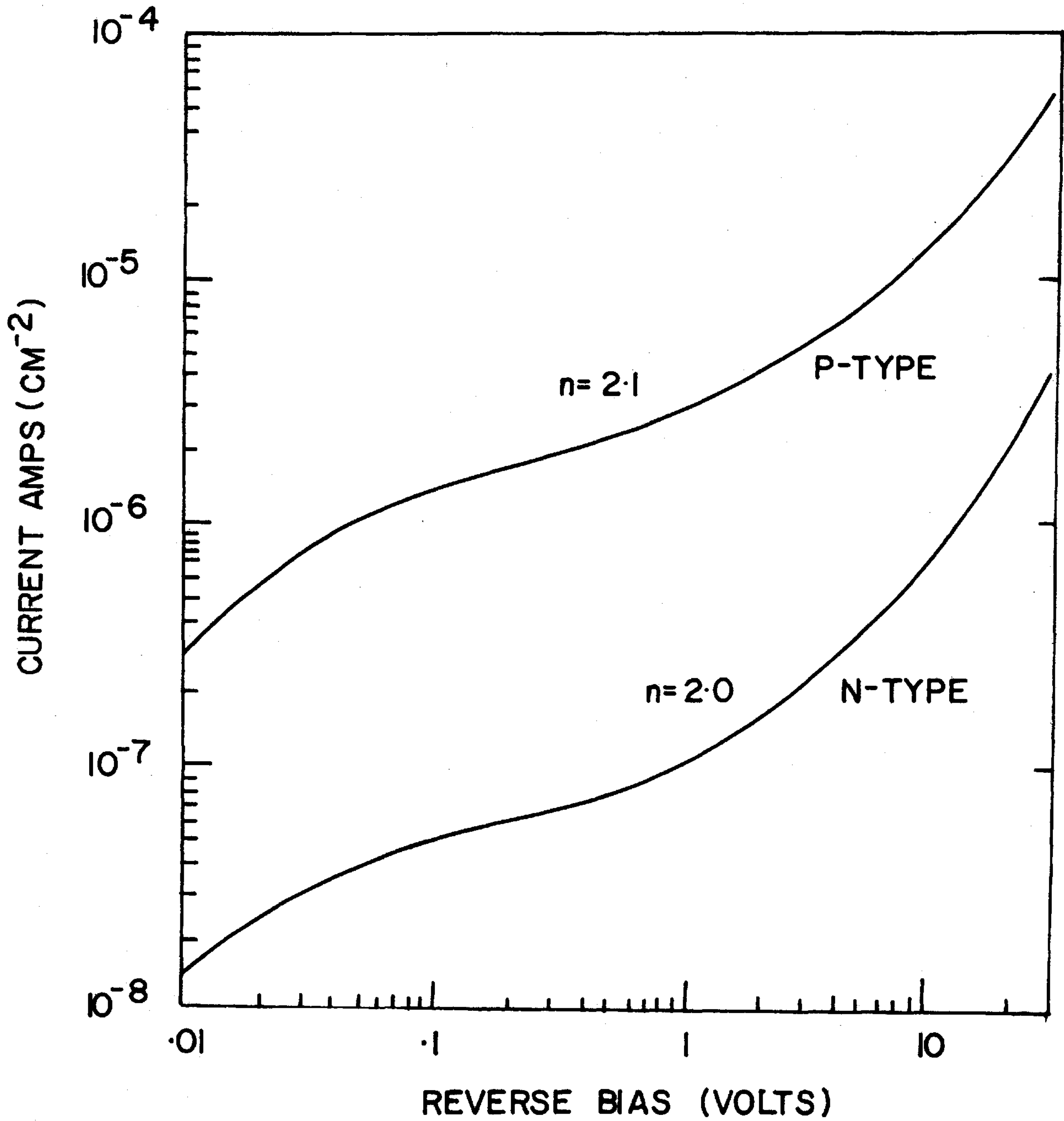


Fig.(6-10) Current-voltage characteristics for reverse biased evaporated P-N junctions. Substrate temperature 700°C

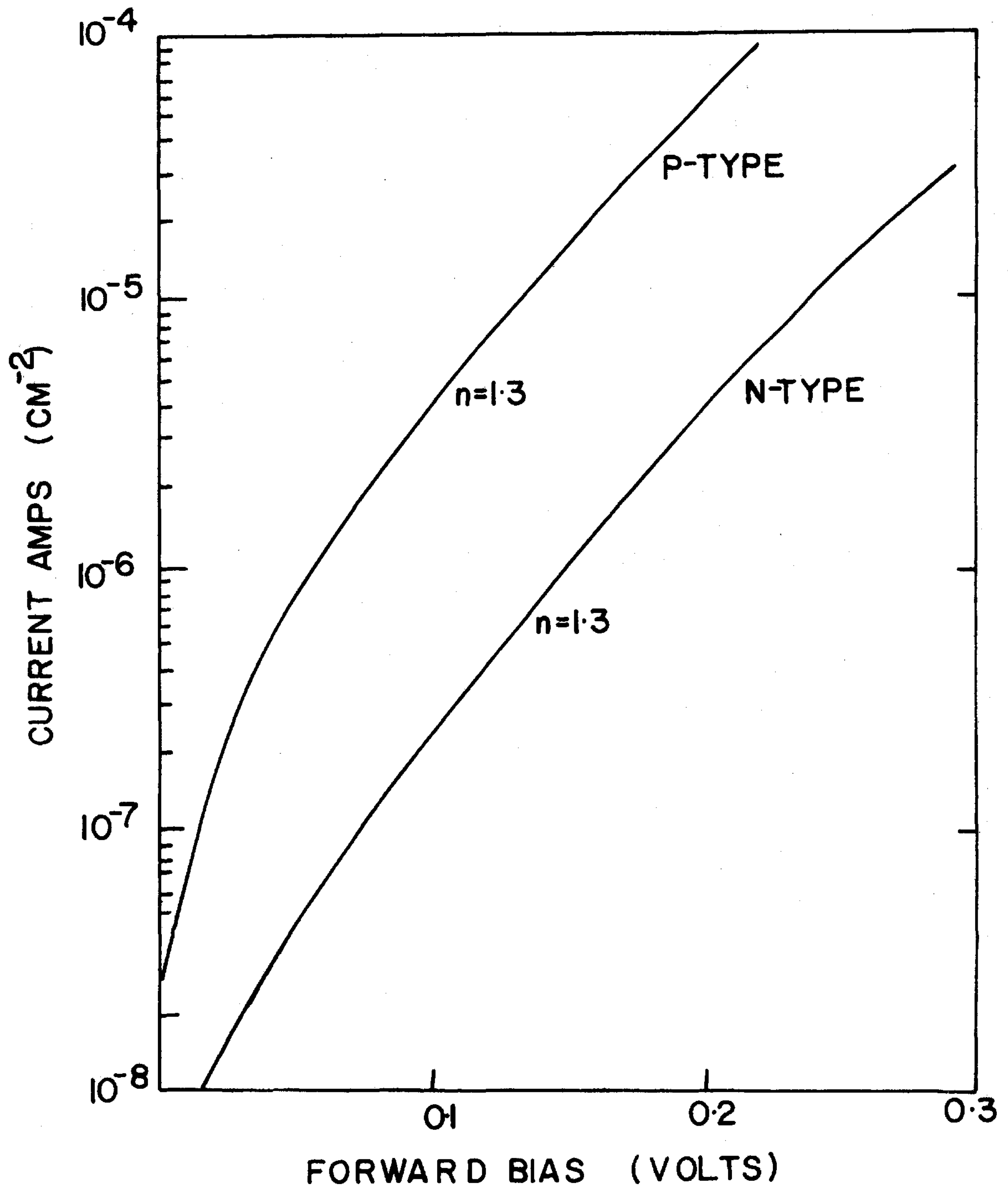


Fig.(6-11) Current-voltage characteristics for forward biased evaporated P-N junctions. Substrate temperature 700°C

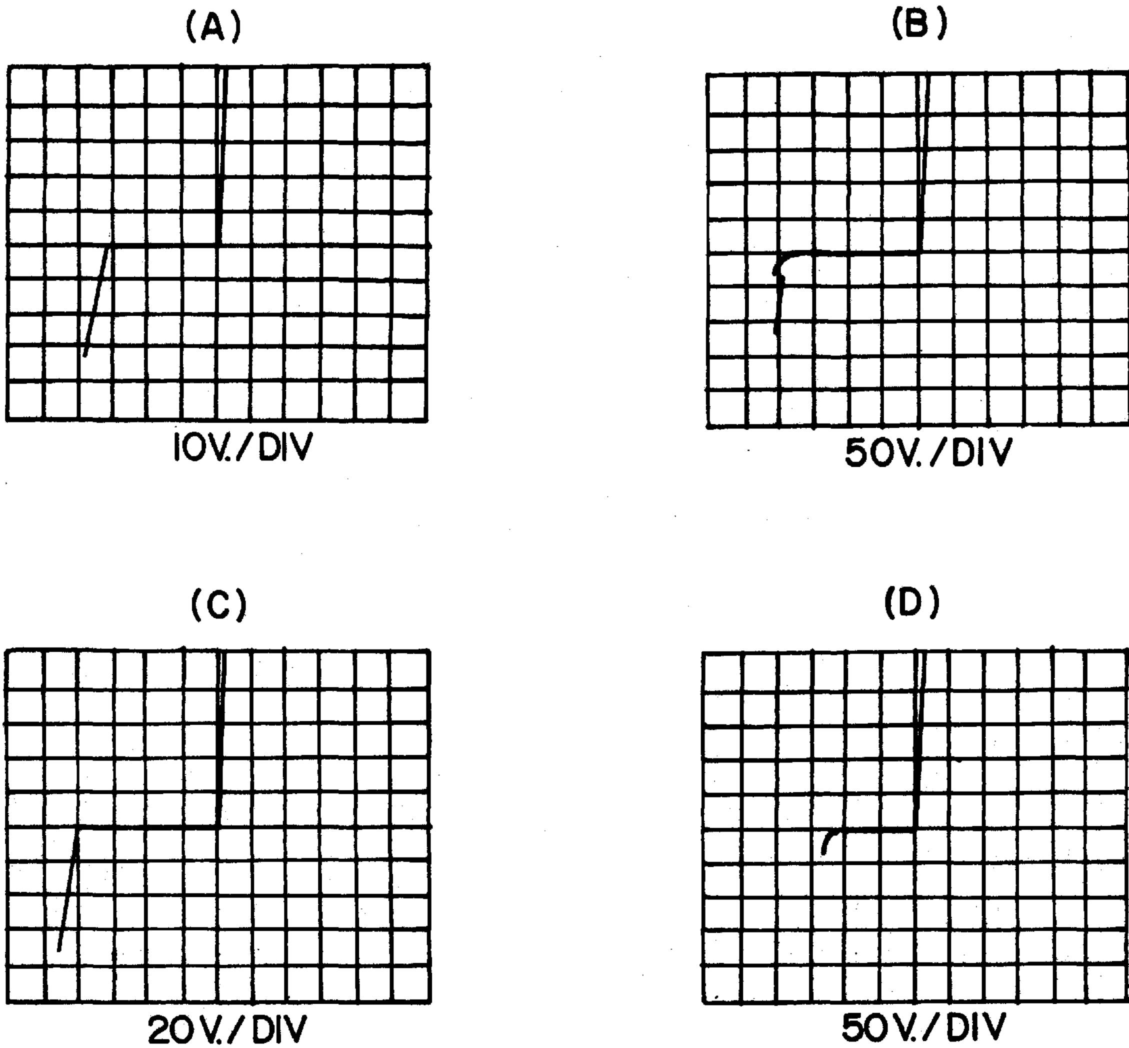


Fig.(6-12) Curve tracer displays of I-V characteristics for evaporated P-N junctions showing breakdown voltages. Current axis 10μA/div.
(A) 1 ohm-cm P-type substrate (B) 15 ohm-cm P-type substrate
(C) 1 ohm-cm N-type substrate (D) 8 ohm-cm N-type substrate

Plots of $1/C^2$ versus V for mesa diodes formed by evaporating P^+ or N^+ layers onto 6 ohm-cm N-type and 12 ohm-cm P-type substrates are shown in figure (6-13). From these plots, base carrier concentrations of $9.3 \times 10^{14}/cm^3$ and $1.2 \times 10^{15}/cm^3$ were obtained for the P^+N and N^+P diodes respectively. These values are in good agreement with those of $8 \times 10^{14}/cm^3$ and $1.1 \times 10^{15}/cm^3$ predicted from 4-point probe measurements of the substrate resistivity. The values for V_D of 0.65 and 0.43 V respectively obtained from the intercept of the $(1/C)^2$ versus V plots with the voltage axis are in poor agreement with those of 0.76 V and 0.79 V derived from approximate calculations using the known doping concentrations. The reason for these discrepancies is not known.

Typical minority carrier lifetimes of 1 to 2 μsec were recorded in the evaporated diodes for injection currents of 0.3 A/cm^2. These relatively long lifetimes indicate that the substrate material within one diffusion length of the junction contains a low concentration of trapping centres.

6.3.3 Schottky Barrier Varactor Diodes

Semiconductor junction diodes possessing highly nonlinear capacitance-voltage characteristics are widely employed in parametric amplification, harmonic generation, mixing and detection systems. The abruptness with which doping concentration may be varied limits the nonlinearity of devices produced by a particular fabrication technique.[75]

The ability of the gas-doping technique to provide abrupt changes in impurity concentration has been utilized in the fabrication of Schottky barrier varactor diodes possessing highly nonlinear capacitance-voltage characteristics. The requirement[76] in this case is for a surface layer of about .1 micron possessing a uniform carrier concentration of $3 \times 10^{17}/cm^3$,

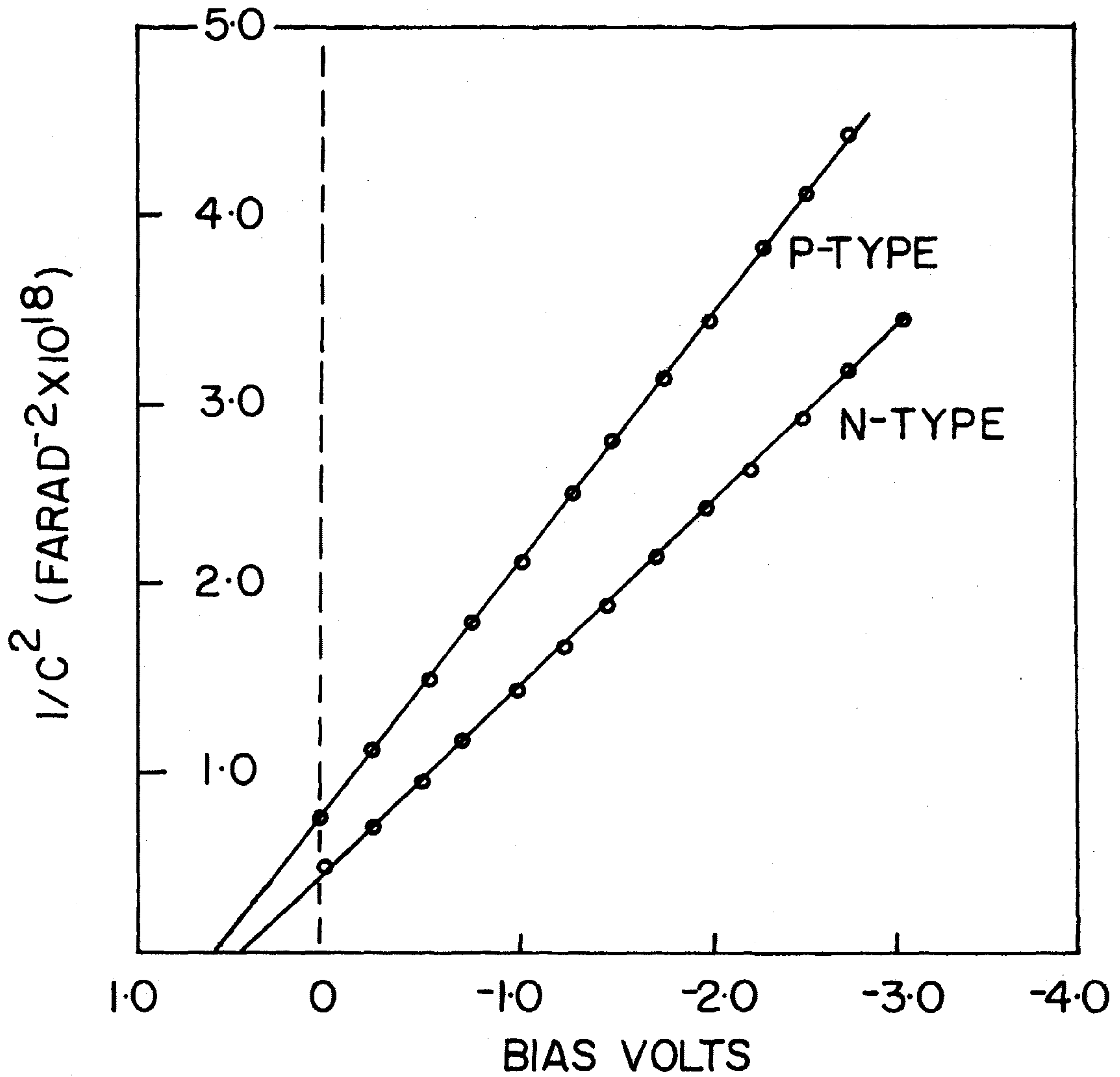


Fig.(6-13) Plots of $1/C^2$ versus bias voltage for evaporated P-N junctions

the carrier concentration afterwards dropping rapidly to that of the substrate ($<10^{15}/cm^3$). Employing 1% arsine in high purity hydrogen as a doping gas and 10 ohm-cm N-type silicon wafers as substrates a number of structures possessing this impurity profile were deposited. Schottky barriers were formed on the top surface by depositing gold dots. Ohmic contact was made to the back surface with evaporated aluminium.

The capacitance-voltage characteristics of gas-doped Schottky barrier varactors are illustrated in figure (6-14) where the capacitance, measured at 150 kHz, is plotted against the total voltage, (applied plus built-in) across the device. The built-in voltage of the gold silicon barrier was taken to be .8 volts.[50] Comparable curves obtained from the literature for diffused[75] and ion-implanted[76] varactor diodes are included for comparison. Expressing the capacitance as $C = V^n$, n values up to $n \hat{=} 20$ were obtained from gas doped structures as compared with $n \hat{=} 2$ for the ion-implanted and $n \hat{=} 1.2$ for the diffused devices illustrated. The highest n values reported in the literature have been $n \hat{=} 15$ and $n \hat{=} 7$ for varactor diodes prepared by low temperature chemical epitaxy[77] and by alloy-diffusion[78] respectively.

The approximate doping profiles of the varactor diodes were determined from the expressions[76]

$$N(x) = \frac{\bar{c}^3}{e\varepsilon A^2} \frac{\Delta v}{\Delta x} \tag{6-5}$$

$$\frac{\bar{c}}{A} = \frac{\varepsilon}{W_D} \tag{6-6}$$

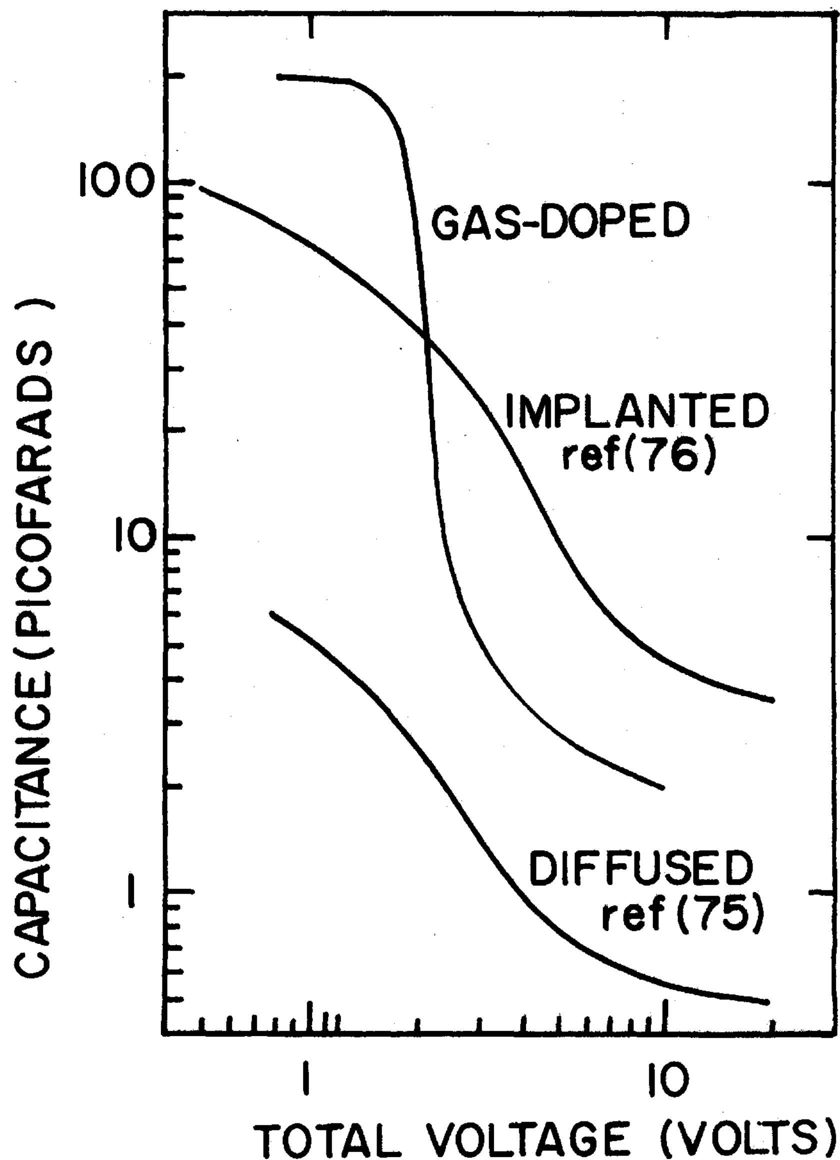


Fig.(6-14) Capacitance-voltage characteristics of hyperabrupt varactor diodes prepared by gas-doping, diffusion(75) and ion-implantation(76). The total voltage is the sum of the built-in potentail (taken to be 0.8 volts) and the reverse bias

where $\bar{c}$ = mean junction capacitance in interval Δc

Δv = increment in applied voltage

W_D = depletion region width

A = junction area

e = electronic charge

ε = dielectric constant for silicon

The impurity profile obtained from the capacitance-voltage characteristic in figure (6-14) is shown in figure (6-15) and is seen to be in reasonable agreement with that predicted from the deposition conditions.

6.3.4 Direct Energy Conversion

Shallow abrupt one sided P-N junctions of the type considered in 6.3.2 have a structure similar to that of devices conventionally employed for direct energy conversion by the beta[79] or photo[50] voltaic effect. Diodes formed by the technique of vacuum evaporation combined with gas-doping were thus evaluated for this application.

Radiation of suitable energy which impinges on a silicon P-N junction is absorbed and results in the creation of electron-hole pairs throughout the device. The distribution of electron-hole pairs will depend on the type and energy of the incident radiation. Minority carriers created by this process may diffuse to the diode depletion region and be accelerated by the built-in electric field. As a result, power may be transferred from the device to an external circuit.

Figure (6-16) shows a schematic representation of a typical energy conversion diode. The idealized I/V characteristic of such a device is given by

$$I = I_o(e^{\frac{eV}{kT}} - 1) - I_R \qquad (6\text{-}7)$$

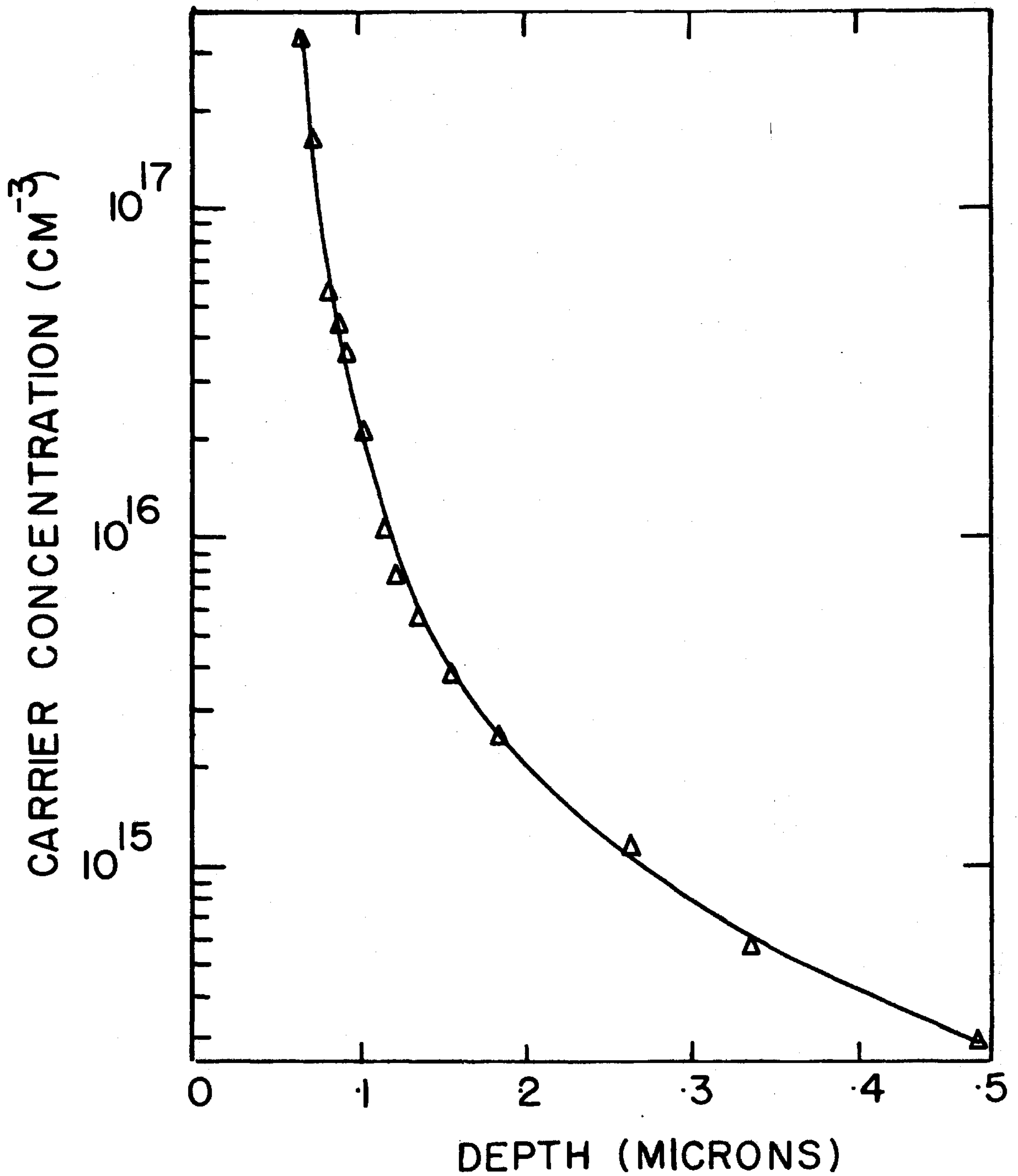


Fig.(6-15) Impurity profile in base region of gas-doped Schottky barrier varactor diode (obtained from C-V characteristic in figure (6-14)

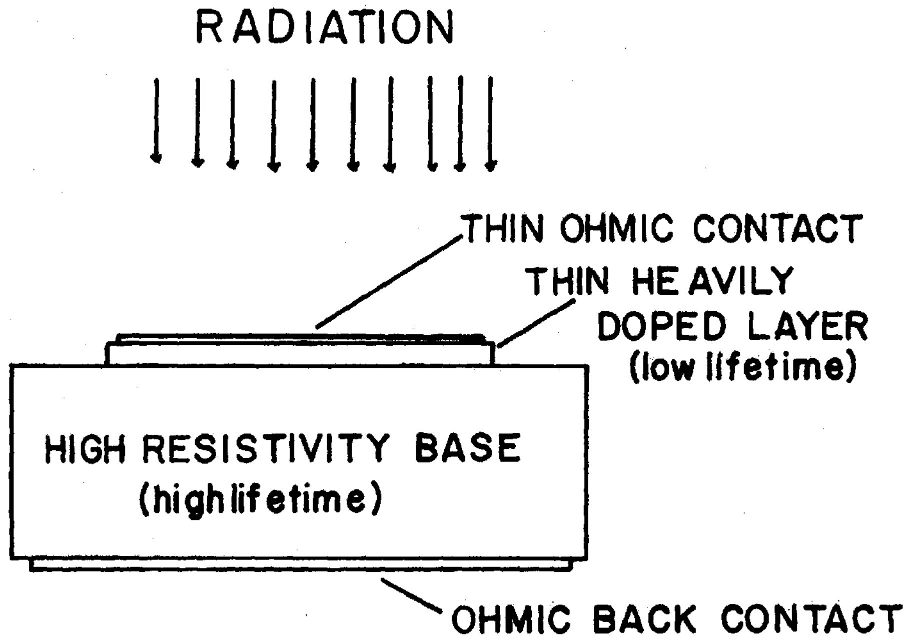


Fig.(6-16) Schematic of direct energy conversion diode

where I_o = diode saturation current

I_R = current generated by radiation

The device is generally characterized by two parameters (1) the short circuit current $I_{SC} = I_R$ and (2) the open circuit voltage V_{oc}. The latter may be obtained by setting I = 0 in (6-7)

$$V_{oc} = \frac{kT}{e} \ln(\frac{I_L}{I_S} + 1) \qquad (6\text{-}8)$$

The practical structure selected represents a compromise between the need to possess a diode having a high built-in voltage and the need to minimize the number of radiation induced minority carriers which recombine before reaching the junction. The top layer of the diode is heavily doped and thus contributes to a high built-in voltage. However, since heavily doped silicon in general, possesses a short minority carrier lifetime, few of the carriers created in this layer will reach the junction. The base region of the diode has a high resistivity ($\sim$10 ohm-cm) and a long minority carrier lifetime. The top layer of the diode is made sufficiently thin to allow most of the impinging radiation to pass through and be absorbed in the base region. Devices fabricated for energy conversion by high energy radiation generally possess an N^+P rather than a P^+N structure since it has been shown that P-type silicon is less susceptible to lifetime degrading radiation damage.[79]

The evaporation gas-doping technique offers, in principal, several advantages in the fabrication of energy conversion devices. The low processing temperature should minimize diffusion of lifetime killing trapping centers into the base region during the fabrication process. The low lifetime top layer of the diode may be made arbitrarily thin to reduce losses in this

region. N^+P junctions formed by evaporating 2500 Å arsenic or phosphorus doped layers onto 10 ohm-cm P-type Si<100> substrates were evaluated as direct beta-voltaic energy convertors. The diodes had an area of ∿0.5 cm^2 and were delineated by masking part of the evaporated layer with black wax and etching in 20 HNO_3:1 HF for ∿30 secs. Low resistance ohmic contacts were made to the devices by evaporating 200 Å of titanium followed by 1500 Å of silver onto the front surface and 3000 Å of aluminium onto the back surface. These contacts were sintered for 10 mins. at 450°C in vacuum before etching and electrical evaluation.

The radiation source consisted of a layer of Promethium 147 deposited onto a stainless steel plate. This isotope provides beta particles having a spectrum of energies up to ∿233 keV. The source strength was approximately 1.4 curies/cm^2. The diodes were placed directly on the source, front contact being made by means of a 1 mil gold wire stretched across the surface.

Typical results for gas-doped diodes are shown in table (6-1). Corresponding results obtained from a standard N^+P phosphorus diffused diode on the same source are included for comparison.

While the gas doped energy conversion diodes are seen to provide values of short circuit current which are comparable with those of the diffused device, values of open circuit voltage are some 30% lower than those of the diffused structure.

The reduced open circuit voltages in the evaporated diodes as compared with the diffused device may be attributed to the some of the following differences in the two strucutres:

(1) Since leakage currents in the evaporated diodes are greater than those in the diffused device, equation (6-8) predicts that the latter should

No.	Base Resistivity ohm-cm	Top layer conc./cm^3	Leakage at 1 volt reverse bias amps/cm^2	Effective lifetime μs	O.C.V. volts	S.C.C. μA/cm^2
AS7	10	1.5×10^{18}	7×10^{-7}	1	.23	27
AS8	10	1.5×10^{18}	5×10^{-7}	1	.24	26
PH4	10	2×10^{19}	1×10^{-6}	3	.21	25
PH9	10	2×10^{19}	2×10^{-6}	2	.21	26
Diffused Diode*	5-10	$\sim 10^{20}$	5×10^{-8}	4	.35	30

Table (6-1)

Properties of Evaporation Gas-Doped and Diffused Beta Voltaic Energy Conversion Diodes

*obtained from Atomic Energy of Canada Limited

possess a higher open circuit voltage.

(2) The doping concentration in the top layer of the diffused diode is some one to two orders of magnitude greater than that in the phosphorus and arsenic gas-doped layers. The diffused device will thus possess a higher built-in voltage.

(3) Diffusion of lifetime killing trapping impurities from the heater materials into the base region of the gas-doped devices may be appreciable even at 700°C. Since the phosphorus diffusion process has a gettering effect on these impurities[80], the diffused devices, despite their higher processing temperature, may possess a longer base minority carrier lifetime.

(4) Since the evaporated silicon probably contains a higher concentration of electrical imperfections than are present in the diffused material, minority carrier recombination in the depletion region of the gas-doped diodes may be much greater than that in the diffused device.

6.4 Summary

In this chapter the electrical characteristics and device applications of homoepitaxial silicon thin films vacuum evaporated onto non heat-treated substrates have been considered. Films evaporated with no intentional doping from 100 ohm-cm P-type source material have been found to be N-type and to possess resistivities of $\sim$5 ohm-cm. Room temperature carrier mobilities in both P and N-type films have been found to be comparable with those of bulk single crystal silicon over the range 10^{17} - 10^{19} carriers/cm^3. Mobilities in N-type films having carrier concentrations from 10^{16} to 10^{17}/cm^3 have been found to be approximately 10% less than those in the

bulk material. Room temperature mobilities as high as $\sim$1000 cm^2/volt-sec have been observed in N-type layers having carrier concentrations of $\sim 1 \times 10^{16}/cm^3$.

While the resistivity and mobility values quoted above are adequate as starting values for the fabrication of most silicon devices, the presence both of resistivities in undoped films which are less than those of the source material and of reduced carrier mobilities in low doped N-type layers indicate the presence of electrically active contaminating centres in the deposited material. Furthermore, temperature dependent Hall effect measurements have shown N-type gas-doped layers to contain compensation centre densities of $\sim 3 \times 10^{16}/cm^3$. The presence of unwanted doping impurities and of compensating centres in the deposited material may be attributed either to carry-over doping, to contamination by the electron gun and heater materials or to residual gases in the vacuum chamber. It is expected that modifications in the system which eliminate these sources of contamination should permit films whose electrical characteristics are identical to those of bulk high purity single crystal silicon to be deposited.

The technique of vacuum evaporation combined with gas doping has been employed in the fabrication at 700°C both of all epitaxial silicon diodes and of devices formed by evaporating P or N-type material onto substrates having the opposite doping type. The characteristics of those devices, while probably to some extent degraded by electrical imperfections in the deposited layers, have been found to be comparable with those exhibited by standard diffused devices.

The ability of the gas-doping technique to provide abrupt changes in impurity concentration has been utilized in the fabrication of hyper-

abrupt Schottky barrier varactor diodes possessing highly non-linear capacitance voltage characteristics. Diodes fabricated by the deposition doping technique have been evaluated as beta-voltaic direct energy convertors.

CHAPTER VII

SILICON FILMS ON SiO_2 SUBSTRATES

7.1 Introduction

Structurally disordered silicon films obtained by deposition onto SiO_2 substrates possess electrical characteristics which,in general, differ widely from those exhibited by bulk single crystal silicon. A number of these characteristics, combined with the obvious compatibility of such films with conventional silicon technology, are of interest in the fabrication of semiconductor devices. In this chapter the structure and electrical characteristics of silicon films vacuum evaporated onto SiO_2 substrates are considered. Properties of polycrystalline silicon relevant to device formation are reviewed and the suitability of this material for the fabrication of thin film resistors for monolithic integrated circuits considered.

7.2 Review: Silicon films on amorphous substrates

The structure and electrical characteristics of silicon films deposited onto amorphous substrates have been considered by a number of authors. Deposition techniques have included vacuum evaporation,[81-83] sputtering,[84] chemical vapor transport[85-90] and R.F. gas decomposition.[91] In general, for substrate temperatures less than 500°C the deposited films are observed to be amorphous. Amorphous silicon films are characterized both by high resistivity and by a relative insensitivity to dopant impurities. The structure and electrical characteristics of amorphous semiconductor films have been extensively studied.[92]

For substrate temperatures in excess of 500°C the deposited silicon films are generally found to possess a polycrystalline structure and to exhibit both a decreased resistivity and an increased sensitivity to dopant concentrations. Carrier mobilities measured in polycrystalline layers are considerably less than those observed in bulk silicon and do not exhibit the same form of dependence on doping concentration as is observed in the bulk material.

The structure and electrical characteristics of deposited polycrystalline silicon have been found to depend strongly on the particular system and deposition parameters employed. Table (7-1) shows briefly some of the properties of polycrystalline silicon films as described by a number of authors and illustrates the considerable variety of results obtained in different deposition systems. Studies of the properties of vacuum deposited polycrystalline silicon films have been complicated both by contamination and by the inability to reproducibly introduce controlled concentrations of doping impurities into the depositing layers.

In the present system, the ability to deposit contamination-free silicon films possessing controlled doping concentrations has been demonstrated. To extend the study of the suitability of silicon vacuum evaporation techniques for device applications, the structure and electrical characteristics of gas-doped polycrystalline films deposited onto SiO_2 substrates were investigated. Both for purposes of comparison and, to enable concentrations outside the range of the gas-doping technique to be obtained, doped polycrystalline films obtained by diffusion of undoped evaporated films were also considered.

Table(7-1): Survey of properties of silicon films deposited onto amorphous substrates

AUTHORS	Deposition Technique and Substrate	Temperature Range (°C)	Film Structure and Preferred Orientation	Minimum Resistivity (Ω-cm)	Doping Technique	Doping Type and Concentration (carriers /cm^3)	Typical Hall Mobility (cm^2/volt sec)
Kataoka[81]	Vac. Evap. on fused quartz and annealed	950-1050	Polycrystal <111> Preferred	~ 10^2			120
Mountvala[82] Abowitz	Vac. Evap. on fused quartz	500 900 1000	Amorphous <110> Preferred <110> to <111> Preferred	$1.3x10^{-1}$	Evap. P and N doped Silicon	P-type only found	
Collins[83]	Vac. Evap. on fused quartz	25-1000	Amorphous to Polycrystal	.02	Boron from Crucible	P	
Kumagai,[84] Thompson, Krauss	Sputter on fused quartz	50-400 Annealed 600-1000	Amorphous Polycrystal	10^4 .1	Sputter P and N doped Silicon	P-type only found	
Ford,[86] Thomas, Laverty	Chem. Vap. SiH_4 in He on SiO_2	500-750	Polycrystal grain size 50-5000Å	5 .1	Chem. Vap.	P only at 10^{18} P,N-$3x10^{20}$	10 .1
Cowher,[87] Sedgwick	Chem.Vap. SiH_4 in H_2 $SiBr_4$ in H_2 on SiO_2	650-750 700-850	Polycrystal	Undoped > 10^5 Doped, $5x10^{-2}$	Chem. Vap.	P-$2x10^{18}$ to $5x10^{19}$ N-10^{14} to 10^{20}	20 to 10 $5x10^3$ to 70
Sirtl,[88] Seiter	Chem. Vap. (CH_3) $SiHCl_2$: Si HCl_3 in H_2	1100	Polycrystal	5.8	Chem. Vap.	N only $7.4x10^{16}$	15 - 34
Bean,[96] Hentzschel, Colman	Chem. Vap. $SiHCl_3$ $SiCl_4$ SiH_4 on SiO_2	1100 1200 930	Polycrystal	$6.5x10^4$ $1.4x10^5$ $8.9x10^3$		$>10^{14}$ $3.3x10^{13}$ $>10^{14}$	<1 1.4 <1
Joseph,[89] Kamins	Chem. Vap. SiH_4 in H_2 on SiO_2	650-1050	Polycrystal	$1.2x10^6$ to $4x10^5$			
Mai,[90] Whitehouse, Thomas, Goldstein	Chem. Vap. SiH_4 in H_2 : N_2 on Silicon Nitride	800 900-1000	Random Polycrystal <111> and <220>		Boron Diffused at 1050°C	P	Mean Value .57 x bulk mobility
Kamins[85]	Chem. Vap. SiH_4 in H_2 on SiO_2	1035	Polycrystal	P-$6x10^{-3}$ N-10^{-2}	Chem. Vap. or diffusion	P-10^{17} to 10^{20} N-10^{16} to 10^{19}	8 at 10^{17} holes/cm^3 45 at 10^{18} " 35 at $3x10^{19}$ " 3 at 10^{16} electrons/cm^3 30 at 10^{18} electrons/cm^3 20 at 10^{19} electron/cm^3

7.3 Experimental

The evaporation techniques and materials employed in depositing silicon thin films onto SiO_2 substrates have been considered in chapter (3). The structures of the deposited films were examined employing HEED and scanning electron microscopy. Their electrical characteristics were determined employing Hall effect, conductivity and T.C.R. measurements. Contacts for Hall effect and conductivity measurements were made using evaporated aluminium and proved to be ohmic over the current ranges considered.

The evaporated films were doped either during deposition by the gas-doping technique or after deposition and removal from the system by diffusion. The diffusion process involved covering with a chemically-deposited phosphorus rich glass at 325°C, a capping with undoped oxide, and a subsequent diffusion drive (900-1050°C) in dry N_2 for 160 min.

7.4 Experimental results and observations

7.4.1 Structure

Evaporated gas-doped films were investigated for the substrate temperature range 600°C to 850°C. Since continuous films were obtained for substrate temperatures throughout this range, reaction of the impinging silicon with the oxide layer, as considered in chapter (4), was minimal. Electron diffraction reflection analysis indicated random polycrystalline films from 600°C to 730°C with a preferred orientation in the <111> direction, as predicted by nucleation theory, appearing above 730°C. The diffraction patterns showed both the structure and the lattice constant of crystalline silicon. Fig. (7-1) illustrates diffraction reflection patterns and the corresponding micrographs obtained from films evaporated

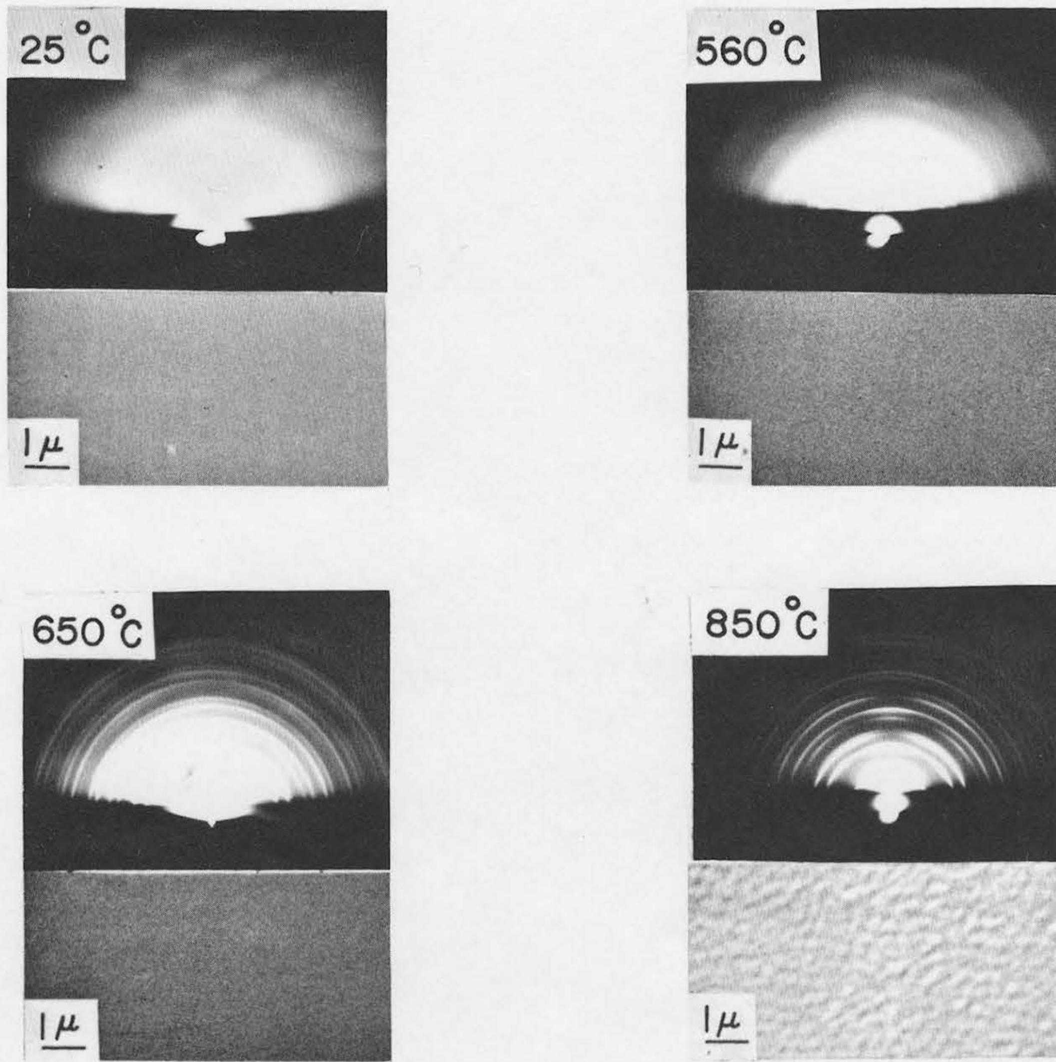


Fig. (7-1): HEED and scanning electron micrographs obtained from 2500 Å silicon films vacuum evaporated onto SiO_2 substrates having temperatures 25°C, 560°C, 650°C and 850°C.

at 25°C, 560°C, 650°C and 850°C respectively.

In the course of initial investigations it was observed that the high temperatures in the diffusion process were sufficient to induce by annealing significant recrystallization in amorphous silicon. Doped polycrystalline layers could thus be produced in a single step from silicon films previously evaporated onto unheated substrates. Such unheated substrate "diffusion-annealed" films eliminate the added process complexity of a heated substrate and are therefore of particular interest for practical applications. Electron diffraction microscopy performed on these diffused layers yielded patterns indicative of small grained randomly oriented polycrystalline silicon, the ring patterns becoming more clearly defined with increased diffusion temperature. Fig. (7-2) shows the electron diffraction-reflection pattern and corresponding micrograph obtained in diffusing 2500 Å of amorphous silicon at 1050°C.

7.4.2 Electrical characteristics

Resistivities observed the polycrystalline silicon films ranged from $>10^4$ ohm-cm in undoped evaporated layers to $<10^{-3}$ ohm-cm in films possessing the highest doping concentrations. Carrier concentrations up to 5×10^{19} / cm^3 (as determined by the Hall effect measurements) were obtained by varying the partial pressure of doping gas present in the system during the evaporation. Average carrier concentrations from $5 \times 10^{18}/cm^3$ to $5 \times 10^{20}/cm^3$ were obtained by diffusing at temperatures between 900°C and 1050°C.

Fig. (7-3) illustrates a plot of Hall mobility versus deposition temperature for a series of P and N-type gas-doped films of thickness 2500 Å possessing constant doping concentrations. The mobility is seen to

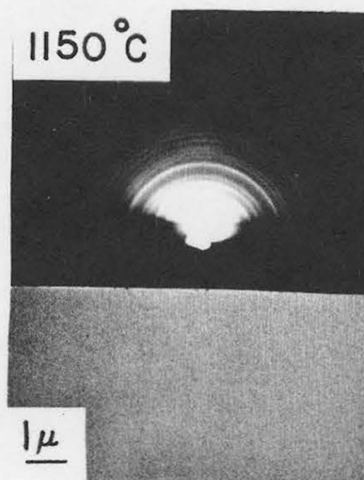


Fig. (7-2): HEED and scanning electron micrographs obtained from 2500 Å silicon film diffusion-annealed at 1050°C.

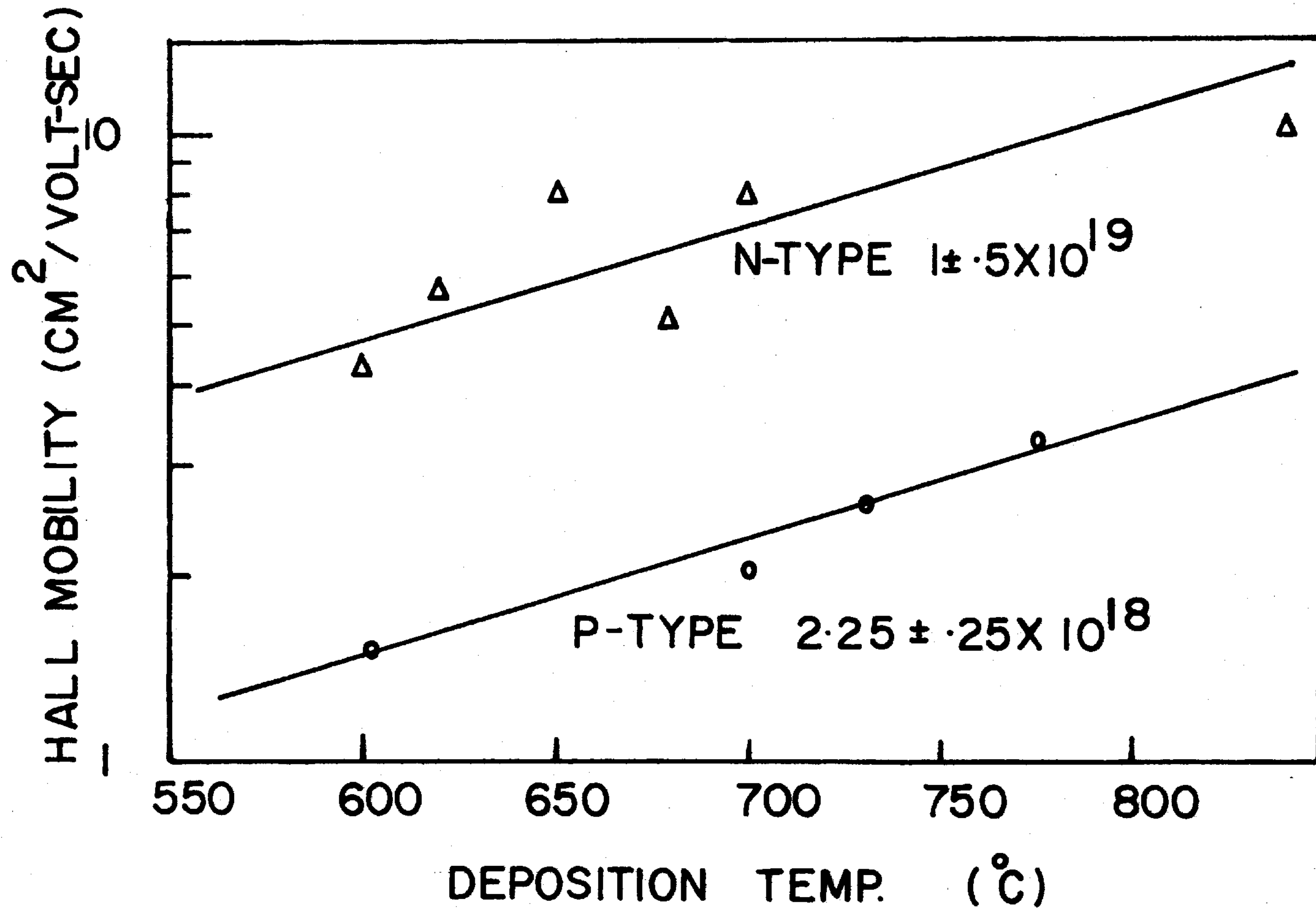


Fig.(7-3) Plots of Hall mobility versus substrate temperature for P and N-type polycrystalline silicon films possessing constant carrier concentrations. Film thickness 2500Å

increase with increasing substrate temperature as a result of the increasing order in the deposited layers. In films having a mean thickness of 2500 Å, crystallite size, as estimated from electron micrographs, ranged from ∿300 Å to ∿2000 Å as the substrate temperature was increased from 650°C to 850°C.

Fig. (7-4) illustrates a plot of Hall mobility versus carrier concentration in a series of 2500 Å films deposited at 730°C. A plot of conductivity mobility versus carrier concentration observed in bulk P-type material is included for comparison.[64] In contrast with the behaviour observed in bulk silicon, the mobility in the polycrystalline layers is seen to increase with increasing carrier concentration over the range considered. Similar effects have been observed in polycrystalline films chemically deposited at 1030°C by Kamins[85] who obtained a mobility peak at approximately 10^{18} carriers/cm^3. The non-occurrence of a peak and the overall lower mobilities observed in the vacuum evaporated gas-doped polycrystalline films as compared with those of Kamins may be ascribed to the smaller crystallite size resulting from the lower deposition temperatures and thinner films employed.

The carrier concentrations,resistivities and mobilities determined in a series of films evaporated onto substrates having temperatures 25°C, 600°C, 730°C and 810°C and subsequently diffused for 160 mins at 1050°C are shown in table (7-2). The final values obtained for the electrical parameters are seen to be virtually independent of the initial deposition temperature.

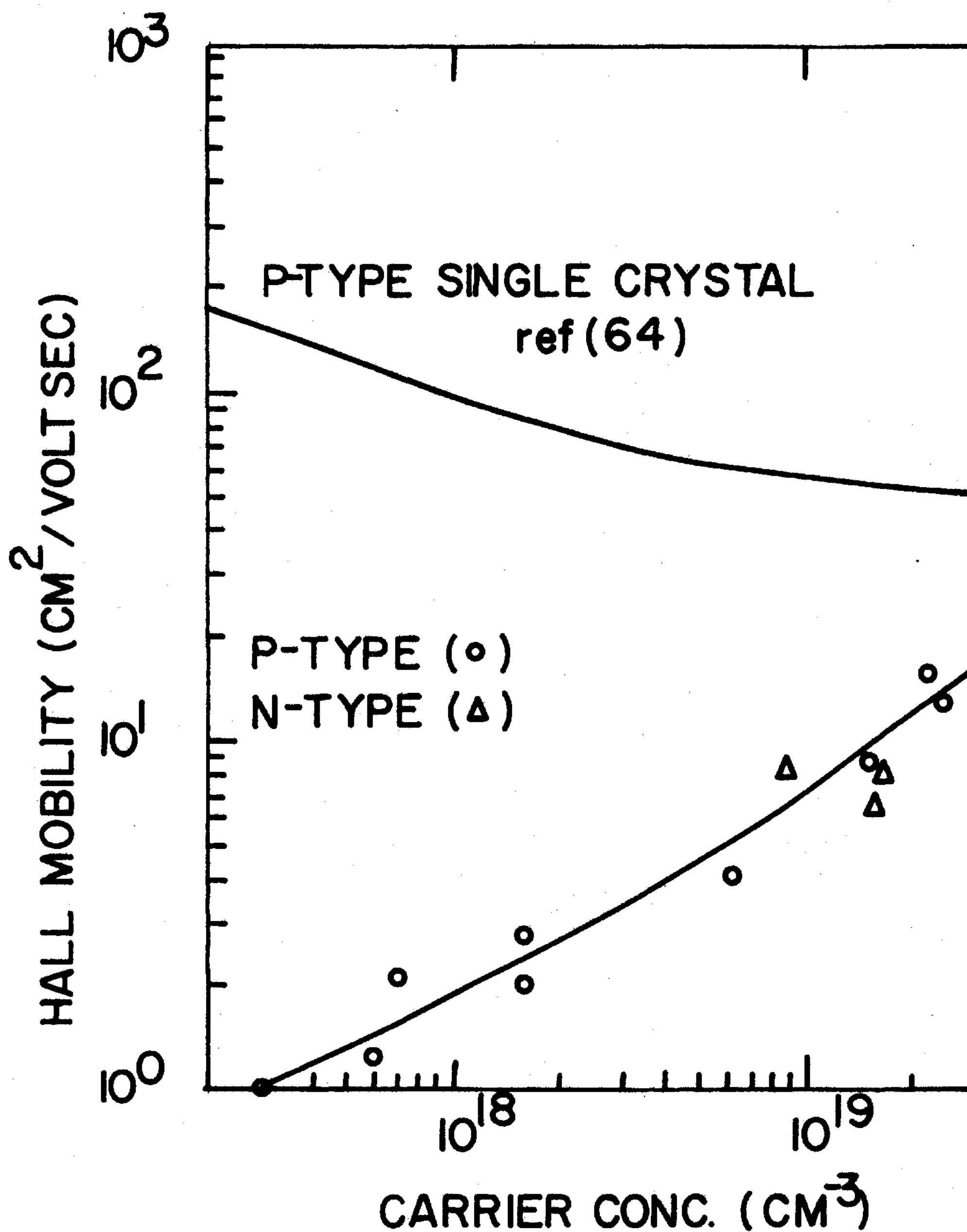


Fig.(7-4) Plot of Hall mobility versus carrier concentration for P and N-type polycrystalline silicon films evaporated onto SiO_2 substrates having temperatures of 730°C. A plot of the conductivity mobility versus carrier concentration observed in P-type single crystal silicon is also shown

Table (7-2)

Sheet Resistivities, Hall Mobilities and Carrier Concentrations in 2500 Å Silicon Films Evaporated onto Substrates Having Temperatures from 25°C to 810°C and Subsequently Diffused for 160 min. at 1050°C.

Sample Number	Thickness Å	Substrate Temp. °C	After Diffusion Sheet Resis. Ohms/□	Mean Carrier conc/cm^3	Mean Mobility cm^2/volt-sec
POX4	2500	25	34.1	3×10^{20}	24
POX10	2500	600	23.8	4.1×10^{20}	25
POX11	2500	730	24.5	4.0×10^{20}	25
POX9	2500	810	30.8	3.6×10^{20}	22

Fig. (7-5) illustrates mean carrier concentrations and Hall mobilities determined in a series of 2500 Å amorphous films diffused at temperatures between 900°C and 1050°C. The highest values of Hall mobility in any polycrystalline deposits were observed in the most heavily doped diffused films, despite their relatively low crystalline order. Again, this demonstrates the strong dependence of Hall mobility on carrier concentration similar to that seen with the gas-doped films. The electrical properties of the diffused films were comparable to N-type gas-doped films having similar structural properties and carrier concentrations.

7.4.3 Temperature coefficient of resistance (T.C.R.)

T.C.R.'s in doped polycrystalline silicon are of importance not only in practical applications but also in understanding the electrical

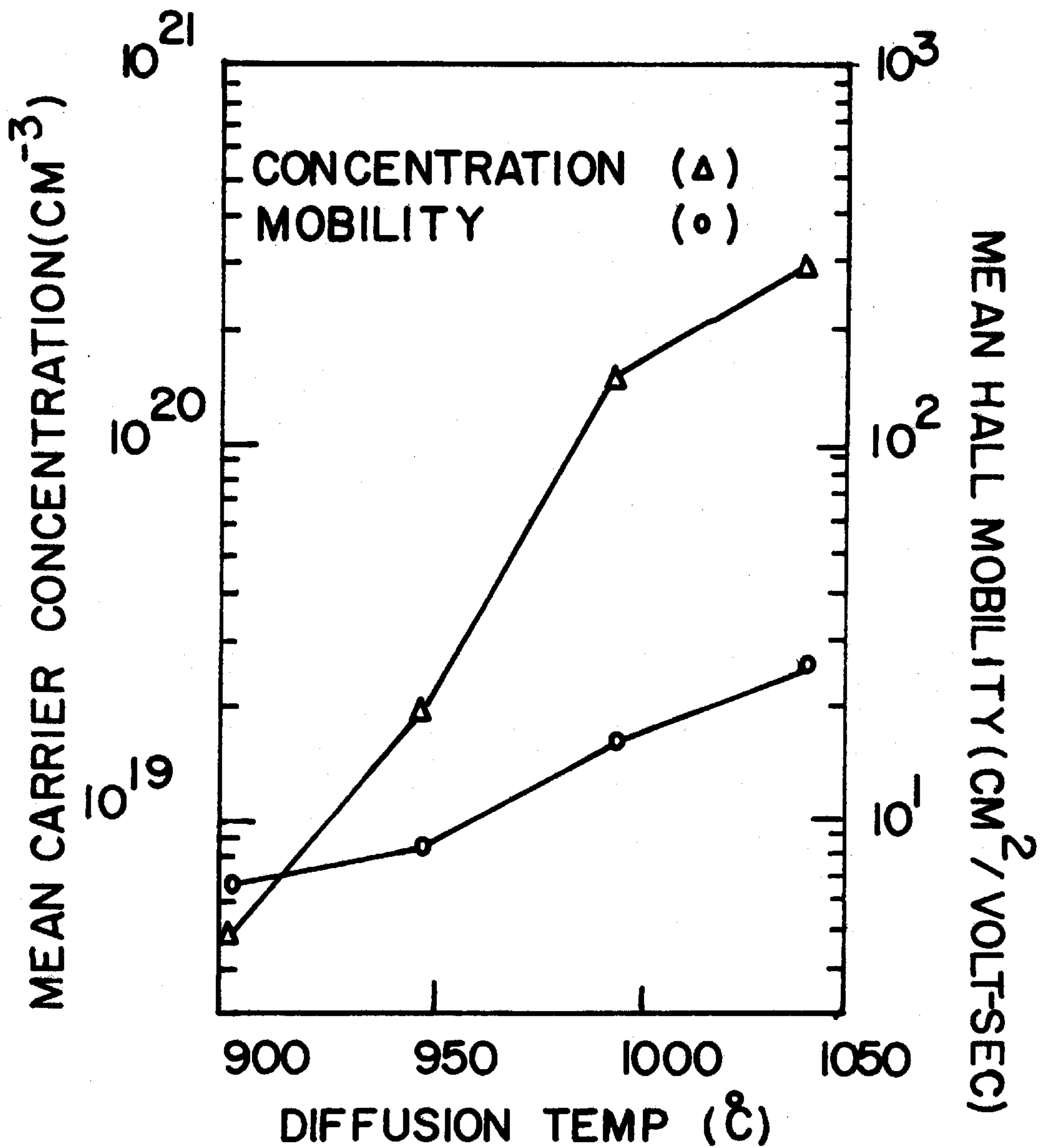


Fig.(7-5) Plots of the mean carrier concentration and Hall mobility versus diffusion temperature for a series of 2500 Å diffusion-annealed silicon films. Diffusion time 160 mins.

transport properties of this material. T.C.R. measurements were performed on suitable resistive samples over the temperature range 0°C to 150°C.

T.C.R.'s in the doped polycrystalline silicon layers were observed to vary widely with resistivity. For gas-doped films the T.C.R.'s were always negative. On the other hand, the T.C.R.'s of diffusion-annealed films were observed to be positive for high sheet resistance and negative for low sheet resistance. Typical variations of normalized resistance with temperature for gas-doped and diffusion-annealed films are illustrated in Fig. (7-6). Figure (7-7) shows a plot of T.C.R. versus carrier concentration for P and N-type 2500 Å gas-doped and diffused films. While the wide variety of processing temperatures employed in the fabrication of these samples result in a considerable spread in the data points,the progression from large negative T.C.R.'s in films possessing low carrier concentrations to small positive T.C.R.'s in films possessing high concentrations is evident.

7.5 Electrical conduction in polycrystalline silicon

Employing an inhomogeneous-film model[93] which presumes substantial numbers of traps to exist at crystallite grain boundaries, most of the observed properties of the polycrystalline material may be qualitatively explained. The model is illustrated in figure (7-8) for N-type silicon. We consider the traps (N_t/cm^2 of grain boundary) to be initially neutral and subsequently to become occupied with carriers contributed by the dopant atoms. A space charge region of the opposite polarity is created by the resultant charged boundaries. The existence of these traps is consistent with the observation[94] that the Fermi level is pinned deep in the forbidden gap at grain boundaries or other defects in both P and N-type silicon.

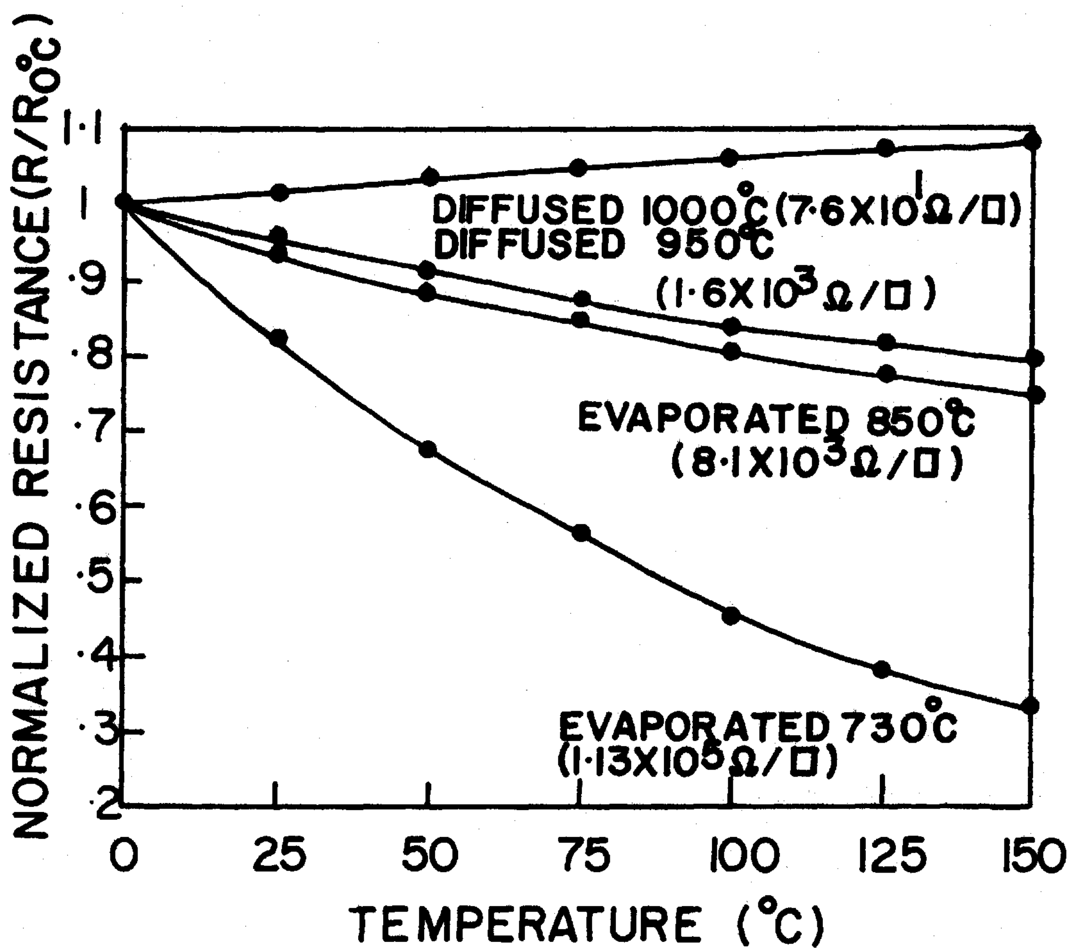


Fig.(7-6) Plots of normalized resistance versus temperature for evaporation gas-doped and diffusion-annealed polycrystalline silicon films

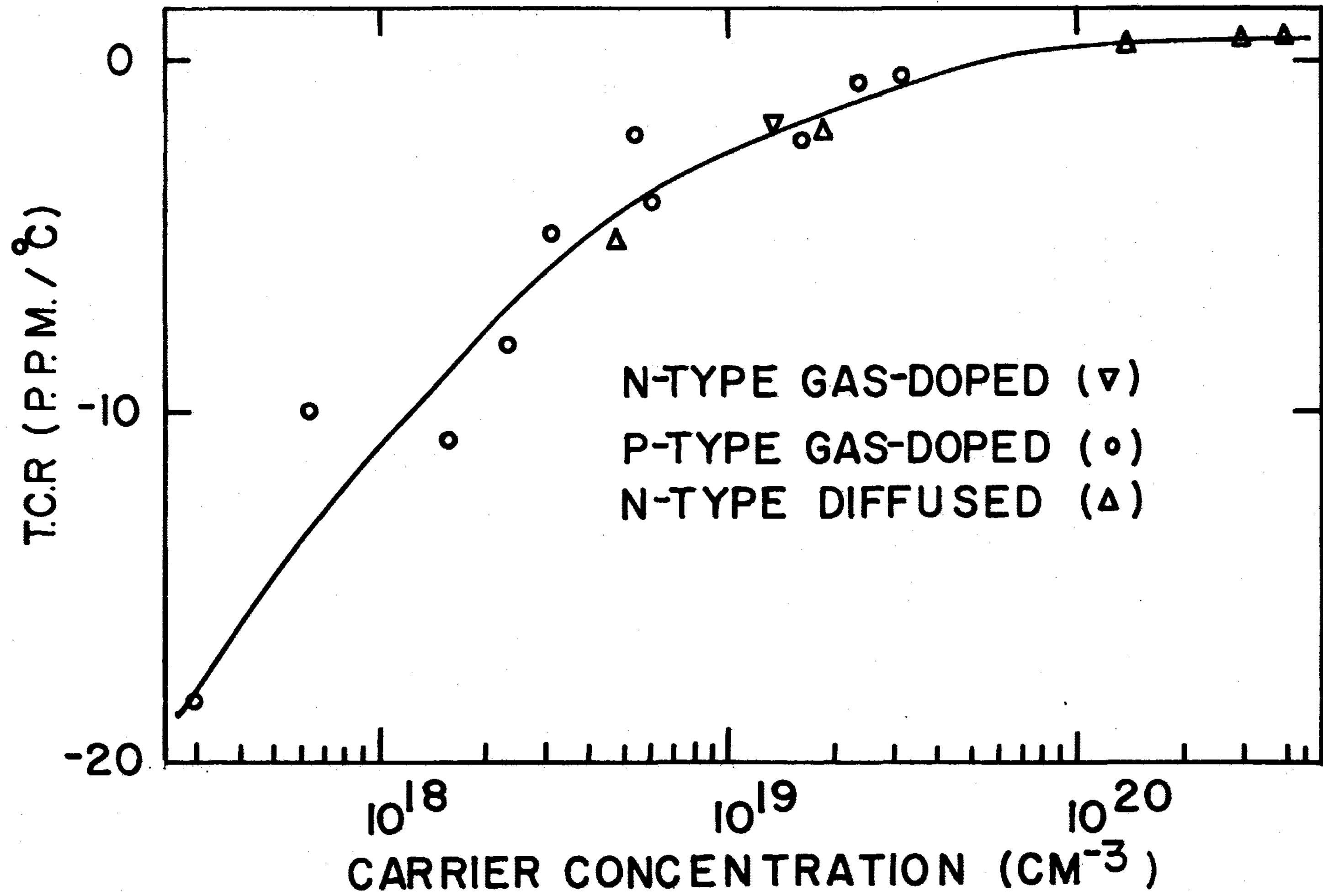


Fig.(7-7) Plot of T.C.R. versus carrier concentration for doped polycrystalline films

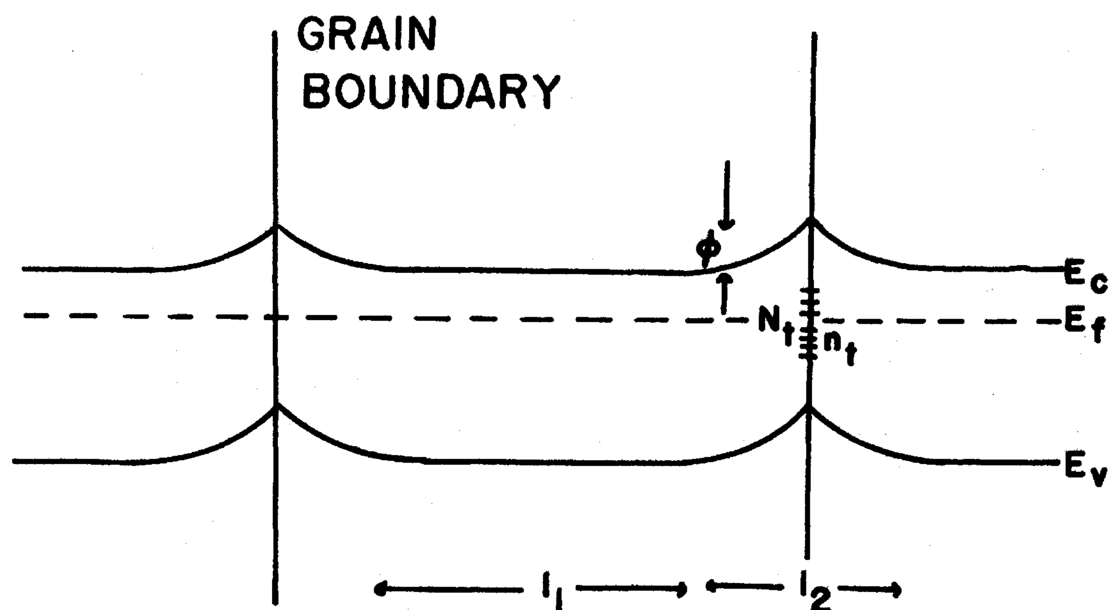


Fig.(7-8) Schematic representation of band structure for the inhomogeneous-film model

From the requirements of space charge neutrality of the grain boundary and the surrounding space charge region, the number of carriers (n_t/cm^2) trapped at the grain boundary will be related to the width of the space charge region by the formula

$$n_t = n_1 \ell_2 \tag{7-1}$$

where n_1 is the majority carrier density in the neutral region (assumed equal to the doping concentration) and ℓ_2 is the width of the space-charge region.

From Poissons equation , the barrier height is given by

$$\phi = \left(\frac{en_1}{2\varepsilon}\right) \left(\frac{1}{2} \ell_2\right)^2 = \frac{en_t^2}{8\varepsilon n_1} \tag{7-2}$$

where ϕ = barrier height potential

e = electronic charge

ε = dielectric constant for silicon

The ratio of free carriers in the neutral region to that at the top of the barrier is

$$\frac{n_1}{n_2} = \exp\left(\frac{e\phi}{kT}\right) \tag{7-3}$$

where k = Boltzmann constant

T = absolute temperature

Combining (7-2) and (7-3) we have

$$\frac{n_1}{n_2} = \exp\left(\frac{e^2 n_t^2}{8\varepsilon kTn_1}\right) \tag{7-4}$$

As the doping concentration is increased, the number of trapped carriers will increase in a manner determined by the energy distribution of the trapping centers. Eventually, the concentration of occupied traps will approach saturation ($n_t \rightarrow N_t$). If the doping concentration is further increased, the barrier ϕ will decrease and the space-charge region become narrower. Since the resistivity of the grain boundaries depends exponentially on barrier height, this resistivity will decrease faster than the resistivity of the crystallites. In the limit, the region near the grain boundary will no longer limit the conductivity and the properties of the polycrystalline layers will approach those of the crystallite material.

We consider the expression

$$\bar{\mu}_H \simeq \frac{A_1}{\rho_1 + \frac{\rho_2 \ell_2}{\ell_1}} \qquad (7\text{-}5)$$

which has been derived[85] for the observed Hall mobility in material possessing low resistivity (ρ_1) grains separated by narrow high resistivity (ρ_2) boundaries, where A_1 = Hall mobility in low resistivity grains

ℓ_1 = length of low resistivity grain

ℓ_2 = length of high resistivity grain boundary

In deriving this expression it has been assumed that $\ell_2 \ll \ell_1$ an assumption valid in the present case only in films possessing the larger crystallites and higher doping concentrations. If for example we take ℓ_1 = 1000 Å, n_1 = $10^{19}/cm^3$ and assume a worst value barrier height of 0.5 eV, we calculate $\ell_1/\ell_2 \stackrel{\sim}{\sim} 6$. While the formulae for the more general case have been derived,[95] the simplified expression (7-5) serves more clearly to illustrate the experimentally observed features.

For very high doping levels ($>10^{20}/cm^3$) the barriers near the grain boundaries will be small and the observed resistivity determined primarily by the resistivity of the crystallites. If the first term in the denominator of (7-5) is dominant the mobility will be close to that of the crystallites. In practice, the observed mobility will be less than that of single crystal material as a result of additional scattering by defects. T.C.R.'s in heavily doped films are positive as in single crystal material possessing equivalent doping concentrations.

As the doping level decreases, the space charge regions widen and the resistivity becomes limited by the resistivity in the barriers. When the second term in the denominator of (7-5) becomes dominant the observed mobility starts to decrease with decreasing carrier concentration. Since the occupation probability of the trapping centres and hence ϕ will decrease with increasing temperature, negative T.C.R.'s are observed. The enhancement of carrier mobility observed with increasing substrate temperature results from a reduction in the number of grain boundaries with increasing crystallite size. The doping concentration at which the transition will occur from films having resistivities dominated by the crystallites to those having resistivities dominated by the grain boundaries will depend principally on crystallite size. For thick $\sim 5\mu$ films chemically deposited at 1030°C, Kamins[85] observed a transition at approximately 10^{18} carriers/cm^3. For the 2500 Å vacuum deposited films considered in the present investigation, the transition, as estimated from the change in sign of T.C.R., occurred at a doping concentration of approximately $7 \times 10^{19}/cm^3$.

7.6 Device applications of deposited polycrystalline silicon

Polycrystalline silicon already finds several applications in integrated circuit technology. High resistivity (>10^5 ohm-cm) undoped material is employed as an isolating medium.[96] Heavily doped polycrystalline silicon is employed as a gate material to reduce the threshold voltages of field effect transistors in silicon gate technology.[97]

Several features of the disordered material make it, in general, an unattractive substitute for single crystal silicon in the formation either of bipolar or of field effect transistors. Minority carrier life-times in polycrystalline silicon have been reported[98] to be of the order of 20 psec. Devices such as bipolar transistors which depend for their action upon minority carrier transport would be inefficient if fabricated in such material. While Kamins[98] has constructed majority carrier transport devices (F.E.T.'s) in polycrystalline silicon, threshold voltages were found to be considerably higher than those in equivalent devices formed in single crystal silicon.

Polycrystalline silicon may however prove useful for the formation of passive circuit elements. In particular, the wide range of resistivities encountered in the disordered material combined with its obvious compat-ibility with single crystal processing technology indicate a possible application in the formation of high value resistors for monolithic integrated circuits. This application is considered in detail in the next section.

7.7 Polycrystalline silicon resistors for integrated circuits

7.7.1 Introduction

High value resistors produced by a single diffusion process exhibit several disadvantages in monolithic integrated circuits. Resistors having

values greater than 20 kΩ require an uneconomical amount of space when fabricated from material having a sheet resistivity of 200 Ω/sq., the maximum conveniently available in monolithic technology. T.C.R.'s for these resistors are typically +2000 PPM/°C and increase with an increase in the diffused sheet resistivity.[99]

Multiple diffused resistors employing the "pinch" effect, while providing high sheet resistivities, have large values of T.C.R. Typical "pinch" resistors measured in this laboratory having a sheet resistivity of 2.5 kΩ/sq. were found to have T.C.R.'s of +6000 PPM/°C. Ion implantation[100] has been employed in producing resistors having sheet resistivities from .8 to 11kΩ/sq. with corresponding T.C.R.'s from +800 to +4000 PPM/°C. However large scale implantation equipment is costly and not yet available in every production facility.

An alternate approach to the problem of obtaining high sheet resistivity consists of depositing a suitable resistive material onto the oxide covering the diffused circuit elements. Resistors of the required values are then produced by selective etching employing photolithographic techniques. Notable[101] among the materials developed for this process are Si-Cr and Cr-SiO compounds offering sheet resistivities from 1 kΩ/sq. to 20 kΩ/sq. with corresponding T.C.R.'s from +150 to -1400 PPM/°C.

In this section, the suitability of doped polycrystalline silicon for the fabrication of IC resistors is considered. Resistors fabricated from this material possess the advantages of high sheet resistivity and dielectric isolation by virtue of their deposition on the SiO_2 over-layer and, in addition, preserve an all silicon technology compatible with conventional production techniques.

Undoped deposited polycrystalline silicon films have been found to possess a resistivity in excess of 10^4 ohm-cm. This is higher than can be practically employed in resistor fabrication. By employing both vacuum evaporation with gas-doping and by diffusion-annealing of undoped amorphous silicon, films possessing resistivities in the range applicable to integrated circuit resistors have been obtained. The fabrication and evaluation of thin film resistors having values and dimensions suitable for integrated circuits are described.

7.7.2 Resistor definition

For successful application of photolithographic techniques combined with selective etching to the delineation of resistors having dimensions typical of integrated circuits, the polycrystalline silicon resistive films must be smooth and must adhere firmly to the SiO_2 substrates. While T.C.R.'s were observed to decrease with increasing deposition temperature for gas-doped films having equal resistivities, surface roughness increased rapidly and adhesion diminished for substrate temperatures in excess of 750°C. A substrate temperature of 730°C was chosen as optimum for the evaporation of gas-doped films for subsequent resistor fabrication. The surface texture and adhesion observed in 2500 Å diffusion-annealed films were approximately equivalent to those of films deposited on substrates having temperatures of 650°C and were thus satisfactory for device fabrication. Evaluations of the etching properties of doped polycrystalline silicon films were made employing standard photolithographic techniques to define resistor test patterns having linewidths from .25 to 2 mil.

Some difficulties were encountered in the adhesion properties of the photoresist solutions when applied directly to the polycrystalline

silicon. By first chemically depositing ∿1000 Å of SiO_2 and employing photoresist and HF etching to define a mask for subsequent silicon etching, linewidths of .25 mil could readily be obtained. Silicon etching was performed in hydrazine hydrate,[102] a preferential silicon etch which leaves the SiO_2 substrates intact.

Fig. (7-9)shows a photomicrograph obtained from part of a .25 mil resistor test pattern and illustrates the high degree of definition possible.

7.7.3 Sheet resistivity and T.C.R.

For the fabrication of high value resistors films possessing sheet resistivities in the range 1 to 10 kΩ/sq. are chiefly of interest. Polycrystalline silicon films having sheet resistivities in this range could be readily produced either by gas-doping or by diffusion-annealing at moderate temperatures. Such films will however be of practical use only if their T.C.R.'s have absolute values within the limits set by a particular circuit design. T.C.R.'s should thus be as close to zero as possible.

Fig. (7-10) shows a plot of T.C.R. versus sheet resistivity for a series of 2500 Å P-type gas-doped films deposited at 730°C. Points representing typical T.C.R.'s and sheet resistivities of 2500 Å films diffusion-annealed at 900°C and 950°C are included for comparison. Fig. (7-11) shows plots of T.C.R. and sheet resistivity versus diffusion temperature for diffusion-annealed resistor films. T.C.R. values quoted were obtained between 0°C and +50°C (ΔT = 50°C) and thus represent a value at approximately room temperature.

By way of comparison, gas-doped and diffusion-annealed 2500 Å films could be produced having a sheet resistivity of 1 kΩ/sq. and a T.C.R. of

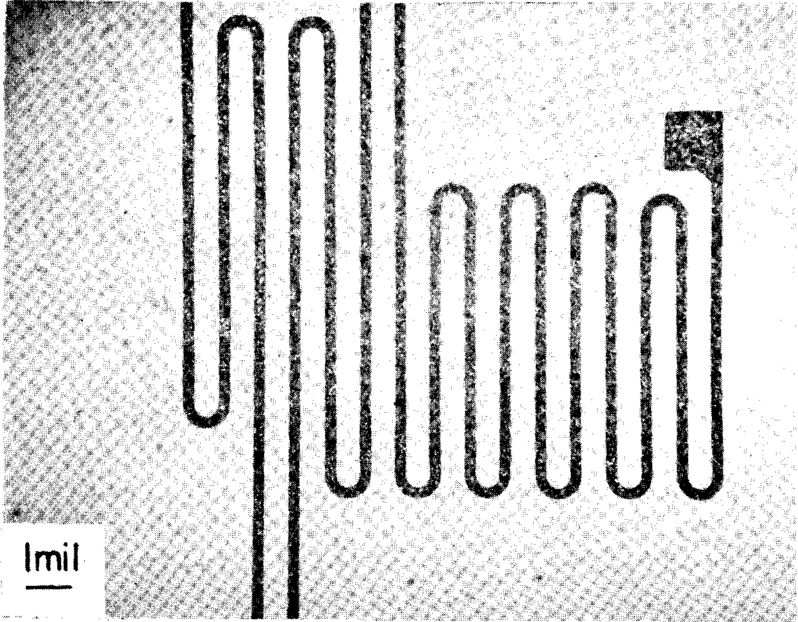


Fig. (7-9): Photomicrograph obtained from part of a 0.25 mil polycrystalline silicon resistor test pattern.

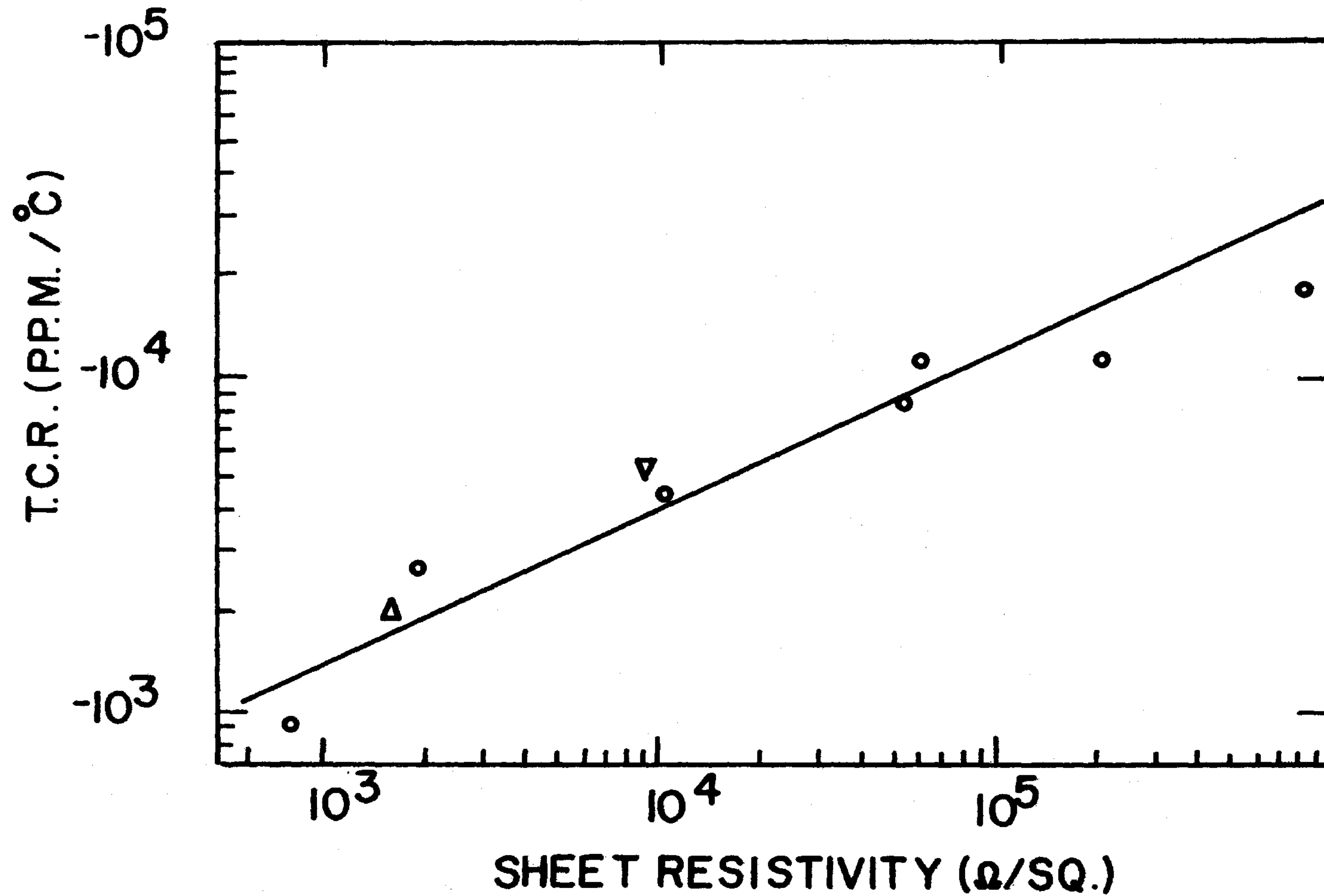


Fig.(7-10) Plot of T.C.R. versus sheet resistivity for a series of 2500 Å P-type gas-doped polycrystalline films deposited onto substrates having a temperature of 730°C. Points representing the sheet resistivity and T.C.R. values of films diffusion annealed at 900°C and 950°C are also shown

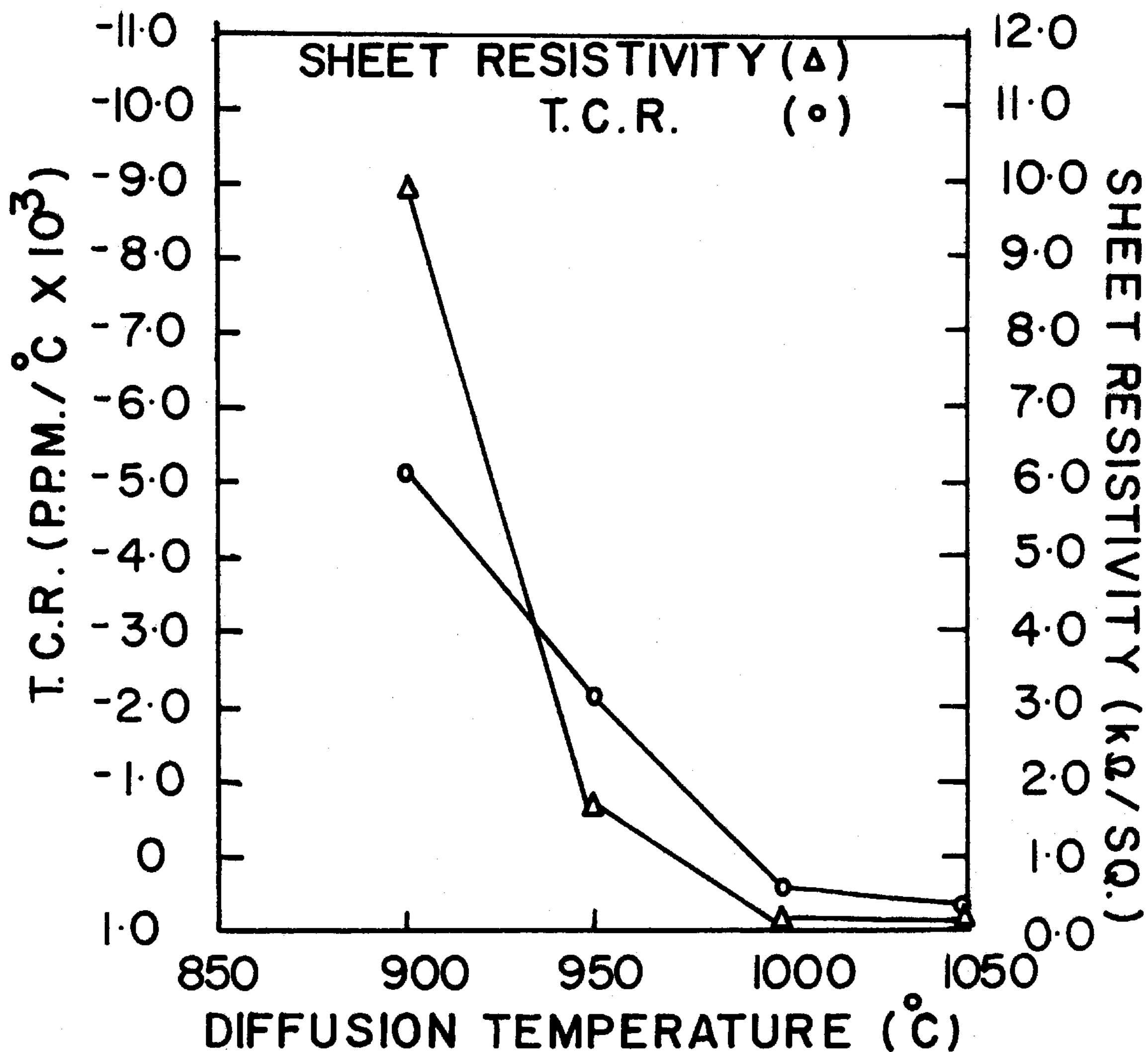


Fig.(7-11) Plots of T.C.R. and sheet resistivity versus diffusion temperature for a series of 2500 Å diffusion annealed silicon thin films Diffusion time 160 mins.

-1000 PPM/°C whereas conventional IC diffused resistors have a TCR of +2000 PPM/°C at 200 Ω/sq.

7.7.4 Resistor linearity and stability

Current-voltage and temperature stability measurements were performed on P and N-type gas-doped resistors having sheet resistivities from 1 kΩ/sq. to 50 kΩ/sq. and on diffusion-annealed resistors having sheet resistivities from 1 kΩ/sq. to 10kΩ/sq. The aluminium contacts to these resistors were sintered for 10 mins. at 450°C and their surfaces protected with undoped "spin-on"* oxide which was subjected to the same temperature cycle. The polycrystalline resistors proved ohmic to within 10% for applied voltages from .01 to 50 volts.

For use in practical applications polycrystalline resistors must exhibit long term stability. A number of such resistors were mounted on headers and heat-treated without bias in air at 200°C. Table (7-3) illustrates changes produced in the values of these resistors after treatment for successive 50 hr. and 200 hr. intervals.

Table (7-3)

Temperature Stability of Diffusion Annealed and Evaporation Gas-Doped Polycrystalline Silicon Resistors

Sample No.	Fabrication Procedure	Mean Carrier conc. Carriers/cm^3	Thickness Å	Sheet Resistivity Ω/sq.cm.	% Change in 200°C Unbiased Heat Treatment 50 hrs.	300 hrs.
POX 1	evap. 730°C	6.2×10^{18}	2500	10.4×10^3	-9.4%	-18.5%
POX 13	evap. 730°C	3.0×10^{19}	1700	1.05×10^3	-2.3%	+1.18%
POX 8	evap. 700°C	2.2×10^{18}	2500	5.54×10^4	-16.9%	-19.8%
DIF 1	Diffusion-Annealed 900°C	4.8×10^{18}	2500	8.90×10^3	-3.44%	-4.26%
DIF 2	Diffusion-Annealed 950°C	1.8×10^{19}	2500	1.66×10^3	-2.06%	-3.8%

*Emulsitone Co. Ltd. New Jersey

As may be seen, substantial changes were produced in resistors fabricated from 2500 Å high resistivity gas-doped layers during both the 50 hr. and subsequent 300 hr. heat treatments. Both the thinner gas-doped films (1700Å) and those diffusion-annealed proved much more stable when subjected to the 200°C heat treatment.

In monolithic integrated circuits,absolute resistor value variations of up to 30% are generally tolerable provided resistor ratios are accurately maintained. Because of this,the instability observed both in the diffusion-annealed and in the thin gas-doped films would probably be acceptable for many applications. In addition, it is expected that modifications in the fabrication procedure and the use of thinner films possessing high doping concentrations would result in increased film stability.

7.7.5 Thickness

The Hall mobility measured in chemically deposited polycrystalline films has been shown[85] to increase rapidly with total film thickness. For reproducibility, good etching definition and high values of sheet resistivity, film thicknesses from 1000 Å to 5000 Å appear most practible for resistor fabrication. The value of 2500 Å generally employed in this investigation is not necessarily optimum. A number of gas-doped films of thickness 1700 Å were investigated and were found to exhibit increased stability and a reduction in T.C.R. over those of thickness 2500 Å. Typical values of 1 kΩ/sq. and -600 PPM/°C were recorded in 1700 Å P-type films having carrier concentrations of 3×10^{19} holes/cm^3.

7.8 Summary

The structure and electrical properties of polycrystalline silicon thin films obtained by vacuum evaporation onto SiO_2 substrates have been

investigated. The deposited layers have been shown to possess structures ranging from amorphous through randomly oriented polycrystalline to oriented polycrystalline as the substrate temperature is increased from 25°C to 850°C. The electrical characteristics of evaporated layers doped both during deposition by gas-doping and after deposition by diffusion have been shown to be consistent both with each other and with those recently[85] reported for thick polycrystalline layers deposited by chemical techniques. Employing an inhomogeneous film model the experimentally observed electrical properties of the polycrystalline material have been qualitatively explained.

The structure and electrical properties of doped polycrystalline silicon thin films on SiO_2 substrates amenable to the production of high value resistors for monolithic integrated circuits have been investigated. Sheet resistivity and T.C.R. values have been shown to be superior to those obtainable in conventional IC single-diffused resistors. Etched line widths of 0.25 mil have been obtained in the polycrystalline silicon by employing photolithographic techniques. Polycrystalline resistors fabricated from material having sheet resistivities from 1 kΩ/sq. to 50 kΩ/sq. have been shown to be ohmic within 10% for applied voltages from .01 to 50 volts.

In view of the obvious compatability of doped polycrystalline silicon with existing silicon technology and of the further improved T.C.R.'s and stability which may be expected to result from other combinations of the deposition and diffusion cycles, it is expected that resistors fabricated from this material may find application in the production of low power monolithic integrated circuits.

CHAPTER VIII

CONCLUSIONS

8.1 Summary

In this thesis has been reported an investigation into the properties and device applications of silicon thin films evaporated onto silicon and silicon dioxide substrates in high vacuum.

8.1.1 Homoepitaxial Layers

The feasibility of depositing device quality single crystal silicon films onto silicon substrates under conditions considerably less restrictive than those employed in previous investigations has been demonstrated. Typical films deposited onto non heat-treated Si<111> and Si<100> substrates having temperatures of 700°C have been found to contain etch pit densities as low as $5 \times 10^5/cm^2$ and $5 \times 10^3/cm^2$ respectively. The structural perfection of the deposited layers has been found to be insensitive to changes in the system pressure over the range 2×10^{-7} to 5×10^{-9} torr.* Such defects as are detected in the evaporated layers may be attributed to the presence of impurities on the substrate surface rather than to interactions with residual gases in the vacuum system. Since the ultra high vacuum conditions employed in previous studies of low temperature growth are impractical for large scale production processes, this relaxation in the pressure requirement considerably enhances the suitability of vacuum epitaxial deposition for industrial applications.

The technique of gas-doping has been developed and has been shown to be capable of reproducibly introducing P and N-type doping impurities in concentrations up to $\sim 3 \times 10^{19}/cm^3$ into the evaporated films. While

*the sensitivity of the compensation centre density to system pressure was not determined

some structural deterioration has been observed in homoepitaxial layers deposited onto Si<111> substrates as a result of the doping process, deterioration in films deposited onto Si<100> substrates at 700°C has been found to be minimal for doping concentrations up to $\sim 1 \times 10^{19}/cm^3$. The combined deposition-doping technique has been shown to be capable of providing silicon layers containing impurity steps more abrupt than may be obtained by conventional methods.

The electrical characteristics of the vacuum evaporated homoepitaxial silicon films have been investigated. The deposited material has been shown to possess a relatively high degree of electrical perfection with room temperature carrier mobilities in N-type material as high as $\sim$1000 cm sec^{-1}/volt cm^{-1}. However, electrical measurements have established the presence both of N-type contaminating dopants having a concentration of $\sim 1 \times 10^{15}/cm^3$ and of compensating centres having a concentration of $\sim 3 \times 10^{16}/cm^3$ in the deposited material.

The combined deposition-doping technique has been employed in the fabrication at 700°C both of all epitaxial silicon diodes and of devices formed by evaporating P or N-type material onto substrates having the opposite doping type. The characteristics of these devices, while probably to some extent degraded by residual structural and electrical imperfections in the evaporated material, have been found to be comparable with those exhibited by standard diffused structures. The characteristics both of hyperabrupt Schottky barrier varactors and of beta-voltaic energy conversion diodes prepared by the evaporation gas-doping technique have been evaluated.

8.1.2 Films on SiO_2 Substrates

The structure and electrical properties of silicon thin films vacuum evaporated onto SiO_2 substrates have been investigated. The films have been doped either during evaporation by the gas-doping technique or after evaporation by diffusion. The characteristics of the evaporated silicon have been shown to be consistent with those recently reported[85] for similar material deposited by chemical techniques. Employing an inhomogeneous film model, the experimentally observed electrical properties of the disordered material have been qualitatively explained.

The suitability of thin films of doped polycrystalline silicon for the production of high value resistors for monolithic integrated circuits has been considered. Sheet resistivities and T.C.R. values measured in 2500 Å polycrystalline films have proved superior to those encountered with conventional diffused resistors. The temperature stability, linearity and etching definition of doped polycrystalline resistors have been shown to be adequate for many applications. In addition, it is expected that modifications in the fabrication procedures and the use of thinner films possessing high doping concentrations would result both in improved stability and in a reduction in the T.C.R. values of the polycrystalline resistors.

8.2 Recommendations

While the structural and electrical perfection of the low temperature vacuum evaporated homoepitaxial layers produced in the present investigation have been shown to be adequate for many device applications, some relatively simple variations in the deposition-doping technique may be

expected to produce a substantial improvement in the characteristics of the deposited material.

Modification of the deposition system to reduce contamination either by carryover doping or by the electron gun and substrate heater materials should permit the evaporation of homoepitaxial films possessing substantially lower concentrations both of unwanted dopants and of compensating centers.

The structural imperfections in the evaporated layers may be attributed to the presence of residual impurities on the substrate surface. Since no especial cleaning procedures have been employed to reduce the concentration of these impurities, films obtained in the present investigation represent a worst case of substrate contamination. Suitable cleaning procedures which reduce the level of such contamination may be expected to result in a considerable improvement in the structural and electrical perfection of the evaporated layers.

(a) external cleaning procedures. The use of HCl vapor etching to remove $\sim 10\mu$ of silicon from the substrate prior to placing in a vacuum system has been found[8] to result in a reduction of approximately two orders of magnitude in the concentration of surface carbon. Since this impurity has been shown to play a dominant role in the growth processes, such a reduction should produce a corresponding decrease in the density of imperfections in the deposited material.

(b) in situ cleaning. Argon sputtering has been reported[8] to be an effective technique for the in situ cleaning of silicon substrates. After sputtering for $\sim 10^3$ sec with a current of $\sim 10\mu A/cm^2$ at 400 eV surface

concentrations of contaminating impurities have been shown to be less than $\sim 10^{13}/cm^2$.

The use either of these or of some other suitable predeposition cleaning process may reasonably be expected to reduce the density of imperfections in the evaporated material to a level comparable with that found in state of the art chemically deposited homoepitaxial films.

Although gas-doping has been shown to be an effective technique for obtaining controlled concentrations of doping impurities in evaporated layers, the fraction of the impinging dopant molecules which contribute free carriers to the evaporated silicon is small. Modifications of the doping technique which would permit a larger number of the impinging molecules to become incorporated into the layer would permit growth to take place at a lower leak gas pressure. Such a reduction in doping gas pressure would result in a decrease in carryover doping and an increase in layer perfection. Several such modifications are suggested below:

1) Since the fraction of the impinging dopant atoms incorporated into the growing layer is limited by the condensation coefficient of the respective doping gas, modifications which would permit this coefficient to be increased should allow higher doping concentrations to be obtained at lower gas pressures. The condensation coefficient of the impinging gas molecules may possibly be increased either by heating or cooling the doping gas, by directing the gas beam at the substrate at an angle of incidence other than $\sim 90°$ or by partially ionizing the gas molecules. Since the complex interactions between the impinging gas molecules and the substrate are not well understood it is difficult to predict which if

any of such modifications may increase condensation.

2) Condensation coefficients for dopant atoms, as opposed to doping gas molecules, should be close to unity. Modifications of the system which would permit the impinging doping gas to be at least partially decomposed before striking the surface should permit an increase in the doping efficiency. Such a decomposition may possibly be achieved either by heating, by electron or U.V. bombardment or through the use of R.F. fields.

8.3 Conclusions

It has been established that vacuum evaporation combined with gas-doping is a versatile technique capable of providing both single crystal and polycrystalline silicon films having a wide range of characteristics of interest for device fabrication. Notable features of the deposition-doping technique include low processing temperature, accurate thickness control and flexibility of doping profile. These advantages, along with those intrinsic to direct deposition systems as outlined in the introduction to this thesis, indicate that the technique of vacuum evaporation with gas doping may find application in the industrial production of silicon semiconductor devices.

APPENDIX A

HALL EFFECT AND CONDUCTIVITY MEASUREMENTS ON EVAPORATED SILICON FILMS

Techniques for the determination of carrier concentration and carrier mobility in thin silicon films by Hall effect and conductivity measurements have been considered in detail by Johansson et al.[103]

The sheet resistivity (ρ_s) and sheet Hall coefficient (R_s) for the configuration shown in figure (A-1) are given by

$$R_s = 10^8 \, (\Delta V_{13}/BI_{24}) \tag{A-1}$$

$$\rho_s = \left(\frac{\pi}{\ell n 2}\right) \left(\frac{\Delta V_{34}}{\Delta I_{12}}\right) \tag{A-2}$$

where B = magnetic field perpendicular to the sample

ΔV_{13} = change in voltage between terminals (1-3) when field B is applied

I_{24} = current between terminals (2-4)

ΔV_{34} = change in voltage between terminals (3-4) when current ΔI_{12} is passed between terminals (1-2)

For a uniformly doped sample having a thickness t

$$n = \frac{r}{R_s e t} \qquad \mu_H = \frac{R_s}{\rho_s} \qquad \text{(A-3) (A-4)}$$

where t = layer thickness

n = carrier concentration/cm^3

μ_H = Hall mobility

r = ratio of Hall mobility to conductivity mobility

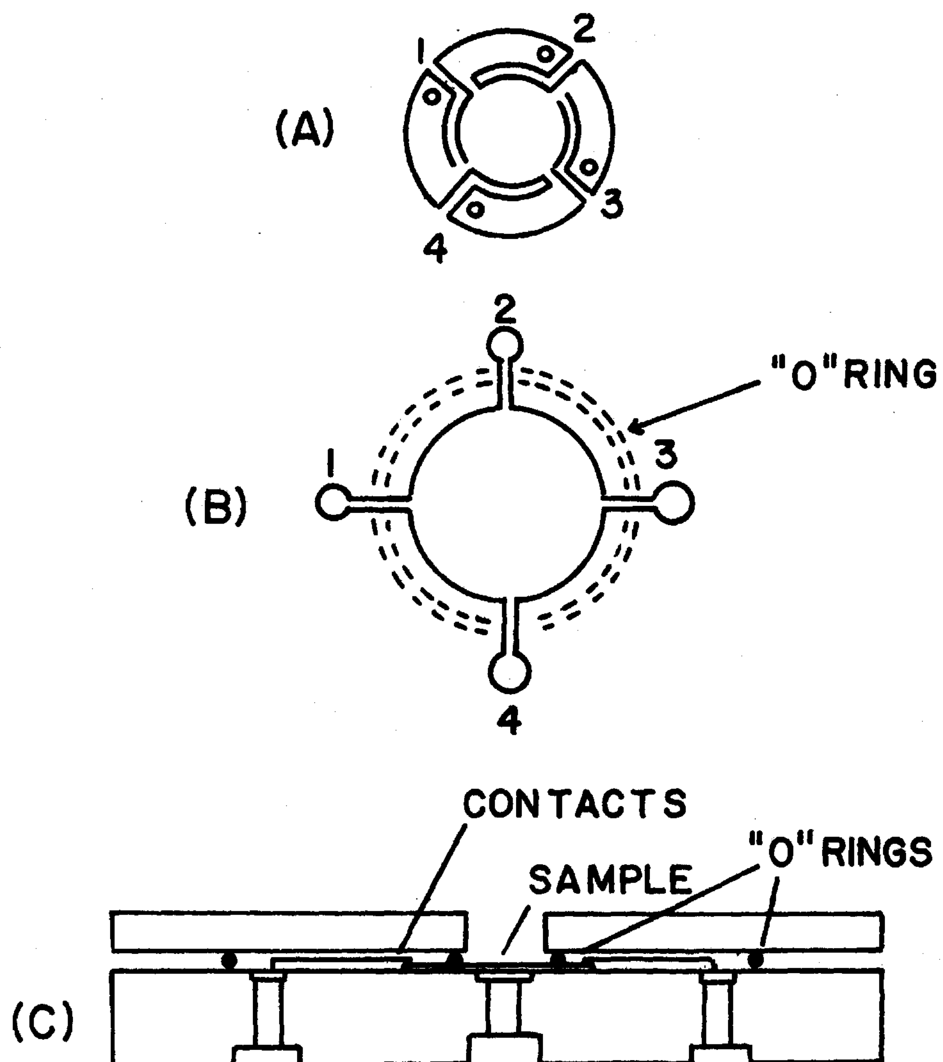


Fig.(A-1) (A) Van der Pauw pattern for measurements on uniformly doped evaporated layers.
(b) Van der Pauw pattern for measurements of impurity profile
(C) Sample holder for anodization and strip etching measurements

The value of r depends on the scattering mechanism and the impurity concentration. For lightly doped silicon, experimental data[104] indicate r = 1.2-1.3 for electrons and r $\approx$ 0.7-0.8 for holes. For heavily doped material r $\approx$ 1. Since considerable uncertainty exists as to the value of r for a particular value of doping, it was assumed in the present investigation that r = 1 for electrons and holes in both the single crystal and in the polycrystalline silicon films. Use of this assumption might lead to a 20-30% error in the value of n obtained for lightly doped layers.

In a non-uniformly doped film, the values of n and μ_H are averages which depend upon the distribution in depth of the carrier concentration and mobility. The carrier concentration and mobility profiles in such films may be determined by making Hall effect and conductivity measurements as successive layers are removed from the sample.

The number of carriers in the ith layer and their corresponding mobility μ_i are given by[103]

$$\mu_i = \frac{\Delta(R_s/\rho_s^{\,2})_i}{\Delta(1/\rho_s)_i} \tag{A-5}$$

$$n_i = \frac{\Delta(1/\rho_s)_i}{e\, d_i \mu_i} \tag{A-6}$$

where $(R_s)_i$ = sheet Hall coefficient after removal of ith layer

$(\rho_s)_i$ = sheet resistivity after removal of ith layer

d_i = thickness of ith layer

Experimental

Van der Pauw[51] clover leaf patterns as shown in figure (A-1) were etched in the deposited layers by masking either with photo-resist or with

thick ($\sim .5\mu$) evaporated aluminium. For accurate measurement of the Hall effect and conductivity voltages, leakage currents to the substrate must at all stages be less than 5% of the conductivity currents through the Van der Pauw patterns. Since SiO_2 is an excellent insulator, no isolation problems existed in measurements on the polycrystalline silicon films. Isolation was achieved in homoepitaxial films by evaporating P or N-type material onto substrates of the opposite doping type. The mesa etched Van der Pauw patterns thus formed P-N junctions with the substrate and could readily be isolated by applying a reverse bias. It was found that leakage currents were sufficiently low for accurate measurement provided the doping concentrations in the P and N-type evaporated layers exceeded 10^{17} and 10^{16} carriers/cm^3 respectively.

To investigate resistivity and impurity profiles in non-uniformly doped samples, anodization combined with HF acid stripping was employed to remove successive layers from the deposited material. The anodization rig was similar to that described by Crowder and Fairfield[105] and is shown schematically in figure (A-1C). The area of the sample to be anodized is defined by a viton "O" ring. Anodizations were performed to constant voltages in solutions consisting of .04N KNO_3, .02N $Al(NO_3)_3$ and 2.5% water in ethylene glycol. Etch step height was determined by measuring the total thickness of silicon removed (using multiple beam interferometry) and dividing by the number of anodization steps. Typical step heights ranged from 200 Å to 300 Å. Employing this technique carrier concentrations could be measured with an accuracy of ±20%.

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