A SINGLE STAGE CASCADE A-D CONVERTER

THE DESIGN AND CONSTRUCTION OF

A SINGLE STAGE CASCADE ANALOG TO DIGITAL CONVERTER

by

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SCOPE AND CONTENTS:

The thesis is concerned with the design, construction and evaluation of an analog to digital converter based on the "cascade" principle. However, this converter requires only one stage, instead of the usual one stage per bit required by conventional cascade converters. This reduction in the number of stages is achieved by storage in analog form, and by feeding the output of the stage back to its input via a switching network. An 8 bit converter that operates up to a clock frequency of 700KHz was built. The converter is shown to have promising possibilities as a low cost general purpose analog to digital converter.

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CHAPTER 1

INTRODUCTION

Due to the rapid advances being made in, and the high accuracy of digital systems, use of digital processing and control systems is rapidly increasing. Since most sensors and transducers are analog devices, it is necessary to have a means of converting analog signals into digital words. This exigency is fulfilled by systems known as analog to digital converters.

The majority of A/D converters can be broadly classified into two categories. They are:

(1) Those in which the analog input is sampled, and an approximation to this sample is generated by the converter. This internally-generated approximation is compared to the input and a more accurate approximation is made. This process continues until the approximation is equal to the input, within the accuracy limits of the converter. For many converters in this category the approximation is made using a digital switching system to control the amplitude of the internal analog comparison voltage, so that a digital to analog converter forms an essential part of the system. A comparator and feedback loop are also essential. The basic system is shown in Figure 1.1. If high accuracy or multiplexed inputs are required with this type of converter, sample and hold circuits are required.

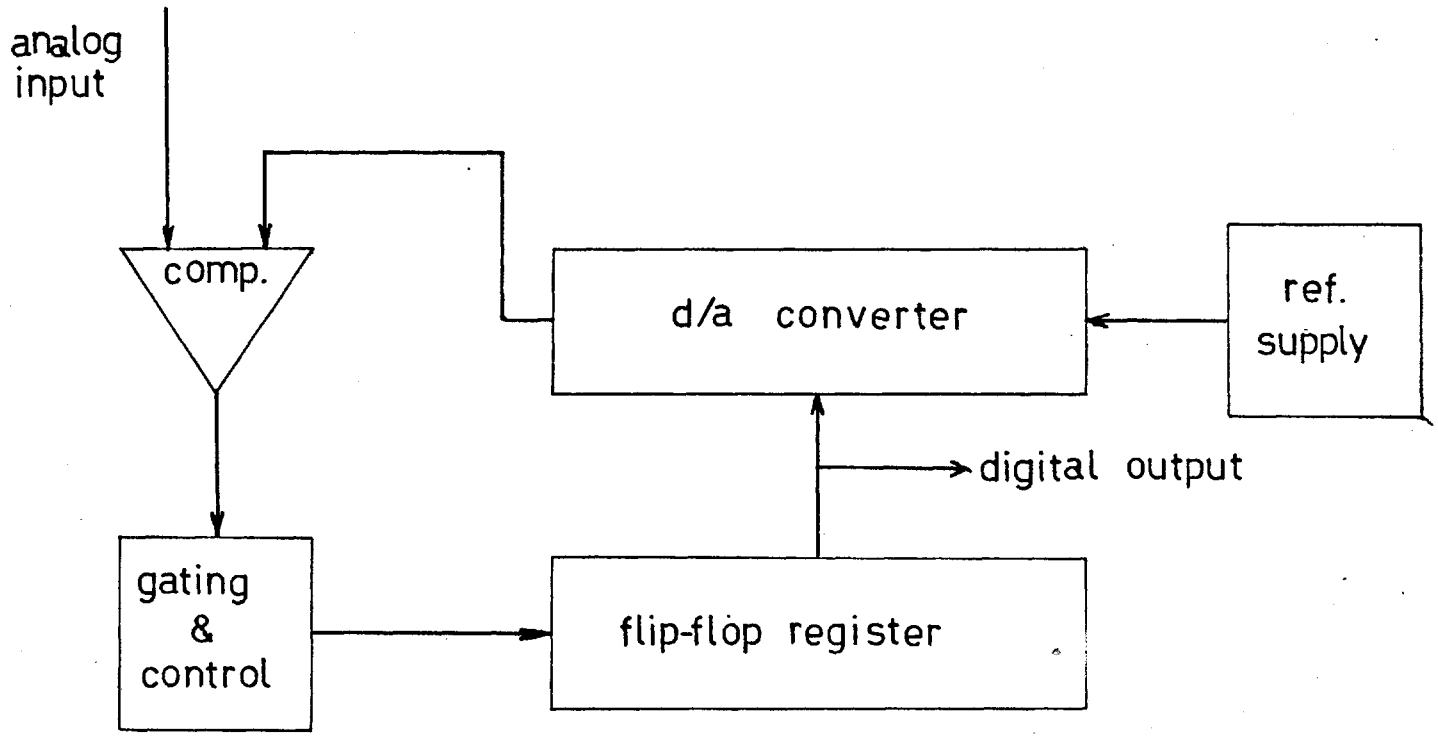


Figure 1.1

A/D converter with a D/A converter in the feedback loop.

(2) Those in which the analog input is operated on, in some controlled manner, and various comparisons made until the analog input has been analysed into a digital word, within the accuracy limits of the system. Sampling of the analog input voltage may also feature in converters within this category.

Chapter two of the thesis contains a review of the following types of A/D converters, which fit into the first category:

(1) Successive approximation

(2) Simultaneous

(3) Counter

(4) Single ramp

and a review of:

(1) Dual ramp

(2) Triple ramp

(3) Voltage to frequency

(4) Cascade

types of converter which belong to the second category.

This review consists of only a brief outline of the above converters because an exhaustive review would be an exceedingly large undertaking. Also included in this review is an introduction to the concept of the single-stage cascade (SSC) converter. Chapter two is concluded with a critical comparison of the various methods of conversion, and the place of the SSC converter in relation

to them is established.

In Chapter three the SSC converter devised by the author is introduced and its principles, speed and accuracy are discussed. It is shown that the sample and hold operation is inherent in the system and hence a separate (and often costly) circuit does not have to be added in order to achieve a small aperture time. The converter is also shown to consist of a relatively small number of components, only two of which require tight tolerances, and to have a high input impedance. A further advantage of the converter is that it is highly suited to large scale integration fabrication.

An investigation of the SSC converter was commenced using Digital Equipment Corporation discrete-component modules. The results obtained are given in Chapter four. They indicated that the SSC converter has promising possibilities. As a result of this a more advanced form of the converter was designed, constructed and evaluated, using integrated circuits, and field-effect transistor switches, as described in Chapter five.

CHAPTER 2

REVIEW OF A/D CONVERSION TECHNIQUES

Analog to digital conversion is realized by a number of different techniques. Some of the currently available techniques are reviewed in this chapter.

2.1 Successive Approximation A/D Converter[1.2.3.4.5.]

This is the most widely used technique for high accuracy, medium conversion rate converters. This method requires only one step per bit to convert any number and a three bit version is shown in Figure 2.1.

The converter operates by repeatedly dividing the voltage range in half. Thus, the system first tries 100, and the output of the D/A decoder is compared against the input analog signal. If the D/A output is the smaller, the M.S.B. remains a one. A one is now entered in the second M.S.B. and the output of the D/A decoder is compared against the analog input. If the D/A output is still the smaller, the second M.S.B. remains a one. A one is now entered in the third M.S.B. and the D/A decoder output is again compared against the analog input. If the D/A output is the larger, the third M.S.B. becomes a zero.

One of the major units in this system is the D/A decoder, and this will be considered in more detail.

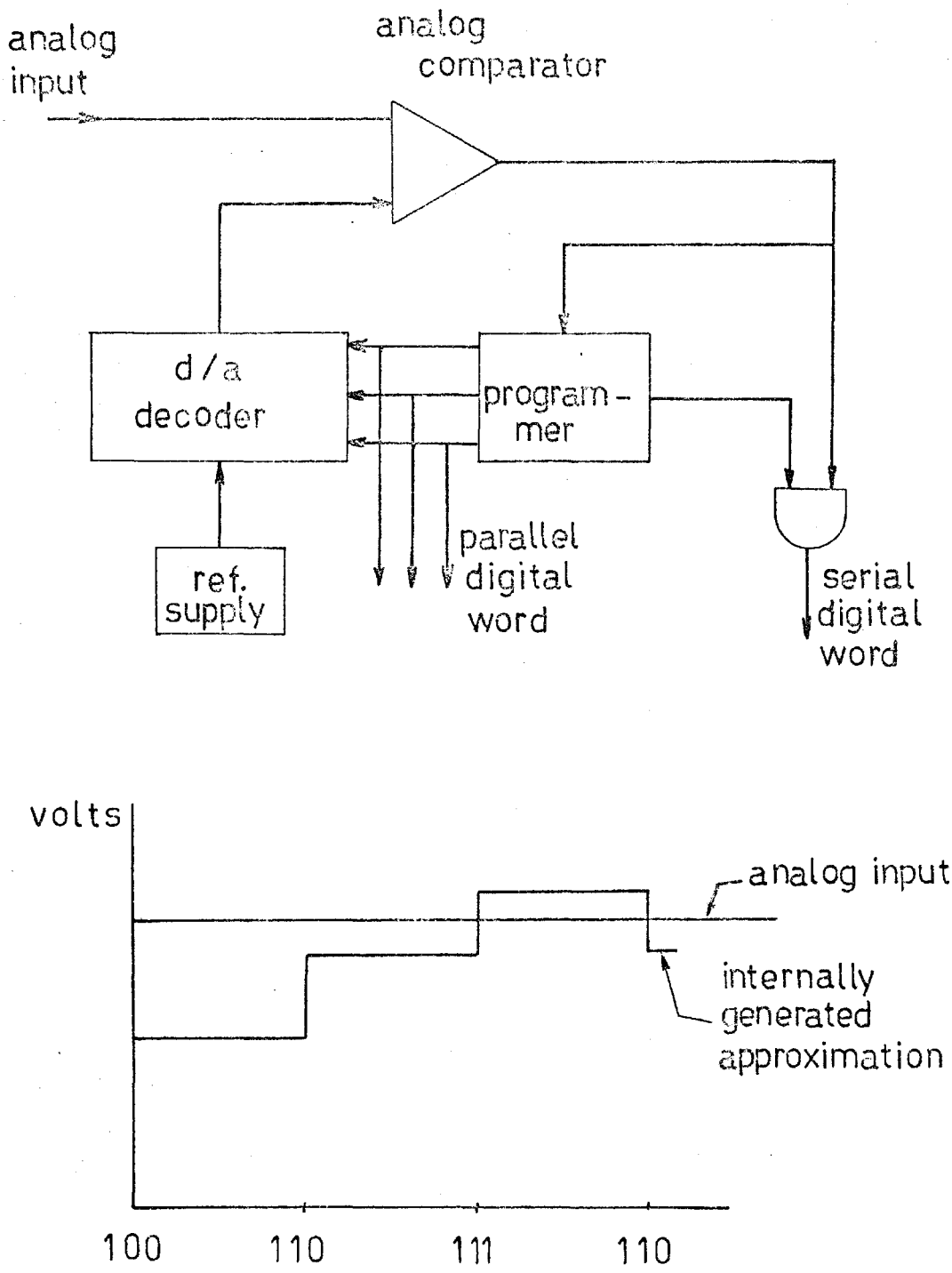


Figure 2.1

Principle of the succesive approximation converter

2.1.1 Digital to Analog Decoder[1,2]

A D/A decoder is used to convert a digital word of binarily weighted information to an analog voltage level. One scheme is the Weighted-Resistor D/A decoder shown in Figure 2.2, where the size of each resistor is inversely proportional to the weighted value of the digital bit it decodes. That the analog output voltage represents the digital number can be shown as follows:[1]-

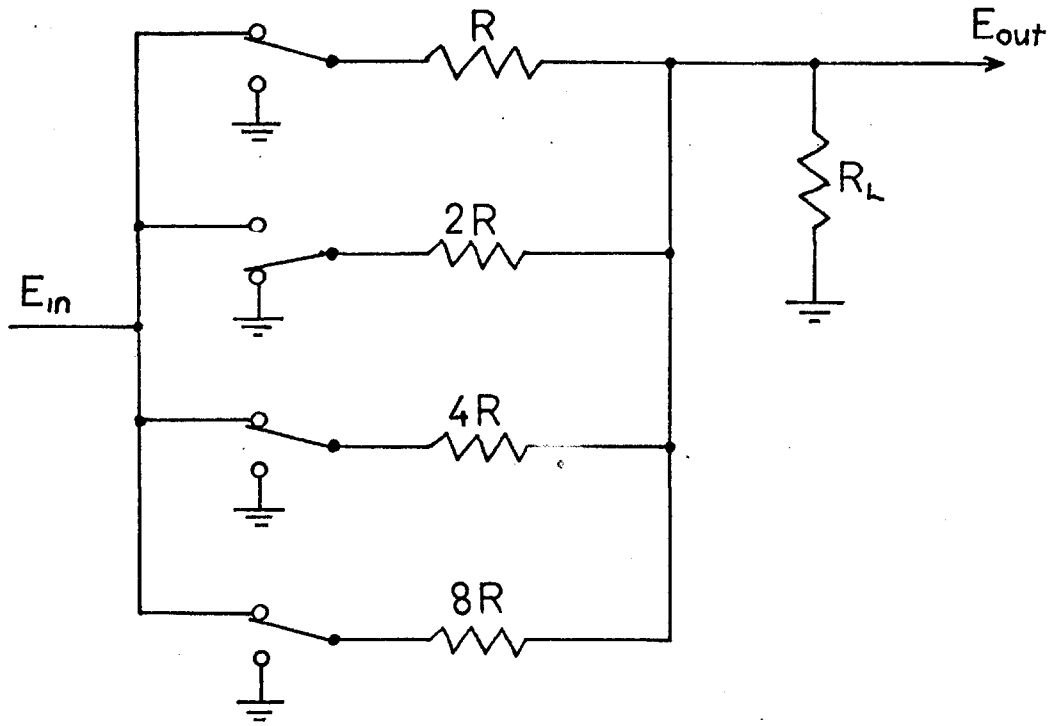
$$E_{out} = E_{in} \frac{R_b}{R_a + R_b}$$

where R_a is the resistance connected between E_{in} and E_{out} terminals and R_b is the resistance connected between E_{out} and ground. If we now convert to conductances,

$$E_{out} = E_{in} \frac{G_a}{G_a + G_b}$$

where $G_a = \frac{1}{R_a}$ and $G_b = \frac{1}{R_b}$. But the total conductance $G_a + G_b$ is constant for all decimal numbers. Therefore E_{out} is proportional to G_a and since G_a is in direct proportion to the binary weighted value of each "one" in the number being converted, E_{out} is an analog representation of the digital input.

This system has two major disadvantages, the first being that if there is a large number of bits in the digital word, very high resistances have to be used for the lower order digits. For example, suppose a 12 bit weighted resistor D/A decoder, which for accuracy reasons requires a M.S.B. resistor of 20 Kohms, is considered. The L.S.B. resistor must then be 2^{11} x 20 Kohms = $2,048 \times 20 \times 10^3$ ohms = 40.96 Mohms. A precision resistor of this high



$$G_a = \frac{1}{R_a} = \frac{1}{R} + \frac{1}{4R} + \frac{1}{8R}$$

$$G_b = \frac{1}{R_b} = \frac{1}{2R} + \frac{1}{R_L}$$

$$G_a + G_b = \frac{1}{R} + \frac{1}{R} + \frac{1}{2R} + \frac{1}{4R} + \frac{1}{8R}$$

$$E_{out} = \frac{E_{in} R_b}{R_a + R_b}$$

Fig. 2.2

Weighted Resistor 4 bit D/A Network

resistance value is expensive, and hence undesirable. The second disadvantage is that it is difficult to obtain resistors with closely matched temperature coefficients if their resistance values differ greatly. With high accuracy systems this is an important consideration.

A circuit which overcomes these disadvantages is the resistive ladder circuit shown in Figure 2.3(a) which utilizes only two resistor sizes, R and 2R.[1] The figure shows a three bit converter converting the binary number 100. The output resistance of this ladder circuit, R_o, can be obtained as follows, assuming it is driven from a low-impedence voltage source. The resistance from node 3 to ground through R_3 and R_6 is

$$\frac{R_3R_6}{R_3+R_6} = \frac{4RR}{4R} = R$$

The resistance from node 2 to ground through R_2, R_3, R_5, and R_6 is R_2 in parallel with the series combination of R_5 and R

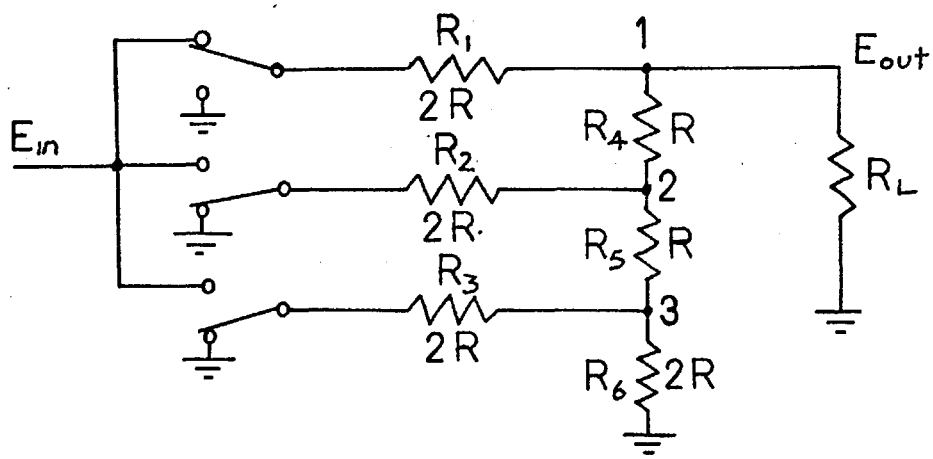
$$\frac{R_2\,(R_5 + R)}{R_2+ R_5 + R} = \frac{2R\ 2R}{4R} = R$$

The resistance from node 1 to ground

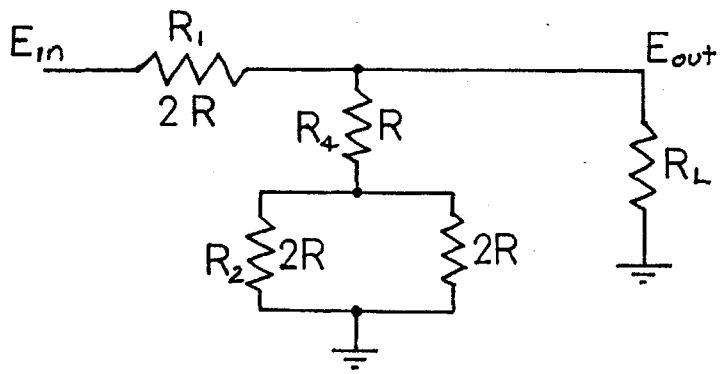
$$Ro = \frac{R_1(R_4 + R)}{R_1 + R_4 + R} = \frac{2R\ 2R}{4R} = R$$

The output voltage can be calculated as follows. The first step is to simplify Figure 2.3 to that shown in Figure 2.3(b). Figure 2.3(b) yields itself to another simplification shown in Figure 2.3(c) and by Thevenins theorem this is further reduced to Figure 2.3(d) and

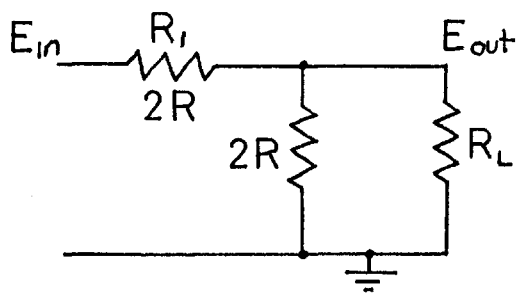
$$E_{out} = \frac{1}{2}\ \frac{R_L}{R + R_L}\ .\ E_{in}$$



(a)



(b)



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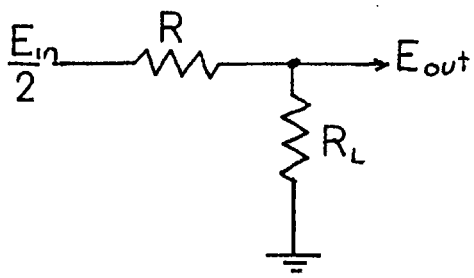


(d)

Fig. 2.3

Conversion of Binary Number 100

Figure 2.3(d) will be the same for any number of bits if the M.S.B. is a one, and all other bits are zeroes. Therefore, increasing the number of bits of the D/A converter does not change the weighting of each bit. However, the resolution of conversion will be reduced as the number of bits is increased.

Figure 2.4(a) shows the same converter switched to convert binary number 010. This circuit is shown simplified in Figure 2.4(b), and using Thevenins theorem a further simplification yields Figure 2.4(c), which in turn yields Figure 2.4(d)

$$\text{Therefore } E_{out} = \frac{E_{in}}{4} \frac{R_L}{R + R_L}$$

A similar procedure is followed in Figure 2.5 for a conversion of the binary number 001 and yields

$$E_{out} = \frac{E_{in}}{8} \frac{R_L}{R+R_L}$$

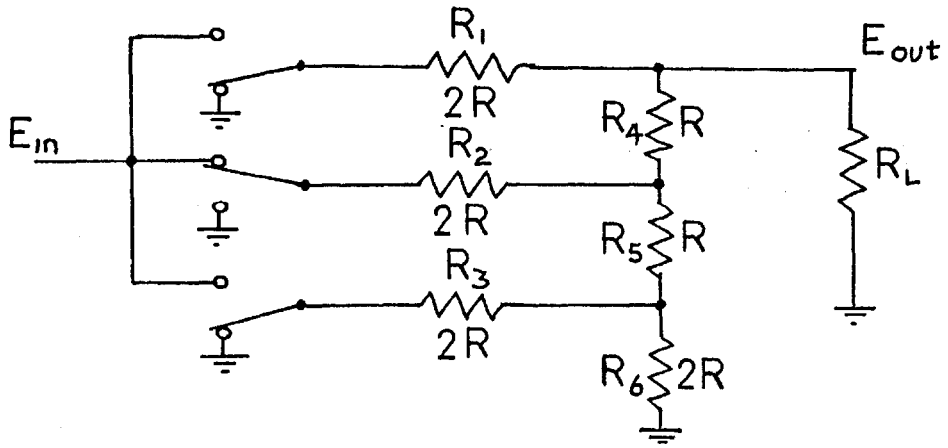
The superposition theorem can be used to calculate the analog output for any digital input, using the equation

$$E_{out} = \left(\frac{1}{2} D_1 + \frac{1}{4} D_2 + \frac{1}{8} D_3 + \ldots\ldots\ldots + \frac{1}{2^n} D_n\right) \frac{E_{in} R_L}{R + R_L}$$

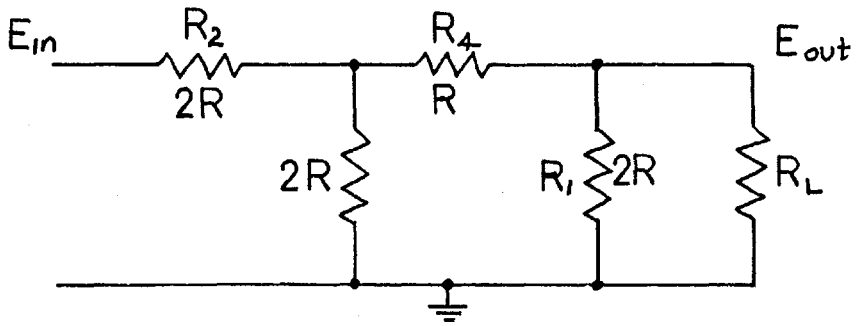
where the D's represent the state of the digital input of a particular bit.

The actual magnitude of R is determined by R_L, accuracy requirements and conversion rate.

The advantage of this circuit is that all resistors in the ladder can be identical. Two may be connected in series to give 2R. Also their temperature coefficients are easily matched.



(a)



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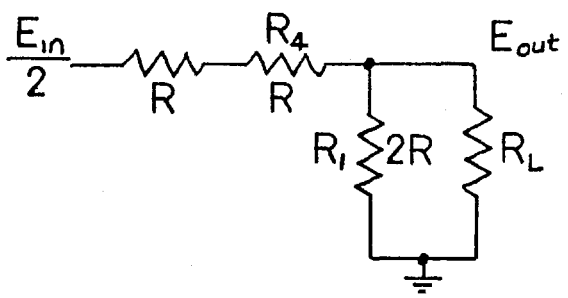

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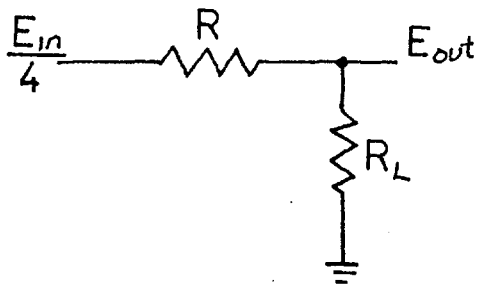
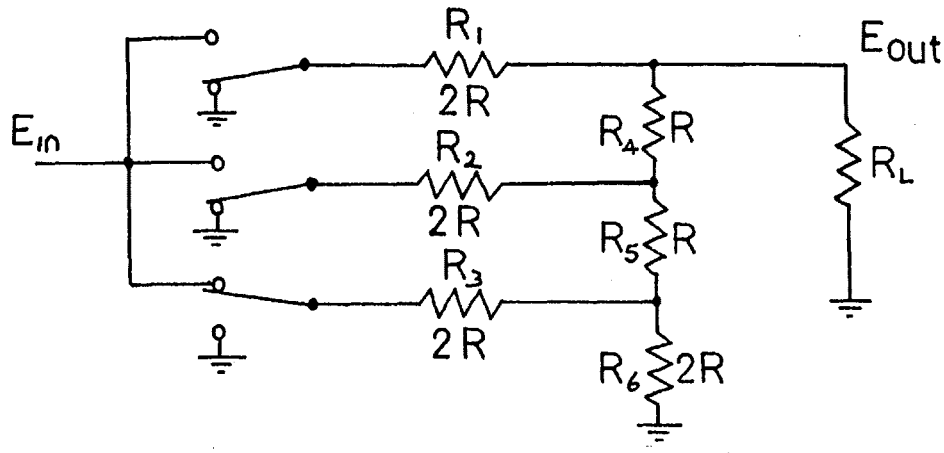


(d)

Fig. 2.4

Conversion of Binary Number 010



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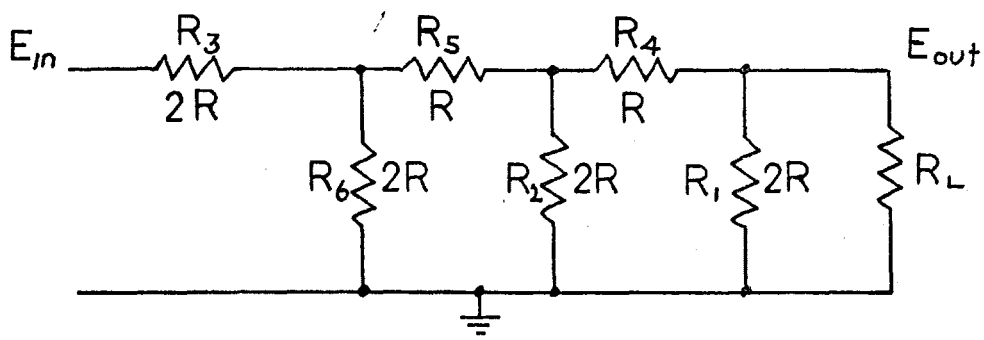

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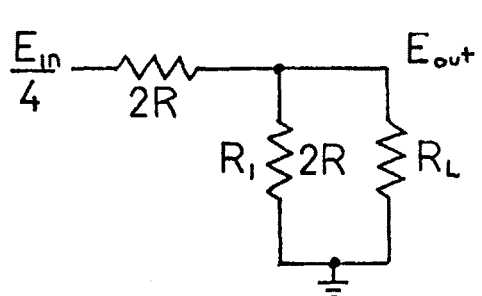
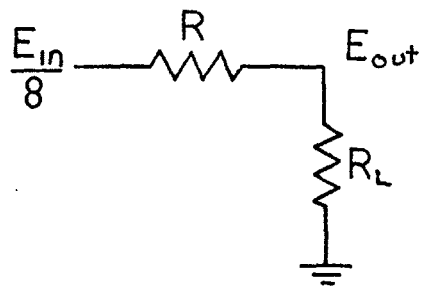


(c)



(d)

Fig. 2.5

Conversion of Binary Number 001

For simplicity, the switches shown in this section have been shown as mechanical contacts. In practise, due to required switching speeds, reliability, operating power and size, the switching is usually carried out by electronic components.

2.1.2 Operation of a Successive Approximation A/D Converter

A Successive Approximation A/D Converter is now considered in more detail as shown in Figure 2.6. This system is most easily understood by taking an example. Assume the analog input is 4 volts and that the maximum possible input is 10 volts. Initially the flip-flops, FF1 to 4, are set to the "zero" state by the reset pulse, and a "one" appears at output 1 of the ring counter. This "one" triggers flip flop FF1 to the "one" state and the digital number 1000 is converted to an analog signal by the D/A decoder. The comparator now has an analog input of 4V and a 5V input from the D/A decoder, this causing the comparator to switch to the "one" state. The next clock pulse occurs and advances the ring counter, which switches FF2 to the "one" state and switches FF1 back to the "zero" state via gate 1. The D/A decoder now supplies 2.5 volts to the comparator, that is, less than the 4 volt analog input so the comparator output switches to the "zero" state. The ring counter output now advances one pulse and switches FF3 into the "one" state but it does not switch FF2 back to the "zero" state because gate 2 is open. The D/A decoder output now corresponds to 0110 and hence supplies 3.75 volts to the comparator. The comparator therefore stays in the zero state. The ring pulse advances and switches FF4 to the

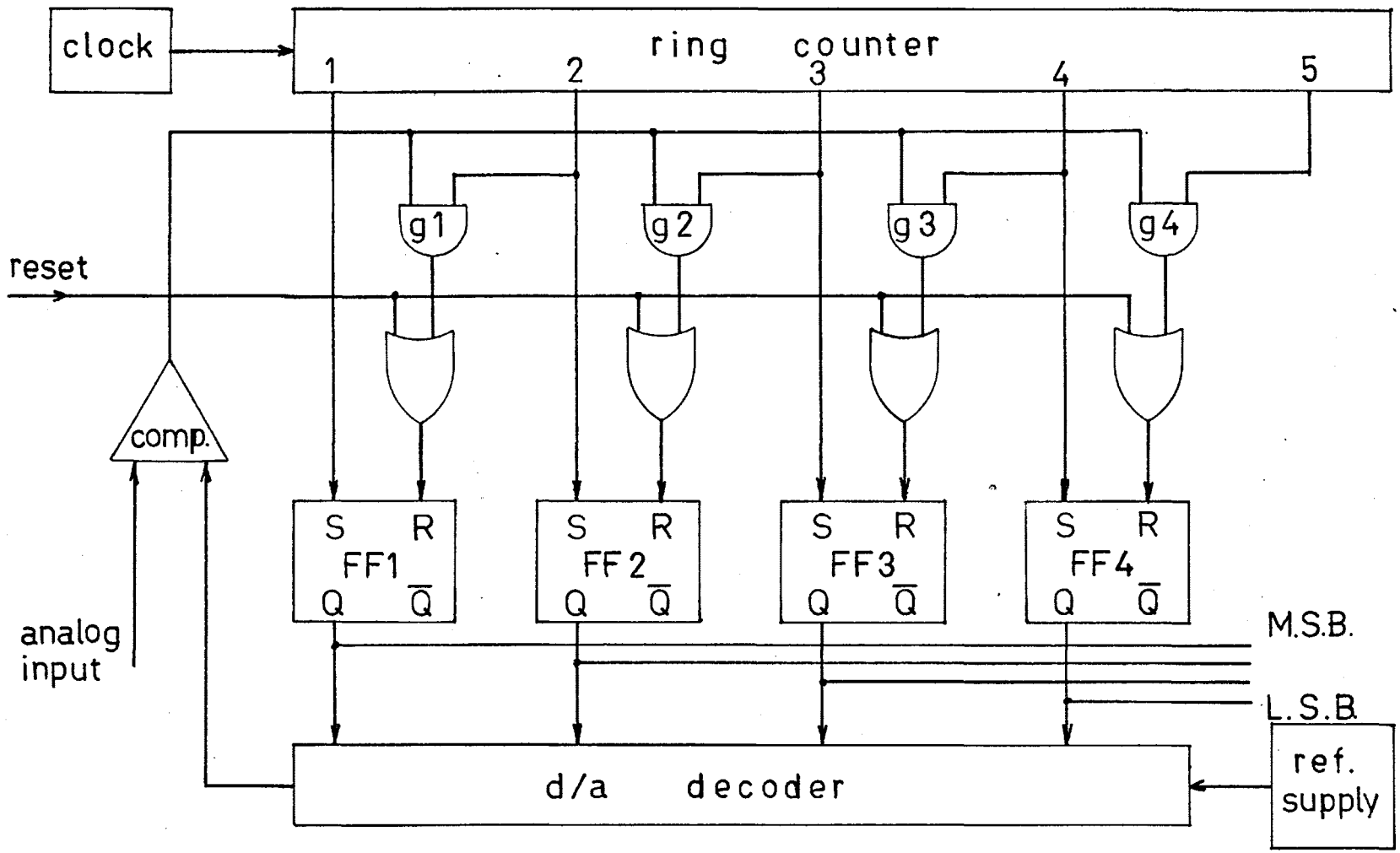


Figure 2.6

Successive approximation A/D converter

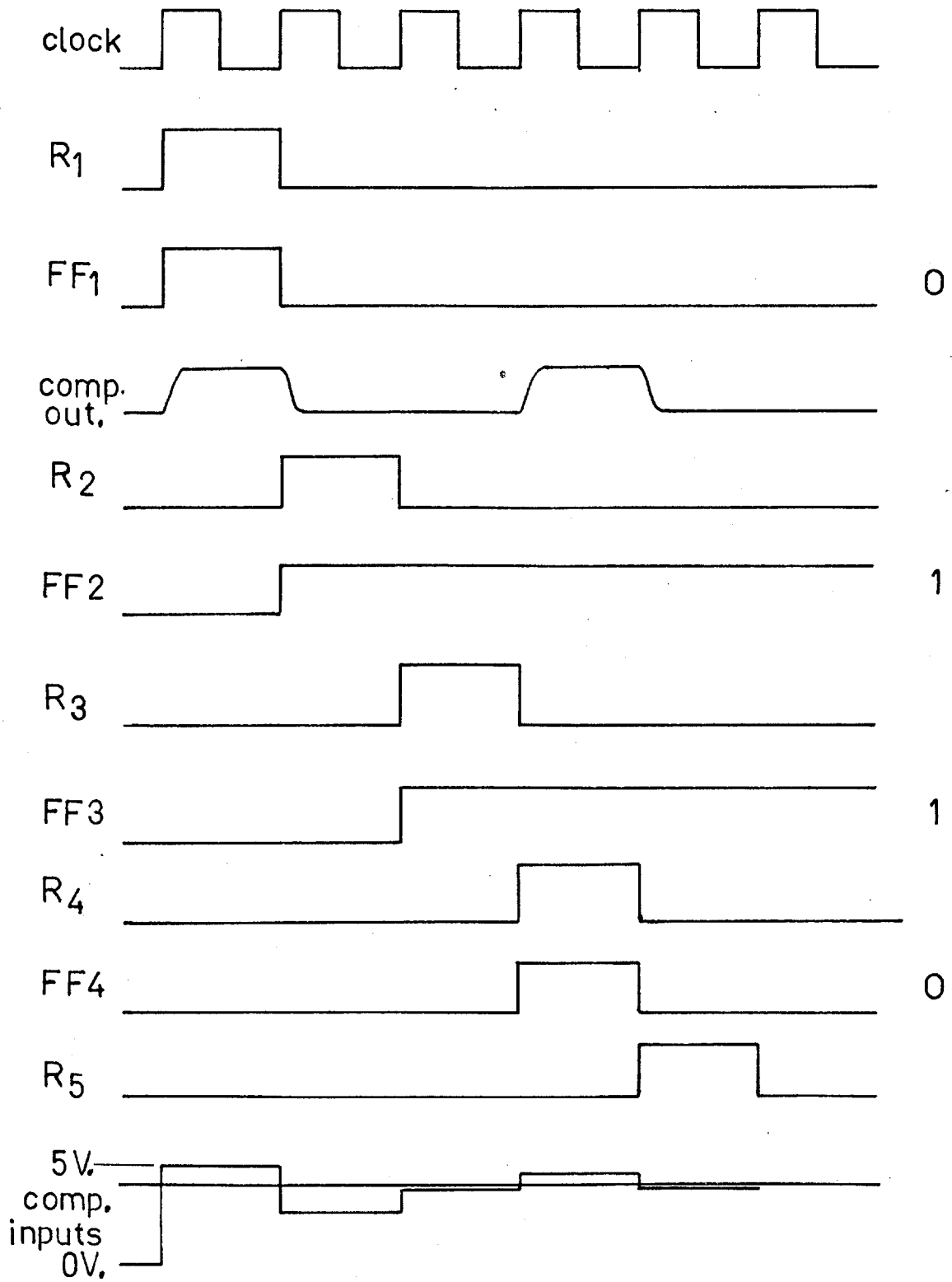


Fig. 2.7

Timing Diagram of Successive Approximation A/D Converter

"one" state leaving FF3 in the "one"state. The D/A decoder output now corresponds to 0111, that is 4.375 volts are applied to the comparator input. The comparator switches to the "one" state opening gate 4, and FF4 is switched back to the "zero" state. The digital output is now available in a parallel form and is 0110. A timing diagram illustrating this example is shown in Figure 2.7.

2.1.3 Aperture Time

Usually the analog signal to be digitized is a time varying signal, and hence it is necessary to know when the signal had the value given by the output. The uncertainty in this time is defined as the aperture time. If a sinusoidal input is assumed, the maximum possible error due to the aperture time occurs when $\frac{dE}{dt}$ is a maximum, that is, at the zero crossover point, and can be calculated as follows:

$$E = E_p \sin\omega t$$

$$\frac{dE}{dt} = E_p \omega \cos\omega t = E_p 2\pi f \cos\omega t$$

$$\text{At crossover } \frac{dE}{dt} = E_p 2\pi f$$

where dt is the aperture time. Therefore, the uncertainty error voltage

$$dE = E_p 2\pi f \, dt$$

is directly proportional to the aperture time.

In the successive approximation converter the aperture time is equal to the total word conversion time. The aperture time can however, be reduced by using a sample and hold circuit at the converter input. The uncertainty error is

then reduced by the ratio of the A/D conversion time to the sampling time of the sample and hold circuit.

2.1.4 Sample and Hold Circuit[6]

A typical Sample and Hold Circuit using an operational amplifier is shown in simplified form in Figure 2.8. When the FET is on, the circuit operates in the sample mode as a unity gain inverter, and has an acquisition time t_a dependent on the time constant of RC:-

$$t_a = RC \ln \left(\frac{100}{\% \text{ accuracy}} \right)$$

The acquisition time is the time required for the voltage across the capacitor to rise to within a specified fraction of the input voltage. When the FET is off, the circuit is in the hold mode, and the voltage that was across C at the instant of switching is retained. The discharge time depends mainly on the leakage of C and also the off resistance of the FET and the amplifier input current. With R = 1Kohm and C = 100pF the circuit settles to 0.05% in approximately 0.8μsec if the on resistance of the FET is negligible compared with 1Kohm.

2.2 Simultaneous A/D Converter[1.2.3]

The simultaneous method requires one comparator for every digital quantization level, and is illustrated in Figure 2.9.

Each comparator has a reference input and the analog signal input. The outputs from the comparators drive logic circuits which provide the digital readout. A two bit converter is shown in detail in Figure 2.10. The comparators are

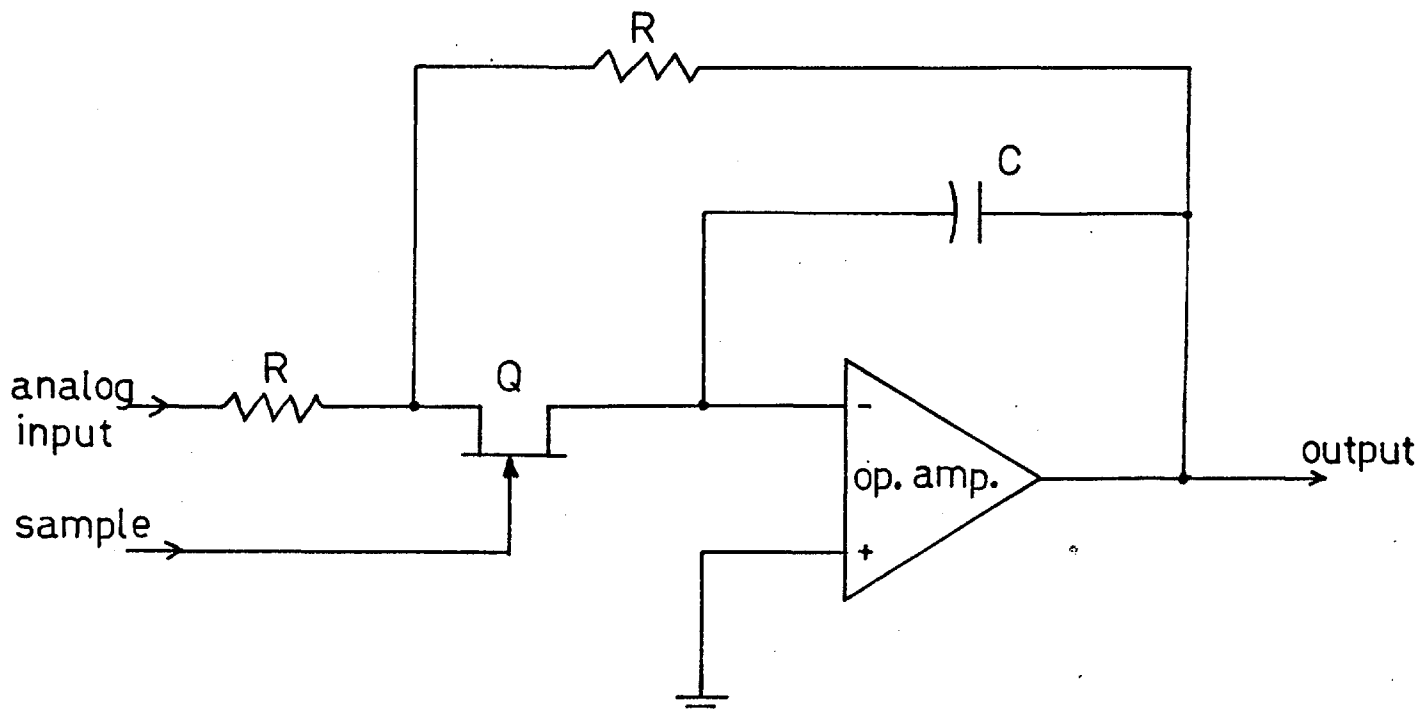


Fig. 2.8

Simplified Sample and Hold Circuit

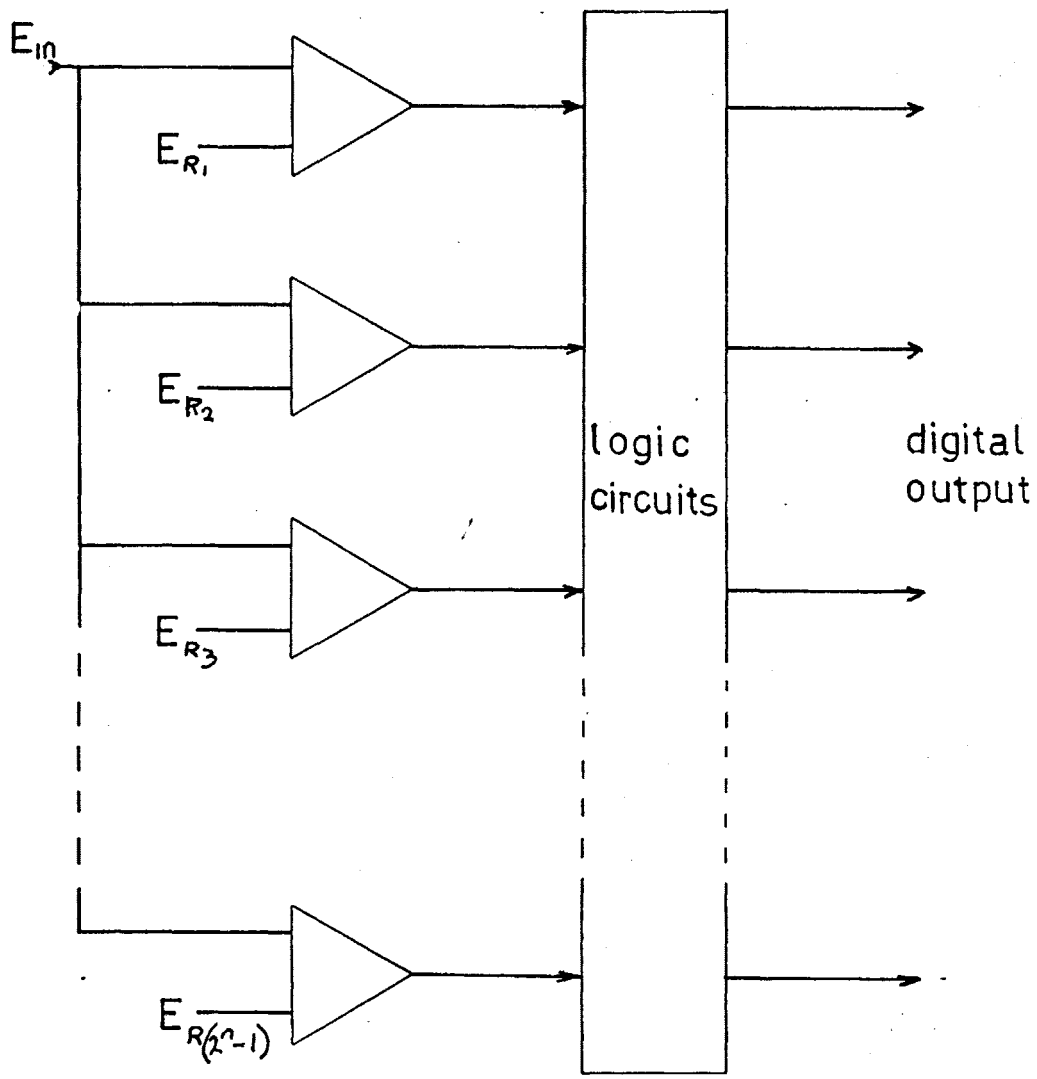


Fig. 2.9

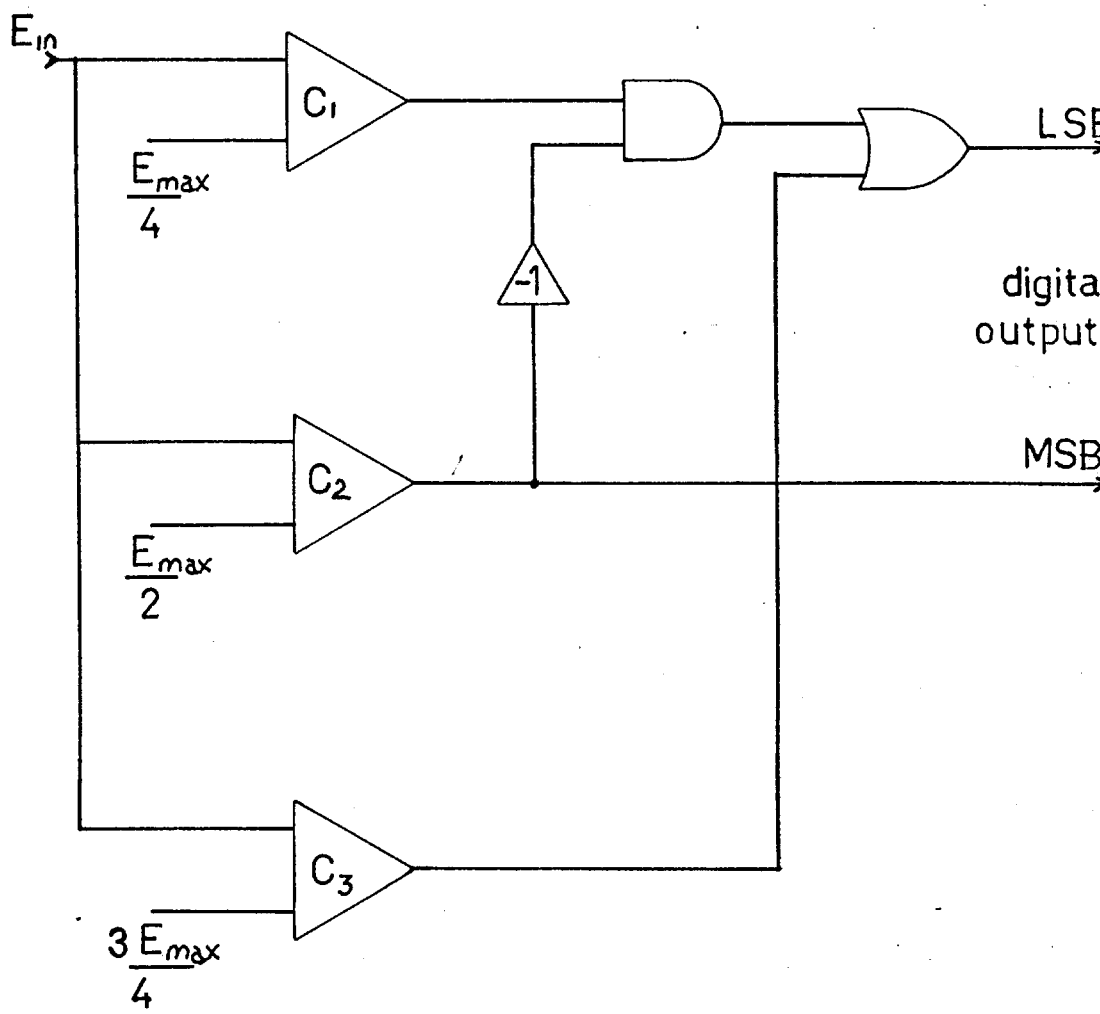
Block Diagram of Simultaneous A/D Converter

in the "one" state if the analog input is greater than the reference input. Therefore, if all three comparators are in the "one" state, the input is between $\frac{3E}{4}$ and E. If C_1 is in the "one" state and C_2 and C_3 are in the "zero" state, the signal is between $\frac{E}{4}$ and $\frac{E}{2}$. This is the fastest type of A/D converter since only one step is required to complete the conversion; however, for systems requiring a large number of bits, this system requires a prohibitive number of comparators, reference voltages, and associated logic blocks. This rapid expansion is illustrated by Figure 2.11 which shows how many additional elements are needed to increase to three bits. An eight bit conversion would require; $2^n - 1 = 1023$ comparators, reference voltages; and $2^n - 2 = 1022$ two input "and" gates and inverters.

A/D converters that are a combination of the simultaneous and successive approximation types are also available. $\frac{n}{N}$ steps are required to complete a conversion, where n is the total number of bits and N is the number of bits converted per step.

2.3 Counter Type A/D Converter[1.2.3]

The counter type A/D converter also uses a D/A decoder in a feedback loop, and is shown in Figure 2.12. The counter advances the D/A decoder output by one step for every clock pulse it receives, resulting in the staircase waveform shown in Figure 2.13. When the D/A decoder output exceeds the analog input the comparator output drops to the zero level and opens the gate; the digital output is then available in a parallel form.



E_{max} is the maximum value of the analog input

Fig. 2.10

Two-bit Simultaneous A/D Converter

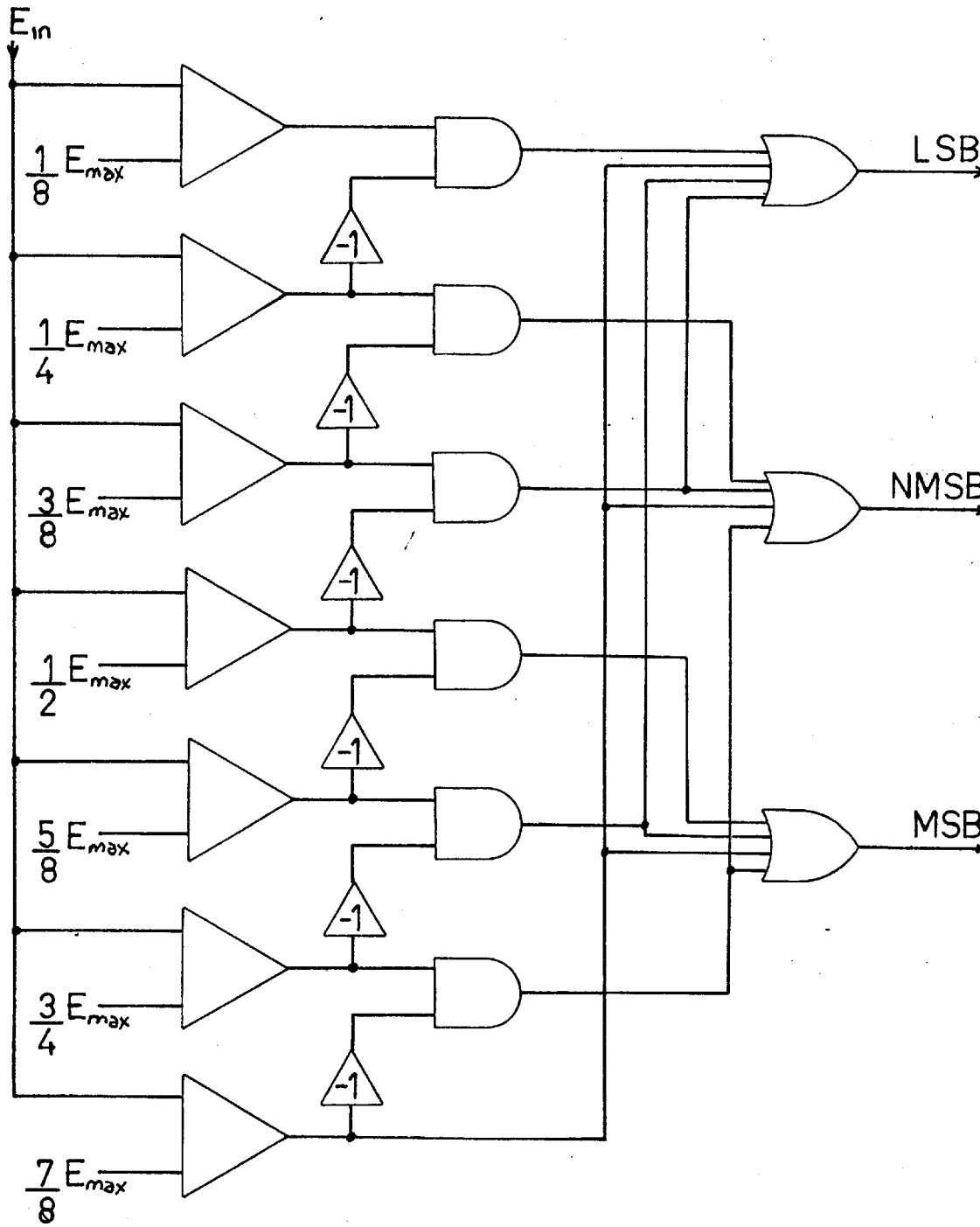


Fig. 2.11

Three-bit Simultaneous A/D Converter

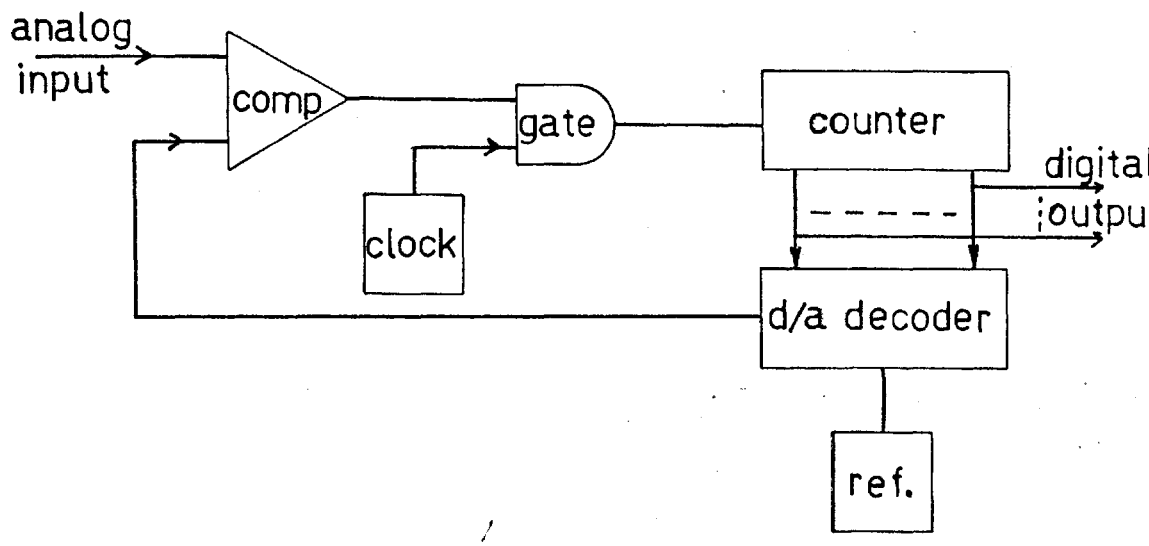


Fig. 2.12

Counter Type A/D Converter

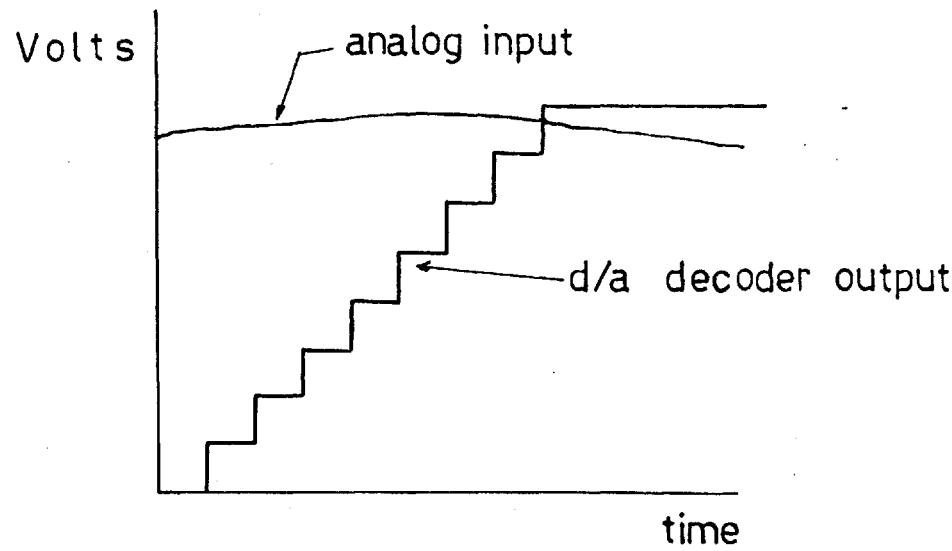


Fig. 2.13

Output of D/A Decoder

A more detailed diagram is shown in Figure 2.14 and the timing diagram related to it is shown in Figure 2.15. A reset pulse is used to reset all flip-flops to the zero state. The counter then counts until the D/A decoder output exceeds the analog input. The digital output is then 1010, as shown in Figure 2.15.

This type of A/D converter is one of the least complex, and is suitable for multiplexed inputs, but it is relatively slow, since for an analog input that is the systems maximum, the conversion requires $(2^n - 1)$ process steps, where n is the number of bits.

2.4 Continuous Counter A/D Converter[2.3]

The continuous counter A/D converter is a modified form of the counter A/D converter; the simple counter is replaced with an up-down counter as shown in Figure 2.16. The counter then counts up or down depending on the direction of the change in magnitude of the analog input. If the input signal does not change by more than $\pm$ 1 LSB between conversion steps, the digital equivalent of the input voltage can be sampled at any time.

For this criteria to hold the maximum rate of change of the input voltage must not exceed the maximum rate of change of the converter. From this statement an expression for the maximum allowable input frequency can be derived as follows[3]

$$\text{Maximum rate of change of converter} = \frac{E_{Ref}}{2^n \Delta T} \qquad (1)$$

Where E_{ref} is the full scale reference voltage, n is the number of bits and ΔT is the time per step.

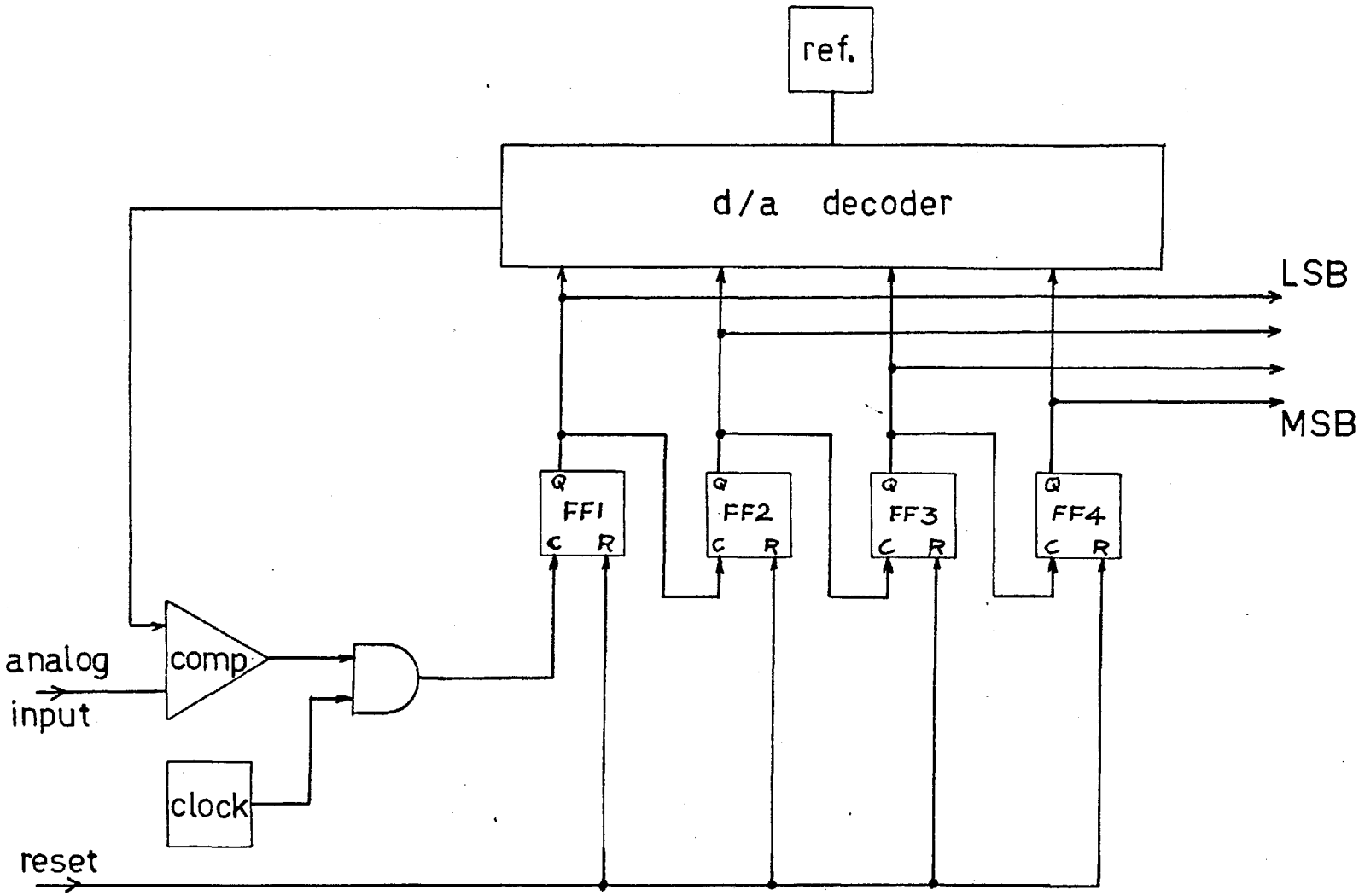


Fig. 2.14

Four bit Counter Type A/D Converter

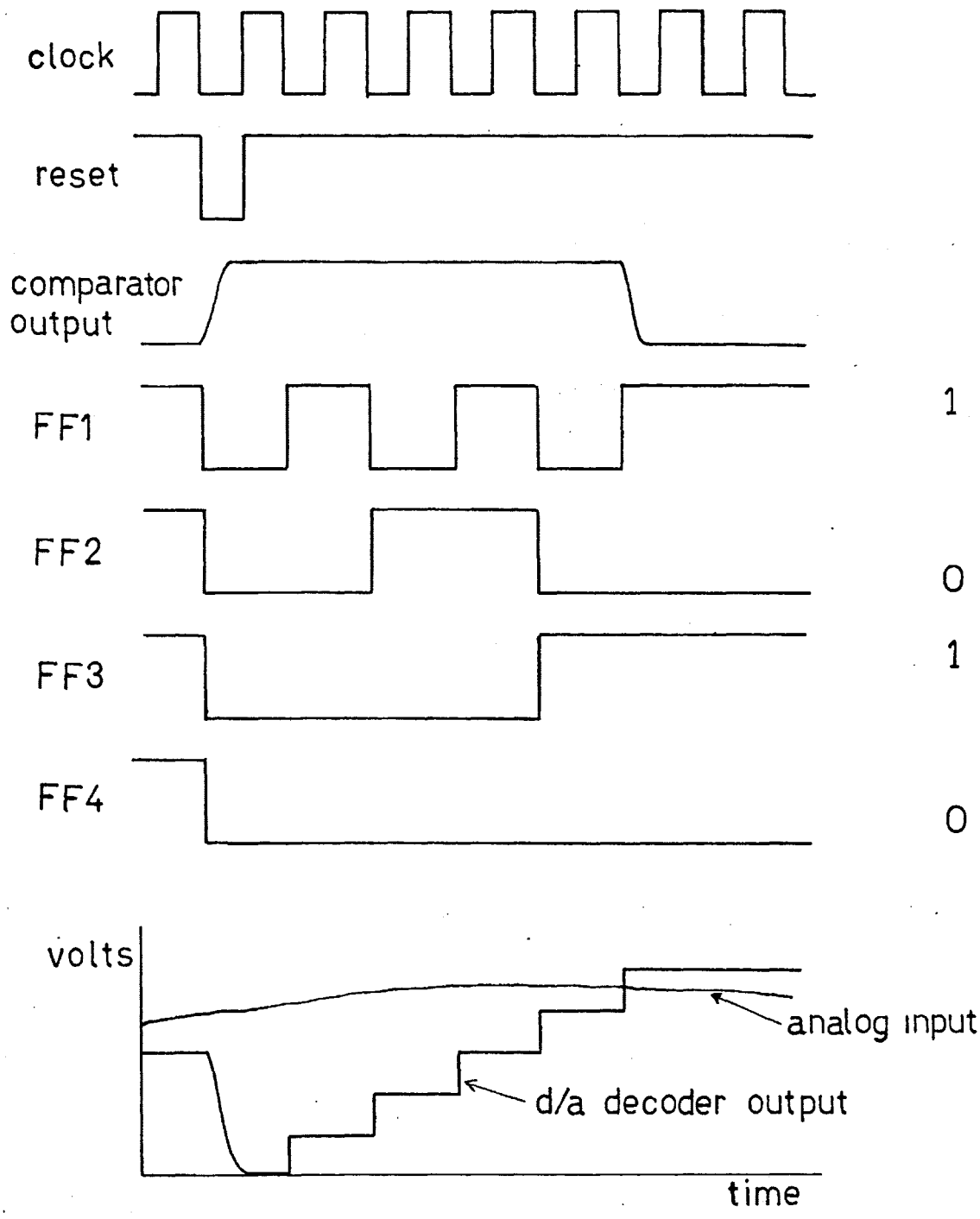
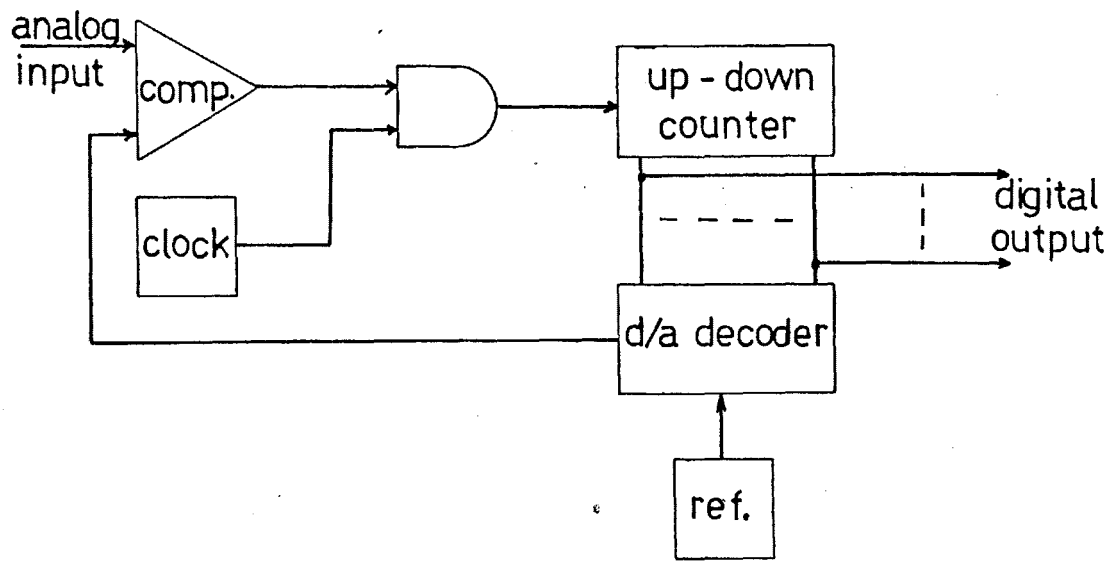
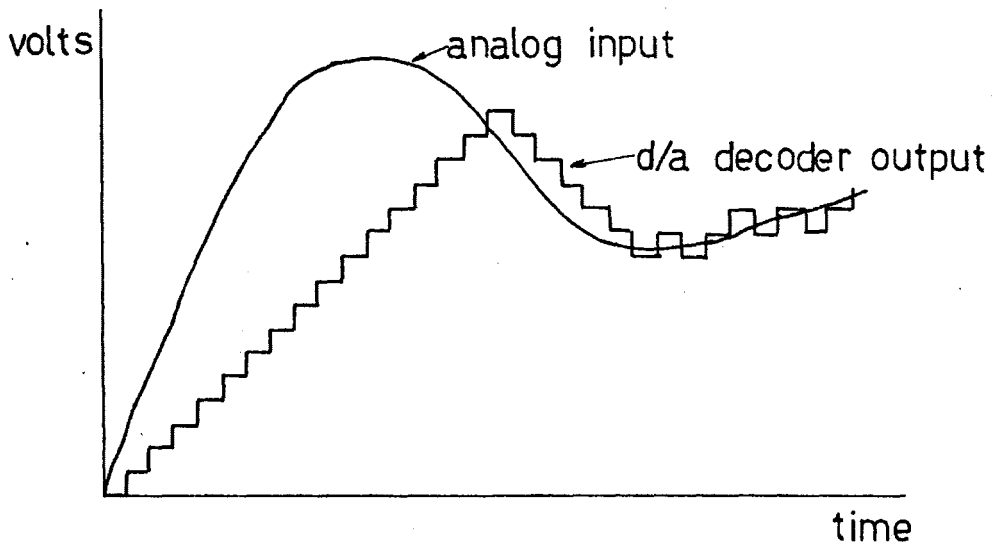


Fig. 2.15

Timing Diagram for Counter type A/D Converter



Continuous Counter A/D Converter



Typical Response

Fig. 2.16

As shown in section 2.1.3 the maximum rate of change of the sine wave is

$$2\pi E_p f = \pi E_{p-p} f \qquad (2)$$

where E_p is the peak value of the input signal, E_{p-p} is the peak to peak value and f is the frequency of the input signal. Combining equations 1 and 2 gives

$$\pi E_{p-p} f_{max} = \frac{E_{ref}}{2^n \Delta T}$$

where f_{max} is the maximum allowable input frequency.

But $E_{ref} = E_{pp}$ therefore $f_{max} = \frac{1}{2^n \Delta T \pi}$ (3)

This means an eight bit converter with a clock frequency of 1MHz has a maximum allowable input frequency of 1.25kHz.

If the condition of equation 3 is not satisfied the converter can require up to 2^n steps to catch up. As a result of this, this type of converter is not very suitable for multiplexed inputs.

2.5 Ramp Type A/D Converter[1.2.3.7]

The object of the ramp technique is to measure the length of time it takes for a linear ramp to change from a zero level to the input voltage. A system capable of this is shown in Figure 2.1[7]. A conversion commences when the control logic opens switch S, which causes the current source I to start charging C in a linear manner, and closes the gate, which causes clock pulses to reach the counter. When the capacitor has charged to E_{in} the comparator changes state and the control logic opens the gate, stopping the count.

Since the count stored is proportional to the width of the pulse supplied to E_{in}, the count stored is a measure of the amplitude of the analog input E_{in}.

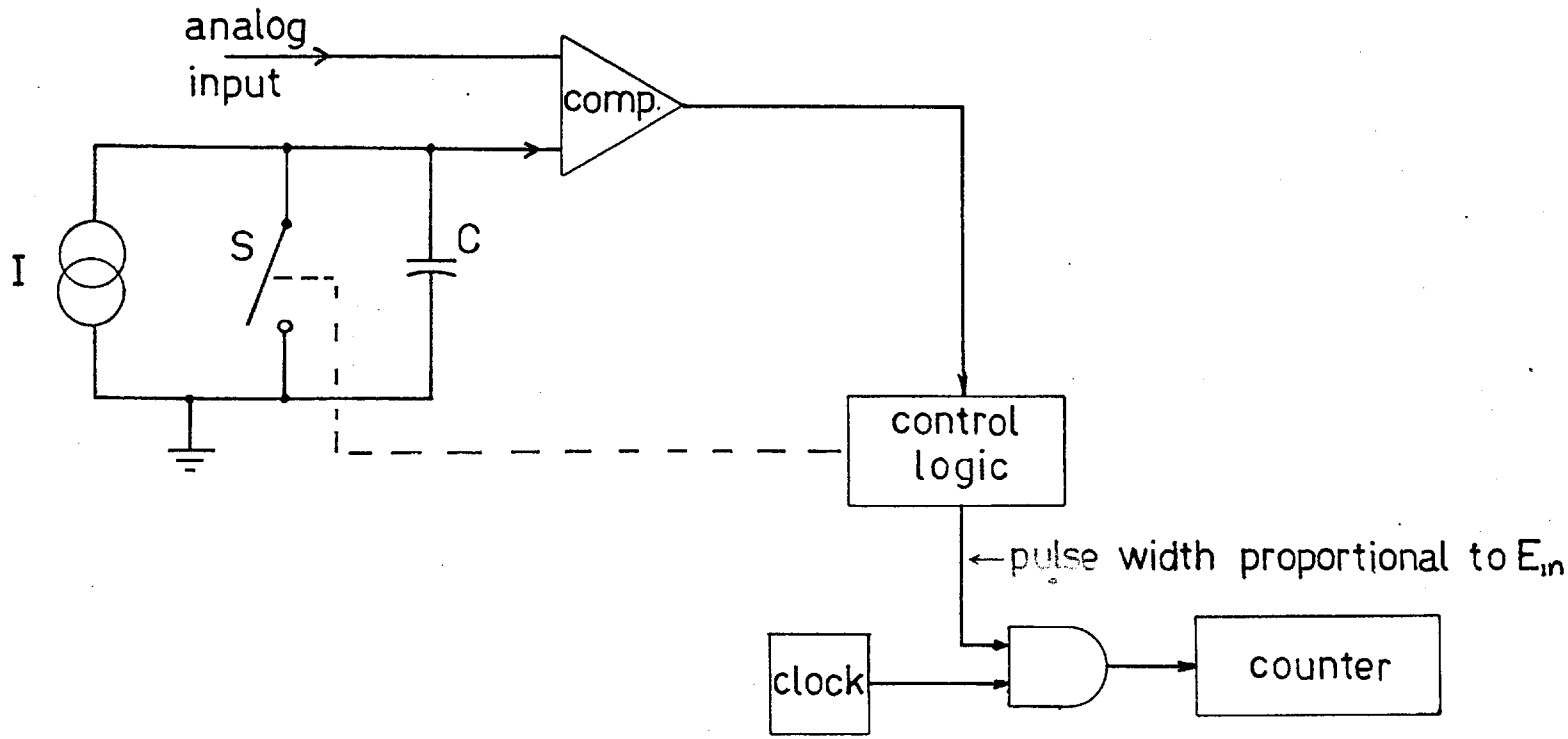


Fig. 2.17

Block Diagram of a Ramp type A/D Converter

A more detailed ramp converter is shown in Figure 2.18[2] and its timing diagram in Figure 2.19. The reset signal:

(l) Prevents clock pulses passing through gate Gl to the counter

(ll) Resets the counters to zero, and

(lll) Resets flipflop FFl

The output of FFl turns transistor Q2 on. When the reset line returns to the "one" condition, FFl is set via gate G2, turning Q2 off which causes the capacitor to start charging, its current being supplied by constant current source Q2. Gate Gl is enabled and clock pulses enter the counter.

Since the comparator is in the "one" state, gates G3 to G_{n+2} are disabled. When the ramp voltage across capacitor C reaches $E_{in,}$ the comparator switches to the "zero" state, disabled gate Gl and enables gates G3 to $G_{n+2.}$ The outputs of gates G3 to G_{n+2} give the counters accumulated count, which is a digital measure of the analog input voltage $E_{in.}$

This system has the advantage of simplicity, but it is relatively slow, requiring one pulse for every quantizing level; that is, a seven bit converter would require 127 pulses before reaching a full scale count. The accuracy of the system is mainly dependent on:

(l) Errors in the capacitor value

(ll) Errors in the constant current source, and

(lll) Errors in the comparator

Accuracies of better than a few tenths of a per cent are difficult to achieve. This system is also very susceptible to noise, because a noise signal on E_{in} would cause it to drop below the ramp voltage and as a result trigger the comparator.

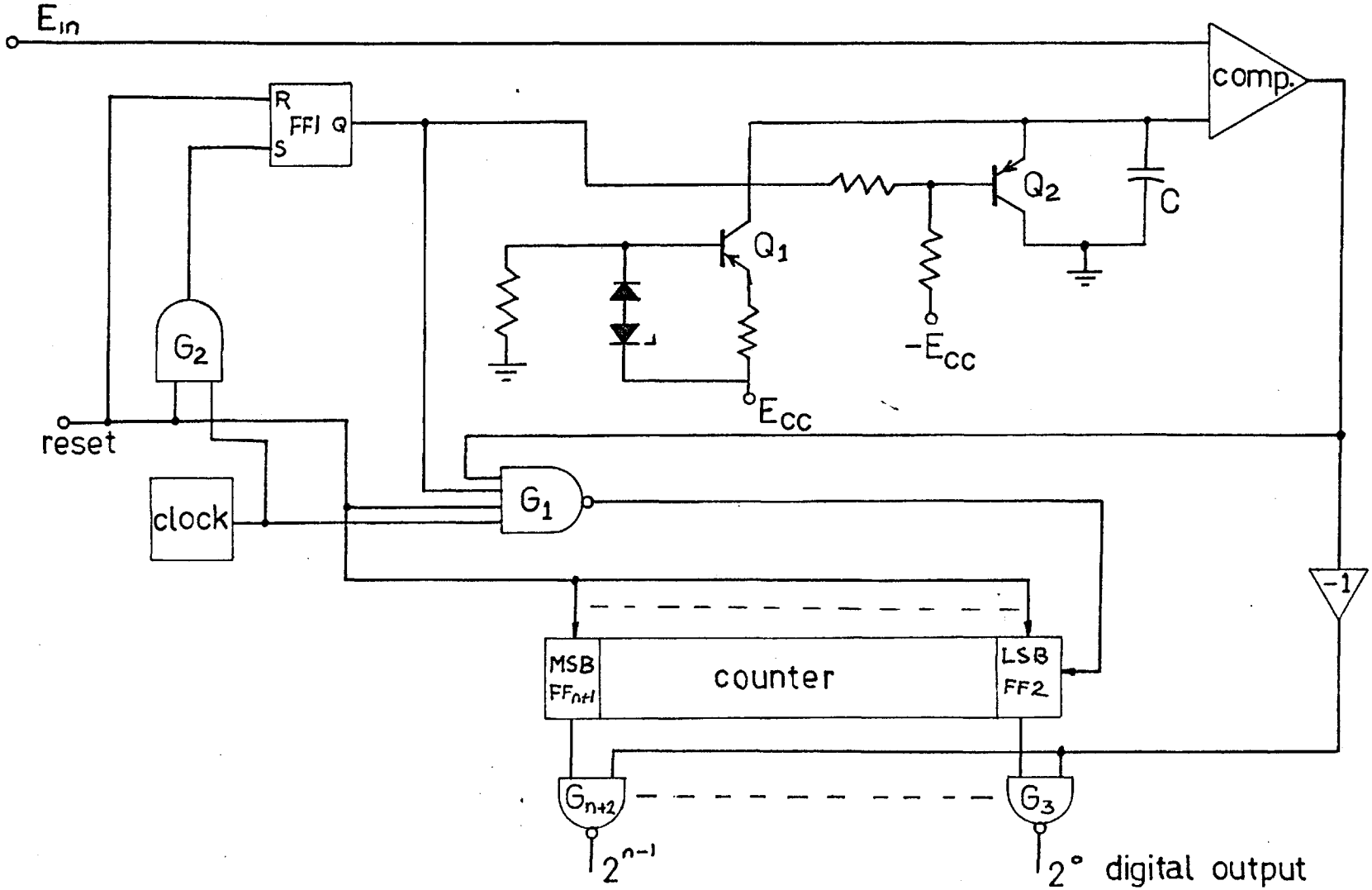


Fig. 2.18

Detailed Diagram of a Ramp type A/D Converter

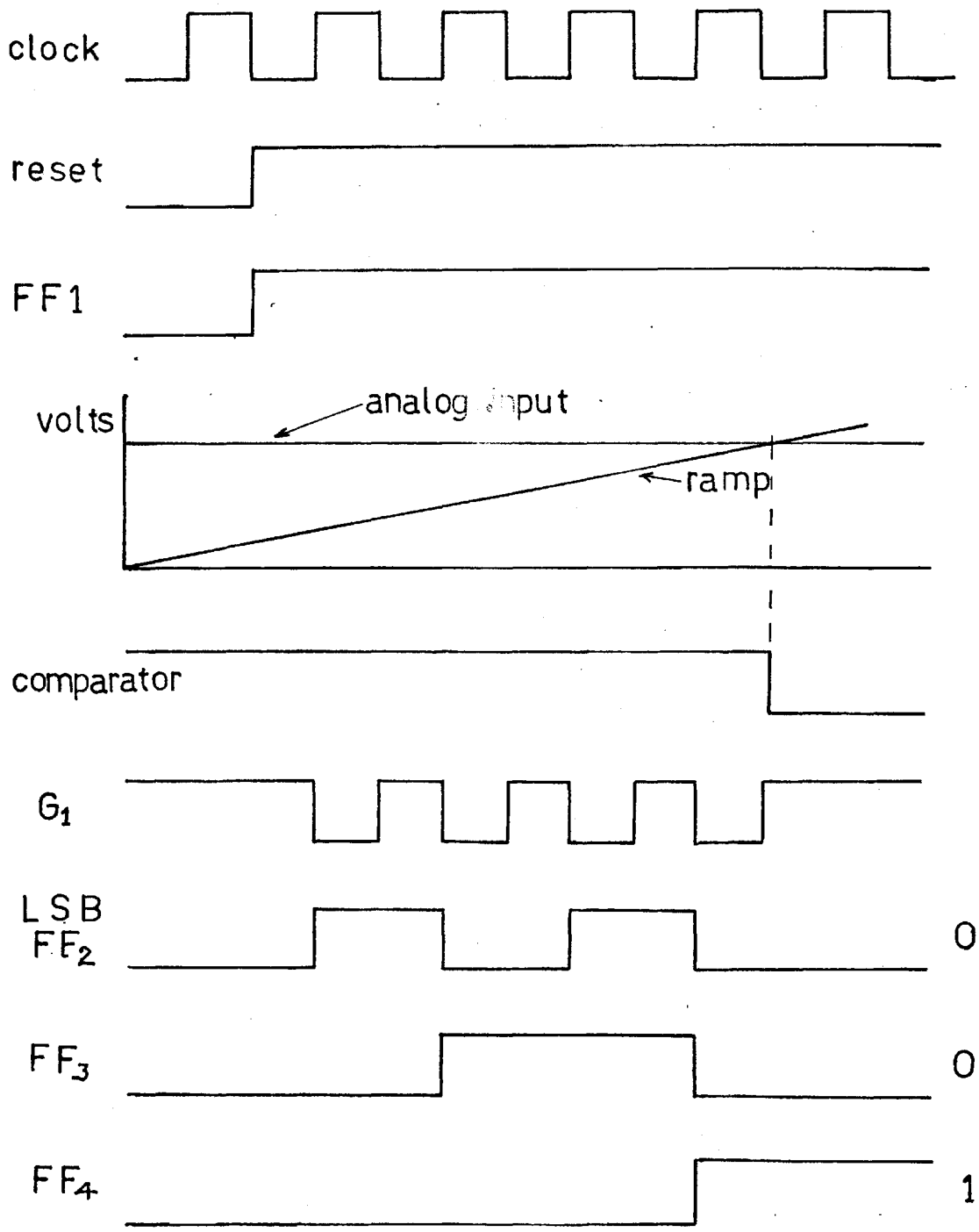


Fig. 2.19

Timing Diagram of a Ramp type Converter

2.6 Dual Ramp or Double Integration A/D Converter[1.2.8.9]

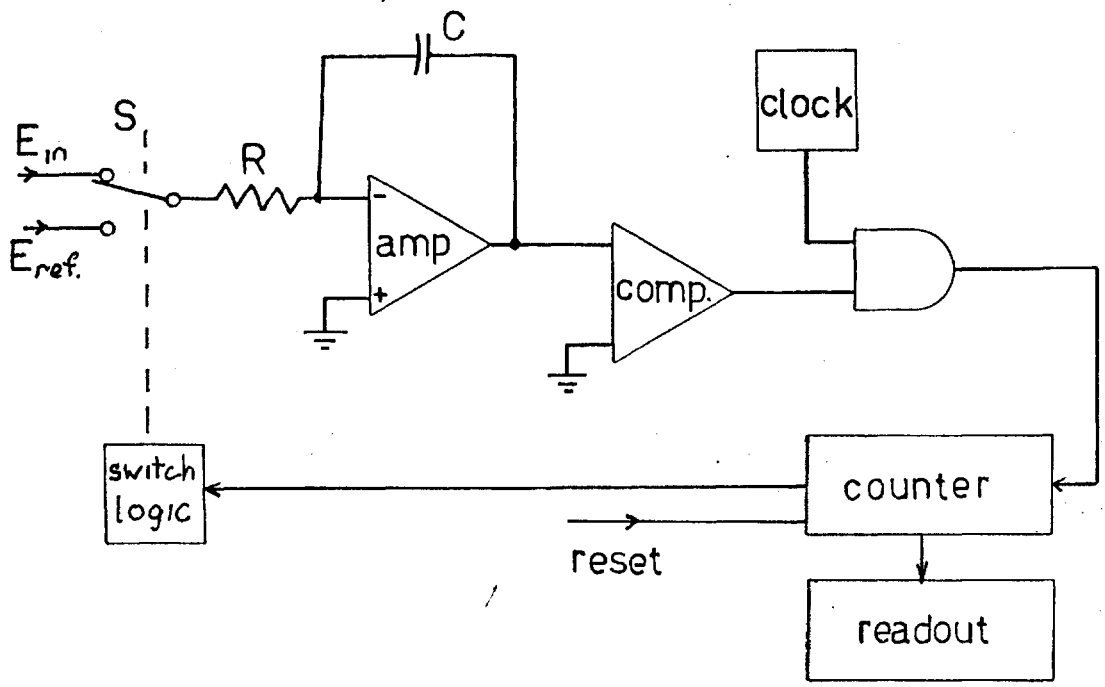
Some of the inaccuracies of the Ramp converter are overcome in the dual ramp converter. In this system, the analog input is integrated for a fixed time interval, the integrator output at the end of this time being proportional to the input signal averaged over the integration time. A reference voltage of opposite polarity to the analog input, and with a magnitude at least as large as the maximum allowable analog input, is then integrated until the integrator's output is reduced to zero. The length of time taken by this second integration is a measure of the amplitude of the input voltage.

A block diagram of a dual ramp converter is shown in Figure 2.20. The reset pulse sets all the counter flip flops to zero, and connects switch S to E_{in}. Integration commences and the comparator switches to the "one" state. Integration continues until the counter fills with "ones", at this point the switch is switched to $-E_{Ref}$, the counter is reset to zero, and integration of $-E_{Ref}$ continues until the comparator changes to the "zero" state, at which point the gate is disabled and the counter receives no further pulses. The digital readout then represents the analog input voltage E_{in}. At the end of time t_1, the integrator output voltage is

$$V_o = \frac{1}{RC} \int_o^{t_1} E_{in} dt = E_{in} \frac{t_1}{RC}$$

At time t_1, the integrator starts to integrate E_{ref} and the voltage drops from V_o to zero during the time interval $t_2 - t_1$.

$$\text{Hence } V_o = \frac{1}{RC} \int_{t_1}^{t_2} E_{ref}\, dt = E_{ref} \frac{(t_2 - t_1)}{RC}$$



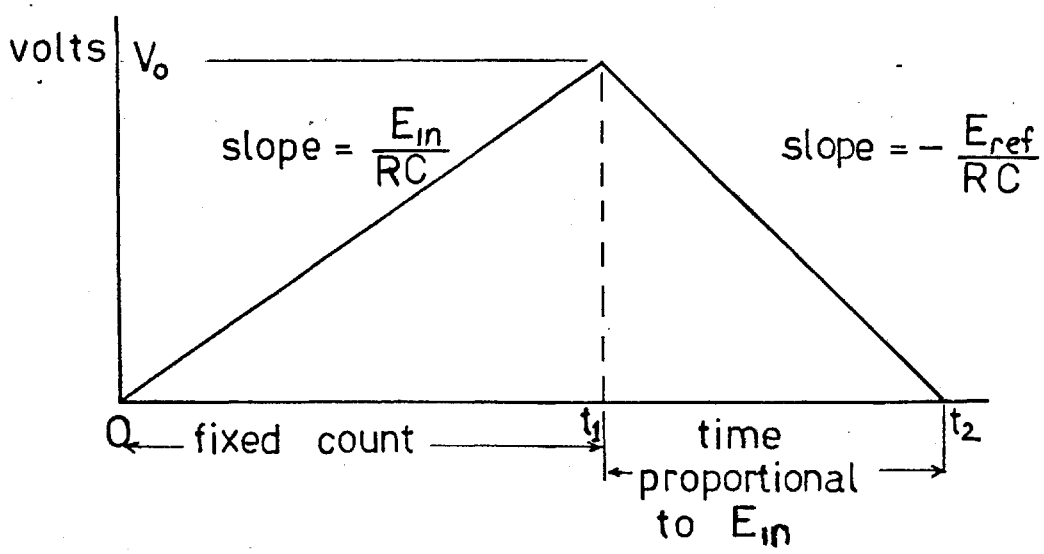


Fig. 2.20
Block Diagram and Operating Characteristic of the dual Ramp Converter

$$\text{Therefore } \frac{E_{in}t_1}{RC} = E_{ref}\frac{(t_2 - t_1)}{RC}$$

$$\text{and } \quad t_2 - t_1 = \frac{E_{in}}{E_{ref}}\, t_1$$

Therefore $(t_2 - t_1)$ is independent of the integrator time constant, and since the same clock is used to measure both the first and second integration intervals, a precision clock is not required.

This type of converter is still relatively simple, and is more accurate than the ramp converter. However, a price has been paid for the increased accuracy, the price being an increased conversion time. For a full scale conversion of n bits, a total of 2^{n+1} clock pulses are now required.

Noise error is reduced in this system because the input signal is integrated, over a period of time.

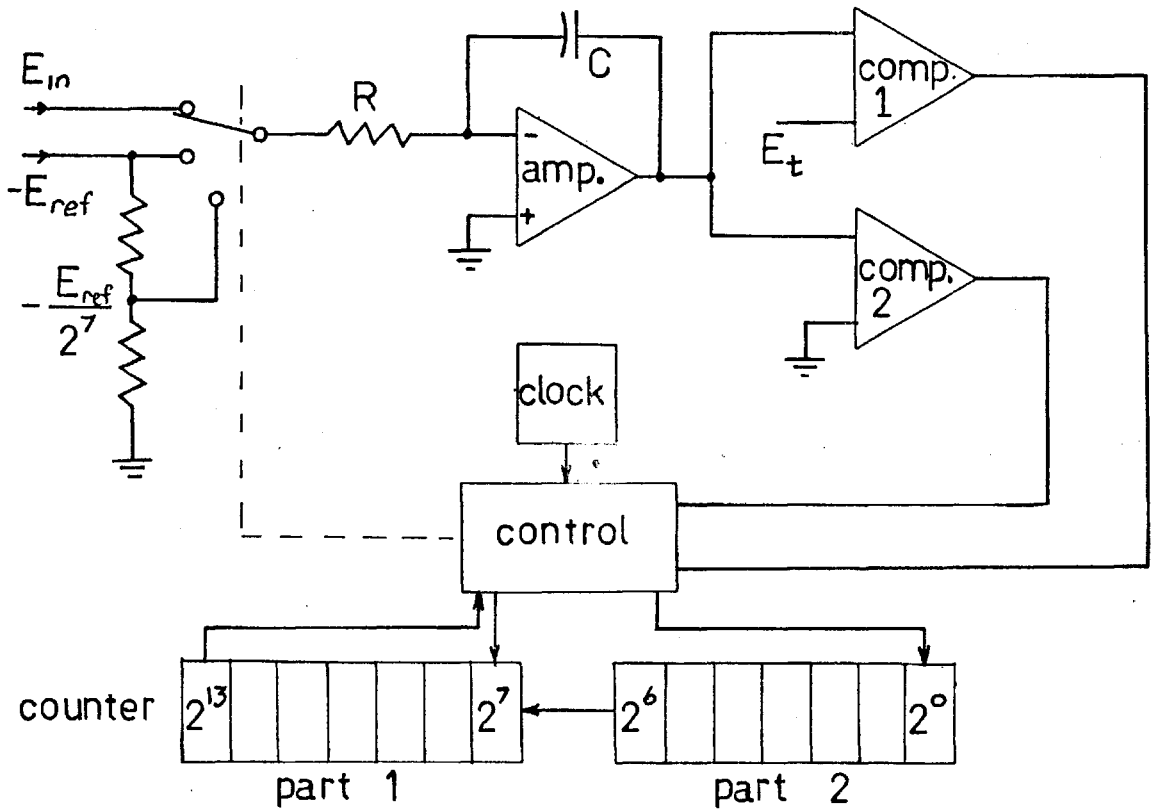
This type of converter is widely used in digital voltmeters.

2.7 Triple Ramp A/D Converter[10]

The triple ramp A/D converter was designed to have the accuracy of the dual ramp converter but be considerably faster. A block diagram of a 14 bit converter is shown in Figure 2.21. The magnitude of the reference voltage E_t on the input to comparator 1 is slightly larger than $E_{ref}/2^7$.

The converter operates as follows:- at t_o integration of E_{in} commences and continues until part 1 of the counter has received 2^7 clock pulses, the last pulse resetting part 1 to zero. The integrator output is then

$$V_o\,(t_1) = \frac{E_{in}}{RC}\,(t_1 - t_o) \qquad (1)$$



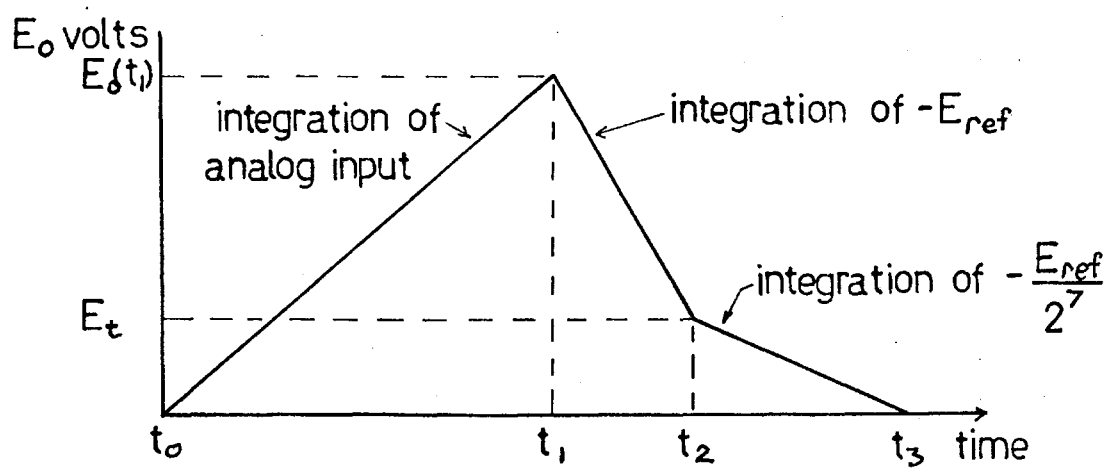


Fig. 2.21

Block Diagram and Operating Characteristic of the Triple Ramp Converter

$$\text{where } t_1 - t_o = \frac{2^7}{f_c} \text{ secs} \tag{2}$$

where f_c is the clock frequency. $-E_{ref}$ is now switched to the integrator input and integrated. During this second integration period clock pulses are again applied to part 1 of the counter. Integration continues until the output has been reduced to E_t; at this time, t_2, comparator 1 changes state.

The number of counts stored in part 1 of the counter at this time is

$$N_1 = 2^7 f_c (t_2 - t_1) \tag{3}$$

The integrator output at time t_2 is

$$V_o (t_2) = \frac{E_{in}}{RC} (t_1 - t_o) - \frac{E_{ref}}{RC} (t_2 - t_1) \tag{4}$$

The voltage $\frac{-E_R}{2^7}$ is now switched to the integrator input, and integration continues until the integrator's output is reduced to zero, which makes comparator 2 change state. During the time interval t_2 to t_3, clock pulses are fed into part 2 of the counter. At t_3, the number of pulses added to the counter is

$$N_2 = f_c (t_3 - t_2) \tag{5}$$

and the integrators output is

$$V_o (t_3) = \frac{E_{in}}{RC} (t_1 - t_o) - \frac{E_{ref}}{RC} (t_2 - t_1) - \frac{E_{ref}}{2^7 RC} (t_3 - t_2) \tag{6}$$

But $V_o (t_3) = O$

$$\text{Therefore } E_{in} (t_1 - t_o) = E_{ref} (t_2 - t_1) + \frac{E_{ref}}{2^7} (t_3 - t_2) \tag{7}$$

Combining equations (2), (3), (5) and (7) gives

$$E_{in} = E_{ref} \frac{N_1 + N_2}{2^{14}} = E_{ref} \frac{N}{2^{14}} \tag{8}$$

where N is the count displayed at the end of time t_3.

Since 2^7 pulses have to be counted in each of the three integrations for a full scale signal, the maximum conversion time is $(3 \times 2^7)/f_c$ as opposed to $2^{15}/f_c$ for the dual ramp converter, i.e. this system is 85 times faster.

2.8 Voltage to Frequency A/D Conversion [2.7]

The simplified diagram of a voltage to frequency converter is shown in Figure 2.22 and related timing waveforms in Figure 2.23.

The output of the integrator is a negative going ramp, the slope of which is governed by the amplitude of E_{in}. The ramp continues until it exceeds $-E_{ref}$ at which point the comparator changes state. This change of state:

(I) Enables gate G2

(II) Triggers the pulse generator

(III) Starts the timer.

The timer enables gate G_1, therefore pulses from the clock can pass through gates G_1 and G_2 to the counter. The pulse generator supplies negative going pulses of closely controlled width and amplitude to the integrator's input. These pulses are used to discharge the capacitor and return the integrator input to zero. The system then repeats this procedure for a length of time determined by the timer. When the timer returns to the "zero" state gate G_1 is disabled, and clock pulses are prevented from reaching the counter. The number of counts displayed is therefore proportional to the amplitude of the analog input voltage.

Since this type of conversion is based on integration, and if the pulses are

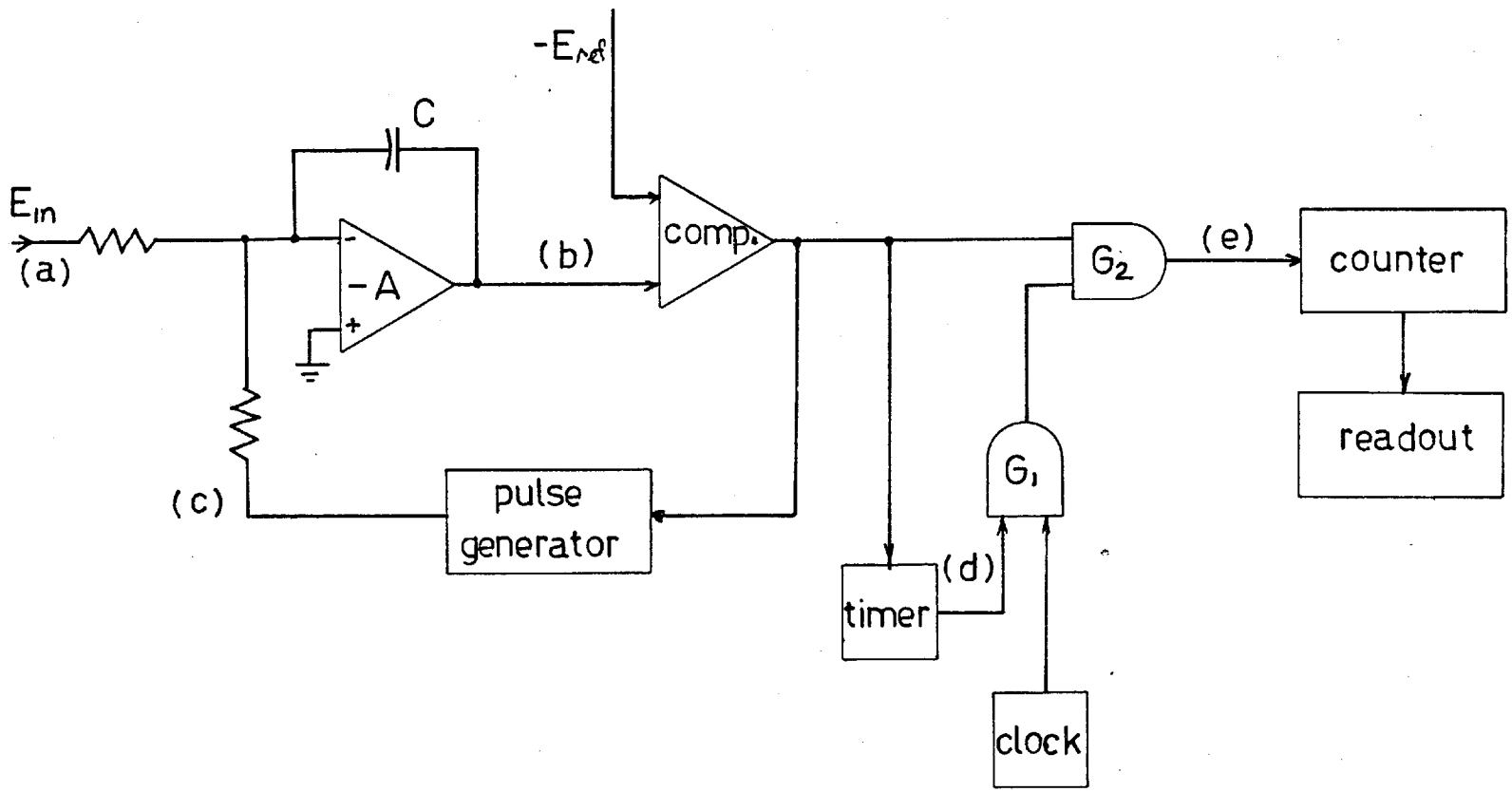


Fig. 2.22

Simplified Voltage to Frequency Converter

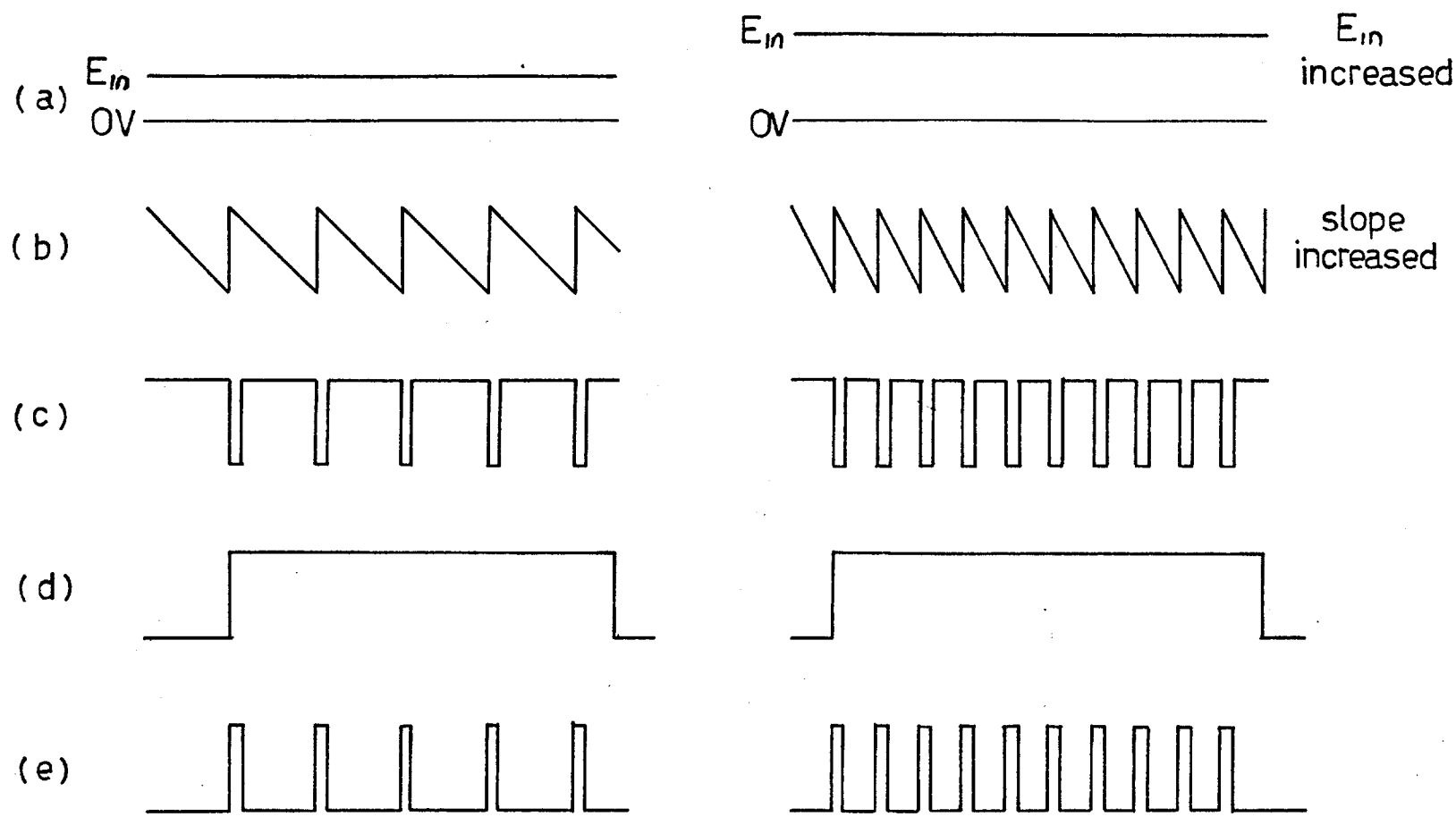


Fig. 2.23

Voltage to Frequency Converter Timing Waveforms

counted for a suitable length of time, this method has a very high noise rejection characteristic.

For a full scale reading, 2^n pulses must enter the counter, the speed of the converter is therefore determined by the time required to generate 2^n pulses.

The accuracy of the system is determined by:

(1) The accuracy and stability of the comparator C

(11) The frequency of the clock

(111) The zero offset voltages at the integrator input.

2.9 Cascade A/D Converter[1.11]

In the cascade converter, the input is first compared with a reference voltage equal to one half the full scale voltage. If the input is greater than the reference voltage, the M.S.B. is a one. The reference is then subtracted from the input and the result is doubled. If, instead, the input is less than the reference, the M.S.B. becomes a zero, and the input is then doubled. The N.M.S.B. is found by repeating the same process. To illustrate this process an example is considered. Assume a 6 bit cascade converter with a full scale analog input of 10 volts, and an analog input of 3.5 V. Operations will be performed as shown in Table 2.1

Table 2.1

Operation of a Cascade Converter

STAGE	INPUT TO STAGE	COMPARISON	RESULTING PROCESS	READOUT
1	3.5V	3.5V < 5V	(3.5-0)2= 7V	0
2	7V	7V > 5V	(7-5)2 = 4V	1
3	4V	4V < 5V	(4-0)2 = 8V	0
4	8V	8V > 5V	(8-5)2 =6V	1
5	6V	6V > 5V	(6-5)2 = 2V	1
6	2V	[illegible] < 5V	(2-0)2= 4V	0

TABLE 2.1

The digital output is 010110 which indicates the analog input lies in the 22nd quantizing level. This level extends from 3.43750 volts to 3.59375 volts; hence the signal has been quantized correctly.

One stage of a cascade A/D converter is shown in Figure 2.24. When a clock pulse is supplied, the D type flip flop will take up whichever state the comparator is in. The flip-flop output performs two functions:

(I) It is part of the digital readout

(II) It determines whether E_{ref} or O will be subtracted from E_{in}.

There must be as many identical stages as there are bits in the digital readout.

The conversion speed of this type of converter is equal the time taken to produce n clock pulses, where n is the required number of bits. Since n identical stages are used, the converter does become somewhat complex.

2.10 Single Stage Cascade Converter[1.12]

The Single Stage Cascade Converter is based on the cascade principle

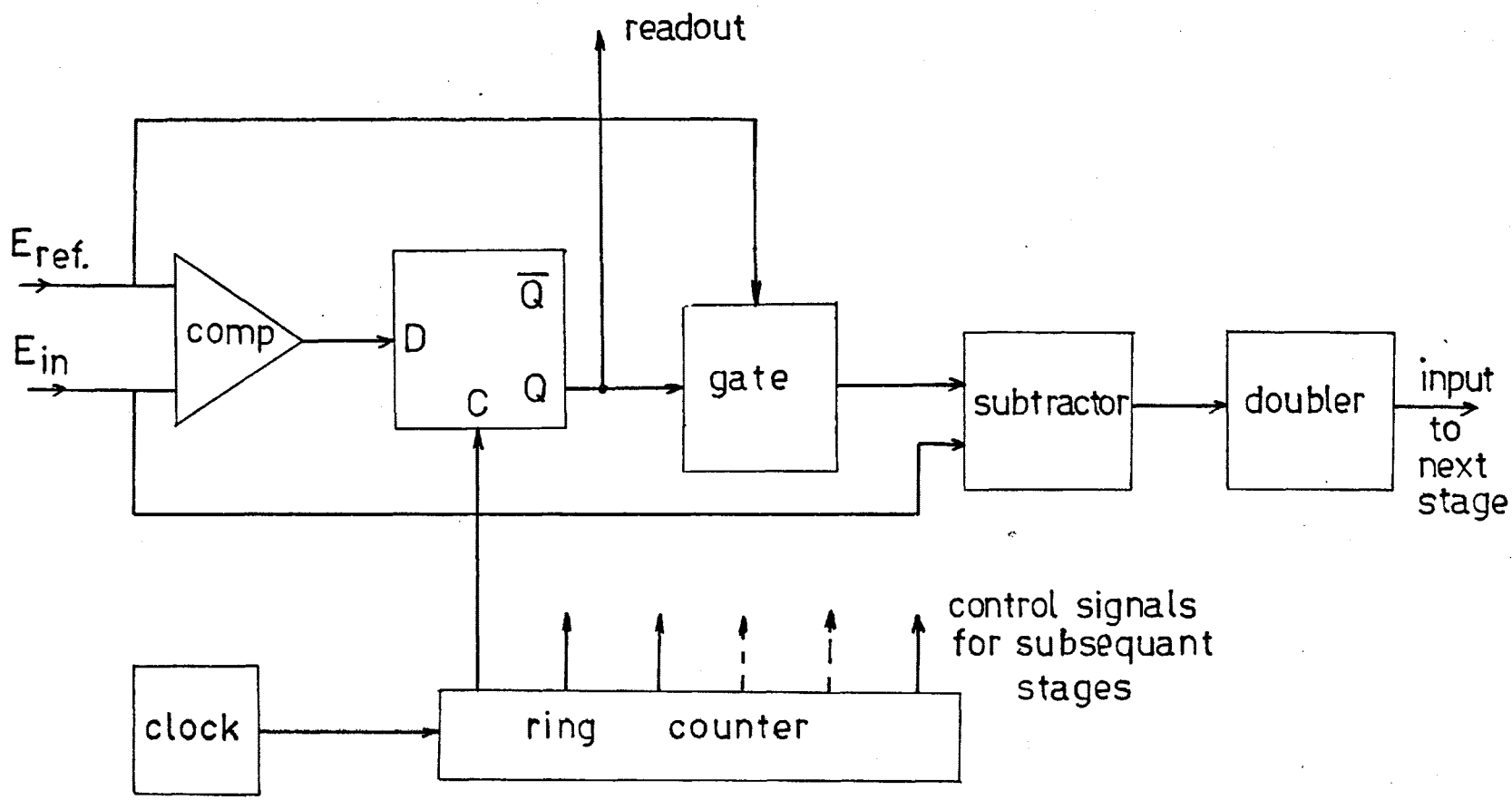


Fig. 2.24

One stage of a Cascade A/D Converter

but uses one stage only. The concept of this converter is mentioned by Richards[1] who also comments on the fact that it has not been exploited.

A block diagram of the converter is shown in Figure 2.25.

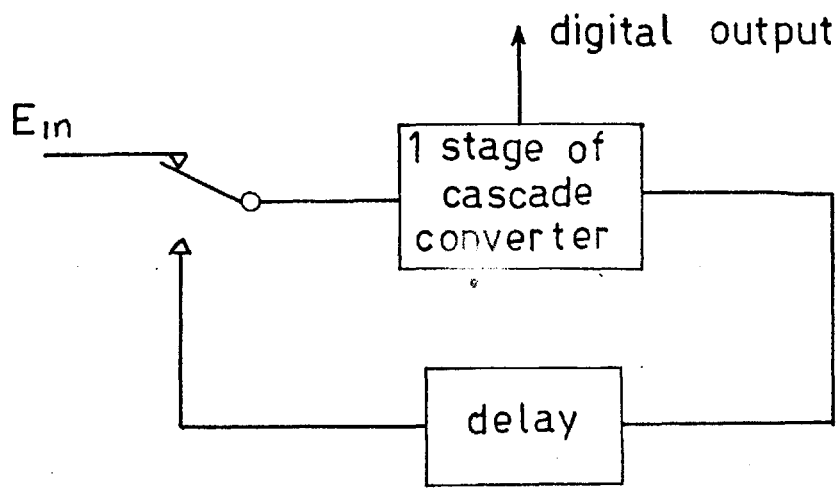


Fig. 2.25

SSC Converter

The switch is in the position shown while the M.S.B. is obtained and in its other position while the remaining bits are obtained. After the signal has been operated on by the single stage of the cascade converter the residue is fed back to the input via the delay block. The delay block provides a delay equal to the time between the development of successive bits. The residue is then operated on by the converter and the process is repeated until the required number of bits is obtained. The output bits are obtained serially from the single stage of cascade converter. The delay block can consist of either a delay line or a sample and hold circuit.

One converter based on this principle appears in the literature[12] and is shown in Figure 2.26. Figure 2.27 shows the waveforms around the system for an input of 7.7V, when the full scale analog input is 10 volts. The incoming sample is fed into the combining network and then to the delay line, the delay of which is equal to the time taken to develop successive bits. A tap on the delay line enables the sample to be compared to the reference voltage of 5 volts. If the sample is greater than this reference, the comparator programs the subtractor to subtract 5V. The result of this subtraction is then multiplied by 2 and fed back to the combining network. If the sample is less than 5V, the comparator programs the subtractor to pass it unaltered, and the cycle continues until a muting pulse is fed to the subtractor interrupting the feedback loop. Table 2.2 tabulates the passage of a 7.7 volt sample through the converter.

Table 2.2

Operation of an SSC Converter

COMPARISON	RESULTING PROCESS	RESIDUE FEDBACK TO THE INPUT	READOUT
$7.7 > 5$	(7.7-5)2=5.4	5.4 volts	1
$5.4 > 5$	(5.4-5)2=.8V	.8 volts	1
$.8 < 5$	(.8-0)2 =1.6V	1.6 volts	0
$1.6 < 5$	(1.6-0)2=3.2V	3.2 volts	0
$3.2 < 5$			0

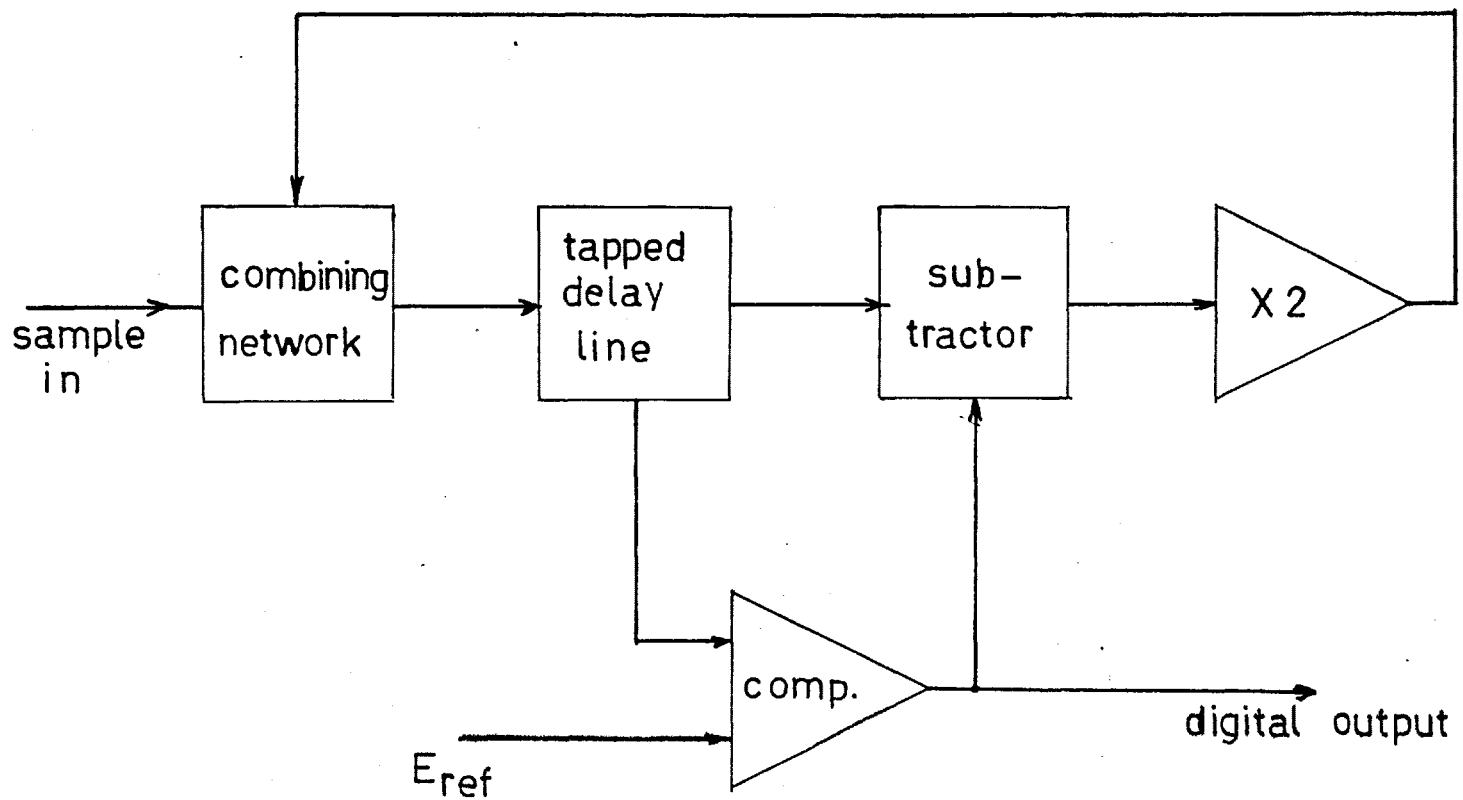


Figure 2.26
SSC Converter Using a Delay Line

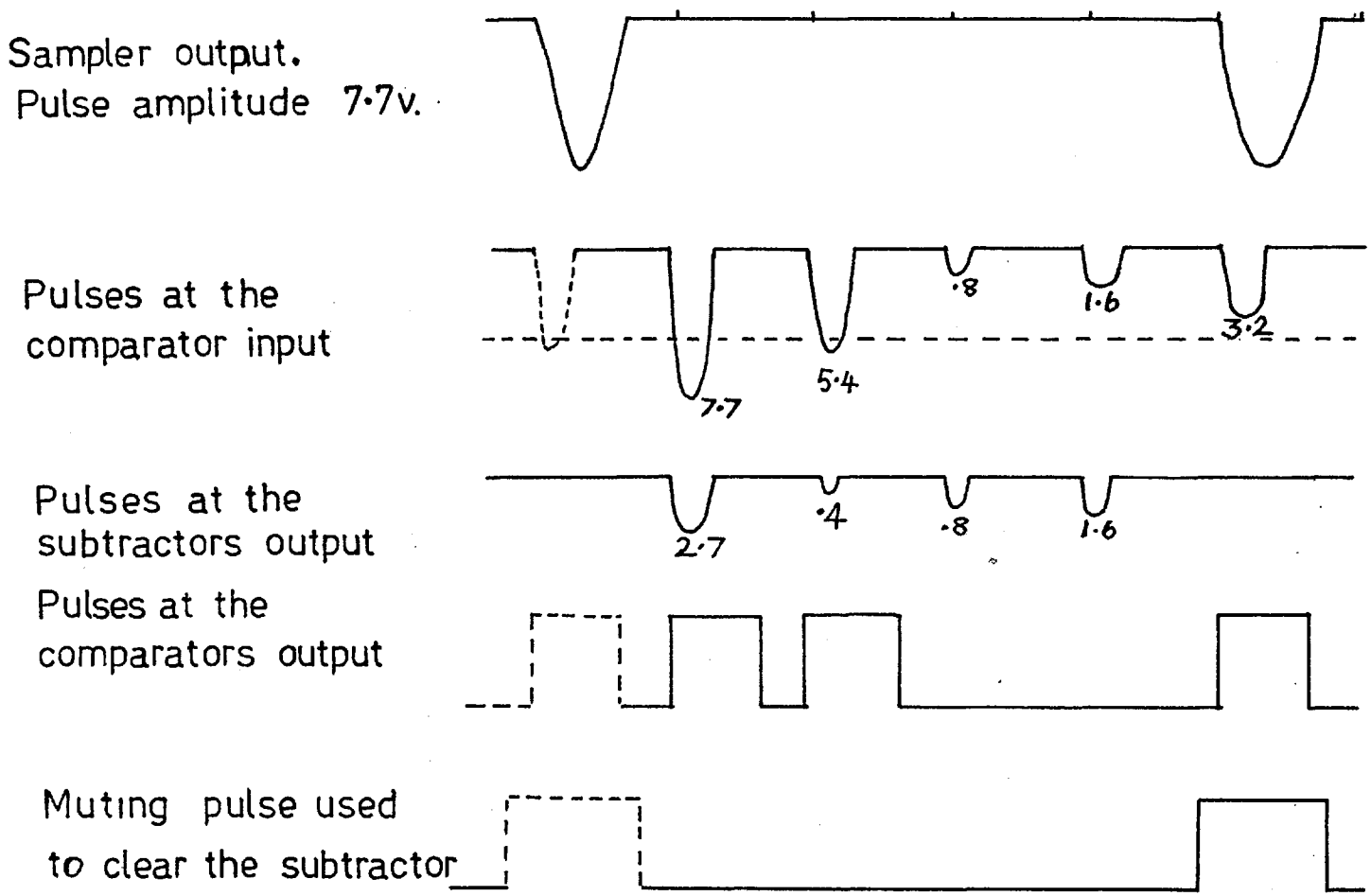


Fig. 2.27

Waveforms of an SSC Converter Using a Delay Line

Comparison of table 2.2 with table 2.1 helps illustrate the similarity between the operations of the cascade and single stage cascade converters. The conversion of a digital word of n bits in the single stage cascade converter is determined by the time taken to pass n clock pulses.

2.11 A Critical Comparison of the SSC Converter

Table 2.3 facilitates a critical comparison of the SSC converter with the other converter techniques reviewed in this chapter. It can be seen from the table that the SSC converter and the successive approximation converter have conversion times of the same order of magnitude. This means that the SSC converter would have to compete with the successive approximation converter. The SSC converter has the advantage of an inherent sample and hold operation and as a result a shorter aperture time. The SSC converter is expected to cost appreciably less since it requires fewer components, and its only precision components are two resistors.

Since the successive approximation converter is the most widely used general purpose converter, the future for the SSC converter is very promising indeed.

Table 2.3

Comparison of Converter Techniques

Converter Type	Suitable For Multiplexing	Max. Conversion Time No. of Clock Pulses For			Aperture Time		Relative Cost	Remarks
		n bits	5 bits μ sec.	8 bits μ sec.	5 bits μ sec.	8 bits μ sec.		
Successive approximation	Yes	n	7.5	27	7.5	27	medium	general purpose, at present it provides a good speed to dollar ratio.
Simultaneous	Yes	NA	NA	NA	NA	NA	depends on resolution	excellent for low resolution systems, operates in about 100 nsecs.
Counter	Yes	2^n-1	48	765	1.5	3.0	low	little additional cost for increased resolution, but conversion speed is low.
Continuous	No	1	1.5	2	1.5	2	low to medium	This is only true if input freq. [illegible] not exceed f_{max} as defined [illegible] section 2.4 equation (3).
Ramp	Yes	2^n	32	256	1	1	depends on resolution	low cost for low resolution used in economy digital voltmeters.
Dual Ramp	Yes	2^{n+1}	64	512	32	256	medium	used in digital voltmeters, good noise rejection properties.
Triple Ramp	Yes	$3 \times 2^{\frac{n}{2}}$	2	9.6	.8	3.2	high	not on the market yet.
Voltage to Frequency	Yes	2^n	320	2,560	320	2,560	high	used in quality digital voltmeters, good noise rejection properties.
Cascade	Yes	n	0.5	1	.1	.12	high	8 bit maximum at the present time Large system. Grey code.
SSC	Yes	n	9.6	16	3.2	3.2	low	high performance to cost ratio. Inherent sample and hold operation. Number of bits can be increased at little additional cost. high input impedance.

CHAPTER 3

SINGLE STAGE CASCADE A/D CONVERTER

In this Chapter, the principles and limits of a single stage cascade converter, devised by the author are discussed.

The SSC converter is based on the converter in Fedida's paper[12] which is outlined in Chapter 2 of this thesis. The main weakness of Fedida's converter is the inclusion of an analog delay line, and one of the major considerations in this design was to overcome the need for the delay line. The system shown in Figure 3.1 achieves this by alternately charging capacitors C_1 and C_2 through field effect transistor switches.

3.1 Operation of the SSC A/D Converter

The six bit SSC converter devised by the author is shown in Figure 3.1(a)&(b) E_{ref} is the full scale analog input voltage, and all switches are closed by a logical "one". When the start button is depressed, the eight stage ring counter is set to binary state 10000000 and the divide by 2 circuit is set; when the button is released the clock starts. The first clock pulse advances the "one" in the ring counter to the second stage, and this "one" is used as a synchronizing pulse; hence it is labelled S. The signal $\frac{C}{2}$ is also a "one", therefore switches 5 and 6 are closed, switches 1, 2, 3, and 4 are held open by the S signal, and switch 7 is held open by the $\frac{\overline{C}}{2}$ signal. The operational amplifier is therefore connected as

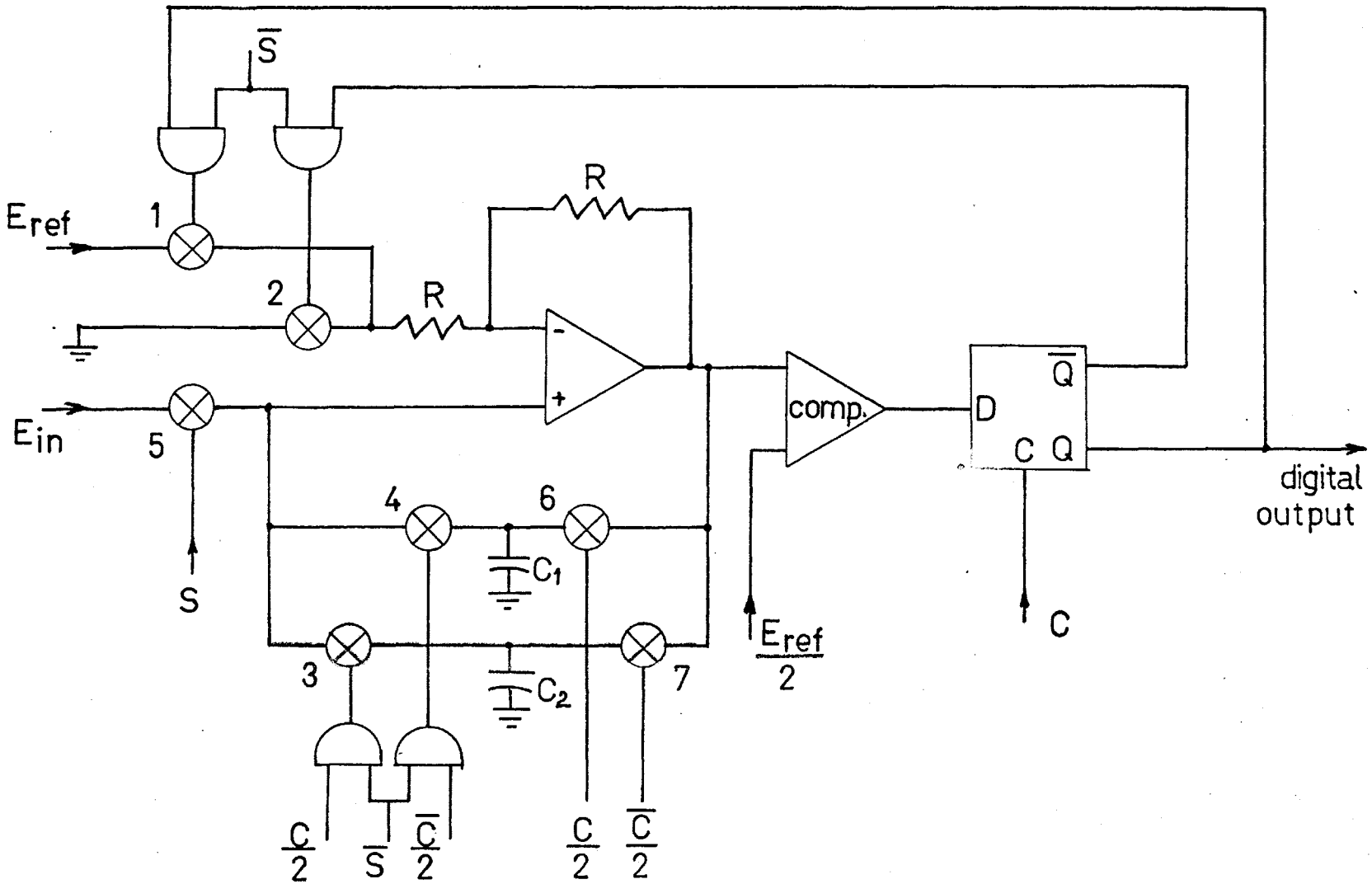


Figure 3.1(a)

Single stage cascade A/D converter

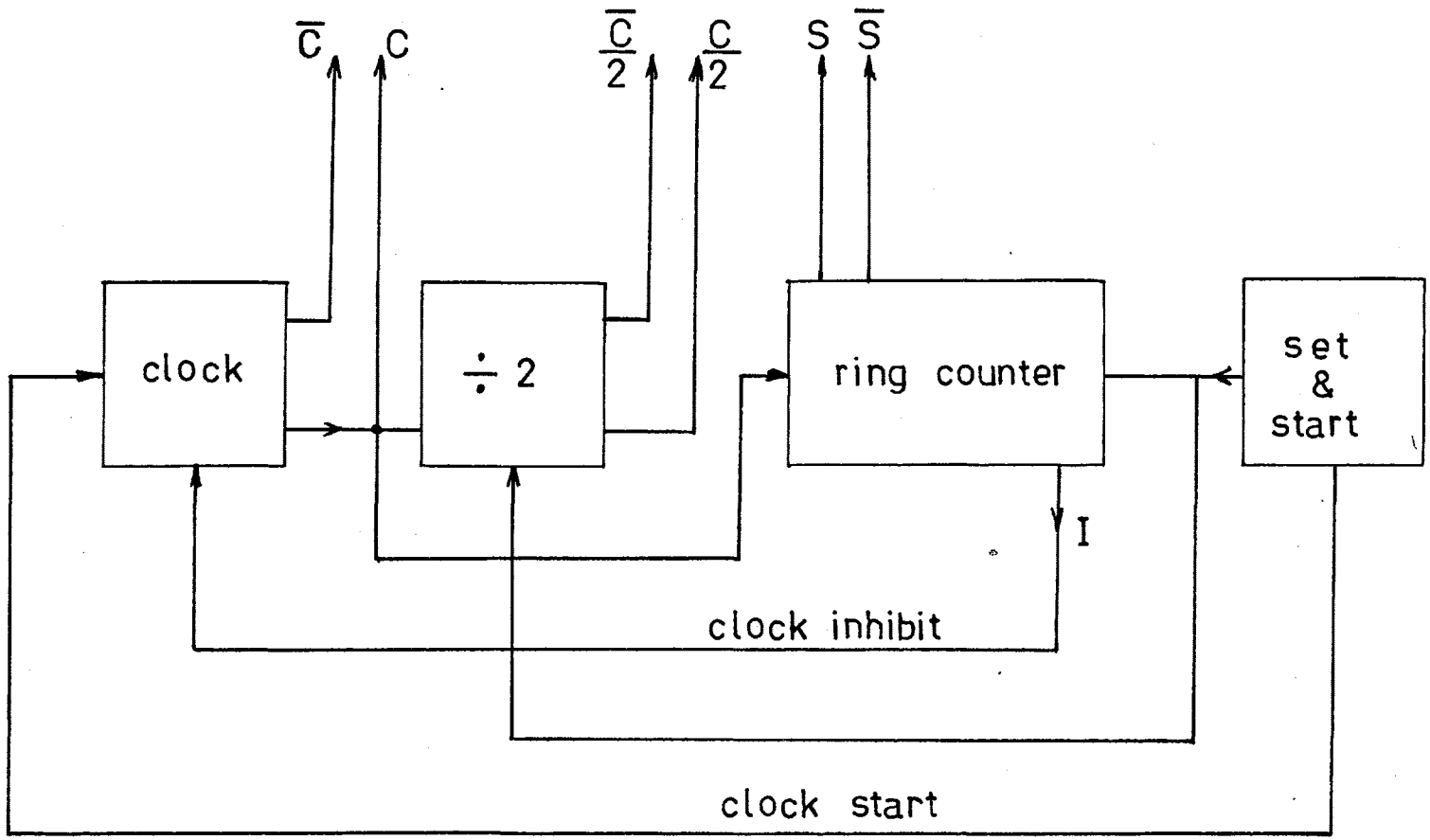


Figure 3.1 (b)

Timing Circuit for the SSC converter

shown in Figure 3.2. This is the configuration of a voltage follower with a gain of one, the analog input voltage therefore appears across capacitor C_1. The analog input is also applied to the comparator input, the output of which is fed to the D input of a D type flip flop. The state of the comparator will be entered into the flip flop when the flip flop receives the rising edge of the next clock pulse. If E_{in} is less than $\frac{E_{ref}}{2}$, the comparator is in the "zero" state and the next clock pulse switches the flip flop into the "zero" state, and a "one" is applied to gate 2. This clock pulse will also have advanced the ring counter so that $\bar{S}$ is now a "one", S a "zero", and $\frac{C}{2}$ a "zero". This means that gates 5 and 6 are opened, and gates 2,4 and 7 are closed. The operational amplifier is now connected as shown in Figure 3.3 and performs the operation

$$E_o = 2 E_{in}$$

If however, the analog input had been greater than $\frac{E_{ref}}{2}$, the comparator would have been in the "one" state and the rising edge of the next clock pulse would have switched the flip flop to the "one" state. Switches 5 and 6 would again open and this time switches 1,4 and 7 would close. The operational amplifier is then connected as shown in Figure 3.4 and performs the operation

$$E_o = 2 E_{in} - E_{ref}$$

When the next clock pulse occurs, switches 4 and 7 open and 3 and 6 close. Switches 1 or 2 will be closed depending on the state of the D type flip flop. This sequence of operations repeats itself at every clock pulse until the last stage in the ring counter switches to the "one" state, this pulse being used to inhibit the clock. The digital output appears in serial form at the output of

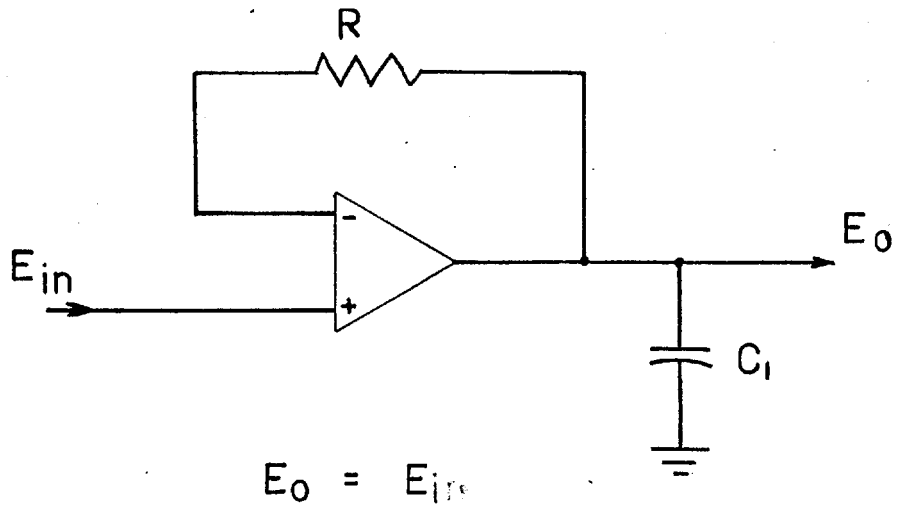
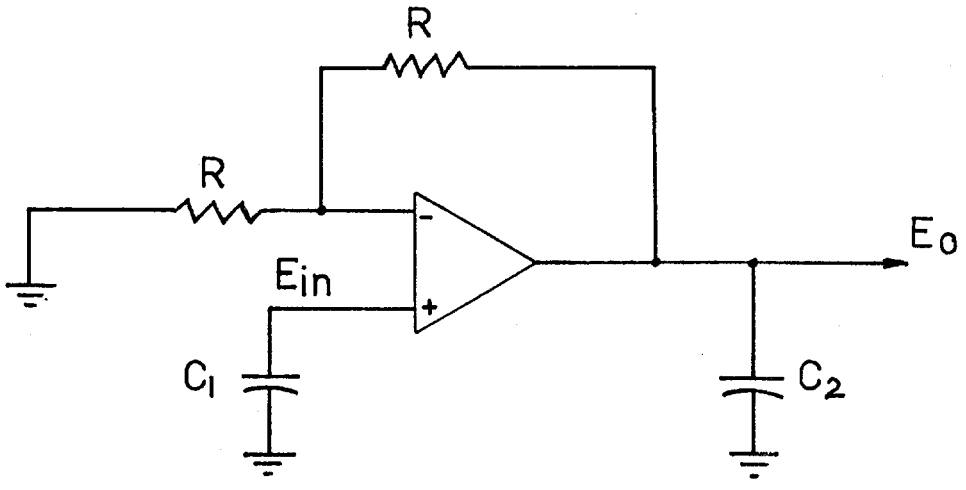


Figure 3. 2

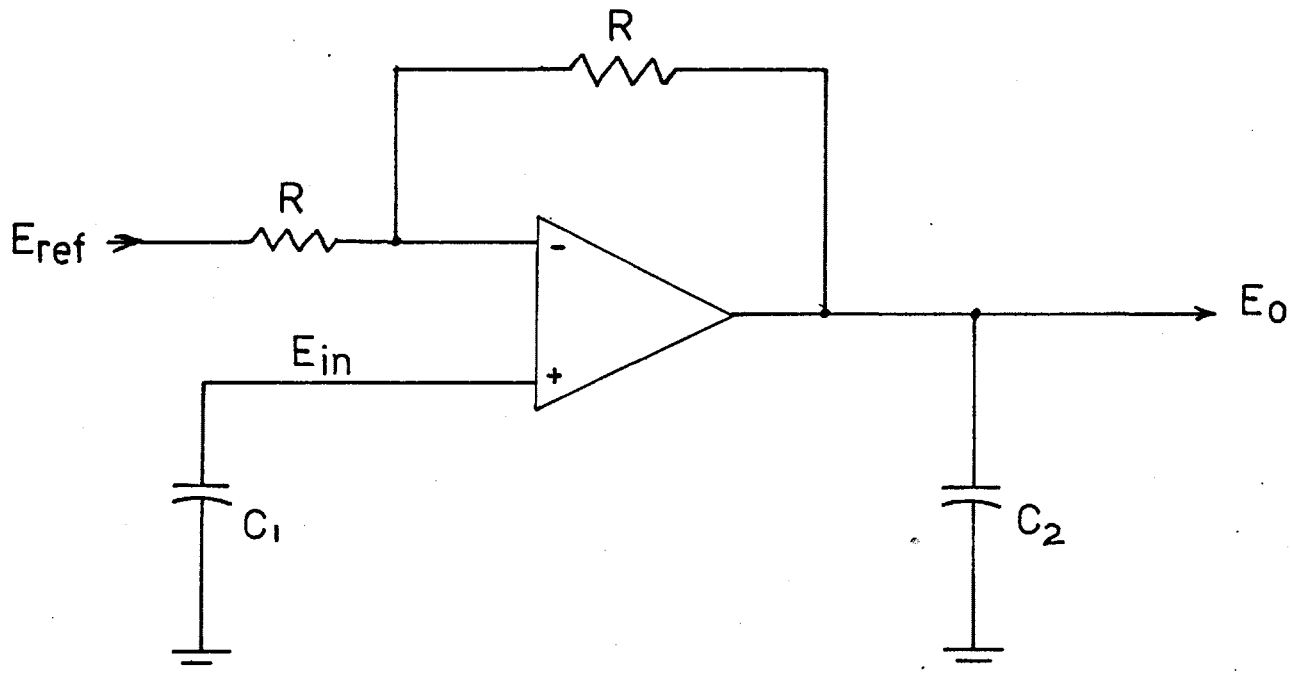
Operational amplifier as a voltage Follower



$$E_o = E_{in}\left(1 + \frac{R}{R}\right) = 2E_{in}$$

Figure 3. 3

Operational amplifier as a non-inverting amplifier



$$E_o = E_{in}\left(1 + \frac{R}{R}\right) - E_{ref}\frac{R}{R}$$

$$= 2E_{in} - E_{ref}$$

Figure 3.4

Operational amplifier performing multiplication
by 2 and a subtraction

the D type flip flop.

To aid in understanding the converters operation, an example is now considered,. assuming:-

(l) An analog input E_{in} of 7.7 volts

(ll) That a six bit output is required

(lll) That E_{ref} = 10 volts.

When the start button has been depressed and released the ring counter is set to binary state 10000000 and switches 5 and 6 are closed; all other switches being open. Switching waveforms are shown in Figure 3.5. Capacitor C_1 is charged to 7.7 volts. Since 7.7 v is greater than 5 volts, the comparator switches to the "one" state and the next clock pulse opens switches 5 and 6 and closes switches 1, 4 and 7. Capacitor C_2 then charges to 2 x 7.7 - 10 volts = 5.4 volts. Since 5.4 volts is still greater than 5 volts, the next clock pulse opens switches 4 and 7 and closed 3 and 6. C_1 then discharges through the low output impedance of the operational amplifier to 2 x 5.4 - 10 = 0.8 volts. Since this is less than 5 volts, the comparator switches to the "zero" state and the next clock pulse opens switches 1, 3 and 6 and closes switches 2, 4 and 7. Capacitor C_1 then discharges to 2 x 0.8 = 1.6 volts. Similar action continues. C_2 is charged to 3.2 volts and then C_1 is charged to 6.4 volts, the next clock pulse causing the ring counter to inhibit the clock. As can be seen from Figure 3.5 the serial output at the $\bar{Q}$ output of the D type flip flop would be 110001, which corresponds to the 49th quantized level.

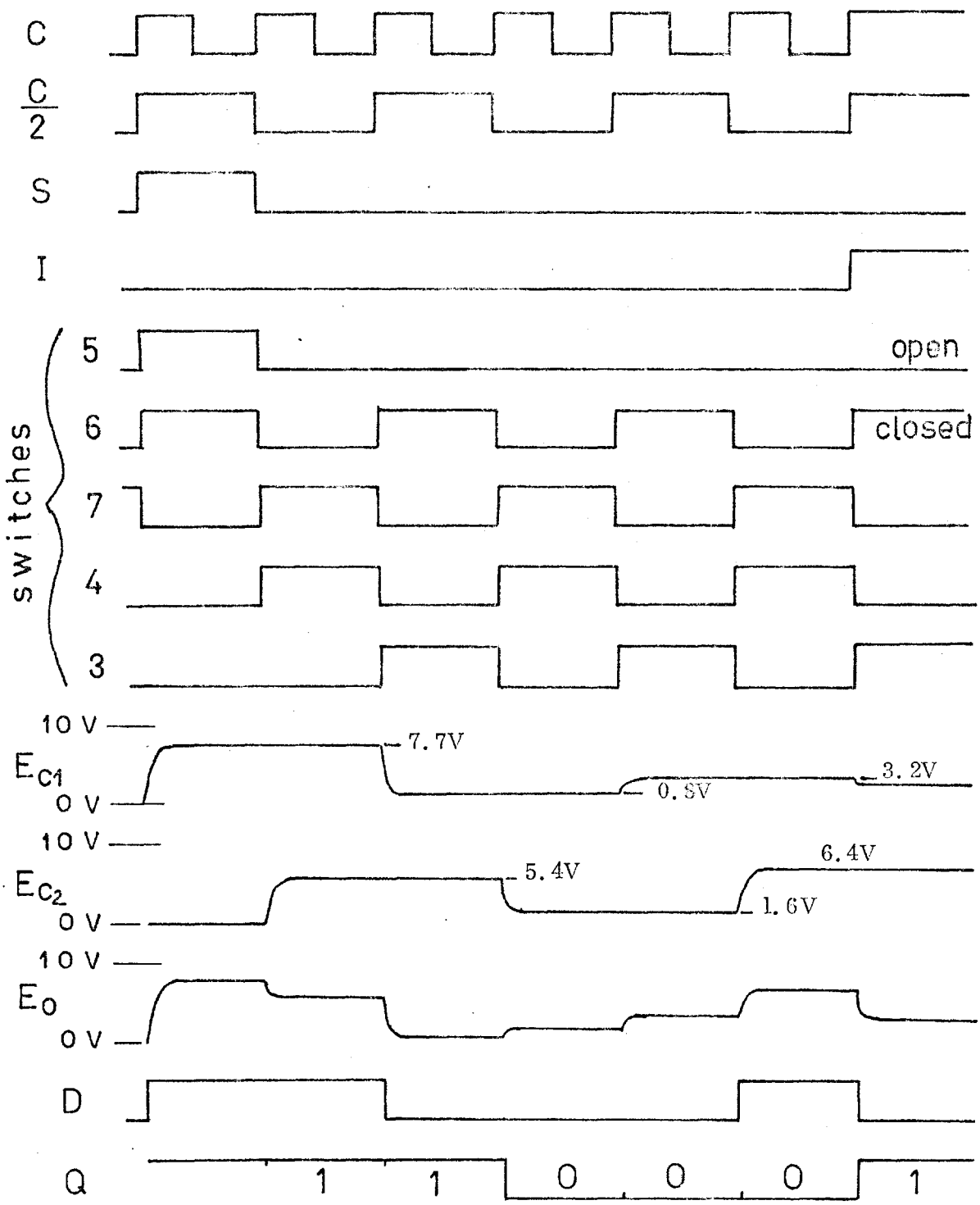


Figure 3.5

Waveforms of the S.S.C. converter with 7.7 volts analog input

3.2 Conversion Rate

The number of clock pulses required to complete one conversion is equal to the required number of bits. To find the maximum conversion rate it is therefore necessary to determine the clock frequency, this being determined by the time taken to charge capacitors C_1 and C_2 of figure 3.1, to within some specified percentage of their ultimate voltage.

The rise time of the voltage across C_1 or C_2 is complex since it is a function of the RC time constant, the slewing rate of the operational amplifier, and the output current capability of this amplifier. This is further complicated by the fact that the resistive component of the RC time constant is a function of the current flowing. This current dependency occurs because the resistive component is the "on" resistance of a field effect transistor, and once the source to drain current increases beyond the "ohmic" (non-saturated) region of the device, the "on" resistance will increase considerably.

The resistive component should also include the output resistance of the operational amplifier, but the closed loop output resistance is exceedingly small as shown below and is negligible.

Load the circuit of figure 3.6 with an incremental current ΔI_L. Since $R_o + R_1 \gg Z_{out}$ the resulting change in current through Z_{out} is therefore ΔI_L and the change in voltage across Z_{out} is

$$\Delta E_o - \Delta e_o = \Delta I_L \; Z_{out} \qquad (1)$$

By definition $e_o = A(e_2 - e_1)$ (2)

but $\Delta e_2 = 0$ because the input impedance at the non-inverting input is infinite

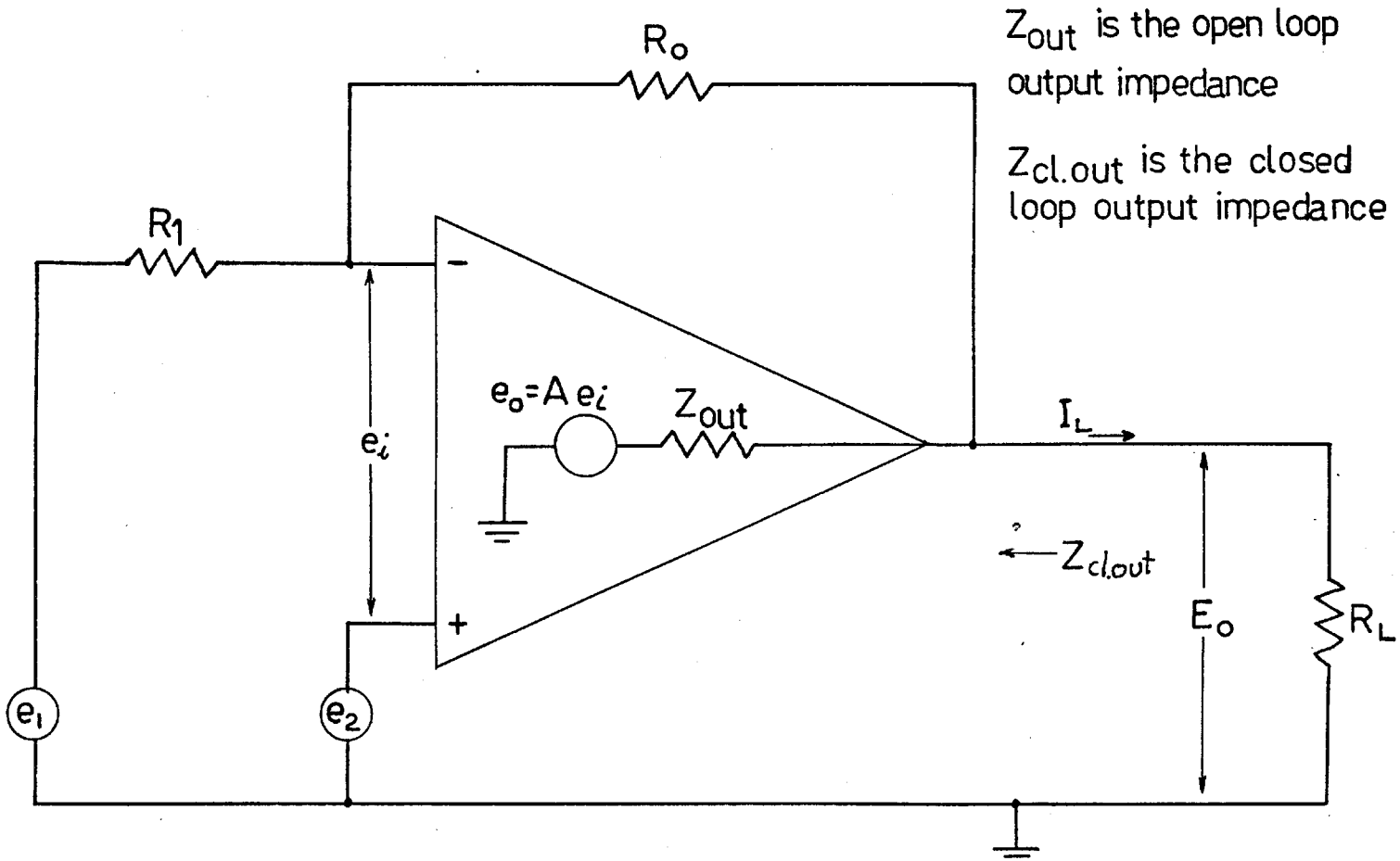


Fig. 3.6

Circuit Showing the Output Impedance of an Operational Amplifier

Therefore from equation (2) (3)

$$\Delta e_o = -A\Delta e_1$$

The change in output voltage E_o is returned to the input by the potential divider consisting of R_o and R_1.

$$\text{Therefore } \Delta e_1 = \Delta E_o \frac{R_1}{R_1 + R_o} \tag{4}$$

Combining equations (1) and (3) yields

$$\Delta E_o + A \Delta e_1 = \Delta I_L \ Z_{out} \tag{5}$$

Substituting equation (4) and (5)

$$\Delta E_o \left(1 + \frac{AR_1}{R_1 + R_o}\right) = \Delta I_L \ Z_{out} \tag{6}$$

but the closed circuit output impedance

$$Z_{cl\ out} = \frac{\Delta E_o}{\Delta I_L}$$

$$\text{Therefore from equation (6) } Z_{cl\ out} = \frac{Z_{out}}{1 + \frac{AR_1}{R_1 + R_o}} \tag{7}$$

In the circulating converter $R_1 = R_o$

$$\text{Therefore } Z_{cl\ out} = \frac{Z_{out}}{1 + \frac{A}{2}} \tag{8}$$

A typical operational amplifier has $Z_{out} = 75$ ohms and $A = 2 \times 10^5$

Therefore from equation (8)

$$Z_{cl\ out} = \frac{75}{10^5} = .75 \times 10^{-3} \text{ ohms}$$

This value will be negligible compared to the "on" resistance of a FET.

It was indicated at the beginning of this section that the longer the capacitor was allowed to charge up, the more accurate is the system; however the fact

that when C_1 is being charged, C_2 is connected to the input of the amplifier and hence is losing charge, must also be considered. It is therefore necessary to calculate the closed circuit input impedance of the operational amplifier, and this is achieved as follows[13]; with the aid of figure 3.7.

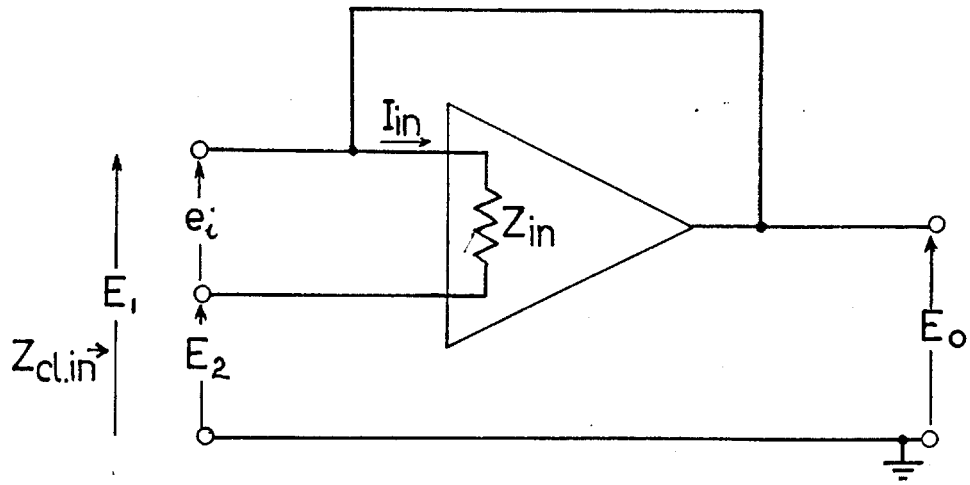


Fig. 3.7

Voltage Follower

When the output voltage changes by ΔE_o the differential input voltage e_i is changed by

$$\Delta e_i = \frac{-\Delta E_o}{A} \approx \frac{-\Delta E_2}{A} \tag{9}$$

The change of differential input voltage Δe_i results in a change in input current

$$\Delta I_{in} = \frac{\Delta e_i}{Z_{in}} \approx \frac{-\Delta E_2}{A Z_{in}} \tag{10}$$

The closed loop input impedance

$$Z_{cl\ in} = \frac{-\Delta E_2}{\Delta I_{in}} \tag{11}$$

Substitute equation (10) into (11)

$$Z_{cl\ in} = AZ_{in}$$

that is, the closed loop input impedance is equal to the open loop input resistance multiplied by the open loop gain.

Taking typical values $Z_{in} = 0.3$Mohm and $A = 2 \times 10^5$, this results in

$$Z_{cl\ in} = .3 \times 10^{11} \times 2 = 60 \times 10^3 \text{ M ohms.}$$

Assuming C_1 is 5,000 pF this gives a discharge time constant of $5,000 \times 10^{-12} \times 60 \times 10^9 = 300$ secs. Thus if clock frequencies in the kilohertz region are used, there is no appreciable loss of charge.

3.2.1 Theoretical Derivation of Capacitor's Charging Waveform

If the system is designed such that neither the operational amplifier or the F E T enter their current saturation regions, an expression for the voltage waveform across capacitors C_1 and C_2 can be derived as follows:-

The RC circuit shown in figure 3.8a has an input voltage as shown in figure 3.8b. The output voltage, that is the voltage across the capacitor is given by:

$$V = iR + \frac{1}{C}\int idt \qquad (1)$$

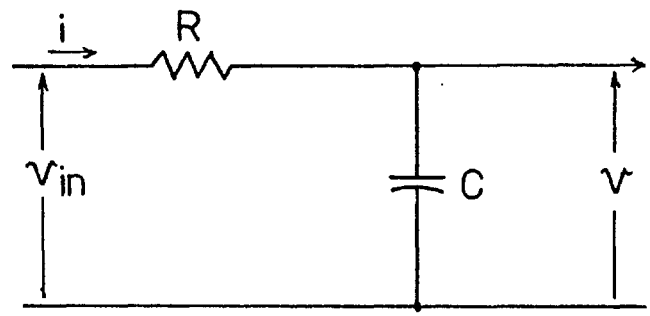
Multiply by C

$$Cv = i\,CR + \int idt$$

Differentiate with respect to t

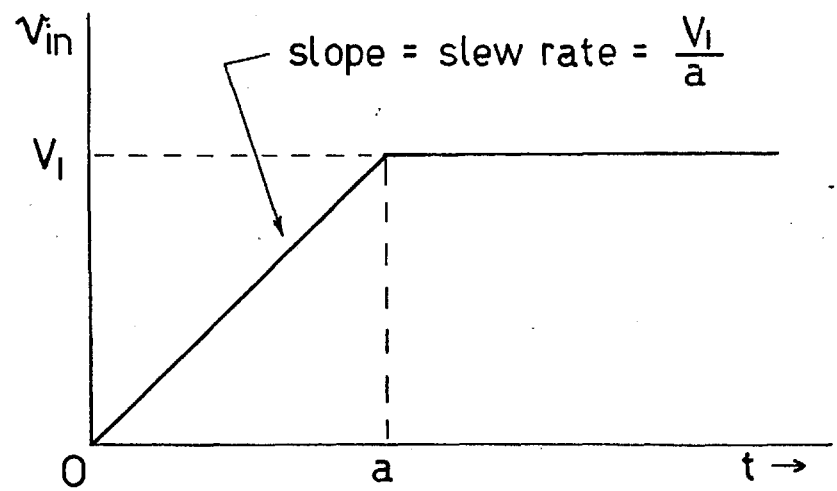
$$C\frac{dv}{dt} = CR\frac{di}{dt} + i \qquad (2)$$

The Laplace transform of this equation can be obtained using the expression



(a)

Operational Amplifier's Loading Circuit



(b)

Input Waveform

Fig. 3.8

Circuit Used to Determine Capacitor's Charging Waveform

$$\mathcal{L}\left[\frac{df(t)}{dt}\right] = sF(s) - f(0)$$

therefore equation (2) becomes

$$Cs\,V(s) = CRs\,I(s) + I(s) \tag{3}$$

since v and i are zero at t = 0

Rearranging equation (3)

$$I(s) = \frac{s\,C}{1 + CRs}\,V(s) \tag{4}$$

The Laplace transform of the waveform shown in figure 3.8b is

$$V(s) = \frac{V_1}{a}\,\frac{1}{s^2}\,(1 - e^{-as}) \tag{5}$$

Substituting equation (5) into (4) gives

$$I(s) = \frac{V_1}{as}\,\frac{C}{1+CRs}\,(1 - e^{-as})$$

$$= \frac{V_1\,C}{asCR}\,\frac{(1 - e^{-as})}{(\frac{1}{CR} + s)} \tag{6}$$

let $\frac{1}{CR} = b$

then

$$I(s) = \frac{V_1}{Ra}\,\frac{1 - e^{-as}}{s(s+b)} \tag{7}$$

$$= \frac{V_1}{Ra}\left(\frac{1}{s(s+b)} - \frac{s^{-as}}{s(s+b)}\right) \tag{8}$$

The inverse Laplace transform of the two terms in the brackets must now be obtained. The first term is a standard form, and the second can be transformed using the operation

$$e^{-as}\,f(s) = U(t - a)\;F(t - a)$$

where U (t-a) is a unit step function at t = a

The inverse transform of equation (8) is

$$i(t) = \frac{V_1}{Ra}\left[\frac{1}{b}(1-e^{-bt}) - \frac{U(t-a)}{b}\left(1-e^{-b(t-a)}\right)\right]$$

$$= \frac{V_1}{Rab}(1-e^{-bt}) - \frac{V_1}{Rab}(1-e^{-b(t-a)})\,U(t-a) \qquad (9)$$

Substitute $b = \frac{1}{CR}$

$$i(t) = \frac{V_1 C}{a}(1-e^{-\frac{t}{CR}}) - \frac{V_1 C}{a}(1-e^{-\frac{(t-a)}{CR}})\,U(t-a) \qquad (10)$$

By inspection of equation (10) it can be seen that $i(t)_{maximum}$ will occur at t=a

Therefore $$i(t)_{max} = \frac{V_1 C}{a}(1-e^{-\frac{a}{CR}}) \qquad (11)$$

The output voltage can be obtained by integrating equation (9) and dividing by C, giving

$$V(t) = \frac{1}{C}\int_o^t idt = \frac{V_1}{CRab}\int_o^t (1-e^{-bt})dt - \frac{V_1}{CRab}\int_a^t (1-e^{-b(t-a)})dt \qquad (12)$$

$$= \frac{V_1}{CRab}\left[t - \frac{1}{b} + \frac{e^{-bt}}{b}\right]_{t\geqslant o} - \frac{V_1}{CRab}\left[t-a-\frac{1}{b} + \frac{e^{-b(t-a)}}{b}\right]_{t\geqslant a}$$

but $b = \frac{1}{CR}$

Therefore $$v(t) = \frac{V_1}{a}\left(t - CR + CRe^{-\frac{t}{CR}}\right)_{t\geqslant o} - \frac{V_1}{a}\left(t-a-CR+CRe^{-\frac{t-a}{CR}}\right)_{t\geqslant a} \qquad (13)$$

at $t = a$

$$v(a) = \frac{V_1}{a}\left(a - CR + CRe^{-\frac{a}{CR}}\right) \qquad (14)$$

Equation (13) describes the output voltage if the operational amplifier is capable of passing the current given by equation (11), when its output voltage is that given

by equation (14) and if the F E T is capa ble of passing this maximum current without leaving its linear "resistive" region.

The equations derived in this section will be utilized in chapter five of this thesis.

3.3 Aperture Time

The term aperture time was defined in section 2.1.3, and it was shown that the related uncertainty voltage was directly proportional to the aperture time. This often leads to the use of sample and hold circuits of the type discussed in section 2.1.4. The SSC converter has an aperture time of only one clock pulse and hence a sample and hold feature is inherent in its operation

3.4 Inverting Amplifier

An ideal operational amplifier is characterized by:

(a) Infinite voltage gain

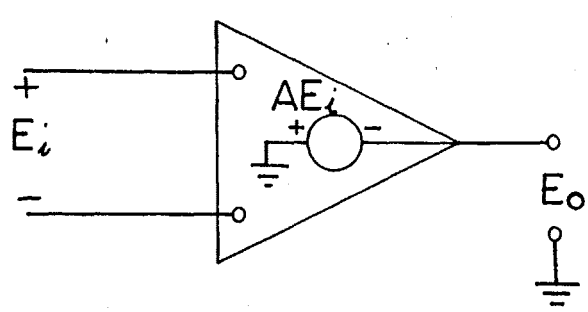
(b) Infinite input resistance

(c) Zero output resistance

(d) Infinite bandwidth

(e) Zero offset

and its equivalent circuit is shown in figure 3.9a. The characteristics of a real operational amplifier differ from these in that the voltage gain, input resistance, output resistance, bandwidth and offset are all finite. An equivalent circuit of a



$Z_{in} = \infty$

$Z_{out} = 0$

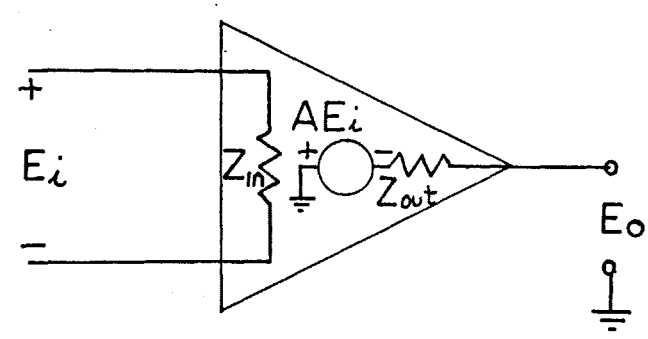
$A = \infty$

$E_o = -AE_i$

$E_o = 0$ when $E_i = 0$

(a)

Ideal Operational Amplifier



A, Z_{in}, and Z_{out} are finite

(b)

Real Operational Amplifier

Fig. 3.9

Operational Amplifier Equivalent Circuits

real operational amplifier is shown in figure 3.9.b

Consider the amplifier shown in figure 3.10

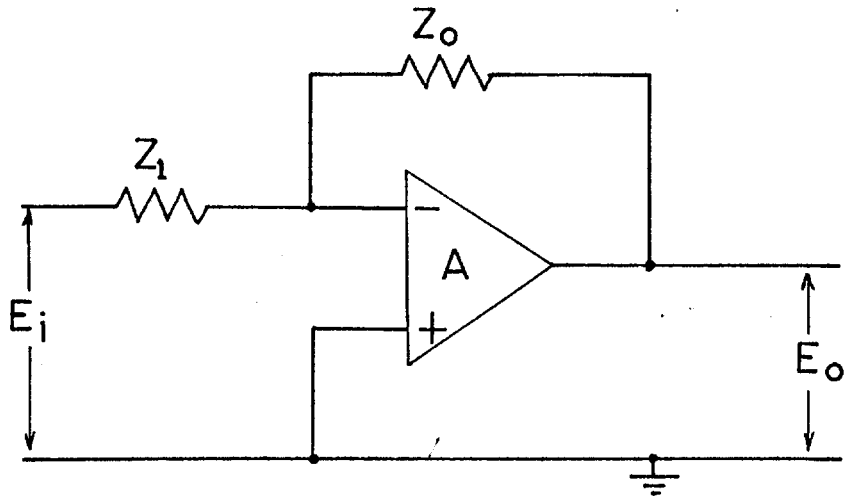


Fig. 3.10

Inverting Amplifier

Using a real operat ional amplifier, the gain is given by[13]

$$\frac{E_o}{E_i} = -\frac{Z_o}{Z_i}\left(\frac{1}{1+U}\right) \tag{1}$$

where $$U = \frac{\left(1 + \frac{Z_{out}}{Z_o} + \frac{Z_{out}}{Z_{load}}\right)\left(1 + \frac{Z_o}{Z_1} + \frac{Z_o}{Z_{in}}\right)}{\left(A - \frac{Zout}{Z_o}\right)} \tag{2}$$

where Z_{out} is the amplifier's open circuit output impedance.

This may be expanded as

$$\frac{E_o}{E_i} = -\frac{Z_o}{Z_1}\left(1 - U + U^2 - U^3 + - -\right)$$

if $U \ll 1$ this simplifies to

$$\frac{E_o}{E_i} \doteq \frac{-Z_o}{Z_i} (1 - U) \qquad (3)$$

Typical open loop parameters are,

$A = 200,000$ $\qquad Z_i = 10\text{Kohms}$

$Z_{in} = .3\text{Mohm}$ $\qquad Z_o = 10\text{Kohms}$

$Z_{out} = 75$

To evaluate equation 3 the term U must be evaluated. From equation 2 U is seen to be a function of Z_{load}, but Z_{load} increases as the load capacitance charges up. The time at which the gain is required occurs when the capacitor is charged to approximately 99.9%, at which time Z_{load} will be very large and

$$\frac{Z_{out}}{Z_{load}} \ll 1$$

therefore this term of equation 3 is negligible.

Solving for equation (2)

$$U = 1.5 \times 10^{-5}$$

which justifies the assumption used to obtain equation (3)

and from equation (3)

$$\frac{E_o}{E_i} = \frac{-Z_o}{Z_i} (1 - 1.5 \times 10^{-5})$$

$$= -.999985$$

This means the gain of this circuit is within 0.0015% of the idealized value, and as a result the accuracy of the gain is entirely dependent on the accuracy and

stability of impedances Z_1 and Z_o.

The finite input offset voltage also introduces an error, but this can be balanced out to a fraction of a millivolt using an external nulling potentiometer. Drift of this offset voltage also introduces an error; this can be minimized by introducing a resistor R_2, as shown in Figure 3.11.

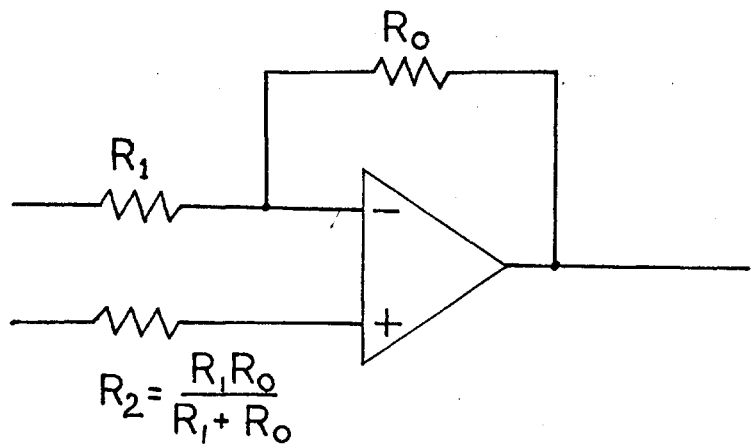


Fig. 3.11

Introduction of a Resistor to Minimize Drift

3.5 The Voltage Follower

A simple voltage follower is shown in Figure 3.12 and is analysed as follows[13].

By Kirchoff's Mesh Law

$$E_2 + e_1 = E_o \qquad (1)$$

but $$E_o = -Ae_1$$

where A is the open loop gain of the operational amplifier

$$\text{then } e_i = -\frac{E_o}{A} \qquad (2)$$

Substitute equation (2) into equation (1)

$$E_2 - \frac{E_o}{A} = E_o$$

As A tends to infinity $\frac{E_o}{A}$ approaches zero

$$\text{and } E_o = E_2 \tag{3}$$

In the SSC converter a feedback resistor is present and the voltage follower has the configuration shown in figure 3.13. Ideally there is zero current through R_o, but in reality the operational amplifier's bias current, I_b, flows through it. Kirchoff's Mesh Law now gives

$$E_2 + e_1 - I_b R_o = E_o$$

$$\text{and } e_1 = \frac{-E_o}{A}$$

therefore $E_2 - \frac{E_o}{A} - I_b R_o = E_o$

Since $\frac{E_o}{A}$ approaches zero as A approaches infinity

$$E_o = E_2 - I_b R_o$$

A typical operational amplifier with bipolar junction transistors as the input devices has a bias current of 80 nanoamps, and if R_o = 10K ohms this results in a .8mV error. The bias current is reduced to typically 1 nanoamp in operational amplifiers with F E T input devices, resulting in an error of .01 millivolts. For a high accuracy system it is therefore necessary to use an operational amplifier with FET input devices.

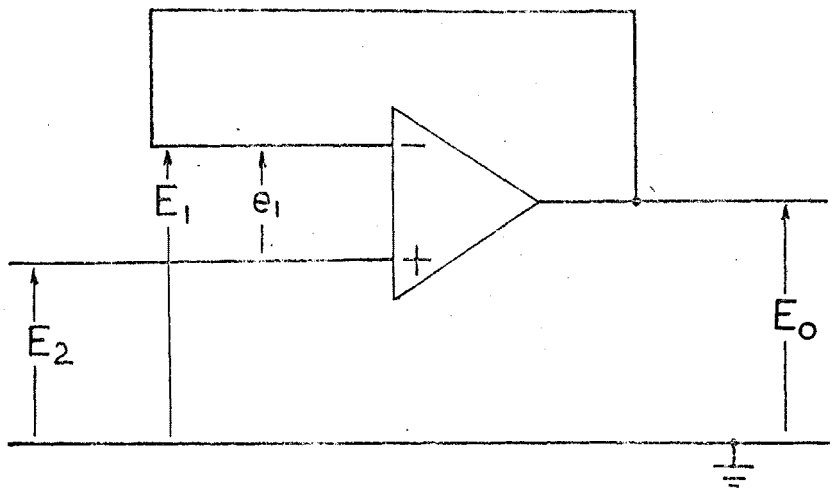


Fig. 3.12

Voltage Follower

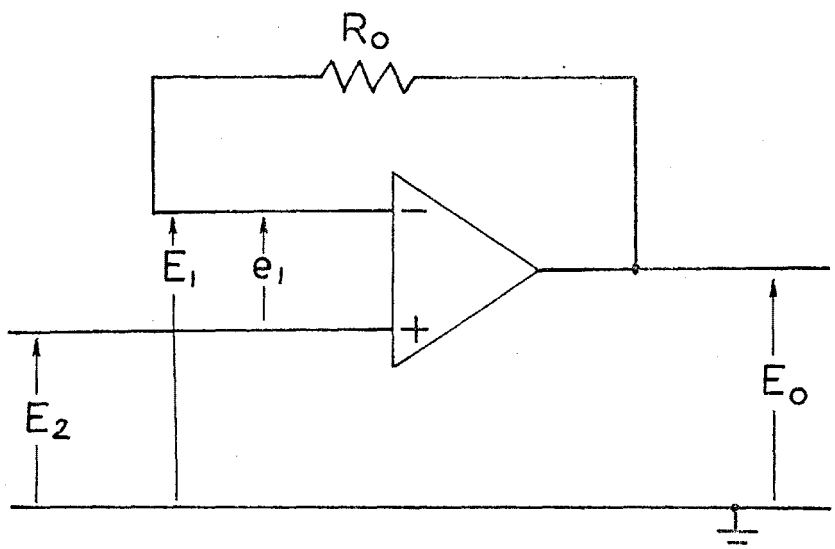


Fig. 3.13

Voltage Follower with a Feedback Resistor

CHAPTER 4

REALIZATION OF AN SSC CONVERTER USING DISCRETE COMPONENTS

To verify the concept of an SSC A/D converter as described in chapter 3 it was decided to build a six bit converter using Digital Equipment Corporation R series modules; because the modules were available and the system could be built rapidly. If verification of the system was obtained, the converter was to be rebuilt in a more compact and up to date form, using integrated circuits and FET's.

4.1 Timing Circuits

A block diagram of the timing circuit is shown in Figure 4.1, and its timing diagram is shown in Figure 4.2. The clock is an R401 gateable clock that produces 100 nsecond pulses from -3V to ground. Flip flops FF1 and FF2 are R201 modules, these modules are connected as divide by two circuits. The ring counter consists of five type R202 dual flip flops. Eight of the flip flops are connected to form an eight stage ring counter. The eighth stage is required to produce the clock inhibit pulse, I, so the clock can be inhibited and a display of the digital readout can be obtained. A block diagram of a ring counter using R202 flip flops is shown in Figure 4.3. The reset and start block is a manually operated pulser. The pulser output is normally a "one" that is -3Volts. When a conversion is required the

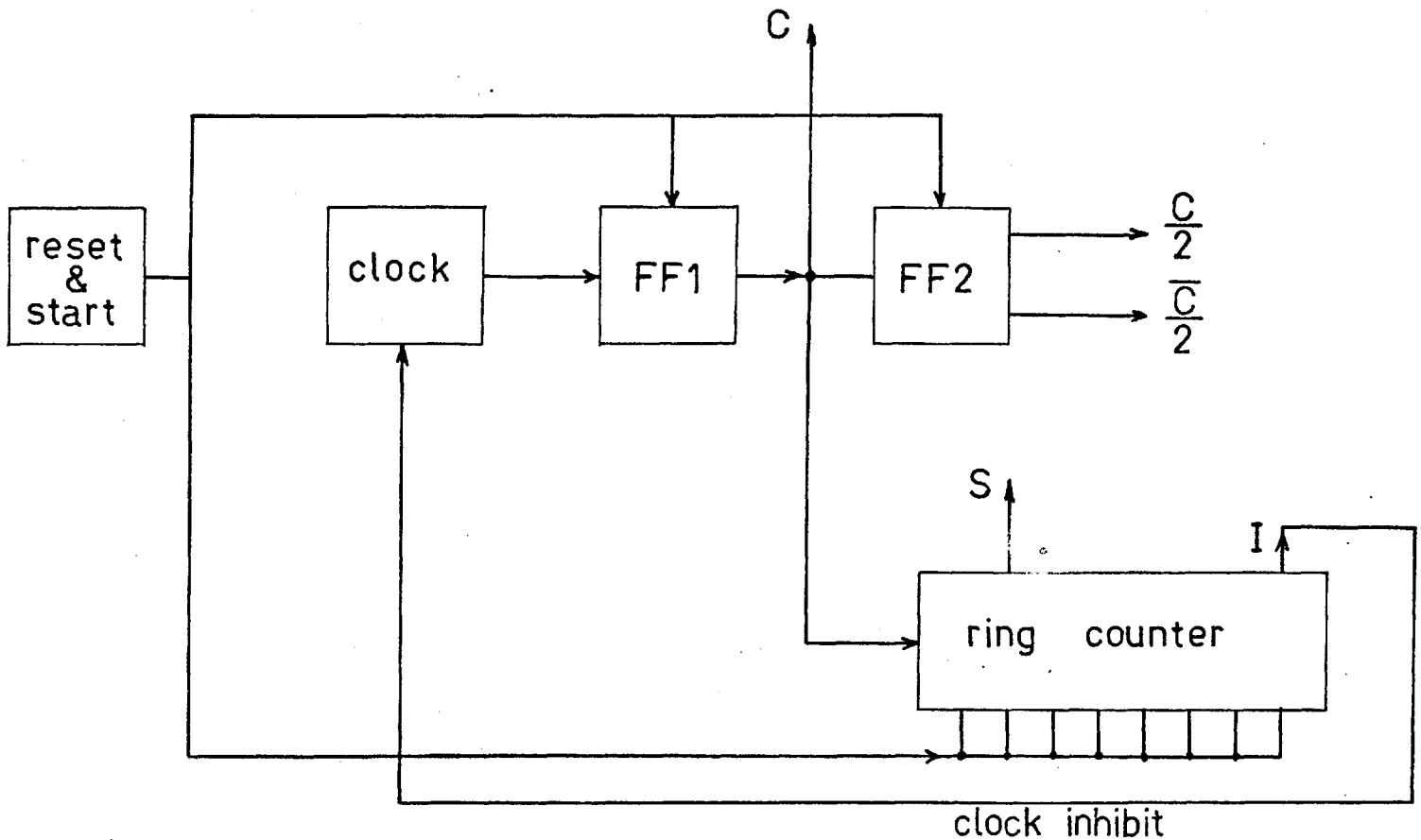


Fig. 4.1

Block Diagram of the Timing Circuit

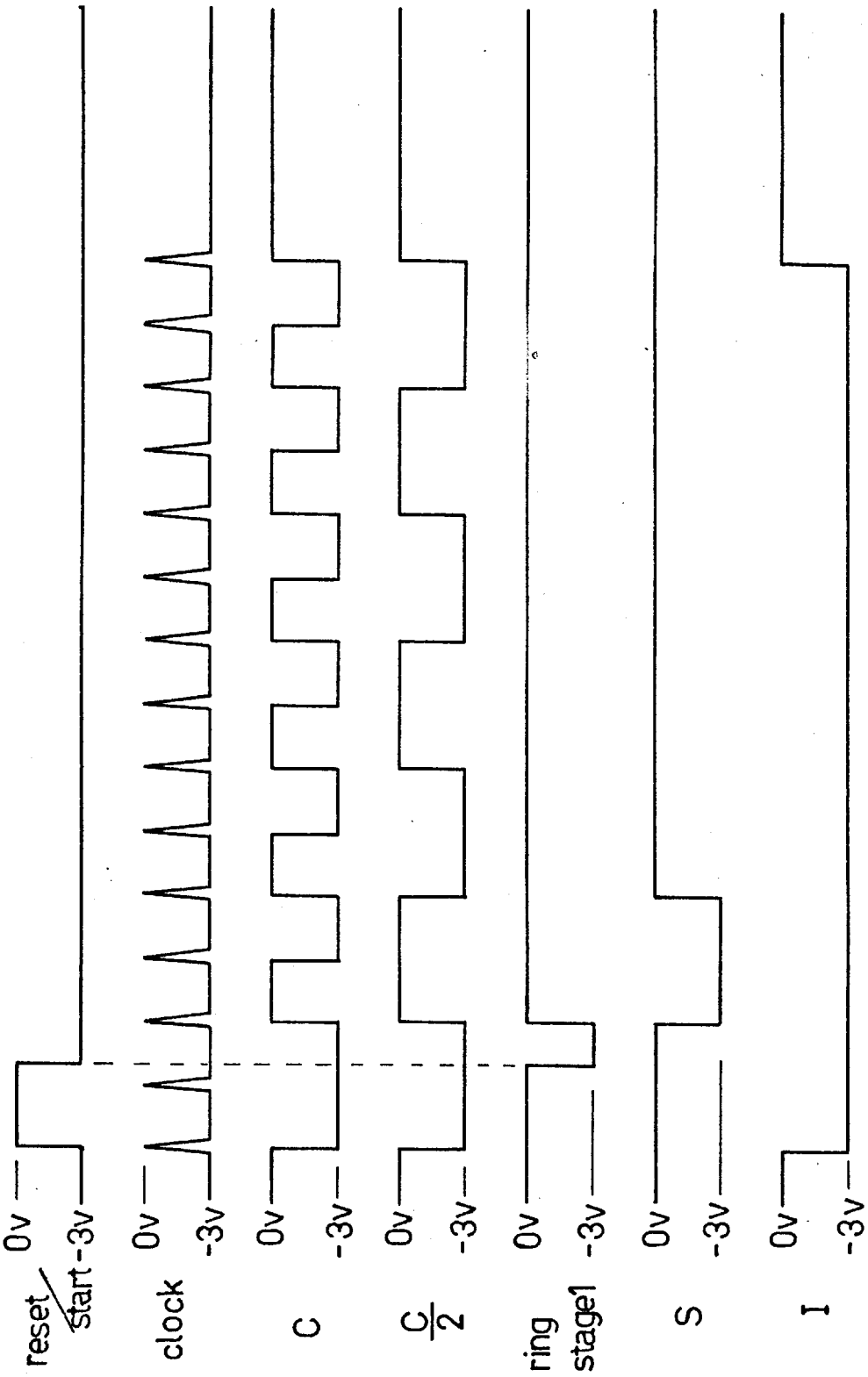


Fig. 4.2

Timing Diagram

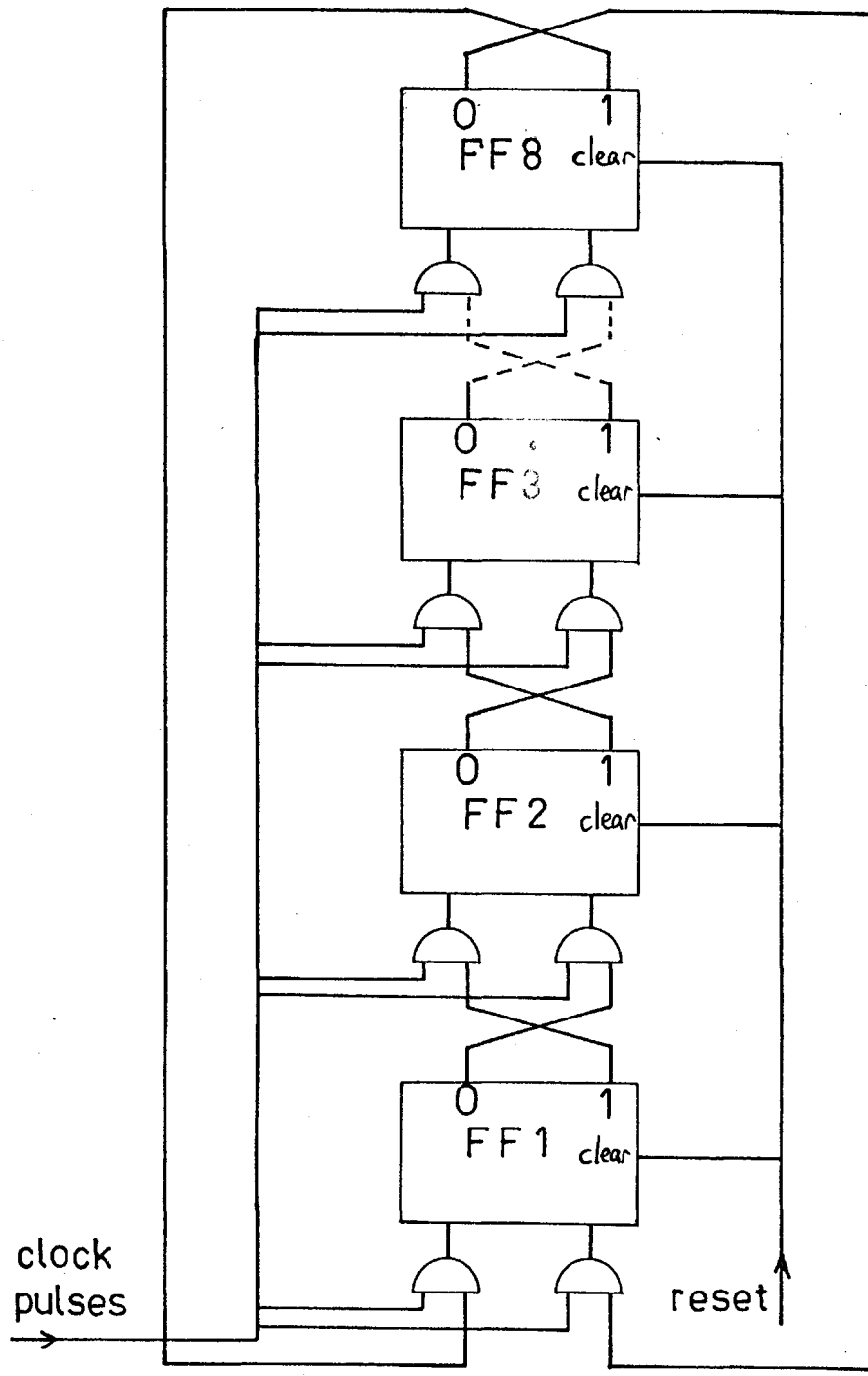


Fig. 4.3

Eight Stage Ring Counter

push button is depressed and the pulser output changes to a "zero", that is, O volts. This signal is used to set FF1 and FF2 and switches the ring counter from the 0000000l to the 10000000 state, that is, the inhibit signal is removed from the clock. When the push button is released, the next clock pulse advances the state of the ring counter to 01000000 and the conversion commences.

A wiring diagram of the timing circuit is shown in figure 4.4, the W520 module is included merely as a supply of -3volts.

4.2 Realization of the SSC Converter

The converter can be realized using Digital Equipment Corporation modules arranged as shown in figure 4.5. The switches 1, 2, 3 and 4 and their respective "and" gates are on an A12l Multiplexer switch module, and switches 5, 6 and 7 and their respective "and" gates are on another A12l module. The comparator is an A502 module. The $-E_{ref}$ supply is an A704 module. Hence E_{ref} is -10V and $\frac{E_{ref}}{2}$ is obtained from the $-E_{ref}$ supply by a potential divider of two 3kΩ precision resistors. A D type flip flop is obtained by using an R20l flip flop module and an R107 inverter as shown. The operational amplifier is a Philbrick type QFT5, FET differential input amplifier; its specification is given in the appendix

A wiring diagram of the converter is shown in figure 4.6.

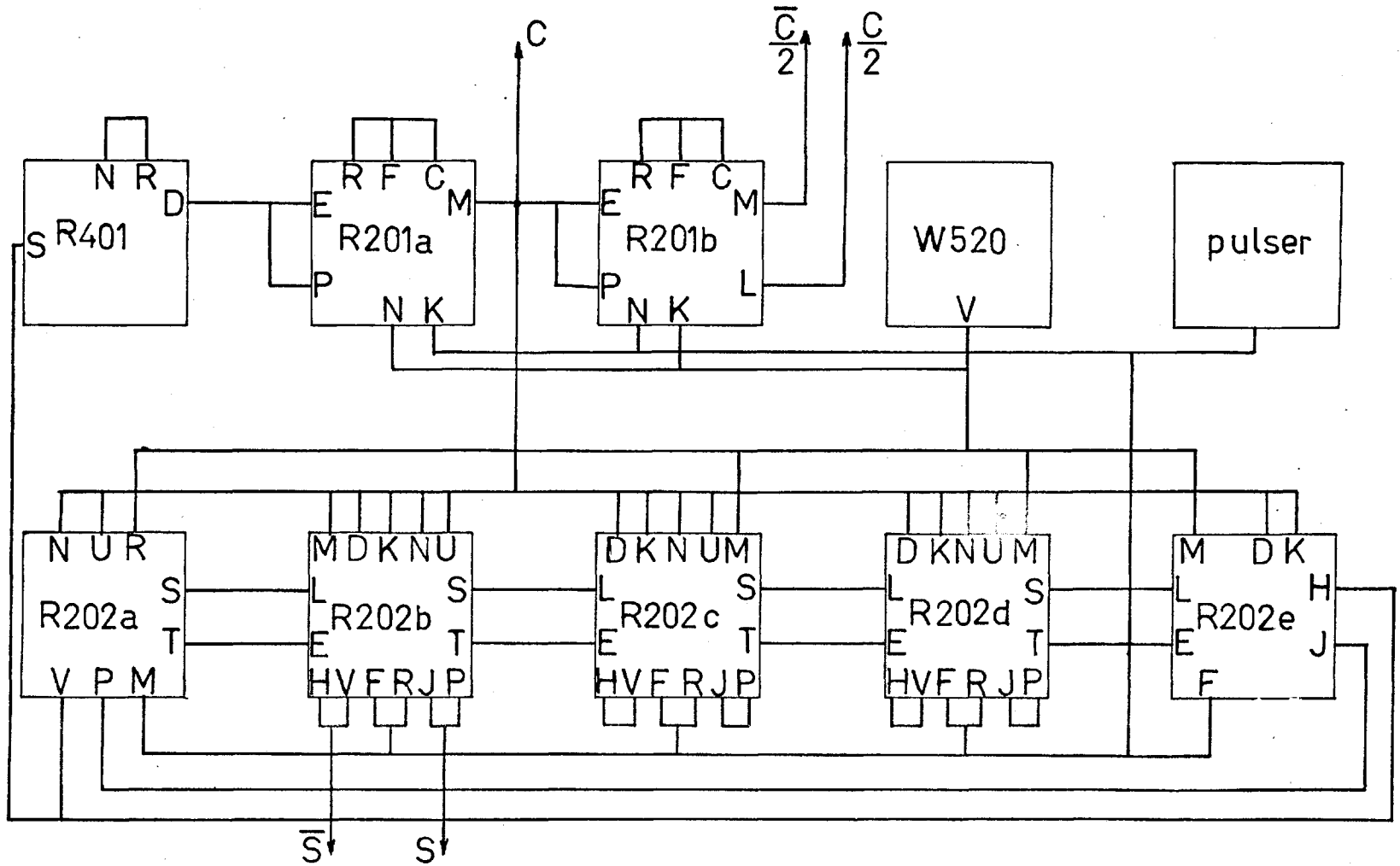


Fig 4.4

Wiring Diagram of the Timing Circuit

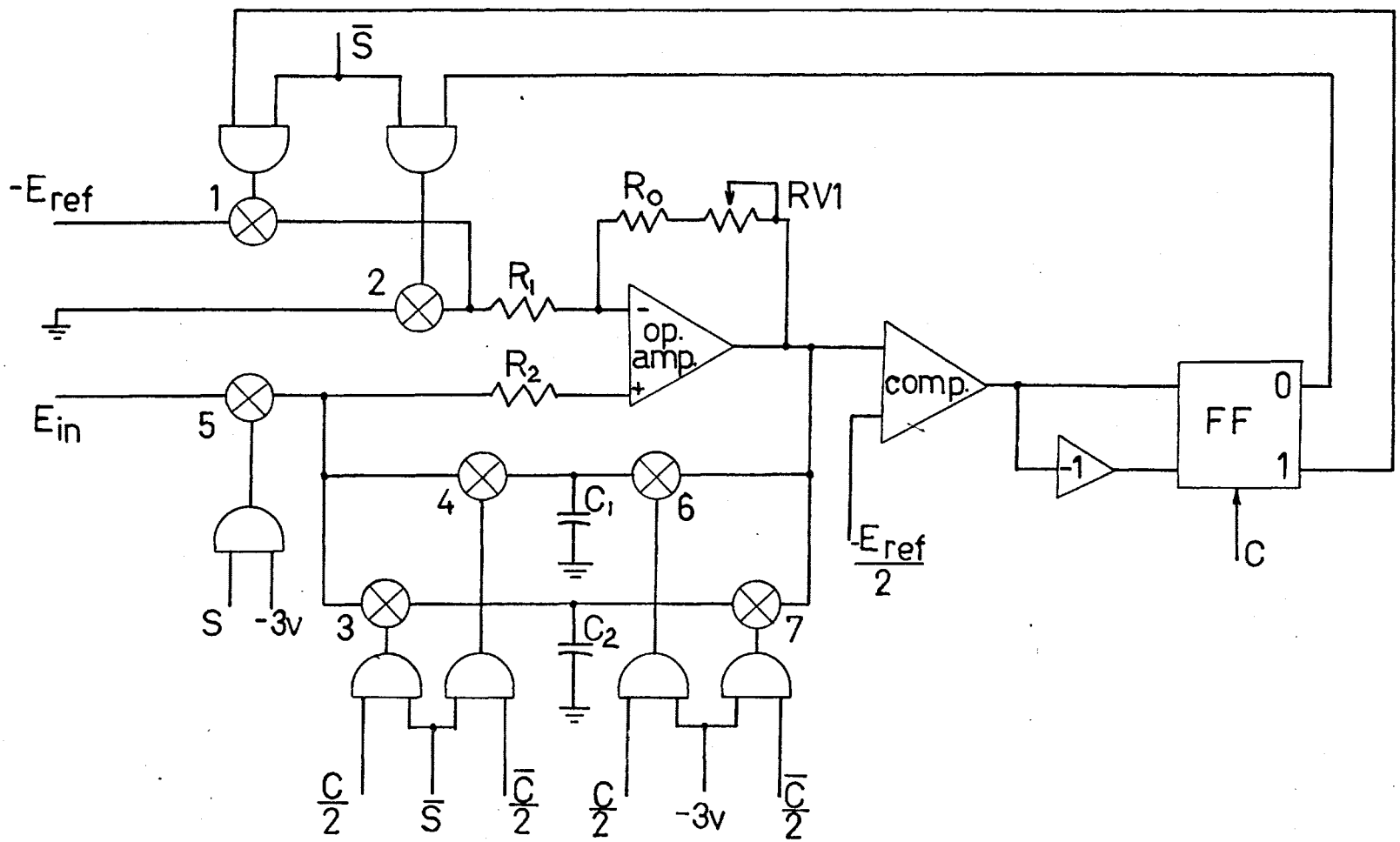


Fig. 4.5

SSC Converter using D. E C Modules

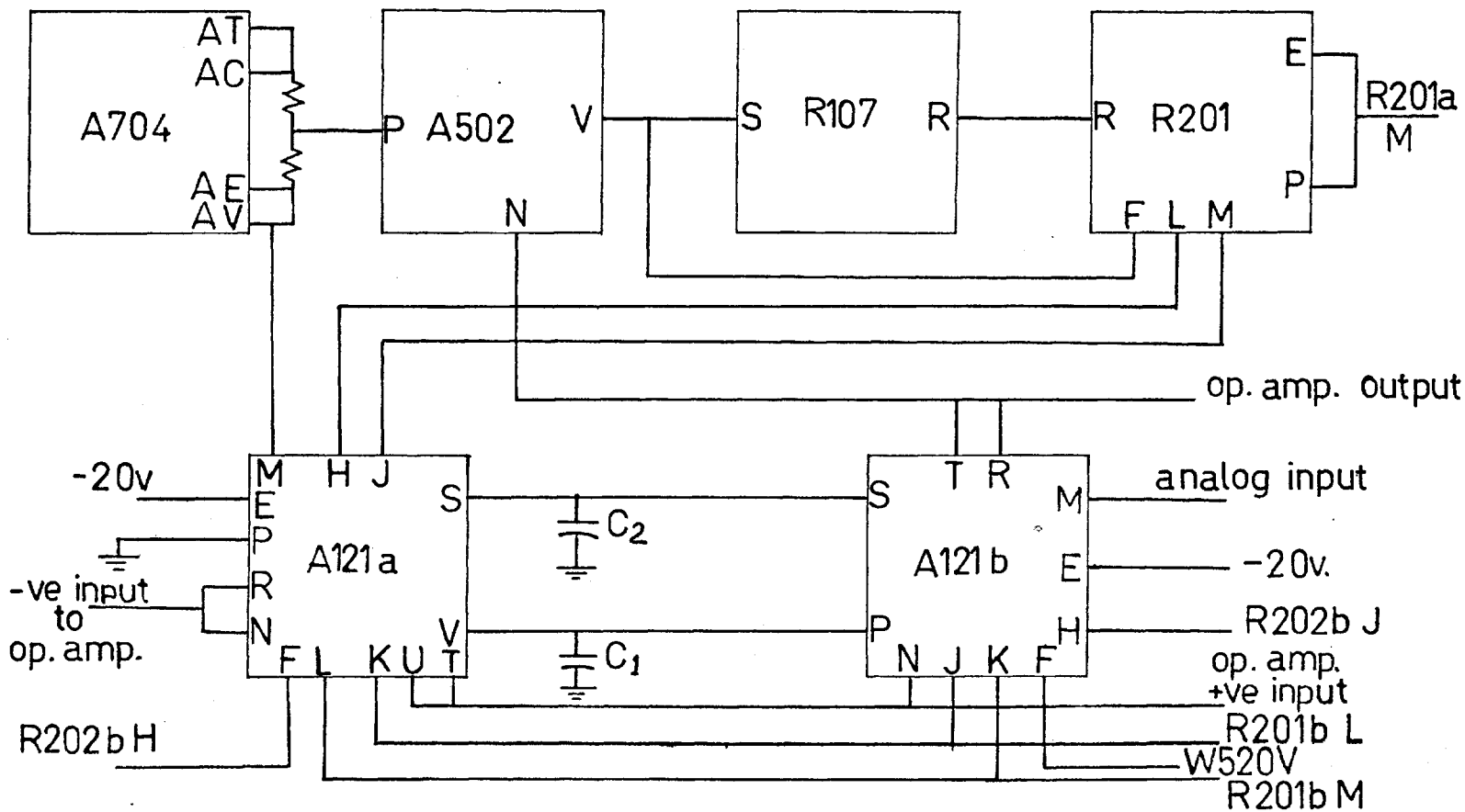


Fig. 4.6

Wiring Diagram of the SSC Converter

4.3 Calibration of the Converter

The calibration procedure was carried out as follows:-

(1) E_{ref} was adjusted to -10.000 volts

(2) $\frac{E_{ref}}{2}$ was adjusted to -5.000 volts.

(3) To obtain an offset null, the lead connected to pin D of the clock module was removed (refer to figure 4.4). The lead connecting pin H of module A121-a to pin L of module R201a figure 4.6, was disconnected from pin L and connected to OV; the lead connecting pin F of module A121-a to pin J of R 202a was disconnected at pin J and connected to -3volts; the lead connecting pin J of module A121-a to pin M of module R201-c was disconnected at pin M and connected to -3V. The above procedure connects the inverting input of the amplifier to ground through switch 2, figure 4.5. E_{in}, figure 4.5 was set to zero volts and the start button pushed, thus connecting the noninverting input to zero volts. The external 2.5K ohm trim potentiometer was then adjusted for minimum reading on a digital voltmeter monitoring the amplifier's output. The null voltage was reduced to -0.5mvolt.

(4) To adjust the amplifier for a gain of two in the noninverting mode, E_{in} was increased and the variable resistor RV_1 of figure 4.5 adjusted for a gain of two. Inputs of greater than -5 volts must not be used or the specifications for the multiplexer switches will be exceeded.

4.4 Results

Oscilloscope photographs of the C, $\frac{C}{2}$, S and I waveforms are reproduced in figure 4.7. The leading edge of the first C pulse was used to trigger the oscilloscope. These waveforms meet the requirements shown in figure 4.2.

An oscilloscope photograph of the operational amplifier's output, with an analog input of -4.000 volts is shown in figure 4.8a. The following steps are seen to have occurred:-

clock pulse one	-4V
clock pulse two	-(4x2-0) = -8V
clock pulse three	-(2x8-10)= -6V
clock pulse four	-(2x6-10)= -2V
clock pulse five	-(2x2-0) = -4V

resulting in a digital readout of 01101.

Some errors in these arithmetic steps are evident, and can be explained, to a large degree by the fact that the turn on delay of the multiplexer switches is 150 n seconds and the turn off delay is 250 n seconds. This means that for 100 n seconds during every switching interval, capacitors C_1 and C_2 are in parallel with each other, and charge will flow from one to the other, introducing an error.

This problem is illustrated in figured 4.8b and c. Figure 4.8b shows the voltage across C_1, and figure 4.8c shows the voltage across C_2, both for an analog input voltage of -4.000 volts. Initially, the voltage across C_1 charges to -4 volts, and the voltage across C_2 is 0 volts. Switching occurs in the following sequence:-

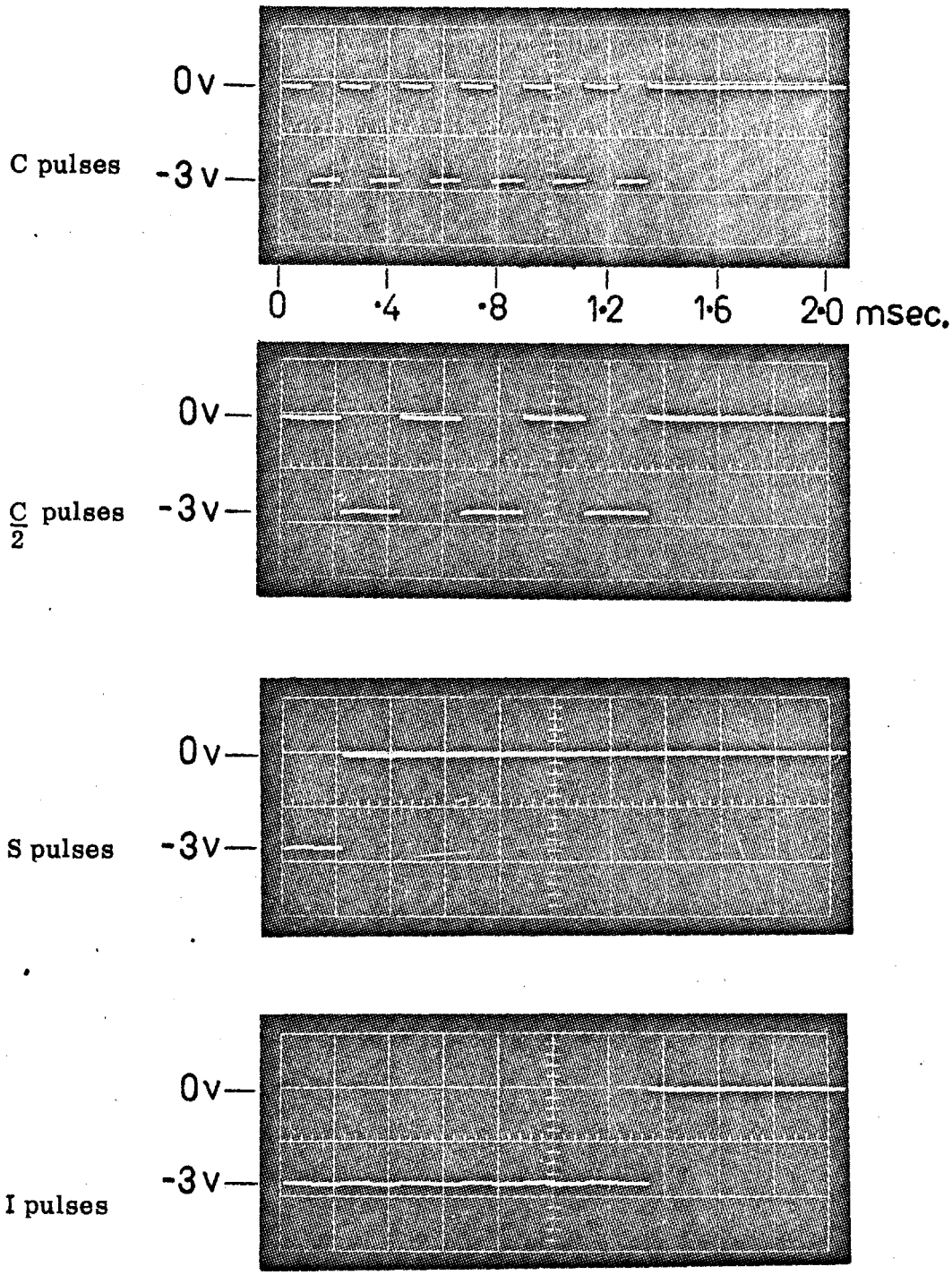
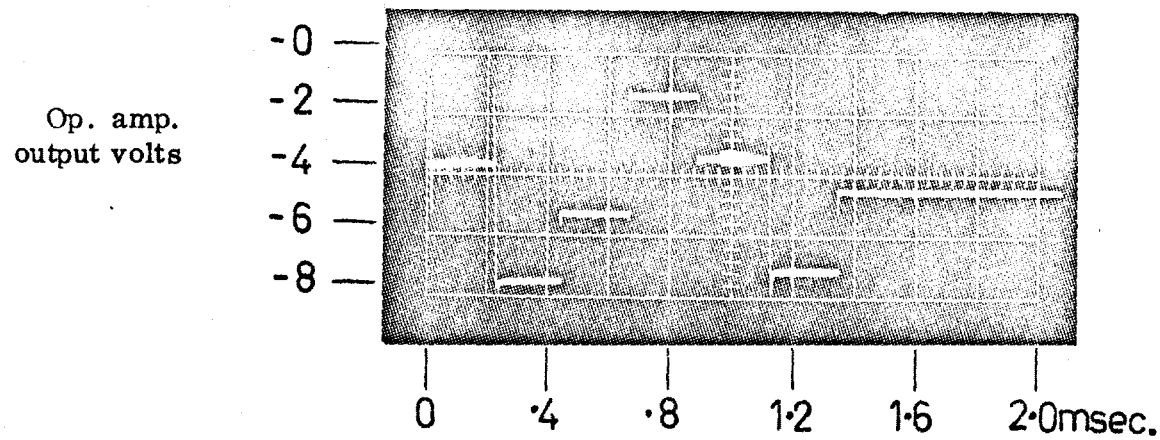
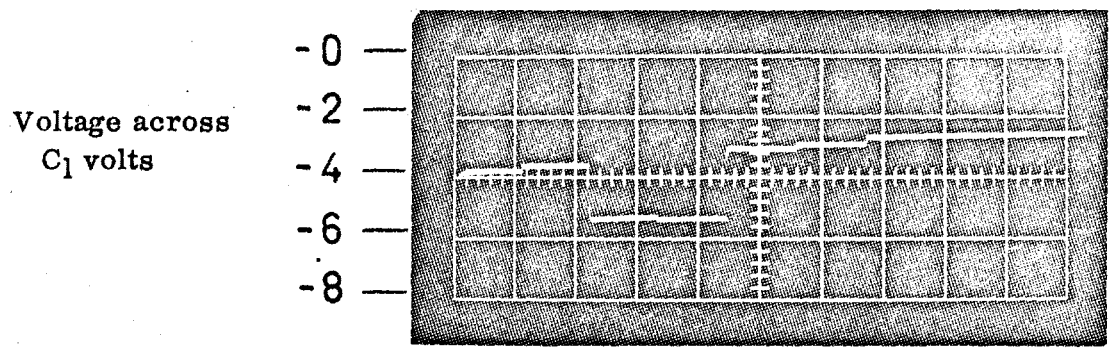


Fig. 4.7

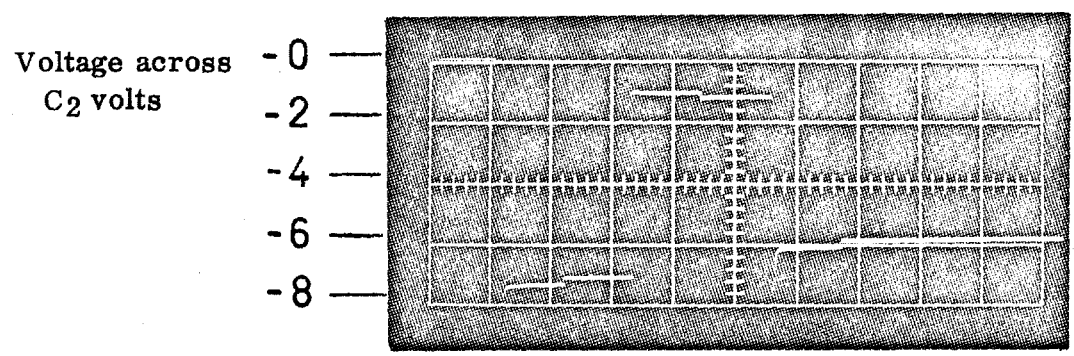
Timing Waveforms



(a)



(b)



(c)

Fig. 4.8

Waveform for a - 4 volt Analog Input

(l) Switches 4 and 7 close. Since switches 3 and 6 are already closed this connects capacitors C_1 and C_2 in parallel with each other

(ll) Capacitor C_1 with -4 volts across it loses some charge to C_2 which has 0 volts across it. The result is a drop in voltage across C_1.

(lll) Switches 3 and 6 open isolating capacitors C_1 and C_2 from each other.

During the next switching interval:-

(l) Switches 3 and 6 close.

(ll) Capacitor C_2 with -8 volts across it loses some charge to C_1 which has -4 volts across it. This results in a voltage drop across C_2.

(lll) Switches 4 and 7 open isolating C_1 and C_2 from each other.

During the next switching interval:-

(l) Switches 4 and 7 close.

(ll) Capacitor C_1 with -6 volts across it gains some charge from C_2 which has -8 volts across it.

(lll) Switches 3 and 6 open and C_1 and C_2 are again isolated from each other.

This type of action continues at all switching intervals.

Table 4.1 compares the measured limits of the quantizing levels to the theoretical limits; it can be seen that a maximum error of less than one quantizing level occurs. The converter operated up to a conversion speed of 35 microseconds.

These results were sufficiently encouraging to induce the author to design a more advanced form of the SSC converter using integrated circuits and field effect transistors.

Table 4.1

Converter Quantizing Errors

Theoretical quantizing levels' limits' volts	Quantizing level	Measured quantizing levels' limits volts	Error mV
0			
	0		
0.156		0.159	+3
	1		
0.313		0.321	+8
	2		
0.469		0.469	0
	3		
0.625		0.621	-4
	4		
0.781		0.771	-10
	5		
0.938		0.947	+9
	6		
1.094		1.082	-12
	7		
1.250		1.234	-16
	8		
1.406		1.384	-22
	9		
1.563		1.566	+3
	10		
1.719		1.708	-9
	11		
1.875		1.887	+12
	12		
2.031		2.011	-20
	13		
2.188		2.185	-3
	14		
2.344		2.328	-16
	15		
2.500		2.492	-8

2.656	16	2.669	+13
2.813	17	2.825	+12
2.969	18	2.987	+18
3.125	19	3.130	+5
3.281	20	3.291	+10
3.438	21	3.459	+21
3.594	22	3.600	+6
3.750	23	3.800	+50
3.906	24	3.910	+4
4.063	25	4.061	-2
4.219	26	4.215	-4
4.375	27	4.403	+28
4.531	28	4.516	-15
4.688	29	4.680	-7
4.844	30	4.820	-24
5.000	31	5.000	0
5.156	32	5.156	0
5.313	33	5.318	+5
5.469	34	5.482	+13
5.625	35	5.641	+16
5.781	36	5.800	+19
5.938	37	5.960	+22

	38		
6.094		6.139	+46
	39		
6.250		6.262	+12
	40		
6.406		6.435	+29
	41		
6.563		6.573	+11
	42		
6.719		6.728	+9
	43		
6.875		6.920	+45
	44		
7.031		7.035	+4
	45		
7.188		7.200	+12
	46/		
7.344		7.331	-13
	47		
7.500		7.561	+61
	48		
7.656		7.681	+25
	49		
7.813		7.834	+21
	50		
7.969		7.997	+31
	51		
8.125		8.160	+35
	52		
8.281		8.298	+17
	53		
8.438		8.469	+31
	54		
8.594		8.633	+39
	55		
8.750		8.834	+84
	56		
8.906		8.906	0
	57		
9.063		9.064	+1
	58		
9.219		9.224	+5
	59		
9.375		9.394	+19

CHAPTER 5

A MORE ADVANCED REALIZATION OF THE SSC CONVERTER

This chapter contains the design, construction details and evaluation of a more advanced version of the SSC converter, utilizing integrated circuits and field effect transistors.

5.1 Timing Circuit

A block diagram of the timing circuit is shown in Figure 5.1 and the resulting timing waveforms are shown in Figure 5.2. The clock is a Digital Equipment Corporation type M401 gateable clock. The remaining blocks are derived from Texas Instruments transistor-transistor logic (TTL) integrated circuits as follows:-

(I) The two divide by two circuits are derived from a dual J-K master-slave flip-flop type number SN7473N.

(II) The eight bit ring counter is derived from two five-bit shift register circuits type number SN7496N and supplies the synchronizing (S) and inhibit (I) signals. The $\overline{S}$ and $\overline{I}$ signals are obtained from the gates on a dual four input nand buffer type number SN7440N.

(III) The reset and start block is shown in more detail in Figure 5.3. This figure also shows the clock inhibit logic. Gates 1 and 2, and the two resistors are required to overcome the problem of bouncing contacts of the pushbutton switch.[14] Gates 3 and 4 are used so the clock can be inhibited

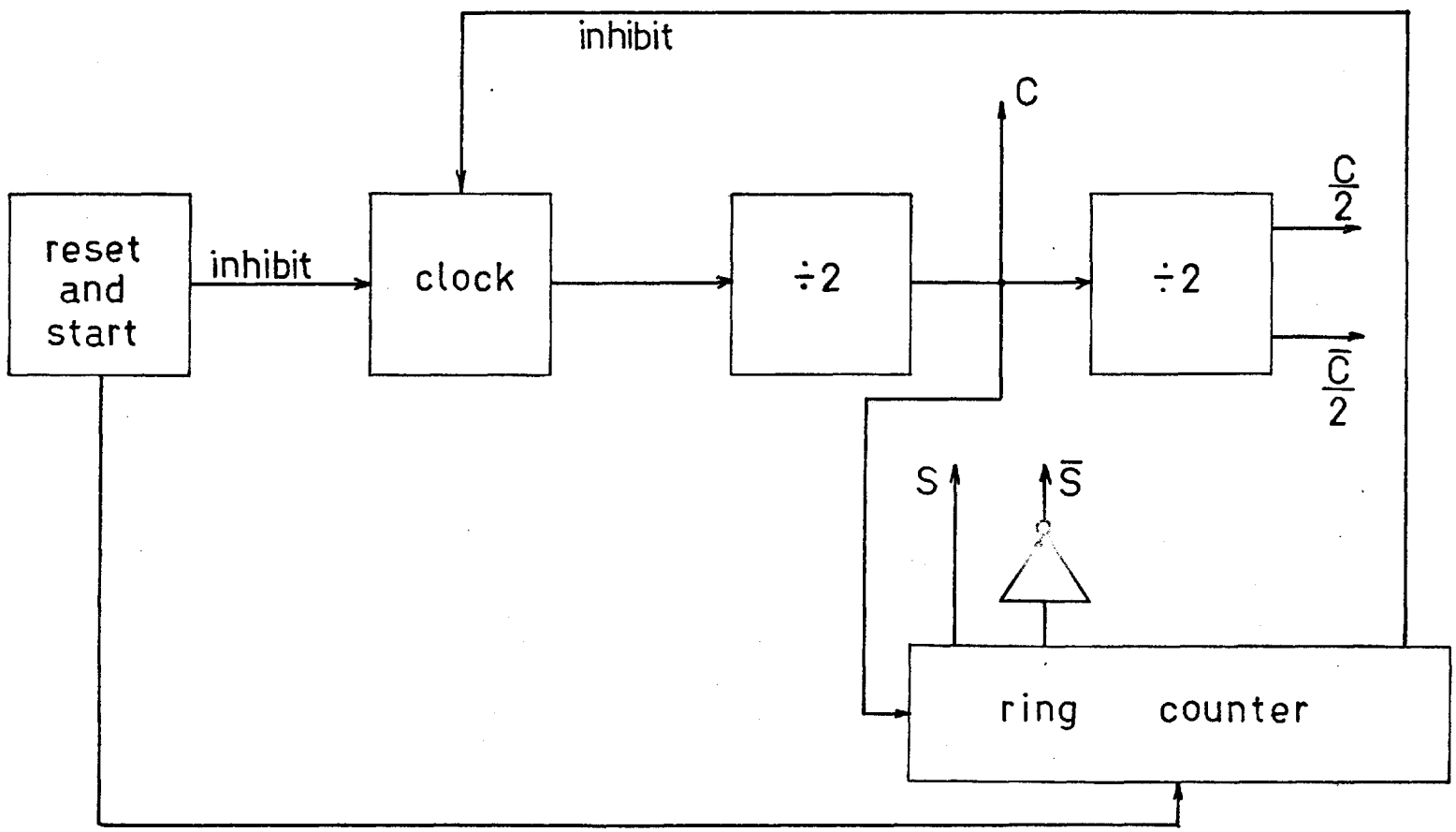


Fig. 5.1

Timing Circuit of the SSC Converter

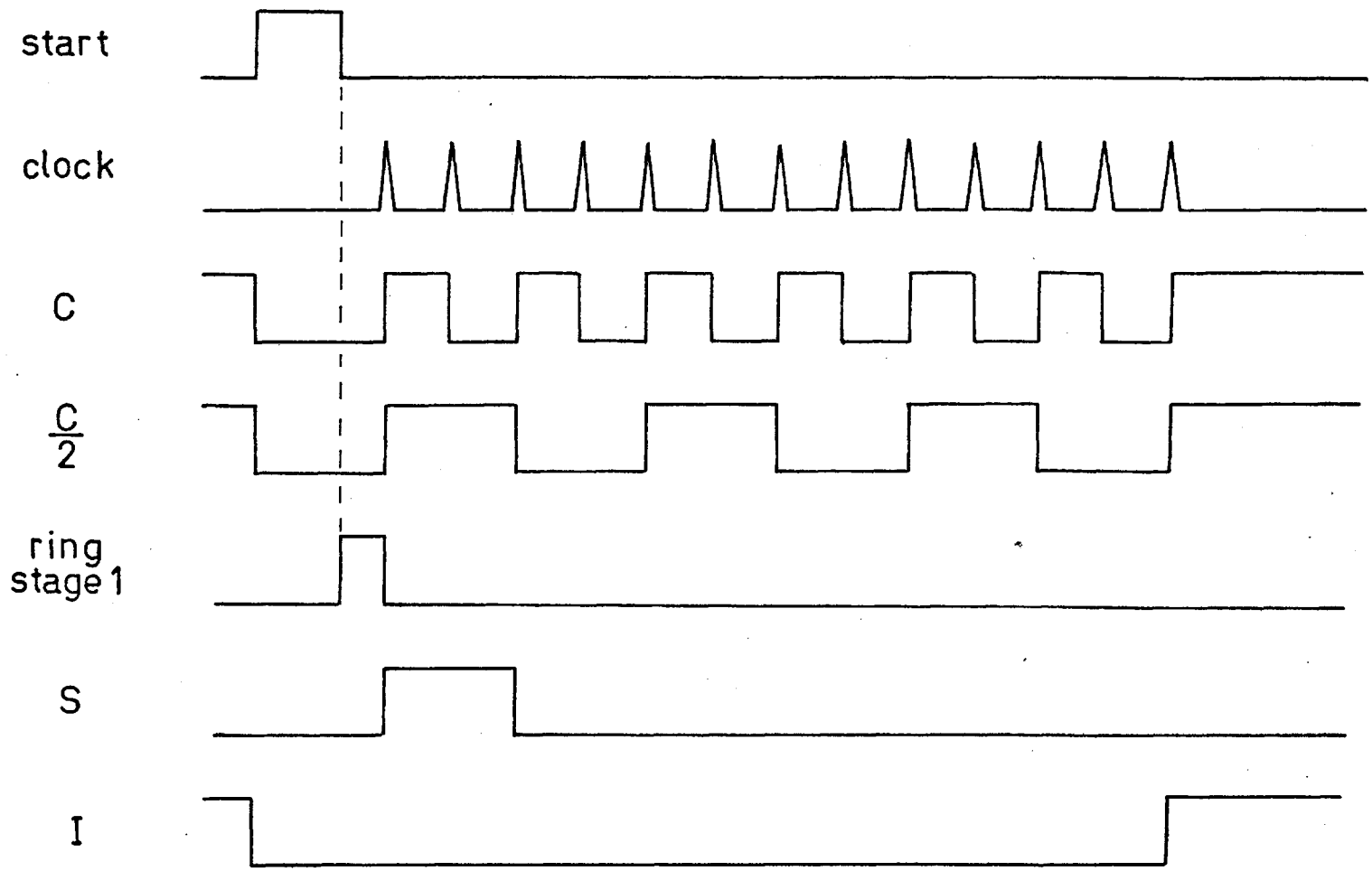


Fig 5.2

Timing Waveforms of the SSC Converter

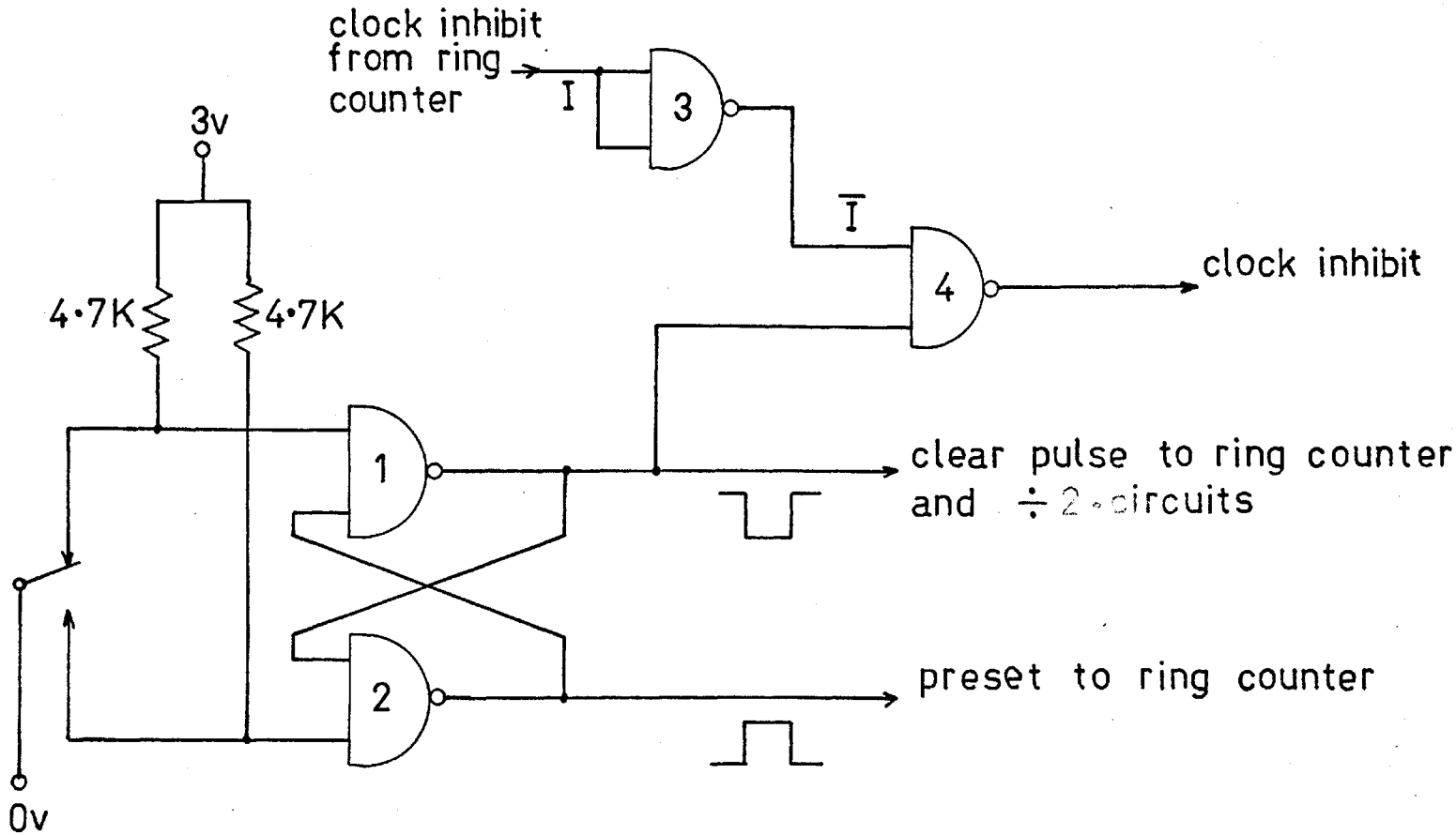


Fig. 5.3

Reset and Start Circuit

by the inhibit pulse from the ring counter, or when the reset-start button is depressed. A logic "one" delivered to the clock will inhibit it. The clear pulse is used to clear the ring counter and the divide by two circuits. The preset is used to set the first stage of the ring counter to the "one" state. The four gates are on a quadruple two input nand gate circuit type number 2N7400N.

A wiring diagram of the timing circuit is shown in Figure 5.4.

5.2 The SSC Converter Block Diagram

The block diagram of the SSC converter is shown in Figure 5.5. The nand gates driving the switches are derived from two dual four input nand buffers Texas Instruments type SN7440N. The not "inhibit" input to the gate driving switch 1 is necessary, because if the converter is on but not operating switch 3 will be open and capacitor C_2 will eventually discharge. As a result if switch 1 is on E_{ref} will appear at the amplifier output at $-E_{ref}$, that is -5V, and be applied to the comparator input, since the comparators other input is at +2.5V a differential input of 7.5V occurs and this exceeds the rating of the comparator. It is therefore necessary to isolate E_{ref} from the amplifier input except when a conversion is in progress. This is achieved using the "not inhibit" signal.

The D type flip flop is one of the flip flops on a Texas Instruments type SN7474N dual D type edge-triggered flip flop. The seven analog switches use field effect transistors (FETs) as their switching elements and are described in detail in section 5.3. The E_{ref} and $E_{ref}/2$ supplies were designed as shown in section 5.4. The comparator is a Texas Instruments type SN72710N comparator and more

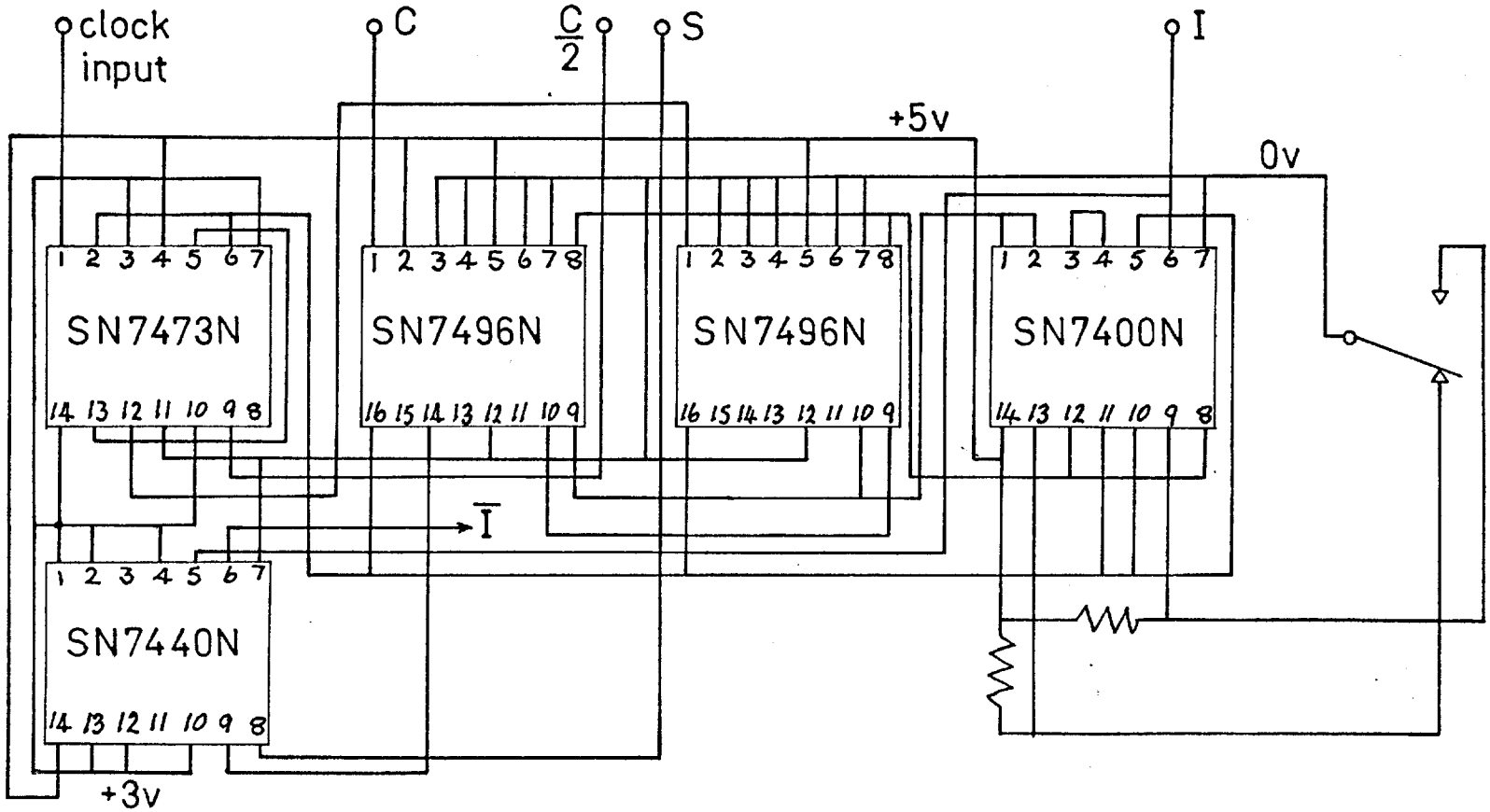


Fig. 5.4

Wiring Diagram of the Timing Circuit

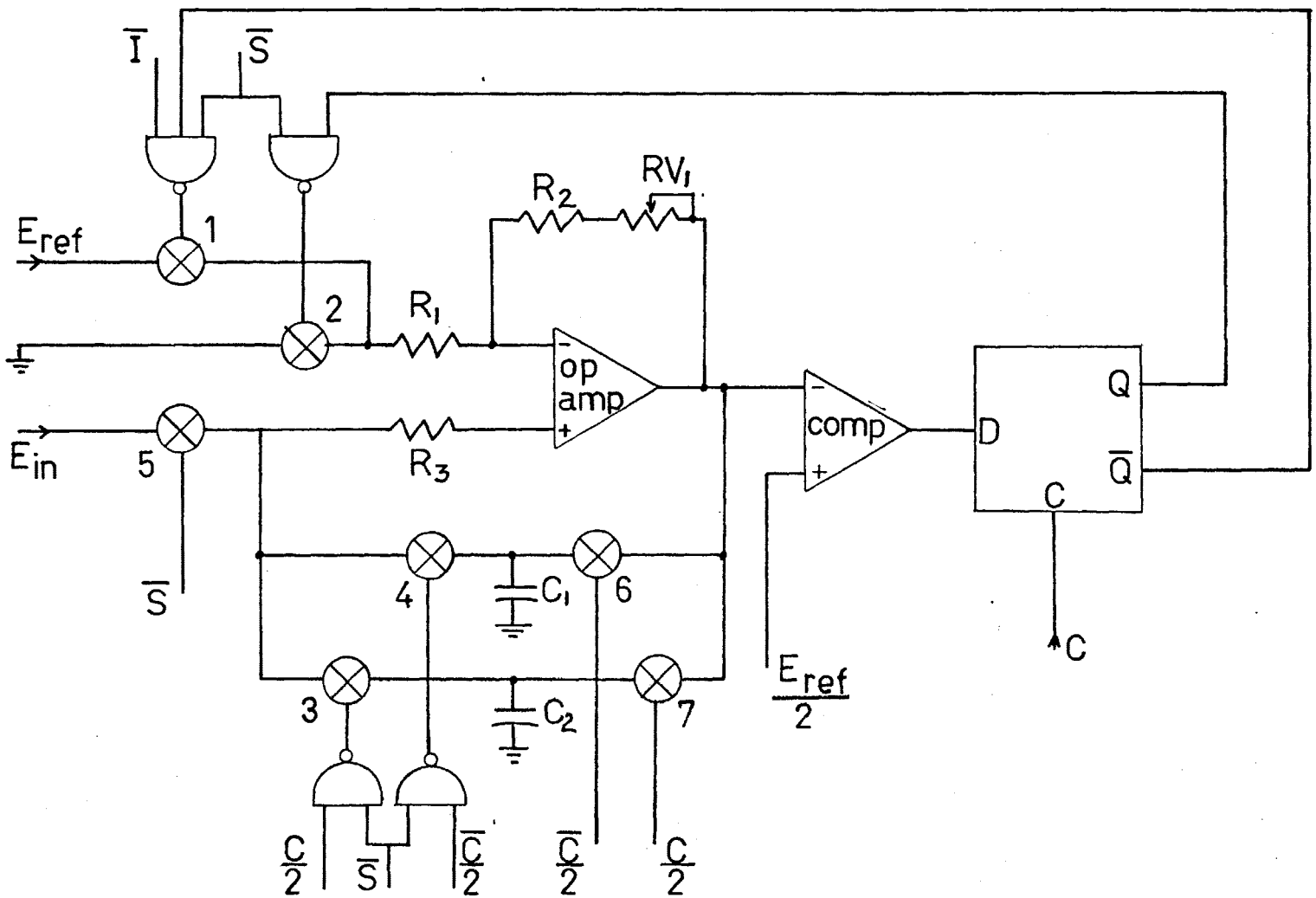


Fig. 5.5

Block Diagram of the SSC Converter

information on this unit is given in section 5.5. Two different operational amplifiers were used and are described in sections 5.7 and 5.8.

The value of the components shown in figure 5.5 are:

$R_1 = R_2 = 10$Kohms

$RV_1 = 200$ ohms

$R_3 = 4.7$K ohms

$C_1 = C_2 = 4,700$pF

5.3 FET Analog Switches[15.16.17.18.19]

The drain characteristics of an n channel junction FET are shown in Figure 5.6. The on resistance, R_{on}, is the reciprocal of the slope of the characteristic before the saturation knee. It can be seen from the figure that as V_{GS}

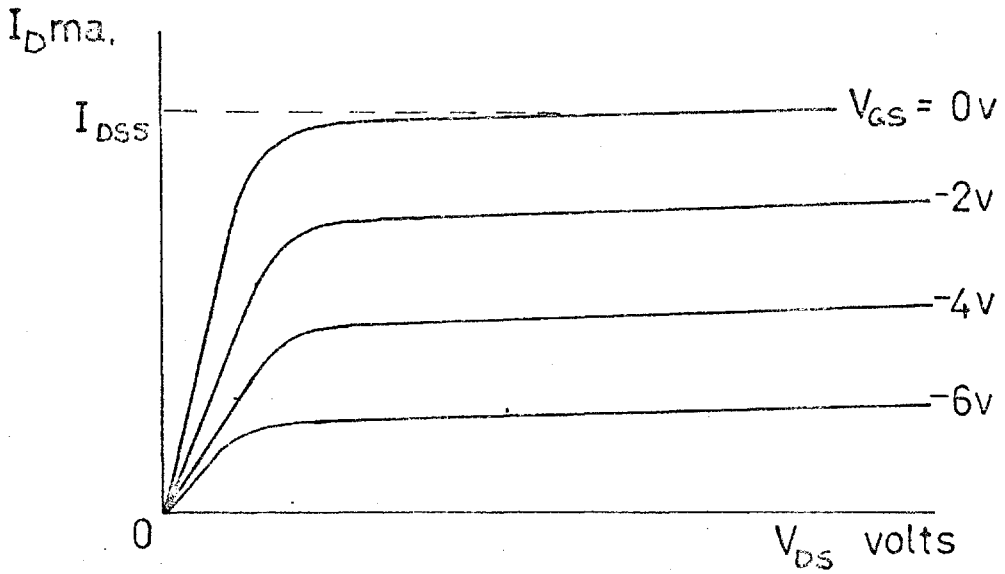


Fig. 5 6

Drain Characteristics of an n Channel FET

becomes more negative the on resistance of the FET increases, until at $V_{GS} = -V_p$ the drain to source current I_{DS} is reduced to zero and the FET is switched off. $-V_p$ is known as the pinch-off voltage. I_{DSS} is the drain to source saturation current.

The simplest FET switch possible together with its associated waveforms is shown in Figure 5.7 The input voltage $-E_{IN}$ is a d.c. value with a possible range from O to $-E_{max}$ and is shown in the figure by a broken line. The output voltage is equal to $-E_{IN}$ when the switch is on.

Suppose R_{ON} must not vary by more than 2:1 and as a result $-E_{GS}$ can only vary from OV to $\frac{-E_p}{2}$. Since $-E_{GS} = -E_G + E_{IN}$, the gate voltage to hold the switch on, E_{GON} must not go more positive than $\frac{-E_p}{2}$. Let $-E_{GON} = \frac{-E_p}{2}$; E_{INMAX} is then $\frac{-E_p}{2}$ to prevent forward biasing of the source to gate junction. The switch is turned off when the gate to source voltage, $E_G - E_{IN}$ is more negative than the pinch off voltage, $-E_p$. Therefore for pinch off to occur when $-E_{IN} = -E_{MAX}$, $-E_{GOFF}$ must be equal to a greater than $-(E_p+E_{MAX})$.

It is seen from the above that this type of switch is only good for input voltages of less than $\frac{E_p}{2}$ and even then R_{ON} varies by a factor of 2:1.

A circuit that provides $E_{GS} = O$ for an input voltage within a specified range, is shown along with its associated waveforms in Figure 5. 8. When the gate drive voltage E_G is positive the diode CR1 is reverse biased and the gate assumes the same voltage as the source; hence R_{ON} is maintained at its minimum value. Application of a negative gate drive voltage forward biases the diode switching it

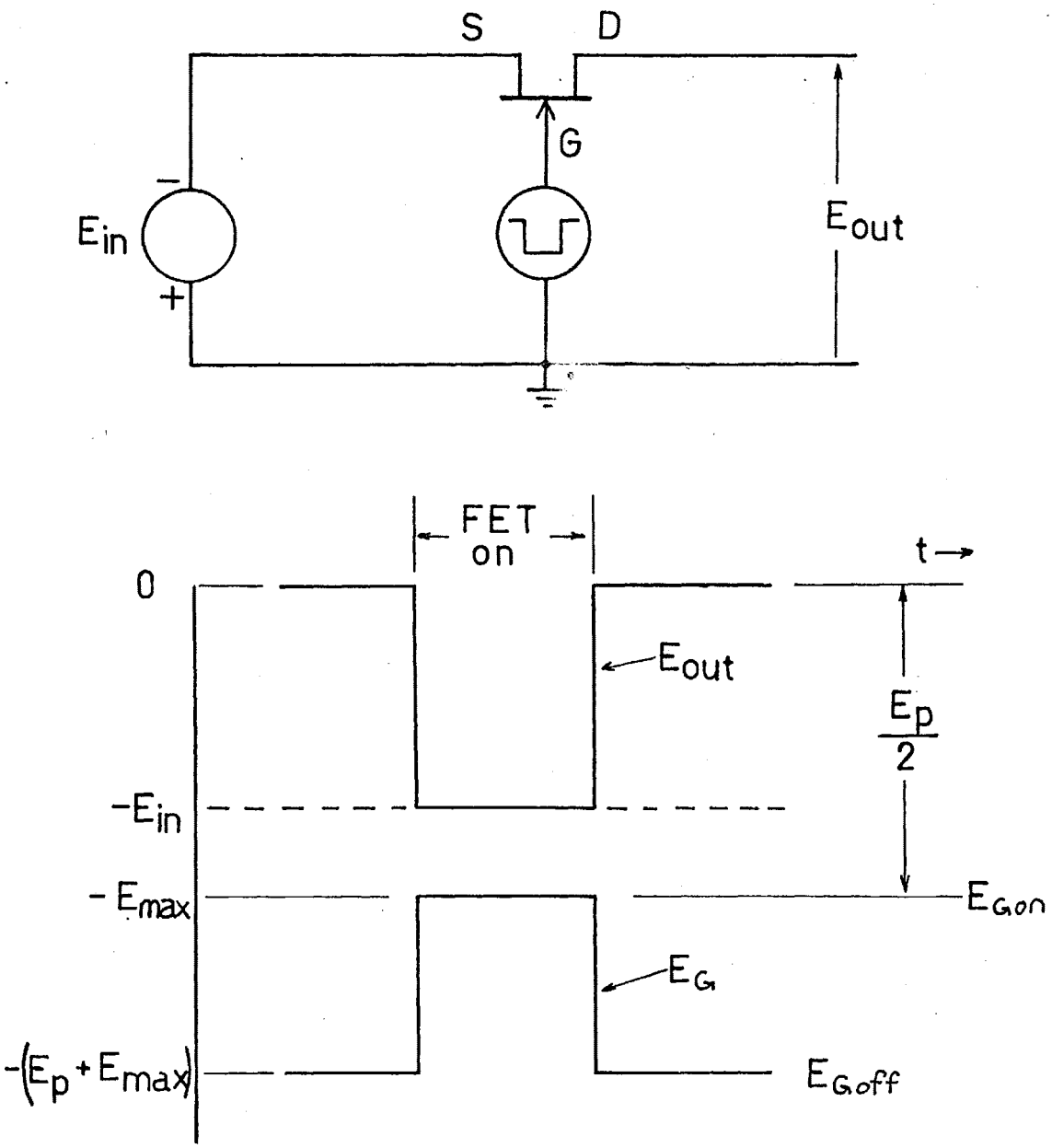


Fig. 5.7

A Simple FET Analog Switch

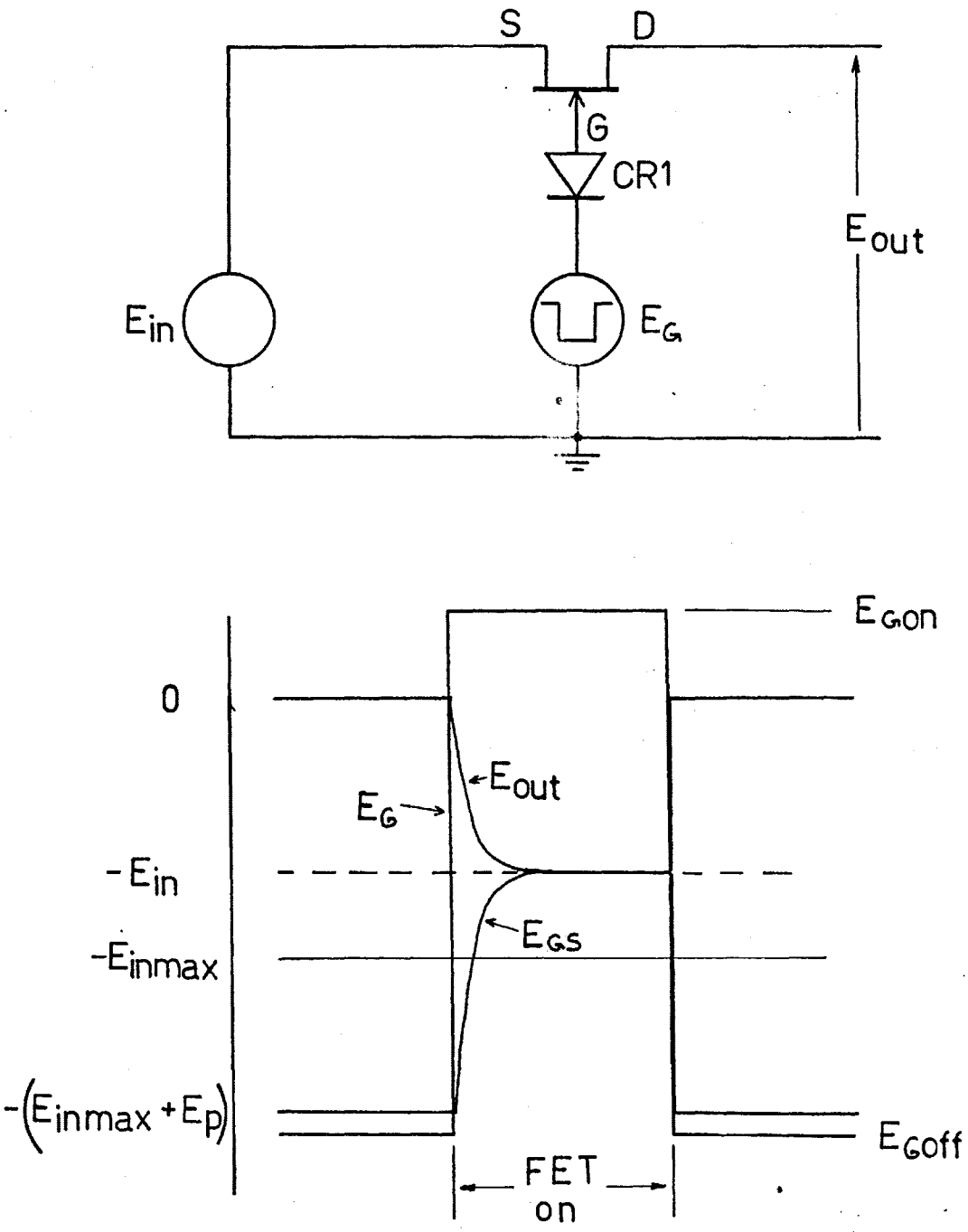


Fig. 5.8

Principles of the FET Analog Switch

on, therefore the negative gate drive voltage is applied to the gate and the switch is turned off. The voltage limits for this circuit are:

(l) E_{IN} cannot be more positive than E_{GON}, as this would result in a forward bias between the gate and source.

(ll) E_{IN} cannot go more negative than $E_{GOFF}-E_p$.

For the SSC converter it was necessary to limit the analog input to the range O to +5V (see section 5.5).

Therefore from (l) $E_{GON} \geqslant 5V$ (1)

and from (ll) $E_{GOFF} \geqslant E_p$ (2)

where E_p is typically -7V

A circuit had to be designed to generate the voltages given by equations(l) and (2) from the integrated circuit logic levels of O and 3V.

A circuit that can meet these requirements is shown in Figure 5.9, where

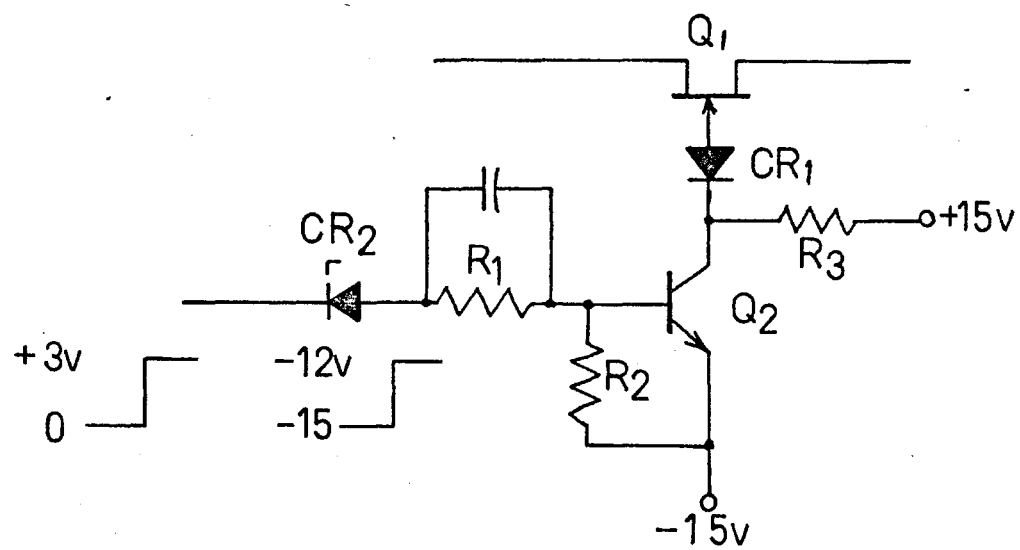


Fig. 5.9

The FET Analog Switch

CR_2 is a 15 volt zener diode and Q_2 is a high speed switching transistor. When the input is at OV the anode of CR_2 is at -15V hence Q_2 is held off, therefore its collector is at +15V and the diode CR_1 is reverse biased and the FET Q_1 conducts. When the input rises to +3V the anode of CR_2 rises to -12volts and the transistor turns hard on, therefore its collector drops to -15V and forward biases the diode CR_1, thus switching the FET off.

Since the FET is switched on by the bipolar junction transistor switching off, the switches will open more quickly than they close, which is the desired switching action as discussed in section 4.4.

The devices selected for this switching circuit were:

(I) A Texas Instruments TIS73 n channel junction FET was selected for Q_1 due to its low on resistance of 25 ohms, high saturation current, I_{DSS}, of 50mamps, and low drain to gate capacitance C_{DG}= 8pF.

(II) A 2N5028 silicon transistor was selected for Q_2 because of its high cut off frequency f_t = 500MHz and the fact that its collector to emitter breakdown voltage V_{CEO} equals the necessary 30 volts.

(III) A 1N3182 was selected for diode CR_1 due to its low leakage current of 2 namps at a reverse voltage of 20 volts.

(IV) A Philips type BZY88C15 zener diode was selected as the 15V zener diode.

The resistance values were calculated as follows:

Let R_3 = 4.7Kohms

Then $I_c = \frac{30}{4.7} = 6.4\text{mA}$

From 2N5028 specifications

$h_{FEmin} = 100$

therefore the necessary base current is

$I_{Bmin} = \frac{6.4}{100} = .064\text{mA}$

Overdrive the base current three times to reduce the turn on time;

therefore $I_B = .192\text{mA}$

The voltage across R_1 and R_2 in Q_2's conducting state is 3 volts, the voltage across R_2 is 0.7 volts (V_{CEsat}) therefore the voltage across R_1 is 2.3 volts.

Let bleeder current through R_2 = 0.3mA

therefore $R_2 = \frac{0.7}{.3} \approx 2.2\text{K}$

The current through R_1 = 0.3 + 0.19mA

= 0.49 mA

therefore $R_1 = \frac{2.3}{.49} \approx 4.7\text{kohms}$

5.3.1 Switching Waveforms

The analog switch shown in Figure 5.9 was tested using a 4.7Kohm resistive load and +5v dc input. Oscilloscope photographs of the switching waveforms as the switch turned on are reproduced in Figure 5.10. Figure 5.11 shows the waveforms for the switch turning off. From the figures it can be seen that the switch turns off more rapidly (0.2μsecs) than it switches on (0.3μsecs) as required.

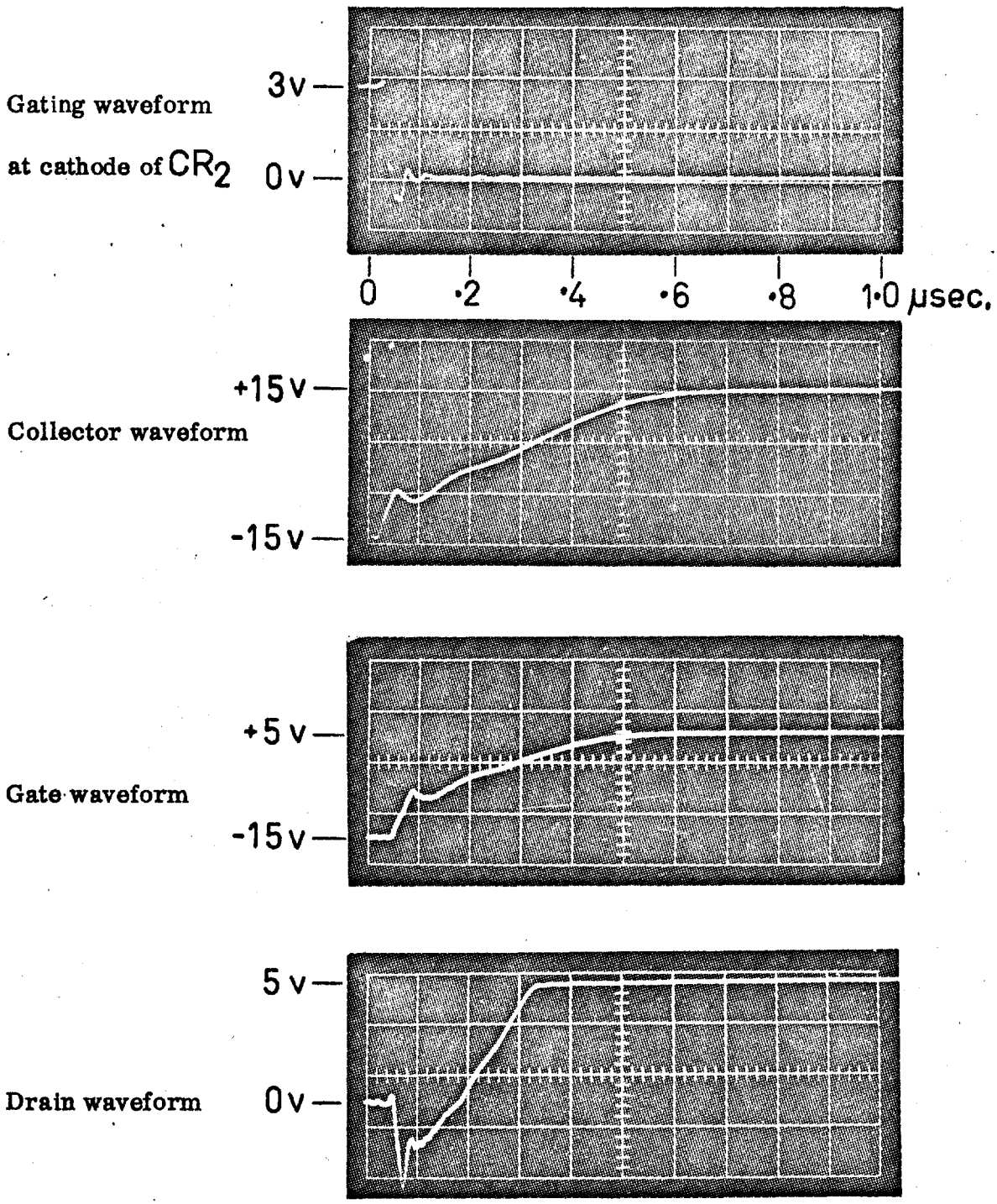


Figure 5.10

Waveforms for switch turning on.

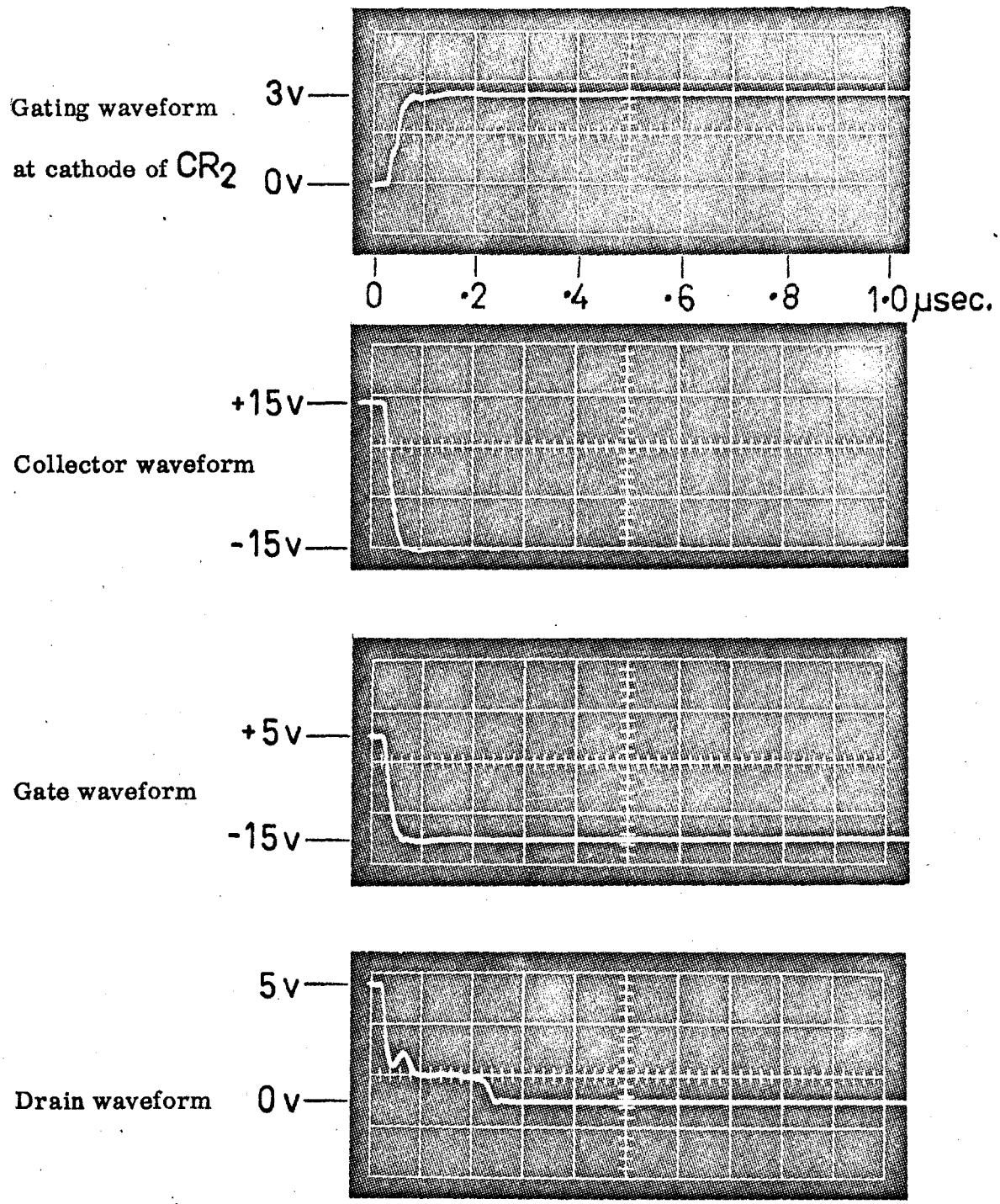


Figure 5.11

Waveforms for switch turning off.

5.4 Reference Supplies

The 5V reference supply shown in Figure 5.12 was designed to meet the following specification:-

(l) Required reference voltage +5V ± 5mV

(ll) Load current 0 to 0.5mA

(lll) Input power supply +15V ± 4%

(lV) Ambient temperature 25°C

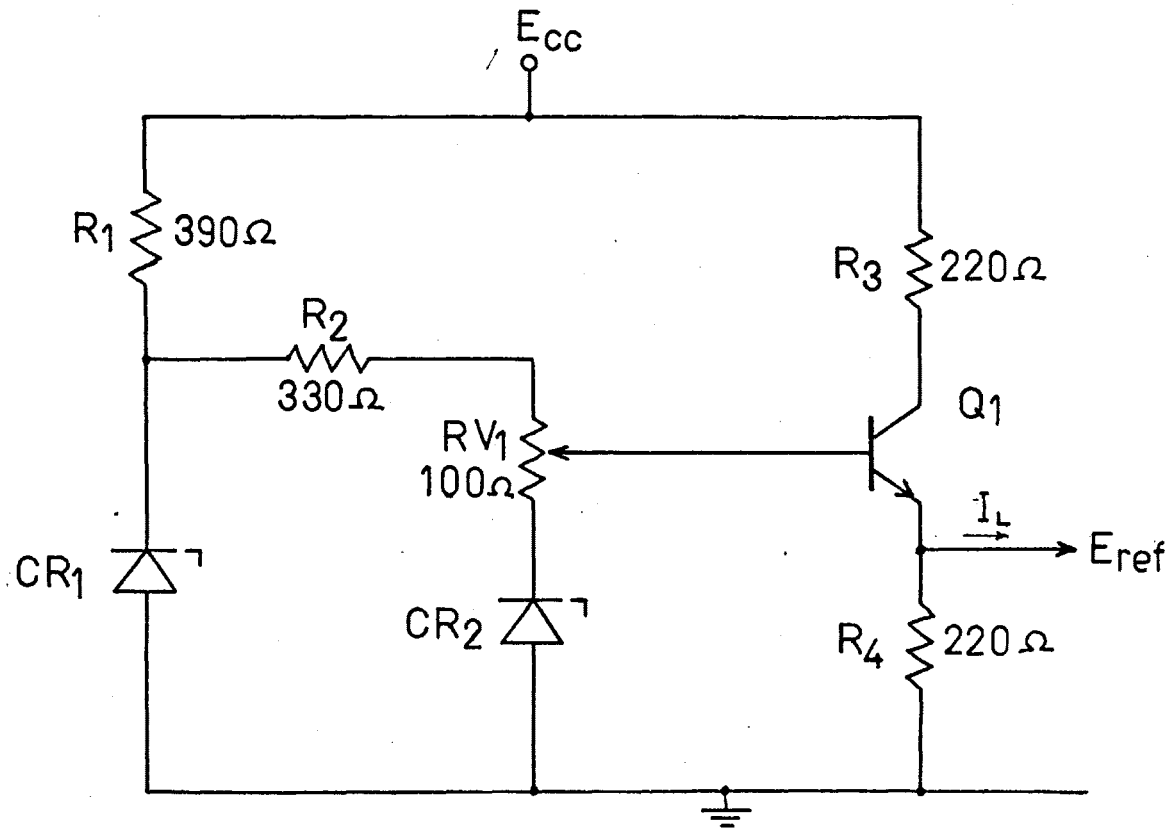


Fig. 5.12

5 Volt Reference Supply

E_{ref} for this circuit varies from its nominal value due to changes in E_{cc}, I_L and temperature Zener diodes CR_1 and CR_2 are used to stabilize E_{ref} against changes in E_{cc}, as follows:-

If E_{cc} changes by ΔE_{cc} the voltage across CR_1 changes by ΔE_{Z1}

$$\Delta E_{Z1} = \Delta E_{cc} \frac{Z_1}{R_1+Z_1} \quad (1)$$

where Z_1 is the dynamic impedance of CR_1. The variation in E_B, the voltage at the base of transistor Q_1, is therefore

$$\Delta E_B = \Delta E_{Z1} \frac{Z_2}{R_2 + R_5 + Z_2} \quad (2)$$

where Z_2 is equal to the sum of the dynamic impedance of CR_2 and R_6; the resistance from the wiper of RV_1 to CR_2. R_5 is the resistance from the wiper of RV_1 to R_2.

Since transistor Q_1 is in the emitter follower configuration, the change in E_{ref}, ΔE_{ref} that occurs due to a change in E_{cc} of ΔE_{cc} is ΔE_B. ΔE_B is obtained by combining equations (1) and (2) which yields

$$\Delta E_{ref}\Big|_{\Delta I_L=0} = \Delta E_{cc} \left(\frac{Z_1}{R_1+Z_1}\right) \left(\frac{Z_2}{R_2+R_5+Z_2}\right) \quad (3)$$

The emitter follower Q_1 is used to reduce the changes in ΔE_{ref} that occur due to changes in load current ΔI_L.

$$\Delta E_{ref}\Big|_{\Delta E_{cc}=0} = \Delta I_L Z_o + \Delta I_Z Z_2 \quad (4)$$

where Z_o is the dynamic output impedance of the emitter follower, and ΔI_Z is the variation in current through CR_2 as a result of the change in load current ΔI_L.

The zener diodes used in the reference supply are:-

(1) CR_1 is a Philips BZY94C10 400m watt zener diode with a breakdown

voltage of 10V at I_Z = 5mA, a temperature coefficient S_Z = 7mV/°C, and a dynamic impedance of less than 25 ohms.

(11) CR_2 is a Texas Instruments 1N752 400m watt reference diode with a breakdown voltage of 5.6V at I_Z = 20mA, a temperature coefficient S_Z = +.006%/°C and a dynamic impedance of less than 11 ohms.

Substituting the above information into equation (3) for ΔE_{cc} = 0.6V (i.e. 4% of 15V) yields

$$\Delta E_{ref} \Big| \Delta I_L = O \quad = 3.0\text{mV} \tag{5}$$

The dynamic output admittance, Z_o of the 2N5183 used as Q_1 is given by

$$Z_o = r_e + \frac{Z_2}{h_{fe}}$$

where r_e is the emitter diode resistance given by

$$r_e \approx \frac{25}{I_{EmA}} = 1.1 \text{ ohms}$$

Z_2, the dynamic resistance between the base of Q_1 and ground is 36 ohms and $h_{femin} = 70$

therefore $Z_o = 1.1 + \frac{36}{70} = 1.61$ ohms

ΔE_{ref} due to a load current variation of 0.5mA is calculated using equation (4) and yields

$$\Delta E_{ref} \Big|_{\Delta E_{cc}=0} = 1.1\text{mV} \tag{6}$$

The worst case variation $\Delta E_{ref\ max}$ due to variations of ΔE_{cc} and ΔI_L is therefore from equations (5) and (6)

$$\Delta E_{ref\ max} = 4.1\text{mV}$$

A similar reference supply was designed to provide the 2.5V reference. The

circuit is shown in Figure 5.13, and meets the specifications

(l) Reference voltage +2.5V ± 5mV

(ll) Load current 0 to 0.1mA

(lll) Input power supply +15V ± 4%

(lV) Ambient temperature 25°C.

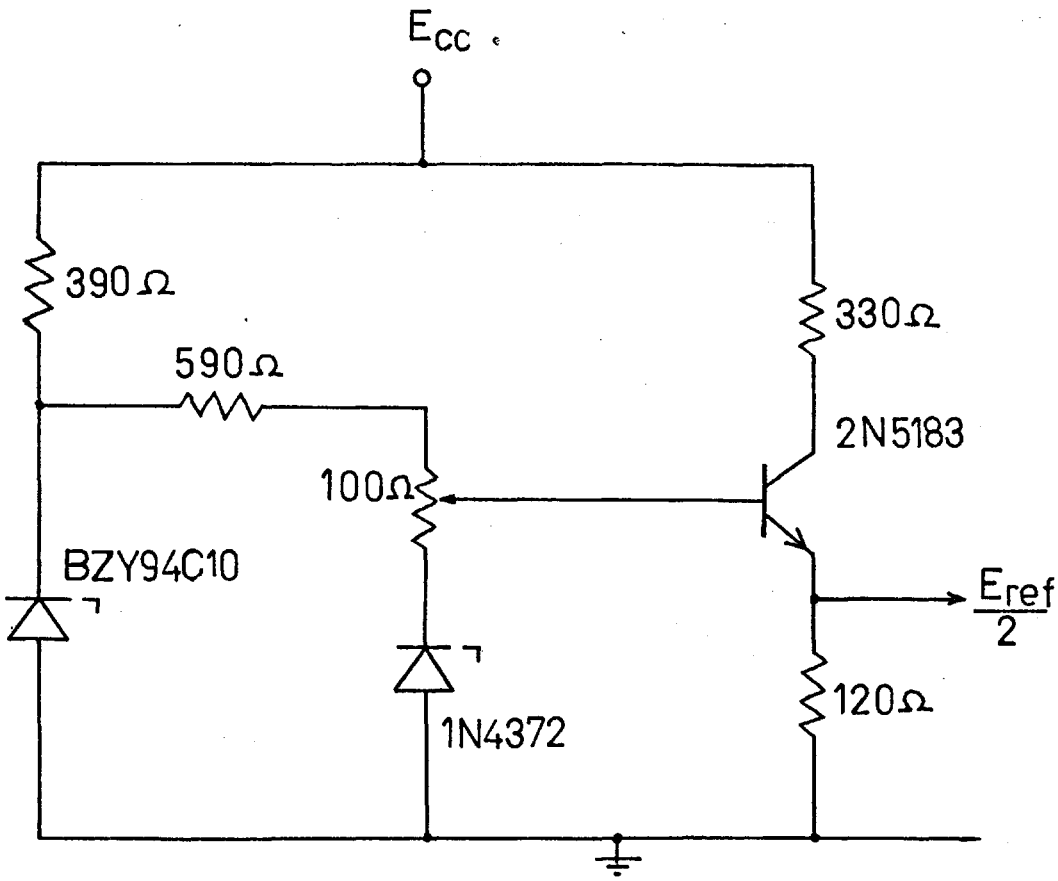


Fig. 5.13

2.5Volt Reference Supply

5.5 Comparator

The comparator used was a Texas Instruments SN72710N integrated circuit. The specification for this comparator is given in the appendix, and it is seen to have a maximum input of ± 5V and a maximum differential input of ± 5 volts. The comparator requires a power supply of +12V and -6 volts. This supply was derived from the ± 15V supply using the circuit shown in Figure 5.14.

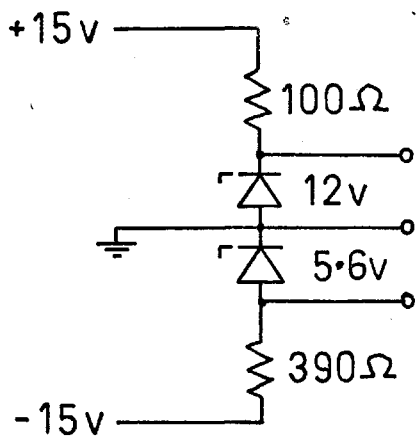


Fig. 5.14

Comparator Power Supply

5.6 Calibration Procedure

The following steps must be followed to calibrate the converter:

(l) Set E_{ref} to 5.000 volts

(ll) Set $\frac{E_{ref}}{2}$ to 2.500 volts

(lll) Remove the Bipolar Junction Transistor's (BJT's) from switches 2 and 5, thus closing switches 2 and 5.

Connect E_{in} to 0V and adjust the operational amplifier's null potentiometer for minimum output voltage.

(lV) Increase E_{in} to some voltage less than 2.5 volts and adjust the gain control potentiometer for a gain of two.

5.7 Results Using a μA741 Operational Amplifier

The specification of the μA741 integrated circuit operational amplifier is shown in the appendix, from which it is seen that the amplifier has a slew rate of 0.5V/μsec, and a short circuit output current of 25mA.

The maximum required output current supplied by equation (11) of section 3.2.1 is

$$i(a)_{max} = \frac{V_1}{a} C(1-e^{-\frac{a}{CR}})$$

$$= 2.4mA$$

this current has to be supplied at a voltage given by equation (14) of section 3.2.1

$$v(a) = \frac{V_1}{a} (a - CR + CR e^{-\frac{a}{CR}})$$

$$= 4.9 \text{ volts}$$

The amplifier is capable of delivering 2.4mamps at 4.9 volts; hence the speed of this system is limited by the slew rate and RC time constant.

The amplifier was calibrated following the procedure of section 5.6. The voltage waveform across C_1 was observed with a full scale analog input of 5 volts. An acquisition time of 14μsecs was observed; where acquisition time is defined as the time taken for the voltage to get within 1% of the input voltage for the last time.

The accuracy of the SSC converter was measured by slowly increasing the analog input voltage from 0 volts to 5 volts and recording the levels at which the binary output changes. A comparison of the theoretical quantizing limits to the

measured limits is shown in table 5.1. The results are obtained with a clock frequency of 20KHz.

Table 5.1

Converter Quantizing Errors Using a μA741 Operational Amplifier

Theoretical quantizing levels' limits volts	Quantizing level	Measured quantizing levels' limits volts	Error mV
0			
	0		
0.078		0.076	-2
	1		
0.156		0.157	+1
	2		
0.234		0.234	0
	3		
0.312		0.314	+2
	4		
0.391		0.391	0
	5		
0.469		0.472	+3
	6		
0.547		0.551	+4
	7		
0.625		0.630	+5
	8		
0.703		0.707	+4
	9		
0.781		0.785	+4
	10		
0.859		0.866	+5
	11		
0.937		0.942	+5
	12		
1.016		1.023	+7
	13		
1.094		1.101	+7

	14		
1.172		1.181	+9
	15		
1.250		1.255	+5
	16		
1.328		1.332	+4
	17		
1.406		1.412	+6
	18		
1.484		1.492	+8
	19		
1.562		1.570	+8
	20		
1.640		1.648	+8
	21		
1.719		1.730	+11
	22		
1.797		1.809	+12
	23		
1.875		1.885	+10
	24		
1.953		1.962	+9
	25		
2.031		2.041	+10
	26		
2.109		2.121	+12
	27		
2.188		2.201	+14
	28		
2.266		2.277	+11
	29		
2.344		2.357	+13
	30		
2.422		2.437	+15
	31		
2.500		2.500	0
	32		
2.578		2.576	-2
	33		
2.656		2.656	0
	34		
2.734		2.736	+2
	35		
2.813		2.815	+2

	36		
2.891		2.894	+3
	37		
2.969		2.973	+4
	38		
3.047		3.056	+9
	39		
3.125		3.129	+4
	40		
3.203		3.208	+5
	41		
3.281		3.287	+6
	42		
3.359		3.368	+9
	43		
3.438		3.446	+8
	44		
3.516		3.523	+7
	45		
3.594		3.604	+10
	46		
3.672		3.681	+9
	47		
3.750		3.761	+11
	48		
3.828		3.834	+6
	49		
3.906		3.914	+8
	50		
3.984		3.992	+8
	51		
4.063		4.071	+8
	52		
4.140		4.150	+10
	53		
4.219		4.228	+9
	54		
4.297		4.307	+10
	55		
4.375		4.386	+11
	56		
4.453		4.463	+10
	57		
4.531		4.540	+9

	58		
4.609		4.620	+11
	59		
4.688		4.700	+12
	60		
4.766		4.777	+11
	61		
4.844		4.856	+12
	62		
4.922		4.937	+15
	63		
5.000			

It can be seen from the table that the errors are within the range of -2 to +15m volts, i.e. within $\pm$ 0.3%. An accuracy of this figure indicates that 7 or 8 bits rather than 6 can be attained.

5.8 Results Using a Philbrick type QFT5 Operational Amplifier

The specification of the QFT5 is given in the appendix and from this it can be seen that the amplifier has a slew rate of 5V/μsec.

The maximum output current according to equation (11) of section 3.2.1 is

$$i(a)_{max} = \frac{V_1}{a} C(1-e^{-\frac{a}{CR}})$$

$$= 5 \times 10^6 \times 4,700 \times 10^{-12}(1-e^{-\frac{1}{.12}})$$

$$= 24\text{mA}$$

This current has to be supplied at a voltage given by equation (14) of section 3.2.1

$$v(a) = \frac{V_1}{a} (a - CR + CRe^{-\frac{a}{CR}})$$

$$= 4.4 \text{ volts}$$

The amplifier is capable of meeting these requirements, but it was observed that the acquisition time was reduced if a current booster (Analog Devices type B100)

was used as shown in Figure 5.15.

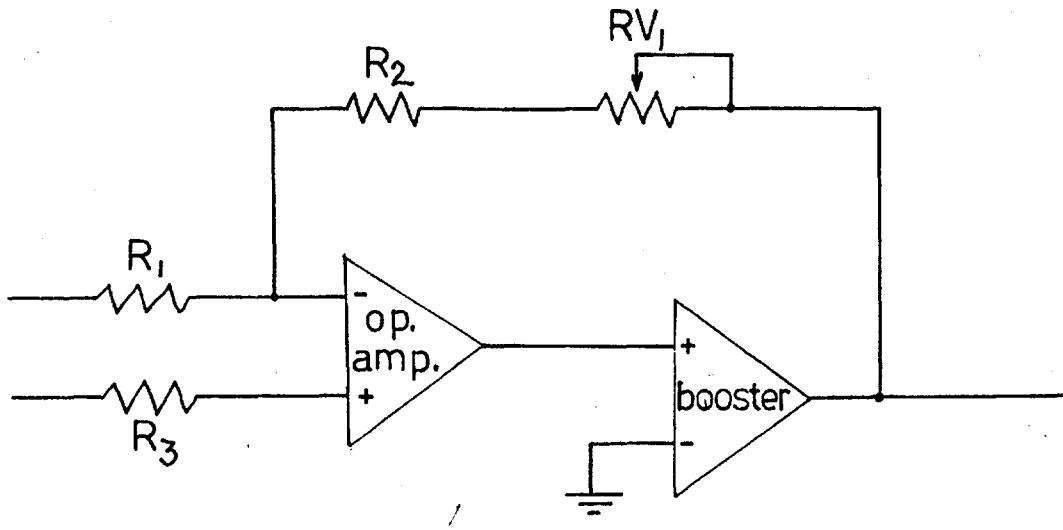


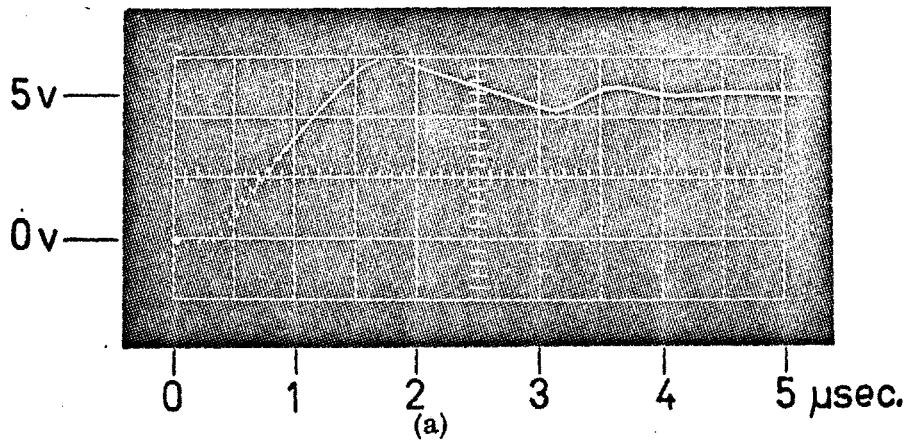
Fig. 5.15

Operation Amplifier with a Current Booster

The specification of the current booster is given inthe appendix. . This reduction in acquisition time is illustrated in Figure 5.16, which shows the waveform across C_1 for a 5 volt input. In (a) the current booster is not used and in (b) the current booster is used. This improvement results largely from a reduction in the time required to recover from the overshoot. The acquisition time from (b) is approximately 3.5μsec.

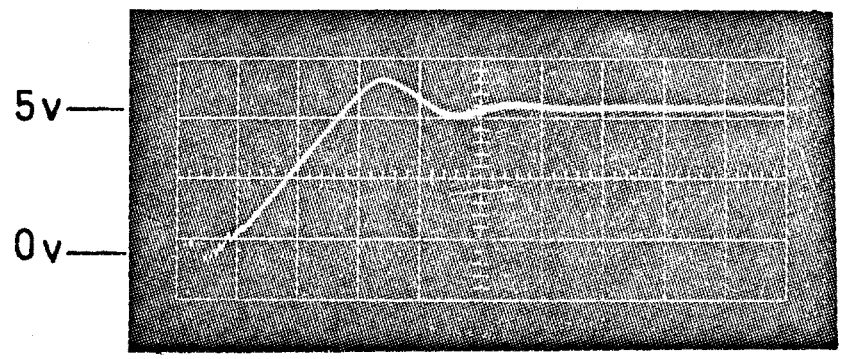
The ring counter was extended by two stages; thus obtaining an 8 bit converter. This utilizes the accuracy of the converter more efficiently.

The converter was calibrated in accordance with section 5.6, and the results recorded in table 5.2 were obtained, with a clock frequency of 200kHz.



(a)

Waveform without the current booster



(b)

Waveform with the current booster

Fig. 5.16

Waveforms across C_1 with a 5 volt input

Table 5.2

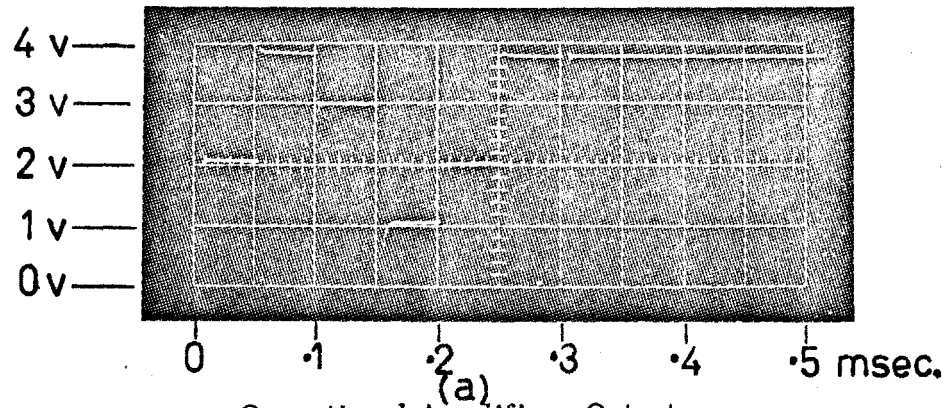
Converter Quantizing Errors Using a QFTS Operational Amplifier

Theoretical quantizing levels' limits volts	Quantizing level	Measured quantizing levels' limits volts	Error mV
O			
.078	4	.075	-3
.156	8	.155	-1
.234	12	.231	-3
.313	16	.307	-6
.391	20	.400	+9
.469	24	.470	+1
.547	28	.542	-5
.625	32	.623	-2
.703	36	.696	-7
.781	40	.776	-5
.859	44	.853	-6
.938	48	.936	-2
1.016	52	1.013	-3
1.094	56	1.038	-6
1.172	60	1.169	-3
1.250	64	1.246	-4
1.328	68	1.318	-10
1.406	72	1.396	-10
1.484	76	1.476	-8
1.563	80	1.557	-6
1.640	84	1.632	-8
1.719	88	1.711	-8
1.797	92	1.790	-7
1.875	96	1.870	-5
1.953	100	1.947	-6
2.031	104	2.022	-9
2.109	103	2.100	-9
2.188	112	2.184	-4
2.266	116	2.258	-8
2.344	120	2.336	-8
2.422	124	2.417	-5
2.500	128	2.494	-6
2.578	132	2.568	-10
2.656	136	2.646	-10

2.734	140	2.726	-8
2.813	144	2.808	-5
2.891	148	2.887	-4
2.969	152	2.962	-7
3.047	156	3.043	-4
3.125	160	3.122	-3
3.203	164	3.198	-5
3.281	168	3.275	-6
3.359	172	3.354	-4
3.438	176	3.436	-2
3.516	180	3.510	-6
3.594	184	3.588	-6
3.672	188	3.665	-7
3.750	192	3.750	0
3.828	196	3.827	-1
3.906	200	3.903	-3
3.984	204	3.982	-2
4.063	208	4.058	-5
4.140	212	4.130	-10
4.219	216	4.210	-9
4.297	220	4.291	-6
4.375	224	4.371	-4
4.453	228	4.338	-5
4.531	232	4.525	-6
4.609	236	4.602	-7
4.688	240	4.680	-8
4.766	244	4.760	-6
4.844	248	4.841	-3
4.922	252	4.915	-7
5.000			

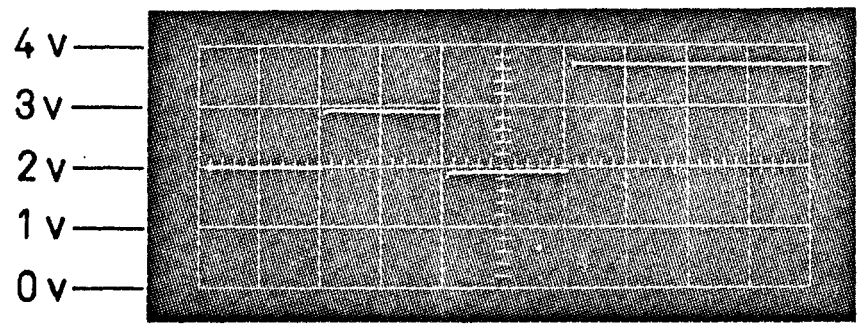
The system switches at the required voltages within ± 10mV, that is, the system has an accuracy of ± 0.2%.

Figure 5.17(a) is an oscilloscope photograph of the operational amplifiers output waveform for an analog input of 2 volts. Figures 5.17(b) and (c) show the waveforms across capacitors C_1 and C_2. It can be seen that the errors, discussed in section 5.4, due to switches closing before others open have been eliminated. It can also be seen that the voltage across the capacitors has not been appreciably effected by the input capacitance of the operational amplifier.



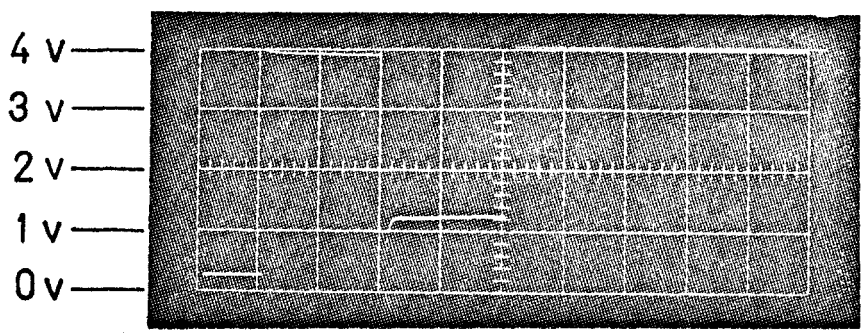
(a)

Operational Amplifiers Output



(b)

Voltage Across C_1



(c)

Fig. 5.17

Converter Waveforms for 2V Input

The clock frequency was increased and the converter operated up to a clock frequency of 350kHz. Figure 5.18(a) shows the amplifier's output at 300kHz for an input of 3 volts. The figure shows that the acquisition time is longest for the first clock pulse; hence if this first sample period could be increased the conversion rate could also be increased. This increased sample time was achieved by using the C/2 pulse to advance the ring counter, and by decreasing the number of stages in the ring counter from ten to six. This results in the timing diagram shown in Figure 5.19. With this timing arrangement the converter operated up to a clock frequency of 700kHz. Figure 5.18(b) shows the waveform with a 500kHz clock frequency for a 3 volt input.

A photograph of the SSC converter is shown in Figure 5.20.

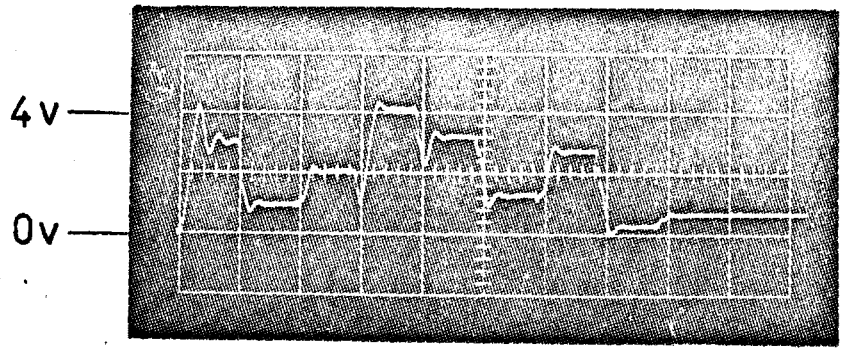
5.7 Converter Component Cost

A list of components and their prices is shown in table 5.3. The table shows that the total component cost is only $131.33 and that the two most expensive items are the current booster and the operational amplifier. It should be noted that this price does not include the clock.

5.8 Conclusions

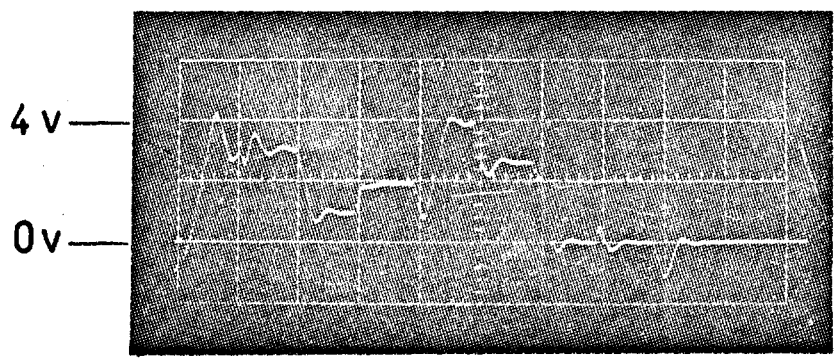
An eight bit SSC converter with an accuracy of $\pm$ 0.2% and a conversion time of 16μsec has been built for a component cost of less than $132. In production this cost could probably be reduced, especially as the converter appears suitable for fabrication as a large scale integration circuit. The cost of this converter compares favourably to other types of converters with similar specifications.

An SSC converter with higher accuracy and speed could be built using:-



(a)

Waveform at 300kHz Clock Frequency



(b)

Waveform at 500kHz Clock Frequency

Fig. 5.18

Waveforms at the Operational Amplifier's Output

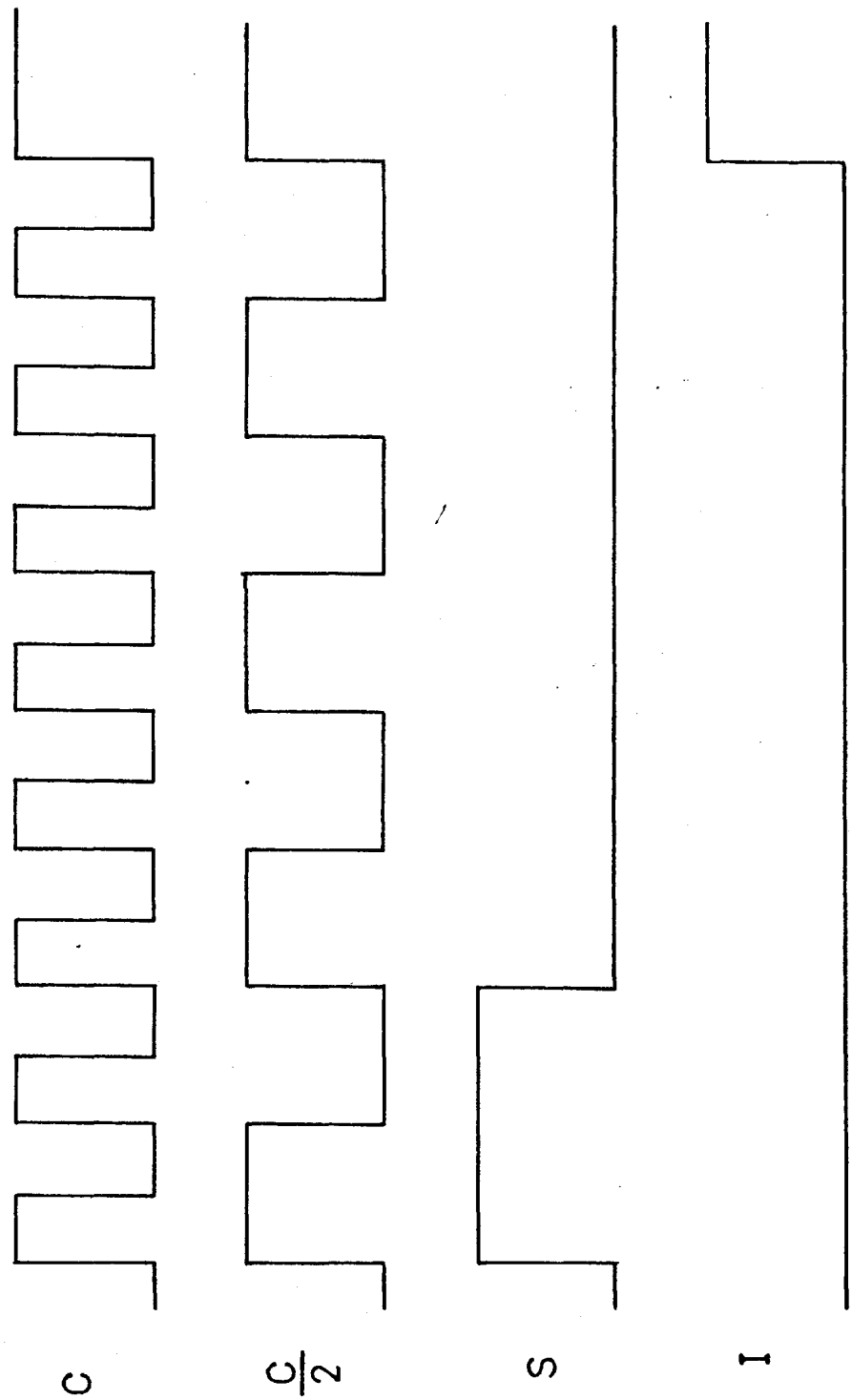


Fig. 5.19

Modified Timing Diagram

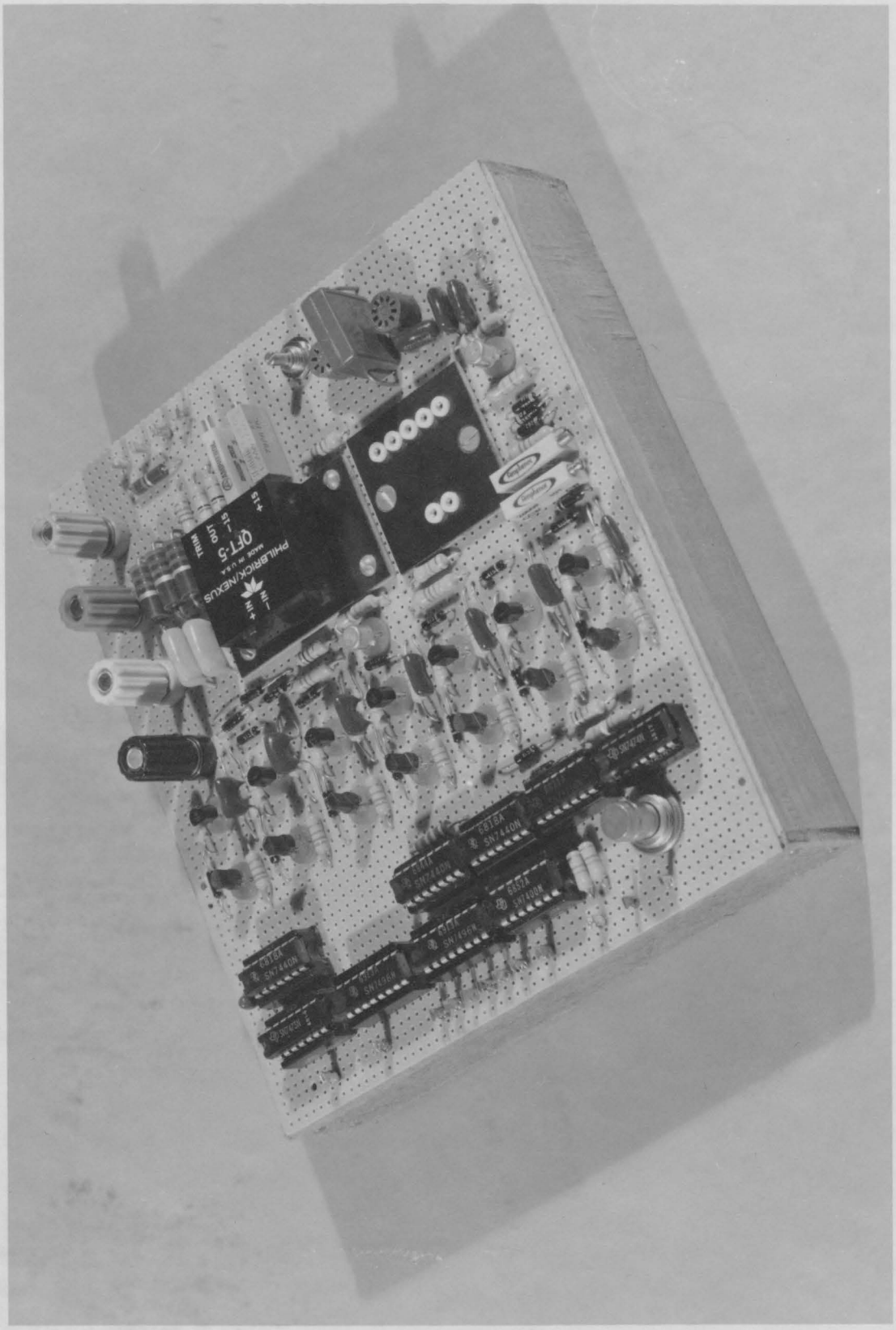


Fig. 5.20 The SSC Converter

Table 5.3

Converter Component Cost

Component type	Number Required	Price Per Item $	Price $
5W resistor	1	0.35	0.35
1/2W resistor	41	0.016	0.66
1% resistor	2	0.50	1.00
multiturn potentiometer	4	2.31	9.24
50pF cap.	7	0.20	1.40
4,700pF cap.	2	0.20	.40
1N3182	7	0.82	5.74
1N4372	1	1.44	1.44
1N752	2	1.20	2.40
BZY88C15	7	0.83	5.81
BZY94C10	2	0.83	1.66
BZY94C12	1	0.83	.83
BZY88C5V6	1	0.75	.75
BZY88C5V1	1	0.75	.75
2N5183	2	0.25	0.50
2N5028	7	0.90	3.60
T1S73	7	1.91	13.37
QFT5	1	20.00	20.00
B100	1	30.00	30.00
SN7440N	3	1.45	4.35
SN7473N	1	3.64	3.64
SN7496N	2	6.68	13.36
SN7400N	1	1.26	1.26
SN7474N	1	2.52	2.52
SN72710N	1	4.80	4.80
Pushbutton switch	1	1.50	1.50
		Total	$131.33

(l) A more accurate comparator

(ll) More stable reference voltages

(lll) Switching FET's with lower on resistance

(lV) An operational amplifier with a higher slew rate

The major advantages of the SSC converter are:-

(l) High performance to cost ratio

(ll) Inherent sample and hold function

(lll) Suitability for L.S.I.

(lV) High input impedance

(V) Little additional cost is involved to increase the number of bits.

The above advantages indicate that the SSC converter has a very promising future indeed, and that further research should be carried out in this field.

APPENDIX

PHILBRICK/NEXUS RESEARCH

A TELEDYNE COMPANY

Allied Drive at Route 128, Dedham, Mass. 02026

QFT-5

FIELD EFFECT TRANSISTOR INPUT

OPERATIONAL AMPLIFIER

SPECIAL FEATURES

- ±10V @ ±5mA GUARANTEED MINIMUM OUTPUT
- HIGH INPUT IMPEDANCES - TYPICALLY $10^{10}\Omega$ DIFFERENTIAL AND COMMON MODE
- 100,000 TYPICAL DC GAIN WITH FULL RATED LOAD
- GOOD SLEWING RATE - 5V/μs MINIMUM

GENERAL DESCRIPTION

NEXUS* type QFT-5 is a new low cost general purpose operational amplifier featuring field effect transistor inputs. This unit is constructed of silicon semiconductors and other selected parts to insure reliable operation over the temperature range of -25°C to +85°C. The QFT-5 typically provides 10^{10} ohms differential and common mode input impedances, and less than 1nA input bias current at 25°C.

PROTECTION

The input circuitry of this amplifier is fully protected against damage due to accidental connection of the input terminals across the power supply. The output circuitry is also protected against short term short circuits to ground and to either power supply terminal at 25°C.

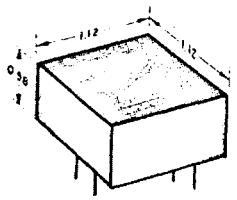
APPLICATIONS

The QFT-5 operational amplifier can be used in a wide variety of industrial and medical applications where cost is an important factor. For detailed applications assistance contact the NEXUS* Applications Engineering Department.

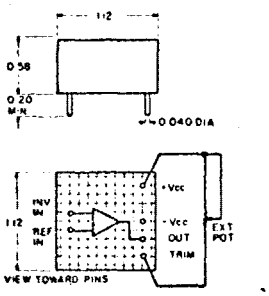
ABSOLUTE MAXIMUM RATINGS*

Storage Temperature	-55°C to +100°C
Operating Temperature	-25°C to +85°C
Supply Voltage	±18 Volts
Common Mode Input Voltage	±18 Volts
Differential Input Voltage	±30 Volts

*Absolute Maximum Ratings correspond to the maximum stresses to which the amplifier can be subjected without permanent damage. Conformance to the electrical specifications under these conditions is not guaranteed.



PACKAGE OUTLINE AND
BASE CONNECTION DIAGRAM



COMMON TERMINAL NOT BROUGHT OUT ON THIS AMP TYPE

Case Size	Pin Dia. (in.)	Grid Spacing (in.)	Weight (gm)	Volume (cu in.)	Mating Socket
08	040	1	30	73	NSK-7

P/N BULLETIN
QFT-5 Nov./67

PHILBRICK/NEXUS RESEARCH A TELEDYNE COMPANY
Allied Drive at Route 128 Dedham, Massachusetts 02026 (617) 329-1600

NEXUS TYPE QFT5

Electrical specifications @ 25°C and ±15 volt supply unless noted

CHARACTERISTICS	SYMBOL	TYPICAL	GUARANTEED	TEST CONDITIONS
RATED OUTPUT				
Usable Voltage Range	E_o	--	±12V (Min.)	R_{LL} = 10kΩ[1]
Usable Voltage Range	E_o	±11V	±10V (Min.)	R_{LL} = 2kΩ[1]
Maximum Current @ Full Output Voltage	I_o	±5.5mA	±5mA (Min.)	R_{LL} = 2kΩ[1]
Short Circuit to Ground (Short Term)	I_{ssg}	--	120mA (Max.)	R_{LL} = short
COMMON MODE				
Rejection Ratio @ dc	CMRR	72dB	60dB (Min.)	E_o = ±5V
Usable Input Voltage Range	E_{cm}	--	±6V (Min.)	-- -- --
OPEN LOOP GAIN	A_o	150,000	75,000 (Min.)	R_{LL} = 10kΩ[1]
	A_o	100,000	50,000 (Min.)	R_{LL} = 2kΩ (Full Load)[1]
FREQUENCY RESPONSE				
Small Signal Unity Gain Inverter	f_t	2.0MHz	1.7MHz (Min.)	R_i = 10kΩ; R_f = 10kΩ
Maximum Frequency for Full Output	f_p	--	100kHz (Min.)	R_i = 10kΩ; R_f = 10kΩ; R_{LL} = 2kΩ[1]
Slewing Rate, Full Load	SR	5.5V/μs	5V/μs (Min.)	R_i = 10kΩ; R_f = 10kΩ
Capacitive Loading w/out Causing Instability	C_L	no limit(μf)	--	R_i = 10kΩ; R_f = 10kΩ
Gain Margin	--	--	12dB (Min.)	R_i = 10kΩ; R_f = 10kΩ
Phase Margin	--	--	60° (Min.)	R_i = 10kΩ; R_f = 10kΩ
RECOVERY TIME FROM OVERDRIVE	τ_{OL}	--	125μs (Max.)	R_i = 10kΩ; R_f = ∞; E_{in} = ±3V
SETTLING TIME (to 0.1% of final value)	τ_s	10μs	--	R_i = 10kΩ; R_f = 10kΩ; E_{in} = ±10V
INPUT VOLTAGE OFFSET				
Temperature Coefficient	TCE_{os}	50μV/°C	300μV/°C (Max.)	-25°C to +85°C
vs. Power Supply	--	--	800μV/V (Max.)	±14V < V_{cc} < ±16V
vs. Common Mode	--	--	800μV/V (Max.)	E_{cm} = ±6V
EXTERNAL OFFSET VOLTAGE TRIM POTENTIOMETER	R_{os}	2.5kΩ	--	-- -- --
INPUT BIAS CURRENT[2]				
Either Input @ 25°C	I_{bias}	--	1nA (Max.)	R_{test} = 1MΩ
Temperature Coefficient	TCI_{bias}	--	0.4nA/°C (Max.)	-25°C to +85°C
vs. Power Supply	--	--	50pA/V (Max.)	±14V < V_{cc} < ±16V
vs. Common Mode	--	--	100pA/V (Max.)	E_{cm} = ±6V
INPUT DIFFERENCE CURRENT	I_{diff}	--	500pA (Max.)	R_{test} = 1MΩ
WIDEBAND INPUT NOISE VOLTAGE	e_n	30μVrms	50μVrms (Max.)	R_i = 100Ω; R_f = 10kΩ; BW=20kHz
INPUT IMPEDANCE				
Differential	Z_d	10^{12}Ω	10^9Ω (Min.)	Test Frequency = dc
Common Mode	Z_{cm}	10^{12}Ω	10^9Ω (Min.)	Test Frequency = dc
OUTPUT IMPEDANCE				
Open Loop	Z_o	5,000Ω	10,000Ω (Max.)	Test Frequency = 10Hz
POWER REQUIREMENTS				
Current, Quiescent	I_{cc}	--	10mA (Max.)	-- -- --
Current, Full Output	I_{cc}	--	15mA (Max.)	R_{LL} = 2kΩ[1]

(1) R_{LL} is the parallel combination of feedback resistor R_f and external load resistance R_L.

(2) Input Bias Current (I_{bias}) was formerly called Input Offset Current (I_{os}). The change in terminology is for the purpose of conforming to recent (but unofficial) conventional usage.

FAIRCHILD LINEAR INTEGRATED CIRCUITS μA741C

FEATURES:

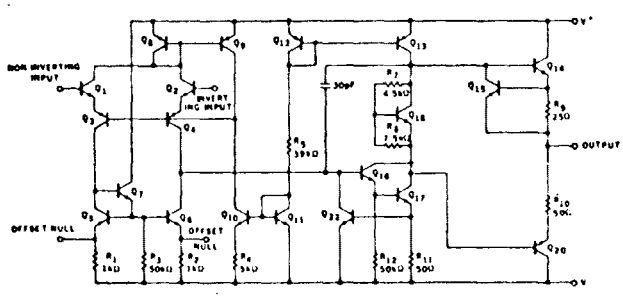
- NO FREQUENCY COMPENSATION REQUIRED
- SHORT-CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP

GENERAL DESCRIPTION — The μA741C is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the μA741C ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA741C is short-circuit protected, has the same pin configuration as the popular μA709C operational amplifier, but requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications. For full temperature range operation (−55°C to +125°C) see μA741 data sheet.

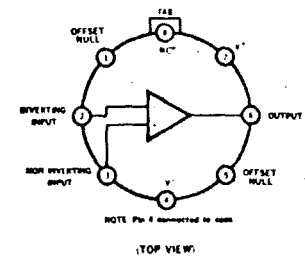
ABSOLUTE MAXIMUM RATINGS

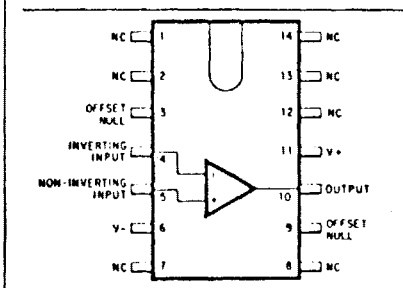
Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage between Offset Null and V−	±0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS





NOTES:

(1) Rating applies for ambient temperatures to + 70°C.

(2) For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

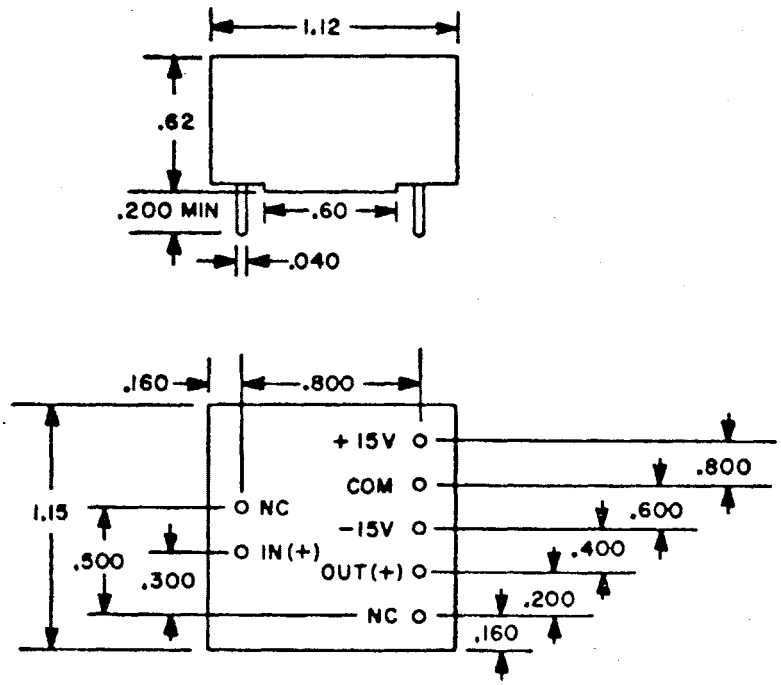
(3) Short circuit may be to ground or either supply.

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			±15		mV
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	20,000	200,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2$ kΩ		0.5		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage				7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15,000			
Output Voltage Swing	$R_L \geq 2$ kΩ	±10	±13		V

ANALOG DEVICES
MODEL 100
CURRENT BOOSTER

OUTLINE DIMENSIONS



ELECTRICAL SPECIFICATION

1. GAIN: 0.9 V/V MIN. 50 M.A. LOAD, 0.85 V/V MIN. 100 M.A. LOAD.
2. OUTPUT VOLTAGE: ± 10 V MIN.
3. OUTPUT CURRENT: ± 100 M.A.
4. FREQUENCY FOR FULL OUTPUT: 1 M.C. MIN.
5. INPUT VOLTAGE OFFSET: 25 °C, 200 M.V. MAX.
6. AVERAGE VOLTAGE DRIFT (-25 °C TO +85 °C): 2.5 MV/°C
7. INPUT CURRENT OFFSET 25 °C: 500 μA MAX.
8. INPUT IMPEDANCE: 9K MIN.
9. POWER SUPPLY REQUIRED: ± (15 TO 16V) AT 100 M.A.
10. TEMPERATURE RANGE: -25 °C TO 85 °C.
11. TEMPERATURE RANGE, STORAGE: -55 °C TO 85 °C.

TYPES SN72 710, SN72 710L, SN72 710N
DIFFERENTIAL COMPARATORS

absolute maximum ratings

Supply Voltages (See Note 1): V_{CC1}	14 V
V_{CC2}	-7 V
Differential Input Voltage (See Note 2)	±5 V
Input Voltage (Either Input, See Note 1)	±7 V
Peak Output Current	10 mA
Continuous Total Power Dissipation: SN72 710 and SN72 710L	200 mW
SN72 710N	300 mW
Operating Free-Air Temperature Range	0°C to 70°C
Storage Temperature Range: SN72 710 and SN72 710L	-65°C to 150°C
SN72 710N	-55°C to 150°C

NOTES: 1. These voltage values are with respect to network ground.
2. These voltage values are with respect to the other input.

electrical characteristics (unless otherwise noted V_{CC1} = 12 V, V_{CC2} = -6 V, T_A = 25°C)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DI}	Differential-input offset voltage	$R_S \leq 200\ \Omega$, T_A = 0°C to 70°C			10	mV
		V_{out} = 1.4 V, $R_S \leq 200\ \Omega$		2	7.5	mV
α_{VDI}	Differential-input offset voltage temperature coefficient (See Note 7)	T_A = 0°C to 70°C		7.5		μV/deg
I_{DI}	Differential-input offset current (See Note 7)	T_A = 0°C to 70°C			25	μA
		V_{out} = 1.4 V		1	15	μA
I_{in}	Input current	T_A = 0°C to 70°C			150	μA
				25	100	μA
V_{in}	Maximum input voltage range (See Note 1)	V_{CC2} = -7 V	±5			V
$V_{in\ D}$	Differential-input voltage range (See Note 2)		±5			V
A_V	Voltage gain	T_A = 0°C to 70°C	500			
			700	1200		
$V_{out(1)}$	Logical 1 level output voltage	$V_{in\ D} \geq 15$ mV, $I_{load} \leq -0.5$ mA	2.5	3.5	4	V
$V_{out(0)}$	Logical 0 level output voltage	$V_{in\ D} \geq 15$ mV, $I_{sink} \leq 1.6$ mA	-1	-0.5	0	V
r_{out}	Output resistance			200		Ω
P_T	Total power dissipation			110		mW

NOTE: 7. Specified for the following output voltage levels: when T_A = 0°C V_{out} = 1.5 V, when T_A = 25°C V_{out} = 1.4 V, and when T_A = 70°C V_{out} = 1.2 V. These output voltage levels were selected as they fall within the logic threshold voltage ranges normally found in digital integrated logic circuits.

switching characteristics, V_{CC1} = 12 V, V_{CC2} = -6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time (See Note 6)	V_{in} = 100 mV		40		ns

NOTE: 6. The interval of time between application of a 100 mV input step function and the time when the output crosses the logic threshold voltage. For testing purposes, conditions are established at the differential-input terminals whereby an input step function from 100 mV to 0 will cause the output voltage to rise just to the selected threshold voltage of 1.4 V. Conditions on the input used as a reference are then adjusted to cause the 100 mV input to drive 5 mV beyond the previously established conditions and the response time is measured.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS 22, TEXAS

SOLID CIRCUIT® SEMICONDUCTOR NETWORKS†

TYPES SN52 710, SN52 710L, SN52 710N, SN72 710, SN72 710L, SN72 710N DIFFERENTIAL COMPARATORS

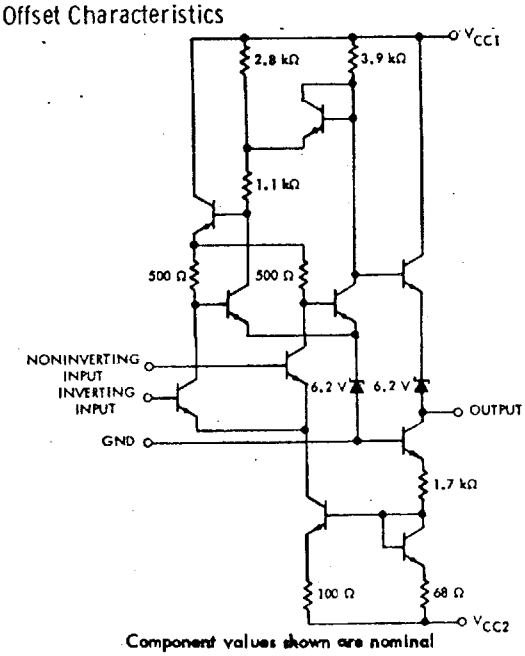
DIFFERENTIAL VOLTAGE COMPARATORS
featuring

- Fast Response Times
- Low Offset Characteristics

description

The SN52 710 circuit is a high-speed comparator with differential inputs and a low impedance output. Component matching, inherent with silicon monolithic circuit fabrication techniques, produces a comparator circuit with low drift and offset characteristics. This circuit is particularly attractive for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed voltage comparator. The SN52 710, SN52 710L and SN52 710N are characterized for operation over the temperature range of −55°C to 125°C. The SN72 710, SN72 710L and SN72 710N are characterized for operation from 0°C to 70°C.

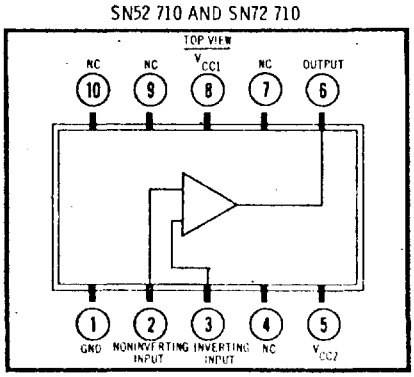
Texas Instruments Series 52/72 catalog lines of linear integrated circuits offer higher reliability, lower cost, smaller size, and less weight than equivalent discrete component circuits.



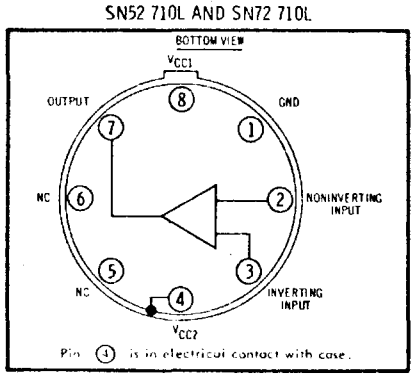
Component values shown are nominal
SCHEMATIC DIAGRAM

TERMINAL ASSIGNMENTS

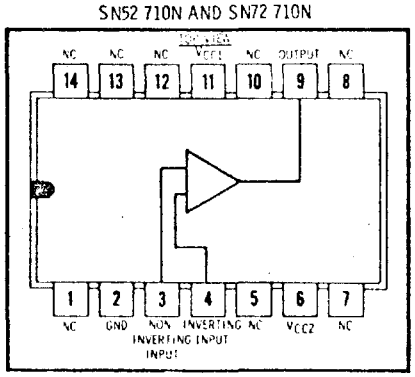
SN52 710 AND SN72 710



SN52 710L AND SN72 710L



SN52 710N AND SN72 710N



NC — No internal connection.
† Patented by Texas Instruments

SC10320
JULY 1967
REPLACES SC9421A FEBRUARY 1967

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