SOLAR CELLS FROM UNPOLISHED SILICON WAFERS

SOLAR CELLS
FROM
UNPOLISHED SILICON WAFERS

On Campus Project

by

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ABSTRACT

Solar cells were made by diffusing impurities into the rough or backside of commercially available silicon wafers to form a junction. The properties of these solar cells were compared to solar cells made by diffusing impurities into the polished surface of similar silicon wafers. The processing steps involved in preparing each type of solar cell were identical.

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INTRODUCTION

The polishing of one surface of a silicon wafer is a portion of the expense in the production of the wafer. This expense is reflected in the cost per kilowatt of power for solar cells made from this type of wafer. If solar cells can be made from unpolished wafers with conversion efficiencies close to those made from polished wafers, the cost per kilowatt of power can be lowered by an amount equal to the total expense of polishing one surface of each wafer.

The development of a processing routine which would generate solar cells with reasonable conversion efficiencies and its application to the two types of solar cells was the objective of this project.

DESIGN CONSIDERATIONS

Doping of silicon wafers is normally achieved by diffusing impurities into the wafer from an oxide deposited on the wafer in a gaseous atmosphere containing the doping impurities. Rather than using this technique to dope a wafer a few drops of a solution[1] were placed on the wafer and the wafer was spun on a photoresist spinner. This solution leaves an adherent uniform film on a clean wafer surface after the solvent is driven out. The speed at which the wafer is spun[2] determines the thickness of the film and the build-up of solution on the outer rim of the wafer. The film contains impurities which diffuse into the wafer at high temperatures to dope the wafer.

Three vials of solutions containing phosphorus as the doping impurity and three vials of solutions containing boron as the doping impurity were obtained. In each case the phosphorus containing solutions formed uniform films. The first vial of boron containing solution formed non uniform films. From the center of rotation streaks formed in the film giving the impression there were particles in the solution which moved out towards the rim of the wafer when it was spun leaving streaks in the film. Diodes made using this boron solution as the doping source exhibited a large current leakage in the forward as well as reverse

direction. Staining[3] of the wafer in a dilute solution of hydroflouric acid containing copper nitrate and viewing under a microscope revealed streaks on the wafer surface indicating the wafer was nonuniformly doped. Filtering and centrifuging of the solution was used to try to remove the particles from the solution but was ineffective. A second vial of solution containing boron was obtained which formed a uniform film of different composition. After diffusion this film would not dissolve in dilute hydrofloric acid. It was found that if the wafer was boiled for 10 minutes in a solution of sulfuric acid and hydrogen peroxide the film would come off in pieces in dilute hydrofloric acid but would remain undissolved. A third type of boron doping source was obtained. It came as two separate solutions which were mixed together in equal parts to obtain a solution which is spun on the wafer. This solution yielded uniform films with properties identical to those of the second vial obtained.

The uniform films indicated that these spin on films could be used to generate uniformly doped layers on wafers of one inch diameter. These one inch diameter wafers were used for the production of solar cells.

In the early days[4] of silicon solar cell technology it was felt that p diffused n substrate solar cells were more efficient than n diffused p substrate solar cells. It

was later discovered that n on p substrate solar cells were more resistant against the damaging radiation which was encountered on space flights. Research has therefore in the later years concentrated on optimizing the efficiency of the n diffused p substrate solar cell.

The bad experience with the first vial of boron doping solution along with the more abundance of literature on the n on p substrate solar cell prompted an non p substrate structure to be choosen for the solar cells produced.

The starting point for making a silicon solar cell is naturally the wafer from which it is made. The short circuit current and the open circuit voltage of the solar cell are dependent on the resistivity of the wafer. The open circuit voltage of the solar cell theoretically increases as the resistivity of the wafer decreases due to the decrease of the reverse saturation current of the diode. The short circuit current decreases with decreasing resistivity of the wafer due to the decrease of minority carrier lifetime. The open circuit voltage is optimized by using low resistivity wafers and short circuit current is optimized by using high resistivity wafers. The parameter which is of interest is the maximum power obtainable from the solar cell. The maximum power is also dependent on the resistivity of the starting wafer. A solar cell with optimal short circuit current or optimal open circuit voltage has to be traded off to optimize

the maximum power output of the solar cell. The resistivity which optimizes the maximum power output is a resistivity of approximately 1 ohm-cm[4].

Wafers with a resistivity close to 1 ohm-cm were therefore choosen for the starting material for the solar cells which were produced.

The next process is the diffusion of impurities into the wafer to form a junction within the wafer. The short circuit current of the solar cell is dependent on the depth of the junction from the surface. A parameter which is easily measured and is dependent on the junction depth is the sheet resistivity of the layer which is diffused into the wafer. The sheet resistivity decreases for increasing depths of diffusion. For a 10 ohm-cm wafer it is reported[5] that the short circuit current increases for increasing sheet resistivity up to about 100 ohms/square and for sheet resistivities greater than 100 ohms/square the short circuit current remains approximately constant.

It would be expected that a similar sort of short circuit current dependence on the sheet resistivity would apply for wafers of 1 ohm-cm[4]. A sheet resistivity of 80 ohms/square was measured for a diffusion at 900°C for a time of 1 hour. It was decided that the short circuit current was close to its optimal value for a sheet resistivity of 80 ohms/square so the time and temperature of diffusion

choosen for the production of solar cells was 1 hour of 900°C.

A diffusion of impurities into the back of the wafer to form a highly doped layer of the same polarity as the wafer creates an electric field which increases the open circuit voltage of the solar cell. The highly doped layer is also much easier to make a low resistance contact[6] to than the 1 ohm-cm wafer.

A highly doped layer on the backside of the wafers was obtained by spinning a phosphorus containing film on the front side and then a boron containing film on the backside of the wafer. Boron and phosphorus diffuse at about the same rate into silicon. When the wafer is placed into a diffusion furnace the phosphorus diffuses into the front forming an n type layer and at the same time boron is diffusing into the back of the wafer forming a similar p type layer. The desired structure is obtained with a single diffusion.

Around the rim of the wafer the phosphorus doped layer on the front and the boron doped layer on the back meet each other. A large current can leak around the junction through the region where these two heavily doped layers meet. This leakage can be made insignificantly small compared to the current generated by the solar cell by completely masking the wafer except for a narrow anulus around the rim and etching through the diffused layers. This isolates the two diffused layers from each other. Care has to be taken after etching the silicon to prevent the etched surface from

becoming contaminated which can cause large currents to leak around the junction.

A model of an ideal solar cell is a current generator shunted by a forward biased real diode. By a real diode is meant a diode with the current voltage characteristics of the unilluminated solar cell. A real solar cell could be modeled as some grid of ideal solar cells coupled parallely with each other by a resistive network. The resistive network models the resistance seen by the current as it flows parallel to the wafer surface to the point of collection. When the solar cell is loaded current flows from each of the ideal solar cells through the resistive coupling network and into the load. The flow of current through a resistor implies there is a potential difference across the resistor. This means that there are variations in the potential differences across the ideal solar cells in the grid. The current flowing through the shunting diode of each ideal solar cell changes significantly for a few tens of millivolt change in voltage. When some of the ideal solar cells are delivering their maximum power others in the grid may only be delivering a small fraction of their maximum power depending on the size of the potential difference variations. The ideal maximum power obtainable from the solar cell is the sum of the maximum powers of each ideal solar cell in the grid. The real maximum power is determined from the sum of the curves with staggered peaks representing the power output

of each ideal solar cell as a function of the voltage at the terminals of the real solar cell. This maximum power is clearly less than the ideal maximum power.

To obtain the maximum power from the solar cell any voltage variations on the wafers surface have to be minimal. Voltage variations on the back of the wafer can be reduced by completly coating the back with a metal that makes a good electrical connection to the silicon and is much more conductive than the silicon. The front surface is harder to deal with. Any metal placed on the surface leaves a shadow under it which decreases the output power of the solar cell. The metal is deposited as a series of narrow straight parallel fingers joined together. The number and size of the fingers are choosen to optimize the output power. The current densities in these fingers can become quite large so there can be a large potential variation along the finger. This can be reduced by increasing the cross sectional area of the finger to reduce the current density.

The metal choosen to deposit on the silicon was aluminum. Aluminum makes a good electrical connection to highly doped n and p silicon[6] and it adheres well to the silicon. It was deposited by evaparation from a tungstun basket in a vacuum of about 10^{-6} torr. The finger structure on the front was defined by placing a sheet of brass with the finger pattern etched out, against the wafer during the evaporation.

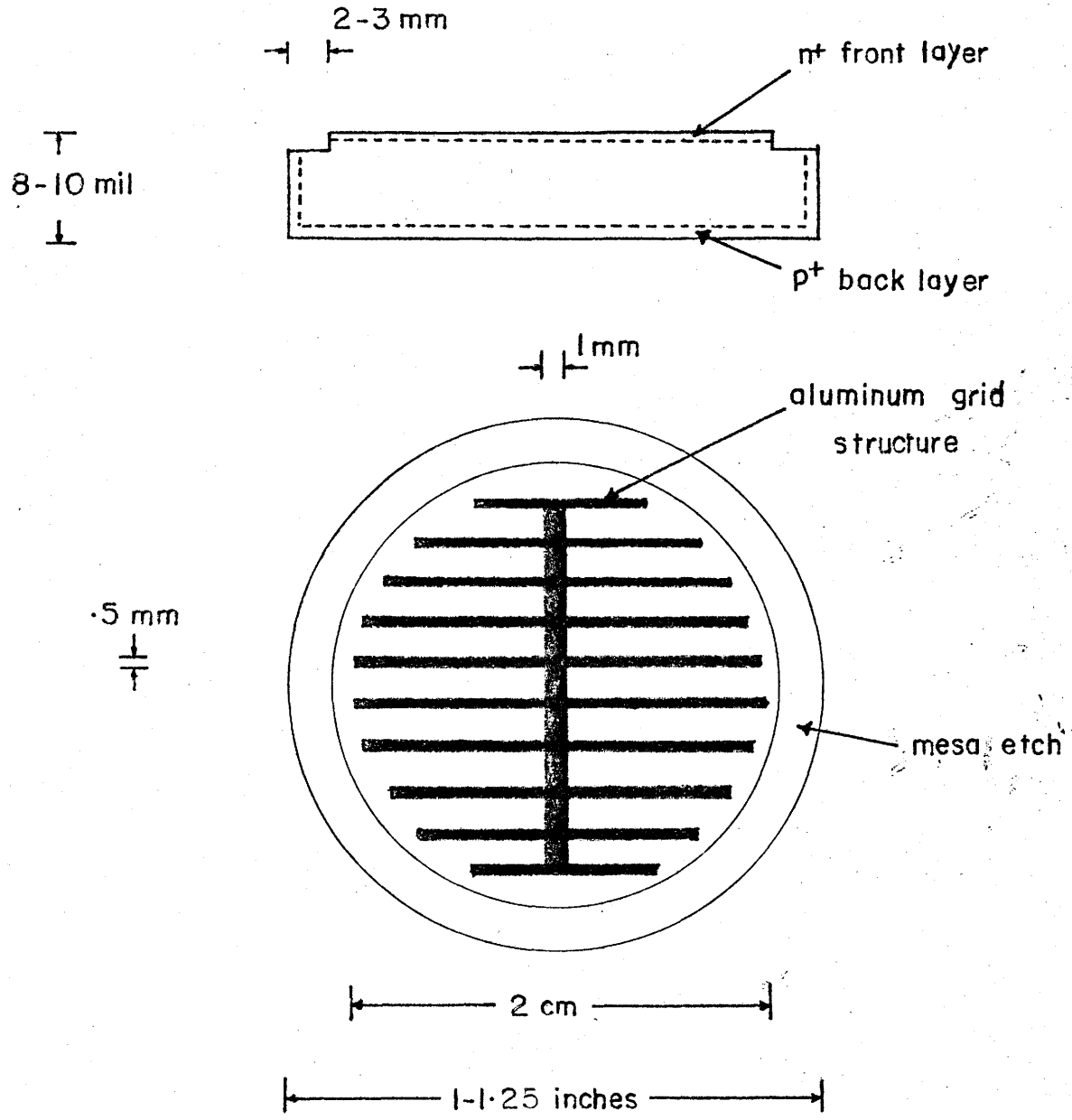

Figure 1 Diagram of Solar Cell Structure

PREPARATION OF THE SOLAR CELLS

In this section the procedure for processing of the wafer into a solar cell is given. A considerable amount of trial and error has to be gone through in order to obtain a procedure which will give good and consistent results. Most of the trial and error part will be left out and only the final acceptable procedure will be presented.

The wafer has to be cleaned to remove any organic material like grease or dust particles and any metallic atoms absorbed on the surface. These materials may diffuse into the wafer when placed in a diffusion furnace. These materials in the bulk of the wafer may lower the quality of the wafer by decreasing the lifetime of carriers.

To remove grease and dust particles the wafer is boiled for about 15 minutes in solution of 1:2:1 distilled water, sulfuric acid and hydrogen peroxide. Without the distilled water the wafer floats on top of the solution not properly cleaning the surface out of the solution. After the boil the solution is completely decanted because there is a violent exothermic reaction if the solution is diluted with water. The wafer is immediately rinsed 7 or 8 times with distilled water to remove all traces of the solution. After each rinse enough wafer is left in the beaker to prevent the exposure of the wafer to the atmosphere from which impurities may be picked up again.

The wafer is then etched in a dilute solution of hydrofloric acid for about a minute to remove the oxide from the surface. This solution is diluted and the wafer rinsed as in the previous step.

To remove absorbed metallic atoms and to grow a thin oxide the wafer is boiled for about 15 minutes in a solution of 4:1:1 distilled water, hydrochloric acid and hydrogen peroxide. The solution is then diluted and the wafer rinsed as before. The oxide serves to protect the surface from becoming contaminated in later processing steps. A silicon surface tends to oxidize in the atmosphere from which impurities can be absorbed. The growth of a thin oxide in the clean environment of the beaker prior to exposure to the atmosphere ensures the oxide is clean.

The tweezers used in handling the wafer during processing are cleaned while the wafer is cleaned by etching in aqua regia and rinsing with distilled water.

The eyedroper used for applying the doping solution is cleaned at the same time by etching in dilute hydroflouric acid and then rinsing with acetone to remove all traces of water.

After cleaning the wafer is removed from the beaker with the tweezers and blown dry with nitrogen. The wafer is immediately placed on a photoresist spinner vacuum chuck with the intended n type surface facing upwards and 2 or 3 drops of phosphorus doping solution is placed on the surface with

the eyedroper. The chuck is then spun at 3000 rpm for one minute. A uniform film is formed except for a ring at the outer edge and occasionally there are a few dust particles on the surface which distorts the film around the particle. These particles don't appear to severely degrade the quality of the diode; however, they can't improve it so the time from cleaning to spinning the film on should be as short as possible to minimuze the number of the dust particles accumulated on the surface. The wafer is then placed in an oven at about 150 ^{0}C for 10 minutes to drive the solvent from the film. After this heat treatment the wafer is returned to the vacuum chuck of the photoresist spinner, this time with the opposite surface facing upwards. A boron containing film is spun on the surface and the wafer is put through the same heat treatment as in the previous case.

The wafer is now ready for diffusion. The wafer is placed into a furnace at a temperature of 900^{o}C for a time of one hour to diffuse the impurities into the wafer. Nitrogen is flowed through the furnace before the diffusion to purge the furnace and also during the diffusion. The nitrogen atmosphere prevents the oxidation of the wafer surface which masks against the diffusion of the impurities into the wafer. After the diffusion the wafer is slowly removed from the furnace to allow it to gradually cool to room temperature.

The films have to be stripped from the wafer surface.

The manufacturer of the doping solutions claims that an immersion in a dilute solution of Hydrofloric acid will dissolve the films, this technique removed the phosphorus doping film satisfactory but the boron doping film would not dissolve. Several other techniques were unsuccessfully tried. It was found that if the wafer was boiled for 10 minutes in a solution of 2:1 sulfuric acid and hydrogen peroxide and then rinsed prior to the etch in dilute hydrofloric acid; the boron doping film would come off in little pieces and remain undissolved in the solution. This leaves the surface clean and free from any traces of the doping films. To protect the surfaces from the atmosphere a thin oxide is grown by boiling for 10 minutes in a solution of 4:1:1 distilled water, hydrochloric acid and hydrogen peroxide. If the surface becomes contaminated the voltage current characteristics of the diode can appear much degraded from those of a diode with a clean surface. The wafer is rinsed with distilled water then it is removed from the beaker with tweezers and blown dry with nitrogen.

The wafer is now ready for metalization. The wafer is placed in a vacuum coater and aluminum is evaporated from a tungstun basket at a pressure of about 10^{-6} torr. The front finger pattern is defined by evaporation through a brass mask with the finger pattern etched out. The back surface is completely coated with aluminum. The aluminum is only making contact with the surface of the thin oxide on the

wafer surface. There is a large resistance between the silicon and the aluminum. To reduce this resistance the wafer is placed into a furnace with a nitrogen atmosphere at about 400° C for 10 minutes. This causes the aluminum to diffuse through the thin silicon oxide and slightly into the silicon. This substantially decreases the electrical resistance between the silicon and aluminum. If the temperature or time of the anneal is too large the aluminum diffuses right through the previously diffused layers causing the diode to short out. The nitrogen atmosphere prevents the oxidation of the aluminum which makes it difficult to make a good connection to when the solar cell is tested. If this connection is poor the voltage current characteristics of the solar all can falsely appear degraded.

A mesa is now etched to isolate the front and back diffused layers. The wafer is completely masked on the backside and all but a narrow annulus on the outer edge of the front surface with black wax dissolved in tricholoroethylene or chloroform. The wax is applied by dabbing it on with a Q-tip. After the wax has hardened the wafer is placed in a solution of 8:5:1 nitric acid; acetic acid and hydrofloric acid. This solution etches the silicon on the exposed annulus. About one minute is sufficient to etch through the diffused layer, isolating the back and front diffused layers from each other. After this time the solution is diluted and the wafer is rinsed 7 or 8 times with

distilled water. Enough water is left in the beaker after each rinse to keep the wafer submerged. Nitric acid is added to the water in the beaker after the final rinse and left for about two minutes. Thus grows an oxide on the freshly etched surface of the annulus. This ensures that the oxide which would inevitably form there is relatively clean. There is some current which leaks through this etched region but it is very small compared to the short circuit current of the solar cell. The solution is then diluted and the wafer rinsed as before. After the final rinse the water is completely decanted and the wafer is rinsed with methanal to remove any water remaining on the wafer. The black wax is completely removed by dissolving it with trichloroethylene or chloroform. The wafer is removed from the beaker with tweezers and is blown dry with nitrogen.

This completes the processing of the wafer into a solar cell and now it is ready to be tested and its performance evaluated. A flow chart of processing steps is illustrated in Figure 2.

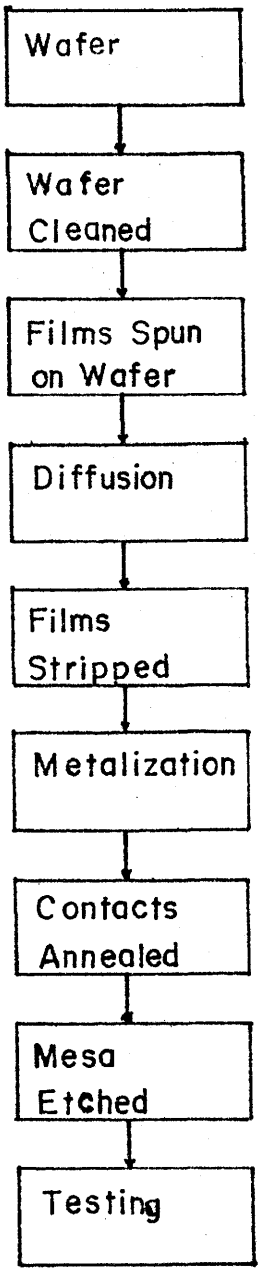

Figure 2 Processing Flowchart

TESTING PROCEDURE

The solar cell could be tested outside in the natural sunlight. A pyranometer or standard solar cell is used to measure the intensity of the incident sunlight in order to determine the conversion efficiency of the solar cell being tested. The efficiency of a solar cell is dependent on the intensity and spectral distribution of the sunlight which varies with atmospheric conditions and the position of the sun in the sky. This method of testing therefore is not in general very reproducible and does not give an accurate comparison of solar cells tested at different times.

To eliminate this problem sunlight was simulated in the laboratory with Sylvania type ELK 300 watt tungsten halogen quartz projector lamp bulbs. The intensity of light falling on the test plane is varied by varying the distance between the lamps and the test plane. An internationally accepted intensity can be obtained with a standard cell tested by Nasa Lewis. When the standard cell is placed in the test plane and the intensity of light adjusted until the voltage current characteristics of the standard cell coincide with those obtained by Nasa Lewis the intensity and spectral distribution of light is similar to what was used by Nasa Lewis. This insures that all the cells tested here are tested under the same conditions of illumination regardless when they were tested. It also allows an accurate comparison between solar cells made and tested here and solar

cells tested at laboratories using the Nasa Lewis standard.

The system used to obtain the voltage current characteristics was assembled from Hewlet Packard components and a high current operational amplifier. The core of the system was a HP9820A calculator which could be programed to send and receive information from a HP6131B Digital voltage source and a HP3490A multimeter through a HP2570A coupler controller. A HP9862A calculator plotter was connected to the calculator on which the current voltage characteristics could be plotted. Figure 3 is a diagram of the system.

The high gain of the operational amplifier and negative feedback through the solar cell causes the voltage at the non inverting and inverting terminals with respect to ground to be the same. The inverting terminal of the operational amplifier has a high input impedence therefore the current flowing through the solar cell is the same as that through the resistor R which is V^1/R. By using a precision resistor for R of the correct size the current flowing through the solar cell can accurately be controlled by V^1. By varying V^1 between 0 and 10 volts a resistor of 100 ohm will allow the current to vary from 0 to 100 milliamperes. The voltage across the solar cell is read by the multimeter. The calculator can control the voltage output of the digital voltage source and can receive the voltage across the solar cell from the multimeter. Starting with V^1 at zero the open circuit voltage of the solar cell is read and printed out

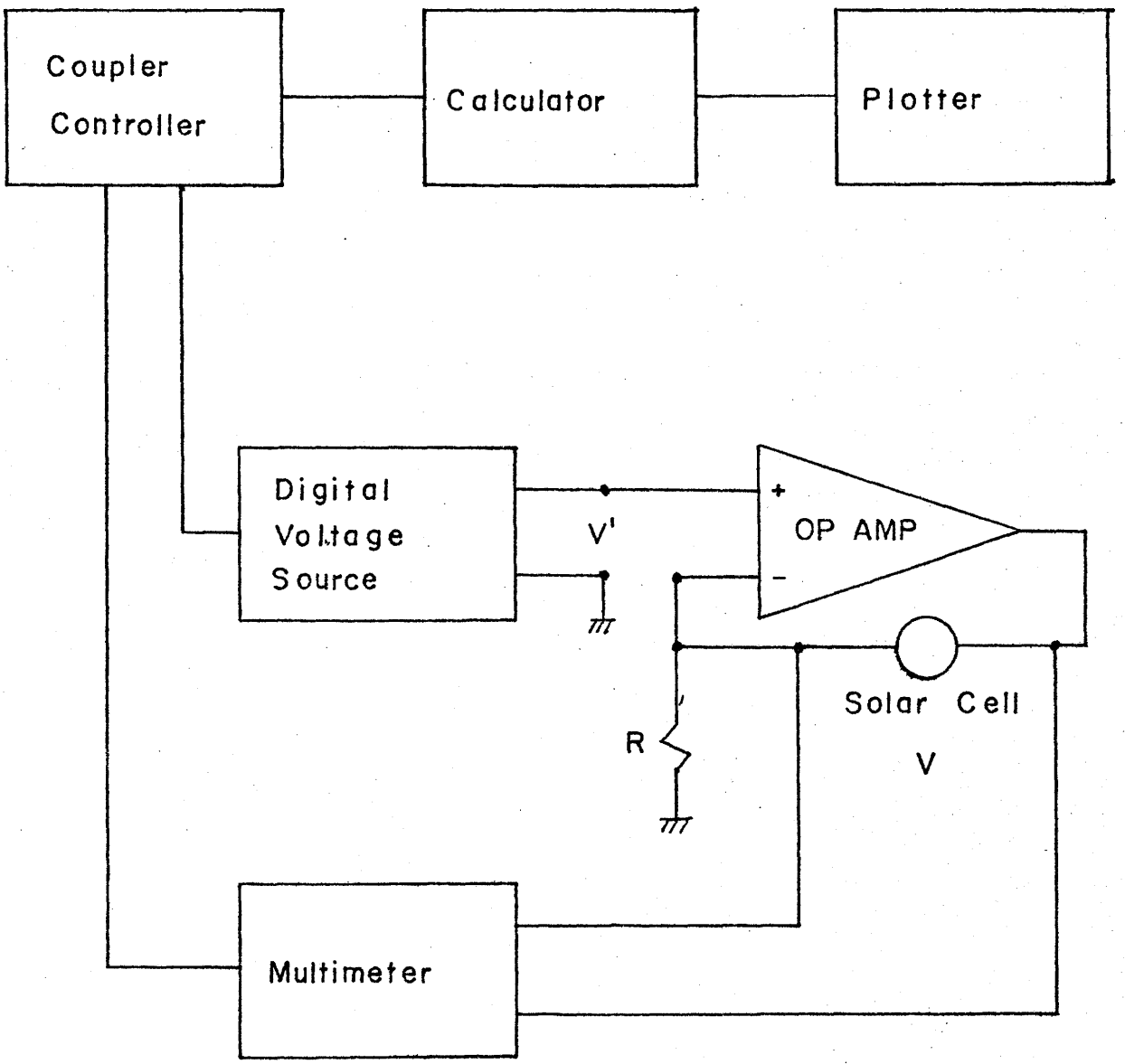

Figure 3 Testing System

after the test. The voltage V^1 is increased in small steps and the voltage across the solar cell is read after each step. Between each step the pen on the plotter advances from the last point representing the read voltage and the current set by V^1 to the newly read voltage and the step increment of current leaving a trace on the graph. The product of the read voltage and set current is taken to determine the power output of the solar cell. If it is the largest such product it is specified as the maximum power output and is printed out at the end of the test. If the voltage across the solar cell is greater than zero the current is increased and the above procedure is repeated. If the voltage across the solar cell is zero or less the current at that increment is specified as the short circuit current of the solar cell. The test is then complete and the open circuit voltage, short circuit current, maximum power point, maximum power and curve fill factor are printed out on the graph of the voltage current characteristics of the solar cell. Figure 4 is a flow chart for the program used in testing the solar cells.

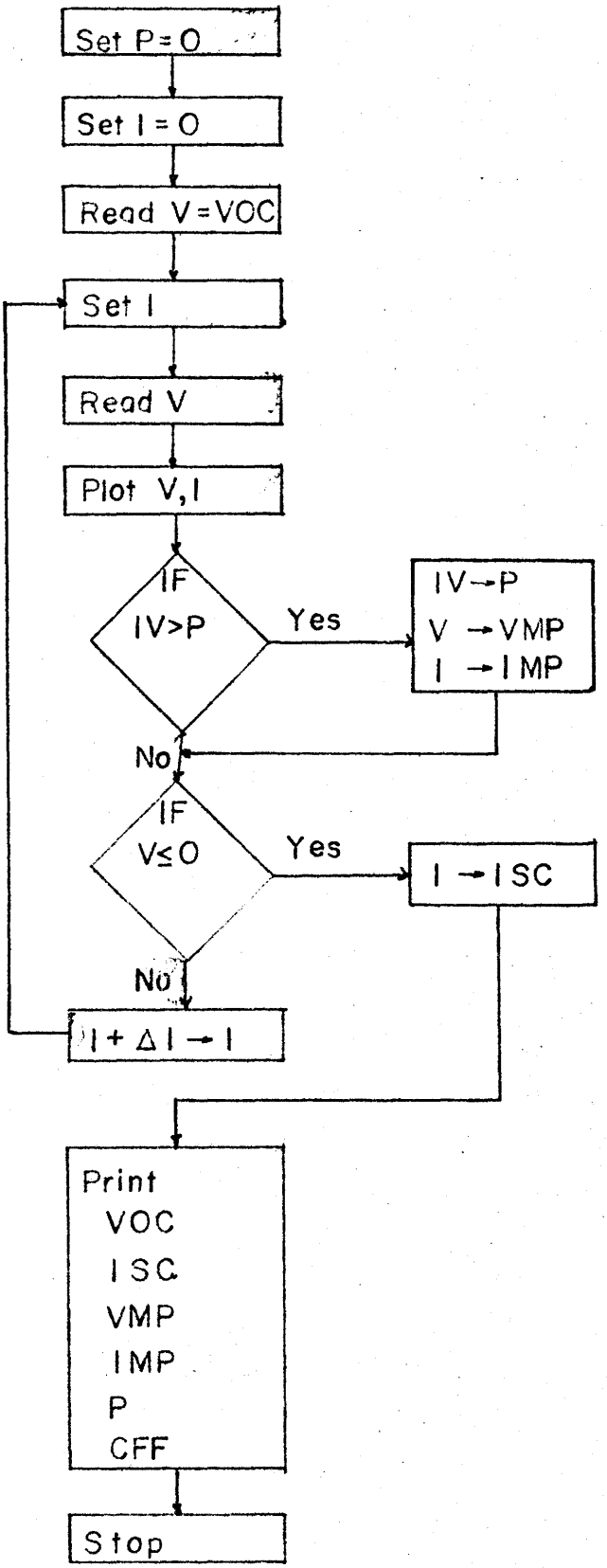

Figure 4 Test Program Flowchart

EXPERIMENTAL RESULTS

The quality of the diffused junction of a solar cell can be determined from the voltage current characteristics of the solar cell without illumination. Figure 5 is a plot of the forward characteristics of a solar cell on a polished surface without illumination. Figure 6 is a similar plot for a solar cell on an unpolished surface. The solar cell on the polished surface turns on sharply over a narrow voltage interval. The solar cell on the unpolished surface turns on gradually over a large voltage interval. A sharp turn on indicates the junction region is relatively free from impurities and damage which degrade carrier lifetimes. Lifetime degrading impurities and damage in the junction region causes the diode to appear "soft" or turn on slowly as in figure 6. When the wafer is sawn the surface is damaged and this damage extends for some distance into the wafer. If this damaged region is not completely removed prior to diffusion it can strongly influence the behavior of the finished diode.[7, 8,9] It would therefore be expected that the damage existing on the unpolished wafer surface causes the diode on that surface to be "soft".

Before the solar cells were tested the intensity of the light from the solar simulator was checked and readjusted using a standard cell. Figure 7 is a plot of the voltage current characteristics of a standard cell. The calibration

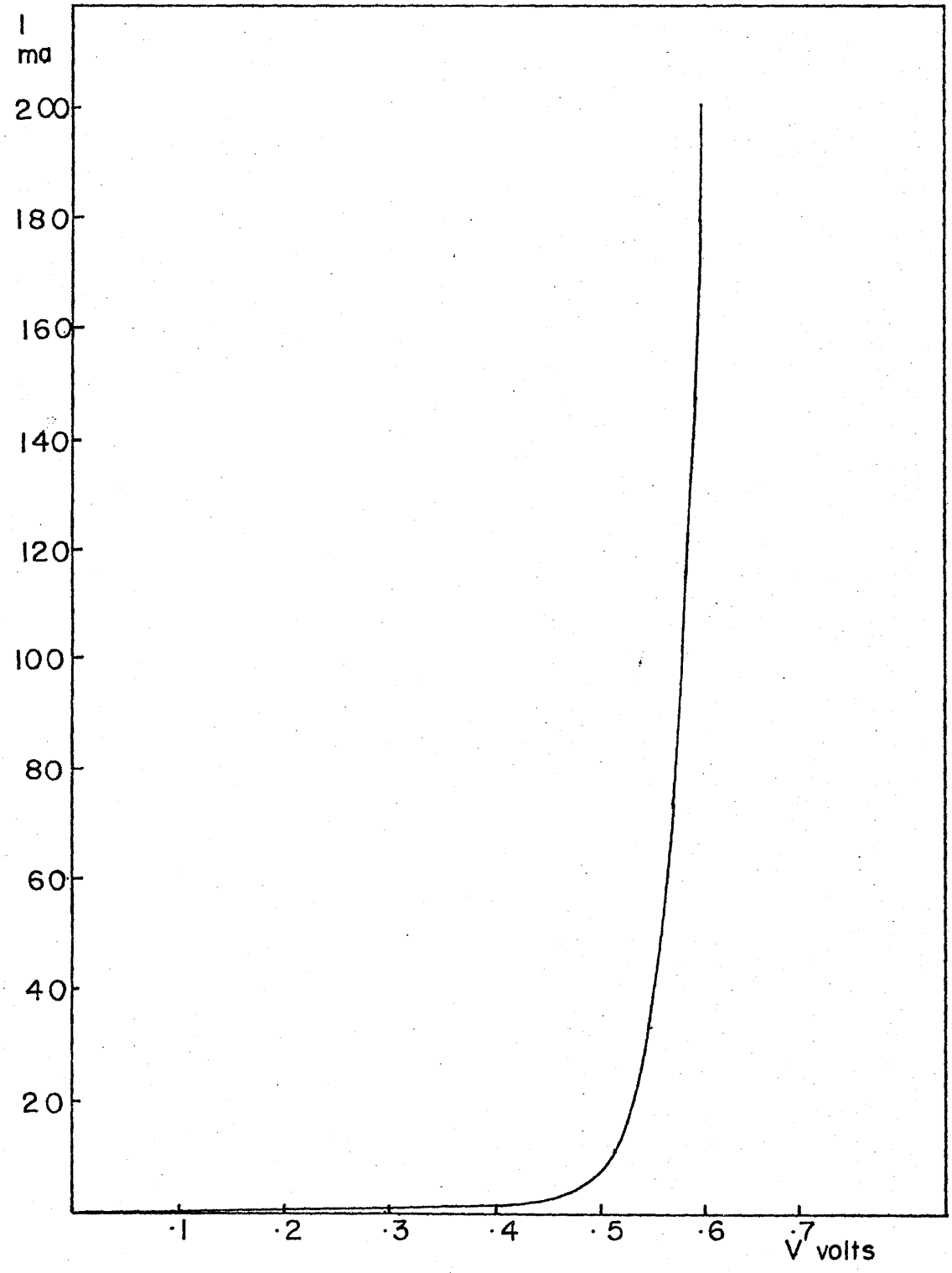

Figure 5 Polished surface dark characteristics

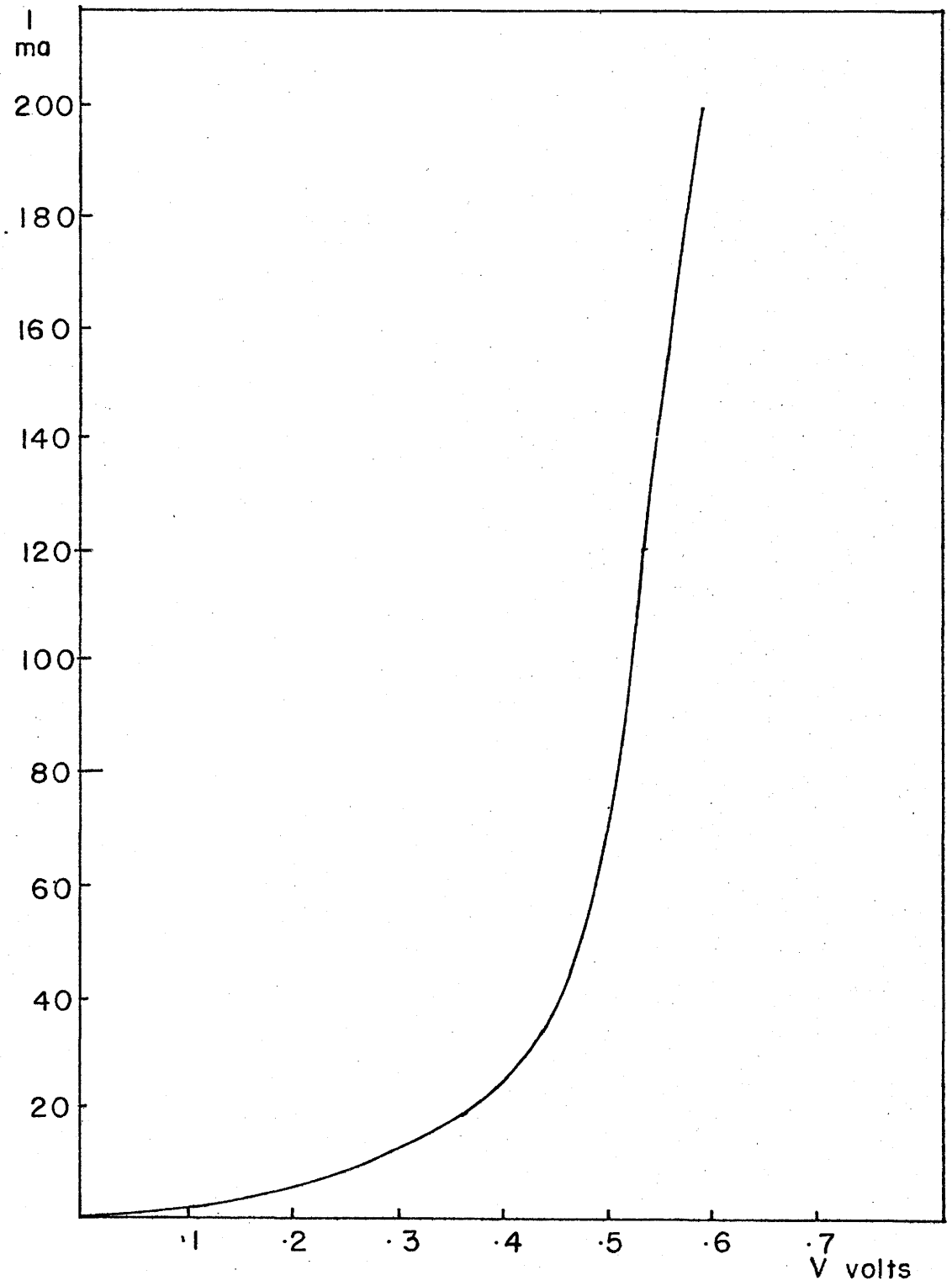

Figure 6 Unpolished surface dark characteristics

is for an air mass 1 spectrum with an intensity of 100 milli watts per square cm. The pertinent data specified by Nasa Lewis for this illumination is: open circuit voltage .528 volts, short circuit current .0581 amperes, maximum power .0206 watts and curve fill factor .672. All of the data corresponds within 2.5% indicating that the solar simulator used was similar to the one used by Nasa Lewis.

Figure 8 is the voltage current characteristics of a polished surface solar cell under illumination. Figure 9 is a similar plot for an unpolished surface solar cell. Excluding the etched portion around the edge of the wafer the active area on both wafers had a diameter of 2.7 cm giving an active area of 5.7 square cm. The short circuit current density of the polished surface solar cell is 17.3 ma/cm^2 and that of the unpolished surface solar cell is 24.4 ma/cm^2. The polished surface of the wafer is highly reflective thus much of the incident light is not absorbed. This low absorbtion causes the short circuit current of the polished surface solar cell to be relatively low. The rough surface of the wafer causes diffuse reflection of normally incident light. Some of this diffusely reflected light falls on another portion of the wafer surface before being reflected away from the wafer. This has the effect of decreasing the overall reflectivity of the wafer surface. Since more light is absorbed the short circuit current density of the unpolished surface solar cell would be expected to be relati-

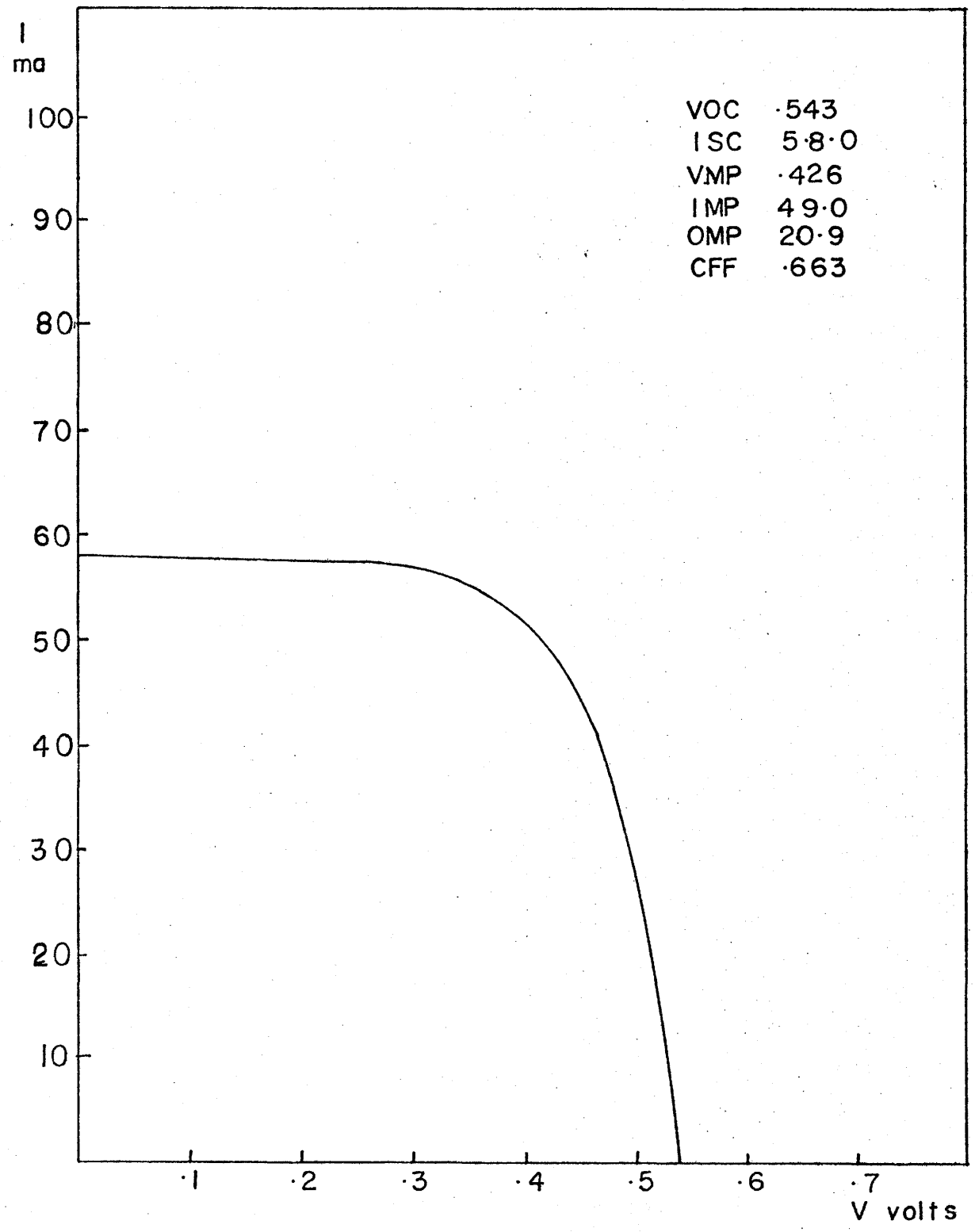

Figure 7 Standard Cell calibration curve

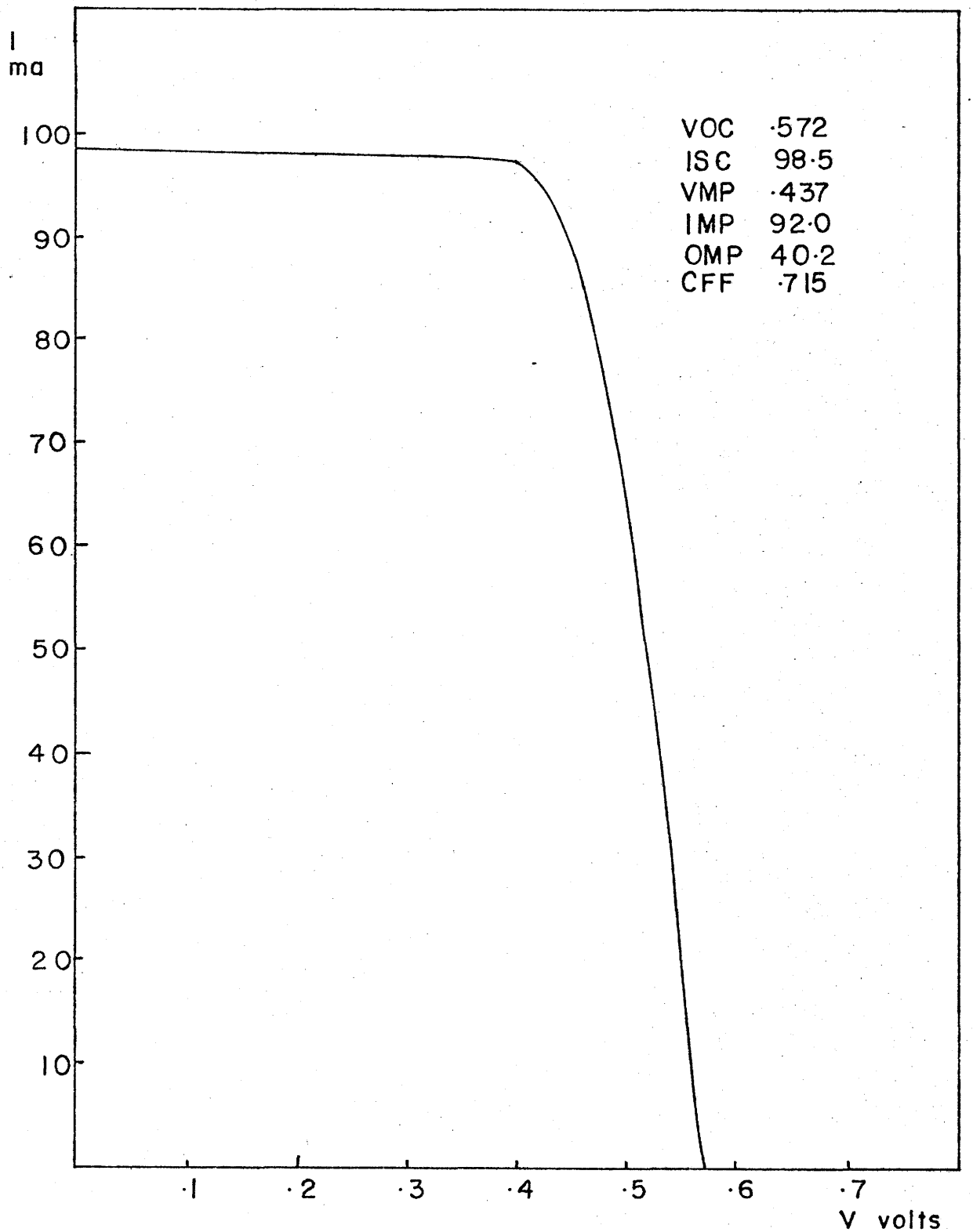

Figure 8 Polished Surface Illuminated Characteristics

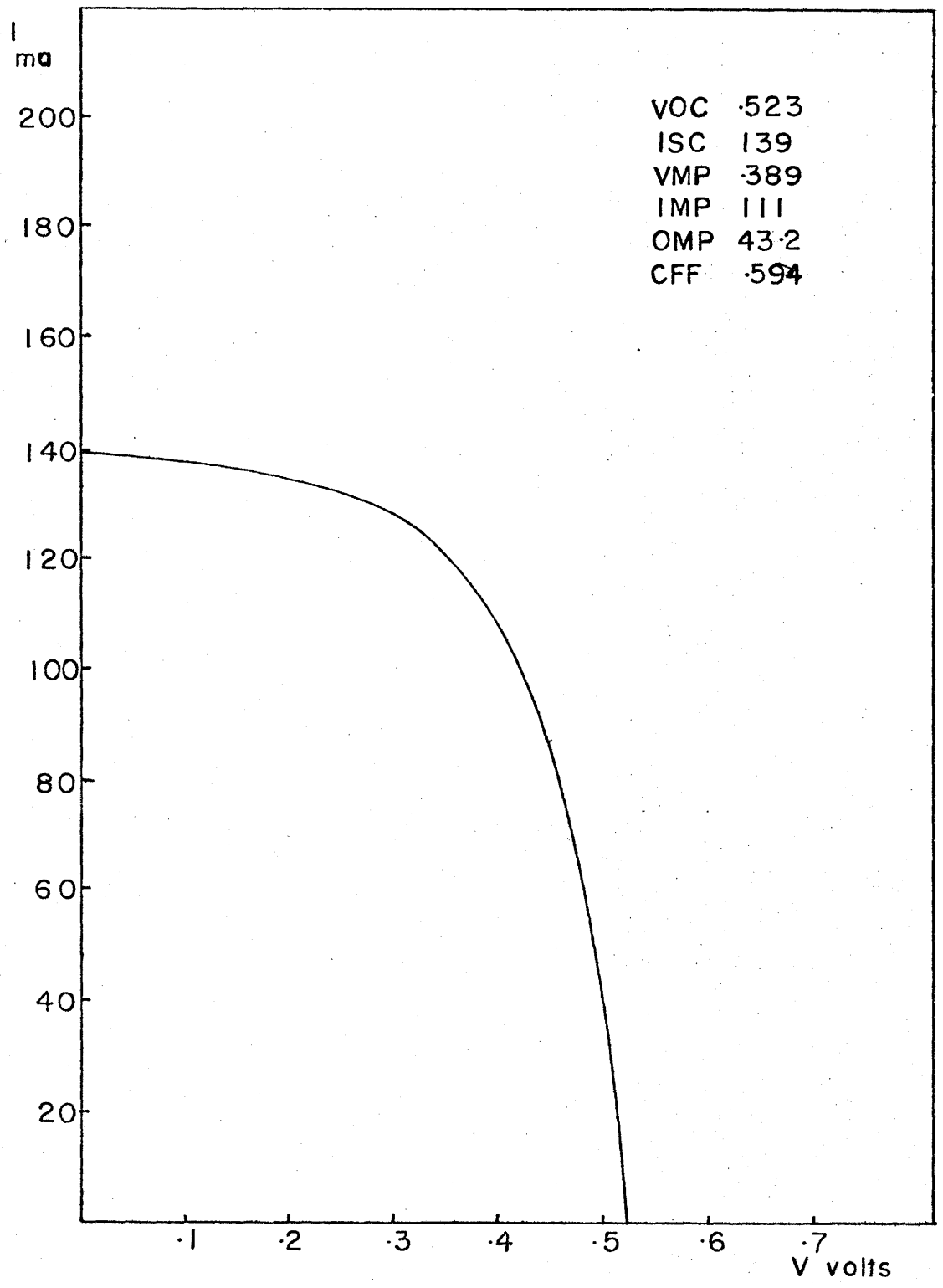

Figure 9 Unpolished Surface Illuminated Characteristics

vely high as is the case. The efficiency of the polished surface solar cell is 7.1% and that of the unpolished surface solar cell is 7.6%. Due to the "soft" voltage current characteristics of the unpolished surface solar cell the open circuit voltage and curve fill factor are relatively low for that type of solar cell. The better voltage current characteristics of the polished surface solar cell results in a larger open circuit voltage and curve fill factor. The high short circuit current of the unpolished surface solar cell is opposed by a low value of open circuit voltage and curve fill factor resulting in a moderate conversion efficiency for that solar cell. The high open circuit voltage and curve fill factor of the polished surface solar cell is opposed by a low short circuit current also resulting in a moderate conversion efficiency for that solar cell. The unpolished surface solar cell is slightly more efficient than the polished surface solar cell but both are moderately high.

CONCLUSION

The manner in which the wafer is processed in preparing the solar cell can significantly influence the voltage current characteristics of the solar cell produced. An error in one or more of the processing steps can result in a solar cell with poor characteristics. The following are a few examples of subtle mistakes which easily occur and result in poor solar cells. Tweezers improperly cleaned can contaminate a large portion of a freshly cleaned wafer surface. Little or no impurities diffuse into the wafer, if the diffusion furnace is not completely purged with nitrogen before the wafer is placed in it. A large contact resistance results from the incomplete removal of the diffusion films. An incomplete masking of the aluminum metalization prior to the etching of the mesa results in a large current leakage after the etching. These as well as numerous other mistakes will severely degrade the performance of solar cell which when properly processed would result in good performance. It therefore can't be over emphasized that excessive care has to be exercised during the processing steps to ensure that the finished solar cell is of good quality and of a reproducable nature.

The efficiency of the polished surface solar cell can be substantially increased by decreasing the reflectivity of the surface. The efficiency of the unpolished surface

solar cell can be slightly increased by decreasing the reflectivity of the surface but more significantly by improving the quality of the junction formed on that surface. To avoid the expense of mechanically polishing the surface of the wafer, perhaps a chemical etch could be employed to remove the damage from the surface leaving a rough damage free surface. The quality of the junction should approach the quality of a junction on a polished wafer when the damage is removed.

The unpolished surface solar cell with an efficiency of 7.6% is competitive with the polished surface solar cell. With an antireflection coating and improved junction characteristics the efficiency could be increased to over 10% making it comparable to present day produced silicon solar cells. More research should therefore be conducted in improving the junction quality of the unpolished surface solar cell.

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