HIGH EFFICIENCY, LOW COST 3" DIAMETER SILICON SOLAR CELLS

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by

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SUPERVISOR: Dr. J. Shewchun

ABSTRACT

Silicon solar cells were produced using inexpensive techniques for obtaining high efficiencies. Large area cells were made with efficiencies greater than 10% (AM1) which were subsequently mounted on a solar panel for future evaluation.

ACKNOWLEDGEMENTS

The author wishes to express his thanks to Mr. R. Singh and Mr. L. Goodridge for their help; to his supervisor Dr. J. Shewchun and particularly to Mr. Ara Kazandjian for his assistance and words of wisdom.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

INTRODUCTION

As concern mounts about future energy alternatives, man has begun looking closer at the sun and using its energy to keep himself warm in the winter and to provide electricity for his modern conveniences.

The silicon solar cell has been known for sometime as being a reliable converter of sunlight into electrical energy. However, until recently, the silicon solar cell has suffered both from low efficiency and high manufacturing costs.

It was the aim of this project to develop a highly efficient (>10%), yet inexpensive cell which was capable of scaling to large areas, (i.e. 3" diameters), without a drastic drop in efficiency. The process was also to be compatible with mass production techniques.

The initial decision to use spin-on diffusion sources as opposed to other diffusion sources was made for several reasons. The spin-on method is very inexpensive compared to other methods[1] and requires little associated apparatus. As well as the cost reduction there are associated benefits of this diffusion method such as good control over surface concentration, minimal surface damage and others.[2]

Previous preliminary work had been done[3] but the cells suffered in several aspects. The need for expensive and time consuming vacuum evaporations was still present and the devices experienced considerable efficiency reductions when built on larger areas. As well, the contacts used, namely aluminum, were inappropriate for making inter-cell connections. These were the problems which had to be solved to achieve a viable product.

The solution to these problems rested basically upon one new approach. Utilizing an electroless plating technique for making nickel contacts and grids, and upgrading these contacts with a solder dip, it was possible to produce a collection grid which was highly conductive, capable of handling the larger currents of increased area cells and also allowed easy cell interconnections.

The resulting increase in efficiency was substantial, yet other improvements were necessary to increase the efficiency. A technique was devised which would considerably reduce the amount of light reflected. By etching a $<100>$ oriented silicon wafer in an aqeous solution of hydrazine hydrate, a "textured" surface resulted which considerably reduced the surface reflectivity. This is made possible by the preferential nature of the hydrazine etch. Hydrazine hydrate selectively etches Si in preferred crystal directions leaving exposed "pyramids" with (111) facets[4] as shown in figure I. Light incident upon this surface will undergo

multiple reflections and thus will have a higher probability of being absorbed by the cell.

The reduction in reflectivity results in improved current generation. A further enhancement of current generation was gained by the application of an evaporated anti-reflection layer of SiO. This treatment can reduce the reflectivity of the cell to about 4%5.

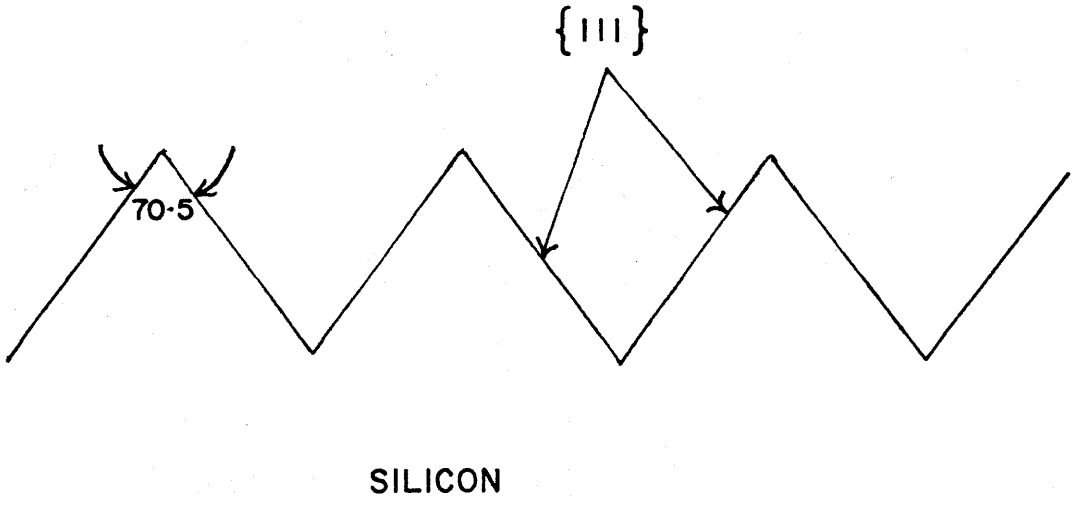


Figure I a): Cross-sectional diagram of silicon (100) wafer schematically showing textured surface with {111} faceted pyramids.

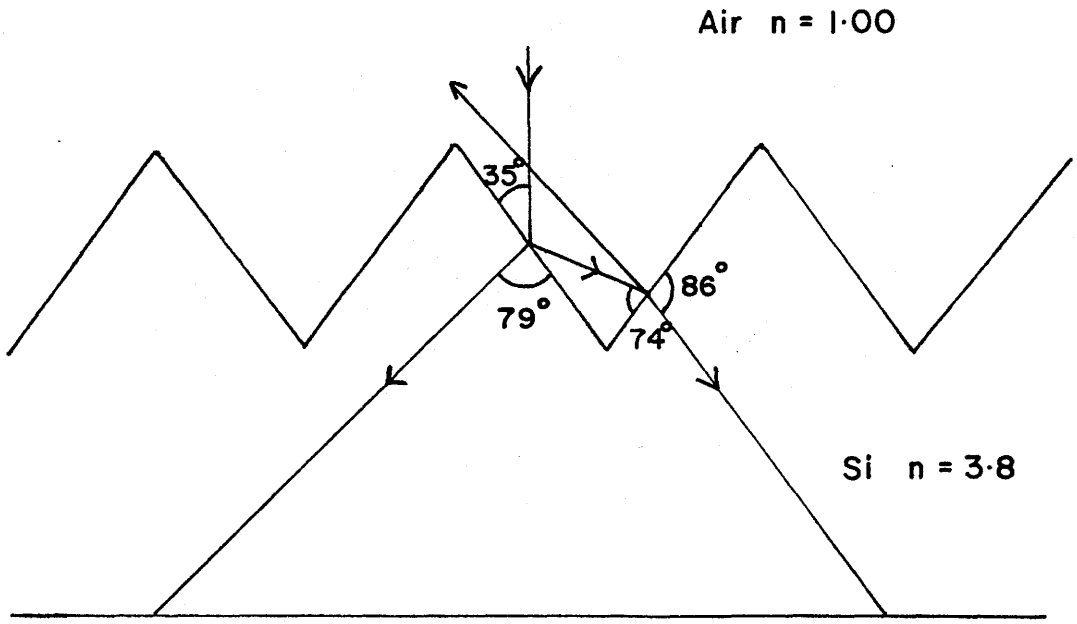


Figure I b): Representation of an idealized textured cell.

EXPERIMENTAL TECHNIQUE

a) Material Considerations

As with any R&D work, the prototypes are very expensive to produce, but along with full scale mass production come reduced prices and processing alterations. The same can hold true with the process developed here. It was decided that in order to sufficiently reduce the surface reflectivity, a texturing procedure was required. Hydrazine hydrate was chosen as a selective etch because of the abundance of literature on this etch and it seemed to give better, more reproducable results than other etches. Unfortunately, hydrazine hydrate is expensive and this may limit its use in a commercial production line. Two other etches have been shown to etch preferentially; ethylene-diamine-pyrocatecol-water and in particular the KOH-H_2O-isopropylalcohol etch appear to be adequate and much cheaper alternates to hydrazine hydrate[6].

The selection of the best spin-on dopant can also pose great problems[7]. It was found that the Borosilicafilm I used previously[8] would not plate entirely. A p^+ diffused aluminum region at the back surface provided a high Voc and also exhibited excellent plating properties. However, an evaporation is a time consuming and costly step. It was

hoped that a spin-on solution containing aluminum as the impurity could be used, but no such solution exists because of the difficulty of reducing Al_2O_3 to free aluminum. A solution containing both gallium and boron as impurities was tried but again the plating was irregular and complete nickel coverage of the back side was seldom achieved. The reason for the failure of the back side to plate using this or the Borosilicafilm I solutions is still not clear. If a cell were fabricated without a p^+ diffusion, the back side would indeed plate, however, the resulting high contact resistance[9] would negate the usefulness of the solar cell. Hence it was decided to continue the use of evaporated aluminum until a substitute p-type dopant was found.

A second problem was also encountered with the spin-on source diffusion method. As reported earlier[10], textured cells processed with spin-on dopants shorted out when the contacts were sintered. It was discovered that the viscosity of the dopant film was sufficiently large to prevent its flow between pyramids as seen in figure II.

A subsequent diffusion would result in p-n junctions being formed only at the very peaks of the pyramids. Thus when contacts were evaporated and sintered, the grid would in fact make contact with the original substrate material and consequently by-pass the junction, resulting in a shorted diode (figure III).

However, a simple reduction in the viscosity of the

dopant solution, (i.e. diluting it with methanol), would result in complete pyramid coverage and proper junction formation. A second application of undiluted dopant was used to insure a high enough impurity concentration and thick enough film to avoid a starved source diffusion. Figures IV and V show the film coverage and final junction formed.

The nickel plating solution used is electroless. This has the convenience of merely placing the silicon wafers in the hot solution to be plated. No connections need be made to the wafers as would be the case in an electroplating technique. The solution used consisted of:

30 g $NiCl_2 \cdot 6H_2O$

10 g $NaH_2PO_2 \cdot H_2O$

70 g $(NH_4)_2HC_6H_5O_7$

50 g NH_4Cl

dissolved in 2500 ml of H_2O. Enough NH_4OH was added during heating to give the solution a pH of at least 9.

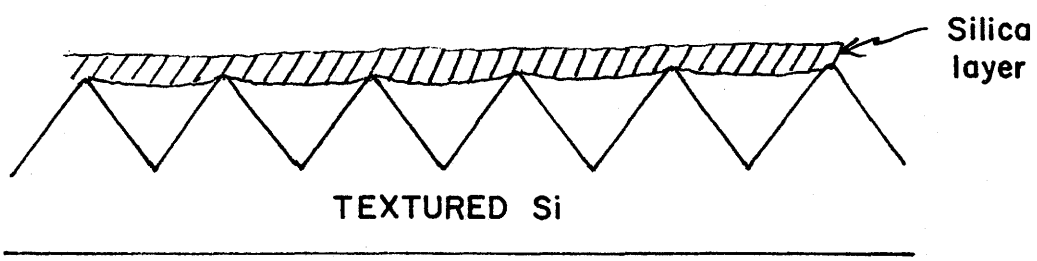


Figure II: Cross-section of textured silicon with viscous dopant spun-on.

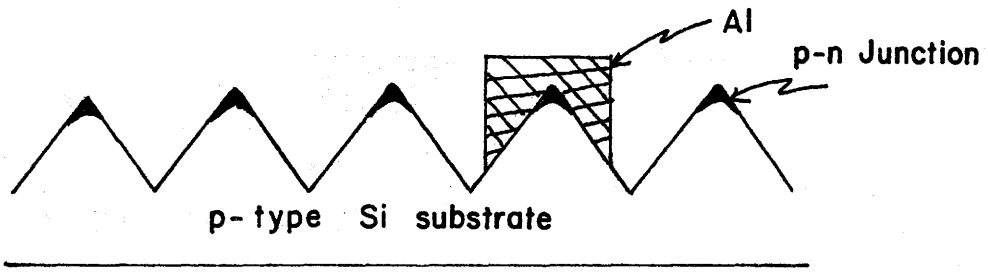


Figure III: Shorted diode.

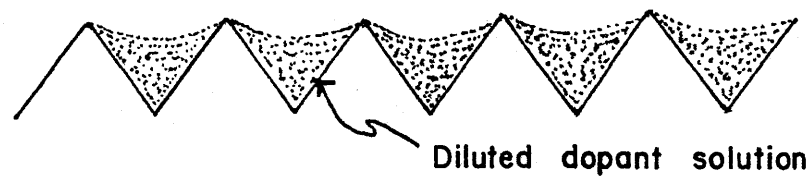


Figure IV: Diluted dopant covering entire textured surface.

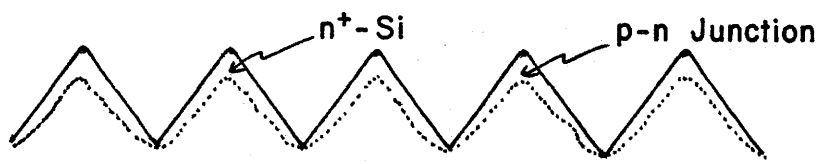


Figure V: p-n Junction.

The flux and the solder used to upgrade the nickel contacts are also very important and much trial and error was needed before an appropriate combination was found.

High temperature solders are useful from the viewpoint of their ability to withstand, without melting, the high temperatures a solar cell attains in bright sunlight. However, at too high a temperature, a solder dip will result in the removal of the front nickel contact grid, particularly if the contact fingers are very fine.

Low temperature solders will not as readily remove the nickel contacts, however, they cannot withstand as high a temperature without melting. The lowest melting point solder made of tin and lead, 63/37, has the added feature of having no plastic state and hence performs much better under primitive dip soldering conditions.

Two types of fluxes were used; an $HCl-ZnCl_2$ solution and Kester 1544, an organic rosin flux. It was found that the rosin flux was superior at higher temperatures while the acid flux was better at lower temperatures. A chart comparing flux behaviour as a function of solder melting points is shown in Table A.

The final choice of solder-flux combination was 63/37 solder with the acid flux. This was necessitated by the grid design which had many fine contact fingers.

Solder	Melting Pt. °C	Acid Flux Behaviour	Rosin Flux Behaviour
63/37	188	Very Good	Poor
50/50	213	Good	Fair
40/60	238	Poor	Very Good

Table A Flux activity comparison

With the large area and corresponding large current generation of a 3" diameter solar cell it was important to keep the series resistance of the conducting grid as low as possible and this necessitated a change in grid design. A new design consisting of three main buss bars was constructed. The buss bars were placed so as to provide the shortest path for current to flow through the collection fingers. This design also provided for any breaks in the collection fingers which may have occurred during the plating or dip soldering process. Other features of the grid are the tapered buss bars which give more exposed surface area and a large pad to make easier cell interconnections. Figure VI compares the old grid design with the new.

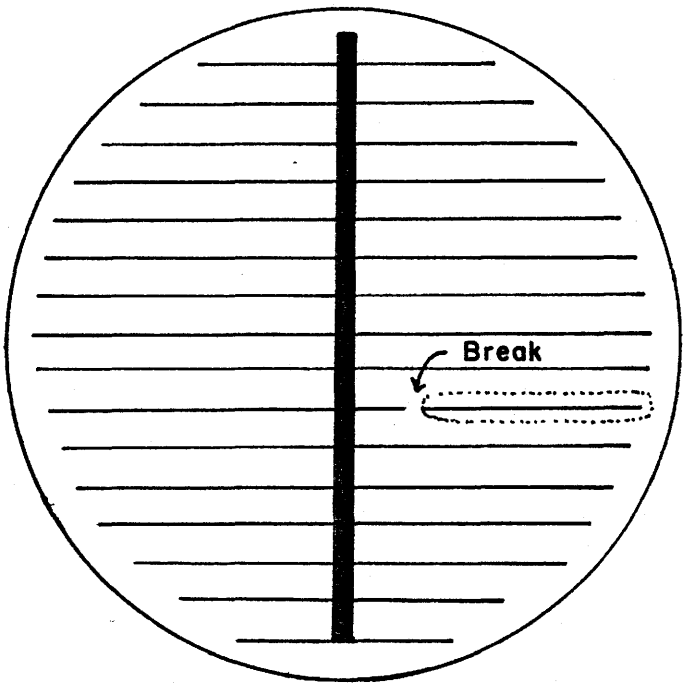


Figure VI a): Old grid design.

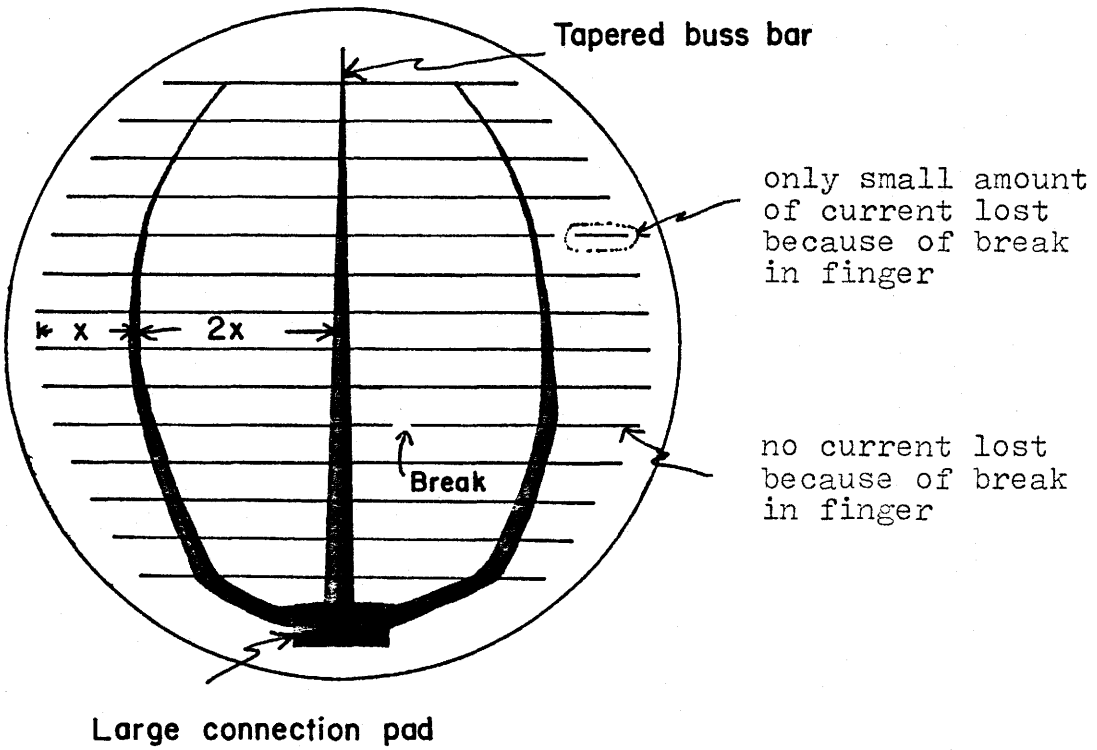


Figure VI b): New grid design.

b) Fabrication Process

The first step towards making a cell is the surface preparation. Hydrazine hydrate does not etch SiO_2. This necessitates a cleaning in hydrofluoric acid prior to texturing. After rinsing away the HF, the Si wafer is placed in a hot (110°C) solution of 60% hydrazine hydrate/40% DI water. The wafer is left to etch for about 6 minutes. Bubble formation necessitates a gentle agitation of the wafer to insure a uniformly textured surface. The resulting surface will display four sided pyramids with heights of approximately 10 micrometers[11]. After removal the wafer is rinsed in DI water.

It then becomes necessary to remove any residual hydrazine hydrate as well as any other contaminants which may hinder the performance of the solar cell. The wafer is first boiled in a solution consisting of H_2SO_4 and H_2O_2 (unstabilized), 5:1 for 5-10 minutes. After rinsing by decanting with DI water, HF is added to the beaker to make an 8% HF solution. This exposes a fresh, clean Si surface. After 2 minutes the wafer is again rinsed thoroughly. Finally an equal amount of H_2O and HNO_3 are combined and the solution heated for about 5 minutes. This procedure makes the Si wafer hydrophilic which makes for better adhesion and uniformity of the phosphorous dopant.

A final rinse is performed to remove all acids and any remaining contaminants[12]. The wafer is blown dry with

nitrogen gas and is placed on the clean vacuum chuck of a photoresist spinner. Several drops of Emulsitone "Phosphorosilicafilm" (Co $5x10^{20}$) diluted 1:1 with methanol are placed on the front surface of the wafer with a clean quartz capillary tube. After the solution has spread to the perimeter, the wafer is spun at 3000 RPM for 20 seconds. A second application of undiluted Phosphorosilicafilm is again spun at 3000 RPM for 20 seconds. The wafer is then placed in a clean petrie dish using clean tweezers and is set in an oven to bake at 150°C for 15 minutes. This step drives off the organic solvents from the dopant film. If not dried properly, an edge stacked, diffused wafer will exhibit non-uniform dopant distribution.

After drying, the wafer is placed in a diffusion furnace which has been previously purged with dry N_2 gas. The phosphorous diffusion is carried out in an N_2 ambient at 900°C for 75 minutes. Upon completion of the diffusion the wafer is placed immediately in a vacuum system and a thick layer of aluminum is evaporated on the back surface. The wafer is again placed in the furnace to undergo an aluminum diffusion at 580°C for 20 minutes in an N_2 ambient to obtain a high conductivity p^+ BSF region.

It is then necessary to remove the excess phosphorous and aluminum from the wafer. This is achieved by first boiling the wafer in a solution of H_2SO_4 : H_2O_2, 5:1. This etches the aluminum. After rinsing in DI water the wafer

is boiled in a solution of H_2O : HCl : H_2O_2, 4:1:1. This step etches any remaining Al and the oxidizing action of the peroxide helps to remove any front surface stains which may have resulted from the diffusion. Another rinse follows and a final etch in 8% HF solution strips the phosphorosilicafilm and any oxide at the back. The wafer is then given a final rinse and blown dry with N_2 gas.

An AR coating of 800 Å thick SiO is then evaporated on the front surface of the wafer in a vacuum system. Shipley positive photoresist (1350-J) is then spun on the front surface of the wafer at 3000 RPM for 30 seconds. The photoresist is dried in an oven for 10 minutes at 80°C. The front contact grid is then defined in the photoresist by exposure to white light through a photographic negative for 90 seconds. After developing in AZ developer, the wafer is rinsed in DI water, blown dry with N_2 gas and baked in an oven at 100°C for 30 minutes to harden the photoresist.

A post bake dip in 8% HF for 20 seconds etches the SiO in the grid slots. After rinsing the wafer in DI water, it is placed in the nickel plating solution at 95°C and allowed to plate for 7 minutes. It is then removed, allowed to cool, rinsed in DI water, stripped of photoresist with acetone, rinsed again and finally blown dry with N_2 gas. The Ni contacts must then be sintered at 300°C in an N_2 ambient for 15 minutes to provide a good ohmic contact.

To upgrade these contacts, one surface of the wafer

is covered with soldering flux and placed on the surface of solder contained in a solder pot which is at 200°C. After a few seconds the wafer is removed and the procedure repeated on the other side. The residual flux is removed by washing in a hot solution of 8 parts DI water, 1 part Liquinox and 1 part NH_4OH. After cooling, the wafer is rinsed in DI water and blown dry with N_2 gas.

Black wax is applied to the front surface of the cell with a Q-tip leaving a 2mm annulus about the perimeter uncoated. After drying, the entire back side is coated with wax and a mesa etch performed in CP4 for 1 minute. The wafer is rinsed in DI water and an oxide grown on the annulus in a solution of 1 part DI water and 1 part HNO_3 for 5 minutes to prevent future contamination on the newly exposed region. The cell is then rinsed and the black wax removed with trichloroethylene. A final rinse in DI water followed by drying with N_2 gas results in a completed cell, ready for testing.

A flow chart follows depicting the processing procedures and figure VIII shows a cross section of the wafer and the result of each processing step.

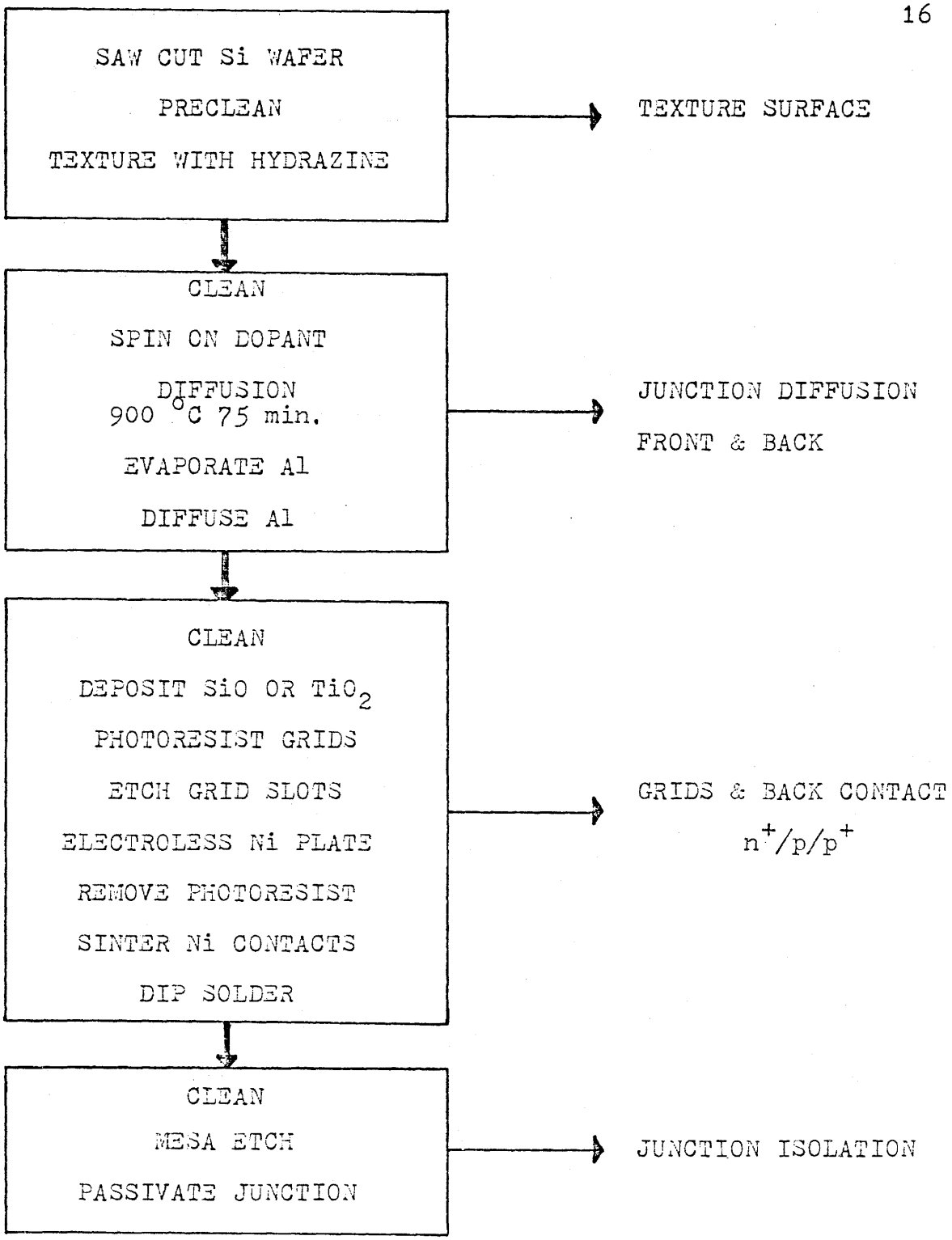


Figure VII: Solar Cell Process Flow Chart

SOLAR CELL FABRICATION STEPS

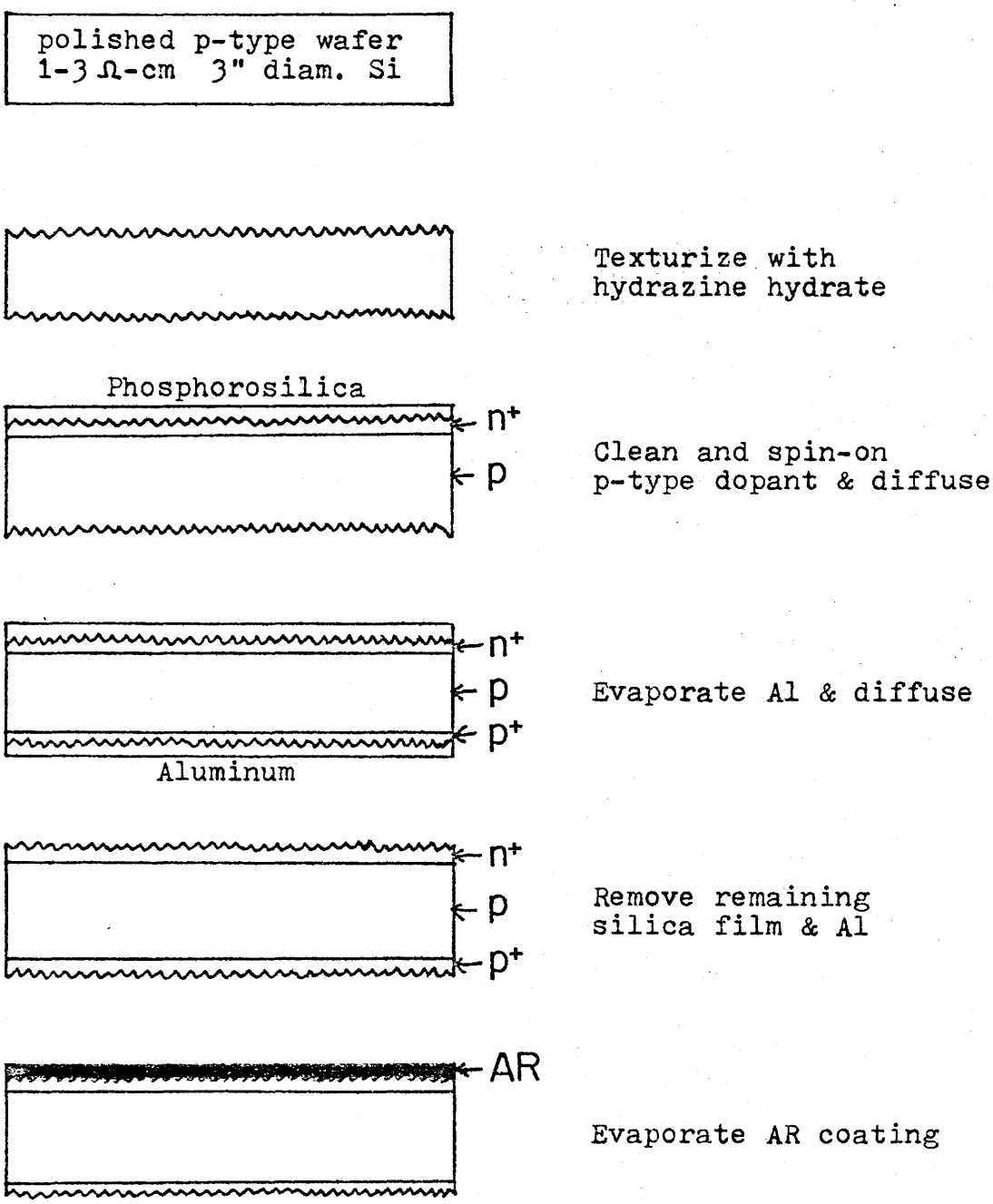
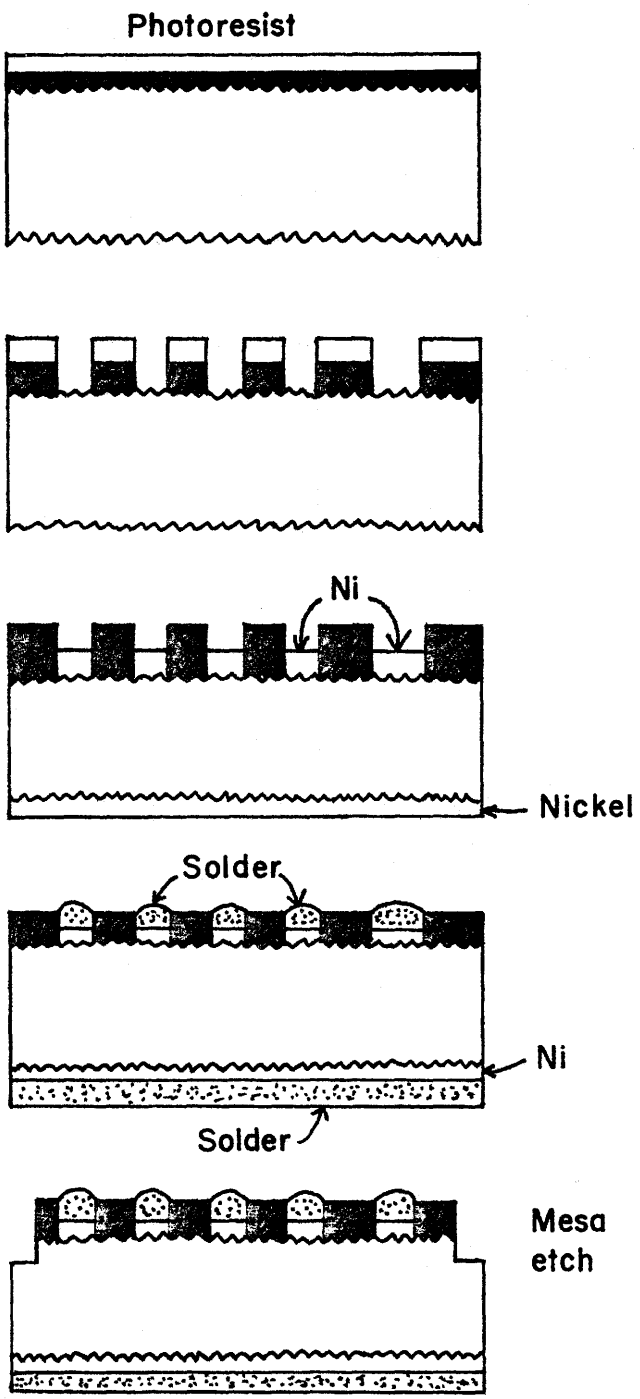


Figure VIII: Wafer cross-section showing results of processing.



Spin photoresist on AR coating

Expose & develop PR. for top grid and etch slots into AR coating

Nickel plate in slots and back side; remove PR.

Sinter Ni contacts then dip solder

Mesa etch and test

Figure VIII: continued.

c) Testing Procedure

The fabricated solar cells were tested using a system assembled from Hewlett Packard components and a high gain operational amplifier. The heart of the system was an HP9820A calculator which could be programmed to send and receive information from a digital voltage source and multimeter through a coupler controller. A calculator plotter was connected to the calculator on which the I-V characteristics could be plotted. Figure IX is a block diagram of the system.

The high gain of the op amp and negative feedback through the solar cell causes the voltage at the non-inverting and inverting terminals with respect to ground to be the same. The inverting terminal of the op amp has a high input impedance, therefore, the current flowing through the solar cell is the same as that through the resistor R which is V_o/R. By using a precision resistor for R of the correct size, the current flowing through the solar cell can be accurately controlled by V_o. By varying V_o between 0 and 10 volts a resistor of 10 ohms will allow the current to vary from 0 to 1 ampere. The voltage across the solar cell is read by the multimeter. The calculator can control the voltage output of the digital voltage source and can receive the voltage across the solar cell from the multimeter. Starting with V_o at zero, the open circuit voltage (V_{oc}) of the solar cell is read and

printed out after the test. The voltage V_o is increased in small increments and the voltage across the cell is read after each step. Between each step, the pen of the plotter advances from the last point representing the read voltage and the current set by V_o to the newly read voltage and the step increment of the current leaving a trace on the graph. The product of the read voltage and set current is used to determine the power output of the device. If it is the largest such product it is specified as the maximum power output (O_{mp}) and is printed out at the end of the test. If the voltage across the cell is greater than zero the current is increased and the above procedure is repeated. If the voltage across the solar cell is zero or less the current at that increment is specified as the short circuit current (I_{sc}). The test is then complete and the open circuit voltage, short circuit current, maximum power, curve fill factor (CFF) and efficiency (EFF) are printed out on the graph of the I-V characteristics of the solar cell. Figure X is a flow chart for the program used in testing the solar cells.

Sunlight used for testing fabricated solar cells was simulated using tungsten halogen quartz projector lamp bulbs. Using a standard cell calibrated by Nasa Lewis it was possible to adjust the intensity of light in the test plane to within 3% of an internationally accepted intensity. This insures that all cells tested here are tested under the same

conditions and allows an accurate comparison with cells made and tested in other laboratories around the world. Figure XI shows a comparison of the spectral distribution of the simulated sunlight and actual sunlight.

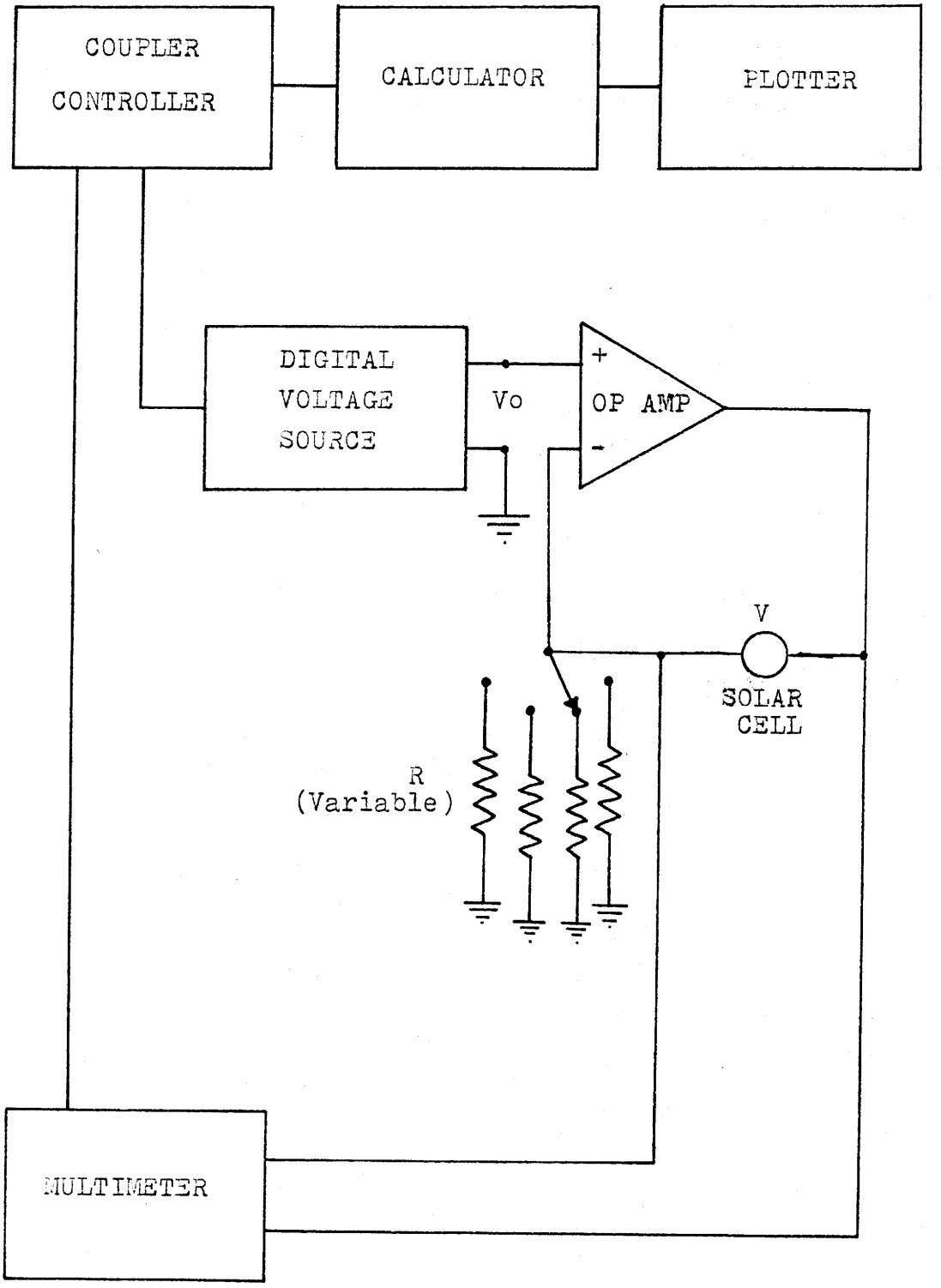
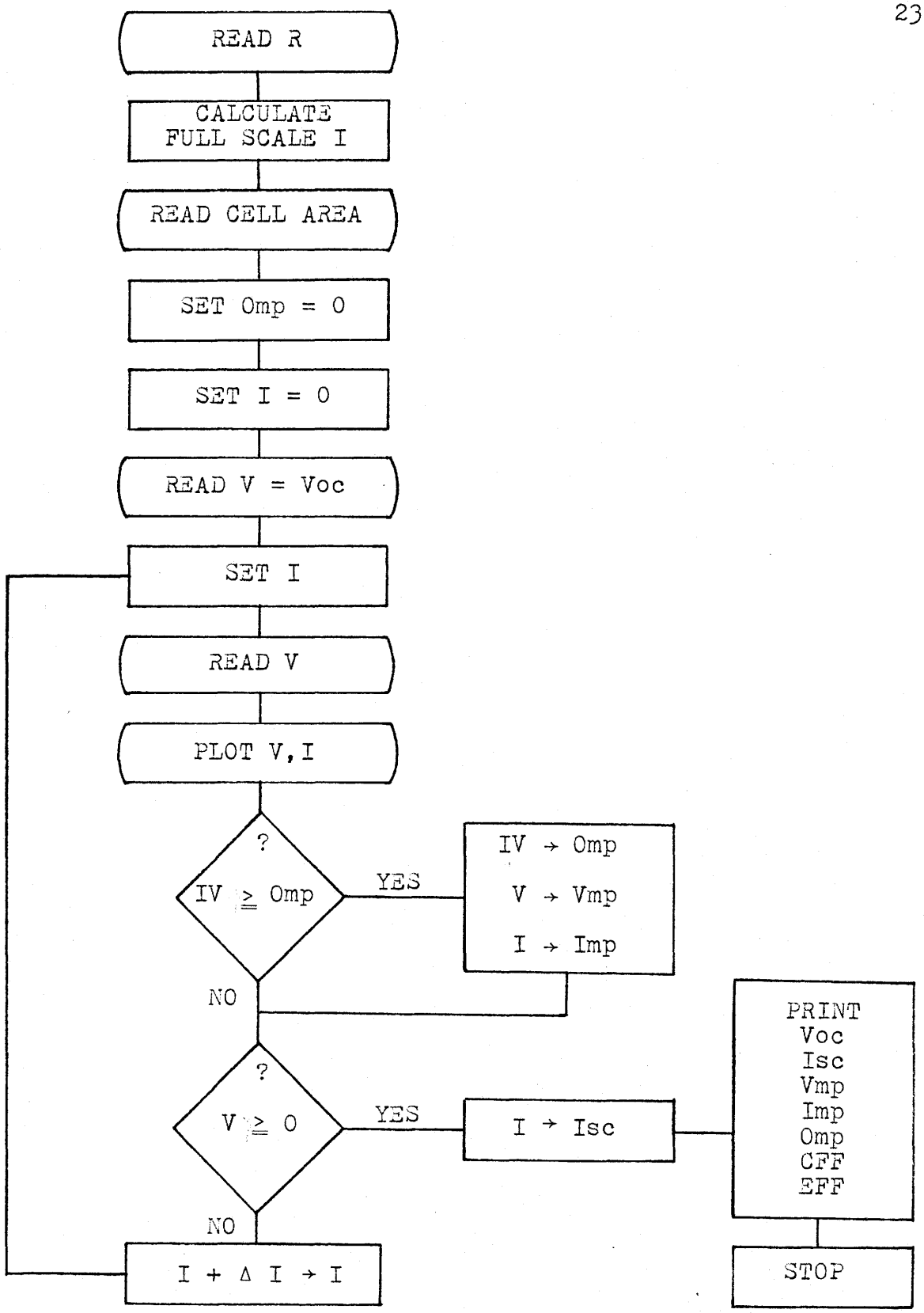


Figure IX: Block diagram of test system.

Figure X: Test program flowchart.


READ R
CALCULATE FULL SCALE I
READ CELL AREA
SET Omp = 0
SET I = 0
READ V = Voc
SET I
READ V
PLOT V, I
? IV ≥ Omp
YES
IV → Omp
V → Vmp
I → Imp
NO
? V ≥ 0
YES
I → Isc
NO
I + Δ I → I
PRINT Voc Isc Vmp Imp Omp CFF EFF
STOP

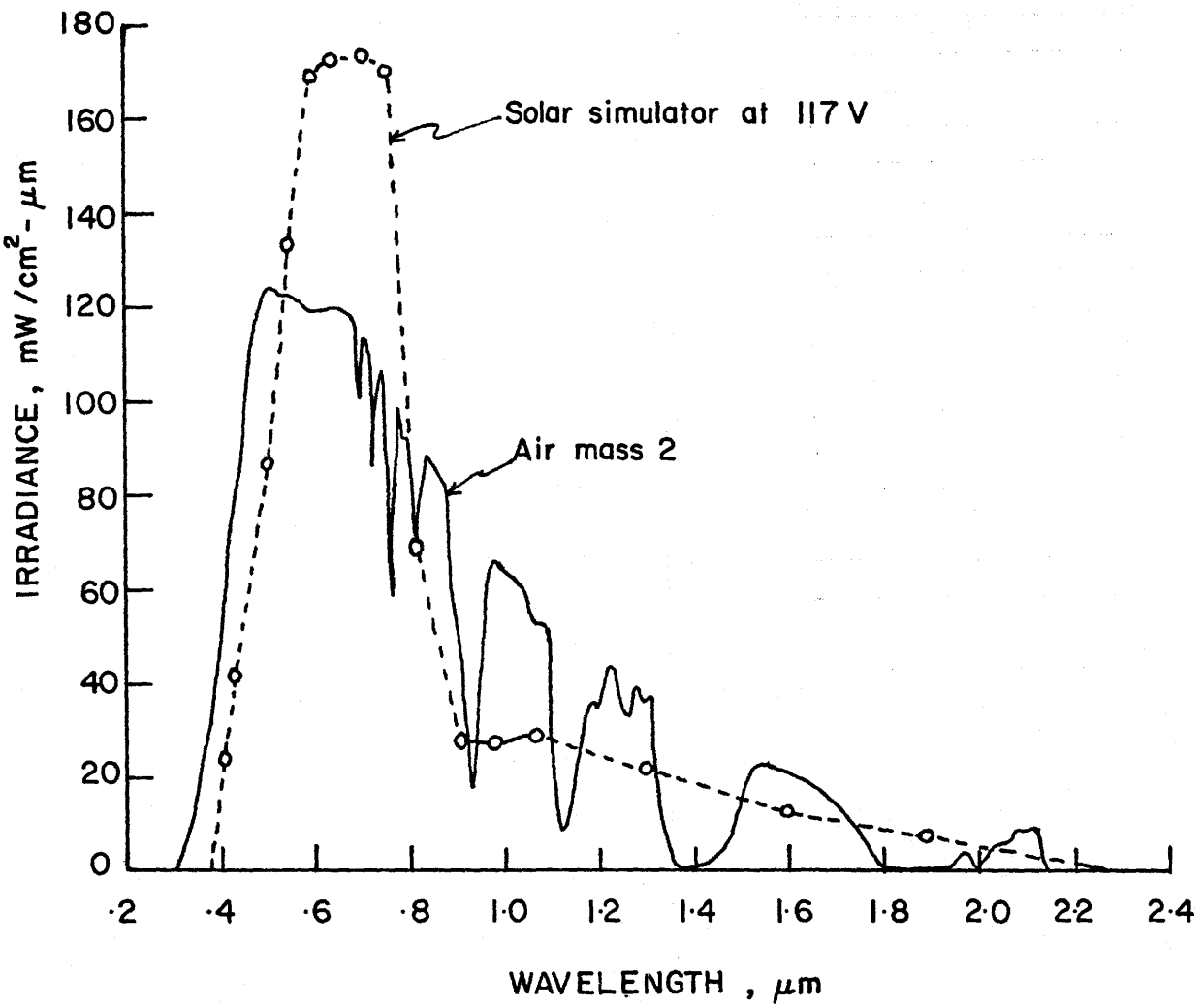


Figure XI: Variation of spectral irradiance with wavelength.

RESULTS

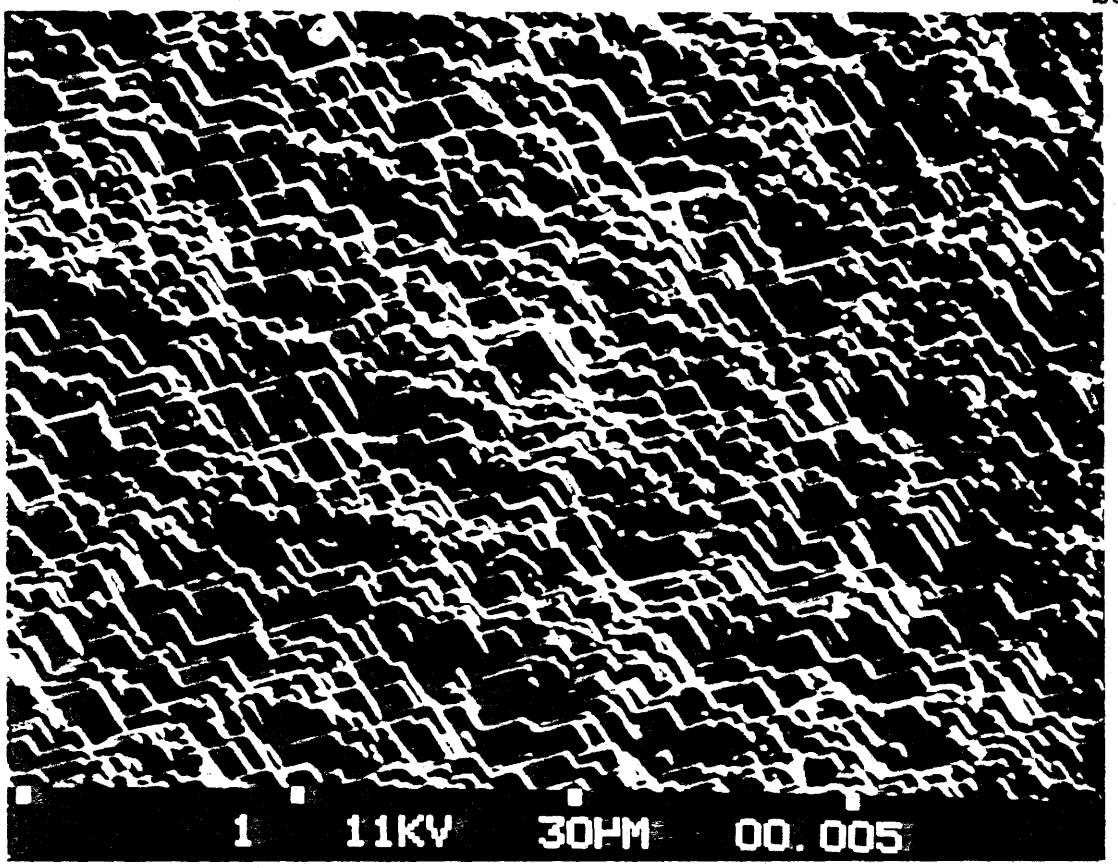
Silicon wafers processed using the hydrazine texturing etch had a velvet appearance. Figure XII shows magnified views of the surface using a scanning electron micrograph. Clearly visible are the four-sided pyramids. With an AR coating, the surface exhibited a very dark, matt appearance, exemplary of a non-reflecting body. Solar cells manufactured with textured surfaces displayed higher efficiencies than previous cells made on polished silicon wafers. Figure XIII shows a starting polished wafer and a finished textured solar cell.

An I-V plot of a typical 3" diameter cell is shown in figure XIV. To obtain a closer look at the behaviour of the diode a dark log I-V plot was made as a function of temperature and is shown in figure XV a) along with its illuminated and dark I-V's, figures XV b) and XV c) respectively. The junction depth was estimated to be 1 micrometer and the resistivity of the surface layer was measured to be 0.002 Ω-cm.

Three inch cells were routinely produced with short circuit current densities of 32 ma/cm^2, open circuit voltages of 0.58 and curve factors of .6 giving efficiencies of over 11%.

Figure XII: a) Scanning electron micrograph of textured surface at 60^{o} angle and 980 magnification;

b) SEM of same surface at 30^{o} angle and 3100 magnification.


1 11KV 30HM 00.005

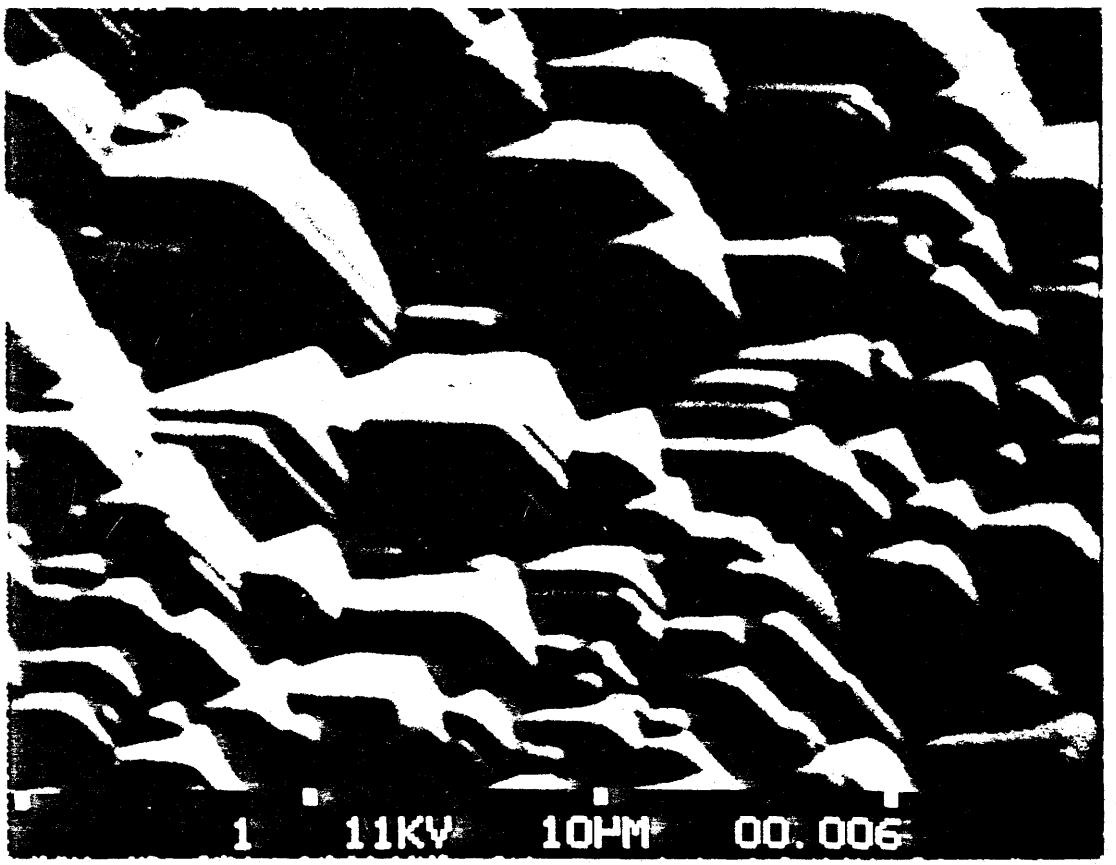

1 11KV 10HM 00.006

Figure XIII: Photograph of starting polished 3" Si wafer and finished textured surface solar cell.

27

Figure XIV: I-V of typical 3" solar cell.

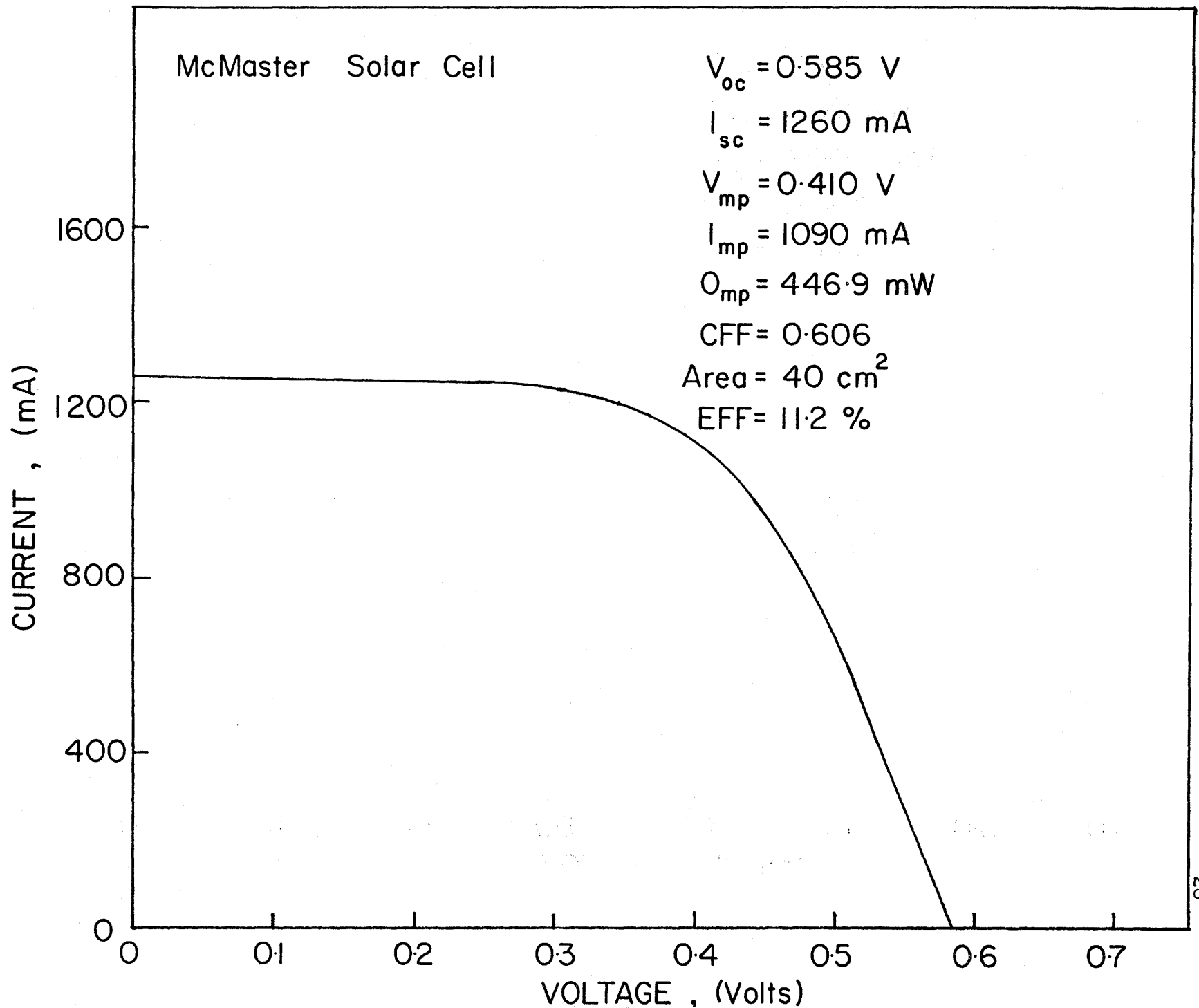
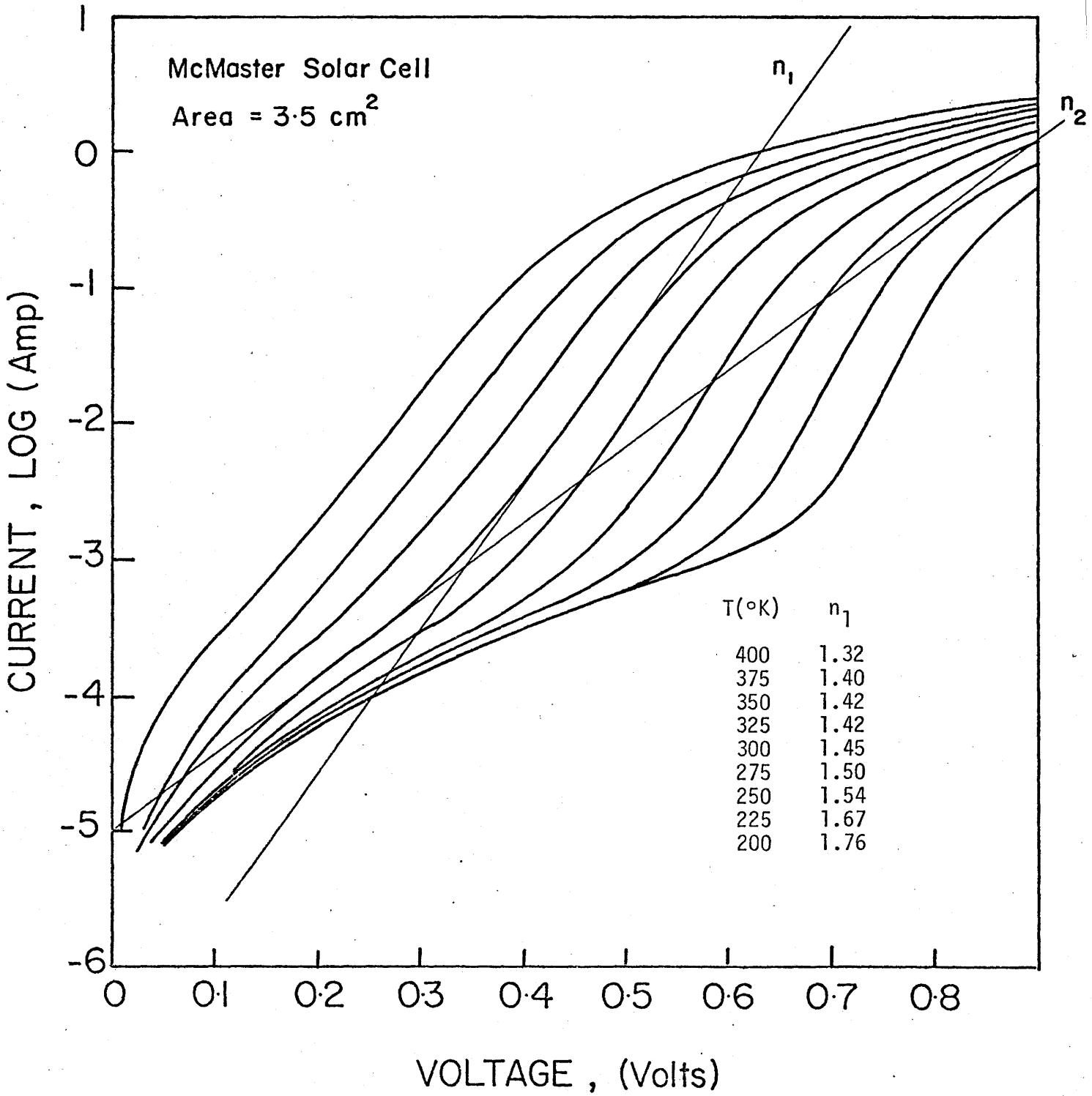
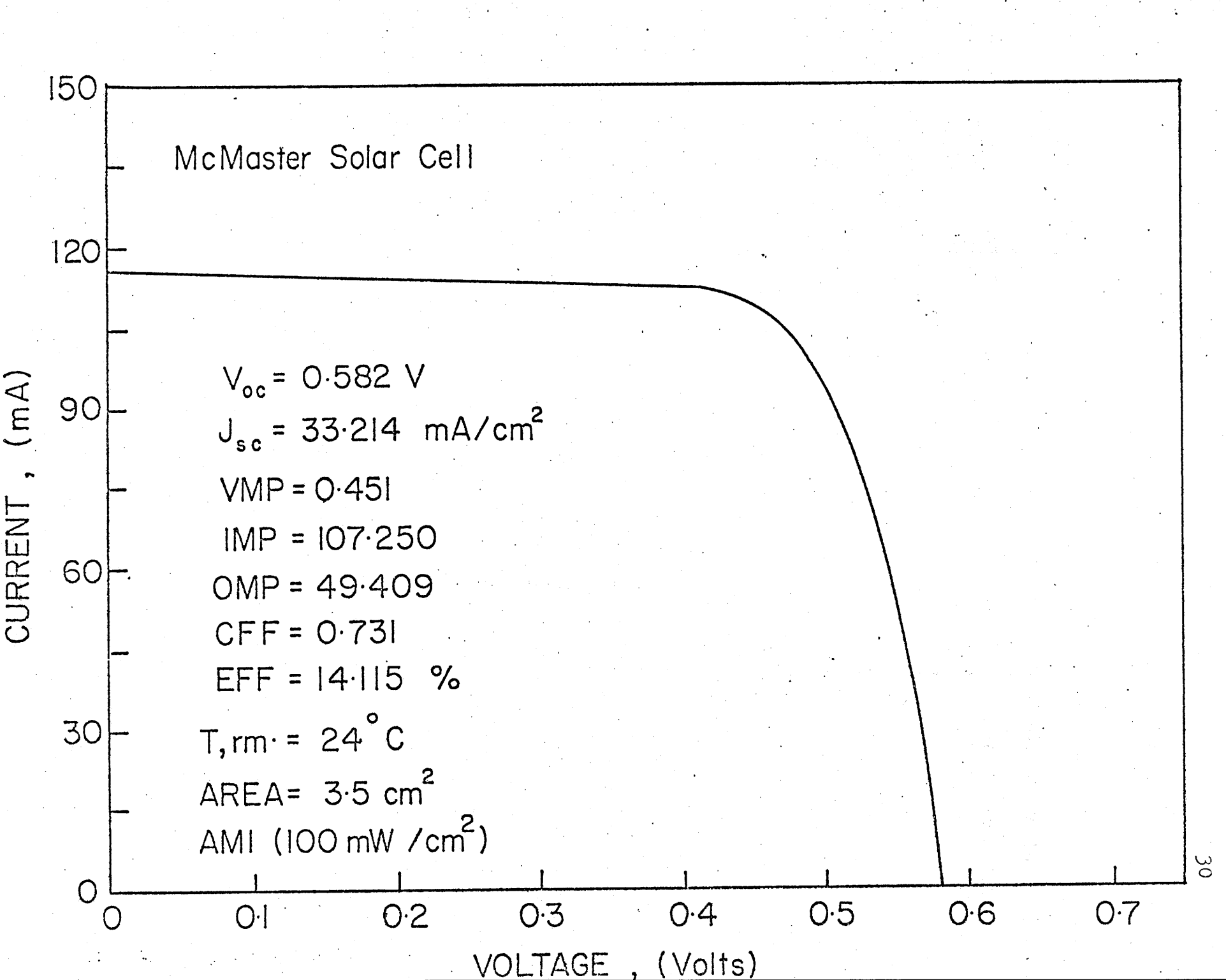

McMaster Solar Cell
V_{oc} = 0·585 V
I_{sc} = 1260 mA
V_{mp} = 0·410 V
I_{mp} = 1090 mA
O_{mp} = 446·9 mW
CFF = 0·606
Area = 40 cm^2
EFF = 11·2 %
CURRENT , (mA)
1600
1200
800
400
0
0
0·1
0·2
0·3
0·4
0·5
0·6
0·7
VOLTAGE , (Volts)

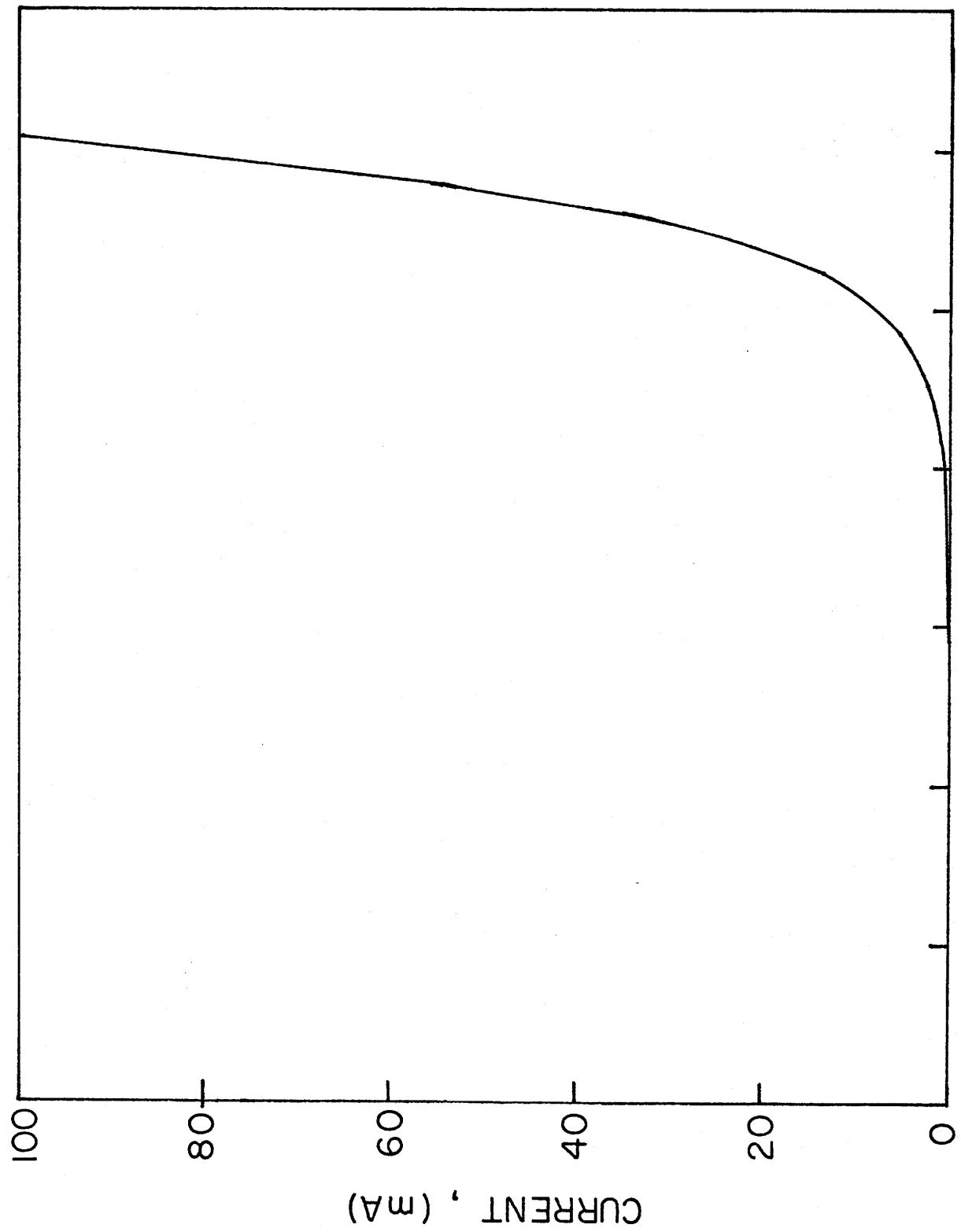
Figure XV: a) Log I-V of a solar cell;

b) Illuminated I-V;

c) Dark I-V.


McMaster Solar Cell
Area = 3·5 cm²
n1
n2
T(°K) n1
400 1.32
375 1.40
350 1.42
325 1.42
300 1.45
275 1.50
250 1.54
225 1.67
200 1.76
CURRENT, LOG (Amp)
1
0
-1
-2
-3
-4
-5
-6
0
0·1
0·2
0·3
0·4
0·5
0·6
0·7
0·8
VOLTAGE, (Volts)


McMaster Solar Cell
V_{oc} = 0·582 V
J_{sc} = 33·214 mA/cm^2
VMP = 0·451
IMP = 107·250
OMP = 49·409
CFF = 0·731
EFF = 14·115 %
T, rm· = 24° C
AREA = 3·5 cm^2
AMI (100 mW /cm^2)
CURRENT , (mA)
VOLTAGE , (Volts)
150
120
90
60
30
0
0
0·1
0·2
0·3
0·4
0·5
0·6
0·7


CURRENT , (mA)
100
80
60
40
20
0
0
0·1
0·2
0·3
0·4
0·5
0·6
VOLTAGE , (Volts)

DISCUSSION

A close examination of the junction itself shown by the semi-log plot in figure XV a) confirms that the diode characteristics are reasonably well behaved. The diffusion region at high voltages has an n value of $\sim$1.4-1.5 using the equation

$$J = J_o \exp(\frac{eV}{nkT}) - 1$$

The saturation current dependence with temperature, $J_o(T)$ indicates an activation energy of about 0.7 eV. The low voltage region has an n value of $\sim$2.0 indicative of recombination effects and, in addition, at low temperature a shunt conductance effect is visible.

Although solar cells made on textured silicon wafers showed higher efficiencies than those made on silicon with a mirror surface, it is interesting to note the difference in curve factor. It was possible to make 3" diameter solar cells on mirror finished silicon with curve factors as high as .79 and routinely .73 whereas textured surface solar cells had curve factors of only .6. The reasons are probably twofold.

Firstly, the etching of the silicon with hydrazine can result in a non-uniform surface texture unless great

care is taken. This non-uniformity will result in a non-uniform p-n junction which reduces the quality of the diode. Evidence of this can be seen in the work done by Liikala on unpolished silicon[13]. The large area of a 3" silicon disk greatly increases the probability of surface non-uniformity.

Secondly, there is a large series resistance on the textured silicon cells, measured to be $\sim 0.2\ \Omega$ for a 3" diameter cell. This again is probably due to 2 reasons. The small resistance of the collection grid may become significant due to the much larger current it must carry on the textured cell. The short circuit current density of a textured cell is about $32 ma/cm^2$ whereas the polished surface cell generates a short circuit current of only about $26 ma/cm^2$.

The series resistance may also be due to a large contact resistance. The front collection grid may only be making contact with the peaks of the pyramids of the textured cells, whereas contact would be made entirely on the polished surface cell. The problem could be partially remedied by making wider grid lines, however, this would shadow the cell and result in a lower short circuit current. The present surface coverage by the grid is $\sim 10\%$.

As can be seen, more work is needed to optimize both the grid design and contact to insure a low series resistance.

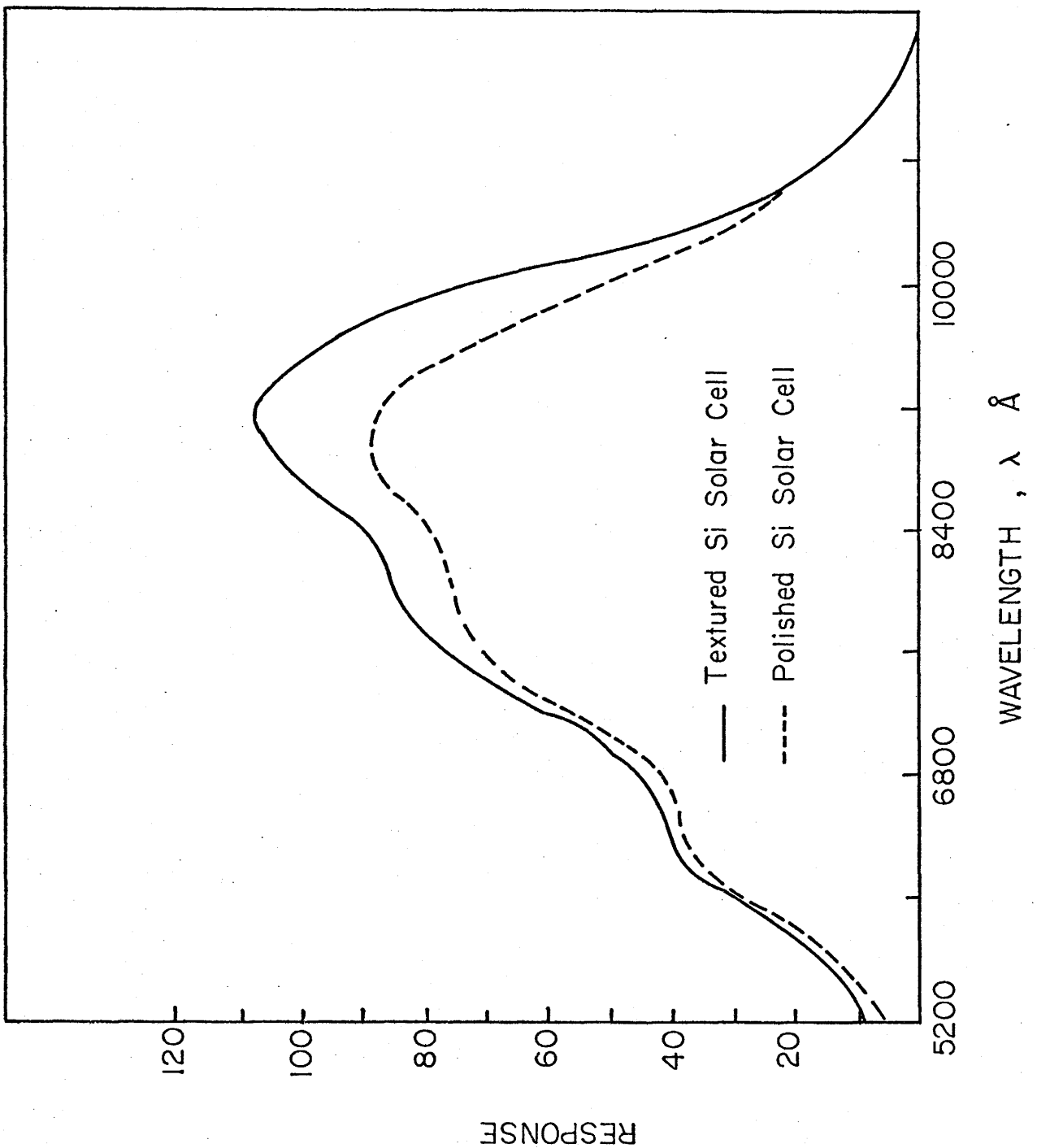
Figure XVI shows a spectral response comparison between a cell with a textured surface and one with a smooth mirror surface. Both were processed in otherwise identical ways. The data would indicate an enhanced IR response, not unlike previous reports on textured surfaces[14], but the situation in the UV is ambiguous. Previous reports also indicate an enhanced UV response. The reasons for any changes are at present speculative at best but this area does deserve more detailed consideration as it will undoubtedly shed light on the enhanced performance of textured surface cells.

One particular processing change may reveal much about the spectral response of the textured cell. Unfortunately, at present both the back side and front side of a silicon wafer are textured by the hydrazine etch. It should be more beneficial if only the front side were textured and the back side left in its semi-polished state. This would provide a relatively smooth surface for unabsorbed IR light to be reflected back into the bulk material of the solar cell. Also the thickness of the wafer would not be reduced as much which can also cause a drop in IR response.

Attempts were made to mask the back side using photoresist and black wax, but neither could stand up to the hydrazine etch. An alternative to this approach would be to grow a thick layer of oxide on the wafer. Hydrazine hydrate will not etch SiO_2 and thus it can be used as a mask to

protect the back side. In fact, it could be possible to also mask the front grid pattern and only texture the surface between the grid fingers. This should lead to a lower contact resistance, however, the alignment problem may be difficult and the added expense of an oxidation system may be prohibitive.

Figure XVI: Comparison of spectral response of cells with different surface finishes.


RESPONSE
120
100
80
60
40
20
5200
6800
8400
10000
WAVELENGTH , λ Å
Textured Si Solar Cell
Polished Si Solar Cell

CONCLUSIONS

Although efficiencies of over 11% (AM1) have been achieved, it is felt that the process is routinely capable of cells in excess of 15%. Several items require further study and optimization. They are:

1. a cheaper selective etch,
2. spin-on p-type dopant, compatible with the Ni plating process,
3. junction depth,
4. front grid design,
5. TiO_2 spin-on AR coating.

With the achievement of the above it should be possible to produce very efficient, large diameter silicon solar cells with very low processing costs.

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