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FIBRE OPTTC TELEPHONE - ANALOG ELECTRONICS

AN OPTICAL FIBRE TELEPHONE SYSTEM

(ANALOG ELECTRONICS)

by

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PART A: McMASTER (ON-CAMPUS) PROJECT*

A Project report submitted in partial fulfillment of
the requirements for the degree of
Master of Engineering

Department of Engineering Physics
McMaster University
Hamilton, Ontario, Canada

1980

*One of two project reports. The other one is designated PART B: OFF-CAMPUS PROJECT

MASTER OF ENGINEERING (1981)
Department of Engineering Physics

McMASTER UNIVERSITY
HAMILTON, ONTARIO

TITLE: An Optical Fibre Telephone System
(Analog Electronics) Part A

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NO. OF PAGES: vi, 64

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ACKNOWLEDGEMENTS

The author would like to express his thanks to Dr. J.P. Marton for his supervision of this project. Special thanks are in order to my associates, Van Tzannidakis, John Goodwin, and Gary Duck.

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CHAPTER 1

INTRODUCTION

One of the main advantages of fibre optics is the large potential increase in information carrying capacity. Because of its higher frequency, light offers an increase of four orders of magnitude over microwave transmission. As well as this, fibre optics is advantageous for other reasons. These include crosstalk immunity, ground loop immunity, E.M.I. immunity, small size and weight, and longer repeater spacing due to the fibres low loss and wide bandwidth.

As an example of the state of the art of optical fibre communications, a system was installed in Chicago in 1977 over a ten kilometer length. It used injection lasers driven at a rate of 44.7 megabits per second. The fibre cable contained 24 fibres, each fibre having the capacity to carry 672 one way voice signals.

Many such systems have been recently built, and evaluation reports are just beginning to appear. Many areas and problems remain to be investigated. For instance, a recent article in the IEEE Journal of Cable Television points out the need for more research into optical splitters and taps. This need was one of the primary motivations for the present project.

For our M.Eng. on-compus project, my associates and I have chosen the design, assembly and preliminary evaluation of a telephone system designed for short or medium distance transmission over optical fibre.

For a successful completion of the project, this system was required to meet the following specifications:

1. Each end of a two party conversation must be able to transmit and receive simultaneously, as is the case with most public telephone systems. Such an arrangement is referred to as a duplex system.
2. This system should have most of the other characteristics of a commercial telephone system, such as:

a) there be a system of audio cues (dial tone, busy tone, ringing tone, etc.)

b) that no adjustments or technical knowledge be required of the user

c) that all of the interconnections be made automatically and be based on a simple number system

d) that all conversations be inaccessible to other parties

3. The system should be compact, and rely on portable power supplies at each station.
4. The system should make use of opitical (as opposed to electrical) types or splitters, employ fibres bidirectionally (rather than using separate fibres for transmitting and receiving), and have all signals carried over a single fibre (i.e. a multiplexed system).
5. Due to the varying numbers of taps, different positions of stations, etc., the system should be able to handle a 60 dB optical loss between any transmitting and receiving points. As well, the receivers must be able to handle multiple signals differing by up to 40 db in optical strength.
6. Although only 3 stations are required to demonstrate a basic tele-

phone system, the parameters and design specifications are to be based on a system with up to 100 stations.

7. It should be possible to change cable lengths and interchange stations without extensive electronic adjustments.

The format of the optical signals was chosen to be analog. This was done for simplicity and because of numerous technical problems encountered when trying to use a clock sync signal over the same link as the data, and over varying lengths of travel. The analog electrical data signals would intensity modulate the light from a suitable optical source. This is different from amplitude modulation in that the modulated intensity can never be less than zero. If all of the optical sources are to operate on the same optical wavelength, then the multiplexing must be done on the electrical data signal. This is done by using radio frequency subcarriers of different frequency as the different data channels. For the sake of simplicity, the voice signals would be amplitude modulated onto the appropriate RF subcarriers. Because of the availability of off the shelf components for the citizen's band frequency range (26.5 MHz - 27.3 MHz), the subcarrier frequencies were chosen from this range.

Once the subcarrier multiplexing had been chosen, a number of solutions become possible to the problem of establishing a conversation link between stations. One solution is to have each station contain the logic necessary to establish a link, provide the audio cues, etc. and the link is made by the station initiating the call. For an N station system, this can be implemented by each station containing its

own unique transmitting subcarrier channel but N possible receiving channels. The caller then receives on the called party's transmitting channel and tells the called party which receiving channel he should use. An N transmitter/1 receiver station cannot be used since a busy signal could not be produced.

Another approach is to use a separate "central" switching station where the links are made. The caller then dials the central station, identifying the called party and the central station activates the appropriate switched connections to link the caller and the called party. It is likely that there would be enough optical reflection in the system such that a significant fraction of the signal transmitted from a station will return to the receiver. If the receiving channel and transmitting channel for each station are the same, this reflected signal could swamp out the conversation. This could be avoided by using a talk/listen switch, but this would violate requirement #1. Instead, separate transmit and receive channels could be used. This is the case with the finished system. Now, 2N subcarrier channels are needed for an N station system.

This second approach was chosen for a number of reasons. With the central processor (C.P.) system, extra stations can be added without changing the existing stations. The individual stations are also much simpler, and this system as a whole is more easily adaptable for linkup with a commercial telephone system. Also, it is the cheapest to produce.

This C.P. version is similiar to a commercial telephone system. On the commercial system, the various "stations" produce different voice

signals on different wires leading to the central switching unit. These signals are all in the same frequency range (audio baseband), and the central switching unit puts the voice signals onto the appropriate outgoing wire. In this optical system, the different voice signals occupy different frequencies, but all on the same "wire". The C.P. then switches the voice signals onto the appropriate ougoing frequency.

The present system used near infrared LED's as the optical source. Either PIN photodiodes or avalanche photodiodes could be chosen as the detector. To avoid the high voltage power supplies required by an avalanche photodiode, PIN photodiodes were chosen.

Initially, multifibre optical cables were to have been used because the availability of couplers and the ease of making splitters. However, the recent development of fused splitters and couplers for single fibres offer lower loss and more flexability in splitting ratios. For these reasons, single fibre cable was used. Because of the short distances over which this cable would be used, dispersion is not a problem. Therefore, the choice between graded index or step index fibre was made only on availability.

There are three possible layout configurations for the optical cable: the star, the line (main trunk) and the tree (a combination of the star and the line).

In the star system, the losses increase linearly with N and all of the signals are roughly the same amplitude at a given receiver. However, the layout is not very flexible, and requires a larger quantity of fibre than the other two layouts.

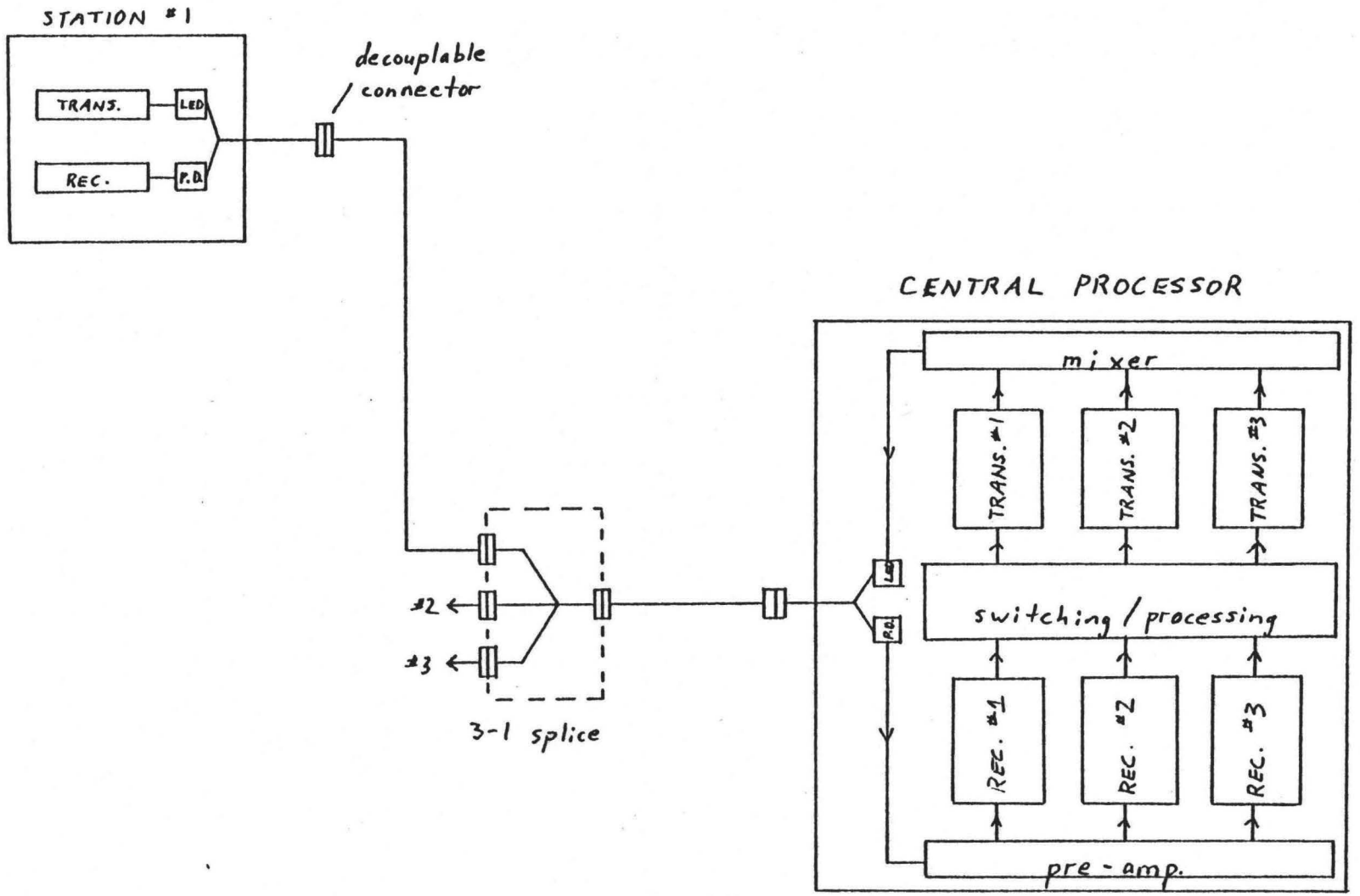


Fig. 1 Layout of Optical Fibre Telephone System

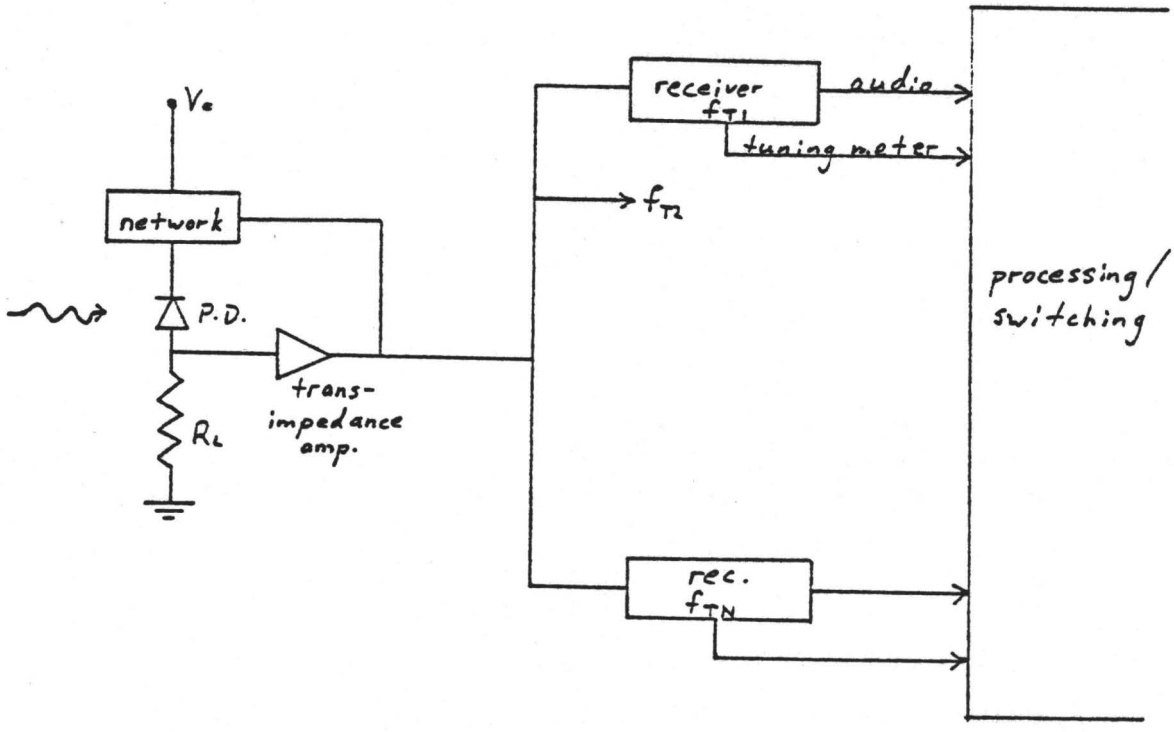
The linear, or main trunk, configuration requires the least amount of cable. However the dynamic range of the signals and the loss at the weakest station increase exponentially with N, due to consecutive tapping.

The tree configuration, which is normally used for CATV, has most of the advantages of the star and linear configurations. This was the configuration chosen.

As shown in Fig. 1, the geometry of the fibre in this tree lay-out takes the shape of a multi-branched "Y". The central processor which does the switching between the various subcarriers is situated at the base of the main arm of the "Y". A single fibre enters each of the telephone stations and the central processor. Inside these units, a fused fibre splice divides the light into two separate fibres. At the end of one of these fibre segments is an LED. Suitably modulated light is produced here and propagates out through the 2-1 splice into the tree. The other fibre segment runs into a photodiode. These detect the signals that have been modulated onto the light coming off the tree.

Each telephone station has an optical receiver consisting of a photodiode followed by an A.M. radio receiver and an optical transmitter consisting of an infrared LED at the output of an A.M. radio transmitter. A telephone station identifies the station to which he wants to speak by means of an ordinary telephone dial switch. This switch is used to interrupt the subcarrier coming from the calling station. The C.P. senses these interruptions and makes the necessary switched connections.

The central processor also uses a photodiode in its optical receiver and an LED in its optical transmitter. However, here there



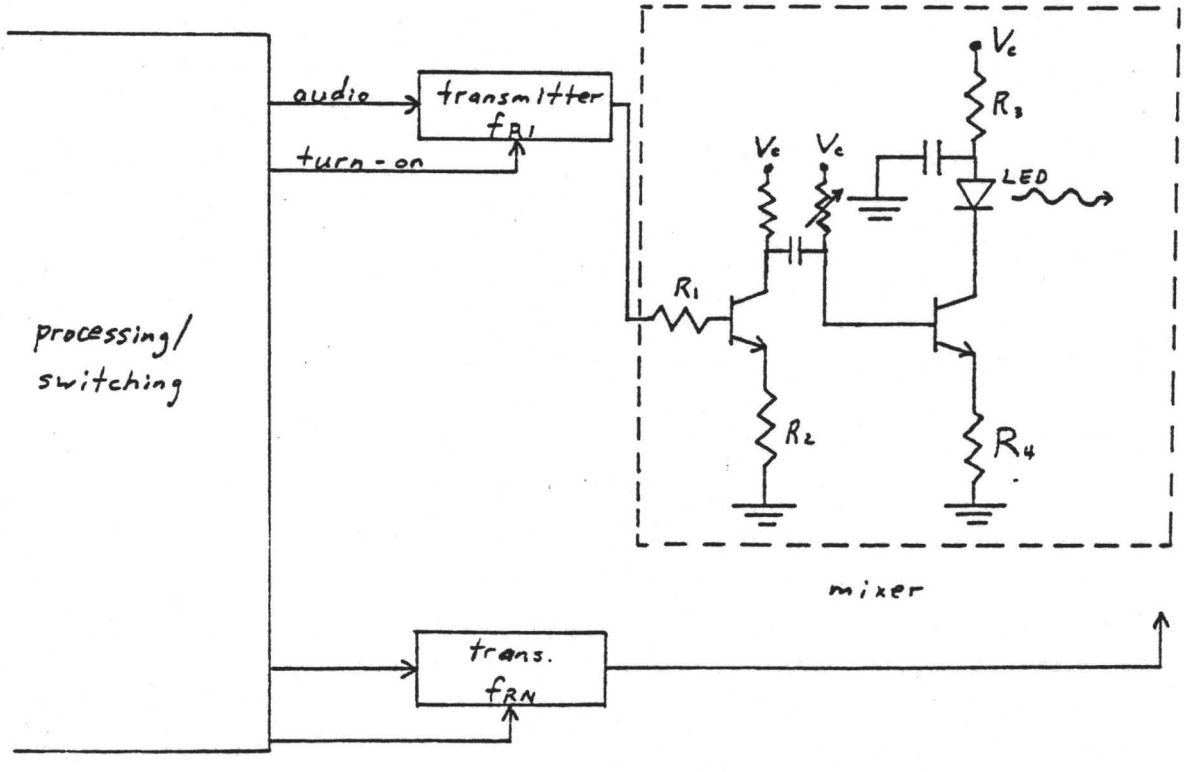


Fig. 2 Central Processor for O.F.T.S.

are N radio receivers and N radio transmitters interfacing with these opto-electronic components. In the C.P., there is a receiver/transmitter pair corresponding to each of the N stations. The C.P. receiver for a station is tuned to the subcarrier that the station transmits on and its C.P. transmitter is tuned to the subcarrier that the station receives on. The central processor is shown in Fig. 2.

Between the radio receiver bank in the C.P. and the radio transmitter bank, there is a switching network. When one station dials the phone number of another station, the C.P. counts the subcarrier interruptions. With this information, the proper audio switch is closed to connect the audio output of the C.P. receiver corresponding to the calling station with the audio input of the C.P. transmitter corresponding to the called station. Another switch is simultaneously closed to connect the reverse path. The same control signal that operates the audio switches also turns on the C.P.'s transmitter to the called party. When the called party's phone senses this subcarrier turn on, ringing stops and two way conversation takes place through the C.P. As well as the basic network of audio switches, the C.P. also contains the TTL logic controlling the switching and the various audio cues (dial tone, busy tone, ring tone). This logic is such that these tones are heard under the same circumstances as in a commercial telephone system.

The work on this project was divided into three sections:

(1) switching logic and peripherals - J. Goodwin

(2) optical fibre, splitters and couplers - G. Duck

(3) analog electronics - A. Jurenas

Parts 1,2 and 3 are described in detail in the reports Goodwin, Duck and Jurenas. The system with three telephones, C.P., power supplies and interconnections is operational, and is now undergoing detailed evaluation. The latter work is being done by V. Tzannidakis, who will report on it at a later date.

AMENDMENT TO CHAPTER 1

Due to the complexity of the analog electronics, it shall be described in two reports. This first report, entitled 'Analog Electronics', will describe and explain the theory of operation of the subsystems and individual circuits which comprise the analog electronic portion of this project. The second report, entitled 'System Analysis' will examine the operation of the more complex circuits in greater and more theoretical detail. It will also describe a preliminary evaluation of the system operation, modifications to the Central Switching and Logic Circuitry, and an analysis of the system configuration, with an emphasis on areas requiring further development work. The report of V. Tzannidakis will deal with an alternative system configuration with respect to signalling, channel switching, and frequency allocation.

CHAPTER 2

STATION ELECTRONICS

I. GENERAL DESCRIPTION

The station consists of a modified Northern Electric Telephone Desk Set, Model NE-500. A block diagram of the station is shown in Figure 3. The modifications made include the following:

(a) The standard handset shell is replaced by one (ITT part number 5402-10-0700) which is identical, except for a removable access plate on the inside of the handgrip area;

(b) The standard 4 wire, 4 foot telephone handset cord is replaced by a 6 wire, 6 foot cord (N.E. part number H6E-03), which is terminated in a motherboard plug;

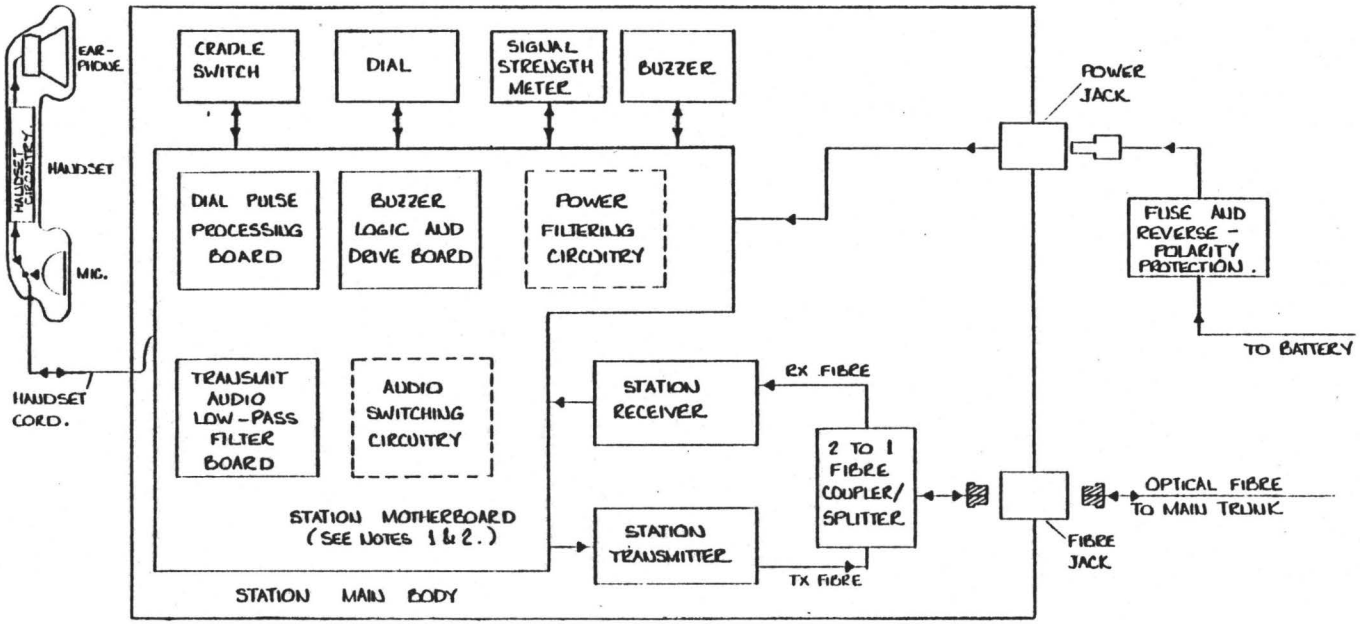
(c) The bell, anti-sidetone transformer, terminal block, and main telephone cord are removed from the main body of the desk set;

(d) A fibre-optic jack, a 2 to 1 fibre-optic coupler, the station transmitter and receiver, a buzzer, a power jack, and the station motherboard, are installed inside the desk set;

(e) The dial and cradle switch are rewired, and fitted with motherboard plugs;

(f) A signal strength meter is installed inside the desk set shell, and terminated with a motherboard plug.

The transmitter is installed beneath the dial. The receiver is installed in the rear of the desk set, behind the cradle switch. The motherboard is installed between the transmitter and the cradle



NOTES. 1. CIRCUITRY SHOWN WITHIN DASHED LINES IS PART OF THE MOTHERBOARD.
2. CIRCUITRY SHOWN WITHIN SOLID LINES IS CONTAINED ON SEPARATE DAUGHTER-BOARDS WHICH ARE MOUNTED ON THE MOTHERBOARD.

FIGURE 3 STATION BLOCK DIAGRAM.

TABLE 1

STATION COMPONENT NUMBERING SCHEME

Circuitry or Device	Number Series
Handset Circuitry (Excluding Transmit Audio Processor)	100's
Tx. Audio Processing Circuitry (Inside Handset)	200's
Tx. Audio Low Pass Filter	300's
Motherboard	400's
Buzzer Logic and Drive Circuitry	500's
Dial Pulse Processing Circuitry	600's
Plugs To Receiver	700's
Motherboard Jacks To Any of the Above Circuits or Units	*4#0's

* # represents the first digit of the number series of the circuitry being connected by the jack. For example, motherboard jacks to the Tx Low Pass Filter are numbered 430's.

switch. The 2 to 1 fibre-optic coupler is mounted on top of the receiver. The fibre-optic and power jacks are installed on the right side of the station main body.

The components on the various circuit boards inside the main station body, and the station handset, are numbered according to Table 1. Note that the transmitter and receiver are treated as independent units with their own numbering schemes.

II. TRANSMITTER

(i) General

The transmitter produces the RF (radio frequency) subcarrier, AM modulates it, and amplifies and buffers it sufficiently to drive an LED. The output of the LED is infra-red light, intensity modulated (IM) according to the AM modulated subcarrier. A block diagram of the transmitter is shown in Fig. 4. A crystal controlled oscillator produces the RF subcarrier, which is amplified by IC1. Transmit audio and dial pulse information, fed into the Gain Control input of IC1, cause the subcarrier to be AM modulated accordingly. The modulated subcarrier is amplified, and then fed to an LED driver. The output of the LED driver is a current proportional to the AM modulated subcarrier. Since the output power (or intensity) of an LED is proportional to the input current, the LED output is an intensity modulated light frequency carrier. The purpose of the 'Gain Control Quiescent Point Adjustment' and the 'Level Adjustment and High Series

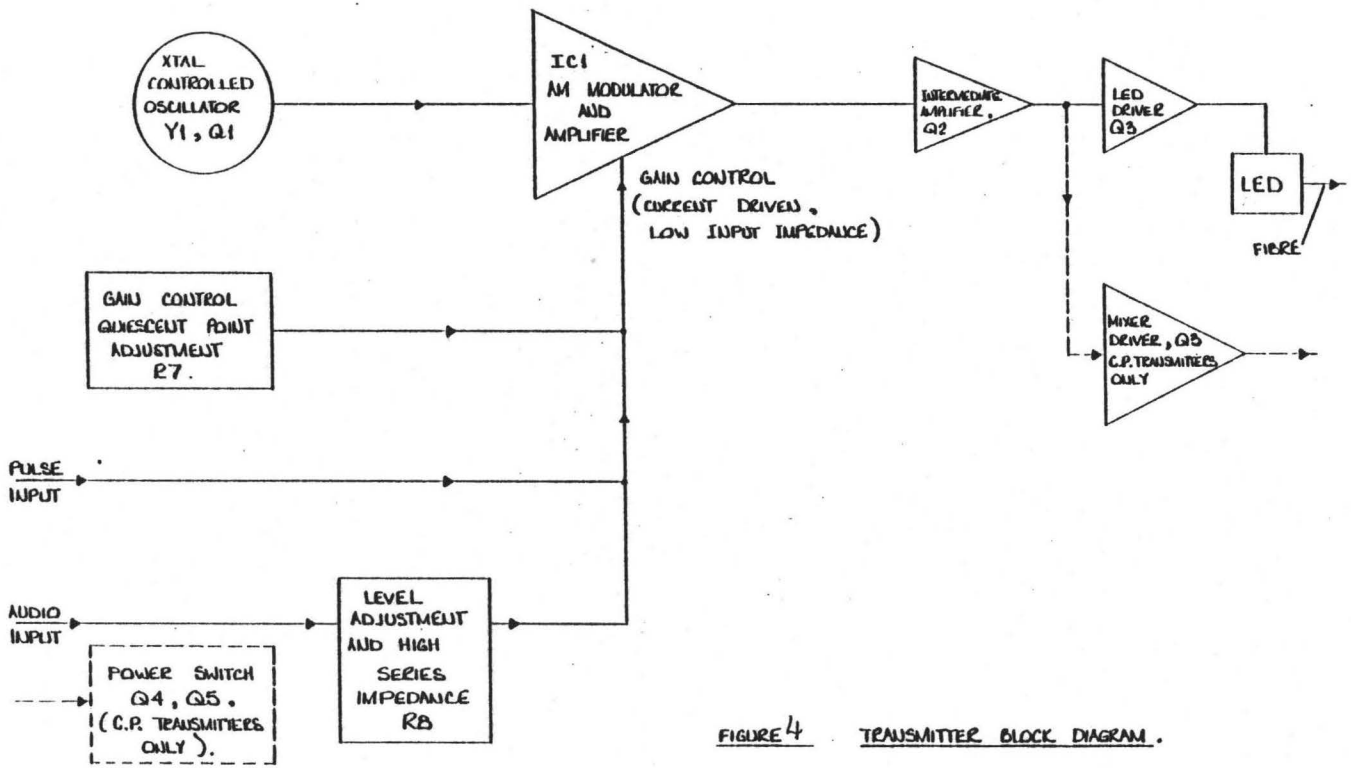


FIGURE 4 TRANSMITTER BLOCK DIAGRAM.

Impedance' is to adjust the index, and to optimize the linearity, of the subcarrier modulator.

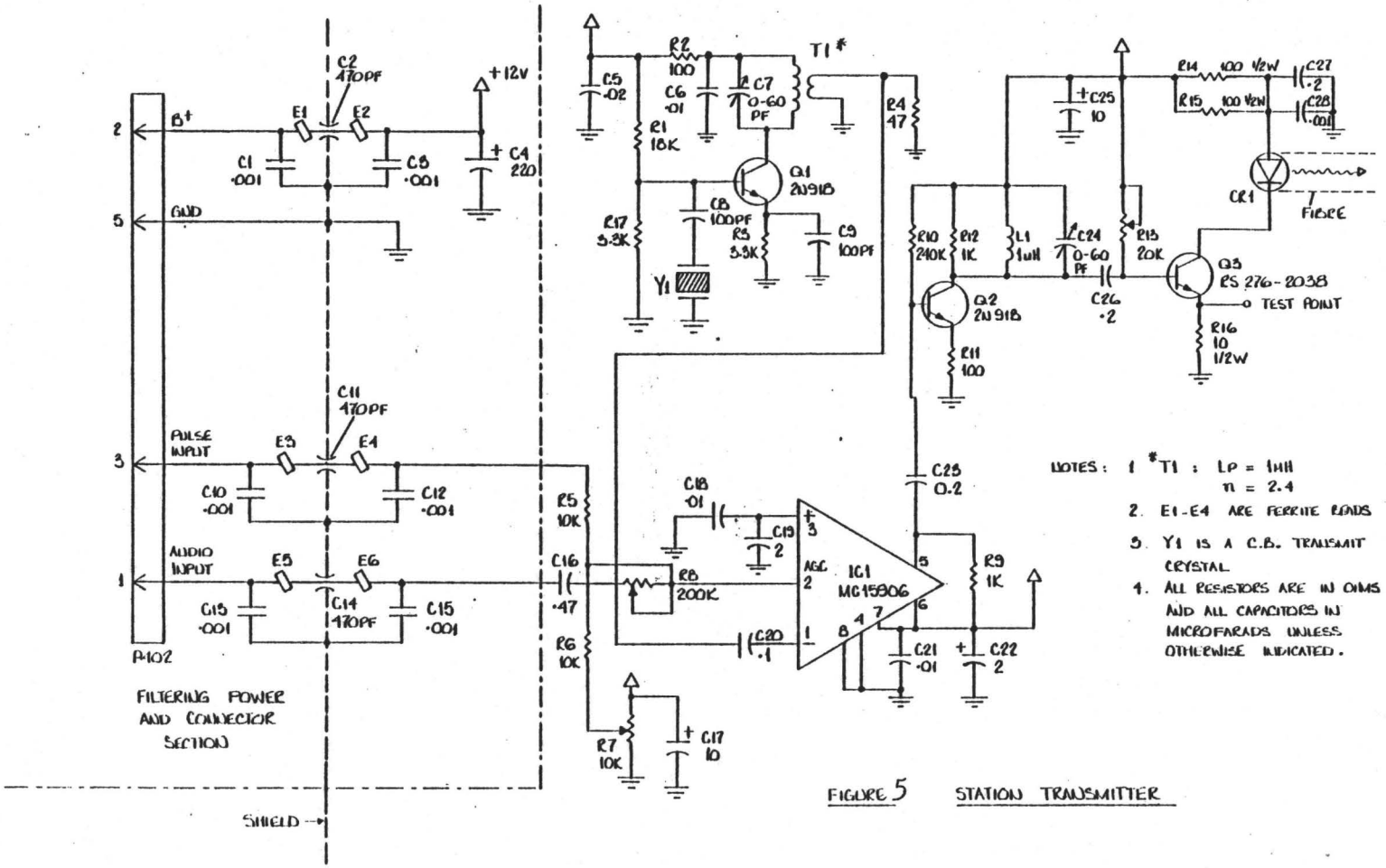
The transmitter circuitry is installed in an enclosure made of 24 gauge copper.

(ii) Detailed Description

A schematic diagram of the transmitter is shown in Fig.5.

The main components compromising the oscillator which generates the RF subcarrier are Q1, Y1, T1, C7, C8, and C9. These, along with other components for biasing, etc., form a Hartley oscillator. Both the crystal Y1, and the tank circuit made up of C7 and the primary of T1, must be inductive for the circuit to oscillate. Since the crystal impedance is inductive only over a very narrow band of frequencies about the nominal frequency, the oscillator frequency is determined by the crystal. A sketch of the output amplitude of the oscillator versus the value of C7 is shown in Fig. 6. The point where $C7=C_{RES}$ is where the tank circuit is tuned to the crystal frequency. The oscillator is stable only on the more gradually sloping portion of the curve (i.e. where C7 is less than C_{RES}), and so C7 is adjusted to place the operating point in that range. The exact operating point is determined by the required output amplitude, which in turn depends on the gains of all the following stages.

The RF voltage developed across the tank circuit is reduced by a factor of 2.4, and then routed to pin 1 of IC1. R4 provides additional loading on the secondary of T1 to keep the voltage at low



NOTES:
1. *T1 : LP = 1HH
   n = 2.4
2. E1-E4 ARE FERRITE BEADS
3. Y1 IS A C.B. TRANSMIT CRYSTAL
4. ALL RESISTORS ARE IN OHMS AND ALL CAPACITORS IN MICROFARADS UNLESS OTHERWISE INDICATED.

FIGURE 5 STATION TRANSMITTER

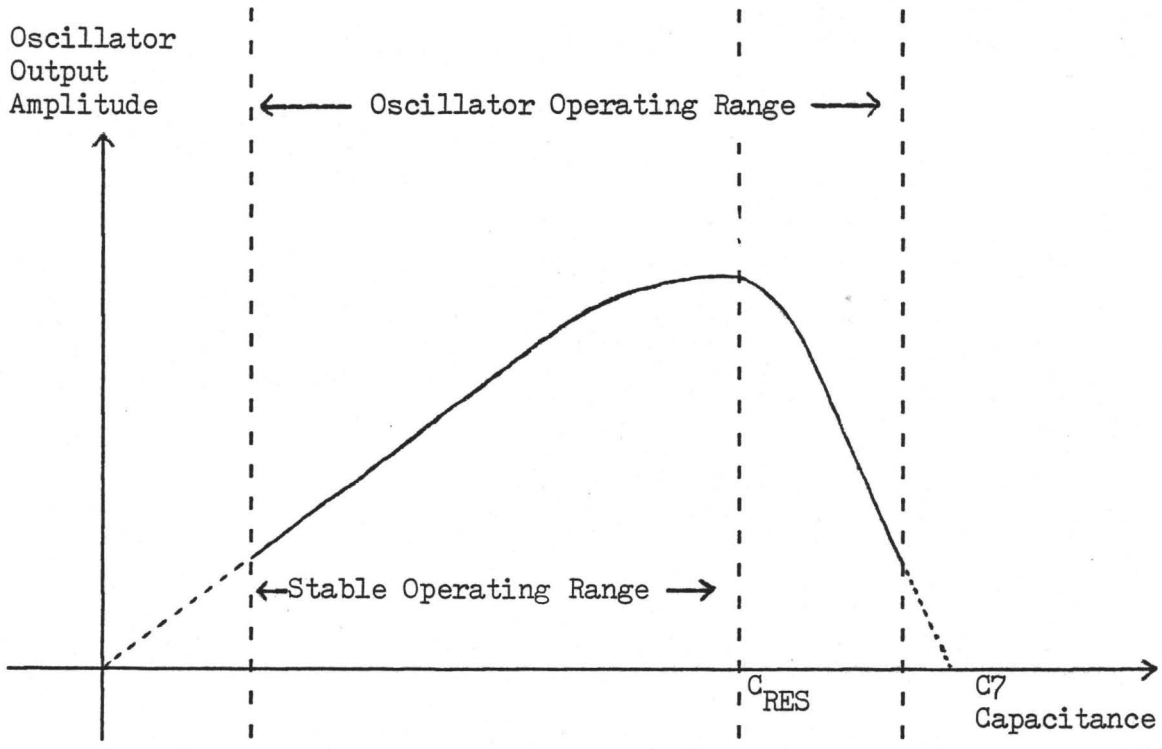


Figure #6
Oscillator Operating Characteristic

levels. For linear and stable operation, the input at pin 1 of IC1 must not exceed 200 mV.

IC1 is a Motorola MC1590G 'High Gain RF Amplifier with Wide Range AGC'. It is used as an amplifier and an AM modulator. The input current to pin IC1-2, the AGC input, controls the gain of IC1. For a certain range of values of input current to pin IC1-2, the RF level at the output of IC1 will be a linear function of that current. It is over this range that amplitude modulation can take place. Pin

IC1-2 is an inverting input. This means that the gain decreases with increasing input current. The input impedance at pin IC1-2 is a 70 ohm series resistance tied to half the power supply voltage.

The quiescent (i.e. no modulation) operating point of IC1 is centered in the aforementioned linear gain control region by potentiometer R7. The voltage from R7 is converted to a current by R6, and is fed into pin IC-2. Voltage pulses applied to terminal 3 of plug 402 are converted to current pulses by R5 and are also applied to pin IC1-2. Because IC1-2 is an inverting input, positive pulses at terminal P402-3 will attenuate the subcarrier for the duration of the pulse. Series resistors R5 and R6 also serve to prevent the pulse source and R7 from loading or interfering with each other.

Transmit audio from a low impedance source is applied to terminal P402-1. It is converted to a current signal by R8, and then fed to pin IC1-2. R8 also functions as a means of fine adjustment of the modulation index. However, the value of R8 is always set to more than 150 kilohms to ensure that pin IC1-2 sees a high impedance (i.e. current) audio source.

The output of IC1 appears across load resistor R9. The RF signal is then fed to intermediate amplifier Q2, which is connected in a common-emitter configuration. Emitter resistor R11 linearizes the gain characteristics of Q2. The gain of that stage is therefore (R12//L1//C24)/ R11. The tank circuit comprised of L1 and C24 serves to tune out the output capacitance of Q2, and also to filter out any harmonics or other undesired frequencies.

The output of Q2 is fed to the LED driver Q3, which is connected

in a common-collector configuration. Both the voltage across emitter resistor R16, and the collector current of Q3, are proportional to the voltage at the base of Q3. R16 also prevents Q3 from loading down the output of the previous stage by increasing the input resistance at the base of Q3. The collector of Q3 is connected to the cathode of LED CR1. The optical output of the LED is proportional to the current flowing through it, and therefore the optical output is proportional to the voltage at the base (or emitter) of Q3. R13 sets the level of the D.C. bias current through Q3 and CR1 (typically about 100 mA). R14 and R15 take up part of the voltage drop between the power supply and the collector of Q3 to reduce the power that Q3 must dissipate. Q3 is fitted with a heat sink. C27 and C28 provide a RF ground at the anode of CR1. The transmit output fibre is permanently bonded to LED CR1, and is routed through a small aperture in the transmitter enclosure. The power and signal inputs are routed in through P402 and the 5 pole, π section, low pass filters. C4 provides power supply filtering.

III. RECEIVER

(i) General

The receiver consists basically of a front-end section, and the main receiver section. A block diagram of the receiver is shown in Fig. #7. The front-end section consists of a photodiode stage, a variable gain RF amplifier, and a secondary AGC circuit. The main receiver section consists of an integrated circuit AM receiver subsystem, an external IF stage, an audio output stage, and various other circuitry required by the subsystem.

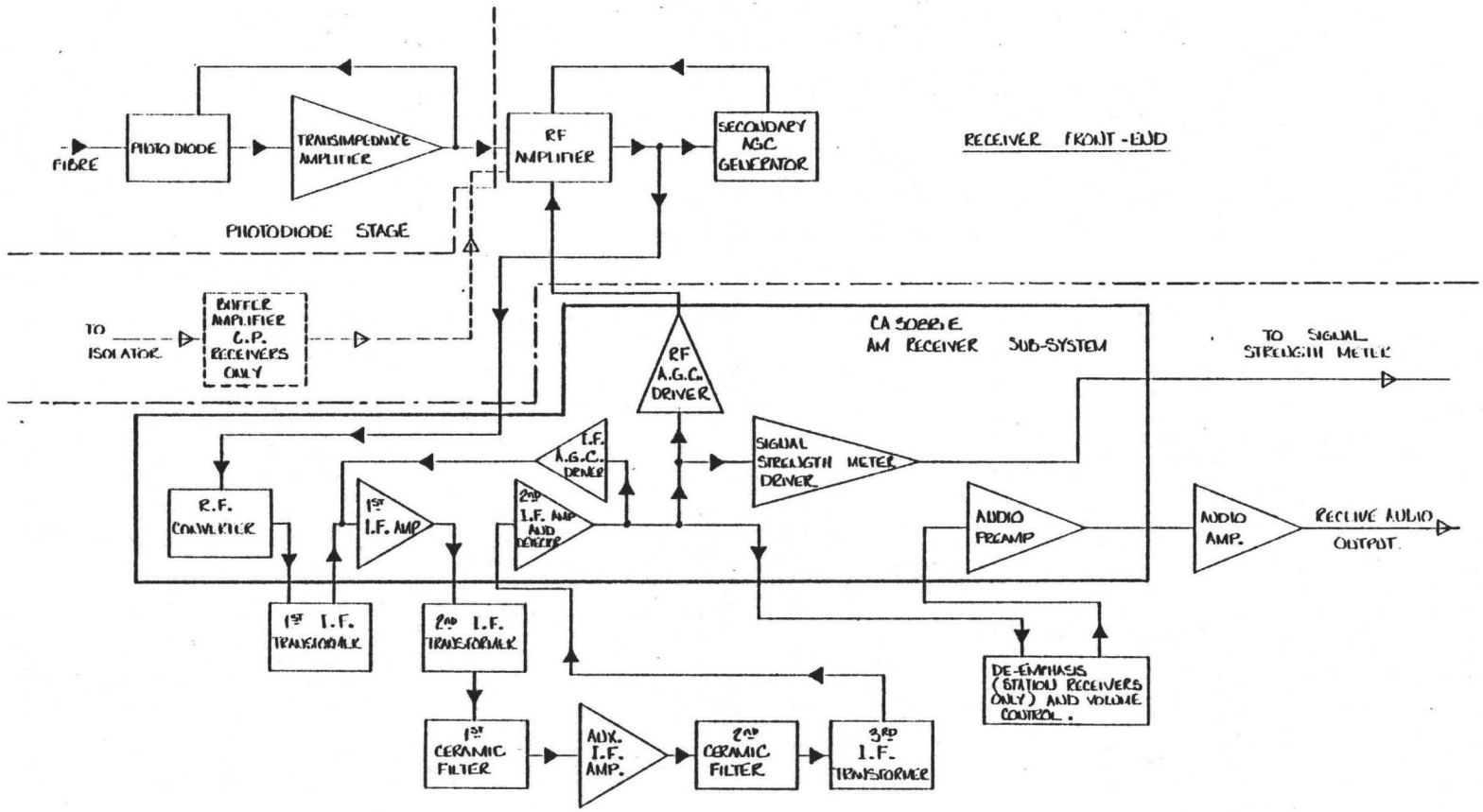


FIGURE 7 RECEIVER BLOCK DIAGRAM

The photodiode stage contains a photodiode which converts incoming light to an electrical current, and a transimpedance amplifier which converts the current signal to a voltage signal and also provides feedback. The purpose of the feedback is described in the next section. The signal is then applied to an RF amplifier, whose gain is controlled by signals from both the AM receiver subsystem, and the secondary AGC circuit. The AGC signal from the subsystem is dependent only on the level of the desired signal, while the secondary AGC circuit responds to all signals within the RF (as opposed to IF) passband. The secondary AGC prevents strong signals in other channels from overloading the converter stage of the subsystem. The signals of other channels are not filtered out until passing through the IF sections of the subsystem.

The signal is routed from the front-end to the AM receiver subsystem. This integrated circuit contains a converter (combination local oscillator and mixer), two IF amplifiers, an envelope detector, AGC and signal strength circuits, and an audio preamp. An external IF amplifier is provided, thus equipping the receiver with a 3 stage IF section. This IF section uses three IF transformers, and two ceramic filters, as shown in Fig. 7. The detected signal drives the following three control circuits: the signal strength meter driver, which produces a low impedance output proportional (but not linearly) to the signal level; the IF AGC driver, which controls the gain of the first IF stage; and the RF AGC driver, which provides a delayed AGC signal to the RF amplifier. The

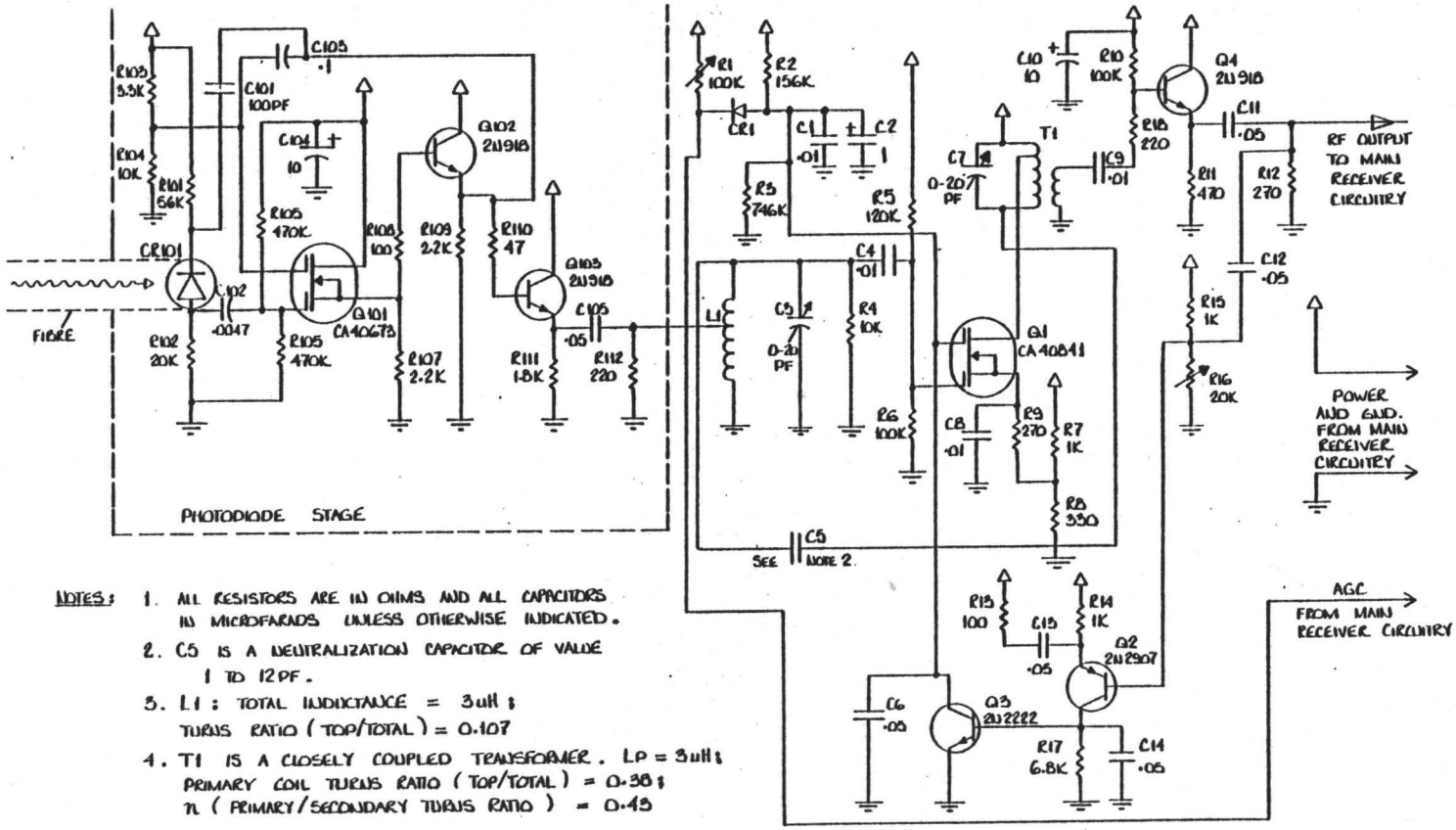
detected signal is then routed through external volume control and deemphasis circuits, through the subsystem audio preamp, and finally to the external audio amplifier.

The receiver circuitry is installed in an enclosure made of 24 gauge copper. The front end and the main receiver sections are separated within this enclosure by a copper shield.

(ii) Detailed Description

Receiver, Front End

A schematic of the receiver front end is shown in Fig. 8. The receive input fibre enters the receiver enclosure through a small aperture, and terminates at the photodiode, to which it is permanently bonded. The photodiode CR1 is reversed biased through R101 and R102. R102 is the load resistor, and R101 is used to isolate the cathode of CR101 from A.C. ground. When light from the fibre impinges on the photodiode, a current proportional to the light intensity flows through CR101 (into the cathode and out of the anode). When there is an absence of light from the fibre, a minute 'dark' current (approximately 0.5 nA) always flows through CR101 in the same direction. Due to the small magnitude of the current (both 'dark' and 'light') through CR101, there is only a small voltage drop across R101 and R102 (less than one volt), and so CR101 remains reversed biased by almost the full power supply voltage at all times. The photodiode is of the PIN type. An important feature of a PIN photodiode is that the internal diode



NOTES:
1. ALL RESISTORS ARE IN OHMS AND ALL CAPACITORS IN MICROFARADS UNLESS OTHERWISE INDICATED.
2. C5 IS A NEUTRALIZATION CAPACITOR OF VALUE 1 TO 12 PF.
3. L1: TOTAL INDUCTANCE = 3uH; TURNS RATIO (TOP/TOTAL) = 0.107
4. T1 IS A CLOSELY COUPLED TRANSFORMER. LP = 3uH; PRIMARY COIL TURNS RATIO (TOP/TOTAL) = 0.38; n (PRIMARY/SECONDARY TURNS RATIO) = 0.45

FIGURE 8 RECEIVER FRONT-END AND PHOTODIODE STAGE.

capacitance, which shunts the diode current source, is relatively constant and independent of the voltage applied across the diode (when reverse biased). If this were not so, the diode capacitance, which is effectively in parallel with load resistor R102, would vary with the signal. The voltage across R102 would then be a non-linear function of the diode current, and intermodulation distortion would result.

The signal across R102 is fed to gate #1 of Q101, a dual-gate Mosfet. Q101 is connected in a source follower configuration. The output signal at the Q101 source is fed through R108 to Q102, which is connected in an emitter-follower configuration. The output signal is then routed through R110 to Q103, another emitter follower, and finally, out of the photodiode stage through C105. Since the source and emitter followers have approximately unity voltage gain, the output signal has approximately the same A.C. voltage magnitude as the signal across R102, but with a much lower source impedance (approximately 10 ohms). R108 and R110 were required to prevent Q102 and Q103 from oscillating, which can occur when emitter followers drive capacitative loads.

The load impedance seen by the photodiode consists of R102, the internal capacitance of CR101 (about 2pF) the capacitance (about 3pF) between gate #1 of Q101 and the source of Q101, and the capacitance (about 3pF) between gate #1 of Q101 and gate #2(which in turn has a capacitance of about 3pF between itself and the drain). The effect of these capacitances is reduced by using positive

feedback for the Miller effect. Referring to the A.C. voltage across R102 as the V_{IN}, the voltage at the emitter of Q101 is $A_1 V_{IN}$, where A_1 is approximately unity. Therefore, the effective capacitance between gate #1 and the source of Q101 is reduced by a factor of 1/(1-A) by the Miller effect. The voltage at the emitter of Q102 is $A_1 A_2 V_{IN}$, where A_2 is also approximately unity. This signal is applied to the cathode of CR101 and gate #2 of Q101. The effective internal capacitance across CR101 is reduced by a factor of $1/(1 - A_1 A_2)$. As explained earlier, R101 isolates the cathode of CR101 from A.C. ground so that feedback could be applied. Note that if feedback wasn't being used, R101 would actually increase the effective diode capacitance by the Miller effect, since the voltage across R101 would be of the opposite polarity (with respect to CR101) as V_{IN}. As with the diode capacitance, the effective capacitance between gate #1 and gate #2 is reduced by $1/(1 - A_1 A_2)$.

The signal is routed from the photodiode stage to a tap on L1. The signal magnitude is increased by a factor of 10 by the tapped tank circuit composed of L1 and C3. This signal is applied to gate #1 of Q1, which is connected in a common source configuration. Gate #2 of Q1 is A.C. grounded, thus isolating gate #1 from the drain, and avoiding the need for neutralization. The drain of Q1 is connected to the tapped tanked circuit composed of C7 and the primary of T1. The voltage across the secondary of T1 is approximately 10 times the voltage at gate #1 of Q1. C5 neutralizes stray coupling between L1 and T1. The signal is next passed through emitter follower

Q4 and routed to the main receiver circuitry.

The output of Q4 is also routed to the base of Q2. The RF signal at the base of Q2 is rectified at the emitter by C13, R13, and the emitter-base diode. The D.C. voltage at the emitter, which corresponds to the signal level, is amplified by a factor of 6.8, and appears across R17. A bias voltage, determined by the setting of R16, also appears across R17. When the voltage across R17 reaches about 0.5V (corresponding to an RF signal level of 50 mV-RMS at the emitter of Q4), Q3 is turned on which reduces the bias voltage at gate #2 of Q1. This is the Secondary AGC action.

When gate #2 of Q1 is biased for a gate #2 to source voltage of more than 4 V D.C., Q1 operates at full gain. When the gate #2 to source voltage is reduced to less than 4 V, the gain of Q1 is reduced proportionately. The maximum gain reduction is about 30 db. The gain control signals to gate #2 come from the collector of Q3 (in the manner described in the preceding paragraph) and from AGC circuitry (referred to as Primary AGC) in the main receiver section. The latter signal is produced by a current source, and the Primary AGC voltage is developed across R1. The setting of R1 determines the range of the Primary AGC voltage. CR1 isolates the Primary AGC circuit from the Secondary AGC circuit.

Receiver, Main Circuitry

A schematic of the main receiver circuitry is shown in Fig.9. A schematic of the RCA CA3088E integrated circuit is shown in Fig. 10.

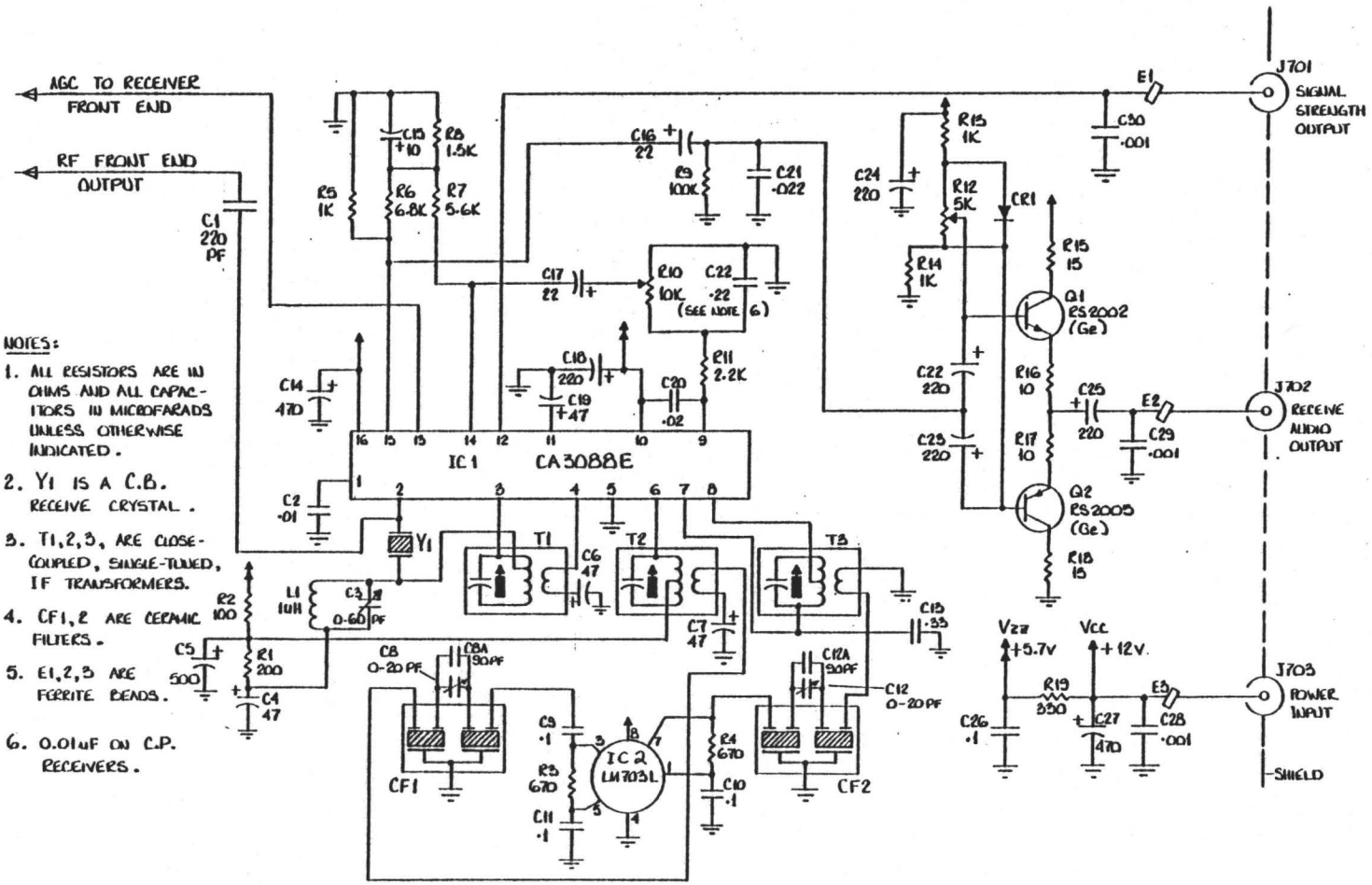


FIGURE 9 RECEIVER MAIN CIRCUITRY

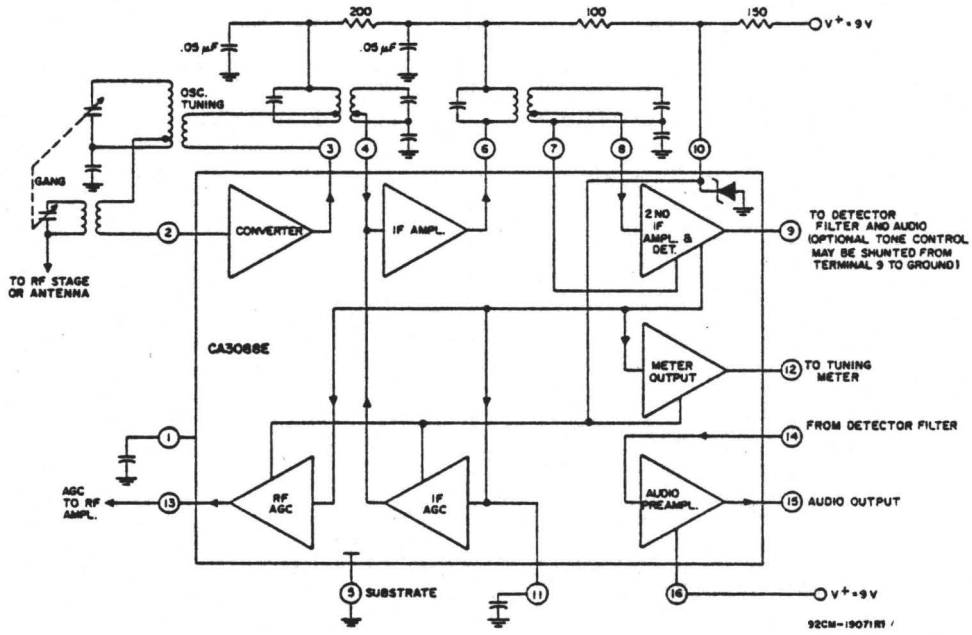


Fig. 10(a) *-Functional block diagram of the CA3088E.*

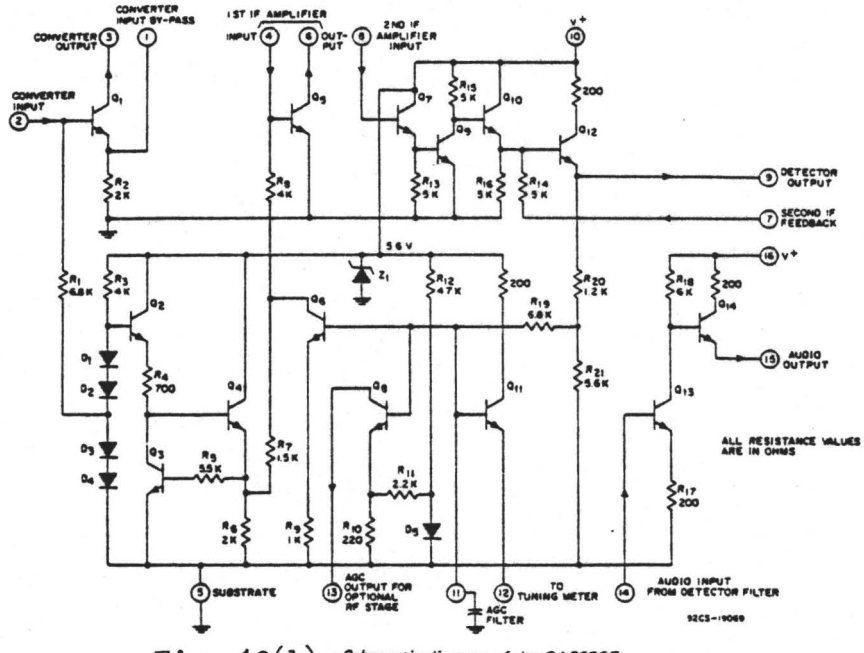


Fig. 10(b) *-Schematic diagram of the CA3088E.*

(After p. 455, Ref. 5)

*In a typical AM Receiver Unit

A detailed description of the theory of operation of the CA3088E can be found in the RCA books 'Linear Integrated Circuits - Selection Guide/Data' and 'Linear Integrated Circuits - Application Notes', and will not be given here. When a reference is made, in the following text, to a component on the CA3088E, as per Fig. 10, the label of the component will have the subscript 'I.C.' added to it.

The signal from the front-end is fed into pin IC1-2, which is the converter input. $Q1_{I.C.}$, together with crystal YI, and the collector tank circuit composed of L1 and C3, form a Pierce oscillator. Its tuning and stability characteristics are similar to that shown in Fig. 6 for the transmitter. By inserting IF (455 KHz) transformer T1 between the collector of $Q1_{I.C.}$ and its tank circuit, and by appropriate biasing on the CA3088E, $Q1_{I.C.}$ also functions as a mixer. The mixer products at the IF frequency appear across the primary of T1, a single-tuned close-coupled transformer. The output from the secondary is routed to pin IC1-4, the input of the first IF amplifier. The output of the first IF amplifier from pin IC1-6 is applied to the primary of T2, also a close-coupled single-tuned transformer. The output of the secondary of T2 is routed to ceramic filter CF1. CF1 consists of two three-electrode ceramic resonators, coupled by C8 and C8A. The output of CF1 is applied to IC2, an auxiliary IF amplifier consisting of a National Semiconductor LM703L differential amplifier. R3 provides the correct matching impedance for CF1, and R4 is the load impedance of IC2. The output of IC2 is routed through CF2, which is identical

to CF1. The output of CF2 is routed to the secondary of T3, another close-coupled single-tuned transformer. The signal from the primary of T3 is applied to pin IC1-8, the input of the second IF amplifier. After amplification, the signal undergoes envelope detection by $Q12_{I.C.}$, and appears at pin IC1-9. R11 and C20 form the detector filter.

From the detector filter, the signal passes through the volume control and low pass/de-emphasis circuit composed of R10 and C22. The values of C22 and R10 are such as to provide a 300 microsecond de-emphasis on the received audio in the stations. The de-emphasized audio is now routed to pin IC1-14, the input of the audio preamplifier. The output of the audio preamplifier appears at pin IC1-15. From here it is routed through C16 to the audio amplifier. The signal at pin IC1-15 is also applied to the feedback circuit composed of R6, R7, R8, and C15. The output of this circuit is fed back to audio preamplifier input, pin IC1-14, in order to establish the proper bias levels for $Q13_{I.C.}$ and $Q14_{I.C.}$. R5 increases the bias current through $Q14_{I.C.}$ to enable it to handle larger signals (up to 2 Vpp). C19 is the AGC filter. Delayed AGC is routed to the front-end from pin IC1-13. The signal strength meter output at pin IC1-12 is routed to jack J701.

The audio amplifier consists of a complementary germanium transistor pair, Q1 and Q2, connected in an emitter follower push-pull configuration. The input audio signal is applied to both bases through C22 and C23. The transistors are biased for class AB

operation. This avoids the crossover distortion of class B amplifiers and the excessive power consumption of class A amplifiers. Class AB operation requires that Q1 and Q2 be biased just at the cutin voltage (0.1 V). This is accomplished by the base biasing circuit consisting of R12, R13, R14, and CR1. By adjusting R12, the voltage difference between the bases of Q1 and Q2 can be adjusted to obtain the required biasing. R15 and R18 reduce the voltage drop across the transistors, and thereby the amount of heat they must dissipate. R16 and R17 provide a slight amount of D.C. feedback to prevent thermal runaway. The final audio is routed through C25 to J702.

Power enters through J703 and is filtered by C27. IC1 contains a 5.7 V Zener diode, which is connected to pin IC1-10, and provides a regulated internal voltage for IC1. The drop from power supply to 5.7 V takes place across R19, and C26 and C18 provide additional filtering.

RF is prevented from entering or leaving the receiver by three 3-pole low-pass filters. Each π section filter is formed by a capacitor (C28, C29, C30), a bead (E1, E2, E3), and the inherent capacitance of each jack.

IV TRANSMIT AUDIO PROCESSING

(i) General

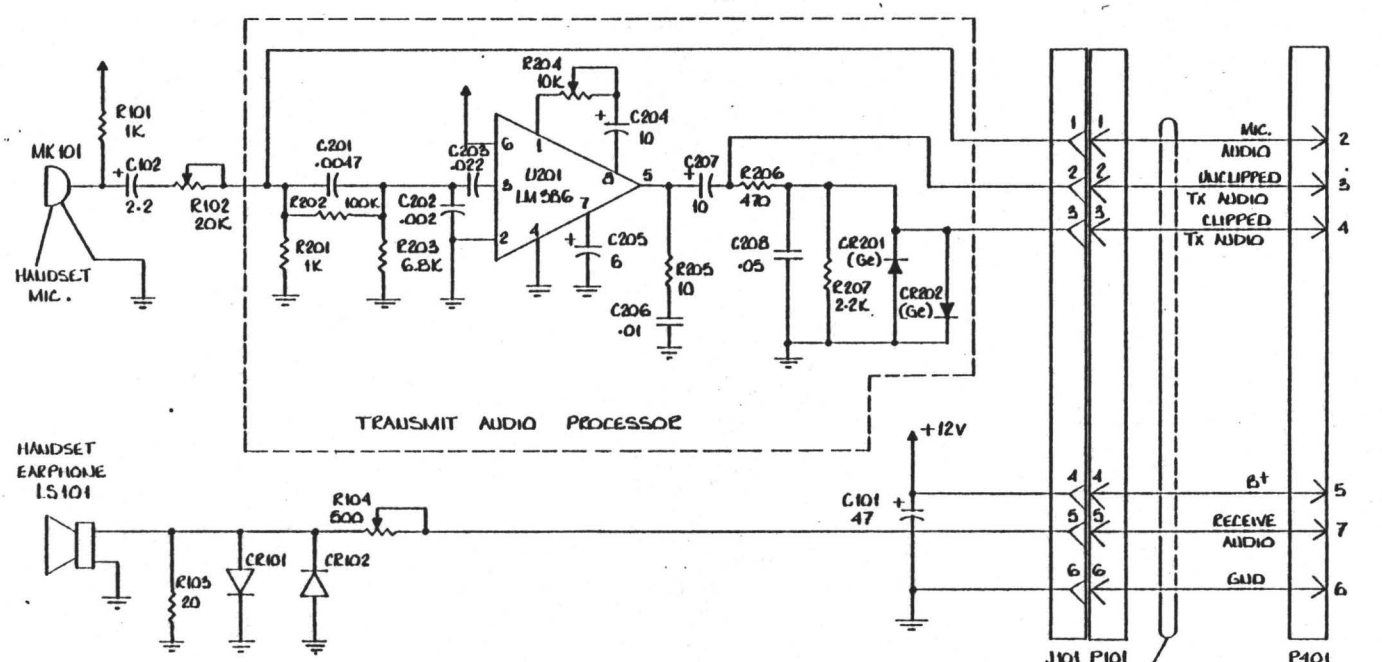
Refer to the Station Block Diagram shown in Fig. 3. The processing of microphone audio is accomplished by the Transmit Audio

Processor portion of the handset circuitry, and by the Transmit Audio Low Pass Filter Board, which plugs onto the motherboard inside the main station body. The Transmit Audio Processor provides amplification, pre-emphasis, and limiting of the microphone audio. The Transmit Audio Low Pass Filter provides a very high attenuation of any frequencies outside of the audio passband.

(ii) Transmit Audio Processor

The Transmit Audio Processor, and other handset circuitry is shown in Fig. 11. Microphone MK 101 is biased by R101. The microphone audio is routed through C102 and variable series resistor R102 to the Transmit Audio Processor section. The ratio of R102 to R201 determines the microphone audio level. This microphone audio is routed to terminal J101-1 for monitoring at the station main body.

The microphone audio proceeds to the pre-emphasis circuit, composed of R202, R203, and C201, which provides a 300 microsecond pre-emphasis. C202 cancels out the pre-emphasis above 5 KHz. The pre-emphasized audio is applied to U201, which is a National Semiconductor LM386 Audio Amplifier. The gain of U201 is set by R204. Compensation against high frequency oscillation is provided by R205 and C206. The amplified audio from pin U1-5 is routed through C207 to terminal J101-2 for monitoring in the station main body. The amplified audio is also applied to a low pass filter formed by R206, R207, and C208. Germanium diodes CR201 and CR202 provide a



NOTES 1. ALL RESISTORS ARE IN OHMS AND ALL CAPACITORS IN MICROFARADS UNLESS OTHERWISE INDICATED.

FIGURE 11 HANDSET CIRCUITRY

limiting action (peak-clipping), which increases the average audio RMS power level for a given maximum peak audio level. The degree of limiting (usually about 10 dB) is determined by the setting of R102 and R204. The final audio, which is pre-emphasized, amplified, and limited, is routed to terminal J101-3.

(iii) Transmit Audio Low Pass Filter

The Transmit Audio Low Pass Filter circuitry is shown in Fig. 12. It consists of an input buffer amplifier, and a five pole, low pass, Chebychev active filter. The active filter uses two of four operational amplifiers contained on a National Semiconductor LM339 integrated circuit. The other two operational amplifiers are not used. Because the theory of operation of this type of filter is fairly involved and can be found in any standard text on active filter design, it will not be dealt with here. However, the basic characteristics of the filter are as follows. The filter configuration is of the multiple-feedback type. Its 3 dB point is at 3.3 KHz, and the ripple level is 1 dB. A five pole Chebychev filter has a stop-band slope of at least 30 dB per octave.

Transmit audio from the handset is routed through terminal P431-3 to the base of Q301, a Darlington transistor. Q301 is connected in an emitter follower configuration, and functions as a buffer amplifier. It is required, because the active filter circuitry which follows, requires a very low impedance signal source for proper operation. Audio from the emitter of Q301 is routed to resistor R301

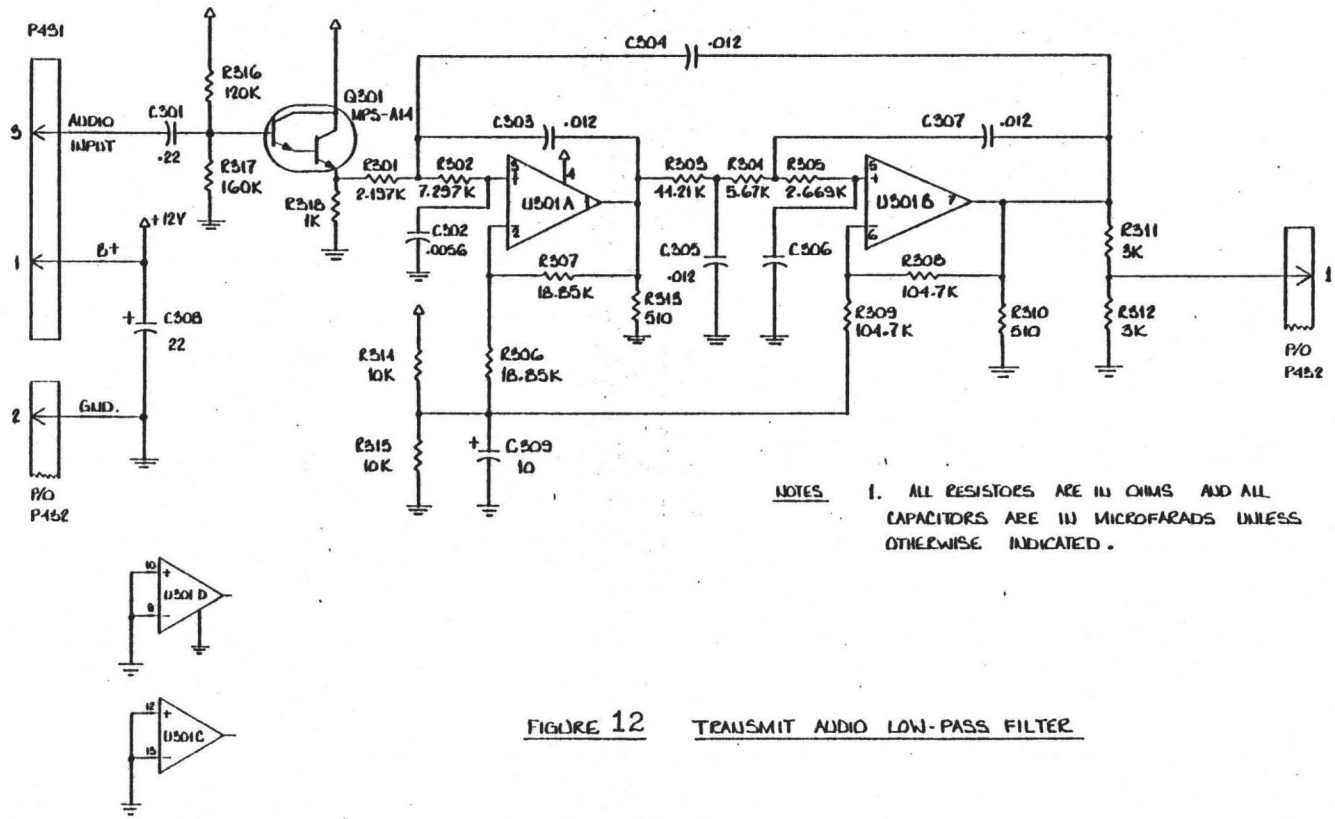


FIGURE 12 TRANSMIT AUDIO LOW-PASS FILTER

which is the start of the active filter circuitry. R316 and R317 bias Q301 such that the D.C. level at the emitter is at half the power supply voltage.

After passing through the active filter, the transmit audio is attenuated by R311 and R312, and routed to terminal P432-1. From there, the transmit audio will be routed by the motherboard to the transmitter. R314, R315, and C309 provide a filtered reference voltage for operational amplifiers U301A and U301B.

Power and ground are routed in through terminals P431-1 and P432-2 respectively. C308 provides power supply filtering. The inputs of operational amplifiers U301C and U301D are grounded to prevent unwanted oscillation.

V PULSE GENERATION

(i) General

A block diagram of the Dial Pulse Processing Board is shown in Fig. 13(b). Pulses created by dry contact closure at the station dial are routed to this unit. The rising side of the pulses is debounced and applied to a comparator/buffer. This is followed by circuitry for debouncing the falling side of the pulses and by a driver stage. Pulses from the driver pass through special shaping circuitry, and are routed to the transmitter pulse input.

The pulses cause short interruptions in the RF subcarrier of the transmitter, to be decoded at the central processor. To avoid 'splatter' (interference in adjacent channels), the duration,

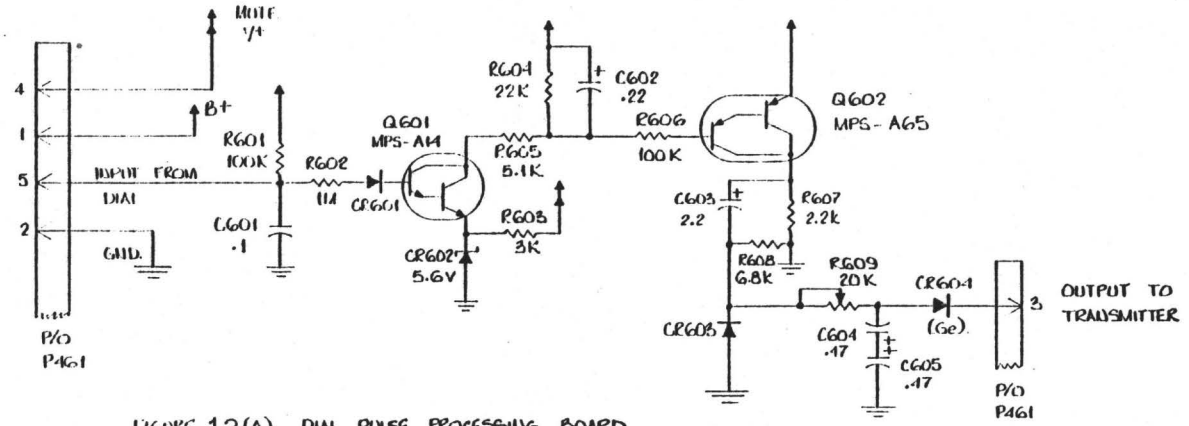


FIGURE 13(A) DIAL PULSE PROCESSING BOARD.

NOTES 1. ALL RESISTORS ARE IN OHMS AND ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE INDICATED.

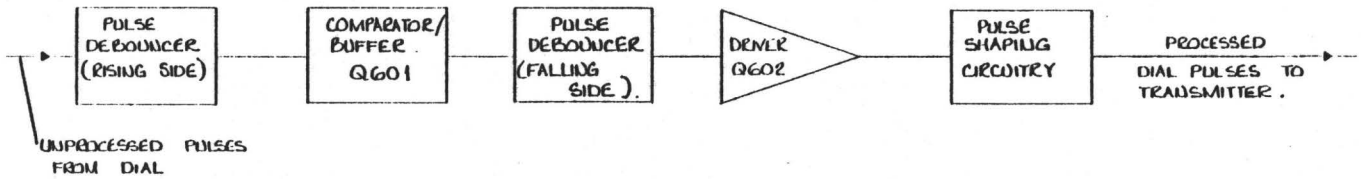


FIGURE 13(B) DIAL PULSE PROCESSING BOARD BLOCK DIAGRAM

shape, and height of these interruptions must be such that negligible harmonics are generated above 5 KHz. The required values are as follows. The duration of the interruption is 2 msec. The rise and fall times are 1 msec each. The maximum attenuation of the subcarrier is to 10% of its unmodulated value, corresponding to a maximum index of modulation of 90% for pulses. The values are set by a single adjustment on the Dial Pulse Processing Board. The adjustment is made after the subcarrier level and the transmit audio index of modulation have been adjusted in the transmitter.

(ii) Detailed Description

A schematic of the Dial Pulse Processing Board is shown in Fig. 13(a). The unprocessed pulses from the dial enter via terminal P461-5. The type of input provided by the dial to this terminal is a normally closed switched ground. The pulses are 50 msec wide, and there is a 50 msec space between pulses. Thus, the pulses have a 10 Hz rate, with a 50% duty cycle.

In the absence of pulses, the junction of R601 and C601 is at ground, and Q601 is off. When a pulse arrives, the input to terminal P461-5 becomes an open circuit with respect to ground. C601 is then charged through resistor R601. When the dial is being used, the Mute V^+ input at terminal P461-4 goes to power supply. This causes a current to flow through R603 and CR602, which clamps the emitter of Q601 to 5.6 V. The voltage across C601 is applied to the base of Q601 through R602 and CR601. R602 prevents Q601

from loading the circuit consisting of C601 and R601. CR601 prevents the base-emitter junction of Q601 from becoming reversed biased when the junction of R601 and C601 is at less than 5.6 V. When the voltage across C601 exceeds approximately 7 V, Q601 is turned on. The time required for C601 to charge up to this value is much larger than time interval, at the beginning of each pulse, during which bouncing may occur. Thus, the circuit ignores any rising side pulse bounce.

When Q601 is turned on, it begins to charge C602 through R605. When the voltage across C602 reaches 1.4 V, Q602 is turned on through R606. Q601 continues to discharge C602 until Q601 is in saturation and C602 has 6 V across it. C602 serves two purposes. First, it provides a transition to the base of Q602 which is smooth and of a specific slope. Second, it helps debounce the falling side of the pulses, as explained later.

When Q602 is initially turned on, a 12 V potential appears across R607, R608, and CR603. The voltage across CR603 starts to charge up C604 and C605 through R609, and the voltage across these two capacitors is applied to terminal P461-3 through germanium diode CR604. Immediately after Q602 is turned on, C603 begins to charge up through R608 and R609. The component values are such that the voltage across C603 is approximately 7 V when the voltage across C604 and C605 is also at about 7 V. At this time, C603 continues to charge up through R608, and C604 and C605 now start to discharge through R609 and R608. The resultant voltage across C604 and C605, since Q602 was turned on, takes the form of a single

smooth and rounded pulse with a height of approximately 7 V. However, since terminal P461-3 is biased at 6 V by the transmitter, the voltage at P461-3 corresponds to the top portion (above the 6 V level) of the pulse across C604 and C605. Therefore, what appears at P461-3 is a very smooth, rounded pulse of approximately 1 V amplitude, superimposed on 6 V D.C. This is exactly the type of pulse waveform the transmitter requires to produce the type of subcarrier interruptions described in the 'General' subsection. CR604 prevents the pulse processing circuitry from bringing the voltage at P461-3 below 6 V D.C. R609 allows adjustment of the depth of the subcarrier interruptions (i.e. the pulse index of modulation).

By the time the falling side of the pulse from the dial arrives at P461-5, C601 is charged up to 12 V, Q601 is on, C602 is charged up to 6 V, Q602 is on, C603 is charged up to 12 V, and C604 and C605 are discharged. At the end of the pulse, the dial grounds terminal P461-5, which discharges C601 and turns off Q601. If there is enough time, between the first falling edge of the pulse and any bounce which may follow, to completely discharge C601, then the 'turn-on' delay caused by R601 and C601 will defeat any bounce which follows. Otherwise, falling side pulse bounce may cause Q601 to briefly turn on again several times. However, when Q601 is turned off, C602 begins to discharge through R604. Only when the voltage across C602 drops to below 1 V, will Q602 turn off. The time required for C602 to discharge is much longer

than the duration of any falling side pulse bounce, and so, if R601 and C601 don't defeat the falling side bounce, C602 will.

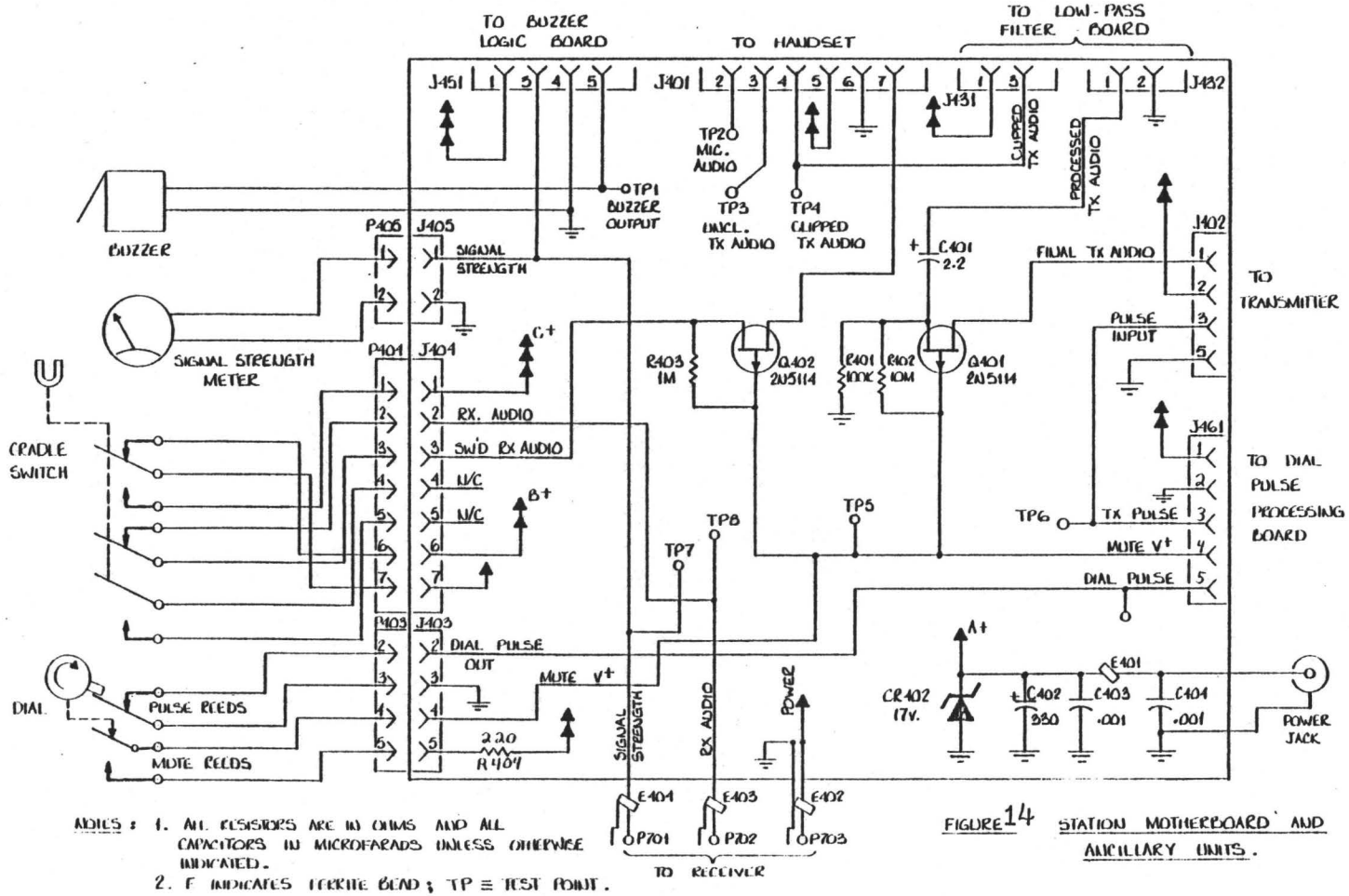
When Q602 is turned off, C603 discharges through R607, R608, and CR603. CR603 clamps the voltage across C604 and C605 to approximately ground potential, while C603 is discharging. It also decreases the discharge time of C603.

Until the next pulse arrives, both Q601 and Q602 are turned off. If the dial has sent the last pulse, the Mute V^+ voltage is removed from terminal P461-4. The only current then drawn by the circuit is approximately 0.12 mA, drawn by R601.

VI POWER, AUDIO CONTROL, AND ANCILLARY UNITS

(i) General

A schematic of the station motherboard, which also shows the station ancillary units and their connections to the motherboard, is shown in Fig. 14. The ancillary units consist of the buzzer, a signal strength meter, a cradle switch, and the dial. Other connections to the motherboard are the handset, the receiver, the transmitter, and the power jack. Also, three daughterboards are mounted via jacks onto the motherboard. These are the Buzzer Logic Board, the Transmit Audio Low Pass Filter, and the Dial Pulse Processor. The motherboard interconnects all the various units, provides power supply filtering, gates transmit and receive audio, and provides many easily accessible test points for troubleshooting.



NOTES : 1. ALL RESISTORS ARE IN OHMS AND ALL CAPACITORS IN MICROFARADS UNLESS OTHERWISE INDICATED.
2. F INDICATES FERRITE BEAD ; TP ≡ TEST POINT.

FIGURE 14 STATION MOTHERBOARD AND ANCILLARY UNITS.

Some additional control circuitry for the receiver audio is contained in the handset circuitry shown in Fig. 11.

(ii) Detailed Description

Power is routed from the battery to the power jack by an external cable (shown in Fig. 3) which contains a 1 Amp, 'slow-blow' fuse, and a 3 Amp (300 Amp surge) diode connected in a 'crowbar' fashion across the (+) and (-) lines in case the battery connections are reversed accidentally.

From the power jack, the battery voltage is routed to a three pole RF filter, comprised of C403, C404, and E401. The battery voltage is filtered at low frequencies by C402. Zener diode CR402 protects the station circuits from overvoltage, and also functions as an auxiliary 'crowbar' protection diode. After filtering, the battery voltage is referred to as the A^+ power supply.

The A^+ voltage is applied to J404-7, the center contact of a set of Form C contacts in the cradle switch. The contact which is closed when the handset is 'off-hook', is routed to J404-6. The contact which is closed when the handset is 'on-hook' is routed to J404-1. There is 12 V D.C. at terminal J404-6 whenever the handset is off the cradle, and this is referred to as the B^+ power supply. Similarly, there is 12 V D.C. at terminal J404-1 whenever the handset is on the cradle, and this is referred to as the C^+ power supply. B^+ power is routed to terminal J403-5

through R404. From there it is routed through the mute reeds of the dial and back to terminal J403-4, where it is referred to as the Mute V^+ voltage. The mute reeds are shorted whenever the dial is turned. The reason for the three power supplies (A^+, B^+, and C^+) is to ensure that the various station units are powered only when they are needed. Processed transmit audio from the handset is routed, through J401-4, to the Transmit Audio Low Pass Filter, via J431-3. Then the transmit audio is routed from J432-1, the output of the Transmit Audio Low Pass Filter, through Q401, to the transmitter input, J402-1. Q401 blocks transmit audio whenever there is a Mute V^+ voltage present. This prevents transmit audio being transmitted along with the dial pulses, which might cause false counts at the central processor.

Receive audio is routed from P702 to J404-2. From there it passes through a pair of switch contacts in the cradle switch, which are closed when the handset is off the cradle, and then it is routed back to J404-3. Since the receiver is powered by A^+ through P703, it is always on. If there is no receive signal present at the station, which can only occur when the handset is on cradle, audible static would emanate from the earphone. Routing the audio through the cradle switch prevents this. Receive audio is next routed from J404-3, through Q402, to the handset via terminal J401-7. Q402 blocks receive audio during dialing(i.e. when a Mute V^+ voltage is present) just as an ordinary telephone does.

The signal strength output of the receiver, from P701, is routed to the signal strength meter input, at terminal J405-1. RF filtering is provided in receiver plugs P701, P702, and P703, by ferrite beads E402, E403, and E404.

Additional receiver audio control is performed by the handset circuitry, as shown in Fig. 11. R104 together with R103 act as an auxiliary receive audio volume control, eliminating the need to open the receiver for final adjustments of earphone audio. CR101 and CR102 protect the earphone (and the user's ear) from large receive audio spikes.

Returning to the motherboard, the switched ground from the dial's pulse reeds is routed, through J403-2, to the input of the Dial Pulse Processing Board, J461-5. The processed pulses from the Dial Pulse Processing Board are routed, through J461-3, to the pulse input of the transmitter, J402-3. The signal strength output from P701 is also routed to the input of the Buzzer Logic Board, J451-3. The buzzer drive output from J451-5 is then routed to the buzzer. Test points TP1 through TP8 are easily accessible terminals on the motherboard, which allow monitoring of critical voltages and signals during troubleshooting.

CHAPTER 3

CENTRAL PROCESSOR ANALOG ELECTRONICS

I GENERAL DESCRIPTION

A block diagram of the central processor is shown in Fig. 15. The optical components consist of a fibre jack, a 2 to 1 fibre optic coupler/splitter, an LED, and a photodiode. The remaining components can be divided into two sections: the analog electronics, which are described in this chapter; and the logic circuitry, which is fully described in the report entitled 'An Optical Fibre Telephone System (Central Switching and Logic)' by John Goodwin.[1]

The incoming light is routed to the photodiode, which is connected to a transimpedance amplifier. The transimpedance amplifier drives three isolators, one for each receive channel. The isolators prevent local oscillator feedthrough between receivers.

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[1] After the preliminary evaluation, described in the report entitled 'System Analysis', it was found that several significant changes had to be made to the C.P. Logic Circuitry and related units, to make the system functional. These changes are also fully described in the report mentioned above. Among the changes was the addition of the 'Sidetone and Auxiliary Gating Unit' shown in Fig. 15, to augment the C.P. Logic Circuitry. It is shown here as a separate unit for simplicity and completeness.

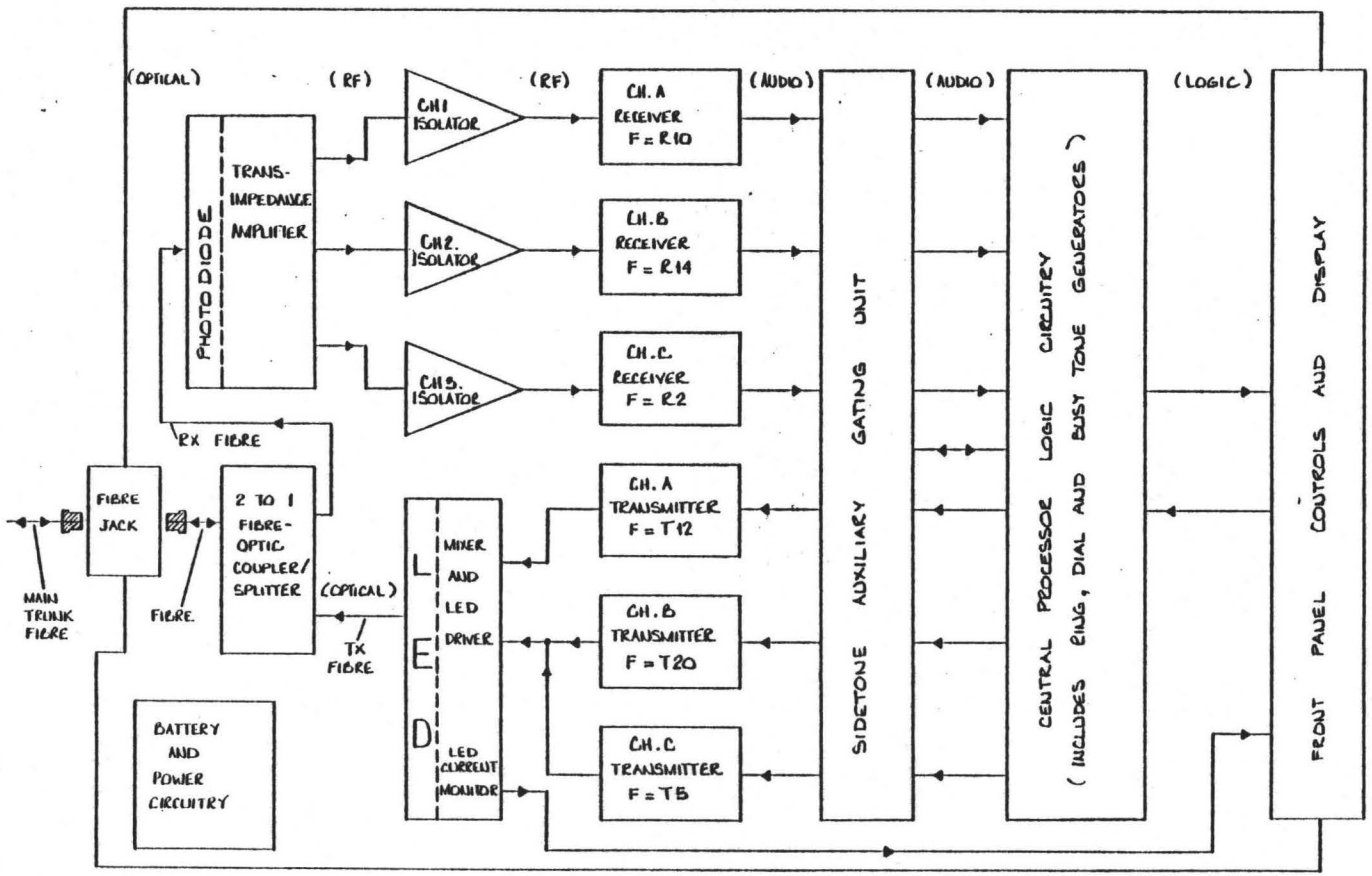


FIGURE 15 CENTRAL PROCESSOR BLOCK DIAGRAM.

The output of each isolator is routed to a receiver. The audio and signal outputs from the receivers are routed through the Sidetone and Auxiliary Gating Unit, to the Central Processor Logic Circuitry. The C.P. (Central Processor) Logic Circuitry switches and routes the various audio signals to their correct destinations, deciphers the control signals from the receivers, generates the dial, busy, and ring tones, and sends out logic signals to the transmitters.

The transmitter audio and logic signals, from the C.P. Logic Circuitry, are routed through the Sidetone and Auxiliary Gating Unit, to the three transmitters. The RF outputs of the transmitters are combined (added) in the Mixer and LED Driver Unit. This unit drives the LED, whose output is routed by fibre to the 2 to 1 Fibre Optic Coupler/Splitter. The Mixer and LED Driver Unit also provides an output for front panel monitoring of the LED current (both D.C. and RF).

The Central Processor also contains a 4.5 Ampere-Hour, 12 V, rechargeable battery, power circuitry, and a front panel containing monitor points, meters, and the power switch.

Since the transmitters and receivers are for the most part identical to those of the stations, they will not be discussed in this chapter, except for specific differences between the station and C.P. units. For a detailed description of the circuits and operation of the transmitters and receivers, refer to the appropriate sections in Chapter 3.

II TRANSIMPEDANCE AMPLIFIER AND C.P. RECEIVERS

(i) Photodiode and Transimpedance Amplifier

The photodiode and C.P. transimpedance amplifier is shown in Fig. 16. It is identical to the 'Photodiode Stage' shown in Fig. 8, except for the following.

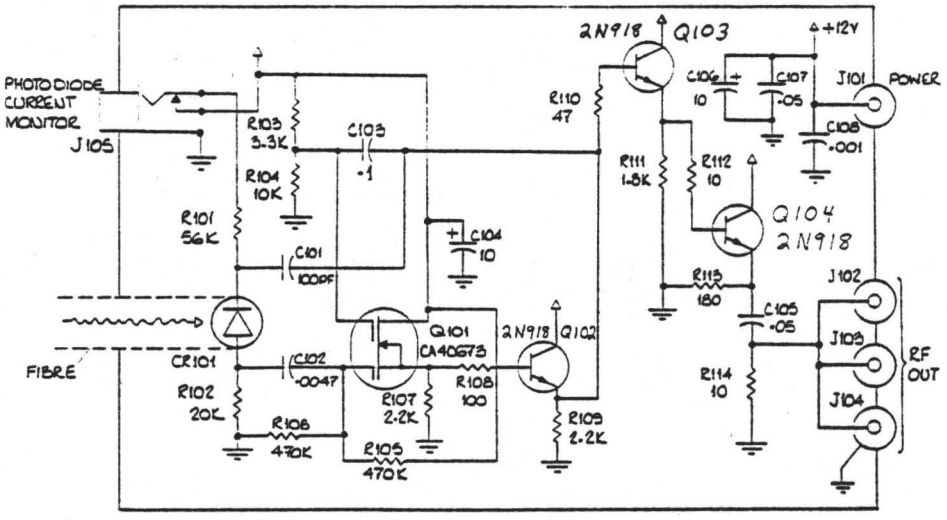
The photodiode and transimpedance amplifier are installed in a separate enclosure, made of 30 gauge brass sheeting. Jack J105 is installed for monitoring the D.C. photodiode current with a picoammeter. Components R112, R113, R114, Q104, C105, C106, C107, and C108 are either different, or non-existent in the station photodiode stage. Q104 is an additional emitter follower, which provides a low enough impedance to drive the three isolators. C106, C107, C108 are used for input power filtering. Jacks J101 through J104 are provided for power input, and for routing the RF output to the isolators.

(ii) C.P. Receivers

The C.P. receiver circuitry is the same as that shown in the block diagram in Fig. 7, and in the schematics in Fig. 8 and Fig. 9, except for the following.

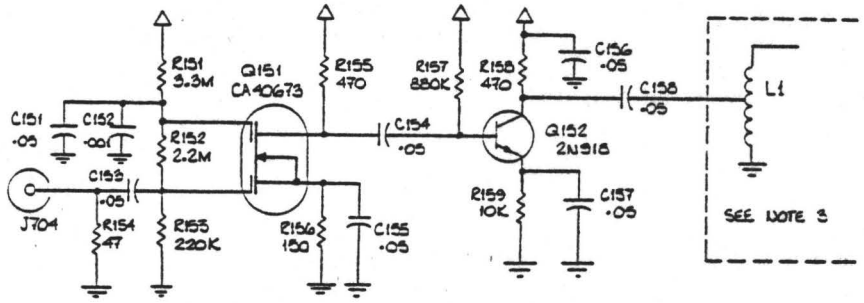
The photodiode stage shown in Fig. 8 is replaced by the C.P. receiver buffer amplifier, shown in Fig. 17. Its purpose is to provide a resistive 50 ohm load to the isolator, and to reduce the local oscillator feedthrough to jack J704.

RF from the isolator enters via jack J704, and is applied to gate #1 of common source amplifier Q151. Gate #2 of Q151 is at



NOTES 1. ALL RESISTORS ARE IN OHMS AND ALL CAPACITORS IN MICROFARADS UNLESS OTHERWISE INDICATED.

FIGURE 16 PHOTODIODE AND TRANSIMPEDANCE AMP.



NOTES: 1. ALL RESISTORS ARE IN OHMS AND ALL CAPACITORS IN MICROFARADS UNLESS OTHERWISE INDICATED.

2. THIS CIRCUIT IS INSTALLED IN C.P. RECEIVERS ONLY.

3. L1 IS PART OF THE RECEIVER FRONT-END, AND IS SHOWN FOR ILLUSTRATIVE PURPOSES ONLY.

FIGURE 17 C.P. RECEIVER BUFFER AMP.

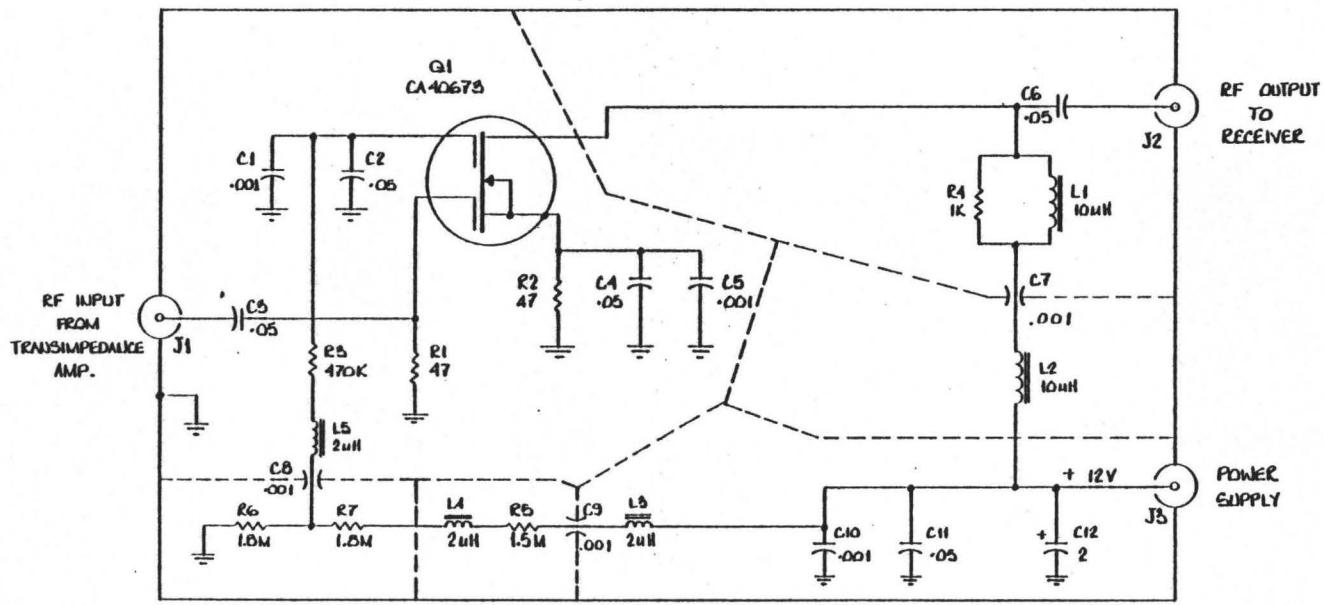
A.C. ground, which isolates the drain from gate #1 in order to reduce local oscillator reverse feedthrough. The gain of Q151 is approximately 1.5 due to the loading of the next transistor. The signal is routed to the base of common emitter amplifier Q152. The emitter current is approximately 0.7 mA, which gives a gm of about 1/40. Since the tap at L1 has an impedance of 50 ohms at resonance, the gain of Q152 is just over unity.

In the receiver main circuitry, shown in Fig. 9, C22 is .01 microfarads, which removes the de-emphasis used in the station receivers. Since C.P. receiver audio is to be retransmitted, de-emphasis is not required or desired. Finally,in C.P. receivers, due to greater spacing between different units, extensive RF filtering was not required, and so beads E1, E2, and E3, and capacitors C28, C29, and C30 were not used.

III ISOLATOR

The purpose of the isolator is to prevent local oscillator leakage at the input of a receiver from feeding through to any other receivers. The C.P. receiver buffer amplifiers did not accomplish this to the required degree.

The isolator, shown in Fig. 18, consists of a very well shielded and filtered, common source, Mosfet amplifier. It has a 50 ohm input impedance, it drives a 50 ohm load (the buffer amplifier input of the receiver), and it has a gain of just less than unity.



NOTES. 1. ALL RESISTORS ARE IN OHMS AND ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE INDICATED.

2. DASHED LINES REPRESENT SOLID COPPER SHIELDS.

FIGURE 18 ACTIVE RECEIVER ISOLATOR.

The isolator enclosure is made of 20 gauge copper, as are the internal shields which partition the enclosure into six compartments. The contents of each compartment will be described in clockwise order, starting with the compartment containing the input jack, J1.

RF from the transimpedance amplifier is routed through J1 and C3 to gate #1 of Q1. Gate #1 is self biased by input resistor R1 and source resistor R2. Gate #2 is biased at 4.2 V through R3 and L5, which allow full transistor gain. Gate #2 is at A.C. ground potential because of C1 and C2, which isolates the drain from gate #1, to further prevent reverse feedthrough from the output to the input. The output from the drain of Q1 is routed to the next compartment, and through C6 to output jack J2. The RF at J2 is externally routed to the C.P. receiver, which has a 50 ohm input impedance. R4 acts as a limiting load impedance in parallel with the receiver input impedance, to avoid any stray oscillations. D.C. power to the drain of Q1 is supplied through L1.

The D.C. drain power enters from the next compartment via feedthrough capacitor C7. This compartment contains RF choke L2. It is connected to the power supply line in the fourth compartment. The fourth compartment contains the power input jack, J3, and power supply filtering capacitors. The 12 V power supply is also routed through L3 and C9 into the next compartment, which contains bias resistor R5 and L4. The bias voltage is then fed to the final compartment, which contains the additional

two bias resistors R7 and R8. The gate #2 bias voltage is then fed through C8 to the first compartment which contains Q1.

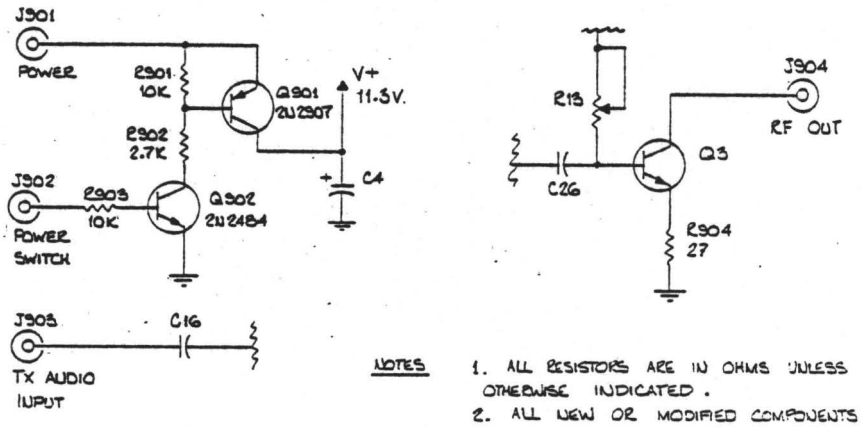
IV C.P. TRANSMITTERS, AND MIXER AND LED DRIVER

(i) C.P. Transmitters

The C.P. transmitter circuitry is the same as that shown in the block diagram in Fig. 4, and in the schematic in Fig. 5, except for the following.

The filtering, power, and connector section shown in Fig. 5, is replaced by the jacks and power switch circuitry shown on the left side of Fig. 19. The RF filtering used in the stations was not required in the central processor due to greater spacing between the different units. Transmit audio enters via J903. Power is routed through J901 to power switch Q901. The power switch is controlled by switch driver Q902, which in turn is controlled by a TTL signal from the C.P. Logic Circuitry, routed through J902. Q901 and Q902 enables the C.P. Logic Circuitry to apply or remove D.C. power from the transmitter circuits, which is necessary for automatic operation. When a TTL signal is applied to J902, it turns on Q902, which turns on Q901. Q901 then routes D.C. Power to the transmitter power bus line.

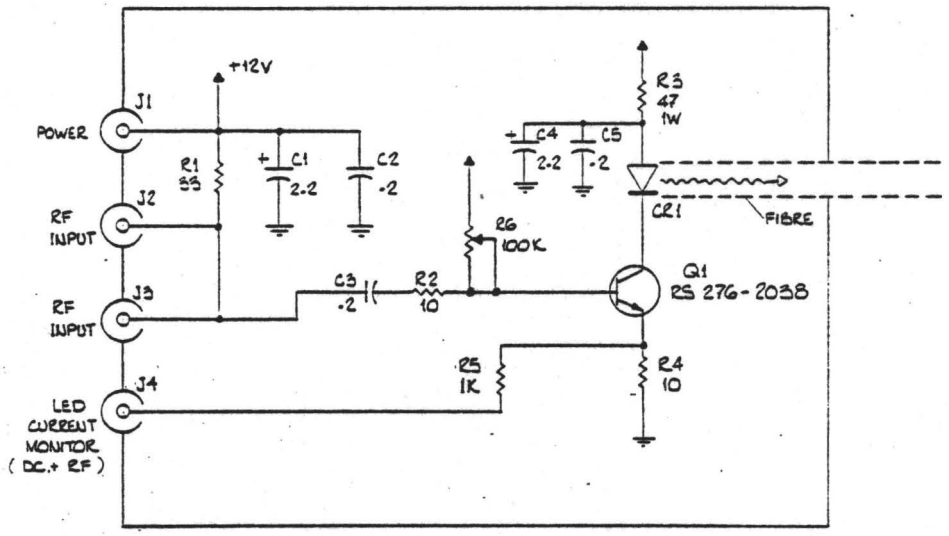
In the C.P. transmitters, the output of the intermediate RF amplifier Q2 is routed through C26 to mixer driver Q3, as shown in Fig. 19. Q3 is connected in a common-emitter configuration, with positive feedback provided by emitter resistor R904 to ensure



NOTES

1. ALL RESISTORS ARE IN OHMS UNLESS OTHERWISE INDICATED.
2. ALL NEW OR MODIFIED COMPONENTS ARE NUMBERED FROM 900 UP.
3. THE 'PULSE INPUT' SHOWN ON STATION TRANSMITTERS IS NOT USED IN THE C.P.

FIGURE 19 TRANSMITTER MODIFICATIONS FOR USE IN CENTRAL PROCESSOR.



NOTES. ALL RESISTORS ARE IN OHMS AND ALL CAPACITORS IN MICROFARADS UNLESS OTHERWISE INDICATED.

FIGURE 20 MIXER AND L.E.D. DRIVER

linearity. The collector of Q3 is routed to J904, and the gain of Q3 is equal to the output impedance divided by 27 (R904).

(ii) Mixer and LED Driver

The mixer and LED driver circuitry, shown in Fig. 20, combines the outputs of the C.P. transmitters, and drives the transmit LED with the combined signal. The circuitry, including the LED, is contained in a 30 gauge brass enclosure.

The RF outputs from the transmitters are routed into the mixer through jacks J2 and J3 (two of the transmitter outputs are connected in parallel externally). The combined currents are applied across load resistor R1. Thus the gain of the mixer driver of each transmitter is 33/27 = 1.2. Because the collector outputs of the mixer drivers are high impedance current sources, they do not load each other, and the currents simply add.

The combined transmit signal is routed through R2 to LED driver Q1, which is connected as an emitter follower. R2 prevents Q1 from oscillating (due to stray capacitance in the emitter circuit), and R6 adjusts the D.C. bias current through Q1 and LED CR1. The collector of Q1 drives LED CR1, whose optical output is coupled to a fibre, which is routed out through a small aperture in the enclosure. R3 drops some of the power supply voltage to reduce some of the power that Q1 must dissipate.

The voltage across emitter resistor R4 is routed through R5 to J4. R5 prevents any load at J4 from significantly affecting

the emitter voltage of Q1. When J4 is terminated with a 50 ohm impedance, the voltage across that impedance is equal to half the LED current, both RF and D.C.

V POWER AND INSTRUMENTATION

The front panel and the power circuitry is shown in Fig. 21. The 12 V, 4.5 Ampere-hour battery is bracketed to the chassis. The battery is charged through input J8, and the battery power is routed through fuse F1 and front panel switch S1 to the power distribution panel. The power input lines from all other C.P. circuitry are connected to this distribution panel. Meter M4 provides a visual indication of the battery condition, and R4 and CR4 establish the meter voltage range of 11 V to 14 V D.C.

The transmitter audio inputs, from the sidetone and auxiliary gating unit, are monitored at jacks J1, J2, and J3. The receiver outputs are monitored by jacks J4, J5, and J6, and are terminated (to ensure that the D.C. level of the outputs is clamped to ground) by resistors R1, R2, and R3. The receiver outputs are then routed through the sidetone and auxiliary gating unit, to the C.P. logic circuitry.

The LED current monitor output from the mixer and LED driver unit is routed to J7. LED's CR1, CR2, and CR3, indicate which transmitters are on, and are activated by the C.P. logic circuitry. Finally, the signal strength signals from the receivers are applied to meters M1, M2, and M3, before being routed to the C.P. logic circuitry.

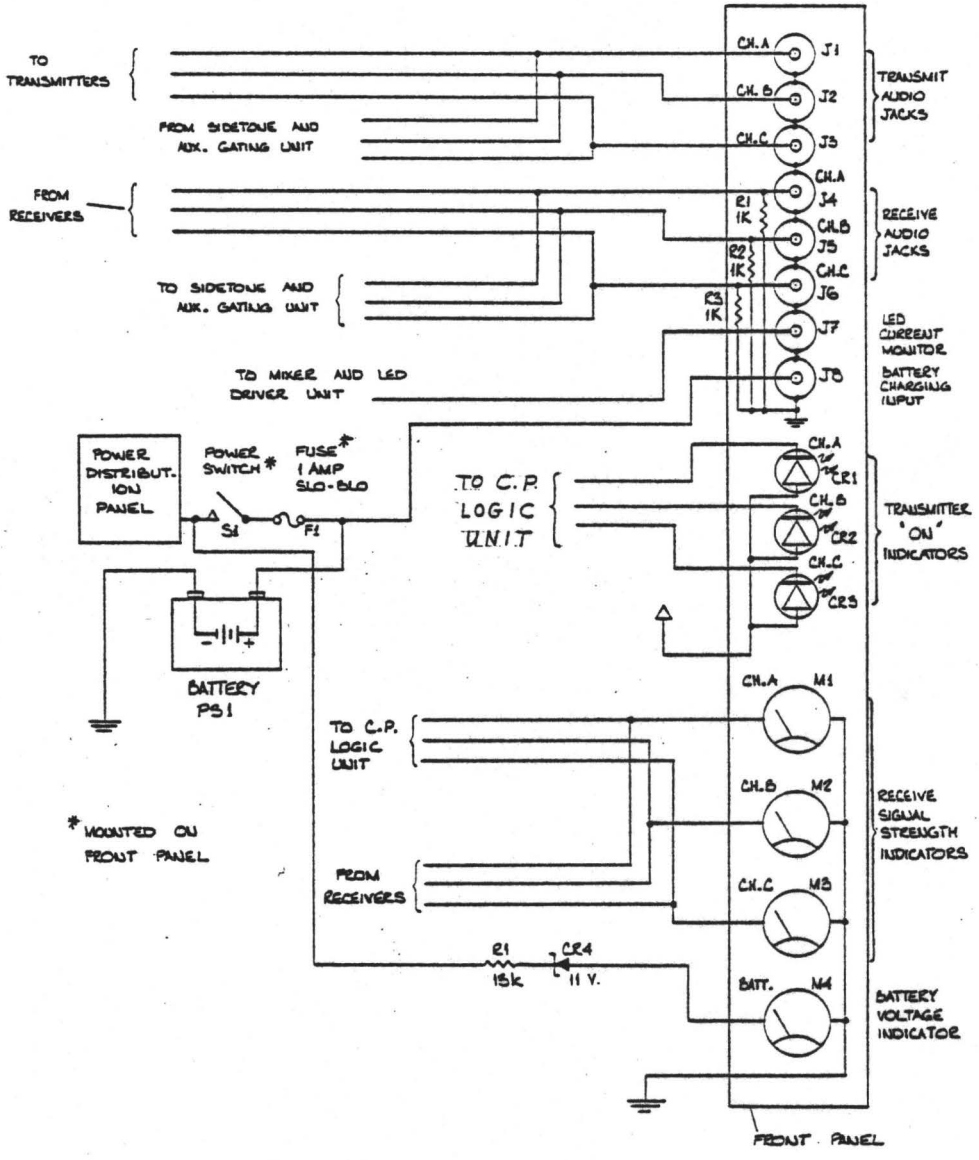


FIGURE 21 FRONT PANEL AND INSTRUMENTATION.

The front panel is a steel 19 inch rack panel, to which is bolted the entire C.P. chassis. The front panel and chassis can be rack mounted, or can be inserted into a steel, 19 inch, chassis enclosure, which is what was used.

CHAPTER 4

CONCLUSIONS

I GENERAL

The primary objectives of this project were achieved. The first objective was to successfully demonstrate the feasibility of a frequency multiplexed, RF subcarrier, telephone communications system, which used optical fibre as the transmission medium, and was 'user oriented' in design. The second objective was to gain an insight into the problems encountered with the implementation of such a system. To date, this is the first known attempt (and achievement) of the particular objectives described above.

The area of greatest difficulty and complexity in this project was the analog electronics. The complexity was further augmented by the high degree of miniturization required. The design problems would have been greatly eased, and the overall design would have been significantly improved, by far more extensive prototyping of the individual units, and by making more use of sophisticated RF test equipment in the very early stages of the RF and IF circuit design. The latter two recommendations cannot be overemphasized to anyone undertaking further development of this system, or the design of a new system based on the same operational principles.

II SUGGESTED AREAS FOR FURTHER DEVELOPMENT AND RESEARCH

The feasibility and practicality of using different ratios in the splitter/coupler units, to optimize system performance, should be investigated. Also, the use of additional fibre jacks, and the effect of this on system losses, should be examined.

System flexibility and performance would be greatly improved by more extensive use of modular design concepts, and by adopting better cabling techniques, both in the logic circuitry, and in the analog electronics.

Finally, the use of other signalling and modulation schemes, and the development of more efficient electro-optical interfaces, should be investigated.

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