AN INTEGRATED CIRCUIT IMPLEMENTATION OF A DIRECT COUPLED GROUNDED GYRATOR

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AUTHOR: Stewart Kramer, B.Eng. (McMaster University)

SUPERVISORS: Professor S. S. Haykim
Professor J. Shewchun

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ABSTRACT:

This thesis presents the results of an investigation of an integrated direct coupled grounded gyrator. A complete analysis is presented for the gyrator using components available in integrated circuit form. Integrated circuit layout and fabrication procedures are discussed.

Close agreement between the theoretical and experimental results is shown. The Q factor of a simulated inductor shows good stability over a wide range of frequency, temperature, and voltage supply.

ACKNOWLEDGEMENTS

The author is grateful to Professors S.S. Haykim, and J. Shewchun for their advice and encouragement. The financial support extended by the National Research Council of Canada in support of this work is acknowledged. The assistance given by Dr.W. Pieczonka of the Solid State Devices Department, Canadian Westinghouse Company Limited, Hamilton, Ontario, in layout and fabrication techniques enabled this work to be completed successfully and was greatly appreciated.

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CHAPTER I

THE ELECTRIC GYRATOR

1.1 INTRODUCTION:

In this chapter, a theoretical analysis of the ideal gyrator is presented in terms of the impedance and admittance matrices. The properties of a non-ideal gyrator are considered, and the imperfections at both high and low frequencies are evaluated. The high frequency effects can be utilized to good advantage by using compensating techniques as outlined in the last section of the chapter.

1.2 CHARACTERIZATION OF AN IDEAL GYRATOR:

An ideal gyrator is a two-port network that can be defined by its device open circuit impedance matrix

$$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} = \begin{bmatrix} 0 & \pm R_o \\ \mp R_o & 0 \end{bmatrix} \tag{1.1}$$

where R_o is real and is called the gyration constant. This element was first proposed by Tellegen[1] as an additional element necessary to synthesize passive networks. The gyrator is uniquely distinguished from the other passive elements by its non-reciprocity; indeed, it is an anti-reciprocal two-port.

The ideal gyrator is thus a two-port network which, at either port presents a driving point impedance that is inversely proportional to the terminating impedance connected across the other port. If the

gyrator is terminated with an impedance at port 2, as in figure 1-1, the input impedance measured at port 1 is given by the relation

$$Z_{IN} = R_o^2 Y_L \tag{1.2}$$

where $Y_L = 1/Z_L$. Alternatively, the admittance is proportional to Z_L as shown by

$$Y_{IN} = g_o^2 Z_L \tag{1.3}$$

where $g_o = 1/R_o$ is called the gyration conductance. It is apparent from equation 1.2, that if Z_L is purely resistive, then the reflected input impedance is purely resistive also and has the same sign. If the terminating impedance Z_L is a capacitor, then it can be seen that the reflected input impedance is now inductive, and if the terminating impedance is inductive, the reflected input impedance is capacitive. Thus, the gyrator has the property of inverting the impedance connected to it.

The voltage-current relations of the ideal gyrator may be thus expressed as shown by

$$I_1 = \pm g_o V_2 \tag{1.4}$$

$$I_2 = \mp g_o V_1 \tag{1.5}$$

with the signs signifying the direction of gyration.

The circuit symbol for a gyrator is as shown in figure 1-2 in which the direction of the arrow signifies the direction of gyration with

$$I_1 = g_o V_2 \tag{1.6}$$

$$I_2 = -g_o V_1 . \tag{1.7}$$

If the direction of gyration is reversed, then the signs of equation 1.6 and equation 1.7 will be reversed.

If terminals 1' and 2' (figure 1-3) are connected together, a three terminal device will be obtained. The Y matrix of this device is

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} 0 & g_o \\ -g_o & 0 \end{bmatrix} . \tag{1.8}$$

The indefinite admittance matrix is obtained from equation 1.8 by completing each row and column to zero and is therefore

$$\begin{bmatrix} y_{11} & y_{12} & y_{13} \\ y_{21} & y_{22} & y_{23} \\ y_{31} & y_{32} & y_{33} \end{bmatrix} = \begin{bmatrix} 0 & g_o & -g_o \\ -g_o & 0 & g_o \\ g_o & -g_o & 0 \end{bmatrix} . \tag{1.9}$$

When any terminal of the device is grounded, the corresponding row and column of the indefinite matrix are crossed out. Thus, when terminal 1 is grounded as shown in figure 1-4, the resultant Y matrix is

$$\begin{bmatrix} y_{22} & y_{23} \\ y_{32} & y_{33} \end{bmatrix} = \begin{bmatrix} 0 & g_o \\ -g_o & 0 \end{bmatrix} . \tag{1.10}$$

Similarly, when terminal 2 is grounded as shown in figure 1-5, the resultant Y matrix is

$$\begin{bmatrix} y_{11} & y_{13} \\ y_{31} & y_{33} \end{bmatrix} = \begin{bmatrix} 0 & -g_o \\ g_o & 0 \end{bmatrix} . \tag{1.11}$$

It is therefore obvious that no matter which terminal of the device is grounded, the resultant two by two matrix is always the same as that of equation 1.8, with a possible reversal of sign as in the case shown in figure 1-5. Thus, the three terminal gyrator exhibits the same properties

in all grounded positions.

If the gyration conductance g_o is real, (i.e. not a function of the complex variable s), equations 1.6 and 1.7 can be written as

$$i_1(t) = g_o\, v_2(t) \tag{1.12}$$

$$i_2(t) = -g_o\, v_1(t) \ . \tag{1.13}$$

Hence,

$$i_1 v_1 + i_2 v_2 = 0 \ . \tag{1.14}$$

That is, the ideal gyrator is a lossless, passive transmission device that does not generate, dissapate, or store energy.

1.3 THE NON-IDEAL GYRATOR:

Practical circuits used to realize a gyrator differ from the ideal form in several respects:

(1) The driving point admittance y_{11} and y_{22} are usually small but nevertheless, have finite values.

(2) The transfer admittances y_{12} and y_{21} usually are not equal.

The non-ideal gyrator may, therefore, be presented by the following Y matrix:

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} g_1 & g_r \\ g_f & g_2 \end{bmatrix} \tag{1.15}$$

where $g_r \neq g_f$ and g_1, g_2 may or may not be equal, but nonetheless, finite. This Y matrix may be split into symmetric and skew-symmetric components as follows:

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} g_1 & 1/2(g_r - g_f) \\ 1/2(g_r - g_f) & g_2 \end{bmatrix} + \begin{bmatrix} 0 & 1/2(g_r + g_f) \\ -1/2(g_r + g_f) & 0 \end{bmatrix} \tag{1.16}$$

The symmetric part on the right hand side of equation 1.16 represents a reciprocal π network composed of the conductances;

$$G_A = g_2 + 1/2(g_r - g_f) \tag{1.17}$$

$$G_B = g_1 + 1/2(g_r - g_f) \tag{1.18}$$

$$G_C = -1/2(g_r - g_f) \ . \tag{1.19}$$

By connecting these two networks in parallel, the model for the non-ideal gyrator is obtained as shown in figure 1-6. The non-ideal gyrator shown in figure 1-6 is passive if the π network given by the symmetric matrix of equation 1.16 is also passive, since the ideal gyrator having a gyration conductance of $1/2(g_r + g_f)$ is lossless. Thus, the non-ideal gyrator is passive if

$$g_1 g_2 - 1/4(g_r - g_f)^2 \geq 0 \ . \tag{1.20}$$

If this condition is not met, the non-ideal gyrator is active, exhibiting a direction of transmission for which the device acts as an amplifier. The activity of a gyrator is a quality which may be put to good use as shown by Holmes[2].

If a non-ideal gyrator having the Y matrix given by equation 1.15 is terminated with a capacitor C at port 2 as in figure 1-7[3], the input impedance seen at port 1 is readily found as

$$Z_{IN}(s) = \frac{g_2 + sC}{(g_1 g_2 + g_r g_f) + sCg_1} \tag{1.21}$$

from which the frequency behavior is obtained. Thus,

$$Z_{IN}(j\omega) = \frac{g_2(g_1g_2 + g_rg_f) + \omega^2C^2g_1 + j\,Cg_rg_f}{(g_1g_2 + g_rg_f)^2 + (\omega g_1C)^2} \tag{1.22}$$

$$= R_{EQ}(\omega) + j\,L_{EQ}(\omega) \tag{1.23}$$

Considering the real and imaginary parts of equation 1.22, the equivalent series resistance and inductance, as shown in figure 1-8 are

$$R_{EQ}(\omega) = \frac{g_2}{g_1g_2 + g_rg_f}\left[\frac{1 + \dfrac{\omega^2C^2g_1}{g_2(g_1g_2 + g_rg_f)}}{1 + \dfrac{\omega Cg_1}{g_1g_2 + g_rg_f}}\right] \tag{1.24}$$

$$L_{EQ}(\omega) = \frac{Cg_rg_f}{(g_1g_2 + g_fg_r)^2}\left[\frac{1}{1 + \left(\dfrac{\omega Cg_1}{g_1g_2 + g_rg_f}\right)^2}\right] \tag{1.25}$$

The quality factor Q of the inductor is calculated in the usual way as

$$Q(\omega) = \frac{\omega\,L_{EQ}(\omega)}{R_{EQ}(\omega)} \,. \tag{1.26}$$

Equations 1.24 and 1.25 give

$$Q(\omega) = \frac{\omega Cg_rg_f}{g_2(g_1g_2 + g_rg_f) + \omega^2C^2g_1} \,. \tag{1.27}$$

The Q factor reaches a maximum value at

$$\omega_{MAX} = \frac{g_2}{C}\sqrt{1 + \frac{g_rg_f}{g_1g_2}} \tag{1.28}$$

and this maximum is given by

$$Q_{MAX} = \frac{g_r g_f}{2(g_1 g_2 + g_r g_f)} \sqrt{1 + \frac{g_f g_r}{g_1 g_2}} \qquad (1.29)$$

For many applications, it is true that

$$g_f = g_r = g_o$$

and

$$g_1 = g_2 = g,$$

with g_o being much greater than g. This is justifyable in practice since generally g is less than 1 micromho which g_o is of the order of a millimho or greater. Under these assumptions, equations 1.28 and 1.29 can be reduced to

$$\omega_{MAX} = \frac{g_o}{C} \qquad (1.30)$$

$$Q_{MAX} = \frac{g_o}{2g} \qquad (1.31)$$

which agrees with the result quoted by Orchard[4]. Under the assumptions made, equations 1.24, 1.25 and 1.26 are evaluated and plotted in figure 1-9.

It should be observed that the frequency of maximum Q is lower than the cut-off frequency of the inductance, and also, the Q can be made arbitrarily large with g_o approaching infinity, at the expense of the value of the inductance.

1.4 HIGH FREQUENCY EFFECTS:

Thus far, the imperfections of the gyrator have been investigated at low frequencies only. As the frequency of operation is increased, another source of departure of a practical gyrator from ideal behavior

occurs. The admittance product $Y_{21}Y_{12}$ becomes frequency dependent. This is due to the inherent phase shift resulting between the input voltage and output current.

If it can be assumed that the phase shift or time delay τ for each transconductance can be accounted for by a single time constant, then the two-port admittance matrix of the gyrator circuit together with its terminations can be characterized by equation 1.32,

$$\begin{bmatrix} Y_1 & Y_{12} \\ -Y_{21} & Y_2 \end{bmatrix} = \begin{bmatrix} Y_1 & \dfrac{g_{120}}{1 + s\tau_1} \\ -\dfrac{g_{210}}{1 + s\tau_2} & Y_2 \end{bmatrix} \tag{1.32}$$

where g_{120} and g_{210} are the transconductances at low frequencies, and Y_1 and Y_2 include the parasitic input capacitances and conductances of the electronic circuit as well as the passive terminations. The characteristic equation is thus

$$Y_1Y_2 + y_{21}y_{12} = 0 \quad . \tag{1.33}$$

If, for simplicity, $Y_1 = Y_2 = Y$ and $y_{12} = y_{21} = y$, so that $g_{12} = g_{21} = g$ and $\tau_1 = \tau_2 = \tau$, then equation 1.33 implies that

$$Y \pm jy = 0 \, . \tag{1.34}$$

Also, for the practical case Y accounts for the parallel combination of the output conductance G_p and the terminating capacitances $C_1 = C_2 = C$, i.e.,

$$Y = G_p + j\omega C \tag{1.35}$$

so that equation 1.34 becomes to a first order approximation

$$G_p - \omega^2 C\tau \pm jg = 0 \quad . \tag{1.36}$$

As shown by Van Looij and Adams[5], the Q factor at higher frequencies becomes

$$Q = \frac{1}{\frac{1}{Q_o} - 2\tau\omega} \tag{1.37}$$

where $Q_o = g/2G_p$ is the Q factor at very low frequencies and 2τ is the transmission time constant from input to input. Equation 1.37 shows that, owing to the internal phase shift, Q increases with frequency, becoming infinite at $\omega = 1/2\tau\ Q_o$ and negative at higher frequencies.

Another method of demonstrating this effect can be achieved by going back to the original equation

$$Z_{IN} = \frac{1}{g_{12}\ g_{21}\ Z_L} . \tag{1.38}$$

Allowing for the high frequency effects,

$$Z_{IN} = \frac{j\omega C}{g^2} - \frac{2\omega^2 C\tau}{g^2} . \tag{1.39}$$

Thus, a negative input resistance equal to $-\frac{2\tau C\omega^2}{g^2}$ is observed as a result of the gyrator loop time delay. The equivalent inductance realized by the gyrator is equal to C/g^2 as before. The negative resistance will therefore contribute a negative Q factor, the magnitude of which is given by

$$Q = \frac{\omega L}{R} = \frac{1}{2\tau\omega} . \tag{1.40}$$

Thus, at higher frequencies, we may achieve any desired Q factor with the addition of a fixed resistance at the input port partially compensating the negative resistance as shown by Riordan[6].

It is possible to compensate the negative resistance effect

demonstrated by equation 1.39 completely, as the following considerations show; under the assumption of equation 1.32, the input admittance becomes

$$Y_{IN} = \frac{y_{12}y_{21}}{Y_2} = \frac{g_{12}g_{21}\,Z_L}{(1 + s\tau_1)(1 + s\tau_2)} \qquad (1.41)$$

where Z_L is the terminating impedance at the output port. If Z_L is taken as $(1 + s\tau_2)/sC_2$, i.e., a resistance $R_2 = \tau_2/C_2$ in series with the terminating capacirance C_2 as shown in figure 1.10. Upon substitution, the input impedance becomes

$$Z_{IN} = \frac{sC_2}{g_{12}g_{21}}(1 + s\tau_1) = sL(1 + s\tau_1) \qquad (1.42)$$

where $L = C_2/g_{12}g_{21}/$ If the gyrator combination shown by figure 1-10 is connected in parallel with the circuit of figure 1-11,

$$s^2C_1C_2 + g_{12}g_{21} = 0\,. \qquad (1.43)$$

Equation 1.43 is the characteristic equation of an undamped resonant circuit and is independent of the phase shift generated by the electronic circuit.

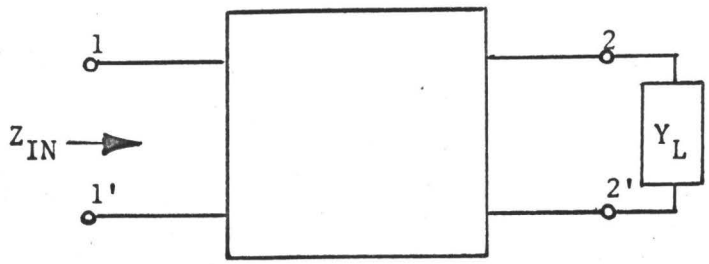


FIGURE 1-1: 2 Port Network

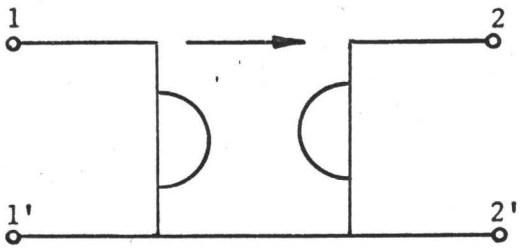


FIGURE 1-2: Equivalent Schematic of Gyrator

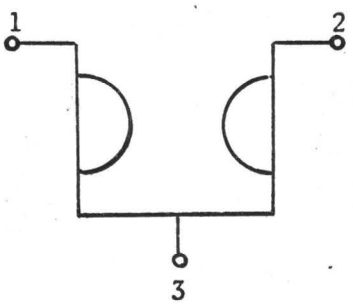


FIGURE 1-3: 3 Terminal Gyrator

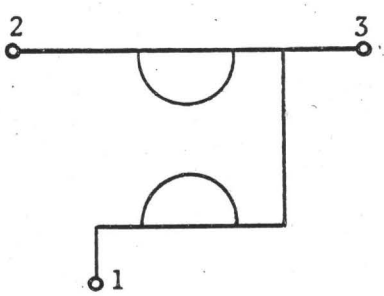


FIGURE 1-4: Grounded Gyrator Having Terminal 1 Connected to Ground

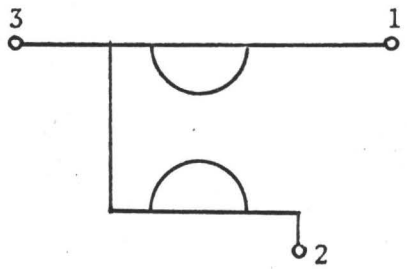


FIGURE 1-5: Grounded Gyrator

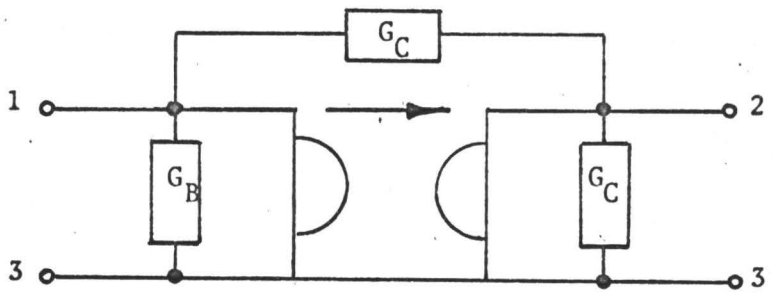


FIGURE 1-6: Equivalent π Network of Non-Ideal Gyrator

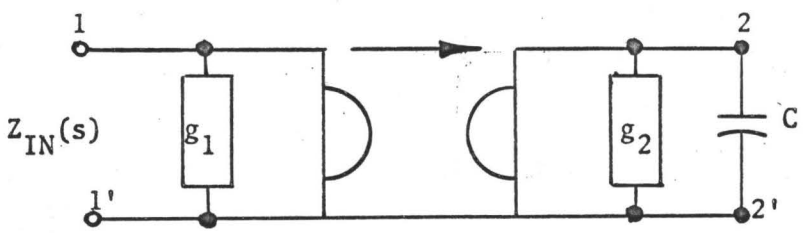


FIGURE 1-7: Simulated Inductor Using Non-Ideal Gyrator

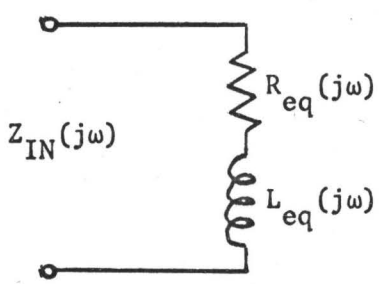


FIGURE 1-8: Equivalent Circuit of Simulated Inductor

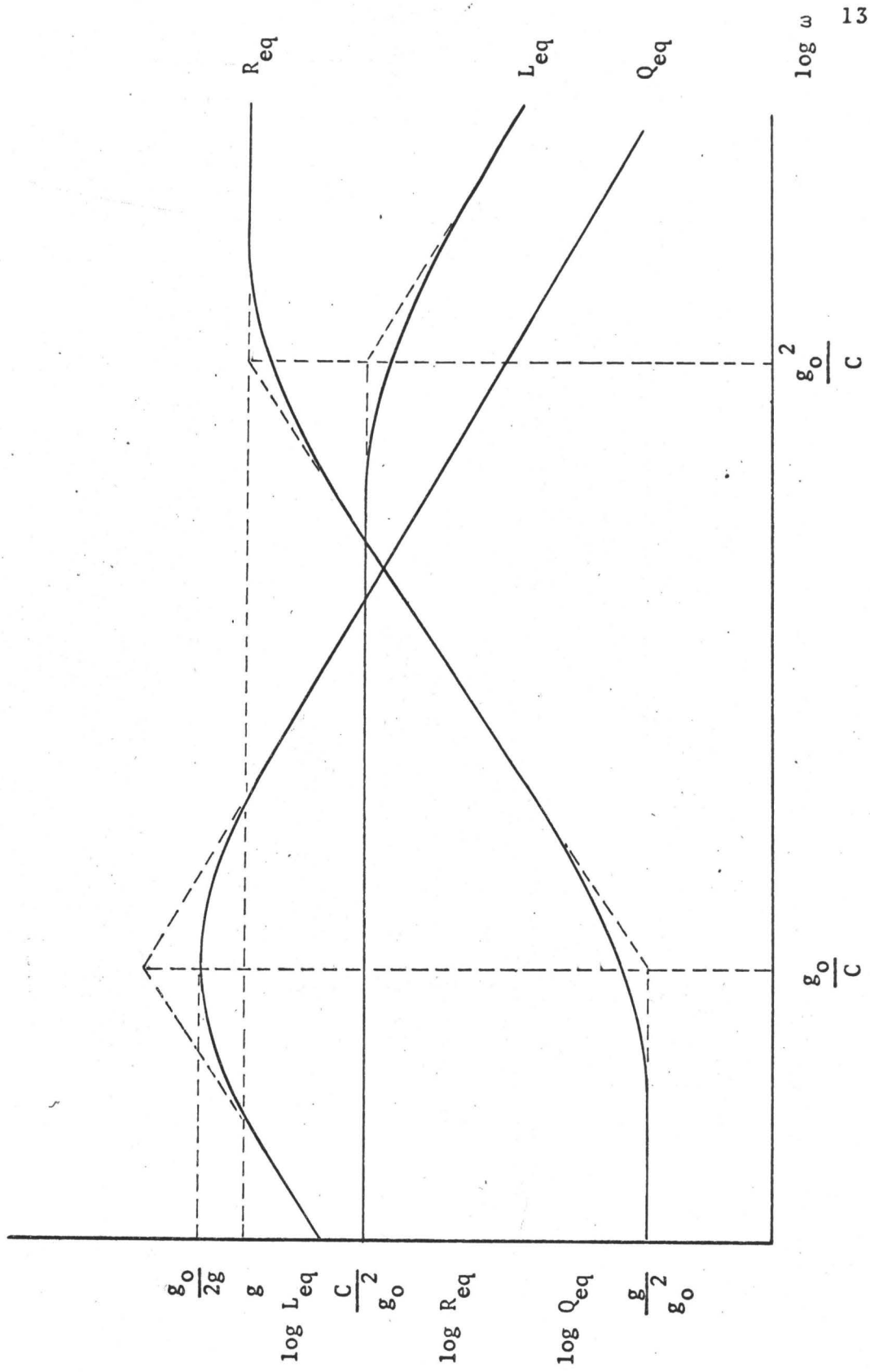


FIGURE 1-9: Equivalent Resistance, Inductance and Q Factor Relationship

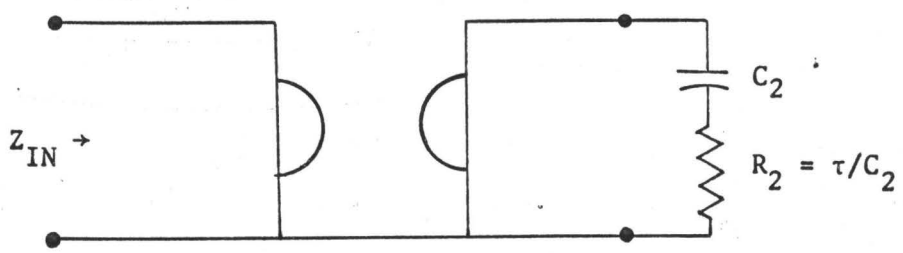


FIGURE 1-10: Compensation of Non-Ideal Gyrator

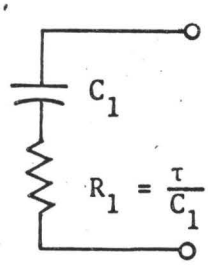


FIGURE 1-11: Input Compensation

CHAPTER II

GYRATOR REALIZATION

2.1 INTRODUCTION:

The various methods by which gyrators are realized are introduced in this chapter. Various types of circuits are given which are used to realize a gyrator. A brief introduction is given to the circuit which will be evaluated and tested fully in the subsequent chapters of the thesis.

Realizations of the gyrator using transimpedance amplifiers, and negative impedance inverters and negative impedance converters are also given.

2.2. PARALLEL CONNECTION OF TWO OPPOSITELY DIRECTED TRANSCONDUCTANCE AMPLIFIERS:

The Y matrix of an ideal gyrator may be split up as expressed by

$$\begin{vmatrix} 0 & g \\ -g & 0 \end{vmatrix} = \begin{vmatrix} 0 & 0 \\ -g & 0 \end{vmatrix} + \begin{vmatrix} 0 & g \\ 0 & 0 \end{vmatrix} \qquad (2.1)$$

The two component matrices on the right hand side of equation 2.1 represent two transconductance amplifiers transmitting in opposite directions. That is, they are voltage controlled current sources of opposite polarity, connected in parallel to form a closed loop. One amplifier has zero phase shift from input to output while the other amplifier has 180° phase shift. To realize y_{11} and y_{22} according to equation 2.1, both amplifiers must have high input and output impedances. Such a configuration is shown in figure 2-1.

2.2.1 Realizations Using Operational Amplifiers -

To realize the controlled sources, consider the operational amplifier circuit shown in figure 2-2[7],[8]. The admittance between ports 1 and 3 with the terminals of port 2 shorted together is

$$\begin{vmatrix} I_1 \\ I_3 \end{vmatrix} = \begin{vmatrix} \frac{1}{2R} & 0 \\ \frac{1}{\alpha R} & \frac{1}{R_s} \end{vmatrix} \begin{vmatrix} V_1 \\ V_3 \end{vmatrix} \tag{2.2}$$

where

$$R_s = \frac{\alpha\beta R}{\alpha\beta + \alpha - \beta} \tag{2.3}$$

and α and β are constants shown in figure 2-2. Similarly, the admittance matrix between ports 2 and 3 with port 1 shorted to ground is

$$\begin{vmatrix} I_3 \\ I_2 \end{vmatrix} = \begin{vmatrix} \frac{1}{R_s} & -\frac{1}{\alpha R} \\ 0 & \frac{1}{2R} \end{vmatrix} \begin{vmatrix} V_3 \\ V_2 \end{vmatrix} \tag{2.4}$$

By appropriately connecting together the current sources given by equations 2.4 and 2.2, the following admittance matrix is obtained:

$$Y = \begin{vmatrix} \frac{1}{2R} + \frac{1}{R_s} & -\frac{1}{\alpha R} \\ \frac{1}{\alpha R} & \frac{1}{R_s} + \frac{1}{2R} \end{vmatrix} \tag{2.5}$$

If G is allowed to be $\frac{1}{\alpha R}$, and

$$K = \frac{\alpha(R + \frac{R_s}{2})}{R_s} \tag{2.6}$$

the Y matrix becomes

$$Y = \begin{vmatrix} K & -G \\ G & K \end{vmatrix} . \qquad (2.7)$$

From equations 2.3 and 2.6 it is seen that

$$K = \frac{3/2\alpha\beta + \alpha - \beta}{\alpha\beta} . \qquad (2.8)$$

Inspection of equation 2.8 shows that K will be zero if

$$\alpha = \frac{\beta}{3/2\beta + 1} . \qquad (2.9)$$

Under these conditions, the circuit of figure 2-3 will function as an ideal gyrator. It is noted from figure 2-3 that there is a terminal common to both inputs, that is, the realization shown is a grounded gyrator. By the parallel connection of two grounded gyrators having the same direction of gyration, a floating gyrator is obtained.

The circuit of figure 2-3 requires a total of four operational amplifiers. By the use of differential amplifiers, the number can be reduced to only two, as shown in figure 2-4[6].

Assuming that the open loop amplifier gains are high,

$$V_2 \doteq V_1(1 + \frac{Z_2}{Z_1}) \qquad (2.10)$$

and

$$V_3 \doteq V_1(1 - \frac{Z_2Z_4}{Z_1Z_3}) \qquad (2.11)$$

$$I_1 = \frac{V_1 - V_3}{Z_5} = \frac{Z_4Z_2\,V_1}{Z_1Z_3Z_5} . \qquad (2.12)$$

Thus the input impedance Z_{IN} is

$$Z_{IN} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \tag{2.13}$$

If either Z_2 or Z_4 is a capacitor and all other elements are resistors, of equal value, Z_{IN} becomes:

$$Z_{IN} = j\omega CR^2 \tag{2.14}$$

If both Z_2 and Z_4 are capacitors, Z_{IN} becomes:

$$Z_{IN} = -\omega^2 C^2 R^3 \tag{2.15}$$

If a variable resistor Ra is connected in series with the input, the circuit becomes a tuneable filter with resonant frequency

$$\omega_o^2 = \frac{Ra}{C^2 R^3} \tag{2.16}$$

2.2.2. Realizations Using Discrete Components -

Thus far, the realizations of gyrators have been carried out using operational amplifiers having finite gains and high but finite input impedances. Considerations now will be given to realizing near ideal voltage controlled current sources, which are suitable for integrated circuit implementation.

Consider the circuit given by figure 2-5[9]. It represents a gyrator of very simple form which is still capable of giving good performance. It is essentially a direct coupled version of Shenoi's gyrator[10] with constant current sources replacing the load resistors, and without biasing resistors (unnecessary with direct coupling) with both improvements reducing the y_{ii} terms of equation 1-15.

The circuit of figure 2-6 incorporates several improvements[11]. The use of differential stages leads to better operating point stability and the use of two stages for each controlled source has the following advantages; First, the direct voltage components at each port of the gyrator may be set independently (i.e., to zero). Secondly, the input admittance of each controlled source (which should be zero) may be decreased by increasing the emitter feedback resistor of the differential stage without decreasing the transconductance which is what occurs with the single stage controlled sources in figure 2-5.

The gyrator as given by figures 2-5 and 2-6 have one terminal of each port returned to ground, so that a floating gyrator can be realized by the use of two gyrators. However, with a small number of changes, a semi-floating gyrator can be obtained. The circuit of figure 2-7 can realize a floating gyrator with the addition of a few components. Again this circuit is based on the antiparallel connection of two transconductances. The use of differential amplifier stages allows one or both ports to be floating. Usually it will not be necessary to have both ports floating since the port to which the capacitor is connected can also have one terminal grounded (see figure 2-7).

2.2.3 Realizations Using Integrated Circuits -

Numerous transistorized gyrator circuits have been proposed. Although generally of high performance, they contain one or more of the following characteristics which make them difficult to be fully integrated inexpensively using present day integrated circuit technology:

(a) mos., pnp and npn transistors in the circuit,

(b) coupling capacitors or high quality pnp and npn transistors, or both,

(c) negative resistors or NICS.

An integrated circect-coupled gyrator has been reported[12] as shown in figure 2-9. It contains 12 low value resistors, 1 diode, 7 npn transistors and 2 low current lateral pnp transistors. The circuit consists of two cross-coupled voltage controlled current sources, one of which has its output current in phase with the input voltage; the other has its output 180° out of phase with the input. The high impedance of the current source is achieved by a pnp and an npn transistor connected in a push pull arrangement. Since high quality floating pnp transistors are difficult to make in an integrated circuit without additional diffusion steps, a lateral pnp transistor is compounded with an npn transistor to replace the pnp transistor.

The experimental results obtained for the direct coupled gyrator of figure 2-9 show close agreement with the theoretical expected results and being stable with frequencies up to 65 KHz.

A difficult version of a direct coupled gyrator is shown in figure 2-10. The circuit consists of two amplifiers transmitting in opposite directions. The two amplifiers are shown individually in figures 2-11 and 2-12. The circuit of figure 2-11 is an inverting amplifier whose output is 180° out of phase with the input while the circuit of figure 2-12 is a non-inverting amplifier with the output in phase with the input.

The inverting amplifier has the first transistor Q_1 in the common collector mode. The second transistor Q_2 is used in the common emitter

mode with a feedback resistor R_5 in the emitter circuit. The load resistor of transistor Q_2 is resistor R_7 in parallel with the input impedance of the Q_3 - Q_4 combination. Q_3 is a lateral pnp transistor having a low h_{fe} of one. It is connected to an npn transistor Q_4 giving an overall h_{fe} of $h_{fe\ pnp}(1 + h_{fe\ npn})$. This is equivalent to the performance of a pnp transistor having an h_{fe} equal to that of the npn transistor. The Q_3 - Q_4 transistor combination is operated in the common base mode, with the collector load resistance being presented by a high impedance current sink obtained with transistor Q_5 operating in the common base mode.

Transistors Q_6 and Q_7 are connected in a Darlington arrangement to give the non-inverting amplifier a high current gain as well as a high input impedance. The Q_6 - Q_7 combination is operated in the common collector mode with its load being resistor R_3 in series with the parallel combination of resistor R_2 and the base input impedance of transistor Q_8. The load resistor of transistor Q_8 is the impedance of the current sink provided by the Q_9 - Q_{10} transistor combination. A thorough analysis of the two amplifiers of figures 2-11 and 2-12 is given in Appendix I.

2.3 SERIES CONNECTION OF TWO OPPOSITELY DIRECTED TRANSRESISTANCE AMPLIFIERS:

The Z matrix of an ideal gyrator with a gyration direction from right to left is given by

$$Z = \begin{bmatrix} 0 & R \\ -R & 0 \end{bmatrix} \qquad (2.17)$$

where R is the gyration resistance. In addition, it is characterized by its zero input and zero output impedance. This matrix can be split up

as shown by equation 2.18,

$$Z = \begin{bmatrix} 0 & R \\ -R & 0 \end{bmatrix} = \begin{bmatrix} 0 & R \\ 0 & 0 \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ -R & 0 \end{bmatrix} \qquad (2\text{-}18)$$

where each matrix on the left hand side of equation 2.18 is realized by amplifiers having a transresistance of value R, one having an output which is in phase with the input while the other has an output which is 180° out of phase with the input. Each amplifier must have both low input impedance and low output impedance. The amplifiers are connected in series transmitting in opposite directions, as shown in figure 2-13.

2.4 CASCADE CONNECTION OF A NEGATIVE IMPEDANCE CONVERTER AND A NEGATIVE IMPEDANCE INVERTER:

An ideal gyrator can also be realized in an indirect manner by the connection of a negative impedance converter (NIC) of the voltage inversion or current inversion type, and a negative impedance inverter (NII) connected in tandem. A NII is a two-port device whose immittance matrix is

$$Z_{NIC} = \begin{bmatrix} 0 & R \\ R & 0 \end{bmatrix} \text{ , or} \qquad (2.19a)$$

$$Y_{NII} = \begin{bmatrix} 0 & G \\ G & 0 \end{bmatrix} \qquad (2.19b)$$

where R and G are real constants and may either be positive or negative. Referring to figure 2-14, when a NII is terminated in a load impedance Z_2 at one port, the input impedance Z_{in} at the other port is the negative of Z_L and inversely proportional to it. Specifically,

$$Z_{IN} = -R^2 / Z_L \qquad (2.20)$$

An NII can be realized by spliting up the Z matrix of equation 2.19a and realizing each matrix by an ideal current controlled voltage source. Such an ideal controlled source is represented by the circuit of figure 2-15, in which $V_2 = RI_1$. In practice, such an ideal source can easily be approximated. Figure 2-16 depicts a representation of a practical amplifier that approximates the ideal controlled source of figure 2-15. It has an impedance matrix:

$$Z = \begin{bmatrix} r_i & 0 \\ R & r_o \end{bmatrix} \tag{2.21}$$

in which r_i, $r_o < R$.

When two such amplifiers are connected in series as shown by figure 2-17, the resultant matrix is:

$$Z = \begin{bmatrix} r_o + r_i & R \\ R & r_o + r_i \end{bmatrix} = \begin{bmatrix} r & R \\ R & r \end{bmatrix} \tag{2.22}$$

The NIC is a two-port device whose input impedance is, ideally, the negative of the impedance at its output terminals. The equations defining an ideal current-inversion negative impedance converter (INIC) are:

$$V_1 = V_2 \tag{2.23}$$

$$I_1 = KI_2 \tag{2.24}$$

where the constant K is the device's gain, and the input impedance, Z_{IN}, equals

$$Z_{IN} = \frac{V_1}{I_1} = -\frac{Z_L}{K} \tag{2.25}$$

The input impedance is 1/K times the negative load impedance Z_L, and so the magnitude of this negative impedance can be varied by changing K.

Similarly, if an impedance Z_L is connected across the input, the output impedance Z_{OUT} equals

$$Z_{OUT} = \frac{V_2}{I_2} = -KZ_L \tag{2.26}$$

The INIC gives the same result in both directions when K equals unity. The first

The first transistorized NIC was designed in 1953 by J. Linvill[13] and several others have since been developed[14],[15],[16],[17],[18]. Several operational amplifier circuits have been proposed as negative impedance converters as shown in figure 2-18. In the configurations shown, when $R_1 = R_2$,

$$g_{11} \doteq \frac{(R + R_1)^2}{R_1 R^2 G_2} \tag{2.27}$$

$$g_{12} \simeq 1 - \frac{R_1(R + R_1)}{R_1 R G_2} \tag{2.28}$$

$$g_{21} \simeq 1 - \frac{(R + R_1)}{R G_2} \tag{2.29}$$

$$g_{22} \simeq \frac{R_1}{G_2} \tag{2.30}$$

where G_2 is the voltage gain of operational amplifier A_2. As the gain of

A_2 approaches ∞, then,

$$g_{11} \to 0,\ g_{22} \to 0,$$

$$g_{12} = 1,\ g_{21} = 1,$$

and the g matrix becomes

$$\begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \tag{2.31}$$

Having established the properties of the NII and the NIC, suppose the cascade connection of a NIC and a NII is terminated with an impedance Z_L at the output port as shown in figure 2-19. Then the impedance measured looking into the input port of the NII is $-R^2/Z_L$. This impedance acts as a load for the NIC, so that if the NIC is of unity conversion ratio, the impedance measured looking into the input port of the NIC will be R^2/Z_L, indicating that the cascade connection of the NII and NIC is equivalent to an ideal gyrator.

However, it should be noted that a major disadvantage of the realization schemes based on the use of NIC's and NII's is that such devices are inherently potentially unstable, so that, unless the necessary precautions are taken, the complete circuit may break into oscillations.

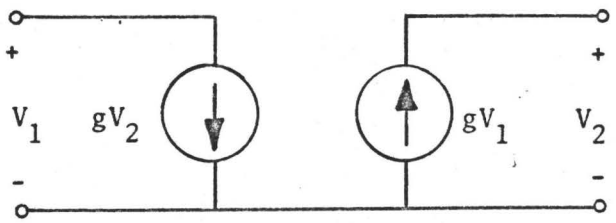


FIGURE 2-1: Ideal Gyrator Realized with Current Sources

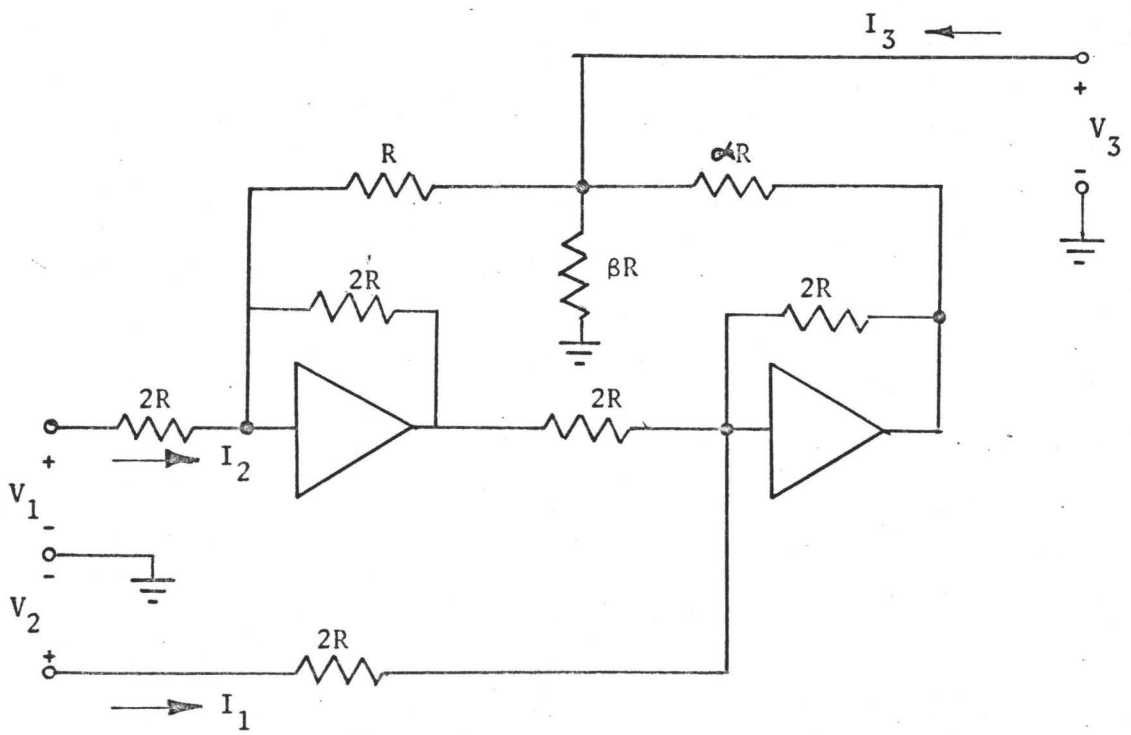


FIGURE 2-2: A Voltage Controlled Current Source

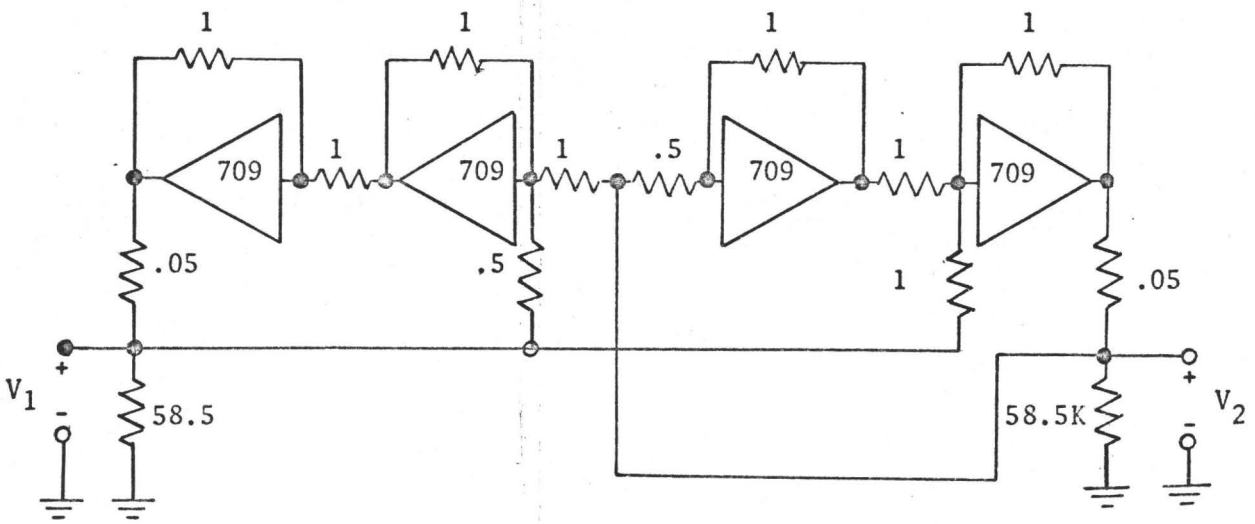


FIGURE 2-3: A Gyrator Realization Using Operational Amplifiers

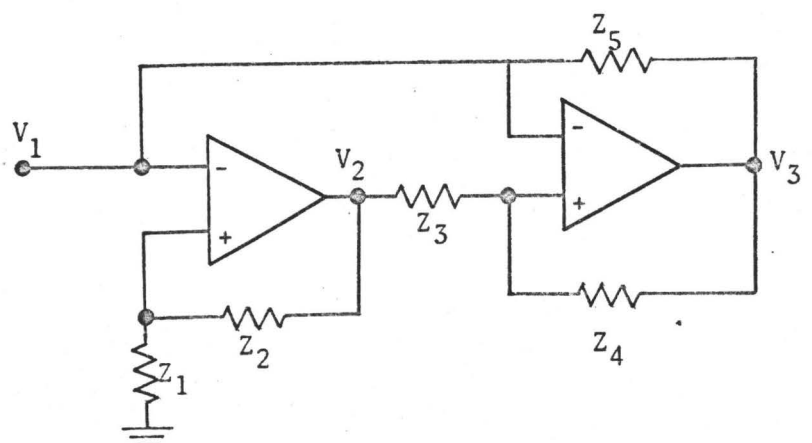


FIGURE 2-4: Grounded Gyrator Using Differential Amplifiers

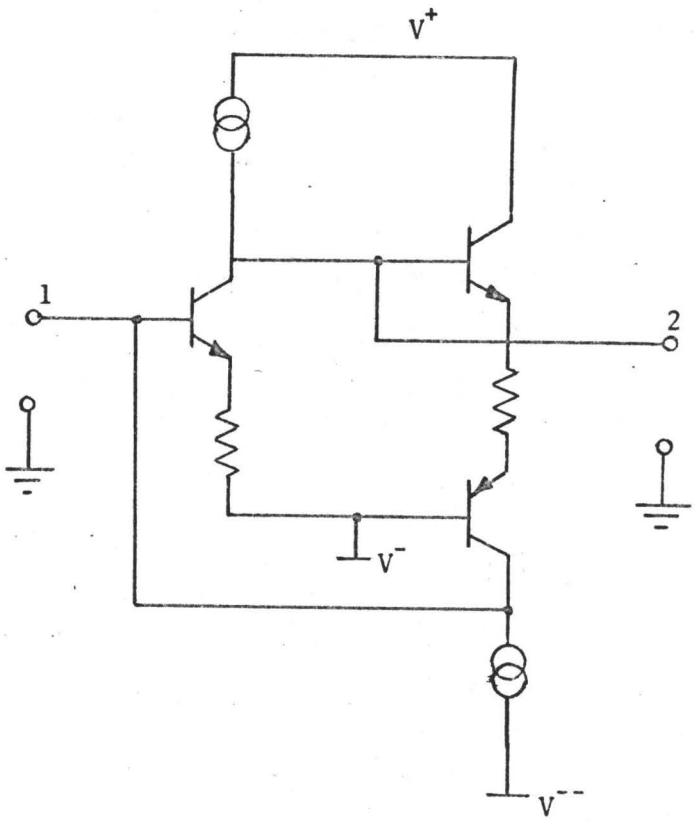


FIGURE 2-5: Grounded Gyrator Using Discrete Components

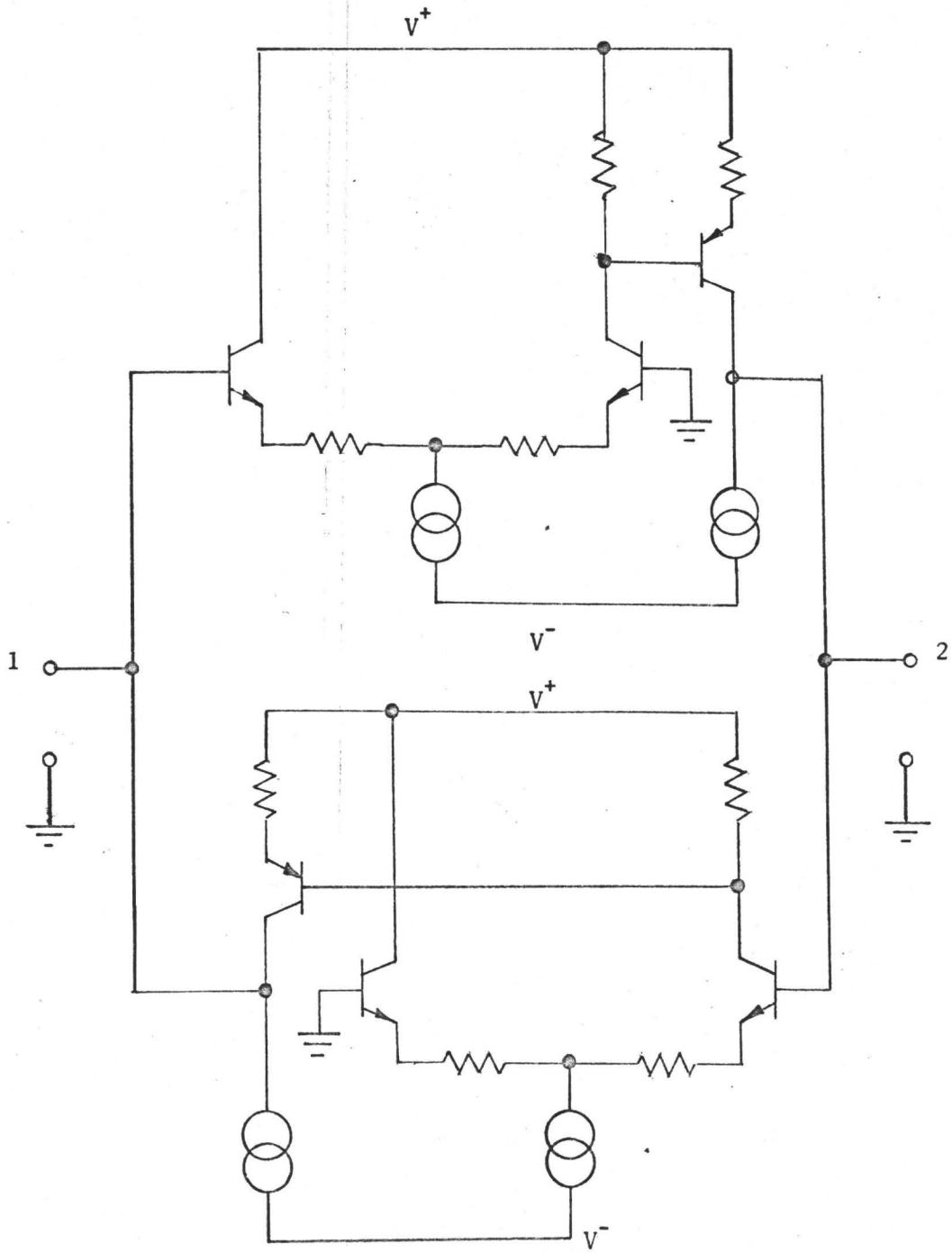


FIGURE 2-6: Grounded Gyrator Realization Using Differential Transistor Stages

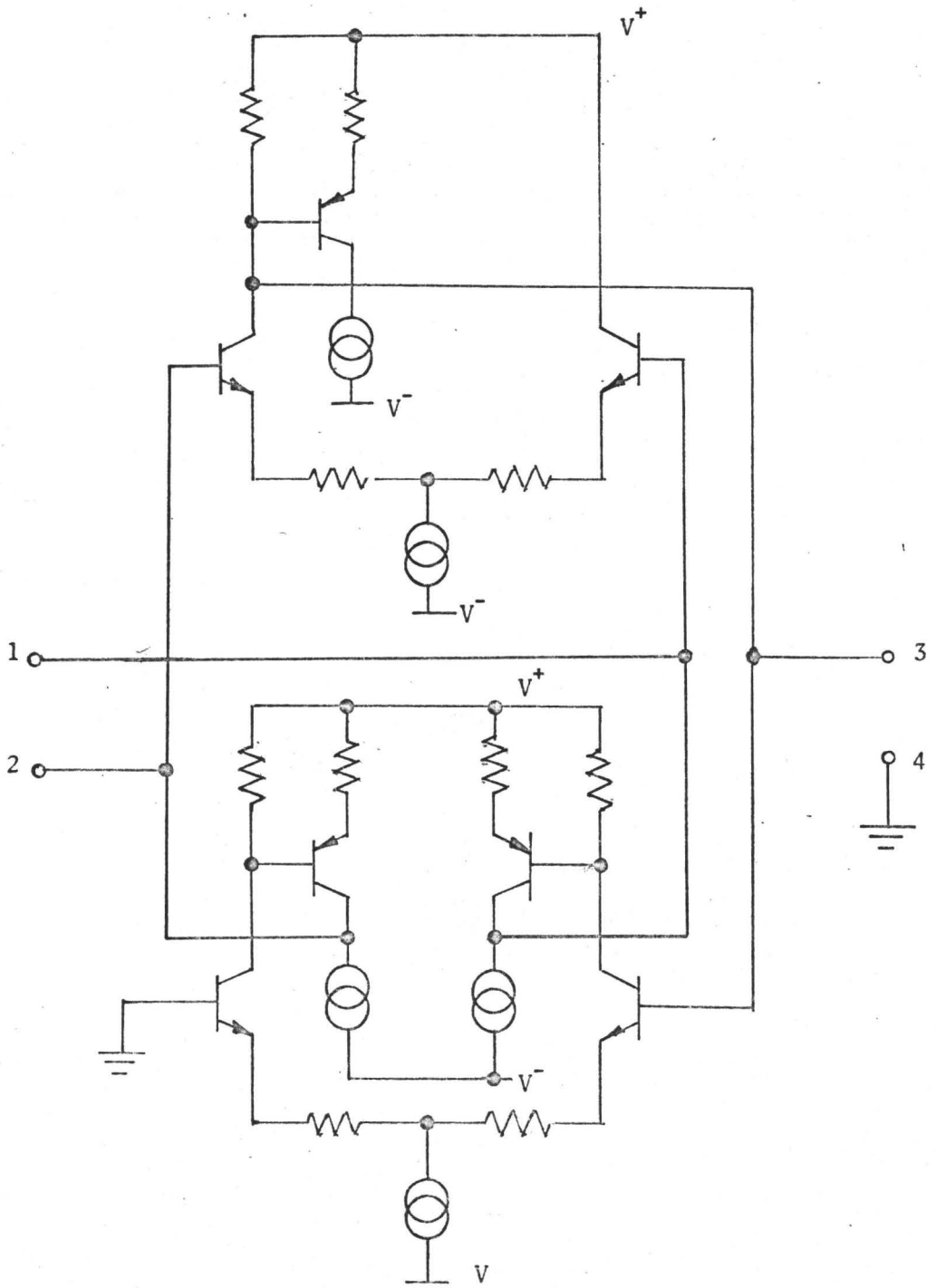


FIGURE 2-7: Semi-Floating Gyrator

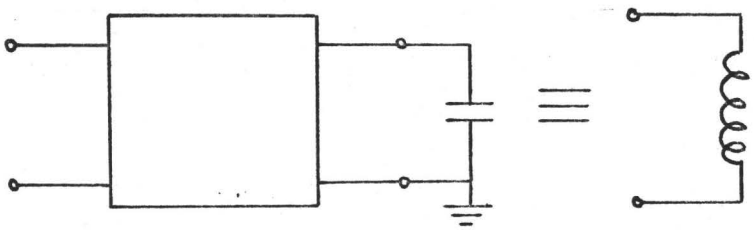


FIGURE 2-8: Simulated Floating Inductor

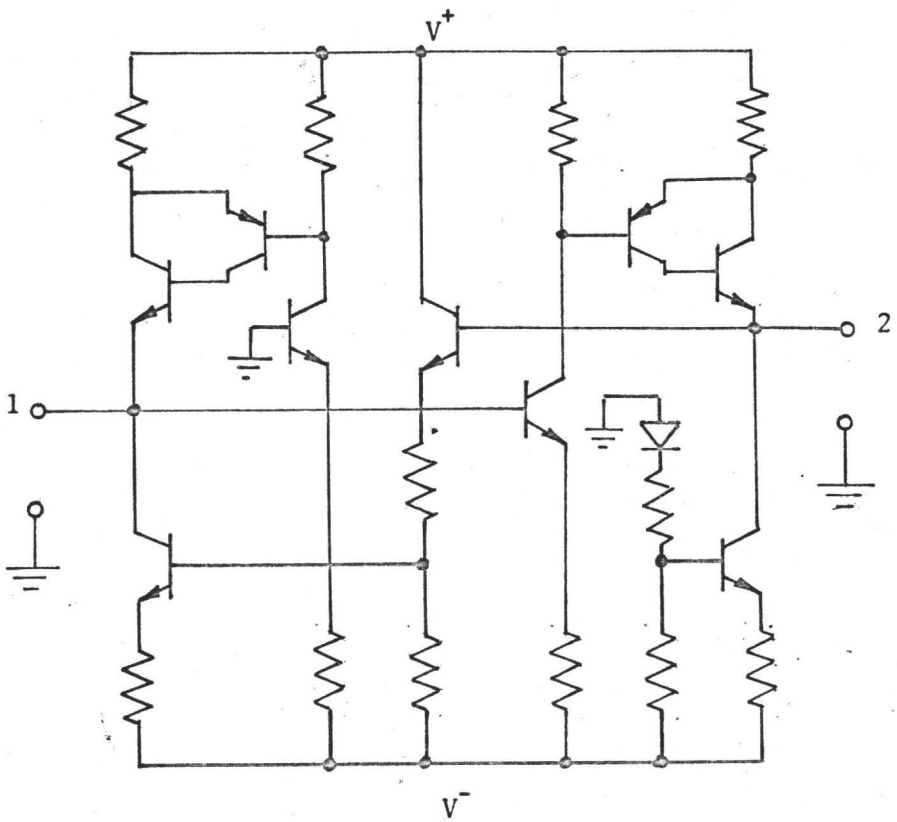


FIGURE 2-9: Direct Coupled Integrated Grounded Gyrator

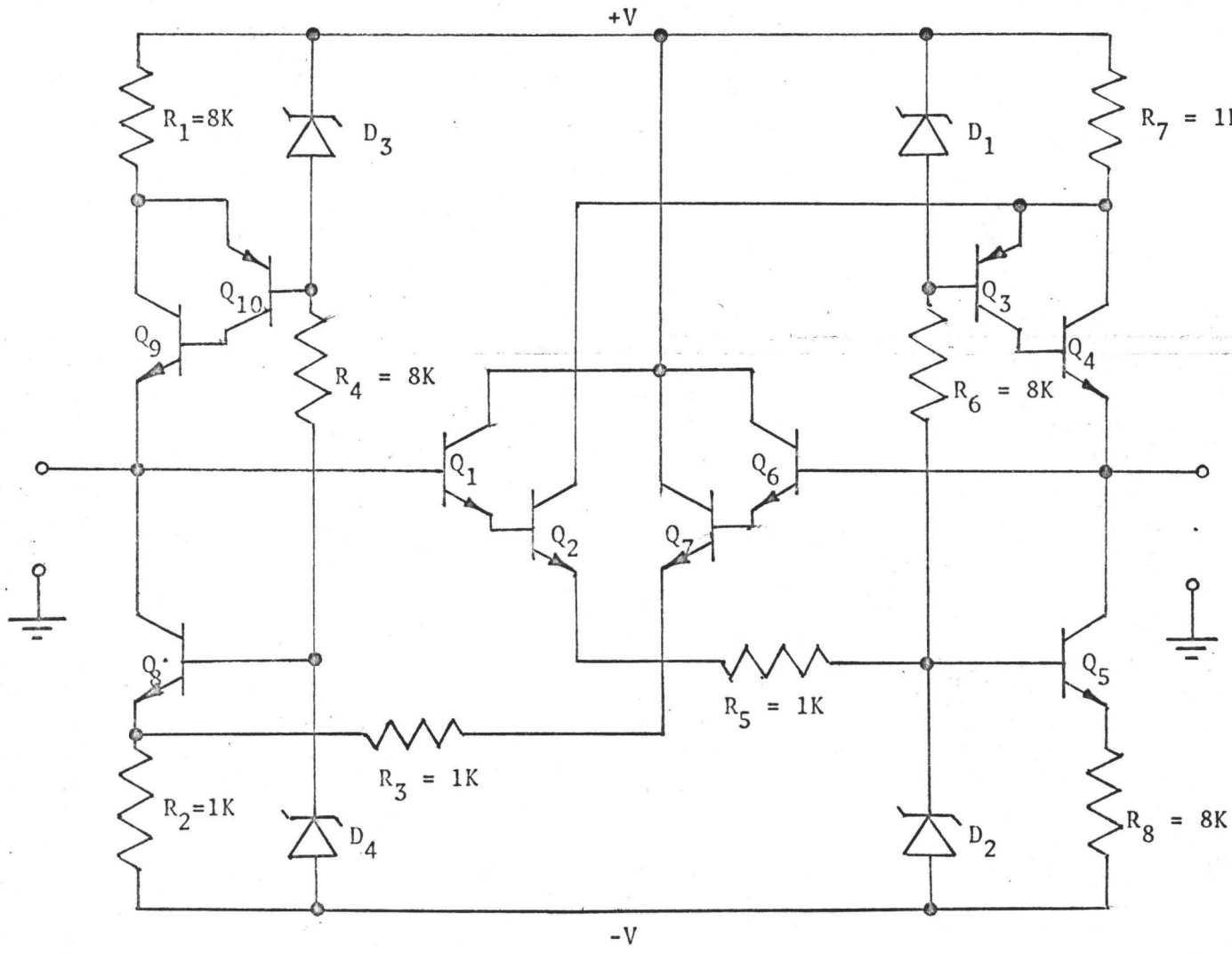


FIGURE 2-10: Improved Integrated Grounded Gyrator

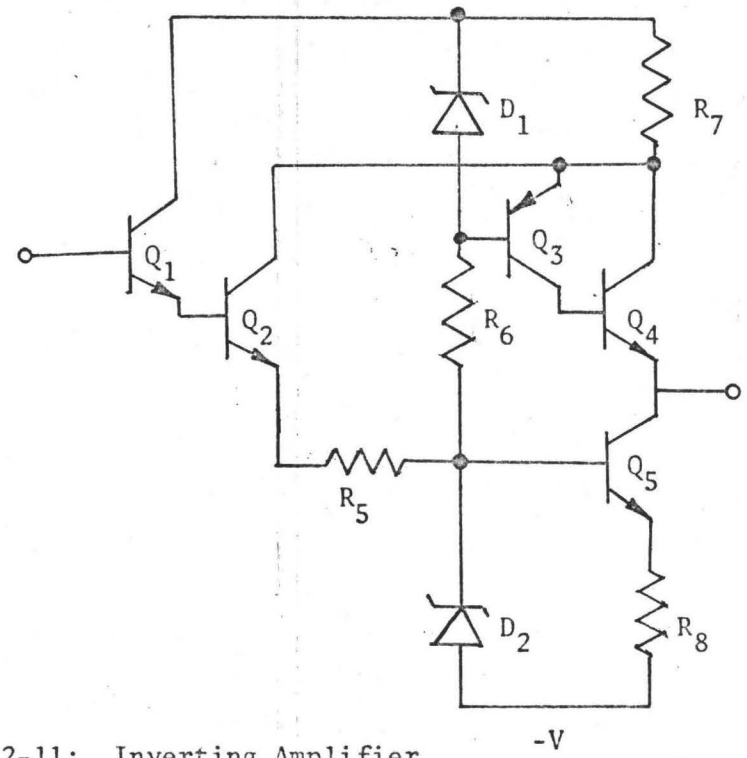


FIGURE 2-11: Inverting Amplifier

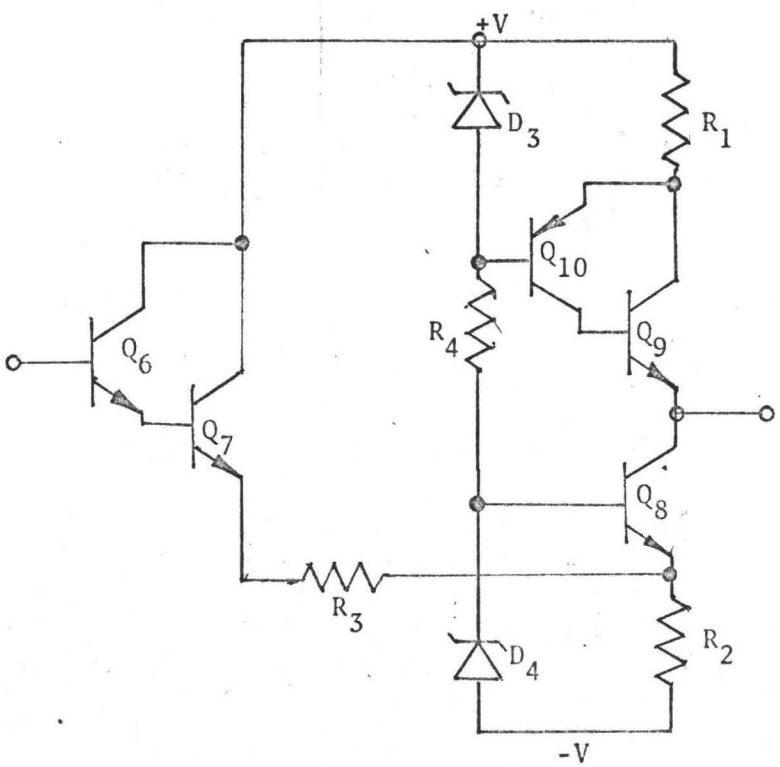


FIGURE 2-12: Non-Inverting Amplifier

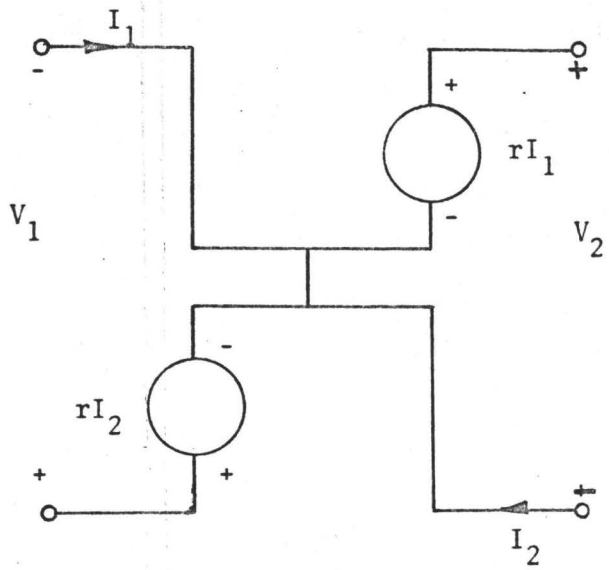


FIGURE 2-13: Series Connection of Two Transresistance Amplifiers

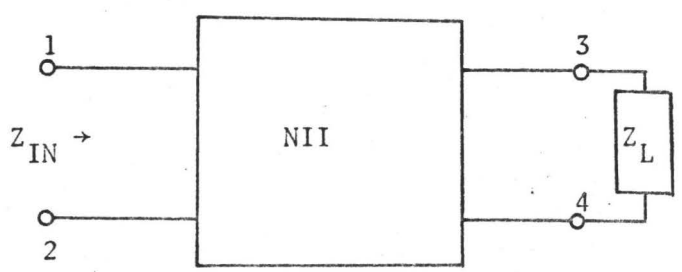


FIGURE 2-14: Negative Impedance Realized Using NII

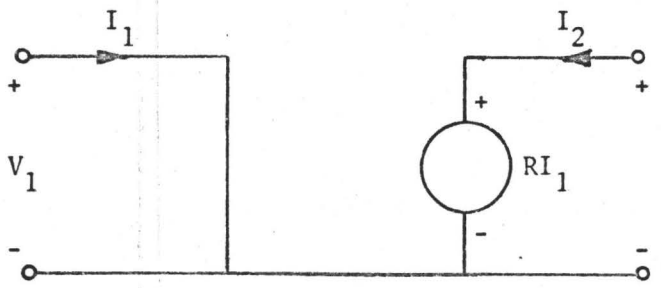


FIGURE 2-15: Current Controlled Voltage Source

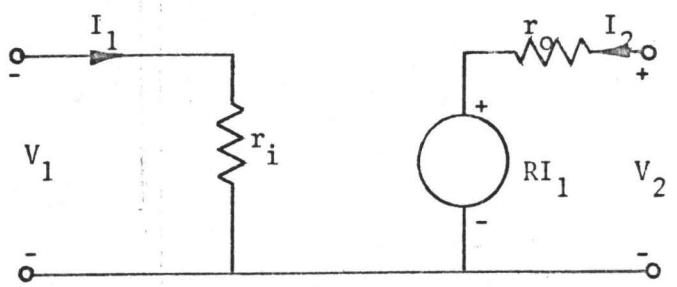


FIGURE 2-16: Practical Voltage Source

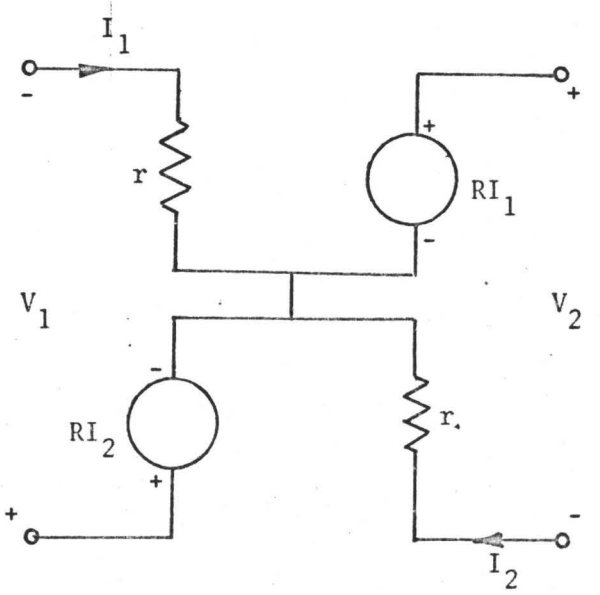
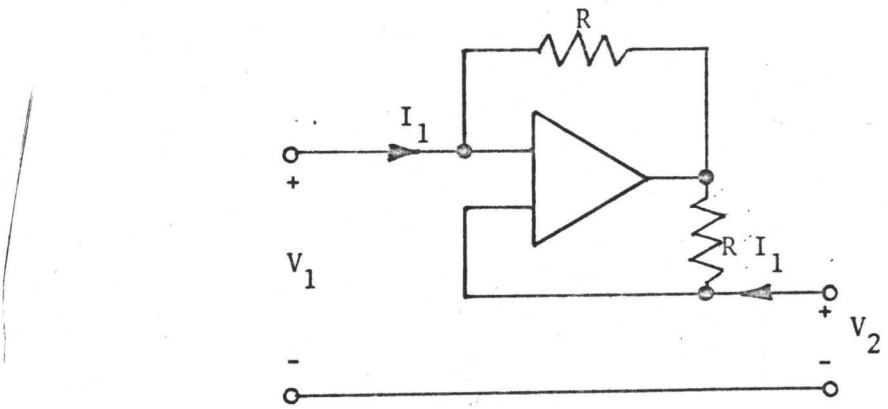
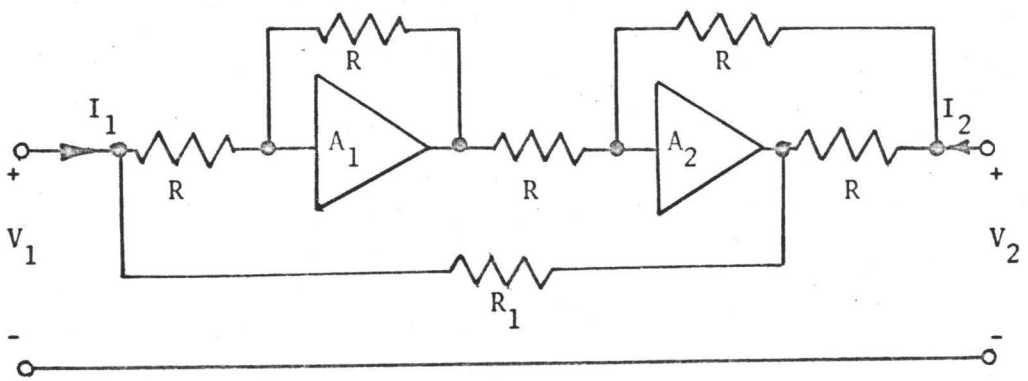


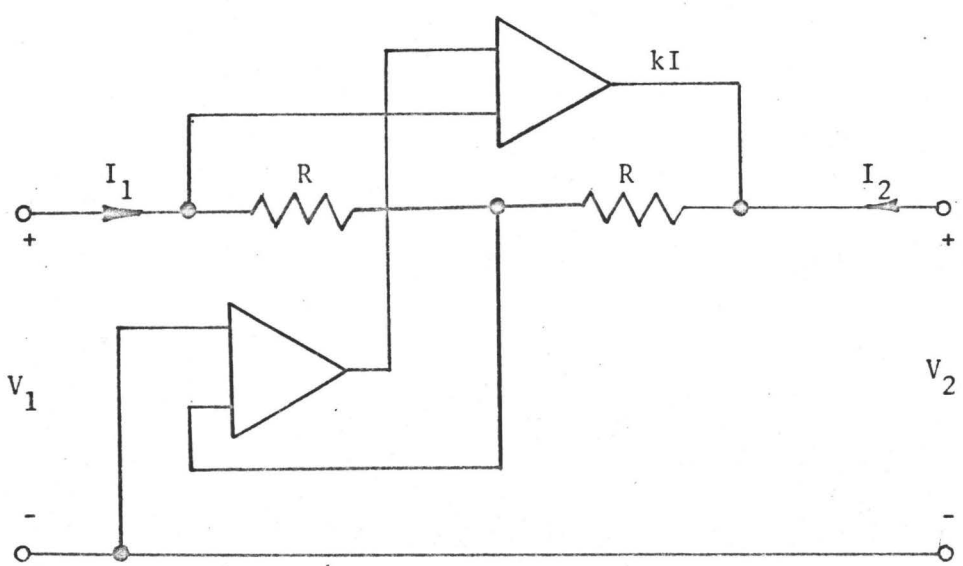
FIGURE 2-17: Non-Ideal NII



(a)



(b)



(c)

FIGURE 2-18: Practical Negative Impedance Converters Using Operational Amplifiers

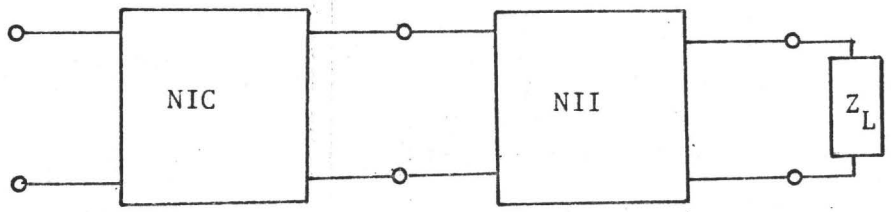


FIGURE 2-19: Gyrator Obtained Using a NII and a NIC

CHAPTER III

INTEGRATED CIRCUIT DESIGN

3.1 INTRODUCTION:

The proper design and application of integrated circuit systems requires an understanding of the basic processes which are used to fabricate the device. This chapter is written in order to obtain a working knowledge of the advantages and disadvantages of monolithic integrated circuits. Listed are the major processing steps used to fabricate the active and passive components used in the direct coupled grounded gyrator.

3.2 FUNDAMENTALS OF MONOLITHIC DESIGN:

The root of the term monolithic may be traced to the Greek: mono - meaning single, and lithos - meaning stone. A monolithic circuit, literally speaking, means a circuit fabricated from a single stone, or single crystal. Monolithic circuits are, in fact, made in a single piece of single-crystal silicon.

Ideally, it would be desirable to fabricate a complete integrated circuit with the same number of process steps required for the most complex component in the circuit. In most instances, this is the three-layer two-junction transistor structure. With a semiconductor monolithic integrated circuit it is possible to approximate this ideal. Two diffusions are necessary to fabricate the base and emitter, respectively, of the integrated transistor. With the monolithic semiconductor circuit,

it is possible to utilize these diffusion cycles also to produce the diffused resistors and capacitors. Hence, no additional steps are necessary for the fabrication of these components. The only added processes, therefore, are those required for electrical isolation and buried layer diffusion of the various parts of a given circuit and those for interconnecting the components of the circuit. It can be seen then, that transistor fabrication represents the basis for the manufacturing of monolithic integrated circuits.

The conventional planar or annular transistor structure consists of three separate semiconductor layers. The parent material of the wafer, called the substrate, represents the collector region into which, by consecutive masked etching and diffusion processes, the base and emitter regions are fabricated. In this fabrication procedure, all transistors on a wafer have a common collector - a procedure which is perfectly permissible since the wafer will subsequently be cut apart into individual transistor dice.

With monolithic integrated circuits, where additional component parts occupy the same die as the transistor, a common substrate is intolerable since the various parts must be electrically isolated from one another. This isolation has been accomplished by electrically isolating the substrate from the active circuit by means of p-n junctions.

The transistor for monolithic semiconductor circuits (figure 3-1) thus differs from its conventional counterpart in that it contains 3 junctions and four semiconductor layers. The extra layer, or region, is the substrate which the monolithic transistor shares with the other integrated circuit components. The p-n junction formed by the transistor

collector region and the substrate represents a diode which, when held in a reverse-biased state, isolates the transistors from the other parts. This form of diode isolation is illustrated in figure 3-2. Here it is seen that, as long as the p-type substrate is held at a more negative voltage than either or both transistor collector regions, the transistors are separated by the high dc resistance of a back-biased diode. There is, however, a capacitive coupling between the components because of the capacitance associated with the isolating p-n junctions. This form of diode isolation is used between elements of many types of monolithic circuits.

3.3 THE NPN SILICON PROCESS:

Fabrication of an epitaxial-diffused integrated circuit begins with a wafer of p-type silicon, with the correct doping density, of about 5 ohm-cm. The starting wafer is either polished to a mirror finish and used directly or subjected to a light final etch to eliminate the final vestiges of surface damage resulting from the polishing operation.

3.3.1 Oxidation -

The first step is the oxidation of the p-type silicon wafer if patterned buried layers are used. This oxide is used to mask the pattern for the buried layer diffusion if a uniform buried layer (over the entire substrate surface), or if no buried layer is employed, the first oxidation will occur after expitaxial growth. The SiO_2 (a highly pure form of common glass) provides a barrier to the diffusants. For effective masking, the thickness ranges between 2000Å and 10,000 Å. It has a shiny or glassy metallic appearance and, depending on its thickness, appears pink,

green, blue or grey. The latter colours are most pronounced as a result of boron and phosphorous doping, respectively,

3.3.2 Buried Layer -

The purpose of the buried layer is to reduce the series collector resistance providing a low resistance path between the collector and emitter contacts. Arsenic or antimony is usually used because of their high solubility and low diffusion coefficient compared with boron and phosphorous. This assures low resistivity and only small amounts of additional diffusion during the latter processing steps (figure 3-3). A doping level of 10^{21} atoms per cubic cm is desired to reduce the sheet resistivity to the lowest possible value obtainable with arsenic.

3.3.3 Epitaxial Layer -

An N-type expitaxial layer is grown after the oxide layer has been removed from the wafer. Phosphine may be used for the N-type doping required (figure 3-4). Typical thickness is 10 - 15 microns with a resistivity of 0.5 ohm-cm $\pm$ 10 percent. This N-type epitaxial layer ultimately becomes the collector regions of transistors or an element of the diodes and diffused capacitors, associated with the circuit. Remaining elements of transistors, diodes, and capacitors, as well as resistors, are formed by subsequent diffusion processes.

3.3.4 Re-Oxidation -

After the epitaxial layer is grown, a new oxide layer is grown over the entire surface to provide the necessary mask for the subsequent isolation diffusion. In practice a 10,000 Å layer is employed. Oxide layers for re-oxidations subsequent to this step, are grown simultaneously

or as the concluding part of the diffusion process, i.e., isolation, base, and emitter diffusion. Either oxygen or water vapour is introduced to enhance the oxide growth.

3.3.5 Isolation Diffusion -

The epitaxial wafer is prepared for an "isolation" diffusion step by means of a photolithographic process. In the process, the wafer is covered with a uniform film of photosensitive emulsion. Unless polymerized, this material is quite readily soluble in certain liquids. Polymerization of the photo resist can be accomplished by exposure to ultraviolet light. By exposing it to ultraviolet light through an apppropriate photographic mask, the polymerization can be made to take place only in the desired areas. The unpolymerized film is readily removed, leaving a polymer which covers selected areas and which is highly resistant to corrosive etches. An etchant containing hydrofluoric acid can be then used to remove the SiO_2 layer where the unpolymerized emulsion has been, leaving untouched the SiO_2 in the areas covered by the polymerized emulsion. (see figure 3-5). The remaining SiO_2 serves as a mask for the diffusion step which follows. The commonly used diffusants (in this case boron), diffuse much more slowly in SiO_2 than in silicon; hence the boron will penetrate into the silicon only in those areas in which the SiO_2 was removed by the etchant. The areas under the SiO_2 will not be exposed to the diffusant. This principle is the basis for all "masked diffusions", which are the heart of monolithic integrated circuit technology.

The wafer is now subjected to a p-type diffusion, during which the impurities enter the silicon only where the silicon dioxide has been removed. A time and temperature cycle is used which will ensure that the

p-type impurities diffuse through the epitaxial layer to the p-type substrate. The areas that remained covered with silicon dioxide are now isolated islands of n-type silicon surrounded by p-type. Isolation results because of the p-n junction formed around each n region, and between any two n regions these junctions result in back to back diodes so that no matter what polarity voltage might appear between the two "islands", there is always a back-biased diode between them.

During the diffusion cycle, a new layer of silicon dioxide grows over the diffused p-region, and the preexisting oxide over the n regions grows thicker.

3.3.6 Base Diffusion -

A second pattern, to form the transistor base regions, resistors, and the anode elements of diodes and junction capacitors, is etched in the silicon dioxide layer, using the photolithographic process previously described. p-type impurities such as boron, are again diffused through the openings into the islands of n-type epitaxial silicon. The depth of this diffusion is controlled so that it is quite shallow and does not penetrate through to the substrate. A layer of silicon dioxide is again grown over the diffused p-type regions (figure 3-6).

3.3.7 Emitter Diffusion -

The oxide coating is again selectively etched to open windows in the base regions, to permit the diffusion of phosphorous for the formation of transistor emitters, and cathode regions for diodes and capacitors.

Windows are also etched into n-regions, particularly those with

low surface concentration, where contact is to be made to the n-type layer, and phosphorous is diffused into these regions simultaneously with the emitter diffusion. This is necessary because aluminum is used as the contacting and interconnecting material. Aluminum is a p-type impurity in silicon, with a maximum solubility of 2×10^{19} atoms per cubic cm. Hence, a large surface concentration of phosphorous in the n region is required to prevent the formation of a p-n junction, when the aluminum is alloyed in, to form the contact.

Phosphorous, with a high surface concentration producing an n^+ region, is diffused to form the transistor emitter area, cathode region for diodes and capacitors, and contacts to the n-type areas. As before, a layer of silicon dioxide is grown over the diffused regions. At this point, the junction formation in the monolithic circuit is complete (figure 3-7).

3.3.8 Pre-Ohmic Etch -

In order to permit interconnection between the various components of the monolithic circuit, a fourth set of windows is etched in the silicon dioxide layer at the points where contact is to be made to each of the various components of the integrated circuits (figure 3-8).

3.3.9 Metalization -

A thin, even coating of aluminum is vacuum-deposited over the entire surface of the wafer. The interconnection pattern between components in the monolithic circuit is then formed by photoresist techniques. The undesired aluminum areas are etched away leaving a pattern of interconnections between transistors, resistors, diodes, and other circuit elements (figure 3-9).

After separation into individual circuits, the die may be mounted on a ceramic wafer, and then to a suitable header by means of a high temperature eutectic solder. Wires only 0.001 in diameter are bonded from the circuit to the proper package leads. This completes the fabrication of a monolithic epitaxial-diffused integrated circuit.

3.4 RESISTORS:

As shown in figure 3-9, a resistor has been fabricated along with an npn transistor. The process consists of diffusing a narrow strip of p-type material into the n-type region.

The basic equation for resistance of a uniform length of material, figure 3-10, is as follows:

$$R = \frac{\rho \ell}{A} = \frac{\rho \ell}{tW} \tag{3.1}$$

where R = resistance

ρ = resistivity of the material

ℓ = length

A = cross-sectional area

t = thickness of material

W = width of material.

In the case of uniformly doped silicon material,

$$\rho = \frac{1}{g\mu N} \tag{3.2}$$

where μ = mobility

g = electron charge

N = net density of impurity atoms.

The hole mobility and the electron mobility in silicon vary with temperature causing a relatively high temperature coefficient of diffused resistors.

Referring again to figure 3-9(a), it can be seen that when a p-type diffusion is made into the n-type region, a p-n junction is also formed. For the resistor to function properly, the n-type region must be connected to a potential that is always higher or equal to the higher voltage connection of the resistor. In the case of the circuit connection of figure 3-9(a), both the resistor and the transistor could have been placed in the same island since the junction formed at the resistor is reversed biased by means of the higher collector potential. For temperatures above 25°C, it is sufficiently accurate to assume that resistance increases by 0.09%/°C.

3.5 PNP TRANSISTORS:

Thus far, only npn transistors have been shown fabricated. The fabrication of pnp transistors is somewhat more difficult, requiring an extra diffusion process. One technique to overcome this problem is to use a lateral type PNP transistor action in series with a npn transistor. This configuration is shown in figure 3-11. The pnp unit is designed with a base width of 3/8 mil, because of the resultant low βeta, the unit is connected to a standard NPN transistor. If the lateral pnp transistor has a beta of about unity, then the beta of the overall unit is given by:

$$\beta = \beta_{LAT\ PNP}\,(1 + \beta_{NPN}) \qquad (3.3)$$

$$\simeq \beta_{NPN}\,.$$

3.6 ZENER DIODES:

Zener diodes can be obtained by the voltage breakdown of a reversed biased p-n junction. To get an effective low-voltage zener diode, a transistor can be used with the collector to base diode shorted and using the emitter-base diode. A lower voltage zener diode can be fabricated by increasing the doping level of the base (using the isolation diffusion impurity concentration instead of the normal base diffusion).

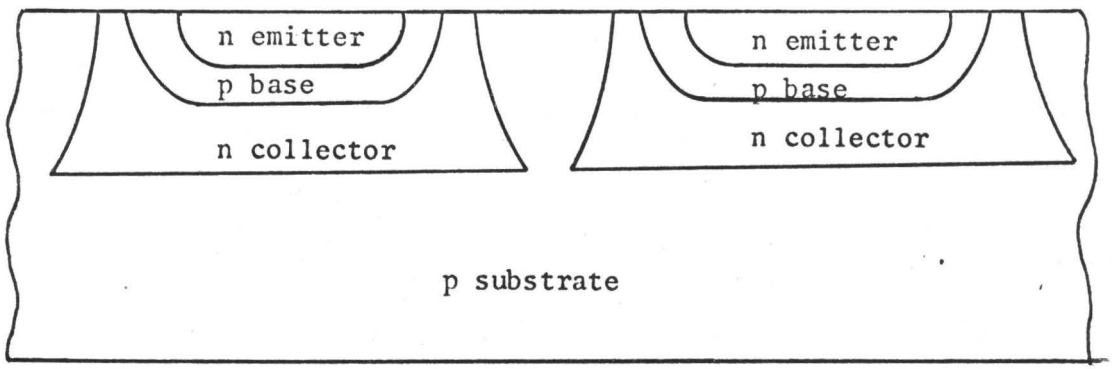


FIGURE 3-1: Cross Section of Monolithic npn Transistors

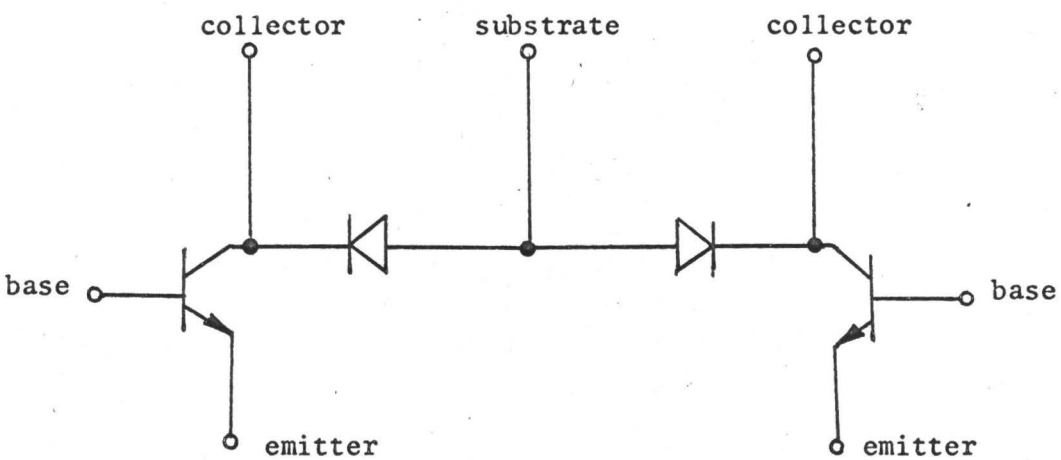


FIGURE 3-2: Equivalent Circuit of Two Isolated Transistors

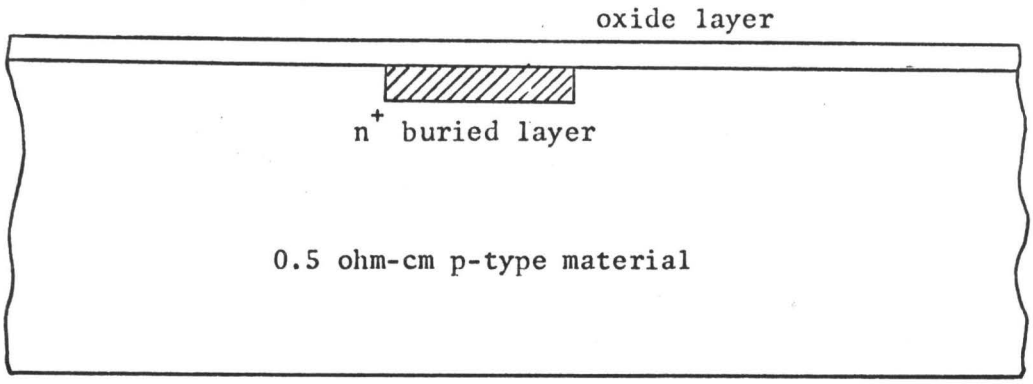


FIGURE 3-3: Cross Section of Buried Layer Diffusion

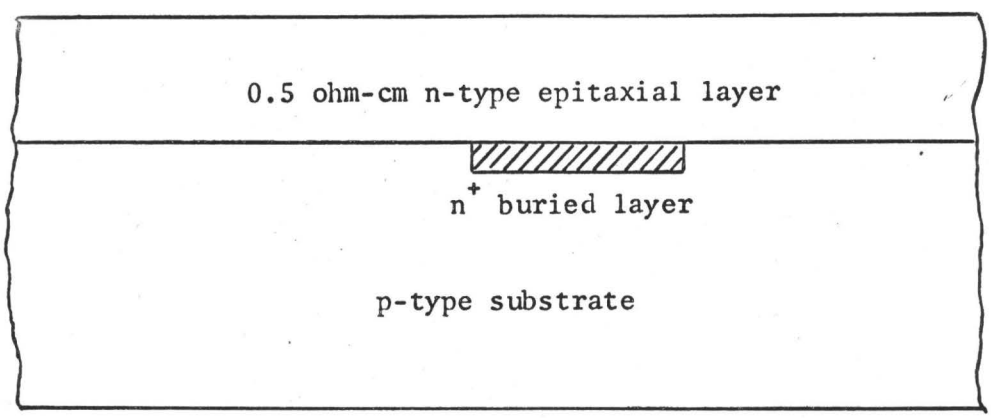


FIGURE 3-4: Cross Section of Epitaxial Layer

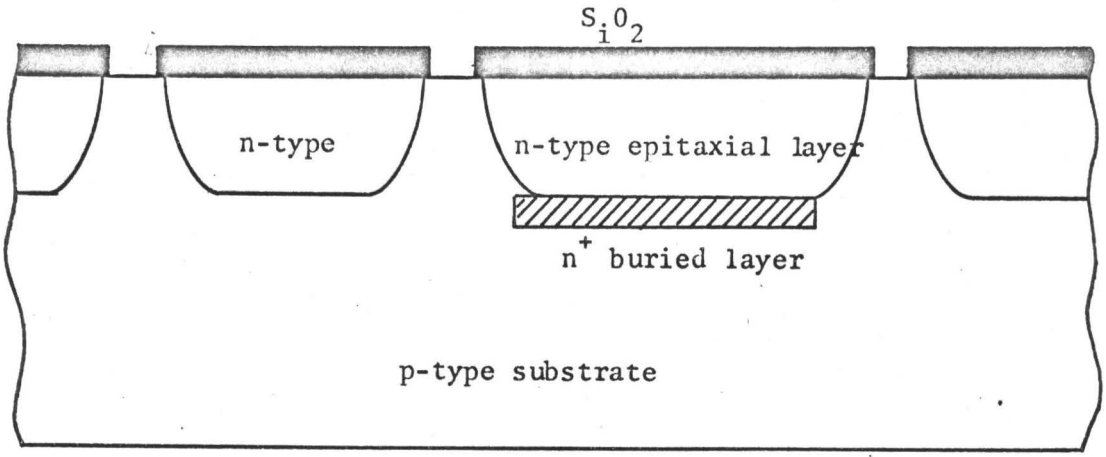


FIGURE 3-5: Cross Section of Isolation Diffusion

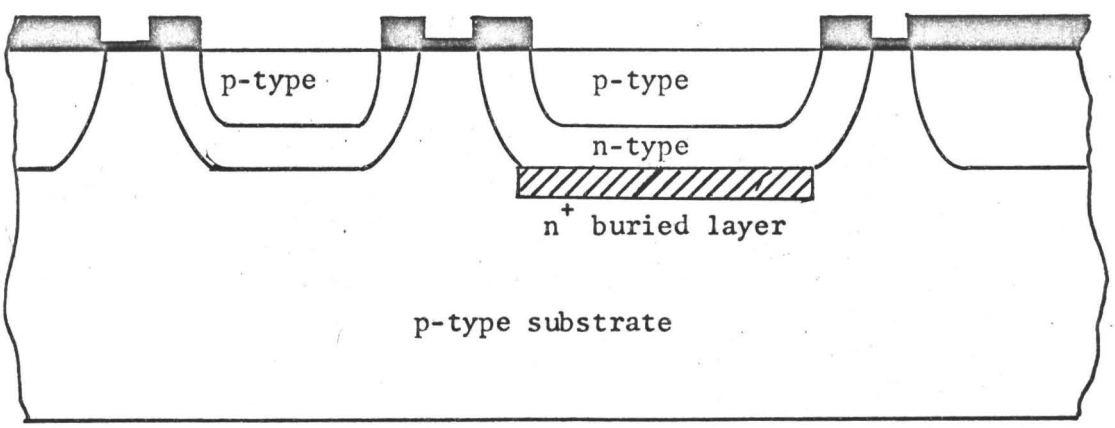


FIGURE 3-6: Cross Section of Base Diffusion

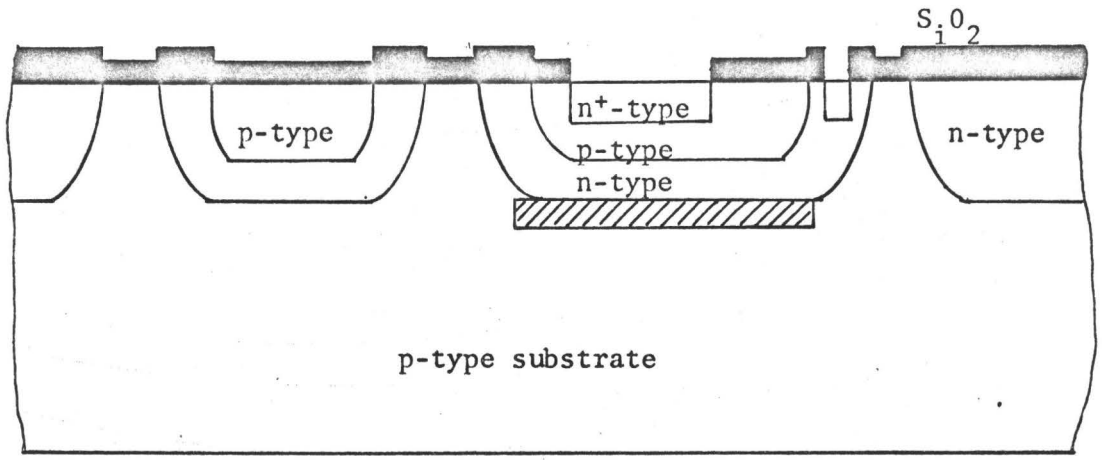


FIGURE 3-7: Cross Section of Emitter Diffusion

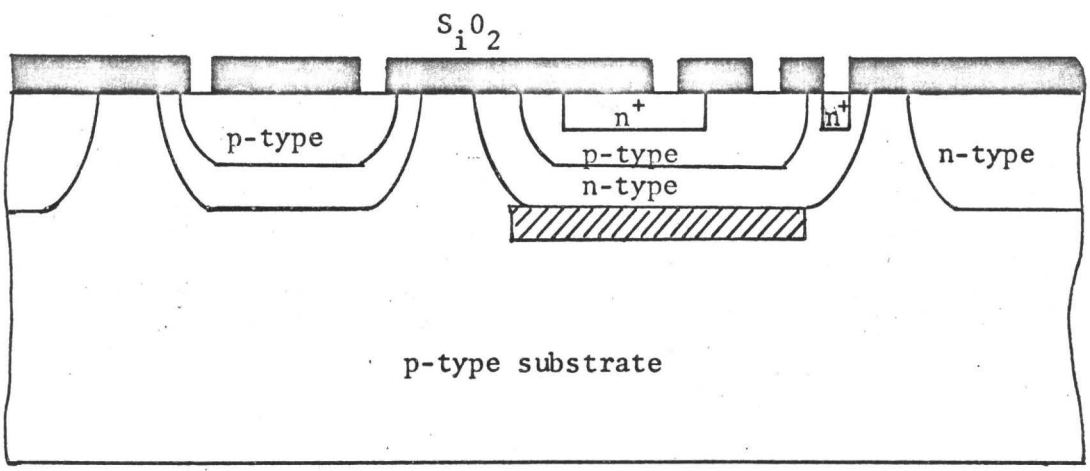


FIGURE 3-8: Cross Section of Openings for Metalization

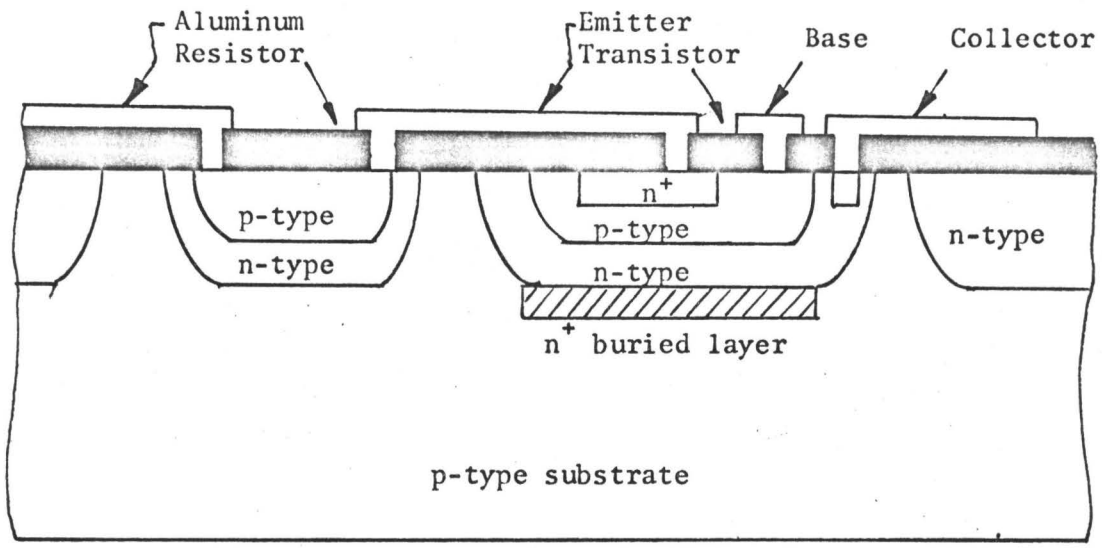


FIGURE 3-9(a): Cross Section of Aluminum Pattern

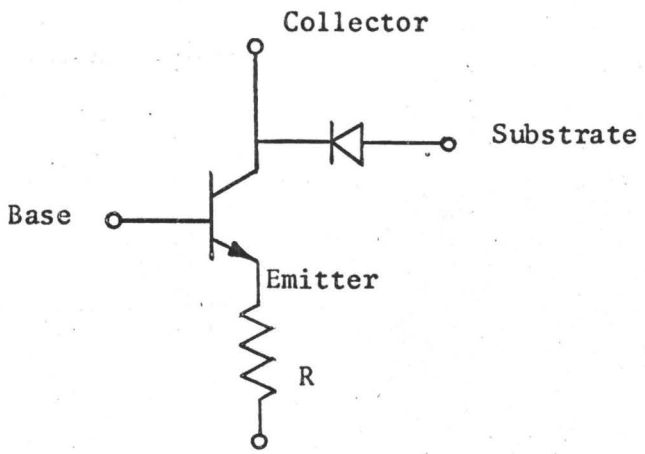


FIGURE 3-9(b): Equivalent Circuit

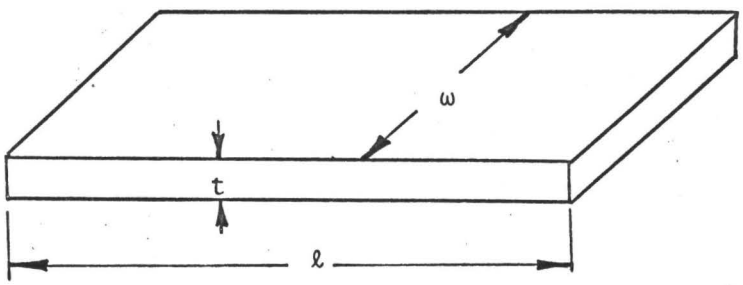


FIGURE 3-10: Equivalent Resistance of Diffused Resistor

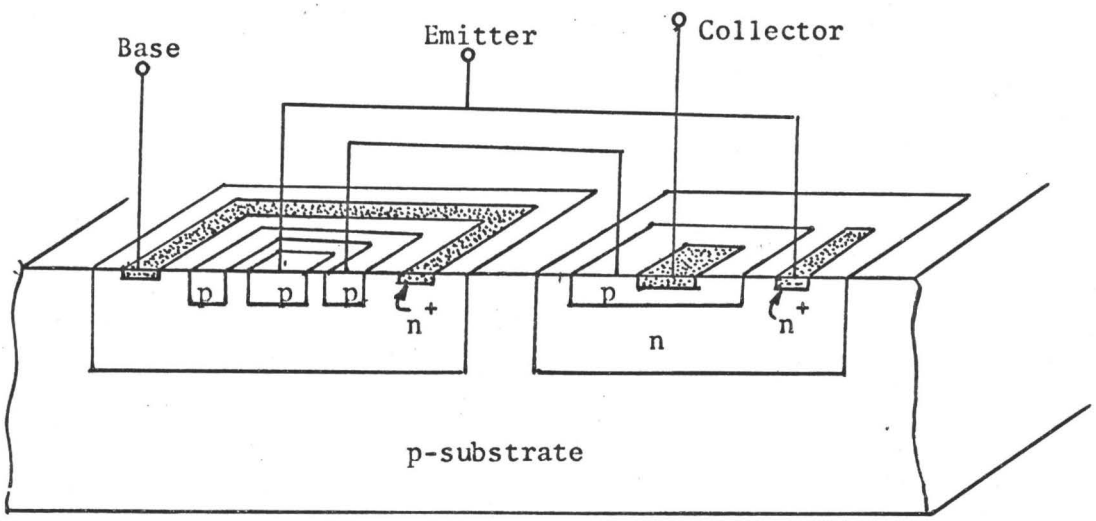


FIGURE 3-11(a): Cross Section of NPN-PNP Transistors

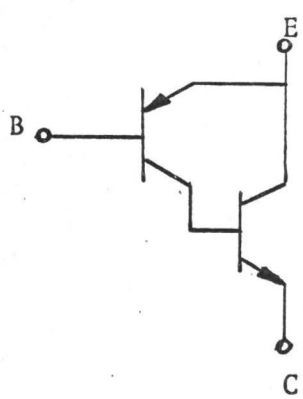


FIGURE 3-11(b): Equivalent Circuit of PNP Transistor

CHAPTER IV

INTEGRATED GYRATOR FABRICATION

4.1 INTRODUCTION:

In integrated circuit form, the small size and amount of material necessary to perform most electronic functions permits the fabrication of large numbers of units simultaneously. To achieve these ends, it is necessary to perform the various fabrication processes in minute selected areas over the entire wafer while the balance of the area is unaffected. Thus in order to realize a gyrator in integrated form, a series of masks are required to implement the complete processing schedule.

4.2 GENERAL FABRICATION PROCEDURE:

The production of a set of precision microphotographic masks is an essential part of the integrated circuit development. Practical mask making as presently performed involves 5 major steps:

1. Mask design and layout.
2. Artwork.
3. First reduction.
4. Second reduction (producing multiple patterns).
5. Copymaking.

The gyrator circuit function is converted into a pattern of active, passive, isolation and interconnecting regions which will realize the circuit. A separate dimensioned layout or scale drawing is made for each

mask. At least one individual mask is required for each major step in the fabrication of the monolithic circuit. A typical series of masks for NPN active devices on a P-type substrate would realize the circuit as follows;

1. Pre-epitaxial growth, i.e., the placing of an N^+ buried diffusion layer to reduce collector series resistance.
2. Isolation diffusion, i.e., creating separate N regions in the epitaxial layer for transistors, diodes and resistors.
3. Base diffusion, i.e., forming the base regions of transistors, diodes and resistor areas.
4. Emitter diffusion, i.e., placing the transistor's emitter, low resistance crossovers (where needed), and low resistivity terminal areas on N collector regions.
5. Pre-ohmic, i.e., making holes through the surface oxide to allow the metalization so as to make contact with terminal areas of circuit elements.
6. Metalization, i.e., establishing the metal interconnection pattern to "wire" the circuit and provide pads or areas to which external connections can be made.

The first of these masks, the mask for the location of the buried layer was not produced, since the silicon wafer which was used for the fabrication of the integrared gyrator was already available. The wafer which was being used for the Westinghouse 1709 operational amplifier, had a series of buried layer patterns which could readily be used for the layout of the gyrator circuit. For this reason, of the normal six masks, only five were actually made.

The scale drawings were drawn 250 times the actual size on paper which was both temperature and moisture stable. These scale drawings were 14.75 inches by 14.75 yielding a final mask size of 59 mils by 59 mils. A typical mask is shown in figure 4-1 which is a copy of the final mask. The black areas are produced by laying strips of black adhesive tape on the clear transparent paper. The original scale drawing is reduced in two steps with the first one being a 5 times reduction. This result is then reduced 50 times and at the same time a multiple array is produced by the "step and repeat" process.

Once the production of the masks is complete, it is now possible to produce the gyrator circuit layout on the silicon wafer. The patterns on the glass masks produced are transferred to the silicon wafer via a very thin uniform photosensitive film called photoresist which is placed on the surface of the wafer. The glass mask with its dark and transparent regions in close contact with the coated wafer permits exposure and polymerization of only the unprotected areas of the film. The unexposed portion is removed and an etchant removes only the exposed silicon dioxide. The etchant must not attack the silicon, the photoresist or the silicon dioxide protected by the photoresist. This etching leaves windows or holes through the silicon dioxide that permits diffusion to be effective only in selected areas.

The individual steps in the process are:

1. The wafer is placed horizontally on a mandrel and held in place by a vacuum. Deposition of an excess of photoresist KPR material is placed on the wafer. The photoresist is a diluted solution mixed in a 1:1 ratio with KPR solvents to permit easy flow.

2. The wafer is spun at 4000 RPM for 60 seconds throwing off the excess photoresist and giving the wafer a uniform coating. The thickness of the photoresist coating is controlled by the speed rotation as well as the viscosity of the KPR, the temperature and the speed.
3. The coating is dried and hardened by permitting the solvents to evaporate at a temperature of 80° - 90°C for ten minutes. This also helps to assure uniform emulsion density.
4. The photoresist coated wafer is carefully aligned with the patterned mask to assure that the light and dark areas of the mask are properly located. This is usually done under a high power split image (ballistic) microscope, having X, Y, and θ motions that permit very accurate movement of one with respect to the other. Each mask has an identifying cross or dot which is aligned with the one on the previous diffusion process. The first mask used has a cross placed at the corner of each individual circuit which is aligned with a slaightly larger cross on the wafer with the epitaxial layer on it. The mask also has a dot which is 4 mils in diameter. All subsequent masks have dots in the same relative position with the dot of each successive mask having a dot a half mil smaller than the previous one.
5. The photoresist film is exposed for 60 seconds by collimated blue light with a heavy content of ultra-violet. This causes polymerization of the exposed areas of the film. The photolithographic area where this process is performed is lighted with yellow light to which the photoresist materials are insensitive.
6. A KPR developer is used which both hardens the exposed film areas while washing away the unexposed regions. This is carried out for a

period of 30 seconds after which the wafer is rinsed with isopropyl alchohol and rinsed with de-ionized distilled water.

7. The developed photoresist is hardened further by baking the wafer at a moderately elevated temperature (between 120°C and 130°C) for a period of 15 minutes.
8. The oxide coating is etched away from the areas of the wafer not protected by the photoresist material. A mixture of NH_4F-H_2O-HF is used. The wafer is repeatedly taken out of the etchant to see when the etchant has gone all the way through the silicon dioxide layer to the silicon and no further. After the silicon dioxide layer has been removed, the photoresist film is also completely removed. It is accomplished by heating the wafer in a solution of sulphuric acid and hydrogen peroxide until white fumes are given off.

The photoresist and etching sequence is repeated many times in the processing of a silicon integrated circuit. This process finds application in the control of diffusion, as well as metalization with a negative photoresist being used for the metalization etch. All the previous photoresist processes were the positive type (i.e., the silicon dioxide of the unexposed areas were etched away, while the aluminum of the exposed area was etched away). Thus, the photoresist etching sequence is employed at each of the following steps:

(a) Prior to isolation diffusion.

(b) Prior to base diffusion.

(c) Prior to emitter diffusion.

(d) Prior to pre-ohmic etching.

(e) After metalization.

4.3 GYRATOR LAYOUT DESIGN:

From figure 2-10 it can be seen that the circuit which is to be fabricated has a total of 10 transistors; 8 npn and 2 pnp low beta. Three of the npn transistors, Q_1, Q_6, and Q_7 have a common collector potential while transistors Q_2 and Q_4 also have a common collector potential. All the other transistors have varying collector potentials relative to each other. Since the collector of an npn transistor and the base of a pnp transistor have the potential of the region in which the transistor is located, there are a minimum of 7 isolated regions required. The layout of the N^+ type buried layers of the Westinghouse 1709 wafer is that shown by figure 4-1. Each buried layer can be surrounded by an isolation diffusion and thus up to 10 isolated regions can be obtained. For convenience, however, the number of isolated regions decided upon was 8 as can be seen in figure 4-2 which is the mask for the isolation diffusion. The cross mark in the lower left hand corner of the mask is used to line up the mask with the cross shown on figure 4-1. This alignment will assure that the isolation diffusion will take place between the buried layers.

The diffused areas inside the largest isolated region in the lower right hand side of the isolation mask are the anodes of the two zener diodes. The isolation diffusion impurity is used here instead of the regular p-type base diffusion impurity so that the zener diode has a lower breakdown voltage. The two zener diodes formed in this region will remain floating and will form diodes D_1 and D_4 in figure 2-10. Diodes D_2 and D_3 are formed by two diffused areas on the isolation strip. The large diffused area in the upper left hand corner is an area to

which the negative supply is connected keeping the entire substrate at the negative potential.

Figure 4-3 shows the mask used for the base diffusion. The low beta lateral pnp transistors Q_3 and Q_{10} can readily be seen in the centre of the mask. They can be identified by their geometry. The emitter is located inside the collector area. The resistors can also be seen diffused during this process. The narrow width resistors are 3/8 mil in width and have a resistance of approximately 900 ohms per mil length. The remaining resistors have a width of 1 mil with the resistance being approximately 250 ohms per mil length. In the lower left hand corner of a mask, a resistor is fabricated having two tapped connections. This resistor along with the resistor located right center on the mask give resistors R_2 and R_7 on figure 2-10. These resistors can thus attain several values depending on which terminal the bond is fastened on to. By having the choice of adjustable resistance, the gyrator can operate at supply voltages of $\pm$ 8 volts to $\pm$ 16 volts. At the upper left hand corner a diffusion is made into the p-type isolation region. This serves to keep the silicon dioxide layer at a low thickness and, at the same time, lower the resistance to the substrate. The remaining diffused regions consist of the p-type base regions of the npn transistors.

Figure 4-4 shows the n-type emitter diffusion mask. The overall size of the monolithic chip is indicated by the heavy outline. Measurements show that the diagram shown by figure 4-4 is approximately 100 times the actual physical size of the chip.

The purpose of the border is to maintain the oxide layer at a minimum since silicon dioxide is extremely hard making it difficult for

the wafer to be cut evenly. The wafer also breaks easier in areas where there is a heavy concentration of impurities.

The diffused areas inside the border consist of emitters that are formed in the base region completing the npn transistor structure. The zener diodes are also completed at this point with the n^+-type impurity being diffused into the high p-type isolation diffusion impurity resulting in a low zener breakdown voltage of 5.8 volts.

The remaining n^+-type diffusions are made into the n-type collector regions to give low resistivity contact regions as well as preventing the formation of a p-n junction with the aluminum.

The pre-ohmic contact mask is shown by figure 4-5. After the emitter diffusion, an oxide layer is grown over the entire wafer which then has holes opened in the areas indicated by the mask of figure 4-5, leaving the remaining suraface protected with an oxide layer.

As in the emitter mask, the oxide at the border has been etched away making it easier to break the wafer along the edges of the dice. The square area in the upper left hand corner is the area to which electrical contact will be made to the substrate. The remaining holes are for contacts to the various components that have been fabricated on the chip.

The metalization mask is shown by figure 4-6 which indicates the connections between components on the substrate as well as pads to which gold or aluminum wire can be bonded making contact with the pins on the header.

The five masks shown by figures 4-2 to 4-6 were all required to fabricate the gyrator circuit. However, there was an additional mask made to allow for the testing of individual components on the die.

This mask is shown of figure 4-7. This pattern was placed at each corner of the metalization mask so that the components at each corner of the wafer could be checked. The test pads of figure 4-7 are located in such a manner so that with the exception of a few npn transistors, all the components can be individually tested. Thus, if the overall circuit does not work, the fault can be traced and corrected without disturbing the remainder of the layout.

The sets of masks shown in figures 4-2 to 4-6 were the result of a second fabrication attempt. For this second set of masks, the components were found to have the following values:

(a) npn transistors at V_{CE} = 10 volts, I_C = 1.0mA.

h_{ie} = 1000 ohms

h_{fe} = 40

h_{re} = 8.0×10^{-4}

h_{oe} = 3.4×10^{-6} mho

(b) npn-pnp transistor at V_{CE} = 10 volts, I_C = 1.0 mA.

h_{ib} = 18.5 ohms

h_{fb} = -0.975

h_{rb} = 5.0×10^{-5}

h_{ob} = 0.85×10^{-6} mho

(c) Zener Diodes breakdown voltage

5.85 volts

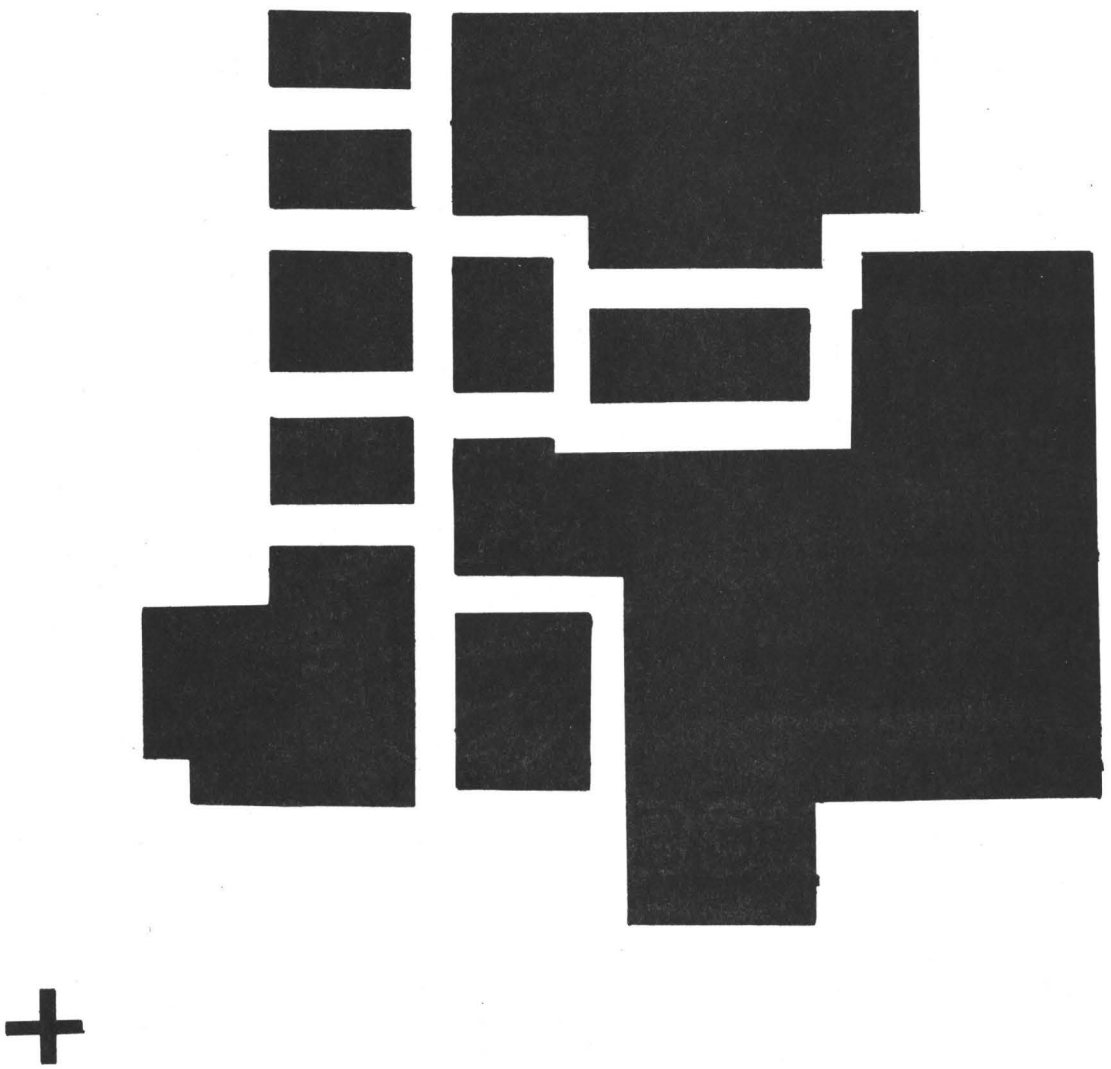


FIGURE 4-1: Buried Layer Pattern

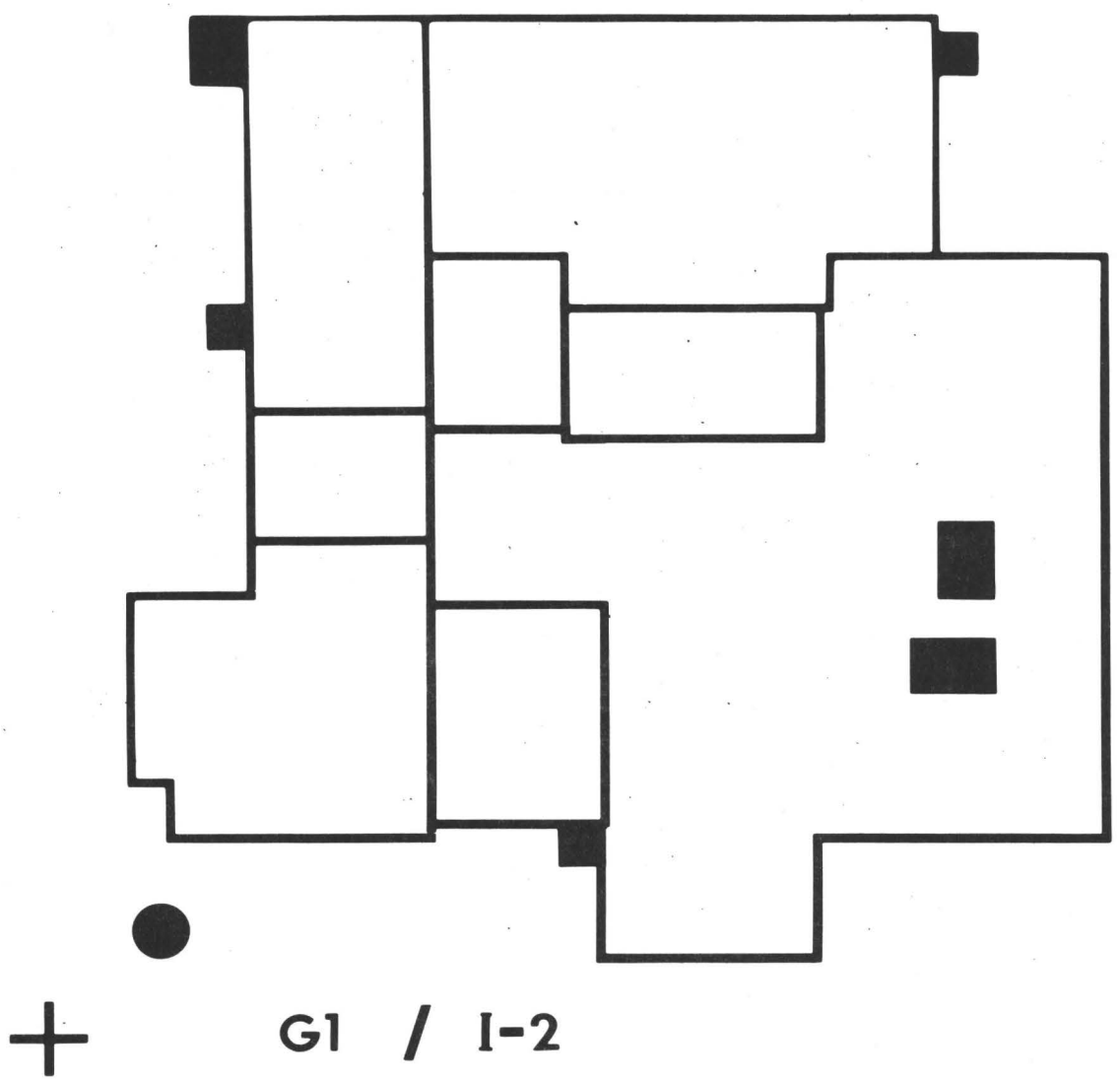


FIGURE 4-2: Isolation Diffusion Pattern

FIGURE 4-3: Base Diffusion Pattern

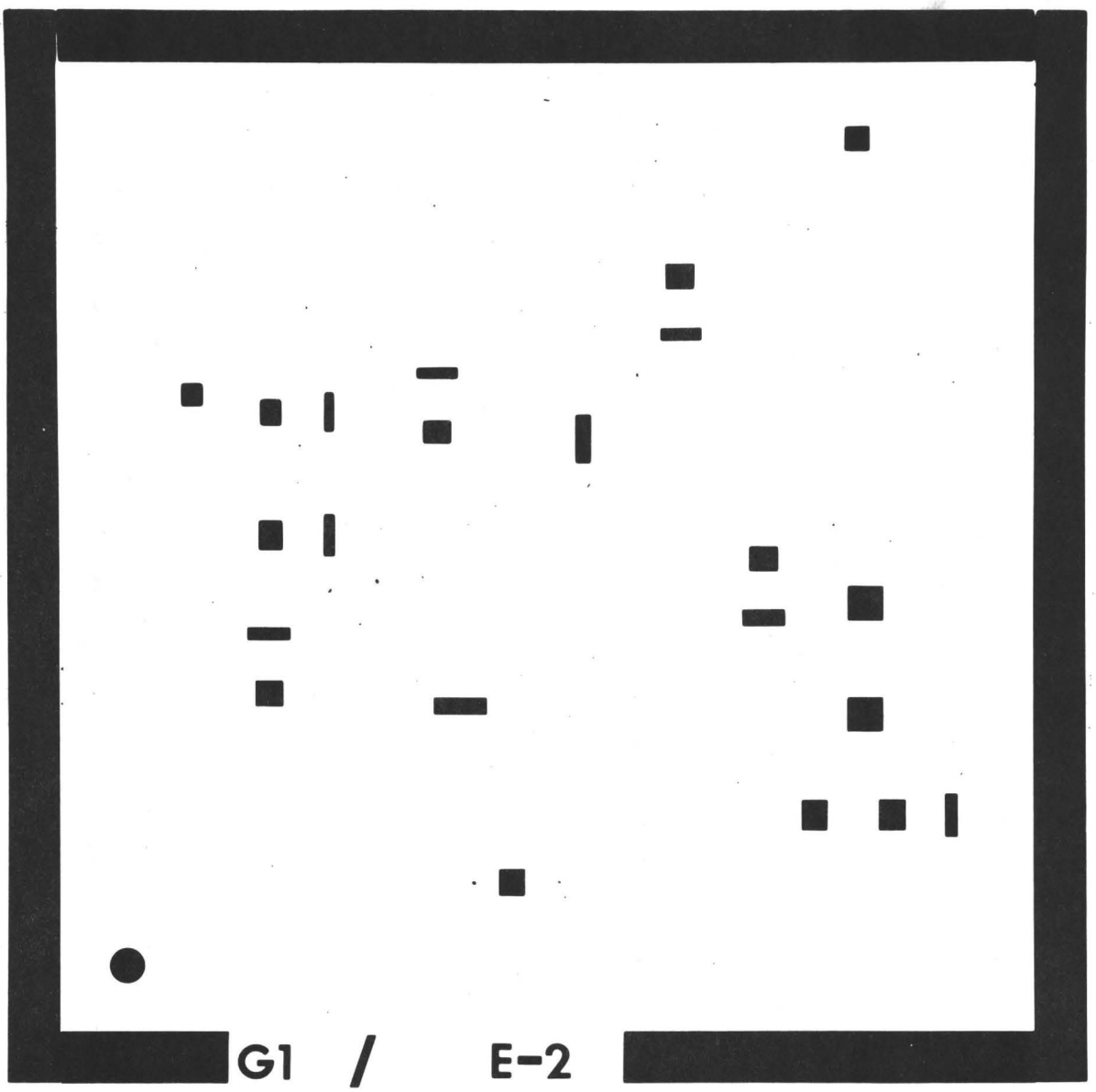


FIGURE 4-4: Emitter Diffusion Pattern

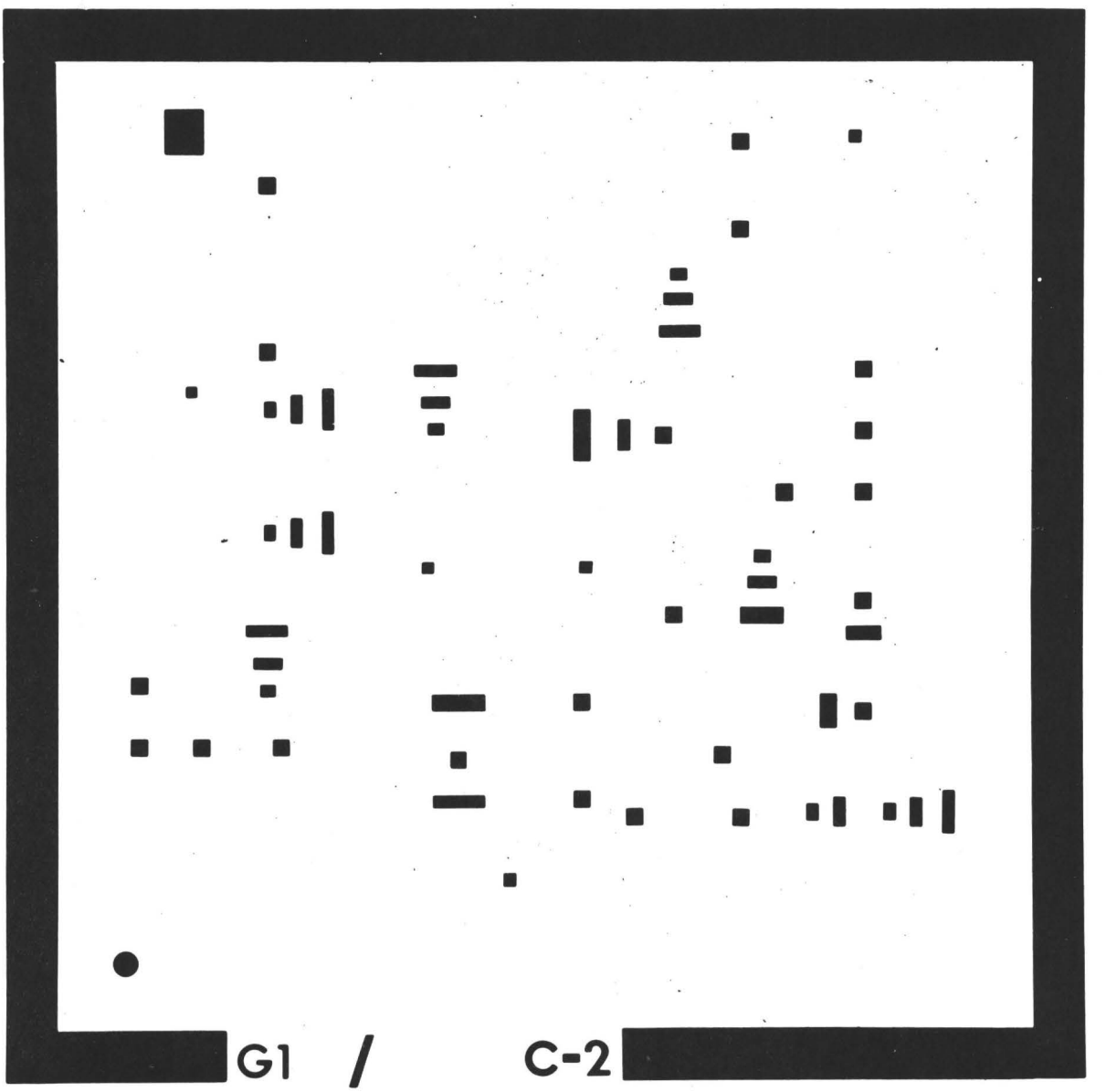


FIGURE 4-5: Contact Pattern

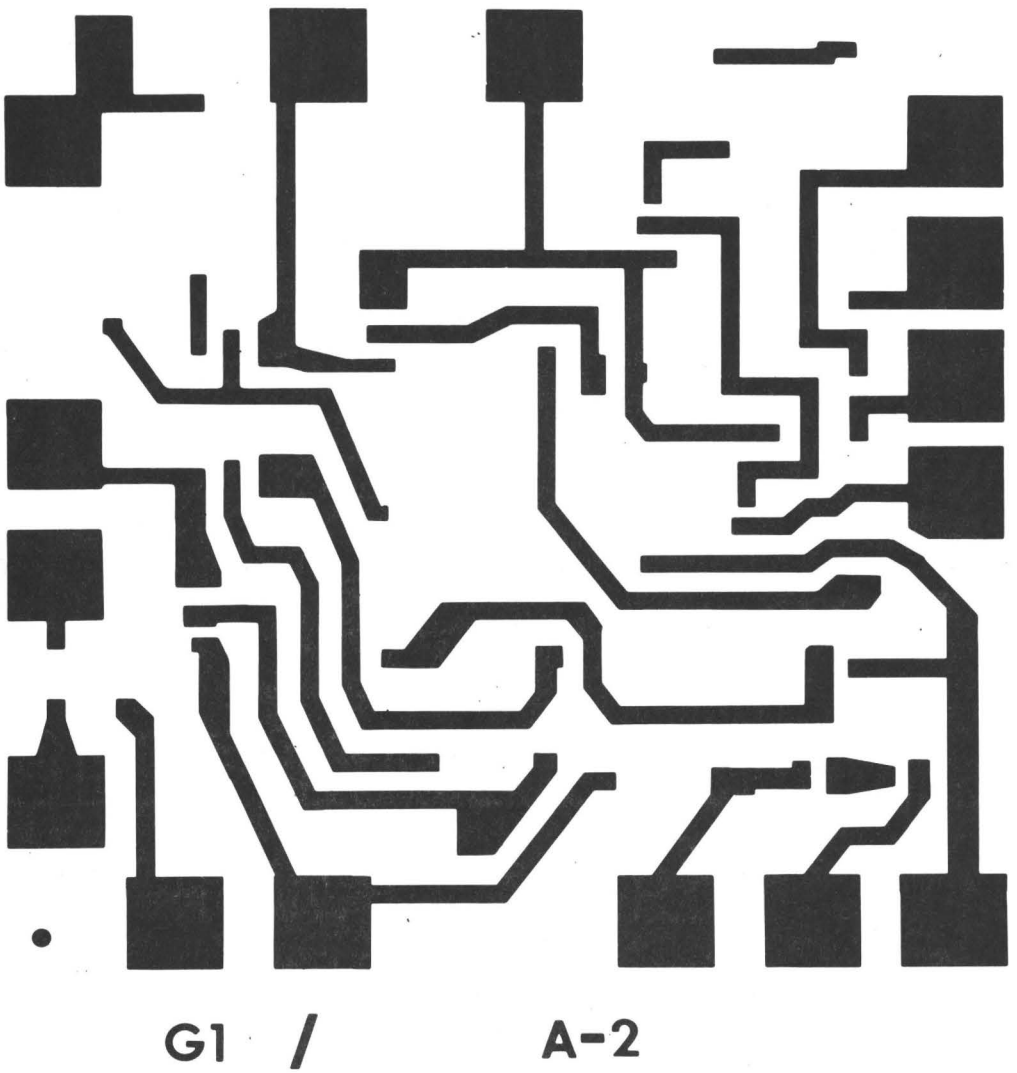


FIGURE 4-6: Metalization Pattern

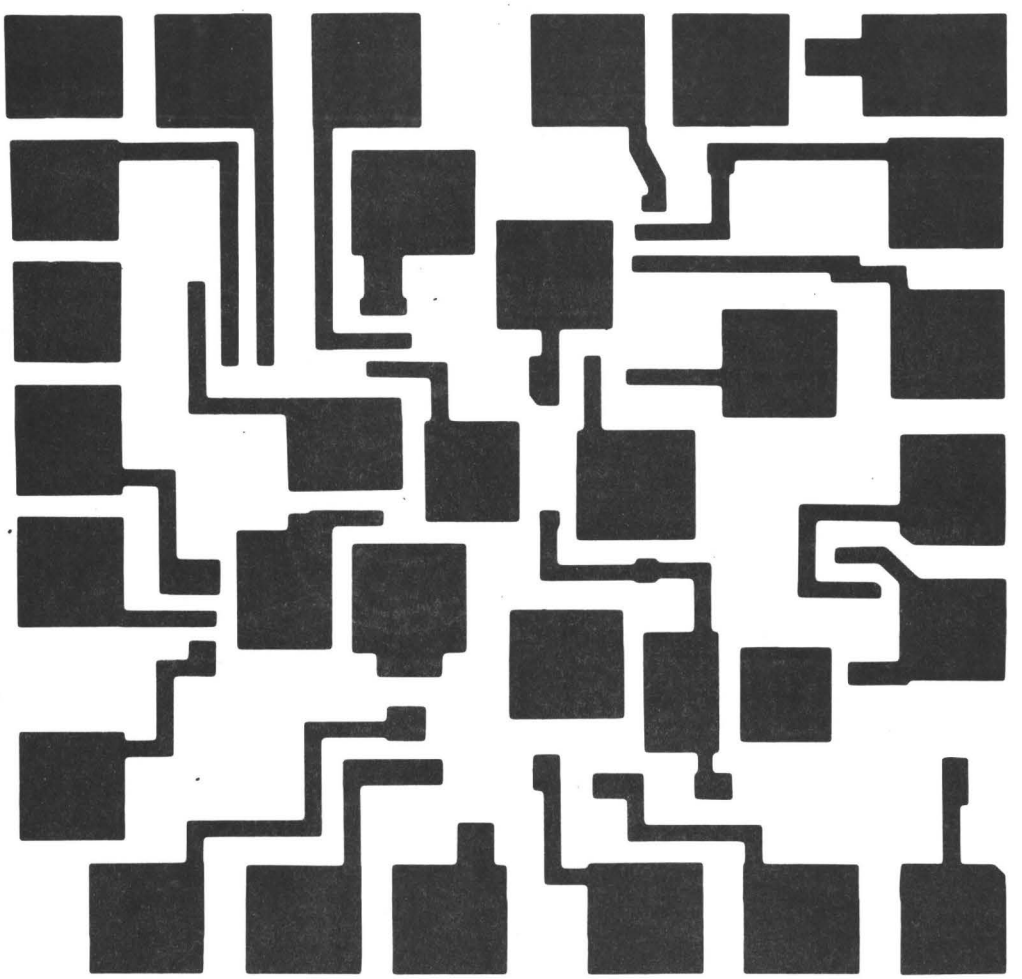


FIGURE 4-7: Component Test Pattern

CHAPTER V

EXPERIMENTAL RESULTS

5.1 INTRODUCTION:

The experimental results presented in this chapter are specifically related to the properties of an inductor, since it is the ability to simulate an inductor that gives the gyrator its most useful property. The parameters of the gyrator are given, followed by a series of graphs which give the quality of the simulated inductor at various frequencies and temperatures.

5.2 EXPERIMENTAL GYRATOR PARAMETERS:

The short circuit driving-point admittances of the gyrator which was fabricated, were obtained by shorting the output of one port to ground and measuring the input impedance of the other port. The transconductances were obtained by measuring the short circuit output current as well as the input voltage. The results obtained are shown in Table 5-1.

Temperature	y_{11}	y_{22}	y_{21}	y_{12}
-25°C	3.3×10^{-6} mho	3.2×10^{-6} mho	-1.02×10^{-3} mho	1.01×10^{-3} mho
25°C	3.0×10^{-6} mho	2.9×10^{-6} mho	-0.96×10^{-3} mho	0.95×10^{-3} mho
75°C	2.75×10^{-6} mho	2.6×10^{-6} mho	-0.90×10^{-3} mho	0.88×10^{-3} mho

TABLE 5-1

This table shows that the transconductances of the gyrator as well as the input and output driving-point admittances vary considerably with

temperature. For room temperature, the values agree closely with the calculated paramters evaluated in Appendix I which are:

$$[Y] = \begin{vmatrix} 3.1 \times 10^{-6} & 0.98 \times 10^{-3} \\ -0.97 \times 10^{-3} & 3.1 \times 10^{-6} \end{vmatrix} \qquad (5.1)$$

While the calculated values of y_{21} and y_{12} are very close in magnitude, the experimentally observed values are different by 2%, thus making the fabricated gyrator slightly active in one direction.

The input impedance expression of the gyrator at room temperature is:

$$Z_{IN} = \frac{1.10 \times 10^{6}}{Z_L} \text{ ohms} \qquad (5.2)$$

where Z_L is the terminating impedance at the output port. At -25°C the expression is

$$Z_{IN} = \frac{0.94 \times 10^{+6}}{Z_L} \text{ ohms} \qquad (5.3)$$

and at 75°C,

$$Z_{IN} = \frac{1.26 \times 10^{+6}}{Z_L} \text{ ohms} \qquad (5.4)$$

Experimental input impedance versus terminating load resistance was plotted at room temperature as well as at -25°C and 75°C. The results are shown in figure 5-1. The graph shows that the expression is very linear for load resistances of 10 ohms to 100,000 ohms. For load resistances below 10 ohms and above 100,000 ohms, the relation becomes non-linear due to the effect of finite input and output admittances of the gyrator. Thus when the load resistance is made zero, the input impedance does not become infinite but becomes equal to the reciprocal

of y_{11} of the Y matrix, and when the load resistance is made infinite, the input impedance becomes equal to $y_{22}/(y_{11}\ y_{22} - y_{12}\ y_{21})$.

Figure 5-2 is the graph showing the relationship between the inductance obtained at one port versus the terminating capacitance at the other port. Again, it can be seen that the relation is linear in the region where the capacitance varies from 1×10^{-10} farads to 1×10^{-6} farads. The expression for this set of lines is;

$$Z_{IN} = j\omega\ 1.10 \times 10^{6}C \text{ at } 25°C$$
$$= j\omega\ 0.94 \times 10^{6}C \text{ at } -25°C$$
$$= j\omega\ 1.26 \times 10^{6}C \text{ at } 75°C$$

where the equivalent inductance is

$$L = 1.10 \times 10^{6}C \text{ at room temperature.}$$

5.3 QUALITY OF SIMULATED INDUCTORS:

To test the quality of the inductor obtained by terminating one port of the gyrator with a capacitor, a parallel LC circuit is set up by terminating the remaining port of the gyrator with another capacitor. If both capacitors are of high quality with low losses, any resulting loss will be due to the gyrator only. Figure 5-3 shows the quality of the simulated indictor at various frequencies obtained by varying the capacitance at the input port while keeping the capacitance at the output port constant. Figure 5-3 shows the Q factor of the gyrator when the terminating capacitances at the output port are 0.1×10^{-6} farads and 0.04×10^{-6} farads. It can be seen that the Q factor has a maximum value occuring at a certain frequency depending upon the terminating capacitance and decreasing at a constant rate predicted by

equation 1.27 in Chapter I. If $y_{11}\, y_{22} << y_{12}\, y_{21}$, and $y_{12} = y_{21}$, $y_{11} = y_{22}$, then

$$Q_{MAX} = \frac{y_{21}}{2y_{11}} \tag{5.5}$$

This expression shows that the maximum Q factor obtainable at low frequencies for this gyrator is 158 which is 50% higher than the observed maximum Q factor obtained in figure 5-3.

It was observed that when a signal was applied to only one of the two amplifiers, an signal was observed at the output terminals of both amplifiers. This was observed even though the unused amplifier had its input terminal connected to ground. The signal at the output terminal of the unused amplifier had a voltage output of approximately one half the output of the amplifier which had a signal applied to it. The signal at the output of the unused amplifier varied from sample to sample. When the connections to the amplifiers were reversed, the voltage at the output of the unused amplifier was again half the voltage at the output of the amplifier which had a signal applied to it. In both instances it was observed that the output signals of the amplifiers were 180° out of phase with respect to each other. From these observations it was concluded that the two amplifier were not perfectly isolated from one another and thus altered the parameters measured when the amplifiers were taken as isolated units. The admittance parameters were altered in such a way lowering the performance of the gyrator resulting in a lower maximum Q factor.

When the gyrator was terminated with lower values of capacitance, the frequency at which the maximum Q occurs increased. The maximum Q

factor also increased as the terminating capacitance decreased as is shown in figure 5-4.

From the theory derived in Chapter I, it is seen that the maximum Q factor occurs at

$$f_{max} = \frac{y_{12}}{2\pi C} \tag{5.6}$$

which assumes that $y_{12} = y_{21}$ and $y_{22} = y_{11}$. From this expression it can be shown that when the terminating capacitance is 0.01×10^{-6} farads, the frequency at which the maximum Q factor should occur is 1.64×10^{4} Hz which is indeed the frequency observed in figure 5-4.

The transconductances given in equation 5.1 were measured at 1000 Hz. which is low enough so that capacitance effects can be neglected. When the transconductance was measured at higher frequencies, it was found that the transconductance decreased with frequency. The transconductance of both amplifiers decreased to 0.707 of their low frequency values at a frequency of 8.5×10^{5} Hz. As shown in figure 5-4 the Q factor becomes larger with increasing frequency. With decreasing capacitance, larger Q factors result until the Q factor approaches infinity when the gyrator is self-oscillating. To avoid these high frequency effects, the technique developed in Chapter I was used to stabilize the gyrator by the addition of a resistor at both ports in series with the capacitance. This technique is used to make the gyrator useful at higher frequencies, as shown in figure 5-5. By varying the value of the resistance, it is possible to control the value of the maximum Q factor attainable. The value of the stabilizing resistance is given by τ/C where τ is the time delay from input to output and

C is the terminating capacitance. The curves of figure 5-5 correspond to a fixed capacitance of 0.001μF in series with resistance of 187 ohms, 100 ohms, 50 ohms and 0 ohms. When the resistance is 187 ohms, the shape of the curve is similar to those at lower frequencies with a slightly reduced Q factor. With lower series resistance, the maximum Q increases and the curve does not fall off as rapidly with increasing frequency.

5.4 DEPENDENCE OF INDUCTANCE ON TEMPERATURE:

The results given in table 5-1 show that the parameters of the gyrator vary considerably with temperature. From Appendix I, it can be seen that the short circuit input and output admittance are approximately given by:

$$y_{11}, y_{22} \doteq \frac{2h_{oe}}{1 + h_{fe}} + \frac{1}{(1 + h_{fe})^2 R} \qquad (5.6)$$

By studying the h parameters of transistors having characteristics similar to the transistors fabricated, it was found that the h_{fe} increases considerably more with temperature than h_{oe} or R. Thus at higher temperatures the short circuit admittances decrease and for lower temperatures, increase.

The resistors diffused in the monolithic process have a large temperature coefficient with the positive change in resistance occuring with an increase in temperature. It is thus seen that the transconductance is lower at higher temperatures. To show the temperature effect on the gyrator, all the curves obtained at room temperature were repeated at +75°C and -25°C. The curves in figures 5-1 and 5-2 show the same

linearity but are offset due to the change in value of transconductance.

Figures 5-6 and 5-7 show the effect temperature has on the Q factor of the simulated inductance. There is approximately a 10% difference between the Q factor at 75°C and -25°C. From equation 5.5 it is seen that the Q factor increases when the admittance parameters decrease faster than the transconductance paramters. Thus the maximum Q factor increases with increasing temperatures as shown by figure 5-6.

From the curves in figure 5-8, it is seen that at higher temperatures, the gyrator tends to become unstable at a lower frequency. This shows that the time delay of the amplifiers increases at higher temperatures. The gyrator was compensated by placing a resistance of 250 ohms in series with the capacitance at 75°C and a 125 ohm resistance with the capacitance at -25°C, with the results given in figure 5-8.

As indicated in Chapter I, the inductance simulated by the gyrator is determined by the terminating capacitance and the forward and reverse transconductance, or

$$L = R_1 R_2 C \tag{5.7}$$

Assuming that the capacitance remains constant with temperature, the inductance will vary with the variation in $R_1 R_2$ due to temperature. The simplest way of measuring this change is by noting the change in temperature. At low frequencies the resonant frequency changed 8.8% when the temperature increased from 25°C to 75°C and changed 9.1% when the temperature was decreased from 25°C to -25°C. This is equivalent to a change in inductance of 1760 parts per million/°C above room temperature and 1820 parts per million/°C below room temperature.

5.5 SEPARATE ISOLATED AMPLIFIERS

From equation 5.5 it was calculated that the maximum Q factor obtainable from this device was 158 which was approximately 50% higher than the experimental values obtained, the reason being the close proximity of the two amplifiers with the resulting cross-coupling. Consequently, two separate gyrator samples were taken and a non-inverting amplifier was chosen from one and an inverting amplifier was chosen from the other. The unused amplifier of each device had its input and output terminal grounded to prevent any interference. The amplifiers were connected as before to form a gyrator. The gyrator was again terminated with a capacitor and the Q factor was measured with the results being shown in figure 5-9. The maximum Q factor has increased to approximately 150 with the frequency at which the maximum Q factors occur being the same as the single unit. At higher frequencies the curves obtained for the double unit were identical to the single unit.

5.6 VARIATION IN POWER SUPPLY:

The gyrator in figure 2-10 was designed to operate at supply voltages of $\pm$ 15 volts. When the supply was varied between $\pm$ 13 volts to $\pm$ 16 volts, the performance of the gyrator was not effected. Resistors R_2 and R_8 were increased by changing the connections on the metalization pattern. This enabled the gyrator to be operated with voltage supplies as low as $\pm$ 10 volts.

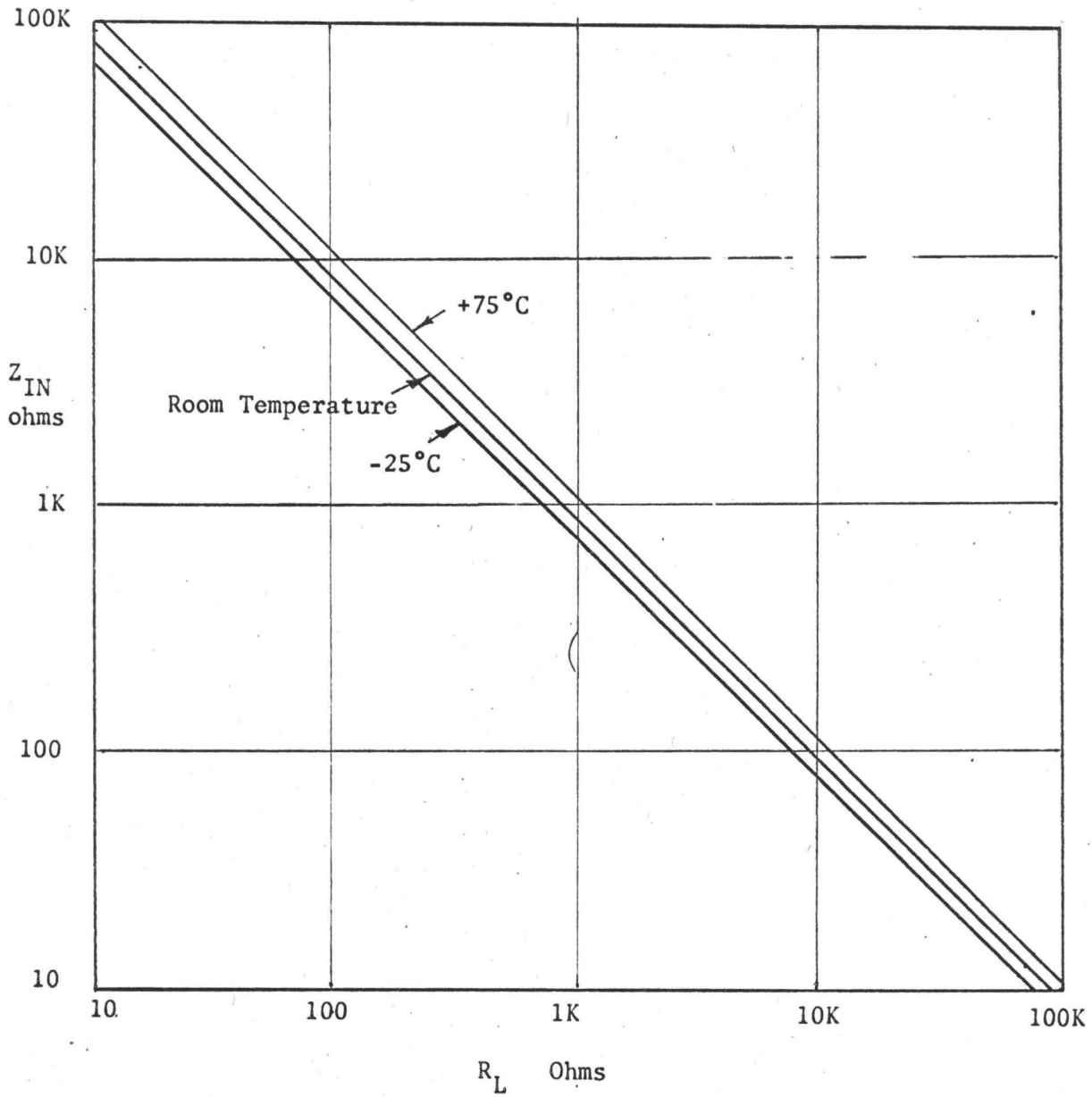


FIGURE 5-1: Input Impedance of Resistive Terminated Gyrator

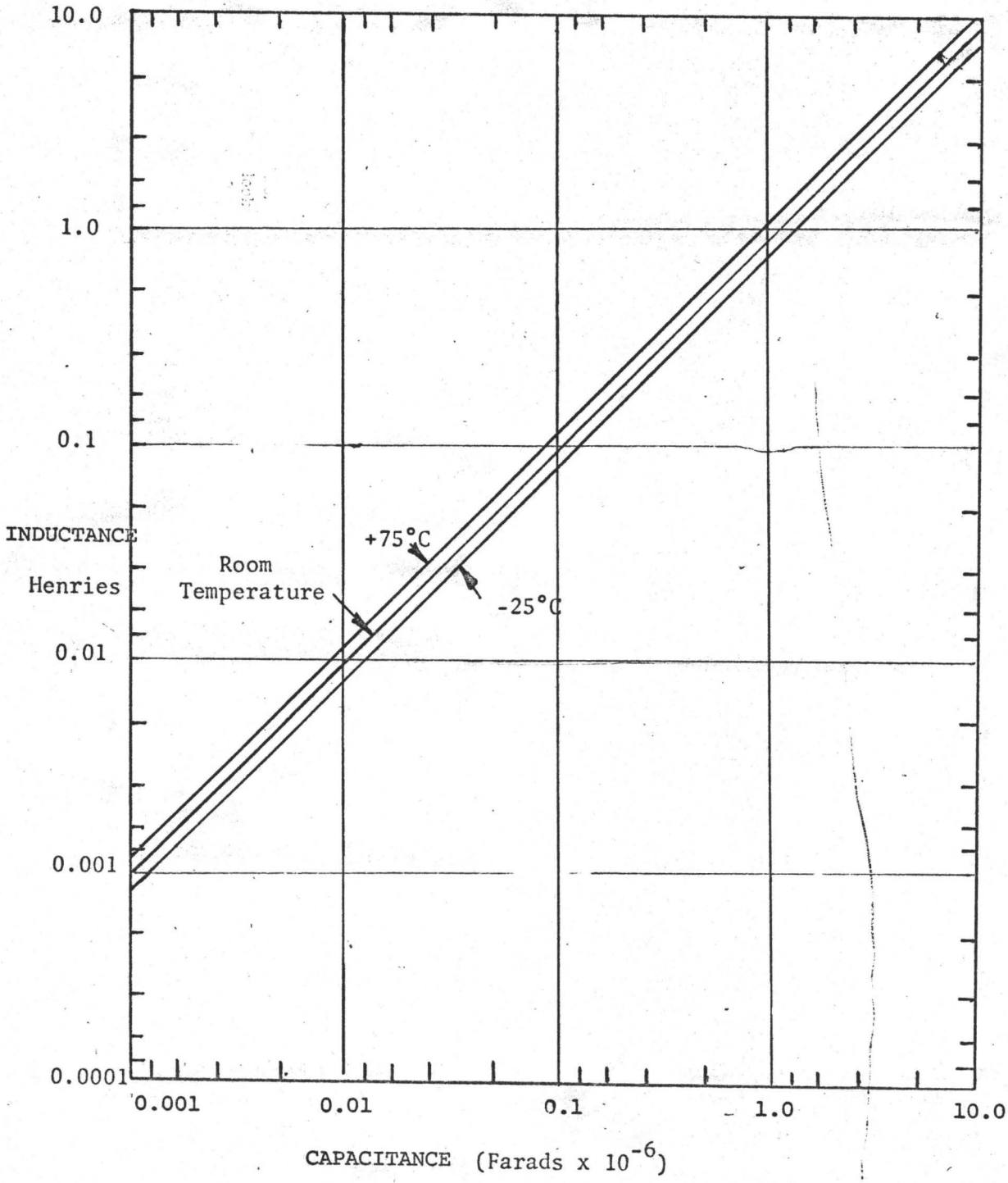


FIGURE 5-2: Input Impedance of Capacitive Terminated Gyrator

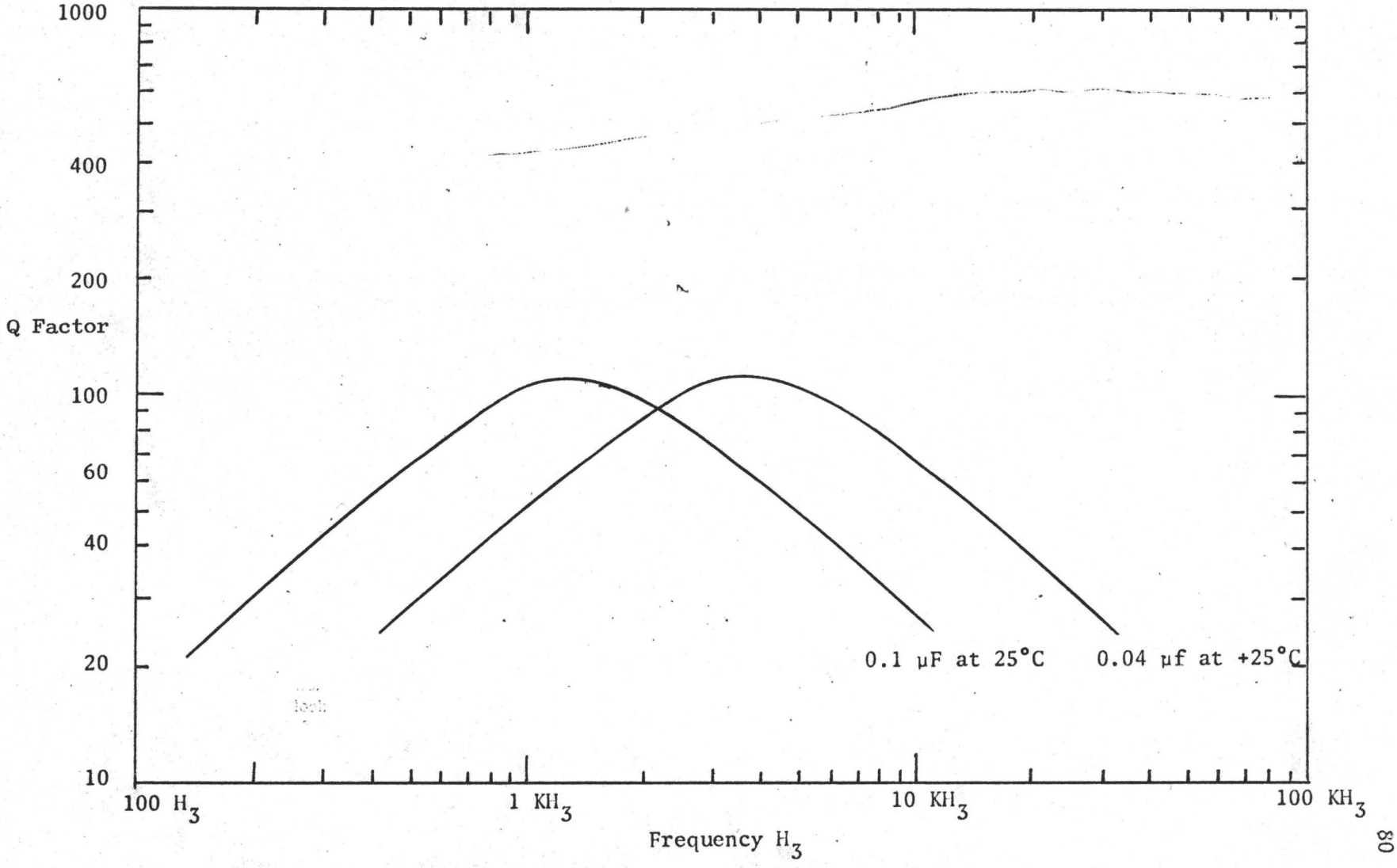


FIGURE 5-3: Q Factor at Room Temperature and Low Frequencies

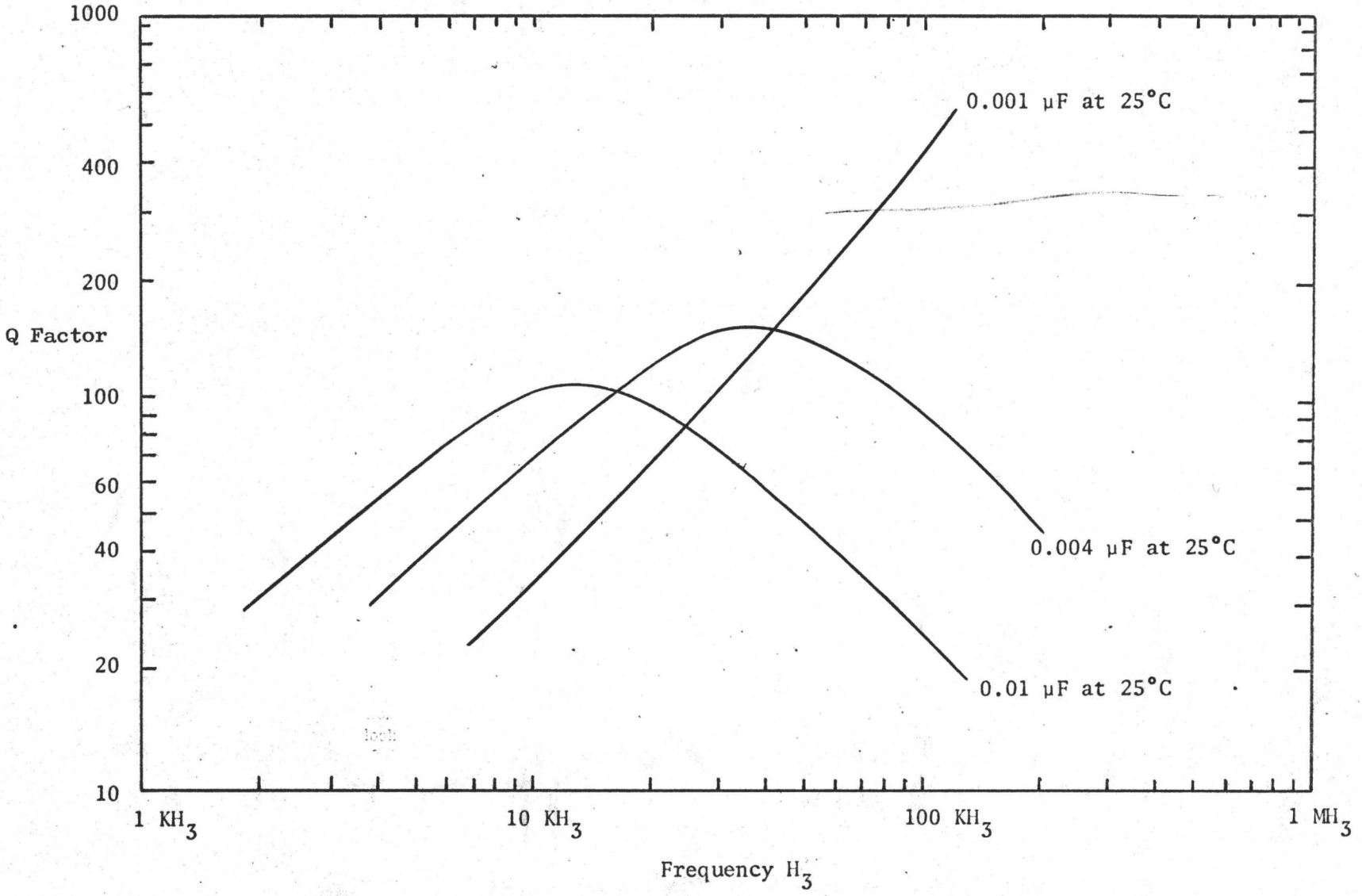


FIGURE 5-4: Q Factor at High Frequencies and Room Temperature

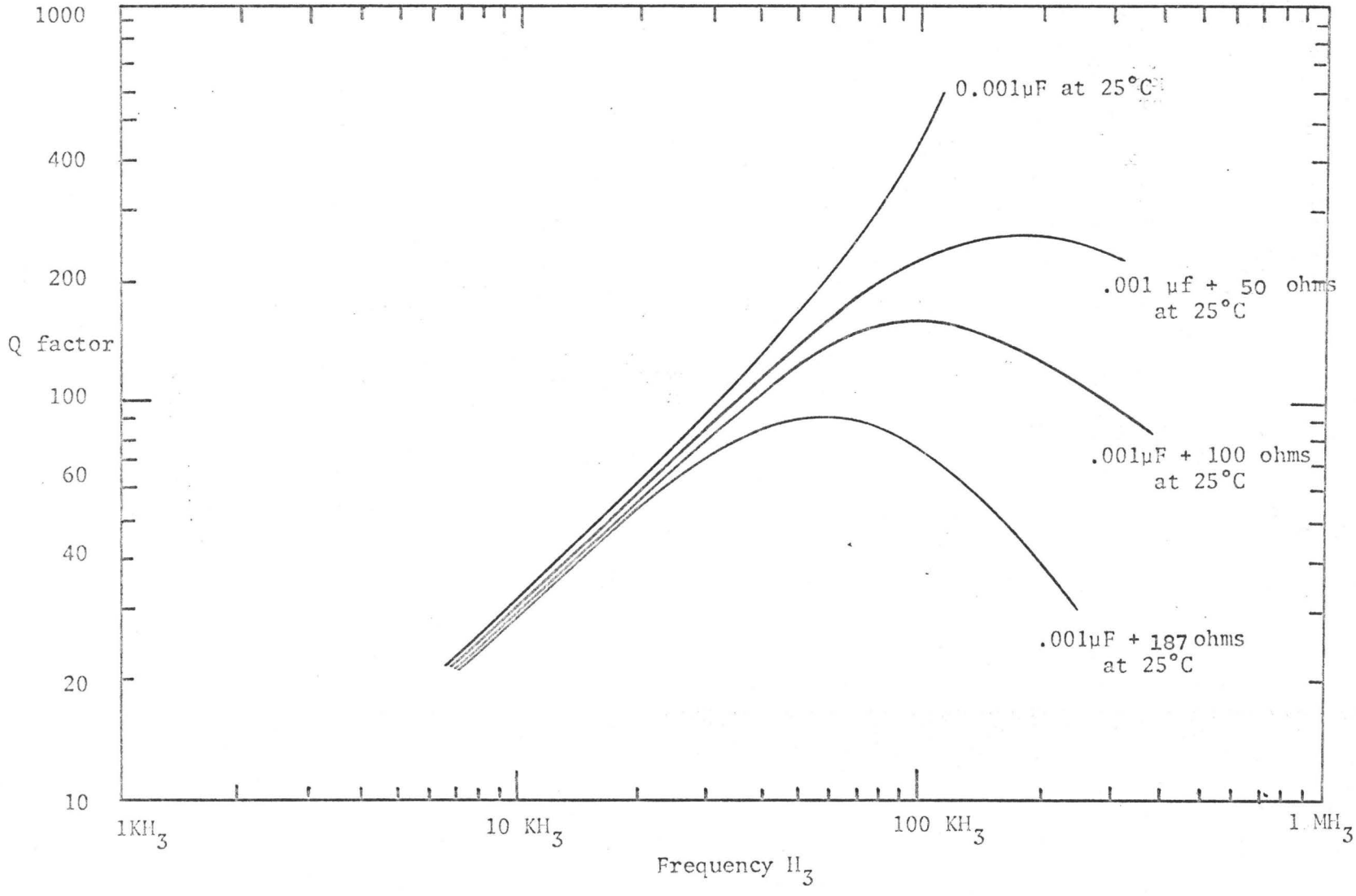


FIGURE 5-5: Q Factor of Compensated Gyrator at Room Temperature

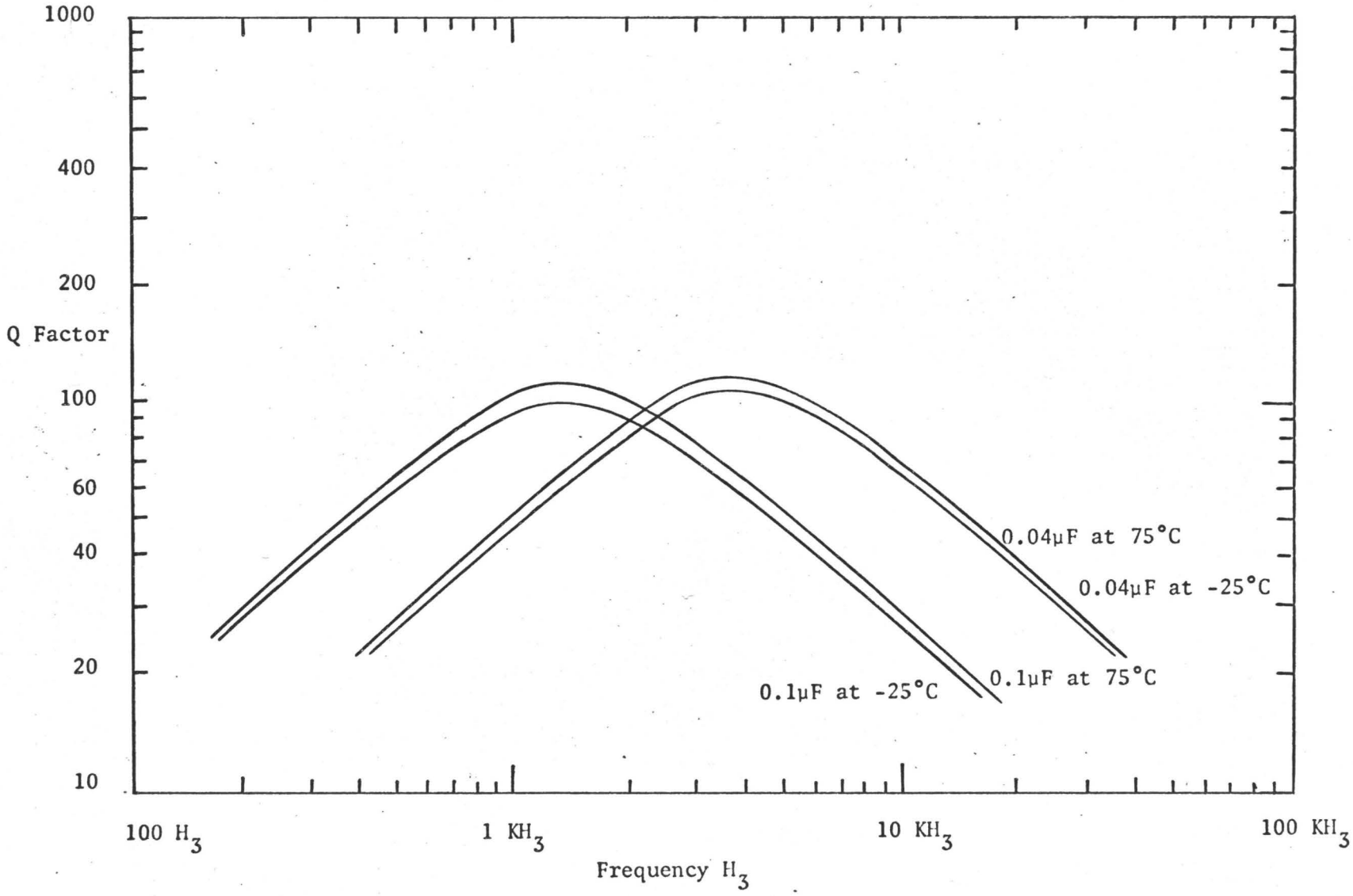


FIGURE 5-6: Q Factor Variation with Temperature at Low Frequencies

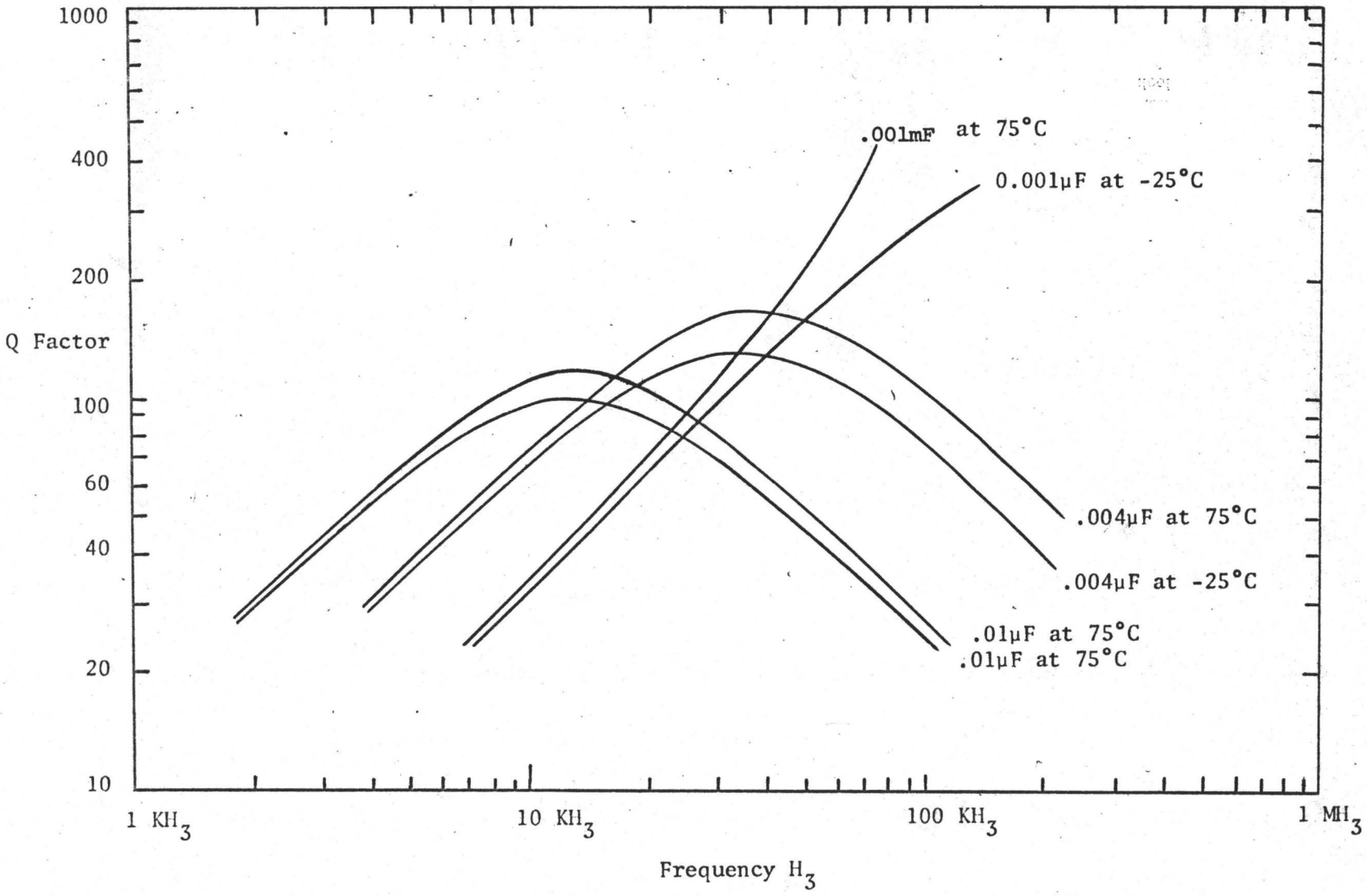


FIGURE 5-7: Q Factor Variation with Temperature at High Frequencies

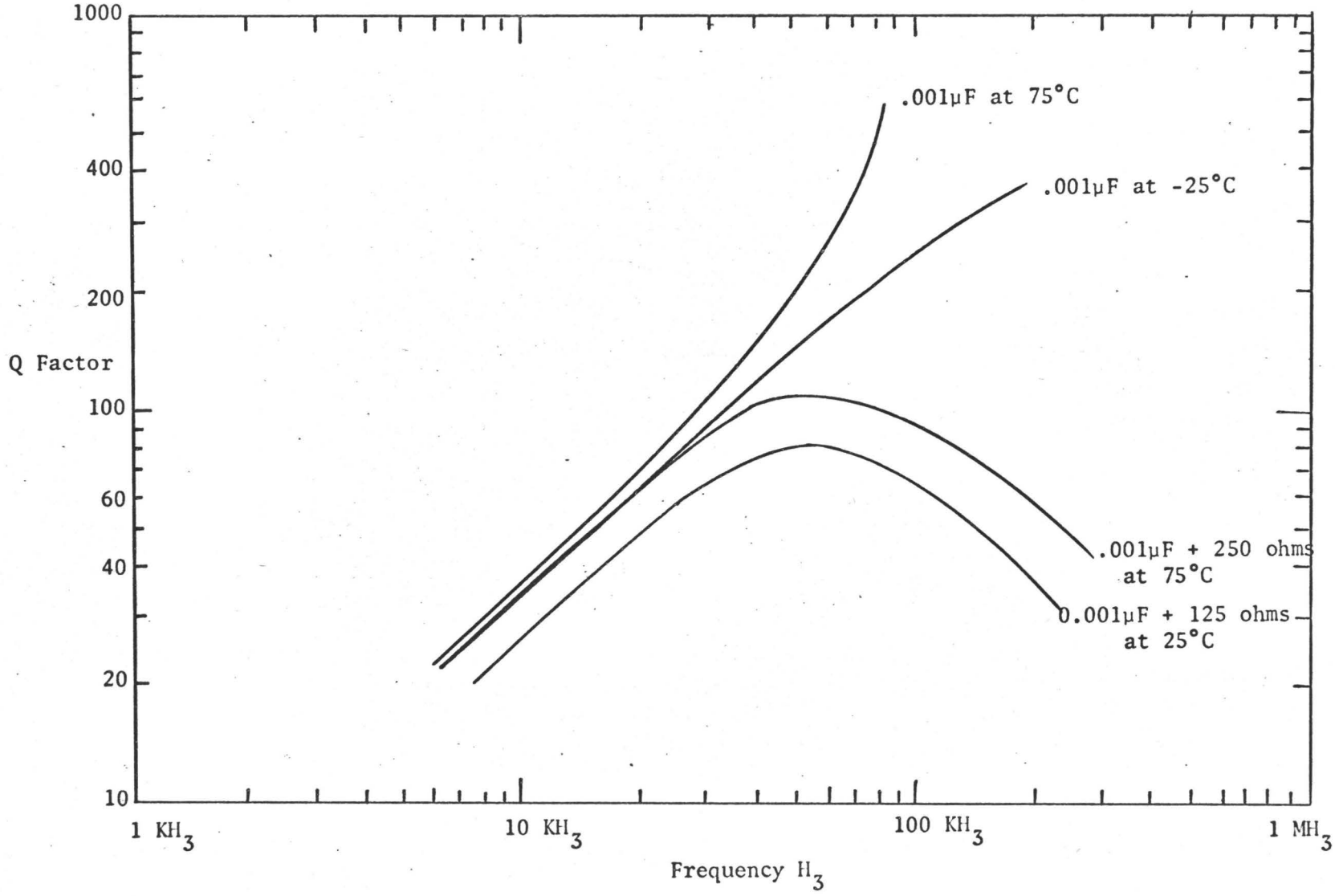


FIGURE 5-8: Q Factor Variation with Temperature and Compensation at High Frequencies

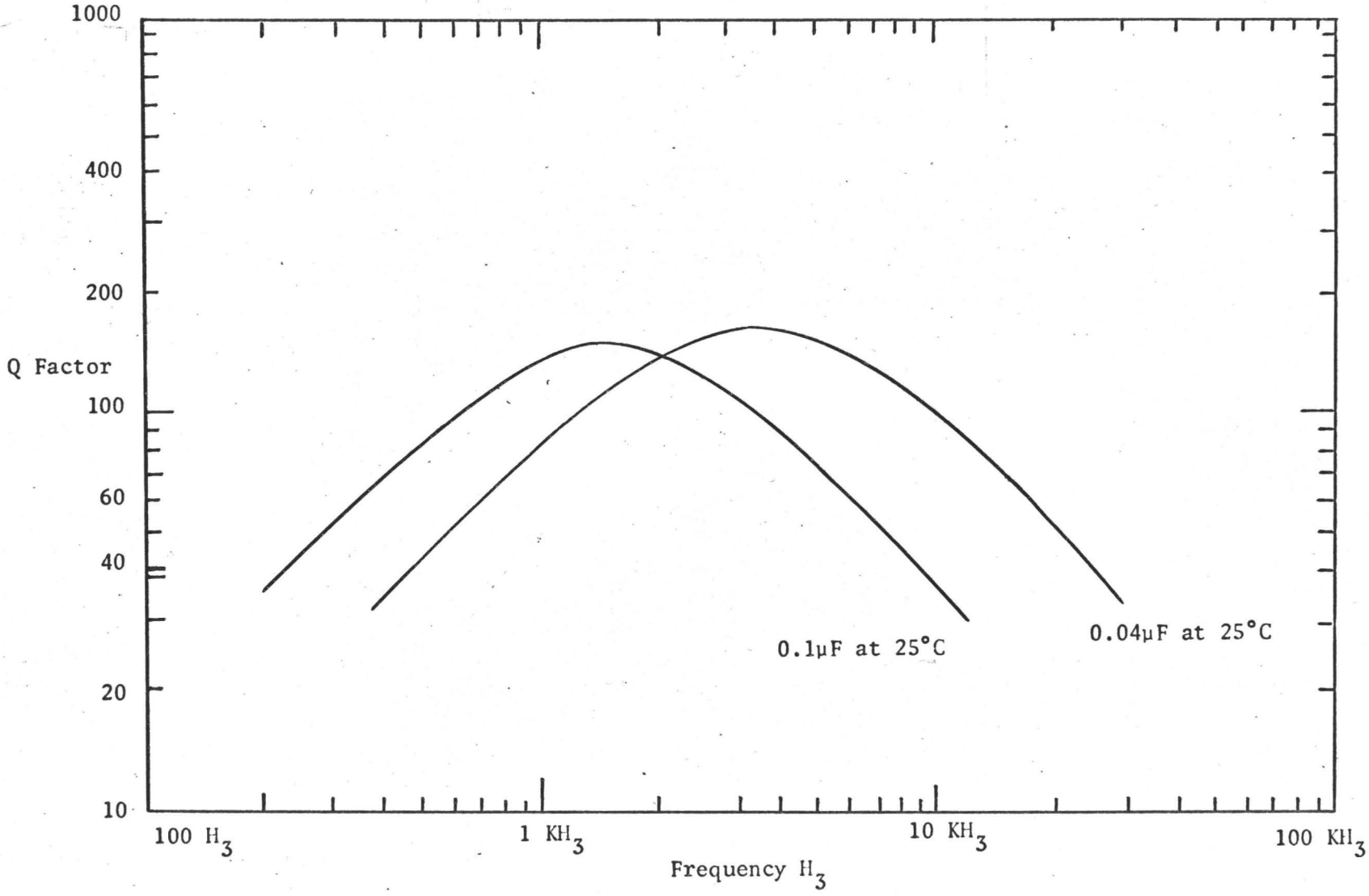


FIGURE 5-9: Q Factor of Gyrator Using Isolated Amplifiers

CHAPTER VI

CONCLUSIONS

From the experimental results given in Chapter V, it can be seen that a relatively high quality monolithic integrated gyrator can be obtained employing the standard fabrication techniques in use today. The results obtained indicate that the qualify of this gyrator is somewhat superior in performance than the gyrator reported by Rao and Newcombe in that the device reported herein has a higher Q factor as well as a higher frequency range. Due to higher operating supply voltages, a larger signal can be applied to the terminals of the gyrator without causing the signal to become distorted. The voltage swing is approximately twice the peak voltage swing of the gyrator of Rao and Newcombe. The gyrator is also suited for varying voltage supplies since the performance is not affected by varying the supply as much as 10%. By using various connections to resistors R_8 and R_4, the gyrator accomodates a wide range of voltage supplies without in any way affecting the quality of the device. Also, the gyrator reported by Rao and Newcombe requires a positive and negative supply voltage as well as a ground terminal. The gyrator shown in figure 2-13 does not need any external ground so that it can operate from both a single or a double supply as well as from a supply where the negative supply is not equal to the positive supply. This is particularly useful in cases where the gyrator output terminals must operate at certain offset d.c. voltages.

Using the compensating techniques developed in Chapter I and demonstrated in Chapter V, the useful frequency range of the gyrator can be extended to a point determined only by the bandwidth of the individual amplifiers. At frequencies where compensation becomes necessary, it is possible to set the Q factor to any value by varying the external resistor connected in series with the terminating capacitor.

The integrated gyrator fabricated is only capable of simulating an inductor which has one terminal connected to ground. However, by connecting a capacitor between output terminals of two grounded gyrators having the same direction of gyration, a floating inductor can be obtained. These grounded gyrators do not have to be operated from the same supply. One device could operate from a single positive supply, while the other from a negative supply with a common ground terminal. This configuration will result in a simulated floating inductor with a d.c. voltage across it.

Due to the fact that the gyration resistance was dependent largely on the resistors R_3 and R_5, the inductance varied considerably with temperature. This was due to the resistance changes in R_3 and R_5 which were not temperature compensated. It is, however, a simple matter to disconnect these resistors and place metal film resistors in their place either externally or on the substrate. This would reduce the variation due to temperature by a factor of 100.

Either resistor R_3 or R_5 or both can be replaced by a variable resistor such as a junction gate field effect transistor. The drain and source terminals would be substituted in place of the fixed resistor. A linear resistor up to several thousand ohms can be achieved with drain to

source voltages up to approximately 5 volts. The resistance can be easily varied by changing the gate to source voltage. This technique is quite practical since present fabrication techniques allow both bipolar and field effect transistors to be produced on the same substrate.

APPENDIX I

CIRCUIT ANALYSIS OF INTEGRATED GYRATOR

A1-1 ANALYSIS OF INVERTING AMPLIFIER:

The output impedance of the inverting amplifier shown in figure 2-11 is the output impedance of the Q_3 - Q_4 combination in parallel with the impedance looking into the collector of Q_5, which is:

$$Z = \frac{1}{h_{ob} - \frac{h_{fb}\ h_{rb}}{h_{ib} + R_8}} \qquad \text{(A1-1)}$$

where h_{ob}, h_{fb}, h_{rb}, and h_{ib} are the h parameters of the transistor operated in the common base mode. R_8 is 8000 ohms. Substituting, the impedance looking into the collector of transistor Q_5 is $Z = 1/h_{ob} = 1.18 \times 10^6$ ohms. Similarly, the output impedance of the Q_3 - Q_4 combination can be found to be 1.18×10^6 ohms so that the output impedance of the inverting amplifier is 5.90×10^5 ohms. The input impedance looking into the emitter of the Q_3 - Q_4 combination is given by

$$Z_{IN} = h_{ib} + \frac{h_{fb}\ h_{rb}}{h_{ob} + \frac{1}{R_L}} \qquad \text{(A1-2)}$$

where R_L is 1.18×10^6 ohms for the open-circuit input impedance and zero for the short circuit input impedance. With $R_L = 0$, the input impedance is equal to h_{ib} or 18.5 ohms. The open-circuit input impedance is 48 ohms. This is considered the load for transistor Q_4 since the

input impedance of the Q_3 - Q_4 combination is much less than the resistance of R_7 which is 1000 ohms.

The current gain A_I for the Q_3 - Q_4 combination is given by:

$$A_I = \frac{h_{fb}}{1 + h_{ob} R_L} \qquad \text{(A1-3)}$$

where the short-circuit current gain is found to be h_{fb} or -0.975 and the open circuit current gain is -0.488.

The current gain of Q_2 is given by

$$A_I(Q_2) = \frac{h_{fe}}{1 + R_L(1 + h_{fe})h_{oe}} \qquad \text{(A1-4)}$$

Thus, the short-circuit current gain is approximately equal to the h_{fe} of transistor Q_2. The exact short-circuit current gain is 39.0 and the open-circuit current gain is 37.4, showing a little difference.

The impedance looking into the base of transistor Q_2 is mainly determined by the resistor R_5 and the overall expression can be reduced to:

$$Z_{IN}(Q_2) = (1 + h_{fe})R_5 \qquad \text{(A1-5)}$$

Thus the input impedance looking into the base of transistor Q_2 is independent of the load resistance of the output stage.

Since the input stage of the inverting amplifier is operated in the common collector mode, the input impedance of transistor Q_2 acts as the load for transistor Q_1. The input impedance of transistor Q_1 and the inverting amplifier is:

$$Z_{IN} = h_{ie} + \frac{R_L(1 + h_{fe})}{1 + h_{oe} R_L} \qquad \text{(A1-6)}$$

where R_L is given by equation A1-5. Thus,

$$Z_{IN} \doteq \frac{R_5(1 + h_{fe})^2}{1 + h_{oe} R_5(1 + h_{fe})} \qquad \text{(A1-7)}$$

The current gain of the first stage is,

$$A_1(Q_1) = \frac{-(1 + h_{fe})}{1 + h_{oe} R_5(1 + h_{fe})} \qquad \text{(A1-8)}$$

The overall short-circuit current gain of the inverting amplifier is:

$$A_{I\ TOTAL} \doteq - \frac{(1 + h_{fe})h_{fe} h_{fb}}{1 + h_{oe} R_5(1 + h_{fe})} \qquad \text{(A1-9)}$$

Substituting the parameters of the transistors yields a current gain of -660 and an input impedance of 7.10×10^5 ohms.

The transconductance of the amplifier y_{21}, is:

$$y_{21} = \frac{I_2}{V_1}\Bigg/_{V_2 = 0} \qquad \text{(A1-10)}$$

which is

$$y_{21} = \frac{h_{fe} h_{fb}}{R_5(1 + h_{fe})} \qquad \text{(A1-11)}$$

and reduces to $y_{21} = 1/R_5$.

The reverse transconductance can be considered to be zero since all the stages have zero reverse current gain.

The Y matrix for the inverting amplifier is thus,

$$[Y] = \begin{bmatrix} 1.41 \times 10^{-6} & 0 \\ -0.97 \times 10^{-3} & 1.69 \times 10^{-6} \end{bmatrix}$$

A1-2 ANALYSIS OF NON-INVERTING AMPLIFIER:

The output impedance of the non-inverting amplifier can be found using similar procedures as used with the inverting amplifier. It is equal to the output impedance of the common base stage of transistor Q_8 in parallel with the current sink impedance of the Q_9 - Q_{10} combination. The output impedance of this stage is identical to that of the inverting amplifier and is 5.90×10^5 ohms.

The input impedance seen at the emitter of transistor Q_8 is 24.4 ohms with the output shorted, and 53.0 ohms with the output open-circuit.

The short-circuit current gain of the output stage is -0.978 while the open-circuit current gain is exactly half the short-circuit gain.

The input impedance of transistor Q_7 is given by the expression

$$Z_{IN}(Q_7) = h_{ie} + \frac{(1 + h_{fe})R_L}{1 + h_{oe}R_L} \qquad \text{(A1-12)}$$

where R_L is equal to R_3 in series with the parallel combination of R_2 and the input impedance of transistor Q_8. Thus

$$R_L = R_3 + \frac{h_{ib} \; R_2}{h_{ib} + R_2} \qquad \text{(A1-13)}$$

and reduces to approximately R_3 since $R_3 = 1000 << h_{ib} = 24$ ohms. The input impedance of transistor Q_7 is

$$Z_{IN}(Q_7) = h_{ie} + \frac{(1 + h_{fe})R_3}{1 + h_{oe} R_3} \qquad \text{(A1-14)}$$

and the current gain of transistor Q_7 is:

$$A_I(Q_7) = - \frac{(1 + h_{fe})}{1 + h_{oe}R_L} \qquad \text{(A1-15)}$$

The input impedance of the non-inverting amplifier and transistor Q_6 is:

$$Z_{IN} \doteq \frac{(1 + h_{fe})^2 R_3}{1 + h_{oe}[h_{ie} + (1 + h_{fe})R_3]} \qquad \text{(A1-16)}$$

and is equal to 7.10×10^5 ohms. The current gain of the amplifier is:

$$A_I = \frac{(1 + h_{fe})^2 h_{fb}}{1 + h_{oe}[h_{ie} + (1 + h_{fe})R_3]} \qquad \text{(A1-17)}$$

and is equal to 660.

The transconductance of the amplifier is readily found to be equal to approximately $1/R_3$.

The Y matrix of the non-inverting amplifier is:

$$[Y] = \begin{bmatrix} 1.69 \times 10^{-6} & 0.98 \times 10^{-3} \\ 0 & 1.41 \times 10^{-6} \end{bmatrix}$$

When the amplifiers are connected in parallel, transmitting in opposite directions, the resultant Y matrix becomes:

$$[Y] = \begin{bmatrix} 3.1 \times 10^{-6} & 0.98 \times 10^{-3} \\ -0.97 \times 10^{-3} & 3.1 \times 10^{-6} \end{bmatrix}$$

APPENDIX II

This appendix is a copy of an article which appears in the IEEE Journal of Solid State Devices, April 1969. The results given in this appendix led up to the final results given in Chapter V.

INTEGRATED CIRCUIT IMPLEMENTATION OF DIRECT COUPLED GYRATOR

by

S.S. Haykim[†], J. Shewchun[*], S. Kramer[†] and D.H. Treleaven[††]

An ideal gyrator may be represented by the parallel connection of two oppositely directed transconductance amplifiers, one with 180 degrees phase shift and the other with zero phase shift. Using such a model, Chua and Newcomb[1] have described an integrated circuit realization of the directly coupled gyrator using bipolar transistors, with a gyration conductance of 0.3 milli-mho and a maximum Q factor of about 18 at 100 c/s or 35 at 5 K c/s. In this article we shall describe an integrated gyrator circuit which also uses bipolar transistors, with a maximum Q factor that is an order of magnitude larger than that reported by Chua and Newcomb. The Q factors reported herein are thus comparable to those reported by Sheahan and Orchard[2] who use a combination of discrete bipolar and M.O.S. field effect transistors; their circuit is, however, more difficult to fabricate in integrated form.

The gyrator circuit is shown in diagramatic form in figure 1(a). The amplifier transmitting from left to right consists of an emitter follower Q1 followed by a common emitter amplifier Q2. The

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† Electrical Engineering Dept., McMaster University, Hamilton, Ont.

* Engineering Physics Dept., McMaster University, Hamilton, Ont.

†† Canadian Westinghouse Co., Hamilton, Ontario

signal developed at the collector of transistor Q2 is applied to a modified Darlington composite pair consisting of a lateral pnp transistor Q3 and npn transistor Q4 and operated in the common base mode. The output signal developed at the emitter of transistor Q4 is thus 180 degrees out of phase with respect to the input signal, and the transconductance of the amplifier is approximately equal to $1/R_5$. The direct current for the modified Darlington composite pair Q_3 - Q_4 is provided by transistor Q5 operated in its common base mode.

The amplifier transmitting from right to left consists of an ordinary Darlington composite pair (Q6 and Q7) operated as an emitter follower. The signal developed at the emitter of transistor Q7 is applied through resistor R_3 to common base transistor Q8. Thus, the amplifier has zero phase shift and a transconductance approximately equal to $1/R_3$. The modified Darlington arrangement of Q9 and Q10, operating in the common base mode, acts as a source of direct current for transistor Q8. Thus, by adjusting R_3 and/or R_5, it is possible to vary the gyration conductance of the circuit.

The various Zener diodes (D_1 to D_4) are employed for the purpose of maintaining the base terminals of the associated transistors in the output circuits of the two amplifier paths at constant d.c. voltages and thereby ensuring their operation in the common base mode.

The gyrator shown in figure 1(a) was implemented with a hybrid monolithic silicon integrated circuit composed of three monolithic silicon chips interconnected as shown in figure 1(b). The largest chip is a Westinghouse "Insta-Circuit Breadboard", WS177T, consisting of some 57 individual components. These are 8 npn epitaxial

transistors, 5 zener diodes, and 44 resistors ranging in value from 20Ω to 20KΩ, all of which are contained on a 0.086" x 0.124" die mounted on a standard T05 header.

The two smaller rectangular chips are Westinghouse IT-11 chips containing 5 epitaxial npn planar silicon transistors and 1 lateral pnp transistor on a 10Ω-cm p-type substrate. These transistors are double-diffused into a 0.35Ω-cm, 10-12μ thick, n-type epitaxial layer over an n^+ epitaxial layer, 2-3μ, grown from a high resistivity p-type substrate. Standard processing conditions give a p-type junction of about 3μ depth. The emitter is diffused to provide a typical base-width of 1.0 - 1.4μ. The lateral pnp is connected with one of the npn transistors in a modified Darlington configuration to give a reasonably good pnp unit.

The lateral pnp transistors have h_{fe} approximately equal to unity, while the npn transistors have an h_{fe} of 70 - 100 (V_{CE} = 5V, I_C = 5ma). The Darlington pair gives a pnp with an equivalent h_{fe} that is closely equal to the h_{fe} of the npn transistor, as shown by

$$h_{fe} = h_{fe\ pnp}(1 + h_{fe\ npn}) \simeq h_{fe\ npn}$$

By measurement, it was found that the gyrator has a mean gyration conductance equal to 0.8 milli-mho. Figure 2(a) shows the Q factor of the gyrator plotted against frequency for different values of terminating capacitance C_1. The increase in the maximum Q factor above 2Kc/s is due to the delay around the gyrator loop.

A 5% change in supply voltages was found to have little effect on the operation of the circuit. Figure 2(b) shows that at low frequencies a temperature change from -25%C to 70°C produces a change in the Q factor that is less than 0.5%. At higher frequencies, however, the temperature changes have a more pronounced effect.

Work is in progress on the monolithic implementation of the gyrator circuit described in figure 1 on a 59 mil by 59 mil chip.

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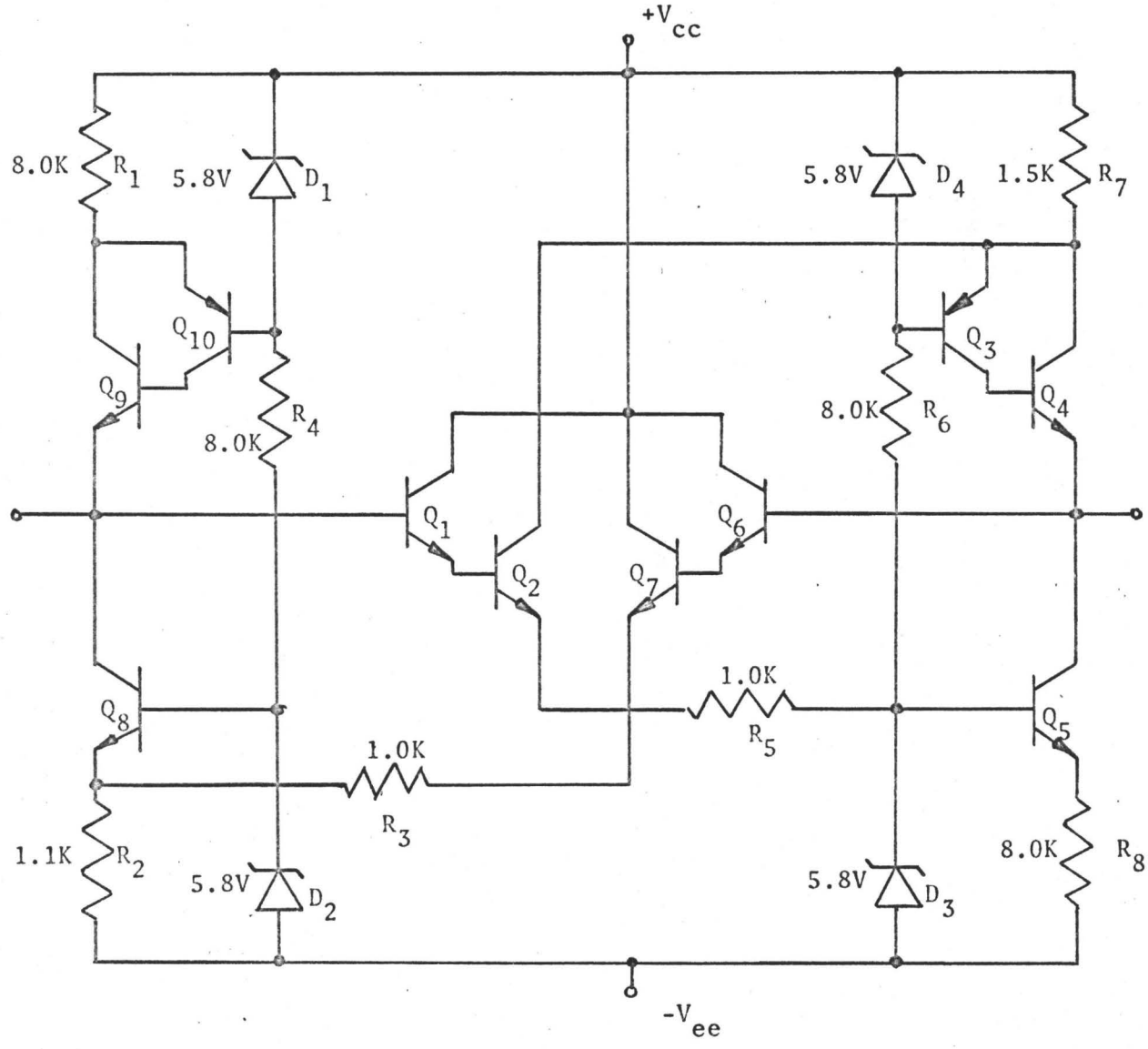

R_1 = 8KΩ
R_2 = 1.1KΩ
R_3 = 1KΩ
R_4 = 8KΩ
R_5 = 1KΩ
R_6 = 8KΩ
R_7 = 1.5KΩ
R_8 = 8KΩ

D_1, D_2 } 5.8V Zener Diodes
D_3, D_4 }

FIGURE 1(a): Grounded Gyrator

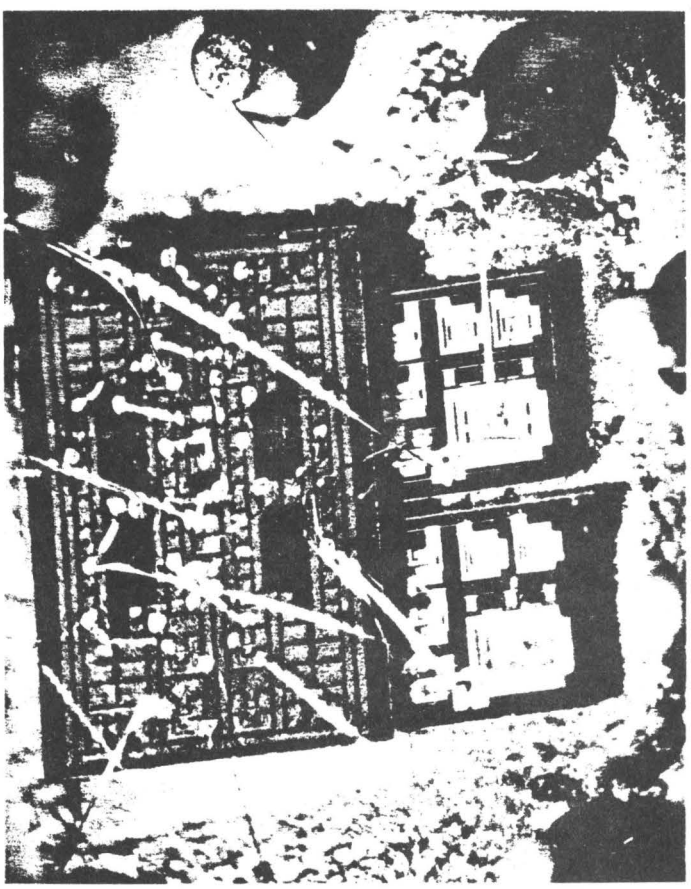

FIGURE 1B

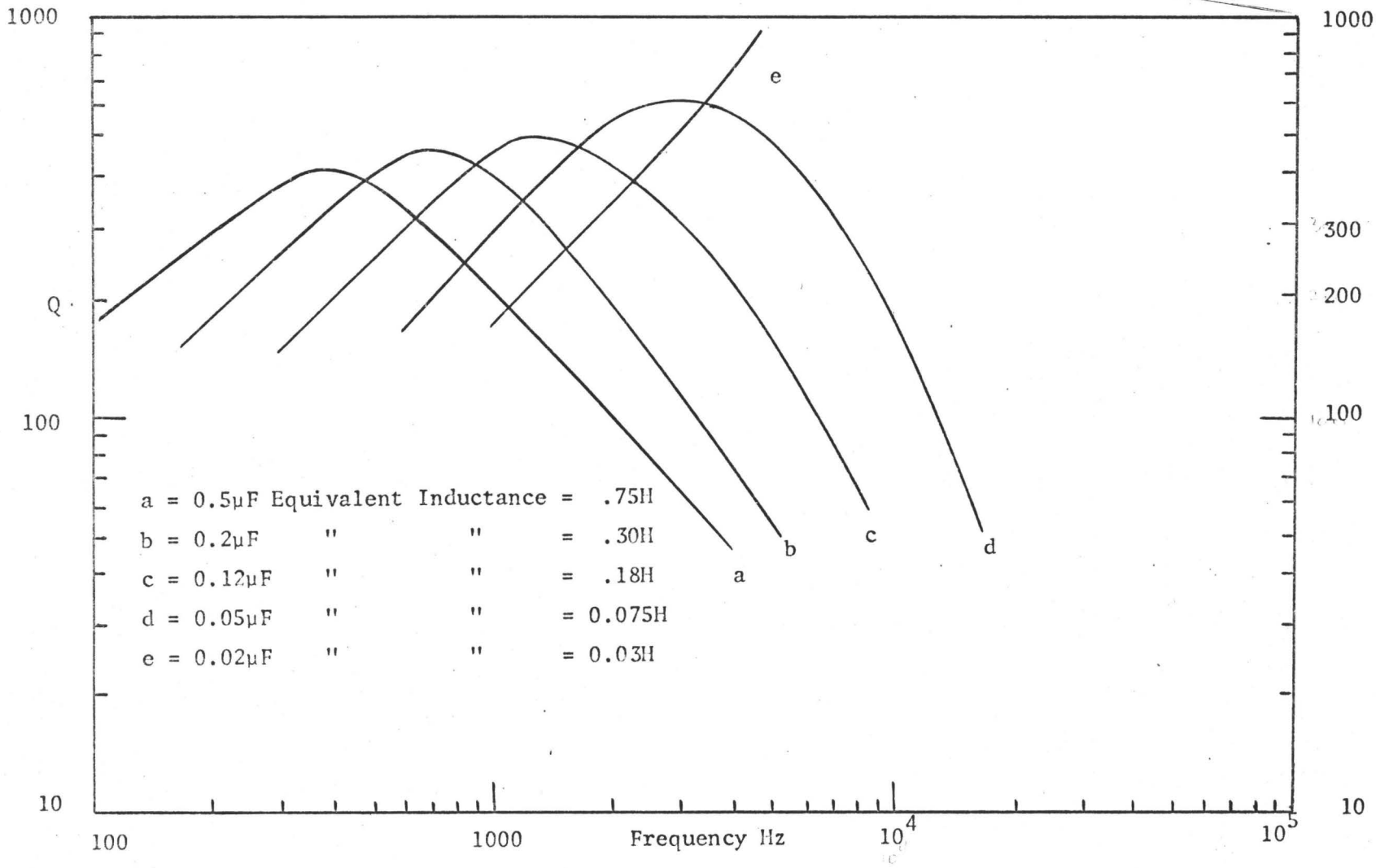

FIGURE 2(a): Measured Q Factor Against Frequency

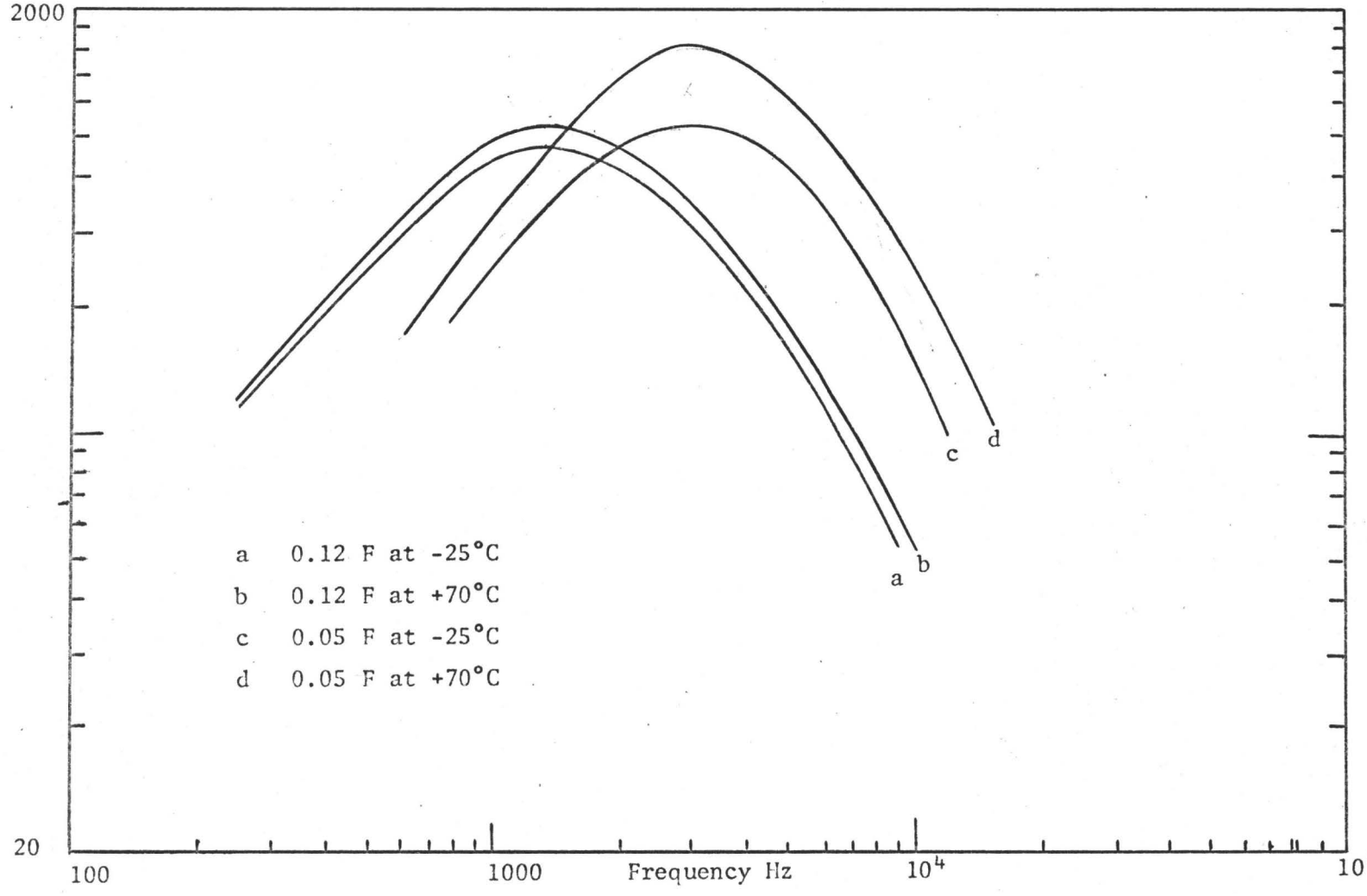

FIGURE 2(b): Q Factor Dependence on Temperature

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