A LOW TEMPERATURE STUDY OF THE N - CHANNEL MOS FET

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by

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SCOPE AND CONTENTS:

The static and dynamic electrical characteristics of silicon n-channel MOS FETs are studied down to cryogenic temperatures. Particular emphasis is directed towards the effect of interface states on the temperature dependence of both the pinch-off voltage and 1/f noise.

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CHAPTER I

Introduction

1.1 The Need for a Low Temperature Active Device

For more than a decade the need for active devices which will function at low temperatures has been recognized[1]. It is possible to distinguish three principal reasons for operating semiconductor devices at low temperatures. One is that the device itself can inherently operate only at these temperatures, as is the case for example with the cryosar or the indium antimonide far infrared detector. For these two cases the use of the device is limited to conditions where low temperature facilities exist for other reasons or where the economic cost of providing them is thought to be justified by the advantages obtained with the devices in question.

The second reason for low temperature operation may be the desire to improve the efficiency or to optimize some desirable characteristic of a device which is otherwise capable of operating at room temperature.

As before, the economic cost of obtaining the higher efficiency is seldom considered justified in practice.

Finally, there is the potentially most important case of the use of semiconductor devices in conjunction with systems which themselves have to operate at very low temperatures. An example of this would be a low noise amplifier required to take full advantage of the excellent resolution of semiconductor radiation detectors operating at cryogenic temperatures[2].

For such a detector it may be convenient to place the amplifier in the same bath as the remainder of the system since it is often desirable to amplify the weak signal and match the impedance of the detector to a terminated cable as close to the point of generation as possible. The advantages to be gained by performing these operations in the low temperature bath are reduced thermal noise, improved frequency response, and reduced pickup of interfering signals.

1.2 The MOS FET as a Low Temperature Active Device

The conventional bipolar transistor is not suitable as a low temperature active device since its operation depends on the flow of minority carriers. The minority carrier concentration is proportional to

the square of the intrinsic concentration, which has both a cubic and exponential temperature dependence, causing the bipolar transistor to be extremely temperature sensitive.

The unipolar insulated-gate field-effect transistor or MOS FET has no injection of excess minority carriers and consequently the temperature dependence of its characteristics is expected to be small. The majority carrier concentration is almost constant down to very low temperatures and even at cryogenic temperatures when the substrate becomes "frozen out" it is still possible to form a surface channel by enhancement-mode operation[3].

It has previously been mentioned that the most important use of an active device at low temperatures would be in conjunction with other systems which themselves must be operated at low temperatures. In this respect the MOS FET is a very versatile device in that it can be operated in either of two regions of its current-voltage characteristics. First, it may be used in the unsaturated mode as an analog switch or variable resistor. In the saturated mode of operation the MOS FET would find use as an amplifier in conjunction with a radiation detector.

1.3 Summary of Contents

It is the purpose of this report to determine the suitability of the MOS FET for low temperature ($4.2^{o}K$ to $300^{o}K$) use in both of the afore mentioned regions of operation. In the case of the unsaturated mode of operation the channel conductance variation with temperature is analysed and shown to be a function of mobility and bulk Fermi level variations with temperature. Discrepancies observed below $77^{o}K$ are postulated to be due to the formation of a charge sheet near the silicon, silicon-oxide interface by trapping phenomena. In the saturated mode of operation the transconductance and 1/f noise variations with temperature are studied. A noise model based on tunneling of the carriers to traps located at the silicon, silicon-oxide interface is used to explain the experimental results. The distribution of these traps over energy and space is shown to play an important role in the low temperature behaviour of MOS FETS.

The experimentation was performed with the use of two individual low temperature facilities. For the region of $77^{o}K$ to $300^{o}K$ a commercial temperature chamber (Delta Design) was used. A liquid helium

cryostat with a proportional temperature controller was constructed to achieve temperatures below 77^{o}K. The two systems are desribed in an appendix.

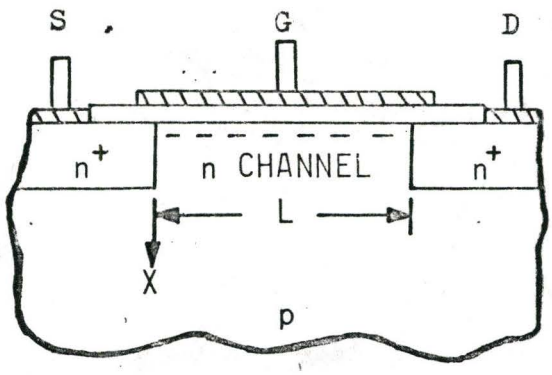
CHAPTER II

MOS Transistor Theory

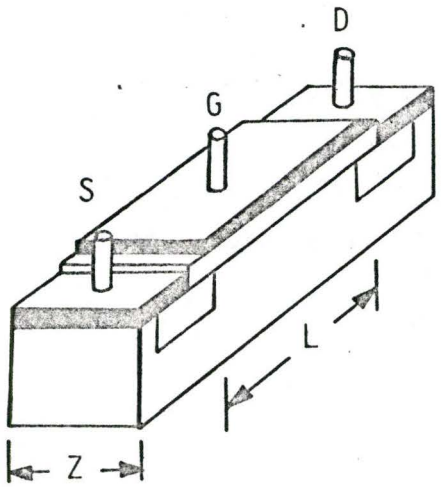
2.1 Physical Structure

The device shown in Fig. 2.1 is designated as an n-channel, depletion type field-effect transistor. The term originates in that the modulation of I_d, the the channel current, by an external field is called the field-effect. The control electrode is called the gate, the two ohmic contacts are the source and drain, and the semiconductor bulk material upon which the channel between the drain and source is formed is called the substrate.

To construct such a device one first starts with a substrate of p-type material. Two separate low resistivity n-type regions are diffused into the substrate. Next, the oxide layer is grown on the surface to a thickness of approximately 1000 Å. Metallic contact to the source and drain are made through holes etched through the insulating oxide layer. The gate metal area is overlayed on the oxide completing the device.



(a)



(b)

FIG. 2.1 n-CHANNEL MOS FET
(a) CROSS-SECTIONAL VIEW
(b) THE LINEAR STRUCTURE

This field-effect transistor has some interesting properties. The metal area of the gate in conjunction with the insulating oxide layer and the semiconductor channel form a capacitor which consequently gives the device a very high input impedance at low frequencies. The source and drain are fundamentally interchangeable. The most important feature of the field-effect transistor is, however, that there is no injection of excess minority carriers. The current is carried by majority carriers.

2.2 Theory of Operation

The following analysis is devided into two sections. The first gives a qualitative description of the internal workings of the MOS FET. The second concentrates on a quantitative discussion which, in due course, yields the characteristic equations describing the MOS FET.

In the following qualitative analysis extrinsic conditions which affect the conduction properties such as oxide traps, silicon surface states and ionic centers within the oxide are lumped together in a single effective charge term, Q_{SS}. Furthermore Q_{SS} is assumed to be constant and located at the silicon, silicon-oxide interface.

2.2.1 Qualitative Analysis

There are three distinct conditions or regions which may be found at the semiconductor surface that are important to MOS FET operation. They are the accumulation, depletion, and inversion regions and are controlled by the external bias on the gate electrode. Generally, for an oxide-passivated surface, surface states or energy states at the silicon, silicon-oxide interface act as ionized donors whose effect is the same as a positive applied gate voltage. In the following discussion drain-to-source voltage is assumed to be so small as to be negligible.

The energy band diagram of an n-channel, depletion type MOS FET under zero applied gate voltage is shown in Fig. 2.2. Electrons from within the p-type bulk are attracted to and accumulated at the surface because of the positive surface state charge. Accumulation results in a downward bending of the conduction and valence bands. The closer the conduction band is bent towards the Fermi level, which is set by the substrate doping, the heavier the surface concentration of electrons becomes. Figure 2.2 illustrates the charge

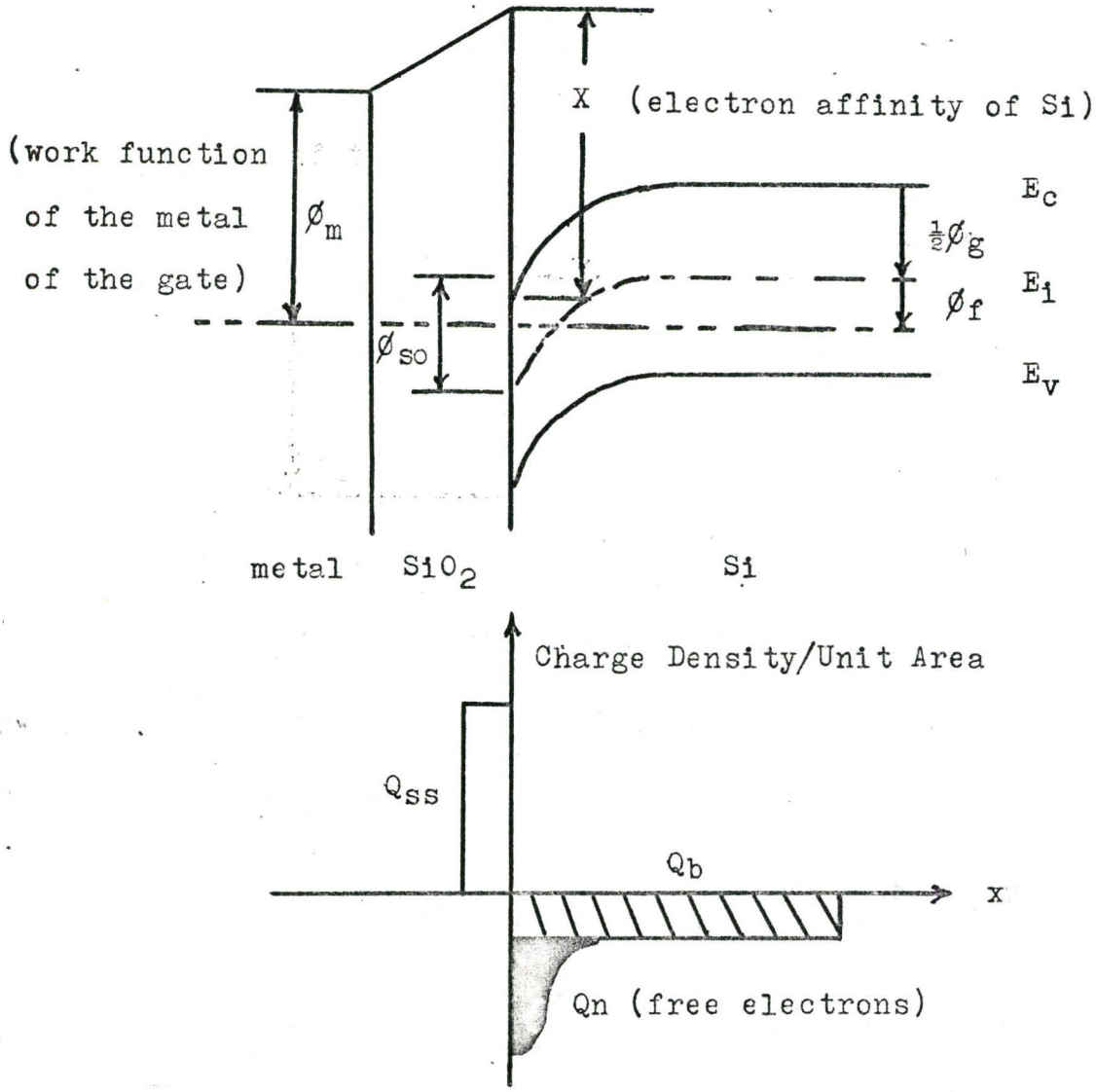


Fig. 2.2 Energy Band Diagram and Charge Distribution for the n-Channel MOS FET with $V_g = 0$

density distribution. The positive charge per unit surface area, Q_{ss}, must be exactly balanced out by the negative charge accumulated near the silicon surface. If a small positive bias is now applied to the gate, additional band bending and accumulation result. Again the total positive charge must equal the total negative charge so as to maintain charge neutrality.

No bending of the bands exists if a negative voltage is applied to the gate such that it just counters the effect of Q_{ss}. A condition which is known as the flat-band case is thus set up. Further application of a negative gate voltage repels from the channel region the mobile electrons and causes the depletion region to extend to the surface. At this voltage conduction can no longer take place.

Conduction between the n-type drain and source occurs only while electrons provide the conducting path. The voltage at which the conduction tends to zero is called the pinch-off voltage. At present it is sufficient to define the pinch-off voltage as that voltage at which the minority carrier density at the surface equals the majority carrier bulk density. This is shown pictorially in Fig. 2.3. A more elaborate definition will be given in the following chapter.

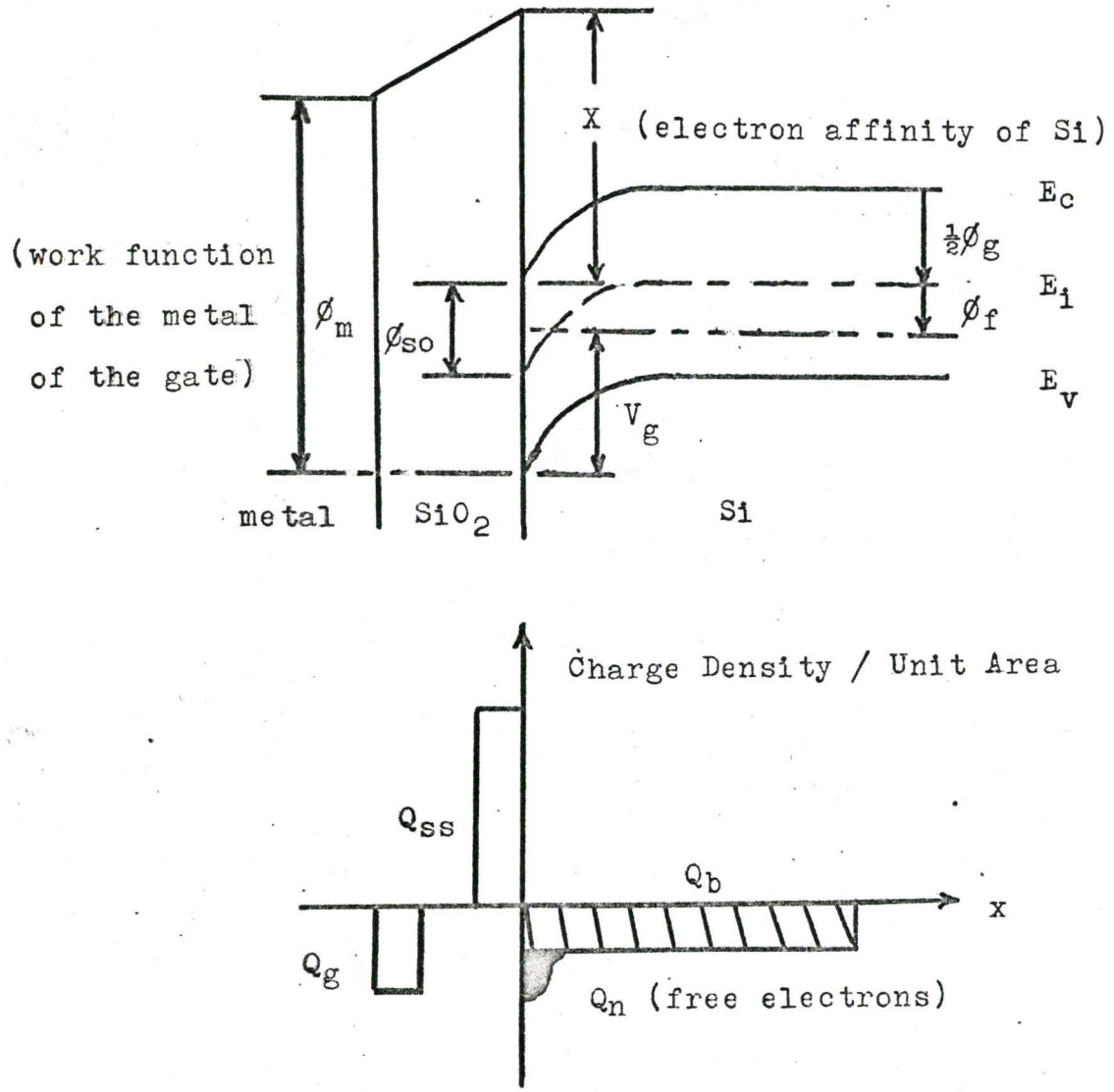


Fig. 2.3 Energy Band Diagram and Charge Distribution for the n-Channel MOS FET with $V_g = V_p$

The end of actual conduction is not an abrupt process in which the channel is completely depleted of carriers but a gradual process. The minority carriers and majority carriers within the channel are decreasing and increasing continuously and at a finite rate for changes of gate voltage.

2.2.2 Quantitative Analysis

In order to bring out some of the important physical parameters which control the electrical characteristics of the surface channel in the MOS FET an analysis based on the theory developed by C. T. Sah is given next [4,5].

Approximations made to develop the theory are as follows:

a) The mobility of current carriers in the channel is independent of the electric fields.

b) The variation of the channel thickness is small along the length of the channel.

c) The thickness of the dielectric over the channel region is assumed to be much greater than the channel thickness.

d) Parasitic resistances (such as at the source and drain) are assumed to be so small as to

be negligible.

e) The channel is completely shielded from the drain, so no drain-to-channel feedback exists.

f) Doping of the substrate is uniform and non-degenerate.

g) The drain current consists only of channel current. Leakage currents are neglected.

h) The gate dielectric is considered to be a perfect insulator.

i) The effects of surface states and interface states are lumped together in a single effective charge term which is assumed to be constant for all conditions.

j) The bulk charge is dependent on the drain to source voltage.

The following "plan of attack" was used by Sah to derive the device equations. By integrating the channel current density over a cross section of the channel the problem of obtaining the external terminal current was reduced to that of finding the total charge in the channel. Sah then proceeded by summing all the system charge to zero and relating it to the gate voltage by the use of Gauss' Law. The expression, thus achieved, was integrated over the length of the channel

and over the drain to source voltage to obtain the following device equation:

$$I_d = u_n C_o (Z/L)\left[(V_g - \phi_{so} - \phi_{ms} + Q_{ss}/C_o)V_d - V_d^2/2 - (4\phi_f V_b/3)\left\{(1 + V_d/2\phi_f)^{3/2} - 1\right\}\right] \qquad (2\text{-}1)$$

where: $\phi_{so} = \phi_{so}(V_g)$ is the surface potential for zero drain to source bias.

$\phi_{ms} = \phi_m - X - \frac{1}{2}\phi_g - \phi_f$ is the work function difference between the metal gate and the semiconductor (see Fig. 2.2).

$V_b = -Q_b/C_o\sqrt{1 + V_d/2\phi_f}$ is the effective bulk charge voltage.

A number of low-frequency small signal parameters may be obtained from Eq. (2-1). The drain conductance, which is defined by $g_d = (\partial I_d/\partial V_d)\Big|_{V_g}$ is given by

$$g_d = (u_n C_o Z/L)\left[(V_g - V_d - \phi_{so} - \phi_{ms} + Q_{ss}/C_o) - V_b\sqrt{1 + (V_d/2\phi_f)}\right] \qquad (2\text{-}2)$$

The condition of zero drain conductance may be used to define the pinch-off voltage for the gate when the drain to source bias is zero. This is then the voltage which must be applied to the gate to induce or cut of the channel conductivity. From Eq. (2-2)

$$V_p = V_g(\ g_d = 0,\ V_d = 0\ )$$

$$= \phi_{so} + \phi_{ms} - Q_{ss}/C_o + V_b \qquad (2\text{-}3)$$

The drain conductance written in terms of this pinch-off voltage is

$$g_d = (u_n C_o Z/L)\left[V_g - V_d - V_p + V_b\left(1 - \sqrt{1 + V_d/2\phi_f}\right)\right] \qquad (2\text{-}4)$$

The condition of zero drain conductance at any drain voltage may be used to define the drain saturation voltage, V_{ds}. For drain voltages greater than this value the drain current is saturated to a constant value independent of the drain voltage and the drain conductance is zero. The drain saturation voltage may be obtained from Eq. (2-4) and is related to the gate pinch-off voltage by

$$V_g - V_p = V_{ds} - V_b\left(1 - \sqrt{1 + V_{ds}/2\phi_f}\right) \qquad (2\text{-}5)$$

The more explicit form obtained from solving the quadratic equation is

$$V_{ds} = V_g - V_p + V_b + (V_b^2/4\phi_f) - V_b\sqrt{1 + (V_b^2/16\phi_f^2) + (V_g - V_p + V_b)/2\phi_f} \qquad (2\text{-}6)$$

In terms of the drain saturation voltage the drain saturation current is

$$I_{ds} = (u_n C_o Z/L)(V_{ds}^2/2 + V_b V_{ds}\sqrt{1 + (V_{ds}/2\phi_f)} - (4\phi_f V_b/3)\left[(1 + V_{ds}/2\phi_f)^{3/2} - 1\right]) \quad (2\text{-}7)$$

The transconductance is another useful small signal parameter which may be derived from Eq. (2-1) and is given by

$$g_m = (\partial I_d / \partial V_g)_{V_d}$$

$$= (u_n C_o Z/L)\left[1 - (d\phi_{so} / dV_g)\right] V_d \quad (2\text{-}8)$$

Calculations carried out by Sah[5] have shown that the effect from the term $(d\phi_{so}/dV_g)$ is rather small and the entire effect of the bulk charge is essentially contained in the drain voltage. The transconductance can therefore be approximated by

$$g_m = (u_n C_o Z/L) V_d \quad (2\text{-}9)$$

and its maximum, which occurs at saturation, is

$$g_m = (u_n C_o Z/L) V_{ds} \quad (2\text{-}10)$$

Sah has noted that the theory he has developed is not entirely valid over the complete extent of the current-voltage characteristics. Discrepancies between

the theoretical and experimental values are to be expected because the theory was developed on the basis of the gradual channel approximation. Discrepancies will thus be found in the transition region of the current-voltage characteristics and also in the low current region near pinch-off (i.e. $V_g \approx V_p$). Here the inversion layer is not yet fully formed and the gate electric field terminates on comparable quantities of mobile charge (in the channel area) and immobile charge (in the depletion region beneath the channel). The gate voltage no longer controls the channel conductance in the manner stated by Eq. (2-1) because of this fact.

It is evident from Eq. (2-1) and Eq. (2-3) that if both the drain-to-source voltage and the gate voltage are maintained constant the drain current will vary with temperature due to the temperature dependence of both the channel current mobility, u_n, and the pinch-off voltage, V_p. These two important mechanisms which contribute to the temperature dependence of the MOS FET will be analysed in the following chapter.

2.3 Low Frequency Noise

The circumstances in which 1/f noise has been observed, and the difficulties of explaining this prevalent type of noise spectrum by a specific mechanism have been discussed in many papers. One of the difficulties is that in general both majority and minority carrier free times are too short to account for very low frequency noise. Additional "slow" events need to be involved.

One explanation of the noise spectra of MOS transistors, based on an equivalent circuit for the semiconductor surface, has been given by A. Jordan and N. Jordan [6]. They concluded that fluctuations of the minority carrier concentration dominated the low frequency noise. The noise spectrum, they obtained, depends on the depletion layer capacitance and not the surface state density. Experiments have shown that the low frequency noise in MOS FETs has a 1/f spectrum down to very low frequencies and is directly proportional to the interface state density [7]. It is for this reason that a second model has been chosen to explain the experimental results.

In this model[8] the low frequency noise voltage spectrum for a MOS transistor is calculated under the assumption that a time constant dispersion giving a 1/f-spectrum could be caused by tunneling of carriers from the channel to traps located at the silicon, silicon-oxide interface and to traps located in the oxide near the interface. The model predicts that the 1/f-noise is directly dependent upon the interface state densitty, mainly the density at the Fermi level at the interface.

Christensson et al[8] calculated the equivalent[gate noise voltage for a MOS FET by determining the change in gate voltage necessary to keep the output (i.e. the drain current) noiseless when the channel was subjected to charge fluctuations. Their model is summarized as follows.

The frequency spectrum of the mean-square fluctuation $\langle(\Delta\Lambda\delta n_t)^2\rangle$ in the number of trapped carriers in an elemental volume $\Delta\Lambda$ is given by

$$S_{\Delta\Lambda\delta n_t} = 4B \frac{\tau}{1 + w^2\tau^2} N_t f_t f_{pt} \qquad (2\text{-}11)$$

where: B = bandwidth of the system.

τ = decay time constant of the capture process considered.

N_t = density of the traps considered ($cm.^{-3}$).

$f_t = 1 - f_{pt} = \dfrac{1}{1 + \exp(E_t - F_t)/kT}$ is the fraction of filled states under steady state conditions.

E_t = trap energy level.

F_t = quasi Fermi level of the traps.

The elemental volume $\Delta\Lambda$ shown in Fig. 2.4 is

$$\Delta\Lambda = Z\, dy\, dx \qquad (2\text{-}12)$$

where Z is the width of the channel.

The mean-square carrier fluctuation

$$\langle(\Delta\Lambda\delta n_t)^2\rangle = \langle(\delta N)^2\rangle \qquad (2\text{-}13)$$

in an elemental volume $\Delta\Lambda$ of the oxide (in the term oxide is included the silicon, silicon-oxide interface region) at a distance y along the channel gives a mean-fluctuation in drain current, $\langle(\delta I_d)^2\rangle$, given by

$$\langle(\delta I_d)^2\rangle = \left(\frac{I_d}{Ln(y)}\right)^2 \langle(\delta N)^2\rangle \qquad (2\text{-}14)$$

where n(y) is the carrier density per unit length in the channel at point y, and δN is the carrier fluctuation in the elemental volume $\Delta\Lambda$.

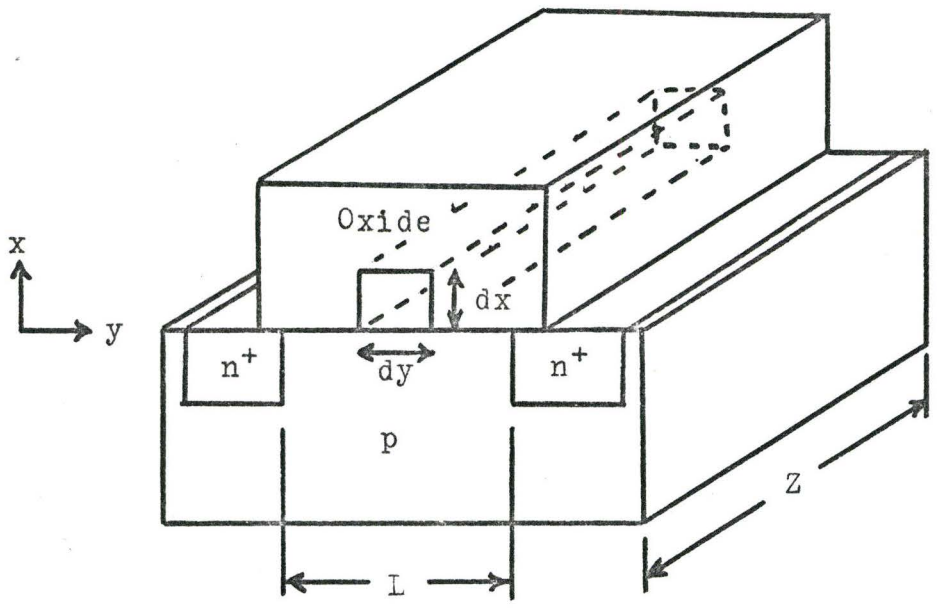


Fig. 2.4 The Elemental Volume Zdydx in the n-Channel MOS FET

From simple MOS FET theory it can be shown that

$$I_d = \frac{uZC_o}{L}\left(V_{ds} - \frac{V_d}{2}\right)V_d \qquad (2\text{-}15)$$

and

$$n(y) = \frac{ZC_o}{q}\left|V_{ds} - V(y)\right| \qquad (2\text{-}16)$$

The frequency spectrum of the mean square fluctuation in drain current due to the fluctuations in the number of carriers trapped in an elemental volume $\Delta\Lambda$ at the point y along the channel may be written, using Eqns. 2-11, 2-14, 2-15, and 2-16 as

$$S_{\delta I_d} = \frac{4Buq^2 I_d}{C_o L^2 \left|V_{ds}-V\right|} N_t\, f_t\, f_{pt}\, \frac{\tau}{1+\omega^2\tau^2}\, dx\, dV \qquad (2\text{-}17)$$

The transconductance, g_m, is given by

$$g_m = \left.\frac{\delta I_d}{\delta V_g}\right|_{V_d} = \frac{uC_oZ}{L}V_d \qquad (2\text{-}18)$$

The frequency spectrum of the gate voltage compensating the charge fluctuations in the elemental volume $\Delta\Lambda$ of the oxide is thus $S_{\delta V_n} = S_{\delta I_d}/g_m^2$

$$S_{\delta v_n} = \frac{4Bq^2}{C_o^2 Z L} \frac{2V_{ds} - V_d}{2V_d} N_t f_t f_{pt} \cdot$$

$$\frac{\tau}{1 + \omega^2\tau^2} \frac{dV\, dx}{|V_{ds} - V|} \qquad (2\text{-}19)$$

The total input gate noise voltage spectrum, $S_{v_n} \equiv v_n^2$, is obtained by integrating equation (2-19) over the distance into the oxide over which traps are distributed and over voltage from zero to the applied drain voltage V_d. Generally there are two types of trapdistributions: a distribution in energy of traps over the silicon bandgap and a distribution over space inside the oxide. Furthermore, f_t changes along the channel under non-equilibrium conditions, and τ may change with distance along the channel, with distance from the interface, and with the trap energy level. The general formula for the spectrum of the noise voltage is then

$$v_n^2 = \frac{4Bq^2}{C_o^2 Z L} \frac{2V_{ds} - V_d}{2V_d} \int_0^{V_d} \int_{E_v}^{E_c} \int_0^{d_t(E)} N(E,x) \cdot$$

$$f_t(E,V) f_{pt}(E,V) \frac{\tau(E,V,x)}{1 + \omega^2\tau^2(E,V,x)} \frac{dx\, dE\, dV}{|V_{ds} - V|} \qquad (2\text{-}20)$$

where: $E_c - E_v$ = bandgap energy of silicon

$d_t(E)$ = distance over which traps of energy E are distributed.

$N(E,x)$ = trap distribution over energy and over distance in the oxide.

The above mathematical expression for the input gate noise voltage was evaluated as follows.

The time constant dispersion was found for a tunneling model by use of SHOCKLEY-READ-HALL statistics.* To calculate the probability of finding an electron at a distance x from the interface a square potential barrier was used. The lowering of the potential barrier by the image force was neglected. The final result obtained was a broad 1/f-spectrum which prevailed up to the frequency region where thermal noise and other noise mechanisms were more important.

To calculate the magnitude of the noise required an integration over voltage along the channel. For small drain voltages, i.e. near equilibrium, this simply meant a multiplication by $f_t f_{pt}(V_d/V_{ds})$. For larger drain voltages, when the factor $f_t f_{pt}$ also changed along the channel, the integration was more complicated.

Christensson et al calculated and compared this

*W. Shockley and W. Read, Pys. Rev. 87, 835, 1952.

factor for different trap levels and distribution. They found the difference in noise contribution from a continuous distribution of traps and a discrete trap level very small at small drain voltages. Such was the case because of the small change in the position of the Fermi level at the surface along the length of the channel. Effectively it was almost the same trap level causing the noise along the entire channel. A continuous trap distribution was found more effective in noise generation at larger drain voltages because the Fermi level position in the bandgap varied along the channel length. The traps in an energy region of about 4kT about the Fermi level were found most effective in noise generation.

Taking together the different calculations of Christensson et al the noise voltage caused by trapping phenomena at the carrier Fermi level at the interface may be written in the 1/f region as

$$\frac{v_n^2}{B} = N_t \frac{4q^2}{C_o^2 ZL} \; 0.25 \; \frac{\pi}{2\alpha\omega} \qquad (2\text{-}21)$$

where: $N_t \approx \frac{N_t(E)}{d_t} \; \frac{4kT}{q}$

$N_t(E)$ is the trap distribution ($cm.^{-2}\ ev^{-1}$)

$\alpha = \frac{2}{\hbar}\sqrt{2}\ m^* W$ and m^* is the effective mass, W is the height of the barrier and $\hbar$ is Planck's constant divided by 2π.

Equation 2-21 lends itself to a theoretical calculation and explanation of the observed temperature dependence of the 1/f noise voltage spectrum. Further insight as to the effects of such parameters as gate voltage, drain voltage, and trap density on the quantity of noise may also be gained. The effects of temperature changes on the quantity of noise will be discussed in the following chapter.

CHAPTER III

Temperature Dependence of the MOS FET

3.1 The Channel Conductance

The mobility of the free carriers in the channel between the drain and source will vary as a function of temperature. The mobility of the conduction band electrons in the channel will be dependent upon the scattering processes, and , in particular, the mean number of collisions per unit time made by an electron. As the temperature decreases, the number of electron-lattice collisions per unit time also decreases. This increases the average drift velocity of the electrons and hence increases their mobility. It may therefore be said that a decrease in temperature will increase the conductivity of the channel by this higher mobility and thus will increase the drain current.

The second factor to be considered is the temperature dependence of the pinch-off voltage. Examination of Eq. (2-3) leads to the conclusion that the temperature dependence of the pinch-off voltage, V_p, may be caused by the temperature dependence of the

bulk Fermi level, the bulk charge and the surface state charge. The bulk charge variation is explicitly dependent upon the movement of the bulk Fermi level with temperature (see Eq. (2-1)). The temperature dependence of the surface state charge is not as evident. It is likely that a more thorough study of the surface state charge will lead to a restatement of approximation (i) in chapter 2.2.

Investigations of temperature effects ($T > 77^{o}K$) in MOS transistors have been reported by F. Heiman and H. Miller [9] and also by L. Vadasz and A. Grove [10]. Vadasz and Grove were able to show that the role of surface states in determining the temperature dependence of their samples was negligible. On the otherhand the density of surface states in the samples used by Heiman and Miller was so large that the influence of the bulk depletion charge and the variation of the mobility with temperature was overshadowed by the temperature dependence of the surface states.

The following study is made with the assumption that, in the range $77^{o}K < T < 300^{o}K$, the mobility variation with temperature and the bulk Fermi level movement with temperature are the significant factors

contributing to the temperature dependence of the MOS FET. By combination of these two factors a solution for the unsaturated channel conductance as a function of temperature is developed and found to be in reasonable agreement with experimental observations. The role of surface state trapping phenomena is discussed in the succeeding section.

The drain conductance written in terms of the pinch-off voltage was given in Eq. (2-4). At very small drain voltages, when the channel is virtually homogeneous (V_d = .01 volts), Eq. (2-4) reduces to the following

$$g_d = u_n C_o \frac{Z}{L} (V_g - V_p) \Big|_{V_d = .01} \qquad (3\text{-}1)$$

Equation (3-1) states that the drain conductance curve plotted as function of gate voltage is a straight line. The gate voltage at which $g_d = 0$ is the pinch-off voltage. It was previously mentioned that the theory is incorrect in the region where $V_g \approx V_p$ because the end of conduction is a gradual process and not an abrupt one. However, for the ease of comparison between theory and experiment, V_p will be defined as that voltage to which the straight line portion of the g_d vs. V_g curve extrapolates for $g_d = 0$.

The pinch-off voltage given by Eq. (2-3) may be written as

$$V_p = 2\phi_f + (\phi_m - X - \tfrac{1}{2}\phi_g - \phi_f) - \frac{Q_{ss}}{C_o}$$

$$+ \frac{\sqrt{4qN_aK_s\epsilon_o\phi_f}}{C_o} \qquad (3\text{-}2)$$

where: $\phi_{so} = 2\phi_f$ is the surface potential at which inversion is considered to take place[5,11].

$Q_b = -\sqrt{4qN_aK_s\epsilon_o\phi_f}$ is the depletion region charge per unit area.

$\phi_{ms} = \phi_m - X - \frac{1}{2}\phi_g - \phi_f$ is the work function difference between the metal gate and the semiconductor. Note: the temperature dependence of the energy gap has been neglected in comparison to that of ϕ_f [12].

$\phi_f = kT/q(\ln N_a/n_i)$ is the bulk Fermi level. At cryogenic temperatures ϕ_f eventually comes to rest at or in the vicinity of the impurity level and the above equation no longer holds.

The entire temperature dependence of the pinch-off voltage can thus be given in terms of ϕ_f.

$$V_p(T) = \phi_f + \frac{2t_{ox}}{K_o\epsilon_o}\sqrt{qN_aK_s\epsilon_o\phi_f} \qquad (3\text{-}3)$$

where: $C_o = K_o\epsilon_o / t_{ox}$ is the capacitance per unit area of the oxide.

Figure 3.1 illustrates the temperature dependence of the above equation for an acceptor doping of 10^{16} cm.$^{-3}$ and an oxide thickness of 1000 Å.

According to this theory the pinch-off voltage decreases in magnitude, almost linearly, with temperature. Below 100°K contributions to V_p from the temperature dependence of the bulk Fermi level become progressively less and less important and the pinch-off voltage becomes almost independent of temperature. One might at first expect that deionization of the impurity dopant would contribute to V_p. However, the effect of the impurity deionization is negligible as ϕ_f eventually comes to rest at or in the vicinity of the impurity level.

Later it will be shown that experimental measurements indicate the pinch-off voltage to be more

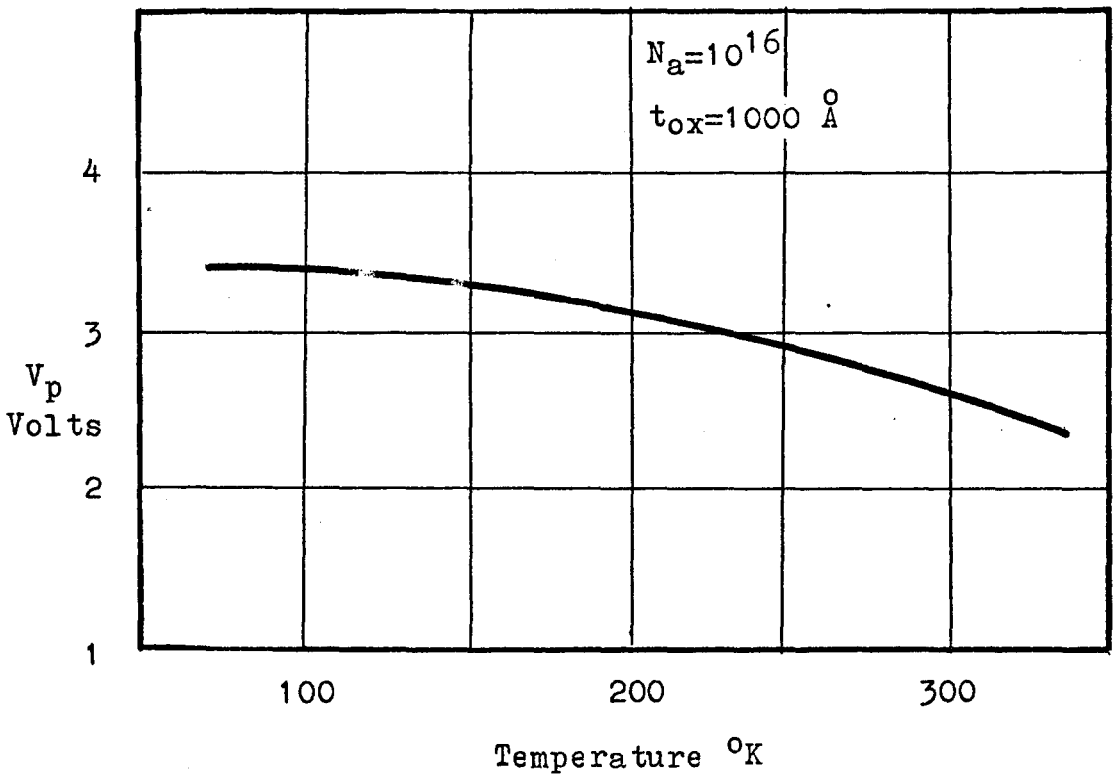


Fig. 3.1 Temperature Dependence of the Pinch-off Voltage (the contribution of $\phi_m - X \frac{1}{e}\phi_g - Q_{ss}/C_o$ has not been included)

temperature dependent below 77°K then at room temperature. A similar observation has been made by H. Nathanson [13] for both n and p channel MOS FETs. This implies that a more thorough examination of the role played by surface states is required because no other term in Eq. (2-3) can account for the large temperature dependence of the pinch-off voltage at cryogenic temperatures.

3.2 Surface States

Many experiments [14] indicate that there are two classes of surface states. States of the first class are called slow surface states or layer states because they exchange charge very slowly , if at all, with the bulk material. The time constants of charge exchange range from a few seconds to months. These states are intimately associated with the surface chemistry and with the oxide layer on the silicon. They are strongly affected by the ambient and are thought to be the result of ions absorbed by the thin oxide covering the surface of the semiconductor. The density of these states appears to depend on the adsorption equilibrium with the ambient, and is not a constant of the surface except in ultrahigh vacuum. These states are of great importance in device

technology because they largely determine the initial surface potential. With present day manufacturing techniques the surface potential due to layer states has been made very stable and is relatively temperature independent [15].

States of the second class are called fast surface states or chargeable interface states because they exchange charge with the bulk material with time constants ranging from milliseconds to microseconds or less. These fast surface states are thought to exist at or near the interface between the semiconductor and the oxide. Their density is unaffected by the atmospheric ambient. Unlike the layer state the chargeable interface states do have a temperature dependence in that they are capable of trapping free carriers.

For the subsequent theory trapping is defined as the capture of a carrier followed by its subsequent release back into the band from which it came, and not by the capture of the opposite carrier amounting to recombination. Schematically this process is represented in Fig. 3.2 by a center with allowed transitions only to one of the bands, the complementary transition being so much less likely that it may be neglected.

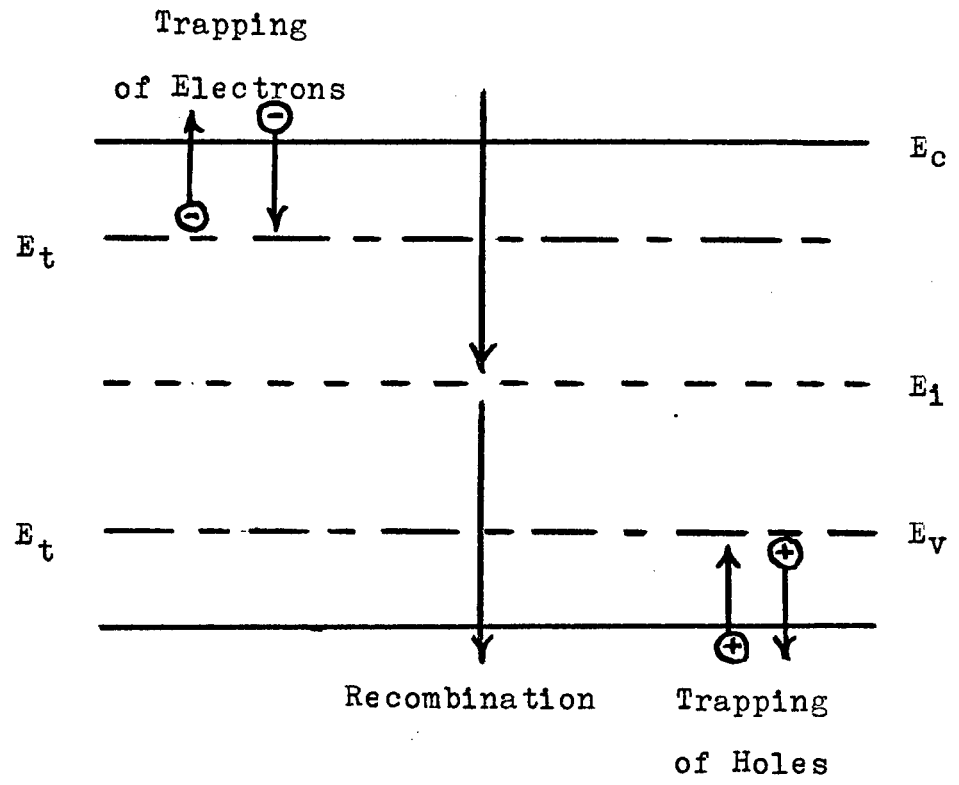


Fig 3.2 Recombination and Trapping Levels

The number of trapped carriers at any one time is governed by Fermi-Dirac statistics. Taking into account the effects of spin degeneracy the probability of a trap site at energy E_t being occupied is given by (16)

$$f(E_t) = \frac{1}{1 + g \exp\left(\frac{E_t - E_f}{kT}\right)} \qquad (3\text{-}4)$$

where: $g = \frac{1}{2}$ for acceptor-type traps and $g = 2$ for donor-type traps.

At equilibrium, the surface potential adjusts itself in such a way that the surface traps are filled in accordance with Eq. (3-4) and over-all charge neutrality exists.

Taking into account the effects of surface state trapping phenomena the pinch-off voltage, previously given by Eq. (2-3), can now be written as

$$V_p = - Q_b / C_o - Q_{ss} / C_o + \phi_{ms} + \phi_{so} - Q_t / C_o \qquad (3\text{-}5)$$

The slow surface states are represented by Q_{ss}/C_o and are temperature independent. Q_t/C_o represents the fast surface states and is given by

$$Q_t / C_o = - q/C_o \int^{E_{gap}} n_t(E)\, dE \qquad (3\text{-}6)$$

where: $n_t(E) = f(E)\, N_t(E)$ is the fraction of available trap sites occupied by electrons under steady state conditions.

The complexity of Eq. (3-6) can be reduced if it assumed that all traps below the Fermi level are completely filled and all traps above are completely empty [9]. The total charge trapped in the interface states is then represented by an energy integral of $N_t(E)$ up to the Fermi level.

$$Q_t / C_o = - q/C_o \int_{E_v}^{E_f} N_t(E)\, dE \qquad (3\text{-}7)$$

Equation (3-7) states that Q_t/C_o will be dependent on both the position of the Fermi level with respect to $N_t(E)$ and to the density of chargeable interface states in the energy region under consideration as is illustrated in Fig. 3.3.

It is necessary to digress for a moment upon the definition of the pinch-off voltage before an explanation of Fig. 3-3 can be given. When it was assumed that no trapping of the channel carriers occured the pinch-off voltage was defined as the gate voltageat which the beginning of conduction was possible.

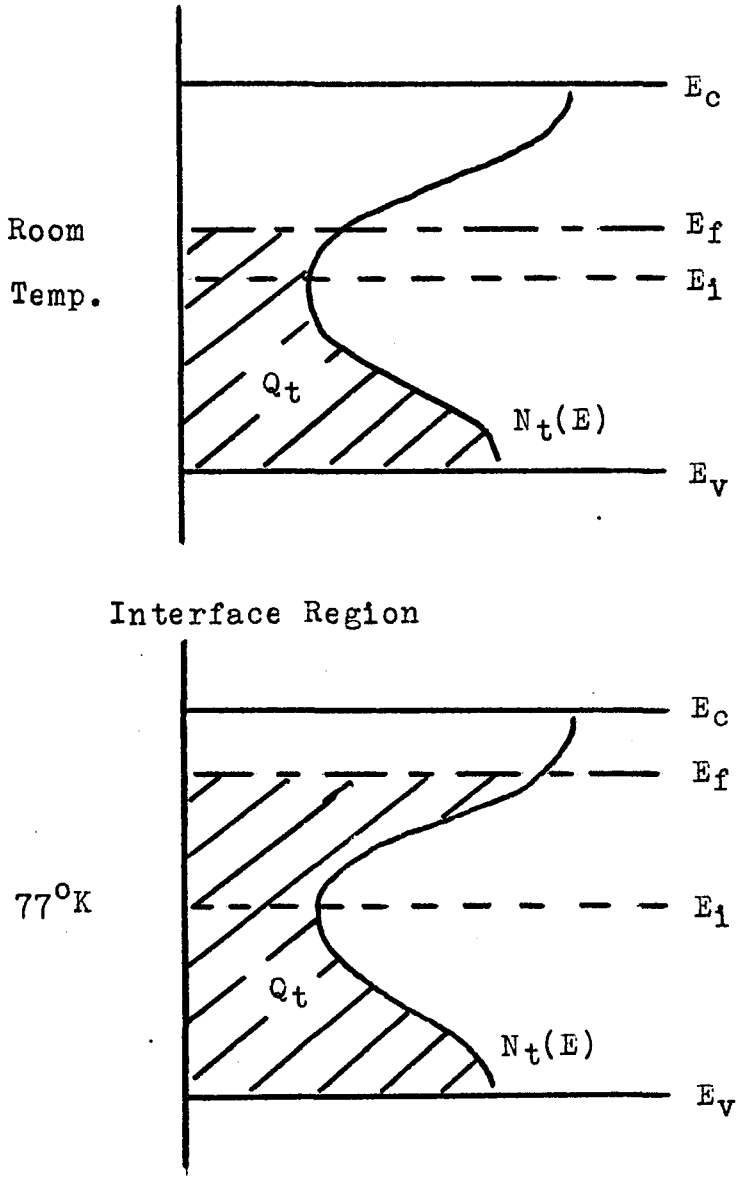


Fig. 3.3 The Temperature Dependence of Q_t

($V_g = V_p$)

However, with the trapping of minority carriers now being a possibility the gate voltage must be large enough to allow the traps to be filled in accordance with Eq. (3-7) before conduction between drain and source can occur. This additional gate potential which is required is represented by Q_t/C_o. The pinch-off voltage may be determined in the same manner as before, although, empirically it may be more convienient to define or determine the pinch-off voltage at a specific drain current level.

Returning to Fig. 3.3 the effects of trapping phenomena upon the pinch-off voltage should now be evident. At room temperature the density of trapped electrons in the interface states is small and the contribution of Q_t/C_o to the pinch-off voltage is insignificant. When the temperature is decreased the Fermi level at the surface moves closer to the conduction band in order to maintain the pinch-off condition. As it does so more and more electrons are trapped in the interface states and eventually the term Q_t/C_o becomes significant.

Equation (3-5) may be regrouped as follows

$$V_p = \phi_{ms} + \phi_{so} - \frac{Q_{ss}}{C_o} - \left(\frac{Q_b + Q_t}{C_o} \right) \qquad (3\text{-}8)$$

where: Q_{ss} = the total positive charge

$Q_b + Q_t$ = the total negative charge

Equation (3-8) states that an increase in Q_t (achieved by decreasing the temperature) has the same effect on the pinch-off voltage as does an increase in Q_b (achieved by a heavier doping of the substrate). Take for example an n channel MOS FET, which at room temperature, has the physical characteristics found at point "A" on Fig. 3.4. Q_t/q may approach and possibly exceed the value of Q_b/q thereby shifting point "A" to the right along the curve of constant Q_{ss}/q as the temperature is decreased. The rate of movement along this curve with temperature is entirely determined by Eq. (3-7).

Nathanson [13] and Heiman and Miller [9] have carried out the integration of Eq. (3-7) assuming the interface state density, $N_t(E)$, to be constant with energy across the bandgap. The temperature dependence of the pinch-off voltage strictly due to trapping phenomena is

$$\frac{dV_p}{dT} = \frac{q}{C_o} N_t \frac{d\phi_s}{dT}\bigg|_{I_d} \qquad (3\text{-}9)$$

where: V_p is defined at a specific current.

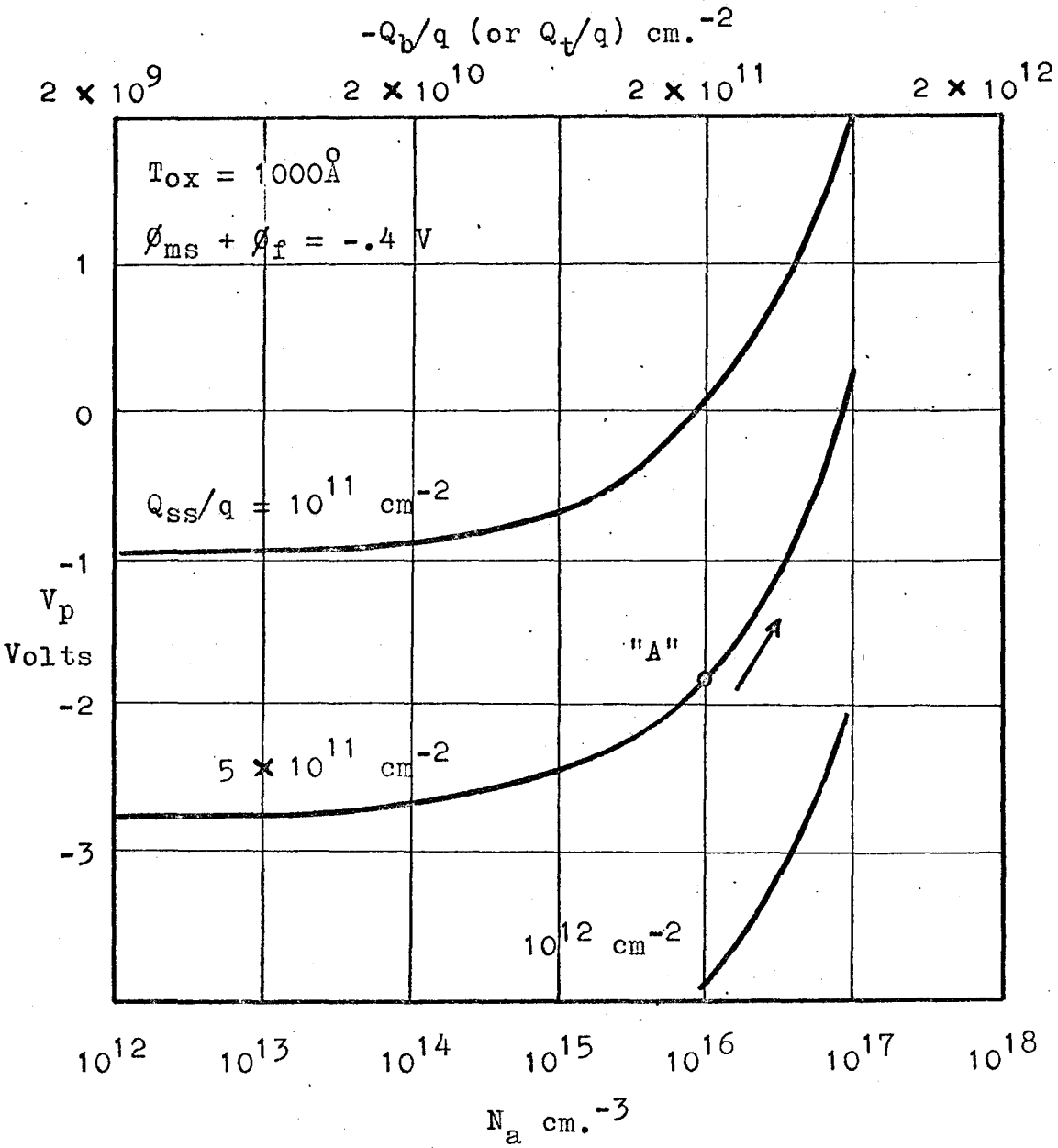


Fig. 3.4 The Effect of Increasing Q_t/q Upon the Pinch-off Voltage

$\frac{d\phi_s}{dT}$ = the change in surface potential required to maintain a constant drain current level for a temperature change of dT.

In the temperature region above 77°K Heiman and Miller have calculated a required interface state density of 2×10^{13} cm.$^{-2}$ ev.$^{-1}$ for a pinch-off voltage temperature dependence of -40mV/°K to -60mV/°K. Nathanson, by the use of degenerate statistics, has calculated an interface state density of 3×10^{15} cm.$^{-2}$ ev.$^{-1}$ for a temperature dependence of -360mv/°K at 3°K. Interface state densities exceeding 10^{13} cm.$^{-2}$ ev.$^{-1}$ have been found near the conduction band edge by P. Gray and D. Brown [17]. The large values obtained for N_t could be reduced considerably through the use of more exacting calculations. However, the preceding simplified model will suffice to explain the observed experimental results.

3.3 The Transconductance

The forward transconductance is the key dynamic characteristic of MOS FETs. It serves as a basic design parameter in audio and radio frequency circuits and is a widely accepted device figure of merit.

The following equations were obtained for the transconductance in Chapter 2.2.2.

$$g_m = \left.\frac{\partial I_d}{\partial V_g}\right|_{V_d} = \frac{u_n C_o}{L^2} V_d \qquad (3\text{-}11)$$

The maximum which occurs at saturation is given by

$$g_{ms} = \frac{u_n C_o}{L^2} V_{ds} = \frac{u_n C_o}{L^2} (V_g - V_p) \qquad (3\text{-}12)$$

The temperature dependent terms, namely u_n and V_p, have already been discussed in Chapter 3.2. Qualitatively the magnitude of the transconductance, for fixed values of V_d and V_g, is expected to vary directly with u_n as the temperature is increased or decreased. In addition, for fixed V_d, the transconductance versus gate voltage characteristics will shift with the pinch-off voltage as the temperature is varied.

3.4 1/f Noise

In Chapter 2.3 it was shown that the origin of low frequency noise in MOS FETs is the capture and emission of carriers by traps located at the silicon, silicon oxide interface and in the oxide. The fundamental

expression developed for the noise voltage is repeated below.

$$\frac{v_n^2}{B} = N_t \frac{4q^2}{C_o^2 ZL} 0.25 \frac{\pi}{2\alpha\omega} \qquad (3\text{-}13)$$

where: $$N_t \approx \frac{N_t(E)}{d_t} \frac{4kT}{q}$$

The noise is strongly dependent upon the trap distribution over energy and over space. For a continuous trap distribution the trap energy range effective in noise generation also changes with temperature as it is proportional to kT. The temperature dependence may therefore show "anomalies" as both the trap distribution and the effective energy range may vary in different proportions. A detailed prediction of the magnitude of the noise voltage at different operating points is thus very difficult to make. The largest noise voltage is obtained at a temperature such that the Fermi level resides in energy regions where the trap density is high and the effective energy range, 4kT, is large.

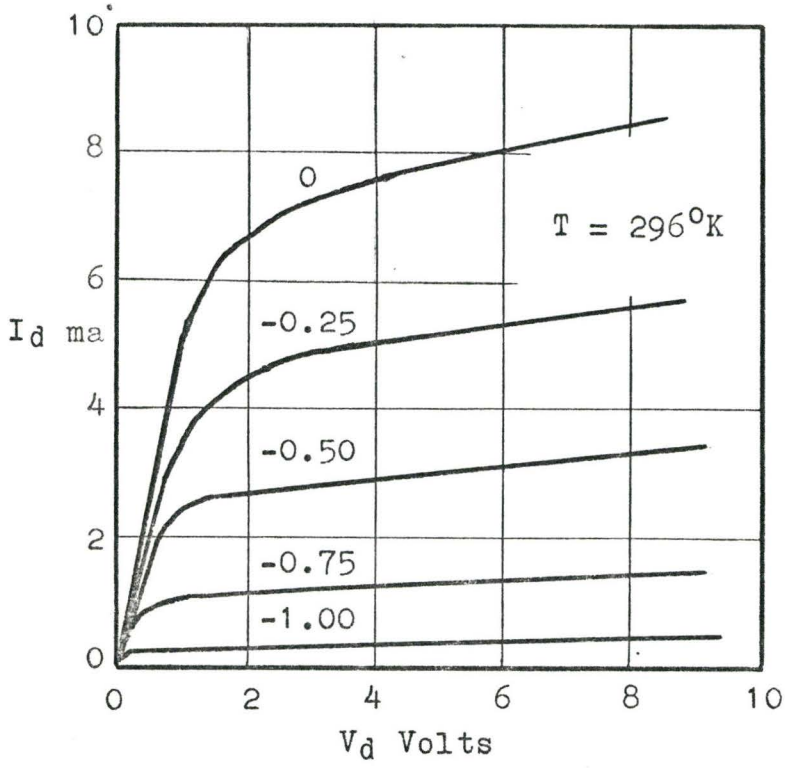
CHAPTER IV

Experimental Results

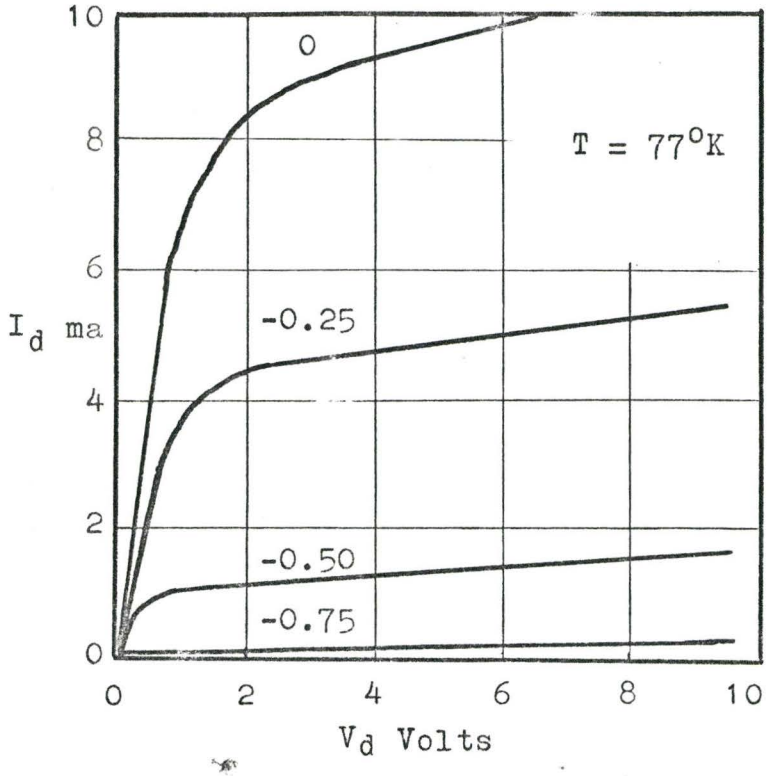
4.1 General Considerations

Before undertaking a detailed examination of particular characteristics such as transconductance and 1/f noise the current-voltage characteristics of the RCA 3N128 n channel MOS FET were analysed. The characteristics are shown for room temperature in Fig. 4.1a, for the temperature of liquid nitrogen in Fig. 4.1b, and for the temperature of liquid helium in Fig. 4.1c. It is concluded from Fig. 4.1c that the MOS FET was incapable of functioning normally at the temperature of liquid helium.

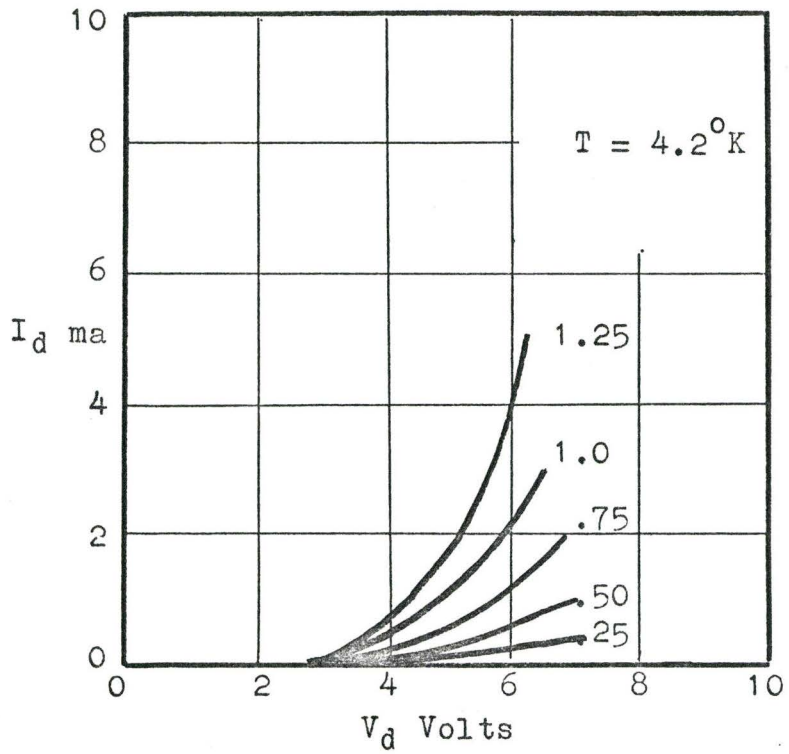
C. Rogers and A. Jonscher [3] have also observed behaviour similar to that shown in Fig. 4.1c for MOS FETs. These characteristics occur if the gate does not overlap both the source and drain regions. Only the area directly beneath the gate may be inverted by an applied potential while the remaining area remains "frozen out". The induced channel under the gate is


10
8
6
4
2
0
I_d ma
0
-0.25
-0.50
-0.75
-1.00
T = 296°K
0
2
4
6
8
10
V_d Volts

(a)


10
8
6
4
2
0
I_d ma
0
-0.25
-0.50
-0.75
T = 77°K
0
2
4
6
8
10
V_d Volts

(b)



(c)

Fig. 4.1 I_d - V_d Characteristics

then isolated from the drain and source regions by very high resistance regions and a conducting channel may not even be formed from drain to source. A high drain voltage is then required before current will flow. Rogers and Jonscher found that if the gate overlapped both the drain and source it was always possible to form a surface channel by enhancement-mode operation even though the substrate was initially "frozen out".

4.2 The Channel Conductance

4.2.1 Introduction

Conductance measurements were taken for several RCA 3N128 n channel MOS FETs to obtain the experimental temperature dependence. Using the circuit of Fig. 4.2, measurements of drain current I_d were taken versus the gate voltage V_g at various temperatures and at a constant drain voltage of .01 volts.

Fixed temperatures were obtained by use of a Delta Design Temperature Chamber or a variable temperature liquid helium cryostat. Both systems are described in Appendix A. Above 77°K the temperature was measured with a copper-constantan thermocouple. Below 77°K a calibrated Allen-Bradley 1/10 watt 270 ohm resistor was used [18].

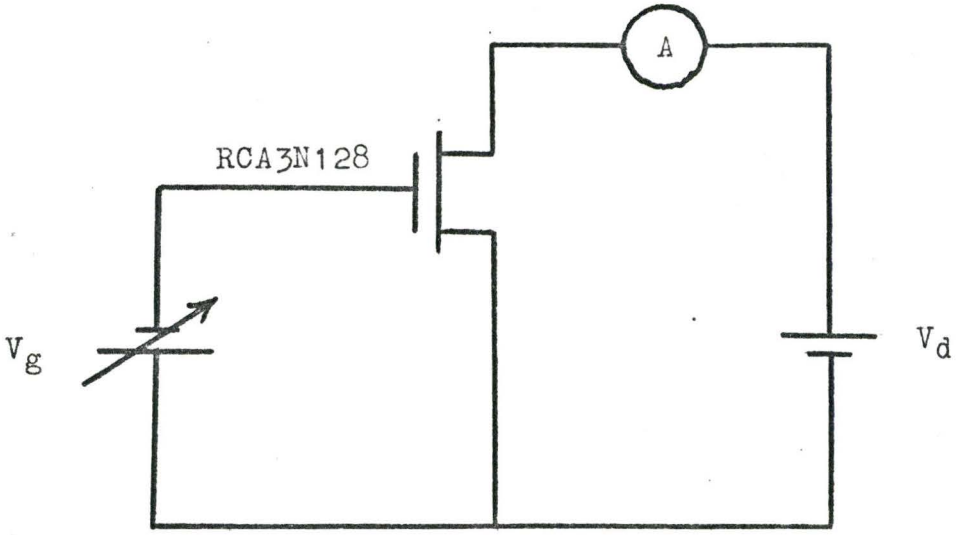


Fig. 4.2 Circuit for Measuring Channel Conductance

4.2.2 Experimental Results and Discussion

In Fig. 4.3 the channel conductance is represented as a function of the applied gate voltage. The drain voltage used was 0.01 volts to ensure that the measurements were taken in a region were the mobility was independent of the drain to source voltage.

From Fig. 4.3 it is seen that once conduction has begun there is always a certain region over which the increase in conductance has a linear dependence on the gate voltage. In this region the mobility is therefore independent of gate voltage. Figure 4.4 is a plot of the conductivity mobility obtained from the slope of the g_d versus V_g curves (see Eq. (3-1)). Results obtained by F. Fang and A. Fowler [19] for the temperature dependence of the effective mobility at a gate voltage of 1 volt above the pinch-off condition are similar in behaviour.

The pinch-off voltage was obtained by extrapolation of the linear portion of the conductance curves to the $g_d = 0$ axis. V_p is plotted as a function of temperature in Fig. 4.5. Above $77^{\circ}K$ the behaviour of the pinch-off voltage with temperature is in agreement with the

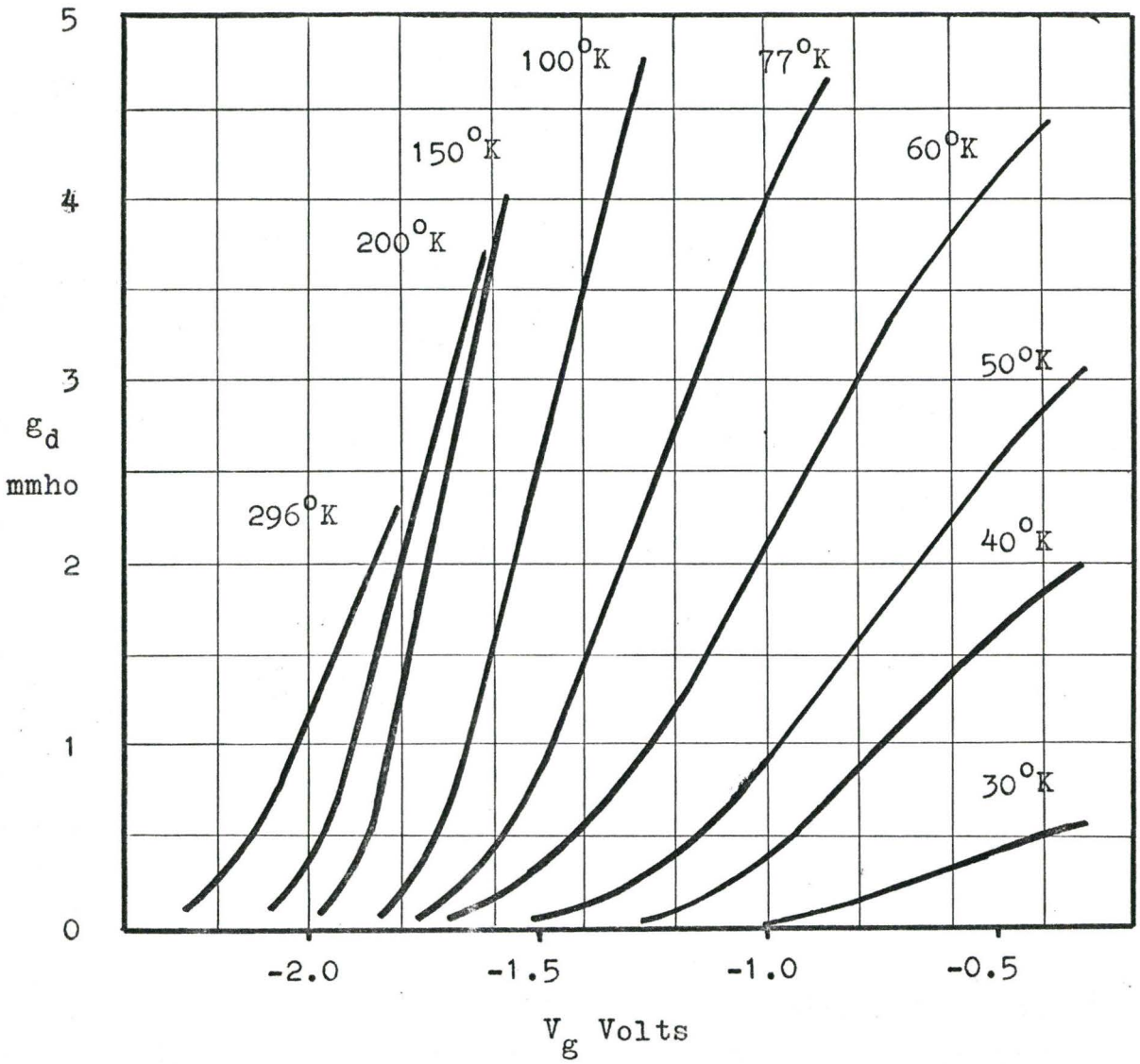


Fig. 4.3 The Temperature Dependence of the Channel Conductance

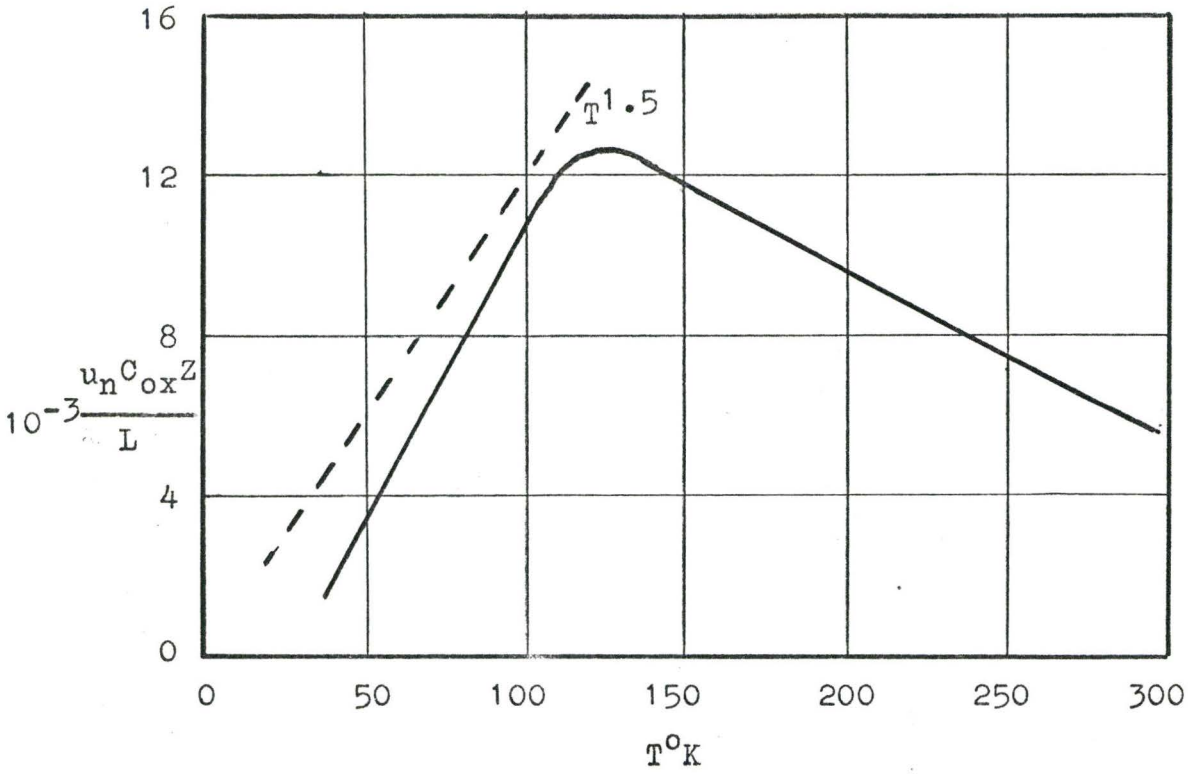


Fig. 4.4 The Temperature Dependence of the Conductivity Mobility

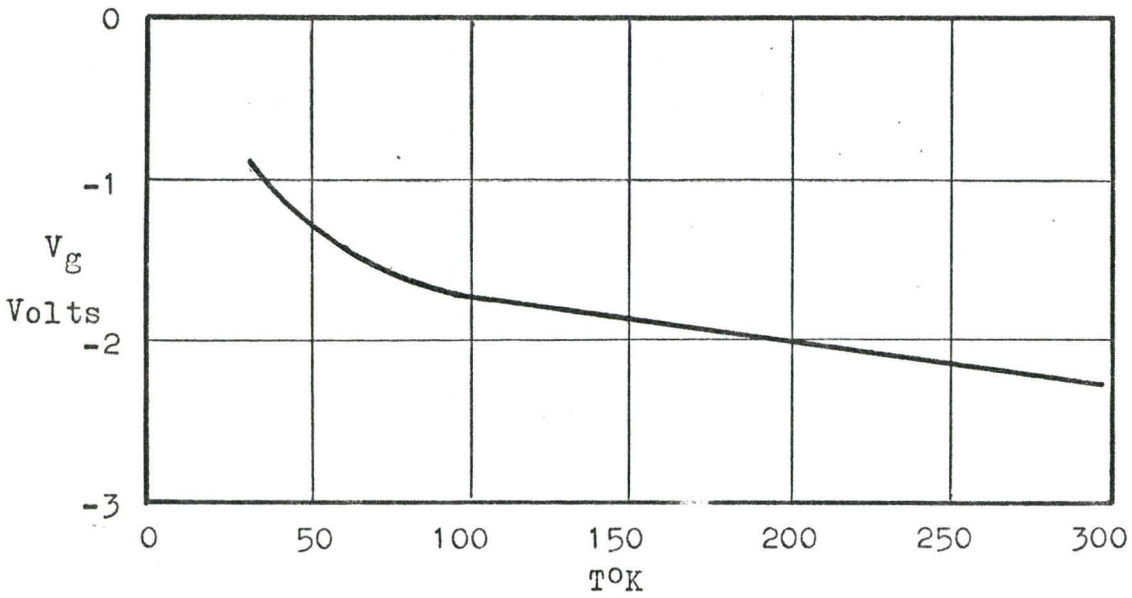


Fig. 4.5 Pinch-off Voltage vs. Temperature

theoretical predictions of Chapter 3.1. However, below 77°K the pinch-off voltage exhibits a much stronger temperature dependence then the theory predicted.

Similar results have been obtained by Nathanson[13] and Roger[20]. Both suggest this large temperature dependence below 77°K is caused by trapping phenomena. Nathanson, however, argues that the interpretation of these low temperature results in terms of an arbitrary density, fixed-energy interface state model, as done in Chapter 3.4, is inconsistent quantitatively with experimental results. His argument is based on the fact that no evidence is found for the effects of these states on d.c. conductance measurements. G. Abowitz et al[21], on the otherhand, have used d.c. channel conductance measurements to quantitatively evaluate the interface state density.

Fang and Fowler[19] suggest the pinch-off voltage does not change appreciably in this temperature range. The results of their Hall measurements demonstrate the apparent shift in pinch-off voltage is caused primarily by what seems to be a sharp decrease in mobility. It is thus apparent that more work must be carried out before any general conclusions can be made and verified.

4.3 The Forward Transconductance

Forward transconductance measurements were taken with the circuit setup of Fig. 4.6. A small signal frequency of 0.01 V rms at 1 kHz was used to plot the characteristics. The transconductance versus gate voltage characteristics at room temperature and the temperature of liquid nitrogen are shown in Fig. 4.7. Figure 4.8 portrays the dependence of the transconductance on temperature at a constant drain to source voltage of 3 volts.

The gradual shift of the curves from left to right is caused by the temperature dependence of the pinch-off voltage. The increase in the transconductance with decreasing temperature is caused by the increase in the mobility. This mobility, because of the drain to source and gate voltages used, is field dependent and therefore cannot be compared with the mobility evaluated in Chapter 4.2.

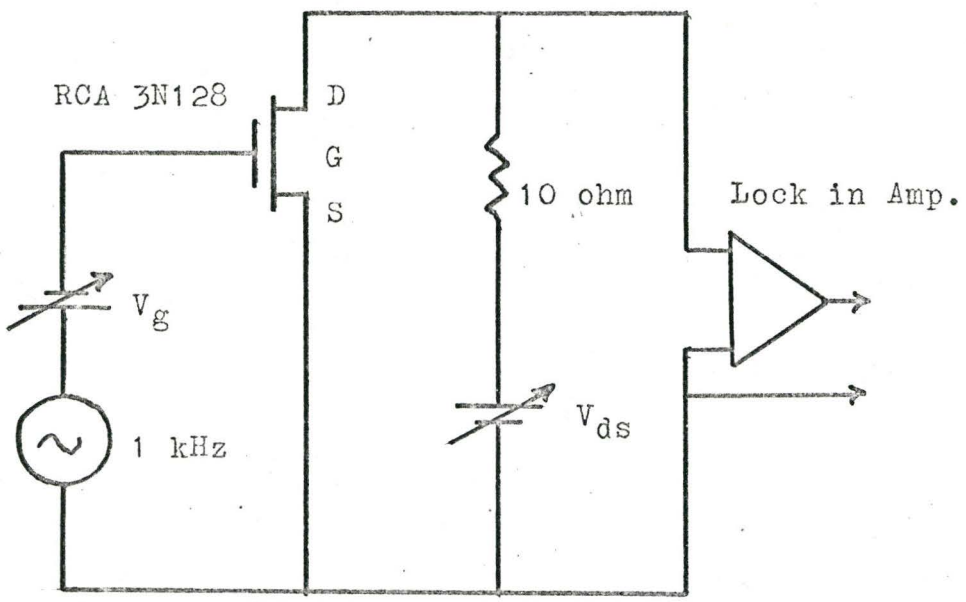


Fig. 4.6 Circuit Arrangement for the Transconductance Measurements

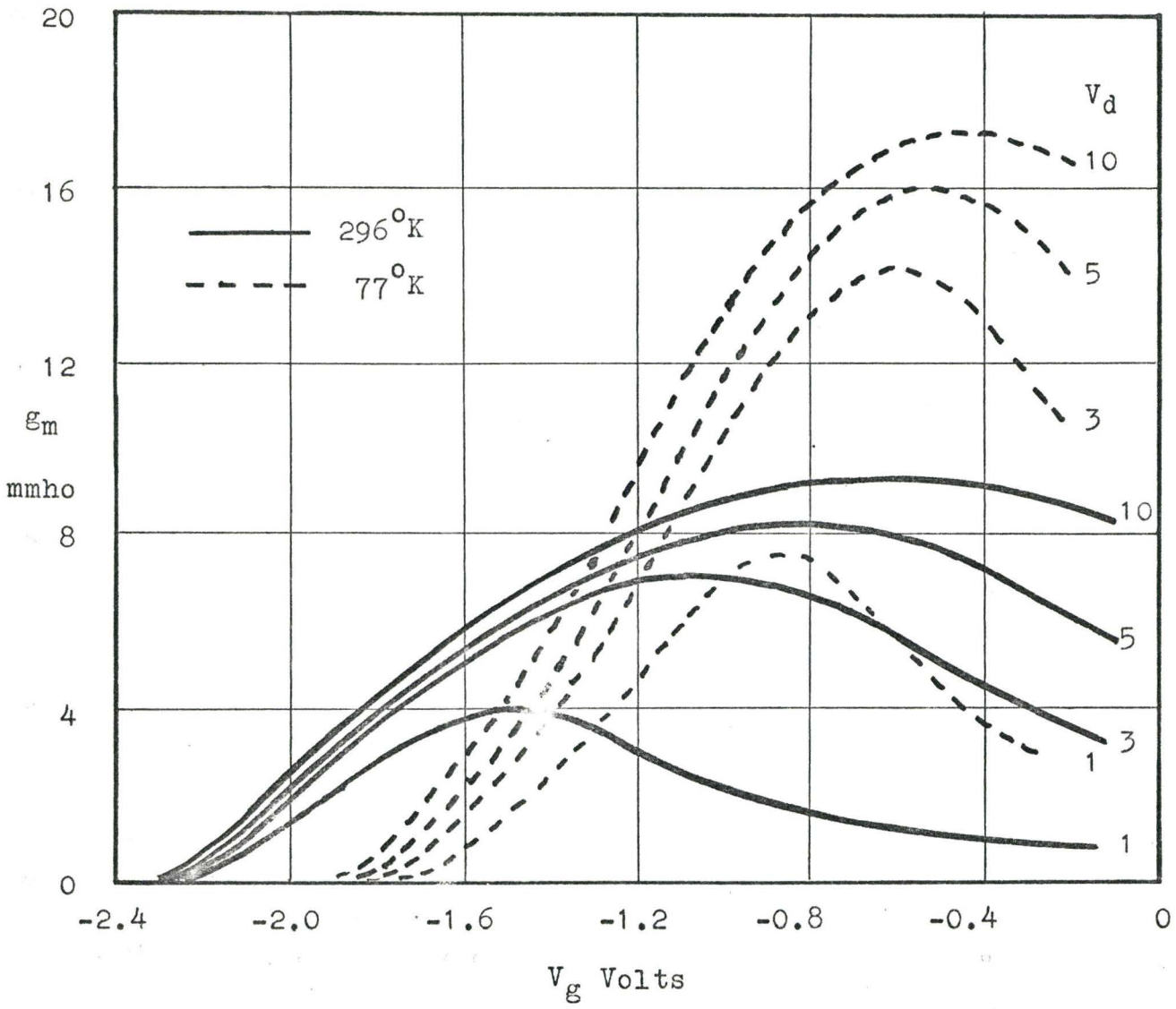


Fig. 4.7 Transconductance vs. Gate Voltage

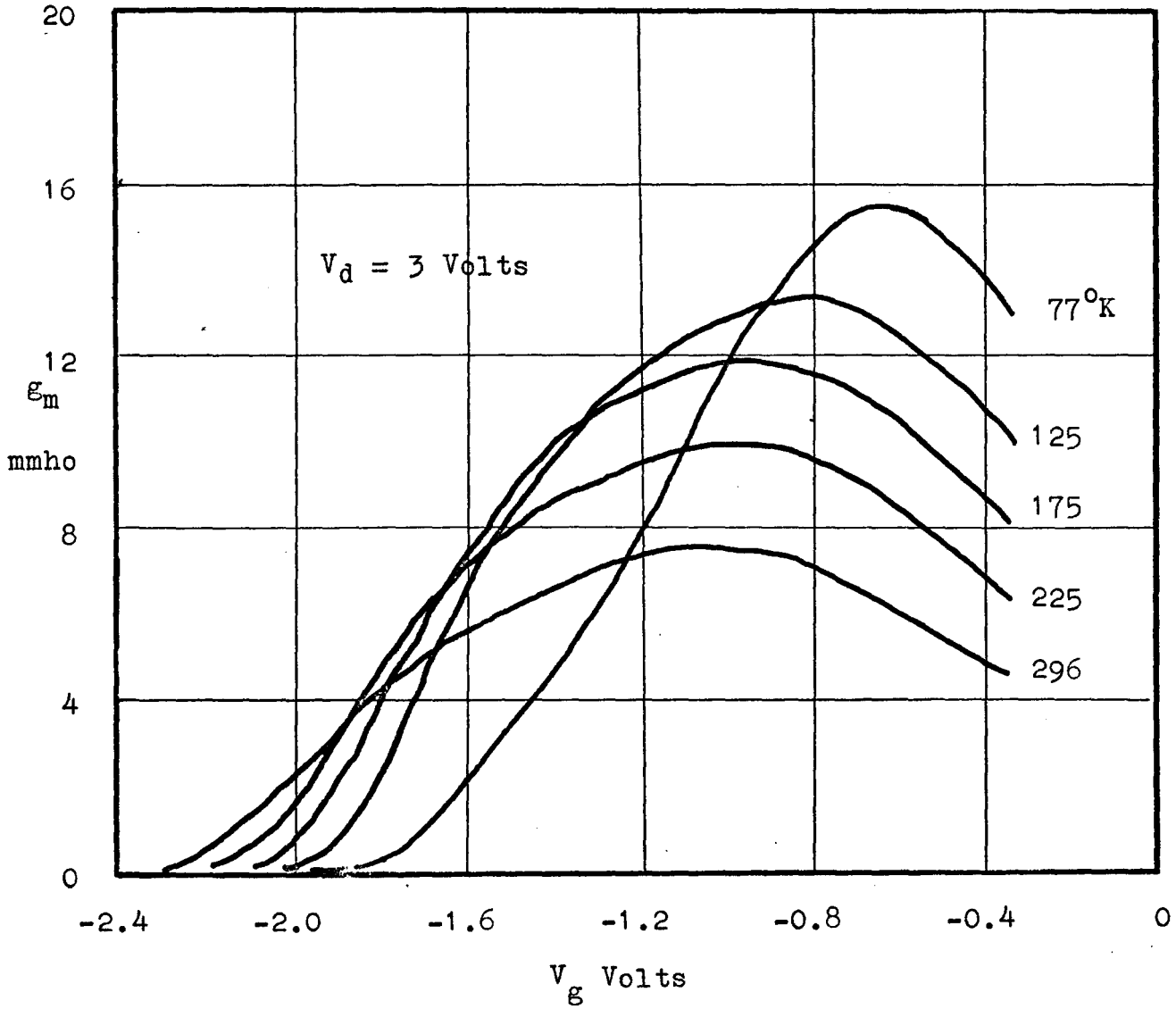


Fig. 4.8 Transconductance vs. Gate Voltage

4.4 1/f Noise

4.4.1 Introduction

Measurements were performed on several RCA 3N128 n channel MOS FETs to obtain the dependence of 1/f noise on temperature and operating point. The measurements were restricted to the low frequency region for the following reasons.

(a) The equivalent input noise voltage, e_n, is sufficient to characterize the noise performance of the device in the low frequency region.

(b) The upper frequency limit was restricted by the capacitance of the leads required to place the device in the temperature chamber.

A block diagram of the equipment used to perform the noise measurements is given in Fig. 4.9. A more detailed diagram of the transistor test jig is shown in Fig. 4.10. Preliminary measurements carried out on the noise measuring equipment are included in Appendix B along with the method of noise measurement. For all measurements taken the background noise was sufficiently below the equivalent input noise voltage of the device.

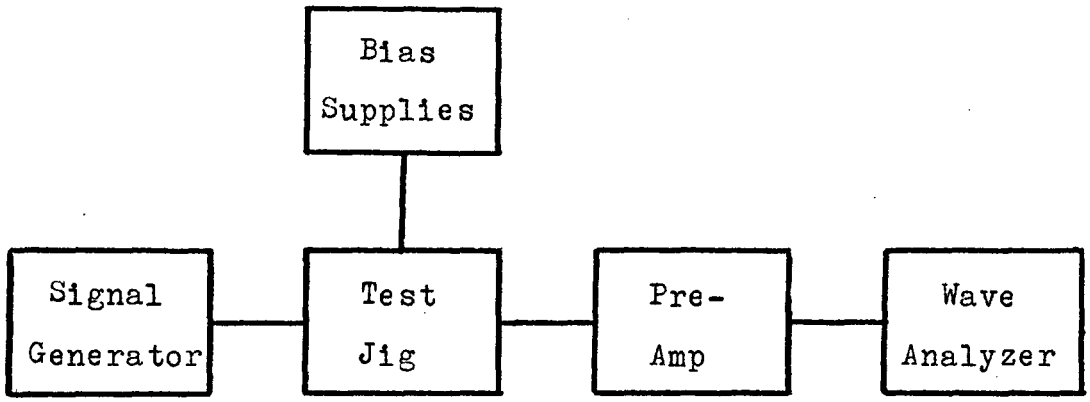


Fig. 4.9 Block Diagram of the Noise Measuring Equipment

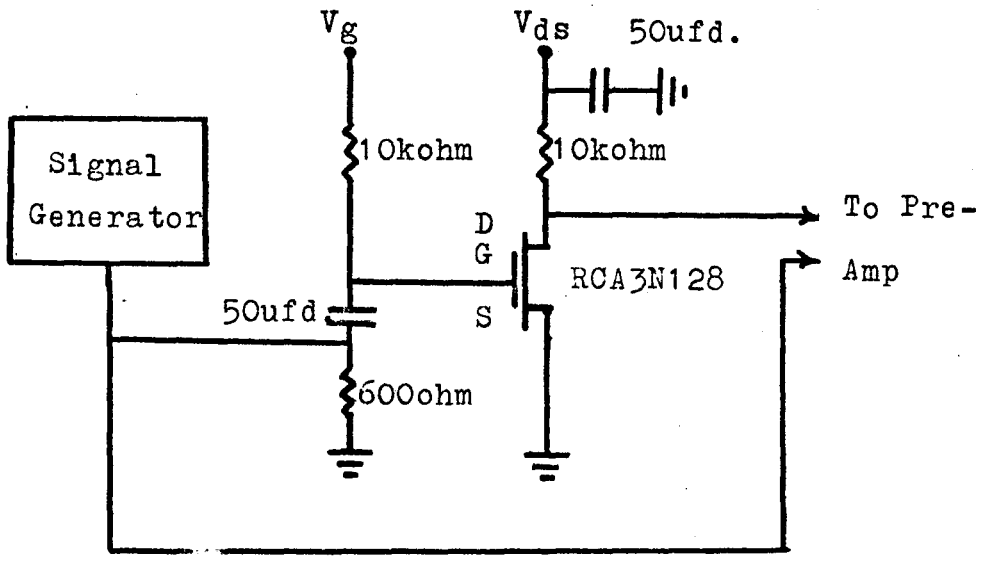


Fig. 4.10 Transistor Test Jig

4.4.2 Experimental Results

It was previously stated in Chapter 3.4 that e_n is a function of d.c. operating point, frequency, and temperature. e_n was measured for a variety of d.c. operating conditions as shown in Fig. 4.11. This allowed the selection of an operating point which assured a reasonable voltage gain from the device for the following noise measurements.

The noise spectra for a RCA 3N128 n channel MOS FET at two distinct temperatures, namely 77°K and 296°K, are shown in Fig. 4.12. The noise spectrum at room temperature shows a breaking point at about 20kHz. Below 20kHz. it roughly follows a 1/f curve. At a temperature of 77°K the noise voltage has increased and the complete spectrum exhibits a 1/f dependence.

The temperature dependence of the noise voltage at several frequencies, namely 10^2, 10^3, and 10^5 Hz., is shown in Fig. 4.13. It is seen, that as the temperature is decreased, the noise at all frequencies continues to increase until a temperature of 200°K is obtained. Below this temperature the noise for the higher frequencies decreases while for the lower frequencies it continues

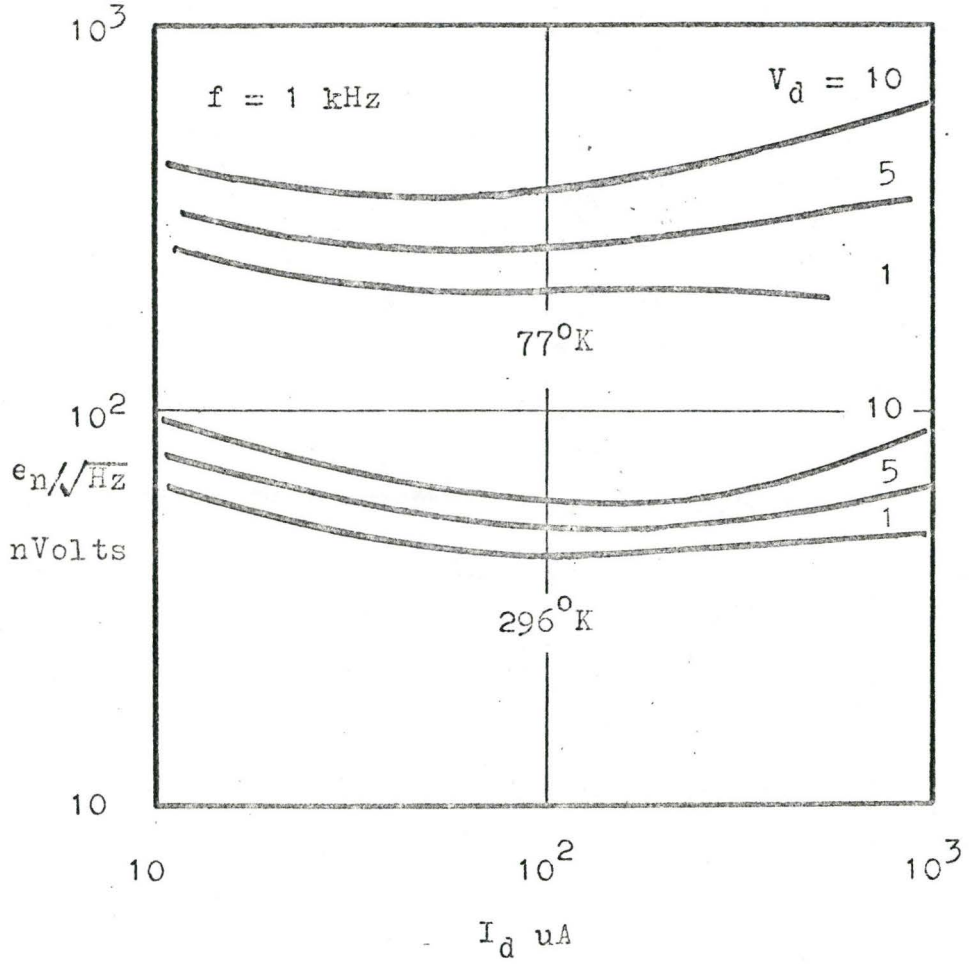


Fig. 4.11 The Dependence of e_n on the D. C. Operating Point

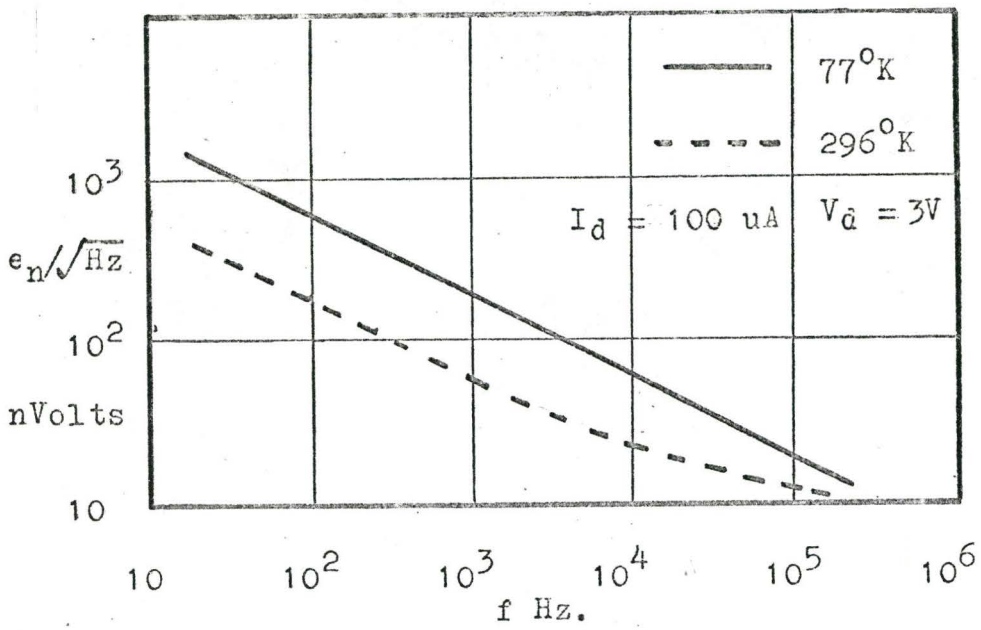


Fig. 4.12 The MOS FET Noise Spectra

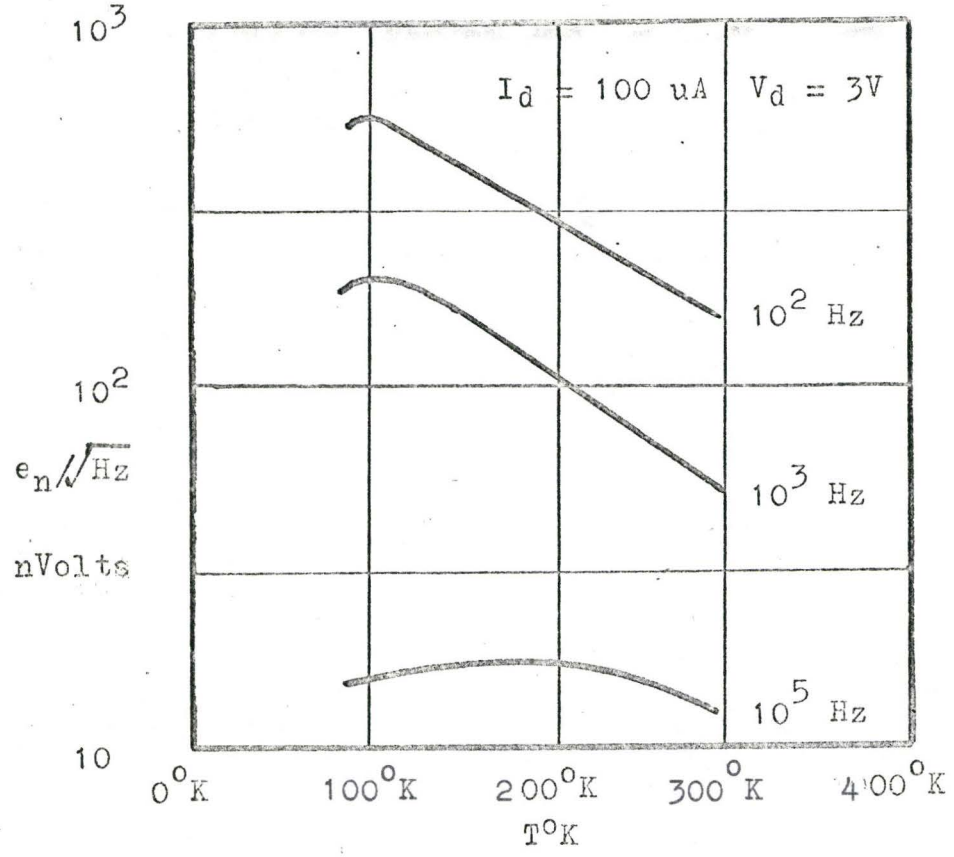


Fig. 4.13 Temperature Dependence of e_n

to increase. Below 100°K the noise voltage at the lower frequencies also begins to decrease.

4.3.3 Discussion of Experimental Results

a) The Dependence of e_n on Drain to Source Voltage

In Fig. 4.11 it is seen that the noise voltage increases with increasing drain to source voltage. One reason for this is a decrease in the channel length, L, is caused by the widening of the depleted region at the drain contact. The decrease in channel length increases the equivalent input noise voltage (see Eq. (3-12)). This increase may also be caused by the movement of the electron Quasi Fermi level, in the vicinity of the drain contact, into a region of increasing interface state density.

b) The Dependence of e_n on Gate Voltage

The magnitude of the noise voltage varies with the gate voltage because it determines the position of the Fermi level at the interface and therefore the trap levels most effective in noise generation. For a continuous trap distribution over energy the magnitude of the noise voltage follows the trap density at the Fermi level determined by the gate voltage. For discrete

trap levels the magnitude of the noise voltage is mainly determined by the electron density at the interface and by the relative position of trap level and Fermi level and thus by the gate voltage.

c) The Dependence of e_n on Temperature

Many of the statements in (b) of this section also apply for case (c). A change in temperature corresponds to a change in the position of the Fermi level at the interface if the same drain current is to be maintained. In calculating such a change one must remember that the mobility also changes with temperature. For a continuous trap distribution the trap energy range effective in noise generationalso changes with temperature because it is proportional to kT. The temperature dependence may therefore show anomalies depending on the trap distribution.

CHAPTER V

Conclusions and Discussion

The RCA 3N128 n channel MOS FET was found capable of operating at temperatures below that of liquid nitrogen. The "freeze out" of the parasitic resistance regions at the drain and source electrodes prevented operation of the device down to the temperature of liquid helium. To alleviate the problem of "freeze out" it would be necessary to manufacture a device in which the gate electrode extended over the entire length of the channel. Unfortunately, with present day manufacturing techniques, it is almost impossible to do so without the risk of of obtaining considerable gate overlap of the drain and source regions (such results are not desirable because the upper frequency limit of the device is lowered by gate overlap). With the advent of ion implantation[22] precision control of the drain and source placement is possible. Devices capable of operating at the temperature of liquid helium can thus be manufactured without risk of degrading other desirable characteristics.

Small signal measurements on the device found the temperature dependence of the parameters g_d and g_m attributable to the pinch-off voltage and channel carrier mobility temperature dependence. Two distinct regions of interest were examined. In the first region, $T > 77^{o}K$, dV_p/dT was practically constant for all of the examined MOS FETs. This behaviour was accounted for by the generally excepted theory which predicts that as the temperature is lowered dV_p/dT is consistent with the almost linear movement of the surface Fermi level towards the conduction band edge. In the second region, $T < 77^{o}K$, marked deviations from linearity were noted in dV_p/dT. To explain this behaviour it was necessary to postulate a model in which trapping of electrons by the interface states formed a negative charge sheet near the silicon, silicon oxide boundary. The transition from the first region to the second occured when the trapped charge density, Q_t/q per unit area exceeded the depletion region charge, Q_b/q per unit area (similar results occur if Q_t/q approaches Q_{ss}/q per unit area). Differences of opinion still exist as to whether or not the temperature dependence of the pinch-off voltage can be explained in this manner. It has even been suggested that this second

region of behaviouf does not exist and that only a sharp decrease in mobility occurs.

The tunneling model, like other models including trapping processes gives rise to a hysteresis in the capacitance voltage curve[8]. Attempts to measure this hysteresis (see Appendix C) proved unsuccessful since repeatable results could not be obtained. A MOS FET with larger gate to source capacitance would be required in order to obtain more useful results.

The detailed behaviour of the low frequency noise was found to be very complex. The theory, after Christensson et al[8], pointed out that the origin of the low frequency noise in MOS FETs may be the capture and emission of carriers by traps located at the silicon, silicon-oxide interface and in the oxide. The trap distribution can give rise to peculiar performance of the noise voltage with gate voltage, drain voltage, and temperature. Without a knowledge of the actual trap distribution over energy and space a detailed prediction of the noise voltage at different operating voltages and temperature would be very difficult to make.

This investigation has found the RCA 3N128 n-channel MOS FET capable of operating to temperatures below that of liquid nitrogen. The only detrimental feature would be the increase of the low frequency input noise voltage (noise measurements on p channel MOS FETs have shown a decrease in the low frequency noise as the temperature is lowered[8]). It has also been shown that further studies are required in order to completely understand the interesting low temperature behaviour of the pinch-off voltage.

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APPENDIX A

Low Temperature Facilities

(1) Delta Design Temperature Chamber

For all experimentation performed in the temperature range above 77°K a Delta Design MK2300 temperature chamber was used. The coolant used was liquid nitrogen. A sketch of the temperature chamber is shown in Fig. 1.

The calibration of the temperature set dial was checked by use of a copper-constantan thermocouple to detect any nonlinearities. The results are shown in Fig. 2.

(2) Liquid Helium Cryostat

The construction of a liquid helium cryostat was a joint venture between the Department of Electrical Engineering (Dr. Chisholm) and the department of Engineering Physics (Dr. Shewchun) for the purpose of materials research.

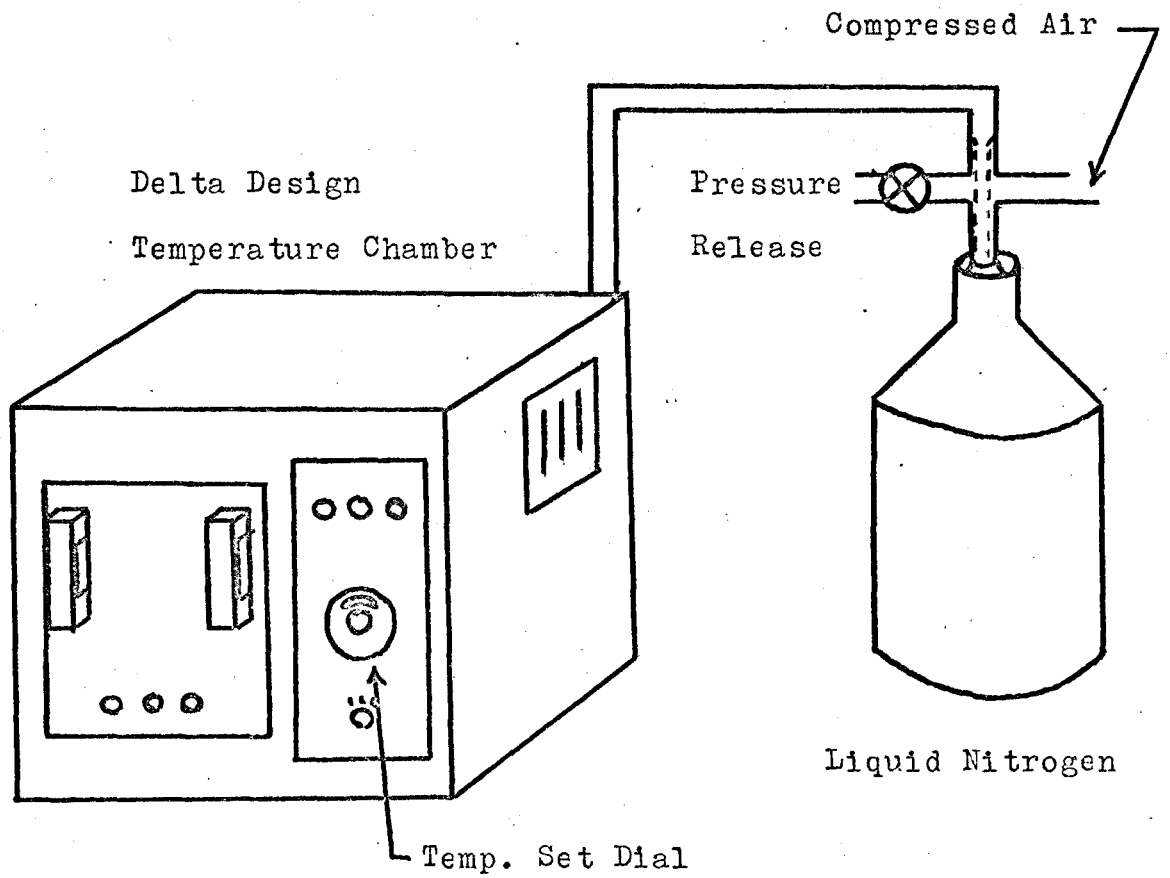

Fig. 1 Temperature Facilities $77^{\circ}K < T < 300^{\circ}K$

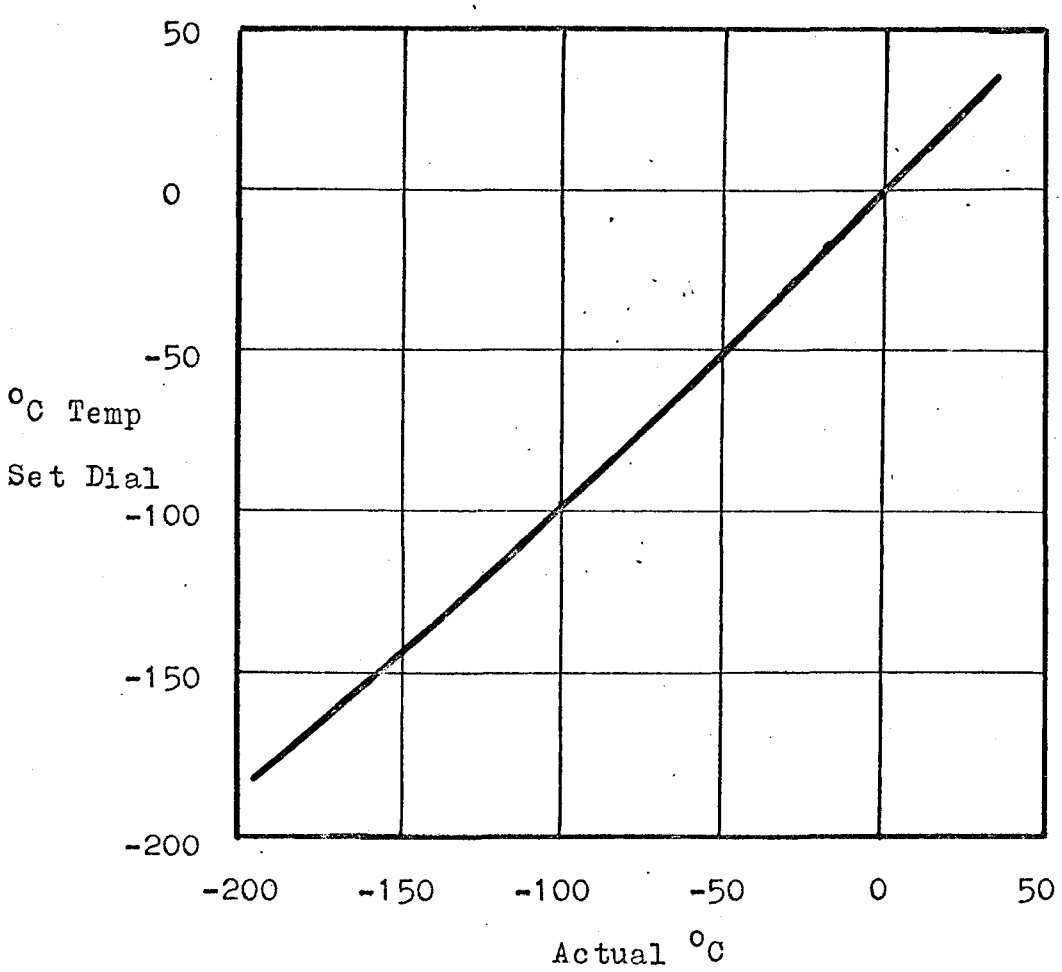

Fig. 2 Calibration Check of the Delta Design Temperature Chamber

A qualitative description of the proportional temperature controller fabricated for the above system is given below.

(a) General Description

The system is a closed loop controller which utilizes a precision a.c. bridge circuit for measurement of the difference in resistance between the rheostat temperature setting and the actual temperature of the cryostat as indicated by the calibrated temperature sensor. This difference in resistance (i.e. temperature of the chamber) is amplified by a narrow band low noise amplifier, phase detected and amplified again to drive a heater.

Fully automatic control can be provided by the system. A single "Set Temperature" control dial is set to the resistance which corresponds to the required temperature. The proportional control feature of the instrument provides precision temperature regulation and prevents large thermal oscillations.

Solid state circuitry in modular design, Fig. 3, is used throughout. These consist of an oscillator,

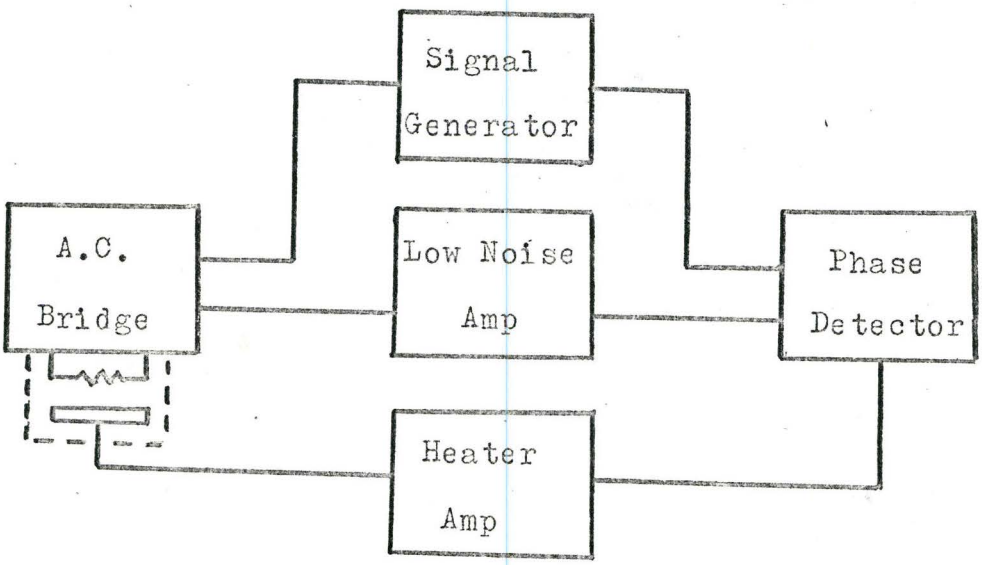

Fig. 3 Block Diagram of the Proportional Temperature Controller

bridge, low noise amplifier, phase detector and heater drive. A meter is provided to indicate the operating mode such as "Heating", or "Cooling".

(b) Detailed Description

The first circuit to be discussed is the phase shift oscillator shown in Fig. 4. The circuit oscillates at the frequency where the phase shift through the R-C network (R_1, C_1, R_2, and C_2) is zero, as long as the positive feedback is equal to or greater than the negative feedback. An AGC is used to hold the gain at the precise value required. For the component values shown the frequency of oscillation is 1 kHz. and the output voltage is 8 volts peak to peak.

The phase detector shown in Fig. 5 is unique in that it is transformerless. The input switch Q_1 and Q_2 alternately switches the amplifier from an inverting configuration to a noninverting configuration. The push-pull drive signal for this switch is obtained by applying the controlling oscillator signal to the analogue to digital converter. The out-of-balance signal from the bridge, being either in phase or 180° out of phase with the controlling oscillator, gives

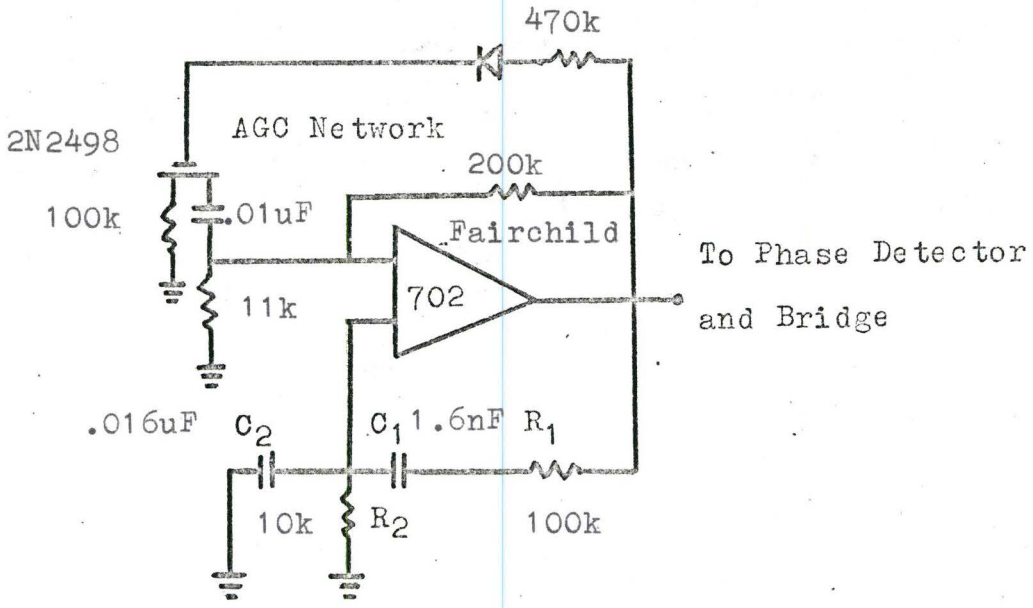

Fig. 4 1 kHz Sine-Wave Oscillator

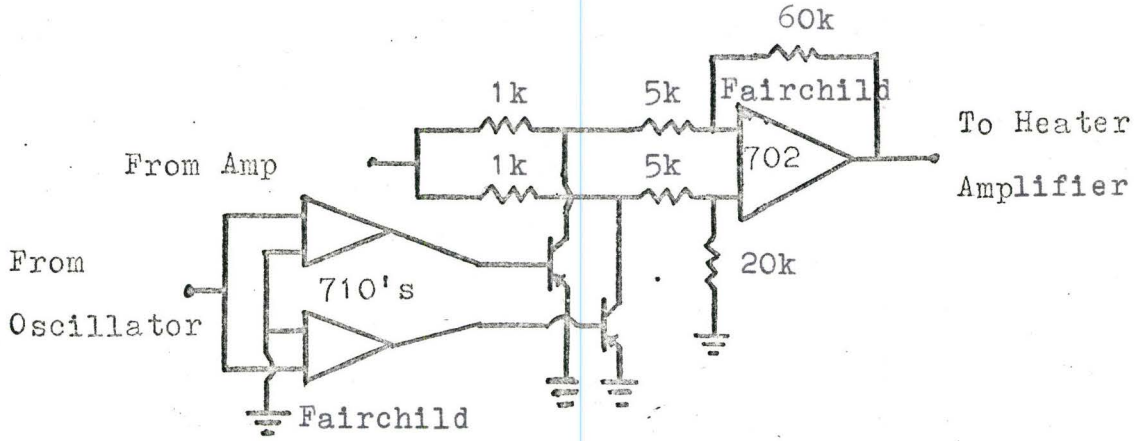

Fig. 5 Phase Detector

one of two outputs from the phase detector as shown in Fig. 6.

The a.c. bridge circuit is shown in Fig. 7. One arm consists of a 1/10 watt carbon resistor mounted in the cryostat. Its value is chosen such that its resistance is in the range 0 to 10 Kohms when at the desired operating temperature. The desired temperature is set by the decade rheostat. A constant voltage source from the oscillator is used to drive the bridge. To minimize heating of the sensor the power level is kept below 1 microwatt.

The low noise amplifier consists of two sections. The first is simply a high gain low noise stage. The second contains a twin T network in the feedback loop to give a passband of 20 Hz. at the 3 db. points. A voltage gain of 10^5 at 1kHz. is obtainable. The equivalent input noise voltage is less than 1 microvolt. See Fig. 8.

The signal output from the phase detector is integrated before being fed into the heater amplifier circuit shown in Fig. 9. By feeding this positive or negative signal into the MOS FET in the input stage, proportional control of the heater about the set d.c.

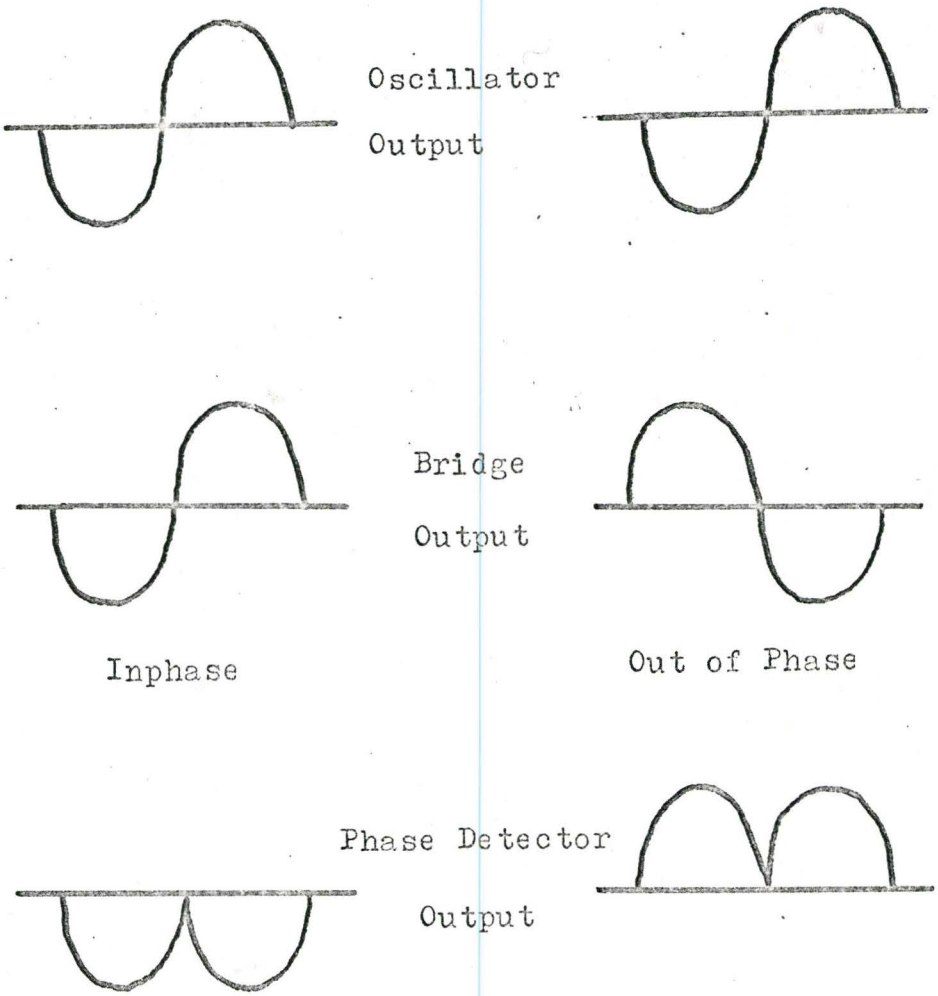

Fig. 6 Phase Detection of the Out-of-Balance Signal From the A.C. Bridge

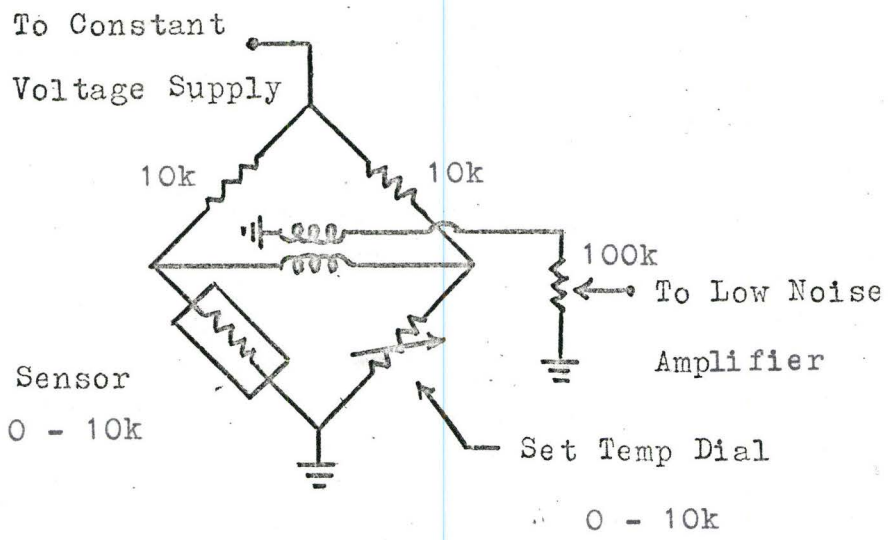

Fig. 7 A.C. Bridge

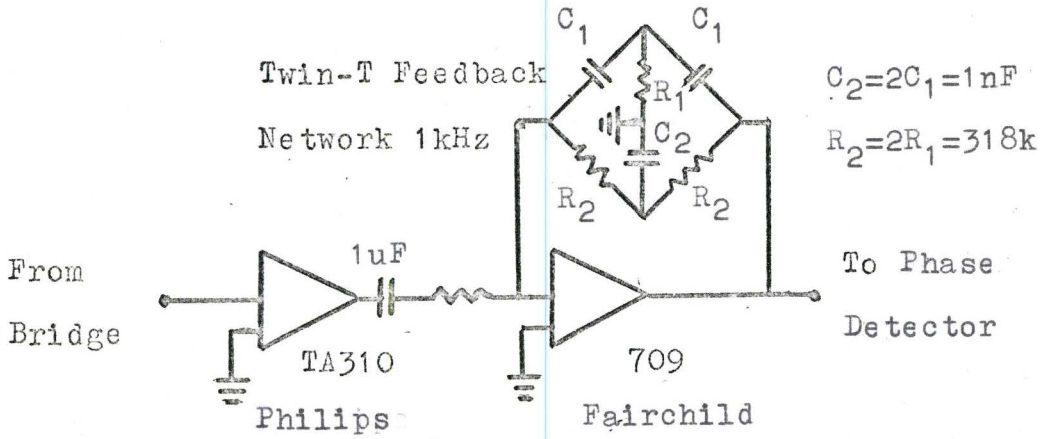

Fig. 8 Low Noise Amplifier

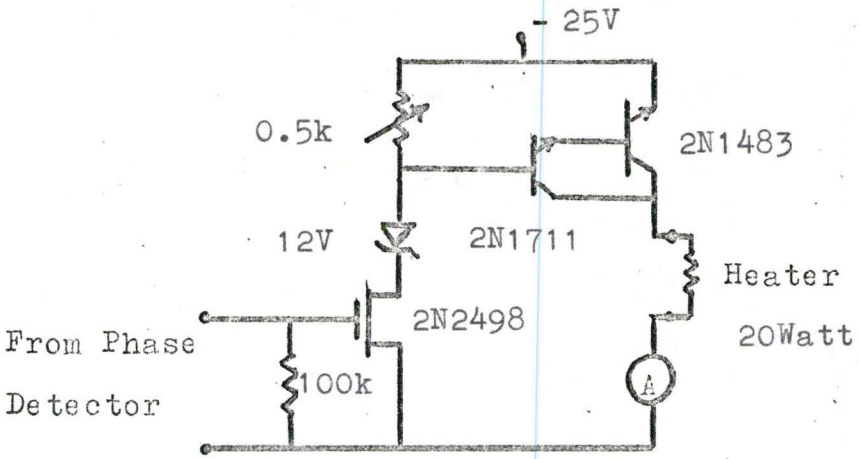

Fig. 9 Heater Control Circuit

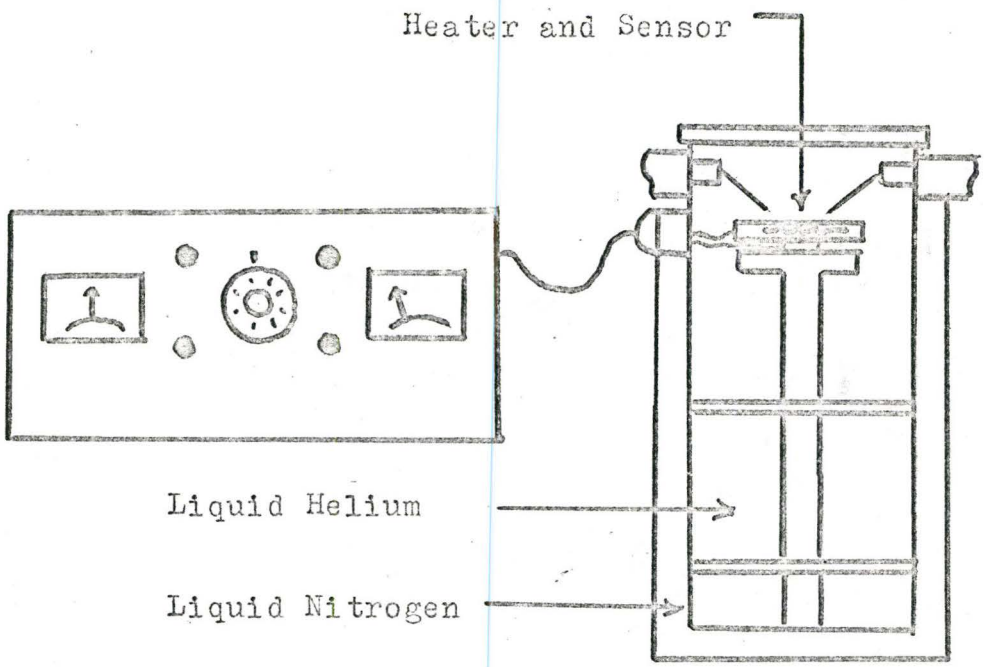

Fig. 10 Liquid Helium Cryostat and Controller

level can be obtained.

The performance capabilities of the complete system (i.e. the temperature controller and the liquid helium cryostat) were not thoroughly tested because the cryostat was still undergoing modifications. The complete system is shown in Fig. 10.

APPENDIX B

Preliminary Measurements on the Noise Measuring Equipment

A block diagram of the noise measuring equipment was shown in Fig. 4.8. The preliminary measurements made to ensure the background noise was negligible compared with the noise of the device were

(a) Equivalent input noise voltage of the Keithley preamplifier as a function of frequency at R_s = 0, 1, and 10 kohm. See Fig. 1.

(b) Frequency response of the Keithley amplifier. See Fig. 2.

The equivalent noise bandwidths of the Quantech wave analyzer were taken as the values of the 3 db. signal power bandwidths.

The procedure for measuring the noise e_n was as follows. The desired bias voltages were applied to the device with the drain current being monitored to ensure no drift occured in the operating conditions. To measure the voltage gain, G_V, of the MOS FET amplifier,

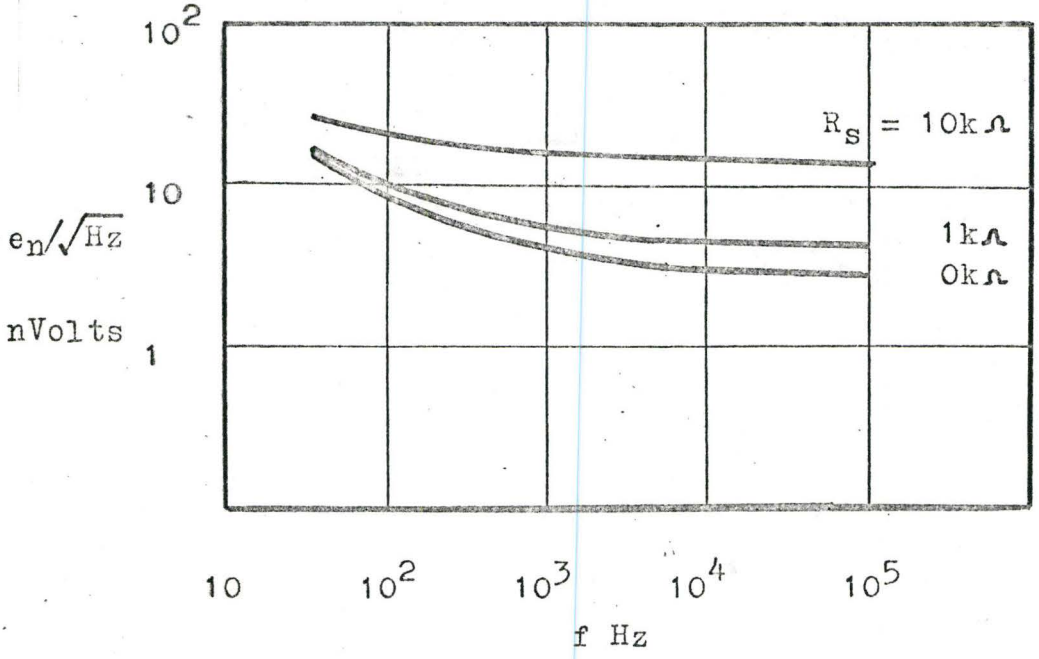

Fig. 1 Equivalent Input Noise of the Keithley Preamplifier

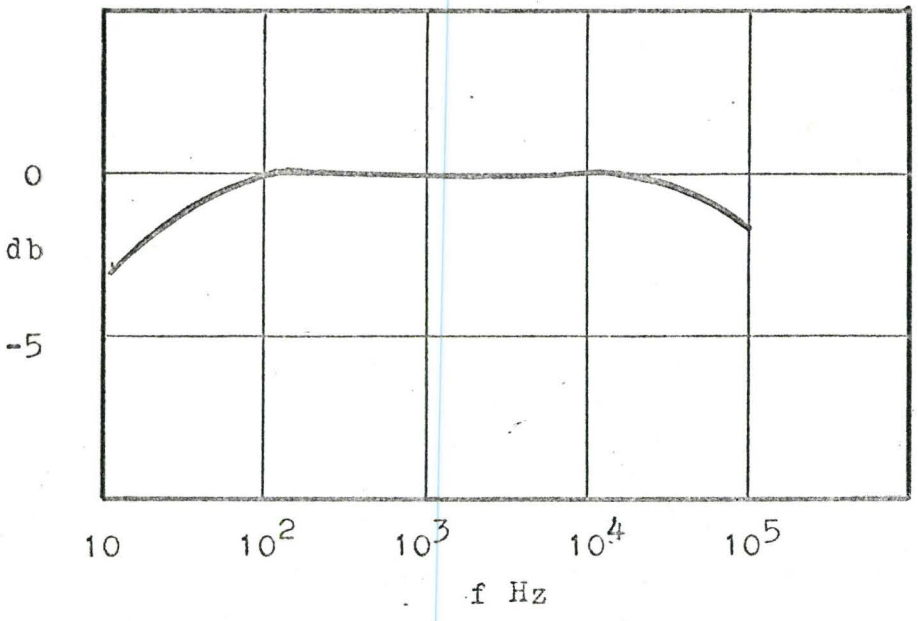

Fig. 2 Frequency Response of the Keithley Preamplifier

a small signal voltage (100 microvolts) at the frequency of interest was applied at the input across the 600 ohm resistor, and the output voltage was measured on the wave analyzer. The known injected voltage was determined by disconnecting the Keithley preamplifier and connecting it across the same 600 ohm resistor. The ratio of the two output voltages on the wave analyzer then gave G_v. The signal generator was then disconnected and the 600 ohm resistor short circuited. The output noise voltage, v_n, in a small frequency bandwidth chosen by the amplifier was then measured on the wave analyzer meter. The equivalent input input gate noise voltage was then given by

$$e_n = \frac{v_n}{G_v G_p \sqrt{B_n}}$$

where: G_p = voltage gain of the Keithley preamplifier.

B_n = equivalent noise bandwidth of the Quantech wave analyzer.

APPENDIX C

Measurement of Hysteresis in the MOS FET Gate to Source Capacitance

To plot the capacitance voltage curve of the MOS FET the device was connected as shown in Fig. 1.

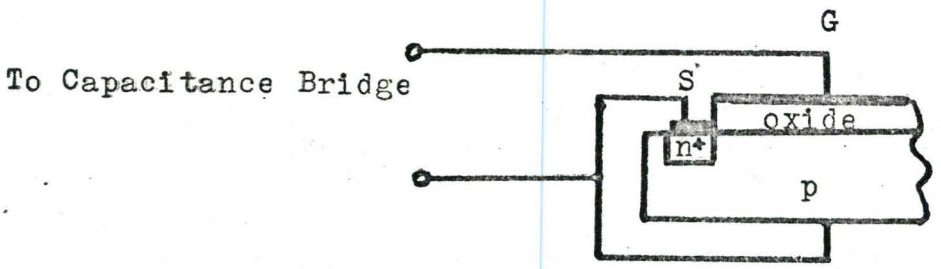

Fig. 1

The sought after hysteresis is exhibited in Fig. 2. These results, however, were not always repeatable. A device with larger gate to source capacitance would have provided more useful results.

Note: Low-temperature hysteresis effects caused by surface-state trapping in MOS capacitors and gate controlled diodes have been reported by A. Goetzberger and J. Irvin. *

* A. Goetzberger and J. Irvin "Low Temperature Hysteresis Effects in MOS Capacitors Caused by Surface-State Trapping", E.D., Vol. 15, No. 12 Dec. 68

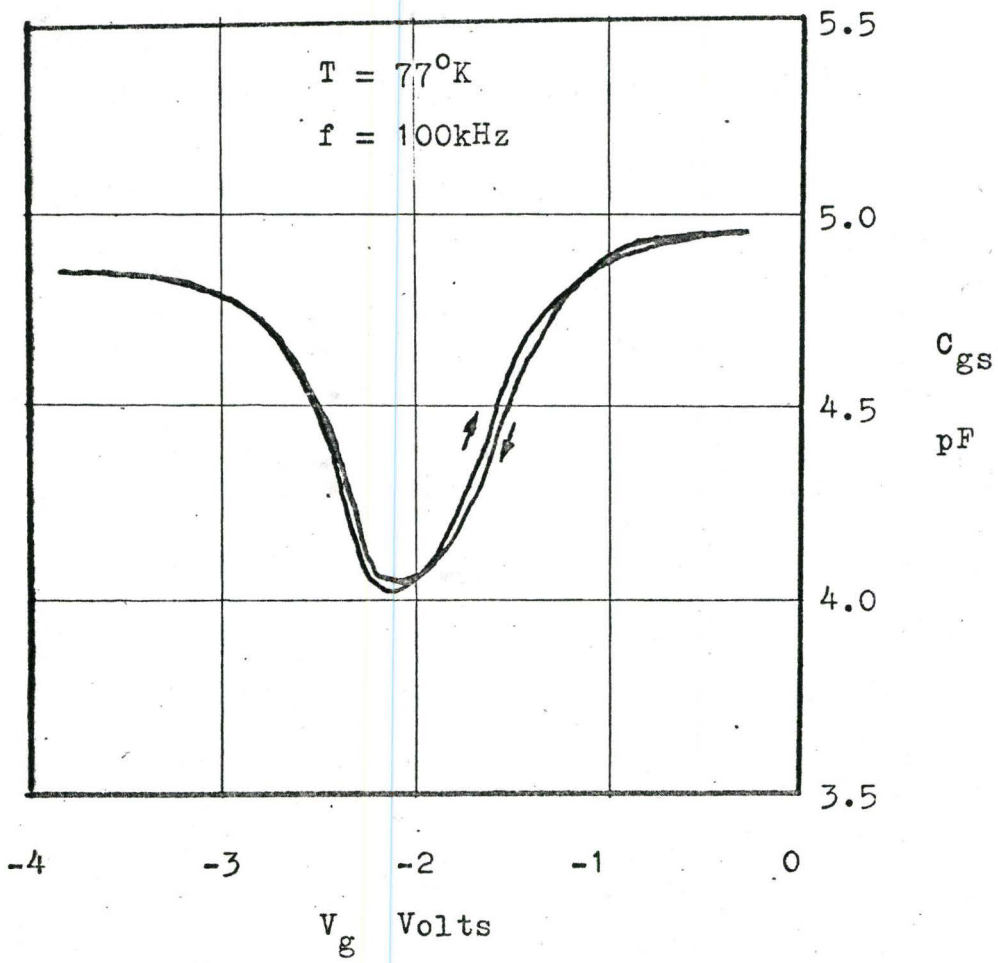

Fig. 2 Hysteresis in the Gate to Source Capacitance Voltage Curve