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NITROGEN IMPLANTED α-SiC

NITROGEN IMPLANTED α-SiC : A CORRELATION BETWEEN ELECTRICAL (C-V) MEASUREMENTS AND DAMAGE STUDIES USING THE CHANNELING TECHNIQUE.

by

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ABSTRACT

The annealing behaviour of ^{15}N implanted, aluminum doped -SiC has been studied by measuring the differential capacitance as a function of applied bias. The samples were doubly implanted at 450°C with 45 KeV and 25 KeV ions, for a dose of $10^{16}/cm^2$ at each energy.

An n-i-p structure with a thick insulator region was found after annealing at 1000°C. The thickness of this i region could be substantially reduced with additional annealing at higher temperatures, and a fairly good n-p junction was obtained after 1480°C anneal.

About 20-30% of the implanted nitrogen ions were found to be electrically active.

The C-V behaviour was found to have large variations with the a.c. measuring frequency.

CHAPTER 1

INTRODUCTION

1.1 Why SiC

SiC is not a new material, however, not until the fifties did researchers realize and begin to exploit its potentialities as a semiconductor. In the closing remarks of the Third International Conference on SiC -- 1973, C. E. Ryan summarized the device potential of SiC as :[1]

1. High temperature devices
2. High power devices
3. High frequency devices
4. High radiation resistant devices
5. High reliability devices
6. Cold cathode devices
7. LED devices
8. Schottky diode devices
9. Specialized devices:
   (a) UV Detectors
   (b) Radiation Detectors
   (c) High temperature photocells
   (d) Heterojunction devices.

The parameters which make SiC such a potentially important semiconductor material are its exceptionally large band gap (~ 3 eV), chemical stability and good thermal conductivity. These factors enable SiC to operate in high temperature environments, at

high power in normal environments and at high current densities. The ability of SiC to operate in high temperature environments where other materials break down is of particular interest.

Table 1.1 lists the intrinsic carrier concentrations of SiC along with Si and Ge at different temperatures (assuming E_g's are constant).

Table 1.1

Intrinsic Concentrations of SiC, Si and Ge

	SiC	Si	Ge
N_i \ E_g	2.9 eV	1.2 eV	0.8 eV
300° K	$2.0\times10^{-5}/cm^3$	$1.7\times10^{10}/cm^3$	$1.8\times10^{13}/cm^3$
600° K	8.3×10^{7}	5.3×10^{15}	1.2×10^{17}
1000° K	1.3×10^{13}	1.2×10^{18}	
1500° K	6.4×10^{15}		

It can be seen here that for a doping level of about $10^{16}/cm^3$, Ge devices will break down for T < 600 K, Si devices will lose their extrinsic properties at T ~ 600 K. However, devices made from SiC can function normally at temperatures well over 1000° K.

Physically, SiC exists in the hexagonal (α) and cubic (β) phases, with the α phase occurring in a variety of polytypes. The bonding of Si and C atoms is basically covalent, with about 12% ionic bonding. SiC is a brittle material, with a hardness just below diamond. It is not attacked by almost all known etching solutions except orthophosphoric acid at 215° C.[2]

1.2 Why Ion Implantation

The progress in SiC technology has been relatively slow and painful in comparsion with Si in the past two decades. The main reasons are:

(i) good quality, reproducible single crystals are hard to grow,

(ii) fabrication difficulties, and

(iii) lack of strong economic incentives.

For the various methods of growing SiC crystals and their problems involved, readers are referred to the technical papers appeared in the three proceedings of the International Conference on SiC.[3]

To fabricate semiconductor devices, diffusion method has long been the most common and well developed technique, however, for SiC, it requires a process temperature of over $1800^{o}C$ and long process times. At such a high temperature, surface of SiC dissociates, this makes the process extremely hard to perform. In addition, it is not possible to use passivating oxide layers at these temperatures to mask against diffusion, making precision fabrication of SiC planar devices very difficult. P-N junctions have been fabricated, but the techniques have not yet been fully developed.[4]

Because of the difficulties experienced in controllably doping SiC by the standard processes, scientists begin to look at ion implantation as an alternative doping technique.

Ion implantation holds good promises, however, it is not without problems. After implantation, a badly damaged surface layer will be formed, the position and width of the layer depend on the dose and energy of the implanted ions. These radiation damage effects result in compensating defect donor and acceptor levels which must be annealed out. Also the implanted dopant must locate on a substitutional site to become electrically active.

Marsh and Dunlap [5] found a p-i-n device behaviour for junctions formed by double nitrogen implant of $10^{15}/cm^2$ at 84 KeV and $10^{15}/cm^2$ at 25 KeV after high temperature annealing (over 1000^oC) and observed a normal p-n junction when samples are annealed up to 1500^oC. However, when the same authors tried to implant group III elements (B, Al, Ga, In, Tl) into n-type SiC with subsequent anneals up to 1700^oC, no type conversion was observed. The presence of electrically compensating defects was suggested to explain this negative results.

1.3 Objective of present work

The purpose of this work is to investigate the potential of nitrogen implantation into p-type SiC as a suitable process for forming junctions and hence devices, and to determine problems involved and potential solutions.

1.4 The Procedure

Samples used were Aluminum doped 6H α-SiC, kindly provided by the Westinghouse Astronuclear Laboratory. The total aluminum concentration was found to be about $10^{19}/cm^3$* by neutron activation analysis. All samples were doubly implanted with 45 KeV and 25 KeV N^{15} ions at a substrate temperature of 450°C. Implant conditions chosen are believed to be potentially suitable conditions from previous results of Campbell etal.[6] Double implants are required to approximate a linear distribution of implanted ions. N^{15} isotope was chosen so that the $N^{15}(p,\alpha)C^{12}$ nuclear reaction could be used to study the lattice location of the implanted nitrogen atoms using channeling technieques. The samples were implanted to a dose of 2×10^{16} ions/cm^2. The calculated doping concentrations were approximately $10^{21}/cm^3$ throughout the region of peak concentration.

The implanted samples were annealed at stages up to a maximum available temperature of 1480°C. At each temperature, electrical properties of the samples were investigated through C-V measurement.

* Value supplied by manufacturer was $10^{18}/cm^3$, which was probably a compensated value.

CHAPTER 2

ELECTRICAL CONTACTS

2.1 General Theory

To investigate the properties of semiconductor devices, in most cases, the metal contact to the semiconductor is extremely important. Usually it is desired that the contact be ohmic.* In principle, this means a contact which has a linear I-V relationship in both directions.

The basic principles for ohmic contacts has been treated in detail by Milnes and Feucht[7]. Theoretically, there are three major approcaches to achieving an ohmic contact: (a) by choosing a metal with the proper relative Fermi level so that the barrier is small for thermally excited current. (b) by heavily doping the semiconductor near the junction so that the current can be carried by quantum mechanical tunneling through the barrier, and (3) by introducing numerious recombination centers in the interface region on the semiconductor side of the junction.

In practice, the first approach works good only for the more ionic semiconductors, e.g. ZnS. For covalant semiconductors such as Si, Ge and GaAs, the resulting barrier tends to remain constant for all metals regardless of the metal work functions, because of the existence of large number of surface states. Therefore, the second appraoch is generally used, i.e. forming a very heavily doped semiconductor region between the metal and bulk semiconductor.

* In some cases, for example, a Schottky diode, rectifying contact is needed. However, the back contact to the diode is still desired to be ohmic.

This method works quite well for Si, Ge and GaAs. However, for wide band gap semiconductors such as SiC, it is difficult to obtain the required heavy doping because of their tendency to compensate for the introduced foreign atoms by the formation of native defects of the opposite type.

2.2 Ohmic Contact To SiC

Because the conventional theoretical approaches to achieving ohmic contacts do not work good on SiC crystals, researchers tend to solve the problem by trying different metals and metal alloys under varying conditions. A search into the literatures has been made, the metals reported forming ohmic contacts to SiC are summarized in Table 2.1.

Table 2.1

Various Metals Reported as Ohmic Contacts to SiC

Metal	Conductivity Type	Process	Reference
In-Ag, Al-Si	n,p	soldered	5
Tungsten	n	bonded in vaccum at 1900°C	8
Tungsten	n,p	fused at 1900°C	9
Si-Al, Si-B	p	fused at 1700°C	9
Au-5%Ta	n,p	alloyed in vaccum	10
Au-Ta	n	alloyed in vaccum at 1250°C	11
p doped Si		fused at 1432°C	12

Table 2.1 (Continued)

Metal	Conductivity Type	Process	Reference
Pt		evaporated in vaccum annealed at 1340°C	12
Cu-Ti, Al-Si	p	eutectic alloy	13
Au		sputtered	14
Ti	n	evaporated in vaccum at 250°C	15
Pt-Sn	n,p	alloyed at 1800°C	16
Ni solution		electroless plating	17

From Table 2.1, it can be seen that in most cases, high alloying or fusing temperatures are required. Such high temperature processes are particularly undesirable for the present work, because the electrical properties of the implanted junction at different annealing temperatures are to be investigated and thus, heating the samples up to a high temperature in a single step is out of question. Therefore, it was decided to investigate the contact problem more fully in the hope that ohmic contacts could be made without high temperature treatment.

The process used was vaccum deposition of metals or metal alloys. A set of blue-black (heavy p-type doping) and green (n-type doping) 6H SiC crystals were used. The sample were cleaned and then etched in HF solution for a few hours before contacts were made in high vaccum (with pressure less than 10^{-5} torr). Subsequent annealings were performed in some cases. The contacts were checked with a curve tracer.

The results obtained are tabulated in Table 2.2.

Table 2.2

Metal Contacts to SiC

Metal	Conductivity Type	Annealing (Temp./Time)	Contacts	Contact[+] Resistance
In-Ag alloy	n,p		non-ohmic	
		430°C/20'	non-ohmic	
Ti + Au	n,p		non-ohmic	
		1100°C/10'	non-ohmic	
Sn + Nicr	n		non-ohmic	
		800°C/10'	non-ohmic	
Sn + Au	n		non-Ohmic	
		800°C/10'	non-ohmic	
In + Au	n		non-ohmic	
		800°C/10'	non-ohmic	
In + Ag	n,p		non-ohmic	
		500°C/10'	non-ohmic	
Nicr	n,p		non-ohmic	
		800°C/10'	non-ohmic	
Mg + Au	n		non-ohmic	
		200°C/15'	non-ohmic	
		650°C/15'	non-ohmic	
Bi + Au	n		non-ohmic	
		240°C/15'	non-ohmic	
		275°C/60'	ohmic at low voltage	~ 20K

Table 2.2 (Continue)

Metal	Conductivity Type	Annealing (Temp./Time)	Contacts	Contact+ Resistance
Cr + Au	p		non-ohmic	
	n		ohmic at low voltage	100 Ω
++Al	n		non-ohmic	
		700°C/15'	non-ohmic	
++Al	p		non-ohmic	
		500°C/15'	non-ohmic	
		600°C/15'	non-ohmic	
		660°C/10'	ohmic	40 Ω
		700°C/10'	ohmic	30 Ω
		750°C/10'	ohmic	150 Ω

\+ Contact resistance depends strongly on the doping level of the particular sample, it is listed here just for illustrative purpose.

++ Al melts at 660°C, for annealing temperatures higher than 660°C, a layer of gold was evaporated on top of the Al contacts.

It can be seen that, Al made satisfactory contacts to p-type SiC with acceptable low heat treatment (660°C). Therefore, it was chosen to be the contact metal in subsequent experiments.

However, it turned out that the process did not work for the implanted samples. Instead of forming ohmic contact to the p-substrate back face, Al contact was found to be ohmic to the implanted face instead. The failure to form ohmic contact to the back face is probably because of the higher resistivity of the samples used. Similar failure has been reported by Frick.[12]

The formation of ohmic contact to the implanted face was a bit puzzling. From previous studies,[5,6] it was found that an insulating layer was formed under the surface after implantation, therefore, the apparent ohmic contact formation must be resulted from some surface effects, which have nothing to do with the semiconductor bulk properties. This belief was supported by later experiments, a metal - (n)semidonductor junction was observed after the implanted nitrogen becomes electrically active, although the surface was still ohmic.

CHAPTER 3

DIFFERENTIAL CAPACITANCE MEASURING TECHNIEQUE

3.1 C-V Measurements

In the study of semiconductor junctions, C-V measurement technique is a powerful analytical tool. From the C-V curves, many properties of the junctions can be deduced.

In the capacitance measurement, a d.c. electric field is applied across the junction. For a given applied field, a definite charge distribution in the device will arise. The differential capacitance of the resulting semiconductor space-charge region is then measured by superimposing a small a.c. voltage on the d.c. bias. The differential capacitance as a function of applied bias is plotted with an automatic display apparatus. A detailed description of the measuring system used can be found in reference 19.

In the present study and studies by earlier investigators[5], an implanted sample was found to show an MIS device behaviour when annealed at temperatures less than 1000°C. After 1000°C or higher temperature anneal, a p-i-n structure and then a rather good p-n junction was observed.

C-V behaviour of an MIS device, an n-i-p structure, and an MS and p-n junction are outlined in the following sections. Possible interpretations of the C-V curves obtained are also discussed.

3.2 Ideal MIS C-V curves

Theory of the MIS structure has been considered in detail elsewhere[20,21], here only a brief description is given.

Consider a p-type MIS diode shown below.

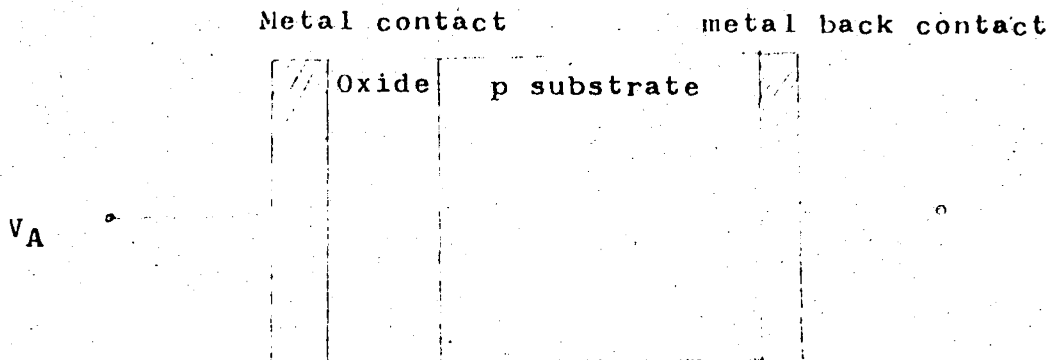


Fig. 3.1 An MIS diode

A d.c. bias, V_A is applied between the metal electrodes.

For the ideal case, effects of the work function difference between the metal and semiconductor, and surfaces states are ignored. The resistivity of the insulator is assumed to be infinite.

When the diode is forward biased with a negative V_A, the majority carriers (holes) in the p-substrate will be attracted to the insulator interface. There will be an accumulation of holes and therefore a high differential capacitance of the semiconductor substrate. As a result, the total capacitance measured will be roughly constant and close to the insulator capacitance alone. It is independent of V_A and is given by :

$$C_i = \frac{K_i \epsilon_o A}{t_i} \qquad (3.1)$$

where K_i is the dielectric constant of insulator

ϵ_o is the free space permittivity (8.85×10^{-14} F/cm)

A is the metal contact area

t_i is the insulator thickness

For positive V_A, the diode is reverse biased, holes will be repelled from the insulator - semiconductor interface and leave behind a region depleted of mobile carriers. This depletion region in effect adds to the thickness of the insulating layer and hence the total capacitance decreases. Since the width of the depletion region depends on V_A, the total capacitance is also a function of the applied bias and can be shown equal to:

$$\frac{C}{C_i} = \left[1 + \frac{2K_i^2 \epsilon_o}{qN_A K_s t_i^2} V_A \right]^{-\frac{1}{2}} \qquad (3.2)$$

where C_i is given by (3.1)

q is the electronic charge

N_A is the compensated substrate impurity concentration

K_s is the dielectric constant of semiconductor

Upon further increase in the applied voltage, minority carriers, created mostly by thermal generation, will be attracted to the

vicinity of the insulator-semiconductor interface and form a narrow inversion region. This inversion layer will shield the semiconductor substrate from effects induced by further increases in V_A. The depletion region thus stops increasing and correspondingly, the capacitance reaches a constant minimum value. This is called the high frequency capacitance.

If the measuring a.c. signal has frequencies low enough in comparsion with the generation rate of minority carriers, the electrons in the inversion region will be able to follow the variation of the signal, the depletion region becomes 'transparent', and the total capacitance will rise again to that of the insulator capacitance C_o. This is the low frequency capacitance.

If the capacitance is measured under such conditions that minority carriers cannot accumulate near the surface in the bias range corresponding to inversion, the depletion capacitance will be obtained. This situation may be encountered if the insulator is very leaky, or if the number of minority carriers present is negligible.

The capacitance-voltage characteristics of an ideal MIS diode are shown in Fig. 3.2.

Due to its wide energy gap, SiC has a negligible minority carrier concentration at room temperature. Therefore a very slow minority carrier generation rate would be expected; hence no inversion layer should be formed in the semiconductor surface at the interface. Later experiments

indeed proved this impossibility, depletion capacitance was obtained for measuring frequency as low as 200 Hz.

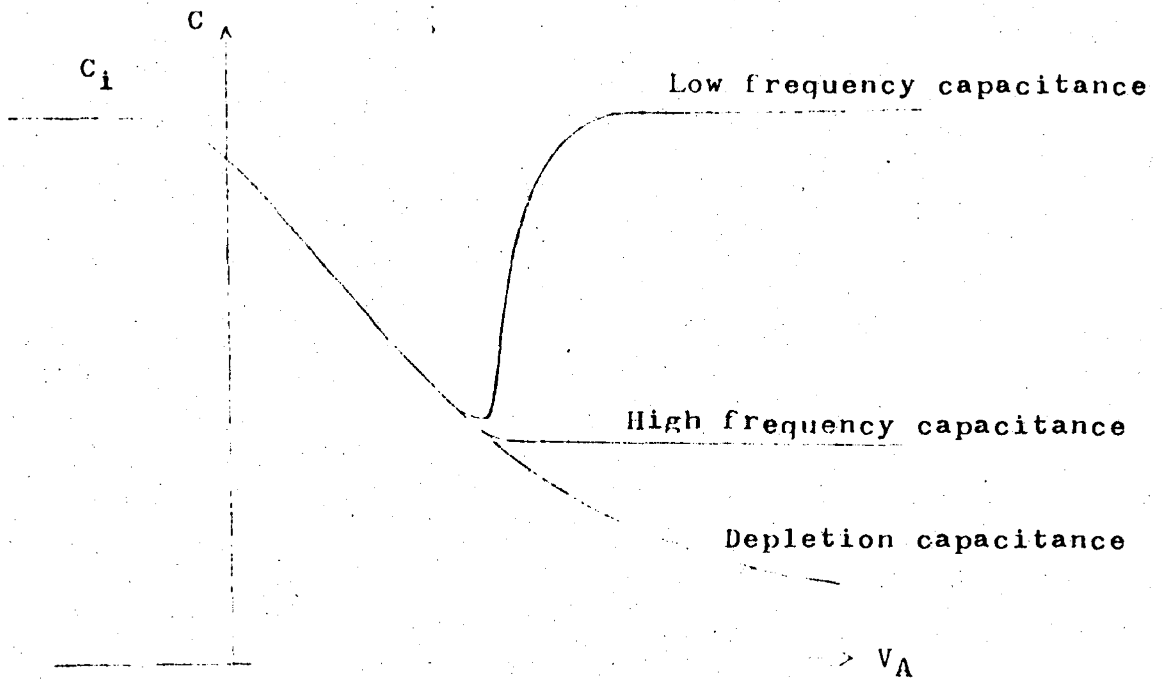


Fig. 3.2 C-V Characteristics of an Ideal MIS DIODE.

3.3 C-V curve of implanted SiC -- low temperature anneal

A typical C-V curve of nitrogen implanted p-type SiC* obtained in the present work after low temperature anneal is shown below.

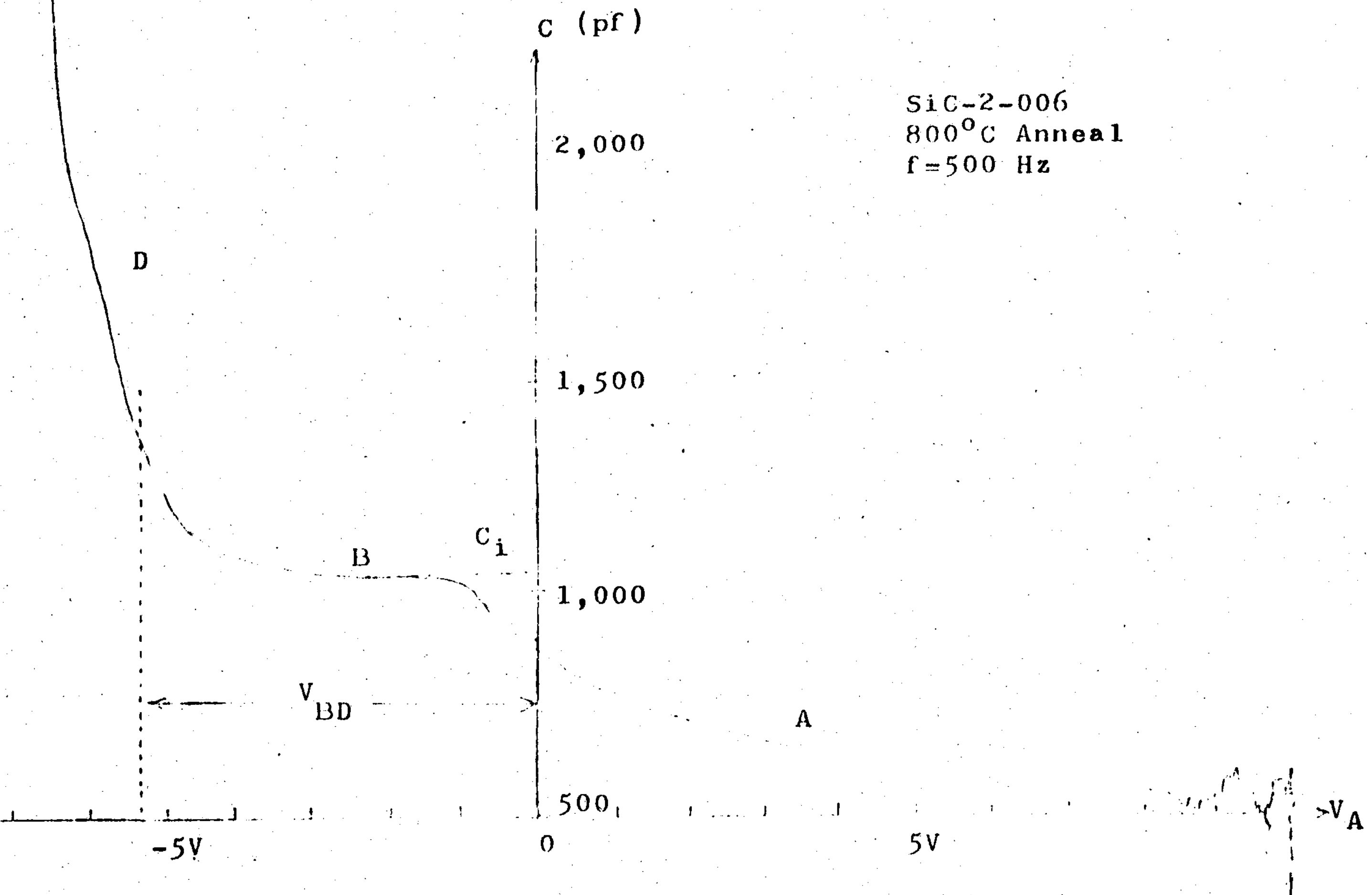


Fig. 3.3 C-V curve of nitrogen implanted (p) SiC -- after 800°C 10' anneal.

From Fig. 3.3, three distinct regions, A,B, and D can be identified.

(i) Region A is the reverse biased region. The total capacitance is seen to follow the depletion capacitance. Eq.(3.2)

* Doubly implanted with 45 KeV and 25 KeV N^{15} ions at a substrate temperature of 450°C, to a total dose of 2×10^{16} ions/cm^2.

is valid in this region. The compensated substrate impurity concentration N_A can be deduced as follow.

Equation (3.2) can be written as:

$$\frac{C_i^2}{C^2} = 1 + \frac{2K_i^2 \epsilon_o}{qN_A K_s t_i^2} V_A$$

Since

$$C_i = \frac{K_i \epsilon_o A}{t_i^2} \qquad (3.1)$$

$$\frac{1}{C^2} = \frac{1}{C_i^2} + \frac{t_i^2}{K_i^2 \epsilon_o^2 A^2} \frac{2K_i^2 \epsilon_o}{qN_A K_s t_i^2} V_A$$

$$= \frac{1}{C_i^2} + \frac{2}{qN_A K_s \epsilon_o A^2} V_A$$

By plotting $1/C^2$ against V_A, N_A can be found from the slope of the plot.

$$N_A = \frac{2}{q S K_s \epsilon_o A^2} \qquad (3.3)$$

where S is the slope of the $1/C^2$ vs V_A plot

(ii) Region B is the forward biased region. The total capacitance is given by the insulator capacitance, Eq. (3.1). Since the insulating layer is actually the damage layer incurred by implantation, equation (3.1) can be used to estimate the junction depth:

$$t_i^2 = \frac{K_s \epsilon_o A}{C_i} .$$

(iii) Region D is the breakdown region. When a large enough forward bias is applied, the insulator will breakdown and become conducting. The capacitance will then rise rapidly. The maximum voltage that an insulator can withstand without breaking down depends on how good the insulator is. The better the insulator, the higher the breakdown voltage (V_{BD}) will be. Therefore, V_{BD} may be used as a good indicator in comparing the relative degrees of damage left after different annealing stages.

3.4 C-V Curves of an N-P Junction, an N-I-P Structure and an M-S Junction.

Consider the abrupt n-p junction as shown below.

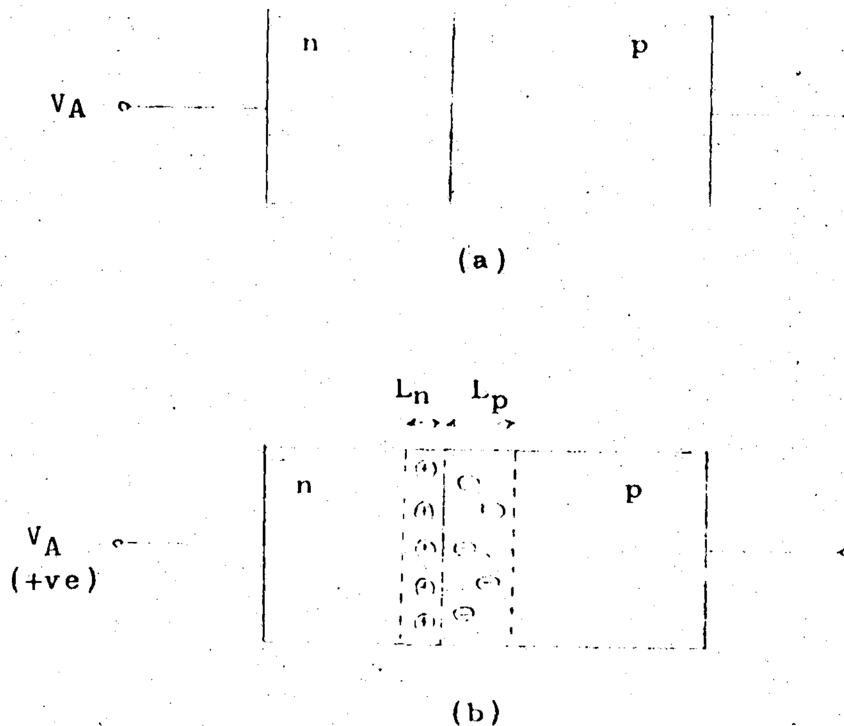


Fig. 3.4 (a) an abrupt n-p junction
(b) with reverse bias

When the junction is reverse biased, holes in the p region and electrons in the n region will be repelled away from the junction. Depletion regions will be formed in both sides of the junction with depletion widths L_n and L_p in the n and p regions respectively. The capacitance is thus given by

$$C = \frac{K_s \epsilon_o}{L_n + L_p}$$

and this can be expressed in terms of the doping levels, N_D and

N_A, and the applied bias V_A as:(22)

$$C = \left[\frac{qK_s\epsilon_o N_A N_D}{2(V_{bi} - V_A)(N_A + N_D)} \right]^{\frac{1}{2}} \quad (3.4)$$

where V_A is positive if the bias is in the forward direction, negative if reverse.

V_{bi} is the built-in voltage of the junction and is given by

$$V_{bi} = \frac{KT}{q} \ln \frac{N_D N_A}{N_i} \quad (3.5)$$

N_i is the semiconductor intrinsic carrier concentration.

For an unsymmetrical barrier with one side more heavily doped than the other, e.g. $N_D \gg N_A$, Eq.(3.4) can be reduced to a simpler form,

$$C = \left[\frac{qK_s\epsilon_o N_A}{2(V_{bi} - V_A)} \right]^{\frac{1}{2}} \quad (3.6)$$

which can also be written as

$$\frac{1}{C^2} = \frac{2}{qK_s\epsilon_o N_A} (V_{bi} - V_A) \quad (3.7)$$

Therefore, by plotting $1/C^2$ vs V_A, a straight line should be obtained. V_{bi} can be deduced from the x-intercept of the curve and N_A can be found from the slope of the straight line, S

$$N_A = \frac{2}{qK_s\epsilon_o S} \qquad (3.8)$$

It should be noted that this is the same as Eq.(3.3) for the MIS structure.

An n-i-p structure has essentially the same C-V response as an MIS diode. When reverse biased (Fig. 3.5 b), the total capacitance of the n-i-p structure is a series combination of the insulator and depletion regions capacitances. If L_n is much smaller than L_p, i.e. the n region is much more heavily doped than the p region, the total capacitance will be the same as that of an MIS diode and is given by Eq. (3.2).

When the structure is forward biased, only the insulator capacitance will be measured and the total capacitance will have a constant value until the insulator breaks down.

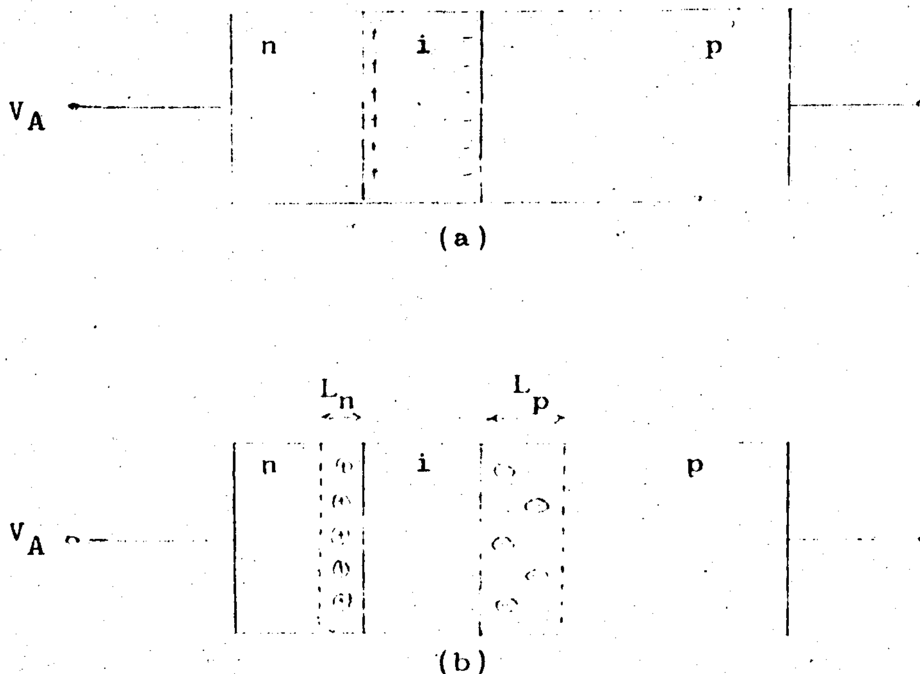


Fig. 3.5 An n-i-p structure. (a) Forward biased, (b) reverse biased.

An MS junction can be considered as a p-n junction with one side much more heavily doped than the other. Equations derived for an n-p junction in the previous pages can be applied equally well here.

3.5 C-V Curve of Implanted SiC -- High Temperature Anneal

A typical C-V curve obtained for an implanted sample* after 1200°C anneal is shown in the following page. A notable feature of the curve is the coming down of the total capacitance in region E. Regions A, B, and D can be readily explained by an n-i-p structure+. To accout for the behaviour in region E, the aluminum contact to the implanted face (which has now been converted into n-type) has to form an MS junction with the crystal rather a resistive contact. The sample will then have a structure as shown in Fig. 3.7.

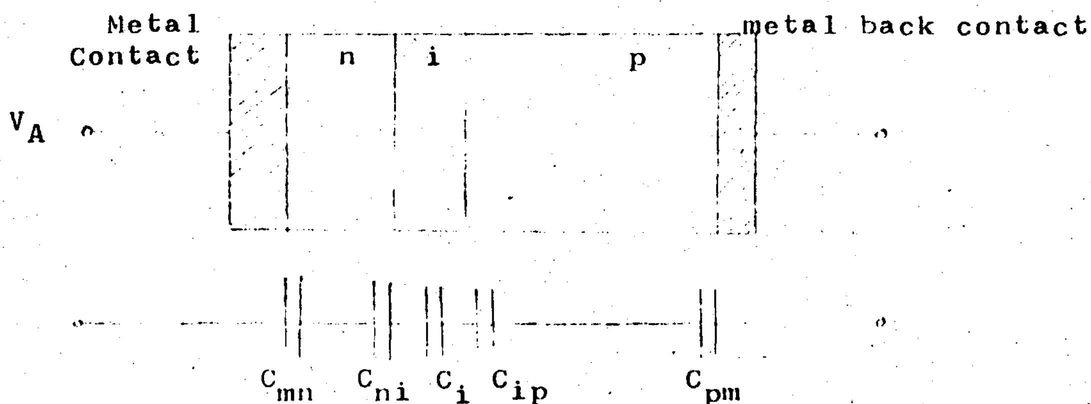


Fig. 3.7 A Possible Model for Implanted SiC after High Temperature Anneal with Individual Capacitances Shown in Series.

* See footnote in P. 17

\+ The presence of an n-region was confirmed by thermal probe test.

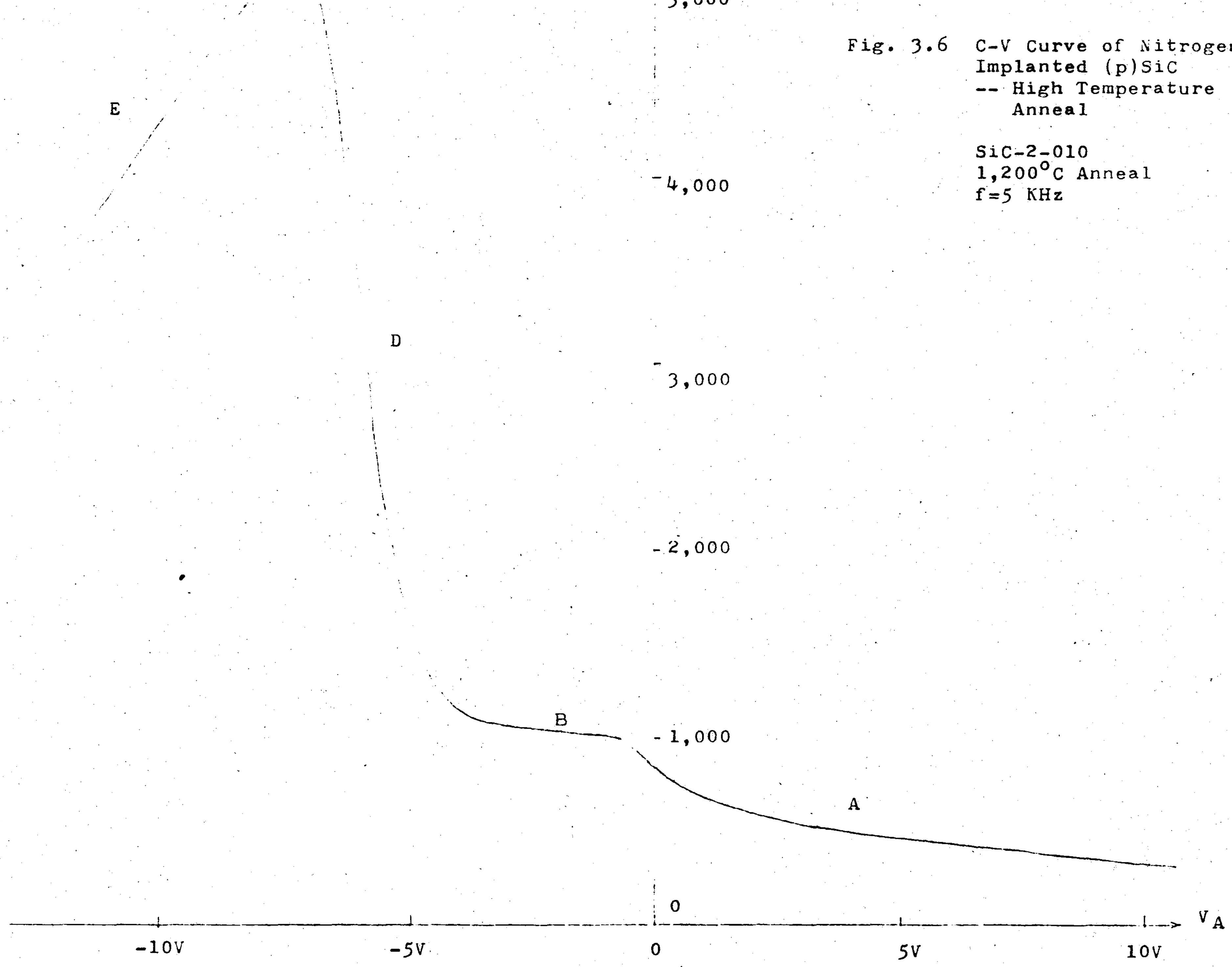


Fig. 3.6 C-V Curve of Nitrogen Implanted (p)SiC -- High Temperature Anneal

The total capacitance of the structure will be the series combination of all the capacitances present and is dominated by the one with the lowest value. C_{pm} is the metal-semiconductor junction capacitance of the back contact. It is included here because of the failure of making good ohmic contact to the p-substrate (Section 2.2). However, the presence of this additional capacitance does not seem to affect the C-V behaviour as will be seen later.

In Fig. 3.7, when V_A is positive, both the front and the back MS junctions are forward biased. C_{mn} and C_{pm} will thus have large differential values. The n-i-p structure, on the other hand, is reverse biased. Therefore, the total capacitance is essentially the same as the reverse biased n-i-p structure. This is region A in Fig. 3.6. If the n-region is much more heavily doped than the p-region*, region A can be used to deduce the doping concentration of the p-region as described in Section 3.3.

When V_A takes a negative value, both MS junctions are reverse biased while the n-i-p structure is forward biased. The capacitance of a forward biased n-i-p structure is just the insulator capacitance C_i as discussed in the previous pages. The total capacitance is therefore a series combination of C_{mn}, C_i, and C_{pm}. However, since the applied voltage will mainly appear across the insulator, the depletion widths of the

* This is true in the present case, as N_D and N_A have values to the orders of $10^{19}/cm^3$ and $10^{18}/cm^3$ respectively.

MS junctions are generally small in comparsion with the insulator width. As a result, C_i will dominate until the insulator breaks down and becomes conducting. This is region B in Fig. 3.6. C_i can be used to estimate the width of the buried damage region by using Eq. (3.1).

When the insulator breaks down under a large forward bias, the total capacitance will adjust itself and rise rapidly to the value limited by C_{mn} or C_{pm} or both. This is region D.

A comment on the back MS junction should be made here. Since aluminum was found to form good ohmic contact with the more heavily doped p-type SiC crystals (Section 2.2), it is very likely that the MS junction may actually behave as a high resistive contact when subjected to large reverse bias. If this is the case, the total capacitance will be given by C_{mn} alone. And region E in Fig. 3.6 is simply the depletion capacitance of the reverse biased front MS junction.

The above supposition is in fact supported by the doping level deduced from the C-V curve in region E*. The impurity concentration was found to have the same order of magnitude as would be expected to present in the converted implanted region. Should the back MS junction have to be considered, the doping concentration deduced would have to be that of the p-substrate. This is because the p-substrate is much less heavily doped than the n-region, C_{pm} would thus dominate the total capacitance and region E would be the depletion capacitance of the reverse biased back MS junction rather than the front. This is obviously not the case.

* From the slope of the $1/C^2$ vs V_A plot.

3.6 Ideal MIS C-V Curves -- A Computer Simulation

In order to compare the experimental results with the ideal theoretical prediction, a computer program was developed which generates the low frequency, high frequency and depletion capacitances for any MIS structure. The program was first prepared by H. B. Lo of Canadian Westinghous Company Limited.[23] The version used here has been modified and improved. The program listing and a sample problem can be found in the Appendix. The program is self explanatory, equations used are based on references 21 and 22.

Fig. 3.8 and 3.9 are the ideal theoretical C-V curves generated by the computer code for p-type MOS(Si) and MIS(SiC) diodes respectively. The oxide or implanted layer thickness used was 1000 Å.

Fig. 3.10 compares the experimental curve obtained for an implanted sample after low temperature anneal with the theoretical prediction. The substrate concentrations used in computing the theoretical curves are found from the slopes of the $1/C^2$ vs V_A plot of the experimental curve. A detailed analysis on the experimental curve reveals the fact that after implantation, there is a redistribution of impurity concentration in the p-substrate near the badly damaged implanted region. This redistribution can be readily seen from an enlarged $1/C^2$ vs V_A plot shown in Fig. 3.11.

Associated with the three slopes in Fig. 3.11 are three distinct doping concentrations:

$$N_{A1} = 7.3 \times 10^{17}/cm^3,$$

$$N_{A2} = 1.2 \times 10^{18}/cm^3 \text{ , and}$$

$$N_{A3} = 1.6 \times 10^{18}/cm^3$$

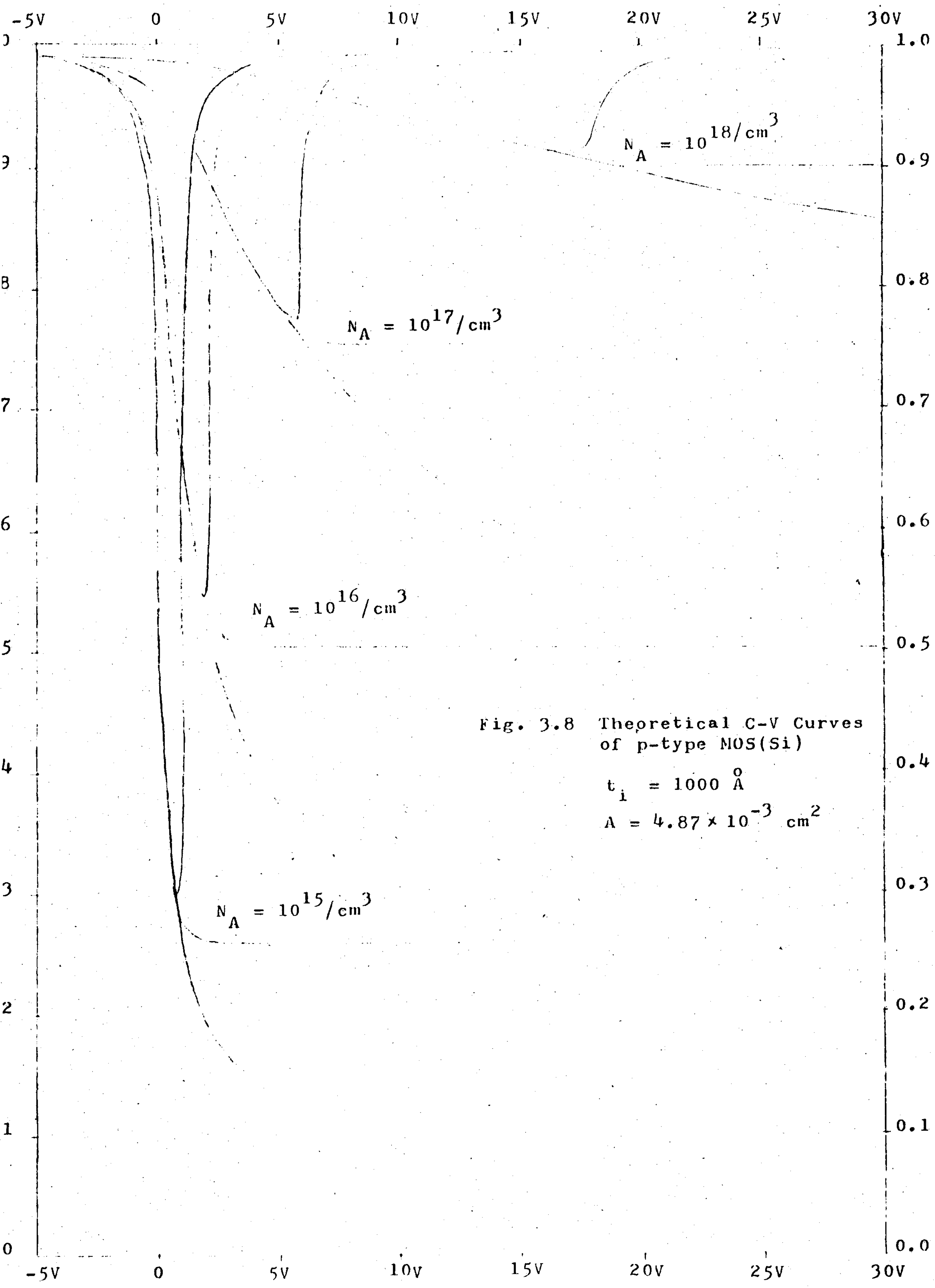


Fig. 3.8 Theoretical C-V Curves of p-type MOS(Si)

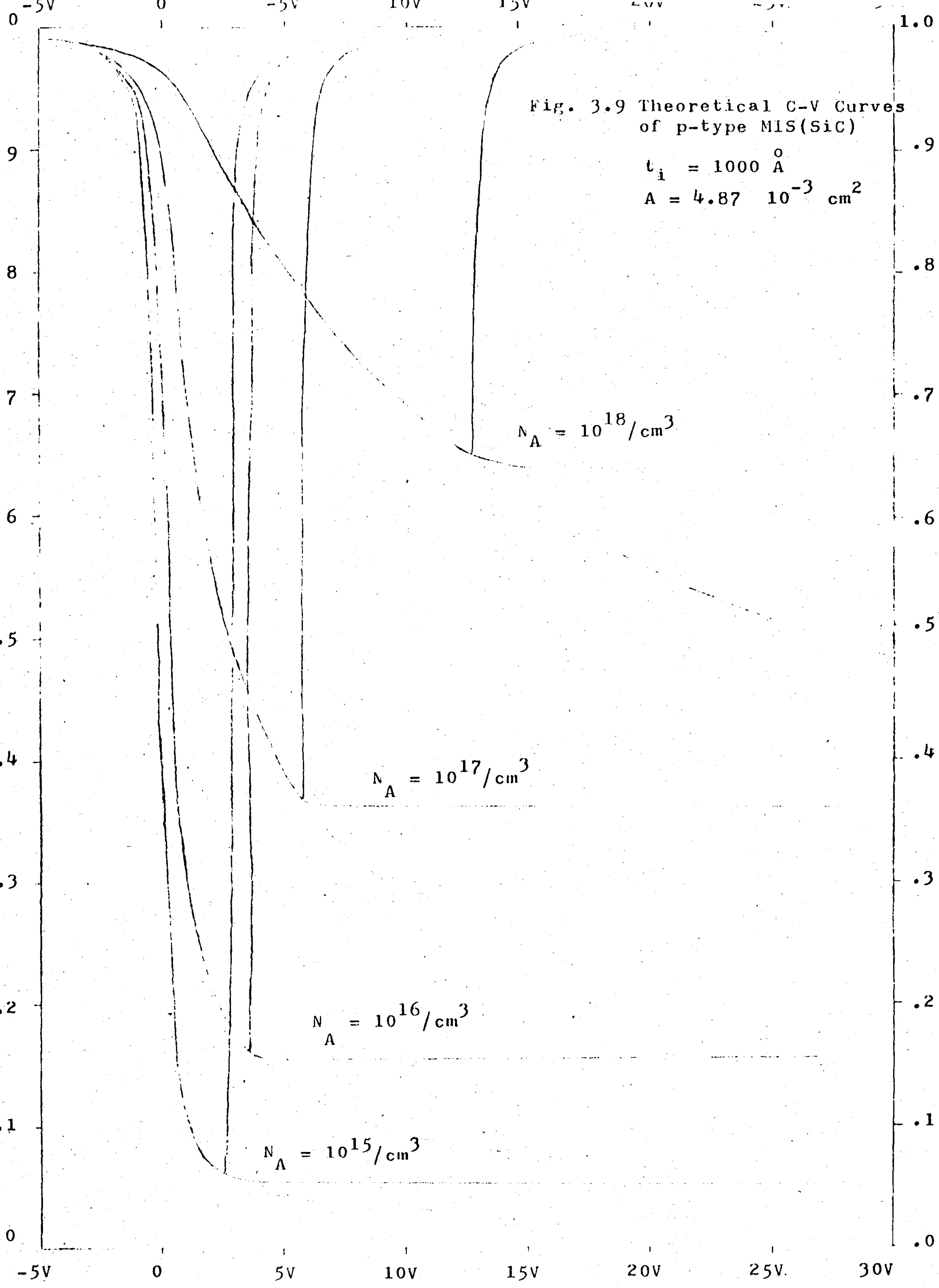


Fig. 3.9 Theoretical C-V Curves
of p-type MIS(SiC)
t_i = 1000 Å
A = 4.87 10^{-3} cm^2
$N_A = 10^{18}/cm^3$
$N_A = 10^{17}/cm^3$
$N_A = 10^{16}/cm^3$
$N_A = 10^{15}/cm^3$
-5V
0
5V
10V
15V
20V
25V
30V
1.0
.9
.8
.7
.6
.5
.4
.3
.2
.1
.0

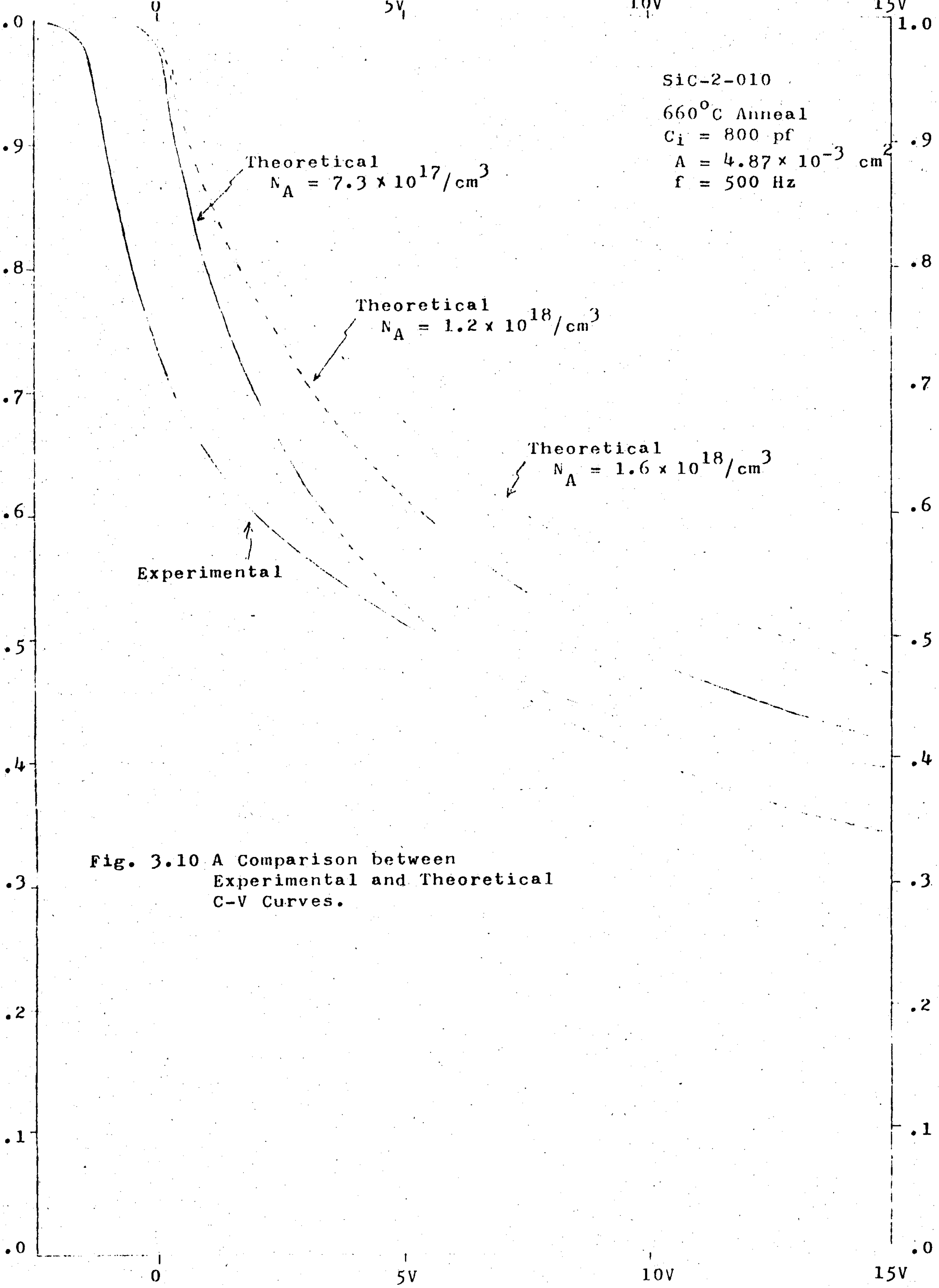


Fig. 3.10 A Comparison between Experimental and Theoretical C-V Curves.

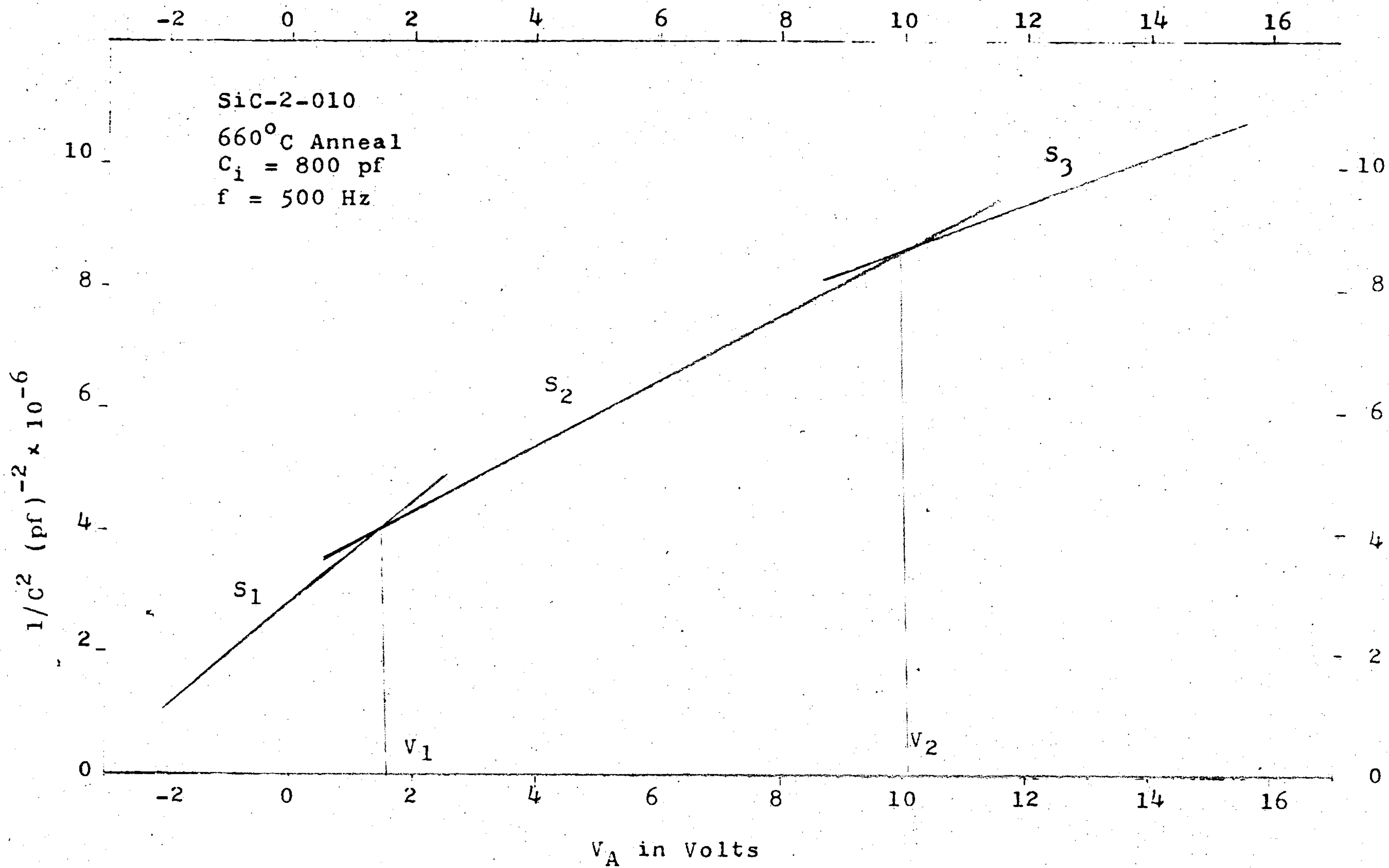


Fig. 3.11 $1/C^2$ vs V_A Plot (obtained from experimental curve in Fig. 3.10)

Therefore, the substrate impurity concentration will have a profile as shown below.

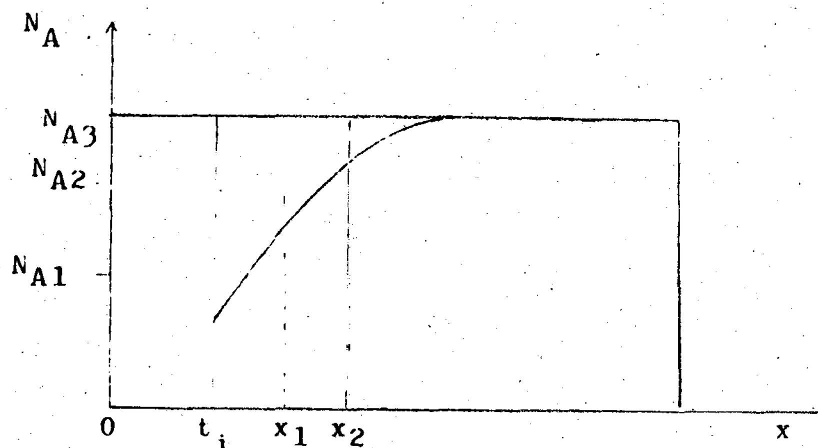


Fig. 3.12 Redistributed substrate impurity conc. profile.
(N_{A3} is taken to be the bulk substrate conc.)

The distance scale in Fig. 3.12 can be estimated by using Eq. (3.1).

$$x = \frac{K_s \epsilon_o A}{C}$$

where C is the capacitance corresponds to V_1 or V_2 in the experimental C-V curve.

The reduction in impurity concentration near the implanted region is probably caused by the defects introduced by deep channeled implanting ions.

Return to Fig. 3.10, it can be seen that the experimental curve is in excellent agreement with the theoretical one if the substrate impurity concentration redistribution is taken into account.

For $V \leq 2V$, the experimental curve agrees perfectly well with the N_{A1} theoretical curve except for a constant horizontal shift of about 1.5V. The horizontal shift is the result of work function difference between metal and semiconductor and surface state effects.

Between $2V \leq V \leq 10V$, the curve follows closely with the N_{A2} curve as expected but a constant horizontal shift of about 3.5V.

For $V \geq 10V$, the experiment curve is expected to follow more closely to the N_{A3} curve.

It should be observed that for the range of voltage under consideration, the experimental curve agrees pretty well with the N_{A2} theoretical curve. Since N_{A2} is about the average concentration over the redistribution region, therefore, in general, a single average concentration can be used in theoretical computation. The required value can be found from the slope of the $1/C^2$ vs V_A plot with V_A some distance away from zero.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Sample Used

Two Westinghouse samples were used in the present investigation. SiC-2-006 was a thin, fairly transparent, well grown single crystal. SiC-2-010 was thicker and slightly greenish in colour. They were grown and ion implanted under identical conditions. However, the bulk acceptor concentration in the former sample was found to be about two times higher than the latter. C-V behaviours of both samples were investigated, each at four different annealing temperatures.

4.2 Frequency Behaviour

Frequency dependence of the C-V measurements at room temperature was investigated by using SiC-2-006 after 800°C anneal. The result is shown in Fig. 4.1. Capacitance measurement was found to be sensitive to the measuring frequency. In general, the capacitance decreases with increasing frequency. It can be seen that when reverse biased, the general behaviour of the C-V curves are the same for all frequencies except that the capacitance is progressively lower with increasing frequency. At large forward bias, however, a deep valley begins to appear at high frequencies.

The observed effect is not understood. It could be resulted from a polarization effect occuring in the damage (insulating) layer.

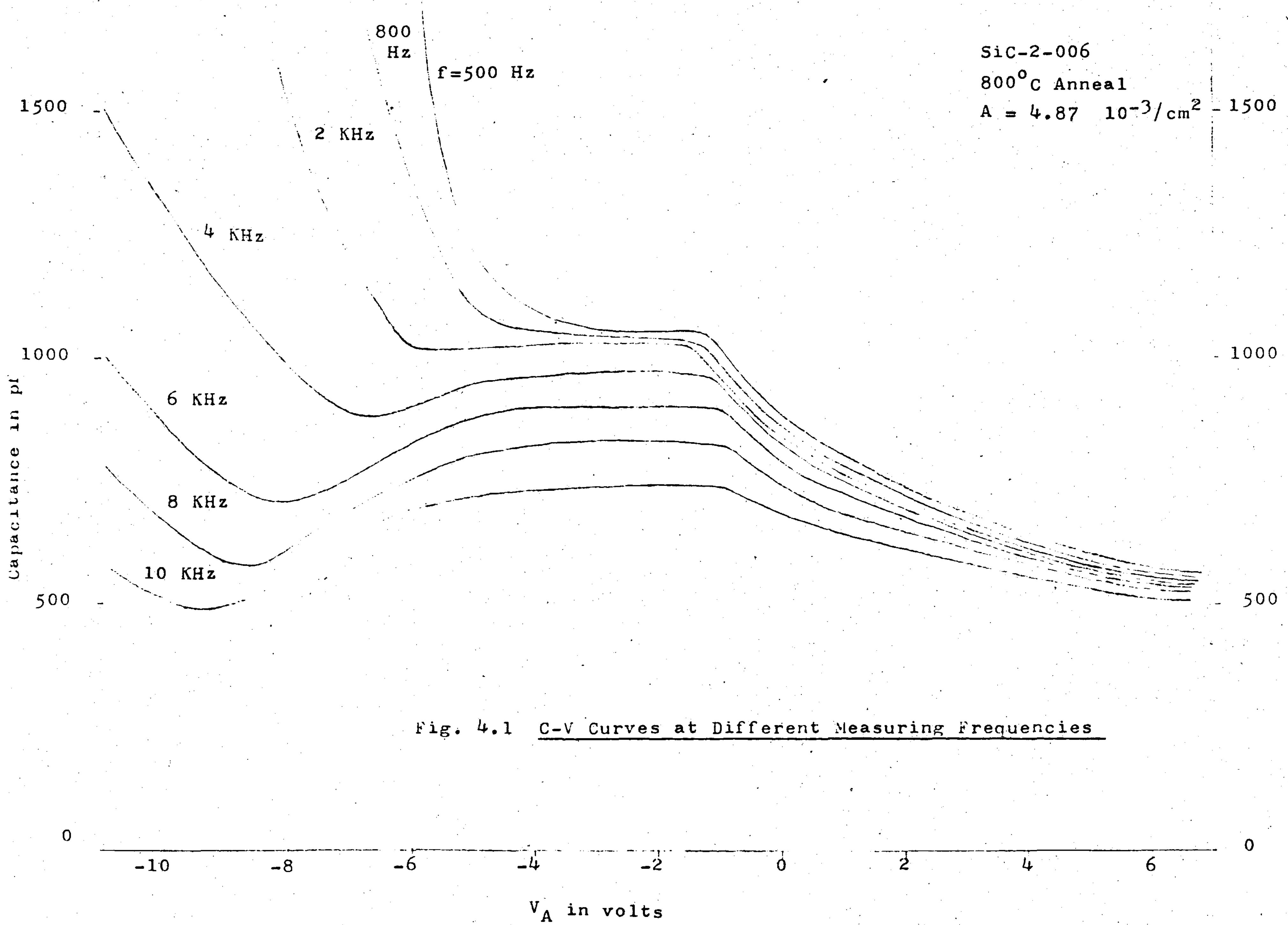


Fig. 4.1 C-V Curves at Different Measuring Frequencies

Dunlap and Marsh, in similar study[5], found that at 300°C the capacitance of a well annealed nitrogen implanted SiC junction diode is essentially independent of frequency. At 23°C, according to the same authors, capacitance decreases in value with increasing frequency.

Gray, in his study of tunneling from metal to semiconductors[24], observed instead, a deep valley at low frequencies. (Fig. 4.2)

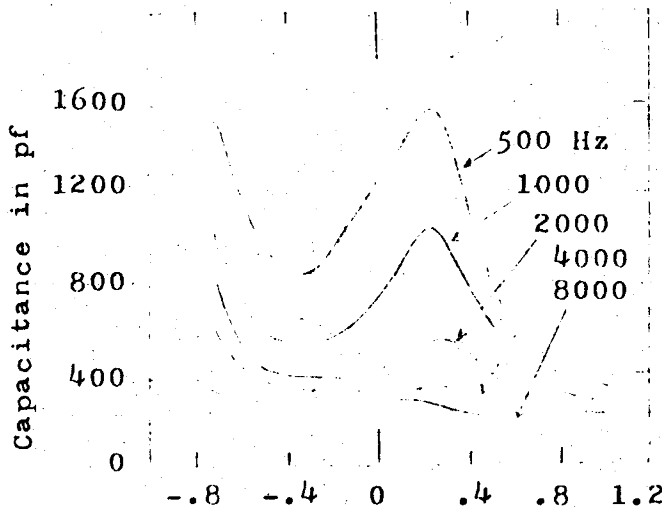


Fig. 4.2 Differential Capacitance versus bias. (after Gray)

The peak in the low frequency curves, as explained by Gray is due to a band of interface states in the $Si-SiO_2$ interface. At the highest frequency, no appreciable charging of the interface states can take place. The capacitance then is that of the oxide layer and space charge region in series.

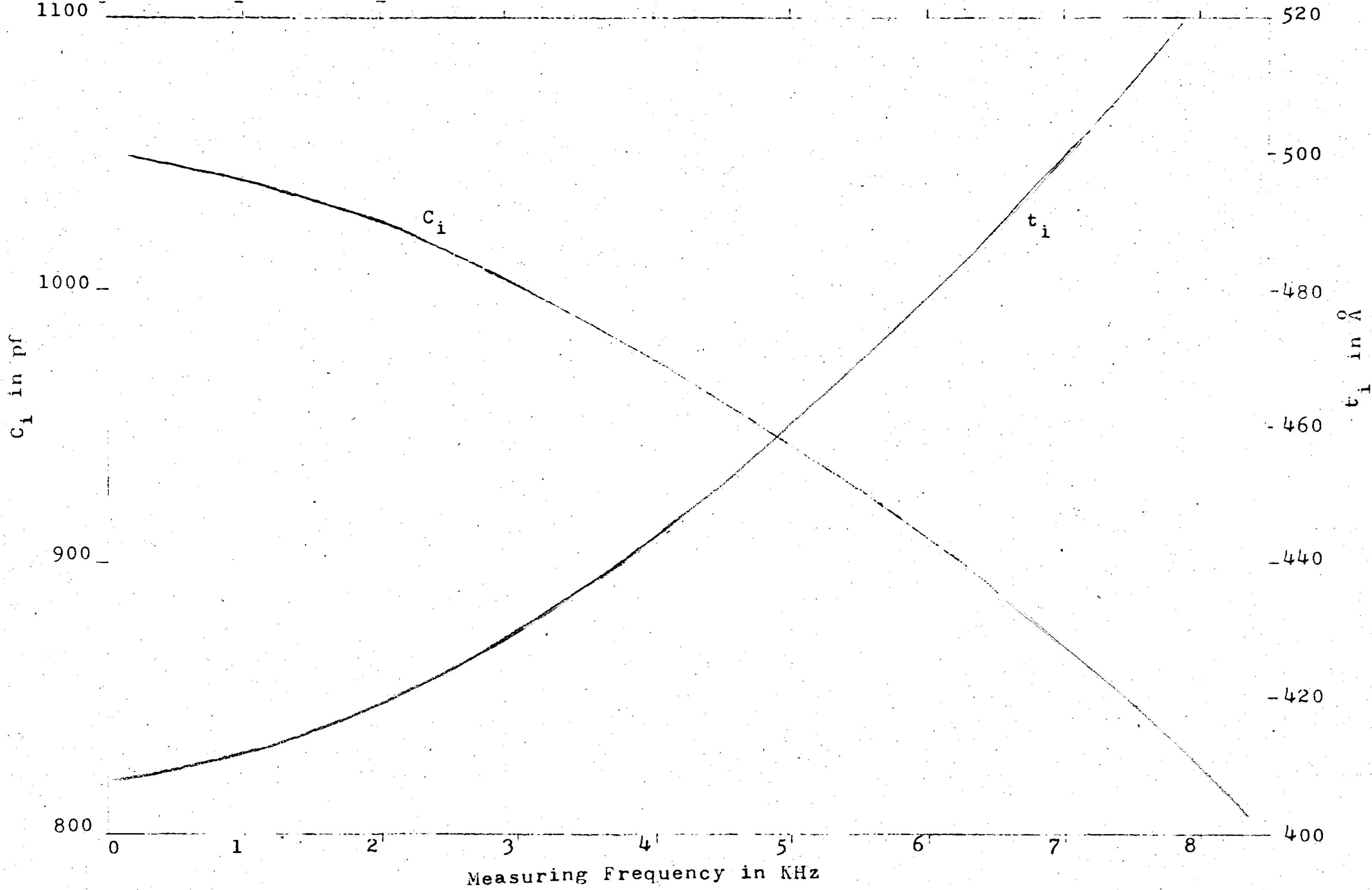


Fig. 4.3 C_i and t_i versus Measuring Frequency Plot

(Taken from Fig. 4.1)

Fig. 4.3 is a plot of C_i against frequency taken from Fig. 4.1. The insulator region width calculated by using Eq.(3.1) is also included. Since the insulator width so determined is subject to large variations in frequency, care should be taken when try to relate it to the effective junction depth or buried damage region width as mention in Sections 3.2 and 3.3.

4.3 Annealing Behaviour

Results obtained from C-V measurements at different annealing temperatures are listed in Table 4.1 in the following pages. The C-V curves were measured at 5 KHz frequency. Curves obtained were generally consistent and reproducible. Aluminum contacts were used in all the measurements shown.

In Table 4.1, N_A and N_D are the substrate acceptor concentration and the converted n-type region donor concentration respectively. They were deduced from regions A and E in the C-V curves (Fig. 3.6) using Eq.(3.3). C_i and t_i are the insulator capacitance and width respectively at the particular measuring frequency. V_{BD} is the breakdown voltage as described in Section 3.3. V_b is the voltage intercept of the $1/C^2$ vs V_A plot. If the structure is a good p-n junction, V_b will be equal to V_{bi}, the built-in junction voltage as discussed in Section 3.4.

A few comments and observations on the table can be made here:

Anneal Temperature	Structure	N_A (cm^{-3})	C_i (pf)	t_i (Å)	V_{BD} (volts)	N_D (cm^{-3})	V_b (volt)
660°C	MIS	9.9×10^{17}	600	720	10	---	7
1000°C	n-i-p	1.1×10^{18}	715	600	8	8.5×10^{19}	6
1200°C	n-i-p	1.1×10^{18}	1050	410	5	6.8×10^{19}	3
1480°C	n-i-p (n-p)??	1.2×10^{18}	1100	390	1.5	3×10^{19}	2.6

Table 4.1 Results from C-V Measurements at Different Annealing Stages

(a) SiC-2-010

Anneal Temperature	Structure	N_A (cm^{-3})	C_i (pf)	t_i (Å)	V_{BD} (volts)	N_D (cm^{-3})	V_b (volt)
800°C	MIS	1.9×10^{18}	950	452	9	---	5
1000°C	MIS	1.8×10^{18}	960	450	10	---	4.2
1400°C	??	---	---	---	--	3×10^{19}	--
1480°C	n-i-p	4×10^{18}	1520	280	1.2	5.5×10^{19}	3.4

Table 4.1 Results from C-V Measurements at Different Annealing Stages

(b) SiC-2-006

(a) By and large, the annealing behaviour of the two samples used are the same. They show MIS device characteristic at low temperature anneals, and change into n-i-p structurres (and possibly n-p junctions) when the annealing temperatures are high enough.

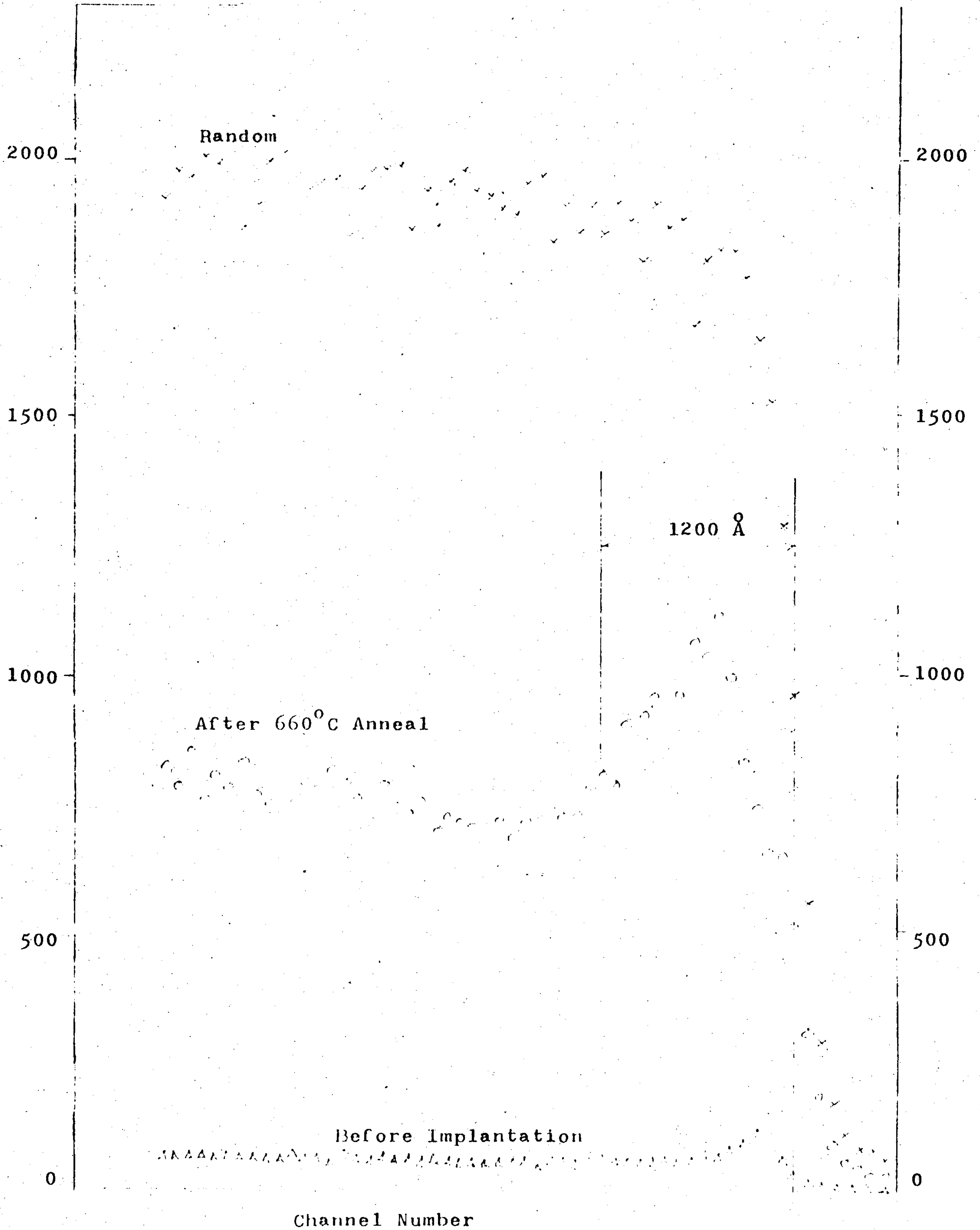
(b) The substrate acceptor concentrations obtained are close to the value provided by the manufacturer ($10^{18}/cm^3$). The increase in N_A with annealing temperature could be result of some of the non electrically active Al (the total Al concentration was found to be $10^{19}/cm^3$ by neutron activation analysis) becoming active by combining with a lattice vacancy to become substitutional. Hence the value obtained for low temperature anneal (i.e. at 660°C or 800°C) could be taken as the initial bulk substrate concentration.

(c) There are large difference in the measured damage region widths between the two samples. Since they were implanted under identical conditions, this difference can only be accounted for by their individual crystal differences.

The effective junction depths are found to be 720 Å and 450 Å for SiC-2-010 and SiC-2-006 respectively. A damage study* on the former sample after 660°C anneal shows a damage peak at around 500 Å beneath surface (fig. 4.4). The junction depth is estimated to be 1200 Å. However, it was found before that the surface of the implanted face was actually conducting at all annealing temperatures. This conductive effect is not known,

* By He^+ backscattering method, using McMaster Van de Graaf accelerator.

Fig. 4.4 Backscattering spectra of 2.0 MeV He^+ obtained for SiC-2-010



it can be just simply surface effects (section 2.2), or as suggested by Fig. 4.4, resulted from a rapid drop off in damage near the surface. In any case, this conductive surface region will extend a few hundred angstroms into the crystal. If this surface region is added to the effective junction depth measured electrically, we will have a good agreement with the junction depth suggested by damage study.

(d) The effective damage width, together with the breakdown voltage, can be used to compare qualitatively the residual damages left after different annealing stages. The decreases in t_i and V_{BD} with increasing anneal temperature indicate that lattice disorder is being annealed out progressively. Fig. 4.5 shows the percentage damage of another identically implanted sample at different annealing temperatures by backscattering method[25]. The reverse annealing behaviour from 1000°C to 1200°C observed is not found in the present electrical study.

(e) The existence of an n-type region under the surface after high temperature anneals is evident by the N_D values obtained. For comparison of the measured donor concentration with the nitrogen concentration, the range distribution of nitrogen in SiC was constructed using the range moments extracted from the tables of Winterbon[26]. This distribution for nitrogen implant conditions of $10^{16}/cm^2$ at 25 KeV and $10^{16}/cm^2$ at 45 KeV is shown in Fig. 4.6. The peak concentration can be seen to be $3*10^{21}$ N-atoms/cm^3. The measured donor concentration should be compared to the calculated

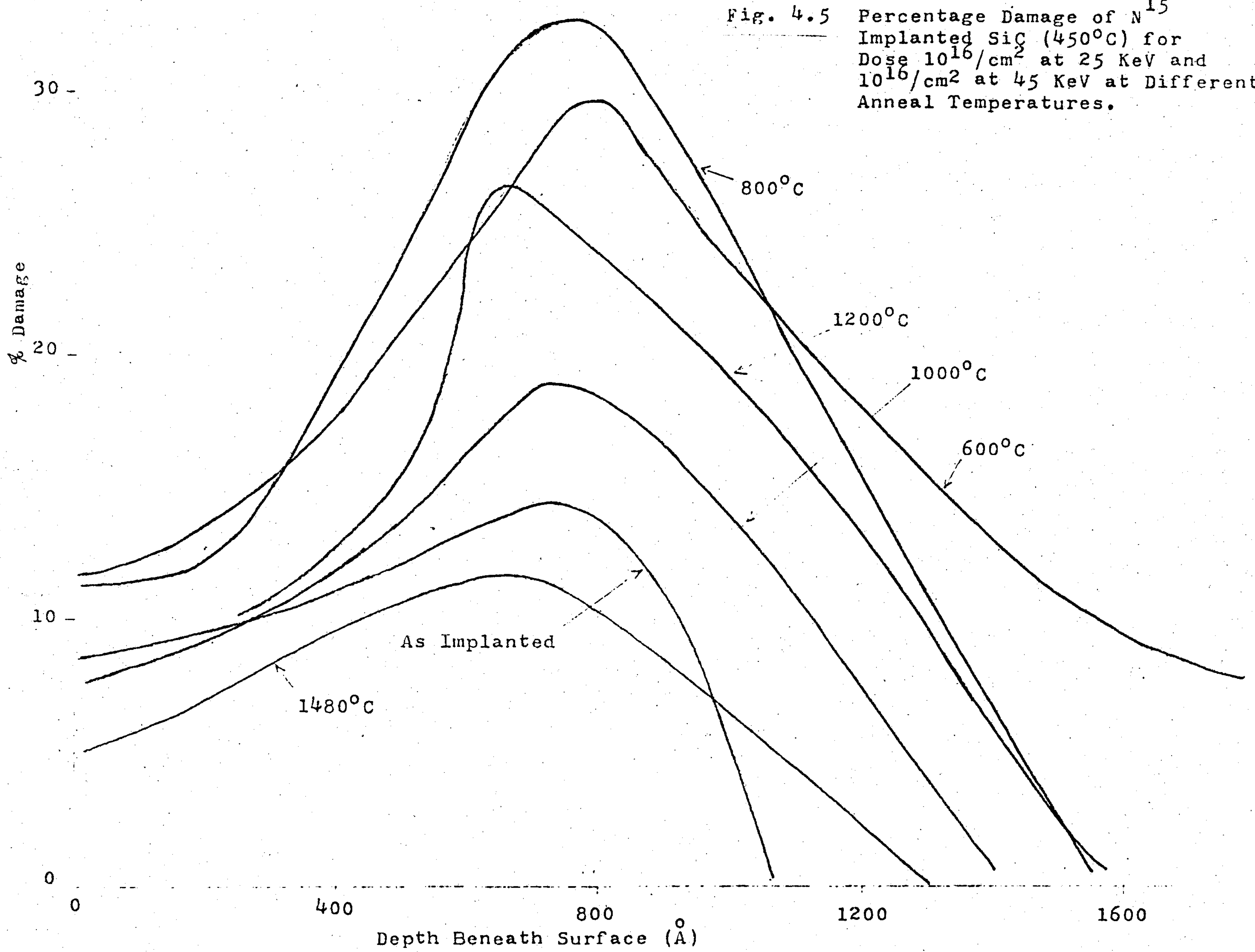


Fig. 4.5 Percentage Damage of N^{15} Implanted SiC (450°C) for Dose $10^{16}/cm^2$ at 25 KeV and $10^{16}/cm^2$ at 45 KeV at Different Anneal Temperatures.

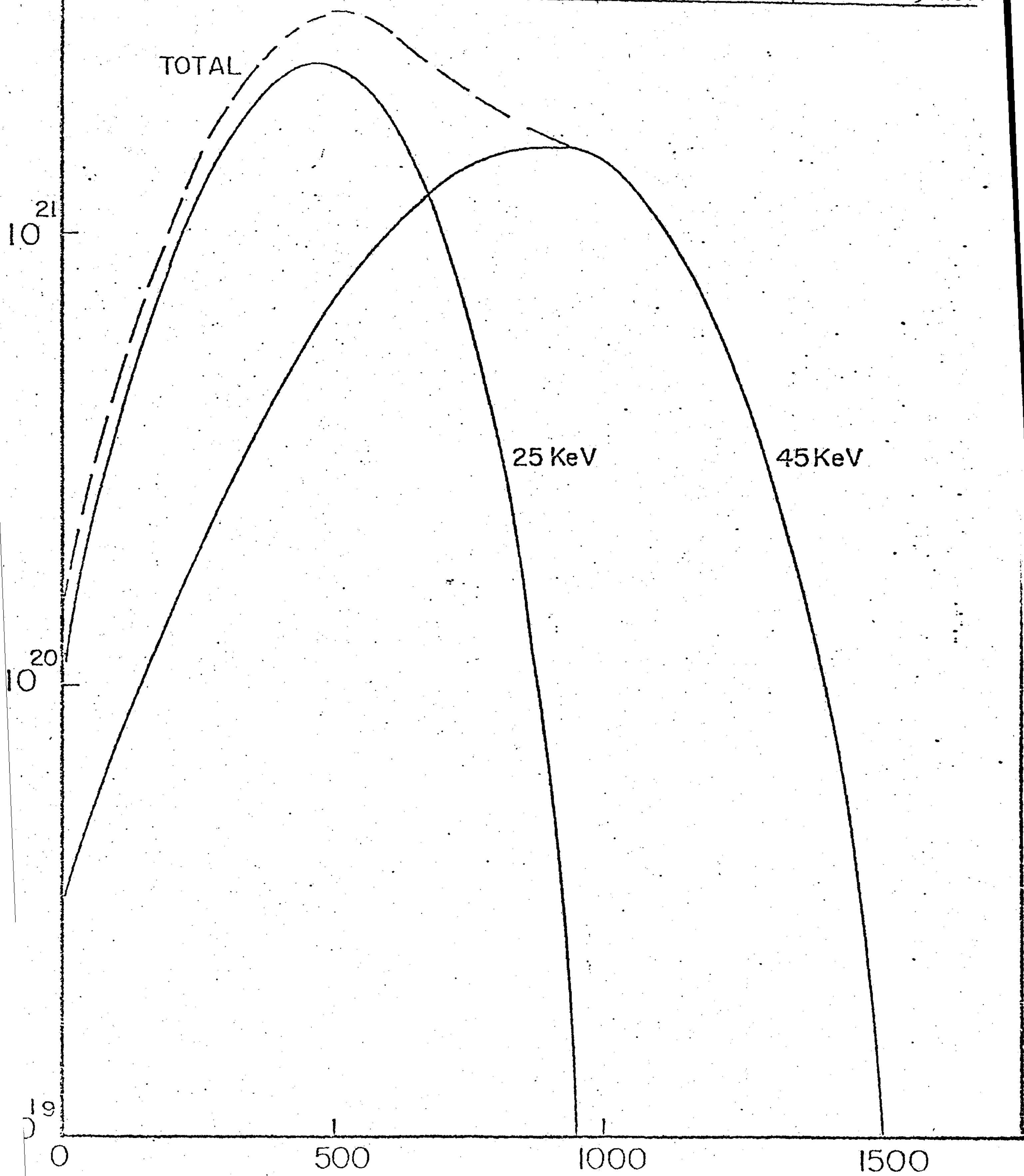


Fig. 4.6 Nitrogen Distribution in SiC for Dose $10^{16}/cm^2$ at 25 KeV and $10^{16}/cm^2$ at 45 KeV.

average nitrogen concentration in a surface layer corresponding to the depletion depth of 100 Å into an N-type layer with a donor concentration of $8\times10^{19}/cm^3$. Therefore assuming an average nitrogen concentration in the first 100 Å beneath the N-type surface of $2.5\times10^{20}/cm^3$, an electrically active donor conversion efficiency of 20-30% is observed. This is somewhat lower than the measured "substitutional" percentage and the 50% electrical activity following 1400°C annealing, observed by Marsh and Dunlap[5]. However, it should be noted that Marsh and Dunlap's results were for implant concentrations an order of magnitude lower than in this study, which would result in lower damage levels, hence better annealing.

The reason for the sudden drop in N_D for SiC-2-010 after 1480°C anneal is not known. However, it is believed that this is probably resulted from experimental discrepency rather than a general annealing behaviour as such drop is not observed in the other sample.

(f) The structural changes at different annealing temperatures can be deduced qualitatively from the voltage intercepts of the $1/C^2$ vs V_A plots. V_b will be large for MIS structures or n-i-p structures with thick insulating layers. When the thickness of the insulator region decreases, V_b will decrease correspondingly, and approach V_{bi}, the build-in junction voltage when a good n-p junction is formed.

In Table 4.2, values of V_{bi} at room temperature are listed for different values of N_D. Where N_A is assumed to be $2\times10^{18}/cm^3$, N_i equals $2\times10^{-5}/cm^3$. Eqn. (3.5) is used.

Table 4.2
Built-in Voltage of SiC p-n junction
for different N_D values at room temperature.

N_D	$10^{19}/cm^3$	$5 \times 10^{19}/cm^3$	$8 \times 10^{19}/cm^3$	$10^{20}/cm^3$
V_{bi}	2.445V	2.546V	2.559V	2.564V

Comparing with values listed in Table 4.2, it can be seen that after 1480°C anneal, SiC-2-010 results in a pretty good n-p junction, although the presence of an i region is still evident. This can be compared with Dunlap and Marsh's result on room temperature implant with a lower dose(5), they also found a rather good p-n junction after 1500°C anneal. SiC-2-006, on the other hand, still behaves as an n-i-p structure.

(g) After 1400°C anneal, SiC-2-006 shows a strange C-V behaviour (Fig. 4.7) which can hot be explained by the model discussed in Section 3.5. Only region E (Fig. 3.6) can be identified and it gives a reasonable N_D value.

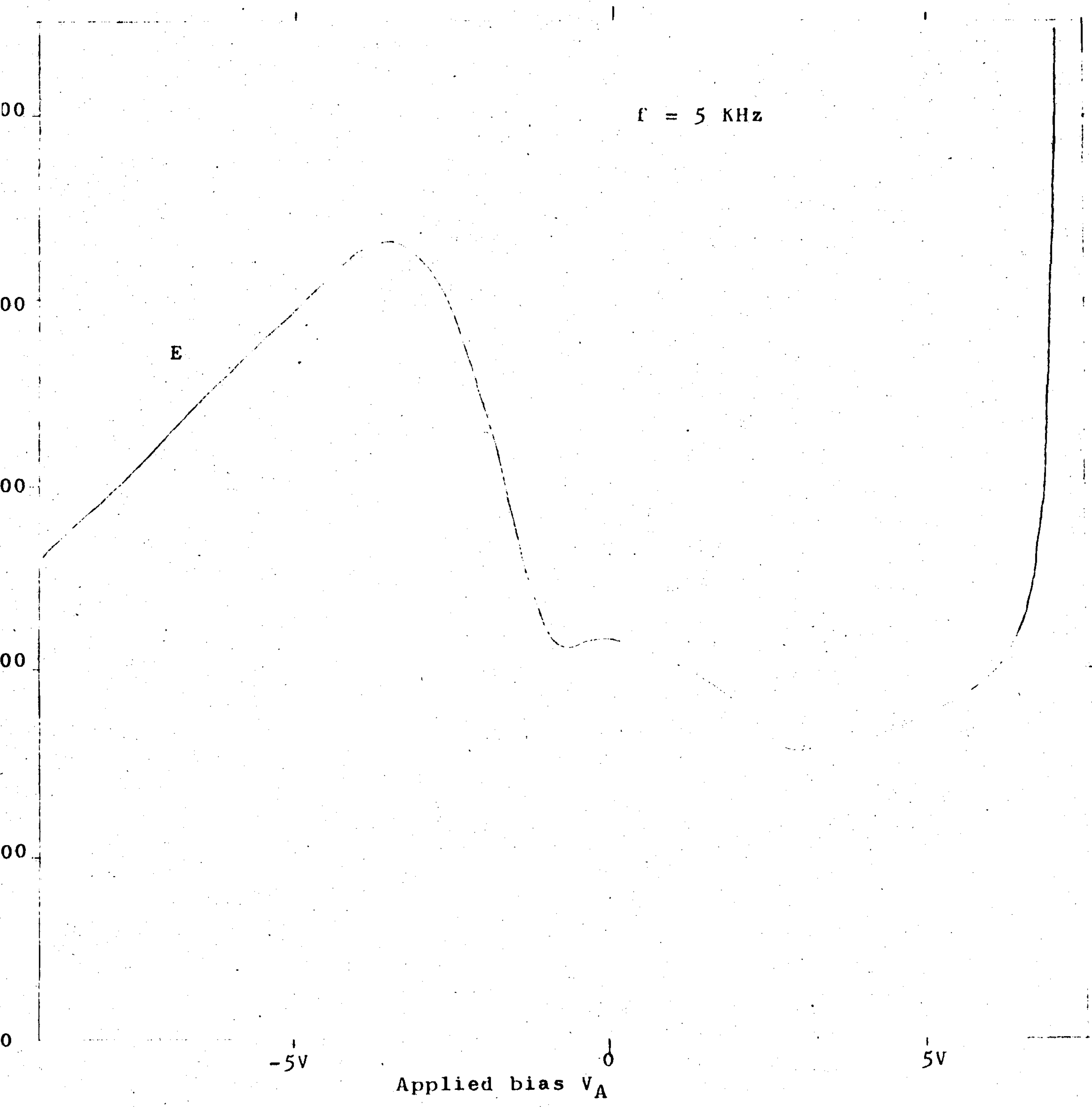


Fig. 4.7 C-V Curve of SiC-2-006 After 1400°C Anneal

CHAPTER 5

CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

5.1 Conclusions

6H, α-type, aluminum doped SiC crystals, doubly implanted with ^{15}N ions at 45 KeV and 25 KeV to a dose of $2 \times 10^{16}/cm^2$ at a substrate temperature of 450^oC have been investigated by measuring the C-V curves at different annealing temperatures.

The annealing behaviour can best be summarized by plotting $1/C^2$ vs V_A as shown in Figures 5.1 and 5.2 for SiC-2-010 and SiC-2-006 respectively.

The lattice damage of the implanted region is persistingly high up to an anneal temperature of 1000^oC. After 1000^oC anneal, an n-i-p structure is observed. A fairly good n-p junction is obtained after 1480^oC anneal.

Existence of a buried damage region is evident after 1000^oC anneal. This insulating region decreases in thickness with increasing anneal temperature.

About 20-30% of the implanted nitrogen ions are found to be electrically active.

The junction depth deduced from the C-V curves is found to be in good agreement with theoretical prediction and with the experimental value estimated from damage study.

Capacitance is found to be subject to large variations in measuring frequency.

Redistribution of substrate acceptor concentration is observed near the implanted region. The measured acceptor level agrees well with the manufacturer's supplied value.

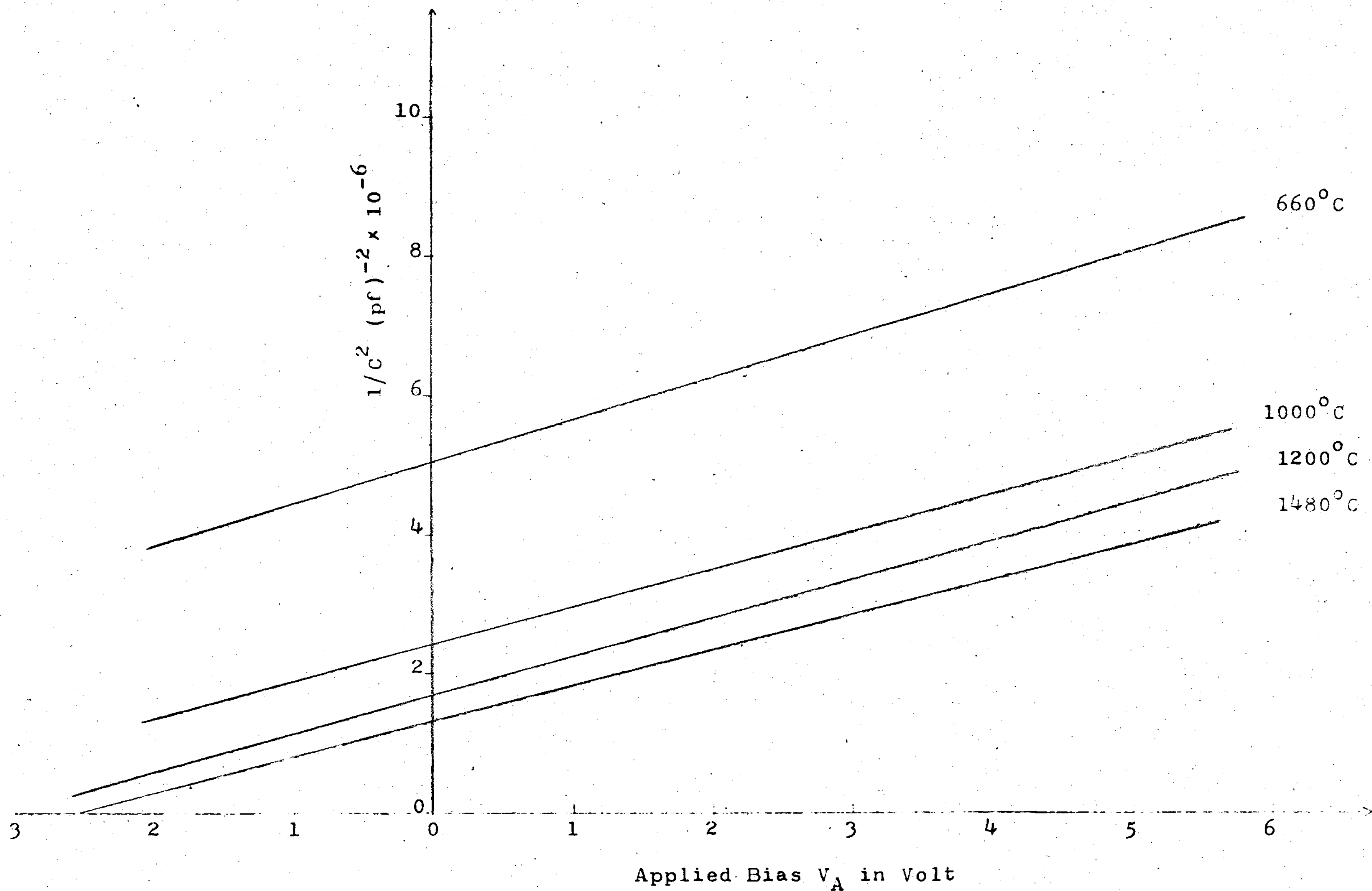


Fig. 5.1 $1/C^2$ vs V_A Plot for SiC-2-010 at Different Annealing Temperatures.

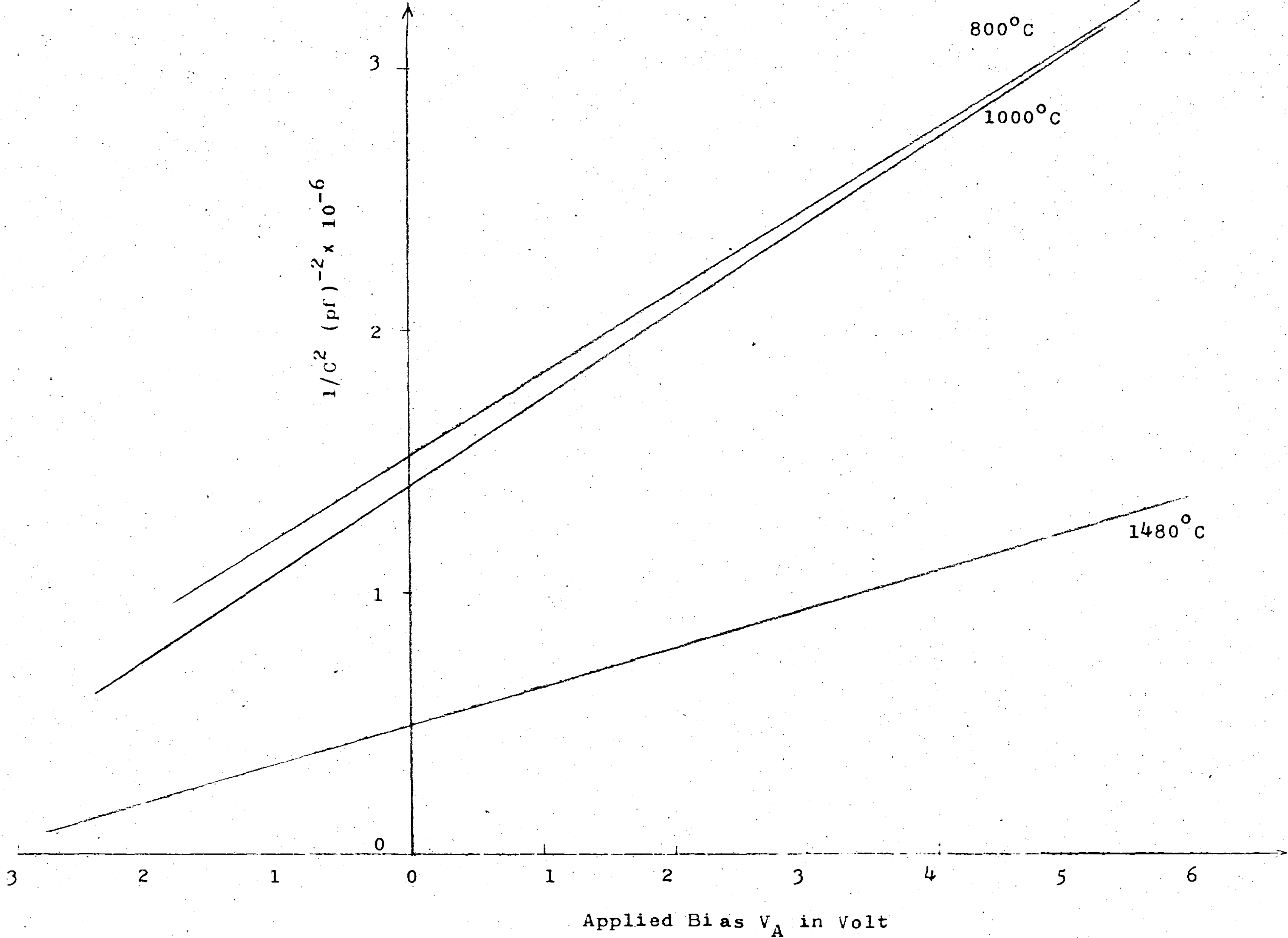


Fig. 5.2 $1/C^2$ vs V_A Plot for SiC-2-006 at Different Annealing Temperatures.

5.2 Suggestions for Further Work

Ion implantation has been shown to be a feasible process for junction formation. The main problem involved is the residual damage left in the crystal after implantation. Most of the damage has been shown to have been annealed out at reasonable high temperatures. However, more work has to be done to fill the many blanks still existing.

As a continuation of the present study, a few suggestions for future work are listed below.

(i) A fairly good p-n junction has been obtained after 1480°C anneal. It is believed that lattice damage can be annealed out completely and a good p-n junction can be formed at still higher annealing temperatures. Work can be done to prove this.

(ii) Although the general annealing behaviours are found to be the same for both samples studied here, large difference appears in junction depths measured. Also a higher annealing temperature is needed for SiC-2-006 to achieve a measurable type conversion and a relatively better p-n junction is obtained for SiC-2-010 after 1480°C anneal. Work can be done to clarify these differences by repeating the experiment with more samples.

(iii) As a complement to the present work, the I-V characteristic can be studied after the 1480°C anneal to confirm the conclusion made here that a pretty good p-n junction has been obtained. Prior to this, method to form low resistance ohmic contacts to both faces of the sample has to be found.

(iv) Work can be directed to find the implanting conditions best suited for p-n junction formation. This can be done by

using samples implanted with different doses and energies at different substrate temperatures, probably higher temperatures and lower doses.

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APPENDIX

```
      PROGRAM TST (INPUT,OUTPUT,TAPE5=INPUT,TAPE6=OUTPUT)
C
C   ** THIS PROGRAM GENERATES IDEAL MOS C-V CURVES FOR BOTH N-TYPE
C   ** AND P-TYPE SEMICONDUCTORS
C   ** IT WAS FIRST PREPARED BY H.B. LO OF CANADIAN WESTINGHOUSE
C   ** HERE IS A MODIFIED VERSION PREPARED BY M.C.CHAN
C   ** THIS PROGRAM IS COMPLETELY GENERAL, IT CAN BE USED FOR ANY
C   ** EXTRINSIC SLC., ENTER THE APPROPRIATE NA,ND,KS,KO,TOX,NI,AR,KT
C   ** THIS PROGRAM IS WRITTEN WITH EO=554000Q/VCM
C   ** TOX IN AMGSTROMS, AR IN SQ CM, KT IN EV, NA,ND,NI IN/CUBIC CM.,
C   ** WATCH FOR ORDERS OF NA,ND,NI, CHANGE STATEMENTS 01,02,03 IF
C   ** NECESSARY
C   ** DOT-- LOW FREQ. RESPONDS
C   ** PLUS -- HIGH FREQ. RESPONDS
C   ** STAR -- DEPLETION APPROX.
C   ** FOR P-TYPE SLC., ENTER CODE=1
C   ** FOR N-TYPE SLC., ENTER CODE=2
C   ** MODE=1, GENERATES LOW FREQ. RESPONDS
C   ** MODE=2, GENERATES HIGH FREQ. RESPONDS
C   ** MODE=3, GENERATES DEPLETION APPROX.
C   ** MODE=4, GENERATES ALL THREE CURVES
C   ** PROGRAM STOPS WHEN CODE READS 9
C
      DIMENSION VAP(500),CC1(500),CC2(500),CC3(500),TITLE(80)
      REAL ND,NA,KO,KS,NI,KT,NPO,NNO,LO,AR
      INTEGER CODE
      J1=5
      J2=6
   99 READ(J1,51) CODE
   51 FORMAT(1I1)
      IF(CODE.EQ.9) GO TO 340
      READ(J1,23) TITLE
   23 FORMAT(80A1)
   18 READ(J1,20) NA,ND,KO,KS,TOX,NI,AR
   20 FORMAT(7F10.0)
      READ(J1,19) USMIN,USMAX,KT,MODE
   19 FORMAT(3F10.0,I1)
      READ(J1,231) BLANK,DOT,PLUS,STAR
  231 FORMAT(4A1)
   01 NA=NA*1.E+15
   02 ND=ND*1.E+15
   03 NI=NI*1.E-6
      EO=554000
      Q=1.6*1.E-19
C*****CONVERT TOX INTO CM
  700 TOX=TOX*1.E-8
  500 COX=KO*AR*(8.854*1.E-8)/TOX
C*****COX GIVEN IN MICRO F.
      GO TO 601
  600 NA=NA/10.0
      COX=COX*AR
  601 WRITE(J2,233)
  233 FORMAT(1H1)
      WRITE(J2,23) TITLE
      WRITE(J2,230) NA,ND,KO,KS,KT,NI
  230 FORMAT(5X,4HNA =,E10.3,/5X,4HND =,E10.3,/5X,4HKO =,E10.3,/5X,4HKS
     1=,E10.3,/5X,4HKT =,E10.3/5X,4HNI =,E10.3/)
```

```
      WRITE(J2,232) TOX,COX
  232 FORMAT(5X,5HTOX =,E10.3,/5X,5HCOX =,E10.3///)
      COX=COX/AR
C*****COX GIVEN IN MICRO F./SQ.CM.
      MM=100
      KK=1
      IF(CODE.EQ.2) GO TO 80
      US=USMIN
      SUM=0.0
      UF=ALOG(NA/NI)
      DU=(US-UF)/100.0
      USOLD=UF
   21 PPO=NI*EXP(UF)
      NPO=NI*EXP(-UF)
      LD=SQRT(2.0*KT*KS*EO/PPO)/Q
      CC=SQRT((EXP(-US)+US-1.0)+NPO/PPO*(EXP(US)-US-1.0))
      IF(US.GE.0.0) QS=-2.0*KS*EO*KT*CC/(LD*Q)
      IF(US.LE.0.0) QS=2.0*KS*EO*KT*CC/(LD*Q)
      PHIS=KT*US
      VAPP=PHIS-QS/(6.25*1.E+12)/COX
      VAP(KK)=VAPP
      IF(MODE.EQ.2) GO TO 401
      IF(MODE.EQ.3) GO TO 402
      IF(ABS(US).GT.1.5) CSLF=KS*EO*(1.0-EXP(-US)+NPO/PPO*(EXP(US)-1.0))
     1/(CC*LD*Q)
      IF(ABS(US).GT.1.5.AND.US.LE.0.0) CSLF=-CSLF
      IF(ABS(US).LE.1.5) CALL CALCAP(CODE,US,NPO,PPO,LD,KT,KS,EO,CSLF)
      CSLF=CSLF/(6.25*1.E+12)
      CLF=1.0/(1.0/COX+1.0/CSLF)
      CLFN=CLF/COX
      CC1(KK)=CLFN
      IF(MODE.EQ.1) GO TO 100
  401 COUNT=1.0
      DO 22 K=1,MM
      U=USOLD+(COUNT-0.5)*DU
      AA=EXP(U-UF)/SQRT((EXP(-U)+U-1.0)+NPO/PPO*(EXP(U)-U-1.0))
      BB=AA*ABS(DU)
      SUM=SUM+BB
      COUNT=COUNT+1.0
   22 CONTINUE
      IF(US.GE.0.0) QN=-SUM*NI*LD*Q/2.0
      IF(US.LE.0.0) QN=SUM*NI*LD*Q/2.0
      XD=(QS-QN)/(ND-NA)
      IF(XD.LE.0.0) XD=0.0
      CHF=COX/(1.0+KO*XD/(TOX*KS))
      CHFN=CHF/COX
      CC2(KK)=CHFN
      IF(MODE.EQ.2) GO TO 100
  402 IF(VAPP.LE.0.0) CDEP=COX
      IF(VAPP.GE.0.0) CDEP=COX/SQRT(1.0+2.0*KO**2*EO*VAPP/((NA-ND)*KS*TO
     1X**2))
      CDEPN=CDEP/COX
      CC3(KK)=CDEPN
  100 IF(US.GT.USMAX) GO TO 200
      USOLD=US
      US=US+0.5
      DU=0.025
```

```
      MM=20
      KK=KK+1
      GO TO 21
   80 US=USMAX
      SUM=0.0
      UF=-ALOG(ND/NI)
      DU=(US-UF)/100.0
      USOLD=UF
   71 NNO=NI*EXP(-UF)
      PNO=NI*EXP(UF)
      LD=SQRT(2.0*KT*KS*EO/NNO)/Q
      CC=SQRT((EXP(US)-US-1.0)+PNO/NNO*(EXP(-US)+US-1.0))
      IF(US.GE.0.0) QS=-2.0*KS*EO*KT*CC/(LD*Q)
      IF(US.LE.0.0) QS=2.0*KS*EO*KT*CC/(LD*Q)
      PHIS=KT*US
      VAPP=PHIS-QS/(6.25*1.E+12)/COX
      VAP(KK)=VAPP
      IF(MODE.EQ.2) GO TO 720
      IF(MODE.EQ.3) GO TO 721
      IF(ABS(US).GT.1.5) CSLF=KS*EO*(EXP(US)-1.0+PNO/NNO*(1.0-EXP(-US)))
     1/(CC*LD*Q)
      IF(ABS(US).GT.1.5.AND.US.LE.0.0) CSLF=-CSLF
      IF(ABS(US).LE.1.5) CALL CALCAP(CODE,US,PNO,NNO,LD,KT,KS,EO,CSLF)
      CSLF=CSLF/(6.25*1.E+12)
      CLF=1.0/(1.0/COX+1.0/CSLF)
      CLFN=CLF/COX
      CC1(KK)=CLFN
      IF(MODE.EQ.1) GO TO 800
  720 COUNT=1.0
      DO 88 K=1,MM
      U=USOLD+(COUNT-0.5)*DU
      AA=EXP(UF-U)/SQRT((EXP(U)-U-1.0)+PNO/NNO*(EXP(-U)+U-1.0))
      BB=AA*ABS(DU)
      SUM=SUM+BB
      COUNT=COUNT+1.0
   88 CONTINUE
      IF(US.GE.0.0) QP=-SUM*NI*LD*Q/2.0
      IF(US.LE.0.0) QP=SUM*NI*LD*Q/2.0
      XD=(QS-QP)/(ND-NA)
      IF(XD.LE.0.0) XD=0.0
      CHF=COX/(1.0+KO*XD/(TOX*KS))
      CHFN=CHF/COX
      CC2(KK)=CHFN
      IF(MODE.EQ.2) GO TO 800
  721 IF(VAPP.GE.0.0) CDEP=COX
      IF(VAPP.LE.0.0) CDEP=COX/SQRT(1.0+2.0*KO**2*EO*VAPP/((NA-ND)*KS*TO
     1X**2))
      CDEPN=CDEP/COX
      CC3(KK)=CDEPN
  800 IF(US.LT.USMIN) GO TO 200
      USOLD=US
      US=US-0.5
      DU=-0.025
      MM=20
      KK=KK+1
      GO TO 71
  200 CSDB=1.414*KS*EO/(LD*Q)
```

```
      CSDB=CSDB/(6.25*1.E+12)
      CDBN=1.0/(COX/CSDB+1.0)
      WRITE(J2,201) CDBN
  201 FORMAT(///5X,27HNORMALIZED FLAT BAND CAP = ,E12.3///)
      IF(CODE.EQ.2) GO TO 98
      VMIN=VAP(1)
      VMAX=VAP(KK)
      IF(ABS(VMIN).GT.20.0) VMIN=-20.0
      IF(VMAX.GT.30.0) VMAX=30.0
      GO TO 220
   98 VMIN=VAP(KK)
      VMAX=VAP(1)
      IF(ABS(VMIN).GT.30.0) VMIN=-30.0
      IF(VMAX.GT.20.0) VMAX=20.0
  220 CALL PLOTCV(CODE,MODE,KK,DOT,STAR,PLUS,BLANK,VAP,CC1,CC2,CC3,
     1VMIN,VMAX)
      GO TO 99
  340 STOP
      END
```

C REFERENCE MAP (R=1)

```
SN  TYPE               RELOCATION
   REAL                                    5226  AR        REAL
   REAL                                    5236  BLANK     REAL
   REAL                                    6271  CC1       REAL       ARRAY
   REAL        ARRAY                      10241  CC3       REAL       ARRAY
   REAL                                    5275  CDEP      REAL
   REAL                                    5273  CHF       REAL
   REAL                                    5262  CLF       REAL
   REAL                                    5227  CODE      INTEGER
   REAL                                    5244  COX       REAL
   REAL                                    5261  CSLF      REAL
   REAL                                    5252  DU        REAL
   REAL                                    5230  J1        INTEGER
   INTEGER                                 5265  K         INTEGER
   INTEGER                                 5217  KO        REAL
   REAL                                    5222  KT        REAL
   REAL                                    5245  MM        INTEGER
   INTEGER                                 5216  NA        REAL
   REAL                                    5221  NI        REAL
   REAL                                    5223  NPO       REAL
   REAL                                    5240  PLUS      REAL
   REAL                                    5254  PPO       REAL
   REAL                                    5271  QN        REAL
   REAL                                    5256  QS        REAL
   REAL                                    5250  SUM       REAL
   REAL        ARRAY                       5232  TOX       REAL
   REAL                                    5251  UF        REAL
   REAL                                    5234  USMAX     REAL
   REAL                                    5253  USOLD     REAL
   REAL        ARRAY                       5260  VAPP      REAL
   REAL                                    5303  VMIN      REAL
   REAL
```

```
      SUBROUTINE CALCAP(CODE,US,XY,XX,LD,KT,KS,EO,CSLF)
C  ** THIS SUBROUTINE CALCULATES THE LOW FREQUENCY MOS CAPACITANCE
C  ** IN THE VICINITY OF ZERO SURFACE POTENTIAL
      REAL LD,KT,KS
      INTEGER CODE
      Q=1.6*1.E-19
      TERM1=ABS(US)/6.0
      SUM1=TERM1
      COUNT=4.0
      DO 30 K=1,10
      TERM1=TERM1*(ABS(US)**2)/((COUNT+1.0)*COUNT)
      SUM1=SUM1+TERM1
      COUNT=COUNT+2.0
   30 CONTINUE
      TERM2=ABS(US)**2/24.0
      SUM2=TERM2
      COUNT=5.0
      DO 31 K=1,10
      TERM2=TERM2*(ABS(US)**2)/((COUNT+1.0)*COUNT)
      SUM2=SUM2+TERM2
      COUNT=COUNT+2.0
   31 CONTINUE
      IF(US.LE.0.0) SUM1=-SUM1
      IF(CODE.EQ.1) SUM11=SQRT(0.5-SUM1+SUM2+XY/XX*(0.5+SUM1+SUM2))
      IF(CODE.EQ.2) SUM11=SQRT(0.5+SUM1+SUM2+XY/XX*(0.5-SUM1+SUM2))
      TERM3=ABS(US)/12.0
      SUM3=TERM3
      COUNT=5.0
      DO 32 K=1,10
      TERM3=TERM3*ABS(US)**2*(COUNT-1.0)/((COUNT+1.0)*COUNT)
      SUM3=SUM3+TERM3
      COUNT=COUNT+2.0
   32 CONTINUE
      TERM4=ABS(US)**2/40.0
      SUM4=TERM4
      COUNT=6.0
      DO 33 K=1,10
      TERM4=TERM4*ABS(US)**2*(COUNT-1.0)/((COUNT+1.0)*COUNT)
      SUM4=SUM4+TERM4
      COUNT=COUNT+2.0
   33 CONTINUE
      IF(US.LE.0.0) SUM3=-SUM3
      IF(CODE.EQ.1) SUM22=0.5*US/SUM11*(-1.0/6.0+SUM3-SUM4+XY/XX*(1.0
     1/6.0+SUM3+SUM4))
      IF(CODE.EQ.2) SUM22=0.5*US/SUM11*(1.0/6.0+SUM3+SUM4+XY/XX*(-1.0
     1/6.0+SUM3-SUM4))
      SUMT=SUM11+SUM22
      CSLF=2.0*KS*EO/(LD*Q)*SUMT
      RETURN
      END
```

```
      SUBROUTINE PLOTCV(CODE,MODE,MPOINT,DOT,STAR,PLUS,BLANK,VAP,CC1,
     1CC2,CC3,VMIN,VMAX)
C*****POINT BY POINT PLOT SUBROUTINE
      DIMENSION VAP(500),CC1(500),CC2(500),CC3(500),VV(150),CAPL(150)
     1,CAPH(150),CAPD(150),YA(150)
      INTEGER CODE
      J2=6
      VV(1)=VMIN
      VV(101)=VMAX
      VINCR=(VMAX-VMIN)/100.0
      COUNT=1.0
      DO 20 K=2,100
      VV(K)=VMIN+COUNT*VINCR
      COUNT=COUNT+1.0
   20 CONTINUE
      WRITE(J2,28)
   28 FORMAT(//5X,21HRESULTS FROM C-V PLOT/)
      IF(MODE.EQ.1) WRITE(J2,411)
      IF(MODE.EQ.2) WRITE(J2,412)
      IF(MODE.EQ.3) WRITE(J2,413)
      IF(MODE.EQ.4) WRITE(J2,414)
  411 FORMAT(10X,16HVAPP        CLFN/)
  412 FORMAT(10X,16HVAPP        CHFN/)
  413 FORMAT(10X,17HVAPP        CDEPN/)
  414 FORMAT(10X,41HVAPP        CLFN         CHFN           CDEPN/)
      MS=1
      MP=MPOINT-1
      IF(CODE.EQ.2) GO TO 50
      DO 21 K=1,101
      DO 22 MM=MS,MP
      MN=MM+1
      IF(VV(K).GE.VAP(MM).AND.VV(K).LE.VAP(MN)) GO TO 25
   22 CONTINUE
   25 FACTOR=(VV(K)-VAP(MM))/(VAP(MN)-VAP(MM))
      IF(MODE.EQ.1.OR.MODE.EQ.4) CAPL(K)=CC1(MM)-(CC1(MM)-CC1(MN))*
     1FACTOR
      IF(MODE.EQ.2.OR.MODE.EQ.4) CAPH(K)=CC2(MM)-(CC2(MM)-CC2(MN))*
     1FACTOR
      IF(MODE.EQ.3.OR.MODE.EQ.4) CAPD(K)=CC3(MM)-(CC3(MM)-CC3(MN))*
     1FACTOR
      MS=MM
   21 CONTINUE
      DO 31 K=1,101
      IF(MODE.EQ.1) GO TO 800
      IF(MODE.EQ.2) GO TO 801
      IF(MODE.EQ.3) GO TO 802
      IF(MODE.EQ.4) GO TO 803
  800 WRITE(J2,510) VV(K),CAPL(K)
  510 FORMAT(5X,2E12.3)
      GO TO 31
  801 WRITE(J2,511) VV(K),CAPH(K)
  511 FORMAT(5X,2E12.3)
      GO TO 31
  802 WRITE(J2,512) VV(K),CAPD(K)
  512 FORMAT(5X,2E12.3)
      GO TO 31
  803 WRITE(J2,513) VV(K),CAPL(K),CAPH(K),CAPD(K)
```

```
  513 FORMAT(5X,4E12.3)
   31 CONTINUE
      IF(MODE.EQ.1) GO TO 420
      IF(MODE.EQ.2) CMIN=CAPH(101)
      IF(MODE.EQ.3.OR.MODE.EQ.4) CMIN=CAPD(101)
      GO TO 60
  420 DO 421 K=2,100
      M=K-1
      N=K+1
      IF(CAPL(K).LT.CAPL(M).AND.CAPL(K).LT.CAPL(N)) GO TO 422
  421 CONTINUE
  422 CMIN=CAPL(K)
      GO TO 60
   50 K=102
      DO 81 M=1,101
      K=K-1
      DO 82 MM=MS,MP
      MN=MM+1
      IF(VV(K).LE.VAP(MM).AND.VV(K).GE.VAP(MN)) GO TO 85
   82 CONTINUE
   85 FACTOR=(VAP(MM)-VV(K))/(VAP(MM)-VAP(MN))
      IF(MODE.EQ.1.OR.MODE.EQ.4) CAPL(K)=CC1(MM)-(CC1(MM)-CC1(MN))*
     1FACTOR
      IF(MODE.EQ.2.OR.MODE.EQ.4) CAPH(K)=CC2(MM)-(CC2(MM)-CC2(MN))*
     1FACTOR
      IF(MODE.EQ.3.OR.MODE.EQ.4) CAPD(K)=CC3(MM)-(CC3(MM)-CC3(MN))*
     1FACTOR
      MS=MM
   81 CONTINUE
      DO 91 K=1,101
      IF(MODE.EQ.1) GO TO 507
      IF(MODE.EQ.2) GO TO 508
      IF(MODE.EQ.3) GO TO 509
      IF(MODE.EQ.4) GO TO 600
  507 WRITE(J2,901) VV(K),CAPL(K)
  901 FORMAT(5X,2E12.3)
      GO TO 91
  508 WRITE(J2,902) VV(K),CAPH(K)
  902 FORMAT(5X,2E12.3)
      GO TO 91
  509 WRITE(J2,903) VV(K),CAPD(K)
  903 FORMAT(5X,2E12.3)
      GO TO 91
  600 WRITE(J2,904) VV(K),CAPL(K),CAPH(K),CAPD(K)
  904 FORMAT(5X,4E12.3)
   91 CONTINUE
      IF(MODE.EQ.1) GO TO 440
      IF(MODE.EQ.2) CMIN=CAPH(1)
      IF(MODE.EQ.3.OR.MODE.EQ.4) CMIN=CAPD(2)
      GO TO 60
  440 DO 441 K=2,100
      M=K-1
      N=K+1
      IF(CAPL(K).LT.CAPL(M).AND.CAPL(K).LT.CAPL(N)) GO TO 442
  441 CONTINUE
  442 CMIN=CAPL(K)
   60 COUNT=0.9
```

```
      DO 35 K=1,10
      IF(CMIN.GT.COUNT) GO TO 36
      COUNT=COUNT-0.1
   35 CONTINUE
   36 WRITE(J2,33)
   33 FORMAT(///5X,45HAXIS GOING FROM LEFT TO RIGHT-NORMALIZED CAP,/)
      WRITE(J2,34)
   34 FORMAT(5X,41HAXIS GOING DOWN-GATE APPLIED VOLTAGE VAPP//)
      IF(K.EQ.1) WRITE(J2,301)
      IF(K.EQ.2) WRITE(J2,302)
      IF(K.EQ.3) WRITE(J2,303)
      IF(K.EQ.4) WRITE(J2,304)
      IF(K.EQ.5) WRITE(J2,305)
      IF(K.EQ.6) WRITE(J2,306)
      IF(K.EQ.7) WRITE(J2,307)
      IF(K.EQ.8) WRITE(J2,308)
      IF(K.EQ.9) WRITE(J2,309)
      IF(K.EQ.10) WRITE(J2,310)
  301 FORMAT(10X,63H0.9
     1        1.0)
  302 FORMAT(10X,63H0.8                              0.9
     1        1.0)
  303 FORMAT(10X,63H0.7                    0.8                  0.9
     1        1.0)
  304 FORMAT(10X,63H0.6          0.7            0.8            0.9
     1        1.0)
  305 FORMAT(10X,63H0.5     0.6         0.7         0.8         0.9
     1        1.0)
  306 FORMAT(10X,63H0.4    0.5        0.6        0.7        0.8        0.
     19       1.0)
  307 FORMAT(10X,63H0.3                              0.65
     1        1.0)
  308 FORMAT(10X,63H0.2          0.4                0.6            0.8
     1        1.0)
  309 FORMAT(10X,63H0.1                    0.4                  0.7
     1        1.0)
  310 FORMAT(10X,63H0.0                              0.5
     1        1.0)
      DO 100 K=1,61
      YA(K)=DOT
  100 CONTINUE
      WRITE(J2,101) (YA(K),K=1,61)
  101 FORMAT(11X,61A1)
      DO 102 K=1,61
      YA(K)=BLANK
  102 CONTINUE
      YA(1)=DOT
      DO 105 K=1,101
      IF(MODE.EQ.1.OR.MODE.EQ.4) JJ=(CAPL(K)-COUNT)/(1.0-COUNT)*60.0+1.0
      IF(MODE.EQ.2.OR.MODE.EQ.4) JK=(CAPH(K)-COUNT)/(1.0-COUNT)*60.0+1.0
      IF(MODE.EQ.3.OR.MODE.EQ.4) JL=(CAPD(K)-COUNT)/(1.0-COUNT)*60.0+1.0
      IF(MODE.EQ.1.OR.MODE.EQ.4) YA(JJ)=DOT
      IF(MODE.EQ.2.OR.MODE.EQ.4) YA(JK)=PLUS
      IF(MODE.EQ.3.OR.MODE.EQ.4) YA(JL)=STAR
      WRITE(J2,104) VV(K),(YA(I),I=1,61)
  104 FORMAT(F11.2,61A1)
      IF(MODE.EQ.1.OR.MODE.EQ.4) YA(JJ)=BLANK
```

```
      IF(MODE.EQ.2.OR.MODE.EQ.4) YA(JK)=BLANK
      IF(MODE.EQ.3.OR.MODE.EQ.4) YA(JL)=BLANK
      YA(1)=DOT
  105 CONTINUE
  402 RETURN
      END
```

C REFERENCE MAP (R=1)

SN	TYPE		RELOCATION				
	REAL		F.P.	2223	CAPD	REAL	ARRAY
	REAL	ARRAY		1547	CAPL	REAL	ARRAY
	REAL	ARRAY	F.P.	0	CC2	REAL	ARRAY
	REAL	ARRAY	F.P.	1312	CMIN	REAL	
	INTEGER		F.P.	1303	COUNT	REAL	
	REAL		F.P.	1311	FACTOR	REAL	
	INTEGER			1315	JJ	INTEGER	
	INTEGER			1317	JL	INTEGER	
	INTEGER			1304	K	INTEGER	
	INTEGER			1307	MM	INTEGER	
	INTEGER			0	MODE	INTEGER	
	INTEGER			0	MPOINT	INTEGER	
	INTEGER			1314	N	INTEGER	
	REAL		F.P.	0	STAR	REAL	
	REAL	ARRAY	F.P.	1302	VINCR	REAL	
	REAL		F.P.	0	VMIN	REAL	
	REAL	ARRAY		2451	YA	REAL	ARRAY

ELS

	0	21		0
	704	28	FMT	221
FMT	1060	34	FMT	0
	256	50		451
	0	82		274
	0	100		1262
	1271	104	FMT	0
FMT	1135	302	FMT	1146
FMT	1170	305	FMT	1201
FMT	1223	308	FMT	1234
FMT	0	402	INACTIVE	725
FMT	735	413	FMT	741
	0	421		253
	0	441		447
	366	508		375
FMT	763	511	FMT	772
FMT	404	600		163
	201	802		210
FMT	1021	902	FMT	1030
FMT				

GTH 2736B 1502

P-TYPE SILICON CARBIDE
NA = .730E+18
ND = 0.
KO = .100E+02
KS = .100E+02
KT = .259E-01
NI = .195E-04

TOX = .540E-05
COX = .798E-03

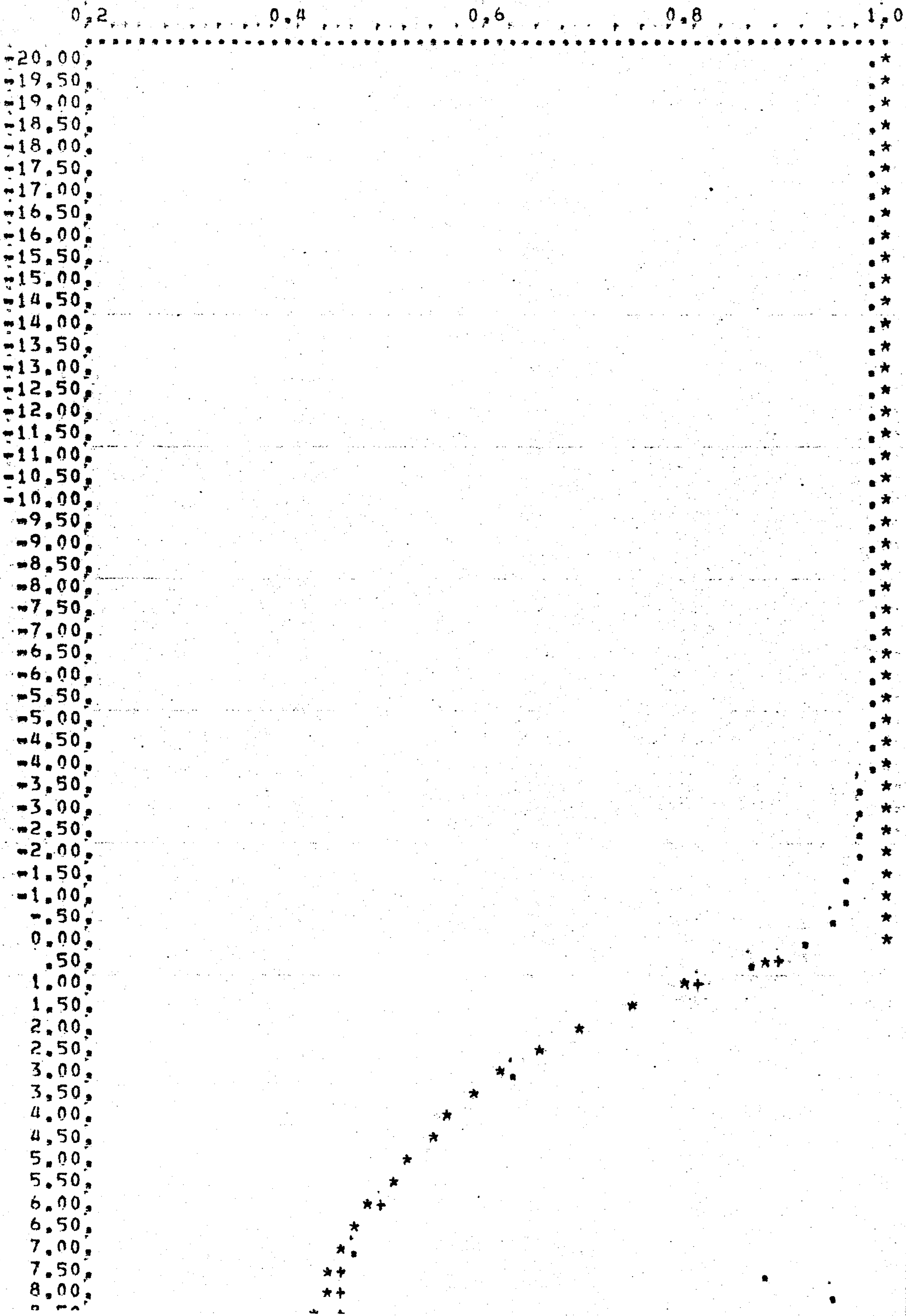
NORMALIZED FLAT BAND CAP = .924E+00

RESULTS FROM C-V PLOT

VAPP	CLFN	CHFN	CDEPN
-.200E+02	.997E+00	.100E+01	.100E+01
-.195E+02	.997E+00	.100E+01	.100E+01
-.190E+02	.997E+00	.100E+01	.100E+01
-.185E+02	.997E+00	.100E+01	.100E+01
-.180E+02	.997E+00	.100E+01	.100E+01
-.175E+02	.997E+00	.100E+01	.100E+01
-.170E+02	.997E+00	.100E+01	.100E+01
-.165E+02	.997E+00	.100E+01	.100E+01
-.160E+02	.997E+00	.100E+01	.100E+01
-.155E+02	.997E+00	.100E+01	.100E+01
-.150E+02	.997E+00	.100E+01	.100E+01
-.145E+02	.996E+00	.100E+01	.100E+01
-.140E+02	.996E+00	.100E+01	.100E+01
-.135E+02	.996E+00	.100E+01	.100E+01
-.130E+02	.996E+00	.100E+01	.100E+01
-.125E+02	.996E+00	.100E+01	.100E+01
-.120E+02	.996E+00	.100E+01	.100E+01
-.115E+02	.995E+00	.100E+01	.100E+01
-.110E+02	.995E+00	.100E+01	.100E+01
-.105E+02	.995E+00	.100E+01	.100E+01
-.100E+02	.995E+00	.100E+01	.100E+01
-.950E+01	.995E+00	.100E+01	.100E+01
-.900E+01	.994E+00	.100E+01	.100E+01
-.850E+01	.994E+00	.100E+01	.100E+01
-.800E+01	.993E+00	.100E+01	.100E+01
-.750E+01	.993E+00	.100E+01	.100E+01
-.700E+01	.993E+00	.100E+01	.100E+01
-.650E+01	.992E+00	.100E+01	.100E+01
-.600E+01	.991E+00	.100E+01	.100E+01
-.550E+01	.991E+00	.100E+01	.100E+01
-.500E+01	.990E+00	.100E+01	.100E+01
-.450E+01	.989E+00	.100E+01	.100E+01
-.400E+01	.987E+00	.100E+01	.100E+01
-.350E+01	.986E+00	.100E+01	.100E+01
-.300E+01	.984E+00	.100E+01	.100E+01
-.250E+01	.981E+00	.100E+01	.100E+01

-.500E+00	.950E+00	.100E+01	.100E+01
0.	.924E+00	.100E+01	.100E+01
.500E+00	.879E+00	.895E+00	.891E+00
.100E+01	.814E+00	.815E+00	.811E+00
.150E+01	.753E+00	.752E+00	.749E+00
.200E+01	.703E+00	.702E+00	.700E+00
.250E+01	.662E+00	.661E+00	.659E+00
.300E+01	.627E+00	.627E+00	.625E+00
.350E+01	.597E+00	.597E+00	.595E+00
.400E+01	.571E+00	.571E+00	.570E+00
.450E+01	.549E+00	.548E+00	.547E+00
.500E+01	.528E+00	.528E+00	.527E+00
.550E+01	.510E+00	.510E+00	.509E+00
.600E+01	.494E+00	.493E+00	.492E+00
.650E+01	.479E+00	.479E+00	.478E+00
.700E+01	.468E+00	.465E+00	.464E+00
.750E+01	.880E+00	.457E+00	.452E+00
.800E+01	.957E+00	.455E+00	.440E+00
.850E+01	.975E+00	.455E+00	.429E+00
.900E+01	.981E+00	.454E+00	.420E+00
.950E+01	.985E+00	.454E+00	.410E+00
.100E+02	.988E+00	.454E+00	.402E+00
.105E+02	.989E+00	.454E+00	.394E+00
.110E+02	.991E+00	.454E+00	.386E+00
.115E+02	.992E+00	.453E+00	.379E+00
.120E+02	.992E+00	.453E+00	.372E+00
.125E+02	.993E+00	.453E+00	.365E+00
.130E+02	.994E+00	.453E+00	.359E+00
.135E+02	.994E+00	.453E+00	.353E+00
.140E+02	.994E+00	.453E+00	.348E+00
.145E+02	.995E+00	.453E+00	.343E+00
.150E+02	.995E+00	.453E+00	.337E+00
.155E+02	.995E+00	.453E+00	.332E+00
.160E+02	.995E+00	.453E+00	.328E+00
.165E+02	.996E+00	.453E+00	.324E+00
.170E+02	.996E+00	.453E+00	.319E+00
.175E+02	.996E+00	.453E+00	.315E+00
.180E+02	.996E+00	.453E+00	.311E+00
.185E+02	.996E+00	.453E+00	.307E+00
.190E+02	.996E+00	.453E+00	.303E+00
.195E+02	.997E+00	.453E+00	.300E+00
.200E+02	.997E+00	.453E+00	.297E+00
.205E+02	.997E+00	.453E+00	.294E+00
.210E+02	.997E+00	.453E+00	.290E+00
.215E+02	.997E+00	.453E+00	.287E+00
.220E+02	.997E+00	.453E+00	.284E+00
.225E+02	.997E+00	.453E+00	.281E+00
.230E+02	.997E+00	.453E+00	.278E+00
.235E+02	.997E+00	.453E+00	.275E+00
.240E+02	.997E+00	.453E+00	.273E+00
.245E+02	.997E+00	.453E+00	.270E+00
.250E+02	.998E+00	.453E+00	.268E+00
.255E+02	.998E+00	.452E+00	.266E+00
.260E+02	.998E+00	.452E+00	.263E+00
.265E+02	.998E+00	.452E+00	.261E+00
.270E+02	.998E+00	.452E+00	.258E+00
.275E+02	.998E+00	.452E+00	.256E+00
.280E+02	.998E+00	.452E+00	.254E+00
.285E+02	.998E+00	.452E+00	.251E+00
.290E+02	.998E+00	.452E+00	.250E+00
.295E+02	.998E+00	.452E+00	.248E+00
.300E+02	.998E+00	.452E+00	.246E+00

AXIS GOING DOWN-GATE APPLIED VOLTAGE VAPP



```
   9.00,                         *    +                                        .
   9.50,                        *     +                                        .
  10.00,                        *     +                                        .
  10.50,                       *      +                                        .
  11.00,                      *       +                                        .
  11.50,                      *       +                                        .
  12.00,                     *       +                                         .
  12.50,                     *       +                                         .
  13.00,                    *        +                                         .
  13.50,                    *        +                                         .
  14.00,                    *        +                                         .
  14.50,                   *         +                                         .
  15.00,                   *         +                                         .
  15.50,                  *          +                                         .
  16.00,                  *          +                                         .
  16.50,                  *          +                                         .
  17.00,                 *           +                                         .
  17.50,                 *           +                                         .
  18.00,                 *           +                                         .
  18.50,                 *           +                                         .
  19.00,                *            +                                         .
  19.50,                *            +                                         .
  20.00,                *            +                                         .
  20.50,                *            +                                         .
  21.00,               *             +                                         .
  21.50,               *             +                                         .
  22.00,               *             +                                         .
  22.50,               *             +                                         .
  23.00,              *              +                                         .
  23.50,              *              +                                         .
  24.00,              *              +                                         .
  24.50,              *              +                                         .
  25.00,              *              +                                         .
  25.50,             *               +                                         .
  26.00,             *               +                                         .
  26.50,             *               +                                         .
  27.00,             *               +                                         .
  27.50,             *               +                                         .
  28.00,             *               +                                         .
  28.50,            *                +                                         .
  29.00,            *                +                                         .
  29.50,            *                +                                         .
  30.00,            *                +                                         .
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N-TYPE SILICON CARBIDE
NA = 0.
ND = .100E+18
KO = .385E+01
KS = .100E+02
KT = .259E-01
NI = .287E-05

TOX = .100E-04
COX = .166E-03

NORMALIZED FLAT BAND CAP = .956E+00

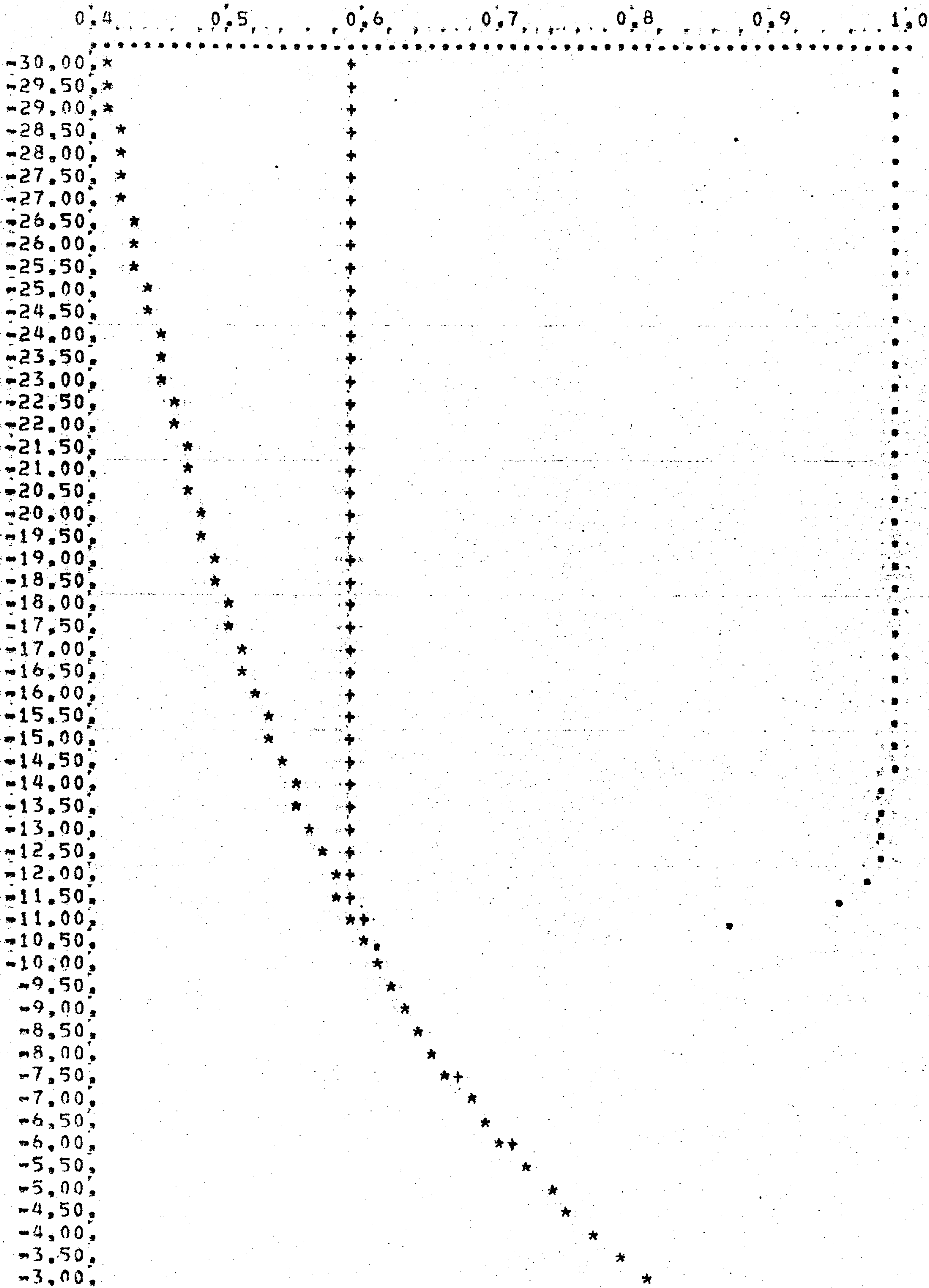
RESULTS FROM C-V PLOT

VAPP	CLFN	CHFN	CDEPN
-.300E+02	.998E+00	.596E+00	.412E+00
-.295E+02	.998E+00	.596E+00	.415E+00
-.290E+02	.998E+00	.596E+00	.418E+00
-.285E+02	.998E+00	.596E+00	.420E+00
-.280E+02	.998E+00	.596E+00	.423E+00
-.275E+02	.998E+00	.596E+00	.426E+00
-.270E+02	.998E+00	.596E+00	.429E+00
-.265E+02	.997E+00	.596E+00	.433E+00
-.260E+02	.997E+00	.596E+00	.436E+00
-.255E+02	.997E+00	.596E+00	.440E+00
-.250E+02	.997E+00	.596E+00	.443E+00
-.245E+02	.997E+00	.596E+00	.447E+00
-.240E+02	.997E+00	.596E+00	.451E+00
-.235E+02	.997E+00	.596E+00	.454E+00
-.230E+02	.997E+00	.596E+00	.458E+00
-.225E+02	.997E+00	.596E+00	.462E+00
-.220E+02	.997E+00	.596E+00	.466E+00
-.215E+02	.996E+00	.596E+00	.470E+00
-.210E+02	.996E+00	.596E+00	.475E+00
-.205E+02	.996E+00	.596E+00	.479E+00
-.200E+02	.996E+00	.596E+00	.484E+00
-.195E+02	.996E+00	.596E+00	.488E+00
-.190E+02	.996E+00	.596E+00	.493E+00
-.185E+02	.995E+00	.596E+00	.498E+00
-.180E+02	.995E+00	.596E+00	.503E+00
-.175E+02	.995E+00	.596E+00	.509E+00
-.170E+02	.994E+00	.597E+00	.514E+00
-.165E+02	.994E+00	.597E+00	.519E+00
-.160E+02	.993E+00	.597E+00	.525E+00
-.155E+02	.993E+00	.597E+00	.531E+00
-.150E+02	.992E+00	.597E+00	.538E+00
-.145E+02	.991E+00	.597E+00	.544E+00
-.140E+02	.990E+00	.597E+00	.551E+00
-.135E+02	.988E+00	.597E+00	.558E+00
-.130E+02	.985E+00	.598E+00	.565E+00

-.115E+02	.957E+00	.599E+00	.588E+00
-.110E+02	.880E+00	.600E+00	.597E+00
-.105E+02	.612E+00	.606E+00	.606E+00
-.100E+02	.616E+00	.616E+00	.615E+00
-.950E+01	.626E+00	.626E+00	.625E+00
-.900E+01	.636E+00	.636E+00	.635E+00
-.850E+01	.647E+00	.647E+00	.646E+00
-.800E+01	.658E+00	.658E+00	.657E+00
-.750E+01	.670E+00	.670E+00	.669E+00
-.700E+01	.683E+00	.683E+00	.682E+00
-.650E+01	.697E+00	.696E+00	.695E+00
-.600E+01	.711E+00	.711E+00	.710E+00
-.550E+01	.726E+00	.726E+00	.725E+00
-.500E+01	.742E+00	.742E+00	.741E+00
-.450E+01	.760E+00	.759E+00	.758E+00
-.400E+01	.778E+00	.778E+00	.777E+00
-.350E+01	.798E+00	.798E+00	.797E+00
-.300E+01	.820E+00	.820E+00	.818E+00
-.250E+01	.844E+00	.843E+00	.842E+00
-.200E+01	.869E+00	.869E+00	.868E+00
-.150E+01	.896E+00	.897E+00	.896E+00
-.100E+01	.921E+00	.928E+00	.927E+00
-.500E+00	.942E+00	.963E+00	.961E+00
0.	.956E+00	.100E+01	.100E+01
.500E+00	.966E+00	.100E+01	.100E+01
.100E+01	.973E+00	.100E+01	.100E+01
.150E+01	.977E+00	.100E+01	.100E+01
.200E+01	.981E+00	.100E+01	.100E+01
.250E+01	.983E+00	.100E+01	.100E+01
.300E+01	.985E+00	.100E+01	.100E+01
.350E+01	.987E+00	.100E+01	.100E+01
.400E+01	.988E+00	.100E+01	.100E+01
.450E+01	.990E+00	.100E+01	.100E+01
.500E+01	.990E+00	.100E+01	.100E+01
.550E+01	.991E+00	.100E+01	.100E+01
.600E+01	.992E+00	.100E+01	.100E+01
.650E+01	.992E+00	.100E+01	.100E+01
.700E+01	.993E+00	.100E+01	.100E+01
.750E+01	.993E+00	.100E+01	.100E+01
.800E+01	.994E+00	.100E+01	.100E+01
.850E+01	.994E+00	.100E+01	.100E+01
.900E+01	.994E+00	.100E+01	.100E+01
.950E+01	.995E+00	.100E+01	.100E+01
.100E+02	.995E+00	.100E+01	.100E+01
.105E+02	.995E+00	.100E+01	.100E+01
.110E+02	.995E+00	.100E+01	.100E+01
.115E+02	.996E+00	.100E+01	.100E+01
.120E+02	.996E+00	.100E+01	.100E+01
.125E+02	.996E+00	.100E+01	.100E+01
.130E+02	.996E+00	.100E+01	.100E+01
.135E+02	.996E+00	.100E+01	.100E+01
.140E+02	.996E+00	.100E+01	.100E+01
.145E+02	.996E+00	.100E+01	.100E+01
.150E+02	.997E+00	.100E+01	.100E+01
.155E+02	.997E+00	.100E+01	.100E+01
.160E+02	.997E+00	.100E+01	.100E+01
.165E+02	.997E+00	.100E+01	.100E+01
.170E+02	.997E+00	.100E+01	.100E+01
.175E+02	.997E+00	.100E+01	.100E+01
.180E+02	.997E+00	.100E+01	.100E+01
.185E+02	.997E+00	.100E+01	.100E+01
.190E+02	.997E+00	.100E+01	.100E+01
.195E+02	.997E+00	.100E+01	.100E+01
.200E+02	.997E+00	.100E+01	[illegible]

AXIS GOING FROM LEFT TO RIGHT=NORMALIZED CAP.

AXIS GOING DOWN=GATE APPLIED VOLTAGE VAPP



-1,00,
-,50,
0,00,
,50,
1,00,
1,50,
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2,50,
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3,50,
4,00,
4,50,
5,00,
5,50,
6,00,
6,50,
7,00,
7,50,
8,00,
8,50,
9,00,
9,50,
10,00,
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11,00,
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