CMOS PHOTODETECTORS FOR LOW-LIGHT-LEVEL IMAGING APPLICATIONS

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By

Naser Faramarzpour

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AUTHOR: Naser Faramarzpour,
B.Sc. Sharif University of Technology, Tehran, Iran
M.S. McMaster University, Hamilton, ON, Canada

SUPERVISORS: Prof. M. Jamal Deen and Prof. Shahram Shirani

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ABSTRACT

Weak optical signals have to be measured in different fields of sciences including chemistry and biology. For example, very low levels of fluorescence emission should be detected from the spots on a DNA microarray that correspond to weakly expressed genes. High sensitivity charge-coupled devices (CCDs) are used in these applications. CCDs require special fabrication and are difficult to integrate with other circuits. CMOS is the technology used for fabrication of CPUs and other widely used digital components. CMOS is not optimized for light detection. CMOS circuits are however cheap, low power and can integrate several components.

Active pixel sensor (APS) is the most common pixel structure for CMOS photodetector arrays. In this work we provide an accurate analysis of the APS signal using new models for the capacitance of the photodiode. We also provide a complete noise analysis of the pixel to calculate the SNR of the pixel and provide optimum operation points. We propose a new mode of operation for APS that can achieve at least 10 dB higher SNR, than conventional APS, at light levels of less than 1 μW/cm^2. We fabricated several APS pixels in CMOS 0.18 μm technology and measured them to confirm the proposed analyzes.

There are applications like fluorescence lifetime imaging that require both sensitivity and fast response. Photomultiplier tubes (PMTs) are commonly used in these applications to detect single photons in pico- to nano-seconds regime. PMTs are bulky and require high voltage levels. Avalanche photodiodes (APDs) are the semiconductor equivalent of PMTs. We have fabricated different APDs along with different peripheral circuitries in CMOS 0.18 μm technology. Our APDs have a 5.5 percent peak probability of detection of a photon at an excess bias of 2 V, and a 30 ns dead time, which is less than the previously reported results.

The low price of CMOS makes modern diagnosis devices more available. The low power of CMOS leads to battery-driven hand-held imaging solutions, and its high integration leads to miniaturized imaging and diagnosis systems. A low-light-level CMOS imager paves the way for the future generation of biomedical diagnosis solutions.

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List of Abbreviations

A/D	Analog to Digital
ADC	Analog to Digital Conversion
AGC	Automatic Gain Control
AMIS	AMI Semiconductor
AMS	Analog mixed signal
APD	Avalanche Photodiode
APS	Active Pixel Sensor
BJT	Bipolar Junction Transistor
C-V	Capacitance-Voltage
CCD	Charge-Coupled Device
CCE	Charge Conversion Efficiency
CDS	Correlated Double Sampling
CFA	Color Filter Array
CMC	Canadian Microelectronics Corporation
CMOS	Complementary Metal-Oxide-Semiconductor
dB	Decibel
DC	Direct Current
DESSIS	Device Simulation for Smart Integrated Systems
DNA	Deoxyribonucleic acid
DOP	Depth of Field
DR	Dynamic Range
IBM	International Business Machines Corporation
ECE	Electrical and Computer Engineering
FET	Field Effect Transistor
FF	Fill Factor
FPN	Fixed Pattern Noise
GC-LBT	Gate-controlled Lateral Bipolar Transistor
GENESIS	General Neural Simulation System
GI	Gastrointestinal
GMAP	Geiger-mode Avalanche Photodiode
GND	Ground
I-V	Current-Voltage
IEEE	Institute of Electrical and Electronics Engineering
JPL	Jet Propulsion Laboratory
LDD	Lightly Doped Drain
LED	Light-Emitting Diode
LOCOS	Local Oxidation of Silicon
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPU	Microprocessor Unit
NHK	Nippon Hōsō Kyōkai, or Japan Broadcasting Corporation
NMOS	n-channel MOSFET
PAPS	Pseudo-Active Pixel Sensor

PCR	Polymerase Chain Reaction
PDP	Photon Detection Probability
PG	Photo-Gate
PMOS	p-channel MOSFET
PMT	Photo-multiplier Tube
PPS	Passive Pixel Sensor
PR	Preset
PRNU	Photo-Response Non-Uniformity
PSD	Power Spectral Density
PSS	Periodic Steady-State
QE	Quantum Efficiency
RF	Radio Frequency
RMS	Root Mean Square
RNA	Ribonucleic Acid
SAPD	Silicon Avalanche Photodiode
SDRAM	Synchronous Dynamic Random Access Memory
SNR	Signal-to-Noise Ratio
SoC	System-on-a-Chip
SOI	Silicon on Insulator
SPAD	Single Photon Avalanche Diode
STI	Shallow Trench Isolation
TIRFM	Total Internal Reflection Fluorescence Microscopy
TX	Transmission gate
UDTV	Ultra-High Definition TV
UHF	Ultra High Frequency
UV	Ultraviolet
VLSI	Very Large Scale Integration

TABLE OF CONTENTS

ABSTRACT III

LIST OF ABBREVIATIONS V

LIST OF FIGURES X

LIST OF TABLES XVIII

CHAPTER 1 INTRODUCTION AND APPLICATIONS 1

1.1. Emerging applications 1

1.1.1. DNA microarrays 1
1.1.2. Fluorescence lifetime imaging 3
1.1.3. Total internal reflection fluorescence microscopy 4
1.1.4. Fluorescence spectroscopy 5
1.1.5. Camera pill 7

1.2. Current solutions 9

1.2.1. Basics of silicon photodetection 9
1.2.2. CCD 10
1.2.3. PMT 12

1.3. Integrated photodetectors 14

1.3.1. Imaging system 15
1.3.2. Advantages of CMOS photodetectors 16
1.3.3. Limitations of CMOS photodetectors 17

1.4. Effect of scaling 18

1.4.1. Effect on Photodiodes 19
1.4.2. Effect on APS arrays 22
1.4.3. Effect on APD detectors 24

1.5. Signal notations 25

1.6. Outline of thesis 26

1.7. Contributions 26

CHAPTER 2 THREE-TRANSISTOR ACTIVE PIXEL SENSOR (APS) 28

2.1. Introduction 28

2.1.1. Passive pixel sensor circuit 28
2.1.2. Three transistor active pixel sensor circuit 29

2.2. Overview of APS implementations in literature 30

2.3. APS signal during integration 31

2.3.1. *C-V* analysis for exponential junction and our *C-V* measurements 32
2.3.2. Analysis of APS signal and comparison to measured APS signal 36

2.4. APS noise 38

2.4.1. Fixed pattern noise 38
2.4.2. Reset noise 38
2.4.3. Shot noise 40
2.4.4. 1/f noise 43
2.4.5. Read-out stage noise 45

2.5. Signal to noise ratio (SNR) of APS 47

2.5.1. Optimum integration time and maximum SNR of pixel 48
2.5.2. Our measurements 49

CHAPTER 3 IMAGE SENSOR WITH PIXEL-LEVEL PROCESSING 53

3.1. Review of APS variations in literature 53

3.1.1. Photogate APS 53
3.1.2. Logarithmic pixels 54
3.1.3. Current-mediated 55
3.1.4. High DR 56
3.1.5. In-pixel ADC 57
3.1.6. Pseudo-active pixel senor 59
3.1.7. Combined structure 61
3.1.8. Conventional APS 62

3.2. APS pixels with internal comparator and integrator 62

3.2.1. APS with comparator 63
3.2.2. APS with integrator 66
3.2.3. Comparison 70

3.3. Multisampling, time-domain APS 71

3.3.1. Architecture and frame-rate analysis 72
3.3.2. Experimental results 76

3.4. Lateral BJT 77

3.4.1. Structure 77
3.4.2. Principle of operation of GC-LBT as photodetector 79

3.5. APS array 81

CHAPTER 4 DC LEVEL MODE APS 82

4.1. Analysis of DC level mode 84

4.1.1. Sense node voltage during reset 84
4.1.2. Sense node voltage after integration and DC level mode analysis 87

4.1.3. Noise analysis of DC level mode: Auto-regressive noise model 89

4.2. DC level SNR optimization 93

4.3. Measurements and comparison 96

CHAPTER 5 AVALANCHE PHOTODIODES AND APD-BASED SYSTEMS ... 100

5.1. Overview of APD implementations in literature 101

5.2. APD design 102

5.2.1. APD layout 102
5.2.2. Device simulation 103

5.3. APD fabrication 104

5.4. APD characterization 105

5.4.1. *I-V* characteristics 106
5.4.2. Breakdown voltage vs. temperature 107
5.4.3. Discussion on breakdown mechanism and microplasma 109
5.4.4. Quantum efficiency of Geiger-mode APDs 115

5.5. Comparison 118

5.6. Geiger-mode passive APD 119

5.6.1. Resistor vs. active load 120
5.6.2. Dark count 121

5.7. Geiger-mode APD with active peripheral circuitry 123

5.7.1. Basics of peripheral circuitry: Schematic and layout 123
5.7.2. Analytic derivation of APD system output 126
5.7.3. Measurement of APD system output 128
5.7.4. Measurements of photo-response and spectral response 129

CHAPTER 6 CONCLUSIONS AND RECOMMENDATIONS 132

6.1. Conclusions 132

6.2. Recommendations 135

REFERENCES 138

APPENDIX A 148

APPENDIX B 150

LIST OF FIGURES

Figure 1-1: Processes of printing a DNA microarray, preparing DNA test samples and scanning the microarray after the experiment. Microarrays are usually printed on glass slides. Test and reference DNA sequences are tagged with red and green fluorescent tags before hybridization. Outcome of a microarray experiment is a two-color image [1.6]. 2

Figure 1-2: (a) Fluorescence spectral response showing the excitation pulse and the emission pulse. (b) Time resolved fluorescence lifetime measurement [1.10]... 3

Figure 1-3: (a) Simplified structure of a TIRFM. The angle of the light beam is high enough to be totally reflected at the glass-water interface. (b) Transport of a single NTF2-Alexa633 molecule across the nuclear envelope of a biological cell (400 frames/s) recorded using TIRFM (Figures taken from [1.13]). 5

Figure 1-4: Simplified setup for excitation and emission spectroscopy. The emitted light from the lamp has a wide spectrum and the excitation and emission diffraction gratings are used to select the wavelengths. The emission from the sample is sensed at an angle perpendicular to the excitation beam in order to minimize the interference of the excitation beam in the photodetector. 6

Figure 1-5: (a) It is difficult to reach some of the regions of the human GI tract, like the small intestine, with conventional endoscopy methods. (b) PillCam of Given Imaging, is a capsule that contains a camera and captures and sends images from inside the GI tract. (c) Some of the pictures taken by PillCam (Figures taken from [1.16], [1.17] and [1.18]). 8

Figure 1-6: A simplified diagram of the camera pill. The pill includes LEDs to illuminate the scene. It captures and transmits real-time video. The pill consists of batteries, and imaging, optics and wireless modules (Taken from [1.23], Fig. 1). 9

Figure 1-7: Top and cross-sectional views of a CCD array. Charges are transferred within columns with a two-phase mechanism. Columns are separated with a thick field oxide and a p^+ channel stop (Taken from [1.25], Fig. 3). 11

Figure 1-8: Four phase and three phase mechanisms of charge transfer in CCD arrays (Taken from [1.26], Fig. 5)... 11

Figure 1-9: Two output node structures for the CCD array: (a) Floating diffusion, and (b) floating gate (Taken from [1.26], Fig. 3). 12

Figure 1-10: Simplified structure of a PMT. A single incoming photon can result in a significant current at the PMT anode.. 13

Figure 1-11: Photomultiplier tube (Taken from [1.27]). An 11200 PMT array, made in super-K neutrino observatory in Japan. The colossal structure is filled

with 50000 tons of pure heavy water to detect subatomic particles thrown by supernovas billions of miles away (Taken from [1.28]). 14

Figure 1-12: Block diagram of an imaging system (Taken from [1.32], Fig. 1) 15

Figure 1-13: A late afternoon landscape picture of Hamilton lakeshore taken by a Canon PowerShot A60 digital camera, which uses a 2 Mega-pixel CCD imager. Blooming is observed in the column of pixels that are in line with the sun. 16

Figure 1-14: A simplified cross-section of a CMOS chip, showing several layers of silicon dioxide and metal on top of the silicon surface. The light has to pass through a deep well, before reaching the surface of the photodiode. 18

Figure 1-15: (a) Lifetime and (b) mobility of minority carriers in silicon. Both of the parameters decrease as the doping concentration level increases. (Taken from [1.34] and [1.36], Fig. 3-23). 21

Figure 1-16: (a) Different pixel sizes for CMOS image sensors. The pixel size shrinks by downscaling of CMOS technology, resulting in higher possible resolutions (Taken from [1.35], Fig. 12). (b) Sample APS layouts for a 0.5 μm technology (10 μm pixel) and a 0.35 μm technology (7 μm pixel) (Taken from [1.33], Fig. 2). 22

Figure 1-17: The maximum SNR that can be obtained from an APS pixel decreases as the technology scales down. The calculations are done assuming that the pixel size scales down proportional to the technology feature size. 24

Figure 1-18: Variation of avalanche breakdown voltage in abrupt p^+/n junctions, as a function of donor concentration on the n side, for several semiconductors (Taken from [1.36], Fig. 5-22). 25

Figure 2-1: PPS pixel structure. Pixel readout and reset are both done at the column level. PPS is the most simple CMOS structure with highest fill-factor... 29

Figure 2-2: (a) Schematic of the three-transistor APS circuit. The dimensions of the photodiode is 20 $\mu \times$ 20 μ, M_1 is 4 μ / 0.4 μ and M_2 and M_3 are 2.4 μ / 0.4 μ. (b) Applied reset voltage and measured output of the APS. The voltage levels at the beginning and at the end of integration are shown by v_2 and v_1 respectively. The difference (v_2 - v_1) is proportional to the incident light power. 30

Figure 2-3: Doping profiles at the junction between two ion-implanted regions. Profiles are close to exponential at the proximity of the junction. w_n and w_p are boundaries of the depletion region. 33

Figure 2-4: (a) Measured C-V characteristics and (b) logarithm of capacitance versus voltage for different values of φ. The value of φ which produces a straight line is closest to the built-in potential of the junction. 35

Figure 2-5: Measured and calculated sense node voltage of APS vs. time. The curve is magnified to show that our analytical model best matches the measured APS output. The pixel is saturated in this example after 1.5 ms. 37

Figure 2-6: (a) APS circuit during reset, and (b) the equivalent small signal circuit used for noise evaluations. I_n is the reset transistor equivalent noise source, g_d is the trans-conductance of M_1 and C_{PH} is the small signal capacitance of the photodiode. 39

Figure 2-7: Equivalent circuit of the APS during integration............ 40

Figure 2-8: APS circuit with (a) column bias transistor and equivalent capacitance of the next stage. (b) Full APS circuit with CDS and read-out stages. 45

Figure 2-9: Small signal equivalent circuits of the readout stage (transistor M_2, M_3 and M_4 of Figure 2-8(a)) for (a) gain and (b) noise calculations ((b) is taken from [2.15], Fig. 8)............ 46

Figure 2-10: (a) SNR of an APS has a peak before the pixel capacitance fully discharges. (b) The optimum integration time decreases as the photocurrent increases. The optimum SNR, however, stays around 54 dB. The reason for the small drop in SNR is that when the i_{PH} value becomes too small, comparable to i_{DK}, the shot noise of i_{DK} becomes important, and the SNR decreases............ 48

Figure 2-11: (a) Photomicrograph of the APS chip that is fabricated in this work. The chip is fabricated in standard CMOS 0.18 μm technology. It contains several APS pixels. (b) The zoomed Photomicrograph of the three-transistor APS pixel. The metal layer connections to the pixel can be easily seen in the picture. A thick 6th layer metal shield is designed to cover the peripheral circuitry of the pixel............ 50

Figure 2-12: Optical setups in our dark room for measuring the photoresponse and noise of the APS circuits. The figures show the setups using (a) a laser source and (b) a Xenon lamp. Laser source is used for selective measurement of the photodetector at a certain wavelength. Xenon lamp is used for wide spectral response measurements. 51

Figure 3-1: A four-transistor APS pixel with photo-gate. Photons have to pass through the poly-silicon gate layer before reaching the silicon surface (Taken from [3.1], Fig. 6)............ 54

Figure 3-2: Logarithmic pixel. In this pixel the load transistor performs the logarithmic current to voltage conversion (Taken from [3.1], Fig. 9)..... 54

Figure 3-3: Current mediated pixel structure. The pixel has to be selected to perform reset (Taken from [3.5], Fig. 2). 56

Figure 3-4: (a) High dynamic range pixel schematic and (b) its layout. High dynamic range is achieved by varying $b(t)$ (Taken from [3.7], Figures 1 and 2)... 57

Figure 3-5: Digital pixel sensor structure. Every four pixels share an ADC unit, resulting is approximately 3 transistors per pixel. (Taken from [3.9], Fig. 3). 58

Figure 3-6: Sigma delta converter cell schematic. It contains 19 transistors and connects to 5 bus lines (Taken from [3.10], Fig. 9). 59

Figure 3-7: (a) Pseudo-active pixel sensor circuit and (b) the pixel. Pixel is similar to passive as it connects to the bus via a single transistor (Taken from [3.13], Fig. 1 and 4). 60

Figure 3-8: Ring reset pixel structure (Taken from [3.15], Fig. 1). 61

Figure 3-9: Combined photo-gate and photodiode structure. The pixel schematic and the correlated double sampling circuit are shown at left. The layout of the pixel is shown at right (Taken from [3.16], Fig. 1). 61

Figure 3-10: Layouts of different APS structures. (a) Three transistor APS has the simplest layout and highest fill-factor. (b) The APS with comparator has 8 transistors. However, our compact design has kept the fill-factor at a high level. (c) The APS with integrator. This design considers a capacitor in each pixel that reduces the fill-factor of the pixel. However, the fill-factor is still at a reasonable level. 63

Figure 3-11: APS with comparator. (a) General schematic and (b) Measured and illustrated waveforms. Channel 1 is the applied reset signal and channel 2 is the measured output, v_O, of the pixel. Channel 3 and 4 show how the sense node voltage and reference level stand with respect to each other to generate the output. 64

Figure 3-12: Full circuit of Figure 3-11(a) with the dimensions of the photodiode and transistors. 65

Figure 3-13: (a) Measured output of the APS with comparator, zoomed in to show the jitter in its output. This jitter is the noise of the output as the pulse width is the output of the pixel. (b) Measured signal (pulse width) and noise (jitter) of the output of the pixel, as a function of light powers. 66

Figure 3-14: APS with integrator. (a) General schematic of the pixel and (b) its measured waveforms. Channel 1 shows the measured output of the pixel, while channel 2 shows the reset signal applied to the pixel, for a 2.5 ms readout time. 67

Figure 3-15: Full circuit of Figure 3-14(a) with the dimensions of the photodiode and transistors. Junction capacitance of the photodiode is approximately 300 fF. 68

Figure 3-16: Output of the APS with integrator, sampled at different levels of incident light power. Measurements are done at different wavelengths. It can be observed that a good linearity exists in the output, unless the output saturates, as shown in the curve for the 700 nm light. 69

Figure 3-17: (a) Multisampling pixel architecture. Each pixel consists of an n^+/p-sub photodiode, a PMOS reset transistor, a clocked comparator and a D flip-flop. The PMOS reset transistor has W/L = 0.4/0.4, and the photodiode size is 5 μm × 20 μm. (b) Time diagram of the circuit signals. Output of the comparator, V_{CMP}, becomes high with the first clock after the sense node voltage drops below V_{REF}. 72

Figure 3-18: Architecture of the multisampling, time-domain APS array. 73

Figure 3-19: Schematic of the integrated (a) clocked comparator and (b) details of the circuit. (c) D flip-flop, with PMOS W/L = 0.4/0.4 and NMOS W/L = 0.4/0.35. 74

Figure 3-20: Minimum sampling time for different array sizes. 75

Figure 3-21: (a) Discharge time of a pixel measured at constant reference voltage of 1.5 V and (b) spectral response of the pixel. 77

Figure 3-22: (a) Cross-section of the GC-LBT, and its internal lateral and vertical transistors. (b) Photomicrograph of the fabricated GC-LBT. (c) top view of the device with showing the size of the important regions of the device. 78

Figure 3-23: Body floating and V_{GB} constant operation mode. (d) Body current generated vs. incident light power, (c) body voltage vs. body current characteristics and (b) the MOSFET drain current vs. the body voltage. The (a) photoresponse characteristics of the device is derived from the (d), (c) and (b) curves. 80

Figure 3-24: Photomicrograph of the array structure fabricated in 0.18 μm CMOS technology. 81

Figure 4-1: Total sense-node voltage versus time for different levels of photocurrent corresponding to different low-light-level illumination conditions. At the absence of photocurrent, the swing output is due to the internal dark current of the photodiode. The DC level varies more than the swing, for the same level of incident light. 83

Figure 4-2: Steady-state DC level $((v_1 + v_2)/2)$ and swing $(v_2 - v_1)$ output of the sense node versus i_{PH}. The DC level has a value close to V_{DD} for zero photocurrent. The curve shown is the displacement of the DC level output from its dark-level value, which corresponds to the output signal. As the DC level corresponding to the zero photocurrent is constant for every pixel, CDS will not be necessary. 88

Figure 4-3: Block diagram showing how reset and integration noise contribute to the steady DC level. Reset noise and integration noise are represented by V_{n2} and V_{n1} respectively. The total noise is calculated in $(v_1 + v_2)/2$. 89

Figure 4-4: (a) Exact values of β obtained in (4-17) and (4-19) are shown vs. i_{PH}, where t_{int} = 30 ms and v_2 = 2.3 V. Note that for low photocurrents, $\beta \approx 1$. (b) Simplified noise diagram of Figure 4-3, assuming $\beta = 1$. 92

Figure 4-5: (a) Output DC level and its noise vs. reset time. Both the signal and noise increase with decreasing the reset time. The noise however, increases more sharply. (b) The SNR of the output DC level has an optimum. In this example, i_{PH} = 10 fA, and t_{int} = 30 ms. 94

Figure 4-6: (a) Theoretical and (b) simulated SNR curves of the proposed DC level method as a function of both the integration time and the reset time. The surfaces correspond to i_{PH} = 3 fA (lower) and i_{PH} = 12 fA (upper). 96

Figure 4-7: Analytically derived SNR of the APS, measured SNR values for our APS, and SNR values reported for some other low-light-level APS circuits in the literature (from the top: [4.12], [4.13], [4.15], [4.7]). The data has been gathered from a variety of pixel sizes. The size of the pixels used in the experiments affects the reported SNR values at different light powers. The data have been adjusted to compensate for the size differences and to make a fair comparison of the different reported SNR values. 97

Figure 4-8: Measured swing of the sense node voltage of the APS vs. the power of light at different wavelengths. The curves show that the generated photocurrent of the APS approximately doubles by changing the wavelength of light in the visible range. 98

Figure 5-1: (a) Cross section and (b) plan view of the layout of our APD. Putting an n-well, inside a p^+ region, creates the avalanche area and also the guard ring. 103

Figure 5-2: Device simulation of the APD under reverse bias, using the DESSIS tool. It shows that the maximum electric field will appear in the desired p^+/n-well junction. 104

Figure 5-3: (a) Photomicrograph of the chip containing APD devices and circuit. Layouts of our APDs with (a) 5 μm, (b) 10 μm and (c) 20 μm diameters. Design rules of the technology do not allow circular features. We have used 45° rotated lines to draw octagons, the closest shape that can be generated to circles. 105

Figure 5-4: Measured *I-V* profiles for different diodes. While a regular p^+/n-well diode shows a low breakdown voltage, our APDs with guard ring show an avalanche breakdown at 10.2 V. The 5 μm APD however, has a high breakdown voltage. 106

Figure 5-5: (a) Breakdown site of a regular p^+/n-well diode compared to (b) the breakdown site of the 10 μm APD and (c) the breakdown site of the 5 μm APD. The line shows the extent of the depletion region in the n-well.. 107

Figure 5-6: Variation of the breakdown voltage of APDs with temperature. The rate of change is approximately 7 mV°C^{-1} that results in $\beta \approx 7 \times 10^{-4}$ °C^{-1}.. 108

Figure 5-7: Schematic of an abrupt p/n-junction at avalanche breakdown. The width of the depletion region with an electric field high enough for impact ionization, w_m, is only a small fraction of the total width of the junction depletion region. 109

Figure 5-8: (a) Measured I-V curve of one of our 10 μm APDs at the onset of breakdown. This region is also known as the multiplication region of the APD, where the current (dark current here) is multiplied by a finite M. The curve clearly shows that the current increases in steps, before complete breakdown. (b) A zoomed version of (a) drawn in linear scale. Different sections of the current curve have resistive characteristics. Resistance of each of the microplasma regions are calculated. It can also be clearly seen that the third microplasma turns on and off a few times before being permanently on. 111

Figure 5-9: Different I-V curves obtained for 9 different APDs with the same layout fabricated on different dies in CMOS 0.18 μm technology. 112

Figure 5-10: Photomicrograph of the APD circuit, with the microscope light on. The circuit consists of a 10 μm APD with a 100 kΩ resistor in series. The APD has a measured 10.2 V breakdown voltage. Photomicrographs taken with the microscope light off, for a reverse bias of (b) 19 V, (c) 20 V, (d) 21 V, (e) 22 V and (f) 23 V. 113

Figure 5-11: The APD circuit (a) and its measured signal, v_S, at (b) 19 V and (c) 20 V applied V_{DD}. The series resistor R = 100 kΩ and the probe resistor R_{PROBE} = 1 MΩ. 114

Figure 5-12: (a) Triggering probabilities at several excess biases vs. the starting position of the carriers in the APD depletion region. (b) The triggering probabilities for carriers starting as minority carriers at the edge of the depletion region (taken from [5.43], figures 4 and 5). 117

Figure 5-13: Dark count of our 10 μm APD, at room temperature, for different values of excess bias. The dark count varies linearly for small values of excess bias and it is in good agreement with the theoretical prediction of Figure 5-12 shown with the solid line. 118

Figure 5-14: Geiger-mode of operation of APD. (a) Schematic of a passive APD circuit and (b) its measured sense node voltage vs. time. Each drop corresponds to a photon arriving at a random time. (c) Schematic of an APD in series with an active load and (d) its measured sense node voltage. The active load is a PMOS transistor with W/L = 10 × 9 / 0.3. The voltage scale in both (b) and (d) is 100 mV, and the time scale is 20 μs for (b) and 2 μs for (d). 120

Figure 5-15: Dark count vs. temperature for an excess bias of 0.5 V. The dark count doubles approximately every 30 °C. Note that to extract the activation energy reported, we plotted $\ln(I_D)$ versus the inverse of the Absolute Temperature. 122

Figure 5-16: plot of $\ln(I_D)$ against the inverse of the absolute temperature used for extracting the activation energy. 123

Figure 5-17: (a) Schematic of the APD circuit with active quench and active reset and (b) diameter of the APD, size of the resistor in ohm, and W/L of the transistors of the circuit in micron. The timing block consists of two

mono-stables in series. Each mono-stable has a bias input that adjusts the width of the output pulse. The first mono-stable causes a delay, and second mono-stable dictates the width of the output of the timing block. 123

Figure 5-18: The schematic of the mono-stable circuit used in the APD periphery. M1 and M2 have W/L of 5/0.35, and M3 has W/L of 4 × 2.5/0.3. The mono-stable is triggered by the falling edge of the input, and it generates a low level output pulse with the width that is adjusted by the V_{BM} input. 125

Figure 5-19: Photomicrograph of the layout of the APD with the peripheral circuits. A large part of the layout area is taken by the capacitors, which are seen as the two L-shaped features at the bottom of the Photomicrograph. 126

Figure 5-20: Equivalent circuits used for analytical derivation of the sense node voltage during (a) active quench and (b) active reset. 127

Figure 5-21: Measured and simulated sense node voltage of the APD circuit. The dead time is about 30 ns. 129

Figure 5-22: Probability of detection of photons for different wavelengths. Increasing the excess bias will increase the probability of detection. Oscillations in the curves are due to the several dielectric layers of CMOS on top of the APD. 130

List of Tables

Table 1-1: Emission wavelength of the maximum average fluorescence yield at the auto-fluorescence maximum of normal bronchial tissue in vivo for different excitation wavelengths [1.14]. 7

Table 1-2: Principal device technology and electrical characteristics. (Taken from [1.33], Table II, with some modifications) 19

Table 2-1: Calculated $v_S(t)$ for different values of m. Note that the sense node voltage for m = 4 is what was experimentally found in the actual diode used in this work. 37

Table 2-2: Shot noise calculated for different analytical models. 42

Table 3-1: Different photogate APS structures.. 62

Table 3-2: Different photodiode APS structures 62

Table 3-3: Comparison of the APS structures 70

Table 5-1: Comparison of some of the reported APD implementations in CMOS with our APD. Note that the 50 kHz dark count for our APD in this table is for the worst case according to Figure 5-13. 118

Chapter 1

INTRODUCTION AND APPLICATIONS

1.1. Emerging applications

CMOS image sensors have recently attracted much attention from the research community. Applications of CMOS imaging systems include machine vision [1.1], digital still and video cameras [1.2], surveillance [1.3] and medical imaging [1.4], [1.23]. These applications can benefit from a CMOS image sensor, as it can offer high integration of optoelectronics and electronic components, low cost and low power consumption. A major challenge in the design of CMOS image sensors is to reduce their high spatial and temporal noise [1.5]. Overcoming these challenges with CMOS photodetectors can particularly benefit biomedical imaging applications that require high sensitivity for low-light-level detection. In the following subsections, some of these biomedical applications will be introduced.

1.1.1. DNA microarrays

Although most cells in a living organism contain the same genes, not all of the genes are used in each cell. Some genes are turned on, or expressed, when needed. Many genes are used to specify features unique to each type of cell. Liver cells, for example, express genes for enzymes that detoxify poisons. In many cases, in order to understand how cells achieve such specialization, or to diagnose if they are malfunctioning, the genes that a cell is expressing should be identified.

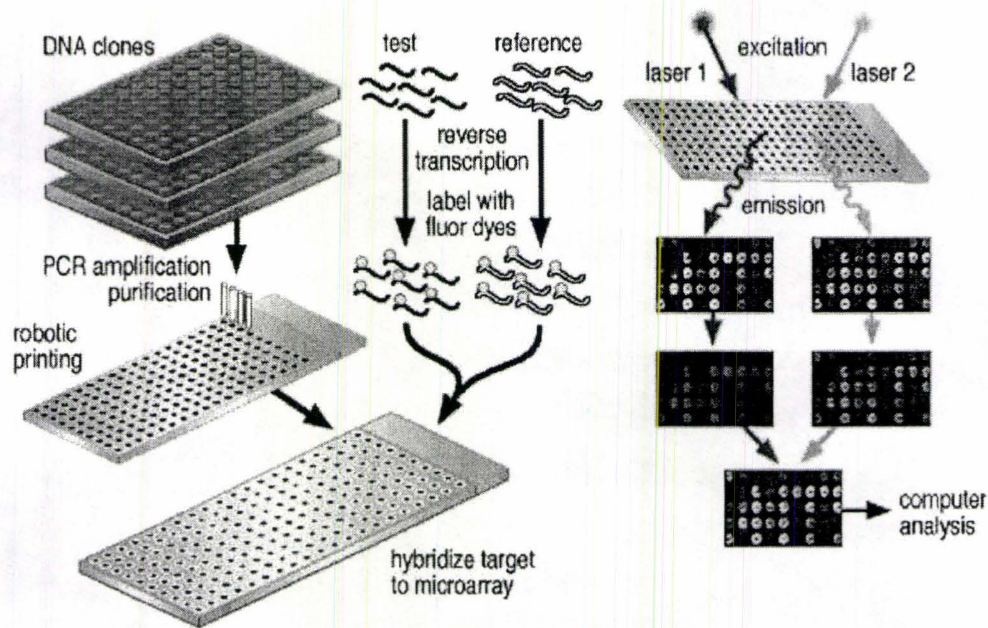


Figure 1-1: Processes of printing a DNA microarray, preparing DNA test samples and scanning the microarray after the experiment. Microarrays are usually printed on glass slides. Test and reference DNA sequences are tagged with red and green fluorescent tags before hybridization. Outcome of a microarray experiment is a two-color image [1.6].

Microarray technology allows scientists to study the expression of many genes simultaneously, instead of studying them one by one [1.7], [1.8]. In a microarray, thousands of individual genes can be spotted on a single square inch slide. Each DNA fragment is single stranded, amplified in number, and put on the slide to form a spot. Figure 1-1 shows the process of making a microarray. In the laboratory, a sample solution is prepared to be tested by the microarray. Messenger RNAs, that are the working copies of the genes being expressed, are purified from cells of a particular type. They are reverse-transcript, amplified in number (PCR) and labeled by attaching a fluorescent dye that allows for them to be monitored later. Figure 1-2(a) shows how the emitted light from a sample fluorescent dye is related to the excitation light. The solution is then exposed to the microarray in a hybridization chamber to allow the DNAs in the solution to bind to the matching molecules on the microarray, if there is any match. Finally, the microarray is illuminated and scanned to obtain the microarray image. A microarray image shows the levels of fluorescence reflection of the spots that are related to the levels of the expression of the corresponding genes in

the sample [1.9]. Some of the spots can have extremely low levels of fluorescence emission, which need to be detected by ultra-sensitive imaging devices.

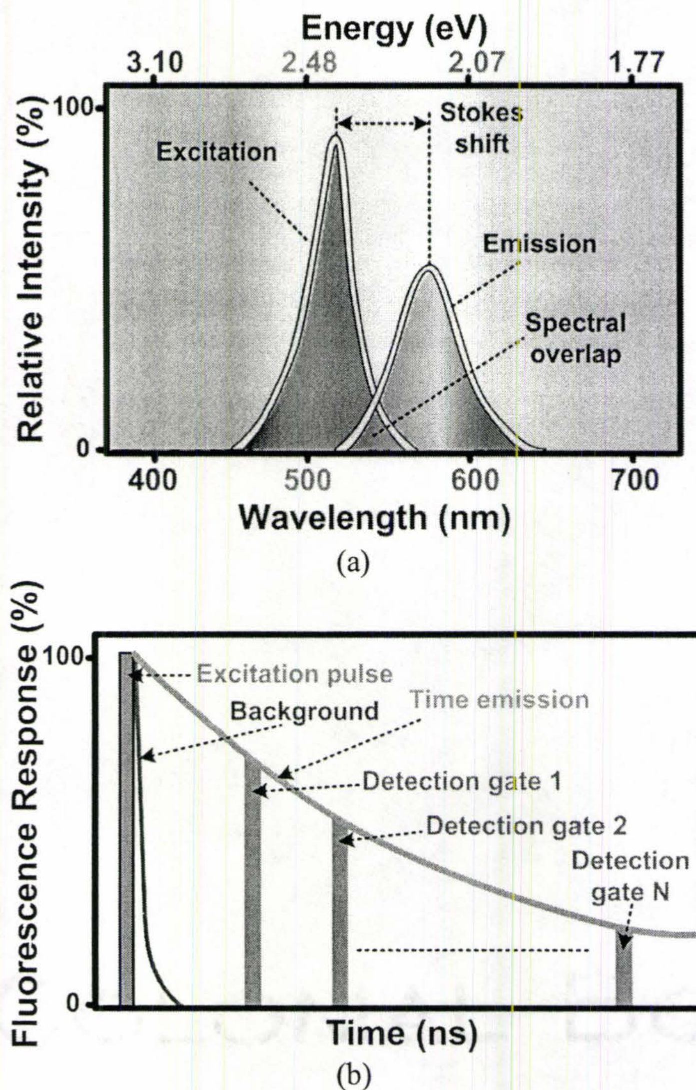


Figure 1-2: (a) Fluorescence spectral response showing the excitation pulse and the emission pulse. (b) Time resolved fluorescence lifetime measurement [1.10].

1.1.2. Fluorescence lifetime imaging

When testing molecules that have overlapping spectra, such as cancerous and non-cancerous cells, one valuable method is time-resolved measurements such as fluorescence lifetime imaging. In such measurements, time resolved techniques are used to determine the relaxation times of fluorescence signals, which is the time it takes for the electronically or optically excited fluorophores to relax back to their

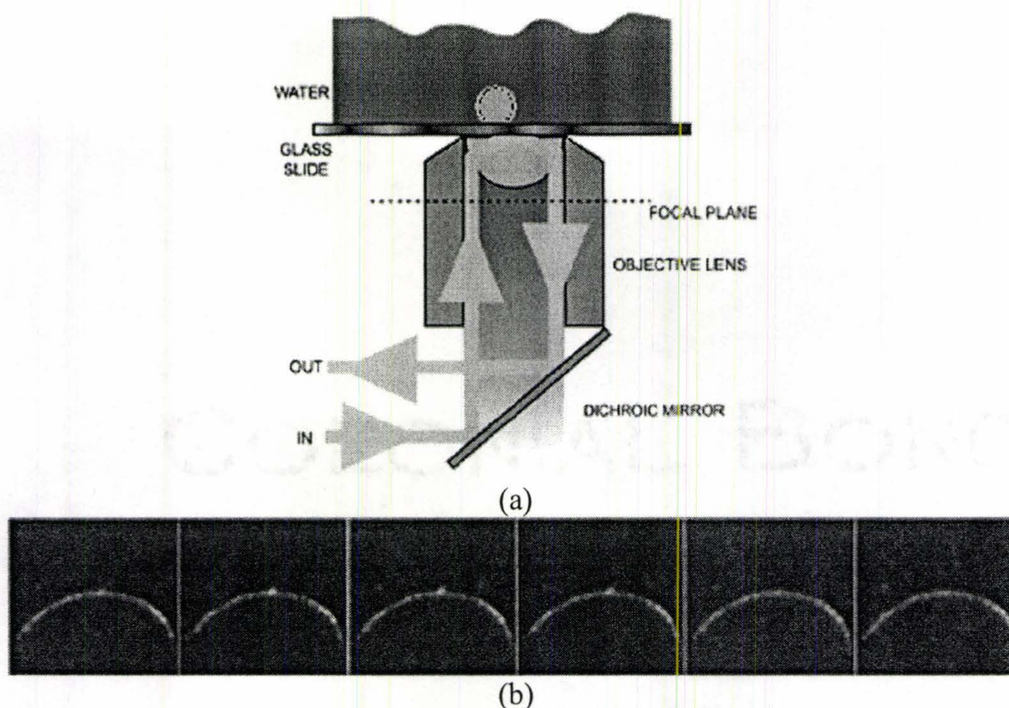
ground state. Since the signal has an exponential decay over time, integrating approaches that have integration times much longer than the average fluorescent lifetime cannot be used. Rather, averaging a number of repeated measurements in narrow sampling windows or gates (Figure 1-2(b)) have been shown [1.10] to be more effective. The background can also be removed by averaging the samples of a number of measurements without excitation. Such high-frame-rate applications require a fast and sensitive imager.

1.1.3. Total internal reflection fluorescence microscopy

Total internal reflection fluorescence microscopy (TIRFM) is a method to observe ultra-thin regions of specimens. It was developed by Daniel Axelrod in the early 1980s [1.11]. TIRFM uses evanescent waves to selectively illuminate and excite fluorophores in a restricted region of the specimen immediately adjacent to the glass-water interface. Evanescent waves are generated only when the incident light is totally reflected at the glass-water interface. The evanescent electromagnetic field decays exponentially from the interface, and thus penetrates to a depth of only approximately 100 nm into the sample medium. The penetration depth d is given by:

$$d(\theta) = \frac{\lambda}{4\pi}\sqrt{n_S^2 \sin\theta - n_C^2} \tag{1-1}$$

where n_S is the refractive index of glass, n_C is the refractive index of water, λ is the wavelength of light and θ is the angle of the totally reflected incident beam.



(a)

(b)

Figure 1-3: (a) Simplified structure of a TIRFM. The angle of the light beam is high enough to be totally reflected at the glass-water interface. (b) Transport of a single NTF2-Alexa633 molecule across the nuclear envelope of a biological cell (400 frames/s) recorded using TIRFM (Figures taken from [1.13]).

Total internal reflection fluorescence microscopy is used to observe single molecule fluorescence. Figure 1-3(b) shows an example of a series of frames obtained by the setup of Figure 1-3(a). The ejection of a protein molecule from the nuclear envelope can be observed. The application requires imaging systems that can detect the low levels of fluorescence reflection and also capture the high speed of cellular events.

1.1.4. Fluorescence spectroscopy

Fluorescence spectroscopy analyzes the spectrum of fluorescence emission from a sample. The approach is widely used in medical and chemical research fields. It is particularly used to study organic compounds, due to its non-invasive nature. Figure 1-4 shows a simplified schematic of a fluorescence spectroscopy setup.

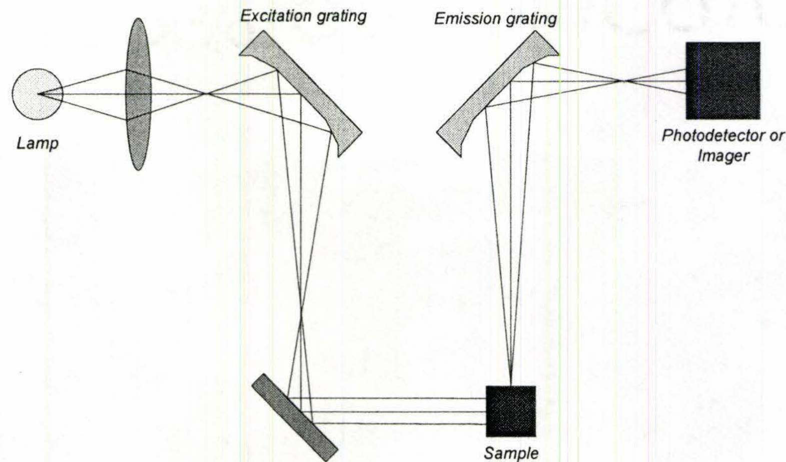


Figure 1-4: Simplified setup for excitation and emission spectroscopy. The emitted light from the lamp has a wide spectrum and the excitation and emission diffraction gratings are used to select the wavelengths. The emission from the sample is sensed at an angle perpendicular to the excitation beam in order to minimize the interference of the excitation beam in the photodetector.

The output of the spectroscopy measurement is most of the time a fluorescence (emission) spectrum or an excitation spectrum. The wavelength of the excitation light is kept constant for obtaining the fluorescence spectra. For excitation spectra, however, the wavelength of the filter controlling the emitted light to the photodetector is kept constant, and the excitation light wavelength is scanned through the desired spectrum to measure the response. Conventional imagers, like charge-coupled devices or CMOS arrays, can typically detect light powers down to 1 $\mu W/cm^2$. In auto-fluorescence applications, the fluorescence yield, which is the ratio of the emitted light power to the absorbed light power, can be very small as the biological samples are not good fluorophores. The emitted light power to the sample is limited, as excess illumination can damage the sample. Table 1-1 shows examples of fluorescence yield for bronchial tissue [1.14]. Image intensifiers or Photomultiplier tubes are widely used in these applications to detect the low level of emitted light from the biological sample. The problem with these detectors is their large size, expensive price, and high output noise.

Table 1-1: Emission wavelength of the maximum average fluorescence yield at the auto-fluorescence maximum of normal bronchial tissue in vivo for different excitation wavelengths [1.14].

Excitation wavelength (nm)	Maximum emission wavelength (nm)	Fluorescence yield at the emission maximum (pW/μW × nm)	Standard deviation at the emission maximum (pW/μW × nm)
350	460	7.9	5.5
365	460	6.9	3.2
380	475	4.7	2.8
395	480	4.5	2.3
405	490	4.2	2.5
420	500	4.5	3.5
435	515	4.0	3.3
450	520	3.5	2.7
465	530	3.1	2.4
480	550	3.5	3.3
495	575	2.3	2.1

1.1.5. Camera pill

Catheter-based video endoscopy, in which a 2 cm diameter tube containing fiber optic cables carrying visible light is inserted into the gastrointestinal (GI) tract of a patient, is one of the most widely used methods for GI cancer screening and diagnosis. Although catheter-based endoscopy provides useful diagnostic information, it has been documented that the procedure is relatively invasive and costly due to the need of specialized equipments, operating suites, as well as the presence of an endoscopist to administer the procedure [1.15].

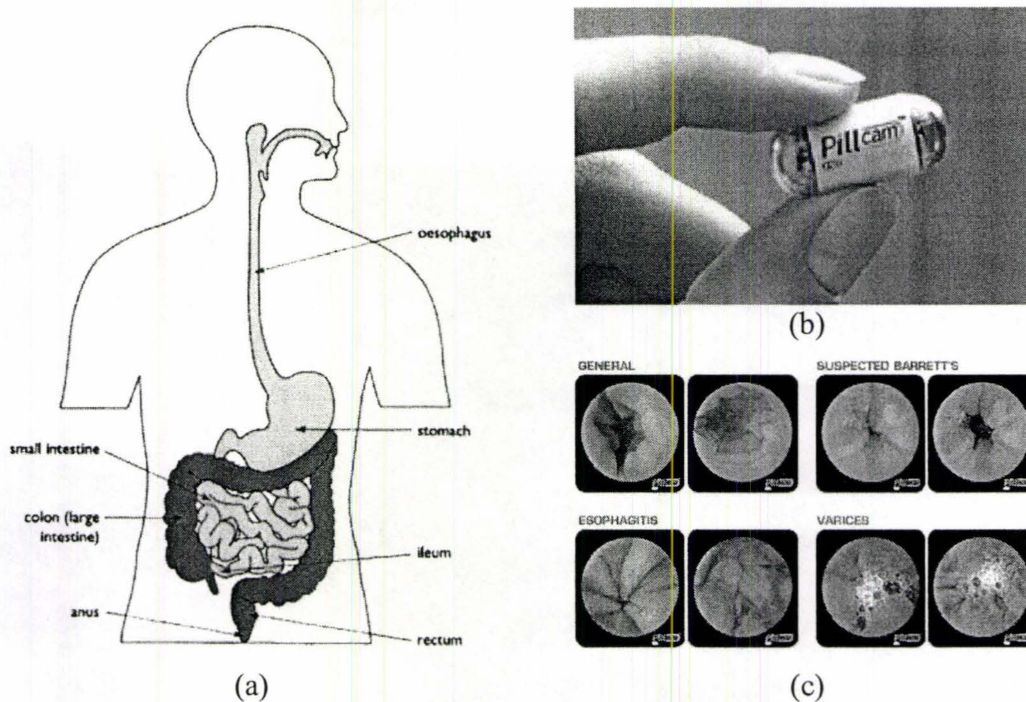


Figure 1-5: (a) It is difficult to reach some of the regions of the human GI tract, like the small intestine, with conventional endoscopy methods. (b) PillCam of Given Imaging, is a capsule that contains a camera and captures and sends images from inside the GI tract. (c) Some of the pictures taken by PillCam (Figures taken from [1.16], [1.17] and [1.18]).

Alternatives that exclude the use of a catheter have recently been investigated and developed. These techniques use ingestible capsule-size cameras, typically the size of a large vitamin pill, to provide visible illumination and acquire the images of the GI tract. The most publicized capsule is the PillCam (previously marketed as M2A) capsule by Given Imaging [1.19]. These capsules were developed to challenge push enteroscopy and radiology in diagnosing diseases usually found in the GI tract: diseases such as obscure bleeding, irritable bowel syndrome, Crohn's disease, and chronic diarrhea [1.20].

Typical wireless imaging capsules are about 11 mm (diameter) × 30 mm (length) and consist of an optical dome, a focusing lens, white light illumination LEDs, batteries, a wireless transmitter with antenna, and an imager. The images are captured over a 7–8 h period inside the GI tract, and then, transmitted using UHF-band radio-telemetry to aerials attached to the patient's body and connected to a waist belt that contains a receiver and electronic memory for storing the received video images. Propelled by

peristalsis, the pill travels through the GI tract without noticeable discomfort, and no air inflation is required [1.20]–[1.22]. Figure 1-6 shows a simplified diagram of a camera pill. The imager of a camera pill, has to consume low power, and be able to integrate with other electronic components of the system. The imager also has to be sensitive to low levels of light, due to the limited illumination of the LEDs in the pill [1.23].

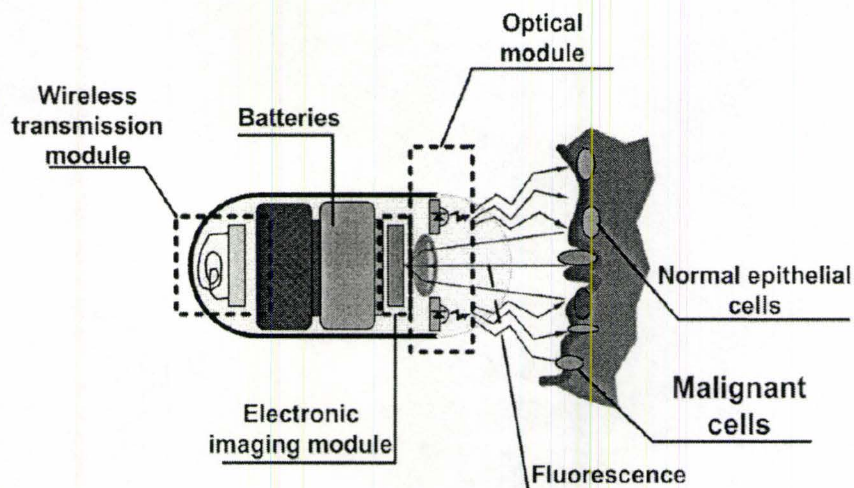


Figure 1-6: A simplified diagram of the camera pill. The pill includes LEDs to illuminate the scene. It captures and transmits real-time video. The pill consists of batteries, and imaging, optics and wireless modules (Taken from [1.23], Fig. 1).

1.2. Current solutions

1.2.1. Basics of silicon photodetection

The basic operation of a photodetector (which can include photodiodes, photogates or phototransistors) is to convert light into electrons. Silicon as a semiconductor material is a good candidate to do so. We know that electrons in silicon can either be in the valence band or in the conduction band. Electrons in the latter band can also be referred to as free electrons. If we shine light on silicon, a photon that enters the silicon can collide with an electron in valence band and give it enough energy to jump into conduction band, leaving behind a hole. The band gap energy of silicon is

1.11 eV. So the incident photon should have at least this much energy to generate an e-h pair. As we have $E = hv$, and $\lambda v = c$, silicon will absorb photons with wavelengths less than 1.1 μm. This includes visible spectrum which is between 0.4 μm and 0.7 μm. It is also worth mentioning that very high energy photons (low wavelength) on the other hand are absorbed so fast (so close to the surface) that cannot practically be sensed by the active part of the sensor. Hence, there will be a wavelength spectrum over which the sensor operates. The ratio of the electron-hole pairs generated to the number of photons incident to the sensor is called quantum efficiency (QE). The QE is a function of wavelength.

1.2.2. CCD

The charge-coupled device, CCD, was first introduced in 1970 [1.24]. It was soon adopted over many other kinds of solid-state sensors due to its relatively low noise and small pixel size. A CCD is an array of MOS capacitors. The electric field created beneath the capacitor gates is used to separate and store light-induced electrons and holes. Assume that a MOS capacitor is fabricated on a p-type silicon. By applying a large enough positive voltage to its gate with respect to the substrate, there will be a narrow inversion layer under the silicon-oxide interface. There will also be a depletion layer spread in the substrate. So there will be an electric field from the edge of gate-oxide interface all the way inside substrate until the edge of the neutral region. The time required to fill the inversion layer thermally is called thermal relaxation time. Now if we shine light on the MOS transistors, photons that are absorbed in the depletion region will generate electron-hole pairs which will help the process of thermal generation, causing a quicker construction of the inversion layer.

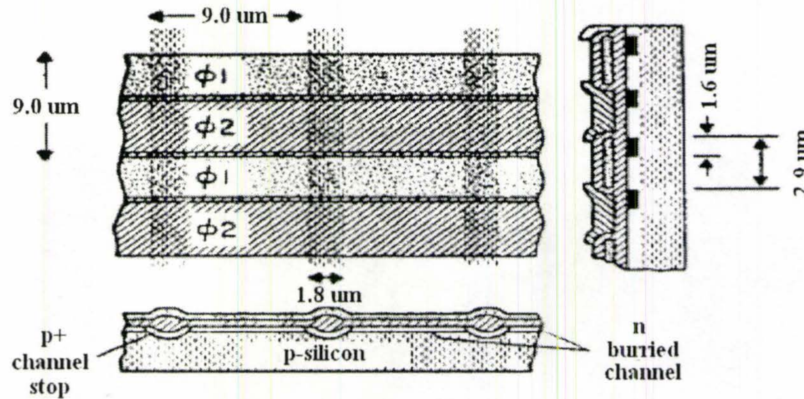


Figure 1-7: Top and cross-sectional views of a CCD array. Charges are transferred within columns with a two-phase mechanism. Columns are separated with a thick field oxide and a p^+ channel stop (Taken from [1.25], Fig. 3).

The above collected charge should be measured. CCDs do not have a charge measurement unit for each cell, but for each line of cells, or even the whole device. Cells are put closely in a line (the columns in Figure 1-7, or the rows in Figure 1-8), and their charge is handed over one by one to the end of the line. This is like people of a village trying to extinguish a fire by standing in a row between the fire and the water well, handing over buckets of water. At the end of the row, the charge will be emptied in the measuring unit.

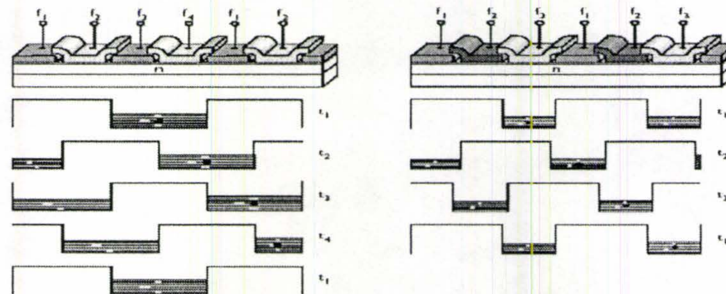
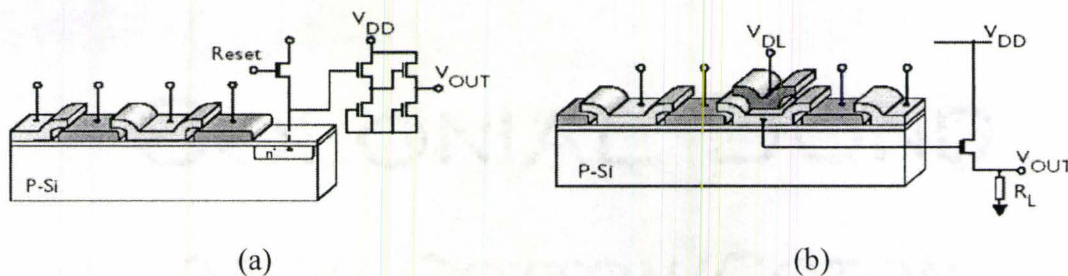


Figure 1-8: Four phase and three phase mechanisms of charge transfer in CCD arrays (Taken from [1.26], Fig. 5).

The process of charge transfer is performed by controlling the gate voltage of cells. Assume that two cells are next to each other, one with an inversion layer under the high voltage gate, and the other empty of charge with a low voltage gate. If the gate voltages are swapped, charge will be transferred between cells. The process of

swapping voltages should be carefully controlled to assure the correct direction of charge movement. Different approaches use different number of cells per pixel to perform this job. (Figure 1-8)

Finally the collected charge should be read in the output node. A small sensing capacitor is used to convert the signal charge to a voltage which can be amplified before transmission. The performance of this stage is judged in terms of its charge conversion efficiency (CCE), the voltage generated per unit charge. The output structure achieves this by dumping the charge on a floating n^+ region, or into a storage capacitor underneath a floating gate.



(a) (b)

Figure 1-9: Two output node structures for the CCD array: (a) Floating diffusion, and (b) floating gate (Taken from [1.26], Fig. 3).

Figure 1-9 shows the two possible output node structures. The floating diffusion node is the most common because of its easy fabrication. Then, the charge should be reset after each readout cycle. The voltage in this structure is linearly amplified (on chip) before sending out. The floating gate method on the other hand, doesn't need the reset mechanism (the charge can be sent to substrate). This can be important because reset operation introduces thermal noise which is different from pixel to pixel. It also has the advantage of being nondestructive. As drawn in the image above, the charge can still travel into the row of cells after sensing.

1.2.3. PMT

The photoelectric effect was discovered by Hertz in 1887, through exposing a negative electrode to UV radiation. Due to photoelectric effect, a material emits electrons after being exposed to photons with high enough energy. Photomultipier tubes, PMTs, use this phenomenon to convert photons into electrons, and then

multiply them to produce the output signal. PMTs became practical after the discovery of a compound photocathode (made of silver, oxygen and cesium, also called S1) that had photoelectric sensitivity about two orders of magnitude more that previously used photocathode materials.

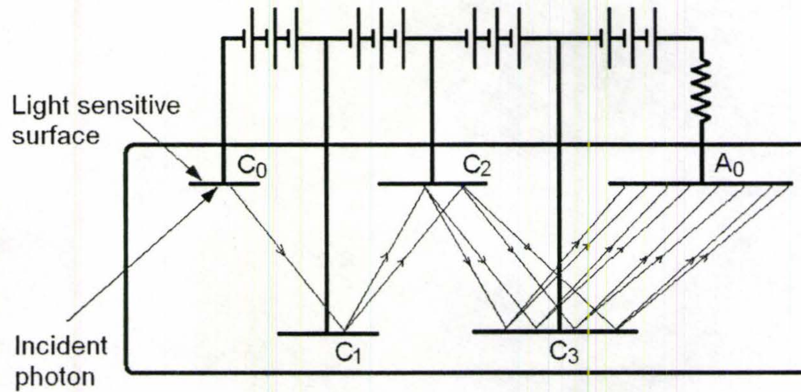
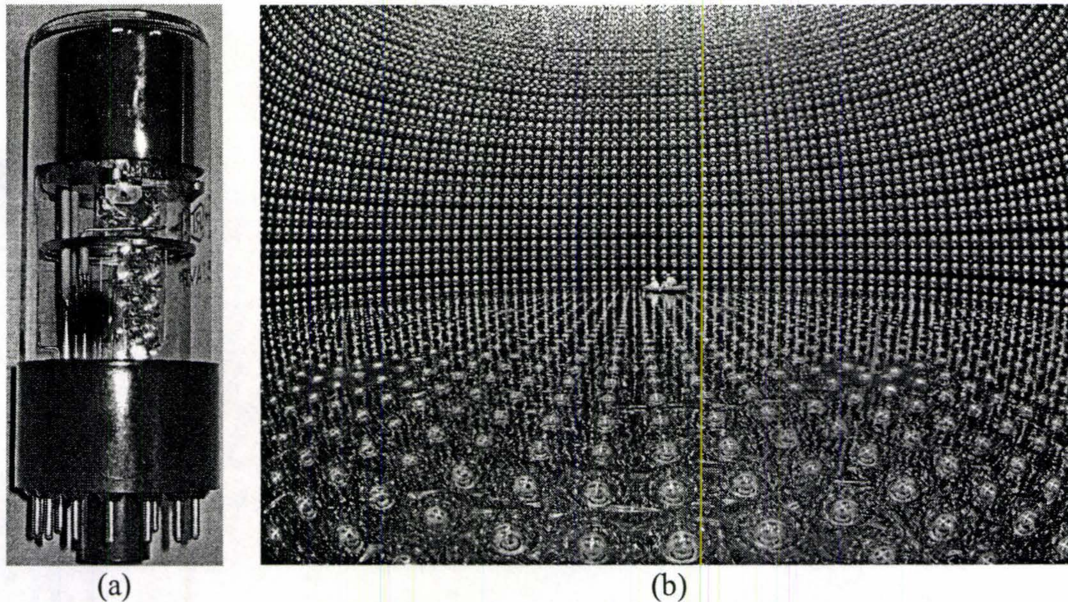


Figure 1-10: Simplified structure of a PMT. A single incoming photon can result in a significant current at the PMT anode.

Light is detected in a photomulipler tube through the following processes. First, light passes through the input window. Second, light excites the electrons in the photo-cathode (C_0 in Figure 1-10) so that photoelectrons are emitted into the vacuum. Third, photoelectrons are accelerated and focused by the focusing electrode onto the first dynode (C_1 in Figure 1-10) where they are multiplied by means of secondary electron emission. This secondary emission is repeated at each of the successive dynodes. Finally, the multiplied secondary electrons emitted from the last dynode (C_3 in Figure 1-10) are collected by the anode (A_0 in Figure 1-10). Figure 1-11(a) shows a simple PMT.



(a) (b)

Figure 1-11: Photomultiplier tube (Taken from [1.27]). An 11200 PMT array, made in super-K neutrino observatory in Japan. The colossal structure is filled with 50000 tons of pure heavy water to detect subatomic particles thrown by supernovas billions of miles away (Taken from [1.28]).

The combination of high gain, low noise, high frequency response and large area of collection have meant that these devices still find applications in nuclear and particle physics, astronomy (Figure 1-11(b)), medical imaging and motion picture film scanning. Semiconductor devices like avalanche photodiodes are replacing photomultipliers in some applications, as we will discuss in Chapter 5, but photomultipliers are still used in most cases.

1.3. Integrated photodetectors

The earliest solid-state image sensors were the bipolar and MOS photodiode arrays developed by Westinghouse, IBM, Plessy and Fairchild in the late 1960's [1.29]. The three-transistor APS was first described by Noble in 1968 [1.30]. The 1970's and 1980's were mostly dominated by research and development of CCD arrays. The MOS structure was researched again by Andoh at NHK, in collaboration with Olympus and Mitsubishi Electric, since the late 1980's [1.31].

CMOS image sensors can offer low-power and high-speed operation, and simultaneously, a much higher level of device integration. The advances in deep

submicron CMOS technologies and integrated microlens have made CMOS image sensors a practical alternative to the long dominating CCD imaging technology. Perhaps the main advantage of CMOS image sensors is that they are fabricated in standard CMOS technologies, which allows for full integration of the image sensor along with the analog and digital processing and control circuits on the same chip, and its lower cost. This camera-on-chip system leads to the reduction of power consumption, cost and sensor size and it also allows for integration of new sensor functionalities.

1.3.1. Imaging system

A simplified diagram of an imaging system architecture is shown in Figure 1-12. The first step is to focus the scene on the plane of the image sensor, in the optical setup of the imager. Advanced imagers have an array of microlenses deposited on the image sensor to focus the light on top of each pixel on the light sensitive area of the pixel. Color imagers use a color filter array, CFA, to capture the color information of the scene. A CFA consists of an array of band pass filters for red, green and blue colors.

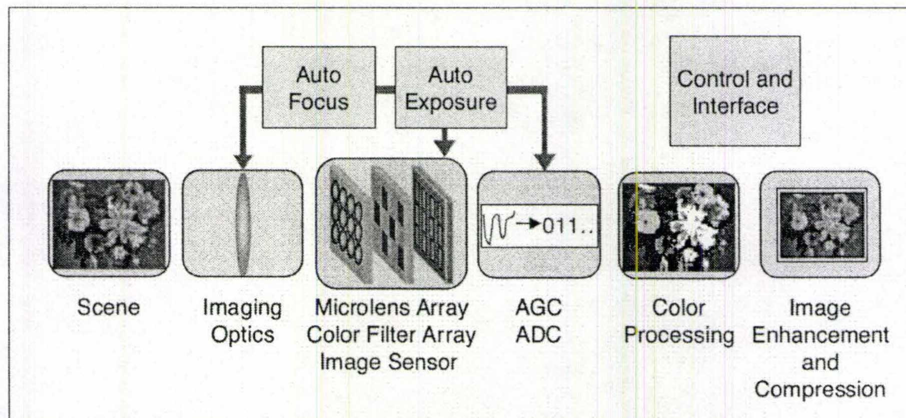


Figure 1-12: Block diagram of an imaging system (Taken from [1.32], Fig. 1)

The output of the image sensor is digitized by an ADC unit. Color correction and white balancing is applied to the image in photography applications. Finally, the image is converted to the desired data format to be transmitted out of the imaging system.

1.3.2. Advantages of CMOS photodetectors

A CMOS imager can be integrated with the ADC, color processing and image enhancement and compression units on the same chip as the image sensor. This will drastically reduce the size of the imaging system and its cost. Another immediate advantage of using CMOS imagers is their low power consumption. These advantages make CMOS imagers a good candidate for miniaturized and hand-held imaging systems.

Compared to CCDs, CMOS imagers do not suffer from smear and blooming. In the CCD structure, during readout, the stored charge packets are shifted towards the output node. During this readout time, the CCD is still exposed to light and the photo-generation can contaminate charge packets transferring through the cell, that belonged to another pixel. This effect is called smear and can be minimized by either having a second shielded row of CCD pixels, for shifting the charges, or by ensuring that the shift register is read out in an effectively shorter time interval than the integration time of the device. Although both solutions are effective, the first one limits the fill-factor of the device, and the second one limits its frame rate.

Figure 1-13: A late afternoon landscape picture of Hamilton lakeshore taken by a Canon PowerShot A60 digital camera, which uses a 2 Mega-pixel CCD imager. Blooming is observed in the column of pixels that are in line with the sun.

Electrons and holes that are generated under a pixel can diffuse to the neighboring pixels. Thus, a pixel may generate an output signal that is corresponding to another

pixel, and as a result, the total quality of the image will be degraded. The diffusion of carriers to the neighboring pixels in CMOS detectors can be prevented by putting pixels in separate wells, or by creating SiO_2 trenches around the pixels. The same tricks can be applied to separate CCD columns. However, charge transfer mechanisms of CCDs do not permit total isolation of pixels in a column, and as a result blooming is not avoidable even in most modern CCD cameras as shown in Figure 1-13.

1.3.3. Limitations of CMOS photodetectors

The architecture of CMOS photodetectors and imagers are limited by the design rules of standard CMOS. The depth and doping concentration of the n+ and p+ regions and wells are also fixed by the technology. Therefore, the designer of CMOS imagers has limited room for layout variations. As a result, the performance of the photodetector devices in CMOS is very much dependent on the technology, as will be discussed in detail in next section.

CMOS imagers, compared to CCDs, have more complex pixels with in-pixel circuitry. The paths from the pixels to the output are also different for different pixels. As a result, the variation of the device parameters affects the response of different pixels on a CMOS imager, causing significant fixed pattern noise.

The dark current of CCDs is significantly lower than CMOS imagers. This is mainly due to the optimized design of CCDs for dark output. Also, the dark current of CCDs is manly due to the thermal generation of carriers in the depletion region, and the leakage in MOS capacitors is negligible. In photodiodes however, the leakage current can be significant. Although the dark current can be corrected, the dark current shot noise will degrade the output quality of CMOS pixels.

The fill-factor of CMOS pixels is low, compared to CCDs. CCD do not have any in-pixel circuits and they do not need any data buses. On the other hand, CMOS pixels suffer from several layers of metal and silicon dioxide that cover the surface of silicon, as well as the passivation layer that is put on top of the chip at the end of the process. Figure 1-14 shows a schematic of a CMOS photodiode with these layers.

The layers force the light to pass through a deep well, from the top dioxide layer to the silicon surface, resulting in some optical diffraction as well as interference of dioxide layers and cross-talk.

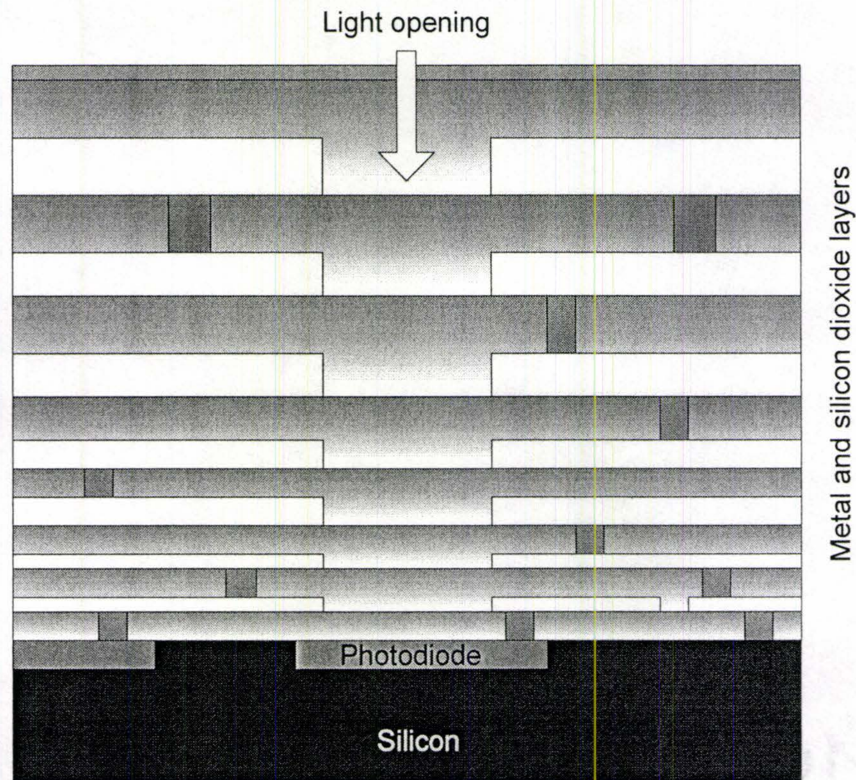


Figure 1-14: A simplified cross-section of a CMOS chip, showing several layers of silicon dioxide and metal on top of the silicon surface. The light has to pass through a deep well, before reaching the surface of the photodiode.

1.4. Effect of scaling

The evolution of CMOS technology has had a significant effect on the characteristics of CMOS image sensors. The minimum feature size of CMOS technology is known to shrink approximately at a scale of 0.7 every three years. This downscaling is, in general, targeted to reduce the cost and increase the clock frequency of digital circuits, like SDRAMs and MPUs. However, analog circuits that are implemented in CMOS technology have not necessarily benefited from this downscaling.

Table 1-2: Principal device technology and electrical characteristics. (Taken from [1.33], Table II, with some modifications)

Year	1980	1983	1986	1989	1992	1995	1998	2000	2002	2004	2007
Min. feature size (μm)	2	1.5	1.0	0.7	0.5	0.35	0.25	0.18	0.13	90 nm	65 nm
L_{eff} (μm)	1.6	1.2	0.8	0.6	0.42	0.28	0.2	0.14	90 nm	65 nm	45 nm
Isolation	LOCOS	LOCOS	LOCOS	LOCOS	LOCOS	LOCOS	LOCOS	STI, SOI	STI, SOI	STI, SOI	STI, SOI
Gate oxide	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2/ON	ON	ON	ON
Gate oxide (nm)	41-47	29-50	20-35	14-24	10-17	7.4	5.8	2	1.5	1.1	0.8
Gate electrode	n+ poly	n+ poly	n+ poly, silicide	n+ poly, silicide	n+, n+/p+ poly, silicide	n+, n+/p+ poly, silicide	n+, n+/p+ poly, silicide	n+, n+/p+ poly, silicide	n+, n+/p+ poly, silicide	n+, n+/p+ poly, silicide	n+, n+/p+ poly, silicide
Substrate doping (cm^{-3})	10^{16}	2×10^{16}	4×10^{16}	8×10^{16}	1.2×10^{17}	2.5×10^{17}	3.4×10^{17}	5×10^{17}	7×10^{17}	1×10^{18}	2×10^{18}
Source/drain junction	Abrupt	Abrupt	LDD	LDD	LDD	LDD, S/D ext	LDD, S/D ext, raised S/D	LDD, S/D ext, raised S/D	LDD, S/D ext, raised S/D	LDD, S/D ext, raised S/D	LDD, S/D ext, raised S/D
Source/drain junction depth (μm)	0.5-0.6	0.45-0.55	0.4-0.5	0.35-0.45	0.3-0.4	0.2-0.3	0.1-0.15	0.07-0.13	48 nm-95 nm	27 nm-45 nm	18 nm-37 nm
Power supply (V)	5	5	5	5	5	3.3	2.5	1.8	1.2	1	0.8
Threshold voltage (V)	1.0	0.9	0.8	0.7	0.6	0.5	0.43	0.37	0.34	0.3	0.3
Threshold voltage variation (mV)	170	125	80	75	75	60-70	50	40	30	25	20

Table 1-2 shows the downscaling of CMOS technology and variation of corresponding device parameters in the past 30 years. The constant decrease of the power supply voltages and the threshold voltages can be observed in Table 1-2. As an immediate result, the design of the signal amplification circuits becomes challenging due to the small analog voltage swing. Further, the decrease of gate-oxide thickness also increases the leakage current of the gate of the MOS transistors and degrades the performance of the input stage of analog circuits. In this section, we will discuss how these changes affect the CMOS image sensors.

1.4.1. Effect on Photodiodes

The carriers that are generated within the depletion region of a photodiode are detected immediately. Many of the photo-generated carriers, however, are not generated within the depletion region. They are generated in the neutral substrate and they diffuse to the photodiode active region. The diffusion length of these minority carriers, in the case of electrons for example, is given by:

$$L_n = \sqrt{D_n \tau_n}\,, \tag{1-2}$$

where τ_n is the carrier lifetime and D_n is the diffusion coefficient of electrons. The diffusion coefficient and mobility are related by the simple Einstein relation:

$$\frac{D}{\mu} = \frac{kT}{q}\,. \tag{1-3}$$

For intrinsic silicon, $D_n = 35\ \mathrm{cm^2/s}$. Carrier lifetime is greatly dependent on the quality of the silicon crystal. For intrinsic silicon, τ_n can range from 1 ms to 1 μs. Both of these parameters depend on the substrate doping concentration, and they both decrease as the doping levels increase with technology down scaling. As a result, carriers that are generated deeper in the substrate have less chance of diffusing to the photodiode active area. Therefore, the spectral response of the photodetectors shifts towards blue and UV as the technology scales down.

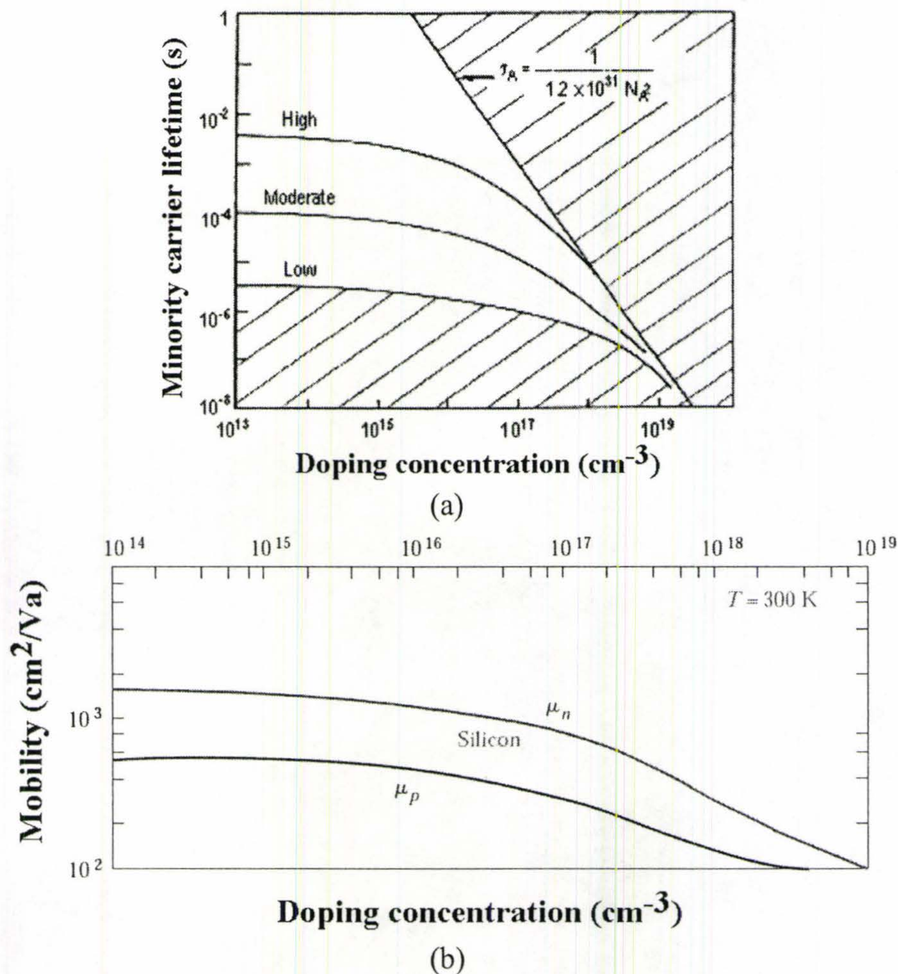


Figure 1-15: (a) Lifetime and (b) mobility of minority carriers in silicon. Both of the parameters decrease as the doping concentration level increases. (Taken from [1.34] and [1.36], Fig. 3-23).

We discussed in the previous section that in a CMOS photodiode, light has to pass through several layers of silicon dioxide and possibly dielectrics to reach the silicon surface. The number of metal layers, and the depth of the well that is shown in Figure 1-14, increase as the technology scales down. The photons will then have more chance of being diffracted, or trapped and reflected within the oxide and metal layers before reaching the silicon surface, reducing the optical quantum efficiency.

Scaling also affects the dark current. Although the thermally induced dark current remains fairly constant with device scaling, tunneling plays a significant role in devices fabricated in deep submicron CMOS technologies. This is a direct result of increased substrate doping concentration and narrower depletion regions. We will

elaborate this fact in more detail when we study the dark count of APDs in section 5.6.2.

1.4.2. Effect on APS arrays

The immediate positive effect of CMOS downscaling on the image sensors is the possibility of making smaller pixels and achieving higher resolutions. Figure 1-16(a) shows the pixel sizes reported for different CMOS imagers in literature. All the reported imagers use a three-transistor pixel structure. Downscaling of CMOS technology makes it possible to make smaller transistors. As a result, same pixel structures can be made in smaller areas as shown in Figure 1-16(b).

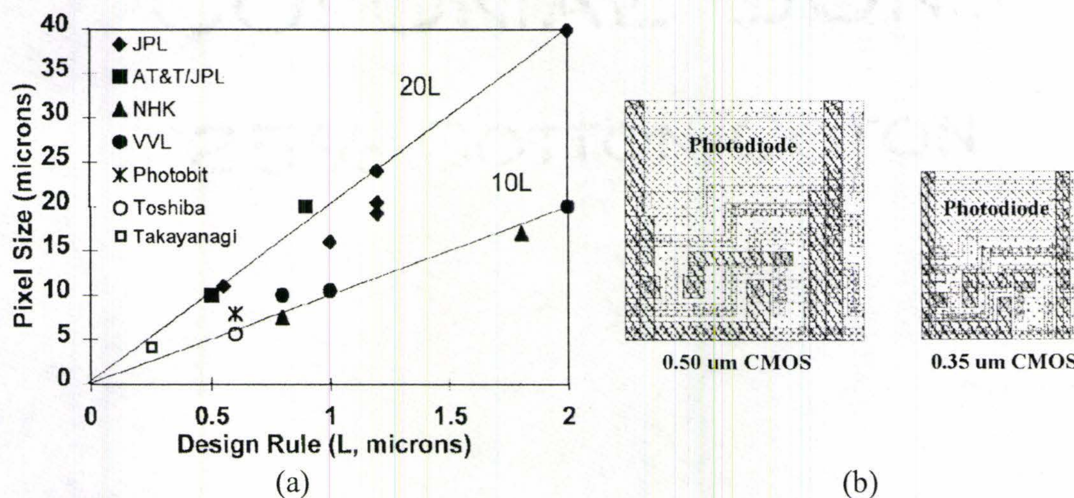


Figure 1-16: (a) Different pixel sizes for CMOS image sensors. The pixel size shrinks by downscaling of CMOS technology, resulting in higher possible resolutions (Taken from [1.35], Fig. 12). (b) Sample APS layouts for a 0.5 μm technology (10 μm pixel) and a 0.35 μm technology (7 μm pixel) (Taken from [1.33], Fig. 2).

It is important to mention a physical phenomenon here that limits the practical pixel size of any imager array. Diffraction is an optical effect that limits the resolution of an imager – no matter how many mega-pixels the camera may have. When light passes through a small opening (camera lens, or the diaphragm opening), it diffracts. As a result, the focused image on the plane of the imager blurs. This blurring becomes more significant for a smaller diaphragm opening, which is called aperture in photography. Aperture comes in f-units, and gets larger for a smaller opening. Aperture is important in photography, as it controls the depth of field (DOF). In

photography, DOF is the distance in front of and beyond the object that appears to be in focus. To increase the DOF, the aperture has to be increased. To decrease the diffraction, aperture has to be decreased. Thus we have conflicting requirements.

The diffraction limit is given by *d*, which is the minimum diameter of spot of light that can be formed at the focus of a lens. The diffraction limit is given by

$$d = 1.22\lambda \frac{f}{A}, \tag{1-4}$$

where λ is the wavelength of the light, f is the focal length of the lens, and A is the diameter of the beam of light (limited by aperture). For example, the Canon EOS-20D camera, with a 55 mm lens, at around f/11, for 510 nm light, has a diffraction limit of about 6.4 μm.

In Section 2.5, we will show that a practical upper limit on the signal-to-noise ratio of a three-transistor active pixel sensor is given by

$$\mathrm{SNR}_{\max} = 10\log(V_{\mathrm{DD}} C_{\mathrm{PH}} / q), \tag{1-5}$$

where V_{DD} is the source voltage and C_{PH} is the capacitance of the photodiode. Assuming that the photodiodes are all n^{+}/p-sub, the junction capacitance of an abrupt junction is given by

$$C_{\mathrm{PH}}(v) = \frac{A}{2}\sqrt{\frac{2q\varepsilon}{v+\varphi} N_a}, \tag{1-6}$$

where A is the area of the diode, and N_a is the doping concentration of the substrate. Replacing v in (1-6) with V_{DD} and applying it to (1-5), we can evaluate how the maximum SNR varies as the technology scales down. Parameters that are affected with technology scaling are V_{DD}, N_a and A. These parameters are extracted according to Table 1-2. Figure 1-17 shows how the maximum achievable SNR varies with the technology feature size. We have assumed that the pixel scales down proportional to the CMOS minimum feature size, as shown in Figure 1-16. The photodiode area is assumed to be:

$$A = (10 \times L_{min})^2, \tag{1-7}$$

where L_{min} is the CMOS technology feature size.

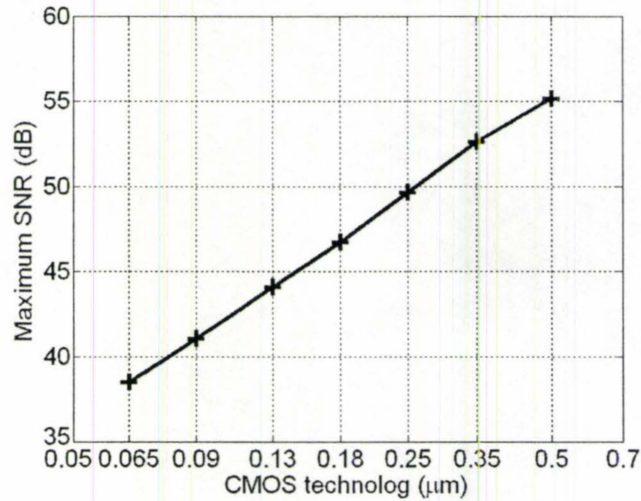


Figure 1-17: The maximum SNR that can be obtained from an APS pixel decreases as the technology scales down. The calculations are done assuming that the pixel size scales down proportional to the technology feature size.

1.4.3. Effect on APD detectors

In Chapter 5 we will introduce an integrated photodetector, called avalanche photodiode (APD), that operates in the breakdown region of the photodiode. The method requires the breakdown mechanism of the photodiode to be avalanche. This makes implementation of APDs in deep sub-micron CMOS challenging, if not impossible. In the next paragraph, we explain why.

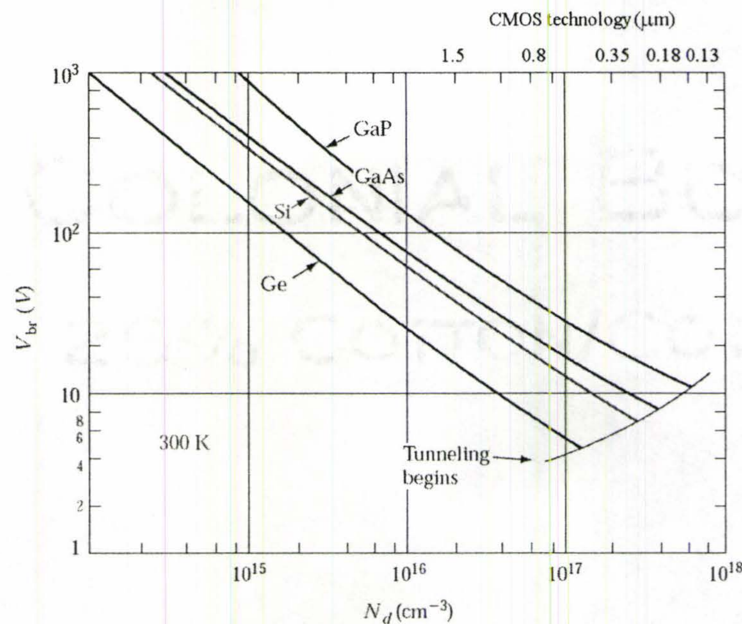


Figure 1-18: Variation of avalanche breakdown voltage in abrupt p$^+$/n junctions, as a function of donor concentration on the n side, for several semiconductors (Taken from [1.36], Fig. 5-22).

Table 1-2 shows that as the technology scales down, the level of doping concentrations in CMOS goes up. As a result, the width of the junction depletion regions of the diodes made in CMOS technology becomes smaller, and their breakdown voltage drops. Figure 1-18 shows the variation of the breakdown voltage with the doping concentration. It should be noted that the measured breakdown voltages of Figure 1-18 correspond to corner breakdown of the corresponding diodes. Considering Table 1-2, Figure 1-18 predicts that 0.18 μm is the smallest scale technology that can accommodate an integrated APD. We will elaborate this fact further in Chapter 5.

1.5. Signal notations

In this work, we will follow the IEEE notation, as described in the standard [1.37]. Variables are named with the following convention:

Incremental small-signal quantities: all lower case (i_d).

Quiescent large-signal quantities: all upper case (I_D).

Instantaneous total values: lower case variable with an upper case subscript (i_D).

RMS values: upper case variable with a lower case subscript (I_d).

All the variables are italic. The subscripts are italic for single characters (v_S), and normal for digits (v_0), or two or more characters (i_{PH}). And for device elements:

Physical parameters: All upper case (C_{PH}).

Incremental model parameters: All lower case (g_m, r_o).

1.6. Outline of thesis

The rest of this thesis is formatted as follows. Chapter 2 introduces the basic three-transistor active pixel sensor (APS). It gives an overview of the previous implementations of APS in the literature, and then presents some signal and noise analysis. Chapter 3 starts with an overview of the reported APS variations in the literature. Then, it introduces our implemented variations of APS and discusses their advantages and disadvantages. Chapter 4 presents a new mode of operation for APS, using the DC level of the sense node voltage, that results in improved low-light-level sensitivity. In Chapter 5, avalanche photodiode (APD) will be introduced as a tool for single photon detection. In all the above chapters, we have combined the theoretical analysis with measurements done on the corresponding devices and circuits that we have fabricated in 0.18 μm CMOS technology. Finally Chapter 6 concludes with a summary of this work and recommended areas for future research.

1.7. Contributions

The research that is performed during this PhD work and presented in this thesis, has resulted in several publications. Here are the highlights of some of the major contributions done in this work:

Signal to noise ratio of the active pixel sensor is a measure of the quality of its output and it should be maximized. The SNR of a conventional APS is a function of several parameters. It can however be optimized for a certain duration of integration time. In [1.38], we have calculated this optimum operation point, shown that this maximum SNR is a property of the pixel and does not change with the level of incident light.

The analysis of the APS signal, that was previously reported in the literature, did not consider the voltage variation of the photodiode capacitance, or modeled the photodiode as an abrupt junction. We have shown that this analysis results in inaccurate signal prediction. We have performed C-V measurement and analysis on the APS photodiode fabricated in modern CMOS technology and obtained accurate C-V model for the photodiode that can precisely model the output signal of the APS [1.39].

There are several variations of the APS structure that incorporate pixel level circuitry. These variations are normally targeted for specific applications. We have designed, measured and compared three most commonly used APS structures in CMOS 0.18 μm technology to find the best structure for low-light-level applications [1.40].

A new mode of operation for the APS has been proposed that can detect light levels down to 10 nW/cm^2 which is about two orders of magnitude lower than the light levels that are detectable by the best conventional APS that are reported in the literature. This mode of operation uses the DC level of the APS sense node, instead of the swing, as the output. It does not change the structure of the pixel, and as a result, keeps its high fill-factor [1.41].

Avalanche photodiodes have been implemented in this work, for the first time to our best knowledge, in CMOS 0.18 μm technology. The APDs are measured and characterized, and their applicability to single photon detection are investigated. We have also designed integrated circuits for active quench and active reset of the APDs in Geiger-mode. Our APDs have a breakdown voltage of 10.2 V, a probability of detection of a single photon of about 5.5%, a dead-time of 30 ns, and a dark count of about 50 kHz [1.42].

This thesis uses some of the material presented in the publications mentioned above.

Chapter 2

THREE-TRANSISTOR ACTIVE PIXEL SENSOR (APS)

2.1. Introduction

2.1.1. Passive pixel sensor circuit

The passive pixel sensor (PPS) is the earliest and most simple CMOS pixel structure. In this structure, each pixel consists of a photodiode and a row-select transistor. Figure 2-1 shows the PPS structure. The PPS uses an integrating approach to detect light. Each operation cycle of the pixel can be divided into two periods. During the integration period, the select transistor is open and the photodiode is floating. The internal capacitance of the photodiode integrates the photocurrent and the dark current that is generated. At the end of the integration, rows are selected one at a time, and connected to the column read buses. The pixel charges are read in parallel for pixels in each row. Then, the photodiodes are reset to become ready for the next integration cycle. Finally, the select transistor is turned off again and the pixel is ready for the next cycle. The PPS has only one transistor per pixel, and thus has the highest FF. However, column readout of the rather small integrated charge of the photodiodes, significantly reduces the performance of this approach.

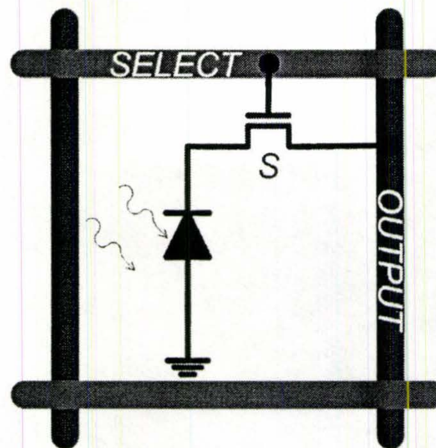


Figure 2-1: PPS pixel structure. Pixel readout and reset are both done at the column level. PPS is the most simple CMOS structure with highest fill-factor.

2.1.2. Three transistor active pixel sensor circuit

Figure 2-2 shows the widely used three-transistor APS circuit. The pixel consists of an n^+/p-sub photodiode, D, and three NMOS transistors. Transistor M_1 is the reset transistor, which resets the photodiode voltage level close to V_{DD} before integration. We call the photodiode voltage, which is shown in Figure 2-2(a) as v_S, the sense node voltage. Transistor M_2 is the source follower, which isolates the sense node from the column read bus. Finally, transistor M_3 is the select transistor, which connects the pixel to the readout bus.

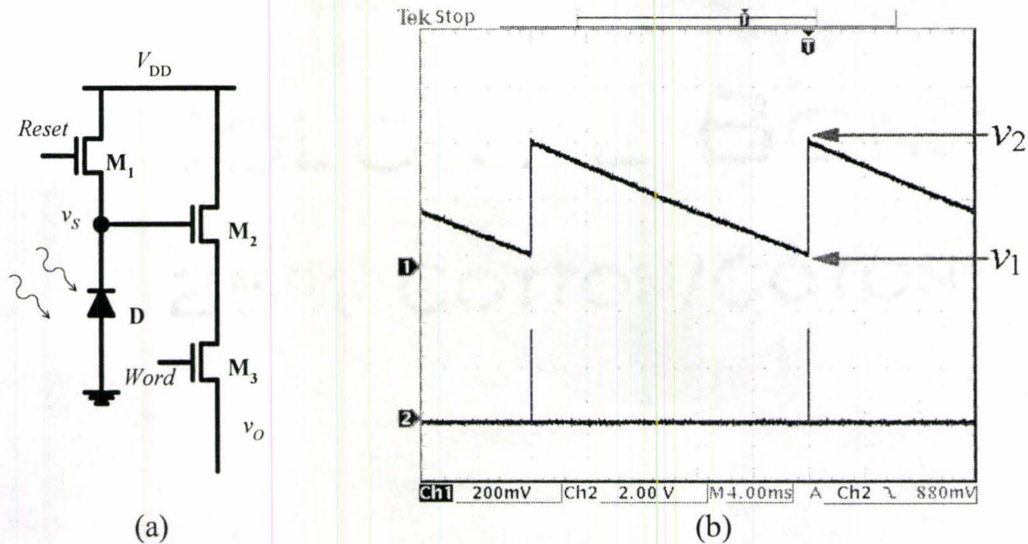


Figure 2-2: (a) Schematic of the three-transistor APS circuit. The dimensions of the photodiode is 20 μ × 20 μ, M_1 is 4 μ / 0.4 μ and M_2 and M_3 are 2.4 μ / 0.4 μ. (b) Applied reset voltage and measured output of the APS. The voltage levels at the beginning and at the end of integration are shown by v_2 and v_1 respectively. The difference (v_2 - v_1) is proportional to the incident light power.

Compared to the PPS structure, APS has two main advantages. First, transistor M_1 performs an internal reset for each pixel. Second, transistor M_2 buffers the sense node, and prevents the small sense node capacitance of being loaded by the large column read bus capacitance. The disadvantage is having two more transistors in each pixel and thus, reduced fill-factor.

The operation cycles of the APS are shown in Figure 2-2(b). Waveform 2 is the applied reset signal to the pixel. The reset signal imposes an integration time of 20 ms, which is equivalent to a frame rate of 50 frames/s. Waveform 1 in Figure 2-2(b) is the output voltage, v_O, which is closely related to v_S. The voltage drops almost linearly during the integration cycle, due to the discharge of the sense node capacitance by the constant photocurrent. The voltage drop, ($v_2 - v_1$), which is about 400 mV in this example, is proportional to the incident light level. The signal analysis during integration will be discussed in depth in section 2.3.

2.2. Overview of APS implementations in literature

Several APS implementations have been reported in the literature. The resolution of the pixels has increased in time with introduction of smaller-scale CMOS

technologies. In 1995, Jet Propulsion Laboratory (JPL) demonstrated a 128 × 128 APS array with on-chip correlated double sampling (CDS) and fixed pattern noise (FPN) reduction circuitry [2.1]. A 640 × 480 APS array with 5.6 × 5.6 μm pixels was introduced by Toshiba in 1997, which had on-chip color filter arrays and microlenses [2.2]. A 800 × 1000 element APS array was also reported by VLSI vision in 1997 [2.3]. A high speed 1024 × 1024 array was introduced by Krymski *et al.* in 1999 [2.4], and an ultra-high speed (10000 frames/s) sensor was introduced by Kleinfelder *et al.* in 2001 [2.5]. A 3840 × 2160 array, with a pixel size of 4.2 μm was suggested in [2.6] by Takayanagi *et al.* for UDTV applications, in 2005.

The above APS implementations all use three-transistor structure of Figure 2-2(a), which is the focus of this chapter. Several variations of the simple APS structure have also been fabricated and reported in the literature. We will cover most of these APS variations in Chapter 3.

2.3. APS signal during integration

During the integration period, the photodiode in the APS structure is floating. As a result, the junction capacitance of the photodiode is discharged by the internally generated photocurrent and dark current. Assuming a constant capacitance for the photodiode, and a constant photocurrent and dark current, then the sense node voltage of Figure 2-2(b), at time t from the beginning of integration, is given by

$$v_S(t) = v_2 - \frac{i_{\text{PH}} + i_{\text{DK}}}{C_{\text{PH}}} t\,. \tag{2-1}$$

In (2-1), v_2 is the sense node voltage at the beginning of integration as shown in Figure 2-2(b), C_{PH} is the junction capacitance of the photodiode, and I_{PH} and I_{DK} are the photocurrent and dark current. The junction capacitance of a diode however is not constant and varies with bias. In this case, it varies with the sense node voltage and as a result, (2-1) is not accurate. In the following subsections, an accurate analysis of the sense node voltage during integration is introduced [2.7].

2.3.1. *C-V* analysis for exponential junction and our *C-V* measurements

In a modern standard CMOS technology, the n^+ and p^+ regions, wells, and channel profiles are made by the ion-implantation method. Ion-implantation offers good control over the number of impurities and their profile. Therefore, junctions produced with this method can be well controlled. The doping profile of implanted impurities has approximately a Gaussian distribution [2.8] given by

$$N(x) = \frac{\Phi}{\sqrt{2\pi}\Delta R_p} e^{-(x-R_p)^2/2\Delta R_p^2}, \tag{2-2}$$

where Φ is related to the doping dose, R_p is the projection range, and ΔR_p is the straggle of the implanted species. Assuming $N(0) = A$ and $|x| << R_p$, then (2-2) can be approximated as

$$N(x) \approx Ae^{x/\beta}, \tag{2-3}$$

where A and β are defined as

$$A = \frac{\Phi}{\sqrt{2\pi}\Delta R_p} e^{-R_p^2/2\Delta R_p^2} \text{ and} \tag{2-4}$$

$$\beta = \frac{\Delta R_p^2}{R_p}. \tag{2-5}$$

Equation (2-3) indicates that if the junction is few standard deviations away from the range of the implantation, which is usually the case in CMOS technology, then the doping profiles at the junction can be approximated with exponential functions. In deep submicron technologies, extremely shallow implanted regions are desired. This calls for reduction of the thermal budget of the process and the creation of as-implanted profiles. Long channeling tails that would thermally be removed now become significant. This causes some deviation from the profile of (2-2), by reducing the slope of the deeper side of the implanted profile in the semi-logarithmic plot [2.8]-[2.10]. The profile however, in the semi-logarithmic plot, stays approximately

linear at few straggles away from the range of the implantation. Thus, the exponential approximation of (2-3) remains valid for such processes, provided adjustments of the parameters defined in (2-4) and (2-5) are made.

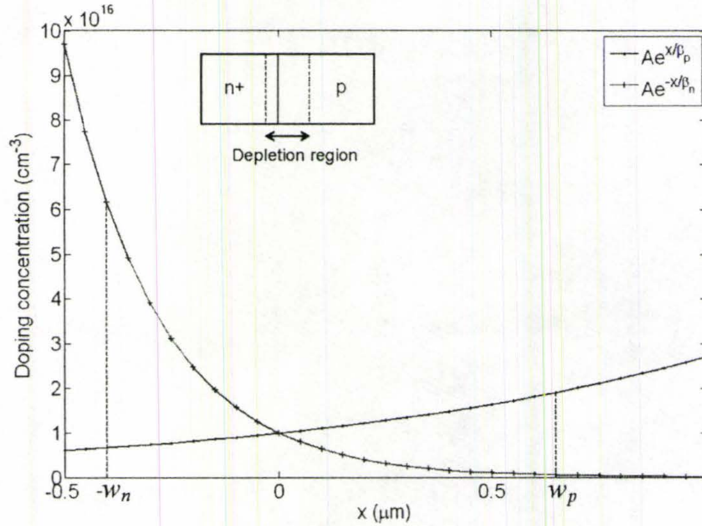


Figure 2-3: Doping profiles at the junction between two ion-implanted regions. Profiles are close to exponential at the proximity of the junction. w_n and w_p are boundaries of the depletion region.

For a pn-junction with exponential doping profiles as shown in Figure 2-3, the voltage drop across the depletion region and the static charge in the depletion region, can be calculated, given the boundaries of the depletion region. Parameters w_n and w_p, in Figure 2-3, indicate the depth of depletion of the n and p sides respectively. Assuming that the n side is more highly doped than the p side, that is $\beta_n << \beta_p$, then $w_n << w_p$ and we get

$$V = \frac{qA\beta_p}{\varepsilon}(\beta_p - w_p)e^{w_p/\beta_p} \text{ and} \tag{2-6}$$

$$Q = qA\beta_p(e^{w_p/\beta_p} - 1), \tag{2-7}$$

where Q is the charge per unit area. The parameter w_p should be eliminated from (2-6) and (2-7), and $dQ/dV|_v$ should be calculated as the voltage-varying capacitance of the junction. A closed form equation for C per unit area, given v, can be derived from (2-6) and (2-7) using a Lambert W function and $C(v)$ is given by

$$C(v)=\frac{\varepsilon}{\beta_p}[1+W(\frac{\varepsilon v}{\beta_p^2 qAe})]^{-1}. \tag{2-8}$$

Note that the Lambert W function is the inverse of the function $f(W) = We^W$ [2.11], [2.12].

Equation (2-8) is the exact equation for the *C-V* characteristic of an exponential junction. However, it does not have a simple form for numerical evaluations and is difficult to be employed in the analysis. A $v^{-1/m}$ characteristic is traditionally assumed for the *C-V* relation of a pn-junction [2.13], [2.14] given by

$$C(v)=C_o\sqrt[m]{\frac{v_0+\varphi}{v+\varphi}}, \tag{2-9}$$

where φ is the built-in potential of the junction, and v_0 and C_0 are the values of photodiode voltage and capacitance at the beginning of integration. Trying to fit (2-9) to (2-8), we found that $m = 4$ is the optimum choice. Note that $m = 2$ corresponds to an abrupt junction, and $m = 3$ to a linear junction. Thus, $m = 4$ can be a good approximation for an exponential junction.

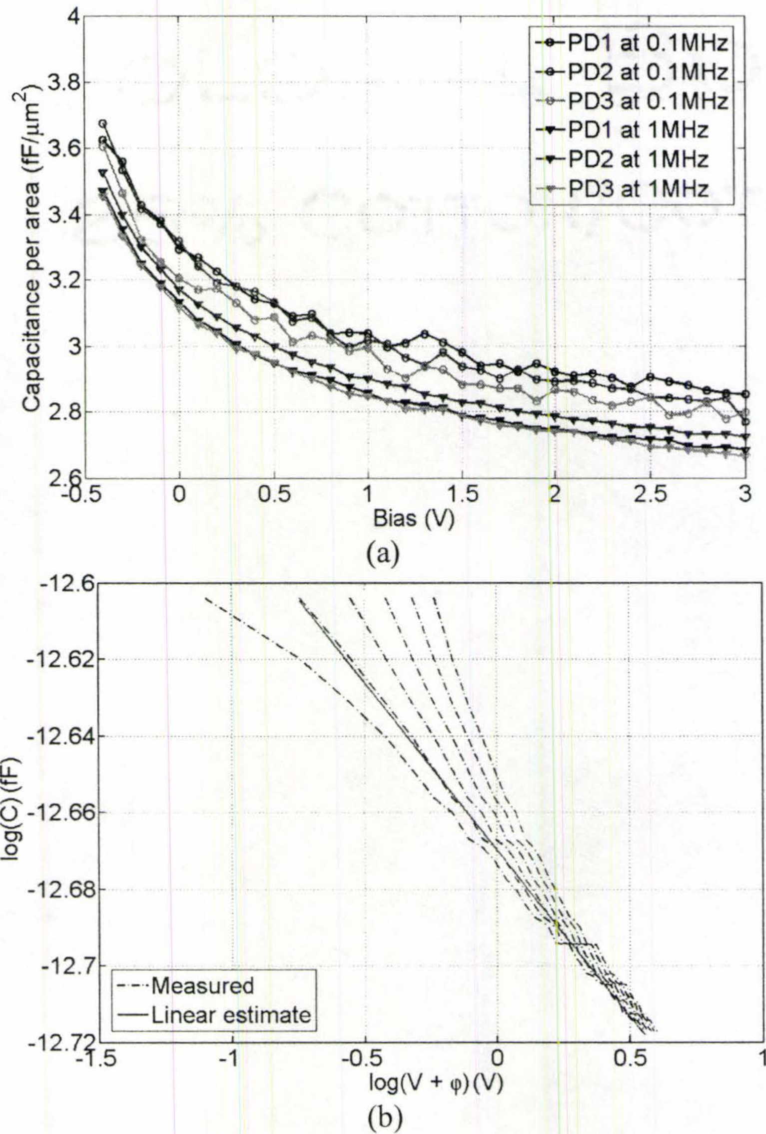


Figure 2-4: (a) Measured *C-V* characteristics and (b) logarithm of capacitance versus voltage for different values of φ. The value of φ which produces a straight line is closest to the built-in potential of the junction.

We measured the *C-V* characteristic of photodiodes fabricated in a commercial 0.18 μm technology to verify the above estimation of m. Measurements are done on 72 μm^2 n^+/p-sub junctions, made separately for the *C-V* measurements, from three different dies at two frequencies. Figure 2-4(a) shows the *C-V* curves obtained from our measurements. In order to extract m, according to (2-9), one can plot $\log(C)$ versus $\log(v + \varphi)$ and relate m to the slope of the curve. However, the actual value of φ is unknown. Multiple plots can be made for different values of φ. The curve which is

closest to a straight line corresponds to the φ closest to the actual built-in potential of the junction. Figure 2-4(b) for $\varphi \approx 0.8$, suggests $m \approx 3.6$, approving that $m = 4$ can be used to describe the diode's *C-V* characteristic.

2.3.2. Analysis of APS signal and comparison to measured APS signal

Figure 2-2(a) shows the active pixel sensor circuit. During reset, transistor M_1 is turned on to bring the sense node voltage (v_S) up close to V_{DD}. During integration, M_1 is opened (in off-state) and the capacitance of the photodiode D will be discharged by its internally generated photocurrent i_{PH} and dark current i_{DK}. In a pinned photodiode APS, a transfer gate is used to transfer the charge to a readout node. In the three transistor structure of Figure 2-2(a), which is considered in this work, the charge is read directly from the sense node. An equation describing the sense node voltage during integration can be written as

$$\frac{dv_S(t)}{dt} \approx -\frac{i_{PH}(t)+i_{DK}(t)}{C(v_S(t))}. \qquad (2\text{-}10)$$

In (2.10), the *dC*/*dt* term is not included. However, considering the small variation of the sense node capacitance during the long integration time, then (2-10) is a good approximation. Equation (2-10) has a closed form solution, assuming constant photocurrent and dark current and (2-9) for the voltage-varying capacitance of the photodiode. This solution is different for different values of *m*. Table 2-1 shows different closed form solutions for (2-10), where v_2 is the value of v_S at the beginning of integration as shown in Figure 2-2(b). Note that these formulas are valid before saturation of the pixel. In the case of saturation, the diode current relation should replace the fixed i_{DK} in (2-10) to obtain v_S.

Table 2-1: Calculated $v_S(t)$ for different values of m. Note that the sense node voltage for $m = 4$ is what was experimentally found in the actual diode used in this work.

m	Junction	Sense node voltage (v_S)
∞	Ideal	$v_2 - \frac{i_{DK} + i_{PH}}{C_0} t$
2	Abrupt	$v_2 - \frac{i_{DK} + i_{PH}}{C_0} t + \frac{(i_{DK} + i_{PH})^2}{4C_0^2}(v_2 + \varphi)^{-1} t^2$
3	Linear	$\left[(v_2 + \varphi)^{2/3} - \frac{2(i_{DK} + i_{PH})}{3C_0}(v_2 + \varphi)^{-1/3} t\right]^{3/2} - \varphi$
4	Actual	$\left[(v_2 + \varphi)^{3/4} - \frac{3(i_{DK} + i_{PH})}{4C_0}(v_2 + \varphi)^{-1/4} t\right]^{4/3} - \varphi$

The choice of m has significant effect on the analytically derived sense node voltage. Figure 2-5 shows different analytic solutions of Table 2-1 for v_S, assuming different values of m. The curves deviate more as time increases. We have fabricated an APS that will be described in the next section. We have measured its output during the integration period that is also shown in Figure 2-5. A good agreement exists between the measured output and the analytic predictions obtained by solving (2-10) for $m = 4$.

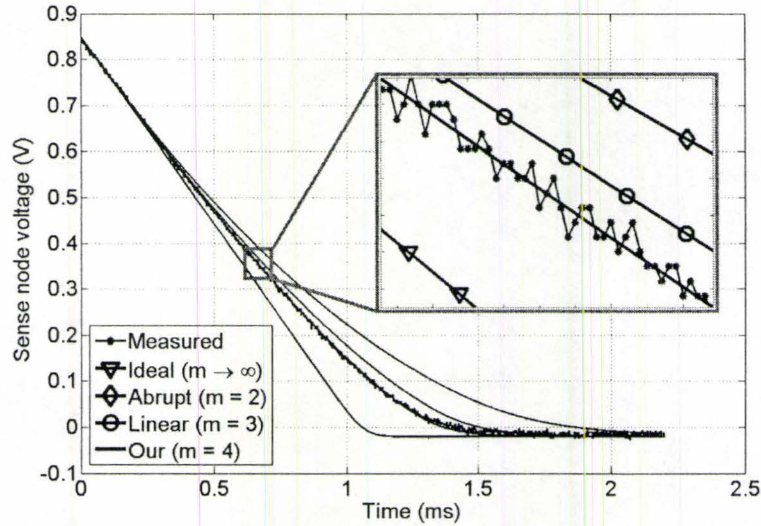


Figure 2-5: Measured and calculated sense node voltage of APS vs. time. The curve is magnified to show that our analytical model best matches the measured APS output. The pixel is saturated in this example after 1.5 ms.

2.4. APS noise

Image sensors suffer from several fundamental and technological non-idealities. The sources of noise in an APS can be divided into two general categories: temporal and fixed pattern noise, FPN. Temporal noise is the most fundamental non-ideality in the APS. This type of noise is independent from pixel to pixel and it changes from frame to frame. The next subsections contain a description of FPN and also several types of temporal noise.

2.4.1. Fixed pattern noise

Fixed pattern noise is the pixel-to-pixel output variation under uniform illumination of the pixel array. This output variation is due to the device and circuit mismatches among the pixels and also the interconnect mismatches across the array. These variations cause two types of FPN: offset FPN, which is independent of the pixel signal, and gain FPN, which is also called photo-response non-uniformity (PRNU).

Offset FPN is fixed from frame to frame but may vary from sensor to sensor. There are more sources of FPN in CMOS imagers compared to CCDs, due to in-pixel circuitry and active readout circuits. Offset FPN can be substantially removed by a method called correlated double sampling, CDS. In this method, the APS output is sampled twice: once at the beginning of the integration period (v_2 in Figure 2-2(b)) and once at the end of the integration period (v_1 in Figure 2-2(b)). Gain FPN however, which might be due to the variation of the photodiode capacitance across the array, is not removed by CDS.

2.4.2. Reset noise

The dominant noise source during reset is thermal noise with the reported value of:

$$\overline{V_n^2} = \frac{kT}{2C_{\mathrm{PH}}}. \tag{2-11}$$

CDS can be used to remove reset noise. However, in some APS circuits and architectures that CDS is not employed, like the one that will be introduced in Chapter 4, reset noise will be present in the APS output.

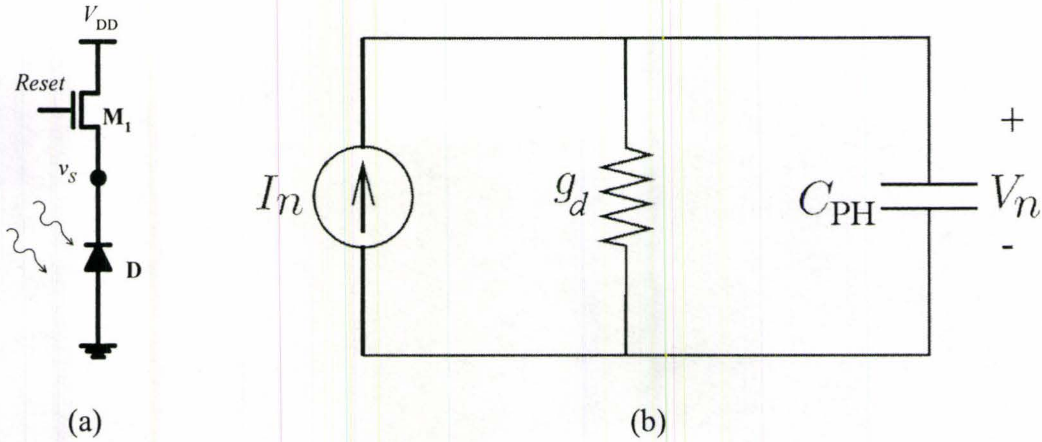


Figure 2-6: (a) APS circuit during reset, and (b) the equivalent small signal circuit used for noise evaluations. I_n is the reset transistor equivalent noise source, g_d is the trans-conductance of M_1 and C_{PH} is the small signal capacitance of the photodiode.

Here, we also present the calculation of the reset noise for a special case when the DC variation of the photodiode voltage is small, and thus we can assume that the transconductance of the reset transistor and the capacitance of the photodiode are constant. The APS circuit during reset is shown if Figure 2-6(a) and the small-signal equivalent circuit for noise analysis is shown in Figure 2-6(b). In this case, the equation governing the output noise is

$$\frac{dV_n(t)}{dt} + \frac{g_d}{C_{PH}} V_n(t) = \frac{I_n(t)}{C_{PH}}. \tag{2-12}$$

The solution to the above equation for fixed g_d and C_{PH} is

$$V_n(t) = \frac{\int_0^{t_r} \frac{I_n(\tau)}{C_{PH}} e^{\frac{g_d}{C_{PH}}\tau} d\tau + K}{e^{\frac{g_d}{C_{PH}}t_r}}. \tag{2-13}$$

Further calculations show that $K = 0$. The mean square of (2-13) is given by

$$\overline{V_n^2} = \frac{1}{e^{\frac{2g_d}{C_{PH}}t_r}} \int_0^{t_r} \int_0^{t_r} \overline{\frac{I_n(\tau)}{C_{PH}} \frac{I_n(\tau')}{C_{PH}}} e^{\frac{g_d}{C_{PH}}(\tau+\tau')} d\tau d\tau' \tag{2-14}$$

and considering the shot noise during reset, we have $\overline{I_n(\tau)I_n(\tau')} = qi_d\delta(\tau-\tau')$ which results in

$$\overline{V_n^2} = \frac{qi_d}{2g_d C_{\text{PH}}}\left(1-e^{-\frac{2g_d}{C_{\text{PH}}}t_r}\right). \tag{2-15}$$

The trans-conductance is defined as $g_d = -di_d/dv_S$. Using the approximation $g_d \approx i_d/v_T$ we will have

$$\overline{V_n^2} = \frac{kT}{2C_{\text{PH}}}\left(1-e^{-\frac{2i_d}{v_T C_{\text{PH}}}t_r}\right), \tag{2-16}$$

which is the exact value of the reset noise. Equation (2-16) is approximated in literature by (2-11). This approximation is valid for the normal conditions of operation of an APS. However, if the reset time becomes small, like the DC mode of operation of the APS that will be introduced in Chapter 4, the exponential term in (2-16) can become significant, and the approximate (2-11) will be inaccurate.

2.4.3. Shot noise

The analysis of shot noise during integration is presented here. During the integration time, the photodiode junction capacitance is discharged with the internally generated photocurrent and dark current. The equivalent small-signal circuit for noise analysis is shown in Figure 2-7.

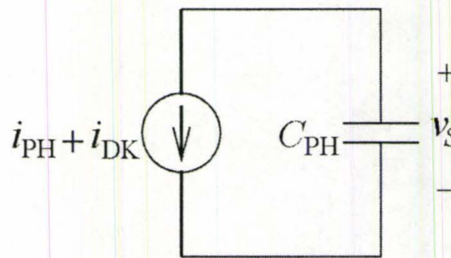


Figure 2-7: Equivalent circuit of the APS during integration.

The equation governing the photodiode voltage during integration, assuming constant photocurrent and dark current, is

$$\frac{d(v_S + V_n)}{dt} = -\frac{i_{\text{PH}} + i_{\text{DK}} + I_n(t)}{C_{\text{PH}}(v_S + V_n)}, \tag{2-17}$$

where the PSD of the shot noise is given by

$$S_{I_n} = q(i_{\text{PH}} + i_{\text{DK}})\ \text{A}^2/\text{Hz}. \tag{2-18}$$

If a constant photodiode capacitance is assumed, then (2-17) can be solved to obtain the noise power.

$$V_n(t) = -\frac{\int_0^{t_{\text{int}}} I_n(\tau)d\tau}{C_{\text{PH}}}$$

$$\overline{V_n^2} = -\frac{\int_0^{t_{\text{int}}}\int_0^{t_{\text{int}}} \overline{I_n(\tau)I_n(\tau')}d\tau d\tau'}{C_{\text{PH}}^2} = \frac{\int_0^{t_{\text{int}}} \overline{I_n(\tau)^2}d\tau}{C_{\text{PH}}^2}$$

$$\overline{V_n^2} = -\frac{q(i_{\text{PH}} + i_{\text{DK}})}{C_{\text{PH}}^2}t_{\text{int}}. \tag{2-19}$$

Equation (2-19) is obtained by assuming a constant capacitance for the photodiode during integration time. To obtain a more accurate analysis [2.15], (2-17) is expanded considering the voltage variant C_{PH} to obtain

$$\frac{dV_n(t)}{dt} - \frac{1}{C_{\text{PH}}^2(v_S(t))}\frac{dC_{\text{PH}}(v_S(t))}{dv_S(t)}V_n(t)(i_{\text{PH}} + i_{\text{DK}}) = -\frac{I_n(t)}{C_{\text{PH}}(v_S(t))}. \tag{2-20}$$

In order to solve (2-20), [2.15] has assumed the (2-9) model for the voltage varying capacitance of the photodiode with $m = 2$ to obtain the total noise power at the end of integration time to be

$$\overline{V_n^2} = \frac{q(i_{\text{PH}} + i_{\text{DK}})}{C_0^2}t_{\text{int}} \times \left(1 - \frac{1}{2(v_0 + \varphi)}\frac{i_{\text{PH}} + i_{\text{DK}}}{C_0}t_{\text{int}}\right)^2. \tag{2-21}$$

Here we present an alternative approach to extract the shot noise at the end of integration time with the more accurate model for the voltage varying C_{PH}. The noise power of the sense node at the end of integration can approximately be written as

$$\overline{V_n^2} \approx q(i_{\text{PH}} + i_{\text{DK}}) \int_0^{t_{\text{int}}} \frac{1}{C_{\text{PH}}(v_S(t))^2} dt \tag{2-22}$$

and after applying the equation for the voltage varying capacitance of the photodiode given in (2-9) for $m = 4$, it simplifies as the following:

$$\overline{V_n^2} = \frac{q(i_{\text{PH}} + i_{\text{DK}})}{C_0^2} \frac{1}{\sqrt{v_0 + \varphi}} \int_0^{t_{\text{int}}} \sqrt{v_0 + \varphi - \frac{i_{\text{PH}} + i_{\text{DK}}}{C_0} t}\, dt$$

$$= \frac{q(i_{\text{PH}} + i_{\text{DK}})}{C_0^2} \frac{2}{3}(v_0 + \varphi) \frac{C_0}{i_{\text{PH}} + i_{\text{DK}}} \times \left[1 - \left(1 - \frac{i_{\text{PH}} + i_{\text{DK}}}{C_0} \frac{t_{\text{int}}}{v_0 + \varphi} \right)^{3/2} \right]$$

$$\approx \frac{q(i_{\text{PH}} + i_{\text{DK}})}{C_0^2} t_{\text{int}} \times \left(1 - \frac{1}{4(v_0 + \varphi)} \frac{i_{\text{PH}} + i_{\text{DK}}}{C_0} t_{\text{int}} \right). \tag{2-23}$$

Let's evaluate the power of shot noise for some sample parameter values. For i_{PH} = 100 fA, i_{DK} = 2.28 fA, C_0 = 22 fF, t_{int} = 30 ms, φ = 0.7 V and v_0 = 2.5 V, the shot noise values are calculated as shown in Table 2-2.

Table 2-2: Shot noise calculated for different analytical models.

Noise model	RMS shot noise, V_n
(2-19)	1 mV
(2-21)	0.95 mV
(2-23)	0.99 mV

Equation (2-21) from [2.15] underestimates the noise. This is mainly due to the photodiode modeling in [2.15] that assumes an abrupt junction for the photodiode. The results show that the simple noise model of (2-19), which is the noise assuming constant photodiode capacitance, is a good approximation.

2.4.4. 1/f noise

To find the output noise power due to the transistor 1/f noise, frequency domain analysis is typically performed. The 1/f noise approximates the state of the integrator at the end of t_{int} to be steady state:

$$\overline{V_n^2} = \int_{f_1}^{f_2} S_I(f)\left|Z(f)\right|^2 df$$

$$= \int_{f_1}^{f_2} \frac{S_{I_d}(f)}{g_m^2(t_r) + 4\pi^2 f^2 C^2} df \,, \tag{2-24}$$

where g_m is the transistor's transconductance, and S_{Id} is the transistor drain current 1/f noise power spectral density (PSD), given in a simple form by

$$S_I = \frac{\alpha_H}{N}\frac{I^a}{f} \ \text{A}^2/\text{Hz}, \tag{2-25}$$

where $a = 2$, N is the number of free carriers[1] and α_H is the Hooge's constant usually given as 2×10^{-3}. Assuming that the impedance of the sense node is dominated by the photodiode capacitance C_{PH}, then we get

$$\overline{V_n^2} = 2 \int_{1/t_{\text{int}}}^{\infty} \frac{\alpha_H}{N}\frac{I^a}{f}\frac{1}{(2\pi f C_{\text{PH}})^2} df$$

$$= \frac{\alpha_H (i_{\text{PH}} + i_{\text{DK}})^a}{N 4\pi^2 C_{\text{PH}}^2} t_{\text{int}}^2 \,. \tag{2-26}$$

The frequency limits are set to $f_1 = 1/t_{\text{int}}$ and $f_2 = +\infty$. These choices for the cutoff frequencies are quite arbitrary. Moreover, the circuit is not in steady state and thus it is not appropriate to use frequency domain analysis.

[1] $J = q\mu_n n_i E \Rightarrow N \approx Ix / q\mu_n AV$, where x and A are the width and area, respectively, and I and V are the total current and voltage across the photodiode, respectively, q is the electron charge and μ_n is the electron mobility.

Here we will discuss the non-stationary 1/f noise model and time domain analysis to obtain more accurate noise power estimates. Now we consider 1/f noise during integration. Similar to the calculation of shot noise, the circuit is not in steady state and thus the frequency domain calculations are not accurate. Here, we propose the simple case at which the 1/f noise source is fed to the fixed capacitance of the photodiode, C_{PH}. The noise power is then

$$\overline{V_n^2(t)} = \frac{q^2}{C_{\mathrm{PH}}^2 A^2} \int_0 \int_0 \varsigma(t_1,t_2) dt_2 dt_1 \,. \tag{2-27}$$

With some suggestions from [2.16] we assume

$$\varsigma(\tau) = \int_{\lambda_L}^{\lambda_H} \frac{1}{4} e^{-2\lambda|\tau|} \frac{4kTAt_{\mathrm{ox}}N_t}{\lambda \log \frac{\lambda_H}{\lambda_L}} d\lambda \,. \tag{2-28}$$

Equations (2-27) and (2-28) give the total 1/f noise at the end of integration to be

$$\overline{V_n^2(t)} = \frac{2q^2 kTN_t t_{ox}}{C_{\mathrm{PH}}^2 A \log \frac{\lambda_H}{\lambda_L}} \int_0^{t_{\mathrm{int}}} \int_0^{t_1} \int_{\lambda_L}^{\lambda_H} \frac{1}{\lambda} e^{-2\lambda(t_1-t_2)} d\lambda dt_2 dt_1 \,, \tag{2-29}$$

where A is the channel area, t_{ox} is the effective gate-oxide thickness, N_t is the trap density and λ_L and λ_H are the lower and higher transition rate bounds in the carrier-number-fluctuation 1/f model that we have used. This model presents a PSD of

$$S_{V_g}(f) \approx \frac{q^2 kTN_t t_{ox}}{2C_{\mathrm{PH}}^2 A \log \frac{\lambda_H}{\lambda_L} f} \,. \tag{2-30}$$

For f inside [λ_L, λ_H], a fixed PSD for $f \ll \lambda_L$ and a 1/f^2 varying PSD for $f \gg \lambda_H$. Thus we claim that (2-28) is a practical and relatively accurate model for 1/f noise.

2.4.5. Read-out stage noise

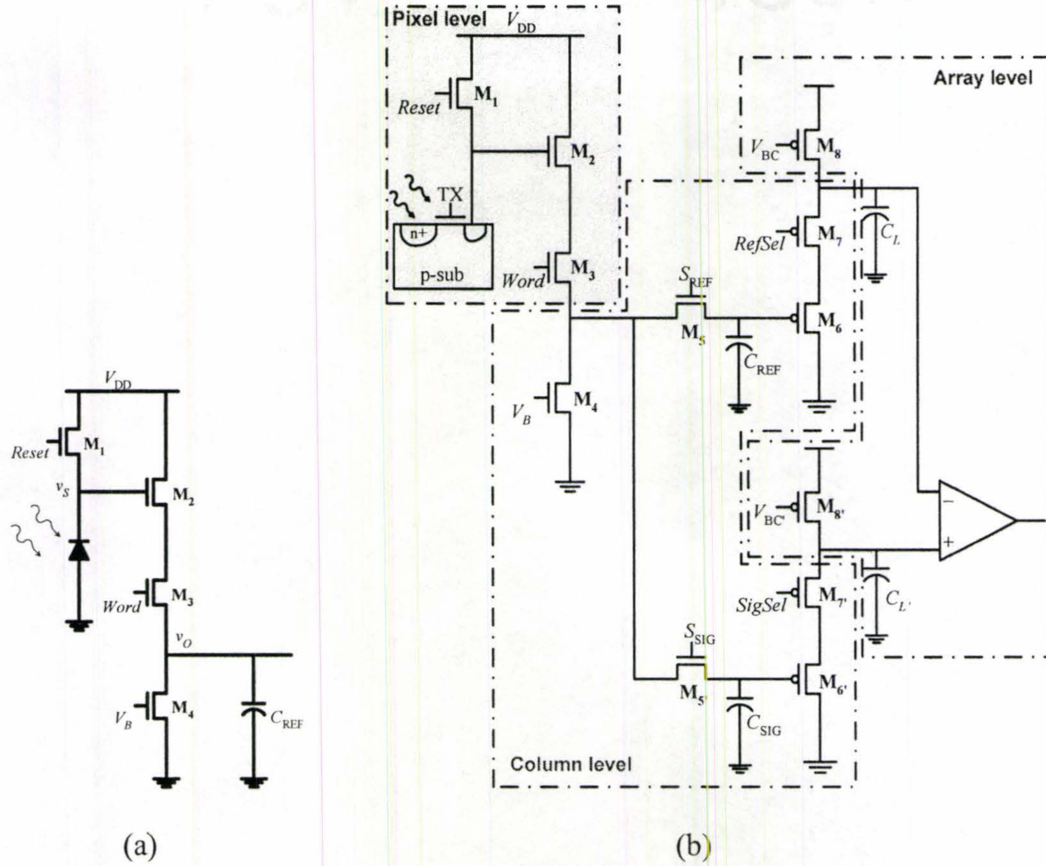


Figure 2-8: APS circuit with (a) column bias transistor and equivalent capacitance of the next stage. (b) Full APS circuit with CDS and read-out stages.

So far, we have only considered the noise that is induced by the photodiode or the reset transistor, M_1. However, during the read-out stage, transistors M_2 and M_3 of the APS pixel are also active. Transistor M_2 buffers the small capacitance of the sense node. Select transistor, M_3, electronically connects the APS output to the column bus. Each column bus is biased with an NMOS transistor, which is transistor M_4 in Figure 2-8(a). Here we will consider the noise contribution of transistors M_2, M_3 and M_4, to the output of the pixel shown in Figure 2-8(a).

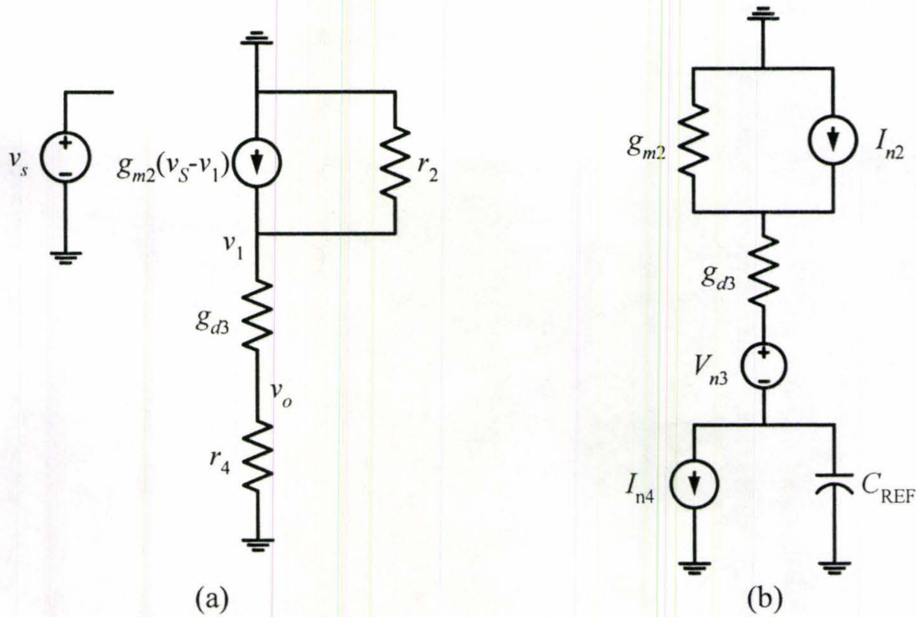


Figure 2-9: Small signal equivalent circuits of the readout stage (transistor M_2, M_3 and M_4 of Figure 2-8(a)) for (a) gain and (b) noise calculations ((b) is taken from [2.15], Fig. 8).

The gain of the buffer stage, which is v_o/v_s in Figure 2-8(a), is close to 1. The exact formula for the gain is obtained by solving the equivalent small signal circuit of Figure 2-9(a), which results in

$$\frac{v_o}{v_s} = \frac{1}{\{1+1/[g_{m_2}(r_2 \parallel r_4)]\}[1+1/g_{d_3}r_4]}, \tag{2-31}$$

where g_{m_2} and g_{d_3} are the transconductance and output conductance values and r_2 and r_4 are the output resistance of the transistors in their respective small-signal models.

The noise of the readout-out stage is calculated by considering the thermal noise of the transistors M_2, M_3 and M_4. Figure 2-9(b) shows the small signal model for noise analysis. Assuming the following PSD for the thermal noise of the MOS transistors,

$$S_I = 4kT\gamma g_m \text{ A}^2/\text{Hz}, \tag{2-32}$$

assuming $\gamma = 2/3$, and defining $\alpha = [1/g_{d_3} + 1/g_{m_2}]$, then the total noise power in the output, due to thermal noise, is given by

$$\overline{V_n^2} = \frac{kT}{C_{\mathrm{REF}}}\left(\frac{2}{3g_{m_2}}\alpha^{-1} + \frac{1}{g_{d_3}}\alpha^{-1} + \frac{2g_{m_4}}{3}\alpha\right). \tag{2-33}$$

Noise of the CDS stage can be calculated in the same way as was done for the readout buffer. Figure 2-8(b) shows the complete APS circuit that includes the CDS and readout stages. The only difference here is that the noise should be doubled as there are two CDS stages in parallel. Thus, with the same calculations, the noise of CDS stage at output will be ($\beta = [1/g_{d_7} + 1/g_{m_6}]$)

$$\overline{V_n^2} = \frac{2kT}{C_l}\left(\frac{2}{3g_{m_6}}\beta^{-1} + \frac{1}{g_{d_7}}\beta^{-1} + \frac{2g_{m_8}}{3}\beta\right). \tag{2-34}$$

2.5. Signal to noise ratio (SNR) of APS

The SNR expression can be obtained by calculating the total noise power using (2-16), (2-23), (2-29), (2-33) and (2-34), and the signal power using Table 2-1. For low-level light, interestingly, the SNR as a function of t_{int} has a peak value that happens before the photodiode fully discharges. Figure 2-10(a) shows the peak occurring for some value of t_{int} (t_{int} = 1.07 s, v_S = 2.16 V, and V_n = 4.3 mV). The peak happens at lower t_{int} as the light level is increased, as shown in Figure 2-10(b). The reason is that as i_{PH} increases, the photodiode discharges faster; thus, the decline in SNR starts at smaller integration times.

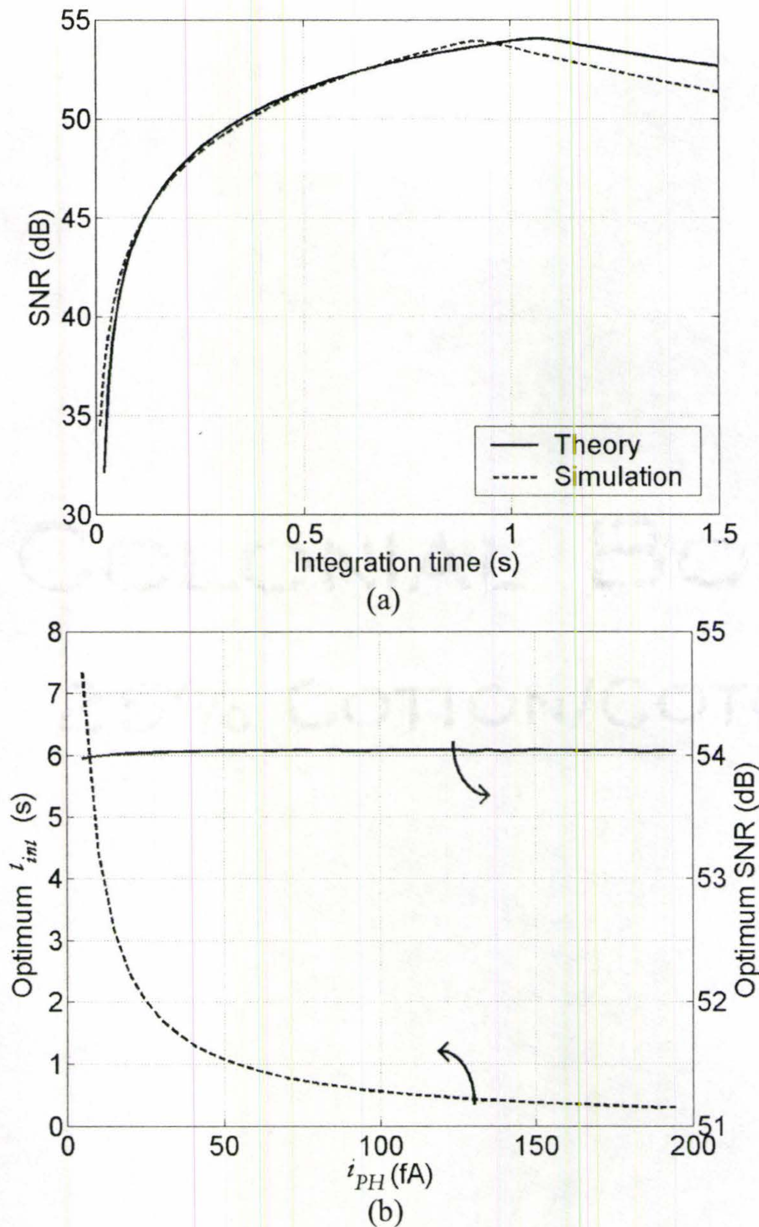


Figure 2-10: (a) SNR of an APS has a peak before the pixel capacitance fully discharges. (b) The optimum integration time decreases as the photocurrent increases. The optimum SNR, however, stays around 54 dB. The reason for the small drop in SNR is that when the i_{PH} value becomes too small, comparable to i_{DK}, the shot noise of i_{DK} becomes important, and the SNR decreases.

2.5.1. Optimum integration time and maximum SNR of pixel

Another interesting result that can be observed is that the maximum achievable SNR by the pixel does not vary with i_{PH}. It is shown in Figure 2-10(b) that the variation in SNR as a function of i_{PH} is negligible. The maximum achievable SNR is a property of the pixel and is not a function of the incident light level. A qualitative explanation can

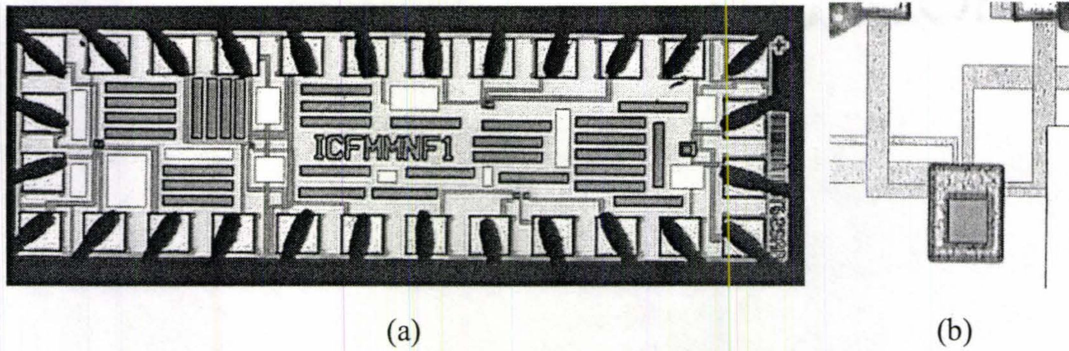
be made considering that the peak SNR happens for integration times very close to the saturation of the pixel. Thus, the signal value $(i_{PH}/C_{PH})t_{int}$ is approximately equal to V_{DD}. Assuming that the noise sources are dominated by the photocurrent shot noise, its power $(qi_{PH}/C_{PH})t_{int}$ can be approximated by qV_{DD}/C_{PH}; thus, the peak SNR will not be a function of photocurrent or integration time, but a function of the capacitance of the pixel and the source voltage ($SNR_{max} \approx 10\log(V_{DD}C_{PH}/q)$). In this example, the maximum SNR is about 54 dB.

The circuit of Figure 2-2(a) is also simulated to verify our theory. We have used the Cadence Spectre analog analyzer for signal and noise simulations of the circuit of Figure 2-2(a). The photodiode is modeled as a diode in parallel to a current source corresponding to the photocurrent. The simulation results, as shown in Figure 2-10(a), follow the analytic SNR very well before the saturation of the photodiode. The simulation suggests that the photodiode may saturate slightly earlier than predicted by our theory, which is due to different models for the leakages of the diode and the transistor in the simulator. Larger leakage currents help the diode to charge faster. The main point that we would like to make here, however, is about the maximum SNR. The maximum achievable SNR of the APS, which is about 53.9 dB, matches our theory very well.

2.5.2. Our measurements

A chip has been designed and fabricated in a commercial CMOS 0.18 μm technology for testing the APS circuit. A photomicrograph of the chip is shown in Figure 2-11(a). The chip has been fabricated, packaged and bonded through CMC[2]. Figure 2-11(b) shows a photomicrograph of an APS circuit on the chip. It corresponds to a pixel with a 20 μm × 20 μm photodiode size. The APS transistors are shielded with a top thick metal layer available in the standard process. The six metal connections to the APS can also be seen in Figure 2-11(b). They correspond to V_{DD}, *GND*, *Reset*, *Word*, and v_O in Figure 2-2(a). There is also a separate connection for the V_{DD} of the reset transistor, to facilitate studying the dynamic range of the pixel, and characteristics of the reset.

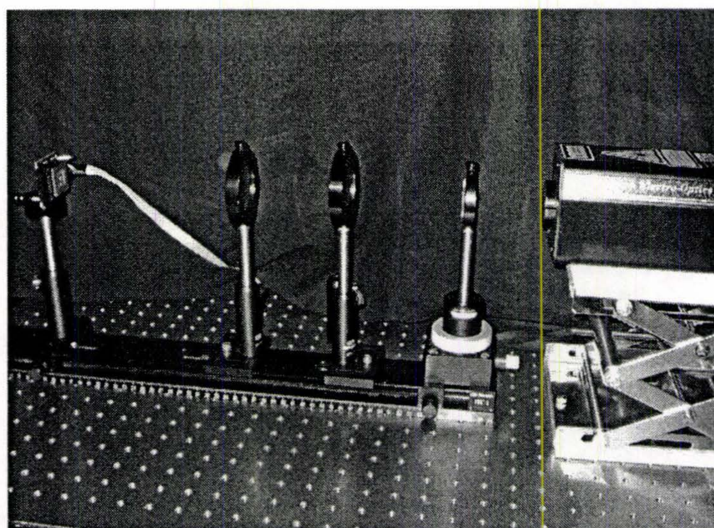
[2] Canadian Microelectronics Corporation. www.cmc.ca



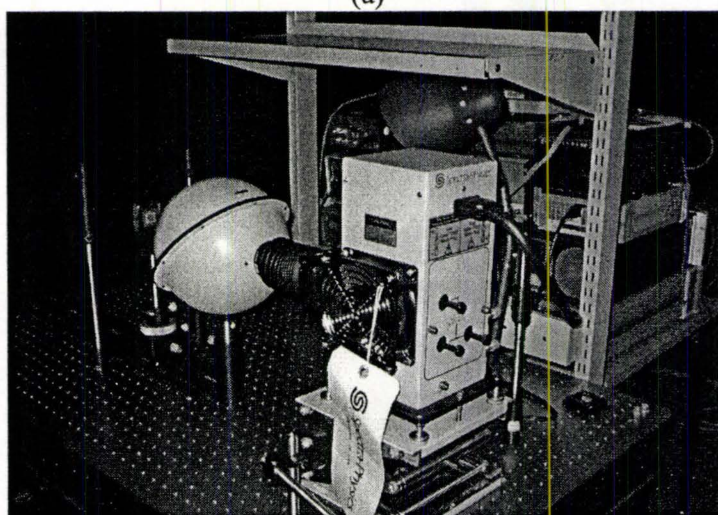
(a) (b)

Figure 2-11: (a) Photomicrograph of the APS chip that is fabricated in this work. The chip is fabricated in standard CMOS 0.18 μm technology. It contains several APS pixels. (b) The zoomed Photomicrograph of the three-transistor APS pixel. The metal layer connections to the pixel can be easily seen in the picture. A thick 6th layer metal shield is designed to cover the peripheral circuitry of the pixel.

Figure 2-12 shows the setups for measurements on the APS. Figure 2-12(a) shows the setup with a 633 nm, 0.5 mW, HeNe Research Electro-optics laser source. Figure 2-12(b) shows the setup with a 75 W, Xenon lamp. Xenon lamps have uniform irradiance over a wide spectrum range covering ultraviolet, visible, and near infrared. They also have good stability in the output power. The lamp is connected to the input port of an integrating sphere through a filter box. The chip is placed on a rail in front of an output port of the sphere. The optical power incident on the chip can be varied by moving it with respect to the sphere. The optical power has been measured by a Newport multi-function optical meter (model 2835-C) and a Newport photodiode (model 818-UV). An integrating sphere scatters light uniformly through multiple reflections along its interior, and provides nearly uniform light flux at its output.



(a)



(b)

Figure 2-12: Optical setups in our dark room for measuring the photoresponse and noise of the APS circuits. The figures show the setups using (a) a laser source and (b) a Xenon lamp. Laser source is used for selective measurement of the photodetector at a certain wavelength. Xenon lamp is used for wide spectral response measurements.

Many precautions are needed for noise measurements. For our measurements, the optical setup was placed on a vibration-isolation table, and the fan that cools the lamp was turned off. Also, measurements were performed in an optically dark room to minimize the background illumination. The dark room in our laboratory also provides 120 dB RF shielding to minimize the external RF disturbances. Finally, stable lamp and voltage sources were used, and connections to the chip were made using triaxial cables.

Results of our measurements will be reported in several places in the following chapters. The APS photo-responses will be discussed and compared in Section 3.2 and measurements on some APS variations will be presented in Sections 3.3 and 3.4. Signal-to-noise ratio of APS will be reported in 4.3. Measurements on avalanche photodiodes will be discussed in Sections 5.4, 5.5 and 5.7.

Chapter 3

IMAGE SENSOR WITH PIXEL-LEVEL PROCESSING

This section will start with a review of some of the variations of the APS. Advantages and disadvantages of each of the structures will be discussed. Then, three different APS structures that are fabricated and measured in this work will be discussed. These APS structures are studied in the context of applications that require low-level light detection systems. The three APS structures studied were – a conventional APS, an APS with a comparator, and an APS with an integrator. A special focus of our study was on both the signal and noise characteristics of each APS structure so the key performance metric of signal-to-noise ratio can be computed and compared. The pixel structures that are introduced in this work can cover a wide range of applications, such as high-resolution digital photography using the APS with a comparator, to ultra-sensitive biomedical measurements using the APS with an integrator.

3.1. Review of APS variations in literature

3.1.1. Photogate APS

The photogate (PG) pixel structure is shown in Figure 3-1 [3.1], [3.2]. Incident photons pass through the PG and generate electrons that are stored in the potential well beneath the gate. The TX transistor allows the reset and signal levels to be read

through different channels utilizing true correlated double sampling (CDS), which reduces both reset noise and fixed pattern noise (FPN) [3.3].

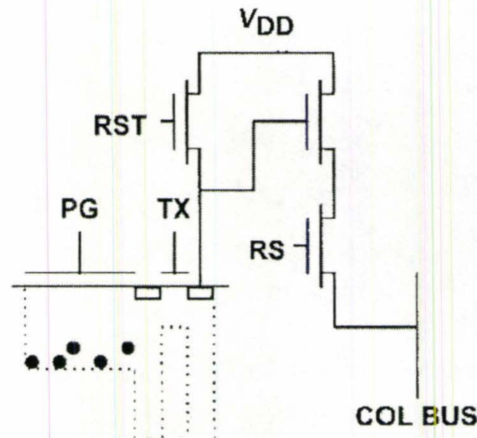


Figure 3-1: A four-transistor APS pixel with photo-gate. Photons have to pass through the poly-silicon gate layer before reaching the silicon surface (Taken from [3.1], Fig. 6).

3.1.2. Logarithmic pixels

Logarithmic pixels are suitable in applications where wide dynamic range is desired. The load transistor produces a voltage that is proportional to the logarithm of the photocurrent [3.1], as shown in Figure 3-2. This is a non-integrating approach, and thus not suitable for low light level applications.

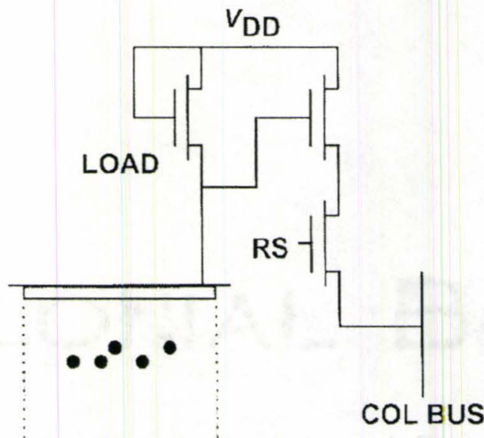


Figure 3-2: Logarithmic pixel. In this pixel the load transistor performs the logarithmic current to voltage conversion (Taken from [3.1], Fig. 9).

A major drawback of logarithmic sensors is their high FPN due to the sensitivity of the output with respect to the device parameters. Thus, CDS is not applicable at the

pixel level. An on-chip calibration approach has been suggested to reduce the FPN [3.4]. The circuit has an extra calibration current column bus. The pixel value is read twice, once with the photocurrent and a second time with the calibration current passing through the logarithmic load. A five-transistor pixel has been realized in a 0.5 μm process. The pixel pitch is $7.5\,\mu\text{m} \times 10\,\mu\text{m}$ in a 512×512 array. The implemented sensor has a dynamic range (DR) of 120 dB, temporal noise of 0.75 % of the total swing, and FPN of 2.5 %.

3.1.3. Current-mediated

The objective of this method is to achieve simple error correction techniques [3.5]. The pixel benefits from small size and simple operation (Figure 3-3). It has three transistors per pixel, and four bus lines that are controlled by two clock signals. The nonlinear photon-to-output signal transfer function however, limits the fixed-pattern noise correction.

The circuit operates as follows. For performing the reset function, RESET, SEL, and Reference enable transistors are turned on to force I_{REF} to pass through the photodiode and generate and store the reference voltage level in the sense node. During integration, photocurrent discharges the sense node similar to APS. A 512×768 imager is fabricated in this work in a 0.7 μm process.

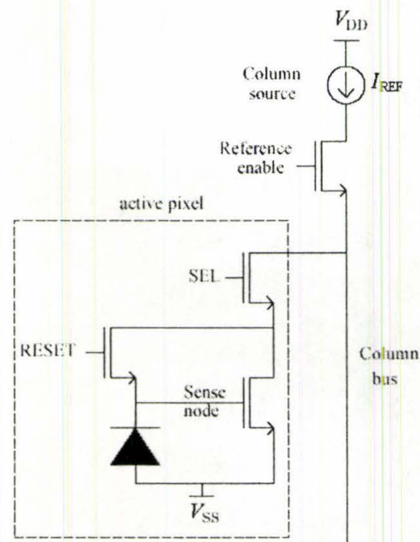


Figure 3-3: Current mediated pixel structure. The pixel has to be selected to perform reset (Taken from [3.5], Fig. 2).

There is another current-mode APS reported in the literature [3.6] that has on-chip FPN cancelation. This approach uses a new readout strategy in which only two current sources are active at any given time, resulting in reduced power consumption. Also, the same addressing signals are used for the electronic shutter, resulting in significant saving of silicon area. A 32 × 32 imager was fabricated in this work using AMIS 0.35 μm CMOS technology.

3.1.4. High DR

There are many reported solutions for increasing the dynamic range (DR) of APS. The logarithmic pixel was one of them. Here is another approach with a pixel circuit that is very similar to APS as shown in Figure 3-4 [3.7].

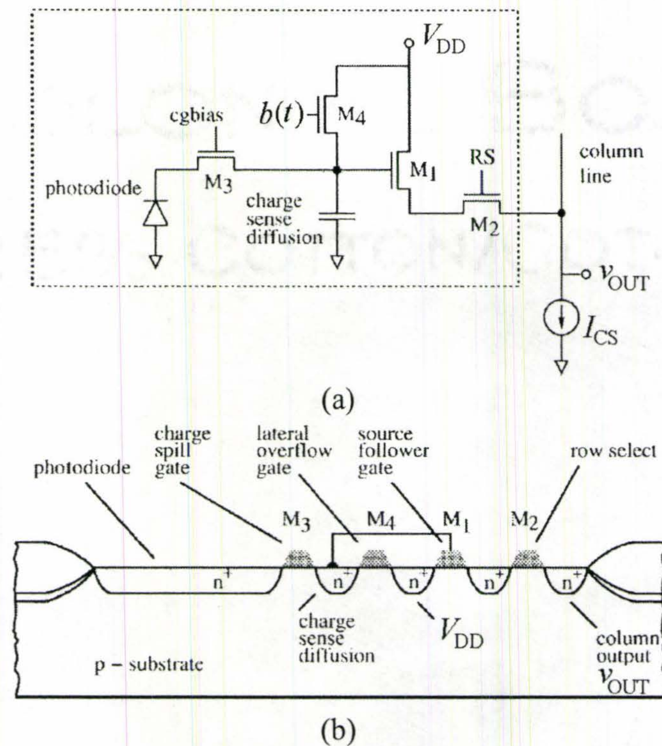


Figure 3-4: (a) High dynamic range pixel schematic and (b) its layout. High dynamic range is achieved by varying $b(t)$ (Taken from [3.7], Figures 1 and 2).

The gate of the spill transistor M_3 is held at a constant potential of approximately 1V. Charge generated over the large n^+ diffusion area is thus sensed using the small capacitance of the sensing node. A high dynamic range is achieved by manipulating $b(t)$. Unlike regular APS, for which $b(t)$ is 0 and jumps to V_{DD} during the reset time, in this pixel structure, $b(t)$ is gradually increased (either smoothly or in steps) to V_{DD}. This allows for much sharper integration slopes of the sense node to be sensed before saturation.

3.1.5. In-pixel ADC

Performing the analog-to-digital conversion inside the pixel can have many advantages. It makes the imager more compatible with digital CMOS, and also more scalable. It eliminates the column and read-out circuit noises. Finally, parallel ADC will provide very high operation speeds [3.8] as the pixel readout is not limited by the bus settling time. Maintaining all analog processing within the pixel can reduce overall system power and allow for easier scaling to larger array sizes.

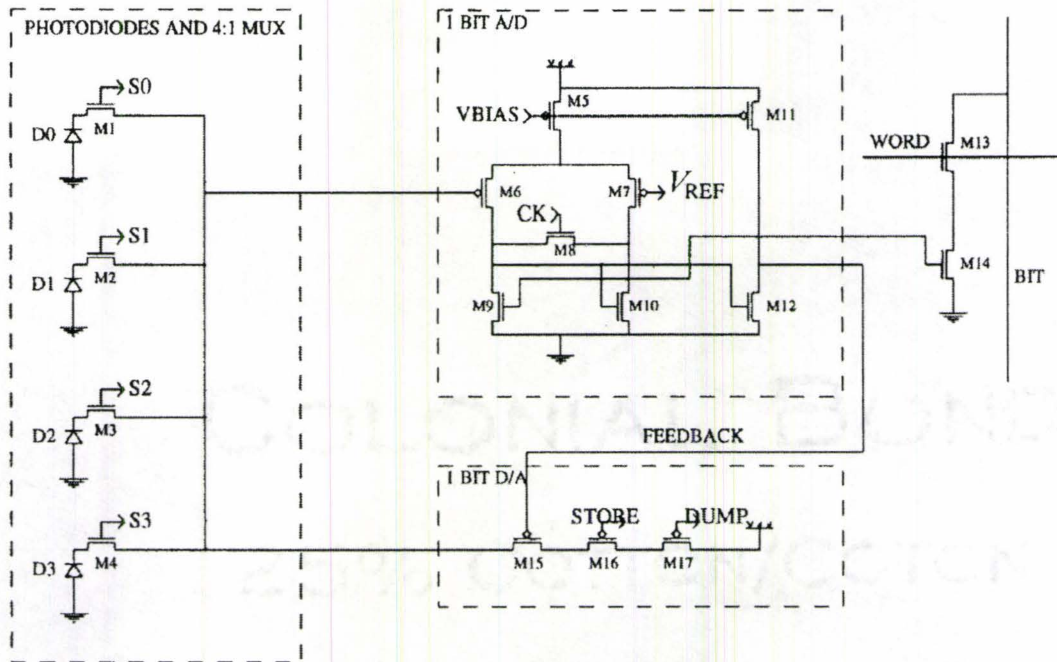


Figure 3-5: Digital pixel sensor structure. Every four pixels share an ADC unit, resulting is approximately 3 transistors per pixel. (Taken from [3.9], Fig. 3).

Figure 3-5 shows the pixel circuit of the digital pixel sensor. The pixel performs sigma-delta ADC. The external circuit provides the pixel with the comparison level, V_{REF}, and reads the digital output bit by bit.

Another work has been reported [3.10] that implements a pixel parallel A/D conversion. This work suggests a free-running continuous oscillator sampled at fixed intervals to be used as a first order $\Sigma\Delta$ converter. The circuit is shown in Figure 3-6 and it is composed of four sections: a differential amplifier which continuously compares the photodiode voltage to V_{LOW}; a bistable half-latch which triggers the reset; a regenerative section that switches the bistable latch and restarts the integration; and pulse capture logic that stores a bit upon reset. The circuit constantly compares the rising photodiode signal with V_{LOW}. It resets the photodiode and generates a "1" output as soon as v_S equalizes with V_{LOW}. The frequency of the output bit represents the signal. The work claims low-power and high DR. The drawback however is the pixel size, reported to be 30 μm × 30 μm for the implementation.

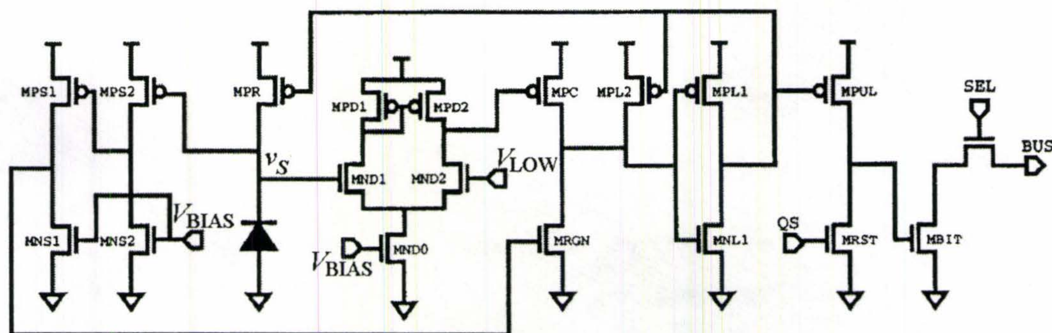


Figure 3-6: Sigma delta converter cell schematic. It contains 19 transistors and connects to 5 bus lines (Taken from [3.10], Fig. 9).

A similar work [3.11] reports a high-speed digital pixel sensor that could achieve 10,000 frames/s. It performs a fully pixel-parallel image acquisition. The pixel consists of a photogate circuit, a comparator, and an 8-bit memory. It uses the same technique as [3.10] for the A/D conversion. However, the pixel size is 9.4 μm × 9.4 μm and it is implemented in 0.18 μm CMOS technology.

In a more recent work [3.12], an 8.3 M-pixel, 60 frames/s digital output CMOS APS has been reported. It is fabricated in 0.25 μm CMOS with a 20 mm × 20 mm die size. The output resolution is 3840 × 2160 with a 4.2 μm pixel size. In this work however, the ADC has been done in the column level, and not in the pixel. The ADC has a 10-bit output. The FPN generated in each pixel and the column analog signal chain is suppressed before the A/D conversion. The dynamic range is 55 dB and the noise floor is 42 e (full well capacity is 25,000 e).

3.1.6. Pseudo-active pixel senor

The so-called pseudo-active pixel sensor (PAPS) pixel structure is shown in Figure 3-7(b) [3.13], [3.14]. This structure offers low dark current and high fill-factor. The integration capacitor and source follower of the conventional APS are moved out of the pixel. The op-amp shown in Figure 3-7(a) fixes the photodiode anode voltage, v_{PIX}, that helps to reduce dark current.

Figure 3-7: (a) Pseudo-active pixel sensor circuit and (b) the pixel. Pixel is similar to passive as it connects to the bus via a single transistor (Taken from [3.13], Fig. 1 and 4).

This approach claims to reduce the dark current by isolating the photon-sensing area from the defective field oxide. An n^+ ring reset structure is proposed. A fill factor as high as 45 % has been achieved. The pixel has been implemented using standard 0.35 μm CMOS with a pixel size of 7.5 μm × 7.5 μm. Figure 3-8 shows the pixel structure of an ordinary APS pixel compared to the proposed pixel [3.15].

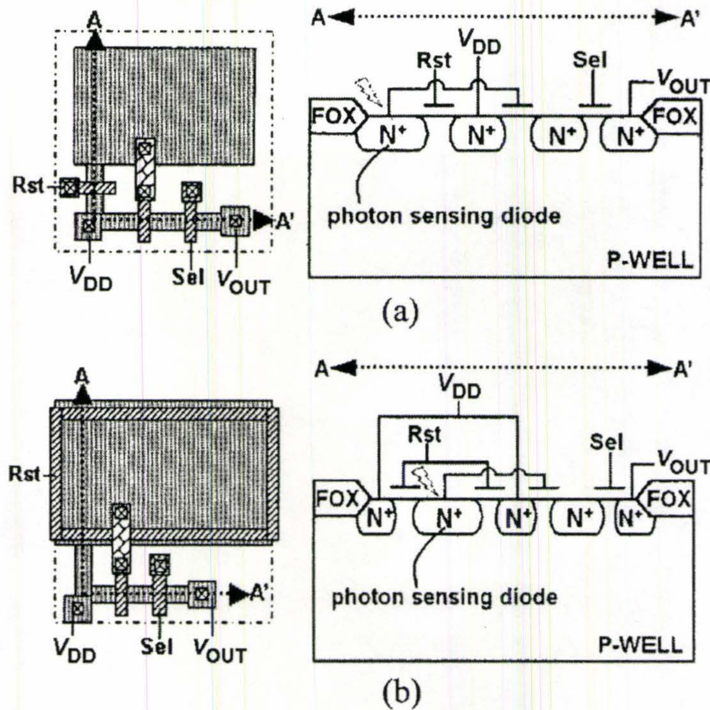


Figure 3-8: Ring reset pixel structure (Taken from [3.15], Fig. 1).

3.1.7. Combined structure

It has been suggested [3.16] that using a combined photogate and photodiode ring structure in an APS pixel can reduce the dark current. In a single integration period, the pixel performs the integration twice. Once with the PG voltage high, letting the photo-gate integrate, and once with photo-gate off. Then using the differential column structure shown in Figure 3-9, the difference is regarded as the signal value.

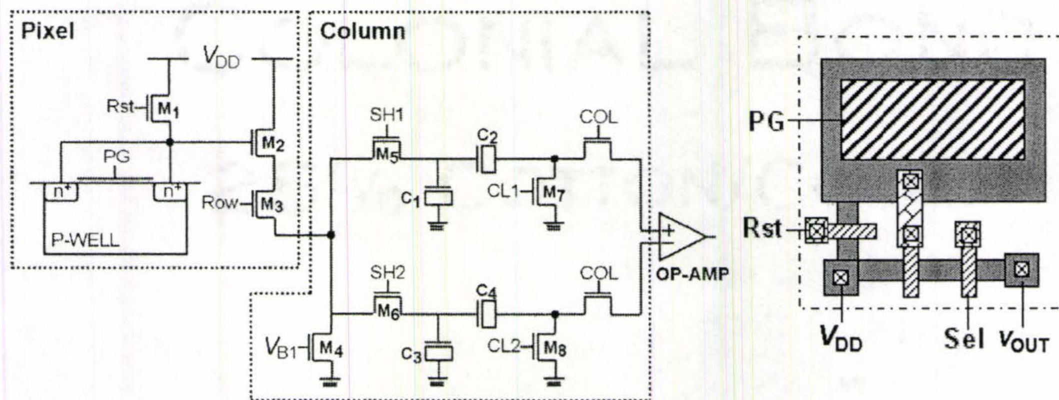


Figure 3-9: Combined photo-gate and photodiode structure. The pixel schematic and the correlated double sampling circuit are shown at left. The layout of the pixel is shown at right (Taken from [3.16], Fig. 1).

The dark current in the CMOS APS cell mainly results from the leakage current in the surface depletion region [3.16]. As the surface depletion region is not affected by the PG, it is claimed that the total sensed dark current in the two periods are the same (considering equal integration times). The subtraction will then eliminate the dark current induced voltage. The circuit has been implemented in 0.35 μm CMOS. Reported dark current is 0.93 nA/cm^2.

3.1.8. Conventional APS

There has also been several conventional APS structures reported in the literature. Here we will compare several parameters of the reported APS. Table 3-1 compares three photogate APS structures and Table 3-2 compares 7 different photodiode APS structures.

Table 3-1: Different photogate APS structures

Reference	Tech. μm	Pix. size μm	Array size	FF %	Read noise	Dark Cur. pA/cm^2	FPN mV	DR dB
Nixon [3.3]	1.2	–	256×256	–	138 μV	500	–	–
Yonemoto [3.17]	0.35	7.4	640×640	24: 47	–	370	8 : 24	–
Sunetra [3.2]	2	40	128×128	26	28 e	1000	3	76

Table 3-2: Different photodiode APS structures

Reference	Tech. μm	Pixel size μm	Array size	FF %	Read noise	Dark Cur. pA/cm^2	FPN mV	DR dB
Cheng [3.15]	3.5	7.5	3×3	42.6	–	–	–	–
Shih [3.13]	0.25	5.8	352×288	58	–	93	5.3	–
McIlrath [3.5]	0.7	15	512×768	–	–	–	–	–
Ricquier [3.18]	0.5	6.6	512×512	15	–	–	5	50
Zhou [3.19]	1.2	24	128×128	29	303	600	6	72
Casadeu [3.20]	0.6	12.8	64×64	28	106e	–	2 %	64
Mehta [3.21]	0.5	20.3	92×52	10	–	–	1 %	–

3.2. APS pixels with internal comparator and integrator

The number of transistors that could fit into a pixel was limited in past. This was due to the large size of transistors compared to the desired pixel pitch for medium- to high-resolution imagers. However, deep submicron technologies have made it

possible to put more transistors into the same die area. This has made the transition from passive pixel sensors (1 transistor per pixel) to active pixel sensors (3 transistors) and beyond, posbbile. It is now feasible to do parts of the data processing within the pixel and to develop smart pixels. Smart pixel systems are integrated and can perform sophisticated tasks faster than conventional imaging systems. In the following subsections, we analyze two APS pixels with in-pixel circuitry that are the core of many smart pixels. We have designed and fabricated a three transistor APS, an APS pixel with internal comparator, and an APS pixel with internal integrator in standard 0.18 μm CMOS technology with the layouts shown in Figure 3-10. In the following, we compare the performance of these APS circuits, and their suitability for different types of applications [3.22].

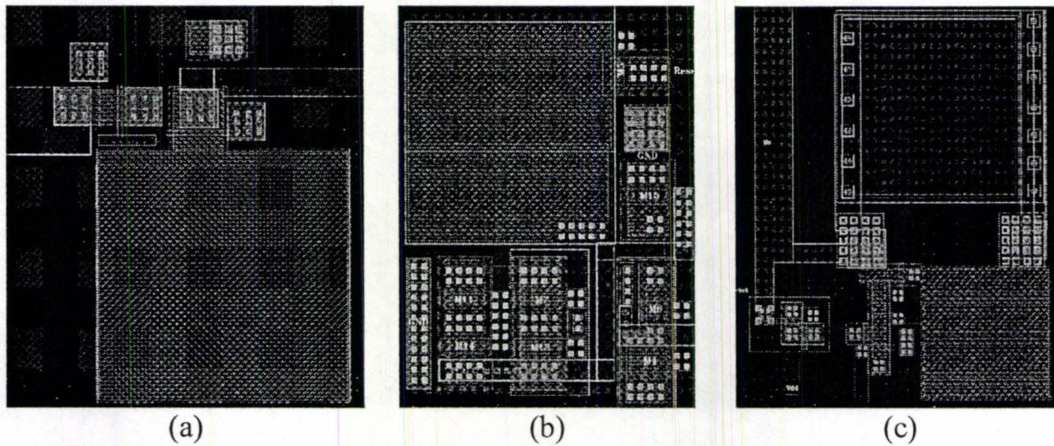


Figure 3-10: Layouts of different APS structures. (a) Three transistor APS has the simplest layout and highest fill-factor. (b) The APS with comparator has 8 transistors. However, our compact design has kept the fill-factor at a high level. (c) The APS with integrator. This design considers a capacitor in each pixel that reduces the fill-factor of the pixel. However, the fill-factor is still at a reasonable level.

3.2.1. APS with comparator

The general structure of our APS pixel with an internal comparator is shown in Figure 3-11(a), with the detailed schematic of the circuit shown in Figure 3-12. The pixel consists of 8 transistors including the reset transistor, with the layout shown in Figure 3-10(b). The pixel has a reference level input and its output has a digital "High" or "Low" value, depending of the value of the reverse voltage across the photodiode relative to the value of reference voltage of the comparator, V_{REF}. The photodiode and

reset transistor combination of the pixel works in the same manner as the conventional APS. The sense node voltage is compared to the reference level, and the result of the comparison is the output of the pixel. Figure 3-11(b) shows different signals from the pixel and how they correspond to each other. Waveforms 1 and 2 in Figure 3-11(b) are the measured reset signal and output of the pixel. Waveform 3 is an illustration of the internal sense node voltage, and waveform 4 is the reference level. After reset, the sense node voltage is above the reference level and the output is low. The sense node voltage will decrease during integration, and if the light level is high enough, it will cross the reference level. Therefore, the duration of the output pulse at low will be inversely proportional to the light level and this is the output signal of the pixel. Compared to the conventional APS where the output is the voltage swing, for APS with the comparator, the output is the duration of the low-level pulse shown in Figure 3-11(b).

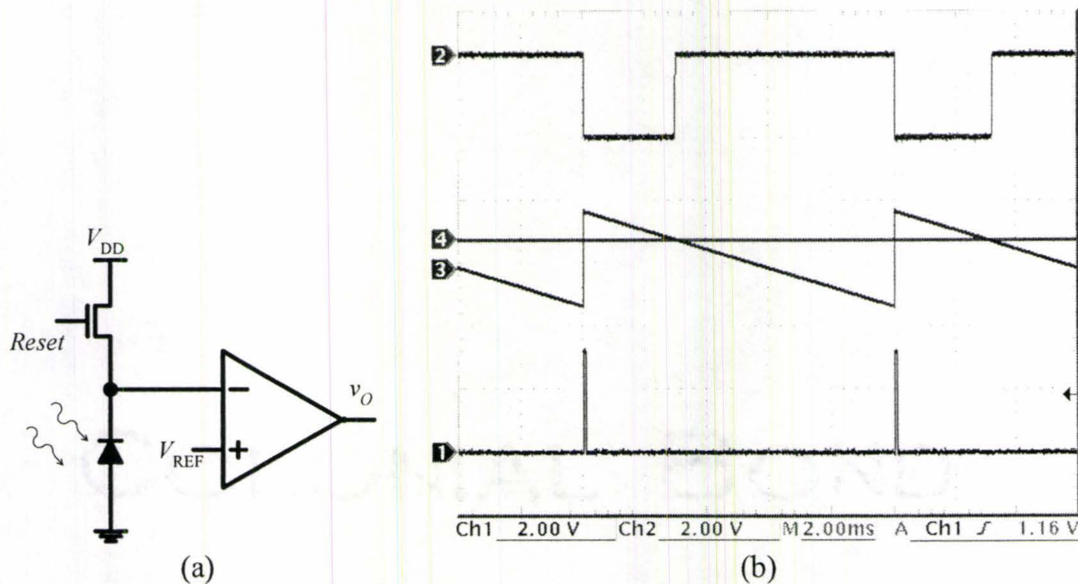


Figure 3-11: APS with comparator. (a) General schematic and (b) Measured and illustrated waveforms. Channel 1 is the applied reset signal and channel 2 is the measured output, v_O, of the pixel. Channel 3 and 4 show how the sense node voltage and reference level stand with respect to each other to generate the output.

The time at which the output of the pixel goes from "High" to "Low" is fixed by the externally applied reset. The time at which the pulse comes back to "High" however, is affected by the noise that is present in the sense node voltage. The noise sources

that contribute to the total noise of the sense node voltage are the same as the three-transistor APS described above in Section 2.4. In this APS with a comparator, an easy way to quantify the noise in from of the jitter in the rising edge of the output pulse of the comparator. Figure 3-13(a) shows the jitter of the output, captured on the storage oscilloscope screen. Figure 3-13(b) shows the root-mean-square (RMS) value of the jitter of the output, compared to the output pulse width. Figure 3-13(b) shows that the signal-to-noise ratio of the output is not the limiting factor in detection of the low-light-levels using this structure. However, sensing lower light levels requires higher integration times to let the sense node voltage drop enough to cross the reference level. This is similar to the three transistor APS, with the difference being that now the reference level can also be adjusted to optimize the detection of the light intensity range of interest.

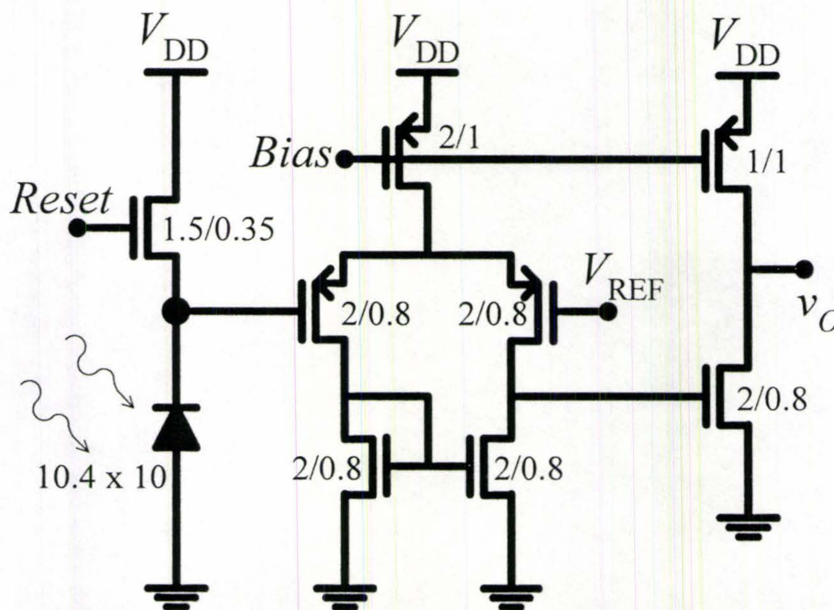


Figure 3-12: Full circuit of Figure 3-11(a) with the dimensions of the photodiode and transistors.

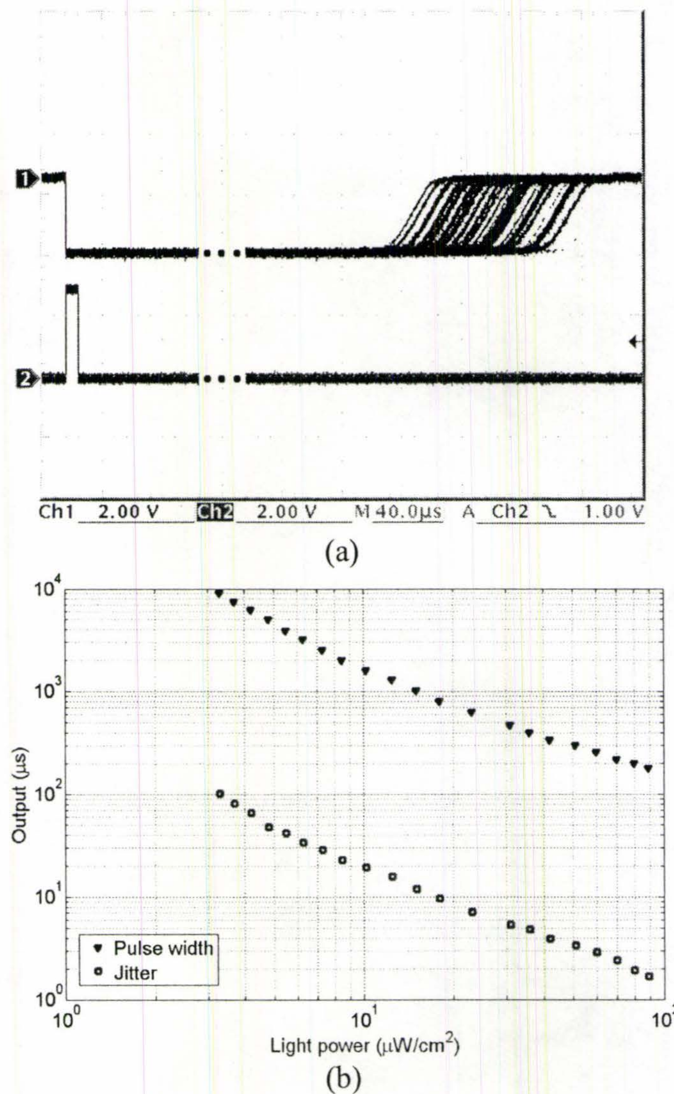


Figure 3-13: (a) Measured output of the APS with comparator, zoomed in to show the jitter in its output. This jitter is the noise of the output as the pulse width is the output of the pixel. (b) Measured signal (pulse width) and noise (jitter) of the output of the pixel, as a function of light powers.

The main advantage of this structure is the immediate analog-to-digital conversion of the signal, inside the pixel, thus eliminating the readout noise of the consequent stages of the imager. It will also provide a parallel and fast A/D conversion of the signal, making it possible to achieve faster scanning times.

3.2.2. APS with integrator

In most of the APS structures, including the two that are described above, the photocurrent is integrated by the junction capacitance of the photodiode. A diode

however, is not a perfect capacitor, as the junction capacitance changes with the applied bias. As a result, output of the APS becomes nonlinear and this has an impact on both the signal and the SNR characteristics. It should be mentioned that the sense node voltage capacitance of an APS has a parallel component equal to the gate-source capacitance of the buffer transistor (M_2 in Figure 2-2(a)). One can reduce the effect of nonlinear capacitance of the photodiode, by making the gate-source capacitance of M_2 high, such that it dominates the sense node capacitance. This solution will keep the capacitance at the sense node voltage relatively constant. However, it will result in an increase in the size of the buffer transistor, thus reducing the fill-factor of the pixel. It will also reduce the charge-to-voltage conversion gain of the pixel, thus degrading its sensitivity. An integrator, using an operational amplifier, can solve this problem by keeping the sense node voltage constant and integrating the current in its fixed capacitor. We have designed a pixel with a current integrator that integrates the photocurrent into an on-chip metal-oxide-metal capacitor. The schematic of the APS with integrator is shown in Figure 3-14(a), with its layout shown in Figure 3-10(c) and the detailed schematic shown in Figure 3-15.

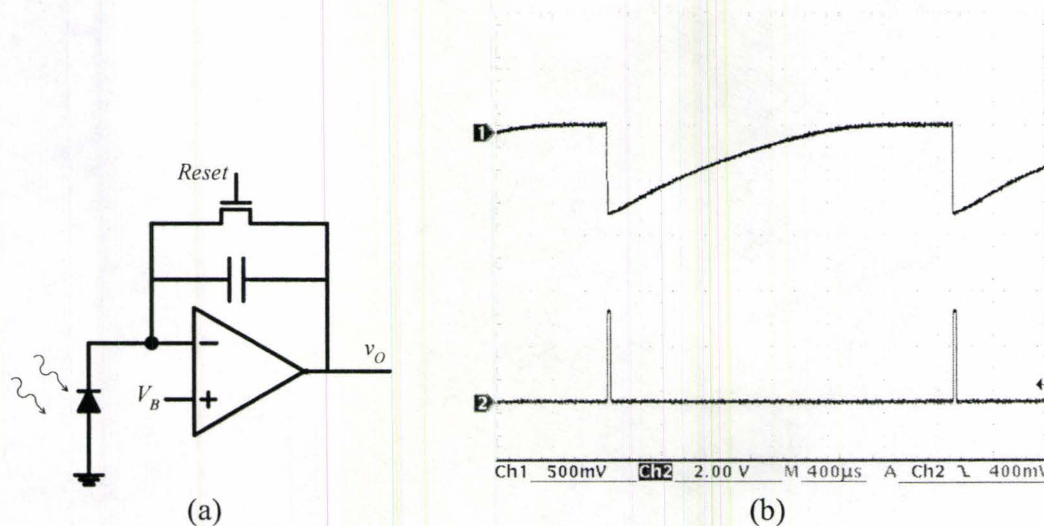


Figure 3-14: APS with integrator. (a) General schematic of the pixel and (b) its measured waveforms. Channel 1 shows the measured output of the pixel, while channel 2 shows the reset signal applied to the pixel, for a 2.5 ms readout time.

The measured output of the APS with integrator is shown in Figure 3-14(b). After the reset period, the capacitance of the integrator is discharged. During integration, the

operational amplifier of the integrator keeps the bias over the photodiode fixed. This causes the photocurrent generated in the photodiode to be integrated in the capacitor rather than the photodiode. The output of the integrator will then increase in proportion to the generated photocurrent during the integration time.

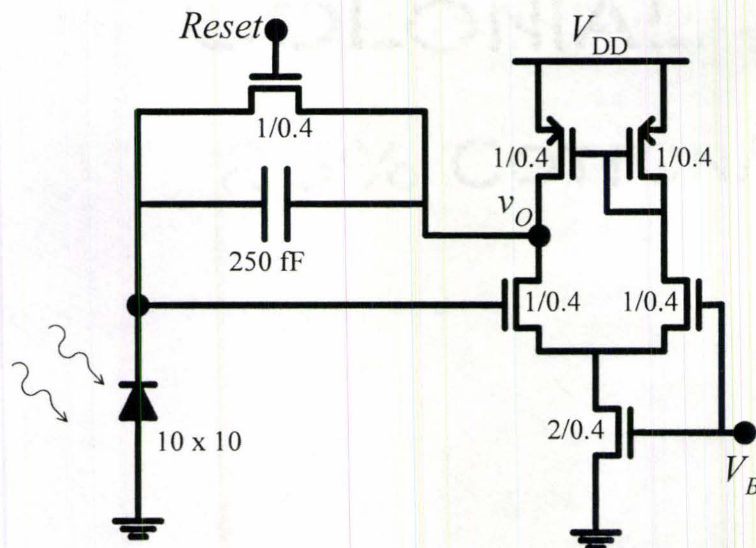


Figure 3-15: Full circuit of Figure 3-14(a) with the dimensions of the photodiode and transistors. Junction capacitance of the photodiode is approximately 300 fF.

Figure 3-16 shows how the output of the APS with integrator varies with the incident light power. The measurements are done for light at different wavelengths and they show good linearity of the output with respect to the power of incident light, unless the pixel is saturated.

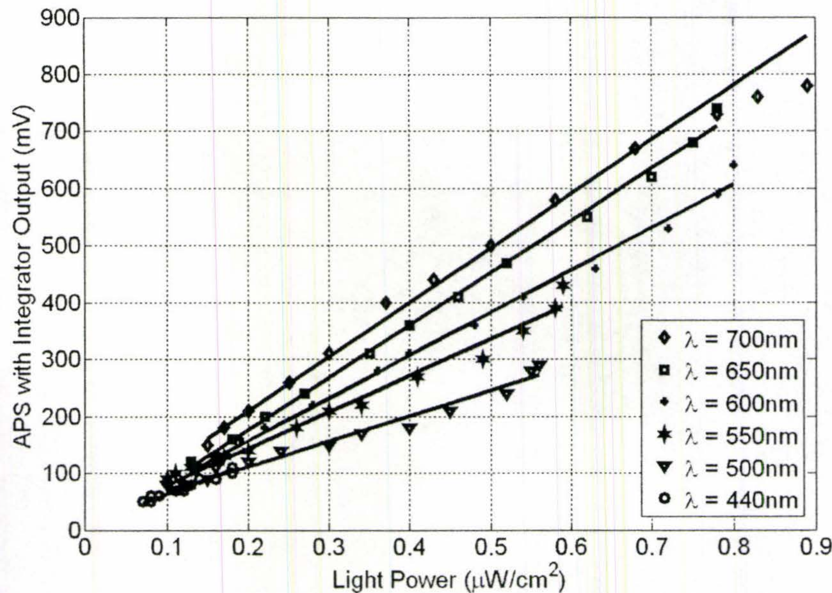


Figure 3-16: Output of the APS with integrator, sampled at different levels of incident light power. Measurements are done at different wavelengths. It can be observed that a good linearity exists in the output, unless the output saturates, as shown in the curve for the 700 nm light.

Analysis of the shot noise during integration, for the APS with integrator, is similar to the three transistor APS with the only difference being in the value of the capacitance. However, the effect of 1/f noise will be more important now, as different elements of the integrator also contribute to the 1/f noise. It is important to remember that frequency domain analysis is not applicable for the analysis of 1/f noise in this circuit, as APS is a switched circuit, and the 1/f noise will appear as a cyclo-stationary process in its output [3.23].

One advantage of the proposed APS with integrator design is that the size of the photodiode and the capacitance of the integrator can be chosen independently. Thus the capacity of the pixel can be adjusted while keeping the photosensitive area of the pixel fixed. The main advantage of this structure, however, is its performance in dark. The amplifier of the structure keeps the bias applied to the photodiode fixed. The bias level is controlled by the input V_B which is very close to zero. At these small bias voltages, the dark current generated in the photodiode is small compared to the dark current of the conventional APS generated at a bias close to V_{DD} [3.14]. As a result,

the output voltage read from the pixel at dark will be small, compared to the three transistor APS.

3.2.3. Comparison

Three different APS structures are introduced in this work. Each of the structures has characteristics that make it suitable for certain types of applications. Table 3-3 compares these structures and some of their key performance measures. The three transistor APS has the simplest structure and highest fill-factor. It is suitable for applications that require ultra-high resolution imaging. It has also the least noisy output, because it has the least number of transistors in its data path to the output.

Table 3-3: Comparison of the APS structures

	APS	APS with comparator	APS with integrator
Photodiode size	20 μm × 20 μm	10 μm × 10 μm	10 μm × 10 μm
Transistor/pixel	3	8	6
Fill-factor	63 %	36 %	15 %
Output swing	1 V	2.2 V	0.8 V
Dark output	50 mV/s	210 mV/s	16 mV/s

The APS with the comparator structure has an acceptable fill-factor of 36 % due to our compact design, and this is shown in Figure 3-10(b). It has a digital output, which makes it applicable to ultra-fast digital imagers. It is possible to adjust the reference level and the integration time, thus achieving good sensitivity at the desired light levels. It also has the widest dynamic range, as the sense node voltage is read and converted to a digital level immediately, and the overhead voltage drops of the amplifier and buffer stages do not affect the output.

The APS with integrator structure has a low fill-factor. It has a low dynamic range, is slow, thus it is not suitable for applications that require high scanning rates. However, its output is the most linear with respect to incident light power, and it has an internal dark current cancellation mechanism. These two features make this APS structure a good candidate for low-level light imaging using longer integration times.

3.3. Multisampling, time-domain APS

Imaging techniques that are used for detection of low levels of light do not generally have high dynamic range. Time-domain APS is a different class of CMOS imagers that may be considered if a combination of moderate speed, sensitivity and dynamic range is required. In this section, we introduce an alternative architecture for time-domain CMOS imagers with multisampling and synchronous readout circuit [3.24]. There have been time-domain sampling techniques reported for CMOS imaging [3.25], which similarly to our method, perform a comparison to a reference level within the pixel. Our method however uses a clocked comparator as well as a pixel-level flip-flop, which can result in time and power savings.

The method presented in this work performs in-pixel A/D conversion allowing more than 8-bit data resolution without reducing the fill-factor of the pixels. The proposed architecture employs a clocked comparator in each pixel that performs a fast and synchronized comparison between the sense-node voltage and the reference voltage in parallel for the whole array. Then, a clocked D flip-flop, which is also designed inside the pixel, captures and stores the state of each pixel. In the array structure, the D flip-flops of the pixels in each row are connected in series to create a shift-register. The shift registers provide synchronous readout of the pixels. We characterize the limits of the architecture as a function of the frame rate, array size and illumination level.

3.3.1. Architecture and frame-rate analysis

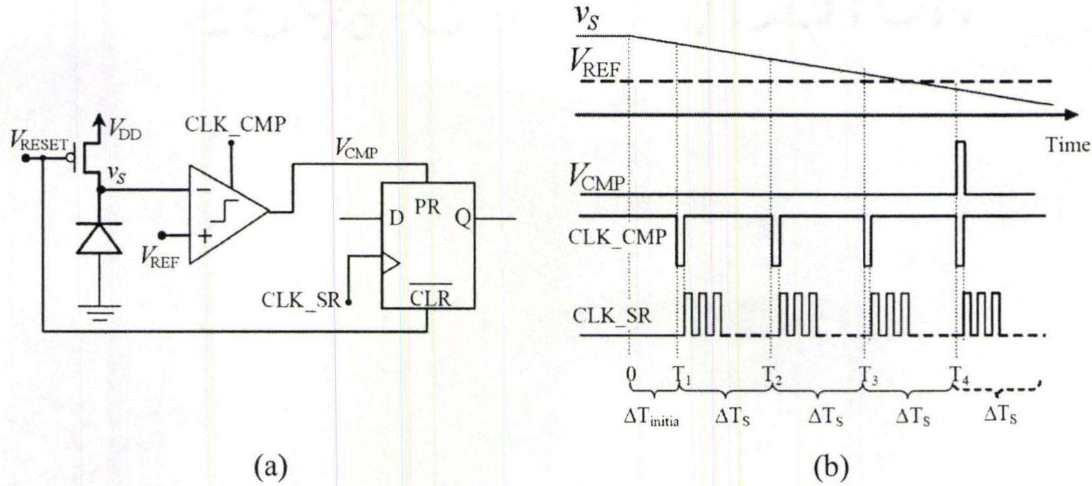


Figure 3-17: (a) Multisampling pixel architecture. Each pixel consists of an n^+/p-sub photodiode, a PMOS reset transistor, a clocked comparator and a D flip-flop. The PMOS reset transistor has W/L = 0.4/0.4, and the photodiode size is 5 μm × 20 μm. (b) Time diagram of the circuit signals. Output of the comparator, V_{CMP}, becomes high with the first clock after the sense node voltage drops below V_{REF}.

Figure 3-17 shows the pixel architecture and the time diagram of the pixel operation. The pixel is composed of an n^+/p-well photodiode, a reset PMOS transistor, a clocked comparator and an edge-triggered D flip-flop with asynchronous inputs. First, the reset transistor is turned on to charge the photodiode capacitance to about $v_S = V_{DD}$. Also, during the pixel reset, the D flip-flop is cleared to Q = 0. The integration time starts by V_{RESET} going low. During the integration time, the photocurrent discharges the photodiode capacitance and v_S decreases with time as shown in Figure 3-17(b). The capacitance of the photodiode, C_{PH}, varies with the applied bias [3.26]. However, the variation is small and the photodiode capacitance C_{PH} can be assumed constant. For a given i_{PH}, the v_S varies linearly with time following:

$$v_S(t) = V_{DD} - \frac{i_{PH}}{C_{PH}} t . \tag{3-1}$$

To provide synchronous sampling of pixels for the whole array, the comparators are activated by a global low-active clock signal, CLK_CMP. When CLK_CMP = 0, v_S is compared to V_{REF}, and the comparator output switches to $V_{CMP} = 1$ once the

photodiode voltage drops below V_{REF}, as shown in Figure 3-17(b). Consequently, the output of the D flip-flop is set to Q = 1, as the comparator output is connected to the asynchronous preset (PR) input of the D flip-flop. After reset, as stated above, and before the preset happens, the output of the D flip-flop is Q = 0. In this way, the flip-flop output equals to the result of the sampled comparison between v_S and V_{REF}. Note that the asynchronous input PR can occur only when the global signal CLK_CMP is also active. Between CLK_CMP pulses, the flip-flop can be used as a cell in a shift register, clocked by the CLK_SR signal which has a much higher frequency. In this manner the sampled pixel outputs are shifted out of the array before the next round of sampling. A 32 × 32 pixel array was implemented in 0.35 μm CMOS technology in this work. The pixel is 30 μm × 26 μm with a fill-factor of 16 %. The complete array structure is shown in Figure 3-18.

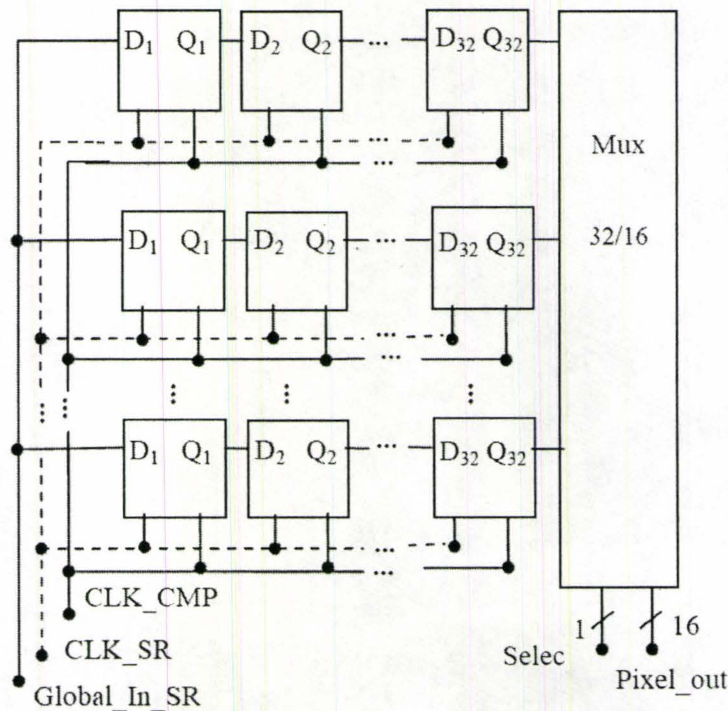
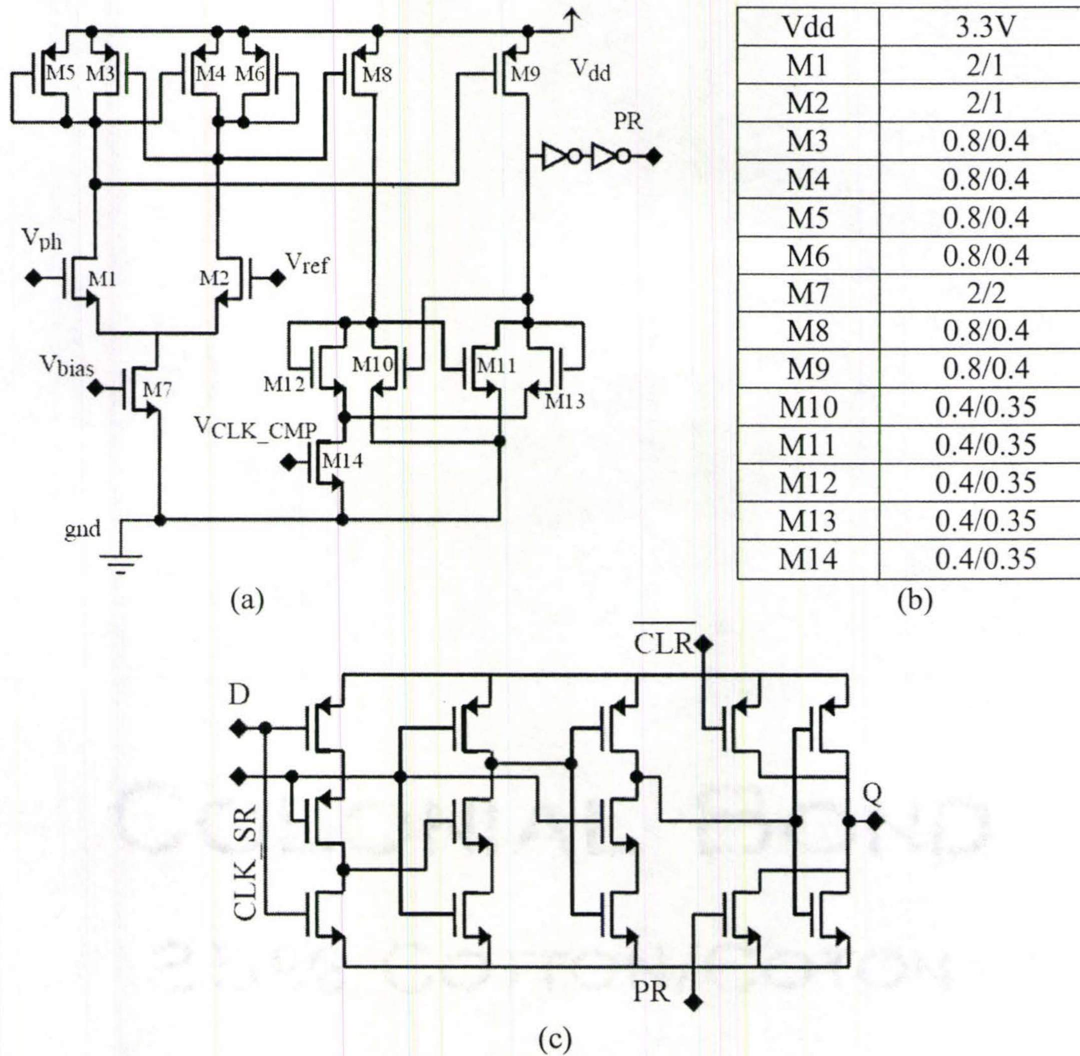


Figure 3-18: Architecture of the multisampling, time-domain APS array.

The schematic of the integrated comparator and the D flip-flop circuits are shown in Figure 3-19. Figure 3-19(a) shows the clocked comparator circuit that has two stages: a pre-amplifier stage and a "track-and-latch" stage [3.27]. The D flip-flop circuit is a dynamic single-clock D flip-flop with an inverter connected to the output and two

transistors to perform the asynchronous preset and clear, with its schematic shown in Figure 3-19(b). Compared to previously reported circuits [3.28], the dynamic single-clock flip-flop provides fast operation, lower number of transistors and requires only a single clock signal.



Vdd	3.3V
M1	2/1
M2	2/1
M3	0.8/0.4
M4	0.8/0.4
M5	0.8/0.4
M6	0.8/0.4
M7	2/2
M8	0.8/0.4
M9	0.8/0.4
M10	0.4/0.35
M11	0.4/0.35
M12	0.4/0.35
M13	0.4/0.35
M14	0.4/0.35

Figure 3-19: Schematic of the integrated (a) clocked comparator and (b) details of the circuit. (c) D flip-flop, with PMOS W/L = 0.4/0.4 and NMOS W/L = 0.4/0.35.

The total pixel integration time, t_{int}, is divided into sampling periods of length ΔT_S, resulting in 2^N possible values for output illumination level, where N is give by

$$N = \log_2(t_{\text{int}} / \Delta T_S)\,. \tag{3-2}$$

The maximum frame rate can be obtained from (3-2) for a given ΔT_S, to be $(1/\Delta T_S)2^{-N}$. The frame rate relates exponentially to the number of bits. For $\Delta T_S = 10^{-4}$ for example, it is about 10 frames/s for 10 bits, and 40 frames/s for 8 bits of data resolution.

The circuit has to be fast enough to shift out the information from the D flip-flops of the whole array within the sampling time ΔT_S. The maximum operation frequency of the multiplexer is lower than the maximum operation frequency of the shift-register. Thus, the sampling time of the whole array, T_S, is mainly limited by the multiplexer delay, T_{MUX}, and is given by

$$T_S = T_{\text{CLK_CMP}} + \left(\frac{C \cdot L}{M}\right) \cdot T_{\text{MUX}}, \tag{3-3}$$

where T_S is the time required to read out 1 bit/pixel from the whole array, $T_{\text{CLK_CMP}}$ is the time required for the clocked comparator to operate, $C{\cdot}L$ is the total number of the pixels in the array and M is the number of output bits of the multiplexer (16 in the case of Figure 3-18).

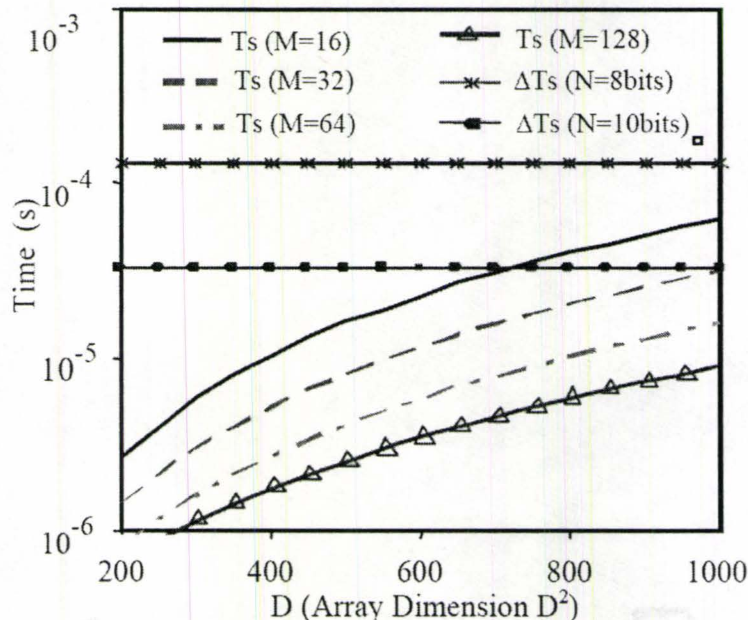


Figure 3-20: Minimum sampling time for different array sizes.

The sampling period of the pixels, ΔT_S, must be greater than the minimum sampling delay of the array, T_S, that is calculated above, which limits the number of bits per pixel for a given frame rate. Assuming t_{int} corresponds to 30 frames/s, $T_{CLK_CMP} = 200$ ns and $T_{MUX} = 5$ ns, Figure 3-20 shows the minimum sample time (T_S) for square arrays of different sizes ($C \cdot L = D^2$) and readout multiplexer with several number of outputs (M). Also, Figure 3-20 shows the maximum number of bits/pixel that each array can achieve. For example, for the given constants, a 1000×1000 array can accommodate 8 bits/pixel, while it cannot accommodate 10 bits/pixel.

3.3.2. Experimental results

The proposed architecture for CMOS imagers was implemented in analog mixed signal (AMS) 0.35 μm technology. The pixel size is 30 μm × 26 μm and the fill-factor is about 16 %, with 32 transistors per pixel. The number of transistors per pixel is lower than the similar architectures that have more than 50 transistors per pixel [3.29]. An n^+/p-sub photodiode was chosen due to the smaller layout area that it would need. The measurements were performed using an illuminator (Spectra Physics, with 100 W Xenon lamp), optical filters and an integration sphere in a dark room. Figure 3-21(a) shows the measurement result for the characteristic discharge time versus illumination intensity, using a constant voltage of $V_{REF} = 1.5$ V. Unlike conventional CMOS imagers where the pixel output is directly proportional to the light level, in the time-domain approach, the output is inversely proportional to the intensity of the incident light. This inherent non-linearity has to be corrected, using digital processing for example, if a linear output is desired [3.30]. Analysis of the slope in Figure 3-21(a) shows that the pixel sensitivity is about 3.4 V/s-Lux. In dark, the pixel discharge time was very long, about 37 seconds, indicating low dark current of the photodiode.

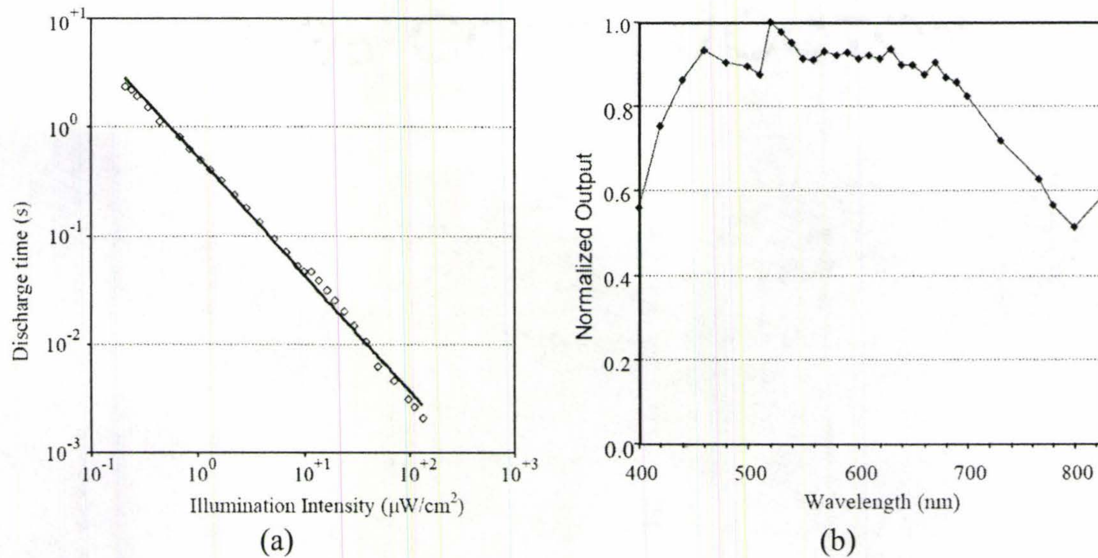


Figure 3-21: (a) Discharge time of a pixel measured at constant reference voltage of 1.5 V and (b) spectral response of the pixel.

Figure 3-21(b) shows the normalized spectral response in the range of 400 nm to 830 nm. The spectral response is higher in the range of wavelengths from 450 nm to 680 nm, and decreases for wavelengths outside this range. This spectral response is typical for the shallow n^+/p-sub photodiodes.

3.4. Lateral BJT

The gate-controlled lateral BJT, GC-LBT, is a hybrid device [3.31] that can operate as a bipolar, a MOS transistor or a combination of both transistors. It is a device that can have controlled photoresopnse or controlled spectral response. In this work, we investigate the CG-LBT operating as a controllable sensor with high sensitivity. The devices are fabricated in standard 0.18 μm CMOS technology. Measurements of the hybrid devices and a careful analysis of the characteristics of the devices are presented. It is shown that the measurement results have good agreement with the theoretical derivations.

3.4.1. Structure

The cross-section of the GC-LBT is shown in Figure 3-22(a). The device has four terminals – Drain (D), Body (B), Source (S) and Gate (G). Figure 3-22(a) shows the lateral BJT in parallel with the MOSFET. It also shows the vertical BJT with the

n-well (V_{DD} terminal), body and source/drain regions corresponding to its collector, base and emitter, respectively. Figure 3-22(b) shows the layout of the device, fabricated in standard 0.18 μm CMOS technology. The six metal paths that connect the device can be seen on the layout, corresponding to the four terminals of the device. The n-well is connected to V_{DD}, and the substrate is grounded.

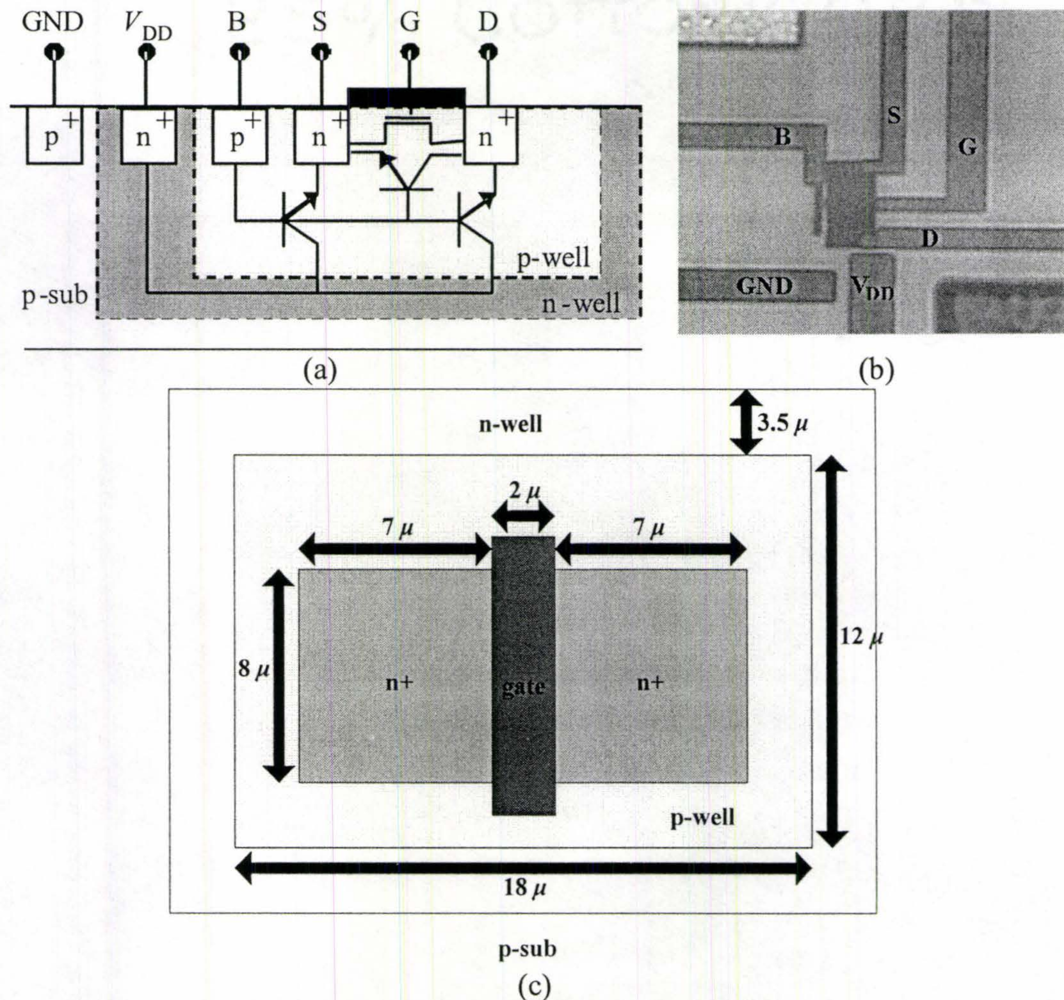


Figure 3-22: (a) Cross-section of the GC-LBT, and its internal lateral and vertical transistors. (b) Photomicrograph of the fabricated GC-LBT. (c) top view of the device with showing the size of the important regions of the device.

In the GC-LBT shown in Figure 3-22(a), photo-generation occurs in the depletion regions of the n-well/p-sub, p-well/n-well, n^+/p-well junctions and in the depletion region below the gate. The photocurrent generated in the n-well/p-sub junction flows

between V_{DD} and ground, and does not contribute to the device output. All the other photocurrents are injected into the body.

The photo-generation is proportional to the depth and volume of the depletion regions. Considering that the n^+/p-well junctions of the drain and source and the channel depletion region, they are shallow and small in area, compared to the p-well/n-well junction. We expect the photocurrent generated in p-well/n-well depletion region to be the dominant component.

3.4.2. Principle of operation of GC-LBT as photodetector

The GC-LBT device can operate in several different modes. Figure 3-23 explains how the CG-LBT works as an image sensor in body floating and V_{GB} constant operation mode. This is the mode of operation that is most suitable for low-light-level applications. Figure 3-23 shows the steps in which the photoresopnse of the device is obtained.

Figure 3-23(d) shows the linear relationship between the generated photocurrent (I_{BPH}) and illuminated light power (P_{OP}). It shows how much photocurrent is generated in the body of the device as a result of photogeneration. Figure 3-23(c) shows the I_{BS}-V_{BS} curve of body-source junction measured in the dark. It shows how the induced I_{BS} current in the device would change the floating body voltage. It is a reverse-biased diode I-V curve. Figure 3-23(b) shows the I_D-V_{BS} characteristics of the transistor, for several biasing V_{GB} voltages. Curves in Figure 3-23(d), (c) and (b) can be combined to analytically obtain the photoresponse of the device, which is the I_D-P_{OP} characteristic. The analytic derivations are also tested against some measurement points that are shown in Figure 3-23(a).

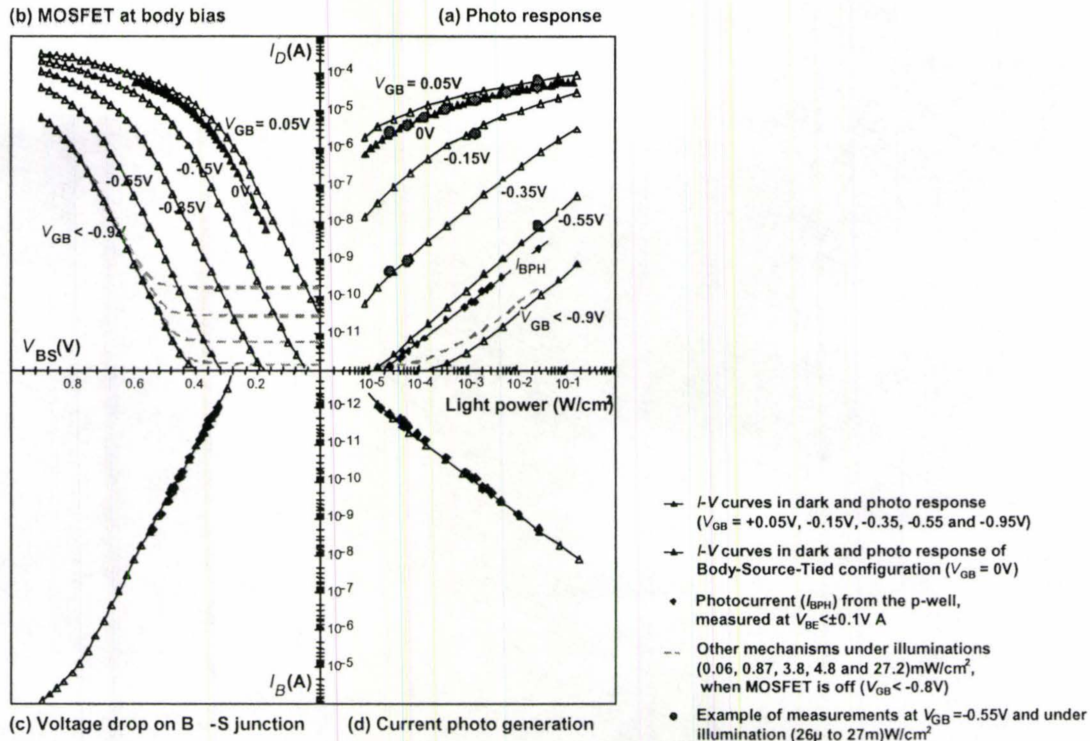


Figure 3-23: Body floating and V_{GB} constant operation mode. (d) Body current generated vs. incident light power, (c) body voltage vs. body current characteristics and (b) the MOSFET drain current vs. the body voltage. The (a) photoresponse characteristics of the device is derived from the (d), (c) and (b) curves.

At body floating and constant V_{GB} operation mode, the GC-LBT shows very high responsivity and wide dynamic range for the output current. The range of the output current can be controlled using V_{GB}. This tunable photoresponse characteristic of GC-LBT can be used to adjust it to different applications. By adjusting V_{GB}, the internal gain of the device can be used to bring the output current to higher levels. However, Figure 3-23(a) also shows that for gain values of more than 10^3, the range of the output current is reduced due to the saturation of the device.

3.5. APS array

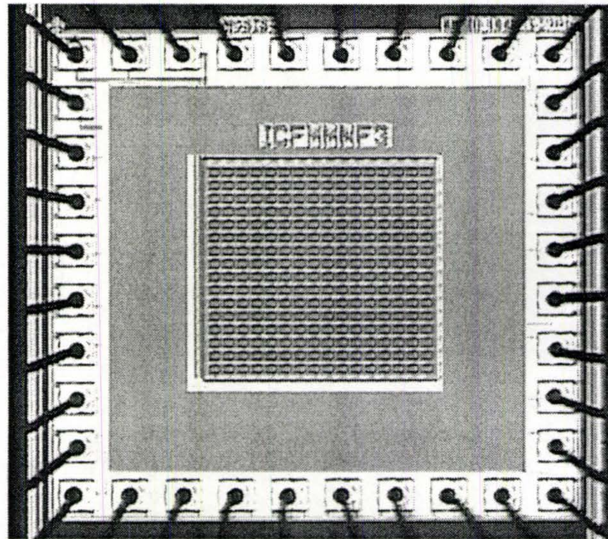


Figure 3-24: Photomicrograph of the array structure fabricated in 0.18 μm CMOS technology.

We have also designed and fabricated a 16 × 16 array of three-transistor active pixel sensors, with a pixel size of 40 μm × 40 μm and a 45 percent fill-factor. Figure 3-24 shows a photomicrograph of the APS array. Although the array can be operated in the conventional APS mode, it is primarily designed to test the application of DC level mode of operation of APS that will be introduced in detail in Chapter 4. The array has global V_{DD} and reset signals. However, each row select and each column output bus is connected to an individual pad. Implementation of on-chip decoders for selecting the rows, and on-chip A/D and shift registers for reading the outputs could reduce the number of pads needed for the chip. We have measured a FPN of about 1% for the conventional APS mode of operation and a FPN of about 2% for the DC level mode of operation of APS. This was expected, as will be described in the next section, due to the fact that DC level mode of operation does not perform CDS, and is greatly dependent on the reset transistor.

Chapter 4

DC LEVEL MODE APS

Active pixel sensors, in general, have an output with low signal-to-noise ratio for low levels of light [4.1]. In many applications, the level of light that should be detected is very low, in the order of microwatts per square centimeter and less [4.2]. It is desired to improve the sensitivity of APS for lower levels of light. One way to increase the sensitivity of APS is to increase its photodiode size. This solution however, will decrease the resolution of the imager, and will not be suitable for applications that require high spatial resolution [4.3]. Another solution is to lengthen the integration time of the APS. The pixel is capable of detecting lower levels of light with longer integration times. However, the rate of temporal variation of the sample can limit the applicability of this solution [4.4]. Also, at long integration times, the internal dark current of the pixel may saturate it. In this chapter we will introduce a new mode of operation for APS that can detect lower levels of light compared to conventional APS, while being able to maintain its high spatial resolution.

Figure 4-1 shows the simulated sense node voltage of the APS circuit with the schematic shown in Figure 2-2(a). Figure 4-1 shows several reset and integration cycles of the sense node voltage, simulated for three different levels of photocurrent. The voltage drop during integration, which is shown in Figure 4-1 as the swing output, is proportional to the power of incident light. This is expected, as for higher levels of light, the photocurrent is higher and discharge of the capacitance of the photodiode happens faster. Interestingly, Figure 4-1 also shows that the DC level of

the sense node voltage varies with light. We will show later, that this variation is mainly due to the incomplete reset of the photodiode, during the short reset time. Figure 4-1 also suggests that the DC level can have much more significant variation than the swing for similar levels of incident light. Our analysis and measurements that will be presented in this chapter approve this fact, and show that DC level can in fact detect two orders of magnitude lower levels of light than swing, for the same pixel structure [4.5], [4.6].

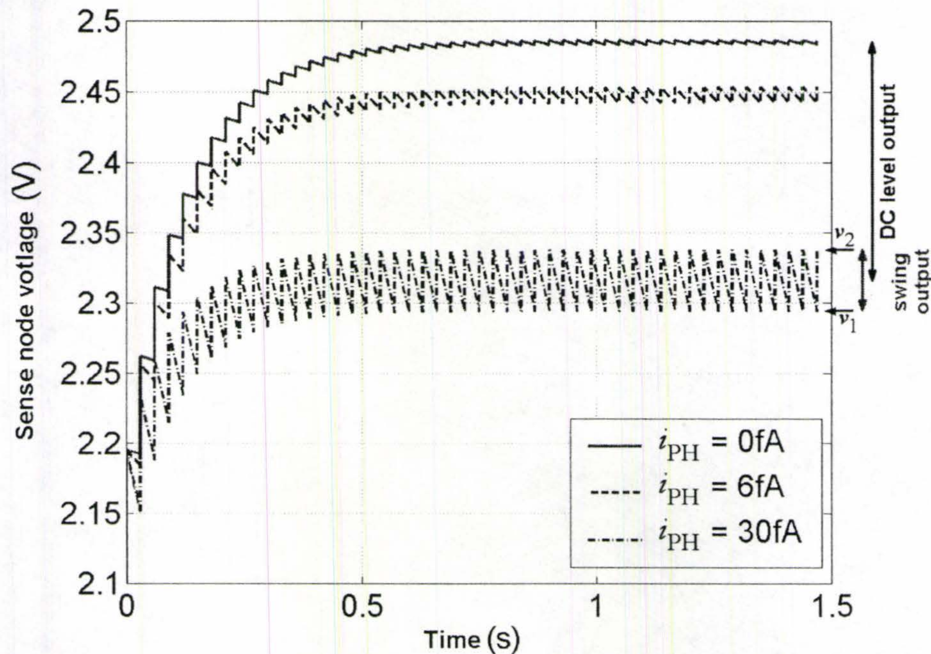


Figure 4-1: Total sense-node voltage versus time for different levels of photocurrent corresponding to different low-light-level illumination conditions. At the absence of photocurrent, the swing output is due to the internal dark current of the photodiode. The DC level varies more than the swing, for the same level of incident light.

There is an interesting story behind how DC level output first came to my attention. I had just received my first APS chip, and I had it set up in the dark room for photoresponse measurement. The photodetector was installed in the dark room in front of the light source. The lights where off in the room and I was observing the APS output on the osciloscope in dark. I was about to turn the Xenon light source on, that my supervisor opened the door and came in to discuss the progress of research. At the moment that he opened the door, I observed a significant drop of the DC line

of the APS output, which was due to the small amount of light that came into the dark room when the door was opened.

4.1. Analysis of DC level mode

In Chapter 2 we discussed the signal and noise analysis of conventional APS, which is the APS swing output. Analysis of the sense node voltage of APS pixel in general, or its DC level in particular, is missing in the literature. This is mainly due to the fact that the swing has always been considered the output of APS and the analytical work has been focused on the signal and noise of the swing output. In this section we will introduce the exact analytic derivation of the signal and noise of the DC level of the sense node voltage.

4.1.1. Sense node voltage during reset

During the reset period of the APS operation cycles, the gate of the reset transistor (M_1 in Figure 2-2(a)) is set to V_{DD}. M_1 is turned on in order to bring v_S up to V_{DD}. However, as v_S increases during reset, the gate-source voltage across M_1 decreases and eventually goes below the threshold voltage of M_1. In sub-threshold mode of operation, a transistor can supply much less current; thus, the speed of reset drops drastically. In one example, it takes less that 0.2 ns for M_1 to bring the sense node voltage from 0 V to $V_{DD} - V_T$, while it takes more than 1 ms for it to bring v_S the rest of the way up to V_{DD} [4.7].

In low-level light conditions, where v_S does not drop much during integration, M_1 will always operate in sub-threshold. The reset time is much shorter than the time necessary for complete reset. As a result, the reset will always be incomplete. The drain current i_D of a transistor in sub-threshold is given by [4.8]

$$i_D = \frac{W}{L} I_0 e^{\left(\frac{v_{GS}\kappa}{v_T} - \frac{v_{SB}(1-\kappa)}{v_T}\right)} \left(1 - e^{-v_{DS}/v_T}\right), \qquad (4\text{-}1)$$

where W and L are the width and length of M_1, respectively, v_T is the thermal voltage, κ is a correction parameter that represents the slope of variation of the surface potential, ψ_S, with respect to the gate voltage in the sub-threshold [4.9], v_{SB} is the

source–body voltage, v_{GS} is the gate–source voltage, and v_{DS} is the drain–source voltage across M_1. The sense-node voltage will be obtained by solving (4-1) together with

$$\frac{dv_S(t)}{dt} = \frac{i_D(t) - i_{PH}(t) - i_{DK}(t)}{C_{PH}(v_S(t))} . \tag{4-2}$$

First, (4-1) is simplified to have i_D explicitly in terms of the sense-node voltage v_S i.e.,

$$\begin{aligned} i_D &= \frac{W}{L} I_0 e^{\left(\frac{v_{GS}\kappa}{v_T} + \frac{v_{SB}\kappa}{v_T} - \frac{v_{SB}}{v_T}\right)} \left(1 - e^{-\frac{v_{DS}}{v_T}}\right) \\ &= \Gamma e^{-\frac{v_{SB}}{v_T}} \left(1 - e^{-\frac{v_{DS}}{v_T}}\right) \\ &= \Gamma \left(e^{-\frac{v_{SB}}{v_T}} - e^{-\frac{v_{DB}}{v_T}} \right) = \Gamma e^{-\frac{v_S}{v_T}} - \Lambda , \end{aligned} \tag{4-3}$$

where

$$\Gamma = \frac{W}{L} I_0 e^{\frac{v_G \kappa}{v_T}} \text{ and} \tag{4-4}$$

$$\Lambda = \Gamma e^{-\frac{v_D}{v_T}} . \tag{4-5}$$

The common body of the pixel is grounded ($v_B = 0$). Now, combining (4-2) and (4-3), the following differential equation for v_S during reset is obtained:

$$\frac{dv_S(t)}{dt} = \frac{\Gamma}{C_{PH}(v_S(t))} e^{-\frac{v_S(t)}{v_T}} - \frac{\Lambda + i_{PH}(t) + i_{DK}(t)}{C_{PH}(v_S(t))} . \tag{4-6}$$

During the short reset period, the photocurrent and the dark current can be assumed constant. The capacitance of the photodiode does not change much either, due to the

limited variation in v_S. Thus, $C_{PH}(v_S(t)) = C_0$ is assumed. Equation (4-6) then has a closed-form solution given by

$$v_S(t) = v_T\left(-\ln B + \ln\left[A - e^{-\frac{tB}{v_T}}\left(A - Be^{\frac{v_1}{v_T}}\right)\right]\right), \tag{4-7}$$

where v_1 is the initial value, which is the value of v_S at the beginning of reset as shown in Figure 4-1, and A and B are defined as:

$$A = \frac{W}{LC_0} I_0 e^{\frac{v_G \kappa}{v_T}} \text{ and} \tag{4-8}$$

$$B = Ae^{-\frac{v_D}{v_T}} + \frac{i_{\text{PH}} + i_{\text{DK}}}{C_0}. \tag{4-9}$$

In (4-8) and (4-9), Γ and Λ have been replaced using (4-4) and (4-5). Equation (4-5) is the result of the reset time analysis. It gives the sense node voltage during reset time, assuming $v_S(0) = v_1$. The equation assumes that the reset transistor is in sub-threshold during the reset time, meaning that $V_{\text{DD}} - v_1$ should be smaller than the threshold voltage of the reset transistor. Sense node voltage at the end of reset, v_2, is simply given by $v_S(t_r)$ in (4-5), where t_r is the duration of the reset period.

A fundamental problem caused by incomplete (sub-threshold or soft) reset for conventional APS is image lag. Improving the quality of reset is possible by employing better reset structures [4.10], [4.11]. Correlated double sampling (CDS) can also remove this image lag to some extent. Our approach, however, is using the incomplete reset to its advantage, and it does not need CDS. It is sufficient to sample the sense-node voltage only once, at the middle of the integration period, to get the desired output signal value. However, there are some drawbacks to this choice. Unlike the swing, the DC level varies nonlinearly with the input photocurrent. Post-processing can be added to compensate for the nonlinear response, if needed. In addition, it takes some time for the DC level to settle to its steady state value. In Figure 4-1 for example, it takes about 0.5 s for the DC level of the sense node, which

has i_{PH} = 30 fA, to settle to the desired level. It should be noted however, that a regular APS operation also needs long integration times for detecting low photocurrent levels. For a similar current, it would take about 1 s for the sense node voltage to drop half way from V_{DD}. Finally, from the device perspective, the DC level depends on the properties of both the photodiode and the reset transistor. Compared to the swing, which is only dependent on the photodiode, the DC level is more susceptible to chip-to-chip variation.

4.1.2. Sense node voltage after integration and DC level mode analysis

Figure 4-1 shows the v_S under periodic integration and reset for a V_{DD} = 2.5 V. We mentioned before that an incomplete reset happens due to the sub-threshold operation of the reset transistor. The value of v_S at the end of reset period is defined as v_2, and that at the end of integration period is defined as v_1. The differential value, (v_2 - v_1), has always been analyzed and extracted as the output value of APS. Precise values of v_2 and v_1 however have not been calculated. We obtain these values here using equation (4-7) and Table 2-1 in the following.

Equation (4-7) gives the sense node voltage during the reset period. Value of sense node voltage at the end of reset period, v_2, is obtained by replacing t with t_r in (4-7). The result is

$$v_2 = -v_T \ln B + v_T \ln\left(A\left(1 - e^{-\frac{t_r B}{v_T}}\right) + B e^{-\frac{t_r B}{v_T}} e^{\frac{v_1}{v_T}} \right), \tag{4-10}$$

where A and B are given in equations (4-8) and (4-9) and t_r is the duration of reset period.

In section 2.3.2, value of sense node voltage during the integration period was analyzed and calculated. The value of sense node voltage at the end of integration time, v_1, can be extracted in a similar way, from Table 2-1, to be

$$v_1 = \left[(v_2 + \varphi)^{3/4} - \frac{3(i_{\mathrm{DK}} + i_{\mathrm{PH}})}{4C_0} (v_2 + \varphi)^{-1/4} t_{\mathrm{int}} \right]^{4/3} - \varphi, \qquad (4\text{-}11)$$

where t_{int} is the duration of the integration period. Equation (4-10) calculates v_2 having v_1, and equation (4-11) calculates v_1 having v_2. For a given set of parameters of operation for an APS pixel, equations (4-10) and (4-11) can be solved together to obtain the steady-state values of both v_1 and v_2, and consequently $(v_1 + v_2)/2$ which is the DC level output of the pixel. Figure 4-2 shows the analytically extracted DC level output and compares it to the analytically extracted swing output.

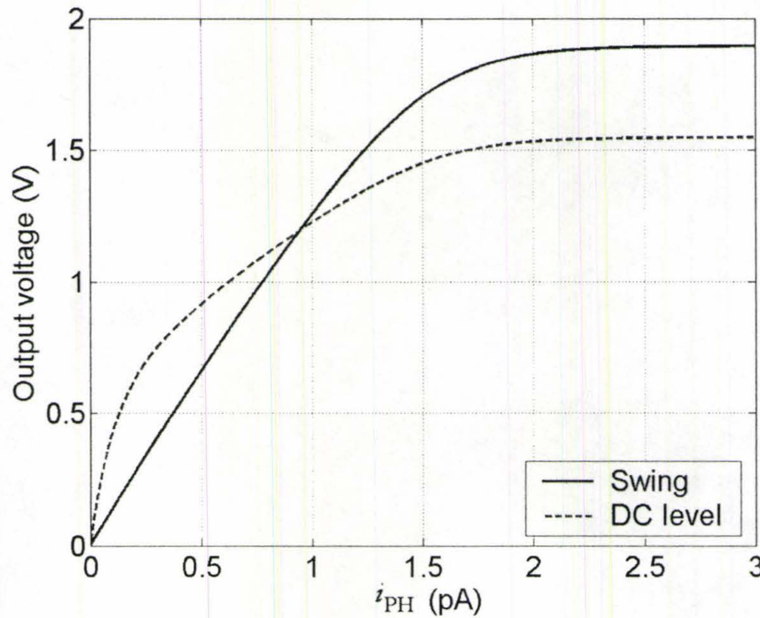


Figure 4-2: Steady-state DC level $((v_1 + v_2)/2)$ and swing $(v_2 - v_1)$ output of the sense node versus i_{PH}. The DC level has a value close to V_{DD} for zero photocurrent. The curve shown is the displacement of the DC level output from its dark-level value, which corresponds to the output signal. As the DC level corresponding to the zero photocurrent is constant for every pixel, CDS will not be necessary.

Figure 4-2 shows that the DC level output has higher values for lower levels of incident light. However, this advantage becomes less significant for larger induced photocurrents, and eventually the swing becomes even better. The DC level also saturates faster and has lower dynamic range.

4.1.3. Noise analysis of DC level mode: Auto-regressive noise model

In section 2.4, we derived equations for the noise of APS sense node voltage during integration and also during reset. In this section, we introduce the noise analysis of the DC level of the APS sense node voltage.

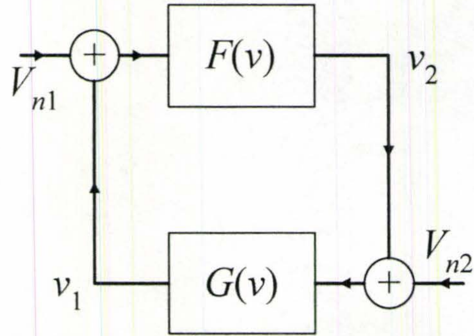


Figure 4-3: Block diagram showing how reset and integration noise contribute to the steady DC level. Reset noise and integration noise are represented by V_{n2} and V_{n1} respectively. The total noise is calculated in $(v_1 + v_2)/2$.

For noise analysis, the signal flow in an APS pixel is modeled with a periodic reset and integration system, using the feedback system shown in Figure 4-3. Each function in Figure 4-3 represents the relationship between the input and the output of each block. $F(v)$ represents reset, and $G(v)$ represents integration. For example, F accepts v, which is the signal value at the beginning of reset, and generates $F(v)$, which is the signal value at the end of reset. V_{n1} and V_{n2} are the integration and reset noises respectively, which are added to the sense node voltage at the end of their corresponding period. We calculate the noise for fixed values of i_{PH}, t_{int}, t_r, and for the steady-state values of v_1 and v_2 shown in Figure 4-1. The goal is to assume V_{n1} and V_{n2} as the inputs to the system and calculate the noise in v_1 and v_2 and consequently $(v_1 + v_2)/2$ as the output of the system.

We start by rewriting equation (4-10) to obtain $F(v)$ as

$$F(v) = -v_T \ln B + v_T \ln\left(A\left(1 - e^{-\frac{t_r B}{v_T}}\right) + Be^{-\frac{t_r B}{v_T}} e^{\frac{v}{v_T}} \right), \tag{4-12}$$

and rewriting equation (4-11) to obtain $G(v)$ to be

$$G(v)=\left[(v+\varphi)^{3/4}-\frac{3(i_{\mathrm{DK}}+i_{\mathrm{PH}})}{4C_0}(v+\varphi)^{-1/4}t_{\mathrm{int}}\right]^{4/3}-\varphi. \tag{4-13}$$

The noise analysis of the system in Figure 4-3 is done by Taylor series expansion of (4-12) and (4-13) to the form given by

$$F(v+V_n)=F(v)+\frac{\partial F}{\partial v}|_v V_n=F(v)+\alpha V_n \text{ and} \tag{4-14}$$

$$G(v+V_n)=G(v)+\frac{\partial G}{\partial v}|_v V_n=G(v)+\beta V_n. \tag{4-15}$$

Equation (4-14) shows that the output noise of F is related to the input noise by a factor of $(dF/dv)|_v$ which we define as α and calculate it to be

$$\alpha=\frac{dF}{dv}|_v=\frac{Be^{-\frac{t_rB}{v_T}}e^{\frac{v}{v_T}}}{A\left(1-e^{-\frac{t_rB}{v_T}}\right)+Be^{-\frac{t_rB}{v_T}}e^{\frac{v}{v_T}}}. \tag{4-16}$$

Similarly we have

$$\beta=\frac{dG}{dv}|_v=\left[(v+\varphi)^{3/4}-\frac{3(i_{\mathrm{DK}}+i_{\mathrm{PH}})}{4C_0}(v+\varphi)^{-1/4}t_{\mathrm{int}}\right]^{1/3}\times$$

$$\left[(v+\varphi)^{-1/4}+\frac{3(i_{\mathrm{DK}}+i_{\mathrm{PH}})}{4C_0}(v+\varphi)^{-5/4}t_{\mathrm{int}}\right]. \tag{4-17}$$

Equations (4-16) and (4-17) suggest that the noise power of the output of the F (and also G) block is linearly proportional to the input noise power with the ratio α^2 (β^2). Given these parameters, the output noise power in $(v_1 + v_2)/2$ based on the input reset and integration noise powers can be calculated for the system of Figure 4-3 to be

$$\overline{V_n^2} = \frac{1}{4}\left(\overline{V_{n1}^2}\frac{\alpha^2\beta^2 + \alpha^2}{1-\alpha^2\beta^2} + \overline{V_{n2}^2}\frac{\alpha^2\beta^2 + \beta^2}{1-\alpha^2\beta^2}\right), \tag{4-18}$$

which is the general formula for the noise of the sense node DC level voltage.

Expanding (4-17) and considering only the highest order nonzero terms, results in the following approximation for β:

$$\beta \approx 1 - \frac{(i_{\text{DK}} + i_{\text{PH}})^2 t_{\text{int}}^2}{8C_{\text{PH}}^2(\nu + \varphi)^2}. \tag{4-19}$$

In practice, the value predicted for the sense node voltage given in (4-13) at the end of integration time is very close to the one given using the linear equation of (2-1). Figure 4-4(a) shows the calculated values of β given in (4-17) and (4-19) for different photocurrent levels. It shows that the assumption $\beta = 1$ is relatively accurate for low-level light conditions.

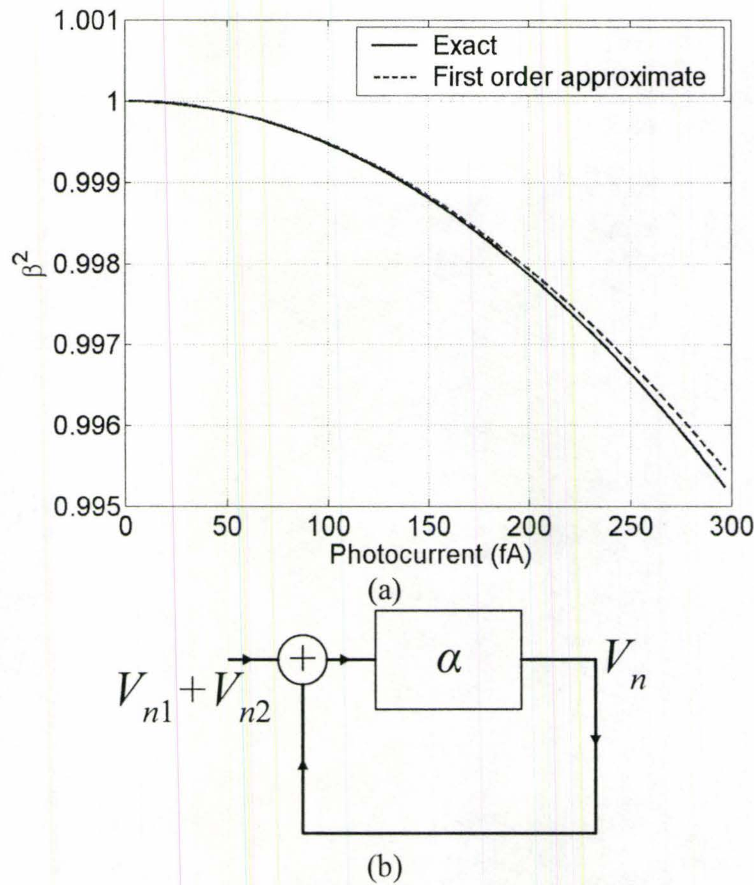


Figure 4-4: (a) Exact values of β obtained in (4-17) and (4-19) are shown vs. i_{PH}, where t_{int} = 30 ms and v_2 = 2.3 V. Note that for low photocurrents, $\beta \approx 1$. (b) Simplified noise diagram of Figure 4-3, assuming $\beta = 1$.

Assuming $\beta = 1$ means that the noise in v_S at the beginning of integration will appear at the end of integration with the same power. Thus, the noise analysis ends up in the simple system of Figure 4-4(b), which, assuming steady-state conditions, results in an autoregressive noise in the DC level with the total power give by

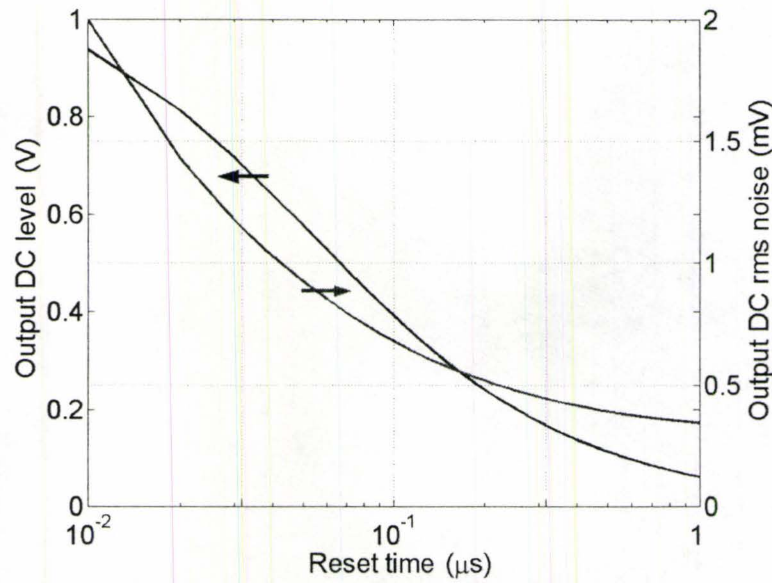
$$\overline{V_n^2} \approx \frac{1}{2}\left(\overline{V_{n1}^2} + \overline{V_{n2}^2}\right)\frac{\alpha^2}{1-\alpha^2}. \tag{4-20}$$

The noise calculated in (4-20) varies with t_r as α given in (4-16) is a function of t_r. If t_r gets large for example, α tends to be 0. This means that a good reset is performed, which suppresses most of the noise. Remember that a perfect reset should leave no noise in the sense node. On the other hand, if t_r is too small, α will tend to be 1. In this case, almost all of the noise power will be handed to the next stage of integration, and

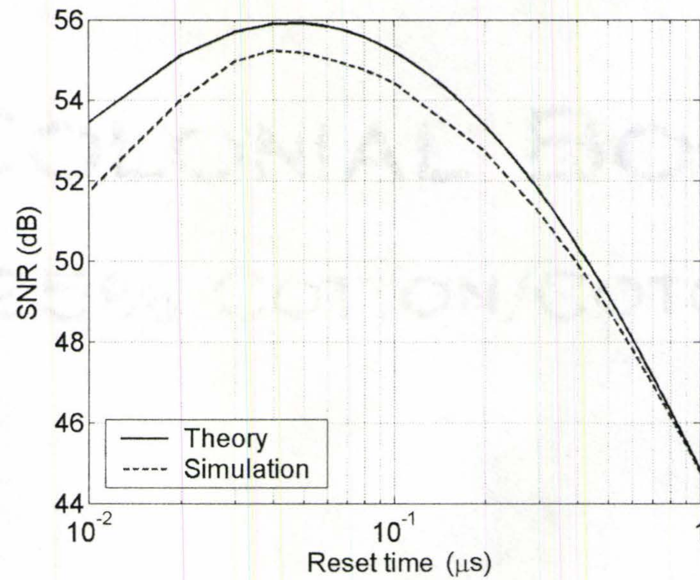
a large value of autoregressive noise will accumulate in the output DC level. This is the disadvantage of choosing small values for the reset time.

4.2. DC level SNR optimization

Figure 4-5(a) shows how the DC level output and its noise vary with the reset time. For larger values of reset time, the signal value is small. As the reset time becomes smaller, the noise increases more rapidly. Therefore, SNR will have an optimum value as the reset time is varied. Figure 4-5(b) shows how SNR varies with t_r. In this example, the optimum SNR occurs at a reset time of 0.05 μs.



(a)



(b)

Figure 4-5: (a) Output DC level and its noise vs. reset time. Both the signal and noise increase with decreasing the reset time. The noise however, increases more sharply. (b) The SNR of the output DC level has an optimum. In this example, i_{PH} = 10 fA, and t_{int} = 30 ms.

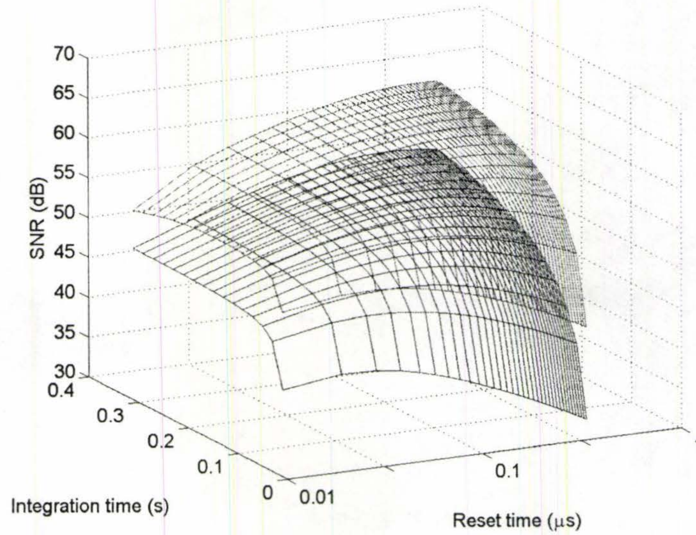
The APS circuit is also simulated for the DC level output to verify the SNR calculations. We have used the periodic steady state (PSS) and periodic noise (Pnoise) analysis of the Cadence Spectre tool for the switched noise simulation. Figure 4-5(b) shows the simulated SNR curve. The simulation suggests a maximum

SNR of about 55.3 dB for a reset time of 0.04 μs, which is close to the results of our theory with a maximum SNR of 56 dB. The slight difference in SNR is due to the difference in the sub-threshold model of the reset transistor. The effect is more significant for smaller reset times. For larger reset times, better reset happens, and the outcome is less sensitive to the sub-threshold model.

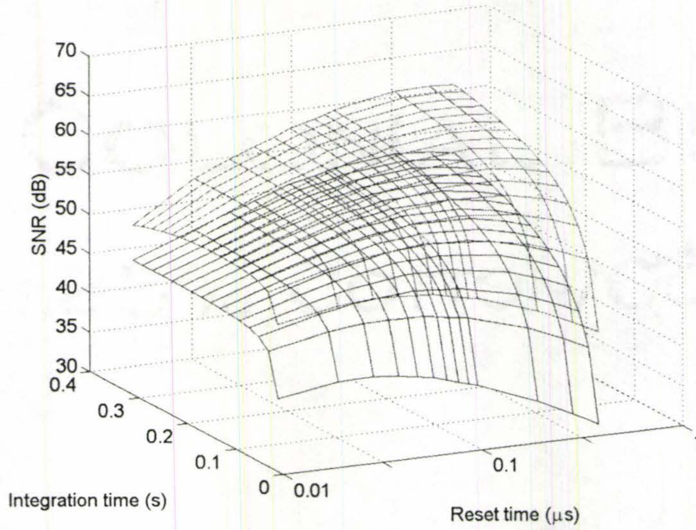
This calculation presents SNR values in the range of 54–56 dB. These are high SNR values compared to reports in the literature. A maximum SNR of about 45 dB is shown in [4.12] for an i_{PH} of above 1 pA. Many SNR curves have been shown in [4.13], with each maxima well below 50 dB. For an output signal of about 0.7 V, Tian et al. [4.7] represents a maximum SNR of about 51 dB. The improved reset solution of [4.14] reports SNR values of about 52 dB. Our method has achieved better performance for lower level light as the DC level is a more sensitive output for smaller i_{PH} values, as shown in Figure 4-2.

Increasing t_{int} can improve the performance of the conventional APS. We have shown in section 2.5 that the maximum SNR can be achieved by varying t_{int}, which does not depend on i_{PH} Figure 2-10(b). Even though increasing the integration time is a simple and effective approach, it may not be practical for some applications. By varying t_r and using the proposed DC level, better SNR can be achieved with the photodetector operating at the same speed.

The optimum SNR that was achieved, however, can vary with both t_{int} and i_{PH}. Considering the constraints imposed by the application, the values of t_{int} and t_r can be jointly optimized. The result will be better than having t_{int} fixed and varying t_r only. For example, with the same parameters that resulted in Figure 4-5(b), an optimum SNR of 59 dB is obtained by letting the device integrate for a longer time. For $t_{int} = 70$ ms, the optimum is achieved at $t_r = 0.1$ μs. Figure 4-6(a) shows how the SNR achieved by our theory varies with both the integration and the reset times. The simulated SNR surfaces are very close to the surfaces of Figure 4-6(a) and are shown separately in Figure 4-6(b).



(a)



(b)

Figure 4-6: (a) Theoretical and (b) simulated SNR curves of the proposed DC level method as a function of both the integration time and the reset time. The surfaces correspond to i_{PH} = 3 fA (lower) and i_{PH} = 12 fA (upper).

4.3. Measurements and comparison

Figure 4-7 shows the measured signal-to-noise ratio (SNR) of the pixel. The SNR values have been evaluated by multiple measurements of the signal at each level of light input. About 50 to 100 voltage samples are collected at each illumination level, and their mean is interpreted as the signal value, and their standard deviation as the noise. The

SNR has been evaluated for both swing ($v_2 - v_1$) and DC level ($(v_2 + v_1)/2$. The chip is illuminated at 640 nm using a narrowband filter ($\Delta\lambda \approx 20$ nm). The light power is measured with a Newport power meter calibrated at the same wavelength. Our low levels of light power are achieved by using several attenuators in the optical path. At light powers less than 0.1 μW/cm^2, the measured power by the power meter is very noisy compared to the DC level of our pixel, which is still very stable. At these low levels of light, the output of the power meter has been sampled multiple times, and then averaged to provide the light power values shown.

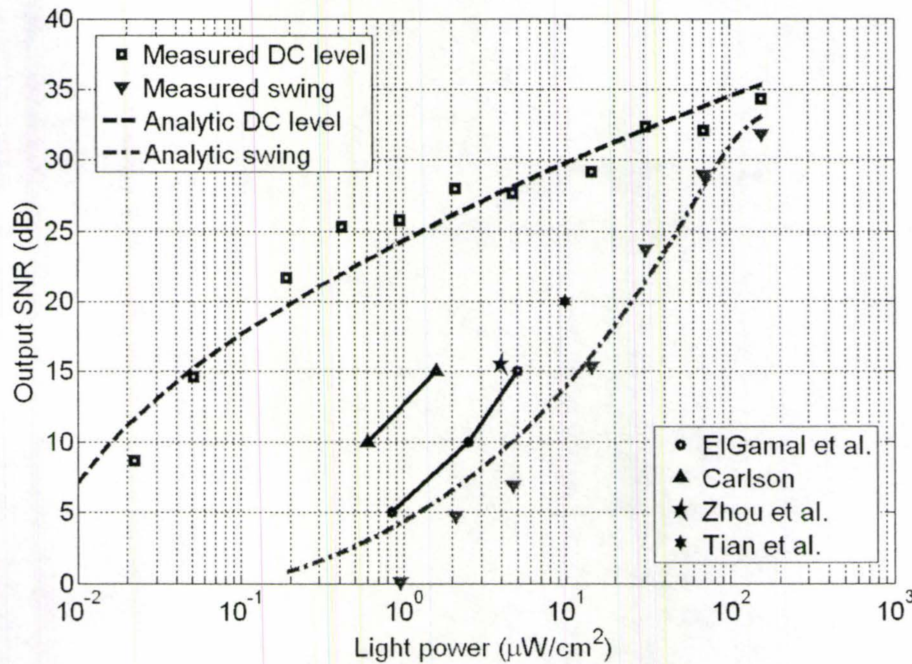


Figure 4-7: Analytically derived SNR of the APS, measured SNR values for our APS, and SNR values reported for some other low-light-level APS circuits in the literature (from the top: [4.12], [4.13], [4.15], [4.7]). The data has been gathered from a variety of pixel sizes. The size of the pixels used in the experiments affects the reported SNR values at different light powers. The data have been adjusted to compensate for the size differences and to make a fair comparison of the different reported SNR values.

Measurements in Figure 4-7 show that the DC level of the output can detect light levels which are two decades of less power compared to the swing of the same pixel. The DC level has about 20 dB better signal-to-noise ratio than the swing at about 1 μW/cm^2. The DC level output has also been compared to some SNR values of other APS circuits reported in literature. Figure 4-7 shows some SNR points achieved in the

work of El Gamal *et al.* [4.12], Carlson [4.13], Zhou *et al.* [4.15], and Tian *et al.* [4.7]. It should be noted that parameters like the pixel size, integration time or readout rate, or the illumination spectrum affect the SNR of the APS, and they should be considered to make a fair comparison of the performance of the pixels. Appropriate changes have been made to the SNR points in Figure 4-7 to account for these differences. For example, the integration times of the pixels were 30 ms in all works except in [4.13] which was 8 ms, for which a 3 dB correction was made to the SNR value. For the light power at the low levels of Figure 4-7, the SNR of the DC level stands well above the conventional APS.

The high SNR of the DC level approach is a combined result of having higher signal levels and lower noise levels. Figure 4-2 compares the analytically obtained signal levels for the two approaches for the same integration time of 30 ms. Although Figure 4-2 suggests that the DC level approach generates a higher signal value than the conventional swing, lhe ower level of noise also greatly contributes to the higher SNR of Figure 4-7.

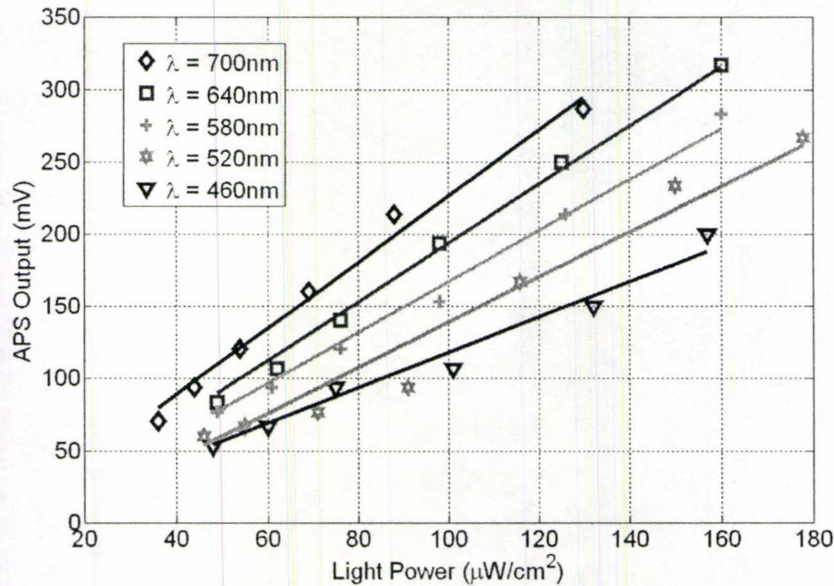


Figure 4-8: Measured swing of the sense node voltage of the APS vs. the power of light at different wavelengths. The curves show that the generated photocurrent of the APS approximately doubles by changing the wavelength of light in the visible range.

Figure 4-8 shows the measured variation of the output of our APS within the

visible range spectrum. It shows a factor of two difference between the responses at the lower end and the higher end of the spectrum, which corresponds to doubling of the photocurrent of the APS. The power of the shot noise will also be doubled, causing an approximately 1.5 dB increase in the SNR value. Doubling the pixel area, or the integration time of APS will also increase its SNR by about 1.5 dB.

The DC level mode of operation of the APS, eliminates the need for CDS. We have observed that at low-light-levels, the swing of the output of APS is negligible, and the output voltage looks like a DC line, as shown in Figure 4-1. Thus, a single sample of the output, preferably at the middle of the integration period, is enough. Displacement of the DC level value from its dark level corresponds to the output of the pixel. It should be noted, however, that if the APS has to be used in an application where temperature variation is significant over short periods of time, then the dark value of the DC level can be affected, and should also be sampled.

The DC level mode of operation of APS does not alter the pixel structure, which preserves the high fill-factor advantage of conventional APS. The DC level performance can be improved by altering the reset mechanism. This can be achieved by decreasing W/L of the reset transistor, decreasing the voltage applied to its gate during reset, or shortening the reset time. These changes will reduce the quality of reset, and increase the sensitivity of the DC level. Our experiments show that variation of the V_{DD} of the reset transistor has negligible effect on the output DC performance. Thus, the reset transistor and the source follower can share the same V_{DD} line. This improved sensitivity can complement the other attractive features of the CMOS photodetectors compared to PMTs, APDs, and CCDs, and can potentially replace them in many emerging biomedical applications where low-light-level sensitivity is a requirement.

Chapter 5

AVALANCHE PHOTODIODES AND APD-BASED SYSTEMS

Very weak optical signals have to be measured in different fields of sciences including nuclear physics, chemistry, biology, and astronomy [5.1], [5.2]. For example, very low levels of fluorescence emission should be detected from the spots on a DNA microarray that correspond to weakly expressed genes of the sample [5.3]. Detection of these light levels can be done using charge coupled devices (CCDs) with ultra-low-noise readout circuitry [5.4], [5.5], or modern CMOS photodetectors [5.6], [5.7], [5.8]. In these devices, the generated photocurrent is integrated in internal capacitors, to convert the photocurrent to a voltage. Therefore, detecting lower levels of light with these devices requires longer integration times.

Applications like quantum cryptography [5.9], profilometry of remote objects [5.10], and fluorescence spectroscopy [5.11], however, require both high sensitivity and fast response of the photodetector. For example, photomultiplier tubes (PMTs) with microchannel plates are commonly used in fluorescence spectroscopy applications to detect single photons in pico- to nano-seconds regime [5.12], [5.13]. In terms of sensitivity and fast temporal response, PMTs are the best photodetectors available and are widely used in applications such as fluorescence lifetime measurements. For the emerging miniaturized and portable applications, however, PMT based photodetection systems have several significant disadvantages including: 1)

requirement of high voltage (~1 kV or higher), which needs bulky specialized circuitry and power supplies; 2) use of glass vacuum tubes that are very fragile and large in size which is not ideal for rugged and size sensitive medical and industrial applications; and 3) time-consuming individualized production/quality control with significantly high cost [5.14], [5.15], [5.16].

Avalanche photodiodes (APDs) operated in Geiger mode [5.17], are the semiconductor equivalent of PMTs. Avalanche photodiodes are used in discrete packages made with special processes, and are often connected to a detection and control electronic chip [5.18]. To increase the use of APD-based detector systems for biomedical applications, integration of the APD and peripheral circuitry on the same chip is highly desired [5.19].

Standard CMOS technology can be used to integrate the photodetector and driving circuits on the same chip. Such CMOS circuits are inexpensive and typically consume low power. Also fast and compact digital circuit modules are available in CMOS. For imaging applications, the active pixel sensor (APS) structure is the most popular pixel configuration in CMOS. The APS consists of a photodiode, and reset, buffer and select transistors. Recent APS circuits in CMOS technology have improved in resolution and sensitivity [5.20], [5.21]. However, the APS uses a photocurrent integration technique, so it cannot offer both high speed and low-light detection characteristics at the same time.

5.1. Overview of APD implementations in literature

Fabrication of APDs in CMOS technology makes it possible to achieve the benefits of the APD as photodetector, and the necessary peripheral circuits on the same chip for an integrated system. However, APDs are difficult to make in CMOS technology, as they need special fabrication steps that might not be available in standard CMOS process. Nevertheless, significant advances have been reported by several groups [5.22]–[5.26]. In [5.22], results of a Geiger mode avalanche photodiode (GMAP) fabricated in 1.5 μm CMOS for use as a photo-receiver was reported. A data rate of 1 Gb/s in the optical data link was achieved from simulations in this work. In [5.23],

several silicon avalanche photodiodes (SAPDs) were fabricated in 0.8 μm CMOS technology. The SAPDs had a 0.5 mm^2 area, with a 400 pA/mm^2 measured dark current, but they were not operated in Geiger mode. In [5.24], the performance of a linear array of single photon avalanche diodes (SPADs) with passive quenching in 0.8 μm CMOS technology was reported. For the 5 μm APD, the dark count was 100 Hz and the dead time of the output was 1 μs. In [5.25], a SPAD with active quench and reset circuits in 0.8 μm CMOS technology was described. A peak detection efficiency of 45 % for a 10 V applied excess bias was reported. At this voltage, the dark count was 40 kcounts/s at room temperature. The overall size of the chip that operates a single 12 μm diameter APD was 1.1 mm × 2 mm. In [5.26], a SPAD array in 0.35 μm technology was described. The peak photon detection probability for this SPAD array was 5 % for a 3 V excess bias, and the dead time was 40 ns.

5.2. APD design

In this work, we have designed and fabricated an APD, along with the driving circuitry, in a standard 0.18 μm CMOS technology [5.27]. In this section, the structure of the APD device and its guard ring will be introduced. Fabrication of the APDs is discussed in section 5.3. Then, in section 5.4, the APDs will be characterized, and the breakdown mechanism will be discussed. Geiger-mode of operation of the APDs are measured and analyzed in both passive and active structure in sections 5.5 and 5.7. Our results are also compared with those for the previous implementations of APDs in CMOS.

5.2.1. APD layout

A regular p$^+$/n-well diode is fabricated in standard CMOS technology as a p$^+$ region implanted within an n-well region. In this diode, the breakdown current will not flow uniformly across the area of the p$^+$ region. The breakdown region of such a diode will be at its edge (this will be discussed later in section 5.4). This due to the higher peak electric field caused by the narrower depletion region at the corners of the diode junction. As the reverse bias increases, the electric field at the perimeter will reach the

onset of avalanche first, and the current will flow there. In APDs, however, it is desired for the breakdown region to be spread over the area of the diode and not at its corners. We have made this possible by creating a p-type guard ring around the p^+ active area of the APD, as shown in Figure 5-1. To create the guard ring, an n-well region is placed within the p^+ region, which is against the conventional rules of the standard CMOS. In our design, the width of the guard ring is 3 μm, with a depth of approximately 0.5 μm. The doping concentration of the p-well is in the range of 10^{17} cm^{-3}, compared to 10^{19} cm^{-3} for the p^+ region. It will be shown that the designed device has excellent avalanche characteristics. However, it should be noted that standard CMOS technology is targeted for digital and analog applications and not optical imaging devices. Most of our design parameters are not optimum, and are dictated by constraints of the fabrication technology. But because it is a standard technology, the cost is very low.

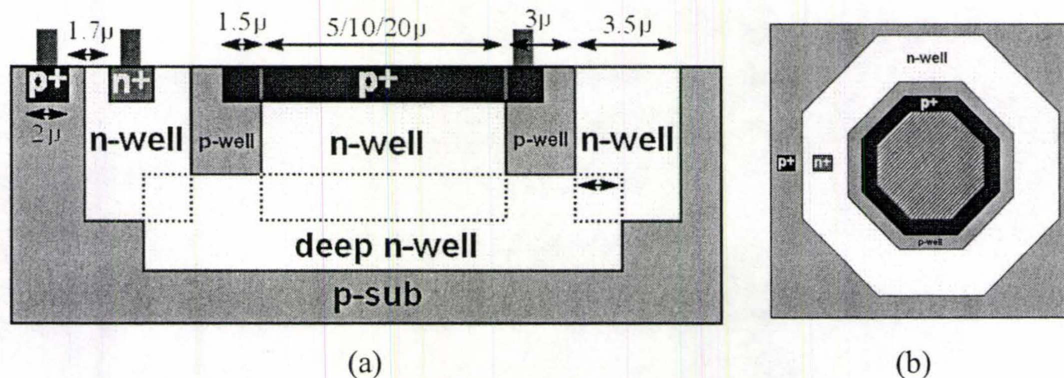


Figure 5-1: (a) Cross section and (b) plan view of the layout of our APD. Putting an n-well, inside a p^+ region, creates the avalanche area and also the guard ring.

5.2.2. Device simulation

Figure 5-2 shows the profile of the electric field created in our APD. The GENESIS simulation package is used to simulate some of the APD performance characteristics. The structure is produced with MDRAW, and the electric field profile is obtained with DESSIS [5.28]. Figure 5-2 shows that the peak electric field is spread under the active region of the APD, which is the p^+/n-well junction.

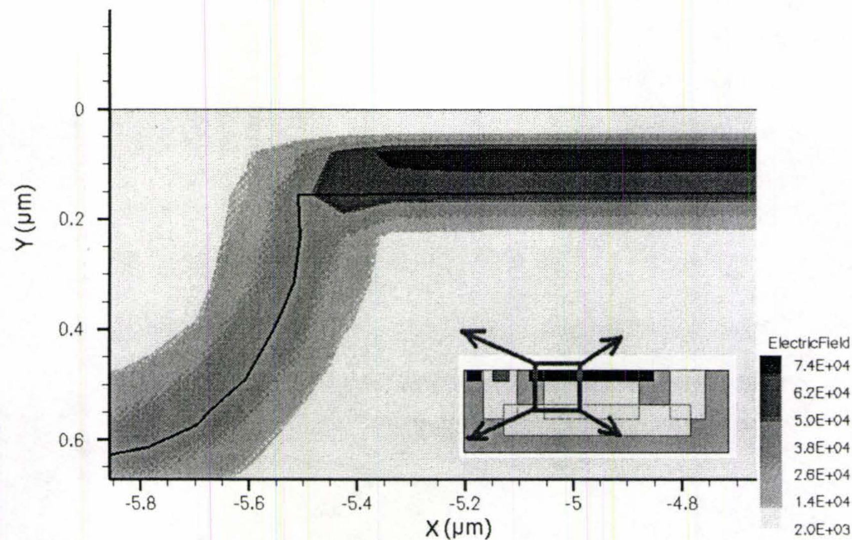


Figure 5-2: Device simulation of the APD under reverse bias, using the DESSIS tool. It shows that the maximum electric field will appear in the desired p^+/n-well junction.

5.3. APD fabrication

We have fabricated our APD in a standard 0.18 μm, single poly, six metal, salicide CMOS technology. We have fabricated APDs with three different diameters: 5 μm, 10 μm, and 20 μm. Figure 5-3 shows the photomicrograph of these APDs, with octagonal active regions. The guard rings of the APDs are shielded by metal layers. A circular shape is desired for APDs to reduce the possibility of corner breakdown. However, the layout rules for the technology does not allow for a circular shape, so instead, the octagonal shape, which is closest to a circle that can be made, is designed. Measurements presented later show no corner breakdown of our APDs.

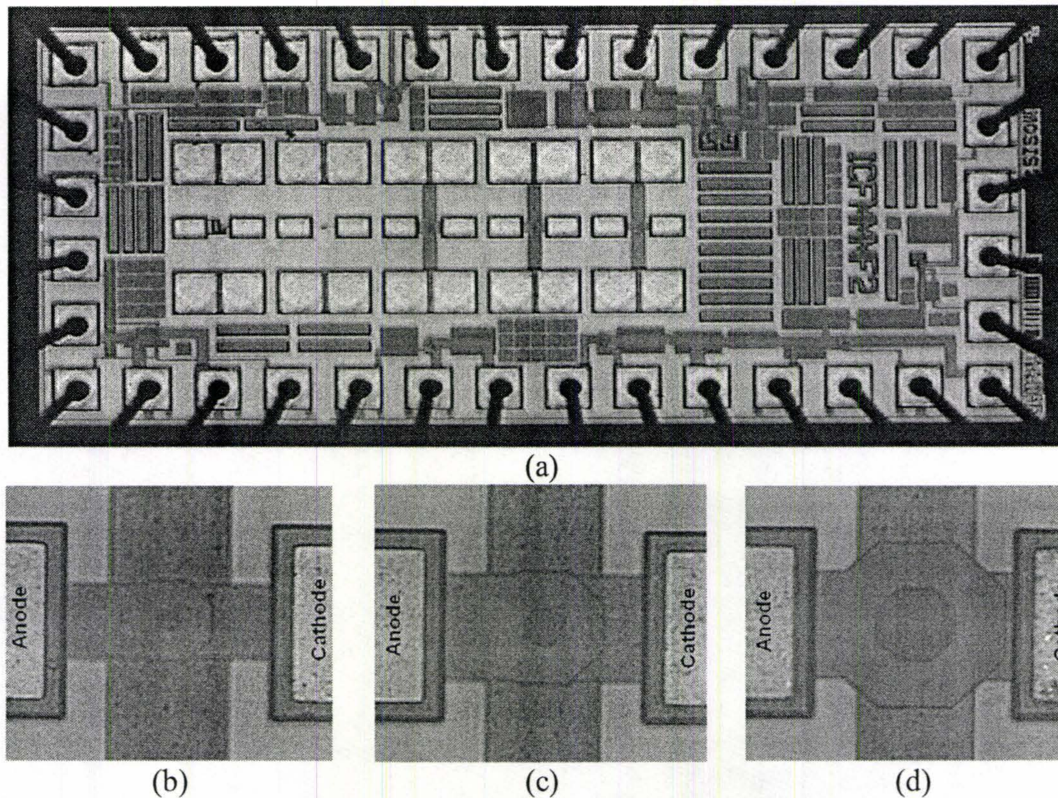


Figure 5-3: (a) Photomicrograph of the chip containing APD devices and circuit. Layouts of our APDs with (a) 5 μm, (b) 10 μm and (c) 20 μm diameters. Design rules of the technology do not allow circular features. We have used 45° rotated lines to draw octagons, the closest shape that can be generated to circles.

5.4. APD characterization

The doping concentration levels in CMOS increase as the technology scales down, causing an increase in the peak electric field in the depletion region of the diodes. Therefore, the breakdown voltage decreases and the width of the depletion region will also decrease. Eventually, the doping levels can become high enough, resulting in a very thin depletion region and tunneling breakdown will replace avalanche breakdown. Tunneling breakdown is known to happen for diodes with a breakdown voltage of about 7 V and lower.

For photon counting applications, we are interested in a diode that breaks down by avalanching. To our knowledge, all previous implementations of APDs in CMOS, have used 0.35 μm or larger technology scales. Therefore, it is important to first

investigate the breakdown mechanism of our APD made in this smaller dimension CMOS technology.

5.4.1. *I-V* characteristics

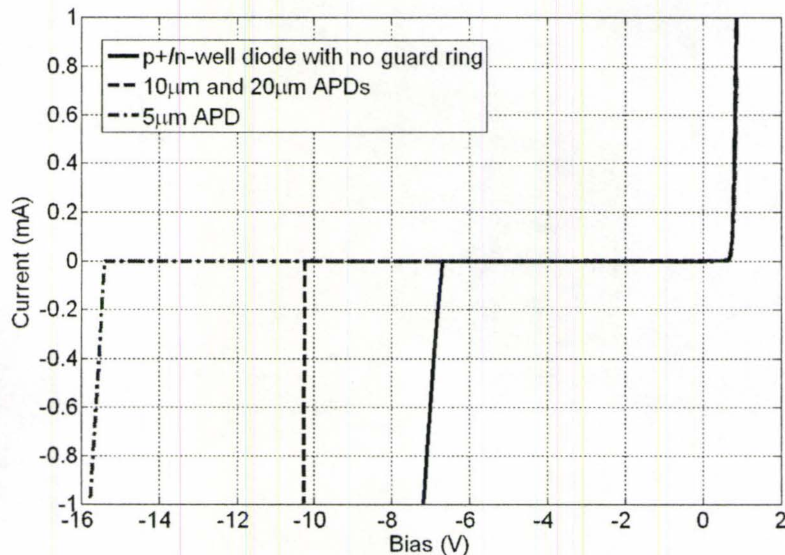


Figure 5-4: Measured *I-V* profiles for different diodes. While a regular p^+/n-well diode shows a low breakdown voltage, our APDs with guard ring show an avalanche breakdown at 10.2 V. The 5 μm APD however, has a high breakdown voltage.

Figure 5-4 shows the measured *I-V* curves for three different diodes that we have made in CMOS 0.18 μm technology. The measured curves are obtained with a 1 mA current compliance to protect the diodes. For a regular CMOS p^+/n-well diode that has no guard ring, that is the p^+ region being surrounded in the n-well as shown in Figure 5-5(a), breakdown happens at approximately 6.7 V. It also does not have a sharp breakdown profile, indicating that edge breakdown is occurring. Our APD, with the structure shown in Figure 5-5(b), has a very sharp breakdown at 10.2 V. The curve shows that the guard ring is effectively eliminating the edge breakdown of the p^+/n-well diode. The high breakdown voltage also suggests that the breakdown mechanism is avalanche, which will be proven later when the temperature-dependent analysis of the breakdown characteristics is described.

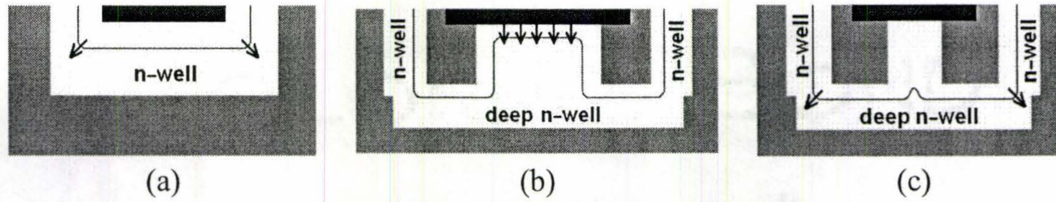


Figure 5-5: (a) Breakdown site of a regular p^+/n-well diode compared to (b) the breakdown site of the 10 μm APD and (c) the breakdown site of the 5 μm APD. The line shows the extent of the depletion region in the n-well.

The 10 μm and 20 μm APDs have similar breakdown behavior. However, interestingly, the 5 μm APD shows a different profile. Its breakdown starts at around 15.4 V with an edge breakdown like behavior. Figure 5-5 illustrates the reason for the different breakdown characteristic of this diode. Figure 5-5(b) shows the cross-section of the 10 μm APD and the boundary of its depletion region. The effective area of the APD is reduced due to the depletion region around the guard ring. The area of the 10 μm APD is large enough to accommodate this depletion region such that the breakdown happens at the desired p^+/n-well junction. However, for the 5 μm APD shown in Figure 5-5(c), the p-well regions get so close that the active area of the APD is almost fully depleted. Therefore, the p^+/n-well junction will no longer be working and the APD performs like a p-well/n-well diode. The breakdown will now happen at the sides of the p-well as shown in Figure 5-5(c). We have measured the breakdown voltage of a separate p-well/n-well diode, made in CMOS 0.18 μm technology, to be 15.2 V. This confirms that the 5 μm APD operates like a p-well/n-well diode.

5.4.2. Breakdown voltage vs. temperature

The breakdown voltage of the APD varies significantly with temperature. It was shown [5.29] that the breakdown voltage of silicon and other semiconductor APDs at temperature T can be described by

$$V_{BR} = V_{B0}[1+\beta(T-T_0)], \tag{5-1}$$

where V_{B0} is the breakdown voltage at temperature T_0 (typically room temperature), and β is the temperature coefficient of the breakdown voltage. Previous studies

[5.30][5.31] show that the value of β is positive for diodes with avalanche breakdown and negative for diodes with tunneling breakdown. The theoretical derivation of β is presented in [5.32] and the theoretical values of β are compared to measured values for several diodes. A value of 7.2×10^{-4} °C^{-1} for β is predicted in [5.32] for a diode with an avalanche breakdown voltage of about 10.2 V.

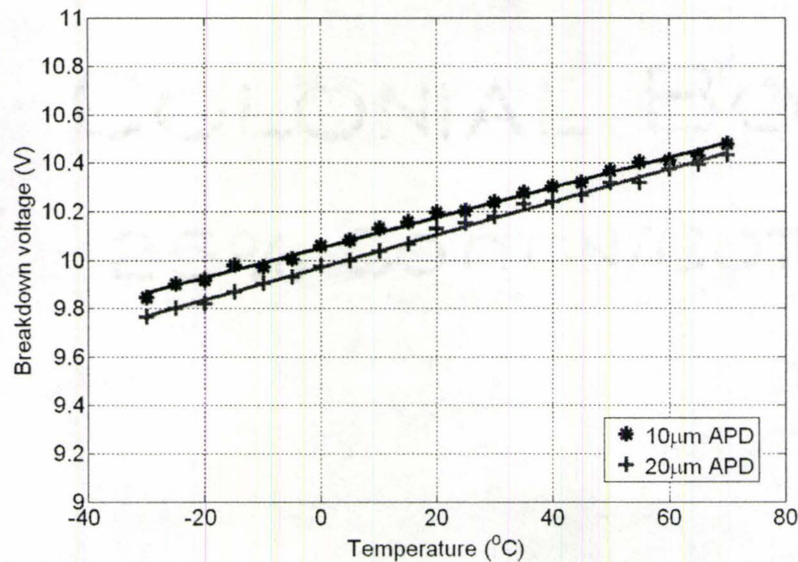


Figure 5-6: Variation of the breakdown voltage of APDs with temperature. The rate of change is approximately 7 mV°C^{-1} that results in $\beta \approx 7 \times 10^{-4}$ °C^{-1}.

Figure 5-6 shows how the measured breakdown voltage of our APDs varies with temperature. A breakdown voltage of 10.2 V is observed at room temperature (20 °C), and a value of $\beta = 7 \times 10^{-4}$ °C^{-1} is extracted for the thermal variation of the breakdown voltage. The positive value of β shows that the breakdown mechanism of our diode is indeed avalanche. The measured β is also in good agreement with the theoretical value [5.32].

A breakdown voltage of 23 V is reported for an APD fabricated in standard 0.35 μm CMOS [5.26]. We have measured a 10 V breakdown voltage for our APD made in 0.18 μm CMOS. Considering this trend, the breakdown voltage of APDs made in CMOS 0.13 μm or smaller, will be low, and the breakdown mechanism will be more likely by tunneling. Thus, it can be expected that standard 0.18 μm or 0.13 μm, may

be the smallest geometry CMOS technology for which an on chip Geiger mode APD fabrication is feasible.

5.4.3. Discussion on breakdown mechanism and microplasma

Previously in this section, we discussed the mechanism of avalanche breakdown in APDs. The APD layout ensures that the maximum electric field happens across the active area of the APD rather than its edges or corners. Impact ionization requires an electric field of at least E_m = 300 kV/cm [5.33]. In a reverse-biased diode, the peak is located at the metallurgic junction. When the reverse bias is just above the breakdown voltage, a narrow strip of high electric filed region around the metallurgic junction performs the impact ionization, rather than the whole depletion region.

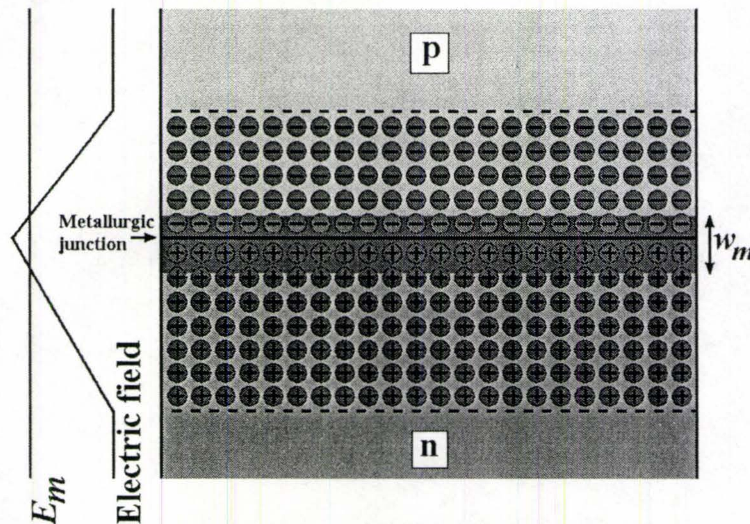


Figure 5-7: Schematic of an abrupt p/n-junction at avalanche breakdown. The width of the depletion region with an electric field high enough for impact ionization, w_m, is only a small fraction of the total width of the junction depletion region.

The high electric field region of Figure 5-7 can be only a few atoms wide. In this narrow region, any device imperfection can cause a local disturbance of the electrical field that can lead to a reduction of the breakdown voltage below the breakdown voltage of the surrounding uniform junction. These tiny spots will be the site of the localized avalanche breakdown of the device. This breakdown condition is generally regarded as being a solid-state analog of a gas discharge plasma, and is called microplasma [5.34]. The microplasma can occur at threading dislocations [5.35],

metal-rich precipitates [5.36], diffusion-induced stacking faults, dopant impurity dislocations [5.37], diffusions voids [5.38] and cracks or mechanical damage [5.39].

At the onset of avalanching, microplasmas switch on and off randomly, producing current pulses of constant height. The microplasma is on for an increasing fraction of the time as the voltage increases until it becomes quiescent. The current carried by microplasma is limited by heating, resistance and space charge effects [5.40].

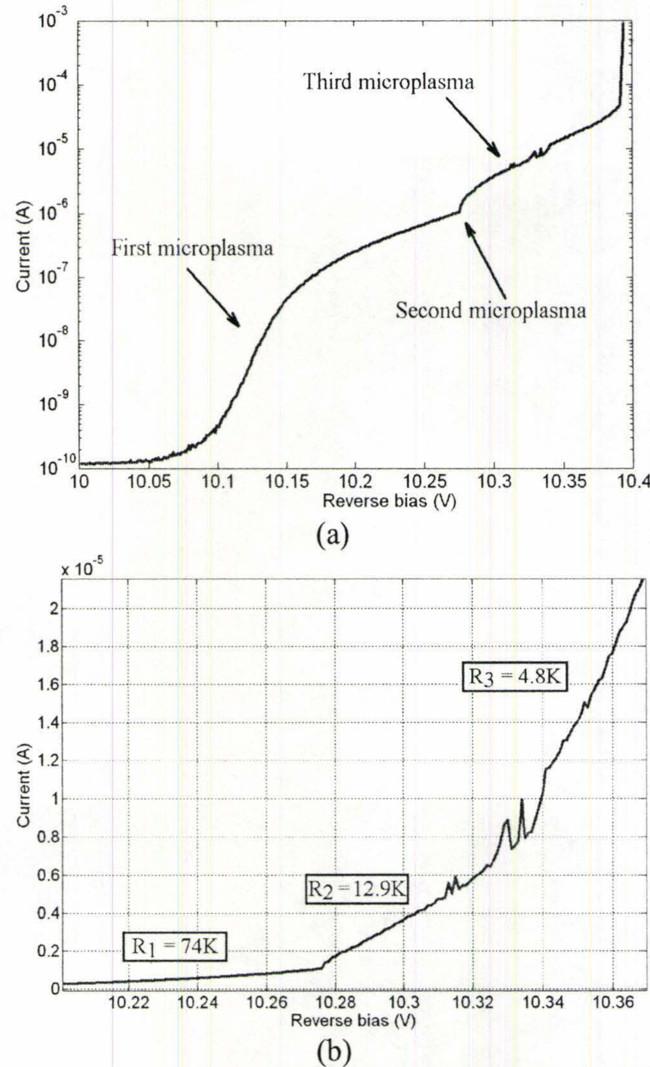


Figure 5-8: (a) Measured *I-V* curve of one of our 10 μm APDs at the onset of breakdown. This region is also known as the multiplication region of the APD, where the current (dark current here) is multiplied by a finite *M*. The curve clearly shows that the current increases in steps, before complete breakdown. (b) A zoomed version of (a) drawn in linear scale. Different sections of the current curve have resistive characteristics. Resistance of each of the microplasma regions are calculated. It can also be clearly seen that the third microplasma turns on and off a few times before being permanently on.

Figure 5-8 shows the mechanism of microplasma regions in one of our APDs. The *I-V* curves are obtained by a semiconductor parameter analyzer, with a 1 kΩ resistor in series with the APD. Figure 5-8(a) shows the *I-V* curve of the APD in semi-log-scale. At about 10.05 V, the avalanche multiplication starts to increase the reverse current of the APD. The increase however, does not sharply continue beyond 10.15 V, as it seems to saturate. This saturation in semi-log-scale is in fact a linear

relationship, or resistive characteristic, meaning that the microplasma tube is acting like a resistance. The resistance is calculated in the linear scale of Figure 5-8(b) to be $R_1 \approx 74\ k\Omega$. At above 10.28 V, a second microplasma tube is turned on. The microplasma tubes will now perform like two resistors in parallel, with the resistance of the second microplasma $R_2 \approx 12.9\ k\Omega$. At around 10.31 V, the third microplasma becomes active. As it was mentioned before, a microplasma tube can turn on and off at the onset of avalanche. This can clearly be seen in Figure 5-8(b). The resistance of the third parallel microplasma is calculated to be around $R_3 \approx 4.8\ k\Omega$. At 10.4 V, so many microplasma tubes are on that the APD can generate currents more than 1 mA.

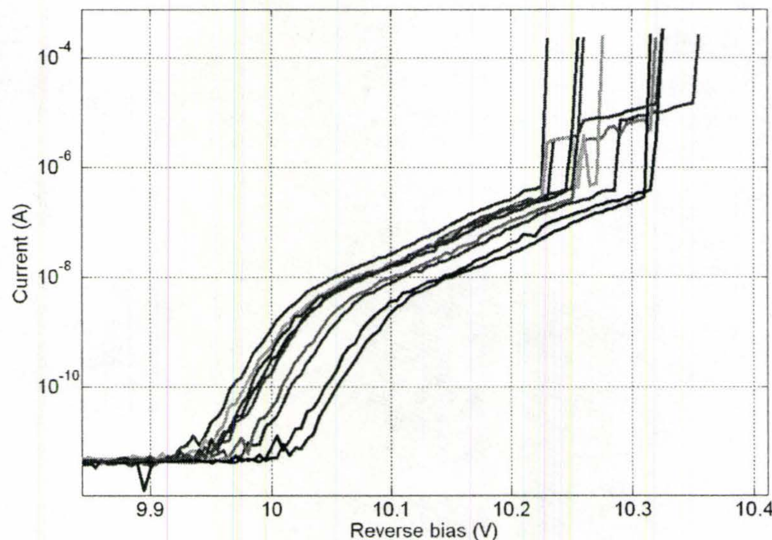


Figure 5-9: Different *I-V* curves obtained for 9 different APDs with the same layout fabricated on different dies in CMOS 0.18 μm technology.

The location of microplasma tubes in an APD active region is random. As a results, APDs that are fabricated with the same layout through the same process can have different onsets for activation of APD breakdown. Figure 5-9 shows several measured *I-V* curves for 9 different APDs fabricated in the same process on different dies. A standard deviation of 29.1 mV is observed in the onset of activation of the fist microplasma of the APDs. A standard deviation of 50 mV is observed for the complete breakdown voltage of the APDs, with a mean around 10.25 V. Also, it can be observed in Figure 5-9 that the microplasmas of different APDs have different activation threshold and characteristics. In Geiger-mode operation of APDs, an

infinite multiplication is desired for every incident photon. It means that several microplasma locations are desired with the onsets of activation as close as possible. In other words, the APDs with the least difference between the onset of first microplasma and onset of infinite gain are desired. In Figure 5-9, the best APD has a difference of less than 0.3 V.

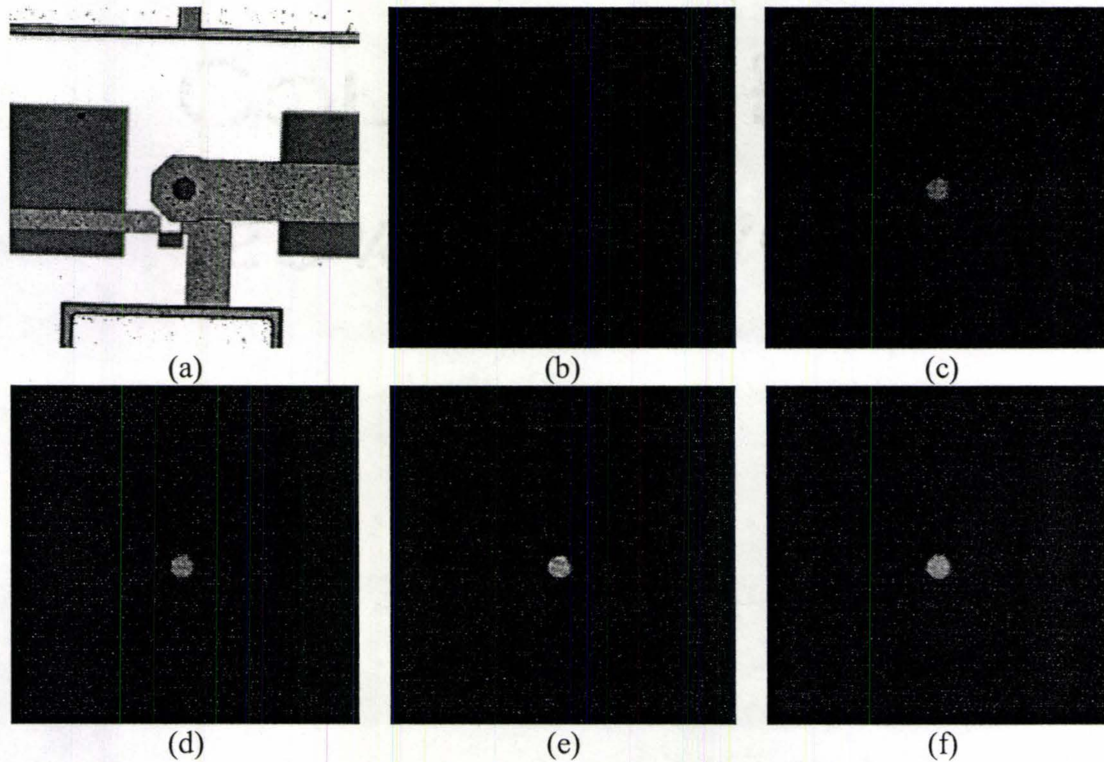


Figure 5-10: Photomicrograph of the APD circuit, with the microscope light on. The circuit consists of a 10 μm APD with a 100 kΩ resistor in series. The APD has a measured 10.2 V breakdown voltage. Photomicrographs taken with the microscope light off, for a reverse bias of (b) 19 V, (c) 20 V, (d) 21 V, (e) 22 V and (f) 23 V.

It is reported that APDs emit light from the microplasma sites during breakdown [5.40]. We have examined this fact by looking at an APD during breakdown in the dark. Figure 5-10(a) shows a photomicrograph of an integrated 10 μm APD in series with a 100 kΩ resistor, with the circuit schematic shown in Figure 5-11(a). Figure 5-10 shows several photos taken from the same spot on the chip at dark. When the applied voltage, V_{DD}, is gradually increased, the APD starts to emit light at 19.3 V. When the applied voltage is decreased from a level higher than 20 V, the APD stops emitting light at 19.1 V. Figure 5-11 also shows the APD voltage, v_S, captured on the

oscilloscope screen. Figure 5-11(b) is taken at 19 V bias, where the APD is working in Geiger-mode. This mode of operation of APD is used for single photon detection and will be descried in detail in Section 5.5. Figure 5-11(c) shows the APD signal at 20 V, where the APD is constantly on, and emits light. The APD current in Figure 5-11(c) is measured to be about 80 μA. When the applied voltage is increased above 20 V, the light emission from the APD increases, as shown in Figure 5-10. The voltage across the APD also increases, from about 10.5 V at 20 V, to about 11.5 V at 23 V. This series resistance in sustaining breakdown condition is know to be R_S, and is considered an effect of space charge, Ohmic drops and local heating [5.41] (which is approximately 50 kΩ in this example).

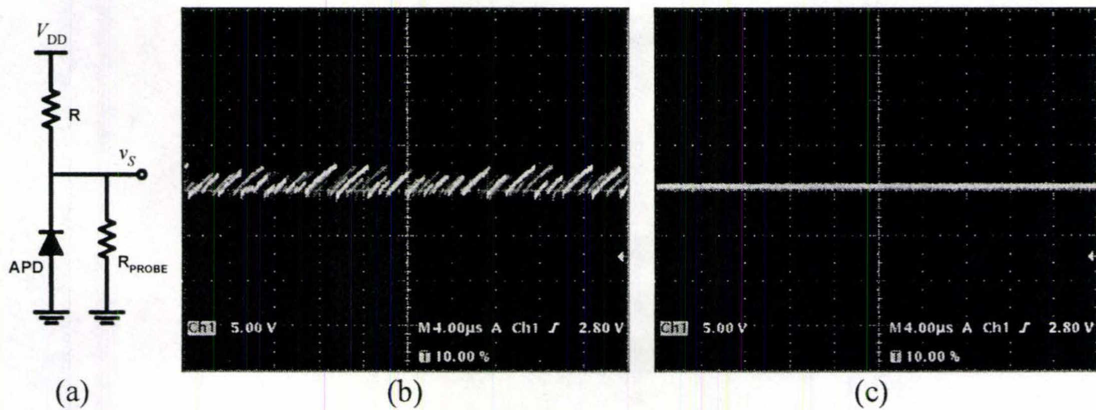


Figure 5-11: The APD circuit (a) and its measured signal, v_S, at (b) 19 V and (c) 20 V applied V_{DD}. The series resistor R = 100 kΩ and the probe resistor R_{PROBE} = 1 MΩ.

The explanation of the observations of Figure 5-10 and Figure 5-11 can be done by a closer look at the *I-V* curve of Figure 5-8(a) which is measured for the same APD. Figure 5-8(a) shows that, although a few microplasma sites can be activated by an applied reverse bias in the range of 10 to 10.4 V, a complete breakdown ($M \rightarrow \infty$) happens at current levels above 80 μA. In the circuit of Figure 5-11(a), the APD current is limited by the large series resistor, R, which is 100 kΩ, in parallel with the oscilloscope probe resistor connected to the sense node, which is 1 MΩ. At applied bias levels below 20 V (Figure 5-11(b)), this resistor limits the breakdown current to levels below 80 μA, where the APD has a finite gain. In this region, the avalanche is not self-sustaining and the microplasma tubes have a short lifetime. At biases above 20 V (Figure 5-11(c)), however, the APD current goes above 80 μA, where the APD

gain is infinite, the avalanche is self sustaining, and the microplasma tubes are constantly on. The large breakdown current that continually passes through the narrow microplasma tubes results in considerable heating of the microplasma regions and light emission from the APD.

5.4.4. Quantum efficiency of Geiger-mode APDs

Calculation of quantum efficiency of APDs is similar to regular photodiodes. However, for Geiger-mode APDs, there is a fundamental difference. In a regular photodiode, if a photogenerated carrier appears in the depletion region of the diode, it will contribute to the photocurrent. In Geiger-mode APD however, a carrier in the depletion region may or may not trigger an avalanche. A brief analytical derivation of the probability of avalanche trigger by an injected carrier follows.

Let's define $P_e(x)$ to be the probability that an electron, injected at distance x from the n^+ edge of depletion region, triggers an avalanche ($P_h(x)$ is similarly defined). Thus, the probability that a pair, at distance x, can trigger an avalanche is given by

$$P_{\text{pair}} = P_e + P_h - P_e P_h . \tag{5-2}$$

Similarly, the probability $P_e(x + \Delta x)$, that an electron starting at position $x + \Delta x$ triggers an avalanche, is given by

$$P_e(x + \Delta x) = P_e(x) + \alpha_e \Delta x P_{\text{pair}}(x) - P_e(x) \alpha_e \Delta x P_{\text{pair}}(x) , \tag{5-3}$$

where α_e is the electron ionization coefficient. Parameters α and β are the ionization coefficient for electrons and holes respectively, defined for the impact ionization as a number of collisions resulting in ionization per unit length traveled by a single carrier though the avalanche region. Impact ionization coefficients depend on electric field [5.42] and are believed to be given by

$$\alpha, \beta = A_{n,p} e^{-B_{n,p}/E} , \tag{5-4}$$

with the parameters defined as

$$A_n = 3.8 \times 10^6 \text{ V/cm},$$

$$A_p = 2.25 \times 10^7 \text{ V/cm},$$

$$B_n = 1.75 \times 10^6 \text{ V/cm, and}$$

$$B_p = 3.26 \times 10^6 \text{ V/cm.}$$

Equations (5-2) and (5-3), and a similar equation to (5-3) for holes, result in the following differential equations:

$$\frac{dP_e}{dx} = (1 - P_e)\alpha_e[P_e + P_h - P_e P_h], \text{ and}$$

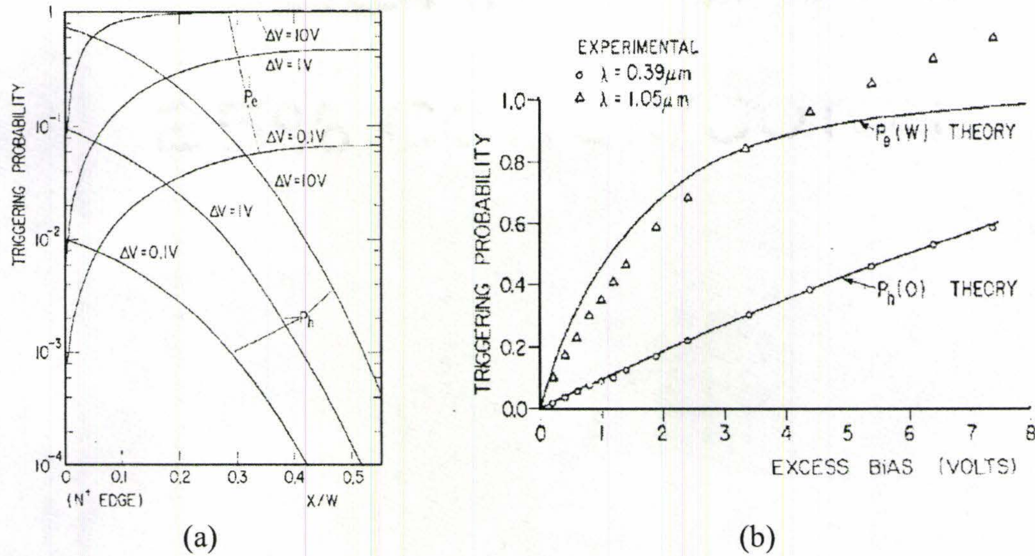
$$\frac{dP_h}{dx} = -(1 - P_h)\alpha_h[P_e + P_h - P_e P_h], \tag{5-5}$$

with the two boundary conditions given by

$$P_e(0) = 0, \text{ and} \tag{5-6}$$

$$P_h(w) = 0. \tag{5-7}$$

The differential equation of (5-5) is solved to give the triggering probabilities that are shown in Figure 5-12.



(a) (b)

Figure 5-12: (a) Triggering probabilities at several excess biases vs. the starting position of the carriers in the APD depletion region. (b) The triggering probabilities for carriers starting as minority carriers at the edge of the depletion region (taken from [5.43], figures 4 and 5).

The measurements of Figure 5-12 are done on a 27 V, n^+/p diode, on a 0.5 Ωcm p-type substrate. Although our APDs are different, it is expected that the same theories apply to the derivation of its triggering probability. We have studied the triggering probability of our APDs by measuring its dark count vs. bias. Dark count is the rate of the avalanche events triggered by an APD at no illumination. At fixed temperature, the flux of carriers into the depletion region of the APD can be assumed constant, and the increase in the dark count of the APD can be assumed to be purely caused by the increase of the triggering probability of avalanche by a single carrier. Figure 5-13 shows the measured dark count of our APD vs. the applied excess bias. It also shows a fitted curve to the measurement points. It shows a relatively linear variation, which is in good agreement with the prediction of Figure 5-12(b). A more complete study of the dark count will be presented in the next section.

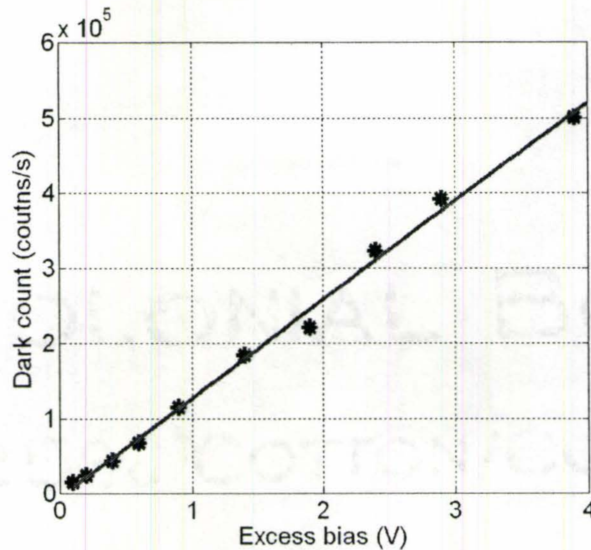


Figure 5-13: Dark count of our 10 μm APD, at room temperature, for different values of excess bias. The dark count varies linearly for small values of excess bias and it is in good agreement with the theoretical prediction of Figure 5-12 shown with the solid line.

5.5. Comparison

In the previous sections, we presented an overview of the APDs that are reported in the literature, and we also introduced and characterized our APD device. Now we can compare our device to the previous implementations of APD. Table 5-1 shows different parameters of these APDs. Our APD has the lowest breakdown voltage, and as a result, it consumes less power and it is easier to be implemented in miniaturized systems. However, our APD suffers from high dark rate, as we will discuss it in detail in the next section.

Table 5-1: Comparison of some of the reported APD implementations in CMOS with our APD. Note that the 50 kHz dark count for our APD in this table is for the worst case according to Figure 5-13.

	Technology (μm)	Breakdown voltage (V)	Diameter (μm)	Peak PDP (%)	Dark current / count
[5.22]	1.5	30	20	-	33 pA
[5.23]	0.8	19	800	-	200 pA
[5.24]	0.8	26.8	5	-	100 Hz
[5.25]	0.8	16	12	45	40 kHz
[5.26]	0.35	23	6	5	6 Hz
Our	0.18	10	10	5.5	50 kHz

5.6. Geiger-mode passive APD

Avalanche photodiode is the semiconductor equivalent of photomultiplier tube [5.10]. The APD is a photodiode that its breakdown mechanism is avalanche and it can operate in two modes. In the first mode, the APD is reverse-biased slightly below its breakdown voltage. The high internal electric field at such bias conditions results in impact ionization of accelerated carriers in the depletion region with the lattice atoms. Each carrier that is injected in the electric field will then be multiplied, resulting in a gain. This internal gain is used in APDs to amplify the small photocurrents generated by low-levels of incident light.

The second mode of operation of APDs is called Geiger mode. In this mode, the APD is reverse-biased above its breakdown voltage. A single carrier in this mode is enough to trigger a sustaining avalanche current. This current should be detected and quenched by external circuitry. There are passive and active circuits that perform this task. In this section, we will focus on the passive approach. In section 5.7, APD with active circuitry will be discussed.

5.6.1. Resistor vs. active load

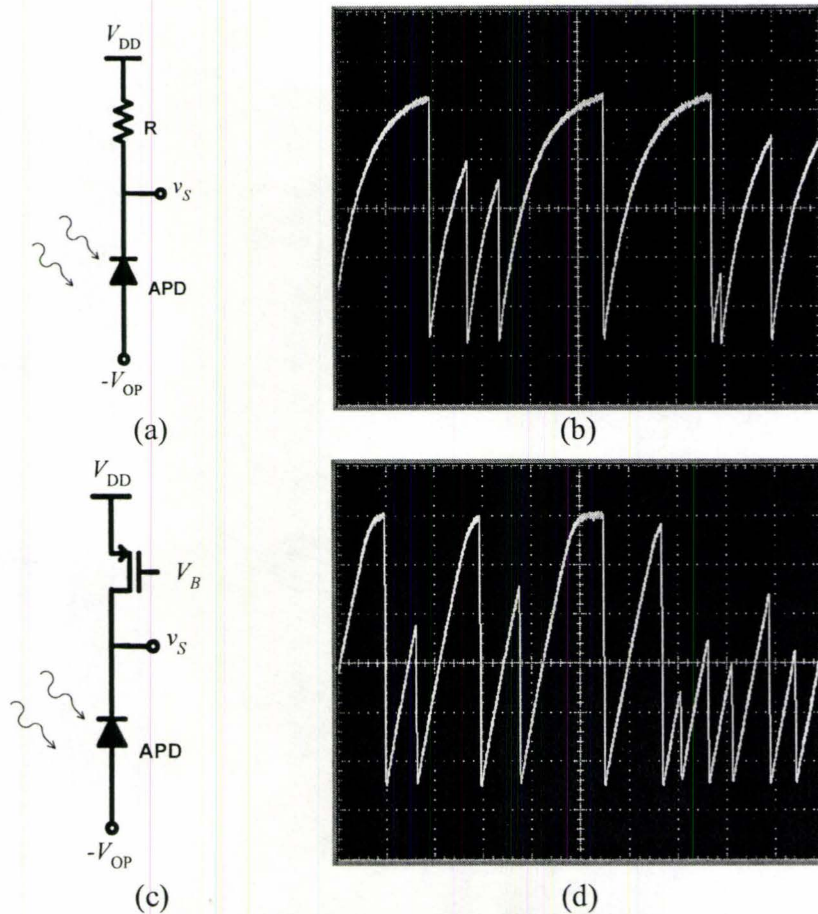


Figure 5-14: Geiger-mode of operation of APD. (a) Schematic of a passive APD circuit and (b) its measured sense node voltage vs. time. Each drop corresponds to a photon arriving at a random time. (c) Schematic of an APD in series with an active load and (d) its measured sense node voltage. The active load is a PMOS transistor with W/L = 10 × 9 / 0.3. The voltage scale in both (b) and (d) is 100 mV, and the time scale is 20 μs for (b) and 2 μs for (d).

Figure 5-14(a) shows the circuit that operates the APD in Geiger mode. It consists of an APD in series with a large resistor (100 kΩ in our design). The total reverse-bias applied to the APD in this circuit, V_{DD}, is above the breakdown voltage (V_{BR}) of APD. When an electron-hole pair is generated in the depletion region of the APD, caused by an incident photon or thermal generation, it triggers the avalanche process, and results in a large current to flow across the APD. The breakdown current passes through the external resistor and brings the sense node voltage, v_S, down. As a result, the bias across the APD drops and eventually becomes less than V_{BR}, terminating the breakdown process. This is called passive quenching, and its process can be better

observed in Figure 5-14(b). Each sharp drop in the sense node voltage of Figure 5-14(b) corresponds to an incident photon (or thermal generation). After the breakdown is quenched, the sense node recharges towards V_{DD} with an RC time constant, C being the junction capacitance of the APD in parallel with parasitic capacitances of the pads, wirings and probe.

In the design of CMOS integrated circuits, transistors are preferred to resistors. We have also implemented and measured an APD in series with an active load instead of a resistor, as shown in Figure 5-14(c). By properly biasing the gate of the transistor, the circuit can be operated in Geiger-mode at the desired recharge speed Figure 5-14(d) shows the measured v_S obtained for the circuit of Figure 5-14(c). The difference between an RC recharge and an active load recharge can be seen by comparing Figure 5-14(b) and Figure 5-14(d). The active load can be a good replacement of a resistor in a Geiger-mode APD circuit considering its smaller layout area, and also the possibility of adjusting its recharge speed by changing the bias voltage of the transistor.

5.6.2. Dark count

It was mentioned earlier that an avalanche event can be triggered by either an incident photon, or a thermally generated electron-hole pair. The number of pulses per second that are generated by an APD in the absence of light is called dark count. Dark count sets the lower limit on the number of photons that can be detected per second. This is why APDs are cooled for low-light-level detection applications. The variation of the dark current of an APD with temperature follows the Meyer-Neldel law:

$$I_D = I_0 e^{-E_A / kT}, \tag{5-8}$$

where E_A is the activation energy. Studying the activation energy can provide insight into the sources of the dark count. For diodes in which the origin of dark carriers is pure thermal generation, the activation energy is normally approximately equal to half of the energy band gap of the material. However, in diodes with a narrow depletion region, a dark carrier can be generated after tunneling into a mid-gap trap state. In the

diodes in which the generation of dark carriers is assisted by tunneling, the activation energy becomes smaller [5.44].

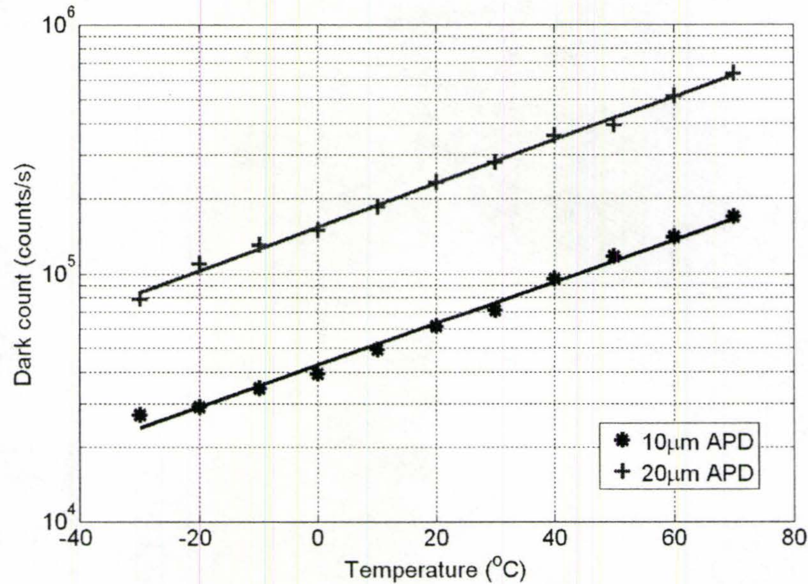


Figure 5-15: Dark count vs. temperature for an excess bias of 0.5 V. The dark count doubles approximately every 30 °C. Note that to extract the activation energy reported, we plotted $\ln(I_D)$ versus the inverse of the Absolute Temperature.

The measured dark counts of our 10 μm and 20 μm APDs are shown in Figure 5-15. The variation of the dark count with temperature is measured for a fixed V_E of 0.5 V. The figure indicates that the dark count increases exponentially with temperature. The activation energy of the diode is ~0.2 eV, which shows the dominance of the tunneling-assisted generation of the dark carriers. Note that this activation energy E_A was obtained from a plot of $\ln(I_D)$ against the inverse of the absolute temperature that is shown in Figure 5-16, according to (5-8). Also, our APD's dark count is relatively higher than the dark counts at 40 kHz reported in [5.25] or less than 1 kHz reported in [5.24] because of its lower breakdown voltage. The high doping concentration levels of 0.18 μm CMOS cause a narrow depletion region, resulting in significant tunneling-induced dark carriers and increased dark count.

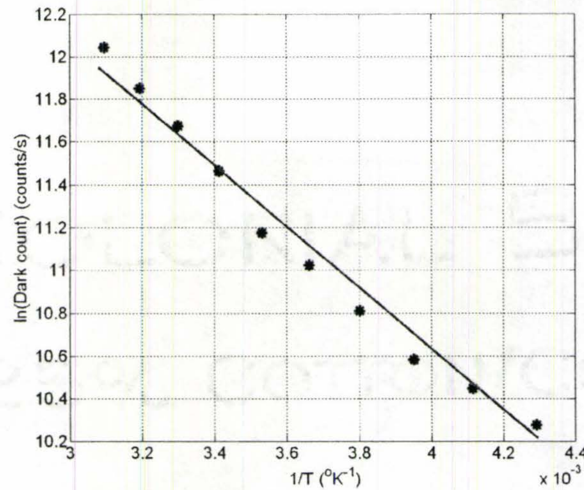
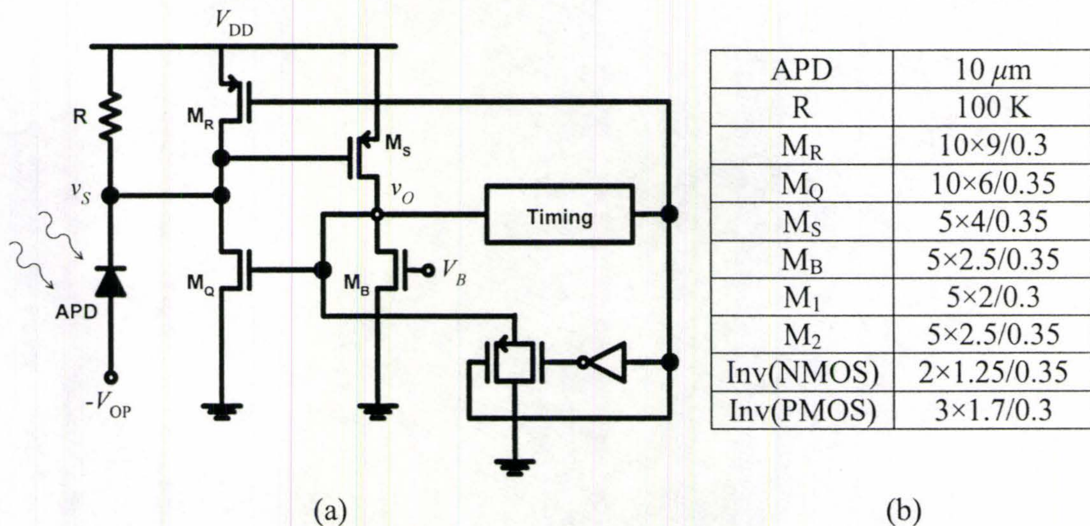


Figure 5-16: plot of $\ln(I_D)$ against the inverse of the absolute temperature used for extracting the activation energy.

5.7. Geiger-mode APD with active peripheral circuitry

5.7.1. Basics of peripheral circuitry: Schematic and layout



APD	10 μm
R	100 K
M_R	10×9/0.3
M_Q	10×6/0.35
M_S	5×4/0.35
M_B	5×2.5/0.35
M_1	5×2/0.3
M_2	5×2.5/0.35
Inv(NMOS)	2×1.25/0.35
Inv(PMOS)	3×1.7/0.3

(a) (b)

Figure 5-17: (a) Schematic of the APD circuit with active quench and active reset and (b) diameter of the APD, size of the resistor in ohm, and W/L of the transistors of the circuit in micron. The timing block consists of two mono-stables in series. Each mono-stable has a bias input that adjusts the width of the output pulse. The first mono-stable causes a delay, and second mono-stable dictates the width of the output of the timing block.

Figure 5-17 shows the schematic of APD and its associated peripheral circuits for operation in Geiger mode. When no current flows in the APD, its reverse bias is equal

to (V_{DD} + V_{OP}). This voltage is above the APD's breakdown voltage V_{BR}. Several terms have been used in the literature for the difference between these voltage levels such as: over-voltage, excess voltage and excess bias. We will use the term excess bias in this work. The value of the excess bias, V_E, is then given by

$$V_E = V_{DD} + V_{OP} - V_{BR}. \tag{5-9}$$

An electron-hole pair can be generated in the depletion region of the APD, either by an incident photon or thermal generation. The electron and hole will then accelerate in opposite directions in the high electric field. They will collide with the lattice atoms, and release other carriers to start the avalanche process. This avalanche current builds up very fast. The current will flow in the quench resistor R, and cause the voltage at the sense node, v_S, to decrease. The quenching loop sense transistor, M_S, will sense this drop, and immediately turn on the quench transistor, M_Q, to quickly bring v_S down to zero. Now, the reverse bias applied to the APD is down to V_{OP}, which is less than V_{BR}. The avalanche process will stop and the current in the APD will immediately dissipate. The action performed by M_Q is called active quenching, and it causes the duration of the avalanche current flow in the APD to be short.

The sense node voltage is kept at zero for a hold-off time, in order to reduce the probability that a subsequent after-pulse is triggered by the release of a trapped carrier. The hold-off time is controlled by a mono-stable in the timing block. At the end of the hold-off time, M_Q will be turned off and the reset transistor M_R will be turned on. Transistor M_R will bring v_S back to V_{DD} to make the APD ready for the next incoming photon. This is called active reset, and its duration is controlled by a second mono-stable in the timing block. At the end of reset time, M_R is turned off and APD is ready to detect another photon.

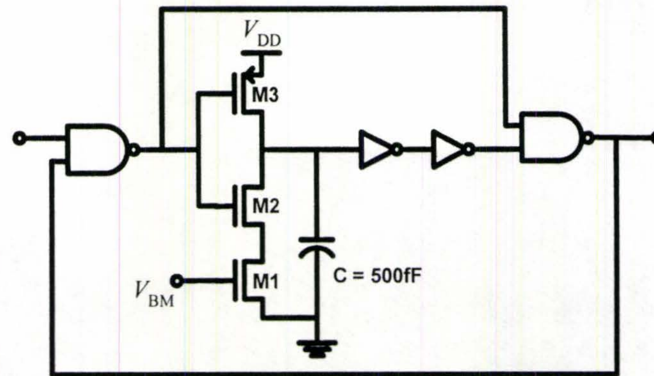


Figure 5-18: The schematic of the mono-stable circuit used in the APD periphery. M1 and M2 have W/L of 5/0.35, and M3 has W/L of 4 × 2.5/0.3. The mono-stable is triggered by the falling edge of the input, and it generates a low level output pulse with the width that is adjusted by the V_{BM} input.

The timing block in Figure 5-17, consists of two mono-stables. The first one controls the quench time of the APD, and simply causes a delay between the time it senses the input, and the time that it activates M_R. The second mono-stable controls the reset time, which is the duration of the output pulse that keeps M_R on. Both mono-stables have a 500 fF internal capacitor, and bias inputs that control the output pulse duration. Figure 5-18 shows a simplified schematic of the mono-stable circuit used in this work [5.45]. Input V_{BM} is used to adjust the width of the output pulse of the mono-stable.

We have also fabricated the full circuit of Figure 5-17, and a photomicrograph of its layout is shown in Figure 5-19. Thick-oxide transistors are used so that 3 V for V_{DD} can be used instead of the 1.8 V that is typical of 0.18 μm CMOS technology. This higher V_{DD} will ensure that enough excess bias is applied to the APD when turned on, and that enough margin exists between V_{OP} and V_{BR}. The APD can be displaced with respect to the peripheral circuit, to achieve a total pixel area of about 90 μm × 100 μm. Most of this area is taken by the capacitors of the mono-stables. The pixel reported in [5.10], which is a simple passive quenched APD with an inverter and a buffer, has a 1.1 % fill-factor. Our pixel, with active quench and active reset circuits, has the same fill-factor. This has become possible by using a smaller scale CMOS technology.

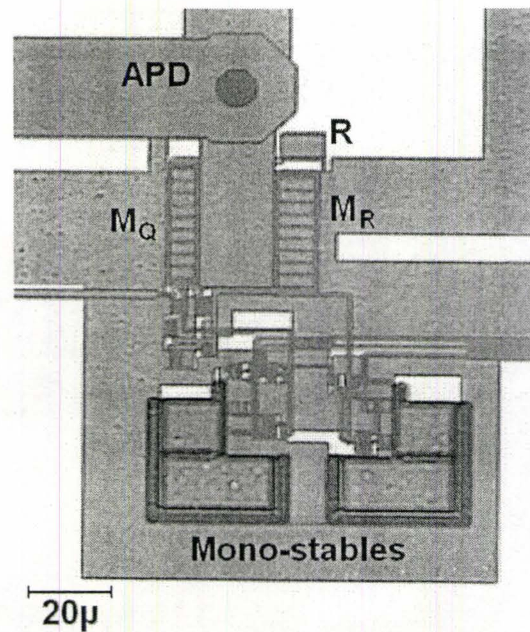


Figure 5-19: Photomicrograph of the layout of the APD with the peripheral circuits. A large part of the layout area is taken by the capacitors, which are seen as the two L-shaped features at the bottom of the Photomicrograph.

5.7.2. Analytic derivation of APD system output

We have measured the performance of the APD with active reset and quench circuits. The dead time of an APD circuit is the time during which the APD cannot sense any incoming photon. It is the duration of the output pulse of the circuit that corresponds to a single incident photon (or thermally generated electron-hole pair). The dead time sets the upper limit on the number of photons that can be detected per second.

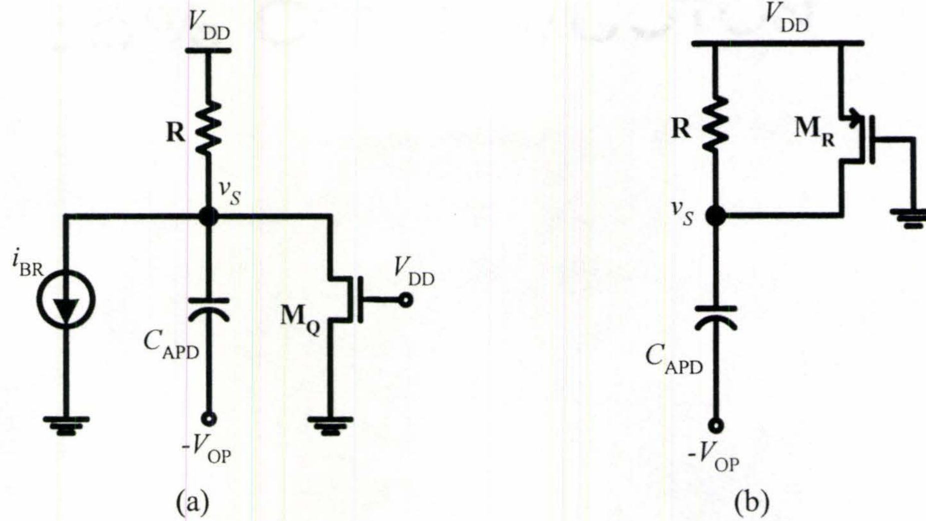


Figure 5-20: Equivalent circuits used for analytical derivation of the sense node voltage during (a) active quench and (b) active reset.

The dead time of an APD circuit can be analytically derived. Most of the dead time is taken by the active quench and active reset periods. When the avalanche process begins, and the sense node voltage decreases by one threshold voltage of M_S, then the active quench loop turns on the quench transistor. Figure 5-20(a) shows the approximate equivalent circuit during active quench. During this period, transistor M_Q brings v_S down to zero. The relation governing the sense node voltage will then be

$$\frac{V_{DD} - v_S(t)}{R} = C_{APD}\frac{dv_S}{dt} + i_{BR} + \mu_N C_{ox}\frac{W_Q}{L_Q}\left[(V_{DD} - V_{TN})v_S(t) - \frac{v_S(t)^2}{2}\right], \qquad (5\text{-}10)$$

with initial condition $v_S = V_{DD} - V_{TP}$. In equation (5-10), W_Q and L_Q are width and length of transistor M_Q and V_{TN} is its threshold voltage. In our design, $W_Q/L_Q = 170$. The breakdown current of the APD is i_{BR} and C_{APD} is the capacitance of the APD measured to be 200 fF for the 10 μm APD at a reverse bias close to 10 V. At the beginning of reset, the sense node voltage and the APD current are both zero. Transistor M_Q is turned off and M_R is turned on. Figure 5-20(b) shows the circuit during reset. The equation governing the sense node voltage will then be

$$\frac{V_{\mathrm{DD}} - v_S(t)}{R} + \mu_P C_{\mathrm{ox}} \frac{W_R}{L_R}\left[(V_{\mathrm{DD}} - V_{\mathrm{TP}})[V_{\mathrm{DD}} - v_S(t)] - \frac{1}{2}[V_{\mathrm{DD}} - v_S(t)]^2\right] = C_{\mathrm{APD}} \frac{dv_S}{dt}, \tag{5-11}$$

with initial value $v_S = 0$ V. In equation (5-11), W_R and L_R are width and length of transistor M_R and V_{TP} is its threshold voltage. In our design, $W_R/L_R = 300$. For a period of time at the beginning of reset, transistor M_R is in saturation. However, this time is very short as the sense node voltage will increase very fast and push transistor M_Q into the linear regime of operation. Therefore, equation (5-11) is a good approximation for the whole reset period.

5.7.3. Measurement of APD system output

The output of the circuit of Figure 5-17 has been measured to evaluate the response of the APD and peripheral circuits to incident photons. The output pad and measurement probes are connected to the node v_O in Figure 5-17 to avoid loading the small capacitance of the sense node. Figure 5-21 shows the variation of the sense node voltage of our circuit as a function of time.

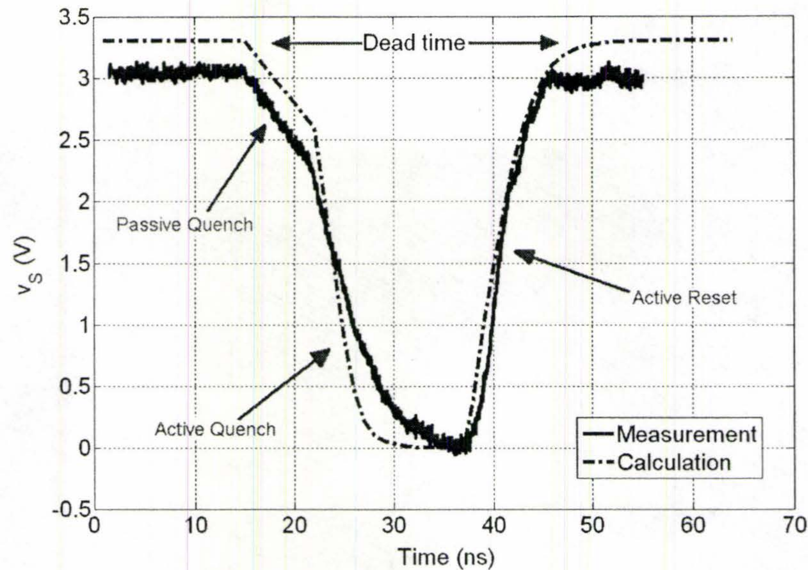


Figure 5-21: Measured and simulated sense node voltage of the APD circuit. The dead time is about 30 ns.

Since the start of avalanche in the APD, v_S will start to drop with passive quenching. It takes about 7 ns for v_S to reach a level that turns on the quench loop. Figure 5-21 also shows a quench time of about 15 ns and a reset time of about 8 ns. The times for active quench and active reset can be adjusted using the mono-stables of the timing block. These delays add to an overall dead time of about 30 ns. Previous implementations of APDs in CMOS have reported dead times of 60 ns [5.25] and 40 ns [5.10], [5.26]. These times are primarily affected by the capacitance of the APD including the capacitance of the guard ring, the size of the reset and quench transistors, and how well they can source or sink current. Figure 5-21 also shows the calculated v_S using equations (5-10) and (5-11), which is in good agreement with the measured results.

5.7.4. Measurements of photo-response and spectral response

Finally, the sensitivity and spectral response of our APD is investigated. The probability of detection of a photon (PDP) indicates the percentage of incoming photons that trigger a pulse in the output of the APD circuit. The PDP is measured by evaluating the number of photons incident on the APD, and counting the number of pulses in its output. The rate of the incoming photons is evaluated based on the power of the incident light at a certain wavelength. The number of pulses generated by the

APD is measured in a fixed time interval several times and then averaged. Measurements are done using a stable wide-spectrum Xenon lamp, connected to an integrating sphere through band-pass filters and attenuators to adjust the wavelength and flux of the incident photons on the APD. Measurements are performed on a vibration isolation optical table. Measurements are repeated in dark, and the dark count is subtracted from the count of the output pulses of the APD at each measurement point. Figure 5-22 shows the measured PDP as a function of the wavelength of the incoming light, at different levels of V_E for the 10 μm APD.

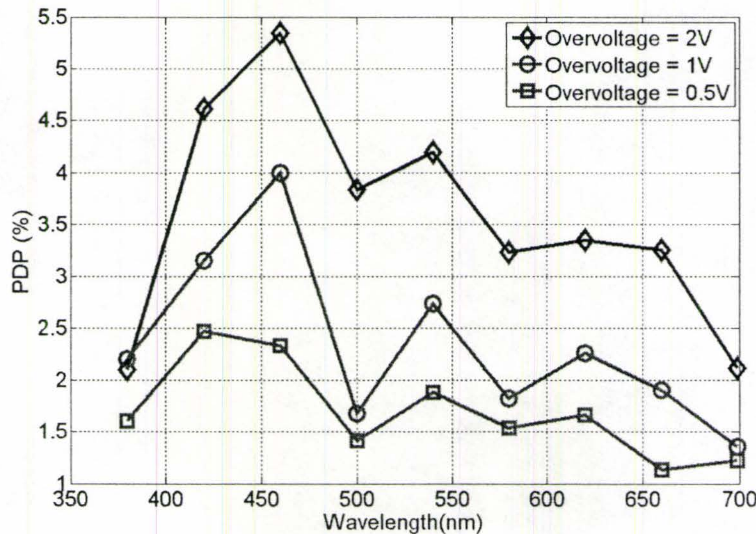


Figure 5-22: Probability of detection of photons for different wavelengths. Increasing the excess bias will increase the probability of detection. Oscillations in the curves are due to the several dielectric layers of CMOS on top of the APD.

The width of the depletion region and the strength of the electric field increase in an APD by applying higher V_E. This will make it easier for an electron-hole pair to start the avalanche breakdown. This is why the PDP increases with V_E, as shown in Figure 5-22. However, increasing V_E, will also increase the dark count and noise of the APD. Also, in practice, when the APD is implemented in CMOS along with the active quench and reset circuits, V_E cannot be greater than V_{DD}. This is according to (5-9) and the fact that $V_{OP} < V_{BR}$. Our APD shows a maximum PDP of about 5.5 % for a V_E of 2 V. The PDP will improve with increasing excess bias, as reported in some previous publications. For example, in [5.26], a peak PDP of 5 % for a V_E of 3 V was reported. In [5.10], the PDP was in 20 % range for a V_E of 5 V, and in [5.25], the peak

PDP was 45 % for a V_E of 10 V. Note that the PDP can be further improved in our device by removing the passivation layer from the surface of the chip.

PDP also varies with wavelength. The active region of the APD is a p+/n-well diode, which is very shallow in 0.18 μm technology. As a result, in longer wavelengths, many of the absorbed photons generate carriers that will recombine before reaching the active region. On the other hand, photons with very short wavelength will be absorbed too close to the silicon dioxide interface to be detected. This is why the PDP in Figure 5-22 decreases for shorter and longer wavelengths. The oscillations that are observed in the PDP of Figure 5-22 are due to the effect of several narrow layers of the silicon dioxide that are deposited on top of the silicon.

Chapter 6

CONCLUSIONS AND RECOMMENDATIONS

6.1. Conclusions

CMOS photodetectors have been considered in this work for low-light-level applications. Several biomedical applications are introduced, like DNA microarrays and camera pill, that require an integrated imaging system that is able to detect very low levels of light. Some of the current photodetectors and imaging systems, like photomultiplier tubes and charge-coupled devices, are introduced. Advantages and disadvantages of these imagers are described in contrast to integrated imaging systems in CMOS technology.

CMOS circuits are low power, cheap, and highly integrated. It is however difficult to achieve high quality photodetection in CMOS, as the technology is not optimized for imaging. It is highly desired to have photodetectors in CMOS that can detect low levels of light. In this thesis we have introduced the challenges in making CMOS imaging systems. The effect of scaling is also described in Chapter 1. The rest of thesis introduces several CMOS pixel structures and imaging systems.

Active pixel sensor is the most commonly used CMOS pixel structure. A comprehensive review of current APS structures, and their variations have been presented in Chapters 2 and 3. Three transistor APS is the pixel structure that is used in most of the APS imaging systems. Signal and noise of this pixel structure has been comprehensively analyzed in this thesis in Chapter 2. We have reported the maximum

SNR of a conventional APS pixel, which is a function of the photodiode capacitance and source voltage. A new model for the capacitance of the photodiode is proposed. This model results in very accurate prediction of the APS signal. The model is verified by measurements on an APS fabricated in 0.18 μm standard CMOS technology.

Different variations of APS are fabricated, measured and compared in this work. Chapter 3 introduces APS structures with in-pixel comparator, in-pixel integrator, multisampling time-domain pixel, and lateral BJT structure. Out compact design for the APS with comparator offers a 2.2 V sense node voltage swing, with a fill-factor of 36%. The APS with integrator achieves the excellent dark output drop rate of 16 mV/s. The multisampling APS structure offers high resolution imaging at high bit-rates due to its parallel internal ADC mechanism. The lateral BJT structure has high responsivity, as it can have internal gain of more than 10^3.

Also, measurements and calculations of Chapter 4 on our fabricated APS suggest that it can be operated in a different mode (DC level output) to get better low-light-level sensitivity. Noise of the DC level of APS has been analyzed in this work for the first time. While conventional APS normally detects light levels down to 1 μW/cm^2, The DC level can detect light powers in the order of 10 n W/cm^2. At 1 μW/cm^2, The DC level output has a 25 dB SNR, which is 10 dB above the best conventional APS. The DC level mode preserves the simple APS structure, it does not need CDS, and the reset time and reset transistor sizes can be adjusted to optimize its sensitivity. However, the DC level mode of operation responds slower to the temporal changes of the incident light power, as it might need several integration and reset cycles to converge.

Active pixel sensors, and all its variations, are integrating devices. They integrate the photocurrent during a fixed integration time before generating the output voltage that is proportional to the incident light level. This integration time should be shorter for high-speed applications, and it should be longer for high-sensitivity applications. As a result, APS or its variations are not applicable to many biomedical applications that require both sensitivity and speed. Fluorescence lifetime imaging for example,

requires detection of emissions in cellular level that decay with nanosecond time constants. Photomultiplier tubes are used in these applications. PMTs are excellent choices that are sensitive and fast. However, they are fragile and bulky, and cannot be integrated. Avalanche photodiodes are semiconductor equivalent of PMTs that are considered in Chapter 5.

In this work, several single photon APDs, along with their peripheral circuitry, are integrated in standard 0.18 μm CMOS technology. Octagonal APDs with 5 μm, 10 μm and 20 μm diameter active region have been fabricated. The 10 μm and 20 μm APDs exhibit good avalanche breakdown characteristics with a breakdown voltage of 10.2 V. Temperature variation of the APDs confirm the avalanche mechanism of breakdown. We expect that it will not be possible to make APDs with much smaller scale CMOS technologies, as the breakdown mechanism will switch to tunneling. The microplasma effect is examined for our APDs to further investigate its breakdown mechanism. Microplasma emission has been observed for our APDs above 20 V reverse bias, which is the upper limit for operation of the APD in Geiger mode.

On-chip passive and active circuits for Geiger mode operation of APDs have been fabricated and measured in Chapter 5. Active quench and reset circuits have been successfully implemented and measured. Our integrated APD and peripheral circuits had a measured dead time of about 30 ns and a PDP of about 5.5% at an excess bias of 2 V –results that are comparable or better than the best published results to date. Fabrication of APDs in 0.18 μm technology improves the fill factor and increases the speed of the pixel. There is also a limit on how small the APD can be made when a standard CMOS technology is used. This is because of the interference of the depletion region of the guard ring with the APD effective sensing area.

The proposed CMOS photodetectors and imaging systems of this work can be used in a wide range of applications. The DC level APS can be used in applications like the camera pill, where low levels of light have to be measured at a relatively low frame rate. If higher frame rates are desired, then the APS with a comparator can be used. The APS with an integrator can be used in DNA microarray applications due to its dark current cancellation ability, and the fact that high spatial resolution is not

needed. Finally, for fast and high sensitivity applications such as like fluorescence lifetime imaging, the fully integrated 2D-APD array system can be used.

6.2. Recommendations

Several areas of the research that have been done during this PhD work can be continued and expanded. Also, new solutions can be proposed for several applications that have been considered in this work. These variations can range from simply changing some of the proposed pixel structures, to seeking solutions in different fabrication technologies. Following are some recommendations for possible future research that are related to this work.

Several solutions that are proposed in this work can be further improved. In the following paragraphs, improvements in resolution, sensitivity and speed will be discussed in the framework of the circuits that are proposed in this work. Then, new possible photodetector solutions in CMOS will be discussed. Finally, application of other CMOS technologies, or non-CMOS solutions will be considered that can expand the applications of the proposed imaging systems.

Most of the low-light-level applications that were considered in this work did not require high spatial resolution. This is an important fact in the trade-off between resolution and sensitivity. In many applications, like consumer photography, high resolution is greatly desired. In order to improve the resolution of the pixel structures that are proposed in this work, the photodiode size can be decreased, and instead, microlenses can be implanted on the array. Some of the in-pixel circuits can also be shared among blocks of several pixels to decrease the average pixel size.

Although sensitivity has been the main focus of this work, most of the solutions that were introduced were at the functional level, or circuit level. The quantum efficiency of the detectors in general can be improved by removing the thin, opaque passivation layer that is deposited on the CMOS circuit at the end of the process. Microlenses can improve the fill-factor of the pixel. Layered color detection schemes, instead of color filter arrays, also improve the overall quantum efficiency.

The speed/sensitivity trade-off was well discussed in this work. It was said in general, that APS solutions, including the DC level, can not offer both high speed, and high sensitivity, and APDs are the only solution for such applications. There are however, approaches to improve the speed of APS pixels. Global shutters are used in high speed applications, both for CCD and CMOS imagers where the level of incident light is relatively high. Frequency response, and parasitic capacitances of the peripheral circuits can also be considered and analyzed for obtaining optimum speed. The speed of the APD can also be improved by decreasing the parasitic capacitance of the guard ring that is parallel to the APD capacitance. The dead-time of the active APD circuit can also be improved by decreasing the series resistor and increasing the W/L of the reset and quench transistors, and choosing faster mono-stable circuits.

It is possible to expand some of the solutions that are proposed in this work. First, the design parameters of an APS can be optimized to achieve maximum sensitivity in DC level mode of operation. Second, a high-resolution array of DC level mode APS can be fabricated with on-chip row and column control circuitry for high-resolution low-light-level applications like DNA microarrays. Third, an accurate model for APDs can be developed (which is currently missing in the literature) that is applicable to GM-APD circuits. Fourth, layout of the CMOS GM-APD and its peripheral circuits can be optimized to achieve response times of 1 ns or less.

There are other photodetector structures or imaging systems that can be implemented in CMOS. Photogate structures and transfer gates can be implemented for on-chip correlated double sampling. Multi-layer photodiodes can be used for filter-free color detection that also optimizes the photosensitivity. Phototransistors can be used instead of photodiodes because they have better responsivity due to internal amplification.

Although the implementations of this work are in CMOS 0.18 μm, other CMOS technologies have also been discussed in several places in this thesis. We have considered the effect of downscaling on photodetection, and also predicted the performance of APDs fabricated in smaller scale CMOS. The implementations of this work however, have all been in CMOS 0.18 μm. It is desired to implement several devices, with the exact same layout, in several different CMOS technologies and

measure the actual difference. In particular, the possibility of successful implementation of APDs in 0.13 μm and smaller-scale CMOS technologies can be verified. BiCMOS technology can also be considered, due to some excellent light detection performances of bipolar phototransistors. Non-CMOS technologies can also be considered to compare the spectral response of the detectors, and to achieve better light detection in deep UV, or infrared.

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APPENDIX A

```
%Signal-to-noise ratio of APS vs. integration time, considering our
model for the capacitance of the photodiode

clc; clear;

K = 1.38 * 10^-23;
T = 300;
q = 1.6 * 10^-19;
idc = 2.28 * 10^-15;
iph = 50 * 10^-15;
Cph = 22 * 10^-15;
V0 = 2.1;
Phi = 0.7;
A = (3 * 10^-4)^2; AlphaH = 2 * 10^-3; mu = 1350; x = 1 * 10^-4;
N = iph * x / (q * mu * Phi * A);
K1 = AlphaH / N;
Vd = 2.5;
Vt = 0.0259;

cB = 1; cE = 150;
DeltaT = 10^-2;

for  c = cB : cE
    tint(c) = c * DeltaT;
    %Calculation of noise
    Vnres2(c) = 0 * K * T / (2 * Cph);
    Vnsh2(c) = q * (iph + idc) * tint(c) / Cph^2;
    Vn1f(c) = (K1 * (iph + idc)^2 / (4 * pi^2 * Cph^2)) * tint(c)^2;
    Vn(c) = (1 * Vnres2(c) + 1 * Vnsh2(c) + 1 * Vn1f(c))^0.5;

    %Calculation of signal

    %Simple models
    %Vs(c) = (iph / Cph(c)) * tint;
    %Vsat = V0 + Vt * log (idc / (iph + idc));
    %Vs(c) = ((iph/Cph(c)) * tint * Vsat) / (Vsat + (iph/Cph(c)) *
tint);
    %Vs(c) = V0 - Vt * log( (idc / (iph + idc)) - ((idc / (iph +
idc)) - exp(V0 / Vt)) * exp(-tint(c) * (idc + iph) / (Vt * Cph)) );

    %Our model with saturation
    if c == 1
        Vss(c) = V0;
    else
        Vss(c) = Vss(c - 1) + DeltaT * (-iph + idc * (exp(-Vss(c -
1)/Vt) - 1)) / (Cph * ((V0 + Phi)/(Vss(c - 1) + Phi))^(1/4));
    end
    Vs(c) = V0 - Vss(c);

    %Vt = ( (V0 + Phi)^1.5 - 3 * (iph + idc) * (V0 + Phi)^0.5 *
tint(c) / (2 * Cph) )^(2/3) - Phi;
    %Vs2(c) =  V0 - Vt;
    %Vs3(c) = Vs(c) - iph^2 * tint(c)^2 / (4 * Cph^2 * (V0 + Phi));
```

```
    SNR(c) = 20 * log10(Vs(c) / Vn(c));
end

[max, maxi] = max(SNR);
maxi, SNR(maxi)

figure(1);
set(gca, 'fontsize', 20);
plot(tint, SNR, 'LineWidth', 2);
ylabel('SNR (dB) (s)'); grid;
xlabel('Integration time (s)');
```

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APPENDIX B

```
%DC level signal calculation

clc; clear;
t = [0 : 0.005 : 1];

V0 = 2.5;
Cph = 22 * 10^-15;
Phi = 0.7;
Trst = 0.2 * 10^-6 ;
Tint = 30 * 10^-3;
Idk = 2.28 * 10^-15;

WL = 10;
Vb = 0.7;
Mu = 1350; q = 1.6 * 10^-19; Es = 11.8 * 8.85 * 10^-24;
Na = 10^17; PhiF = 0.0259 * log(Na/(1.5 * 10^10)); VsP = 2.47;
I0 = Mu * Vb^2 * (2 * q * Es * Na)^0.5 / (4 * PhiF + 2 * VsP)^0.5;
Vgb = 2.5; Vdb = 2.5;
k = 1.3;
I = 2.3 * 10^-15;
Vt = 0.0259;

%*****************************************************************
for KK = 1 : 2000 - 5
    Iph(KK) = Idk + (KK - 1) * 10^-15;

    V(1) = 2.1;
    T(1) = 0;
    for j = 2 : 100;
        if mod(j, 2) == 1
            %Integration
            %V(j) = V(j - 1) - (Iph(KK) / Cph) * Tint;
            V(j) = ( (V(j - 1) + Phi)^(3/4) - (3*Iph(KK)/(4*Cph)) *
(V(j - 1) + Phi)^(-1/4) * Tint)^(4/3) - Phi;
            %V(j) = Vt * log( (Idk / Iph(KK)) - ((Idk / Iph(KK)) -
exp(V(j - 1) / Vt)) * exp(-Tint * Iph(KK) / (Vt * Cph)) );
            T(j) = T(j - 1) + Tint;
        else
            A = ((WL / Cph) * I0 * exp(Vgb * k / Vb));
            B = A * exp(-Vdb / Vb) + I / Cph;
            K = A - B * exp(V(j - 1) / Vb);
            V(j) = Vb * (-log(B) + log(A - K * exp(-Trst * B / Vb) )
);
            T(j) = T(j - 1) + Trst;
        end
    end

    Sw(KK) = V(j) - V(j - 1);
    DCL(KK) = (V(j) + V(j - 1))/2;
end

figure(1);
```

```
set(gca, 'fontsize', 36);

plot(Iph * 10^12, DCL(1) - DCL, 'r', Iph * 10^12, Sw - Sw(1), 'b',
'linewidth', 4, 'markersize', 10);
legend('DC level', 'Swing');
xlabel('Photocurrent(pA)');
ylabel('Output(V)');

%************Draw sample ones
figure(2);
TE = 67;

Iph(KK) = Idk + 0 * 10^-15;

V(1) = 2.1;
T(1) = 0;
for j = 2 : 100;
    if mod(j, 2) == 1
        %Integration
        %V(j) = V(j - 1) - (Iph(KK) / Cph) * Tint;
        V(j) = ( (V(j - 1) + Phi)^(3/4) - (3*Iph(KK)/(4*Cph)) * (V(j
- 1) + Phi)^(-1/4) * Tint)^(4/3) - Phi;
        %V(j) = Vt * log( (Idk / Iph(KK)) - ((Idk / Iph(KK)) -
exp(V(j - 1) / Vt)) * exp(-Tint * Iph(KK) / (Vt * Cph)) );
        T(j) = T(j - 1) + Tint;
    else
        A = ((WL / Cph) * I0 * exp(Vgb * k / Vb));
        B = A * exp(-Vdb / Vb) + I / Cph;
        K = A - B * exp(V(j - 1) / Vb);
        V(j) = Vb * (-log(B) + log(A - K * exp(-Trst * B / Vb) ) );
        T(j) = T(j - 1) + Trst;
    end
end

set(gca, 'fontsize', 36);
plot(T(1:TE), V(1:TE), 'g', 'linewidth', 4, 'markersize', 10); hold
on;
xlabel('Time(s) DC level output Swing output');
ylabel('Sense node voltage(V)');

Iph(KK) = Idk + 10 * 10^-15;

V(1) = 2.1;
T(1) = 0;
for j = 2 : 100;
    if mod(j, 2) == 1
        %Integration
        %V(j) = V(j - 1) - (Iph(KK) / Cph) * Tint;
        V(j) = ( (V(j - 1) + Phi)^(3/4) - (3*Iph(KK)/(4*Cph)) * (V(j
- 1) + Phi)^(-1/4) * Tint)^(4/3) - Phi;
        %V(j) = Vt * log( (Idk / Iph(KK)) - ((Idk / Iph(KK)) -
exp(V(j - 1) / Vt)) * exp(-Tint * Iph(KK) / (Vt * Cph)) );
        T(j) = T(j - 1) + Tint;
    else
        A = ((WL / Cph) * I0 * exp(Vgb * k / Vb));
```

```
        B = A * exp(-Vdb / Vb) + I / Cph;
        K = A - B * exp(V(j - 1) / Vb);
        V(j) = Vb * (-log(B) + log(A - K * exp(-Trst * B / Vb) ) );
        T(j) = T(j - 1) + Trst;
    end
end

plot(T(1:TE), V(1:TE), 'c', 'linewidth', 4, 'markersize', 10); hold
on;

Iph(KK) = Idk + 50 * 10^-15;

V(1) = 2.1; %Initialize sense node voltage
T(1) = 0;
for j = 2 : 100;
    if mod(j, 2) == 1
        %Integration
        %V(j) = V(j - 1) - (Iph(KK) / Cph) * Tint;
        V(j) = ( (V(j - 1) + Phi)^(3/4) - (3*Iph(KK)/(4*Cph)) * (V(j
- 1) + Phi)^(-1/4) * Tint)^(4/3) - Phi;
        %V(j) = Vt * log( (Idk / Iph(KK)) - ((Idk / Iph(KK)) -
exp(V(j - 1) / Vt)) * exp(-Tint * Iph(KK) / (Vt * Cph)) );
        T(j) = T(j - 1) + Tint;
    else
        %Reset
        A = ((WL / Cph) * I0 * exp(Vgb * k / Vb));
        B = A * exp(-Vdb / Vb) + I / Cph;
        K = A - B * exp(V(j - 1) / Vb);
        V(j) = Vb * (-log(B) + log(A - K * exp(-Trst * B / Vb) ) );
        T(j) = T(j - 1) + Trst;
    end
end

plot(T(1:TE), V(1:TE), 'm', 'linewidth', 4, 'markersize', 10); hold
on;
legend('Photocurrent = 0pA', 'Photocurrent = 10pA', 'Photocurrent =
50pA');
```