FULL BRIDGE DC/DC CONVERTER WITH ZERO CURRENT SWITCHING SYNCHROUNOUS RECTIFICATION FOR AUXILIARY POWER UNITS

FULL BRIDGE DC/DC CONVERTER WITH ZERO CURRENT SWITCHING SYNCHRONOUS RECTIFICATION FOR AUXILIARY POWER UNITS

By

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A Thesis
Submitted to the Department of Electrical and Computer Engineering
and the School of Graduate Studies
of McMaster University
in Partial Fulfillment of the Requirements
for the Degree of
Master of Applied Science

Master of Applied Science (2014) McMaster University
(Electrical and Computer Engineering) Hamilton, Ontario

TITLE: **Full Bridge DC/DC Converter with Zero Current Switching Synchronous Rectification for Auxiliary Power Units**

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NUMBER OF PAGES: XII, 85

ABSTRACT

Auxiliary power unit (APU) is a device that provides non-propulsion power in vehicles. In conventional commercial vehicles, APU is usually an alternator. For hybrid electric vehicles (HEVs) and electric vehicles (EVs), APU is a DC/DC converter. This APU provides power from the high voltage (HV) DC battery to the low voltage (LV) DC battery. The input side of the APU is the HV battery, which also provides power for the traction motor. The output side of the APU is the LV battery, which provides power for the electrical control systems and other electronic devices. Therefore, the design of the APU greatly impacts the operation and overall efficiency of the vehicle.

The design challenges of APU include large output current, strict efficiency requirement and low electromagnetic interference (EMI). In this thesis, a phase shifted full bridge (PSFB) DC/DC converter with current doubler synchronous rectifier is proposed for APU applications. The proposed converter is able to endure large output current with low power loss. In addition, soft switching is applied to the converter based on the load conditions. This can effectively reduce EMI and improve converter efficiency. Detailed converter operating principles and design considerations are described.

To further improve the converter efficiency, a zero current switching (ZCS) synchronous rectification (SR) control scheme is proposed. The proposed control scheme maximizes the SR MOSFET on-time and, therefore, reduces MOSFET body diode

conduction loss. The proposed control scheme is verified by experimental results with a 2.4 kW, 100 kHz prototype.

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my advisor Dr. Ali Emadi for his guidance, care and support. He has given me full support to realize my ideas and has guided me in the right direction to the completion of this research. What's more, he has given me valuable suggestions, which I am especially grateful for. It has been my honor to be under the supervision of Dr. Emadi for the past two years.

This research was undertaken, in part, thanks to funding from the Canada Excellence Research Chairs Program.

I would like to thank the senior research engineers Dr. Pierre Magne and Dr. Berker Bilgin in our group. With their tremendous help, I have been able to gain experience in research and engineering. This thesis would not have been produced if it were not for their time and effort.

I would also like to thank the colleagues and friends from the McMaster Automotive Resource Centre (MARC) for their kind support and for the happy time spent together. My thanks are especially given to Fei Peng, Haizhong Ye and Ping Liu. They have offered me great help in research and in experimental set-up.

I would also like to thank my mother and father for their love and endless support. I would like to dedicate this thesis especially to my parents.

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Chapter 1

INTRODUCTION

1.1 INTRODUCTION

With increasing concerns in fuel economy and environmental problems, hybrid electric vehicles (HEVs) and electric vehicles (EVs) are gaining more and more popularities nowadays. For HEVs and EVs, the most important and challenging part lies in developing high efficient power electronic systems [1]-[3]. The power electronic systems include several DC/DC converters and inverters or the integration of converter and inverter systems. Among the power electronic circuits in HEVs and EVs, auxiliary power unit (APU) is one essential part that has significant impact on vehicle operations.

In HEVs and EVs, APU is a DC/DC converter that connects the high voltage (HV) DC system and the low voltage (LV) DC system and transfers energy from the former to the latter. The LV system is connected to a LV battery, which is 12V for light duty vehicles, and various electrical loads. These loads include the control system, vehicle climate system, lighting system, etc. When all the utilities are turned on, the total power can be as high as 2.4 kW.

For 1-3 kW isolated DC/DC converters, full bridge is one of the most popular topology for the input stage [4]. Over the past years, intensive research on full bridge DC/DC converter has been conducted and focused on soft switching techniques for this

topology [5]-[10]. For zero voltage switching (ZVS), the idea is to utilize the transformer leakage inductance or certain auxiliary circuits to deplete the energy stored within parallel capacitor of full bridge MOSFETs, and turn on the MOSFET only after its body diode has turned on. For zero current switching (ZCS), the current through the full bridge MOSFET has to be decreased to zero before turning off the MOSFET.

In this thesis, a full bridge (PSFB) converter with current doubler rectifier is designed for APU. The full bridge control signals are phase shifted to ensure the ZVS operation of the input stage. Current doubler rectifier is used on the secondary side to reduce current stress on the transformer and output filter inductor, which is further explained in Chapter 2.

To reduce converter secondary side power loss, synchronous rectification (SR) is adopted for the current doubler. This yields reduction of power loss as the conduction loss of MOSFET is much less than that of its body diode. Moreover, in this thesis, a ZCS SR control scheme is proposed to reduce conduction loss of the current doubler by increasing the SR MOSFET conduction time, and hence by reducing the conduction time of MOSFET body diode.

1.2 RESEARCH GOALS

APU design is essential for the vehicle operation. Literature available has been focused on the integration of APU with the vehicle system [11]-[14]. This thesis is then focused on the design and efficiency improvement of the converter.

There are mainly two objectives for this thesis. The first is to identify the converter design requirements for APU, to select the converter topology for APU, to present the

converter design considerations of APU and give a design example of APU to verify the operation of the converter.

The second objective is to further improve the APU efficiency by proposing a ZCS SR control scheme and to verify the effectiveness of the method by experimental results.

1.3 OVERVIEW OF CHAPTERS

The outline of the thesis is as follows.

Chapter 2 introduces the background knowledge of APU. First, APU in aircraft and commercial trucks is briefly introduced. Then, APU in HEVs and EVs is described in details. Based on the characteristics of APU in HEVs and EVs, the converter topology for APU is selected.

Based on the selected topology, the converter operating principle is introduced in Chapter 3. First, the background of soft switching is introduced. Then the converter steady state operation is described with ten operation modes. After that, the duty cycle loss period is particularly elaborated in detailed equations. This is to provide foundations for design considerations in Chapter 4 and an improved control scheme in Chapter 5.

Based on the operating principles, Chapter 4 presents the detailed design considerations and experimental results for the converter. First, a design example is given with typical parameters from automobiles. Then design equations of the transformer, resonant inductor and output filters are presented. After that, the converter prototype is described. Finally, experimental results of the control signals, duty cycle loss and ZVS states under various load conditions are presented.

After the completion of the converter design, Chapter 5 proposes a zero current switching (ZCS) synchronous rectification (SR) control scheme to further improve the converter efficiency. Comparison between conventional SR control scheme and the proposed SR control scheme is conducted. The results are verified by experiments.

Finally, Chapter 6 concludes the thesis. Major contributions are presented and the thesis is summarized.

Chapter 2

AUXILIARY POWR UNITS

2.1 INTRODUCTION

Auxiliary power unit (APU) is a system in vehicles that provides power which is not used for propulsion. APU can be widely found in aircrafts, ships, and land vehicles. APU may consist of a small engine and battery, or a power converter and battery. The function of APU can include creating a comfortable vehicle environment, and helping start the traction engine/motor. This chapter first introduces the background knowledge of APU in aircraft, commercial trucks and hybrid electric vehicles (HEVs) or electric vehicles (EVs). Then the APU in HEVs and EVs is described in details. Finally the design objectives for APU in HEVs and EVs are presented, and the APU topology is selected according to the design requirements.

2.1.1 APU in Aircraft

The structure of aircraft turbine engine determines that it's not possible for the engine to start by itself [15]. The turbine engine requires air flow before ignition, which calls for external power provided to it for rotation. APU is a good solution for this. With the energy from accumulator and fuel tank, APU is able to generate compressed air for the main engine of aircraft. In this way, the aircraft is able to start without reliance on

power supplies from the airport. What's more, when the main engine stops at flight, APU enables the main engine to start again.

In addition to providing air compression for the main engine to start, aircraft APU also ensures a comfortable environment in the aircraft cabin. It provides power to the air conditioning system, lighting system, etc. Before the aircraft takes off or after it lands on the ground, the main engine can stop and only the APU is at operation to provide power for the electrical system. This greatly saves the aircraft energy.

In aircraft, APU provides power with 115V, 400 Hz AC, or 28V DC for the electrical system. The 400 Hz frequency is designed with a tradeoff among the cost, size and efficiency of APU.

2.1.2 APU in Commercial Trucks

In commercial trucks, APU is mostly a small diesel engine with a low voltage battery pack. It mainly provides power for the climate control, lighting system, cooling system, etc. Like APU in aircraft, APU in trucks also saves a great deal of power for the main engine, when the vehicle is not running on the road. For example, some APU consumes only 1 US gallon of fuel for 8 hours running, while the main engine would cost 2 US gallons for 1 hour idling (Cat 600) [15]. This saves enormous amount of energy when the driver is taking a rest on a static truck.

Besides, APU also provides power to heat the engine, which enables the engine to start quickly at cold weather conditions. In some trucks, there are some other devices that require constant power supply. Under such conditions, APU also plays important roles in providing efficient power.

2.1.3 APU in Hybrid/Electric Vehicles

As is shown in Figure 2.1 [16], in hybrid electric vehicles (HEVs) or electric vehicles (EVs), there is a high voltage (HV) battery (usually rated at 200V – 400V), which provides power for the traction motor. Also, there is a low voltage (LV) battery (rated at 12V for light duty vehicles [17]), which provides power for other electronic devices, such as lighting systems, air conditioning, audio systems, etc. The problem is that the power stored in the LV battery is very limited, and is very easy to deplete if the LV battery is not charged. The general solution is to use a DC/DC converter to transfer energy from the HV battery to the LV battery, and keep the normal operation of the vehicle. Here, the DC/DC converter is the main topic of this thesis. In the rest of the thesis, APU specifically refers to this DC/DC converter in HEVs and EVs.

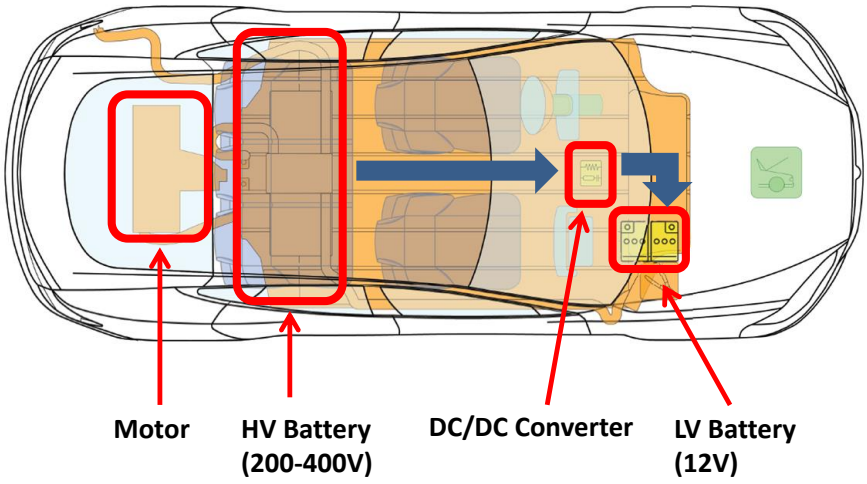


Figure 2.1 APU in Hybrid/Electric Vehicles

2.2 APU IN INDUSTRY

Figure 2.2 shows the layout of APU in 2004 Toyota Prius [18]. The DC/DC converter lies in between the HV side and the LV side and transfer energy from the former to the latter. It is worth mentioning that there is one isolation transformer in the DC/DC converter. This is the isolation requirement for all the HEVs and EVs to ensure the safe operation of the vehicle.

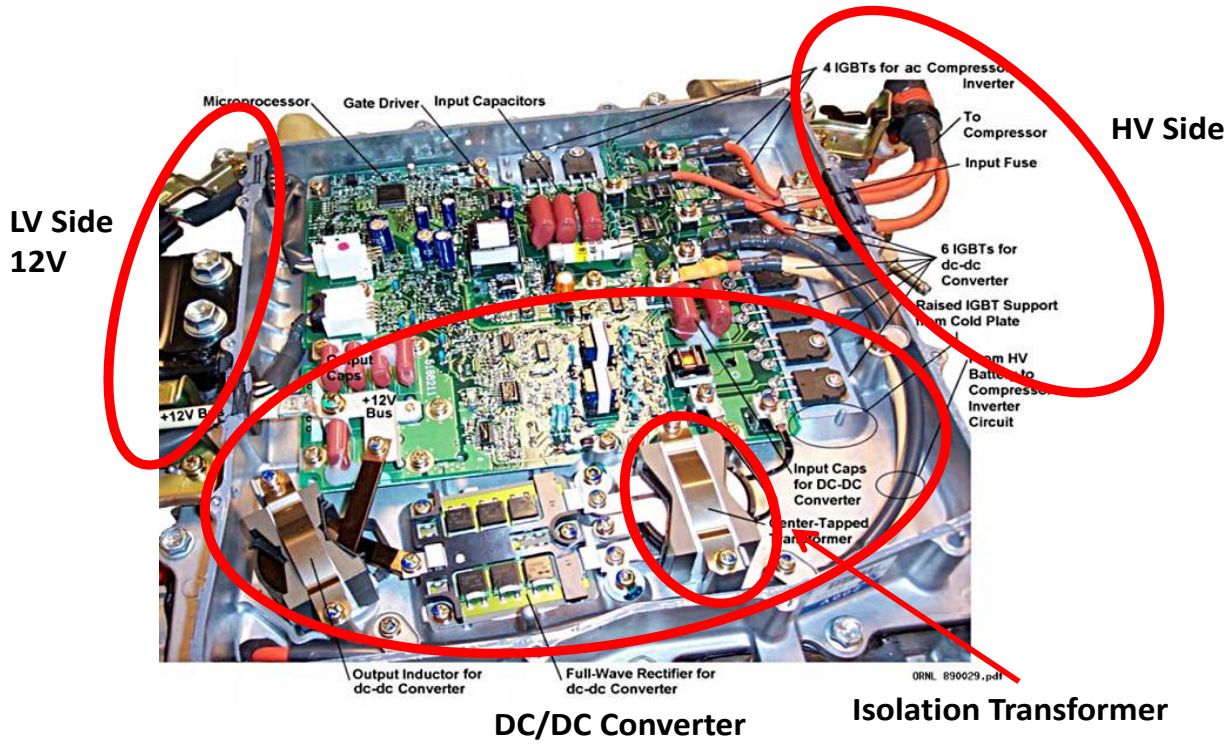


Figure 2.2 APU in 2004 Toyota Prius

TABLE I and TABLE II show the APU parameters of some HEVs and EVs on market [19]-[25]. It is demonstrated that the current rating of APU is usually between 100-200A, and the power rating of APU is usually between 1.2-2.4 kW.

Table 2.1 APU Parameters in HEVs

Model	Jetta Hybrid 2013	Chevrolet Volt 2011
Nominal Input Voltage	220 V	345.6 V
Power		2.2 kW
Output Current	150 A	165 A

Table 2.2 APU Parameters in EVs

Model	Ford Transit Connect Electric 2011	Coda Electric 2010	Tesla Roadster 2008
Nominal Input Voltage	300 V	333 V	366 V
Power		2.2 kW	
Output Current	110 A		200 A

2.3 APU DESIGN OBJECTIVES

According to the information of APU from Section 2.2, there can be three design objectives for APU.

First, the basic requirement is that the HV side of the vehicle should be isolated from the LV side of the vehicle, which requires the use of high frequency transformer in the DC/DC converter. What's more, the converter should satisfy the power rating of 1.2-2.4 kW.

Second, since the APU output current is extremely high compared with output voltage, the DC/DC converter output side should be able to endure the high current pressure.

Third, since the APU power is high, a little change in efficiency can result in a big difference in energy consumption. Hence the efficiency requirement for DC/DC converter is high.

2.4 APU TOPOLOGY

2.4.1 Basic Topology

As has been discussed in Section 2.3, the DC/DC converter for APU has to be an isolated type to ensure the safe operation of the vehicle. Hence the diagram of basic APU topology is illustrated as Figure 2.3.

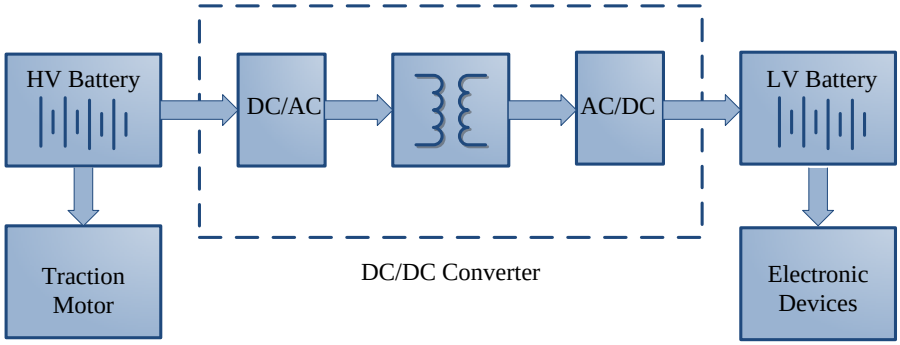


Figure 2.3 Basic APU Topology

As is shown in Figure 2.3, the input of the DC/DC converter is the HV battery, and the output of the DC/DC converter is the LV battery. There is an isolation transformer in the converter. Before the transformer it is the primary side, which transforms HV DC into AC. The primary side is basically an inverter. After the transformer it is the secondary side, which transforms AC into LV DC. The secondary side is basically a rectifier. The converter primary side and secondary side topologies are described in details in the rest of Section 2.4.

2.4.2 Primary Side Topology

For primary side, the number of power electronic switches determines the power rating of the converter. For 1-3 kW isolated DC/DC converters, full bridge is one of the most popular topology [4]. The basic topology of a full bridge converter is shown in Figure 2.4.

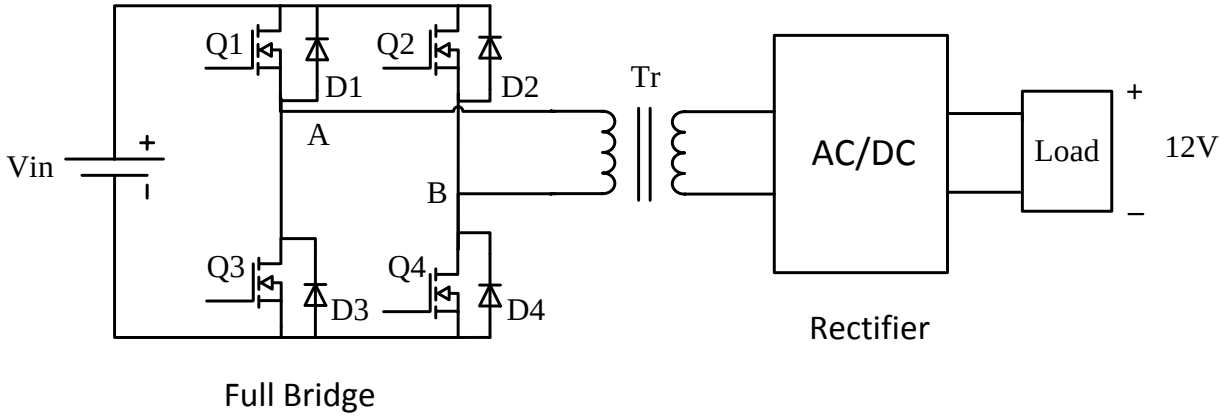


Figure 2.4 Full Bridge DC/DC Converter

For the converter shown in Figure 2.4, Q1 – Q4 make up the full bridge. When Q1 and Q4 are both turned on, the current goes from A to B. When Q2 and Q3 are both turned on, the current goes from B to A. Hence the full bridge generates alternating current on the primary side. The alternating current is able to transfer through the high frequency transformer to the secondary side, which rectifies the AC into output DC.

2.4.3 Secondary Side Topology

For the secondary side, the output current is extremely high compared with the output voltage. For high output current applications, current doubler is preferred than centre tap rectifier, for its advantage in transformer and inductor optimization [26]. A

typical current doubler rectifier is shown in Figure 2.5. In current doubler rectifier, there is only one coil at the transformer secondary side. In contrast, in a conventional center-tap transformer, there are two secondary side coils, and each of them is of the same size as in current doubler transformer. Therefore, current doubler transformer saves material and potentially reduces transformer size. Another advantage of the current doubler rectifier is that it utilizes two output filter inductors to share the output current. Each filter inductor shares half of converter output current. Also, the two inductors work in an interleaved way, therefore the output current ripple is half of the inductor current ripple. Therefore, in this work, current doubler topology is adopted for the converter secondary side.

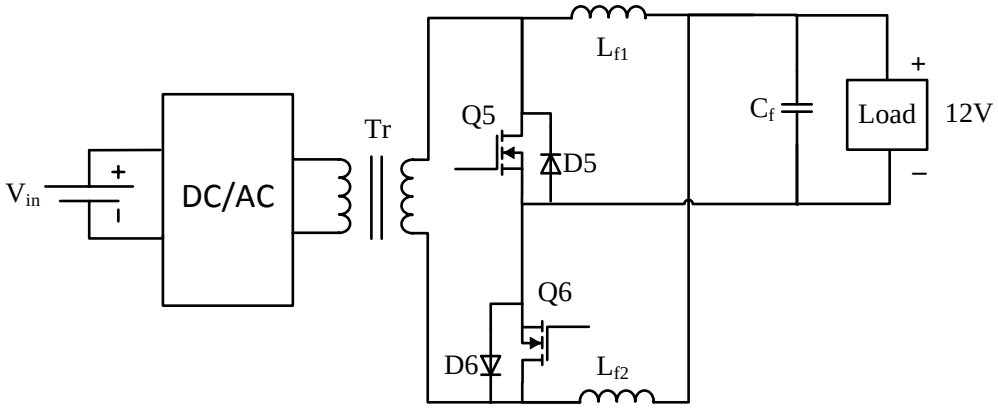


Figure 2.5 Current Doubler Rectifier

2.4.4 Synchronous Rectification

From the view of rectifier switches, there are conventional rectifiers, which use diodes as the rectifier switches, and synchronous rectifiers, which use MOSFETs as the rectifier switches. These two types of rectifiers are shown in Figure 2.6 and Figure 2.7. For synchronous rectifier in Figure 2.7, Q5 and Q6 turn on when the voltage would turn

on the diode, hence the operations of these two types of rectifiers are the same. The difference is that the forward voltage in MOSFET is much lower than that in diode under the same current rating. Hence the conduction loss can be greatly reduced by applying synchronous rectifier.

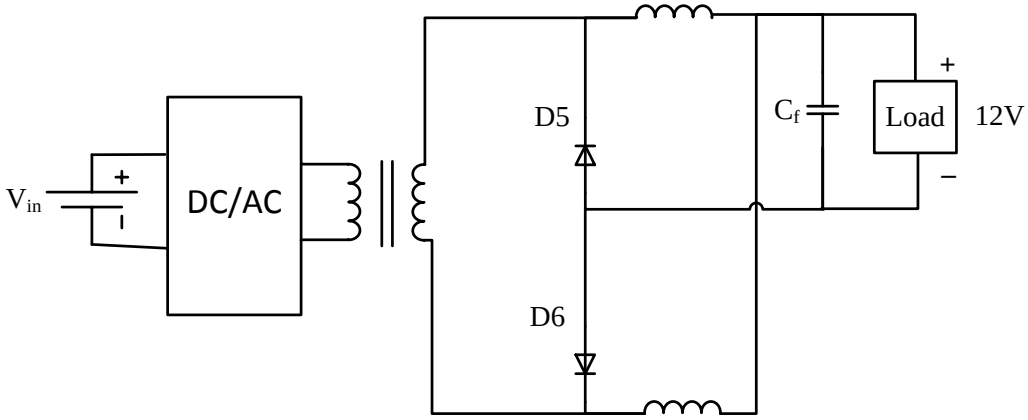


Figure 2.6 Diode Rectifier

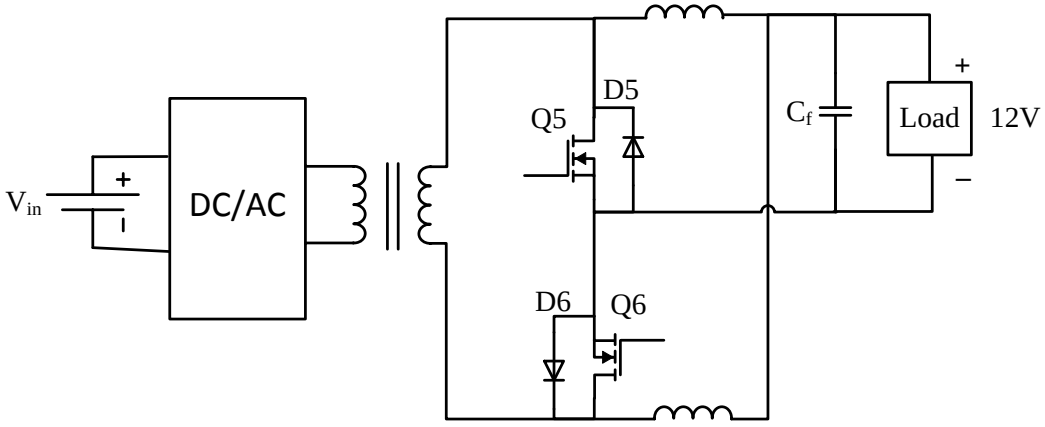


Figure 2.7 Synchronous Rectifier

Table 2.3 shows the parameter comparison of a typical rectifier diode and a typical rectifier MOSFET. Both of them can endure 50A forward current. For the

MOSFET, it requires the use of gate driver, which makes the total cost of a synchronous rectifier a little bit higher than that of a diode rectifier. However, the power loss of the MOSFET is much lower than the diode, which is shown in Figure 2.8. Hence synchronous rectifier is preferred than diode rectifier in high current applications like APU, and is adopted in this work.

Table 2.3 Parameter Comparison between Diode and MOSFET Rectifier

Rectifier Type	**Part Number**	**Forward Current**	**Forward Voltage**	**On Resistance**	**Price**
Diode	APT60S20BG	50A	0.9V		$ 6.44
MOSFET	IRFS7530-7PPBF	50A		1.1mΩ	$ 5.15 MOSFET $ 2.75 Gate Driver

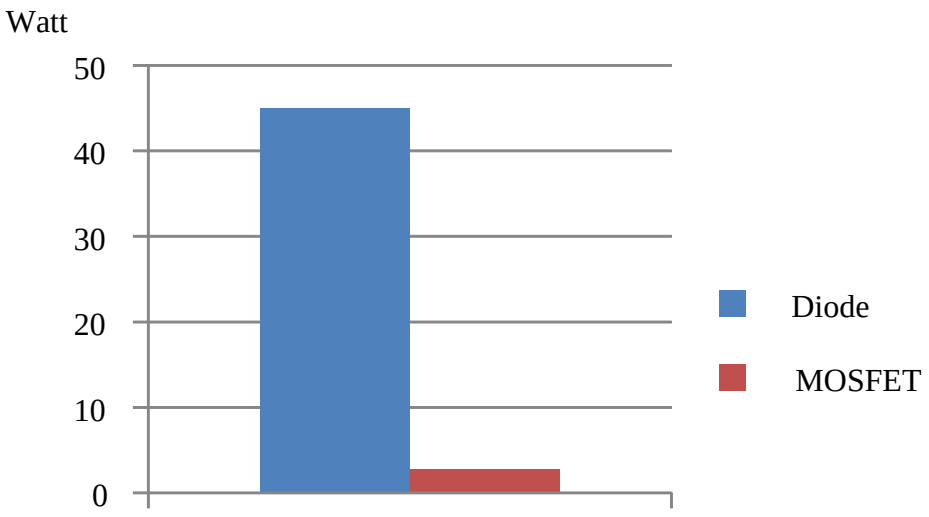


Figure 2.8 Power Loss Comparison between Diode and MOSFET

2.4.5 Conclusion

To sum up, the final topology for APU is shown in Figure 2.9, which is full bridge DC/DC converter with current doubler synchronous rectifier. In this converter, Q1 – Q4 forms the full bridge; Q5 & Q6 make up the synchronous rectifier; L_{f1} & L_{f2} make up the current doubler. The detailed operating principle will be described in Chapter 3.

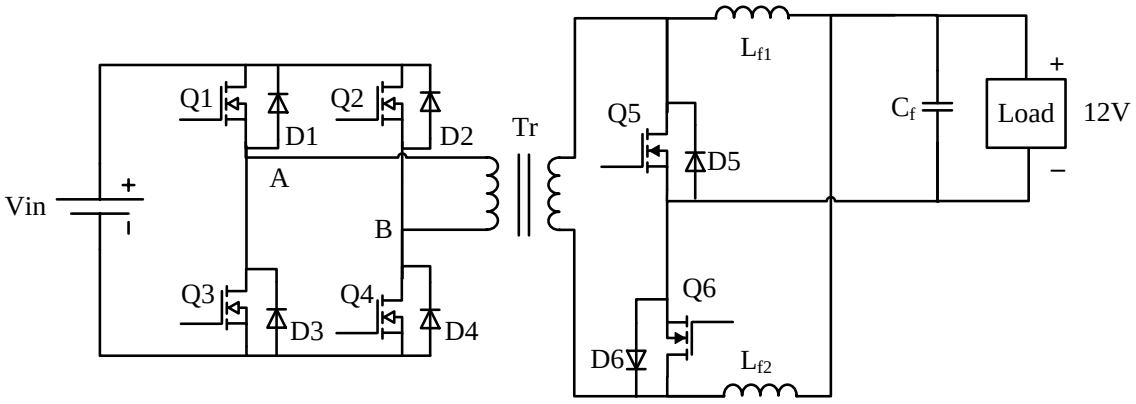


Figure 2.9 Full Bridge with Current Doubler Synchronous Rectifier

Chapter 3

CONVERTER OPERATION

3.1 INTRODUCTION

In last chapter, the topology for APU is finalized as full bridge DC/DC converter with current doubler synchronous rectifier. In this chapter, the operating principle of the proposed converter is described in details.

For full bridge DC/DC converter, the working frequency is relatively high (50 kHz or higher). High frequency can effectively reduce transformer size and output filter size. However, it also results in large switching loss and electromagnetic interference (EMI). To solve these problems, soft switching has been widely adopted in full bridge DC/DC converters [5]-[10].

In this chapter, the background knowledge of soft switching is first introduced. Then the converter operation modes are described in details.

3.2 SOFT SWITCHING

Figure 3.1 shows the MOSFET voltage and current. V_g is the MOSFET gate drive voltage. V_{ds} is the drain to source voltage across the MOSFET. I_{ds} is the current through the MOSFET. These three values will be used in the following explanation of hard switching and soft switching.

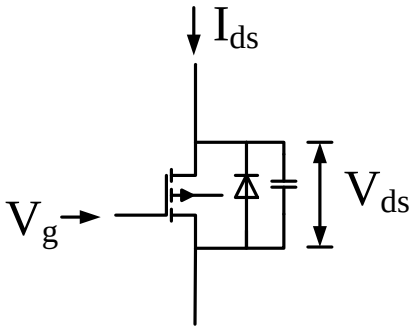


Figure 3.1 MOSFET Voltage and Current

Figure 3.2 shows the diagram of hard switching. For hard switching, when the MOSFET turns off and turns on, there is a transition period. During the transition period,

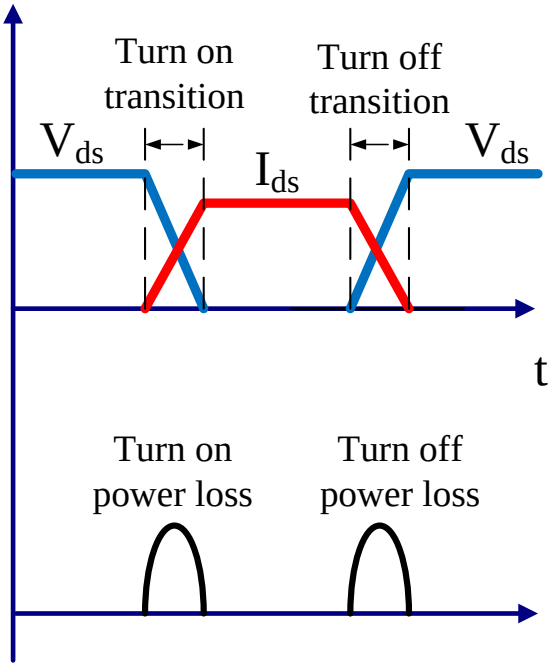


Figure 3.2 MOSFET Hard Switching

the MOSFET voltage V_{ds} and MOSFET current I_{ds} are overlapped. Since the power is the product of the voltage and current, power loss is hence generated during the switching period.

Compared with hard switching, soft switching gets rid of the overlap of V_{ds} and I_{ds}. Figure 3.3 shows zero voltage switching (ZVS) turn on. For ZVS turn on, the MOSFET gate drive voltage V_g is not applied until V_{ds} drops to zero. Hence I_{ds} starts to rise after V_{ds} drops to zero, and the overlap between the current and voltage is avoided.

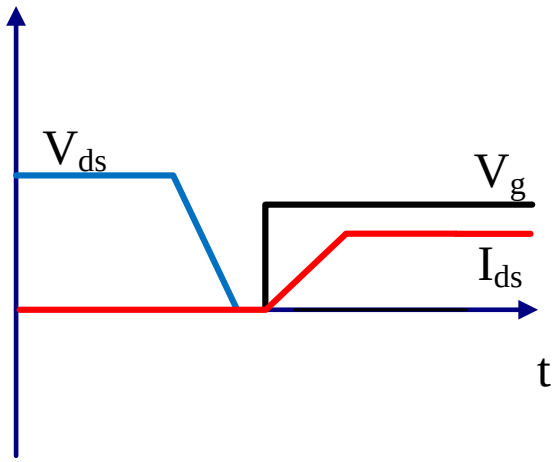


Figure 3.3 Zero Voltage Switching (ZVS) Turn on

Figure 3.4 shows zero current switching (ZCS) turn off. For ZCS turn off, V_g goes low after I_{ds} drops to zero. Hence V_{ds} does not rise until I_{ds} drops to zero, and the overlap between MOSFET current and voltage is avoided.

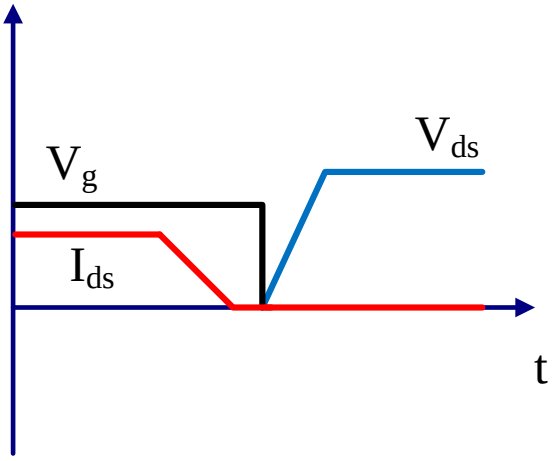


Figure 3.4 Zero Current Switching (ZCS) Turn off

For full bridge DC/DC converter, ZVS is more commonly adopted. Figure 3.5 shows how ZVS is achieved on a full bridge MOSFET. As is shown, the MOSFET Q has a body diode D and body capacitor C. To achieve ZVS, the voltage on the capacitor has to be discharged to zero before Q turns on. Detailed full bridge ZVS process is explained in Section 3.3.

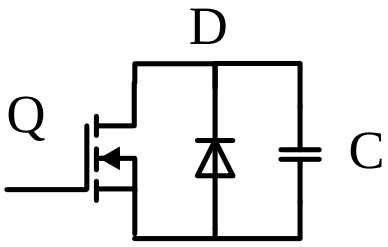


Figure 3.5 ZVS on MOSFET

3.3 **OPERATING PRINCIPLES**

3.3.1 Operation Waveforms

Figure 3.6 presents the proposed topology for the APU. The converter input voltage V_{in} is the DC voltage of the high voltage battery in the vehicle, and the output voltage is 12V. Q1, Q2, Q3 and Q4 are the full bridge MOSFETs at the primary side. T_r is the high frequency transformer with turns ratio of n. Q5 and Q6 are synchronous rectifier MOSFETs. L_{f1}, L_{f2} and C_f constitute the inductors and capacitor of the output filters.

Figure 3.7 illustrates the converter main waveforms with respect to time. V_{g1} to V_{g6} are the control signals of Q1 to Q6, respectively, and i_p, v_p, $i_{Q5/6}$, $v_{Q5/6}$ can be found in Figure 3.6. Basically, the on-time of V_{g1} to V_{g4} is half of the switching period minus a little bit of dead time. V_{g1} and V_{g4}, or V_{g2} and V_{g3} work in a phase shifted way to achieve ZVS, and this type of full bridge converter is called phase shifted full bridge (PSFB) converter. The equivalent circuits in each time intervals are shown in Figure 3.8 – Figure 3.18. Detailed operation modes are described as follows.

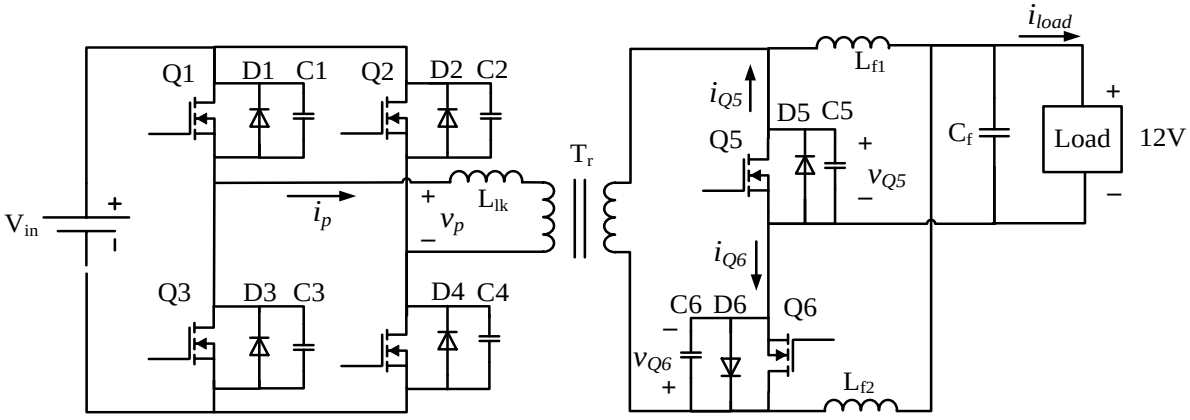


Figure 3.6 Full Bridge Converter with Current Doubler Synchronous Rectifier

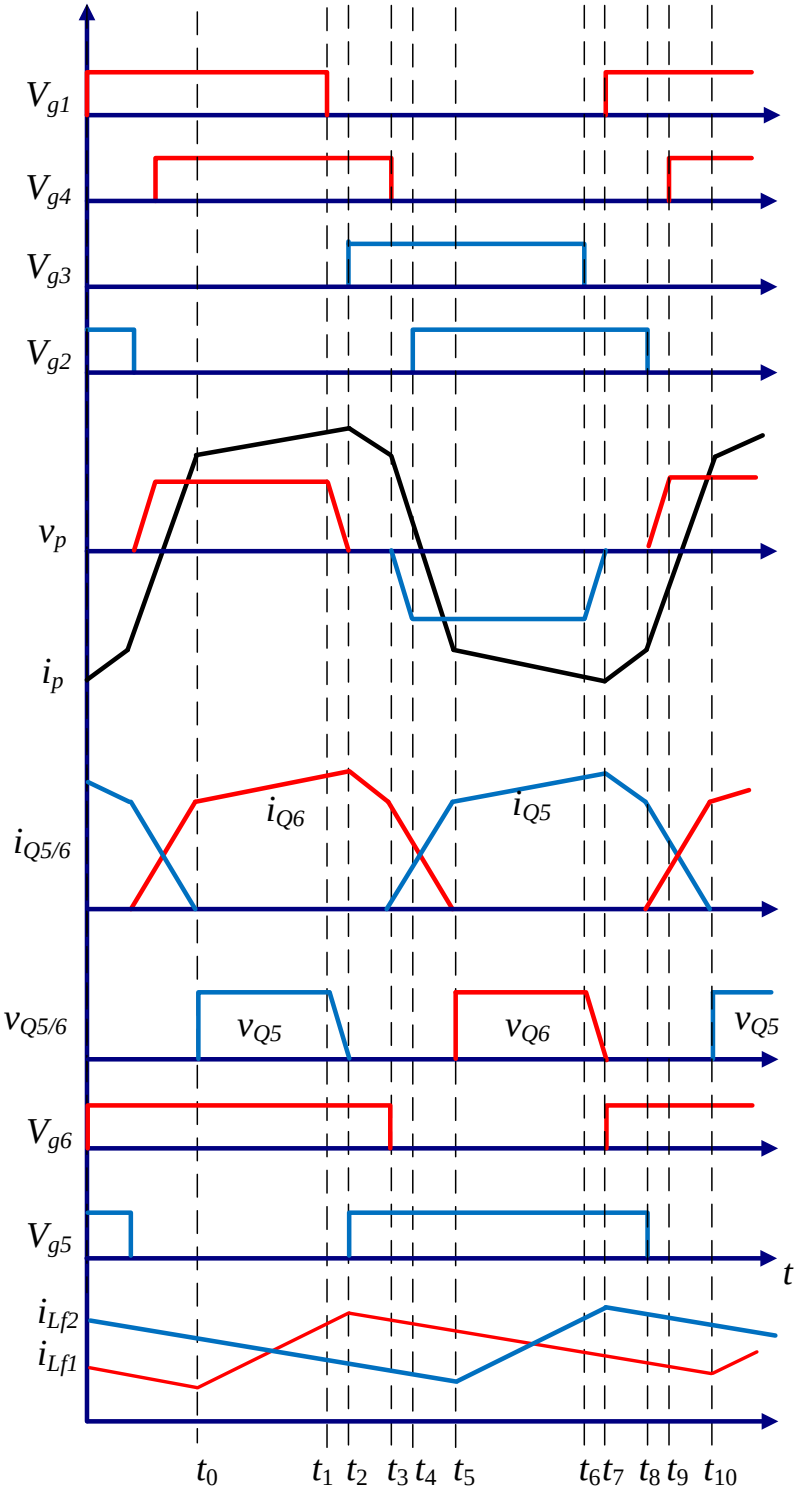


Figure 3.7 Converter Operation Waveforms

3.3.2 Converter Operation from t_0 to t_1

In this mode (Figure 3.8), Q1 and Q4 are conducting. On the primary side, current flows from Q1 to Q4, and the battery energy is transferred from the transformer primary side to the secondary side. The primary side current value increases. The increasing rate is given as follows:

$$\frac{i_p(t) - i_p(t_0)}{t - t_0} = \frac{V_{in} - nV_{out}}{n^2 L_{f1} + L_{lk}} \tag{3-1}$$

In Equation (3-1), $n^2 L_{f1}$ is the equivalent inductance of L_{f1} reflected to the primary side, where n is the transformer primary to secondary side turns ratio.

On the secondary side, the transformer secondary side voltage is

$$V_s = \frac{1}{n} V_{in} \tag{3-2}$$

Current increases in L_{f1} and decreases in L_{f2}. L_{f1} and L_{f2} works in the interleaved way, and the output current is the sum of the currents in these two inductors. Q6 carries all the secondary side current. The output filter inductor currents increasing/decreasing rates are given as follows:

$$\frac{i_{Lf1}(t) - i_{Lf1}(t_0)}{t - t_0} = \frac{\frac{1}{n} V_{in} - V_{out}}{L_{f1}}$$

$$\frac{i_{Lf2}(t) - i_{Lf2}(t_0)}{t - t_0} = \frac{-V_{out}}{L_{f2}} \tag{3-3}$$

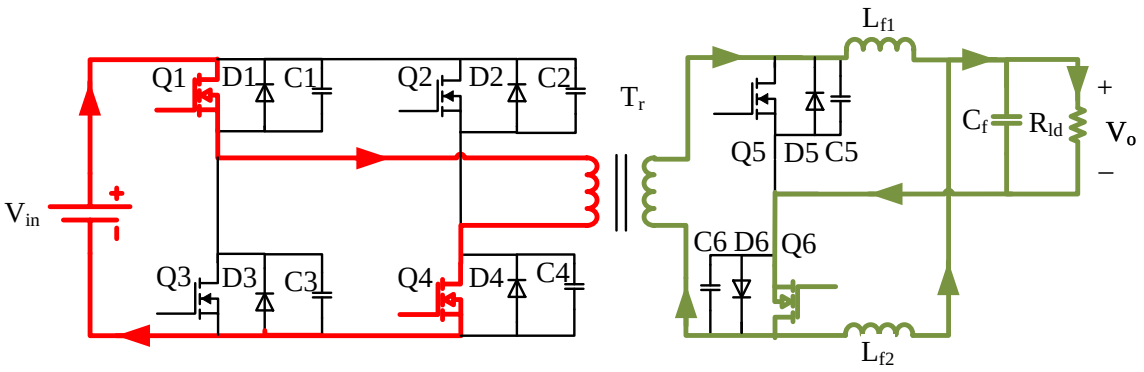


Figure 3.8 Converter Operation Mode from t_0-t_1

3.3.3 Converter Operation from t_1 to t_2

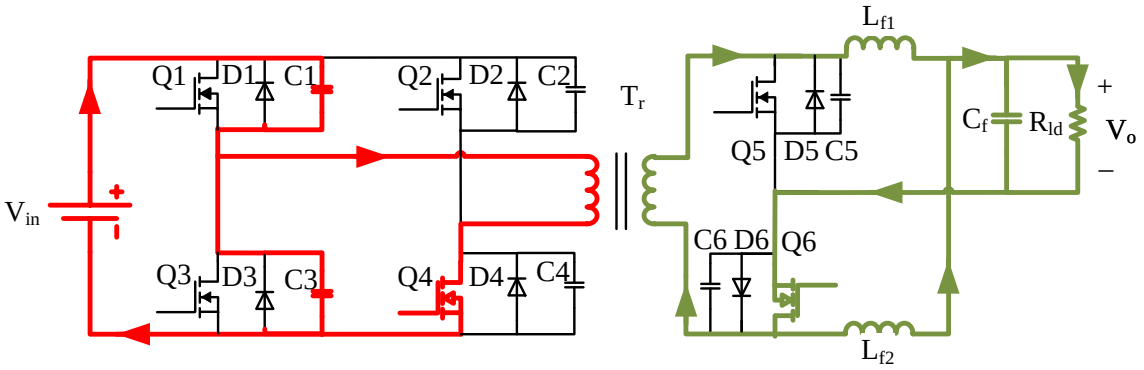
This time interval is the dead time period between Q1 and Q3. At t_1, Q1 turns off. On the primary side, the current discharges C3 from the voltage of V_{in}, and charges C1 from zero voltage, as is shown in Figure 3.9(a). When the voltage across C3 decreases to zero, D3 conducts, which provides condition for zero voltage turn on of Q3, as is shown in Figure 3.9(b). During this period, the primary side equivalent inductance is $n^2 L_{f1(2)} + L_{lk}$, which is usually large enough that the primary side current can be considered as constant. Hence the time required to discharge C3 and charge C1, or the time required to provide ZVS condition for Q3, is

$$t_{13} = \frac{(C1 + C3)V_{in}}{i_p} \tag{3-4}$$

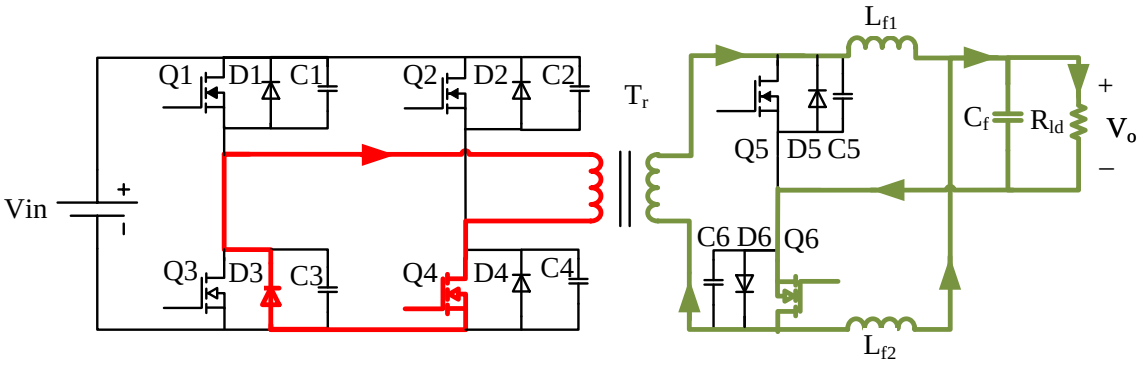
To ensure the zero voltage turn off of Q3, the dead time between Q1 and Q3 has to be larger than t_{13}, which means

$$t_{d13} = (t_2 - t_1) > t_{13} = \frac{(C1 + C3)V_{in}}{i_p} \tag{3-5}$$

On the secondary side, C5 is discharged. When v_{Q5} reaches zero, Q5 also meets the condition for zero voltage turn on.



(a)



(b)

Figure 3.9 Converter Operation Mode from t_1-t_2, (a) before D3 Turns on (b) after D3 Turns on

3.3.4 Converter Operation from t_2 to t_3

This interval is the freewheeling period when no voltage is applied on the transformer (Figure 3.10). At t_2, Q3 and Q5 turn on with zero voltage. On the primary

side, current flows from Q3 to Q4. On the secondary side, voltage and current across Q5 are both zero, and the current flows through Q6. Currents in both the two output filter inductors decrease, and the decreasing rates are given as:

$$\frac{i_{Lf1}(t) - i_{Lf1}(t_2)}{t - t_2} = \frac{-V_{out}}{L_{f1}}$$

$$\frac{i_{Lf2}(t) - i_{Lf2}(t_2)}{t - t_2} = \frac{-V_{out}}{L_{f2}} \quad (3\text{-}6)$$

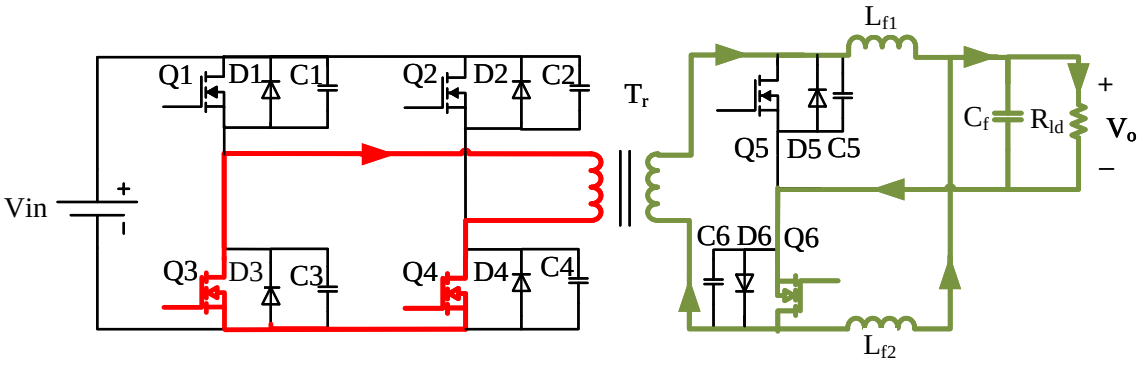
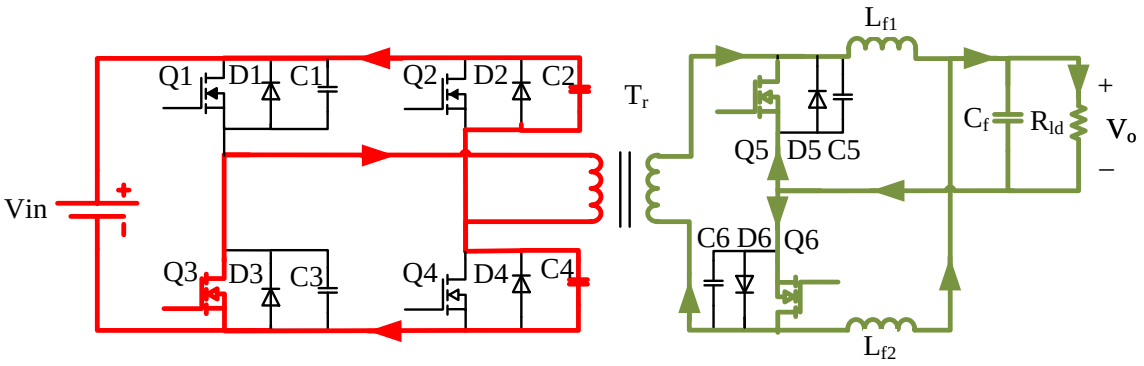


Figure 3.10 Converter Operation Mode from t_2-t_3

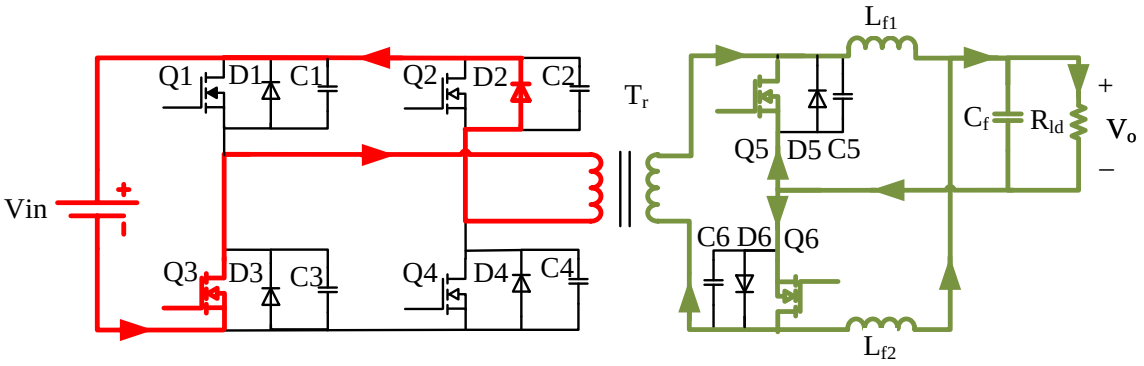
3.3.5 Converter Operation from t_3 to t_4

This is the dead time period between Q4 and Q2. At t_3, Q4 turns off. On the primary side, current discharges C2 from the voltage of V_{in} and charges C4 from zero voltage, as is shown in Figure 3.11(a). This causes the change in transformer voltage direction. When the voltage on C2 is discharged to zero, D2 conducts, which provides the condition for zero voltage turn on of Q2, as is shown in Figure 3.11(b). On the secondary side, i_{Q6} decreases and i_{Q5} increases because of the change in voltage direction on transformer [27]. However, the current cannot change instantly because of the

transformer leakage inductance. Both Q5 and Q6 are on, and the transformer secondary side is short circuited. During this time, there is duty cycle on the primary side, but no duty cycle on the secondary side [28]. This is called duty cycle loss. The equations of duty cycle loss period are described in Section 3.4.



(a)



(b)

Figure 3.11 Converter Operation Mode from t_3-t_4, (a) before D2 Turns on (b) after D2 Turns on

Since the transformer secondary side is short circuited, the energy available to discharge C2 and charge C4 is only the energy stored in the transformer leakage inductance. Hence there might not be sufficient energy to discharge C2, in which case Q2

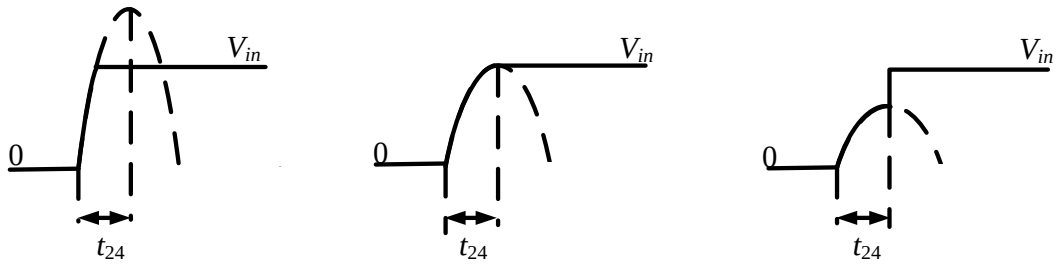
cannot realize zero voltage turn on. The energy for discharging C2 depends on the current value, or the load conditions. Three different conditions are described as follows.

Figure 3.12 shows the details of the rising edge of voltage on C4 during the resonant period between C2, C4 and L_{lk} [28]. Figure 3.12(a) shows the case that there is more than enough energy in the leakage inductance to discharge C2. Figure 3.12(b) shows the case that the energy stored in leakage inductance is equal to the energy required to discharge C2. Figure 3.12(c) shows the case that energy stored in leakage inductance is insufficient to discharge C2. It is seen that no matter which case it is, after a certain amount of resonant time, the voltage on C4 reaches the peak value, and the voltage on C2 reaches the minimum value. This resonant time t_{42} is determined by the leakage inductance and capacitance of C2 and C4. t_{42} is given as [28]:

$$t_{42} = \frac{\pi}{2}\sqrt{L_{lk}C_{MOS}} \tag{3-7}$$

where $C_{MOS} = C2 = C4$.

To minimize the turn on loss of Q2, Q2 is desired to turn on when the voltage on C2 reaches the minimum value. Hence the dead time between Q2 and Q4, t_{d42}, should be equal to t_{42}, regardless of the load conditions.



(a) (b) (c)

Figure 3.12 Detail of the Rising of Voltage on C4 During (t_3-t_4), with (a) More than Sufficient Energy, (b) Exactly Sufficient Energy and (c) Insufficient Energy

Conventionally, Q6 turns off at t_3 with zero voltage. However, I_{Q6} has not dropped to zero at t_3 and I_{Q6} then transfers to the body diode D6. This causes relatively large conduction loss. An improved control scheme is described in Chapter 5 to reduce the power loss.

3.3.6 Converter Operation from t_4 to t_5

Figure 3.13 shows the equivalent circuit of this interval. During this period, secondary side voltage remains zero and duty cycle loss still exists. Duty cycle loss ends after primary side current reduces to zero, rise in the other direction and reaches the value of reflected current in L_{f2}.

During this period, i_{Q6} decreases and i_{Q5} increases. The increasing/ decreasing rates of the primary side current and output filter inductor currents are expressed as:

$$\frac{i_p(t) - i_p(t_4)}{t - t_4} = -\frac{V_{in}}{L_{lk}}$$

$$\frac{i_{Lf1}(t) - i_{Lf1}(t_4)}{t - t_4} = \frac{-V_{out}}{L_{f1}}$$

$$\frac{i_{Lf2}(t) - i_{Lf2}(t_4)}{t - t_4} = \frac{-V_{out}}{L_{f2}} \tag{3-8}$$

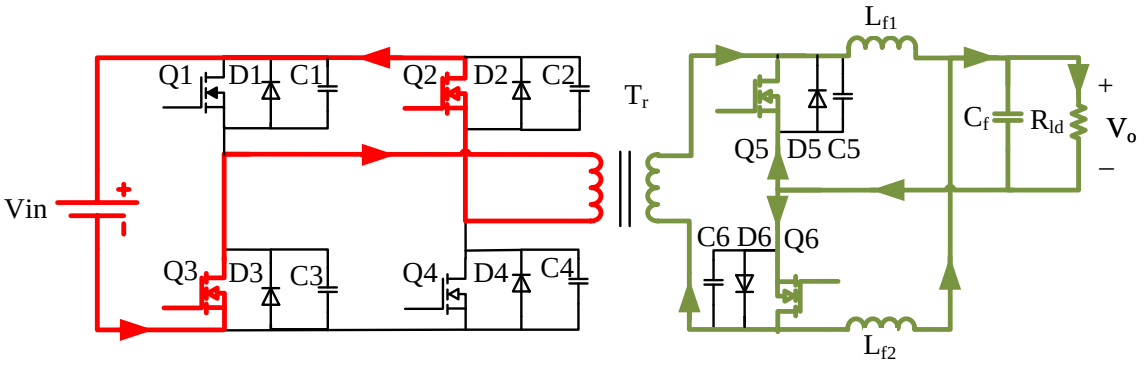


Figure 3.13 Converter Operation Mode from t_4-t_5

3.3.7 Converter Operation from t_5 to t_6

In this mode (Figure 3.14), Q2 and Q3 are conducting. On the primary side, current flows from Q2 to Q3, and the energy again begins to be delivered from the primary side to the secondary side. During this period, i_p is the reflected current of L_{f2}. The value of i_p increases, and the increasing rate is given as follows:

$$\frac{i_p(t) - i_p(t_5)}{t - t_5} = \frac{V_{in}}{n^2 L_{f2} + L_{lk}} \tag{3-9}$$

On the secondary side, transformer secondary side voltage begins to appear. Current in Q6 is zero and all the current flows through Q5. i_{Lf2} increases and i_{Lf1}

decreases. The output filter inductor currents increasing/decreasing rates are given as follows:

$$\frac{i_{Lf1}(t) - i_{Lf1}(t_5)}{t - t_5} = \frac{-V_{out}}{L_{f1}}$$

$$\frac{i_{Lf2}(t) - i_{Lf2}(t_5)}{t - t_5} = \frac{\frac{1}{n}V_{in} - V_{out}}{L_{f2}} \tag{3-10}$$

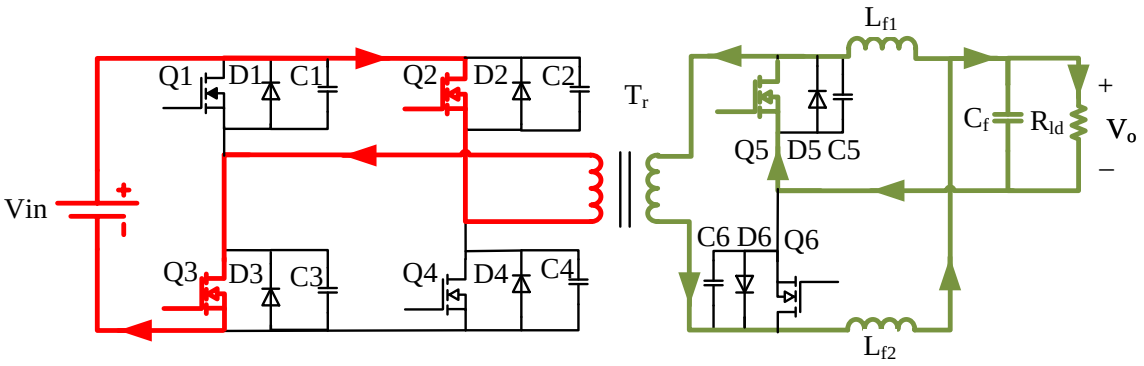


Figure 3.14 Converter Operation Mode from t_5-t_6

3.3.8 Converter Operation from t_6 to t_7

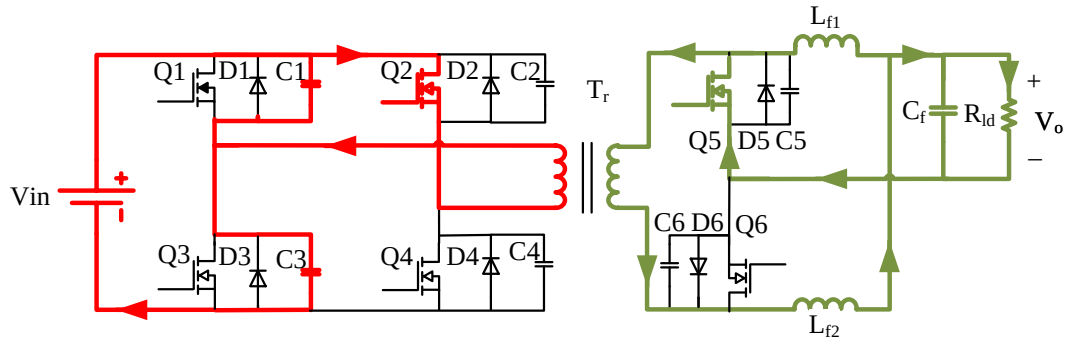
This time interval is the dead time period between Q3 and Q1. At t_6, Q3 turns off. On the primary side, the current discharges C1 from the voltage of V_{in}, and charges C3 from zero voltage, as is shown in Figure 3.15(a). When voltage across C1 decreases to zero, D1 conducts, which provides condition for zero voltage turn on of Q1, which is shown in Figure 3.15(b). The time required to discharge C1 and charge C3, or the time required to provide ZVS condition for Q1, is

$$t_{31} = \frac{(C1 + C3)V_{in}}{i_p} \tag{3-11}$$

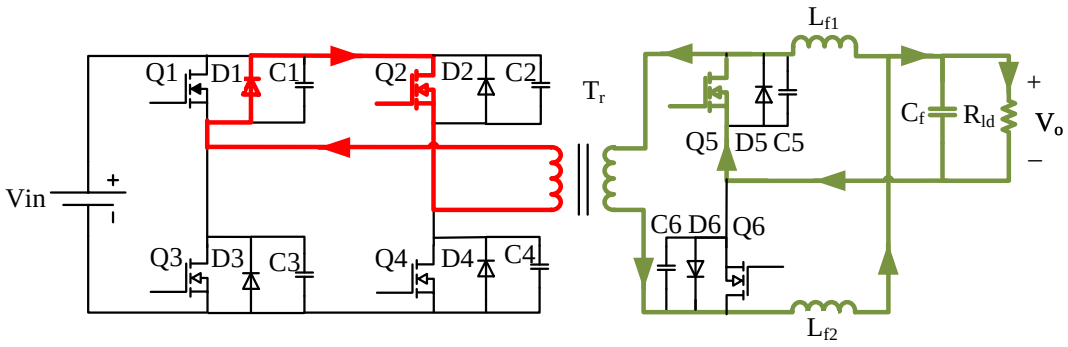
To ensure the zero voltage turn off of Q1, the dead time between Q3 and Q1 has to be larger than t_{31}, which means

$$t_{d31} = (t_7 - t_6) > t_{31} = \frac{(C1 + C3)V_{in}}{i_p} \tag{3-12}$$

On the secondary side, C6 is discharged. When v_{Q6} reaches zero, Q6 also meets the condition for zero voltage turn on.



(a)



(b)

Figure 3.15 Converter Operation Mode from t_6-t_7, (a) before D1 Turns on (b) after D1 Turns on

3.3.9 Converter Operation from t_7 to t_8

This interval is the freewheeling period when no voltage is applied on the transformer (Figure 3.16). At t_7, Q1 and Q6 turn on with zero voltage. On the primary side, current flows between Q1 and Q2. On the secondary side, voltage and current across Q6 are both zero, and current flows through Q5. Currents in both the two output filter inductors decrease, and the decreasing rates are given as:

$$\frac{i_{Lf1}(t) - i_{Lf1}(t_7)}{t - t_7} = \frac{-V_{out}}{L_{f1}}$$

$$\frac{i_{Lf2}(t) - i_{Lf2}(t_7)}{t - t_7} = \frac{-V_{out}}{L_{f2}} \qquad (3\text{-}13)$$

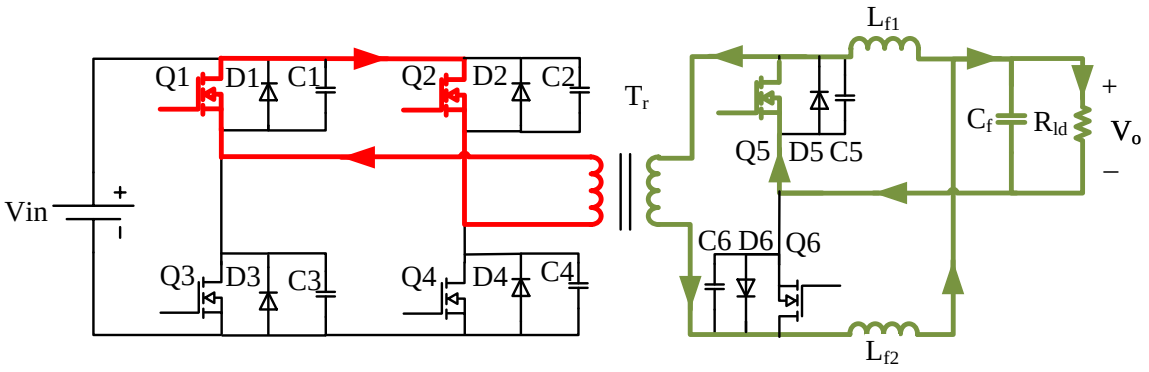
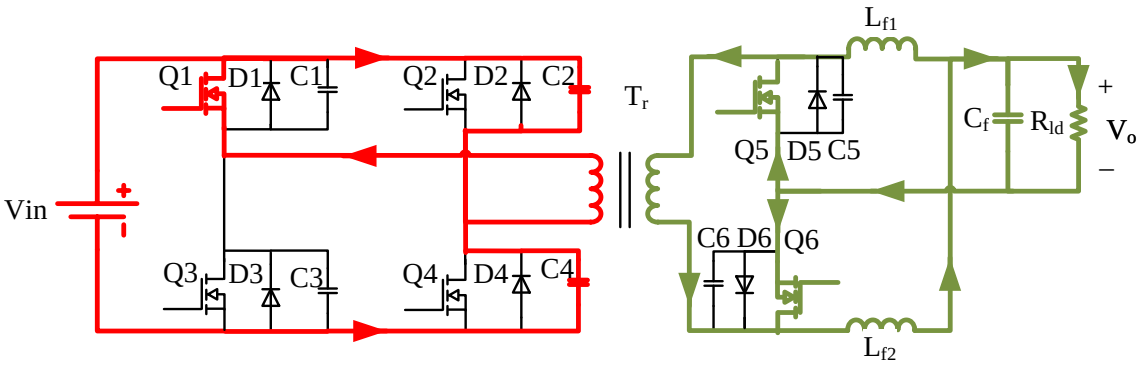


Figure 3.16 Converter Operation Mode from t_7-t_8

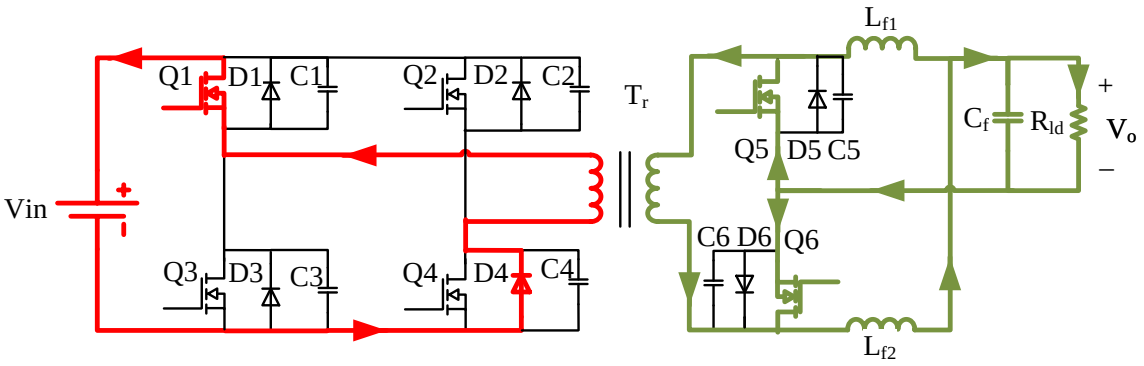
3.3.10 Converter Operation from t_8 to t_9

This is the dead time period between Q2 and Q4. At t_8, Q2 turns off. On the primary side, current discharges C4 from the voltage of V_{in} and charges C2 from zero voltage, as is shown in Figure 3.17(a). This causes the change in transformer voltage direction. When the voltage on C4 is discharged to zero, D4 conducts, which provides the

condition for zero voltage turn on of Q4, as is shown in Figure 3.17(b). On the secondary side, i_{Q5} decreases and i_{Q6} increases [27]. The transformer secondary side is short circuited by Q5 and Q6. Duty cycle loss starts at t_8.



(a)



(b)

Figure 3.17 Converter Operation Mode from t_8-t_9, (a) before D4 Turns on (b) after D4 Turns on

Like in time interval t_3 to t_4, the optimum dead time between Q2 and Q4 is given as:

$$t_{d24} = \frac{\pi}{2}\sqrt{L_{lk}C_{MOS}} \tag{3-14}$$

where $C_{MOS} = C2 = C4$.

3.3.11 Converter Operation from t_9 to t_{10}

Figure 3.18 shows the equivalent circuit in this interval. At t_9, Q4 turns on with zero voltage. During this period, duty cycle loss still exists. The increasing decreasing rates of the primary side current and output filter inductor currents are expressed as:

$$\frac{i_p(t) - i_p(t_9)}{t - t_9} = -\frac{V_{in}}{L_{lk}}$$

$$\frac{i_{Lf1}(t) - i_{Lf1}(t_9)}{t - t_9} = \frac{-V_{out}}{L_{f1}}$$

$$\frac{i_{Lf2}(t) - i_{Lf2}(t_9)}{t - t_9} = \frac{-V_{out}}{L_{f2}} \qquad (3\text{-}15)$$

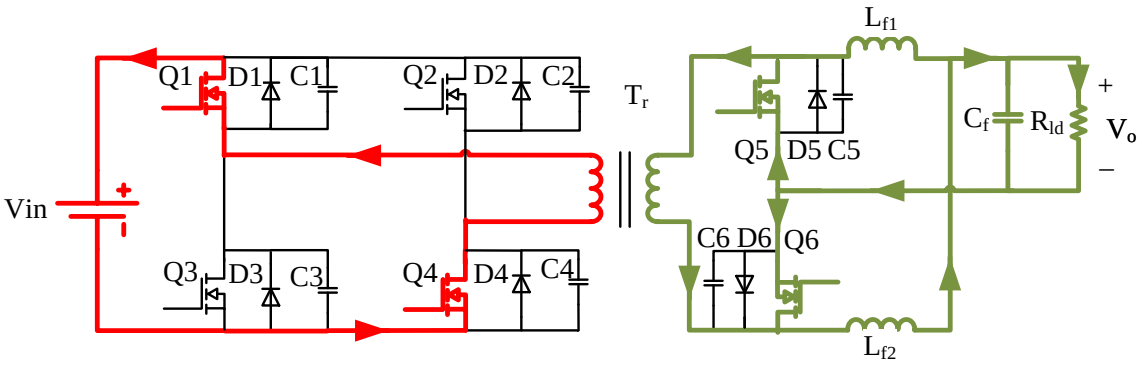


Figure 3.18 Converter Operation Mode from t_9-t_{10}

3.4 **DUTY CYCLE LOSS**

As is described in Section 3.3, duty cycle loss happens because of transformer leakage inductance. Figure 3.19 shows the detailed waveform of i_p, where v_s is the transformer secondary side voltage. As is shown in Figure 3.19, the duration of duty cycle loss is given as:

$$\frac{T}{2}D_{dcl} = \frac{i_{pv} + i_{pm}}{\frac{V_{in}}{L_{lk}}} \tag{3-16}$$

where

$$i_{pv} + i_{pm} = i_{pv} + i_{pp} - \frac{V_{out}}{nL_f}(1 - D)\frac{T}{2} \tag{3-17}$$

As is shown in Figure 3.19, Δi_p corresponds to Δi_{load}, thus $(i_{pv} + i_{pp})/2$ corresponds to i_{load}, and the relationship is given as:

$$\frac{i_{load}}{2} = n\frac{i_{pv} + i_{pp}}{2} \tag{3-18}$$

With (3-16), (3-17) and (3-18), the duty cycle loss is described by:

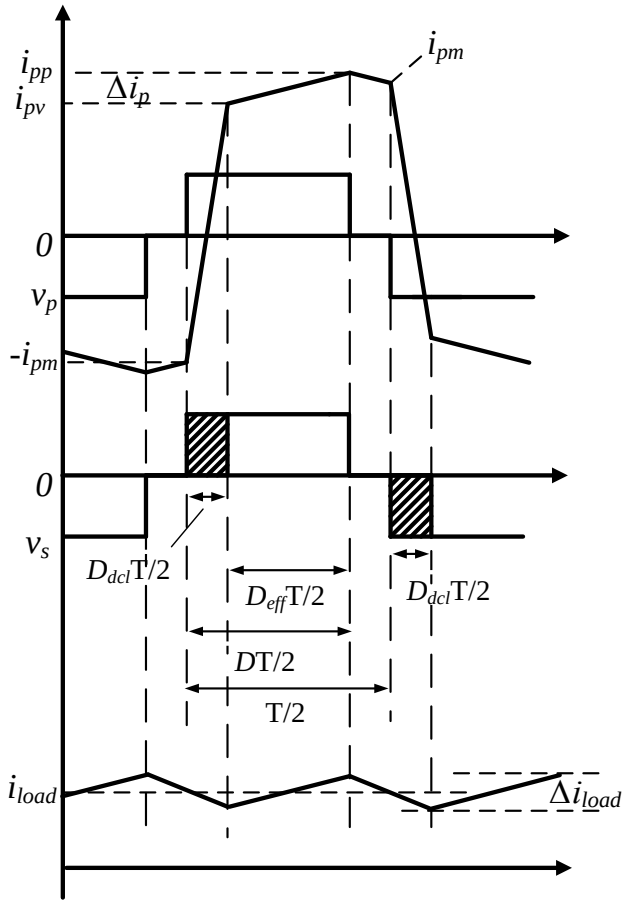


Figure 3.19 Duty Cycle Loss in PSFB with Current Doubler Rectifier

$$D_{dcl} = \frac{2}{T}\frac{L_{lk}}{V_{in}}\frac{1}{n}\left[i_{load} - \frac{V_{out}}{L_f}(1-D)\frac{T}{2}\right] \tag{3-19}$$

When i_{load} is much larger than $V_{out}(1-D)T/(2L_f)$, which is usually the case except for extremely light load condition, the equation can be simplified as:

$$D_{dcl} = \frac{2L_{lk}i_{load}}{nTV_{in}} \tag{3-20}$$

In current doubler topology, the relationship between V_{in} and V_{out} is described by:

$$V_{out} = \frac{\frac{V_{in}}{n} D_{eff}}{2} \tag{3-21}$$

The primary side duty cycle D equals to effective duty cycle (secondary side duty cycle) D_{eff} plus duty cycle loss D_{dcl}, and is described as:

$$D = D_{eff} + D_{dcl} \tag{3-22}$$

With equations (3-20), (3-21) and (3-22), the effective duty cycle can be obtained as:

$$D_{eff} = \frac{Rn^2T}{Rn^2T + L_{lk}} D \tag{3-23}$$

where R is the load resistance,

$$R = \frac{V_{out}}{i_{load}} \tag{3-24}$$

Chapter 4

EXPERIMENTAL VERIFICATION

4.1 INTRODUCTION

This chapter describes the experimental verification of the converter operating principle introduced in Chapter 3. First, converter design specifications are given. Based on the specifications, design considerations of the major components are explained in details. Finally, the experimental results are presented to verify the operation of the converter.

4.2 DESIGN SPECIFICATIONS

The converter design specifications are derived based on the battery voltage and electrical system power ratings in automobiles, and are given as follows:

- input voltage V_{in}: 230-330V
- output voltage V_{out}: 12V
- maximum output power: 2400W
- switching frequency f_s: 100kHZ

To design the 2.4 kW converter, two 1.2 kW converters are designed and they work in an interleaved way to achieve 2.4 kW. The benefits of doing this are to reduce the

output filter requirement and increase the flexibility to extend power ratings. Detailed converter set-up is described in 4.4.1. In Section 4.3, the design is based on the 1.2 kW converter.

4.3 EXPERIMENTAL DESIGN

4.3.1 Resonant Inductor Design

As has been discussed before, the ZVS of Q2 and Q4 requires the resonance between resonant inductor L_r (including leakage inductance L_{lk}) and MOSFET output capacitor C_{MOS}. The desired ZVS range of Q2 and Q4 determines the value of L_r. The design process is explained as follows.

As has been discussed in 3.3.4, at t_3, Q4 turns off. The primary side current discharges C2 and charges C4. When the voltage on C2 is discharged to zero, D2 conducts. To realize zero voltage turn on of Q2, Q2 has to be conducted after D2 conducts, or after the voltage of C2 is discharged to zero. During this period, transformer secondary side is short circuited, and the energy available to discharge C2 is only the energy stored in the resonant inductor. So the leakage inductance has to be large enough to provide adequate energy to charge C4 and discharge C2. The inductance of the resonant inductor has to satisfy [29]

$$L_r i_p^2 > C_{MOS} V_{in}^2 \tag{4-1}$$

where L_r is the resonant inductance, i_p is the primary side current, C_{MOS} is the MOSFET output capacitance, and V_{in} is the input voltage. To realize ZVS at any input voltage, V_{in} should be of the maximum value.

In this work, the ZVS range is selected as 1/3 load to full load. Hence the primary side current is

$$i_{pmin} = \frac{\frac{1}{2} i_{out}}{3 \times n} \tag{4-2}$$

In the proposed converter, this is given as

$$i_{pmin} = \frac{\frac{1}{2} \times 100}{18} = 2.78\ (A) \tag{4-3}$$

The MOSFET output capacitance is selected to be 1500pF. According to (4-1), L_r is calculated to be $21\mu H$. In the experimental prototype, $L_r = 20\mu H$ is selected.

4.3.2 Transformer Turns Ratio Design

According to (3-20), (3-22) and (3-23), the transformer turns ratios *n* is given by:

$$\frac{Rn^2T}{Rn^2T + L_{lk}} D + \frac{2L_{lk} i_{load}}{nTV_{in}} = D \tag{4-4}$$

In (4-4), the primary side duty cycle D should always be less than 1, which means

$$\frac{2i_{load}(Rn^2T + L_{lk})}{nTV_{in}} < 1 \tag{4-5}$$

When selecting the value of *n*, the worst case happens when the load current i_{load} reaches a maximum value (chosen as 100A here) and the input voltage V_{in} reaches a minimum value (230V here) is considered. According to Figure 4.1, the range of transformer turns ratio should be $2.3 < n < 7.3$ with $L_{lk} = 20\mu H$. To fully take benefits of current interleaving at the output, *D* has to be as close as possible to 1. Also, large

value of *n* will reduce the current stress on the switches at the input stage. Therefore, larger n is preferred. Considering design allowance, *n*=6 is selected.

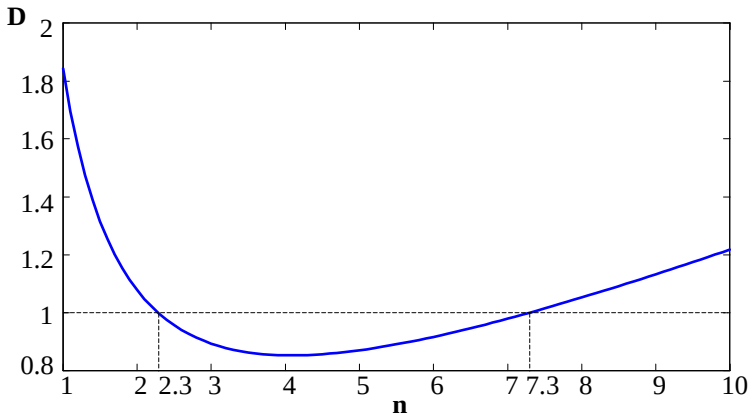


Figure 4.1 Relationship between *D* and *n* with V_{in}=230V, i_{load}=100A

4.3.3 Transformer Turns Number Design

As to transformer design, the primary side number of turns is given by (4-6).

$$N_p = \frac{V_{in} DT}{A_e T_f} \tag{4-6}$$

where A_e is the effective core area and T_f is the magnetic core saturation flux density. EE-55 core with $A_e = 353\ mm^2$ and $T_f = 0.2$ is selected. With (3-20), (3-21) and (3-22), the $V_{in}D$ part in (4-6) is given as (4-7).

$$V_{in}D = V_{in}\left(D_{eff} + D_{loss}\right) = 2nV_{out} + \frac{2L_{lk} i_{load}}{nT} \tag{4-7}$$

The only variable is i_{load}. N_p should satisfy the full load condition, which is given as (4-8).

$$N_p \geq \frac{\left(2nV_{out} + \frac{2L_{lk} \times 100}{nT}\right)T}{A_e T_f} = 29.8 \tag{4-8}$$

For transformer size consideration, N_p is selected as 30. N_s is given as:

$$N_s = \frac{N_p}{n} = 5 \tag{4-9}$$

To finish the design, the filling factor needs to be considered. Filling factor k_f is the ratio of the wire size to the core effective volume, which is given as

$$k_f = \frac{V_p + V_s}{V_e} \tag{4-10}$$

where V_p is the primary wire size, V_s is the secondary wire size, and V_e is the effective volume of the core. Here, for EE-55 core, $V_e = 44000mm^3$. The preferred filling factor is around 0.5.

The primary wire size is determined by the maximum primary side current i_{pmax}, which is given by

$$i_{pmax} = \frac{\frac{i_{out}}{2}}{n} = 8.3A \tag{4-11}$$

Usually, the wire is chosen to endure $3A/mm^2$. For EE-55 bobbin, the perimeter is 80mm. Hence the primary side wire size is

$$V_p = 8.3 \div 3 \times 30 \times 80 = 6667\ mm^3 \tag{4-12}$$

For secondary side, the current is

$$i_{pmax} = \frac{i_{out}}{2} = 50A \tag{4-13}$$

Hence the secondary side wire size is

$$V_s = 50 \div 3 \times 5 \times 80 = 6667\ mm^3 \tag{4-14}$$

The filling factor is then calculated to be

$$k_f = \frac{V_p + V_s}{V_e} = 0.303 \tag{4-15}$$

Considering skin effect, all the wires should be made up of multiple small size conductors. This increases the total wire size. Moreover, with more wires having been winded on the bobbin, the perimeter for wire winding would be larger and the wire size would be larger. Hence the filling factor obtained in (4-9) is desirable and EE-55 core is adopted for this application.

4.3.4 Filter Inductor Design

Usually, the output filter inductor is designed so that the output current ripple is 20% of the output current. For current doubler rectifier, the two inductors work in an interleaved way, and the current ripple on each inductor is 40% of the inductor current. The inductor current ripple is given as:

$$\Delta i_L = \frac{P_{out} \times 0.4}{2 \times V_{out}} = 20A \tag{4-16}$$

For current doubler rectifier, the relationship between inductor value and inductor current ripple is given as [30]:

$$L_f = \frac{V_{out} \times (2 - D)}{2 \times \Delta i_L \times f_s} \tag{4-17}$$

D is between 0-1, so L_f is 3-6 μH. In this prototype, to save size, L_f is selected to be $3\mu H$.

4.3.5 Filter Capacitor Design

The output capacitor is selected to hold the voltage transient when there's a load change [31]. The worse load change is the change from full load to zero load. The capacitor has to make sure that during such a transient, the voltage ripple has to be within 10% of the output voltage.

$$\Delta V_{out} = 0.1 \times V_{out} = 1.2V \tag{4-18}$$

During such a transient, the time it takes the output current to decrease from the maximum current to zero is

$$t_{tr} = \frac{L_f \times i_{out}}{V_{out}} = 25\mu s \tag{4-19}$$

During the transient, most of the current goes to the capacitor equivalent series resistance (ESR). It is assumed that the ESR takes 90% of the transient voltage and the capacitance takes 10% of the transient voltage [31].

$$ESR \leq \frac{0.9 \times \frac{1}{2} \times \Delta V_{out}}{i_{out}} = 5.4m\Omega \tag{4-20}$$

$$C_{out} \geq \frac{i_{out} \times t_{tr}}{0.1 \times \frac{1}{2} \times \Delta V_{out}} = 42mF \tag{4-21}$$

4.3.6 Gate Driver Design

Because of the MOSFET gate drive voltage and current requirement, gate driver is needed to control the MOSFET turn on and turn off. As is shown in Figure 4.2, the gate drive IC gets PWM control signals from the micro-controller and amplifies the control signal. Both the micro-controller and the gate driver is powered by the low voltage (control) system.

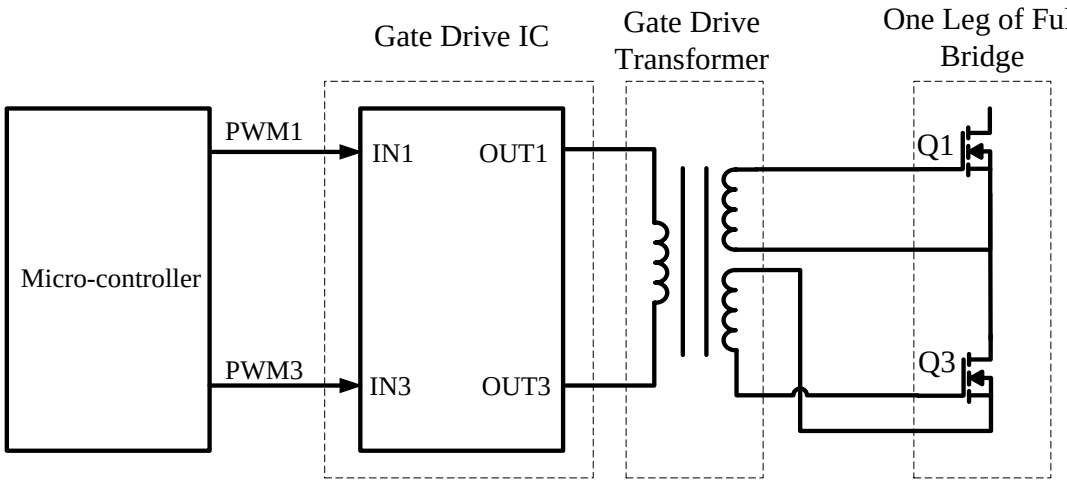


Figure 4.2 Gate Driver for One Leg of Full Bridge

After being amplified by the gate drive IC, the PWM control signals go via the gate drive transformer, and reach the full bridge MOSFET. The reason to use the gate drive transformer is to provide isolation between the low voltage system and the high voltage (power) system. The most important design consideration for the gate drive transformer is the volt second product. The volt second product (ET) is calculated as follows:

$$ET = \frac{V_{dr} D_{on}}{f_s} \tag{4-22}$$

where V_{dr} is the gate drive voltage, D_{on} is the duty cycle of each MOSFET and f_s is the switching frequency. In this application, $V_{dr}$is 12V, D_{on} is fixed 0.5 and f_s is 100 kHz. Hence ET is calculated as 60 $V \cdot \mu s$. A gate drive transformer with ET larger than 60 $V \cdot \mu s$ is desired for this application.

4.4 EXPERIMENTAL RESULTS

4.4.1 Prototype Description

Based on the design considerations described in Section 4.3, the PCB is designed and the converter is built. PCB schematic, PCB layout and bill of materials are presented in Appendix A to Appendix C.

As has been discussed in Section 4.2, two 1.2 kW prototypes are interleaved to achieve 2.4 kW. The converter diagram is shown in Figure 4.3 and the prototype picture is shown in Figure 4.4.

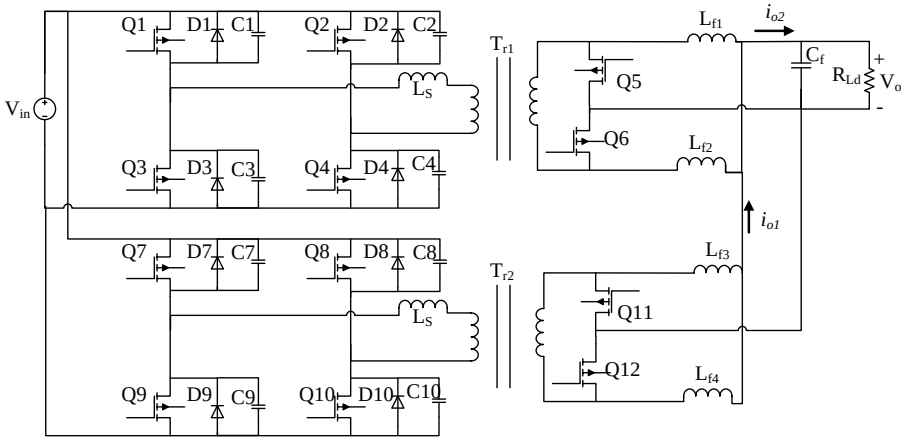


Figure 4.3 Interleaved Full Bridge with Current Doubler Synchronous Rectifier

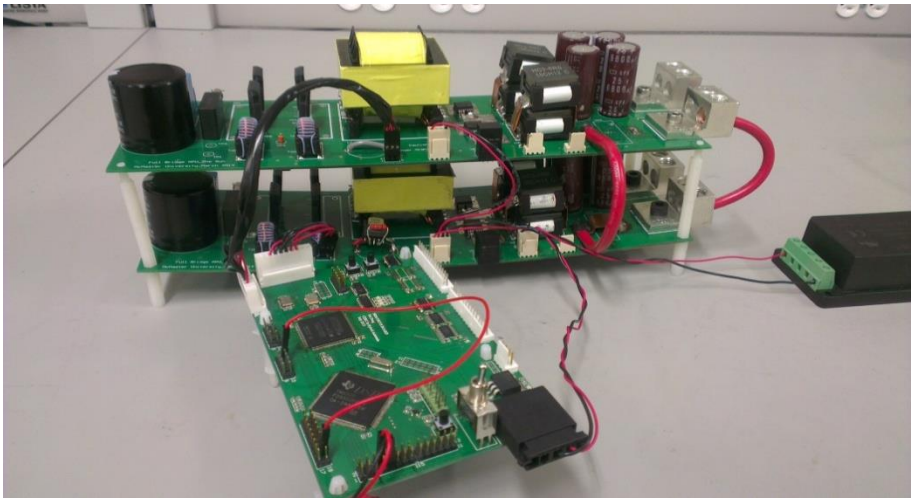
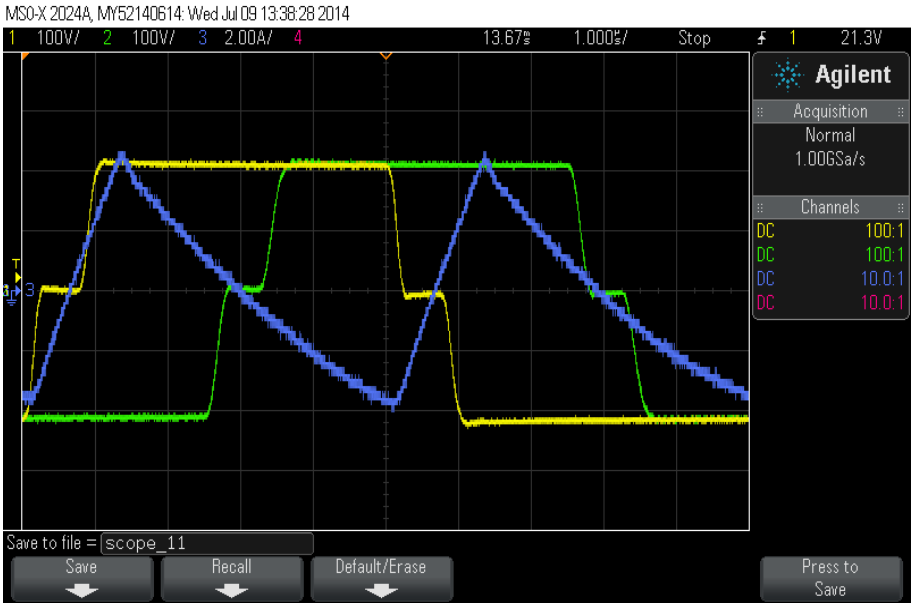
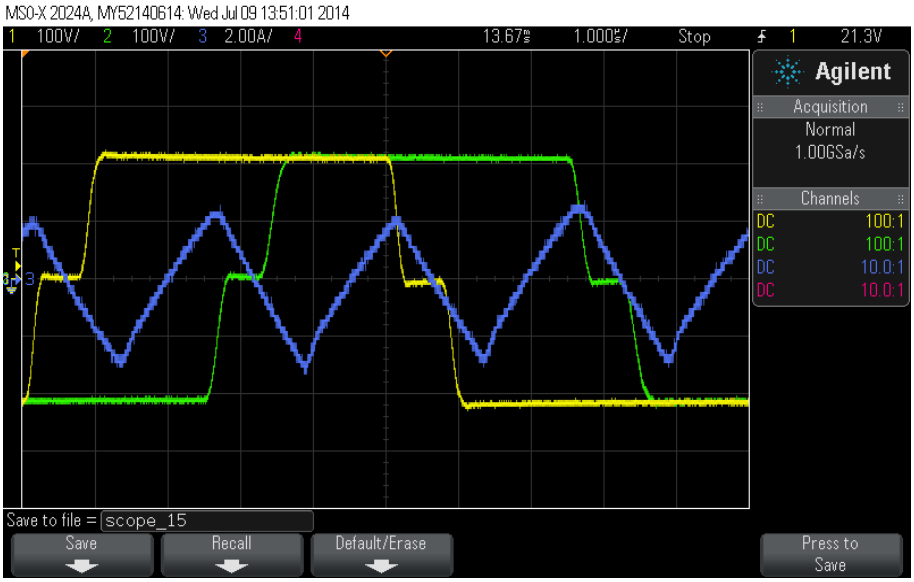


Figure 4.4 Interleaved Converter Prototype

Experiments are conducted to verify the effectiveness of interleaving control scheme. Figure 4.5(a) shows the output current ripple before interleaving, which is the current ripple of i_{o1} in Figure 4.3. Figure 4.5(b) shows the output current ripple after interleaving, which is the current ripple of i_{o2} in Figure 4.3. In Figure 4.5(a) and Figure 4.5(b), Chanel 1 (yellow curve) and Chanel 2 (green curve) respectively stand for the transformer primary side voltage of the two interleaved converters. Chanel 3 (blue curve)



(a)



(b)

Figure 4.5 Output Current Ripple (a) before Interleaving (b) after Interleaving

stands for the output current. Chanel 3 in Figure 4.5(a) stands for i_{o1} and Chanel 3 in Figure 4.5(b) stands for i_{o2}. It is shown that current ripple in Figure 4.5(b) is about half of the current ripple in Figure 4.5(a), which verifies the effectiveness of the interleaved control.

4.4.2 Control Signal Results

The phase shifted full bridge (PSFB) gate drive signals are shown in Figure 4.6. Chanel 1 (yellow), Chanel 2 (green), Chanel 3 (blue) and Chanel 4 (pink) respectively stand for gate drive signals for Q1 to Q4, which are V_{g1} to V_{g4} in Figure 3.7. It is shown that each of the control signal work in 50% duty cycle minus a little dead time. Control signals of Q1 and Q3, or Q2 and Q4 are complementary to each other. Q1 and Q4, or Q2 and Q3 are phase shifted to generate the duty cycle of the system.

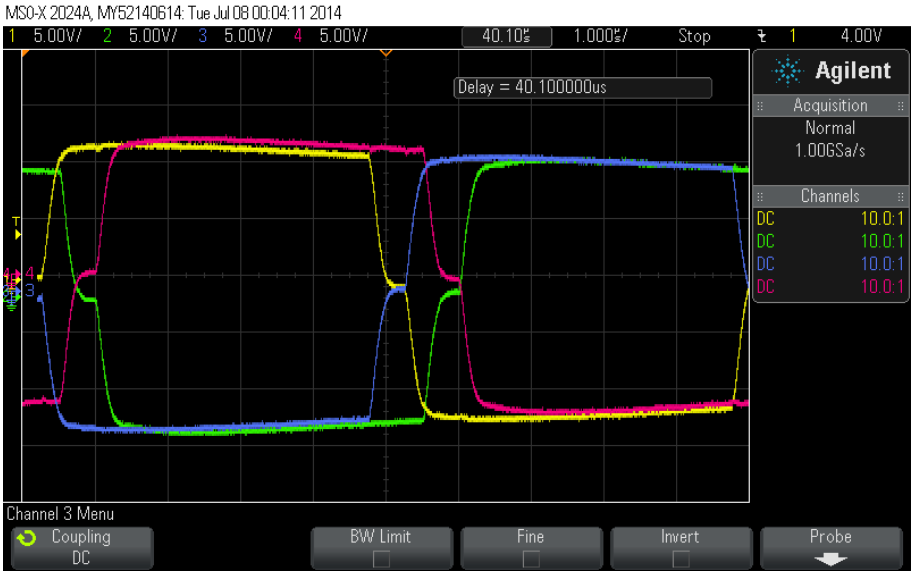


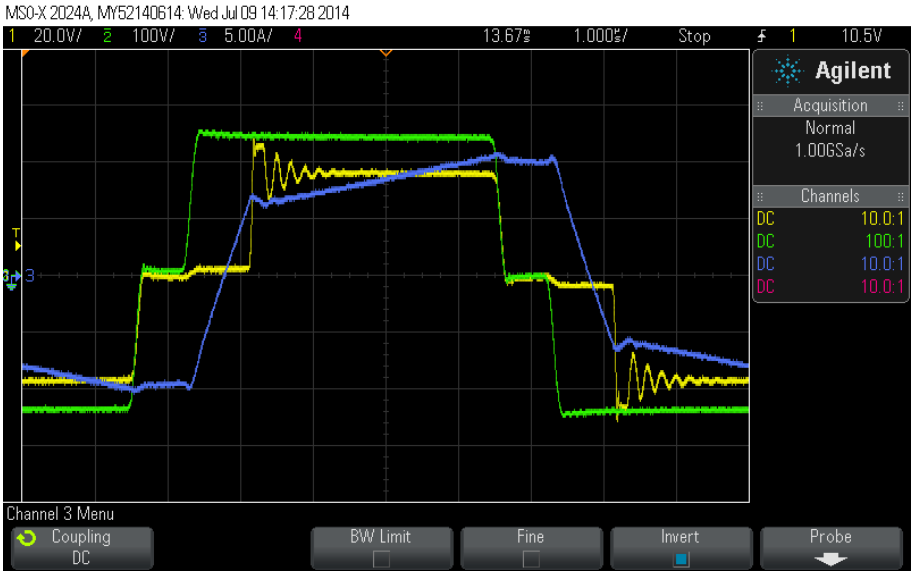
Figure 4.6 Phase Shifted Full Bridge Control

4.4.3 Duty Cycle Loss Results

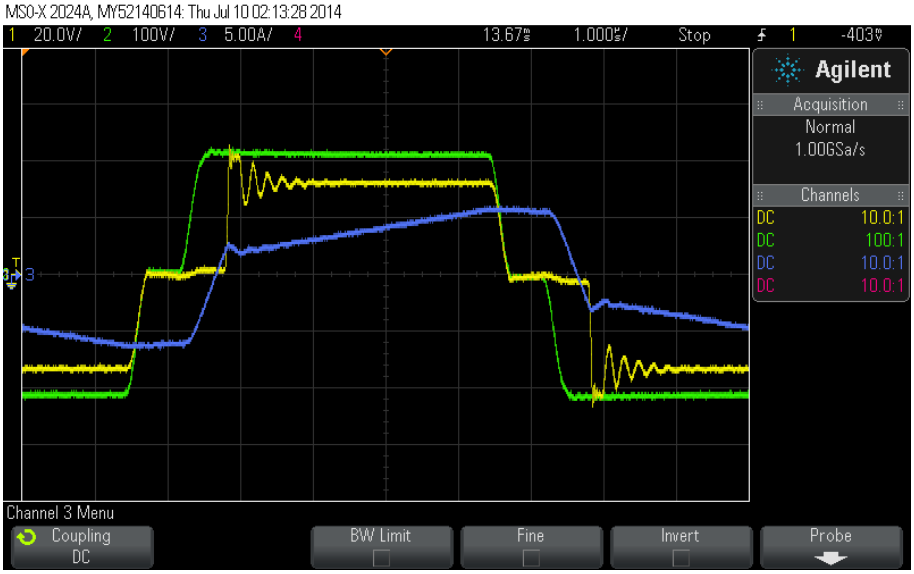
Figure 4.7(a) shows duty cycle loss at full load (1.2 kW) and Figure 4.7(b) shows duty cycle loss at half load (600W). Chanel 1 (yellow) stands for transformer secondary side voltage v_s. Chanel 2 (green) stands for transformer primary side voltage v_p. Chanel 3 (blue) stands for transformer primary side current i_p. In Figure 4.7, the scale for Chanel 3 is 5A/div. It is shown that the peak currents in Figure 4.7(a) and Figure 4.7(b) are 10A and 5A respectively.

From Figure 4.7 it is seen that:

- The characteristics of v_p, v_s and i_p agree with the waveforms shown in Figure 3.7, which verifies the operation of PSFB.
- Secondary side duty cycle is lost when i_p rises or drops sharply. According to 3.3.5, the rising or dropping rate of i_p is V_{in}/L_{lk}
- Duty cycle loss period is larger in full load than in half load. This can be seen from Equation (3-20). The equation show that D_{dcl} is proportional to i_{load}, which results in larger duty cycle loss in Figure 4.7(a) than Figure 4.7(b).



(a)



(b)

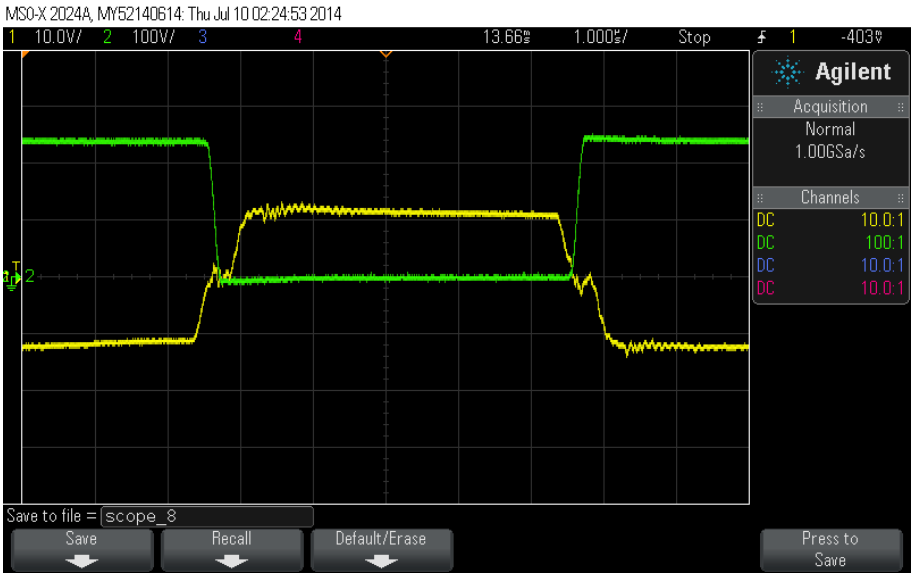
Figure 4.7 Duty Cycle Loss at (a) Full Load (b) Half Load

4.4.4 ZVS Conditions

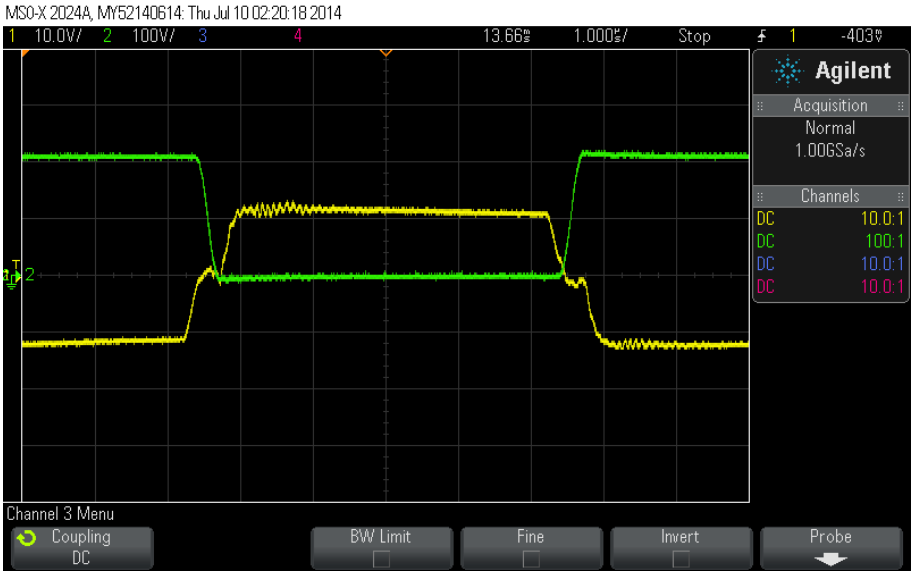
Figure 4.8(a), Figure 4.8(b) and Figure 4.8(c) respectively show the ZVS condition of Q1 at full load, half load and quarter load. In Figure 4.8, Chanel 1 (yellow) stands for gate drive voltage of Q1, which is V_{g1}. Chanel 2 (green) stands for the drain to source voltage of Q1.

From Figure 4.8, it is seen that Q1 can achieve ZVS at full load and half load conditions. At quarter load, Q1 can marginally achieve ZVS. This is because the primary side current i_p in quarter load condition is smaller. According to Equation (3-5), with a smaller i_p, the dead time between Q1 and Q3 should be larger.

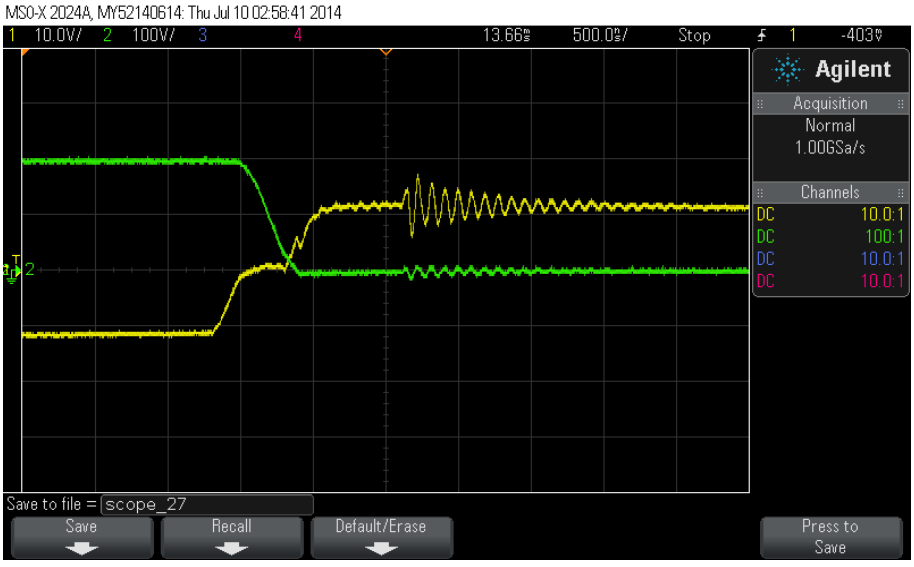
For Q3, the ZVS conditions are the same as those of Q1.



(a)



(b)



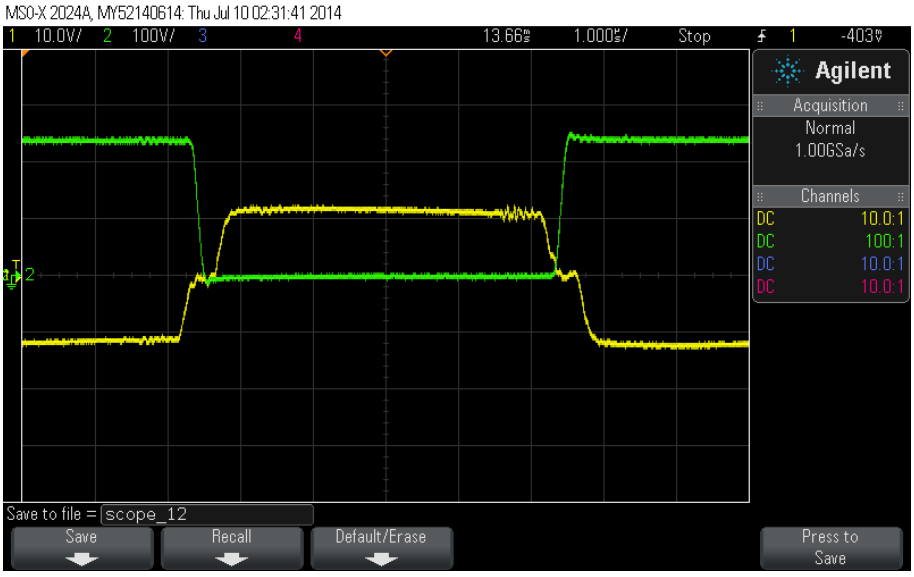
(c)

Figure 4.8 ZVS Condition of Q1 at (a) Full Load (b) Half Load (c) Quarter Load

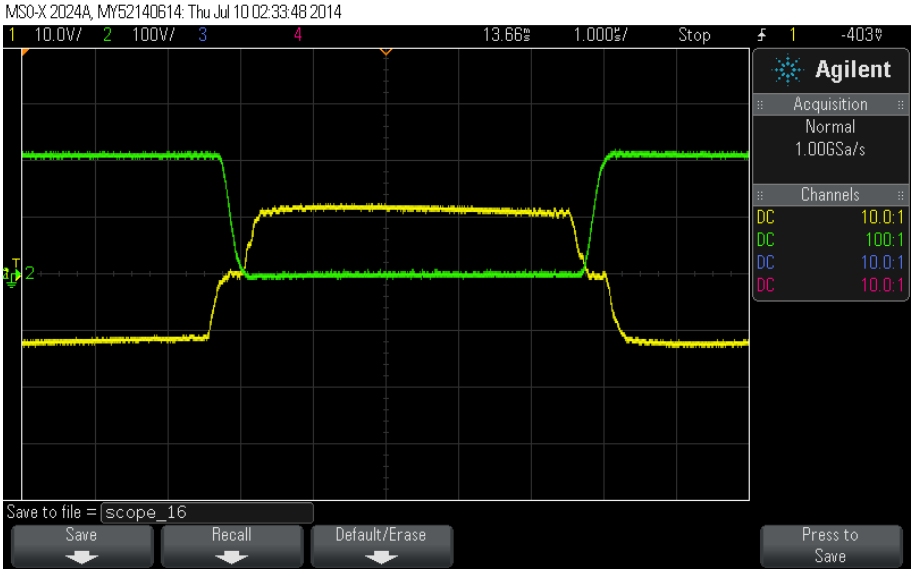
Figure 4.9(a), Figure 4.9(b) and Figure 4.9(c) respectively show the ZVS condition of Q2 at full load, half load and quarter load. In Figure 4.9, Chanel 1 (yellow) stands for gate drive voltage of Q2, which is V_{g2}. Chanel 2 (green) stands for the drain to source voltage of Q2.

From Figure 4.9, it is seen that:

- At full load and half load, Q2 can achieve ZVS. At quarter load, Q2 cannot achieve ZVS. This is mainly because for Q2, energy used to provide ZVS conditions are merely from the resonant inductance (including the leakage inductance), as is discussed in 3.3.4. If the load is low, there might not be enough energy for Q2 to achieve ZVS. According to 4.3.1, the resonant inductor is designed for Q2 to achieve ZVS for 1/3 load or above, hence ZVS is lost in quarter load conditions.
- As is seen from Figure 4.9(c), when the MOSFET loses ZVS, the drain to source voltage drops sharply. This results from the sudden turn on of the MOSFET. During the sudden turn on period, the energy stored in MOSFET parallel capacitors is lost in heat. Moreover, the sudden switching of MOSFET causes large EMI, which affects the converter operation.


MSO-X 2024A, MY52140614: Thu Jul 10 02:31:41 2014
1 10.0V/ 2 100V/ 3 4
13.66s 1.000s/ Stop
1 -403V
Agilent
Acquisition
Normal
1.00GSa/s
Channels
DC 10.0:1
DC 100:1
DC 10.0:1
DC 10.0:1
Save to file = scope_12
Save
Recall
Default/Erase
Press to Save

(a)


MSO-X 2024A, MY52140614: Thu Jul 10 02:33:48 2014
1 10.0V/ 2 100V/ 3 4
13.66s 1.000s/ Stop
1 -403V
Agilent
Acquisition
Normal
1.00GSa/s
Channels
DC 10.0:1
DC 100:1
DC 10.0:1
DC 10.0:1
Save to file = scope_16
Save
Recall
Default/Erase
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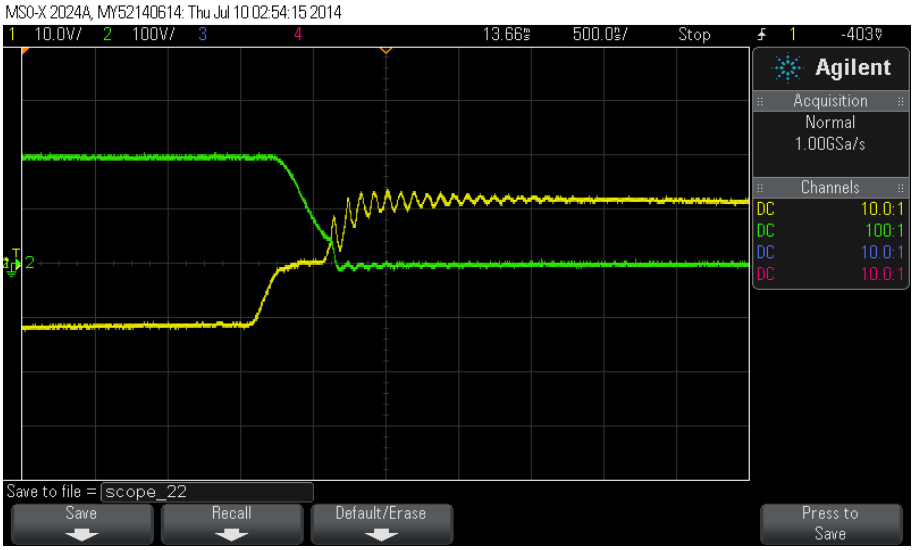
(b)



(c)

Figure 4.9 ZVS Condition of Q2 at (a) Full Load (b) Half Load (c) Quarter Load

Chapter 5

ZERO CURRENT SWITCHING (ZCS) SYNCHRONOUS RECTIFICATION (SR)

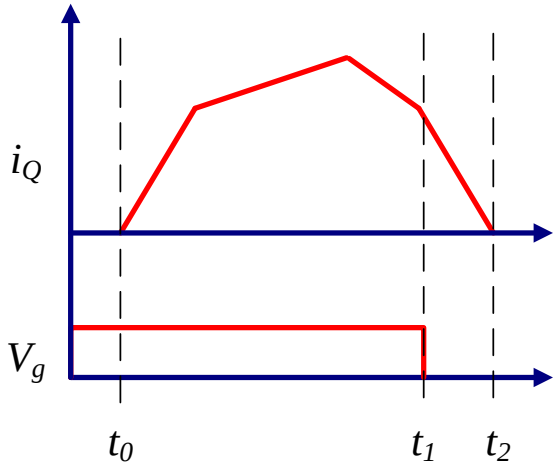
5.1 INTRODUCTION

From Chapter 2 to Chapter 4, a phase shifted full bridge DC/DC converter with current doubler synchronous rectifier (SR) is designed for auxiliary power units. The proposed converter is able to carry large output current for APU, and is also able to achieve zero voltage switching with a wide range of load conditions. However, due to the large current at the converter secondary side, power loss at the secondary side is still high. In this chapter, a zero current switching (ZCS) SR control method is proposed to reduce the power loss on the SR MOSFETs.

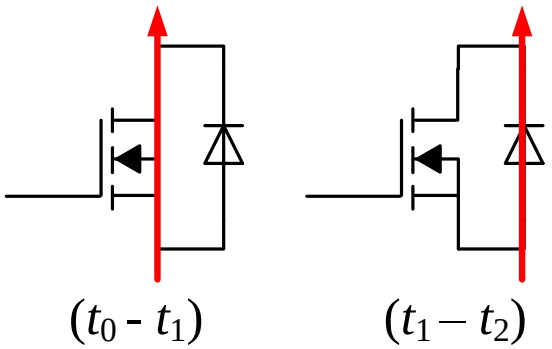
As has been discussed in 2.4.4, replacing diode rectifiers with MOSFET rectifiers can greatly reduce power loss, since conduction loss in MOSFETs is much less than that in diodes. However, in practical applications, MOSFETs might not be able to completely replace diodes due to the control scheme.

Figure 5.1 shows the condition when the SR MOSFET turns off at non-zero current. In Figure 5.1(a), i_Q stands for the MOSFET current, and V_g stands for the MOSFET gate drive voltage. The MOSFET turns off at t_1, when the MOSFET current is

not zero. Figure 5.1(b) shows that the current goes through the MOSFET from t_0 to t_1, and has to transfer to the MOSFET body diode from t_1 to t_2. From t_1 to t_2, the power loss is increased because of the much larger conduction loss in the diode.



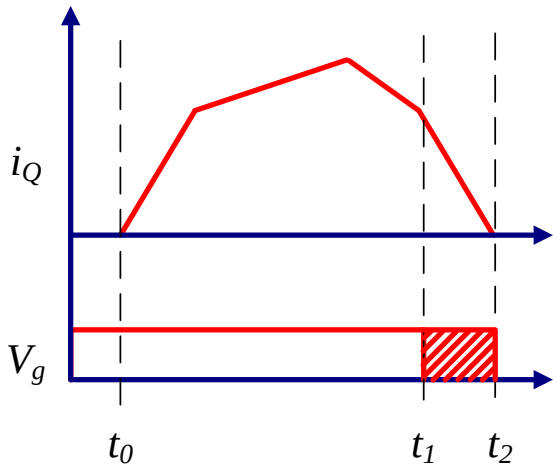
(a)



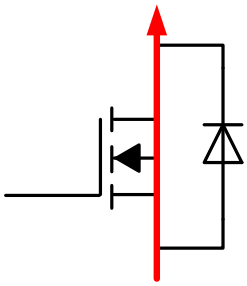
(b)

Figure 5.1 SR MOSFET Non-zero Current Turn off (a) Waveforms (b) Current Flow

Figure 5.2 shows the condition when the SR MOSFET turns off at zero current. In Figure 5.2(a), The MOSFET turns off at t_2, when the MOSFET current is not zero. Figure 5.1(b) shows that the current always goes through the MOSFET from t_0 to t_2. Hence the MOSFET power loss in condition shown in Figure 5.2 is much less than that in Figure 5.1.



(a)



(b)

Figure 5.2 SR MOSFET Zero Current Turn off (a) Waveforms (b) Current Flow

Comparing Figure 5.1 and Figure 5.2, it is seen that to minimize the power loss on SR MOSFET, the MOSFET on-time should be maximized. In the following of this chapter, it is shown that the MOSFET on-time is not maximized in the conventional SR control scheme. Then a ZCS SR control scheme is proposed to maximize the MOSFET on-time.

5.2 CONVENTIONAL SYNCHRONOUS RECTIFICATION CONTROL

Generally, there are two ways for SR control: externally driven and self-driven [32]. For externally driven, the SR driven signals are derived from external circuits. A typical externally driven method is shown in Figure 5.3. For self-driven, the SR is directly driven by the transformer secondary side voltage. In PSFB, transformer secondary side voltage is zero during freewheeling period, and cannot be utilized to drive SR [33]. Therefore, externally driven is widely used in SR control in PSFB [27], [31]-[33].

Figure 5.4 shows the conventional SR control scheme and Figure 5.5 shows the corresponding converter waveform [27], [31]-[33]. In Figure 5.4 and Figure 5.5, V_{g1} to V_{g6} represent control signals of Q1 to Q6, respectively. It is shown that SR control signals have logic relationship with the full bridge control signals. Moreover, Q5 and Q6 are turned on and turned off with zero voltage. However, this control scheme does not consider the time between t_3-t_5, or t_8-t_9. As is shown in Figure 5.5, at t_3, Q6 turns off. However, i_{Q6} has not decreased to zero at this time. This current then transfers from the

MOSFET Q6 to its body diode D6. This causes a larger conduction loss since D6 has a much larger forward voltage than Q6.

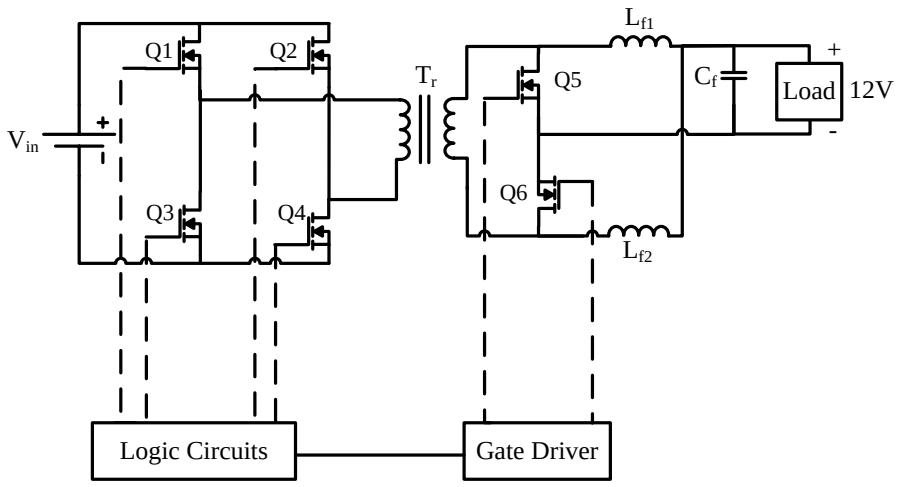


Figure 5.3 Externally Driven SR Control

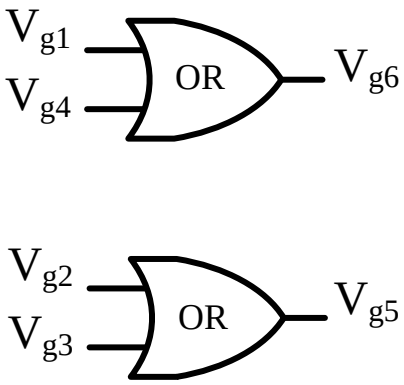


Figure 5.4 Conventional SR Control Scheme

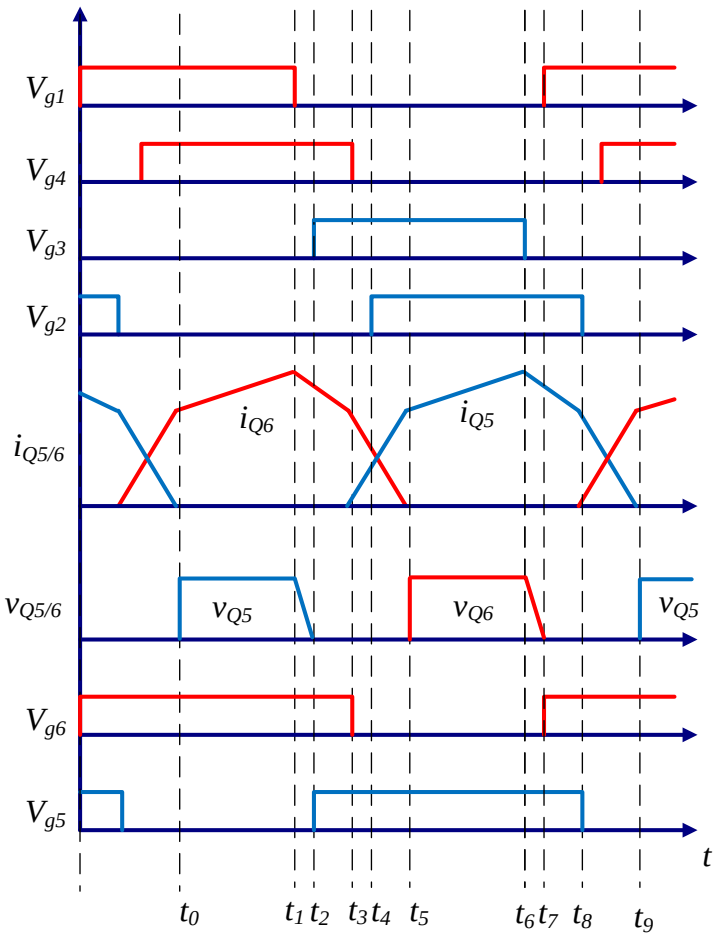


Figure 5.5 Conventional SR Control Waveform

5.3 PROPOSED SYNCHRONOUS RECTIFICATION CONTROL

The problem mentioned in Section 5.2 can be solved by delaying the Q6 turn off time from t_3 to t_5. The delay time t_{dcl} is the duty cycle loss time. With (3-20), t_{dcl} can be expressed as:

$$t_{dcl} = \frac{T}{2} D_{dcl} = \frac{L_{lk} i_{load}}{n V_{in}} \tag{5-1}$$

It is worth noting that if Q6 does not completely turn off at t_5, duty cycle loss will continue as the secondary side of the transformer will be kept to 0 by Q6, which is not desirable. Hence, in practice, the MOSFET turn off delay time $t_{d(off)}$ and fall time t_f should be deducted from t_{dcl}. As a result, the final control scheme and corresponding waveforms are shown in Figure 5.6 and Figure 5.7.

As is shown in (5-1), to obtain t_{dcl}, the average values of load current i_{load} and input voltage V_{in} are required. i_{load} can be obtained from the current sensor, which is already installed for current control. V_{in} can be described by (5-2), according to (3-21) and (3-23)

$$V_{in} = 2nV_{out}\frac{Rn^2T + L_{lk}}{DRn^2T} \tag{5-2}$$

From (5-2) can be seen that t_{dcl} can be determined from the measurements of V_{out}, which is usually already available for the control loop of the output voltage. Hence, the proposed method does not require extra sensors if both a current and voltage loops are used to control the converter.

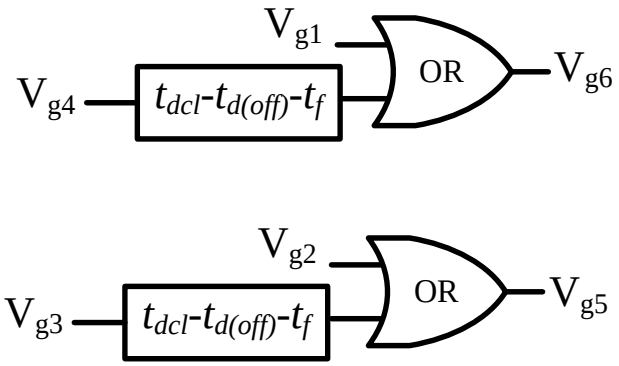


Figure 5.6 Proposed SR Control Scheme

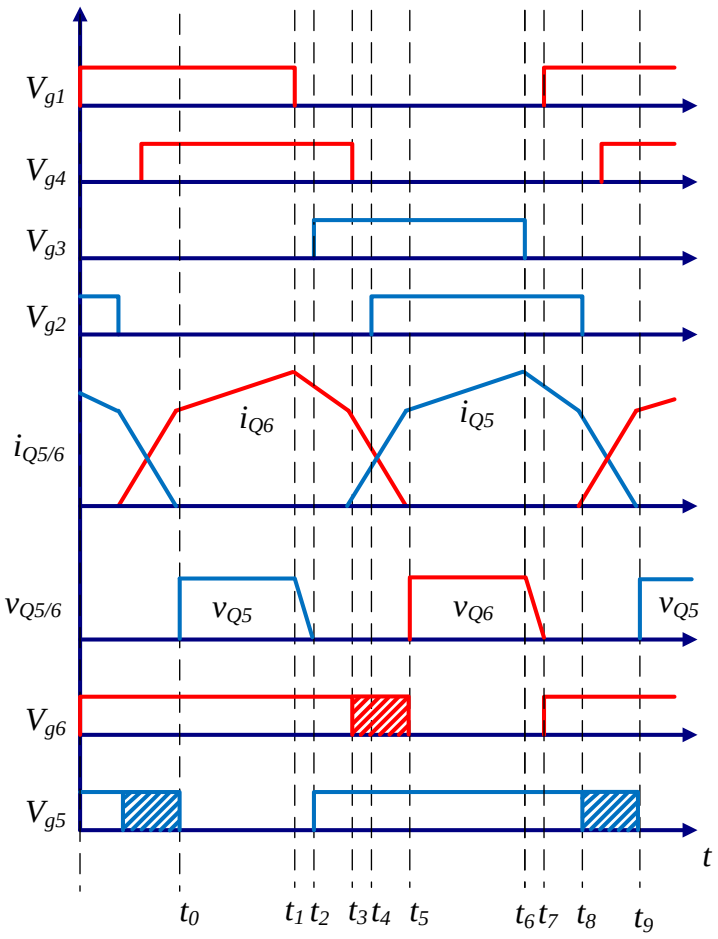


Figure 5.7 Proposed SR Control Waveform

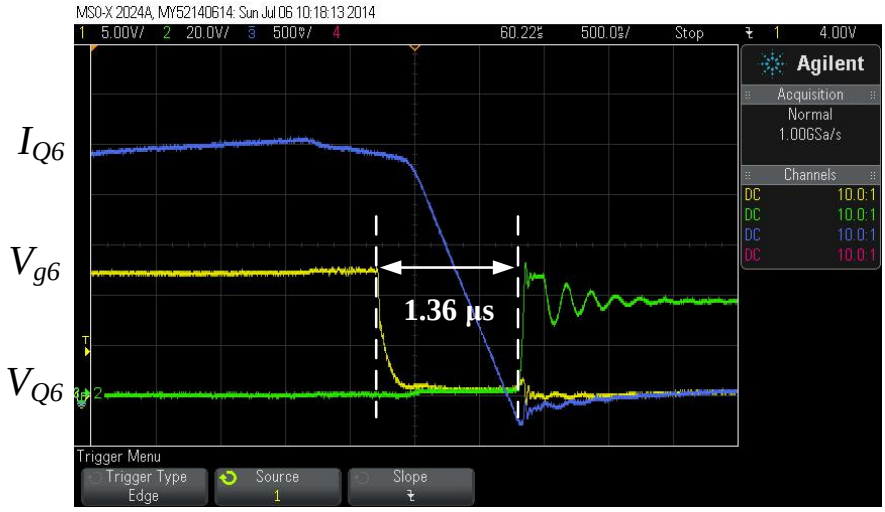
5.4 EXPERIMENTAL VERIFICATION

Experiments are conducted with input voltage of 244.8V, which is the voltage of Camry 2012 high voltage battery [19]. Figure 5.8 shows the SR waveform of conventional control and proposed control at 100A output current. Open-loop implementation of the proposed SR control has been tested, and Figure 5.9 shows the efficiency comparison between conventional SR control scheme and proposed SR control scheme under various load conditions. It is worth mentioning that for the MOSFET

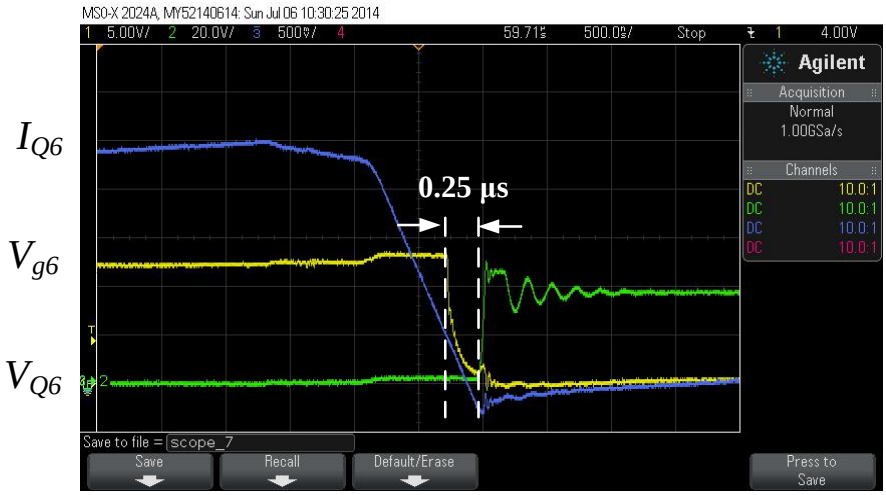
current measuring in Figure 5.8, to reduce the impact of current transducer to the circuit, only 1/5 of the MOSFET current is measured with a 0.1V/A current transducer.

For Figure 5.8, the duty cycle loss time is $1.36\ \mu s$ according to (5-1). As is shown in Figure 5.8(a), Q6 turns off when the MOSFET currents are high. To minimize MOSFET conduction loss, Q6 should be turned off as close to the zero current point as possible. In Figure 5.8(b), considering the MOSFET turn off delay time and fall time, Q6 is turned off $0.25\ \mu s$ before the zero current point, according to the datasheet of AUIRFS8409-7P. The results verify the calculation in (5-1).

The efficiency comparison between conventional SR control method and proposed SR control method is shown in Figure 5.9. As is shown in Figure 5.9, efficiency is improved by up to 0.9% thanks to the proposed SR control method. Efficiency is better improved in heavy load conditions than light load conditions, because with heavier load, the duty cycle loss time and MOSFET current are larger.



(a)



(b)

Figure 5.8 Experimental Results of PSFB with Synchronous Rectifier at V_{in}=244.8V, i_{load} =100A under (a) Conventional SR Control Scheme (b) Proposed Control Scheme. Scales: Ch1: 5V/div, Ch2: 20V/div, Ch3: 0.5V/div, Time Scale: 0.5us/div

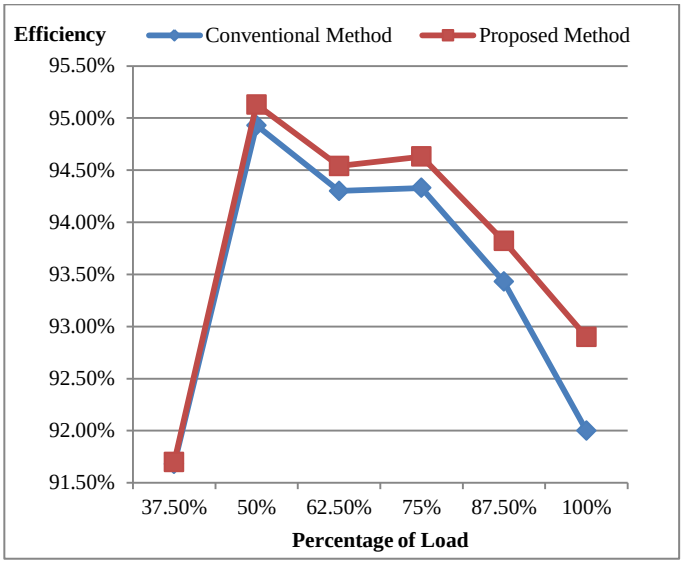


Figure 5.9 Experimental Results of Efficiency Comparison between Conventional SR Control Method and Proposed SR Control Method at V_{in}=244.8V

Chapter 6

CONCLUSION

6.1 MAJOR CONTRIBUTIONS

In this thesis, a phase shifted full bridge (PSFB) DC/DC converter with current doubler synchronous rectifier (SR) for auxiliary power units (APU) is discussed. The converter operation and design considerations are presented. Moreover, a zero current switching (ZCS) SR control scheme is proposed. The major contributions of the thesis are as follows.

First, detailed topology selection and design considerations specifically for APU applications are presented. The topology selection is based on the analysis of existing APU in hybrid electric vehicles (HEVs) and electric vehicles (EVs). The converter design considerations are to meet the specific requirements for APU applications.

Second, a ZCS SR control scheme for PSFB is proposed. The proposed SR control scheme is not available in literature. The equations to achieve the ZCS SR control scheme are presented. Practical design considerations are explained. The application requirements for the control scheme are analyzed. Comparison of conventional and proposed SR control scheme is conducted. Experimental results are given to verify the effectiveness of the proposed control scheme.

6.2 SUMMARY OF THESIS

In Chapter 2, APU in aircraft and commercial trucks is introduced, and APU in HEVs and EVs is researched on in details. From the analysis of APU in industry, three requirements are considered for topology selection. First, from the isolation requirement, high frequency transformer is adopted. Second, based on the power rating requirements, full bridge topology is adopted for the primary side of the converter. Third, based on the high output current requirements of APU, current doubler rectifier and synchronous rectifier are adopted for the secondary side of the converter.

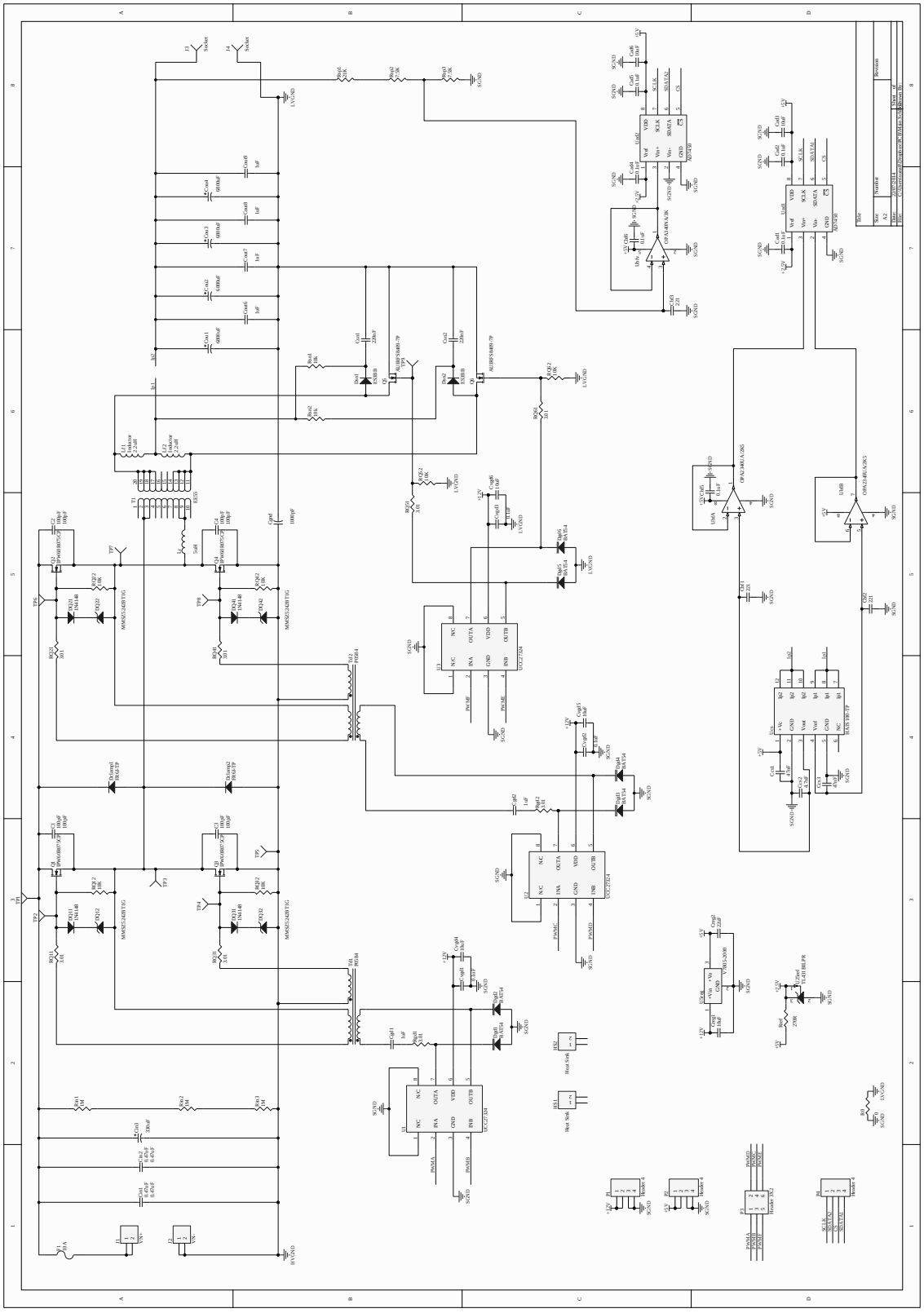
In Chapter 3, the operation of proposed converter is described in details. First, the concept of soft switching is introduced. Then the converter operation is described in ten operation states. The equations for primary side current and output inductor currents are given. Soft switching conditions for different full bridge MOSFETs are described and the equations of dead time are presented. At last, the equations for duty cycle loss and effective duty cycle are given, which lay foundations for the transformer design in Chapter 4 and ZCS SR control in Chapter 5.

In Chapter 4, a 2.4 kW converter design example is given and the experimental results are presented. The experimental results show that the converter is able to work in the desirable way. First, the interleave control effectively reduced the output current ripple. Second, the converter voltage and current waveforms agree with the waveforms of PSFB. Third, the full bridge MOSFETs are able to achieve ZVS in a desirable range of loads.

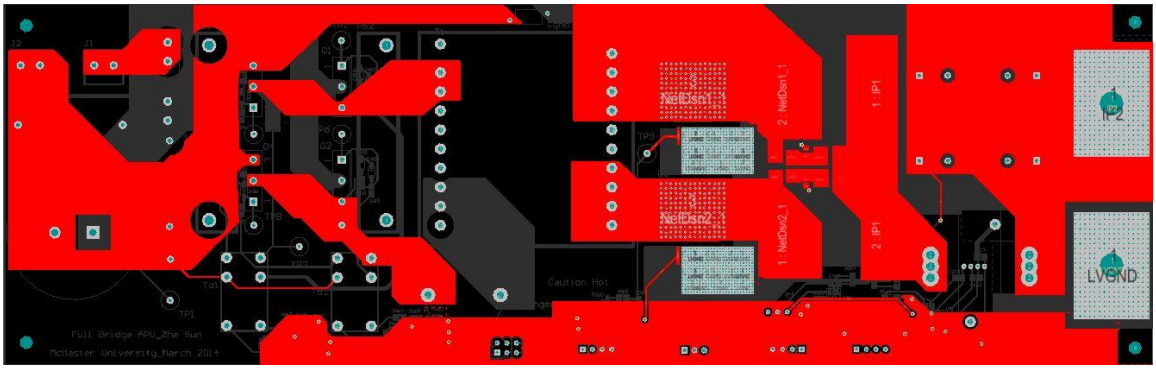
In Chapter 5, a ZCS SR control scheme is proposed for PSFB in APU applications. Conventional SR control scheme and proposed SR control scheme are compared. Experimental results show that the proposed SR control scheme is applicable to the converter. Measured efficiency map demonstrates that the proposed control scheme can improve the converter efficiency, especially at heavy load conditions when the conduction loss at the output stage is the highest.

Appendix

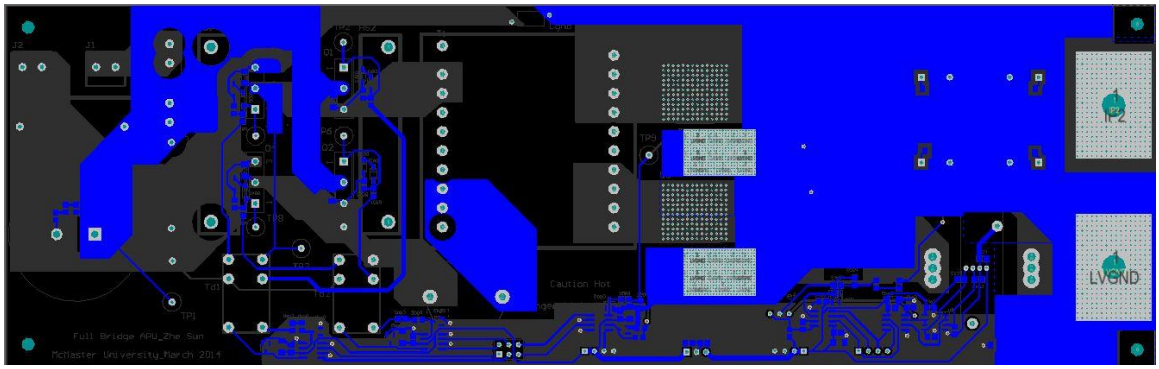
APPENDIX A
SCHEMATIC OF THE EXPERIMENTAL SET-UP



APPENDIX B
PCB LAYOUT OF THE EXPERIMENTAL SET-UP



PCB Layout of Top Layer



PCB Layout of Bottom Layer

APPENDIX C
BILL OF MATERIALS OF THE EXPERIMENTAL SET-UP

Component	Value	Footprint
C1, C2, C3, C4	100pF	C1206
Cad1, Cad2, Cad4, Cad5, Cbf5, Cbf6, Cvgd1, Cvgd2, Cvgd3	0.1uF	C0805
Cad3, Cad6, Cvgd4, Cvgd5, Cvgd6	10uF	C1206
Cbf1, Cbf2, Cbf3	221	C0805
Ccs1, Ccs3	47nF	C0805
Ccs2	4.7nF	C0805
Cgd1, Cgd2	1uF	C0805
Cgnd	1000pF	Ceramic disk 10mm
Cin1	0.47uF	10uF MKP
Cin2	0.47uF	EMI CAP
Cin3	330uF	CAPPRS10-35x35
Cou1, Cou2, Cou3, Cou4	6800uF	CAPPR7.5-18x41.5
Cout6, Cout7, Cout8, Cout9	1uF	C1206
Creg1	10uF	C0805

Creg2	22uF	C0805
Csn1, Csn2	220nF	C0805
Dclamp1, Dclamp2	FR6J-TP	SMC
Dgd1, Dgd2, Dgd3, Dgd4, Dgd5, Dgd6	BAT54	SOT-23
DQ11, DQ21, DQ31, DQ41	1N4148	SOD-123
DQ12, DQ22, DQ32, DQ42	MMSZ5242BT1G	SOD-123
Dsn1, Dsn2	ES3BB	SMB
F1	10A	FC-211 Fuse Hoder
HS1, HS2	Heat Sink	Heat Sink
J1	VN+	ED120/2DS
J2	VN-	ED120/2DS
J3, J4	Socket	LAM2A Lug
Lf1, Lf2	Inductor	HC3 PW INDUC
Lr	Inductor	POTENTIAL INDUC
P1, P2, P4	Header 4	HDR1X4
P3	Header 3X2	HDR2X3

Q1, Q2, Q3, Q4	IPW60R075CP	TO-247
Q5, Q6	AUIRFS8409-7P	D2PAK-7
R0	0	R1206
Rgd1, Rgd2, RQ11, RQ21, RQ31, RQ41, RQ51, RQ61	3.01	R0805
Rin1, Rin2, Rin3	1M	R0805
RQ12, RQ22, RQ32, RQ42, RQ52, RQ62	10K	R0805
Rref	270R	R0805
Rsn1, Rsn2	10k	R2512
Rsp1	21K	R0805
Rsp2, Rsp3	7.5K	R0805
T1	EE55	EE55
Td1, Td2	P0584	P0584
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	Socket	Test Point
U1, U2, U3	UCC27324	8-SOIC

U5reg	V7805-2000	V78XX-2000
U25ref	TL431BILPR	TI-LP3
Uad1, Uad2	AD7450	8-SOIC
Ubf	OPA2340UA/2K5	TI-D8_N
Ubfv	OPA340NA/3K	TI-DBV5_N
Ucs	HAIS 100-TP	HAIS 100-TP

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